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NVAX: A High Performance Single Chip VAX Microprocessor

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May 5, 1992 VA171

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Presentation Outline

- What is NVAX?
- CPU Comparisons
- NVAX Design Goals
- NVAX Chip Overview
- NVAX Chip Internals
- Functional Results
- Performance Results
- Conclusions

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What Is NVAX?

- A Single-Chip VAX Microprocessor
- Designed to make use of high-performance RISC-like microarchitectural techniques as applied to the VAX CISC architecture
- Implemented in an advanced CMOS technology
- Used in multiple system environments

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What Is NVAX?
High-Performance Design

- VAX 9000 architectural heritage
- NVAX Ibox acts as a front-end to a RISC-like pipeline with multiple functional units
- On-chip Translation Buffer (TB), Virtual Instruction Cache (VIC), and Primary Cache (Pcache)
- On-chip controller for writeback Backup Cache (Bcache)

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VAX 9000: FIRST MACROPIPELINED VAX - TAKE HIGH LEVERAGE IDEAS, EXPLOIT CMOS

USE RISC IMPLEMENTATION TECHNIQUES TO IMPROVE PERFORMANCE

What Is NVAX?
Advanced CMOS Technology

- 0.75 µm, 3-metal layer, 3.3v CMOS-4 technology with support for 5v input signals
- CMOS-4 process is optimized for high-performance microprocessors, is fully qualified, robust and reliable, and in volume production
- Same process used for Alpha 21064 (EV-4) chip

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SHORT CHANNEL LENGTH = 0.5µm

NOT EXOTIC; OPTIMIZED

Slide No. 5

What is NVAX?
Advanced CMOS Technology, cont.

- 71.4 MHz (14ns) and 83.3 MHz (12ns) operation—better than most industry RISC chips
- 1.3M transistors, 16.2mm x 14.6mm die size
- 339-pin thru-hole PGA package

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What Is NVAX?
Multiple System Environments

- **VAX 4000-500**: 71.4 MHz (14ns) operation, 128KB Bcache
- **VAX 6000-600**: 83.3 MHz (12ns) operation, 2MB Bcache

The *same* NVAX chip is used in all system environments.

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ANNOUNCED PRODUCTS ONLY. ADDITIONAL SYSTEMS TO BE DISCUSSED IN NTG NEXT FUTURE

NOTE 16:1 BCACHE SIZE RATIO

MENTION COUGAR "TECHNOLOGY DISPLAY"

CPU Comparisons

	VAX 6000-500	NVAX Systems	VAX 9000-400
CPU Speed	62.5 MHz (16 ns)	**71.4 MHz (14ns)— 83.3 MHz (12ns)**	62.5 MHz (16 ns)
Pipeline	Micro	**Macro**	Macro
Branch Prediction	None	**512x4 bit, 1 outstanding**	1024x1 bit, 2 outstanding, target buffer

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CPU Comparisons, cont.

	VAX 6000-500	NVAX Systems	VAX 9000-400
TB	64 entries, fully associative	**96 entries, fully associative**	1024 entries, split, direct mapped
VIC	None	**2KB, direct mapped, 32-byte block**	8KB, direct mapped, 32-byte block

← FULLY ASSOCIATIVE ACTS BIGGER

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CPU Comparisons, cont.

	VAX 6000-500	NVAX Systems	VAX 9000-400
Pcache	2KB, direct mapped, 8-byte block, writethrough	**8KB, 2-way set associative, 32-byte block, writethrough**	128KB, 2-way set associative, 64-byte block, writeback
Bcache	512KB, direct mapped, 128-byte block, writeback	**128KB–2MB, direct mapped, 32-byte block, writeback**	None

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1/4

CPU Comparisons, cont.

	VAX 6000-500	NVAX Systems	VAX 9000-400
Technology	CMOS-3	**CMOS-4**	ECL
Chips	Several	**One**	Many

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NVAX Design Goals

- Time-to-market, without sacrificing quality
- Performance DON'T LIMIT CYCLE TIME
- Support for multiple system environments
- Take full advantage of the advanced CMOS-4 process

REDUCED DESIGN TIME BY 4 MONTHS OVER ORIGINAL SCHEDULE

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NVAX Design Goals

The Implications

- Time-to-market, complexity, and performance tradeoffs were made throughout the design cycle
- Aggressive schedules required concentrating on high-leverage design points, and on an unprecedented verification effort, resulting in a balanced, high-quality, functional, and reliable product
- Design was done working closely with systems and CAD groups, and with CMOS process engineers

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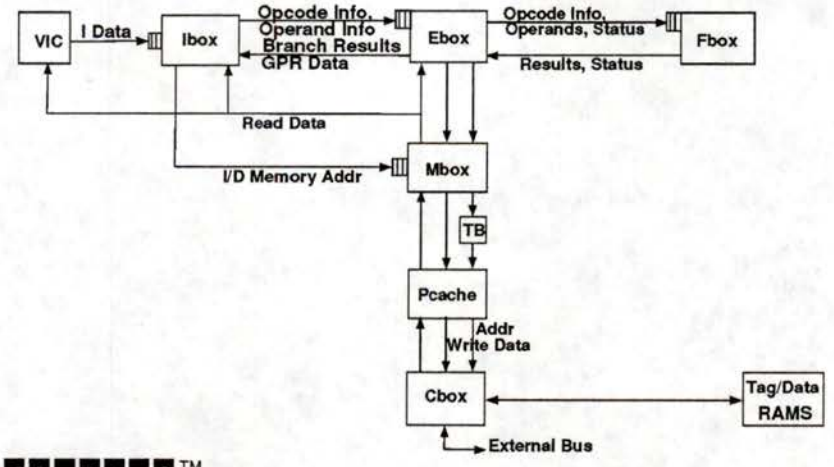
SEQN IN FUNCTIONAL RESULTS

NVAX Chip Overview

Chip Block Diagram



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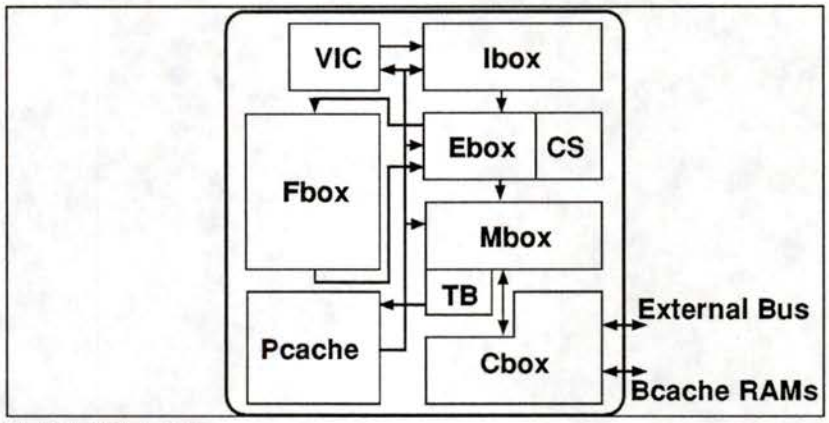
- SHOW CACHE HIERARCHY
- MENTION QUICKS

NVAX Chip Overview
Chip Organization



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NVAX Chip Overview
Functional Unit Summary

- **Ibox**: Instruction fetch, decode, and dispatch of instruction for further processing
- **Ebox**: Integer and logical instruction execution; interrupt and exception processing
- **Fbox**: Floating point and integer multiply instruction execution
- **Mbox**: Memory management and access to first-level Pcache
- **Cbox**: Interface to second-level Bcache and external bus

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Slide No. 16

NVAX Chip Overview
The Ibox

- Instruction fetch of up to 8 bytes per cycle
- Instruction decode and issue unit dispatches instructions for further processing
- Pipelined complex specifier unit calculates operand effective addresses and makes memory requests
- 2KB, direct mapped VIC, with 32-byte blocks and parity protection on tags and data
- Branch prediction for conditional branches

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ONE COMPONENT/CYCLE

LOAD/STORE UNIT FOR RISC MACHINES

VIRTUAL CACHE = FLUSH ON REI

NVAX Chip Overview
The Ebox

- Pipelined integer and logical instruction execution
- Fbox operand steering
- Instruction retire and result store orchestration
- Interrupt and exception processing
- Specialized hardware features to speed execution
- 1600-word control store with 20-location patch capability

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} EBOX/FBOX COORDINATION

CONTROL STORE USED FOR ALL INSTRUCTIONS; NOT A LIMIT TO CYCLE TIME

USED: 1500
STRING, QUEUE: 270
OS SUPPORT: 447
INTERRUPTS, EXCEPTIONS, RESET: 225

HALF IN COMPLEX INSNS, OS SUPPORT, BOOKKEEPING

NVAX Chip Overview
The Fbox

- 4-stage floating point and integer multiply pipeline with conditional data-dependent bypass of the final stage BASED ON MINI ROUND OF FINAL RESULT
- Non-pipelined floating point divider
- Ebox supplies operands, stores results, and coordinates fault and exception handling

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NVAX Chip Overview
The Mbox

STRONG R/W ORDERING
NO HITS UNDER MISS

- Reference sequencing of requests from multiple sources
- 96-entry, fully associative TB with parity protection
- Hardware TB miss sequencing and refill
- 8KB, 2-way set associative, writethrough Pcache, with 32-byte blocks and parity protection on tags and data

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NVAX Chip Overview
The Cbox

- Controller for a writeback cache with 32-byte blocks, using ECC-protected tag and data RAMs on the CPU module
- Support for 4 cache sizes (128KB, 256KB, 512KB, 2MB) and multiple tag and data RAM speeds allows system designer to choose cache configuration independently of CPU speed
- External bus interface provides support for cache coherence protocols for use in MP systems

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- SECDED ECC
- NO SUBBLOCKS FOR PERFORMANCE
- MP SUPPORT FOR ALL SYSTEMS
- OWNERSHIP PROTOCOLS
- EXTERNAL BUS IS NON-PIPED: I, D MISS, WB ALL OUTSTANDING
- FILLS SUPPLY REQUESTED QW FIRST

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1/2

NVAX Chip Overview
RISC vs. CISC

The terms RISC and CISC apply primarily to *macro*architecture, but certain *micro*architectural design and implementation techniques have become associated with RISC designs. These same techniques may be applied to CISC architectures, such as the VAX, in order to improve performance.

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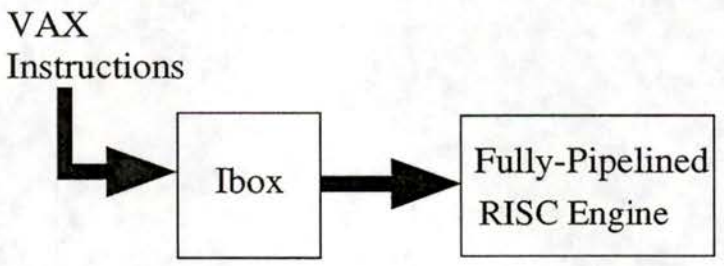
NVAX Chip Overview
A RISC-Like CISC Chip



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NVAX Chip Internals
Components of Performance

$$Performance = \frac{1}{CPI * CycleTime * InstructionCount}$$

Component	Influencing Factors
CPI	Microarchitecture
Cycle Time	Process Technology, Design Style, Microarchitecture
Instruction Count	Algorithms, Compilers, Macroarchitecture

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NVAX Chip Internals

Application of RISC Microarchitectural Techniques

- Macropipelined: Autonomous functional units
- Queued interfaces between boxes
- Data scoreboards
- Branch prediction

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NVAX Chip Internals

Autonomous Functional Units

Decrease in the average Cycles Per Instruction (CPI) is most strongly affected by doing more things in parallel. The usual way to do this is to divide instruction execution into smaller steps which can be performed in parallel by fully-pipelined autonomous functional units.

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NVAX Chip Internals
Autonomous Functional Units, cont.

- Instruction fetch, decode, operand evaluation —Load/Store design within instructions (Ibox)
- Integer, logical, and floating point instruction execution on canonical operands (Ebox, Fbox)
- Memory management and cache access (Mbox, Cbox)

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NVAX Chip Internals
Inter-Box Queues

With autonomous functional units, queues are required at the critical box boundaries to normalize the rates at which each unit operates.

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NVAX Chip Internals
Inter-Box Queues, cont.

- Instruction queue: Opcode information (Ibox to Ebox)
- Source queue, destination queue: Pointers to operands and results (Ibox to Ebox)
- MD registers: Memory operand data (Ibox and Mbox to Ebox)
- Branch queue: Branch information (Ibox to Ebox)

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NVAX Chip Internals
Inter-Box Queues, cont.

- Specifier queue: Ibox-generated memory specifier addresses (Ibox to Mbox)
- PA queue: Pre-translated physical addresses for outstanding memory stores (Mbox)
- Write queue: Pending packed Bcache writes (Cbox)

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NVAX Chip Internals
Data Scoreboards

With autonomous functional units, operations occur out of order with respect to the actual execution of instructions. Scoreboards are required to control access to the correct data.

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NVAX Chip Internals
Data Scoreboards, cont.

- Ebox/Fbox GPR write to Ibox GPR read:

```
MOVAL   M,R0
ADDL2   (R0),R1
```

- Ibox GPR write to Ebox/Fbox GPR read:

```
MOVL    R0,M
ADDL2   (R0)+,R1
```

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Slide No. 32

NVAX Chip Internals
Data Scoreboards, cont.

- Fbox GPR write to Ebox GPR read:

```
ADDF2    R0,R1
MOVL     R1,M
```

- Ebox/Fbox memory store to Ibox operand read:

```
MOVL     R0,(R1)
ADDL2    (R1),R2
```

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NVAX Chip Internals
Branch Prediction

With PC redirection done early in the pipeline and conditional branch results calculated late, there is a large performance degradation if the pipeline is allowed to drain waiting for a conditional branch result. Branch prediction attempts to predict the path that a conditional branch will take and redirect PC along that path before the condition is known.

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NVAX Chip Internals

Branch Prediction, cont.

- 512-entry RAM, indexed by low bits of branch PC
- Each entry contains 4 bits which record the actual direction of the most recent branches
- 16-bit lookup table provides the prediction for each bit pattern
- Prediction added to branch queue, with trap mechanism used to back out on incorrect prediction

BT PATTERN ENCODING

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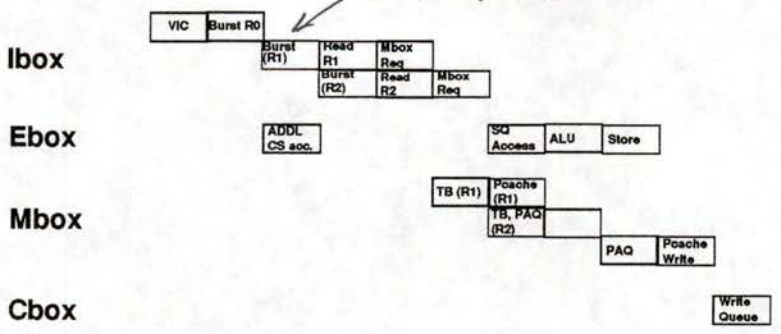
Slide No. 35

NVAX Chip Internals

Example 1: ADDL3 R0,(R1),(R2)

CSU EXTENSION



GAPS = STALLS

PARALLELISM LIMITED BY LOOKING AT ONLY 1 INSTRUCTION

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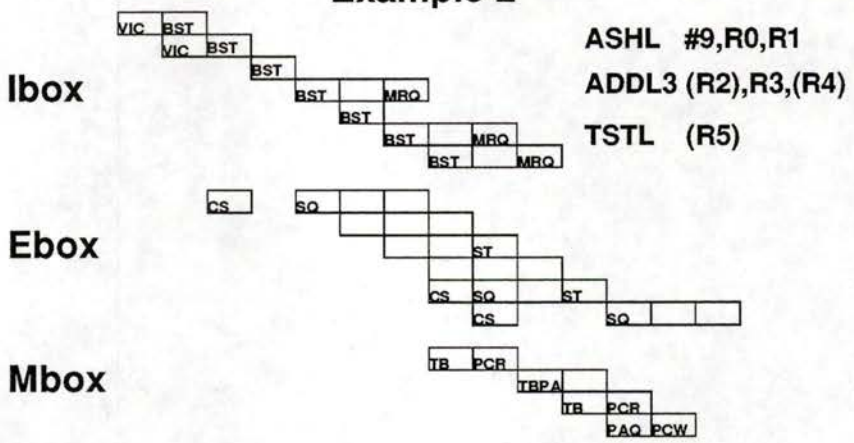
Slide No. 36

NVAX Chip Internals
Example 2



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MORE PARALLELISM

- CBOX SLOWS DOWN, IBOX PLOWS AHEAD

NVAX Chip Internals
Performance Monitoring Hardware

- Provides access to critical statistics: TB and cache hit rates, CPI, stalls, etc.
- Implemented as a combination of hardware and microcode. Dynamically loaded microcode patches enhance the basic capability
- Access and control provided by privileged performance monitoring program

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- APPLICATIONS BEING DEVELOPED
- PHOTO CODE USED BEFORE AND AFTER ANNOUNCEMENT TO TUNE SOFTWARE

Functional Results

- Virtually no bugs in pass 1 parts: Fab to operating system boot in two weeks, attributable to unprecedented design verification effort
- Patchable control store used as a debugging tool, and to fix the minor bugs that did exist in pass 1
- Pass 2 parts shipping to customers in production systems

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Performance Results

Benchmark	VAX 4000-500	VAX 6000-600
TPC-A	62.4	91.0
SPECmark	30.5	40.5
SPECint	24.3	30.9
SPECfp	35.5	48.6

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Slide No. 40

Conclusions

- RISC concepts applied to a CISC machine in order to increase performance significantly over previous VAX microprocessors
- Design takes full advantage of advanced CMOS-4 technology, resulting in 83.3 MHz operation
- Support for multiple system environments and configurations
- Which provides leadership performance in VAX products

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Author(s): G. Michael Uhler (Print Name) 74344 (Badge No.) 225-4735 (DTN)

(Print Name) (Badge No.) (DTN)

Today's Date: April 6, 1992

Title: NVAX: A High Performance Single Chip VAX Microprocessor

Type of Publication (article, paper presentation, degree presentation, photos, slides etc.): Slide Presentation

Name of Journal, Conference, Symposia, Magazine, Newspaper etc.: Spring 1992, DECUS U.S. Chapter Symposium

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Legal Representative	Bob Feltovic	

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Co-Author		
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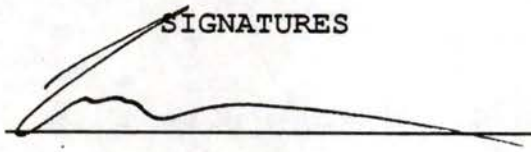
Author		4/7/92
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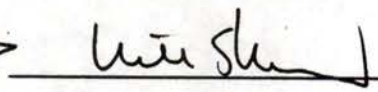
Consulting Engineer		4/7/92
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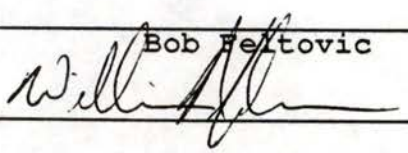
SCO STAFF MEMBER	Bob Feltovic 	4/8/92

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   YES--see slide 40: Performance Results. However, these numbers were obtained from performance reports released as part of the October NVAX announcement, or from the recently audited TPC-A results for the VAX 6000-600.

   Initials: WO

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ABSTRACT APPROVAL SIGNATURES

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Consulting Engineer		
Legal Representative	Bob Feltovic	

TECHNICAL PUBLICATION APPROVAL SIGNATURES

	SIGNATURES	DATE
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Legal Representative	Bob Feltovic	5/11/92
SCO STAFF MEMBER		4/8/92

BRANCH TAKEN = 2
BRANCH MISPREDICT = 6/4
VIC MISS = 3
PCACHE MISS = 4

TB MISS = 12,28

NVAX: High Performance Single Chip VAX Microprocessors

Michael Uhler
Semiconductor Engineering Group
Digital Equipment Corporation

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Slide No. 1

NVAX: High Performance Single Chip VAX Microprocessors

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Slide No. 2

Presentation Outline

- What is NVAX?
- CPU Comparisons
- NVAX Design Goals
- NVAX Chip Overview
- NVAX Chip Internals
- Functional Results
- Performance Results
- Conclusions

- OVERVIEW OF WHAT NVAX IS
- NVAX DESIGN GOALS AND THEIR IMPLICATIONS
- DETAILS OF THE DESIGN
- RESULTS

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What Is NVAX?

- Two Single-Chip VAX Microprocessors with a common core, providing two chip interfaces
- Designed to make use of high-performance RISC-like microarchitectural techniques as applied to the VAX CISC architecture
- Implemented in an advanced CMOS technology
- Used in multiple system environments

IMPLEMENTED USING TECHNIQUES TRADITIONALLY ASSOCIATED WITH RISC DESIGNS

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What Is NVAX?
Two Chip Interfaces

- Compatibility with existing VAX 4000 and VAX 6000 systems, with support for directory-based broadcast cache coherence protocol
- Compatibility with DECchip 21064 microprocessor and systems in which it is used, with support for conditional write update snoopy cache coherence protocol

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ALLOWS SYSTEM DESIGNER TO PICK THE APPROPRIATE INTERFACE FOR THE SYSTEM

What Is NVAX?
High-Performance Design

- VAX 9000 architectural heritage
- NVAX Ibox acts as a front-end to a RISC-like pipeline with multiple functional units
- On-chip Translation Buffer (TB), Virtual Instruction Cache (VIC), and Primary Cache (Pcache)
- On-chip controller for writeback Backup Cache (Bcache)

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VAX 9000: 1ST MACROPIPELINED VAX TAKE HIGH LEVERAGE IDEAS, EXPLOIT CMOS

USE RISC IMPLEMENTATION TECHNIQUES TO IMPROVE PERFORMANCE

CONTAINS THE USUAL COMPONENTS OF A STATE-OF-THE-ART MICROPROCESSOR

What Is NVAX?
Advanced CMOS Technology

- 0.75 µm, 3-metal layer, 3.3V CMOS-4 technology with support for 5V input signals
- CMOS-4 process is optimized for high-performance microprocessors, is fully qualified, robust and reliable, and in volume production
- Same process used for Alpha 21064 (EV-4) chip

LEFF = 0.5

NOT EXOTIC - OPTIMIZED

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Slide No. 7

What is NVAX?
Advanced CMOS Technology, cont.

- 62.5 MHz (16ns) to 90.9 MHz (11ns) operation—better than most industry RISC chips
- 1.3M transistors, 16.2mm x 14.6mm die size
- 339-pin and 431-pin thru-hole PGA packages

AS USED IN VAX 4000, 6000

AS USED IN 2106-COMPATIBLE SYSTEMS

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Slide No. 8

What Is NVAX?
Multiple System Environments

- **VAX 4000-100**: 71.4 MHz (14ns) operation, 128KB Bcache
- **VAX 4000-400**: 62.5 MHz (16ns) operation, 128KB Bcache, no VIC
- **VAX 4000-500**: 71.4 MHz (14ns) operation, 128KB Bcache
- **VAX 4000-600**: 83.3 MHz (12ns) operation, 512KB Bcache

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What Is NVAX?
Multiple System Environments, cont.

- **MicroVAX 3100-90**: 71.4 MHz (14ns) operation, 128KB Bcache
- **VAXstation 4000-90**: 71.4 MHz (14ns) operation, 256KB Bcache

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What Is NVAX?
Multiple System Environments, cont.

- **VAX 6000-600**: 83.3 MHz (12ns) operation, 2MB Bcache
- **VAX 7000-600**: 90.9 MHz (11ns) operation, 4MB Bcache
- **VAX 10000-600**: 90.9 MHz (11ns) operation, 4MB Bcache

32:1 RANGE OF BCACHE SIZES

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Slide No. 11

CPU Comparisons

	VAX 6000-500	NVAX Systems	VAX 9000-400
CPU Speed	62.5 MHz (16 ns)	**62.5 MHz (16ns)— 90.9 MHz (11ns)**	62.5 MHz (16 ns)
Pipeline	Micro	**Macro**	Macro
Branch Prediction	None	**512x4 bit, 1 outstanding**	1024x1 bit, 2 outstanding, target buffer

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CPU Comparisons, cont.

	VAX 6000-500	NVAX Systems	VAX 9000-400
TB	64 entries, fully associative	**96 entries, fully associative**	1024 entries, split, direct mapped
VIC	None	**2KB, direct mapped, 32-byte block**	8KB, direct mapped, 32-byte block

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Slide No. 13

FULLY ASSOCIATIVE ACT BIGGER

CPU Comparisons, cont.

	VAX 6000-500	NVAX Systems	VAX 9000-400
Pcache	2KB, direct mapped, 8-byte block, writethrough	**8KB, 2-way set associative, 32-byte block, writethrough**	128KB, 2-way set associative, 64-byte block, writeback
Bcache	512KB, direct mapped, 128-byte block, writeback	**128KB–2MB, 32-byte block or 128KB-8MB, 64-byte block, direct mapped, writeback**	None

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Slide No. 14

9000 DOESN'T HAVE A SECOND LEVEL OF CACHE HIERARCHY, BUT THE "PCACHE" IS QUITE LARGE.

CPU Comparisons, cont.

	VAX 6000-500	NVAX Systems	VAX 9000-400
Technology	CMOS-3	CMOS-4	ECL
Chips	Several	One	Many

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NVAX Design Goals

- Time-to-market, without sacrificing quality
- Performance
- Support for multiple system environments
- Take full advantage of the advanced CMOS-4 process

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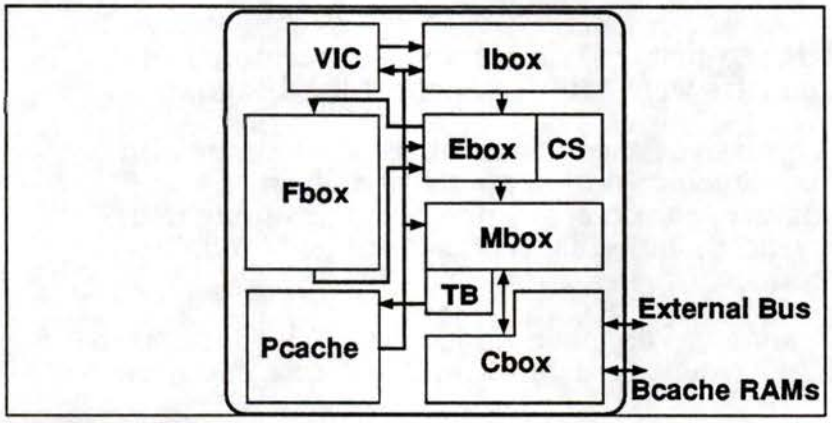
NVAX Chip Overview
Chip Organization



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NVAX Chip Overview
Functional Unit Summary

- **Ibox**: Instruction fetch, decode, and dispatch of instruction for further processing
- **Ebox**: Integer and logical instruction execution; interrupt and exception processing
- **Fbox**: Floating point and integer multiply instruction execution
- **Mbox**: Memory management and access to first-level Pcache
- **Cbox**: Interface to second-level Bcache and external bus

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Slide No. 20

NVAX Design Goals
The Implications

- Time-to-market, complexity, and performance tradeoffs were made throughout the design cycle
- Aggressive schedules required concentrating on high-leverage design points, and on an unprecedented verification effort, resulting in a balanced, high-quality, functional, and reliable product
- Design was done working closely with systems and CAD groups, and with CMOS process engineers

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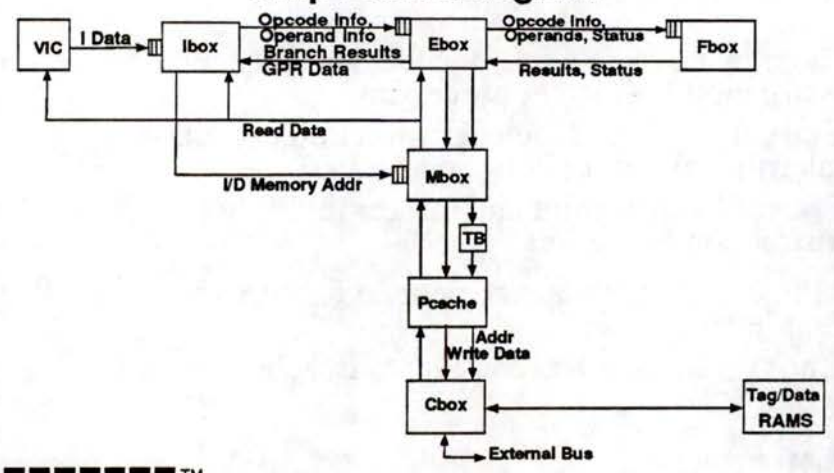
SEEN IN FUNCTIONAL RESULTS

NVAX Chip Overview
Chip Block Diagram



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SHOW CACHE HIERARCHY

SHOW PLUGS

NVAX Chip Overview
The Ibox

- Instruction fetch of up to 8 bytes per cycle
- Instruction decode and issue unit dispatches instructions for further processing
- Pipelined complex specifier unit calculates operand effective addresses and makes memory requests
- 2KB, direct mapped VIC, with 32-byte blocks and parity protection on tags and data
- Branch prediction for conditional branches

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ONE COMPONENT/CYCLE

LOAD/STORE UNIT FOR RISC MACHINES

VIC => FLUSH ON REI

Slide No. 21

NVAX Chip Overview
The Ebox

- Pipelined integer and logical instruction execution
- Fbox operand steering
- Instruction retire and result store orchestration
- Interrupt and exception processing
- Specialized hardware features to speed execution
- 1600-word control store with 20-location patch capability REPLACE OR ADD MICROINSTRUCTIONS

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} EBOX/FBOX COORDINATION

CONTROL STORE USED FOR ALL INSTRUCTIONS; NOT A LIMIT TO CYCLE TIME

USED: 1500
STRING, QUEUE = 270
OS SUPPORT = 447
INTERRUPTS, EXCEPTIONS, RESET = 225

=> HALF IN COMPLEX INSTRUCTIONS, OS SUPPORT, BOOKKEEPING,

Slide No. 22

FP/INT MULT INSTRUCTION EXECUTION

NVAX Chip Overview
The Fbox

- 4-stage floating point and integer multiply pipeline with conditional data-dependent bypass of the final stage BASSO ON MINI ROUND OF FINAL RESULT
- Non-pipelined floating point divider
- Ebox supplies operands, stores results, and coordinates fault and exception handling

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Slide No. 23

MEM MGT / PCACHE ACCESS

NVAX Chip Overview
The Mbox

- Reference sequencing of requests from multiple sources
- 96-entry, fully associative TB with parity protection
- Hardware TB miss sequencing and refill
- 8KB, 2-way set associative, writethrough Pcache, with 32-byte blocks and parity protection on tags and data

STRONG READ/WRITE ORDERING

NO HITS UNDER MISSES

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Slide No. 24

NVAX Chip Overview
The Cbox

- Controller for writeback cache with tag and data RAMs on the CPU module PROTECTED WITH ECC
- Support for multiple cache sizes and tag and data RAM speeds allows system designer to choose cache configuration independently of CPU speed
- External bus interface provides support for cache coherence protocols for use in MP systems

MP Support For All Systems

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NVAX: DIRECTORY-BASED BROADCAST PROTOCOL
NVAX+: CONDITIONAL WRITE UPDATE SNOOPY PROTOCOL

NVAX Chip Overview
RISC vs. CISC

The terms RISC and CISC apply primarily to *macro*architecture, but certain *micro*architectural design and implementation techniques have become associated with RISC designs. These same techniques may be applied to CISC architectures, such as the VAX, in order to improve performance.

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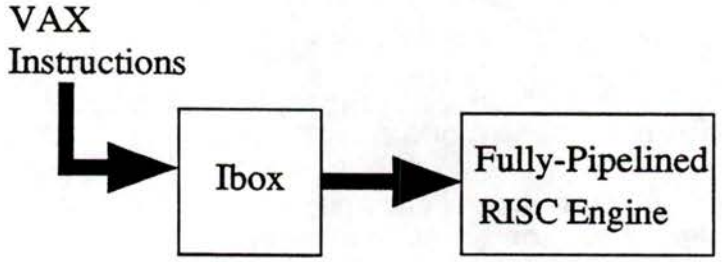
NVAX Chip Overview
A RISC-Like CISC Chip



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Slide No. 27

NVAX Chip Internals
Components of Performance

Component	Influencing Factors
CPI	Microarchitecture
Cycle Time	Process Technology, Design Style, Microarchitecture
Instruction Count	Algorithms, Compilers, Macroarchitecture

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Slide No. 28

NVAX Chip Internals

Application of RISC Microarchitectural Techniques

- Macropipelined: Autonomous functional units
- Queued interfaces between boxes
- Data scoreboards
- Branch prediction

AKA - SUPER PIPELINED

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NVAX Chip Internals

Autonomous Functional Units

Decrease in the average Cycles Per Instruction (CPI) is most strongly affected by doing more things in parallel. The usual way to do this is to divide instruction execution into smaller steps which can be performed in parallel by fully-pipelined autonomous functional units.

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NVAX Chip Internals
Autonomous Functional Units, cont.

- Instruction fetch, decode, operand evaluation —Load/Store design within instructions (Ibox)
- Integer, logical, and floating point instruction execution on canonical operands (Ebox, Fbox)
- Memory management and cache access (Mbox, Cbox)

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NVAX Chip Internals
Inter-Box Queues

INSTRUCTION QUEUE
OPERAND AND
RESULT QUEUES

With autonomous functional units, queues are required at the critical box boundaries to normalize the rates at which each unit operates.

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NVAX Chip Internals

Inter-Box Queues, cont.

- Instruction queue: Opcode information (Ibox to Ebox)
- Source queue, destination queue: Pointers to operands and results (Ibox to Ebox)
- MD registers: Memory operand data (Ibox and Mbox to Ebox)
- Branch queue: Branch information (Ibox to Ebox)

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NVAX Chip Internals

Inter-Box Queues, cont.

- Specifier queue: Ibox-generated memory specifier addresses (Ibox to Mbox)
- PA queue: Pre-translated physical addresses for outstanding memory stores (Mbox)
- Write queue: Pending packed Bcache writes (Cbox)

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NVAX Chip Internals

Data Scoreboards

With autonomous functional units, operations occur out of order with respect to the actual execution of instructions. Scoreboards are required to control access to the correct data.

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Slide No. 35

NVAX Chip Internals

Data Scoreboards, cont.

- Ebox/Fbox GPR write to Ibox GPR read:

```
MOVAL   M,R0
ADDL2   (R0),R1
```

- Ibox GPR write to Ebox/Fbox GPR read:

```
MOVL    R0,M
ADDL2   (R0)+,R1
```

EBOX WRITES ADDRESS INTO RQ.
IBOX READS ADDRESS

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Slide No. 36

NVAX Chip Internals

Data Scoreboards, cont.

- Fbox GPR write to Ebox GPR read:

```
ADDF2   R0,R1
MOVL    R1,M
```

- Ebox/Fbox memory store to Ibox operand read:

```
MOVL    R0,(R1)
ADDL2   (R1),R2
```

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EBOX STORES TO MEMORY; MUST READ UPDATED RESULT

NVAX Chip Internals

Branch Prediction

With PC redirection done early in the pipeline and conditional branch results calculated late, there is a large performance degradation if the pipeline is allowed to drain waiting for a conditional branch result. Branch prediction attempts to predict the path that a conditional branch will take and redirect PC along that path before the condition is known.

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NVAX Chip Internals
Branch Prediction, cont.

- 512-entry RAM, indexed by low bits of branch PC
- Each entry contains 4 bits which record the actual direction of the most recent branches
- 16-bit lookup table provides the prediction for each bit pattern
- Prediction added to branch queue, with trap mechanism used to back out on incorrect prediction

BIT PATTERN ENCODING

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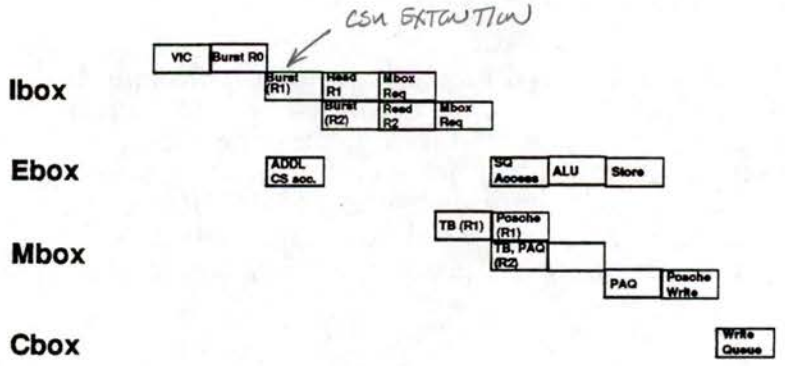
NVAX Chip Internals
Example 1: ADDL3 R0,(R1),(R2)



GAPS = STALLS

PARALLELISM SHOWN LIMITED BY LOOKING AT 1 INSTRUCTION

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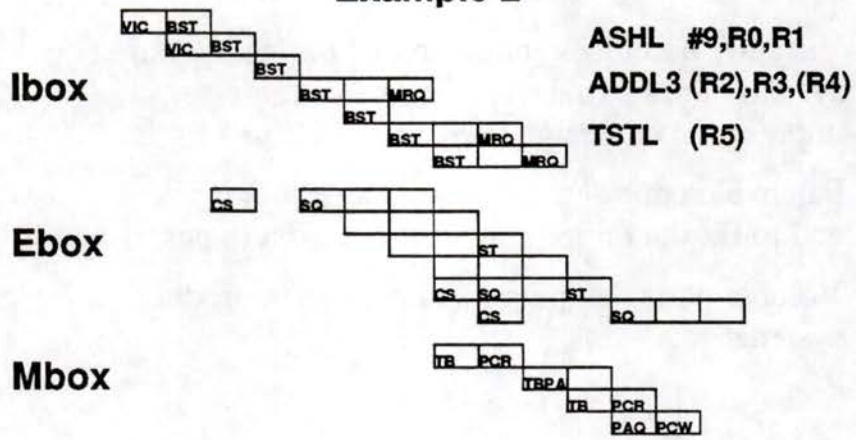
Slide No. 40

NVAX Chip Internals
Example 2



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Slide No. 41

MORE PARALLELISM

EBOX SLOWS DOWN, IBOX RUNS AHEAD

NVAX Chip Internals
Performance Monitoring Hardware

- Provides access to critical statistics: TB and cache hit rates, CPI, stalls, etc.
- Implemented as a combination of hardware and microcode. Dynamically loaded microcode patches enhance the basic capability
- Access and control provided by privileged performance monitoring program

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Slide No. 42

APPLICATIONS BEING DEVELOPED

PROTO CODE USED TO TUNE SOFTWARE

Functional Results

- Virtually no bugs in pass 1 parts: Fab to operating system boot in 16 days, attributable to unprecedented design verification effort
- Patchable control store used as a debugging tool, and to fix the minor bugs that did exist in pass 1
- Volume parts shipping to customers in production systems

FITS 4 MONTHS EARLIER THAN ORIGINAL SCHEDULE

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Performance Results

Benchmark	VAX 4000-600	VAX 6000-600	VAX 7000-600
TPC-A	103.8	102.3	123.8
SPECmark	41.0	42.1	46.6
SPECint	31.8	31.5	34.0
SPECfp	48.6	51.1	57.6

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Conclusions

- RISC concepts applied to a CISC machine in order to increase performance significantly over previous VAX microprocessors
- Design takes full advantage of advanced CMOS-4 technology, resulting in up to 90.9 MHz operation
- Support for multiple system environments and configurations
- Which provides leadership performance in VAX products

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REQUEST FOR TECHNICAL PUBLICATION APPROVAL

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Today's Date: May 29, 1992

Title: The NVAX and NVAX+ High-Performance VAX Microprocessors

Type of Publication (article, paper presentation, degree presentation, photos, slides etc.): article

Name of Journal, Conference, Symposia, Magazine, Newspaper etc.: ____
Digital Technical Journal

Date of Abstract Submission Requirement: N/A

Date of Publication Submission Requirement: June 8, 1992

Date of Publication or Presentation: DTJ issue, September-November, 1992

Abstract of Paper's Content:

NVAX and NVAX+ are high-performance VAX microprocessors that use techniques that have traditionally been associated with RISC designs to dramatically improve the performance of these chips over previous VAX microprocessors. The two chips provide an upgrade path for existing systems, and a migration path to the new Alpha systems. The design evolved throughout the course of the project as time-to-market, performance, and complexity tradeoffs were made. Special features were also added to the design to address issues of debug, maintenance, and analysis.

NOTE TO REVIEWERS

This paper discusses NVAX+, VAXstation 4000, model 90, MicroVAX 3100, model 90, VAX 4000, models 100, 675, and 690, VAX 7000, model 600, and VAX 10000, model 600, all of which are currently unannounced products. However, the publication date of this article is in the DTJ issue targeted for September-November, 1992, which is well after the July announcement date for these products. In addition, all of these products were discussed at DECWorld and DECUS, and the most recent issue of Digital Review mentions the products by name based on information obtained at DECWorld. This paper contains no information about these systems that is not already in the public domain. Therefore, the fact that these systems have not yet been officially announced should not preclude review of this article. In the unlikely event that these systems are not announced on time, we will make a decision about whether to remove all references, or stop publication of the article.

There is one semi-sensitive piece of information which has intentionally been left as TBD in the paper: the cycle time at which NVAX+ will be shipped in VAX 7000 and VAX 10000 systems. Rather than set expectations with this paper, we simply chose to defer any statement pending a final decision (presumably in June) on the cycle time.

It is important that all individuals in the approval loop realize and appreciate that each of the approval signatures will reflect the reviewing person has examined the proposed publication or public disclosure to determine, to the best of their knowledge, whether the material meets any of the criteria listed in questions 1-5 below. Therefore, each person in the signature loop is required to place his/her initials after review of each of the questions and place full signature and date on the last page.

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   Yes. The combination of the NVAX/NVAX+ performance monitoring hardware and microcode patch capability is the subject of a pending patent request. Based on the current schedule, the patent will be filed before the DTJ issue goes to press.

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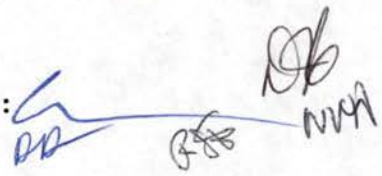
Initials: 

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Consulting Engineer _____ _____

Legal Representative _____ _____

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TECHNICAL PUBLICATION APPROVAL SIGNATURES

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