Box 27
folder 21

2 of 3 102749950

FRIGATE

PHASE 0 REVIEW

Frigate Phase 0 Agenda

Time	Activity	Presentor
8:30- 9:00 AM	Coffee	
9:00- 9:15 AM	Introduction	Reid Brown
9:15- 9:45 AM	Business Plan	Reid Brown
9:45-10:30 AM	Project Plan	Dave Cutler
10:30-10:45 AM	Break	
10:45-11:00 AM	Field Service Impact Statement	Mike Li
11:00-11:15 AM	Manufacturing Impact Statement	TBD
11:15-11:30 AM	Documentation Plan	Ken Western
12:00- 1:00 PM	Lunch	
1:30- 3:30 PM	Technical Review and Design Alternatives	Dave Cutler
3:30- 3:45 PM	Break	
3:45- 4:30 PM	Question Answer	All

BUSINESS PLAN REVIEW

Market and Product Requirements

- Frigate IS a Mid-Range VAX
- Frigate offers greater VAX performance at a lower cost/MIP

PRODUCT REQUIREMENTS

- Frigate MUST be 100% of a VAX
  - Floating Point performance is critical
  - Decimal performance is less important
  - Compatibility mode is not performance sensitive, may be done in software

MARKET REQUIREMENTS

(For Mid-Range VAX systems in 2-4 years)

- Greater performance range via multiprocessing

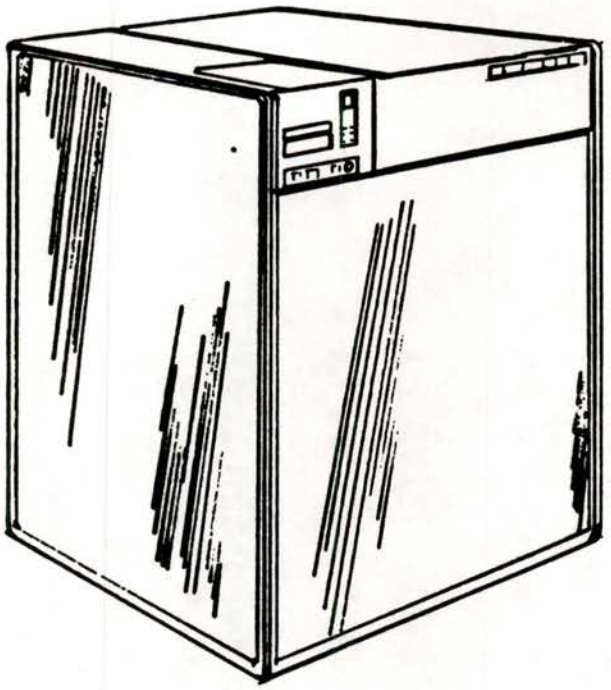
  FRIGATE: Large system is MP Kernel, from one to four processors

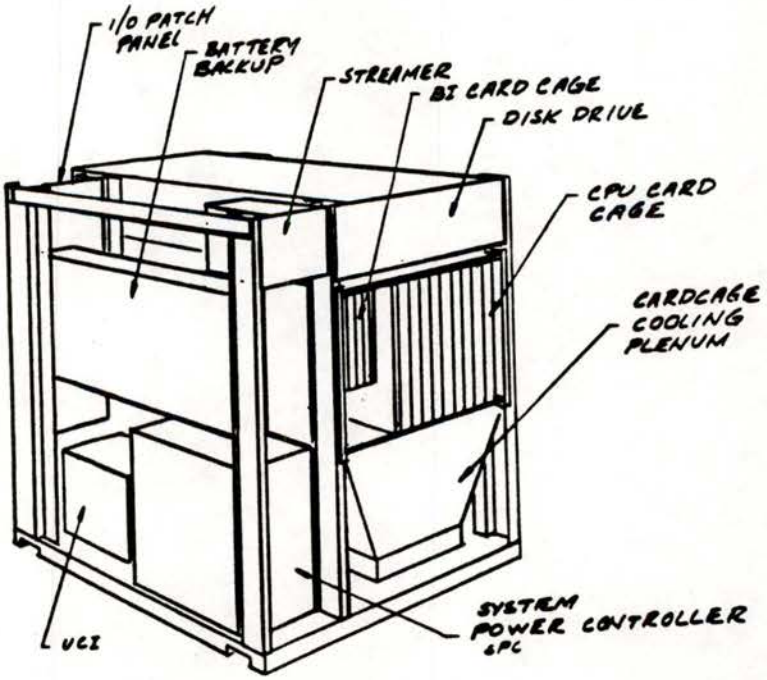
- Mid-Range must deliver lowest Cost/MIP

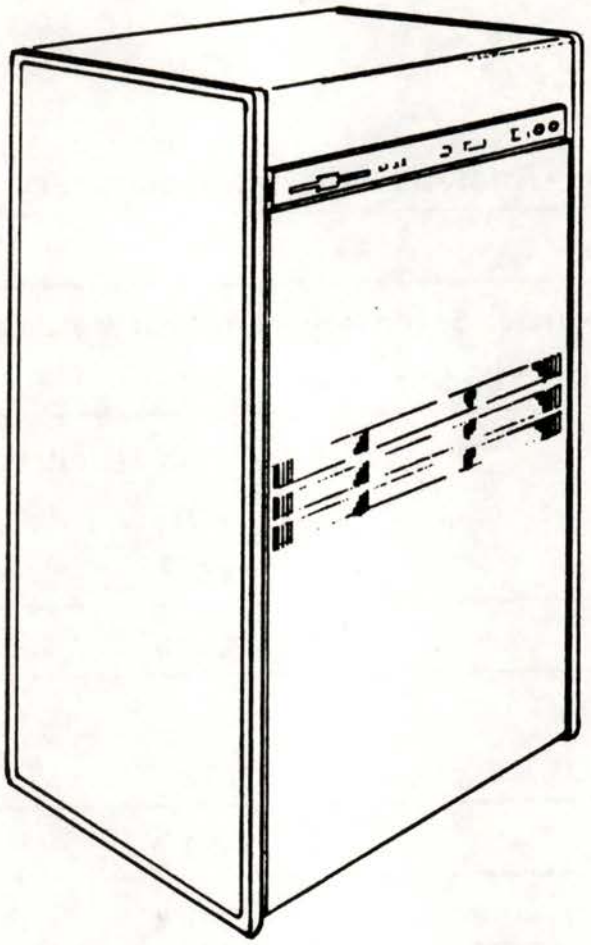
  FRIGATE: Cost/MIP = 16.6K/MIP

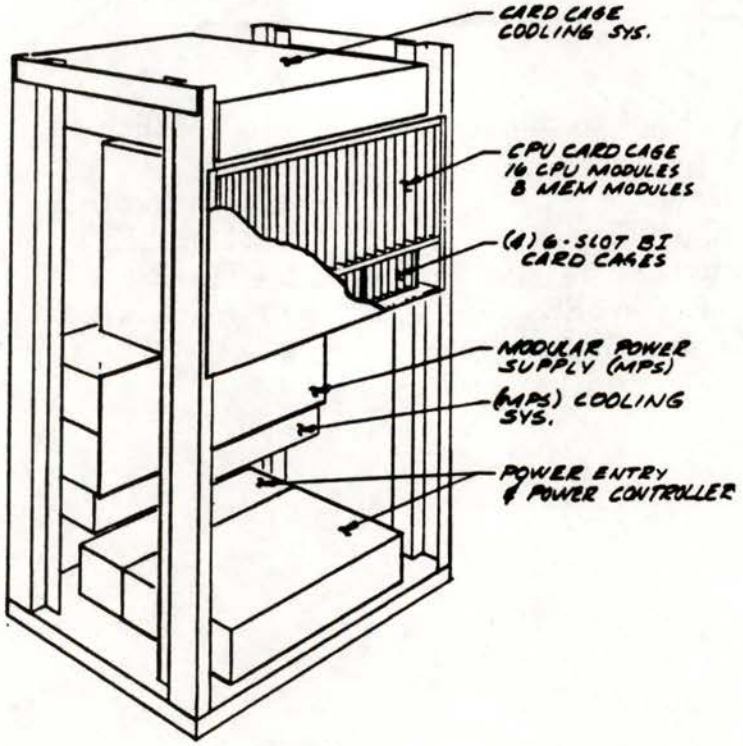
- 750/780/Skipjack Packaged System replacement

  FRIGATE: Entry System is bounded, has integral mass storage sub-system




I/O PATCH PANEL
BATTERY BACKUP
STREAMER
BI CARD CAGE
DISK DRIVE
CPU CARD CAGE
CARDCAGE COOLING PLENUM
UCI
SYSTEM POWER CONTROLLER
SPC




CARD CAGE COOLING SYS.
CPU CARD CAGE 16 CPU MODULES 8 MEM MODULES
(4) 6-SLOT BI CARD CAGES
MODULAR POWER SUPPLY (MPS)
(MPS) COOLING SYS.
POWER ENTRY & POWER CONTROLLER

5.2 Financial Base Case Analysis - Numerical Summary

Executive Summary – Lifetime Base Case

Lifetime Base Plan (FY85-94)	$M	% NOR
Number of Units	10,000 (Units)	
Total Lifetime Revenue	1,938	100
Less Cost of NOR	665	34
Gross Margin	1,273	66
Development Expense	72	4
Selling, Marketing, G&A Expense	532	27
Pre-Tax Profit	669	35
Taxes	281	14
Profit After Tax	388	20

After Tax NPV @ 30% Hurdle Rate	$16.7 Million
Internal Rate of Return	35.8%
Cash Payback Date	12 Quarters from FRS (Q2 FY91)
Max. Negative Cash Flow	$–241 Million
Markup (Lifetime)	5.4 Times
Development Period to FRS	13 Quarters (Q2 FY88)
5-Year Cost-of-Ownership	$–
BMC % MLP	0.3%

3.1 System/ Product Worldwide Forecast

Frigate	FY88	FY89	FY90	FY91
Unit Shipments:				
External	1,400	2,600	3,000	3,000
Internal	140	260	300	300
TOTAL	1,440	2,860	3,300	3,300
System Net Revenue ($M):				
Systems	165.2	310.4	355.3	352.5
Add-Ons	62.4	115.2	134	130.5
Layered Software	31.2	58.6	67	66.9
Total System NES	258.8	484.2	556.3	549.9
as % Corp NES				
System Service Revenue	3.5	16.5	26.1	42.5
System NOR	262.3	500.7	582.4	592.4
as % Corp NOR				
% Unit Dist by Op System				
% VMS	90	80	70	70
% ULTRIX	10	20	30	30
	100	100	100	100

3.2 Detailed Worldwide Unit Ship Forecast by Market Group

Marketing Group	Worldwide Unit Forecast by FY			
	FY88	FY89	FY90	FY91
Internal to DEC (IEG)	140	260	300	300
Technical:				
OEM	434	806	930	930
End User	658	1,222	1,410	1,410
Commercial:				
End User (Office, etc.)	308	572	660	660
TOTAL EXTERNAL	1,400	2,600	3,000	3,000
Geographic Mix % Shipments To:				
United States	80	64	64	64
Europe	18	27	27	27
GIA	2	9	9	9
	100	100	100	100

Source: Mid-Range System Long Range Plan; 12+ Process.

3.3 Impacted Products: Phaseover Forecast Summary

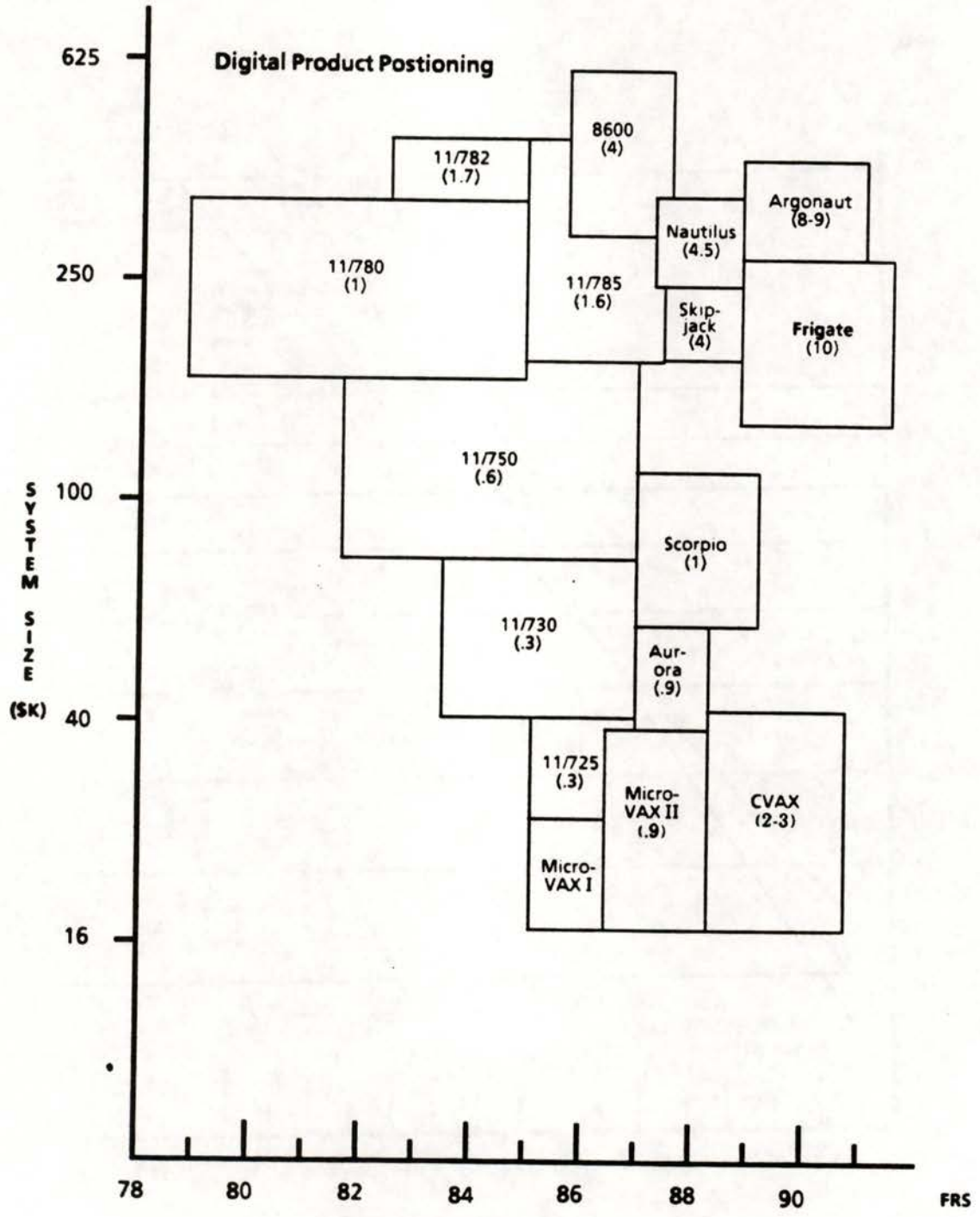
	Pre-FRS		Post-FRS			
Nautilus	**FY86**	**FY87**	**FY88**	**FY89**	**FY90**	**FY91**
Unit Shipments:		3,150	5,500	750	50	
NES		1,014	1,638	223	15	
Service Revenues		13	21	3	.2	
NOR		1,027	1,659	226	15.2	

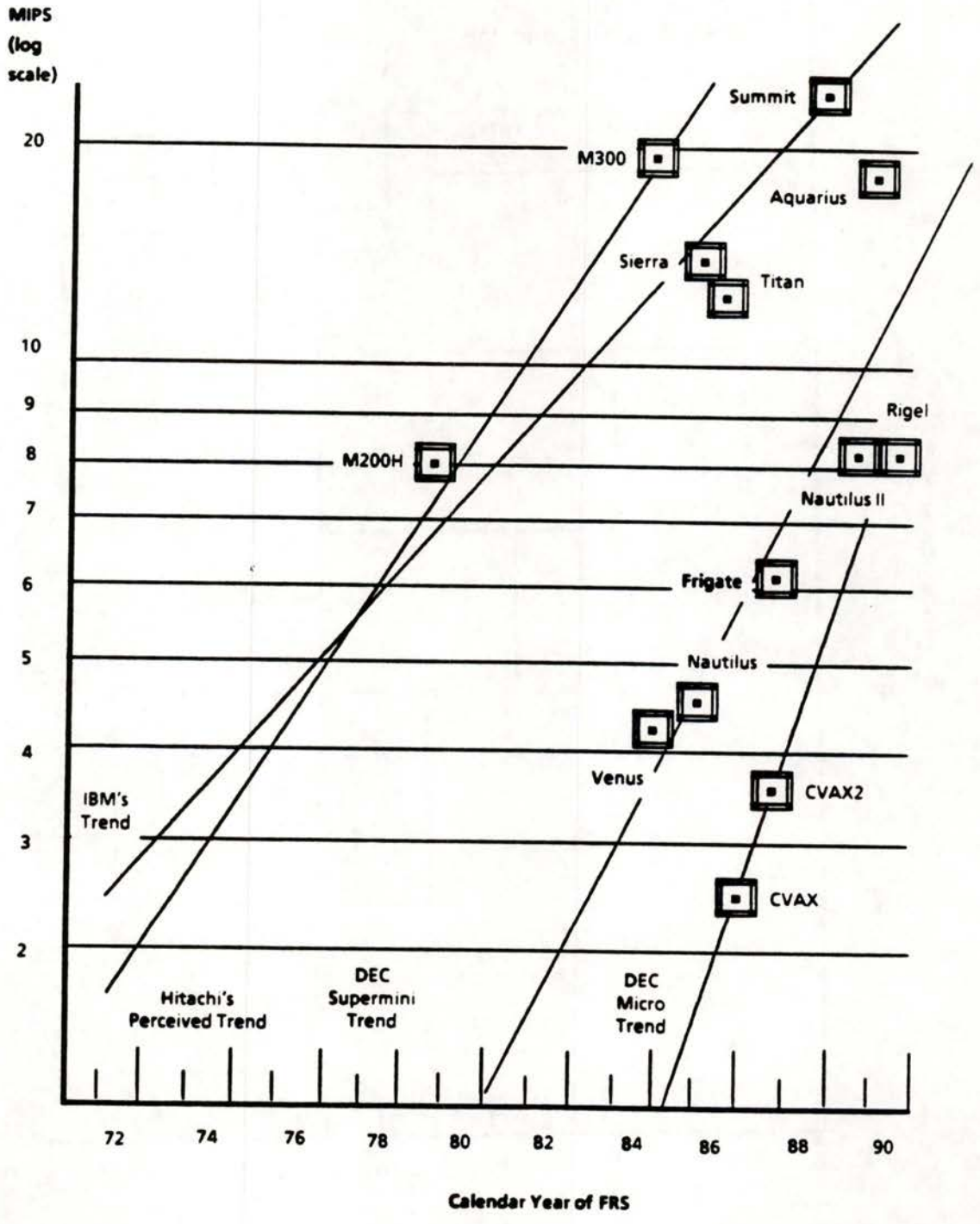
	Pre-FRS		Post-FRS			
8600	**FY86**	**FY87**	**FY88**	**FY89**	**FY90**	**FY91**
Unit Shipments:	2,400	960	730			
NES	1,872	312	234			
Service Revenues	12	4	3			
NOR	1,884	316	237			

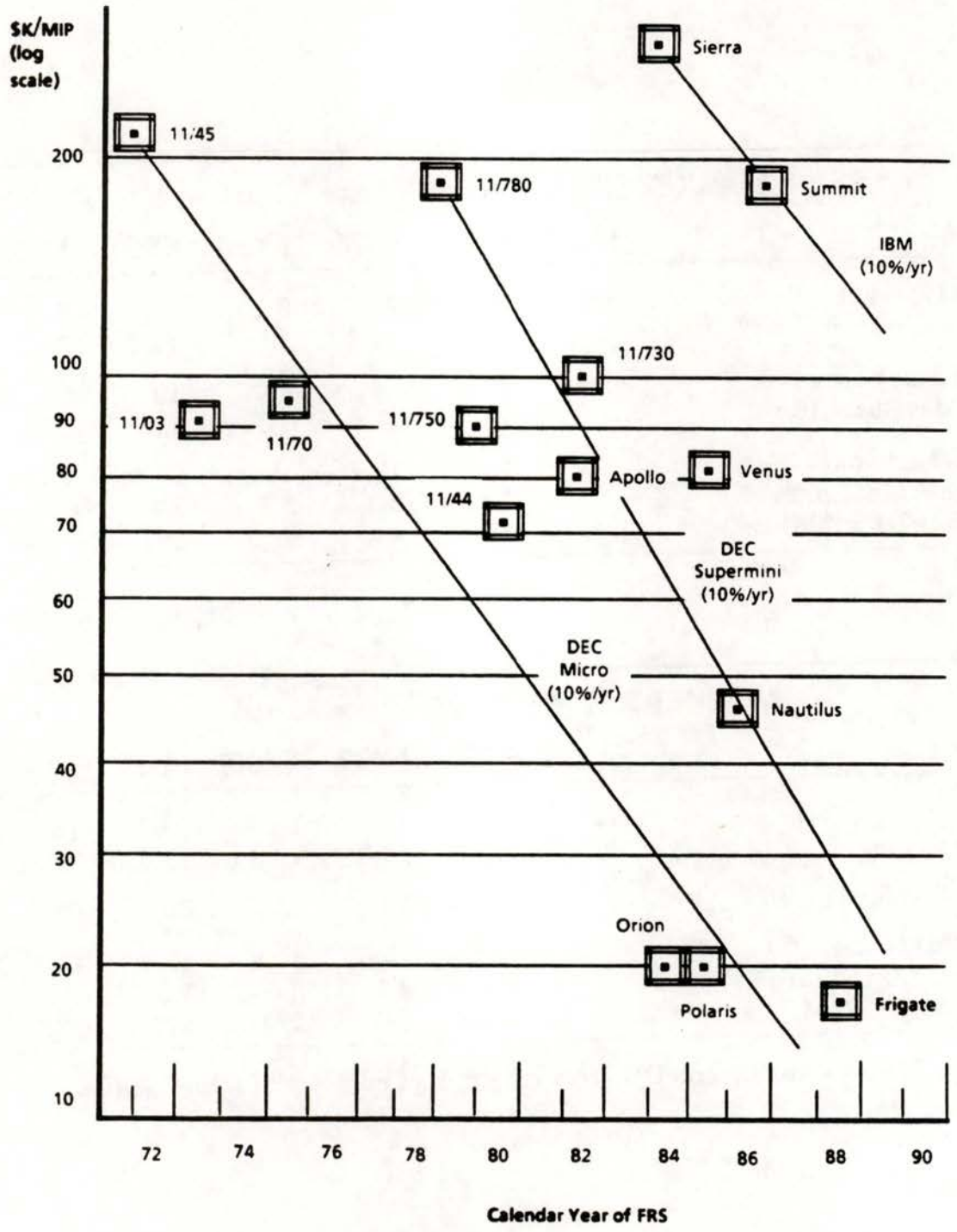
Source: 12+ Volumes, Corporate Revenue Plan

1.5.2 Applications (Market Segmentation)

Application Area	Lifetime NOR	%	Channels
Technical Application Segment	$1.36B	70	Sales force – SMUs, AMCs
Traditional Digital business, serving customers with technical applications requiring significant computing resources.			
Business Professional Segment	$.58B	30	Sales force – SMUs, AMCs
Commercial/Business applications, including office automation and more traditional data processing.			


Digital Product Postioning
625
250
100
40
16
SYSTEM SIZE ($K)
8600 (4)
11/782 (1.7)
Argonaut (8-9)
Nautilus (4.5)
11/780 (1)
11/785 (1.6)
Skip-jack (4)
Frigate (10)
11/750 (.6)
Scorpio (1)
11/730 (.3)
Aur-ora (.9)
11/725 (.3)
Micro-VAX II (.9)
CVAX (2-3)
Micro-VAX I
78
80
82
84
86
88
90
FRS


MIPS
(log
scale)
20
10
9
8
7
6
5
4
3
2
Summit
M300
Aquarius
Sierra
Titan
Rigel
M200H
Nautilus II
Frigate
Nautilus
Venus
CVAX2
CVAX
IBM's
Trend
Hitachi's
Perceived Trend
DEC
Supermini
Trend
DEC
Micro
Trend
72
74
76
78
80
82
84
86
88
90
Calendar Year of FRS


$K/MIP
(log
scale)
200
100
90
80
70
60
50
40
30
20
10
Sierra
11/45
11/780
Summit
IBM
(10%/yr)
11/730
11/03
11/70
11/750
Apollo
Venus
11/44
DEC
Supermini
(10%/yr)
DEC
Micro
(10%/yr)
Nautilus
Orion
Polaris
Frigate
72
74
76
78
80
82
84
86
88
90
Calendar Year of FRS

MARKET SIZE ($100-250K Price Band)

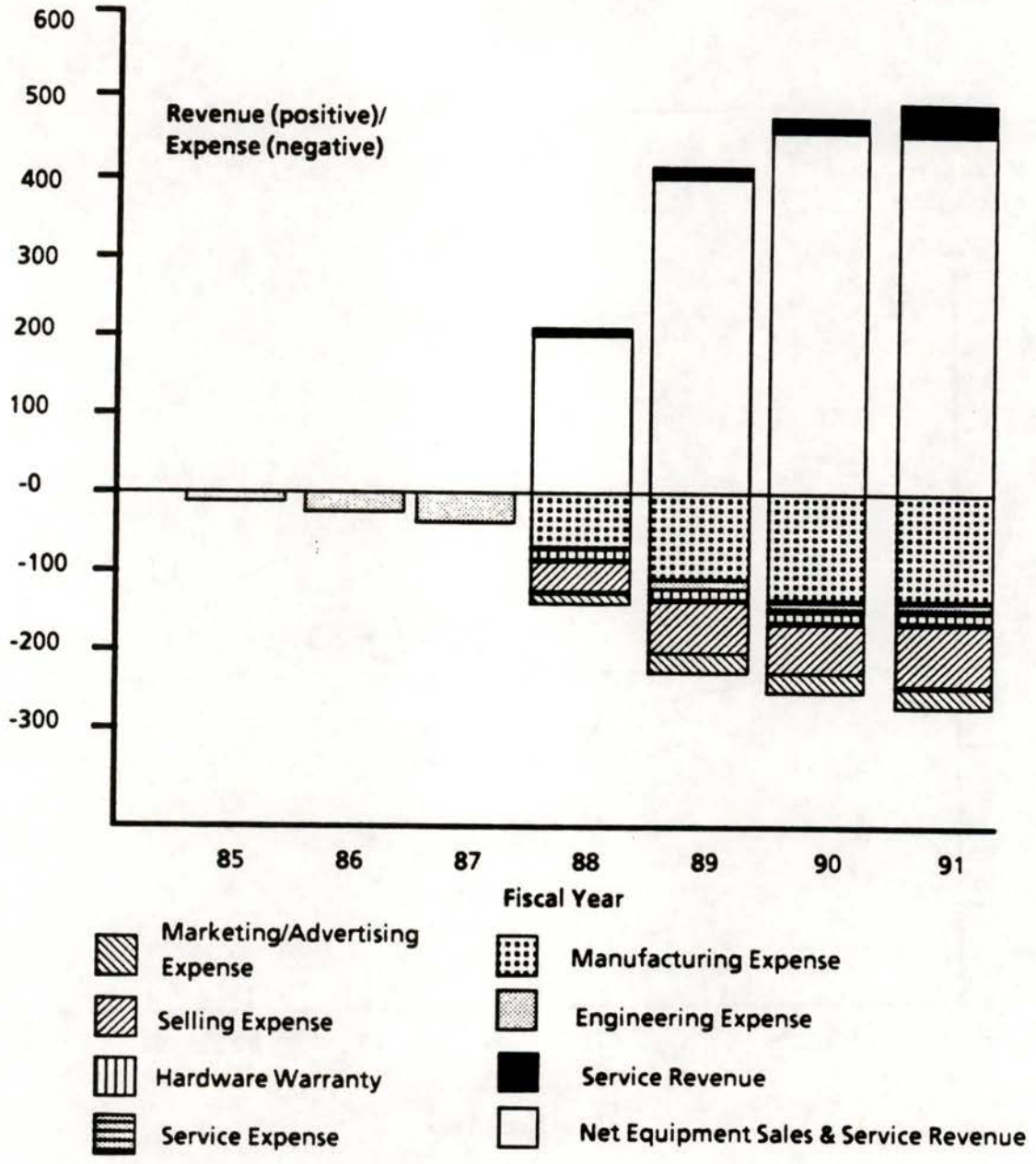
	FY87	FY88	FY89	FY90	FY91	FY92
Total Market ($B)	5.8	6.5	7.3	8.1	9.0	9.8
Growth (%)		12	12.3	11	11.1	8.8
IBM Mkt Share (%)		17	18	19	19	20
HP Mkt Share (%)		11	11	11	11	11
DEC Mkt Share (%)		15.9	19.7	19.9	20.4	18.5
Frigate Mkt Share (%)		2.1	3.3	3.5	3.1	
Frigate NES ($M)		135	243	282	281	

MARKET SIZE ($250-625K Price Band)

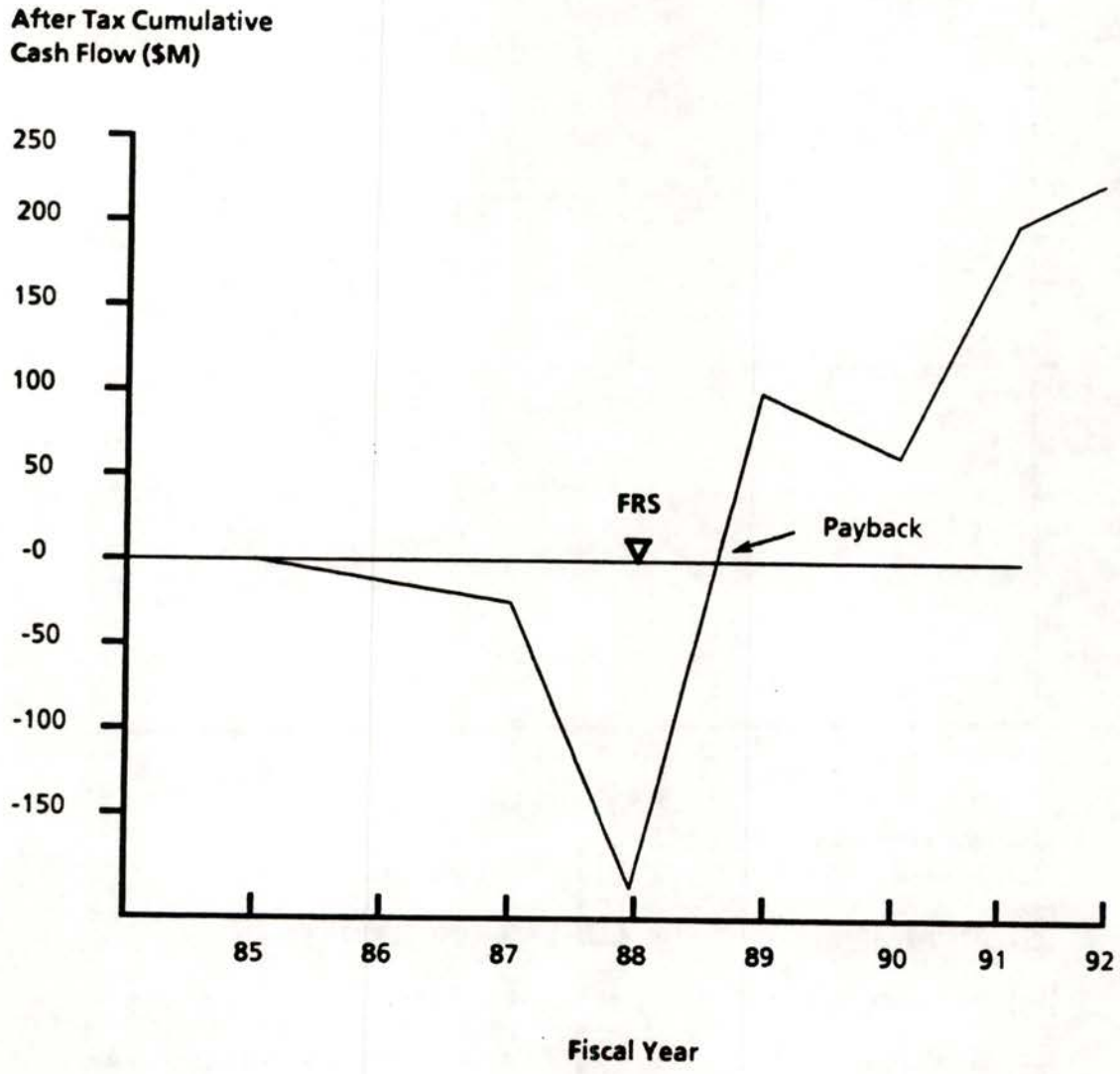
	FY87	FY88	FY89	FY90	FY91	FY92
Total Market ($B)	9.1	10.5	12	13.6	15.2	16.7
Growth (%)		15.4	14.3	13.3	11.7	9.9
IBM Mkt Share (%)	52	58	58	58	60	60
DEC Mkt Share (%)		13.5	15.6	13.8	11.7	8.8
Frigate Mkt Share (%)		1.2	2.1	2.0	1.8	
Frigate NES ($M)		124	247	277	276	

Source: "Market Sizing and DEC System Product Forecast", (John Coombs, 5-MAR-85).

5.5 Pre-Tax Revenue and Cash Outlay Bar Charts



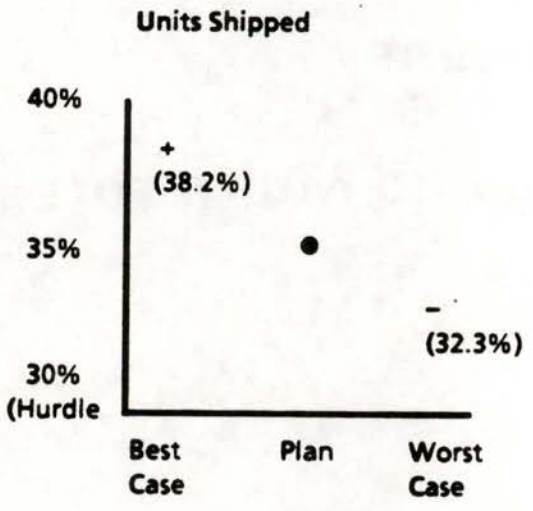
5.4 Cumulative Cash Flow Graph

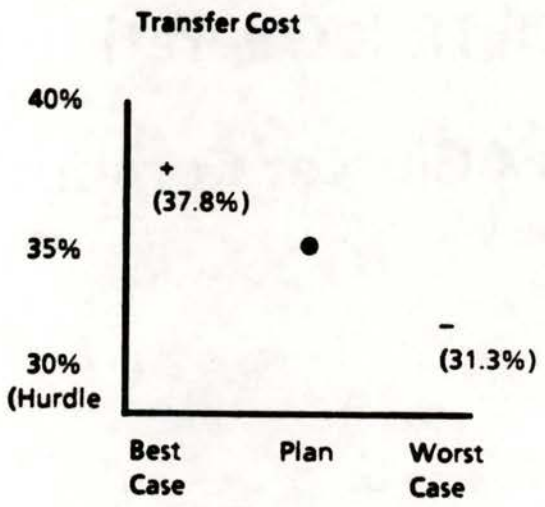


Sensitivity Analysis

Assumptions	Best Case	Plan	Worst Case
Number of Units Sold	12,500	10,000	7,500
Transfer Cost:			
Entry System	$31K	$33K	$39K
High End System	$61K	$63K	$69K

The effect of these variances on the internal rate of return (IRR) is:





Project Plan —

Frigate Overview

- High Performance
- Mid Range
- BI Based
- Full VAX Processor
  - VMS Operating system
  - ULTRIX Operating System
- VAX Cluster Computing and Multiprocessing

Key Product Attributes

- Single Processor Performance is 6 times VAX-11/780
- Up to 4 Processors in a Single Backplane, yielding 20 times VAX-11/780
- $20k Kernel Transfer Cost
- FRS September FY88

Product Deliverables

- Full VAX Processor on three F-Series (Nautilus) Modules
- Memory Controller Module on a single F-Series Module
- Multiprocessor Clock and Console Module on a single F-Series module
- Dual-BI Adapter Module on a single F-Series Module
- 8 Mbyte Memory array utilizing 256 Kbit Dynamic RAMs
- 32 Mbytes Memory array utilizing 1 Mbit Dynamic RAMs

Basic Systems

- A bounded entry-level system
- A high-end system configured using building block approach

Entry Level Single Processor System Package

(Based on VAX-11/750)

- A Six-Slot CPU Backplane
- A Four-Slot Memory Backplane
- A Six-Slot BI Backplane
- A power subsytem
- A system cabinet

Multiprocessor System Package

(Based on Skipjack)

- A 16 Slot CPU Backplane
- An Eight-Slot Memory Backplane
- Four Six-Slot BI Backplanes
- A Power Subsystem
- A System Cabinet

Detailed Cost Breakdown

Subsystem Product Costs

ITEM	Cost ($K)
CPU	8.0
Memory controller	1.0
Console controller	1.5
Dual-BI adapter	2.0
8 Mbyte memory array module	2.0
Single-processor backplanes	1.5
Single-processor power and packaging	4.0
Multiprocessor backplanes	2.0
Multiprocessor power and packaging	5.0

Kernel Transfer Costs

Kernel Transfer Costs

ITEM	Cost ($K)
CPU	8.0
Memory controller	1.0
Console controller	1.5
Dual-BI adapter and BI backplane	2.0
8 Mbyte memory array module	2.0
Single-processor backplane	1.5
Single-processor power and packaging	4.0
TOTAL	20.0

Single-Processor System Transfer Costs

Single-Processor System Transfer Costs	
ITEM	**Cost ($K)**
Kernel system	20.0
16 Mbytes memory (24 Mbytes total)	4.0
Battery backup	.75
BI-COMBO	.75
BSA	2.5
AIE	.75
RAXX	3.0
MAYA II	.75
Terminals (2)	.5
TOTAL	33.0

Multiprocessor System Transfer Costs (Two CPUs)

Dual-Processor Transfer Costs	
ITEM	Cost ($K)
1st CPU	8.0
2nd CPU	8.0
Memory controller	1.0
Console controller	1.5
Dual-BI adapter and BI backplane	2.0
Multiprocessor backplanes	2.0
Multiprocessor power and packaging	5.0
40 Mbytes memory	10.0
Battery backup	.75
BI backplane (2 total)	.5
BI-COMBO (4)	3.0
BSA	2.5
AIE	.75
RAXX (3)	9.0
TA82	8.3
MAYA II	.75
TOTAL	63.0

A.2 Development Budget

PROJECT COSTS ($M)	FY85	FY86	FY87	FY88
People	**2.47**	**3.63**	**4.91**	**5.64**
Number of people	18	23	27	27
Manpower cost per person	.137	.158	.182	.209
Material Expense	**.075**	**.33**	**.79**	
Design support	.075	.1	.1	
Gate array test parts		.06	.06	
Gate array qualification parts			.5	
Power/packaging material			.05	
Custom chip parts		.17	.08	
External Expense	**.1**	**4.41**	**5.50**	**.63**
Diagnostics	.1	.47	.55	.63
LSI logic		1.0	.5	
CXO – module layout		.5	.22	
CXO – BP, Emech, system		.2	.1	
Qualification – components		.1	.3	
Qualification – system			1.0	
Module tooling		.1	.3	
Manufacturing support		.16	1.09	
Memory engineering		1.0	.5	
Power/packaging subcontracting		.52	.56	
Custom chip design/fabrication		.36	.38	
Miscellaneous	**.2**	**.5**	**.5**	
TOTAL EXPENSES	**2.845**	**8.87**	**11.7**	**6.27**

PROJECT COSTS ($M)	FY85	FY86	FY87	FY88
Capital Equipment	**.625**	**.525**	**5.1**	
Big items	.5			
Laboratory	.02	.08	.04	
Prototypes		.4	5.0	
Miscellaneous	.105	.045	.06	
TOTAL FRIGATE ($M)	**3.47**	**9.395**	**16.8**	**6.27**

Field Service

FRIGATE Business Metrics

	BMC	COO	YMC/MLP	MIPS
Single Processor FRIGATE System	$350	$121K	4.2%	6
Dual Processor FRIGATE System	$600	$206K	4.2%	10
IBM 4341-12	$1055	$412K	3.5%	1.5
IBM 4361-5	$746	$280K	3.7%	1.3
IBM 4381-2	$722	$575K	1.6%	2.7
DG MV/10000	$1060	$245K	6.9%	2.2
PRIME 9950	$1703	$471K	5.5%	2.5
PERKIN-ELMER 3250XP	$1302	$272K	7.9%	3.0
GOULD/SEL 32/8750	$2574	$464K	9.7%	2.8

Reliability Goals

MSI $M	MSE $M	LABOR $M	MATERIAL $M	BIE $M	TRAINING $M	MISC $M	GR. MARGIN %
82.1	61.84	26.2	21.7	10.1	2.0	1.9	24.6
@mtbf = 8200hrs/cpu, mttr = 2 hrs							
82.1	54.4	18.76	21.7	10.1	2.0	1.9	33.8
@mtbf = 8200hrs/cpu, mttr = 1 hr							
82.1	80.02	35.67	30.35	10.1	2.0	1.9	2.5
@mtbf = 4100hrs/cpu, mttr = 2 hrs							
82.1	69.93	25.58	30.35	10.1	2.0	1.9	14.2
@mtbf = 4100hrs/cpu, mttr = 1 hr							

MSI = Maintenance Service Income

MSE = Maintenance Service Expense

BIE = Branch Inventory Expense

Volume = 10k units

BMC single $350 = 70%

BMC dual $600 = 30%

Generic Maintainability

- Thermal sensors in system
- Ball bearing fans
- No cable connections on the modules
- Machine readable revisions for microcode and hardware
- LED indicators for power-up test failure indications

Frigate Maintainability Features

- FSB single error correction and logging buffers
- Array's row and column address is part of ECC data
- Scan path'ed cpu, memory and FSB controller
- Dedicated scan path bus
- The LRU architecture in Frigate's cache system allows greatly reduced cache array data testing-time
- EXEC module is microcode controlled; high visibility into the most complex part of the cpu
- Memory testing is implemented in memory controller hardware; reduces testing time
- Self-configuring memory for different array type and starting address
- Cache data has parity error detection
- Console communication with other subsystems is not dependent on the FSB being operational

System Maintainability Goals

- Independent console subsystem
- Operator's console log
- Machine readable boot code versions
- Bootpath verification on boot as well as boot failure indicators
- Scan path shadowing
- CDROM being both the console load media and distribution media
- In multi-cpu environment, the console subsystem will be able to diagnose a failing cpu, while the remaining system continues to operate

Risk and Dependencies

Technology:

- Scan path shadow register
- Console strategy depends upon NV-RAM
- CDROM as console load media depends upon the NV-RAM

System Architecture:

- Online failing cpu diagnosis has complex relations between hardware, operating software and console subsystem; there is a risk that there may be insufficient resources to clearly achieve this goal

Software:

- Symmetric multiprocessing support is solely dependent upon the VMS operating system's effectiveness

Miscellaneous:

- Course development is too far away from source of information; the risk of having the desired level of training is high
- The extra effort in communicating over 3000 + miles might still be easily underestimated

FRIGATE MANUFACTURING IMPACT

Strategy

- Use existing Nautilus facilities where possible
- Introduce Frigate modules on an existing line with L200 experience
- Utilize existing products/processes: Lower costs/ Better time-to-market

FRIGATE MANUFACTURING IMPACT

Product Milestones

- Module Prototype Builds - September 1986
- Final Breadboard Functional - November 1986
- Prototype System Builds - December 1986
- Start VMS Qualification - January 1987
- Start Field Test - April 1987
- Complete RQT - June 1987
- FRS - September 1987

FRIGATE MANUFACTURING IMPACT

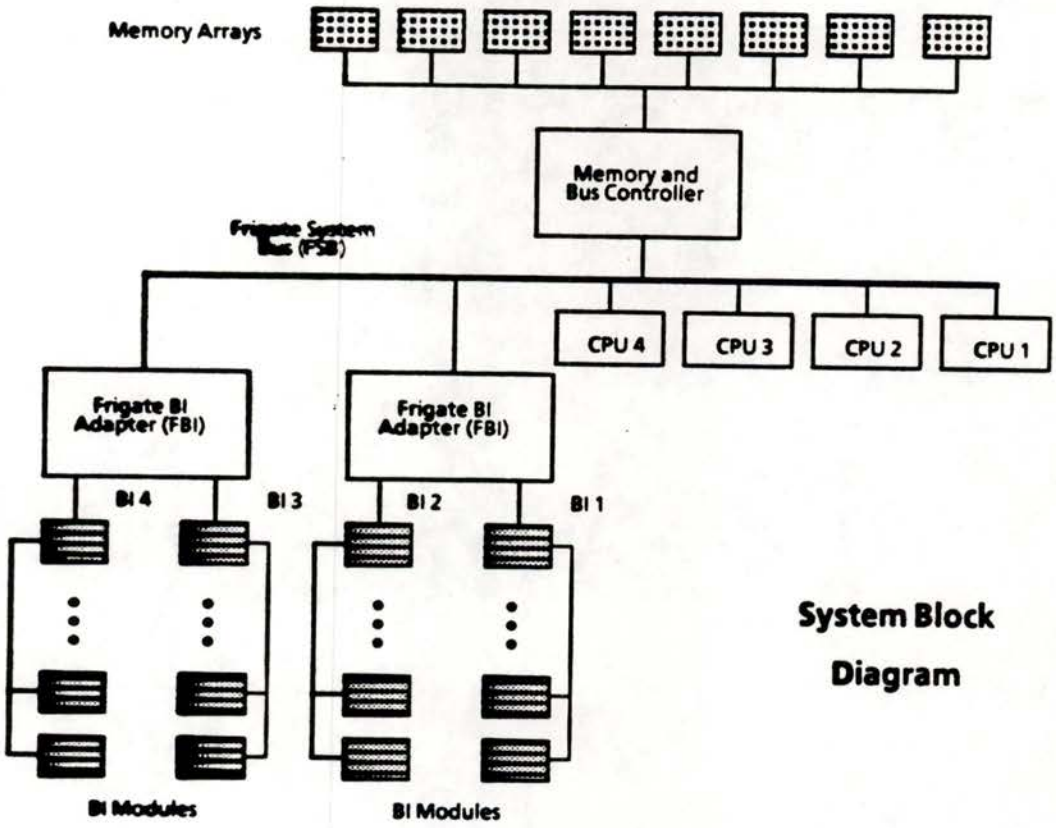
Impact by Plant

- Burlington (Stage 1 power):
  - Minimal = 5/6 people; 150K capital
- Kanata (Stage 1 Backplanes):
  - NPSU = $112K; Capital = $109K
- Far East (Stage 1 Memory):
  - Minimal
- Greenville (Stage 0 PC Boards):
  - Minimal (existing process)
- Salem (Stage 1):
  - Moderate: NPSU=$300K; Test=$350K
- Salem (Stage 2/3):
  - Significant: 60-85 People, $1-3M in capital.

Frigate

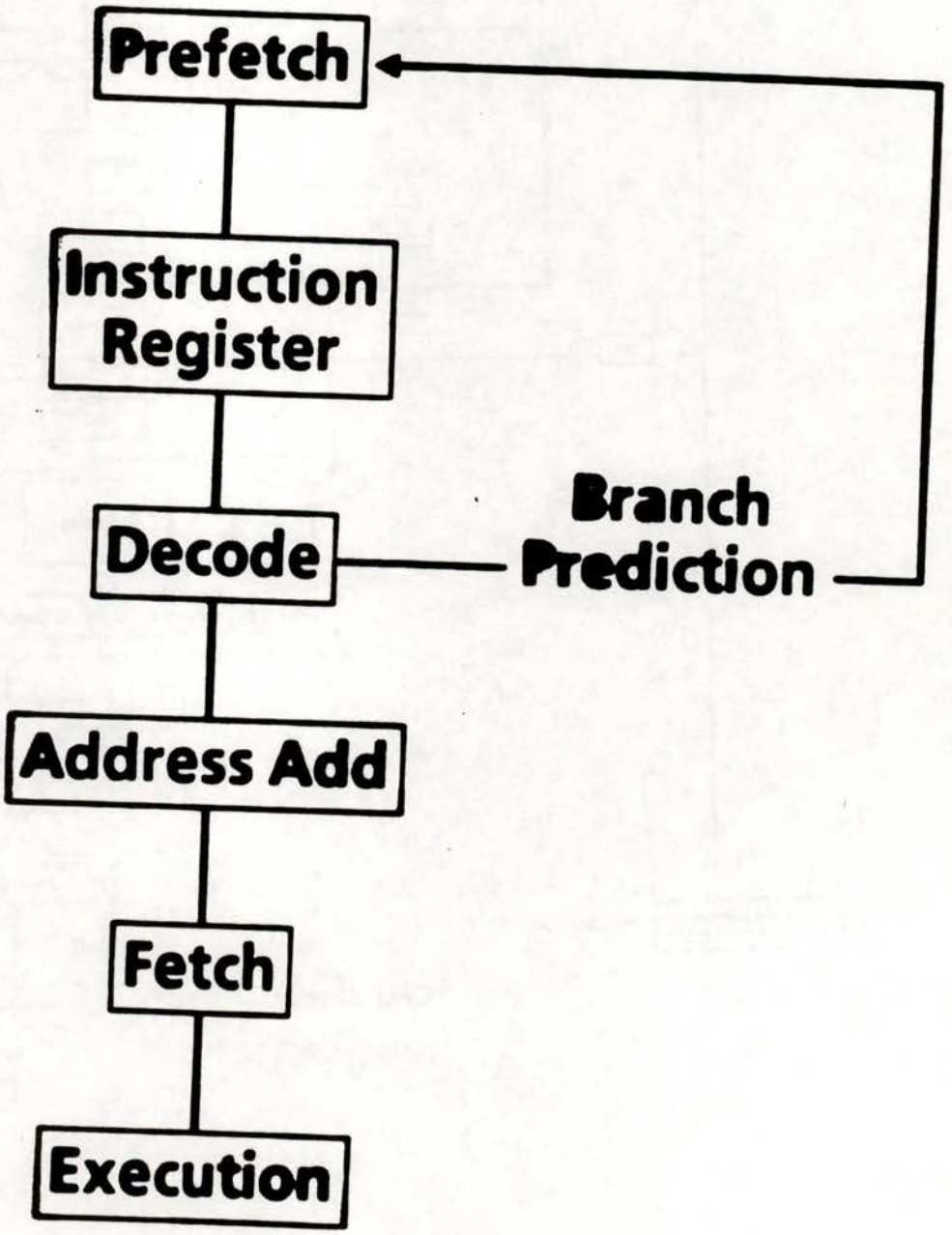
Technical

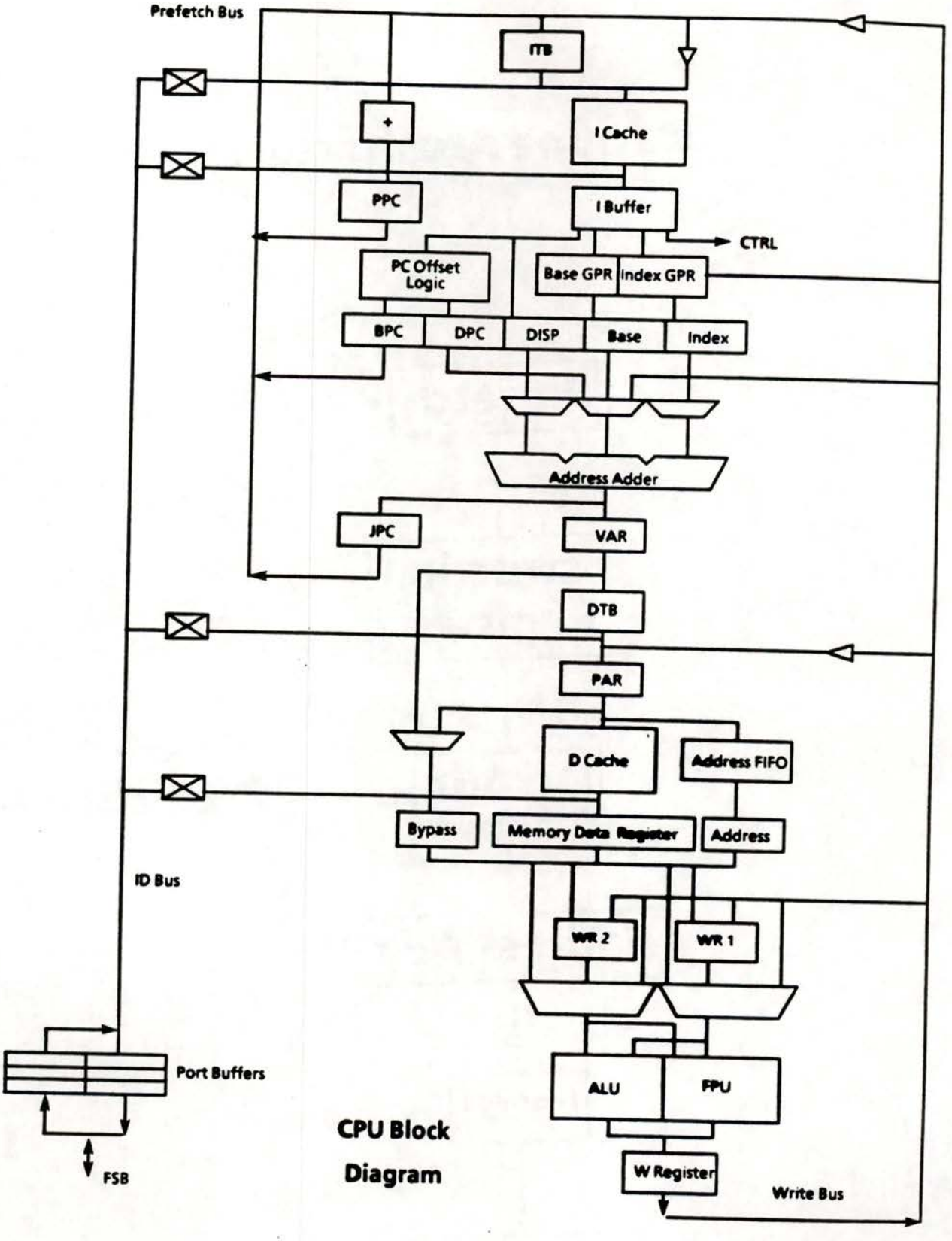
Review



System Block Diagram

Machine Architecture





CPU Block Diagram

Instruction Frequency Data
This data was collected on 4-FEB-1985 08:16:16.53
This data was written to dua1:[cutler]basketcpl.cod
Total number of instructions traced was 13514888
Number of character string instructions was 70040
Average character string length was 38

Pascal compiler compiling Forest's benchmarks

Name	Count	Percent	Cumula
MOVL	2529490	18.72	18.72
BNEQ	828999	6.13	24.85
BEQL	825662	6.11	30.96
CMPW	701968	5.19	36.15
CMPL	472978	3.50	39.65
CVTWL	458349	3.39	43.04
MOVW	348289	2.58	45.62
MOVZBL	336903	2.49	48.11
MOVAL	323971	2.40	50.51
BGEQ	244014	1.81	52.32
BBC	241611	1.79	54.11
CLRL	225928	1.67	55.78
RSB	224723	1.66	57.44
BRW	224336	1.66	59.10
BGTR	208121	1.54	60.64
MOVAB	206328	1.53	62.17
CMPB	199325	1.47	63.64
CVTBL	194324	1.44	65.08
PUSHL	193329	1.43	66.51
MOVZBW	190339	1.41	67.92
TSTL	188296	1.39	69.31
BRB	161229	1.19	70.50
ADDL2	150402	1.11	71.62
RET	148928	1.10	72.72
CALLS	146487	1.08	73.80
ADDL3	144462	1.07	74.87
MNEGW	138564	1.03	75.90
BLEQ	135176	1.00	76.90
AOBLEQ	132793	0.98	77.88
MOVB	132080	0.98	78.86
BSBW	129705	0.96	79.82
TSTW	118538	0.88	80.69
BLSS	116719	0.86	81.56
ACBL	111624	0.83	82.38
BBS	109237	0.81	83.19
JMP	108209	0.80	83.99
BLBC	101775	0.75	84.75
BSBB	96991	0.72	85.46
INCL	86593	0.64	86.10
AOBLSS	84428	0.62	86.73
SOBGTR	81381	0.60	87.33
SUBL3	78859	0.58	87.91
MOVZWL	77622	0.57	88.49
EXTZV	77292	0.57	89.06
BLBSU	74904	0.55	89.61
CASEB	73359	0.54	90.16
DECL	70382	0.52	90.68
CVTLW	64264	0.48	91.15
MULL3	61398	0.45	91.61
BBCC	61254	0.45	92.06

SUBL2	59508	0.44	92.50
INSV	58776	0.43	92.94
INCW	55387	0.41	93.35
SUBB3	48460	0.36	93.70
MNEGL	46440	0.34	94.05
JBB	41850	0.31	94.36
CLRB	40237	0.30	94.66
SUBB2	37479	0.28	94.93
MOVAW	32571	0.24	95.17
MULL2	31383	0.23	95.41
ASHL	29461	0.22	95.62
CVTBW	27580	0.20	95.83
BGTRU	27466	0.20	96.03
DECW	26323	0.19	96.23
CMPZV	25432	0.19	96.41
CLRW	24582	0.18	96.60
SOBGEQ	23767	0.18	96.77
PUSHAL	22872	0.17	96.94
REMQUE	22589	0.17	97.11
BLBS	22044	0.16	97.27
DIVL2	21572	0.16	97.43
MOVQ	19560	0.14	97.58
MOVC3	18091	0.13	97.71
MOVAQ	16537	0.12	97.83
INSQUE	15831	0.12	97.95
POPR	14178	0.10	98.05
BVS	13261	0.10	98.15
CLRQ	13227	0.10	98.25
MOVC5	13148	0.10	98.35
LOCC	12672	0.09	98.44
BGEQU	11056	0.08	98.52
TSTB	11001	0.08	98.60
ADDW3	10351	0.08	98.68
BICL2	10163	0.08	98.76
SPANC	9523	0.07	98.83
PUSHAB	9435	0.07	98.90
PUSHR	9257	0.07	98.96
BISL2	8776	0.06	99.03
ADDW2	8390	0.06	99.09
CMPC5	7139	0.05	99.14
BISB2	6960	0.05	99.20
CMPC3	6756	0.05	99.25
BICB3	5780	0.04	99.29
EDIV	5631	0.04	99.33
BVC	5442	0.04	99.37
EMUL	5185	0.04	99.41
BICW2	5181	0.04	99.45
PROBER	4948	0.04	99.48
ADDB3	4859	0.04	99.52
BICB2	4597	0.03	99.55
CASEW	4167	0.03	99.59
MCOML	4071	0.03	99.62
BICW3	3977	0.03	99.64
ACBB	3941	0.03	99.67
BLEQU	3522	0.03	99.70
SUBW3	3349	0.02	99.72
MOVTC	2511	0.02	99.74
BISB3	2470	0.02	99.76
CALLG	2443	0.02	99.78

SUBW2	2359	0.02	99.80
MNEGB	2215	0.02	99.81
CHME	2159	0.02	99.83
PUSHAQ	2002	0.01	99.84
EXTV	1941	0.01	99.86
BBBS	1595	0.01	99.87
BISL3	1533	0.01	99.88
BISW2	1440	0.01	99.89
CMPD	1034	0.01	99.90
PUSHAW	991	0.01	99.91
INCB	948	0.01	99.91
CVTLD	892	0.01	99.92
CVTLB	889	0.01	99.93
CHMK	838	0.01	99.93
FFS	789	0.01	99.94
CVTPL	769	0.01	99.95
SUBP6	768	0.01	99.95
MOVD	636	0.00	99.96
BISW3	620	0.00	99.96
BICL3	555	0.00	99.96
DIVL3	533	0.00	99.97
DECB	493	0.00	99.97
DIVW2	480	0.00	99.98
MCOMB	470	0.00	99.98
MCOMW	437	0.00	99.98
MULD3	400	0.00	99.99
ADDB2	335	0.00	99.99
BITW	288	0.00	99.99
BBSC	232	0.00	99.99
CVTDL	181	0.00	99.99
CVTWB	154	0.00	99.99
ADDD3	150	0.00	100.00
SKPC	142	0.00	100.00
TSTD	78	0.00	100.00
SUBD3	66	0.00	100.00
XORB2	65	0.00	100.00
MATCHC	58	0.00	100.00
BITL	54	0.00	100.00
CVTDF	39	0.00	100.00
DIVD2	34	0.00	100.00
BITB	31	0.00	100.00
CASEL	25	0.00	100.00
DIVD3	20	0.00	100.00
ACBW	16	0.00	100.00
DIVB3	11	0.00	100.00
ROTL	10	0.00	100.00
CVTLF	4	0.00	100.00
ADDD2	2	0.00	100.00
MULD2	2	0.00	100.00
DIVP	1	0.00	100.00
MNEGF	1	0.00	100.00

Instruction Size

Size	Count	Percent	Cumula
1	373651	2.76	2.76
2	3377042	24.99	27.75
3	3053412	22.59	50.35
4	2859321	21.16	71.50
5	2006192	14.84	86.35
6	726751	5.38	91.72
7	514500	3.81	95.53
8	411130	3.04	98.57
9	52660	0.39	98.96
10	132110	0.98	99.94
11	4790	0.04	99.98
12	2256	0.02	99.99
13	220	0.00	99.99
14	819	0.01	100.00
15	0	0.00	100.00
16	34	0.00	100.00
17	0	0.00	100.00
18	0	0.00	100.00
19	0	0.00	100.00
20	0	0.00	100.00
21	0	0.00	100.00
22	0	0.00	100.00
23	0	0.00	100.00
24	0	0.00	100.00
25	0	0.00	100.00
26	0	0.00	100.00
27	0	0.00	100.00
28	0	0.00	100.00
29	0	0.00	100.00
30	0	0.00	100.00
31	0	0.00	100.00
32	0	0.00	100.00
33	0	0.00	100.00
34	0	0.00	100.00
35	0	0.00	100.00
36	0	0.00	100.00
37	0	0.00	100.00
38	0	0.00	100.00
39	0	0.00	100.00
40	0	0.00	100.00

Average Instruction Size = 3.77

Specifier Size

Size	Count	Percent	Cumula
1	15935545	67.15	67.15
2	4223293	17.80	84.94
3	2401408	10.12	95.06
4	300665	1.27	96.33
5	636732	2.68	99.01
6	234895	0.99	100.00

Average Specifier Size = 1.58

Specifier Type (all)

Type	Count	Percent	Cumula
a=#0x	1893826	7.98	7.98
a=#1x	213046	0.90	8.88
a=#2x	116837	0.49	9.37
a=#3x	67119	0.28	9.65
[Rx]	1620620	6.83	16.48
Rn	8784726	37.02	53.50
(Rb)	639612	2.70	56.19
-(Rb)	155235	0.65	56.85
(Rb)+	1142089	4.81	61.66
-(Rb)+	10057	0.04	61.70
b=(Rb)	3129100	13.18	74.89
-b(Rb)	184080	0.78	75.66
w=(Rb)	1219662	5.14	80.80
-w(Rb)	22785	0.10	80.90
l=(Rb)	403799	1.70	82.60
-l(Rb)	47644	0.20	82.80
Bdb	3612679	15.22	98.02
Bdw	469622	1.98	100.00

Specifier Type (index)

Type	Count	Percent	Cumula
(Rb)	188020	11.60	11.60
-(Rb)	0	0.00	11.60
(Rb)+	0	0.00	11.60
-(Rb)+	0	0.00	11.60
b=(Rb)	798982	49.30	60.90
-b(Rb)	98058	6.05	66.95
w=(Rb)	294505	18.17	85.13
-w(Rb)	6160	0.38	85.51
l=(Rb)	221220	13.65	99.16
-l(Rb)	13675	0.84	100.00

Memory Reads Per Instruction

Number	Count	Percent	Cumula
0	7986052	59.09	59.09
1	5111791	37.82	96.91
2	411987	3.05	99.96
3	4980	0.04	100.00
4	78	0.00	100.00
5	0	0.00	100.00
6	0	0.00	100.00

Average Memory Reads Per Instruction = 0.44

Memory Writes Per Instruction

Number	Count	Percent	Cumula
0	11838839	87.60	87.60
1	1676049	12.40	100.00
2	0	0.00	100.00

Average Memory Writes Per Instruction = 0.12

Register Reads Per Instruction

Number	Count	Percent	Cumula
0	4222928	31.25	31.25
1	6428678	47.57	78.81
2	2460890	18.21	97.02
3	313746	2.32	99.34
4	83943	0.62	99.97
5	4703	0.03	100.00
6	0	0.00	100.00
7	0	0.00	100.00
8	0	0.00	100.00
9	0	0.00	100.00
10	0	0.00	100.00
11	0	0.00	100.00
12	0	0.00	100.00

Average Register Reads Per Instruction = 0.94

Register Writes Per Instruction

Number	Count	Percent	Cumula
0	8195039	60.64	60.64
1	5314218	39.32	99.96
2	5631	0.04	100.00

Average Register Writes Per Instruction = 0.39

Specifier Access Type

Type	Count	Percnt	Cumula
read	10962358	46.19	46.19
write	5974325	25.17	71.36
modify	1027204	4.33	75.69
addres	1108191	4.67	80.36
vfield	578159	2.44	82.80
branch	4082301	17.20	100.00

Total number of operand specifiers was 23732538
Number of nonfetch operand specifiers was 17120237
Percent of nonfetch operand specifiers was 72.14

BACPLANA.LOG;3 21-MAR-1985 17:58

```
Frigate 4 stage pipeline (tblcache) simulation model
Analysis of file dua1:basketcpl.cod
Simulation was run on 19-MAR-1985 13:58:41.95
Data cache miss rate is set at  5%
Number of cycles required for cache fill is set at 12
Data cache address miss rate is set at 25%
Data cache miss forced write rate is set at 33%
Dynamic branch prediction was used to predict conditional branches
    Branch table size is  4096 entries
    Branch counter width is     1 bits
    Branch block size is     4 bytes

Total number of simulation cycles =  61276780
Total number of instructions executed =  13514888
Average number of cycles per instruction =  4.53

Number of instructions that stop decode =     703773
Number of instructions that stop fetch =     616579
Total number of branching instructions =    4397539
Number of prefetch virtual page address matches =  60053979
Percent prefetch virtual page address matches =  98.00
Number of conditional branch instructions =    3032090
Percent conditional branch instructions =  68.95
Percent of branches predicted correctly =  75.86
Percent of branches incorrectly predicted =  24.14
Number of unconditional branches =     762320
Percent unconditional branches =  17.34
Number of instructions that stop pipe and then branch =     603129
Percent stop and branches =  13.72

          Pipeline Utilization Cycles

Stage          Idle      Stall       Wait       Work
Prefetch    39114649          0    7246738   14915393
Decode      15574204   15839969    9512558   20350049
Operand     29520286          0    8013724   23742770
Execute     25702357        353          0   35193869

Autoinc/dec register write wait cycles =       1072
Register base wait cycles =       7245
Double invalid register wait cycles =     367372
Indirect autoinc/dec register write wait cycles =          0
Instruction buffer dry wait cycles =    9136869

       Pipeline Utilization Percent

Stage      Idle Stall  Wait  Work
Prefetch   63.8   0.0  11.8  24.3
Decode     25.4  25.8  15.5  33.2
Operand    48.2   0.0  13.1  38.7
Execute    41.9   0.0   0.0  57.4
```

Time of execution

Instruction Cycles Data

Name	Cycles	Percnt	Cumula	Average
MOVL	8309551	13.56	13.56	3.29
MOVC5	4285216	6.99	20.55	325.92
RET	3948523	6.44	27.00	26.51
CALLS	3710647	6.06	33.05	25.33
BBC	2495831	4.07	37.13	10.33
CMPW	2282289	3.72	40.85	3.25
CVTWL	1457798	2.38	43.23	3.18
CMPL	1340884	2.19	45.42	2.83
MOVAL	1208928	1.97	47.39	3.73
MOVW	1154912	1.88	49.28	3.32
PUSHL	1089371	1.78	51.05	5.63
BBS	1056409	1.72	52.78	9.67
ACBL	1044245	1.70	54.48	9.36
MOVZBL	1041626	1.70	56.18	3.09
AOBLEQ	1033499	1.69	57.87	7.78
RSB	975572	1.59	59.46	4.34
MOVC3	965864	1.58	61.04	53.39
BEQL	950955	1.55	62.59	1.15
INSV	921261	1.50	64.09	15.67
BNEQ	919725	1.50	65.59	1.11
EXTZV	870415	1.42	67.01	11.26
BBCC	795070	1.30	68.31	12.98
CMPB	748890	1.22	69.53	3.76
CVTBL	709643	1.16	70.69	3.65
MOVAB	682655	1.11	71.80	3.31
CASEB	649259	1.06	72.86	8.85
MOVB	640672	1.05	73.91	4.85
MOVZBW	624650	1.02	74.93	3.28
BSBW	616226	1.01	75.94	4.75
BLBC	607456	0.99	76.93	5.97
AOBLSS	606527	0.99	77.92	7.18
JMP	600593	0.98	78.90	5.55
TSTL	568414	0.93	79.82	3.02
ADDL3	548250	0.89	80.72	3.80
CLRL	475772	0.78	81.50	2.11
REMQUE	449332	0.73	82.23	19.89
BRW	410096	0.67	82.90	1.83
SOBGTR	399682	0.65	83.55	4.91
DIVL2	368539	0.60	84.15	17.08
BSBB	366126	0.60	84.75	3.77
LOCC	338055	0.55	85.30	26.68
INSQUE	321214	0.52	85.82	20.29
TSTW	317614	0.52	86.34	2.68
MOVZWL	300692	0.49	86.83	3.87
CMPZV	298971	0.49	87.32	11.76
POPR	292421	0.48	87.80	20.62
MULL3	283325	0.46	88.26	4.61
SUBL2	277140	0.45	88.71	4.66
BGEQ	271330	0.44	89.16	1.11
SUBB3	271298	0.44	89.60	5.60
MNEGW	269424	0.44	90.04	1.94
SUBL3	261921	0.43	90.47	3.32
ADDL2	254391	0.42	90.88	1.69
INCL	249708	0.41	91.29	2.88
BRB	240941	0.39	91.68	1.49
BGTR	238209	0.39	92.07	1.14

CVTLW	228328	0.37	92.44	3.55
JSB	213123	0.35	92.79	5.09
MOVTC	196676	0.32	93.11	78.33
PUSHR	194830	0.32	93.43	21.05
SPANC	194460	0.32	93.75	20.42
CLRB	180548	0.29	94.04	4.49
BLBS	173132	0.28	94.32	7.85
BLEQ	148659	0.24	94.57	1.10
SOBGEQ	148334	0.24	94.81	6.24
MOVQ	148109	0.24	95.05	7.57
INCW	147384	0.24	95.29	2.66
CMPC3	143180	0.23	95.53	21.19
CMPC5	135765	0.22	95.75	19.02
CVTBW	132509	0.22	95.96	4.80
BLSS	130000	0.21	96.18	1.11
PUSHAL	120961	0.20	96.37	5.29
EDIV	111807	0.18	96.56	19.86
ASHL	106923	0.17	96.73	3.63
MULL2	106238	0.17	96.90	3.39
DECL	103344	0.17	97.07	1.47
SUBB2	101504	0.17	97.24	2.71
MOVAW	98100	0.16	97.40	3.01
MNEGL	96503	0.16	97.55	2.08
SUBP6	86063	0.14	97.70	112.06
BLSSU	84830	0.14	97.83	1.13
CALLG	81992	0.13	97.97	33.56
CVTPL	79976	0.13	98.10	104.00
CLRQ	77886	0.13	98.23	5.89
CLRW	77152	0.13	98.35	3.14
BGTRU	69251	0.11	98.46	2.52
DECW	65645	0.11	98.57	2.49
PROBER	59808	0.10	98.67	12.09
PUSHAB	44795	0.07	98.74	4.75
TSTB	41313	0.07	98.81	3.76
CASEW	38471	0.06	98.87	9.23
EMUL	36341	0.06	98.93	7.01
MOVAQ	35747	0.06	98.99	2.16
CHME	34146	0.06	99.05	15.82
ACBB	31335	0.05	99.10	7.95
BISB2	30676	0.05	99.15	4.41
BICB3	30247	0.05	99.20	5.23
ADDB3	30155	0.05	99.25	6.21
ADDW3	29640	0.05	99.29	2.86
BICL2	27803	0.05	99.34	2.74
BVS	26522	0.04	99.38	2.00
ADDW2	25666	0.04	99.42	3.06
EXTV	24520	0.04	99.46	12.63
BISL2	22187	0.04	99.50	2.53
SUBW3	21143	0.03	99.53	6.31
CMPD	18919	0.03	99.57	18.30
BICB2	17430	0.03	99.59	3.79
CHMK	17202	0.03	99.62	20.53
BGEQU	16165	0.03	99.65	1.46
BICW2	15748	0.03	99.67	3.04
BBSS	15106	0.02	99.70	9.47
BISB3	12997	0.02	99.72	5.26
DIVL3	12540	0.02	99.74	23.53
BICW3	10955	0.02	99.76	2.75
MULD3	10773	0.02	99.78	26.93

MCOML	10550	0.02	99.81	2.59
PUSHAQ	9731	0.02	99.83	4.86
FFS	9156	0.01	99.84	11.60
BLEQU	8487	0.01	99.86	2.41
DIVW2	8160	0.01	99.87	17.00
BVC	7324	0.01	99.88	1.35
BISL3	6967	0.01	99.89	4.54
BISW2	6797	0.01	99.90	4.72
CVTLD	6720	0.01	99.91	7.53
CVTLB	6212	0.01	99.92	6.99
PUSHAW	4674	0.01	99.93	4.72
MOVD	4541	0.01	99.94	7.14
MATCHC	3777	0.01	99.95	65.12
ADDD3	3661	0.01	99.95	24.41
BISW3	3651	0.01	99.96	5.89
SUBW2	2552	0.00	99.96	1.08
DIVD2	2528	0.00	99.97	74.35
SKPC	2088	0.00	99.97	14.70
SUBD3	2000	0.00	99.97	30.30
INCB	1911	0.00	99.98	2.02
BBSC	1876	0.00	99.98	8.09
ADDB2	1789	0.00	99.98	5.34
MCOMB	1535	0.00	99.98	3.27
DIVD3	1534	0.00	99.99	76.70
BICL3	1342	0.00	99.99	2.42
BITW	1215	0.00	99.99	4.22
MCOMW	1165	0.00	99.99	2.67
DECB	1068	0.00	99.99	2.17
CVTDL	773	0.00	100.00	4.27
CVTWB	486	0.00	100.00	3.16
BITL	440	0.00	100.00	8.15
TSTD	417	0.00	100.00	5.35
CVTDF	317	0.00	100.00	8.13
DIVB3	252	0.00	100.00	22.91
CASEL	229	0.00	100.00	9.16
ACBW	128	0.00	100.00	8.00
DIVP	116	0.00	100.00	116.00
XORB2	75	0.00	100.00	1.15
BITB	75	0.00	100.00	2.42
ROTL	58	0.00	100.00	5.80
CVTLF	40	0.00	100.00	10.00
MULD2	39	0.00	100.00	19.50
ADDD2	26	0.00	100.00	13.00
MNEGF	22	0.00	100.00	22.00

Frigate 4 stage pipeline (tblcache) simulation model
Analysis of file dua1:basketcpl.cod
Simulation was run on 20-MAR-1985 05:24:49.55
Data cache miss rate is set at 5%
Number of cycles required for cache fill is set at 12
Data cache address miss rate is set at 50%
Data cache miss forced write rate is set at 33%
Dynamic branch prediction was used to predict conditional branches
    Branch table size is 4096 entries
    Branch counter width is 1 bits
    Branch block size is 4 bytes

Total number of simulation cycles = 63182119
Total number of instructions executed = 13514888
Average number of cycles per instruction = 4.68

Number of instructions that stop decode = 703773
Number of instructions that stop fetch = 616579
Total number of branching instructions = 4397539
Number of prefetch virtual page address matches = 61958941
Percent prefetch virtual page address matches = 98.06
Number of conditional branch instructions = 3032090
Percent conditional branch instructions = 68.95
Percent of branches predicted correctly = 75.08
Percent of branches incorrectly predicted = 24.92
Number of unconditional branches = 762320
Percent unconditional branches = 17.34
Number of instructions that stop pipe and then branch = 603129
Percent stop and branches = 13.72

Pipeline Utilization Cycles

Stage	Idle	Stall	Wait	Work
Prefetch	40989665	0	7268821	14923633
Decode	15572922	17908472	9344657	20356068
Operand	29400169	0	10062174	23719776
Execute	27607526	523	0	35194904

Autoinc/dec register write wait cycles = 794
Register base wait cycles = 7281
Double invalid register wait cycles = 302280
Indirect autoinc/dec register write wait cycles = 0
Instruction buffer dry wait cycles = 9034302

Pipeline Utilization Percent

Stage	Idle	Stall	Wait	Work
Prefetch	64.9	0.0	11.5	23.6
Decode	24.6	28.3	14.8	32.2
Operand	46.5	0.0	15.9	37.5
Execute	43.7	0.0	0.0	55.7

Instruction Cycles Data

Name	Cycles	Percnt	Cumula	Average
MOVL	8881086	14.06	14.06	3.51
MOVC5	4285702	6.78	20.84	325.96
RET	3946875	6.25	27.09	26.50
CALLS	3708042	5.87	32.96	25.31
BBC	2495075	3.95	36.90	10.33
CMPW	2409390	3.81	40.72	3.43
CVTWL	1559042	2.47	43.19	3.40
CMPL	1414983	2.24	45.43	2.99
MOVAL	1259247	1.99	47.42	3.89
MOVW	1227908	1.94	49.36	3.53
PUSHL	1146438	1.81	51.18	5.93
MOVZBL	1118294	1.77	52.95	3.32
ACBL	1075799	1.70	54.65	9.64
BBS	1057472	1.67	56.32	9.68
AOBLEQ	1038120	1.64	57.97	7.82
RSB	1025552	1.62	59.59	4.56
MOVC3	967564	1.53	61.12	53.48
BEQL	950026	1.50	62.62	1.15
INSV	924495	1.46	64.09	15.73
BNEQ	916860	1.45	65.54	1.11
EXTZV	872632	1.38	66.92	11.29
CMPB	807628	1.28	68.20	4.05
BBCC	794618	1.26	69.46	12.97
CVTBL	778276	1.23	70.69	4.01
MOVAB	695152	1.10	71.79	3.37
CASEB	680965	1.08	72.87	9.28
MOVZBW	679086	1.07	73.94	3.57
MOVB	673914	1.07	75.01	5.10
BSBW	646424	1.02	76.03	4.98
BLBC	622050	0.98	77.01	6.11
JMP	619456	0.98	78.00	5.72
AOBLSS	607907	0.96	78.96	7.20
TSTL	591726	0.94	79.89	3.14
ADDL3	574816	0.91	80.80	3.98
CLRL	495652	0.78	81.59	2.19
REMQUE	453373	0.72	82.31	20.07
SOBGTR	412456	0.65	82.96	5.07
BRW	408511	0.65	83.61	1.82
BSBB	385337	0.61	84.22	3.97
DIVL2	368869	0.58	84.80	17.10
TSTW	346388	0.55	85.35	2.92
LOCC	342064	0.54	85.89	26.99
INSQUE	324872	0.51	86.40	20.52
MOVZWL	316390	0.50	86.90	4.08
CMPZV	298346	0.47	87.38	11.73
MULL3	295557	0.47	87.84	4.81
POPR	293760	0.46	88.31	20.72
SUBB3	283246	0.45	88.76	5.84
MNEGW	279947	0.44	89.20	2.02
SUBL2	279491	0.44	89.64	4.70
BGEQ	271828	0.43	90.07	1.11
SUBL3	269382	0.43	90.50	3.42
ADDL2	261015	0.41	90.91	1.74
INCL	260378	0.41	91.32	3.01
CVTLW	249937	0.40	91.72	3.89
BRB	240239	0.38	92.10	1.49

BGTR	228982	0.36	92.46	1.10
JSB	224202	0.35	92.82	5.36
SPANC	197134	0.31	93.13	20.70
PUSHR	196866	0.31	93.44	21.27
MOVTC	196722	0.31	93.75	78.34
CLRB	185121	0.29	94.04	4.60
BLBS	174873	0.28	94.32	7.93
INCW	161230	0.26	94.58	2.91
MOVQ	153851	0.24	94.82	7.87
SOBGEQ	148761	0.24	95.06	6.26
BLEQ	148358	0.23	95.29	1.10
CMPC3	143044	0.23	95.52	21.17
CVTBW	137575	0.22	95.73	4.99
CMPC5	136939	0.22	95.95	19.18
BLSS	129710	0.21	96.16	1.11
PUSHAL	126019	0.20	96.36	5.51
EDIV	112195	0.18	96.53	19.92
SUBB2	111508	0.18	96.71	2.98
ASHL	111061	0.18	96.89	3.77
MULL2	108120	0.17	97.06	3.45
DECL	105538	0.17	97.22	1.50
MNEGL	104126	0.16	97.39	2.24
MOVAW	100741	0.16	97.55	3.09
SUBP6	85944	0.14	97.68	111.91
BLSSU	84817	0.13	97.82	1.13
CLRW	82524	0.13	97.95	3.36
CLRQ	82109	0.13	98.08	6.21
CALLG	81740	0.13	98.21	33.46
CVTPL	79976	0.13	98.34	104.00
DECW	71497	0.11	98.45	2.72
BGTRU	68919	0.11	98.56	2.51
PROBER	59764	0.09	98.65	12.08
PUSHAB	48530	0.08	98.73	5.14
TSTB	44498	0.07	98.80	4.04
CASEW	38493	0.06	98.86	9.24
EMUL	36351	0.06	98.92	7.01
MOVAQ	35899	0.06	98.97	2.17
CHME	34730	0.05	99.03	16.09
BICB3	34621	0.05	99.08	5.99
BISB2	33230	0.05	99.14	4.77
ACBB	32241	0.05	99.19	8.18
ADDB3	31507	0.05	99.24	6.48
ADDW3	30387	0.05	99.29	2.94
BICL2	29634	0.05	99.33	2.92
ADDW2	27885	0.04	99.38	3.32
BVS	26522	0.04	99.42	2.00
EXTV	24792	0.04	99.46	12.77
BISL2	23161	0.04	99.49	2.64
SUBW3	22380	0.04	99.53	6.68
BICB2	19839	0.03	99.56	4.32
CMPD	19115	0.03	99.59	18.49
CHMK	17227	0.03	99.62	20.56
BICW2	16769	0.03	99.65	3.24
BGEQU	16123	0.03	99.67	1.46
BBSS	15115	0.02	99.70	9.48
BISB3	13514	0.02	99.72	5.47
DIVL3	12693	0.02	99.74	23.81
BICW3	12118	0.02	99.76	3.05
MCOML	11910	0.02	99.77	2.93

MNEGB	11101	0.02	99.81	5.01
PUSHAQ	10339	0.02	99.83	5.16
FFS	9119	0.01	99.84	11.56
BLEQU	8487	0.01	99.85	2.41
DIVW2	8160	0.01	99.87	17.00
BISL3	7902	0.01	99.88	5.15
BVC	7317	0.01	99.89	1.34
CVTLD	7180	0.01	99.90	8.05
BISW2	7176	0.01	99.91	4.98
CVTLB	6193	0.01	99.92	6.97
PUSHAW	4893	0.01	99.93	4.94
MOVD	4858	0.01	99.94	7.64
BISW3	4040	0.01	99.95	6.52
ADDD3	3832	0.01	99.95	25.55
MATCHC	3777	0.01	99.96	65.12
SUBW2	2627	0.00	99.96	1.11
DIVD2	2425	0.00	99.97	71.32
SKPC	2089	0.00	99.97	14.71
SUBD3	2048	0.00	99.97	31.03
INCB	2011	0.00	99.98	2.12
BBSC	1901	0.00	99.98	8.19
ADDB2	1856	0.00	99.98	5.54
DIVD3	1561	0.00	99.98	78.05
MCOMB	1535	0.00	99.99	3.27
BICL3	1358	0.00	99.99	2.45
BITW	1280	0.00	99.99	4.44
MCOMW	1270	0.00	99.99	2.91
DECB	1190	0.00	99.99	2.41
CVTDL	761	0.00	100.00	4.20
CVTWB	462	0.00	100.00	3.00
TSTD	417	0.00	100.00	5.35
BITL	402	0.00	100.00	7.44
CVTDF	399	0.00	100.00	10.23
DIVB3	251	0.00	100.00	22.82
CASEL	229	0.00	100.00	9.16
ACBW	128	0.00	100.00	8.00
DIVP	116	0.00	100.00	116.00
BITB	106	0.00	100.00	3.42
XORB2	78	0.00	100.00	1.20
ROTL	60	0.00	100.00	6.00
CVTLF	39	0.00	100.00	9.75
MULD2	28	0.00	100.00	14.00
ADDD2	26	0.00	100.00	13.00
MNEGF	22	0.00	100.00	22.00

```
Frigate 4 stage pipeline (tblcache) simulation model
Analysis of file dua1:basketcpl.cod
Simulation was run on 20-MAR-1985 21:57:40.15
Data cache miss rate is set at  5%
Number of cycles required for cache fill is set at 12
Data cache address miss rate is set at 75%
Data cache miss forced write rate is set at 33%
Dynamic branch prediction was used to predict conditional branches
    Branch table size is  4096 entries
    Branch counter width is    1 bits
    Branch block size is     4 bytes

Total number of simulation cycles =  65020551
Total number of instructions executed =  13514888
Average number of cycles per instruction =  4.81

Number of instructions that stop decode =    703773
Number of instructions that stop fetch =    616579
Total number of branching instructions =   4397539
Number of prefetch virtual page address matches =  63797408
Percent prefetch virtual page address matches =  98.12
Number of conditional branch instructions =   3032090
Percent conditional branch instructions =  68.95
Percent of branches predicted correctly =  75.62
Percent of branches incorrectly predicted =  24.38
Number of unconditional branches =    762320
Percent unconditional branches =  17.34
Number of instructions that stop pipe and then branch =    603129
Percent stop and branches =  13.72

          Pipeline Utilization Cycles

Stage          Idle      Stall       Wait       Work
Prefetch    42824370          0    7263976   14932205
Decode      15559449   19976264    9148646   20336192
Operand     29181843          0   12120480   23718228
Execute     29445844        637          0   35195087

Autoinc/dec register write wait cycles =        534
Register base wait cycles =       7322
Double invalid register wait cycles =     240537
Indirect autoinc/dec register write wait cycles =          0
Instruction buffer dry wait cycles =    8900253

      Pipeline Utilization Percent

Stage      Idle Stall  Wait  Work
Prefetch   65.9   0.0  11.2  23.0
Decode     23.9  30.7  14.1  31.3
Operand    44.9   0.0  18.6  36.5
Execute    45.3   0.0   0.0  54.1
```

12%

Instruction Cycles Data

Name	Cycles	Percnt	Cumula	Average
MOVL	9400315	14.46	14.46	3.72
MOVC5	4286869	6.59	21.05	326.05
RET	3946890	6.07	27.12	26.50
CALLS	3705085	5.70	32.82	25.29
CMPW	2536159	3.90	36.72	3.61
BBC	2493054	3.83	40.55	10.32
CVTWL	1655450	2.55	43.10	3.61
CMPL	1484965	2.28	45.38	3.14
MOVW	1307398	2.01	47.39	3.75
MOVAL	1305737	2.01	49.40	4.03
PUSHL	1206021	1.85	51.26	6.24
MOVZBL	1191487	1.83	53.09	3.54
ACBL	1108137	1.70	54.79	9.93
RSB	1078877	1.66	56.45	4.80
BBS	1058624	1.63	58.08	9.69
AOBLEQ	1043808	1.61	59.69	7.86
MOVC3	968296	1.49	61.18	53.52
BEQL	949343	1.46	62.64	1.15
INSV	927373	1.43	64.06	15.78
BNEQ	913974	1.41	65.47	1.10
EXTZV	875847	1.35	66.82	11.33
CMPB	867988	1.33	68.15	4.35
CVTBL	845808	1.30	69.45	4.35
BBCC	795237	1.22	70.67	12.98
MOVZBW	730162	1.12	71.80	3.84
CASEB	713096	1.10	72.89	9.72
MOVB	712841	1.10	73.99	5.40
MOVAB	708985	1.09	75.08	3.44
BSBW	675756	1.04	76.12	5.21
JMP	638011	0.98	77.10	5.90
BLBC	635990	0.98	78.08	6.25
TSTL	611047	0.94	79.02	3.25
AOBLSS	609211	0.94	79.96	7.22
ADDL3	598834	0.92	80.88	4.15
CLRL	513182	0.79	81.67	2.27
REMQUE	457803	0.70	82.37	20.27
SOBGTR	422454	0.65	83.02	5.19
BRW	407280	0.63	83.65	1.82
BSBB	401894	0.62	84.26	4.14
TSTW	375771	0.58	84.84	3.17
DIVL2	368909	0.57	85.41	17.10
LOCC	344416	0.53	85.94	27.18
MOVZWL	330776	0.51	86.45	4.26
INSQUE	328325	0.50	86.95	20.74
MULL3	305743	0.47	87.42	4.98
CMPZV	297999	0.46	87.88	11.72
SUBB3	296182	0.46	88.34	6.11
POPR	295273	0.45	88.79	20.83
MNEGW	290462	0.45	89.24	2.10
SUBL2	280993	0.43	89.67	4.72
SUBL3	277927	0.43	90.10	3.52
BGEQ	272464	0.42	90.52	1.12
INCL	272267	0.42	90.94	3.14
CVTLW	271962	0.42	91.35	4.23
ADDL2	267696	0.41	91.77	1.78
BRB	239282	0.37	92.13	1.48

JSB	234084	0.36	92.49	5.59
BGTR	222789	0.34	92.84	1.07
SPANC	199527	0.31	93.14	20.95
PUSHR	198278	0.30	93.45	21.42
MOVTC	196674	0.30	93.75	78.32
CLRB	192731	0.30	94.05	4.79
BLBS	175927	0.27	94.32	7.98
INCW	175087	0.27	94.59	3.16
MOVQ	158407	0.24	94.83	8.10
SOBGEQ	149362	0.23	95.06	6.28
BLEQ	147789	0.23	95.29	1.09
CMPC3	143098	0.22	95.51	21.18
CVTBW	142887	0.22	95.73	5.18
CMPC5	138150	0.21	95.94	19.35
PUSHAL	131427	0.20	96.14	5.75
BLSS	129534	0.20	96.34	1.11
SUBB2	120846	0.19	96.53	3.22
ASHL	115330	0.18	96.70	3.91
MNEGL	113079	0.17	96.88	2.43
EDIV	112518	0.17	97.05	19.98
MULL2	110859	0.17	97.22	3.53
DECL	106216	0.16	97.39	1.51
MOVAW	103229	0.16	97.54	3.17
CLRQ	87653	0.13	97.68	6.63
CLRW	87188	0.13	97.81	3.55
SUBP6	85845	0.13	97.94	111.78
BLSSU	84791	0.13	98.08	1.13
CALLG	81880	0.13	98.20	33.52
CVTPL	79976	0.12	98.32	104.00
DECW	78046	0.12	98.44	2.96
BGTRU	68622	0.11	98.55	2.50
PROBER	59775	0.09	98.64	12.08
PUSHAB	50109	0.08	98.72	5.31
TSTB	46732	0.07	98.79	4.25
CASEW	38537	0.06	98.85	9.25
BICB3	37718	0.06	98.91	6.53
EMUL	36407	0.06	98.96	7.02
MOVAQ	36167	0.06	99.02	2.19
CHME	35248	0.05	99.07	16.33
BISB2	34837	0.05	99.13	5.01
ACBB	33197	0.05	99.18	8.42
ADDB3	32876	0.05	99.23	6.77
BICL2	31809	0.05	99.28	3.13
ADDW3	31156	0.05	99.33	3.01
ADDW2	30647	0.05	99.37	3.65
BVS	26522	0.04	99.41	2.00
EXTV	24995	0.04	99.45	12.88
BISL2	24262	0.04	99.49	2.76
SUBW3	24046	0.04	99.53	7.18
BICB2	21460	0.03	99.56	4.67
CMPD	19492	0.03	99.59	18.85
BICW2	17920	0.03	99.62	3.46
CHMK	17523	0.03	99.64	20.91
BGEQU	16328	0.03	99.67	1.08
BBSS	15097	0.02	99.69	9.47
BISB3	14553	0.02	99.71	5.89
BICW3	13071	0.02	99.73	3.29
MCOML	12762	0.02	99.75	3.13
DIVL3	12717	0.02	99.77	23.86

MULD3	11597	0.02	99.81	28.99
PUSHAQ	10433	0.02	99.83	5.21
FFS	9047	0.01	99.84	11.47
BISL3	8864	0.01	99.85	5.78
BLEQU	8485	0.01	99.87	2.41
DIVW2	8160	0.01	99.88	17.00
BISW2	7496	0.01	99.89	5.21
CVTLD	7372	0.01	99.90	8.26
BVC	7317	0.01	99.91	1.34
CVTLB	6094	0.01	99.92	6.85
MOVD	5469	0.01	99.93	8.60
PUSHAW	5363	0.01	99.94	5.41
BISW3	4354	0.01	99.95	7.02
ADDD3	3931	0.01	99.95	26.21
MATCHC	3777	0.01	99.96	65.12
SUBW2	2619	0.00	99.96	1.11
DIVD2	2490	0.00	99.97	73.24
INCB	2252	0.00	99.97	2.38
SUBD3	2097	0.00	99.97	31.77
SKPC	2088	0.00	99.98	14.70
BBSC	1965	0.00	99.98	8.47
ADDB2	1899	0.00	99.98	5.67
DIVD3	1591	0.00	99.98	79.55
MCOMB	1522	0.00	99.99	3.24
MCOMW	1465	0.00	99.99	3.35
DECB	1326	0.00	99.99	2.69
BICL3	1326	0.00	99.99	2.39
BITW	1260	0.00	99.99	4.38
CVTDL	765	0.00	100.00	4.23
CVTWB	545	0.00	100.00	3.54
TSTD	414	0.00	100.00	5.31
CVTDF	410	0.00	100.00	10.51
BITL	399	0.00	100.00	7.39
DIVB3	250	0.00	100.00	22.73
CASEL	223	0.00	100.00	8.92
BITB	153	0.00	100.00	4.94
ACBW	128	0.00	100.00	8.00
DIVP	116	0.00	100.00	116.00
XORB2	73	0.00	100.00	1.12
ROTL	70	0.00	100.00	7.00
CVTLF	57	0.00	100.00	14.25
MULD2	39	0.00	100.00	19.50
ADDD2	26	0.00	100.00	13.00
MNEGF	24	0.00	100.00	24.00

```
Frigate 4 stage pipeline (tblcache) simulation model
Analysis of file dua0:basketcpl.cod
Simulation was run on 28-MAR-1985 12:03:01.37
Data cache miss rate is set at 10%
Number of cycles required for cache fill is set at 12
Data cache address miss rate is set at 25%
Data cache miss forced write rate is set at 33%
Dynamic branch prediction was used to predict conditional branches
    Branch table size is  4096 entries
    Branch counter width is    1 bits
    Branch block size is     4 bytes

Total number of simulation cycles =  66374095
Total number of instructions executed =  13514888
Average number of cycles per instruction =  4.91

Number of instructions that stop decode =     703773
Number of instructions that stop fetch =     616579
Total number of branching instructions =    4397539
Number of prefetch virtual page address matches =  65151202
Percent prefetch virtual page address matches =  98.16
Number of conditional branch instructions =    3032090
Percent conditional branch instructions =  68.95
Percent of branches predicted correctly =  76.47
Percent of branches incorrectly predicted =  23.53
Number of unconditional branches =     762320
Percent unconditional branches =  17.34
Number of instructions that stop pipe and then branch =     603129
Percent stop and branches =  13.72

          Pipeline Utilization Cycles

Stage          Idle      Stall       Wait       Work
Prefetch    44200688          0    7279869   14893538
Decode      15569808   21091105    9388191   20324991
Operand     29381738          0   13256293   23736064
Execute     30799568        457          0   35194476

Autoinc/dec register write wait cycles =       1068
Register base wait cycles =       7374
Double invalid register wait cycles =     356624
Indirect autoinc/dec register write wait cycles =          0
Instruction buffer dry wait cycles =    9023125

       Pipeline Utilization Percent

Stage      Idle Stall  Wait  Work
Prefetch   66.6   0.0  11.0  22.4
Decode     23.5  31.8  14.1  30.6
Operand    44.3   0.0  20.0  35.8
Execute    46.4   0.0   0.0  53.0
```

Instruction Cycles Data

Name	Cycles	Percnt	Cumula	Average
MOVL	9757859	14.70	14.70	3.86
MOVC5	4287742	6.46	21.16	326.11
RET	3948443	5.95	27.11	26.51
CALLS	3708788	5.59	32.70	25.32
CMPW	2564539	3.86	36.56	3.65
BBC	2495380	3.76	40.32	10.33
CVTWL	1732823	2.61	42.93	3.78
CMPL	1521181	2.29	45.22	3.22
MOVW	1392860	2.10	47.32	4.00
MOVAL	1357383	2.05	49.37	4.19
PUSHL	1271109	1.92	51.28	6.57
MOVZBL	1247457	1.88	53.16	3.70
ACBL	1123165	1.69	54.85	10.06
RSB	1112264	1.68	56.53	4.95
BBS	1058396	1.59	58.12	9.69
AOBLEQ	1044543	1.57	59.70	7.87
MOVC3	969373	1.46	61.16	53.58
BEQL	947102	1.43	62.59	1.15
INSV	930216	1.40	63.99	15.83
BNEQ	915618	1.38	65.37	1.10
CMPB	904163	1.36	66.73	4.54
CVTBL	883320	1.33	68.06	4.55
EXTZV	877275	1.32	69.38	11.35
BBCC	794425	1.20	70.58	12.97
MOVZBW	755202	1.14	71.72	3.97
MOVB	752445	1.13	72.85	5.70
MOVAB	722301	1.09	73.94	3.50
BSBW	720686	1.09	75.02	5.56
CASEB	697717	1.05	76.07	9.51
TSTL	652498	0.98	77.06	3.47
JMP	644489	0.97	78.03	5.96
BLBC	639942	0.96	78.99	6.29
ADDL3	624846	0.94	79.93	4.33
AOBLSS	609602	0.92	80.85	7.22
CLRL	539928	0.81	81.67	2.39
REMQUE	459938	0.69	82.36	20.36
BSBB	443213	0.67	83.03	4.57
BRW	408470	0.62	83.64	1.82
SOBGTR	403455	0.61	84.25	4.96
TSTW	388428	0.59	84.84	3.28
DIVL2	369202	0.56	85.39	17.11
LOCC	346174	0.52	85.91	27.32
MOVZWL	342290	0.52	86.43	4.41
INSQUE	330101	0.50	86.93	20.85
MULL3	309186	0.47	87.39	5.04
SUBB3	300199	0.45	87.84	6.19
CMPZV	298590	0.45	88.29	11.74
MNEGW	297560	0.45	88.74	2.15
POPR	297334	0.45	89.19	20.97
CVTLW	290686	0.44	89.63	4.52
SUBL3	286116	0.43	90.06	3.63
INCL	284127	0.43	90.49	3.28
SUBL2	282555	0.43	90.91	4.75
ADDL2	279170	0.42	91.33	1.86
BGEQ	270762	0.41	91.74	1.11
JSB	249050	0.38	92.12	5.95

BRB	240604	0.36	92.48	1.49
BGTR	235189	0.35	92.83	1.13
CLRB	204153	0.31	93.14	5.07
SPANC	200302	0.30	93.44	21.03
PUSHR	199776	0.30	93.74	21.58
MOVTC	196702	0.30	94.04	78.30
INCW	179701	0.27	94.31	3.24
BLBS	176940	0.27	94.58	8.03
MOVQ	165137	0.25	94.83	8.44
SOBGEQ	148349	0.22	95.05	6.24
BLEQ	148310	0.22	95.27	1.10
CVTBW	146145	0.22	95.49	5.30
CMPC3	143855	0.22	95.71	21.29
CMPC5	139183	0.21	95.92	19.50
PUSHAL	138872	0.21	96.13	6.07
BLSS	129817	0.20	96.32	1.11
SUBB2	123635	0.19	96.51	3.30
MNEGL	116424	0.18	96.69	2.51
ASHL	116135	0.17	96.86	3.94
EDIV	112917	0.17	97.03	20.05
MULL2	111192	0.17	97.20	3.54
MOVAW	108526	0.16	97.36	3.33
DECL	107613	0.16	97.52	1.53
CLRQ	93781	0.14	97.67	7.09
CLRW	93558	0.14	97.81	3.81
SUBP6	86204	0.13	97.94	112.24
BLSSU	84806	0.13	98.06	1.13
CALLG	82249	0.12	98.19	33.67
DECW	80288	0.12	98.31	3.05
CVTPL	79976	0.12	98.43	104.00
BGTRU	69034	0.10	98.53	2.51
PROBER	59777	0.09	98.62	12.08
PUSHAB	53442	0.08	98.70	5.66
TSTB	48371	0.07	98.78	4.40
BICB3	40093	0.06	98.84	6.94
CASEW	38482	0.06	98.90	9.23
MOVAQ	38169	0.06	98.95	2.31
EMUL	36350	0.05	99.01	7.01
BISB2	35583	0.05	99.06	5.11
CHME	35513	0.05	99.12	16.45
ADDB3	34118	0.05	99.17	7.02
ACBB	33729	0.05	99.22	8.56
ADDW3	32834	0.05	99.27	3.17
ADDW2	32182	0.05	99.32	3.84
BICL2	31772	0.05	99.36	3.13
BVS	26522	0.04	99.40	2.00
SUBW3	25345	0.04	99.44	7.57
EXTV	25289	0.04	99.48	13.03
BISL2	24958	0.04	99.52	2.84
BICB2	22605	0.03	99.55	4.92
CMPD	19650	0.03	99.58	19.00
BICW2	18881	0.03	99.61	3.64
CHMK	17879	0.03	99.64	21.34
BGEQU	16563	0.02	99.66	1.50
BISB3	15373	0.02	99.68	6.22
MCOML	15237	0.02	99.71	3.74
BBSS	15148	0.02	99.73	9.50
BICW3	13864	0.02	99.75	3.49
DIVL3	12969	0.02	99.77	24.33

MULD3	11965	0.02	99.81	29.91
PUSHAQ	11154	0.02	99.82	5.57
BISL3	9481	0.01	99.84	6.18
FFS	9069	0.01	99.85	11.49
BLEQU	8483	0.01	99.86	2.41
CVTLD	8237	0.01	99.88	9.23
DIVW2	8160	0.01	99.89	17.00
BISW2	8094	0.01	99.90	5.62
BVC	7324	0.01	99.91	1.35
CVTLB	6285	0.01	99.92	7.07
PUSHAW	5654	0.01	99.93	5.71
MOVD	5552	0.01	99.94	8.73
BISW3	4765	0.01	99.95	7.69
ADDD3	4020	0.01	99.95	26.80
MATCHC	3798	0.01	99.96	65.48
SUBW2	2590	0.00	99.96	1.10
DIVD2	2440	0.00	99.97	71.76
INCB	2265	0.00	99.97	2.39
SUBD3	2252	0.00	99.97	34.12
SKPC	2089	0.00	99.98	14.71
ADDB2	2054	0.00	99.98	6.13
BBSC	1894	0.00	99.98	8.16
DIVD3	1681	0.00	99.98	84.05
MCOMB	1537	0.00	99.99	3.27
MCOMW	1483	0.00	99.99	3.39
BICL3	1387	0.00	99.99	2.50
BITW	1318	0.00	99.99	4.58
DECB	1164	0.00	99.99	2.36
CVTDL	767	0.00	100.00	4.24
CVTWB	587	0.00	100.00	3.81
TSTD	420	0.00	100.00	5.38
CVTDF	349	0.00	100.00	8.95
BITL	333	0.00	100.00	6.17
DIVB3	276	0.00	100.00	25.09
CASEL	234	0.00	100.00	9.36
BITB	131	0.00	100.00	4.23
ACBW	128	0.00	100.00	8.00
DIVP	116	0.00	100.00	116.00
XORB2	75	0.00	100.00	1.15
ROTL	66	0.00	100.00	6.60
MULD2	40	0.00	100.00	20.00
CVTLF	38	0.00	100.00	9.50
ADDD2	26	0.00	100.00	13.00
MNEGF	23	0.00	100.00	23.00

BACPLAN2.LOG;2 30-MAR-1985 13:25

Frigate 4 stage pipeline (thicache) simulation model
Analysis of file dua0:basketcpl.cod
Simulation was run on 29-MAR-1985 04:21:03.75
Data cache miss rate is set at 10%
Number of cycles required for cache fill is set at 12
Data cache address miss rate is set at 50%
Data cache miss forced write rate is set at 33%
Dynamic branch prediction was used to predict conditional branches
    Branch table size is 4096 entries
    Branch counter width is 1 bits
    Branch block size is 4 bytes

Total number of simulation cycles = 68349082
Total number of instructions executed = 13514888
Average number of cycles per instruction = 5.06

Number of instructions that stop decode = 703773
Number of instructions that stop fetch = 616579
Total number of branching instructions = 4397539
Number of prefetch virtual page address matches = 67126067
Percent prefetch virtual page address matches = 98.21
Number of conditional branch instructions = 3032090
Percent conditional branch instructions = 68.95
Percent of branches predicted correctly = 75.10
Percent of branches incorrectly predicted = 24.90
Number of unconditional branches = 762320
Percent unconditional branches = 17.34
Number of instructions that stop pipe and then branch = 603129
Percent stop and branches = 13.72

Pipeline Utilization Cycles

Stage	Idle	Stall	Wait	Work
Prefetch	46113769	0	7300167	14935146
Decode	15561566	23166015	9264851	20356650
Operand	29312801	0	15311852	23724429
Execute	32774365	647	0	35195412

Autoinc/dec register write wait cycles = 782
Register base wait cycles = 7451
Double invalid register wait cycles = 295395
Indirect autoinc/dec register write wait cycles = 0
Instruction buffer dry wait cycles = 8961223

Pipeline Utilization Percent

Stage	Idle	Stall	Wait	Work
Prefetch	67.5	0.0	10.7	21.9
Decode	22.8	33.9	13.6	29.8
Operand	42.9	0.0	22.4	34.7
Execute	48.0	0.0	0.0	51.5

Instruction Cycles Data

Name	Cycles	Percnt	Cumula	Average
MOVL	10385814	15.20	15.20	4.11
MOVC5	4286909	6.28	21.47	326.20
RET	3947729	5.78	27.25	26.51
CALLS	3706296	5.42	32.67	25.30
CMPW	2698802	3.95	36.62	3.84
BBC	2494139	3.65	40.27	10.32
CVTWL	1830301	2.68	42.94	3.99
CMPL	1593708	2.33	45.28	3.37
MOVW	1468677	2.15	47.42	4.22
MOVAL	1408404	2.06	49.49	4.35
PUSHL	1332799	1.95	51.44	6.89
MOVZBL	1322221	1.93	53.37	3.92
RSB	1159111	1.70	55.07	5.16
ACBL	1156460	1.69	56.76	10.36
BBS	1059808	1.55	58.31	9.70
AOBLEQ	1050441	1.54	59.85	7.91
MOVC3	971024	1.42	61.27	53.67
CMPB	965662	1.41	62.68	4.84
CVTBL	951344	1.39	64.07	4.90
BEQL	946886	1.39	65.46	1.15
INSV	933566	1.37	66.82	15.88
BNEQ	913601	1.34	68.16	1.10
EXTZV	881396	1.29	69.45	11.40
MOVZBW	812197	1.19	70.64	4.27
BBCC	794970	1.16	71.80	12.98
MOVB	788136	1.15	72.95	5.97
BSBW	749081	1.10	74.05	5.78
MOVAB	736518	1.08	75.13	3.57
CASEB	728412	1.07	76.19	9.93
TSTL	674707	0.99	77.18	3.58
JMP	664168	0.97	78.15	6.14
BLBC	653922	0.96	79.11	6.43
ADDL3	653284	0.96	80.06	4.52
AOBLSS	610591	0.89	80.96	7.23
CLRL	556839	0.81	81.77	2.46
REMQUE	464248	0.68	82.45	20.55
BSBB	460585	0.67	83.12	4.75
TSTW	417493	0.61	83.74	3.52
SOBGTR	415075	0.61	84.34	5.10
BRW	407978	0.60	84.94	1.82
DIVL2	369176	0.54	85.48	17.11
MOVZWL	356864	0.52	86.00	4.60
LOCC	349026	0.51	86.51	27.54
INSQUE	333057	0.49	87.00	21.04
MULL3	321349	0.47	87.47	5.23
CVTLW	313728	0.46	87.93	4.88
SUBB3	310675	0.45	88.38	6.41
MNEGW	305381	0.45	88.83	2.20
POPR	298805	0.44	89.27	21.08
CMPZV	296805	0.43	89.70	11.67
INCL	296406	0.43	90.14	3.42
SUBL3	295558	0.43	90.57	3.75
ADDL2	287043	0.42	90.99	1.91
SUBL2	284804	0.42	91.40	4.79
BGEQ	271271	0.40	91.80	1.11
JSB	258888	0.38	92.18	6.19

BRB	239673	0.35	92.53	1.49
BGTR	227190	0.33	92.86	1.09
CLRB	210850	0.31	93.17	5.24
SPANC	202368	0.30	93.47	21.25
PUSHR	201290	0.29	93.76	21.74
MOVTC	196668	0.29	94.05	78.32
INCW	193355	0.28	94.33	3.49
BLBS	179313	0.26	94.60	8.13
MOVQ	171197	0.25	94.85	8.75
CVTBW	151404	0.22	95.07	5.49
SOBGEQ	148738	0.22	95.28	6.26
BLEQ	147562	0.22	95.50	1.09
PUSHAL	145777	0.21	95.71	6.37
CMPC3	143838	0.21	95.92	21.29
CMPC5	140459	0.21	96.13	19.67
SUBB2	134326	0.20	96.33	3.58
BLSS	129325	0.19	96.52	1.11
MNEGL	123569	0.18	96.70	2.66
ASHL	120847	0.18	96.87	4.10
EDIV	113691	0.17	97.04	20.19
MULL2	113555	0.17	97.21	3.62
MOVAW	109937	0.16	97.37	3.38
DECL	108277	0.16	97.52	1.54
CLRW	99630	0.15	97.67	4.05
CLRQ	98281	0.14	97.81	7.43
DECW	87377	0.13	97.94	3.32
SUBP6	86349	0.13	98.07	112.43
BLSSU	84796	0.12	98.19	1.13
CALLG	82065	0.12	98.31	33.59
CVTPL	79976	0.12	98.43	104.00
BGTRU	68381	0.10	98.53	2.49
PROBER	59760	0.09	98.62	12.08
PUSHAB	55627	0.08	98.70	5.90
TSTB	50835	0.07	98.77	4.62
BICB3	43376	0.06	98.84	7.50
CASEW	38465	0.06	98.89	9.23
MOVAQ	37825	0.06	98.95	2.29
BISB2	37542	0.05	99.00	5.39
EMUL	36340	0.05	99.06	7.01
CHME	35841	0.05	99.11	16.60
ADDB3	35528	0.05	99.16	7.31
ACBB	34820	0.05	99.21	8.84
BICL2	34671	0.05	99.26	3.41
ADDW2	34558	0.05	99.31	4.12
ADDW3	33603	0.05	99.36	3.25
SUBW3	26956	0.04	99.40	8.05
BVS	26522	0.04	99.44	2.00
BISL2	25833	0.04	99.48	2.94
EXTV	25313	0.04	99.52	13.04
BICB2	23507	0.03	99.55	5.11
BICW2	20031	0.03	99.58	3.87
CMPD	19848	0.03	99.61	19.20
CHMK	17950	0.03	99.63	21.42
BISB3	16345	0.02	99.66	6.62
MCOML	16242	0.02	99.68	3.99
BGEQU	16229	0.02	99.71	1.47
BBSS	15128	0.02	99.73	9.48
BICW3	14807	0.02	99.75	3.72
DIVL3	12986	0.02	99.77	24.36

MULD3	12853	0.02	99.81	32.13
PUSHAQ	12174	0.02	99.82	6.08
BISL3	10373	0.02	99.84	6.77
FFS	9057	0.01	99.85	11.48
BISW2	8718	0.01	99.86	6.05
CVTLD	8512	0.01	99.88	9.54
BLEQU	8483	0.01	99.89	2.41
DIVW2	8160	0.01	99.90	17.00
BVC	7317	0.01	99.91	1.34
MOVD	6255	0.01	99.92	9.83
CVTLB	6255	0.01	99.93	7.04
PUSHAW	5764	0.01	99.94	5.84
BISW3	5066	0.01	99.95	8.17
ADDD3	4193	0.01	99.95	27.95
MATCHC	3777	0.01	99.96	65.12
SUBW2	2632	0.00	99.96	1.12
DIVD2	2518	0.00	99.97	74.06
INCB	2419	0.00	99.97	2.55
SUBD3	2271	0.00	99.97	34.41
SKPC	2088	0.00	99.98	14.70
ADDB2	2062	0.00	99.98	6.16
BBSC	1935	0.00	99.98	8.34
DIVD3	1659	0.00	99.98	82.95
MCOMW	1630	0.00	99.99	3.73
MCOMB	1533	0.00	99.99	3.24
BICL3	1395	0.00	99.99	2.51
BITW	1325	0.00	99.99	4.60
DECB	1310	0.00	99.99	2.66
CVTDL	777	0.00	100.00	4.29
CVTWB	542	0.00	100.00	3.52
TSTD	420	0.00	100.00	5.38
CVTDF	406	0.00	100.00	10.41
BITL	346	0.00	100.00	6.41
DIVB3	297	0.00	100.00	27.00
CASEL	212	0.00	100.00	8.48
BITB	132	0.00	100.00	4.26
ACBW	128	0.00	100.00	8.00
DIVP	116	0.00	100.00	116.00
XORB2	74	0.00	100.00	1.14
CVTLF	67	0.00	100.00	16.75
ROTL	67	0.00	100.00	6.70
MULD2	38	0.00	100.00	19.00
ADDD2	26	0.00	100.00	13.00
MNEGF	23	0.00	100.00	23.00

```
Frigate 4 stage pipeline (tblcache) simulation model
Analysis of file dua0:basketcpl.cod
Simulation was run on 29-MAR-1985 22:07:20.88
Data cache miss rate is set at 10%
Number of cycles required for cache fill is set at 12
Data cache address miss rate is set at 75%
Data cache miss forced write rate is set at 33%
Dynamic branch prediction was used to predict conditional branches
    Branch table size is  4096 entries
    Branch counter width is    1 bits
    Branch block size is    4 bytes

Total number of simulation cycles =  70113969
Total number of instructions executed =  13514888
Average number of cycles per instruction =  5.19

Number of instructions that stop decode =    703773
Number of instructions that stop fetch =    616579
Total number of branching instructions =   4397539
Number of prefetch virtual page address matches =  68890638
Percent prefetch virtual page address matches =  98.26
Number of conditional branch instructions =   3032090
Percent conditional branch instructions =  68.95
Percent of branches predicted correctly =  76.58
Percent of branches incorrectly predicted =  23.42
Number of unconditional branches =    762320
Percent unconditional branches =  17.34
Number of instructions that stop pipe and then branch =    603129
Percent stop and branches =  13.72

         Pipeline Utilization Cycles

Stage          Idle      Stall       Wait       Work
Prefetch    47936981          0    7279567   14897421
Decode      15555367   25210337    9044634   20303631
Operand     29048917          0   17352496   23714556
Execute     34539216        683          0   35195438

Autoinc/dec register write wait cycles =        506
Register base wait cycles =       7563
Double invalid register wait cycles =    236576
Indirect autoinc/dec register write wait cycles =          0
Instruction buffer dry wait cycles =   8799989

      Pipeline Utilization Percent

Stage      Idle Stall  wait  Work
Prefetch   68.4   0.0  10.4  21.2
Decode     22.2  36.0  12.9  29.0
Operand    41.4   0.0  24.7  33.8
Execute    49.3   0.0   0.0  50.2
```

Instruction Cycles Data

Name	Cycles	Percent	Cumula	Average
MOVL	10825776	15.44	15.44	4.28
MOVC5	4289695	6.12	21.56	326.26
RET	3947680	5.63	27.19	26.51
CALLS	3703943	5.28	32.47	25.29
CMPW	2821909	4.02	36.50	4.02
BBC	2491372	3.55	40.05	10.31
CVTWL	1926608	2.75	42.80	4.20
CMPL	1662723	2.37	45.17	3.52
MOVW	1547613	2.21	47.38	4.44
MOVAL	1463405	2.09	49.46	4.52
MOVZBL	1395595	1.99	51.45	4.14
PUSHL	1389143	1.98	53.44	7.19
RSB	1214257	1.73	55.17	5.40
ACBL	1188780	1.70	56.86	10.65
BBS	1061904	1.51	58.38	9.72
AOBLEQ	1056455	1.51	59.88	7.96
CMPB	1027152	1.46	61.35	5.15
CVTBL	1016640	1.45	62.80	5.23
MOVC3	971856	1.39	64.18	53.72
BEQL	946004	1.35	65.53	1.15
INSV	937378	1.34	66.87	15.95
BNEQ	910838	1.30	68.17	1.10
EXTZV	884532	1.26	69.43	11.44
MOVZBW	862807	1.23	70.66	4.53
MOVB	822639	1.17	71.84	6.23
BBCC	794816	1.13	72.97	12.98
BSBW	779174	1.11	74.08	6.01
CASEB	759767	1.08	75.16	10.36
MOVAB	748847	1.07	76.23	3.63
TSTL	700910	1.00	77.23	3.72
JMP	683407	0.97	78.21	6.32
ADDL3	678398	0.97	79.17	4.70
BLBC	666944	0.95	80.13	6.55
AOBLSS	612460	0.87	81.00	7.25
CLRL	577445	0.82	81.82	2.56
BSBB	476932	0.68	82.50	4.92
REMQUE	468293	0.67	83.17	20.73
TSTW	445016	0.63	83.81	3.75
SOBGTR	424107	0.60	84.41	5.21
BRW	406582	0.58	84.99	1.81
MOVZWL	371268	0.53	85.52	4.78
DIVL2	369516	0.53	86.05	17.13
LOCC	352595	0.50	86.55	27.82
INSQUE	337293	0.48	87.03	21.31
CVTLW	334443	0.48	87.51	5.20
MULL3	332534	0.47	87.98	5.42
SUBB3	324511	0.46	88.44	6.70
MNEGW	315867	0.45	88.90	2.28
INCL	307177	0.44	89.33	3.55
SUBL3	304912	0.43	89.77	3.87
POPR	300128	0.43	90.20	21.17
CMPZV	296419	0.42	90.62	11.66
ADDL2	292084	0.42	91.04	1.94
SUBL2	286732	0.41	91.44	4.82
BGEQ	271909	0.39	91.83	1.11
JSB	271403	0.39	92.22	6.49

BRB	239106	0.34	92.56	1.48
BGTR	221552	0.32	92.88	1.06
CLRB	215869	0.31	93.18	5.36
INCW	206876	0.30	93.48	3.74
SPANC	204938	0.29	93.77	21.52
PUSHR	202940	0.29	94.06	21.92
MOVTC	196711	0.28	94.34	78.34
BLBS	179464	0.26	94.60	8.14
MOVQ	178806	0.26	94.85	9.14
CVTBW	157790	0.23	95.08	5.72
SOBGEQ	149286	0.21	95.29	6.28
PUSHAL	148441	0.21	95.50	6.49
BLEQ	147151	0.21	95.71	1.09
CMPC3	143713	0.20	95.92	21.27
SUBB2	143418	0.20	96.12	3.83
CMPC5	142186	0.20	96.32	19.92
MNEGL	131633	0.19	96.51	2.83
BLBS	129167	0.18	96.70	1.11
ASHL	125662	0.18	96.88	4.27
MULL2	116480	0.17	97.04	3.71
EDIV	113822	0.16	97.20	20.21
MOVAW	112480	0.16	97.36	3.45
DECL	109566	0.16	97.52	1.56
CLRW	102864	0.15	97.67	4.18
CLRQ	101637	0.14	97.81	7.68
DECW	93448	0.13	97.95	3.55
SUBP6	86329	0.12	98.07	112.41
BLSSU	84791	0.12	98.19	1.13
CALLG	82064	0.12	98.31	33.59
CVTPL	79976	0.11	98.42	104.00
BGTRU	68127	0.10	98.52	2.48
PROBER	59724	0.09	98.60	12.07
PUSHAB	58150	0.08	98.69	6.16
TSTB	53376	0.08	98.76	4.85
BICB3	47262	0.07	98.83	8.18
BISB2	39871	0.06	98.89	5.73
CASEW	38480	0.05	98.94	9.23
MOVAQ	38029	0.05	99.00	2.30
ADDB3	37049	0.05	99.05	7.62
ADDW2	37003	0.05	99.10	4.41
CHME	36840	0.05	99.15	17.06
EMUL	36324	0.05	99.21	7.01
BICL2	36071	0.05	99.26	3.55
ACBB	35821	0.05	99.31	9.09
ADDW3	34475	0.05	99.36	3.33
SUBW3	28210	0.04	99.40	8.42
BISL2	27145	0.04	99.44	3.09
BVS	26522	0.04	99.47	2.00
BICB2	25845	0.04	99.51	5.62
EXTV	25712	0.04	99.55	13.25
BICW2	20954	0.03	99.58	4.04
CMPD	20666	0.03	99.61	19.99
CHMK	18232	0.03	99.63	21.76
MCOML	17542	0.03	99.66	4.31
BISB3	16992	0.02	99.68	6.88
BGEQU	16360	0.02	99.71	1.48
BICW3	15664	0.02	99.73	3.94
BBSS	15125	0.02	99.75	9.48
MNEGB	13318	0.02	99.77	6.01

MULD3	13016	0.02	99.81	32.54
PUSHAQ	12408	0.02	99.82	6.20
BISL3	11029	0.02	99.84	7.19
FFS	9084	0.01	99.85	11.51
CVTLD	8969	0.01	99.87	10.05
BISW2	8615	0.01	99.88	5.98
BLEQU	8483	0.01	99.89	2.41
DIVW2	8160	0.01	99.90	17.00
BVC	7324	0.01	99.91	1.35
MOVD	6667	0.01	99.92	10.48
CVTLB	6354	0.01	99.93	7.15
PUSHAW	6013	0.01	99.94	6.07
BISW3	5597	0.01	99.95	9.03
ADDD3	4595	0.01	99.95	30.63
MATCHC	3777	0.01	99.96	65.12
SUBW2	2707	0.00	99.96	1.15
DIVD2	2541	0.00	99.97	74.74
INCB	2485	0.00	99.97	2.62
SUBD3	2303	0.00	99.97	34.89
SKPC	2110	0.00	99.98	14.86
ADDB2	2066	0.00	99.98	6.17
BBSC	1969	0.00	99.98	8.49
DIVD3	1799	0.00	99.98	89.95
MCOMW	1757	0.00	99.99	4.02
MCOMB	1522	0.00	99.99	3.24
DECB	1499	0.00	99.99	3.04
BICL3	1344	0.00	99.99	2.42
BITW	1291	0.00	99.99	4.48
CVTDL	763	0.00	100.00	4.22
CVTWB	627	0.00	100.00	4.07
TSTD	417	0.00	100.00	5.35
CVTDF	415	0.00	100.00	10.64
BITL	289	0.00	100.00	5.35
DIVB3	261	0.00	100.00	23.73
CASEL	223	0.00	100.00	8.92
ACBW	128	0.00	100.00	8.00
DIVP	116	0.00	100.00	116.00
BITB	99	0.00	100.00	3.19
CVTLF	76	0.00	100.00	19.00
XORB2	73	0.00	100.00	1.12
ROTL	60	0.00	100.00	6.00
MULD2	28	0.00	100.00	14.00
ADDD2	26	0.00	100.00	13.00
MNEGF	25	0.00	100.00	25.00

FRIGATE SYSTEM BUS

- o 64 Bit data path
- o Synchronous 70 nS cycle
- o 76Mbyte / second usable bandwidth
- o Error detection and recovery
- o Central arbitration
- o Aligned transfers
- o TTL (Fast series) drivers and receivers
- o Tri-state

Arbitration

- Centrally controlled
- Two level fixed priority

  with round-robin between devices at same level
- I/O adapters have highest priority
- CPU's have lower priority
- Two transactions may be active simultaneously

Transaction Types

- Read: Word, Long, Quad, Octa
- Read Interlocked: Word, long
- Write masked: Long
- Write: Quad, Octa
- Write Cached: ~~Octa~~ Quad
- Write Invalidate: Quad, Octa
- Write unlock
- Interlock / unlock
- Interprocessor Interrupt

INTERRUPTS

- Interprocessor interrupts
- Memory controller
- FSB adapter interrupts
- BI device interrupts
- BI -unibus interrupts
- Power fail

Error Recovery

- Parity is checked on each transfer
- Transmitted data is saved in a "shadow" register
- Any bus device may detect an error
- Detector asserts error, causing master to abort
- Master retries using the saved data and control

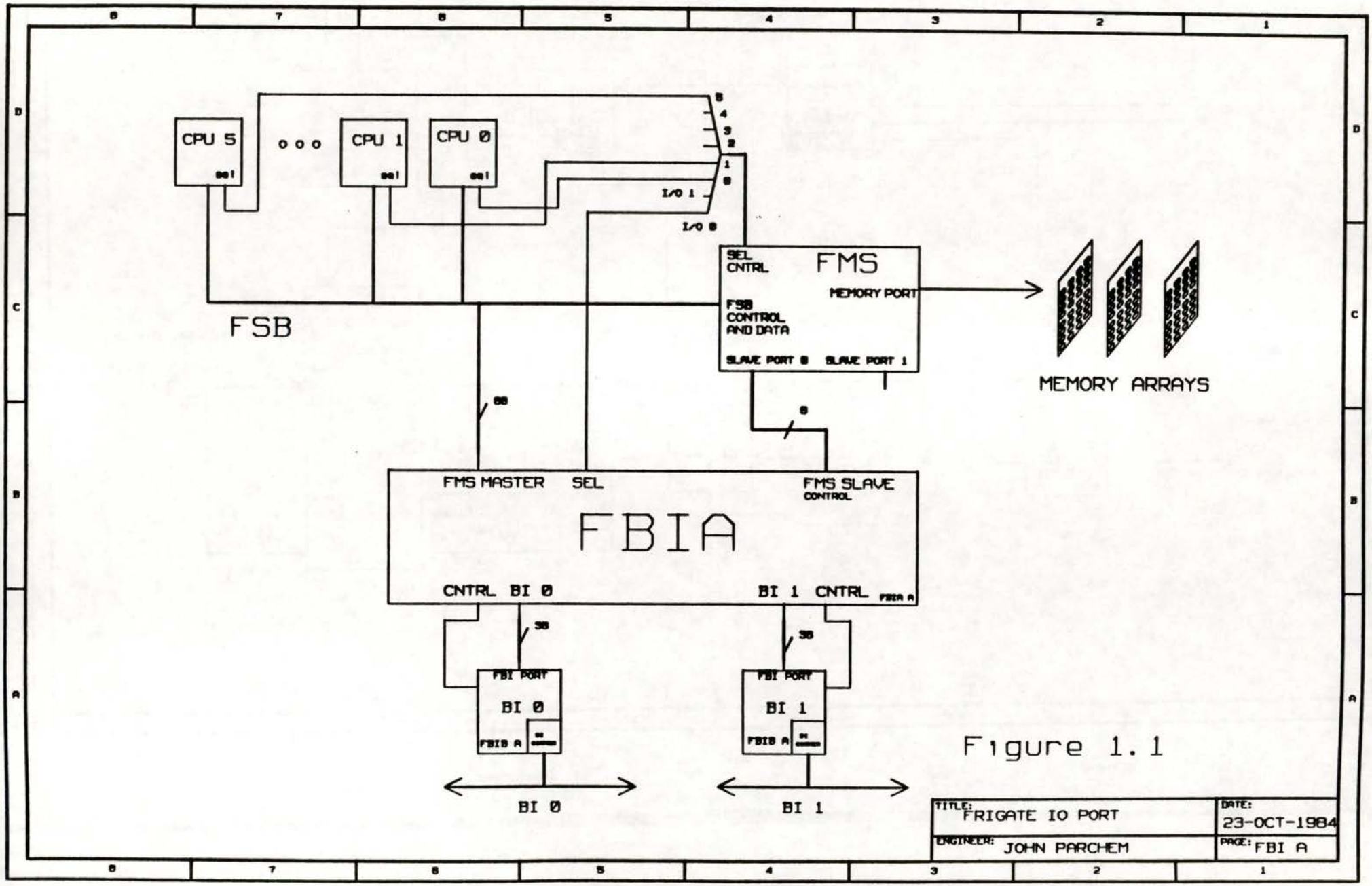

CPU 5
CPU 1
CPU 0
FSB
I/O 1
I/O 0
SEL CNTRL
FMS
MEMORY PORT
FSB CONTROL AND DATA
SLAVE PORT 0
SLAVE PORT 1
MEMORY ARRAYS
FMS MASTER SEL
FMS SLAVE CONTROL
FBIA
CNTRL BI 0
BI 1 CNTRL
FBI PORT
BI 0
FBIB A
BI 1
BI 0
BI 1
TITLE: FRIGATE IO PORT
DATE: 23-OCT-1984
ENGINEER: JOHN PARCHEM
PAGE: FBI A

Figure 1.1

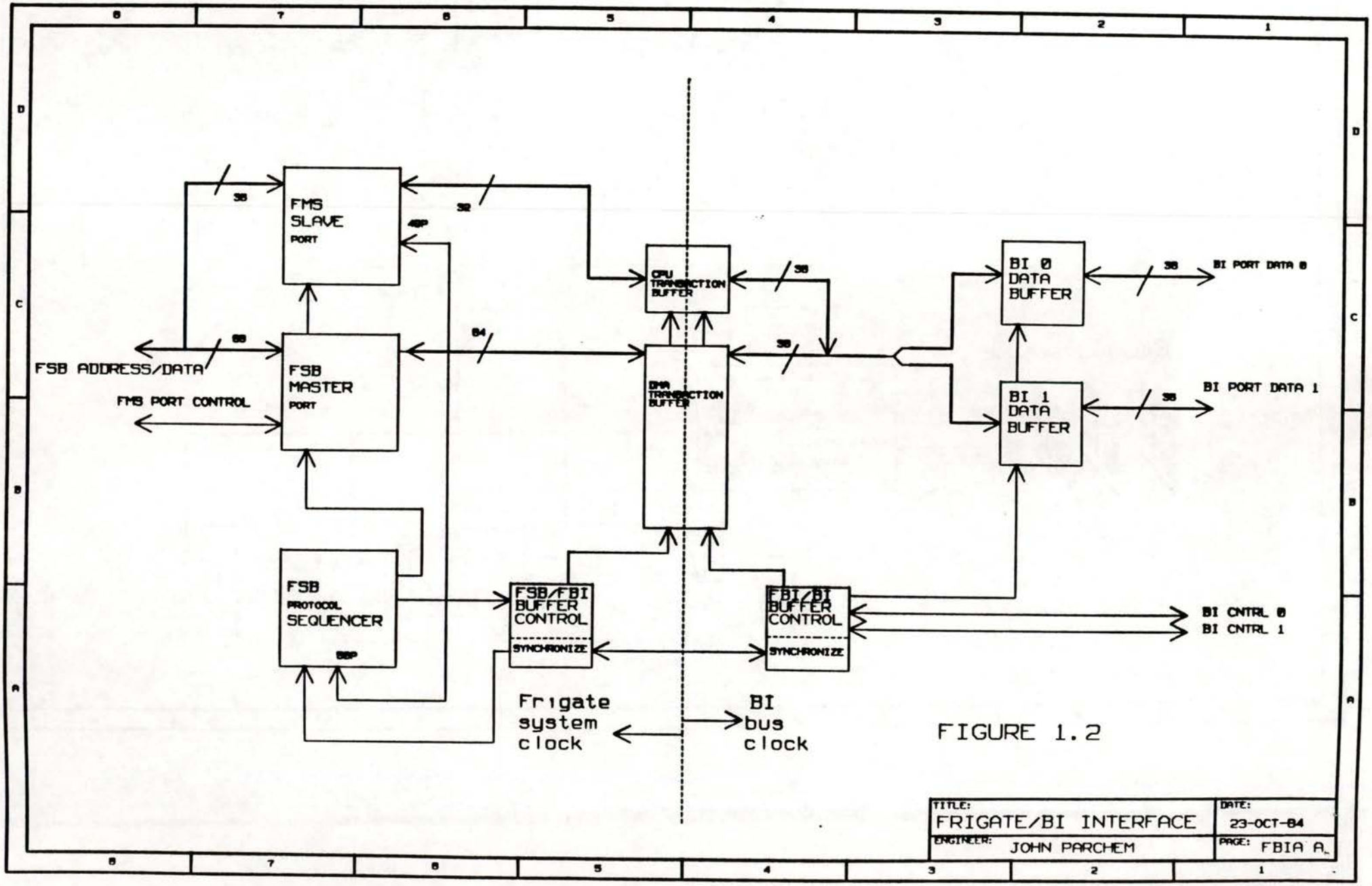

FMS SLAVE PORT
36
32
48P
CPU TRANSACTION BUFFER
36
BI 0 DATA BUFFER
36
BI PORT DATA 0
FSB ADDRESS/DATA
36
FSB MASTER PORT
64
36
DMA TRANSACTION BUFFER
BI 1 DATA BUFFER
36
BI PORT DATA 1
FMS PORT CONTROL
FSB PROTOCOL SEQUENCER
8BP
FSB/FBI BUFFER CONTROL
SYNCHRONIZE
FBI/BI BUFFER CONTROL
SYNCHRONIZE
BI CNTRL 0
BI CNTRL 1
Frigate system clock
BI bus clock
TITLE:
FRIGATE/BI INTERFACE
DATE:
23-OCT-84
ENGINEER:
JOHN PARCHEM
PAGE:
FBIA A

FIGURE 1.2

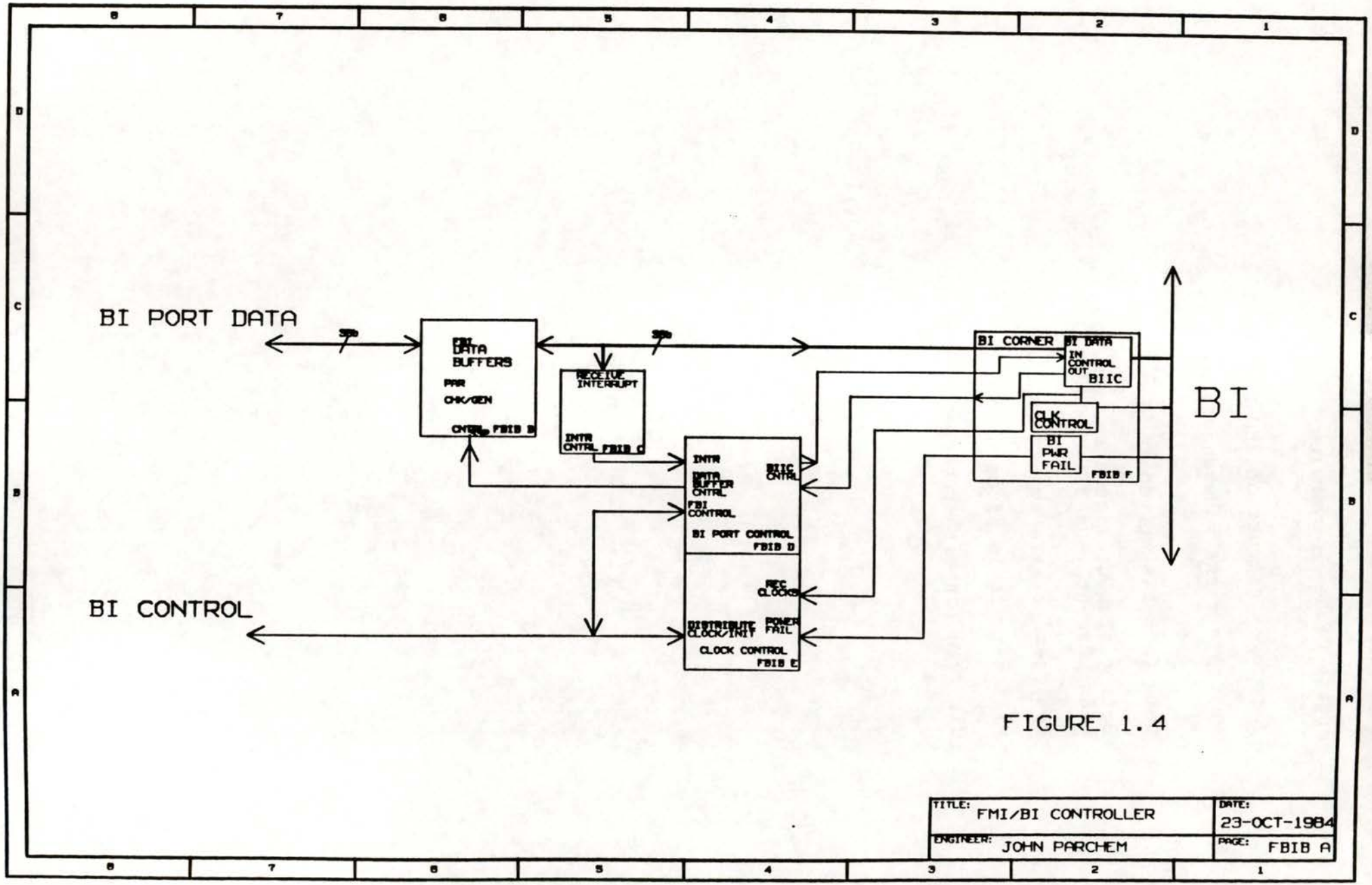

BI PORT DATA
BI CONTROL
BI
32b
32b
FBI DATA BUFFERS
PAR
CHK/GEN
CNTRL FBIB B
RECEIVE INTERRUPT
INTR CNTRL FBIB C
INTR
DATA BUFFER CNTRL
FBI CONTROL
BI PORT CONTROL
FBIB D
BIIC CNTRL
REC CLOCKS
DISTRIBUTE CLOCK/INIT
POWER FAIL
CLOCK CONTROL
FBIB E
BI CORNER
BI DATA IN
CONTROL OUT
BIIC
CLK CONTROL
BI PWR FAIL
FBIB F
TITLE: FMI/BI CONTROLLER
DATE: 23-OCT-1984
ENGINEER: JOHN PARCHEM
PAGE: FBIB A

FIGURE 1.4

Frigate Caches - Overview

- Separate Instruction and Data Caches
- Multiple cache coherency scheme is SRC's Firefly strategy
- Data Cache is Writeback
- Both caches utilize a custom fully-associative Least-Recently-Used cache building-block chip
- Replacement strategy is true LRU
- Fill size is 16 bytes
- Hit rate for either cache is greater than 96%

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April 30, 1985

Cache Modeling Effort

- Simulation driven by actual VAX instruction traces (utility program obtained from VAX Architecture Group)
- Different organizations studied:
    - Fully associative, Least Recently Used (LRU)
    - Fully Associative, Random Replacement
    - Direct Mapped
    - Set Associative
- Write Through vs. Writeback cache scheme
- Hit rate vs. organization, cache size, fill size
- Impact of fill size on bus demand
- Statistics such as
    - reads / instruction
    - writes / instruction
    - per cent reads to same page
    - detailed writeback statistics

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```
**** * Separate I and D cache performance model w/unaligned data * ****

Trace file = epasmm.trc

D cache is  writeback
I cache line width =  8
I cache fill size  =  2
D cache line width =  8
D cache fill size  =  2

total number of instructions    =   455912
total number of references      =  1852586
total number of reads           =   547371
total number of I-stream reads  =   311819
total number of data reads      =   235552
% of data reads previous page   =       45
total number of writes          =   118942
total number,  read/mod/writes  =        0
total number, other operations  =    13519

Cache Size in bytes
  I cache          1024      2048      4096      8192     16384     32768     65536
  d cache          1024      2048      4096      8192     16384     32768     65536
-------------------------------------------------------------------------------------
  L R U  - tot     90.6      94.6      96.3      96.8      96.9      96.9      96.9
  L R U  - I       89.6      94.7      96.5      97.1      97.2      97.2      97.2
  L R U  - D       91.9      94.6      96.0      96.3      96.4      96.4      96.4
memory writes =   17299     11736      7602      3997      1279       307         0
"extra reads" =    6962      4922      3971      3475      3430      3427      3423
unwritten mods=     854      1910      4060      6801      9448     10416     10718

  F A R  - tot     89.5      93.5      95.4      96.2      96.6      96.7      96.8
  F A R  - I       89.3      93.8      95.8      96.7      97.0      97.1      97.2
  F A R  - D       89.8      93.2      95.0      95.7      96.0      96.2      96.3
memory writes =   23101     15609     10349      6687      3987      2305      1249
"extra reads" =    9019      6298      4780      4077      3726      3603      3531
unwritten mods=     766      1669      3372      5470      7407      8752      9648

D Mapped - tot    85.7      90.9      93.7      95.5      96.2      96.6      96.8
D Mapped - I      85.4      91.1      93.8      96.0      96.8      97.0      97.1
D Mapped - D      86.3      90.6      93.6      94.9      95.4      96.1      96.3
Memory writes =   28421     18451     11887      7432      5222      2158       939
"extra reads" =   12734      7989      6154      5101      4710      4080      3924
unwritten mods=     837      1823      3627      5800      7332      9173     10035

 2 assoc - tot    88.4      92.9      95.3      96.3      96.7      96.8      96.9
 2 assoc - I      88.4      93.2      95.6      96.7      97.1      97.2      97.2
 2 assoc - D      88.4      92.5      94.9      95.8      96.3      96.3      96.4
Memory writes =   24444     15992      9867      5716      2558      1124       141
"extra reads" =   10343      6685      4801      4041      3681      3633      3559
unwritten mods=     836      1790      3608      6034      8427      9777     10602

 BUTTS       job terminated at  4-JAN-1985 00:55:36.21

 Accounting information:
 Buffered I/O count:              63      Peak working set size:  2000
 Direct I/O count:             19019      Peak page file size:    2713
 Page faults:                 881009      Mounted volumes:           0
 Elapsed CPU time:      0 02:37:20.81     Elapsed time:     0 07:46:59.63
```

Separate Instruction and Data Caches

- Both caches are composed of:
    - 128 entry LRU translation buffer (single Frigate cache chip)
    - 4Kb LRU cache organized as 512 entries of 64 bits each (8 Frigate cache chips)
    - TB and cache are accessed simultaneously; cache access is made on last page accessed. If translated page address <> last page, second access is made.
- Twice the read bandwidth; allows an independent instruction and data cache access each processor cycle
- Twin 4Kb caches performance on par with single 8Kb cache
    - twin cache effective hit rate = 96.3%
    - single 8Kb hit rate = 96.5%

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WRITEBACK vs. WRITETHROUGH CACHE -- BUS DEMAND IMPACT

1) data taken from cachesim result MIST::[butts.ff]aepasmm.log

2) Simulation interval = 400 nsec / instruction * 455,912 instructions
= 0.182 sec

WRITE-THROUGH ANALYSIS

Instruction Reads:	311,819 * (1 - 0.965) * 16	=	175K byt
Data Reads:	235,552 * (1 - 0.960) * 16	=	151K
Data Writes:	118,942 * (1) * 8	=	952K

Total bus traffic for simulation interval		=	1.28M by

Average Bus Demand -- Write-through cache

= 1.28M bytes / 0.182 seconds = 7.03M bytes /
****

WRITEBACK CACHE ANALYSIS

Instruction Reads:	311,819 * (1 - 0.965) * 16	=	175K byt
Data Reads:	235,552 * (1 - 0.960) * 16	=	151K
Data Writes:	7602 * 8 + 3971 * 16 + 4060 * 8	=	157K

Total bus traffic for simulation interval		=	0.483M b

Average Bus Demand -- Writeback cache

= 0.483M bytes / 0.182 seconds = 2.65M bytes /
****

RESULT:

2.65M bytes / sec

7.03M bytes /sec = 38% of bus demand while providin
enhanced memory subsystem perfor

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Cache Coherency Scheme

- SRC's Firefly scheme
- Two additional status bits for each cache line
    - MODIFIED bit indicates that local copy has been modified; only a single modified copy exists at a time
    - SHARED bit indicates that other copies may exist is other system caches and modifications must be broadcast
- FSB supports 'read with cache intent' function; on read miss, if copy is contained in any system cache, the first one to respond asserts SHARED on FSB and supplies the data. Both receiving and all hitting caches set SHARED.
- modifications of SHARED data are broadcast to all system caches; all responding caches are updated, the local MODIFIED bit is set, and all remote MODIFIED bits are cleared
- write misses cause 'read with cache intent', followed by appropriate write action
- cache with MODIFIED copy must write entry to memory when displaced

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Cache Performance, Power and Board Space Summary for Three Schemes

Cache	I-stream Read	Data Read/Write	Bus Demand	Packages	Board Space	Power
4Kb FALRU	114.0 nsec	127 nsec	2.63 Mb / sec	32	30.9 sq.in.	20.1 watts
32Kb direct map	112.0	126	2.47	122	55.8	41.5
16Kb 2-way SA	111.6	125	2.36	224	98.4	70.4

[from cache performance summary -- 12/05/84, mist::[butts.deceast]cp.rno]

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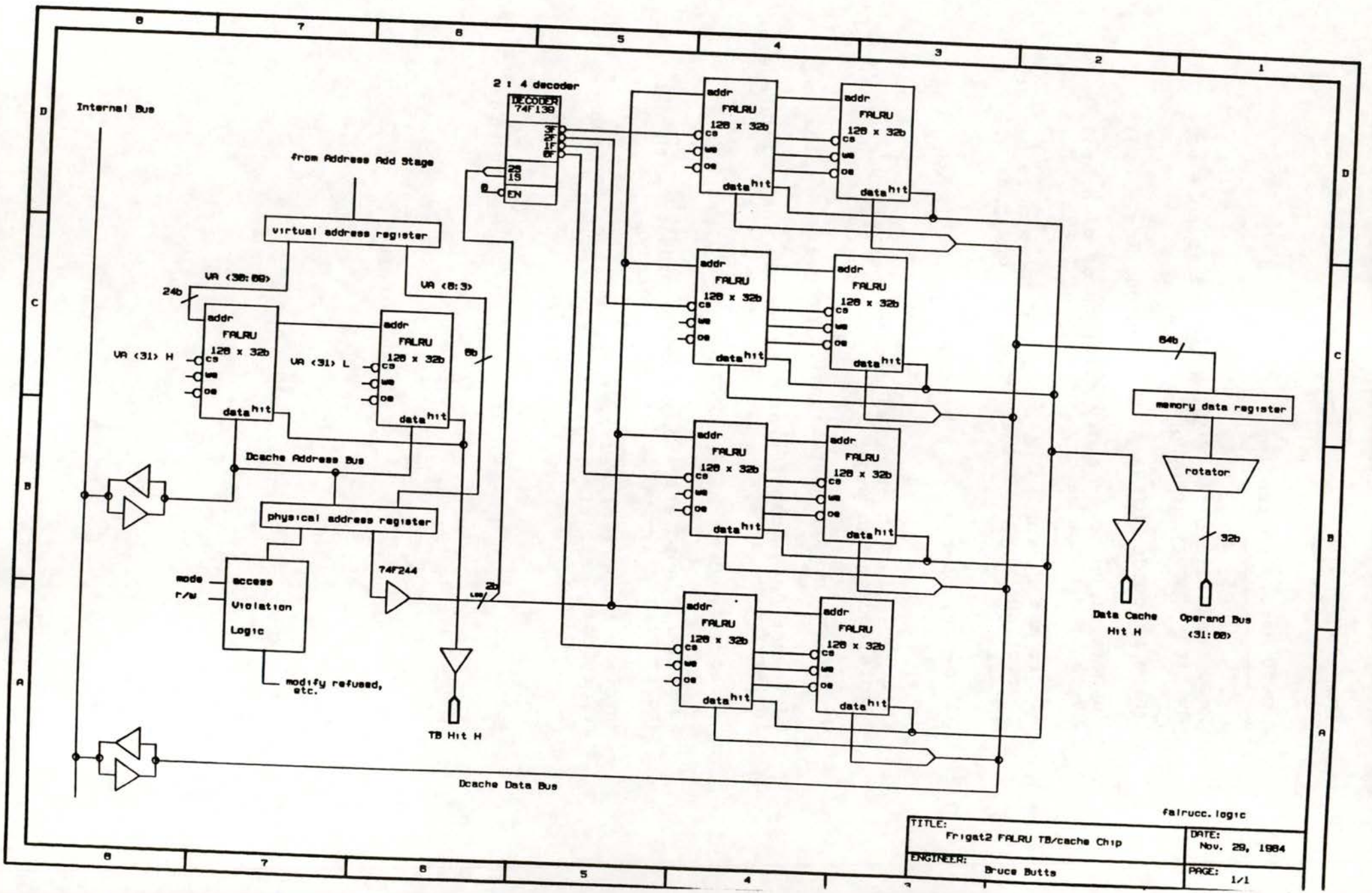
2 : 4 decoder
DECODER 74F139
Internal Bus
from Address Add Stage
virtual address register
VA <30:00>
VA <8:3>
24b
VA <31> H
VA <31> L
addr
FALRU
128 x 32b
cs
we
oe
data hit
8b
Dcache Address Bus
physical address register
74F244
mode
r/w
access
Violation
Logic
modify refused, etc.
TB Hit H
Dcache Data Bus
84b
memory data register
rotator
32b
Data Cache Hit H
Operand Bus <31:00>
falrucc.logic
TITLE: Frigat2 FALRU TB/cache Chip
DATE: Nov. 29, 1984
ENGINEER: Bruce Butts
PAGE: 1/1

Frigate Memory Controller

- Read bandwidth of 46 / 51 Mb/second (single vs. multiple memory array operations)
- Write bandwidth of 38 / 46 Mb/second (as above)
- Support of up to 8 memory array cards of 8 or 32 Mb each; maximum memory capacity of 256Mb
- 64 bit memory word plus 8 bit ECC for single bit error correction, double bit error detection, plus all 0's and all 1's detection
- All memory operations are single or double word reads or writes
- Interlocks for interlocked memory operations are maintained on 8Mb pages
- One or two memory operations in progress simultaneously
- Handshake data transfer of data -- can take advantage of faster future arrays
- Hidden refresh of memory arrays
- Support for automatic memory configuration with mix and/or partially-populated memory arrays
- Hardware support of memory test functions for reduced memory diagnosis times

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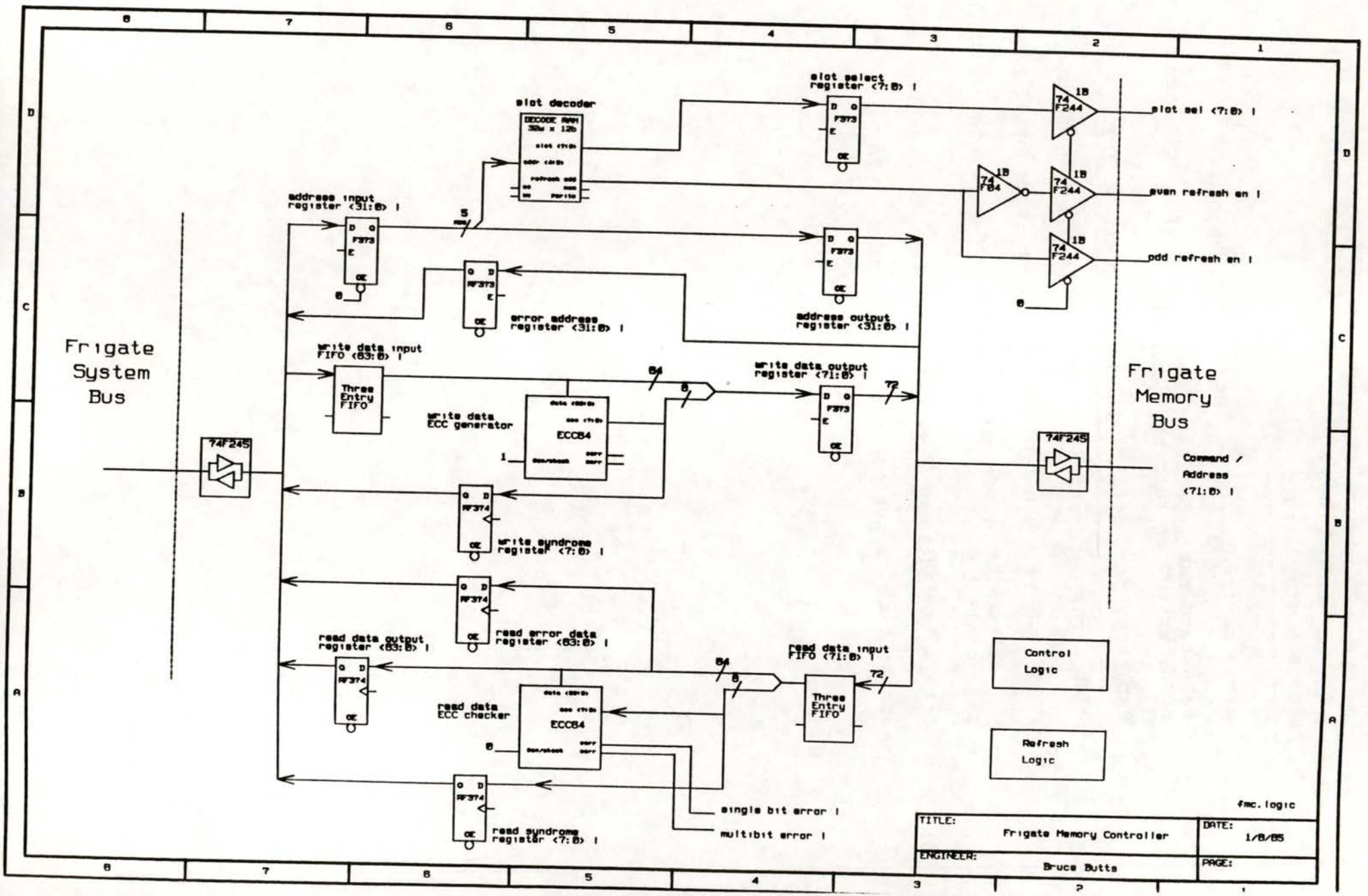
slot decoder
slot select register <7:0>
slot sel <7:0>
even refresh en
odd refresh en
address input register <31:0>
error address register <31:0>
address output register <31:0>
Frigate System Bus
Frigate Memory Bus
write data input FIFO <63:0>
Three Entry FIFO
write data ECC generator
ECC84
write data output register <71:0>
74F245
Command / Address <71:0>
write syndrome register <7:0>
read error data register <63:0>
read data output register <63:0>
read data input FIFO <71:0>
read data ECC checker
read syndrome register <7:0>
single bit error
multibit error
Control Logic
Refresh Logic
fmc.logic
TITLE: Frigate Memory Controller
DATE: 1/8/85
ENGINEER: Bruce Butts
PAGE:

Frigate Memory Arrays

- array cards are 'dumb' inexpensive design
- each card has separate timing logic for simultaneous read, write, or refresh operation
- 8Mb array card utilizing 256K bit DRAMs at FRS
- 32Mb array card utilizing 1M bit DRAMs 6 months later
- organized as 4 banks of DRAMs, each n words by 72 bits
- one or two banks accessed simultaneously to achieve fill size of 16 bytes
- arrays handshake on read data transfers to signal data ready
- access time is currently 6 70 ns cycles - 420 ns

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Fully Associative
Least Recently Used
Cache Chip

Features:

--128 entries, each of;
- -32 data bits
- -30 tag bits
- -2 direct clear status bits - valid and write-in-progress (WIP)
- - 2 status bits - shared and modified

-Support for writeback cache operation

-Fully associative

-True LRU

-Cascadeable in both width and depth

-Suitable for both translation buffer and cache designs

Design implemented as a generator so that modifications/improvements are simplified

TB/Cache Chip
Theory of Operation

Search Cycle

if address already present in tag array then

address has charged-up the address array lines

data-out lines are charged-up as result of hit

both data and address are re-circulated to front of FIFO

all tags/data from front of FIFO to location of hit are shifted one position

else

address and data are entered at front of respective queues

Tag/data shifted off the end of paired queues are lost.

Single line reset on valid bit column invalidates all entries.

All other columns are identical.

TB/Cache Chip
Timing

Derived from SPICE simulations

-- layouts produced by MEGAN
-- layouts extracted by IV
-- SS and TT CMOS 1 models used

Input Pads

-- furnished "as-is" by Parker's group Hudson
-- TT = 3-4 ns

Address Lines

-- 2 ns

Hit Lines

--Alternate low and high assertions
--4-5 ns worst case

Data Lines

--4 ns

Output Pads

--Obtained from Hudson
--Redesigned with P-channel pullups
--Increases CVf^2 power
--8 ns worst case
--5 ns typical

Total Search Time

--23 ns worst case
--"end-to-end" timing
--array logic, therefore rolling wave control via self-timed logic

Self-timed Logic

--probable ~18 ns (perhaps less)

TB/Cache Chip
Basic Storage Cell Design

Single Clock (CLK and CLKB)

Three Clocked Inverters

Totally Static -- Clock Activated only for Shift

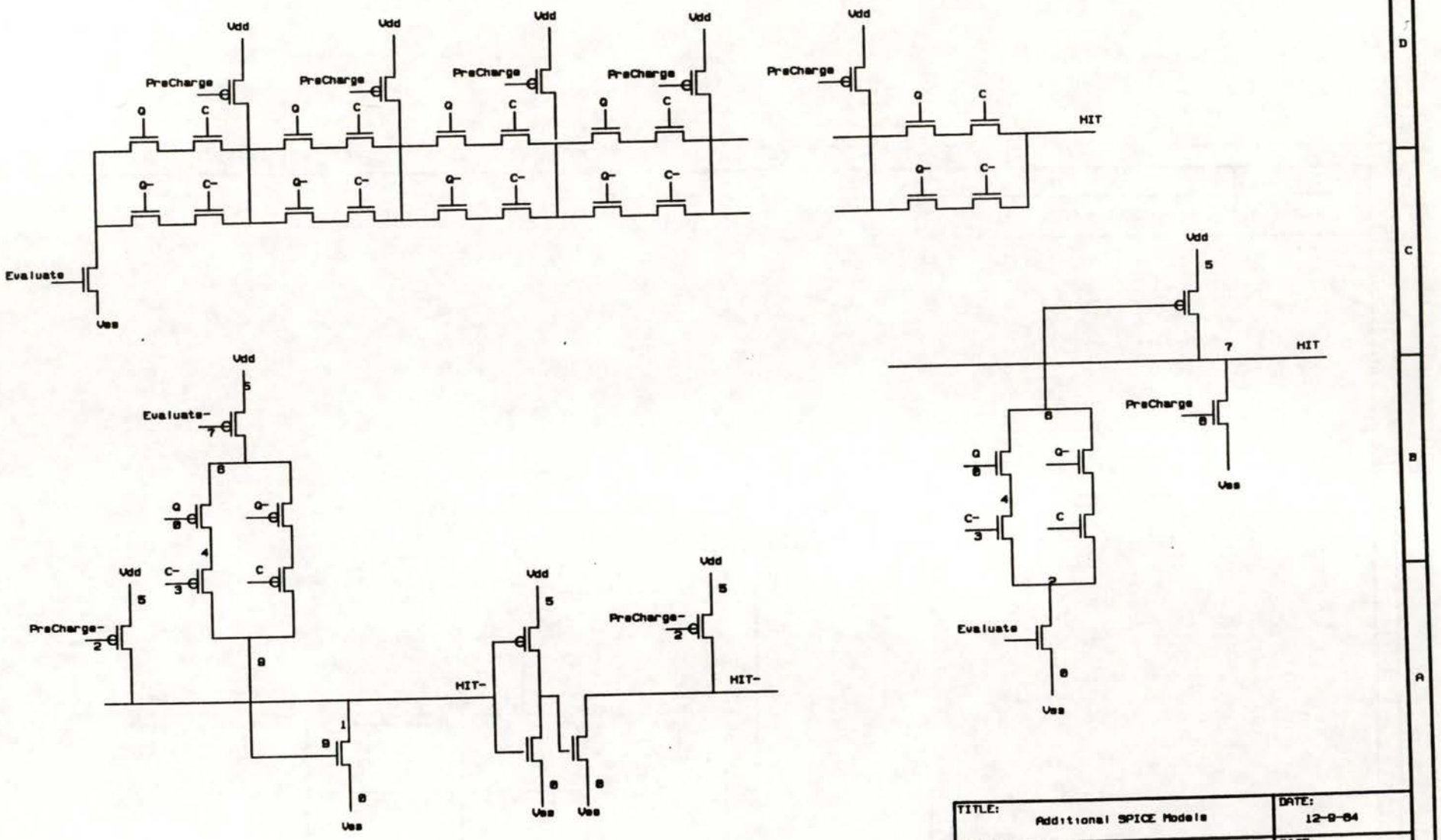
Overdrive of Q-output on Q'-output

Slight, but tolerable, increase in power consumption

Cell size 55 x 54 microns

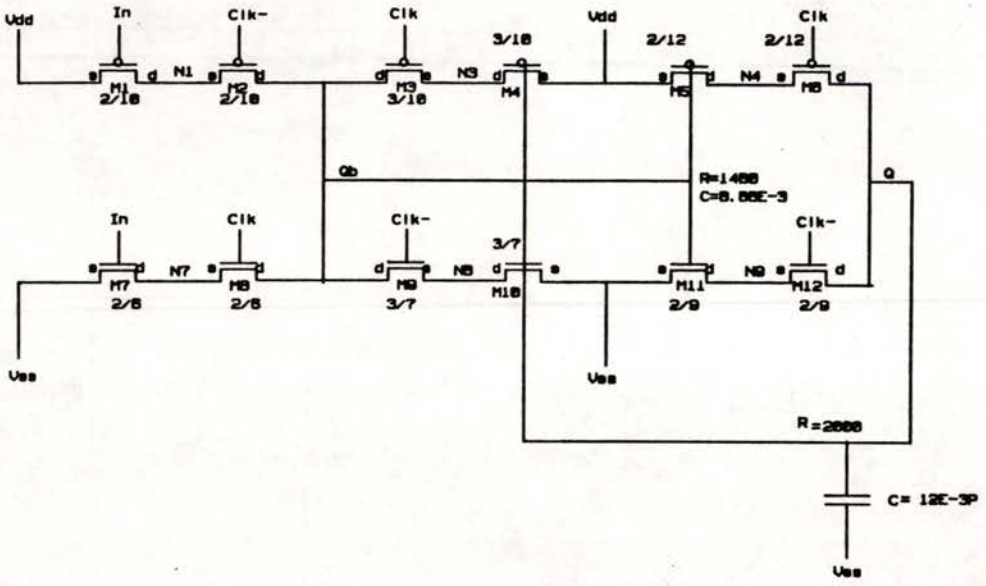
Additional pulldown logic for data array increases cell size to 55 x 76 microns

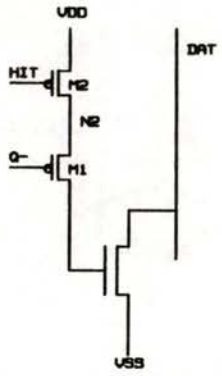
Total array size 280 x 230 mils, excluding pads
-- easy to manufacture



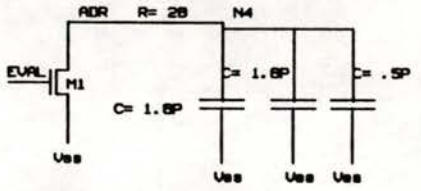
TITLE: Additional SPICE Models	DATE: 12-9-84
ENGINEER: Ted Kehl	PAGE:

STORAGE CELL SHIFT TIMING





PULLING DOWN THE ADDRESS LINE



TITLE: TLB Spice Model	DATE: 11-27-84
ENGINEER: Ted Kehl	PAGE:

HARDBACK BOOK-
CONTENTS NOT
SCANNED

Frigate Field Service Impact Statement

DIGITAL EQUIPMENT CORPORATION

HARDBACK BOOK-
CONTENTS NOT
SCANNED

Frigate Manufacturing Impact Statement

digital
DIGITAL EQUIPMENT CORPORATION