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FOREFRONT

T. Litt

VAX VMS Systems and Servers

Systems for the '90s

Q1 FY92

Opportunity in the USSR

Jesse Lipcon Reports on His Trip to the USSR

This Digital Employee, American Hero & Explorer, Comments on VAX Computers in Space

FOREFRONT

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FOREFRONT strives to support a forum for the entire VSS WW community to share information, directions and key accomplishments in all its functional dimensions i.e., Customers, Markets, Engineering and Manufacturing. The goal is to highlight technical efforts and successes that lead to new products and markets for DEC.

This is your information forum. Your participation is vital to its continuation and success. You are encouraged to contribute articles which are of interest to the VSS community. FOREFRONT is a quarterly publication. We are now accepting articles for the next edition; the deadline is August 15th.

If you wish additional copies of FOREFRONT or know of someone who wants to be added to the mailing list, please provide us with their name, location, and badge number. Forward this inforation or any comments to VSNEWS::WILLETT.

Contents

Danger and Opportunity in the Soviet Union

Dick Willett
Jay McManus

"It was our intention to combine this article with some recent information from Jesse Lipcon's most recent trip to the Soviet Union. Unfortunately, time constraints and Jesse's busy schedule prevented us from interviewing him. In a future edition, we hope to provide you with an update."

In Chinese, the character for the word "Crisis" is made up of two different symbols, one representing "Danger" and the other "Opportunity." The symbolism points to the forces at play in the Soviet Union, where the energies of Russian perestroika meet the Western push for new technological markets.

Last November, two Digital teams headed by ESB Group Manager Jesse Lipcon visited several computer manufacturers in the Soviet Union. The opportunity? The Soviets have illegally cloned VAX and PDP-11 hardware, providing Digital with three natural advantages: market share in technical/manufacturing applications, wide appreciation of Digital architecture and software, and a broad base of knowledgeable users. The danger? Digital will wait until it has mapped out a completely refined strategy. And, in six months, the opportunity may disappear.

Many surprises awaited Jesse and his team. Expecting to find party hacks, incompetence, and laziness ("We pretend to work, they pretend to pay us"), they discovered responsible managers, an educated workforce, and a strong work ethic — the foundation for potential Digital partnerships. Modern business and marketing skills, on the other hand, are almost completely absent. There is little or no understanding of pricing, supply and demand, inventory control, or just-in-time manufacturing. Consistent quality is elusive.

Still, the team saw enough to draw some interesting conclusions. Mainframe "dinosaurs" still live in the West because of the large commercial applications that traditionally feed them. So it is in the Soviet Union: applications serving the old Communist system run on cloned IBM mainframes. In the new market economy, however, those applications will be replaced. The slate will be wiped clean. And the Soviet Union could become the ultimate two-tier computing model: intelligent PCs and a distributed network of VAX/VMS servers.

"We have the opportunity to achieve dominance," Jesse says. "Look at our superior CASE environment, our networking and price/performance – the 'go anywhere' nature of our machines. Then consider the pool of VAX/VMS knowledge in the USSR, the natural market share, and the potential. By some estimates, there is enough demand there to double our annual shipments of MicroVAXs. But we must move boldly to exploit these advantages. The window is closing very quickly."

Module inspection area.

State of the Computer Art in USSR

The two Digital teams visited four facilities in the Soviet Union. Capabilities, in general, appeared five to six years behind state-of-the-art in the West and Japan.

Whether the developments are on slower-moving technologies such as printed circuit boards and metals fabrication, or disks and semiconductor components, the lag time seems consistent. The team found "reasonable" manufacturing capability in printed circuit boards, plastics, and metals fabrication.

Let's take a closer look at one of the companies. Founded in 1966, Sigma is located in Vilnius, Lithuania and employs 17,000 in three different facilities. Primary products are computers, graphics workstations, hard disk drives, instrumentation, electric meters, and photocopiers. Sigma makes extensive use of CAD in PC board layout, mechanical part design, and tool design.

The hard disk, an RK06-type drive, is produced at an annual rate of 6000 units. A clone of the Digital PDP-11, now scheduled for phase-out, it has an installed base of more than 3000 units. In 1990, Sigma planned to produce 910 units of an 11/730 clone, dubbed the CM-1700, but by the end of the calendar year had shipped only 100. Moscow Central Administration had stopped providing the "customers" to whom Sigma could ship the product. A MicroVAX II clone, now in final design stages, awaits a supply of chips from another facility.

More than 5,000 are employed at the Vilnius facility – one-fifth working in the central design group at the Research Institute as computer systems engineers, system programmers, and application programmers.

At the Kaunus facility, the team saw pilot production of 20-inch color monitors. Annual planned output is only 50 units. The team's verdict: poor quality, and even poorer workmanship.

Printed circuit board manufacture, assembly and test is carried out at the Sigma facility in Taurage, near the coast of the Baltic Sea. Refurbished in 1985 with Western capital investment, the plant appeared tightly controlled and well maintained – comparable to typical Western board shops. Assembly and test capability, however, was less impressive: little automatic insertion, lots of hand assembly and touchup, and large stocks of inventory. Manufacturing cycle time: 6 weeks from bare etch to finished module. Of the 34,000 modules produced annually, 30% is ticketed for non-Sigma customers in Lithuania and Poland. Sigma has also entered a joint venture with Intermico, an Austrian computer vendor, to produce a special-purpose PC for automated banking systems.

For 1990, Sigma had planned output totaling greater than 200 million rubles – including 40 million in consumer goods and other miscellaneous categories. After the economic shockwaves of the past year, however, the projection was revised to less that 150 million.

Despite the uncertainty in the USSR, the Digital team noted three strengths at Sigma:

- Strong base of technical skill — plus knowledge of VMS, networking, and applications programming. These assets would be critical if Digital decided to enter into a CSO-type partnership with Sigma.
- Installed base of VAX clones, and technical knowledge of VAX systems. This would be an advantage if the company were to become a Digital distributor.
- Printed circuit board manufacturing capability. This provides Digital an immediate doorway to a business relationship. It would also arm Sigma with hard currency to fund purchase of key Western materials.

Total Vertical Integration

Because no market economy has existed since the Russian Revolution, Jesse notes, there is no rationalized production – the kind that encourages a network of specialized and efficient suppliers. And because none of the manufacturers can count on quality supplies, companies are integrated vertically. The computer makers build their own PC boards, modules, plastics, and metals. With the excess capacity, the facilities produce items ranging from pens and toy airplanes to fishing equipment and slot machines. Electronmash, a facility in Kiev, even owns an oxen farm to supply the company cafeteria with meat and dairy products.

Send in the Clones

In the USSR, computer cloning is an art form. It began at Electronmash, a computer company located in Kiev, Russia. Electronmash started with copies of the IBM 360, then added a copy of the Hewlett-Packard M6000. Finally, in the late 70s, another change in direction: clones of the PDP-11. A copy of the PDP-11/34, before it is phased out this year, will have shipped more than 20,000 units since 1983. At Sigma, the Soviets have been zealously cloning, chip for chip and bit for bit, the PDP-11/730 – which they have renamed the CM-1700. And the CM-1702, based on the MicroVAX II. It is ironic, Jesse notes, that Digital stopped production of the 11/730 in 1987 after building 13,000 units. The soul of the machine lives on, however, in the 3,000 units of the CM-1700 the Soviets have shipped since that date.

How do the cloners do it? The team's hosts freely volunteered the strategy: the KGB purchases MicroVAXs through a front operation in the Far East, then ships them back to Electronica – a company located in Veronezh, Russia. There, the chip sets are subjected to a kind of primitive reverse engineering: each layer is photographed, then shaved off to reveal the next layer, which is photographed, and so on.

The Opportunity Beckons

Despite the shortcomings in the USSR, including a crumbling infrastructure, the team found ample reason for optimism – and a role for Digital amidst perestroika. But Jesse cautions that time is critical for four major reasons:

- An Influx of PCs from the Pacific Rim – "The VAX 11-730 clone is winding down production", Jesse says, "and it's not hard to see why. Who is going to buy a 730 for 200,000 rubles, when you can purchase a PC with 10 times the performance for 60,000 rubles?"
- The Lengthening Shadow of UNIX – "VMS dominates the cloned VAX base and technical computing to the same extent it did on our VAX systems in the mid 80s. With PCs arriving, however, UNIX is not far behind. And Sun Microsystems is rumored to be making a major push."
- Slipping Market Share – "The cloners have typically trailed Digital by five years. This gap is now widening, because the VLSI CPU supplier in Voronezh has failed to clone the original MicroVAX II chip set. There is serious doubt they'll ever be able to. Meanwhile, we're losing market share as obsolete 11/730 clones fall to PCs."
- New Generation of Applications – "In the transition from a Communist system to a market economy, all the old applications – those that ran on IBM mainframe clones – will have to be thrown out. We've got an opportunity to create the ultimate two-tier computing environment: Intelligent PCs backed up by a 'distributed mainframe' network of VAX/VMS servers."

A Call to Action

Tentative steps in the USSR towards restructuring the economy have stripped the old Communist apparatus, but left little in its place. Until early last year, for example, Sigma depended entirely on Moscow for its product strategy, production plan, sales and order administration. Now, the company must be more independent, succeeding or failing on its own merits. Seventeen managers from the Vilnius facility have been scattered throughout the USSR as "salesmen," who then established 100 "dealers." But since the dealers receive only a 3% to 5% commission, there is little incentive to sell product. Assuming, of course, that anyone really understood sales and marketing.

For the immediate future, the outlook is not good. Output in the overall Soviet electronics industry, according to state forecasts, will drop 41% over the next two years.

Amidst the chaos and uncertainty, however, the Digital team sees opportunity. Jesse made a number of key recommendations:

- Do not, at least initially, plan on assembling systems in the Soviet Union. There is simply not enough added value to justify the effort.
- Explore possibilities to take on Sigma and Electronmash as qualified suppliers for low-level components in areas of slow-moving technology.

Jesse Lipcon inputing data into a Soviet MicroVAX II clone (CM1702).

Digital team (from left to right); Jenny Holmes, Interpretator from Argus Trading Limited; Joe Cannizzaro, VIPS; Bob Allely, DEC Mfg., Ayr, Scotland; Jesse Lipcon, ESB; Bob Krause, DEC International Trade Office.

- Examine the avenue of barter to generate hard currency, which can then be used to purchase Digital equipment.
- Launch an aggressive effort to locate Soviet software partners – and match them with needed projects. The typical Soviet software engineer earns an annual salary of 5000 rubles, less than 1% of his Western counterpart's salary at realistic exchange rates. Even with the much lower levels of productivity, software value could be created which would be "unaffordable" at Western salary scales. In addition, this scheme would absorb rubles, allowing market penetration without the need for hard currency.
- To jump start the sales and marketing engine, sign up the cloners as CSO distributors. Sigma, for example, offers a solid base of skills – in addition to knowledge of VMS, networking, and applications programming.

The energy in these recommendations, Jesse says, comes from a sense of urgency. Time is critical. Of course, the situation is complex. We're going to take some false steps, and we're going to make mistakes. But let's be bold. Let's start doing."

Speaking of Politics

In order to speak to their counterparts at Sigma in Vilnius, the Digital team brought two translators. The Russian language, although spoken throughout the Soviet Union, proved an obstacle because Lithuanians, like their comrades in many other of the republics, have rediscovered nationalism. But Lithuanian, a derivative of Latin, refused to yield to many technical terms.

"One of our translators was a woman from Argus Trading," Jesse recalls, "a firm with offices in London and Moscow. At first, she translated the word "impedance" as "impotence" – so no one could understand what we were talking about.

"Finally, Joe Cannizzaro and I dashed to the blackboard. We madly scribbled equations, drew pictures of transmission lines, and they eventually figured it out."

Perestroika and Pointing Fingers

At Vilnius, Sigma officials lament the poor-quality laminates sent from a factory in Moldavia, one of the more independent Soviet republics. In one area, a Turkish majority is trying to secede from Moldavia itself, adding to the general chaos.

"The folks at Vilnius told us that the terrible laminates they receive make it impossible to manufacture controlled-impedance printed circuit boards," Jesse says. "Not only that, but they can't even discuss the matter with the supplier, because all the Moldavians are interested in is fighting among themselves.

"Well, I asked, do you ever analyze the failures from the field? No, they replied, it never occurred to them. So then I asked if they sent failed chips back to their vendors for analysis. Again, the answer was no. Why not, I asked? They told me the vendors wouldn't take the chips back, nor reimburse for them, because the vendors aren't interested in quality. Why should they – they've got a monopoly!"

A Brief Overview of the Alpha Program

Harriet Cohen

The Alpha Program mission is to:

Be recognized as the worldwide standard for meeting customer needs using next generation computer system, service, application, and business technologies.

Achieving the program mission will:

- Provide our current customers with superior systems, software, services, and solutions for growing their businesses and protecting their current investments in computing, enabling Digital to protect its installed base, and
- Provide new customers with leading edge systems software, services, and solutions, enabling Digital to penetrate new markets and expand its installed base.

The mission will be achieved by providing the VMS environment on a complete range of hardware platforms built on a new Digital-developed architecture. These hardware platforms will be among the leaders in the industry in both absolute performance and cost/performance in each price band throughout the 1990's and into the 21st century.

The architecture for these hardware platforms incorporates essential features of the VAX privileged architecture with a superscalar (i.e., multiple instruction issue) RISC instruction set architecture. This approach shortens the time required to develop the VMS environment on a RISC architecture while providing the architectural constructs necessary for leadership performance.

The Alpha Program mission is to:

Be recognized as the worldwide standard for meeting customer needs using next generation computer system, service, application, and business technologies.

The availability of VMS on RISC both preserves customer investment and ensures that third party application developers and customers can move quickly to the Alpha platform.

Third party developers will have access to Alpha systems in less than one year. This will allow them to begin verification of their applications.

Digital Internal Use Only

The major components of the Alpha Program are:

A. Alpha Architecture. A new, Digital-developed RISC architecture which provides compatibility with current VAX systems, as well as essential features necessary for product leadership in the 1990's.

The Alpha architecture will include both a processor architecture and an I/O architecture to ensure that balanced system performance is achieved.

B. Alpha Systems. A family of Alpha platforms which covers the range of computing needs, from notebook to data center.

C. The VMS environment on Alpha. VMS and the full complement of layered products will be delivered on Alpha over time.

D. Third Party Software. Third party applications are essential to the success of the Alpha Program. Programs are being developed to ensure that key third party applications are available for Alpha at the time that volume revenue shipments begin.

E. Compatibility between VAXes and Alpha. The compatibility between VAXes and Alpha systems provides maximum investment protection (e.g., in source code, images, data, and training) for current VAX customers. The goal is to have a transition that is as smooth or smoother than the transition from VMS V4.7 to VMS V5.0.

F. Reliability and Quality. The software, hardware, documentation, training, and services will be of high quality and reliability. Careful attention will be paid throughout the development and delivery process to creating robust and high quality products and services.

We will continue to keep you informed of our progress in upcoming issues of *FOREFRONT.*

VAX 4000 Wins Award

Karen Quatromoni, P. R. Representative

VAX 4000 Model 300 Wins Digital Review Target Award

Digital's VAX 4000 Model 300 won Digital Review's prestigious Target Award for the Best Computer System/Multiuser. In addition, the VAXserver 4000 Model 300 won the Best Computer System/Server!

Accepting the awards for Digital was Lucien Philippon, Entry VAX Product Manager. The ceremony was held at DECUS in Las Vegas this past fall.

An excerpt from Digital Review's awards story reads, "...The VAX 4000 Model 300 represents a leap in the VAX price/performance ratio and brings VAX computing to an unprecedented level.

...the new VAX 4000 is more than an impressive follow-on to the MicroVAX line. The new system has been built from the ground up to function as a server."

Digital Review is an independent third-party publication that targets users of Digital products. Digital Review's 84,000-plus readers selected a number of Digital products as winners of the Target Awards. The readers based their preferences on product technological innovation, user-friendliness, and price/performance.

Improving Print Sets in ESB

(A simple application of SIX SIGMA methodology)

Joe McMullin
ESB Operations Manager

ESB's process for creating print sets has improved considerably over the last year with further improvements anticipated in the near future. This short article summarizes how we are applying the SIX SIGMA methodology to achieve these improvements. Additionally, it describes the actual refinements we have achieved in the print sets.

Introduction

In the last issue of *FOREFRONT* Subhash Dandage wrote about ESB's vision of and commitment to SIX SIGMA. We have been applying this methodology to a number of different processes including the development of engineering prints, print sets and K-PL's.

Over the last 20-25 years, the process of developing print sets has drifted away from our customers' needs. We are hearing direct complaints from our customers about these print sets. So we decided to analyze this process using the six steps of SIX SIGMA. (See highlighted box for a list of the six steps.) Here is what we found.

Step 1: What are print sets?

Top level print sets are controlled by a table of contents, called TC drawing. It lists all the prints that make up the print set. This drawing is routinely pre-titled "Field Maintenance Print Set." We asked ourselves simple questions like: "Is this print set really used for Field Maintenance?" "Who actually determines what prints will be included?" "Does what is being included meet today's needs?" "With all the Field Maintenance Manuals we do, do we also need a Field Maintenance Print Set?"

After long discussions about the 'product' we were creating, we truthfully came to the conclusion that it was undoubtedly at a very low sigma level.

Here is a sample of some specifics we uncovered.

1. According to DEC standards there are two types of Field Maintenance Print Sets.

MP print sets....these sets can be, and they are, SOLD to customers. *No Confidential Information Allowed.*

EM print sets....these sets are for internal use only. *They cannot be sold.*

2. Print Sets were being treated as stand-alone DEC products, priced and SOLD to customers, and we had no controlled process for ensuring high quality, accurate and meaningful print sets. This created several kinds of defects (see Step 5).

Step 2: Who are the customers and what do they need?

It was clear, once our "product" was defined, that the two types of print sets had two different customers. For the MP print sets the main customers are external, paying DEC customers. On the other hand, the EM print sets were used primarily by the internal Field Service people.

Both customers require high quality, accurate meaningful print sets. MP sets cannot contain confidential information; EM sets can.

Step 3: Who are the suppliers?

All of the prints in the print sets come directly from released Engineering drawings and other released documents. CSSE is the major supplier of inputs as to what will be included in each print set.

After our analysis, it became evident that there was another existing supply of information that would provide better quality and useful prints sets – the Illustrated Parts Breakdowns (IPB's). However, IPB's were only available in 8 1/2 x 11 format. So, working with the Chief Engineer's office, we created a new print code, IB, for the IPB in "B" size format. Now we could replace all the top level Unit Assembly drawings and K-PL's with the IB drawings.

Step 4: What is the process for creating print sets?

The process for creating print sets wasn't very clear when we got started. There were no clear answers to questions like:

"Who actually determines what prints will be included in the EM? In the MP? Is it Design Engineering, CSSE or is it a combined effort?" "Who determines what is confidential?"

What we did know was that these print sets were being sold as a DEC product and needed to be treated in that manner. The generic process for creating print sets is thus similar to that for developing any other DEC product. The necessary first step is for Engineering and CSSE to define the strategy and requirements for a given print set.

We began to test improvements with the VAX4000-300 and applied what we learned to the VAX4000-200. We are now applying the improved process to the ESB products currently under development.

Step 5: Mistake-proof the process.

The process generates several kinds of defects. For instance,

1. Confidential information can go out to customers.

2. MP print sets are not legible for various reasons:

a. The lettering on some drawings is too small. After several generations of copying, legibility gets sacrificed.

b. There are multiple module rework illustrations on one drawing.

3. Accuracy can leave a lot to be desired. When ECO's get processed, there can be a significant time factor before prints sets get updated.

4. We are including prints that no longer serve any useful purpose as part of Field Maintenance Print Sets.

The following improvements were instituted in creating the ESB portion of the VAX4000-200/300 print sets:

1. Eliminated confidential information from the MP print sets by educating the ESB Design Engineers of the confidentiality issue, and when possible, by structuring the drawings so that confidential prints could easily be left out. Example, Sheets 1 thru 10 non-confidential and Sheets 11 thru 15 confidential.

2. Eliminated the ESB Unit Assembly drawings and the K-PL's from print sets. Replaced them with IB drawings [IPB] which are much easier to read as well as better in quality and usefulness.

3. Eliminated ESB lower level piece part prints and specifications (for example 74 class drawings and purchase specifications) from the print sets.

Step 6: Continuous improvement.

We have not yet developed the metrics that we need to track to ensure continuous improvement. This will be done in the near future. Nonetheless, the process already shows potential for further improvement. As examples, we are now evaluating the possibility of combining the Field Maintenance Manuals and the Field Maintenance Print Sets into one cohesive document.

Future Activities

This was one of ESB's first applications of the SIX SIGMA methodology to an administrative process. We have learned from this experience and we are improving the methodology as we apply it to other processes. The ESB product announcement process, the INTRO systems, Field Test Systems process and the user documentation process have all been analyzed. There are a large number of processes for us to look at in order to make any real difference. This is just a start.

In the next issue of *FOREFRONT* we will share with you another ESB improvement activity.

Six Steps to Six Sigma

Step 1: Define the products you create or the service you provide.

Step 2: Identify the customer(s) for your product or service, and determine what they consider important.

Step 3: Identify what you need from your suppliers to provide products/services that satisfy your customers.

Step 4: Define the process for doing work.

Step 5: Mistake-proof the process and eliminate wasted effort.

Step 6: Ensure continuous improvement by measuring, analyzing, and controlling the improved process.

VSS Progress Towards A Data-Managed Environment

Dave Carlson
I.M. Development Manager

Executive Summary:

As VSS and its Product Creation Units (ESB, DCSS [Data Center Systems and Servers] and VMS) position themselves to meet the intense global competitive challenges posed by pressures on time-to-market and life-cycle profitability, focus will be directed at the importance of data/information management as a key enabler in the cost effect availability and delivery of information for timely decision-making. Quality time and effort will be invested by the "providers" and "consumers" of data/information to build, model and establish the integration of business processes and information technology tools. This will provide the foundation for delivering the enterprise-wide efficiency and effectivity that have been targeted by VSS. Some of the benefits of moving towards a data managed environment and requirements for success in VSS are explored in this article.

In today's highly competitive business environment the importance of managing data as an asset has become a critical success factor for every organization. The need for real time, usable, high quality information is growing as the pressure to contain information management costs continues to mount.

Every enterprise is composed of groups of people whose activities create information that is "supplied" to other groups who, as "consumers" of that information, use it as input into their workstream. Broadly speaking most organizations, departments or workgroups are both "consumers" and "suppliers" of information.

Traditional approaches to providing information to consumers, such as writing report programs in 3GL's (third generation languages), are proving to be ineffective or insufficient in the minds of many consumers due to the pace of change and expense associated with this approach. The explosion of "user-friendly" spreadsheet, query and graphics tools and the advent of "desktop computing" has caused information consumers to raise their demands for data/information. In addition, the development of industry standards for "Openness" are rapidly moving corporations to diversify in their purchase and use of hardware and software into heterogeneous computing environments. This in turn opens up a tremendous new source of data/information as proprietary data structures are no longer an obstacle to information consumers.

Need for a "Data Managed Environment"

To compete globally, corporations, and VSS is no exception, are rapidly discovering that they have a need to integrate their information environments in order to make rational decisions governing virtually every aspect of their business. Unfortunately, many companies are finding that because they have ignored basic data management fundamentals, they are unable to share data in any meaningful or consistent way. Why? Because common data is often defined differently from business to business, department to department and application to application. As such, attempts at integration are abandoned and/or additional overhead is added within the organization to translate, filter, or otherwise "polish" the data to make possible its use between organizations within the enterprise. Working toward a *"Data Managed Environment"* is critical in achieving integration within an organization.

Definition of Data Managed Environment

What is a data managed environment? Basically, it is an environment where data providers and consumers have invested the time in understanding the relationship between their business needs/processes and the creation, storage and use of data/information within the enterprise.

Data-managed environments share several common traits. There is a strong focus on modeling and documenting the business processes and their specific data requirements. Lots of hard work is invested in defining the meaning of the data (data definitions) and in defining business rules to guide information consumers in the consistent use of the data. These environments also employ tools such as data dictionaries to define and manage the data. A well managed data dictionary process is crucial in a data managed environment as it serves as the foundation for identifying and storing the enterprise's data and their definitions. From a human perspective, information/data providers and consumers have a keen awareness of the value and cost of managing the enterprise's data. They are interested in the consistent and cost effective use of the data. In effect they look at data if it were just as valuable as an asset as a building or a production machine on the shop floor.

The Benefits

Although the journey to a data-managed environment can be arduous, the benefits make the effort worthwhile. Amongst the benefits are:

1. Dramatic reductions in redundant creation and management of data. For most companies and for the VSS enterprise, this will result in significantly reduced costs in the form of overhead and other operating resource reductions.

2. Cycle times for application development or data retrievals will be greatly reduced. Many information requests can be handled quickly from a site Information Service Center rather than end up in a long application development queue.

3. Applications/data bases can be easily modified which allows fast turnaround for change requests by information consumers.

4. Organizations will trust and use the data provided because it is modeled and defined properly and will meet the great majority of their analytical/reporting needs.

5. The enterprise can achieve integration of its information systems locally and globally to deliver the performance targets for sustainable competitive requirements, making the fullest use of all its investments in Information Management assets.

In short, Data Managed Environments will be a key enabler to enhancing enterprise-wide efficiencies and effectivity thus enhancing its global *competitiveness.* For VSS this is a strategic necessity and a requirement.

The VSS Commitment to Data Managed Environment

VSS has made significant progress in achieving a data managed environment. All business applications development work now undertaken at the Headquarters Operations in Boxborough, Mass., US, is managed under a development *Methodology* that stresses the data management approach in creating solutions for data consumers.

Before any code is generated, Information Management and their business project partners model their business processes and data to ensure the optimum design for applications or data bases. They take the time to define the data and the business rules governing the use of the data and they use the latest dictionary tools to manage that data. This approach is yielding many advantages to VSS business groups including faster turnaround to build or modify applications and data bases, better understanding of the business processes and eventually will result in lower cost and higher levels of integration as data becomes more shareable and redundancy is reduced.

A major side benefit from the modeling work is also a new orientation of business and Information Management personnel to ask "do I really want to automate this current process or should I think about re-engineering the business process before I apply information technology?" In fact, many of the process and data models produced by VSS personnel are facilitating major change in processes across VSS.

Realignment of IM Resources in VSS

In addition, the orientation towards data management is manifesting itself in the design of IM organizations within *VSS*. In the past, IM organizations were constituted primarily of programmers with little or no data management resources. In many cases today these organizations have rebuilt their IM groups to include a mix of data management personnel (data modelers, data base administrators) and programmers. This in turn has enabled a great deal of collaboration on the part of the various data management communities with VSS and Digital to work together on the job of integrating the data in such critical subject areas as revenue, inventory, orders, personnel, etc.

VSS Data Management Directions and Digital's Data Warehouse Network

The above focus on re-architecting the VSS data management activities will draw synergy from the development of the Digital Data Warehouse Network. Under this concept these "data warehouses" would contain the corporation's data under a single focus for each given subject area. In other words for a subject area such as revenue, there would be *one* data warehouse containing world wide revenue for all of Digital (today it is estimated that there are more than 50 large data bases in the company that manage revenue or revenue-related data!). These new warehouses may not necessarily be single physical data bases, but will have logical extensions and the warehouse data in many cases will be distributed.

Personnel from the VSS data management domain are actively involved in the design of this data warehouse architecture. Operationally VSS has been working to identify and use some of the emerging warehouses for some subject areas. Clearly there is tremendous potential for VSS and Digital to reduce cost and process cycle times in pursuit of our business goals of delivering sustainable world class competitiveness.

Requirements for a Successful Realization of a True Data Managed Environment in VSS

1. A heightened awareness of the cost and value of data/information within all business entities in VSS is critical to the successful realization of the benefits of operating within a data managed environment. VSS spends upwards of *$50M* annually to manage data/information. The data "suppliers" and "consumers" and information management communities are gradually internalizing this significant level of ongoing investment effort and are beginning to link this expenditure stream with cost of data.

To further facilitate this awareness, it would be necessary for a tops-down approach to address the potential benefits. Senior managers must take the lead in this regard and demonstrate leadership in proactively managing this space. The renewed focus on profitability within the corporation should be of great assistance in facilitating this awareness.

2. VSS will continue the excellent momentum it has attained in developing applications/data bases under methodologies that employ sound data management techniques and we have to fully leverage the excellent software tools at our disposal to design, implement and maintain data bases and applications.

3. Continue the excellent partnering between Information Management and Business Project Leaders will also be key to building the data managed environment. Also vital will be continued, effective collaboration between the data management communities within VSS and between the PCU's, ABU's and IBU's if the goal of enterprise-wide data integration is to become a reality.

Conclusion

The VSS Information Management organization is working very hard at driving towards achieving a data managed environment. We solicit and welcome your help in making this a reality for VSS and Digital.

VSS Info-Service Center News

Info. Center Staff

Feature Article:

Compound Document Architecture (CDA) opens up a vast capability for information workers to directly import/export documents from one format to another. For example, it enables a user on a PC using an application like Lotus 1-2-3 to convert the information and include it into a Compound Document Application. Images scanned in using a Scanner are also able to be incorporated into Compound Documents. Digital Applications (DECwrite, DECdecision, DECPresent) are based on this Architecture. These applications contain built in 'front end' and 'back end' translators to 'import/export' documents.

Perhaps the simplest use of this Architecture is through the use of the DCL command CONVERT/DOCUMENT. This DCL command will let the user convert data from one format to another. The user supplies the name of the data file that is to be converted and uses the '/FORMAT=' switch to tell the CDA converters how to read this data. The name of the output file is specified next along with another '/FORMAT=' switch to tell the CDA converters how to write the data.

Example:

$ CONVERT/DOC lotus.wk1/format=WK1 lotus.dtif/format=DTIF.

This command will convert a file created by Lotus 1-2-3 into a format that will be able to be read by a DECwindow compound document application.

Certain input formats can not be converted to certain output formats. For example, a DCA formatted file (IBM's Document Content Architecture) can not be translated to a DTIF (Digital Table Interchange Format).

A document has been created which provides a road map view of the CDA converters at a glance. Users can now determine if a desired output format can be created from a given input format. This 'CDA Road Map' can be pulled from the VSS Info Center's notes conference located at MSBCS::VSS_INFO_CENTER. It is in PostScript form.

New Products

Access RDB databases from within PC Lotus 1-2-3

The DataLens driver from SOMA of Toronto allows Lotus 1-2-3 users on PCs to query Rdb/VMS databases and VAX RMS files on a VAX/VMS server. The driver makes use of Digital Equipment Corporation's PATHWORKS for DOS networking software and SQL/Services software library to perform the actual queries. Installation was very easy and completed in less than 10 minutes. The documentation was very robust although a few Lotus query examples would have been helpful for testing out the driver with a live database.

The required Lotus 1-2-3 files were updated and access to a RDB was made on the first attempt. Ordering info: the DEC part number is QB-GVHAD-WA. US list price is $95. Both 5.25 & 3.5 diskettes are shipped with the product.

A hot line is provided with the license to answer any technical questions that one may have.

Query RDB/RMS databases on your PC/MAC with DECquery –

PC users can query Rdb/VMS databases and VAX RMS files on a VAX/VMS server. The DECquery tool makes use of Digital Equipment Corporation's PATHWORKS for DOS networking software and SQL/Services software library to perform the actual queries. This tool is available now for the PC and is in field test for the MAC.

Functions that can be performed with DECQUERY are:

Joins: Joining data from one table with another based on a common data element.

Subsets: Culling out data the does not meet your AD HOC query criteria. Ability to group data records in columns and aggregate values (e.g., calculates totals, subtotals, minimums, maximums for statistical reports).

Reports: Allows users to generate customized, semi-complex reports from the collected data.

Exports: Once data is collected that meets your criteria, It can be saved and exported to several formats (Lotus 1-2-3 .WK1, .DIF, .DBF, Ascii_tabular, Comma delimited text).

Currently this tool allows read only access to a single database. Future versions will allow access to multiple databases during the same query session. Ordering info: Digital Part Number for DECquery is QB-GGDAW-AA for MSWindows QB-GGBAW-AA for DOS character cell. US list price is $199. DECquery notesfile location is VIA::DECQUERY.

Helpful Hints from the Info Center

Help Save A Tree

Printers that can handle PostScript files will accept several useful print command qualifiers. There is a qualifier command to change the orientation of the file (PAGE_ORIENTATION = LANDSCAPE or PORTRAIT). Another will allow you to put multiple PostScript pages on a single sheet of paper (NUMBER_UP=2). In addition, you can specify a subset of pages to print from your PostScript file (PAGE_LIMIT=(10, 12)). Below is an example of the DCL print command along with the parameter qualifier that allow you to put 2 pages on a sheet of paper, only print out pages 10-16, and turn the page orientation sideways (landscape mode):

$ print/queue=(Your PostScript Queue's name)/Param=(data=post, NUMBER_UP=2,-
"PAGE_LIMIT=(10,16)",
PAGE_ORIENTATION=landscape).

Is Your Terminal Insecure?

By using the BREAK key, a user can 'break' out of the current terminal session and 'LOCK the LAT.' What this buys a user is the ability to keep an application active yet allows them to leave their terminal unattended AND secure. (I.e., a user in the middle of a DATATRIEVE or LOTUS 1-2-3 session can Hit the BREAK key, get the LOCAL> prompt, type in LOCK and supply a password when asked. The prompt then becomes UNLOCK PASSWORD> until the correct password is entered. By typing in RESUME at the LOCAL> prompt the user is put back into the application (a Ctrl-W might be needed to refresh the application.)

Doing the Work of Two

A user on the LAT can also have multiple sessions going. By using the BREAK key the user can get the LOCAL> prompt and log on again. To switch between sessions the user need only hit the BREAK key and issue a FORWARD command at the LOCAL prompt.

Running out of disk space? Here are a few quick tips that might help you out.

1) Mail Hints – From within mail issue the command COMPRESS. This will make your mail file smaller. Empty you wastebasket with the PURGE command or use the MAIL command SET AUTO_PURGE to empty you wastebasket automatically every time you exit the mail application.

2) DCL SET FILE Command – By issuing the DCL SET FILE command with the / VERSION_LIMIT switch, you can limit the number of versions of a file you wish to keep. Wildcards are allowed in file names. $ SET FILE /VERSION_LIMIT=1 NETSERVER.LOG. This command will limit the number of versions kept for the NETSERVER.LOG file to 1 (the most recent).

"PC Week" User Poll Rates VAX 6000 Number 1

Ruth Porter
Press and Analysis Relations Consultant

If you've noticed the posters in the lobbies of BXB1 Digital's first place finish in the 1989 "PC Week" corporate user satisfaction poll - well, get ready for a new version of that poster. The VAX 6000 systems won first place again!

Once more, buyers of minicomputers have rated Digital's VAX 6000 systems Number One in the "PC Week" Poll of Corporate Satisfaction. Quality of support for its operating system, range of available applications, quality and variety of languages and programmers' tools, and clarity of documentation are just a few of the categories in which users were asked to rank their systems.

The 1990 "PC Week" user satisfaction survey tabulated the responses of 531 corporate or institutional buyers who have had installed for at least three months one or more of the models listed. (The 1989 survey included 460 responses of users whose systems had been installed for at least six months.)

Competing for top spot in the 1990 poll were the VAX 6000 series and the HP 3000 Series 900. The VAX 6000 systems edged out the HP 3000 Series 900 in most of the 24 categories, earning 14 first-place finishes or first-place ties. In the 1989 poll, the VAX 6000 systems also finished first with 9 first-place finishes versus 8 first-place finishes for the runner-up, the HP 9000 Series 800 system.

The equipment included in the 1990 survey, with their relative rankings and overall weighted scores, is listed below.

Rank	System	Overall Weighted Score
1	DEC VAX6000 Sys	78
2	HP3000 Series 900	78
3	HP9000 Series 8xxS	77
4	DEC MicroVAX3000 Sys	76
5	NCR Tower-32 Series	71
6	IBM AS/400 Series	69
7	Wang vs. Series (5000, 7000, 8000, 10000)	65
8	DG Eclipse MV/Family	64

There were 24 categories in which these minicomputers were rated in the 1990 survey. They are listed on the following page in their order of importance to the users who were polled. Categories with a star (*) are those in which Digital's VAX 6000 systems were rated number 1. Categories in which the HP 3000 Series 900 received a number 1 rating are marked with a pound sign (#). The IBM AS/400 Series took no first places in 1990. [IBM's AS/400 took two firsts in the 1989 survey for Range of Security Options Available and Quality of DASD Support. The DASD (direct-access storage device) Support question was least important in 1989 and was dropped in the 1990 survey.] *See following page for list of categories.*

Don Harbert and Pauline Nist accept the PC Week "Poll of Corporate Satisfaction" award given to the VAX 6000 for the second year in a row. Presenting the award is (center) Susan Pasieka, PC Week regional sales manager.

Categories which in minicomputers were rated:

- # *Overall System Reliability*
- # *Overall System Performance*
- # *Cost of Equipment, Service and Support from the Vendor*
- * *Quality of Support for the Vendor's Own Operating System*
- # *Value Relative to Cost*
- * *Ability to Connect System with Similar Class of Processor*
- * *Completeness and Organization of Documentation*
- *# *Ability to Add Users Incrementally*
- *# *Clarity of Documentation*
- # *Quality of Equipment, Service, and Support from Vendor*
- # *Ease of Maintenance*
- * *Range of Applications Available*
- * *Quality and Variety of Languages and Programmers' Tools*
- * *Ability to Connect with Systems with a Different Class of Processor*
- * *Quality and Variety of End-User Interactive Environments*
- * *Support for Host-Based Application Development*
- # *Effective Cost-per-User Ratio*
- *# *Range of Security Options Available Support for Multivendor Networking and Applications Portability*
- * *Ability to Support Distributed Applications Running on PCs*
- * *Options for Creating Wide Area Networks*
- * *Ability to Function as a Server in a PC-Based Network*
- # *Depth and Quality of Training Provided by Vendor Availability of Support for 3rd-Party or Non-Proprietary Operating Systems.*

Let's go for three years in a row!

If you are interested in getting a reprint of this report, contact Ruth Porter.

Systems Integration and Performance Engineering

Sas Durvasula
Group Manager

"We know our customers want standards, and Digital's strategy is to provide the products and services our customers need to integrate a multi-vendor computing environment."

Ken Olsen

Digital has made a major strategic change in its approach to marketing VAX/VMS systems. VAX/VMS is now offered as an open system into distributed, heterogeneous client/server environments. This change is a necessary step in making Digital a leading systems vendor in the 1990's. In order to make this a reality, DEC's products need to be interoperable with other vendors' hardware and software, from desktop to datacenter.

Our customers have been using VAX/VMS systems for the past fourteen years to solve a variety of problems, through several thousand applications currently run on VMS systems. DEC needs to extend this mature computing environment to include systems from other vendors. This implies that the hardware and software pieces to support this environment must be in place. The migration of customers into these complex environments must be transparent to the user.

This is only possible if all the pieces are integrated and work well together. How do we guarantee, with some level of confidence, that all of these components work well together? Experience has shown us that setting up these configurations and testing them helps us better understand these environments. In order to accomplish this, VSS has given its Systems Intergration & Performance Group,"SPE" the mission to test for functionality, performance, and integrability to interoperate.

Our customers today use PC's, workstations and host systems (department or datacenters) connected through local area networks running VMS, MSDOS, different flavors of Unix, MAC OS, DECNET, TCP/IP and MVS. To effectively integrate our products into these environments, we need to design and manufacture our products to meet the various standards and protocols that allow easy connection to interoperate. Digital has offered Network Application Support, "NAS" to transition our products to an open systems environment. We are offering Unix, Posix and XPG compliance as a necessary first step.

Systems integration entails work in several areas of development-tools for modeling, workloads development and testing for compliance to standards. Most systems environments today are heterogeneous; that is systems with different operating systems connect through networks that operate with different protocols.

To meet our customers' expectations Digital needs to:

1) Understand their environments needs
2) Size their requirements
3) Protect their investments/provide competitive products
4) Allow growth for long term
5) Provide predictable and dependable performance
6) Provide the necessary consulting help.

Digital is embarking upon a fascinating set of challenges. Our VAX/VMS family of computers coupled with our recent desktop PC's and workstation offerings, along with our NAS tools, make us uniquely qualified to deal with these challenges and provide the most dependable products, solutions, and services to meet our customers' needs.

When every vendor is claiming that their systems are open, it is important to demonstrate to our customers that Digital has it now and that it is a leader in providing standards and implementing them. As Digital develops Posix interfaces to VAX/VMS and RISC/VMS, SPE will test to ensure that the POSIX interface makes our systems truly open. SPE will also monitor the performance of these interfaces to make sure they substantiate our claims in the marketplace.

The client/server computing environment also offers challenges. The first is to make sure that all the hardware and software components are available to make the systems work in a heterogeneous environment. Individual components may work. However, when put together in various heterogeneous configurations they may not. The questions of interoperability and compliance to standards must be examined. The best way to study functionality is to set up the configurations and test them. Typical customer environments must be run on these configurations to uncover problems before the systems go to customers. Since maximum configurations may not always be available, a more efficient technique of modeling these environments will be used to predict system capacity. Care will be taken to validate the models with measured data to avoid gross errors in prediction. This effort will help us provide Performance Summary and Configurations Guidelines documents which are extremely critical in selling into these environments.

SPE will continue to develop the necessary modeling tools that will allow us to model the base products and their behavior in differing environments. We have organized the client/server application environments into four broad categories: data, network, compute, and PC LAN. Aggressive efforts are underway to characterize each of these environments through the development of standard workloads which can be used to characterize our products. SPE has built an integration lab where these environments are set up and used to validate our modeling efforts and predict systems behavior. Experiments in this lab will also help us understand the boundary conditions of the systems response time and throughput.

We have networked client/server pilot integration projects that will allow us to understand the hardware/software bottlenecks and how we can fine tune our products before they reach our customers. The name of the game is to specify our products accurately and set the right expectation to our users. These efforts will also allow us to influence our product development efforts so as to continuously improve our designs to provide leadership products to our customers. We help our customers to design the growth they need using the tools we offer as part of our integration effort. In essence, Digital will be a leading systems integrator as we are attacking several problems in a scientific way to do the system integration through modeling, synthesis, and integration pilot projects. There is no longer scope for brute force methods to succeed as the problem of systems integration is increasingly complex, as well as, nonlinear.

We are also piecing together packaged servers that can be marketed to solve the customer's problems in several application areas. We have projects under way to make our servers integrate effectively into the open systems markets.

Digital will win with customers in open system intergration because we are taking a scientific approach and using methods to model the problem and piece together solutions that work.

The future is heterogeneous, client/server computing with compliance to open standards. Digital is on its way to becoming a leading vendor in these markets in the 90's, provided we aggressively continue our efforts in systems integration and performance engineering.

System Performance Evaluation Cooperative Update

Bhagyam Moses, Engineering Manager
Jeff Detjen, Senior Engineer

Spec Update

System Performance Evaluation Cooperative (SPEC) is a non-profit organization founded around two years ago with the goal to facilitate the industry with a meaningful suite of benchmarks to fairly compare the performance of computer systems across vendors. It is represented by 22 major computer companies with 9 Steering Committee members. DEC is a Steering Committee member. The members include ARIX, AT&T, Bull, S.A., Compaq, Control Data, DEC, Dupont, Fujitsu, HP/Apollo, IBM, Intel, Intergraph, MIPS, Motorola, NCR, Prime, Seimans, Silicon Graphics, Solbourne, Stardent, Sun and Unisys.

Benchmarks are submitted to SPEC by members. The benchmarks must solve a real problem, must run on all vendor systems and must represent a real application environment. The benchmarks are evaluated by SPEC members to make sure that they meet this criteria. This is mostly done at what is called a "bench-athon" where all the SPEC members bring their systems and engineers to a particular location and test all the benchmarks over a week. Most of the testing is done to verify any portability changes made by vendors and to ensure that these changes did not change the benchmark and that they did not handicap anyone else from running the benchmark. It takes one or more bench-athons to vote the benchmarks in. The benchmarks are voted in by the Steering Committee.

SPEC Release 1 was announced in October 2, 1989. This release consists of 10 compute-intensive benchmarks and was the first suite announced by SPEC. SPEC SDM1 is the second release announced more recently on May 14, 1991 which consists of 2 system level benchmarks. SPEC not only provides benchmark suites but also publishes a quarterly newsletter that consists of performance data provided by its members on the SPEC benchmarks. Data on over 100 systems has been published to date. The trade press and industry consultants have written several articles on SPEC. SPECmarks are quoted quite commonly in literature.

SPEC Release 1

Fifty benchmarks were submitted to be included in Release 1; however, only 10 benchmarks passed the benchathon testing. Thus, the suite consists of 10 benchmarks – six of them are in Fortran doing floating point operations and four of them are in C computing integer arithmetic.

In the results sheet published in the newsletter, all 10 benchmarks are listed with elapsed time on a reference system (VAX 11/780), the elapsed time taken on the system under test and the ratio between the two. This ratio is referred to as the SPEC ratio. The geometric mean of the 10 SPEC ratios is what is called the SPECmark for Release 1. SPEC also publishes system throughput for multiprocessor systems. To prevent confusion with SPECmark, SPEC uses SPECthruput as the throughput metric (# of CPUs @ SPEC throughput ratio).

SPEC Release 1 was recently quoted in the press as "losing its luster" (Computerworld, 5/13/91). This was mainly because of the SPEC data presented by IBM and HP using their new RISC optimizing compilers. Their compiler optimizations have been showing extremely high SPEC ratios for the Fortran benchmarks. However, the recently published data from HP and IBM attach unrealistic SPECratios to matrix300 benchmark in SPEC Release 1, indicating that the benchmark was optimized away not to do any of the work it was designed to do. Table 1 presents the HP and IBM data in question.

SPECratio is the ratio between the time it takes to run the benchmark on the system and the time it takes on the reference system - VAX 11/

780. SPECmark is the geometric mean of the IO benchmark SPECratios. SPECint is the geometric mean of the integer benchmark SPECratios. SPECfp is the geometric mean of the floating point benchmarks.

Referencing Table 1, it can be seen that the SPECratios on the matrix300 are substantially higher than the SPECratios.

Figure 1 is used to show the impact of matrix300 on SPECmark, SPECint and SPECfp on the IBM RS6000 Model 550/950 and HP9000/730 respectively.

Maximum difference is seen in the SPECfp (44%) with a 30% boosting of the SPECmark. Matrix300 is a floating point benchmark and, therefore, has no impact on the SPECint.

The impact on the HP results are slightly lower than the IBM system, with SPECfp increased by 25% and SPECmark by 16%. This is because the SPECratio for matrix300 on the IBM system was 729 while on the HP system it was 273. See Figure 2.

The optimization of the matrix300 benchmark is done solely by the compiler and its ability to recognize code that is badly aligned or not used later in the program. As time goes on, many other companies besides HP and IBM will be able to increase their SPECratio equally high. The two optimizations that caused the benchmark to be broken are:

1. Elimination of dead code
2. Optimization of cache misses.

Elimination of dead code:

VAX Fortran compiler does remove dead code from scalar values but does not achieve this level of optimization with array values. The IBM and HP compilers are optimized to remove dead code from array values as well.

Table 1.

SPEC Release 1 Benchmarks	IBM RS6000 550/950 SPECratio	HP730/750 SPECratio
001.gcc	28.6	46.5
008.espresso	33.9	55.2
013.spice2g6	47.2	60.9
015.doduc	49.6	64.0
020.nasa7	144.4	73.7
022.li	33.8	50.3
023.eqntott	40.0	52.6
030.matrix300	729.8	273.3
042.fpppp	86.6	107.0
047.tomcatv	138.0	67.4
SPECmark	72.2	72.2
SPECint	33.8	51.0
SPECfp	119.7	91.0

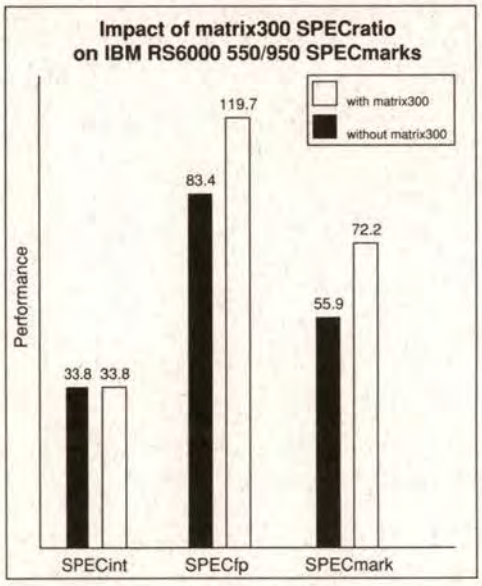


Figure 1.

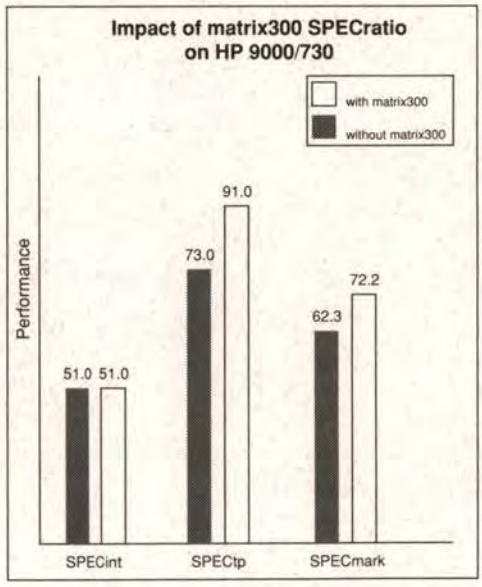
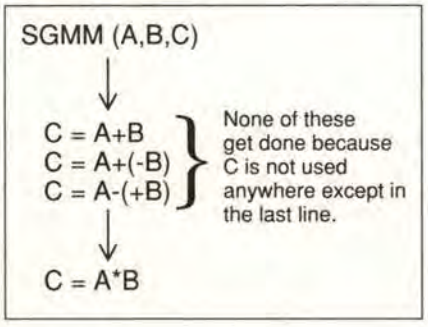


Figure 2.

In matrix300, there are two matrices – one consisting of all 1.0s and the other with all 2.0s. The benchmark manipulates the values of the two matrices and creates a third matrix. The highly optimizing compilers recognize that the program is working with the same values and the same operations within the same arrays. When the compiler goes through and optimizes the code, it realizes that many of the commands are redundant, so the compiler eliminates them. The values used during the manipulation of the data in the matrices is not used in the program until the last iteration of the program. So if the compiler recognizes that the intermediate values are not used, then it eliminates these operations.

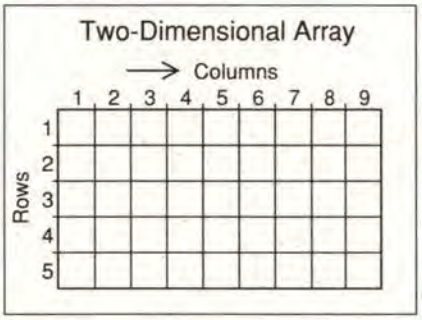
For example:



To reduce cache misses:

The ability of the compiler to recognize that a program is fetching data in an inefficient manner and then to make the necessary changes to become efficient is another area that these highly optimizing compilers score well. The approach used by the compilers is to reduce the cache misses as far as possible.

A major portion of the code in matrix300 goes through a two dimensional array to compute a single value to be used in other parts of the program. In most FORTRAN programs, the most efficient method of obtaining data from an array is to go down the rows in each column. However, the matrix300 code goes across the columns. This causes very few values of each fetch to be used in the computation. The HP compiler recognizes this and changes the stride to fetch across the columns so that all the values fetched will be used, so that there are fewer cache misses.



In summary, these optimizations on a real application program are in fact welcome. However, when benchmarks are set up to do consistent amount of work across all systems to measure elapsed time, and some systems do all the operations while some do not, then it becomes an unfair game.

Note: SPEC is working on this problem and solution should be made available in the next release.

SPEC SDM 1

SPEC SDM 1 consists of two system level benchmarks – SDET and KENBUS. They were both developed to represent software development environments. SPEC was anxious to announce this release to address the issues that SPEC Release 1 evaluates the CPU power and not the total system performance. The metric used by SDM to evaluate work done is the number of scripts completed per hour (throughput). The script consists of a sequence of typical commands executed by a software engineer.

SDET represents a large commercial UNIX/C based software development environment. This workload model was developed by Steve Gaeden while he was a student under Domenico Ferrari and later the workload was characterized at AT&T.

KENBUS1 represents UNIX/C usage in a research and development environment. This workload was developed by Ken McDonell at Monash University and used to be known as MUSBUS.

Both these benchmarks exercise the system to determine its maximum throughput capacity. SPEC SDM data is presented on two separate sheets - one for SDET and one for KENBUS. A throughput curve with supporting data and a description of the configuration used is required. The curve represents the throughput behavior as the workload is increased. Although several processes are running on the system, the concept of users is not promoted because remote terminal emulators are not used.

VAX6000 Model 500 SDET data is provided in Figure 3, as a sample of an SDM datasheet.

Table 2 presents the data that was made available to the press at the May 14, 1991 SPEC SDM1 announcement.

The interesting point in Table 2 is that the RS6000-550 with a SPECmark of 72.2 performs at 21.7 on SDET. The VAX systems show close SPECmark performance on SDET as well. See Figure 4.

In summary, SPEC has two benchmark suites - one CPU intensive and the other system level. There are a few issues with SPEC Release 1 that are currently being worked on. The matrix300 problem should be resolved soon. Publishing of data for products to be announced in 12 months was recently reduced to 6 months to address the issue, with compiler versions coming out more rapidly than anticipated. SPEC's venture into system benchmarks is a move in the right direction. SPEC is working on future releases that will include I/O and commercial benchmarks. SPEC works with both profit making and non-profit making performance organizations, not only to avoid redundancy of efforts, but to jointly address the issues around fair benchmarking in computer performance evaluation.

Note: People in DEC that are actively involved with SPEC are:

DEC SPEC Program Office – Bhagyam Moses, Kathy Campos

Attendees at Steering Committee/ Board/Subcommittee meetings – Bhagyam Moses (voting member), Paul Kruger, Dileep Bhandarkar, Mike Greenfield, Alex Bronstein

Attendees at Benchathons (have attended at least one benchathon) – Jeff Detjen, Jim Lo, Bob Sibley, Paula Smith, Paul Douglas, Rajiv Mahajan, Saurabh Srivastava

Project Leaders for Benchmarks – Jim Lo, Bruce Keith.

DEC has hosted three meetings and more recently hosted the SPEC SDM1 announcement and Steering Committee meeting on May 14, 1991.

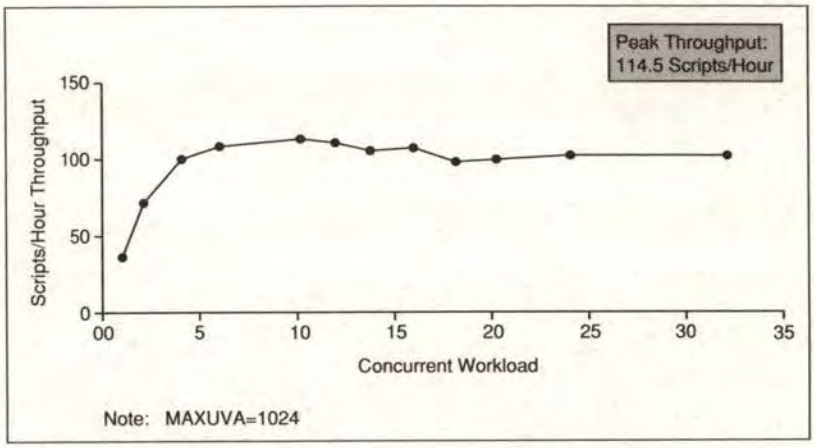


Figure 3.

Table 2.

System	SPEC-MARK	Scripts/Hour SDET	Relative to 780	KENBUS	relative to 780
CDC 4680	42.6	267.9	24.8	2097	20.5
RS6000-550	54.3	234.6	21.7	–	–
RS6000-530	32.1	140.6	13.0	–	–
RS6000-320H	24.6	136.4	12.6	–	–
DECstation 5000 Model 1200	18.5	133.7	12.4	1055.4	10.3
VAX6000-520	–	210.4	19.5	1434.4	14.0
VAX6000-510	13.2	114.5	10.6	992.9	9.7
SparcStation 2	17.6?				
tmp files(mem)		171.4	15.8	986.0	9.6
tmp files(disk)		140.4	13.0	935.9	9.1

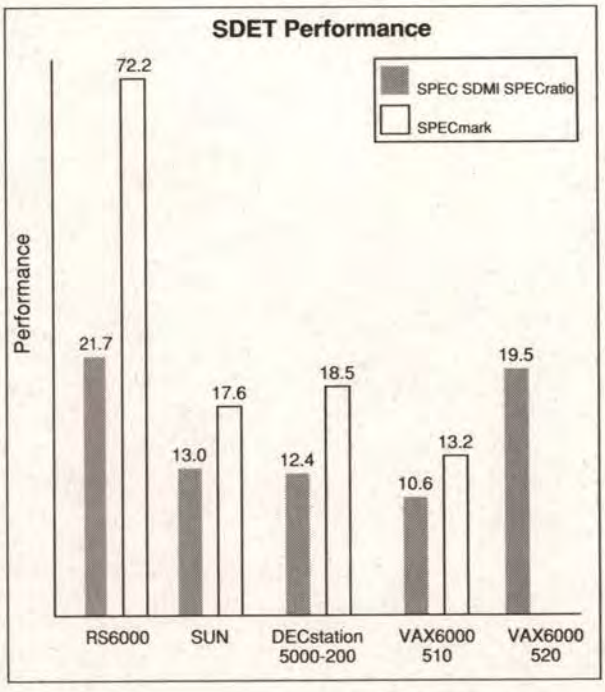


Figure 4.

New VAX VMS Poster with Larry Bird

After receiving numerous requests from Sales and our Channels partners for a new VAX family poster, VSS Marketing decided to take an unusual approach to generate new excitement around its VAX line. In June, VSS introduced a new VAX family poster which features Digital's VAX family of superstar products along with basketball superstar Larry Bird – under the theme of *"Power and Strength Come in All Shapes and Sizes".*

Our mission was to symbolize the power and strength our VAX systems are known for combined with an image that people could readily identify with. Larry Bird of the Boston Celtics fit that image – and allowed us also to publicize Digital's affiliation as the official computer system of the NBA.

The one-hour photo session with Larry was conducted very quietly and under tight security at Digital's Parker Street photo studio. After the session, Larry kindly autographed the basketballs used as props which were then donated to national charities. These basketballs are commanding huge bids (up to $2,000 each) for worthy causes.

Per the terms of our contract with Larry, the posters were printed in limited quantity – and have been distributed to sales management and our channels partners. Unfortunately, they are not available for order.

VSS Marketing would like to take this opportunity to say thanks to all of VSS – marketing, product management and engineering – along with the VAX workstation group, for helping make this poster a reality and for bringing us a product lineup that exemplifies "power and strength in all shapes and sizes". We can all be proud of the effort that made this possible.

Larry Bird, seen here palming the ball with Bill Demmer at the photo shoot, is featured in the newest VAX VMS poster for Sales and Channels distribution,showing that "Power and Strength Come in All Shapes and Sizes."

Awards

Q3 Patent Award Recipents

Front row, left to right: Victoria Triolo, Mark Haq, Bill Grundmann, Maurice Steinman, Rick Hetherington, and David Pimm.

Back, left to right: Andy Ingraham, David Webb Jr., Dave Hartwell, Paul Natusch, and Rick Gillett.

Missing from the photo was: Robert Silver, Elbert Bloom, Leon Hesch, William Samaras, Darrel Donaldson, Tryggve Fossum, Francis McKeen, Dwight Manley, and Mathew Adiletta.

Entry Systems Business Gives Q3 Awards

Duncan Anderson, Entry Systems Business (ESB) Marketing Manager, recently recognized two ESB employees for outstanding contributions in Q3 1991.

Karen Quatromoni was recognized for managing the press/analyst activities in conjunction with three other groups for Digital's January 22, 1991, announcement of the VAX 4000 Model 200, VAX 6000 enhancements, and new storage products for the VAX 6000 family of computers. She was also recognized for being a team player.

Karen has been a Digital employee for almost eight years, working as a promotional writer and editor of the company sales magazine. She has been working at Press and Analyst Relations for the past three years.

Donna Marx won for assembling kits of promotional materials including direct marketing pieces, sales literature, presentations, and reprints of trade magazine articles and analyst reports for use by European marketing managers. Donna also took it upon herself to support two additional ESB managers and their direct reports when they were without a secretary.

Donna has been an administrative secretary at Digital for six and a half years. She currently supports Lou Greer, ESB Sales Training Manager, and his direct reports.

Steve Hirst wins VMS UK Quality Prize

VMS UK have instituted a quality prize - a cash prize of two hundred pounds awarded quarterly to the member of VMS UK judged to have made the most significant contribution to improving the overall quality of VMS.

Steve Hirst has been judged the winner of the Q3 '91 prize, for a long period of energetic, persistent, and imaginative work testing the movefile component of the XQP. Steve's strong commitment to the quality of movefile is apparent to anyone who has worked with him. Steve's work had previously gone largely unrecognized, which the judges decided was an important consideration.

The VMS UK quality engineering group aims to improve the overall productivity and quality of VMS UK by introducing, promoting and supporting better software engineering methodologies and processes. Currently, the quality engineering group is introducing formal inspections of code and other project documentation, and is engaged in test planning and specification. In the near future they plan to introduce structured testing into the department.

Continued on next page.

Promotions

Jack Pinder receives 25th Anniversary Award

The VSS Headquarters Organization recently celebrated the 25th Anniversary Service Award for Jack Pinder, VSS Facilities/Planning Manager. Throughout his years, Jack has been instrumental in site Search, Selection, Construction and Startup of key manufacturing facilities for DEC in Europe, US and GIA.

In Europe Jack was involved with Ayr and Edinburgh, Scotland, Galway (Phase II) and Clonmel, Ireland, and Kaufburen, Germany. In the US, Jack was involved with Westfield, Westminster, Boston, Derry, Augusta, Greenville, Burlington and Phoenix. In GIA, Jack helped start-up pilot plant in San German.

Jack, an avid fisherman and wood carver, is married with four children and resides in Leominster.

VSS wishes Jack continued success in the years to come.

Joe LaRose, new VSS Finance Manager

We are pleased to announce Joe LaRose as the new VSS Finance Manager. As many of you know, Joe has been the VSS Manufacturing Controller for the past two years. Joe has held a series of Finance positions within Digital, starting in 1976 as the Controller for the GIA Field Organization, moving next to be the Corporate Manager of Internal Audit and then to the Computer Systems Manufacturing Organization as the Group Controller.

Joe will be replacing Rich Butler in the role of VSS Finance Manager. We welcome Joe to his new position and look forward to his becoming a member of the VSS Staff and the Operations Finance Staff.

Bill Demmer
Dick Fishburn

Steve Delahunt promoted to Consultant Engineer

Steve Delahunt was promoted to the position of Consultant Engineer in April, 1991. This promotion was as a result of Steve's work on the AQUARIUS program. Steve was the AQUARIUS SYSTEM CONTROL UNIT (SCU) project leader. He was responsible for the design of 16 MCA3 gate array types and 4 Multi Chip Unit (MCU) types, and the SCU microcode. In addition Steve provided consulting help to the XJA project and was the interface to the AQUARIUS Memory Module design team in SHR. Steve's technical contributions in the SCU area include: the overall architecture of the SCU; the interfaces between the SCU and the Mbox, XJA, Memory and SPU; and some of the control logic. Also Steve drove the debug of the SCU both in simulation and in hardware. The SCU supports fully configured VAX9440 systems with 4 CPUs, 4 XMIs and full memory and has had only a handful of bugs throughout the debug.

Steve also contributed widely in many other areas in the AQUARIUS program. He wrote the initial requirements documents for SID (the gate level synthesizer) and for AUTODLY, the timing analyzer. Also Steve developed a process which would allow individual MCAs to be timing analyzed in 2 hours, instead of the 4 days that the system model took. Since the SCU has interfaces to all the major AQUARIUS subsystems, i.e., the CPUs the Memory, the XJAs and the SPU, Steve was much in demand during the AQUARIUS system debug and spent much time in the lab during that phase of the project.

Currently, Steve is working on a File Server project, which involves groups from LKG, SHR, and MRO.

Before AQUARIUS Steve worked on the VENUS project (VAX8600), where he was responsible for the clock module and the clock distribution. He also provided clock system consulting to the ANDROMEDA and MORNINGSTAR projects and invented a self-deskewing clock system for the VENUS 2 project.

Steve joined DIGITAL in 1982. Prior to that he worked for International Computers Ltd (ICL) in the UK for 13 years, where he was involved in ECL mainframe development since 1970, and was the product manager for the ICL 2970 mainframe. He also led several other projects, both ECL and CMOS.

Steve graduated from the University of Manchester in England in 1969 with a Bachelor of Science (double major with honors) in Physics and Electronic Engineering. Steve has applied for and received 5 patents. Steve spends much of his free time with his family and has a young son and daughter. In addition, he is interested in electronic design and construction, maintaining his house, gardening, and ham radio.

Dick Sites promoted to Senior Consultant Engineer

I am very pleased to announce that the Corporate Consulting Engineer Review Board has informed us that Dick Sites has been promoted to Senior Consultant Engineer.

Dick has worked in the Semiconductor Engineering Group since 1980. He holds a Ph.D. in Computer Science from Stanford and a B.S. in Mathematics from MIT.

Dick's promotion is in recognition of his many technical achievements in Digital over the last 11 years. In particular, the development of the Alpha processor architecture and new software translation technology as well as the V-11 (VAX 8200) processor chip set. Dick has filed 22 patent applications in both hardware and software technologies since 1983.

Please join with me in offering congratulations to Dick upon his achievement of this significant milestone in his career.

Maurice Marks

Zarka Cvetanovic promoted to Consultant Software Engineer

Zarka Cvetanovic has been promoted to Consultant Software Engineer in recognition of the leadership role she has played in parallel processing research at Digital. Zarka joined Digital in 1986 to work on the Andromeda parallel processor system, a prototype consisting of 64 MicroVAX processors. Upon completion of this project, she formed and led an advanced development team which explored parallel processing issues for the VAX 6000 series systems. More recently she has been involved in combined vector/parallel processing and has optimized a number of benchmarks for our key customers. As a member of the VSS/Midrange Systems Engineering Group, Zarka is currently working on the performance modeling and analysis of future Digital products.

Zarka received a Ph.D. degree in Electrical and Computer Engineering from the University of Massachusetts, Amherst, in 1986. Since then, she has published eight technical papers in international conferences as well as technical journals, including IEEE Transactions on Computers, The Journal of Supercomputing, and IBM Journal of Research and Development. Zarka is a member of IEEE and ACM.

Doug Williams

Brian Allison promoted to Sr. Consulting Engineer

I am pleased to announce that the Consulting Engineer Review Board has informed us that Brian Allison has been promoted to Senior Consulting Engineer.

Brian has worked for Mid-Range VAX Systems since starting as a VAX 11/750 microcoder in 1977.

Brian was promoted to Consulting Engineer in 1985. His current promotion is corporate recognition of his contributions to the VAX 6000 product platform, the VAX 6000-200 product, and the new Laser platform.

Brian authored the VAX 6000-200 system specification. He drove the bus definition to 64ns performance, delivering 100 MBytes/sec of throughput, targeted to support both CVAX and Rigel processors. He was a key player in defining SMP console specifications with VMS and he ensured that the original XMI specification allowed for the eventual implementation of write-back caching (implemented for Mariah and NVAX). The ISS revenue to date for the VAX 6000 product family is $5.9B. The product family has won numerous awards including the Digital Review Target Award for best multi-user system in 1989 and 1990 and it was Top-Rated in the PC Week poll of Corporate Satisfaction in the mini-computer category for both 1989 and 1990.

Please join me in offering my congratulations to Brian upon his achievement of this milestone in his career.

Pauline Nist

VAX 9000 Historical Hardware Overview

Warren Peluso
Group Engineering Manager

The VAX 9000 System development (AKA Aquarius) was the largest technical and program management challenge ever attempted by Digital in its 34 year history. At its peak, the program was comprised of over a thousand employees across many Digital organizations and involved dozens of external suppliers. In addition, several strategic vendor relationships had to be developed in order for the program to succeed.

The program was initiated in the 1984 timeframe during the developmental wind-down phase of the VAX 8600 (AKA Venus). As the corporation was preparing to start shipping the VAX 8600, a small group of engineers and managers, under the leadership of Group Manager Joe Zeh, started discussions and planning about a high-performance follow-on product to the VAX 8600. Subsequently, an advanced development program, code named Alpha, was initiated to determine feasibility of some of the key concepts being proposed for what was to be eventually code named Aquarius.

Approximately six years later, thanks to a major commitment from management, and after a long and significant effort by many dedicated and committed employees, the VAX 9000 is shipping!!!! The Aquarius Program goal was to develop a 30 MIPS (minimum) VAX-based processor system capable of competing in a wide range of high-performance applications. The system had to be expandable to a quad processor (100 MIPS min., including overhead) and was required to have vector processing capability as an option. It was also determined that any technology development undertaken for Aquarius had to be readily extendable to follow-on products planned for the Aquarius system family. This would allow Digital to maximize the return-on-investment for the significant development dollars required to bring Aquarius to market and would allow us to introduce competitive follow-on products that would maintain Digital on the high-performance systems "price-performance curve" for some time to come. (Reference paragraph below.)

All of these suppliers played a strategic role in Aquarius. In some instances, Digital resources were co-located at these suppliers' facilities in order to facilitate communications between the respective development teams and to help solve problems.

The VAX 9000 High-Performance System spans a broad range of hardware technological firsts of which Digital has a right to be proud. Some of the more salient ones being:

Some of the major strategic vendor relationships developed during the long development cycle were:

Motorola – MOSAIC 3 semiconductor technology. (77 Gate-Array options plus 5 Custom chip designs)

Liebert – AC front-end power-conditioning subsystem.

Fujitsu –1. STRAM (Self-Timed RAM) semiconductor technology. 2. Planar module technology.

3M Corp. – High-performance TAB tape.

Rogers Corp – 1. High-performance TAB tape. 2. Power bus bars.

Hughes Corp.– Controlled-impedance flexible signal cable.

Mitsui Corp.– Controlled-impedance flexible signal cable.

HDSC (High Density Signal Carrier)

The HDSC is a state-of-the-art 4 inch square multi-layer controlled-impedance substrate which permits optimum interconnection of the high-performance cpu chips (MOSAIC 3 and STRAM). It is the "heart" of the VAX 9000 hardware technology, being a major contributor to the system's ability to achieve its excellent high-speed performance. Signal lines are 0.7 mils wide and are spaced 3 mils apart (center-to-center). It has nine copper layers (4 power/ground, 2 signal, 2 signal reference, 1 pad) alternately sandwiched between layers of low dielectric constant polyimide insulating material (Er=3.5). Because this whole sandwich is only about 10 mils thick, it is mounted on a rigid baseplate for structural support. The baseplate also functions as a heat sink for the high power chips interconnected on the HDSC. The backside of the cpu chips are epoxied to the baseplate through cut-outs in the HDSC. The I/O signals on each chip are brought onto the HDSC via a two metal-layer flexible TAB (Tape Automated Bonding) tape.

Note: As a point of reference, the diameter of a typical human hair is about 4-to-5 mils thick.

The HDSC started out as an advanced development program back in 1984/85 with a company then known as Trilogy. Trilogy, you may recall, was the company that planned to implement wafer-scale integration but encountered implementation problems (a great idea, but a little ahead of its time). At that time, Trilogy had the core technologists and the base HDSC technology. Digital eventually purchased the assets of Trilogy, and subsequently started planning for full scale HDSC development in Cupertino, CA.

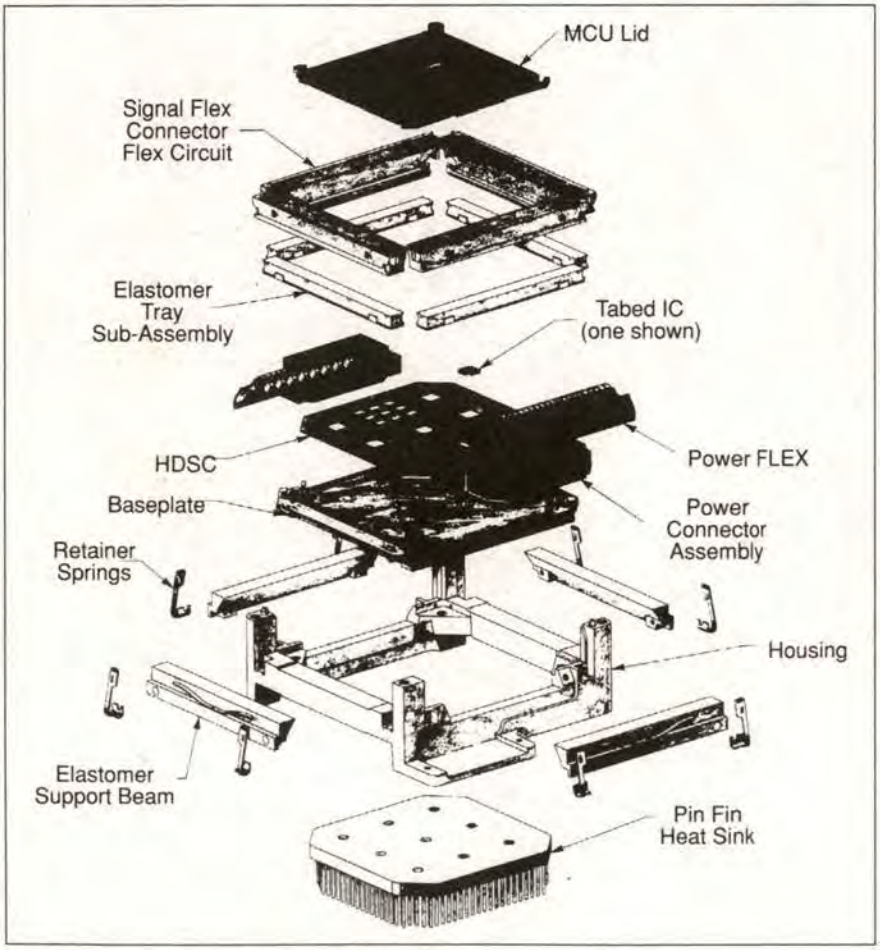


Figure 1. Exploded view of Multi Chip Unit.

Planar Module

The planar module (AKA Planar) is a controlled-impedance 24 layer printed wire board (10 signal, 10 ground, 2 pad layers). It is approximately 1/4 inch thick, and being 25 inches square, it is the largest known two-dimension multi-layer circuit board in full production today. It is the interconnect medium (mother board) for up to 16 MCU's, 13 for the scalar CPU and 3 for the optional vector processor. The Planar carries no power in its layers. Instead, power for the MCU's is delivered to them via special connectors mounted on each MCU which plug into mating connectors mounted on copper bus bars adjacent to the Planar.

The Planar is principally a product of our development agreement with Fujitsu, since Fujitsu was the only PWB supplier with the resources and capacity to work with us to develop such a large board at the program onset. Since then, our Greenville (GSO) plant has also developed the Planar for VAX 9000. In fact, we are pleased to say that GSO was actually the first supplier to "pass" the stringent qualification testing for the Planar. Both GSO and Fujitsu supply Aquarius with planar modules today.

MOSAIC 3 (AKA—> MCA 3, MCA = Macro Cell Array)

MOSAIC 3 is the third generation of Motorola's MOSAIC bipolar semiconductor technology (MOSAIC 1 was used for the VAX 8600/8650). We have implemented MOSAIC 3 in the design of an ECL (Emitter Coupled Logic) custom gate-array, with 77 unique option types plus 5 custom circuit designs for the VAX 9000. These 82 high-performance chip types, coupled with architectural and system design enhancements, provide the backbone of the excellent performance of the VAX 9000.

The MCA3 gate array has 10,000 equivalent gates capability. Each gate can be selected during the design process to be a low, medium, or high power device, depending on performance requirements. 35 watts is the maximum power design limit allowed for each chip in order to maintain device junction temperatures within acceptable limits so that high reliability can be achieved. The gate array has 360 I/O pads (256 signal and 104 power/ground). These 360 pads (90/side), on a 4 mil pitch, are bonded to a flexible TAB tape interconnect which fans out to an 8 mil pitch. This matches the 8 mil pitch outer-lead bond footprint on the HDSC.

Because of the excellent internally developed CAD tools that were available to us, we were able to achieve up to 98.9% utilization of the available silicon in some of our gate array designs!

The five custom chip design types used on VAX 9000 use the same MOSAIC 3 technology as the gate arrays, except that these five chips are generally much more dense than the gate array designs. Power for these custom designs is also limited to 35 watts, and 4 of the 5 designs also use 360 leaded TAB. The fifth design uses 232 leaded single-metal layer TAB tape.

Digital and Motorola had an agreement from the beginning to jointly co-develop the MCA 3 technology since there were significant new areas of technology development required in order for this product to meet our requirements. Motorola had the bipolar semiconductor device physics and silicon process expertise while Digital had the circuit, packaging, and systems design knowledge. Motorola therefore developed the fundamental semiconductor device structures and silicon fabrication process while Digital focused on a broader range of technology areas, such as circuit design, CAD, floorplanning, routing, power bussing, packaging, assembly, test, and failure analysis.

STRAM (Self-Timed RAM)

STRAM architectural technology used on the VAX 9000 is a Digital invention. Unlike the more conventional RAM technology available on the market at the inception of Aquarius, these devices have both input and output latches incorporated into them. They also have the timing critical "write pulse" generation circuitry included into the design. Having both of these features incorporated right into the STRAM silicon instead of on separate silicon chips, as is usually done, provides the VAX 9000 with a distinct system performance advantage.

Two STRAM organizations are used on the VAX 9000, 1Kx4 and 4Kx4. These devices use ECL semiconductor technology and were co-developed by Digital and Fujitsu. Fujitsu currently supplies both of these devices to us in a 48 leaded single-metal layer TAB tape package.

TAB (Tape Automated Bonding) Tape

The high-performance TAB tape used on the VAX 9000 is a controlled-impedance 2 metal-layer design with 360 total leads. One of the metal layers is for the 360 I/O leads (256 signal and 104 power/ground) and the other layer is a ground reference for the signal layer so that the signal lines on that layer will maintain a controlled- impedance. Power and ground is brought into the chip via the 104 leads assigned on the signal layer for that purpose. These power and ground leads are dispersed uniformly around the chip to provide good power distribution and signal integrity control.

This TAB tape provides excellent signal integrity and system performance characteristics, compared to the more conventional PGA (Pin Grid Array) package. When provided in its special carrier, ease of testing and handling is also facilitated.

One of the many design challenges faced by the Aquarius team was the development of a TAB test fixture suitable for "at speed" testing of 360 leaded, 8 mil pitch, Tabbed MOSAIC 3 devices. The fixture had to be controlled-impedance in order not to degrade the quality of the tester signals delivered to the chip under test, and it had to be robust enough to sustain a production environment. The team subsequently developed a fixture with better than 1GHZ capability that is in production at Motorola today.

In terms of suppliers, 3M was the initial strategic supplier for the high-performance TAB tape. Late in the program Rogers Corp. also became a strategic supplier for this material. Today, Digital is the only computer manufacturer utilizing high-performance TAB tape in a volume production environment.

MCU (Multi-Chip Unit)

The MCU, Figure 1, is the point at which most of the Aquarius base technology comes together as an assembly; e.g., HDSC, MCA3 chips, STRAMS, Signal-Flex connectors, etc. Thirteen MCU's comprise a single scalar CPU, and three MCU's make up the optional vector processing unit. Depending on the system's size and configuration, four-to-six more MCU's are used in the System Control Unit (SCU).

The MCU was designed in MRO. Pilot manufacturing of the unit was begun in a small facility in Mt. View, CA, and was then transitioned into Digital's larger facility in Cupertino, CA, for volume manufacturing. The design of the MCU assembly and manufacturing process was also quite a challenge, and is a story in itself.

Continued on next page.

Power System

The VAX 9000 incorporates a very sophisticated and highly reliable state-of-the-art power system, from the front-end primary power conditioning unit down to the individual power regulators that deliver DC power to the chips.

The system has N+1 redundancy for all major power busses and uses 300 Amp power regulators bussed together to deliver power to the semiconductors. Up to five regulators can be paralleled together to provide 1500 Amp power buss capability. Load sharing is used so that all regulators on a buss share the load equally. Several microprocessors within the power system provide an intelligent communication network for monitoring and controlling the power system.

Summary

Looking back in time, the VAX 9000 was a long and challenging program requiring the dedication and commitment of many people. It involved significant risk across a spectrum of new developments which were required to come together at the same time. It wasn't easy, but the goal was achieved and with what appears to be excellent results! Today the VAX 9000 is shipping, and feedback from the field indicates that our customers are very pleased with its performance.

Having recently won Datamation's "Product Of The Year Award" and looking to the future, the VAX 9000 system family has the opportunity to be our flagship product for many years to come. Let's keep the momentum going!

Quality Levels of Power Supplies Exceeds Expectations and Program Goals

Bob Carpenter
Senior QA Engineer

The quality and reliability of the VAX 9000 power units designed at MRO and manufactured in BTO has been outstanding, and I wanted to share some of this information with you. Its quality levels have well exceeded expectations/program goals ever since FRS. There are a number of factors which contributed to this design success, and they are captured in the V9000 power postpartum report. The excellence of BTO power manufacturing is also reflected in these results. BTO and MRO worked closely together during the design, qual, and start-up of V9000 power. Problems were resolved very quickly through this joint effort which resulted in entering the manufacturing phase at a very high quality/reliability level.

This level of excellence has been maintained by close monitoring of goodness levels through the system manufacturing process, as well as field installation and customer performance. All failures are handled through a closed loop failure analysis process which is typically four days from fail to corrective action implementation. BTO has a component F/A lab which complements the analysis/corrective action cycle. Everyone involved with this development and manufacturing effort should feel real proud, and after you take a look at a summary of the data, I think you'll agree with me. I've also included details of each power unit's performance, customer installation information, the method of failure rate/MTBF calculations, and field reliability graphs.

V9000 BTO Power Unit Quality Summary:
(H7380, H7382, H7386, H7388, H7389)

* Average power FRU yield at CAB integration:	99.8%
* Average power FRU yield through system 96 hr test:	99.5%
* Average power FRU yield @ customer installation: (One fail out of all V9000 installations!)	99.98%
* Average yield at customer after an average of 3189 hrs:	99.82%
* Average failure rate after 2300 hrs. at customer site: (Twice as good as program goal: .44/FRU/1st 1k hrs.)	.0017/FRU
* Average power unit pt. est. MTBF in field: (Three times as good as spec/goal ave: 600K hrs.)	1851K hrs.

Note:
1. The internal BTO yield data represents the last four months, and the customer installation/field failure rates/MTBF is data from FRS to the end of April.
2. The power units above make up most of the V9000 "power system," i.e., in the Model 420 there are 19 - H7380's, 6 - H7382's, 2 - H7386's, 6 - H7388's, and 1 - H7389.
3. There are two power units in the V9000 power system (H7215/H7214) which were designed for Calypso and are manufactured in PR. Their field performance is also running above the MTBF spec.
4. This data reflects power units manufactured in the U.S. and tracked in U.S. installed systems.

Customer Installed VAX 9000 Power (July 1990 through April 1991)

Photo 1. H7380

		Q1	Q2	Q3	Q4	Total
Total	210's	35	29	17	0	81
To	410's	16	29	16	4	65
Date	420's	4	30	13	4	51

Number of Power Units per System

	210	410	420
H7380	9	15	19
H7382	4	6	6
H7386	1	2	2
H7388	4	6	6
H7389	1	1	1

Total Power FRU's Installed (JUL90-APR91)

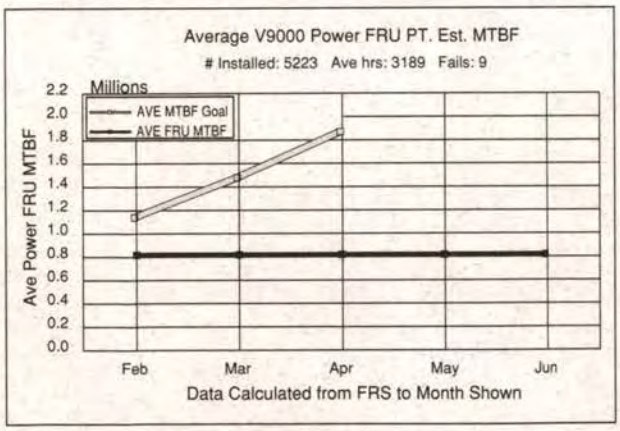
	Q1	Q2	Q3	Q4	Total
H7380	631	266	640	136	2673
H7382	260	470	242	48	1020
H7386	75	147	75	16	313
H7388	260	470	242	48	1020
H7389	55	88	46	8	197

Total V9000 Power FRU Installed = 5223

V9000 Systems Shipped Per Month (Average Runtime To Date at 90% UP)

	Jul	Aug	Sep	Oct	Nov	Dec	Jan	Feb	Mar	Apr
# Systems	8	12	29	13	16	65	11	14	21	8
Runtime	6156	5508	4860	4212	3564	2916	2268	1620	972	324

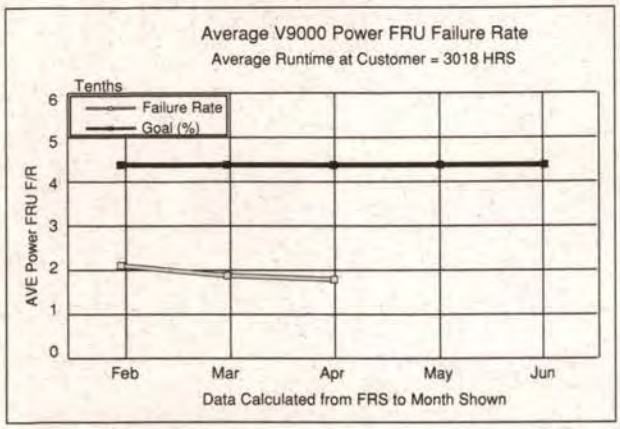
Weighted Average Runtime To Date = 3189 hours



Number of Power Units Failed/Returned/Confirmed

	Confirmed Fail	Upgrade/NTF
H7380	1	1
H7382	8	3
H7386	0	0
H7388	0	2
H7389	0	0

Customer Installation Failures (48 hr. process): 1
Customer Installation Goodness: 1/5223 = 99.98%



Power FRU Field Performance (Jul90-Apr91)

	Installed	Failed	Goodness	Failure Rate
H7380	2673	1	99.96%	.00037
H7382	1020	8	99.18%	.00784
H7386	313	0	100.00%	–
H7388	1020	0	100.00%	–
H7389	197	0	100.00%	–
Total	5223	9	99.82%	.00172

Goal for failure rate in first 1000 hrs. at customer site: *.0044/FRU*

Actual failure rate at customer site at an average of 3189 hrs.: *.0017/FRU*

Average FRU MTBF using: %GOOD = e = 1800K hrs.
Average FRU MTBF using point estimate = 1464K hrs.
80% Confidence LCL: 1851K x .7909 = 1464K hrs.

VAX 9000 Sales

"VAX 9000 gets DSTO thumbs up"...(Model 420). Computerworld Australia"
Account: Defense Science and Technology Organization, Adelaide Australia
Application: Signal Processing for Over the Horizon Radar (OTHR)

"British Gas soon to receive 2nd VAX 9000! (Other divisions have 3 on order)"
Account: British Gas, Transmission Division
Application: Valve Operation

"Hyundai Petrochemical intalls VAX 9000 Model 410"
Account: Hyundai Petrochemical Company, Seoul, Korea
Applications: Payroll, Purchasing, Accounting, Plant-wide IS

"Lee County installs VAX 9000 to manage explosive growth"
Account: Lee County, Fort Myers, Florida
Applications: Office Automation – All-In-1, Lotus 1-2-3

"Franklin Int'l Institute orders VAX 9000 Model 420"
Account: Franklin International Institute, Salt Lake City, Utah
Application: Order Processing

"Schlumberger installs 2nd VAX 9000 in the U.S."
Account: Schlumberger Well Services
Application: Geophysical applications including Seismic Analysis

"DCS&H Installas VAX 9000 Down Under! (Another on Order – both are Models 410's"
Account: Department of Community Services & Health, Canberra, Australia
Applications: All-In-1 and Oracle

"Roadway Package System, Inc. orders VAX 9000 Model 410 (previously all-IBM shop)"
Account: Roadway PackageSystem, Inc., Pittsburgh, Pennsylvania
Applications: General Business & Accounting

"CogniSeis Development chose the VAX 9000 over Convex and IBM"
Account: CogniSeis Development, Houston, Texas (SCMP)
Application: Disco – Seismic Data Processing

"VAX 9000 donated to MIT for design of America's Cup entry..."
Account: Massachusetts Institute of Technology, Cambridge, MA
Applications: Research, Aero and Fluid Dynamics, Oceanic Engineering, etc.

VAX Computer Aboard Discovery Shuttle

One of Digital's specially designed VAX computers was aboard the shuttle Discovery as part of the NASA experiment to test the use of commercial computer software technology in space. Orbiting the globe in the shuttle's cargo bay was a militarized version of the VAX 6000 series computer modified by Raytheon Co., a Digital licensee, to meet the rigors of space travel as part of NASA's Data Systems Experiment (DSE). The DSE project, a joint effort by Digital and NASA, supports a new initiative for the Space Shuttle system under the "Hitchhiker" program. The experiment involved a computer in space generating commands for a robotic system situated at the Goddard Space Flight Center in Greenbelt, Md.

The successful tests verified that standard VAX commercial architecture and standard commercial software, VMS and the ADA Language, can be used in the harsh environment of space. "This could mean a tremendous cost savings by eliminating the need for many custom written software programs," said Harvey Weiss, vice president Government Systems.

The Mil-Spec computer was produced by Raytheon's Equipment Division and delivered to NASA in October 1989. The computer is a Raytheon Model 860 VAX computer presently being delivered to the military, but modified to resist the rigors of space travel, such as the extreme forces of a rocket launch, the vacuum of space and the temperature extremes of the intended application.

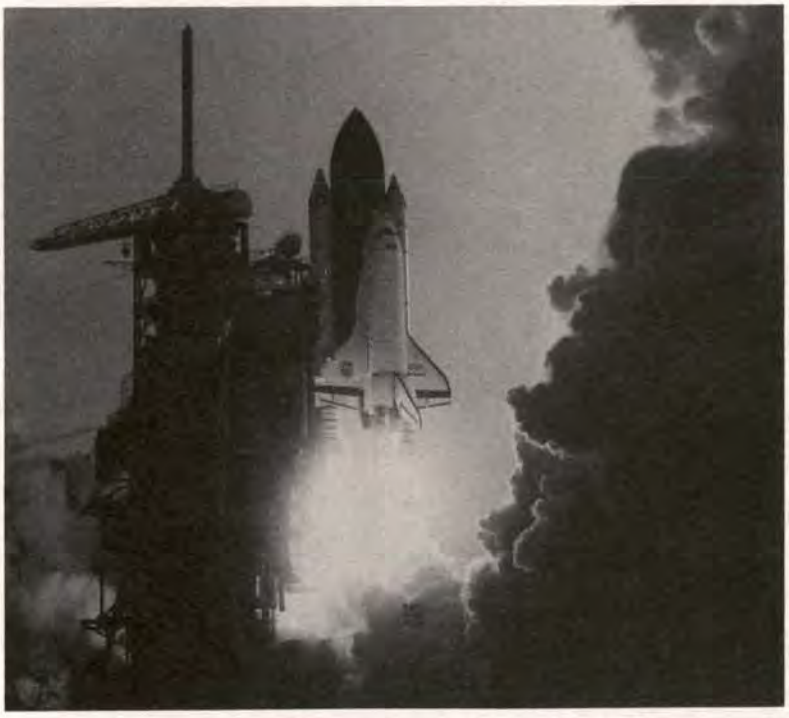
Controllers at Goddard Space Flight Center also report, based on Discovery's orbital velocity of 17,438 mph, that VMS is now the fastest commercially-available operating system.

Future NASA projects such as the Space Station Freedom and the Mission to Planet Earth Observation Satellites will use computer systems that can benefit from the availability of commercial standard parts and software. The Data Systems Experiment is one of the first steps to qualify the use of commercial computer architectures and software in space.

VAX to play a key role in August Shuttle mission.

VAX 9000 mainframes are vital to the most complex space investigation of the upper atmosphere ever attempted.

NASA's upper atmosphere research satellite mission will be launched by US Space Shuttle in August to study environmental changes affecting the earth's upper atmosphere.



Space Shuttle Discovery, April 28, 1991, Kennedy Space Ctr, Florida.

Scientists urgently want to know more about atmospheric changes caused by release of chlorofluorocarbons and nitrous oxide into the upper atmosphere.

Two VAX9000 systems - delivered and installed by CSO Science Systems and Applications - will receive and process data from UARS, measuring the chemical composition, temperature, winds and energy inputs of the atmosphere.

The vector-processing VAX 9000 systems can handle massive amounts of data and are compatible with other hardware and software installed at NASA. Plus, Digital was picked for our scientific processing capability and strengths in networking and multivendor systems integration.

Space VAX

With the advent and success of the initial flight of the "Space Vax," Digital has visibly demonstrated its commitment to invest its technological resources in the future. Although this first step into space was classified as an experiment, its successful results are potentially far reaching.

Digital is now confronted with the opportunity and challenge of becoming a formidable participant in our national space effort.

Eugene A. Cernan
Executive Consultant
Aerospace and Government

Eugene A. Cernan, Captain, USN (Ret.)

Professional Background

Digital Equipment Corporation

The Cernan Group, Inc., and The Cernan Corporation
1981 - Present, Chairman and President

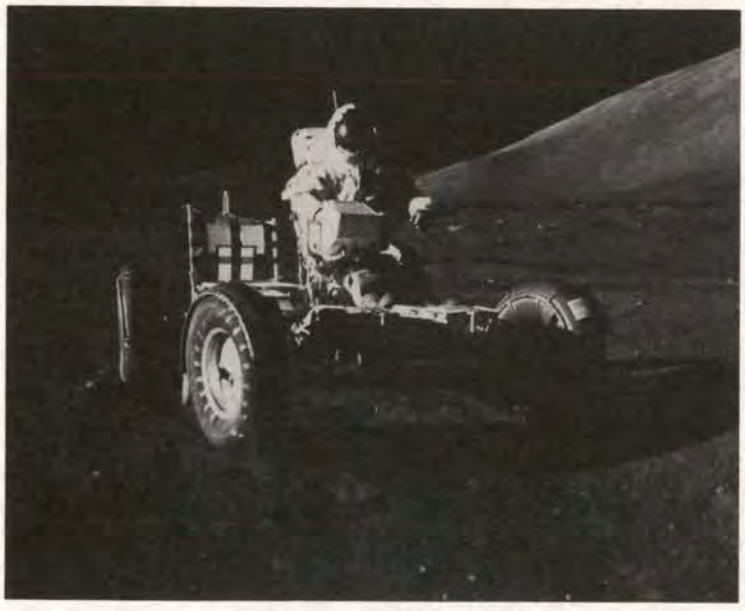
Coral Petroleum, Inc.
1976 - 1981, Executive Vice President International

United States Navy
1956 - 1976, Captain and NASA Astronaut

Captain Eugene A. Cernan joined Digital Equipment Corporation in 1987. He is Executive Consultant - Aerospace and Government for the Government Systems Group organization. Captain Cernan also acts as a Technical Consultant with the ABC Television network in support of ABC News and Special Events programming. He appears with regularity as a news commentator and covers space and related documentary activities.

NASA Career Highlights

NASA Group 3, October 1963
Gemini 9 pilot, June 1966
Gemini 12 back-up pilot
Apollo 7 back-up
Apollo 10 lunar module pilot, May 1969
Apollo 14 back-up commander
Apollo 17 commander, December 1972



Cernan checks out "stripped down" Rover prior to loadup.

VMS Documentation Wins Regional and International Awards

Margie Sherlock
Senior Technical Writer

At the annual Society for Technical Communications (STC) awards banquet in March, seven writers, editors, and artists from the VMS Documentation Group received awards of Excellence or Achievement.

Each year the STC sponsors the documentation competition, which honors writers, editors, and artists for outstanding work in their fields. Contestants enter their work in one of three competition categories: Publications, Art, or Electronic Documentation. Judges from the technical communication industry select winners in each category based on how well each entry communicates technical information. Judges consider many factors, including writing, editing, organization, graphics, and overall presentation.

The VMS books were selected during the STC's 1990/1991 Publications Competition, sponsored by the Boston and Northern New England chapters of the STC. Judges evaluated hundreds of documents submitted by large and small companies.

Winners in the top three categories (Distinguished, Excellence, Merit) automatically advance to the international competition. In addition to the regional competition awards, the Desktop-VMS User's Guide and A TP System Case Study won Excellence awards in the STC International Competition. The International Competition winners were announced during the annual STC Conference, which was held in New York City from April 14-17.

The STC is a nonprofit, international organization for professional communicators and technical communication educators, researchers, managers, and students. The VMS Documentation group has a firmly established tradition of winning STC awards and has won many regional and international awards in previous competitions.

The winning books and contributors are as follows:	
A TP System Case Study Viv Schupman, writer	Award of Excellence
Desktop-VMS User's Guide Margie Sherlock, writer Ken Wiggins, editor Natalie Pitula, artist	Award of Excellence
Desktop-VMS System Manager's Guide Kemlo Aki, writer Ken Wiggins, editor Natalie Pitula, artist	Award of Achievement
Desktop-VMS Installation Guide Kemlo Aki, writer Ken Wiggins, editor Natalie Pitula, artist	Award of Achievement
VMS DECwindows Transport Manual Kevin McDonough, writer Jill Angel, editor	Award of Achievement

VMS Documentation Group receives Excellence Award. Front row, left to right: Kemlo Aki, Jill Angel, Natalie Pitula, and Margie Sherlock. Back row, left to right: Viv Schupmann, Ken Wiggins, and Kevin McDonough.

VMS Engineering Europe: The U.K. Investment

Catherine E. Foley
VMS Engineering, X/Open Program Mgr.

VMS Development in Europe

In the fall of 1987, VMS engineering announced its plans to have an Engineering presence in Europe. A significant part of those plans has included supporting major VMS engineering investments in the U.K. Since its founding, the VMS engineering investment in Europe has expanded considerably, both in the U.K. as well as in a second country and location — Varese, Italy. Initially the U.K. effort was launched, managed, and staffed by Bill Laing, who later was joined by Bob Landau and Jim Johnson. The group has since grown to a team of 39 and is managed by Mike Cassily. In addition to Mike, the team includes development engineers, a quality engineering team, a product manager, and 5 technical writers.

The group was located first in Basingstoke and then moved to Newbury, which is situated in the Thames Valley of England, 60 miles west of London. When longer range planning was completed, it was decided to move the group to Scotland. Currently, the group is distributed between Newbury and the new facility, located in Livingston, Scotland. The relocation of the group is expected to be complete in August, 1991. The Livingston facility is located in central Scotland, about 12 miles outside of Edinburgh and about 45 miles from Digital's Ayr manufacturing facility, and 9 miles from Digital's South Queensferry semiconductor facility.

Initiating VMS Development in the U.K.

The initial focus of the VMS/U.K. development group in Basingstoke was to provide distributed and reliable application services in the base operating system. The objective was to enable customers to design and build highly available distributed applications.

A significant milestone for development in the U.K. was achieved when VMS Version 5.4 shipped the first version of integrated distributed transaction management services (DECdtm) in the Fall of 1990. The DECdtm services employ a two-phase commit protocol that enables application developers to build distributed applications that can survive individual CPU and mass storage subsystem failures. As a key base system function, these services are now supported by a suite products, including VAX Rdb/VMS, VAX SQL, VAX DBMS, VAX ACMS, VAX RMS Journaling, and VAX Rally.

Providing the Next "Unfair Advantage" on VMS for Digital

In early 1990 the focus for VMS engineering in the U.K. expanded beyond supporting distributed and reliable application services to include porting and enhancing the VMS file system for strategic new platforms. Under the management of Mike Cassily and technical direction of Bill Laing, the VMS/U.K. engineering group has launched several key projects in the area of file I/O and data management to support strategic new platforms.

The importance of the VMS Engineering/U.K. initiatives and the anticipated edge that they will offer Digital have been understood and well received by many, including several senior VMS specialists, who recently attended the VMS Partners Meeting in Nashua, NH. These senior field specialists have dubbed these initiatives, launched by the U.K., as the next "unfair advantage" for Digital and VMS. We now look to this multi- disciplined committed team, with a proven track record providing distributed TP services, to help VMS provide that next "unfair advantage."

Digital's new facility located in Livingston, Scotland.

VMS DECWindows Motif: Supporting Open Systems Standards

Catherine E. Foley, VMS Engineering
Janis Horn, VMS Product Management

Support for the Open Software Foundation's Motif user interface has been added to DECwindows. DECwindows is now available as a new VMS layered product, referred to as VMS DECwindows Motif Version 1.0. As a standard Graphical User Interface (GUI), Motif is a combination of leading interface technologies developed jointly by the Open Software Foundation, Digital, Hewlett-Packard, and Microsoft. When OSF requested graphical user interface (GUI) technologies, several vendors responded, including Digital - who responded with our DECwindows XUI. It was selected as the base GUI technology and now represents about 90-95% of OSF/Motif.

In the past, DECwindows functionality was delivered as part of the base VMS operating system. Separating this functionality from VMS allows for greater flexibility in delivery of the features to customers and minimizes the burden and cost of royalty encumbrances. This new product is currently in field test and is expected to ship to customers in Q1 FY92. To support customer migration, current VMS service customers will be allowed, for a limited time, to receive VMS DECwindows Motif V1.0 media and licenses free of charge.

This new layered product which provides base windowing technology is based on industry-standard OSF/Motif™ Version 1.1.1 and MIT X11 Release 4. In the first offering, the Motif user interface is incorporated as the design center for DECwindows applications. Added-value development and productivity tools are available in the form of separate DECwindows packages and layered products.

Motif's standard API is based on the DECwindow's X User Interface (XUI), with additional features contributed by HP. Although the Motif API replaces the DECwindows API, the traditional DECwindows API will continue to be maintained and supported by Digital within the VMS DECwindows Motif layered product. XUI was previously delivered in DECwindows with base VMS. Because both Motif and XUI are based on the X Window System, applications written to either toolkit continue to run, regardless of which environment the user selects.

Version 1.0 Highlights

Some highlights of Version 1.0 include:

- Motif language bindings: Bindings are provided for for Ada, C, FORTRAN, and Pascal.
- Porting tools for XUI applications: Version 1.0 includes XUI-to-Motif porting tools for programmers porting XUI applications to Motif. These tools are for programs written in the C language and are helpful when converting XUI UIL sources to Motif Presentation Description Language.
- Backing store support in the DECwindows server: Backing store support enables the server to save the contents of an occluded window and to automatically restore the contents of that window when that window is no longer occluded. This capability offers performance benefits for those applications that generate windows with complicated graphics that may take considerable time to redraw.
- Enhanced imaging capabilities: X Image Extension (XIE) is a new feature that provides X-server based image rendition and display services. This allows interaction directly on the server, not remotely on the host system. XIE also allows for transmission of compressed images and for applications to utilize image hardware on the server in the future.

- LinkWorks™ multimedia information linking and navigation support: As a new technology, Link-Works allows users to link data objects from one application to data objects in another application. This capability is similar to "hyper appli-cation" features offered by other vendors. The first four DECwindows out-of-the-box applications to support LinkWorks are Bookreader, Calendar, Cardfiler, and Mail.
- New DECwindows Motif Help: The new DECwindows Motif Help System allows users to display online help files using Bookreader from their applications. Users of the system can make use of referential links, graphics and complex formatting in their help files. DECwindows Motif Help is provided as programming support only; that means DECwindows out-of-the-box applications do not utilize the new DECwindows Motif Help in the first release of VMS DECwindows Motif.
- Internationalization support: All out-of-the-box applications have moved text strings into User Interface Language (UIL) files and can now be translated for countries that use the ISO Latin-1 Character Set.
- Interoperability enhancements: Support for font alias files and additional fixed-width fonts from the MIT X11 distribution enables a wider variety of third-party applications to work with DECwindows. Font fallback support enables DECwindows applications to display on a wide variety of third-party workstations and Xterminals.

Product Packaging Notes

For the short-term, the VMS DECwindows Motif layered product kit will include both client (Version 3.0 level) and device-specific support (Version 3.0 level) for its first release. Concurrently, VMS will begin to ship the new DECwindows device support (V3.0 level), as well as ship the old XUI DECwindows client files (V2.1 level) to all customers for at least one more full VMS "generally available" release. This duplicate shipment of the device support (at the V3.0 level) will continue until VMS and the new VMS DECwindows Motif layered product are synchronized.

In the long term, it is intended that DECwindows device- specific support will remain with the VMS kit and license only.

All other DECwindows files for application support will be included solely in the new VMS DECwindows Motif layered product kit and license.

A Competitive Solution for End Users and Application Developers

Buying Motif from Digital has advantages:

- Digital created it. Our Motif is the cleanest and most bug free in the industry.
- Digital offers added value with a number of advanced and powerful Motif compliant widgets (tools).
- From DEC VUIT to the Motif tool kit, we offer the most ideal Motif application development environment.
- We have the complete story:
  - An offering of standards that no other vendor can match
  - Integration of other hardware and software platforms
  - Cross-platform graphical user interface
  - Unparalleled communication capabilities
  - Scalability: unlimited system growth.

Back To The Future – VMS Partners Program

Ann Grecoe
VMS Partners Program Manager

"When Ken Olsen decided to come to the VMS Partners meeting in April," says Bill Demmer, "I was just as pleased as everyone else. I was surprised by the Partners' energy and enthusiasm as they peppered Ken with questions for over an hour. I was proud of them all."

Sharing Bill's pride were the the 79 Partners who listened as their spokesperson, VMS Partner Joe Bates from Burlington, MA, outlined for Ken what the group had agreed upon were the most significant challenges facing VAX VMS.

Joe addressed four topics - the product, the selling process, the marketing, and the vision. He asked that VMS and ULTRIX be more clearly differentiated; pointed to the amount of business being lost because of the price differential between RISC and CISC workstations; emphasized the importance of making quality the company's first goal; and asked that Ken take the lead in articulating a vision that could unite the company again - just as the "One Company, One Architecture, One Operating System" theme had done in the 1980's.

Ken was impressed and asked Joe to make the same presentation again at the Executive Committee meeting the next morning. That meeting closed with a promise that the Partners' concerns would be addressed and that members of the Executive Committee would return for the groups next meeting in the Fall.

Later that day, there was additional follow up. Jack Smith, Bill Strecker, and Bill Demmer joined the Partners for an evening session. Jack thanked them for their input, reminding them that they were the "eyes and ears" of the company and said how much their unfiltered input was valued. Bill Strecker and Bill Demmer then joined a group of 15 Partners for dinner, exploring further the issues the Partners had raised.

(left to right) Phil Auberg, Manager of VMS Marketing welcoming Ken Olsen to the VMS Partners Meeting.

Helping One Another to Help Our Customers

The Partners' exchange with Ken and other members of the Executive Committee typifies the mission of the VMS Partners Program. Started by VMS Marketing in 1988, the Program identifies the key technical experts who devote most of their time promoting and supporting VMS in the field. Its primary aim is to make sure that there is an active, ongoing dialogue between the field and VMS Marketing, Engineering and Product Management.

For the 125 Senior Sales Support people now involved, the VMS Partners Program provides a direct link to the people in engineering, marketing and product management who make the decisions and understand the technical issues.

"When I need an answer for a customer," says Patti Thompson, VMS Partner from Houston, TX, "I know who to call, and I know that my call will be returned. That frees an incredible amount of time so I can do the other parts of my job — working closely with sales and other support personnel to deliver in-depth product information, giving non-disclosure presentations and helping to design complex system configurations."

Gregg Scott, VMS Partner from Bloomington, MN, echoes Patti's comments and points to another invaluable feature of the Program.

"Every week", says Greg," we get two mailings from the Program Office. The News Update keeps us up to speed on VMS software, layered products, and developments in the ULTRIX World. The Partners Update keeps me abreast of the release strategy, phase reviews, and other current information on the products in development. With that kind of support, along with the Partners' Notesfile, I often don't have to pick up the phone at all."

The Partners are also active participants in the development of the VMS Product Information Disclosure (PID). Because the emphasis is now on current customer concerns - what customers really want to know instead of what we think they might like to hear - the Partners can use PIDs much more effectively.

Keeping Current with The Competition

For VMS Marketing, Product Management, and Engineering, the Partners provide invaluable input that cannot be gained by any other means.

"The Partners' detailed monthly reports go far beyond a simple list of wins and losses" say VMS Marketing Manager Phil Auberg. "It's required reading for all of us. When we win, we know why and precisely how we solved the customer's problem. When we lose, the Partners give us invaluable insight into the competition's strategy. If there is a hot issue, we can jump right on it."

The Partners' participation, of course, is not limited just to the preparation of monthly reports. For example, John Hildebrand from Dallas, TX and Bryan Beske, from Columbus, OH, were key participants in what the DCVN broadcast VMS Marketing did in October 1990 as part of the kick-off for the Open VMS Campaign.

Bill Demmer speaks at the VMS Partners Meeting

"John and Bryan answered the questions customers called in with a lot of credibility," says Rich Kittle, Open VMS Marketing Manager. "They deal with customers every day, speak their language, and are often a lot quicker than we are to get to the question behind the question that's actually being asked."

In fact, the VMS Partners have become such a visible entity within the corporation that marketing and engineering groups outside VMS come to them for input on their hardware and software products. Like VMS Marketing, they value the input the Partners can give as they set new product directions or respond to tactical moves from Digital's competitors.

VMS Partners Biannual Meetings

Just as other groups ask the Partners for input, it is no longer unusual to see engineering and marketing managers from outside the VMS community in attendance at the formal VMS Partners Meetings which are held twice yearly, usually in the Nashua area.

These week long events include presentations from Corporate about VAX VMS Marketing directions, VMS Marketing and Engineering initiatives, and specifics about new hardware and software products. Speakers are also invited from groups like ULTRIX and NAS to keep the Partners updated on the Corporation's overall messages and directions. These meetings provide an opportunity for the Partners to share pertinent information and experiences from their respective areas so that all may benefit from knowledge gained by individual or team wins and the relevant issues between the U.S., Europe and GIA.

The Partners in turn, give feedback to VMS Marketing Product Management and Engineering. In the April meeting, for example, the Partners reported high customer interest for VMS to continue strengthening its system management capabilities and to clearly articulate the release strategy.

Poised For Growth

As the program enters its fourth year, there are plans to work for greater representation from Europe and GIA. Also under consideration is the suggestion that a Leadership Council be formed so that Partners from the different geographies will have one spokesperson to represent them.

Far more important than whether a Council comes together before the next worldwide meeting, however, is the hope that unites all the Partners. That's the expectation that when Ken returns in the Fall, the group will be able to report substantial progress toward the common goal of keeping VAX VMS the company's flagship product.

Resources:

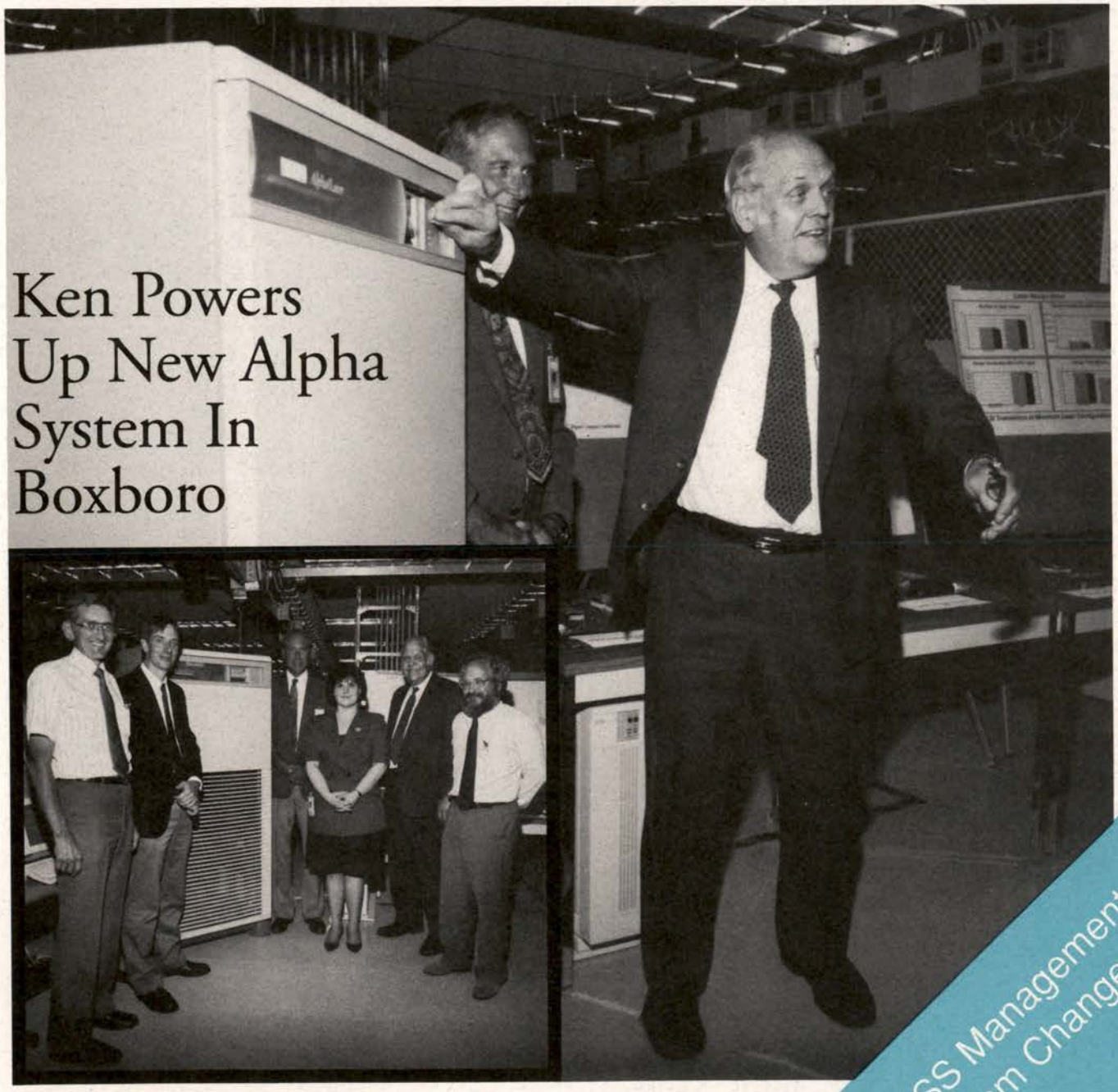
Program Manager – Ann Grecoe
DTN 264-3557
VMSMKT::VMS_PARTNER
Restricted Notes File
Release Strategy
New Products
Phase Review
News Update
Partner Update
Monthly Report
Customer Issues
Wins
Losses
Competitive
Hot Topics

digital

S168BC1-CC:Y8P TT *
M 341 100 MRC1-2/S43
TIMOTHE LITT
DIGITAL EQUIPMENT CORPORATION
200 FOREST ST
MARLBORO MA 01752-3011

FOREFRONT

VAX VMS Systems and Servers
Systems for the '90s
Q2 FY92



Ken Powers Up New Alpha System In Boxboro

VSS Management Team Changes

FOREFRONT

A VAX VMS Systems and Servers Quarterly Publication.

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Contents

Newest VAX System, NEPTUNE

Lawrence Chisvin *Hardware Principal Engineer, SEG/AFL*
Rebecca L. Stamm *Hardware Principal Engineer, SEG/AFL*
Masood Heydari *VAX 6000-600 Program Manager, DCSS*

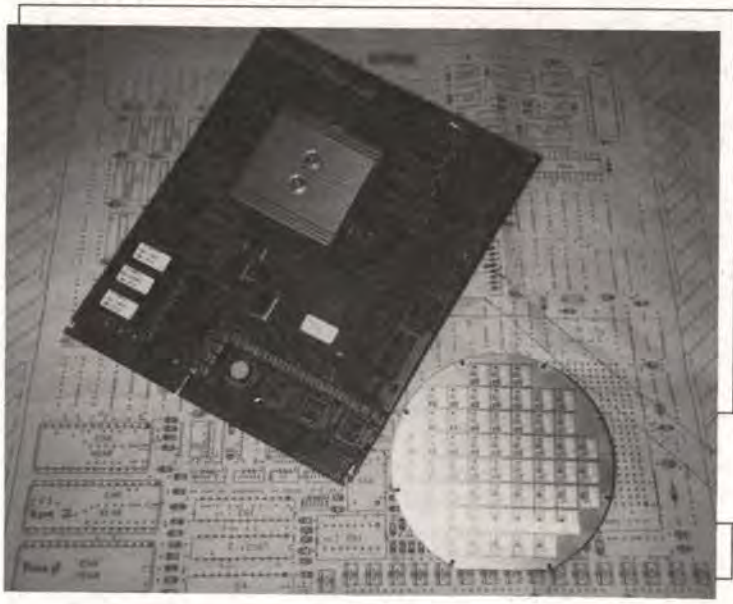
The newest XMI2-based VAX system, the VAX 6000 Model 600 (NEPTUNE), provides more than an order of magnitude performance improvement over the original VAX 6000 (CALYPSO) system in fewer than four years. The CALYPSO series started with the Model 200 (2.8 VUPs) in May 1988. The XNP processor module, which is the major new component in the NEPTUNE system, continues the progress of the VAX 6000 series of products. It supports the same modular expansion ability, and features the powerful symmetric multiprocessing (SMP) capability of all VAX 6000 products.

There are several major reasons for this rapid growth. The implementation of the VAX architecture using full custom CMOS microprocessors, designed and manufactured in Hudson, allows DEC to efficiently exploit the progress of the CMOS technology curve for increased speed and density. Furthermore, the XMI platform was designed from the start to be quickly and easily upgraded. The new NEPTUNE system uses the same I/O and memory adapters that were used by previous models of the VAX 6000 series. This important characteristic of the CALYPSO computer family allows the system to be upgraded simply and gradually. It also minimizes development time, since only a single module needs to be designed with each new microprocessor.

The XNP processor, the engine that propels the new VAX 6000 Model 600, is a single-module XMI2-based implementation of the VAX architecture. The module contains the NVAX CPU chip, an XMI2 bus interface/system support function ASIC chip (NEXMI), a handful of off-the-shelf system support components (PROM, local RAM, UART, time-of-year clock, input/output ports), and the memory necessary to support a 2Mb write-back backup cache (tag and data RAMs). Both the module and the two major VLSI components were designed and verified in Hudson's AFL (Architecturally Focused Logic) group.

The heart of the NEPTUNE system is the NVAX CPU chip. It is the largest and most highly-integrated VAX chip ever designed. Fabricated in Hudson's 0.75 micron CMOS-4 process, it contains 1.3 million transistors on a die that measures 574 mil by 636 mil (a mil is one thousandth of an inch). The die is packaged in a 339 pin ceramic pin grid array (CPGA). Its performance is achieved through architectural innovations, the use of advanced design and layout tools, and the speed and density improvements made possible by state-of-the-art CMOS fabrication techniques.

The single NVAX die is partitioned into five major subsections, called "boxes." Each box is responsible for a number of carefully defined functions, and the coordinated operation of all the boxes support the code and architectural features that define a VAX. The NVAX box functions include a VAX instruction prefetch and parse unit (Ibox), an execution unit (Ebox), a memory management unit (Mbox), a floating point co-processor (Fbox), and a control unit for the off-chip write-back backup cache and NVAX pin bus interface (Cbox). The die also contains a 2KB virtual instruction cache (VIC), an 8KB primary instruction/data write-through cache (Pcache), a translation buffer for fast virtual to physical address mapping, and the logic necessary for chip clocking, reset, and testability.



XNP Module and NVAX Wafer

The backup cache controller allows a choice of four sizes: 128 kilobytes, 256 kilobytes, 512 kilobytes, or 2 Megabytes. It allows for tag RAM access times ranging from 8ns to 35ns, and data RAM access times ranging from 8ns to 50ns. This configurability allows the NVAX CPU to be used in a variety of system platforms; and it let the NEPTUNE system designers defer a final decision on the backup cache size and speed until actual system benchmark tests had been run. For the optimum price/performance tradeoff, a 2 Megabyte cache was chosen, using 20ns data RAMs and 15ns tag RAMs.

The NVAX design makes use of both traditional pipeline techniques (called micro-pipelining) within each box, and a more advanced pipelining method (called macro-pipelining) among the boxes. Each box runs semi-autonomously (though under control of a synchronous clock), and information is shared between the boxes through inter-box control signals and queues. This internal structure regulates the flow of execution among the NVAX boxes, keeping each box as busy as possible. Another architectural feature of the NVAX CPU is a sophisticated branch prediction mechanism. Based upon the previous history of branches taken for a section of code, this logic makes an educated "guess" about which fork will be taken on a branch instruction, and starts to prefetch based upon this decision.

One feature of the NVAX chip which has proven extremely useful during debug and system test is the patchable control store, which provides the ability to modify the microcode in a running system. This capability has been used extensively to debug and correct chip problems. Of the ten first pass NVAX bugs that affected system operation, seven were either corrected or worked around by altering the microcode using the patchable control store.

Planning for the NVAX project began with one person in July 1987. Performance modeling was initiated in February 1988, and schematic design started in July of 1989. Layout and final verification were completed, and the chip was taped out, on November 30, 1990. Tape out had originally been scheduled for December 1990, and the system FRS date was targeted for June of 1992. An FRS in November of 1991 places the actual date seven months earlier than originally planned.

The team responsible for the NVAX chip consisted of 29 CMOS circuit/logic designers, 3 chip architects, 25 CMOS layout designers, 10 verification engineers, and one manager, for a total of 68 people. Each NVAX box (not including the RAM arrays) is roughly equivalent in transistor count to a Microvax chip (125K transistors), and was assigned a box leader and a design team. The final design included 595 pages of schematics.

Almost half of the 1.3 million transistors on the chip are in the primary data/instruction cache (Pcache) array, which consists of 620,000 devices. This highly compact RAM array occupies 13% of the chip area. The extreme density of the Pcache array makes it more susceptible to manufacturing defects, so the capability to repair the array was designed into the chip. There are 128 rows in the Pcache, and as many as 2 rows in each block of 16 rows can be repaired. If more than 2 rows in a block of 16 are defective, the cache is beyond repair. The RAM repair is performed by blowing selected fuses using a laser beam, based upon initial testing of the chip after fabrication. This process has been highly successful so far, and has allowed shipment of many die that would otherwise have been non-functional due to Pcache failure.

Concurrent with the design of the NVAX chip, SCO's Advanced Semiconductor Development Group (ASD) was developing Hudson's new .75 micron CMOS-4 process. The NVAX was the first planned production chip to be fabricated using CMOS-4, and the creators of the process worked closely with the chip designers to ensure that the process would be ready in time and support the requirements of the new high-performance CPU.

NVAX was designed with an even more extensive CAD tool arsenal than previous chips. The Hudson CAD group, which had an excellent working relationship with the NVAX team, provided the suite of CAD tools that were a major component in the eventual success of the chip. OCCAM, a new tool which synthesizes schematics from a behavioral model, was used very successfully in some areas of the chip. CLEO and FACS, automatic layout tools, were used to quickly lay out sections of the control logic, and a new tool called GLOW aided in planning the chip routing and floor plan. CZAR, an automatic circuit sizer, was used for the first time. Another new tool, NTV (New Timing Verifier), is capable of analyzing circuitry for critical paths, and together with SPICE (an analog circuit simulator) resulted in a chip that runs at its predicted speed in the system. NTV was used in each box, then on the whole chip, to identify critical paths. On-chip clock and signal interconnect RC delays and electromigration problems were analyzed automatically for the first time using a tool called WAWOTH. Layout netlists were extracted heirarchically by a new tool called HILEX, and interconnect parasitic capacitance were obtained by a new 3-dimensional extraction tool called CUP. HILEX and CUP took advantage of multiprocessing to significantly reduce elapsed run times.

The NVAX functional verification team used a detailed DECSIM behavioral model to test the accuracy of the design. In addition to running AXE and MAX (architectural exercisers used on previous projects), NVAX-specific assembly language exercisers were created using a new, Hudson-created pseudo-random code generation tool called SEGUE. These exercisers were run on pseudo-randomly generated configurations in conjunction with various "demons" (pseudo-randomly selected design provokers built into the model). They were run on the behavioral model almost continuously for six months. This verification was performed on several VAX clusters, as well as on the SPRITE behavioral simulation accelerator (developed by the SEG CAD group). In addition to these pseudo-random tests, 140 NVAX-specific focused tests were created and run on the behavioral model. Another locally-created tool, SAVES, provided test coverage analysis by post-processing the simulation trace files.

CHANGO, an AFL-developed logic simulator that provides performance comparable to behavioral simulation, allowed far more schematic-based model simulation to be performed than on past projects. Box-level CHANGO simulations, driven and compared on-the-fly with behavioral simulations, detected many design inconsistencies. The box-level verification worked well, and only one logic bug was found when the full-chip CHANGO model was finally created. Tens of thousands of AXE and MAX cases were run on this model, and the NVAX-specific exercisers were run continuously for two months before tape out. Probably the most significant accomplishment using the CHANGO model was the simulation of the VMS boot process (about 25 million CPU cycles) on a model derived from the schematics: something that had never been done before!

Altogether, about 1 billion CPU cycles were simulated on the behavioral model, and about 75 million cycles were run on the schematic model. A total of 348 functional bugs were detected and logged before tape out. The result of the thorough pre-tape out verification effort is that only 15 bugs existed in the first pass of NVAX, and only 10 of those were

evident in system operation. Furthermore, no interruption in the system test and debug effort was caused by any of the problems.

The efforts of the NVAX chip team, the CAD group, ASD, and Hudson manufacturing resulted in functional parts from the first released NVAX lot. This was an unprecedented event. The booting of VMS on a part from the first lot took place over two whirlwind weeks. Testing started on the first wafer on Wednesday, February 20, and by Monday, February 25 the first NVAX chip had been packaged and installed in a system. On February 27 the VMS banner was reached, and the system completed VMS boot on March 8. This impressive coordinated effort was the result of hard work and tremendous cooperation between the VMS group in Spitbrook, the systems engineers in Boxboro, and the chip, process, and module teams in Hudson. A combination of innovative design, verification, layout and checking tools, coupled with special chip features (such as the patchable control store) and careful directed effort by the participants, enabled the first pass version of the NVAX chip to go to customer field test, a remarkable feat for a CPU chip of any size.

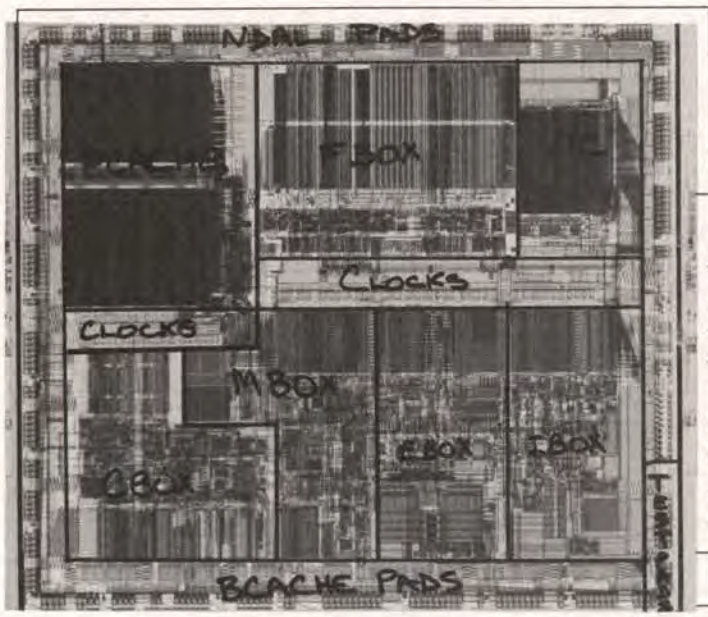
The NVAX CPU is one of two dense, complex integrated circuits that form the basis of the XNP processor. The other major chip is the NEXMI, which performs several basic functions. Firstly, it integrates the NVAX CPU into the subsystems that form the XMI2-based VAX 6000 platform. Secondly, it supplies the control logic for a core of system support functions necessary in a working VAX computer.

The NVAX CPU pin bus is not directly compatible with the XMI2. The NEXMI translates commands between the NVAX and the XMI2, performing a crucial multiprocessor cache coherence function in that process. Since the backup cache on the XNP processor module is a write-back cache, a processor in the NEPTUNE system often contains the only accurate version of a memory location. This makes the cache coherence function far more complex, and forces a close relationship between the NVAX CPU and the NEXMI system interface chip. The NEXMI also routes data between the CPU and the memory/peripheral controllers, and aids in module arbitration where necessary.

In addition to its important bus interface function, the NEXMI also provides the logic to implement a set of core system support functions. Many of the functions are provided by off-the-shelf components, and in those situations the NEXMI acts as a controller. Other functions are provided by the NEXMI chip itself. Some significant system support functions that the NEXMI either provides or coordinates include PROM (for power-up initialization, the VAX console facility, and diagnostic tests), EEPROM (for configuration and module-specific information), a local scratch-pad RAM, a console UART, a time-of-year clock, a programmable interval timer, and a set of programmable input and output ports.

The NEXMI chip is an ASIC device, implemented in Hudson's 1 micron CMOS-3 process using a standard cell design approach. Packaged in a 339 pin ceramic pin grid array, it houses about 250,000 transistors on a die that is approximately half an inch on a side. This makes the NEXMI the largest standard cell (in both physical size and transistor count) designed within DEC. Detailed logic and timing simulation was used throughout the design and verification phases of the project to minimize the design time, and to provide highly functional first pass prototypes. The methodology was successful. In that first pass NEXMI parts were able to be used for all system debug, and were eventually used for field test.

The ORCHID design management system was used to coordinate the different components of the logical and physical design process, and to provide feedback about the design data base that was used in func-



First 0.75 um, Local Interconnect, Tungsten Plug, 3 Level Metal VLSI Product Chip with 1.3 Million Transistors. Advanced Semiconductor Development Group, February 1991.

tional, timing, and physical integrity checking. The ATLAS semi-custom physical design tool suite was used to lay out most of the subchips that formed the NEXMI design, and to aid in the important physical floor planning of the chip. Although the NEXMI was designed primarily using a standard cell building block technique, several sections received full-custom treatment for reasons of density or critical timing requirements. This combination resulted in a dense yet reliable and high-yielding fabricated integrated circuit.

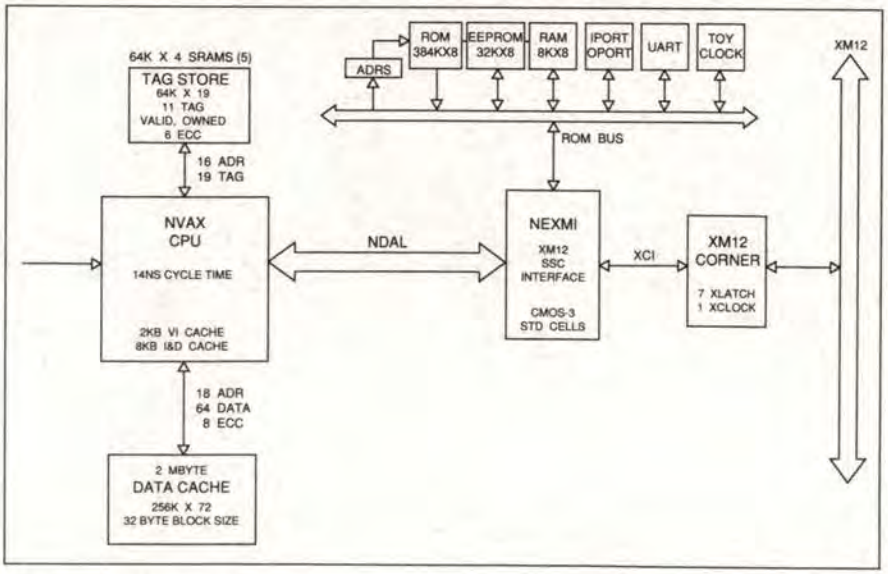
The functional verification of NEXMI was initially performed on a behavioral model, and as the structural, schematic-based design segments became available they were integrated into the environment. Both focused and pseudo-random testing was performed. To allow for simpler pattern generation, and to provide automatic checking of NDAL (NVAX pin bus) and XMI transactions, various behavioral transactor models were integrated into the NEXMI simulation environment. A bus monitor model which checked for consistency between transactions appearing on the three NEXMI buses (NDAL, ROM, and XMI) was also created. This greatly improved the automatic testing of the three bus interfaces on the NEXMI chip.

Use of TEMPEST, a tool jointly developed by the AFL MTV group and the Test Engineering group, allowed the verification test simulation traces to be quickly translated into ATE chip test vectors. These test vectors are used as an early check of the chip's functional ability. TEMPEST has the ability to handle complex tester timing and control, and to generate DECSIM patterns that can be debugged on a simulation model before being used on a fabricated chip. It allowed both the NEXMI and NVAX first prototype wafers and packaged parts to be tested with very few problems.

During the design of the XNP processor, module-level signal integrity and transmission line propagation delay were major concerns. Design experience and detailed simulation techniques were used to ensure that the module would support the performance capability of the individual components. Measurements have been taken on the final hardware product using high-speed digital oscilloscopes, and they show that this module performance goal was achieved.

The people involved in the module design brought with them a wealth of experience in what principles should be followed in order to minimize the possibility of poor signal integrity. This included component placement and etch considerations. Certain geometric routing patterns have been shown to be best for transmission line signal integrity and performance, and each signal etch was scrutinized with these principles in mind. As well, an exhaustive analysis was performed which identified which module components had common signals, and the component placement decisions were based on minimizing critical signal lengths. As one further example of the type of trade-offs that were made, components were mounted on both sides of the module to minimize signal lengths.

After the component placement and etch routing rules-of-thumb and design principles showed where everything should go, a significant effort was launched to further refine and test what the results would be. Since this was all done before any hardware had been fabricated, SPICE simulation was performed on detailed models of the module etch and components. This simulation showed places where changes had to be made in order to achieve the final goal. All this effort resulted in a module that supports the class of performance provided by the VAX 6000 Model 600.



XNP Block Diagram.

Another important goal of the module design team was the coordination of the engineering and manufacturing communities in order to reduce the cost of the bare circuit etch board (PWB), the module assembly, and the test process. The module was designed in accordance with the existing DEC standards where appropriate, but the module team went beyond that when some improvement was identified. One notable improvement that is not covered in the DEC module standard is the use of the Wenesco soldering process. Much of the board was designed using surface mounted components, but there were enough through-hole components so that it was advantageous to address their special needs. The Wenesco process, which is basically a localized wave solder fixture, allows all the through-hole parts to be soldered to the module simultaneously. In the past, each through-hole component was soldered to the module individually and by hand. New module design guidelines were necessary to support the Wenesco fixture, and the module design and manufacturing groups worked together to create the rules. Many other issues were discussed and resolved through the use of a Design for Manufacturability (DFM) log that was maintained by the manufacturing producibility group.

An important facet of module manufacturing is the initial testing of the assembled module, since the cost of finding a defect increases dramatically at each stage of system integration. As such, a considerable module design emphasis was placed on Design for Testability (DFT). JTAG boundary scan was designed into both of the VLSI devices (NVAX and NEXMI), simplifying the in-circuit testing of the XNP module. In the past, test patterns from the integrated circuit tester were translated into a special Teradyne format to be used on the L280 module tester. This was a very time consuming activity. JTAG scan testing allows the L280 to do component interconnect testing directly with a simpler set of test patterns. Boundary Scan Interconnect (BSI) software provides the bridge from the JTAG information in the VLS module layout database to L280 test patterns. The interconnect of the JTAG signals on the module enables the VLSI devices to be tested together or independently.

Another test feature that has seen a significant amount of use is the parallel port. Both VLSI devices have this feature, which allows the user to view the internal state of the chip during normal functional operation. This feature was invaluable during the module debug phase of the project, providing the troubleshooting team with insight into the detailed and largely invisible operation of the highly integrated NVAX and NEXMI chips. The rapid debug time that has characterized the project from first power-on was made possible by the parallel test port.

The delivery of working hardware and a functional version of VMS allowed the next phase of the NEPTUNE project to begin: a massive test and integration effort necessary to ensure that the new system achieved the quality expected of a VAX. The System Integration team is chartered with the responsibility for testing the interaction of the system's hardware and software components. This includes managing the qualification process, performing Design Verification Testing (DVT), coordinating the full system testing, monitoring the progress of the Reliability Confidence Testing (RCT), organizing the field test effort, coordinating the system characterization, and performing the system performance evaluation.

Comprehensive testing of a new system such as the VAX 6000 Model 600 is performed using both directed and random tests. Directed tests are well defined, carefully bounded tests that are designed to check specific hardware or software features. These might test new features that the NEPTUNE system provides, or they might ensure that previously supported features also work as expected on the new system. The directed tests, though necessary, cannot possibly exercise all the aspects of a system as complex as the VAX 6000. Random testing is required to push the system into as many different states as possible, and to do so as quickly as possible.

Faced with the difficult, error-prone, and potentially time-consuming task of random system exercising, the VAX 6000 Model 400 (RIGEL) System Integration Group developed a pseudo-random test package called the System Integration Test Package (SITP). This test suite, used very successfully on the RIGEL project, has since been used on the Model 500 (MARIAH) and was naturally extended for use on the new NEPTUNE system. Each system team has added to the original SITP, enhancing the test suite to address the needs of the particular project. Of course, the SITP package represents only one of many workloads that were used to qualify the Model 600.

With any computing system as new and innovative as the NEPTUNE, a significant number of issues are going to arise during the months of detailed testing. Although the system integration effort was coordinated from Boxborough, much of the testing and characterization was going on at other selected sites. Each issue that was found at any of the sites had to be carefully analyzed and appropriately resolved. Many of these issues were simply informational, and provided a better understanding of the new XNP-based system. Some were legitimate problems, and these had to be dispatched and corrected quickly.

All problems found during system integration were logged and tracked through a VAX Notes conference called the Neptune Prototype Problem Reports (NPPR). Each problem was assigned to a member of the System Integration Team, and that person was then responsible for following the problem to closure. This usually involved working with various groups, keeping track of the progress of the issue, and reporting back when the issue had been resolved. Regular NPPR meetings were attended by representatives of the system integration subgroups, and each unresolved NPPR was discussed to determine what steps had to be taken to close it.

The major reason for the success of the NEPTUNE project is the coordinated effort that took place between all the groups involved in its design, implementation, and verification. From the very start of the program a number of groups, spread out over many sites and including several different organizations within the company, worked in a focused manner to identify and resolve each issue. From the early stages of the chip and module design tasks until the final system integration effort, people worked together in an organized and constructive fashion to create the world-class performance and quality of the VAX 6000 Model 600.

Neptune Program Team.

Alpha System Powers On

Dick Willett

Digital's first Alpha system came to life September 5th in Boxborough when Ken Olsen turned the ceremonial key to power on Laser/Ruby.

The event marked the culmination of two years of engineering effort on the part of Hudson Semiconductor Engineering, Boxborough Systems Engineering and the VMS Engineering teams. It also marks the start of the efforts leading up to announcement and first revenue shipment of Digital's RISC VAX.

Ken Olsen, Bill Demmer, VSS Engineering VP, Bob Supnik, Alpha Program Mngr, Don Harbert, VMS Engineering Manager and Pauline Nist, Manager of VSS-Data Systems and Servers Engineering and the Laser engineering team were all present for the event.

Powered on was the full configuration of the highend Alpha VMS Laser/Ruby system. In addition to the Laser system, static displays of the Laser modules were presented: CPU, Memory, I/O processor, XMI adapter, and the SCSI/DSSI adapter.

When announced, Laser/Ruby will represent the mid to high end of Digital's systems. When configured as a VAX, Laser will be the highest performance VAX system and offer complete compatibility with all existing VAX systems. When configured as a RISC VAX, Laser will offer industry leadership RISC performance and source, code, image and data compatibility with existing VAX systems.

Over the next few weeks the full suite of Alpha systems will power on, and over the next year they will be introduced. Together they will serve to demonstrate to the industry the energy and excitement Ken Olsen saw at the engineering power on of the Laser/Ruby system.

Ken Olsen praised the team's efforts to date and the design concept that Laser offers. "We take a lot of bad press, however, whenever customers come and see the level of excitement and technical expertise that has just been demonstrated they go away realizing how well we are going to do in the 90's." Laser offers an opportunity to... "to rapidly move towards a time when we have one hardware platform running VMS, Alpha VMS and Unix."

"This event is as significant as a similar one twelve years ago when Ken came to turn on the first VAX," reminisced Bill Demmer, "Only this time we did better. At the first VAX power on Ken discovered the first bug." Bill also pointed out that this system is a first step in his plan of populating the industry with Alpha systems.

Pauline Nist spoke of the team's drive for quality and market success. "We have demonstrated our commitment to quality and time to market. All the gate arrays worked with Pass 1 parts, and the time from design start to this power on has been only one year."

Steve Noyes pointed out that the Laser system contained 4 times the number of gates as the first VAX 6000 system, and yet the design was completed 3 months faster. This was due to improvements in CAD tools and processes and to the use of 1,500 VUPs worth of VAX 6000s used to simulate the Laser design. The initial VAX 6000 only had access to about 50 VUPs for its simulations.

"We're on a roll to FRS now, and while there is a lot of work yet to be done, once we get rolling we can't be stopped," said Vaughn Mackie, Alpha Laser Product Manager.

Ken Olsen and Bill Demmer power on the Alpha System.

digital *Alpha/Laser*

VSS Management Team Changes

Bill Demmer

In these times of constant change it is important for VSS to focus on those core areas that are of strategic importance for our future. Our mission is to provide the broadest range of high quality leadership solutions based on system and server platforms utilizing VAX VMS. To facilitate achieving this goal I have made several changes in my staff.

VMS is the software thread that ties all of our VAX platforms together. Don Harbert has accepted the position of VMS manager. Don will continue to report to me as he leads our VMS development and marketing efforts.

Replacing Don as manager of Data Center Systems and Servers (DCSS) is Pauline Nist. Pauline brings a wealth of experience in Mid-Range Computing to her new position. Pauline will have responsibility for all Mid-Range and High-End CMOS-based Systems and Servers, as well as the gallium arsenide advanced development program.

With the availability of fully functional prototypes, the overall Alpha program effort across Digital is gaining strong momentum. To lead the effort of focusing the work of Sales, Services, Channels, Applications and Engineering, I am pleased to announce the appointment of Peter Graham to the newly created position of the Alpha Business Manager.

To help provide Alpha the largest possible market appeal, I am pleased to announce the appointment of Steve Jenkins as group manager of the Alpha Software group. In this role, Steve will form an engineering team to do development work on the porting of Digital's OSF to Alpha systems. This represents an opportunity for us to leverage Digital's technology leadership skills towards providing customer valued extensions to industry standard products.

In Q1, VSS welcomed the Memory group as part of the new organization reporting to me. Tom Frederick leads our Memories efforts in continuing to deliver high-quality products that meet Digital's time-to-market and profitability requirements.

I am also pleased to announce that the Independent Software Vendor Group (ISVG), will expand its charter to include management of Digital's VAX/VMS application portfolio, as well as its current RISC/UNIX management responsibilities. Mike Mancuso, ISVG Group Manager, will report to both Dom LaCava and myself.

FY92 offers great opportunity for the VAX business and I believe the above changes will help us realize this potential. The number of new and exciting programs we are involved with should catapult the VAX family back into an industry leadership position and set the direction for Digital on into the next century.

Don Harbert

Pauline Nist

Mike Mancuso

Bill Demmer

Tom Frederick

Steve Jenkins

Peter Graham

15,000th VAX 6000 Ships to Switzerland

Andrea Harris
Literature Manager

In the three years since their 1988 debut, VAX 6000 systems have found their way into every conceivable type of business, all over the world. The hallmark 15,000th VAX 6000 system was shipped this past April from our manufacturing facility in Galway, Ireland. Purchased by a Swiss communications organization, the system will be used to help provide a myriad of communications services to people all over Switzerland.

Generaldirektion PTT, or Swiss PTT, encompasses three departments that provide postal, telephone, and telegraph services throughout Switzerland. The Telecommunications Department and the Postal Department are responsible for mail processing and delivery, a postal checking system, charge cards, telephones, telegraph, telex, telefax, packet-switching, messaging services, radio and television broadcasting stations, and postal buses, spanning all of Switzerland. The Presidential Department handles general administration tasks such as personnel, finances, general computer services, and leasing and construction of buildings.

The Swiss PTT uses VAX 6000 systems for the enterprise-wide production needs of its Telecommunications and Postal departments. In the Presidential department, VAX 6000 systems concentrate on the needs of individual departments.

The Swiss PTT uses its VAX 6000 systems to provide services such as telefax, cellular telephones, videotex, and private leased lines. It operates radio and television transmission stations and collects taxes on all television sets to support the national services.

Computer-based applications in the Postal Department support the dispatching of staff throughout Switzerland and the sorting of mail with optical readers. The Postal bus system is looking at ways for VAX 6000 systems to enhance its value as a commuter transit system and as a popular tourist attraction.

No stranger to VAX 6000 systems, the Swiss PTT will add the new system to its stable of 60 other VAX 6000 systems. This long-standing customer configures VAX 6000 systems as DSSI VAXclusters to maximize resource sharing and minimize security risks. These clusters use the Rdb/VMS database in a variety of applications. According to Digital Sales Account Manager Fabiano Chies, "The VAX 6000 system's strengths in data center computing, clustering, communications, expandability, and distributed processing allow the Swiss PTT to improve customer services while operating more cost-effectively. The VAX 6000 system provides the commercial strength needed for critical, decentralized applications at the Swiss PTT."

As the Swiss PTT and Digital Equipment Corporation move ahead in this successful association, new applications for VAX 6000 systems will continue to increase. Digital software engineers and third-party software application developers are working with Swiss PTT to enhance the family of expanding applications at the Swiss PTT.

VAX 6000 systems have been the answer to customers' needs 15,000 times. The Swiss PTT is just one example of how these premier systems are helping our customers do business.

F

Martin McCarthy, Plant Manager, Galway, accepts an award on behalf of the VAX 6000 line from VAX 6000 Field Programs Manager, Betsy Steele, for shipping the 15,000th VAX 6000.

Recommendations for the U.S. Power Electronics Industry

Don Staffiere
Group Hardware Manager

Recently a study was released by the R&D committee of the Power Sources Manufacturers Association (PSMA) concerning the technology status of the power electronics industry.

The committee is chaired by Don Staffiere, Group Hardware Manager in VSS engineering. The committee is made up of senior personnel from IBM, OECO, Sandia Labs, MIT, U. of Buffalo, U. of Wisconsin, the Electric Power Research Institute and Digital Equipment Corp., each involved in power electronics. The purpose of the study was to understand where power technology is today and what areas need attention to raise the level of technology.

The following is a summary of their findings.

Introduction

The initial goal of Power Sources Manufacturers Association's Research and Development Committee was to ascertain the current status of related R&D in the United States. The next goal was to recommend where "technology investments" might best be made to improve the power sources industry and the electronics industry as a whole.

One of the chief outcomes of the Committee's activities was increased communication between various industry groups. Much progress has been made in the coordinating endeavors and reducing duplication of effort through contacts with organizations including the IEEE Power Electronics Society, Power Sources Manufacturers Association (PSMA), Electric Power Research Institute (EPRI) and the National Committee on Power Electronics. Information sharing and increasing the visibility of the power electronics community was one of the major efforts of the R&D Committee. A result of this activity should be a substantial decrease in redundant studies and the enhancement of the technology transfer process.

The committee was made up of representatives from manufacturers of power sources, users of power sources, research groups and higher education. The group conducted this study during the past year and a half. The results represent a cumulative effort of hundreds of hours of research, meetings and report writing.

What follows is a summary of the findings, a brief report on the status of various industry segments and a set of recommendations for the future.

Summary of Findings

In general, the Committee found research activity was excellent but, the ability to turn that technology, quickly and efficiently, into product was poor.

More specifically the committee found:

- Shorter product cycles and competitive pressures are affecting industry's ability to effectively transition technology from R&D into products. Manufacturing technology and design for manufacture are issues requiring greater attention. New mechanisms need to be found for shortening the technology transfer and development phase.
- University research has been forward thinking and productive. However, there is a significant shortage of university power electronics programs in the United States. This shortage affects the availability of trained manpower and the level of research activity. Also, closer coordination between universities and the various industry segments is inevitable and desirable. Some evidence of these mechanisms producing closer ties is already demonstrated by various university/industry consortia.
- National research laboratories such as Sandia Laboratories in Albuquerque, New Mexico, through their Cooperative Research and

Development Agreements (CRADA) and various funding agencies can significantly contribute to industrial R&D activity. Incentives and mechanisms for technology transfer programs are now in place at the national labs and their capabilities need to be integrated into the U.S. industrial framework.

Status of Industry

Following are some brief notes on particular segments of the industry as analyzed by the R&D Committee.

Power Semiconductors - Not badly positioned with a lot of work in process in the low power devices. Poor market share in higher power areas including BJT's, IGBT's, and GTO's in the international marketplace.

Magnetics - Materials need further study in order to have a domestic technology capability. Efforts are just getting underway by the Magnetics Materials Producers Association (MMPA).

Capacitors - Area of greatest concern because of investments in technology development being minimal. Technology is moving slowly in most capacitor technologies and there is a strong recommendation to enhance the research activity. If the suppliers cannot conduct the research alone, then users must get involved through collaborative research.

Technology Translation Into Product - To be competitive in the global market, an effective transition path has to be found for moving technology into product. Traditional roles of universities and industries in research are no longer valid. The two groups need to interact so as to provide mechanisms for sharing resources and costs associated with development of base technology.

Recommendations

In general, the Committee recommends more coordinated research between parties with common areas of interest so that funding bases can be larger and turnaround times can be shorter. Such joint efforts provide critical mass and shared funding needs and allow development of a more significant base of generic technology. This model is seen to be in effect today with the Power Semiconductor Committee recently formed through PSMA. Their objective is to work on generic issues, such as common test methods and parameter assessments, to avoid wasteful redundancy and to grow as an industry without compromising competitive position. There is much potential that by working together other areas can be identified for future research and/or development programs which could include semiconductor processing equipment.

Specifically the R&D Committee recommends:

- More research needs to be conducted in Magnetics. Research in magnetic materials was found to be especially weak and the U.S. lags significantly behind studies being conducted in Japan. A committee has recently been formed through PSMA to address the materials issues in the Magnetics areas and to help close this gap through the combined efforts of industry and higher education.
- Improved technology for capacitors. Getting more performance in smaller volumes with high reliability is desirable for capacitor users. Because capacitors are a low profit margin product, manufacturers' ability to invest in research is very limited. This situation must be addressed aggressively to have a major impact on industry.

  To the best of the committee's collective knowledge research in this area is limited to some work at Sandia National Laboratories and some government programs. One approach to remedying this particular situation is through the coordinated efforts of multiple agencies such as the National Aeronautics and Space Administration (NASA), DOD and EPRI along with users and manufacturers of the products to develop programs which will enhance capacitor technology. This should include process development.
- Improvements in CAD *connectivity*. Studies in Power Computer Aided Design show that connec-tivity along a process is the key to maximum performance. Individual computer programs addressing separate aspects of the design and manufacturing process need to be able to "talk" to one another. In this way development and manufacturing time is reduced. A *canned* total solution program is not recommended and the preferred alternative, connectivity, would

provide a more flexible approach to manufacturing systems from design to finished product. Connectivity *products* are becoming increas-ingly available.

- Broader based committee involvement. The Committee met with representatives from the automotive and appliance areas. There was significant technology overlap amongst UPS manufacturers, a part of the power sources community, and manufacturers of drives (which is a core business of both automotive and appliance manufacturers). Consequently, representatives from the appliance and automotive areas need to be involved in the various committees being established through PSMA. It is noted that this could present new business opportunities for PSMA members.

Conclusion

As stated in the introduction, fragmentation in the "power community" is noticeable. Much progress has been made in coordinating activity and reducing duplication of effort through contacts with organizations including the Power Sources Manufacturers Associates, the IEEE Power Electronics Society, EPRI and the National Committee on Power Electronics. Information sharing and increasing the visibility of the power electronics community was one of the major efforts of the R&D Committee. This activity should result in substantial decrease in redundant studies and should enhance the technology transfer process. The report on manufacturing competitiveness is expected to soon follow this report.

The International Enclosure Series

Ron Cohen
CEDG Group Product Manager

Digital is many things to many people. We manufacture and offer a myriad of computer products and services to virtually every industry in almost every geographical area of the world.

While computer operating systems, architectures, software, and media have evolved over time, one rather functional as well as highly visible aspect has gone largely unchanged for well over a decade (except for mandated performance and functional upgrades). What I am referring to is the system or option cabinet/enclosure.

Routinely every new product or program requiring an enclosure, has to go through complex testing and qualification to pass Digital as well as industry standards pertaining to packaged systems. History reveals that nearly every new application has required a substantial level of enclosure customization to ship product. This equates to time to market delays, higher costs (i.e., tooling, inventory and engineering expenses).

While our present enclosure products serve the purpose, we have to be cognizant that they have been problematic in terms of economically and practically meeting corporate and industry needs which have evolved over time and through technical changes and mandate.

To insure our future success in terms of achieving corporate marketing goals, we have gone ahead and developed the H9A00 International Enclosure Series (IES). This is Digital's newest corporate system/option packaging format developed by CEDG (Corporate Enclosure Design Group). As its name implies, the H9A00 International Enclosure Series is compliant with virtually all proposed European Common Market requirements, as well as domestic requirements. This includes but is not limited to metric dimensioning, European material sourcing availability (if required), and Six- Sigma compliance which includes consideration for assembly, quality control, servicing and distribution.

Please note, that during the H9A00 Series development cycle, it was referred to as the NEP or "New Enclosure Program."

The H9A00 development effort was initiated three years ago and supported by Corporate Management to resolve a plethora or recurring problems relating to products being packaged into old designs requiring what is often referred to as "Band-Aid™" solutions.

In retrospect the "Band-Aid™" solutions were ultimately effective, but costly in terms of tooling, time to market, and resulted in fragmented manufacturing volumes,

Continued on next page.

higher inventory, redundant engineering resource requirements, and mixed or diluted corporate image.

The H9A00 Series, many technical attributes are measurable in terms of increased strength, rigidity, shielding, cable management, improved cooling, and provision for acoustic sound absorption material. All of these enhancements were the result of documented problems routinely encountered over the past decade across the corporation.

Perhaps equally or more important is the business or marketing enhancement aspect which is the result of a radically new aesthetic styling image which emphasizes a broad horizontal air slot pattern. This represents a welcome departure from the current aesthetics which are largely representative of twelve and fifteen year old designs.

The Physical Design

The IES design's overall height is 1700mm (66.9"). Internally all IES models have 1500mm (59") of vertical mounting space. Comparatively, this is 165mm (6.5") greater than today's current H9640 and H9650 series.

The IES Models (cabinet assy's) are available in the sizes listed in Table 1.

From a marketing and business perspective the H9A00 IES cabinet has been developed to effectively replace the current H9640 Cross Product and H9650 Corporate Enclosure Series which are now in service, but as previously stated, representative of twelve and fifteen year old designs.

A Brief Cabinet/Enclosure History

A well known philosopher and historian once said, "that those who do not study their history are doomed to relive it."

Historically, the H9A00 Series is Digital's fifth Enclosure Series since 1957.

Initially Digital started out with the original CAB-1 cabinet/enclosure series for the PDP-1 through the PDP-7. These were all welded tubular framed cabs, about 70" tall, and painted pastel light blue. Several colors including a beige "fleck" were available.

The second generation was the H960 Series released in 1968. It replaced the earlier all welded tubular series. The H960 stood 72" tall, and included a painted black "S" frame with grey end panels. It evolved over time to include a 47" "lo-boy" version with a Formica™ top. Early versions destined for military applications (e.g., Bunker-Ramo) could be special ordered in military light green.

The third generation called the H9600 was released in 1975. This series consisted of four models, either 50" or 60" tall, and either 27.5" or 47" wide. The "S" frame was zinc plated for good grounding. By 1983 the H9600 had to be updated for compliance with the FCC's mandate for EMI/RFI attenuation. It was rename the H9650 and is little more than an extensively modified (Band-Aided™) H9600.

External Dimensions

Model	Height	Width	Depth
H9A00 SWHB	1700mm (66.9")	600mm (24.5")	865mm (34")
H9A02 WBHB	1700mm (66.9")	800mm (31")	865mm (34")
H9A03 B1/2HB	1700mm (66.9")	1000mm (38")	865mm (34")
H9A04 DWHB	1700mm (66.9")	1200mm (47")	865mm (34")

Internal Dimensions

Model	Height	Width	Depth
H9A00 SWHB	1500mm (59")	465mm	635mm
H9A02 WBHB	1500mm (59")	665mm	635mm
H9A03 B1/2HB	1500mm (59")	865mm	635mm
H9A04 WBHB	1500mm (59")	1065mm	635mm

Table 1.

The fourth generation (low cost smaller systems) made its debut in 1979 as the H9640 Series. It was available in 42" and 60" tall versions, as well as 21.5" and 29" widths. The H9640 Series was made FCC complaint in 1983.

Benchmarking

To insure the success of the program, the H9A00 Series Design has been benchmarked against its current Digital counterparts, and more importantly the premier or "best in the business" outside (non-DEC) computer cabinet/ enclosure manufacturers. This includes Schroff, Rittal, Lion, Equipto, Trimm, and Everest. In every comparison, Digital's H9A00 Series compared favorably in terms of cost and performance. Compared against our largest rival (IBM) enclosure products, our enclosure products are notably superior in terms of appearance, fit, and operation.

Conclusion

The success of the H9A00 program is the result of the close relationship established between the CEDG (Corporate Enclosure Design Group), and the many organizations which contributed to the H9A00's development.

The CEDG product development team consists of the following:

Don Staffiere, *Program Manager*
Jane Derosby, *Secretary*
Wayne Rett, *Engineering Manager*
Ron Cohen, *Product Manager*
John Benson, *Lead Principal Engineer*
Dave Dalrymple, *Principal Engineer*
Dave Alessandrini, *Engineer*
Jim Fritscher, *Designer*
Steven Wolski, *Draftsman*
Rod Huff, *Draftsman.*

The list of internal groups which actively supported the H9A00 program from concept to fruition spans the entire corporation. Special thanks go to the Colorado Mass Storage Group, Industrial Design, and the Westfield Enclosure Business Group all of whom have worked together to get to where we are today.

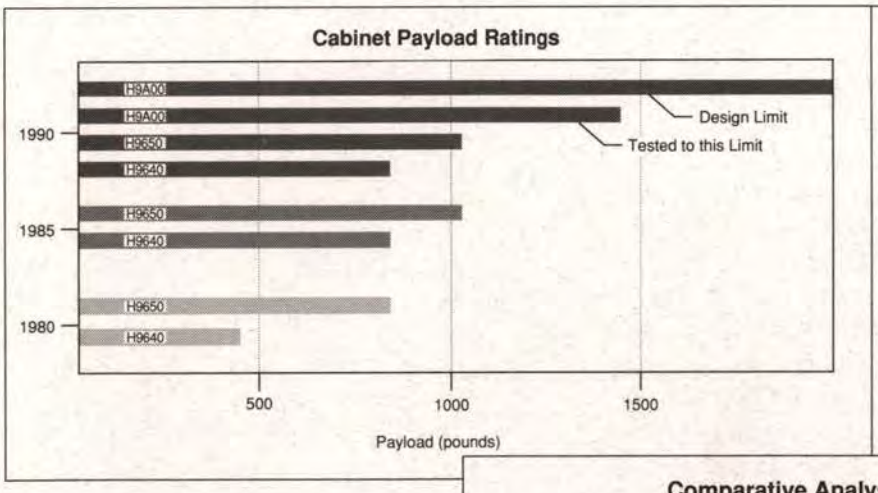


Figure 1. Cabinet Payload Ratings

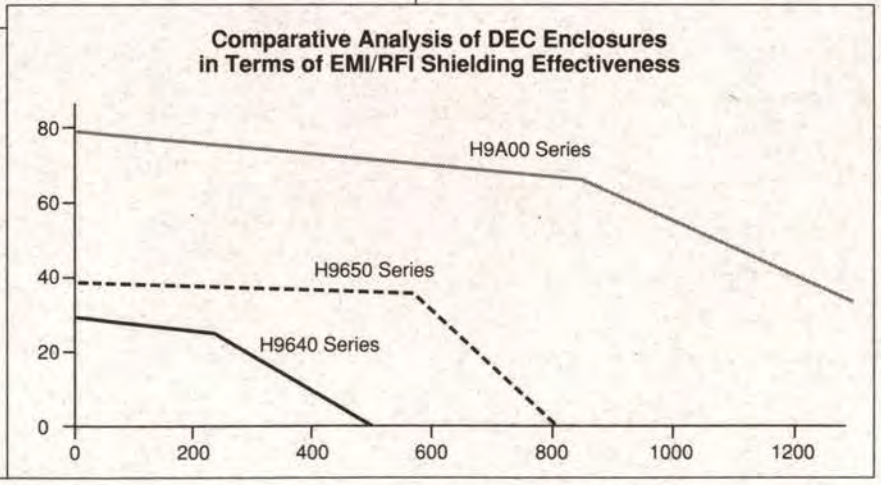


Figure 2. Comparative Analysis of DEC enclosures in terms of EMI/RFI shielding effectiveness.

Use SIX SIGMA In Marketing? Yes!!

Barbara Townes
Entry Systems Business Marketing

In Entry Systems Business Marketing we applied the Six Sigma principles to our product announcement process, and we have seen the following results:

- ***A better informed product announcement team***
- ***Team development of the product announcement plan***
- ***Ownership and responsibility by individuals as team members***
- ***Greater commitment to announcement deliverables, including timeliness and quality***
- ***Definition of "areas we can influence/control" versus "areas we can TRY to influence but have little/no control"***
- ***Commitment to improving areas we can influence/control.***

Initial Six Sigma Application: MicroVAX 3100 Models 10e, 30, 40, 80

Our first application of Six Sigma principles to our announcement process occurred last winter with announcement preparations for the replacement of current MicroVAX 3100 products. Core announce-ment team members were identified, a one-day Woods meeting was set up, and an agenda developed. At the meeting Subhash Dandage, Six Sigma Consultant for ESB, gave a brief summary of the Six Sigma principles to the participants, who had already undergone the Waterfall Training. Then Subhash guided us through the six steps of Six Sigma.

Step 1: Define the products or services you create or provide

The first step was not complicated since we were well able to identify our "product," which is the announcement process itself.

Step 2: Identify customers and define what they consider important

The second step was more difficult and provided insight to us as we identified more customers than originally anticipated. We thought the customers for product announcement were the field and the "real" or paying customers. As we analyzed and discussed customers we learned they include the following:

- Paying customers
- Sales representatives
- Sales support
- Internal Digital groups including product marketing, applications and industry marketing, channels, sales and operations, etc.
- Press, consultants, and analysts.

These customers are worldwide, including Europe and GIA. We have a GIA Marketing Manager who represents GIA and is tied into all of our announcement plans and activities. Our European Marketing and MARCOM managers are also tied in, and participate via a teleconference at each announcement meeting.

Step 3: Identify what is needed from suppliers

For obvious purposes we decided to refer to suppliers as our "sources." Identifying sources also was an eye-opening step! Some of our sources are also our customers! Sources include all those people on whom we're dependent to complete announcement activities. Sources are also worldwide, including GIA and Europe as indicated above.

Announcement activities include:

- Product readiness, which drives most announcement activities,
- Product positioning, which includes internal and competitive,
- Literature, which includes sales update, info sheet, VAX brochure, SOC, etc.,
- Training for sales reps, sales support, technical edit and configuration specialists, hotline centers, ACTs/ DCCs, applications and industry marketing, etc.,

- Direct marketing, which includes all the marketing to the installed base, i.e., DECdirect,
- Programs to the field and customers to drive revenue,
- Performance test data to position systems across various application environments,
- Channels activities to drive sales to distributors, OEMs, etc.,
- Rackmount models and marketing,
- Events plan which includes the announcement event, customer events, DECUS, trade shows, etc.,
- Press, Analysts, and Consultant briefings, media, etc.

The sources are all the people who manage these activities and who contribute articles, data, equipment, programs, etc. Easy to see why some of our sources are also our customers.

Step 4: Define the process

Then we defined the process for doing the work. Since ESB has announced numerous products over the last few years, we have a well developed process (see Figure 1), and the application of the six steps is expected to improve this process.

However, the next step proved to be the most difficult: mistake-proofing the process.

Step 5: Mistake-proof the process

In this part of Six Sigma analysis, the goal is to identify the "defects," or areas where failures or imperfections occur. In a manufacturing or engineering environment defects can be identified more easily than in a marketing environment because of two reasons. One, engineering and manufacturing disciplines are more mature; marketing is still young as a discipline. Two, marketing activities are generally less tangible than engineering development and manufacturing build processes.

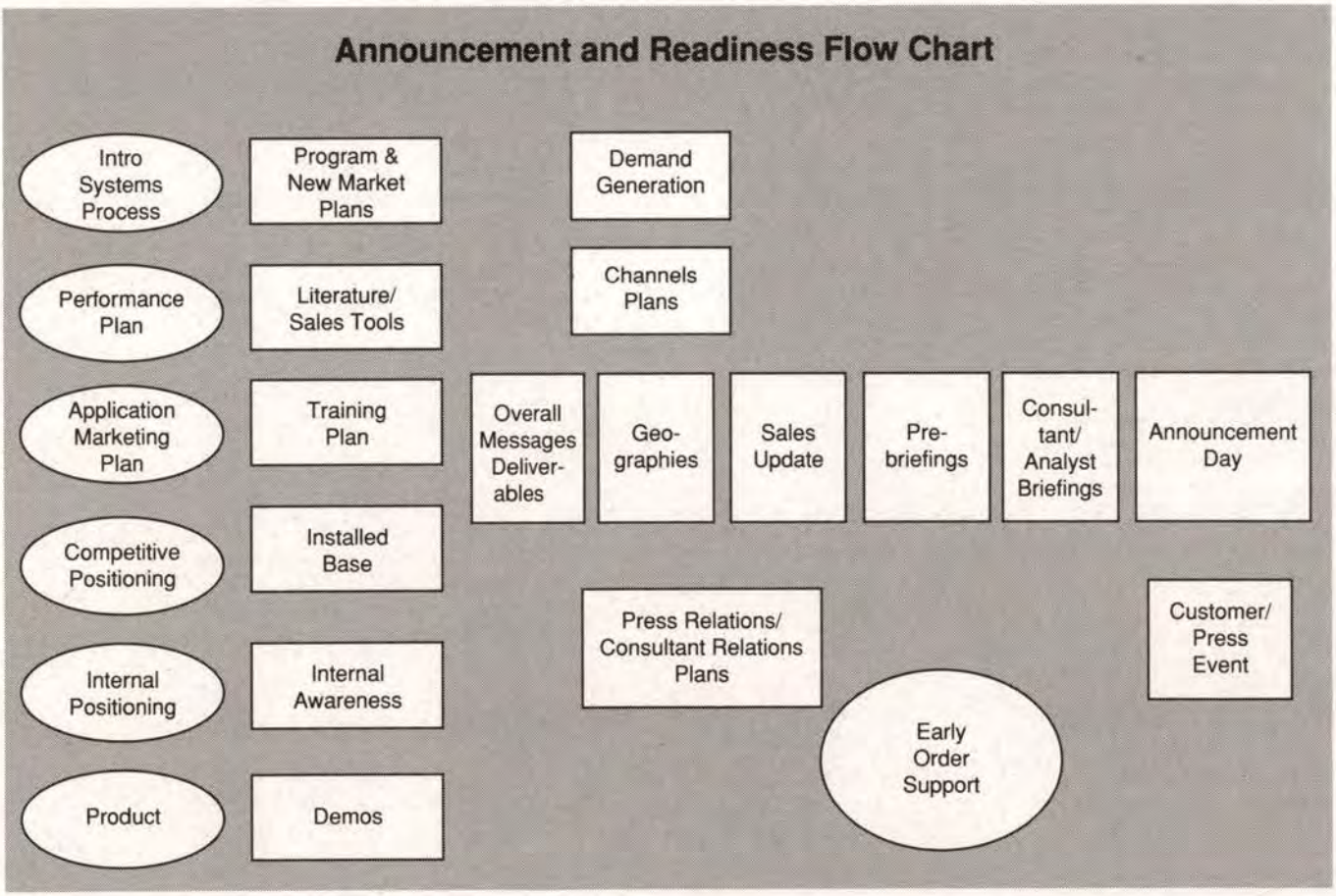


Figure 1. Announcement and Readiness Flow Chart

We used the following model (see Figure 2) throughout the meeting. One major advantage of the model was that it made it easy to understand the impact of our sources on our product.

Our sources need to clearly understand what we need from them in order to help us deliver the product. We have to be specific in terms of the deliverable and the schedule, and we need to regularly update our sources regarding any changes to the deliverable or schedule. For instance, one of our sources provides us with the performance test information. We need that data to support announcement activities such as sales update and training. However, if hardware is not available in time to complete the testing, the performance groups cannot deliver. Therefore, it's important for us to update them on hardware schedules as well as announcement schedules.

This is a crucial part of the Six Sigma process that can add significant value in terms of understanding what's required from sources, and the impact of delays and un-met deliverables.

Using this model we tried to assess the effective areas of the previous announcement, which was the VAX 4000-200 announcement. In some areas we quantified defects. For instance, we have a continuing goal to work collaboratively with more industry and application marketing groups. Currently, we feel we work successfully with 2 to 4. We set a goal for improving that to 4 to 6.

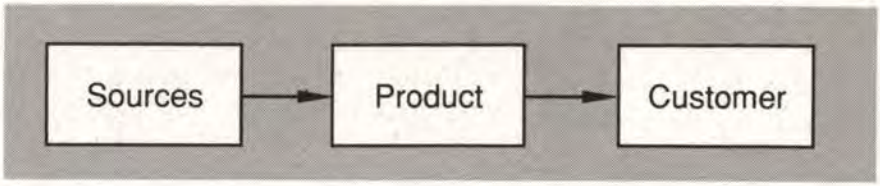


Figure 2.

In other areas we projected percentage improvement estimates as a measure of success. For instance, we felt that we only trained an estimated 25 to 30% of the field when we announced the VAX 4000-200, and we wanted to improve that to 50%, and more, with succeeding products.

The defects we identified, whether a specific number or a percentage, became the baseline. Using that baseline, we set goals for improving the MicroVAX 3100 replacement product announcement.

Step 6: Ensure continuous improvement

Since this was our first Six Sigma application we did not fulfill step 6.

Second Six Sigma Application: VAX 4000-500

Since we had learned so much and seen the effectiveness of Six Sigma on our announcement plan for the MicroVAX 3100 replacement products, we decided to apply the process to our next announcement, the VAX 4000-500, replacement for the VAX 4000-300. We followed a similar process, i.e., identifying the core team members, developing the agenda, and setting up a one-day Woods meeting. At that meeting I acted as the Six Sigma leader as well as being the Announcement Manager.

Our goal this time around was to complete the applications of the six steps in the morning, and, in the afternoon, to do the following additional work:

- Review the proposed announcement plan,
- Have each core member refine his/her section of the plan,
- Review each section with the team,
- Leave the meeting with a first draft announcement plan developed and agreed-to by the core team.

This was a highly efficient procedure and it worked very well. We went through the Six Sigma steps much more quickly because most of us had worked together as a team during the first Six Sigma application. We did not short circuit the steps, but we were able to accomplish them quickly. There were several differences, however.

When we came to Step 3, Identifying Suppliers/Sources, we had learned enough to know that it was necessary to separate our sources into two groups:

- Sources we can influence and/or control, and
- Sources we cannot control (only try to influence).

The latter includes activities such as announcement dates, pricing, product ship readiness, etc. Separating these helped us better identify those areas where we could plan for improvement, and the areas where we needed management support in order to further improve the announcement process. Some of our goals for improvement the second time around were more aggressive. Some goals stayed the same because, at this point, we had not been able to achieve the objectives we had set the the first time.

A second difference was Step 6, Ensuring Continuous Improvement. In order to improve we need to have measurements. We looked back at the work we had done with the MicroVAX 3100 replacement products announcement plan. We used those goals and a current assessment of our success or not in meeting those goals as a baseline for understanding what we might accomplish this time around. We set our goals for the VAX 4000-500 announcement plan in much the same way as we had done the first time, that is, we were quantitive in some areas, and in other areas, we set more qualitative goals for improvement.

When we had finished the application of the six steps, we went to the afternoon's activities. In preparation I had prepared a proposed announcement plan based upon previous announcements and based on my assessment of where the project was at the time. The team members were given time to review the plan, and within a defined period of time, they were expected to come back with any revisions or additions.

When we came back together as a team, each player presented their sections. The team reviewed the section contents, and we ended up with a first draft sufficient to begin announcement meetings at an advanced stage of operation. Instead of spending time refining the plan, we were able, in our first formal announcement meeting with an expanded team, to focus on activities.

Value Added

At a time when resources are becoming scarce, Six Sigma has helped us improve our announcement plan and process, thus making us more productive. This could be achieved due to time we spent as a team, analyzing our goals, working together to identify customers and sources, defining and applying metrics for measuring improvement, and managing the improvement process. Plus, we learned how dependent we are upon each other to be successful.

VSS Information Service Center

Staff: Dave Carlson, *Manager*
Kevin Harrington
Karen Young

What is the VSS Information Service Center?

The VSS Information Service Center is a function of the VSS Information Management group, managed by Dick Scheib. It was established in Q3-Q4, FY91 with the following charter:

- ***Support VSS in using current desktop and information technologies to accomplish the business goals.***
- ***Provide a support environment for using & learning these technologies.***

Simply stated it is:

A place where resources – both people and equipment – are available to assist you in using your desktop hardware/ software.

Today's desktop environment is growing...it's becoming more *powerful* and more *sophisticated* – especially, with the advent of Digital's strategy for NAS and open systems.

So, what is NAS?

According to the NAS architecture and marketing documentation, NAS stands for "Network Application Support." It is Digital's *system* architecture and product set for providing open integrated systems to delight our customers worldwide.

Enterprises today are facing the serious problem of developing an integrated, computing system that takes into account – and makes the best use of – multiple vendor platforms. For years, enterprise departments have solved their business problems by purchasing a diversity of hardware platforms, operating systems, and software applications. These purchases are often incompatible with the solution acquired by a neighboring department.

Today, an enterprise needs a computing system where the resources, hardware and software applications, can be shared throughout the enterprise. Applications in the 90's will be required to have the following qualities:

- Openness
- Portability
- Inter-operability
- Distributed processing.

The fundamental goal of NAS is to make it easier to create, operate and evolve enterprise-wide information systems. This requires a highly integrated system that spans the enterprise. NAS is an architecture as well as a set of services based on international and industry standards. So, what does all this mean? It means that *any desktop* can work across any *heterogeneous computing environment.*

As we within Digital and VSS begin to implement and use this OPEN environment ourselves, we in the VSS Info Service Center are here to assist the members of VSS in utilizing this NAS environment as easily, efficiently and cost-effectively, as possible. Our services are geared towards enabling you to utilize this environment.

The VSS Information Service Center provides services to help answer questions, like

- This thing won't print?
- How do I keep my files organized?
- I need to do "XYZ," what software and hardware should I be using?
- I need some data, but I don't know how or where to get it or what software to use?

- I need to use a color printer...a PC...a MAC...DECwrite..how do I do it?

The VSS Information Service Center also provides an environment where VMS workstations, PC's/MS-DOS, and Apple Macintosh's may be used. Color printers and scanners are also available.

We are located in BXB1. You can contact us by any of the following:

- Stop by! We're located in BXB1 2nd floor Poles F7-G7,
- Send MAIL to MSBCS::INFOHELP, or
- Call, DTN: 293-5421.

Helpful Hints from the VSS Info Service Center

Q. "How do I include text files created with EDT into DECwrite, and not lose the format?"

A. To include a file in ASCII format, which has been created using a text editor:

1. Start DECwrite.

2. Open your *receiving* DECwrite document, and place the cursor where you want the included text to appear:

→ Choose *file* from the MENU bar
→ Choose *import/export*
→ Choose *include text file...*

DECwrite displays the *include text file* dialog box:

1. Enter the name of the text file you want to include.

2. Toggle the *include text as* option to Program.

3. Click on *OK.*

Q: "Sometimes when I print a file in DECwrite or DECpresent, it says 'Print file has been queued,' but nothing prints...what's wrong?"

A: When you print a file from DECwrite or DECpresent, it is given a *Job flag name* to be processed by the print que. The name is DECWRITE:*document_name* for DECwrite documents and DECPRESENT:*document_name* for DECpresent presentations. There is currently a maximum length for this name of 31 characters.

This limit is being fixed in future releases of software, but if you are having problems with a particular file not printing when it says it has been queued, then you should shorten the name of your document. Limiting your DECwrite document name to no more than 22 characters, and your DECpresent presentation name to no more than 20 characters, will eliminate this problem for you.

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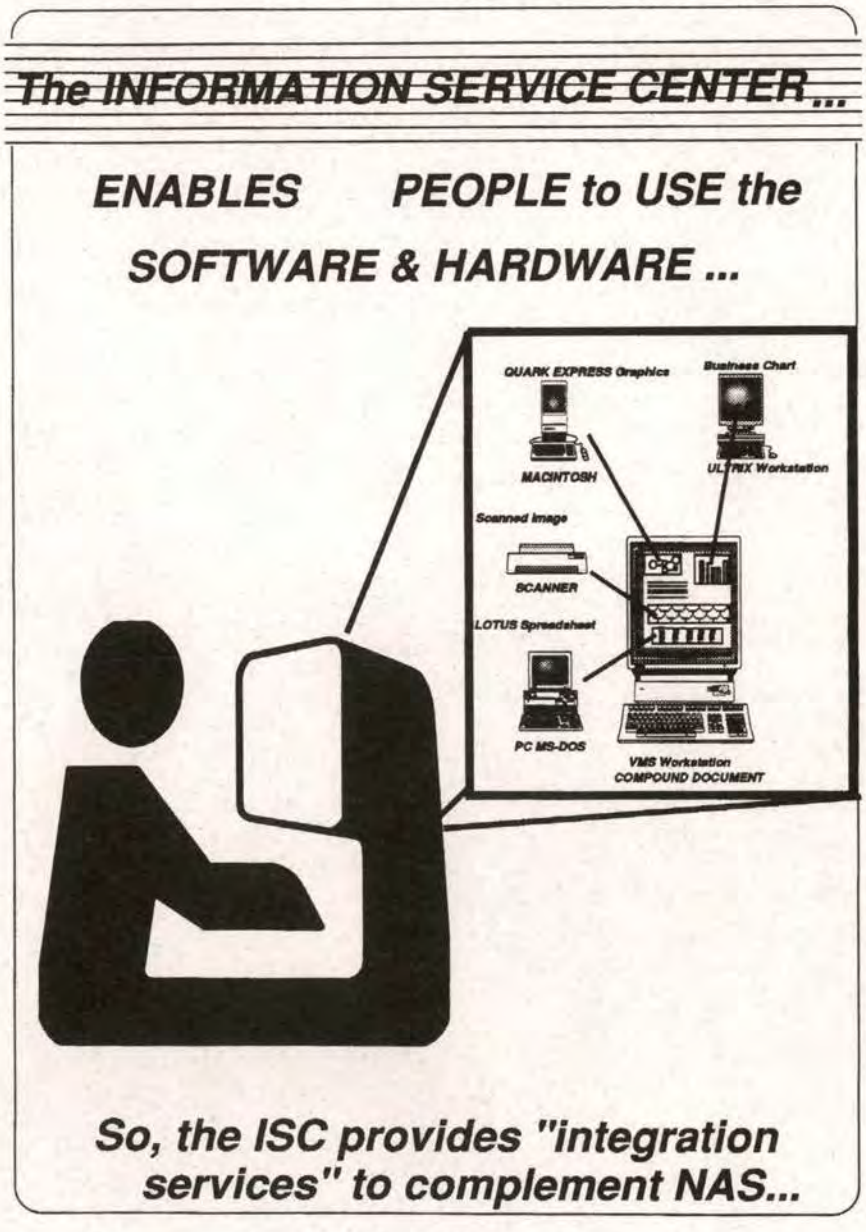


Memories Product Creation Unit Joins VSS

Madeline Flynn
Marketing Manager

Under the leadership of Tom Frederick, the goal of the Memories Product Creation Unit (PCU) is to supply both internal Digital customers and external end-user customers with "best in class" *cost* and *quality* semiconductor-based memory products, subsystems, and services. As a new member of VSS, Memories will continue to design, manufacture, and market memory products, including primary and secondary solidstate storage, that enhance the performance of Digital systems and increase the profitability and competitive advantage of the corporation.

The expertise of the Memories' engineers encompasses the development of very complex memory subsystems incorporating sophisticated gate arrays, such as the VAX 9000 and VAX 6000 memories, to simple cost-sensitive SIM-type products. "Through years of experience, our group has amassed a wealth of knowledge regarding memory error correction, unique memory power distribution problems, and the special aspects of memory packaging, manufacturing, and test," says Ron Given, the group's Engineering Manager.

During system design and development, memory engineers become an integral part of the client's design team, working closely with system designers to optimize memory and bus interconnects. In a collaborative effort the engineers make tradeoffs between memory features and system attributes to achieve the best overall system performance. Additionally, the use of common design and verification tools helps ensure an optimal overall design. Close collaboration has also proven to reduce both system and memory costs and improve time-to-market significantly.

Over the past five years, the Memories group has consistently met FRS commitments for 33 consecutive memory products. "We want to ensure that we deliver our memory products on time," Ron states. "We fully intend that our record for meeting FRS commitments remains unbroken."

At the same time, the Memories group has controlled engineering costs, maintaining spending at the same level during the past three

Memories Product Creation Unit (PCU): back row - left to right; Ron Given, Brian Miner, Steve Cullen, Bill Coates, Frank Sebastion, Tom Frederick, Joe Lawrence, Jack Miller, Siox Mallard, and Ed Lee.
Front row - left to right; M. L. Krakauer, Mary Young, Tony Wain, Pete Rojcewicz, and Dick Cook.

years. Staffing has dropped and productivity increased. One cost saving measure is to design memory products to be used across systems. For example, MS44 memories are used in five systems including the VAXstation 3100 Model 76 and DECsystem 5100 systems.

From a manufacturing perspective, product quality and cost are foremost. A problem-free installation rate of 99.96% attests to the very high quality standards of Digital's memory manufacturing. Manufacturing has also been very aggressive in reducing product costs from year to year and is active in the Six Sigma program.

"Memory manufacturing provides major benefits to the company by centrally managing the sourcing of memory products, whether manufactured internally or purchased," says M.L. Krakauer, the Memories Manufacturing Manager. "In this role, the group effectively accommodates shifts in demand across groups while reducing overall inventory at the corporate level."

For each new memory, the group performs a *make/buy* evaluation and selects the best option. "If we decide to manufacture the memory, it is because in-house manufacturing is the most cost-effective option," says M.L. "Our manufacturing plants are leaders within the corporation in terms of cost and quality."

Managing DRAM sources for the corporation and for Memories is another key group responsibility. The availability of cost-competitive, high-quality DRAM parts affects the profitability of the corporation as a whole. Consolidation of DRAM requirements gives Digital more leverage with DRAM vendors in terms of volumes and cost. Approximately 80% of the DRAMs sourced by the group go into Digital memory products. The remainder are used in other Digital products.

Over the past year, Memories has improved the global balance of Digital's DRAM supplier base significantly. The group has also increased the focus on vendor relations to help ensure a cost-competitive and dependable source of high-quality DRAMs.

DRAM technical and business consulting services provided by the group, in the U.S. and overseas, help internal Digital design groups who need DRAM components for their products. The Memories group matches individual needs with available parts and works with suppliers in defining components that satisfy specific Digital needs.

"Currently we are working with a vendor to define a high-bandwidth DRAM targeted for Digital's future systems," Steve Cullen, the group's DRAM Business Manager states.

Because memory products are sold to end users as well as supplied to internal groups, Memories product management and marketing efforts span product development and management as well as strategic and operational support to the Field for aftermarket sales. To build sales awareness, Memories develops training tools and advice packages in addition to participating in sales training programs. The group also stimulates aftermarket memory sales through numerous marketing programs. For example, Memories and Digital's Direct Marketing Organization (DMO) combined forces to conduct direct merchandising programs, such as the Make-The-Call program for VAX 6000 and VAX 4000 customers. In addition, joint programs with the Service Account Organization (SAO) equip Digital service engineers to identify memory sales leads.

In its role within VSS, Memories looks forward to working with VSS groups to maximize the organization's overall contribution to the corporation. Memories will continue to set high standards and apply its expertise and resources diligently to achieve company goals.

Digital in China

Ralph Christensen
VSS Group Personnel Manager

This past May, Digital Equipment Corporation was invited by the Chinese Academy of Sciences (CAS) and the Chinese Enterprise Management Association (CEMA) to prepare a seminar on the management of high tech organizations in an open market environment. The senior leadership of these two influential ministries very open, on and off the record, about their need for fundamental reform. They are also very aware that they have a great deal to learn about this capitalistic/market system which they have been at ideological odds with for 40 years. Just as many westerners have a very superficial understanding of Communism, and how it really works, the Chinese also have much to learn about market systems and how they really work. We each have a high level conceptual understanding of the differences, but not the nuts and bolts implications of the theory. The real power of the Chinese insight, is that they understand what they don't know. They were very clear with us that while they are impressed with our technologies, they know that technologies will come and go. They really want to learn about the management and organization systems that can leverage the development of their future technologies. Digital's purpose of the trip was to strengthen our presence, and relationship with senior government and industrial leaders in China. Digital's revenues in China had grown steadily to $62M in 1988, and then faltered, following the serious political problem there in that year.

China's Business Climate

China's communist government has controlled its business environment for decades. As you would expect, this has had a significant impact upon the business climate. Industry strategy is developed as part of China's 5-year plan. Decisions are made by Government and Industry bureaucrats, with limited input from technologists or the market. Their focus on bureaucracy creates walls between agencies that make our Digital "Stovepipes" feel like a family reunion.

Industries don't talk with the universities about research or market needs. Industries don't talk with each other about joint research. Hierarchy reigns supreme. It is the source of power. Decisions are all made centrally. A technologist would not think to disagree with management. Once an organization is designed to develop a particular product, the organization retains a life of its own, long after a product has shipped. They don't have the flexibility to move the organization on to new work, hence often creating a bloated organization full of people with little focus.

Digital representatives visiting China. From left to right; Bill Johnson, George Chamberlain, Marty Hoffman, Maggie Hoffman, Art Fisher, Bob Mackey, Peter Graham, John Adams, Ralph Christensen, and Bruce Palmer

Consumer goods to meet the most basic human needs (food, clothing, shelter), appear to be in good supply. The shops seemed well stocked, but with very little selection. Most wear a common style of clothing, although Western styles are beginning to appear. Prices are artifically fixed and are incredibly low by western standards. $2.00 for a shirt, $6 for a coat, $1 for simple shoes. (Imported Western goods equal or exceed prices in our stores, if you can find them.)

However, the average salary is roughly the equivalent of $40/month. Salaries are fixed by a very rigid government system. All start with equal salaries, whether as a doctor, an engineer, a shopkeeper or farm laborer. Salary increases are time based, with little to do with performance. Even most Senior Government/Business Leaders earn only 100-150 dollars/month. The primary source of motivation seems to be housing size and quality, which is determined by the government, and could cost as little as $5/month.

The government seems to be acknowledging its need to move China into the world marketplace. The officials speak openly on and off the record of the need for reform and increased openness. They talk of the need to make fundamental changes in how they manage government and industry. However, they clearly do not want to follow the reform lead of the Soviet Union and other Eastern European countries. The Chinese leaders believe that Gorbachev is out of control and that such change would destroy China. They hope for a much slower and controlled transition. During the past ten years, the government has begun to sponsor joint ventures with private companies; some from outside of China, some from within. Beijing brags up its Kentucky Fried Chicken venture as the chain's largest restaurant in the world. China has very obviously chosen to joint venture in the hotel industry. Beijing sports many of the most modern hotels you'll see anywhere. Their elegant architecture poses a striking contrast to the government housing skyline of stark high rise apartments of brick, and mud housing collectives seen in and out of the cities. I spent considerable time with the president of a software joint venture company who was most eager to learn how to manage in an open-market environment.

The Digital Seminar

The opening ceremonies began with closely orchestrated "informal" tea meetings between government officials and the Digital contingent. The formal opening ceremony included both government, CAS, CEMA and Digital leaders, as well as the nearly 125 industry leaders who came to learn about doing open hierarchy business.

My two presentations covered organization and work design for development of new technologies/products, and education and development. The message of my first presentation was that traditional hierarchy is no longer capable alone of developing new knowledge which is the basis of new technology and products. I emphasized the need to manage hierarchy in parallel with virtual, flexible, temporary teams focused on specific work. I dealt with the very delicate balance of integrating virtual teams with hierarchy. I felt that the topic piqued their interest. They had

Over the course of the 5 day seminar, Digital provided presentations on:

- ***Digital History and Products***
- ***Technology Development***
- ***Marketing***
- ***Project Management***
- ***Financial Management***
- ***Organization/Work Design***
- ***Compensation/Benefits Culture***

Continued on next page.

Ralph Christensen speaks at recent business seminar in China.

many excellent questions and expressed many times their interest in these organizational and management issues. They consider these issues to be at the base of their needed transition.

They were also intrigued with the variety and availability of our development opportunities for technical and management employees. They don't seem to have figured out how to integrate technical development needs with educational sources like universities or internal training. They were interested that we don't ask training recipients to sign a commitment to pay for the training should they leave their work unit. This is the general practice in China which seems to dis-incent people to receive training, which training would be far too expensive for an employee to ever pay on their own.

I explained that we acknowledge that a small percentage will abuse the system and leave, but that we don't want to create policy which dis-incents the 98% in order to control the 2%. Lights seemed to go on.

I felt that all of the presentations were very well done and well received. China is desperately searching for this basic type of management education. I believe that herein lies an intriguing EIS opportunity to provide education about infrastructure and management. I believe that Digital's networked system style of computing can only be fully leveraged in China when their infrastructure itself becomes more flexible and networked conceptually and in practice. They are clearly reaching out for change and reform, albeit at their own controlled pace. My sense is that the more their infrastructure becomes interactive and flexible, the more obvious it will become that our product/services style will meet their needs.

New Boxboro Training and Development Center

Joe Senz
Development Manager

The Boxboro Training and Development Group recently opened its new Training and Development Center; thus renewing the business' commitment to Technical and Professional development of its employees. The new facilities represent a "significant" upgrade in space and capital equipment by providing seating for up to 22 students and a "DEC-windows" workstation environment on a stand-alone cluster.

The open house, held in July was an opportunity for employees to see the new facilities, meet the training and development staff, receive a copy of the current program offerings and generally talk about training and development opportunities.

Don Harbert, Sas Durvasula, and Pauline Nist along with Joe Senz led the management team which proposed and sponsored the new facility. This leadership team was looking toward the future and there was a certain excitement about the work ahead of us, new products, new technology, creative ideas, and new cooperation. There are new systems, business models, accountabilities and many opportunities coming out of our current state of change. The management team was clear that these opportunities need to be met by a knowledgeable and well skilled workforce and the organization needed to provide the environment for continuous learning.

The Boxboro Training and Development Group, formerly known as MSB Education and Training, was formed during the latter part of 1983. Among its first offerings was the "Littleton Forum" series and a course some of you may remember titled, "A Systematic Approach to Digital System Design," taught by William Fletcher.

Today, we deliver seminars, technology and product focused programs, and offer a variety of learning activities to support the technical, business and personal development needs of our individ-

iual employees, managers, as well as intact group development. With the new facilities and equipment in BXB1-1 we are able to offer both the complete VAX/VMS and ULTRIX software curriculums, design and CAD tools, and training on many of the new productivity tools such as DECwindows, DECwrite, DECpresents, and DECdecision. In addition to the many technical offerings we also provide personal and business development programs such as: *Investment in Excellence, Project Management, Stress Management, Doing Business with Europe,* and *Time Management,* just to name a few.

The Training and Development staff are on-site at BXB1 to answer any questions you may have concerning education, training and development and to make arrangements for your training needs.

The Boxboro Training and Development Group

Joe Senz, Manager, 293-5215, MSBCS::SENZ;

Bette Parker, 293-5213, MSBCS::BETTE;

Kristin Cote, 293-5230, MSBCS::COTE.

To review any of the course descriptions listed below:

1. Set Host MSBCS,

2. Username = COURSES (no password required).

To register, contact Kris Cote, 293-5230, MSBCS::COTE or Bette Parker, 293-5213, MSBCS::BETTE.

November 1991 - February 1992

Training & Development Course Schedule

C Programming	October	28 - November 1
VMS Utilities & Commands	November	4-8
UNIX/ULTRIX System Overview	November	14-15
ULTRIX Utilities & Commands	November	18-22
DECwrite Style Files	November	25-26
ULTRIX For VMS Users	December	2-3
Page Layout & Design	December	6
KT Project Management	December	10-12
DECpresent	December	16-17
VMS Internals I	January	6-10
DECwrite	January	13-15
DECwrite Style Files	January	16-17
C Programming	January	20-24
ULTRIX For VMS Users	February	3-4
ULTRIX Utilities & Commands	February	10-14
DECwindows	February	17
DECpresent	February	18-19
Basic DECdecision	February	20-21

Promotions and Awards

Recipients of Digital's Q4 Patent Awards

Back row
(from left to right)
Dave Sager, Rick Gillett, Tryggre Fossum.
Front row
(from left to right)
Paul Wade and Rueysen Lin.

New Book Describes Digital's Patent Application Process and Program

Prospective inventors can learn about Digital's patent program and application process in a book titled, *Intellectual Property: Digital Guide to the Patent Process.* The book, sponsored by the Corporate Intellectual Property Protection Committee (IPPC), was produced by Corporate Research and Architecture (CRA) and Corporate User Information Products, Merrimack (CUIP/MK). It describes patents and other types of intellectual property, and explains why patents are important to Digital. The book tells how to recognize when you may have a patentable invention, how the Invention Disclosure Form (IDF) is prepared and reviewed, how the actual patent application is submitted to the U.S. Patent and Trademark Office, and Digital's patent incentive award program for employee–inventors.

To order the guide, access the VTX Literature Order System (VTX LOS). The part number is EF-A1274-50.

Promotion of Mike Uhler to Senior Consulting Engineer

I am pleased to announce that the Corporate Consulting Engineering Promotion Board has approved my nomination of Mike Uhler to Senior Consulting Engineer for his technical leadership of and contributions to the NVAX architecture development. Mike has contributed significantly in the architecture of the last three generations of VAX processors. Quoting the Board, "we commend him on his outstanding contributions in the Semiconductor Engineering Group and his specific achievements in the development of the Rigel, Mariah, and NVAX microarchitectures."

Mike is NVAX's chief architect and he has contributed several innovations in the development of its very complex architecture. To implement a fully micro and macro pipelined VAX in a single VLSI chip is no small feat. He has made key contributions to this project spanning the architecture development, the performance/ behavioral modeling, design tradeoffs, and verification. NVAX booted VMS on first pass and the architecture has successfully passed several layers of testing. This speaks to the quality, thoroughness, and intellectual excellence and energy that Mike brings to these most complex programs.

Please join me in congratulating Mike on his accomplishments and the high honor this promotion brings.

Dan Casaletto

Bill Samaras Promotion to Consulting Engineer

I am pleased to announce that the Corporate Consulting Engineer Review Board has approved the promotion of Bill Samaras to Consulting Engineer.

This promotion recognizes Bill's significant technical contributions in the area of high speed clocking and data transfers in three VAX development projects, and more recently, to the development of IEEE 896 (Futurebus+) electrical specifications.

Bill has been with DEC for 9 1/2 years, and has been awarded 5 patents. He has made several technical presentations at IEEE conferences, and at internal and external technical seminars. Bill is currently on staff at the University of Lowell Continuing Education Department and teaches *Digital Electronics.*

Charlie Cassidy promoted to Hardware Consulting Engineer

Charlie Cassidy, an engineer well known for his knowledge on solid state disk/memory applications and performance characterics, was promoted to the position of Hardware Consulting Engineer in early 1991.

As a member of the Memory PCU, Charlie was the key technical driver behind Digital's thrust into the solid state disk products. Before the acceptance of this technology, Charlie demonstrated the benefits of solid state disks and initiated the product development.

Charlie has an outstanding knowledge of Error Correction Codes (ECC) and has made significant contributions in this technology, having designed Reed-Solomon codes for multiple symbol detection and correction in solid state disks and block oriented memories.

As a charter member of the XMI ARG, Charlie was a key contributor in the early phases of the XMI development. He conceived of and developed an event-driven queuing model of the bus and memory subsystem. This model helped determine queuing and priority policies. This was the first time that this approach was used at Digital to analyze bus and memory behavior to effect design trade offs.

Additionally, Charlie developed a performance modeling tool for use in the initial stages of memory design. This tool allows quick and easy evaluation of architectural trade offs early in the preliminary design phases prior to behavioral modeling.

Promotion of Catherine van Ingen to Consultant Engineer

I'm pleased to announce that Catherine van Ingen has been promoted to Software Consultant Engineer. Catherine is currently working on the Laser program and is responsible for all VMS related software issues. These include the system error interfaces, the console OS interface, system I/O interfaces and system specific PAL code. She also coordinates system level software debug, insuring that the appropriate pieces of hardware, console, boot code and VMS code appear in the right order. Catherine is the author of several sections of the Alpha System Reference Manual.

Catherine joined Digital in 1987, working on several different projects within HPS/ISB. The most significant of these was the specification of the NPORT architecture which is currently being used on several I/O adapters in support of the Alpha program.

Catherine joined the Laser team in the Summer of 1990 and has been instrumental in the programs many successes to date. Please welcome me in congratulating Catherine on this significant achievement in her career.

Brian Allison

Commercial Computers in Space

Daniel Kilgore
Strategic Acount Mgr. (NASA)

Computers on space vehicles have generally fallen into the domain of special purpose devices. Each computer has to be especially designed and fabricated to suit the mission and environment of each space vehicle. Most space computer systems are based on decades old architecture with 16 bit processing units and data paths. This has caused restricted compute capability and limited memory sizes for space-borne computers. These smaller architecture computers are very difficult to program. Programs are usually written in assembly language of the machine itself. All this creates a situation that fosters expensive special purpose hardware that is programmed with expensive one-of-a-kind software. This software is cumbersome to write, difficult to debug, and very expensive to maintain over the life cycle of a space mission. The space-borne computers have failed to benefit from the explosive computer revolution that has taken place over the last 10 years. These space computers don't reflect the compute power and capability of today's desktop computers and they do not take advantage of today's commercially available software or software development tools. If commercial off-the-shelf software and hardware could be employed in space, big cost savings could be achieved while, at the same time, larger more complex problems in space could be tackled.

The VAX computer used on the shuttle.

In an effort to utilize commercially available software and emerging software development tools, NASA Goddard Space Flight Center, recently flew an experimental VAX computer on shuttle Discovery on STS-39. The experiment, known as Data System Experiment (DSE), tested a modern commercially available computer architecture running standard commercial software in the space environment. DSE flew a Digital Equipment Corp. VAX computer. This computer was designed and built by Raytheon Corp. to withstand the extreme vacuum environment of space flight. It had to be strong to hold up to the vibration of shuttle launch. It had to be conduction cooled to handle the vacuum of space. It had to operate in a very wide temperature range of 0 to 50 degrees C. Aside from these space environmental considerations, the computer is built to a standard VAX architecture specification. The SpaceVAX is equivalent to a commercially available VAX Model 6000/210. It performs at 2.5 Million Instructions Per Second. Although modest by today's standards, the compute capability is many times more powerful than most space computers. The SpaceVAX is configured with 16 Megabytes of memory. It has an Ethernet Controller, a 1553B communication Controller and a SCSI disk controller. Each of these devices are mounted in the VAX BI bus. On the SCSI bus is one 300 Megabyte erasable optical disk. The disk can sustain a 10 Mbps data rate with a removable media.

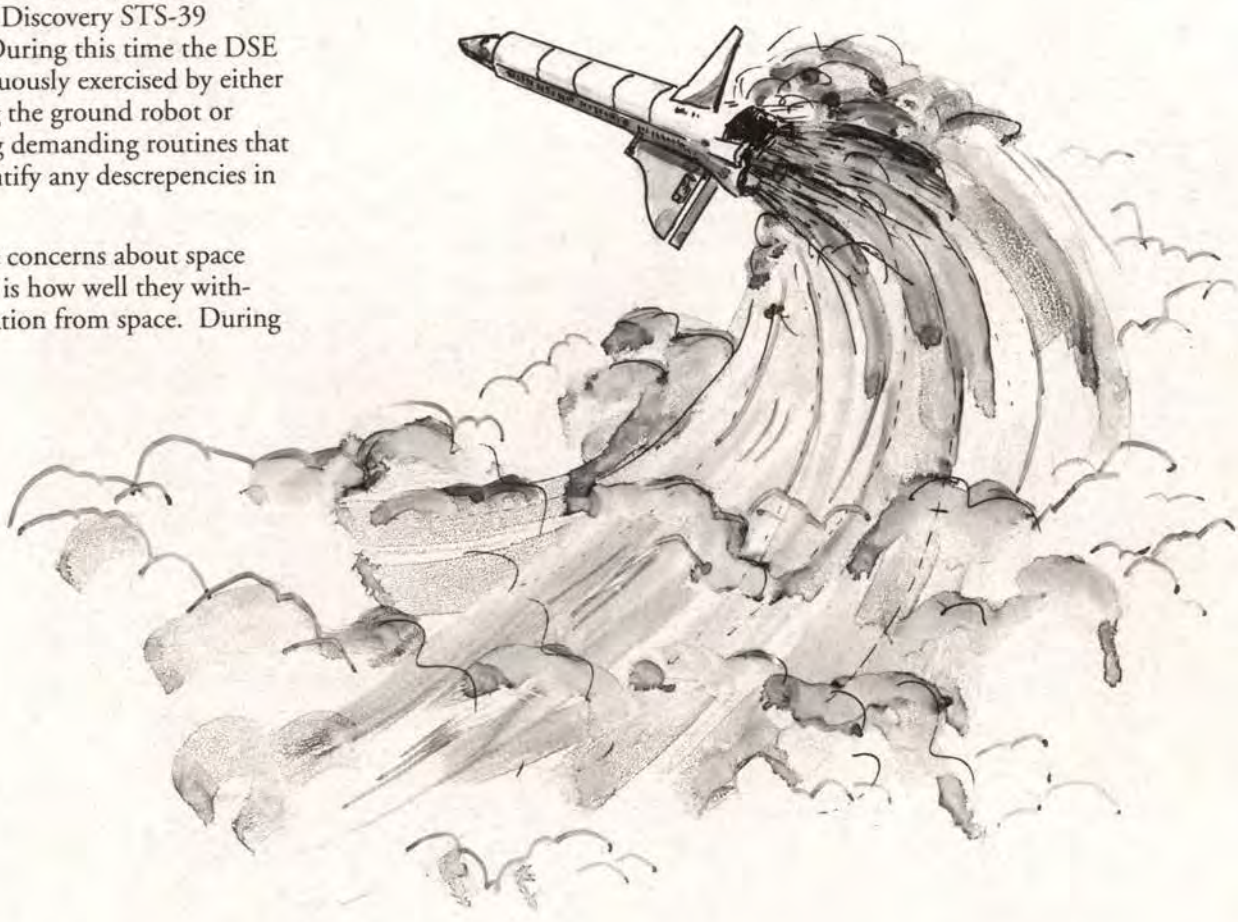
The software environment is based on Digital's standard commercially available VMS Version 5 operating system. Included in the experiment was rotating erasable optical disk that had a 300 Megabyte capacity. This allowed booting the VAX computer from disk, just as is done on Earth. In addition to the operating system, the Ada runtime

system, Ada compiler, and standard VMS tools such as editors, link/loader, symbolic debugger were installed on the SpaceVAX system.

The DSE experiment successfully demonstrated an autonomous robotic program. The operating environment for the robotic program is stored on the erasable optical disk. The actual robot is located on the ground at the Goddard Space Flight Center Robotics Lab. A position toward which the robot was to move was transmitted to the SpaceVAX. The trajectory path was calculated by the SpaceVAX while on orbit and transmitted back to the ground to move the robot. After the robot moved to its new position, an object was placed in the robot work space and that object location was transmitted to the SpaceVAX. Move commands were repeated showing that the SpaceVAX would move the robot around the object without collision. The DSE experiment operated 26 hours and 9 minutes during the Discovery STS-39 mission. During this time the DSE was continuously exercised by either controlling the ground robot or performing demanding routines that would identify any descrepencies in the DSE.

One of the concerns about space computers is how well they withstand radiation from space. During the experiment the SpaceVAX was operated through the South Atlantic Anomaly, an area of increased radiation events, and did not experience any Single Event Upsets. The DSE Mil Std-1553 interface was successfully checked out while the system was on orbit. Another test involved sending Ada source code to the on orbit SpaceVAX. The Ada program was compiled; the Ada library objects were linked into run-time programs, and the programs were run to compute the robot paths. The commercial VAX Ada compiler and link/loader were successfully used on orbit during the DSE experiment. The DSE experiment was a technology experiment to qualify the computer and the optical disk as candidate technology for the Hitchhiker avionics and the OAET Configurable High Rate Processor System (CHRPS) testbed. The Principal Investigator on the DSE is Danny Dalton, Code 735, Goddard Space Flight Center.

The DSE experiment that ran on the shuttle Discovery is one of the first implementations of commercially available computing technology to be used in space. The success of DSE holds the promise of increased computer performance in space and has the potential to leverage commercial software in space. This will provide for better performance with a greatly reduced cost of life cycle maintenance. It will allow software to be developed on standard commercial workstations and have the run-time code transferred to space-borne computers. With such increased capability for space-borne computers, larger tasks can be attempted. Applications in robotics, artificial intelligence, image processing, and Earth Science data reduction can now be considered in the realm of space-borne computing.



VMS Engineering Europe: The Investment in Italy

Catherine E. Foley
VMS Engineering

Launching VMS Development in Italy

In the fall of 1987, VMS Engineering announced its plans to establish an engineering presence in Europe. Engineering in Italy was formally initiated in October 1987 in Turin. Unlike its partner VMS Engineering organization in Livingston, Scotland, the development in Italy was first initiated as part of ULTRIX Engineering. The original project proposal was to explore as an advanced development project the viability of implementing a UNIX™ interface in the VMS operating system. One of the first engineering projects launched there was a VMS POSIX advanced development project. Today, VMS/Italy Engineering provides important "open systems" expertise and focus for the VMS organization.

The team consists of 16 engineers and one manager reporting to Mike Cassily, who is based in the VMS group in Nashua, NH. Many of the VMS/Italy engineers have strong UNIX backgrounds and bring a critical mix of skills and experience to VMS development.

The engineering group originally based in Turin, Italy, is now located in Varese, Italy. Varese is 35 miles north of Milan in the Lakes Region of northern Italy, not far from the Swiss border. A future relocation of engineering to a permanent site in Gallarate, Italy (which is just 20 miles from Milan), is anticipated.

Initiating POSIX Development for VMS

In July 1988, under the direction of Ron Kita, the VMS POSIX prototype was successfully demonstrated in Spit Brook. Soon after that critical milestone, it was agreed to transition the project from an advanced development effort to full product development status. The engineering responsibility for POSIX development transferred from ULTRIX to VMS in the Spring of 1988. Following Ron Kita's relocation back to the U.S. in the Fall of 1988, David Solomon from the VMS group in Nashua joined VMS/Italy Engineering and provided key support and direction in a variety of areas, including project management and local management of the engineering group. Ernesto Colciago joined VMS/Italy in November 1989 as the development manager. Giovanni Giuliani has been the technical leader for the VMS POSIX effort. Andrea Vincenzi, a member of the original POSIX prototype effort, assumed project management responsibilities for Version 1 in April 1990.

Demonstrating An Ongoing Commitment to Open System Standards

The mission of the VMS/Italy group is the development and integration of key base system standards into VMS: the first deliverable is VMS POSIX Version 1.0, which is now in external customer field test. As the engineering group completes the final development for Version 1.0, they have launched the next critical follow-on effort: to provide the interfaces, services, and utilities required for X/Open XPG3 Base Branding certification.

VMS Demonstrates A Commitment To Open System Standards

Catherine E. Foley
VMS Engineering

Increasingly, the user community is looking beyond the view that equates UNIX with openness. More and more, they expect their Open Systems to address portability and interoperability. To meet that need, Digital is phasing in support for additional standards that will allow users to build open systems environments based on VMS. Those standards include OSF/Motif, IEEE POSIX, and others. VMS is committed to meeting user needs for open technology through support of industry standards that meet the customer needs and align well with product direction.

At Spring DECUS in Atlanta, new open systems capabilities were demonstrated for VMS using the VMS Open Systems Demo. It shows VMS support for industry standards that offer key benefits of open systems computing:

- Application portability,
- Interoperability,
- User portability.

Overview of Demo Application

The VMS Open Systems Demo is an inventory control application for a factory that manufactures tables. The application keeps track of parts that are used to make the tables. The demo highlights POSIX, Motif, TCP/IP and NFS industry standards in an environment consisting of:

- A VAXstation 3100 – running VMS DECwindows Motif Version 1.0 and the external field test version of VMS POSIX Version 1.0,
- A DECstation 5000 – running ULTRIX Version 4.1 and DECwindows Motif,
- A SPARCstation 2 – running SunOS Version 4.1.1 and Digital's implementation of OSF/Motif for Sun and referred to as DECwindows Motif for Sun.

The demo was built on VMS using VAXset tools (LSE, CMS, and MMS) and the VMS Linker and is written using the ANSI standard C language and the VAX C compiler. On the ULTRIX and Sun system, the tools *make* and *RCS* were used, as well as the standard compiler *cc* on ULTRIX and *gcc* on Sun.

Elements of POSIX 1003.1 provided in the POSIX-conforming implementations on VMS, ULTRIX, and SunOS enable the demo application to run on these three different systems. DECwindows Motif, which provides a consistent user interface across these three systems, enhances the portability of the application and the user and enables the display of multiple windows and applications.

TCP/IP connects the systems together and supports interoperability of the application across heterogeneous environments. Files that are NFS-mounted from VMS, via the UCX product, are remotely accessible for reading and writing.

Demo Contents and Prerequisites

It is possible to get a copy of the demo software and associated documents. However, due to the size of the demo kit, the demo is not available on the network. Instead, it is orderable as a kit from the SSB. Offering a single kit ensures that all of the software component pieces work together.

The demo kit consists of two TK50 tapes each containing a *backup* saveset of the essential demo files, including: UCX, VMS POSIX executables (which replace certain VMS 5.4 executables), DECwindows Motif for Sun and VMS, VAX C, and all sources and executables for the demo. The kit does not contain the ULTRIX RISC or DECwindows Motif for ULTRIX RISC, nor does it contain the license PAKs for these products.

While the demo kit contains most of what you'll need, there are certain prerequisite components, such as hardware, software, and Product Authorization Keys (PAKs) required to install and run the demo. They are briefly highlighted below:

- *VAXstation 3100* with at least 200 MB of system disk space and 12 MB of RAM.

  VAXstation must be running VMS Version 5.4 with a MUP. A VAX/VMS PAK is required.

- *DECstation* (optional) with at least 200 MB of system disk space and 16 MB of RAM. DECstation must be running ULTRIX RISC Version 4.1 with the MUP. DECstation must also be running DECwindows Motif with the MUP. PAKs for both of the above software components are also required.

- SUN SPARCstation II (optional) with 200 MB of disk space and16 MB of RAM. The SPARCstation must be running SUN OS V4.1.1. No PAKs are required.

  The following documentation is included in the demo kit. PostScript versions of these documents are also available on the network for you to review in advance of ordering the kit.

- Demo Fact Sheet (BULOVA::DOCD$:[POSIX_PUBLIC]fact_sheet.ps)
- Demo Installation Guide (BULOVA::DOCD$:[POSIX_PUBLIC]demo_install.ps)
- Demo Presentor's Guide (BULOVA::DOCD$:[POSIX_PUBLIC]demo_presentor.ps)

Demo Support

VMS Engineering has tried to eliminate the potential for problems by offering a "shrink-wrapped" kit and clearly indicating all prerequisite components. Additional technical support is not possible. Further, organizations who wish to show this demonstration at events, will need to provide their own staffing. It is strongly recommended that the demo only be shown using the recommended hardware and software configurations. If you encounter a show-stopper bug, please contact STAR::MARCHESANO, although no guarantees are made that such bugs can be addressed.

Demo Futures

This demo has been shown at many events and in many forums in addition to Spring DECUS, including the Digital State of the Company meeting, the Corporate Analysts and Consultant's Briefing, the Open Advantage Announcement, and the U.S. Sales Support Symposium. Plans are underway to show this demo at several fall events including European DECUS and Telecom '91. The VMS group is interested in hearing from you should you decide to show the demo at other events. Your feedback from such events is welcome.

VMS Engineering is currently evaluating the possibility of extending this demo to support key commercial strength capabilities available on VMS as contrasted with a UNIX™ environment. Should such enhancements be made, notification of an updated demo will be placed in a future edition of *FOREFRONT*.

The development of this demo has been a team effort, with substantial direction and support received from Peter George, the VMS POSIX teams located in Varese and Marlborough, and the VMS DECwindows team located in Nashua. Valuable contributions were also made by the VMS documentation group, Ken Ballou, Greg Tarsa, Michael O'Bryan, Steve Marchesano, Marion Stanz, Jody Little, and Gil Tardif. Those of us involved with the initial launch of the demo would like to extend our thanks to these and many other individuals who made the demo development and deployment possible and successful.

Demo Ordering Information

The demo is not available directly from engineering. It must be ordered through the established SSB channels. To order the VMS Open Systems Demo kit, please send mail to:

WMOIS::MARTINATH and WMOIS::G_HUCKABY and copy STAR::MARCHESANO.

Your order must contain the following information:

Ship To:	***Your ship-to address***
Subject:	***Order #JS-12191-FT***
Copies:	***Number of copies***
Cost Ctr.:	***Cost center number to be charged****

***Note: a sum of $44.50 per kit will be charged to your designated cost center to cover the cost associated with the kit. Shipping costs, which are also charged to your cost center, range between $1.50- $3.00 for UPS and about $8.00 for FEDex.**

The Open VMS Demo. From left to right, Allan White, Cathy Foley, and Peter George

VMS POSIX – A Cornerstone of Open Systems

Don Topaz
VMS Documentation

***Q:** What operating system is it if your files have names like "/cont/usr/user/smith/sales.1991.dat," if your application forks a child process instead of creating a subprocess, and if you list the files in your directory by entering the command "ls" (using lowercase only, please!)?*

***A:** If you can also use volume shadowing, VAXclusters, and VMS system services and layered products, then the answer is a VMS operating system using VMS POSIX.*

VMS POSIX is a key element in Digital's Open System capabilities, offering customers the portability of open systems along with the commercial strength that is the hallmark of VMS. VMS POSIX offers users the features of VMS, plus the capability of working in an open environment.

What is the difference between POSIX and VMS POSIX?

POSIX is an industry response to the need for application portability. The user community - that is, our customers and potential customers - want to run the same application using different computers and different platforms. The systems are not compatible (even UNIX systems on different platforms are often incompatible), so individual versions of the application source code must be developed and maintained for each platform. The cost can be overwhelming.

The solution to the problem is a 3-way agreement among standards organizations, software vendors, and programmers:

- Standards organizations agree to develop and maintain functional specifications and syntax rules for software.
- Software vendors agree to produce an environment that will run any application that conforms to those specifications.
- Programmers agree to use only the facilities included in the standards and to abide by the syntax rules specified by the standard.

POSIX is the response of the standards organization; it is a set of standards and draft standards that have been generated by the IEEE and ISO. VMS POSIX is one of Digital's responses as a software vendor; it provides the environment to develop and run applications conforming to the POSIX standards. In short, the POSIX standards serve as the functional specification for the software product called VMS POSIX.

VMS POSIX Version 1.0 includes support for standards and draft standards for the system application programming interface (POSIX 1003.1), shell and utilities (1003.2), and real-time programming (1003.4). POSIX 1003.1, which includes all of the ANSI C language as well as a series of system services, has been approved as a final standard. POSIX 1003.2 and 1003.4 are mature drafts that are currently being considered and evaluated by the standards community.

The POSIX standards and drafts are based on the UNIX operating system, and POSIX 1003.1 and 1003.2 are similar to the common part of most UNIX systems. With VMS POSIX, a user can develop and run applications that can also be run on other systems (including UNIX systems) that support the same open standards and drafts.

Portability: The Key Advantage of POSIX

From a customer perspective, a software product that conforms to a POSIX standard provides the opportunity to write and maintain a single version of source code that will run on multiple platforms. Source code that strictly conforms to POSIX standards can be compiled, linked, and run on any platform that offers a POSIX-conformant product, such as VMS POSIX.

For example, an application created by the VMS Engineering group and shown at Spring DECUS demonstrated the portability and interoperability of an application that conforms to open standards. Using a single version of source code, the demonstration application was compiled, linked, and run concurrently on a VAXstation (VMS), a DECstation (ULTRIX), and a SUN workstation. The application, which complied with the POSIX, TCP/IP, and Motif standards supported on each of the three platforms, demonstrated that the open system's theory of portability and interoperability can, in fact, work in practice.

For example, suppose a customer's application is to be run on both VMS and other platforms that support the POSIX 1003.1 standard. The customer would then write source code (or modify existing code) that strictly conforms to the POSIX standard. (An application conforms to the POSIX standard when it is written in C and uses only the services and functions listed in the POSIX standard.) The source code can then be compiled, linked and run on any platform that supports the POSIX 1003.1 standard.

By extension, an application can be readily ported to all of the platforms on which it will run when the application conforms to the standards supported by all of the platforms. For example, if all of the target platforms support the POSIX 1003.1, TCP/IP, and Motif standards, then the application is fully portable when it includes only the facilities defined by any of those standards.

For application designers, the question of portability presents a series of challenges. When considering an application that will run on different platforms, the application designer begins by identifying the standards that are supported by all of the target platforms. This step establishes the standard interfaces (for example, POSIX 1003.1, TCP/IP) that could be used in an application that can be ported without modification on each platform. Then, the designer considers the purpose of the application, the suitability of the available standards to achieve that purpose, and the trade-offs that are inevitably involved.

Features of VMS that are not explicitly referenced in the source code (for example, disk shadowing and VAXclusters) can be used freely in a portable application. An application running on VMS that conforms to standards such as POSIX can take advantage of these features, and the same source code can be used on other POSIX-conformant platforms (where, obviously, the shadowing and cluster features would not be available). On the other hand, the use of system-specific features in the application code (for example, VMS callable utilities or proprietary layered products) would affect the portability of an application, requiring a revision to the source code for other platforms. The trade-off considerations, therefore, are essentially a comparison of the advantages of portability to the advantages of system-specific features.

From an engineering perspective, the development of VMS POSIX has presented a series of challenges. For the most part, this has been due to the functional specifications (that is, the POSIX standards), having been developed by a group outside of Digital Software Engineering. To implement the functional specs, the VMS POSIX engineering group was required to develop innovative solutions to issues such as a file system that must accept file names such as "sales.march.1991.dat" and process generation that requires new processes to be created as independent child processes and not dependent subprocesses.

Using VMS POSIX Interactively

VMS POSIX provides both an interactive interface and a callable interface. The interactive interface, a shell based on the draft POSIX 1003.2 standard, is an environment that will seem familiar to UNIX-based users with many of the same functions and features as the Korn shell. The commands and utilities available in VMS POSIX include both those that have analogs in the VMS environment (such as ls and cd, comparable to the DCL- level DIRECTORY and SET DEFAULT commands), as well as features and utilities that are unique to UNIX, including pipes and complex utilities (such as awk). The vi text editor and application development utilities such as make, c89 (the POSIX equivalent of cc), and ar are also included in the VMS POSIX product.

The interactive user who wants the benefit of both the DCL and POSIX environments is well served by VMS POSIX. A user can move back and forth easily between the VMS POSIX shell and DCL environments, issue DCL commands from the VMS POSIX shell, or issue POSIX commands from DCL level.

On the other hand, a user can remain at either the DCL or POSIX command level, executing POSIX programs from DCL-level or DCL applications from the VMS POSIX shell.

Programming with VMS POSIX

The POSIX callable interface is based on POSIX standard 1003.1 and draft standard 1003.4, and it also provides access to the utilities defined by 1003.2. POSIX 1003.1 and 1003.4 include all of ANSI C, a set of system services, plus a set of real-time programming services. (Future POSIX standards may support language bindings to Ada and FORTRAN; at this time, however, all POSIX applications are written using C.) VMS POSIX uses the VAX C compiler, and the applications are linked to runtime libraries and header files that are specific to VMS POSIX.

A POSIX application program may use some concepts that are different from other applications running on a VMS system, for example:

- To execute an image independent from the main body of the application program, POSIX applications require a new, child process to be generated by a fork, compared to the VMS procedure of creating a subprocess. Although child processes are in some ways analogous to a subprocess, a child process in the POSIX environment is an independent process that can continue to exist even if the parent process is terminated.
- Files can be accessed using a container file system. The VMS POSIX container file system, which provides portability for POSIX-conformant applications by accepting any path or file name allowed by the POSIX standards, serves as a mapping mechanism, translating the POSIX path name to a file name compatible with VMS.
- The POSIX 1003.1 standard uses the concept of signals to inform a process that an event such as an error or the termination of a child process has taken place. For each one of a defined set of signals, the application determines the action to be taken when a signal is delivered to the process: the process might be terminated, temporarily stopped, or continued, or the signal itself might be ignored or intercepted by the application. Signals in the POSIX environment are analogous to asynchronous system traps (ASTs) in the VMS environment. Although ASTs may provide a more robust set of capabilities than do signals, signals have the advantage of portability: they will function exactly in the same way on any POSIX-conformant system.
- For realtime applications, VMS POSIX is based on draft 9 of the POSIX 1003.4 standard. This draft standard includes synchronization functions such as binary semaphores (used to control access to system-wide resources), clocks and timers (which let an application synchronize and coordinate activities according to a predefined schedule), and priority scheduling (which gives the application control over execution sequences).
- VMS POSIX also includes the interprocess communication functions of event notification, message queues, and shared memory that are in draft 9 of 1003.4.

Target Market and Delivery Schedule

The nature of the VMS POSIX product raises important questions about its target market – would the product appeal more to VMS-based users or to UNIX-based users? The decision to focus on existing VMS users was based on feedback from marketing organizations and an analysis of the VMS POSIX product. Such users might typically have new or existing applications that would be run on VMS and other platforms; VMS POSIX would provide them with an opportunity to generate applications without the need to revise the source code for each platform while retaining all of the benefits of VMS for other applications. Interest from UNIX-based users is also anticipated. These users could be attracted by VMS features such as volume shadowing and VAXclusters, which can be used in a POSIX-conformant application.

VMS POSIX is currently in external field test and is expected to be available shortly after VMS V5.5 is released.

Customers Begin Migration to Alpha

Paul Steeves

Customers have already begun to move applications onto the Alpha VMS environment as part of the Alpha VMS migration research project! In fact, one application has been ported to run on the Alpha simulator — and it only took two days to port!

It is common wisdom that a key factor in the success of a new system is the number and quality of the software applications that are available with it upon release. Customers purchase systems to run the applications that help them succeed in their respective businesses. Digital is committed to ensuring that the Alpha systems are introduced with the applications that are required to help our customers succeed. To do that, third party application providers must be assisted in getting their applications running before the initial release.

Porting an application from one platform to another sometimes involves changing the application to account for differences in the platform. In the case of moving from VAX VMS to Alpha VMS these changes have been minimized by the design of the new system and the fact that the operating system is essentially the same. However, in cases where an application took advantage of specific features of the VAX hardware architecture, some changes may be required.

The Alpha migration research project is an effort by Alpha VMS engineering & product management to learn about the technical issues around porting a non-Digital application early in the development cycle in order to use this knowledge to simplify the effort for the majority of customers. It is the first step in a larger application rollout plan and is designed to feed the knowledge gained into the organizations responsible for the subsequent phases of the rollout.

The project involves bringing a small number of customers (five) onto the VMS development floor to work side-by-side with VMS engineers (and other support people) to port the customer's application. The migration process gets "jump started" by bringing the customer experience and VMS expertise together early on. The overall project goals are:

- ***Assist the customers in porting their applications from VAX to Alpha.***
- ***Prove the feasibility and simplicity of porting non-Digital applications.***
- ***Learn as much as possible about the porting process — where do customers have difficulty, what skills are needed for Digital personnel to assist them?***
- ***Learn what tools are needed by customers to perform the port — and refine those tools.***
- ***Determine the viability of the cross-development environment for customers, for both Alpha Resource Center use and customer-located environments. (Cross-development involves the use of existing VAX hardware to develop Alpha-targeted applications.)***
- ***Transfer all the knowledge gained from the research to the appropriate organizations involved in the subsequent migration efforts.***
- ***Have the applications ready when the hardware becomes available.***

To gain the greatest amount of benefit from the small number of customers, the five applications were chosen with a spectrum of migration characteristics in mind:

- One is highly portable (written in C, no VAX dependencies) in order to prove how easy it is to move from VAX to Alpha.
- One is a highly portable FORTRAN application to gain experience with the FORTRAN migration.
- One is "VAX dependent" (uses ASTs, atomicity assumptions, etc.) in order that we could encounter the more difficult aspects of moving an application and find the easiest solutions for the subsequent customers.
- One is partly recompiled, partly translated to test this migration model.
- One is a DECwindows application, to gain experience with DECwindows migration.

This is a six-month research project that stretches from this past June until December of 1991. At that point, the applications will be ported (on a simulated environment), and ready to be run on early hardware. The knowledge acquired through the project will also have been transferred to the porting centers and support groups that need it.

To guarantee the transfer of knowledge, VMS engineering has included the appropriate organizations from the earliest stages of the project. The Performance and Porting Engineering Group (P/PEG) and the Colorado Support Center have both provided the bulk of the direct support to the five customers. Additionally, an open-invitation forum about migration progress is held on a bi-monthly basis, monthly reports are made available, and a daily log of the customer progress is kept in a notes file. Several groups have already benefited from the research. The VMS and Alpha Migration Tools (AMT) documentation groups have both received extensive feedback on the documentation the customers have used. The customers also provided extremely useful feedback on the week-long training course they attended (in general, they believed it needed a more high-level language focus).

Early Success

One customer application, a code management tool, is already up and running Alpha native code on the Alpha simulator. The port was accomplished using the DECC cross compiler and the Alpha cross linker.

This application is a 100% "C" language implementation which makes extensive use of Runtime Library and System Services, but contains no dependencies on VAX architecture. As a result, only a few small changes to the source code were required to achieve successful compile and link. Most of those changes were due to ironing out the migration process and will likely disappear when Alpha VMS and the porting tools mature.

Other Customers

In total, five customer applications were selected for participation in the project. They consist of three highly portable applications (the code management application being one), one VAX dependent application (relies on many specifically VAX architecture features), one partially portable/partially translated application (an environment that will be used by some early customers waiting for later compilers). They all participated in a week-long training course in June and most have already begun to port. The following describes two of the applications that have already begun work as part of the project.

The VAX Dependent Application

This application is estimated to require 6 man months to migrate to Alpha. It is designed to be portable and currently runs on twelve different vendor platforms. The code is layered in such a way that only10% of it is machine specific. That code takes advantage of several VAX dependencies that will require redesign to work on Alpha.

Because of the extent of the work involved, this customer will be working in a cross-development environment at their site in addition to working in the Nashua facility. As a test of remote cross-development, they have been loaned a VAX 4000-300 system to run the cross-development tool kit. The success of this remote development effort will be important in understanding the potential for future remote porting efforts. For any applications that require several months worth of work it is unlikely that a company can free up their best engineers to work off site in a porting center. For early porting efforts the cross tool kit may be used at the customer sites for initial development and at the supported porting center (with the real hardware) for final debug.

The Partly Ported/Partly Translated Application

One of the tools available for migration is the software translator (also known as VEST) which takes non-privileged VAX executables and translates them into Alpha executables. Some customers will choose to use this method to migrate applications. Another option is to translate part of an application and the CAD application that is a combination of FORTRAN and C and is a good candidate to test this partly ported/partly translated case. Eventually we will recompile the entire application, but the customer agreed to initially translate only part of the application for the purposes of research.

The initial translation of the entire image went very smoothly. They were able to translate the entire application and get it running in the debug environment in less than a day. They had no trouble using what they had learned in training and applying it to the actual use of the tool on their application. At the end of the first day the customer stated, "I found VEST to be very simple and straightforward to use."

The ported part of the application also progressed rapidly and was tested separately. This customer will be returning in the Fall when the native development environment supports the ported image communicating with the translated image. At that point we will begin to gain insights into how well this mixed enviroment works and where we need to make changes to simplify the migration.

Cross Development Tool Kit

One goal of the research effort was to test the viability of cross development tools in helping with early application migration.

We have found customers are interested in the cross compilers long term because they will allow them to keep VAX/ALPHA sources on one system and build both the ALPHA and VAX versions of the application. There is also a strong need for the cross tools if the idea of centralized porting centers with remote customer development is going to be viable. See below for customer-participant responses.

Ongoing Effort

In the coming months the research on the VAX dependent application will be fully staffed by the customer and accelerating. This work will deliver a mother-lode of crucial information for use by the porting centers with some of Digital's most important software partners. The FORTRAN application will be complete as well, giving us a better indication of what is in store for the many FORTRAN application vendors.

The more we learn now about the Alpha migration, the easier it will be for all of our customers, both application vendors and end users, when we invite them to move with us onto the technology that will carry VMS through the '90s.

The following are customer-participant responses to the question: "Could you use the development tools at your site?"

"You betcha. The sooner, the better."

"Yes. It would help to become familiar with the tools and be able to port much of our software before we get the hardware."

"These tools are not only useful for an alpha port, but would also be highly useful for some of our DECstation port work... My guess from what I've seen is that we can have 98% of the port done before the first seed machine shows up."

"We absolutely need these tools at our facility at least 9 months before we could ship an application."

"One thing that would really help now is having the DEC C compiler available. I'm not thrilled about porting to a new platform and using a new compiler at the same time."

DECram For VMS, V1.0 Performance

Sandeep Deshmukh
Senior Software Engineer

This article examines the performance of DECram for VMS, a RAM disk product from DEC, and compares it with Turbodisk, an equivalent product from EEC Systems Inc., and with magnetic disks on VAX/VMS systems. The VAX platforms used for the comparative study were: VAX 4000 Model 300, VAX 6000 Model 510 and VAX 9000 Model 410.

Based on internal testing, DECram delivers significantly better I/O performance compared to magnetic disks, and offers comparable performance to Turbodisk.

A computer system performance is dependent on the CPU speed and I/O subsystem speed, along with other factors. For a CPU intensive application the I/O subsystem performance does not play a major role. For an I/O intensive application, a very fast CPU cannot deliver a good system throughput if the I/O subsystem is slow. Although the trend thus far has been for CPU speed to double every two years, I/O subsystems, speed have not seen such dramatic improvements. As a result, CPU intensive applications enjoy the luxury of using fast CPUs for higher throughput, whereas I/O intensive applications have encountered only marginal speedups.

There are some software and hardware solutions that can increase the performance of I/O intensive applications. RAM disk is a software solution that reduces long disk accesses by accessing the frequently used files, which can be referred to as "hot" files, from the system memory. The hot files have to be identified and copied to the system memory reserved for RAM disk. By moving these hot files to the memory, an I/O transaction becomes a memory access performed at a much faster rate. Since the cost of memory has decreased rapidly, this solution is viable to deliver better performance. A solid-state disk is a hardware solution that uses dynamic semiconductor memory to store the data, instead of the slower magnetic storage elements.

Description of DECram for VMS

DECram for VMS (DECram) is a memory-resident disk device driver used to create and manage memory-resident disks. Frequently used files can be accessed much faster from DECram devices than from physical disk. DECram devices can be accessed through the VMS file system just as physical disks are accessed, requiring no change to applications or system software.

DECram software requires one page of system space in memory per block of disk space allocated. The amount of memory dedicated to a DECram device is determined by the number of blocks needed for a particular application file and a small amount of memory for the system resources required by each DECram device. To realize I/O performance improvements, frequently accessed files in an application have to be moved to the DECram device and the application has to point to those files to access them.

Data placed on RAM devices is volatile. Therefore, read-only files and temporary scratch files are good candidates for DECram. If system crashes during the application run, it can be restarted without losing any critical data or results. With the use of RMS Journaling, files moved to a DECram device which need to be non-volatile can be journaled to allow for recovery after a system failure.

DECram devices can be used as local devices on nodes within a VAXcluster, however, due to the characteristics of a RAM disk, DECram devices are not served in a VAXcluster nor can they be used as a shadow member.

Test Methodology

The effectiveness of DECram was measured by comparing the execution times of various benchmarks with magnetic disks. Comparisons were done for the following VAX platforms in standalone configuration: VAX 4000 Model 300, VAX 6000 Model 510 and VAX 9000 Model 410. The performance metric was elapsed time in seconds. CPU time is also provided to show how I/O intensive each benchmark is and how the CPU utilization changes with the use of a RAM disk. The execution time using magnetic disks is referred to as the baseline time.

Typically DECram disk devices would be used to store only read-only or scratch files, not the whole application including the executable. For that reason, small synthetic benchmarks were not chosen which can be completely transferred to the RAM disk and run from there to deliver 1500 to 1600% performance improvement. Rather, large benchmarks which only use input files or scratch files on the RAM disk were chosen for the testing.

Configuration

- DECram for VMS, V1.0
- Turbodisk V5.00-08
- VAX C V3.2
- VAX Cobol V4.4
- VAX 9000 Model 410 running VAX/VMS 5.4-2, 256 MB of memory, six RA90 disks on a KDM70 local controller.
- VAX 6000 Model 510 running VAX/VMS 5.4-1, 384 MB of memory, six RA90 disks on HSC70.
- VAX 6000 Model 510 running VAX/VMS 5.4-1, 384 MB of memory, two RF72 disks on XMI-based KFMSA controller.
- VAX 4000 Model 300 running VAX/VMS 5.4-4QN, 128 MB of memory, six RF72 disks on an embedded DSSI controller.

Observations

CHEMPAK

CHEMPAK is a molecular chemistry application written in Fortran. It calculates integrals and derivatives of functions to determine the characteristics of electron orbitals of molecules.

This is a very I/O intensive application. It creates four scratch files, totaling 10,000 blocks, to be used in further calculations. The storage and retrieval of data from these files generates considerable I/O traffic. The scratch files are deleted at the end of the run. This behavior is ideal for the use of a RAM disk because the size of the scratch files is not too much to reserve from memory and that the volatility issue of RAM disk does not arise for scratch files. (See Figure 1.)

Results

See Table 1 listed below.

The baseline configuration refers to the setup using magnetic disks, RAM disks being disabled. Note that the baseline elapsed time on the VAX 9000 was higher than that on the VAX 6000. This is because for the VAX 6000 baseline testing the I/O subsystem contained RF72 disks and for the VAX 9000 baseline testing it contained RA90 disks. Since this is a very I/O intensive benchmark, use of RF72 disks, which has shorter access times than the RA90 disks, causes this benchmark to be executed faster on the VAX 6000.

Disk Configuration	CPU time	Elapsed time	Percent CPU (%)	Performance Improvement
VAX 9000 Model 410				
Baseline	58	570	10	
DECram	59	191	31	3x
Turbodisk	61	191	32	3x
VAX 6000 Model 510				
Baseline	121	503	24	
DECram	123	222	55	2.3x
Turbodisk	123	221	55	2.3x
VAX 4000 Model 300				
Baseline	214	591	36	
DECram	218	308	71	1.9x
Turbodisk	218	307	71	1.9x

Table 1.

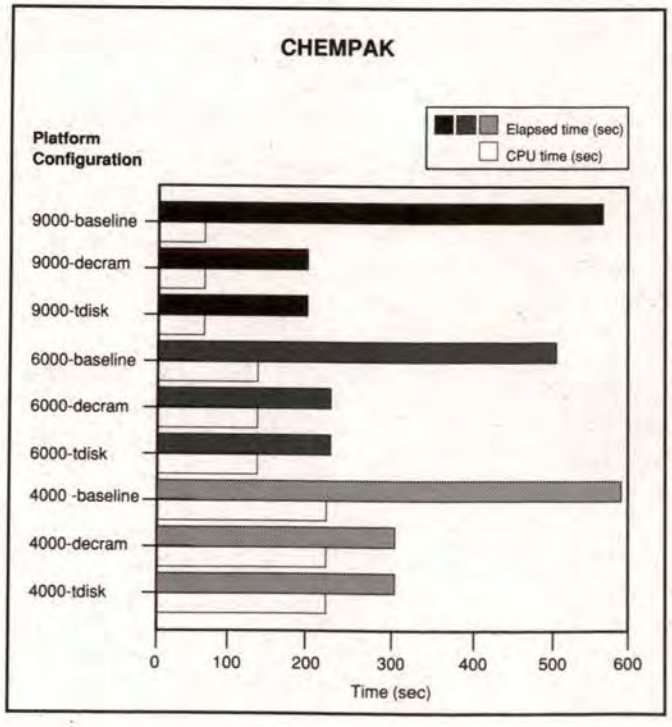


Figure 1.

RAM disks used 10,000 blocks of memory to store the scratch files. DECram delivers about 3x improvement in performance over the baseline configuration. DECram and Turbodisk provide about the same performance improvements (within 1%). The VAX 9000 delivers the best performance improvement using DECram. This is because when the hot files are moved to the memory, the application becomes more CPU intensive and a faster CPU can deliver more transactions leading to a reduced execution time.

GCC

GCC is based on the GNU C Compiler version 1.35 distributed by the Free Software Foundation. This benchmark measures the time it takes for the GNU C Compiler to convert 19 preprocessed source files into optimized SUN-3 assembly language (.s files) output. GCC is representative of the work performed in the software engineering environment and can be used to predict how well a system compiles code. (See Figure 2.)

In this case, 15,000 blocks were allocated to RAM disks. The executable and 19 source files were copied to the RAM disks.

Results

See Table 2 listed below.

DECram delivers 2.8x improvement over the baseline configuration. This benchmark does considerable I/Os to the executable and source files, hence we notice the performance enhancements with DECram enabled, especially for a fast CPU. DECram and Turbodisk deliver about the same performance.

VAX 9000 Model 410		
Disk Configuration	Elapsed time	Performance Improvement
Baseline	133	
DECram	47	2.8x
Turbodisk	47	2.8x
VAX 6000 Model 510		
Disk Configuration	Elapsed time	Performance Improvement
Baseline	188	
DECram	99	1.9x
Turbodisk	100	1.9x
VAX 4000 Model 300		
Disk Configuration	Elapsed time	Performance Improvement
Baseline	243	
DECram	176	1.4x
Turbodisk	176	1.4x

Table 2.

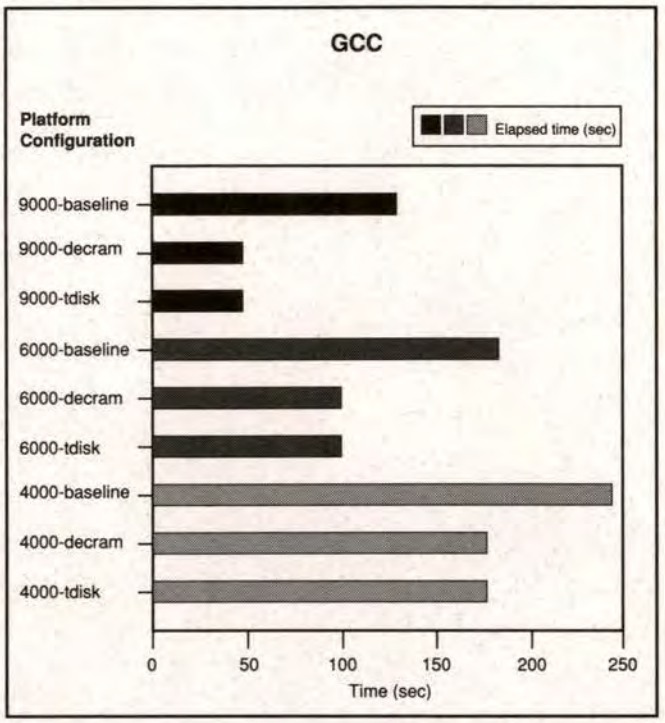


Figure 2.

Dun & Bradstreet General Ledger

The Dun & Bradstreet General Ledger Update (Figure 3) is part of the FABS suite of benchmarks. It simulates the transaction read, edit, and posting of 24,000 records to a 26,000 record GL master file. This test is CPU intensive, consequently the improvement with DECram enabled is expected to be lower than the other observations (CHEMPAK and GCC).

Considerable I/Os are done on the GL master file which is 40,000 blocks big. Therefore, 40,000 blocks were allocated to RAM disks and this file was copied to it.

Results

See Table 3 listed below.

DECram delivers 1.4x improvement in performance over baseline configuration for this benchmark. Here, note that mainly for VAX 4000 and VAX 6000 this benchmark is CPU intensive making the scope for improvement with RAM disk limited. DECram and Turbodisk performance is almost equal.

Conclusions

- DECram for VMS can provide up to 3x improvement in performance over the baseline configuration of magnetic disks, based on the benchmarks tested.
- Significant performance enhancement possibility when using DECram for VMS with I/O intensive applications.
- Performance enhancements are seen when DECram for VMS is enabled for CPU intensive applications, but not as great when compared to using DECram for VMS with I/O intensive applications.
- DECram for VMS is a competitive product.

Availability

DECram for VMS, V1.0 became available in July, 1991; for additional information please contact:

Lynn Moore
DECram for VMS Product Mgr.
Digital Equipment Corporation
110 Spit Brook Road
Nashua, New Hampshire
03062-2698.

VAX 9000 Model 410

Disk Configuration	CPU time	Elapsed time	Percent CPU (%)	Performance Improvement
Baseline	128	220	58	
DECram	132	152	87	1.4x
Turbodisk	132	153	86	1.4x

VAX 6000 Model 510

Disk Configuration	CPU time	Elapsed time	Percent CPU (%)	Performance Improvement
Baseline	293	384	76	
DECram	289	311	93	1.2x
Turbodisk	290	313	93	1.2x

VAX 4000 Model 300

Disk Configuration	CPU time	Elapsed time	Percent CPU (%)	Performance Improvement
Baseline	589	669	88	
DECram	568	598	95	1.1x
Turbodisk	566	593	95	1.1x

Table 3.

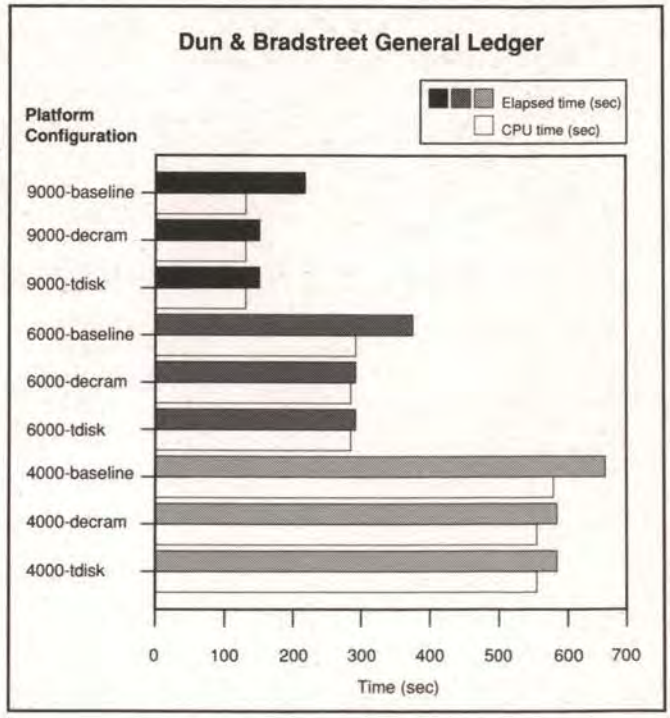


Figure 3.

digital

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MARLBORO MA 01752-3011

FOREFRONT

VAX VMS Systems and Servers
Systems for the '90s
Q3-Q4 FY92

A Computing Architecture for the 21st Century

Alpha

"Today the paradigm shifts. This marks one of the most significant announcements in Digital's history. We now have the fastest machines at the lowest price per unit of computing power," Ken Olsen.

"Digital's current products (VAX, MIPS, X86, etc.) are the best investment today and offer a secure stepping stone to the leading computer architecture for the future," Bill Demmer.

Bill Demmer Announces Four New Vice Presidents

FOREFRONT

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Contents

Welcome to The World of Alpha

Bill Demmer
Vice President

On February 25, 1992 we introduced the Alpha architecture, the world's fastest microprocessor, and new open business practices for licensing and selling Alpha technology. Customers can now see Digital's clear vision for the future of computing, and a consistent product strategy based on leadership open systems.

What is Alpha?

Alpha is a new, open computer architecture that positions Digital as the industry leader for the rest of the decade and into the next century. Alpha will cover multiple operating systems, desktop, super computers, embedded real time, LAN products and more.

Both the Alpha architecture and the first Alpha microprocessor were announced simultaneously in three geographies – South Queensferry, Scotland, Hudson, Massachusetts and Tokyo, Japan. This first announcement sets the foundation for Alpha to become the leading industry standard 64-bit computer architecture.

Specifically, the February 25 announcement included these four strategic items:

1. Digital has the world's first 64-bit, super-pipelined, superscalar RISC microprocessor. This microprocessor is the industry's fastest, supports the largest address space, and has the widest data pipeline.

2. As proof of our confidence in our open architecture and open systems, Digital will license the Alpha architecture and sell Alpha chips. This means that vendors in addition to Digital will be manufacturing and selling Alpha chips, and system houses in addition to Digital will be building and selling Alpha systems.

3. Digital will, by the end of 1992, be selling Alpha systems, desktop to data center, and these systems will be supported by both VMS and OSF. These operating systems will be available to other vendors selling Alpha systems.

4. Digital welcomes Cray and Kubota as the first of our system partners. Cray and Kubota will be developing and selling Alpha systems to complement Digital's system products.

This announcement sets the vision for Digital's future. We can use this vision today to invigorate sales of Digital's current products and services. The long-term objective is to make Alpha the de facto industry standard for 64-bit computing.

This is an exciting new direction for Digital. Customers can appreciate the leadership position that Alpha commands and they can see how to buy and use Digital's current products to begin their Alpha implementations.

Alpha: A Computing Architecture for the 21st Century

Dick Sites
Linda Lindgren

Editor's Note: In this article, one of the two designers of the Alpha architecture describes why Alpha will be one of the major computer architectures that take customers into the next century.

Subsequent articles in FOREFRONT will describe the superior characteristics built into other levels of the Alpha implementation, such as: chip design, fabrication, and compilers.

Throughout the history of computing there have been many different computing architectures, optimized for many different kinds of technology and applications. Some span only one system and last for only one generation. Others, like IBM's System 360 architecture, have delivered a consistent computing environment for more than two decades. Still others, like the VAX VMS architecture, are able to incorporate new performance technologies (clusters, integrated vector processing, and multiprocessing) – to last more than a decade – and to span a broad range of systems.

A Computing Architecture for the 21st Century

Even the best computing architectures, however, don't last forever. In fact, the most popular computer systems in the world today, both complex instruction set computers (CISC) and reduced instruction set computers (RISC), share an underlying limitation in their architectures that makes the development of a new computing architecture inevitable: they are all 32-bit systems.

While systems based on both CISC and RISC 32-bit architectures will continue to deliver leading-edge performance for years to come, they will not be able to keep pace with improvements in memory technology to meet the demands of the "supercomputing-like" applications of the 21st century, including: visualization, very large databases, imaging, multimedia, simulation and modeling.

Characteristics of a 21st Century Computing Architecture

A careful analysis of past computing architectures, as well as a projection of current technology trends, yields a number of core characteristics that a computing architecture must have to be viable into the 21st century.

In the 60s and 70s, the most successful computing architectures were designed for a single, controlled, and proprietary operating environment. The goal was to provide binary compatibility across a range of systems – and multiple generations. This compatibility over time and across systems protected customer investments in applications and operational expertise, as well as providing a stable environment for application development.Despite being optimized for a single, "proprietary" operating system, these architectures supported many different languages, a broad range of applications, and a broad range of systems. VAX VMS is, of course, the best example of this kind of computing architecture, and the benefits to users, developers, and IS managers are well known.

In the 80s, new computing architectures focused on exploiting performance for single-user PCs and workstations. The development of RISC architectures achieved new levels of price/performance. Compared to the broad multi-language

and multi-system range of the "computer family" architectures of the 60s and 70s, however, architectures in the 80s focused on a narrow range of systems: PCs, workstations (and, only recently, small servers); and a narrow range of operating environments: MS-DOS or the UNIX operating system. For the most part, these architectures did not provide binary compatibility for applications from one implementation of hardware to the next. Nor do the operating environments they support offer the robustness required to run critical applications.

To be successful in the 90s and beyond, a computing architecture must deliver the benefits of both the "family" architectures of the 60s and 70s and the highly competitive "price/performance" architectures of the 80s. In other words, a 21st century architecture will provide both investment protection and competitive performance across a broad range of systems.

The following are some of the characteristics of a 21st century architecture.

A 25-Year Design Horizon

First and foremost, a 21st century computing architecture will be designed, from the beginning, to last at least 25 years.

Customers have roundly and soundly rejected the "just recompile with each new implementation" mentality of computing. In general, most major computer users are unwilling and unable to undergo a major technology transition any more frequently than once every ten years – and only then for significantly more performance or functionality.

A computer architecture that delivers competitive performance *and* binary compatibility for 25 years would be highly desirable. But is it possible?

The IBM System 360 and 370 family of computers, designed in the 1960s, has provided a viable, binary compatible computing family for 28 years.

Digital's VAX systems have not only provided binary compatiblity across a broad range of systems for 15 years, they deliver the best price/performance in the industry today. And VAX systems will continue to deliver both binary compatibility and highly competitive price/performance for several more years.

Given these past accomplishments, designing a 25-year architecture certainly seems feasible. Nevertheless, the challenges of designing a computing architecture to last the *next 25 years*, with no compromise in performance, should not be minimized.

Today, there are many more computer technology vendors and many, many more computer users than when the System 360 or VAX were designed. Technology, markets, and applications are changing much more rapidly and unpredictably than they were even five years ago.

In fact, because there are so many fast changing, interdependent variables, a very important characteristic of a 21st century computing architecture is that it does *not* predict what will happen in world computing (or the world itself) over the next 25 years.

In other words, no assumptions about technology and no features that could get in the way of future innovation or implementation can be built into the architecture.

In the 1990s, a 25-year architecture must start with the "cleanest of possible slates." Every "classic" computing architecture technique must be re-examined. "Natural" assumptions about instruction sets and physical memory must be discarded. For the architecture to endure, instruction decoding and data paths are stripped down to their very simplest levels.

A 64-Bit Architecture

Most people in the industry agree that the next computing architecture will be a true, full-speed 64-bit computing architecture, including: 64-bit data, 64-bit registers, 64-bit addressing, 64-bit operation, and 64-bit compilers.

But is a 64-bit architecture "big enough" to last 25 years?

Given the historical "consumption" of 6/10ths of a bit per year, moving from a 32-bit to 64-bit architecture should actually provide a comfortable 50 years of growth.

The move from a 32-bit to 64-bit is not just a doubling, *it provides four billion times the address space* – and the architectural underpinnings and performance to last 25 years.

Performance Scaling x 1,000

A computing architecture for the 21st century must have a very fast implementation. Not just the first generation, *but every implementation,* must be among the most competitive, in terms of price and performance, for its time.

In fact, we believe a 21st century architecture must be able to scale effectively over a range of 1 to 1000.

Over the last twelve years, computing performance has improved by a factor of 100. Given the ever-accelerating rate of technical advancement and demand for performance, it's very likely that a 25-year architecture will have to be able to scale over a performance range of at least 1,000.

One prediction that can confidently be made about performance gains in the next century is that they will not be achieved through CPU clock speed alone. Amazingly, computer cycle times are already approaching

the speed of light. Given a chip of some dimension and the limits of physics, cycle times in the 1/4 to 1/2 nanosecond range are the best that are likely to be achieved – at least in our lifetime.

Three-Dimensional Performance

With clock speeds today already approaching five nanoseconds, the best performance gain that can be achieved through clock speed alone is in the "factor of ten" range.

This means that a 21st century architecture must be able to take advantage of performance improvements in *all three dimensions of performance:* CPU clock speed, multi-issue instruction (superscalar), and multiple processors, including massively parallel processing.

A Very Broad Family of Systems

Thirty years of 20th century computing has shown that today's mainframe is tomorrow's notebook. A computing architecture that does not scale well across a broader range of systems is soon limited in its usefulness. At a minimum, an architecture for the 21st century must be able, from the beginning, to be implemented on a single chip on the low end. On the high end, it must be able to support very large, even massively parallel, multiprocessing systems.

Unbiased Support for Multiple Operating Environments

Unlike all past computing architectures, an architecture for the 21st century will *not* be targeted for, nor show any bias towards, any particular operating system, language, or style of computing.

Very few organizations today rely on one operating environment. Different applications – production, client/server, PC, realtime, high-security – require different operating environments for optimal performance. And new operating systems and environments are likely to be invented and become important over the next 25 years.

Today, computing architectures are optimized for a particular operating environment via different interrupt modes, types of memory management, and physical memory addressing – all of which are defined in the computing architecture.

In contrast, an architecture that can be optimized for multiple computing environments can solve a wider variety of customer problems, which enables it to become more pervasive, and so attract more solutions development, and so solve a wider variety of customer problems, and so on.

Such a truly unbiased architecture has no "also runs" in terms of operating systems, languages, or styles of computing. An unbiased architecture is able to be optimized (in terms of interrupts, operating modes, physical memory mapping, etc.) to support multiple high-performing operating environments – regardless of whether the performance desired is: SPECmarks, transactions per second, floating point, realtime, integer, COBOL processing speeds – or a performance dimension not even defined today.

Open – To Implementation by Multiple Vendors

Perhaps the most dramatic change to come in computing architectures is the idea of an open computing architecture – one that can be implemented by many different vendors at all levels of integration.

To be open, an architecture must be designed in such a way that a combination of support for standards and licensing will make it profitable for *other vendors* to implement portions of the architecture – and feasible for customers to mix and match chips, systems, compilers, and software from multiple sources to meet their needs.

In the past, a single vendor assumed both the authority and responsibility for being the "sole source implementer" of all aspects of the architecture: chip design, fabrication, systems, compilers, operating environment – and, at one time, even applications.

A 21st century architecture, however, must be open to implementation by other vendors at all levels. For one thing, customers are demanding open solutions, available from multiple vendors. For another, practically speaking, the life of a computing architecture is increasingly dependent on its ability to achieve high volume in the marketplace. The ever-larger amounts of capital required for designing and fabricating new computer chips (approaching $1 billion in the next few years!) means that only those architectures that achieve high volume will generate the capital needed to produce the next generation of chips.

Alpha – The World's Next Computing Architecture

While every computing solution reflects quality of execution at all levels of implementation – chip design, fabrication, compilers, operating system, development tools, and applications – a superior, long-lasting computing architecture is the foundation that every subsequent layer of computing technology leverages.

In 1975, Digital engineers working on the new VAX computer architecture made a prediction about when their new architecture would begin to face the limits of its endurance as a leading-edge technology. In October 1992, they calculated, the world would begin to need a new computing architecture. Until then, theirs would be the best computing architecture in the world.

With Alpha, Digital is ready to deliver the world's 21st century computing architecture.

Architects of the Future

The designers of Digital's next generation computing architecture are senior consulting engineers Dick Sites and Rich Witek. Dick Sites, who has been at Digital for 11 years has a B.S. in mathematics from M.I.T., a Ph.D. in computer science from Stanford University and has worked at IBM, Hewlett-Packard, Burroughs, and the University of California, San Diego. Dick led the VAX 8200 microcode group and has filed 22 patent applications in hardware and software technologies. He studied computer architecture under Fred Brooks, an architect for IBM's System/360. In 1971, while at IBM, Dick worked on the precursor to the IBM 801 RISC computer. [He was promoted to Senior Consulting Engineer at Digital in March 1991.]

Rich Witek has been at Digital for 14 years. His previous work experience includes positions at Bell Labs and the Argonne National Laboratory. Rich has a B.A. in computer science from Aurora College and has done graduate work in computer science at both Northwestern University and Boston University. Rich was one of the three engineers who led the development of the MicroVAX chip. He is the author of several technical papers.

Most recently, his "A 50-MIPS (Peak) 32/64b Microprocessor" paper was presented at the IEEE Solid-State Circuits Conference in February, 1989. Four patents have been issued to Digital for Rich's work. [He was promoted to Senior Consulting Engineer at Digital in August 1987.]

The Evolution of Computing Architectures

	60s IBM 360 PDP-11 Family Architectures	70s VAX IBM 370	80s PC/Workstation Architectures	21st Century Architectures
Design Goal	Binary compatibility		Raw performance	Binary compatibility AND very fast, balanced performance
Design Horizon	15 - 20 years		5 - 10 years	25+ years
Address Space	16-, 24- and 32-bit			32-bit 64-bit
Performance Optimization	FP	FP and TPS	FP or TPS	All (FP, TP, realtime integer, COBOL)
Instruction Issue	Single-stream		Single-stream	Multi-stream
Processor	Single processor	Single-to-multiprocessor	Single-to-multiprocessor	Single-to-multiprocessor to massively parallel
System Scaling	Narrow (mainframe or mini only)	Broad (micro-to-mainframe)	Narrow (desktop, server)	Very broad (embedded chip to supercomputer)
Hardware Implementation	Board *		Multi-chip	Single-chip
Operating System	Single, proprietary		Single, UNIX	Many (production, PC, client/server, realtime, high-security, context-switching, massively parallel)
Languages	Many		Single or few	Many
Open Architecture	No		Some	Yes

* The VAX architecture was moved to a single VLSI chip in 1984

Both the goals and implementation of computing architectures have changed over time. The Alpha architecture combines the best features of compatible CISC family architectures and high-performance RISC systems.

"Alpha VMS"

Kathleen Morse,
Consulting Software Engineer

As information about Alpha is disseminated to customers, their first question is "What is Alpha?" That question is quickly followed by many others, such as: "What is Alpha VMS? How is it different from VAX VMS? How is it the same? What will it mean to my application?"

To answer these questions, you must first ask "What is VMS?" If you asked ten different people, you'd probably get ten different answers. Users would say VMS is: MAIL, NOTES, EDIT, COPY, PRINT ...all the things that are used in their daily activities. System managers would say that VMS is: DCL, SYSMAN, AUTHORIZE, SYSGEN parameters, clusters, ACLs, etc. Application programmers would identify VMS with: system services, run-time libraries, C, FORTRAN, DEBUG, LINK, LIBRARIAN, and all the various CASE tools that they use to accomplish their work. System programmers would say VMS is: user-written device drivers, MACRO32, XDELTA, kernel-mode code, ASTs, and so on. VMS is many things to many different people.

Port of VMS

Alpha VMS is a true "port" of the VMS V5.4-2 sources to the Alpha architecture, just as other operating systems in the computer industry are ported. Crossdevelopment tools were built that accepted VAX MACRO32, BLISS, and C sources, and output Alpha VMS object modules/images. VMS has NOT been rewritten or redesigned, nor rewritten in C.

To understand what occurred during the port of the VMS software, consider Diagram 1.

The lowest level of the operating system code was modified to work on Alpha systems, such as boot code, memory management code, and scheduling code. This "kernel" of an operating system has intimate knowledge of the hardware. The next layer of operating system software, such as system services and file services, has very little knowledge about hardware. (For example, logical name translation or mailbox devices are software constructs with no hardware-specific knowledge at all.)

Layered above the operating system are the callable run-time libraries (RTLs) and user interfaces, such as Motif, XUI, and DCL. These layers of software interface with lower layers of software, not with hardware. All the various VMS utilities speak to these software layers below them.

Thus, "porting VMS" to Alpha means that all the various layers of software that make up the VMS software environment have all been moved to the Alpha system.

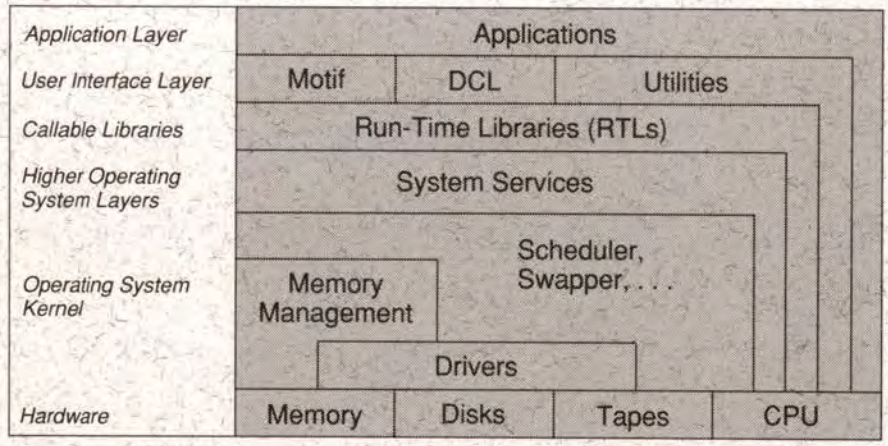


Diagram 1: What Software has Knowledge of Hardware?

Moving VMS Applications

So what does this mean to VMS applications? It means that all the various pieces of software that make up VMS will be there, still use the same interfaces, and look just the same as they did to VAX VMS programs. All the various runtime libraries, system services, file system, application interfaces, network interfaces, layered products, etc., will be there for a VMS application to use.

While it is possible for an application to have hardware-specific knowledge built into it (such as memory page size), it is much more likely to be protected from hardware specifics by the underlying layers of software. Moving a VMS application to Alpha VMS is easy – just recompile and run. Experience in moving real customer applications to Alpha has proven this to be true; even the migration of code as complex as the VMS operating system has gone smoothly and ahead of schedule.

So when we say "VMS is VMS," what we're really saying is that all the layers of software that comprise the VMS environment will be there on Alpha VMS systems just as they are on VAX VMS systems. System managers, users, programmers – all see the same VMS environment whether it be on a VAX system or on an Alpha system. So customer investments made in VAX VMS solutions are protected in the future by Alpha VMS: applications, data, training, support, site policies and procedures, etc.

64 Bit Hardware

64-Bit hardware functionality consists of two main features, 64-Bit integers and 64-Bit virtual addressing. VMS will initially support 64-Bit integers and phase in 64-Bit addressing in a later release. Alpha VMS will provide access to 64-bit integers through standard mechanisms for the various languages such as C, FORTRAN, etc. Another nice new feature is that 64-bit integers make possible an efficient internal representation of 18 digits of packed decimal data. The COBOL compiler for Alpha systems will transparently convert packed decimal data upon input/output to/from this new representation. Packed decimal calculations are then done very quickly with the new format, rather than by a very slow VAX instruction emulation package as was done for MicroVAX systems. This means that COBOL applications will have good performance on Alpha systems.

What about 64-bit virtual addressing? VMS has a number of interfaces, such as item lists, that have 32-bit virtual addresses embedded in them. Initially, VMS for Alpha systems will be implemented with 32-bit virtual addressing to preserve the application interfaces and ensure easy migration of applications to Alpha. Just as VMS systems have evolved in the past from isolated systems to networks to clusters, so the VMS environment will continue to evolve, making 64-bit virtual addressing available to future applications. Digital is committed to providing a 32-bit environment for applications that have no need for 64-bit virtual addressing, so that these 32-bit applications will NOT need changes in the future when VMS on Alpha provides 64-bit virtual addressing capabilities for those applications that do need a larger address space.

Summary

In summary, Alpha VMS has been designed so Alpha VMS users will quickly see the same rich-featured, robust environment as VAX VMS users see today:

- Same software development environment
- Same user interface
- Same file system
- Same system management
- Same networking and network management
- Same cluster systems
- Same ...

Thus, we can truly tell our customers: "VMS is VMS."

The October Momentum continues...

The announcement activities at the World Trade Center in Boston, October 30, 1991, collaboratively produced by public relations groups from Corporate, VSS, ISB, Storage, TSNG, and NAS, attracted dozens of editors from the top trade, business and industry press, and resulted in extensive press coverage and positive consultant comments.

Business press clips from *The Boston Globe, Wall Street Journal, New York Times* and *The Boston Herald* as well as analyst reports from Gartner, Forrester and Dataquest exceeded expectations.

A separate Analyst Event on October 29th drew thirty-nine consultants. Fifty-five consultants from Gartner, Forrester, Dataquest, New Science, Meta Group, Computer Economics, IDC, and InfoCorp were briefed the week before the October 30th announcement through a consultant roadtour. Key editors from *DEC Professional, Systems Integration,* and *VAR Business* were also briefed prior to the announcement.

Scores of customer events ran worldwide through the quarter highlighting the leadership price/performance VAX 4000-500 and VAX 6000-600 products announced on October 30th.

Below are a few clippings from various business articles:

The Boston Globe

"Digital Equipment Corporation, yesterday came roaring back with a new soup-to-nuts product line plus a revamped software strategy."

"Digital's announcement was hailed by Wall Street and industry analysts."

"This is the best hardware Digital has had in five years."

THE WALL STREET JOURNAL.

"The power and pricing of the new product rival computers built around a hot new technology known as reduced instruction set computing, or RISC."

"Even analysts who have been skeptical of Digital's prospects were impressed."

Digital NEWS

"Vice President Bill Demmer boasted that the midrange upgrades represented the single-largest performance boost in DEComputers since the VAX was introduced 14 years ago."

"The audited benchmark results for the just announced VAX 6000 Model 600 series and the VAX 4000 Model 500 series indicate DEC is now running neck and neck with low-cost UNIX boxes in price-performance. The VAXs offer up to three times the performance of their predecessors, said Demmer, vice president of VAX VMS Systems and Servers."

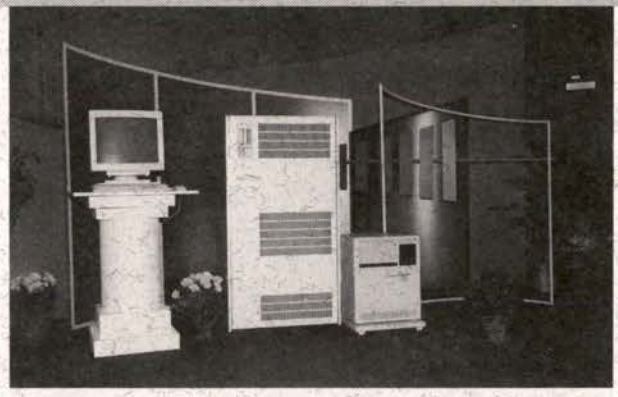
SYSTEMS INTEGRATION®

"Digital Equipment Corporation is totally revamping the way it licenses software in a move that could revolutionize midrange and large-system software sales in general."

"On the hardware side, DEC has beefed up the price/performance of its VAX 4000 and 6000 processors."

Continued on next page.

Photos from the October Announcement...




digital


PRESS

"The Voice of the Customer" for the Alpha Program

Don Alusic

The Alpha program is making major changes in the attitudes of some our significant customers and their account managers about the perception of Digital's direction and viability. One customer in the Alpha Customer Advisory Board started with a very skeptical outlook and has come around to saying, "I think I finally believe you and see that the Alpha program offers something very significant for the computer industry." An account manager stated that the "Alpha business and marketing direction is one of the most important perspectives that I have heard in years and one which will get Digital back on track and focused again."

These statements are a component of what the Alpha program has termed the *The Voice of the Customer.* Bob Supnik has declared that keeping the program well grounded with customers and customer feedback is a very key goal for the entire Alpha program. This has lead to continuing interaction with many customers of widely varying backgrounds and interests and across a wide variety of geographies.

With the Alpha program VSS has launched a series of Customer Advisory Boards to develop ongoing relationships with a consistent set of customers to interact about a specific program. These interactions have a technical flavor to them, but focus heavily on the business and marketing issues associated with the Alpha program rollout. There are specific groups for end users and CSOs in the US as well as groups in Europe and Japan.

The specific goals of the Customer Advisory Boards, according to Gareth Taube, the Customer Programs Manager include "the creation of Digital/customer partnerships to ensure mutual business success with the Alpha program. It will provide a vehicle for key customers to play an active role in the Alpha rollout."

For the US End User Customer Advisory Board participant customers were selected via a nomination process that produced over 50 nominees from the areas marketing and program office organizations. Approximately 15 customers were selected from a diversified set of industries. This includes AETNA, Allen-Bradley, Amoco, Bell Atlantic Tricon Leasing, Corning, Eastman Kodak, E. I. Du Pont, Fermi National Accelerator Lab, McGraw Hill, Merck, Midwest Stock Exchange, Pittsburgh Supercomputer, Rockwell Int'l and University Of Texas. Each customer was accompanied to the meetings by their account manager.

The first two meetings were held in the Boston area in May and October of 1991. The customers eagerly accepted the challenge of providing feedback to the Alpha program. The topics included such areas as Business/Marketing Strategies, Program Overview, Application Plans and Growth Paths. Their feedback ranged from without this capability we won't buy any Alpha's to we would like to know more about this area. Discussion topics included topics such as Clusters, UNIX, migration paths for current VAX customers and desktop strategies.

An account manager stated that the "Alpha business and marketing direction is one of the most important perspectives that I have heard in years and one which will get Digital back on track and focused again."

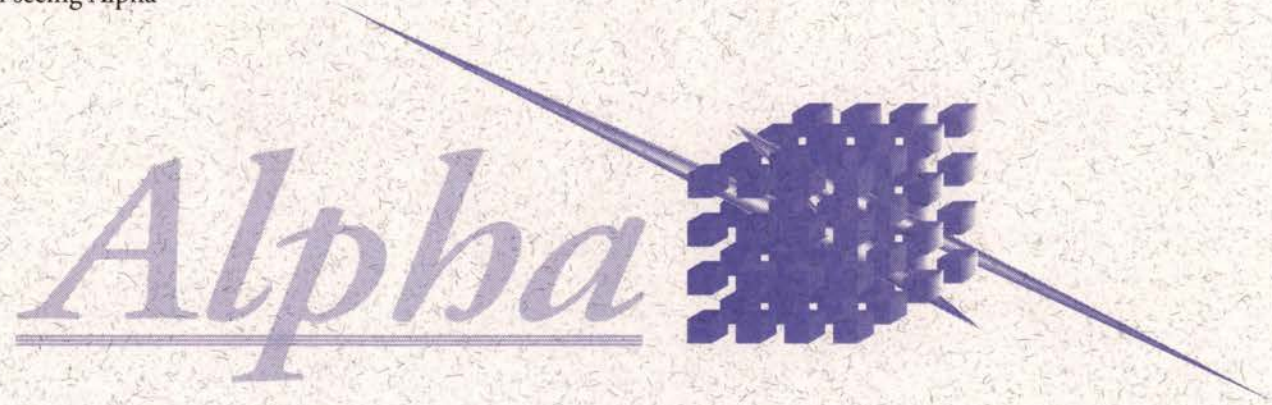
After the second meeting customers and account representatives were very pleased with the direction and progress of the program. Comments included, *with Alpha, Digital has the opportunity to lead the computer industry, and to compete beyond IBM.* One account manager thought this was the most significant move for Digital in many years. The customers also encouraged us to keep going as fast as possible and not to become complacent. They noted that they had heard promises before. They would like to see the potential of Alpha becoming a reality.

In Europe the Alpha cab has an enthusiastic mixture of direct and indirect customers. The customers view the Alpha program very favorably and encouraged Digital to get the message to the marketing place early. This will show a strong future for VMS and allow them and other customers to include Alpha in their long range planning. They also encouraged Digital to get its layered products and applications on Alpha as soon as possible. They also suggested that we develop incentives for third party databases and applications vendors to move their products to Alpha coincident with the first systems.

The Japanese cab has a mixture of the VAX VMS and IBM MVS customers which provides a different flavor. The interaction revealed a strong interest in seeing Alpha develop the basic technologies and development environment to allow these customers to off-load and downsize their mainframes. They were particularly interested in Alpha as a database engine as well as a strong desktop and desktop integration offering.

The Alpha program has seen some key benefits from the cabs. The marketing and technical strategies were refined to more closely match customer needs. In addition development priorities were reordered based on customer feedback. The customers have provided feedback on their major applications for VMS, UNIX and other operating environments which they must have supported on Alpha systems. This data will help Digital meet the customer needs and understand the Alpha shipment ramp up.

Future meetings will be held in all geographies throughout the Alpha rollout window. This is a key component of the *Voice of the Customer* activity for the Alpha program and one that will lead to better products and services for the customers as well as for Digital.



Systems Integration Magazine Readers Name Digital's VAXft System Product of the Year

Jan Stryker

Fault-tolerant VAXft System Honored

The readers of *Systems Integration* magazine have chosen Digital Equipment Corporation's VAXft computers, a series of high-performance, fault-tolerant processors, as Product of the Year in the magazine's second annual product awards competition. The award will be announced to the general public in the Systems Integration December 1991 issue.

Finishing ahead of Tandem Computer's Integrity S2 in the fault-tolerant computers category, the VAXft system was voted the top system by a poll of more than 110,000 *Systems Integration* readers worldwide.

Systems Integration readers were asked to select products which best served their needs in the past year. The award is considered particularly significant because it represents the buying choices of information system professionals from around the world who manage, implement, specify and purchase computer systems, products and services. These include value-added resellers, manufacturers of computer systems and peripherals, in-house system integrators and other volume buyers of computer technology.

"We are delighted that the skilled professionals who read *Systems Integration* recognize the VAXft system as the superior high-performance, fault-tolerant solution," said Ann Katan, Fault-Tolerant Program Manager. "We thank them and *Systems Integration* for this award."

All products in the competition were nominated by *Systems Integration* readers in a special ballot in February of 1991. An editorial/industry board reviewed the nominations and narrowed the list to a select group of finalists, covering 35 different categories. This list was published in a special check-off ballot in the magazine's July 1991 issue. Winners were announced at the Las Vegas Sands Hotel Casino on October 21, 1991 as part of the COMDEX trade show.

Digital's VAXft series is a family of fault-tolerant computer systems that protect user organizations against unscheduled down-time that can cost significant amounts of money and even threaten the welfare of information-dependent businesses. The VAXft series meets the performance, capacity and availability demands of a wide range of applications running under the VMS operating system. Using VAXft systems, VAX system users can configure production systems which rank among the most dependable systems now available.

The VAXft series is fully compatible with all other VAX and VAXcluster systems. Fault-tolerant capabilities can be introduced to enterprise-wide computer systems wherever they are needed, without rewriting existing applications.

VAXft series systems are implementations of a hardware-intensive fault-tolerant architecture. They provide continuous processing together with high levels of data and computational integrity. Today, the series offers four levels of performance, packaged in 11 configurations, to deliver fault-tolerant systems for a broad spectrum of applications.

Digitals VAXft system receives 1991 Systems Integration Product of the Year Award in the Fault Tolerant category. Pictured (left to right) are: Bill Lynch, Group Manager of Fault Tolerant Systems Marketing and Product Management; Fernando Colon Osorio, Corporate Consulting Engineer, Manager of High Availability and Fault Tolerant Business Unit; and Susan Chouinard, Publisher, Systems Integration Magazine.

Using Cp and Cpk to Improve Product Design...

A Practical Application of Six Sigma in Engineering

Joe Jasniewski
Design Assurance

Abstract

The Design Assurance segment of the Entry Systems Business group is currently engaged in implementing the Six Sigma philosophy in its product qualification test methodology; specifically, qualification of Power System components. This article presents a test method for measuring the quality of a power system design and an example of how this quantification was used to improve a design.

Introduction

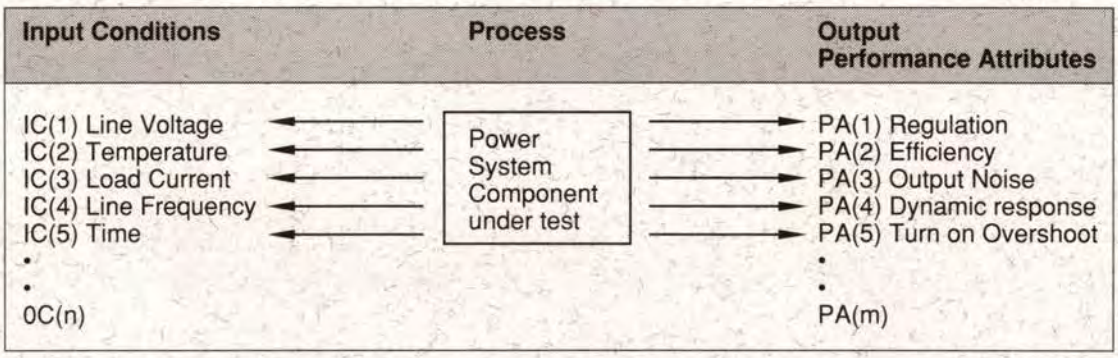
In Six Sigma terminology, the quality of a design is judged using two metrics: Cp, process capability, and Cpk, a measure of the shift of the mean. A Six Sigma design is achieved when Cp >= 2 and Cpk >= 1.5. Meeting these two conditions assures a very small probability of defective operation due to the design – about 3 chances per million.

In product design, an early assessment of the design's performance is desirable before full scale manufacturing is initiated. These assessments can be obtained before building prototypes by utilizing simulation techniques. However, empirical testing of prototype hardware is the most common way of ascertaining design quality.

The old paradigm for qualification testing was to conduct pass/fail tests at specification extremes. This method, however, rarely provided useful information on design margins, nor did it provide definitive clues on how to improve the design. Now, design quality is reported using Cp and Cpk. This will allow for dramatic improvements in the design process, due to the precise *behavioral* information contained in these measures.

Power System Test Philosophy

Given a well-specified power system component which provides measurable performance attributes (PA(1)...PA(m)) and does so under parametric input conditions (IC(1)...IC(n)), the theory behind our test methodology is outlined in the flow chart below.



If each Performance Attribute, PA(m), can be shown to have a Six Sigma performance, Cp>= 2 and Cpk >= 1.5, across all legal combinations of Input Conditions, then, given even m = 100 Attributes, manufacturing would still contend with an acceptable number of total defects. On the other hand, given only m = 10 Attributes, each at a Three Sigma design level, manufacturing would have to contend with a 50% yield (see Table 1). One of every two components in production would be rejected and reworked, or, worse, actually ship with some Output Performance Attribute out of specification at some Input Condition combination. The impact on manufacturing yields and costs, not to mention field service costs, is tremendous. This table demonstrates the importance of having Cp >= 2.0 and Cpk >= 1.5 on every specified Performance Attribute.

(Table 1 assumes a +/- 1.5 sigma average common cause shift of the mean in a typical process. In our case, this shift is in the performance of any one measured Attribute.)

The testing methodology consists of determining the performance level (Cp and Cpk) for each Attribute under all combinations of allowable parametric Input Conditions. Attributes that display Cp < 2 or Cpk < 1.5 would be investigated and designs modified to improve the performance.

Test Results

In order to evoke a measurable deviation in the Performance Attributes of a power system component, the parametric Input Conditions must be modulated between their specified limits and applied as test conditions. Some of these conditions are easily modulated (input voltage), while others present difficulty (temperature) or are impossible (time). In the test process for power system components now being used in Design Assurance, a random modulation scheme is employed wherever practical. The modulation and consequent application of these randomized Input Conditions is carried out quickly on a microVAX-based automated test system.

The test system also collects and stores the resultant data in tables. Typically, 1000 randomized combinations of parametric Input Conditions are run for each type of Performance Attribute to be measured. The measured values for each are recorded in columns (see Table 2) and contain the "yield behavior" across the entire n-dimensional span of applied Input Conditions. These columns can be loaded easily into a spreadsheet such as DECalc-Plus to determine the mean and standard deviation. By using these values and the specification limits, Cp and Cpk are determined for each Performance Attribute using standard formula.

Number of Tested Performance Attributes	Overall *Yield*			
	Each Attribute at Three Sigma	Each Attribute at Four Sigma	Each Attribute at Five Sigma	Each Attribute at Six Sigma
1	93.32%	99.379%	99.9767%	99.99966%
7	61.63	95.733	99.839	99.9976
10	50.08	93.96	99.768	99.9966
100	00.10	53.64	97.70	99.966

Table 1.

#	Input Conditions					Performance Attributes			
	VLine	5amps	3 amps	12amps	2amps	5V	3V	12V	2V
1	57.58	40.5	19.6	1.8	5.9	5.1546	3.3931	12.2452	2.0791
2	52.3	25.2	5	4.9	7.0	5.1549	3.3934	12.2441	2.0880
3	46.36	55.8	2.2	0.9	2.9	5.1523	3.3934	12.2427	2.0993
4	57.58	63.9	11.4	3.1	6.1	5.1533	3.3934	12.2454	2.0849
5	59.78	44.1	19.2	0.9	0.2	5.1548	3.3936	12.2463	2.0878
•									
•									
•									
995	59.78	28.8	4.4	3.7	7.5	5.1560	3.3940	12.2485	2.0887
996	52.3	19.8	11.8	3.3	2.3	5.1555	3.3934	12.2464	2.0893
997	38.22	2.7	20	1.5	8.4	5.1547	3.3918	12.2405	2.0753
998	58.24	52.2	19.8	2.7	7.5	5.1543	3.3931	12.2472	2.0753
000	39.32	58.5	14.4	0.3	7.4	5.1513	3.3919	12.2408	2.0827
1000	41.52	85.5	9.9	4.6	2.1	5.1507	3.3924	12.2422	2.0898
Spec Range	38-60V	0-90A	0-20A	0-5A	0-10A	4.950-5.200	3.250-3.450	11.40-12.60	2.058-2.142

Table 2.

As an example, the values in the "2V" column are tabulated and plotted as a frequency spectrum in Figure 1. For this distribution, the mean is calculated to be 2.0867 Volts and the sigma is 0.007 Volts. Superimposed in Figure 1 are the upper and lower engineering specification limits. It is clearly noticeable that the spectrum is not centered between the specification limits. Cp is calculated to be 2.0 and Cpk = 1.36. In order to improve the design, it is necessary to make a design change which would shift the measured mean toward the nominal specification value.

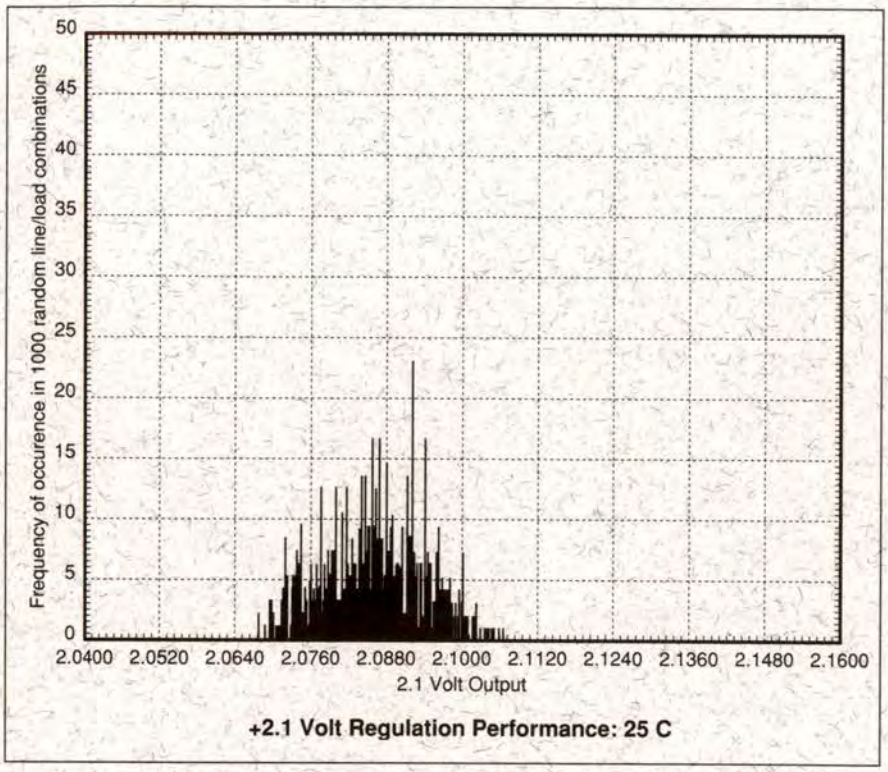


Figure 1.

Design Improvement

In the old paradigm, the above results would have been totally acceptable without further investigation since there were no measurement data values beyond the specification limits. However, when the circuit designer evaluated the above Cp and Cpk information, he was able to identify a corresponding design problem and make a simple geometric location change to a key reference component on the module. The change was incorporated in the second pass etch design and the device was retested.

Figure 2 shows the resultant spectrum obtained from the new test data. Now, the Cp = 7.0 and the Cpk = 6.7. With this level of the 2V regulation performance across the specified input conditions, manufacturing can be assured of a VERY low level of defects due to this parameter. For this case, a single change – the location of the reference component – affected both the nominal value as well as the stability of the voltage regulation. The design of this circuit has now been improved to fully meet Six Sigma criteria, with respect to the 2V line/load regulation performance, at nominal (25°C) operating temperature.

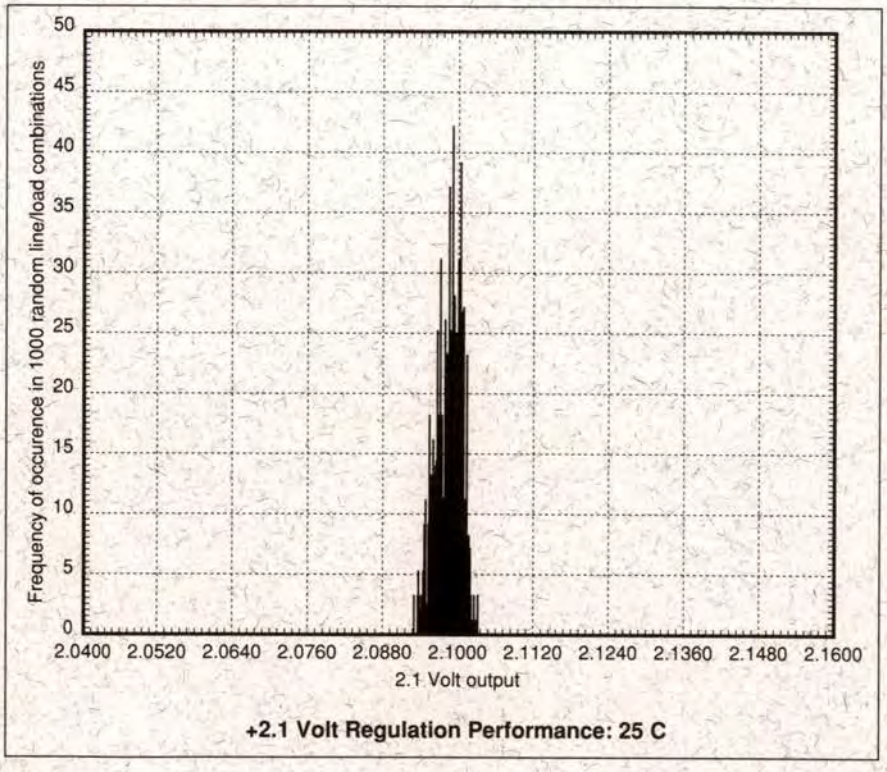


Figure 2.

Temperature Effects

Operating temperature is a difficult test condition to modulate randomly. The problem is due to the mass of material comprising a typical power system component. The corresponding long thermal time constant prohibits rapid temperature changes, so the random modulation scheme becomes impractical. The tests are simply repeated at the extremes of operating temperature. The data is then analyzed looking for variation due to temperature in the Cp and Cpk. As long as Cp remains >= 2.0 and Cpk does not become less than 1.5, it is assumed that the Output Performance Attribute meets Six Sigma criteria for design across the entire operating temperature range. Table 3 shows the Cp and Cpk for the 2V line/load regulation at the temperature extremes of 5°C and 50°C.

50 C	Cp	= 6.36
	Cpk	= 6.06
5 C	Cp	= 6.89
	Cpk	= 6.44

Table 3.

Assumptions

This method of test and analysis makes several significant assumptions. These are listed and discussed below.

1. The limited number of prototypes tested are fully representative of the design's capability and behavior.

Given that each of these is a custom-built prototype and has been checked out by the designer prior to testing, the assumption that the hardware represents the paper design is valid. Historically, products are released to manufacturing based on qualification test results taken from a few representative samples. This can result in significant insight into the design, eventhough little data is obtained on unit-to-unit variations.

2. The random selection of Input Condition values covers the extremes of the specification limits as well as realistic combinations of operational parameters within the specification limits.

The random number generator has been tailored to give a uniform distribution of random values. This distribution includes values which will apply the specification extremes of each input condition during testing. Also, it is correct to assume that actual operating conditions are random values which occur only at some point within the specification limits. This is because the exact values for any specific product configuration are unknown, prior to building the configuration and measuring it.

3. The distribution spectrum of each Performance Attribute is a normal distribution; the standard deviations calculated from the distributions exhibited by the test data are representative of the true Sigma measure.

While it is indeed possible to do a more accurate analysis of the spectrum distributions and to determine Sigma more precisely, it is fair to assume normality in order to quickly identify design performance aberrations. The intention is to implement corrective action early in the design cycle.

4. The average common cause shift in a typical process, be it a manufacturing process or a circuit set up to provide voltage, is +/- 1.5 Sigma.

Variation due to common causes is the sum of random variation in the many components of a process. Individually, the variation each component contributes is of little consequence, but all components together will effect a natural random scatter in the process performance. From past manufacturing experience, this is known to average +/- 1.5 Sigma for open-loop processes. While some of the processing a power system component does is certainly closed-loop, most of its Performance Attributes are directly dependent on incident component values.

Conclusion

It is possible to obtain more useful information from qualification test processes by restructuring test methodologies and by intelligently analyzing test data. Instead of using a traditional pass/fail test process, we can provide a more definitive measure of product performance. It was shown how the information contained in the Cp and Cpk measures allowed a design improvement to be implemented early in the design cycle.

Test and analysis in Power System component qualification now leads us to two simple metrics, Cp and Cpk, which are excellent measures of design quality. By designing for high values of Cp and Cpk, sufficient margins are assured to cover unit-to-unit performance variation due to common cause. The result is a product that is easy to manufacture and gives high quality at low expense. The ultimate beneficiary is the customer, who is able to purchase robust product performance at competitive cost.

The Newest Member of the VAX4000 Family, *Omega*

Jon Crowell, Engineering Manager
Tom Kopec, Design Engineer

Introduction

The Omega project was chartered to design and qualify a follow-on system to the VAX4000 Model 300. A key objective was to have the system qualified and ready to ship when the NVAX CPU chip became available in volume. Early on in the project, it was decided to structure the design to produce two discrete products for the effort of creating one. The first of these systems, the VAX4000 Model 500, was announced October 30th with Neptune (VAX6000 Model 600). The second system, VAX4000 Model 600, will be qualified in March and announced at a later date. The Omega project was managed by ESB Engineering in the Mill.

The Omega CPU modules were designed to upgrade existing VAX4000 Model 300 systems. The upgrade requires swapping the MS670 memory modules for the new MS690 memory modules. The VAX4000 Model 500 provides three times the performance of the Model 300 for about a 50% increase in price. The Omega system supports all of the IO adapters and expansion options of the previous Model 300 systems.

The Omega systems utilize two new, full custom CMOS-3 chips designed in Hudson. The NMC (NDAL Memory Controller) is a high performance 64 bit wide, interleaved, ECC memory controller. The NCA (NDAL to CPbus Adapter) provides a bus adapter to two CVAX pin buses (CPbus) which enables the Omega design to utilize all existing high performance VLSI I/O adapters designed for previous ESB products.

In addition to the new VLSI devices, a new series of high performance memory arrays was designed to support the Omega CPUs. The MS690 memory array, designed by memory engineering, supports a 72 bit wide data path, interleaving and fast test mode. The memory array stores 64 bits of data and eight bits of ECC, generated and checked by the NMC.

The memory arrays will be offered in 32, 64 and 128 MB variants. The systems support up to four memory arrays for a maximum system memory of 512MB. To accommodate the memory arrays, the BA440 enclosure backplane was re-designed to bus the 33 additional lines required to support the new memory module. This backplane was phased into the Model 300 last year to enable easier upgrades.

The BA440 pedestal enclosure supports the VAX4000 Models 300, 500 and 600. The enclosure was designed for utilization in an open

VAX 4000 Model 500

office environment. The fans used to provide cooling for the modules and storage are speed controller based on the ambient temperature to allow the system to operate quietly. The BA440 power system provides 644 watts of DC power from a standard 15A wall circuit.

The system was qualified to operate in a Class "B" environment, 10°C - 40°C (50°F-104°F). The BA440 backplane interconnect distributes the power and all signals between the buses, adapters and storage devices. There is a dedicated slot for the CPU with a 270 pin connector, four slots for MS690 memory modules and seven Q-bus slots. Four cavities for DSSI or SCSI storage elements are located at the top of the enclosure.

The Omega systems support DSSI and SCSI tape ISAs (Integrated Storage Assemblies). These are cableless bricks that allow a storage element to be easily plugged into one of the four storage slots. The new RF73 ISA is a 2GB disk option that is supported in the BA440. The new dual RF35 ISA supports two RF35 drives in a single cavity. The 3.5" RF35 is an 852MB, high performance DSSI disk drive. The single system pedestal will be able to support six RF35 disk drives with 4.8 GB of disk storage for high QIO applications. This RF35 configuration can support over 360 QIOs per second for random I/Os. If configured with RF73 ISA, six GBs of storage can be supported in addition to the TF85 2.6 GB tape drive for backup.

The base system provides two DSSI buses based on the SHAC VLSI host adapter. These two adapters have been measured servicing over 2700 QIOs per second when using RF73 disk drives. The base system has a high performance Ethernet adapter based on the SGEC VLSI adapter.

There are several ways to expand the base VAX4000 system, the most common is expanding to another DSSI based system to create a two or three node DSSI VAXcluster. The Q-bus in the VAX4000 can be expanded to supplement an additional 10 Q-bus slots to each system using the B213A enclosure. Using the DSSI expansion enclosures and the Q-bus DSSI adapter (KFQSA), the base system can be expanded to support a total of 28 DSSI disks which allows a total of 56 GB's of disk storage.

CPU Module

The KA680 CPU Module is the core of the VAX4000 Model 500 system. This single 8.5" x 10.5" module contains a processor 24 times the speed of a VAX11/780, an ECC memory controller, two mass storage (DSSI) interfaces, an Ethernet interface, and an expansion bus (Q22) interface. The module is upward-compatible with the KA670 (VAX-4000 Model 300) CPU module.

The NVAX CPU chip is an advanced implementation of the VAX architecture in SEG's industry-leading CMOS-IV technology. This device packs 1.3 million transistors on a die approximately six-tenths of an inch on a side. The CPU is partitioned into five semi-autonomous units:

1. The instruction prefetch and parse unit (IBOX)

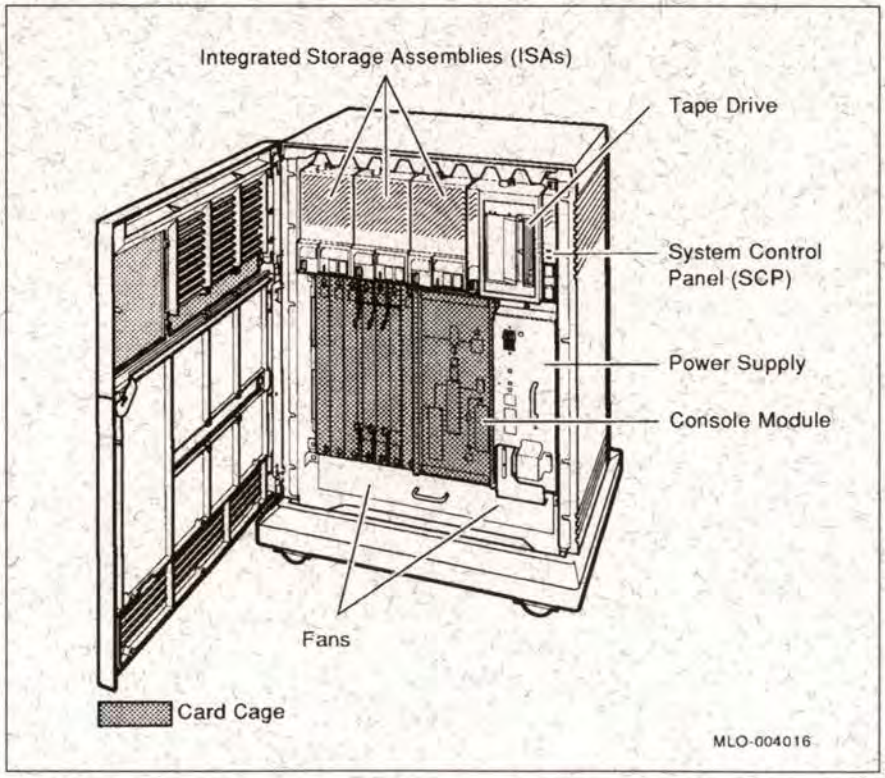
2. The execution unit (EBOX)

3. The memory-management unit (MBOX)

4. The floating-point unit (FBOX)

5. The cache-control and system-interface unit (CBOX).

Each of these units can run in parallel, performing its part of the work needed to execute the instruction stream. This "Macro-pipelining" allows the processor to do more work per clock cycle than a simpler, non-pipelined implementation, but requires significantly more active devices and control complexity.



BA440 Enclosure

The IBOX contains two significant features that improve the system's performance. First, a traditional prefetcher is used in conjunction with a Virtual Instruction Cache (VIC). This 2KByte cache operates with virtual addresses, allowing the instructions it contains to be accessed without waiting for a virtual-to-physical address translation. The second feature, which works closely with the VIC, is the Branch Prediction system. The Branch Prediction system uses a small history of recently executed branch instructions to predict the instruction flow that will follow a branch. When the branch is predicted correctly, the execution pipeline proceeds with no penalty; when the branch is predicted incorrectly, the pipeline is flushed and restarted.

The MBOX contains a 96-entry fully-associative Translation Buffer to support fast virtual-to-physical address translations. The MBOX also controls the on-chip 8KB cache. This on-chip instruction and data cache is 2-way associative, and is write-through. The CBOX keeps this cache a strict subset of the off-chip Backup Cache by passing invalidate requests into the MBOX.

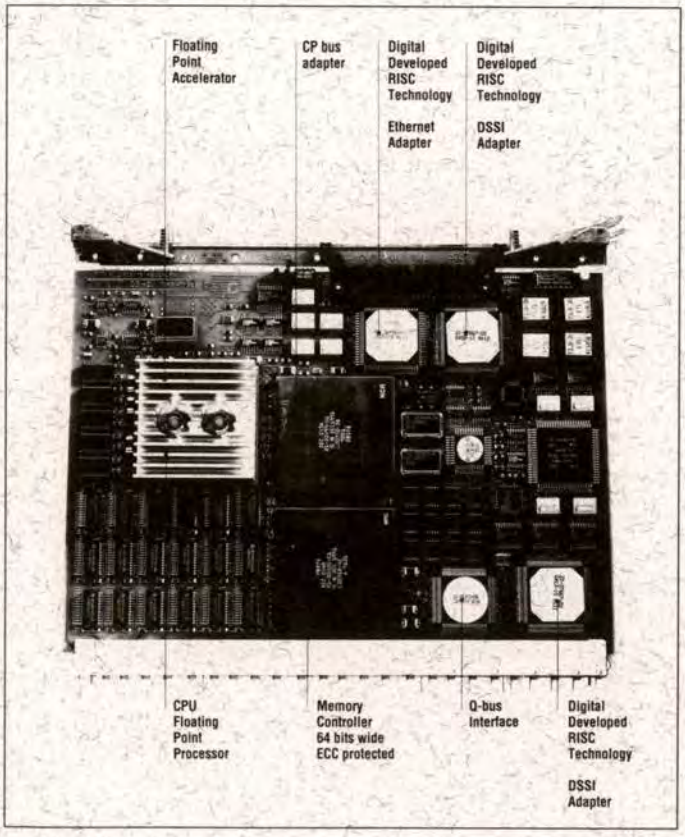
The CBOX is responsible for the control of the Backup Cache. This cache consists of a 128KByte ECC protected Data array, and an array of 4096 ECC protected tags. Both arrays are built from 25ns static RAMs. This cache is a direct-mapped "writeback" cache, which reduces bus and memory traffic by writing data to memory only when necessary. The CBOX also controls the processor-memory-IO bus (NDAL). The NDAL is a 64-bit parity-protected pended bus, which implements a protocol that supports the writeback cache. The NDAL runs at one-third the processor cycle time (42ns with the 14ns cycle used on the KA680).

The KA680 memory is controlled by a custom CMOS-III memory controller chip (NMC). This 148,000 transistor device provides support for up to 512MB of ECC protected memory, on up to four modules each containing 32, 64, or 128MB of memory. The memory backplane interconnect is 71 bits wide, to accommodate 64 data and 7 ECC bits. Each memory module supports two-way interleaving, allowing interleaving even with a single memory module. The maximum sustained read bandwidth of the memory subsystem is 54 Megabytes per second when used with the KA680 CPU module. The first 64-bit Quadword of data is typically returned within 420 nanoseconds after it is requested, and subsequent quadwords return every 84 nanoseconds.

The NMC is also responsible for the arbitration of the NDAL. The NDAL arbitration is folded in under the previous cycle, and uses hardware flow control signals to control service queue depths in the Memory and IO subsystems.

IO devices are supported by the NCA a 155,000 transistor CMOS-III chip designed to interface the NDAL bus to a pair of CVAX-pin (CP) buses. The NCA also provides support for the full DEC STD 032 Interval Timer.

A dual CP-bus strategy was chosen for several reasons. First, placing the Q22 bus adapter and the system ROM/console interface on a separate bus allows the system to optimize throughput on the mass storage and Ethernet devices without degrading the latency seen on the Q22 bus. The dual-bus structure reduces the loading on each bus to the point where no external buffering is needed for any device, saving significant module area. The dual bus structure also allows much simpler arbitration, with the Q22 interface highest priority on one bus and the Ethernet adapter highest priority on the other.



KA680 CPU Module

The NCA is optimized to work with the SHAC DSSI and SGEC Ethernet controllers. Read prefetch and write buffering is provided to allow these devices to run efficiently in "Double Octaword" mode, where the device may transfer two octaword (16-byte) bursts in a single bus grant. The NCA supports single-cycle acknowledgment, maximizing the throughput of each transfer. The maximum sustained read bandwidth seen by these devices is 24 megabytes per second.

The two DSSI (Digital Small Storage Interconnect) mass storage buses are controlled by a pair of SHAC (Single-Host Adapter Chip) interfaces. The SHAC is a single-chip implementation of the CI port architecture and DSSI Physical interface. It is based on a custom RISC processor that was specifically designed for peripheral processing applications, and that runs at more than 10 MIPS. These chips offload much of the packet processing burden from the CPU, and allow both chips to support the 4 megabyte/second data rate of the DSSI bus simultaneously.

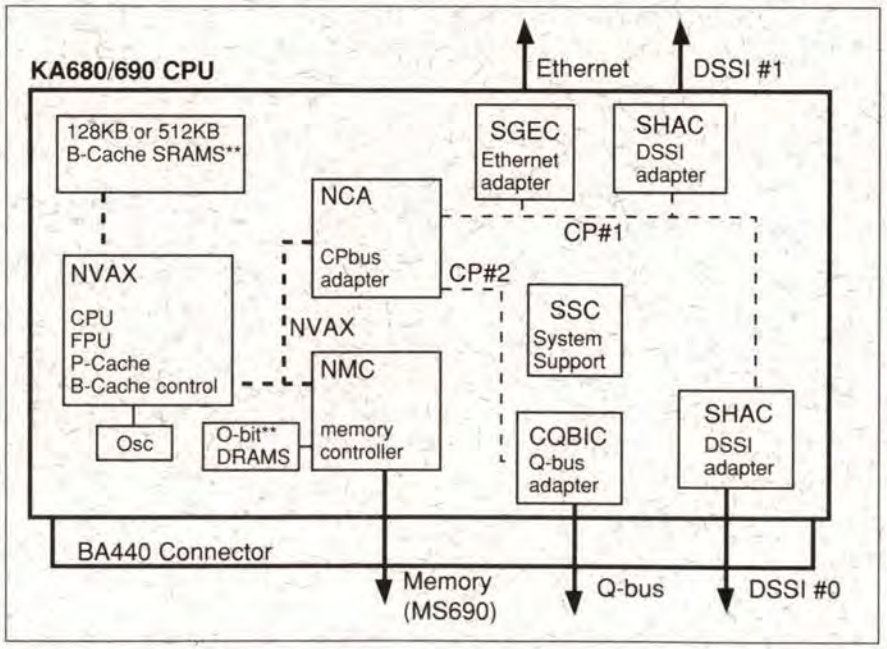
The Ethernet is controlled by a SGEC (Second Generation Ethernet Controller) interface. This chip is based on the same 10-MIPS RISC processor that is used in the SHAC chips. With its highly optimized microcode and logically separate 128-byte transmit and receive FIFOs, the SGEC in a VAX4000 Model 500 system is capable of supporting a fully-loaded Ethernet without loss of packets.

A Q22 backplane expansion bus is supported by the CQBIC Q22 interface chip. This device was originally designed for the MicroVAX 3500 series, and is used in all current MicroVAX and VAX4000 products that support a Q22 bus. The CQBIC provides scatter-gather mapping for Q22 memory space, and is responsible for system restart and power-up control. System Console support is provided by the SSC chip, also designed for the MicroVAX 3500. This chip provides the Console Serial Line interface, 1KB of nonvolatile RAM, programmable timers, and ROM decoding.

Console firmware is contained in 512KB of FLASH EPROM. This EPROM is capable of being erased and written under program control. The use of FLASH technology has provided the KA680 with several advantages and opportunities. Because the ROMs do not need to be removed for firmware upgrades, the ROM sockets became unnecessary. With the opportunity to upgrade the firmware by simply booting an image (either in manufacturing or the field) we avoided the rush to get final firmware into the volume programming site, and we have the opportunity to support new devices easily in the future; as the Omega series is planned to have a long product life, this capability is especially important. An unexpected, but very important, advantage of the FLASH EEPROMs was the speed with which we could turn around a new version of firmware during debug; we could have all the systems in the lab upgraded shortly after the creation of a new image, in less time than it would take to program a single set of ROMs!

Because the KA680 was designed as the first in a series of at least 2 CPUs, the module was designed with the ability to support either a 128KB or a 512KB backup cache. Because the RAMs for these two cache configurations are not available in compatible packages, a dual footprint was designed which would accept either device. Careful attention to the geometric properties of the cache layout resulted in this dual array occupying only slightly more area than a single-footprint design, and resulted in excellent signal integrity.

The Omega project team lead the development of Tangential Via technology for PWB layout. Tangential Vias allow the reduction or elimination of the standard 25-mil dispersion etch between surface-



Block Diagram of KA680 CPU

mount pads and the connecting via. The lower lead inductance allows much improved decoupling of the power planes, and the ability to place a via closer to the pad allows denser packing of SMT devices. The combination of excellent power supply decoupling and involvement of the RFI Compliance group throughout the project resulted in a module that is amazingly quiet in terms of radiated emissions, especially considering the 286MHz master clock.

The module, system, and PWB manufacturing groups have been directly involved in the Omega project from the very beginning. The strong partnership between these groups resulted in many significant achievements. The module is constructed on an 8-layer FR4 PWB, which costs $109 compared to $345 for the VAX4000 Model 300 CPU PWB. The module assembly group in Kanata, Canada is assembling the modules with fast cycle time and low defect rates, and the module burn-in had already been reduced to10 hours at FRS (in contrast to the typical 48 to 96 hours). Early and persistent attention to the compatibility of the module design with the PWB and assembly has resulted in a product which will save Digital more than $5 million in material costs alone over the life of the product.

The KA680 module design was extensively simulated to help ensure as few problems as possible when the first modules and chips arrived. DECSIM behavioral models for all the VLSI parts were integrated with structural and behavioral models for the rest of the module. The NVAX, NMC, and NCA design teams put in place a strong verification effort, and the system-level verification was kept closely coupled with the chip verification to provide maximum coverage with minimum overlap. Half of the system-level verification was in the area of directed tests which focused on specific area of concern such as Q22 latency and cache coherence. The remainder of the effort was the use of a functional exerciser which was designed to drive the system to high levels of CPU and DMA activity while allowing the insertion of errors. This effort lead to VLSI parts that were fully usable on their first pass, and a module that had a total of two wiring errors (both of which were found in simulation between module layout and first turn-on).

A serious effort was put into the Signal Integrity design of the KA680. All of the different subsections of the board were carefully analyzed using SPICE before any module layout was done. This analysis was targeted toward defining a set of geometric rules which would allow reasonably easy module layout while maintaining good waveforms and delays. After the preliminary layout was complete, hundreds of signals were re-analyzed to make sure that the rules did in fact result in the desired characteristics. This upfront work resulted in no signal problems on the module, and one simple problem in the memory interconnect which was resolved with a receiver change on the MS690 memory module.

The KA680 physical design was done in partnership with the DPE group. Because we had a goal to reduce the cost of the PWB as much as possible, we developed a strategy which would allow the release of both 8 and 10 layer artwork with all surface and routing layers being identical. The layout was initially done as a 10-layer layout, with full, separate power layers for 5 and 3.3 volts. The 3.3 volt layer and one ground layer were then removed from the design, and an isolated region of 3.3 volts was created on the remaining power layer. Because the fastest signals on the module (the cache signals) would have to cross this boundary, extra care was taken in the placement so that all signals that crossed the plane boundary would obey a set of rules developed to minimize crosstalk and reflection effects. Both 8 and 10 layer modules are populated in the first round of prototypes, so that the two designs could be directly compared; because the placement and routing of the module were identical, the layer construction was transparent to the module build process. The results of the comparison of the two designs showed that we were successful in creating a module with a split power plane and one fewer ground plane which had no significant signal degradation compared to the full-plane design. This was key to the significant cost reduction we achieved on this PWB design.

The NVAX CPU contains internal support for sophisticated performance monitoring measurements. The processor can directly report such metrics as clocks per instruction and detailed hit and miss rates throughout the cache structure. ESB and DCSS are working together to understand what this information can teach us about the interplay of software and hardware, and how we can use this knowledge to improve the performance of future systems.

System and Module Verification

The module was powered up on May 13th, 1991, and VMS login was reached after about 16 hours of hardware and software debug. About 1 week later the first module was running at 14ns with all of the caches enabled. In another 3 days a module was running VMS at a 10ns cycle. The VAX4000-500 was announced five months after power was first applied and volume customer shipments of the system began in just over 6 months after the power was switched on and four months ahead of our phase 1 schedule.

Once the first modules were built, we made extensive use of the internal DVT code which had been evolved since its development for the MicroVAX 3500. This code consists of a small realtime executive which provides support for a modular collection of device exercisers. Many of the exercisers used on the KA680 were taken with no modification from the KA670 DVT suite, and new exercisers were written to test the KA680's unique features. The ease of adding new exercisers combined with the debugging advantages of a simple monitor resulted in a system which allowed problems to be traced quickly to their root cause.

The base system supports over 40 storage and Q-bus options that can be configured in the system when ordered. The Omega systems were run through a detailed DEC STD 038 test to verify that all of the options will install, configure and function correctly in the systems. This includes testing the new system in various DSSI VAXcluster configurations.

The system was submitted to the various regulatory tests including FCC/VDE, PTT and Saftey soon after power-on. Many other DEC internal tests were started at this time including SQM (layered product testing), CVC (cluster verification), NQT (network qualification test), Diagnostic verification, Fault insertion and Field test. All testing was started with first pass hardware and some regression testing was done with second pass hardware (FRS Level).

Performance

The performance of the system in multistream and transaction oriented environments was measured with the TPC Benchmark™ A. This is a benchmark which simulates a banking system, but which generally indicates performance in environments which are characterized by concurrent CPU and IO activity and which have more than one program active at any given time. The benchmark produces two metrics, the TPC-A Transactions per Second (TPS), and the TPC-A dollars per Transaction per Second ($/TPS) for a fully configured system (including terminals and 5 years of maintenance). The VAX4000 Model 500 is rated at 62.4 TPSA-Local, a relatively high rating for a uniprocessor system. More importantly, the price/performance is rated at $11,945/tpsA-Local, the best price/performance in the industry.

System performance in technical single-stream environments is estimated by the SPEC™ suite of benchmarks. This suite consists of standalone benchmarks which are taken from various scientific and engineering problems. Advanced Compiler Technologies such as cache blocking and code scheduling were used to optimize the codes for the NVAX processor. The overall SPECmark™ for the VAX4000 Model 500 is 30.5, over 3 times that of the VAX4000 Model 300.

Other technical benchmarks were also run, and their results are presented in Table 1.

Benchmark	VAX4000 Model 500	VAX4000 Model 300
DR Labs (MicroVUPs)	50.9	10.0
Suite of 99 (VUPs)	23.8	9.3
LINPACK 100x100 Double (MFLOPS)	6.9	4.3
SLALOM (MFLOPS)	4.3	0.8
DHRYSTONES MIPS (OPT w/KAP)	55.5	19.2

Table 1. Benchmark results.

VAX4000 Computer Wins *Systems Integration* Magazine Product of the Year Award

Karen Quatromoni

Digital Equipment Corporation's highly successful VAX 4000 computer was selected as the Midrange Computer Product of the Year by *Systems Integration* Magazine readers.

VAX 4000 computers are powerful deskside computers that deliver reliable, investment-protected computing in the cost-sensitive midrange. They are ideal for organizations evolving their systems into flexible, distributed processing environments.

The *Systems Integration* Product of the Year Awards competition is a recognition, by readers of the magazine, of the products and companies that best served the needs of systems integrators during the last year. The 1991 competition marks the second annual presentation of these awards.

The VAX 4000 computer finished ahead of IBM's AS/400 C-Series, Hewlett-Packard's HP 3000 980/100 system, NCR's 3445 system, and Pyramid Technology's MIS Server T Series. "We are pleased with the market acceptance of the VAX 4000 family of computers," said Rene Martinez, Entry VAX Marketing Manager at Digital. "We are also pleased that *Systems Integration* Magazine readers, who are primarily resellers, VARS, and systems integrators, have found success in reselling our systems."

Nominations for the awards were requested via an open-ended ballot – listing product categories only – in the February 1991 issue of the magazine. Dozens of reader nominations in each of the categories were reviewed by a board of editorial and industry advisors who narrowed each category's nominees to a select few. The finalists were then listed on a special ballot published in the July 1991 issue. On this ballot, readers were asked to vote for their choice as winner in each category where they had direct experience integrating, specifying, or networking these products for computer systems.

Winners were announced at an awards ceremony held at the Sands Hotel Casino in Las Vegas, on October 21, during COMDEX. The results are also to be published in the December 1991 issue of *Systems Integration.*

Published monthly, *Systems Integration* is the leading technical magazine serving systems integrators. Its subscribers include more that 105,000 resellers/integration professionals working in VAR/third-party, OEM, or in-house integration environments.

Digital Equipment Corporation, headquartered in Maynard, Massachusetts, is the leading worldwide supplier of networked computer systems, software, and services. Digital pioneered and leads the industry in interactive, distributed, and multivendor computing. Digital and its partners deliver the power to use the best integrated solutions – from desktop to data center – in open information environments.

VAX4000 wins Systems Integration Magazine's Product of the Year Award.

Continuous Improvement in New Product Start Up

Mary Doddy
Manufacturing Engineering Manager

Abstract

Six Sigma methods are being used in ESB to drive continuous improvement. Design and Manufacturing partners have made the commitment to use the Six Sigma methodology on the Cobra program and all future products to achieve leadership in New Product Start=Up. Learning from the past products and improving the future products is the focus of our Six Sigma driven continuous improvement activities.

Introduction

The first Entry Systems Business (ESB) Alpha System is known by the code name Cobra. Cobra is the cornerstone of ESB's road map for continuous improvement. We have been applying Six Sigma methods to Cobra since the early concept efforts which began in the spring of 1990. Learning from Cobra, we are committed to continuously improve all future ESB products. Figure 1 shows our continuous learning model.

Cobra has just exited Phase 1 and has completed most of the Group 0 prototype non-revenue unit (NRU) build.

During phase 0, the emphasis of Cobra Six Sigma activities was on baselining the previous products (primarily VAX 4000/Pele) and on mapping and understanding the Cobra design processes. During phase 1 the focus shifted to simultaneously developing the Cobra product and the manufacturing process. This involved mapping the Cobra manufacturing processes, estimating Opportunities for Defects (OFD), and estimating design and process capabilities. Figure 2 shows our Cobra Six Sigma activities at a glance. We now have a strong design/manufacturing partnership and we have a closed loop learning process in place.

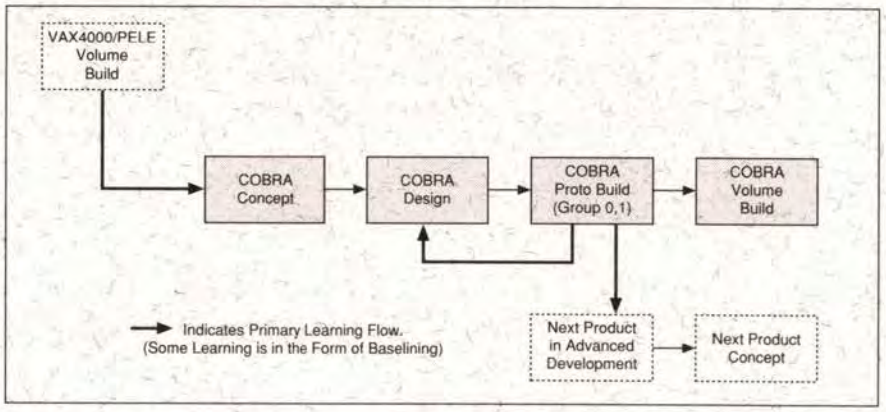


Figure 1. Continuous Learning Model.

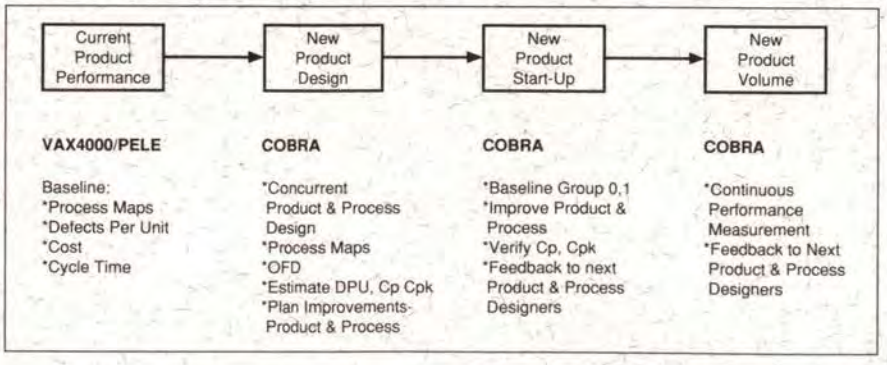


Figure 2. Cobra Six Sigma Activities.

Cobra Phase 0 Activities

Determining the starting point seems to be the most common difficulty once you have obtained initial training and understanding of Six Sigma. Cobra Design Engineers and Manufacturing Partners decided to start by baselining existing ESB products in Manufacturing. In essence, baselining constituted the first four steps of "the six steps of Six Sigma." This allowed us to attack steps 5 and 6 during Cobra development and startup.

A baseline is a thorough analysis of the manufacturing assembly process to measure where the process is today with respect to quality, cost, and cycle time. In the fall of 1990, baselines were conducted on stage I, stage II, and mechanical fabrication processes in Westfield, MA and Ayr, Scotland plants for VAX4000/Pele and microVAX3900/Mayfair products. The baselining teams consisted of Design and Manu-facturing Engineers involved in Cobra as well as PELE/Mayfair. This facilitated the maximum transfer of learning into Cobra. The process of baselining was similar to the one used in the Mass Storage Organization.

When we began these baselines, the level of understanding of the Six Sigma concepts was quite varied across the participants. Most of the Design Engineers had had Waterfall training plus one additional Six Sigma course, while many of the Manufacturing participants had had little or no Six Sigma training. This was not a major problem, however. In fact, baselining was used as an opportunity to learn by doing. This initial Six Sigma activity energized a core group of Cobra engineers and led to formal training plans for all groups (Design and Manufacturing) involved with Cobra.

The results and learnings from these baselines were published and made available to the whole Cobra team. They were also shared with others in the corporation to use as examples of how to begin implementing Six Sigma.

Six Sigma became an integral part of the Cobra Development and Manufacturing Start Up work. Six Sigma goals and plans were included in the Phase 0 Exit criteria. Most Engineering and Manufacturing plans are now written in terms of Six Sigma and continuous improvement. The Six Sigma plans and activities are reviewed quarterly at the Project 5x5 meetings and at various Project Status, Technical and Manufacturing Engineering meetings.

Process Mapping was the other major Phase 0 Six Sigma activity. During Phase 0 the module and enclosure design processes were mapped and reviewed for opportunities to reduce defects, cost and cycle time. Supporting functions such as Information/Documentation and Order Administration were also mapped in order to achieve improvement. Some assembly and test process maps were created along with the corresponding Opportunity for Defect (OFD) estimates. These initial maps along with the learnings from the baselines helped Manufacturing and Design understand where improvements could be made long before any hardware was built. As product designs evolve these assembly and test process maps will be updated and reviewed.

Cobra Phase 1 Activities

During Phase 1 detailed manufacturing process maps were drafted for every major subassembly of the Cobra System. This included both the NRU and volume processes. Many of the Manufacturing and Design Engineers were learning about process mapping and estimating OFDs as they applied it to Cobra in Phase 1. Estimates of Cp and Cpk were derived where data from baselines of other products and from vendors was applicable to Cobra. Additionally, Cp and Cpk estimates were derived during initial testing of Cobra subassemblies (for example, see Joe Jasniewski's article in this issue of *FOREFRONT*).

The process maps were also used to understand how and where data on cost, cycle time and quality should be collected during the NRU and volume builds. Various data collection methods are planned depending on the manufacturing site. Most Cobra sites have adopted a common software tool, QiSPC, for data collection, process monitoring and data analysis/reporting. For the first time, one common tool will be used across NRU and volume builds in ESB, providing a significant cross learning. While we are learning these new processes, data collection has started for Group 0 (NRU) build. Reports will be expected for

all Cobra builds while we continue to learn. These reports will be in the form of baseline reports from all Group 0 (NRU) build sites. Designers and Manufacturing Engineers will use these early build results to make product and process improvements for the Group 1 (pilot – built in the volume manufacturing plants) and volume builds.

During Phase 1, Manufacturing Engineers have been continuing the training of plant personnel on Cobra and Six Sigma. This is critical to the success of the Group 1 (pilot) builds in the volume manufacturing sites. Additionally, efforts targeted at understanding some of the key Vendors' process capabilities have begun.

Future Cobra Activities

Baseline reports will be issued as we complete the Group 0 (NRU) builds. These reports will be used in three ways: (1) to improve Group 1 (pilot) quality, cost, and cycle time; (2) to help mature Cobra Manufacturing processes; and (3) to support continuous improvement of next generation products, currently in Advanced Development. It is very important to use this information in the next generation product as soon as it is available. If we waited to share learnings until volume production, we would miss a generation of product before improvements could be made. Our aggressive Six Sigma plans require improvement in each successive generation of product.

Initial Cobra NRU data and baseline reports will be used to calculate Cp and Cpk. Cp and Cpk are metrics of capability that reflect the match between the product and the manufacturing process. As additional data is made available from subsequent builds these metrics will be recalculated and plans and goals for further improvement will be established. The process maps, OFDs, cost, and cycle times will also be monitored as build data is made available, as designs change and as processes are modified.

The initial experience on Cobra will aid in setting the commitments for long term reporting of Six Sigma status for Cobra through it's entire life cycle. It will also set the direction for the long term data collection, reporting and continuous improvement for future ESB products.

Recommendations for Future Products

The Cobra efforts have helped many people learn about Six Sigma and improvement. One of the key points learned is to maintain a closed loop of continuous communication between Design and Manufacturing during NRU and volume periods. In the past the original designers received very little feedback on their designs. Support Engineering usually worked on resolving the problems without the knowledge of the original designer. Closing the loop between the original designers and NRU/volume Manufacturing is the key to designing Six Sigma quality products.

Mapping or modeling as early as possible is another critical requirement. The Cobra team has indicated that manufacturing processes should have been mapped even sooner in the development cycle. For future programs it is recommended that process mapping, estimating OFDs as well as cost and cycle time be started in Advanced Development. Clear goals for quality, cost, cycle times, Cp, Cpk, etc. should be set at that stage.

Accelerated feedback is required so learnings get from one product into the immediate following product. Product-to-product improvement cannot skip a generation of product. Learnings must be shared throughout Design and Manufacturing. These learnings can be process maps, simulations efforts, various analyses as well as data from very early prototype builds.

The final recommendation is to continue to measure what you do for the express purpose of achieving improvement. Keep your mind open to learn and set goals directed toward Six Sigma quality. Do not be afraid to try new approaches. ESB has been learning while achieving good results. The focus is on doing whatever we can to continually improve towards aggressive goals.

The High Availability System PCU Joins VSS

Dick Willett

The High Availability Systems Group (HAS), which is focused on VAXcluster systems development, has joined the VSS organization. According to George Hoff, HAS PCU Manager, "Perhaps rejoin would be more appropriate, since VAXclusters were started in MSB with the shipment of the CI Adapter for the VAX 11/780 in 1982." The initial product was limited to a high speed DECnet link between processors. This was soon expanded to include shared access to high performance storage via the HSC-50 and a steady stream of VMS enhancements including a highly advanced distributed storage access solution (distributed lock manager). VAXcluster functionality has been a strong competitive advantage for the VAX system family and developments are underway to continue the evolution of leadership systems architecture for the Alpha systems.

HAS is a PCU with all of its revenue derived from VAXcluster related products such as CI Adapters and the recently announced Disaster Tolerant VAXcluster Solution (Multi Data Center Facility). Product development is currently focused on scaling cluster interconnect capacity to meet the increased demand of Alpha processors. Opportunities to expand Disaster Tolerant offerings are also underway which will evaluate lower cost configurations. Karen Mitchell, the HAS Finance Manager notes that under the New Management System, the P&L position of a business must be a major consideration in evaluating future plans. "The challenge for this PCU is to generate new product revenue more quickly as current products decline and reduce costs to improve PCU profit margins.

The initial VAXcluster offering was limited to a single interconnect (CI) with a CI Adapter which could deliver about 2MB per second. Ed Anton, HAS Hardware Development Manager, was involved in the latest CI Adapter development. "The goal of the CIXCD Program was to achieve a high throughput to support the VAX 6000 and VAX 9000 high performance cluster processors. The new adapter tripled throughput and support for multiple adapters/host VAXcluster performance well into the range of the largest mainframe systems. The CIMNA is an enhanced CIXCD under development to support Alpha systems with even higher performance through the incorporation of the N PORT host-adapter interface protocol. We are also developing a N Port Turbo Channel to CI Adapter for MIPS platforms under contract to the Open Systems Group. As we look to the future, we anticipate a shift to FDDI based clusters which offer high bandwidth (100 mbits per sec), greatly expanded interconnect range and open standard protocols".

The High Availability Systems Group (HAS). Back row, from left to right; Bill Lavigne, Jim Kuenzel, Ken Baker, Jim Griffith, and Pete Mullin. Front row, from left to right; George Hoff, Ed Anton, Karen Mitchell, Steve Polit, Karen Hellen, Don Reczek, and Verell Boaen.

The high performance and interconnect range capabilities of the FDDI plus VMS Host Based Volume Shadowing presented the critical elements for multi-site VAXclusters, according to Jim Kuenzel, HAS FDDI Program Manager. The ability to keep shadow copies of data at a site 20 km away provided a recovery capability for a site disaster, i.e., Disaster Tolerance. "The HAS group initiated a system project to provide a complete Disaster Tolerant VAXcluster solution in FY91. The capability delivered is operation of two sites separated by 20 km as a single VAXcluster, with data shadowing between sites and total cluster operational visibility from a system management station at either site. This product, VAXcluster Multi DataCenter Facility (MDF), was announced along with the new VAX 4000/6000 systems October 30 of this year." Initial reaction to this product has been very positive according to Gailyn Casaday, HAS Product Management Manager. "Customers needs for protection of critical databases and TP systems are expanding rapidly and Digital's MDF solution is the industry leader." There are currently four field test sites and customer installations will start worldwide this quarter. With the introduction of VAXcluster MDF, Digital can now offer the fullest range of systems availability solutions in the industry. Bill LaVigne, Marketing, sees the extension of Digital's capabilities into disaster tolerant computing as a key differentiator in the market. "We have redefined the market to include a new level of system availability with MDF. Our competitors can only partially address customer needs."

One of the generic attributes which have contributed to the broad success of VAXclusters is a strong commitment to systems quality. The Cluster Validation Group (CVG) plays a critical role in maintaining cluster quality by an extensive test program which is pursued via a 7x24 operation at their test facility in Salem, NH. The group is constantly upgrading their clusters with the latest CPU, storage and VMS revisions to test for full functionality under heavy load/large configuration conditions. This requires a lot of equipment: multiple VAX 8000/6000/4000 systems which include close to 100 processors plus several hundred disks. Mixed combinations of LAVC, DSSI cluster and CI clusters are tested, as well as FDDI and MDF. Pete Mullin, CVG Manager, is currently working closely with VMS in developing plans to test Alpha clusters." Being part of VSS is a plus as we pursue closer integration of our test process with the Alpha development program," according to Pete.

The configuration testing in CVG is complemented by performance modelling and characterization, carried out by the Systems Performance Group (SPG), managed by Steve Polit. The MDF product required a major modelling effort. As noted by Steve, "We needed to understand the system performance under many more configurations than could practically be tested. Detailed simulation models, combined with measured data, enabled us to do this." At present SPG is developing models that will predict throughput and latency for systems that will be configured with the FDDI Switch, currently under development.

"The goal of the CIXCD Program was to achieve a high throughput to support the VAX 6000 and VAX 9000 high performance cluster processors. The new adapter tripled throughput and support for multiple adapters/host VAXcluster performance well into the range of the largest mainframe systems. The CIMNA is an enhanced CIXCD under development to support Alpha systems with even higher performance through the incorporation of the N PORT host-adapter interface protocol. We are also developing an N Port Turbo Channel to CI Adapter for MIPS platforms under contract to the Open Systems Group. As we look to the future, we anticipate a shift to FDDI based clusters which offer high bandwidth (100 mbits per sec), greatly expanded interconnect range and open standard protocols."

The VAXcluster Technical Office lead by Verell Boaen is responsible for ongoing development of the VAXcluster architectural specifications, (SCA, CI, VAX CI Port, and N Port). The FDDI uses the same transport layer protocol used for LAVC running on the ethernet known as NI-SCA Xport. Storage plans to use this protocol in their FDDI Storage Arrays. VTO is currently developing detailed NI-SCA_Xport specification and is working with VMS to explore enhancements. Verell notes how critical HAS/VMS partnering is: "It is critical that thorough consideration be given to both architectural issues and their implications on implementation performance. A joint effort with an implementation group (like the VMS driver team) is the best approach to making a viable architecture. Being in the same organization makes it a bit easier."

Another organization which plays a critical role in maintaining VAXcluster system quality is the VAXcluster SASE ESU managed by Don Reczek. "The VAXcluster support requirements entail a strong focus on systems," notes Don. "Our group supports HAS products such as CIXCD and MDF, as well as cluster field problems requiring engineering support. We have a highly skilled systems team and can draw on additional expertise from other groups in HAS such as CVG which allow us to be responsive. VAXclusters have a valuable reputation for systems quality which we intend to protect and grow."

Ken Baker, Systems Engineering Manager, shares this view. "A major benefit of the VAXcluster architecture was to require a focus on systems performance early in the life of the VAX family. As hardware becomes more of a commodity, customers will shift investment to system integration solutions. The definition of systems will expand beyond a cluster to encompass multiple clusters in an environment with multiple system architectures and operating systems. The emergence of high performance public networks is beginning to drive the multi-site system interconnect model and the wide area network closer together. HAS is leading a joint project with NAC to develop a high performance FDDI switch and to integrate this technology into VAX Alpha Clusters in FY93. The Systems Engineering organization, along with all other HAS organizations, will be assigned to minimize time to market and maximize performance. The peak capacity of an FDDI switch is 50 times greater than a CI star coupler."

George is very optimistic about the future of VAXclusters and HAS. "The initial vision which formed the basis of VAXclusters has been validated over the past ten years by the broad acceptance of this systems architecture. The extension of the architecture to Ethernet LAVC, DSSI and FDDI, as well as a long list of processors and storage devices, reflects Digital's strength in bringing new technologies to market. The advances in functionality, such as Distributed Lock Manager, shadowing, and recovery facilities, reflect the ongoing strength of VMS software engineering. The performance and reliability growth reflect an ongoing commitment to systems engineering by HAS and others to ensure that the VAXcluster leadership position is protected. The next twelve months will offer the opportunity to take a larger step in cluster performance than that achieved in the previous nine years. Alpha processors and switched FDDI interconnect will provide worldclass technology which will be integrated into Digital's worldclass system architecture VAX/Alpha Clusters. There couldn't be a better time for HAS to join VSS to play our role in making it happen!"

ISV Group Joins VSS

Lynn Berman

Mike Mancuso, Group Manager of the Independent Software Vendor (ISV) Group, has recently joined VSS. The ISV Group will focus on driving new applications onto VMS platforms. ISVG now reports to the USS Group and the VSS Group.

Since its inception in 1988, the ISV Group has focused its activities on RISC UNIX applications recruit-ment, develop-ment and merchan-dising. These activities are handled directly by ISVG or in conjunction with other, appropriate Digital organizations: the Field for recruitment activities, Engineering groups for development support, IBUs and Channels Marketing for merchandising programs. More than 2,400 UNIX-based applications are now in Digital's worldwide portfolio.

"The continuous customer interest in existing and emerging VMS-based applications is the strongest line of defense against those who question Digital's commitment to its VMS business partners and users," says Mike. "VAX VMS has been and continues to be a major source of revenue for Digital and its development and distribution communities."

The connection between the VSS and ISVG organizations is designed to enhance VMS applications recruitment, support and merchandising activities.

Within the VAX world, the ISV Group's responsibilities are similar to those for the RISC world. First, ISVG will bolster its broadbase recruitment activities, identifying application developers interested in developing their solutions for the VAX platform.

Second, ISVG will strive for a fresh, objective look at the applications key to driving VAX VMS business in the high-end, mid-range and desktop markets. "We have to challenge our current applications thinking to ensure the right mix of solutions for these systems," says Mancuso. "If solution leaders or emerging leaders are not currently running on Digital's VAX VMS environment, we will recruit, support and design merchandising activities to increase market and license share.

In broad terms, ISVG brings applications to Digital's portfolio by identifying and addressing three stages of activity: developers must "Decide" that Digital's platforms are important to their busines; they must "Develop" their application solutions for use on Digital's platforms; they must "Distribute" their products to generate revenue for their businesses.

Technical support and business services for developers worldwide is key to Digital's success in managing these developer partner relationships. ISVG offers a range of support services and opportunities to

Independent Software Vendor Group (ISV), back row from left to right; Jim Repsher, Mike Mancaso, Steve tocman and Mike Wells. Front row from left to right; Bob Brownson, Judy Marrazzo, and Karen Johnson.

all Digital developers, regardless of program affiliation. Known as Common Services, these include ISVNet; development systems at reduced prices for purchase or lease; access to Development Technology Centers for hands-on experience and dedicated technical support; a listing in SOFTbase, Digital's online worldwide reference database; use of the Digital "Authorized Solution Provider" logo; user interface training; pre-release software opportunities; and others.

"The continuous customer interest in existing and emerging VMS-based applications is the strongest line of defense against those who question Digital's commitment to its VMS business partners and users," says Mike, "VAX VMS has been and continues to be a major source of revenue for Digital and its development and distribution communities."

Real-time communications, personalized technical support, public conferences, and ISVG specific marketing/merchandising programs are key features of ISVNet, Digital's online, worldwide electronic network for developers and distribution channels. Through ISVNet, users can reach The Electronic Connection for access to product, pricing, configuration and corporate information, as well as online shopping services. Targeted developers and distributors are invited to use Digital's networking strengths within their businesses, through the creation of private notes conferences for real-time communications with their VARs or other business partners.

Providing market specific, target focus campaigns designed to drive incremental license share worldwide is another key ISVG responsibility. Merchandising programs are in place for CASE/Manufacturing; Database and Commercial Tools; Engineering; Science and R&D; and Traders/Banking/Office market segments. Augmenting these activities are dedicated account managers, onsite with Digital's Top 30 CSOs, who work closely with ISVG marketing segment managers to develop CSO-specific revenue generation and awareness campaigns.

One of the most visible merchandising programs is the International Business Development Forum, which has generated more than 100 million dollars in incremental and workstation revenues to date. Designed to help developers and worldwide distribution channels meet to forge business alliances, the first Forum resulted in more than 100 new developer-distributor/VAR relationships; this year's Forum, which took place in September, hosted twice as many attendees and is expected to surpass previous goals.

The alliance with VSS promises to be rewarding for ISVG and Digital. For further information on ISVG's goals, please call 1-800-DEC-ISVN.

Videoconferencing Technology...
Advanced Communications Capability Benefits VSS Worldwide Operations

Bill Dumont

Face to Face Full Motion Video, A Reality in VSS!

Over the last 18 months the VSS PCU and related manufacturing locations have implemented Video Conferencing technology, forming one of the largest networks in the company today.

The systems provide capability for groups of people in 2 or more remote locations to meet in real time, full motion video (and audio).

The capability consists of a network of video conference rooms that are outfitted with video conferencing systems. These systems consist of dual TV monitors, a camera, audio equipment, graphics camera and codec devices that send and receive video images. Room control units manage the camera, monitors and other aspects of the system. A meeting administrator manages the equipment and protocol of the meetings and an automated scheduling system is used to book slots of time for conferences.

Video Conferencing, since its inception in VSS, has been used primarily by New Product Start-up Teams. Recently, however, many other uses are beginning to emerge.

The DVS Network

VSS and manufacturing counterparts make up the bulk of what is called the "Digital Video Service" Network (DVS). This network is a mixed terrestrial/satellite network currently spanning the US and Europe. Digital sites on the DVS network are stated in the chart below.

A conference can be scheduled between any of the above locations by contacting one of the site contacts listed above. Restricted access sites are locations that have limited usage to specific on-site businesses.

The DVS network also has access to a service offered by US Sprint called the "Meeting Channel." The Meeting Channel Network provides connectivity to public Video Conferencing rooms throughout the world as well as many private conference rooms owned by other companies.

Benefits

Video Conferencing in VSS has shown significant reductions in travel cost by key user businesses. However, users have reported that the most significant benefit is the enhanced communications that occur because of the technology. VSS business people are making more informed decisions faster because they can have face to face meetings with their colleagues that may never have occurred without the availabilty of video conferencing technology.

Continued on next page.

Site Code	Site Name	Contact	DTN
NIO	Salem, New Hampshire	Georgie Boucher	285-3336
BXB2	Boxboro, Mass	Cindy Cue	293-5330
SGO	San German, Puerto Rico	Iris Gonzalez	721-3126
GAO	Galway, Ireland	Claire Devaney	822-4021
MLO*	Maynard, Mass (5-1)	Bonnie Roe	223-3461
AYO	Ayr, Scotland	Heather Brown	823-3416
ZKO2*	Nashua, New Hampshire	Sylvia Holley	381-1002
EDO	Livingston, Scotland	Morag Currie	824-3347
REO	Reading, England	Jessica Philbrick	830-3811
GEO	Geneva, Switzerland	Michele Krebs	821-4097
LKG	Littleton, Mass	Debi Thompson	226-7480

* = Restricted Access Sites.

Coming Soon to DVS

The network on a corporate level is basically in its infancy and it is estimated that it will grow to 50 or 60 Video Systems by the end of FY92. Along with growth of the network, additional capabilities are planned as well. VSS is currently involved with beta testing a new Multi-point device that will soon be offered by PictureTel Corporation in Peabody, Mass. Multi-point will allow 3 or more site locations to participate in a single conference.

A networking gateway is also planned to be installed for December. The gateway will provide capability for sites on the DVS network to communicate to other sites (in and outside the company) who are using a Video Networking Service offered by AT&T called Switched 56. This will immediately expand the number of sites VSS will be able to connect to. Sites such as Acton (AKO1), Palo Alto (UCO), Albuquerque, Boxboro (BXC), Seattle, New Jersey, and 3 locations in Japan will be accessible with this new gateway.

Although utilized to a high degree today, there is still available capacity for additional VSS business groups to take advantage of this capability. For more information on Video Conferencing in VSS please contact Marty Wilcox, SALEM::Wilcox. User and Sprint Meeting Channel Guides are available through any of the site contacts listed.

VSS Information Service Center

Staff: Dave Carlson, *Manager*
Kevin Harrington
Karen Young

Desktop Software "Helpful Hints"

Here are some "helpful hints" from the VSS Information Service Center. If you have a question about how to do something with desktop software, contact us by sending MAIL to MSBCS::INFOHELP.

Some DECpresent Questions...

Q. "How do I eliminate that Sample Text on each slide in DECpresent?"

A. When you start creating a presentation in DECpresent, some sample text appears on each slide you create. Although this text is intended to show you how the slide title, subtitle and items will appear for that particular template, it can be annoying when you become familiar with that style or template.

To stop the sample text from displaying...

In DECpresent...

Pull-down CUSTOMIZE from the MENU bar...

=> Release on "Preferences..."

In the "Preferences" Dialog Box...

=> Click OFF the "Copy Items from Template" setting

Click on OK...

The text will no longer appear when you create a slide.

Q. How do I scale an image that I have created, e.g., using the print screen utility or a scanner?

A. Often these images are too large to fit on a slide. In those cases, you need to scale the image. The procedure you use to scale an image can also be used to scale pictures.

Most objects that are resized using MB3 result in distortion of the image. To scale without distorting the image, hold the SHIFT key while scaling/changing size with MB3. SHIFT/MB3 scales the image proportionately.

Once you have scaled the image/picture, you can use the "Keep Natural Size" button in the MODIFY LINK...dialog box to avoid accidental problems with scaling images.

To prevent accidental scaling of a graphic:

1. Click MB1 on the image to select it...

2. Press MB2 to display the pop-up menu...

3. Choose "Modify Link..." from the menu...

4. Click MB1 on the KEEP NATURAL SIZE button and click on OK.

If you need to scale the graphic later, choose Modify Link again and turn the button off.

Questions about MAIL...

Q. How can I spell check a MAIL message I want to send?

A. In order to spell check a mail message, you must invoke the TPU/EVE editor from mail...It's not difficult, just different.

Using DECwindows MAIL:

Create ("CREATE-SEND") your MAIL message...when you have finished typing the message, before you "SEND" it...

=> Pull down "ChangeEditor" from the Menu Bar,

=> Select "DECterm EVE" and release...

...an editing window containing your message will appear...click in the window to activate, then...

=> Press the "DO" key (on the function row, above the arrow keypad)...

...At the bottom left of the window, "COMMAND:" will appear...

=> Enter SPELL...

You will now be in the Spellchecker software...where you can replace/edit as necessary...this window is a terminal window so the mouse functions don't work...

=> when message appears as you want it, type CTRL Z.

You will be returned to your "MAIL:CREATE" window, where the message, "Using editor DECterm EVE" will be displayed, rather than the text of the message...

=> click on "SEND", and your 'spell-corrected' message will be sent.

Using VMS MAIL:

At the MAIL prompt, enter "MAIL> SET EDITOR TPU"

...now do the normal, "MAIL> SEND/EDIT"

to compose your message.

You will now be invoking the TPU/EVE editor.

When your message is ready to be spell-checked, hit the "DO" command...

The word "COMMAND" will appear in the lower left corner of the screen,

Enter "SPELL", and you will invoke the Spellchecker...when message is corrected, type "CTRL Z" and your message will be sent...

Note: You have now set your default editor to be TPU/EVE...if you want to set it back to EDT, then MAIL> SET EDITOR EDT is the appropriate command...

Some DECwrite Questions...

Q. How can I crop an image...I only want part of this picture in my document?

A. Although you can't actually edit the image in DECwrite, you can use "FRAMES" to accomplish this. By making a frame smaller than its contents, you can crop (hide) artwork that you do not want in view. You might crop a scanned photograph, for example, to eliminate an unwanted part of the picture.

Remember, to create a Frame, in V1.1 of DECwrite...

1. Position the cursor in the text where you want the anchor point for the frame to occur.

2. From the Menu Bar, choose Elements => Create Frame, then choose a style from the submenu... the pointer changes shape...

3. Place the pointer and drag MB1 to move the pointer diagonally across the screen until the frame is the correct size.

DECwrite places a fixed frame on the page based on the starting position of the pointer. DECwrite anchors a floating frame to text based on the current cursor location.

Once you have the frame created, position the image inside so that only what you want to see actually appears. Note that none of the frame's contents is deleted. To display the entire contents, either enlarge the frame, or select the frame and choose "DRAW => Snap to Contents".

Q. How do I prevent "hyphenation" in my document...I don't want any words to be hyphenated?

A. You can prevent hyphenation at the word level or at the paragraph level in DECwrite...

To prevent hyphenation at the WORD level:

Position the cursor in the word that you don't want hyphenated in this document,

=> Pull down "EDIT" from menu bar...

=> Select "Insert Character [->" and release on "Don't Hyphenate".

If you don't want any hyphens at all, you'll have to modify the paragraph style that you are using:

=> Pull down "STYLE" from the DECwrite Menu bar,

=> Select "Paragraph Style [->" and pull down and release on the style you are using, e.g., "Body Text..."

Paragraph Style Dialog Box will appear,

=> click on "OPTIONS..."

Paragraph Options Dialog Box will appear,

=> turn OFF the "Hyphenate" box

=> click on OK

=> Click on OK in Paragraph Dialog Box.

SSD Technology Meets the Needs of High-Performance Systems

Madeline Flynn
Marketing Manager

A dramatic increase in processor speeds forces an I/O solution that takes us beyond traditional magnetic storage capabilities. Digital's first endeavor to meet the I/O demands of our high-powered high-end systems was the development of the ESE20 solid state disk. Over the last three years, the solid state disk has proven to be a valuable asset to our customers whose businesses required very fast access to critical data.

Solid state disk (SSD) technology plays a key role in Digital's strategy to satisfy customers' high-performance storage needs in a variety of environments. SSD technology can provide very fast data access plus non-volatile storage and sharebility, a powerful combination for high-end and VAXcluster customers. By moving frequently used files to an SSD, customers can dramatically improve performance in I/O-intensive applications.

Digital's ESE20 Solid State Disk supports 1200 I/O requests per second, a speed that is 30 times faster than the request rate supported by traditional magnetic disk devices. Besides keeping pace with today's very fast processors, Digital's SSD complements other high-performance solutions such as DECram for VMS and the VMS Disk Striping Driver.

The Memory PCU began exploring solid state disk as a high-performance storage solution in anticipation of the MIPS explosion and a rapidly expanding VAXcluster installed base. We wanted to give customers very fast access to frequently used data, thereby improving application performance," states Charlie Cassidy, one of the initial drivers of the SSD development group. "Nearly 60% of the I/O accesses are directed to 1% to 3% of customer online data," continues Charlie, "and a relatively small, very fast storage device can boost performance significantly."

ESD built a proof-of-concept SSD model in 1986. Charlie Cassidy and Larry Biro, the design engineers, utilized the MS780-H memory as the basis of the prototype. They replaced the SBI interface with a custom RA81 controller interface and modified the firmware of the RA81 controller to act like a solid state disk rather than a magnetic disk. The prototype interfaced to the SDI through the modified RA81 controller.

Tests conducted by Systems Performance groups showed a 25% to 50% performance improvement when I/O-intensive applications were moved from magnetic disk to the prototype running on VAX 8650 and VAX 8700 systems. Based on these results, Digital decided to proceed with development of the ESE20.

"We designed the ESE20 to be a time-to-market product," says Charlie. "We had to satisfy a growing need as quickly as possible. Some VAX 8000 customers were already experiencing I/O bottlenecks. Increased processor speeds in future systems were bound to magnify the problem."

Other high-performance alternatives available to customers were sparse and implementation was often relatively painful. Customers could add memory and recode applications to make frequently accessed data memory-resident. This development-intensive option did not provide sharability and the storage medium was volatile. Another option, using third-party software that simulated a disk file in memory, had similar drawbacks. A third alternative, balancing disk accesses across spindles (striping) consumed considerable system manager time and provided nominal benefits.

To expedite development, the group designed the ESE20 around an existing memory product. Jim Stegeman and Rich DiMascio, the designers, chose a new memory that had the right characteristics, including capacity, size, packaging, and power, to satisfy the functional requirements of the ESE20. They integrated a custom-designed two-board set, including a memory controller and an SDI interface, with the memory boards. A data retention system built from an RD54 hard disk, a Qbus disk interface, and an uninterruptible power supply (UPS) completed the design. The resulting 120 MB ESE20 SSD supported 300 I/O requests per second and offered non-volatility of data and sharebility across nodes.

Ease-of-use was a key ESE20 design criteria satisfied by the product's SDI interface. The ESE20 looked like any other SDI disk device to the controller and to user applications, simplifying both installation and implementation. Customers didn't have to recode applications or change their operations to implement an ESE20.

Shortly after introduction of the ESE20, work began on an enhanced version that quadrupled performance to 1200 I/Os per second. Digital improved the ESE20's performance through modifications to controller protocols that used a cylinder/track/sector addressing scheme to access ESE20 data. By implementing Logical Block Number (LBN) addressing, this "enhanced" version eliminated rotational delay and other overhead.

"Marketing of the ESE20 within the company and to customers was a challenge because the concept was new," says Bob Christ, the Marketing Manager for Solid State Disks. "Customers traditionally evaluated disk storage in terms of capacity and $/MB. They naturally applied the same metrics to the ESE20 because of its disk characteristics. In reality, the ESE20 is a performance-enhancer rather than a traditional storage device. The value of an ESE20 lies in its ability to do work, measured in dollars per I/O requests per second, and the performance boost it provides to customers."

"As a systems vendor with an integrated SSD product, Digital offers superior systems solutions for customers with time-sensitive and disk I/O-intensive application environments," continues Bob. "ESE20 capabilities have given our customers the opportunity to do things that otherwise would be impossible or impractical. For example, a pharmaceutical company was able to maintain a large homogeneous five-node VAXcluster by moving the most active system files from magnetic disk to an ESE20. The ESE20 relieved the bottleneck at the company's system disk, thereby eliminating the need to break up the VAXcluster into multiple clusters or maintain multiple copies of the system disk. Another customer, a large freight carrier, was able to bring its largest transportation hub online using the ESE20. Without the ESE20, excessive wait times for answers to routing inquiries made it impossible to add a large hub to the system."

In the near future, Digital will introduce a new SSD product that provides a growth path for the ESE20 installed base. This product offers customers larger capacity in a smaller package that integrates with existing storage cabinets. Customers will be able to store more data on this high-performance device while conserving floor space, a costly resource. In addition, ESD will take advantage of the lower cost of emerging technologies, such as newer DRAMs and more cost-effective and higher-reliability data retention systems, to improve price performance.

ESD's longer term strategy focuses on technologies that make SSD capabilities available on a wider range of systems with differing interconnects. "As processing power is being driven down the system ladder, smaller systems are running more complex production applications that can benefit from SSD capabilities," says Bob. "In addition, our current ESE20 customers are looking for bigger and better SSD solutions."

"Our strategy is to build flexibility into our next generation of SSD products," says Geoff Hogan, the ESE20 Product Manager. "We want our SSD products to be viable for future systems and interconnects. Our platform approach, which incorporates industry-standard packaging, will allow us to accommodate new technologies with minimal modifications. To provide the best price-performance products, we are considering all of our options. We plan to offer customers a choice of SSD solutions."

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A Strategic Investment in Our Future

Joe Senz
HRD Mgr.

Fundamental changes are affecting the entire computer industry. These include changing technologies, increasing need to sell more performance and value for fewer dollars, and the need to solve more complex customer problems. To remain competitive, "idea and information technology" companies must be flexible and able to understand and meet changing customer needs and opportunities in a more product-integrated manner.

Everyone in the company is experiencing some impact of change. We are shifting to new paradigms for our work and management processes which require us to think, relate, and manage in new ways. The need to maintain a flexible, productive work force is not going to go away, even with an upturn in business. The reassessment of work and skill mix requirements must be an ongoing process if we are to continue to adapt to changes in the business environment, maintain competitiveness, and succeed in the marketplace.

Human Resource forecasts tell us:

- The *1982* graduation rate for engineers will not be equaled until the year 2012,
- Demand will out-pace supply by 1995,
- 85% of the work force for the year 2000 are current employees.

This coupled with the fact that 75% of Digital engineers have been out of school for 6 or more years and we draw the conclusion that Training, Education and Development is a strategic investment in addressing our human resource needs and one of our major strategies to ensure success in the '90s.

We must strengthen core job competencies cross-functionally; provide employees with new skills to meet current and changing business requirements; and provide managers with skills and tools to ensure development in a continuous learning environment.

Employees of VSS organizations are moving to meet this challenge. Interest in upgrading their technical and professional skills is on an increase. In the first quarter since the opening of the new Boxboro Training and Development Center over 180 employees have attended classes. This represents a 43% increase from the previous quarter. Some managers have made the commitment to "Team Training." This approach not only teaches a needed set of skills or processes but gives the group a new "common language" which improves communication and helps to promote "team work."

It is important that we continue our investment in the future in the following ways:

- Continue all technical training required to support product development.
- Continue to develop all of our employees to ensure our requirements for future talent are met.
- Train our employees and managers in the new reality of world market, total solutions, technical partnerships, and customer service.

Human Resource forecasts tell us:

- ***The 1982 graduation rate for engineers will not be equaled until the year 2012,***
- ***Demand will out-pace supply by 1995,***
- ***85% of the work-force for the year 2000 are current employees.***

- Continue to re-skill or upgrade knowledge of our employees in areas where technology or competitive pressures may obsolete current skill sets.
- Develop our managers to understand and use abilities in coaching, mentoring, and motivating employees (the "art" of management).
- Support the "T.Q.M." initiative by making sure you and everyone in your organization attends the appropriate training and that everyone thoroughly understands the 5 or 6 metrics that will make their businesses successful.
- Develop a mind set that Education is part of the work and the responsibility of all. Each individual contributor and manager should spend at least four weeks per year in some form of development work.
- Be wise with the expenditure of training dollars. Use our own talented employees to train others where appropriate. Send one person to external workshops/conferences when required, with the clear understanding that they will share the new information with others. Be creative and cost effective in meeting development needs.
- Utilize our Human Resource Development organization wherever possible to meet your training and development needs and to help identify resources and alternatives.

To review any of the course descriptions listed below:

1. Set Host MSBCS

2. Username = COURSES (no password is required).

To register, contact Kristin Cote, 293-5230, MSBCS::COTE or Bette Parker, 293-5213, MSBCS::BETTE.

March 1992 – April 1992
Training and Development Course Schedule

Microsoft Project
PRCJT01, BXB1 Training & Dev. Center ..... March 4

UNIX and ULTRIX System Overview
UUCSO04, Boxboro Training & Dev. Center ..... March 5 – 6

Writing in a Technical Environment
WTCHE01, BXB1 Training & Dev. Center ..... March 10 - 23

Intro to EXCEL
EXCEL01, BXB1 Training & Dev. Center ..... March 10

Advanced EXCEL
EXCAD01, BXB1 Training & Dev. Center ..... March 11

Alpha Technical Overview Seminar
ALCPH02, BXB1 Training & Dev. Center ..... March 16 – 17

OSF/1 Technical Overview
OSCIN01, BXB1 Training & Dev. Center ..... March 18

Winning With Customers
WWC0001, BXB1 Training & Dev. Center ..... March 19 – 20

OSF/1 Virtual Memory
OSCVM01, Boxboro Training & Dev. Center ..... March 26

C Programming
CPCRG03, BXB1 Training & Dev. Center ..... March 30 – April 3

VMS Internals II
VMCS202, Boxboro Training & Dev. Center ..... April 6 – 10

Time-Based Competitive Reengineering
TBCR002, BXB1 Training & Dev. Center ..... April 14

POSIX Compliant Programming for VMS Programmers
POCIX01, BXB1 Training & Dev. Center ..... April 22 – 24

ULTRIX for VMS Users
UVCU003, Boxboro Training & Dev. Center ..... May 4 - 5

ULTRIX Utilities and Commands
UUC0003, Boxboro Training & Dev. Center ..... May 11 – 15

*** Dates are subject to change*

Awards

Bill Demmer congratulates the recipients of Digital's Q4 Patent Awards

Barry Maskas

Satish Rege

Norbert Riegelhaupt

Jesse Lipcon

Unable to attend the photo session with Bill were: Hansel Collins, James Leahy, Donald Smelser, Noreen Hession, Barbara Altman, Simon Steely, Robert Dickson, Robert Supnik, Rick Gillett, and Darrel Donaldson.

Judy Parsons receives Q4'91 Quality Award

Judy has been recognized as self-motivated and a perfectionist. She has shown a great commitment to ensure that DECdtm users have a good usable interface clear, precise documentation.

Here, in the VMS Engineering (UK) group, we believe the key to our success is our people. We are a team of committed people and we expect excellent quality work from each other. In return, we try to recognize the efforts of our team members. Quality awards are one of the methods used by the group to show their appreciation.

We expect to carry on bettering the quality of our work at all times by improving our software engineering techniques and by continuing to get the best people. People like Rudi Martin, recent graduate from Glasgow University. Rudie has been awarded third prize in the "Young Software Engineer of the Year" award for 1991. This is an award given by the Scottish Software Federation. This federation, by representing and enhancing the interests of the software industry, promotes Scotland as a center of excellence in the design, development and marketing of quality software.

Shirin Sherkat-Khameneh

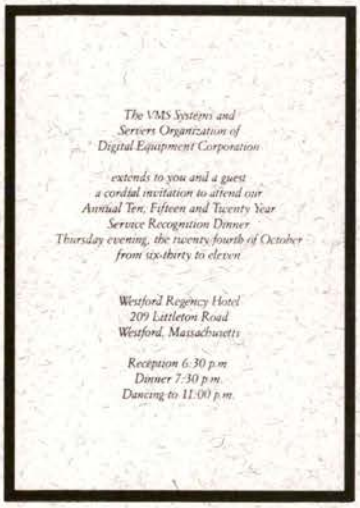
1991 Service Recognition Awards

Five-Year ...

VSS held its annual Five Year Service Award Luncheon on November 13, 1991, at the Westford Regency. Nancy Nagler, DCSS Personnel Manager, and Jesse Lipcon, ESB Manager, were MC and guest speaker. More than 60 employees were in attendance to celebrate their five years of service.

Five-year recipients...

Michael Badzinski
Karin Baker
Karen Barnard
Douglas Barta
Andrew Bartczak
Susan Bartow
Joseph Bates
Elizabeth Bohanan
Mark Bourgeois
Diane Boutotte
Carol Boutwell
Douglas Burns
Mark Cacciapouti
Michael Connell
Gerald Cotter
Jonathan Cromwell
Sean Cudmore
Zarka Cvetanovic
Niamh Darcy
Paula Deangelis
Frances Delano
Deborah Desrosiers
Roland Doucette
Donald Duffy
Dora Elguezabal
Meaghan Engdahl
James Esselstyn
Patricia Flannagan
Nitin Godiwala
Matthew Goldman
Nancy Gonelli
Franklin Greco
Richard Grenier
John Hersey
Andrew Ingraham
Ramesh Joginpalli
Margarita Johnson
David Juitt
Mark Kelleher
Leslie Kendall
Thomas Kopec
Beth Lawrence
Paul Leveille
Loralyn Lewis
Morgan Liu
Carolyn Macmunn
James Marcheterre
David Maruska
George Maruszak
Michael McKeon
Jonathan Mooty
Ruth Morgenstein
Susan Morse
Nancy Newsted
Joseph Notarangelo
John O'brien
Frances Oloughlin
Roland Quellette
Bimal Patel
Raoji Patel
Jill Patton
Nancy Pavlin
Donald Pettini
Rhoda Philips
Donald Pettini
Traci Post
Cheryl Preston
Kevin Quan
Sean Reilly
Douglas Richard
Michael Rickabaugh
William Rogers
Mitchell Rosich
Paul Rotker
Michael Serating
Richard Simon
James Sloan
Sylvia Strarratt
Maurice Steinman
Farhad Touserkani
Steven Varieur
Judy Weiss
Dawna Whelan
Jeffrey Wong
MaryEllen Zurko



The VMS Systems and Servers Organization of Digital Equipment Corporation

extends to you and a guest a cordial invitation to attend our Annual Ten, Fifteen and Twenty Year Service Recognition Dinner Thursday evening, the twenty-fourth of October from six-thirty to eleven

Westford Regency Hotel
209 Littleton Road
Westford, Massachusetts

Reception 6:30 p.m.
Dinner 7:30 p.m.
Dancing to 11:00 p.m.

Bill Demmer Congratulates the Recipients of 1991 Service Awards

"In Digital the individual is still the vehicle that makes things happen. Each and every one of you has a stake in the future of Digital and each and every one of you has the power and hopefully the will to make an effective contribution. All of you have the opportunity to directly impact the growth of this company."

Following Bill's speech, Bill personally congratulated each of the attendees.

Ten-year recipients...

Fifteen-year recipients...

Twenty-year recipients...

10th

Joseph Astone
Phillip Auberg
Joseph Backus
Richard Bagley
Charles Barker
Arthur Beaverson
Stephen Bellanca
Collin Blake
George Bleisch
John Boucher
James Brierley
Joseph Broderick
Jon Brown
David Cantor
Susan Careau
Barbara Chandler
Robert Chen
David Chesley
Brian Chew
Robert Christ
Noella Clark
Joan Clementi
Michael Collins
Norman Commo
John Costello
Steve Corcoran
Stephen Cote
Brent Covert
Ronald Desharnais
Charles Devane
Richard Devlin
Dan Doherty
Joseph Donaher
Geoffrey Donoghue
Katherline Dunn
Charles Dunn
Mary Ebens
Michael Ferris
Douglas Field
B Flanagan
Glenn Garvey
Olga Ginzburg
Karen Goldstein
Mark Gorham
Ann Grecoe
Keith Griffin
Richard Grote
Robert Haller
Charles Hammond
Mark Haq
Don Harbert
George Harris
Robin Harris
Masood Heydari
Stephen Howard
John Hurley
Joe Jasniewski
Gregory Jordan
Kathleen Kelly
Carl Kunze
Virgina Lamere
Patricia Lee
Gary Lidington
Andrea Macmillan
George Marashian
Richard Marcello
Kevin Martin
David Mayo
Dennis Mazur
Renee McCarthy
Michael McDonough
Joseph McFadden
John McMullen
Patrice McNally
Ann McQuaid
Peter Mellow
Richard Meyer
Kevin Milano
Robert Mondor
Martha Moore
Michael Murphy
Nancy Nagler
Varish Panigrahi
William Parke
Bette Parker
Susan Peppercorn
L Pilant
Michael Robie
Kimberly Roger
Ping Sager
David Sanborn
Robert Sanzone
Roberta Schelberg
David Shattuck
John Sherwood
Niranjan Sheth
Stephen Shirron
Donald Simon
Susan Slane
Mark Sorenson
Dean Sovie
Douglas Stefanelli
John Stevens
Mark Stiles
Cheri Vaillancourt
Patricia Vanolinda
Paul Waitkus
Thomas Webb
Ralph Weber
Paul Wesolowski
Richard Woodbury
Douglas Williams
Paul Yamartino
Stephen Zalewski

15th

Jay Akers
Barbara Altman
Susan Azibert
Susan Baust
Alan Belancik
Carolyn Belman
Roger Bisbo
Paul Brodeur
Charles Butala
Thomas Cafarella
Clemmie Collins
Ernest Crocker
Paul Destefano
Robert Dickson
Thomas Donahue
Donald Dossa
Parmellee Eastman
Michel Fein
Gail Barlow
Carl Gibson
Clair Grant
James Grochmal
Peter Grosse
Michele Hakala
Mark Hamel
Walter Hamel
David Hartwell
Gerard Herviux
Susan Hunt
William Hunt
Jaclynn Jones Real
William Kelly
Wilbert Knight
Adam Kojnok
John Koziol
Patricia Kulak
Charles Landino
Robert Rappaport
Joseph LaRose
James Leahy
Ray Lin
Daryl Long
John Lyons
Jack Mason
Clare Matthews
Paul McGown
Bruce Meacham
Jonathan Montague
Kathleen Morse
Cynthia Murrey
Roger Niles
Vincent Orgovan
Edward Paderson
Charles Parsons
Mark Pascarelli
Dominic Gasbarro
Robert Rabello
Bary Poland
Robert Richard
Frederick Roemer
John Shoreman
Robert Sibley
James Stegeman
John Stockwell
Louis Tancredi
Carol Udall
Anthony Vaccaro
David Vaughn
Donald Villani
Robert Willard
Richard Willett
Robert Wilson
Mark Yanow
Anthony Zacconi
Doris Langlois
Pete Rego

20th

Gary Andries
John Andruszkiewicz
Fred Carberry
Andrew Corcoran
Roger Dame
Sheila Deneault
Mary Ann Derzius
John McAllen
Linda Greska
Paul Guglielmi
Anthony Lacobone
Vincent Kalinwoski
Arthur Lemieux
Ronald Sommer
Jay Nichols
Robert Pratt
Dick Scheib
William Gaillardet
Don Smelser

Victor Souza
Michael Thomas
Robert Wolf

On 6 June 1966, Joe McMullin and John Keddy met for the first time on their first day as Digital employees. Initially, they chose separate paths within Digital, but in August 1987 when John joined ESB, they were once again together on MLO5-5. Joe had joined ESB three years earlier in August 1984.

Joe McMullin Celebrates 25 Years

Joe has not moved around much in his 25 years at Digital. He spent 18 years within the Large Computer Group (PDP-6, PDP-10, DECsystem 10, DECsystem 20) moving from MLO5-5 to Marlboro. In 1984, Joe returned to MLO5-5 where he has spent the last seven years in ESB. Joe is now sitting at pole 27D, just a few feet from pole 27A where he started 25 years ago. The two organizations in which Joe has worked have changed their names several times giving the impression to the uninformed that Joe has been more mobile than he has. However, Joe has moved vertically; he started as a Wireman and as he accumulated substantial practical knowledge of how things get done, he moved up thru the ranks to become an Engineering Operations Manager.
Joe has recently taken on two new assignments that were not even in thevocabulary until recently. He is the ESB Environmental Product Management Program Manager and the ESB Benchmarking Manager. He is demonstrating the enthusiasm of a 25 year-old and not that of a 25 year veteran. We all look forward to Joe's next 25 years.

John Keddy Celebrates 25 Years

John was the Supervisor of the Field Service Logistics group during his first several years at Digital. He was a member of the team that created the logistics organization that supported Field Service Engineers worldwide. Many of the policies and procedures that the team developed in conjunction with the Product Managers in Field Service are still being followed today.

John worked in Finance, Manufacturing, Sales Support, and then he returned to the Service organization. This variety of assignments combined with John's practical and conscientious pursuit of results make him an invaluable person within ESB.

His current assignment as an Engineering Operations Analyst is as varied as his whole career has been. John's several assignments include: space management for ESB, management of the disposition of Non Revenue Units (NRU's) after product development is complete, administering environmental recycling, product development support (KPL's, labels, etc.), and several more.

Lou Klotz receives 25th Anniversary Award

VSS Manufacturing recently celebrated the 25th Anniversary Service Award for Lou Klotz, Strategic Long Range Planning Manager for DCSS Manufacturing - or as Lou puts it "100 quarters and counting".

Throughout his years, Lou has been instrumental in new product introduction in one form or another, from the initial days of PDP-8 manufacturing, through ten years in Low End product design. He spent four years with Manufacturing Test Applications and eight years with Mid-Range Systems manufacturing.

As an individual contributor Lou was involved in the design of the PDP-8E, TSS-8, PDP-8A, VT100, various low end options, and the corporations initial custom semiconductor designs. Lou's management involvement included the 1103L, Manufacturing Test Applications, Process Information Control Systems, Low End Memory Products and the introduction of Mid-Range Systems such as the VAX8800.

Lou is an avid boater and woodworker. He has been married for twenty four years to his best friend Patty. They have two children Richard and Dianne, and reside in Westford, Ma.

Promotions

Bill Demmer Announces Four New Engineering Vice President Appointments

"I am extremely pleased to announce the following Engineering Vice President appointments . . .

Tom Frederick, Vice President of Engineering

"I'm very proud to be named VP of Engineering, but I really believe that my promotion is the result of the success of my people, the engineers, manufacturers, marketers and STO personnel, who contribute toward making Digital's memory business the success that it is." Tom places great value on the cross-functional collaboration of his people, and he builds a strong team relationship among his groups through cross-functional meetings, goal sets, and measurements.

Tom has managed the memory organization since 1988 and his team has tripled volume, and aftermarket profits grew nine-fold from 1988 to 1991.

Having joined Digital in 1975 as Marketing Development Manager for the COEM business, Tom took on various responsibilities including that of International Commercial OEM business manager. In 1983, Tom joined the CSS organization as their Worldwide Field Marketing Manager and in 1985 moved to Europe to become the CSS European Area Manager. Tom returned to the States in 1988 and accepted his current position as manager of the memory organization.

Prior to "life at Digital," Tom had extensive sales and marketing responsibilities with IBM, Computer Sciences Corporation, U.S.A., and Barry Wright Corporation. Tom also served in the U.S. Marine Corps and received his B.A. from Brown University and M.B.A. from the University of New Hampshire.

Don Harbert, Vice President of the VMS Group

Don has been group manager for VMS responsible for development and business management of the VMS Operating System. Prior to the VMS management role, Don was manager of the Data Center Systems and Servers Group with engineering and business responsibility for VAX 6000, VAX 9000 and follow-on products for data center applications. Don joined Digital in 1981 as a manager in the Semiconductor Engineering Group and moved to the Mid Range Systems Group in 1983. Don obtained B.S. and M.S. degrees in electrical engineering from Iowa State University.

Continued on next page.

Jesse Lipcon, Vice President of Entry Systems Business Engineering

Jesse Lipcon holds bachelors (1965) and masters (1966) degrees from Massachusetts Institute of Technology, where he was elected to Tau Beta Pi and Eta Kappa Nu. He has 24 years of engineering experience, including the last 19 years with Digital Equipment Corporation. He has contributed in the areas of real-time I/O and data acquisition, design and evolution of the Q-Bus, design of the Ethernet physical channel, and development of the MicroVAX family of computer systems. He is currently V.P. of Entry Systems Business Engineering responsible for the MicroVAX family and VAX 4000 products and he is also a Corporate Consulting Engineer.

Bob Supnik, Vice President of Advanced VAX VMS Systems Engineering

Bob has been the Technical Director of VMS Systems and Servers which creates Digital's VAX VMS systems and is also the Director of the Alpha Program. He joined Digital in 1977 as Supervisor, then Manager, to the Storage Subsystems Group until 1978. From there he joined the CSD/LSI Microprocessor Group as Product Strategist where he worked for one year. In 1979, Bob became CSD/LSI J-11's Project Manager. He managed this project until 1981, at which time he became the Group Manager for the Semiconductor Engineering Advanced Development Group. While managing the SEG AD Group, Bob also became involved in MicroVAX Chip Project as Project Manager and Microprogrammer. He worked on the latter two projects until 1984, then became the Group Manager for the Semiconductor Engineering Microprocessor Development Group. During his years as Group Manager of the SEG MD Group, Bob received a promotion to Corporate Consultant Engineer, VLSI Technology, and also became SEG's Technical Director. Bob holds a BS in Mathematics and History from MIT; and an MA in History from Brandeis University.

. . . let us all extend heartfelt congratulations to each of these individuals for the significant contribution they have made to the Corporation."

Bill Demmer

Peter George Promoted to Senior Consultant Software Engineer

Peter George was promoted to the position of Senior Consultant Software Engineer in December 1991. This promotion is in recognition of Peter's technical contributions to DECwindows and to the OPEN VMS strategy and products.

Having played a key role in developing and selling the workstation software strategy which moved Digital from a proprietary windowing system (UIS) to an open strategy based on X-Windows, Peter was then the driving force behind the DECwindows program that implemented the new strategy. As initial corporate architect and then project leader for DECWindows V1, Peter drove the design, development, and delivery of both VMS DECwindows and of the components common to both VMS and ULTRIX. He worked across multiple software and hardware organizations to bring this large, complex project to market. During this time, Peter was widely recognized not only for his delivery of the VMS software but for technical and project management skills that enabled the necessary collaboration across many organizations making significant contributions to the DECwindows program.

In addition to Peter's work on DECwindows, he conceived the original OPEN VMS strategy, then became the OPEN Systems Technical Director and program manager. In this role, Peter drove the definition of related architectures and products. He coordinated the delivery of multiple products within and beyond VMS, contributing technical direction in particular to the VMS projects such as VMS POSIX V1 and Motif on DECwindows V3.

Peter joined Digital in 1980 after graduating from MIT with an MS/BS in Computer Science in Engineering. His initial contributions to Digital were in VMS V3 human interfaces and utilities. He became project leader and primary developer for DCL and associated facilities for VMS V3 and VMS V4. Then he served as developer, designer, project leader, and supervisor of VMS workstation software, delivering three versions based on the proprietary UIS windowing system before helping to champion the move to open systems. Currently, Peter is Technical Director of the VAX VMS Development and Release Group.

Peter has significant experience as a speaker at DECUS, CSO Technical Exchanges, and internal training events such as DVN broadcasts and Digital University. He has co-authored two papers: "The Making of a MicroVAX Workstation," Digital Technical Journal, Volume 2 (1986) and "VAXstation Useability," Conference on Human Factors (1986). In addition he was a contributor to the X Window System Standard in 1987.

Peter enjoys playing softball and is an enthusiastic (some say fanatic) member of the Digital Nashua-Merrimack Softball League. The Devos Team, on which he plays 3rd base, were finalists in the 1991 league championship series.

Laura Woodburn

Hai Huang Promoted to Consulting Engineer

It is with great pleasure that I announce the promotion of Hai Huang to consulting engineer. Hai has made significant contributions to the VMS Product and to Digital by his recent development of VAX Vectors and his overall contributions and expertise to the VMS Executive.

Hai is presently contributing to the Alpha VMS Executive, having been project leader for the Alpha VMS Exception Processing effort and now serving as project leader for the Alpha VMS Executive changes in support of POSIX.

Rod Gamache

Joel Emer Promoted to Senior Consultant Engineer

I am pleased to announce the promotion of Joel Emer to Senior Consultant Engineer. It is the result of 13 years of important contributions to research and product development at Digital.

Joel has a Ph.D. in Electrical Engineering from the Univ. of Illinois, and an M.S. and a B.S. from Purdue Univ.

Joel is an expert in performance modeling of computer systems, and has been instrumental in developing this technology and using it to improve our understanding of system behavior. This insight has led to important innovations in computer design. Joel's study of the VAX-11/780 micro-PC histograms showed how VAX programs spent their time, and helped designers focus on speeding up the high-frequency, time-consuming tasks. This work is acknowledged to be a major milestone in the development of RISC architectures.

Joel developed performance models for the VAX 8600 and the VAX 8200. Some of these programs are still being used to model today's Alpha systems. He led a research project to create a high performance VMS file server, which was productized as the Distributed File Service. During a two-year stay at MIT, he worked on the Mercury project doing research on heterogeneous distributed applications. Joel was a member of the original EVAX taskforce that led to the Alpha architecture.

Recently, Joel has worked on a project to increase processor performance through instruction level parallelism using multi-issue architectures and optimizing compilers. He has developed a compiled, event-driven performance simulator, which lets us model programs at very high rates. This allowed us to get early insight into Alpha performance on large programs.

I am sure all those who know Joel will join me in congratulating him on this well-deserved promotion.

Tryggre Fossum

Margarita Johnson Promoted to Executive Secretary

I am pleased to announce that Margarita Johnson has been promoted to the position of Executive Secretary reporting to me.

Margarita has been with Digital for five years. She joined the company working for the SEG/CAD ESPS Group as a Senior Secretary. From there she joined the SCIT Finance organization as an Administrative Secretary. Margarita then continued as an Administrative Secretary supporting the SCIT Q&R/PMO/SCU organization. She subsequently joined the Alpha Program Office and has been with us for two years.

Please join me in congratulating Margarita on her promotion.

Bob Supnik

Wilma Evans Promoted to Executive Secretary

The VSS Manufacturing and Operations organization is pleased to announce that Wilma Evans has been promoted to the position of Executive Secretary reporting to Dan Jennings.

A twelve-year employee of Digital, Wilma moved to New England five years ago from Chicago, where she worked for the Field organization.

VSS wishes Wilma continued success in the future.

Today's VMS: High Integrity Functionality and Open Systems Benefits

Steve Stebulis
VMS Product Management

Today's VMS operating system offers our customers solutions that best fit their particular computing needs. Customers that require a computing environment with the open system benefits of interoperabililty, application portability, and a consistent user interface across multi-vendor platforms can count on VMS to provide solutions. For customers that need a high integrity production systems environment where mission critical applications must not fail, VMS also provides a solution to their computing requirements. And for customers that need an environment that requires both open systems and production system capabilities, VMS offers them a solution.

VMS, today, adheres to more industry standards than any other "proprietary" operating system. In February, Digital will deliver on its commitment and ship VMS POSIX to customers wanting their environment to be POSIX compliant. Customers running VMS POSIX can run POSIX-compliant applications on their VMS platform. VMS will be one of the first proprietary operating systems in the industry to deliver the POSIX 1003.1 standard for basic system services, and support the late draft proposed standards of 1003.2 for shell and utilities services and 1003.4 for realtime portability.

Today, VMS also offers the superior functionality that it has long been noted for. And Digital continues to enhance and improve this functionality as is inherent in its last two releases – VMS Version 5.4-3 (aka Sigma) and VMS Version 5.5 (aka Magic).

VMS Version 5.4-3, a maintenance update to VMS Version 5.4, started shipping to customers in October. This release of VMS provides a number of bugfixes and a few enhancements to the V5.4 release. These fixes are the latest in a series of updates meant to produce a more stable and robust production system environment.

VMS Version 5.4-3 introduces proactive memory reclamation that is designed to reclaim memory from inactive processes when a deficit is first sensed but before the memory resource is depleted. Pro-active reclamation of memory typically maintains a sufficiently large cache of free pages so that active, demanding processes do not have to wait for reclamation to take place. Therefore, response times typically improve in memory constrained environments.

In previous versions of the VMS operating system, while inactive processes continued to retain unused memory, active processes frequently were not allowed to grow when memory was con-strained. When using systems that perform memory-intensive ac-tivities where little free memory was available, users typically experienced perceptible delays while the system attempted to reclaim memory by trimming and swapping. Overall system performance is expected to improve as the system makes memory currently consumed by idle processes available to active processes.

Another feature of this release is support for Local Area VAXcluster (LAVc) over Digital's Fiber Distributed Data Interface (FDDI) adapter called the Digital Equipment XMI to FDDI Adapter (DEMFA). Version 5.4-3 supports the use of the DEMFA in multiple adapter LAVc configurations as an Ethernet adapter replacement.

Today, VMS also offers the superior functionality that it has long been noted for. And Digital continues to enhance and improve this functionality as is inherent in its last two releases –VMS Version 5.4-3 (aka Sigma) and VMS Version 5.5 (aka Magic).

VMS Version 5.4-3 also provides support for the use of up to four Local Area Network (LAN) adapters on each local area VAXcluster system. Previous versions of VMS allowed the use of only one LAN adapter for each local area VAXcluster system. Adapters can be either Ethernet or FDDI.

VMS Version 5.5 is the first functional release of VMS since version 5.4. This release has new capabilities that support Digital's position as a powerful production system environment while en-hancing its open system strategy.

VMS Version 5.5 software supports the following new CPUs:

- VAX 6000 Model 600 series systems
- VAX 4000 Model 500 systems
- VAXstation 4000 Models 60 systems and VLC (Very Low Cost) systems
- MicroVAX 3100 Models 30, 40, and 80 systems.

VMS Version 5.5 software contains a major rewrite of the internals of the VMS batch/print facility. No documented interfaces were changed as a result of this rewrite. These changes to VMS 5.5 provide improved scalability and performance for larger configurations, automatic failover of the queue manager for higher availability, and improved management and end-user features such as user specified job retention and batch time stamps to show time of job step completion. This redesign also includes an extensive change in the queue file database format and usage. In the VMS Version 5.0 job controller, the queue database is implemented as a distributed database that is shared among all the nodes within a VAXcluster system. In the new design, the queue database will not be distributed. A single queue manager will access its queue database on behalf of all processes in a VAXcluster system. Another feature of this new subsystem is the ability to automatically move queues from a failing VAXcluster node to a specified alternate node ensuring high availability.

Another feature of this release is Cluster-wide Tape Server Support. The VMS TMSCP server enables cluster-wide access to TMSCP-compliant tape controllers/drives. It can provide access to all VMS supported TMSCP tape controllers, regardless of local interface. It supports satellite access to HSC-connected tape drives in mixed-interconnect VAXcluster systems, as well as cluster-wide access to locally connected TMSCP controllers. TMSCP tape server support extends the resource sharing advantages of VAXcluster systems by providing tape access on a cluster-wide basis.

VMS Volume Shadowing Phase II (host-based) support has been extended for SCSI disks, thus extending shadowing to a wider range of disk devices and hardware configurations. VMS Volume Shadowing Version 5.5 also increases the number of shadow sets supported in a VAXcluster system from 32 to 75.

DECdtm Version 1.1 provides maintenance and extensions to the DECdtm facility. Other extensions supported with this release include direct support for transaction timeouts and extended reason codes for transactions.

A feature that has long been asked for in the VMS file system is the ability to "atomically" move a file. This feature is critical to building safe disk defragmentation packages. The file system provided in VMS Version 5.5 has this feature. "Atomically" moving a file means it is either moved completely and contiguously, or it is not moved at all. This "movefile" service in the file system will automatically exclude critical system files, assuring that defragmentation cannot disrupt system uptime. This new functionality has been crucial in building a Digital online disk defragmentation product for VMS. This disk defragmentation product will be a layered product, licensed separately. The primary goal of the product is data integrity. This function provides a safe and reliable means upon which Digital (and third-parties) can achieve Online disk defragmentation, Online disk optimization and Online optimization of indexed files.

In addition to the production system features described above, VMS version 5.5 provides the underpinnings for new open system features in VMS. Some changes have been made to the base operating system to facilitate the layering of a future release of the VMS POSIX layered product on VMS. The VMS POSIX layered product will add IEEE POSIX 1003.1, 1003.2 and 1003.4 interfaces to the VMS operating system. These interfaces define a set of system services; application developers can rely on these services being on any vendor's system claiming POSIX conformance. As a result of these services, applications written with POSIX services can be ported at the source code level to any vendor's POSIX conforming systems.

The VMS POSIX layered product will incorporate all of these standards to conform to government requirements and provide a rich set of development utilities and realtime extensions necessary for developing portable POSIX applications.

Continued on next page.

In addition to the POSIX capabilities available with VMS V5.5 and the VMS POSIX layered product, DECthreads services are available with this release. DECthreads services are part of the Open Software Foundation's Distributed Computing Environment and are based on the IEEE POSIX standard 1003.4A. DECthreads are a user-mode run-time library that allows a program to create and control multiple threads of execution within a process. DECthreads services provide both a stable, upwardly compatible interface and an open, POSIX-compliant interface. DECthreads services are a completely new facility. These runtime- library routines provide a set of portable services that support concurrent programming. The DECthreads RTL services provide an API usable from all VMS languages and a C only API that conforms to the draft POSIX 1003.4A PThreads standard.

DECthreads services include operations to create and control threads and to synchronize access to global data within an application. DECthreads services allow an application to perform many actions simultaneously, which will likely result in an improvement in the overall performance of the application. DECthreads services execute at the same time by overlapping computation with I/O and other events that stall a portion of the application.

VMS Version 5.5 begins shipping to new hardware customers in late November and will be generally available in late January. This release strengthens Digital's commitment to be the high integrity open systems vendor offering our customers solutions to their computing requirements with it's VMS Operating system.

VAXstation 4000 VLC

John Kirk
Senior Consulting Engineer

One of the two newest members of DEC's VAX-based workstation family, the VAXstation 4000 VLC offers considerably lower price and significantly better performance than the VS3100 Model 38 that it supersedes.

Based on the Digital/Hudson designed and manufactured DC222 VAX Processor chip, the VLC achieves 6 VUPs performance and with an integral 2-D graphics accelerator, provides industry leadership graphics performance for this class of machine,10-pixel vectors are drawn at greater than 150,000/sec.

The DC222 is fabricated in Hudson's CMOS-3 (15) process and packaged in a low cost, 132-pin quad flatpack package with 25 mil lead spacing. It combines in a single chip, the Integer and Floating point units and clock generator of the previous generation CVAX three chip set and increases the on-chip cache from 1 KBytes (CVAX) to 8 KBytes.

Low component count is a feature of the VLC, the entire System Module comprises only some 30 ICs, excluding RAM. Each 8 MBytes (up to the maximum of 24 MBytes) of RAM is plugged in as a pair of SIMM assemblies that each add only 12 chips to this total.

Open Box

An equally striking feature is overall physical size – the entire machine, including power supply, space for 24 MBytes of system memory and an optional 120 MB hard disk drive is housed in a desktop enclosure that measures only 2.4" x 15.5" x 14.5" and weighs less than 9 lbs.

The VLC and the second newly announced workstation, the VAXstation 4000 Model 60, share a common design for memory, standard I/O and graphics. The Model 60 uses the higher performance DC595 (Mariah) CPU chip together with its separate FPA and clock chips and has a large second level cache. The common components are interfaced directly to the DC222 pin bus in the case of the VLC and via a "personality ASIC" that converts the DC222 pin bus to the Mariah CPU bus and controls the CPU second level cache in the case of the Model 60.

Standard I/O includes four programmable speed asynchronous serial lines, one with full modem control; SCSI bus, for both the optional RZ23L internal disk and external SCSI devices; Ethernet controller; Time of year Clock with Non-volatile RAM; sound I/O chip for audio input and output; 256KB of ROM for power-on self-test, bootstrap code and integral graphics accelerator. To allow the user flexibility in his/her choice of video monitor, the actual frame buffer is a plug-in option module, allowing (at present) either 1024 x 768 or 1280 x 1024 screen resolutions. Both frame buffers are 8 plane, the lower resolution selectable for 60 or 72 Hz. vertical refresh rate, the higher resolution one refreshing at 72 Hz.

As mentioned above, low chip count is a feature of the VLC, this is achieved by high integration. In addition to the space savings made possible by the new CPU chip, three custom designed gate arrays are used in the VLC design. At the heart of the VLC (and the Model 60) is a 223-pin Ceramic Pin Grid Array (CPGA) custom chip, the DC7201, which has approximately 83,000 gates. This chip connects directly to the 32-bit address/data bus of the CPU chip and controls all the machine functions. It spawns two further busses; a 16-bit bus (EDAL) to which the I/O device controller chips are connected and a 32-bit bus (MDAL) for memory – both system memory and the graphics frame buffer. Memory is actually organised 64-bits wide for performance reasons, but multiplexed down to 32-bits for connection to the MDAL – a second 144-pin gate array chip performs this multiplexing (and data latching) function.

The DC7201 controls the memory timing and outputs memory addresses and control signals directly, providing support for\up to 24 MBytes of system memory. It also performs all the device decoding for the peripheral controller chips attached to the EDAL bus and implements internally the serial line controllers, including a 48 entry receive data FIFO. Another major portion of this chip is the graphics accelerator – known as LCG for Low Cost Graphics. This is another processor in its own right, it accepts commands from the CPU via a FIFO buffer that resides in system memory, processing the commands put there completely independently: line drawing, area fills, block moves of data, either within the frame buffer or between the frame buffer system memory are all implemented in hardware and operate in parallel with CPU operations. The VLC has up to 15 times the vector drawing performance of the VAXstation 3100 Model 38.

Two of the peripheral controllers, SCSI and Ethernet, perform DMA transfes to/from system memory. Here, again the DC7201 is involved. The peripheral controller data flows through the DC7201 – MDAL <–> EDAL and the DC7201 performs data buffering and mapping from the address supplied by the peripheral controller to non-contiguous pages in system memory as necessary; what is usually referred to as scatter/gather mapping. The graphics accelerator can also read and write main memory in addition to its normal operations on .he frame buffer; in fact this is one of the major features of the LCG, the ability to "draw" to any piece of memory. As many graphics operations require drawing to off-screen memory, this is a major advantage as off-screen memory can be a part of the system memory, allocated as needed, rather than having to add more Video RAMs as an extension of the frame buffer for this capability. The graphics accelerator can also directly control copies to/from system memory and frame buffer memory.

Related to the DMA and graphics accelerator system memory operations is one last feature of the DC7201 – the ability to offload the CPU during these DMA and graphics accelerator write (to system memory) operations. As the CPU

has an internal data cache, when one of the DMA controllers or the graphics accelerator writes to memory, it is possible that the location being written may also be contained in the CPU data cache. To prevent the CPU from possibly reading stale data from its cache, it is thus necessary to invalidate this cache entry as main memory is being updated by the DMA or graphics writing to it. This is normally done by passing the DMA address to the CPU during every such write cycle and letting the CPU decide whether or not to invalidate that line in the cache. To filter out uncessary invalidate requests from being passed back to the CPU, a copy of the entries in the CPU's cache tag store is kept in a separate SRAM memory connected to the EDAL - the Invalidate Filter RAM. Every time a cache allocate occurs, the CPU outputs the address to the DC7201 to access system memory. The address is made up of two sections, the INDEX and TAG portions. The CPU cache is actually an eight-way set associative cache with each set being 1 KBytes, so during a cache allocate cycle, the CPU also outputs the set number on dedicated pins. The DC7201 takes this set number and uses it, together with the INDEX field of the memory address to address the Invalidate Filter SRAM. The TAG portion of the address is stored at this address. Subsequent DMA or graphics write operations perform a lookup in this Invalidate Filter SRAM to decide whether the CPU need be told to perform a cache invalidate or not.

In all, the VAXstation 4000 VLC is a highly optimized, busless machine that brings VAX VMS to a new class of users. Although it has no expansion bus, it incorporates as standard all the features that are necessary in a high performance workstation while allowing the user to add memory as necessary to suit the application and to add storage using external expansion boxes. A new expansion box, developed specifically for the VLC allows a 3=" floppy or hard disk to be added, packaged in a small desktop enclosure only slightly larger than the drive itself.

By knowing and controlling the configuration of the system closely, it has been possible to build a VAX VMS system using less power, occupying less space and able to be sold for a price more usually associated with PC class machines. All this while improving performance and maintaining software compatibility with previous generations of VAX workstations.

Complete system with SZ03 Expander Box

Admiral Hopper Remembered

Dick Willett

Rear Admiral Grace Murray Hopper (USNR Ret.) passed away New Year's Day at her home in Arlington, Virginia. She had celebrated her 85th birthday on December 9.

At the time of her death she was employed as a senior consultant at Digital Equipment Corporation, and until 18 months ago was actively representing the company at industry forums, making presentations that focused on Government issues and participating in corporate educational programs.

In September, President George Bush awarded the National Medal of Technology to Admiral Hopper for her pioneering accomplishments in the development of computer programming languages that simplified computer technology and opened the door to a significantly larger universe of users. She was the first woman to receive the award as an individual.

Ken Olsen, a long time friend and associate said, "Grace took every opportunity to challenge people, young and old, to consider the infinte possibilities of technology. We will miss her brilliance and humor."

Grace was buried with full military honors in Arlington National Cemetery in a service steeped in the rich Navy tradition that she loved. At her request, a simple standard issue stone, similar to thousands of others that stand row-upon-row in Arlington National Cemetery, marks her final resting place.

Rear Admiral Grace Murray Hopper

digital

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FOREFRONT

Alpha AXP and VAX Systems
21st Century Computing Today
Q2/Q3 FY93

Digital Announces Alpha AXP Worldwide

FOREFRONT

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FOREFRONT strives to support a forum for the entire AVS WW community to share information, directions, and key accomplishments in all its functional dimensions, that is, customers, markets, engineering, and manufacturing. Its goal is to highlight technical efforts and successes that lead to new products and markets for Digital.

This is your information forum. Your participation is vital to its continuation and success. You are encouraged to contribute articles that are of interest to the AVS community. The deadline for submitting articles for the next edition is January 15.

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Alpha AXP Announced Worldwide

On November 10, Digital announced a complete family of industry leading Alpha AXP workstations, departmental servers, data center servers, mainframe-class servers, and system software, plus a host of services, layered products, peripherals, and upgrade programs.

Alpha AXP and VAX Systems (AVS) and Workstation and Servers Group (WSG) personnel were key contributors at announcement events that spanned the world:

- Bill Demmer, Digital AVS Vice President, was the keynote product presenter at the primary Corporate event at the World Trade Center in Boston.
- Don Gaubatz, Vice President, Workstations and Servers Group, provided press and customers with the Alpha AXP story at the West Coast Corporate launch in San Francisco.
- Don Harbert, Vice President, OpenVMS Engineering, presented the Alpha AXP systems vision and details in Tokyo.
- Jesse Lipcon, Vice President, Entry Systems, was the technical expert presenting Alpha AXP product details in London.
- Bob Supnik, Alpha AXP Program Office Vice President, provided engineering support for Bill Demmer in Boston.

Other key AVS and WSG personnel who were instrumental in the launch of Alpha AXP systems around the world, included; Pauline Nist in Boston, Peter Graham in London, Duncan Anderson in Australia, Al McGuire in Brazil, Peter Conklin in Toronto, and Lou Philippon in Hong Kong.

In Boston, the announcement went off flawlessly. All of the speakers delivered very informative messages. Bill showed a number of charts, which clearly indicated the Alpha AXP advantages technically as well as competitively. Bob Palmer, Win Hindle, and Bill Demmer sat together on a panel to entertain a number of enthusiastic questions. At the end of the presentation Bill and Bob Supnik were surrounded by reporters, while they answered their questions.

"The Digital Alpha AXP products clearly overshadowed the announcements from HP and Sun."

All of the breakout sessions were well attended and the CSO demo area was very busy all day.

The "Beat the Alpha Clock" game show capped off the day at the Customer Reception. Customers and CSOs competed against each other to test their knowledge of Digital and the Alpha AXP system. The audience was completely captivated as they cheered on the contestants, and watched in amazement as the Alpha AXP system competed in a live demo against well-known competitive systems.

Much of the coordination and management of this critical announcement was done by the AVS and WSG Marketing organizations...who are to be congratulated for a great job in helping develop this worldwide, world-class announcement.

Here's what we heard from around the world:

Don Gaubatz – West Coast

"We did two events in three hours in San Jose. The customer event was first, where we presented the Alpha AXP product story to more than 1,000 customers. I was surprised by what a major show this was — there was a huge demo area with more than 60 systems staffed by key ISVs. People were very enthusiastic.

"Next we went to the press event. It was standing room only, with about 65 reporters. We repeated our presentations, and then had a very detailed question and answer period for about 30 minutes, followed by one-on-ones for another hour or more. Digital's announcement was the only event shown on the evening TV news, and I think the other stories we're seeing bear out how well our Alpha AXP story has been received."

Don Harbert – Tokyo
"The Alpha AXP vision and the Alpha AXP products were received with enthusiasm by over 130 members of the daily and computer industry press core. Headlines included:

'DEC Japan to Sell Workstations and Servers with Mainframe-Class High Performance,' *Nihon Keizai Shimbun*

'DEC Japan Announced the World's Fastest Server with 64-Bit MPU,' *Nikkei Keizai Shimbun*

"The products were also received with enthusiasm by over 400 customers during a special presentation on November 13. The Digital Alpha AXP products clearly overshadowed the announcements from HP and Sun."

Jesse Lipcon and Peter Graham – London
"The UK management team hosted a first-class customer event on the day before the announcement at the Cafe Royale in London. After the event one major customer said to Peter Graham, 'Thanks for inviting me to come. The presentations were OK, the lunch was excellent, and we're going to buy some Alpha AXP systems.'

"At the London press event Peter and I handled the 'Alpha AXP Update' sessions for press from all over Europe. Feedback was uniformly positive, especially that Digital had met its committed schedule for Alpha AXP product shipments."

Duncan Anderson – Sydney, Australia
"The reaction in Sydney was stunning! The game plan 'Downunder' was three-fold—customer, customer, and customer. We hosted key current and new prospective customers across the continent in a ten-day series of events.

"Customers clearly voiced back to us their overwhelming acceptance of Digital's new strategy, business practices, and products."

"Going into these events, the primary questions in our customer's minds were: 'Can Digital continue to be my strategic partner for the long haul? Will Digital make it through its current financial difficulties? How difficult will the transition to Alpha AXP systems be for my company?'

"Customers clearly voiced back to us their overwhelming acceptance of Digital's new strategy business practices and products. They saw this announcement as more than a product announcement but as a stunning rebirth of a *bold, new* Digital, better suited to meet its changing and diverse computing needs."

Peter Conklin – Toronto
"We had an excellent customer turnout and a very professionally staged event. Their response was excellent! No difficult questions were asked. And the comments we picked up about the HP and SUN announcements were very encouraging.

"On Monday morning, we hosted a non-disclosure breakfast with 30 to 40 analysts. One customer asked how our high-performance systems would put demands on networks. We answered with the FDDI story. Another asked for clarification on our UNIX plans—given the Olivetti announcement. We explained both the System V plans Olivetti has (very briefly), and our strategy of OSF/1 with applications support for System V, Berkeley, and AES 'habitats.' In fact, we added this to the product speech to help others understand this during the customer meetings.

"Toronto has a very small trade press, so we handled them with a non-disclosure briefing Monday afternoon. This gave us a trial run for Tuesday and more time for customers.

"On Tuesday, we hosted two customer sessions, one in the morning and another in the afternoon. The stage was formed from our standard trade show booth with window-like blinds that had the Alpha AXP logo as a backdrop surrounding a dual rear projection screen. The presenters used TelePrompTers and the result was excellent. The

SAS Canada president was the special speaker and did a marvelous job. At the end of the presentations, the curtains parted to reveal the demo room behind the stage and the final speaker invited the audience to join us as we started the journey into 21st century computing. The audience stampeded over the raised stage into the demo room and looked at the demos for an hour or so.

"Between the two sessions, we had approximately 500 customers and prospects. The local Marketing team had run ads the Friday before and the response was excellent. Audience feedback was extremely positive; I heard no negatives. One customer left Digital ten years ago and had became a SUN customer. He had been to SUN's announcement that morning and his comment was 'SUN is abandoning their customers, but Digital is now back in technical computing!' Another customer has been an avid HP workstation purchaser. His comment was 'Last month we bought our last HP workstation.'

"All in all, the event was very worthwhile. The Canadian marketing and event teams are to be commended. They decided to work jointly with SAS to start an aggressive selling campaign to sell AXP workstations into all the mainframe SAS customers in Canada. With programs like this, Canada will become one of our AXP leaders!"

Lou Philippon – Hong Kong

"About 40 members of the press and consultants from the Asia region welcomed the Alpha AXP Systems announcement at the Digital facility, hosted by Bobby Choonavala, President of GIA. The attendees marveled at the display and full operation of the Alpha AXP workstations and the Alpha AXP departmental system. Tony Leung, Asia Region Marketing Director, aired a live, fifteen-minute interview for a local business Hong Kong radio station, a first in this part of the world for Digital. In addition to the systems announcement and live demos, the members of the press were particularly astounded by Bobby's announcement that over 20 Alpha AXP Systems orders had been received within the Asia Region.

"The consultants, and the more technical press, were particularly fascinated by the speed at which the Alpha AXP workstations executed the Mandelbrot Set benchmark vs HP and SUN workstations. I highlighted the basic workstation, server, and software capabilities, noting their orderable, shippable state. The general manager of the SAS Institute provided the best live customer proof points that the press could get anywhere—ease of migration, quality of migration tools/services, and dramatic performance improvements. Additionally, the local Hong Kong, Chinese, and English press carried innovative half-page ads touting our messages of the unique 64-bit technology systems vs the competition.

"Asia Marketing will be conducting appropriate customer Alpha AXP announcement events within their respective countries in the weeks to come, covering the countries of Korea, PRC, the Philippines, Malaysia, Taiwan, Singapore, India, Indonesia, etc. The GIA Asia Region team looks forward to very successful Alpha AXP sales activities in FY93 as a means of exceeding their 25 percent plus annual revenue growth."

Al McGuire – Brazil

"The Alpha AXP product was kicked off through several events. The country management put tremendous support behind Alpha. They translated the videos into Portuguese and worked to get many customers and prospects to attend the events. The formal press introduction took place in Sao Paolo with about 30 members of the press. Most of the questions were about Brazilian business issues and local product availability.

"The plan was to present the same materials at 6PM to 300 invited customers and prospects. We had to wait an extra half hour because customers couldn't park their cars due to the traffic jam. Instead of the planned 300, 517 actually showed up. They were standing 20 deep across the back of the room. They gave a long applause at the end of the product presentation, which was followed with a reception.

"On November 11 we went to Rio De Janiero to do the same presentation for the local customer base. They planned on 250 attendees, but over 300 showed up . They were just as enthusiastic as the Sao Paolo audience.

"I expect that we will see far more business with Alpha because of aggressive Alpha AXP products, a very energetic new country management team, the merging of Digital with MicroTec (the biggest PC distributor in Brazil) and new import policies that are just starting. The opportunity in Brazil is tremendous."

World Trade Center, Boston

Digital Introduces Alpha AXP Computing

Meeting Customer Needs with New Systems, Software, Applications, Services, and Business Practices

Alpha AXP Computing is a complete set of systems, software, applications, and services with new business practices that provide a universal platform enabling unlimited open computing possibilities.

Alpha AXP computing, the first advanced 64-bit, twenty-first century architecture, is a major technology milestone for the computing industry. For Digital, it reflects a renewed determination to help customers succeed. Alpha AXP computing enables users to:

- Run today's commercial and scientific applications faster, at lower cost
- Use today's applications in more innovative ways, such as downsizing mainframe applications to client/server networks
- Explore fully advanced applications such as virtual reality, imaging, multimedia, artificial intelligence, language translation, advanced simulation, and voice recognition

"Today is the beginning of a new revolution in computing," said Bob Palmer, President and Chief Executive Officer. "With nearly limitless 64-bit computing power, and the applications of three major operating systems, the path ahead leads wherever the imagination can take it. Alpha AXP computing will enable customers to invent profitable new ways to serve people."

"The new products and services announced mark the next phase of our Alpha AXP roll-out, which demonstrates that Digital satisfies customer needs today, and has the partners, products, services, and commitment to continue to satisfy their needs well into the twenty-first century," he added.

New Products

- The first universal platform — Alpha AXP — offering a choice of three open software environments, a choice of open standards, and a choice of hardware and network interconnects.
- A family of Alpha AXP systems, ranging from the industry's most powerful desktop workstation to the industry's most powerful mainframe-class server.
- A comprehensive software suite of languages, tools, and utilities, and commitment from more than 1,000 vendors to port more than 2,000 applications to the Alpha AXP platform.
- A complete new portfolio of services to help customers gain the benefits of Alpha AXP technology for their existing environment and for new applications.
- Enhancements to Digital's Alpha AXP ready upgrade program to make it attractive for customers to buy VAX- or MIPS-based systems today and upgrade to Alpha AXP systems in the future.

"The Alpha AXP announcement returns Digital to its strongest competitive position in years. It is the result of a massive company-wide effort involving all of Engineering, Marketing, Sales, Service, and Manufacturing — as well as over 1,000 application and system partners. This announcement is only one in a series of planned major Alpha AXP announcements," said Win Hindle, Digital Senior Vice President.

"Today is the beginning of a new revolution in computing. With nearly limitless 64-bit computing power, and the applications of three major operating systems, the path ahead leads wherever the imagination can take it. Alpha AXP computing will enable customers to invent profitable new ways to serve people."

Bob Palmer

The Universal Platform for Universal Platform for Open Choice

Alpha AXP computing goes beyond "open" to create the first universal platform. It provides choice of operating system software, open standards, popular peripherals, and vendors. Since no one software

Front row, l-r: DEC 4000 AXP Server, DEC 3000 Model 500S AXP Server, DEC 3000 Model 400S AXP Server (on pedestal), DEC 3000 Model 400 AXP Workstation, and DEC 3000 Model 500 Workstation.

meeting the specifications agreed to by UNIX System Laboratories and the Open Software Foundation for a unified UNIX software platform. This means it is able to support applications written to all the popular UNIX variants — including System V, OSF, and Berkeley derivatives such as the ULTRIX operating system. A software development version is available now, and volume shipment of an end-user version will begin in March, 1993.

The OpenVMS AXP operating system provides the world's highest functionality software environment — with features that deliver leadership data protection, integrity, availability, and scalability. The OpenVMS AXP operating system is available now. The Windows NT operating system will provide the familiar Microsoft Windows environment on the fastest hardware platform in the industry.

The universal platform will provide a choice of popular open standards, including: POSIX, SQL, TCP/IP, OSI, ANSI languages, and others. The universal platform also will provide a choice of popular hardware interconnects — EISA, SCSI-2, TURBOchannel, VME, Futurebus+, Ethernet, and FDDI — so all popular peripherals and networks can be used.

Unbounded Performance; Cost-Effective for Decades

AXP system performance begins where 32-bit reduced instruction set computing (RISC) systems leave off. Unlike IBM, Hewlett-Packard, and Sun RISC systems, Alpha AXP computing offers 64-bit addressing — four billion times the data addressing capacity of current 32-bit systems.

For example, 32-bit addressing can directly address all the words in 111 file cabinets. Sixty-four bit addressing provides the power to address all the words in a row of file cabinets stretching around the world 5,000 times.

"Our goal is to create the 64-bit universal standard. Sixty-four bits will enable the full potential, at affordable prices, of entire application arenas that are only being experimented with today, such as multimedia, imaging, and virtual reality," said Bill Demmer, Vice President, Alpha AXP and VAX Systems.

"Today's first Alpha AXP systems set new industry performance records, and Alpha AXP technology will sustain that performance for decades. The Alpha AXP architecture is operating-system independent and we are aggressively partnering at all levels of integration. Twenty-first century computing starts today," he added. These new products include a family of workstations and servers based on the Alpha AXP architecture. They offer the best price/performance in the industry among systems in their respective classes from IBM, H-P, or Sun Microsystems. The new Alpha AXP models offer leadership performance across a wide range of industry-standard benchmarks, including SPECfp92, SPECint92, and SPEC89.

DEC 3000 AXP Workstations

Workstation Model 400 offers 107.5 SPECmark89 units of performance and Model 500 offers large expansion capacity. Digital will also introduce additional workstations,

The Model 400 (left) breaks the 100-SPECmark performance barrier and the Model 500 offers large expansion capacity.

and EISA-based AXP systems running Windows NT in the first half of 1993.

Alpha AXP Servers

Server versions of the two DEC 3000 AXP workstations offer very high performance. DEC 4000 AXP servers offer multiprocessing, powerful Futurebus+ I/O, twice the expansion of competitive models, and up to 247.0 SPECthruput. The DEC 7000 AXP data center server is the most expandable data center system in the industry in processing power, I/O, disk and memory capacity; it delivers 604.4 SPECthruput89. The DEC 10000 AXP mainframe-class server uses the fastest microprocessors in the industry — 200MHz, delivers over 654.6 SPECthruput89. The DEC 3000 AXP, DEC 4000 AXP, and DEC 7000 AXP servers are available now; the DEC 10000 AXP server will be available in the first quarter of 1993.

Solutions for Competitive Business Advantage

Today, more than 2,000 applications from 1,000 vendors are already committed to run on AXP systems running the OpenVMS AXP or DEC OSF/1 for Alpha AXP operating systems. To support application migration, Digital has shipped more than 800 AXP systems to software developers and opened more than 30 Application Migration Centers worldwide.

Digital's staged software delivery is on schedule, with software products for applications developers available on both DEC OSF/1 for Alpha AXP and OpenVMS AXP systems. The 19 layered software products announced include DEC FORTRAN and DEC C compilers, DECnet networking and DEC Rdb database.

The next stage, a complete CASE and run-time environment, is available to all developers through Digital's Application Migration Center programs. Services is an integral part of Digital's Alpha AXP solutions capability. Digital leads the industry in multivendor open services, servicing more than 14,000 products from 1,300 vendors. Digital offers a dedicated set of multivendor services focused on smoothly integrating Alpha AXP technology with existing multivendor environments. Digital is committed to support its partners with the same level of service as for its own products.

Front row, l-r: the DEC 3000 Model 400S AXP Server, the DEC 3000 Model 500S AXP Server, and the DEC 4000 AXP Server. Rear, l-r: the DEC 10000 AXP Server and the DEC 7000 AXP.

The expanded services portfolio includes new migration, training, and consulting services that help UNIX, OpenVMS, and Windows NT customers easily move to Alpha AXP-class computing. New design-in and support services help Digital's Alpha AXP partners build, deliver and support Alpha AXP-based products.

Digital's goal is to give customers the widest choice of leadership solutions across the broadest range of market segments. Digital is actively recruiting partners and will sell its products at all levels of integration — chips, boards, system, boxes, software, solutions, and design — and will license intellectual property in alliances that will broaden the Alpha AXP market.

There are now more than 35 Alpha AXP partners, including Olivetti, Cray Research, Kubota Pacific, Aeon Systems, and Raytheon.

Alpha-Ready Upgrade Program Protects Customer Investments

All OpenVMS VAX and ULTRIX DECsystem products are "Alpha-ready." They support the same software, data, applications, networks, clusters and peripherals, as Alpha AXP systems. This means that over 85 percent of customers' typical computing investments in hardware, software, and training are protected. With Alpha-ready upgrades, Digital protects the other 15 percent of customers' investments — the central processor itself. With today's Alpha AXP announcement, Digital has improved its Alpha-ready Upgrade Program dramatically.

Alpha AXP Partners Program

Partnering Alpha AXP Systems

Mary Kulas

Back row, l-r: Roger McIntyre, Margaret Brender, John Doherty, Mary Kulas, and Paul Curtin. Front row, l-r: Ed Barker, Julaine Hansen, and Susan Blownt.

Digital intends to make Alpha AXP the predominant computing architecture of the 21st century. In order to do so, Digital plans to:

- Create a large market for Alpha AXP based products
- Build industry-wide support and momentum
- Expand into markets which Digital has little or no current business.

Partnerships are key to Digital's ability to accomplish these goals. Bill Demmer created the Alpha AXP Partners Program Office in July in recognition of the integral role partnerships will have in establishing the Alpha AXP technology as an industry standard and as a means of maximizing Digital's return on investment. The focus of this Program Office, managed by Paul Curtin, is to ensure the successful recruitment and support of system houses that will use the Alpha AXP technology in their future products.

The Program Office also works closely with other Digital groups that are working with semiconductor companies, OEMs, and software vendors. The Program Office recognizes that Digital's open business practices mean bringing technology to market at many different levels ranging from selling Alpha AXP chips, components, systems, and solutions, to joint design teams for customized Alpha AXP based components.

Announced Partnerships

Some of the partnerships that Digital has announced to date include:

- Aeon Systems, which developed the VMEAlpha64 CPU board.
- Andersen Consulting, systems integration partner, will use Alpha AXP technology to deliver new innovative solutions to their clients.
- Cray Research will use Alpha AXP chips in future massively parallel processing (MPP) products. The Alpha AXP microprocessor will allow Cray to complete one initial MPP system this year and to demonstrate to their customers over 100 Gflops of performance.
- Encore is building a high-performance UNIX platform using Alpha AXP technology.
- Kubota Pacific Computer is integrating the Alpha AXP processor with their own new graphics technology to produce the industry's most advanced 3D graphics and imaging solutions.
- Raytheon developed a ruggedized, militarized workstation incorporating the Alpha AXP technology.
- Olivetti, a full systems vendor, will incorporate Alpha AXP technology into future products.

Background

The members of the Program Office have diverse backgrounds, coming from the Strategic Relations Group, Workstations, GIS/VSS, and Fault Tolerant Group. Paul Curtin, the group's manager, most recently worked as Business Development Manager for the Strategic Relations Group. He was responsible for a number of strategic deals, including Digital's relationship with Cray Research. Prior to this, he managed the New Computing Structures Group. He joined Digital in 1983 as Manager of External Relationships in Corporate Research.

Alpha AXP Achievements by OpenVMS and DECnet

Robert Supnik
Peter Conklin

US OpenVMS Alpha Team

At the Alpha AXP Quarterly on July 15, 1992, the Program Office announced the first recipients of the new Alpha Program Achievement Awards.

The recipients of the Achievement Awards are:

OpenVMS Alpha Team
DECnet Alpha Team

Both teams achieved the functionality planned over two years ago within their planned schedule. From a standing start to porting completion, each team produced quality software in the expected time frame, and actually increased the functionality promised originally. These teams achieved excellent schedule performance through solid program management, and demonstrated a high level of commitment to the program.

Achievement Awards

This recognition is presented by the Alpha AXP Program Office to engineering teams for either:

- Excellence in performance against committed Alpha AXP scheduling
- Achievement of competitive benchmarks

Future Awards

Awards for competitive benchmarks will be presented to teams that have demonstrated they have:

- Determined competitive benchmarks
- Set goals to achieve benchmark
- Established a process to measure their progress
- Achieved competitive benchmark

These awards reinforce the Alpha AXP Program's goals of world-class program execution in terms of

Livingston, Scotland OpenVMS Alpha Team

Certificate of Alpha Achievement

Presented to the *OpenVMS Alpha* team

In recognition of excellence in schedule performance *over an aggressive two-year program.*

Robert M. Supnik, Vice President Alpha

Peter F. Conklin, Alpha Product Director

July 15, 1992

speed and quality. Future awards will be announced by the Program Office throughout the year to teams who complete these objectives.

Congratulations to the OpenVMS Alpha and DECnet Alpha teams for their outstanding performance.

DECnet Alpha Team.

Alpha AXP Distributed Systems and Cray Supercomputers

A Total Digital Solution for High-Performance Technical Computing

Karen Quatromoni

This past January, Digital announced it would sell, market, and distribute Cray Y-MP EL supercomputers. This particular Cray model is an air-cooled, entry-level supercomputer that easily integrates into Digital's open distributed computing environment. Digital is uniquely positioned to win many opportunities in high-performance technical computing (HPTC) environments with Cray supercomputers and Alpha AXP distributed systems, the DEC 4000 Model 600 systems, which complement the Cray systems. Here's why.

Almost all Cray systems are sold as part of a network of integrated systems. There are a number of reasons for this. A Cray system is sold primarily for its ability to run multiple copies of very large, numerically intensive floating point applications, most often in batch mode. Smaller systems are also used to collect and analyze data, which is then sent to the Cray Y-MP EL for processing.

Most customers access information through workstations or servers. It is therefore less expensive for users to prepare their work directly on the networked Alpha AXP system in an interactive fashion because it frees up production supercomputing time for the users. Both systems are doing their assigned tasks in the most cost effective manner for the users.

DEC 4000 Model 610 AXP systems "back-end" a Cray Y-MP EL supercomputer. Cray systems integrate very well with Digital's Alpha AXP systems.

Today Cray systems are sold with a variety of RISC workstations and systems from many vendors, including Digital, SUN, and IBM. But Digital's Alpha AXP distributed systems are especially well-suited to complement Cray systems. The first departmental system based on Digital's Alpha AXP RISC computer architecture, this system offers customers unparalleled power and performance, large amounts of memory and storage, and super-high speed networking. The Alpha AXP distributed system is ideal for CPU-intensive technical applications with a mix of floating point and integer requirements such as CAD/CAM and seismic analysis, to name just a few. The system is low cost and is sold in a package that can be placed virtually anywhere.

In addition, Digital's OpenVMS operating system, as well as OSF/1, works well with the UNICOS operating system, Cray's version of the UNIX operating system. These operating systems support standards such as the Network File System (NFS), used to pass data from one system to the other, FDDI fiber-optic networks, for high-speed communications, and many other standards.

But the most important reason Digital can win in this market is that Digital is the only vendor that can provide customers with a total supercomputing solution—a Cray supercomputer system, networked interactive servers, service, and support. For more information or help with Cray/Alpha AXP sales opportunities, call the Cray Helpline at DTN 297-4164.

Honing the Alpha AXP Program Through Customer Feedback

Don Alusic

Customer feedback is one of the most critical elements of the Alpha AXP Program. At an Alpha AXP End User Customer Advisory Board meeting held in late October, twelve senior information management customers previewed the November systems announcement and program status.

This group has been meeting over the last two years and has representation from Aetna, Allen-Bradley, Amoco, Bell Atlantic Tricon Leasing, Corning, DuPont, Fermi National Laboratory, GTECH, Merck, Pittsburgh Supercomputer, Rockwell International, and University of Texas. The following comments were made by members of the Customer Advisory Board about the Alpha AXP Program and board:

"Very worthwhile! It seems that our inputs were reflected in the program."

"Excellent discussions! Thanks for encouraging them. You demonstrated significant progress; pretty much on schedule. A remarkable achievement."

"Well organized. Followed an effective plan throughout the two years the meetings spanned."

"The entire team was always very effective in presenting the best of Digital."

"It is great to see the impact of our discussions on Digital's products and business practices."

"Very impressed with the listening and actions from the meetings."

"The program group deserves a lot of credit for developing and executing a successful customer feedback loop."

"The first [session] was good, but each succeeding session has been better."

One of the customers participated in the Alpha AXP announcement video. He felt that Digital has been listening and really understands the open business and will be able to compete. These customers are very supportive of the Alpha AXP Program and are convinced that it will have a significant place in the information technology industry. They are part of the continuing effort by the Alpha AXP Program to listen to the "Voice of the Customer."

During the past two years the Alpha AXP Program, with the support of AVS Customer Programs group, has been hosting a series of four, one and one-half day interactive meetings with a group of high-level customers from a diverse selection of industries. This group of

Back row, l-r: Larry Jones (Aetna), Margaret Knox (University of Texas), Ray Maliszewski (DuPont), Linda Walsh (GTECH Corp.), Duane Davis (Corning, Inc.), George Faini (Merck & Co.), Michael Levine (Pittsburgh Supercomputer Center).
Front row, l-r: Joe Gentile (Amoco), Joe Nemecek (Allen-Bradley), Larry Akin (Rockwell International), Jack Pfister (Fermi National Accelerator Lab), Leo Eineker (Bell Atlantic Tricon Leasing).

customers has been ably supported by their account managers.

The meetings reviewed the Alpha AXP Program plans for the system platforms, OpenVMS, OSF/1, and Windows NT, as well as our storage and balanced systems plans. The last two meeting also previewed announcement messages and product positioning prior to the February technology announcement and the November systems announcement. This preview included extensive discussions of application plans, Alpha AXP-ready programs, and software business practices.

Virtually every customer indicated that they would attend similar meetings in the future. They were enthusiastic about the potential for Digital with the Alpha AXP Program, and their ability to help Digital achieve this potential with continued customer input and honing of our direction and plans.

System Performance/ Availability Monitoring

Paul Toomey and Brendan Murphy
DCSS Manufacturing

Abstract

The reliability of hardware and software, as measured in laboratory environments, can differ substantially what is to be seen by the end customer. A number of factors that affect customer's systems are difficult to recreate in a lab environment (for example, system management procedures, third-party applications, configuration problems, and problems with release processes). These factors have a significant impact on overall system availability.

The Digital Product Performance (DPP) program captures the behavior of Digital's systems at customer sites. This data is interpreted to provide root cause analysis of the major factors affecting customer perceived performance of Digital systems.

Historical Perspective

The DPP program has evolved from a number of previous programs; one originated from the Field, managed by Mike Robey, and one from the Galway Manufacturing site. The program originating from Galway provides the framework of the DPP program and was originally used to monitor VAX 8000 and early VAX 6000 systems. It was extended to include VAX 9000, VAX 6000, and VAX 4000 families, and a number of Alpha AXP based products.

The behavior of several hundred systems is captured and electronically transferred to Galway on a weekly basis providing millions of hours of real system availability information. The majority of the monitored systems reside in Europe with a small but growing number in the US. The monitored sample includes both internal Digital systems and external customers.

The Monitoring/Reporting Process

A software tool, Monitoring Performance History (MPH), has been developed to capture system availability information (see Figure 1). After installation on the customer site, MPH requires no user intervention. A lot of effort is spent to ensure that the MPH software has minimal impact on the customer, both in terms of workload and disk requirements. Data is stored in a temporary work area in preparation for transportation back to Galway.

The transport mechanism used is dependent upon the customer. For internal Digital systems DECnet is used. For external customers, the DPP program uses the AES/DSNLink transport mechanism. AES/DSNLink provides automatic,

Systems Performance/ Availability Monitoring

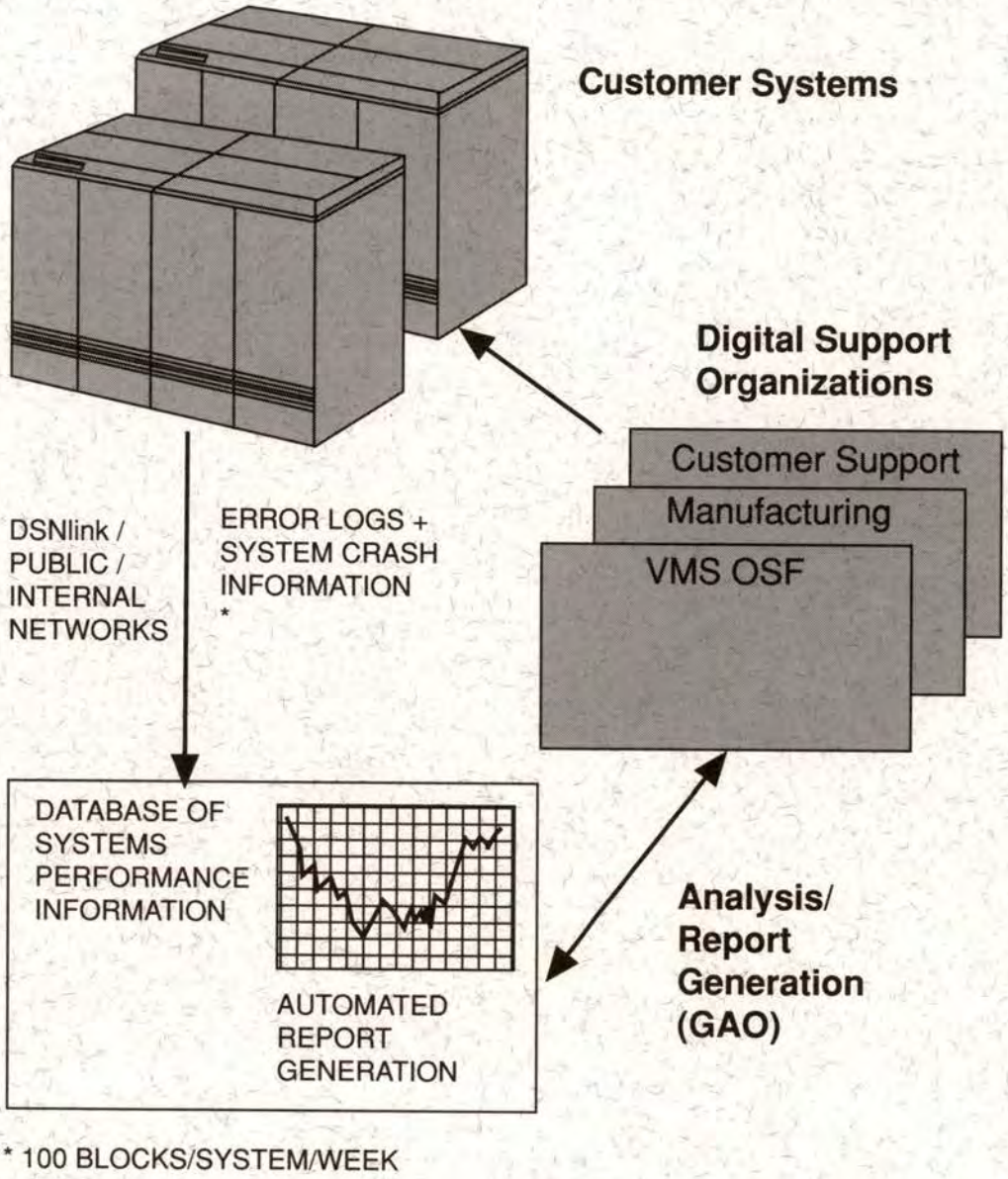


Figure 1.

secure links between the customer and the local Customer Service Center (CSC). Software residing on European CSC sites automatically routes the availability data back to Galway.

The availability data is loaded into an Rdb database, with a summary of the data being sent to the relevant product support groups. Database structures and filtering algorithms have been developed by the GAO team and Ted Gent in BXB. The relevant product support groups investigate certain behaviors to provide root cause analysis of product behavior. Information that assists this task is provided by CLUE (Crash Log Utility Extractor), which is included in the MPH kit. CLUE, developed in Galway, captures a footprint of the dump file, which is also transported back to Galway.

Software has been developed to generate reports from the DPP database. Reports can be generated for individual systems, groups of systems, families of systems, and for different versions of the operating system.

Once a month, the data is collated

and an executive report is produced. If product problems are identified during this process they are fed directly to the relevant support or field groups. Occasionally, problems are identified that require further investigation. This is performed either using the data currently in the database or by developing software to capture extra information on the customer systems.

The DPP program does not restrict its investigations to hardware and software reliability problems. The program has and will investigate nonproduct related areas, which have been identified as having a significant impact on the customer (for example, the software release process, clusters, system management problems, etc.).

With the development of OpenVMS and the general customer trend towards heterogeneous environments, it will not be possible to recreate all possible configurations within a test environment. DPP provides access to the behavior of Digital's products in a far greater combination of configurations than could ever be created in a lab environment.

The DPP executive report provides an overview of current product behavior as perceived by the customer, and the availability trends over the last nine months. This report has a wide distribution within Digital.

Recent Successes

Regular Reporting

The program has reported Mean Time Between Crash rates and several other key system performance/availability metrics for almost a year. Graphs are generated that indicate clear trends in system availability over time for VAX 9000, VAX 8000, and VAX 6000 families.

All reports generated are for Digital internal use only. A restricted notes file has also been established. Distribution of reports is managed from GAO. Contact CLADA::BMURPHY or LANDO::TOOMEY if you need more information on reports.

Alpha AXP Products Availability Reporting

The program has placed a clear emphasis on monitoring and reporting the availability of Alpha AXP based products as quickly as possible. Currently 10000, 7000, and 4000 series products are being monitored and reported on. The reports highlight both operating system problems and hardware related problems. The information is supplied weekly to both OpenVMS AXP and Hardware Engineering teams to help ensure that both the operating system and hardware reach a mature/stable state as quickly as possible.

Performance Goals for Prereleased Products

By capturing and interpreting current products, it is possible to work with the relevant Engineering group to:

- Set achievable goals for the behavior of the product on the customer site.
- Identify the relevant field test goals.
- Provide a mechanism to monitor field test systems.

The Future

OSF System Monitoring

Over the next few months the program will begin monitoring and reporting on systems running the OSF operating system.

Expanding the Number of Monitored Systems

As the program gains support the number of systems monitored in the US and GIA areas will increase. A special emphasis will be placed on key accounts.

Developing the Communications/Collection Process

As DSNLink, the customer to Digital communications process, becomes more widely used it will be easier to access customer machines. Ultimately, the communication process will allow us to receive availability information from customer machines via public data networks, as well as via modem.

Network Monitoring

A program has been initiated to investigate the behavior of network products. As this behavior is understood, the program will be expanded to monitor full networks.

Overall Goal

The overall goal of the systems performance/availability monitoring work is to provide Digital with real-time information. This information will be used to improve the overall performance/availability of our systems and networks. It effectively provides information for action to the relevant development and support organizations and works with them to drive improvement. This work will increase customer satisfaction and reduce support costs.

The GAO team, with partner organizations in the US, plans to develop and mature the systems performance/availability monitoring process. They will also continue to work with software and hardware developers and maintainers to drive improvements in product performance and availability.

Special Acknowledgment

Throughout the development of this program Ted Gent has acted as a technical consultant to the team, providing general guidance and technical support. Without his enthusiastic support the program could not have achieved its current level of success.

Digital Wins Enterprise Technology Award

Dick Willett

Digital won the Network World Enterprise Technology Award for FDDI network adapters at Interop in San Franciso, October 26 to 30, 1992. The DEMFA adapter significantly contributed to the achievement of this industry recognition. This is an important milestone as it symbolizes the goodness of our adapters in an enterprise network environment. Congratulations to the DEMFA team who made this possible and to DEMFA management who stood by the team members through the different development stages.

The DEC FDDIcontroller 400 is a high-performance network adapter. It provides FDDI connectivity to Alpha AXP and VAX systems through XMI. There are two unique features that distinguish this adapter from other adapters.

1) The DEC FDDIcontroller 400 (also referred to as DEMFA - Digital Equipment XMI to FDDI Adapter) can sustain a continuous transfer rate of 100 Mbps for all frame sizes larger than 69 bytes[1]. 100 Mbps is the maximum bandwidth achievable through FDDI.

2) The DEMFA adapter has the capability to filter Logical Link Control (LLC) headers in the adapter. This hardware assists off-load processing from the device driver and therefore increases the application performance.

The FDDI packet header is about a third of the Ethernet header (20 bytes). The FDDI PHY protocol can support bandwidths up to 100 Mbps. Technology trends showed that network bandwidth would increase further to Gbps. So it became necessary to define an adapter architecture that could sustain such high bandwidths[2]. The initial challenge was to implement an adapter for FDDI that has 30 times the packet throughput (about 446000 packets/second) of Ethernet.

Different alternatives were examined before a new architecture was defined for the DEMFA. Since none of the existent adapter architectures satisfied these performance goals, there was a need to define a new architecture. Some of the main ideas behind the new architecture are processing user datagram packets using ASICs and a hardwired pipelined processing approach without any microprocessor intervention to receive and transmit packets.

With the development of the DEMFA, Digital developed a key technology, which is currently used by different FDDI adapters being designed at DEC. As networks evolve to offer higher bandwidths, and as networks become the main data highways for user applications, there will be critical need for this technology, as in distributed computing environments.

Back row, l-r: Andy Russo, Dave Gagne, and Fred Doll.
Third row, l-r: Dave Stockdale, John Bridge, Ed Wu, Satish Rege, Dave Pickett.
Second row, l-r: Dominic Gasbarro, Bob Hommel, Lea Walton, Ron Edgar, and Ken Wong.
Front row, l-r: Ram Kalkunte, Mike Nohelty, Sas Durvasula, George Nielson, and Gerard Koekhoven.

Many of the ideas from the design of the DEMFA are being patented. There are a total of 10 pending patents, indicating originality shared by very few products. It also generated a set of trade secrets for Digital.

Two DEMFA designers, Satish Rege and Ram Kalkunte, are authors of a chapter on FDDI adapter design in a recently published book from John Wiley [3]. This is one of the first books on FDDI that discusses the design of FDDI products from a practical perspective.

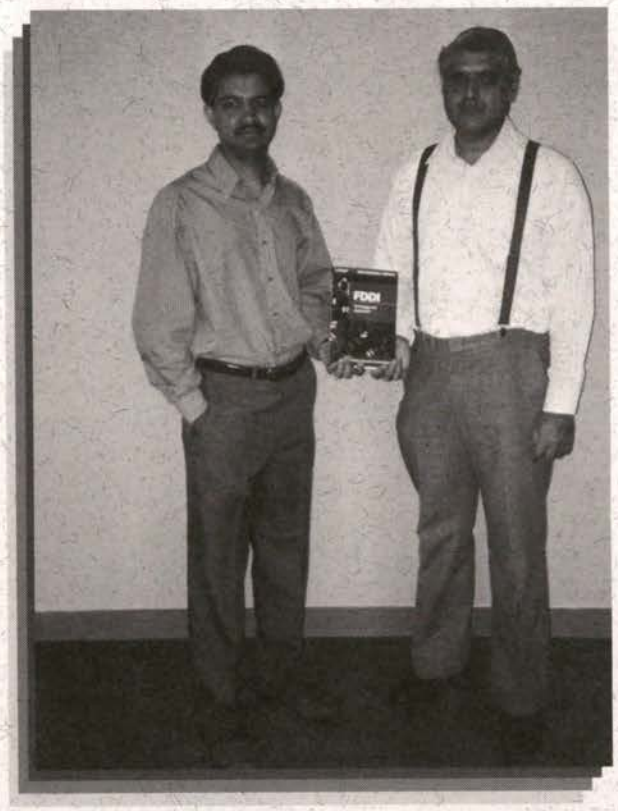
Interop's 1992 Network World Enterprise Technology Award Winner—the board, the book, and the award.

References

[1] R.S. Kalkunte, "Performance Analysis of a High Speed FDDI Adapter," *Digital Technical Journal*, Vol. 3, No. 3 (Summer 1991).

[2] S.L. Rege, "The Architecture and Implementation of a High Performance FDDI Adapter," *Digital Technical Journal*, Vol. 3, No. 3 (Summer 1991).

[3] *FDDI: Technology and applications*, edited by S. Mirchandani and R. Khanna, John Wiley and Sons, Inc, New York.



Ram Kalkunte, Principal Engineer, and Satish Rege, PhD, Consulting Engineer. Authors of "Chaplin," based on DEC FDDI controller 400 entitled "FDDI Adapter Design in the FDDI Technology and Application," published by John Wiley in November, 1992.

AVS Continues Its "Outward Focus" Series

Joe Senz

What We Plan

Outward Focus is a series of half-day programs which will be presented by an external analyst in seven segmented areas. Each session will feature an interactive presentation by the analyst covering the industry trends, customer buying patterns, emerging technologies, business pressures on organizations, and the goals of today's user. Each presentation will contain slides, literature, and statistics relevant to the topic.

Purpose

The name of the program "Outward Focus" describes its intent. Digital is changing and this change calls for a closer alignment of product design teams with Marketing, the Field, Manufacturing, and an increase in understanding of the customer's computing environment and needs.

Many of us have not experienced customer contact or developed knowledge of how customers use computer systems/products.

We want to raise the awareness level of our employees so that we can help move them from a point of little/no marketing or customer exposure to a point where they know how and why customers select and use certain products and systems in their organizations.

Learnings

Changes will result from this awareness. As the employee gains new perspectives of customer and industry needs:

- They will be able to build and strengthen communication within Marketing, Engineering, Manufacturing, and the Field.
- They will be able to look at centralization and integration and learn the need to value the database and the machine. They will also value the importance of customer needs.

Understanding Technical Customers and Their Computing Needs

International Data Corporation

Presenter: Vicki J. Brown
Date: February 4, 1993
Topics Covered:

- The spectrum of technical computing products. Where do each of these products fit within the industry?
  - DOS and Mac-based personal computers
  - UNIX workstations (for example, Sun)
  - Minisupercomputers (for example, Convex)
  - High-performance minis
  - Massively parallel systems (for example, Intel)
  - High-performance mainframes (for example, vector S/390s)
  - Supercomputers (for example, Cray)

Segment	Date	Group	Presenter
Technical Computing	2/4/93	I.D.C.	Vicki Brown
Enterprise Networking	4/15/93	B.R.G.	Kevin O'Neill
Database and Transaction	6/17/93	Aberdeen	Peter Kastner Processing
Consulting/Solutions	8/19/93	G2	Mark Hodges

To Enroll: Set host to MSBCS USERNAME:courses (no password is required)
You must enroll in each individual session you wish to attend.
Location: Boxboro Host Hotel (Just off Rt.495. Exit 28, Rt. 111)
Tuition: $170 for each session

- The broad array of technical computing applications and user needs.
  - IDC Workstation Audit results of application usage
  - Details from IDC high-performance applications research
  - Data showing revenues generated by each of 15 application types
- How do customers make price, performance, and other trade-offs to select the most optimal computer hardware and software solution for their application?
- IDC marketplace overview for each major product area.
  - Market dynamics
  - User issues
  - Key technology trends
  - Factors driving industry growth
- The importance of software versus hardware platforms.
  - Where/when is the software application most critical?
  - How often do customers write their won software?
  - Will third-party applications drive sales of hardware? If yes, for which applications/platforms? Why?
- Users' selection criteria for future purchases.
  - Workstations
  - High-performance systems

Enterprise Networking

Business Research Group

Presenter: Kevin D. O'Neill
Date: April 15, 1993
Topics Covered:

- What does today's multivendor network look like?
- How has it evolved and where is it going?
- Who makes the purchase decision and what are the key criteria?
- What is the organizational impact?
- What are the most important applications on the network?
- What are the most important benefits customers are seeking and why?
- What are the biggest obstacles users are encountering?
- What is the "real" impact of standards and the network?
- What drives buying behavior and how do customers perceive different vendors, such as, Sun, HP, IBM, and NCR?
  - What do customers expect from their network vendor in terms of services?

Database and Transaction PROCESSING

Aberdeen Group

Presenter: Peter S. Kastner
Date: June 17, 1993
Topics Covered:

- How transaction processing provides a competitive advantage to users.
- Transaction processing solutions at the mainframe, midrange, and microcomputer levels.
- The role of databases and the features necessary for a robust transaction processing database system.
- Fault tolerance, roll back, and recovery.
- Benchmarks and their meaning.
- Standards issues.
- The buying criteria of users.
- Market size and growth potential.
- Competitive offerings and strategies of major suppliers.

Consulting Solutions

G2

Presenter: Mark Hodges
Date: August 19, 1993
Topics Covered:

TBD

Jim Cassell of Gartner Group presents "Glass House Computing" to the DCSS Engineering Organization. This seminar was the first in a seven part series of "Outward Focus" programs.

DEC 4000 AXP Information: Continuous Improvement and Innovation

Judy Hall, Kathe Rhoades, Joyce Snow, Betsy Comstock, and Mary Ellen Connell

The DEC 4000 AXP server is part of Digital's new family of flagship computers based on the groundbreaking Alpha AXP architecture. Alpha AXP architecture is a 64-bit RISC architecture that provides exceptionally fast compute power. Other systems in the Alpha AXP hardware family are the DEC 3000 workstations and the DEC 7000 data center system.

The development of the DEC 4000 server gave impetus to a new approach to creating information to support the hardware. This new vision was conceived in 1989 by Len Kreidermacher and Judy Hall of ESB, and Debbie Murphy of IDC (Information Design and Consulting). They prepared a comparative analysis of hardware information from Digital's competitors and worked with Field Service, Engineering, and documentation designers to develop a strategy/vision statement.

Released in 1990, the strategy had the following goals: to develop a new approach to creating hardware information for the Alpha AXP family of computers, to utilize new technology, and to improve overall customer satisfaction.

In 1991, ESB partnered with IDC to assemble an integrated information team, headed by Judith Scott of IDC. This team represented several different organizations within Digital. Writers, editors, illustrators, course developers, information designers, and human factors specialists joined together to create best-in-class system information.

A New Paradigm

The new information paradigm called for rethinking the way information products are typically developed. In the past, information for customers and Field Service tended to be fragmented. Hardware, Software, Marketing, Field Service, and Educational Services created their own information, independent of other groups. As a result, customers received documentation that was sometimes redundant, contradictory, confusing, or difficult to access.

The DEC 4000 Information Team refocused on the customer. Its goals were:

- Make sure that Digital internal divisions are invisible to the user and do not affect ease of access to information.
- Treat the DEC 4000 as a system and document it as an integrated whole, from hardware to software.
- Integrate representatives from Human Factors, Corporate Design, Manufacturing, Engineering, Service, Marketing, and other groups onto the team.
- Use surveys, field visits, benchmarking, and user views to find out what customers want.

- Provide multiple ways for customers to access information.
- Provide customers and Field Service with a cross-information-set map to help them locate and order information products.
- Measure for continuous improvement during development and beyond.

Installation Design: A Success Story

One of the more far-reaching achievements of the DEC 4000 Information Team is the creation of a new operating model for installation design and information.

"Day 1" testing of previous systems, in which volunteers simulate a customer's experience of hardware installation, revealed numerous problems for installers. Most problems resulted from a lack of communication between various Digital organizations. Each group was providing an isolated piece of a patchwork. As a result, installers experienced:

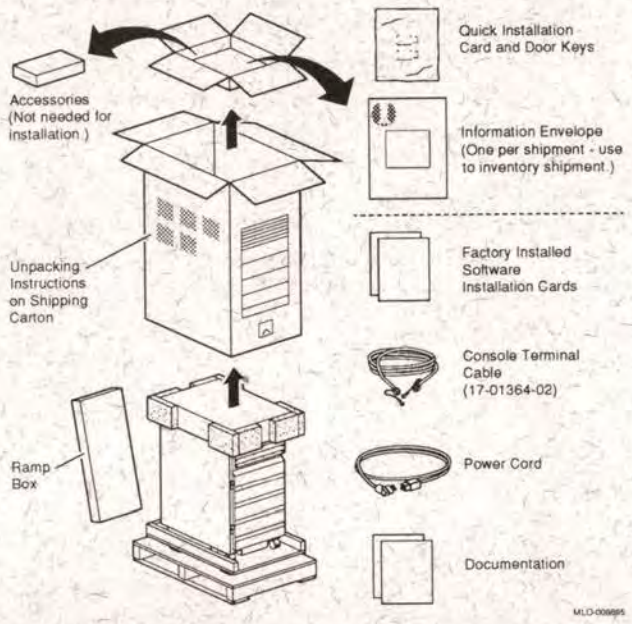
- Lots of loose pieces of information with nothing tying them together
- Difficulty finding the installation documentation
- Information spread over many documents, requiring installers to have several books open at once
- Too many words and not enough illustrations

To solve these problems, the DEC 4000 Information Team prototyped and created a "quick installation" card that would give installers all the system installation information they needed in one short, simple document. In addition, the team formed partnerships with Human Factors, Engineering, Factory Installed Software (FIS), Packaging, Industrial Design, and Manufacturing to design a new installation process. The partners cooperated by:

- Working with Engineering and Manufacturing to minimize the number of loose pieces in the shipment
- Creating a "day 1" and a "day 2" box as a way to help customers organize and simplify the complexity of a typical shipment
- Working with Engineering to design a simple, useful startup screen
- Working with the Factory Installed Software (FIS) team on FIS information (FIS lets installers bring up the operating system software much faster than installation from a distribution kit)
- Determining a process for handling embedded drives

The end result – a greatly simplified installation process and easy-to-use installation information. During DEC 4000 Human Factors Day 1 testing, participants installed the hardware in less than half an hour. In the past, this installation process often took much longer. The team expects the streamlined installation approach to increase customer satisfaction; contribute to Digital's profitability; and set the standard for Digital's hardware product installation design.

The installation team consisted of many representatives from several organizations: Judy Hall, Joyce Snow, Betsy Comstock, Nan Bulger, Debbie Falck, Bob McClain, Mike Collins, Dave Keir, and many others who worked on this innovative design.



Usability Testing

To ensure the usability of the DEC 4000 AXP system and its documentation, the DEC 4000 Information Team adopted a strategy of early and frequent testing. This strategy was unusual because in the past the limited availability of hardware meant that testing could occur only once.

In January and February 1992, a Group 0 prototype DEC 4000 AXP system was made available every Friday. During six sessions, system managers and users unfamiliar with the system tried out various operator and service tasks. This early testing resulted in improvements to

the hardware design and also allowed the information team to see how users approached tasks on the system. The Group 0 testing was made possible by Gerry Ganong, Mike Chautin, Jose Flores, and their group, who shared DEC 4000 systems, lab space, and technical support. It was coordinated by Betsy Comstock of Human Factors.

Usability testing continued in July with seven all-day sessions. Compared to past usability testing on this class of product, this testing differed in the following ways:

- The installation team that planned and conducted the testing consisted of people representing many disciplines, including manufacturing, design assurance, packaging, engineering, CSSE, operations, documentation, and human factors.
- Members of the information team (writers, an editor, and illustrators) performed and observed a dry-run test and made significant detailed improvements to the "Day 1" documentation prior to the first "real" test session with people who were seeing the system for the first time.
- Service procedures were tested in addition to the usual "Day 1" procedures.
- A larger than usual number of people observed one or more sessions. From six to ten observers attended each session, for a total of at least 35 observers.
- Observers participated actively in the sessions. At logical break points, participants pulled up their chairs with the observers and gave their impressions of the system and things they would like to see changed. Observers took action items and in some cases made improvements before the next day's session began.

During "Day 1" task sessions, participants unpacked, installed, and brought up the software as if the system had just been shipped to them. These tasks were performed easily by both "end-user" participants — people acting as customers who would install their own systems — and "service" participants — Digital Field Service engineers. Even though they were not trying for speed, it only took these first-time installers an average of 53 minutes from the time they opened the first box to the time they reached the DCL ($) prompt.

Figure 1 gives the mean time in minutes for the three end-user sessions and the two service sessions for three main parts of the installation.

The core team involved in continuous improvement testing included Betsy Comstock, Mary Ellen Connell, Susan Marsh, Joyce Snow, Richard Clayton, Mike Chautin, and Jose Flores.

Key to Improved Illustrations

The DEC 4000 Information Team also applied its new operating paradigm to the creation of document illustrations. In the past, as with the installation process, artists responsible for providing illustrations in the documentation often felt they were working in isolation.

The DEC 4000 illustrators broke this cycle by partnering with the Illustrated Parts Breakdown (IPB) group. By drawing on the IPB's Unigraphics experience and close relationship with hardware designers, the illustrators were able to efficiently capture online engineering drawings for final illustrations. The close working relationship between these groups has eliminated redundant illustrations and created a standard base of drawings that is highly accurate as well as reusable.

The illustration team consisted of the following people: Dave Hamel, Linda Uglevich, Steve Cordeiro, Bob Astapoveh, Carol Senecal, Diana Ledoux, Gerri Ledoux, Anne Nault, and Ron Walsh.

Document Design: Innovation in Presentation

The DEC 4000 Information Team also took an innovative approach to

Mean Number of Minutes to Perform "Day 1" Tasks

From	To	Three End-User Sessions	Two-Service Sessions	All Sessions
1 Start to unpack	Turn power on	27	20	24
2 Turn power on	Boot FIS	7	11	8
3 Boot FIS	$ prompt	20	22	21
1->>>3 Start to unpack	$ prompt	54	53	53

Figure 1

document design. Typically, Digital products have been "overdocumented," providing customers everything they need to know, plus more, confusing them in the process. Based on competitive analysis and customer surveys, the team decided that hardware information needed to be streamlined.

One solution was to create quick reference cards for specific key tasks, such as hardware installation and site preparation. The documents were graphics-intensive, so users could quickly identify components and perform tasks. This information simplified the site preparation and installation process and greatly reduced page count. A quick reference information map was also created to help customers and Service understand the design of the information set, introduce them to marketing literature and courses related to DEC 4000, and provide telephone and fax numbers for ordering information.

For longer documents, such as the *Owner's Guide for System Managers*, the writers applied Information Mapping principles. Information Mapping is a technique that "chunks" information into modular units that are simple to understand and easy to reuse.

Members of the DEC 4000 Information Team and the DEC 3000 Workstation Information Team drove the creation of an IDC information mapping doctype. This design is based on a similar design used for course development. The new design helped writers apply a "value filter" to information, always asking the question, "Does this information help the user perform key tasks?" With both the DEC 3000 and DEC 4000 teams using the same approach, the documentation for both platforms achieved a consistent look and feel.

Another innovative area was cover design. Here the goal was to give Alpha AXP hardware documentation covers a unique look that customers could quickly associate with Digital's Alpha AXP program.

Team members met with Debbie Falck of Corporate Design, as well as members of the DEC 3000 and DEC 7000 groups, to devise a strategy that would work for each group and still identify any Alpha AXP system. The final design includes several constant elements—a diamond-shaped Alpha AXP logo and a background "image" that can be produced in full color or one color. In addition, each platform is distinguished by a simple line drawing of the system superimposed on the graphic. The design is printed on a white background, which contributes to its crisp, clean look.

The new design received the green light from the Alpha AXP Program Office as well as from the Review Board for DEC STD 073 (Manufacturing and Packaging for Publications), the committee responsible for ensuring consistency in product packaging. Equally gratifying, the Alpha AXP Program Office requested that other groups creating Alpha AXP specific documents begin adopting elements of the design to ensure a consistent strategy across the entire Alpha AXP program.

The document and cover design teams included the following people: Laura Baumann, Debbie Falck, Kathe Rhoades, Jackie Unch, Kanti Timberlake, Keith Carter, Bruce Stone, Steve Cordeiro, and Mike Fein.

Correct SPICE Results

Cheryl Preston
Senior Hardware Engineer

In the Q1 FY93 *Forefront* issue, an article titled "Continuous Improvement in ESB's Module-Level Signal Integrity Process" was printed. An error was made in the reproduction of one of the figures that contradicted the message of the article. The following figures contain the corrected representations.

The purpose of the article was to show how ESB has improved its module-level signal integrity process by designing for signal integrity with the use of SPICE (Simulation Program with Integrated Circuit Emphasis). By taking this approach ESB Design Assurance has changed from passive empirical testing to active simulation, and to solving signal integrity issues prior to the layout of the module. These changes reduced the number of empirical problems found., therefore reducing the number of etch revisions necessary, cost associated with each revision, and time associated with each revision. Using the SPICE results as a guideline to understand the potential network problems is effective since the SPICE results track the empirical data.

In the following figures, Figure 1 contains the SPICE results and Figure 2 contains the empirical data. Using SPICE to evaluate this network allowed the team to choose the least expensive module layup, etch routing, and termination with confidence.

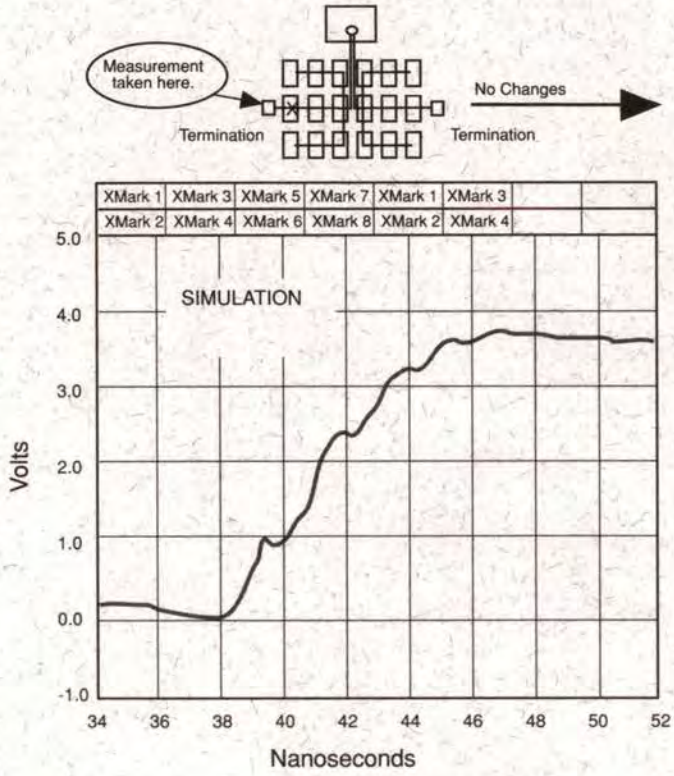


Figure 1

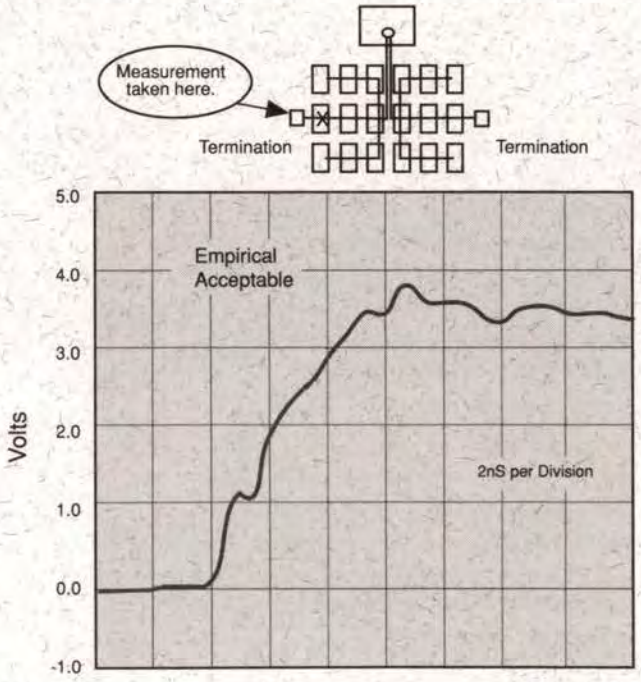


Figure 2

Alpha and VAX Systems Marketing Organization

Ken Swanton

The AVS Marketing organization has realigned its strategies. The new focus is to build on recent success at reversing the AVS revenue decline, introduce Alpha AXP systems, improve channels and partnering, and market at a higher level of integration with lower costs. The following groups now comprise AVS:

OpenVMS Servers Marketing – Mike Cuccia
Continue proven FY92 program, including: Worldwide OpenVMS Champions, four-part message (open, price/performance, functionality, Alpha ready), OpenVMS on VAX and Alpha AXP systems, sales tools, air cover, corporate reviews, etc. Mike has a ten-year sales and product marketing background, most recently as the OpenVMS Server Program coleader.

Alpha AXP Servers Marketing – Al McGuire
Introduce Alpha AXP servers into targeted opportunities, including targeting across AVS's Alpha AXP servers, in close cooperation with Alpha AXP marketing managers in each country/industry. Al has 15 years of product marketing and Corporate PR background. He was most recently in the Alpha AXP Business office.

Indirect Channels Marketing – Duncan Anderson
Lead a renewed focus on indirect channels business, including new channels development and channels support. Duncan will be measured on the combined VAX and Alpha AXP Channels sales budget and future growth attained by the new Alpha AXP Channels Sales model. Duncan has 14 years of volume sales, product marketing, and manufacturing experience, most recently as marketing manager for the Entry Systems Business.

. . . AVS Marketing focus is to build on recent success at reversing the AVS revenue decline, introduce Alpha AXP Systems, improve channels and partnering, and market at a higher level of integration with lower costs.

Systems Partners and Integrators Marketing – Ed Barker
Accelerate recent growth of system integration (Digital and non-Digital business), and market and grow the product and capabilities of our Partners Program, such as Alpha AXP partnering with Cray Research. Ed has been with Digital for 12 years and has managed groups in Manufacturing, Engineering, and Marketing, most recently as the High End System Marketing manager.

Server Base Product Marketing – Steve Blanchette
Accelerate efforts to improve the integrated packaging, pricing, positioning, and base product sales tools and support across all VAX and Alpha AXP servers (includes further easy to sell enhancements to ADVANTAGE-SERVERS). Manage the new AVS Product Introduction Committee (PIC). Steve has 9 years of product marketing and management experience, most recently as Mid-Range System Base Product Marketing manager.

OpenVMS Base Product Marketing – Phil Auberg
Continue successful openness of OpenVMS effort, but primary focus is on marketing the high functionality of OpenVMS (especially clusters). Also managed the OpenVMS Partners program. Phil has 11 years of software and hardware engineering and product marketing experience, most recently as VMS Software Marketing manager.

Integrated Servers Marketing – Steve Koenig
Make a large, successful business out of AVS's first highly integrated systems engineered server solution ACCESSWORKS and continue driving AVS towards success in a PC-centered world. Steve has over 20 years of experience in sales, engineering, business management, contracts, and product marketing.

Communications and Marketing Services – Wally Cole
Provide communications (PR, consultant relations, literature, sales communications, advertising) functions, sales training, customer event and trade show coordination, IBU program coordination, communication systems, and budget management. Wally has 12 years of product marketing and hardware and software product management experience.

A critical piece of this organization is that many managers also report to one of Bill Demmer's staff members to ensure close coupling.

AVS Forms Open Systems Marketing Office

Rae LaFlamme
AVS Software Marketing

Rich Kittle leads the AVS Open Systems Marketing Office as part of AVS Software Marketing.

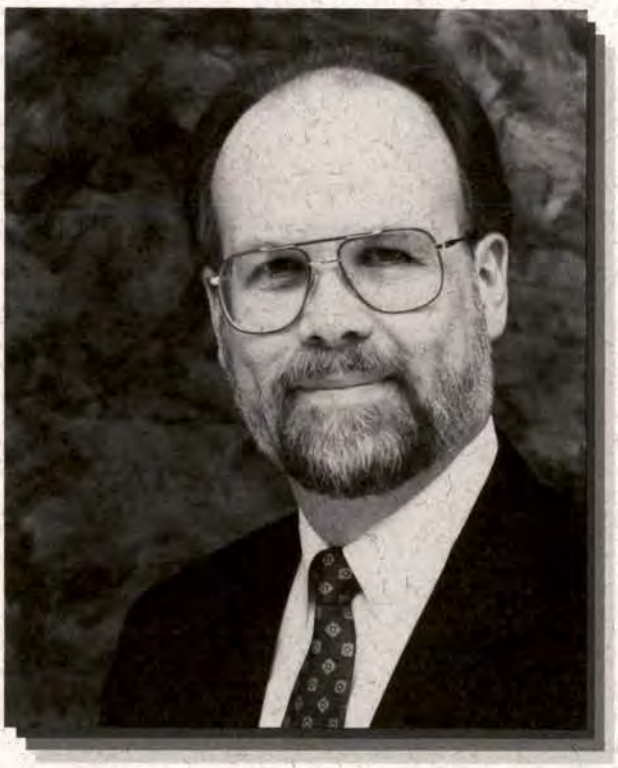
In support of AVS, the OpenVMS Software Marketing Group (formerly VMS Marketing) has made great progress in moving OpenVMS into the Open Systems market over the past several years. The addition of POSIX and XPG3 conformance to our OpenVMS software, and our public commitment to increase the use of Open Standards, has led to significantly increased business potential around the world. The move to an open, multivendor computing environment has even led to the name change of the VMS operating system to OpenVMS.

According to Bill Demmer, AVS Vice President, "It is critical to the future of OpenVMS Systems that we enhance our product and marketing activities in the Open Systems space. Our current and prospective customers expect this; and there are many segments of the market who still have not heard our message."

To increase efforts to reinforce the OpenVMS Open Systems message both internally and to customers, AVS (Alpha AXP and VAX Systems) has created the Open Systems Marketing Office (OSMO), managed by Rich Kittle. As an integral part of the OpenVMS movement since its earliest days, Rich developed the "Open" message, built the strategy to get it to the market, and has been instrumental in gaining acceptance for OpenVMS across the Corporation and in the marketplace. Rich is managing this office from within the AVS Software Marketing group reporting to Phil Auberg, Manager of AVS Software Marketing.

Says Phil, "Rich Kittle is well qualified to handle this tremendous under-taking. His work over the last few years has helped to change market perceptions that Open is not limited to UNIX; it equals conformance to industry standards. This has led many customers to view the once considered proprietary OpenVMS as an operating system that conforms to more industry standards than some UNIX derivations on the market today."

The OSMO is responsible for positioning all AVS products for success in the Open Systems market, for advancing Open Systems issues for AVS across the industry, and for driving Open Systems market requirements into AVS product development. Rich and the other members of the OSMO team are creating the Open Systems messages that AVS will use to support our products and are working across AVS Marketing to drive the Open Systems Marketing strategy.



Rich Kittle
AVS Open Systems Marketing Office

"OSMO allows us to continue our aggressive efforts to keep the industry analyst and press communities abreast of OpenVMS's advances in Open Systems," says Rich. "Additionally, it allows us to communicate to several levels inside of Digital."

In addition to his role as the manager of OSMO, Rich has taken on a wider corporate role in the Open Systems effort. He has joined the Corporate Open Systems Marketing Team, managed by Jean-Claude Monney, as the AVS representative. Rich also supports Richard Straub as the Alternate at the X/Open Marketing Managers Committee. These functions are important recognition of the role that OpenVMS has obtained in the Open Systems market.

OSMO plans to work extensively in not only the US and GIA, but with the European market where X/Open has heavy influence and open systems, XPG branding in particular, are a requirement of most IT businesses. According to Jean-Claude Monney, "Rich and many others worked to prepare the European Analyst and Press communities, and Digital country management for the July 7, 1992 announcement which included delivery of XPG3 BASE Branding and the name change to OpenVMS. We are looking to enhance this type of effectiveness by bringing people from multiple product lines within Digital into the Corporate Open Systems Marketing team. We are very glad to have Rich as part of our organization."

As an example of a cross-group effort involving multiple product lines, Rich is currently working with Steve Gonzalez, a Digital UNIX partner, to develop a unified open systems message across product lines. The final outcome of their efforts will be a presentation within which each open systems product group can then position their products.

In the past, Rich has been instrumental in influencing VMS engineering direction in the open systems space. He has worked with a team of OpenVMS Product Management and Engineering on the product delivery of POSIX V1.0 in February 1992. OpenVMS also achieved XPG3 BASE Branding in June 1992, a certification by X/Open that an operating system is in fact open. Rich and his colleagues were instrumental in enabling these events.

Rich and the OSMO will continue to stay involved with engineering to influence further delivery of open systems capabilities on OpenVMS in the areas of OSF's DCE (DECthreads hooks are included in the OpenVMS V5.5 base operating system), continued POSIX conformance as approved POSIX standards emerge, and commitment to XPG4 Branding.

"I am extremely excited about this opportunity," says Rich. "The efforts put forth by the OpenVMS open standards community over the last few years have helped spread the word that OpenVMS is in fact as open as any UNIX system on the market today. But our efforts need to multiply in order for Digital to achieve it's goals." Rich expects that OSMO's effort and its continued involvement in the more global Open Systems effort will do much to increase AVS business in the future, and enable other product lines to succeed as well.

Patents

The following patents were recently issued to Digital Equipment and include one or more AVS inventors. Titles and names supplied to us by the US Patent and Trademark Office are reproduced exactly as they appear on the original published patent.

Front row, l-r: Jesse Lipcon, Bill Samaras, Andy Ingraham, and Larry Herman. Back row, l-r: V.P. Bill Demmer, Bill Grundmann, Doug Ryder, Doug Williams, Don Smelser, Ron Salett, Tryggve Fossum, and Doug Manley.

Patent Number	Inventors	Title
5,107,462	W.R. Grundmann, V.R. Hay, L.O. Herman, D.M. Litwinetz	Self-timed register file having bit storage cells with emitter-coupled output selectors for common bits sharing a common pull-up resistor and a common current sink.
5,109,495	D.B. Fite, T. Fossum, W.R. Grundmann, D.P. Manely, F.X. McKeen, J. E. Murray, R.M. Salett, E. Samberg, D.P. Stirling	Method and apparatus using a source operand list and a source operand pointer queue between the execution unit and the instruction decoding and operand processing units of a pipelined processor.
5,111,424	D.D. Donaldson, R.B. Gillett	Lookahead bus arbitration system with override of conditional access grants by bus cycle extensions for multicycle data transfer.
5,113,515	D.B. Fite, R.C. Hetherington, M.M. McKeon, D.P. Manley, J.E. Murray	Virtual instruction cache system using length responsive decoded instruction shifting and merging with prefetch buffer outputs to fill instruction buffer.
5,113,521	F.X. McKeen, T. Fossum, D.P. Bhandarkar, C.A. Weicek	Method and apparatus for handling faults of vector instructions causing memory management exceptions.
5,115,455	W.A. Samaras, D.T. Vaughan, A.D. Ingraham	Method and apparatus for stabilized data transmission.
5,125,083	D.B. Fite, T. Fossum, R.C. Hetherington, J.E. Murray, D.A. Webb	Method and apparatus for resolving a variable number of potential memory access conflicts in a pipelined computer system.

For comments or more information about patents please contact Tom Stylianos, Tom.Stylianos@BXB.MTS.DEC.COM or DTN 293-5836.

Promotions

Kathy Morse
Senior Consulting Engineer

Kathy Morse

Kathy Morse has been promoted to Senior Consulting Engineer. Kathy has been with Digital for 16 years in VMS development. She joined Digital in 1976 as the only new college hire to work on VMS V1.0. She was instrumental in the early work on VMS and has been a key contributor in a number of areas of OpenVMS/VAX development.

Kathy was one of the major designers for VMS Symmetric Multiprocessing for VMS V5.0. She was also the technical leader and supervisor of the Low-End CPU group for VMS Engineering. This team shipped MicroVMS support for the MicroVAX products within VMS.

Over the last several years Kathy has played a lead role in the development of Alpha AXP systems. She was a member of Bob Supnick's Alpha AXP Technical Task Force and also a member of the RISC VAX Task Force, whose work led to the OpenVMS AXP Program. Kathy was a contributing author to the OpenVMS AXP design spec, writing several chapters of the Working Design Document. She has represented OpenVMS AXP on multiple cross-group technical teams.

Kathy designed and led a team that implemented the development environment in which the OpenVMS AXP developers work and in which the Alpha AXP operating system is built. Her work on the system integration environment and processes that support it has been instrumental in helping OpenVMS AXP meet its aggressive schedule and keep the releases on time over the last 18 months.

Kathy has also been very active and has done an exceptional job working with customers and Digital groups through her OpenVMS AXP presentations at DECUS. She has served as the OpenVMS AXP interface for the roll-out of technical information to customers.

Sean Keenan
AVS Manufacturing Manager

Sean Keenan has been appointed to the position of AVS Manufacturing Manager, reporting to Bill Demmer and Dan Jennings. In this role, Sean will be responsible for continuing and enhancing the close relationship between Manufacturing and Engineering, leading to the development and delivery of world-class competitive VAX and Alpha AXP products.

Sean has been with Digital since 1975. He has spent most of this time in various management positions in the Galway plant including four years as AVS Manufacturing Business Manager. Sean's most recent assignment brought him to the US as the European representative to the AVS Business Operations staff.

Sean Keenan

Giovanni Giuliani
Consulting Engineer

Giovanni Giuliani is the first Consulting Engineer at Corporate Engineering in Italy. His promotion is in recognition of his significant contribution in delivering both VMS POSIX and more widely, the overall VMS strategy for open systems.

VMS POSIX has extended VMS OS by providing the open interfaces of IEEE POSIX 1003 and X/Open XPG3. This product represents one of the cornerstones of OpenVMS, which allow it to be X/Open branded.

Giovanni joined the Engineering Center at Varese, Italy in October 1988 when the site was opened. Since then he has worked on the VMS POSIX project. He assumed overall technical responsibility of the project, and directly lead the file system development. Presently, he is the VMS/Italy technical director.

In addition, Giovanni teaches a monographic set of lectures on "UNIX programming and internals" as part of the Operating System Course at the Engineering University in Milan, Italy.

Before joining Digital, he was the initiator and then the leader of the UNIX Kernel Development group in Olivetti. Giovanni graduated with honors in Electrical Engineering from Milan University in 1982.

Giovanni Giuliani

Beverly Schultz
OpenVMS Alpha AXP Group
Engineering Manager

Beverly Schultz

Beverly Schultz has accepted the position of OpenVMS Alpha AXP Group Engineering Manager reporting to Don Harbert.

Since 1990 Beverly has been the group manager of Office and Teamware Engineering working for Jeff Rudy. She has been responsible for ALL-IN-1 and ALL-IN-1 options in our time-shared environment; for TeamLinks for Windows and Mac clients with VMS and UNIX servers in the PC environment; for software that allows interoperability of these products; and for services that enhance all of our office offerings, specifically in the areas of routing and workflow, file cabinets, team administration, profiling, and management.

From 1981 to 1990 Beverly worked in Digital's Languages and Tools group managing the development of VAXset products DEC/CMS, DEC/Test Manager, VAX Language Sensitive Editor, VAX Source Code Analyzer, and Program Design System, as well as the VAX C and PL/I compilers, APL, and the VAX Debugger.

Prior to joining Digital, Beverly was involved in software development for process control and factory floor automation. She has a B.S. in Mathematics from Valparaiso University, Indiana and an M.S. in Computer Science from the University of Dayton.

Tom Benson
Consultant Software Engineer

Tom Benson

Tom Benson has been promoted to Consultant Software Engineer. The promotion is in recognition of Tom's outstanding contribution to the design and development of OpenVMS AXP Systems.

Tom was the project leader and primary designer for the OpenVMS AXP Macro Compiler. This compiler processes VAX Macro-32 source code in order to produce Alpha AXP VMS object modules. In a sense, it treats CISC assembly language as a high-level language source to generate RISC instructions. Tom provided a robust yet compatible design, which allowed easy porting of OpenVMS/VAX Macro code (approximately half of the operating system) to OpenVMS and System.

After the design and initial implementation of the compiler, Tom concentrated on making the compiler produce optimized Alpha AXP instruction sequences. Many of the same kinds of analysis typically used in high-level language compilers were applied here to VAX assembly language. He also recommended source code optimization techniques that have been frequently used to improve the compiled operating system code. Significant gains in the performance of OpenVMS AXP resulted from this work.

Tom received a B.S. in 1977 and an M.S. in 1978 in Computer Science from Syracuse University. He worked in Digital's VAX BASIC group until 1983. Tom was project leader for the VAX Code Generator in the Technical Languages and Environment group from 1983 to 1986. He then joined VMS Engineering, where, prior to joining the Alpha AXP effort, he contributed to many components of DECwindows. Tom served as project leader for FileView, the Session Manager, and the XLIB portions of the V1.0 DECwindows release.

Tom has applied for four patents related to his work on the OpenVMS AXP Macro Compiler, and has made numerous DECUS presentations.

Bob Supnick
Technical Director of Engineering

Bob Supnik has been appointed Technical Director of Engineering, reporting to Bill Strecker. In this role, Bob will drive the formulation and evolution of technology, product, and process strategies for Engineering. He will inspect engineering projects and programs on an ongoing basis, and foster communication, innovation, and cooperation in the technical community.

Bob joined Digital in 1977 to work in the Storage Advanced Development Group. He then moved to Semiconductor Engineering were he managed the J-11 and MicroVAX projects, the Advanced Development Group, and the Microprocessor Design Group. For the past four years, he has been the Technical Director for Alpha AXP, and Technical Director of Semiconductor Engineering and, then, the Alpha AXP and VAX Systems Group. Bob holds a M.A. degree in History from Brandeis and B.S. degrees in Math and History from M.I.T.

Bob Supnick

Awards

This program provides AVS Manufacturing Operations Management a means of awarding individuals and teams whose contributions far exceed expected performance. Particular emphasis is placed on recognizing individuals and teams for contributions that increase the effectiveness of the AVS business. The program also permits the recognition of individuals and teams external to the business, who have significantly contributed to its success.

Pictured l-r: Ronan Fox, Pat Moran, Felicity O'Shaughnessy, Brendan Murphy, Maggie Hayden, Denis O'Donnell, and Richard Collins.

GAO Systems Engineering Team

This award is for the outstanding technical contribution from the GAO Systems Engineering people participating in the DPP program. Their performance as a "virtual" team, through close collaboration and solid relationships with their counterparts in the US, resulted in producing a world-class Digital program.

The team has demonstrated creativity, initiative, and leadership in the development of the DPP program. The results of this program will be lower costs through early problem identification in new products, and reduced defects in steady state products.

GAO SE demonstrated a strong ability to work as a team during the initial data collection process. This required making personal contacts with managers in Digital Services in the UK and Europe to explain the benefits of performance monitoring. This was a key factor that has opened the door to European external customer systems monitoring.

A program of this nature is faced with many obstacles, for example, distance, time, and unfamiliar faces. The Galway SE group has demonstrated excellent team spirit and participation while working with both European and US counterparts.

Cobra Manufacturing Team and Optimization Model Development Team

First row, l-r: Greg Yannekis, Linda Trafton, Wanda Petkauskos, and Cheryl Nickolas. Second row, l-r: Dan Jennings, Bruce Arntzen, Allan Lyall, Alex Morton, Mary Doddy, and Jay Akers.

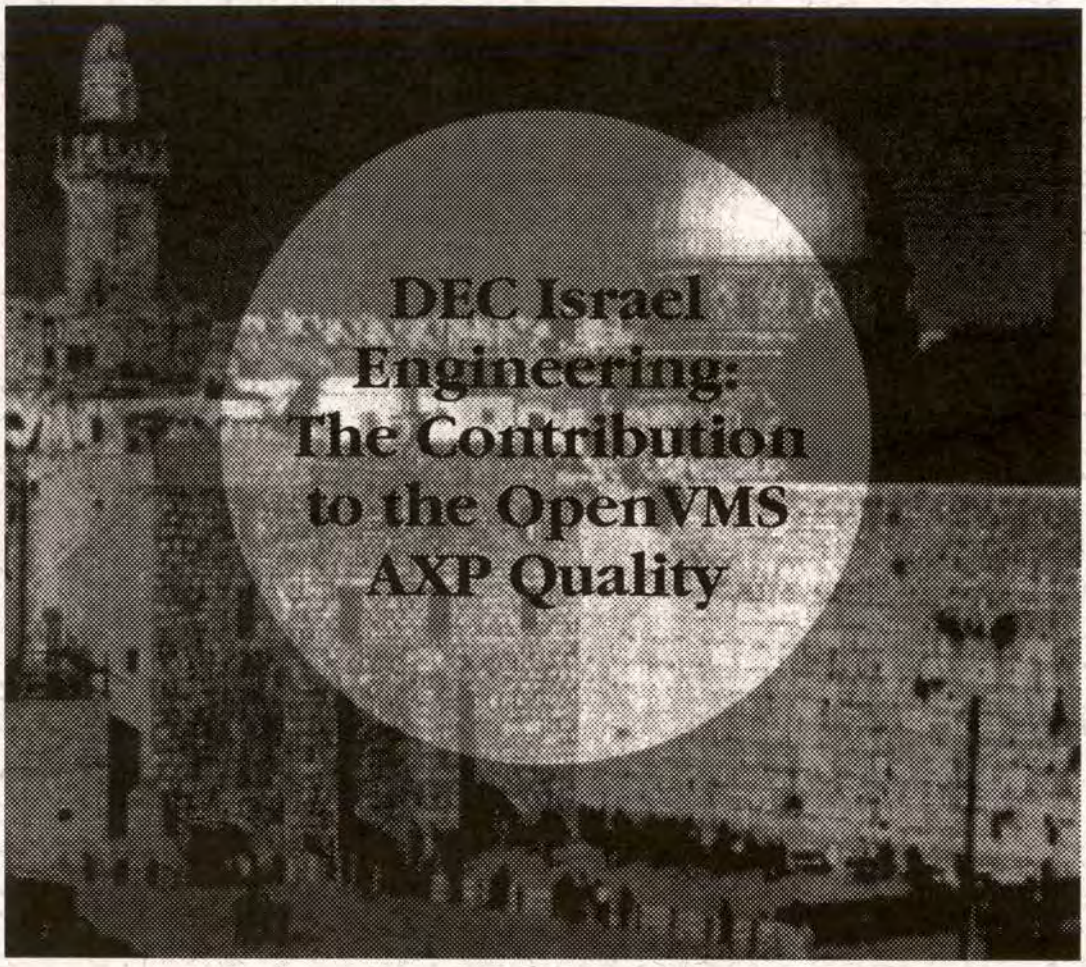
The Cobra Manufacturing Team and Optimization Model Development Team have been recognized for their leadership and commitment.

The Cobra Team developed a model for introducing new systems into manufacturing.

This model has improved integration with plants and design engineering, and reduced New Product introduction spending. The team's use of a protocol document provided a clear method for communicating expectations and responsibilities across the team.

The Optimization Model Development Team managed the development and implementation of a Network Optimization Modeling Tool. Over a three-year period they developed a technologically solid decision support tool that addresses a complex business problem. The tool provides Digital with a competitive advantage over other companies in the industry.

The enthusiasm, leadership, openness, and integrity of these teams has contributed significantly to the success of AVS.



DEC Israel Engineering: The Contribution to the OpenVMS AXP Quality

Nitzan Hefetz
Engineering Projects

Last summer, Don Harbert, vice president of the VMS group, visited Israel and had the opportunity to get a first hand impression of Digital Israel Engineering achievements.

"There is an excellent work force, with an entrepreneurial spirit," says Don Harbert. "Israel is a country with a highly sophisticated scientific community linked to industry, and a labor force that creates high value-added exports." The Digital Israel Engineering organization supplies quality engineering services and capabilities to Digital US and Europe.

This is done by several dedicated teams carrying out specific tasks. Their work is done in collaboration with relevant groups within Digital's Engineering organizations.

The Israeli engineering activities are divided into two major areas:

1. Engineering Projects

- OpenVMS AXP testing
- Testing technologies
- UNIX/CALYX support

2. International Systems Engineering

- Localization
- Coengineering
- Architecture
- Original engineering

Digital Israel Engineering Projects

"The goal of our OpenVMS AXP Testing group is to contribute to the quality of OpenVMS AXP software, by providing and supporting tests, and other methods of product verification," says Gil Weiser, general manager of Digital Israel.

At present, the Israeli OpenVMS AXP Testing Team consists of high-level software engineers, some of them are new immigrants from Russia.

All the testing work done by this team, is in accordance with, and in full collaboration with the

OpenVMS AXP Verification group in ZKO.

The OpenVMS AXP Verification group sets the goals, specific tasks, priorities, and approves the milestones and time table.

Our engineering team in Israel develops the environment and the tests against the appropriate subsystems. The team members design and perform the tests, issue and submit QARs (Quality Assurance Reports), supply the documentation, as well as the source code, and maintain the test suites.

"Our basic strategy in testing is to design and develop a comprehensive test suite of test cases, based on the 'Gray Box' methodology," says Shlomo Feldman, technical leader of the OpenVMS AXP Testing Project. "This methodology includes all functionality testing, based on documentation and a thorough understanding of source code."

The OpenVMS AXP Testing Team has developed a first version of a Test Driver, which provides an environment that allows a user to develop, build, and execute tests. It provides common library functions and a control mechanism for test execution and sequencing of individual test cases in a test module.

This tool, called TESTER, includes the following functions:

- Common environment and control mechanism for test execution
- Hierarchical test-suite structure
- Sequencing of test cases in a test module
- Common library of functions for the test developer
- Common repetitive tasks, done by the TESTER, on behalf of the application
- Regression testing mechanism (integrated with DTM)
- Concurrent synchronous/ asynchronous processes
- Symbolic names on invocable test cases
- Static/Dynamic enable/disable test case execution
- Debug and traceability support
- Mixed build and execution environment — OpenVMS AXP
- User extendability of TESTER common library
- Auxiliary TESTER tools

Pictured r-l: Don Harbert (VP VMS Group), Nitzan Hefetz (Engineering Projects Mgr.), Boris Raikhlin, Shlomo Feldman, Shlomo Urbach, Zvi Palgi, Oleg Fraimovich, Yaacov Fenster, Boris Gubenko.

Testing Technologies Team

Growing in a "project oriented" fashion, the current Testing Technologies Team is in close working relations with the Engineering organization of the Digital Repair Center in Nijmegen, Holland. At Digital Holland's request, our Testing Technologies Team has developed various products.

CIS - Console Interface Service
The Console Interface Service is a software product that allows users to connect and manage hardware objects under test, through an RS232 console port. The CIS is an integral part of the Information Based Repair (IBR) project, now under development by Digital in Europe.

VMD - VAX Memory Diagnostics
VAX Memory Diagnostics is a software tool used in the process of memory module diagnosis. VMD has the capability to display test results down to the suspected chip name. It also supplies users with relevant guidelines for repair. The product has already been installed in 14 DRO locations, worldwide. VMD was enhanced recently to an RMD-RISC Memory Diagnostics version, to cover the diagnostics and repair needs of RISC memory modules.

FFI - Functional Failure Isolator
Today, the Israeli Testing Technologies Team is developing a Functional Fault Isolator (FFI); a test tool for the diagnosis and repair of microprocessor based modules. The FFI is a dedicated ROM emulator, which includes special hardware and software features, aiming to support the diagnostics activities of the Module Under Test (MUT), in the DRO repair environment.

UNIX/CALYX Team
The UNIX/CALYX Team is working in collaboration with ISS Systems

In this photo, Don Harbert (left) and Gil Weiser, General Manager of Digital Israel (second from the right), meeting members of the Israeli press.

Engineering. Major tasks carried out by the team are:

- Nonvolatile disk cache driver development
- NFS/network benchmarks
- Buyer's workbench project
- Ongoing support of major European accounts

International Systems Engineering

The International Systems Engineering (ISE) group is engaged in several major projects of localization, coengineering, architecture, and original engineering, in order to answer the specific needs of the international market.

Summary

Through Digital's sophisticated communication networks, the Israeli engineering groups are tightly integrated with engineering groups in the United States, Europe, and Japan. Digital Israel's General Manager, Gil Weiser, explains that due to time intervals and different weekends (in Israel, Sunday is a working day), the Israeli Engineering teams are working when other foreign groups are not. This creates a 24-hour work cycle.

In addition to the R&D in the Engineering organization of Digital Israel, Digital Jerusalem, established in 1985, a design center for VLSI chips. "These chips are at the leading edge of technology, for which only world-class engineers can complete the designs. In Israel we have found these world-class engineers," says Vice President Don Harbert. "The design group has successfully designed several chips that have given our products unique capabilities in the area of computer communication."

Besides sales and R&D, Digital's activities in Israel include software development and joint projects with Israeli firms. This has already led to the integration of Israeli products in Digital systems worldwide.

Digital Israel has established a business development center, which surveys both the Israeli marketplace and the demands of Digital's worldwide customers. The center attempts to match Israeli technologies, ideas, and know-how with Digital customer's needs worldwide.

Digital's Israel headquarters is in Hertzliya (near Tel-Aviv). Other facilities are in Haifa and Jerusalem.. There are over 3,000 Digital systems installed and successfully operating in Israel.

Digital Israel has over 2,000 customers in Israel. A major Israeli market research company recently published the findings of its survey, which concluded that Digital Israel has 50 percent of the total mid-range computer market and 30 percent of the total workstation market in Israel.

There are 75 Israeli software houses engaged in developing Digital-based applications in collaboration with Digital Israel.

It is the intention of Digital Israel Engineering group to continue working aggressively to achieve Digital's commitment to innovation and progress.

Don Harbert and Gil Weiser.

OpenVMS Partners Bid Farewell to Ken Olsen

Ann Grecoe

Open VMS Partner Program Manager Ann Grecoe presenting plaque to Ken Olsen.

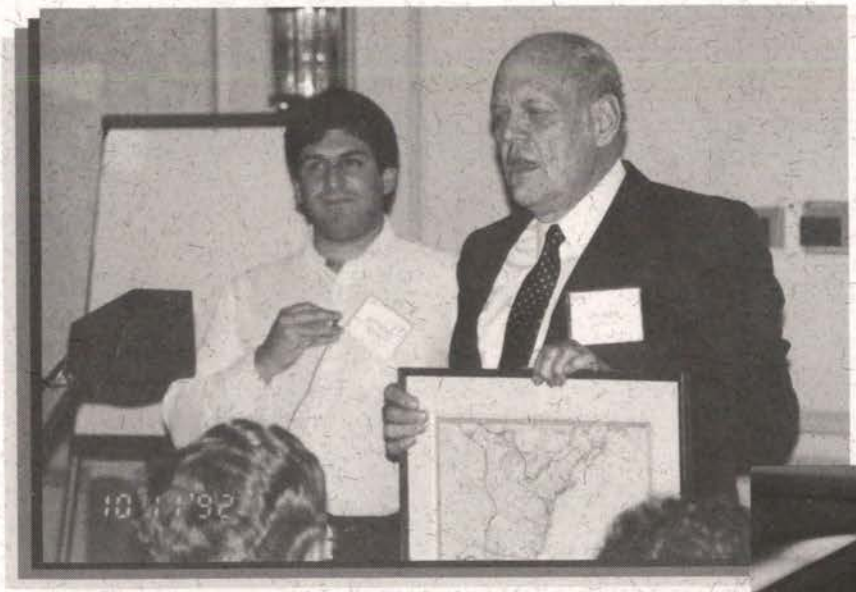
On October 11 to 16, the eighth meeting of the OpenVMS Partner Program was held in Nashua, NH. Each OpenVMS Partner sent their personal and heart-felt appreciation to retiring President Ken Olsen for his continuous respect and support of their technical expertise and their value to the Company.

After opening remarks from Bill Demmer, Vice President of AVS, and Don Harbert, Vice President of OpenVMS Engineering, the Partners bid farewell to Ken Olsen. In appreciation of the support Ken has provided the OpenVMS Partner Program over the years, Jeff Needle, on behalf of the OpenVMS Partners, presented Ken with a framed antique map of North America, since one of Ken's hobbies is collecting maps.

Ann Grecoe, OpenVMS Partner Program Manager, then read a plaque the Partners had written to Ken upon learning of his retirement. Each Partner signed the plaque and extended an invitation to Ken to remain an OpenVMS Partner and to return to their meetings as a fellow engineer.

Over 200 employees crowded the ballroom of the Clarion to hear Ken reflect on the Company he started in 1957 with three employees and some lawn furniture.

When Ken thought the evening had ended, he was surprised once more when four of the OpenVMS Partners, Paul Blaney of Canada, Pierre Dysli of Switzerland, and John Lynch and Carlos Santiago of the US, wheeled in a cake in the shape of an 11/780, the first system to run VMS!



Open VMS Partner Jeff Needle presents antique map to Ken Olsen.

October 12, 1992

Dear Ken:

Each and every OpenVMS Partner sends their personal and heart-felt appreciation for the encouragement, support, and wisdom you have continually provided us. Your candid remarks at the podium, your open acceptance of our questions and feedback, and your willingness to actively participate in the OpenVMS Partners program are unequaled in the Industry and will be deeply missed.

You have seen the energy we bring to our customers, have heard our remarks, and have provided a competitive advantage to us as OpenVMS Partners . Upon your retirement, we extend you the invitation to remain an OpenVMS Partner; to return to our meetings as a friend and fellow engineer; to keep our spirits and our goals soaring.

We are thankful for all you have done, all you stand for, and the challenges you have left for us to complete. Our words and thoughts for you on your retirement are kind ones; our memories are fond ones; and our thanks are immeasurable.

Sincerely,

The OpenVMS Partners

Presenting cake in the shape of the 11/780 is Paul Blaney (Canada), John Lynch (US), Pierre Dysli (Switzerland), and Carlos Santiago (US), all OpenVMS Partners.

A Royal Release!

Dennis McCormick

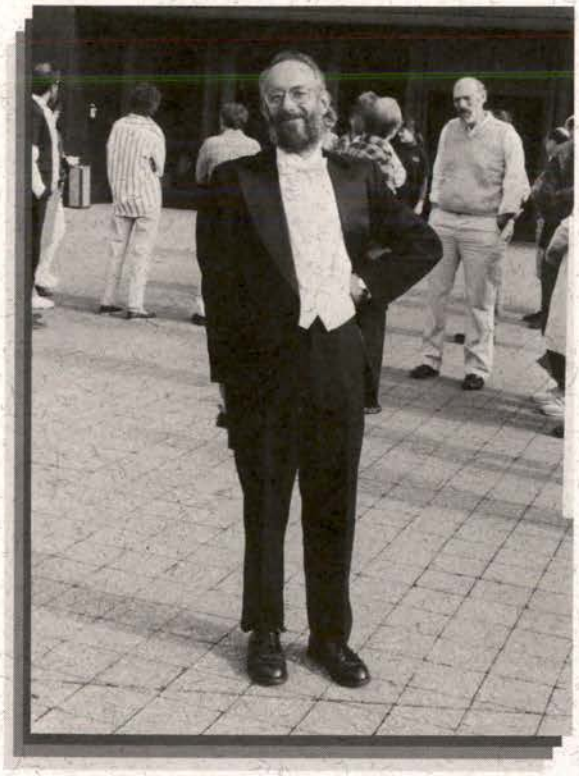
Quietly, the gleaming white Lincoln stretch limousine glides into position outside the ZKO3-2 entrance at Digital's Spitbrook Road facility. The chauffeur-bodyguard piloting it emerges quickly, anticipating his grand charge's exit. The time — 10:16 A.M., October 30, 1992.

Inside, a gathering of engineers in the Metcalfe-Boggs conference room crackles with excitement. The celebrity is immersed in royal garb. Escorts prepare themselves. The final pronouncement is declared, "All is ready!" Word flies by E-mail and word-of-mouth, "10:30 is the time!"

Outside, the crowd multiplies — chattering, laughing, cameras already snapping. The chauffeur, catching a spot in the reflection on the limousine's sun roof, hurriedly attacks it with a shot of window cleaner and a swipe. Above, others line the fourth floor plate glass for an aerial view of the event.

A stirring from inside — all faces turn. An engineer, decked in white tie and tails for the celebration, stands ready near the door. A shout goes up. Escorted by a cheering crowd, and arrayed royally in purple and gleaming gold — it's OpenVMS AXP Version 1.0! Pictures are taken. More cheers, into the limo, and off to SSB in Westminister flies the first operating system to be released for Digital's new Alpha AXP chip.

The above celebration was a demonstration of the excitement and pride with which the OpenVMS AXP engineering group released Version 1.0. Only three weeks off the originally scheduled release date set over two years ago, this release set a new standard for production and quality.



The "royal garb"— a purple cloth bag in which was placed the tapes for the trip to SSB — was signed in gold ink by contributors to the project, and will be permanently display in the ZKO facility Hustvedt conference room. Purple and gold are the official Alpha AXP logo colors. The bag and limousine were the ideas of and personally funded by members of the OpenVMS Alpha AXP engineering team.

VAXstation 4000 Model 90 Design

Michael Callander, Sr. Principal Engineer and
Andrew Ladd, Principal Engineer

Introduction

The VAXstation 4000 Model 90, code named Cougar, is the newest member of the VAXstation product line. Based on the NVAX processor chip, the Model 90 provides significantly more CPU performance than any previous VAXstation. Rated at 32.7 SPECmarks, the system provides 2.7 times the performance of its predecessor, the VAXstation 4000 Model 60. Model 90 is available as a complete system or as a board upgrade to the Model 60 systems. The Model 90 systems are available with three different graphics accelerators, a maximum of 128MB of main memory; integrated Ethernet, and SCSI-1 adapters. It also has an optional TURBOchannel adapter and an optional synchronous communications adapter

Three major goals were initially defined for the Cougar project: CPU performance, time-to-market, and upgrade compatibility with the VAXstation Model 60. The performance and time-to-market goals were driven by the state of the workstation marketplace. High-performance RISC workstations had become a dominate force in the workstation market and a significant improvement in performance was required to keep OpenVMS VAX workstations competitive. Cougar achieves the performance necessary to provide customers with a high-speed OpenVMS VAX workstation before migrating to higher performance Alpha AXP systems.

CPU performance was the focus of the Cougar design, although equivalent or better graphics performance was highly desirable. The project performance goals were to achieve 2.5 times the CPU performance of the Model 60 and to stay on par with the Model 60 in graphics performance. In the end, Cougar exceeded the CPU performance goal as well as achieved higher graphics performance than the Model 60.

The Cougar development schedule called for an eleven-month period from project start to first revenue shipment. To meet this aggressive design schedule, a clear set of design guidelines and methodologies were put in place by the design team. The first rule was to borrow as much logic from existing designs as possible. Secondly, all new logic had to be implemented in off-the-shelf parts or in programmable logic. At the time, the available resources did not allow for a design of a completely new NVAX system nor did the schedule permit the time for developing custom or semi-custom chips. The final piece of the design methodology was to build a single prototype system and have it running within three months of the project start. This system would serve as a debugging and verification platform for any new programmable logic and as a software development system.

There were several advantages to designing Cougar as a module upgrade to the Model 60 system. First, it provided customers with a low-cost upgrade path by maintaining their investment in memory, I/O, and graphics options. Second, the designers reduced the engineering effort required to develop the system. This was true because Cougar uses the same enclosure, power supply, memory SIMMs, I/O options, brackets, cables, and two of the same graphics options used in the Model 60. An upgrade consists of a simple board swap and possibly a graphics option change.

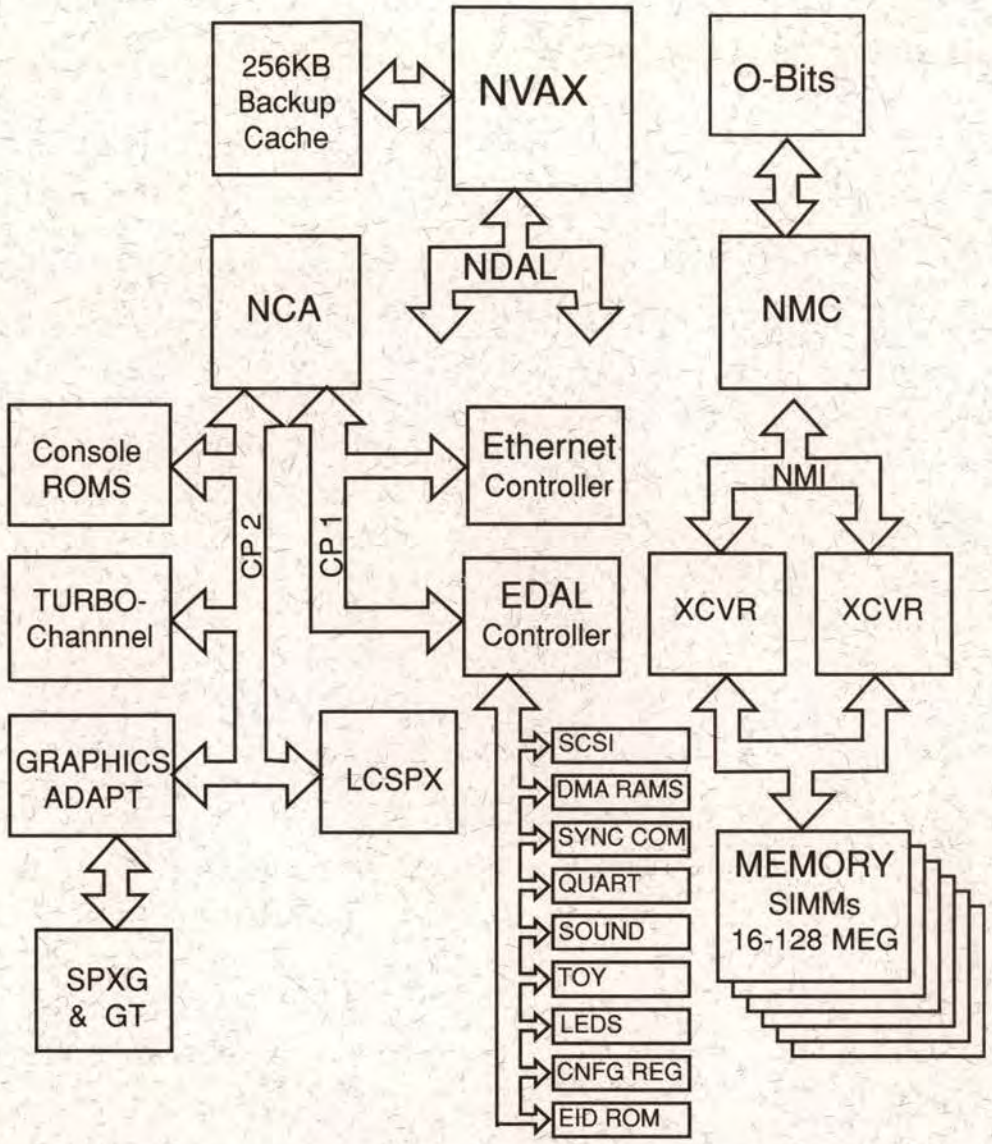


Figure 1

Cougar Development

One of the key factors that led to Cougar's successful development was the existence of the VAX 4000 Model 500 system. This system, code named Omega, was nearing completion when Cougar was proposed. Omega offered a high performance, single processor, highly integrated NVAX system on which a VAX workstation could be based.

The Omega system core was used as the starting point of the Cougar system. As shown in Figure 1, this core consisted of three custom chips: the NVAX CPU, the NVAX Memory Controller (NMC), and the NVAX I/O Adapter (NCA). In addition, the core supported various write back secondary cache sizes. The three custom chips communicate via a 64-bit bus named the NDAL. The NMC provides a high-performance memory interface for the NVAX and the NCA. It controls a 64-bit memory bus, named the NMI, used to communicate with the DRAM SIMMs. The NCA provides an interface between the NVAX and two independent CDAL busses, which provide either programmed I/O (PIO) or direct memory access (DMA) support for the I/O devices. By using the NMC and NCA chips with the NVAX processor, the Cougar design team utilized a well defined base system on which they integrated the memory, I/O, and graphics subsystems required for a workstation.

The Cougar memory design was very straightforward. The NMC expected memory to be configured in sets, where each set contains two 64-bit interleaved banks. A 32-bit low-cost gate array, used on the VAXstation VLC, was chosen to perform the multiplexer and transceiver functions required for this interleaving. Two of these gate arrays were used to implement the 64-bit to 128-bit memory data path.

The NMC contained most of the memory control logic, so only a single PAL was required externally to generate bank selects and control signals for the transceiver gate arrays. Memory was configured as two sets that use four of the Model 60's memory SIMMs to form each set. Cougar supports memory configurations of 16MB, 32MB, 64MB, 80MB, or 128MB.

Cougar's I/O design centered on interfacing the various standard and optional I/O devices onto the two CDAL busses provided by the NCA. The base system requirements included SCSI, Ethernet, Quad Uart, sound, and time-of-year support. Optional devices included a synchronous communication adapter as well as a TURBOchannel adapter. Aside from the TURBOchannel adapter, all Model 60 I/O support was provided by a private I/O bus called the EDAL. The Model 60 used a modified CDAL bus to handle the TURBOchannel adapter.

The easiest method to support the EDAL I/O devices, from both a software and hardware perspective, was to design an EDAL interface to one of NCA's CDAL busses. The design team accomplished this by designing the interface using two Xilinx Field Programmable Gate Arrays (FPGA). The CDAL to EDAL Adapter Chip (CEAC) controlled most of the functionality of the interface while the SCSI Quadword FIFO chip (SQWF) provided the SCSI DMA data path. Most of the Cougar design work revolved around these two Xilinx chips.

Module space and routing requirements forced the design team to pursue devices with fairly high integration levels. One unique benefit of using the Xilinx FPGAs was the ability to get good integration levels and pin counts on each chip while having the flexibility to reprogram the devices. The time required to fix a bug after it was identified was usually less than an hour as opposed to the many weeks it took to fabricate another gate array. Later, when the design was stable, these two chips were converted to standard gate arrays produced by Hudson's semi conducter plant. Converting the Xilinx chips to gate arrays contributed to a significant cost savings in the overall CPU module manufacturing cost.

Pictured l-r: Tom Wenners, Andy Ladd, Mike Warren, Mitch Noreross, Lauren Carlson, Pat Sullivan, Gregg Bouchard, Mike Callander, and Curt Miller.

Early in the design phase, the team decided to take the Ethernet functionality off the EDAL and place it directly on one of the CDAL busses. Although the Lance Ethernet controller connected directly to the EDAL, it required a significant amount of support from the CEAC and SQWF chips, including DMA address mapping hardware. The design team quickly realized that Omega's Ethernet controller, the SGEC chip, already connected to the CDAL and required minimal support from the FPGAs. In addition, the SGEC software drivers already existed in this configuration, which further reduced the work required to support the Ethernet controller.

After the Ethernet controller was stripped from the EDAL, the only remaining DMA device left on the EDAL was the SCSI controller. The CEAC and SQWF both combine to form a SCSI DMA controller that produces higher DMA bandwidth than that of the Model 60. The EDAL supports a Quad Uart Chip, which provides four serial lines for the keyboard, mouse, modem, and printer/console ports. It supports a sound chip that allows both record and playback functions through a jack on the front panel. An optional synchronous communications adapter that connects to the EDAL supports synchronous WAN communications. Finally, other devices such as the watch chip (which contains the time-of-year counter and battery backed-up RAM) and the Ethernet ID ROM are also supported on EDAL.

The Cougar VAXstation supported the TURBOchannel bus with the TURBOchannel Adapter module, previously designed for the Model 60. This adapter provides one TURBOchannel slot at the rear of the Cougar system. It was fortu-

nate for the design team that this adapter already interfaced to a bus very similar to the CDAL. Two small PALs were all that were required to interface the TURBOchannel Adapter to one of NCA's CDALs. One of these PALs also supplied the bus arbitration control for the same CDAL. In the graphics area, Cougar provides support for three options. The SPXg and SPXgt modules offer 3-D graphics acceleration and the LCSPX module offers 2-D graphics acceleration. Both the SPXg and SPXgt are offered on the Model 60 while the LCSPX is a new graphics option offered only on Cougar.

The base graphics option for Cougar is the LCSPX module, which is a high-performance 2-D graphics accelerator. The entry level 2-D graphics accelerator offered on the Model 60 is called Low Cost Graphics (LCG). LCG is the only option offered on the Model 60 that is not offered on Cougar. Cougar abandoned LCG in favor of the LCSPX because much of the LCG functionality was implemented in a gate-array that was not compatible with Cougar. It was beyond the project's schedule to design an LCG compatible controller.

Because LCG was not feasible as an entry-level graphics option on Cougar, the design team searched for an alternate 2-D graphics accelerator. They found that a new X terminal, the VXT 2000, was being developed with graphics based on a cost reduced version of the SPX graphics module originally used in VAXstation 3100. Coincidentally, the VXT 2000 graphics module interfaced directly to a CDAL bus and was also software compatible with the original VAXstation 3100 SPX option. As a result, the module could interface directly with one of the CDAL busses and required only minimal software effort to work with Cougar. Therefore, the VXT 2000 graphics module was chosen as the basis of Cougar's entry level graphics option based on ease of design into the system.

The VXT 2000 module presented only two problems to the design team. First, the module was the wrong shape to fit directly into the Cougar enclosure. This was fixed with a simple module relayout in order to fit within the enclosure. This new module was named LCSPX.

The second problem was performance. Based on early performance predictions, it was determined that LCSPX would be as fast as the Model 60's LCG on many operations, but would be slower on others. In order to provide a higher performance option, a speed analysis was performed on the LCSPX. The original speed was set at 20MHz. However, it was determined that by upgrading a number of components, such as VRAMs, DRAMs, SRAMs, and the Scanproc, the LCSPX could run at 25MHz. This 25 percent speed increase brought LCSPX performance to a point where its performance exceeded LCG for almost all graphics operations.

Model 60 SPXg and SPXgt graphics options were the only 3-D graphics accelerators available on any VAX workstation. SPXg is an 8-plane 3-D graphics accelerator, while SPXgt is a 24-plane 3-D graphics accelerator based on the SPXg design. The design team decided to support SPXg and SPXgt on Cougar because any other non-VAX workstation 3-D option would have required a major software development.

A subset of LCG control logic in the Model 60 provides the interface to the SPXg and SPXgt in that system. An alternate way to interface with these modules was required because, as previously described, Cougar did not support LCG. The design team found that the SPXg/gt development group had designed a VAXstation 3100 CPORT bus adapter, which communicated with the SPXg/gt modules. This adapter was used as an early hardware development tool for SPXg/gt designers.

In addition, VMS level software support already existed for this adapter. This low-speed design utilized a large number of PALs and MSI devices for the interface. This design was easily adaptable to one the CDAL busses on Cougar. As a result, a high-speed, high-density version of this adapter was designed for the Cougar system module using two large AMD MACH PALs and a few MSI components. The AMD MACH PALs provided the logic density, speed, and high pin count required to design an interface to the SPXg/gt modules and provide system level 3-D performance comparable to the Model 60.

Cougar Verification

The use of the Omega core chip set and the use of programmable logic for all new parts of the design led the Cougar design team to an interesting verification methodology. Instead of relying solely on traditional simulation for verification, a breadboard was built to verify the Cougar I/O and graphics subsystems.

The team used an Omega system in a test backplane as the heart of this breadboard system. The actual breadboard was an etch module containing all the logic on the two Cougar CDAL busses. The breadboard was physically attached to the Omega CPU module via extended socket pins from the NCA chip. These pins were soldered into the breadboard, connecting the breadboard CDAL busses to the CDAL busses on the Omega CPU. The designers utilized a phase lock loop on the breadboard, which regenerated the CDAL clocks to minimize clock skew. This configuration

allowed the CDAL busses to run at full speed.

The breadboard had a number of features to facilitate debugging and to make quick design changes. All important signals were buffered and sent to stake pins for logic analyzer connections. The pinouts on the two Xilinx gate arrays were fully reconfigurable via six-inch coax jumper wires. All the MACH PALs had through-hole resisters at each pin to allow for quick pinout modifications. By utilizing a slightly modified Omega console, it took the design team only a few weeks to debug and verify all the breadboard logic including the EDAL and graphics interfaces and devices. As bugs were found they were quickly fixed in the programmable parts, often in a matter of minutes.

The breadboard was also used as a software debugging platform. Because the breadboard was software compatible with the final Cougar system, the Cougar console, and diagnostic, the VMS teams utilized the breadboard while real Cougar prototypes were being built. During this time, a base version of the console and diagnostic code was developed and debugged. VMS boot support, SCSI, Ethernet, serial line, sound, and graphics drivers were all debugged on the breadboard.

This early breadboard system provided a rich environment for debugging and design verification. Once real prototype systems were available the console and VMS operating system came up in less than a day. This allowed the project to quickly ship a large number of systems to a wide variety of internal sites for development and verification work. After the initial prototype systems were available, only one additional logic bug was found in the system design. Again, because programmable logic was used, this bug was easily corrected.

CPU and Graphics Performance

The Cougar workstation is the fastest VAX workstation ever produced. It is comparable to Digital's current RISC based workstations and is competitive with many of the workstations now offered by the industry. Using the SPECmark benchmark suite, Cougar performs 2.7 times faster than the Model 60. Table 1 illustrates the CPU performance of Cougar compared to other Digital workstations.

The LCSPX performance exceeds the performance of the Model 60's LCG option for most graphics operations. Table 2 compares Cougar's LCSPX graphics performance with other Digital workstations. Table 3 illustrates SPXg and SPXgt performance on Cougar and Model 60, compared against other Digital workstations.

Conclusion

As mentioned in the introduction, the Cougar development schedule called for first revenue shipments starting eleven months after the project started. Although the manufacturing plant built shippable hardware within the eleven-month goal, the first revenue shipments actually occurred one month later. While the team came very close to meeting their time-to-market goal, they exceeded the CPU and graphics performance goals.

TABLE 1 CPU Performance Comparison

Workstation	SPECmark Rating
VAXstation 4000 Model 90	32.7
VAXstation 4000 Model 60	12.0
VAXstation 3100 Model 76	6.8
DECstation 5000 Model 240	32.4

TABLE 2 2-D Graphics Performance Comparison

Workstation	2-D Area Fill (Mpixels/sec.)	2-D Vectors (Kvectors/sec.)
VAXstation 4000 Model 90 LCSPX	18.2	266.0
VAXstation 4000 Model 60 LCG	14.6	216.0
VAXstation 3100 Model 76 SPX	14.2	183.0
DECstation 5000 Model 240 PXG	13.9	263.0

TABLE 3 3-D Graphics Performance Comparison

Workstation	3-D Polygons (Kpolygons/sec.)	3-D Vectors (Kvectors/sec.)
VAXstation 4000 Model 90 SPXgt	33	295
VAXstation 4000 Model 60 SPXgt	33	300
VAXstation 4000 Model 90 SPXg	30	295
VAXstation 4000 Model 60 SPXg	30	295
VAXstation 3100 Model 76 SPX	6	57
DECstation 5000 Model 240 PXG	52	302

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