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ON THE COVER

An artisan's concept of expanding bit density.

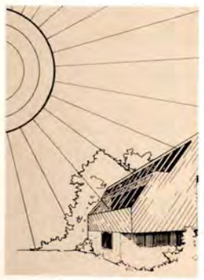


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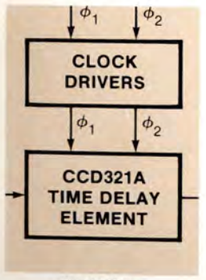


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64K CCD Memory

First Low-Cost Solid-State Bulk Memory

by Bruce Threewitt

In 1975, the first charge-coupled device (CCD) digital memory (9216 bits) appeared as part of the CCD family. The earliest CCDs were of simple architecture to demonstrate the feasibility of the CCD memory concept. Subsequent architectural advances succeeded in filling the memory gap between mechanical memories and semiconductor RAMs but were not particularly consistent with memory cost goals. Recently, high-volume RAM and high-volume CCD manufacturing technologies have merged. This factor, in conjunction with bulk memory-like architecture, has resulted in the production of a highly dense, low-cost bulk storage device.

Charge coupling is the collective transfer of the mobile minority charge carriers in a semiconductor storage element to a similar adjacent storage element by simply manipulating the voltage externally. The amount of electrical charge in each element represents information. Interconnection of the storage elements is made through the substrate, thereby reducing space requirements for interconnects.

These features reduce memory cell size by as much as a factor of three *(Figure 1)*, simplify the manufacturing process, and improve yield. Also, NMOS logic circuitry can be incorporated in the periphery of the memory chip to provide control logic functions, resulting in optimum architectural flexibility. Furthermore, little peripheral circuitry is required for a CCD memory, resulting in efficient use of chip area.

In less than three years, CCD memory chip capacity has increased sevenfold, from 9K to 64K bits. This rapid growth, nearly double that of MOS dynamic RAM *(Figure 2)*, can be attributed to several factors:

- Compatibility with MOS process technology
- High packing density, resulting in low cost
- Low power dissipation, giving higher reliability
- Improved yield due to dark (leakage) current averaging*
- Fewer contacts per bit, resulting in better yield*
- Low testing cost
- Faster access time (latency) than magnetic storage memories and higher data rate than large MOS RAMs.

Perhaps the single most important reason for CCD success is that the fabrication technique is the same as that used to manufacture high-volume, n-channel MOS RAMs. Consequently, the years of experience with a familiar manufacturing process can be put into practice immediately.

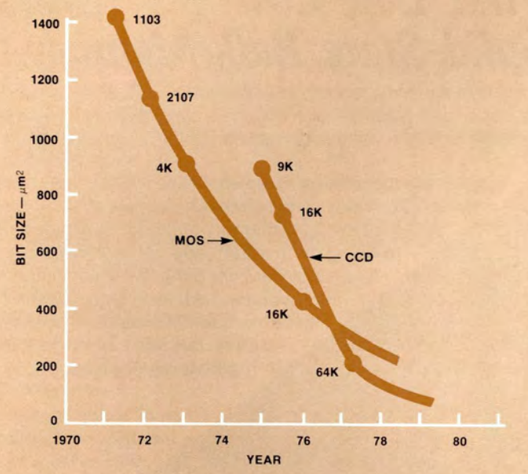


Fig. 1 CCD and MOS Memory Bit (Cell) Size Improvement

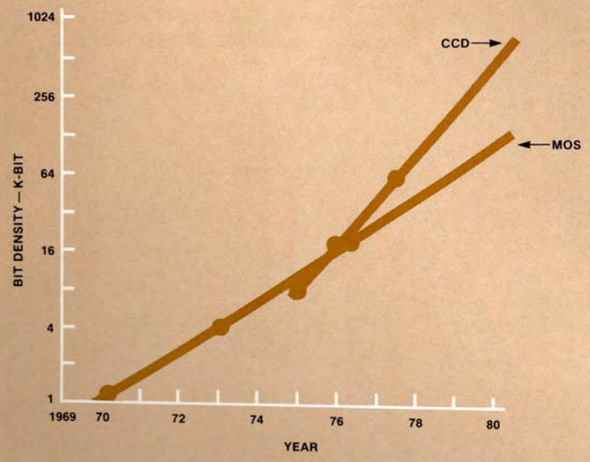


Fig. 2 CCD and MOS Dynamic Memory Growth

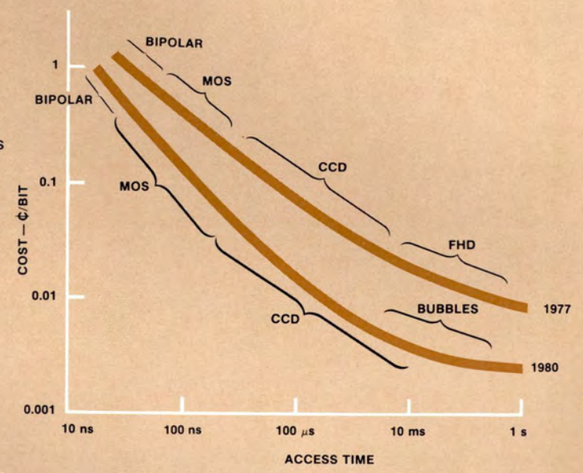


Fig. 3 Memory Cost Versus Performance

*Not applicable to LARAMs

CCD memory is a low-cost alternative for bulk memory and is not intended as a replacement for high-speed RAM. In general computer architectures, a memory can be utilized as a cache for storing data in block form, which need not be accessed randomly. Since a computer usually performs operations sequentially, it is well suited to CCD serial organi- of memory cycle s time, thus making emory more prac- in *Figure 3*, CCDs and RAMs and at a s.

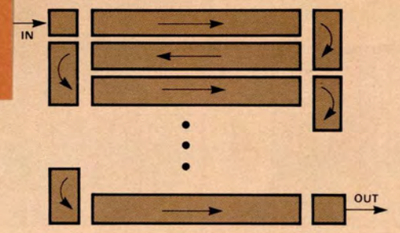
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age applications, it chitecture, process ce characteristics. *re 4)*, offering vari-

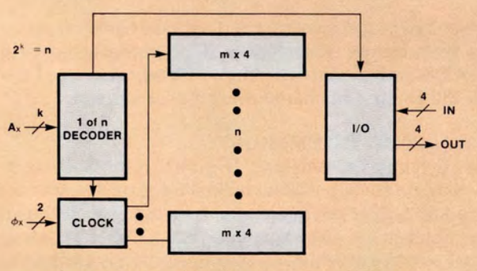
simplest organiza- quency range.

- Line Addressable Random Access Memory (LARAM) — a combination of CCD and RAM architectures. This memory offers high performance (low power dissipation, low clock capacitance, excellent latency) but lacks the high density required for low-cost memory.
- Serial Parallel Serial (SPS) — the best organization for high-density, cost-effective memory. Combines the performance and density benefits found in other architectures with significant latency improvements when compared to magnetic media.

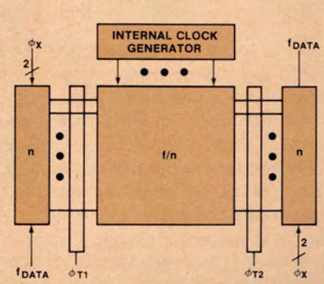
Development of the SPS architecture is in keeping with the goal of replacing magnetic bulk-storage memories with semiconductor memories. Briefly, SPS works like this. Data is entered into a serial input register at frequency f. When the register is full, a serial-to-parallel conversion occurs, and data is shifted in parallel at frequency f/n, where n is the length of the serial register. At the other end of the parallel register, a parallel-to-serial conversion takes place, and data is shifted out at frequency f.



SERPENTINE ARCHITECTURE



LINE ADDRESSABLE RANDOM ACCESS MEMORY (LARAM)



SERIAL-PARALLEL-SERIAL ARCHITECTURE

PARAMETERS	SERPENTINE	LARAM	SPS
DENSITY	GOOD	POOR	EXCELLENT
POWER	HIGH	LOW	LOWER
FREQUENCY RANGE	WIDE	LIMITED	LIMITED
LATENCY	AVERAGE	EXCELLENT	POOR
CLOCK LOADING	HIGH	LOW	LOW

Fig. 4 CCD Memory Architecture

These features reduce memory cell size by as much as a factor of three *(Figure 1)*, simplify the manufacturing process, and improve yield. Also, NMOS logic circuitry can be incorporated in the periphery of the memory chip to provide control logic functions, resulting in optimum architectural flexibility. Furthermore, little peripheral circuitry is required for a CCD memory, resulting in efficient use of chip area.

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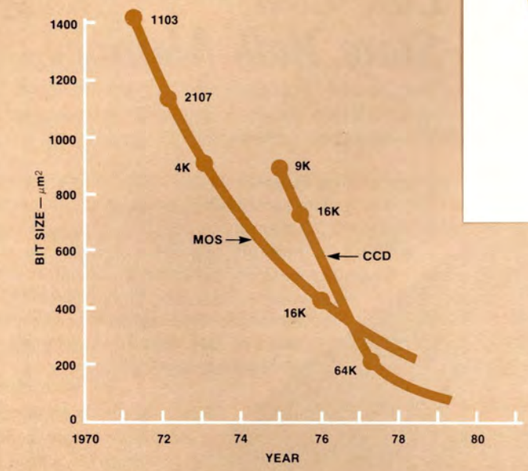


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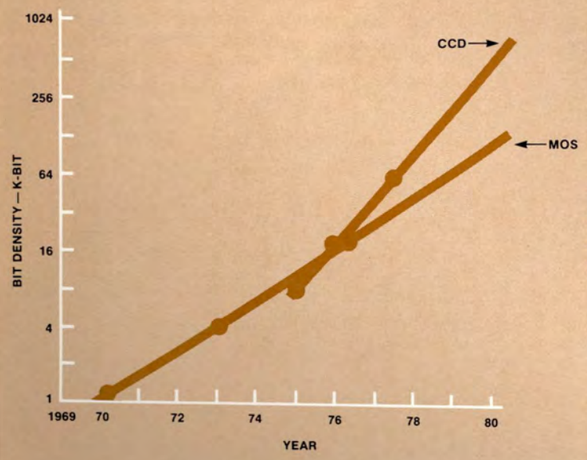


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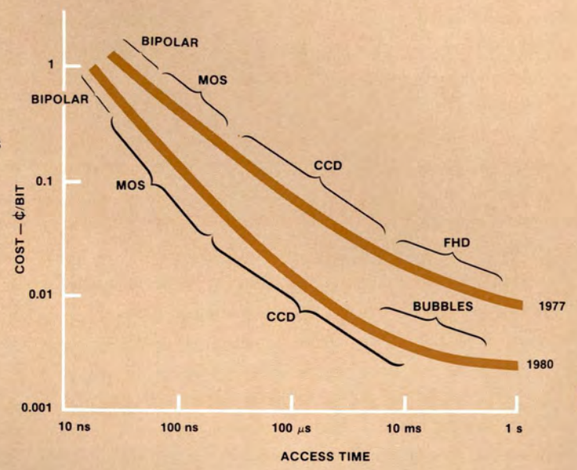


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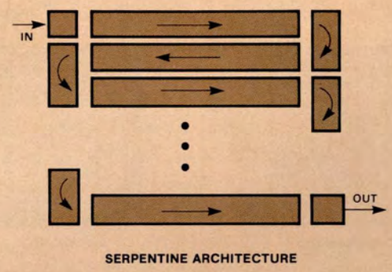
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CCD MEMORY COMPONENT ARCHITECTURES

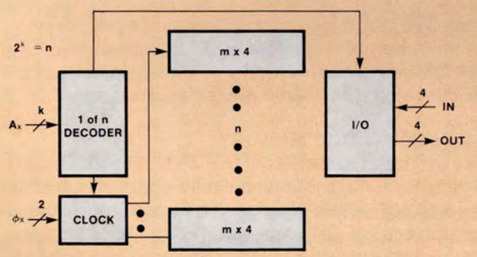
To produce a CCD memory for bulk-storage applications, it is imperative to select the appropriate architecture, process and clocking schemes to optimize device characteristics. There are three major architectures *(Figure 4)*, offering various cost-performance trade-offs.

- Serpentine or synchronous — the simplest organization featuring a wide operating-frequency range.
- Line Addressable Random Access Memory (LARAM) — a combination of CCD and RAM architectures. This memory offers high performance (low power dissipation, low clock capacitance, excellent latency) but lacks the high density required for low-cost memory.
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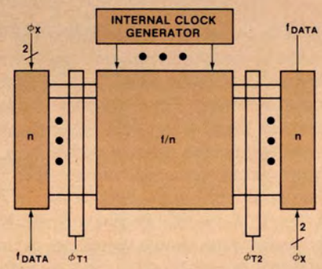
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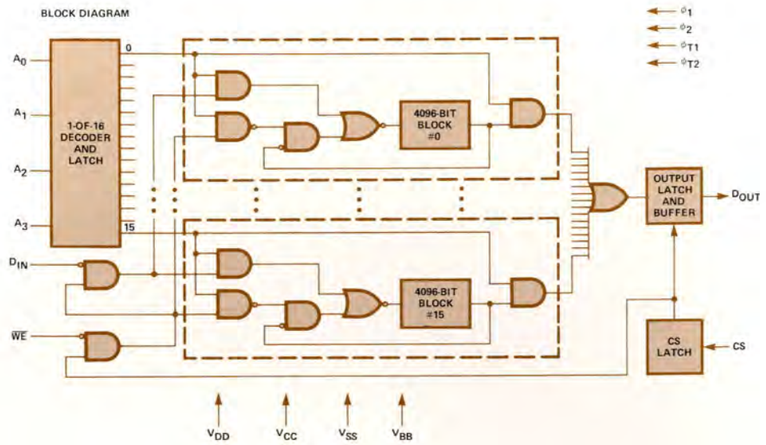


Fig. 5 F464 Block Diagram

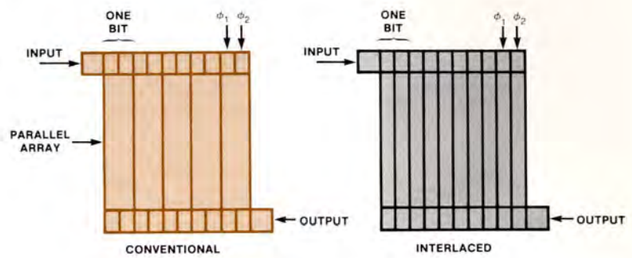


Fig. 6 SPS Structures

The SPS structure is extremely dense since the serial-to-parallel and parallel-to-serial conversions require little overhead logic. Rather, these conversions involve clocking the cells in a different direction. Four external clocks are required to accomplish these functions, two phases for the serial registers and two for the parallel conversion. The two parallel-conversion clocks are only connected to the interface between the serial and parallel registers.

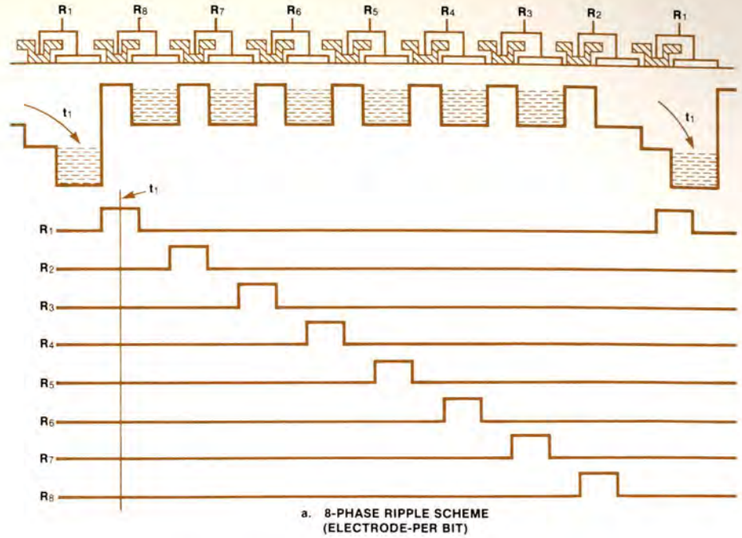
Since parallel conversion is a low capacitance function, the external input capacitance of these two phases is very low. The serial-register clocks only drive 2n bits per block; therefore, the clock capacitance for these clocks is also relatively small. The low capacitance of all four external phases makes interfacing to TTL logic much simpler with standard low-cost drivers. The internal parallel phases are much lower frequency (f/n; typically n = 64) than the serial-register clocks and can be buffered on the CCD memory chip without dissipating significant power.

The best process approach for SPS architecture is buried channel. It is preferred, at 64K-bit densities, over surface channel because of higher transfer efficiency with no "fat zero" requirement and a higher maximum frequency. "Fat zero," a small (non-zero) amount of charge representing a "0", is required in surface-channel devices to compensate for surface state losses. Therefore, a "0" is represented by a partially full, rather than an empty, storage well that decreases the amount of charge available for storage.

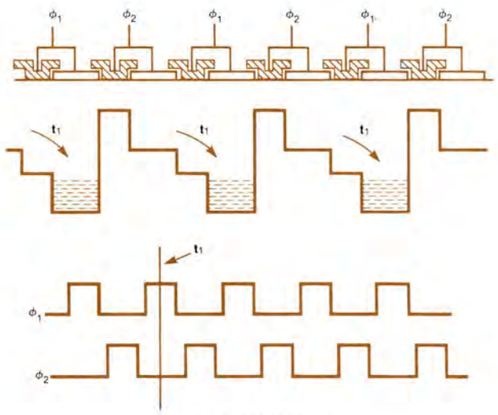
THE F464 64K-BIT CCD MEMORY

The F464 dynamic CCD memory *(Figure 5)* is the first economically feasible semiconductor bulk-storage device. Bits are organized 65,536 x 1 in 16 randomly accessible SPS shift registers (blocks) of 4096 bits each. Four TTL- compatible address inputs are provided for selecting one of the 16 blocks for Read and Write or Read-only operations. Each shift-register block is implemented using an *interlaced* SPS structure in which each bit (two electrodes) of the 2-phase serial input register serves two parallel shift registers *(Figure 6)*. The input serial register transfers data to the odd-numbered parallel registers and then, on a second scan, transfers the next 32 bits of data to the even-numbered parallel registers. As a result, each serial input register stores 32 bits using 64 electrodes that service 64 parallel shift registers. In a conventional SPS structure, each bit of the serial shift register serves only one parallel shift register.

In the usual SPS structure, the minimum width of the parallel shift register is limited to the width of two electrodes of the serial shift register. Using the interlaced scheme, this width is



a. 8-PHASE RIPPLE SCHEME (ELECTRODE-PER BIT)



b. 2-PHASE SCHEME

Fig. 7 CCD Clocking Schemes

limited to that of only one electrode; hence, the packing density is doubled. To further enhance the packing density, an 8-phase ripple technique is used in the F464 to shift the data in the parallel shift registers *(Figure 7a)*. Normally, in a synchronous 2-phase clocking system *(Figure 7b)*, two CCD electrodes are required to store one bit of information, while in a ripple system, a little more than one electrode is needed for storing one bit. In general, the number of electrodes, n_b, required to store one bit is given by

$$n_b = \frac{N}{N-1}$$

where N is the number of ripple clocks.

As the number of ripple phases is increased from two to eight, the number of electrodes required to store one bit is reduced from two to 1.14. Thus, by using the 8-phase ripple system, packing density is almost twice that of a 2-phase system. In addition, the ripple technique reduces the number of transfers required to move a packet from a shift-register input to output. In an M-bit shift register, the number of required transfers is M x n_b. Thus, a 63-bit shift register needs only 72 transfers in an 8-phase ripple system, compared to 126 transfers in a standard 2-phase system. This obviously minimizes signal degradation. Another advantage is the reduction of average leakage current per bit since the charge collected is reduced in proportion to the number of electrodes required to store a bit.

F464 OPERATION

The 16 blocks, each consisting of a 4096-bit SPS shift register for data storage, are randomly accessible using four Address inputs (A_0-A_3). The data in all 16 blocks advances simultaneously at the rate of one bit per cycle. Each block has its own reference charge generator, sense amplifier, input/output

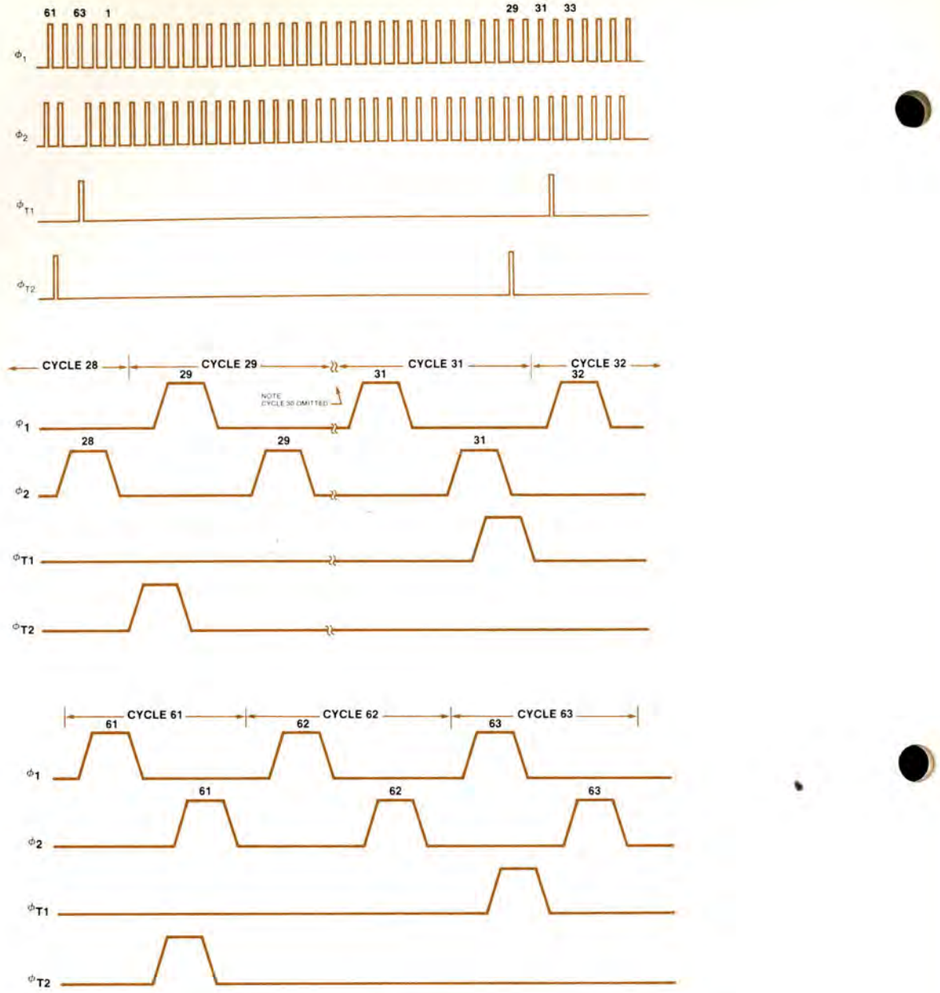


Fig. 8 MOS-Level Clocks

logic, and CCD input circuit. The Data In (D_{IN}), Data Out (D_{OUT}), and Write Enable ($\overline{WE}$) circuits are common to all blocks and are activated by the Chip Select (CS) signal to minimize standby power.

The memory requires four MOS-level clocks *(Figure 8)*. The two high-frequency clocks, ϕ_1 and ϕ_2, run at a frequency equal to the data rate and control the movement of data within the input and output series registers of each 4096-bit block. These clocks also control all the peripheral MOS circuits. The two low-frequency transfer clocks, ϕ_{T1} and ϕ_{T2}, are used to transfer charge from the serial-to-parallel and parallel-to-serial registers of each block.

Interlacing of the data is achieved by first transferring data from the input serial register into the parallel registers when the charge packets are under the ϕ_1 gates, then reloading the input register with the next 32 bits and transferring this data when the charge packets are under the ϕ_2 gates. Parallel-to-serial transfer is accomplished in a similar manner. To achieve proper transfer phasing, the two transfer clocks must be asymmetrical around a 32-cycle interval, but symmetrical around a 64-cycle interval. The ϕ_{T1} and ϕ_{T2} clocks are skewed to achieve correct bit storage in each block. When ϕ_{T1} occurs during ϕ_1 time, ϕ_{T2} occurs during ϕ_2 time, 1.5 cycles prior to ϕ_{T1}. When ϕ_{T1} occurs during ϕ_2 time, ϕ_{T2} occurs during ϕ_1 time, 2.5 cycles prior to ϕ_{T1}. *Figure 8* illustrates the clock phase relationships, which are generated only once in a memory system using simple logic at minimum cost.

The functional timing diagram for a Read cycle is shown in *Figure 9*. The four Addresses (A_0-A_3) and Chip Select (CS) are buffered when ϕ_1 is HIGH. The trailing edge of ϕ_1 latches the information and disables the addresses and chip-select buffers to prevent changes that occur on these pins from entering the internal circuitry when ϕ_1 is LOW.

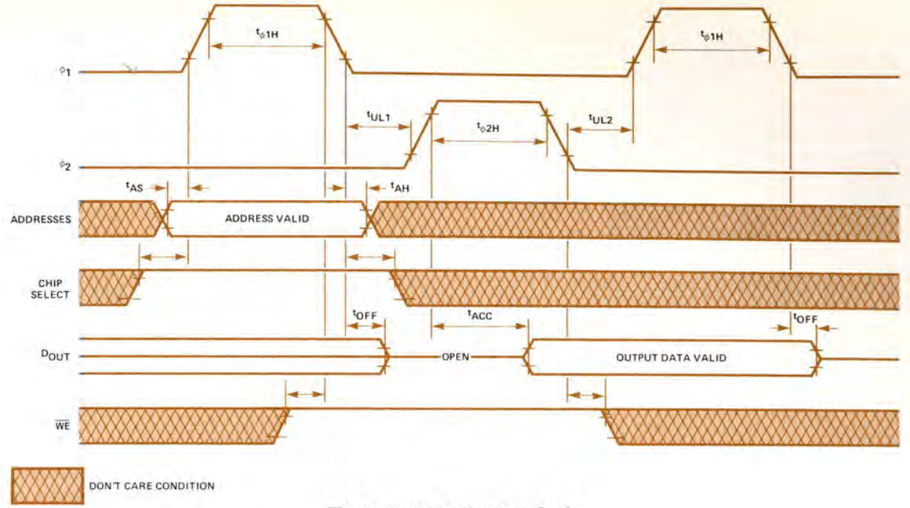


Fig. 9 Read-Recirculate Cycle

The $\overline{WE}$ dynamic buffer is unconditionally preset during ϕ_1 time. In the Read-only mode, $\overline{WE}$ remains HIGH, disabling the buffer. In the Write mode, $\overline{WE}$ may go LOW before or after the trailing edge of ϕ_1, and the $\overline{WE}$ buffer is activated by ϕ_1 going LOW or $\overline{WE}$ going LOW, whichever occurs later. The D_{IN} buffer, which is disabled during ϕ_1 HIGH time, is enabled when the $\overline{WE}$ buffer is activated. Therefore, in the Write mode, the data must be valid before ϕ_1 goes LOW or $\overline{WE}$ goes LOW, whichever occurs later. Following are the four modes of operation.

Standby (Recirculate) Mode
In the standby mode (CS LOW), the contents of all 16 blocks are recirculated automatically, and the device disregards the $\overline{WE}$, Address, and D_{IN} inputs. The output latch goes into the high-impedance state after the trailing edge of the ϕ_1 clock. Minimum power dissipation occurs when the device is operated in the recirculate mode with minimum ϕ_1 and ϕ_2 pulse widths at the lowest allowed frequency.

Read-Recirculate Mode
In this mode ($\overline{WE}$ HIGH and CS HIGH), the data from the selected block is presented to the output buffer immediately following the leading edge of ϕ_2 and appears at the output (D_{OUT}) after a delay equal to the access time t_{ACC}. Thus, the access time is referenced from the leading edge of the ϕ_2 pulse and is independent of the duration of ϕ_2. The output buffer is latched by the trailing edge of ϕ_2 and output data remains valid at the D_{OUT} pin until the end of the ϕ_1 clock pulse in the next cycle. D_{OUT} then goes into the high-impedance state until the next bit is accessed. The data in all 16 blocks recirculates automatically.

Read and Write Mode
In the Read and Write mode ($\overline{WE}$ LOW and CS HIGH), the output data from the selected block is available at the output pin as in the Read-recirculate mode; however, the recirculate path of that particular block is disabled. Input data present at the D_{IN} pin during ϕ_2 is written into the selected block by the falling edge of ϕ_2, while the other 15 blocks automatically recirculate their contents.

Read-Modify-Write Mode
The Read-Modify-Write mode (CS HIGH, $\overline{WE}$ HIGH goes LOW) is simple because the memory is always in the Read mode whenever CS is HIGH. Since the access time is referenced to the leading edge of ϕ_2 and the setup times of $\overline{WE}$ and D_{IN} are referenced to the trailing edge of ϕ_2, this mode of operation requires only an extended ϕ_2 HIGH time to provide the required modify time.

PERFORMANCE

The F464 dynamic serial CCD memory operates over a 1- to 5-MHz frequency range with power dissipation of less than 3.5 μW per bit in the active mode at 5 MHz and less than 1 μW per bit in the standby (recirculate) mode at 1 MHz. Typical capacitance on the TTL-compatible inputs — Addresses, CS, $\overline{WE}$, and D_{IN} — is only 5 pF and, on the 12 V clocks, capacitance is 100 pF (ϕ_1 and ϕ_2) and 30 pF (ϕ_{T1} and ϕ_{T2}). Use of CCD techniques, interlaced SPS architecture and electrode-per-bit design results in a chip of less than 40K mil^2 that fits in a standard 16-pin DIP (300 mils wide).

CONCLUSION

The buried-channel CCD process using SPS architecture, coupled with proven Isoplanar n-channel silicon-gate technology, successfully fulfills bulk memory requirements for high density and low cost. The 64K CCD serial memory is made to order for bulk storage. It should be emphasized that CCD memories are not intended to replace high-speed RAMs. In serial applications, cost/performance trade-offs make 64K-bit CCD more cost effective. Interfacing the F464 with microcomputers is simple due to the solid-state nature of CCD memories. At the system level, peripheral logic requirements are extremely small.

The 64K CCD memory is an excellent vehicle for demonstrating workable techniques that can be used in larger memories such as 256K and 1 megabit. All indications point to 256K CCD memory availability by late 1979 or early 1980 at costs under 10 millicents per bit. Solid-state replacement of mechanical memories will be well under way at that time. □

The author wishes to acknowledge the assistance of Ramesh C. Varshney and K. Venkateswaran in preparation of this article. These two gentlemen, along with their design team, on their first attempt, designed a high-volume low-cost 64K CCD bulk memory.



What is an LCD?

by Keith Riordan

Liquid crystal displays (LCDs) differ from other types of displays in that they scatter, rather than generate, light. Two basic types are available: reflective, which require front illumination, and transmissive, which require rear illumination. Both types use a field-effect cell that is filled with liquid crystal material.

A liquid crystal material is an organic compound — that is, a compound containing carbon, hydrogen, oxygen, and nitrogen — that has the optical properties of solids and the fluidity of liquids. In the liquid crystal state, which is exhibited over a specific temperature range, the compound has a milky, yellow appearance. At the high end of the temperature range, the milky appearance gives way to a clear liquid. At the low end of the range, the compound turns to a crystalline solid.

The molecules of a liquid crystal compound are in the form of long, cigar-shaped rods. Because of the special grouping of the atoms that form these molecules, the rods act as dipoles in the presence of an electrical field. This characteristic enables the molecules to be aligned in the direction of the electrical field and provides the basis for operation of a liquid crystal display.

FIELD-EFFECT CELL STRUCTURE

A field-effect liquid crystal cell consists of two glass plates, each with a transparent conductive coating, between which the liquid crystal material is sandwiched *(Figure 1)*. A thin film of indium oxide — a transparent electrical conductor — is deposited on the top, or front, glass plate. This oxide is patterned to produce a series of 7-segment characters. Each segment has a lead that extends to the long edge of the glass. The bottom, or back, glass plate also has an indium oxide coating, but the pattern is designed as a common electrode that, when the plates are fused, registers to the top glass pattern. The oxide-coated side of both the top and bottom glass plates is entirely covered by an evaporated layer of silicon monoxide dielectric, which produces the desired alignment of the liquid crystal molecules.

After the conductive and dielectric coatings have been applied, the top and bottom plates are fused to within 0.0005 inch by a glass ring that has a 0.05-inch opening on one side. Both plates have a strip of solderable metal — gold over copper over chrome — on the side with the opening. This opening is used to introduce the liquid crystal material into the display envelope, after which the metal strips are soldered to seal the opening.

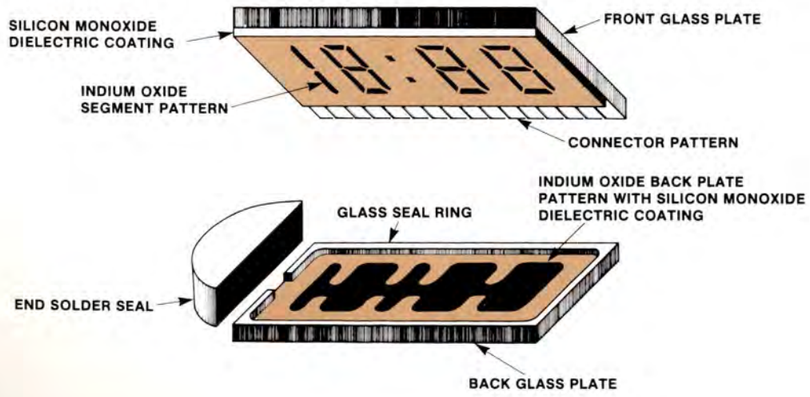


Fig. 1 Field-Effect Cell Structure

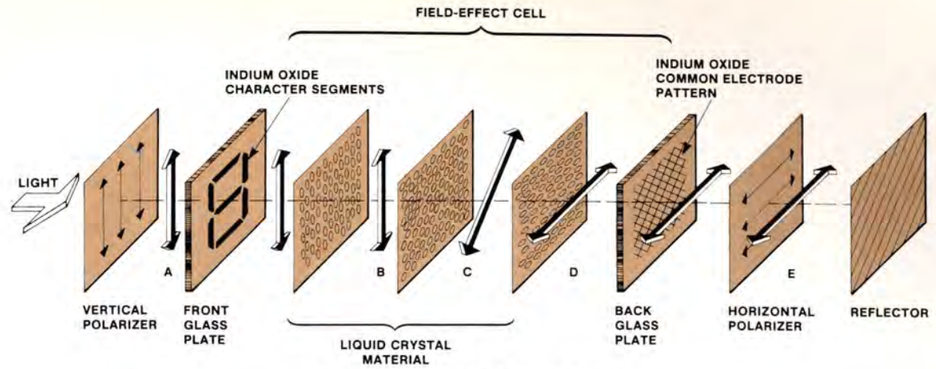


Fig. 2 Unenergized Reflective LCD

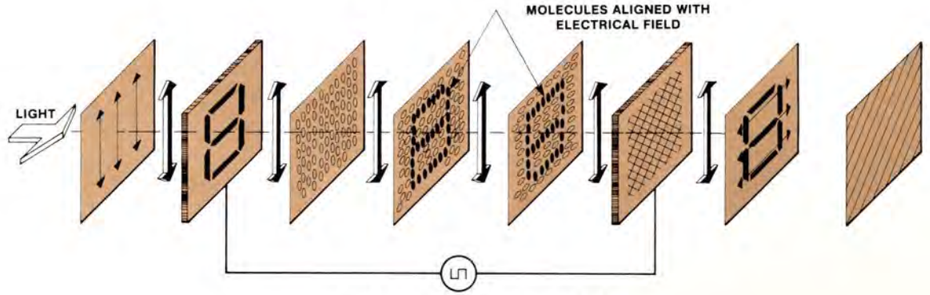


Fig. 3 Energized Reflective LCD

REFLECTIVE LCD OPERATION

A reflective LCD consists of a vertical polarizer, liquid crystal field-effect cell, horizontal polarizer, and reflector *(Figure 2)*. With no voltage applied, the treatment of the liquid crystal cell plates produces a uniform alignment of the crystal molecules. If the front and back plates are mounted at right angles to one another — according to the way in which the crystal molecules line up — a 90-degree rotation, or twist, of the alignment occurs. Vertically polarized light entering the front of the cell (A) follows the rotation of the crystal alignment as it passes through the cell (B, C, D). Having been rotated 90 degrees, the polarized light passes through the horizontal polarizer to the reflector (E). The light is then returned through the cell, again rotating 90 degrees, and passes out of the LCD through the vertical polarizer.

When voltage is applied across one or more of the character segments *(Figure 3)*, the crystal molecules in the area of the segments align themselves with the electrical field. Rotation therefore does not occur in the region of the energized pattern elements. The vertically polarized light conforming to the image produced by these elements cannot pass through the horizontal polarizer but is, rather, absorbed by it. The energized display elements therefore appear as black images against a light background.

TRANSMISSIVE LCD OPERATION

A transmissive LCD consists of a vertical polarizer, field-effect cell, horizontal polarizer, and light source. The light source, which may be of any suitable type, is in the same position as the reflector in a reflective display.

With no voltage applied to the cell, light from the source passes through the horizontal polarizer, is twisted by the cell, and passes out of the LCD through the vertical polarizer at the front of the display. When voltage is applied to the cell, the twist is destroyed in the region of the energized pattern segments. The horizontally polarized light emitted by the source is absorbed by the vertical polarizer, forming the black-on-white image of the energized pattern segments.

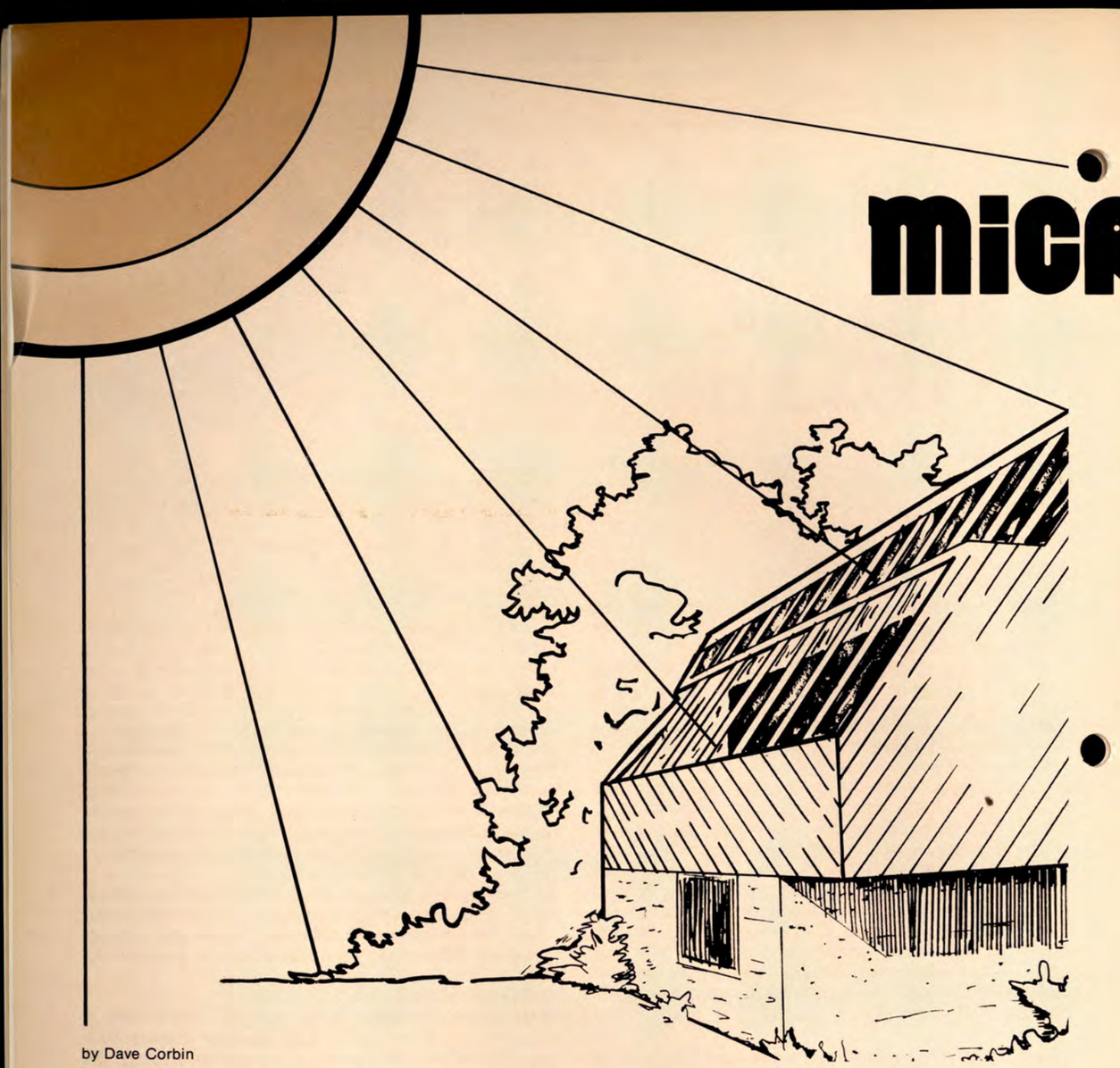
A white-on-black effect can be achieved by using two horizontal (or two vertical) polarizers. In this case, light in the area of the energized pattern elements passes through both polarizers while light in the surrounding area is absorbed.

FAIRCHILD LCDs

Fairchild has entered the LCD market with a line of 3 1/2-, 5 1/2-, and 6-digit watch and 8-digit calculator displays. Supported by a major investment in production capacity, the LCD product range will continue to expand as customer needs and desires are identified. □

Device No.	Description	Digit Height (mm)	
		Hour and Minute	Second
FLC3503-1	Lady's 3-1/2 digit	3.3	
FLC3505-1	Man's 3-1/2 digit	4.6	
FLC3505-2	Man's 3-1/2 digit	5.1	
FLC3507-1	Man's 3-1/2 digit	6.7	
FLC5505-1	Man's 5-1/2 digit	5.1	3.6
FLC5505-3	Man's 5-1/2 digit	5.3	3.8
FLC6005-2	Man's 6-digit	4.6	3.1
FLC6005-3	Man's 6-digit	4.5	3.1
FLC8004-1	8-digit calculator	3.5	
FLC8006-1	8-digit calculator	6.0	

MICROPROCESSOR-BASED SOLAR CONTROLLER



by Dave Corbin

Energy is being consumed today in greater quantities than ever; at the same time, yesterday's seemingly unlimited resources are now seen to be quite finite. As a result, energy conservation has assumed a new importance, and the search for alternative energy sources has begun in earnest. One of the more promising possibilities is harnessing the sun as a direct source of heat.

The solar heating systems now being installed in homes, apartment complexes, and businesses contain heat collecting and storing devices from which resources are drawn during non- and low-sunlight periods. Although there are many types of such systems, the most common circulate water or some other liquid through solar heating panels, or collectors, during the day and store the heated fluid in tanks. When required, this fluid is pumped through radiators or radiant coils to provide area heating. To maintain comfort and make the best use of the available energy, the user must continuously monitor the temperature of every area to be heated, as well as the temperatures of the collectors and the storage tanks. Valves must then be opened or closed and pumps turned on or off to maintain the desired relationship among the system components. A computerized energy mangement system, or solar controller, can perform all of the monitor and control functions with optimum efficiency.

A microprocessor-based solar controller designed by Fairchild for Rho Sigma, Inc., a major manufacturer of solar controls, is specifically intended to accept the low voltages produced by thermistor temperature sensors, process and display the data, and provide outputs for relay and switch opening and closing. The solar controller contains a single-board F8™ microprocessor, two input and two output cards, an A/D converter control card, a display control card, two 4K EPROM program storage cards, and a 1K RAM and memory address card *(Figure 1)*.

Also included in the unit are an A/D converter, a 5-digit LED display, and a 16-key keyboard. The display automatically sequences through all input channels, displaying the number and temperature of each channel for one second before cycling to the next. The keyboard can be used to halt this sequencing and either make the display continuously monitor only one channel or convert it to a clock-only display that shows time of day.

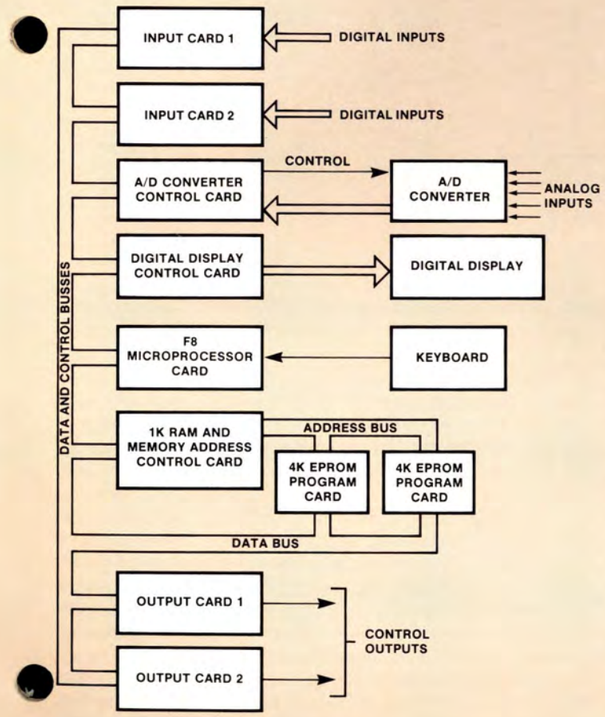


Fig. 1 Solar Controller Functional Block Diagram

CONTROLLER OPERATION

The microprocessor is programmed to solve a set of logic/arithmetic equations. These equations are contained in the EPROM program storage, with the associated constants being held in the 1K RAM. The keyboard can be used to change a number of the equation constants, permitting system changes to be made without hardware modification.

In normal operation, the A/D converter receives analog temperature information from as many as 16 thermistors and presents the converted data to the microprocessor. Digital data, such as that produced by switch closures and teletype signals, can be presented directly to the microprocessor through the 16 digital inputs of the input cards. These data are used to solve the system functional equations and produce two types of microprocessor outputs.

In the channel-monitor modes, temperature information is output to the display in degrees Fahrenheit or Celsius, depending upon resident program. In the time-display mode, a timekeeping routine program assumes control of the display circuitry and the temperature information is not provided.

The other microprocessor output consists of control signals that are suitable for opening and closing relays and activating solid state switches. These signals perform such functions as turning on pumps and opening valves to let water run into the storage tank or circulate through radiators.

Since program storage is in ROM, power failure does not cause catastrophic loss of memory. When power is restored, a resetting sequence begins, with the controller ensuring that all valves and controls are turned off so that stored energy is not lost. The controller then cycles through all of the inputs, decides what the system operating conditions should be, and generates the necessary output signals. This analysis takes approximately five seconds. To indicate to the user that power has been off, the display flashes until manually reset.

Originally designed for use in solar heating applications, the intelligent microprocessor-based controller is applicable to any system in which the ability to deal with multiple sensor inputs and generate control outputs is required. □

CIRCUIT IDEAS Digital

by Charles Alford

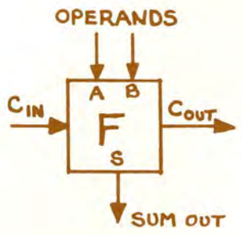


Fig.1 Full Adder Symbol

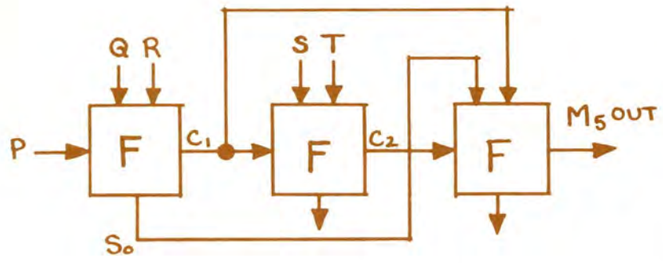
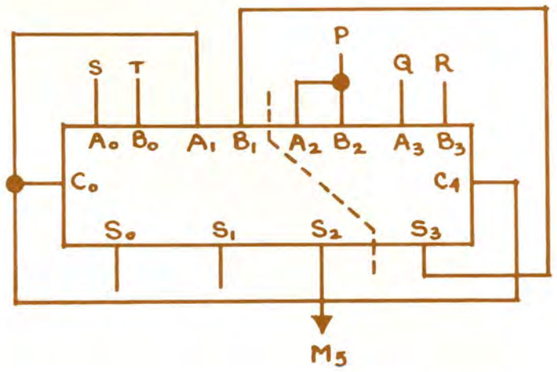


Fig. 2 5-Input Majority Function



4-bit Adders

Family	Part No.
TTL	7483
LS-TTL	LS83
LS-TTL	LS283
CMOS	40283

Fig.3 Implementing the 5-input Majority Function with a 4-bit Adder

4-BIT ADDER SERVES AS 5-INPUT MAJORITY GATE

A majority gate is one whose output is True if a majority of its inputs are True, a function also known as voting logic. A full adder *(Figure 1)* acts as a 3-input majority gate since the C_{OUT} is True if any two or all three of the inputs are True.

To obtain a 5-input majority function, as shown in *Figure 2*, inputs P, Q and R are combined in the first adder. Inputs S and T are applied to the second adder, along with the carry C_1 from the first adder. Note that the carry C_2 from the second adder is not sufficient indication that a majority of the inputs are True, since it will be True if only S and T are True but will be False if only P, Q and R are True. But if any two or all three of S_0, C_1 and C_2 are True, then it must be that three or more of the inputs are True. Thus the third adder is used a majority gate for S_0, C_1 and C_2.

A slight dilemma occurs in trying to implement *Figure 2* with one MSI package since there is no triple adder available, and in the 4-bit adder only one carry is brought out of the package whereas access to two carries is needed. The dilemma is solved by using one adder of the 4-bit circuit as an input and an output that are effectively independent of each other, as shown in *Figure 3*. Input function P connects to both operand inputs of the third adder, which means that its C_{OUT} is always equal to P and is independent of its C_{IN}. Thus the function of the first adder in *Figure 2* is performed by the fourth adder in *Figure 3*, whose C_{OUT} is available. The functions of the second and third adders of *Figure 2* are performed by the first and second adders of *Figure 3*. The C_{OUT} of this second adder passes through to the Sum output of the third adder to provide the final output. □

CCD COMB FILTERS FOR TELEVISION RECEIVERS

by Steve Barton

In an NTSC color television receiver, the method and degree of separation of the luminance (brightness) and chrominance (color) information in the detected video signal have a considerable effect on the quality of the displayed picture.

The standard technique for processing the luminance component of the NTSC video signal *(Figure 1a)* is to place a trap circuit, tuned to the color subcarrier frequency, in the luminance channel. The trap removes most of the chrominance signal components and shapes the frequency response of the luminance channel to produce an overall low-pass filter response *(Figure 1b)*.

Conventional chrominance signal processing circuitry is designed with a band-pass response of from 3.1 to 4.1 MHz *(Figure 1c)* so that luminance signal components below 3.1 MHz are not accepted by the chrominance channel. The chrominance signal is thus treated as a double-sideband signal with a maximum modulating frequency of 500 kHz.

TRAP/BAND-PASS DISADVANTAGES

In the luminance channel, the presence of the 3.58-MHz trap causes a number of problems. For example, luminance signal frequencies above approximately 3 MHz are lost, reducing the horizontal resolution of the displayed picture. At the same time, the trap has virtually no rejection of the I-signal component of the chrominance signal below 3.1 MHz; the chrominance signal sidebands not rejected by the trap interfere with the luminance in areas of fine color detail. The worst effect produced by the trap circuit is ringing on the vertical edges of the displayed picture, which is partly responsible for dot crawl on the vertical edges. Ringing is worst on a transition between areas of highly saturated colors with different hues and brightness levels. On such a transition, step changes in color subcarrier amplitude and phase, and in luminance signal amplitude, occur and tend to excite the 3.58-MHz trap.

Although it rejects luminance signal components below 3.1 MHz, the chrominance circuitry does accept luminance signals in the 3.1- to 4.1-MHz region of the spectrum, causing a "cross-color" effect in areas of the picture having fine luminance detail. The band-pass nature of this circuitry also keeps the full bandwidth of the I-signal chrominance component from being used, which reduces the amount of horizontal color resolution possible.

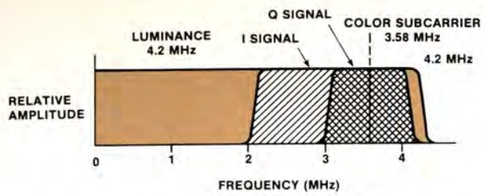


Fig. 1a Spectrum of NTSC Video Signal

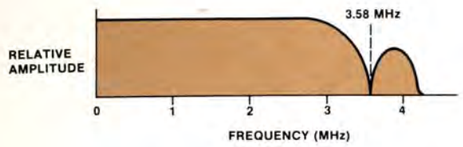


Fig. 1b Overall Frequency Response of Luminance Channel

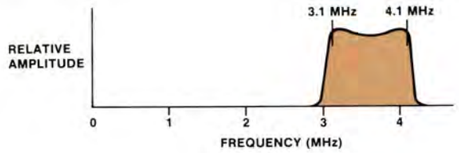


Fig. 1c Overall Frequency Response of Chrominance Channel

These problems arise largely because the conventional trap/band-pass separation technique processes the luminance and chrominance signals as though they possess continuous spectra and makes no use of the frequency interleaving of these signals in the NTSC system.

FREQUENCY INTERLEAVING

In an NTSC-encoded composite video signal, frequency interleaving is the result of energy distribution characteristics. The spectral energy of the luminance signal in a vertically correlated television picture (no change from line to line) is clustered around harmonics of the horizonal scanning frequency (f_h), with very little energy between the harmonics. The chrominance sidebands are spaced at multiples of f_h away from the color subcarrier frequency, which in the NTSC system is at 227.5 f_h, or midway between two of the harmonics of f_h. The spectra of the luminance and chrominance signals are thus interleaved *(Figure 2)*.

An ideal device for separating the luminance signal from the composite video signal is a filter with a frequency response that matches the spectral distribution of luminance energy across the luminance signal bandwidth. Similarly, the chrominance signal can be separated by a filter with a response that matches the spectral distribution of chrominance sidebands across the chrominance bandwidth. The frequency response of both these filters contains a large number of pass-bands spaced at intervals of f_h, with a stop-band midway between each adjacent pair of pass-bands. Because this response resembles the teeth of a comb, the filters are generally referred to as "comb" filters.

BASIC COMB FILTERS

A basic comb filter to perform luminance and chrominance signal separation consists of a time delay element and two summation networks that combine direct and delayed signals *(Figure 3)*. If the delay time (T) is equal to the horizontal scanning period ($1/f_h$), the filter transfer function to the luminance output is maximum at multiples of f_h and the transfer function to the chrominance output is minimum at multiples of f_h *(Figure 4)*.

The combed luminance output signal represents the sum of the picture content of successive scanning lines. Since the color subcarrier frequency is an odd harmonic of $f_h/2$, the color subcarrier phase changes by 180 degrees between corresponding points on successive scanning lines. The chrominance signals therefore cancel when the lines are summed, leaving only the luminance signal.

The combed chrominance output signal represents the difference in picture content between successive scanning lines. In a vertically correlated picture, the luminance signal is the same on successive scanning lines, so luminance cancellation occurs when the difference is taken. Because of the 180-degree phase change of the color subcarrier from line to line, the combed chrominance signal remains.

The physical effect of the filter is that each line in the displayed television picture is the average of the corresponding transmitted line and the previously transmitted line in the same field.

A comb filter for luminance and chrominance signal separation can be realized using as a time delay element a device that provides a non-dispersive delay of exactly one horizontal scanning period (1H). A glass block delay, which employs acoustic-wave propagation, has been used in the past for this purpose. The charge-coupled device (CCD) analog shift register, however, lends itself readily to such delay applications and has, in addition, marked advantages over the glass block.

For example, glass-block insertion loss is typically greater than 6 dB, while the CCD has 0 dB insertion loss. Similarly, the CCD has high input and low output impedances, which simplifies matching; the input and output impedances of the glass block, in contrast, change with frequency. The CCD can also handle the full 4.2-MHz NTSC video signal bandwidth, but the glass block cannot pass the full bandwidth unless the signal is modulated onto an rf carrier.

The delay time of the glass is dependent, to some extent, upon temperature, and there is a long-term aging effect on the delay time. The delay time of the CCD shift register is dependent upon the clock frequency, which can be referenced to the color subcarrier by using a phase-locked loop to produce a high degree of accuracy. An additional advantage of the CCD is that it is packaged in a 16-pin DIP and is, therefore, considerably smaller than the glass block.

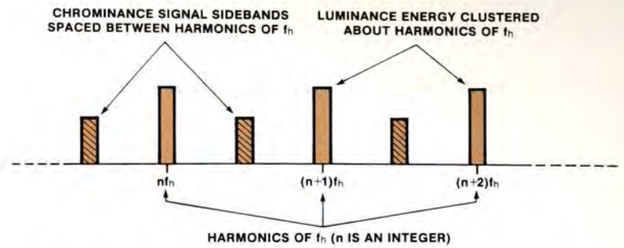


Fig. 2 Interleaving of Luminance and Chrominance Signal Spectra

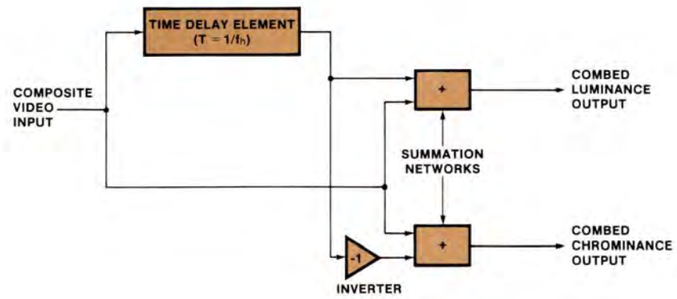


Fig. 3 Basic Comb Filter

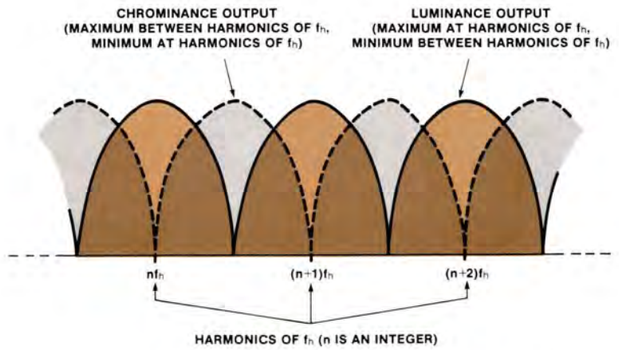


Fig. 4 Transfer Functions for Basic Comb Filter

REALIZATION OF A CCD COMB FILTER

A practical CCD comb filter, intended specifically for NTSC television applications, can be constructed using the CCD-321A shift register as the time delay element. The CCD321A is a 910-bit analog shift register that provides a delay of exactly 1H when driven by a clock signal of four times the color subcarrier frequency.

In this CCD comb filter *(Figure 5)*, a 14.3-MHz (four times the NTSC color subcarrier frequency) crystal-controlled oscillator is the source of clock signals for the clock drivers that supply the CCD shift register with two-phase clock signals. With an NTSC composite video signal at the system input, the input attenuator gives a video signal amplitude of 400 mV peak-to-peak at the input of the CCD321A delay element. The low-pass filter removes the 14.3-MHz clock component from the CCD output signal. The delayed and filtered composite signal is fed to a phase splitter, which supplies anti-phase delayed signals to the two summation networks. Each summation network is also supplied with a direct video signal through the variable attenuators. In practice, the functions of the summation networks and output buffers are performed by two video operational amplifiers, resulting in better combing action over a wider frequency range than is possible with circuits using discrete components.

The upper frequency limit of combing is determined by the frequency response of the low-pass filter and the CCD delay element, the output of which starts to fall off as the signal frequency approaches half the clock frequency. The lower limit of combing is determined by the value of the coupling capacitors used in the system; these are made large enough so that the time constants are equal to several vertical scanning periods.

VERTICAL RESOLUTION IMPROVEMENT

The comb filter provides optimum luminance and chrominance signal separation in a vertically correlated television picture. In practice, however, television pictures are often not vertically correlated. Luminance spectral energy in such a picture is present at frequencies between harmonics of f_h. Removal of this energy by the comb filter results in loss of vertical resolution and its attendant problems. There are two basic techniques for solving these problems.

The first technique removes as little of the luminance information from between harmonics as possible. This is accomplished by restricting combing to those portions of the spectrum in which luminance and chrominance signal interleaving occurs. Addition of a band-pass filter to the comb filter *(Figure 6)* restricts combing to the range of frequencies containing the color subcarrier sidebands. This filter has a pass-band of from approximately 2.1 to 4.1 MHz if the entire chrominance signal bandwidth is used. Its pass-band is from approximately 3.1 to 4.1 MHz if the chrominance signal is treated as a double-sideband signal.

The second technique provides combing across the full video bandwidth, but adds a signal containing some of the luminance information removed by combing. To implement this technique, the combed chrominance of the basic comb filter is passed through a 2-MHz low-pass filter to remove the chrominance information *(Figure 7)*. The resulting signal is added to the combed luminance signal. The net effect for the luminance signal is that combing occurs only above 2 MHz. The low-pass filter output represents changes in picture content in the vertical direction; this is used as a "detail signal" to improve vertical resolution.

The CCD321A can be used as a delay element to construct an efficient, economical comb filter that performs more than adequate separation of luminance and chrominance in an NTSC television receiver. Such a filter is the first that is low enough in cost to be acceptable for receiver, as well as broadcast and professional, applications. The use of the comb filter does produce a loss in vertical color resolution, but the improvements in displayed picture quality — particularly on vertical edges — more than compensate for the degradations on horizontal edges, and vertical resolution correction can be readily provided. □

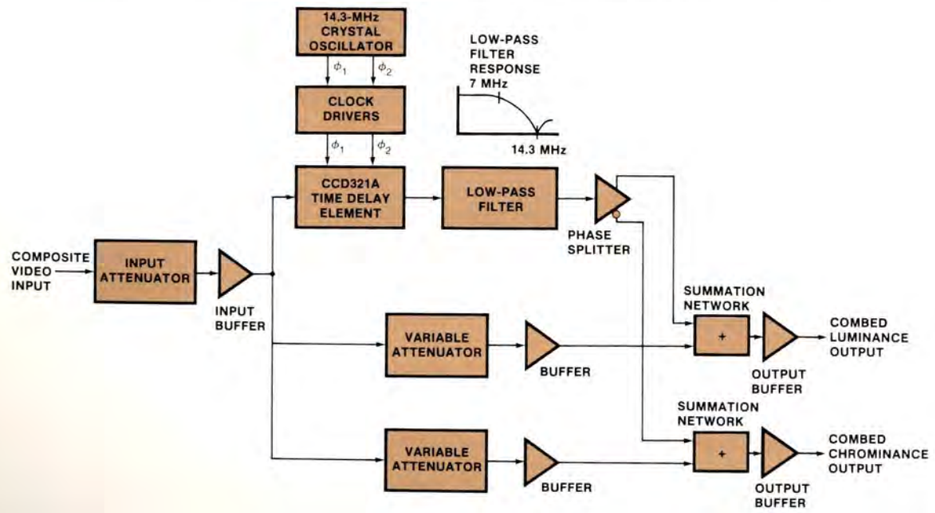


Fig. 5 Functional Block Diagram of Practical CCD Comb Filter

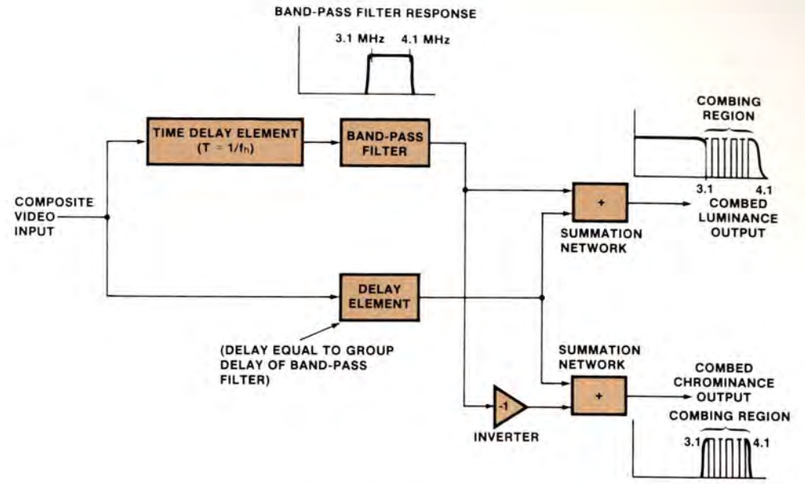


Fig. 6 Comb Filter with Restricted Combing Bandwidth

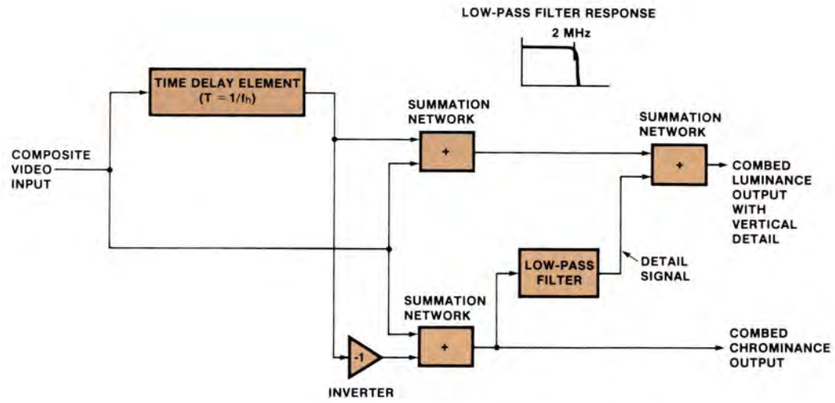


Fig. 7 Comb Filter with Addition of Detail Signal

NEW PRODUCTS

F8 AND F3870 DEVELOPMENT SYSTEMS NOW HAVE FLOPPY DISK OPTIONS

The F8-DOS-III floppy disk operating system provides a bulk storage capability for the Formulator™ Mark II and Mark III microcomputer development systems. It supports up to four iCOM® floppy disk drives, yielding over one megabyte of total storage capacity, and functions as a fast, convenient, reliable, and extremely efficient facility for auxiliary program and data storage during F8 and F3870 software development.

With batch operation, linking loader, relocating assembler, editor, and real time debugger features, the F8-DOS-III is the most powerful and complete development software package available for F8 and F3870 development. For information contact:

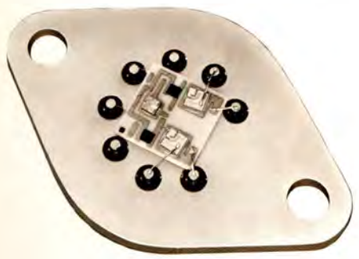
Carlo Bruno
Fairchild Instrumentation Systems Group
1725 Technology Drive
San Jose, California 95110
Phone: (408) 998-0123 ext. 434



Floppy Disk System with Associated Equipment

VERSATILE DUAL HIGH-CURRENT HAMMER DRIVER AVAILABLE

Capable of driving two 5 A loads at a 110% duty cycle, the new SH3011 dual 5 A driver is ideal for use in a wide range of applications, including matrix-impact printers and high-current solenoids and relays. The high-density SH3011 hybrid package contains two drivers, each producing a 5 A output, that have a high voltage (80 V) capability. The inputs are TTL compatible and the outputs are completely separate.



High-Current Hammer Driver

D/A CONVERTER USES PULSE WIDTH RATIO TECHNIQUE

The μA9706 D/A output interface circuit is a monolithic digital-to-analog converter using a pulse width ratio conversion technique. This CMOS integrated circuit accepts a serial digital input word and continuously outputs eight independent pulse streams, or channels. Each of these pulse-width-ratioed streams can, when filtered, provide 64 discrete analog levels. When two channels are properly summed, 4096 analog levels can be provided with 12-bit precision.

The μA9706 features an internal memory, excellent stability that requires no adjustment, and CMOS technology. The 14-pin package is powered by a single +5 V supply, making it ideal for such applications as remote control television and audio systems, remote control models and games, and all types of microprocessor control systems.

MOTOR SPEED CONTROL HAS UNEXCELLED ACCURACY

The μA7392 dc motor speed control is designed for precision, closed-loop motor speed control systems, such as those used for capstan drive motors in automotive and portable tape players. It compares actual motor speed to an externally presettable reference voltage, with motor speed being determined by frequency-to-voltage conversion of the input provided by a tachometer generator. The result of the comparison controls the motor speed through the system negative feedback loop, which affords the excellent speed control accuracy.

Thermal and over-voltage shutdown are included for self-protection, and a "stall-down" feature protects the motor from burn-out during extended mechanical jams.

In addition to such low-current applications as tape player capstan motors, the μA7392 is designed so that the emitter of its output stage is available to drive directly into a power transistor or power Darlington transistor for very high current applications.

For current requirements between these two extremes, the μA7391 without an external power transistor may be used instead of the μA7392.

ANALOG SHIFT REGISTER REDESIGNED

The CCD321A is a redesigned version of the CCD321 analog shift register. The purpose of the redesign was to improve device signal-to-noise ratio and input stage linearity, optimize audio performance, and reduce clock high levels to below 15 V. With only a few simple dc adjustments, the CCD321 and CCD321A are pin-for-pin compatible.

The CCD321A-1 and CCD321A-2 are high-quality video delay lines with excellent linearity and signal-to-noise ratio for high-quality broadcast applications. They replace the standard glass delay lines in such types of video processing as time-base correction, comb filtering, drop-out compensation, signal-to-noise enhancement, and vertical aperture correction. Among the advantages the CCD321A has over glass delay lines are 0-dB insertion loss, high input and output impedances, and clock-dependent fixed delay.

The CCD321A-3 is intended primarily for use in time-base compression and expansion systems, eliminating the need for large memories and relatively expensive high-speed A/D and D/A converters. Typical applications are recording and processing high-bandwidth, high-speed transient phenomena, high-speed analog data acquisition, and correction of time-base errors for video tape recorders.

The CCD321A-4 is available for use in providing basic delay of audio bandwidth signals. As an audio delay line, it is ideal for guitar amplifiers, fuzz boxes, reverberation and echo effect chambers, and other special-purpose audio applications.

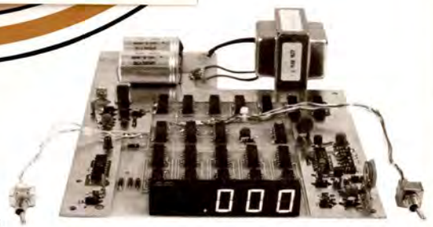
Tear

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cies up to 500 MHz. The measured frequency is displayed on five 1/2-inch LED digits with overflow indicated in the upper right corner of the display.



The FTK0130 has two ranges — MHz and kHz — both of which use the full 5-digit display. By setting the input-select switch to select the high-frequency input, the decimal point is automatically shifted to the right to display frequencies between 99.999 and 499.99 MHz. High frequencies are measured using the 50 Ω input, which has a typical sensitivity of 100 mV and an input capacitance of 10 pF. Lower frequencies are measured via a high-impedance input that also makes the FTK0130 useful in higher impedance applications. This input has a 1 MΩ impedance with a parallel capacitance of 20 pF.

An experienced kit builder can assemble the FTK0130 in two evenings. An optional metal case with pre-drilled holes and a silk-screened front panel is also available. The FTK0130 operates from 110 Vac, 60 Hz power.



The FTK0130 frequency counter marks the beginning of a family of test instruments to be introduced by the Solid State Technology Kit department. Previously introduced were an automobile calendar clock, a calendar clock with a radio-alarm feature, and a 6-digit wall calendar clock. These kits are complemented by a full line of components from virtually all divisions of Fairchild. For more information, contact your local representative for dealer locations, or write Solid State Kit Marketing, Department 30-701, 4001 Miranda Avenue, Palo Alto, CA 94304.

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bugger features, the F8-DOS-III is th
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VERSATILE DUAL HIGH-CURRENT HAMMER DRIVER AVAILABLE
Capable of driving two 5 A loads at a 110% duty cycle, the new SH3011 dual 5 A driver is ideal for use in a wide range of applications, including matrix-impact printers and high-current solenoids and relays. The high-density SH3011 hybrid package contains two drivers, each producing a 5 A output, that have a high voltage (80 V) capability. The inputs are TTL compatible and the outputs are completely separate.



High-Current Hammer Driver

D/A CONVERTER USES PULSE WIDTH RATIO TECHNIQUE
The μA9706 D/A output interface circuit is a monolithic digital-to-analog converter using a pulse width ratio conversion technique. This CMOS integrated circuit accepts a serial digital input word and continuously outputs eight independent pulse streams, or channels. Each of these pulse-width-ratioed streams can, when filtered, excellent stability that requires no adjustment, and CMOS technology. The 14-pin package is powered by a single +5 V supply, making it ideal for such applications as remote control television and audio systems, remote control models and games, and all types of microprocessor control systems.

MOTOR SPEED CONTROL HAS UNEXCELLED ACCURACY
The μA7392 dc motor speed control is designed for precision, closed-loop motor speed control systems, such as those used for capstan drive motors in automotive and portable tape players. It compares actual motor speed to an externally presettable reference voltage, with motor speed being determined by frequency-to-voltage conversion of the input provided by a tachometer generator. The result of the comparison controls the motor speed through the system negative feedback loop, which affords the excellent speed control accuracy.

Thermal and over-voltage shutdown are included for self-protection, and a "stall-down" feature protects the motor from burn-out during extended mechanical jams.

In addition to such low-current applications as tape player capstan motors, the μA7392 is designed so that the emitter of its output stage is available to drive directly into a power transistor or power Darlington transistor for very high current applications.

For current requirements between these two extremes, the μA7391 without an external power transistor may be used instead of the μA7392.

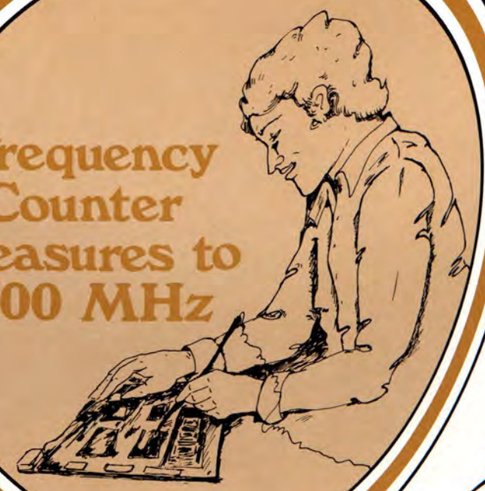
optimize audio performance, and reduce clock high levels to below 15 V. With only a few simple dc adjustments, the CCD321 and CCD321A are pin-for-pin compatible.

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Frequency Counter Measures to 500 MHz



The FTK0130 frequency counter, part of Fairchild's Solid State Technology Kit™ line, measures frequencies up to 500 MHz. The measured frequency is displayed on five 1/2-inch LED digits with overflow indicated in the upper right corner of the display.



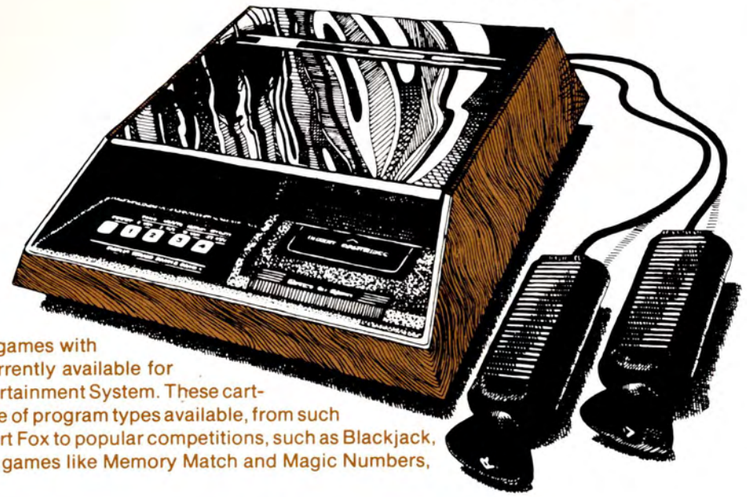
The FTK0130 has two ranges — MHz and kHz — both of which use the full 5-digit display. By setting the input-select switch to select the high-frequency input, the decimal point is automatically shifted to the right to display frequencies between 99.999 and 499.99 MHz. High frequencies are measured using the 50 Ω input, which has a typical sensitivity of 100 mV and an input capacitance of 10 pF. Lower frequencies are measured via a high-impedance input that also makes the FTK0130 useful in higher impedance applications. This input has a 1 MΩ impedance with a parallel capacitance of 20 pF.

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CHANNEL F™

FAIRCHILD VIDEO ENTERTAINMENT SYSTEM



Seventeen Videocart™ interactive game cartridges — comprising 30 games with more than 500 variations — are currently available for the Fairchild Channel F Video Entertainment System. These cartridges represent the broadest range of program types available, from such combat games as Spitfire and Desert Fox to popular competitions, such as Blackjack, Baseball, and Backgammon, mind games like Memory Match and Magic Numbers, and educational math programs.

Major Channel F components are a game console, a pair of eight-way hand controls, an adaptor box, and the optional Videocart game cartridges. The adaptor is essentially an interface that permits a player to switch easily from normal television to game play, or *vice versa*. The action of the hand controls depends upon the game being played, but the full range of operation encompasses vertical, horizontal, and diagonal motion, and clockwise and counterclockwise rotation, of the mobile screen elements.

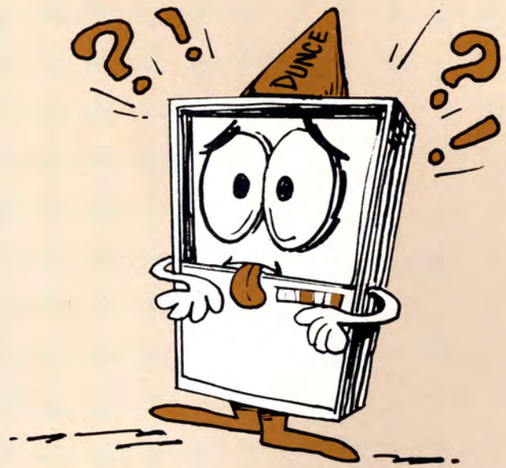
The heart of the system is an F8™ microprocessor. The microprocessor and its associated 16K RAM, which are incorporated into the game console, make the Channel F system the first truly programmable home electronic game center.

Instructions for specific games are retained in ROM program stores. Hockey and tennis instructions are contained in ROMs within the console; program stores for other games are mounted on printed circuit boards within the Videocart cartridges. The information in the ROMs establishes operating parameters for the microprocessor and loads preliminary data into the RAM. Additional transient data are supplied by the five selector control buttons on the console and by the hand controls. Interaction of the ROM, RAM, microprocessor, and controls produces the games on the television screen and allows them to be played.

With a Videocart cartridge inserted into the console (or one of the resident games enabled), the player selects one of four difficulty modes, one of four time limits and, with some cartridges, variations of a particular game. Once the game has begun, the players can "freeze" the action for an indefinite period of time and resume the game where they left off. During the interruption — that is, after the action is "frozen" — the Channel F system can be reprogrammed for a new time limit, difficulty mode, or both, because such transitory information is held in the console RAM.

The Channel F system can be used with any make or size of television set, either color or black-and-white. It has been approved for consumer use by the Federal Communications Commission. The Channel F Video Entertainment System and the Videocart game cartridges are sold through leading retail outlets.





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