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PROGRESS

Switching Regulators Efficiently Control Power Sources



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■ Switching regulators, although somewhat more complex than fixed or adjustable series-pass regulators, offer power-supply designers significant advantages — namely, flexibility and high efficiency. Also, they can be used under a wide range of power conditions, from battery operation to high-power, high-current applications. The feature details these adavantages and explains the device operation modes that include step-up, step-down and inverting — a mode that provides an output of opposite polarity to the input. Several examples of switching-regulator applications are described that require very few external components, including a dual tracking regulator, a combination step-up and series-pass regulator, and a negative input/output regulator. A valuable table of switching regulator design formulae is also included. ■ A coin sorter, discussed in the second article, is a simple example of how to combine the optical sensitivity of the CCD camera with the decision-making capability of the microprocessor. It is intended to illustrate the potential usage of accurate high-speed sorting systems in modern industrial environments. ■ The circuit idea this month offers a solution for dividing an incoming frequency by an odd number, yet producing an output that has a 50% duty cycle. ■ Put a nichrome-link PROM in a plastic package and moisture penetration becomes a problem that could eventually cause device failure through corrosion of the nichrome fuses. Silicon-nitride surface glassivation can eliminate this potential problem, but the devices still must be carefully tested to provide good reliability data. Biased Pressure Temperature Humidity (BPTH), described in a short article, proves to be effective. ■ The final article describes the OCM-1, a complete microcomputer on a single board. All that's necessary for most applications is to connect it to a power supply and a teletypewriter. Based on the F8 CPU, the OCM-1 includes a Fairbug™ monitor contained in a PSU, memory, interface circuitry, a clock, a user breadboard area, and I/O lines that are truly bidirectional. Extra sockets are provided for expanding the microcomputer capabilities.

On the Cover
Man has long controlled water power to run his mill. Today, modern power sources still require regulation.



PROGRESS

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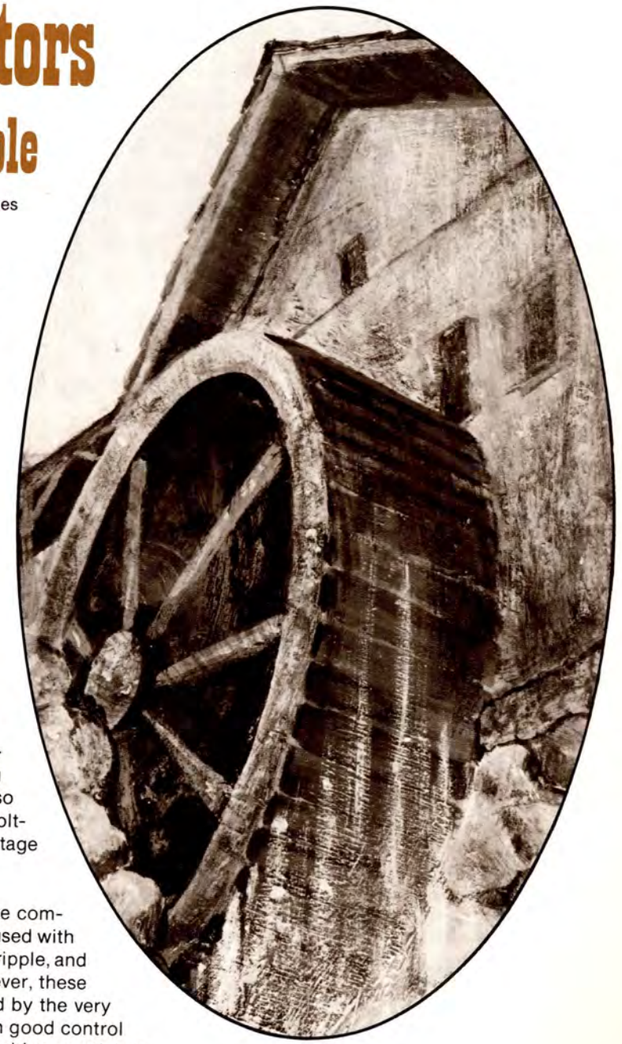
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Switching Regulators
efficient and flexible

by David Jones



THE BACKGROUND

Regulated power supplies are found almost universally in system design. Basically, they consist of some type of network to convert ac input voltages to unregulated dc voltages and a voltage regulator to provide dc voltage regulation. Integrated circuit voltage regulators have been available for about 10 years, evolving from the first industry standard, the μA723. This device had low output currents compared to present devices and required several external components and significant design considerations. It was followed by a series of 3-terminal regulators that provided higher output currents (up to 1 A) with most of the circuitry on the chip but had a limited number of fixed output voltages. The introduction of adjustable 4-terminal regulators solved this output voltage limitation.

Such *series-pass* regulators have dominated the power supply regulator market because they are simple, easy to use, offer high performance, and a wide range of high quality circuits is available from a number of manufacturers. Increasing concern about wasted power has caused designers to seriously consider switching regulators, which are not only much more efficient but also provide output voltages *higher or lower* than the input voltage supplied. In addition, then can provide an output voltage of the *opposite polarity*.

Switching regulators do have some drawbacks. They are complex, require some external components, and should be used with some degree of care. They generate noise and an output ripple, and are slower to respond to transient load conditions. However, these disadvantages can be minimized and are overshadowed by the very high efficiency (up to 90%) of switching regulators. With good control electronics, attention to timing, and some filtering, switching regulators can be used in power supply designs that provide lower operating costs and reduce power dissipation. A new integrated circuit switching regulator subsystem, the μA78S40, makes possible a variety of switching *or* series-pass regulator systems with minimum external parts.

THE CONCEPT

Switching regulators are capable of storing energy and cycling on and off as necessary to supply adequate power to the load. They store energy in inductors and capacitors, which do not dissipate power. (Series-pass regulators apply the input/output differential voltage across a pass transistor, which *does* dissipate power.) Output transistors act as switches with the on/off cycle rate determined by the input/output voltages and the load current. Control circuitry monitors the output voltage and modifies timing to maintain a constant output voltage. While the regulator is off, energy is stored in an output capacitor which averages the current flow to the load. The basic modes of operation provide *increased, decreased, or inverted* voltage at the output from a fixed input voltage.

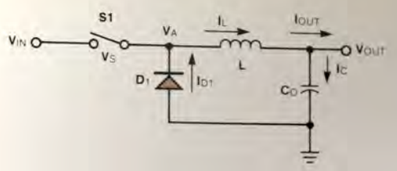


Fig. 1a Step-Down Voltage Regulator

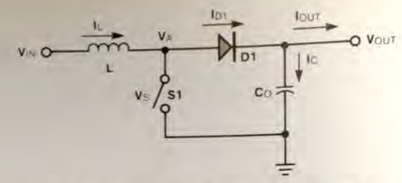


Fig. 1b Step-Up Voltage Regulator

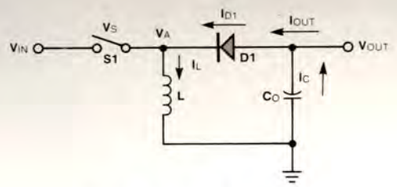


Fig. 1c Voltage Inverter

Figure 1 illustrates the three basic operating modes of a switching regulator. The same basic components — a switch, a diode to direct current, an inductor and a capacitor to store energy — are used for the step-down, step-up, and inverting modes. In a step-down voltage regulator *(Figure 1a)*, when the switch closes, the applied voltage (V_A) rises toward the input voltage, and voltage $V_A - V_{OUT}$ is applied across the inductor, causing current to increase from zero. This current flows to the load/output capacitor. If the instantaneous inductor current is less than the load current, the output capacitor provides additional current causing a slight decrease in the output voltage. If the instantaneous inductor current exceeds the output (load) current, the excess current flows into the output capacitor, increasing the output voltage. The instantaneous inductor current increases continuously until the switch opens. Because the inductor current cannot change instantaneously, when the switch does open V_A drops to $-V_D$ and the diode supplies the inductor current path. At this time, the voltage across the inductor is $-(V_{OUT} + V_D)$; hence the inductor current falls at the rate of $-(V_{OUT} + V_D)/L$ and continues to fall until zero-current is reached or the switch closes again, starting the cycle over.

The on/off cycling of the switch is governed by a control circuit to maintain an average inductor current equal to the output current. The average capacitor current is zero, and the output voltage remains constant. Such control circuits may have an oscillator with on and off timing set so the inductor current will increase to its maximum and then decrease to zero. There is also some type of a sensing circuit for the output voltage that adjusts the oscillator to increase the off time if the output voltage becomes too high. In this type of a system, the maximum output current is 1/2 of the peak value of the inductor current. When the output current is less than this value, the control circuit increases the off-time by an amount adequate to make the average inductor current equal the output current.

Peak current in a step-down regulator is a function of the input, output, and switch voltages, the inductor size, and the amount of time that the switch is on. Similarly, the amount of time required for the inductor current to drop to zero is related to the output, switch, and diode voltages and is the off-time. The ideal on/off-time ratio is a function of the input, output, switch and diode voltages, with the maximum output current being 1/2 of the peak value of the inductor current. The average input current is a function of 1/2 of the peak inductor current and the percentage of time that the switch is on. Regulator efficiency (excluding control circuit current and switching losses) can be expressed as $(V_{OUT}/V_{IN})(V_{IN} + V_O - V_S/V_{OUT} + V_D)$ a function of the input, output, switch, and diode voltages. If the switch and diode voltages can be kept small compared to the input and output voltages, extremely high efficiency is possible. (If the switch and diode voltages were zero, the regulator would be 100% efficient.) Ripple on the output is a function of the peak current, the on/off-time cycling, and the output capacitor. It can be reduced by increasing the output capacitance, which does not affect the other portions of the circuit.

Switching regulators operating in a step-up mode, *Figure 1b*, provide an output voltage *greater* than the input voltage. In the case of a step-up regulator, when the switch closes, the applied voltage drops to almost zero ($V_A = V_S$), and voltage $V_{IN} - V_S$ is applied across the inductor, causing the inductor current to increase linearly. Because the applied voltage is less than the output voltage, the diode is reverse-biased and current cannot flow to the output. Again, when the switch opens, the inductor current cannot change instantly, and the applied voltage changes to the total of the output voltage plus the diode voltage. At this time current can flow through the diode to the load capacitor, and the inductor current decreases at a linear rate, determined by $V_{OUT} + V_D - V_{IN}$. Timing adjustments control the average diode current (I_{D1}) so it is equal to the load current. The diode current can only

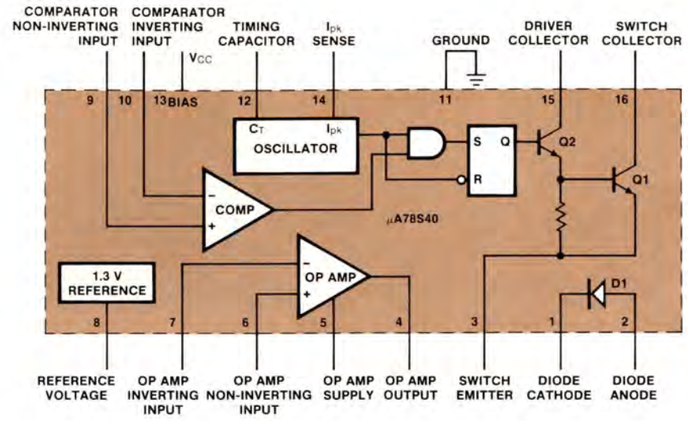


Fig. 2 μA78S40 Universal Regulator Partitioning

flow during off-time, so the maximum output current is $(I_{pk}/2)(t_{off}/t_{on} + t_{off})$. If the load current is less than the maximum output current, off-time is increased by a dead time with no current to the output. Input current can flow during both on and off-times, so the average input current is always greater than the maximum output current.

With a step-up regulator, on-time is a function of the input and switch voltages and inductance; off-time is a function of the input, output, and diode voltages, and inductance. The on/off ratio and the maximum output current are also functions of the circuit voltages, as is the efficiency of the regulator. In the step-up mode, efficiency approaches 100% as the switch and diode voltages become small relative to the input and output voltages, the same as in the step-down mode. Output ripple, a function of peak and output currents, the off-time, and the output capacitance, can also be reduced by increasing the output capacitance without affecting overall regulator performance.

Figure 1c illustrates a basic voltage inverter that generates a negative output from a positive input. Upon closing the switch, the applied voltage $V_{IN} - V_S$ is impressed on the inductor and causes inductor current to increase linearly. When the switch opens, the current cannot change instantaneously so the applied voltage decreases to $(V_{OUT} - V_D)$ which forward biases the diode. The current decays linearly, and the diode current flows to the load with its average value equal to the load current. Since input current only flows when the switch is closed, it is equal to $(I_{pk}/2)(t_{on}/t_{on} + t_{off})$.

Optimum time-on and time-off values for the inverter mode of operation are functions of the input, output, and switch voltages, and inductance. The ratio of on-time to off-time depends only on the voltages. Maximum output current and average input current are always less than 1/2 of the peak current. In the inverter mode, efficiency depends on the input and output voltages and is basically independent of current level. As with the step-up and step-down modes, output ripple can be minimized by increasing output capacitance without affecting regulator performance.

THE REGULATOR

In order to operate effectively in step-down, step-up, and inverting modes, a switching regulator should have several functional building blocks common to all of its operational modes, minimizing the need for external parts and maximizing its versatility. The μA78S40 universal regulator meets this goal and allows a wide variety of regulators to be built with minimum external parts. This regulator's functional blocks are illustrated in *Figure 2* and outlined below.

- A Current-Controlled Oscillator
- A Temperature-Compensated Current-Limiting Circuit
- A Temperature-Compensated Voltage Reference
- An Error Amplifier
- A Power-Switching Circuit
- A High-Gain Amplifier

The current-controlled oscillator has drive circuitry for the transistor power switch. Oscillator frequency is set by an external capacitor so it can be varied according to application. The oscillator duty cycle is internally fixed at 8:1. A current-limiting circuit controls oscillator on-time, adjusting the duty cycle for optimum timing. This temperature-compensated current-limiting circuit senses the switching transistor current across an external resistor and modifies the oscillator on-time, limiting the peak current and protecting the switching transistors.

A 1.3 V temperature-compensated voltage reference source can provide up to 10 mA of current without an external pass transistor. A high-gain differential comparator disables the power switch when the output voltage becomes too high. A

SWITCHING REGULATOR TIMING CONSIDERATIONS

Optimization of regulator on-time and off-time depends on CIRCUIT VARIABLES such as inductance and switch and diode voltages — and on SYSTEM VARIABLES such as input/output voltages. Consider the following conditions and consequences.

- *On-time too short — Inductor peak current isn't high enough, so the maximum output current is reduced. However, efficiency does not suffer.*
- *On-time too long, or off-time too short — Without current limiting, after several cycles the inductor current will exceed the expected peak current and continue to increase, which could lead to excessive current flow and* DEVICE DESTRUCTION.
- *Off-time too long — Inductor current falls to zero and stays there for some time before the switch turns on again. Consequently, average inductor current is less than half of peak current, and the available output current is reduced. However, efficiency does not suffer.*
- *On-time too long — Current limiting for the switch is unacceptable when the inductor current is constant at the peak current, because inductor voltage drops to zero. Therefore, switch voltage increases (to V_{IN} - V_{OUT}), creating a large efficiency loss and possibly DESTROYING the switch.*
- *Off-time too short with on-time adjusted by current limit — No efficiency is lost, but the inductor current does not drop to zero. Therefore, average inductor current is in excess of half of peak current, and the maximum output current exceeds half of the peak current.*

power Darlington switching transistor handles 1.5 A of current and can withstand up to 40 V. The switch collectors and the emitter drive are externally available to allow optimized connection of the switch. A power-switching diode handles 1.5 A of forward current and 40 V of reverse voltage.

The high-gain independent operational amplifier has 150 mA output current capability and a separate positive voltage supply connection. Its input common mode range *includes* ground. It may be connected to provide series-pass regulation or feedback control for switching regulators.

This switching regulator can operate over a wide range of power conditions, from battery power to high-voltage, high-current supplies. Low voltage requirements with minimum current drain make the regulator very useful in battery or 5 V systems. It typically operates from 2.2 to 40 V dc. At the 5 V level, the regulator draws only 2 mA. A low standby-current drain significantly improves regulator efficiency in low-power applications and greatly increases battery lifetime in battery applications. This high efficiency in low-power applications is *not* typical of other switching systems. Combined with the capability of the μA78S40 to handle up to 40 V input and provide as much as 1.5 A switching current, efficient low power operation makes the regulator performance over a wide operating range unmatched.

Using a versatile circuit such as this requires some care, but the benefits are well worth the attention since this IC subsystem provides the user with the flexibility for optimizing power supply performance. A critical parameter is oscillator timing. Although the on-time/off-time ratio is internally fixed at 8:1, the user can adjust this ratio down through the proper selection of peak current, the oscillator capacitor value, the inductor value, and the input/output voltages. Peak current is determined solely by the current-limiting circuit. Selection of the timing capacitor is based on the off-time required. The user should establish the off-time and let the current-limiting circuit modify the on-time. This off-time can be set by the user for either intermittent or continuous operation. For intermittent operation, the user should set the off-time equal to the time required for the inductor current to drop to zero. For continuous operation, the off-time should be set at something less than the time required for the inductor current to drop to zero. When operated in the continuous mode, average inductor current exceeds 1/2 of the peak current, making more power available at the output. However, timing is very critical *(See Box)*, and if on-time and off-time periods are too short, switching losses can significantly reduce efficiency. With this regulator, on-time and off-time should be kept greater than 10 μs.

Switching is accomplished by a Darlington pair with the switch emitter as well as both transistor collectors available for external connection. Either the collector inputs or the emitter output can be used. If the emitter output is used, the collector inputs can be shorted, resulting in a switch voltage of 1.6 V typical. If the collector inputs are used with the emitter grounded, the user must consider the performance tradeoffs between shorting both collectors or using the switch output. System performance is affected by the input and output voltages, the output current, and the expected variations of the input voltage. If both collectors are shorted, there is no switching loss due to base current (switch voltage is typically 1.1 V). If the switch output is used, base drive through the driver is provided by connecting an external resistor to the input voltage line (switching voltage is typically 0.5 V). A switching diode in the circuit is capable of handling voltage up to 40 V and current up to 1.5 A for both step-up and step-down modes. To use the regulator for inverting applications, an external diode is required because the diode voltage drops below the circuit common.

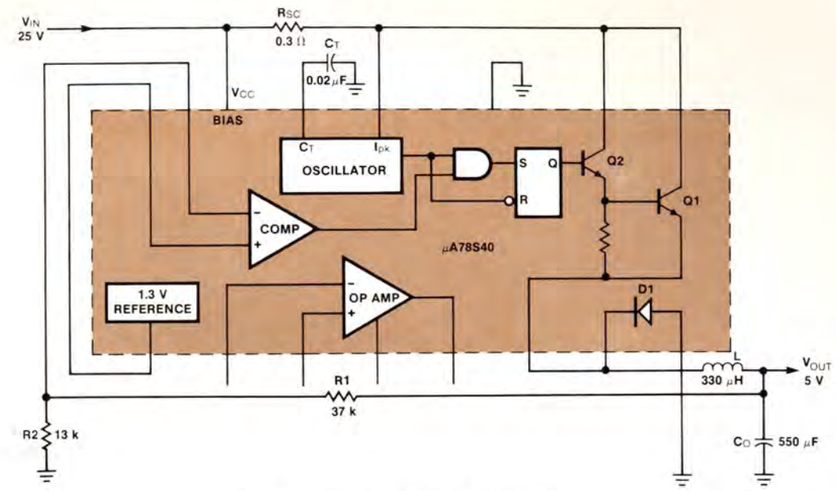


Fig. 3 Step-Down Voltage Regulator

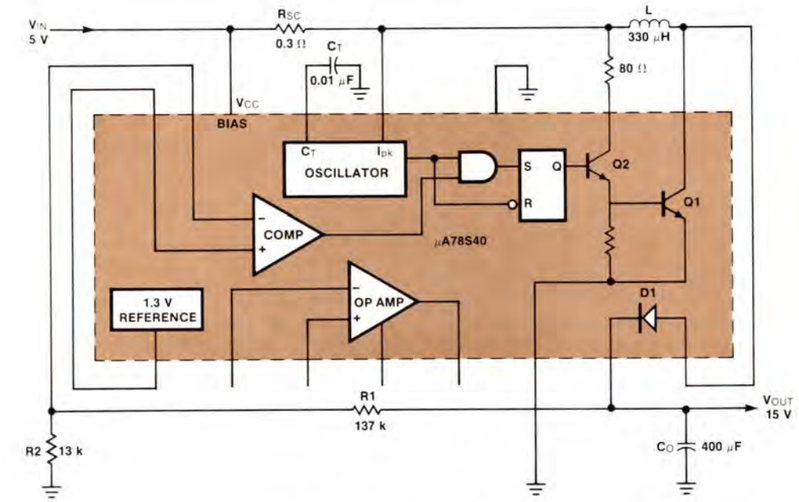


Fig. 4 Step-Up Voltage Regulator

THE APPLICATIONS

Typical applications of the universal regulator include the three switching regulator modes previously discussed; step-down, step-up, and inverting. *Figure 3* illustrates the necessary connections for using the μA78S40 in the step-down mode. This version satisfies a requirement for a 5 V output at 500 mA with output ripple less than 25 mV. In this application, the power switch (Q1 and Q2) is connected between the +25 V supply and the inductor. Switch voltage is determined by the emitter output limit of 1.6 V. For this value, off-time is approximately three times the on-time. Considering that the on-time should be greater than 10 μs, off-time is set by the user at 60 μs (C_T = 0.02 μF), and the inductor value is selected at 330 μH. The output voltage is set by resistors R1 and R2. Output capacitance is calculated to be 400 μF. The circuit standby power is less than 50 mW. Efficiency at full load is 79%; at 10% of full load it is 70%.

For operation as a step-up voltage regulator, the μA78S40 is connected as shown in *Figure 4*. In this case, the objective is to use a 5 V input and get a 15 V output at 150 mA, again with output ripple less than 25 mV. Using V_S = 0.5 V and V_D = 1 V, on-time is approximately 2 1/2 times the off-time. Timing capacitance is selected at 0.01 μF, setting the off-time at 30 μs. On-time is consequently approximately 73 μs. An 80 Ω resistor on the drive collector provides a 50 mA base drive to the switch. With a peak input current of 1.1 A, R_{SC} is selected at 0.3 Ω. At full load with an average input current of 555 mA, efficiency is 80%. At 10% of full load, regulator efficiency is 78%. Output capacitance is calculated to be 492 μF.

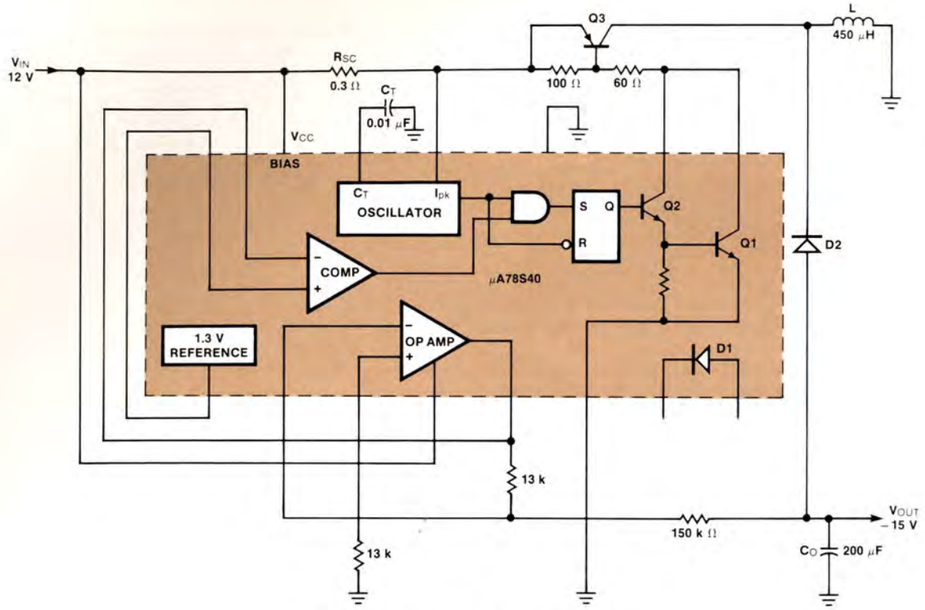


Fig. 5 Inverting Voltage Regulator

A voltage inverter configuration is shown in *Figure 5*. This mode requires an external pnp transistor (Q3) and a catch diode (D2). With a +12 V input, output voltage is -15 V at 200 mA, with output ripple less than 50 mV. With a timing capacitor value of 0.01 μF, off-time is 30 μF. Peak current can be calculated (0.96 A) as can the value of the inductor (500 μH). Average input current for this inverter mode is 275 mA with a regulator efficiency of 93% at full load and 90% at 10% load. Output ripple is held to 50 mV by using an output capacitor with a value of 251 μF. In this inverter mode, the internal operational amplifier inverts the output voltage to compare it to the 1.3 V reference. This is only possible because the common mode range of the op amp includes ground. Circuit breakdown does not limit output voltage, because no portion of the control circuitry sees any negative voltage.

MORE SOPHISTICATED APPLICATIONS

With the addition of a few external parts, the μA78S40 can provide output power up to 100 W and output voltages up to and even exceeding 100 V. Two regulated outputs can be made available by using a switching output and a series-pass output.

One such interesting variation is the use of the universal regulator to provide a constant output for voltage inputs that are both higher and lower than the output, *Figure 6*. In this case, 12 V at 100 mA is provided at the output for input voltages over a 4 V to 24 V range. This is done by using a step-up mode similar to the version shown in *Figure 4* to provide a 15 V output and then using the internal op amp as a series-pass regulator to reduce the 15 V output to a 12 V output. When the input voltage exceeds 16 V, the step-up regulator circuit follows the input at approximately the input voltage minus 1 V, but the series-pass output remains constant at 12 V. The op amp exhibits excellent noise rejection, so output ripple is virtually non-existent at the 12 V output. Regulator efficiency is about 50% for the upper and lower limits of the input range (4 V and 24 V) and increases to a maximum of about 75% for intermediate voltages.

Another variation involves the addition of an external pnp transistor and an external catch diode to the step-down regulator. *Figure 7*. The transistor (Q3) increases output current capability by a factor of 10 and also improves switching efficiency because the switching voltage drops from 1.6 V to 1 V. The npn Darlington pair switch is connected to provide the base drive for Q3, with a 56 Ω resistor limiting the base drive to 500 mA. A peak input current of 10 A (plus the 0.5 A base drive) with an input voltage of 30 V provides a 5 V, 5 A output. The average input current is 1.1 A. Efficiency of the regulator is approximately 73%, with the control circuit dissipating the base drive power (0.5 A x 30 V). In this case the off-time/on-time ratio is about 4:1, with the off-time at 150 μs and on-time at 38 μs. Output capacitance of 2500 μF keeps output ripple to 100 mV. The external diode (D2) is required to handle the 10 A switching current.

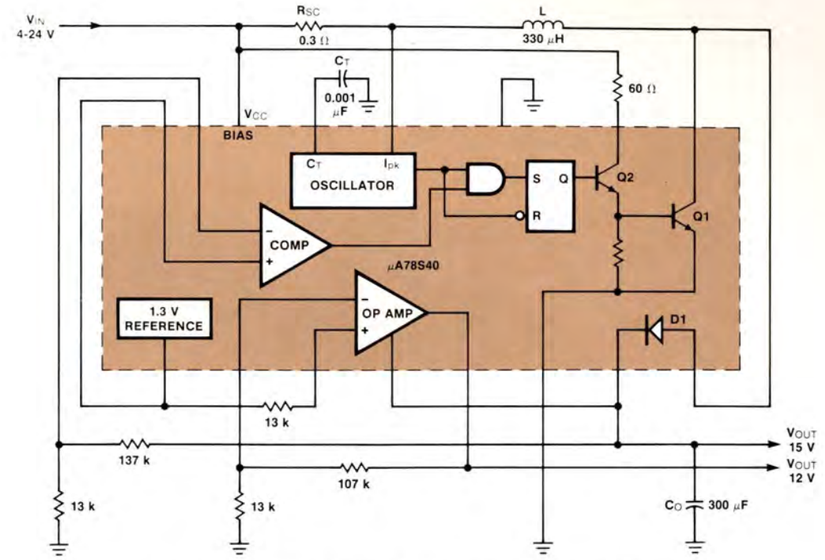


Fig. 6 Constant Output Voltage Regulator Over 4-24 V Input Range

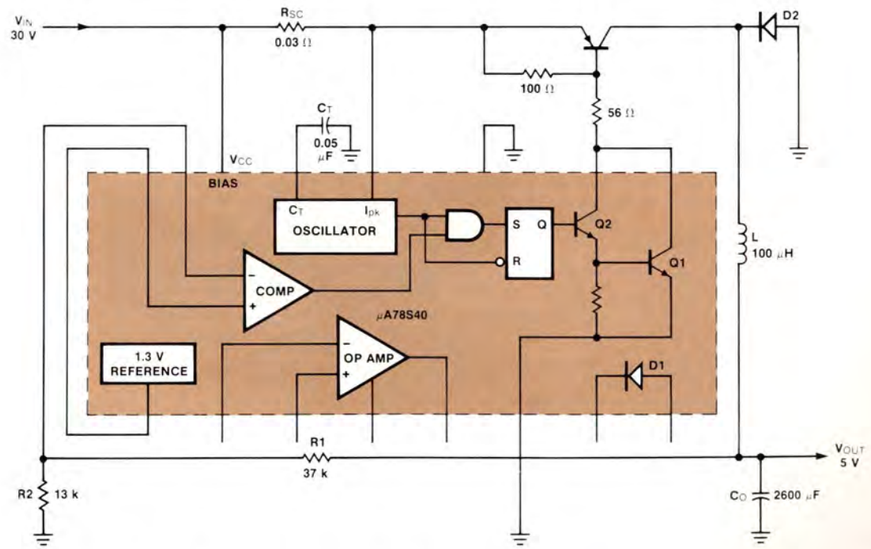


Fig. 7 Modified Step-Down Regulator with 5A, 5 V Output

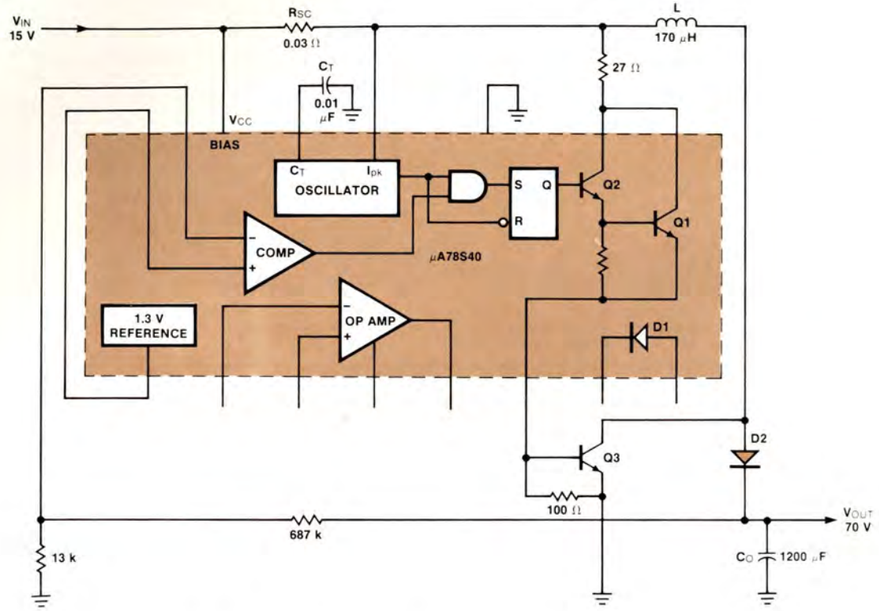


Fig. 8 Switching Regulator with 15 V Input, 70 V Output

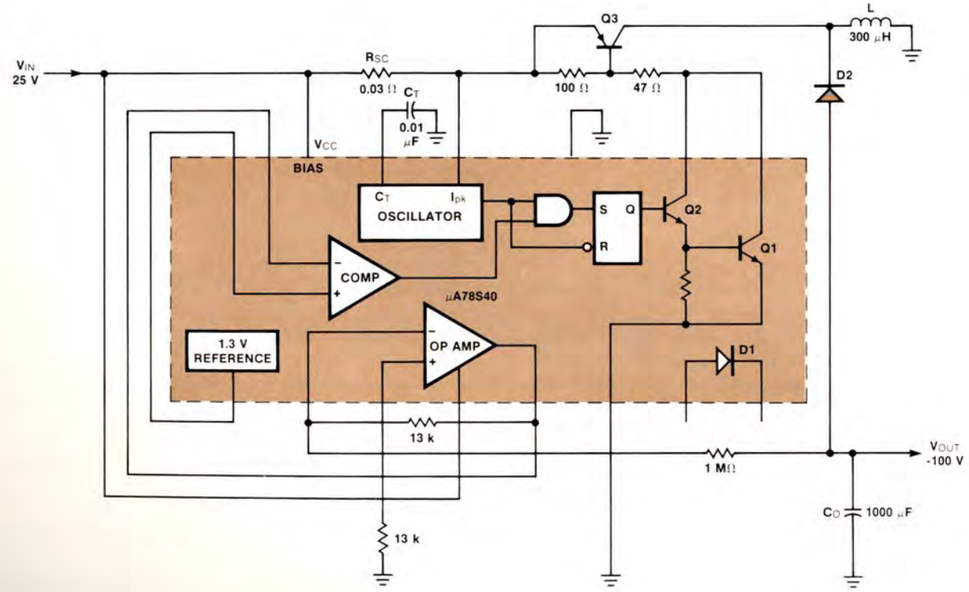


Fig. 9 Switching Regulator with 25 V Input, -100 V Output

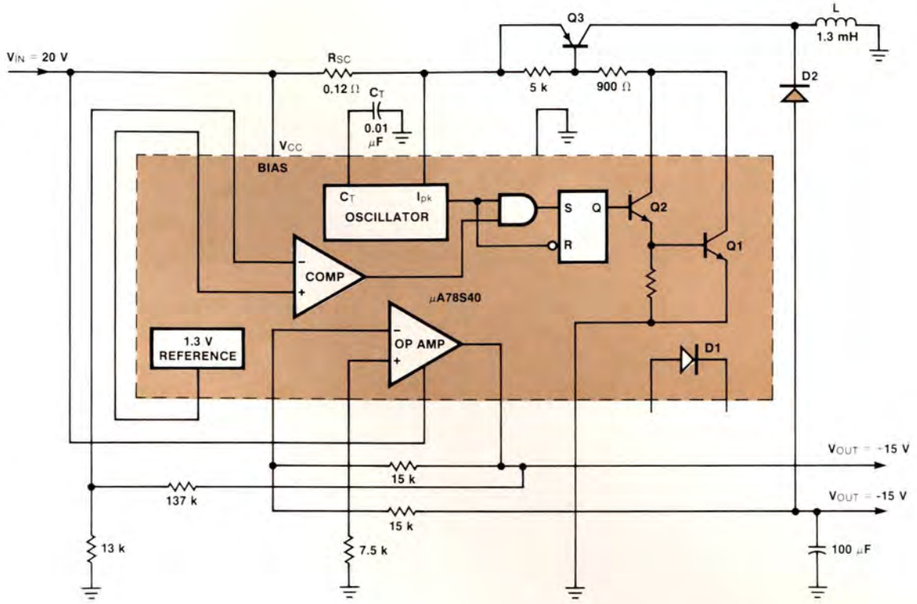


Fig. 10 Dual Tracking Supply

The addition of a boost transistor and a flyback diode to the step-up regulator configuration develops a regulated 70 V, 1 A output, *Figure 8*. The Darlington pair switch emitter output provides base drive to the external npn transistor Q3. Output voltage is limited by this transistor and diode breakdown voltages, not by the IC. The base drive to Q3 is limited to 0.5 A by a 27 Ω series resistor on the switch collector. For this situation (15 V in — 70 V, 1 A out) the on/off ratio is 4:1 with on-time at 120 μs and off-time at 30 μs (C_T = 0.01 μF). Average input current is 5.4 A, (1/2 the peak current plus the 0.5 A base drive). Regulator efficiency is 84%, and output ripple is limited to 100 mV by a 1200 μF output capacitor.

A voltage inverting regulator with an external pnp switch (Q3) and an external diode (D2) can generate almost any negative voltage, because the external transistor and diode limit the output voltage, *Figure 9*. This particular version provides -100 V at 1A from a +25 V input. The peak current is 10.5 A, average current is 4.44 A, and the regulator efficiency is 83%. The on-time to off-time ratio is a little more than 4:1, resulting in an off-time of 30 μs and an on-time of 126 μs. A 1000 μF output capacitor limits output ripple to 120 mV.

Figure 10 illustrates a dual-tracking regulator that provides both +15 V and -15 V outputs from a single +20 V input. The negative output voltage is generated with an inverter circuit similar to the circuit of *Figure 5*, but the op amp is connected in a gain-of-1 configuration with its output divided down and compared to the 1.3 V reference voltage. As shown, this regulator provides ±15 V at 100 mA with 80% efficiency — 75% postive voltage, 85% negative voltage — with output ripple limited to 30 mV.

A high-output regulator with two outputs is illustrated in *Figure 11*. From a single 5 V input voltage, a 12 V and a 15 V output are provided. Two external npn transistors are used; Q3 boosts the step-up function, and Q4 increases the series-pass output to 1 A. A total of 1.5 A is available from the two outputs, with 80% efficiency on the 15 V output and 64% efficiency on the 12 V output.

The final switching regulator variation shown is a negative input/output regulator, *Figure 12*. This presents a slightly more difficult challenge, since the reference voltage is referred to a negative input rather than ground. A ground reference of -2.6 V can be generated by using the op amp as a differential amplifier. Then, using a typical step-down regulator configuration, a -48 V input produces a -12 V output at 300 mA with a regulator efficiency of 85%.

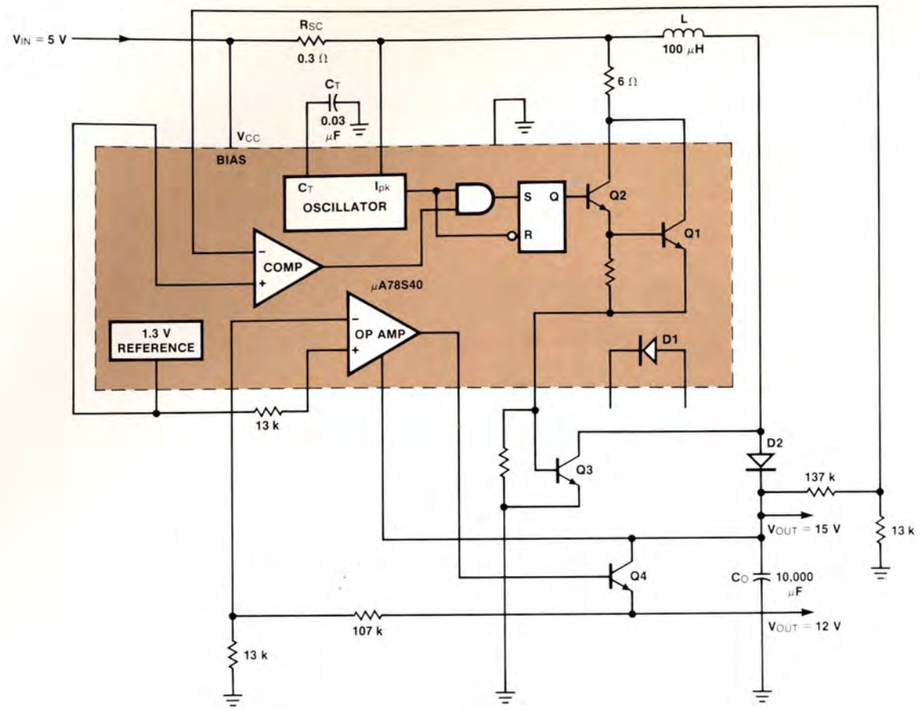


Fig. 11 Step-Up and Series-Pass Regulator

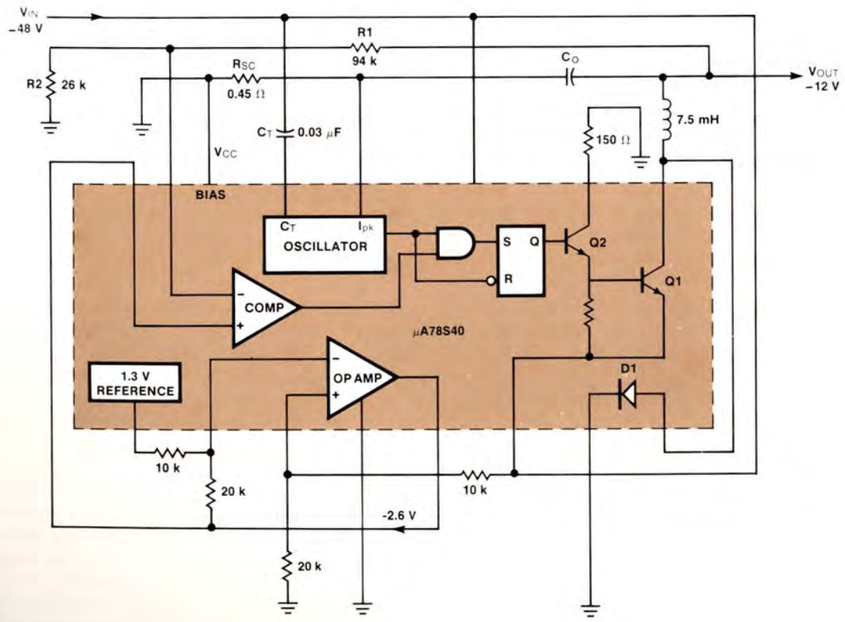


Fig. 12 Negative Input/Output Regulator

THE ANALYSIS

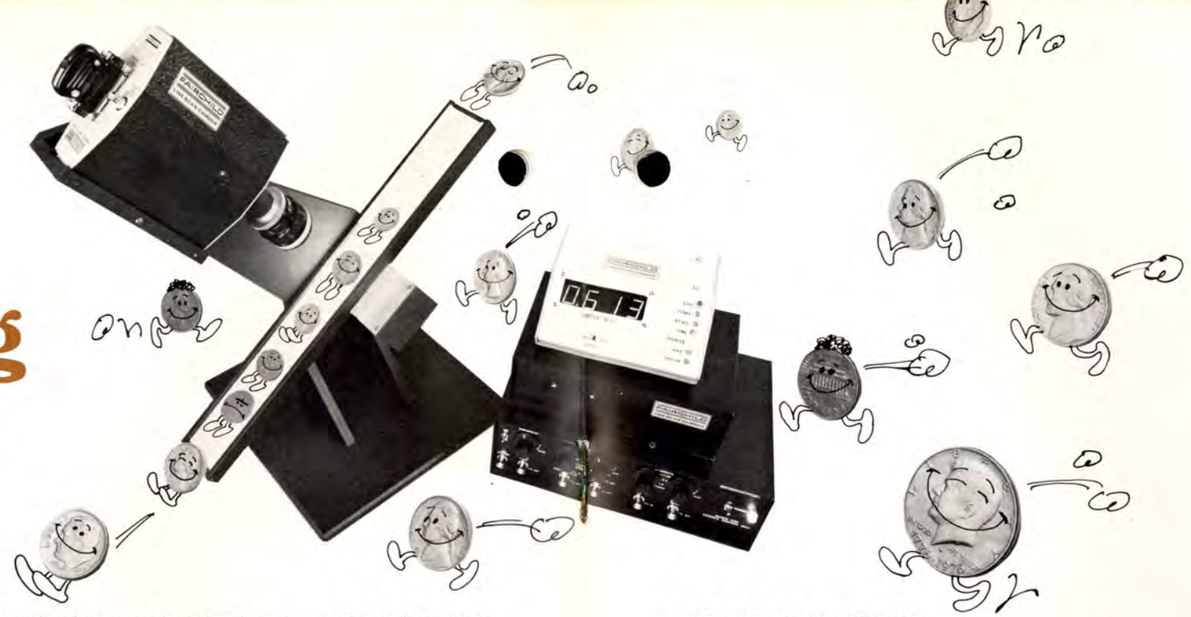
Switching regulators, although somewhat more complex than series-pass regulators, offer power system designers very high efficiency voltage regulators appropriate for a variety of applications. A wide range of power conditions can be met, from battery operation to high-power, high-current applications. Step-down, step-up, and inverter modes of operation are possible with the μA78S40 universal regulator with a minimum number of external parts. Constant output voltages can even be supplied when the input voltages cover a substantial range. The advantages of switching regulators — low operating cost, high efficiency, low power dissipation — are enhanced by the on-chip circuitry of the μA78S40 universal regulator and the circuit partitioning. This partitioning makes available to the power supply designer the common functions needed for most power supply systems and minimizes the need for external components. There are some inherent disadvantages involving switching regulators such as slower response to load changes, some output ripple, and some noise. However, these disadvantages are often outweighed by the advantages of lower operating cost, high power-conversion efficiency, and versatility. □

78S40 Design Formulae

CHARACTERISTIC	STEP DOWN	STEP UP	INVERTING
I_{pk}	$2\ I_{OUT(max)}$	$2\ I_{OUT(max)} \bullet \frac{V_{OUT} + V_D - V_S}{V_{IN} - V_S}$	$2\ I_{OUT(max)} \bullet \frac{V_{IN} + \lvert V_{OUT}\rvert + V_D - V_S}{V_{IN} - V_S}$
R_{SC} *	$0.33\ V/I_{pk}$	$0.33\ V/I_{pk}$	$0.33\ V/I_{pk}$
$\frac{t_{on}}{t_{off}}$	$\frac{V_{OUT} + V_D}{V_{IN} - V_S - V_{OUT}}$	$\frac{V_{OUT} + V_D - V_{IN}}{V_{IN} - V_S}$	$\frac{\lvert V_{OUT}\rvert + V_D}{V_{IN} - V_S}$
L *	$\frac{V_{OUT} + V_D}{I_{pk}} \bullet t_{off}$	$\frac{V_{OUT} + V_D - V_{IN}}{I_{pk}} \bullet t_{off}$	$\frac{\lvert V_{OUT}\rvert + V_D}{I_{pk}} \bullet t_{off}$
t_{off}	$\frac{I_{pk} \cdot L}{V_{OUT} + V_D}$	$\frac{I_{pk} \cdot L}{V_{OUT} + V_D - V_{IN}}$	$\frac{I_{pk} \cdot L}{\lvert V_{OUT}\rvert + V_D}$
C_T*(μF)	$45 \times 10^{-5}\ t_{off}(\mu s)$	$45 \times 10^{-5}\ t_{off}(\mu s)$	$45 \times 10^{-5}\ t_{off}(\mu s)$
C_O *	$\frac{I_{pk} \cdot (t_{on} + t_{off})}{8\ V_{ripple}}$	$\frac{(I_{pk} - I_{OUT})^2 \cdot t_{off}}{2\ I_{pk} \cdot V_{ripple}}$	$\frac{(I_{pk} - I_{OUT})^2 \cdot t_{off}}{2\ I_{pk} \cdot V_{ripple}}$
Efficiency	$\frac{V_{IN} - V_S + V_D}{V_{IN}} \bullet \frac{V_{OUT}}{V_{OUT} + V_D}$	$\frac{V_{IN} - V_S}{V_{IN}} \bullet \frac{V_{OUT}}{V_{OUT} + V_D - V_S}$	$\frac{V_{IN} - V_S}{V_{IN}} \bullet \frac{\lvert V_{OUT}\rvert}{\lvert V_{OUT}\rvert + V_D}$
$I_{IN(avg)}$ (Max load condition)	$\frac{I_{pk}}{2} \bullet \frac{V_{OUT} + V_D}{V_{IN} - V_S + V_D}$	$\frac{I_{pk}}{2}$	$\frac{I_{pk}}{2} \bullet \frac{\lvert V_{OUT}\rvert + V_D}{V_{IN} + \lvert V_{OUT}\rvert + V_D - V_S}$

Fast Sorting with CCD

by Howard Murphy and Joe Rothstein



Charge-coupled imaging devices, introduced in the early 1970's, have been designed into a myriad of industrial applications. These range from sophisticated scientific optical instruments for use in research laboratories to rugged industrial inspection systems for steel, lumber, and glass mills; from facsimile and OCR scanning systems to miniaturized low-light-level television cameras; and from precision geometric instrumentation to simple object counting systems. In many of these applications, the CCD image sensor is used as a functional replacement for components manufactured using older technologies, e.g., the Vidicon tube in a TV camera. CCD sensors offer significant advantages — wider dynamic range, broadened spectral response, low voltage and low power operation, monolithic solid-state reliability, high operating speeds and precise geometric accuracy.

On the other hand, CCD technology is creating solutions to engineering problems that seemed almost impossible to solve economically in the past. Camera systems using CCD line-scan image sensors are being used for non-contact measurement, inspection, defect detection, shape and pattern recognition, color sorting, and for a wide variety of quality process-control industrial applications. The self-scanning feture makes this system ideal in a large variety of industrial applications in which the object or material to be inspected is in motion or is being moved by a conveyor belt or other mechanism. The sensor provides scanning along one axis of the object while object motion provides scanning in the other. The use of fully automatic optical inspection systems enhances productivity by improving quality control in automated manufacturing processes.

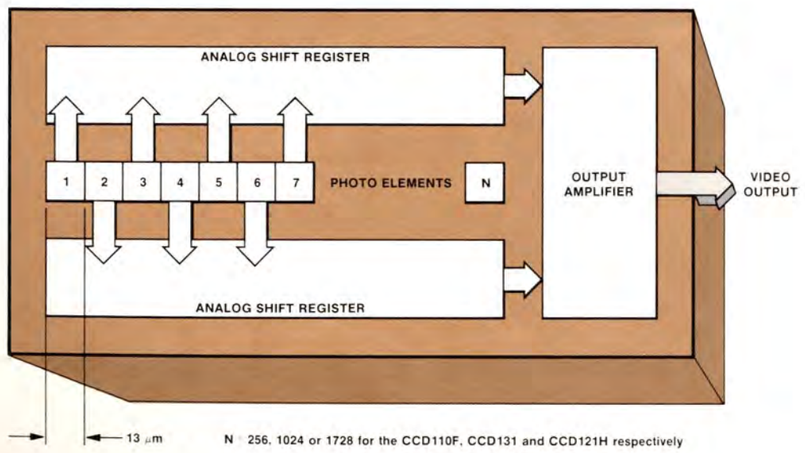


Fig. 1 Linear Image Sensor Block Diagram

THE CCD IMAGE SENSOR

The essence of a line-scan system is, of course, a line-scan sensor. In a typical CCD sensor *(Figure 1)*, a row of 13 μm-square photosites is formed within a monolithic silicon chip, at present, either 256, 1024, or 1728 photosites in a row. The photosites detect light from the object and accumulate charge packets of electrons that are directly proportional to the light intensity. The packets, representing information, are periodically transferred to the adjacent analog shift registers, and are then transported out of the CCD as a serial analog-video data stream, controlled by external clock signals.

CCD LINE-SCAN CAMERA SUBSYSTEMS

There are presently three models of line-scan camera subsystems — the 256-element CCD1100, the 1024-element CCD1300, and the 1728-element CCD1400. The choice among them is determined primarily by resolution requirements, since each camera model offers essentially equivalent performance in other respects. The line-scan camera can be ordered equipped with a C-mount lens with a focal length to meet the specific application.

Each camera subsystem includes a line-scan camera, a camera-control unit and interconnecting cables. Within the camera is a CCD image sensor, a logic board to provide clock signals for controlling sensor operation, and a video processing assembly to generate an analog-video and a binary-video output signal. The analog-video signal is a continuous analog representation of the spatial distribution of image brightness, obtained by sample-and-hold processing of the raw sensor output. The binary-video output, provided by a comparator, is a digital version of the analog video waveform and corresponds to black-to-white and white-to-black transitions of the analog-video signal across the threshold. The threshold adjustment can be varied across the full dynamic range of the camera.

The camera-control unit provides the power supply voltages and interface connections for the subsystem input and output signals. It also contains the adjustment controls for camera exposure time, video data rate, the threshold voltage for the binary-video comparator, and an AGC off-on switch.

AN APPLICATION EXAMPLE — COIN SORTER

When a CCD camera subsystem is combined with the versatile microprocessor, the result is a powerful metrology system that includes an internal decision-making capability. This dynamic combination can best be illustrated by describing a simple system such as a coin sorter; the concepts can readily be extended to solve more complex industrial problems. The basic operating principle of the coin sorter *(Figure 2)* is the optical measurement of the diameter of an unknown object, and comparison of the measured diameter to a diameter-limit table for six denominations of U.S. coins.

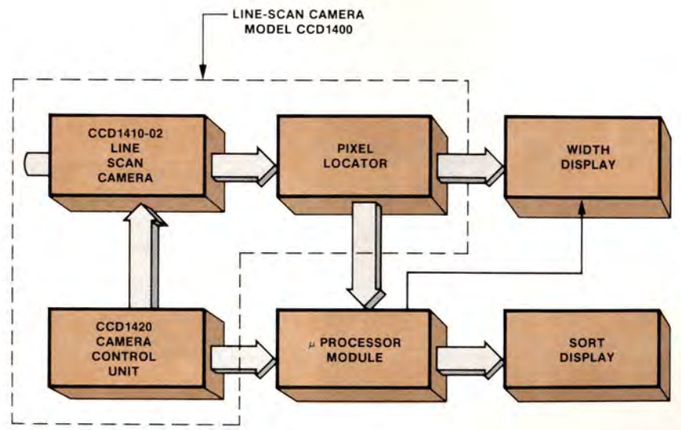


Fig. 2 Optical Sorting System

A CCD1400 line-scan camera subsystem measures the backlighted opaque objects which are transported past the camera by a conveyor mechanism — a gravity-powered slide. The image sensor within the camera has 1728 photosites spaced along an active channel length of 0.884". The camera is equipped with a 50-mm focal-length lens and provides a scanned line length of 1.728" across the coin slide at a lens-to-object working distance of 5.8". Each sensor photosite, or pixel, thus senses the brightness of a 0.001"-square area in the object plane; the total image sensing array detects the spatial distribution of brightness across a 1.728"-long scan line which is 0.001" wide in the axis of object motion. The length of the scan line covered by the camera could, of course, be set to any desired width by selecting different lens focal length and working distance; the available resolution in this particular camera would remain 1728 pixels per scan line under any condition.

The maximum velocity of objects moving past the camera is assumed to be 20 ips. The smallest object of significant interest to the coin-sorter system is a U.S. dime with a diameter of 0.7". Hence a dime will travel by the camera in approximately 35 ms. It seems reasonable to ask that the system check the width of each object at least 100 times as it passes the inspection station, thus requiring the camera to provide 100 scan-line readouts in 35 ms. This defines a 350 μs exposure time which, in turn, requires a video data rate of about 5 MHz per pixel. These conditions are comfortably within the normal operating range for the CCD line-scan camera, although they are considerably faster than can be achieved by other technologies. Exposure-time and data-rate adjustments can be made by front panel controls on the camera-control unit.

The binary video output of the camera is a HIGH TTL-compatible signal for a readout of pixels that detect an image brightness above an adjustable threshold level; it is a LOW signal during the readout of pixels detecting less than the threshold brightness value. Therefore, the binary video output for this system is HIGH for scan-line locations that are not shadowed by coins and LOW when coins interrupt light transmission.

A counter in the pixel-locator accessory *(Figure 3)* provides a bit-parallel data stream to indicate which of the 1728 sensor pixels in the camera are supplying data at the moment. As video transitions from white to black and black to white occur, the edge detector, driven by the binary video output, strobes the pixel addresses into a FIFO buffer memory. These addresses then become available at the FIFO output as latched parallel 15-bit words to be used by the microprocessor portion of the system for dimensional analysis. When an object enters the camera's field of view, two address words are stored in the FIFO during each scan line; the first indicates the pixel address of the left edge of the object and the second word indicates the address for the right edge.

A FIFO buffer memory used as a data interface between the camera and data processor permits asynchronous operation of the two portions of the system. The camera is running at a 5-MHz data rate with a 350-μs exposure time to achieve a high density of scan lines across the smallest object, while microprocessors are typically restricted to clock rates below 1 MHz and require two-to-six clock cycles per arithmetic operation. The pixel-locator accessory, designed for use in camera-microprocessor interface applications, is equipped with an optional hand-shake I/O capability for ease of system design and control.

The 8-bit microprocessor hardware used for the coin-sorter camera system *(Figure 4)* includes an F6800 MPU, a 256-byte RAM, and a PROM that stores a development program called JBUG. Capability for audio tape I/O is included in the JBUG

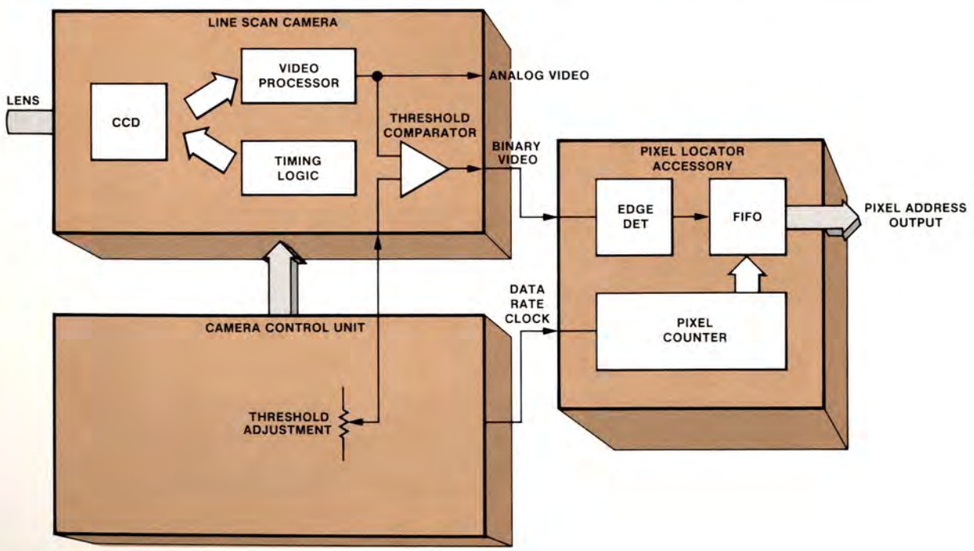


Fig. 3 CCD1400 Camera Configuration Using Pixel Locator Accessory

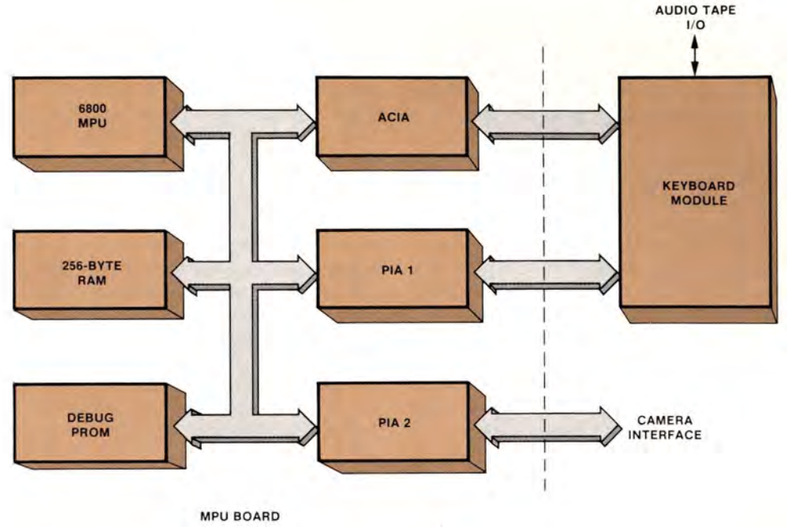


Fig. 4 Microprocessor Hardware

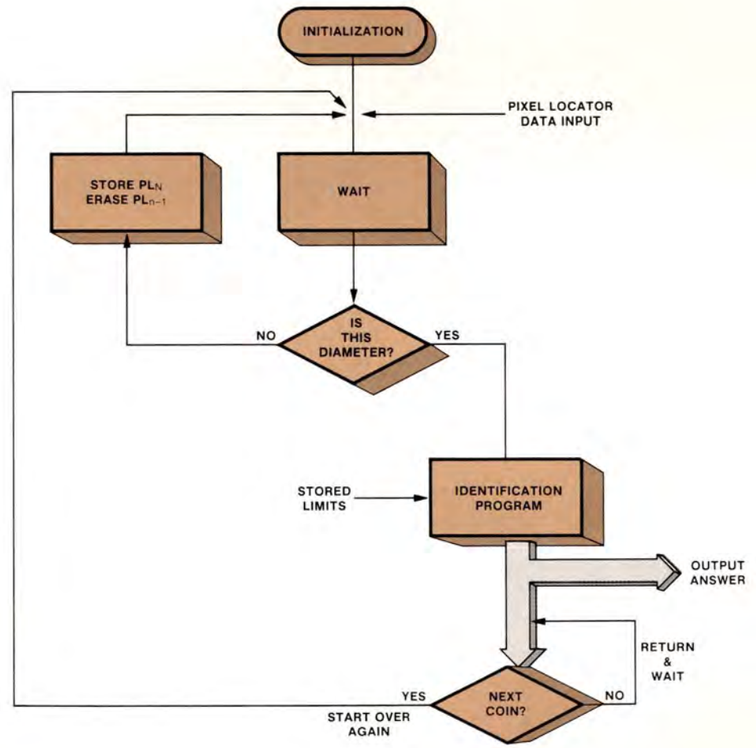


Fig. 5 Microprocessor Software

program and hardware. An F6820 peripheral interface adaptor with two 8-bit bidirectional I/O ports is also used. Eight of the lines are microprocessor inputs, driven by the pixel-locator output; the other eight lines are outputs to the display from the coin-sorter program.

As a coin (or slug) moves through the camera's field of view, the measured dimension is a chord with a width that starts at zero pixels and increase until the camera scan line crosses the center of the coin. Dimensional data is supplied to the microprocessor as 8-bit address words at the end of each camera scan-line readout. After system initialization *(Figure 5)*, the microprocessor follows a compare-and-branch procedure to determine when the camera scan is through the coin center. This is accomplished by comparing the current measured width of the coin (PL_N) with the preceding measured width (PL_{N-1}); the program determines that a diameter is PL_{N-1} for the first two inputs where $PL_N < PL_{N-1}$. The first measurement portion of the program is executed faster than the 350-μs exposure time, hence, the microprocessor spends most of its time in a loop waiting for an interrupt indicating that new input data is ready.

When the coin diameter is determined, the program branches to an identification procedure *(Figure 6)*, which is a series of compare-and-branch instructions. The measured diameter is compared to low and high specification limits that were supplied to the microprocessor during initialization and stored in designated RAM addresses.

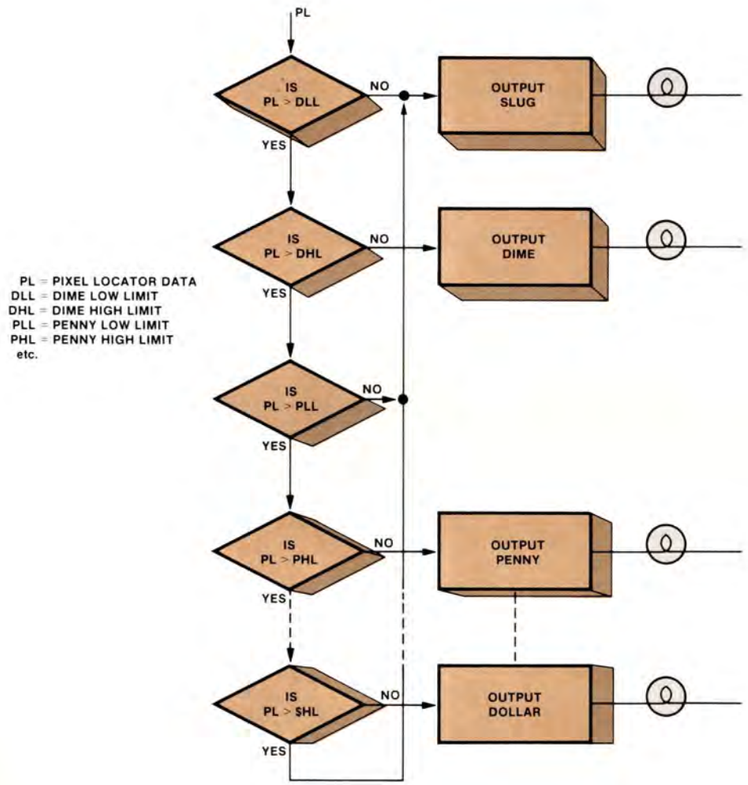


Fig. 6 Identification Program

If the measured diameter (PL) is less than the low limit specified for a dime (DLL), the program outputs a "1" on a bit line which drives the SLUG indicator light. If DLL < PL < DHL (high limit for dime), the program outputs a bit on another line to illuminate a DIME indicator. If DHL > PL > PHL (high limit for penny), the system signals the SLUG indicator. This procedure is repeated through the high spec for a silver dollar ($HL). The program then enters another wait loop until PL goes to zero, which indicates that the analyzed object has moved completely past the camera inspection line.

The microprocessor is dealing with 8-bit pixel addresses which provide adequate resolution for coin identification. The 1728-element camera resolution is represented in the pixel locator as 13-bit BCD numbers. A full-resolution digital display of measured-object diameters *(Figure 7)* is driven by the pixel-address output. The strobe input to the display-circuit latches is controlled by the microprocessor so that the display continuously shows the measured diameter of the last object analyzed.

CONCLUSION

The coin-sorter system is a simple example of the broad potential of the line-scan camera/microprocessor combination. Actually, modern vending machines require considerably more complex analytical ability to foil users of washers, slugs and counterfeit coins. However, these simple principles of system design and operation can be adapted for sorting rapidly moving items, e.g., oranges, apples, and other fruit and vegetables, by size, in a food-processing plant. With a little more microprocessor programming, nuts, washers, and other mechanical components could be sorted in a hardware manufacturing plant.

The system can be generalized into a two-dimensional inspection capability by using a more complex set of microprocessor software and a larger RAM storage capacity. Also, the system can be made "self-educated", i.e., the high and low limits of the diameter widths could be derived by measuring a statistical sample as it passes the inspection station, as opposed to having the limits supplied by the operator.

The coin-sorter system design exploits the high-speed capability and excellent optical sensitivity of the CCD image sensor combined with the flexibility of the CCD-camera subsystem. A key requirement for all non-contact inspection-system designs is the precise dimensional accuracy inherent in CCD image sensors. In addition, CCD imaging devices offer wide dynamic range, linearity, and low light-level operation.

The relatively detailed consideration given to the overall design of this simple system should provide an appreciation of the exciting potential that optical inspection systems have in modern manufacturing operations.□

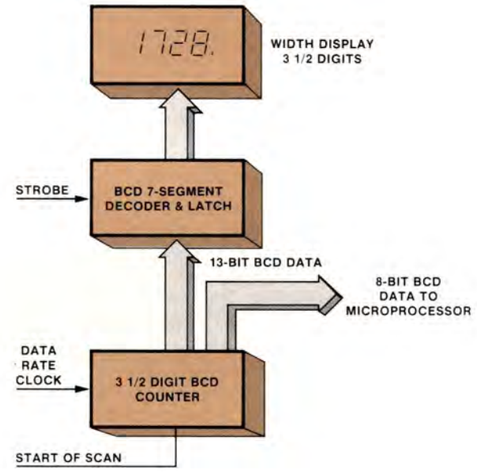


Fig. 7 Measured-Width Display System

CIRCUIT IDEAS Digital

by Charles Alford

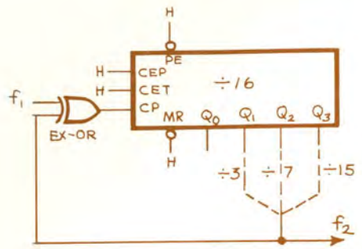


Fig 1 Divide by 3, 7 or 15

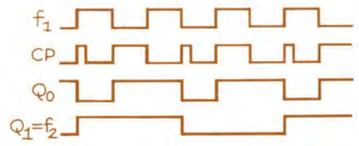


Fig.3 Waveforms for Fig.1 in ÷3 Connection

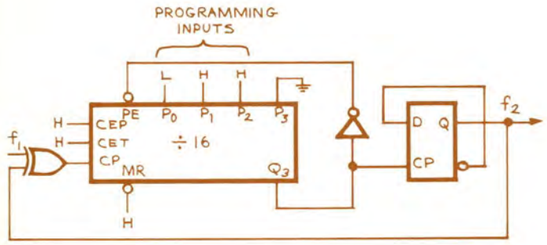


Fig. 2 Programmable odd-ratio divider

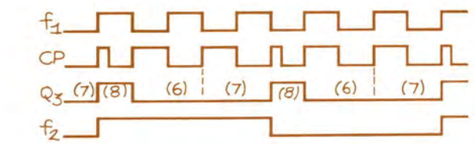


Fig.4 Waveforms for Fig.2 ÷5 Mode

Family	Counter	EX-OR	Flip-Flop
TTL	9316	7486	7474
LP-TTL	93L16	9L86	LS74
LS-TTL	LS161	LS86	LS74
CMOS	40161B	4030B	4013B

ODD RATIO DIVIDERS WITH 50% DUTY CYCLE OUTPUT

A design task that arises occasionally involves dividing an incoming frequency by an odd number, yet producing an output that has a 50% duty cycle. The circuit of *Figure 1* will perform such a function, provided that the input frequency f_1 has a 50% duty cycle. When the feedback signal to the Exclusive-OR gate is LOW, the gate output has the same phase as f_1, and thus the counter advances on the rising edge of f_1. When the feedback signal goes HIGH, however, the gate output becomes the complement of f_1, and the counter thenceforth advances on the falling edge of f_1. In this transition from rising-edge to falling-edge sensitivity, the counter effectively gains a clock. The feedback signal will have a 50% duty cycle (minus small differences in rising and falling propagation delays) only if there is uniform spacing between the rising and falling edges of f_1. Waveforms for the divide-by-3 connection are shown in *Figure 3*.

A broader selection of divide ratios is obtained by using a little more logic, as shown in *Figure 2*. The counter operates in a programmable mode, with the rising edge of Q3 clocking the flip-flop and enabling the parallel loading into the counter, which occurs on the next rising edge of CP. The flip-flop is necessary because, in the programmable mode, none of the counter outputs are symmetrical. The overall divide ratio is expressed as follows.

divide ratio $N = f_1/f_2 = 2M - 1$
where M is the divide ratio of Q3 of the counter with respect to its CP input rising edges.

To obtain a particular divide ratio M, the parallel inputs are set to nine minus M. For example, to obtain an overall divide ratio of 5, M must be 3 and the preset data must be 6, which is the value indicted in *Figure 2*. Waveforms for this divide ratio are shown in *Figure 4*. Once again, a 50% duty cycle at f_2 is dependent on equal spacing between the rising and falling edges of f_1. □

Are Your Plastic PROMs Protected ?

by Joseph Ferro



NICHROME LINKS

The fabrication of nichrome link programmable read only memories in plastic packages requires good process control to assure device reliability. Moisture penetration in plastics could lead to electrolysis causing corrosion of the nichrome fuses. Fuse protection is provided by the surface glassivation layer applied to the chip, and a reliable method of evaluating the effectiveness of this glassivation is necessary. The testing method used should provide meaningful reliability prediction data in a short time.

Biased Pressure Temperature Humidity (BPTH) testing is an effective process control method for plastic encapsulated nichrome link PROMs. With the control limit established, reliability is *better than 0.001%/1,000 hours*. Both chemical vapor-desposited phosphovapox and plasma-deposited silicon nitride glassivation techniques were evaluated. Silicon-nitride protected devices proved to have a life three times that of the phosphovapox devices and five times that of unglassivated devices.

The PROMs tested are high-power devices (typically 0.5 W) creating a problem in terms of humidity bias testing. Chip temperature is approximately 50° C higher than ambient temperature, driving the moisture away from the chip. For moisture to permeate the chip surface, a 50% duty cycle was used.

At 85° C and 85% relative humidity, the *Bias Temperature Humidity test* requires at least 2000 hours to obtain meaningful reliability data, not timely enough for process control. *Unbiased* autoclave humidity tests (pressure cooker tests) are meaningless for process control, since failures cannot be produced because of the absence of a voltage gradient across the devices under test. In more than 44,000 device hours of testing, no failures occurred.

BPTH DEVICE TESTING IS EFFECTIVE

Considering these factors, *Biased Pressure Temperature Humidity* testing is conducted with biased units in an autoclave. Environment at the device surface is maintained at 100% relative humidity, 121° C, and 15 psig with the power cycled. Two important objectives are accomplished with the BPTH test: fast results are available for process control and reliability predictions of device life times are possible.

Evaluations were made on PROMs manufactured with the Isoplanar Schottky process, meaning the semiconductor elements are separated by an insulating film of thermally grown oxide, *Figure 1*. The device has a dual-layer metallization system of aluminum doped with silicon and copper with a dielectric layer of phosphovapox. A surface-protecting glassivation layer is deposited on top of the device, which is then encapsulated in epoxy.

Resistance of the nichrome fuse in these devices is approximately 300 Ω. Devices under test are biased to draw read current through each selected bit (fuse), with a power supply voltage of 5 V. When selected, the unprogrammed fuse typically draws 1 mA. Therefore, an addressed unprogrammed fuse has a typical potential drop of 300 mV.

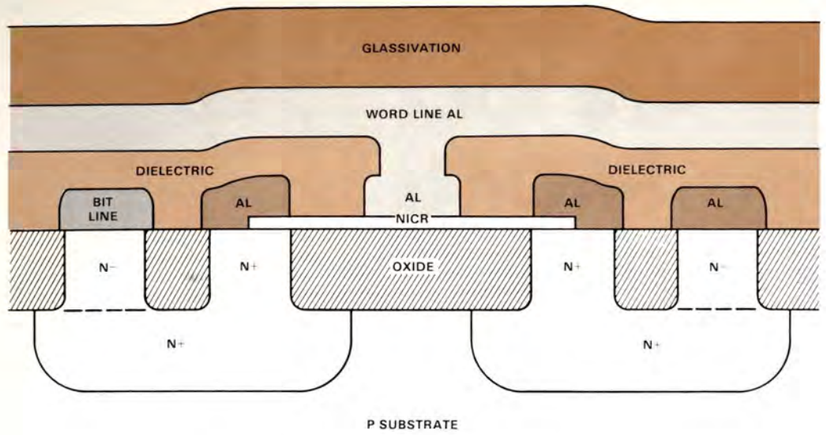


Fig. 1 Cross Section of Isoplanar Schottky PROM.

PHOSPHOVAPOX GLASSIVATION

An acceleration factor between Biased 85° C/85% Relative Humidity and Biased Pressure Temperature Humidity testing was established. Devices from five different assembly lots were evaluated using 85° C/85% RH and BPTH tests. These lots were all glassivated with a single layer of phosphovapox from 1.2 to 1.4 μm thick. Results of both tests are plotted in *Figure 2*. The dominant failure mode for both tests was nichrome fuse corrosion. However, with the BPTH test, aluminum corrosion became the primary failure mode for units surviving beyond 336 hours. The time required to obtain 50% cumulative failure for the 85° C/85% RH test was 4,000 hours. For the BPTH test, only 200 hours were necessary, indicating an acceleration factor of 20.

NON-GLASSIVATED DEVICES

A group of devices without any surface glassivation was subjected to both tests, with the results of the 85° C/85% RH test also plotted in *Figure 2*. Time to 50% cumulative failure was 2,350 hours with the primary failure mode being nichrome fuse corrosion. With the BPTH test, the primary failure mode was corrosion of the top layer of aluminum metallization at the point of greatest potential difference between adjacent metal lines. A possible explanation is that the non-glassivated surface becomes moisture saturated, causing the aluminum metallization to corrode before any moisture can reach the nichrome fuses beneath the dielectric layer. Because the failure modes of the two tests were different, BPTH testing cannot be used effectively for non-glassivated nichrome PROMs, although this technique may still be appropriate for other non-glassivated devices not employing nichrome links.

SILICON-NITRIDE GLASSIVATION

Silicon nitride has been shown to be an excellent ionic contamination and moisture barrier. Several devices with a 6000 ±500 A° coating of silicon nitride were evaluated with both tests. The results of these tests compared to the BPTH tests of the phosphovapox devices are shown in *Figure 3*. Time to 50% cumulative failure for the silicon-nitride glassivated units was 660 hours compared to 200 hours for the phosphovapox glassivated units. The primary failure mode for the silicon-nitride devices in the BPTH tests was corrosion of the aluminum at the bonding pads and at cracks in the glassivation. No corrosion failures at all occurred until the 400-hour point. This aluminum corrosion is consistent with the results obtained with the phosphovapox glassivated devices that survived beyond 336 hours of testing. Failure of the silicon-nitride glassivated devices because of nichrome fuse corrosion was limited to less than 5%. With the 85° C/85% RH test, *no corrosion failures at all occurred in 7,000 hours*. Based on the acceleration factor determined for the BPTH test, a projected 50% cumulative failure level would be in excess of 13,000 *hours* for the 85° C/85% RH test.

The silicon-nitride glassivation demonstrates excellent protection against nichrome fuse corrosion. Results indicate that device life times are improved a factor of more than three when using silicon nitride instead of phosphovapox. Compared to unglassivated device, the improvement is fivefold. The results are tabulated below.

	TIME TO 50% CUMULATIVE FAILURE	
GLASSIVATION	BPTH TEST	85° C/85% RH TEST
Non-glassivation		2350
Phosphovapox	200	4000
Silicon Nitride	660	13000?

PROCESS CONTROL MEANS LIMITS

There is little agreement as to the relationship between 85° C/85% RH bias testing and actual field performance. Acceleration factors ranging from 50 to 10^6 have been reported. Assuming that an acceptable field failure rate (for electrolytic corrosion failures) is 1% in one million operating hours or about 114 years, the failure rate per 1,000 hours is 0.001%. With an acceleration factor of 1,000, this field failure rate goal can be met if the failure rate per 1,000 hours of operation at 85° C/85% RH is less than 1%. Because of the power cycling, and to be conservative, a failure rate of 1% per 2,000 hours of 85° C/85% RH testing was established.

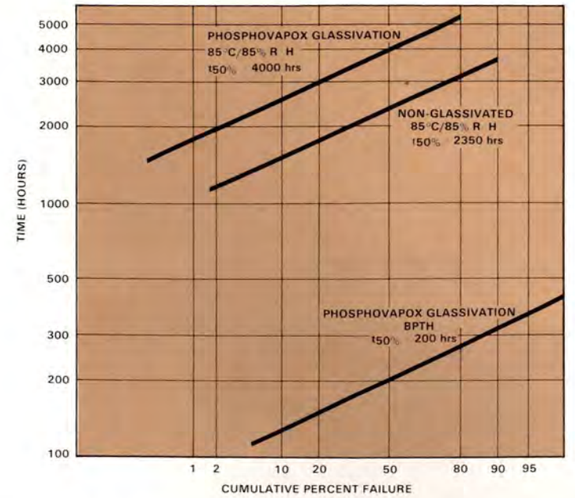


Fig. 2 85°C/85% RH versus BPTH Test Results for Phosphovapox Glassivated Devices. 85°C/85% RH Test Results for Unglassivated Units are Shown for Comparison.

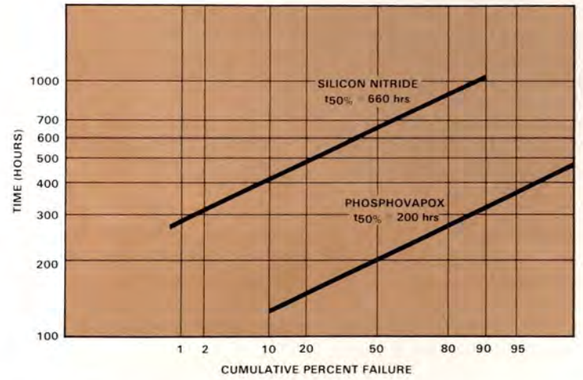


Fig. 3 BPTH Test Results for Silicon Nitride versus Phosphovapox Glassivation.

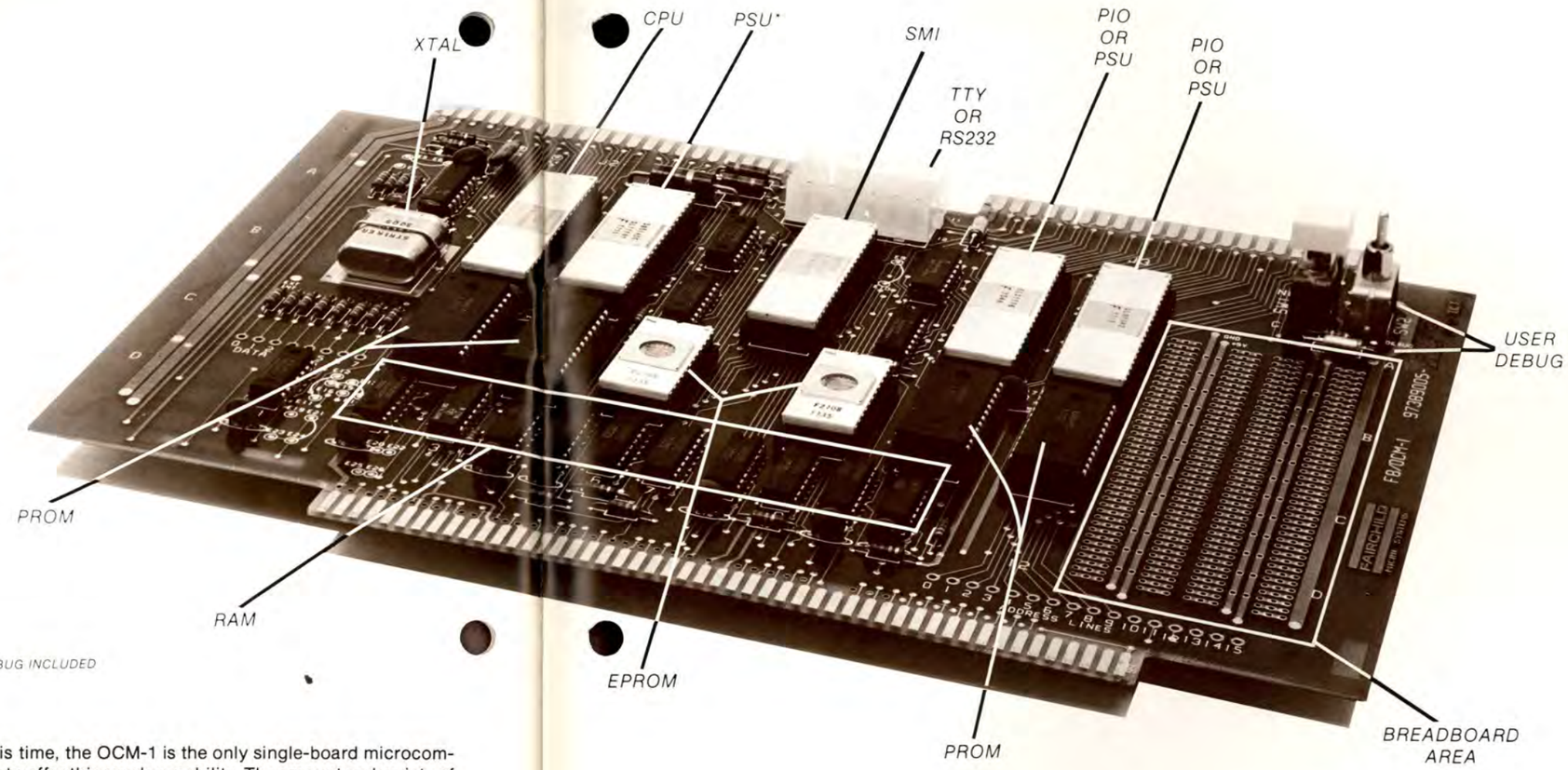
The process control limit for the BPTH testing was based on the same factors, taking into account the acceleration factor of 20. Thus, the acceptable failure limit for the BPTH test was established at 1% per 100 hours of operation under BPTH conditions. To avoid the cost of large sample sizes and to minimize sensitivity to sampling variations by allowing more failures, a limit of 20% failure in 175 hours was determined to be an appropriate test condition by extrapolating a line parallel to those in *Figure 2* through the 1% failure per 100 hours point. Beyond the 20% failure per 175 hours limit, the devices can be assumed to have reached a wear out condition because of humidity effects.

ACCURATE RESULTS FASTER

Biased Pressure Temperature Humidity testing is an effective process control test providing meaningful reliability prediction data in a relatively short period of time. By conducting controlled tests of nichrome link PROMs, BPTH test were shown to have an acceleration factor of 20 over normal 85° C/85% Relativity Humidity tests. In addition, by testing devices without glassivation, with phosophovapox glassivation, and with silicon-nitride glassivation, it was possible to conclude that the silicon-nitride glassivation offers more than three times the protection against corrosion than that provided by phosophovapox glassivation for plastic encapsulated nichrome link devices. In fact, the plastic PROMs with the silicon-nitride glassivation proved to be as reliable as hermetic PROMs. □

Single-Board Microcomputer

by Juan Monico



*FAIRBUG INCLUDED

SINGLE-BOARD MICROCOMPUTER
Based on the F8 and completely supported by Formulator™ program development aids, this microcomputer is built on a 7 1/2" x 10 1/2" printed circuit board with room left over for a pre-drilled 8-square-inch breadboard area for customizing by the user. Features such as truly bidirectional I/O lines and sockets that can be used for different functions provide completeness and flexibility that mean you can use this microcomputer the way you get it. Just hook up a power supply and teletypewriter...

WHAT YOU GET
An OCM-1 single-board microcomputer system provides the following features.

- Complete F8 Instruction Set Execution
- Complete Fairbug Resident Monitor
- Up to 64 Individually Programmable, Bidirectional Latched, and Decoded I/O Lines
- User-Defined Breadboard Area
- TTY or RS-232C Interface
- Static Memory Interface
- Two or Four Programmable Interrupts
- 64 Bytes of High-Speed Scratch-Pad Memory
- 1K Bytes of RAM for Permanent Storage
- Up to 6K Bytes of ROM
- Up to 4K Bytes of PROM
- Up to 2K Bytes of EPROM
- 2 MHz Crystal-Controlled Clock
- Simple Access to Address and Data Busses

At this time, the OCM-1 is the only single-board microcomputer to offer this much capability. The amount and variety of storage available, the number of bidirectional I/O lines, the interfaces provided, and the functions possible have generally required more than one board, often several.

HOW YOU GET IT
The system is based on the 8-bit F8 CPU and also includes an F8 Program Storage Unit, a static memory interface circuit, 1K byte of RAM, a TTY RS-232C interface, a clock, and supporting circuitry. These basic units provide a portion of the total capability. Two 8-bit I/O ports and the high-speed 64-byte scratch-pad memory are included in the CPU. The Program Storage Unit (PSU) contains the Fairbug™ Resident Monitor and also provides 1K of ROM and two more 8-bit I/O ports. This unit plugs into a socket and can be replaced by other circuits if it is not required.

Sockets are provided for the other circuits used in the OCM-1, and they provide for the expansion capabilities and versatility possible with this microcomputer board. Four sockets are available for 1K PROMs. Two sockets are available for 1K Erasable PROMs. Two other sockets are provided that can accept either F8 PIO circuits or F8 PSU circuits. In either case, four additional 8-bit I/O ports are provided, bringing the total to 64 bidirectional I/O lines. Also, either the PIO or PSU circuit can be used in place of the Fairbug circuit if this monitor is not required for a particular application. This provides another 1K byte of ROM. This same socket can also accept the K-D Bug system in place of the Fairbug. The K-D Bug system contains all of the functions of the Fairbug and also includes the capability of operating with a calculator-style keyboard and an LED display. OCM-1 microcomputers are normally furnished with the Fairbug. K-D Bug is an optional monitor.

BIDIRECTIONAL I/O
Each of the possible 64 I/O lines on the OCM-1 is truly bidirectional and fully decoded on the board, offering direct TTL compatibility. These lines are programmable for either input or output functions with single-byte instructions. Each line can be used for both input and output at the same time. A line can be providing an input from a key-closure on a keyboard matrix and also be providing an output to drive a display segment. Simultaneous use of these I/O lines greatly expands the capability and versatility of the system.

TERMINAL INTERFACE
A circuit is included on the board for interface to a standard teletypewriter or other 20 mA current loop terminal. Simple jumper connections convert this circuit for RS-232C interface applications.

SOME NICE TOUCHES
In addition to the flexibility offered by the interchangable nature of using sockets for storage and I/O functions, there are other advantages incorporated in the OCM-1 board. A Formulator-compatible 100-pin edge connector is included as well as two 44-pin edge connectors for I/O connections. A large pre-drilled breadboard area is available for user-defined functions. Switches allow simple selection of either the system or user-defined starting address.

In its standard configuration, the OCM-1 has two interrupts and two timers - one each in the PSU and one each in the static memory interface. If two more PIO circuits are used, two additional interrupts and timers are provided. A "daisy chain" priorty systems determines the order of servicing simultaneous interrupt requests.

All of the lines of the Data Bus and the Address Bus are brought out on the board for simple user access.

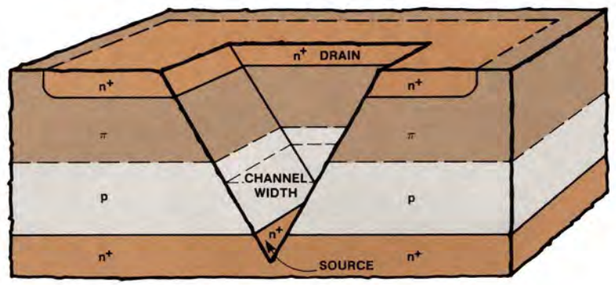
Included with each OCM-1 microcomputer are a user's manual, a Fairbug user's guide, an F8 programming guide, an F8 microprocessor user's reference card and technical data sheets on the circuits. □

NEW PRODUCTS RECENTLY ANNOUNCED

VMOS POWER TRANSISTORS ANNOUNCED

A line of VMOS (Vertical MOS) is now available from Fairchild. Combining the power handling capabilities of conventional bipolar with the high impedance and negative temperature coefficient of FETs for the first time, VMOS transistors provide several advantages.

- Direct Interface to CMOS, MOS, TTL, and DTL
- Fast Switching Times
- No Second Breakdown
- Linear Transfer Characteristics
- Simple Biasing
- No Thermal Runaway
- Increased Current/Power Handling
- Zener Input Protection
- Wide Bandwidth



The devices are vertical channel enhancement mode FETs with a "V" groove in the silicon to define the channel area, *see Figure*. With VMOS devices, the current flow is vertical as opposed to horizontal, providing several important advantages. First, because each V groove creates two surfaces, current density is doubled. As a result, total chip capacitance is low. Second, diffusion depth determines the length of the channel, a process that is much more controllable than the use of mask spacings as in conventional MOS. The width-to-length ratio of the channel is greater, so comparable current density is obtained with much shorter channels.

Fairchild VMOS includes n-channel devices and the first p-channel VMOS devices in the industry. With p-channel devices, complementary designs, grounded drain circuits, and other previously unobtainable possibilities can be achieved. The first VMOS devices have breakdown voltages of 60 V and 90 V and drain-to-source resistances between 4 Ω and 12 Ω at 1 A. In n-channel, the devices now available are the 2N6657, 2N6658, 2N6661, and a new device, the FVN-2. In p-channel, the devices now available are the FVP-1 and the FVP-2. A TO-3 package with 25 W power dissipation is used for the 2N6657, 2N6658 and the FVP-1. A TO-39 package with 6.25 W power dissipation is used for the 2N6661, FVP-2 and the FVN-2. These devices will be available in TO-92 and Dynawatt packages in the near future.

Applications of VMOS power transistors cover a broad range, including audio drivers, transducer drivers, solenoid drivers, microprocessor interface, core memories, lasers, switching power supplies and switching regulators.

ERROR DETECTION CIRCUIT OFFERS STANDARD POLYNOMIALS

A 16-bit programmable cyclic redundancy generator/checker is a new TTL Macrologic error-detection circuit for identifying data transmission errors. The device, designated the 9411 CRC Generator/Checker, uses a 3-bit control input that selects one of eight generator polynomials, including CRC-16, CRC-CITTA, their reciprocals, and the 6-bit Passenger Airline Reservation System (PARS) polynomial. For polynomials of less than 16, automatic right justification is provided, and separate Clear and Preset inputs are used to accommodate floppy disc and other similar applications.

The device operates on serial data streams and incorporates cyclic encoding and decoding schemes for error detection. For encoding, the data stream is divided by the selected polynomial with the result including a remainder that is added to the data as check bits. For error detection, this bit stream is divided by the same polynomial. If there are no errors, this result does not contain a remainder. Many polynomials can be generated, but the relatively small number presently used are directly available from the 9411 by supplying appropriate logic levels to three Select inputs.

4K STATIC MOS RAM OFFERS BOTH LOW AND STANDARD POWER VERSIONS

A 4K n-channel silicon-gate MOS RAM (1K x 4) requiring no external clocks or refresh logic is now available, the F2114. It is available in 200, 300, and 450 ns access times in both low power (350 mW) and standard power (500 mW) versions.

The circuit is designed for applications requiring high performance, low cost, large bit storage, and simple interface. Included, of course, are microcomputers, CRTs, modems, and similar applications that are not necessarily speed sensitive. These memories are TTL compatible, have separate Chip Select, 3-state outputs, and common data I/O. As potential replacements for 2101 memories, they offer significant reduction of power dissipation (500 mW for one 2114 versus 1 W for four 2101s), and significant space requirement reduction (one 2004 requires only 22% of the area of four 2101s).

NEW DIODES AVAILABLE

A new dual varactor diode, primarily for FM tuner applications, is the 1005 (RF5). It is mounted in a standard TWN package with the common cathode on the center pin. It is specified at 37 to 42 pF capacitance at 3 V, 1 MHz; has a capacitance ratio C_3/C_{30} at 1 MHz of 2.5 min, 2.8 max; and 30 V min breakdown voltage at 10 μA.

A new high-current, high-conductance switching diode, the FDH1000, is also available. It offers V_F = 1 V at 500 mA with an 8-ns switching time, a significant accomplishment in the trade-off between conductance and capacitance/switching time requirements.

DEVICES PRESENTLY AVAILABLE. ORDER SPECIFICATIONS BY PRODUCT NUMBER.

POWER AMPLIFIER LINE ADDS TWO

Intended primarily for automotive applications, two new audio power amplifiers are now available — the TDA2002 and the TDA2002A. They supply up to 10 W to a 2 Ω load, and both circuits feature thermal shutdown, short-circuit protection, low external component requirements, and minimum space requirements. In addition, the TDA 2002 features guaranteed overvoltage protection.

These high-current devices are suitable for automotive AM, FM, and CB radios or other industrial applications with a load impedance of 4 Ω or less. Both are available in the new 5-lead TO-220 package in a popular vertical mounting configuration or a horizontal mounting configuration. Minimum board space is required with excellent thermal resistance.

PRECISION OP AMP NEEDS NO EXTERNAL NULLING

A new precision op amp with very good stability, very low noise, high gain, high common mode rejection ratio, low current and voltage offset is the μA714. Typical V_{OS} is 10 μV with dV_{OS}/dt at 0.3 μV/ °C. It can be used in all precision op amp applications and does not require null potentiometers. In instrumentation systems, it can replace chopper-stabilized amplifiers, improving performance and noise characteristics. Other uses include differential input amplifier, precision reference amplifier, absolute value amplifier, and DAC summing amplifier applications.

NEGATIVE ADJUSTABLE VOLTAGE REGULATOR PROVIDES 5 A OUTPUT

Capable of supplying over 5 A over a -24 V to -2.2 V, output range, the μA79HG is a new hybrid voltage regulator with all of the characteristics of a monolithic 4-terminal adjustable voltage regulator. It features internal current limiting, low drop-out voltage, and power dissipation of 50 W. The regulator is a monolithic voltage regulator chip with a discrete series-pass element and short-circuit detection transistors, packaged in the popular TO-3 can.

NEW SCHOTTKY FPLAs AVAILABLE

Two new high-speed Field Programmable Logic Arrays have joined the bipolar LSI line - the 93458 and 93459 16 x 48 x 8 Isoplanar FPLAs. Each circuit has 16 inputs, 48 product terms, and eight outputs. Both circuits have the 16 inputs with their complements fuse-linked to the inputs of 48 AND gates for 48 product terms and the inputs of the 48 AND gates fuse-linked to eight 48-input OR gates for eight summing terms. Any of the outputs may be programmed either HIGH or LOW, and are enabled when Chip Select is LOW. The devices are identical except for the output stages with the 93458 featuring uncommitted collector outputs and the 93459 featuring 3-state outputs.

STANDARD CONTROL MODULES EMERGE

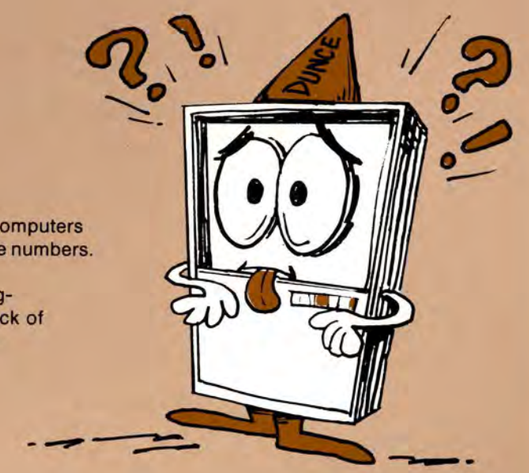
Based on the FCM7040 control circuit, a line of standard control modules is being developed by Fairchild Microsystems. The first module is a general-purpose controller designated the Model 760. This unit has the potential of providing as many as 20 inputs, four controlled ac power outputs, one comparator input, on audible output, drive for a 4-digit display and 10 LED indicators. Applications are quite broad because different ROM patterns can be used to allow different types of input data and control commands. Typical uses are for washer/dryer controls, dark room controls, microwave oven controls, or any number of appliance control situations.

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send us your old label (or copy it) including the most important part, the code numbers on the side. Computers are funny machines, least ours is; they run strictly by the numbers.

Naturally, we want to save money by not wasting Progress copies and postage, but we also want to keep track of you. So — if you will remember this one little request, we will be very grateful.



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