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Low power Schottky TTL combines the best qualities of high speed TTL (74N, even 74H) and low power 93L. Available from several manufacturers, LSTTL is fast becoming a replacement for standard TTL. In fact, over the rest of this decade, it will dominate TTL designs and by 1980 will be the lowest cost TTL family. The feature this month describes the low power Schottky TTL concept and explains its many advantages over conventional TTL. Some interesting background material is also included on the Schottky barrier diode and the man who gave it its name.

Many monolithic 3-terminal regulators are available with current capabilities up to 1.5 amps, but what about the designer who requires one for higher currents A hybrid 3-terminal regulator with a 5-amp output-current capability, now available, is the subject of the second article.

The inherent capability of charge-coupled devices to manipulate information in the form of charge packets makes the CCD technology ideal for analog signal processing. The third article introduces the first in a series of CCD analog shift registers designed specifically for systems that require complex manipulation of analog information.

Next is a brief overview of available interface circuits for CMOS systems. These include both CMOS and bipolar ICs, the latter often overlooked by the designer.

Circuit Ideas presents a practical approach to high speed multiplication of word lengths up to 24 bits. The 8 x 8 multiplication scheme shown has a typical multiplying time of 68 nanoseconds.

This month's New Products section highlights a programmer, used in conjunction with the Qualifier™ 901 tester to create and modify device testing programs. Developed by Fairchild Systems Technology, the *Programmer* is a compact unit that mounts easily on any teletypewriter stand and provides the user with a method to write his own special programs. Also discussed are two new UHF prescalers and two pairs of very fast 2048-bit and 4096-bit field-programmable ROMs (PROMs).

In this issue
The basic Schottky-transistor schematic creates interesting shapes for the cover photographs that show a variety of low power Schottky applications.

PROGRESS

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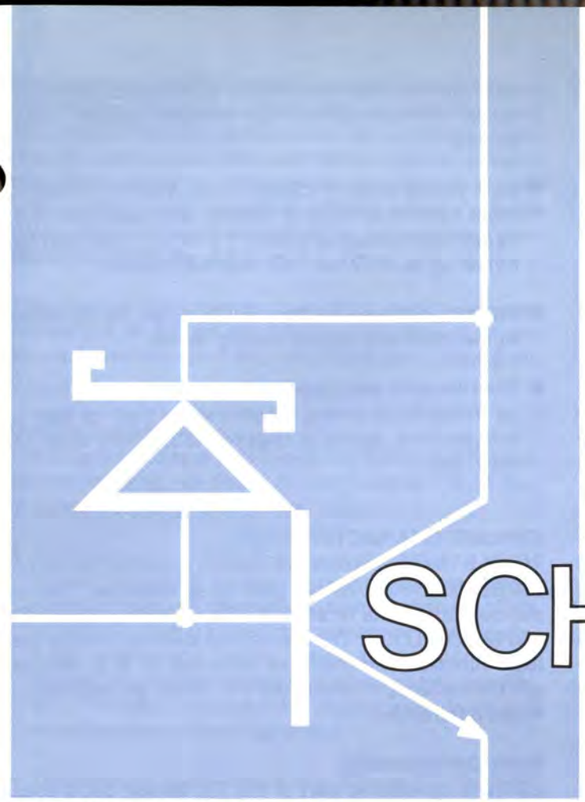


LOW POWER SCHOTTKY TTL

by Peter Alfke and Charles Alford

For many years TTL has been the most popular digital integrated circuit technology, offering a good compromise between cost, speed, power consumption and ease of use. As the price of TTL circuits decreased and the average IC complexity increased to MSI (medium scale integration), the cost and size of the power supply and the difficulty of removing the heat dissipated in the TTL circuits became increasingly important factors. Recent improvements in semiconductor processing have made it possible to not only reduce TTL power consumption significantly, but also to improve the speed over that of standard TTL.

The 9LS low power Schottky TTL family combines a current and power reduction by a factor of 5 (compared to 7400 TTL) with anti-saturation Schottky diode clamping and advanced processing. Shallower diffusions and higher sheet resistivity are used to achieve circuit performance better than conventional TTL. With a full complement of popular TTL functions available in 9LS and in the new, more complex and powerful LSI MACROLOGIC™ TTL circuits*, low power Schottky is destined to become the dominating TTL logic family.

9LS represents more than just a conventional speed versus power trade-off. This is best illustrated by *Figure 1* which compares 9LS to other TTL technologies. Note that 9LS dissipates eleven times less power than 9S or 74S, suffering a delay increase of only 1.7 times.

*Macrologic, PROGRESS, Vol. 3, No. 2, March/April 1975.

The 9L low power non-Schottky family by comparison also dissipates eleven times less power than 74H, and 74L dissipates ten times less power than 74N, but both suffer a delay increase of 3.4 times.

The performance of 9LS is not just the result of Schottky clamping. 9LS is four times faster than 9L at the same power dissipation, while 9S and 74S are only two times faster than 74H at the same power. The new and higher level of efficiency exhibited by 9LS is the result of advanced processing, which provides better switching transistors with no sacrifice in manufacturability.

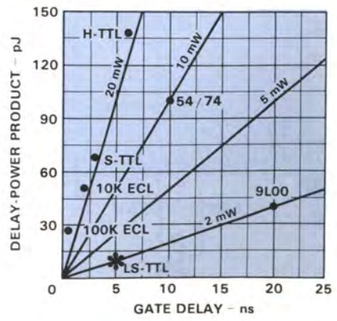


Fig. 1. Delay-Power Product for Popular Logic Families

To the system designer the advantages of this new TTL family are many:

- Less supply current allows smaller, cheaper power supplies, reducing equipment cost, size and weight.
- Lower power consumption means less heat is generated, which simplifies thermal design. Packing density can be increased or cooling requirements reduced, or perhaps both. The number of cooling fans can be reduced, or slower, quieter ones substituted.
- Reliability is enhanced, since lower dissipation causes less chip temperature rise above ambient; lower junction temperature increases MTBF. Also, lower chip-current densities minimize metal related failure mechanisms.
- Less noise is generated, since the improved transistors and lower operating currents lead to much smaller current spikes than standard TTL; consequently, fewer or smaller power supply decoupling capacitors are needed. In addition, load currents are only 25% of standard TTL and 20% of HTTL; therefore, when a logic transition occurs, the current changes along signal lines are proportionately smaller, as are the changes in ground current. Rise and fall times, and thus wiring rules, are the same as for standard TTL and more relaxed than for HTTL or STTL.
- Simplified MOS to TTL interfacing is provided, since the input load current of LSTTL is only 25% of a standard TTL load.
- Ideally suited for CMOS to TTL interfacing. All Fairchild CMOS and most other 4000 or 74C CMOS are designed to drive one 9LS input load at 5.0 V. The 9LS can also interface directly with CMOS operating up to 15 V due to the high voltage Schottky input diodes.
- Best TTL to MOS or CMOS driver. With the modest input current of MOS or CMOS as a load, any 9LS output will rise up to within 1 V of V_{CC}, and can be pulled up to 10 V with an external resistor.
- Interfaces directly with other TTL types, as indicated in the input and output loading tables.
- The functions and pinouts are the same as the familiar 7400/9300 series, which means that no extensive learning period is required to become adept in their use.

CIRCUIT CHARACTERISTICS

The 9LS circuit features are easiest explained by using the 9LS00 2-input NAND gate as an example. The input/output circuits of all 9LS TTL, including, SSI, MSI and MACROLOGIC TTL are almost identical. While the logic function and the base structure of 9LS circuits are the same as conventional TTL, there are also significant differences.

Input Configuration

LSTTL is considered part of the TTL family, but it does not use the multi-emitter input structure that originally gave TTL its name. All 9LS TTL, with the exception of some early designs*, employ a DTL-type input circuit with Schottky diodes to perform the AND function. Compared to the classical multi-emitter structure, this circuit is faster and it increases the input breakdown voltage to 15 V. Each input has a Schottky clamping diode that conducts when an input signal goes negative, as indicated by the input characteristic of *Figure 3*.

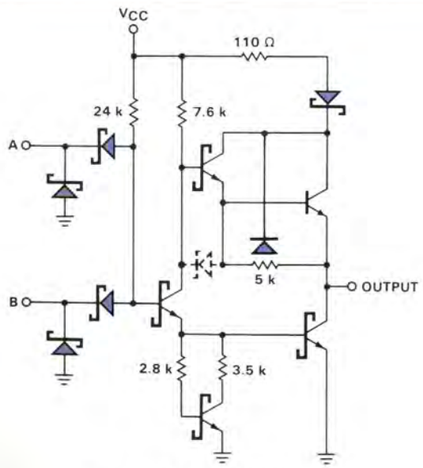


Fig. 2. 2-Input NAND Gate

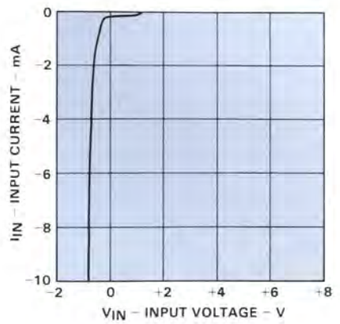


Fig. 3. Typical Input Current-Voltage Characteristic

*The 9LS03, 05, 22, 74, 109, 112, 113 and 114 use transistor inputs at present, but will be redesigned by the first part of 1976 to incorporate diode inputs.

This helps to simplify interfacing with those MOS circuits whose output signal tends to go negative. For a long TTL interconnection, which acts like a transmission line, the clamp diode acts as a termination for a negative-going signal and thus minimizes ringing. Otherwise, ringing could become significant when the finite delay along an interconnection is greater than one-fourth the fall time of the driving signal.

The effective capacitance of an LSTTL input is approximately 3.3 pF. For an input that serves more than one internal function, each additional function adds 1.5 pF.

Output Configuration

The output circuits of 9LS low power Schottky TTL have several features not found in conventional TTL. A few of these features are discussed below.

- The base of the pull-down output transistor is returned to ground through a resistor-transistor network instead of through a simple resistor. This squares up the transfer characteristics since it prevents conduction in the phase-splitter until base current is supplied to the pull-down output transistor. This also improves the propagation delay and transition time. (See *Figure 4*)
- The output pull-up circuit is a 2-transistor Darlington circuit with the base of the output transistor returned through a 5 kΩ resistor to the output terminals, unlike 74H and 74S where it is returned to ground which is a more power consuming configuration. This configuration allows the output to pull up to one V_{BE} below V_{CC} for low values of output current.
- As a unique feature, the 9LS outputs have a Schottky diode in series with the Darlington collector resistor. This diode allows the output to be pulled substantially higher than V_{CC}, e.g., to +10 V, convenient for interfacing with CMOS. For the same reason, the parasitic diode of the base-return resistor is connected to the Darlington common collector, not to V_{CC}. Some early 9LS designs – the 9LS00, 02, 04, 10, 11, 20, 32, 74, 109, 112, 113 and 114 – do not have the diode in series with the Darlington collector resistor. These outputs are, therefore, clamped one diode drop above the positive supply voltage V_{CC}. These older circuits also contain a "speed-up" diode that supplies additional phase-splitter current while the output goes from HIGH to LOW, and also limits the maximum output voltage to one diode drop above V_{CC}. Since this is the fastest transition even without additional speed-up, this diode is omitted in all new designs.

Output Characteristics

Figure 5 shows the LOW state output characteristics. For low I_{OL} values, the pull-down transistor is clamped out of deep saturation to shorten the turn-off delay. The curves also show the clamping effect when I_{OL} tends to go negative, as it often does due to reflections on a long interconnection after a negative-going transition. This clamping effect helps to minimize ringing.

The waveform of a rising output signal resembles an exponential, except that the signal is slightly rounded at the beginning of the rise. Once past this initial rounded portion, the starting-edge rate is approximately 0.5 V/ns with a 15 pF load and 0.25 V/ns with a 50 pF load. For analytical purposes, the rising waveform can be approximated by the following expression.

$$v(t) = V_{OL} + 3.7\,[1 - \exp(-t/T)]$$

where

$T = 8$ ns for $C_L = 15$ pF and 16 ns for $C_L = 50$ pF

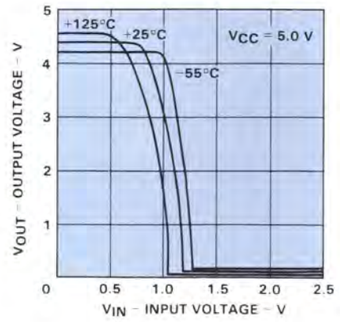


Fig. 4. Typical Output vs Input Voltage Characteristic

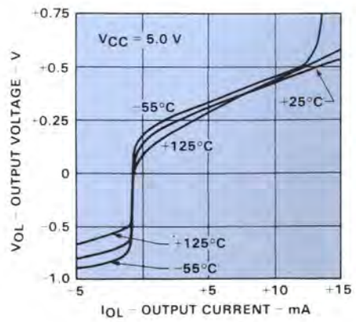


Fig. 5. Typical Output Current-Voltage Characteristic

The waveform of a falling output signal resembles that part of a cosine wave between angles of 0° and 180°. Fall times from 90% to 10% are approximately 4.5 ns with a 15 pF load and 8.5 ns with a 50 pF load. Equivalent edge rates are approximately 0.8 and 0.4 V/ns respectively. For analytical purposes, the falling waveform can be approximated by the following.

$$v(t) = V_{OL} + 1.9\,u(t)\,[1 + \cos \omega t] - 1.9\,u(t-a)\,[1 + \cos \omega(t-a)]$$

where

$u(t) = 0$ for $t < 0$
$= 1$ for $t > 0$

and

$u(-a) = 0$ for $t < a$
$= 1$ for $t > a$

For t in nanoseconds and $C_L = 15$ pF, $a = 7.5$ ns, $\omega = 0.42$

For $C_L = 50$ pF, $a = 14$ ns, $\omega = 0.23$

AC Switching Characteristics

Low power Schottky TTL gates have an average propagation delay of 5 ns measured under the traditional 15 pF load. At higher capacitive loads, the delay increases at a rate of less than 0.1 ns/pF, as shown in *Figure 6*. Although some drive capability is lost by using high value resistors and small transistor geometries in LSTTL, actually more drive is gained by using non-gold doped transistors with much higher current gain than those in conventional TTL. Even at 200 pF load, TTL circuits are still faster than "full power" TTL such as 9000, 7400, 5400.

Figure 7 shows the power dissipation of various logic families as a function of the input frequency. Under static conditions, only CMOS uses less power than LSTTL, but CMOS loses this advantage when operating at more than a few 100 kHz. At speeds over 1 MHz, LSTTL is the most efficient logic.

The delay times of LSTTL are rather insensitive to variations in temperature and supply voltage, as shown in *Figures 8* and *9*. The average propagation delay changes less than 2 ns over the full military temperature range, less than 1 ns over the commercial temperature range, less than 1 ns over the military supply voltage range, and less than 0.5 ns over the commercial voltage range. Compare this to standard TTL where changes of 6 ns over temperature and several ns over supply voltage are typical. As a result, the designer can use the guaranteed maximum delay values with much more confidence and less additional worst-case derating.

INTERCONNECTION DELAYS

For those parts of a system in which timing is critical, designers should take into account the finite delay along the interconnections. This delay ranges from about 0.12 to 0.14 ns/inch for the type of interconnections normally used in TTL systems. Exceptions occur when using ground planes with STTL to reduce ground noise during a logic transition; ground planes give higher distributed capacitance and delays of about 0.15 to 0.22 ns/inch.

Most interconnections on a logic board are short enough that the wiring and load capacitance can be treated as a lumped capacitance for purposes of estimating their effect on the propagation delay of the driving circuit. When an interconnection is so long that its delay is one-fourth to one-half of the signal transition time, the driver output waveform exhibits noticeable slope changes during a transition. This is evidence that during the initial portion of the output voltage transition, the driver sees the characteristic impedance of the interconnection (normally 150 Ω to 200 Ω) which, for transient conditions, appears as a resistor returned to the quiescent voltage existing just before the beginning of the transition. This characteristic impedance forms a voltage divider with the driver output impedance, tending to produce a signal transition having the same rise or fall time as in the no-load condition but with a reduced amplitude. This attenuated signal travels to the far end of the interconnection, which is essentially an unterminated transmission line, whereupon the signal starts doubling. Simultaneously, a reflection voltage is generated which has the same amplitude and polarity as the original signal; *e.g.,* if the driver output signal is positive-going, the reflection will be positive going and, as it travels back toward the driver, it adds to the line voltage. At the instant the reflection arrives at the driver, it adds algebraically to the still-rising driver output, accelerating the transition rate and producing the noticeable change in slope.

If an interconnection is of such length that its delay is longer than half the signal transition time, the attenuated output of the driver has time to reach substantial completion before the reflection arrives. In the limit, the waveform observed at the driver output is a 2-step signal with a pedestal. In this circumstance, the first load circuit to receive a full signal is the one at the far end, because of the doubling effect, while the last one to receive a full signal is the one nearest the driver since it must wait for the reflection to complete the transition. Thus, in a worst-case situation, the net contribution to the overall delay is twice the delay of the interconnection because the initial part of the signal must travel to the far end of the line and the reflection must return.

When load circuits are distributed along an interconnection, the input capacitance of each will cause a small reflection having a polarity opposite that of the signal transition; and each capacitance also slows the transition rate of the signal as it passes by. The series of small reflections, arriving back at the driver, is subtractive and has the effect of reducing the apparent amplitude of the signal. The successive slowing of the transition rate of the transmitted signal means that it takes longer for the signal to rise or fall to the threshold level of any particular load circuit. A rough but workable approach is to treat the load capacitances as an increase in the intrinsic distributed capacitance of the interconnection. Increasing the distributed capacitance of a transmission line reduces its impedance and increases its delay. A good approximation for ordinary TTL interconnections is that distributed load capacitance decreases the characteristic impedance by about one-third and increases the delay by one-half.

Another advantage of LSTTL is its higher output impedance during a positive-going transition. Whereas the low output impedance of STTL and HTTL allows these circuits to force a larger initial swing into a low impedance interconnection, the low output impedance also has a disadvantage. It makes the reflection coefficient negative at the driven end of the interconnection whenever a transmission line is terminated by an impedance lower than the characteristic impedance. Therefore, when the reflection from the essentially open end of the interconnection arrives back at the driver, it will be "re-reflected" with the opposite polarity. The result is a sequence of reflected signals which alternate in sign and decrease in magnitude, commonly known as ringing. The lower the driver output impedance, the greater the amplitude of the ringing and the longer it takes to damp out.

On the other hand, the output impedance of LSTTL is closer to the characteristic impedance of the interconnections commonly used with TTL, and ringing is practically non-existent. Thus no special packaging is required. This advantage, combined with excellent speed, modest edge rates and very low transient currents, are some of the reasons that designers have found LSTTL extremely easy to work with and very cost effective.

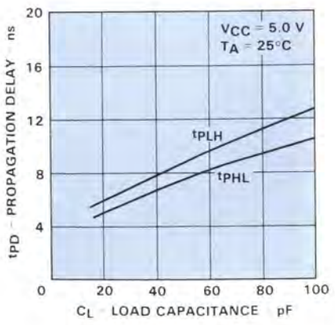


Fig. 6. Typical Propagation Delay vs Load Capacitance

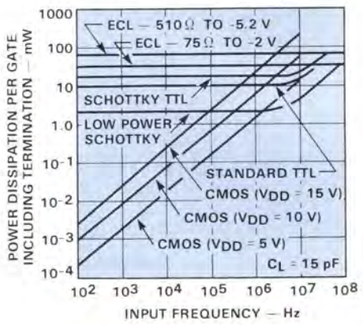


Fig. 7. Typical Power Dissipation vs Input Frequency for Several Popular Logic Families

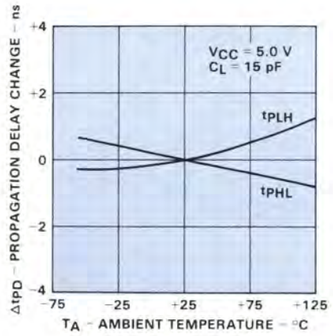


Fig. 8. Propagation Delay Change with Temperature

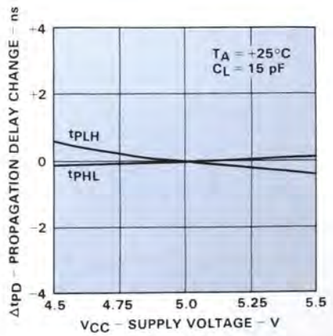


Fig. 9. Propagation Delay Change with Supply Voltage

UNUSED INPUTS

For best noise immunity and switching speed, unused AND or NAND-gate inputs should not be left floating, but should be held between 2.4 V and the absolute maximum input voltage. Two possible ways of handling these unused inputs are:

Connect an unused input to V_{CC}. Most 9LS inputs have a breakdown voltage > 15 V and require, therefore, no series resistor. For all multi-emitter conventional TTL inputs, a 1 to 10 kΩ current-limiting series resistor is recommended to protect against V_{CC} transients that exceed 5.5 V.

Connect an unused input to the output of an unused gate that is forced HIGH.

Note, do not connect an unused LSTTL input to another input of the same NAND or AND function. This method, although recommended for normal TTL, increases the input coupling capacitance and therefore reduces the ac noise immunity.

WHAT IS A SCHOTTKY DIODE?

A Schottky diode, also called a "hot carrier diode", offers two big advantages over the conventional pn-junction diode – very high speed due to extremely short recovery time and a substantially lower forward-voltage drop for a given current, or an order-of-magnitude higher current for the same voltage.

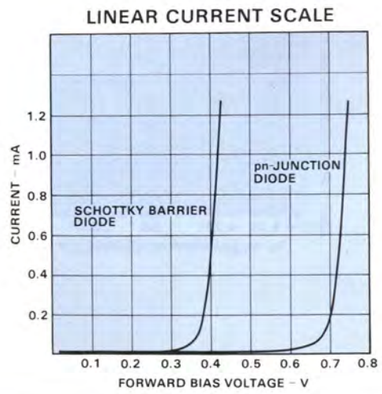
The more familiar pn-junction diode that exists at the boundary of two differently doped sections inside a semiconductor crystal relies on *minority* carriers for current transport. In contrast, a Schottky diode is formed by the metal-to-semiconductor contact at the surface of the semiconductor crystal and relies on *majority* carriers for current transport (electrons in the case of n-type semiconductor). Charge storage is negligible and forward-to-reverse recovery is extremely fast.

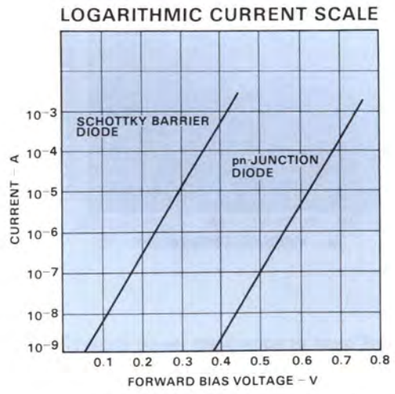
Metal-semiconductor contacts can be classifed into two groups according to their current/voltage characteristics. Those contacts with a *linear* characteristic are called ohmic and are used extensively in monolithic integrated circuits for interconnecting the various components on a chip. Those with a *non-linear* rectifying characteristic are called Schottky barrier diodes. Whether a metal-semiconductor contact is ohmic or rectifying, *i.e.,* has linear or non-linear characteristics, depends on the properties of the metal and on the doping level and the type of the semiconductor.

The rectifying non-linearity of a Schottky diode results from the presence of a potential barrier at the metal-semiconductor interface, which the carriers must surmount by thermionic emission before they can flow through the junction. The barrier potential can be reduced by forward bias (metal more positive than the n-type semiconductor) to increase the carrier flow from the semiconductor into the metal. Under reverse bias, the Schottky diode behaves similarly to a pn-junction diode; the reverse current is small and almost voltage independent unless the breakdown voltage is exceeded.

The Schottky barrier height is always less than the energy gap of the semiconductor. Thus, for a given voltage, the current flowing in a Schottky barrier diode is orders-of-magnitude larger than in a pn diode of the same area; but, the forward current follows the same exponential law, doubling for every increase of 18 mV in forward voltage, *i.e.,* increasing tenfold for every voltage increase of 60 mV (See Figure).

Rectifying metal-semiconductor contacts were discovered and investigated by Ferdinand Braun in 1874. Despite many attempts to understand their current-flow mechanism, the correct physical model was not discovered until half a century later by Walter Schottky. Researchers at Bell Labs in the late forties were investigating metal-semiconductor interfaces when they accidentally discovered the transistor. From then on, most efforts in the semiconductor industry have been directed toward pn-junction devices. Only in the past six or seven years have manufacturers gained the understanding of surface phenomena and developed the metallization techniques required to produce reliable Schottky barrier diodes.





WHY SCHOTTKY TTL?

With the use of Schottky diodes, the saturation delay normally encountered in saturated logic (TTL, DTL and RTL) can be avoided. These logic families operate by turning their transistors either fully on or fully off. The amount of base current applied to turn on a transistor is critical. Too little current will not turn the transistor on sufficiently. Too much current will turn the transistor on quickly; however, when the base current is interrupted, the transistor continues to conduct until the excess charge in the base disappears, usually through thermal recombination.

The designer of saturated logic circuits therefore faces a problem. He must design the circuit parameters so that each transistor receives sufficient base current even under the worst-case combination of manufacturing tolerances–positive resistor tolerances and low transistor current gain(beta)–and environmental conditions –low supply voltage, low temperature that reduces beta and increases V_{BE}, and high fan-out that increases the collector current of the output stage. On the other hand, he must be concerned about overdriving the transistor and causing excessive saturation delays under the opposite worst-case conditions–negative resistor tolerances, high beta, low V_{BE}, high temperature, high supply voltage and low fan-out–where the transistor may receive ten times more base current than required.

Conventional TTL circuits use gold doping to increase the probability of thermal base-charge recombination, thus decreasing saturation delay; but, this also lowers beta and makes the circuit less efficient. As early as 1955, an elegant circuit trick, the Baker clamp, was developed to overcome this problem. A diode is connected between the base and the collector; originally a germanium diode was used. If this diode has a very low forward-voltage drop, it starts conducting when the collector becomes slightly forward biased with respect to the base. The excess current applied to the base terminal of the transistor then flows through this diode into the collector. The transistor only receives the base current necessary to pull the collector into the "soft saturation" region. There is no excess charge storage and the saturation delay is non-existent.

At first, monolithic integrated circuits could not use this trick, since no pn-junction diode was available with a voltage drop significantly lower than that of the base-emitter diode. The Schottky barrier diode, however, has this desirable characteristic. By 1970, a great deal of progress had been made in the understanding and manufacturing of these diodes. Metal-silicide and refractory-metal contacts assured high temperature stability and the surface effects of silicon were better understood and controlled. All the major TTL manufacturers introduced a line of Schottky TTL circuits where all the transistors that normally would be saturated are equipped with anti-saturation Schottky barrier clamp diodes. These Schottky TTL circuits are very fast; but, since the emphasis is on speed, they consume more power than normal TTL and their short rise and fall times cause interconnection problems.

Low power Schottky TTL consumes one-quarter the current and power of conventional TTL and uses Schottky diode clamping and advanced processing to regain the speed that is lost because of the lower internal charging currents. The 9LS family offers performance superior to conventional TTL while saving 75% of the power dissipation.

WHO IS MR. SCHOTTKY?

"Schottky" has become a semiconductor household word, yet how many engineers know the man behind the name? Is he

1. a famous soviet scientist, inventor of **ТТЛ ЛОГІК**?
2. one of the three Nobel prize winners from Bell Labs who invented the transistor in 1948?
3. a German physicist who invented the screen-grid tube in 1915?
4. a research scientist with one of the leading U.S. semiconductor manufacturers?

If you checked 1, 2 or 4, you are wrong, but this would not be surprising for we researched several libraries before we found only the briefest biographical information on Walter Schottky.

He was born in June 1886 in Zürich, Switzerland, where his father, a well known German mathematician, had a teaching assignment. Walter Schottky received doctorates in engineering and natural sciences from the University of Berlin and spent several years as a professor at the universities of Würzburg and Rostock. He also worked in the research department of Siemens, the German telecommunications giant.

Most of his early research dealt with electrons and ions in vacuum tubes. He invented the screen-grid tube in 1915 and later discovered an irregularity in the emission of thermions, known as the "Schottky effect"–the reduction in the minimum energy required for electron emission under the influence of an electrical field. During the thirties, Walter Schottky worked mainly on the theory of semiconductor physics which, at that time, had the bad reputation of being the "physics of dirt effects" or the study of "order-of-magnitude effects". Semiconductors such as selenium and copper-oxide rectifiers, overvoltage protectors and photovoltaic cells were used commercially but there was no clear understanding of their theory of operation. Walter Schottky established the boundary-layer theory for crystal rectifiers that explains how special concentration and potential conditions exist in the boundary layer of the semiconductor and how these conditions depend on the current through the rectifying junction.

Walter Schottky remained active in semiconductor research for several decades until his death in 1956. He wrote several books, few if any translated into English, and published many articles in scientific journals, *e.g.*, Zeitschrift für Physik and Annalen der Physik.

High Power 3-Terminal Voltage Regulator

by Len Arguello

As the trend toward smaller equipment increases and higher volumetric efficiency becomes more important in overall system design, power supply requirements increase accordingly. The monolithic voltage regulator, because of its high performance and reliability, cost effectiveness, and ease of use has become an integral part of most system designs. Three-terminal regulators are available covering the voltage range from 2.6 to 24 V, with current capability from 100 mA to 1.5 A. To meet the demands for variable voltages or non-standard voltage options, two pairs of 4-terminal adjustable regulators rated at 500 mA and 1 A respectively have been introduced.*

But, what about the designer who needs a voltage regulator with higher current capability? He has thus far been forced to add external components to a basic voltage regulator – anywhere from a single series pass device to several components – depending upon his requirements such as thermal protection, current limiting, etc.

Now, the 78H05 *(Figure 1)* is available with a 5 A output current capability. It is a hybrid integrated circuit offering all the inherent characteristics of the monolithic 3-terminal voltage regulator, *i.e.,* full thermal and short circuit protection, and is packaged in a standard TO-3 providing 50 W power dissipation. The 78H05 voltage regulator is intended for a wide range of systems where a regulated 5 V supply is required and can be used for a variety of on-card regulation and circuit isolation applications.

VOLTAGE REFERENCE

Until recently, the normal voltage reference used in a voltage regulator was a temperature-compensated Zener diode, However, it is limited to a breakdown voltage greater than 6 V, thus imposing a lower limit on the input voltage to the regulator. Zeners also require excessively tight process control to maintain a satisfactory tolerance for non-adjustable regulator applications.

A voltage reference that does not use a Zener diode has been developed from the predictable temperature, current and voltage relationships in an emitter-base junction. To obtain a temperature-compensated reference voltage, the positive temperature coefficient of an emitter-base voltage differential between two transistors operated at different current densities is added to the negative temperature coefficient of emitter-base voltage. *Figure 2* shows such a reference. Transistor Q1 operates at a considerably higher current level than Q2 and the emitter-base voltage differential is amplified by the voltage gain of transistor Q2.

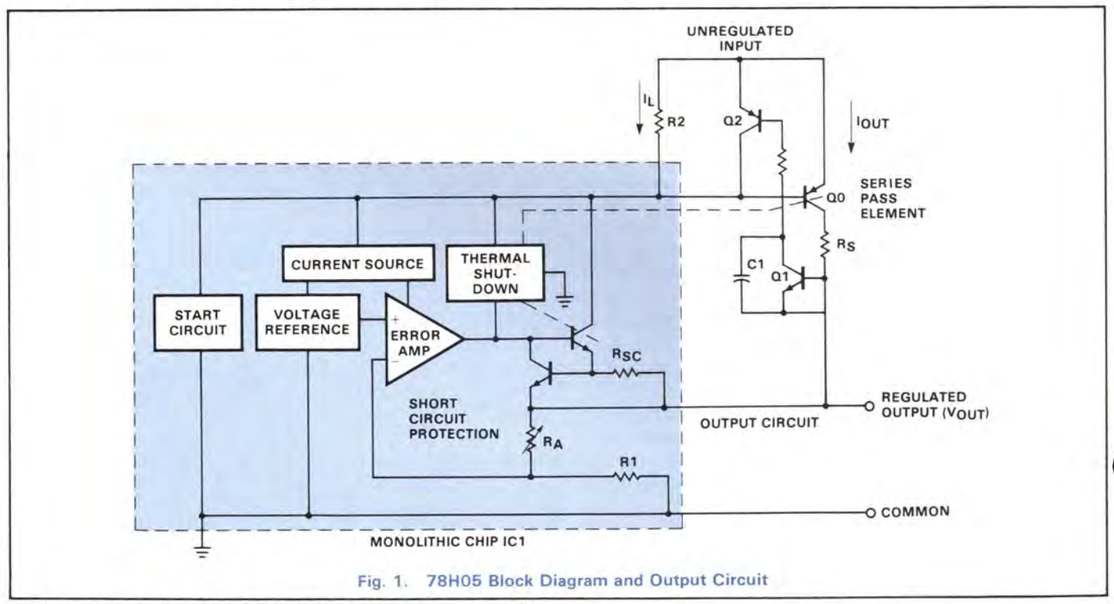


Fig. 1. 78H05 Block Diagram and Output Circuit

*"4-Terminal Variable Regulators," PROGRESS, Vol 3, No. 1, Jan./Feb. 1975

The reference voltage can be expressed as follows.

$$V_{REF} = V_{BE3} + I_{CQ2}\ R2 + I_{BQ3}\ R2$$

$$V_{REF} = V_{BE3} + \frac{R2}{R3}\ (\Delta V_{BE}) + I_{BQ3}\ R2$$

$$V_{REF} = V_{BE3} + \frac{R2}{R3}\ \left(\frac{KT}{q}\ \text{Ln}\ \frac{J1}{J2}\right) + I_{BQ3}\ R2$$

$$V_{REF} \cong V_{BE3} + \frac{R2}{R3}\ \left(\frac{KT}{q}\ \text{Ln}\ \frac{R2}{R1}\right)$$

where J = current density
K = Boltzmann's constant
T = ° Kelvin
q = Electron charge

By selecting the resistor ratios R2:R3 and R2:R1, a low voltage, temperature-compensated reference is obtained.

$$\frac{KT}{q} \approx 0.026\ \text{V at } 300°K$$

Figure 3 shows a simplified schematic of the actual circuit used in the regulator. The base-emitter drops of Q4, Q5 and Q6 have been added to increase the reference level to 5 V. The reference then becomes:

$$V_{REF} = (V_{BE3} + V_{BE4} + V_{BE5} + V_{BE6}) + \frac{R2}{R3}\left(\frac{KT}{q}\ \text{Ln}\ \frac{R2}{R1}\right)$$

Resistors R1, R2 and R3 are selected so that the reference voltage is constant over the temperature range and also has a nominal value of 5 V at room temperature.

A very tight reference voltage tolerance is, therefore, obtained without special process controls. This is because base-emitter characteristics are better understood and more predictable than Zener references. Also, monolithic circuits lend themselves more readily to resistor and transistor matching than to generating absolute values of resistance. An external adjustment to trim output voltage is unneccesary in most applications. An additional benefit is that this reference has low noise output compared to a Zener reference, thus eliminating the need for a large bypass capacitor to remove noise.

ERROR AMPLIFIER

An error amplifier (see *Figure 1*) compares the output feedback signal with the voltage reference and corrects the output by the amount of the error. The regulator circuit shown in *Figure 3* has the error amplifier combined with the voltage reference. The advantage is that noise at the regulator output is minimized since the amplifier and reference are no longer separate sources of noise. In *Figure 3*, transistor Q3 is used as the error amplifier; and at the same time, its base-emitter voltage is used as part of the reference.

A current source is used as the active load to the error amplifier. A negative feedback path is provided through feedback resistors R4 and R5. If the voltage at the output increases due to a reduction in load current, that voltage change is transmitted to the base of transistor Q3. Transistor Q3 then conducts more, effectively reducing the base drive to the output transistor by current steering. The result is a decrease in output voltage, which tends to correct the change in output voltage due to the load current change. As the loop settles, an equilibrium value at the output is reached. The output voltage is derived using the following formula.

$$\text{Output Voltage} = V_{REF}\ \left(\frac{R4 + R5}{R5}\right)$$

Varying the resistor ratio (R4 + R5): R5 yields different fixed output voltages.

THERMAL OVERLOAD PROTECTION

One of the benefits of including the series pass transistor on the common substrate is that it is then possible to incorporate both thermal and current overload protection. Low power

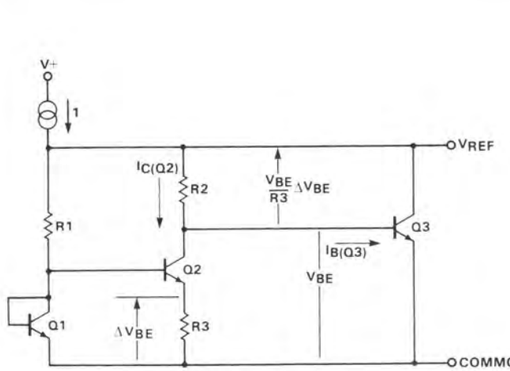


Fig. 2. Voltage Reference Based on Base-Emitter Voltage

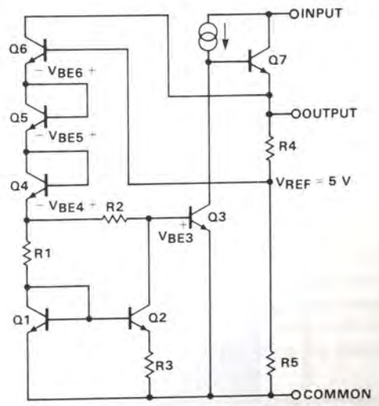


Fig. 3. Simplified Circuit for the Regulator

IC regulators usually rely on current limiting for overload protection as there is no practical way to sense junction temperature in a separate pass transistor. As a result, excessive heating of the pass transistor is one of the primary failure mechanisms of solid-state regulators. A thermal overload protection circuit in a hybrid regulator with the pass transistor on a common substrate limits the maximum temperature of the transistor junction. This limiting is independent of input voltage, the type of overload or degree of package heat sinking.

The base-emitter junction of a transistor is used to sense the temperature of the series pass device. The temperature limiting transistor normally is biased below its conduction threshold so that it does not affect normal circuit operation. If the pass-device temperature rises to its maximum limit due to a load fault or other condition, the temperature limiting transistor turns on. This removes the base drive to the output transistors and shuts down the regulator, preventing further chip heating.

OUTPUT CIRCUIT (See Figure 1)
Output voltage V_{OUT} is derived from the monolithic chip IC1 which is also a reference as well as a buffer and driver for the output stage. When a load is placed across the output terminals, the load current supplied by IC1 is sensed by resistor R2, which then develops a voltage drop that forward biases the emitter-base junction of Q0. At this time, IC1 begins to supply base current to Q0, which supplies the bulk of the load current (≈95%) during operation. The output circuit is designed so that the worst-case current requirement of the Q0 base added to the current through R2 always remains below the current limit threshold of IC1. Resistor R_S in conjunction with Q1 and Q2 make up a current-sense and limit circuit to protect the series pass device from excessive current drain. As the output current begins to increase, the voltage drop across R_S starts to forward bias the emitter-base junction of Q1. As Q1 conducts, its collector current flows through the Q2 base; thus Q2 begins to conduct and therefore shunts away some of the current available to the base of Q0. This process continues until a natural state of electrical equilibrium is reached, at which time the 78H05 is in a current-limit mode of operation. Capacitor C1 provides frequency stability by adding a pole in the output-circuit transfer function that lowers the overall loop gain below the critical levels at high frequencies.

78H05 CONSTRUCTION
The 78H05 voltage regulator is constructed using state-of-the-art hybrid circuit technology and is packaged in a hermetically sealed TO-3. A beryllium-oxide substrate is used in conjunction with an isothermal layout to optimize the thermal characteristics of the device and still maintain electrical isolation between the various chips. This ensures nearly ideal thermal transfer between the series pass device and the temperature sensing circuit within IC1, thus providing the thermal-limiting feature. All active chips are gold-eutectic attached to the beryllium-oxide substrate. The substrate is reflow soldered onto a solid copper slug that fits within the cavity of the TO-3 header aluminum base. This process guarantees junction-to-case thermal impedances in the order of 1.5 to 2°C/W thereby providing package dissipation as high as 50 W at 25°C case temperature. Output voltage sensing is performed at the device output pin, so that the error amplifier can correct for any output voltage errors caused by finite impedances in the output circuit, *i.e.*, lead bonds, metal traces, etc. Some 78H05 typical characteristics and applications are shown in *Figures 4* and *5* respectively.

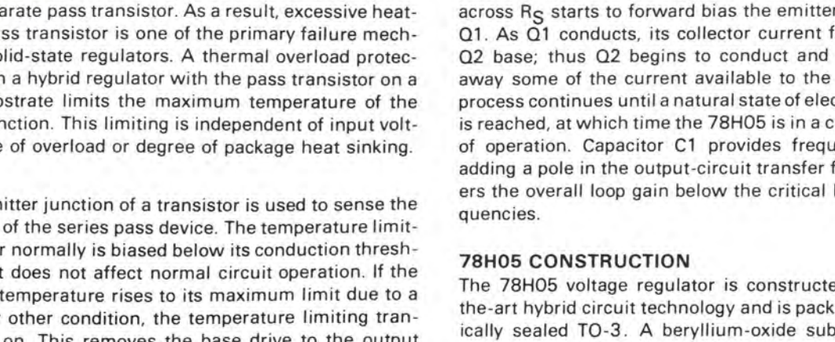
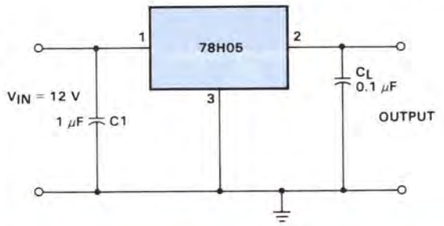


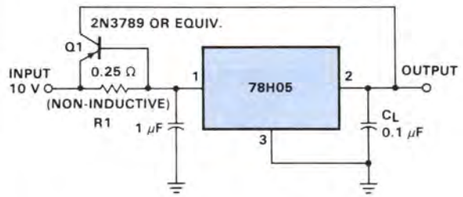
Fig. 4. Typical Characteristic Curves

Fixed Output 5 A Regulator



This is the basic application for the 78H05 and can be used when a fixed 5 V output is required with 5 A current capability. The input capacitor C1, as well as C_L, are required for stability when the regulator is placed at some distance from the main power source. C_L and C1 should be attached as close as possible to the 78H05 socket.

10+ A Regulator



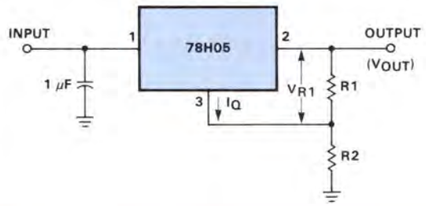
For applications requiring output current in excess of that offered by the basic device (5 A), the circuit shown can be used. The value of R1 determines the point at which Q1 begins to conduct, thus bypassing the regulator. In this circuit, the 78H05 is used as a high current reference device, and the overall circuit does not offer short circuit protection. The maximum current capability of this circuit can be defined as:

$$I_{O(MAX)} = \left[I_{SC} - \frac{V_{BE1}}{R1}\right] \beta_{Q1(MIN)}$$

where:

I_{SC} = 78H05 short circuit current

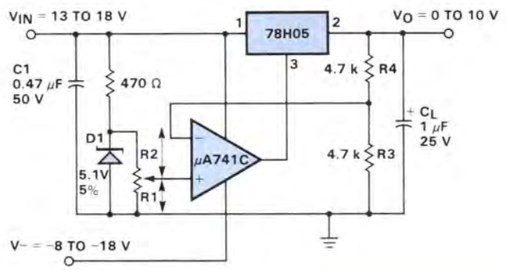
Increased Output Voltage



In this circuit, a voltage pedestal developed across R2 is added to the normal regulated output V_{R1} to provide an output voltage that can be described by the following:

$$V_{OUT} = V_{R1}\left(1 + \frac{R2}{R1}\right) + I_Q R2$$

0-10 V Adjustable Regulator



When an application requires a continuously variable voltage, or a voltage that can be adjusted to a given output, this adjustable regulator circuit can be used. The output voltage is given by the expression:

$$V_{OUT} = V_{Z1}\left(\frac{R1}{R1 + R2}\right)\left(1 + \frac{R4}{R3}\right)$$

Care should be taken to insure that the input voltage never exceeds 18 V (ripple included) or damage to the μA741C may occur. For a V_{IN} of more than 18 V, a higher working-voltage op amp must be used. This circuit offers all the 78H05 features plus the capability of adjusting the output above and below the nominal 78H05 output.

Fig. 5. Typical Applications

NOTE: Maximum 50 W power dissipation for the 78H05 must be observed and proper heat sinking must be used when required.

CCD Analog Shift Register

INTRODUCTION

Over the past few years, CCD technology has been used successfully in the development of image sensors, 256 to 1728 elements in length and 100 x 100 elements in area. A 244 x 190 element device will soon be introduced. Briefly, they operate as follows: Light photons falling on the sensors generate packets of electrons in potential wells which are then electronically transferred and shifted out of the device by external clocking. A line of video information representing the object pattern is thus obtained for processing in various ways, depending on the particular application.

Early in CCD development, it was apparent that this technology could be used to store digital information in very high densities. Design efforts soon produced a 9216-bit digital CCD memory to fill the cost/performance gap between MOS memories and the much slower rotating magnetic memories*.

The inherent capability of charge-coupled devices to manipulate information in the form of charge packets makes the CCD technology ideal for analog-signal processing, *i.e.,* delay, filtering, signal correlation, enhancement of signal-to-noise ratio. The CCD311 130/260-bit analog shift register is the first in a series of analog devices to exploit this relatively new technology.

DESCRIPTION

The CCD311 consists of the following functional elements (*Figure 1*):

Two charge-injection ports—These ports are located at the front ends of the analog shift registers. Analog information in voltage form is applied to each input port at V_{IA} or V_{IB}. When the sampling control signals, ϕ_{SA} and ϕ_{SB}, are activated, a charge packet linearly dependent on the voltage applied at the input port is injected into its corresponding 130-bit analog shift register.

Two 130-bit analog shift register—These registers transport the charge packets from the charge-injection ports to a gated charge detector by external clocking of the registers. Analog shift register A is clocked by analog transport clocks, ϕ_{1A} and ϕ_{2A}, and register B is clocked by ϕ_{1B} and ϕ_{2B}.

*"CCD Fills the Memory Gap," PROGRESS, Vol. 3, No. 1, Jan/Feb 1975

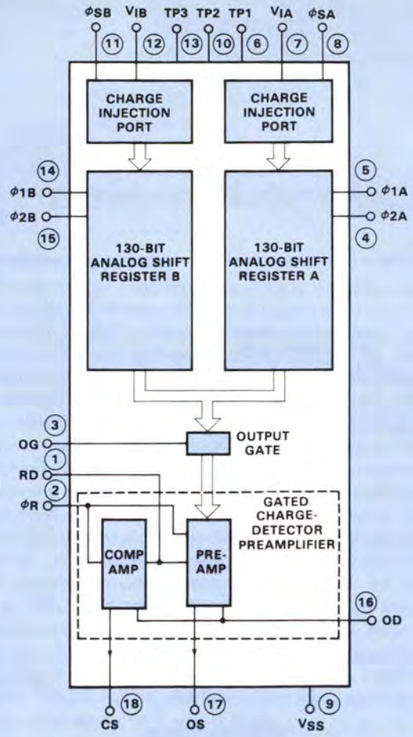


Fig. 1. CCD311 Block Diagram

Gated differential charge-detector preamplifier—Charge packets from the analog shift registers are delivered to a precharged diode connected to the gate of the output MOS transistor. The diode potential changes linearly in response to the quantity of signal charge and produces a signal at the output OS. A reset MOS transistor, driven by the reset clock ϕ_R, recharges the charge detector-diode capacitance before the arrival of each new signal charge packet from the analog shift registers.

MODES OF OPERATION

The CCD311 can be operated either as a 130-bit or 260-bit analog delay line as described below.

130-bit analog delay—Either 130-bit analog shift register, A or B, can be operated as an analog delay line. The driving waveforms for shift register A are shown in the timing diagram (*Figure 2a*). The input voltage signal is applied directly to V_{IA}; it is sampled by the analog sample clock ϕ_{SA} which then injects a proportional amount of charge into the first bit of register A. The input voltage A1, which is sampled between t = 0 and t = t_c, appears inverted at the output terminal OS at t = 260 t_c, and so on. The reset clock ϕ_R is summed internally with the output waveform and the composite waveform appears at terminal OS. By using differential amplification between the compensation source CS and output OS, reset-clock pulses can be eliminated from the video waveform to recover the analog information.

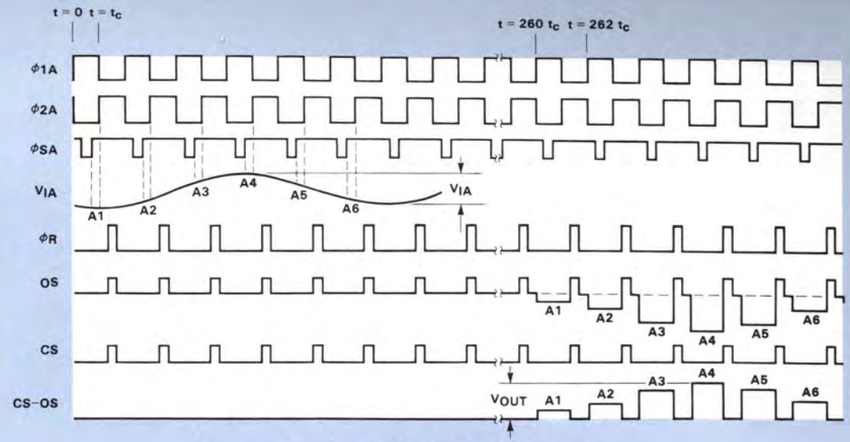


Fig. 2a. Register A Timing Diagram

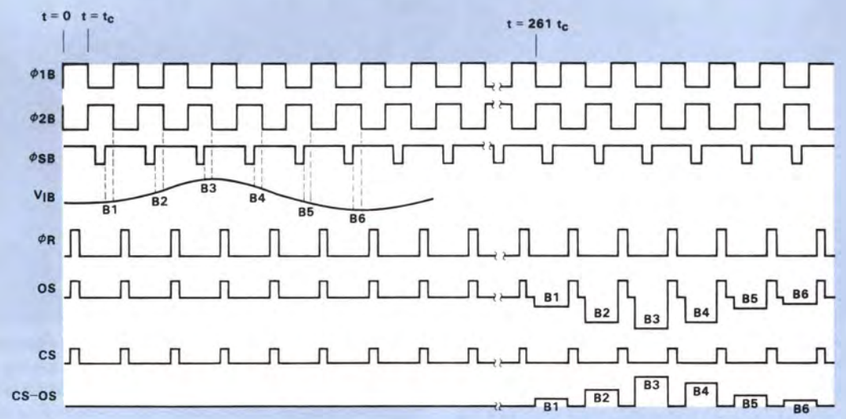


Fig. 2b. Register B Timing Diagram

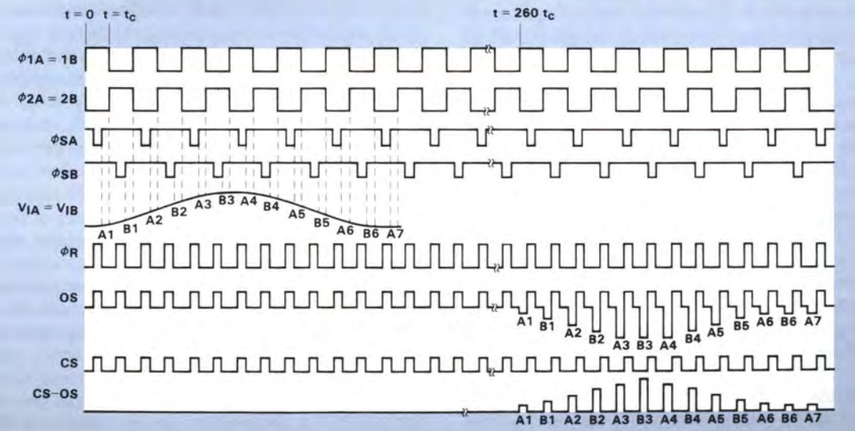


Fig. 2c. Multiplexed Operation

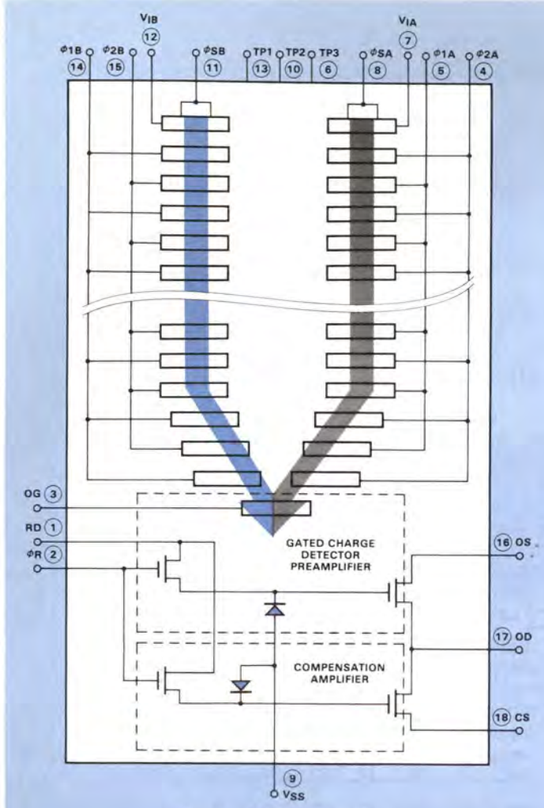


Fig. 3. Circuit Diagram

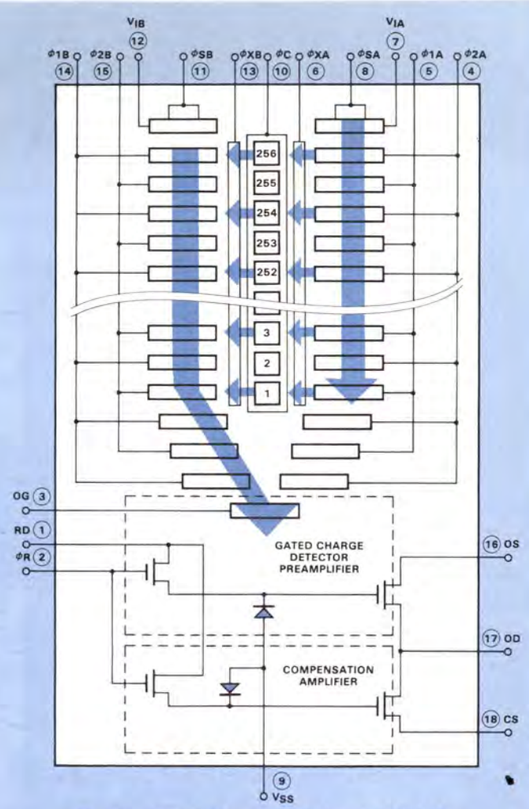


Fig. 4. Circuit Diagram – Selected CCD311

Shift register B can be operated in an analogous fashion as shown in the timing diagram *(Figure 2b)*. Note the timing relationship differences between the A and B register clocks.

260-bit analog delay—The two registers can be multiplexed to double the sampling rate of an input voltage signal. The timing diagram (*Figure 2c*) shows the relationship of the timing waveforms for this mode of operation. Here, $\phi_{1A} = \phi_{1B}$, $\phi_{2A} = \phi_{2B}$ and ϕ_{SA} and ϕ_{SB} are clocked as before. The same input signal voltage is applied to both V_{IA} and V_{IB}. Between $t = 0$ and $t = t_c$, the input signal voltage A_1 is sampled by register A. Between $t = t_c$ and $t = 2\,t_c$, the input signal B_1 is sampled by register B. The charge packet corresponding to A_1 appears at the output at $t = 260\,t_c$ and the charge packet corresponding to B_1 appears at $t = 261\,t_c$. Since the charge-detector diode must be recharged twice as often, reset clock ϕ_R must be clocked at twice the frequency required for 130-bit operation.

The two modes of operation are shown in the circuit diagram in *Figure 3*. Register A operation is shown in grey, B in blue and multiplexed operation is accomplished by simultaneous use of both registers.

Selected CCD Mode

Using selected CCD311s, analog information can be read into analog shift register A, transferred in parallel to the analog storage cells, then transferred in parallel to analog shift register B and read out in serial form (*Figure 4*). In this mode, the device performs time-base compression or expansion. The timing diagram for time-base compression is shown in *Figure 5*. The analog input voltage is applied to the input port V_{IA} of register A. Analog transport clocks, ϕ_{1A} and ϕ_{2A}, are clocked to transfer the corresponding charge packets into register A where they are stored under the ϕ_{2A} electrode. Control clocks ϕ_{XA}, ϕ_C and ϕ_{XB} (TP3, TP2, TP1 pins respectively) are then clocked to transfer all the charge packets in parallel from ϕ_{2A} to ϕ_{1B}. After time T_X, register B is clocked to transfer these charge packets into the output amplifier. Note that the output rate is twice the input rate.

The sequence of transfers is not limited to the above. The analog storage cells are bidirectional in the sense that the charge packets can be transferred in either direction under the control of the appropriate clocks. Therefore, the above sequence can be performed with the roles of the shift registers reversed, *i.e.,* by reading the information into register B, transferring it in parallel to the analog storage cells, transferring it in parallel to register A and then reading it out serially from register A. In fact, information can be fed into one register, parallel transferred to the storage cells and fed back to the same register.

APPLICATIONS

The CCD311 is designed for use in analog signal processing systems where delay of analog information is required. Delays can be varied, which gives the CCD311 a distinct advantage over glass delay lines that can only provide fixed delays.

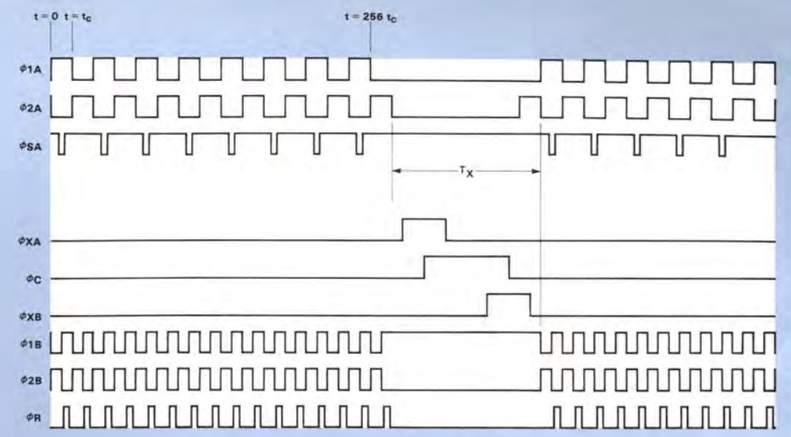


Fig. 5. Timing Diagram for Time Base Compression

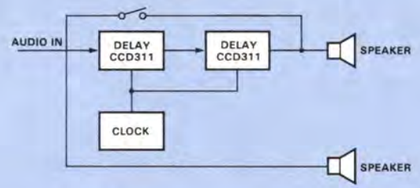


Fig. 6. Phase Adjuster/Reverberator

The CCD311 can shift data across a wide range of frequencies from 10 kHz to 15 MHz clock rate (ϕ_R). With $\phi_{1A} = \phi_{2A} = \phi_{1B} = \phi_{2B} = 5$ MHz and $\phi_R = 10$ MHz (data rate = 10 MHz), a typical signal-to-noise ratio of 50 dB is obtained. Under the same conditions, a non-linearity of typically 4-5% is introduced by the charge injection ports. The following are examples of potential CCD applications.

Time-Base Correction for Video Tape Recorders

When television signals are reproduced from video tapes, time-base errors are introduced due to various factors including contraction or expansion of the recording medium and tape-to-head speed variations. These errors must be eliminated to avoid picture distortion at the TV receivers. The technique used by broadcasting stations is to feed the composite video information from the recorder into an A/D converter at a rate related to the time-base error. This is accomplished by phase locking the signal to the horizontal time base as well as to the color subcarrier reference signal. The digital information is then stored in a digital memory, which provides a delay for the video information, and then is recalled through a D/A converter at a rate proportional to the station synchronization signals. In essence, an A/D converter, a digital storage memory and a D/A converter are required. These functions can be accomplished using CCD311s; information is fed and retrieved at the same rates as above.

Audio Delay

A phase adjuster or reverberator can be constructed using a number of CCD311s for delaying audio signals (*Figure 6*). Clocking each device at 10 kHz provides a 26 ms delay through each device which can be varied by simply adjusting the clock frequency.

Signal Averager (Selected CCD311)

Signal averaging can easily be performed by selected CCD-311s. The first line of information is read into register A, then transferred in parallel to the analog storage cells. The same line is again read into register A and transferred in parallel to the analog storage cells. By repeating this process N times, the signal information is enhanced $\sqrt{N}$ times over the noise. At this point, the information in the analog storage cells can be transferred to register B and read out of the device.

CONCLUSION

The wide range of operating frequencies (10 kHz to 15 MHz) and flexible clocking requirements make the CCD311 a powerful device for systems that require complex manipulation of analog information. A detailed device description has been presented here, along with brief outlines of a few applications that immediately come to mind. This by no means exhausts the possible applications for this revolutionary new device; future articles will discuss other ideas such as how to build filters, signal correlators and so on. Also, with a little imagination, the experienced system designer will think of many more applications for the analog-information delay feature of the CCD311.

interface
interface
interface
interface

Circuits for CMOS Systems

by Rob Walker

Complementary MOS (CMOS) digital logic continues to grow in popularity as more and more functions are added to this prolific family. Originally designed for aerospace applications, CMOS logic is now used in portable instruments, industrial and medical electronics, automotive applications, and computer peripherals.

In terms of functions available, CMOS logic generally parallels that of TTL*. This infers similar system design, therefore the unique aspects of CMOS interface are electrical, rather than logical. The electrical differences are as follows:

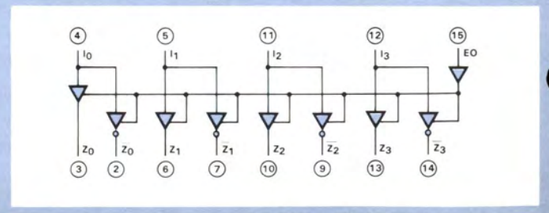
- CMOS output drive at V_{DD} = 5 V is 1/40 of standard TTL output drive, therefore increasing the need for drivers to operate relays, displays, and even TTL.
- CMOS power supply voltage may range from 3 to 18 V (practical limits are 4 to 12 V); interface elements should operate over the same range. In addition, if CMOS is not operated at 5 V, level translators are required at input and output to interface to 5 V logic. The wide operating supply-voltage range of CMOS combined with low power requirements open up interesting possibilities in power-supply regulators.
- CMOS circuits require inputs above 70% V_{DD} for logic HIGH, below 30% V_{DD} for logic LOW. The high level requirement is a problem when driving CMOS from TTL.

Considering the popularity of CMOS, surprisingly little information is available on interface circuits for CMOS systems. Often bipolar ICs are completely overlooked. The following CMOS and bipolar circuits offer a quick reference to standard available interfaces for CMOS applications.

F4104 QUAD LOW VOLTAGE TO HIGH VOLTAGE TRANSLATOR WITH 3-STATE OUTPUTS

The F4104 CMOS translator interfaces low voltage CMOS and TTL circuits to high voltage CMOS circuits. It has four Data inputs, an active HIGH Output Enable input, four Data outputs, and their Complements. With the Output Enable HIGH, the Outputs are in the low impedance ON state, either HIGH or LOW as determined by the Data inputs; with the Output Enable LOW, the Outputs are in the high impedance OFF state.

The device uses a common negative supply (V_{SS}) and separate positive supplies for inputs (V_{DDI}) and outputs (V_{DDO}). V_{DDI} must always be less than or equal to V_{DDO}, even during power turn-on and turn-off. The output may operate up to 15 V; typical propagation delays are 75 ns at V_{DDO} = 10 V.



*"CMOS, You've Come a Long Way", PROGRESS, Vol. 2, No. 10, Oct/Nov/Dec.

F4049 HEX INVERTING BUFFER AND F4050 HEX NON-INVERTING BUFFER

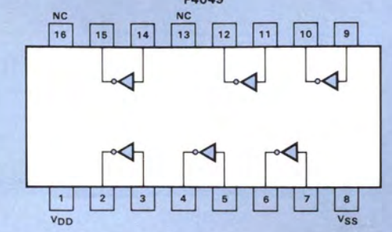
These CMOS buffers provide high current output capability suitable for driving TTL or high capacitance loads. Since input voltages in excess of the buffer supply voltage are permitted, these buffers may be used to convert logic levels of up to 15 V to standard TTL levels. The F4049 provides six inverting buffers, the F4050 six non-inverting buffers. Their guaranteed fan out into common bipolar logic elements is given here. Typical propagation delay is 45 ns when operating at V_{DD} = 5 V.

Guaranteed fan out of F4049, F4050 into common logic families

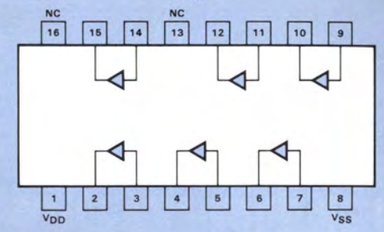
DRIVEN ELEMENT	FAN OUT
Standard TTL, DTL	2
9LS, 93L, 74LS	9
74L	16

Conditions: $V_{DD} = V_{CC} = 5.0 \pm 0.25$ V
$V_{OL} \leq 0.5$ V, T_A = 0 to 75°C

F4049

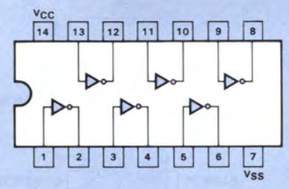


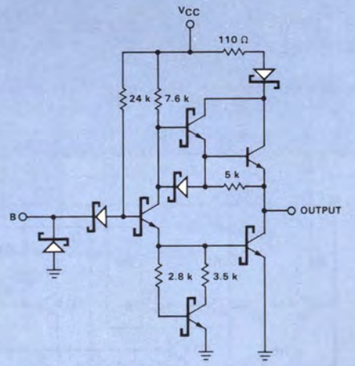
F4050



9LS04 HEX INVERTER

This low power Schottky hex inverter provides interface between second generation CMOS (F4500, 4000B, 74C, etc.) and TTL. Typical propagation delay is 5 ns, 10 times faster than CMOS buffers, and fan out is 5 standard loads. The 9LS04 utilizes diode inputs allowing operation with inputs from CMOS systems operating in excess of 10 V. Power dissipation is 2 mW per buffer.

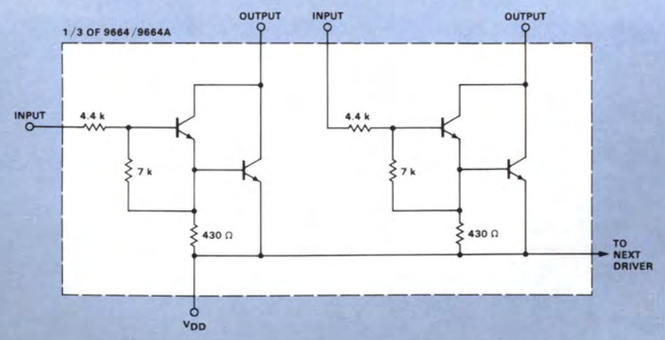


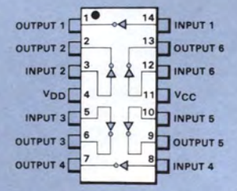


9664/9664A LED, RELAY OR LAMP DRIVER

The 9664/9664A bipolar hex LED/lamp driver converts CMOS signals to high output currents for LED display, digit select, incandescent lamps, relays or other applications where high output drive current is important. The 9664 offers 10 V breakdown voltage; the 9664A is selected for 20 V operation for those applications where higher breakdown voltage is required.

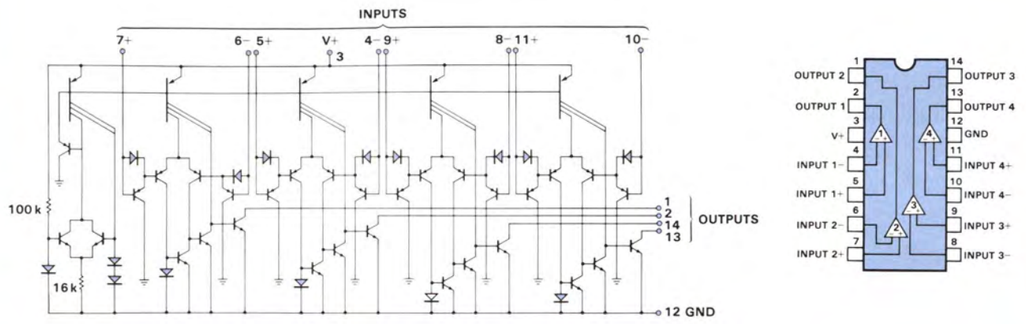
Since the 9664A accepts inputs to 20 V, it can be used in high voltage CMOS systems. The CMOS device pin driving the 9664 cannot be used simultaneously to drive other logic circuits because of the loading effect of the 9664 on the CMOS output.





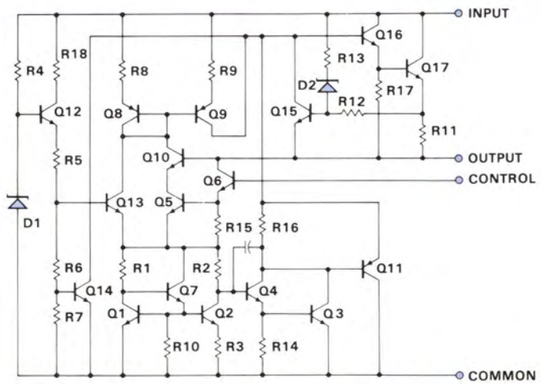
μA775 QUAD COMPARATOR

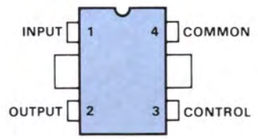
The μA775 bipolar quad comparator consists of four independent voltage comparators designed specifically to operate from a single power supply over a wide range of voltages. It has an unusual characteristic in that the input common-mode voltage range includes ground, even though the μA775 is operated from a single power-supply voltage (+2 V to +36 V). This device allows voltage comparisons near ground potential. Applications include limit comparators; simple analog to digital converters; pulse, squarewave and time delay generators; wide range V_{CO} and multivibrators.



μA78MG 4-TERMINAL ADJUSTABLE VOLTAGE REGULATOR

This single compact bipolar regulator with 500 mA capability is sufficient for all but the very largest CMOS systems. The adjustable output voltage feature (5 to 30 V) allows fine tuning of system speed product. Other features include internal thermal overload protection, internal short-circuit current protection and output safe-area protection.

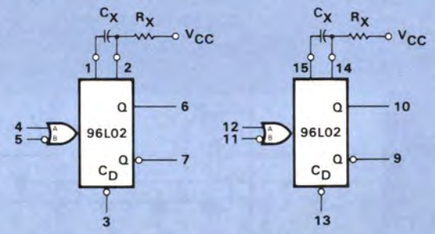




Note: Heat sink tabs connected to common

96L02 LOW POWER DUAL RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

The TTL 96L02 monostable provides an output pulse with duration and accuracy as a function of external timing components. It has excellent immunity to noise on the V_{CC} and ground lines. The 96L02 is pin and function equivalent to the F4528 dual CMOS monostable; it exhibits superior stability and speed and is usable in 5-V CMOS systems. Typical power dissipation is 25 mW/monostable and typical propagation delay is 50 ns. The 96L02 offers a retriggerable 0-to-100% duty cycle and an optional retrigger lock-out capability. It is also pulse-width compensated for V_{CC} and temperature variations.



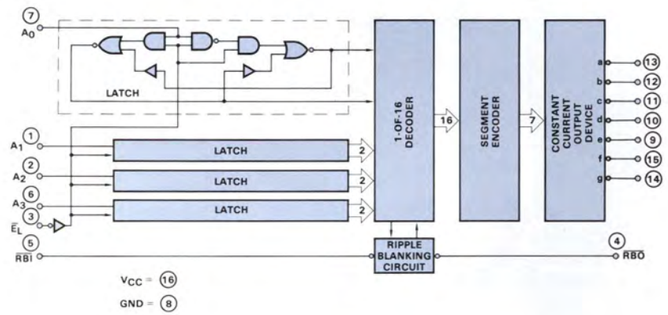
9374 7-SEGMENT DECODER/DRIVER LATCH

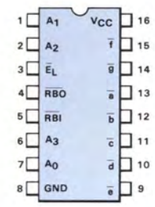
The 9374 TTL decoder/driver has latches on the address inputs and active LOW constant-current outputs to drive LEDs directly. This device accepts a 4-bit binary code and produces output drive to the appropriate segments of the 7-segment display. It has a decode format which produces numeric codes 0 through 9 and other codes as shown in the truth table.

Latches on the four data inputs are controlled by an active LOW Latch Enable $\overline{E}_L$. When $\overline{E}_L$ is LOW, the state of the outputs is determined by the input data. When $\overline{E}_L$ goes HIGH, the last data present at the inputs is stored in the latches and the outputs remain stable.

The 9374 also provides automatic blanking of the leading and/or trailing edge zeros in a multidigit decimal number, resulting in an easly readable decimal display conforming to normal writing practice. In an 8-digit mixed integer fraction decimal representation, using the automatic blanking capability, 0060.0300 would be displayed as 60.03. Leading-edge zero suppression is obtained by connecting the Ripple Blanking output ($\overline{RBO}$) of a decoder to the Ripple Blanking input ($\overline{RBI}$) of the next lower stage device. The most significant decoder stage should have the $\overline{RBI}$ input grounded; and since suppression of the least significant integer zero in a number is not usually desired, the $\overline{RBI}$ input of this decoder stage should be left open. A similar procedure for the fractional part of a display will provide automatic suppression of trailing-edge zeros.

Another 9374 feature is the reduced loading on the data inputs when the Latch Enable is HIGH (only 10 μA typ). This allows many 9374s to be driven from a CMOS device in multiplex mode without the need for drivers on the data lines. The 9374 logic must be operated from a 5 V supply; logic inputs are also limited to 5 V.



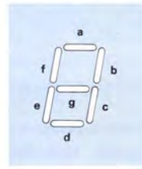


TRUTH TABLE

BINARY STATE	INPUTS $\overline{E}_L$	$\overline{RBI}$	A_3	A_2	A_1	A_0	OUTPUTS a	b	c	d	e	f	g	$\overline{RBO}$	DISPLAY
–	H	*	X	X	X	X	← STABLE →							H	STABLE
0	L	L	L	L	L	L	H	H	H	H	H	H	H	L	BLANK
0	L	H	L	L	L	L	L	L	L	L	L	L	H	H	0
1	L	X	L	L	L	H	H	L	L	H	H	H	H		1
2	L		L	L	H	L	L	L	H	L	L	H	L		2
3	L		L	L	H	H	L	L	L	L	H	H	L		3
4	L		L	H	L	L	H	L	L	H	H	L	L		4
5	L		L	H	L	H	L	H	L	L	H	L	L		5
6	L		L	H	H	L	L	H	L	L	L	L	L		6
7	L		L	H	H	H	L	L	L	H	H	H	H		7
8	L		H	L	L	L	L	L	L	L	L	L	L		8
9	L		H	L	L	H	L	L	L	H	H	L	L		9
10	L		H	L	H	L	H	H	H	H	H	H	L		-
11	L		H	L	H	H	L	H	H	L	L	L	L		E
12	L		H	H	L	L	H	L	L	H	L	L	L		H
13	L		H	H	L	H	H	H	H	L	L	L	H		L
14	L		H	H	H	L	L	L	H	H	L	L	L		P
15	L	X	H	H	H	H	H	H	H	H	H	H	H	H	BLANK
X	X	X	X	X	X	X	H	H	H	H	H	H	H	L**	BLANK

* The $\overline{RBI}$ will blank the display only if a binary zero is stored in the latches.

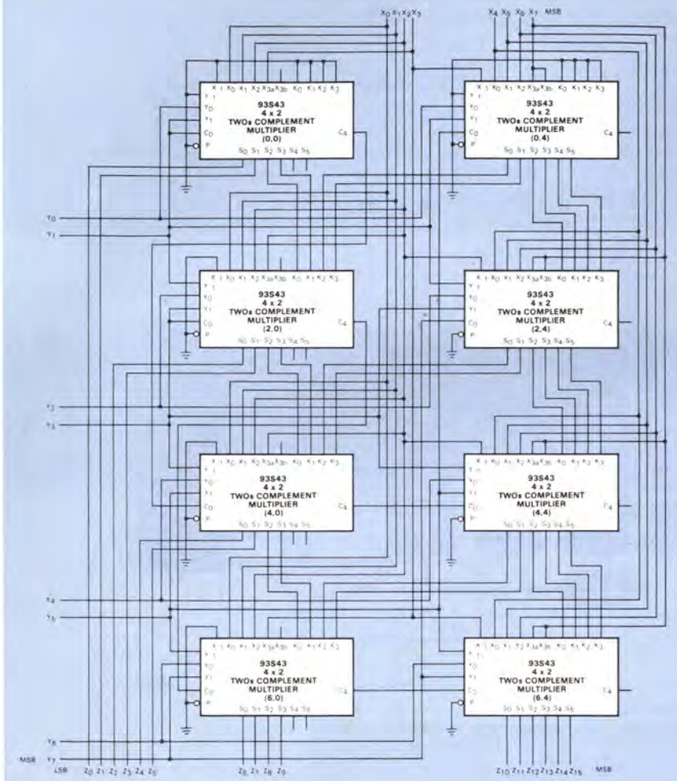
** $\overline{RBO}$ used as an input overrides all other input conditions.



Note: The numbering system of the 34000 series CMOS has been changed to conform to that of the industry's popular 4000 series. The "3" in the FSC part number is now replaced with an "F", e.g., 34528 becomes F4528.

CIRCUIT IDEAS Digital

by Raj Sengottaiyan and Rob Walker



PIN NAMES

$X_{-1}.X_0.X_1.X_2.X_{3a}.X_{3b}$	Multiplicand Inputs
$Y_{-1}.Y_0.Y_1$	Multiplier Inputs
$K_0.K_1.K_2.K_3$	Constant Inputs
C_0	Carry Input
$\overline{P}$	Polarity Control
$S_0.S_1.S_2.S_3.S_4.S_5$	Product Outputs
C_4	Carry Output

PERFORMANCE AND PART COUNT

Array Size	Typical Delay Without Adders (ns)	Typical Delay With Adders (ns)	Number of 93S43s Req'd.	Number of 74S181s Req'd.
8x8	68	57	8	3
12x12	104	75	18	5
16x16	140	93	32	7
20x20	176	111	50	9
24x24	212	129	72	11
28x28	248	147	98	13
32x32	284	165	128	15
48x48	428	237	288	23
64x64	572	309	512	31

MULTIPLY TWO 8-BIT NUMBERS IN 68 ns

Interest in fast multiplication schemes is on the increase. New applications such as fast Fourier transforms, digital filters, and very high performance processors require faster multiplication than is possible with conventional sequential add-shift algorithms[1]. Multiplication may be performed directly using ROM table look-up, but an impractical number of ROM bits are required for word lengths of six bits and beyond. One approach[2] is the use of conversion to logarithms with ROM table look-up, addition, and ROM reconversion. This approach has limited accuracy using practical ROM sizes.

Recent developments in Schottky technology now provide another approach for high speed multiplication. The 93S43 is a combinatorial MSI device that utilizes a modified "Booth's Algorithm" to multiply two bits by four bits. With appropriate interconnection, arrays of 93S43s are practical for direct multiplication of word lengths up to 24 bits. The interconnection scheme for an 8 x 8 multiplication array, shown here, has a typical multiply time of 68 ns. Note that the multiplication is combinatorial; no clocks, shifting, or control logic are required. For still higher speeds, 74S181 ALUs can be added. Part requirements and typical delays for various array sizes are given in the table. A full description of this multiplication technique is available in App Note 329.

REFERENCES

1. I. Flores, The Logic of Computer Arithmetic, Englewood Cliffs, N.J. Prentice-Hall, 1963.
2. T. Brubaker, J. Becker, "Multiplication Using Logarithms Implemented With Read-Only Memory," IEEE Transactions on Computers, August 1975.

NEW PRODUCTS

Recently announced devices presently available. Order specifications by product number.

QUALIFIER™ 901 TESTER NOW HAS PROGRAMMER

The Qualifier 901 IC tester is a low cost benchtop system for testing DTL, TTL and CMOS devices. Fully automatic, it is a self-contained microcomputer system that uses a microprocessor to control the internal functions. Device test programs are normally supplied on QUAL-CARD™ optically coded plastic cards; current listing covers more than 1400 device types by manufacturer. However, there has been a growing demand from the user for a method to write his own special programs.

To meet this demand, Fairchild System Technology has introduced the *Programmer* for creating and modifying device programs in the user's plant. It is similar to a small computer system with a microprocessor CPU, a PROM for operating system storage, a RAM for test-program storage and work space, plus I/O capabilities.

The *Programmer* is a compact unit that mounts easily on any teletypewriter stand, is adjustable to any transmission rate, and accommodates a broad line of RS232C compatible terminals. The Qualifier 901 tester and *Programmer* are linked with a simple plug-in cable con-

nector. To modify a QUAL-CARD program, the procedure is simple. The appropriate QUAL-CARD is inserted in the optical reader which is an integral part of the Qualifier 901 tester. The program is then transmitted to the *Programmer* and printed out via the teletypewriter. The user gives simple commands for program change to the *Programmer*, using the teletypewriter. The *Programmer* now transmits the new program to the tester for immediate use while the teletypewriter reader/punch simultaneously punches a paper tape for future testing.

To generate a new program, the *Programmer* can be used as a stand-alone unit or in connection with the Qualifier. Once the new program is written, a program tape is punched on the teletypewriter reader/punch and the program is ready for transmission to the Qualifier tester at any time. The user can connect the *Programmer* to two testers if he wishes, transmit the new program to one, flip a switch and transfer the program to the other.

For information on the *Programmer* system to increase the versatility of the Qualifier 901 tester, or for information on the benchtop tester, call Marketing Services, Fairchild Systems Technology, (408) 998-0123 or write

Marketing Services
Fairchild Systems Technology
1725 Technology Drive
San Jose, Ca. 95110

NEW UHF VARIABLE-MODULUS PRESCALERS AVAILABLE

Two low-cost versatile UHF prescalers for use in digital TV and FM tuning, communications, instrumentation and test equipment are now available. Made with the Isoplanar II process, both circuits use dual modulo ratios. The 11C83 is an ECL 1 GHz ÷ 248/256 prescaler; the 11C90 is an ECL 650 MHz ÷ 10/11 prescaler.

The divide-ratio control inputs as well as the prescaler outputs are compatible with TTL, CMOS and MOS. Input frequency can be dc or ac coupled, the latter simplified by an internal self-biasing network. The dual divide-ratio technique allows low-frequency logic to control the prescaler and achieve a broad range of overall divide ratios. This provides the versatility of a fully programmable divider with the frequency capability of a fixed prescaler. As a result, a phase locked loop can operate with a much higher reference frequency thereby giving faster lock-up times and reduced residual FM noise.

Packaged in the 14-pin DIP, the 11C83 is designed specifically for the digital TV-tuning market and is part of a complete phase-locked-loop tuning system which also includes a PROM and CMOS and low-power Schottky logic.

The 11C90, packaged in a 16-pin DIP, has the same pinouts as the popular 93H90 VHF prescaler, but with the addition of an input biasing network, TTL/CMOS-compatible mode-control inputs and TTL output.

2K AND 4K BIPOLAR PROMs ARE THE FASTEST

The 93436/93446 and 93438/93448 are fully docoded high speed 2048-bit and 4096-bit field-programmable ROMs, organized 512 words by four bits and 512 by eight bits respectively. Manufactured using the Isoplanar Schottky process to reduce chip size and enhance performance, these PROMs have typical access times of 30 and 40 ns, up to 40% faster than similar devices. Advanced nichrome fuse links provide wide, clean gaps for long-term reliability.

The 93436 and 93438 2K PROMs are identical except for the output stage; this is also true of the 93438 and 93448 4K devices. The 93436 and 93438 have uncommitted collector outputs, while the 93446 and 93448 have 3-stage outputs. They each provide an on-chip address and buffer and a chip-select input for easy memory expansion. Both PROM pairs are available in full military and commercial temperature ranges, packaged in 16-pin (93436/38) and 24-pin (93446/48) DIPs.

LOW POWER SCHOTTKY AND MACROLOGIC™ TTL
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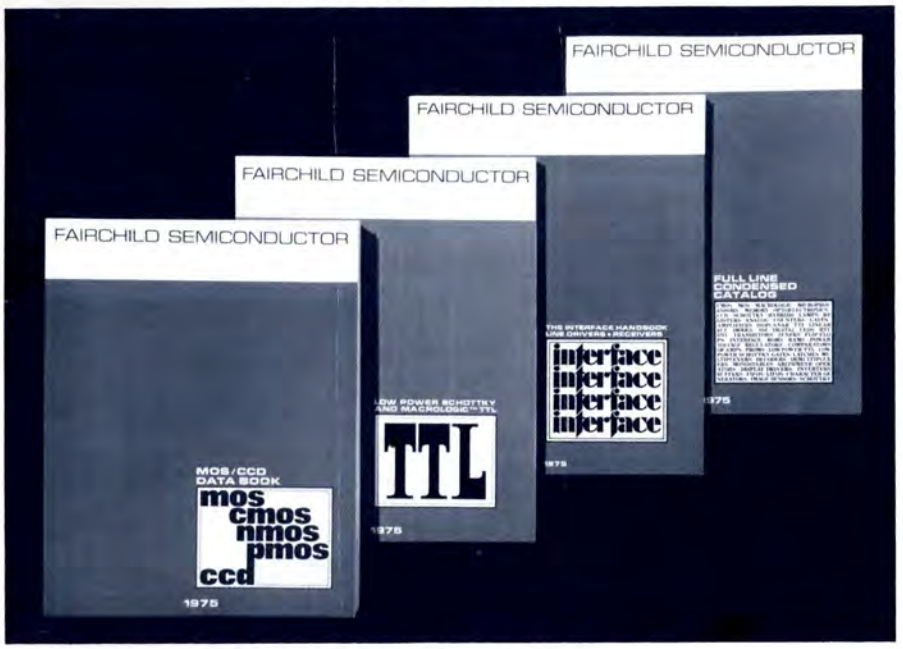

Low Power Schottky and MACROLOGIC TTL

Low power Schottky is fast becoming the TTL family leader, primarily because of its reduced power consumption and improved speed over standard TTL. Now, a complete data book is available giving detailed characteristics on over 175 LSTTL devices and on seven of the new, more complex and powerful MACROLOGIC TTL circuits. A section on design considerations is also included, plus two selector guides – one for SSI including a replacement guide, the other, by function, for MSI.

MOS, CCD

MOS and CCD have important features in common – similar technologies, high packing densities providing low cost per bit, and applications in moderate speed, low power digital systems. Recent technology improvements, refinement of the Isoplanar process in particular, have quadrupled circuit performance in the past few years, at the same time substantially reducing cost. This data book offers a broad range of MOS, CMOS and CCD devices, organized by function within the product sections, to aid the equipment designer in choosing the best circuits to meet his system requirements.

For your copies of the Low Power Schottky and MACROLOGIC TTL and the MOS, CCD data books, use the PROGRESS mailing card, or drop us a line.

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