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More and more automobiles are being produced with electronic ignition systems as standard equipment. At the same time, electronic ignitions are gaining popularity among owners of cars with conventional systems, because they offer better performance and are easy to install. The feature this month offers a comprehensive comparison of the conventional inductive-storage system, used in automobiles for decades, and the breaker-point electronic ignition system, one of several types available today. A list of terminology and definitions is included for quick reference to ignition-system nomenclature.

The evaluation of the effects of stray capacitance and stray lead inductance on transistor performance has always been one of the circuit designer's most difficult tasks. The second article discusses an easy method to determine these effects using SPEEDY, and presents some interesting data showing how these feedback strays influence gain and stability.

A standard *subnanosecond* ECL family called F100K, designed to meet the data-processing industry demand for faster processing rates, higher machine densities and greater system reliability, is described in another article. The F100K circuits offer subnanosecond speeds, multipurpose functions, advanced processing and packaging to provide system performance and density approaching that of custom LSI, but with the cost and producibility advantages of high volume standard building blocks.

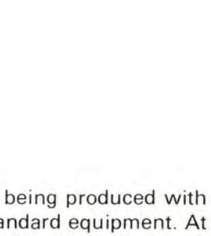
The new products in this issue include a charge-coupled linear image sensor with 1728 elements, a 40 x 9 MOS FIFO for data buffering, the new 11C00 family of functional elements designed for instrumentation and communications applications, and a group of industry-standard core memory drivers and sense amplifiers.

And finally, two simple circuit ideas are presented—a switch debouncer and a switch synchronizer—to alleviate some of the problems of interfacing a switch to a digital system.

Starting in July, PROGRESS will return to a monthly publication schedule.

In this issue

Since the basic purpose of any ignition system is to create a spark, it seems only natural to focus on the spark plug for our cover. Can you identify the classic automobiles?



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PROGRESS

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by Len Arguello

AUTOMOTIVE IGNITION SYSTEMS

The increasing use of electronic ignition systems as standard equipment by the automotive industry has stimulated demands for such systems by owners of cars not so equipped. Several are available to replace the conventional system. But, before the potential buyer decides whether or not to switch to one of these new systems, he should have an objective picture of the relative merits of both conventional and electronic ignition systems, in terms of operation, performance and limitations.

The objective of any ignition system, in conjunction with an internal combustion engine, is to generate the *voltage* necessary to break down the gap between the spark-plug electrodes. The resultant spark then ignites the combustible mixture in the cylinder. To insure that the flame front that originates at the spark plug during ignition is adequately propagated within the cylinder, a minimum amount of *energy* must be available in the spark. An even more important element for effective ignition is *timing*; that is, the spark must occur at precisely the correct moment at the proper cylinder for maximum engine efficiency.

Conventional vs Electronic

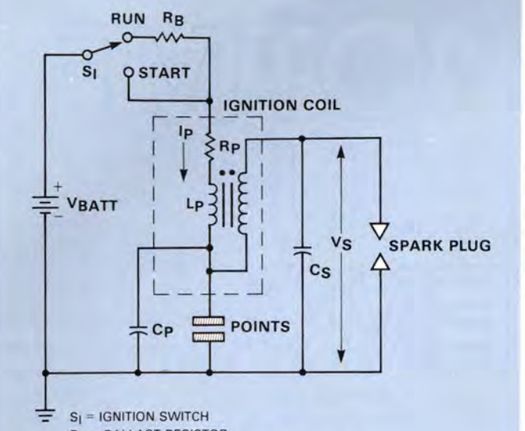


Fig. 1. Conventional Ignition System

THE CONVENTIONAL (KETTERING) IGNITION SYSTEM

The Kettering ignition system is an inductive storage system, basically consisting of an induction coil, breaker contacts (points), capacitor (condenser) and power supply. Invented by Charles Kettering, it has well served the automotive world for over half a century. A typical circuit is shown in *Figure 1*.

Operation is quite straightforward. When the ignition switch is on and the points are closed, the primary current I_P flows, increasing exponentially with a time constant τ . This current can be defined by the expression

$$I_P(t) = \frac{V_{BATT}}{R_B+R_P}\left(1-e^{-t/\tau}\right) \qquad (1)$$

where

$$\tau = \frac{L_P}{R_P+R_B}$$

The term t in *Equation 1* is defined as the time the points remain closed between ignition cycles. This time, often referred to as the system *dwell time*, determines the level the primary current will reach before the points reopen. Dwell time is dependent upon engine speed and, for speeds below 1000 rpm, it is typically long enough to allow steady state current levels to be reached in the primary circuit. Dwell time should not be confused with *dwell angle*, often called "dwell", which is defined as the number of degrees of distributor shaft rotation during which the points remain closed; dwell angle is not a function of engine speed.

As current flows in the primary inductance, L_P, electrical energy is stored in the primary circuit at a magnitude depending upon the current level reached when the points open.

$$E(t) = \frac{L_P I_P^{\,2}(t)}{2} \qquad (2)$$

Substituting $I_P(t)$ from *Equation 1* in *Equation 2*,

$$E(t) = \frac{L_P}{2}\left[\frac{V_{BATT}}{R_B+R_P}\left(1-e^{-t/\tau}\right)\right]^2 \qquad (3)$$

where E = energy in joules or watt-seconds.

This equation shows very clearly that the stored energy is dependent upon the engine speed, which is one of the major drawbacks of an inductive storage ignition system.

When the points open, the energy stored in the primary circuit is dissipated in the secondary winding, and in lossy components in the primary. In the ideal case where no lossy components exist in the primary, all of the stored energy is released for dissipation in the secondary winding. Therefore, assuming no transfer losses in the ignition coil,

or $$E_{Primary} = E_{Secondary}$$

$$\frac{L_P I_P^{\,2}}{2} = \frac{C_S V_S^{\,2}}{2} \qquad (4)$$

where V_S = maximum available secondary voltage.

therefore,

$$V_S = \sqrt{\frac{L_P}{C_S}}\, I_P \qquad (5)$$

Substituting I_P from *Equation 1* in *5,*

$$V_S = \sqrt{\frac{L_P}{C_S}}\left[\frac{V_{BATT}}{R_P+R_B}\left(1-e^{-t/\tau}\right)\right] \qquad (6)$$

Figure 2 shows secondary voltage and primary current as a function of engine speed for a typical ignition system. The degradation in secondary voltage follows the primary current; however available energy decreases at a greater rate, since it is proportional to the square of the primary current (*Equation 2*).

The actual secondary voltage is less than that indicated by *Equation 6* because of shunt loads, ignition coil efficiency, leakage inductance, and most important, because of losses that occur across the breaker points. The breaker-point switching losses can be considered the major element limiting secondary voltage to less-than-ideal levels, especially at low engine rpm. Condenser C_P is placed across the breaker points primarily to minimize this effect. *Figure 3* shows the race conditions between the contact-opening rate and the rate of voltage rise across the contacts. If the latter is less than the first, the problem is minimized. The voltage at which arcing or limiting occurs increases with time as the points separate. Thus, even large contact voltages do not produce arcing if the rate of rise is low enough (*Figure 3*).

The contact voltage rate of rise is also affected by the primary coil inductance, L_P, and the secondary capacitance C_S reflected at the primary winding as

$$C_S' = C_S N^2$$

where C_S' = reflected secondary capacitance,
N = ignition transformer turns ratio.

The resonant frequency of the primary circuit can be expressed as:

$$f_P = \frac{1}{2\pi\sqrt{L_P C_S'}}$$

Therefore the approximate rise time of the primary voltage is as follows *(Figure 4)*.

$$t_r = \frac{\pi\sqrt{L_P C_S'}}{2} \qquad (7)$$

But, secondary voltage limiting at low engine speeds is not the only major problem caused by breaker-point arcing. Arcing across contact surfaces also creates extremely high temperature "hot spots", resulting in contact pitting and erosion. This condition effectively widens the original gap setting, decreasing dwell angle and limiting the energy to the system. Eventually this condition leads to hard starting, rough idling, and severe misfiring at high engine rpm. Because of this problem, the automobile ignition system often requires frequent maintenance.

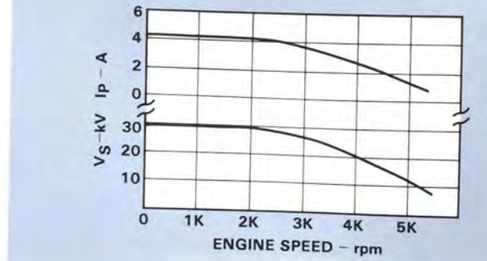


Figure 2

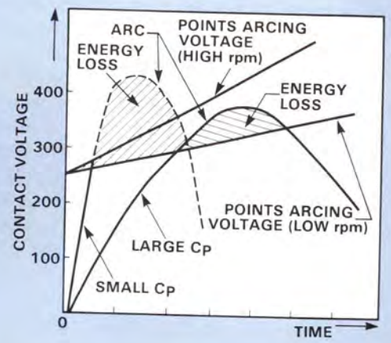


Figure 3

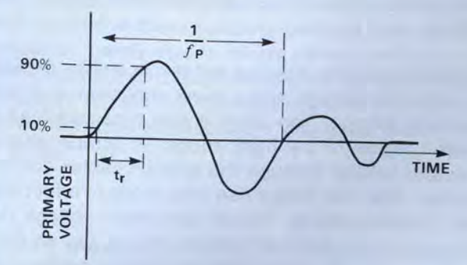


Fig. 4. Definition of Rise Time, t_r (Equation 7)

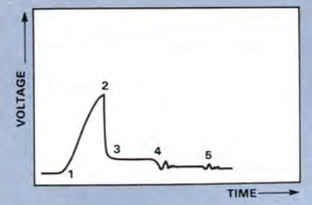


Figure 5

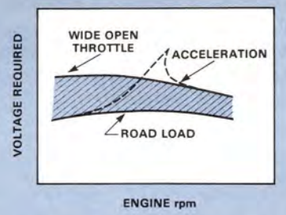


Fig. 6. Effects of Speed and Load

The spark-plug voltage waveform in *Figure 5* qualitatively demonstrates what happens in the secondary winding as a result of the points opening, assuming the available voltage is sufficient to ionize the mixture between spark-plug electrodes. The voltage at the spark plug starts to rise at point 1, with a rise time as defined by *Equation 7*, and reaches the ignition level at point 2. At this point, a large secondary current begins to flow, its magnitude depending upon the type of ignition cables used, *i.e.,* resistive vs wire core, and the voltage level at the point of ignition. The region from 3 to 4 is known as the system "burn time". It varies depending upon the voltage level at point 2 and the amount of energy available at the spark plug. When there is insufficient energy to support ionization as shown at point 4, the remaining energy is dissipated by ringing. Point 5 shows a small disturbance that occurs the moment the points again close, allowing current to flow through the coil primary and the cycle to repeat.

The two most important characteristics of the voltage waveform are the "burn time" or spark duration and the rise time (time from 1 to 2). If the spark duration is too long, over-heating and erosion of the spark plug tips occur, resulting in rapid wear. Too short a burn time causes incomplete burning of the air/fuel mixture resulting in loss of power and increased air polluting emissions. Typical burn times vary for the conventional ignition system, depending on engine speed and cylinder variables.

Too long a rise time provides excessive energy dissipation with fouled plugs and a lower maximum available secondary voltage. Too short a rise time can lead to radiation losses of the high frequency components of the output voltage through the ignition cables and coil structure. Also, too long a rise time tends to affect high speed ignition timing. Typical secondary-voltage rise times are in the order of 100 to 150 μs. On an eight cylinder engine, the time between ignition cycles at an engine speed of 5000 rpm corresponds to 3 ms. Thus, if angular crank shaft rotation = 90° (one firing cycle) and time = 3 ms,

$$\text{time/degree} = \frac{3 \times 10^{-3}}{90} = 33\ \mu s/\text{degree}$$

This shows that, for a rise time of 150 μs, the ignition timing error contributed by rise time is approximately 4.8 degrees. This error is normally cancelled out by statically timing the engine to manufacturer's specifications. Theoretically, the timing error should remain at a minimum regardless of engine speed.

The exact values of secondary voltage and energy required for proper car operation under most operating conditions depend upon a number of factors, some of which are:

Condition of Spark Plugs
Fouled plugs tend to increase both the voltage and energy required for ignition. The spark plug gap also affects the required voltage. The wider the gap setting, the higher the required voltage for ionization.

Cylinder Temperature and Pressure
The minimum voltage required to break down the air/fuel mixture in a cylinder is dependent upon the compression of the gas at the time of ignition. As the product of gas pressure and electrode spacing increases, the required voltage for proper break down of the spark plug gap also increases.

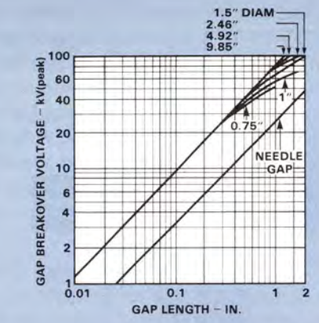
$$V_B \propto \frac{P_d}{T}$$

where:

V_B = Gap Breakover Voltage
P = Cylinder Pressure
d = Electrode Spacing
T = Temperature of mixture inside cylinder.

Speed and Load
The effects of speed and load in a typical 4-cycle automotive engine are illustrated in *Figure 6*.

Acceleration
A sudden wide-open throttle situation can cause an increase in the spark plug voltage requirement. This is a result of the rapid increase in compression pressures when the throttle is opened, especially since the thermal time constant of the plug prevents its temperature from increasing instantaneously (*Figure 6*).



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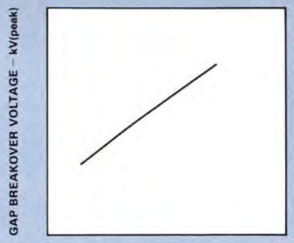

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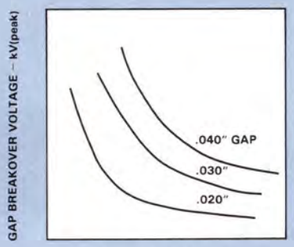


c.

Table of Multiplying Factors

PRESSURE IN. Hg	PRESSURE mm Hg	TEMPERATURE – °C −40	−20	0	20	40	60
5	127	0.26	0.24	0.23	0.21	0.20	0.19
10	254	0.47	0.44	0.42	0.39	0.37	0.34
15	381	0.68	0.64	0.60	0.56	0.53	0.50
20	508	0.87	0.82	0.77	0.72	0.68	0.64
25	635	1.07	0.99	0.93	0.87	0.82	0.77
30	762	1.25	1.17	1.10	1.03	0.97	0.91
35	889	1.43	1.34	1.26	1.19	1.12	1.05
40	1016	1.61	1.51	1.42	1.33	1.25	1.17
45	1143	1.79	1.68	1.58	1.49	1.40	1.31
50	1270	1.96	1.84	1.73	1.63	1.53	1.44
55	1397	2.13	2.01	1.89	1.78	1.67	1.57
60	1524	2.30	2.17	2.04	1.92	1.80	1.69

Figure 7

Figure 7 shows graphs of gap breakover voltage versus gap distance, cylinder pressure and electrode temperature. They apply to a voltage that is continuous or at a frequency low enough to permit complete deionization between cycles. In *Figure 7a,* temperature is 25°C and pressure is 29.9 in. Hg. Peak kilovolts should be multiplied by the factors given in the associated table for temperature and pressure other than the above.

In conclusion, two major items limit the basic performance capability of the conventional ignition system. The first and most important to the average person who does not require high speed performance (above 5000 rpm) is the use of mechanical breaker points to switch the current in a high-energy inductive circuit. The second is the dependence of high speed engine performance upon ignition coil and ballast-resistor parameters, an inherent limitation of the inductive storage system.

THE ELECTRONIC IGNITION

Substituting a high efficiency, high speed solid state switch for the breaker points in the high energy circuit greatly improves the low speed performance of an ignition system. Historically, this has been the basic difference between the conventional and electronic ignition systems. In concept, the solid state ignition has been available for many years, but early semiconductor devices used in these systems suffered from reliability problems, mainly due to severe stress conditions. The evolution of highly sophisticated, high power semiconductor technology has solved these problems and gained the auto manufacturers' support of the electronic ignition.

Figure 8 shows some of the various types of electronic ignition systems, most of which are currently available. The one described here falls under the category of a breaker-point system, an energy storage type with fixed dwell and breaker-point input (*Figure 9*). The three basic circuit blocks are all that is necessary to achieve a significant improvement in engine performance over that using the conventional system.

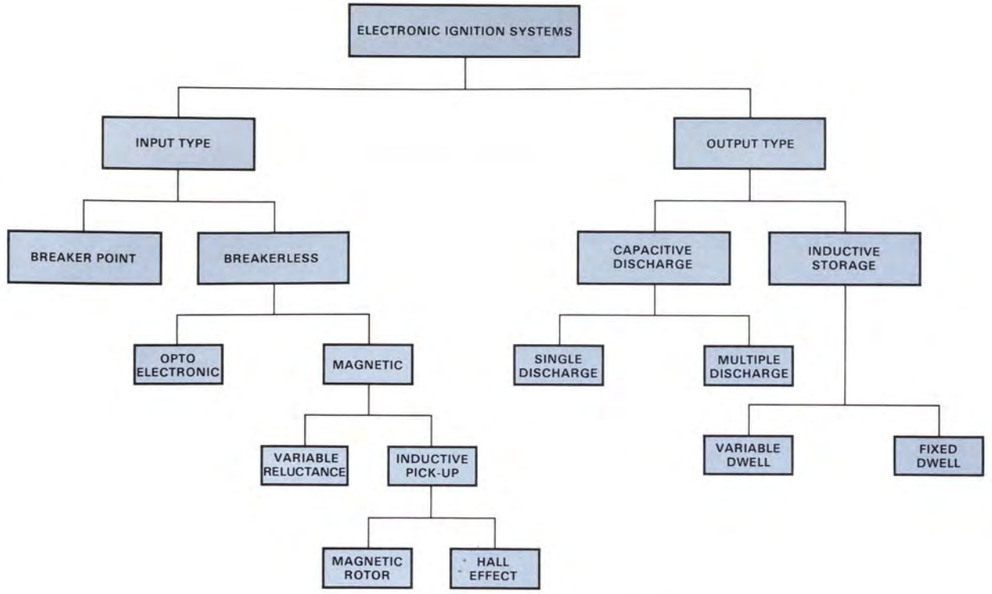


Fig. 8. Types of Electronic Ignition Systems

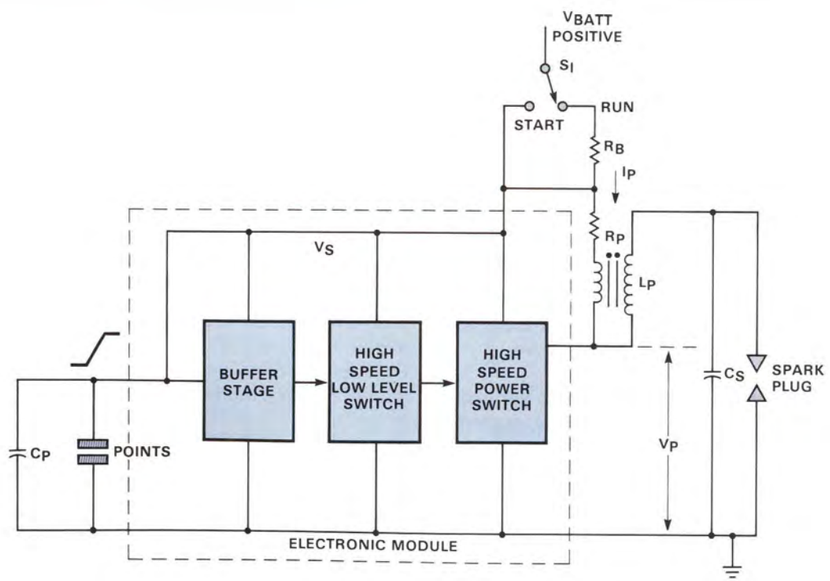


Fig. 9. Electronic Ignition System

The Buffer Stage

The buffer stage provides isolation between the breaker points and the low level switch circuitry. The input current requirement is minimal, therefore the current through the breaker points for a given V_S is mainly determined by this stage. This circuit must have reasonable noise immunity and must be designed to minimize the effect of high speed point bounce upon the output current. At this point it should be noted that condenser C_P is no longer required for system operation although it does provide some degree of inherent high speed point-bounce immunity.

High Speed, Low Level Switch

The main function of the low level switch is to receive the input from the buffer stage and convert it into a high speed voltage step capable of sourcing and sinking currents as required by the output stage. The output-voltage low levels (V_{OL}) from this switch should allow for a very fast base-charge recombination to take place in the following stage during its turn-off period.

High Speed Power Switch

The power switch is the most important element in the electronic ignition module. Basically, it performs the same function as the breaker points in a conventional system, but, much more efficiently. Because the output device acts as a switch in series with the ignition-coil primary, its required parameters are related directly to the quality of the coil and to the drive capabilities of the preceding stage. Most important of all, these devices will be exposed to extremely hostile climatic and electrical environments, therefore, the system design must guarantee operation under adverse conditions.

Power Device(s) Requirements

Figure 10 shows a simplified equivalent load circuit for the output device of a typical inductive-storage electronic ignition system. After the breaker points close and at a time determined by the total subsystem propagation delay, transistor Q1 conducts heavily. The magnitude of the collector current $I_P(t)$ is given by

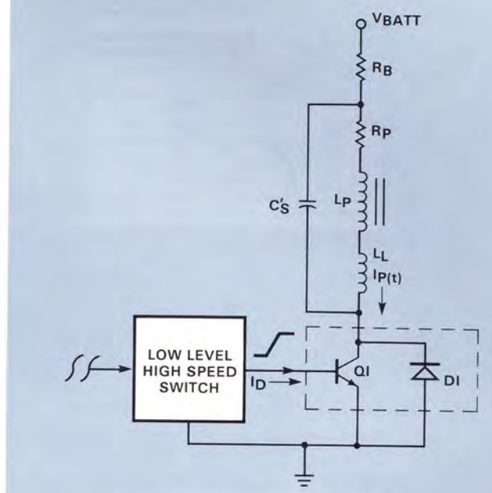
$$I_{P(t)} = \left(\frac{V_{BATT} - V_{CE(SAT)1}}{R_P + R_B}\right)\left(1 - e^{-tR_P/L_P}\right)$$

where the first term is the steady-state component of $I_P(t)$.

The steady-state current level can only be reached when the engine speed is slow enough to allow the dwell time, t, to be longer than approximately

$$5\,\frac{L_P}{R_P + R_B}$$

In a typical case at room temperature, this occurs at engine speeds below 2000 rpm. At speeds beyond this, the classical exponential term begins to limit the maximum achievable current level (*Figure 11*).



L_L = PRIMARY LEAKAGE INDUCTANCE

Fig. 10. Output Circuit

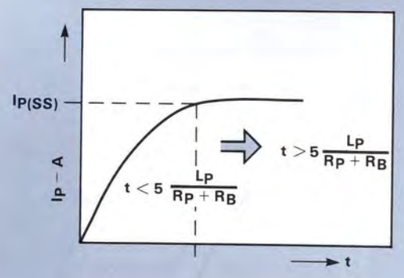


Figure 11

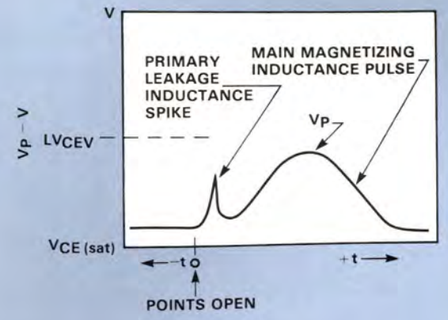
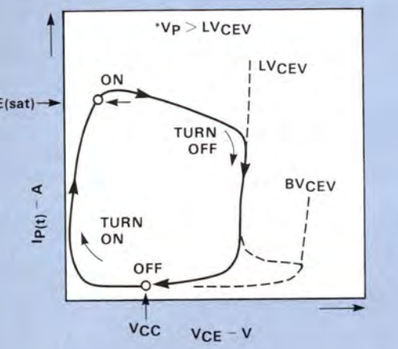
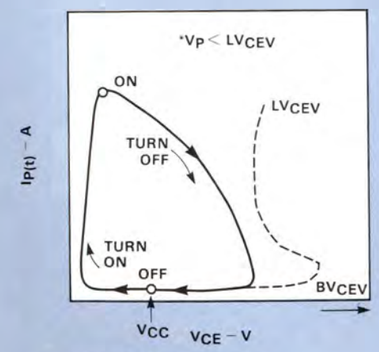


Fig. 12. Primary Voltage (not to scale)





*OPEN SECONDARY CONDITIONS

Fig. 13. Output Transition Inductive Load Line

The energy stored in the ignition coil primary is

$$E_P = \frac{I_P^2(t)L_P}{2}$$

For the steady-state current to be realized, the output-transistor current gain, β, must be

$$\beta_1 \geqslant \frac{I_{P(SS)}}{I_{D(MIN)}} \quad @ \quad V_{CE} = V_{CE(SAT)}, \text{Temp} \leqslant -40^\circ\text{C}.$$

All external parameters should be derated to accommodate this temperature extreme.

The moment the distributor cam lobe comes in contact with the rubbing block, the contacts open causing Q1 to switch off. This initiates a rapid collapse of the stored magnetic field in the inductance L_P, the time of which is limited only by the natural resonant frequency of $L_P + L_L$ and C'_S. This is true as long as Q1 fall time is negligible, *i.e.,* if

$$t_{off(Q1)} \ll \frac{\pi}{2}\sqrt{(L_P+L_L)C'_S}$$

This is the case for most high speed switches. The waveform at the collector of Q1 for an open plug condition (maximum available voltage) is shown in *Figure 12*. The peak amplitude of these voltages varies primarily as a function of stored energy, therefore, to insure that secondary breakdown does not occur in Q1, the $BV_{CEV(Q1)}$ rating must exceed the worst-case main magnetizing-inductance peak voltage. If this is not the case, then the energy content of the area under the curve, by which V_P exceeds BV_{CEV}, must be much less than the energy required to destroy the device. For maximum reliability, the first choice is the more logical one.

Figure 12 represents a worst-case requirement because it implies no shunt resistance across the primary. In practice, when the spark plug voltage reaches the breakover level, the plug ionizes and introduces an effective voltage clamp across the coil primary. The clamping level depends primarily upon spark-plug gap opening. Therefore, the magnitude of V_P is controlled by cylinder conditions. The primary leakage inductance spike is not affected by secondary conditions, therefore, as a minimum requirement, the output transistor must be able to withstand the energy content of this pulse in its forward safe-area region. The forward safe-area rating of the output device should be wide enough to enclose $V_{P(MAX)}$ and $I_{P(SS)}$, a feasible situation under open secondary conditions. The output device inductive load line is shown in *Figure 13*.

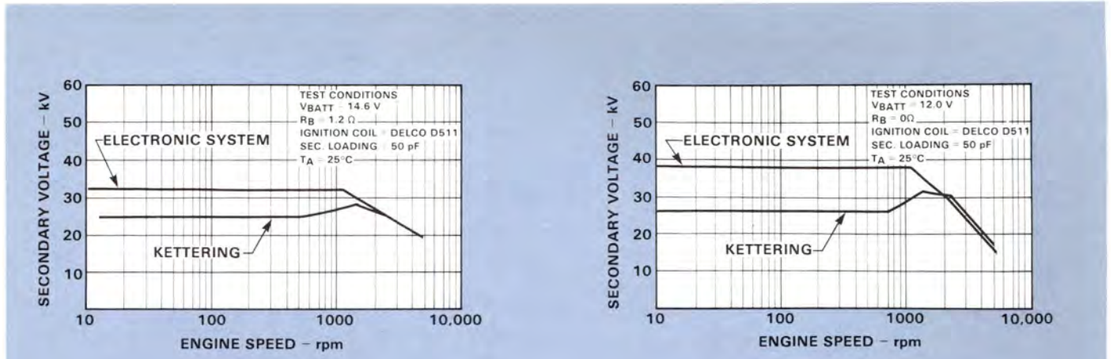


Figure 14

The last major device parameter that should be mentioned is power dissipation. For all non-current limit-type ignition systems, the worst-case power dissipation is encountered under steady state conditions, *i.e.,* ignition key on, breaker points closed. At this time, the power dissipation of the device is

$$P_D = \left(\frac{V_{BATT}}{R_B+R_P}\right)V_{CE(SAT)}$$

The device should be capable of maintaining a below-rated junction temperature at this power level, at a worst-case ambient temperature of 100°C. For current-limited devices, the power dissipation under current-limit conditions could be higher than the above, *i.e.,*

$$P_{D(LIM)} = \left(V_{CC} - [I_{LIM}(R_B+R_P)]\right)I_{LIM}$$

$P_{D(LIM)}$ becomes greater than P_D as $R_B + R_P$ becomes smaller for a given current-limit level, I_{LIM}.

Systems Environmental Requirements

Any electronic ignition system to be used in an automobile could be exposed to one or more of the following environmental situations.

Environmental Condition	Worst-Case Level
Ambient temperature (under hood)	–40°C to +100°C
Humidity, relative @ 37°C	98%
Salt atmosphere	
Mechanical vibration	
Mechanical shock	
Electrical transients (long term)	125 V for 4.5 s
Noise (EMI)	

CONCLUSION

The superior performance of the breaker-point electronic ignition system compared to the conventional Kettering system is illustrated in *Figure 14*. When compared to other available electronic ignition systems, the breaker-point ignition requires the least amount of effort and mechanical expertise to install. Its distinct advantages over the Kettering system are summed up briefly below.

ADVANTAGE	WHY
Longer point life	No arcing across points
Maintains timing accuracy longer	No change of point setting due to arcing
Higher voltage available at spark plug	More energy available plus faster switching time
Longer plug life	Ability to fire a wider gap or a more deteriorated spark plug
Easier starting and smoother idling	Maximum voltage available at low rpm
Improved fuel economy	Stays in tune longer
Less emissions	More efficient burning of mixture

The only way to improve on the breaker-point system would be to replace the points completely with a solid state device. This will be the subject of a future article.

IGNITION SYSTEM TERMINOLOGY AND DEFINITIONS

Kettering Ignition System—Inductive system commonly used for internal combustion engines. Employs induction coil, breaker contacts, capacitor, and suitable power supply such as a battery.

Semiconductor Ignition System—An ignition system for internal combustion engines employing the use of solid-state semiconductors for switching purposes.

Inductive System—An ignition system that stores its primary energy in an inductor or coil.

Capacitor Discharge System—An ignition system that stores its primary energy in a capacitor.

Types
Breaker Triggered—A semiconductor system that utilizes conventional breaker contacts to time and trigger the system.

Breakerless—A semiconductor system that does not use mechanical breaker contacts for timing or triggering purposes, but retains the distributor for distribution of the secondary voltage.

Distributorless—A semiconductor ignition system that does not utilize breaker contacts to time or trigger the system nor does it utilize a distributor for distribution of the secondary voltage.

PARAMETER DEFINITIONS

Secondary Available Voltage (Evaluation)
Open Circuit—The secondary output voltage delivered by the ignition system with a 50 pF secondary load, measurement to be taken at the supply voltage specified after the system has been temperature stabilized.

Secondary Available Voltage (on Engine)—Secondary available voltage is the voltage that is available for firing the spark plug. Data for available voltage curve are obtained by making a connection from the secondary coil terminal to the input of a cathode ray oscilloscope (through a voltage divider), then disconnecting the longest spark plug lead from its plug and observing the voltage developed on that lead. The plug end of this lead is taped to prevent flashover to grounded areas, and the lead is arranged in about the same position with respect to engine-grounded areas as it would be if connected to the spark plug. Unless otherwise specified, the longest lead is selected because the higher electrostatic capacity of that lead will give it the lowest available voltage.

Readings are made at constant engine speed, at various increments from idle to speed. At each check point, the speed is held for a sufficient length of time for the observer to be reasonably sure that he has observed the maximum, most usual, and minimum voltages that are likely to occur. Usually, only the minimum values are plotted.

Required Voltage (Engine or Vehicle)—The voltage required to fire the spark plugs. Requirement data are obtained using the same instrumentation as for available voltage runs, but with all spark plug leads connected. Values plotted are the maximum voltage observed viewing all cylinders simultaneously. Requirements are usually determined with the engine operating at full load (wide-open throttle) and under a variety of part-load conditions to ascertain the maximum required voltages.

Ignition Reserve (Engine or Vehicle)—The difference between the minimum available and maximum required voltages. An adequate ignition "safety factor" is important if an engine is to be reasonably free from troubles caused by moisture or dirt losses, "leaky" secondary leads, and fouled spark plugs.

Rise Time—The time required, in microseconds, for the output voltage wave form to rise from 10% of maximum to 90% maximum output. Measurement to be made under the same conditions as the secondary available voltage.

Average Current—The input current to an ignition system as measured on a dc ammeter. In most instances the engine speed must also be specified.

Peak Coil Current—Applies to inductive systems only, and is the peak current flowing through the ignition coil primary winding at the instant the contacts open.

Contact Current—The peak current flowing through the contacts of a contact-triggered system at the instant the contacts open.

Spark Duration—The length of time a spark is established across a spark gap or the length of time current flows in a spark gap.

Primary Voltage—The peak magnitude of the first half cycle of the voltage induced across the induction coil primary winding.

Timing Lag—The number of engine degrees retard in timing caused by electrical lag in the system. Generally stated as number of engine degrees per 1000 rpm engine speed.

Cut-In Speed—The minimum speed at which the ignition system will operate properly. Distributor and/or engine rpm should be specified.

Stored Energy—The amount of energy stored in the primary of the ignition system.

Inductive System

$$W_p = \tfrac{1}{2} Li^2$$

where:

W_p = energy stored in the primary field, joules
L = primary inductance, henries
i = current flowing in the primary winding, amps

Capacitor Discharge System

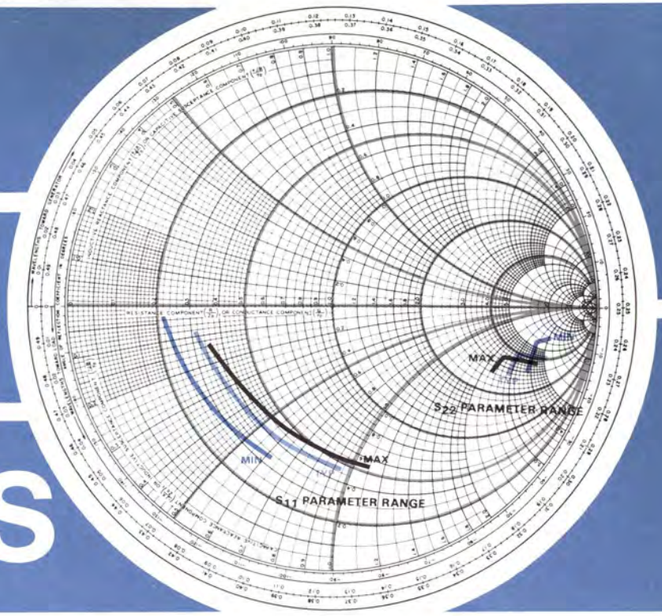
$$W_p = \tfrac{1}{2} CE^2$$

where:

W_p = energy stored in the primary capacitor, joules
C = primary capacitance, farads
E = peak primary voltage, volts

Report of Electrical Equipment Committee approved January 1970. SAE recommended practice.

FEED BACK STRAYS



STRAYS STRAYS STRAYS STRAYS STRAYS STRAYS STRAYS

by Will Alexander

Stray capacitance and stray lead inductance have always concerned circuit designers. Stray emitter lead inductance is known to reduce gain; the effect on stability is unclear. Stray collector-to-base capacitance is known to reduce both gain and stability, but how much? Evaluation of the effects of strays is a big and unrewarding task, but SPEEDY* can make it easier and also clear up the above uncertainties.

STRAY INDUCTANCE AND STRAY CAPACITANCE

Stray inductance can be added to any or all of the transistor leads in combination with stray capacitance between any two of the three leads. Of all the possible combinations, only two have strong effects on transistor performance. Stray inductance in the common lead (emitter) and stray capacitance between input (base) and output (collector) are the important strays because they introduce feedback, thus reducing gain and often stability. In narrow band amplifiers, other strays can be tuned out and thus are of little importance. In some cases, strays actually help match the transistor to its source impedance. In wide band amplifiers, strays can be troublesome, but again, some wide band amplifiers appear to like certain strays.

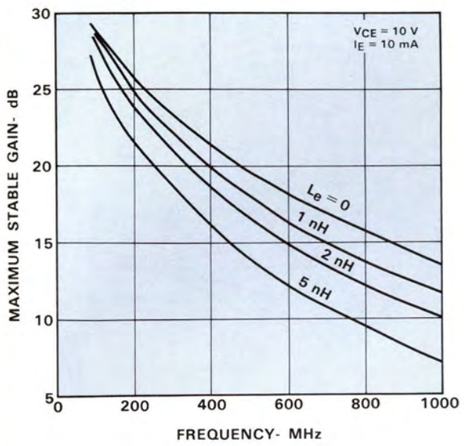
*Description of this system available upon request

CALCULATED PERFORMANCE

To determine the effect of feedback strays, the user need only make up a SPEEDY file, using scattering parameters available from the S DATA file and adding a circuit description which includes the strays. Following directions to analyze the data, SPEEDY calculates new S parameters and provides data on the transistor performance factors briefly reviewed below.

Maximum stable gain (MSG or G_{MS}) is the most important figure of merit. Transistors with high MSG are easy to match, easy to tune and give high performance, trouble-free amplifiers. MSG is simple to measure or calculate as it is the ratio of the forward voltage gain to the reverse voltage gain.

Maximum available gain (MAG, G_{MA} or $G_{A(MAX)}$) can be achieved when the transistor is unconditionally stable, that is when the stability factor, K, is greater than 1. When K is less than 1 the transistor should be loaded until K is 1 or larger. When K is 1, MAG and MSG are equal. Conservative design requires that MAG be 2 to 3 dB lower than MSG. It is difficult to determine accurately, as it involves measuring amplifier gain under perfectly matched conditions or making complex calculations with all four transistor parameters.



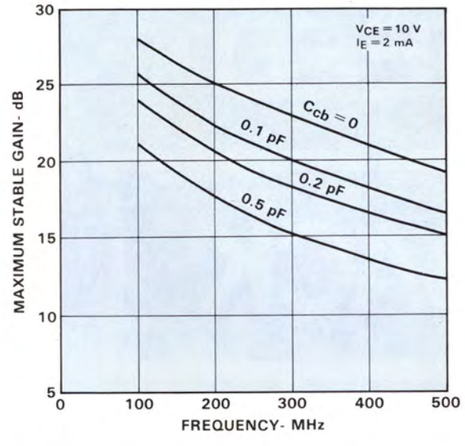
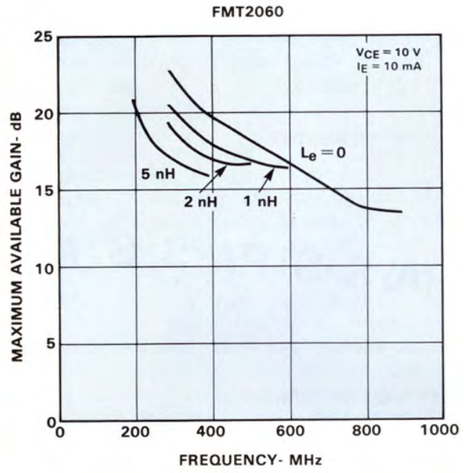


Figure 1.



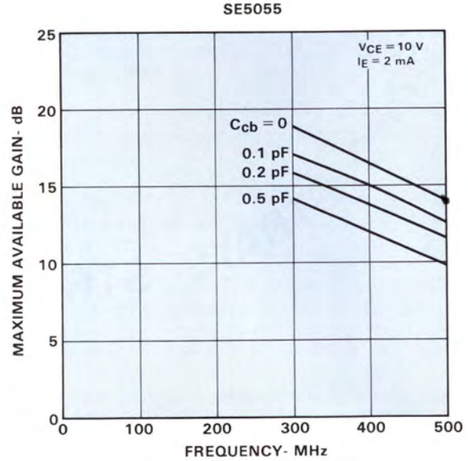


Figure 2.

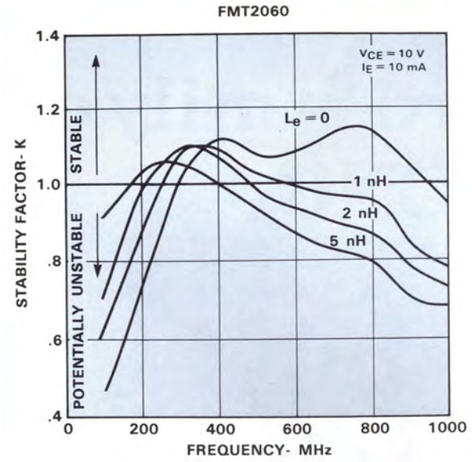
Rollett's stability factor (K) shows when an amplifier is stable ($K > 1$), or potentially unstable ($K < 1$). It also indicates the sensitivity of the amplifier, and amplifiers with K less than 1.1 are difficult to tune. K can be calculated fairly easily if MAG and MSG are known.

Transistor input and output impedance can be conveniently shown on a Smith Chart. The magnitude of the input or output reflection coefficient changes slowly with frequency and results in circular arcs on the chart.

CHOICE OF TRANSISTOR

For a worst-case analysis, transistors with minimum emitter lead inductance, L_e, or collector-to-base capacitance, C_{cb}, are chosen. The selection really narrows down to the best package. The physical size and construction of the Micro-T make it a natural for emitter-lead-inductance calculations. It is the best of the low cost packages with an internal emitter lead inductance of less than 1 nH. The transistor chosen for these sample calculations is the FMT2060.

To evaluate collector-to-base stray capacitance, an SE5055 is used. It is packaged in a TO-72 with the emitter and base leads reversed, therefore base and collector leads are diametrically opposite. This version of the TO-72 package is preferred because the transistor C_{cb} is a remarkable 0.13 pF. Also the device maintains its low capacitance on the pc board due to the shielding effects of the isolated case plus the in-circuit shield of both the emitter and case leads.



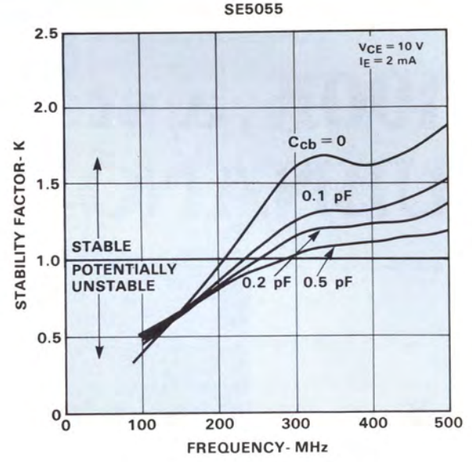


Figure 3.

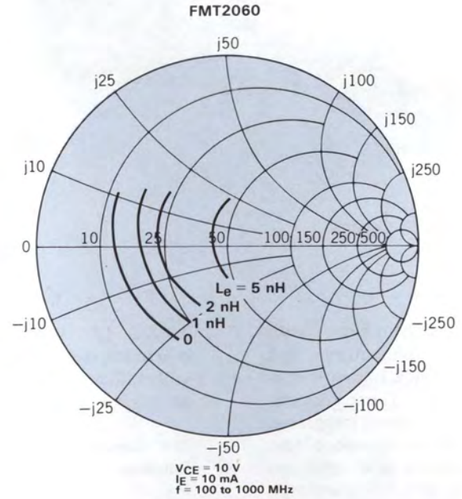


Figure 4.

RESULTS FROM SPEEDY

The graphs in Figure 1 show a reduction in maximum stable gain for an increase in either stray. For emitter lead inductance, the maximum available gain decreases with frequency as might be expected (Figure 2). For collector-to-base capacitance, both MAG and MSG reductions are almost independent of frequency.

Feedback strays decrease the stability factor at high frequency, but when $K < 1$, feedback appears to increase the stability factor (Figure 3). This increase is especially apparent for stray emitter lead inductance. The change of input impedance with emitter lead inductance is quite large. (Figure 4). This change would tend to cast doubt on the measurement of the real part of the input impedance, h_{ie}, to find the transistor base resistance, r_b'.

OTHER STRAYS

There are two interesting strays that were not analyzed. A small emitter bypass capacitor is worth studying, especially if it is used to series resonate the emitter lead inductance. Also, a small unbypassed emitter resistor gives surprising results, especially with respect to the stability factor.

REFERENCES

P. Sturzu; "Dial S DATA for CAD;" PROGRESS, Vol. 2, No. 6, June 1974

M. Vellequette; "High Frequency Computer Aided Design;" PROGRESS, Vol. 2, No. 8, August 1974

D. Porter; "S DATA*II, S-Parameter Data Bank with Interpolation;" PROGRESS, Vol. 3, No. 1, January, February 1975

F100K, a standard family of SUBNANOSECOND ECL

By J. W. Hively, H. H. Muller and W. K. Owens

Competitive pressure in the data processing industry, with ever-increasing data volumes and new architectures, has stimulated the need for faster processing rates, higher machine densities, and greater system reliability. These requirements can only be met by the use of higher speed integrated circuits with more on-chip integration and multipurpose logic functions. Advanced packaging techniques and optimum system interconnects must be applied to take full advantage of this increased circuit performance. To facilitate system architecture, these high performance integrated circuits also must be less sensitive to environmental influence, i.e., easier to use and have a tighter ac window.

The new F100K standard subnanosecond ECL family has been designed to meet all these requirements. It was planned to provide next-generation system performance and density without total use of LSI while still being compatible with LSI approaches. Fully compensated ECL is used to eliminate most of the traditional ECL limitations while retaining all the advantages.

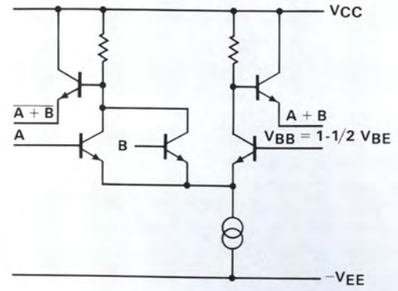
SELECTION OF CIRCUIT APPROACH

Many circuit implementations were carefully considered prior to selecting the optimum gate configuration for the F100K family. Some of the circuits studied are shown in *Figure 1*. The emitter-follower current-switch (E^2CL) and current-mode logic (CML) gates were eliminated mainly because of poor capacitive drive and lack of output wired-OR capability. The CML gate also has low noise margins. The 2-1/2D, EFL, DCTTL and hysteresis gates were eliminated due to the lack of simultaneous complementary outputs along with difficult temperature and voltage compensation characteristics that lead to the loss of system noise immunity.

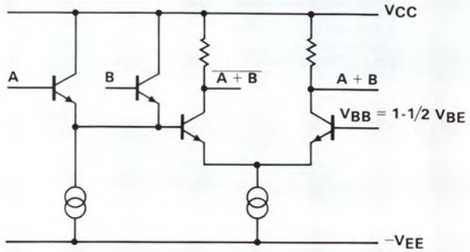
The choice narrowed down to the current-switch emitter-follower ECL gate which offers the following characteristics:

- High fan-out capability
- Simultaneous complementary outputs
- Excellent ac characteristics
- Compatability with existing ECL logic and memories
- Series gating capability
- Good noise immunity
- Amenable full compensation and extended temperature characteristics
- External wired-OR capability

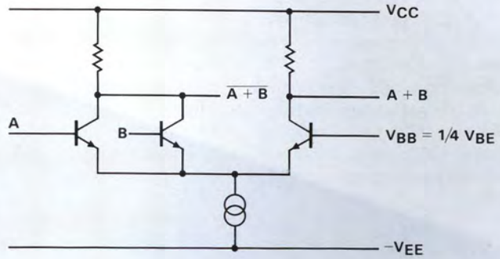
F100K circuits operate with a V_{EE} power supply of −4.5 V ±7% to reduce power dissipation. However, a −5.2 ±10% power supply can be used if desired since these circuits are fully voltage and temperature compensated. Therefor F100K directly interfaces with the widely available 2-r ECL circuits. It should be emphasized that F100K is a *standard ECL family* with subnanosecond switching speed. Major segments of the computer industry were involved in its definition to ensure its acceptance as a standard product family.



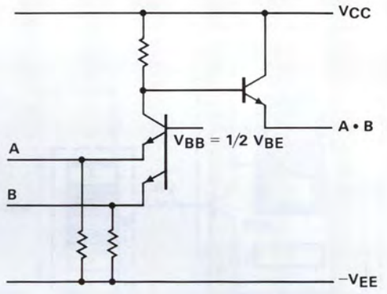
a. ECL Current-Switch Emitter-Follower



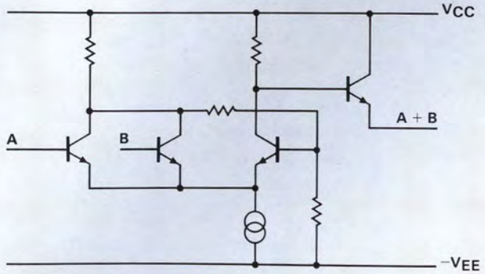
b. E^2CL Emitter-Follower Current Switch



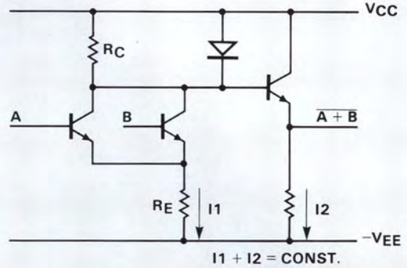
c. CML Current Mode Logic



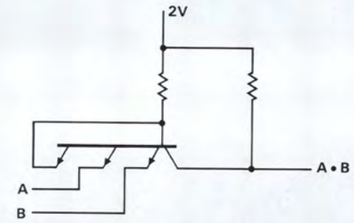
d. EFL Emitter-Follower Logic



e. FBG Feedback Gate, Hysteresis Gate



f. 2-1/2 Diode Logic



g. DCT^2L AND Gate

Fig. 1. Gate Configuration Options

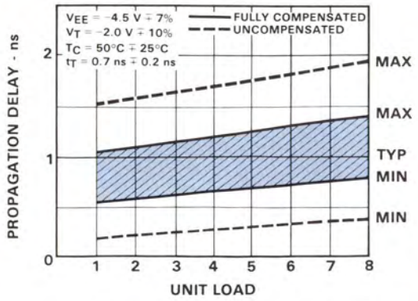


Fig. 2. Comparison of Propagation Delays

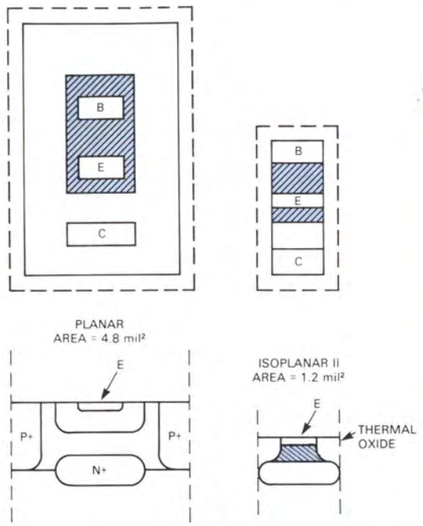


Fig. 3. Transistor Structures

F100K PHILOSOPHY

The four key features of F100K are high speed at reduced power, high level of on-chip integration, most flexible logic functions available to date, and optimum I/O pin assignment.

The high speed is obtained by the use of ECL design techniques and the advanced Isoplanar II process. All circuit inputs have similar loading characteristics to ease drive requirements, i.e., buffers are incorporated where an input pin would normally drive more than one on-chip gate. The on-chip delay incurred by buffering is less than the system delay caused by an output which drives a capacitance of higher than 3 unit loads. Full compensation was selected for the F100K family to provide improved switching characteristics. Full compensation results in constant signal levels, constant thresholds and improved noise margins over temperature and voltage variations from chip to chip, and thus a tighter ac window in the system environment. A comparison of fully compensated ECL to conventional ECL shows a 2:1 improvement in system ac performance due solely to full compensation (*Figure 2*). And, the improved speed has been achieved at reduced power. This power reduction is accomplished by the use of advanced process technology that reduces parasitic capacitances and improves tolerances, by optimum circuit designs using series gating and collector and emitter dotting, and by designing for the use of a −4.5 V V_{EE} power supply.

Higher on-chip integration is made possible by using the 24-pin package to increase the number of pins available for logic by 62% over the conventional 16-pin package. The emphasis in F100K is to minimize the number of SSI functions and maximize the use of MSI and LSI to reduce wiring delays and thus make more efficient use of the fast on-chip switching technology. Only 10 SSI functions are needed to serve all the system needs presently requiring 25 functions in the ECL 10K family.

The logical extension of the F100K family is LSI and already a function providing the equivalent of up to 285 gates, *i.e.,* a 16 x 4 read/write register file, is being developed.

F100K was planned to minimize the total number of logic functions by increasing the flexibility of each function and by making use of more I/O pins. Since next-generation system performance and ease of system designs are major F100K goals, pin assignment is important and was planned to minimize crosstalk, noise coupling and feedthrough, to facilitate OR-ties and ease power-bus routing. Some of the key considerations in selecting the F100K pin assignments were:

- Locate power pins in the center on opposite sides of the package to ease system design and chip layout and to provide low inductance connections.
- Provide two V_{CC} pins, one for the circuit reference and one for the outputs to minimize noise coupling and maximize logic flexibility.
- Locate in-phase outputs adjacent to input pins, where possible, to prevent slowdown due to feedback.
- Locate inverting outputs of logically independent gates adjacent to each other for the shortest possible wired-emitter OR-ties. This provides an AOI function.
- Locate common pins such as common reset and common clock at pin number 22 and address or control inputs at pins 19 and 20. This is to maximize use of CAD for board layouts.
- When feasible, to create multipurpose functions, mode control pins are used to change the character of the functions. These pins can either be controlled by standard logic levels or hard wired, *i.e.,* tied to V_{CC} or left open.

REALIZATION

The fabrication technology of the F100K family is the advanced Isoplanar II process which provides transistors with very high, well controlled switching speeds, extremely small parasitic capacitances and f_T in excess of 5 GHz.

The technology can best be described by comparing the integrated circuit transistor structures of the conventional Planar* process and that of the Isoplanar II process *(Figure 3).* The top view shows the area needed for each structure; the dashed area is the center of the isolation area.

*Planar is a patented Fairchild process.

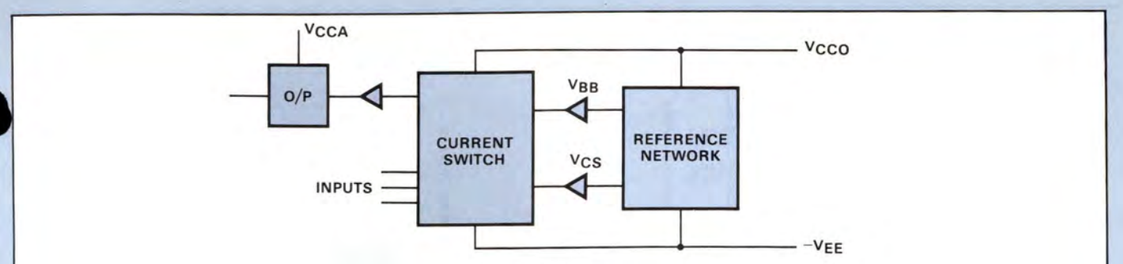


Fig. 4. ECL Gate

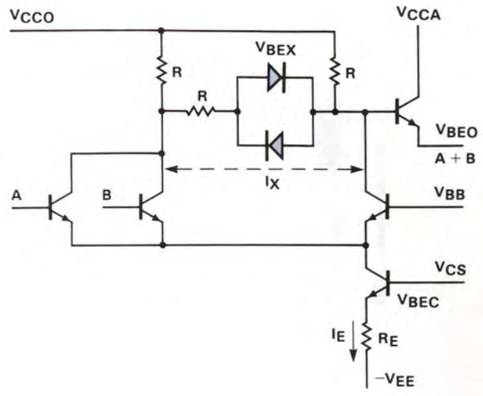


Fig. 5. Temperature Compensation

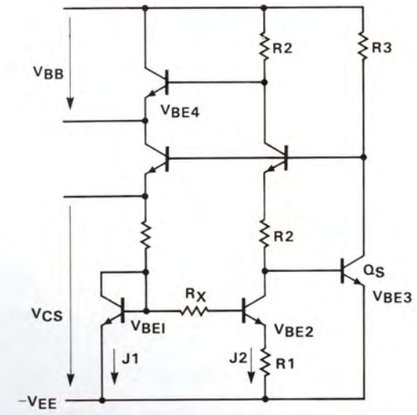


Fig. 6. Reference Network

In the Isoplanar process, a thick oxide is selectively grown between devices instead of the P+ region which is present in the Planar process. Since this oxide needs no separation from the base-collector regions, a substantial reduction in device and chip size can be realized. The base and emitter ends terminate in the oxide wall therefore the masks can overlap the device area into the isolation oxide. This overlap feature means that base and emitter masking does not have to meet the extremely close tolerances that might otherwise be necessary, and standard photolithographic processes can be used.

The "walled emitter" structure allows over a 70% reduction of the transistor silicon area compared to that a conventional Planar transistor. For a given emitter size, the collector-base area is also reduced by more than 60%. The reduced junction areas result in corresponding reductions in collector-base and collector-substrate capacitances.

Since the active transistor area is only under the emitter, all capacitance and resistance values outside this area are reduced. Parasitic values are further reduced by taking advantage of the masking alignment latitude resulting from the self-aligning nature of the structure.

The heart of F100K is fully compensated ECL[2]. The basic gate consists of three blocks – the current switch, the output emitter followers, and the reference or bias network *(Figure 4).* The current switch allows both conjunctive and disjunctive logic. The output emitter followers provide high drive capability through impedance transformation and allow for increased logic swing. The bias network sets dc thresholds and current-source bias voltages. Temperature compensation at the gate output is achieved by incorporating a cross-connect branch between the complementary collector nodes of the current switch and driving the current source with a temperature insensitive bias network[3] *(Figure 5).*

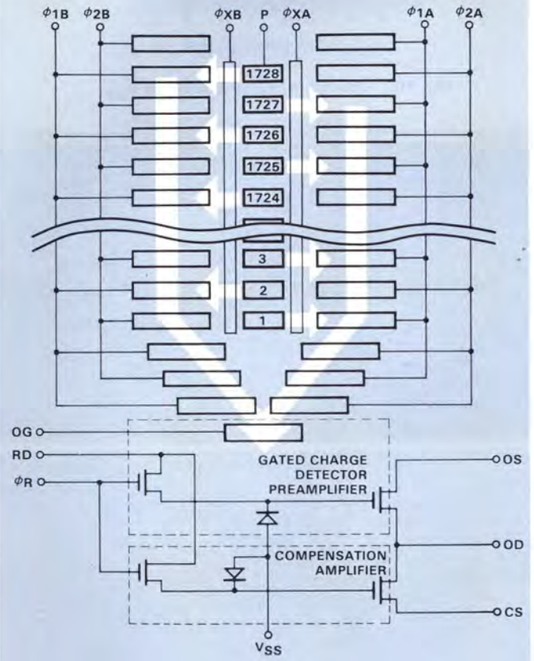
As junction temperature increases and the forward base-emitter voltage of the output emitter-follower decreases, the collector node of the current switch must become more negative. Since the current-source bias voltage, V_{CS}, is independent of temperature, the switch current increases with temperature due to the temperature dependence of V_{BEC}. The combination of temperature controlled current, I_e, and the cross-connect branch current, I_x, forces the proper temperature coefficient at the collector node of the current switch to null out the V_{BEO} tracking coefficient.[1]

The schematic for the reference network displays a V_{BE} amplifier in the bottom left corner *(Figure 6).* Two base-emitter junctions are operated at different current densities, J1 and J2. The resulting voltage difference, V_{BE1} minus V_{BE2}, appears across R1 and is amplified by the ratio R2/R1. Note that R2 is used twice, once to generate V_{CS} and once to generate V_{BB}. The different current densities, J1 and J2, result in a positive temperature tracking coefficient across R2, which cancels the negative diode-tracking coefficient of V_{BE3} and V_{BE4}. The V_{CS} and V_{BB} thus generated are temperature insensitive at the extrapolated bandgap voltage of silicon[2,3] (approximately 1300 nV).[4] RX in the V_{BE} amplifier compensates for process variations of β and $\triangle V_{BE}$[5]. Voltage regulation is achieved through a shunt regulator shown at the right side of the schematic.

NEW PRODUCTS

Recently announced devices presently available. Order specifications by product number.

CCD121 BLOCK DIAGRAM



CHARGE-COUPLED LINEAR IMAGE SENSOR HAS 1728 ELEMENTS

The CCD121 is a monolithic self-scanned 1728-element charge-coupled image sensor designed for page scanning; specifically it provides a 200 line per inch resolution across an 8-1/2 inch page. The device may also be used for facsimile readers, optical character recognition, as well as imaging applications that require high resolution, high sensitivity and high speed.

In addition to a row of 1728 sensing elements, the CCD121 chip includes: two charge transfer gates, two 2-phase analog shift registers, an output charge detector/preamplifier, and a compensation output amplifier. The 2-phase analog shift registers both feed the input of the charge detector resulting in sequential reading of the 1728 imaging elements.

Fabricated using buried-channel n-channel Isoplanar technology, the CCD121 is packaged in a 24-lead DIP with a glass window and a low-reflectance optical cavity.

MOS FIFO FOR DATA RATE BUFFERING

A new p-channel MOS FIFO (First-In First-Out) memory organized 40 words by nine bits is now available. The 3351 acts as an "elastic" memory between two or more subsystems that operate at different speeds. Words are accepted at the input, automatically shifted towards the output and may be removed at any rate in the same sequence as the entry. The 3351 features high load and unload speeds, independent asynchronous inputs and outputs, total TTL compatibility without additional components and 3-state outputs. Word length may be easily expanded by using a cascading scheme requiring no additional logic. Packaged in a 28-pin ceramic DIP, the 3351 operates over the commercial temperature range, 0°C to 70°C.

11C00 SERIES DESIGNED FOR INSTRUMENTATION AND COMMUNICATIONS MARKETS

The six members of the 11C00 family are functional elements specifically designed for communications, instrumentation, entertainment and industrial control electronics. The 11C01 is an ECL dual 5-4 input OR/NOR gate providing very high speed, typically 700 ps delay. Operating from standard ECL or TTL power supplies, the 11C05 ECL divide-by-four counter offers a maximum operating frequency above 1 GHz over the 0° to 75°C temperature range. The 11C06 is a high speed ECL D-type flip-flop capable of toggle rates over 750 MHz. Designed primarily for high speed prescaling, it can also be used in any application which does not require preset inputs. The 11C44 phase/frequency detector contains several of the functional elements used in phase-locked loop applications – a phase/frequency detector, a phase detector, a charge pump, and an amplifier. It is especially useful for motor speed control, frequency synthesizers, and clock recovery from encoded data. The 11C24 and 11C58 voltage-controlled multivibrators operate over broad frequency ranges – dc to 30 MHz for the 11C24 dual TTL VCM and dc to 155 MHz for the 11C58 ECL VCM. Operating frequency is determined by an applied voltage in conjunction with an external capacitor. These devices are used as clock generators and as variable frequency elements in phase-locked loops.

INDUSTRY STANDARD CORE MEMORY DRIVERS AND SENSE AMPLIFIERS AVAILABLE

The 55325/75325 core memory drivers convert standard TTL signals into high current, high voltage signals for driving core memories. Each device contains four 600 mA switches, two source switches and two sink switches; selection is made by the appropriate logic and strobe inputs. The output transistors are capable of withstanding 24 V and the sink output transistors have internal voltage surge protection for switching inductive loads.

The 7528/7529, 7534/7535, and 75234/75235 dual core memory sense amplifiers sense low-level analog pulses of a core memory and transform these pulses into TTL/DTL signal levels. Two different threshold selections are available: ± 4 mV maximum variation for the 7528, 7534 and 75234 and ± 6 mV maximum variation for the 7529, 7535, and 75235. The ± 4 mV devices are ideal for use in high speed core memories, and the ± 6 mV devices provide an economical trade off where cost is a concern.

CIRCUIT IDEAS Digital

by Peter Alfke

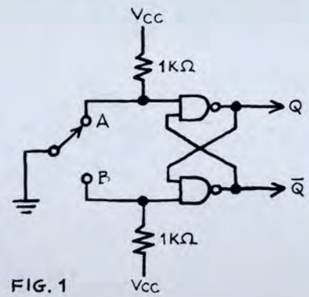


FIG. 1

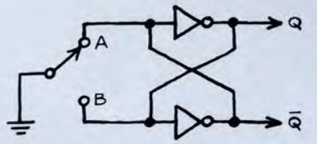


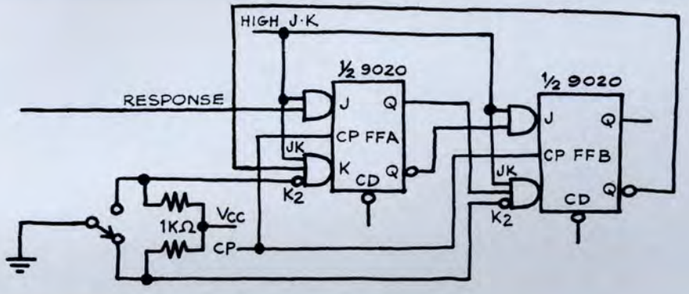
FIG. 2

SWITCH DEBOUNCER

Interfacing switches, relay contacts, or push-button contacts to digital systems requires some special precautions. All switch contacts bounce, *i.e.,* during closing, they dissipate excess mechanical energy by opening and closing several times, sometimes as long as 10 ms, before they settle in the closed condition. Using the switch to directly control a digital system can lead to ambiguous operation; using it as a clock or count input inevitably results in multiple triggering and counting.

A switch debouncing latch consisting of two cross-coupled latches is the well known solution to this problem. *Figure 1* shows the straightforward implementation using TTL or CMOS NAND gates. Each switch requires one-half a gate package and two pull-up resistors. The latch is set (Q goes HIGH) as soon as A is grounded and stays HIGH (independent of contact bounce) until the contact is moved back all the way and B is grounded.

Figure 2 shows a simpler configuration that performs the same function but requires only one-third of a hex inverter package and *no* pull-up resistors. The on-resistance of the switch must be low enough to force the gate output to ground (< 10 Ω for TTL, < 100 Ω for CMOS); but, once the latch has switched, *i.e.,* a few nanoseconds after the first contact closure, the contact current is reduced to almost zero.



SWITCH SYNCHRONIZER

In many digital systems, a switch is used to initiate a routine or program. This seemingly simple task poses several design problems for the following reasons.

- The switch is activated asynchronously
- It bounces
- It may or may not stay activated longer than it takes to complete the routine.

The circuit shown above implements this function using only one dual flip-flop, the 9020, and a single-pole double-throw (SPDT) switch. When the switch is not activated, FF A is set and FF B is reset (A $\bar{B}$). Depressing the switch activates the $\bar{K}$ input of FF A, causing the next clock pulse to reset it (A $\bar{B}$). This activates the J input of FF B, causing the subsequent clock pulse to set it ($\bar{A}$ B). The two flip-flops stay in this state regardless of any changes in the switch because the active LOW $\bar{K}$ inputs from the switch are inoperative due to a LOW level on the other K inputs. When the routine or program ends, the Response input goes HIGH, causing the next clock pulse to set FF A (A B). If the switch has been released, the subsequent clock pulse resets FF B (A $\bar{B}$), returning the system to the idle state. If the switch has not yet been released, the AB state persists until the switch is released and the next clock pulse resets FF B, returning the system to the idle state. In either case, FF A can be used as a synchronous control flip-flop.

The Interface Handbook
Line Drivers
and Receivers

Digital signals transmitted any distance, only a few inches in some cases or up to several miles, must enter the analog world of transmission lines before arriving at their digital destinations. Therefore, special attention should be given to the interface between the digital and analog areas – often one of the least understood considerations in a system design. This handbook is intended to shed some light on this important design procedure – interfacing of systems (or subsystems) for the transmission of information from one location to another via line drivers, transmission lines and line receivers.

The Interface Handbook is not intended to be a textbook on line drivers and receivers in the formal sense, nor is it a "cookbook" of applications since each system must be designed based on its unique requirements. It is presented as a refresher on the basics of pulse transmission line theory combined with methods for determining signal quality and feasibility of the particular data transmission system. Only those areas that directly affect the transmission of digital signals are covered. This handbook contains the essential elements to aid the system designer in making an informed decision regarding the quality of data received at the end of a transmission line.

A product information section at the back of the handbook contains data sheets and new product information to ease the part-selection dilemma. In addition to Fairchild proprietary devices, there are data sheets on a number of alternate-source devices identified with the same numbers as the "first-source" parts. For your copy of the Interface Handbook, just use the PROGRESS return card.

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