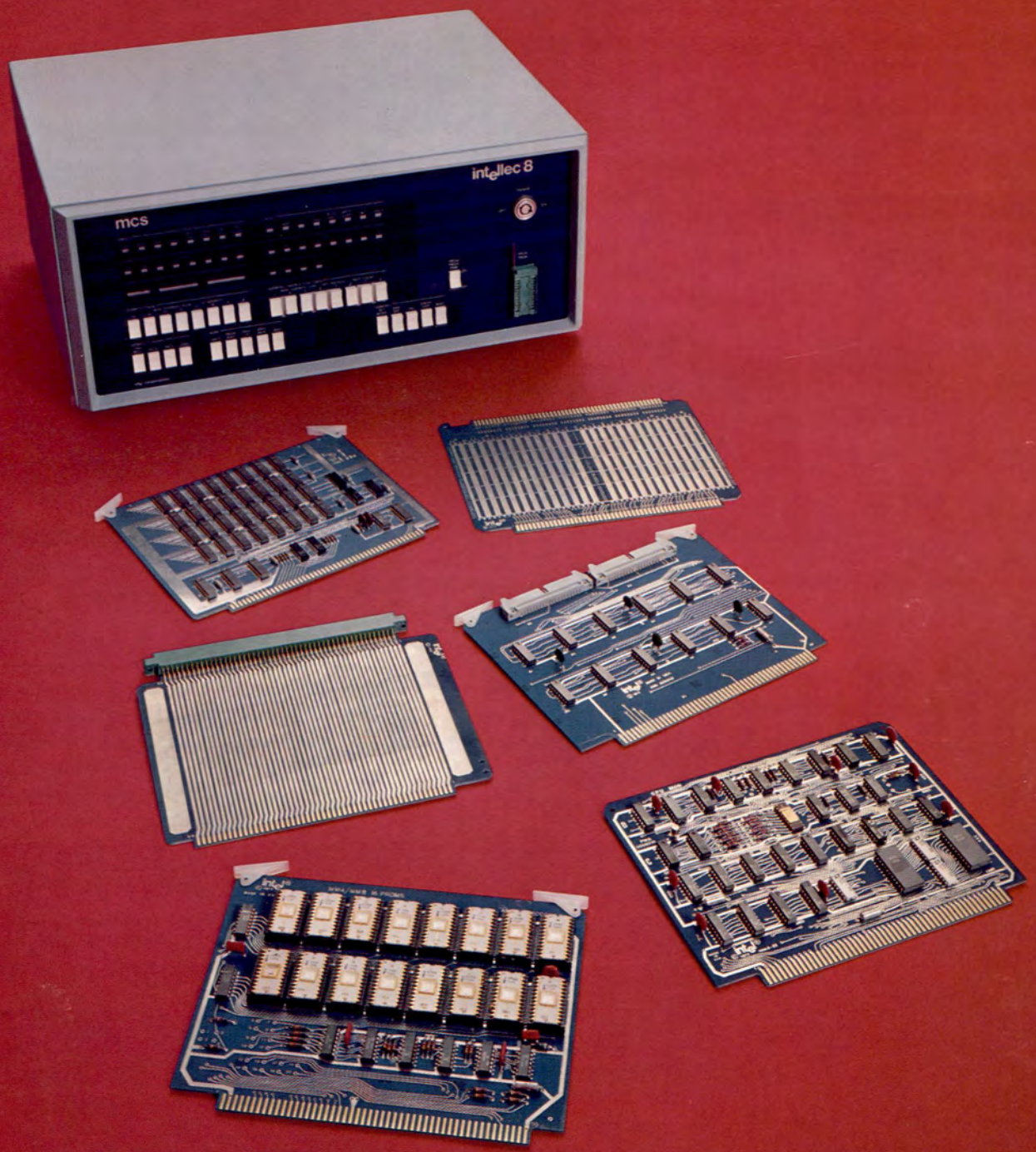
Intel Corp

intellec™

A NEW, EASY, AND INEXPENSIVE WAY TO DEVELOP MICROCOMPUTER SYSTEMS



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The Leader in Microcomputers

The widespread usage of low-cost microcomputer systems is made possible by Intel's development and volume production of the MCS-4 and MCS-8 microcomputer sets. To make it easier to use these sets, Intel now offers complete 4-bit and 8-bit modular microcomputer development systems called Intellec 4 and Intellec 8.

The Intellec modular microcomputers provide a flexible, inexpensive, and simplified method for developing OEM systems. They are self-contained, expandable systems complete with central processor, memory, I/O, crystal clock, power supplies, standard software, and a control and display console.

The major benefit of the Intellec modular microcomputers is that random access memories (RAMS) may be used instead of read-only memories (ROMS) for program storage. By using RAMS, program loading and modification is made much easier. In addition, the Intellec front panel control and display console makes it easier to monitor and debug programs. What this means is faster turn-around time during development, enabling you to arrive at that finished system sooner.

The Intellec 8 Eight-Bit Microcomputer Development System The Intellec 8 is a microcomputer development system designed for applications which require 8-bit bytes of data to perform either binary arithmetic manipulations or logical operations. The Intellec 8 comes complete with power supplies, display and control panel, and finished cabinet. It can directly address up to 16K 8-bit bytes of memory which can be any mix of ROMS, PROMS, or RAMS. The Intellec 8 is designed around the Intel 8008 central processor chip. There are 48 instructions including conditional branching, binary arithmetic, logical, register-to-register, and memory reference operations. I/O channels provide eight 8-bit input ports and twenty-four 8-bit output ports—all completely TTL compatible. The unit has interrupt capability and a two-phase crystal clock that operates at 800 kHz providing an instruction cycle time of about 12.5 μs.

The Bare Bones 8 has the same capability as the Intellec 8 only it does not include the power supplies, front panel, or finished cabinet. It is designed as a rack-mountable version.

The Intellec 8 system comes with a standard software package which includes a system monitor, resident assembler, and text editor. The programmer can prepare his program in mnemonic form, load it into the Intellec 8, edit and modify it, then assemble it and use the monitor to load the assembled program.

Other development tools for the Intellec 8 include a PL/M compiler, cross assembler, and simulator designed to operate on general-purpose computers. PL/M, a new high-level language, has been developed as an assembly language replacement. A PL/M program can be written in less than 10% of the time it takes to write that same program in assembly language without loss of machine efficiency.

The Intellec 4 Four-Bit Microcomputer Development System The Intellec 4 is a 4-bit microcomputer development system for both prototype and production applications. It contains 5K bytes of program memory, data storage, I/O, TTY interface, standard software, control panel, and power supplies—all in a small, compact cabinet. The Intellec 4 is designed around the Intel 4004 four-bit parallel central processor chip. It has a repertoire of 45 instructions, 16 working registers, a four-level address stack, and the capability of directly addressing over 43K bits of memory. The unit has a two-phase crystal clock that operates at 750 kHz providing an instruction cycle time of about 10.8 μsec.

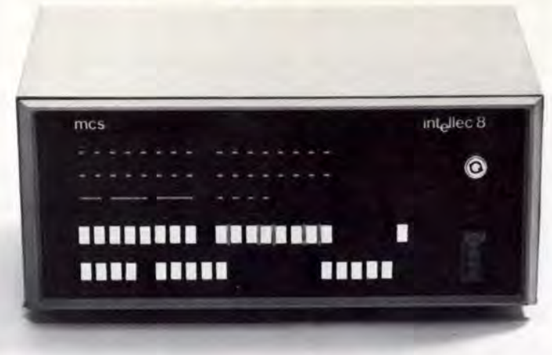
Bare Bones 4 has the same capability as the Intellec 4 only it does not include the power supplies, front panel, or finished cabinet. It is designed as a rack-mountable version.

Standard software for the Intellec 4 includes a System Monitor and Resident Assembler. Additional developmental assembler and simulator software packages written in FORTRAN IV and designed to operate on general purpose computers are also available.

Standard Microcomputer Modules Microcomputer Modules, standard cards that can be purchased individually so that the designer can develop his system with as little or as much as he needs, are also available. For example, the 4-bit Central Processor Module is a complete microcomputer system in itself. It contains the 4004 CPU, program storage, data storage and I/O, all on a single module. The 4-bit OEM Systems Module is the ultimate in volume/cost effectiveness. It contains the 4004 CPU, crystal clock and mask-programmed (4001) ROMS for program storage and RAMS (4002) for data storage.

Additional CPU, PROM Memory, Input/Output, PROM Programmer, Data Storage, Instruction Storage, Control, Universal Prototype, and other standard modules provide developmental support and systems expansion capability.

intellec 8™



Features

- Ideal for developing MCS 8 Systems.
- The Intellec 8 microcomputer system has 5K bytes of memory (expandable to 16K), I/O, TTY interface, standard software, control panel, power supplies, and a compact finished cabinet (less than 0.8 ft.^{3}). Bare Bones 8 is a rack-mountable unit and comes without the power supplies, front panel and finished cabinet accessories.
- The heart of the Intellec 8 is Intel's eight-bit "computer-on-a-chip," the 8008. This is an 8-bit parallel CPU with a repertoire of 48 instructions, seven working registers, an eight level address stack, interrupt capability, and it directly addresses 16K bytes of memory.
- DMA channel is standard.
- Standard software provided with the Intellec 8 includes a system monitor (loader, hex memory dump, instruction editor), a resident assembler, and a text editor.
- With this system, all program development may be done in RAM memory.
- A complete PROM programmer is provided as an option. After the program is firm, it may be committed to non-volatile storage in Intel's 1702A programmable and erasable Read-Only-Memory.
- Complete system control and hardware debugging aids are provided via the control panel.
- Crystal clocks are used for system stability.
- System is expandable to 16 microcomputer modules in a single chassis.

Specifications

Word Size:	Data: 8 bits Instruction: 8, 16, or 24 bits
Memory Size:	5K bytes expandable to 16K bytes
Instruction Set:	48, including: conditional branching, binary arithmetic, logical, register-to-register and memory reference operations
Machine Cycle Time:	12.5 μs
System Clock:	Crystal controlled
I/O Channels:	4 expandable to 8 input ports 4 expandable to 24 output ports } TTL Compatible
Interrupt:	Single Level
Direct Memory Access:	DMA Standard
Memory Cycle Time:	900 nanoseconds
Operating Temperature:	0°C to 55°C
Power Supplies:	+5v ± 5% 12 amps* −9v ± 5% 1.8 amps* **required for maximum system*
Physical Size:	Intellec 8: 7" x 17⅛" x 12¼" (table top only) Bare Bones 8: 6¾" x 17" x 12" (suitable for mounting in standard RETMA 7" x 19" panel space)
Weight:	30 lb.
Standard Software:	System Monitor Resident Assembler Text Editor
Support Software:	PL/M Compiler Cross Assembler Simulator } written in FORTRAN IV

Standard Systems and Optional Modules

INTELLEC 8 (imm8-80) Standard System includes the following Modules and Accessories:

Central Processor Module
Input/Output Module
PROM Memory Module
RAM Memory Module
Chassis with Mother Board
Power Supplies
Control and Display Panel
Finished Cabinet
Standard Software

System Monitor
Resident Assembler
Text Editor

BARE BONES 8 (imm8-81) Standard System includes the following Modules:

Central Processor Module
Input/Output Module
PROM Memory Module
RAM Memory Module
Chassis (rack mountable with Mother Board)
Standard Software

System Monitor
Resident Assembler
Text Editor

OPTIONAL MODULES available for the Intellec 8 and Bare Bones 8:

PROM Programmer Module with Control Software
Additional I/O or Output Modules
Additional RAM Memory Modules
Universal Prototype Module
Module Extender
Drawer Slides and extenders for Rack Mounting

Software

Standard All peripheral interface to Intellec 8 standard software is via TTY, model ASR33. The standard software includes a System Monitor, Resident Assembler and Text Editor.

A. System Monitor

1. Contained in four 1702A PROMs located on the PROM memory module.
2. Program assigned to upper 1K of memory.
3. Lower 15K of memory may then be used for either program or data storage.
4. Intellec 8 modular computer systems have a control program called a Resident Monitor in PROM so that no "bootstrap" operation need ever be performed. The monitor functions are as follows:
   a. Load RAM memory from paper tape, either in BNPF format or hexadecimal format.
   b. Display the contents of RAM memory on a printer.
   c. Modify individual bytes of RAM memory, move blocks of RAM memory, fill blocks of RAM memory with constant data.
   d. Write contents of RAM memory to paper tape in either BNPF or hexadecimal format.

B. Resident Assembler

1. Translates mnemonic code to binary machine code.
2. Loaded into system RAM memory via paper tape.
3. 4K of memory storage is required for both the resident assembler and the symbol table.
4. This two pass assembler generates a program tape which is reloaded via the monitor.

C. Text Editor

1. Loaded to system via paper tape.
2. Edits the source program during program development.

Development Support: PL/M Compiler, Assembler and Simulator In addition to the standard software available with the Intellec 8, Intel offers a PL/M compiler, cross assembler, and simulator written in FORTRAN IV and designed to run on any large scale computer. These routines may be procured directly from Intel, or alternatively, designers may contact three nation-wide computer time-sharing services: AL/COM, G.E., and Tymshare, for access to the programs.

PL/M Compiler PL/M is a high level procedure-oriented systems language for programming the Intel MCS-8 microcomputer. The language retains many of the features of a high-level language, without sacrificing the efficiencies of assembly language.

A significant advantage of this language is that PL/M programs can be compiled for either the Intel 8008 or future Intel 8-bit processors without altering the original program.

Assembler The MCS-8 Assembler generates object codes from symbolic assembly language instructions.

It is designed to operate from a time shared terminal with input by paper tape or directly from the terminal keyboard.

Simulator The MCS-8 Simulator, called INTERP/8, provides a software simulation of the Intel 8008 CPU, along with execution monitoring commands to aid program development for the MCS-8.

PL/M

A NEW HIGH LEVEL SYSTEMS LANGUAGE THAT ANYONE CAN USE AND UNDERSTAND

Intel Makes it Easier to Program the MCS-8 Microcomputer PL/M is a new high level language concept developed by Intel to meet the special needs of microcomputer system programming. For the first time, programmers can utilize a true high level language to efficiently program microcomputers. PL/M is an assembly language replacement that can fully command Intel's 8008 CPU and future processors to produce efficient run-time object code. Programming time and costs are drastically reduced, and training, documentation and program maintenance are simplified. User application programs and standard systems programs may be transferred to future computer systems that support PL/M without reprogramming. These are advantages of high-level language programming that have been proven in the large computer field and are now available to the microcomputer user.

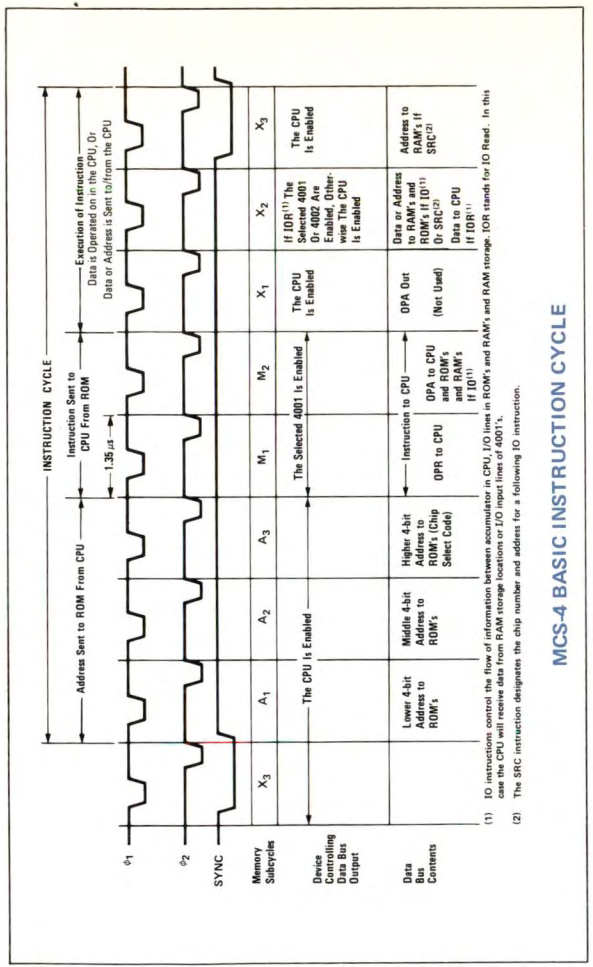
PL/M Allows the Programmer to Concentrate on the Problem PL/M is derived from IBM's PL/I. PL/I is a very extensive and sophisticated language which promises to become the most widely known and used language in the near future. The general structure of PL/I is very well suited to efficient implementation of the Intel MCS-8 microcomputer system. PL/M is a subset of PL/I with emphasis on those features of PL/I that accurately reflect the nature of systems programming requirements.

PL/M was designed by Intel to provide additional developmental software support for the MCS-8 microcomputer system. It permits the programmer to concentrate more on his problem and less on the actual task of programming than is possible with assembly language.

PL/M Coding
Program Development
Time: 15 Minutes
Number of Bytes
of Program: 114

PL/M vs ASSEMBLY LANGUAGE *As an example of comparative programming effort between PL/M and assembly language, this program to computer prime numbers was written twice, first in PL/M, and then in assembly language. The PL/M version was written in fifteen minutes, compiled correctly on the second try (an "end" was omitted the first time) and ran correctly the first time. The program was then coded in Intel MCS-8 assembly language. Coding took 4 hours, program entry and editing another 2 hours, debug took an hour to find an incorrect register designation, the kind of problem completely eliminated by coding in PL/M. Results of this one short test show a 28 to 1 reduction in coding time. This ratio may be somewhat high, overall ratio in a mix of programs is more on the order of 10 to 1. The hand coded version produced 110 8-bit bytes of program, the PL/M version: 114 bytes. In this example, in order to gain 28 to 1 in coding time, the user had to sacrifice 3% in generated code efficiency.*

Assembly Coding
Program Development
Time: 7 Hours
Number of Bytes
of Program: 110

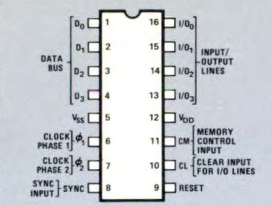


(1) IO instructions control the flow of information between accumulator in CPU, I/O lines in ROM's and RAM's and RAM storage. IOR stands for IO Read. In this case the CPU will receive data from RAM storage locations or I/O input lines of 4001's.

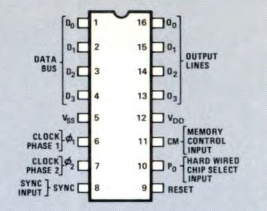
(2) The SRC instruction designates the chip number and address for a following IO instruction.

MCS-4 BASIC INSTRUCTION CYCLE

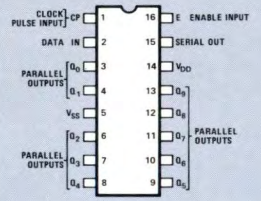
4001 ROM



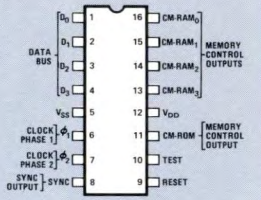
4002 RAM



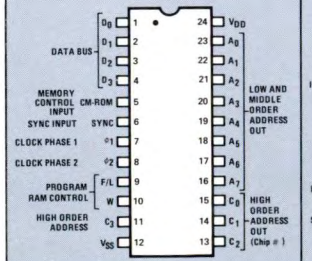
4003 SR



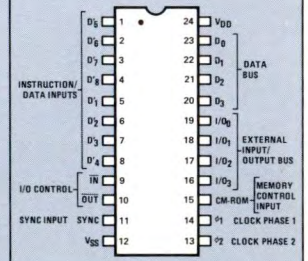
4004 CPU



4008



4009



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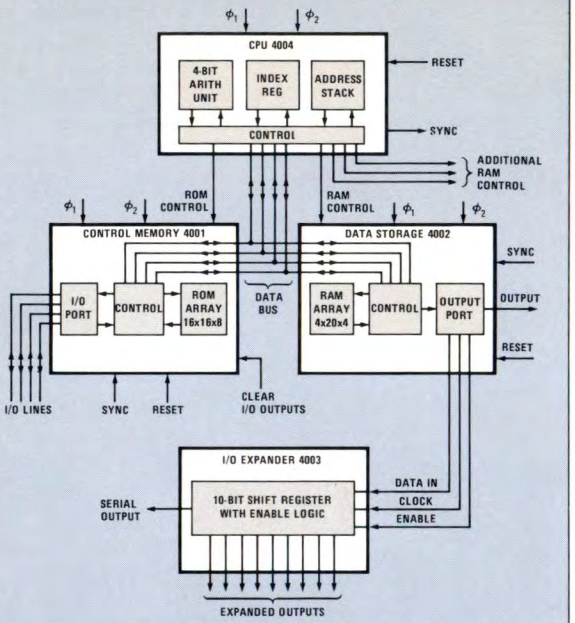
MCS-4™

MICRO COMPUTER SET



MCS-4 BASIC SYSTEM

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3065 Bowers Ave., Santa Clara, Ca., 95051
Phone: (408) 246-7501

MCS-4™ Instruction Set

[Those instructions preceded by an asterisk (*) are 2 word instructions that occupy 2 successive locations in ROM]

MACHINE INSTRUCTIONS

MNEMONIC	OPR $D_3 D_2 D_1 D_0$	OPA $D_3 D_2 D_1 D_0$	DESCRIPTION OF OPERATION
NOP	0 0 0 0	0 0 0 0	No operation.
*JCN	0 0 0 1 $A_2 A_2 A_2 A_2$	$C_1 C_2 C_3 C_4$ $A_1 A_1 A_1 A_1$	Jump to ROM address $A_2 A_2 A_2 A_2, A_1 A_1 A_1 A_1$ (within the same ROM that contains this JCN instruction) if condition $C_1 C_2 C_3 C_4$[1] is true, otherwise skip (go to the next instruction in sequence).
*FIM	0 0 1 0 $D_2 D_2 D_2 D_2$	R R R 0 $D_1 D_1 D_1 D_1$	Fetch immediate (direct) from ROM Data D_2, D_1 to index register pair location RRR.[2]
SRC	0 0 1 0	R R R 1	Send register control. Send the address (contents of index register pair RRR) to ROM and RAM at X_2 and X_3 time in the Instruction Cycle.
FIN	0 0 1 1	R R R 0	Fetch indirect from ROM. Send contents of index register pair location 0 out as an address. Data fetched is placed into register pair location RRR.
JIN	0 0 1 1	R R R 1	Jump indirect. Send contents of register pair RRR out as an address at A_1 and A_2 time in the Instruction Cycle.
*JUN	0 1 0 0 $A_2 A_2 A_2 A_2$	$A_3 A_3 A_3 A_3$ $A_1 A_1 A_1 A_1$	Jump unconditional to ROM address A_3, A_2, A_1.
*JMS	0 1 0 1 $A_2 A_2 A_2 A_2$	$A_3 A_3 A_3 A_3$ $A_1 A_1 A_1 A_1$	Jump to subroutine ROM address A_3, A_2, A_1, save old address. (Up 1 level in stack.)
INC	0 1 1 0	R R R R	Increment contents of register RRRR. [3]
*ISZ	0 1 1 1 $A_2 A_2 A_2 A_2$	R R R R $A_1 A_1 A_1 A_1$	Increment contents of register RRRR. Go to ROM address A_2, A_1 (within the same ROM that contains this ISZ instruction) if result ≠ 0, otherwise skip (go to the next instruction in sequence).
ADD	1 0 0 0	R R R R	Add contents of register RRRR to accumulator with carry.
SUB	1 0 0 1	R R R R	Subtract contents of register RRRR to accumulator with borrow.
LD	1 0 1 0	R R R R	Load contents of register RRRR to accumulator.
XCH	1 0 1 1	R R R R	Exchange contents of index register RRRR and accumulator.
BBL	1 1 0 0	D D D D	Branch back (down 1 level in stack) and load data DDDD to accumulator.
LDM	1 1 0 1	D D D D	Load data DDDD to accumulator.

INPUT/OUTPUT AND RAM INSTRUCTIONS

(The RAM's and ROM's operated on in the I/O and RAM instructions have been previously selected by the last SRC instruction executed.)

WRM	1 1 1 0	0 0 0 0	Write the contents of the accumulator into the previously selected RAM main memory character.
WMP	1 1 1 0	0 0 0 1	Write the contents of the accumulator into the previously selected RAM output port. (Output Lines)
WRR	1 1 1 0	0 0 1 0	Write the contents of the accumulator into the previously selected ROM output port. (I/O Lines)
WPM	1 1 1 0	0 0 1 1	Write the contents of the accumulator into the previously selected half byte of read/write program memory (for use with 4008/4009 only)
WRϕ[4]	1 1 1 0	0 1 0 0	Write the contents of the accumulator into the previously selected RAM status character 0.
WR1[4]	1 1 1 0	0 1 0 1	Write the contents of the accumulator into the previously selected RAM status character 1.
WR2[4]	1 1 1 0	0 1 1 0	Write the contents of the accumulator into the previously selected RAM status character 2.
WR3[4]	1 1 1 0	0 1 1 1	Write the contents of the accumulator into the previously selected RAM status character 3.
SBM	1 1 1 0	1 0 0 0	Subtract the previously selected RAM main memory character from accumulator with borrow.
RDM	1 1 1 0	1 0 0 1	Read the previously selected RAM main memory character into the accumulator.
RDR	1 1 1 0	1 0 1 0	Read the contents of the previously selected ROM input port into the accumulator. (I/O Lines)
ADM	1 1 1 0	1 0 1 1	Add the previously selected RAM main memory character to accumulator with carry.
RDϕ[4]	1 1 1 0	1 1 0 0	Read the previously selected RAM status character 0 into accumulator.
RD1[4]	1 1 1 0	1 1 0 1	Read the previously selected RAM status character 1 into accumulator.
RD2[4]	1 1 1 0	1 1 1 0	Read the previously selected RAM status character 2 into accumulator.
RD3[4]	1 1 1 0	1 1 1 1	Read the previously selected RAM status character 3 into accumulator.

ACCUMULATOR GROUP INSTRUCTIONS

CLB	1 1 1 1	0 0 0 0	Clear both. (Accumulator and carry)
CLC	1 1 1 1	0 0 0 1	Clear carry.
IAC	1 1 1 1	0 0 1 0	Increment accumulator.
CMC	1 1 1 1	0 0 1 1	Complement carry.
CMA	1 1 1 1	0 1 0 0	Complement accumulator.
RAL	1 1 1 1	0 1 0 1	Rotate left. (Accumulator and carry)
RAR	1 1 1 1	0 1 1 0	Rotate right. (Accumulator and carry)
TCC	1 1 1 1	0 1 1 1	Transmit carry to accumulator and clear carry.
DAC	1 1 1 1	1 0 0 0	Decrement accumulator.
TCS	1 1 1 1	1 0 0 1	Transfer carry subtract and clear carry.
STC	1 1 1 1	1 0 1 0	Set carry.
DAA	1 1 1 1	1 0 1 1	Decimal adjust accumulator.
KBP	1 1 1 1	1 1 0 0	Keyboard process. Converts the contents of the accumulator from a one out of four code to a binary code.
DCL	1 1 1 1	1 1 0 1	Designate command line.

NOTES: [1]The condition code is assigned as follows:

C_1 = 1 Invert jump condition C_2 = 1 Jump if accumulator is zero C_4 = 1 Jump if test signal is a 0

C_1 = 0 Not invert jump condition C_3 = 1 Jump if carry/link is a 1

[2]RRR is the address of 1 of 8 index register pairs in the CPU.

[3]RRRR is the address of 1 of 16 index registers in the CPU.

[4]Each RAM chip has 4 registers, each with twenty 4-bit characters subdivided into 16 main memory characters and 4 status characters. Chip number, RAM register and main memory character are addressed by an SRC instruction. For the selected chip and register, however, status character locations are selected by the instruction code (OPA).

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PL/M is an Efficient Language Tests on sample programs indicate that a PL/M program can be written in less than 10% of the time it takes to write the same program in assembly language without reducing efficiency. The main reason for this savings in time is the fact that PL/M allows the programmer to define his problem in terms natural to him, not in the computer's terms. Consider the following sample program which selects the largest of two numbers. In PL/M, the programmer might write:
If A>B, then C = A; else C = B;

Meaning

"If Variable A is greater than Variable B, then assign A to Variable C; otherwise, assign B to C."

A corresponding program in assembly language is twelve separate machine instructions, and conveys little of original intent of the program.

Features of the PL/M Language The systems programmer has at his disposal a language that is specifically oriented to systems design, yet is easy to learn and written in a terminology with which he is already familiar. Because of the ease and conciseness with which programs can be written and the error free translation into machine language achieved by the compiler, the time to program a given system is reduced substantially over assembly language.

Debug and checkout time of a PL/M program is also much less than that of an assembly language program, partly because of the inherent clarity of PL/M, but also because writing a program in PL/M encourages good programming techniques. Furthermore, the structure of the PL/M language enables the PL/M compiler to detect error conditions that would slip by any assembler. The PL/M compiler is written in ANSI Fortran IV and thus will execute on most machines with little alteration.

Intellec 8, Eight-bit Microcomputer Development System.

intel delivers.

Intel Microcomputer Systems Group

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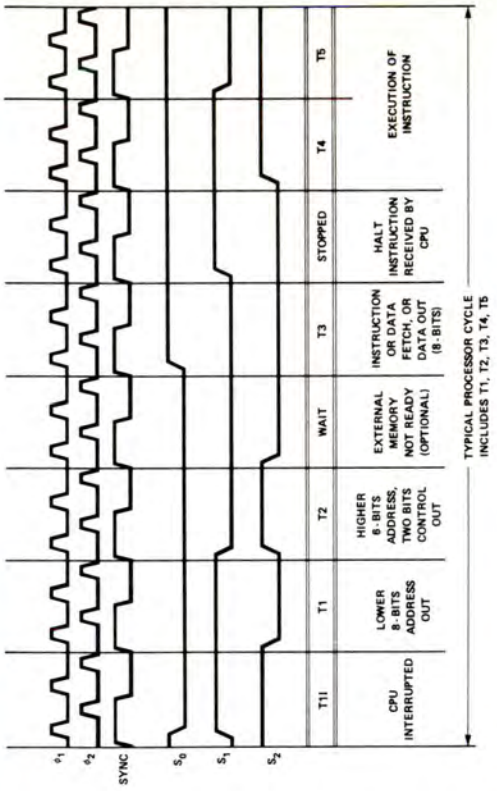
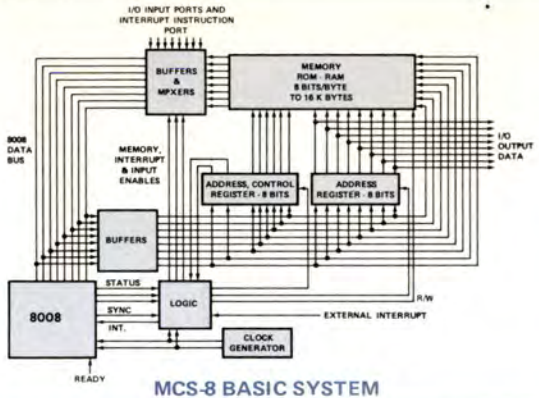
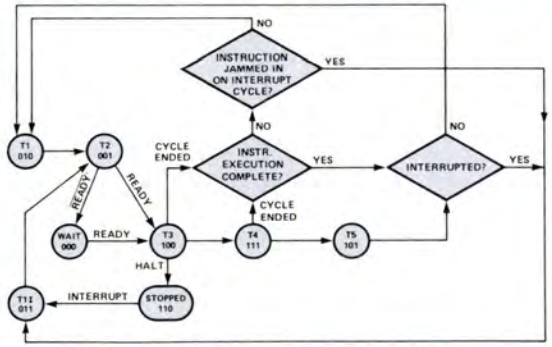


MCS-8 BASIC INSTRUCTION CYCLE



MCS-8 BASIC SYSTEM



CPU STATE TRANSITION DIAGRAM

CYCLE CONTROL CODING

D_6	D_7	CYCLE	FUNCTION
0	0	PCI	Designates the address is for a memory read (first byte of instruction)
0	1	PCR	Designates the address is for a memory read (additional bytes of instruction or data)
1	0	PCC	Designates the data as a command I/O operation
1	1	PCW	Designates the address is for a memory write data

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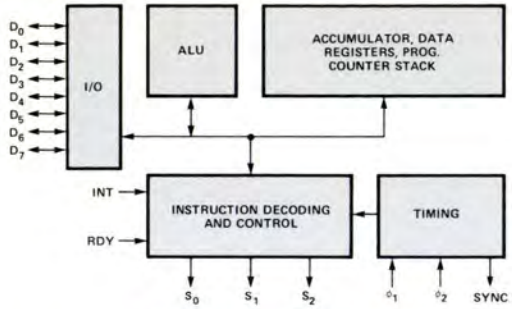
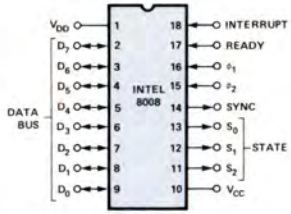
MCS-8™

MICRO COMPUTER SET



8008 BLOCK DIAGRAM



8008 PIN CONFIGURATION

intel®
3065 Bowers Ave., Santa Clara, Ca., 95051
Phone: (408) 246-7501

MCS-8™ Instruction Set

INDEX REGISTER INSTRUCTIONS

The load instructions do not affect the flag flip-flops. The increment and decrement instructions affect all flip-flops except the carry.

MNEMONIC	MINIMUM STATES REQUIRED	INSTRUCTION CODE $D_7 D_6$	$D_5 D_4 D_3$	$D_2 D_1 D_0$	DESCRIPTION OF OPERATION
(1) Lr_1r_2	(5)	1 1	D D D	S S S	Load index register r_1 with the content of index register r_2.
(2) LrM	(8)	1 1	D D D	1 1 1	Load index register r with the content of memory register M.
LMr	(7)	1 1	1 1 1	S S S	Load memory register M with the content of index register r.
(3) Lrl	(8)	0 0 B B	D D D B B B	1 1 0 B B B	Load index register r with data B . . . B.
LMI	(9)	0 0 B B	1 1 1 B B B	1 1 0 B B B	Load memory register M with data B . . . B.
INr	(5)	0 0	D D D	0 0 0	Increment the content of index register r (r ≠ A).
DCr	(5)	0 0	D D D	0 0 1	Decrement the content of index register r (r ≠ A).

ACCUMULATOR GROUP INSTRUCTIONS

The result of the ALU instructions affect all of the flag flip-flops. The rotate instructions affect only the carry flip-flop.

ADr	(5)	1 0	0 0 0	S S S	Add the content of index register r, memory register M, or data B . . . B to the accumulator. An overflow (carry) sets the carry flip-flop.
ADM	(8)	1 0	0 0 0	1 1 1	
ADI	(8)	0 0 B B	0 0 0 B B B	1 0 0 B B B	
ACr	(5)	1 0	0 0 1	S S S	Add the content of index register r, memory register M, or data B . . . B to the accumulator with carry. An overflow (carry) sets the carry flip-flop.
ACM	(8)	1 0	0 0 1	1 1 1	
ACI	(8)	0 0 B B	0 0 1 B B B	1 0 0 B B B	
SUr	(5)	1 0	0 1 0	S S S	Subtract the content of index register r, memory register M, or data B . . . B from the accumulator. An underflow (borrow) sets the carry flip-flop.
SUM	(8)	1 0	0 1 0	1 1 1	
SUI	(8)	0 0 B B	0 1 0 B B B	1 0 0 B B B	
SBr	(5)	1 0	0 1 1	S S S	Subtract the content of index register r, memory register M, or data B . . . B from the accumulator with borrow. An underflow (borrow) sets the carry flip-flop.
SBM	(8)	1 0	0 1 1	1 1 1	
SBI	(8)	0 0 B B	0 1 1 B B B	1 0 0 B B B	
NDr	(5)	1 0	1 0 0	S S S	Compute the logical AND of the content of index register r, memory register M, or data B . . . B with the accumulator.
NDM	(8)	1 0	1 0 0	1 1 1	
NDI	(8)	0 0 B B	1 0 0 B B B	1 0 0 B B B	
XRr	(5)	1 0	1 0 1	S S S	Compute the EXCLUSIVE OR of the content of index register r, memory register M, or data B . . . B with the accumulator.
XRM	(8)	1 0	1 0 1	1 1 1	
XRI	(8)	0 0 B B	1 0 1 B B B	1 0 0 B B B	
ORr	(5)	1 0	1 1 0	S S S	Compute the INCLUSIVE OR of the content of index register r, memory register m, or data B . . . B with the accumulator.
ORM	(8)	1 0	1 1 0	1 1 1	
ORI	(8)	0 0 B B	1 1 0 B B B	1 0 0 B B B	
CPr	(5)	1 0	1 1 1	S S S	Compare the content of index register r, memory register M, or data B . . . B with the accumulator. The content of the accumulator is unchanged.
CPM	(8)	1 0	1 1 1	1 1 1	
CPI	(8)	0 0 B B	1 1 1 B B B	1 0 0 B B B	
RLC	(5)	0 0	0 0 0	0 1 0	Rotate the content of the accumulator left.
RRC	(5)	0 0	0 0 1	0 1 0	Rotate the content of the accumulator right.
RAL	(5)	0 0	0 1 0	0 1 0	Rotate the content of the accumulator left through the carry.
RAR	(5)	0 0	0 1 1	0 1 0	Rotate the content of the accumulator right through the carry.

PROGRAM COUNTER AND STACK CONTROL INSTRUCTIONS

(4) JMP	(11)	0 1 B_2 B_2 X X	X X X B_2 B_2 B_2 B_3 B_3 B_3	1 0 0 B_2 B_2 B_2 B_3 B_3 B_3	Unconditionally jump to memory address $B_3 \ldots B_3B_2 \ldots B_2$.
(5) JFc	(9 or 11)	0 1 B_2 B_2 X X	0 C_4 C_3 B_2 B_2 B_2 B_3 B_3 B_3	0 0 0 B_2 B_2 B_2 B_3 B_3 B_3	Jump to memory address $B_3 \ldots B_3B_2 \ldots B_2$ if the condition flip-flop c is false. Otherwise, execute the next instruction in sequence.
JTc	(9 or 11)	0 1 B_2 B_2 X X	1 C_4 C_3 B_2 B_2 B_2 B_3 B_3 B_3	0 0 0 B_2 B_2 B_2 B_3 B_3 B_3	Jump to memory address $B_3 \ldots B_3B_2 \ldots B_2$ if the condition flip-flop c is true. Otherwise, execute the next instruction in sequence.
CAL	(11)	0 1 B_2 B_2 X X	X X X B_2 B_2 B_2 B_3 B_3 B_3	1 1 0 B_2 B_2 B_2 B_3 B_3 B_3	Unconditionally call the subroutine at memory address $B_3 \ldots B_3B_2 \ldots B_2$. Save the current address (up one level in the stack).
CFc	(9 or 11)	0 1 B_2 B_2 X X	0 C_4 C_3 B_2 B_2 B_2 B_3 B_3 B_3	0 1 0 B_2 B_2 B_2 B_3 B_3 B_3	Call the subroutine at memory address $B_3 \ldots B_3B_2 \ldots B_2$ if the condition flip-flop c is false, and save the current address (up one level in the stack.) Otherwise, execute the next instruction in sequence.
CTc	(9 or 11)	0 1 B_2 B_2 X X	1 C_4 C_3 B_2 B_2 B_2 B_3 B_3 B_3	0 1 0 B_2 B_2 B_2 B_3 B_3 B_3	Call the subroutine at memory address $B_3 \ldots B_3B_2 \ldots B_2$ if the condition flip-flop c is true, and save the current address (up one level in the stack). Otherwise, execute the next instruction in sequence.
RET	(5)	0 0	X X X	1 1 1	Unconditionally return (down one level in the stack).
RFc	(3 or 5)	0 0	0 C_4 C_3	0 1 1	Return (down one level in the stack) if the condition flip-flop c is false. Otherwise, execute the next instruction in sequence.
RTc	(3 or 5)	0 0	1 C_4 C_3	0 1 1	Return (down one level in the stack) if the condition flip-flop c is true. Otherwise, execute the next instruction in sequence.
RST	(5)	0 0	A A A	1 0 1	Call the subroutine at memory address AAA000 (up one level in the stack).

INPUT/OUTPUT INSTRUCTIONS

INP	(8)	0 1	0 0 M	M M 1	Read the content of the selected input port (MMM) into the accumulator.
OUT	(6)	0 1	R R M	M M 1	Write the content of the accumulator into the selected output port (RRMMM, RR ≠ 00).

MACHINE INSTRUCTION

HLT	(4)	0 0	0 0 0	0 0 X	Enter the STOPPED state and remain there until interrupted.
HLT	(4)	1 1	1 1 1	1 1 1	Enter the STOPPED state and remain there until interrupted.

NOTES:

(1) SSS = Source Index Register, DDD = Destination Index Register — These registers, r_i, are designated A(accumulator–000), B(001), C(010), D(011), E(100), H(101), L(110).

(2) Memory registers are addressed by the contents of registers H & L.

(3) Additional bytes of instruction are designated by BBBBBBBB.

(4) X = "Don't Care".

(5) Flag flip-flops are defined by C_4C_3: carry (00-overflow or underflow), zero (01-result is zero), sign (10-MSB of result is "1"), parity (11-parity is even).

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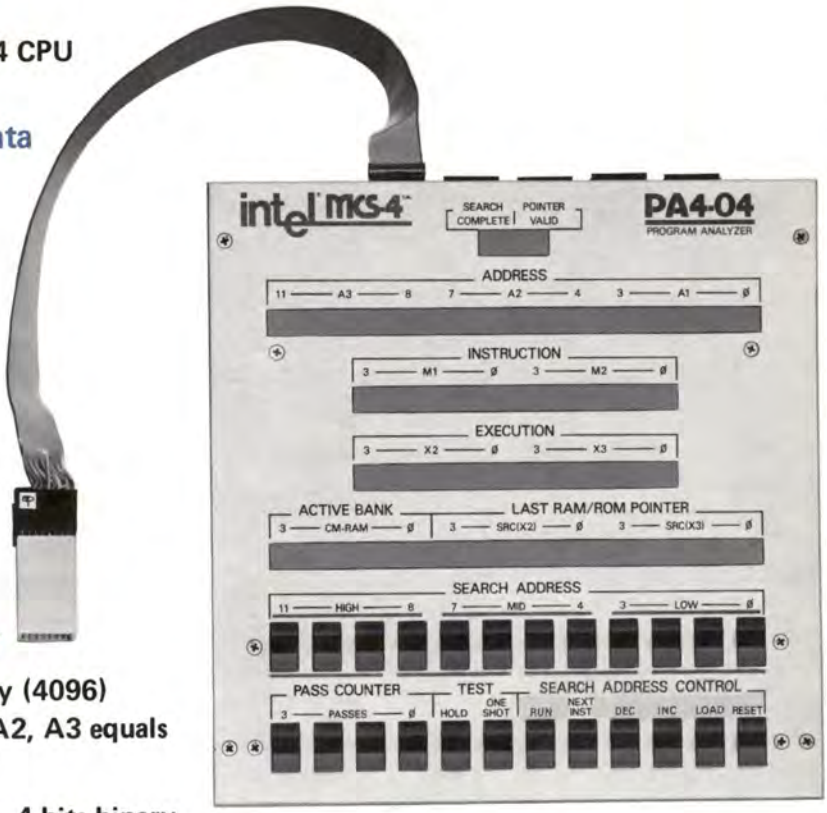
JUNE 1973

PA4-04 PROGRAM ANALYZER FOR MCS™-4 SYSTEM DEVELOPMENT

■ Simple Connection to CPU

16-pin DIP-CLIP attaches to 4004 CPU



■ Latches and Displays All Data

- □ Address: 12 bits binary (A1, A2, A3)
- □ Instruction: 8 bits binary (M1, M2)
- □ Execution: 8 bits binary (X2, X3)
- □ Bank Select: 4 bits binary (CM-RAM 0-3)
- □ RAM/ROM Pointer: 8 bits binary (SRC-X2,-X3)

■ Full Program Addressability

- □ Search Address: 12 bits binary (4096) Displays CPU data when A1, A2, A3 equals preset search address.
- □ Program Loop Addressability: 4 bits binary Displays CPU data when the preselected search address has been accessed 1 to 15 times. The number of passes is determined by the pass counter setting.
- □ Next Instruction Addressability: Displays CPU data of next instruction executed after the preselected search address. Facilitates altered-sequence program debugging (JUN, JIN, ISZ, JMS, JCN, BBL).
- □ Increment or Decrement Address: Displays CPU data at the preselected search address incremented or decremented by one.

■ Status Indicators

- □ Search Complete: Indicates that data now displayed is from selected addresses and passes.
- □ Pointer Valid: Indicates that an SRC has been issued.

■ Control Switches

- □ Reset: Sets CPU program counter to location zero and initializes program analyzer.
- □ Test One Shot: Asserts (sets to active state) CPU test line for two instruction cycles.
- □ Test Hold: Holds asserted CPU test line indefinitely. This is used with a JUMP or TEST instruction to cause a pseudo halt of the processor.
- □ Load: Enters search address and number of passes into the program analyzer and initiates search sequence.
- □ Run: Provides sync pulse at search address for hardware debugging. A terminal is provided on the back panel for easy access to the sync signal.

PA4-04 Program Analyzer

The PA4-04 Program Analyzer is a compact (9"x 9" x 1.5") portable unit providing a powerful real-time analysis capability for MCS-4 users. The PA4-04 was designed as an MCS-4 development tool and for convenient field service of microcomputer systems. It can be used with all SIM4 prototyping kits. Its applications are:

- **MCS-4 Software Debugging**
- **MCS-4 System Debugging**
- **CPU Data Logger**
- **Program Event Detector**
- **Address Comparator**
- **Binary Display Unit**
- **Troubleshooting in the Field**

The analyzer connects to the 4004 CPU via a 16-pin DIP-CLIP and displays all of the significant CPU parameters. In the free running mode, a 12-bit address display provides a continuous indication of the program counter value and a sync pulse at a selected location. In the search mode, the following parameters are latched and displayed as the CPU accesses a preselected search address: ADDRESS, INSTRUCTION, EXECUTION DATA, ACTIVE BANK, and LAST RAM/ROM POINTER.

A switch selectable pass counter provides interrogation of program loops by delaying the display until after a preset number of passes (1 to 15) have been made through the preset SEARCH ADDRESS.

SEARCH CONTROL and TEST switches provide additional features for easy program debugging.

All displayed parameters are also accessable in buffered TTL form via external 16-pin DIP sockets on the back panel. This allows for external monitoring needed for data logging applications.

The PA4-04 requires a single external power supply (+5VDC, 2.0A) which is connected to banana plugs provided on the back panel.

Operating Procedures

1. Connect 5 volt power supply to analyzer via banana plug connectors. (Connect ground to MCS-4 system common as well.)

2. Connect analyzer to 4004 CPU via DIP-CLIP connector.

3. Set "SEARCH ADDRESS" switches to desired program address.

4. Set "PASS CNTR" switches to desired number of passes.

5. Push "LOAD" (push "RESET" also if execution from location zero desired as well).

6. The "SEARCH COMPLETE" indicator will light when the CPU executes the preset number of passes of the search address or after execution of the next instruction after the search address/pass count ("NEXT-INST" switch on). All CPU data displays will latch-up at "SEARCH COMPLETE" time.

7. The "POINTER VALID" indicator will light when the CPU executes an SRC instruction. The "LAST RAM/ROM POINTER" will display the last SRC executed before "SEARCH COMPLETE" time.

8. Further program analysis can be made by performing any one of the following:
   a. Push "INC" to increment search address by one location. (Push "RESET" switch also if execution from location zero desired as well.)
   b. Push "DEC" to decrement search address by one location. (Push "RESET" switch also if execution from location zero desired as well.)
   c. Set "SEARCH ADDRESS" and/or "PASS CNTR" switches to desired new setting. Push "LOAD" (push "RESET" also if execution from location zero desired as well).
   d. Push "NEXT-INST" switch and perform any one of the above operations for analysis of altered-sequence program flow (JUN, JIN, ISZ, JMS, JCN, BBL).

9. Miscellaneous operations:
   a. Push "TEST ONE SHOT" switch to assert CPU test line for 2 instruction cycles.
   b. Push "TEST HOLD" switch to assert CPU test line indefinitely.
   c. Push "RUN" switch to provide a sync pulse at the preset search address. (CPU data display does not latch-up in this mode. In this mode the "PASS CNTR" switches must be set to zero.)

Ordering Information

Product Code:	PA4-04
Price:	$495.00

Printed in U.S.A.

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INTEL CORPORATION 3065 Bowers Avenue, Santa Clara, California 95051 • (408) 246-7501

MCS™-4 4-bit Microcomputer Set

COMPONENTS

Product	Product Description	Quantity 1-24	Quantity 25-99	Quantity 100-999
P4001[1,2]	2048 Bit Mask Programmable ROM	$ NA	$ NA	$ 15.00
P4002-1	320 Bit RAM (Metal Option No. 1)	30.00	21.00	15.00
P4002-2	320 Bit RAM (Metal Option No. 2)	30.00	21.00	15.00
P4003	10 Bit Shift Register	6.00	4.20	3.00
C4004	Central Processor Unit	60.00	42.00	30.00
P4008	Address Latching Unit	30.00	21.00	15.00
P4009	I/O Control Unit	30.00	21.00	15.00
C1702A/S314 [9] Unprogrammed (Quartz lid)	Erasable and Electrically Reprogrammable 2048 Bit ROM (Static only)	60.00	48.00	40.00 ↓

PROTOTYPE KIT

• MICRO COMPUTER SYSTEM – 4k INSTRUCTION CAPACITY

Product	Product Description	Price
* SIM4-03 [3]	MCS-4/1702A microcomputer card (max. capacity 16 ROMs, 16 RAMs)	$625.00
MP7-03 [4]	1702A Programmer Card (Completely stuffed)	400.00
MCB4-20 [5]	MCS Interface and Control Module for SIM4-03/MP7-03	450.00

• PROM CONTROL PROGRAMS REQUIRED FOR PROTOTYPING WITH SIM4-03

Product	Product Description	Price
C1702A/A0540 [6] C1702A/A0541 [6] C1702A/A0543 [6]	Control ROMs for the MCS-4 PROM Programming System. (These devices must be ordered as a set.)	$210.00 ↓
C1702A/A0544	Control ROM for PROM duplicating	70.00 ↓
C1702A/740 Set [7]	SIM4 Hardware Assembler (These 4 devices must be ordered as a set. See note for price.)	280.00 ↓
C1702A/750 Set [8]	MCS-4 Hardware Simulator (These 9 devices must be ordered as a set. See note for price.)	630.00 ↓

• SYSTEM AND PROGRAM DEBUG MODULE

Product	Product Description	Price
* PA4-04	Program Analyzer	$495.00

SUPPORT SOFTWARE

Program	Price
MCS-4 Assembler written in FORTRAN IV [10]	$1250.00
MCS-4 Simulator written in FORTRAN IV [10]	750.00

(Also available via timesharing through Applied Logic Corporation, General Electric Company, and Tymshare, Inc.)

DENOTES NEW INTEL PRODUCT

MICROCOMPUTER NOTES

1. Minimum order for the 4001 and 1302 is 100 units per pattern. Minimum order for 8416 is 500 units per pattern.
2. These prices exclude mask charges. Mask charges for the 4001 and 1302 are $600.00 (including three units). Mask charge for 8416 is $1100 (including three units).
3. The price of the SIM4-03 card is for a fully stuffed card (containing one 4004, four 4002s, and all interface circuits excluding the electrically programmable ROMs).
4. The MP7-03 interfaces directly with the SIM4-03 and SIM8-01 cards.
5. The unit price includes LED display, connectors, metal box for mounting, two transformers, and one capacitor. The unit is shipped completely assembled.
6. Only 1702As may be programmed with these PROM control programs. To program the 1702, program A0542 must be substituted for A0543 on the SIM4 systems and program A0862 must be substituted for A0863 on the SIM8 system.

MCS™-8 8-bit Microcomputer Set

COMPONENTS

Product	Product Description	Quantity 1-24	Quantity 25-99	Quantity 100-999
C8008	8 Bit Central Processor (500kHz)	$120.00	$ 84.00	$ 60.00
C8008-1	8 Bit Central Processor (800kHz)	180.00	126.00	90.00
P2102	1024 Bit Fully Decoded Static RAM	35.85	28.70	23.90
C1702A/S714 Unprogrammed [9] (Quartz lid)	Erasable and Electrically Reprogrammable 2048 Bit ROM (Static only)	60.00	48.00	40.00 ↓
P1302 [1,2]	Mask Programmable 2048 Bit Static ROM	NA	NA	16.50
* P8416 [1,2]	Mask Programmable 16,384 Bit Static ROM	NA	NA	48.00

PROTOTYPE KIT

• MICRO COMPUTER SYSTEM – 3k INSTRUCTION CAPACITY

Product	Product Description	Price
SIM8-01 [11]	MCS-8/1702A Prototyping Card (Maximum capacity 2k x 8 ROM, 1k x 8 RAM)	$900.00
MP7-03 [4]	1702A Programmer Card (Completely Stuffed)	400.00
MCB8-10 [5]	Micro Computer System Interface and Control Module for SIM8-01/ MP7-03	450.00

• PROM CONTROL PROGRAMS REQUIRED FOR THE SIM8-01

Product	Product Description	Price
C1702A/A0860 [6] C1702A/A0861 [6] C1702A/A0863 [6]	Bootstrap Loader and PROM Programmer Control ROMs for the SIM8-01 Card. (These 3 devices must be ordered as a set.)	$210.00 ↓
C1702A/A0840 Set [12]	SIM8 Hardware Assembler for the SIM8-01. (These 8 devices must be ordered as a set. See note for price.)	560.00 ↓

SUPPORT SOFTWARE

Program	Price
* MCS-8 PL/M Compiler written in FORTRAN IV [10] (July 1973)	$1250.00
MCS-8 Assembler written in FORTRAN IV [10]	1250.00
MCS-8 Simulator written in FORTRAN IV [10]	750.00

(Also available via timesharing through Applied Logic Corporation, General Electric Company, and Tymshare, Inc.)

NOTE: ↓ = PRICE LOWERED

7. The ROM pattern for the SIM4 Hardware Assembler may be ordered in punched paper tape format for $100.00. To order, specify tape numbers A0740, A0741, A0742, and A0743.
8. The complete set of ROM patterns for the SIM4 Hardware Simulator may be ordered in punched paper tape format for $200.00. To order, specify tape number A0750 through A0758.
9. PROGRAMMING: If the customer provides a tape in the proper format, there will be additional charge of $10.00 per unit for programming. If the program is provided as a truth table only, a one time set up charge of $90.00 per pattern will be made for converting to tape, in addition to the $10.00 charge per unit for programming.
10. The purchase price of these software programs is refundable at the rate of 10% of additional MCS purchases up to the total price of the software purchased. These programs are also available through three national computer timesharing services: Applied Logic Corporation, General Electric Company, and Tymshare, Inc. Contact your local timesharing representative for information.
11. The price for the SIM8-01 is for a fully stuffed card (containing 1k x 8 RAM and all interface circuits) excluding the electrically programmable ROMs.
12. The additional program tapes A0848, A0849, A0850, are included with the SIM8 Hardware Assembler. The complete set of ROM patterns for the SIM8 Hardware Assembler may be ordered in punched paper tape format for $200.00. To order, specify tape numbers A0840 through A0850.

MCS™-4 Modular Microcomputer Development Systems

* MICROCOMPUTER MODULES

(Sept. 1973)

Product	Standard Modules	Price[15]
imm4-42	**Central Processor** – Includes CPU, four 4002s, sockets for four PROMs, I/O Ports and Crystal Clock	$395.00
imm4-22	**Instruction/Data Storage** – Includes four 4002s, sockets for four PROMs, and I/O Ports	295.00
imm4-24	**Data Storage**[13] – Includes four 4002s and capacity for twelve additional 4002s	195.00
imm6-26	**PROM Memory** – Includes sockets for sixteen 1702A PROMs	125.00
imm4-72	**Control** – Interfaces Central Processor to RAM Memory for Instruction Storage and contains timing circuitry for reset and test lines	95.00
imm6-28	**RAM Memory**[14] – 4k x 8 Static Memory	795.00
imm4-60	**Input/Output** – 8 Input and 8 Output ports	150.00
imm4-44	**OEM System Module** – Includes CPU, Crystal Clock, four 4002s and combined capacity for up to sixteen 4001s and 4002s	Quantity[15] 100-up $263.00

Product	Accessory Modules	Price[15]
imm4-76	1702A PROM Programmer and Control Software	$350.00
imm6-70	Universal Prototype Module	40.00
imm6-72	Module Extender	35.00

* intellec™ 4[16]

(Oct. 1973)

Product	Description	Price[15]
imm4-40	**Complete Table Top Development System**	$2195.00
	Standard Modules (Included in price)	
	Central Processor Module Control Module RAM Memory Module Complete with: Chassis; Power Supplies; Control and Display Panel; Finished Cabinet; Standard Software – system monitor, resident assembler.	
	Optional	
	Individual Microcomputer Modules and Accessory Modules – prices are as shown above.	
imm6-34	Drawer Slides and Extenders for rack mounting	40.00

* BARE BONES 4[16]

(Oct. 1973)

Product	Description	Price[15]
imm4-41	**Complete Rack Mountable System.** Same as intellec 4 except excludes control panel, power supplies, and cabinet	$1540.00

SUPPORT SOFTWARE

Program	Price[15]
MCS-4 Assembler written in FORTRAN IV[10]	$1250.00
MCS-4 Simulator written in FORTRAN IV[10]	750.00

(Also available via timesharing through Applied Logic Corporation, General Electric Company, and Tymshare, Inc.)

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MICROCOMPUTER NOTES (con't.)

13. Modules containing 8, 12, or 16 4002s are available on request. Minimum order – 25 modules.
14. Memory configurations of 1k, 2k, and 3k bytes are available on request.
15. For higher quantity pricing, contact your local Intel Representative.
16. Not available through distributors.

MCS™-8 Modular Microcomputer Development Systems

* MICROCOMPUTER MODULES

(Sept. 1973)

Product	Standard Modules	Price[15]
imm8-82	**Central Processor** – Includes 8008-1 CPU Crystal Clock and Interface Logic	$450.00
imm6-26	**PROM Memory** – Includes sockets for sixteen 1702A PROMs	125.00
imm6-28	**RAM Memory**[14] – 4k x 8 Static Memory	795.00
imm8-60	**Input/Output** – 4 Input and 4 Output Ports	175.00
imm8-62	**Output** – 8 Latching Output Ports	125.00

Product	Accessory Modules	Price[15]
imm8-76	1702A PROM Programmer and Control Software	$350.00
imm6-70	Universal Prototype Module	40.00
imm6-72	Module Extender	35.00

* intellec™ 8[16]

(Oct. 1973)

Product	Description	Price[15]
imm8-80	**Complete Table Top Development System**	$2395.00
	Standard Modules (Included in Price)	
	Central Processor Module Input/Output Module PROM Memory Module RAM Memory Module Complete with: Chassis; Power Supplies: Control and Display Panel; Finished Cabinet; Standard Software – system monitor, resident assembler, text editor.	
	Optional	
	Individual Microcomputer Modules and Accessory Modules – prices are as shown above	
imm6-34	Drawer Slides and Extenders for rack mounting	40.00

* BARE BONES 8[16]

(Oct. 1973)

Product	Description	Price[15]
imm8-81	**Complete Rack Mountable System.** Same as intellec 8 except excludes control panel, power supplies, and cabinet	$1750.00

SUPPORT SOFTWARE

Program	Price[15]
* MCS-8 PL/M Compiler written in FORTRAN IV[10] (July 1973)	$1250.00
MCS-8 Assembler written in FORTRAN IV[10]	1250.00
MCS-8 Simulator written in FORTRAN IV[10]	750.00

(Also available via timesharing through Applied Logic Corporation, General Electric Company, and Tymshare, Inc.)

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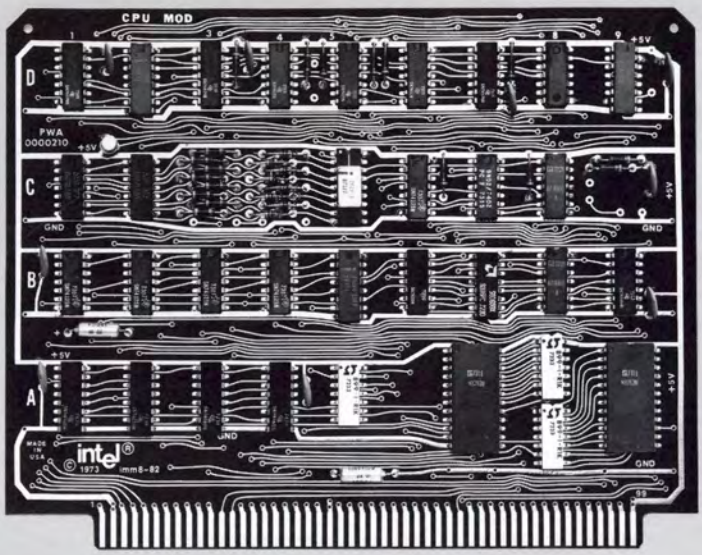
617/861-1136 ▪ Telex: 92-3493

800 Southgate Office Plaza, 5001 W. 78th St.,
Bloomington, Minnesota 55437 ▪ 612/835-6722

intellec 8

MODULE DESCRIPTIONS



Modules may be ordered individually. All modules are 8" wide, 6.28" high and use standard 100-pin connectors.

imm8-82 **Central Processor Module**

- Intel's 8008-1 eight-bit parallel single chip CPU—p-channel silicon gate MOS.
- Accumulator and six 8-bit working registers.
- Subroutine nesting up to seven levels.
- Interface to 16K 8-bit bytes of PROM, ROM, or RAM via the PROM Memory Module and RAM Memory Module.
- Interface for expansion to eight 8-bit input ports and twenty-four 8-bit output ports, via the I/O and Output Modules.
- Interrupt capability.
- Two phase crystal clock.
- All module interfaces are TTL compatible.

imm6-26 **PROM Memory Module**

- Provides sockets for up to sixteen 1702A electrically programmable and erasable PROMs for a system's fixed program memory (maximum 4K bytes/module).
- For volume requirements, Intel mask programmed 1302 ROMS may be substituted in the same module.

imm6-28 **RAM Memory Module**

- A 4K x 8 n-channel MOS memory system using Intel's 1024 bit static RAM (2102).
- Address latching, data latching, and module select decoding are provided on the card.
- Provides both program storage and data storage.

imm8-60 **Input/Output Module**

- Four 8-bit input ports (32 lines).
- Four 8-bit data latching output ports (32 lines).
- Asynchronous transmitter/receiver is associated with one pair of ports for TTY communication.
- All input and output ports are TTL compatible.

imm8-62 **Output Module**

- Eight 8-bit data latching output ports (64 lines).
- All output ports are TTL compatible.

imm8-74 **Control and Display Panel**

- Provides complete operator control for Intellec 8 and displays system status.
  Address and Data Entry switches.
  Status, instruction code, data and address displays.
- Complete program development tool.
  ADDRESS, PROGRAM SEQUENCE, and MODE CONTROL switches permit easy alteration and examination of the program during the debugging phase of program development.
- Control and socket for 1702A PROM programming is also provided.

imm6-70 **Universal Prototype Module**

- Accommodates 14, 16, 24, or 40 pin wire wrap sockets (maximum of 52 16-pin sockets).
- Provides breadboard capability for developing custom and specialized interface circuits.

imm6-72 **Module Extender**

- Extends Intellec modules out of card chassis for ease in test and system debugging.

imm8-76 **PROM Programmer Module**

- Provides all timing and level shifting circuitry for programming Intel's electrically programmable and erasable 1702A PROMs.
- This programmer is controlled by special system software that is supplied with the module.

Chassis Module (Used in the Intellec 8 and Bare Bones 8)

- Capacity for up to sixteen microcomputer modules. (16 sockets with standard system.)
- PC Mother Board eliminates back plane wiring—all cards plug into common bus.
- Standard 100 pin connectors (125 Mil centers) are used for all boards in system.
- Space is provided for additional memory and I/O modules and unique customer developed system interface modules.
- A fan is provided.

intellec™ 4

Features

- Ideal for prototyping MCS 4 Systems.
- The Intellec 4 is a complete microcomputer system with 5K bytes of program memory, data storage, I/O, TTY interface, standard software, control panel, power supplies, and a compact finished cabinet (less than 0.8 ft.^{3}). Bare Bones 4 is a rack-mountable unit and comes without the power supplies, front panel and finished cabinet accessories.
- The heart of the Intellec system is Intel's four-bit "computer on a chip," the 4004. This is a 4-bit parallel CPU with a repertoire of 45 instructions, sixteen working registers, a four level address stack, and capability of directly addressing over 43K bits of memory.
- DMA Channel is standard.
- Standard software provided with the Intellec 4 includes a system monitor which provides a loader, hex memory dump, and instruction editing, and an assembler which is loaded to RAM program memory.
- With this system, all program development may be done in RAM memory.
- A complete PROM programmer is provided as an option. After the program is firm, it may be committed to non-volatile storage in Intel's 1702A programmable and erasable Read-Only-Memory.
- Complete system control and hardware debugging aids are provided via the control panel.
- Crystal clocks are provided for system stability.
- System is expandable to 12 microcomputer modules in a single chassis.

Specifications

Word Size:	Data: 4 bits Instruction: 8 or 16 bits
Memory Size:	Instruction Memory: 1K Bytes (8 bits) in PROM switchable to 4K bytes (8 bits) RAM Data Storage: 320 words (4 bit), expandable to 2560 words
Instruction Set:	45, including conditional branching, binary and decimal, arithmetic, register-to-register and I/O
System Clock:	Crystal Controlled
Machine Cycle Time:	10.8 μs
Direct Memory Access:	DMA Standard
Memory Cycle Time:	900 nanoseconds
I/O Channels:	4 input ports, 8 output ports, expandable to 16 input ports, 48 output ports
Operating Temperature:	0°C to 55°C
Power Supplies:	+5v ±5% 8 amps* −10v ±5% 1.8 amps* **required for maximum system*
Physical Size:	Intellec 4: 7" x 17⅛" x 12¼" (table top only) Bare Bones 4: 6¾" x 17" x 12" suitable for mounting in standard RETMA 7" x 19" panel space
Weight:	30 lb.
Standard Software:	System Monitor Resident Assembler
Support Software:	Cross Assembler, Simulator } written in FORTRAN IV

Standard Systems and Optional Modules

INTELLEC 4 (imm4-40) Standard System includes the following Modules and Accessories:

- Central Processor Module
- Control Module
- RAM Memory Module
- Chassis with Mother Board
- Power Supplies
- Control and Display Panel
- Finished Cabinet
- Standard Software
  - System Monitor
  - Resident Assembler

BARE BONES 4 (imm4-41) Standard System includes the following Modules:

- Central Processor Module
- Control Module
- RAM Memory Module
- Chassis (rack mountable with Mother Board)
- Standard Software
  - System Monitor
  - Resident Assembler

OPTIONAL MODULES available for the Intellec 4 and Bare Bones 4:

- PROM Programmer Module with Control Software
- Instruction/Data Storage Module
- Input/Output Module
- Data Storage Module
- ROM Memory Module
- Universal Prototype Module
- Module Extender
- Drawer Slides and extenders for Rack Mounting

Software

Standard All peripheral interface to Intellec 4 standard software is via TTY, model ASR33. All control after system start-up is provided through the TTY.

A. System Monitor

1. Contained in four 1702A PROMs located on the Central Processor Module.
2. Intellec 4 modular microcomputer systems have a control program called a Resident Monitor in PROM so that no "bootstrap" operation need ever be performed.

   The monitor functions are as follows:

   a. Load RAM memory from paper tape, either in BNPF format or hexadecimal format.

   b. Display the contents of RAM memory on a printer.

   c. Modify individual bytes of RAM memory, move blocks of RAM memory, fill blocks of RAM memory with constant data.

   d. Write contents of RAM memory to paper tape in either BNPF or hexadecimal format.

B. Resident Assembler

1. Translates mnemonic code to binary machine code.
2. Loaded into system RAM Memory via paper tape.
3. Data storage devices (4002 RAM) store label and symbols (eight/RAM).
4. This two pass assembler generates a program tape which is reloaded via the monitor.

Developmental Support: Cross Assembler and Simulator In addition to the standard software provided with the Intellec 4, Intel offers a cross assembler and simulator written in general FORTRAN IV and designed to operate on general purpose computers. The package consists of a simulating routine, which enables the computer to simulate the operation of an MCS-4 microcomputer set and an assembly routine used primarily as an aid to programming the simulated microcomputer.

The routines may be procured directly from Intel, or alternatively, designers may contact three nationwide computer time-sharing services—AL/COM, G.E., and Tymshare—for access to the programs.

The 4004 Central Processor Chip is the heart of each Intellec 4 System.

intellec 4

MODULE DESCRIPTIONS

Modules may be ordered individually. All modules are 8" wide, 6.28" high and use standard 100-pin connectors.

imm4-42 **Central Processor Module**

- This is a complete microcomputer system with the processor, program storage, data storage, and I/O in a single module.
- The heart of this module is Intel's 4004 single chip four-bit parallel processor—p-channel silicon gate MOS.
- Accumulator and sixteen working registers (4 bit).
- Subroutine nesting up to 3 levels.
- For development work, the CPU interfaces to standard semiconductor memory elements (provided by Intel's standard memory and I/O interface set 4008/4009).
- Sockets for 1K bytes of PROM (Intel 1702A PROM) are provided.
- 320 words (4-bit) of data storage (Intel 4002) are provided.
- Four 4-bit input ports and eight 4-bit output ports (includes TTY interface).
- Bus-oriented expansion of memory and I/O.
- Two phase crystal clock.

imm4-22 **Instruction/Data Storage Module**

- This microcomputer module has memory capacity identical to the Central Processor Module and is used for expanding memory and I/O.
- Sockets for 1K bytes of PROM program storage are provided.
- 320 words (4-bit) of data storage are provided.
- Four 4-bit input ports and eight 4-bit output ports.

imm4-24 **Data Storage Module**

- This microcomputer module has capacity for sixteen Intel 4002 RAMS—1280 words (4-bit) of data storage.
- 320 words (4-bit) of data storage are provided.
- A maximum Intellec 4 system may contain up to 2560 words of storage—decoding for this expansion is provided.
- A 4-bit output port is associated with each RAM on this microcomputer module providing sixteen 4-bit output ports on each module.
- All output ports are TTL compatible.

imm4-60 **Input/Output Module**

- This module provides input and output port expansion without additional memory.
- Eight 4-bit input ports and eight 4-bit output ports are provided.
- Ports on this module are TTL compatible.

imm4-72 **Control Module**

- Contains circuitry required to interface the Central Processor to instruction storage on the RAM Memory Module.
- This module also contains debouncing and timing circuitry for RESET and TEST control lines to the CPU.

imm6-26 **PROM Memory Module**

- Provides sockets for up to sixteen 1702A electrically programmable and erasable PROMs for a system's fixed program memory (maximum 4K bytes/module).
- For volume requirements, Intel 2048-bit mask programmed MOS ROMs (1302) may be substituted in the same module.

imm6-28 **RAM Memory Module**

- A 4K x 8 n-channel MOS memory system using Intel's 1024-bit Static RAM (2102).
- Address latching, data latching, and module select decoding are provided on the card.
- Provides program storage for up to 4K instructions.

imm4-44 **OEM System Module**

- For final volume production systems where cost and card count must be minimized.
- Contains 4004 CPU, crystal clock, 320 words of data storage, and provision for a combination of up to sixteen 256 x 8 masked program ROMs (4001) for program storage and 80 x 4 data storage devices (4002 RAMs).
- Instruction and data storage is expandable using the Data Storage Module.

imm6-70 **Universal Prototype Module**

- Accommodates 14, 16, 24, or 40 pin wire wrap sockets (maximum of 52 16-pin sockets).
- Provides breadboard capability for developing custom and specialized interface circuits.

imm6-72 **Module Extender**

- Extends Intellec modules out of card chassis for ease in test and system debugging.

imm4-74 **Control and Display Panel**

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  Status, instruction code, data and address displays.
- Complete program development tool.
  ADDRESS, PROGRAM SEQUENCE, and MODE CONTROL switches permit easy examination of the program during the debugging phase of program development.
- Control and socket for 1702A PROM programming is also provided.

imm4-76 **PROM Programmer Module**

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- This programmer is controlled by special system software supplied with module.

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- A fan is provided.

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