X6818.2013

Data General Corporation

3 NEW COMPUTERS FROM DATA GENERAL NOVA 1200, NOVA 800, SUPERNOVA SC.


FETCH
DEFER
EXECUTE
NOVA 1200
RUN
ION
FETCH
DEFER
NOVA 800

THE FAST NEW NOVAS.

Announcing three very fast, very economical new computers from Data General Corporation: Nova 1200, Nova 800, and Supernova SC.

Nova 1200 is the least expensive 16-bit, multi-accumulator small computer available. It combines a high degree of large- and medium-scale integrated circuitry to achieve great economy, high performance, and reliability. It has a memory cycle time of 1200 nanoseconds, and executes arithmetic and logical instructions in only 1350 nanoseconds.

Nova 800 is even faster than Nova 1200. It has a basic memory cycle time of 800 nanoseconds, and executes arithmetic and logical instructions in a single 800-nanosecond cycle. Its extremely flexible input/output structure makes its high speed very effective in I/O-oriented applications.

Supernova SC is the world's fastest small computer. It takes full advantage of an all-monolithic memory by overlapping instruction retrieval and execution, giving it the ability to execute arithmetic and logical instructions in a single 300-nanosecond memory cycle.

The three new computers are additions to Data General's extremely successful Nova line of mini computers.

All the Novas—the original Nova, the Supernova, and the new Nova 1200, Nova 800, and Supernova SC—share the same basic central processor architecture.

Their central processors are organized around multiple general-purpose registers or accumulators. There are four full sixteen-bit accumulators, two of which may be used as index registers. Arithmetic and logical instructions manipulate the contents of these accumulators. There is less need to address or access memory. And the availability of these multiple registers improves the efficiency of accumulator-to-memory operations and data flow between the computer and peripheral devices.

This multi-accumulator organization cuts down on the number of instructions necessary to execute a program. The Nova-line computers are much easier to program than single-accumulator machines, and complex software routines such as multiplication, division, and floating point can be performed without constantly referencing memory.

Based on this multi-accumulator design, the Novas have a powerful, flexible instruction set. For example, the same instruction that adds or subtracts can also rotate right or left the 17-bit word (16-bit accumulator combined with the carry bit), or swap its right and left halves, test the result and/or carry for a skip, and specify whether or not the result shall actually be retained.

The second major feature common to all the Novas is software. Data General offers the most extensive software library available with any line of 16-bit machines. It includes FORTRAN IV, ALGOL 60, Disc Operating System, Time Sharing BASIC, relocatable assembler, editor, symbolic debug package. And it all runs, without modification, on any of the Nova computers.

The third major common feature of the Nova line is that all the Novas use the same interfaces to the same peripheral devices. That means that a magnetic tape unit, for example, might be interfaced to a Nova 1200 and then, in a matter of minutes, be plugged in to a Supernova SC with no wiring modifications.

Data General offers all the important mini computer peripherals: discs, magnetic tape units, paper-tape equipment, card readers, plotters, Teletypes, line printers, real-time clocks, A/D, D/A, communications equipment.

The most visible feature common to the Nova line is mechanical design. The basic Nova package consists of four major elements: first, a front console panel. Second, a chassis, which consists of seven slots for mounting 15-inch square printed-circuit boards and a printed-circuit back panel through which the seven slots interconnect. Third, a power supply. Fourth, a central processor.

All of this tells you that the new Novas are part of a complete line of mini computers that use compatible software, hardware, and peripherals. The next three sections of this brochure describe the differences between the Nova 1200, Nova 800, and Supernova SC.


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MEMORY STEP
INST. STEP
PROGRAM LOAD
NOVA 1200
AC0
AC1
AC2
AC3
DEPOSIT
EXAMINE
DATA GENERAL CORPORATION

THE NOVA 1200 IS VERY FAST.

To be better than the competition, a mini computer must go faster and cost less than the competition. That's what the Nova 1200 does.

The Nova 1200 is the least expensive 16-bit mini computer available. Yet it has a cycle time of 1200 nanoseconds and executes arithmetic and logical instructions in only 1350 nanoseconds. That's at the upper end of the 16-bit performance range.

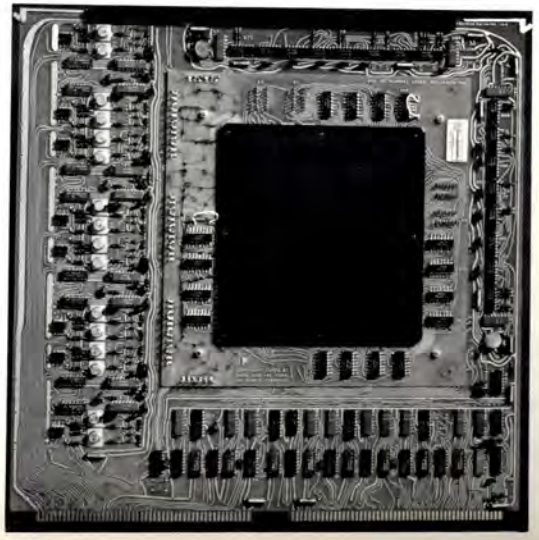
The Nova 1200 is the first mini computer to employ large-scale integrated circuits in its central processor. It takes full advantage of the highest level of integrated circuitry available (both large- and medium-scale) to achieve very high performance at the lowest price possible. And in the simplest package possible: the Nova 1200 central processor fits on a single 15-inch square printed circuit board.

The Nova 1200 4K core memory has a cycle time of only 1200 nanoseconds. Yet it is the simplest, most reliable mini computer memory available. It fits on one printed circuit board. Sixteen monolithic IC's replace the conventional XY drive circuits and their associated selector circuits. The monolithic circuits are reliable, easy to test, and compact, and their use eliminates many discrete components normally used in the XY drive circuits.

As part of its standard configuration, the Nova 1200 has a Direct Memory Access (DMA) data channel. In data channel operations, data does not have to pass through the central processor, so these operations take place at memory speed (1.2 microseconds).

Nova 1200 is a simple, compact, reliable package: in its basic configuration, the entire Nova 1200 computer, including central processor, 4096-word by 16-bit core memory, Teletype interface, Direct Memory Access data channel, and control panel, uses fewer IC packages than most mini computers use in their central processors alone.

Nova 1200 is the direct successor to Data General's first mini computer, the Nova. It is completely software compatible with the whole Nova line of mini computers, and the same peripheral interface boards used in the other Novas plug into the Nova 1200.

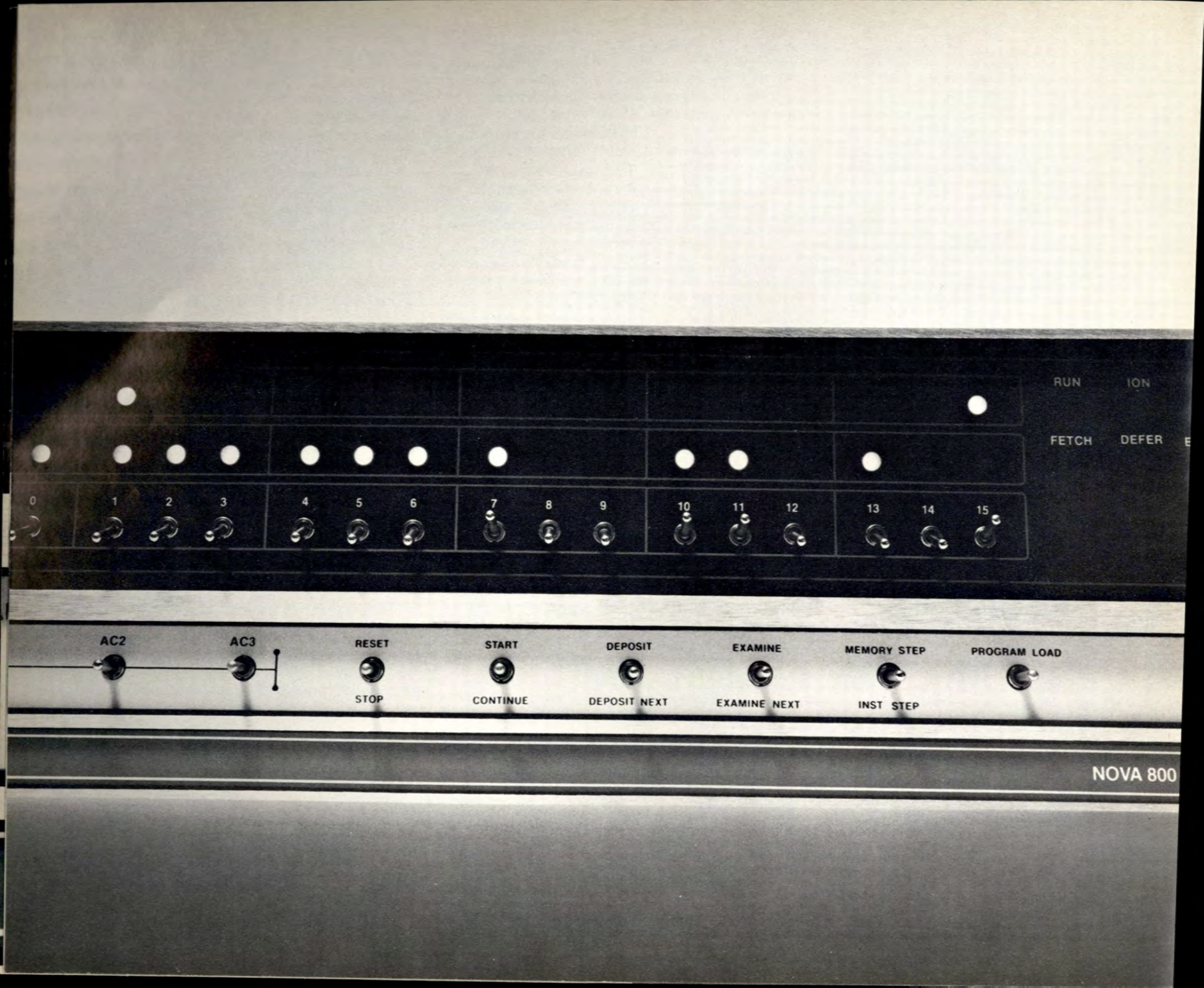


Like the original Nova, the Nova 1200 is packaged in a 5¼-inch high rack-mountable cabinet with a chassis that has plug-in slots for seven 15-inch square printed circuit subassembly boards. With a one-board central processor and one-board 4K core memory, the Nova 1200 has five slots open for memory and interface expansion. A 10½-inch high jumbo chassis with 17 subassembly slots is available with the Nova 1200. The jumbo chassis makes expansion very economical.

Automatic program load and power monitor and auto restart are central processor options and require no additional printed circuit boards.

Most important, the Nova 1200 is 2½ to 3 times faster than Nova, and costs almost one-third less.

And when you compare Nova 1200 with all the other 16-bit, multi-accumulator mini computers, it comes up at the top of the performance curves, and at the bottom of the price curves. Because the whole idea is to go faster and cost less than the competition.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EXAMINE
EXAMINE NEXT
MEMORY STEP
INST STEP
PROGRAM LOAD
NOVA 800

NOVA 800 IS FASTER.

Some people need a mini computer that goes even faster than the Nova 1200. That's the Nova 800.

Nova 800 is a fully-parallel, multi-accumulator, 16-bit, general-purpose computer. It has an 800 nanosecond cycle time, and executes arithmetic and logical instructions in a single cycle. Its basic configuration includes a 4096-word by 16-bit core memory, Direct Memory Access data channel, and Teletype interface.

Automatic program load, power monitor and auto restart, and hardware multiply/divide are central processor options and require no additional printed circuit boards.

Nova 800 uses its speed most effectively in applications with high input/output requirements. The Nova 800 has a built-in data channel with a high speed capability for fast I/O devices and a standard capability for slower devices.

The data channel is a true cycle-stealing channel: it can interrupt the central processor in the middle of an instruction. So the latency time for handling a data channel request is very low.

Nova 800 uses the same compact package as the other Nova-line computers. It's 5¼ inches high, and its chassis includes seven slots for mounting 15-inch square subassembly boards. A 10½-inch high jumbo chassis with 17 subassembly slots is also available. This chassis makes expansion very economical.

The Nova 800 uses the same peripheral interfaces as all the other Novas. A hardware/software system developed around the Nova 1200 can be upgraded to Nova 800 performance simply by substituting the two-board Nova 800 central processor for the one-board Nova 1200 processor, and the faster Nova 800 4K core memory boards for Nova 1200 memories. Interfaces remain exactly the same, and the same software runs faster.

Nova 800 is a faster mini computer for more money. And when that's what you need, it's very reassuring to know where you can get it.


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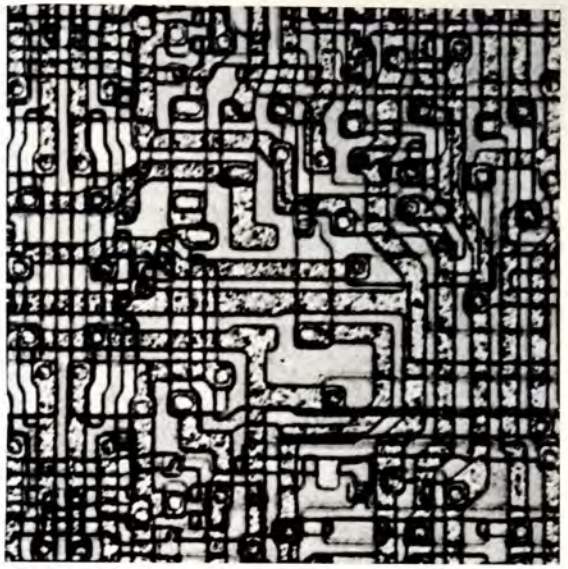
CHANNEL START
DATA GENERAL CORPORATION
SUPERNOVA SC



SUPERNOVA SC IS SUPERFAST.

Some people need a computer that goes very fast; it must have an instruction execution time well below half a microsecond. In the past, because there were no mini computers that could meet their requirements, these people bought much larger, more expensive machines.

Supernova SC is the world's fastest mini computer. Using all-monolithic memory, its memory cycle time is 300 nanoseconds, faster than most large-scale data processing computers. More important, its execution time for arithmetic and logical instructions is also 300 nanoseconds: a single instruction cycle. This means that the Supernova SC can handle applications that no mini computer has been able to tackle before. At a mini computer price.

Supernova SC has all the performance features and options built into the Supernova: it uses the same central processor as the standard Supernova, and 800-nanosecond core memory can be interchanged and mixed with 300-nanosecond monolithic memory. As in the Supernova, power-monitor and auto restart and hardware multiply/divide are central processor options, and do not require additional printed circuit boards. Memory allocation and protection is also available.

Supernova SC is fastest because it takes full advantage of a high-speed, all-monolithic memory. Since there is no memory re-write required with monolithic memory, it overlaps the execute cycle with the retrieval of the next instruction. Thus it can execute arithmetic and logical instructions in 300 nanoseconds.

The large scale integrated circuitry used in the Supernova SC memory is high-speed dynamic MOS. This technology yields the high density necessary to make a monolithic memory economically feasible today for a mini computer. The 4096-word by 16-bit memory uses sixty-four 1024-bit chips. These 18-pin packages occupy roughly the same amount of board space taken by a core mat of the same capacity, and the complete 4K monolithic memory is mounted on a single 15-inch square printed circuit board. Monolithic memory is also available in 1K and 2K blocks.

Supernova SC is completely software compatible with the other computers in the Nova line, and it uses the same peripheral interfaces. Like the others, it's a 16-bit, multi-accumulator, general-purpose computer. And, like all the others, it comes in a 5¼-inch, rack-mountable cabinet with a seven-slot chassis. A 4K configuration has three slots open for memory expansion and additional interfaces.

The only real difference between the Supernova SC and all the other Novas and Supernovas is speed. The others are fast, but Supernova SC is fastest.

TOGETHER, THEY'RE WINNING THE MINI COMPUTER WAR.

The Nova line is winning the mini computer war. The first Novas were shipped in 1969. In 1970, Data General's delivery rate makes it one of the big three: only two other manufacturers ship more mini computers. Among the major small-computer manufacturers, Data General is the one company that has significantly increased its share of the market over the last two years.

Data General is winning the war by providing the kind of service you should expect from a major manufacturer. Data General customers are served by a staff of sales engineers, application engineers, and field service engineers located in offices throughout the United States, and in Europe and the United Kingdom. In Canada, Datagen of Canada Ltd. is responsible for manufacturing, sales, and service of the Nova line.

Data General field service engineers are located nationwide, within easy reach of almost every Nova-line computer. Ever since the first Nova was installed, this field service staff has established a remarkable record of fast, efficient service.

Of course, Data General's field service staff has something extra going for it: the products. Nova computers and peripherals are the simplest, most reliable, and most easily maintained available.

Reliability is an integral part of the product design. The Nova mechanical package is simple and makes all the major subsystems easily accessible for service. Data General's 15-inch printed circuit boards allow most major subsystems to be mounted on a single board, minimizing interconnections. And because the Nova computers use the highest level of medium- and large-scale integrated circuitry available, parts counts are low, there are fewer connections, and fewer potential failures.

Troubleshooting and servicing a Nova computer in the field is simple. Few boards are involved, so a malfunction usually can be isolated very easily to a single board. A spare is slid into its slot, and the original board is mailed to the Data General factory for repair. And no operating time is lost.

Free customer training classes for Nova maintenance and programming are held on a frequent, regular schedule at the Data General plant. Each customer also receives complete documentation, covering use of the computer and its software, interfacing and installation,and maintenance. Customer documentation is continuously updated, as is the extensive library of Nova software.

Data General also offers the most liberal quantity discount schedules available.

To put it most simply, Data General is winning the mini computer war by consistently providing the best performing, least expensive mini computers and all the hardware, software, customer support, and service that go with them.

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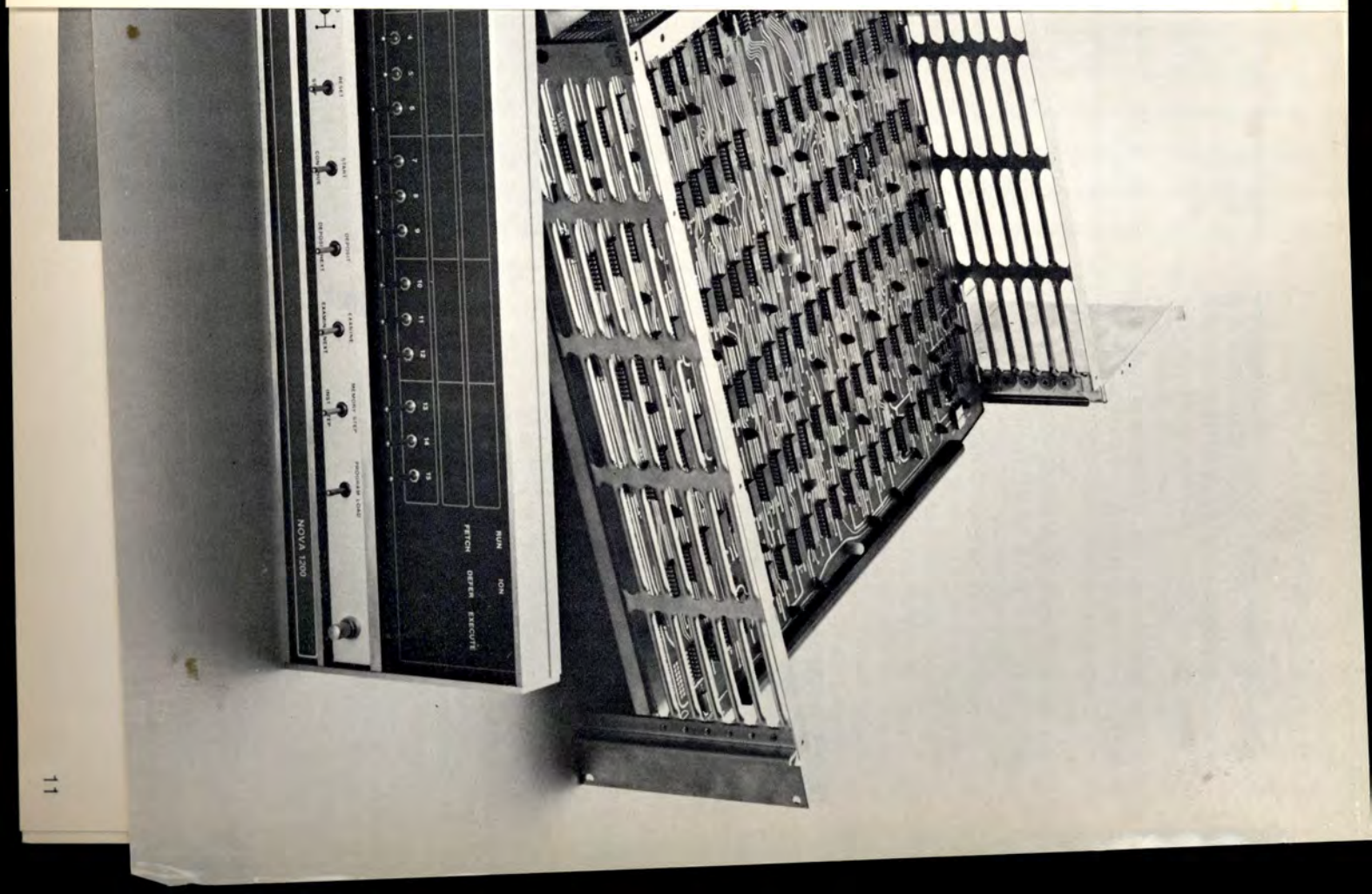

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I want more information about

- ☐ Nova 1200
- ☐ Nova 800
- ☐ Supernova SC
- ☐ Timesharing BASIC
- ☐ Numerical Control
- ☐ Data Communications

Name _____ Title _____

Company/Organization _____ Phone _____

Address _____ State _____ Zip _____

City _____

My application interest is _____

NOVA 1200

Nova 1200 is a 16-bit word, general-purpose computer with a cycle time of 1200 nanoseconds. It has four accumulators, two of which may be used as index registers. Core memory comes in blocks of 2K or 4K and can be expanded to 32K. The computer is 5¼-inches tall and comes in a table-top enclosure or with slide mounts for a 19-inch rack. The standard chassis has 7 subassembly slots. The central processor uses one slot, and the remaining slots may hold up to 24K of core memory or interfaces for peripheral devices. A 10½-inch high jumbo chassis with 17 subassembly slots and an expansion chassis with 7 additional slots are available.

The price of the Nova 1200, including 4K of core memory, Direct Memory Access data channel, automatic interrupt source identification, and Teletype interface, is $5,450.

NOVA 800

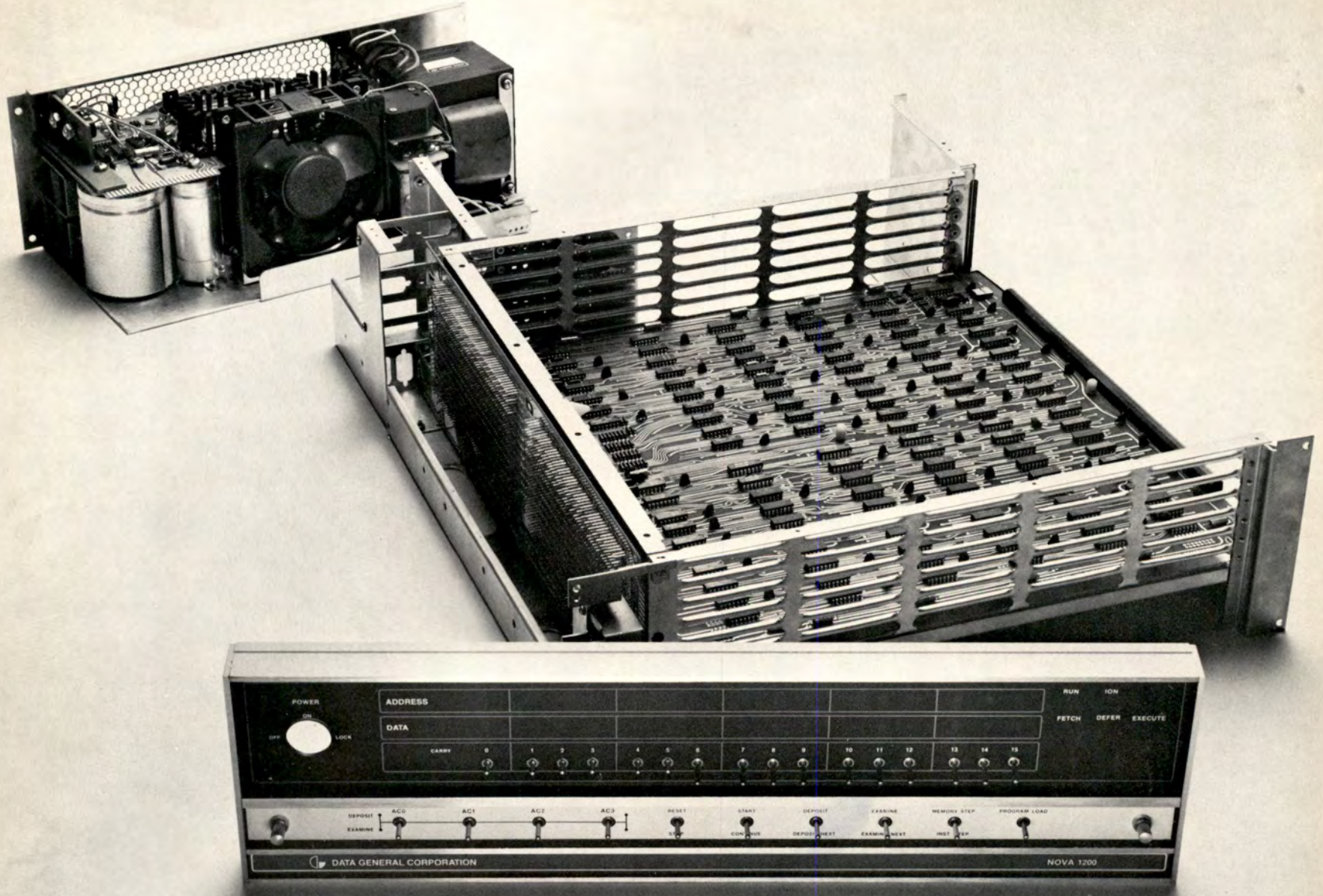
Nova 800 is a 16-bit word, fully parallel, general-purpose computer with a cycle time of 800 nanoseconds. It has four accumulators, two of which may be used as index registers. Core memory comes in blocks of 2K or 4K and can be expanded to 32K. The computer is 5¼-inches tall and comes in a table top enclosure or with slide mounts for a 19-inch rack. The standard chassis has 7 subassembly slots. The central processor uses two slots, and the remaining slots may hold up to 20K of core memory or interfaces for peripheral devices. A 10½-inch high jumbo chassis with 17 subassembly slots and an expansion chassis with 7 additional slots are available.

The price of the Nova 800, including 4K of core memory, Direct Memory Access data channel, automatic interrupt source identification, and Teletype interface, is $6,950.

SUPERNOVA SC

Supernova SC is a 16-bit word, fully parallel, general-purpose computer. It has four accumulators, two of which may be used as index registers. Its all monolithic memory has a cycle time of 300 nanoseconds, comes in blocks of 1K, 2K, or 4K, and can be expanded to 32K. Interchangeable core memory with a cycle time of 800 nanoseconds is available in 4K blocks. The computer is 5¼-inches tall and comes in a table-top enclosure or with slide mounts for a 19-inch rack. The standard chassis has 7 subassembly slots. The central processor uses three slots, and the remaining slots may hold up to 16K of monolithic or core memory or interfaces for peripheral devices. An expansion chassis with 7 additional subassembly slots is available.

The price of the Supernova SC with 4K monolithic memory, automatic program load, Direct Memory Access data channel, automatic interrupt source identification, and Teletype interface, is $11,900.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PROGRAM LOAD
DATA GENERAL CORPORATION
NOVA 1200

THEY USE THIS COMPATIBLE SOFTWARE.

The same software runs on all the Nova computers: Nova 1200, Nova 800, Supernova SC, Nova, and Supernova. Programs developed on one machine will run, without modification, on the others.

The Nova system software includes a standard assembler, a relocatable assembler, a relocatable linking loader, a character-oriented text editor, a completely symbolic debugger, single-user BASIC, timesharing BASIC, FORTRAN IV, ALGOL 60, general purpose Disc Operating System, mathematical routines, floating point interpreter, and hardware diagnostics.

Standard Assembler. The standard assembler is a two-pass system producing absolute binary and an assembly listing. Input/output is fully buffered using the priority interrupt system. A binary search is used for symbol table lookup, and hence a rapid assembly speed is achieved. The assembly language is free form. The input need not be precisely formatted into columns as is required by many small-computer assemblers.

Relocatable Assembler. The relocatable assembler has all of the features of the standard assembler. In addition, it produces relocatable binary, allows the user to define double precision integer and floating-point constants, and provides conditional assembly features.

Relocatable Linking Loader. The relocatable linking loader, in combination with the relocatable assembler, loads any number of programs and links all global symbols. The user can choose whether or not to load local symbols into a global symbol table (for access by the symbolic debugger). He can force a program to be loaded into any specific area of core. The loader can also selectively load programs from library tapes.

Editor. The character-oriented text editor facilitates the editing of any type of text. Text editors for small computers are usually line oriented: all insertions and deletions are on a line basis. The Nova editor operates on a character as well as a line basis. The user changes minor text errors in comments, for example, without deleting the entire line. Specific areas can be located quickly using string searches. This eliminates the need for source line numbering that otherwise must be done by the assembler (or user himself). All I/O is completely buffered.

Debugger. The debugger is completely symbolic. Any numerical value can be replaced by a user-defined or assembler-defined symbol. Memory searches and dumps, instruction examination and modification, and program patches can be made using instruction format commands, rather than octal commands. Program debugging is simpler for novices, since there is no need to know octal codes for instructions.

The symbolic debugger can accept from the relocatable loader a symbol table containing local as well as global symbols, so the user can employ symbolic names, rather than absolute addresses, while he is debugging a program.

Up to eight breakpoints within a user program can be active at a time.

Basic. Two BASIC systems are available: a single-user version and a timesharing version. BASIC is an easily-learned language that allows the programmer to solve problems using a number of common statements closely resembling simple algebra.

Single-user BASIC runs in any Nova computer with at least 4096 words of core memory and Teletype. This version of BASIC makes it possi-

ble for a dedicated computer system to be used for general computation when it is not needed for its primary function.

Timesharing BASIC runs in any Nova computer with at least 8192 words of core memory, and it can support up to sixteen users. It includes the matrix extension, for construction and easy manipulation of matrices, and the string extension, which permits the manipulation of alphanumeric data. Timesharing BASIC is especially attractive as a very economical means of supplying a general computing capability in a technical environment. An eight-user BASIC system costs considerably less than eight sophisticated desk calculators, and provides a great deal more computer power. It can also be less expensive than using a timesharing utility, and in many cases can offer comparable service with greater flexibility.

Algol. Data General's ALGOL 60 compiler is designed for mini computer systems developers and other sophisticated users.

It is a full implementation of ALGOL 60. It generates optimized assembly language code. Recursive procedures are allowed. Specification of formal parameters is not mandatory. Array declarations may be any arithmetic expression, including function calls. Integer labels and conditional expressions can be used. A program in ALGOL can call assembly language subroutines.

Extensions provide for the manipulation of character strings, pointer and based variables, and subscripted labels. Data General's ALGOL provides virtually unlimited precision arithmetic, allowing the user to achieve, for example, up to 30 digits of precision.

No other mini computers (and very few large computer systems) offer full ALGOL 60 with these features.

Fortran. Data General's complete ANSI Fortran IV produces optimized machine language code. The full Fortran IV, which allows up to 31 characters in variable names and up to 128 dimensions per array, has a series of significant extensions: lower as well as upper bounds for array dimensions; mixed mode expressions; strings within quotes; conditional subroutine returns; recursive subroutines; mixed ASCII and binary I/O under format control; conditional compilation. Programs written in Fortran may call assembly language subroutines.

Disc Operating System. The Disc Operating System, using Data General's fixed-head disc storage, simplifies user operation and greatly increases the efficiency of programming on the Nova computers. The operating system is device-independent and handles all user I/O, including interrupt-driven buffered service of all devices. The operating system provides a comprehensive file system capability for files of virtually any length and permits both random and sequential access.

A powerful command language interpreter enables easy access and use of the system via a Teletype console. An extensive library of system software is supported, including the relocatable assembler, editor, linking loader, and ALGOL 60 and FORTRAN IV compilers.

Mathematical Routines. The mathematical routines provided for the Nova computers range from input/output conversion to interpretive floating point. A complete library of single and double precision arithmetic routines (signed and unsigned), special code conversion, random number generation, etc., is available.

Floating Point Interpreter. The floating point interpreter is patterned after the Nova hardware architecture. Four floating point accumulators are implemented to manipulate floating point quantities. Register-to-register and memory-reference operations are defined to provide complete floating arithmetic, conversion, plus elementary transcendental functions. The interpreter is reentrant, and is therefore compatible with timesharing applications.

An extended interpreter is available for applications requiring greater precision. All of the above features are provided, as well as the specification of any length mantissa precision. For example, twenty-two digit accuracy can be obtained by specifying five-word mantissa precision. The extended interpreter is supplied as a relocatable program that calls a complete library of floating point subroutines. For applications requiring faster floating point calculators, the individual subroutines may be called without entering the interpreter.

Diagnostics. Extremely thorough diagnostics are provided for both mainframes and peripherals. The Nova central processor diagnostic, for example, makes a gate-by-gate check of the CPU logic, rather than a simple functional check. Peripheral diagnostics are equally thorough.

Datapoint. Datapoint is a two-axis, point-to-point machine tool parts programming language. The Datapoint language is easy to learn, consisting of a small number of supervisory and editing commands and a number of geometric statements. The commands are brief (1 to 3 characters) and generally self-explanatory. The geometric statements for parts programming are equally simple.

Core data is in permanent memory or a buffer that holds text input and temporary memory. Buffer space is dynamically allocated. An extensive set of error messages prevents users from creating programs that cannot be executed.

Jumbo Central Processor. Nova 1200 and Nova 800 are available in 10½-inch high chassis that include central processor, front console, power supplies, expanded back wiring panel, and 17 slots (rather than the standard seven) for mounting 15-inch square subassembly boards.

Table Top Cabinet. Nova 1200 and Nova 800 central processors are available with slides for mounting in a standard 19-inch rack, or with a cabinet for table-top use. There is no additional cost for the cabinet.

Expansion Chassis. An expansion chassis is available for all Nova-line computers. It includes a back wiring panel, a power supply, and slots for mounting seven subassembly boards. This unit can be mounted directly above the central processor frame and is used to mount additional memory and peripheral interfaces.

Core Memories. 4096 or 2048 16-bit words of core memory and all necessary electronics, mounted on a single 15-inch square subassembly board which plugs directly into one of the chassis slots with no wiring modification.

All Monolithic Memories. 4096, 2048, or 1024 16-bit words of monolithic memory and all necessary electronics, mounted on a single 15-inch subassembly board which plugs directly into one of the chassis slots with no wiring modification. Interchangeable with core memory. Monolithic memory has a 300-nanosecond cycle time and is available only with Supernova.

THESE COMPATIBLE OPTIONS AND PERIPHERALS.

Power Monitor and Auto Restart. Provides power level detection and a flag which is attached to the program interrupt and can be sensed by the program. It allows the program to become aware of an imminent power failure so it can provide for an orderly shut down. The program automatically restarts at location 0 when power is restored.

Real-Time Clock. Provides a flag which can be enabled by the program to provide a program interrupt at a fixed frequency. The AC line or a crystal clock may be program-selected as the time source.

Teletypes and Teletype Input/Output Interface. Provides an interface to any one of the Teletype models listed below:

Teletype ASR33: keyboard/printer, 8 channel reader/punch, 10 char./sec.
Teletype KSR33: keyboard/printer, 10 char./sec.
Teletype KSR35: keyboard/printer, 10 char./sec.
Teletype ASR37: keyboard/printer, 8 channel reader/punch (upper/lower case), 15 char./sec.
Teletype KSR37: keyboard/printer (upper/lower case), 15 char./sec.

Teletype Modification Kit. Converts Teletype ASR 33TZ to on-line operation for use with Teletype Input/Output Interface.

High-Speed Perforated Tape Reader and Control. Senses eight-channel, fan-fold, perforated Mylar or paper tape photoelectrically at 300 characters per second.

High-Speed Perforated Tape Punch and Control. Punches eight-channel, fan-fold paper tape at 63.3 characters per second. A remote-operation modification allows power turn-on and turn-off under program control.

Card Readers and Control. Soroban SCCR card reader and control operates at 225 or 400 cards per minute.

Incremental Plotters and Control. Plotters and control interfaces for the California Computer Products 500 Series units (drum or flat-bed) or the Houston Instruments Complot DP-1 Digital Plotter (uses Z-fold paper).

Discs and Disc Control. Control and interfaces for up to eight discs. Head-per-track discs have storage capacities of 64K, 128K, or 256K 16-bit words. Data transfer is through the data channel. Discs are rack-mountable.

Magnetic Tape Transports Control. Controls up to eight synchronous read/write 7- or 9-track, industry-compatible tape transports.

Line Printer and Control. Line printer and control includes full ASCII interface with paper-advance

characters. Line printers are either 356 lpm, 80 columns, 64 characters or 245 lpm, 132 columns, 64 characters.

High-Speed Communications Controller. Used with high-speed full-duplex or half-duplex synchronous data sets (Bell 201, Bell 301, or equivalent). Allows automatic line synchronization, word assembly, and end-of-transmission recognition.

Data Communications Interface. Input/Output Interface for Bell System type 202 data set or equivalent for operation at 1200 baud.

16 Line Teletype Multiplexer. Controls up to 16 Teletypes or Bell type 103 modems. Allows for programmed bit assembly/disassembly of characters.

Multiprocessor Communications Adapter. Connects up to fifteen Nova-line computers into a multiprocessor system by permitting blocks of data to be transferred from one computer to another through the computers' data channel facilities.

360/370 Interface. A very flexible, generalized interface that makes it possible for any Nova-line computer with appropriate software to emulate all standard IBM peripheral controllers. Communications take place via the System 360 or 370 selector or multiplexer channel.

Analog-to-Digital Converters and Interfaces. Analog-to-digital converters are available having 1 to 256 channels and word length of 8 to 14 bits. The analog-to-digital interface also runs 3½ digit panel meters.

Digital-to-Analog Converters and Interfaces. Digital-to-analog converters are available having 1 to 32 channels and word lengths of 8 to 14 bits.

Hardware Multiply/Divide. Multiplies two 16-bit numbers to produce a 32-bit product, and divides a 32-bit dividend by a 16-bit divisor to produce a quotient and a remainder.

Memory Allocation and Protection (MAP). Provides instruction protection, memory mapping, and memory protection, allowing a number of programs to share processor time. Available only with Supernova.

Supernova High Speed Data Channel. Allows very high speed data transfers between the Supernova and external devices by circumventing the standard Supernova data channel. Consecutive transfer rates range from 1MHz for the various data channel operations.

Automatic Program Load. For the Nova 1200 and the Nova 800, automatic program load (hardwired bootstrap loader) is a central processor option and does not use an additional subassembly slot. It is standard equipment for the Supernova. Programs can be loaded automatically through standard I/O devices or data channel devices.

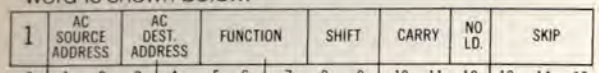
General Purpose Wiring Frame and Boards. The frame with 200-pin connector is mounted on a standard Data General 15-inch square subassembly board and plugs directly into one of the chassis slots. The frame carries up to eight 3¼" by 6¾" general purpose wiring boards, which are available with or without wire-wrap pins and sockets.

General Purpose Interface. The interface is mounted on a standard Data General 15-inch square subassembly board. It includes Busy and Done logic, device selection, interrupt request and acknowledge logic, interrupt mask, and I/O signal selection. Mounting spaces are provided for integrated circuits or sockets. Also available with 16-bit input register and 16-bit output register and with data channel synchronization and request logic, current address register and word count register.

Cabinets. Vertical rack-mounting cabinets, 19 inches wide and 29 inches deep, are available in heights of 63 inches and 28 inches. Cabinets include side panels, full length rear door with louvres, and removable top panel.

Arithmetic and Logical Instructions

The structure of an arithmetic or logical instruction word is shown below.



000	COM	01	L	01	Z
001	NEG	10	R	10	O
010	MOV	11	S	11	C
011	INC				
100	ADC				
101	SUB				
110	ADD				
111	AND				

001	SKP
010	SZC
011	SNC
100	SZR
101	SNR
110	SEZ
111	SBN

Each instruction in this class specifies one or two accumulators to supply operands to the function generator, which performs the function specified and produces a carry bit, whose value depends upon a base value specified by the instruction, the function performed, and the result obtained. The base value may be derived from the Carry flag, or the instruction may specify an independent value.

operation and test the result for a skip without affecting Carry or any accumulator.

The Carry flag can be used in conjunction with the sign of a result to detect overflow in operations on signed numbers, but its primary use is as a carry out of the most significant bit in operations on unsigned numbers, such as the lower order parts in multiple precision arithmetic. For unsigned numbers, a carry is produced if addition or incrementing increases the number beyond $2^{16}-1$. In subtraction, the condition is the same if, instead of subtracting, the complement of the subtrahend is added and 1 is added to the result (subtraction is performed by adding the twos complement). In terms of the original operands, the subtraction A−B produces a carry if A ≥ B.

The arithmetic and logical class includes eight functions: five arithmetic, three logical. In the following descriptions, ACS and ACD refer to the source and destination accumulators.

COM Complement. Place the (logical) complement of the word from ACS in ACD.

NEG Negate. Place the twos complement of the number from ACS into ACD. Complement Carry if ACS contains zero. (Forming the twos complement of zero generates a carry, because complementing zero produces a word containing all 1s, and adding 1 to that produces all zeros again, plus a carry.)

MOV Move. Place the contents of ACS in ACD.

INC Increment. Add 1 to the number from ACS and place it in ACD. If the result is 2^{16}, complement Carry.

ADC Add Complement. Add the (logical) complement of the number from ACS to the number from ACD and place the result in ACD. If the original ACD > ACS, complement Carry.

SUB Subtract. Add the twos complement of the number from ACS to the number from ACD and place the result in ACD. If the original ACD ≥ ACS, complement Carry.

ADD Add. Add the number from ACS to the number from ACD and place the result in ACD. If the result is ≥ 2^{16}, complement Carry.

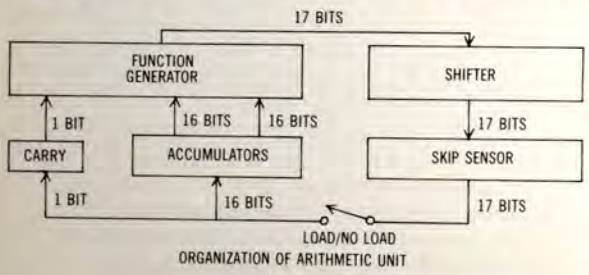
AND And. Place the logical AND function of the word from ACS and the word from ACD in ACD.

These are the basic forms of the eight arithmetic and logical instructions in which the result is loaded, there is neither shifting nor skipping, and the present state of the Carry flag is used as a base value for carry generation (the Carry flag is complemented if a carry is generated by an arithmetic function, otherwise the original state is retained).

By appending other symbols to the basic mnemonics, the programmer can specify zero, 1, or the complement of the current state of the Carry flag as the base value for carry generation; can shift (rotate) the 17-bit function result with carry one place to the left or right, or swap halves of the 16-bit function result; and he can inhibit the loading of the 17-bit final result into ACD and Carry. He can also test the final result, whether loaded or not, for a skip as follows:

SKP Always Skip.
SZC Skip on Zero Carry.
SNC Skip on Nonzero Carry.
SZR Skip on Zero Result.
SNR Skip on Nonzero Result.
SEZ Skip if Either Carry or Result is Zero.
SBN Skip if Both Carry and Result are Nonzero.

AND THIS POWERFUL INSTRUCTION SET.



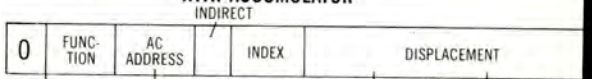
ORGANIZATION OF ARITHMETIC UNIT

The 17-bit output of the function generator, comprising the carry bit and the 16-bit function result, then goes to the shifter. Here the 17-bit result can be rotated one place right or left, or the two 8-bit halves of the 16-bit function result can be swapped without affecting the carry bit. The 17-bit shifter output can then be tested for a skip; the skip sensor can test whether the carry bit or the rest of the 17-bit word is or is not equal to zero. The 17-bit shifted word can be loaded into Carry and one of the accumulators selected by the instruction. However, loading is not necessary: an instruction can perform a complicated arithmetic and shifting

Memory Reference Instructions

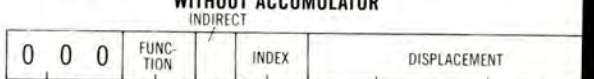
There are two formats for memory reference instructions, depending on whether an accumulator is specified.

WITH ACCUMULATOR



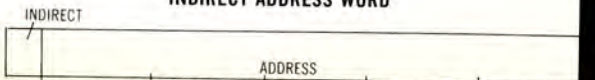
01 LDA
10 STA

WITHOUT ACCUMULATOR



00 JMP
01 JSR
10 ISZ
11 DSZ

INDIRECT ADDRESS WORD



Memory reference instructions must address a memory location. Each instruction word contains information for determining the effective address E, which is the actual address used to fetch or store the operand or alter program flow. The address information comprises an 8-bit displacement, a 2-bit index selection, and a single indirect bit. The displacement can directly address any location in four groups of 256 locations each. It can be an absolute address. That is, it may be used simply to address a location in page zero, the first 256 locations in memory. It can also be taken as a signed number used to compute an absolute address by adding it to a 15-bit base address supplied by an index register. The index bits can select AC2 or AC3 as the index register; either of these accumulators can thus be used as an ordinary index register to vary the address computed from a constant displacement, or as a base register for a set of different displacements. The program can also select the program counter as the index register, so any instruction can address 256 words in its own vicinity (relative addressing).

The computed absolute (15-bit) address can be the effective address. However, the instruction can use it as an indirect address. That is, it can specify a location to be used to retrieve another address. The word read from an indirectly addressed location contains an absolute address and an indirect bit; this address can be the effective address, or it can be another indirect address.

The program can make use of an automatic indexing feature by indirectly addressing any memory location from 00020 to 00037 (addresses are always octal numbers). Whenever one of these locations is specified by an indirect address, the processor retrieves its contents, increments or decrements the word retrieved, writes the altered word back into memory, and uses the altered word as the new address, direct or indirect. If the word is taken from locations 00020-00027, it is incremented by 1; if taken from locations 00030-00037, it is decremented by 1.

There are three pairs of memory reference instructions. Two instructions move data between memory and the accumulators; two modify a memory location and test the result for a skip; and two allow the programmer to alter the normal program sequence by jumping to an arbitrary location. The modify-memory instructions are used to count loop iterations or successively modify a word for a series of operations. The jump instructions are especially useful for calling and returning from subroutines. In the following descriptions AC is the accumulator (if any) specified by the instruction, and E represents the effective address calculated from the address information given by the instruction.

LDA Load Accumulator. Load the contents of location E into AC.

STA Store Accumulator. Store the contents of AC in location E.

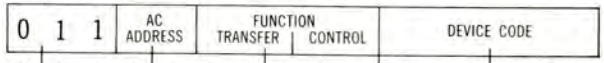
ISZ Increment and Skip if Zero. Add 1 to the contents of location E and place the result back in E. Skip the next instruction in sequence if the result is zero.

DSZ Decrement and Skip if Zero. Subtract 1 from the contents of location E and place the result back in E. Skip the next instruction in sequence if the result is zero.

JMP Jump. Load E into PC. Take the next instruction from location E and continue sequential operation from there.

JSR Jump to Subroutine. Load an address one greater than that in PC into AC3 (hence AC3 receives the address of the location following the JSR instruction). Load E into PC. Take the next instruction from location E and continue sequential operation from there.

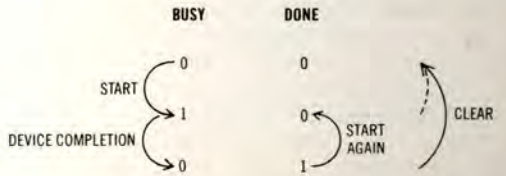
Input/Output Instructions. The format for input/output instructions is shown below.



000	NIO	01	S
001	DIA	10	C
010	DOA	11	P
011	DIB		
100	DOB		
101	DIC		
110	DOC		
111	SKP	00	BN
		01	BZ
		10	DN
		11	DZ

Input/output instructions govern all transfers of data to and from peripheral equipment, and perform various operations within the processor. An input/output instruction word has six bits for specifying the device. This format allows sixty-four device codes, of which sixty-two can be used to address devices (octal 01-76). The code 00 is not used, and 77 is used for special functions, including reading the console data switches and controlling the program interrupt.

Every device has a 6-bit device selection network, an Interrupt Disable flag, and Busy and Done flags. The selection network decodes the device code part of the instruction so that only the addressed device responds to signals sent by the processor over the I/O bus. The Busy and Done flags together denote the basic state of the device. When both are clear the device is idle. To place the device in operation, the program sets Busy. If the device will be used for output, the program must give a data-out instruction that sends the first unit of data—a word or character depending on how the device handles information. When the device has processed a unit of data, it clears Busy and sets Done to indicate that it is ready to receive new data for output, or that it has data ready for input. In the former case the program would respond with a data-out instruction to send more data; in the latter with a data-in instruction to bring in the data that is ready. If the Interrupt Disable flag is clear, the setting of Done signals the program by requesting an interrupt; if the program has set Interrupt Disable, then it must keep testing Done or Busy to determine when the device is ready.



In all input/output instructions two bits either control or sense Busy and Done. In a skip instruction, the two bits specify the flag and the state

on which the skip is to occur. In a transfer instruction, these bits can be used to specify a control function to be performed in addition to the transfer. Control functions are available to start the device by clearing Done and setting Busy; to clear both Busy and Done, idling the device; and to generate a special pulse whose effect, if any, depends on the device.

The overall sequence of Busy and Done states is determined by both the program and the internal operation of the device.

The data-in or data-out instruction that the program gives in response to the setting of Done can also restart the device. When all the data has been transferred the program generally clears Done so the device neither requests further interrupts nor appears to be in use, but this is not necessary. Busy and Done both set is a meaningless situation.

With a single device code the program can address up to three registers in the device. These are referred to simply as the A, B and C buffers. For each buffer there is a pair of transfer instructions, one to move data into an accumulator from the buffer, another to move data from an accumulator out to the buffer. Thus every one of these six transfer instructions must specify a device and an accumulator, and may specify a control function as well.

DIA Data In A
DOA Data Out A
DIB Data In B
DOB Data Out B
DIC Data In C
DOC Data Out C

The amount of data actually supplied or accepted by the device depends on the size of its buffer, its mode of operation, and so forth. The remaining input/output instructions specify a device and either a function or a skip condition.

NIO No IO Transfer. Perform the specified control function.
SKPBN Skip if Busy is Nonzero.
SKPBZ Skip if Busy is Zero.
SKPDN Skip if Done is Nonzero
SKPDZ Skip if Done is Zero.

Input/output instructions with the device code 77 (CPU) perform a number of special functions rather than controlling a specific device. In a transfer instruction there may or may not actually be a transfer, but the start and clear control functions turn the interrupt on and off. The skip instructions sense the Interrupt On and Power Failure flags. In some cases the assembler recognizes a special mnemonic that includes both the instruction mnemonic and the CPU device code (these are given in the second column).

NIOS CPU INTEN
Interrupt Enable.
NIOC CPU INTDS
Interrupt Disable.
DIA AC, CPU READS
Read Switches. Read the contents of the console data switches into AC.
DIB AC, CPU INTA
Interrupt Acknowledge. Place in AC the device code of the first device on the bus that is requesting an interrupt ("first" means physically closest to the processor on the bus).
DOB AC, CPU MSKO
Mask Out. Set up the Interrupt Disable flags in the devices according to the mask in AC. For this purpose each device is connected to a given data line, and its flag is set or cleared as the corresponding bit in the mask is 1 or 0.
DIC O, CPU
Clear IO Devices. Clear the control flip-flops, including Busy, Done and Interrupt Disable, in all devices connected to the Bus.
DICC O, CPU IORST
IO Reset. Clear all IO devices and disable the interrupt.
DOC O, CPU HALT
Halt the Processor.
SKPBN CPU
Skip if Interrupt On is Nonzero.
SKPBZ CPU
Skip if Interrupt On is Zero.
SKPDN CPU
Skip if Power Failure is Nonzero.
SKPDZ CPU
Skip if Power Failure is Zero

Multiply-Divide Instructions. Hardware multiply-divide options are available for all Nova computers.

MUL Multiply. Multiply the unsigned integers in AC1 and AC2 to generate a double length product; add the product to the unsigned integer in AC0, and place the high and low order parts of the result respectively in AC0 and AC1 (in other words the result left in AC0 and AC1 is AC0+AC1×AC2).
DIV Divide. If the unsigned integer in AC0 is greater than or equal to the unsigned integer in AC2, set Carry and go immediately to the next instruction without affecting the original contents of the accumulators. Otherwise Divide the double length unsigned integer in in AC0 and AC1 by the unsigned integer in AC2, producing a single length quotient including leading zeros, and then clear carry. Place the quotient in AC1 and the remainder in AC0.

INSTRUCTION EXECUTION TIMES

	Supernova SC	Supernova Core	Nova 800	Nova 1200	Nova
LDA	1.2μ	1.6μ	1.6μ	2.55μ	5.2μ
STA	1.2	1.6	1.6	2.55	5.5
ISZ, DSZ	1.4	1.8	1.8	3.15*	5.2
JMP	.6	.8	.8	1.35	2.6
JSR	1.2	1.4	.8	1.35	3.5
Indirect addressing add	.6	.8	.8	1.2	2.6
Base register addressing add	0	0	0	0	.3
Autoindexing add	.2	.2	.2	.6	0
COM, NEG, MOV, INC	.3*	.8*	.8*	1.35*	5.6
ADC, SUB, ADD, AND	.3*	.8*	.8*	1.35*	5.9
*If skip occurs add	.3/.6‡	.8	.2	1.35	
IO input (except INTA)	2.8	2.9	2.2†	2.55	4.4
NIO	3.2	3.3	2.2†	3.15	4.7
IO output	3.2	3.3	2.2†	3.15	4.7
†S, C or P add			.6		
IO skips	2.8	2.9	1.4*	2.55	4.4
INTA	3.6	3.7	2.2	2.55	4.4
MUL			8.8		11.1
Average	3.7	3.8			
Maximum	5.3	5.4			
DIV	6.8	6.9	8.8		11.9
Unsuccessful	1.5	1.6	1.6		
Interrupt	1.8	2.2	1.6	3.0	5.2
Latency					
With multiply-divide	9.0	9.0	10.6		12.0
Without multiply-divide	5.0	5.0	4.6	6.0	12.0

‡Add .3μ if arithmetic or logical instruction is skipped, otherwise add .6μ

SPECIFICATIONS

Nova 1200 Specifications. Nova 1200 is a 16-bit word, general-purpose computer with a cycle time of 1200 nanoseconds. It has four accumulators, two of which may be used as index registers. Core memory comes in blocks of 2K or 4K and can be expanded to 32K. Nova 1200 comes in a 5¼" tall package which includes either slides for mounting in a standard 19-inch rack or a table-top enclosure. The standard chassis has 7 subassembly slots. The central processor uses one slot, and the remaining slots may hold up to 24K of core memory or interfaces for peripheral devices. A 10½-inch high jumbo chassis has 17 slots. High-speed Direct Memory Access (DMA) channel, and automatic interrupt source identification are standard equipment. Automatic program load and power monitor and auto restart are central processor options and require no additional printed circuit boards.

Electrical Specifications (Power Requirements). 115 or 230 volts ±20%, 47 to 63 Hz single phase power capable of supplying 15 amperes (other frequencies and voltages available on special order). Receptacle required to receive standard three wire plug. Power Dissipation 300 watts typical. I/O Bus Levels Ground and +3 volts (standard TTL integrated circuit logic levels).

Environmental Specifications. Operating Temperature 0°C to +55°C. Relative Humidity to 90%. Dimensions: Weight 50 pounds; Height 5¼ inches; Width 19 inches. Depth 23 inches.

Nova 800 Specifications. Nova 800 is a 16-bit word, fully parallel, general-purpose computer with a cycle time of 800 nanoseconds. It has four accumulators, two of which may be used as index registers. Core memory comes in blocks of 2K or 4K and can be expanded to 32K. Nova 800 comes in a 5¼" tall package which includes either slides for mounting in a standard 19-inch rack or a table-top enclosure. The standard chassis has 7 subassembly slots. The central processor uses two slots, and the remaining slots may hold up to 20K of core memory or interfaces for peripheral devices. A 10½-inch high jumbo chassis has 17 slots. High-speed Direct Memory Access (DMA) channel, and automatic interrupt source identification are standard equipment. Automatic program load, power monitor and auto restart, and hardware multiply/divide are central processor options and require no additional printed circuit boards.

Electrical Specifications (Power Requirements). 115 or 230 volts ±20%, 47 to 63 Hz single phase power capable of supplying 15 amperes (other frequencies and voltages available on special order). Receptacle required to receive standard three wire plug. Power Dissipation 300 watts typical.I/O Bus Levels Ground and +3 volts (standard TTL integrated circuit logic levels).

Environmental Specifications. Operating Temperature 0°C to +55°C. Relative Humidity to 90%. Dimensions: Weight 50 pounds; Height 5¼ inches; Width 19 inches; Depth 23 inches.

Supernova SC Specifications. Supernova SC is a 16-bit word fully parallel, general-purpose computer. It has four accumulators, two of which may be used as index registers. Its all monolithic memory has a cycle time of 300 nanoseconds, comes in blocks of 1K, 2K, or 4K, and can be expanded to 32K. Interchangeable core memory with a cycle time of 800 nanoseconds is also available. Supernova SC comes in a 5¼" tall rack-mountable package which includes slides for mounting in a standard 19-inch rack. The Supernova central processor uses three slots, and the remaining slots may hold up to 16K of monolithic or core memory or interfaces for peripheral devices. High-speed Direct Memory Access (DMA) channel, automatic interrupt source identification, and automatic program load are standard equipment. Power monitor and auto restart and hardware multiply/divide are central processor options and require no additional printed circuit boards.

Electrical Specifications (Power Requirements). 115 or 230 volts ±10%, 47 to 63 Hz single phase power capable of supplying 15 amperes (other frequencies and voltages available on special order). Receptacle required to receive standard three wire plug. Power Dissipation 600 watts typical. I/O Bus Levels Ground and +3 volts (standard TTL integrated circuit logic levels).

Environmental Specifications. Operating Temperature 0°C to +55°C. Relative Humidity to 90%. Dimensions: Weight 60 pounds; Height 5¼ inches; Width 19 inches. Depth 22 inches.

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