X6818.2013

Control Data Corporation

1604-A

CONTROL DATA 1604-A COMPUTER

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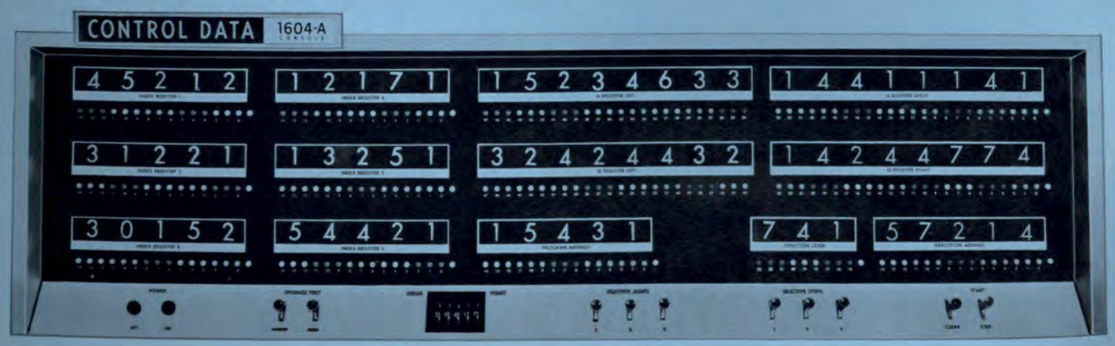
The Control Data 1604-A is a large-scale general purpose digital computer designed to satisfy large-scale computing and data processing requirements. Featured are a storage capacity of 32,768 48-bit words, exceedingly fast computation and transfer speeds, and special provisions for handling input-output operations.

The 1604-A incorporates modifications to the Control Data 1604 Computer which are the result of Control Data's program of continuing product improvement. In summary, the 1604-A can be considered as an extension of the field-proven, highly reliable 1604 Computer, being used today in advanced research and scientific applications in government, industry, and universities.

1604-A CHARACTERISTICS

- stored-program, general-purpose digital computer
- parallel mode of operation
- 48-bit word length
- single-address logic, 2 instructions per 48-bit word:
  - operation code . . . . . 6 bits
  - index designator . . . . . 3 bits
  - base execution address . . . . . 15 bits
- 6 15-bit index registers
- indirect addressing feature
- 32,768 48-bit words of magnetic core storage:
  - storage in two independent 16,384 word banks, alternately phased
  - 4.8 microseconds effective cycle time (representative program)
  - 6.4 microseconds total cycle time each bank
- highly versatile input/output facilities:
  - 3 48-bit buffer input channels
  - 3 48-bit buffer output channels
  - 1 high speed 48-bit bi-directional input/output transfer channel (4.8 microseconds, 48-bit parallel word)
- program interrupt
- control console includes:
  - 350 character per second paper tape reader
  - 110 character per second paper tape punch
  - input/output electric typewriter
  - translated contents of all operational registers displayed as Arabic numerals (octal)
- flexible repertoire of 62 instructions provides:
  - fixed binary arithmetic (integer and fractional) • floating point binary arithmetic • multiple precision capabilities • logical and masking operations • indexing • memory searching • input/output • sequence control (conditional and unconditional).
- binary arithmetic—modulus 2^{48} minus one (one's complement):
  - parallel addition, 1.2 microseconds basic add time (without access)
- real-time clock
- completely solid state:
  - diode logic • transistor amplifiers • magnetic core memory
- small size—goes in 20′ x 20′ room
- power requirements—20,000 BTU's per hour, 3500 CFM, 5.9 kw per hour



INPUT/OUTPUT COMMUNICATION

One of the outstanding features of the Control Data 1604-A is its provisions for flexible input-output communication. In addition to communicating with standard peripheral equipment such as magnetic tape units, printer, card reader/punch, and typewriter, the 1604-A is also used for real-time control or communication such as radar and sonar systems, and special display and output systems. Its input-output capability can be assessed from the fact that read/write operations can be carried out on six high-speed, high density tape units simultaneously.

In the 1604-A Computer, input-output operations are carried out independently of the main computer program. When transmission of input-output data is required, the main computer program is used *only* to initiate an automatic cycle which buffers data to and from the computer memory. The main computer program then continues while the actual buffering of data is carried out *independently and automatically*.

The input-output section of the 1604-A contains the facility for several modes of communication. For *normal exchange of data* with peripheral equipment, independent control is provided for the transfer of data via three 48-bit input and three 48-bit output channels asynchronously with the main computer program. For *high-speed communication*, one bi-directional 48-bit input/output transfer channel is provided. Communication control is performed by the external function instruction. In addition, the interrupt feature provides requests from peripheral equipment to the computer.

BUFFER OPERATION

The three buffered input channels and the three buffered output channels are rapidly scanned by a scanner which looks for action requests from all channels. Input action requests are initiated from the peripheral equipment by indicator "flags." A complete scan is made in 2.4 microseconds.

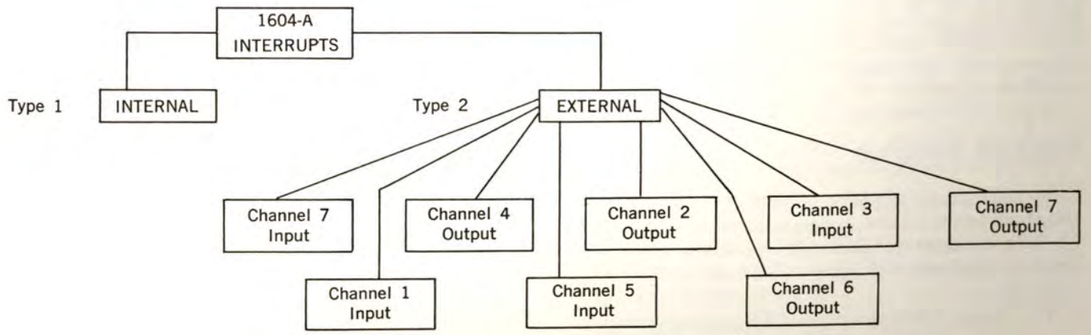
Initial output requests demand that one word be transferred by auxiliary sequence to an output register. Data is then transferred automatically to the selected peripheral equipment at its rate of speed. On subsequent requests, with a word already in memory, transfer of data proceeds at the speed of the selected peripheral equipment.

Memory of the 1604-A may be used by either the main computer program or by the Input/Output Control. A scanner prevents simultaneous use of memory by them. During I/O operations, the Input/Output Control will request the use of memory. When a request is detected by the scanner, memory is given to the Input/Output Control. The main program proceeds until a memory reference is required. Then the main computer program waits until it can access memory.

Maximum data rate through the Input/Output Control is approximately 1 million characters per second. If a system includes a Control Data 606 Magnetic Tape Transport that needs simultaneous data flow, more than ½ of the total time for data transfer to and from memory is available to the Computation Section of the 1604-A.

PROGRAM INTERRUPT

Certain conditions may arise which make it necessary to interrupt the main computer program. This may be caused by 1) a peripheral device initiating a signal on a common interrupt line which links all pieces of peripheral equipment or 2) the occurrence of specific internal conditions. Interrupts in the 1604-A are classified first as internal and external. External interrupts are classified into eight categories—one for each of six buffered channels, and one for Channel 7 input, and one for Channel 7 output, shown as follows:



When a selected interrupt occurs, control is automatically transferred from the main computer program to one of the memory locations shown in the table below. For example, if an interrupt condition exists on Channel 5, control is automatically transferred to Location 15.

MEMORY LOCATION	TYPE	
00007_8	Internal Interrupt	
00010_8	External Interrupt – Channel 7	(output)
00011_8	External Interrupt – Channel 1	
00012_8	External Interrupt – Channel 2	
00013_8	External Interrupt – Channel 3	
00014_8	External Interrupt – Channel 4	
00015_8	External Interrupt – Channel 5	
00016_8	External Interrupt – Channel 6	
00017_8	External Interrupt – Channel 7	(input)

In addition, the 1604-A has a Masked Interrupt Register (MIR) which is used to allow or disallow all selected interrupts. The 1604-A instruction repertoire includes instructions which clear or set any or all bits of the MIR. Thus, with one instruction any one or all selected interrupts may be allowed or disallowed.

Finally, a two-position manual (optional) switch on the 1604-A allows complete program compatibility with Control Data's 1604 Computer. By setting the switch to a position marked "1604," programs written for the 1604 will operate without change on the 1604-A.

HIGH-SPEED TRANSFER OPERATION

The main computer program performs the high-speed input-output transfer of information between 1604-A's or between one 1604-A and peripheral equipment having comparable speed. Only one instruction is required for a block of input or output data. A 48-bit word is transferred in or out in 4.8 microseconds. All transfer operations are carried out via channel 7.

EXTERNAL FUNCTION

This instruction provides control and communication between the 1604-A and peripheral equipment. It contains eight sub-instructions which select and sense peripheral equipments, or activate buffer channels.

The select sub-instruction 74.0 is interpreted as follows (see illustration below): The leftmost 6 bits are the operation code; the next 3 bits designate that this is a select sub-instruction; the next 3 bits are the channel or internal condition selection code; the next 3 bits are the equipment selection code; and the last 9 bits specify the operation for the selected equipment.

Code	0	Internal Condition or Channel selection Code	Equip. selection Code	Condition code– specifies operation for selected equipment
Operation Code 6 bits	Index Designators b = 0 3 bits	3 bits	3 bits	9 bits
		Base Execution Address 15 bits		

74.0–SELECT EXTERNAL EQUIPMENT OR INTERNAL CONDITION

The channel activate sub-instructions 74.1 through 74.6 are interpreted as follows (see illustration below): The leftmost 6 bits are the operation code; the next 3 bits designate that this is an activate sub-instruction (plus indicating the channel); and the last 15 bits indicate the initial address for data storage in the buffer operation.

Code	Select channels 1-6	Initial address for data storage in buffering operation
Operation Code 6 bits	Index Designators b = 1-6 3 bits	Base Execution Address 15 bits

74.1 - 74.6–ACTIVATE BUFFER CHANNELS 1 - 6

The sense sub-instruction 74.7 is interpreted as follows (see illustration below): The leftmost 6 bits are the operation code; the next 3 bits designate that this is a sense sub-instruction; the next 3 bits are the channel or internal condition selection code; the next 3 bits are the equipment selection code; and the last 9 bits specify the operation for the selected equipment.

Code	7	Internal Condition or Channel selection Code	Equip. selection Code	Condition code– specifies operation for selected equipment
Operation Code 6 bits	Index Designators b = 7 3 bits	3 bits	3 bits	9 bits
		Base Execution Address 15 bits		

74.7–SENSE EXTERNAL OR INTERNAL CONDITION

MAGNETIC CORE STORAGE SECTION

The storage section of the Control Data 1604-A is a large-capacity magnetic core storage system providing high-speed, non-volatile, random-access storage for 32,768 48-bit words. One 48-bit word may contain either a 48-bit data word or two 24-bit instructions. The read access time, i.e., the time from request of data to delivery of data from storage, is 2.2 microseconds.

The 32,768 48-bit word magnetic core storage section of the 1604-A Computer is controlled by a two-phase timing system, each phase controlling one-half (16,384 48-bit words) the total storage. All *odd* storage addresses reference one storage unit, all *even* addresses reference the other storage unit. The read access time of each section is 2.2 microseconds after which, without delay, the next arithmetic operation is initiated.

Each unit has a total storage cycle time of 6.4 microseconds. The storage cycles of the two sections overlap one another in the execution of a program, with the result that the effective cycle time is 3.2 microseconds when addresses of alternate memory banks are referenced. Average effective cycle time for random addresses is approximately 4.8 microseconds for a representative program.

EXPLANATION OF REGISTERS

***A-Register** – Principal arithmetic register, which functions as a 48-bit accumulator in most arithmetic operations. Quantity zero is represented by a binary zero in each stage. Contents of A may be shifted either to the right or left. Shifting may involve only the contents of A or may include the contents of Q. The leftmost sign bit is extended on shifts to right; bits shifted off the right end of A or Q are dropped. The left shifts are circular, with lower order bits being replaced by higher order bits. Multiply, divide, and floating point instructions are sequenced operations involving both A and Q.

***Q-Register** – Assists accumulator in performing more complicated arithmetic operations. Used with A to perform double precision arithmetic. Q may be shifted right or left, singly or in conjunction with A. Q may contain mask in logical operations.

Program Control Register, U^1, – Holds program step while the two instructions contained in it are executed. The 48-bit instruction word is taken from storage location specified by P and entered in U^1, the upper instruction being executed first. Execution of lower instruction follows, except when upper instruction is a jump or when it provides for conditional skipping of lower instruction.

Auxiliary Program Control Register, U^2, – An accumulator used in the modification of execution address of current instruction. This modification consists of adding contents of an Index Register to execution address of current instruction.

***P-Register** – Functions as the program address counter, which provides continuity between individual steps of the program by generating the addresses at which individual steps are contained. Upon completion of each sequential step, the count in P is advanced by one to specify address of next step. Jump instructions clear P and enter the new address in it.

***Index Registers, B^1-B^6,** – Provide modification of execution addresses in program loops. Contents of an Index Register can be advanced each pass through a loop, with an exit initiated on a given threshold. Alternate approach allows an Index Register to be preset, then reduced by one count each pass through the program – with an exit after zero.

Storage Address Registers, S^1-S^2, – Represent even and odd 16,384-word memory units respectively. Receive addresses of instructions from P and addresses of operands from U^2.

Storage Restoration Registers, Z^1-Z^2,–Represent even and odd 16,384-word memory units respectively. These registers hold the 48-bit word to be written in a given storage location.

Master Masked Interrupt Register, MMIR – Provides capability of masking all external interrupts with one instruction, at the programmer's option.

Masked Interrupt Register, MIR – Provides interrupt capability, under program control, from the various channels, including Channel 7.

R-Register–Functions as exchange register for transmission involving B-Index Registers. Used in advancing or reducing count in a given B-Register. During several instructions, used to count repetitive operations. R used with floating point instructions in performing arithmetic operations on the exponent or characteristic.

X-Register – An exchange or auxiliary arithmetic register. All input-output data passes through X.

External Function Register, O^0,–Used for exchanging control information with input-output equipment.

Output Registers, O^1 through O^4, O^1 through O^3,–Used for output buffer operations where data is transmitted at speed of input-output equipment. Where high-speed transfer is required, output transfer operations carried out via O^4.

*Operational Registers

SPECIAL 1604-A PROGRAMMING FEATURES

- Ease of Handling Constants:
  Special instructions permit the programmer to enter constants from the instruction word itself.
- Special Instructions:
  These permit the programmer to increase the A or the Index Registers by a value in the instruction word itself.
- Indexing:
  Availability of 6 Index Registers (B-Boxes) – Allow multiple address modifications without extraneous "housekeeping."
  Indirect Addressing – Simplifies table look-up and sorting.
  Both *count down* and *count up* indexing–Available on the 1604-A to perform looping. Both can be used at the *start* of a loop as well as at the *end* of a loop.
- Four Search Instructions:
  Equality Search – Searches list of words to determine equality with value in the accumulator.
  Threshold Search – Searches list of words to determine if any word is greater than value in the accumulator.
  Masked Equality Search – Searches list of words to determine if a portion of any word is equal to the value in the accumulator.
  Masked Threshold Search – Searches list of words to determine if a portion of any word is greater than the value in the accumulator.
- Floating Point:
  Allows extreme range of values to be stored and operated upon without extraneous "housekeeping," difficult manipulations, or unnecessary loss of significance.
- High-Speed Input-Output Transfers:
  Block transfer of data can be transmitted to or from the computer at computer speed.
- Buffering:
  Data can be transmitted to or from the computer asynchronously with the main computer program.
- External Function:
  Provides control or condition sensing communication with peripheral equipment by main program.
- Program Interrupt:
  Permits interrupt of main computer program for higher priority operations.
- Logical Commands:
  Permit bit-by-bit analysis and/or interpretation of selected portions of words in computer memory.

OPERATING CONTROLS

The model 1604-A control console contains all the indicators and switches required to operate the computer. Projection-type indicators display octal digits of the operational registers, and program address and current instruction (function code and execution address). Three bits of information in each octal digit are translated in the console, and an Arabic numeral 0-7 is projected on the control panel. Immediately below each numeral display are three binary push-button switches, providing the operator with manual input to the registers. A clear button is located at the end of each register display; colored background for numerals (red, green, yellow, and blue) are used to indicate various control conditions. Breakpoint address, selective jump and stop switches are provided.

DESIGN

Control Data's highly qualified and experienced staff of engineers has created the 1604-A system for maximum reliability. Solid-state components are used throughout the 1604-A, and extremely wide tolerances are designed into all circuits.

Maintenance is facilitated by an unusually high degree of standardization and modularization throughout the computer. All circuits are pluggable. The basic bi-level amplifier-inverters are direct-coupled, of printed-circuit construction, and operate at an equivalent clock-rate of five megacycles per second. This circuit is repeated 9000 times in the computer. Approximately 7500 cards are used in a single 1604-A, approximately 900 cards on each of the eight page-frame assemblies.

Only two power supply levels are used throughout: +20v and −20v. Only two logical signal levels are used: −.5v and −.3v. All pluggable cards have eyelet test points for attaching oscilloscopes for tests. Pin-type, trifurcated connectors are used for all cards; back-of-bay wiring to the card connectors is by solderless, crimped AMP taper pins.

1604-A PROGRAMMING SYSTEMS

The machine characteristics of the 1604-A Computer are complemented by a unified and complete set of programming systems. Included are an integrated operating system for processing of programming tasks and special-purpose programs and systems for particular applications. The integrated operating system is the CO-OP MONITOR SYSTEM which was developed jointly with the users group for the 1604-A, CO-OP. Special-purpose programs and systems include PERT, a Linear Programming System, and a General Sort Program.

The 1604-A Users Group, called CO-OP, has developed an extensive library of utility and special function programs for the computer. These programs are immediately available for creation of a library for a particular installation. A current index of the CO-OP library is included following the system description.

CO-OP MONITOR SYSTEM

The CO-OP Monitor for the Control Data 1604-A Computer is a multi-level automatic control system designed to process scientific or business programs with equal efficiency. It consists of the following:

Master Control System – the core of the CO-OP Monitor System. Designed to permit a wide variety of subordinate control systems to run under it and to be adaptable to any equipment configuration attached to a 1604-A Computer. Satellite Computers, such as the Control Data 160-A, may be included in the equipment configuration.

Automatic Job Sequencing – initiates the job to be run and releases control to the specified subordinate control system. Processing from this point is controlled by this subordinate control system. Processing is terminated by the Job Sequencer, or by operator statements from the typewriter.

Operator-System Communication – the Master Control System provides for communication between the operator and the Monitor. Operator-to-Monitor communication is via the "comment from operator" medium. The operator may impose priorities on job processing and may supply programmer-requested information to the system. He may also control the computer environment tables within the computer.

Input/Output Assignment – Logical equipment assignments, made by the programmer on the Monitor control record which accompanies each job, are translated into physical assignments by means of three internal tables. The assignments are made by forming a correspondence between the logical unit numbers requested by the programmer and the equipment listed in an available equipment table.

Central Input/Output Control – All I/O operations are controlled by two routines, READ and WRITE. These routines call on individual subroutines, one for each different type of equipment, listed in the Available Equipment Table. The READ and WRITE routine sets up the transfer of a block of memory locations and initiates the transfer.

Unified Interrupt Control – The interrupt control of the Master Control System deals with the programming complexities which arise as a result of interrupt selection and enables a programmer to utilize the 1604-A interrupt feature with a minimum of effort. Under program control, the programmer may use the interrupt control to detect the occurrence of certain events automatically.

Program and Library Routine Loading–Program and library routines are loaded by the Relocatable Binary Loader. This Loader reads in and relocates subprograms and library routines such as the I/O routines specified in the Running Hardware Table. The library tape is divided into two files. The first contains system information and is written in absolute binary. The second includes all subroutines made up of relocatable binary card images and a directory of routines in BCD format.

FORTRAN-62

The FORTRAN-62 source language processor accepts a language of symbolic algebraic-like statements. The statements have a form similar to normal algebraic notation with additions to control the machine and the compilation of the language.

The FORTRAN-62 language contains several advanced statements which make it more useful and powerful than previous languages. Sharing of *common* data regions by programs and sub-programs has been facilitated by the blocking of these data regions and affixing identifiers to each block. The buffering of data transmissions has been made available to the programmer in a simple and straightforward fashion. The I/O statements have been combined with the operating system to give a much greater flexibility in the use of equipment types, thus allowing specification of equipment at run time.

COBOL

The CODASYL* Committee has sponsored an effort to improve automatic programming techniques for data processing problems. COBOL object programs produced by Control Data are modular at the *paragraph* level. The system is constructed to allow for the many varieties of peripheral equipments available to Control Data users. Automatic I/O buffering is a standard feature of COBOL. The flexible and modular construction of the Control Data system makes the continued development of more powerful techniques for the solution of data processing problems easy.

LINEAR PROGRAMMING SYSTEM

The Control Data Linear Programming Code is called CDM2 for Control Data Mathematical Programming System 2. The code accommodates both straight linear programming problems and separable programming problems. It is based on SCM2 which was developed at Standard Oil of California and which, in turn, was an outgrowth of RSM1 developed at the Rand Corporation.

**Conference on Data Systems Languages*

Recovery Procedures – The Master Control System interprets the recovery key specified by a programmer on the monitor control record. If the program fails in some way whereby the monitor can retain control, recovery procedures will automatically be instigated. The recovery procedures provide the programmer with postmortem dump information on the state of the memory after termination.

Subordinate Control Routines – The Monitor control record prepared by the programmer specified the subordinate control routine to be used in processing this job. When the Master Control System has completed the initialization of the job processing, the subordinate control routine is loaded into memory and control released to it. The subordinate control routine normally supplied with the CO-OP Monitor System is the CO-OP Control System.

Source Language Processors – The source language processors of the CO-OP Monitor System provide the three basic language capabilities for computing tasks: assembly language (CODAP-1), algebraic language (FORTRAN-62), and commercial data processing language (COBOL). These processors operate with the Monitor and produce the relocatable binary format required by the loader.

CODAP-1

The CODAP-1 source language processor accepts a language of symbolic operation codes and addresses. The operation codes contain the full set of 1604-A machine instructions and a set of pseudo instructions for control of the assembly and conversion of data. The input to the assembler may be from any of the I/O equipments . . . with the format of the source language defined in terms of a fixed field card image. Output of the assembler may be a listing of the source and assembled program with a binary copy of the assembled program for later loading and execution. The binary copy may be either fixed or relocatable format, as desired.

PERT

PERT is an abbreviation for Program Evaluation and Review Technique. It is a management tool developed by Booz, Allen, and Hamilton for planning major development projects. Control Data has programmed this technique for the Control Data 1604-A Computer. To use PERT, the project, or a portion thereof, is divided into tasks. These tasks are characterized by events connected by activities. The interrelationships of these fundamental events and activities determine the progress of the project. In summary, the PERT System mechanizes the evaluation of these interrelationships.

1604-A INPUT/OUTPUT EQUIPMENT

STANDARD INPUT/OUTPUT EQUIPMENT

- The Monitoring Typewriter is a modified electric typewriter which monitors information during computer operation. The computer can present typed copy for the operator by buffering data to the typewriter. Or, the operator can use the typewriter keyboard to make computer entries during computation by buffering data into the computer.
- The Control Data 350 Paper Tape Reader reads punched paper tape at the rate of 350 characters per second.
- The Model 110 Teletype Paper Tape Punch provides punched paper tape output at the rate of 110 characters per second.

OPTIONAL INPUT/OUTPUT EQUIPMENT

- The 1610-A Control Unit permits direct communication between the 1604-A and the 088 Collator and 523 Card Punch; a manual switch will permit the 160 or 160-A to use the 1610-A and associated equipment.
- The 1612 Line Printer, offering maximum output of 1000 lines per minute, also contains 120 print positions with 64 characters in each position.
- The 1615 Tape Control Unit controls up to eight 606 Tape Transports from one pair of 1604-A channels.
- The 1617 Card Reader is an on-line peripheral device which photo-electrically reads standard, 80-column punched cards at a rate of 250 cards per minute.

CONTROL DATA SATELLITE COMPUTER SYSTEM

Either the desk-size Control Data 160 or 160-A Computers are an integral part of the Control Data Satellite Computer System. Used with the 1604-A and the 606 Magnetic Tape System, the desk-size computers can be operated either in the on-line or off-line mode under program control. The desk-size computers have access to magnetic tape units and can control punched card equipments, as well as medium- and high-speed printers.

CONTROL DATA 606 MAGNETIC TAPE TRANSPORT

The Control Data 606 Magnetic Tape Transport is a high quality, high performance magnetic tape unit for storage and manipulation of digital information in data processing and computing systems. Maximum reliable operating time, easy programming and control, maximum tape life and the very shortest maintenance time are basic characteristics of 606 operations.

The 606 features complete pneumatic control of the tape. Tape movement is controlled by valving either a vacuum or a pressure to the two synchronously driven fluted capstans which rotate continuously in opposite directions. Vacuum is used to hold the tape to the driving capstan while pressure in the non-driving capstan causes the tape to float over it on a cushion of air. The use of pneumatic capstans eliminates the need for pinch rollers or mechanical clutches and results in smooth uniform tape acceleration with a minimum of tape stress and stretch. The tape is braked smoothly and precisely by a pneumatic brake pad.

Vacuum tape loop boxes are used rather than mechanical tape arms to provide uniform and precisely controlled tape tension. The vacuum column loops are photo-electrically sensed and the signals generated are used to digitally control the DC shunt servos which drive the reels. All other motors used in the 606 are the AC induction type conservatively rated for maximum life. Integrally mounted and direct coupled brakes complete the simple straight forward reel servo system.

The head assembly consists of individual read and write heads, an erase head and pressure pad. The dual gap seven channel head construction provides "read while write" capabilities as well as format compatibility with all major existing tape systems including the IBM 727 and 729 series. Head and tape wear is minimized by use of jets of air to maintain precise contact pressure between the tape and the head gaps. The reliability of the recording is enhanced by the broad band erase head and by precise mechanical and electrical skew compensation. The recording reliability is further improved by two tape cleaners which function during all read and write operations.

The electronics of the 606 are composed of standard computer building block modules that have been tested and field proven in Control Data's computer systems. Included as an integral part of the 606 circuits are complete read-write circuits, skew control, and motion control. All incoming and outgoing data and control information is in digital form.

When used with the Control Data 1604 or 1604-A Computers, the 606 is connected through a Control Data 1615 Tape Control Unit. Up to eight 606 Transports may be connected to one 1615 Control Unit, and the resulting system is program compatible with the Control Data 1607 Magnetic Tape System. The 1615 Control Unit may also be used to operate 606 Transports with the 1604, 1604-A, 160 and 160-A Computers in the Control Data Satellite Computer System.

The Control Data 606 Tape Transport is designed for full computer control and requires no programmed delays. Local control of off-line operations and

tape load and unload procedures is provided by a bank of operator keys and status indicators. Tape changing is simplified by straight line threading and the use of leaderless tape which requires but a single wrap on the take-up reel. Industry and system compatibility is maintained by use of 10½ inch reels and IBM standard EOT and BOT-load point reflective spot sensing.

A major goal in the design of the 606 was to achieve a high degree of performance with an absolute minimum of service. A second design goal was to make certain that any required maintenance could be performed as simply and quickly as possible.

Methods used to achieve these goals are the use of a design that eliminates most electrical and mechanical adjustments and the cooling of solid state components by placing them directly in the path of a blast of cooling air. Quick maintenance by the replacement of major components is facilitated by the use of pluggable modules and sub-assemblies. Convenient access to all components is made possible by careful attention to their placement and by the use of snap off skins and hinged panels.

In multiple unit installations, off-line maintenance is facilitated by a single unit design philosophy which eliminates shared components and composite cabinets. The independent construction permits each 606 to be removed from the line for testing and maintenance without affecting operation of other units.

Careful manufacturing coupled with a rigid quality assurance program guarantees the reliability inherent in the engineering design of the 606. The final production step is a full operational check-out with a Control Data 160-A Computer. This extra step assures the highest level performance of the 606 Magnetic Tape Transport.

SPECIFICATIONS

RECORDING FORMAT

Method – NRZ (non-return to zero – change on ones)

Seven Track Recording
- Data – 6 bits
- Parity – 1 bit

Inter-Record Gap – ¾ inch

Tape Markers
- End-of-Tape & Load Point reflective spot

Compatible with IBM 727 and 729-I, II, III & IV Tape Units

TAPE

Width – ½ inch

Length – 2400 feet with 1½ mil base Mylar tape

Reels – 10½ inch, IBM hub with file-protect ring

TAPE SPEED

Read/Write – 150 inches per second

Reverse Movement – 150 inches per second

Rewind and Unload – 225 inches per second

Start time – 4 millisec. max.

Stop time – 4 millisec. max.

RECORDING DENSITY

High – 556 frames per inch

Low – 200 frames per inch

CHARACTER RATE

83,400 per sec. @ High Density

30,000 per sec. @ Low Density

HEADS

Physical Spacing: (forward direction)
- Erase gap to write gap – 7/16 inches
- Write gap to read gap – 0.300 inches

PANEL

Operator Controls with Indicators
- Power
- Forward
- Reverse
- Unload
- Unit No. Selector
- Load Point
- Hi-Lo Density
- Ready
- Clear

Operation Indicators Only
- Read
- Write
- Fault
- File Protect

PHYSICAL

Size: Height – 72 inches
Depth – 33 inches
Width – 28 inches

Weight – 800 pounds

Power – 115v, 60 cycle, 3KW

Specifications subject to change without notice.

REPERTOIRE OF 1604-A INSTRUCTIONS

INPUT-OUTPUT

Operation	Average Execution Time μs
Input transfer	4.0 + 4.8r**
Output transfer	4.0 + 4.8r
External Function	6.4
Select External Equipment	
Activate Buffer Channel #1	
Activate Buffer Channel #2	
Activate Buffer Channel #3	
Activate Buffer Channel #4	
Activate Buffer Channel #5	
Activate Buffer Channel #6	
Sense External Condition	

ARITHMETIC

Increase Accumulator	3.0
Add	7.2
Subtract	7.2
Multiply Integer	25.2 + .8n#
Divide Integer	65.2
Multiply Fractional	25.2 + .8n
Divide Fractional	65.2
Floating Add	18.8
Floating Subtract	18.8
Floating Multiply	36.0
Floating Divide	56.0
Replace Add	13.2
Replace Subtract	13.2
Replace Add One	13.2
Replace Subtract One	13.2

SHIFT

Accumulator Right Shift	2.8 + .4s##
Q Register Right Shift	2.8 + .4s
AQ Right Shift	2.8 + .4s
A Left Shift	2.8 + .4s
Q Left Shift	2.8 + .4s
AQ Left Shift	2.8 + .4s
Scale **A**	2.8 + .4s
Scale **AQ**	2.8 + .4s

TRANSMISSIVE

Operation	Average Execution Time μs
Enter **Q**	3.0
Enter **A**	3.0
Load **A**	7.2
Load **A**, Complement	7.2
Load **Q**	7.2
Store **A**	7.2
Store **Q**	7.2
Substitute Address (upper)	7.2
Substitute Address (lower)	7.2
Storage Skip	8.8
Storage Shift	12.8
Selective Set	7.2
Selective Clear	7.2
Selective Complement	7.2
Selective Substitute	7.4
Load Logical	7.4
Add Logical	7.4
Subtract Logical	7.4
Store Logical	7.2

SEARCH

Equality Search	4.0 + 3.6r
Threshold Search	4.0 + 3.6r
Masked Equality	4.0 + 3.6r
Masked Threshold	4.0 + 3.6r

INDEXING

Enter Index	3.0
Increase Index	3.0
Load Index (upper)	7.2
Load Index (lower)	7.2
Index Skip	5.6
Index Jump	4.4
Store Index (upper)	7.2
Store Index (lower)	7.2

JUMPS AND STOPS

Operation	Average Execution Time μs
A Jump	
Jump if **A** is zero	4.0
Jump if **A** is not zero	
Jump if **A** is positive	
Jump if **A** is negative	
Return Jump if **A** is zero	7.2
Return Jump if **A** is not zero	
Return Jump if **A** is positive	
Return Jump if **A** is negative	

JUMPS AND STOPS

Operation	Average Execution Time μs
Q Jump	
Jump if **Q** is zero	4.0
Jump if **Q** is not zero	
Jump if **Q** is positive	
Jump if **Q** is negative	
Return Jump if **Q** is zero	7.2
Return Jump if **Q** is not zero	
Return Jump if **Q** is positive	
Return Jump if **Q** is negative	
Selective Jump	
Jump unconditionally	4.0
Jump if Lever Key #1 Is Set	
Jump if Lever Key #2 Is Set	
Jump if Lever Key #3 Is Set	
Return Jump Unconditionally	7.2
Return Jump if Lever Key #1 Is Set	
Return Jump if Lever Key #2 Is Set	
Return Jump if Lever Key #3 Is Set	
Selective Stop	
Stop Unconditionally (normal jump)	4.0
Stop if Lever Key #1 Is Set (normal jump)	
Stop if Lever Key #2 Is Set (normal jump)	
Stop if Lever Key #3 Is Set (normal jump)	
Stop Unconditionally (return jump)	7.2
Stop if Lever Key #1 Is Set (return jump)	
Stop if Lever Key #2 Is Set (return jump)	
Stop if Lever Key #3 Is Set (return jump)	

* b – B-Box designator or indirect addressing

** r – number of repeated executions

† j – Condition designator (jump & EF sub-instructions)

n – number of one's in multiplier

s – number of positions shifted

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