CHAPTER 3 MODULES

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Before applying the views of computer systems, technology, packaging, and manufacturing, expressed in the previous chapters to the DEC computers discussed in the following chapters, a brief review of printed circuit module technology is in order. Module technology is important because modules were DEC's first products, and because the progress in semiconductor technology that has formed the major element of the technology push driving the computer industry is evident in module technology in a scale convenient for close examination and understanding.

The first modules produced by DEC were called "Digital Laboratory Modules" and were intended to sit on an engineer's work bench and be interconnected with simple cords equipped with banana plugs. As shown in Figure 1, the modules were mounted in aluminum cases 1-3/4 by 4-1/2 by 7 inches in size, and all of the logical signals were brought out to the front of the case, where they appeared on miniature banana jacks mounted in a schematic diagram of the logical function performed by the module. The modules were offered in three speed ranges with compatible signal levels. The three speed ranges were 500 KHz, 5 MHz, and 10 MHz.

The Digital Laboratory Module product line was supplemented by the Digital Systems Modules. These modules, samples of which are shown in Figure 2, were

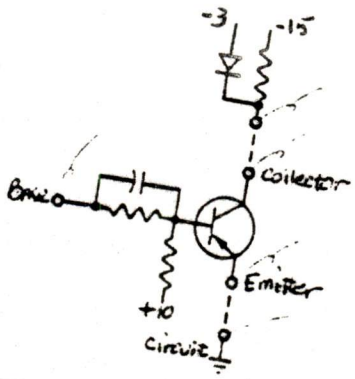
identical to the Laboratory Modules in circuitry, signal levels, and speed range, but had a different packaging scheme. The System Module packaging was designed for rack mounting and used 22-pin Amphenol connectors at the backs of the modules rather than banana plugs at the front. The System Module mounting method was chosen for the PDP-1 computer.

The circuits used in both module series were based on the M.I.T. Lincoln Laboratory TX-2 computer circuits. All of the TX-2 basic circuits were used, except those gates which used emitter followers. The emitter follower gates were not short circuit proof, and it was felt that misplaced patch cords in Laboratory Module configurations or slipping scope probes in System Module configurations would cause a high fatality rate for those circuits.

A brief review of some of the circuits follows to indicate how much present day logic design differs from logic design of twenty years ago. Today designers deal with ALUs and microprocessors as units, whereas twenty years ago, single gates were units.

In the early module designs, most logical operations were performed using saturating PNP germanium transistors, as described in Chapter 3. While the use of transistors in radios and television sets relies on the linear relationship between base current and emitter/collector current to provide the amplification of radio frequency and audio frequency signals, the use of transistors in computer circuits (except those using ECL) relies primarily on the behavior of transistors in either the saturated state or the cut-off state. The use of transistors in such circuits can best be appreciated from the simple example shown in Figure 3.

Figure 3 is a schematic of an inverter. If the base lead is brought to a sufficiently negative voltage, the resulting base current will saturate the transistor, effectively connecting the emitter to the collector. If, on the other hand, the base is grounded, no base current flows, no emitter/collector current will flow, and the transistor will be in the cut-off state. The collector would then assume the voltage of the negative voltage source, were it not for the "clamp diode" which limits the voltage of the collector to -3 volts.



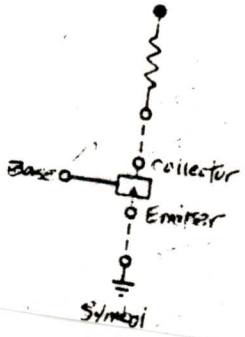


FIG. 3

Inverter (Schematic)

FIG. 4

Inverter (Symbolic)

To simplify the logic drawings, a symbolic drawing like that in Figure 4, was customarily used to represent this circuit. Note that neither Figure 3 nor Figure 4 shows the emitter directly connected to ground or the collector directly connected to the negative supply. Rather, a dotted line is shown. This is because Laboratory Modules and System Modules often used a series connection of up to three inverter gates between the negative supply and ground to accomplish various logical functions. This practice would seem strange by today's standards because today's transistors use silicon and each saturated transistor has a 0.7 volt voltage drop across it. In Laboratory Modules and System Modules, germanium transistors were used, and these had only about a 0.1 volt voltage drop.

The Digital Laboratory Modules and the Digital System Modules used a dual polarity logic system employing both levels and pulses. The logical voltage levels were -3 volts and ground. Correspondence between the logic state, ONE or ZERO, and the voltage levels of -3 and ground were indicated at each point in the logic diagram by a diamond. The diamond defined the necessary voltage level for the action desired. A solid diamond denoted that a -3 volt level was an assertion , and a hollow diamond indicated that a ground level was an assertion.

Series arrangements of inverters, while useful, were not sufficient to provide all logical functions. A more general arrangement was to add diodes to the circuit of Figure 3 to form NAND gate or NOR gates, as shown in Figures 5 and 6.

Figs 5 & 6 to be supplied.

Except for very small amounts of delay, the inputs and outputs of these circuits changed simultaneously, thus no information was stored. The storage of information was accomplished by bi-stable devices called "flip-flops" whose state was controlled by the application of pulses. Before discussing the construction of flip-flops, therefore, it is necessary to briefly describe the generation of pulses.

Pulses, which were used both in NAND/NOR circuits like those in Figures 5 and 6 and for controlling flip-flops, were generated by pulse amplifiers. Pulse amplifiers were very powerful logical elements because they not only amplified and standardized the shapes of pulses, but they also gated pulses. This latter feature meant that when the same logical gating was to be done on a whole register of flip-flops, it could often be done once, at the pulse amplifier which drove the register. The pulse amplifier would typically be arranged to operate in response to a pulse or level change and produce an output via a pulse transformer. The pulse transformer had both terminals of its secondary winding available so that either positive or negative pulses could be obtained depending upon which terminal was grounded. A negative pulse (ground to -3 volts and back to ground) was represented in the logic drawings by a solid triangle, and a positive pulse (-3 volts to ground and back to -3 volts) was represented by a hollow triangle.

The use of pulses is emphasized a great deal in the following discussion because the concept of gating a pulse at the source and using the gated pulse to transfer data from register to register on a parallel basis used an absolute minimum of logic. This method was referred to as "East Coast" logic, while "West Coast" logic used gating at each bit position to do parallel

tranfers. These distinctions seem strange in the 1970's when gates are much cheaper than "a dime a dozen", but in the late 1950's and early 1960's much of computer design involved this level of component reduction ingenuity.

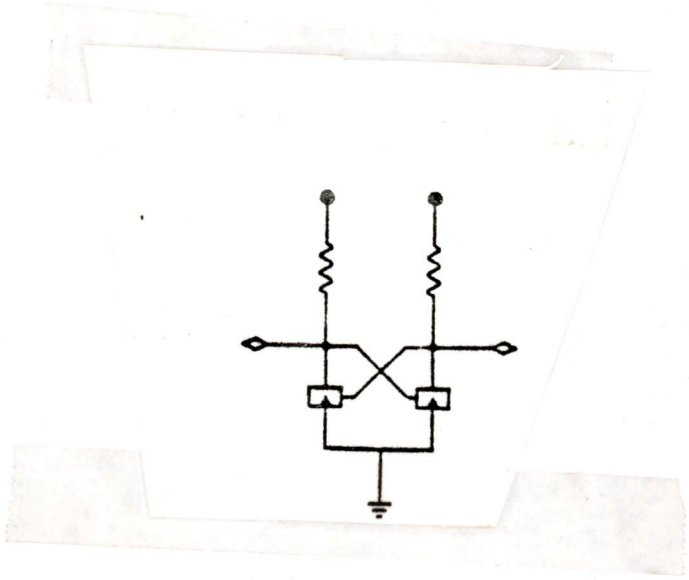


FIG. 7

Basic Flip-Flop

Returning to the discussion of gates and flip-flops, a primative flip-flop can be obtained by interconnecting two grounded emitter inverters as shown in Figure 7. When one inverter is cut-off, its output is negative. This holds the

other inverter on, which in turn holds the first inverter off. If an additional inverter circuit is added to the circuit of Figure 7, the circuit of Figure 8 is obtained. The application of a negative pulse to the input of the additional inverter changes the state of the flip-flop. In the actual implementations of DEC Laboratory Module flip-flops, buffer amplifiers were added to the outputs to permit a single flip-flop to drive the inputs of many other gates. The buffer amplifiers also provided delays at the outputs of the flip-flops such that the output did not change until after the activating pulse was over. This permitted the state of the flip-flop to be sensed while the flip-flop was being pulsed, a necessary feature for the simple implementation of shift registers, counters, and adders.

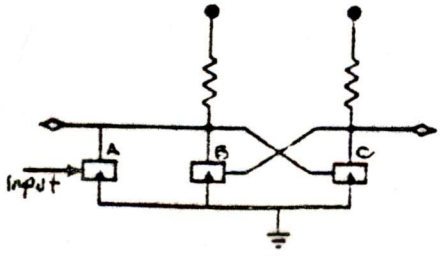


FIG. 8

Flip-Flop @ Inverter

Collections of the inverters, gates, and flip-flops just described were packaged in appropriate quantities (i.e. as many as would fit within the size and pin contraints) and sold as Laboratory Modules and System Modules. There were a relatively small number of module types available in the Laboratory Module Series. For example, in the first product line, the 100 Series:

103	6 Inverters
110	2 6-input negative diode NOR's
201	1 buffered flip-flop
302	1 one-shot
402	1 clock pulse generator
406	1 crystal clock
410	1 Schmitt trigger circuit pulse generator
501	3 level standardizers
602	2 pulse amplifiers
650	1 tube pulser (15 volt 100 nanosecond pulses)
667	4 level amplifiers (0 to -15 volts)
801	1 relay

By contrast, there were many System Module types developed. With their higher packing density, lower cost, and fixed backplane wiring, they were used for computers, memory testers, and other complex systems of logic.

It is interesting to note that a large percentage of the modules on the above list were used for the generation and conditioning of the pulses and levels used in the relatively small number of logic circuits. Reference to a present day IC catalog would reveal very few pulsing and clocking circuits and a great many logic circuits. The emphasis on pulses was one of economy, as noted previously.

In 1960 DEC began building modules with slightly different circuitry than that described above. While transistor inverters, buffered delayed flip-flops, and their associated pulse logic were the best choice for 5 and 10 MHz logic, C-D (capacitor-diode) gates and unbuffered flip-flops were found preferable for

low speed logic because greater logic density and lower cost could be achieved.

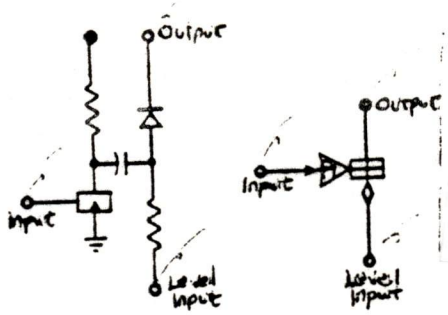


FIG. 9
NEGATIVE C-D GATE

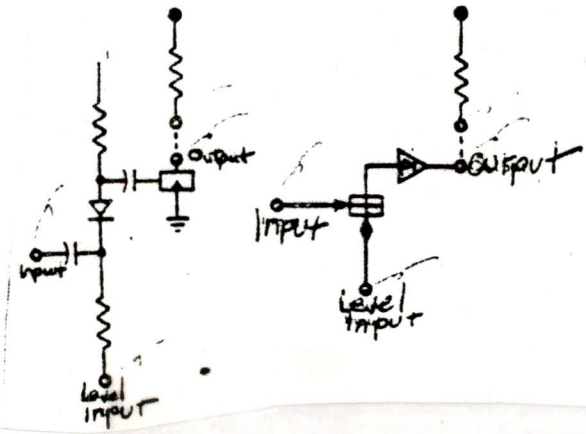


FIG. 10
POSITIVE C-D GATE

A negative capacitor-diode gate is illustrated in Figure 9. With both the level input and the pulse input at ground for sufficent time to allow the capacitor charge to reach three volts, a negative level change or a negative pulse at the pulse input will cause a positive pulse to appear at the output. Such gates could drive the direct set input of any flip-flop which required a positive pulse, and were built into some unbuffered flip-flop inputs to be used for shifting and counting.

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~~The significant aspect of the losic was that~~

It was quite easy to go from ~~basic losi~~ resister transfer level structures to the ~~lo~~ logical diagrams using the ~~initial~~ systems modules. ~~The If we~~

~~Assuming there is a basic A~~ In the PDP-1, the Accumulator was the basic ~~struc~~ register in which all arithmetic re operations were carried out; ~~tosether with~~ operands ~~that~~ eminated from memory and ~~were~~ held in the Memory ~~Buffer~~ Buffer register, MB.

~~Fisure __shows a simp the simplified and del detailed~~

Figure 8.1 shows the interconnection of ~~the~~ two resisters ~~both~~ in simplified form and with all the resister transfer commands that could be given by the control section ~~of the computer s which effe effect operations on the resisters (in this case just the AC).~~

~~Note, there are 5 basic five five operations can be carried out on the accumulator (the there were~~

Figure 8.2 shows the logic diagram for 1 bit of the accumulator and MB for the operations given in the resister transfer diagram.. The ~~first~~ operation to clear the AC is carried out by just ~~pulsing~~ connecting a pulse amplifer to all 18 bits of the a AC ~~, and.~~ Complementing the AC is carried out ~~by connecting a transistor to sround connecenting a~~ transitor at one of the complementing the inputs, ~~and shorti emitting~~ a negative pulse. Addition is done ~~by~~ a two step processs: fist, the MB and AC is ~~given~~ half added to the AC usins the exclusive or operation where, the AC is complemented if the corresponding MB bit is a one; second, the carry operation is given. ~~Carry is slishtlyl more complex and consists~~

A carry at a given bit position is initiated if the ~~AC is 0 (it had been a 1 and~~ MB is 1 and the AC is 0 (corresponding on to an initial condition of two 1s before the half add. Once a carry is started ~~and eminates from the carry propsate line, pc, flip flops carry propsate signal, P2 P,~~ a carry will continue to propsate if each bit of the AC is a 1. ~~In this way, a~~

In a simlar way, a one can be added to the accumulator by simply pulsing the least signifcant digit of the AC and having it propsate along all the digits that are one, complemnting ~~the~~ each digity of the AC as ~~propsates for~~ from digit to digit.

Here, the relation ship between a one is emitted pulse is emitted from the carry proposste line, p2, if a o pulse is inserted into the carry propste input, c2.

A positive capacitor-diode gate is illustrated in Figure 10. With the level input at -3 and the capacitor input at ground for a sufficient time to allow the charge on the capacitor to become stable, a negative level change or a negative pulse at the capacitor input will cause the transistor to conduct, grounding the output for an amount of time determined by the gate time constant or the input pulse width, whichever is shorter. Gates of this type were not cross-coupled to form flip-flops, but could be used to set and clear unbuffered flip-flops by momentarily grounding the correct flip-flop outputs in a fashion similar to the inverter gate that was added to Figure 7 to obtain Figure 8.

The principal advantages of the capacitor-diode gates were:

1) The level input to the gate was used to charge a capacitor and was isolated from the rest of the circuit by a diode. Thus, no DC load was presented to the circuit driving the level input of a C-D gate.

2) The resistor-capacitor time constant of the gate required that the conditioning level be present a certain amount of time before the pulse input occurred. This introduced a delay between the application of a new gate level and the time the gate was conditioned, and allowed the sampling of unbuffered flip-flop outputs at the same time that the flip-flop was being changed.

3) The resistor-capacitor combination differentiated level changes, permitting a level change to create a pulse.

The use of saturating MADT transistors and toroidal pulse transformers appeared to be nearing an operating limit at 10 MHz. The pulses needed to operate the circuits shown in the previous diagrams were 40% of the cycle time of 10 MHz logic, tightly constraining transformer recovery time and making it difficult to design circuits that were not excessively sensitive to repetition rate. Furthermore, gate delays were large enough to prevent some needed logic configurations from propagating within the 100 nanosecond interval implied by the 10 MHz rating.

A major break with previous circuit geometries appeared necessary. The use at IBM of non-saturating logic encouraged an exploration in that direction. The project was called the "VHF Logic" project because operation at 30 MHz or better (the bottom end of the VHF radio band) was the goal.

The complex 30 mHz flip-flops were packaged one to a module, so a great many interconnections were needed to implement logical functions. In systems designed for 30 MHz operation, the use of leads longer than a few centimeters was expected to require special care, hence the availability of a satisfactory transmission line hookup medium was felt to be an essential element for ease of use. A new solid wall coaxial cable had just been introduce, the 50 ohm impedance version of which was chosen to hook up the VHF modules. It appeared to have a strong enough center conductor for practical hookup between modules while not being too bulky for easy hand bending.

Due to the low impedance needed for the coaxial cable connections, substantial driving current was necessary to achieve adequately high signal voltages, and hence considerable power had to be dissipated. The ability to

drive a load at any point along the transmission line was deemed necessary for practical hookup, and 3 volt swings had to be available for compatibility with existing modules. These needs were met by choosing a 60 milliampere output current, producing a 1.5 volt swing on a double-terminated 50 ohm line and a 3 volt swing with a 50 ohm load when interfacing to existing slower logic. These voltage and current levels required the addition of heat sinks to the output transistors. This was accomplished by installing spring clips that fastened the cases of the transistors directly to the connector pins, exploiting the connectors as heatsinks and at the same time providing a minimum inductance connection from the transistor collector (common to the case) out of the module.

The VHF modules contained a novel delay line implementation which has reappeared in recent days in the ECL boards of the KL10 processor. Flip-flop feedback delay was provided by a 10 nanosecond stripline etched onto the printed circuit board. A meander pattern was selected with a degree of local coupling between the loops to achieve a seven to one delay to risetime ratio. Both the delayed and undelayed ends of this 50 ohm stripline were made available at the module pins. The undelayed outputs switched simultaneaously with the flip-flop outputs, allowing a subsequent gate to subtract a delayed flip-flop output from the undelayed complement output side of the flip-flop and produce a 10 nanosecond pulse when the flip-flop changed state.

The performance of the VHF modules was rated at 30 HMz, which was the limit of the module testers used on the production floor. Bench testing demonstrated 40 MHz capability with the promise of 50 MHz performance if adequate testing apparatus could be found. Risetimes were better than 1.

Modules delivered to customers were used to build satisfactory high performance systems, but the need for such high performance was not widespread. In addition, the product development cycle was by the standards of the time quite long (two years) and the enthusiasm for the VHF modules amongst the DEC engineers flagged, further attenuating product momentum. Despite their failure as a product, the VHF modules eventually made a contribution to computer progress. To produce timesharing systems, the PDP-6 needed a way of comparing relocated addresses at very high speed. A high speed register comparator was quickly designed using current mode logic similar to the VHF modules.

As a series of general purpose products for engineers to use, the cost of the VHF modules and the inconvenience of their wiring was too great. Further developments in general purpose logic modules were to lie in the opposite direction: cheaper, more compact, easier to use, and slower.

By 1964 the decreasing cost of semiconductors during the early 60's had caused the cost of System Module mounting hardware to become a significant portion of the total module cost. In response to this trend, a new type of module was developed which was a 2.5 by 5 inch printed circuit card with a color coded plastic handle. The printed circuit card provided its own mechanical support - there was no metal frame around it as there had been in the System Module design. The new modules, called Flip-Chip modules, plugged into connector blocks that could support eight such modules.

The first series of the new modules was designated the "R-Series" and was identified by using red handles. The R-Series circuits were a reaction to the

rather complicated set of usage rules developed for the previous products. The goal was to make these easy to use and inexpensive . Integrated circuits were not used because they were more expensive than discrete components and the computer industry had not yet decided on the type of integrated circuit to use. The building block for R-Series logic was the diode gate, a sample of which is shown in Figure 11. The other basic circuit was the DCD (diode-capacitor-diode) circuit shown in Figure 12. The DCD gate was used to provide standardized levels to active devices such as flip-flops and to produce the logical delay necessary to sense and change flip-flops at the same time.

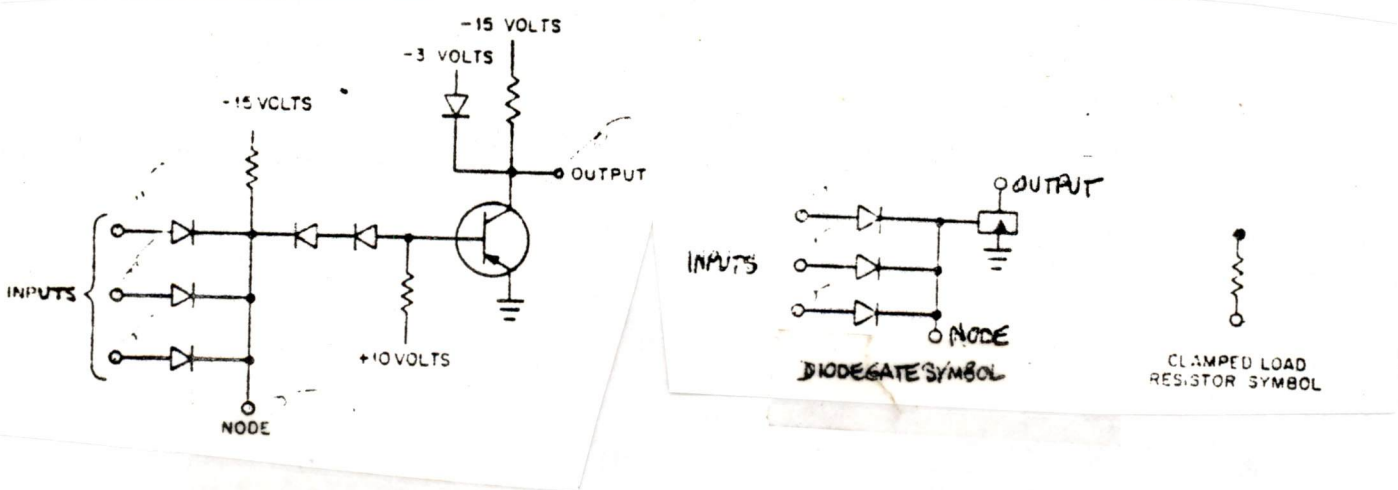

FIG. 11
DIODE GATE

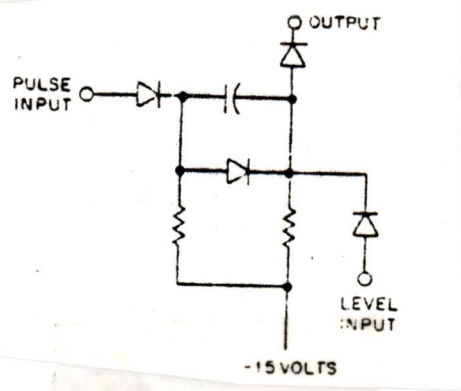

FIG. 12
DCD GATE

A second series of the new modules was developed for the first PDP-8s. This series was called the S-Series, although it also had red handles. The S-Series modules used the same circuits as their R-Series counterparts, but with variations to the values of the load resistors and DCD gate storage capacitors to obtain greater speed.

The B-Series with blue handles was essentially the same as the 6000 series of 10 MHz System Modules, but repackaged on the new 2.5 inch by 5 inch cards, and used silicon transistors rather than germanium transistors. The new silicon transistors were a mixed blessing. While they had temperature sensitivity characteristics superior to those of the germanium transistors, and their voltage drop characteristics permitted the elimination of the bias resistor to +10 volts, they did not saturate as well as the germanium transistors. Because they did not saturate well, the voltage between the collector and the emitter in the saturated state was not as low as it was with germanium transistors. This meant that the series arrangement of three inverters discussed in conjunction with the dotted lines in Figure 4 could not be used. Instead, only two of the silicon transistor inverters could be connected in series if the output was intended to drive another inverter. The first computer to use the B-Series modules was the PDP-7.

Analog applications were the target market for the A-Series modules, which had amber handles. This series, still being manufactured today, includes analog multiplexers, operational amplifiers, sample and hold circuits, comparators, digital to analog converters, reference voltage supplies, analog to digital converters, and various accessory modules. The peak development rate for analog modules occurred in 1971 with 38 new types and declined to 5 new types

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in 1977.

While all of the preceding modules had been designed as user-arrangeable building blocks, the green handled G-Series was intended for modules that would only be sold as part of a system. For example, all of the DEC core memory circuits have been in the G-Series because a core memory system is sufficiently complex that a cookbook approach using a standard series of modules is not appropriate. The G-Series is still actively used today for circuits other than logic, generally in peripheral devices such as disks, tapes, and terminals.

Like the A Series and G Series, the W (white handle) Series is still manufactured, and is used to provide intput/output capability between Flip-Chip modules and other devices. Lamp drivers, relay drivers, solenoids drivers, level converters, and switch filters are included in this family, but the only modules used widely today are the W900-W999 modules which include cable termination modules and blank boards upon which the user can mount ICs and wire wrap them together.

While the W-Series provided a variety of interface capabilities, the circuitry used therein was still too fast for typical industrial applications. Computer-oriented logic, by its very nature, is high speed and provides noise immunity far below that required in small-scale industrial control systems located physically close to the process they control.

Unfortunately, industrial electrical noise is not predictable to the nearest order of magnitude. Thus, attempts to solve the problems with "high level

logic" whose voltage thresholds were merely a few times greater than computer-type logic levels did not work well.

A new series of modules, the K-Series (with blac(K) handles), was developed which relied on a combination of voltage, current, and time thresholds to protect storage elements such as flip-flops and timers from false triggering. Since industrial controls typically interact with physically massive equipment, time thresholds are particularly attractive. There are four ways of exploiting these:

1) basic 100 Khz slow-down circuits everywhere
2) optional 5 KHz slow-down circuits available
3) transition-sensitive (edge-detecting) circuits provided with hysteresis to allow additional discrete capacitor loading when all else fails
4) replacement of the conventional monostable multivibrator or "one-shot" circuit by a timing circuit having both a low impedance and hysteresis at the input.

The hardware for the K-Series was specially designed to fit the NEMA (National Electrical Manufacturers Association) enclosures traditionally used with relay implemented industrial controls, but used the same connectors as the other Flip-Chip modules. Sensing and output terminals were provided with screw terminals and indicator lights, and appropriate arrangements were made to interface with 120 VAC devices. Wire wrap terminals were protected from external voltages but were available for oscilloscope probes. Magnetically latched reed relays and diode arrays that could be programmed by snipping out diodes were provided as memory elements that would retain data during power

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failures.

FIG. 13
K-Series Circuit

Gating in early K-Series modules was accomplished with discrete diode-transistor circuits such as that shown in Figure 13. Other K-Series modules used integrated circuits for the logic functions. In these designs the inputs to the ICs were protected with filter/trigger circuits which filtered out the noise and then restored the fast rise-times required by the ICs. Outputs were protected from output-induced noise and converted to standard

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K-Series signals by circuits similar to those used in the discrete logic gates.

Unlike other DEC modules, the K-Series modules were not directly useful for constructing computers or computer-like data processing subsystems due to their low speed and high cost. They did play an important part in bringing digital logic into industrial applications, and the noise protection techniques developed for these modules were useful in the design of the PDP-14 Industrial Controller (Chapter 6).

By 1967 the electronics world had settled on transistor-transistor-logic (TTL) as the technology of choice for integrated circuits and the cost for logic functions implemented in TTL ICs had dropped below that of discrete circuit implementations. With much more logic fitting into the same printed circuit board area, a single Flip-Chip card could now accommodate much more complicated functions. However, there were not enough connector pins available to get the necessary signals on and off the card. The answer to the problem was to keep the cards the same size, but to have etch and associated contacts on both sides of the printed circuit board. This increased the number of contacts from 18 to 36, and a new series with magenta handles (M-Series) was born. Subsequently, some G-Series and W-Series modules were also designed with ICs and double sided boards.

The advent of TTL brought the first power supply and signal level change in DEC's history. The -15 volt and +10 volt supplies were no longer required. Only a single +5 volt supply was needed to supply the logic signals which were now 0 and +3 volts. The packaging was kept consistant, however, as the old

single-sided modules could be plugged into the new connector blocks, and careful attention to pinning arrangements allowed double-sided module to be used in a single sided block at a sacrifice of some circuits.

The basic TTL circuit is the NAND gate shown in Figure 14.

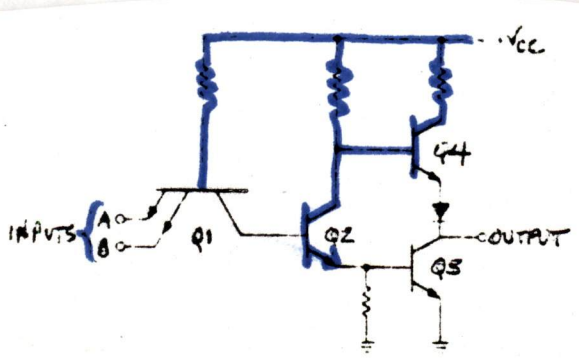

FIG. 14 TTL NAND Circuit

The input of the TTL gate is a multiple emitter transistor. If either input is

at or near ground (0 to 0.8 volts), Q1 becomes saturated, bringing the base voltage of Q2 low, turning off Q3 and turning on Q4 making the output high (+2.4 to +3.6 volts). If both inputs are high (above 2.0 Volts), Q2 has base current supplied to it through the collector diode of Q1, turning Q2 on. This in turn provides base current to Q3, saturating it and cutting off Q4, making the output low (0 to 0.4 volts).

Like the transistor inverter circuits discussed in conjunctuion with System Modules, TTL NAND gates can be cross-connected to form flip-flops.

The first generation of M-Series modules were used in a redesign of the PDP-8 called the PDP-8/I. The circuits used in these modules used TTL integrated circuits which were called "7400 series" integrated circuits because of a growing tendency in the semiconductor industry to standardize part numbers for TTL circuits, calling a package of 4 NAND gates a 7400, a package of six inverters a 7404, etc. The KI10 processor used in the PDP-10 was designed from higher speed circuits using the 74H00 series of TTL integrated circuits. The 74H00 circuits were similar to the earlier 74 series, but were faster and used much more power. The first PDP-11 (the PDP-11/20) used both 7400 and 74H00 series ICs, as did the PDP-8/E. Both of these latter machines used 8.5 inch by 10.4 inch "extended quad" modules.

In 1970 an M-Series 18-bit machine, the PDP-15, was constructed. It was the last of a generation which started with the PDP-1 (System Modules), and grew through the PDP-7 and PDP-9 (B-Series modules). The PDP-15 and the PDP-11/45 used Schottky TTL, a circuitry with such rapid switching speeds that four-layer boards had to be used such that the inner layers of power and

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ground etch could provide shielding.

In 1972 work began on a new PDP-10 processor, the KL10. This used ECL current switching non-saturating logic from several vendors including the MECL (Motorola Emitter Coupled Logic) 10,000 series. This line of circuits is in some ways an integrated circuit version of the VHF modules. The basic gate is shown in Figure 15.

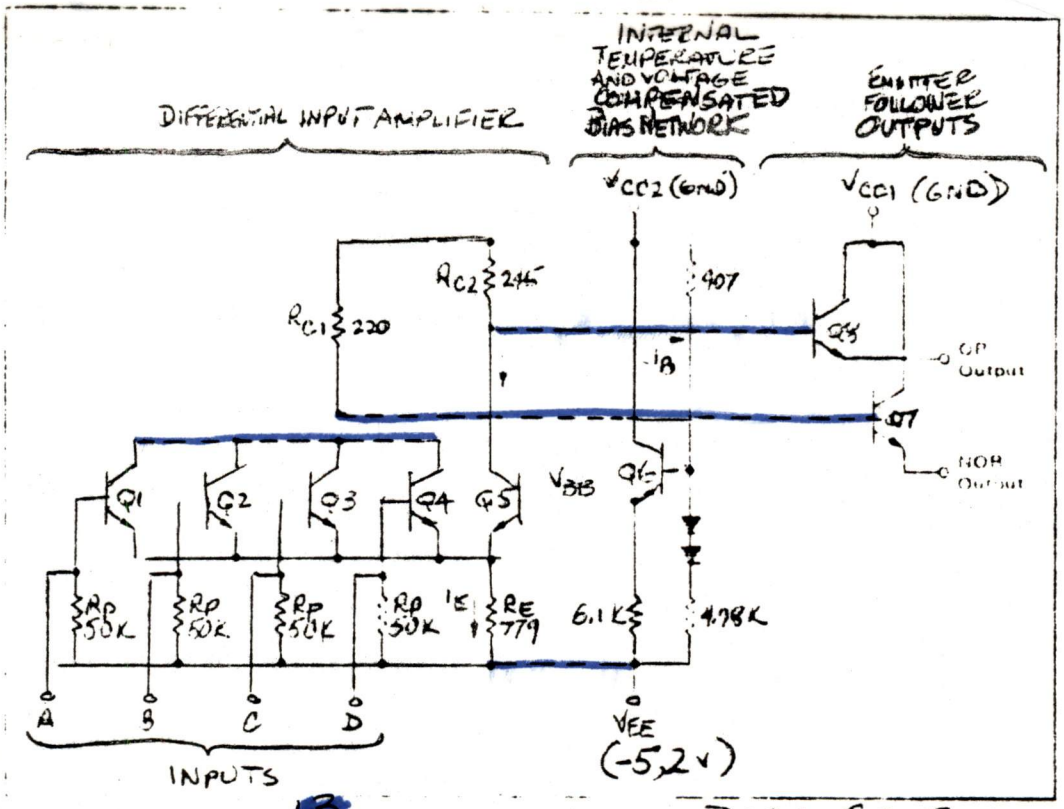


FIG. ~~13~~ 15 MECL, 10,000 BASIC GATE

Q6 has a temperature compensated internally generated reference voltage on its base of -1.3 volts. The outputs drive 50 ohm terrminated transmission lines returned to -2 volts. There is a complementary pair of outputs so that the circuit is both an OR and a NOR gate. At 25 degrees Celsius the upper level will between -0.81 and -0.96 volts, while the lower level will be between -1.65 and -1.85 volts. The circuits, like the Schottky circuits, are so fast that multi-layer boards are required. In addition, a great deal of care in signal line termination is required. As with the previous logic families studied, flip-flops can be created. The ECL master-slave flip-flops are quite complex, requiring 32 transistors and 7 diodes.

As the various module circuit technologies developed, not only could more logic functionality fit in a given space, but also the space provided on individual logic modules was increased. By 1973, the "hex" module (8.5 by 15.6 inches) was widely used, principally in the PDP-11 family. By 1977, DEC computers were using 12 by 15.6 inch "extended hex" modules.

An evolution in circuits has continued as the technology has changed. As integrated circuits have become more powerful by the reduction of the size of their active elements, each new computer introduced is smaller, faster, and generally lower cost than its predecessor. While only DEC examples have been mentioned here, the trend toward smaller, faster, and less costly computers has been true across all of the computer manufacturers.

The chart below shows the number of module types that were started each year from 1957 through 1977.

Figures:

John I've added photos.

4

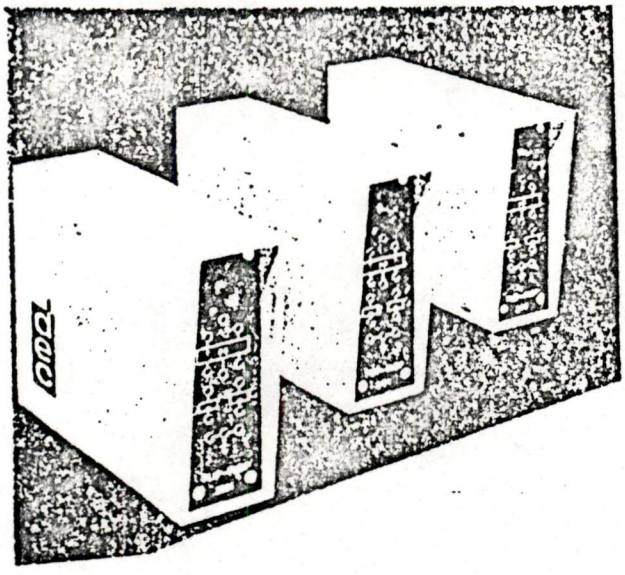
CHAPTER 4 MODULES

Dick Best, Russ Doane, John McNamara

Before applying the views of computer systems, technology, packaging, and manufacturing, expressed in the previous chapters to the DEC computers discussed in the following chapters, a brief review of printed circuit module technology is in order. Module technology is important because modules were DEC's first products, and because the progress in semiconductor technology that has formed the major element of the technology push driving the computer industry is evident in module technology in a scale convenient for close examination and understanding.

The first modules produced by DEC were called "Digital Laboratory Modules" and were intended to sit on an engineer's work bench and be interconnected with simple cords equipped with banana plugs. ~~As shown in Figure 1, the modules were mounted in~~ a aluminum cases 1-3/4 by 4-1/2 by 7 inches ~~in size, and all of~~ the logical signals ~~were~~ brought ~~out~~ to the front of the case, where they appeared on miniature banana jacks mounted in a schematic diagram of the logical function performed by the module. The modules were offered in ~~three speed ranges with compatible signal levels. The three speed ranges were~~ 500 KHz, 5 MHz, and 10 MHz.

The Digital Laboratory Module product line was supplemented by the Digital Systems Modules. These modules, samples of which are shown in Figure 2, were



Need photo in a rack and ~~not~~ go patched.

fig 1 DIGITAL LABORATORY MODULES

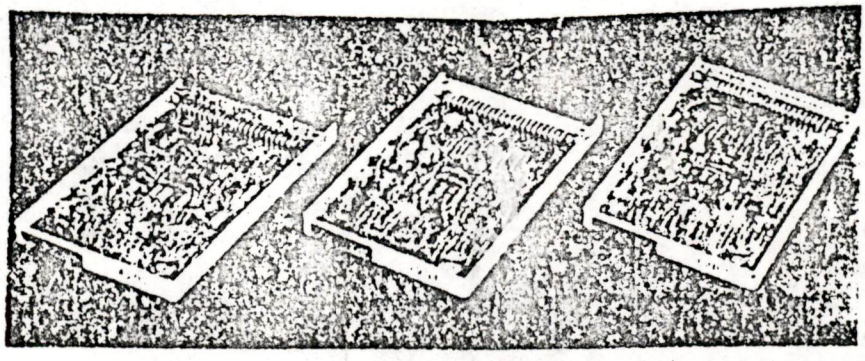


fig 2 DIGITAL SYSTEM MODULES

FIGURE 1 – LABORATORY AND SYSTEM MODULES

Identical to the Laboratory Modules in circuitry, signal levels, and speed range, but had a different packaging scheme. The System Module packaging was designed for rack mounting and used the 22-pin Amphenol connectors at the backs of the modules for soldered interconnection, rather than banana plugs at the front. Later mounting panels were available in taper pin interconnection to facilitate wiring. The System Module mounting method was chosen for the PDP-1 computer so that 25 modules could be mounted in a 5 1/4 x 19", wired mounting panel.

The circuits used in both module series were based on the M.I.T. Lincoln Laboratory TX-2 computer circuits. All of the TX-2 basic circuits were used, except those gates which used emitter followers. The emitter follower gates were not short circuit proof, and it was felt that misplaced patch cords in Laboratory Module configurations or slipping scope probes in System Module configurations would cause a high fatality rate for those circuits.

A brief review of some of the circuits follows to indicate how much present day logic design differs from logic design of twenty years ago. Today designers deal with ALUs and microprocessors as units, whereas twenty years ago, single gates, arithmetic logic units (ALUs), registers, and individual flip flops were units. In the early 1960s

In the early module designs, most logical operations were performed using saturating PNP germanium transistors, as described in Chapter 3. While the use of transistors in radios and television sets relies on the linear relationship between base current and emitter/collector current to provide the amplification of radio frequency and audio frequency signals, the use of transistors in computer circuits (except those using ECL) relies primarily on the behavior of transistors in either the saturated state or the cut-off state. The use of transistors in such circuits can best be appreciated from the simple example shown in Figure 3.

Figure 3 is a schematic of an inverter. If the base lead is brought to a sufficiently negative voltage, the resulting base current will saturate the transistor, effectively connecting the emitter to the collector. If, on the other hand, the base is grounded, no base current flows, no emitter/collector current will flow, and the transistor will be in the cut-off state. The collector would then assume the voltage of the negative voltage source, were it not for the "clamp diode" which limits the voltage of the collector to -3 volts. The +10 volt bias voltage could be varied for marginal checking following the ~~Lincoln~~ TX-2 circuits of chapter 3. The -3 volt supply was generated on each module using 4 forward biased diodes from the ~~-15~~ ~~basically~~ ~~even~~ relatively poorly regulated -15 supply.

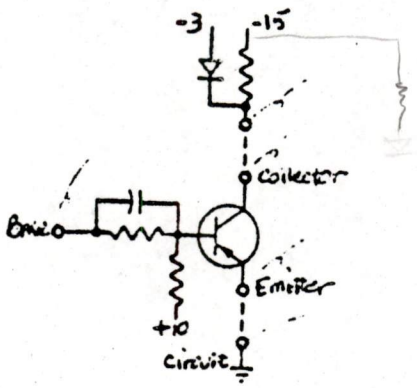


FIG. 3

Inverter (Schematic)

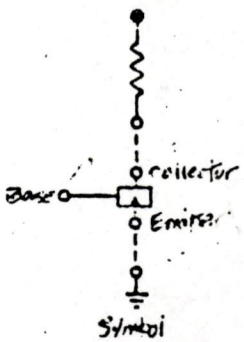


FIG. 4

Inverter (Symbolic)

Except for very small amounts of delay, the inputs and outputs of these circuits changed simultaneously, thus no information was stored. The storage of information was accomplished by bi-stable devices called "flip-flops" whose state was controlled by the application of pulses. Before discussing the construction of flip-flops, therefore, it is necessary to briefly describe the generation of pulses.

[Insert 5.1]

Pulses, which were used both in NAND/NOR circuits like those in Figures 5 and 6 and for controlling flip-flops, were generated by pulse amplifiers. Pulse amplifiers were very powerful logical elements because they not only amplified and standardized the shapes of pulses, but they also gated pulses. This latter feature meant that when the same logical gating was to be done on a whole register of flip-flops, it could often be done once, at the pulse amplifier which drove the register. The pulse amplifier would typically be arranged to operate in response to a pulse or level change and produce an output via a pulse transformer. The pulse transformer had both terminals of its secondary winding available so that either positive or negative pulses could be obtained depending upon which terminal was grounded. A negative pulse (ground to -3 volts and back to ground) was represented in the logic drawings by a solid triangle, and a positive pulse (-3 volts to ground and back to -3 volts) was represented by a hollow triangle.

INSERT A

The use of pulses is emphasized a great deal in the following discussion because the concept of gating a pulse at the source and using the gated pulse to transfer data from register to register on a parallel basis used an absolute minimum of logic. This method was referred to as "East Coast" logic, while "West Coast" logic used gating at each bit position to do parallel

5.1 Pulses were used for the computer clocks and for carrying out the register transfer operations among the registers.

A pulse, as it name implies, was a very well controlled, short event in which a logic signal is asserted. Pulses were generated by pulse amplifiers which were blocking oscillator circuits employing pulse transformers. Insert A from page 5 Pulse amplifiers were important because they produced high energy (high fanout) standard, shaped pulses which could be used to gate a complete 18-bit register as a single, logical signal. Pulse signals were normally distributed on twisted pair wiring and could travel the long distances needed in the early, large sized digital systems (eg. PDP-1), without degradation.

~~Pulse~~ In addition to the use of ~~pulse amplifiers~~ for ~~the clock~~ clocking, pulse amplifiers were significant because logic ~~can be performed~~ at the input determines the condition for causing register transfer operations.

tranfers. These distinctions seem strange in the 1970's when gates are much cheaper than "a dime a dozen", but in the late 1950's and early 1960's much of computer design involved this level of component reduction ingenuity.

~~Logical desig~~

Even recent logical design texts emphasize the need to minimize logic and reduce the number of gates ~~on~~ in a ~~circuit~~ system.

In addition to the DEC logic, clocked sequential circuits and serial Bureau of Standards based logic alternatives, there was a concern about how logic was represented. Two logic design representations were used; "East Coast" logic" was diagramatic and was typified in DEC's logiccal design and register tranfer diagrams; "west Coast Logic" was Boolean equations and time based ~~solely~~ on finite symbolic and algebraic, being difference equations.

where the schematic to physical conversion was rather direct

Gschwind (19__) described the DEC system effectively in his, textbook.

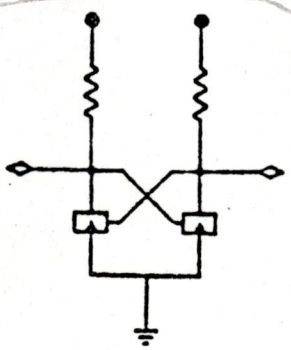
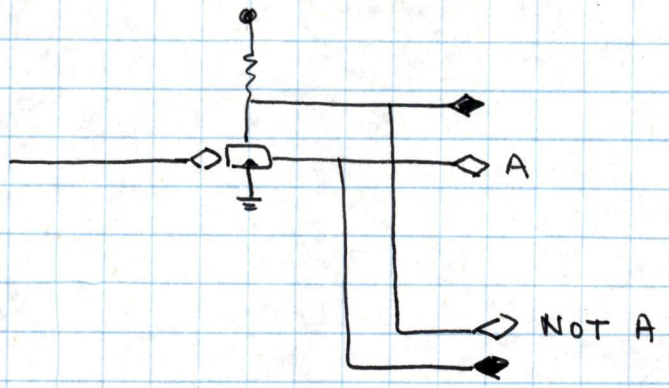


FIG. 7

Basic Flip-Flop

Returning to the discussion of gates and flip-flops, a primative flip-flop can be obtained by interconnecting two grounded emitter inverters as shown in Figure 7. When one inverter is cut-off, its output is negative. This holds the



Logical states and corresponding voltages for DEC dual polarity logic ~~system~~

← Same signal →		← Inverted signal →	
A ◇	¬A ◆	¬A ◇	A ◆
0 (-3)	1 (-3)	1 (0)	0 (0)
1 (0)	0 (0)	0 (-3)	1 (-3)

Fig. 4.1 Signal naming convention and signal levels through inverter (NOT gate) for DEC dual polarity logic ~~system. conventio~~

To simplify the logic drawings, a symbolic drawing like that in Figure 4, was customarily used to represent this circuit. Note that neither Figure 3 nor Figure 4 shows the emitter directly connected to ground or the collector directly connected to the negative supply. Rather, a dotted line is shown. This is because Laboratory Modules and System Modules often used a series connection of up to three inverter gates between the negative supply and ground to accomplish various logical functions. This practice would seem strange by today's standards because today's transistors use silicon and each saturated transistor has a 0.7 volt voltage drop across it. In Laboratory Modules and System Modules, germanium transistors were used, and these had only about a 0.1 volt voltage drop.

The Digital Laboratory Modules and the Digital System Modules used a dual polarity logic system employing both levels and pulses. The logical voltage levels were -3 volts and ground. Correspondence between the logic state, ONE or ZERO, and the voltage levels of -3 and ground were indicated at each point in the logic diagram by a diamond. The diamond defined the necessary voltage level for the action desired. A solid diamond denoted that a -3 volt level was an assertion , and a hollow diamond indicated that a ground level was an assertion.

Series arrangements of inverters, while useful, were not sufficient to provide all logical functions. A more general arrangement was to add diodes to the circuit of Figure 3 to form NAND gate or NOR gates, as shown in Figures 5 and 6.

Figs 5&6 to be supplied.

other inverter conducting, which in turn holds the first inverter off. If an additional inverter circuit is added to the circuit of Figure 7, the circuit of Figure 8 is obtained. The application of a negative pulse to the input of the additional inverter changes the state of the flip-flop. In the actual implementations of DEC Laboratory Module flip-flops, buffer amplifiers were added to the outputs to permit a single flip-flop to drive the inputs of many other gates. The buffer amplifiers also provided delays at the outputs of the flip-flops such that the output did not change until after the activating pulse was over. This permitted the state of the flip-flop to be sensed while the flip-flop was being pulsed, a necessary feature for the simple implementation of shift registers, counters, and adders.

so that B conducts and C will be off

simultaneous data exchange between two registers

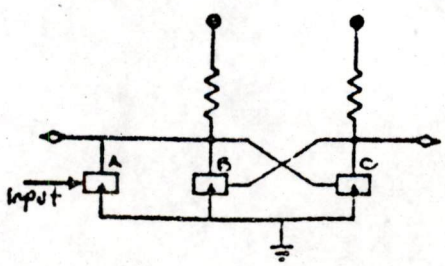


FIG. 8

Flip-Flop @ Inverter

Collections of the inverters, gates, and flip-flops just described were packaged in appropriate quantities (i.e. as many as would fit within the module size and meet the pin contraints) and sold as Laboratory Modules and System Modules. There were a relatively small number of module types available in the Laboratory Module Series. For example, ~~in~~ the first product line, ~~the~~ 100 Series:

103	6 Inverters
110	2 6-input negative diode NOR's
201	1 buffered flip-flop
302	1 one-shot
402	1 clock pulse generator
406	1 crystal clock
410	1 Schmitt trigger circuit pulse generator
501	3 level standardizers
602	2 pulse amplifiers
650	1 tube pulser (15 volt 100 nanosecond pulses)
667	4 level amplifiers (0 to -15 volts)
801	1 relay

By contrast, there were many System Module types developed. With their higher packing density, lower cost, and fixed backplane wiring, they were used for computers, memory testers, and other complex systems of logic.

It is interesting to note that a large percentage of the modules on the above list were used for the generation and conditioning of the pulses and levels used in the relatively small number of logic circuits. Reference to a present day IC catalog would reveal very few pulsing and clocking circuits and a great many logic circuits. The emphasis on pulses was one of economy, as noted previously.

8.1 Invert

In 1960 DEC began building modules with slightly different circuitry than that described above. While transistor inverters, buffered delayed flip-flops, and their associated pulse logic were the best choice for 5 and 10 MHz logic, C-D (capacitor-diode) gates and unbuffered (non-delayed) flip-flops were found preferable for

low speed logic because greater logic density ~~and~~ became lower cost could be achieved.

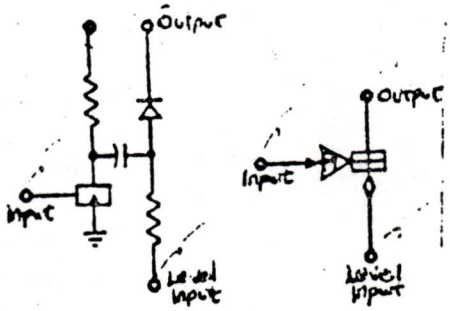


FIG. 9
NEGATIVE C-D GATE

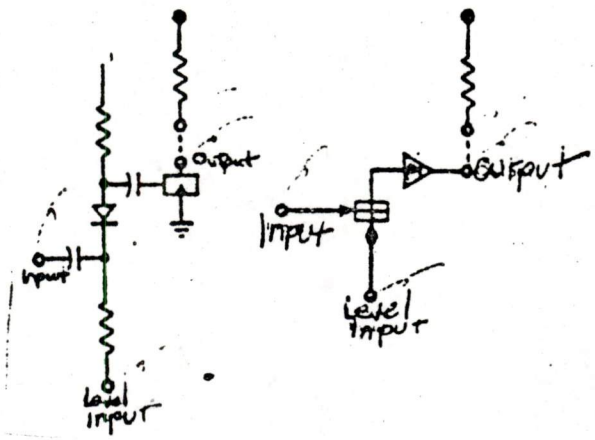


FIG. 10
POSITIVE C-D GATE

A negative capacitor-diode gate is illustrated in Figure 9. With both the level input and the pulse input at ground for sufficent time to allow the capacitor charge to reach three volts, a negative level change or a negative pulse at the pulse input will cause a positive pulse to appear at the output. Such gates could drive the direct set input of any flip-flop which required a positive pulse, and were built into some unbuffered flip-flop inputs so they could be used for shifting and counting. Note, here the ~~charge in the~~ capacitor serves as the delay element ~~used in the earlier buffered flip-flops~~.

A positive capacitor-diode gate is illustrated in Figure 10. With the level input at -3 and the capacitor input at ground for a sufficient time to allow the charge on the capacitor to become stable, a negative level change or a negative pulse at the capacitor input will cause the transistor to conduct, grounding the output for an amount of time determined by the gate time constant or the input pulse width, whichever is shorter. Gates of this type were not cross-coupled to form flip-flops, but could be used to set and clear unbuffered flip-flops by momentarily grounding the correct flip-flop outputs in a fashion similar to the inverter gate that was added to Figure 7 to obtain Figure 8.

The principal advantages of the capacitor-diode gates were:

1) The level input to the gate was used to charge a capacitor and was isolated from the rest of the circuit by a diode. Thus, no DC load was presented to the circuit driving the level input of a C-D gate.

2) The resistor-capacitor time constant of the gate required that the conditioning level be present a certain amount of time before the pulse input occurred. This introduced a delay between the application of a new gate level and the time the gate was conditioned, and allowed the sampling of unbuffered flip-flop outputs at the same time that the flip-flop was being changed.

3) The resistor-capacitor combination differentiated level changes, permitting a level change to create a pulse.

4) ~~The combined system~~ cost was significantly less than with the buffered flip flops.

The use of saturating MADT transistors and toroidal pulse transformers appeared to be nearing an operating limit at 10 MHz. The pulses needed to operate the circuits shown in the previous diagrams were 40% of the cycle time (40 nanoseconds) of 10 MHz logic, tightly constraining transformer recovery time and making it difficult to design circuits that were not excessively sensitive to repetition rate. Furthermore, gate delays were large enough to prevent some needed logic configurations from propagating within the 100 nanosecond interval implied by the 10 MHz rating.

A major break with previous circuit geometries appeared necessary. The use at IBM of non-saturating logic in Stretch encouraged an exploration in that direction. The project was called the "VHF Logic" project because operation at 30 MHz or better (the bottom end of the VHF radio band) was the goal.

The complex 30 mHz flip-flops were packaged one to a module (see Fig 10.1), so a great many interconnections were needed to implement logical functions. In systems designed for 30 MHz operation, the use of leads longer than a few centimeters was expected to require special care, hence the availability of a satisfactory transmission line hookup medium was felt to be an essential element for ease of use. A new solid wall coaxial cable had just been introduce, the 50 ohm impedance version of which was chosen to hook up the VHF modules. It appeared to have a strong enough center conductor for practical hookup between modules while not being too bulky for easy hand bending.

Due to the low impedance needed for the coaxial cable connections, substantial driving current was necessary to achieve adequately high signal voltages, and hence considerable power had to be dissipated. The ability to

drive a load at any point along the transmission line was deemed necessary for practical hookup, and 3 volt swings had to be available for compatibility with existing modules. These needs were met by choosing a 60 milliampere output current, producing a 1.5 volt swing on a double-terminated 50 ohm line and a 3 volt swing with a 50 ohm load when interfacing to existing slower logic. These voltage and current levels required the addition of heat sinks to the output transistors. This was accomplished by installing spring clips that fastened the cases of the transistors directly to the connector pins, exploiting the connectors as heatsinks and at the same time providing a minimum inductance connection from the transistor collector (common to the case) out of the module.

The VHF modules contained a novel delay line implementation which has reappeared in recent days in the ECL boards of the KL10 processor. Flip-flop feedback delay was provided by a 10 nanosecond stripline etched onto the printed circuit board. A meander pattern was selected with a degree of local coupling between the loops to achieve a seven to one delay to risetime ratio. Both the delayed and undelayed ends of this 50 ohm stripline were made available at the module pins. The undelayed outputs switched simultaneaously with the flip-flop outputs, allowing a subsequent gate to subtract a delayed flip-flop output from the undelayed complement output side of the flip-flop and produce a 10 nanosecond pulse when the flip-flop changed state.

The performance of the VHF modules was rated at 30 HMz, which was the limit of the module testers used on the production floor. Bench testing demonstrated 40 MHz capability with the promise of 50 MHz performance if adequate testing apparatus could be found. Risetimes were better than 1. nanosecond ?

Modules delivered to customers were used to build satisfactory high performance systems, but the need for such high performance was not widespread. In addition, the product development cycle was by the standards of the time quite long (two years) and the enthusiasm for the VHF modules amongst the DEC engineers flagged, further attenuating product momentum. Despite their failure as a product, the VHF modules eventually made a contribution to computer progress. To produce timesharing systems, the PDP-6 needed a way of comparing relocated addresses at very high speed. A high speed register comparator was quickly designed using current mode logic similar to the VHF modules.

As a series of general purpose products for engineers to use, the cost of the VHF modules and the inconvenience of their wiring was too great. Further developments in general purpose logic modules were to lie in the opposite direction: cheaper, more compact, easier to use, and slower.

By 1964 the decreasing cost of semiconductors during the early 60's had caused the cost of System Module mounting hardware to become a significant portion of the total cost. In response to this trend, a new type of module was developed which was a 2.5 by 5 inch printed circuit card with a color coded plastic handle. The printed circuit card provided its own mechanical support - there was no metal frame around it as there had been in the System Module design. The new modules, called Flip-Chip modules, plugged into connector blocks that could support eight such modules.

The first series of the new modules was designated the "R-Series" and was identified by using red handles. The R-Series circuits were a reaction to the

rather complicated set of usage rules developed for the previous products. The goal was to make these easy to use and inexpensive . Integrated circuits were not used because they were more expensive than discrete components and the computer industry had not yet decided on the type of integrated circuit to use. The building block for R-Series logic was the diode gate, a sample of which is shown in Figure 11. The other basic circuit was the DCD (diode-capacitor-diode) circuit shown in Figure 12. The DCD gate was used to provide standardized levels to active devices such as flip-flops and to produce the logical delay necessary to sense and change flip-flops at the same time. ~~The first R-series operated at 1MHz, and eventually ti circuits now,~~ some PDP-8 ~~this technique worked at~~ 2 MHz (with Dick Best?),

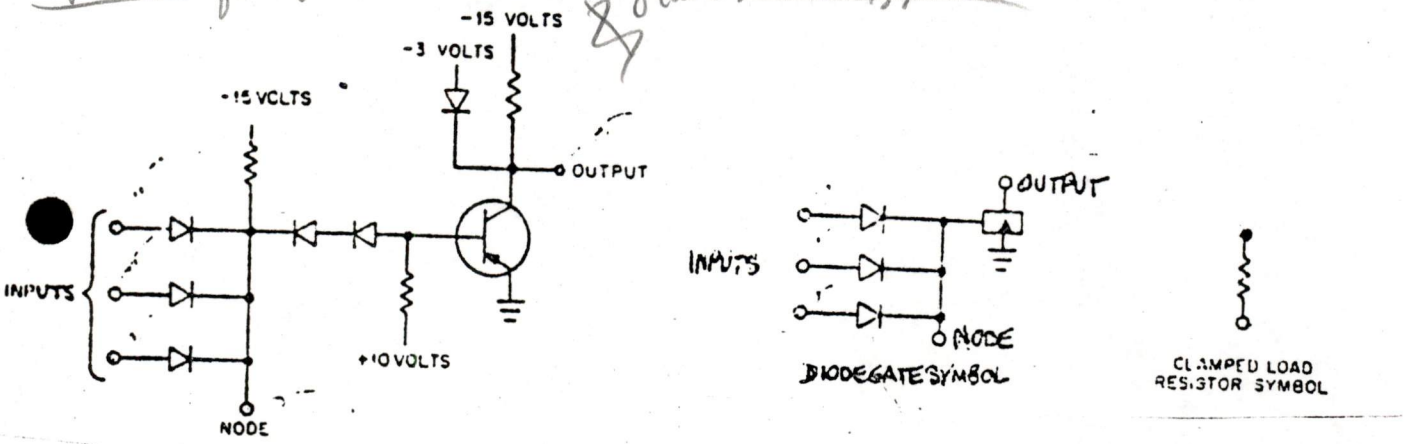


FIG. 11
DIODE GATE

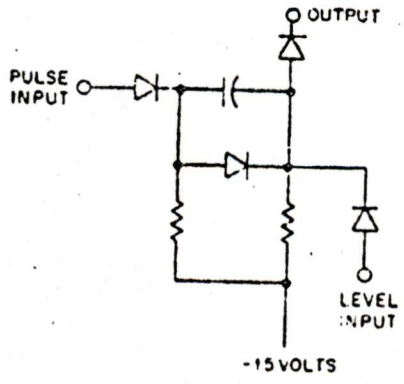


FIG. 12
DCD GATE

A second series of the new modules was developed for the first PDP-8s. This series was called the S-Series, although it also had red handles. The S-Series modules used the same circuits as their R-Series counterparts, but with variations to the values of the load resistors and DCD gate storage capacitors to obtain greater speed. than the 1Mhz R-series. —John Ash Did what this part was?

The B-Series with blue handles was essentially the same as the 6000 series of 10 MHz System Modules, but repackaged on the new 2.5 inch by 5 inch cards, and used silicon transistors rather than germanium transistors. The new silicon transistors were a mixed blessing. While they had temperature sensitivity characteristics superior to those of the germanium transistors, and their voltage drop characteristics permitted the elimination of the bias resistor to +10 volts, they did not saturate as well as the germanium transistors. Because they did not saturate well, the voltage between the collector and the emitter in the saturated state was not as low as it was with germanium transistors. This meant that the series arrangement of three inverters discussed in conjunction with the dotted lines in Figure 4 could not be used. Instead, only two of the silicon transistor inverters could be connected in series if the output was intended to drive another inverter. The first computer to use the B-Series modules was the PDP-7; ~~and~~ the PDP-10 processor ~~was a~~ was based on and extended the B-series

Analog applications were the target market for the A-Series modules, which had amber handles. This series, still being manufactured today, includes analog multiplexers, operational amplifiers, sample and hold circuits, comparators, digital to analog converters, reference voltage supplies, analog to digital converters, and various accessory modules. The peak development rate for analog modules occurred in 1971 with 38 new types and declined to 5 new types

in 1977.

While all of the preceding modules had been designed as user-arrangeable building blocks, the green handled G-Series was intended for modules that would only be sold as part of a system. For example, all of the DEC core memory circuits have been in the G-Series because a core memory system is sufficiently complex that a cookbook approach using a standard series of modules is not appropriate. The G-Series is still actively used today for circuits other than logic, generally in peripheral devices such as disks, tapes, and terminals.

Like the A Series and G Series, the W (white handle) Series is still manufactured, and is used to provide input/output capability between Chip-Chip modules and other devices. Lamp drivers, relay drivers, solenoids drivers, level converters, and switch filters are included in this family, but the only modules used widely today are the W900-W999 modules which include cable termination modules and blank boards upon which the user can mount ICs and wire wrap them together.

While the W-Series provided a variety of interface capabilities, the circuitry used therein was still too fast for typical industrial applications. Computer-oriented logic, by its very nature, is high speed and provides noise immunity far below that required in small-scale industrial control systems located physically close to the process they control.

Unfortunately, industrial electrical noise is not predictable to the nearest order of magnitude. Thus, attempts to solve the problems with "high level

logic" whose voltage thresholds were merely a few times greater than computer-type logic levels did not work well.

A new series of modules, the K-Series (with blac(K) handles), was developed which relied on a combination of voltage, current, and time thresholds to protect storage elements such as flip-flops and timers from false triggering. Since industrial controls typically interact with physically massive equipment, time thresholds are particularly attractive. There are four ways of exploiting these:

1) basic 100 Khz slow-down circuits everywhere
2) optional 5 KHz slow-down circuits available
3) transition-sensitive (edge-detecting) circuits provided with hysteresis to allow additional discrete capacitor loading when all else fails
4) replacement of the conventional monostable multivibrator or "one-shot" circuit by a timing circuit having both a low impedance and hysteresis at the input.

The hardware for the K-Series was specially designed to fit the NEMA (National Electrical Manufacturers Association) enclosures traditionally used with relay implemented industrial controls, but used the same connectors as the other Flip-Chip modules. Sensing and output terminals were provided with screw terminals and indicator lights, and appropriate arrangements were made to interface with 120 VAC devices. Wire wrap terminals were protected from external voltages but were available for oscilloscope probes. Magnetically latched reed relays and diode arrays that could be programmed by snipping out codes were provided as memory elements that would retain data during power

failures.

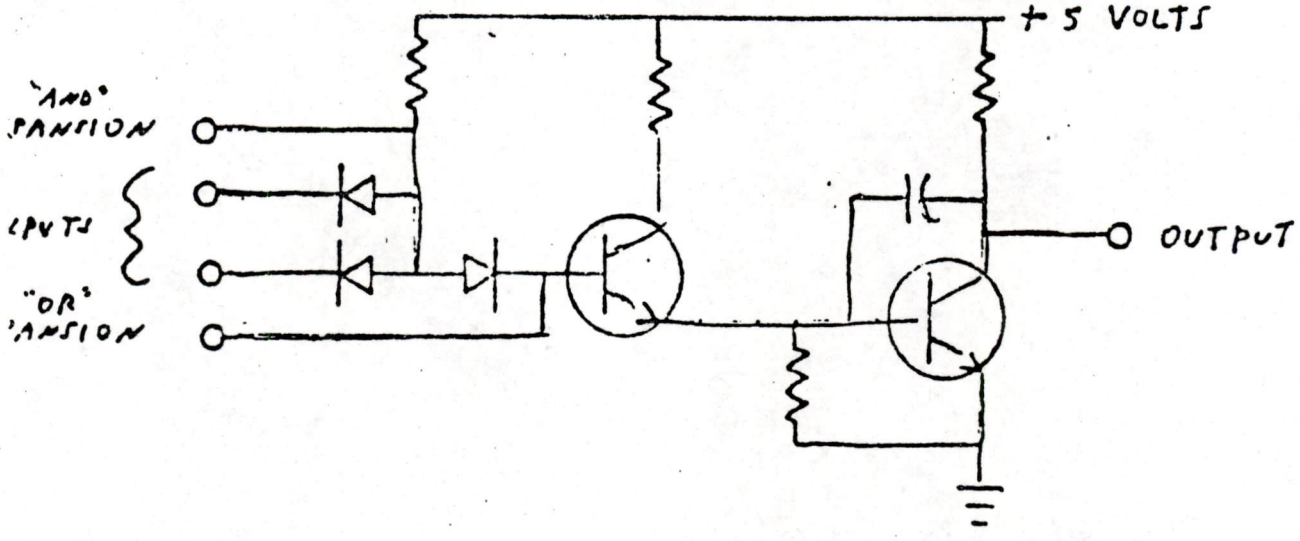


FIG. 13
K-Series Circuit

Gating in early K-Series modules was accomplished with discrete diode-transistor circuits such as that shown in Figure 13. Other K-Series modules used integrated circuits for the logic functions. In these designs the inputs to the ICs were protected with filter/trigger circuits which filtered out the noise and then restored the fast rise-times required by the ICs. Outputs were protected from output-induced noise and converted to standard

K-Series signals by circuits similar to those used in the discrete logic gates.

Unlike other DEC modules, the K-Series modules were not directly useful for constructing computers or computer-like data processing subsystems due to their low speed and high cost. They did play an important part in bringing digital logic into industrial applications, and the noise protection techniques developed for these modules were useful in the design of the PDP-14 Industrial Controller (Chapter 6).

By 1967 the electronics world had settled on transistor-transistor-logic (TTL) and the dual-in line package (DIP) as the technology of choice for integrated circuits and the cost for logic functions implemented in TTL ICs had dropped below that of discrete circuit implementations. With much more logic fitting into the same printed circuit board area, a single Flip-Chip card could now accommodate much more complicated functions. However, there were not enough connector pins available to get the necessary signals on and off the card. The answer to the problem was to keep the cards the same size, but to have etch and associated contacts on both sides of the printed circuit board. This increased the number of contacts from 18 to 36, and a new series with magenta handles (M-Series) was born. Subsequently, some G-Series and W-Series modules were also designed with ICs and double sided boards.

The advent of TTL brought the first power supply and signal level change in DEC's history. The -15 volt and +10 volt supplies were no longer required. Only a single +5 volt supply was needed to supply the logic signals which were now 0 and +3 volts. The packaging was kept consistant, however, as the old

single-sided modules could be plugged into the new connector blocks, and careful attention to pinning arrangements allowed double-sided module to be used in a single sided block at a sacrifice of some circuits.

The basic TTL circuit is the NAND gate shown in Figure 14.

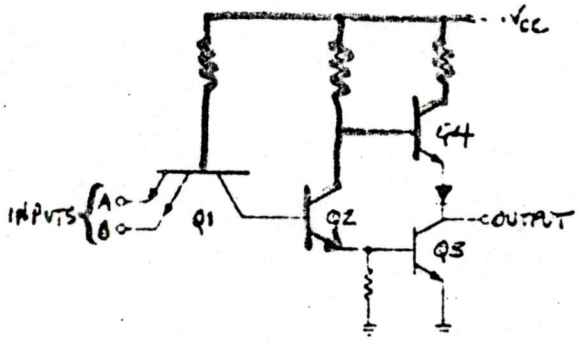


FIG. 14 TTL NAND Circuit

The input of the TTL gate is a multiple emitter transistor. If either input is

at or near ground (0 to 0.8 volts), Q1 becomes saturated, bringing the base voltage of Q2 low, turning off Q3 and turning on Q4 making the output high (+2.4 to +3.6 volts). If both inputs are high (above 2.0 Volts), Q2 has base current supplied to it through the collector diode of Q1, turning Q2 on. This in turn provides base current to Q3, saturating it and cutting off Q4, making the output low (0 to 0.4 volts).

Like the transistor inverter circuits discussed in conjunctuion with System Modules, TTL NAND gates can be cross-connected to form flip-flops.

The first generation of M-Series modules were used in a redesign of the PDP-8 called the PDP-8/I. The circuits used in these modules used TTL integrated circuits which were called "7400 series" integrated circuits because of a growing tendency in the semiconductor industry to standardize part numbers for TTL circuits, calling a package of 4 NAND gates a 7400, a package of six inverters a 7404, etc. The KI10 processor used in the PDP-10 ~~was~~ and the PDP-15 were designed from higher speed circuits using the 74H00 series of TTL integrated circuits. The 74H00 circuits were similar to the earlier 74 series, but were faster and used much more power. The first PDP-11 (the PDP-11/20) used both 7400 and 74H00 series ICs, as did the PDP-8/E. Both of these latter machines used 8.5 inch by 10.4 inch "extended quad" modules. ~~More important by~~ used general purpose modules and Note the earlier DEC IC machines (i.e. 8/I, 8/L, KI10, and PDP-15) had relatively low packing density since most interconnections were carried out on the backplane. The 8/E and 11/20 used a few specialized modules and interconnections were carried out on the printed circuit etch of the module. In ~~1970 an~~ M-Series ~~18-bit machine, the~~ PDP-15, was constructed. It was the last of the 18-bit generation which started with the PDP-1 (System Modules), and grew through the PDP-7 and PDP-9 (P-Series modules). The PDP-15 and the PDP-11/45 used Schottky TTL, a circuitry with such rapid switching speeds that four-layer boards had to be used such that the inner layers of power and

project initiated in 1970 and first shipped in 1972

ground etch could provide shielding. Also the

In 1972 work began on a new PDP-10 processor, the KL10. This used ECL current switching non-saturating logic from several vendors including the MECL (Motorola Emitter Coupled Logic) 10,000 series. This line of circuits is in some ways an integrated circuit version of the VHF modules. The basic gate is shown in Figure 15.

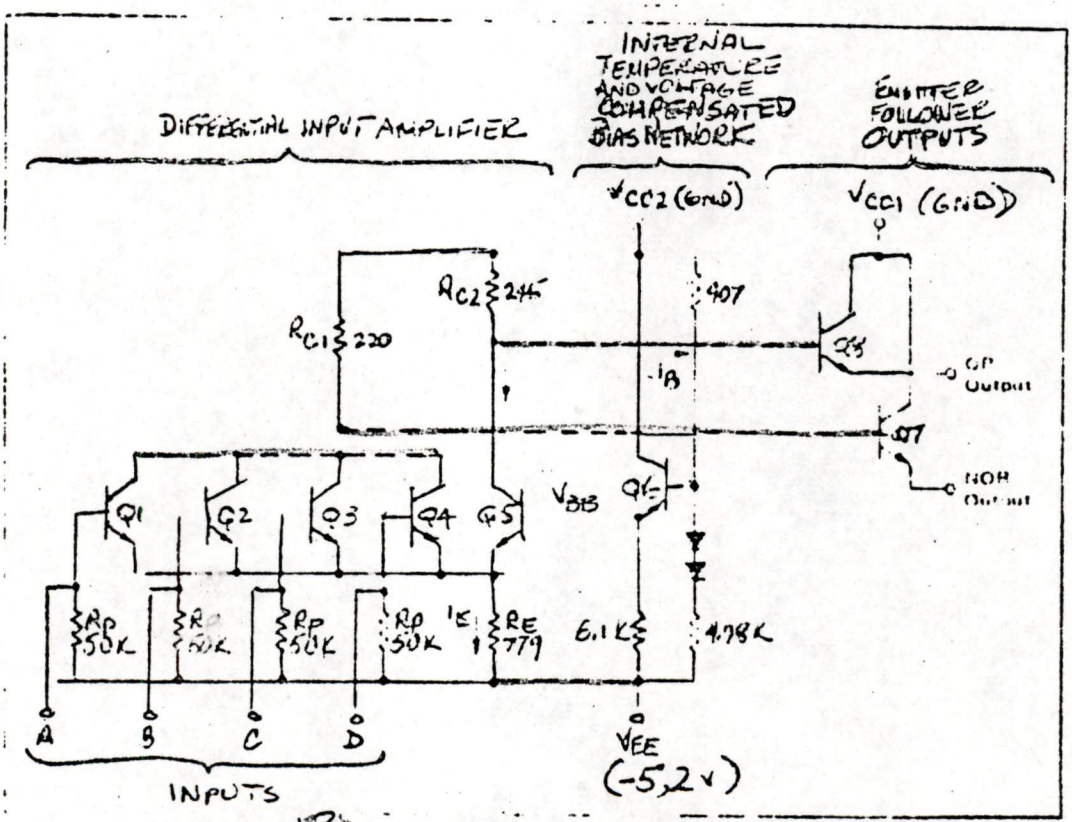


FIG. ~~13~~ 15 MECL, 10,000 BASIC GATE

Q6 has a temperature compensated internally generated reference voltage on its base of -1.3 volts. The outputs drive 50 ohm terrminated transmission lines returned to -2 volts. There is a complementary pair of outputs so that the circuit is both an OR and a NOR gate. At 25 degrees Celsius the upper level will between -0.81 and -0.96 volts, while the lower level will be between -1.65 and -1.85 volts. The circuits, like the Schottky circuits, are so fast that multi-layer boards are required. In addition, a great deal of care in signal line termination is required. As with the previous logic families studied, flip-flops can be created. The ECL master-slave flip-flops are quite complex, requiring 32 transistors and 7 diodes.

As the various module circuit technologies developed, not only could more logic functionality fit in a given space, but also the space provided on individual logic modules was increased. By 1973, the "hex" module (8.5 by 15.6 inches) was widely used, principally in the PDP-11 family. By 1977, ~~DEC~~ computers ~~were~~ was using 12 by 15.6 inch "~~extended~~ super hex" modules.

An evolution in circuits has continued as the technology has changed. As integrated circuits have become more powerful by the reduction of the size of their active elements, each new computer introduced is smaller, faster, and generally lower cost than its predecessor. While only DEC examples have been mentioned here, the trend toward smaller, faster, and less costly computers has been true across all of the computer manufacturers.

The chart below shows the number of module types that were started each year from 1957 through 1977.

R. Best, R. Doane, J. McNamara Edited 3/17/78

Figures: Photos of

1. Photograph of Digital Laboratory Module in a System ← need photo of system
2. Photograph of Digital System Module
3. Schematic of an Inverter Used in Digital System Modules
4. Symbolic Drawing of an Inverter
4.1 Signal naming convention and signal levels through inverter (NOT gate) for DEC dual polarity logic.
5. OR Gate
6. AND Gate
7. Flip-Flop
8. Flip-Flop With Inverter
9. Negative C-D Gate
10. Positive C-D Gate
10.1 ~~30 Mhz logic module~~ Photograph of 30 Mhz flip flop
11. Diode Gate
12. D-C-D Gate
13. K Series Circuit
14. TTL Circuit
15. ECL Circuit

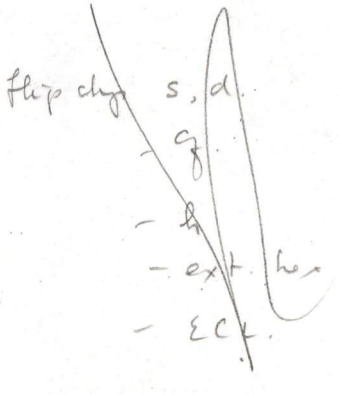
8.1 Register transfer representation of PDP-1 accumulator, AC.

8.2 Logic diagram of PDP-1 accumulator abit, AC<j>.

10.2 Photograph of ~~single~~ double height Flip Chip modules used in PDP-7 and PDP-8

15.1 Photograph of super hex modules ~~to~~ as used in VAX-11/780.

16. Time line chart of the ~~number of~~ modules introduced each year at DEC ~~Since 1970~~



The adder illustrated below is built from negative C-D gates and unbuffered flip-flops.

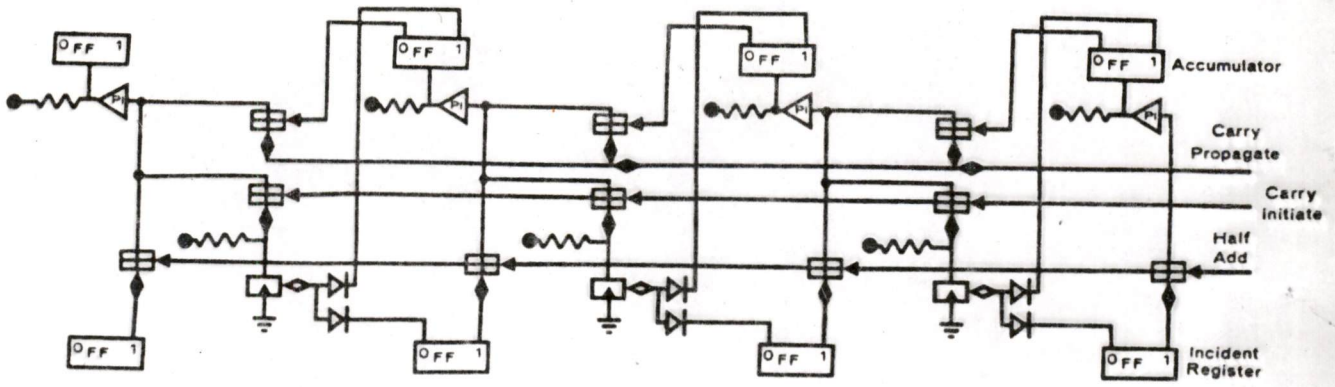


Figure ~~56~~ 23
Parallel binary adder
(DEC Flip-Flop Type 4215 for accumulator)

Figure 23
Parallel binary adder
(DEC Flip-Flop Type 4215 for accumulator)

This is also a two step add; a half add is followed by a carry.

VHF (See Russ Doane's insert.)

FLIP-CHIPS
1964 -

STRATEGY AND PACKAGES:

Each year the cost of semiconductors decreased, causing the cost of the hardware used to house the semiconductors to be more significant. The answer was a 2.5 x 5 inch card with a labelled and color-coded plastic handle to be plugged into a connector block that can hold 8 such modules with sufficient insertion depth to support them. An added production gain was made by making 4 modules at once, and cutting the "quad" into "singles" after assembly.

THE CIRCUITS

R SERIES

The R-series (red handles) circuits were a reaction to the rather complicated set of usage rules developed for the previous products. The goal was to make these easy to use

Dick: too long? Need a diagram?

Thom 3-2237

VHF MODULES

USING EMITTER-COUPLED LOGIC (E C L)

The use of saturating MADT transistors with toroidal pulse transformers appeared to be near its limit at 10MHz in the 6000 Series. The pulses already needed to be 40% of the minimum time interval to achieve adequate "on" times, tightly constraining transformer recovery and making it difficult to design circuits that were not excessively sensitive to repetition rate. Series gating stacks had to be limited to two transistors for many purposes. Gate delays were large enough to prevent some needed logic configurations from propagating within the 100ns interval implied by the 10MHz rating.

A major break with previous circuit geometries appeared necessary. The use at IBM of non-saturating logic encouraged an exploration in that direction. The project was dubbed "VHF Logic" because operation at 30MHz or better (the bottom end of the VHF radio band) was a goal.

Solid-wall co-ax had just been introduced, and the 50 ohm version of this product appeared to have a strong enough center conductor for practical hookup between modules while not being too bulky for easy hand bending. Since leads longer than a few centimeters were expected to require special care, the availability of a satisfactory transmission-line hookup medium was felt to be an essential element for ease of use, and the 50 ohm impedance level was therefore adopted. (Remember that in those days, each flip-flop was going to need its own separate module, imposing about 1cm of intermodule leadlength in addition to connector pins and any printed wiring length).

POWER DISSIPATION

Due to the low impedance needed for practical co-ax hookup, considerable power had to be dissipated. Moreover, 3 volt swings had to be available for compatibility with existing modules. The ability to drive at any point along a co-axial transmission line appeared necessary for practical hookup. These needs were met by choosing a 60 milliampere output current, producing a 1.5 volt swing on a double-terminated 50 ohm line and a 3 volt swing with a 50 ohm load when interfacing to existing slower logic.

These voltage and current levels required heatsinking of the output transistors. Spring clips were designed to fasten the transistor TO18 cans directly to the connector pins, exploiting the connector as a heatsink and at the same time providing a minimum-inductance connection from the transistor collector (common to the case) out of the module.

LOGIC DELAY LINES

Flip-flop feedback delay was provided by 10ns stripline etched onto the p c board. A meander pattern was selected with a degree of local coupling between loops to achieve around a 7:1 delay-to-risetime ratio. Both the delayed and the undelayed ends of this 50 ohm stripline were made available at the module pins. The undelayed outputs switched simultaneously, allowing a subsequent gate to subtract a delayed flip-flop output signal from its complement undelayed, to produce 10ns pulses when needed.

PERFORMANCE

Rated performance was 30MHz, limited by the capabilities of the production

sters. Bench testing demonstrated 40MHz capability, with ~~every~~ evidence at 50MHz performance could have been promised if the testing problem had en solved. Risetimes were better than 1.5ns, despite the need for 100 ohm sistors at transistor bases to damp the self-oscillation of the ffectively) common-collector circuit geometry.

dules delivered to customers were used to build satisfactory high rformance systems. However, the need for this level of performance was not despread, being limited to advanced laboratory instrumentation. The o-year product development cycle wore out the initial enthusiasm of most GITAL people, futher attenuating product momentum.

LATION TO OTHER PRODUCTS

spite their failure as a product, the VHF modules eventually made a ntribution to computer progress. To produce the first commercial mesharing systems, the PDP-6 ~~group~~ needed ~~a way of comparing relocated~~ dresses at high speed. The PDP-6 relocation comparator was designed very ickly ~~using current-mode logic~~.

IS THAT REALLY WHAT IT DID?

t as a series of general-purpose products for engineers to use, the cost of e VHF modules and the inconvenience of their wiring was too great. Further velopments in general-purpose logic modules were to lie in the opposite rection: cheaper, more compact, easier to use, and slower.

a high-speed register comparator which was quickly designed using current-mode logic.

(and inexpensive). Intesrated circuits were not used because (1) they were more expensive than discrete components and (2) the world had not as yet decided on the type of IC to use.

DIODE GATE

The buildins block was a diode sate (see Fisure 24). The transistor emitters were always at sround. The load resistor was a 2 ma (instead of 10 ma load in previous desisns) and the input load was 1 ma with a fan-out of 18. The node inputs allowed expansion of the sate with the addition of one diode per input.

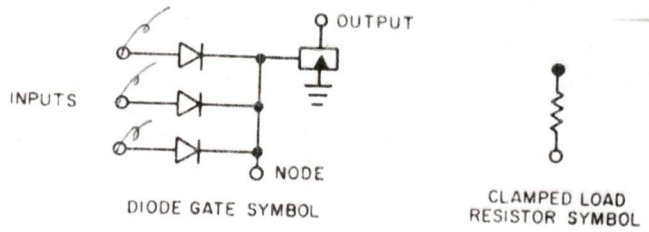
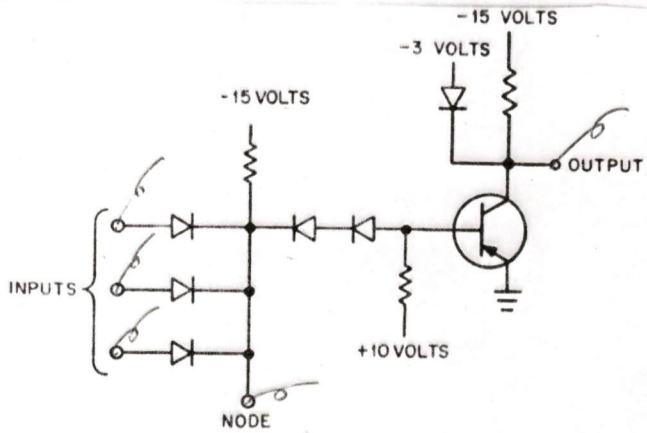


Figure 4 Diode Gate and Clamped Load Resistor Symbols

24

Diode-Gate Symbol Clamped Load Resistor Symbol



24
Figure 2 Multiple Input Diode Gate

Fisure 24 - Basic Diode Gate Circuit

NOR and NAND losic can be created as shown in Fisure 25.

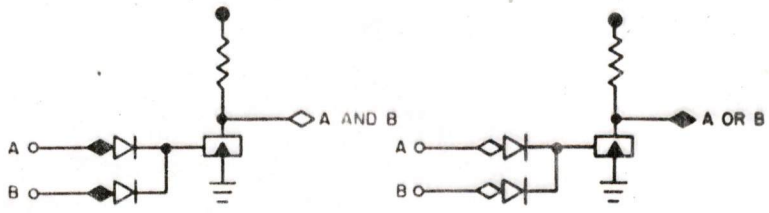


Figure 5 Diamonds Indicating the Voltage Levels

25

Figure 25 - NOR And NAND Examples

DCD GATE

The other basic buildins block is the diode-capacitor-diode sate illustrated in Figure 26.

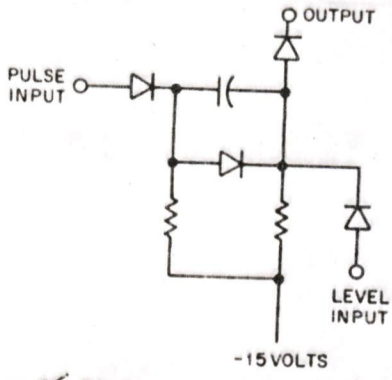


Figure 26 Diode-Capacitor-Diode Gate Circuit

Figure 26 - Diode-Capacitor-Diode Gate Circuit

The DCD sate standardizes inputs to active devices such as flip-flops and produces the losical delay needed to sense and chanse flip-flops at the same time. The pulse input is a positive-soins level chanse from -3V to sround. If the pulse input has been at -3V and the level input at sround for a set-up time and the pulse input soes to sround a positive pulse will appear at the output. If the level input had been at -3V also, no pulse would have appeared at the output. If the level input had sone to -3V at the same time as the pulse input went to sround a pulse would still be senerated. The capacitor provides the losical delay. The DCD sate symbol is shown in Figure 27.

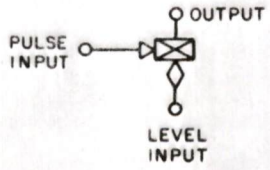
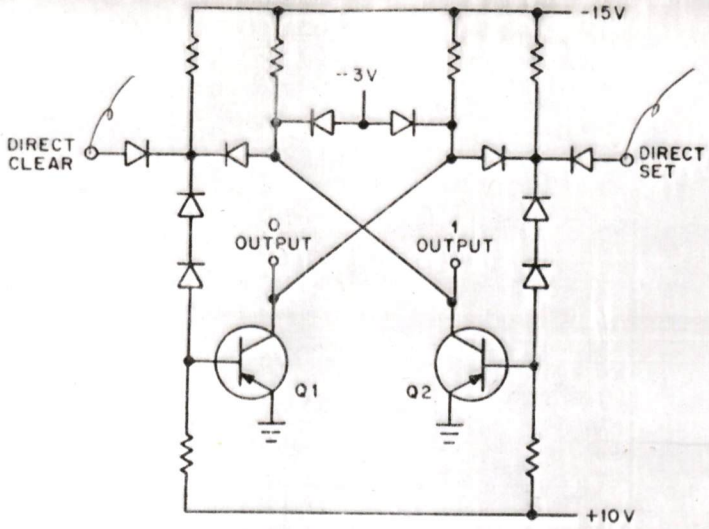


Figure 27 Diode-Capacitor-Diode Gate Symbol

Figure 27 - Diode-Capacitor-Diode Gate Symbol

flip-flop

A flip-flop is made from a pair of diode sates connected back-to-back as shown in Figure 28. The flip-flop can be set and cleared by srounding the appropriate output with the output of a diode sate.



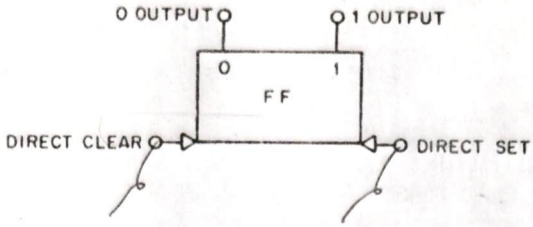
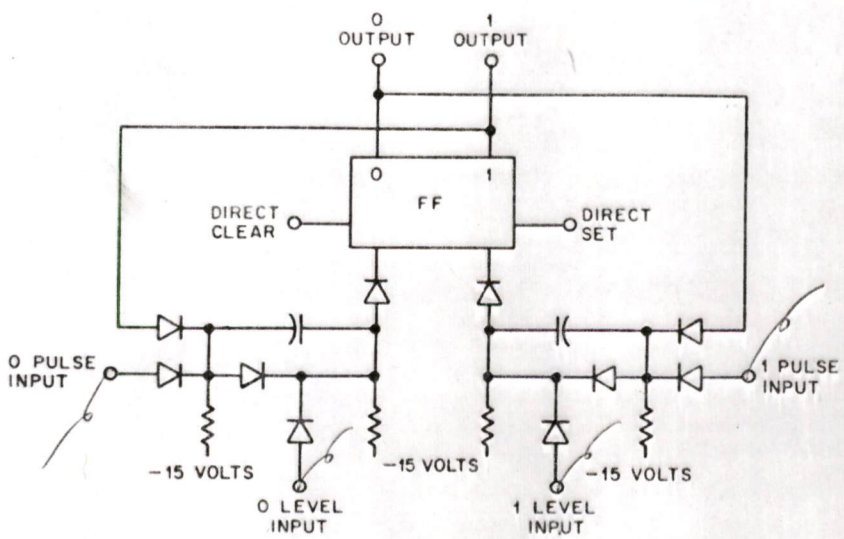


Figure 9 Flip-Flop Schematic and Symbol

28

Figure 28 - Flip-Flop Schematic and Symbol

It can also be set and cleared by using the positive output pulses from a DCD gate. Figure 29 shows a flip-flop with built-in DCD gates.



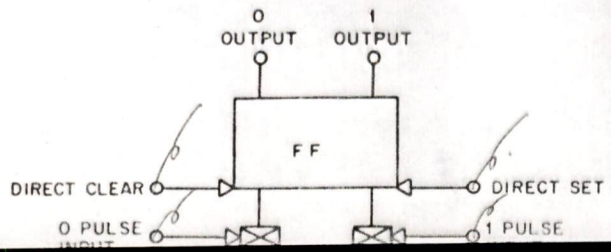


Figure 28 - Flip-Flop Schematic and Symbol

It can also be set and cleared by using the positive output pulses from a DCD gate. Figure 29 shows a flip-flop with built-in DCD gates.

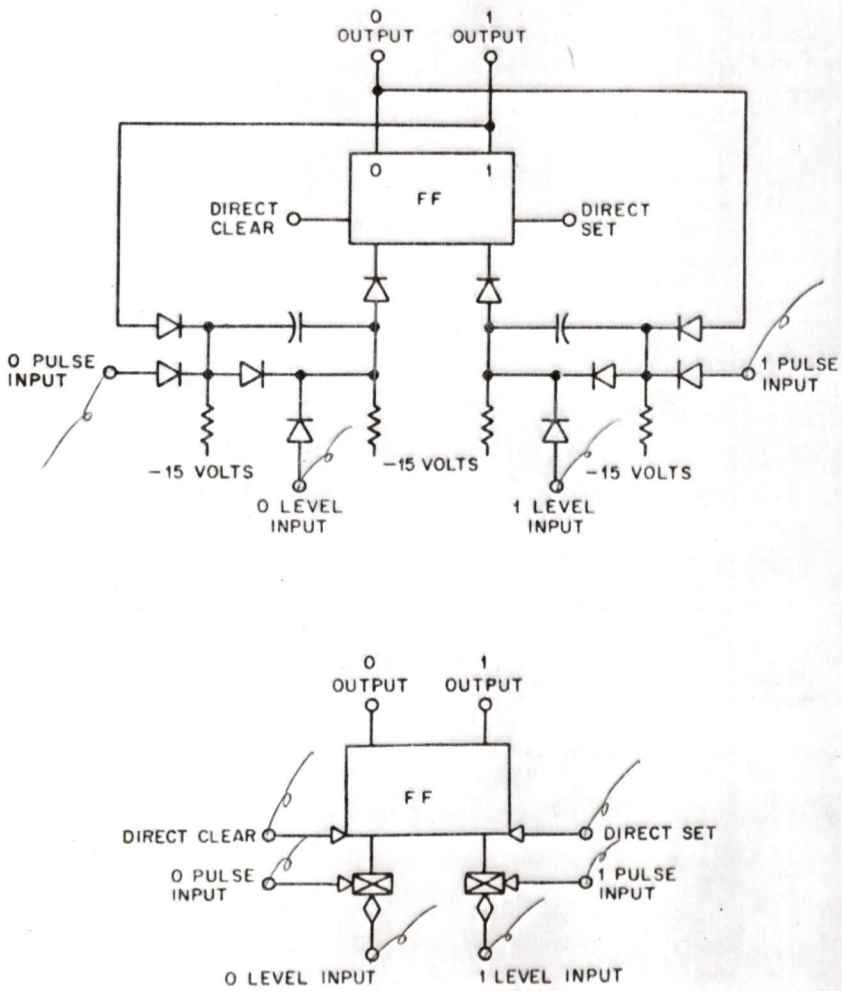


Figure ~~10~~ 29 Flip-Flop with DCD Gates, Schematic and Symbol

Each DCD gate is conditioned by the opposite flip-flop output as well as an external input. Therefore, the "set" input DCD gate can only be enabled if the flip-flop is in the ZERO state. Complementing a flip-flop with such gates

is easy, as shown in Figure 30.

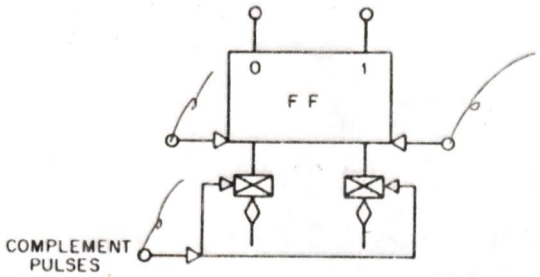


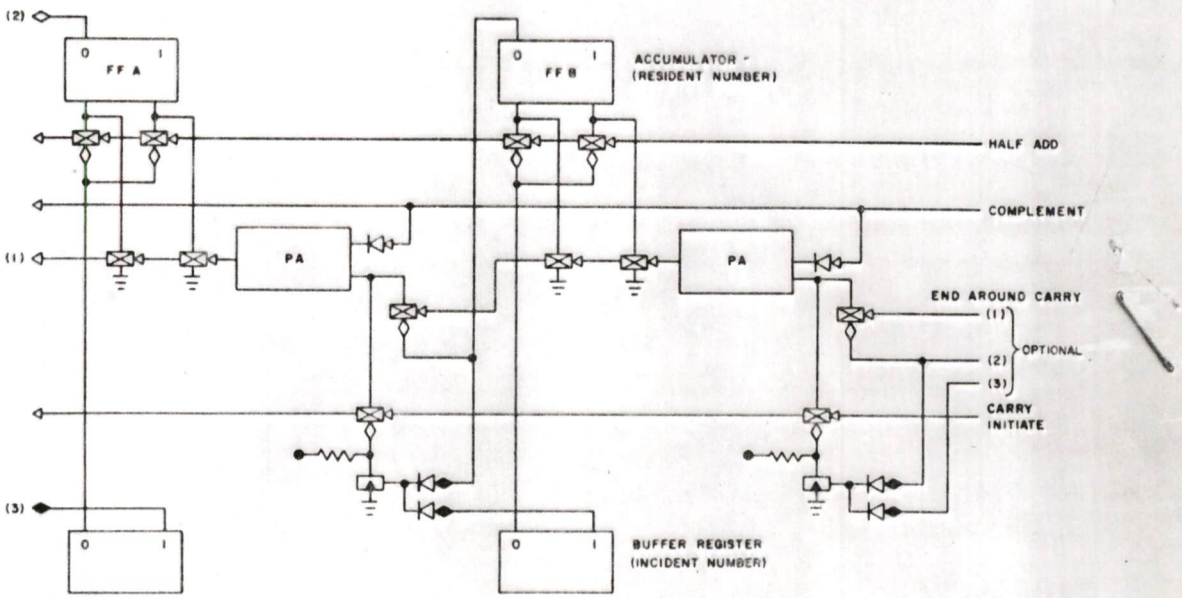
Figure ~~11~~ 30 Complementing

Figure 30 - Complementing

The clock has an output pulse that goes from -3V to ground for 100 nanoseconds, returning to -3V. Its maximum prf is 2 MHz. The delay was triggered by a D-C-D gate and produced an output that was at -3V for the duration of the delay. The trailing edge of its output could drive the pulse input of a DCD gate.

ADDERS

Figure 31 shows an adder using R-series circuits.



31
Figure ~~28~~ Parallel Adder
(R201 Flip-Flops in Accumulator and
Any Flip-Flops in Incident Register)

Figure 31 - Parallel Adder

Addition is performed in two steps. The first step is half add and the second step is the carry.

THE S SERIES

The first PDP8 was constructed from modified R-series circuits called the S series. The load resistor and the DCD gate storage capacitor were changed to achieve higher performance.

THE B SERIES

The B series with the blue handles was essentially the 6000 series of 10 MHz circuits repackaged on Flip Chip cards, and using silicon PNP transistors instead of germanium. The diode drop of silicon is sufficiently greater than that of germanium that the base input network does not need a biasing resistor from the base to +10V. The inverter is illustrated in Figure 32.

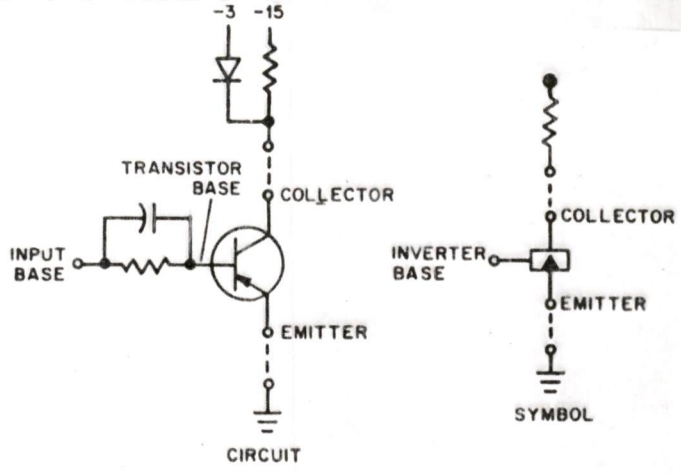


Figure 32 Inverter Circuit and Symbol

The silicon allowed the elimination of the bias input resistor to +10V but it does not saturate as well as the previous germanium transistors. Therefore, only 2 inverters could be put in series if the output was to drive another inverter. If the output is to drive a pulsed device such as a pulse amplifier three inverters may be put in series with the pulse going to the inverter whose emitter was at ground.

Buffered flip-flops were used as in the 6000 series so that the delay in the buffer would allow sensing and changing a flip-flop with the same pulse.

The B series was used in the PDP7, the repackaged PDP4 (which was built with 1000 and 4000 series System Modules).

THE A SERIES

The A series with the amber colored handles were Flip Chip modules for analog use. A100 series is for analog multiplexers, A200 series for operational amplifiers, A400 series for sample and hold, A500 series for comparators, A600 series for digital-to-analog converters, A700 series for reference voltage supplies, A800 series for analog-to-digital converters and A900 for accessory analog modules. The peak development rate of analog modules occured in 1971 with 38 new types, reducing to 5 in 1977. The more recent analog modules are quads or hexes in the A000 series, and are combinations of all the other circuits in much more compact form using integrated circuits.

THE G SERIES

The G series with the green handles were intended to be only sold as part of a system. For example, all of the core memory circuits were in the G series; a core memory is sufficiently complex that a cook book approach using a standard series of modules could not be used. G series is still actively being used for circuits other than logic generally in peripheral devices such as disks, tapes, terminals, etc.

THE W SERIES

The W white handled series provided input-output capability between Flip Chip and other devices. Since all early Flip Chip circuits used the same logic levels of 0 and -3V all System Modules were compatible.

Inputs of R series circuits only draw current when the input is at ground. Many inputs of B series and System Modules draw current at -3V. In order for R series to drive such circuits a higher current clamped load was necessary. Several W series modules made clamped loads of various sizes available.

W series cable connector modules terminated cables to a module to make the cable ends available to the back panel.

Types W050 and W051 provided high current for lights, relays, solenoids, etc. The W501 was a comparator used to convert low frequency or noisy signals to standard 0 and -3V levels. The W510 converted positive logic (0 and +3V) signals to negative (0 and -3V) levels. The W600 series provided low power outputs for driving devices needing signal levels between +20V and -15V. Inter-series converters were not necessary for levels - all circuits used 0 and -3V. Pulses did need to be converted and could be done with the existing pulse amplifiers and a table of rules. The W700 contains switch filters to remove contact bounce from relays and other switches.

INDUSTRIAL K-SERIES, 1968: (See Russ Doane's insert.)

INTEGRATED CIRCUITS AND DOUBLE DENSITY, 1968

By 1967 the world had settled on TTL IC devices and the cost had finally become lower than discrete components. With much more logic fitting into the same card area there weren't enough connector pins available. The answer was to keep the same size cards and connectors except to put contacts on both sides of the cards, increasing the number of pins on a single card from 18 to 36. The M series (magenta handles) resulted. Some new G series and W series modules also were double sided and began to use TTL integrated circuits.

M SERIES, INTEGRATED CIRCUITS

For the first time in DEC's history the signal levels and power supply levels changed. Instead of a principal supply

DICK
Is THIS ANYTHING CLOSE TO WHAT YOU NEED?
30 Nov '77
R. Doane

K SERIES

CONTROL MODULES

NOISE IMMUNITY

Computer-oriented logic, by its very nature, is high speed and provides noise immunity far below that required in small-scale industrial control systems located physically close to the process they control.

Unfortunately, industrial electrical noise is not predictable to the nearest order of magnitude. Thus attempts to solve the problem with "high level logic" whose voltage thresholds were merely a few times greater than computer-type logic levels were only marginally rewarding.

K Series circuits rely on a combination of voltage, current, and time thresholds to protect storage elements (flip-flops, timers) from false triggering. Since industrial controls typically interact with physically massive equipment, time thresholds in particular are attractive. There are four ways of exploiting these:

1 basic 100 KHz slow-down circuits everywhere
2 optional 5 KHz slow-down circuits available
3 transition-sensitive (edge-detecting) circuits provided with hysteresis to allow additional discrete capacitor loading "when all else fails".
4 replacement of the conventional monostable multivibrator or "one-shot" ciruit by a timing circuit having both a low impedance and hysteresis at the internal analog voltage-sensing node.

SPECIAL PRODUCTS INCLUDED

The hardware for this series is specifically designed for NEMA enclosures such as those traditionally used with relay logic,

motor starters, etc in heavy industry. However, K Series modules also fit standard 19 inch rack connectors as used with other FLIP CHIP modules.

Sensing and output circuits are provided with screw terminals and indicator lights, and are available with 120VAC ratings for full compatibility with industrial elecromechanical devices. Inputs from limit switches and the like see a moderate inductive load to assure normal contact arcing, required to break down adsorbed films which would otherwise reduce contact reliability. Solid state AC switches are fully protected against false triggering. Voltages present in the external environment are excluded from the wire-wrap connections within the logic.

Every wire-wrap post is accessible for probing either by general-purpose test equipment (meters, osscolloscopes) or by the special K Series test probe that shows logic states and stretched-for-visibility pulses on two indicator lights, and has a built-in illuminator for use in dimly-lit environments.

Magnetically-latched reed relay memory elements are provided for non-volatile storage of control system state in the event of a power failure.

PROMs (as they were later called) are included, using discrete diodes physically clipped out of the circuit for storing control sequences, etc.

Lights, thumbwheel and toggle switches, and calibrated timer controls are mounted directly on printed circuit boards to avoid the wiring and soldering as well as the custom-made bracketry otherwise needed for internal controls and maintenance aids.

Binary and binary-coded decimal counters as well as shift registers, comparators, and bit rate multipliers are all 4 bits wide and are all assigned the same pinouts for the 4-bit data

paths. All discrete gating elements are grouped three to a module, and again pinouts for similar functions are standardized. The avoidance of randomly-assigned pinouts is a help when designing, wiring, and debugging a K Series system.

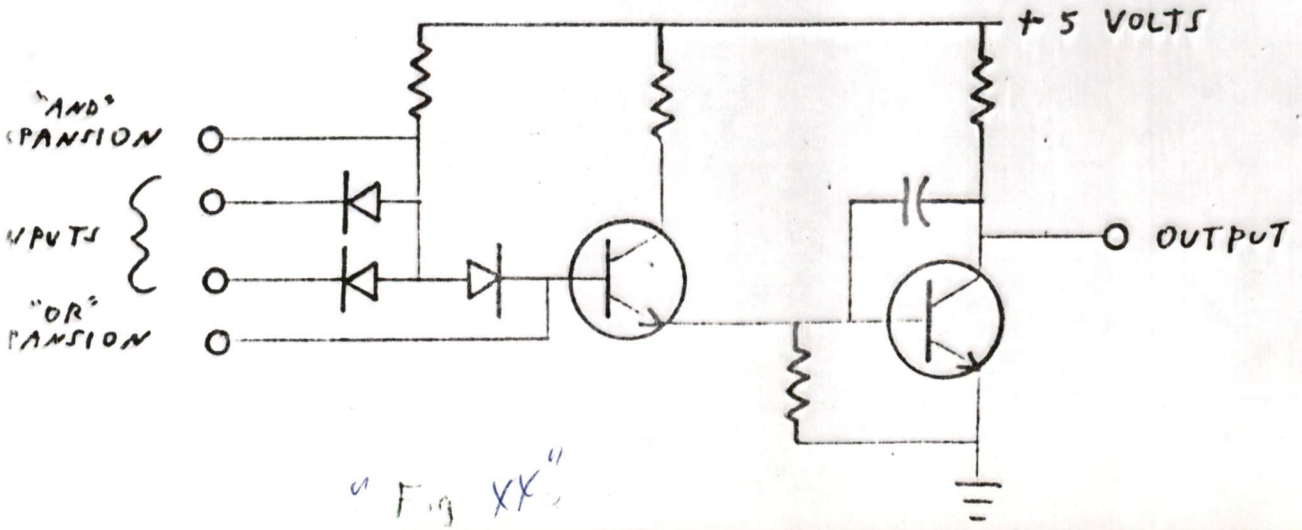
Numbers assigned to K Series products are similar to the conventions adopted for earlier module series:

K0xx	Gate expanders
K1xx	Gates
K2xx	Memory (flip-flops, counters, etc.)
K3xx	Timing
K4xx	Controls (lights, switches, etc.)
K5xx	Input voltage converters
K6xx	Output drivers
K7xx	Power supplies
K8xx	Mounting hardware, etc.

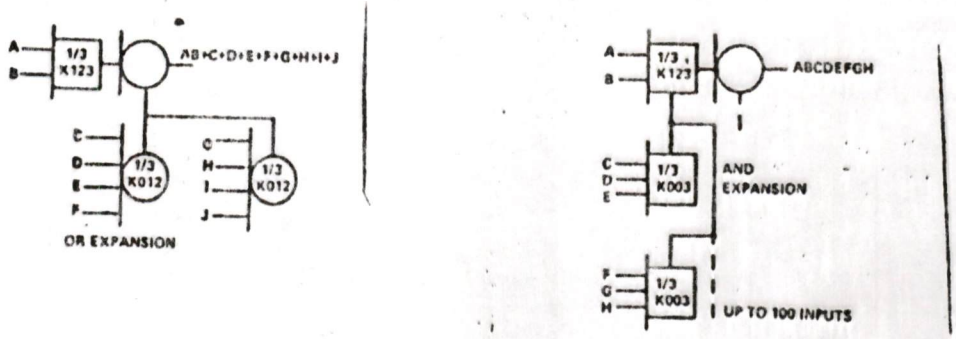
CIRCUITS

Gating is accomplished with discrete diode-transistor circuits. Every output transistor has a Miller-effect capacitor of 680 picofarads for establishing a noise inhibiting time threshold.

The basic gates have pin connections to both the anode node for the input diodes, and also the cathode of the diode that connects that node to the transistor output circuit. These connections are used with a variety of diode-resistor gate expanders to provide complex gating structures at low cost.



"Fig XX"



LOGIC FUNCTIONS WITH GATE EXPANSION

Most K2xx products used integrated circuits for the logic functions. Inputs were protected by filter/trigger circuits to first strip off noise and then restore fast risetimes required by the I Cs. Outputs were protected from output-induced noise and converted to standard K Series signals by circuits similar to those used within discrete gates. RTL integrated circuits were found to be significantly easier to combine with these discrete-component noise isolating circuits than either TTL or DTL I Cs.

The most troublesome circuits in noisy environments had traditionally been the monostable multivibrators used for time delay. There were three reasons for this:

1 A high value of charging resistance is necessary to provide long delays with small inexpensive capacitors, and

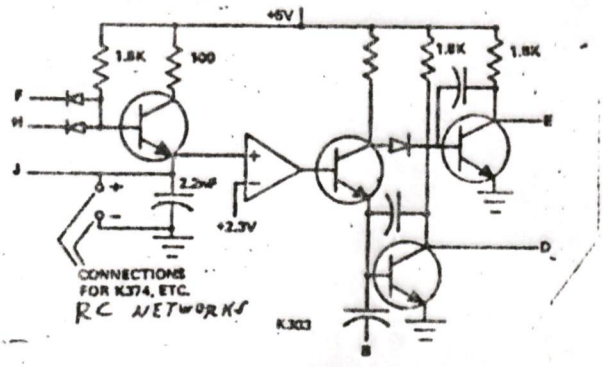
2 Traditional circuit geometries obtained circuit simplicity by placing the timing capacitor in a series path with both its terminals ungrounded, so the charging resistor had to be a significant part of the noise-inhibiting shunt conductance. Morover,

3 As the switching point was approached during timeout, a diminishing voltage threshold remained to be

overcome to switch the circuit, resulting in a particular type of noise effect called "time jitter".

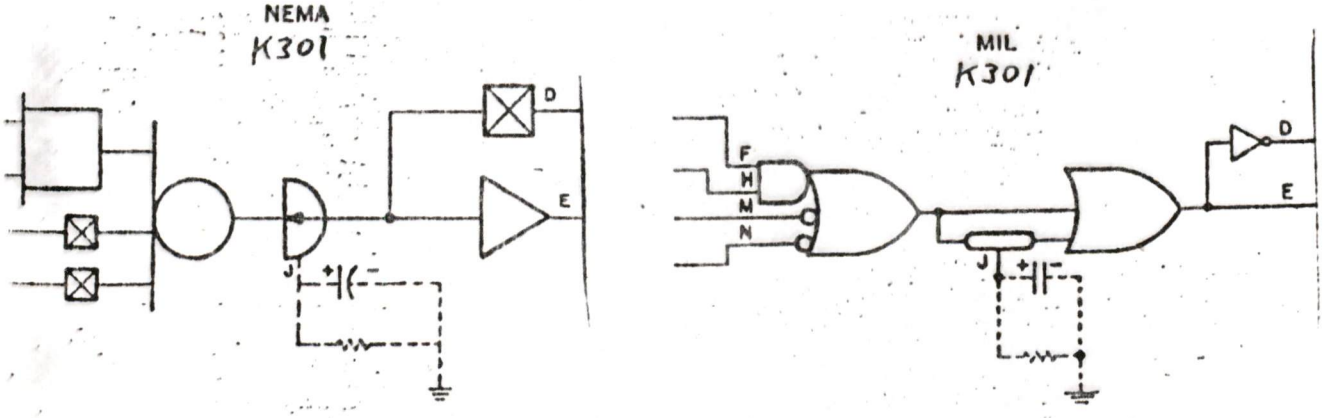
To make matters worse, the timing resistance in many control systems needs to be placed on the control panel some distance from the logic system, creating a long antenna for noise pickup at the most vulnerable circuit node.

All K Series timing circuits were designed to avoid these problems two ways. First, all timing capacitors have one end grounded. This converts the analog-voltage node to a very low impedance point, with the timing capacitor itself acting as a large filter capacitor. Second, the voltage-sensing circuit is provided with a small but finite hysteresis, so a small voltage modulation near the switching threshold cannot produce multiple threshold detections.



K303 TIMER SIMPLIFIED SCHEMATIC

Fig 3



AC input circuits use small step-down transformers to achieve two essential funcions:

* Isolation of logic ground from AC neutral potential, to prevent ground loops
* Magnetizing-current inductive loading of line-voltage silver contacts, to prevent dry-circuit failure of the contacts by accumulation of an insulating film; the energy stored in the magnetizing inductance forms a contact-cleaning arc at each switching event.

AC output circuits use a triac thyristor driven by an isolating transformer, again to prevent ground loops.

Power regulators in the same plug-in printed board format are included to facilitate the construction of small, low-power control systems.

SUMMARY SPECIFICATIONS

Frequency range: DC to 100 KHz. Control points on some modules allow reduction to 5 KHz when building RS flip-flops or multi-state control sequence storage elements out of gates. (Gates themselves don't really need to be slow if all storage devices are noise-resistant)

Signal levels: 0 V and +5 V, regardless of fanout used.

Fan-out: 15ma available from all outputs; typical inputs 1-4 ma. Wired-OR and Wired-AND capability provided for.

Waveforms: Trapezoidal. No fast transients to cause cross-talk

where wiring is bundled (though computer-type point-to-point wiring is recommended for ease of signal tracing). External capacitive loading (as for noise filtering of long logic wires inadvertently placed in a high noise field) affects speed only; no risetime dependence for correct circuit operation.

Temperature range: -20 C to +65 C for simple logic gates and interface circuits. Complex modules employing integrated circuits limited to 0 C minimum.

Noise immunity: False "1": 30ma at 1.6V for 1.5usec typical. False "0": 3ma at 3V for 1.5usec typical. Time thresholds can be increased by a factor of 20 for RS flip-flops and multi-state control sequence storage elements constructed from simple gates.

Power requirements: +5V, 10% tolerance. Dissipation typically 200mw per counting or shifting flip-flop, 30mw per control flip-flop, 10 mw per two-stage diode gate.

Compatibility: M Series TTL outputs can drive K Series logic gates and output interface drivers directly. Other K Series inputs may be driven from M Series modules after passing through a K Series gate, provided they meet certain timing requirements defined in an application note. M Series inputs can be driven by K Series outputs, subject to precautions against multiple responses due to the slow transitions a t K Series outputs: also covered in an application note.

RELATIONSHIP OF K SERIES TO OTHER PRODUCTS

Unlike other DIGITAL module series, the K Series is not directly useful for constructing computers or computer-like data processing subsystems due to its slow speed and higher cost per logic function.

K Series interface modules, however, played an important part in the introduction of powerful digital logic into industrial applications. With the knowledge of noise protection gained and the K Series interface modules, the PDP-14 Industrial Programmed Controller and other industry-oriented systems could be designed and applied with confidence.

of -15V and a bias supply of +10V there was a principal supply of +5V. The logic levels went from previous 0 and -3V levels to 0 and +3V. We, at least, kept the packaging consistent - a single-sided module could be plugged into a double-sided connector block and a double-sided module could be used in a single-sided connector. The first M series modules were partitioned in such a way that half of the circuits were available to a single-sided connector back panel.

M000 series:	signal converters
M100 series:	gate circuits
M200 series:	flip-flops
M300 series:	delays
M400 series:	clocks
M500 series:	input converters
M600 series:	high power logic drives and output converters
M700 series:	complex logic modules
M900 series:	cable connectors and terminators

CIRCUITS:

The basic TTL circuit is the NAND gate shown in Figure 33.

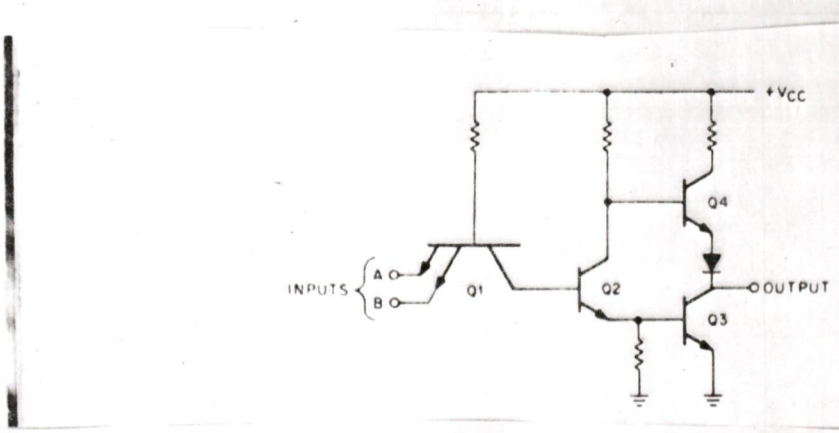
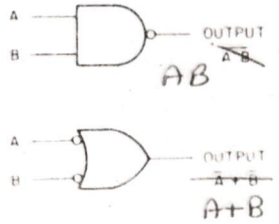


Figure 33 - TTL NAND

The input of the TTL gate is a multiple-emitter transistor. If either input is at ground (0 to +0.8V) Q1 becomes saturated, bringing the base voltage of Q2 low, turning off Q3 and turning on Q4 making the output high (+2.4 to +3.6V). If both inputs are high (above +2.0V) Q2 has base current supplied to it through the collector diode of Q1, turning Q2 on. This in turn provides base current to Q3, saturating it and cutting off Q4, making the output low (0 to 0.4V).

The MIL symbology used for this gate is shown in Figure 34.



A	B	OUTPUT
L	L	H
L	H	H
H	L	H
H	H	L

Figure 34 NAND Gate Logic Symbol and Truth Table

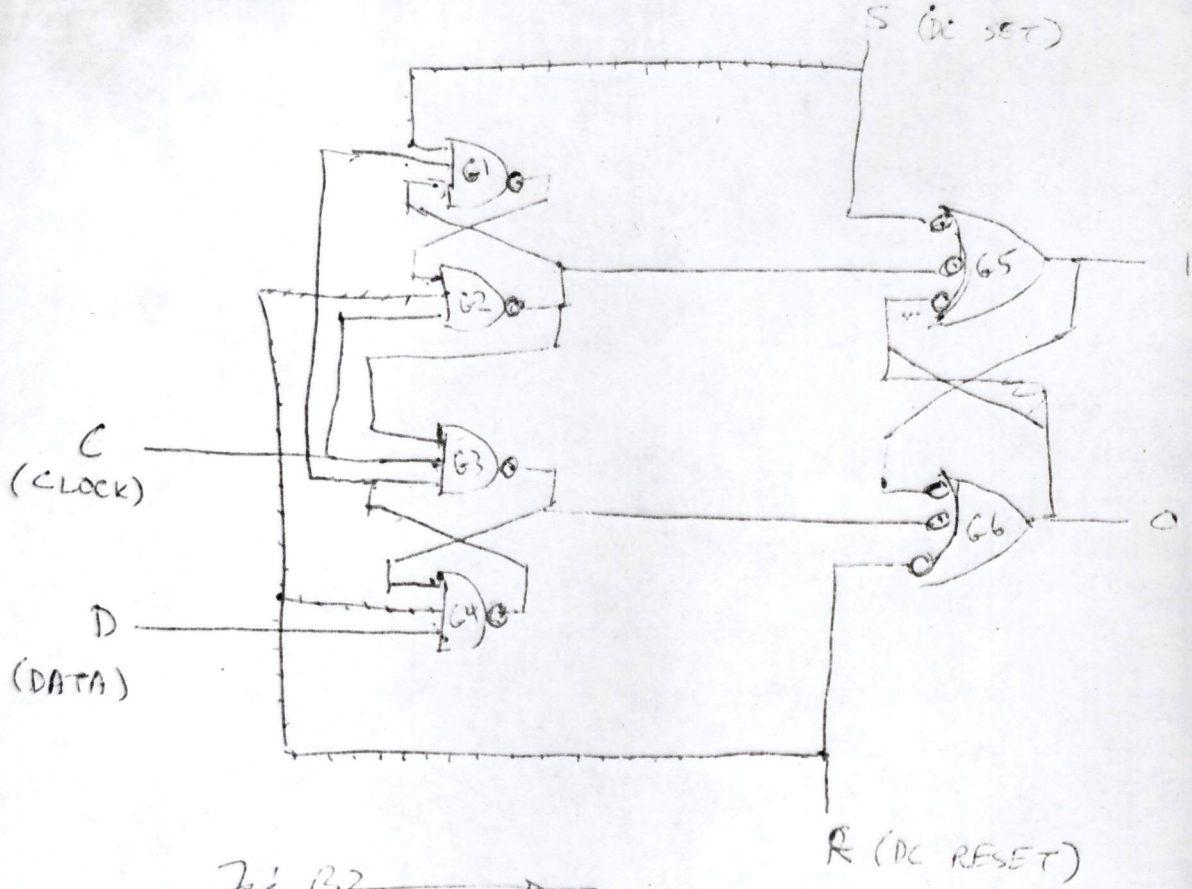
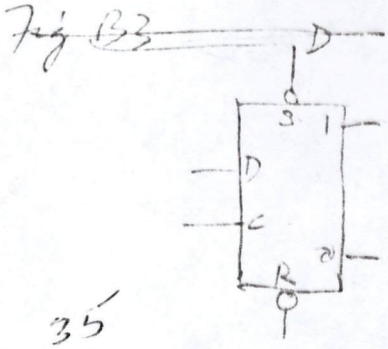


Fig B3



LOGIC SYMBOL

35

Fig B3. D FLIP-FLOP

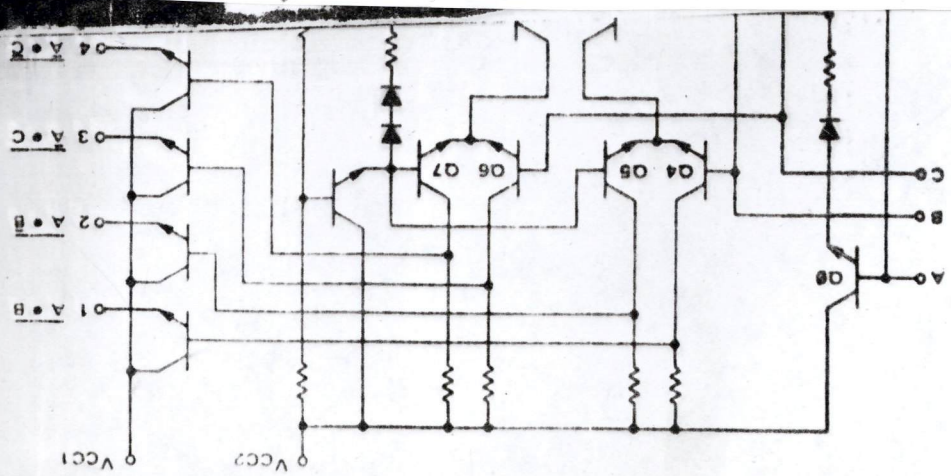


Figure 34 - NAND Gate Logic Symbol and Truth Table

The upper symbol is the NAND (Negated AND) and the lower symbol is the NOR (Negated OR). In the NAND gate the inputs are true when high. In the NOR gate the input circles indicate that those inputs are true when low.

The D type flip-flop is shown in Figure 35. The flip-flop assumes the state of the "D" input at the leading (positive going) edge of a clock input.

Figure 35 - D Flip-Flop

With the clock input at its normal low voltage G2 and G3 will have high outputs. With the set and reset inputs high the output gates G5 and G6 can remain as they were; that is G5 on and G6 off or vice versa. A low set input will force G5 off and its output will bring G6 on. Similarly, a low reset input will make the 0 output high and the 1 output low. The dotted lines allow low set and clear inputs to override the clock input if it should be high. Normally, S and R inputs are high, C is low and D can be either.

The clock and data circuit works as follows: With the C input low the outputs of G2 and G3 are high. A high D input will cause a low input to G1 and G3. The output of G1 will be high. If then the C input goes high the output of G2 goes low, setting the flip-flop. It also holds an input to G3 low so that if the D input should change while C is high the flip-flop output will not change. Similarly, with a low C and a low D input the output of G4 will be high causing the G1 output to be low. If then the C input goes high the output of G3 goes low, resetting the flip-flop. It also holds an input to G4 low so that if the D input should change while C is high the flip-flop will not change.

Thus, the D flip-flop has characteristics like the R-series flip-flops with D-C-D gates. Both respond to the leading edge of a clock and are insensitive to further data inputs until the clock returns to its quiescent state.

The J-K flip-flop has clock gated inputs J and K; if the J input is high at clock time the flip-flop will be set, and if the K input is high it will be reset. If both J and K inputs are high or are not connected at clock time the flip-flop will be complemented. The schematic and logic symbol are shown in Figure 36.

Figure 36

APPLICATIONS;

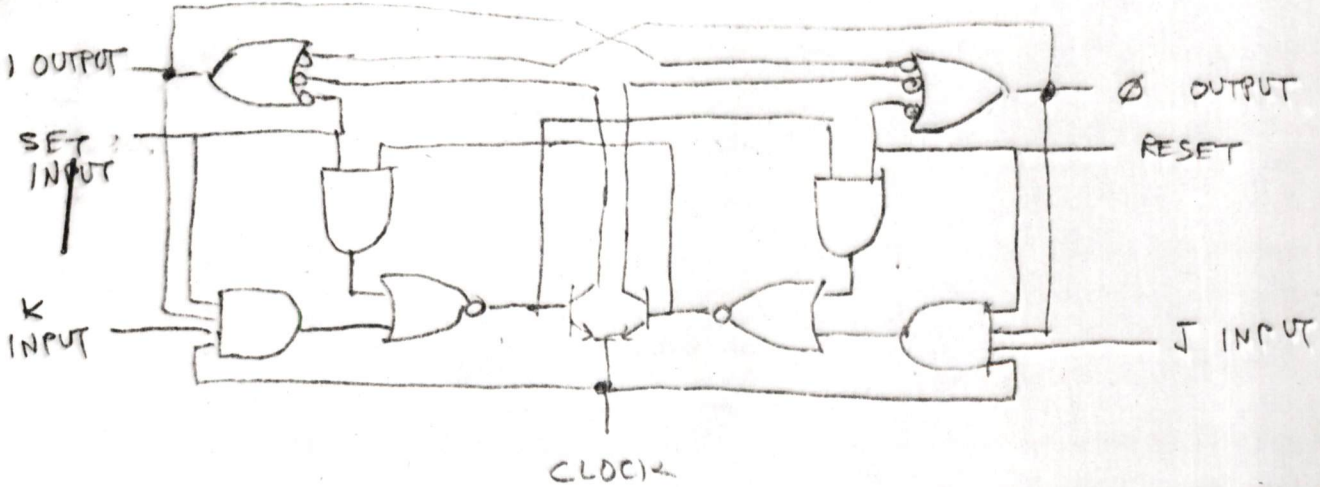
The first generation M-series modules were used in a redesign of the PDP8 called the PDP8/I. The KI10 processor used in the PDP10 was then designed from higher speed circuits using the 74H00 series of IC's (the first M-series modules used the 7400 series). 74H00 IC's are similar to the 7400 except that they use more power and are faster. The first PDP11 was built using 7400 series IC's (PDP11/20). To achieve higher density, extended length quad modules were used. Modules had been made in quads before and separated into 4 singles or 2 doubles after assembly and had a depth of 5 inches. The PDP11 modules had a depth of 8.5 inches and were quads as one module, measuring 8.5" x 10.4". The back plane had an array of connectors so that 4 quad modules could be plugged into 2 aligned connector blocks.

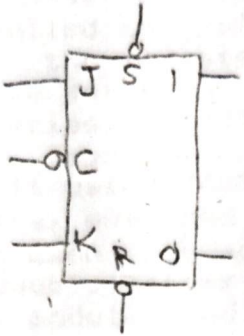
In 1970 the PDP15 was built, a generation that started with the PDP4 (System Modules), the PDP7 and PDP9 (B-series). The Schottky IC's were used. The switching speed of Schottky circuits are so fast that 4-layer boards had to be used; inner layers of power and ground provided shielding.

In 1972 a new PDP10 processor, the KL10, was built using Motorola MECL 10,000 series current switching non-saturating logic. This line of circuits is like an integrated circuit version of the earlier DEC VHF 8000 series circuits. The basic gate is,shown in Figure 37.

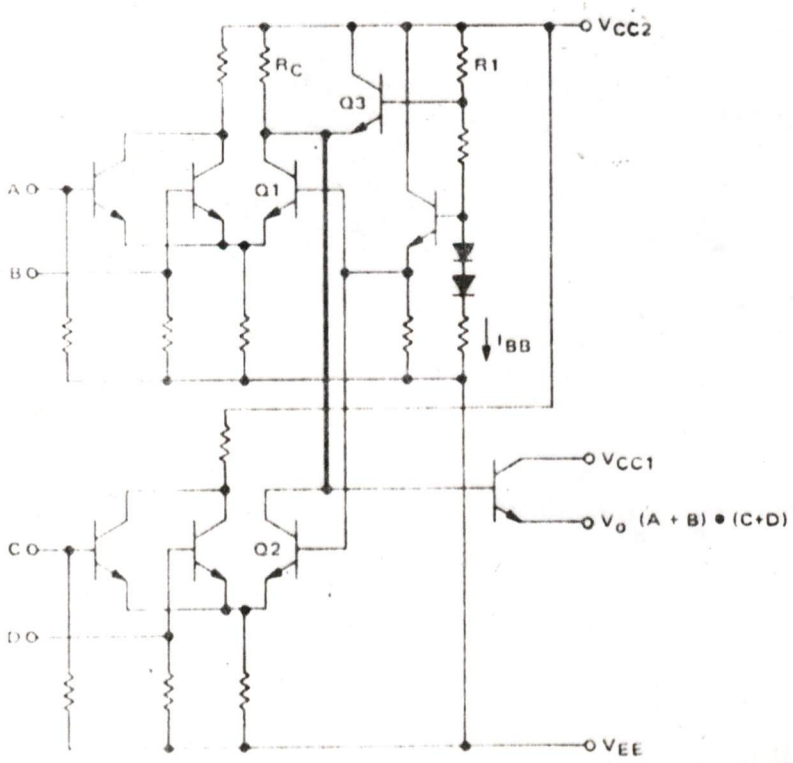
Figure 37 - MECL 10,000 Basic Gate

Q6 has a temperature compensated internally generated reference voltage on its base of -1.3 volts. The outputs drive 50 ohm terminated transmission lines returned to -2


1 OUTPUT
SET INPUT
K INPUT
Ø OUTPUT
RESET
J INPUT
CLOCK


J
S
1
C
K
R
0

15: Collector Dotting



volts. There is a complementary pair of outputs so that the circuit is both an OR and a NOR gate. At 25 degrees Celsius the upper level will be between -0.81 and -0.96 volts while the lower level will be between -1.65 and -1.85 volts. The circuits are so fast that multilayer circuit boards were necessary with power and ground on the inner layers.

More complex gate structures can be built as shown in Figures 38 and 39. A master-slave type D flip-flop contained a total of 32 transistors and 7 diodes.

Figure 38 - Series Gating

Figure 39 - Collector Dotting

By 1973 the hex module (8.5 x 15.6 inches) was being used,

plugged into three properly aligned connector blocks. In 1977 the first VAX computer, the 11780, used 12" deep hexes. All of the above developments were in the M-series.

An evolution in circuits has continued as technology grew. As integrated circuits became more powerful by reduction of the size of their active elements each re-design of an old computer became smaller, faster and generally lower cost than its predecessor. The PDP11 family used LSI (Large Scale Integrated) circuits in the LSI11, where the processor and some memory all fit on one quad (10.5" x 8.5") board.

The chart below shows the number of circuit types that were started each year from 1957 through 1977.

JOHN

RLB's latest 2/24/78

Retain this copy for art Jean.

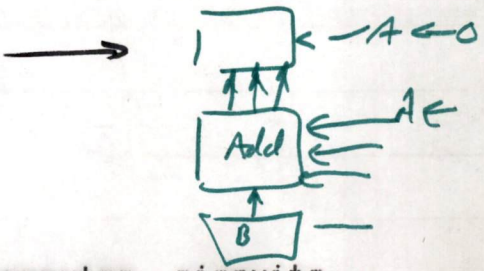
IN THE BEGINNING
1957-1959

THE PACKAGES:

DIGITAL TEST EQUIPMENT (LAB MODULES)

Digital Laboratory Modules are fully coordinated solid state computer circuits used to develop and test digital circuits, components and systems. All logical signals are available on the graphic front panels, and logical interconnections are made with stacking banana-Jack patch cords. Units in all three speed lines are directly compatible. The circuits are mounted in aluminum cases measuring 1-3/4 by 4-1/2 by 7 inches.

100 Series: up to 5 MHz
3000 Series: up to 500 KHz
5000 Series: up to 10 MHz



SYSTEM BUILDING BLOCKS (SYSTEM MODULES)

Digital System Modules are solid state computer circuits used in the design and construction of digital systems. A wide variety of fully coordinated units is available in three directly compatible speed lines. Each module is mounted in an aluminum frame measuring 1/2 by 4-1/2 by 6 inches. Up to 25 modules can be inserted in a standard 19-inch mounting panel. All connections are made through 22-pin Amphenol plugs.

1000 Series: up to 5 MHz
4000 Series: up to 500 KHz
6000 Series: up to 10 MHz

THE CIRCUITS:

The point of departure for the circuits was the Lincoln Lab TX-2 computer*. All of those basic circuits were used except the emitter follower gates which were not short circuit proof. Short circuit proof circuits are essential with patch cord interconnected circuits (Lab Modules) and are desirable features in System Modules where a slipping scope probe or clip lead can accidentally short out circuits during debugging.

*see page

THE TRANSISTOR INVERTER

Most logical operations are performed with saturating PNP germanium transistor inverters. When a transistor is turned completely on or "saturated," the collector is practically a

short circuit to the emitter of the transistor. If the emitter is at ground in this condition, the output from the collector will also be at ground.

When a transistor is turned completely off or "opened," the collector-to-emitter path is an open circuit. If the collector is connected to a clamped load resistor, the collector will be at -3 volts.

Binary
0 010 110
1 110 110

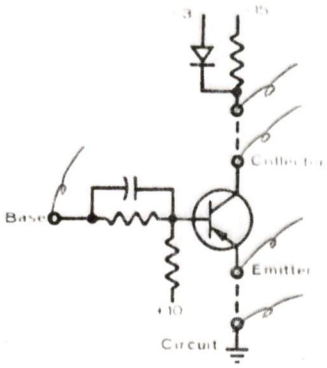


Figure 1

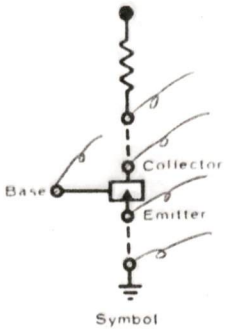


Figure 2

Figure 1 is a schematic drawing of an Inverter and Clamped Load Resistor. The capacitor shunting the input resistor is used to provide overdriving current to the transistor during input level changes, thus switching the transistor much more rapidly. The resistor to +10 volts biases off the transistor to protect against noise voltage. The load resistor is clamped to -3 volts with a diode so that, when the transistor is off, the output signal is always at -3 volts regardless of the loading on the inverter output.

To simplify logic drawings, the symbology of Figure 2 is used. When the input is negative, the output is "shorted" to ground. When the input is positive or at ground level, the transistor is open circuited and the output, if connected to a clamped load resistor, is at -3 volts.

DEC LOGIC

Dual-polarity level logic is used. The "logical" voltage levels are -3 volts and ground. Correspondence between the logic state, ONE or ZERO, and the voltage levels of -3 and ground is indicated at each point in the "logic" drawing by a diamond. This diamond defines the necessary voltage level for the action desired. A solid ◆ diamond denotes a -3 volt level for assertion and a hollow ◇ diamond denotes a ground level for assertion.

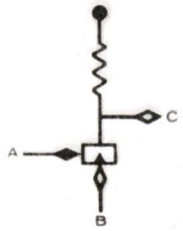
With these symbols, the logical designer is able to produce in one step a logic drawing which can be directly implemented with DEC Modules. This method also allows a combination of amplification and gating without added inversions, usually necessary if a single logic state is always associated with a single logic voltage level.

The illustrations below show how this method is used to form an AND gate or an OR gate from single inverters. The inverter serves as an AND gate when the definitions are:

A = 1, if negative (-3V)

B = 1, if ground

C = 1, if ground

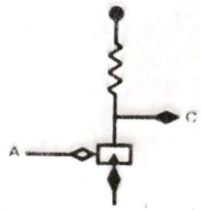


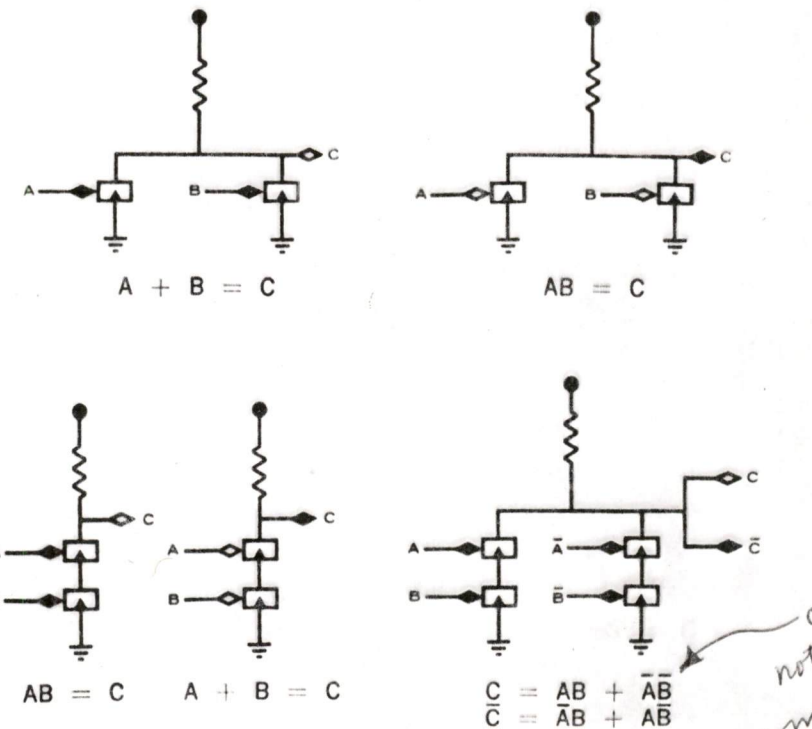
AB = C

The same inverter serves as an OR gate if the definitions are:

A = 1, if ground

B = 1, if negative





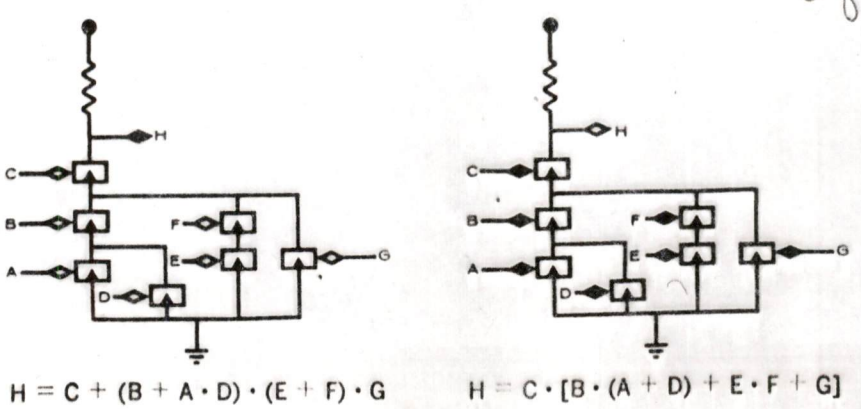


Figure 3 Common AND and OR gate possibilities

H = C+(B+AD)(E+F)G H = C[B(A+D)+EF+G]

Figure 3: Common AND and OR gate examples

After the desired logic has been performed with level gates in series and parallel combinations, the results can be sampled and read into a flip-flop or other active element with a DEC Standard Pulse. This may be accomplished by applying the conditioning level to the emitter of an inverter and the sampling pulse to the base of the same inverter. The collector of this inverter (or the collector of a diode gate used in the same manner) can be used to drive one flip-flop or other active element. The sampling pulse must be narrower than the delay of a buffered flip-flop (see flip-flops below).

DIODE LOGIC

Diodes may be added to the inverter input in order to form an AND or an OR gate. The circuit in Figure 4 illustrates a diode gate which can serve as a NOR gate for negative signals or a NAND gate for ground signals. When both A and B are at ground, the positive bias on the base assures that the transistor will be cut off and that the collector of the inverter will be at a negative voltage. If either A or B is unconnected, the circuit will act as a simple inverter.

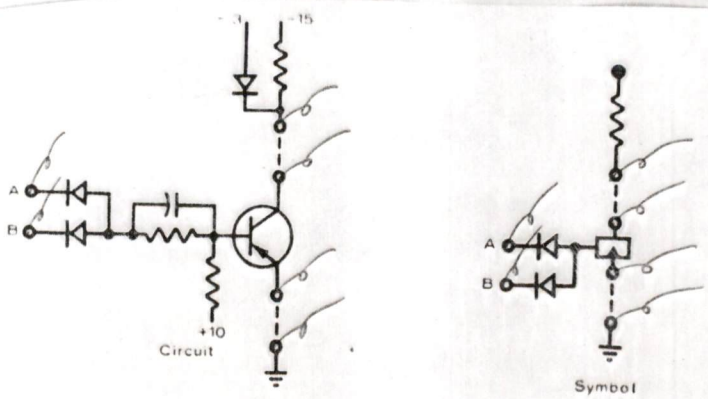


Figure 4

Figure 4

Figure 5 shows a similar diode gate with the diodes in the reverse direction and a negative bias voltage. This circuit will operate as a NAND gate for negative signals and a NOR gate for ground levels.

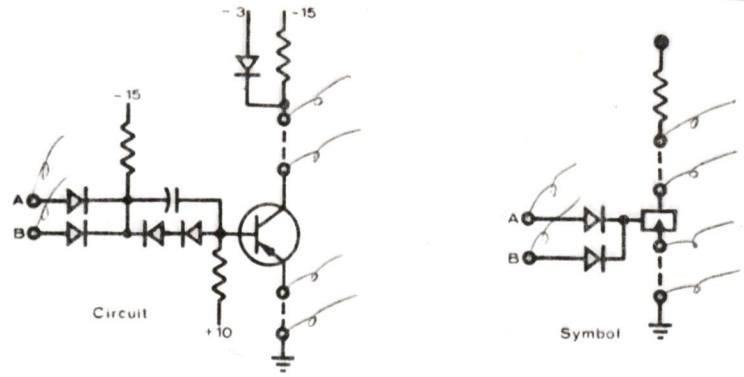


Figure 5

Figure 6 shows a group of two input negative AND circuits which are NORed together.

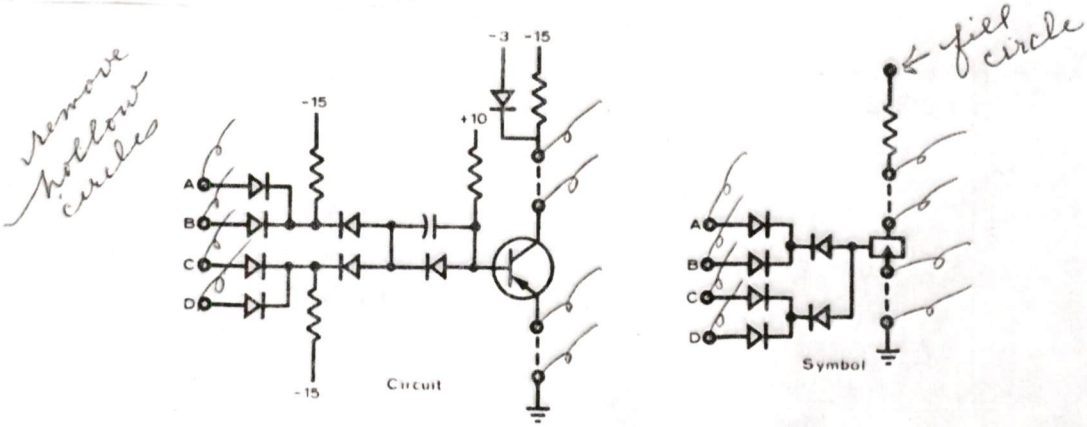


Figure 6

All Diode Gates are permanently connected to a transistor inverter which re-establishes the voltage level after every gate. Thus, Diode Gates may be cascaded indefinitely.

PULSE AMPLIFIERS

Pulse Amplifiers are a powerful logical element because they not only amplify and standardize the shape of pulses, but also gate pulses. When the same logical gating is to be done on a whole register of flip-flops, it often can be done once before the pulse amplifier drives the register.

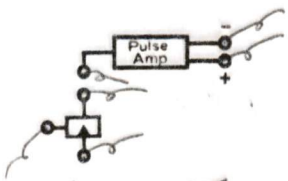


Figure 7

Figure 7

The output of the pulse amplifier comes from a pulse transformer, which has both terminals available so that either positive or negative pulses may be obtained, depending on which terminal is grounded. Positive pulses

are used to direct set and clear flip-flops without inverters. Negative pulses are used for setting, clearing and complementing with inverters. A negative pulse is indicated by a solid triangle, a positive pulse is indicated by a hollow triangle.

FLIP-FLOPS

If two grounded inverters are interconnected, as in Figure 8, a bi-stable "flip-flop" is obtained. When one side is cut off, its output is negative. This holds the other side on, which, in turn, holds the first side off.

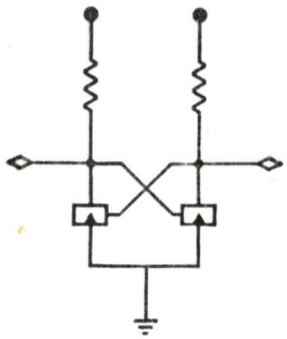


Figure ~~9~~ 8

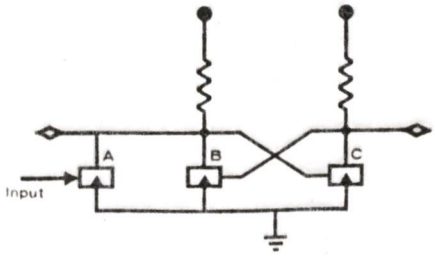


Figure ~~10~~ 9

If a grounded inverter A is connected to the off side B of the flip-flop in Figure 9, the state of the flip-flop can be changed by pulsing the base of transistor A with a negative signal.

It is desirable to have flip-flops with very low output impedance so that they can drive many other circuits. For this reason, many DEC Flip-Flops have buffer amplifiers on each side of the flip-flop. A simple network is placed between the flip-flop in Figure 10 and the output amplifiers, which delays the change in the output. When the flip-flop is changed with a standard pulse, this delay is long enough so that the output does not change until after the pulse is gone. This allows flip-flops to be sensed while they are being changed, which makes shift registers, counters and adders relatively simple.

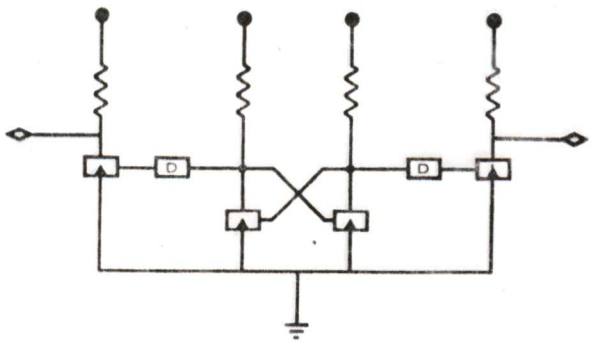


Figure 10

The symbol for a flip-flop is shown in Figure 11. In order

to set the flip-flop to the desired state, the inputs at the bottom are "shorted" through inverters to ground. When the input on the ZERO side has been shorted to ground, the ZERO output is set to the -3 volt level and the ONE output is at ground. This is defined as the ZERO state. Similarly, when the flip-flop is in the ONE state, the ONE output is at -3 volts and the ZERO output is at ground.

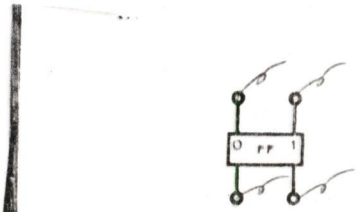


Figure 12 11

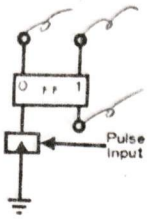


Figure 13 12

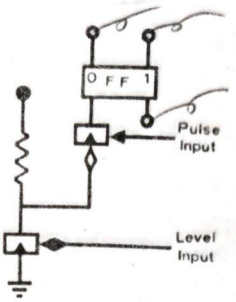


Figure 14 13

Figure 11 Figure 12 Figure 13

Flip-flops are changed by momentarily shorting an input to ground, as shown in Figure 12. The input to the inverter is a DEC Standard Negative Pulse of 2.5 volts amplitude relative to ground.

To gate information into a flip-flop, two inverters can be connected in series, as in Figure 13. If the level input is at ground when the upper inverter is pulsed, the flip-flop terminal will not be shorted to ground; but if the level input is at -3 when the negative pulse arrives, the input is shorted and the flip-flop is cleared.

When the Flip-Flop has buffer amplifiers, it is permissible to use the buffer as the level gate. This added flexibility is useful since it allows gating into a flip-flop with only one inverter.

Figure 14 is a "Jam transfer" gate employing Buffered Flip-Flops. The contents of flip-flop A can be "Jammed" into flip-flop B with a single pulse independent of the previous state of flip-flop B.

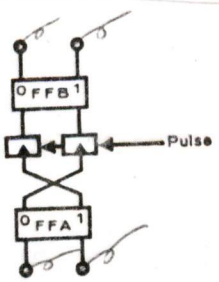


Figure 15 14

Figure 14

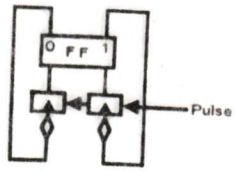


Figure ~~17~~ 15

Fisure 15

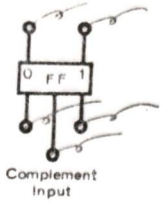


Figure ~~18~~ 16

When the inverters of Fisure 15 are pulsed, the state of the flip-flop will be changed or "complemented." On some Flip-Flops this sating is done internally, and a complement terminal is brousht out, as in Fisure 16. There is also a complement output terminal P which will deliver a DEC Standard Negative Pulse every time the flip-flop complement input is pulsed. This P pulse output is useful in counters and adders.

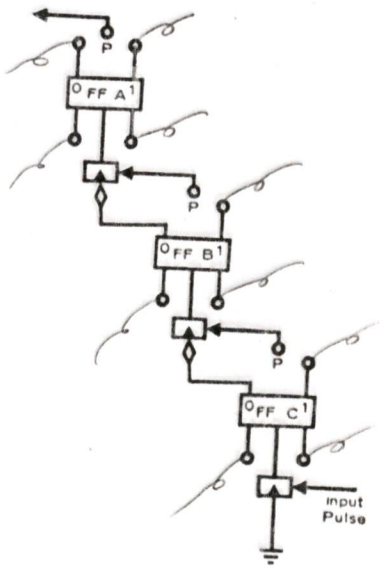


Figure ~~19~~ 17

A typical counter arrangement using Complementing Flip-Flops is shown in Fisure 17. The pulses beins counted enter on the right. They always complement flip-flop C and senerate a standard pulse at P. This P Pulse complements flip-flop B when flip-flop C holds a ONE. When this P Pulse sets throush the sate and actually complements B, it will senerate a P Pulse out of B. The process is continued down the lensth of the counter. Only one inverter and one flip-flop are needed for each bit in the counter.

System Module buffered flip-flops also have direct clear and set terminals which allow flip-flop resisters to be set or cleared without the use of pulse sates on each flip-flop. The input to these terminals is a DEC Standard Positive Pulse of 2.5 volts amplitude relative to sround. These pulses can be produced by DEC Delays, Pulse Amplifiers, Clocks, and Pulse Generators.

Delay Units are flip-flops which have only one stable state. When the input terminal is "shorted" to ground by a gated standard pulse, the level output terminal will switch from its normal ground level to the -3 volt level for an adjustable fixed period of time. A standard pulse will be produced at the pulse output when the level output returns to its normal 0 volt condition. The pulse output comes from a pulse transformer which has both terminals available so that either positive or negative pulses may be obtained, depending on which terminal is grounded. Typical waveforms for a delay unit are shown in Figure 18.

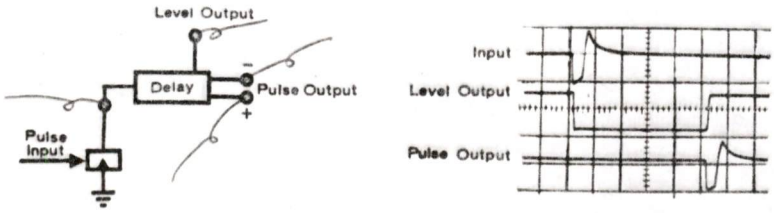


Figure ~~21~~ 18

Figure 18

There were a relatively small number of types of modules available in each of the Lab Module Series. For example, in the first product line, the 100 series:

103: 6 inverters
110: 2 6-input negative diode NOR's
201: 1 buffered flip-flop
302: 1 one-shot
402: 1 clock pulse generator
406: 1 crystal clock
410: 1 Schmitt circuit pulse generator
501: 3 level standardizers
602: 2 pulse amplifiers
650: 1 tube pulser (15 volt 100 nsec pulses)
667: 4 level amplifiers (0 to -15 volts)
801: 1 relay

By contrast there were many System Module types developed. With their higher packing density, lower cost and fixed back panel wiring they were used for computers, memory testers, and other complex systems of logic. Core memory designs required high pulse current driving modules and sense amplifiers. The growth of the number of types of various module lines can be seen in figure .

CAPACITOR-DIODE GATE AND UNBUFFERED FLIP-FLOPS 1960 -

The transistor inverter, buffered delayed flip-flops and pulse logic were the best choice for 5 and 10 MHz logic. For low-speed logic, however, the C-D (capacitor-diode) gates and unbuffered flip-flops were attractive due to the greater density and lower cost that could be achieved. These techniques were only used in

System Modules, principally in the 4000 series.

A negative capacitor-diode gate is illustrated in Figure 19. With both inputs at ground for several time constants to allow the capacitor charge to be 3 volts a negative level change or negative pulse at the base input will cause a positive pulse to appear at the output. Such gates could drive the direct set of any flip-flop that required a positive pulse, and were built into some unbuffered flip-flop inputs to be used for shifting, counting, etc.

A positive capacitor-diode gate is illustrated in Figure 20. With the level input at -3V and the pulse input at ground for several time constants to allow the capacitor charges to become stable a negative level change or a negative pulse at the capacitor input will cause the transistor to conduct, grounding its output for an amount of time determined by the gate time constant or input pulse width, whichever is shorter. Such gates were not built into flip-flops but could be used to set and clear unbuffered flip-flops by momentarily grounding the correct flip-flop outputs.

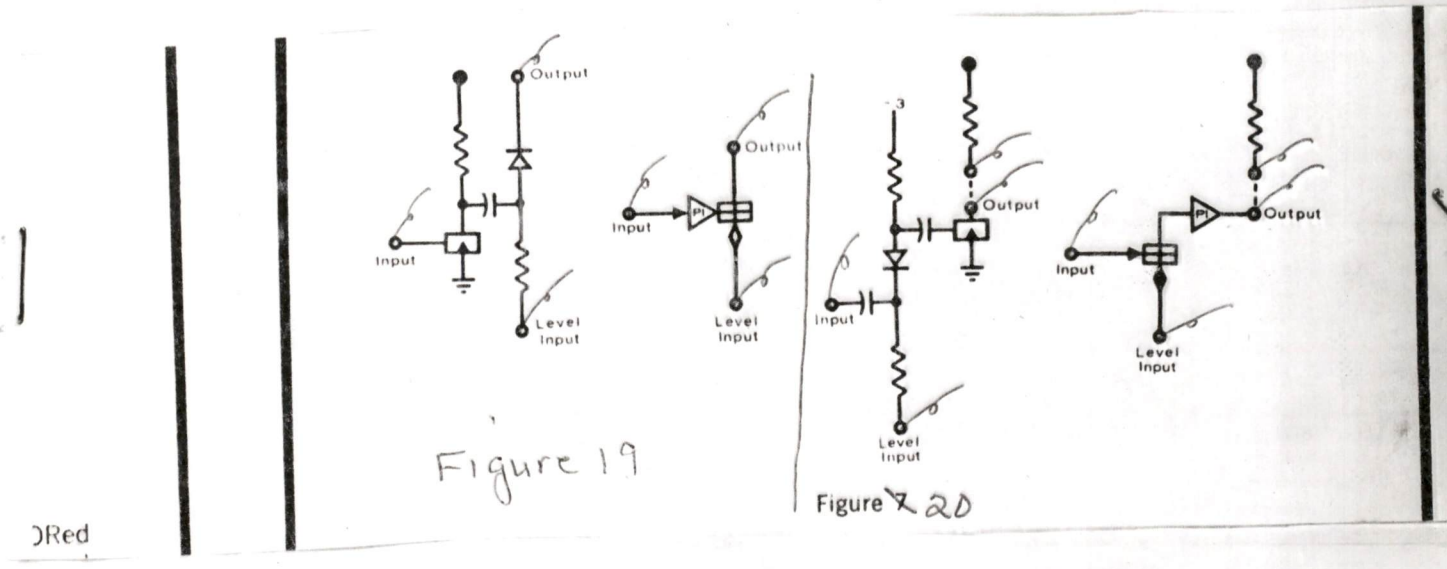


Figure 19

Figure 20

Circuit Symbol

Negative capacitor-diode gate

Figure 19

Circuit Symbol

Positive capacitor-diode gate

Figure 20

The principal advantages of the C-D gates are:

1. The level gate input, the resistor, presents no DC load.

2. The RC time constant of the gate requires that the conditioning level be present a certain amount of time before the pulse occurs. This introduces a delay between the application of a new gate level and the time the gate is conditioned, and allows the sampling of unbuffered flip-flops at the same time the flip-flop is being changed.

3. The capacitor-resistor combination differentiates a level change. This is useful when it is desired to use a level change to trigger a unit which normally operates from a pulse.

A full durati DEC Standard 0.4 microsecond Pulse can be produced from a level change using a Type 4604 Pulse Amplifier as

a standardizer. The Type 4603 may be used if the input is driven by a Negative Capacitor-Diode Gate when a feedback loop is connected as shown in Figure 21.

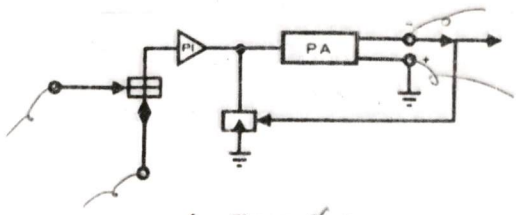


Figure 8 21

Figure 21

ADDER APPLICATIONS:

The adder illustrated below is built with inverter pulse logic techniques.

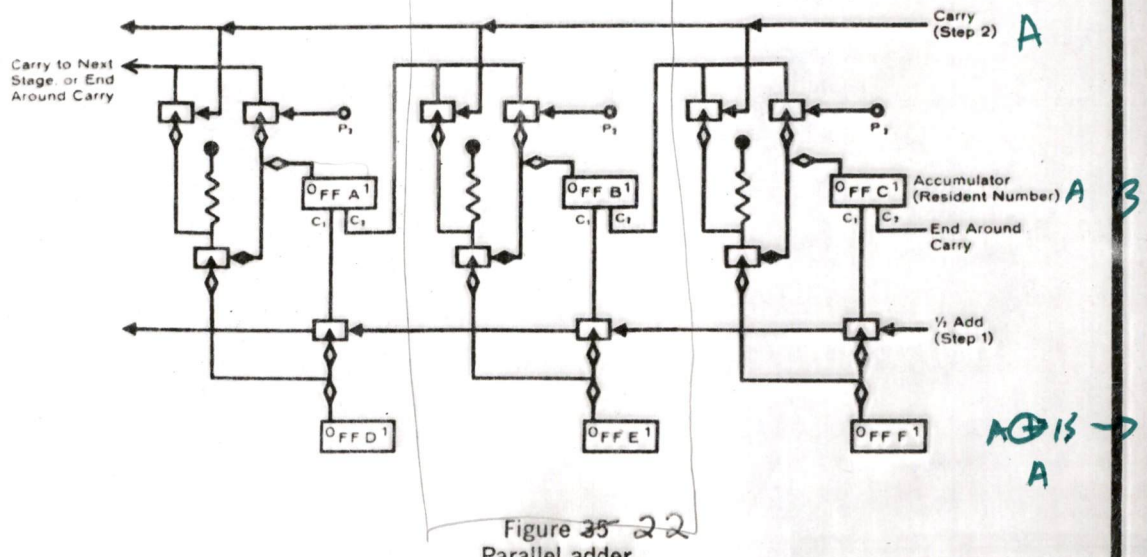


Figure 35 22
Parallel adder
(Accumulator Flip-Flops DEC Type 1201 or 4201)

Figure 22
Parallel adder
(Accumulator Flip-Flops DEC Type 1201 or 4201)

The first step is half-add. Each digit of the accumulator is complemented if the corresponding digit of the incident number is a ONE.

The second step is a carry. A carry will be generated if a digit in the accumulator is ZERO and the corresponding incident number digit is a ONE. The carry will be propagated if an accumulator digit is a ONE and it also receives a carry pulse from the next less significant accumulator digit.