PACKAGING 12/1/77

Figure 1 suggests that packaging is a completely recursive process where boxes (packages) are placed within boxes (packages) on an indefinite basis. Packaging is ~~just~~ iterative, ~~and~~ not recursive, because for each level (IC, module,...cabinet, room) of packaging, a completely different design problem exists. However, for a computer system consisting of a set of components, each component can be thought of as a system itself which in turn is decomposed into lower level components. The computer systems we describe herein can be nicely decomposed into three to five distinct levels. At the topmost level these physical components correspond to the PMS level components from which the final computer engineer (the user/buyer) conceptualizes and builds the computer.

Packaging the electronic and electromechanical components that constitute a system at a given level consists of: interconnecting the set of the components via signal carrying links and holding (packaging) them within some basically mechanical structure such that as a unit system they carry out the objective function (i.e., meet the design specification). Figure 2 introduces a few of the packaging problem subtleties. There is some visual effect in addition to the function for which it was designed. The visual effect may, in fact, be the dominant reason (or deciding factor) in whether the object is purchased. While we are only interested here in what is basically electronic signal processing there are two side-effects: power is consumed and there is an electromagnetic interface (EMI). Power, in turn, requires cooling or heat dissipation to some outside environment by convection, radiation or conduction so that the system will ultimately not

burn up...or malfunction when stored or operated outside a limited temperature range. The EMI interface is bi-directional: signals ~~eminate~~ emanate from the package and must be controlled in order to avoid interference with the radio frequency spectrum; and other equipment broadcasts radio frequency interfering (RFI) signals which must not interfere with the package's function. In addition to cooling (or heating) other environmental constraints include humidity, air quality (dust, corrosiveness, salinity, etc.). ~~Left unsaid in the figure are the implicit costs associated with the design, and these costs mostly determine the applicability of the design.~~

While the significant price and performance gains come from improvements of semiconductor and magnetic technologies, gains are not fully realized without concomitant gains in packaging technology. The packaging of DEC computers has been generally decoupled from the logic (semiconductor) technology generations. The reader should observe that for each new generation, there are two generation steps to fully realize the gains. The first step assimilates and uses the technology in what is simply a substitution of an existing structure. The second step takes fuller advantage of the technology by appropriate packaging. This comes about from a basically conservative engineering attitude where a project tends to only concentrate on one variable at a time.

Seymore Cray*, the designer of the CDC 6600 (12/64) and 7600 (12/69) computers and most recently the Cray 1 (12/75) computer, described packaging as the most difficult part of the computers designer's job. His rule of thumb indicates that with every generation of large computer, the size decreases by roughly a factor of five--and each generation takes roughly five years.

While it is easy to understand why one of Cray's super computers is so dominated by packaging, we want to examine the effect of packaging on small computers. At the extreme, we should observe that the first hand-held scientific calculator, the HP35, was simply a new package for a common object, the calculator--which has been with us about 100 years.

Although semiconductor density was high enough to permit only a few integrated circuits to be necessary to implement a calculator, it wasn't until they were re-packaged in a particular fashion that the hand-held calculator came into existence. Currently this embodiment is synonomous with the calculator name--in the future, the calculator might take on some other form (e.g., watch, pencil, voice actuated, hearing aid, notebook).

Packaging seems to be the dominant reason for the PDP-8 and minicomputer phenomenon--although marketing, the coining of the name, and the ability to easily manufacture (also part of packaging) are alternative explanations. We believe the PDP-8 was the original minicomputer, yet its antecendent PDP-5 had roughly the same instructions set, was about the same size for a complete system with peripherals. Since the PDP-8 was packaged in a separate box which could fit into roughly 1/3 of a standard relay rack

*Lawrence Livermore Laboratory lecture in December 1974.

cabinet, it was small enough to be incorporated into other systems on a dedicated basis. Thus, it was perceived and used as a component to build other larger systems.

*Lawrence Livermore Laboratory lecture in December 1974.

because of double spacing

THE PACKAGING DESIGN PROBLEM

As we briefly mentioned above, packaging is the complete design activity of interconnecting a set of components together via a mechanical structure in order to carry out a given function. In order to package a large structure such as a computer, the problem is further broken into a series of levels each with components that carry out a given function. Figure 3 shows the hierarchy of levels that have evolved these last twenty years for the DEC computers. There are eight levels which describe the component hierarchy resulting in a computer system. For example the transistion from the second to the third generation can simply be described as adding an intermediate level to the hierarchy, which in turn minimized the need for additional circuitry at the discrete and integrated circuitry (IC) level. That is, there was a transition of taking hardware that existed at one level and agglomerating at a lower level.

For each packaging level there is a set of interrelated design activities as shown in Fig. 4. The activities (or disciplines) are almost independent of the level they are carried out, although a design activity (e.g., logical design) is often carried out (i.e., partitioned) across several levels. For some levels a design activity doesn't exist. For example, since integrated circuits operate at low voltages,there is not a safety design problem associated with IC chip design. However, since there are many circuits on a single IC and each can be operated at a special voltage, there are both power supply design and power dissipation (cooling) problems associated with IC design.

We first note (Fig. 4) that the initial design problem is to simply perform a certain function. Furthermore, performing the function causes a number of side effects that have to be solved. For example, the integrated circuits and other equipment that do information processing require power to operate. The power creates a safety hazard; and since each power supply operates at less than 100% efficiency, heat must be carried away from the power supply and the components being powered. In this way the cooling problem is created. Sometimes cooling is carried out using conduction to an outside surface so that it may be carried away by the air in a room. Mostly cooling problems are solved by convection with a fan in the cabinet by carrying air into the room so that the room is left to cope with carrying the heat away. In the process, the fans create acoustical noise pollution in the room, making it ~~difficult~~ harder for humans to cohabit the room. If the computer is used in an unusually harsh environment (dust, corrosion, etc.) then a special heat exchanger is required in order to avoid contamination of the components.

Finally, a particular package exhibits mechanical characteristics such as weight and size. These parameters directly affect manufacturing and shipment costs. They determine whether a system can be built, and whether it can be shipped in a certain size (e.g., Boeing 707 airplane) or distribution channel (e.g., parcel post or United Parcel). The dynamic characteristics determine the type of vehicle (air ride van) in which equipment must be shipped.

It is also necessary to examine the particular design parameter in order to determine whether it is a constant (meets the German VDE standard x), a

goal (cheap as possible), or part of a more complex objective function (measured in bits/sec/$ or part of a system benchmark--jobs/sec/$). Thus a system may be determined by a government standard (e.g., safety and EMI), a market consideration, a distribution channel (shipped via parcel post), a method of sales (catalog and customer installable), a competitor characteristic (e.g., no louder than x, faster than y, or cheaper than z), for a physical operating environment (dusty, hot and with high RFI).

The following table lists the various kinds of design activities and whether they are likely to goals, constraints, or part of more complex objective functions. The table also gives the dimensions of various metrics (e.g., cost, weight) available to measure the designs and many of these metrics are used in subsequent comparisons.

Table Design Activities, Metrics and Environment Setting Goals and Constraints

Design Activity	Determining Environment and [Metrics]
Primary function and performance (e.g., memory)	Market, next highest level (i.e. the consumer) of system [memory size (bits), operation-rate (bits/sec.)]
Human engineering	Human factors criteria, competitive market
Visual / Aesthetics	Market, other similar objects, the environment in which the object is to exist--usually only

single spacing

	important at outer-most level
Acoustic noise	Government standards, operating environment, market [decibels]
Mechanical	Shippability (e.g., air cargo container size, truck vibration), handling, assembly/disassembly time [weight, floor area, volume, expandability, acceleration, frequency response
EMI	
radiation input	Government standards, must operate within intended environment (e.g., high noise) [power vs. frequency] [Standard #no. ØØØ] guide standard #
Power	Operating environment, market [watts, voltage supply range]
Cooling and environment	Market, intended storage and operating environment, government standards [heat dissipation, temperature range, air flow, humidity range, salinity, dust particle, hazardous gas]
Safety	Government standards [Standard no. ØØØ]
Cost	
cost/metric	[cost/performance (its function)--cost/bit and

single spacing

ratios	cost/bit/sec., cost/weight, cost/area, cost/volume, cost/watt]
density metrics	[weight/volume, watts/volume, operation-rate/volume]
power metrics	[operation-rate/watt; efficiency = power out/power in]
reliability	[reliability--failure rate (Mean Time Between Failures, Mean Time To Repair (MTTR)]

Given the basic design activities, we must now examine their interaction with the hierarchy of levels (i.e., the systems) being designed (see Table 00). Here we look at each level, and discuss the interaction of the design activities and with other design activities (e.g., function requires power, power requires cooling, cooling requires fans, fans create noise and noise requires noise suppression).

Table Interrelationship of Hierarchy of Levels and Design Activities

Activity \ Level	Chip	IC	Module	Backplane*	Box*	Cabinet	Computer Systems
Functional components	logic ---------->			spatial	what	configura-tion of options	selection of right (user is designer)
	electrical circuit design		physical layout	physical layout	will fit and operate	boxes, what configs. will operate	
	physical layout						
Human interface						location of console, size for use	placement for use
Visual					somewhat	determines	set of cabs,

				seen, bought for integration	system appearance	attractive place to be
Acoustic			Airflow vibration	---------->	quiet for operators and users
Mechanical loading,	buildable	shippable	serviceable	---------->	floor
	signal transmission	---------->			room size
EMI	noise coupling and rejection of ext.RFI	inter/intra module noise containment and shielding	coupling, RFI	RFI containment, external RFI shield	away from rfi input (outside operating range)

Power	special on-chip supplies	dist. and regulation	dist. and regulation	control, dist. and regulation	inter-connection with computer system	by user. special power for high availability

Cooling to and other environment	chip to IC: cooling special envir.	chip to IC: module cooling special envir.	IC to cooling	module	cooling & covering	source of room air/ environment	interbox couplin

Safety	power ----------> for various systems		determines safety if used at this level	determines user level safety

Dominant design activities	circuit/ logic ---------->	mechanical, power, cooling, EMI, acoustic	configuration visual, shipping EMI, safety	user configuration design

*Can be taken together as a single level.
(Alternatively, the box level may be eliminated in large systems)

Computer Systems Level

At the topmost level is the computer system, which for the larger mini and DECsystem 10 computers in this book consists of a set of components within cabinets, which are housed in a room, and interconnected by cables which can be subjected to external environment (e.g., people walking on them). Observe that a large computer system such as the DECsystem 10 occupies a set of cabinets (Fig. 00, page 00) whereas a WPS78 word processing system is either only one or two cabinets (see Fig. 00, page 00) ~~depending on whether its printer is present~~. The functional design activity is the selection and

interconnection of the cabinets, with a basic computer cabinet holding processor, memory, and interfaces to peripheral units. Disks, magnetic tape units, printers, and terminals occupy free standing cabinets. The functional design is usually carried out by the user and consists of selecting the right components to meet cost, speed, number of users, data-base size, language (programming), reliability and interface constraints. Aside from the functional design problem, cooling and power design are significant for larger computers. For smaller computers accessibility, acoustic noise and visual considerations are significant because these machines become part of a local environment--and must "fit in".

Cabinet Level

The ultimate person responsible* for a computer system takes as given, the collection of computer system components (the cabinets) and connects them to form a system as described above. For the hardware computer system designer, the component associated with the cabinet is often his largest system. For example, the central processor designer is often responsible for primary memory and interfaces to peripheral equipment. This functional design insures that the various components (i.e., boxes) that make up a cabinet level system will operate correctly when interconnected. Since the cabinet is the lowest level component that most users interface to and observe, the physical design, visual appearance, and human factors engineering are also dominant design activities. Safety and EMI characteristics are also important because the cabinet also serves as last place for shielding. Cooling and power distribution can be a problem

within cabinets since a number of different boxes may cohabit a cabinet. Thus there may be thermal and EMI noise pollution when box components interface poorly. The mechanical structure of a cabinet is responsible for maintaining its physical integrity when shipped.

Box Level

Box level functional design consists of taking one or more backplanes, the power supplies for the box and any user interface such as an operator's console and interconnecting them mechanically. The PDP-8 is the original integral box level design (see Fig. 00, page 00). It should be noted that when system are not distributed at the box level, then no separate box is required and backplanes are mounted directly in a cabinet; hence box and backplane design are merged as one. In a similar fashion, when only a single backplane is used, it is hard to separate the design associated with the box and backplane. In this way, power, cooling the backplane to hold the modules and the box to cover and support the other components becomes a single design.

If systems are sold at the box level, then the visual characteristics may be important, otherwise, the design is basically mechanical and consists of cooling, power distribution, and control of acoustic noise. The structure must be basically quite sound in order to provide for shipment.

*A significant computer engineering task performed mostly by the user/buyer

Backplane Level

This level of design (when we separate it from the box level design) is just the final level of interconnection for the computer components that are designed to stand alone (e.g., a basic computer disk, terminal). Backplane design is part of the computer's logical design. Figure 00, page 00 shows the Omnibus backplane for PDP-8 and how it is used to interconnect the basic components. Secondary design activities include holding, powering and cooling modules so they may operate correctly. Since the signals are transmitted on the backplane then there is an EMI design problem. For industrial control systems whose function is to switch power (see PDP-14 on page), then additional safety problems are created.

future generations
layout will
encompass box & card

Module Level

In the third and fourth generations, module level design is one of the physical layout design problems associated with logical design. In the second generation module level design (see Fig. 00, page 00) was a circuit design activity taking discrete circuits and interconnecting them to provide a given logic function. Chapter 00 describes the electronic circuit designs of the second generation. Now, this interface between circuit and logical design is within a chip level design. This shift in roles (function) will be described below on the section discussing the interrelationship between the technology generations and packaging. The integrated circuits that perform the functions are assigned to different positions on the module. Note in a recent implementation of the LSI-11, a processor with 32 Kbytes of memory is packaged on a single double sized

module (see Fig. 00, page 00). Since module level design is basically electronic, we note again that power, cooling and EMI considerations dominate.

[Need brief description of ceramic, plastic DIP, TO-5, flat pack alternatives to DIP]

Integrated Circuit Package and Chip Level

Since the Integrated Circuit is often identified as a package with a configuration of two rows of pins, called the Dual In-line Package (DIP (see Fig. 5 00, page 00) we synonomously equate the IC package with DIP. The part of the semiconductor wafer, called a chip (see Fig. 00, page 00) is actually the Integrated Circuit. Thus, for every DIP there is currently only one chip; and since we equate DIP to IC, we can discuss the IC and chip as a single level. In the future, we might expect multiple chips to be packaged within a single DIP, creating a different design problem at the DIP (IC) and at chip levels. Figure 5 shows a single DIP with two chips as used by the LSI-11.

Logical design is a part of the functional design problem at the chip level. The task is to supply a terminal behavior that can be used at the next (module level) and depending on the technology generation this function can vary from a simple gate (in the early third generation) to a full computer (late in the fourth generation). A completely correlated design activity is the circuit design with transistors; as such, the logician can interconnect the various transistors in accordance with a well established set of rules so that the circuit will carry out the required logical function. The physical assignment of circuits (functions) to geometry forms the remaining part of the functional design.

Other design activities at this level include generic to electrical signal processing: power, heat dissipation and EMI. Since some ICs are designed to operate in hostile environments, there is a considerable mechanical design activity associated with packaging, interconnection and manufacturing.

THE PACKAGING EVOLUTION

Figure 6 shows how correlation of packaging and the computer classes with the computer generations (and time). For each new generation, there is a short, evolutionary transition phase, but ultimately, the new technology is repackaged in such a way that a complete information storage or processing component (e.g., bit, register, processor) occupies a small fraction of the space and takes a fraction of the cost it did in the former generation. We can observe from the lowest level processing that quite discrete events mark the generation starting from 1 bit per vacuum tube chassis in the first generation and evolving to a complete computer on a single integrated circuit chip to mark the fifth generation. It is also worth noting that in the first generation, a chassis permanently mounted in an equipment bay was used whereas later on, as computers were built on a production basis, modules were created which were significantly smaller, more producible and removeable for servicing.

Although it is difficult to do precisely, the second packaging time line indicates the transition in package size for a basic processor and primary memory. For the minicomputer we use Whirlwind (perhaps overzealously) which is roughly the size and power of the LSI-11 (a four chip, 16-bit

processor). Whirlwind occupied a complete building and the processor portion, a large room.

In the case of the computer classes several computers are given to mark the various technologies and sizes. Here, it is clear that the package plays a significant event in the determination of the new classes. Note the super, mini, micro, calculator, and terminal lines.

It is difficult to be too precise about the class distinctions as a given computer class can neither be precisely defined in price nor performance terms; we mostly argue that the price, packaging hierarchy and market distribution structure determines the computer class. In the following table we give the packaging hierarchy with time for what might roughly be considered to be a minicomputer.

Table Physical Structure Packaging Hierarchy versut Technology Generation for Roughly Constant Performance Computers

clean up

			cabinet	cabinet
		room	box(es)	?
building	room	cabinets	backplane	module(s)
rooms	cabinets	backplanes	modules	integ.ckts.
bays	?	module	integ.ckts.	chip
chassis	chassis	disc.ckts.	chip	
disc.ckt.	disc.ckts.			

early first	late first	late second	late third	early fourth
(e.g. Whirlwind)	?	(PDP-1)	(PDP-8/E)	(CMOS-8)

Note: The line shows what is required for the processor part only. Only one each (e.g., 1 room...1 integrated circuit) of next lowest level component is required/processor.

In a similar fashion, we can observe how a particular computer component, now called the Universal Asynchronous Receiver-Transmitter (UART) has evolved with time in the following table.

Table __ Packaging Hierarchy Evolution for Universal Asynchronous Receiver Transmitter (UART) Telegraph Line Controller

backplane modules	2 modules	module		
discrete circuit	discrete circuit	IC chip	IC chip	chip area
early second	late second	early third	late thrid	late fourth

This logic carries out the function of interfacing to a communications line carrying serial data which is encoded by a DC level to denote a 1 or 0 and transforming the data to parallel on a character by character basis for entry into the rest of the computer system. The UART has three basic components: the serial/parallel conversion and buffering; the interfaces

to both the computer and to the communications lines; and the sequential controller for the circuit. The preceding table shows the evolution of the UART packaging hierarchy with time.

The UART is probably the first fourth generation part computer component, since it is somewhat less complex than a processor, yet large enough, identifiable with a clean, standard interface.

Of historical note, we feel that DEC played a significant part in the development of the UART technology. With the PDP-1, the first UART was designed using 500 Khz systems modules (see Fig. 8). The PDP-1 was used in a message switching application as described in chapter 00. We called the interface a line unit, and it was subsequently repackaged in the late second generation to be on two extended systems modules (see Fig. 9). The UART function was built into the PDP-8 using programming (see page 00). Late in the third generation (or at the beginning of the fourth generation) we were able to develop a two chip UART, and ultimately one that occupies a single chip; this, subsequently evolved to become a standard IC. It was used in the PDP-11 DL-11 communications line interface module most recently (see Fig. 10).

Currently a single chip (Fig. 11) can interface to a computer bus, handle both the receiver and transmitter functions, and have options for various line protocols and speeds.

THE DEC COMPUTERS PACKAGING GENERATIONS

With this general background on packaging, we can examine the DEC packaging evolution more specifically. Figure 3 gives the general archetype of the packaging structure and DEC, but specific schemes have been used at different generations. Figure 12 shows how the hierarchies have changed with the technology generations. The figure is segmented into the different product groupings. A product is identified as being at a unique level if it is sold at the particular packaging level. Note that with time, lower level components are available for use within other systems and different packaging hierarchies. The first computers (i.e., PDP-1 to PDP-6) were sold at the cabinet level as complete hardware systems. The PDP-8 was significantly smaller and sold at the mechanical box level so that it could be incorporated in other hardware systems and within other packaging hierarchies (e.g., as part of an industrial control system, instrumentation for a submarine). For smaller systems, a box level system often sufficed. Note that the PDP-8 was also available at the cabinet level for a complete system.

Subsequently the systems evolved to be available down to the backplane level with the LSI-11, and currently to the module level for the PDP-8, as embodied in the CMOS-8. The following tables expand on Fig. 12 and give the components, the interconnection scheme and the mechanical structure for various members of family.

The following table shows the original packaging hierarchy for most of DEC's second generation computers, which used a relatively common packaging scheme based on the PDP-1. The most significant change occurred in the late second generation when Flip Chip modules (see Fig. 12) were introduced

so that backplanes could be wire wrapped automatically, enabling lower cost and greater scale production. Figure 12 shows:

Table Physical Structure Hierarchy for Second Generation Cabinet-Held Computer Systems (1, 4, 5, 6, 7, 9, KA10, LINC, 12)

	computer	
cables	cabinets*	floor/room
int.cables	backplane(s)	cabinet frame
soldered wires**	module***	backplane, connect
PCB etch	discrete ckt.	PCB
(interconnect0	(component)	(holding structure)

*single cabinet pair for PDP-5

**changed to wire wrap after PDP-6

***originally called systems modules, and changed to Flip Chip modules after PDP-6

With third generation IC technology, another packaging level was also added. In the case of DECsystem 10 and the 18-bit family, these computers were not available as boxed components. In chapter 00 we discuss how the unavailability of "boxed" 18-bit computers may have caused their demise. Also of significance was the packaging of later third generation computers (past the 8/I and 8/L) to the M-series Flip Chip modules to reflect the change in logical design with ICs. In all recent computers the module is treated as part of a single monolithic logical design, and partitioning (assignment of particular functions to physical components across multiple

levels) is across the IC, module and backplane levels. This design activity is also shown in Table 00.

Table Physical Structure Hierarchy for Third Generation Box-Held Computers (8/I, L, E, F, M, A, 11/04-11/70)

				cabinet	
	box ---------->		int.cables	boxes	cab.frame
wire wrap bp.	module	box, etc.			
PCB etch	ICs	PCB			
Wire board	chip	DIP			
(interconnect)	(component)	(holding structure)			

Computer-in-a-box Computer-system-in-a-cabinet

This change to wire wrap technology also enabled the box level production of computers as shown in the following table for PDP-8, LINC-8 and the 8/S. Here, the changes to wire wrap and two level (box and cabinet level) products is clear.

Table Physical Structure Hierarchy for Second-Generation Box-Held Computers (8, LINC-8, 8/S)

				cabinet	
	box ---------->		int.cables	box	cab.frame
int.cables	backplanes	box			
wire wrap	module	backplane + connect			

PCB etch discrete ckt. PCB

(interconnect) (component) (holding structure)

Computer-in-a-box Computer-system-in-a-cabinet

The change to IC packaging in the third generation is whon in the preceding table for computers that are sold at the box level. Note that this set of computers includes all the PDP-8 and PDP-11 computers. In this way, the minicomputer tradition continues to be available at the box level of the hierarchy.

The LSI-11 hierarchy is represented in Fig. 12 at three levels. Although components are sold as separate modules (e.g., communications line interfaces, additional primary memory), a complete system requires a backplane, thus the lowest level for the product is the backplane. For larger systems, a power supply is combined and placed in a metal box (the 11/03), and finally a complete system such as the 11V03 is available with terminal, and mass storage in a single cabinet.

The CMOS-8 hierarchy is presented in the following table.

LSI-11?

Table Physcial Structure Hierarchy for Fourth Generation Module-Held Computer System (CMOS-8)

system in desk

terminal-->cables term.,mass store, desk

module ----------> cables modules term.

PCB etch	ICs	PCB
wire board	chip	DIP
(interconnect)	(component)	(holding structure)

Computer Module	Terminal	System

Note, that chapter 00 on the PDP-8 family describes the structure of the CMOS-8 module. Footnote 1: Here we are taking the liberty of describing a component that is not currently available as a product, except as a spare part. The CMOS-8 module[1] is a complete computer with processor, 16 Kword memory, and all the optional controllers to directly interface up to five peripheral options. For a computer packaged in this fashion, a backplane is not used, and doesn't exist at a level. The computer system within a CRT terminal exists at somewhere between a box and cabinet configuration called the VT78. the third level of the hierarchy is within 1 or 2 cabinets (i.e., a desk) complete with mass storage (i.e., two floppy disks) and a separate stand alone printer (cabinet) for letter quality printing.

SPECIFIC CABINET AND BOX-LEVEL DESIGNS

Cabinet and box-level design is perhaps the most difficult part of computer design, yet it is perceived (incorrectly) to be trivial and left till last ~~?test?~~ or because there is not a single discipline or complete set of well understood laws that govern the design. This deception arises from the fact that, on first glance, the only physical law is that not more than one thing can occupy the same space at a given time. Also, everyone has some (usually strong) feeling about what an attractive package is. However, as

---

we have tried to state emphatically in the introduction, a number of disciplines must be understood. These range from acoustical engineering to heat transfer, aesthetics, human engineering to RF engineering, and finally understanding just what function a package is to perform. In addition to this understanding, each box type requires a separate specialized manufacturing process. Obviously no one person fully understands all the disciplines necessary to correctly design a package. Herein lies the problem: Packaging is the integration of a number of separate disciplines. To be specific we want to look at the basic packaging problem by first ennumerating the possibilities for placing modules within a particular box package. By being quite restrictive, we can build a grammer ~~and~~ with six production rules sentences that describe the possible DEC boxes. ~~With these sentences,~~ even with this simple grammar, about three million possibilities still about three million possibilities exist for this; basically simple can be generated. st~~ructure~~. The large (combinatorial) number of possibilities arise from the basic size and way a box is held, the console mounting, cooling, power supply location and the way modules are mounted within the box. We can explore these possibilities by simply writing statements that express the alternatives for the separate decision dimensions.

~~SOME OF THE COMMON~~ A GRAMMAR ~~AND SYNTAX~~ TO GENERATE THREE MILLION BASIC BOX/CABINET ALTERNATIVES

Size and mounting

1. The box is	1/2	cabinet depth by	3-3/4"	high width	fixed	mounting (40)
	full		5-1/4"		slides	
			10-1/2"		right	
			15-3/4"		hinge	

				21"		left hinge

Console

2. The console is	non-existent					(14)
	simple, with power on-off for maintenance					
	for programming and maintenance					

Cooling

3. Cooling is carried out by				box-level cabinet-level	fan(s) giving	(29)
	plenum forced air	flow	normal parallel	to the module mounting axis		(8); or

cooling is carried out by natural convection with

air entry at		and exhaust	top		(21)
	bottom				
	right side		right side		
	left side		left side		
	front		front		
	rear		rear		

Power supply location

---

4. The external power supply is mounted | separately somewhere | (12)
| behind the box (attached) |
| on the back of cabinet |
| on the front of cabinet |

or; an internal supply is mounted using a mounting scheme identical to the one used by the modules; or the power supply uses a different mounting scheme and is located at the

| bottom | of the cabinet
| top |
| right side |
| left side |
| front |
| rear |

Module mounting

5. There are | zero | backplanes for mounting modules | (3)
| one |
| multiple |

6. The module pin axis is | top | mounted, oriented in | horizontal | (24)
bottom			
front		vertical	
rear			
right side			
left side			

lane with IC side facing | top |

---

bottom	
front	
rear	
right side	
left side	
	(3.9×10^6)

We can apply now given the six sentences (1 point in the decision space) that descirbes the PDP-8/A:

1. The box is 1/2 cabinet depth with 10-1/2" high with fixed mounting.

2. The console is for programming and maintenance.

3. Cooling is carried out by box-level fans giving forced air cooling flow parallel to the module mounting axis.

4. The box power supply uses a different mounting scheme and is located at the bottom of the box.

5. There is one backplane for mounting modules.

6. Modules are rear (wall) mounted, oriented in the horizontal plane with IC side facing up.

Alternatively, we can give the conventional three views of a PDP-8/A to show the location and configuration of the various box components (see Fig.

13). In this case a top view is adequate to show the configuration and air flow--although a side or front view is necessary to show the number of modules and length.

Obviously there are more than the 3.9 million possibilities that can be generated from the above grammar--although not all of these are feasible. It is important to have some way to relatively methodically examine the more common possibilities. In fact, we note that the above grammar doesn't even include the original PDP-8 package which consists of a box mounted on slides with two backplanes that can be hinged apart so as to provide access. Thus, it is not purely a box mounted on slides or a book-like structure suspended with hinges.

It is useful to look at how some of the design alternatives for a given dimension or several dimensions interact with other dimensions or effect evaluation criteria. Of all the dimensions to consider in the design, perhaps the most important is how the box (or module mounting structure) is placed in a cabinet. This placement effects air flow, shippability, configurability, cable placement, serviceability, etc. Here, we have a classical case of design tradeoffs. The scheme that provides the best metrics (i.e., packaging density (in modules/cu.in.) highest weight), has the poorest access for service, and cable connection characteristics, and only reasonable serviceability. These characteristics are given in the following table:

Table __ Fixed, Drawer and Hinged Box/Cabinet Mounting

	SERVICE ACCESS	CABLING	DENSITY	COOLING	APPLICABILITY
Fixed	Good for either backplane or module, but not both unless a thin cabinet is used	Best (i.e., shortest, and right)	Good for thin or rear cabinet PS mounting	Best (known)	Box not needed; box can be used
Drawer	One side access	Long + moves	Very high	Can be	High density, self contained
Drawer (with tilt) for service	Good	Lonter + much more moves	Very high	Cooled*	
Drawer vertical mounting modules	Very good	Longer + moves	High		
Hinged (module backplane)	Very good	Short	Medium	Good (if fans are fixed to cage0	Separate box is awkward

*Density restricts cabinet airflow

We can look qualitatively at the past packaging schemes. Figure 14 shows the various boxes (top view) as they fit within a cabinet profile. In some cases there is not a two level cabinet/box hierarchy as we have noted in the previous discussion on the packaging evolution because these structures have only been available at the cabinet level as we showed in Fig. 12. As one might guess from the table, the author's biasses run to packaging schemes that are not the highest density, that are fixed so that the conditions can be well-understood and that they may be cabled rigidly. It is interesting to note how the evolution for the larger computers is toward these fixed structures. In some real sense, packaging is quite a matter of designer preference because the only clear goal is manufacturing cost. Marketing considerations, especially for OEM use, drives toward getting the highest density (to minimize volume, floor space and rack mounting height). Although it can be shwon that poor airflow increases operating temperatures and therefore decreases component life, we designers are too loath to make all the necessary measurements and carry out the calculations. In this way we can usually show that any increase in MTBF has a corresponding cost savings.

In the following table, we give the metrics for the various packages in terms of their pay load--expressed in Printed Circuit Board area. Thus we get pay load ratios of board area per cu. ft. of box, per sq. ft. of floor.

Power Supplies

This section will give cost and performance characteristics of various DEC supplies as shown in Table x. It will list a set of supplies, their (relative) cost, MTBF, volume/year, power, technology, size, regulation, voltage, efficiency, and the ratios cost/watt, cost/cu. in., and what it's used on, the year introduced.

Modules

It isn't clear what should be said here. Phister has quite a bit. It will depend on what happens in the Modules chapter. We should clearly reference board area. We must bring in the backplane and get at the pay load of board area, square inches of panel area and cu. inches, then talk of efficiencies. The pin should also be a metric. Line width is the standard metric...but I'd just as soon not give it.

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AN OVERVIEW OF MANUFACTURING

The result of a design project is an entity which is manufactured. However, very little is written about manufacturing in computer engineering literature as we generally discuss algorithms, logic design, and circuit technology. And yet for a computer to be commercially successful, it must be manufacturable, economically operable and serviceable. Moreover, for most of the computer engineering discussed in this book, because the designs are intended for production, engineering costs are small (1-10%) compared with other product and lifecycle costs. The product cost is termined by the price of the components and the manufacturing process. The lifecycle cost includes the purchase price, the operational and service costs. For production, machines must be easy to assemble and test, repair must be rapid, engineering changes must be introduced smoothly, and the production line cannot be held up because of shortages of components -- all parts of traditional manufacturing understanding.

A detailed discussion of manufacturing is clearly beyond the scope of this text. For process engineering we suggest [Grant and Leavenworth, 19xx]. Information on test equipment is to be found mainly in manufacturers manuals, but a survey is given in [ ]. A reference on quality control is [Juran 1962] and a discussion of learning curves is in [ ].

he Life Cycle of a Product

Figure Lifecycle shows a simplistic process flow for the major phases and

milestones in the life of a product. In reality, planning and designs for many of the phases go on concurrently. The early research, advanced development and definitional phases are not shown. Often times, products may proceed from the idea to engineering breadboard and are terminated because they may not meet original goals or because better alternative ideas arise.

The engineering breadboard usually is built with wirewrapped boards rather than printed circuit boards in order to accommodate changes. At this stage schedules are made for manufacturing start up. Other organizations formulate and execute plans: systems' engineering - for product test/verification; software engineering - special software and verification; marketing - for promotion and product distribution; sales - for training; field service - training and parts logistics; and software support.

The engineering prototype proves the design using the printed circuit modules that will be used in the manufacturing. All peripherals in the planned systems configurations are tested on the prototype. Usually a number (10-100-depending on the complexity, cost and volume) of prototypes are constructed. The complete system must meet the product specification.

Limited release (LR) to manufacturing is a major milestone. The product is placed under formal engineering change control; specifications and documentation are available for the product and manufacturing process. For the integrated circuits, second sources of supply and testing procedures are in place. Process control tapes for the numerically controlled machine tools, e.g., component insertion, backplane wiring, and printed-circuit board drilling, are ready. Any special tooling for the mechanical

packaging has been obtained. Finally, the engineering change order (ECO) procedure for the hardware and microcode is set. Testing at all levels has been specified; test programs for computer-controlled testers have been written, special test equipment has been built, and diagnostic programs are ready. There must also exist a clear process by which engineering change orders (ECOs), including microprograms, can be made quickly in response to any as yet undetected design errors or changes that are necessitated by manufacturing process or parts availability.

Design maturity testing (DMT) with a number of engineering prototypes verifies the design and justifies the risk of a pilot run. Tests for reliability and functionality are conducted. Environmental testing (shock, temperature, humidity, static discharge, radiation, power interrupt, safety) is conducted at this stage.

The pilot run shakes down and verifies the actual manufacturing process by building a small number of units at the manufacturing plant using the product and process documentation.

Product announcement usually occurs during the DMT period but can be as early as limited release or as late as first customer shipment -- depending on the marketing strategy. This strategy is clearly a function of the volume, novelty, and competitive needs.

Process maturity testing (PMT) verifies that the product is being manufactured with the desired cost, quality, and product rate. The steady-state phase of manufacturing continues, with possible perturbations due to the introduction of product enhancements or process changes to lower product costs, until the product is phased out.

Manufacturing Process Flows

An overview of a manufacturing process is given in Figure Manufover which shows how a product moves through the various factories. There are different DEC and independent manufacturer plants for boards, peripherals, memories, and central processors that form the box-level and independent hardware (e.g., memory modules) components. Integration from the other stages and stack storage occurs at the stage called final assembly and test (FA&T). Here, the software system operations manuals and other documentation that is to be run is also integrated and tested.

In Figure process60 we give the complete flow for a typical volume manufacturing line -- the 11/60 central processor facility in Aguadilla, Puerto Rico. Integrated circuits occur outside this factory and are sent to be inserted, soldered in, and tested. The photographs in Figures x through y show several test points in the process.

Integrated circuit failure rate versus time follows a bathtub-shaped curve, high at either end of the life cycle, as shown in Figure Bath. The manufacturing process includes extensive thermal cycling to ensure that the "infant mortality" cases are discovered early during manufacturing, because it is more expensive to find defective components at the larger, more integrated systems level. The temperature/humidity environmental chambers which house n CPU's each are shown in Fig. TChamber. Figures 2224 and lvstation show small heated enclosures used to induce failure during the test and repair of modules.

Since testing occurs at each stage in the manufacturing process, dedicated logic must be added to the design, to provide physical access "probes" for

the test equipment. To test a particular function, it must be: specifiable, invokable, and observable. For example, the function of an adder can be clearly specified but it cannot be easily invoked or observed if its inputs and outputs are etch runs on a printed circuit board. Several testing strategies are used: add signal lines from the adder to the backplane where there are adequate probe access points; probe directly onto the module etch or IC pins; and subsume the adder in a function whose inputs and outputs can be more easily controlled and observed. The general problem can be modelled by the simple circuits shown in Fig. obs. Each gate could be part of a computer on a chip where there is no possibility for repair. The problems of observation and control exist at all levels of integration. Examples of observation points at each level are given in Table Obslevels for the 11/60 computer.

In Fig. QVstation, the function being tested is a complete CPU which is packaged on several printed circuit modules. Behavior is being induced by PDP-11 programs and observed by inspecting of the results in memory using a diagnostics program or manually. However, a lower level of behavior can be observed (on the special display panel at the right) and controlled (by varying the clock rate of the CPU). The lights on the display panel are driven from backplane signals and show the contents of certain registers, e.g., micro-instruction register, program status register, and the ALU output register.

Table: Obslevels

vel in computer hierarchy	Observation point	Stage in manufacture of computer	Example

electrical circuit	transistor contacts on metallization layer	semiconductor fabrication	wafer test with micro-probe
switching circuit	leads on ~~i.c.~~ IC package	incoming inspection of ICs	
register transfer	etch run	module	probe on PC board (module-specific test) GR
register transfer	backplane	module	2224 memory exerciser for cache
PMS (Pc)	Unibus	CPU	
PMS (Pc)	contents of memory	CPU	diagnostic programs at subsystem level, e.g., memory-management unit, or processor instruction set tests
PMS (C)	contents of memory	System integration	peripheral diagnostic programs
PMS (C)	Unibus	System integration	DECX-11 bus exerciser

Figure APT shows the final acceptance of a unit (CPU, memory, power supply, and console) prior to final assembly and test of the system using a system called Automatic P? Testor. In both Figs. OVstation and APT, the entire instruction set is tested; a central computer system loads the diagnostic programs and monitors their execution. Several hundred lines emanate from this system to all of the computers under test throughout the production line. The Unibus of the processor under test serves as the umbilical cord [Chapter 00, p. 00] to accept the diagnostic programs and to be monitored by making memory observations.

Modules are tested using several methods. One method (see step j of Fig. Process60), uses the GR tester. Here, every signal input and test point on the module is probed using a fixed "bed of nails" test probe. The testor then selects the desired input and test point. In another method, (see step k, Fig. Process60) the module under test is placed in a processor in which all of the other modules are known to be good to be verified. This later test is necessary because the first test usually doesn't run at the operational speed of the computer, nor is such a test guaranteed to cover 100% of the logic.

Following the inter-plant transfer, systems integration begins. Figure FA&T shows the process flow for the 11/60 at the Westminster Plant. For some computer systems, FA&T is carried out by having an individual technician follow a system through each of the three phases: incoming test the CPU cabinet assembly, integration of peripherals, and final acceptance. Thus one or more have individual responsibility for fabricating a single system in what is a traditional, hand-crafted,

job-shop fashion.

Alternatively, FA&T is carried out in what is fundamentally a continuous, production line environment called the Common Systems Integration (CSI) line. Here, workstations exist at each stage of the production line, and are interconnected by conveyors.

The floor plan of the Westminster Common Systems Integration (CSI) area is shown in Fig. CSI. Figure spurs shows four of the workstations in the integration phase. A turntable in the center of the spurs routes the systems to the workstations.

"Statistical Quality Control", Grant & Leavenworth, 4th Edition, McGraw-Hill, 19XX

"Quality Control Handbook", Juran, J. M. McGraw-Hill 1951; Second Edition, 1962.

An Overview of Manufacturing

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