

SUBJ: MINUTES

DATE:

FROM:

PAGE 1
02-05-75
GORDON BELL

1093

* * * * *
PLEASESEND TO: FILE
* * * * *

SUBJ: OOD STAFF MEETING MINUTES--January 30, 1975

To: OOD

1. Plowman, Van Roekens, Tays and Saviers can have the capability to move their own personnel files to do salary planning, planning programs to do salary planning.
2. We are supposed to inform OC of 1 for 1 people replacements.
3. Arnie described the technical edit program in sales. Platz is doing a more detailed version, based on EPLAS for Westminster. Arnie asked OOD to support the questionnaires.
4. We discussed the ROI/PLC parameters for the VT50.
5. We voted for an overrun for Stockebrand for 1 month in order to hold group together.
6. Henry Lemaire proposes to obtain some MOSTEK facilities. We recommend that the proposal be part of manufacturing budget.
7. The word "fraud" should not be used on people who are terminated. Mismanagement is a less libelous word.

GB:mjk

SUBJ: CLASSIC 11

DATE:
FROM:PAGE 1
02-07-75
GORDON BELL

* * * * *
 PLEASESEND TO: FILE
 * * * * *

To: Distribution

The attached project prospectus (copies only to Teicher and Spector) from Ken Bowles at UC/SD is something that I want to get involved with. He came to me because we have been unresponsive through his sales/marketing group.

How is it?

I believe this is the follow-on CLASSIC,..or intelligent terminal of the type we would all like to have. His demands and goals are totally reasonable (I seriously doubt whether he can get that much out of the CAI software with this small of a system right now, however, there are still lots of things he can do that are reasonable that do fit the system. I'm also intrigued about some of the other goals which we might otherwise say are unreasonable that can be done (e.g. emulation of other machines).

Here's what I want:

1. Steve should use this as his benchmark low end complete system.
2. Steve, Stocky, and Len Hallio should get together to work the display issue and how Len and Stocky's plans mesh with the perceived need/use/solution of Bowles.
3. We should get Bowles to come here for a general discussion about the UC/SD direction together with anything that has not been written down. Obviously we can't say anything about our own direction, but we can show a willingness, and try to sell him on the 11. If they go this way, the big bucks and real problem that we win with is the software. That is the major undertaking and a really hard part (assuming we get on the stick and get him a terminal fit for human consumption, and the right system price.

SUBJ: CLASSIC 11

DATE:
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GORDON BELL

4. Let's get a fix on his language concerns. He thinks PASCAL is "the right" language for programming. I'd like Al to put this in perspective. BASIC isn't, and I hate the thought of a PL/1 investment.
5. Let's get a clear line of who is involved from a sales/marketing viewpoint-- which market group? sales?--so that those interfaces are being handled smoothly. If we get more involved, it can be direct.
6. Let's get a way for us to work with him (at arms' length) such that we understand and complement one another. I believe this is a desirable sale because he is just idealistic and unreasonable enough to provide a goal for a product. I even want to find the way to get the business.

GB:mjk

Distribution-----
Steve Teicher (For his low end study group)
Charlie SpectorCC: Al Brown
Peter Christy
Dick Clayton
Len Halio
Andy Knowles
Ed Kramer
Larry Portner
Tom Stockebrand

COMPUTER SPECIAL SYSTEMS

LABOR RATES

	Hourly	Daily	Weekly (40 hrs)	Monthly (160 hrs)
System Engineer - A (5-10 yrs experience)	\$50.00	\$400.00	\$2,000	\$8,000
System Engineer - B (3-6 yrs experience)	\$43.00	\$344.00	\$1,720	\$6,880
System Engineer - C (1-4 yrs experience)	\$36.00	\$288.00	\$1,440	\$5,760
System Technician - A	\$30.00	\$240.00	\$1,200	\$4,800
System Technician - B	\$23.50	\$188.00	\$ 940	\$3,760
System Technician - C	\$22.00	\$176.00	\$ 880	\$3,500
Wireman - A	\$18.00	\$144.00	\$ 720	\$2,880
Wireman - B	\$15.00	\$120.00	\$ 600	\$2,400
System Programmer - A (5-10 yrs experience)	\$50.00	\$400.00	\$2,000	\$8,000
System Programmer - B (3-6 yrs experience)	\$42.00	\$336.00	\$1,680	\$6,720
System Programmer - C (1-4 yrs experience)	\$36.00	\$288.00	\$1,440	\$5,760
Engineering Writer - A	\$39.00	\$312.00	\$1,560	\$6,240
Engineering Writer - B	\$31.00	\$248.00	\$1,240	\$4,960
Technical Illustrator	\$27.00	\$216.00	\$1,080	\$4,320
Technical Typist	\$19.00	\$152.00	\$ 760	\$3,040

The above rates apply to all custom hardware/software products. Each rate includes labor associated with design, assembly, testing, documentation, and acceptance of custom products.

8/74

CSS-466-A-4

COMPUTER SPECIAL SYSTEMS LABOR RATES

	Hourly	Daily	Weekly (40 hrs)	Monthly (160 hrs)
✓ Senior Program Manager/ Consultant	\$75.00	\$600.00	\$3,000.00	\$12,000
✓ System Engineer - A (5-10 yrs experience)	\$58.00	\$464.00	\$2,320.00	\$ 9,280
System Engineer - B (3-6 yrs experience)	\$50.00	\$400.00	\$2,000.00	\$ 8,000
System Engineer - C (1-4 yrs experience)	\$42.00	\$336.00	\$1,680.00	\$ 6,720
System Technician - A	\$35.00	\$280.00	\$1,400.00	\$ 5,600
System Technician - B	\$27.00	\$216.00	\$1,080.00	\$ 4,320
System Technician - C	\$26.00	\$208.00	\$1,040.00	\$ 4,160
Wireman - A	\$21.00	\$168.00	\$ 840.00	\$ 3,360
Wireman - B	\$17.00	\$136.00	\$ 680.00	\$ 2,720
System Programmer - A (5-10 yrs experience)	\$58.00	\$464.00	\$2,320.00	\$ 9,280
System Programmer - B (3-6 yrs experience)	\$49.00	\$392.00	\$1,960.00	\$ 7,840
System Programmer - C (1-4 yrs experience)	\$42.00	\$336.00	\$1,680.00	\$ 6,720
Engineering Writer - A	\$45.00	\$360.00	\$1,800.00	\$ 7,200
Engineering Writer - B	\$36.00	\$288.00	\$1,440.00	\$ 5,760
Draftsman	\$31.00	\$248.00	\$1,240.00	\$ 4,960
Technical Typist	\$22.00	\$176.00	\$ 880.00	\$ 3,520

The above rates apply to all custom hardware/software products. Each rate includes labor associated with design, assembly, testing, documentation, and acceptance of custom products.

1124

NOTE: Numbers in parenthesis refer to instructions on reverse. (1)

NAME OF OFFEROR Digital Equipment Corporation		ITEM OF SUPPLIES AND/OR SERVICES TO BE FURNISHED (2) System Engineer A	
HOME OFFICE ADDRESS (Include ZIP Code) 146 Main Street, Maynard, Mass. 01754		QUANTITY	TOTAL AMOUNT PROPOSED FOR ITEM (3)
DIVISION(S) AND LOCATION(S) WHERE WORK IS TO BE PERFORMED Maynard, Marlboro (Mass.)		GOVERNMENT SOLICITATION NO.	

By submission of this form the offeror claims exemption as checked below from requirements for submitting cost or pricing data on the basis that the price offered is, or is based on, an established catalog or market price of an item sold in substantial quantities to the general public or is a price set by law or controlled by regulation (see ASPR 3-807). Check I, II, or III below and provide applicable information. (3)

I. CATALOG PRICE: (4)
 Catalog identification CSS-466-A-4 Date 8/74
 Period Covered (5) From 8/74 to next revision

SALES CATEGORIES:

A. U. S. Government sales (6)	<u>10% - 15% (est'd)</u>	* Units
B. Sales at Catalog Price to the General Public (7)	<u>85% - 90% (est'd)</u>	* Units
C. Sales to the General Public at other than Catalog Price (8)	<u>0</u>	* Units

(* If the offeror's accounting system does not provide precise information, the offeror should insert his best estimate and explain in an attachment the basis for his estimate.)

LIST THREE SALES OF THE ITEM OFFERED. (9)

CATEGORY:		DATE	NO. OF UNITS SOLD	PRICE/UNIT	
B	C				
1.	<input checked="" type="checkbox"/> <input type="checkbox"/>	<u>10/73</u>	<u>16 (hrs.)</u>	<u>\$50/hour</u>	Based on catalog CSS-466-A-3 dated 2/73 covering period 2/73-7/74
2.	<input checked="" type="checkbox"/> <input type="checkbox"/>	<u>3/74</u>	<u>40 (hrs.)</u>	<u>\$50/hour</u>	
3.	<input checked="" type="checkbox"/> <input type="checkbox"/>	<u>11/73</u>	<u>144 (hrs.)</u>	<u>\$50/hour</u>	

II. MARKET PRICE: Set forth the source and date or period of the market quotation or other base for market price, the base amount and applicable discounts. (10)

III. LAW OR REGULATION Identification: (11)

The offeror represents that all statements made above and on attachments submitted are accurate and are submitted for the purpose of claiming exemption from requirements for cost or pricing data. The offeror also represents that, except as stated in an attachment, a like claim for exemption involving the same or a substantially similar item has not been denied by a Government contracting officer within the last two years. Pending consideration of the proposal supported in whole or in part by this submission and, if this proposal or a modification thereof is accepted by the Government, thereafter until the expiration of three years from the date of final payment under a contract resulting from this proposal, the contracting officer or any other authorized employee of the United States Government is granted access to books, records, documents and other supporting data which will permit verification of the claim.

TYPED NAME AND TITLE Robert E. Walsh, Contracts Dept. Manager	SIGNATURE <i>RE Walsh</i>
NAME OF FIRM Digital Equipment Corporation	DATE OF SUBMISSION 1/20/75

1125

NOTE: Numbers in parenthesis refer to instructions on reverse. (1)

NAME OF OFFEROR Digital Equipment Corporation		ITEM OF SUPPLIES AND/OR SERVICES TO BE FURNISHED (2) System Engineer B	
HOME OFFICE ADDRESS (Include ZIP Code) 146 Main Street, Maynard, Mass. 01754		QUANTITY	TOTAL AMOUNT PROPOSED FOR ITEM (\$) _____
DIVISION(S) AND LOCATION(S) WHERE WORK IS TO BE PERFORMED Maynard, Marlboro (Mass.)		GOVERNMENT SOLICITATION NO. _____	

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I. CATALOG PRICE: (4)
 Catalog identification CSS-466-A-4 Date 8/74

Period Covered (5) From 8/74 to next revision

SALES CATEGORIES:

A. U. S. Government sales (6)	<u>10% - 15% (est'd)</u>	* Units
B. Sales at Catalog Price to the General Public (7)	<u>85% - 90% (est'd)</u>	* Units
C. Sales to the General Public at other than Catalog Price (8)	<u>0</u>	* Units

(* If the offeror's accounting system does not provide precise information, the offeror should insert his best estimate and explain in an attachment the basis for his estimate.)

LIST THREE SALES OF THE ITEM OFFERED. (9)

CATEGORY:		DATE	NO. OF UNITS SOLD	PRICE/UNIT	
B	C				
1. <input checked="" type="checkbox"/>	<input type="checkbox"/>	<u>4/74</u>	<u>24 (hrs.)</u>	<u>\$43/hour</u>	Based on catalog CSS-466-A-3 dated 2/73 covering period 2/73-7/74
2. <input checked="" type="checkbox"/>	<input type="checkbox"/>	<u>3/74</u>	<u>56 (hrs.)</u>	<u>\$43/hour</u>	
3. <input checked="" type="checkbox"/>	<input type="checkbox"/>	<u>3/74</u>	<u>240 (hrs.)</u>	<u>\$43/hour</u>	

II. MARKET PRICE: Set forth the source and date or period of the market quotation or other base for market price, the base amount and applicable discounts. (10)

III. LAW OR REGULATION Identification: (11)

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TYPED NAME AND TITLE Robert E. Walsh, Contracts Dept. Manager	SIGNATURE <i>RE Walsh</i>
NAME OF FIRM Digital Equipment Corporation	DATE OF SUBMISSION 1/20/75

DEPARTMENT OF DEFENSE
CLAIM FOR EXEMPTION FROM SUBMISSION OF CERTIFIED COST OR PRICING DATA

FORM APPROVED
OMB No. 22-R0294

1126

NOTE: Numbers in parenthesis refer to instructions on reverse. (1)

NAME OF OFFEROR Digital Equipment Corporation		ITEM OF SUPPLIES AND/OR SERVICES TO BE FURNISHED (2) System Engineer C	
HOME OFFICE ADDRESS (Include ZIP Code) 146 Main Street Maynard, Mass. 01754		QUANTITY	TOTAL AMOUNT PROPOSED FOR ITEM(S)
DIVISION(S) AND LOCATION(S) WHERE WORK IS TO BE PERFORMED Maynard, Marlboro (Mass.)		GOVERNMENT SOLICITATION NO.	

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I. CATALOG PRICE: (4)
Catalog identification CSS-466-A-4 Date 8/74

Period Covered (5) From 8/74 to next revision

SALES CATEGORIES:

- | | | |
|--|--------------------------|---------|
| A. U. S. Government sales (6) | <u>10% - 15% (est'd)</u> | * Units |
| B. Sales at Catalog Price to the General Public (7) | <u>85% - 90% (est'd)</u> | * Units |
| C. Sales to the General Public at other than Catalog Price (8) | <u>0</u> | * Units |

(* If the offeror's accounting system does not provide precise information, the offeror should insert his best estimate and explain in an attachment the basis for his estimate.)

LIST THREE SALES OF THE ITEM OFFERED. (9)

CATEGORY:		DATE	NO. OF UNITS SOLD	PRICE/UNIT
B	C			
1. <input checked="" type="checkbox"/>	<input type="checkbox"/>	<u>12/73</u>	<u>24 (hrs.)</u>	<u>\$36/hour</u>
2. <input type="checkbox"/>	<input type="checkbox"/>	_____	_____	_____
3. <input type="checkbox"/>	<input type="checkbox"/>	_____	_____	_____

Based on catalog
CSS-466-A-3 dated
2/73 covering period
2/73-7/74

II. MARKET PRICE: Set forth the source and date or period of the market quotation or other base for market price, the base amount and applicable discounts. (10)

III. LAW OR REGULATION Identification: (11)

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TYPED NAME AND TITLE Robert E. Walsh, Contracts Dept. Manager	SIGNATURE <i>RE Walsh</i>
NAME OF FIRM Digital Equipment Corporation	DATE OF SUBMISSION 1/20/75

CLAIM FOR EXEMPTION FROM SUBMISSION OF CERTIFIED COST OR PRICING DATA

1127

NOTE: Numbers in parenthesis refer to instructions on reverse. (1)

NAME OF OFFEROR Digital Equipment Corporation		ITEM OF SUPPLIES AND/OR SERVICES TO BE FURNISHED (2) System Technician A	
HOME OFFICE ADDRESS (Include ZIP Code) 146 Main Street, Maynard, Mass. 01754		QUANTITY	TOTAL AMOUNT PROPOSED FOR ITEM (\$)
DIVISION(S) AND LOCATION(S) WHERE WORK IS TO BE PERFORMED Maynard, Marlboro (Mass.)			GOVERNMENT SOLICITATION NO.

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I. **CATALOG PRICE:** (4)
Catalog identification CSS-466-A-4 Date 8/74

Period Covered (5) From 8/74 to next revision

SALES CATEGORIES:

- A. U. S. Government sales (6) 10% - 15% (est'd) * Units
- B. Sales at Catalog Price to the General Public (7) 85% - 90% (est'd) * Units
- C. Sales to the General Public at other than Catalog Price (8) 0 * Units

(* If the offeror's accounting system does not provide precise information, the offeror should insert his best estimate and explain in an attachment the basis for his estimate.)

LIST THREE SALES OF THE ITEM OFFERED. (9)

CATEGORY:		DATE	NO. OF UNITS SOLD	PRICE/UNIT	
B	C				
1.	<input checked="" type="checkbox"/> <input type="checkbox"/>	<u>11/73</u>	<u>256 (hrs.)</u>	<u>\$30/hour</u>	Based on catalog CSS-466-A-3 dated 2/73 covering period 2/73 - 7/74
2.	<input checked="" type="checkbox"/> <input type="checkbox"/>	<u>12/73</u>	<u>56 (hrs.)</u>	<u>\$30/hour</u>	
3.	<input checked="" type="checkbox"/> <input type="checkbox"/>	<u>3/74</u>	<u>160 (hrs.)</u>	<u>\$30/hour</u>	

II. **MARKET PRICE:** Set forth the source and date or period of the market quotation or other base for market price, the base amount and applicable discounts. (10)

III. **LAW OR REGULATION** Identification: (11)

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TYPED NAME AND TITLE Robert E. Walsh, Contracts Dept. Manager	SIGNATURE <i>RE Walsh</i>
NAME OF FIRM Digital Equipment Corporation	DATE OF SUBMISSION 1/20/75

CLAIM FOR EXEMPTION FROM SUBMISSION OF CERTIFIED COST OR PRICING DATA

1128

NOTE: Numbers in parenthesis refer to instructions on reverse. (1)

NAME OF OFFEROR Digital Equipment Corporation		ITEM OF SUPPLIES AND/OR SERVICES TO BE FURNISHED (2) Programmer C	
HOME OFFICE ADDRESS (Include ZIP Code) 146 Main Street, Maynard, Mass. 01754		QUANTITY	TOTAL AMOUNT PROPOSED FOR ITEM(S)
DIVISION(S) AND LOCATION(S) WHERE WORK IS TO BE PERFORMED Maynard, Marlboro (Mass.)			GOVERNMENT SOLICITATION NO.

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I. **CATALOG PRICE:** (4)
Catalog identification CSS-466-A-4 Date 8/74

Period Covered (5) From 8/74 to next revision

SALES CATEGORIES:

- A. U. S. Government sales (6) 10% - 15% (est'd) • Units
- B. Sales at Catalog Price to the General Public (7) 85% - 90% (est'd) • Units
- C. Sales to the General Public at other than Catalog Price (8) 0 • Units

(* If the offeror's accounting system does not provide precise information, the offeror should insert his best estimate and explain in an attachment the basis for his estimate.)

LIST THREE SALES OF THE ITEM OFFERED. (9)

CATEGORY:		DATE	NO. OF UNITS SOLD	PRICE/UNIT	
B	C				
1. <input checked="" type="checkbox"/>	<input type="checkbox"/>	<u>12/73</u>	<u>24 (hrs.)</u>	<u>\$36/hour</u>	Based on catalog CSS-466-A-3 dated 2/73 covering period 2/73 - 7/74
2. <input checked="" type="checkbox"/>	<input type="checkbox"/>	<u>2/74</u>	<u>520 (hrs.)</u>	<u>\$36/hour</u>	
3. <input checked="" type="checkbox"/>	<input type="checkbox"/>	<u>11/73</u>	<u>240 (hrs.)</u>	<u>\$36/hour</u>	

II. **MARKET PRICE:** Set forth the source and date or period of the market quotation or other base for market price, the base amount and applicable discounts. (10)

III. **LAW OR REGULATION** Identification: (11)

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TYPED NAME AND TITLE Robert E. Walsh, Contracts Dept. Manager	SIGNATURE <i>RE Walsh</i>
NAME OF FIRM Digital Equipment Corporation.	DATE OF SUBMISSION 1/20/75

1129

NOTE: Numbers in parenthesis refer to instructions on reverse. (1)

NAME OF OFFEROR Digital Equipment Corporation		ITEM OF SUPPLIES AND/OR SERVICES TO BE FURNISHED (2) Wireman A	
HOME OFFICE ADDRESS (Include ZIP Code) 146 Main Street, Maynard, Mass. 01754		QUANTITY	TOTAL AMOUNT PROPOSED FOR ITEM (\$)
DIVISION(S) AND LOCATION(S) WHERE WORK IS TO BE PERFORMED Maynard, Marlboro (Mass.)			GOVERNMENT SOLICITATION NO.

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I. CATALOG PRICE: (4)
Catalog identification CSS-466-A-4 Date 8/74

Period Covered (5) From 8/74 to next revision

SALES CATEGORIES:

A. U. S. Government sales (6)	<u>10% - 15% (est'd)</u>	* Units
B. Sales at Catalog Price to the General Public (7)	<u>85% - 90% (est'd)</u>	* Units
C. Sales to the General Public at other than Catalog Price (8)	<u>0</u>	* Units

(* If the offeror's accounting system does not provide precise information, the offeror should insert his best estimate and explain in an attachment the basis for his estimate.)

LIST THREE SALES OF THE ITEM OFFERED. (9)

CATEGORY:		DATE	NO. OF UNITS SOLD	PRICE/UNIT	
B	C				
1. <input checked="" type="checkbox"/>	<input type="checkbox"/>	<u>2/74</u>	<u>64 (hrs.)</u>	<u>\$18/hour</u>	Based on catalog CSS-466-A-3 dated 2/73 covering period 2/73 - 7/74
2. <input checked="" type="checkbox"/>	<input type="checkbox"/>	<u>12/73</u>	<u>8 (hrs.)</u>	<u>\$18/hour</u>	
3. <input type="checkbox"/>	<input type="checkbox"/>				

II. MARKET PRICE: Set forth the source and date or period of the market quotation or other base for market price, the base amount and applicable discounts. (10)

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TYPED NAME AND TITLE Robert E. Walsh, Contracts Dept. Manager	SIGNATURE <i>RC Walsh</i>
NAME OF FIRM Digital Equipment Corporation	DATE OF SUBMISSION 1/20/75

DIGITAL EQUIPMENT CORPORATION

1130

February 3, 1975

Jane M. Pugh
Assistant Keeper
Science Museum
South Kensington
London SW7 2DD
England

Dear Miss Pugh:

Ken Olsen just handed me your letter of January 8, regarding MIT's Whirlwind. We have it in storage now, and Ken is keeping it for the Smithsonian. The MITRE Corporation is also trying to get it back. Hence, it is somewhat in limbo. We cannot promise a core memory or core memory plane to you just now, but we could make some other parts available--such as a switch register or a flip-flop from its accumulator. Ken would like to keep one of the cores systems in tact, and give it to the Smithsonian, and dismantle the other stack so that planes could be made available to various museums. But until this matter is cleared up with MITRE and the Smithsonian, we can't really move. Therefore, we will try to get a loan of a part of the the memory core system, but we could get you other parts and photographs if you are interested.

As for your letter of 24 July to me, I have certainly been late in responding. We have been in the mode of cutting back our museum program, because we have increased pressure for capital and people in the current unsettled economic climate. Nevertheless, we are still proceeding, and in fact, since our museum group really had little noticeable output for their expenditure of time, capital, etc., it is just as well that we are doing little. It has been really difficult to get the museum going.

I had asked Roy Gould to prepare a kit of parts that had to do with the minicomputer part of technology for you and others, but he has not made progress along these lines. I hope he will take this opportunity to assemble some materials and forward them if you're interested. I am starting to get some material from other places (e.g. the University of Illinois, Manchester,) and would like to get these parts put into perspective and will get them into displays around our facilities to build up interest in the historical section. Our museum will consist of 2 parts: the collection of old parts, and the working part that explains machines with demonstrations. As a Corporate Office, I'm pushing for the later, because of the general need, but I'm personally interested in the archival section (which will be small).

I would like you to give me an idea of some of the machine parts that you could obtain. I will buy these most likely for my personal collection, which I will loan to our museum; DEC and/or Ken Olsen may also buy some of the parts.

I am interested in all types of historical parts: mechanical

calculators, early data processing and storage equipment and conventional 1st and 2nd generation computers.

I think it is important to get some functional mechanical equipment, and I personally want a Thomas Arithometer.

I would hope that some parts of early English machines are still around in various junk stores (e.g. STC, ICT, Ferranti). In this regard, I have some pieces of the DEUCE, but would like to get some of ACE, and PEGASUS, together with other machines that were commercial versions of the Manchester machines. STC made a copy of our PDP-1, and I would like part of it, but we probably should go after it through ITT. In fact, if you have names of people within the UK computer industry, I would correspond directly.

As for the mechanics of purchasing, please let me have an idea of the parts and the money involved, and I'll send a check for the account. We should try a few purchases, and see if it is all right with both you and I. I'm sure we can get lawyers (solicitors) involved, but if we keep it simple, that pain can be avoided. Your commission should be whatever you think is fair--I have no knowledge of these matters. The equipment can be delivered to our DEC office in London (and to Reading) for transshipment. It might be useful to talk with our manager, Mr. Geoff Shingles of the U.K. office, because I've talked with him about this from time to time--hopefully he'll call you first at 01,589,6371, but the UK office number that he's at is: 58 35 55.

I hope we can get started with the collection.

Sincerely,

Gordon Bell
Vice President, Office of Development

cc: Geoff Shingles, U.K. Office
Roy Gould
Ken Olsen
Mimi Cummings

DIGITAL EQUIPMENT CORPORATION
146 Main Street
Maynard, Massachusetts 01754



SCIENCE MUSEUM

South Kensington London SW7 2DD

Telephone 01-589 6371 ext

JAN 13 1974

Mr Kenneth Olsen
 President
 Digital Equipment Corporation
 MAYNARD
 Massachusetts
 U.S.A.

Your reference

Our reference

Date 8 January 1975

Dear Sir

A large new display on the history, operation and applications of computers is in preparation at this Museum. Through Professor Arthur Porter, and Professor Jay Forrester, I have heard that the old Whirlwind computer may be in your custody. If this is indeed the case, I wonder if there is a possibility of a loan of a small piece of the core store. We have a good collection of early storage methods - delay lines, Williams tubes and early drums, but have no example of the early core stores. As the Whirlwind is credited as being the first machine to use core storage, it would obviously greatly enhance our display to be able to show a sample of its core.

I look forward to hearing from you,

Yours sincerely

Jane Pugh

Jane M. Pugh
 Assistant Keeper

Baby In Smithsonian

Panel available

try to find it - many - but have permission now!

MITRE

[Signature]

To: ^{TKO} Roy Gould + Sally + Hold.



SCIENCE MUSEUM

South Kensington London SW7 2DD

Telephone 01-589 6371 ext

1133

JUL 30 1974
2-32

eg old stuff
Ace

Professor Gordon Bell
Vice-President, Engineering
Digital Equipment Corporation
146 Main Street
MASSACHUSETTS 01754
U S A

Your reference GB:mjk

Our reference 100/123/13

Date 24 July 1974

Dear Professor Bell

First of all please let me apologise for the delay in replying to your letter of June 11th. This has been due to circumstances quite beyond my control, and I assure you it does not at all reflect a lack of interest on my part to the content of your letter.

I will answer the points raised in the same order. Concerning exchanges of objects, this can be a possibility, depending on the items involved. If you could give me a better idea of exactly what sort of artifacts you are looking for, I hope we will be able to come to a mutually satisfactory agreement. I am certainly very keen to have some parts of a Whirlwind, for instance.

I have been advised that I may be able to act as a purchasing agent for you, provided that this did not conflict with my Museum work and interests. It is not clear whether you are interested in just computers or also early calculating machines and mathematical instruments. Again I would be grateful for details of what you think this would involve, as it will have to be considered by senior officers here.

As to the other points, I shall be most pleased to give you any help and advice that I can for your new Museum etc. I was delighted to receive your book, thank you very much indeed. We had not seen a copy before, and it has already proved most helpful in the preparation of one part of our forthcoming exhibition.

I look forward to hearing from you.

Yours sincerely

E Bechlake

pp Jane Pugh
Assistant Keeper
Department of Astronomy
Mathematics & Earth Sciences

what
can
we
do
here?

also a kit of
DEC stuff
let's start by an offer

1107
1134

digital

June 11, 1974

Miss Jane Pughe
Asst. Keeper, Computing Section
Science Museum
Exhibition Road
London, SW7, England

Dear Miss Pughe:

It was a pleasure talking with you on Friday, June 7, regarding possible interaction with you and the Science Museum. Professors Wilkes and Randall have spoken enthusiastically of your efforts and exhibits at the Museum.

I'm interested in some means of cooperating with you in the establishment of our own DEC museum in Massachusetts. DEC is a manufacturer of mini (and larger) computers with sales of about \$400M (about 1/3 of which is in Europe). It was founded in 1957, and its antecedent machines include MIT's Whirlwind and the Lincoln Laboratories TX-0 and TX-2. A booklet of DEC is attached. Our own museum will include parts of Whirlwind, the TX-0 (operational), other machines (operational) and various technological parts.

The cooperation we might explore:

1. Exchange of computers or computer parts with the Science Museum. We have nearly all of Whirlwind. Also, we have parts or complete machines of our early DEC machines. I (and Prof. Wilkes) feel that Whirlwind should be represented in your museum. Similarly, I believe it might be interesting to have a working U.S. machine (minicomputer) exhibit, too.
2. Your acting as a purchasing agent for early British and European, computing instruments for me. Here, I would like to personally buy machine parts which could be loaned to our museum; I have no intention of having our corporation buy parts which would not have wide appeal to the general American public. Since you have knowledge of this field, I would like to prevail upon you to consider such an arrangement. (I will wait until I hear from you before I contact Sotheby's 1 Bond St. W1). This arrangement would have to be cleared through the Science Museum.
3. Since we (I and others directly involved in our own museum) are considering a museum, we would like to have benefit of your counsel from time to time.
4. As a student of computing machinery, I would like to establish contact, because I may write other books about computing. Enclosed is a book

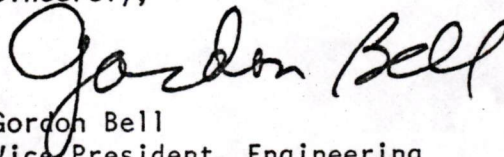
To: Miss Pughe
June 11, 1974

From: Gordon Bell
-2-

written by myself and Allen Newell of post Von Neuman computing;
and this may eventually go into another edition.

Please consider the above possibilities, and I look forward to hearing
from you, and eventually visiting with you.

Sincerely,



Gordon Bell
Vice President, Engineering
Professor, Computer Science
Carnegie-Mellon University (on leave)

GB:mjk

cc: Ken Olsen
Geoff Shingles
Roy Gould
Sally Lymberg

SUBJ: OOD STAFF MINUTES

DATE: PAGE 1
FROM: 01-24-75
GORDON BELL

* * * * *
PLEASESEND TO: FILE
* * * * *

SUBJ: OOD STAFF MEETING MINUTES--1/23/75

To: OOD
CC: Mark Abbett, Ed Corell, Tom Stockebrand

- 1. A. Ed Corell and Tom Stockebrand will get together to work on the terminal plan.
- B. We will get Tom a decision on his request for budget over-run to maintain the group by February 1.
- 2. Becky Hawes introduced us to the Corporate Salary Planning process for 1975,
- 3. Mark will get back with expense visibility on the recruiting mechanism. The cost center pays for recruiting.
- 4. A. We will go to OC to ask for a policy to add people to spend according to budget.
- (B. Larry asked for 5 hires; 3 are approved as a replacement. We recommend the other 2 to OC--Larry is under budget.)
- 5. Gordon will get George Plowman to take over the Engineering Committee. (Notes on Eng. Co. Charter attached.)
- 6. We currently believe we aren't effectively communicating with Field Service and Production. We will talk with them once/quarter (Shields/Cudmore--St. Amour).
- 7. Core and MOS now meet the budget. Components is paying for core on 11/WD!
 - A. 32K--progress in understanding ringing, better operating point, redressed lines, Two systems running at margin and room temperature. Report at schedule review on Wednesday, Feb, 15, looks good,
 - B. MOSTEK--failure rates up on early devices at 70deg. C.

GB:mjk

TO: Gordon Bell

DATE: January 22, 1975

To: O2D, Eng. Committee,

FROM: Rony Elia-Shaoul

~~1140~~

George Plowman

DEPT: Micro Products

EXT: 2102 LOC: 11-2 (ML11/E61)

SUBJ: ENGINEERING COMMITTEE CHARTER

In chatting with Lorrin today about the Engineering Committee Charter, he made the following suggestions with which I concur:

- 1) The Engineering Committee should be a compromise of engineers, managers, and supervisors, who have been at D.E.C. for 5 or more years, and have done a number of significant projects.
- 2) They should be an advisory board to management (OOD), and to project engineers (workers).
- 3) They should offer opinions on key policies, products, projects, business, manufacturing, or any other issues requested of them.
- 4) They should not be responsible for creating or enforcing policies.
- 5) They should have a direct pipeline to you, Ken, and Pete so that when their opinions arrive, they do so unadulterated!
- 6) Areas of review could include:
 - a) Project plans - how something is accomplished, budgets, and manpower.
 - b) Products - will it work? State of the art, reliability, technology, and manufacturing issues.
 - c) Engineering design procedures.
 - d) Manufacturing problems, testing, etc.
- 7) As far as standards, procedures, and ECO activities, these should be handled by the responsible people in the designated areas. The Engineering Committee can ask, however, to review some procedures should it become necessary.

The following is a suggested list of people we suggest could be members of this committee:

Group A. Practicing Engineer - 5

Ralph Dieter
Al Kent
Alan Kotok
Jesse LipconJim O'Loughlin
Pat Sullivan
Don Vonada
Don White

Group B. Supervisors and Managers who were originally engineers (5-6)

Vince Bastiani	Steve Rothman
Bruce Delagi	Grant Saviers
Russ Doane	Tom Stockebrand
Len Hughes	Steve Teicher
Lou Klotz	Mike Titlebaum
Walter Manter	Allan Wallack
Dennis O'Connor	

~~1141~~

Group C. Marketing and business managers who were originally engineers.
(We can think of only three, we should have at least six.)

Roger Cady
Jerry Dulaney
Bob Savel

Honorary Chairman - Ken Olsen

Chairman - Gordon Bell

Vice Chairman - Allan Kent
- Dick Best

Secretary - To be selected by membership

/cjf



INTEROFFICE MEMORANDUM

TO: 00D

DATE: January 29, 1975

FROM: Gordon Bell

1142

DEPT: 00D

EXT: 2236 LOC: ML12/A51

SUBJ: 00D STAFF AGENDA--JANUARY 30, 1975

12:30 Lunch	Gathering data for product spec, on line technical editing for orders--information	Laut/Goldfein
1:30	Semiconductor Proposal	Lemaire
2:30	Decision on Stocky's request for budget over-run to maintain the group.	

GB:mjk

FUTURE AGENDA ITEMS

<u>Date</u>	<u>Topic</u>	<u>Responsible</u>
2/6	Expense visibility on recruiting expenses	Abbett
2/20	Production communications (1/qt.)	Cudmore
2/20	Perception of Product Manager function-- outline for workshop presentation	Portner/Clayton Puffer/Bell
3/13	Field Service communications (1/qt)	Shields
3/13	DEC Safety Standard	Cudmore/Minezzi
3/16	Analysis of Product Manager's Workshop	Abbett/Cronkite
?	Hardware/Software Systems Plan	Portner/Clayton
?	2x2 Report	Puffer

digital

INTEROFFICE MEMORANDUM

TO: 00D
 cc: Mark Abbett

DATE: January 22, 1975
 FROM: Gordon Bell
 DEPT: 00D
 EXT: 2236 LOC: ML12/A51

SUBJ: STAFF MEETING AGENDA--JANUARY 23, 1975

12:30 Lunch	12", integrated, low cost terminal with TPS proposal Information	Stocky
1:30	Salary Planning - Proposal Information	Abbett Becky Hawes
2:00	Charging of interview expenses for college recruiting Proposal	Abbett
2:15	Engineering Committee Absenteeism--attachment Discussion	Puffer
2:30	Gathering data for product spec, on line technical editing of orders--Information	Laut Goldfein
3:30	Budgeting for tests (see Puffer-Cudmore interchange) Discussion	Puffer
4:30	Budgetary changes	Croxon Morris

Future Agenda Items

<u>Date</u>	<u>Topic</u>	<u>Responsible</u>
	Hardware/Software Systems Plan 2x2 report	Portner/Clayton Puffer
2/20	Perception of Product Manager function-- outline for workshop presentation	Portner/Clayton Puffer/Bell
3/13	DEC Safety Standard	Cudmore
3/16	Analysis of Product Manager's Workshop	Abbett/Cronkite



INTEROFFICE MEMORANDUM

1144

TO: 00D
DATE: January 14, 1975
CC: Mark Abbett
Jim Cudmore
Dick Best
FROM: Gordon Bell
DEPT: 00D
EXT: 2236 LOC: ML12/A51
SUBJ: 00D STAFF MEETING MINUTES--January 9, 1975

1. John Cronkite presented the Product Manager's school.
2. Best and Amann--we are asking Jim Cudmore to come back in 8 weeks with a DEC Safety Standard. Ron Minezzi is presenting a first pass at Engineering Committee. *March 13*
3. Ken described the organization vis a vis the Woods Meetings. The implications for us:
 - A. It may be appropriate to have an interface to P/L's similar to their interface with manufacturing, finance, personnel (sales has a similar problem).
 - B. We are moving to systems versus computer components (e.g. disk) PSG's for P/L interface. Computer component level will exist intra central engineering.
4. We approved Nat's plan to establish a Communications Review Board inside the software standards framework.
5. Gordon will call Leng and Marcus relative to the problem of planning and building communications systems.
6. The production interface. The 2x2--Bob will work on it specifically with Howard Reed and Jim Cudmore (if appropriate). The issue certainly needs cleaning up and a plan. Bob should report back on this. *?*
7. Stocky came to ask for \$20K-40K for a 12", integrated, low cost terminal with TPS (20K for terminal, 20K for TPS). Stocky will deliver a 1 page proposal on the subject. *→*

GB:mjk

Future Items:

1. Hardware/Software Systems Plan

Portner/Clayton



INTEROFFICE MEMORANDUM

TO: O²D

DATE: January 14, 1975

FROM: Mark Abbett

DEPT: Central Engineering Personnel

EXT: 2633 LOC: ML12/All

SUBJ: PERSONNEL COMMITMENTS FROM
1/9/75 O²D STAFF MEETING

Following John Cronkite's presentation on the design of the Product Managers Workshop, the following commitments and decisions were agreed to:

- 1. That individual participants will be charged for expenses.
- * 2. That the O²D Vice Presidents will be asked to discuss their perceptions of the Product Management function. Outlines for this presentation should be discussed at Gordon's February 20th Staff Meeting.
- 3. One Vice President will be responsible for the wrap-up and concluding remarks. This commitment should be made by February 1st.
- 4. That the hand-out information should include articles on Product Management.
- 5. That John Cronkite will draft a letter to participants for Vice Presidential signature by January 16th.
- 6. That John Cronkite and Dick Clayton will have the responsibility of talking to Win, Bill Long, Julius, Brad Vachon, Charlie Spector, and John Leng to ask for their participation in the Workshop and explain it's design. Product Line Managers will be asked to participate in the second full day.
- 7. A questionnaire will be designed to ask participants what was learned, what follow-up is needed, what is the frequency and design of future meetings, and who should be invited to future sessions, etc. The questionnaire should be as descriptive as possible.
- * 8. At the March 6th Staff Meeting, following this Workshop, one agenda item should be an analysis and follow-up commitments as a result of the Workshop.

clg

cc: John Cronkite
Mary Jane Keeney

* Mary Jane: Please note for future meetings



INTEROFFICE MEMORANDUM

TO: Distribution

DATE: January 29, 1975

FROM: Gordon Bell

1146

DEPT: 00D

EXT: 2236 LOC: ML12/A51

SUBJ: IBM SYSTEM 32

Everybody's got their idea of what the significance of the IBM System 32 is. As I read the press releases and all the other documentation associated with it, it is clear to me that the main significance of the announcement is that IBM is trying to address the programming problem by first, having a machine that is just basically an RPG 2 machine; and secondly, and most important, providing a set of applications programs which are tailored to particular industries together with a set of input parameters which allow programs to be constructed for specific cases. That is, they are writing a program that is essentially a program writer, and thereby hoping to eliminate the need for the programmer, or programming as we know it today on an applications basis.

I think it is important for us to go out quickly and get the documents associated with this and see what techniques they have developed, and see if we can formulate how these techniques, i.e. new programming technology, can be applied for our own use.

I think they know something that we don't know.

GB:mjk

Distribution

02D

Peter Christy

Ed Favre

Irwin Jacobs

Dave Schroeder

Pete Van Roekens

digital

1147

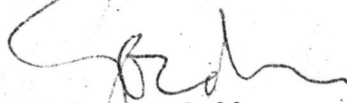
December 4, 1974

Dr. Craig Fields
ARPA
1400 Wilson Blvd.
Arlington, Virginia 22209

Dear Craig:

Here's the research proposal we discussed. Hope to get your reaction next Wednesday.

Sincerely,



Gordon Bell
Vice President
Engineering

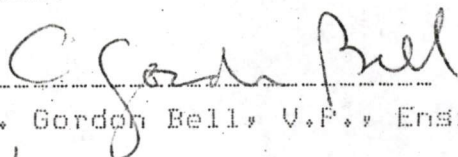
GB:mjk

COMPUTER TERMINAL RESEARCH

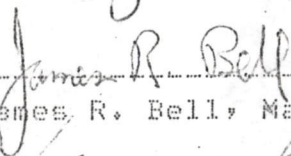
A Proposal
by
Digital Equipment Corporation
Maynard, Massachusetts

to the
Advanced Research Projects Agency
Department of Defense

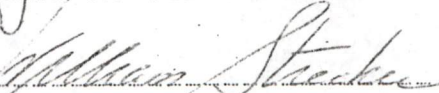
Approvals:



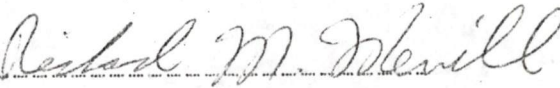
C. Gordon Bell, V.P., Engineering



James R. Bell, Manager, R&D



William Strecker, Supervisor, R&D



Richard M. Merrill, A/N Displays



Mark J. Sebern, R&D

A PROPOSAL FOR TERMINAL RESEARCH

Overview

There are several differing approaches to the development of a portable computer terminal, each appropriate to a certain set of design criteria. One option is exemplified by commercially available thermal printers, while hand-held teleprinter replacements illustrate another. There are also large variations in local storage and processing power, as well as in packaging and power supply. While no single research effort is likely to produce a unit with all desirable features, it is the intent of this proposal to advocate two distinct, yet related, avenues of investigation.

Portable Terminal System

The first area of proposed research is the development of a self-contained Portable Terminal System (PTS). We propose to build for ARPA an engineering prototype of a system that will replace an ASR33 (or model 40) Teletype in all possible modes: off-line editing, on-line full-duplex, and remote protocol operation. The PTS will incorporate a five inch video display refreshed from memory with three operating modes: (1) large characters, 40 columns by nine rows; (2) small characters, 80 columns by eighteen rows, for text editing; and (3) graphic mode for vector drawings or signature verification. This last mode requires a 4K byte fast memory and provides a resolution of eight dots per inch.

The PTS will incorporate a standard N-key rollover Digital keyboard and an available eight bit microprocessor. A model has already been shown capable of sustained operation at 9600 baud over an asynchronous line.

The PTS will be packaged in two attache cases, each capable of fitting under an airline seat. The first case will contain the controls, video display, UART, memory, and keyboard, while the second will hold two floppy disk drives (or cassettes) and a copier. For the engineering prototype, each would contain its own transformerless power supply.

The second proposed research project will investigate consumer equipment systems (CES); that is, systems which use available consumer products as components in terminal or computation applications. Specifically, the first phase of this work will be the construction of a low cost, variable character set terminal, using a standard television receiver as the display. The proposed 256-character set will consist of contiguous eight by twelve dot matrices, allowing graphic capability by appropriate character definition, an approach that has been demonstrated in the DEC VT-30 display system. Further enhancements, such as color display on a standard color television set, will also be considered.

The flexibility of a dynamically variable character set, together with the inclusion of a small microprocessor like the DEC PDP-11/WD, will provide considerable latitude in application. The terminal will likely resemble a DEC RT02 remote data entry terminal, less the display. A full ASCII or other keyboard will be provided, together with connections for the TV antenna lead, serial line, and optional audio cassette. Such a terminal can automatically request its character set from a host system, or load that data from cassette, thus facilitating limited graphics, foreign language processing, unusual type fonts (such as APL), complete mathematical notation, and a variety of other applications.

Since the utility of any hardware system depends greatly on appropriate software support, the second phase of this research will include the design and implementation of a small number of applications software packages for use with the variable character set terminal described above. These applications will be chosen from the fields of engineering computation, office automation, computer aided learning, small business systems, household computer uses, and the like. While this software will be in the nature of a demonstration, the selected problem areas will be sufficiently realistic to test the utility of this terminal design.

Concurrent with this software development will be further exploration of Consumer Equipment Systems. This effort will continue work on the use of ordinary audio cassette recorders for data storage, consider employing broadcast FM subcarriers as a means of data base access, study the use of commercial video recorders in terminal and stand-alone applications, and so on. The goals of this part of the investigation are to develop hardware/software systems which exploit the variety of consumer electronic equipment now available, and to assess the worth of this approach in bringing computing power to a larger segment of the public.

Schedule and Cost

1151

Each of these two research projects will be headed by its own principal investigator. They will proceed independently, while sharing support personnel and services. The PTS project will require two engineers full time with support services for a total cost of \$135,000 over nine months. It will yield a complete PTS system, along with technical documentation.

The CES project will involve one engineer and one programmer each two-thirds time with support services for a total cost of \$120,000 over eighteen months. It will provide two preliminary reports at six month intervals and a final research report, with one or more operating prototypes and accompanying applications software.

Submitted by:



Richard M. Merrill
Principal Investigator, PTS



Mark J. Sebern
Principal Investigator, CES

digital

INTEROFFICE MEMORANDUM

TO: 00D

DATE: January 8, 1975

FROM: Gordon Bell

DEPT: 00D

EXT: 2236 LOC: ML12/A51

SUBJ: 00D STAFF MEETING AGENDA--January 9, 1975

12:30 Lunch	Course outline for Product Managers Workshop	Cronkite Abbett
1:30	Fire hazards in our equipment.	Puffer Amann Best
2:15	Separate standards process for networks.	Portner Teichholtz
2:30	Report on Operations Committee Woods Meeting	Clayton Bell
2:45 3:00 4:00	3 Short Items <i>Stocky</i> Systems	Bell Bell Portner Clayton
2:55		

mjk



INTEROFFICE MEMORANDUM

TO: 00D

DATE: 1/2/75

FROM: Gordon Bell

DEPT: 00D

EXT: 2236 LOC: 12-1

SUBJ: STAFF MEETING AGENDA--JAN 2, 1975

12:00 Status of Reallocation of people Abbett
Lunch

1:00 Joint Software/Hardware Planning Proposal Portner

(Henry Lemaire will join you today.)

mj

digital

INTEROFFICE MEMORANDUM

TO: 00D

DATE: December 17, 1974

FROM: Gordon Bell

DEPT: 00D

EXT: 2236 LOC: ML12/A51

SUBJ: 00D STAFF MEETING AGENDA--DECEMBER 19, 197412:30 Budgets
Lunch

Croxon

1:30 Primate Exchange

Bill Thompson's proposal
How/who to do?

Thompson

PSG's--clarifying their roles, low keying
some, beefing up others. Who to do?2:30 Personnel--proposal for engineering manager
categories.

Abbett

3:00 Proposal to integrate graphics as a central
product.

Hindle, Kramer, Halio

4:30 EEO audit update

Otis Courtney

Future Agenda Items:

Review of Quality and Field Integration--who to organize?

PDP-11 Handbook

GB:mjk

TO: Win Hindle
Ed Kramer
✓ Gordon Bell
(Chairman, Products Committee)

DATE: November 5, 1974

FROM: Len Halio

DEPT: Graphic Display Systems

EXT: 6935 LOC: MR2-4

NOV 07 1974

[O²D - For discussion
at Staff Mtg.
+ return.]

SUBJ: Graphics Funding

Over the past two years the growth of the Graphic Systems Product Line has been both impressive and consistent.

I believe this is due to the high degree of identity and "esprit de corp" of the people associated with it as well as the ability of the principles to formulate cogent long term business plans which mature into real products, in a timely fashion. This ability to focus on a business, set plans, and then bring resources to bear to complete those plans is, of course, the forte of a product line structure.

The disadvantage for graphics, is that it is a product in a market oriented company. The true long term growth of graphic products lies in their ability to become a necessary tool in many diverse markets; from a designers console, to a real time process monitor, to the output terminal of a management information system.

The structure to accomplish this at DEC today is through central engineering funding. As a central facility, the graphics group, in conjunction with the product lines (through the PSG), is free to develop consistent long term plans with some surety of funding depending on its past performance and current requirements (much as a product line).

The facility of shared funding by contrast is self defeating in this respect. If it was the Products Committee's desire in suggesting shared funding for graphics so as to protect its growth, I submit shared funding accomplishes precisely the opposite effect.

- * When product lines budget the next years engineering budget, they may not know the detail of the projects they will begin that year, but rather that some level of engineering will be required. This money is committed to a hiring plan to sustain that growth. When the product line is approached for shared monies, it is not uncommon to find all the engineering funds committed for internal projects and people.
- * Budget adjustments and cuts usually reflect disproportionately on a shared project as opposed to internal product line efforts. Unless the project is basic to the business, (usually handled by

Make it great with graphics

FY '73

FY '74

FY '75

\$2M

\$1M

\$0M

Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4 Q1

\$12M

\$10M

\$8M

\$6M

\$4M

\$2M

Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4 Q1

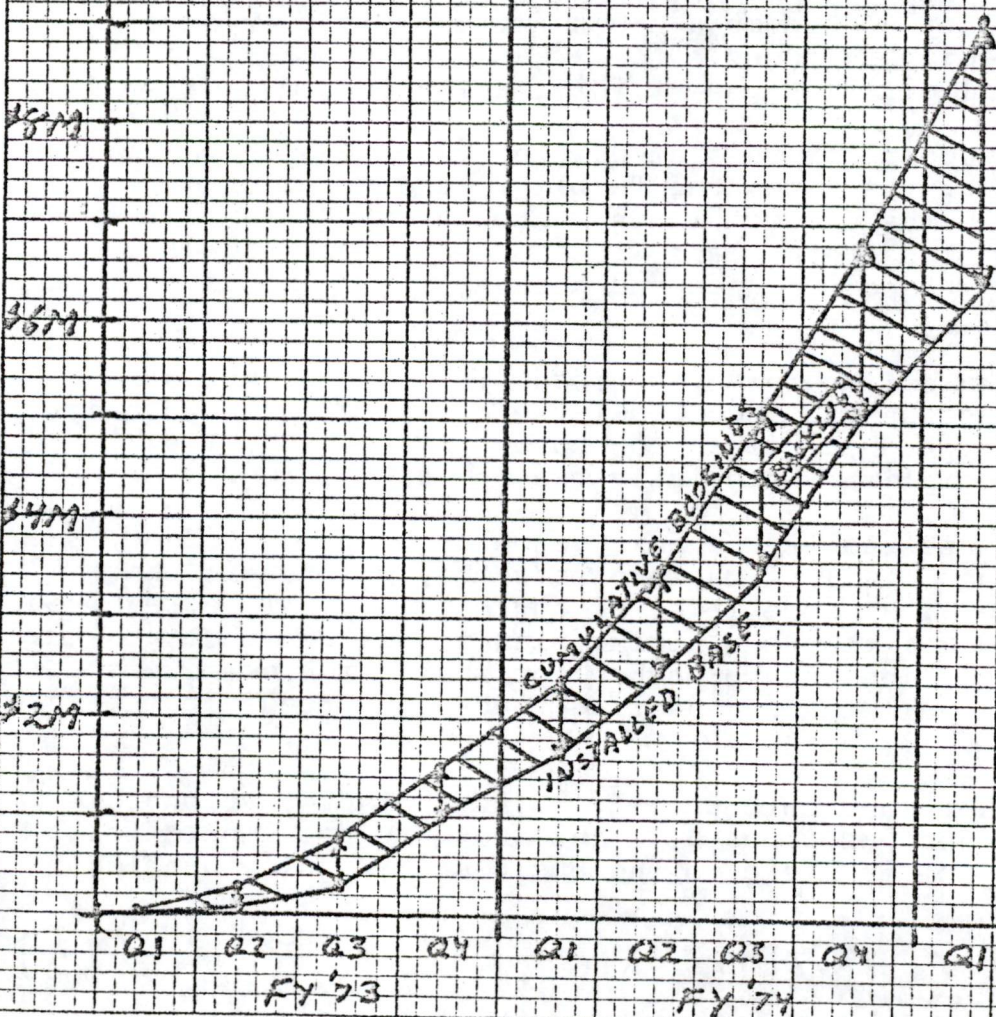
FY '73

FY '74

FY '75

GRAPHICS - PL 39

3 YR GROWTH PERFORMANCE



internal groups), product lines will usually opt to drastically reduce or eliminate funds for shared efforts rather than affect internal projects during times of cut-back.

- * There is no funding continuity. Whereas a product line can base its future growth on past successes, a shared group has no formula for continued funding, it operates solely on a project to project basis. Hence, long term issues are clouded and low yield, but essential efforts such as support usually suffer. Personnel motivation is difficult.
- * Launching a project becomes a complex and frustrating simultaneous equation of project definition, product definition, funding parameters and continuous budget adjustment, as product lines jockey for a most beneficial position.

Many of the above objections are either eliminated or greatly reduced by either becoming centrally funded (that algorithm allows continuous funding based on current use of product types) or, of course, by becoming a stand-alone product line.

However, as a stand-alone product line we would diminish the incentive of product lines using our products. Unrestricted selling of the products is possible only if the expenses of development and support can be accrued back to the parent product line. Central funding eliminates this problem. Another possibility is to set up a "dealership/product line". Here not only will the graphics product line sell directly to the market, but will sell through the normal product lines where appropriate (i.e. ECP, IPG, LDP, etc.) at a discount equal to the savings of selling cost and warranty. At first this might be viewed as counter-productive time, but it is essential to return revenues to offset the expenses. Any time wasted setting up this procedure is probably less than that spent in trying to secure funding under the shared arrangement.

In summary then, I believe central funding is proper for the graphics effort or secondarily, a product line structure (actually first as my personal bias). However, the shared funding proposal should be avoided as most disruptive to the emerging graphic business.





INTEROFFICE MEMORANDUM

TO: ✓ Gordon Bell
Dick Clayton
Bob Puffer
Phil Laut

DATE: December 9, 1974

1157

FROM: *Mark Abbett*
Mark Abbett

DEPT: Central Development Personnel

EXT: 2633 LOC: ML12/All

SUBJ: DEFINING LEVELS OF ENGINEERING
MANAGER POSITIONS

DEC 11 1974

BACKGROUND

There are presently three levels of Engineering Manager positions: E01, Group Engineering Manager, E15, Senior Engineering Manager, and E02, Engineering Manager. There is no consistency in how we have our people classified. For example, Jega Arulpragasam is classified as a Group Engineering Manager, while two levels below at Engineering Manager we have John Clarke, Steve Teicher, and Lorrin Gale. Bill Demmer, for some reason, is classified as a Product Line Manager and Grant Saviers as a Senior Engineering Manager.

Attached is a first pass at setting up some criteria for each classification. There may be some additional criteria that should be used and some existing criteria that should be eliminated. I feel a little bit nervous as to the different levels of scope of responsibility and complexity of products and would appreciate any inputs from you in further definition. Please consider the criteria and I will be setting up a one half hour meeting with you during next week to discuss this in more detail. The goal will be to get some agreement at Gordon's next Staff Meeting.

clg

cc: Dave Larson
Brian McDonald
Jerry Patton
Joe Underwood

ENGINEERING MANAGER CLASSIFICATIONS (Must have Cost Center responsibility to qualify)

<u>LEVELS</u>	<u>SALARY RANGE</u>			<u>CRITERIA</u>		
	Min.	Mid.	Max.	<u>BUDGET</u>	<u>ORGANIZATION SIZE</u>	<u>SCOPE OF RESPONSIBILITY</u>
Grp. Eng. Manager E01	27	35.1	43.2	\$2 to \$4 million	40 and more employees	design, marketing and product support
Sr. Eng. Manager E15	20.7	26.5	32.3	\$1 to \$2 million	20 - 40 employees	design, ^{quality,} and product support
Eng. Manager E02	19.2	24	28.9	\$0 to \$1 million	10 - 20 Generally split between hourly & professional employees	design, some times product support, & no marketing

Responsible for several areas - i.e. a range.

?? →

Responsible for profitability for a # of products.

*Project Eng.
- Senr. P.E.
- P.M.
- S.P.M.]*

<u>NUMBER OF PRODUCTS</u>	<u>IMPACT OF PRODUCTS ON CORPORATE BUSINESS</u>	<u>COMPLEXITY OF PRODUCTS</u>	<u>SAMPLING OF MANAGERS</u>	<u>PRESENT SALARIES</u>	<u>SIZE OF ORGANIZATION</u>	<u>BUDGETS IN MILLION OF DOLLARS</u>
a family of products	50 - 100 million in sales	usually state of-the-art technology design	Demmer Saviers	40 K 30.3K	75 65	3.8 3.8
2 products	15 - 50 million in sales	heavy design although fairly standard	Teicher Clarke Delagi Corell	23 K 31.8K 30.8K 27 K	26 22 14 36	2.0 2.035 .621 2.0
1 product	0 - 15 million in sales *Can be budgeted or projected sales.	fairly standard design with heavy product support	Arulpragasam Ryder Platz Gonzales	32 K 29.5K 23 K 21.3K	19 18 21 11	.875 1.2 1.1 .408

digital

INTEROFFICE MEMORANDUM

1160

Bob

TO: Phil Laut
Gordon Bell
Al Bertocchi
Bob Lander

DATE: November 20, 1974

FROM: Bill Thompson

DEPT: Corporate Planning

EXT: 3779

LOC: PK 3-2

NOV 27 1974

NOV 21 1974

SUBJ: Planning and Control of Engineering Expense

For several years you and I have been theorizing a better way to plan and control (understand) engineering expense. You have been doing this for your end as best the system will allow. The current system focuses the company by cost center to the project. A more appropriate focus is the project--the cost center is only an accounting convenience. My current feel of conditions - we have planned more projects than is rational - Products Committee calmly discussed how "norm" was currently 2X plan on major projects - Ken says he can't see what is going on - leads me to conclude the time is ripe to change.

I propose that all planning, budgeting and measuring be done by project. This should be done for both Central and Product Line Engineering. Specifically, this would mean:

1. Resource allocation by project
2. First level budgeting by project
3. Corporate focus on variance analysis by project
4. Budgets would be for the life of project not a fiscal year
5. Clear view of "committed" expenditure
6. Breaking out projects between investment in the future and support
7. Cost center managers focus should be overhead costs to support his "direct labor"
8. Close the reporting loop between the strategy groups understanding of project and reality.

I clearly see the advantage of project control as a great improvement in communication within and without engineering. The best example is the current reallocation of resources due to budget. It would be beautiful to communicate the ever changing priorities by the project that has been changed. How many people have different views of the active committed projects?

I would like to see you set this project as a clear short term objective. I would like to spend time with you specing the specifics.

/p

To → Gordon Bell
I agree
Bob Lander

MJ - Agenda - O²D, ask Thompson

Phil + Al + Bob + O²D
Subject of O²D?
to O²D



INTEROFFICE MEMORANDUM

TO: Vince Bastiani
Roger Cady
Julius Marcus

DATE: February 11, 1975

1161

FROM: Gordon Bell

DEPT: 00D

EXT: 2236 LOC: ML12/A51

SUBJ: GETTING RID OF MODEMS WITH A TIMESHARED DIGITAL FILTER

The BTL 1 Mhz digital filter has 32-8 Khz filters. I believe this single system could replace 32 modems (or more) with direct inputs to the filters.

GB:mjk

cc: Jessee Lipcon
Ed Kramer
Mark Sebern

digital

INTEROFFICE MEMORANDUM

TO: Bill McBride
CC: Ed Kramer
John Mucci
George Thissell

DATE: February 12, 1975

FROM: Gordon Bell

1162

DEPT: 00D

EXT: 2236 LOC: ML12/A51

SUBJ: ED FREDKIN/GT44

I got a call from Ed Fredkin at 213-796-7063, who's visiting Cal. Tech (from MIT). He is the owner of a GT44 with extended memory. He's not getting much work out of it because the software isn't especially good, and is complex.

He would like help of some kind. Can you please call him regarding help?

GB:mjk



INTEROFFICE MEMORANDUM

TO: Phil Laut
Bob Puffer
Grant Saviers

DATE: February 12, 1975

1163

FROM: Gordon Bell

DEPT: 00D

EXT: 2236 LOC: ML12/A51

SUBJ: ATTACHED LIST OF PRODUCTS (PROJECTS) WHICH WOULD BE DROPPED

There is still clear hostility toward the disk group as evidenced by products which the group VP and PLM's would like to kill.

I believe the area is getting better, and the current RK06/7/RP02/Trident/RSL strategy is a place to establish clear leadership and demonstrate good business sense. 00D has to do everything to come up with a really good strategy on the disk and tape areas.

I wanted TS02 for program distribution and backup. The PLM's say--distribute RSL, (floppy--too small) etc. Also TS02 will backup an RK06--there is a real education problem as to why this is a good product to me, as I currently favor it. They would have also dropped anything else given the chance (knowledge), e.g. 6250 tape.

GB:mjk

Attachment

SUBJ: KL10

DATE:
FROM:

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GORDON BELL

* * * * *
PLEASESEND TO: FILE
* * * * *

SUBJ: USING A KL10 (or equivalent) TO GET US TO UNDERSTAND
VIROS (SNARK) + 11/85

To: Bruce DeLad

Somehow I believe we (you) have to get 20 or so terminals
to the above computer as a mechanism for the product lines
who will be selling UNICORNS with such a system; they would
use it as communication medium:

1. All messages would be communicated via MAIL--directly
to you and your group. All specs, manuals would be stored
there.
2. Learn the software.
3. Use the software in real life (e.g. editors, typesetting)
to do secretarial work.
4. Benchmark the system.
5. Learn some of the exotic languages--APL, DBMS, SIMULA,
COBOL (multi-terminal).

How and when can we start? Is there a cheap enough 2020?
What about more terminals on the VIROS system in Marlboro?
GB:mik

cc: Dick Clayton, Roger Gourd, Bill Kiesewetter, John Leng
Mike Mensh

SUBJ: STRATEGY/BUDGET SEQUENCE

DATE:
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* * * * *
PLEASESEND TO: FILE
* * * * *

To: Distribution

Bill Thompson has proposed the following sequence to firm up the strategy/budget:

1. The Marketing Committee will iterate over the sequence of products as they did in the first meeting. It would also be very helpful if we could provide cogent input...
2. Technology strategy (cogent input). Why are we doing what we are doing in each area? Where do we stand in the area? Is it a matter of need, competition, cost reduction, etc....I believe this entire statement should be no longer than 20 pages for all, and each area should be about one page with a statement, a set of graphs as to where we are-- growth, NOR, etc.
3. Product Line Interaction at a high level with PLM + PL Mkt + PL Dev. etc. managers. Thompson has proposed a 1/2 day meeting of OOD with each PL, at which time, we go over the strategy with each PL (about 5 or 6 people from the PL). I believe we must use this opportunity to jointly interact with the PL's at this level...It will get a lot of the noise out of the system that we currently have. Also, I'm looking forward to trying to understand their businesses and the products needed.
4. Products Committee. We must use them as a warmup-test for the woods and we will present strategy/budget there. The next Tuesday will be dry run.

OOD. We need a proposal, and dress rehearsal for the Woods meeting.

The areas: 8 (hardware-software), memory, disk, tape, terminals (Puffer for all, including alphanumeric), LSI-11-micro, small, medium and large computer systems, communications and network,

SUBJ: STRATEGY/BUDGET SEQUENCE

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non-human (real time) systems, human interfaced systems (time-shared + single user), languages, Software/systems size matrixes vs time should also be included.

I believe it would be best if each of you wrote the above sections, and I want to write an overview. (Right now, the COMM section is up to Julius, and I.) I want to soon get Dick and Larry involved as it is a network problem.

What you think?

GB:mik

Distribution

OOD

Henry Lemaire
Julius Marcus
Bill Thompson

Baspro

SUBJ: COMMENTS ON TERMINALS

DATE:
FROM:

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GORDON BELL

1167

* * * * *
PLEASESEND TO: FILE
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SUBJ: COMMENTS ON COMPUTING WITH TOPS 10/BASIC/LA30/VT05 &
FROM HOME (OR CONFESSIONS OF A CLOSET PROGRAMMER)

To: Distribution

Over the last 10 weeks I have spent probably on the order of 10 to 20 hours per week programming, totally using the BASIC language from the DEC-10. I have an LA30 and VT05 coupled together and I have computed almost totally from home. During that time, the whole thing, a side from the fact that I have developed a useful program and have gained a lot of insight into the financial aspects of products, has been useful from a learning experience. I would highly recommend it. It is a completely self-taught kind of thing, and it can be done in the privacy of your own home--hence, no one knows how slow, fast, or badly one learns. Programming isn't totally foreign to me. I have written some relatively good sized programs, but the last serious programming I was involved with was the PDP-6 monitor and the beginning of the design automation programming at DEC. While at CMU I wrote a few programs in a teaching mode to make sure I knew enough about the language to teach them.

I think it is especially important for the management of DEC to engage in this, because we don't pay enough attention to programming. It is almost essential in fact, if one hasn't done a substantial amount of programming, to re-engage in it for a few months to write something of a fairly serious nature--at least a several hundred line program that actually does something that one wants done or would like to be able to understand.

The comments on the whole process can be broken into the various component parts--the terminal, the phone line, the people you interface with while doing the program (those who run the system, maintain the various languages, and others who use the system), the system itself in this case--the engineering PDP-10 CS/2, and

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DATE:

FROM:

the language that one uses to write the program, and of course the customer--in this case, myself and Phil Laut.

THE PROGRAM

The program is called Phil's Financial Desk Calculator, which is in fact a collection of subroutines and some specific programs put together which do the dog work that is associated with a lot of the financial kind of reporting that Phil Laut does. It is about 1500 lines long. The key program that we are using now is a program that looks at a product over its entire lifetime and calculates product contribution, ROI, and all other kinds of parameters given the sales and cost data. The key attribute of the program is that there are a lot of variables and one can search a space and compare the results of a program under various conditions including project slip date, number of units sold, price increases/decreases, cost increases/decreases, and a variable work in process and a variable accounts receivable, all of which affect the product contribution. In fact, it can be used a number of ways: First, given the product, look how good it is, and how sensitive it is to various disasters that have been known to befall other products. Second, given the notion of a product, and the cost, one can find out how many units one has to sell for a product to be successful. Third, do exploration into pricing, and the sensitivity of payoff to volume. Fourth, go back and look at certain products; for example, the whole history of the -10, and determine its success as a product.

The thing is relatively easy to use. For example, by typing in about a half a page of numbers (which takes about 5 to 10 minutes) for a product like the LA36, I can get results in 10 minutes and start the exploration of the space looking for what the effects of various market and pricing conditions are. Here the important thing is that this whole thing has got to be interactive. In a system like this, one cannot calculate most of these things in a closed form because of the non-linearities; and in effect what we are doing in each case is really simulating the product conditions. Thus in doing it one can quickly essentially simulate various marketing conditions and arrive at alternatives in the 'what if' situations.

This is the kind of interactive optimization and use of computers that is sadly missing from DEC. Nearly all of our use of computers within EDP and Manufacturing is clearly pre 1950--the task is to keep score, not help with the game.

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Another interesting thing I learned was that a free format input program isn't quite right. Initially one simply typed in the product plan; now the program asks for various attributes of the plan in a prompting (check list) mode, and input is substantially faster.

To a large extent, the program is successful, but to a certain extent it still needs improvement. To some extent that it fails is my fault, but I certainly put a large share of the blame on the -10 BASIC language. BASIC is a depressing story onto itself.

TERMINALS

Anybody who uses a computer has quite strong feelings about the terminal, because even though it is not the terminal the user sees all the time, the terminal is what the user appears to see. To the extent the keyboard feels right and the response time is right, one may enjoy or dislike a particular terminal. Terminals we are all talking about here are purely the dumb kind. Even the low cost terminal. If you look at the whole system from a cost standpoint, then the terminal is clearly the lowest cost component of the system. That is, the user's time is the most expensive, the system time is the 2nd most expensive, and the cost of the terminal is clearly the least expensive part of the system; hence, the feelings about terminals is quite justified. For the terminals we use at DEC and the people who use them, the cost of the terminal is insignificant; and anything that can be done to get 5% out of the process by better coupling of human to machine, pays off extremely rapidly.

FEELINGS ON TERMINALS

I got both a CRT and an LA30 by accident. I started out with a CRT (VT05) and found I couldn't use it because I didn't have hard copy, and I was finding that I was writing my program in long hand, putting them in, and then as I made changes I had to make them in long hand and the next day I would get a hard copy from the machine. The whole process was extremely tedious.

Quite by accident I brought an LA30 home in addition to the VT05 and found to my amazement that I in fact needed and used them both, but now I believe that this is the only civilized way to compute. The VT05 is by far the most pleasant terminal to interact with--there is no head to get in the way of

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viewing; there is no head noise; the terminal is substantially quieter; and finally one is viewing the text at a normal angle, and one can see 20 lines simultaneously as contrasted with only a few in the LA30 in a convenient way without moving the hands.

Beneath the terminals the wiring is a mess. It is like component hifi. There is a modem with 2 long cables to the 2 terminals, the terminals plug in, the modem plugs in, and a phone is involved. (I finally had to get a second phone because it was beginning to interfere with the rest of the family.) Especially since I was on the computer one day for 13 1/2 hours but it certainly kept the incoming phone calls down.) In the case of these 2 terminals, generally they are too big and too heavy, and too noisy. The VT05 is quite long, and it is hard to get a desk or table that is right. The LA30 is hard to move and as a result the things occupy quite a space, and I have not yet found a very good way of positioning them together. This is doubly true since the conventional desks are not of the same height as the LA36, so one ends up with a height differential of about 6 inches between the 2 terminals. You have to have 2 chairs, or one slides around and sort of makes do with what one has. Along this whole thing of having portable terminals, I have noticed a great number of TI terminals used within DEC simply because they are portable and quiet. I used one for one weekend and wasn't really that satisfied with it because the thing wasn't dark enough to suit me. The modems that we sell certainly leave a lot to be desired and they don't always work at the high speeds; although generally once one finds one that works, it will generally work at low speed.

From a speed standpoint, I have been quite satisfied at running at 30 ch/sec., and on many occasions I have used the terminal as a line printer. It can type out say 2 pages of a program, which is about all I can type in in an evening, and get running. So I simply set it to type out, then go away, and it grinds away. I would be dead without this. The thing about writing programs, if you do have 30 ch/sec, that is about all one is capable of reading. By doing that, one really works hard to first fit in the space in the time that you can get in 30 ch/sec; and secondly, really work on the human interface so that you don't have to type and read a lot. 30 ch/sec. is about all one can process, unless it is poorly organized.

The whole thing of an environment issue is that you are programming interactively. I find that noise generally

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distracts me. From this point of view, I want to do a lot in our terminal room. I think that we have to put baffles on every teletype in the public terminal rooms, because I just don't see how people can accomplish very much with lots of terminals going all the time. This is in the particularly low noise environment, so it hits me quite hard. In fact I am able to do almost anything else in a high noise environment, but I simply can't program very well without relative quiet. From my standpoint, I am certainly motivated to work on the noise aspects of the mill to get better conditions for programmers. It really is difficult to program without a pretty quiet environment.

Both of these terminals simply take up so much space, I can't allocate any typewriter space. The thing that probably bugs me most about our terminals is that they don't really behave well as a typewriter, and they must. One thing that you clearly want to do with a terminal is to use them as a typewriter. I am now using the terminal as a typewriter--the standard editing program on occasion, but generally just a typewriter--and I am finding that not having upper/lower case and backspace, in the case of the LA30, is just intolerable. I am happy to say that the LA36 solves all these problems. But again the way that I use the 2 terminals is that I type at the VT05 and then the LA30 is slave to it (I type and read at the VT05 screen).

MODEM

Now going from the modem, one encounters the telephone system. In general this is a pain. I have been in an environment apparently coupled through the Waltham exchange, and through the Arlington 646 exchange, and the whole thing is bad. On rainy nights I can't run at 300 baud. Perhaps it's my modem. (I finally bought some outside after trying our own!) After a few tries to botch various things up and to get my own direct data set, I sort of resigned myself that the powers that be will tell me how fast I am going to run my terminal. I work at that rate. The other thing I find that my computing bills are slightly higher when I compute at 30 ch./sec. In effect I am getting more out of the computer, and I am getting more work done too--I have a very small sample size; but the faster the terminal the more interaction you get with the machine, and again the expensive part of computing is my time. In fact with the amount I get paid there is probably no way I can afford to compute anyway, unless I program at a fantastic number of instructions/hour. (This is not an argument for you not to program and use the machine--can you imagine a Ford executive

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who always took the train and had no drivers license.)

In going from the phone line and into the Maynard system to DEC phone system, one loses a couple of minutes getting into the appropriate line. We definitely need some dial-in lines in the Arlington area so that one doesn't have to go through the operator to get a connection. That ties up a couple of minutes and what is worse, most of the time the machine is down on an unscheduled basis is because the phone system is patched wrong. I have lost more time because of the poor phone than because of machine downtime. Particularly, in the case of the machine, most all the downtime is scheduled. [I have found the regularly scheduled downtime of Sat. from 5PM to midnight frustrating as this is one of my prime times for programming.]

As one finally gets through the Digital exchange, given that it is patched right, one gets into the computer system and the computer operators.

CS/2 COMPUTER SYSTEM

In general, this part works fine but if it doesn't, the onus has been on the user to prove that it doesn't. In one case, I had to prove that the lines were down at CS/2 before people would go around and try to fix them. In the machine room, there is no capability to dial out through the phone exchange, back through various lines in order to check out if the various dial in lines are working properly.

TOPS 10 SYSTEM--CS/2

As one gets into the computer and through all the operational stuff, and is finally talking to the TOPS 10 monitor, one gets into a couple of fairly subjective areas. In the case of the TOPS 10, I have simply lost touch with what is available there. I found that running in the PDP-10 environment an extremely awesome and bewildering thing to a user who just wants to compute and doesn't really want to get into a knowledge of computing. There is almost no way that one can avoid learning a lot about the system in computing there. For example, even though I am just using the BASIC language, I still have to know a lot about log in, talking to other users, spooling on the line printer, backing up on DECTape, interfacing with the operators, and in general I don't know if this material is covered. Right now I either ask Mary Jane,

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or I ask an operator. I have forgotten almost all about how you talk to the monitor, or monitor commands. I know that what I fought for years ago in the minicomputer area, is that all the information be published. I simply wouldn't know where to start looking to obtain information about computing--getting into the -10, and computing on it. There is a large part of computing that I should know about, even when I am using it, that I simply store in other people and don't know. This should really concern us as designers. I don't know how to avoid it; however, good help commands and much higher speed lines can help.

BASIC

I am using a relatively pure form of BASIC, which runs on the PDP-10, that may have some extensions beyond the original Dartmouth BASIC. I think it is a terribly sad tale to have to say that I am computing in BASIC. BASIC is a horrible language. It is totally a non-structured programming language, and the only thing that BASICs have in common is a name--i.e. BASIC is a license to invent a language. The whole issue of BASIC is beyond the scope of this note, and all I can say is that it is an even sadder thing to find that BASIC was the only alternative that I had in which to compute. My requirements were fairly simple. I needed a system that was fairly easy to use and had both strings and real numbers, random access and sequential files as primitives. The only alternatives I had were APL (I had no terminal), and ALGOL (I didn't think the string statements were sufficient). Alas, I ended up in BASIC. In retrospect, I think I probably should have used ALGOL even though the strings weren't quite up to snuff.

I have learned to structure programs within the limits of BASIC such that I don't spend time which is exponential with program size. With a bit of thought, discipline and many rules, it is possible to write bigger programs in BASIC--although there are limits. My subprograms are about 15-20 lines long--hence, a 20-24 line scope is quite useful.

MACHINE ACCOUNTING AND THE USER

The accounting of the CS/2 time to me is quite good and I believe we must insist that it be used throughout DEC. One is issued monthly bills which reflect storage charges; and I am billed also on CPU time, kill/core/secs., and connect time. Disk read/write times and page charges are also

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Included.

I feel there are fundamentally 2 ways of operating computing: either totally free, or that one has a budget and computes accordingly. Even though this goes into a CC overhead, I really haven't had to budget for computer time yet, because I don't have time to use very much time. The fact that it is accounted, I can look at the bills, and I know what the relative charges are, does permit to make some tradeoffs. That is, when I can I encode information on the disk, I compute rather than have a big program, and in general try to manage the resources according to the charges. I think if everybody did this the machine would run a lot better and more cheaply. I am totally opposed to any kind of a charging scheme that is based on a sort of ad hoc allocated scheme, because that is purely a figment of some accountant's imagination who doesn't understand that with computing you don't have to go through the whole business of allocating and playing games that one does in a complex system involving people where it is too expensive to account things.

I may have a distorted view, but accounting seems to be one of the fine arts where one takes a number of relatively precise tokens, and with gusto and imagination, thinks of different, arbitrary bins to put the tokens in. Generally, by using too few or too many bins or the wrong bins, the obvious can be totally disguised so that no one understands where the tokens are.

The machine knows what it is doing and can account for its resources perfectly. It is simply an accountant's game to play it any other way. I think we must get all the DEC machines run this way, because it is only through knowledge on the part of the users, through the accounting, through the charging, that they can be intelligent in their use of the machine. They will also migrate to the right kinds of languages for the right jobs because of efficiency both in their time and the machine time. Bear in mind that the highest cost is a person's time, so in general the trade offs will always be to have the easiest use.

THERAPY AND HOME COMPUTING

The other thing about using the machine is right now I am finding it an extremely relaxing thing to do; because after working one more hour at DEC a day, and interacting with lots of people, I certainly need a relaxation that is not people intensive. I don't know of anything quite so satisfying as being able to interact with quite such an intelligent device and to build something and get immediate results. Of course

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this whole thing has been contagious in my family. My wife and son (14) are also heavy machine users at this point. I am rationalizing that I am finding out what the computer in the home market is like, permitting them to have their own job number; but in general, they are restricted to run when the machine is lightly loaded. I believe that we need a policy for allowing families to use the machines after hours. It really becomes clear how tedious it is to get a machine to do a job. It is clear to me that from the loading I see after 6, there is a lot of machine there that could be usefully used in teaching families more about computation. I think it would be basically useful. Also I think in some cases, or in many, it would be very helpful if some of the professional programmers did programming at home with their own terminals at home; because again the machine is there, and I believe if they have the discipline of themselves they can get substantially more done in a quiet environment than they can in the mill. This, of course, needs to be looked at on an individual basis.

In the case of programmers, alternative work pattern contracts might be drawn up with conditions such as:

1. Daily report in times would be via terminal at home.
2. Computer used for most memos and meeting notices to appear at DEC.
3. Regular pattern of interaction days.
4. Some use of machine during low accounting hours to achieve a better load on the machine.
5. Some contract agreements on productivity, but with the security of having a full-time job.

GB:mik

Distribution

Product Line Managers

OOD

Jim Bell

Al Brown

John Clarke

Pete Conklin

Ed Corell

Bill Demmer

SUBJ: COMMENTS ON TERMINALS

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- Len Hallö
- Al Huefner
- Jim Mills
- Clay Neal
- Ron Rutledge
- Mark Sebern
- Tom Stockebrand
- Steve Teicher
- Nat Teichholtz
- Pete Van Roekens
- Larry Wade
- John Wolaver
- Mel Woolsey



February 17, 1975

Mr. George Michaels
Computation Group
Lawrence Livermore Laboratory
Livermore, California 94550

Dear George:

I'm glad you invited me to talk at LLL, and look forward to seeing the laboratory again. I hope I'll have time to see various facilities, and to interact with you about where you think computation is headed. I hope Dr. Fernbach will be available for some discussion. The abstract of a talk is enclosed, which gives a view of this.

I'm in the process of collecting parts from past computers, such that we might someday have a museum at DEC. Is there any chance of getting parts from some of the machines LLL has used and/or spawned--especially LARC, the CDC machines and Stretch?

Sincerely,

A handwritten signature in cursive script, appearing to read "Gordon Bell".

Gordon Bell
Vice President, Office of Development
Professor, Computer Science
Carnegie-Mellon University (on leave)

GB:mjk

Enclosure

digital

INTEROFFICE MEMORANDUM

TO: PLM
00D

DATE: February 17, 1975

FROM: Gordon Bell

DEPT: 00D

EXT: 2236 LOC: ML12/A51

SUBJ: RANDOM MINICOMPUTER EVALUATION CRITERIAFrom: "Minicomputers: Low-cost Computer Power for Management"
by Donald P. Kenney

APPENDIX

BID EVALUATION SHEET

Date: _____ Prepared by: _____

Rating values: 10, excellent; 8, very good; 6, good; 4, average or nominal
value; 2, poor; 0, unacceptableA rating of zero for any asterisk factor is cause for rejection, regardless of
overall score.

<i>Factor Evaluated</i>	<i>Weight</i>	<i>×</i>	<i>Rating</i>	<i>=</i>	<i>Score</i>
<i>I. Vendor Organization (40%)</i>					
◦ Stability (years in business, project as a percent of business)	4	×		=	
◦ Financial rating	3	×		=	
◦ Experience with similar systems	7	×		=	
◦ Client satisfaction	4	×		=	
Maintenance and software support	5	×		=	
Timeliness of delivery	2	×		=	
Quality of proposal (revealed level of understanding)	4	×		=	
Level of staffing and manage- ment for project	3	×		=	
Project plan and organization	2	×		=	
Quality and cost control techniques	1	×		=	
Experience with proposal hardware/software	5	×		=	
Subtotal					

Factor Evaluated	Weight	×	Rating	=	Score
II. Proposed System (60%)					
A. General (25%)					
◦ Suitability for user's intended solution (such as specified volume, timing, inputs, outputs, storage, retrieval, routing, controls, recovery, interrupts)	8	×		=	
◦ Capability compared to cost	3	×		=	
Simplicity	1	×		=	
◦ Compatibility	2	×		=	
Scheduling (realism, mileposts, accountability)	1	×		=	
Ease of installation, cutover plan	2	×		=	
Consideration of alternatives/trade-offs	1	×		=	
Training	1	×		=	
Documentation	1	×		=	
Growth potential	2	×		=	
Test-acceptance plans	1	×		=	
Backup/recovery	2	×		=	
Subtotal					
B. Software (20%)					
◦ Suitability to problem (such as control, security, error handling, translation, file organization, formatting, sorting, updating)	7	×		=	
Modularity	2	×		=	
Use of previously developed hardware	4	×		=	
◦ Ease of revision and maintenance	4	×		=	
Versatility	2	×		=	
Report, printing, file, record-keeping capacity	1	×		=	
Subtotal					
C. Hardware (15%)					
◦ Suitability to project (such as terminals, computer, peripherals, capacity)	5	×		=	

Factor Evaluated	Weight	×	Rating	=	Score
◦ Performance compared to cost (storage capacity, speed, redundancy)	2	×		=	
◦ Reliability	2	×		=	
◦ Maintainability and manufacturer support	2	×		=	
◦ Number in use	1	×		=	
In-house experience	1	×		=	
Ease of changing configuration	2	×		=	
Subtotal					
Summation					
Subtotal I					
Subtotal II-A					
Subtotal II-B					
Subtotal II-C					
Total (maximum = 1,000)					

SUBJ: LOBBY EXHIBITS

DATE:
FROM:PAGE 1
02-17-75
GORDON BELL

* * * * *
 PLEASESEND TO: FILE
 * * * * *

SUBJ: EXHIBITS IN OUR FACILITIES (PRELUDE TO THE MUSEUM)

To: Roy Gould

I am intending to put together various exhibits on computer technology which might be put in various DEC buildings (for the time being, I would like to do one, and see what it looks like).

The exhibit would include the parts I currently have in my office, plus those which other people are sending me.

In order to make a really effective exhibit, I want to include Whirlwind! Would you please get me a list of the parts so that I can select some? or if possible, I would like:

1. One each of the registers: AR, AC, BR, IOR, PC to show the digit slice approach. We'll hang them together from the ceiling as they were in WW.
2. A plane and photo of core memory.
3. An electrostatic storage tube (if there were any).
4. Diode matrix for time pulse distributor (for changing control easily).
5. I/O--what can we have? a CRT, light pen/gun would be nice?, a flexometer.
6. A console register.
7. Part of marginal check/maintenance console.
8. Drum and/or tape.
9. Some interconnection cable.

SUBJ: LOBBY EXHIBITS

DATE:
FROM:PAGE 2
02-17-75
GORDON BELL

The emphasis will be to show WW as:

1. The first (early mini) 16 bits, in contrast to other long word machines.
2. The memory: core, disk, tape.
3. Unique I/O--CRT and camera (just now in use).
4. The flexo as an I/O device (used in late 2nd).
5. Marginal checking to increase reliability (used until 3rd gen.).
6. Bit slices (still used).
7. Design for reliability.
8. Forerunner of microprogramming.

WHEN:

GB: MJK

CC: Mimi Cummings, Mary Jane Keeney, Ken Olsen, Bob Reed,
John Trebendis

To: Dick Clayton and Henry Hemanie

cc: O²D, Products Committee

1182

I would like a 15 minute
Status report at Products
Committee regarding our
direction and ability to
be competitive in memories.
Our "luck" seems to be
bad there now, Gordon.

S
RE & SERVICES

**H-P Confirms
Price Cuts on
New 21MX Minis**

CUPERTINO, Calif. — Hewlett-Packard slashed prices 10 per cent or more on its new 21MX minicomputer line last week.

The cuts, as predicted (Data Topics, Feb. 10), came about a month after Digital Equipment cut PDP-11 series and some memory prices, but H-P's top minicomputer marketer denied his firm's action was a response in a developing price war.

"I always thought you determined a price war by a company cutting profits to get the price down," Edward McCracken, H-P Data Systems division marketing manager, said.

The reduction has not affected H-P's profit structure, he said, but was made possible by savings in the cost of 4K RAM semiconductor memory used in the 21MX line.

"We're simply passing on the savings that came directly from Texas Instruments," he said.

At the same time, however, other H-P marketers who asked to remain unidentified said they saw the H-P cuts as putting pressure on DEC and Data General to follow suit.

Mr. McCracken, for his part, claimed the 21MX reductions lower the price of minimum 8K configurations well below the prices of equivalent DEC and Data General configurations and give 16K, 32K and 64K versions a competitive price edge.

In OEM quantities of 50, H-P's systems, including memory parity, are as follows:

In 8K systems, prices dropped 10 per cent
Continued on Page 60

Why were we so unhelpful to pick wrong part?

**Prices Reduced
10% by H-P on
21MX Minis**

Continued from Page 50

cent to \$6,150 from \$6,800; in 16K systems prices dropped to \$7,650 from \$8,950, a 15 per cent dip; in 32K systems prices dropped 18 per cent to \$11,800 from \$14,000; and in 64K systems prices dropped 18 per cent to \$15,345 from \$18,777.

Mr. McCracken said the most significant factor in the price competition is in options beyond basic memory.

Without options such as memory parity, extended arithmetic unit and power recovery "We wouldn't look quite as good." However, he said most minicomputers offer little capability without the options.

Price savings in the H-P line range from \$2,000 to more than \$10,000, vis-a-vis the competition, Mr. McCracken said.

Both Mr. McCracken and Dick Anderson, division general manager, predicted further price cuts, based on the same reason: reductions in semiconductor prices that would enable the firm to pass the savings on to customers.

In fact, Mr. Anderson said the price of 4K RAMs should halve within a year.

bring mine of Dec. 1973.

P.S. Please bring your cost projection slides of the last year I'll

MIX OF BUSINESS

FY 75

FY 80

66%

NORAM

50%

25%

EUROPE

35%

9%

GIA

15%

1183

digital

February 17, 1975

Dr. Peter Weiner
Head, Computer Science Division
RAND Corporation
Santa Monica, California


Dear Peter:

I hope your visit, with Ivan Sutherland, proved worthwhile to ARPA.
I hope we can see any recommendations that are not proprietary--although
it is probably out of your hands.

Already we are starting to see better communications with ARPA; therefore,
it will be worthwhile from our standpoint.

We are hoping to have a museum at DEC someday. Since RAND is a part of
computer history, I would like to ask you for parts of some of the
machines used there; or in the case of JOHNIAC, I would like to get a
small part, photographs, etc. that could be part of a Von Neuman
machine exhibit.

Sincerely,


Gordon Bell
Vice President
Office of Development

GB:mjk

digital

February 17, 1975

Clifford E. Carter
 Assistant Director of Engineering
 Computing Services Office
 University of Illinois at Urbana-Champaign
 Urbana, Illinois 61801

Dear Dr. Carter:

I received the documents and photographs on ILLIAC and am really delighted. I want to use these to make an exhibit in the Maynard engineering building.

I think it is important to have all of the key dates in the history of ILLIAC, if you could supply those too--when the machine was first running instructions and when it was dismantled. I think I know how many copies were made of it, but it would be useful to check this.

I look forward to the second package.

Sincerely,

Gordon Bell

Gordon Bell
 Vice President, Office of Development

GB:mjk

Enclosure

— note, I have some questions about ILLIAC (S), Is it right? Dates? # of machines built?

S

*Send letter +
return to file*

February 5, 1975

Dr. Gordon Bell
Digital Equipment Corporation
146 Main Street
Maynard, Massachusetts 01754

FEB 06 1975
2-53

Dear Dr. Bell:

This is the first of two packages on Illiac I. In this one I have tried to give some picture information as well as supply a manual.

In the next one I will send a Williams-tube chassis and two of the original storage tubes.

Please let me know if there are other items you might want.

Sincerely,

Clifford E. Carter

Clifford E. Carter
Assistant Director
of Engineering

CEC:dkw

Dear Dr. Carter,

*I received the documents and photographs
on ILLIAC and am really delighted. I look forward to*

the second package. ~~and want to will~~

*I want to ~~start we will~~ use them to make an exhibit
in ~~the mill~~ our ~~mill~~ the Maynard engineering building.*

cc: JFB Minn, Gould.

1186



February 17, 1975

John Whitney
600 Erskine Drive
Pacific Palisades
California 90272

Dear Mr. Whitney:

Thank you for your letter of February 4, 1975.

I have turned your request for a computer system over to Bill McBride, the product manager of the Graphics group. Since I am not funding development outside of DEC and am not directly responsible for graphics development, I do not believe I can fund your project from our development budget.

I would like to be kept informed of any developments you have in regard to using computers for motion picture production.

Sincerely,

A handwritten signature in cursive script that reads "Gordon Bell".

Gordon Bell
Vice President
Office of Development

GB:mjk

cc: Bill McBride

Subject: HP Basic on 3000 ~~vs~~ RSTS/E as / HP Sales Document → + gB tests of same programs
 To: Clayton, Portner, Sarah Murphy, Mark Bramhall, Demma, Pete Conklin, Pete VanRochems, Delagi

Fm: gBell.

1187 Using K110 + 10 BASIC.

According to an H.P. internal document:

	t. sec.
RSTS/E (Virtual)	497
RSTS/E (Integer)	7
HP 3000 integer	.83 (.37 compiled)
HP Real	.97
HP double	1.13
KI10 Basic (Real)	.2

6x10000 IF statements in a Do.

Integer	RSTS/E	14.1
	HP	14.1 0.6
Real (only)	KI10 - Basic	.7

gB. Include .05 sec. Compile

gB test

10000 (+, -, *, /)

RSTS/E (Integer)	10.9
HP (Integer) (Compiled)	1.1
KI10 (Real)	.65

gB →

note KI10 Basic only has Reals (not integer + double).

SUBJ: SMALL SYSTEM'S STUDY GROUP

DATE:

PAGE 1

02-20-75

FROM:

GORDON BELL

* * * * *
 PLEASESEND TO: FILE
 * * * * *

SUBJ: THE SMALL SYSTEM'S STUDY GROUP AND AN ALTERNATIVE TO
 MOVE FASTER

To: Distribution

It is time we (DEC) get serious about the LSI-11 and start planning to use it NOW! I want direct participation from those who will be responsible for its ultimate market success: LDP, IPG, COMM, and some computation configuration (CLASSIC-11).

I was glad to see the study group in action. Although a lot has been accomplished in group intercommunication, I want corporate commitment from the users. There is a lot to do. It is clear you have won over Corell and Hughes and they are contributing ...the only ones?

The real problem I see is that the various other groups and product lines are not part of the thing, and you are doing the planning for them...which if you accept a theorem of DEC: he who plans, does; or a corollary: planning for someone else usually comes to naught.

I believe there are important applications areas for the LSI-11, and I believe you must get the implementers in those areas (only about 4) to meet weekly to discuss common problems, but each area goes off and starts to build products. We have historically been slow to adopt machines into the end user groups...let's not make the same mistake again. The common issues you have are:

1. Mechanical packaging. What do you have in common? Can you use the same modules? [I believe the testing problem (cost) says they have to be very similar...same box, etc.]
2. Options. What are their configurations? This would establish the priorities for what to LSI.
3. Common PMS structures. Can you all go to the computer

SUBJ: SMALL SYSTEM'S STUDY GROUP

DATE:

FROM:

module approach, which right now I want to go to, assuming it makes sense for the customers and you understand the pitfalls, problems, and how much it costs. Likely competitive announcements in the LSI are from Motorola, Fairchild, et al., namely, I see them all going to a few, very general LSI parts to do controls--in essence back to more conventional structures for control distributed out from the processor (off loading it), but still multi-computers. Motorola has a simple part in design for multiport memories and bus couplers like UNIBUS window. (In discussing this with them, they have a more deep understanding than we do about systems!)

I believe this has happened in every generation starting with Whirlwind. Namely, at the first of a generation, control is concentrated in a central place due to economies or technology costs somewhere else. As the technology becomes more familiar, control moves out to local controls; and finally, the local controls become quite complex processors (in fact computers), which are interconnected...and the process starts over again.

I see the same thing happening in LSI. Namely, the processor was first used exclusively for the control of a device through its program. As the technology improves, the integration takes place, and the machine is off loaded (and off loads the designer) by having a functionally separate part doing that control function. With the LSI-11 and its microcode, one has a more complex tradeoff. But I don't think it will be without a lot of pain, and with not a lot of payoff. Things may be different this time around though, as one functionally separates the I/O, it can and will be done in separate modules (computer modules) ala the Hughes proposal. If and when one wants to spend the extra money for the other computer, the programs, microprograms, vs the more integrated approach of a single system, one gets through LSI.

Right now I don't fully understand the future, but my belief is that it will be to still have separate modules, together with as much integration for local control as possible, simply to ease the programming problem (especially for high data rate transfer devices).

This functional separation should be quite ideal for many different environments to get away from a hairy operating system with multiprogramming.

SUBJ: SMALL SYSTEM'S STUDY GROUP

DATE:

FROM:

4. Programming. What will the support policy be? How do you do the networking?

If you take this approach, that is getting the various groups involved, so that they do the planning for their own areas:

0. Conventional boxed systems--who?

1. Communications--here I have a strong desire to use the computer module approach to do the communications stuff for all our COMM. I would like to put no options (aside from serial, high speed links) on any of our machines. I would have functional modules for each type of COMM problem--asynchronous, synchronous, and the multi-drop--and then have these modules interconnectable in the same way that Hughes proposed for the CLASSIC. A UNIBUS interface might exist (as opposed to HS serial) for directly coupling the COMM stuff to a conventional (e.g. 04-70/85) computer. As an aside, it might also be the way to do the interface to disks (e.g. floppy) if you happen to end up with that stuff in the CLASSIC configuration. I hope your group has read and digested the work by BBN on the HS-IMP using the Lockheed Sue--as their approach is somewhat similar. Note, COMM is exploring (has) a 360 front-end data management system that would be part of a totally functional computer approach. The BBN HS IMP is the archetype of such a system.
2. Industrial/LDP (real time)--again, here I am convinced the computer module thing is the right way to go. I have shunted 2 applications your way (Weid at U. of Chicago using several 8080's), and the American Electric Power problem which also has high data rates.

In the case of IPG, I believe that there will be 2 basic structures:

1. The loosely coupled things made of remote control, data logging, etc. and preprocessing. This will look the same way as we are going in networks, except that you would provide much more capability at an input-output point, and the local control will occur there, much the same way as in the human body.
2. In some of these problems, as a distributed point gets overloaded and needs more computation and/or coordination through more memory (global variables), a set of modules have to be combined to carry out the function. This in

SUBJ: SMALL SYSTEM'S STUDY GROUP

DATE:
FROM:PAGE 4
02-20-75
GORDON BELL

turn begins again to look much like the communications problem I call this--set parallelism,, which occurs when there is a set of problems to be solved all using the same (or relatively the same) algorithm, but involving some common global memory. I believe set parallelism with multiple interconnected computers would have evolved if the industry had evolved slower and the control problems harder to solve.

It is interesting to note that we build a significant number of machines in this structure in CSS. Here is where to find out about the applications, or in talking to the customers directly or better yet, having done applications personally,

3. The CLASSIC 11 structure (Corell, Stocky, Clarke, Teicher,?)-- I'm glad this one is being done deeply although we do have a product there now; and if you can use the computer module approach here, and have it be cost-effective, then it will work everywhere else. The cost constraint is the most severe. Again, the SACI system, UC/SD, Ken Bowles, will be good, demanding input.

However, again the real problem is who is going to do this. Are you (is it included within the \$30K called enclosure in your budget)? I see it unfunded! It would be interesting if Corell took this one. I believe there are people available with experience in the company that could be useful here and I would like to get them to help. Rick is very useful in the determination of the CLASSIC structure since he has understanding about the use, and packaging. Alternatively, Len Hallio has an approach to scan displays that looks quite interesting and might be helpful. It would be interesting to know if he has looked at the packaging problem.

Right now I believe that the current VT50 package should not be used to house the LSI-11 in the computer configurations because:

1. It is totally non-modular, hence has no way to grow or change with changes in the problem, or customer requirement (e.g. different line characteristics, different I/O, different program size).
2. It cannot be field upgradable (changable to whatever is the limit of what it eventually might be).
3. It requires a whole new set of customers who don't want to fix it themselves, understand it, open it, expand it, etc.

SUBJ: SMALL SYSTEM'S STUDY GROUP

DATE:
FROM:PAGE 5
02-20-75
GORDON BELL

which with the exception of a couple of our markets I don't believe exist.

4. There is no way to house floppy, and I don't want to try to push tape cassettes anymore in a burgeoning market that has a relatively nice media (e.g. DEC announced a thing called CLASSIC, for 3 separate markets predicated on floppy),... and is nice.
5. It isn't up to what at least one manufacturer has come up with that I think will be the standard--HP2640.

Is this the right approach? Don't we want commitments from Julius, Ed, and Brad, and (? on the CLASSIC) to help get going?

GB:mjk

Distribution

Ed corell
Andy Knowles
Ed Kramer
Julius Marcus
Steve Telcher
Brad Vachon
Dick Clayton



1193

February 18, 1975

Mr. David Rosenberg
31 Douglas Avenue
Maynard, Massachusetts 01754

Dear Dave:

I have received your memo of February 12, 1975 summarizing your present employment status and requesting action on my part. In order to make a judgement on your appeal, I have reviewed all of the documentation from you and your management relative to your performance. In addition, I have heavily weighed the findings and recommendations of Brian McDonald, who acted as a third party in reviewing your appeal.

I believe that you were handled fairly and that there was sufficient verbal and written warning as to your performance. I further believe that, under the circumstances, you were given a reasonable choice between payment of accrued benefits and severance pay or payment of accrued benefits and a three month contract.

In summary, I support the action taken and will not take any further action on your appeal.

Sincerely,

A handwritten signature in cursive script that reads "Gordon Bell".

C. Gordon Bell
Vice President,
Engineering

clg

digital

INTEROFFICE MEMORANDUM

TO: Clay Neal
Larry Portner

DATE: February 21, 1975

CC: Julius Marcus

FROM: Gordon Bell

DEPT: 00D

EXT: 2236 LOC: ML12/A51

SUBJ:

When are we getting dual port support on RP04 under RSX11D?

GB:mjk

digital

INTEROFFICE MEMORANDUM

TO: Mark Abbett
Larry Bornstein

DATE: February 24, 1975

CC: 00D

FROM: Gordon Bell

DEPT: 00D

EXT: 2236 LOC: ML12/A51

SUBJ: STOCK PLAN

We would like you to work out a stock plan whereby stock for our engineers is allocated at the time of project completion. This might be done on an allocated or reserved, which we hold in escrow until the proper time.

GB:mjk

SUBJ: HEWLETT PACKARD

PAGE 1
02-25-75
FROM: GORDON BELL

* * * * *
 PLEASESEND TO: FILE
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SUBJ: HP

To: Ed Kramer

As being responsible for competitive analysis of HP, I'm counting on you to start. We have no real information, visibility about HP through the organization.

My concern for HP is through direct connections: customers, manuals, advertising. Already they are taking much market share, through 21MX, and in reading their internal sales document on selling against RSTS, it's clear that we are in much trouble with IAS, RSX11's, and RSTS. On computational benchmarks using BASIC, they out perform us by a factor of 10-20--in essence, a compiler versus an interpreter. Meanwhile, the pressure on RSTS is for more features, too. We have let a product get obsolete, with no real alternative strategy.

In order that I can get a better appraisal of the situation, would you please send me several copies of the 3000 documentation for understanding, and analysis. I will make sure they get in the responsible hands so that we can move. Also, I would like several of us to visit and operate an HP3000. Could you find a suitable site?

It is also possible the PDP-10 is in some competitive problem, too with the 3000 system, as it performs about the same as a KI, with more features, and 1/2 the cost. This is my gut level feeling having run the benchmarks!

Dick and Larry, we are responsible for producing state-of-the-art products; and I view we have a problem here which must take priority over being hassled.

GB:m.jk

cc: Marketing Committee, Dick Clayton, Irwin Jacobs, John Leng
 Larry Portner, Charlie Spector, Jerry Todd
 Dick Angel, Win Hindle, John Levy, Larry Wade

SUBJ: OOD STAFF MINUTES

DATE:
FROM:PAGE 1
02-25-75
GORDON BELL

* * * * *
 PLEASESEND TO: FILE
 * * * * *

SUBJ: OOD STAFF MEETING MINUTES--Feb. 20, 1975

To: OOD

1. Production Communication

- A. Cudmore, Smith and Clayton will come back with a proposal as to the responsibility for design, fabrication and testing at the systems level.
- B. We have a 1-loop control system for manufacturing the LA36.
- C. Sample the output of the engineering process (Gordon might do this). We do not design worst case. What is the level of our designers? Can we track designs by ECO's? (This might inhibit badly needed ECO's.) Are we doing enough in design aids? (Dick Best, can you propose something here?)
- D. Low end products--we need pressure to meet volume/producibility requirements.

2. Gordon would like the strategy written down by the individual VP's within next 2 weeks. Gordon will write an overview of the plan. This should really be cleaned up before the Woods meeting. While we have a start at it, state-of-the-art and competitive information is lacking.

3. We discussed the process to arrive at a decision. The problems:

- A. Every group is working the problem--OC, MC, Ken + MC + several PLM, PLMC?, PC, OOD, PSG, John Fisher, etc.
- B. There is the possibility of noise in the formal organization because:
 - many links
 - many filters

SUBJ: OOD STAFF MINUTES

PAGE 2
DATE: 02-25-75
FROM: GORDON BELL

- see attachment

C. There are some unclear goals--e.g. do we spend in relationship to where we earn it, or where we'd like to earn it?--corporate problem.

GB:m.jk

Attachment

CC: Dick Best, Jim Cudmore, Henry Lemaire, Jack Smith



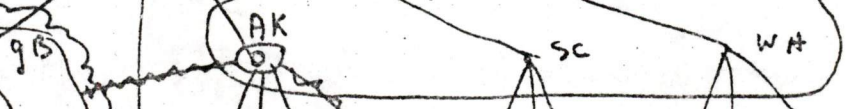
Gordon perceives problem set.

PL.

MC.

P

OOD



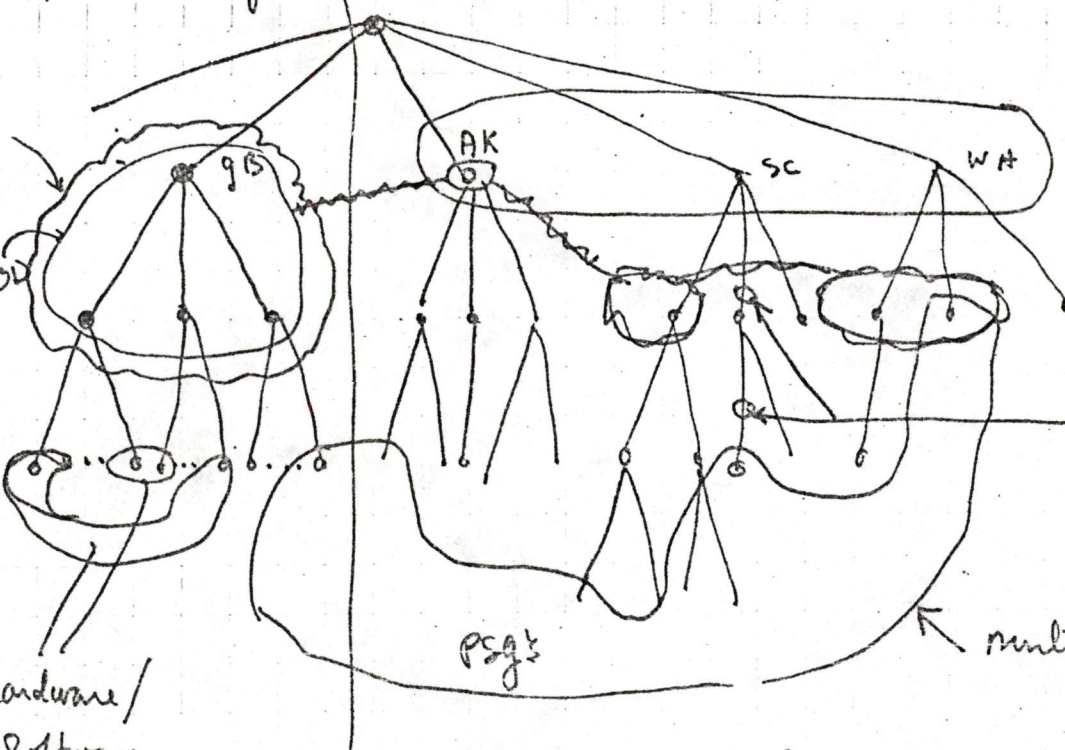
PLM.

poor-comm.

hardware/
software
tradeoffs.

psg

multi-level psg.



SUBJ: ANALYSIS OF MAKE/BUY

DATE: PAGE 1
FROM: 02-25-75
GORDON BELL

* * * * *
PLEASESEND TO: FILE
* * * * *

SUBJ: ANALYSIS OF MAKE/BUY

TO: PHIL LAUT

CC: OOD, MC, John Fisher, Pete Kaufmann

I'm really puzzled as to how to deeply analyze and decide how we allocate engineering in several of the peripheral areas. If we pushed the algorithm of spending versus where we either earn or intend to earn NOR, it would increase:

- 1. Memory
- 2. Tape
- 3. Floppy
- 4. Other peripherals (paper tape)
- 5. LA's
- 6. PDP-8

and reduce:

- 1. CPU's
- 2. Software
- 3. Alphanumeric terminals

It is also hard to allocate between manufacturing cost reduction and new products. In some of the make/buy decisions, it is almost as expensive to buy a unit (i.e. bring it into WM) as to make it from an engineering standpoint (e.g. WF).

As we move to get all projects into product measurement system, better investment guidelines and styles of analysis should emerge.

Since new designs (e.g. memory) bring lower costs, and we pass the savings along to the customers, ROI and PC analysis are really difficult since it has to come from increased sales. I believe these styles will look like:

SUBJ: ANALYSIS OF MAKE/BUY

DATE:
FROM:

PAGE 2
02-25-75
GORDON BELL

1. Lower costs (the memory case)
2. New, incremental business, like VT and LA
3. Systems
4. Software which generates incremental business
5. P/L engineering which generates incremental business
6. Cost reduction in manufacturing and make/buy cases.

Allocation algorithms are at best guidelines, and I really believe we have a problem of analysis, understanding, and proposing the direction.

Meanwhile, we have to get our engineering and product managers, who believe that their own investments are better than other product investments, to be patient.

GB:mjk

SUBJ: REPACKAGING

DATE:
FROM:PAGE 1
02-25-75
GORDON BELL

* * * * *
 PLEASESEND TO: FILE
 * * * * *

SUBJ: 11/04,05,LSI-11, etc. REPACKAGING

To: Distribution

For those of you who missed a talk I gave a year or so ago on packaging, I don't want any systems or computers we sell to be drawer mounted or to have cables coming from modules (with no strain relief). The drawer clearly stands out as the worst packaging schemes (e.g. fixed, page, drawer) by all criteria except local density (inversely proportional to reliability).

I am thoroughly disgusted with the fact that Vince is having to spend his effort to put the PDP-11 products (e.g. 11/04) in a decent box. (He is using a variant of the 8/A box for the communications market.) There are a reasonable number of cables; and cooling, reliability, and low cost are the criteria.

Ironically, COMM also took an order for one of our other computers from an enlightened customer, who demands round cables when going between bays instead of internal-type cable in the UNIBUS.

Going this way provides more of a market separation by letting each P/L pick their own box design. The OEM could be differentiated by being crammed together, expensive, and high power density. I assume each OEM wants to make their money with lots of service calls. For the systems we have to service either on a warranty or contract basis, we should probably pick the boxes that Vince is going to use.

It is clear that the new LSI-11 is using the 2 box strategy. Can we get either industrial or COMM to take the design responsibility for the LSI-11 used in systems? I am prepared to work to fund things this way, and I suggest we use the box for systems we sell.

I want each of us to give Vince full support in this endeavor, and I would hope that other product lines could also be able

1203

SUBJ: REPACKAGING

DATE:
FROM:

PAGE 2
02-25-75
GORDON BELL

to use the box in order to get a reasonable housing. I want
the systems we are responsible for (e.g. RT-11, RSX-11/S/M)
to use it!

GB:mjk

To: Steve Teicher
Mike Tomasic
Dick Gonzales

Dave Nevala

Larry Nye

cc: Bob Armstrong, Vince Bastiani, Roger Cady, John Clarke
Dick Clayton, Bill Long, Bob Puffer, Bob
Savell, Jack Shields, Ken Olsen

INTEROFFICE MEMORANDUM

digital

TO: Ed Corell
CC: Phil Laut
Andy Knowles
Bob Puffer
Bill Steul

LOC/MAIL STOP
ML1/E62
ML12/A16
MR2/A52
ML1/E38
MR2/F21

DATE: February 25, 1975
FROM: Gordon Bell
DEPT: OOD
EXT: 2236
LOC/MAIL STOP: ML12-1

GB

SUBJ: FY75 Printer Budget

You are authorized to overrun your budget by up to \$350K, to do the following projects in FY75:

- 1) LA36RO
- 2) LA36 Communication options and forms control
- 3) Basic LA180

Please provide a coordinated Manufacturing/Engineering delivery schedule within 30 days to the Product Lines for planning purposes.

/ale

SUBJ: LEARNING--FACTOR IN SALARY

DATE:
FROM:PAGE 1
02-26-75
GORDON BELL

* * * * *
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SUBJ: CONTINUING LEARNING--A FACTOR IN SALARY, AND OUR OWN PLANNING

To: Engineering Managers
 Consulting Engineers
 Mark Abbett
 Dennis Burke

CC: Ken Olsen

In general, I get 3 kinds of news about products (other than the financial results):

1. Things are really going well--this occurs when the project is on time, and performing well above the goals you have set for the project (good news travels to me fast).
2. The bad news (which moves to me very slowly), is of 3 types:
 - A. An internal product is screwed up and is affecting other products.
 - B. A product can't be produced and the noise is that it's production's fault (they can't track the ECO's fast enough).
 - C. The product is out in the field and our customers react to it.
3. A product is really no good because it is not up to the market's expectation in terms of cost/performance--most often the performance (capability) is the problem.

In being fortunate to have a slower growth rate than last year, and by having a wider range of experience because of the diversity of products we produce, and because more is known about the products from an academic/intellectual sense, we should make fewer mistakes. However, a slower growth rate inhibits new employee entries who have better backgrounds.

SUBJ: LEARNING--FACTOR IN SALARY

DATE:
FROM:PAGE 2
02-26-75
GORDON BELL

Many of the mistakes I came in contact with last week (e.g. the race in the logic that hangs the specific terminal that I am now typing at; the really bad method used to allocate storage in an operating system that makes it come crashing to a stop under reasonable load; the lack of understanding which permits our products to be oversold even though by any rational expectations (i.e. a salesman's or customer's) the product should do the task even if it isn't explicitly spelled out; the PC board that might catch fire under various failure conditions; and the product we can produce in high volume that people are skeptical of being able to sell) are impossible by any rational expectation of engineers.

At this time when we are doing our salary planning, and you are feeding back to each of your people, please take the opportunity to think about our futures in a highly technical, rapidly evolving field. Professionals out of school more than 5 (and definitely 10) years are at a definite disadvantage of recent employees--especially those who don't have advanced degrees, or do not read beyond the superficial material of trade magazines. How many of your employees are members of IEEE, the ACM, and read their publications?

Much of the understanding about our technology has occurred in the last 5 years. However, many of the disasters which I am aware of could have been avoided by having the knowledge (e.g. an algorithm) that is at least 10 years old. In the case of a very few software engineers, knowledge of how to design recent algorithms may not be necessary because they have good fundamental knowledge to rederive the algorithms from first principles--but this number of people is not over 10. For the rest of us who are not so bright, we must look elsewhere for other techniques.

As production begins to understand their own processes for producing products, it is clear that the largest gains can be made by controlling the quality of the process that produces the product (e.g. design engineers).

We have many excellent on-premise university programs. These are meant to be taken by you, me, and our fellow engineers. (If you really want to learn some of the material deeply, then let me urge you to get involved in teaching one of the courses.) There are other ways to learn, of course, and I'm happy to hear of the ways you're using. This might include learning a new language, an algorithm or being able to solve certain classes of problems. As I sift through the plethora

1207

SUBJ: LEARNING--FACTOR IN SALARY

DATE:
FROM:

PAGE 3
02-26-75
GORDON BELL

of incoming resumes, the clear tragedies are those who stopped learning; and there are lots looking for management, marketing, and planning positions. There is really no escape with technology when one is in this industry.

I would be happy to get feedback on the extent you agree with me, on this point.
on this point. However, I do want to understand your plans in this area of learning your living.

GB:mjk

digital INTEROFFICE MEMORANDUM

TO: Distribution

DATE: February 24, 1975

FROM: Gordon Bell

DEPT: 00D

EXT: 2236 LOC: ML12/A51

SUBJ: FE PLAN

I'm impressed that you have the skeleton of a COMM plan based on the COMM Front Ends.

The future might permit a more modular system based on LSI-11, but there is work to really test out such a scheme.

Are you benchmarking (competitively analyze) these schemes in terms of cost/line at the FE and systems level?

How well do they turn out? The store and forward system ala ARPA also needs to be considered I believe.

An early review with OOD, Demmer, Van Roekens, Conklin, Pearson, etc., might be worthwhile.

GB:mjk

Distribution

Vince Bastiani
Tony Lauck
Nat Teichholtz

cc: OOD
Don Alusic
Julius Marcus
Pete Van Roekens

digital

INTEROFFICE MEMORANDUM

TO: Ed Kramer

DATE: February 24, 1975

CC: Al Michels

FROM: Gordon Bell

DEPT: 00D

EXT: 2236 LOC: ML12/A51

SUBJ: DR. WIED

I called him and said:

1. LDP is his official interface; I'm just the developer.
2. Al Michels is a supplier for awhile, hence, Ed gets modules through him.
3. Ed would contact him in regard to his request.

I hope something can be worked out since he has an interesting application.

GB:mjk

digital


February 26, 1975

Gerald J. Burnett
Director
Information Systems Division
Teknekron, Inc.
2118 Milvia Street
Berkeley, California 94704

Dear Gerry:

Anything we can do to help, please let me know. Sorry we
couldn't get you here now.

Regards,



Gordon Bell
Vice President
Office of Development

GB:mjk

cc. Bill Jorg

Teknekron, Inc.

2118 MILVIA STREET
BERKELEY, CALIFORNIA 94704 • (415) 848-1464

February 21, 1975

FEB 25 1975
2-31

Mr. C. Gordon Bell
Digital Equipment Corp.
146 Main Street
Maynard, Mass. 01754

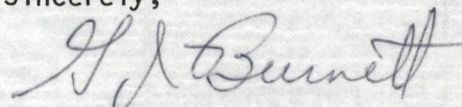
Dear Mr. Bell:

I would like to thank you for giving me the opportunity to interview with Digital Equipment Corporation. I believe our joint conclusion was that my interests and your needs did not match at this point in time. However, I enjoyed our visit and would look forward to meeting with you again in the future.

I have accepted a position in Berkeley, California at Teknekron as Director of a group delivering software and professional services. Teknekron is an OEM of Data General; however, I would expect that I will get them also involved with DEC equipment.

Thanks again for your time.

Sincerely,



Gerald J. Burnett, Ph.D.
Director, Information Systems Division

GJB/t1

*Dear Jerry
Any fly we can do
to help! please let
me know. Sorry
we couldn't get you
here now.
Regards*

*Gordon
Bill Long
Ted Johnson
Jerry Moore*



A Consortium of University Scientists and Engineers
WASHINGTON, D.C.
BERKELEY, CALIFORNIA



INTEROFFICE MEMORANDUM

TO: John Trebendis

DATE: March 3, 1975

FROM: Gordon Bell

1212

DEPT: 00D

EXT: 2236 LOC: ML12/A51

SUBJ: EXHIBIT PARTS

Could you get me a computer lab?

Can you get modules for an exhibit?

1. The lab units (1969)--extrusions.
2. Systems modules--various types
1200, 4000, 6000 series
3. Long systems modules (Teletype transmitter + receivers)
4. PDP-6 Systems modules.
5. Flip chip (R-series, B-series)
single/double/quad
6. Large modules (single/double/quad/hex)
7. Teletype modules for flip/chip series

GB:mjk

SUBJ: OPERATING SYSTEMS

DATE:
FROM:

PAGE 1
03-04-75
GORDON BELL

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PLEASESEND TO: FILE
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SUBJ: OPERATING SYSTEMS

TO: LARRY PORTNER

CC: OOD

I believe we've really a disaster in the works vis a vis the mushiness of existing operating systems (and computers?).

At the high end GPTSS (which already seems too late):

- 1. RSTS (or TOPS 11)
- 2. IAS
- 3. RSX with swapping and scheduling (In progress)
- 4. RT with multi programming.
- 5. 11/85

At the low end:

- 1. RSX-11/M
- 2. RSX-11/S
- 3. RT-11

With the price of 5K of memory moving to be about \$100 (also the price of a cheap service call), I have trouble understanding the low end, low core request for 2 operating systems which have identical functional capability. (Say we sell 10,000--that's only 1 million savings to handle manuals, training, support, standards, etc. etc.)

The next disaster in process could quite easily be using the PDQ WCS to enhance FORTRAN on RT11 to get a bigger memory in lieu of using a larger address space which we have to define.

I believe the two PM's involved here have to come at this from a business viewpoint. The development costs and incremental memory costs are the trivial costs, the rest will kill us.

SUBJ: OPERATING SYSTEMS

DATE:
FROM:PAGE 2
03-04-75
GORDON BELL

Let's discuss this at staff meeting so that the review of these quite black and white hot issues can be looked at.

Unlike the CPU strategy that requires explicit tool up dollars in production and we kill; operating systems get us in subtle ways. Have we ever not released software that was done?? (Remember the work we have on DOS, and how we're unable to sell new hardware to these users unless we continue massive support?) We really can NEVER drop an operating system once it gets in the field.

Larry, please position the primate on your posterior.

GB:mjk

SUBJ: STATE OF ENGINEERING

DATE:

FROM:

PAGE 1

03-04-75

GORDON BELL

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PLEASESEND TO: FILE
* * * * *

SUBJ: STATE OF DEC ENGINEERING AND TO REST OF COMPANY
AT KEN'S WOODS MEETING

To: OOD, Julius Marcus (COMM + Alpha Terminals), Henry Lemaire

CC: Ken Olsen

For the last 2 years I have asked for reports from each of the engineering groups on the state of the products and the long range plans. This was a prelude to a presentation at a 1-day Operations Committee Woods meeting,

At the PM/EM workshop last week, one request was to get an overview of the various product areas. The meeting by Dick and Larry seemed to be extremely well received, was quite fast moving, and served the need to some degree except that it was billed as an internal output-only meeting.

I would like to again have the yearly 1-day meeting whereby everyone presents their plan. This year the product manager could present the business plan. It would be attended by the product lines, who would also present their plans in the same context. After the MC/OOD Woods meeting, the plan should be more firm than at any other time, and we could give everyone a view of the plan when it is most solid.

To a certain degree, it is too late to present this widely since the April OOD/MC woods meeting will be the final decision point. Ken has asked that the format be that we present and the MC approve. I have asked each of you to prepare a short strategy position paper to be used at that meeting.

GB:m.lk

TO: Dick Clayton
Larry Portner

DATE: March 4, 1975

CC: Ken Olsen

FROM: Gordon Bell

DEPT: Central Engineering

EXT: 2236LOC: ML 12-1

SUBJ: MARKETING COMMITTEE PRESENTATION - MARCH 10th

Ken has asked us (Dick and me) to present the competition at the next Marketing Committee, regarding the 32/36-bit question. I believe you two should present the competition picture simply, although for this pass (by Friday) I'd like details!

Let's take this opportunity to get things into a competitive perspective. I'm certain we have all the data in charts already, so all that's needed is to reproduce it in those cases.

The parts of it:

1. Hardware (Dick organize)
2. Operating Systems (Angel and Clay Neal)
3. Languages (Al Brown)
4. Nets (Nat)

Each part should be about one page (although I'd like more details).

The competitors:

1. Interdata 7/32, 8/32
2. Varian
3. Eclipse, Eclipse VAX
4. HP 2IMX, 3000
5. Modcomp IV, new
6. SEL 32-bit
7. PDQ, 11/70
8. 11/85, 11/85(32), integrated-low-cost 10, 11/LSI(32)

Hardware Attributes:

t. ship
\$P (with some standard configuration memory - say 16 Kwt?)
\$M (16Kw)
direct address size

- continued

Dick Clayton, Larry Portner

March 4, 1975

Hardware Attributes (continued)

Physical mem size
 No. sets of registers, # registers, width
 t. context - switch
 t. interrupt - response

Data - types
 Speed (add, add float, mult, multi float) plus
 some standard benchmark, e.g. Whetstones/Sec or
 Gibson mix

PMS-structure (rough with bandwidths identified)
 Mem - I/O bandwidth available
 Multiprocessor capability
 Hardware RAS
 Rough IC count + logic type

Language Attributes:

For { ALGOL, APL, BASIC (level), COBOL, RPG, System Prog. Language }
 do:

0. Year of introduction
1. Computer, interpreter
2. Working set size of translator(+ size with overlays)
3. Compile (translation) speed
4. Execution (interpretation speed) only for Fortran
5. Object code representation (+ size measure)
6. Debugging capability
7. Object level optimization

Operating System Attributes:

1. Year of introduction
2. File types and data structures
3. Structure
4. t. response
5. size
6. languages supported

Net Capability & Comm Attributes:

Nat has to outline these and include our major competitors: Interdata, HP, Modcomp (e.g. line speed, file capability, support, number virtual channels, flow-through).

SUBJ: ARPA

DATE:
FROM:

PAGE 1
03-04-75
GORDON BELL

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PLEASESEND TO: FILE
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SUBJ: ARPA

TO: Bruce Delaai, Dick Clayton

CC: Bill Strecker, John Levy, Alan Kotok

I got a call from Craig Fields today regarding other options he wants for ARPA to insure their success of the small 10 proposal.

If we only deliver 1 of the prototypes and are not intending to go into production, he would like to either/or or both:

1. Get their money back in the form of credit for 11's.
2. Be able to buy the computer at between 10 and 100 at a fixed amount (say the \$50K).

Bill Strecker has an alternative proposal which would use standard parts (e.g. KL10 or other memory, a CLASSIC, RK05's, or just floppy) and be really low cost, with this only 3 or 4 boards would be built, and CSS might build it.

The more I look at the qotss systems on the 11 and the plummeting memory costs, the more attractive a low performance 10 looks (i.e. it looks a lot like a 192K HP21MX, but with great software). Somehow I would really like to breadboard a really low cost 10 to get a feel for feasibility/utility.

GB:mjk

digital

INTEROFFICE MEMORANDUM

TO: 00D
Henry Lemaire
Julius Marcus

DATE: March 6, 1975

FROM: Gordon Bell

DEPT: 00D

EXT: 2236 LOC: ML12/A51

SUBJ: KEY BUDGET RESULTS AS/4PM, March 4

The key recommendations:

1. No sales meetings this summer.
2. No college recruiting--unless we come back with a way to make plan.
3. Expenses flat: Q3, Q4, Q1FY76.
4. FY76 will be delayed by 1 quarter, yielding NOR of 675.
5. Resulting Engineering budget: $675 @ 4.6\% = 31.1$ or a cut of $32.5 - 31.1 = 1.4$.

Please cut each area back by $1.4/32.5 = 4.3\%$

GB:mjk

SUBJ: OEM SALEABLE SOFTWARE

DATE:
FROM:

PAGE 1
03-11-75
GORDON BELL

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*PLEASE**SEND TO: FILE
* * * * *

To: Bill Long

CC: MC, OOD, Win Hindle, Irwin Jacobs, Brad Vachon

I've run across quite a lot of high quality software which, for various reasons our customers have written on our machines and they would like the software marketed, either as an add-on or as an integrated hardware/software product. (The later case is the more common.) These include: languages, specialized text handling, data-base, etc.

Much of this requires an OEM in order to get max impact of highly trained sales/application people found in OEM's (and lacking in much of our marketing/sales groups).

The power demand monitor is clearly a case in point--where in this case we've developed a hopefully nifty package, but it's doubtful if we can afford to sell and apply it. IBM charges 2 times as much for the same thing (1/2 their price is for field applications no doubt). The OEM (e.g. Stone and Webster) is the way to go so that the most knowledgeable people do the applying, and then since another organization is making money, we have a real chance of competing with IBM rather than being inevitably forced out of the business within DEC because the price was too low and the product was unprofitable.

There are other situations like this with external development. By having higher level tools, it would seem like you have unique products rather than the iron you sell; hence, more buffering against the economy.

What do you think? Can I steer a few external products of this type to you for evaluation?

G:mik

SUBJ: PRESENTATION TIMETABLE

DATE:
FROM:PAGE 1
03-06-75
GORDON BELL

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SUBJ: TIMETABLE FOR PRESENTATION AND APPROVAL OF THE DEVELOPMENT STRATEGY (AND BUDGET)

To: Distribution

March 6 Payoff tables and graphs for all major products
(Bell and Laut)

March 11 MC Presentation of competition for Large minis
(Dick Clayton)
Terminal strategy to MC (Laut/Marcus)

March 10 to 12 Presentation of 32/36 bit strategy to PL
Managers (Bruce Delagi Chairman)

March 17 Written draft of complete strategy to OOD for
review. More comments on plan by MC.

March 18 or 19 Dinner meeting with OOD and interested PL
Managers to discuss draft (Bill Thompson to
schedule)

March 21 "The Plan" (written) sent to P/L's and group VP's.
(Informal discussion of plan between OOD, PLM,
key PL people on 1:1 basis.
(Bill Thompson to schedule)

March 31 - April 1 Presentation of plan to MC by OOD.
(Fisher/Thompson/Olsen schedule logistics
and housing)

GB:mjk

Distribution

OOD
 Henry Lemaire (memory)
 Julius Marcus (COMM + Alpha Terminals)

cc: Marketing Committee, PL Managers, Ken Olsen, Bill Thompson



March 13, 1975

J. W. Graham, Director
Computer Systems Group
University of Waterloo
Waterloo, Ontario, Canada
N2L 3G1

Dear Wes:

I am very sorry to take so long in responding to your request for a statement of our intentions to extend our agreement. I was very impressed with your implementation of the WATFOR-11 compiler in such a timely fashion. I am most pleased with the close working relationship that has developed between WATFAC and Digital Equipment Corporation. Accordingly I am pleased to inform you that it is the intention of Digital to extend our agreement with WATFAC for a period of at least one year, upon expiration of the current agreement. It is also our intention to give you the option of on-call maintenance for the PDP-11/45 during this extended one year period.

Al Brown is working with Bob Trocchi of the Educational Products Group in getting the details of the marketing relationship between WATFAC and Digital across to our sales force in the form of sales brochures and product announcements. Al Brown has informed me that you are scheduled to give a presentation on WATFOR-11 at our spring DECUS. I am scheduled to give the keynote speech at DECUS, so I hope that I see you then.

I look forward to a mutually beneficial relationship between WATFAC and Digital in the future. I trust that any delay in my giving you written assurances of our intention to extend the agreement has not hampered your plans in any way.

Your products should contribute greatly to extending the capability of the PDP-11. Again, congratulations on a fine effort; see you at spring DECUS.

Sincerely yours,

A handwritten signature in cursive script that reads "Gordon Bell".

Gordon Bell
Vice President
Office of Development

GB:mjk

cc: Al Brown, Bob Trocchi

DIGITAL EQUIPMENT CORPORATION, 146 MAIN STREET, MAYNARD, MASSACHUSETTS 01754
(617)897-5111 TWX: 710-347-0212 TELEX: 94-8457

SUBJ: PROJECTED MEMORY PRICES

DATE:
FROM:PAGE 1
03-24-75
GORDON BELL* * * * *
PLEASESEND TO: FILE
* * * * *CONFIDENTIAL
-----SUBJ: ATTACHED PROJECTED PRICES OF MAIN MEMORIES AS A MEANS
OF MODELLING SYSTEM PRICES IN 1975-1980.

In wondering about how the virtual memory system would look in the next few years, I started to understand (build a model) what the system prices would look like if things went along as they are heading for now. This discussion:

1. Looks at memory cost in an extremely conservative way based on historical and various market projections (fig. 1) giving a price decline of 26%/year. Each 10 years, the price declines by X10. In 1972 the cost was \$.005/bit. (Cost/bit=\$.005/1.26^{t-1962}),
2. Assumes a memory price based on 3X markup
Price/bit= \$.015/1.26^{t-1962} (This checks with Telex papers rumored IBM rental of 1 Megabyte for \$1K/month in 1976.)
3. Defines our systems in terms of memory sizes.
4. Plots memory system prices for various memory sizes which we now use, and also the total system prices assuming memory is .2X the system.
5. Draws conclusions.

Exponential projections into the future scare me; this one is no exception, but is necessary. This is perhaps the most interesting projection I've made. Even though it's implications are frightening, I believe it is conservative, at least if you limit the systems to be effective out until only 1980 (only 4.5 years away). Thus what we are planning for now are at their middle to end-of-life.

SUBJ: PROJECTED MEMORY PRICES

DATE:
FROM:PAGE 2
03-24-75
GORDON BELLMEMORY COSTS

I am absolutely certain that the memory costs will meet the objective of 25.8% yearly price decline. The reasons that the decline will continue:

1. Core did and MOS is just moving in and is following at least as aggressive curve (probably more).
2. We held up the prices of memory by having a captive core facility. The minute MOS comes in at a lower price it will take away our umbrella, and our competitors who do not use our markups (i.e. have no core facility) will continue to follow their own pricing; and we will be forced to follow (in essence go to more unbundling and to higher priced CPU's). I pointed this out in the Dec. 1973 memory plan to you all; BCG has recently confirmed this; and HP is doing it!
3. This will make memory less of a dominant contributor of profit. Markup will go from 4 or 5 to 3. The percentage of the system in memory may also go down (.3 to .2).
4. CPU speeds have been increasing, and with it the need for more memory to run out of. Fred Brooks quotes 1 byte of memory/instruction/sec in the IBM world. In our real time systems, there is more processing. Hence, the memory sizes are smaller per fast CPU. Probably the poorest balanced system announced so far is the DG Eclipse which can probably execute 1 million instructions/sec and would require 1 million bytes of memory by this measure. This raises the volume.
5. We know enough about hierarchies, and with CCD and bubble memories, the main memory can be balanced to be both fast and to achieve a lower cost target beneath pure MOS.
6. All projections are at least this aggressive.
7. The technology under-pinnings of density, price, yield, history support it. Thus,
Cost/bit = \$.005/1.26^t (t=1972)

Memory Price

The X3 markup looks like a limit, considering new competitors in silicon valley and by HP. This checks with IBM-Telex papers.

Price/bit = \$.015/1.26^t (t=1972)

SUBJ: PROJECTED MEMORY PRICES

DATE:
FROM:PAGE 3
03-24-75
GORDON BELL

Note, ours was actually higher in 1972 due to umbrella and capacity. But we will have to get into line in 1972. Now HP sells 8K for about \$800 (on the curve),

A definition of system functionality by memory size

I've had a hard time with the notion of system functionality, but it is now a bit clearer to me (had hopefully even on the right track). It is:

Memory size, to a first approximation, determines the functionality (use) of system. Through memory size, one can easily classify a machine structure and functionality (i.e. its use).

I believe the ranges of functionality are not orthogonal at all with price as we have been working with, but almost totally correlated with price!

In essence there are just 2 uses!

1. Interactive--connected to people (e.g. POS, teller terminals, text manipulation, programming).
2. Real time--connected to a mechanical process.
3. Hybrid--in a few instances both, e.g. IAS

There are 4 types of machine structure denoted by memory size, that define a system's use. Two attributes: dedicatedness versus programmable and 1 program versus multiprogramming give the 2X2 combination of structure. These are shown in Table 1.

The whole notion of batch is just an interactive use which has no time limit on completion. Iron is simply a classification as to don't know, don't care, and may end up in a dedicated application.

Memory System Price and Total System Price

Figure 2 now uses the categories of system, by memory size and plots both memory system (only) price (left scale) and the imputed total system price (right scale) for each size system. Historically, primary memory (core) has been 25% to 30% of DEC's business. In this model, I assume it is 20%, thus our historically high markups will balance lower future markups. Note, we

SUBJ: PROJECTED MEMORY PRICES

DATE:
FROM:PAGE 4
03-24-75
GORDON BELL

can cross check some points: A dedicated 4K machine sold for less than 20K in 1966--PDP-8; in 1964 a LINC, 1 user sold for about \$50K; in 1968 a 65K-to-128K PDP-10 sold for between 350 and 600K; currently a 1 user CLASSIC might sell for about 4.5K, if packaged in an integrated way, (here, the disk prices are the anomaly.)

Here the model which has been valid in the past, may be in some trouble. Namely, memory cost has fallen enough to not determine the system's price, but rather there are proportionally more limits by the disks display, but most drastically by the packaging and power costs which haven't fallen. If one integrated all this into a VT8/E-type design, where memory was shared with processor, and disks were more tightly integrated, the cost of \$1.5K might have been achieved. Note, that the MCM APL terminal is just this.

Implications

----- 1. The high end.

The operating system price (size) in 1977 will be a small number (overhead price of about \$25K). The 10 will be drawn into the mini-price arena due to memory price declines. Note, Interdata's 1 megabyte for \$170K is precisely a 256K word 10. The 10 will invariably be benchmarked (e.g. the Eclipse), and for now the only separation will be lack of monitors by Interdata, Modcomp, et al. Clearly these competitor companies won't have the resources to do the software now, but will evolve into just like us (IAS, RSTS/V7, RT11F/B).

The 10 and high end 11 will be separated for awhile by the general purpose versus special purpose and by lack of software for higher priced systems where the customers begin to measure performance at the language level and worry about the user interface.

The 10 might come down in price through the high end mini competitors (already the 2010 is at 250K).

The low end 10 which uses 32K-65K words could be available for \$25K or \$50K in CY 1977. Here the emphasis would be not on a new monitor, but the restricted use to a single language or single problem to gain efficiency, and minimize program cost.

2. Mid

SUBJ: PROJECTED MEMORY PRICES

DATE:
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GORDON BELL

Fast machine, lower priced memory, and small memory are inconsistent! Assume the 11/40 system price is 50K in CY74. This amounts to about 48KW average. In CY77, this amounts to 128K words average, hence should PDC better get more physical memory space "pdq"?

3. Low end

The memory cost here of say \$600 (1977) for 8K will be a very small part of the system, and permit more capability in monitors. Note, this is approximately the license price of RT11; and the price of 1.7 days of software support people.

The calculator people who sell at \$8K (same as CLASSIC) will begin to go at us competitively, because they will be working up to a more functional unit at same price.

The calculator people (HP, Tektronix, and possibly the hand-held guys such as TI) will also go down in price, giving them more volume, and putting more pressure on our relatively higher priced systems. Note, they are lower in price because the application is fixed (e.g. BASIC).

4. Applications

I believe we want to be working away from low level monitors, and languages as we have done in the past. Alas, we have a whole new set to do? The special function languages and systems are going to chew away at all parts of us, if we're not careful.

5. 10 versus 11

I'm unhappy that we even think of the 11VAX extensions as a new machine. However, I believe the 11 will be pestered and limited without the extensions. The machine is clearly limited in the 77-80 time frame at <100K which will be 128KW-512KW, and get into timesharing. The 10 and 11 will clearly conflict in the future (as we start to see the problems in large 11/70 that demand RAS, and quality just to stay alive).
...the price (markup) probably also has to get there.

6. If the model is correct and I believe it is,

A memory size determines the outcome of a system and each

SUBJ: PROJECTED MEMORY PRICES

DATE:
FROM:

business (our market product lines) is only capable of selling at a constant price (e.g. \$50K) due to fixed selling methods, etc.

Therefore, all systems will evolve to a substantial amount of generality to do the same function in a mass overlapped fashion. Here we see: IAS, RSTSV7 extensions for GPTSS, RT FG/BG, and 2-PDP-10 systems! The 11VAX adds more! Also, new competitors will take over our traditional systems at lower prices, while we sell up?

GB:mjk

Attachments

Distribution

Product Line Managers

OOD

Marketing Committee

VAX Group

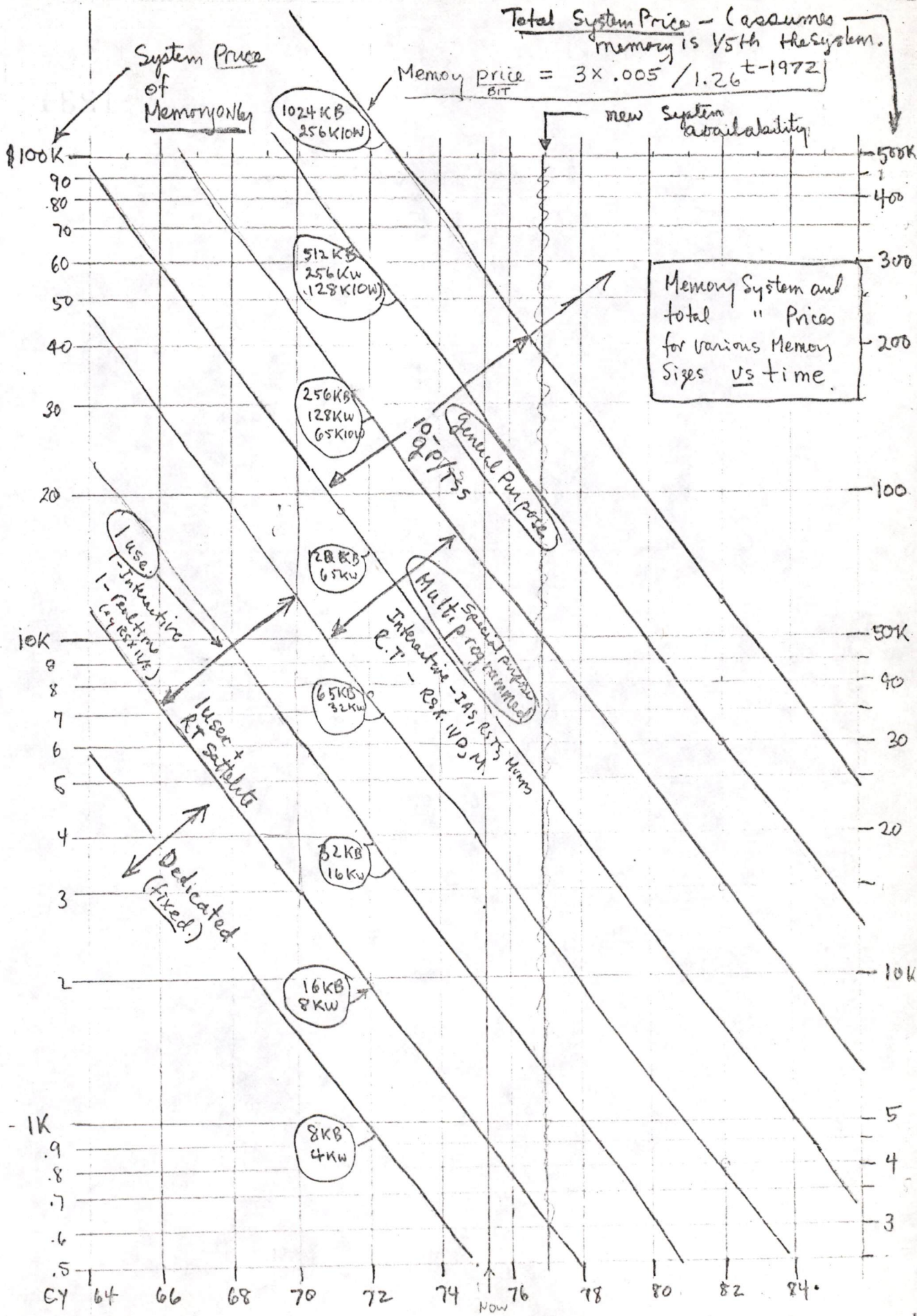
Bruce Delagi

Steve Teicher

Larry Wade

Mel Woolsey

cc: John Fisher
Ken Olsen
Bill Thompson



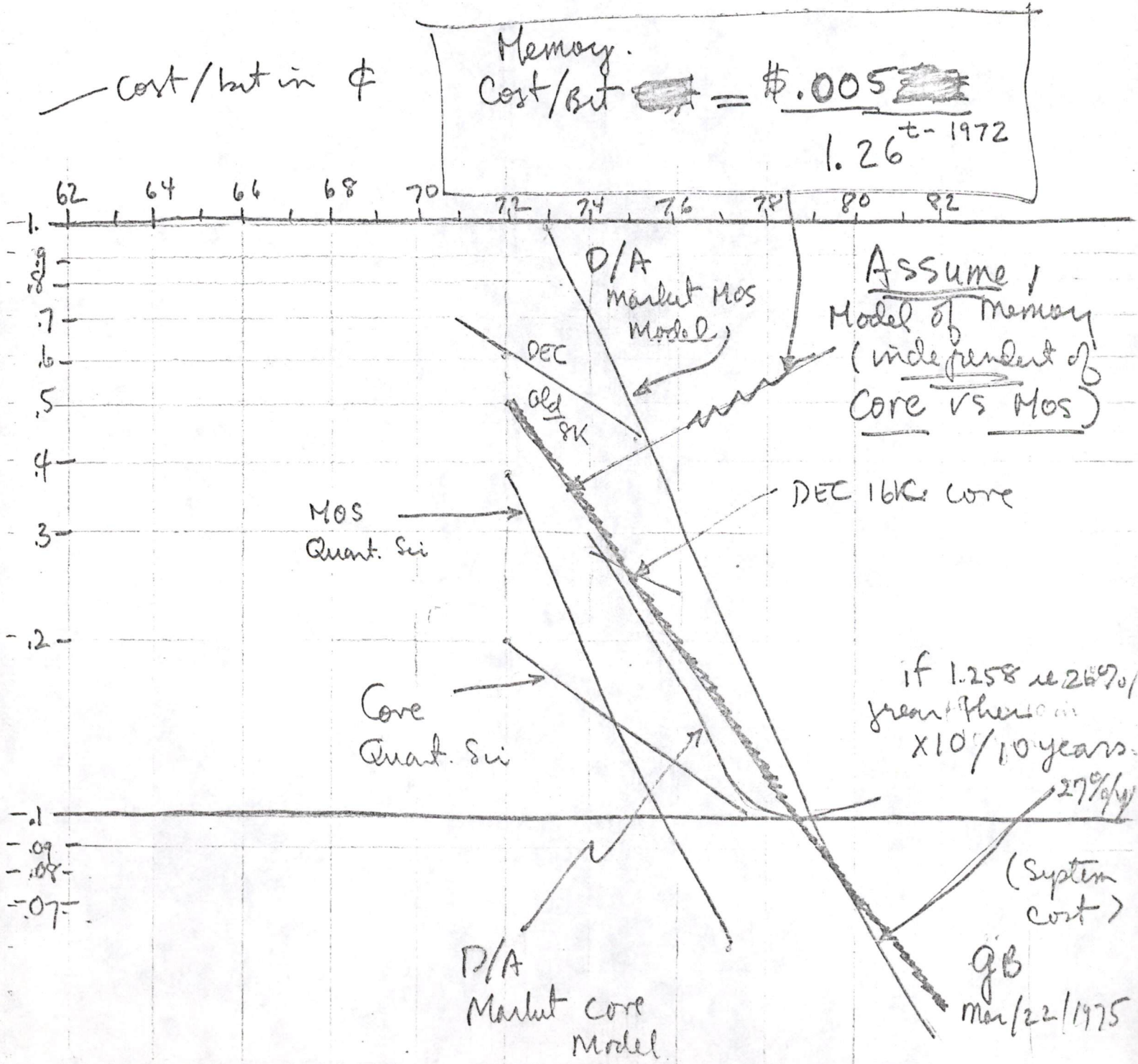


Table A--SYSTEM STRUCTURE, MEMORY SIZE, AND
RESULTANT USE

Structure	Memory Range	Function (use)	
Dedicated (fixed-] use)	16KB (4KB - 8KB)	Interactive--e.g. POS	Special purpose, Fixed
		Real time--e.g. scope, traffic control, automobile	
Programmable (1 user)	16KB - 65KB	Interactive--RT11	Small scale, generality
		Real time--RSX11S,M	
Dedicated (multiprogrammed n-users)	65KB - 256KB	Interactive--MUMPS, Trans. Process n RSTS	Special purpose
		Real time--RSX-11M, D	
Programmable (multiprogrammed n-users)	128KB - 1024KB	Interactive--IAS, TOPS 10, RSTS	Generality
		Real time--RSX-11D	

There are many implications of the 4 categories of structure and the 2-sub categories as to the operating system, its overall system structure, etc.

SUBJ: UC AT IRVINE

DATE:
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03-25-75
GORDON BELL

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SUBJ: TRIP REPORT: UNIVERSITY OF CALIFORNIA, IRVINE
THE DEC-8 CONFERENCE ON COMPUTING AT THE UNIVERSITY

I gave a talk on the delivery mechanism, computer, operating system, etc. at the above conference that Julien Feldman organized. It was a 2-day conference and there were a dozen or so speakers and some working sessions/discussion groups.

A list of the attendees will be sent to Charlie Spector if any one of you is interested. It might be worth sending a mailing to them.

In general there was a lot of controversy and questioning about how computer aided instruction or how computers in the university would be used in the next few years. clearly a big problem in mass CAI, in fact some people think is insoluble, is the high cost to write the CAI texts; in fact there is data on the PLATO system, that it takes 150 to 300 man hours to write 1 interactive console hour. Thus at these prices, there has to be whole different mechanism for writing programs. Right now the whole thing is probably impossible because of the tremendous lack of standards in this area. There isn't a device, that is a computer, and particularly a language that is well enough accepted that goes on the various kinds of machines that allows any standardization to occur here; hence, there is almost no exportability of programs among systems, and even among installations. We of course, contribute to the chaos by our own languages, BASICS etc., and although we are just part of the problem, the educators themselves are clearly a part of it, because they don't want to standardize yet.

While I was there I visited the UC, Irvine, computing system which consisted of a Sigma 9 or 7 and a PDP-10. The Sigma was running more users than a PDP-10, and had better response times. They also had a superb APL that ran better on the Sigma

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FROM: GORDON BELL

than the PDP-10 APL, primarily because it was a smaller program and was run with overlays as opposed to a single program. The machine with the APL (SIGMA), had a number of Tektronix graphic scopes on them for this purpose, and APL had been enhanced with graphics. It is by far the most impressive system that I have ever seen. APL is the only language for graphics as far as I can tell. Perlis tried to convince me of this several years ago, but he never got his system really working. These people had extended APL, and the results were just beautiful--that is plotting a single vector was plotted as a time series, plotting pairs were plotted as line segments and so on, so that all of the elements of APL correspond to picture elements and the impressive thing is that with a very small APL program, create 3 dimensional surfaces very cleanly. This really had very high payoff in some of the physics programs because one could see force fields calculated, etc., Prof. Alfred Bork, of the physics department has done an incredible job in producing a number of programs for teaching various levels of physics up to various parts of quantum mechanics. When we get our CLASSIC 11 with graphics and APL, he'll be the ideal user.

It is worth a trip to simply see the system in action. The Tektronix graphic terminal part is in Irvine, and the results really show it. Namely, there are Tektronix (50 to 100) scopes and there were just lots of graphics being used in this application. All of the stuff was far better than any of the graphics I have seen on any of our systems, including the flickery Caldec/REDAC system that we use to layout printed circuit boards. The other thing--these are really low cost. It shows what you can do when one has a good low cost graphics terminal. One of the themes of the conference was trying to understand just where the economies are headed in future CAI systems. It is clear that the CLASSIC kind of system is what everybody is counting on as one of the alternatives. It was their expectation and I reinforced it by some numbers that one wants to get on a production learning curve here, and really turn these things out in high volume as we hope to do in the case of CLASSIC.

At the other end of the spectrum, one expects lower cost timesharing systems along the lines that were used in the PDP-10 and the SIGMA for this application. The real difference here is that the levels of programs that are run on a large machine are entirely different from what one expects to run on a small machine. Also the unanimous need was that whatever one did on a small machine should be transportable from the small machine to the large machine. In fact, Ted Kehl who runs the computation center at UCLA, and has a large 91

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GORDON BELL

believes that one should be constrained when using languages to have the ability to move from the large machine to the small machine, (2) to move from the small machine to the large machine, (3) whatever languages that are chosen are to be a committed language and that authors should be encouraged to use these committed languages where standards are kept and enforced; and the computation center essentially has a commitment to this over a long period of time. Kehl also believed that there should be enough kinds of facilities so that there could be duplicate development of course ware so that one can have various options and alternatives to understand this whole process as opposed to really locking on a single standard, which isn't really in the cards for right now.

Also there was a person from Mel Plesekoph's office and he suggested a terminal that he thought was ideal. He wanted a desk mounted computer with graphics--note, it is CLASSIC 11 with Len Hallio's terminal, and he also wanted a portable version of that same terminal; and then he wanted one that had some ability to have a printer attached to it,

From what I could tell, there is a great deal of interest in Tektronics to try to supply exactly that. Notice that in the Tektronics display, I have described above, they had APL character sets on them already, so there is a lot of knowledge that APL can be an important interactive thing. For everybody who was there and who had switched from BASIC to APL, there was just no comparison in terms in the amount of work that one could do at the terminals, and one got from students, there was just no way to move students from APL back to BASIC after they had experienced APL. The productivity by any reasonable means was an order of magnitude better.

It is also interesting to note that Hewlett Packard is betting on the high speed magnetic tape to do the same job as the floppy disk. I hope this is true, because I think it is one of the world's biggest losers but I just can't believe that HP is that dumb. The other piece of gossip is that there is a pedestal stand for the 2640 and a 21MX plugs into the bottom of the pedestal, giving them something probably like our CLASSIC. Since we have an APL for an RT system that was written in Oregon, I really believe we ought to push to investigate this and dissect it and see how good the APL is, vis a vis some of the other APL systems, because I view it as a very important product in this and the engineering market place. As an old BASIC programmer of 2 months.. anything is better.

Comment on the PDP-10 versus the SIGMA 7

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DATE:
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GORDON BELL

Their belief is that there is too much terminal interaction on the PDP-10 and that is why it doesn't run as many users. Someday someone ought to try to understand where all the performance goes down the drain on the PDP-10. How much really gets delivered to the users? I saw the SIGMA clearly out performing the -10. They had about 60 users on a 128K SIGMA 7, which is more than a comparable 10. Someday if we get into a competitive situation with a real monitor, the 10 is probably going to have to get rid of its full duplex time consuming, highly interactive, unnecessary, style in the terminal area, and streamline that part of the system. But it probably won't come to a crisis until the VIROS system gets out, in which case the marketplace will go bananas when they find out that we have helped the hacker at the terminal to the exclusion of much performance. Is the market big enough for the hackers who do the system programming on the DEC system 10 or are there people who would like to skip all that garbage and just run at some reasonable language such as APL? After all you really can't compute at that interface,

GB:mjk

Distribution

Al Brown
Dick Clayton
Pete Conklin
Len Hallö
Bill Kiesewetter
Ed Kramer
John Leng
Larry Portner
Charlie Spector
Pete Van Roekens
Mel Woolsey

SUBJ: LANGUAGES POLICY

DATE:
FROM:PAGE 1
03-24-75
GORDON BELL

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SUBJ: LANGUAGES POLICY--WHAT IS IT (ESPECIALLY VIS A VIS PL/1,
 BASIC)

Attached is the abstract of a talk I'm going to give at a DECUS session (it's not the keynote topic). The talk goal is to inspire some feedback, plus give them some of my concerns about programming in BASIC (or other non-standard languages).

Also attached is a note by George Poonan of R&D outlining pros and cons on PL/1.

Right now we're clearly going to have to do work on all BASICS. RSTS is slow, and needs features and BASIC on the 10 needs features. If a BASIC standards group ever acts beyond entry-level BASIC, it may not standardize on RSTS, but move to the current Dartmouth version (done about the same time as RSTS), that doesn't have all our syntactic sugar, but does have subprograms--thus facilitating sharing. The way BASICS have evolved, we could do a subset of PL/1 and call it BASIC, and the world would probably be better off. John Xenakis is implementing an interactive subset of PL/1 on the 10 and it looks and "feels" quite superior to BASIC.

I view that we now have very marginal support for all our languages except for APL-10, COBOL-10, FORTRAN-10, and MACRO-10, and various other 10 languages (e.g. ALGOL< SIMULA, LISP, etc.). The 11 languages don't have complete packages for debugging (e.g. only ODT), running (e.g. only Interpreter for RSTS), sharing (library), and some are incomplete.

Should we do a few languages well with compiler, interpreter, debuggers, runtime library extensions, formatters, etc., on the 11? The priorities feel to me:

1. FORTRAN--debugger, string package, encourage sales of WATERLOO fast FORTRAN for interactive use to be announced by them at DECUS.

SUBJ: LANGUAGES POLICY

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2. COBOL--finish, debuggers, plus other support, also the mini-COBOL as subset.
3. BASIC--I'd like to not invest in any beyond the min. std., plus wait till a standard occurs,
4. PL/1--subset call it: BASIC--WHOOPIE, Probably interpret first to get user reaction and then a compiler.
5. APL--encourage someone else to build and rent on our machines. (probably the best and could (should) replace BASIC, FORTRAN, and PL/1 in interactive use).
6. MACRO--DDT

Do we want to keep going incrementally reacting to the market or is there a leadership position?

COMMENTS PLEASE!

GB:mjk

Distribution

Product Line Managers
Software Engineering Managers
Software Engineering Consultants
Marketing Committee
Al Brown
George Poonan
Dave Stone
Larry Wade
Mel Woolsey

COMMENTS ON USING BASIC(tm) AND QUESTIONS ABOUT
IT'S EVOLVING FUTURE

C. G. Bell
January 30, 1975

ABSTRACT

BASIC has been used extensively as both a language for learning about programming and more recently to build system applications. It was initially conceived as a very simple language which could run effectively as a time-shared system on mid-second generation hardware.

From this beginning, it has evolved into many dialects and applications. Each new implementation of BASIC promises new capabilities that are in some way subset compatible with earlier ones--especially the first--i.e. "Dartmouth BASIC." There is even a standards activity to sort out some of these issues. But it mainly addresses the "Dartmouth BASIC" level language while the dialects are well beyond this in all directions.

As a fellow computer user, I am currently entrapped in a program written in BASIC. I think it is worth asking a few hard questions about its future: should we just ignore the work on structured programming knowing that the basic BASIC language violates many of the principles? In asking new users to learn BASIC, are we teaching them all the bad tricks of assembly and sub-assembly language programming? Is it possible to have a better basic BASIC and superset? Does anyone care about non-transportability of programs among machines that this situation encourages? Does anyone want a program library? Is there a better basic basis for programming?

Are the users-manufacturers ensnared in a self-defeating programming language evolution that leads nowhere because the basic foundation is insufficient.

(tm) Dartmouth College

*



Done [unclear] [unclear]

INTEROFFICE MEMORANDUM

1243

TO: Larry Wade
CC: J. Bell
A. Brown
P. Christy
L. Frampton
E. Peters
SUBJ: PL-1

LOC/MAIL STOP
ML12-2/E39

DATE: March 18, 1975
FROM: George Poonen
DEPT: R & D Group
EXT: 3537
LOC/MAIL STOP: ML3-4/E41

[Handwritten signature]

MAR 21 1975

At the last meeting held on Wednesday, March 12, I sensed a feeling that we were slipping into doing PL/1 without any explicit objective. I might very well have been mistaken but in case I am not I would like to re-emphasize some of the pros and cons. While I am all for doing PL/1 there are sufficient reasons for NOT doing PL/1. Therefore it is absolutely essential that we have some well defined goals for PL/1 on the PDP-11.

PROS

CONS

- 1. There is a definite need for a suitable high level language to program a number of emerging applications, e.g. small information system (report available from Market Data Center).
- 2. Claims have been made that
 - a. the PL/1 user population is growing fast and has overtaken FORTRAN.
 - b. PL/1 is catching on fast in Europe
- Note: However, none of these claims have been substantiated by data.
- 3. PL/1 will certainly enhance our image. Today PL/1 is almost synonymous with IBM.
- 4. During the last few years Burroughs, CDC, and UNIVAC have or are implementing PL/1. In addition Honeywell has PL/1 on Multics (For more data see Lois Frampton's report).

- 1. The majority of product lines have NOT expressed any enthusiasm for PL/1.
- 2. As far as I know we have not been inundated with requests for PL/1.
- 3. Cf Farrell Woods letter, and Datamation 73 the number of PL/1 users has remained relatively constant for the last few years. The Datamation survey indicated the following ordering (with respect to usage)
 - COBOL
 - Assembly
 - FORTRAN
 - PL/1
 - Other
 with PL/1 having less than 10%.

4. The world may not go to PL/1.
5. We dilute our intensely thin effort.

only not on other machines.

9. The market loves new languages - eg. BASIC, ⁺, etc.
a good one would probably be significant.

1244

5. Data General is very likely to implement PL/1 Cf conversation with Bob Freiburghouse. If the contract is signed DG will have one in 2 years.

6. ANSI standardization is expected in 1976. This should increase its availability and desirability.

7. Some major users such as GM, Ford, Sylvania, Kodak? appear to be interested in our doing PL/1.

8. If DG comes out with PL/1 first theirs will be the de facto standard. It is essential that we keep close track of what is happening at DG and whether the contract with Freiburghouse has been signed.

4. I doubt if we will be able to provide the full standard on the -11. There is no subset standard.

5. If Transaction Processing is the major market area that needs PL/1, then we had better define the functional requirements of this area. Subsetting PL/1 is difficult. Without any explicit objectives it can be disastrous.

6. Others such as Bell Northern Research, Canada take the opposing view Cf letter to Al Brown.

User / Technical

1. Without a doubt superior to COBOL, FORTRAN, or BASIC.

2. Very suitable for application programming.

3. A suitable subset of the language, e.g. the one proposed in the report or the one proposed by Freiburghouse is easier to learn, implement and is suitable for most of the applications mentioned in the report.

4. Since the last report some tools have been developed, e.g. Parser Generator. This can be used both for parsing as well as other phases. This will greatly aid in formally defining the subset as well as implementation.

0. There is a need for a good language.
— no amt of tinkering will make BASIC st.

1. In its full generality very powerful, hard to learn and almost impossible to implement.

2. NOT the ideal implementation language. A number of superior implementation languages are available.

3. No one at DEC as far as I know, has implemented a PL/1 compiler before. However, at least a number of us have implemented other compilers which have included almost all the features for the subset we have mentioned.

There is not a defined "interactive PL/1" — Interactive computing is us.

Don't make it
the Impl Language!

Really nice language

5. Suitable for data base applications

4. Almost all existing DBTG proposals and implementations have been based on COBOL.

Economic

1. We will be implementing a subset.

1. Historically almost every first attempt at doing PL/1 by manufacturers has been a disaster. It is generally felt that the main reason was trying to do full PL/1 without a full understanding.

However, our understanding has certainly improved since then.

2. Unlike FORTRAN we will not be able to do a crash project to implement PL/1. We will have to plan ahead.

3. There is no reason to believe that a PL/1 implementation will cost less than the FORTRAN IV PLUS implementation. Some believe it will cost 1 1/2 -2 times as much.

In conclusion

- a. The market data does not conclusively point to PL/1;
- b. PL/1 is sufficiently complex that we must plan ahead about two years;
- c. we cannot do full PL/1. Therefore we must carefully evaluate the market goals and define our objectives so that in turn we can define an adequate subset. A preliminary definition of such a subset exists with respect to certain applications.

If our market perspective has changed let us re-evaluate the subset in terms of the new markets.

GP/bd

SUBJ: SYSTEM FORECASTS/ENG. BUDGET

DATE:
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GORDON BELL

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SUBJ: A LOOK AT THE FEBRUARY SYSTEM FORECASTS FOR FY76-77
 AND THE FY76 ENGINEERING BUDGET

To: Distribution

I plotted the data that Curtis/Frith collected from OCG, OEM, IPG, LDP, TELCO, BUS and DEC-10 to get some feeling of where the business is supposedly going over the next few years so that we could compare this with our spending and product plans. The categories of the size dimensions of the matrix: terminals, micro (LSI-11), small (8/11-04-05-a40(BGS)), mid 40, 35-40-PDQ, large 45-70-85, and MACRO (10's). The categories of the function dimension of the matrix are: Iron, 1 user, real time, timesharing.

While it isn't worth it now, these categories are probably bad, e.g. iron eventually ends up being used for either: real time processing-LDP, switching--COMM, control--continuous--IPG, control-discrete--IPG), or interactive (1 user, n-user dedicated application with varying sized data-bases, n-user 1 language, n-users/1-languages). This function dimension needs improving, and "transaction processing" will make it more muddy!

Marketplace

Figure 1 shows the total NOR plotted by increasing system size, so that one can observe migration of the various segments. This should be viewed with Figure 3, which shows the growth of each of the segments independently. One gets an idea of the relative growth, and sizes of each of the segments. Anything that has a linear growth (e.g. MACRO and MID) are in essence losing % internally. Here the B is clearly diminishing and the high growth businesses are terminals and the micro segments.

The MICRO 8 and small segment are really quite similar, and the whole set is not growing that rapidly, but are at the expense of the 8. Eventually, the MICRO may take business from the low end UNIBUS, given the systems are forthcoming.

SUBJ: SYSTEM FORECASTS/ENG. BUDGET

DATE:
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Figure 3A plots the % NOR for each functional category versus time. Here, Iron (OEM) is losing Internal market share in FY75 along with real time and 1 user to interactive computing.

In getting these top down forecasts for the first time, I had the terminals separated and I want to keep it this way; but it's not clear how we deal with the add-on part of the terminals on each of the business product segments. For example, should we count the terminals on the time shared systems we sell as terminals or as the system? (These obvious choices: all terminals are separated; only the terminals DCG sell are separated; and terminals are separated for each product market product line.)

Figure 2 shows the projected NOR for 74-77 on a % basis for each categories of the size dimension. (It might also be instructive to do this on the basis of a good function dimension.)

The main value of looking at NOR by % is to gauge whether our engineering expenditures match where we expect to be selling. Note: the PDP-10 has been excluded from the expenses, although the relative NOR is shown.

ENGINEERING EXPENSES VERSUS WHERE WE GET NOR

Figure 5 provides an alternative way of looking at the information, where % projected NOR (for FY74, 76, 77) is plotted against % expenditures for each system size. For totally fair (not necessarily most profitable, or one we want) allocation, each investment should be solely on its return. (I am extremely worried about terminals--not the expense, but will we be able to get the NOR in this new to us, competitive, commodity marketplace?)

Figure 4 shows a similar plot but by technology area.

GB:mjk

Distribution

PLM
OOD
PC
MC
Vince Bastiani

John Clarke

Ed Corell

Brian Croxon

1248

SUBJ: SYSTEM FORECASTS/ENG, BUDGET

DATE:
FROM:

PAGE 3
03-24-75
GORDON BELL

Bruce Delagi

Bill Demmer

Henry Lemaire

Ken Olsen

Bob Peyton

Grant Saviers

Tom Stockebrand

Steve Teicher

Mike Tomasic

Larry Wade

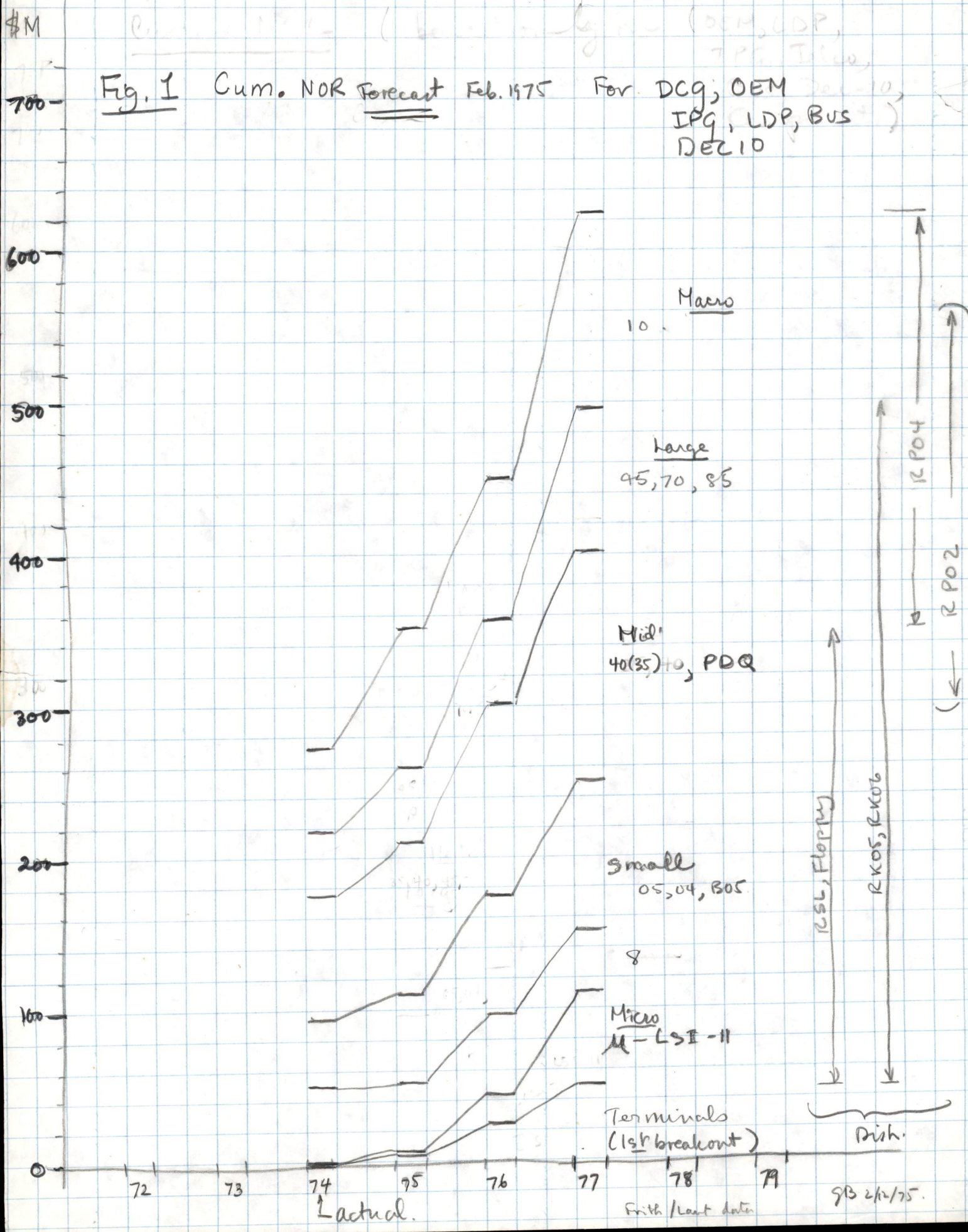
Mel Woolsey

Arthur S. Bell

1252

Cum. NOR Forecast (DCG, OEM, IPG, LDP, BUS, TPE, Telco, DEC 10)

Fig. 1 Cum. NOR Forecast Feb. 1975 For DCG, OEM, IPG, LDP, BUS DEC 10



7am



12 13 14 15 16 17

Fig 2. Feb 75 - Projected % NOR + % C. Eng. Expense FY76

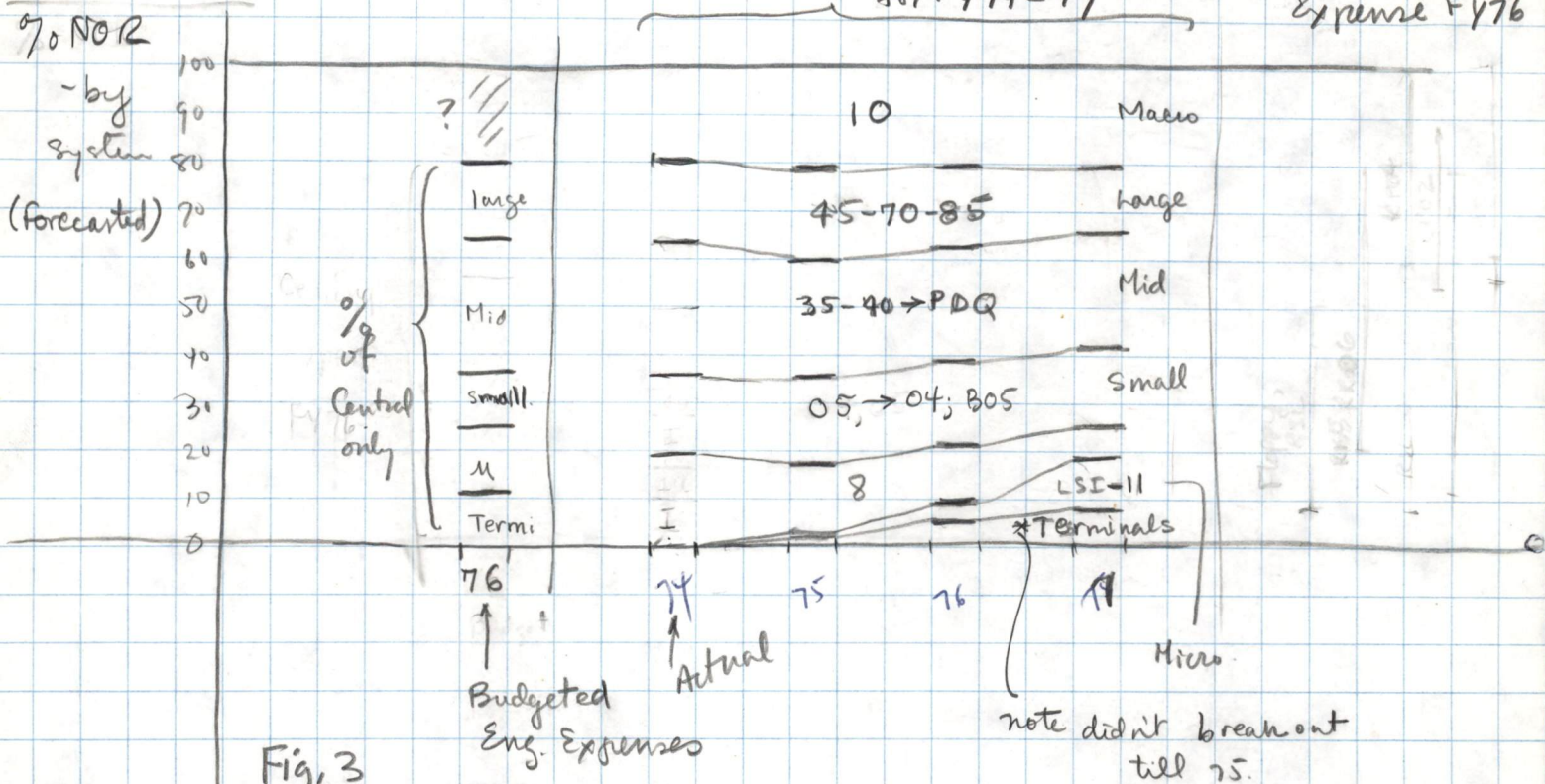


Fig. 3

\$M - NOR for each product-class. (Projected Feb. 75)

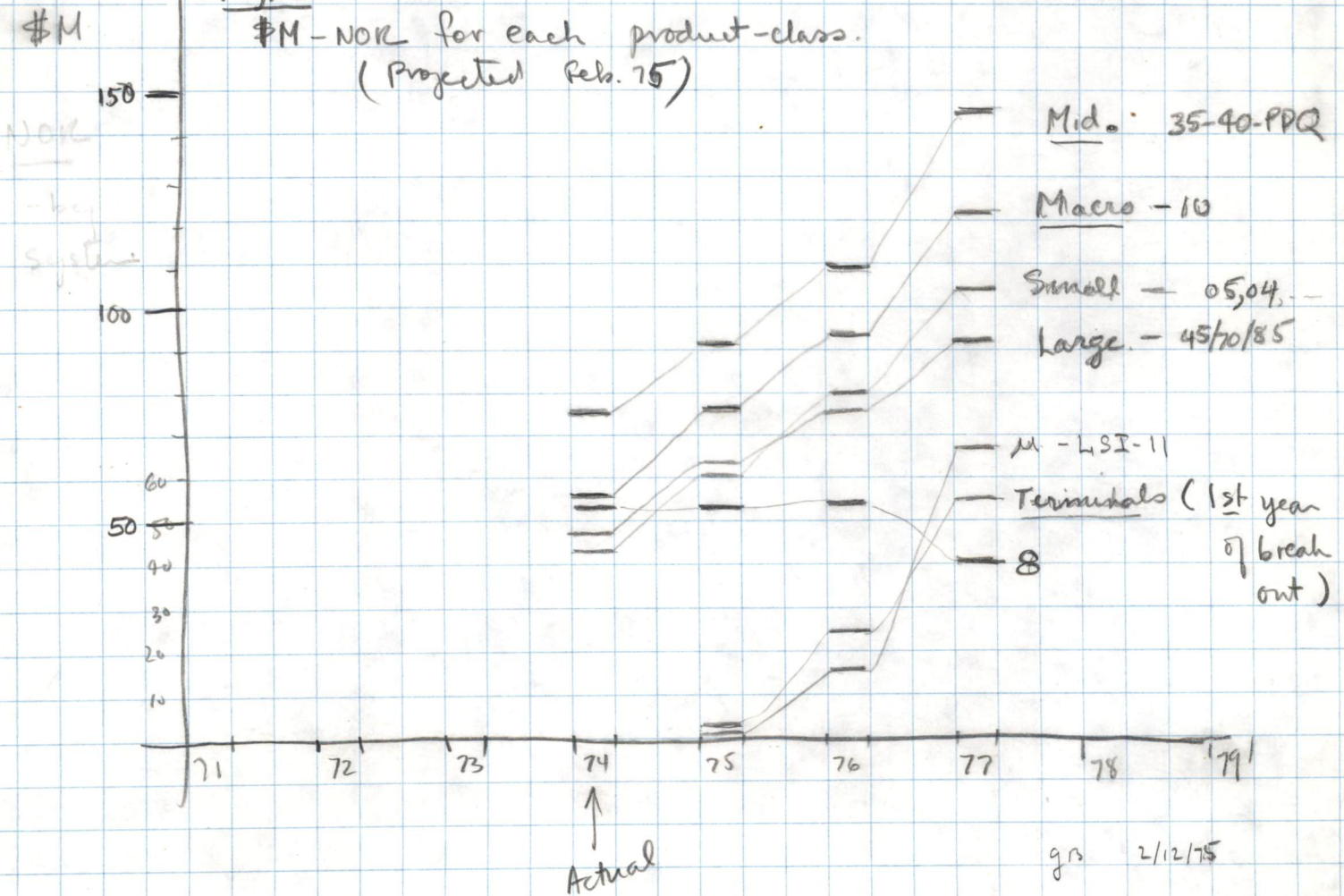
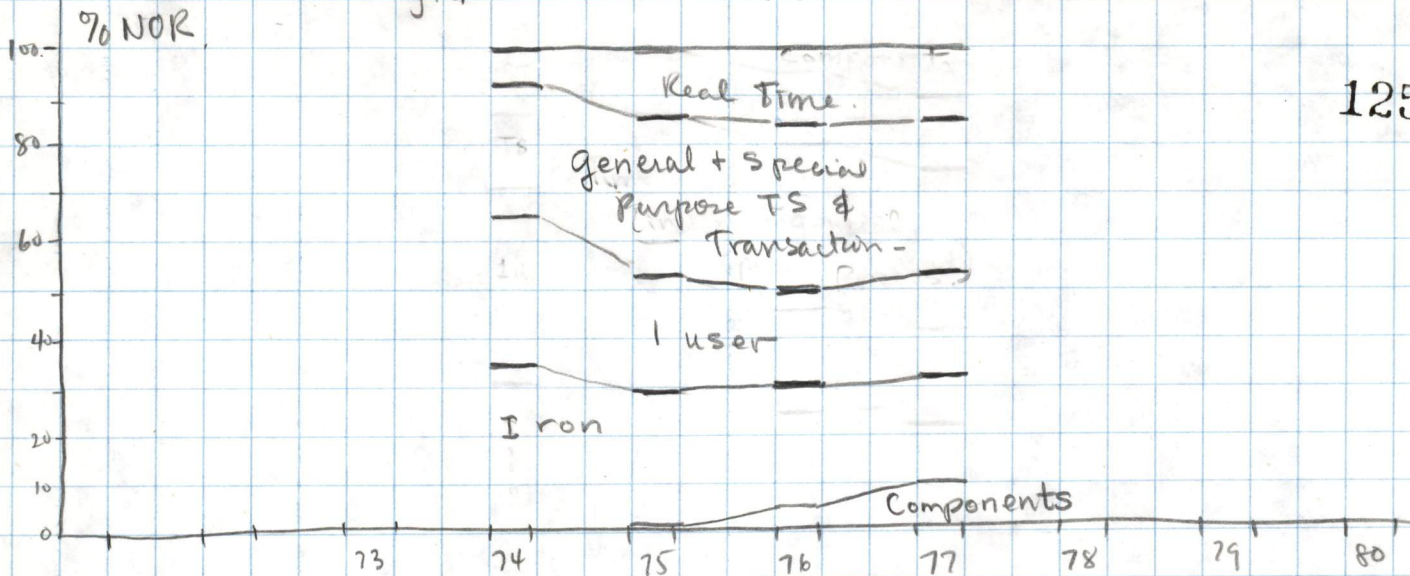


Fig. 3A Functions (% NOR) vs time.

1254



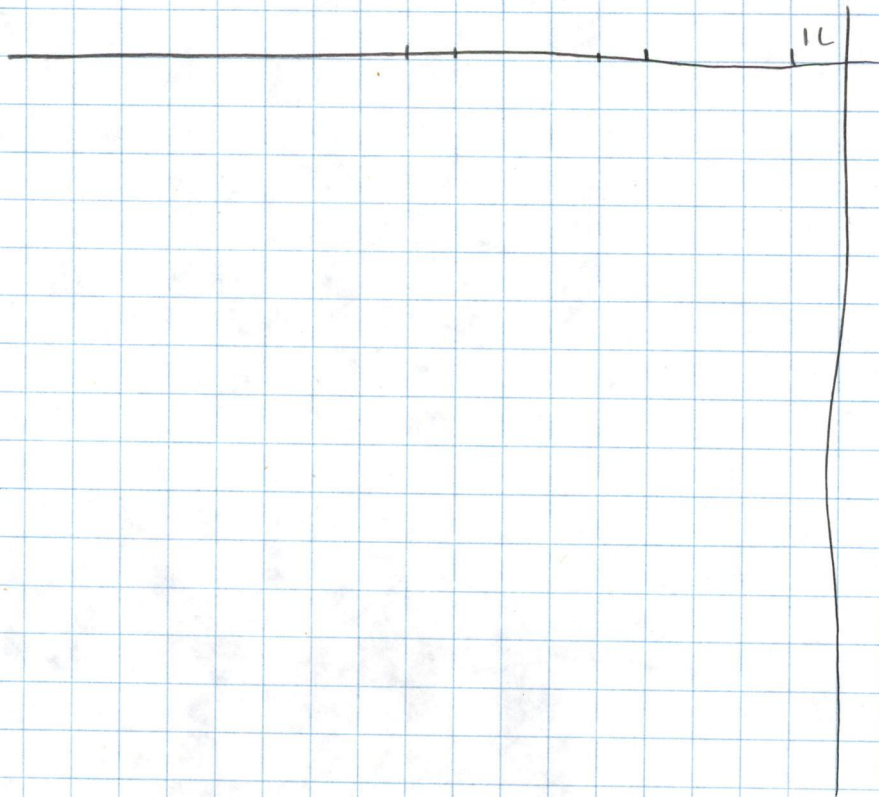
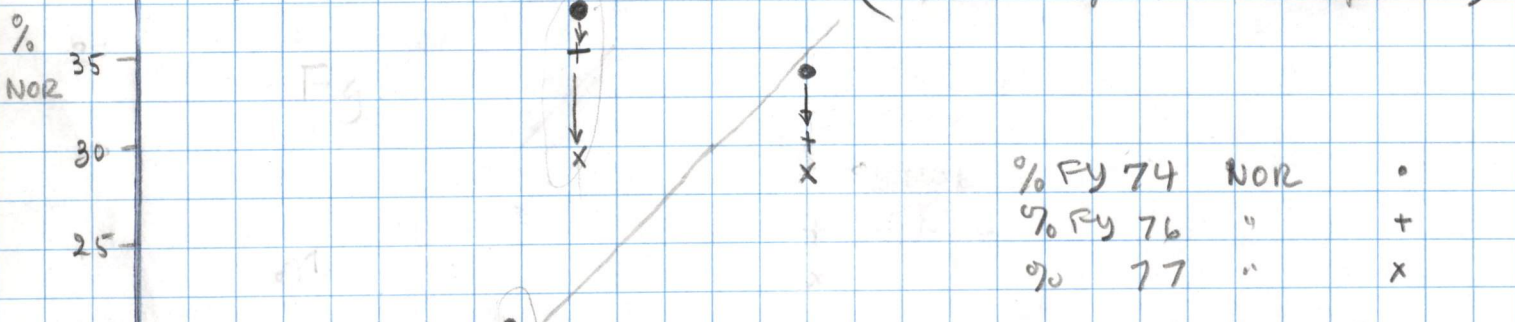
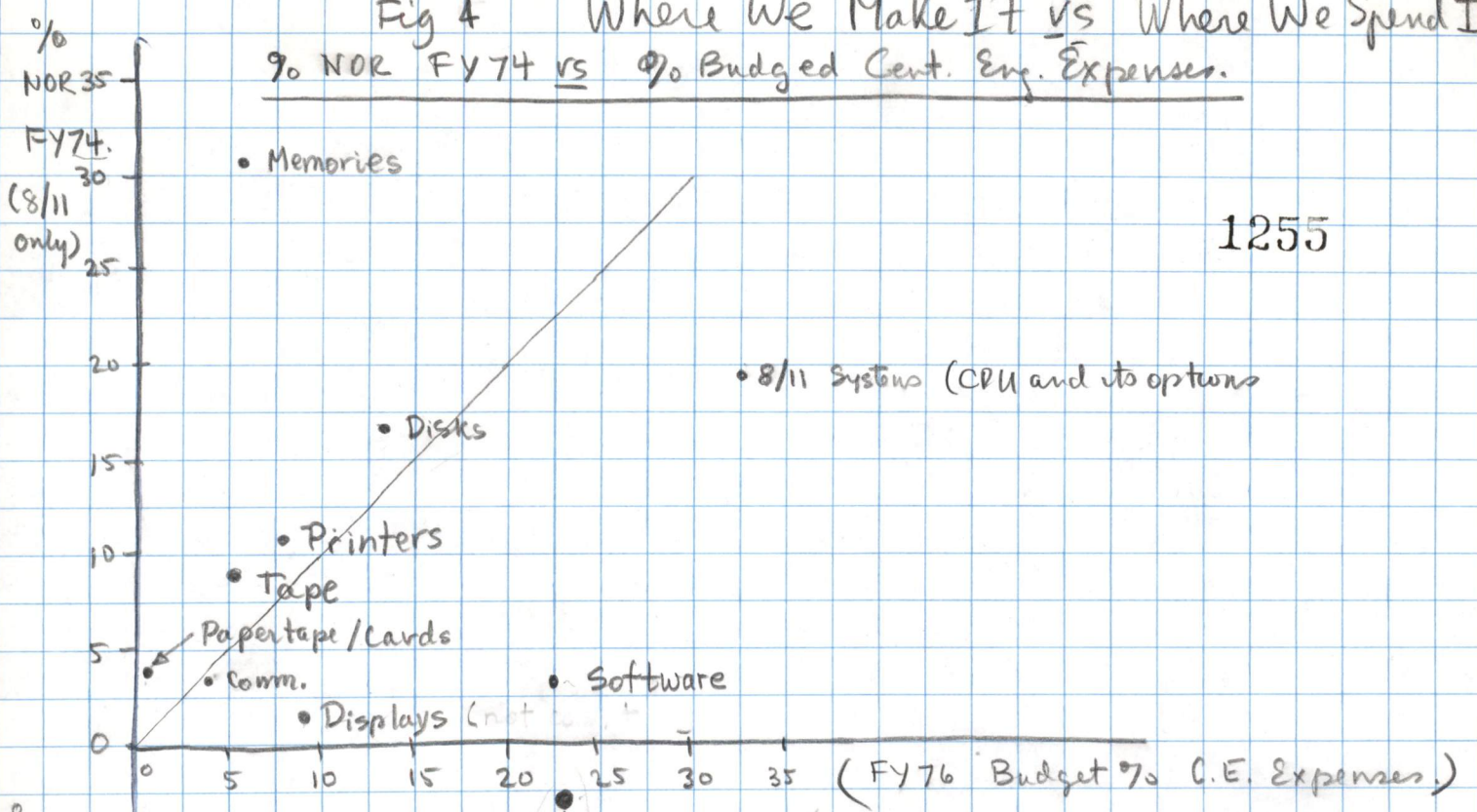


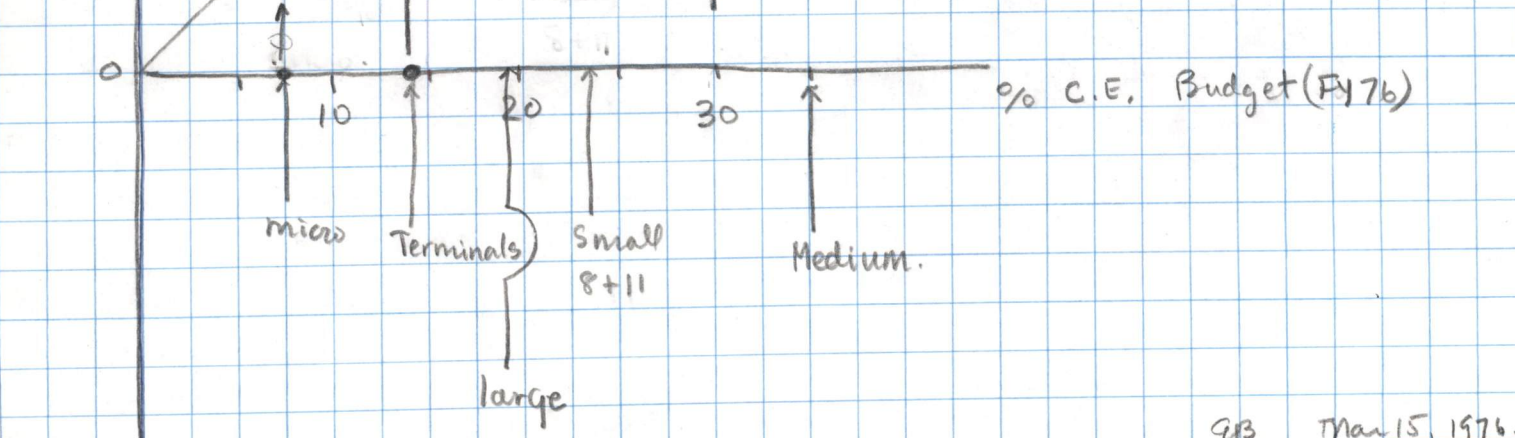
Fig 4 Where We Make It vs Where We Spend It!
 % NOR FY74 vs % Budged Cent. Eng. Expenses.

1255



% FY 74 NOR	
+	•
+	+
x	x

Fig 5
 % NOR for FY 74, 76, 77
 vs
 % Cent. Eng. Expenses.
 by
 system size (Excludes PDP-10)



SUBJ: PHIL'S DESK CALCULATOR

DATE:
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GORDON BELL

* * * * *
 PLEASESEND TO: FILE
 * * * * *

SUBJ: PHIL'S INTERACTIVE DESK CALCULATOR PROGRAM TO CALCULATE
 PROJECT/PRODUCT P&L, ETC,

INVITATION

Having given a demo of the above to Operations Committee and the Product Line Managers, this memo describes the program, how it is used, the results, and other uses. Phil Laut and I would like to get with you to demo the program and talk about its uses in Product Management.

THE PROGRAM AND USES

The program called PROJEC operates in two modes:

1. A simple desk calculator whereby P&L-type functions are done. In an immediate mode a user can put up a P&L statement on a periodic basis (quarterly, semiannually, bi-yearly, etc.), and then do various operations, (e.g. combine rows by addition, subtraction, multiplication, etc., calculate ROI on a row, discount a row and all the standard functions that one does with a P&L statement row). The P&L statement can be saved on a file and reread. This is done purely like a desk calculator and everything is done on a command-by-command basis. There is no programming involved.
2. Calculation of P&L for an input file or set of input files. A text file which contains input data to the P&L worksheet is read and then a P&L analysis is carried out to determine various indicators (product contribution, NQR, product contribution %, ROI %, crossover date, development per sales ratio) plus the normal proforma P&L statement for the input data over the product's life.

PROJEC is used to study a product/project from a P/L standpoint. It's use includes: generating a base P&L case, observing effects of project slip, different costs, prices, sales

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volumes, work in process and accounts receivable delays. From this, sensitivity to factors can be computed, to arrive at prices, etc. with respect to a demand curve, etc.

Finally, there is an editor called PREDIT, which allows the user to easily input data in the format suitable for PROJEC. Actually PREDIT was written to facilitate the inputting of data although the input to PROJEC is a standard ASCII text file which can be prepared using BASIC, SOS, TECO, etc. editors.

USE OF PROJEC FOR P&L OF AN INPUT FILE

The following will describe the use of the program which inputs the data from the file and does the P&L calculation. The memo will show how the program has been used to analyze the LA36 plan together with some conclusions on pricing.

Figure 1 shows the input file, a standard BASIC text file, consisting of 16 lines of text--1000 to 1180--note, no lines 1070 and 1080. I have probably overly annotated the input file but one can see the structure of input format. An entry consists of an attribute defined by a name (i.e. a text string) terminated by a colon (e.g. MFG,START,UP:), with a separator, followed by a list of values or a single value, terminated by a ";". Each item of the value list corresponds to a value of a time series. For example, on line 1110, the attribute, /PRICE: is the per unit price beginning in fiscal '73, and the prices for fiscal 73 thru 79 are 0,0,1.52, 1.473, 1.372, 1.439, 1.45. The dates are written in a format which is shown at the top of the figure. The date is either a 2 digit, 3 digit, 4 digit, or 6 digit number. These are written such that I can easily transform, and do arithmetic on the dates. The key attributes of dates are T.DATE:, which is the date of the plan; begin date, T.BEGIN:, which is the beginning date of the project (that is when the P&L starts); T.END:, the time the project ends from the P&L; T.C:, denotes when the file was changed (a list). In this way one can time-stamp all the changes that are appended to the plan. Note that the project name and the project author are present, and these are standard text strings. Line 1060 has multipliers for time scale of P&L, in this case, 12 month intervals. The number of units is in thousands and the dollars are in kilo-bucks.

RUNNING THE PROGRAM

PROJEC is run like all BASIC programs. Figure 2 shows a run of a base case. One calls the program (OLD PROJEC). A number of

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questions are asked by the program to get various file names that will specify the names of the attributes the program knows about; the print plot format file, which tells how many attributes (lines of the P&L) are to be in output format; and the output file in this case the LA360 (which is the name of the output file where the results go). If I had named the output TTY, then some of the results would come to the teletype.

There are a number of questions asked about the base cases that are to run. These are: the ship delay in months, the sales, cost, and price alternatives. Each of these can have a list of alternatives to look at and one gets all combinations of the cases. In this case, we are going to run the standard plan unchanged so each of these multipliers are 1. The accounts receivable time is 3 months and the work in process time (built into DEC) is 9 months. We then give the command, CPL, to calculate P&L; and the program responds by asking if the file is to be direct or indirect. In the case of indirect files, the file contains the names of other files to process. In this case it is the direct file, so it simply processes the file called LA36N--which is given in Figure 1. Executing CPL takes about 1 second. Now, unfortunately, the user has to return to BASIC, which is shown in the figure to copy the LA360; that is the output file to the teletype; the remainder of Figure 2 shows the results of the run (copied from file LA360).

There are 3 parts to the output results. The first part is the key sheet, which denotes the abbreviations of the output are called; the second part gives the attributes that are not put in the P&L statement. In this way the user can see what the plan was in total; and the third part is goodness indicators and P&L.

These goodness indicators denote ship delay, the sales factor, the cost factor, the price factor, NOR, product contribution, % product contribution, %return on investment, the development dollars, the development dollars per NOR %, and the crossover date, in this case the 10th month, 76th year. Here one can look at the P&L to get the various indicators. At this point, the reader ought to understand both the input file and the results of the base case, because they are just the standard DEC P&L with the exception that the ROI is calculated on the basis of last row on the P&L statement. ROI is like the product contribution row except it assumes that manufacturing materials are purchased 9 months before the unit is shipped, and that bills are collected 3 months after the product is sold. Therefore, one can see the effect of all this.

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USE OF THE PROGRAM FOR OTHER ANALYSES

In Figure 3, we use the program to explore some pricing alternatives. The pricing guidelines are 50% product contribution.

To run the program, everything proceeds as it did before, except that in this case, 5 alternative prices are used: .95, 1, 1.05, 1.1, 1.2 (the average is 1.06); and everything else is the same. The program simply gives the indicators for these pricing factors. We thus explore the sensitivity of NOR, and product contribution to price. In Figure 3A, % ROI, and % product contribution, product contribution dollars, and NOR dollars for the various pricing cases are plotted. Note, we really should raise the price by 6% in order to achieve the 50% product contribution goal.

In Figure 4, other cases are tried to determine sensitivity of the project to slip, different sales alternatives; a cost overrun of 15% and a stable price. There are $2 \times 3 \times 2 = 12$ alternatives to consider and the results of the indicators for these 12 cases are shown. Note, that in assuming no slips, there is no volume which will allow the 50% goal to be made. Raising the volume to a factor of 2 does help, provided the costs do not change. If we have a cost overrun of 15% on the project, the project does deviate from the contribution goal.

EXPLORING THE PAYOFF FOR A DEMAND CURVE

In Figure 5, I have explored the return assuming a certain price demand relationship. It assumes a doubling of volume for a 25% price decrease and there is a 10% learning curve, i.e., the cost decreases 10% each time the volume doubles. Going to a lower demand, provided the price increases, makes the product look better from a percent contribution; although NOR is lower. NOR and product contribution are non-linear, and worst case is getting a double volume at a lower price, whereas if we sold 4 times the units at much lower prices and higher demand, would give better results.

THE USE OF VARIOUS INDICATORS FOR MEASURING A PRODUCT GOODNESS

In Figure 2A, I have plotted 4 different indicators--product contribution per year, cumulative product contribution over the life of the project, effective investment per year (this includes capital equipment costs, work in process delays, and accounts receivable delays), and the accumulative investment. In each case the indicators are shown at the plan (times 1),

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at half the volume (times .5) and twice the volume (times 2). Here we can see how these indicators can be used to measure the project. Note, that the negative part of the scale (risk) is plotted in units of \$2 million, and the positive part (payoff) is plotted in units of \$25 million. Here one can observe how we can use various indicators for running the various product businesses. Note, that the one we now use is the product contribution per year--the first one,

Note, that cumulative product contribution is different than the cumulative investment (assumes work in process and accounts receivable). From the cumulative product contribution, the investment appears to pay off just before fiscal '76 ends; whereas, if you look at the cumulative investment, the payoff occurs after fiscal '76, or there is a year difference in apparent crossover. Different volumes of course effect the payoff time by several months.

Since the effective investment per year is the basis for calculating the ROI, and I am not using interest in the cumulative investment curve, then the payoff occurs much after fiscal '76. That is, it assumes there is no interest on the money. The effect of putting interest on the money is to slide the payoff time out further. Immediate money is worth more, and the time value of money is multiplied by the investment and the effect is to simply move the crossover date out further depending on the interest rate. In fact, the ROI percentage is that value of money such that the net amount that the project loses is equal to the net amount the project gains. The reason we haven't used ROI calculations is that it requires moving the inventories and receivable, and is an iterative process; it requires a search for that value of interest such that the net gain or net loss of the project is zero. I calculate the ROI percentage to the nearest 1% by doing a binary search for positive investment percentages. Beginning with 64%, I try 7 times to determine the percentage investment in the range $0 < ROI < 128$.

LOOKING AT OTHER PROJECTS

Figures 7 and 8 show the cumulative investment for various disk projects and for various display alternatives. In the case of Figure 8, Stockebrand has been working the work in process, and inventory delay problems by a single assembly line, and it is clearly worthwhile.

Note the project really looks much better by only having a 3 month inventory versus having a 9 month inventory. This has

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no effect on PC or %PC, as we measure projects within DEC. It affects the project payoff and also drastically limits the investment by the work in process.

USE OF THE PROGRAM FOR RANKING PROJECTS

In Table 1, various projects are ranked using the program. From an investment standpoint, we would like to use this as another set of inputs to look at projects.

FUTURE EXTENSIONS

In general, having worked at a terminal exploring various projects, has reaffirmed my faith that interactive computing is the only way to compute, and that we are in a fundamentally good business. One can with a relatively good program, explore lots of alternatives quickly and look for various optimizations in profit, NOR, or what have you. The program leaves a lot to be desired in terms of its interactive capability, but with it one can get a feeling of what a really great program would be like. The current BASIC and the standard VT terminals place clear limits on one's ability to interact. In extending the program, plotting is the highest priority. Here I'd like to see all the plots that I did, which are attached, indicating demand curves and sensitivity analysis done on line.

Some of the other extensions include looking at multiple projects and it would be nice to roll up the whole company in terms of its products: by hardware systems, by hardware/software systems, by technology, and on an individual basis with lots of cross checks against the input system forecast and project history. The common way of analyzing a P&L is by risk analysis, where one puts probabilities of different things happening and then the P&L is in effect simulated, and the net P&L is calculated. As long as there is a linear relationship between the various input factors, such as price, cost, etc., with the output, then we can simply use the various alternatives and take the average of all of these cases as one explores the various end points.

USE AND RELEVANCE

1. OOD might use indicators such as those of Table 1 to evaluate various projects when indeed we get into development budget bucks.
2. I see the product managers might use the program for pricing aids, and to determine whether they have a good

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project/product. This will let us explore various plans before their final evaluation..

GB:mjk

Distribution

Product Managers
Product Line Managers

OOD

Pat Spratt
Jack Smith
Irene Leary
Bill Thompson
Bob Curtiss
Herb McCauley
Ron Rutledge

date is: 2digit YR | 3-digit FYQ (eg 751) | 4digit YRMM (7503) | 6 digit YRMMDD

- In the value-list, one can set switches:
1. BDate (eg B761) denotes the begin date is FY76 for the value list
 2. CDATE (eg. C750315) date of change for this value list or C# refers to a change vector, T.C
 3. I# (eg I12) interval of list

```

LIST
LA36N 19:20 09-MAR-75
1000 T.DATE: B740700 750130
1010 T.BEGIN: 720700
1020 T.END: 790700
1030 T.C: 750306
1040 PS.AUTHOR: ED.CORELL
1050 PJ.NAME: C740700 B740700 LA36N
1060 *T: 12 *#: 1000 *$: 1000
1090 #: 0,0,6.6,13.342,34.552,34.488,28.125
1100 C750306 0,0,6.6,25,34.552,34.448,28.125
1110 /PRICE: 070,1.52,1.473,1.372,1.439,1.45
1120 /COST: 0,0,0.73,0.667,0.6,0.6,0.6
1130 MFG.START.UP: 0,0,150
1140 /FS.WARR: 0,0,0.1,0.1,0.1,0.1,0.1
1150 HARDW: 336,1072,1071,100,100,100,100
1160 CAP.EQUIP: 0,0,500
1170
1180
READY
    
```

denotes file was edited and changed on this day.

note a string has to be "held together" with intervening characters such as . or _

← latest change per unit price, begin FY73

← " " cost

← unit fs. warr.

← development

Vector - denotes FY73, 74, 75, ..., 79.

Multipliers for time (12 month intervals), # (1000 units), \$ (Kilobucks).

The basic form of input is thus:

attribute-name: value₁ value₂ ... value_n

Separator for Basic space, tab, carriage return, or comma

can be blank, [i] if more sets of values to be appended as to new changes, or [c]

In the value list the

← start it, normally should wait till it loads, + is

PLS NAME ATTRIBUTE FILE: ?ATRB
 PLS NAME PRNT/PLOT FORMAT FILE ?REG
 PLS NAME PRNT/PLOT OUTPUT FILE ?LA360
 SHIP DELAY (MONTHS) ?0
 SALES ALTS (FACTORS) ?1
 COST ALTS (FACTORS) ?1
 PRICE ALTS (FACTORS) ?1
 ACCTS REC. TIME (MONTHS): ?3
 WORK IN PROCESS TIME (MONTHS) ?9
 * TCPL ← First (only command) Calc. P&L.
 DIRECT OR INDIRECT FILE (D OR I):
 PLS NAME FILE (OR INDIRECT FILE) TO PROCESS: ?LA36N
 * T C

← name of attributes that this version of prog. needs to know
 specifies which attributes are to be in output format —
 some of the possibilities:
 REG - std DEC.
 FULL - all - about 40.
 EMPTY - none (used when just getting the indicators)
 multipliers of the plan for #; price;
 cost;

Project dly
 Can't have alts

READY
 COPY LA36N TO UNIT:
 31 BOOK: BOKB 'BOOKINGS
 2 #: SHP# 'SHIPMENTS
 13 S S 'SALES (NET)
 12 C X 'COST
 38 M TM 'MANUFACTURING FIXED COSTS TOTAL
 14 F TF 'FIELD SERVICE TOTAL
 37 G MG 'GROSS MARGIN
 15 D TD 'DEVELOPMENT TOTAL
 22 SSTU 'SOFTWARE SUPPORT TOTAL
 23 SATP 'SALES COSTS TOTAL
 11 MKT: M..M 'MARKETING
 19 P.CN 'PRODUCT CONTRIBUTION
 29 %PCZ '% PRODUCT CONTRIBUTION
 36 CAP.EQUIP: C.EX 'CAPITAL EQUIPMENT (INCREMENTAL)
 28 ROIX 'ACTUAL INVESTMENT FOR ROI CALC

 FILE: LA36N PROJECT: LA36 DATED: /50130
 T.DATE: 7407 12 7501 _750130
 P.J.NAME: 7407 12 7407 _LA36
 P.S.AUTHOR: 7207 12 7501 _ED.CORELL
 T.BEGIN: 7207 12 7501 _720700
 T.END: 7207 12 7501 _790700
 T.C: 7207 12 7501 _750306
 *.T: 7207 12 7501 _12
 *.#1: 7207 12 7501 _1000
 *.#2: 7207 12 7501 _1000
 /PRICE: 7207 12 7501 _0_0_1520_1473_1372_1439_1450
 /COST: 7207 12 7501 _0_0_730_667_600_600_600
 MFG.START.UP: 7207 12 7501 _0_0_150000
 /FS.WARR: 7207 12 7501 _0_0_100_100_100_100_100
 HARDW: 7207 12 7501 _336000_1072000_1071000_100000_100000_1000
 00_100000

Input Data, that will not appear in output
 Base output (Result)

ACCTS REC: 3 MONTHS. WORK IN PROCESS: 9 MONTHS.
 SD SA.F CS.F PR.F K# MGR K# PC PCZ RIZ K#DEV D/SZ XOVR
 0 1.0 1.0 1.0 184614 88944 48 83 2879 1.6 74/10

"goodness" Indicator
 total output file
 Case.

Code →

	X	72/07	73/07	74/07	75/07	76/07	77/07	78/07	
BOK									
SHP 1K	0	0	6.6	25	34.5	34.4	28.1	128	
S 1M	0	0	10	36.8	47.4	49.5	40.7	184	
C 1M	0	0	4.81	16.6	20.7	20.6	16.8	79.7	
M.T 1K	0	0	150	0	0	0	0	150	
F T 1K	0	0	659	2500	3455	3444	2812	12872	
G M 1M	0	0	4.4	17.6	23.2	25.4	21	91.8	
D T 1K	336	1072	1071	100	100	100	100	2879	
SST									
SAT									
M..									
P.C 1M	-0.33	-1.07	3.33	17.5	23.1	25.3	20.9	88.9	
XPC	0	0	33.2	47.6	48.7	51.1	51.4	48.1	
C.E 1K	0	0	500	0	0	0	0	500	
ROI 1M	-0.33	-4.68	-8.56	7.8	20.5	27.6	35.8	78.2	

READY
5500
RUNNH

Fig. 3 Examining Some Cases of Plan for Price alts

```

PLS NAME ATTRIBUTE FILE: ?ATRB
PLS NAME PRNT/PLOT FORMAT FILE ?EMPTY
PLS NAME PRNT/PLOT OUTPUT FILE ?TTY
SHIP DELAY (MONTHS) ?0
SALES ALTS (FACTORS) ?1
COST ALTS (FACTORS) ?1
PRICE ALTS (FACTORS) 0.95,1,1.05,1.1,1.2
ACCTS REC. TIME (MONTHS): ?3
WORK IN PROCESS TIME (MONTHS) ?9
* TCPL (calc. P/L).
DIRECT OR INDIRECT FILE (D OR I): ?D
PLS NAME FILE (OR INDIRECT FILE) TO PROCESS: TLA36N
LA36N LA36 DATED 75/130
ACCTS REC: 3 MONTHS, WIP: 9 MONTHS
SD SA.F CS.F FR.F K#F K#NET PC% RIZ K#DEV D/S% XOVR
0 1.0 1.0 1.0 175383 79714 45 75 2879 1.6 7612
0 1.0 1.0 1.0 184614 88944 48 83 2879 1.6 7610
0 1.0 1.0 1.1 193844 98175 50 91 2879 1.5 7609
0 1.0 1.0 1.1 203075 107406 52 99 2879 1.4 7607
0 1.0 1.0 1.2 221537 125867 56 115 2879 1.3 7605
0 1.0 1.0 1.1 195691 100021 50 92 2879 1.5 7608
    
```

no output of P/L

if TTY get results in both a file called TTY, and on output Teletype.

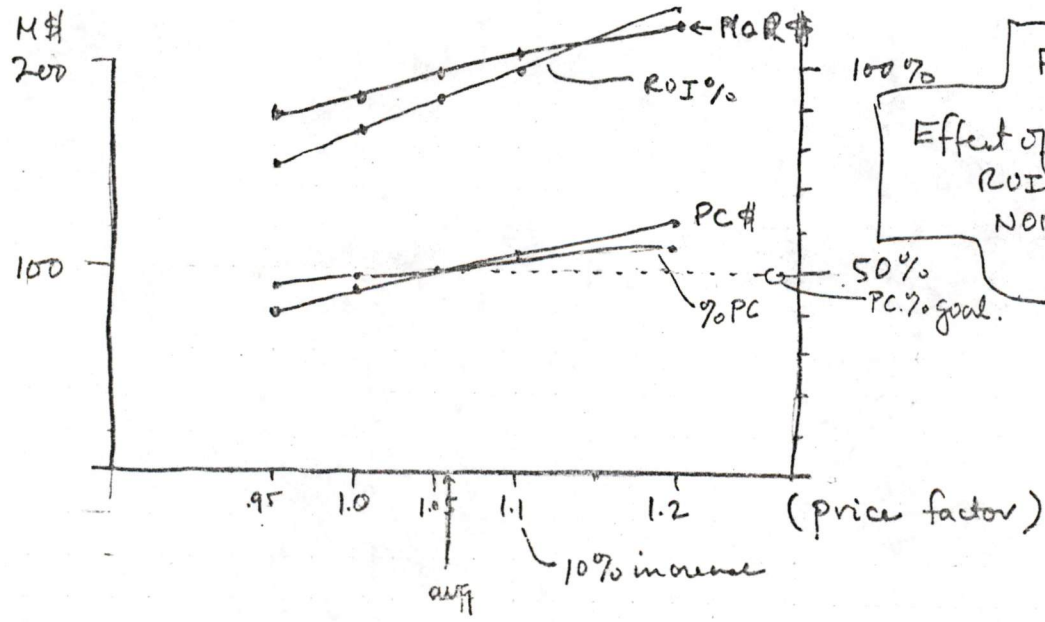
Examine sensitivity to price

File to work on. Div/NOR
crossover date.

alternatives
ENG. GOAL!
avg for all cases

NOR * K# PC * K# ROI % Dev K#

Note Price too low
Assuming nothing happens to Costs!



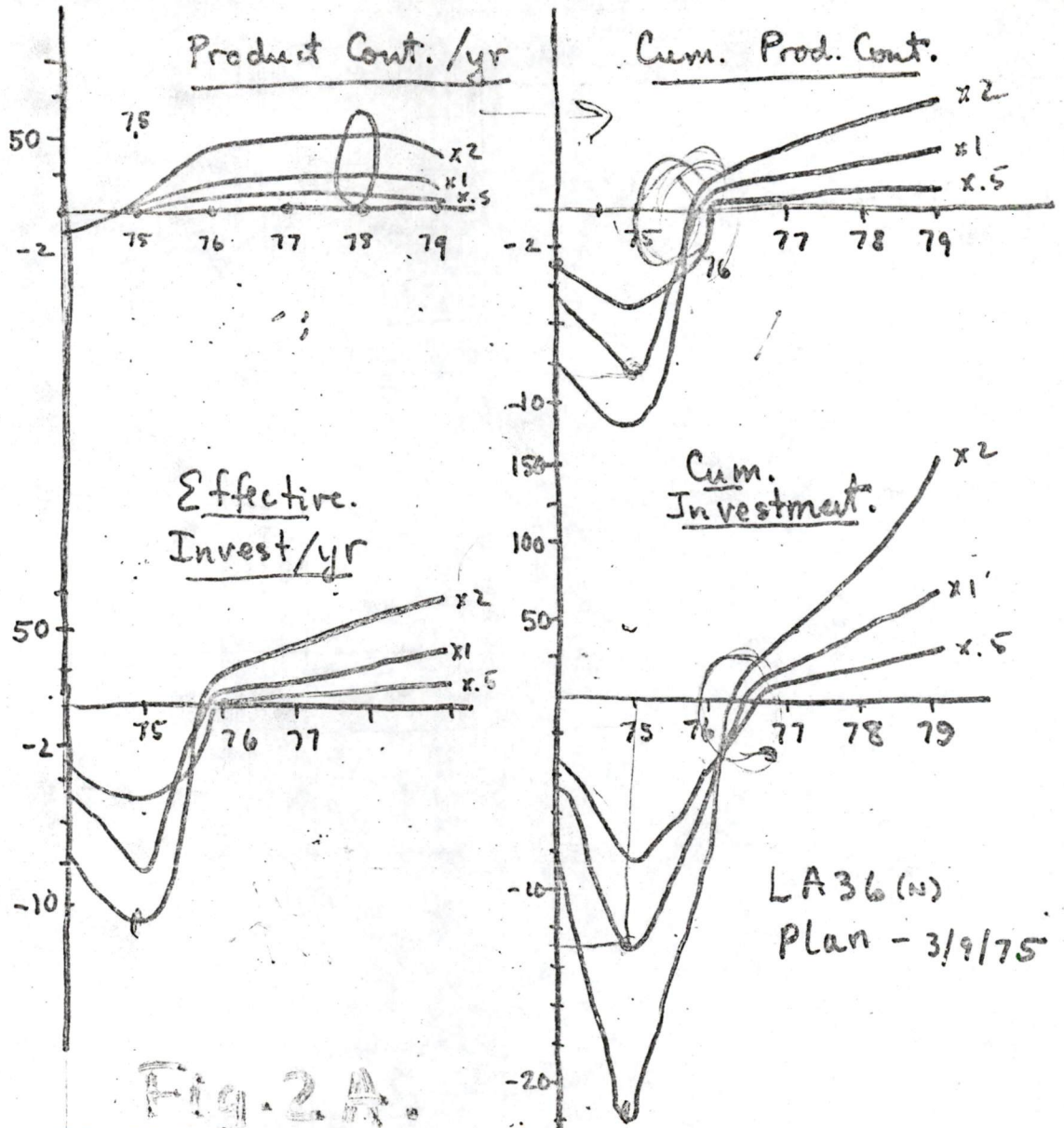


Fig. 2.A.

PC, Cum. PC, Invest, Cum. Invest as Indicators

Use → pricing
project evaluation
plan-format

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Extensions: (Product Mgr. use).

Plotting of:

- roi, pc, Cum roi, Cum pc, etc.
- Sensitivity of indicators to Price, Cost, #, slips, wip.
- demand curves
- Alt. project sets.

Risk analysis

Roll up by systems, + technology with cross checks.

Therapy

Terminals → both LA + VT needed. Prefer VT(05), but LA if 1.

Modems, + Phone System → poor, unreliable

Computer System → reasonably good + helpful.

Being down (eg. scheduled Sat. eve) bad

BASIC → really quite poor.

Encourages poor programming

Not a std, but a name for a home grown lang

Programming → tedious, to do a trivial task.

Interpreters + high quality compilers for a language
are both needed + Spec. Editors for docum.

Interactive design tools → only way to do task.

eg. high payoff for establishing right prices

→ Recommend using the computer ←

Fig. 4. Examining alts of slip (3 months), Sales off x factor of 2, .5, Cost overruns by 15%

* TCAL

SHIP DELAY (MONTHS) ?0,3
 SALES ALTS (FACTORS) ?1,2,.5
 COST ALTS (FACTORS) ?1,1.15
 PRICE ALTS (FACTORS) ?1
 ACCTS REC. TIME (MONTHS): ?3
 WORK IN PROCESS TIME (MONTHS) ?9

Command to request more alts. 1267
 Delay
 Exam. vol. sensitivity
 Cost overrun

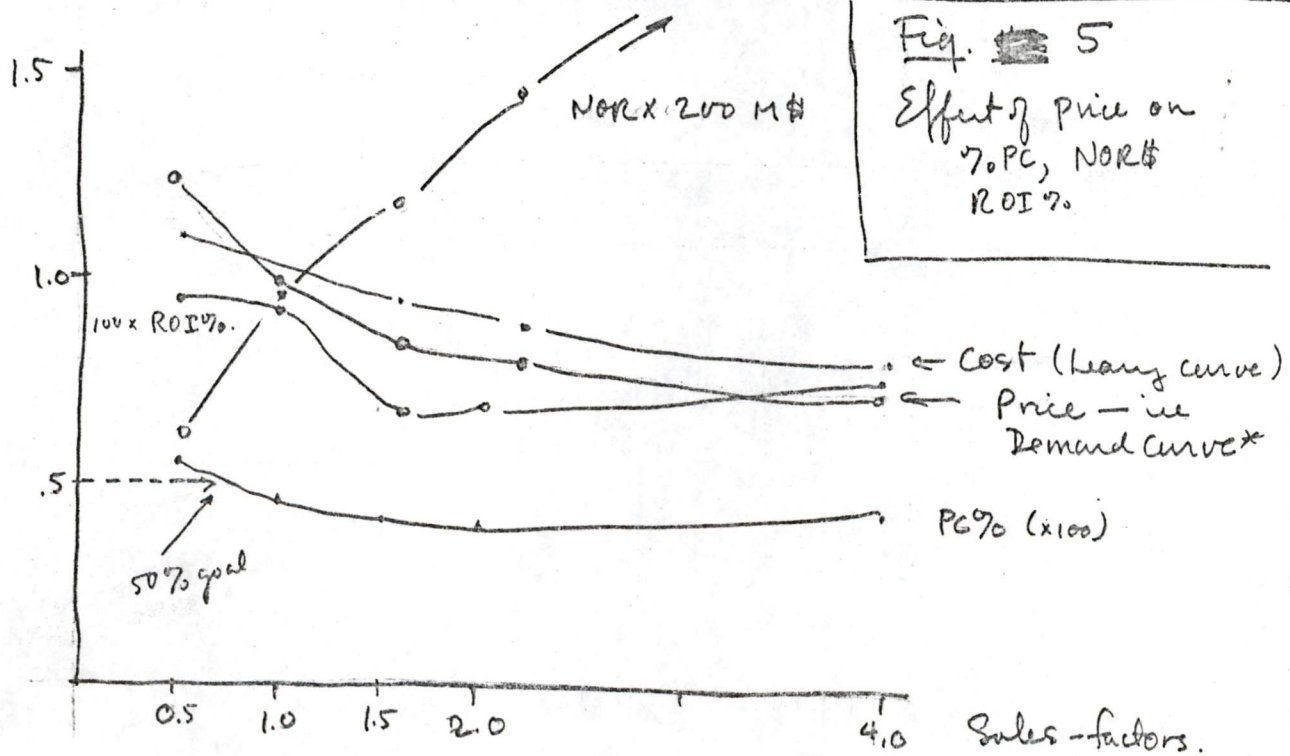
* TCPL

DIRECT OR INDIRECT FILE (D OR I): ?D
 PLS NAME FILE (OR INDIRECT FILE) TO PROCESS: ?LA36N
 LA36N _LA36 DATED_750130
 ACCTS REC: 3 MONTHS, WIP: 9 MONTHS

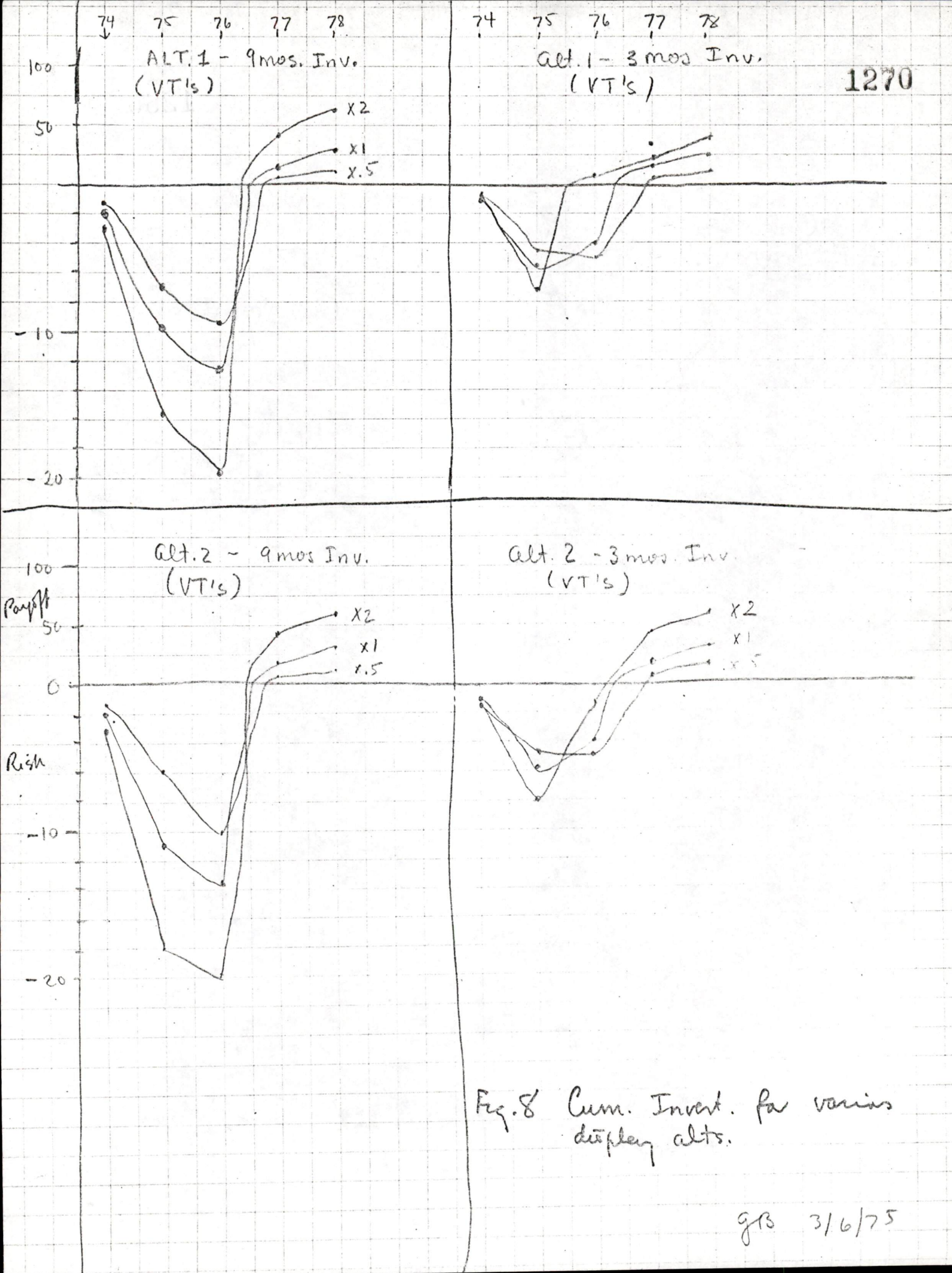
SD	SA.F	CS.F	PR.F	K\$PC	K\$NET	PC%	RIZ	K\$DEV	D/SZ	XOVR
0	1.0	1.0	1.0	184614	88944	48	83	2879	1.6	7610
0	1.0	1.2	1.0	184614	76979	41	63	2879	1.6	7702
0	2.0	1.0	1.0	369228	180918	48	91	2879	0.8	7609
0	2.0	1.2	1.0	369228	156988	42	71	2879	0.8	7701
0	0.5	1.0	1.0	92307	42957	46	69	2879	3.1	7612
0	0.5	1.2	1.0	92307	36975	40	53	2879	3.1	7705
3	1.0	1.0	1.0	174383	84055	48	79	2981	1.7	7612
3	1.0	1.2	1.0	174383	72801	41	63	2981	1.7	7705
3	2.0	1.0	1.0	348767	171243	49	91	2981	0.9	7611
3	2.0	1.2	1.0	348767	148735	42	69	2981	0.9	7704
3	0.5	1.0	1.0	87191	40462	46	65	2981	3.4	7702
3	0.5	1.2	1.0	87191	34835	39	51	2981	3.4	7707
1	1.2	1.1	1.0	209415	94658	44	70	2930	1.9	7665

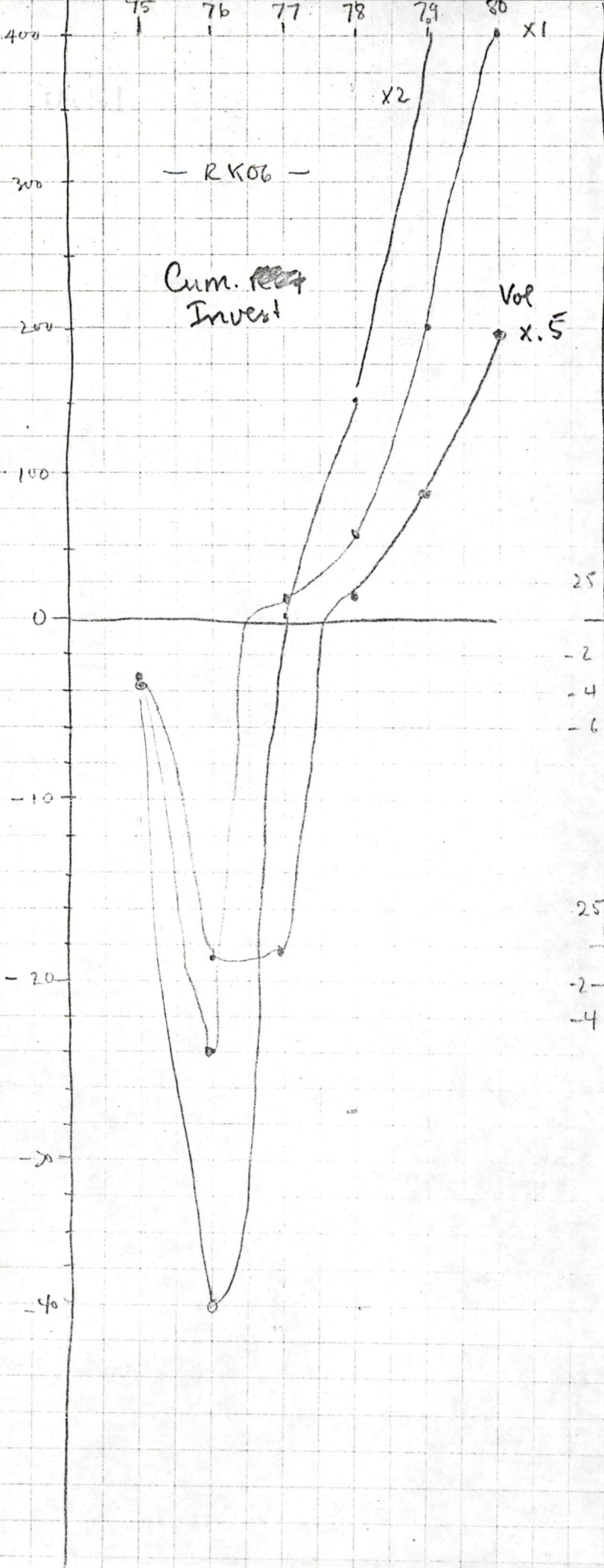
assum no slips, there is no volume to make 50% PC goal!

avg. of cases.



- Demand Curve assumes doubling of volume occurs for a 25% price decrease.
- Cost Curve - assumes 10% heavy i.e. 10% decrease in cost with doubling volume.





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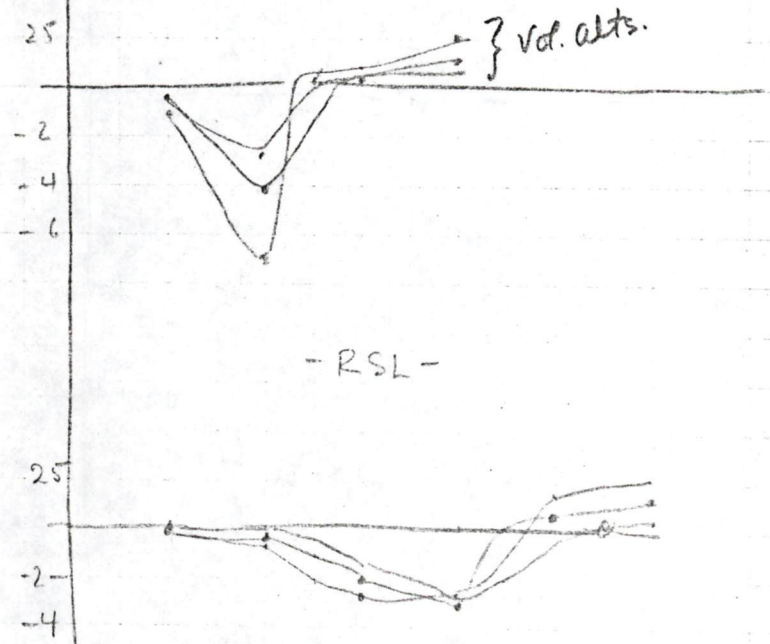


Fig. 7 Disks Cum. Invest
 9/3 3/6/75

Table 1.

Name	Dev.	Sales		Product		PC	ROI	Dev % of Sales	Notes
		Dollars	Millions	Contri- bution	Millions				
<u>Peripherals & Terminals</u>									
RK06	9.7	619.0	1	478.0	1	77	127	1.6	1 - 77/06
LA36	2.9	184.6	2	88.9	2	48	83	1.6	1 - 76/10
Displays (2) (9 mos. inv.)	7.2	70.1	3	30.7	3	43	67	10.3	3 - 76/12
Displays (1) (9 mos. inv.)	6.5	61.1	4	26.6	4	43	65	10.6	4 - "
RX01	.45	27.7	5	17.2	5	62	119	1.6	1 - 74/08
LA180	1.1	26.9	6	13.7	6	50	67	3.9	2 - 77/09
RSL	3.1	22.0	7	12.3	7	57	79	14.0	5 - 78/06
								4.7%	(Central Eng.)
								9.6%	(Eng.)

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SUBJ: DOUBLE BUFFERING OF THE FLOPPY

To: Distribution

In suggesting and encouraging a non-DMA transfer device for the RX01, I did not endorse running the device at 1/2 its capacity by having only 1 buffer (2 was the suggestion). For low performance devices, we shouldn't arbitrarily limit them by saving \$4-6. The incremental cost/performance increase is $\$6/2=3$ for large block transfers.

The marketing culture, which expects DMA for disks, may respond to the RX01 by its price; but by limiting it and not using a double (swinging) buffer, they have a hard time accepting DMA. Mary Ellen Corey has suggested a DMA interface for LSI-11. It's not clear she's worked the numbers, i.e. a program transfer takes up about 15 microsec./word or at 36 microsec./word transfer, 42% of the LSI-11 running at full speed--or a few percent in use after considering the seek time. This is probably less than LSI-11 loses on memory refresh. Also, a microcode block transfer would help. We can get floppy to transfer at full speed? Are there any options? Is it too late?

GB:mik

Distribution

Bob Peyton, Chuck Youse

cc: Bob Bean, Mary Ellen Corey, Bob Puffer, Steve Teicher



INTEROFFICE MEMORANDUM

TO: Bob Puffer
Grant Saviers

LOC/MAIL STOP
ML1/E38
ML1/E58

DATE: March 18, 1975
FROM: Gordon Bell
DEPT: OOD
EXT: 2236
LOC/MAIL STOP: ML12/A51

CC: Bill Long
Mike Tomasic
John Holman

PK3/A60
PK3/M12
PK1

SUBJ: Diabolo 5 Megabyte Disk from Xerox

It is my understanding that we just booked an order from Xerox for a CSS controller for the above disk. Can it be done with sufficient quality, clarity, etc., such that it could be a back-up to something we're doing? (Is it too little, too late to back-up anything?)

/ale

SUBJ: PRICE POSITION

DATE:
FROM:PAGE 1
03-18-75
GORDON BELL

* * * * *
 PLEASESEND TO: FILE
 * * * * *

SUBJ: PERSPECTIVE ON OUR PRICE POSITION IN THE MARKETPLACE/
 MACHINE OVERLAP

To: Competitive Specialists for MODCOMP, HP, DG, INTERDATA
 and Bob Curtis (Jack Courtemanche, Ned Somerville,
 Ivan Tanner)

cc: Dick Clayton, John Fisher, Phil Laut, Larry Wade

I am uncomfortable with our ability to focus on each of the competitors. We may be working too well to optimize a set of machines across a price and performance range, and the competitors are moving into cover all the holes effectively. Also, while we have many machines, I don't believe the number is unreasonable for the range.

For each competitor, and each machine, I would like the rough data (by March 21):

Unit Price:

Price/extra memory:

Price range: min-avg-max

Time first ship:

Rough performance: fxd, flt (nearest DEC model or

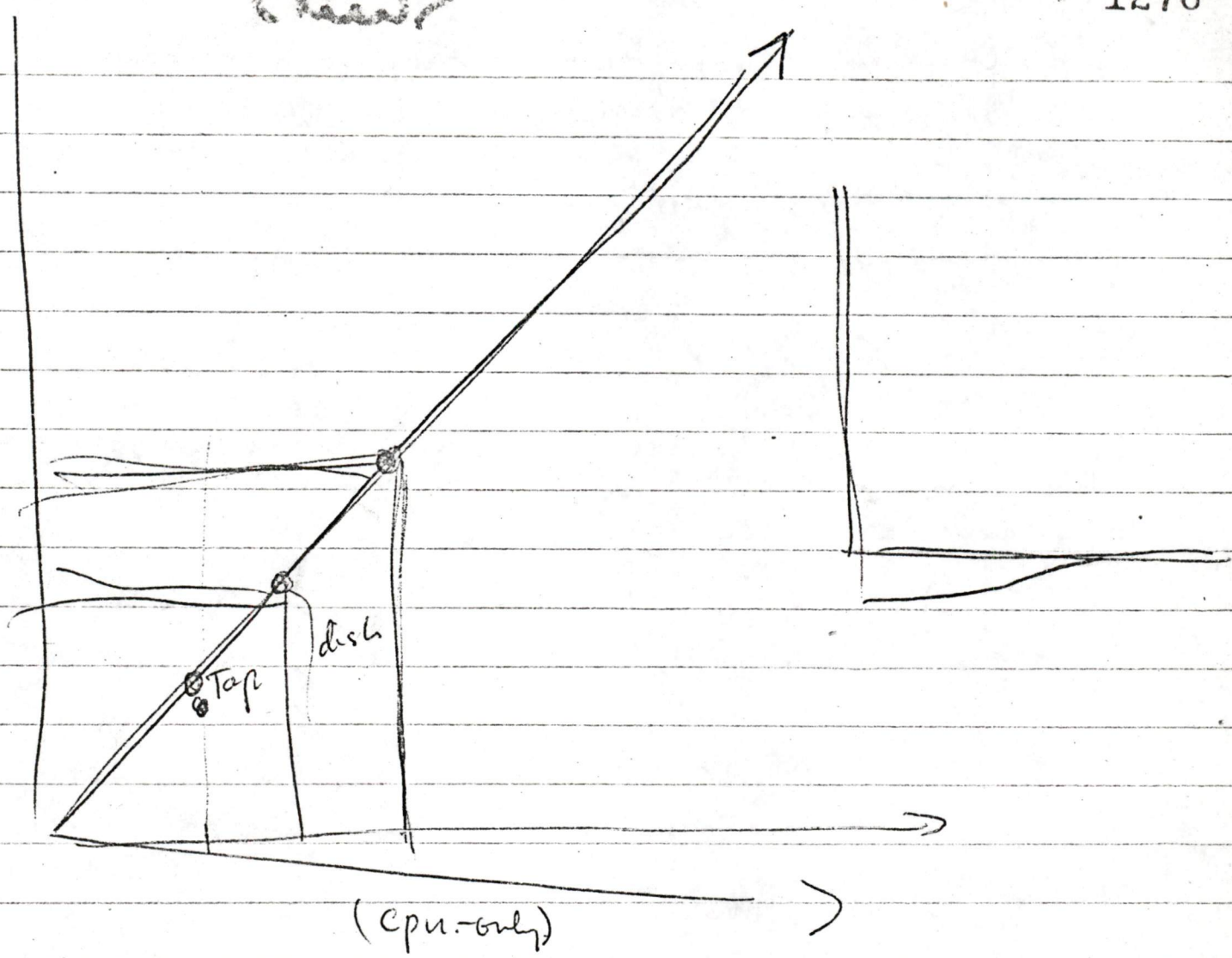
In terms of our models)

For HP, I'd like to include their programmable calculator down to the one that sells for \$795.

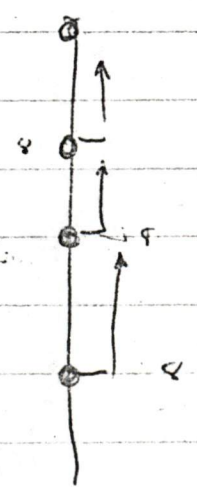
The attached 2 line graphs, give an indication of the means of the attack for the comparison; namely, I want to get at the breadth of time and size of holes to see how we are going to succeed.

What's your (low) term
(think?)

When
we
Speed

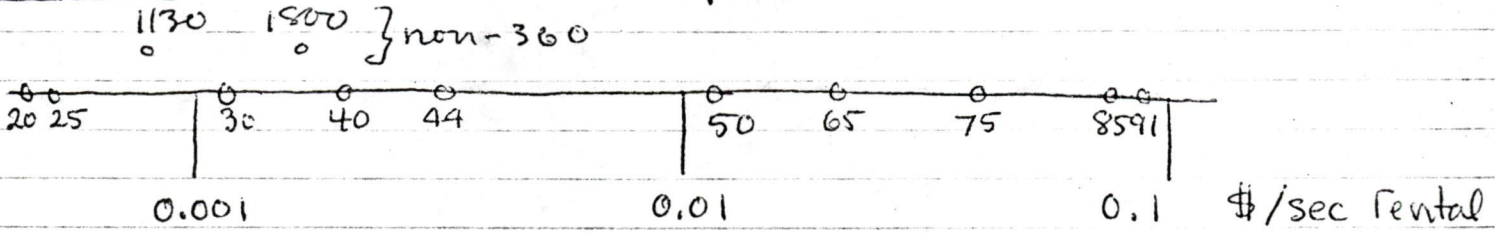


When we're lazy



A Comparison of Machine Families in Terms of Cost and Performance Ranges.

IBM 360 Models in 1971-72 prior to 370.



Does not include: System 2,3,6,10 and System 7 series.

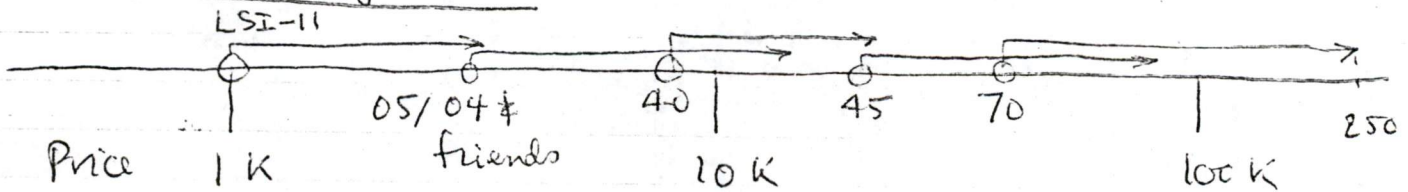
10 machines cover price range of 250
 " " " perf " " 314.

Thus $\sqrt[3]{250} \approx 2$ (each machine covers a price range of only 2.)

If we ignore 25, 85, and 44 (not part of 360 series initially - but included to respond to competition)

We get: 7 machines over 250 w
 $\sqrt[6]{250} = 2.5$ price/machine,

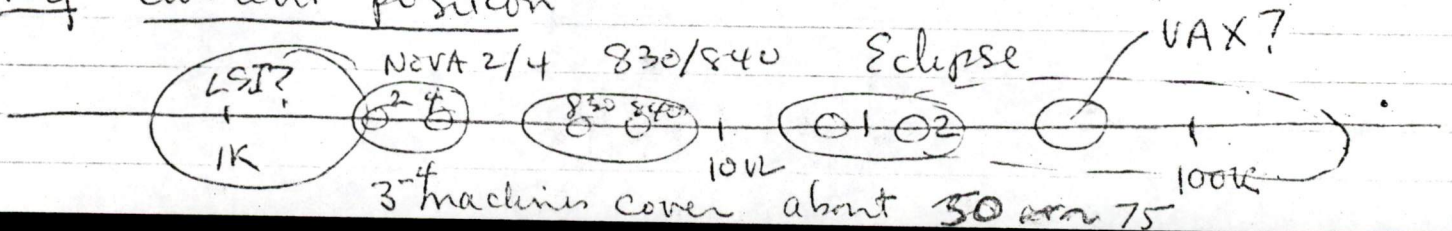
DEC Models of PDP-11 (~1975)



5 machines cover a range of $\sim (200 \sim 250)$
 " " " perf " " 5 ~ 100 (depends on mix)

$\sqrt[5]{200} \approx 2.9$ Price factor cover/machine

Pq Current position



SUBJ: 11/85

DATE:
FROM:

PAGE 1
03-27-75
GORDON BELL

* * * * *
PLEASESEND TO: FILE
* * * * *

SUBJ: UNDERSTANDING THE 11/85 (TOPS 10 OR SNARK) VIA USING IT

To: distribution

OOD is meeting with the Product Lines regarding development strategy. I feel you have the opportunity to sell Business Products on the 10, but it is probably best through use.

They require RSTS at the high end (i.e. new BASIC 10), COBOL-- you have one with full capabilities and debugging, RPG to bring people over from IBM, Dibel to move up, including their applications, and a DBMS of some type.

They also would like to offer some amount of word processing, which you have much of already, both using typewriters and scopes.

Computing with (using) the 10 is important to selling it. How about some terminals?

GB:mjk

Distribution

-
- Al Avery
- Bruce Delagi
- Roger Gourd
- John Leng

cc: Dick Clayton, Irwin Jacobs, Larry Portner

SUBJ: VT20R/ VT50

DATE:
FROM:

PAGE 1
03-27-75
GORDON BELL

* * * * *
PLEASESEND TO: FILE
* * * * *

SUBJ: VT20R, SCAN GRAPHICS, VT50

To: Distribution

We really have to work on the terminals strategy, I just learned of another, the VT20R for typeset, also using the LSI-11. We were, in part, proceeding with the VT51 for being programmable for typesetting,

Can we put 3-15 minute, information only, items on the PC agenda?

GB:mjk

Distribution

Products Committee
Ed Corell, Win Hindle, Bob Lane
Julius Marcus, Bill McBride, Stan Olsen,
Tom Stockebrand, Len Hallö

CC: Ken Olsen

digital

INTEROFFICE MEMORANDUM

TO:

DATE: March 28, 1975

FROM: Gordon Bell

DEPT: 00D

EXT: 2236 LOC: ML12/A51

SUBJ: FAMILY TREE/DEVELOPMENT HISTORY

As a hobby, I'm putting together some family trees of all our computer systems. These will be used for us to all gain more insight into the development process and it will be exhibited in the museum. Some sketches are attached, but I need more (better) and correct information for all machines or models. Could you give me as much key information as you remember about the project:

- First paper on project proposal
- Project start (put several dates if it isn't clear).
- Announce
- First operational
- First ship
- Volume ship
- Withdrawn (traditionalized)
- Price at minimal (unit price)--specify configuration + average + maximum.
- Relatedness to other machines (compatibility of instruction set/I-0)
- Key people
- Goals
- Other
- Where files are kept on the project

I'm using Jack Smith's data for quarter ship volumes, but need better breakout on models. Jack can you send me the detailed sheets here?

GB:mjk

cc: Jack Smith

digital

128+

INTEROFFICE MEMORANDUM

TO: John Clarke (PDP-5...8)

DATE: March 28, 1975

digital

INTEROFFICE MEMORANDUM

TO: Dick Clayton (LINC...12; PDP-11)

DATE: March 28, 1975

digital

INTEROFFICE MEMORANDUM

TO: Dick Devlin (PDP-4...15)

DATE: March 28, 1975

digital

INTEROFFICE MEMORANDUM

TO: Alan Kotok (PDP-6...10)

DATE: March 28, 1975

digital

INTEROFFICE MEMORANDUM

TO: Roger Cady (11/20, 40)
Jim O'Loughlin

DATE: March 28, 1975

Bruce Delagi (11/45)
Steve Teicher (05,04, LSI-11)
Bill Demmer (11/70)

FROM: Gordon Bell

DEPT: 00D

EXT: 2236 LOC: ML12/A51

digital

INTEROFFICE MEMORANDUM

TO: Roy Moffa (MPS)

DATE: March 28, 1975

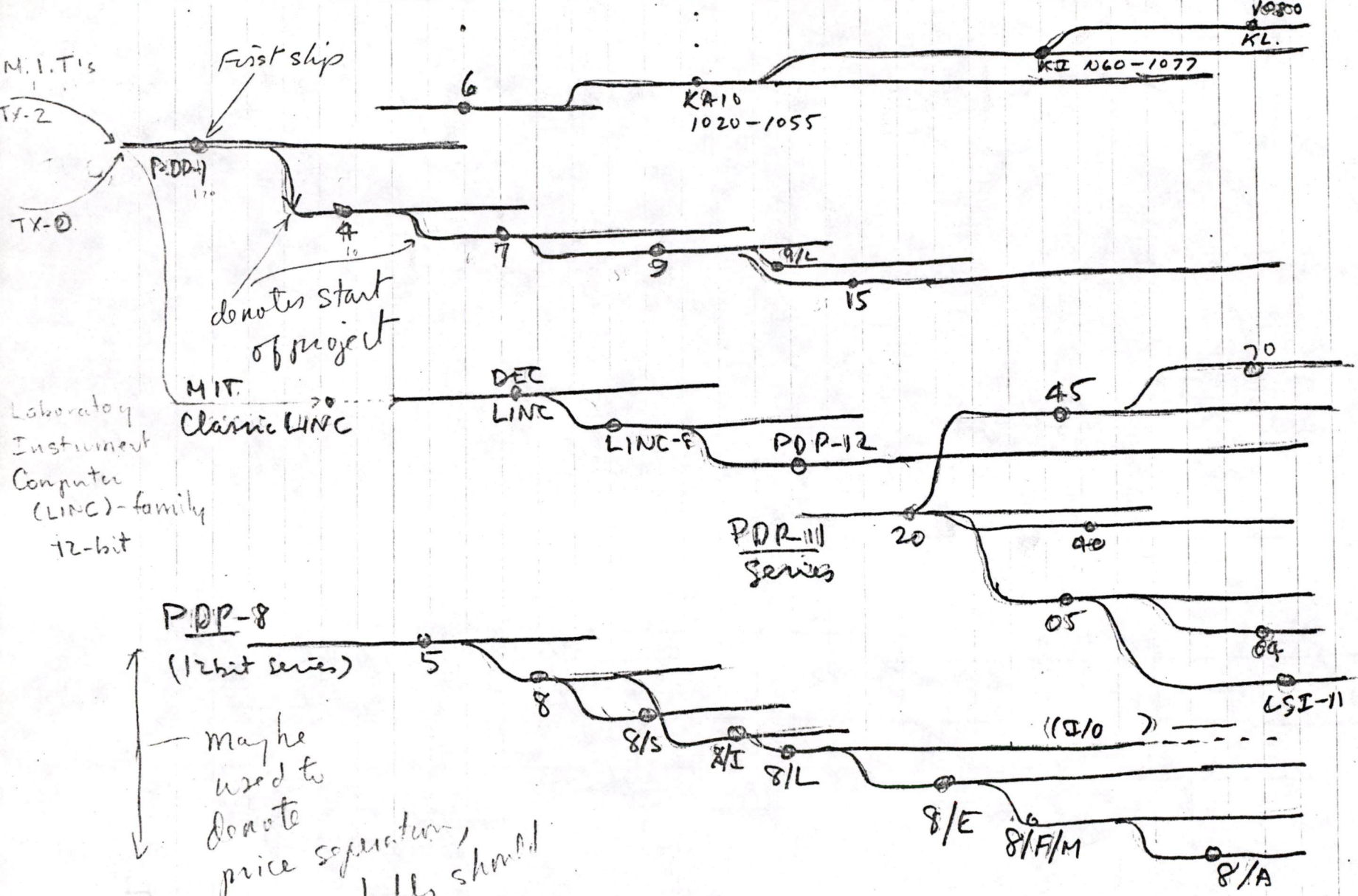
FROM: Gordon Bell

DEPT: 00D

EXT: 2236 LOC: ML12/A51

SUBJ: FAMILY TREE/DEVELOPMENT HISTORY

60 62 64 66 68 70 72 74 76



Maybe used to denote price separation, but probably should be used to denote functional/physical separation in a taxonomic sense.

1285

169

170

171

172

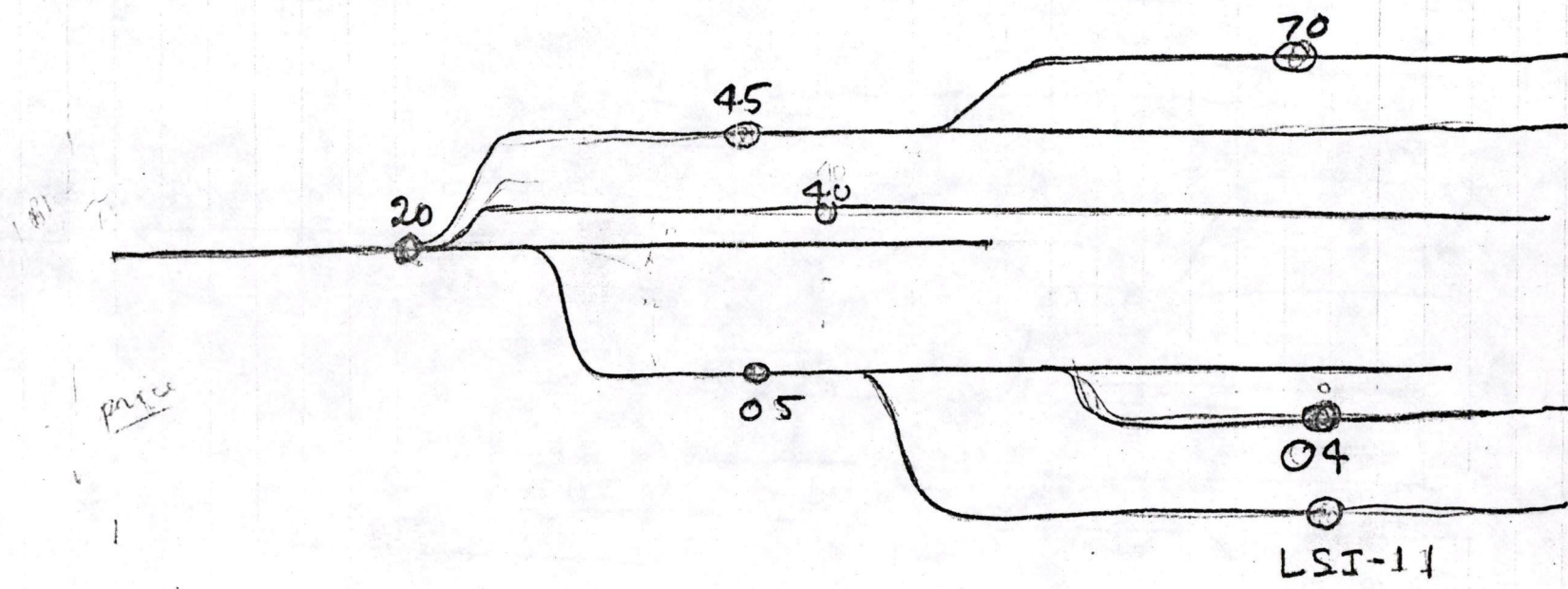
173

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177

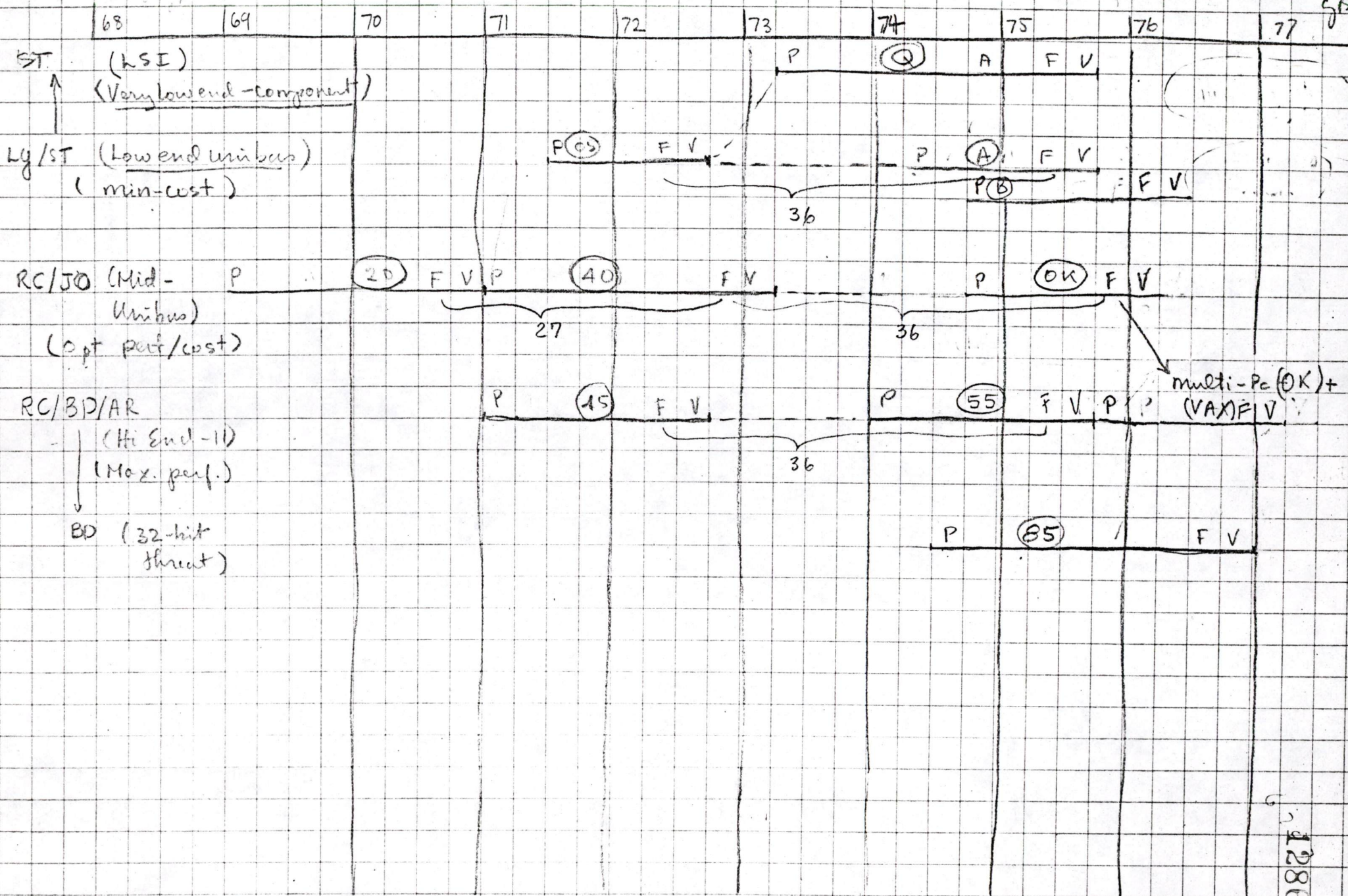


JB
Mar 15, 1978

Non-8, 15 Minis + Midi's - Resource Allocation.

Nov 3, 74 SB

CY	68	69	70	71	72	73	74	75	76	77	
L S I	ST (Min-cost)	Q					P	A	F V		
Sub- Unit							30/				
S M R I I II	LG/ST/RK05 (Min-cost) A-04 B				P	A? F V 15/48		P	A	F V 18 21	W?
M I d - II	RC/JO 20 (optimum) 40 PDQ n P PDQ+ VAX		P	A?	F V		W				
				24/39	P	A?	F V				W?
				↑ t.eng			30/45		P	F V	
				↑ t.ship						P	F V
L a r g e II	RC/SD/WD 45 (Hi. perf.) 55				P	A	F V				W?
						21/54		P	A	F V	
							21/				
36	BD 85 (Hi Perf.)							P		F V	
									30/		
				x			x x x		x x x	x x x	x
Eng		1 1 1 1	1 1 1 1	2 2 3 3	3 3 3 1	1 1 1 1	2 3 4 6	6 6 6 3	3 2 1 1		
Mkt/Sales		1 1 1 1	1 1 1 2	3 4 4 4	4 4 4 3	3 3 3 6	6 8 8 8	8 7 6 5			
Produced		1 1 1 1	1 1 1 1	3 3 4 4	4 4 4 3	3 3 3 3	3 6 6 6	8 7 7 6	6 6 6		

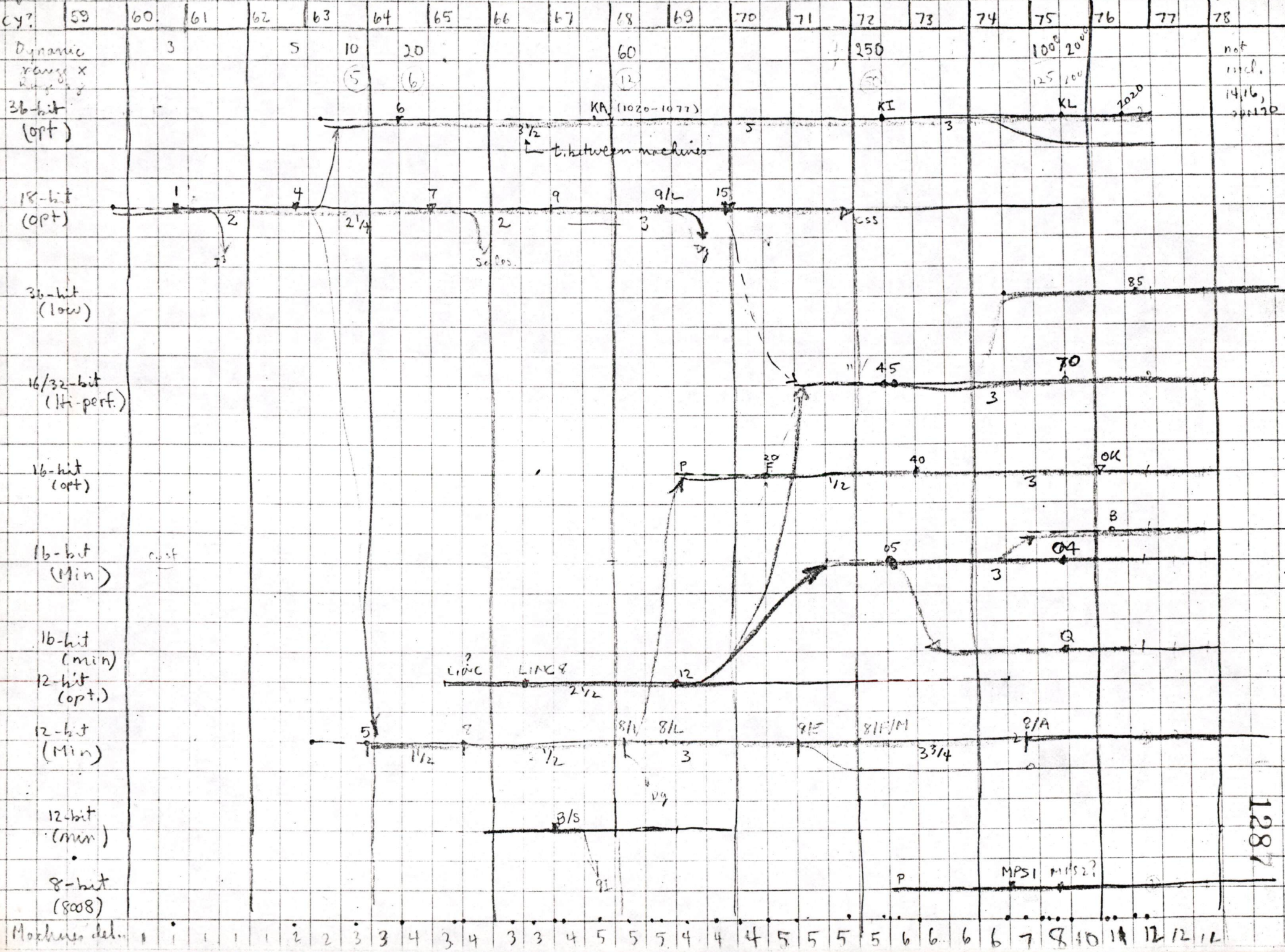


1286

gfb

Group 5

98 11/10/70



digital

INTEROFFICE MEMORANDUM

TO: 00D

DATE: March 25, 1975

FROM: Gordon Bell

DEPT: 00D

EXT: 2236 LOC: ML12/A51

SUBJ: 00D STAFF MEETING AGENDA--March 27, 1975

12:30 Lunch	Field Service Communications	Shields
2:00	Responsibility for Design, Fabrication, and Testing at the systems level	Clayton/Smith/Cudmore
3:00	Brad Vachon (Woods Meeting)	

NOTE: NO STAFF MEETING APRIL 17!!

FUTURE AGENDA ITEMS

<u>Date</u>	<u>Topic</u>	<u>Responsible</u>
4/3	DEC Safety Standard	Mondani/Minezzi
4/3	Operating Systems	00D
4/3	Development Managers Committee Meetings	00D
4/3	Yellow book--a monster?	00D
4/24	EEO Position	John Sims
5/1	Engineering Process	Best
?	2x2 Report	Puffer
Q4	Production Communications	Smith/Cudmore

GB:mjk

SUBJ: PC.ISP COMPATIBILITY

DATE:
FROM:PAGE 1
03-31-75
GORDON BELL

* * * * *
 PLEASESEND TO: FILE
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SUBJ: Pc,ISP COMPATIBILITY INVESTMENT ANALYSIS BASED ON
 DEC SOFTWARE

To: Peter Christy

CC: Bob Bean, Denny Pavlock, VAXC

In getting a handle on cost to convert (upgrade) to an extended PDP-11, we need to get a better definition of this dimension. This seems best done by assuming one, and using it.

(Would you please attempt to analyze the investment using this definition. Modify, if necessary, interacting with Richy, me, VAXA, etc.)

MODEL

 Figure 1 shows the general operational notion of machines consisting of hardware, operating system(s), and languages. At each level, a machine exists which may be well defined by the previous level, or several lower levels (e.g. in 11/D privileged VM).

MACHINES WE SUPPORT AND THE PROBLEM OF POORLY DEFINED INTERFACES

 We support a fairly large number of machines ranging from many hardware models to languages. In trying to extend the 11 architecture, we need to provide a higher level interface that supports the notion of a process. However, it is not clear that many of our multiple operating systems have a very well defined interface. Instead operating systems have "holes" to allow direct access to particular I/O and other hardware features. Hence, each combination of machine X operating system provides another machine which constrains compatibility. I believe we must develop a well-defined interface (e.g. 11/D VM) that all languages, utilities, special applications use. In this way, we can modify, evolve, change, etc. any lower level without affecting our investment in a higher level software.

SUBJ: PC.ISP COMPATIBILITY

DATE:
FROM:PAGE 2
03-31-75
GORDON BELL

It is the task of Richy Lary to design this interface in such a way that software can be transported as we develop new machines and operating systems throughout the next 5 years.

Table 1 attempts to define the various hardware, software, languages machines we support. Note, the relatively large number--say, in contrast to PDP-10 which is 1 software, going on 2. There are 2 hardware machines going on 3. Richy is getting this in a better operational state, as a basis for definition of the next 11.

WHAT WILL THE 11 EXTENDED USER MACHINE BE?

If Table 1 is correct, we probably should provide the ability to create user interfaces like the current 11/VM. We can also, by software, provide multiple 11/20 virtual machines; in contrast, it is probably less useful to provide multiple 11/70 VM's, except for development of monitors. As we extend the address space, we automatically get an 11/VAX user machine interface. To get better performance and be competitive, we must place more operating system capability in hardware. This implies that we cannot support the plethora of interfaces we're used to.

The task of VAXA is to define this hardware interface together with the software interface.

SOFTWARE INVESTMENT AS A KEY DESIGN CRITERIA OF THE INTERFACE

The interface we provide in subsequent machines should be a tradeoff of: permitting as much user-level software to run, versus taking advantage of new capabilities that might be provided (e.g. Recursive Virtual Machines).

For the machines in Table 1, would you?

1. Quickly ascertain that these are the machines we should consider.
2. Enumerate the programs by type, name, quantity, and general quality for each machine. This would include: diagnostics, operating systems, operating system specific handlers (e.g. COMTEX), VM-level (e.g. FORTRAN IV+), and language specific applications (e.g. DIBOL Machine: Accounts Receivable Package).
3. Estimate the code (in %) investment that our users have.

1291

SUBJ: PC.ISP COMPATIBILITY

DATE:
FROM:

PAGE 3
03-31-75
GORDON BELL

This will enable us to: first, find out what the machines really are; second, evaluate the investment we have; and finally, estimate the investment of our users,

GB:mjk

Attachments (2)

Application task (eg. Cogo).

User task structure (eg. Fortran)

Extended Op Sys (eg. IAS)

Operating System eg. I1/D

Pc + Kio Options

Basic II
C :=
(Pc + Mp)
(eg. I1/70)

Pu

resource (i/o, Mp)

i/o interface

I1/D interface

Hardware provided machine

non-privileged user interface

Privileged user interface (Direct i/o control)

"Hob" to provide direct access to more inner machine.

Note each level provides a particular machine with generally increasing capability

Fig. Ring representation of I1 Machines (specific instance).

	Machine	Provides	Built-on.	Provision in -nexted.
Hardware	11/User Mode	32 K Protected in 8-64~8k byte Segs.	11's ^ - (04,05,20). (KT)	Yes, Segs $\geq 2^{10}$ B
	11/VAX User.	22 ²⁴ K protected.	all fut. except LSI-11, PDQ	Main interface
	11/20	11/20 hardware. 28K + 4K i/o page, Interrupts.	All 11's	Buildable w/ software (Useful)
	11/40KT	11/20; 124K phys + 4K i/o mappable onto 11/u.m.	40/A40 (BOS)	↑
Hardware	11/45KT	11/40KT + Kernel + Supervisor Machines (x11/u.m.); I+D-space; Default traps for Segs.	45	not provided in hdw. (Probably)
	11/70KT	11/45KT + Unibus map into 22-bit physical Memory		not useful in software.
	11/D Priv. VM	11/uM w i/o page mapped into mem. space	40KT? ; " " " "	? - Can do except for 32 word i/o.
Software	11/D VM	11/uM + D-ops + S/M-ops	11/uM	↑
	11/S/M VM	11/uM + S/M-ops	11/uM	main interface
	IAS VM	11/uM + IAS + D-ops	11/uM.	↓
	KT VM	11/uM + RT-ops + 11/20?	?	redefine as
	DOS	?	?	Buildable
Sys.	RSTS (Int.)	?	?	Redefine as 11/D VM
	Mumps	?	?	?
	RSTS (Ext)	BASIC+, Files	RSTS (Int.)	?
Lang.	Mumps. (Ext.)	MUMPS Lang, FILES.	MUMPS (Int.)	?

Table 1. 11-FAMILY MACHINES AND WHAT THEY PROVIDE - 98 3/30/75

1293

1294

SUBJ: COS.PERFORMANCE

DATE:
FROM:

PAGE 1
03-31-75
GORDON BELL

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PLEASESEND TO: FILE
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SUBJ: Cos.performance CHARACTERIZING THE PERFORMANCE OF
RSX11/M, D, RSTS, TOPS 10, and VIROS COMPONENTS

To: Rollins Turner, Peter Christy, Larry Wade

CC: VAXA

In trying to understand the kinds of modifications we might make to the 11 in terms of instruction-set, structure, implementation(s), operating system, etc., we need to know something about the nature of monitors (operating systems), and specifically their performance. It is difficult to completely characterize and model them, but we do need a model in order to go after, and hopefully get, a significant improvement. Can you characterize these in terms of capability, size, residency, and performance values for various components?

This should be both from a user's viewpoint, and an internal structure.

For example, what file structures are supported, what is mapping on files, and what is the performance (in accesses), and in time for various disks? What terminal modes are supported, what is maximum rate and what is cost (time)?

GB:mjk

1295

digital

April 4, 1975

Maarten van Swaay
Director of Instrumentation
Department of Chemistry
Kansas State University
Willard Hall
Manhattan, Kansas 66506

Dear Mr. van Swaay:

I am sorry that we have caused you this inconvenience. I have asked John Clarke, Engineering Manager for PDP-8, to incorporate this change in our manuals.

Thank you for your consideration of us and others with the same potential problem.

Sincerely,

Gordon Bell

Gordon Bell
Vice President
Office of Development

GB:mjk

cc: John Clarke



KANSAS STATE UNIVERSITY

John please respond for if working PDP-8 I have manager of 1296

Department of Chemistry
Willard Hall
Manhattan, Kansas 66506
Phone: 913 532-6665

*Dear -
So I am sorry that we
have caused you this inconvenience
I have asked John Clark, evening ~~manager~~
to incorporate this change
to other manuals &*

March 27, 1975

Mr. Gordon Bell
Vice President of Engineering
Digital Equipment Corp.
Maynard, Mass. 01754

*Thank you for your
consideration of us and others
with the same
potential problem.*

APR 01 1975

Dear Mr. Bell:

After many frustrating days I have finally satisfied myself that the CLEAR key and the CAF instruction on our PDP/8-E with lab peripherals clears all flags and interrupt enabling registers, with one important exception: the interrupt request from the M8650 receiver and transmitter channels are both enabled by CLEAR and CAF.

I have thoroughly read and re-read much of the documentation accessible to most users: Introduction to Programming
Small Computer Handbook LAB/8-E Users Handbook
LAB/8-E Maintenance Manual
OS/8 Handbook

In none of these did I find a single reference to the important difference between the teletype interface and most other peripherals. The only references I finally uncovered are the print set (hardly considered normal reading for a programmer) and a single sentence buried in the processor maintenance manual (volume 1, p. 3-171). May I suggest that future versions of the M8650 module be made more consistent with other peripherals, or that the difference be explicitly stated in such documents as Small Computer Handbook and Introduction to Programming?

The need for more explicit information is clearly illustrated by the fact that a letter and numerous phone conversations with DEC personnel failed to yield an answer to my questions on unexpected interrupts.

Yours sincerely,

Maarten van Swaay

Maarten van Swaay
Director of Instrumentation

MvS/nhh

cc: John Davies
Kansas City

SUBJ: OOD MINUTES

PAGE 1
DATE: 04-07-75
FROM: GORDON BELL
EX: X2236
MS: ML12-1/A51

* * * * *
TO: FILE
* * * * *

SUBJ: OOD STAFF MEETING MINUTES--April 3, 1975

To: Distribution

1. Format/purpose of OOD staff meetings.

Gordon was asked to report back with a written statement as to what he expects of the staff meeting. It was suggested that the purpose of the staff meeting is to work budget issues, intergroup issues (manufacturing, field service, software support, sales, marketing, etc.), The meetings with the product lines last week would be counted as staff meeting "time". Various other issues include miscellaneous general policies, administrative issues (such as, the COOP program and employment, review of workshops, and the general notion of the engineering process), Also at this time Gordon would report on Operations Committee and we would review details of workshops (e.g, product managers, engineering managers).

Also it is a time that Gordon uses to raise issues that should be reviewed by everybody (e.g, the board shop, the lack of commonality in our packaging directions... Dick's packaging hobbies versus Bob's Corporate Packaging). It should also be a time where issues will be uncovered and reviewed, and the committee would be used as a body to look at each specific area.

Gordon will defer an official staff meeting charter until he gets through with the corporate 32-bit question. Meanwhile the meeting will be rescheduled to be 10:30 to 12:30 on Thursday (this will start April 24 with Henry in attendance and Julius as of May 1). It was generally felt that an OOD Jungle (Woods) meeting was worthwhile. Will hold one on a quarterly basis, and the responsibility will be distributed on an alphabetical basis (Dick is responsible for the logistics of the next Jungle meeting).

As a means to improve efficiency, Gordon will appoint a secretary who will help with agenda, write-up minutes, and serve as Chairman in his absence. For the next few months, Dick will be the secretary.

DIGITAL

INTEROFFICE MEMORANDUM

SUBJ: OOD MINUTES

PAGE 2
04-07-75
FROM: GORDON BELL
EX: X2236
MS: ML12-1/A51

2. Vince Bastiani will work with Dick to formulate the policy and document the previous UART case, and also to look at this particular chip on a cost benefit analysis; including the alternatives as to whether we hold a proprietary chip or whether we help get a public chip.
3. LA36 RFI problem is under control, but Bob will come back with a proposal on how we are going to coordinate the whole business of safety, RFI, EMI, and various standards (e.g. UL, CSA, VDE, and European countries) proposal. He will get with Jim Cudmore to try to figure out how we are going to get at this thing.
4. Larry presented his organization, and we discussed the ramifications. That in turn created a discussion of better integration between hardware and software systems. Larry and Dick will discuss how communications can be better integrated into our products. For now, Nat has been assigned the problem of Communications product planning. He needs someone else, and it has been suggested that Tony Lauck perform this integration role. Bob and Gordon are going to meet with Stan regarding the integration of displays and LA terminals.

Distribution

OOD, Henry Lemaire, Julius Marcus, Mark Abbett

SUBJ: MACHINE EXTENSIONS TO PDP-11

DATE:
FROM:
EX:
MS:

PAGE 1
04-04-75
GORDON BELL
X2236
ML12/A51

* * * * *
 * * * * * TO: * * * * * FILE * * * * *
 * * * * *

CONFIDENTIAL

Several of us are looking at extending the 11 architecture such that it would be better implementable across a broader performance range (e.g. with larger memories and on still smaller machines).

The chief problem being addressed is extending the address space such that a program can access large arrays easily.

I would like your input as to the various deficiencies in the 11 you think would significantly improve the capability of future implementations, while retaining a very high degree compatibility with existing programs.

Implementations? Instruction set? Structures (e.g. multi-processors, networks, etc.)? Capabilities? Operating Systems improvements?

GB:mjk

To: Engineering Managers

DIGITAL

INTEROFFICE MEMORANDUM

SUBJ: 11 PROGRAMMED I/O

DATE:
FROM:
EX:
MS:PAGE 1
04-08-75
GORDON BELL
2236
ML12-1/A51

* * * * *
 * TO: FILE * * * * *
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SUBJ: Plo*--vs(KIo+Pc)* BRIEF NOTE ON 11 PROGRAMMED I/O
 AND CHANGES IN PDP-11 ISP FOR BETTER I/O TRANSMISSION

To: VAXC, Chuck Kaman, Jim O'Loughlin

I have long been against Plo's (i.e. channels in the IBM
 venacular) because:

0. Historically, the IBM 709, 7090 provided them in a really maximally costly way.
1. They add logical, and physical complexity, without much payoff (low duty factor). Their real function is to pass information, without change,
2. As a somewhat intelligent device, they require more coordination from a higher level intelligent processor, Pc, than either another Pc or a lesser device,
3. Another processor which has to be programmed, diagnosed, and stocked.
4. Programs have to be written for it, dynamically, by Pc.
5. In the limit, 1 memory cycle is required to transfer data, for high speed devices, the NPR is used, and achieves this limit.
6. Even in the case of IBM channels, an interrupt/block transfer to Pc is often required since the Pc executes a program to plan the transfers.
7. I/O computers organized in the fashion of the 6600, and networks are the real answer to I/O by doing significant data reduction and preprocessing,

Most of the things Plo's can do well, a Pc can do substantially better (e.g. optimize disk blocks in order of arrival time). When a Pc is used this way, and runs out of capacity, we simply add a second Pc of the same type,

I do believe we should have more powerful I/O instructions

DIGITAL

INTEROFFICE MEMORANDUM

SUBJ: 11 PROGRAMMED I/O

PAGE 2
 DATE: 04-08-75
 FROM: GORDON BELL
 EX: 2236
 MS: ML12-1/A51

In our Pc, to assist in transferring and manipulating data from the I/O world. This includes:

1. More rapid response to interrupts to transfer blocks (vectors) between the Mp (via Pc) and an I/O controller, Kio.
2. Actually processing information on the fly for certain tasks. For example, in communications tasks, it is appropriate to take in a character, translate it, put it in a queue, and evoking a process (interrupt) in the Pc, if necessary.

The performance gain, attributable to channels, can be obtained by:

1. Giving commands rapidly to a simple device controller, Kio.
2. Double buffering a second command in Kio.

CURRENT INTERRUPT PROCESSING IN Pc

Responding to an interrupt, and transferring a word takes:

Save PC, PSW	4
MOVE IO, LOC	5
ADC LOC	3
DEC CTR	3
BR	1
RTI	3

Total 19 Memory Cycles

ADDING BLOCK TRANSMISSION

By placing a control block for block transfers, in the trap vector locations, we get:

----->	!I/O Control!
!	
-----	-----
!PTR IOC !!	!Pfr to LOC!
-----	-----
!New PSW !	!Misc. CTR!

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: 11 PROGRAMMED I/O

DATE: PAGE 3
FROM: GORDON BELL 04-08-75
EX: 2236
MS: ML12-1/A51

!New PC !

This takes 6 memory cycles per word transferred.

USE OF BLOCK TRANSMISSION IN MICROCODED MACHINES USING CURRENT PROGRAMMED Kio's.

The 11A40 can implement the instruction directly and achieve the 3X speed up.

For the PDQ, the variables can be moved into its WCS, and in principle, achieve a speed of 2 memory cycles with current programmed controllers (Kio)--another factor of 3. Note, that in this case, since the PC doesn't move, there is no need to fool with the stack, etc.

Summary of changes:

Current controllers via programming	19
Additional block transfer instruction for current controllers	6
Microcode caching of data for block transfer instructions using current controllers	2
Best case--NPR controllers	1

IMPROVING THE RESPONSE TIME FOR HIGH SPEED CONTROLLERS

A second problem, getting commands to an NPR-controller, Kio fast, can be solved in a similar way. Although in principle, it could be handled by double buffering in the controller.

In this case, a block of instructions are sent to the controller at interrupt level. This could be accomplished in several ways, including a block transfer instruction. Most likely, this instruction should be executed at a high priority level, and an interrupt caused to a lower level, signifying command completion. This needs to be worked out based on our current K's.

*Pc--central processor; Plo--I/O processor (IBMese=channel)-- a device which executes commands (instructions) from a stored program the Plo is interpreting; Kio--io controller--simple device to execute 1 instruction at a time.

GB:m.jk

digital**INTEROFFICE MEMORANDUM**

TO: Lloyd Tucker

LOC/MAIL STOP
PK3-2

DATE: April 9, 1975

CC: Dick Clayton

ML5/E71

FROM: Gordon Bell

DEPT: OOD

EXT: 2236

LOC/MAIL STOP: ML12/A16

SUBJ: Signatory Authorization

Please enter signatory authorization as follows:

Cost Center	385	394
Location Code	MY	MY
Manager	R. Clayton	R. Clayton
Badge #	1590	1590
Advances	\$500	\$500
Business Expenses	\$3,000	\$3,000
Purchase Requisition (Expense)	\$20,000	\$20,000
Purchase Requisition (Capital)	\$20,000	\$20,000

/ale



INTEROFFICE MEMORANDUM

TO: Jean Haynes

DATE: February 18, 1975

1318

FROM: Gordon Bell

DEPT: 00D

EXT: 2236 LOC: ML12/A51

SUBJ: AIR TICKET REIMBURSEMENT

The attached check for \$838.02 covers the following personal air tickets for 1974:

<u>Date</u>	<u>Ticket/Carrier</u>	<u>Amount</u>
1/25/74	314796	\$ 99.27
1/30/74	314982	25.00
3/19/74	318904	99.27
4/16/74	455887	63.00
8/14/74	TWA	105.27
9/26/74	TWA	105.27
10/25/74	DL	52.74
10/19/74	TWA	104.73
11/12/74	AA	183.47
	TOTAL	\$838.02

GB:mjk

Attachment

C. GORDON BELL GWENDOLYN K. BELL PAGE FARM ROAD LINCOLN, MASS. 01773		No. 378	53-209/113
PAY TO THE ORDER OF	<i>Digital Equipment Corp</i>	<i>Apr 6 1975</i>	<i>\$838⁰²</i>
	<i>Eight hundred thirty eight and ⁰²/₁₀₀</i>		DOLLARS
Middlesex Bank NATIONAL ASSOCIATION - MASSACHUSETTS		<i>G K Bell</i>	
⑆0113⑆0209⑆ 09 177 910 9⑆⑆			

SUBJ: STAFF MINUTES

DATE:
FROM:
EX:
MS:

PAGE 1
04-11-75
DICK CLAYTON
3638
ML5-2/E71

* * * * *
TO: FILE
* * * * *

SUBJ: OOD STAFF MEETING MINUTES--April 10, 1975

Attendees: Larry, Phil, Bob, Dick
Guests: Ken Olsen, Vince Bastiani

1. SDLC Chip--Vince proposed that Digital go after the SDLC chip as a non proprietary device with more than one real vendor (funding primarily via PO for working parts). Vince will try for short term proprietary status of parts. Vince will send status report after formal decision and bi-monthly thereafter.
2. Topic for woods--how we build the Interaction between the development groups toward the end of better system/product development. Larry is to structure the meeting with Ed Schein/John Cronkite. Date tentatively: . Location: Cape Cod.
3. Gordon's assignments were fine with everyone.
4. A rather lengthy discussion ranged around the issue of our individual and collective roles in continuing to drive for more forceful, aggressive, and effective development strategies and processes. It was felt that Ed Schein could help us work these issues.

RC:mjk

D I G I T A L

INTEROFFICE MEMORANDUM

SUBJ: BRAZIL

DATE:
FROM:
EX:
MS:

PAGE 1
04-14-75
GORDON BELL
2236
ML12-1/A51

* * * * *
TO: FILE
* * * * *

SUBJ: BRAZILIAN AND OTHER 'DEVELOPING COUNTRY' MARKETS

←←←←←

TO: TED JOHNSON

CC: RON SMART

FROM GWEN ON BRAZIL

I have three major contacts:

Rubens Vax da Costa, former President of the National Housing Bank now Director, Abril S.A., Sao Paulo, Brazil. Still well connected with the government. (This is mainly a publishing firm, but he is in his forties and I doubt if he is out of action.) (PhD economist from Johns Hopkins)

Jaime Lerner (architect-politician) former Mayor of Curitiba and now Director of the Metropolitan Region formed from the joining of the states of Guanabara and Rio de Janeiro. He is in his 30's and definitely on his way up in the government structure.

These would take rather 'subtle' cultivation--invitations from Gordon and I to visit us on a trip to the US--or our visiting them.

Victor Gradin, the prime mover in Salvador Bahia. He is director of many organizations--ranging from the cocoa board to the new very large scale industrial estate in Salvador. He likes to wheel and deal (in his early forties) and with a letter of introduction would take to direct contact by someone of the level of Ron Smart. (I believe his PhD is from Stanford.) He was influential, for example, in bringing large international drug companies to locate on the industrial estate--so he would know who was coming, there might be a direct tieup here.

FROM GORDON ON BRAZIL

Various academic contacts at Dept./Dean level:
Head of Engineering at Telephone Company invited me to talk there 2 years ago. He is well connected, probably the right

DIGITAL

INTEROFFICE MEMORANDUM

SUBJ: BRAZIL

DATE:
FROM:
EX:
MS:PAGE 2
04-14-75
GORDON BELL
2236
ML12-1/A51

level to go to government.

It was clear that we weren't approaching Brazil seriously two years ago. Although things have improved, we should still get serious. My feeling is that a powerful, well-known national is the only way. I have no experience on these matters; my only experience was in Australia to hire Ron Smart, who was well known, respected, bright, and very energetic. This seems like the only answer. My friend at the Telephone Company may be the right person, if we want to go in, in a big way.

I can start through my academic friends here to gather names. In general, I can probably get introductions through these friends, and then ask them in turn, at almost any place.

What about through HBS or a bank to look for people?

FROM GWEN ON THE PHILIPPINES AND INDONESIA

In March, I was on a UN mission to the Philippines and will be with the same group in Indonesia in July. While there, I worked with the President of the University of the Philippines, the President of the Women's University of the Philippines, the Director of the Commission on Human Settlements, the Population Commission, and the Environmental Authority; I had access to (and met) President Marcos and the Head of the Development Bank. I cannot predict specifically who or what in Indonesia. I would be willing to coordinate these trips and have a lunch or dinner with the significant people that I deal with, if there is someone appropriate from DEC.

D I G I T A L INTEROFFICE MEMORANDUM

SUBJ: TERMINALS

DATE:
FROM:
EX:
MS:

PAGE 1
04-14-75
GORDON BELL
2236
ML12/A51

* * * * *
TO: FILE
* * * * *

SUBJ: NOISE AT NSF MEETING, LLL RE TERMINALS; and OURS

To: Distribution

Tektronix graphic terminals are really selling well apparently. They are apparently going to be more aggressive, and generally entrance terminals with language (e.g. APL). Jack Shemer, a performance measurement computer scientist type at Xerox, is working within XDS on terminals.

People do perceive the HP2640 as the standard, quality terminal. However, I believe there is a bigger market that buys only on price...and may trade off far more in user productivity (hopefully not the case here).

I believe we must go ahead and create the low cost and 33KSR standard image for VT50 with 20 lines, lower case and optional copier.

The VT51 will be the programmable features one, to cover all the 2640 features and at 25% lower price.

We need dialogue on the low cost, scan graphics, and the LSI-11 with terminal. Len's package looks well on way to a great Classic 11.

GB:mjk

Distribution

-
- Ed Corell
- Len Hallö
- Win Hindle
- Andy Knowles
- Bill McBride
- Stan Olsen
- Tom Stockebrand
- Steve Teicher

CC: Ken Olsen, Bob Puffer

Subj: MINUTES FOR OOD MEETING OF 8/21/75

01684

Present: Dick Clayton, Julius Marcus, Larry Portner, Bob Puffer

1. Minutes: no comments.
2. VAX organization and product. Bruce Delasi

Bruce discussed the Marketing Committee presentation and acceptance of the VAX Board concept. This will be essentially the VAX PSG and consist of Win, Ed Kramer, Irwin Jacobs, Larry Portner and Dick Clayton.

A discussion of compatibility at the Marketing Committee showed that expectations on binary level compatibility are not well understood. Bruce will resolve this issue promptly.

The concept of a Program Development office and much of the staffing looks good. Larry and Dick are formally and JOINTLY on the line for the management of Bruce and the VAX project. This will include formal weekly status meetings with Larry, Bruce and Dick. It was clear that the list of project decisions, milestones, and assigned responsibilities is not yet visible (and probably missing).

Julius Marcus noted that Product Line management level people still need a 1-3 page VAX positioning document covering strategy and product that is specific enough to generate gut feelings.

3. VT61 BUSINESS PLAN Mike Wurster/Stocky

In general, the business plan left everyone with a warmer feeling that people could explain where the VT61 was going. About 25% of the projected volume seems completely dependent on a good level of Block Mode support across at least RSTS, RSX11M, and RSX11D. It is by no means clear how such support will happen. It is presently not planned formally by any group. We will review this status in 6-8 weeks.

Julius noted that Block Mode support might well be best placed in a communications front end, not each individual operating system (again 6-8 weeks for review).

SUBJ: AGENDA/MINUTES OOD

PAGE 5
DATE: 08-27-75
FROM: DICK CLAYTON

01685

4. MICRO PROCESSORS

Hushes/Corell et al

OOD approved the proposal to move promptly to one of the outside microprocessors for application in the LA36 cost reduction, as well as adoption as a de facto inhouse standard for controller and peripheral applications. John was to proceed on vendor selection.

5. HARDWARE DEVELOPMENT BUDGET

Puffer

Bob presented the budget situation for "Hardware Development" (outlined in Bob's memo of 8/20/75). It was agreed that formal action would be deferred until after the Sept. Woods. It was also agreed that most of Bob's proposals seemd sound and probably consistent with expected NOR charges (4%-9% per quarter increase).

Dick expressed concern about the advisability of holding the RK07 schedule in the light of RK06 slippage. (This represents at most a \$50K question.)

RC:mjk

Attachment



6/17

INTEROFFICE MEMORANDUM

TO: Distribution

LOC/MAIL STOP

01693

DATE: June 10, 1975
FROM: Bill Avery
DEPT: Industrial Products Engineering
EXT: 6313
LOC/MAIL STOP: ML5-2/E50

SUBJ: SERIAL BUS SPECIFICATION

Bill
Bring to a head... when?

Gordon

Attached is a copy of the Serial Bus Specification for your information and review.

This is the third version of a multidropped serial bus specification; the second and third were defined to expand the capability of the serial link beyond that of the first version.

The three versions are summarized as follows:

Version 1: A proprietary protocol designed primarily for multidropping sixty-four (64) 1200 baud terminals on a 1MHz coaxial cable. Each bus transaction could transfer a one or two byte data field.

Version 2: An extension of version 1 to allow the inclusion of peripherals on the cable. Each bus transaction could transfer any one of eight pre-defined data field lengths (1,2,4,5,9,16,128, or 144 bytes).

Version 3: Designed for common carrier or dedicated cable operation and to allow any data field length up to 256 bytes. The protocol is based on SDLC, but extended to provide those functions necessary for a bus.

The attached specification includes the following:

Section 1: A description of the serial bus

Section 2: A discussion of serial bus performance

Section 3: The serial bus protocol

Section 4: A discussion of serial bus interfacing.

Appendix A: Application of the bus protocol to other serial bus structures.

The serial bus protocol defines the protocol extensions necessary to implement the serial bus extensions defined in Appendix A. However, subsets of the serial bus protocol can be implemented to minimize device interface costs while maintaining the upward compatibility.

The following persons have worked on the ad-hoc committee to define the serial bus specification:

Dave Rogers	11 Engineering
Vince Bastiani	DEC Comm.
Dave Nelson	11 Engineering
Tony Lauck	DEC Comm.
Bill Avery	Industrial Products Engineering

Any comments or recommendations would be greatly appreciated.

SUBJ: AGENDA/MINUTES OOD
 DATE: 09-04-75
 FROM: DICK CLAYTON
 EX: 3638
 MS: ML5-2

* * * * *
 TO: FILE
 * * * * *

SUBJ: OOD STAFF AGENDA--9/4/75

10:30 Review Minutes
 10:35 Review agenda
 10:40 Product Line Mgr. Dinner Meetings Portner
 11:00 Business Plan Review Procedure Laut
 11:30 Product Managers Review
 Job description Abbett
 Green Sheet Portner/Clayton
 Overall organization perception All
 12:15 Assignment of Best/Noelcke Puffer/Clayton
 12:30 Role of OOD Secretary (rotation) All

FUTURE AGENDA ITEMS

When do we want to finalize capital & operating budgets?

9/11 OOD-MKT Committee interface (40 min.)
 9/11 Sales meetings (especially Spain) (10 min.) Clayton
 9/11 Status of microprocessor project (15 min.) Hughes
 9/11 What is our affirmative action status Abbett
 and what problems are key for
 next 12 months (30 min.)
 9/11 What is PDQ status and what have we learned? (15 min.) Demmer
 9/18 What is the purpose, form, and content of the upcoming MIT lecture series? (30 min.) Puffer/Cronkite
 9/18 What is 3 year serial bus strategy? (20 min.) Bastiani/Clayton

SUBJ: AGENDA/MINUTES OOD

DATE:
FROM:

PAGE 3
09-04-75
DICK CLAYTON

SUBJ: MINUTES FOR OOD MEETING OF 8/28/75

01700

Present: Dick Clayton, Phil Laut, Henry Lemaire, Julius Marcus,
Larry Portner, Bob Puffer

Guests: John Leng, Ulf Faserquist, Brian Croxon, Mike Gutman,
Vince Bastiani, Bill Avery

1. Review of minutes--no comment.

2. Corporate Woods (Sept.)

Gordon and Larry directed to strongly push to hold Central Engineering a constant percent of FY76 revenue (assuming an increase is expected).

3. Fire Prevention

Julius mentioned a DEC 10 fire the night before at an AEC site. It was felt that it may well be smart to devote one or more full OOD sessions to the topic of product design and product liability (are we doing enough?).

4. Communications Strategy

Vince Bastiani

A general discussion centered on some of the key implications of our communications development. Some of the major topics were:

A. IO--the bipolar MSI microprocessor used in the implementation of the interprocessor link has several important possibilities most of which need to be better understood. The IOP seems to be a good bit hanging processor to hang on the UNIBUS (do we need, or can we stand, another computer architecture?). The system implications of IOP for partitioning of hardware and more importantly partition of software, are very great. These seem to not yet be answered.

In four weeks Vince will report back on their formal recommendations for IOP usage by the product groups.

In four weeks Vince and Mike will address the software system architecture strategy question as they relate to our overall communications strategy.

In 6-8 weeks, a formal statement of total systems architecture strategy will be forthcoming from Bastiani, Bell, Clayton, Lauck, Corbin, Xenakis, etc.

01701

- B. LSI Communication Strategy--a sync line interface and 4 line ASYNC MUX is being done for LSI-11.
- C. Business Plans for most communications projects will be done in 6-8 weeks by Tony.
- D. (Editorial: it is clear we, OOD, must spend more time to help insure Vince gets a total communications strategy happening!)

5. Serial Bus

There seems to be a reasonably good bus spec that allows for single or multiple masters. Julius, Vince and Bill Avery believe this bus spec and its support should be a significant part of future systems architectures.

Bastiani and Avery will push the present product analysis further to show the technology and cost assumptions that are necessary to make this the preferred system architecture for most peripherals.

Clayton will push the issue to become part of the basic systems architecture (assuming it continues to look like the way to go).

6. Memory for DEC 20

John Lens, Henry Lemaire and their troops discussed the various considerations for the next DEC system 20 memory product. It seems the DEC 20 plans are to move to 4K MOS based memories for shipment by late FY77. This seems primarily motivated by uncertainty in the in house 64K memory development and the expectation that the 4K based design would allow quick transition to the 16K chip in the FY78 time frame (thereby much lower product cost).

Brian and Henry are concerned that the industry 4K MOS capacity is strained and the proposed DEC 20 strategy may incrementally cost DEC much more than the projected DEC system 20 savings.

John and Henry agreed to further JOINTLY refine their

SUBJ: AGENDA/MINUTES OOD

DATE:
FROM:

PAGE 5
09-04-75
DICK CLAYTON

understandings of the problem. Bob pointed out that this may well be one that Ken finally calls on instinct! The issue is to be reviewed by OOD in early October.

01702

INTEROFFICE MEMORANDUM

LOC/MAIL STOP

TO: Gordon Bell
Phil Laut
Henry Lemaire
Julius Marcus
Larry Portner
Bob Puffer

DATE: August 13, 1975
FROM: Dick Clayton
DEPT: Computer Systems Development
EXT: 3638
LOC/MAIL STOP: ML5/E71

SUBJ: OOD STAFF MEETING - AUGUST 21, 1975
GORDON BELL'S OFFICE

AGENDA

10:30 A.M.	Review of Minutes.	
10:35	Review this weeks Agenda.	Delagi et al
10:45	What is VAX Organization?	Delagi et al
11:05	What are VAX Goals and Products?	Delagi et al
11:35	VT61 Business plan review.	Puffer
12:05 *	Microprocessor selection for printers.	Hughes/Corell
12:20	Should Printer Engineering spend more on budget in FY 76 (unspent 75 plan).	Puffer
12:40	End. Lunch.	

FUTURE TOPICS

8/28/75	Where does Vince find funding for SDLC in-house chip development? (15 min.)	Vince Bastiani/ Bob Savell
8/28/75	Is there an action plan that allows follow-up on a field oriented product safety problem?	Shields/OOD
8/28/75	Product Managers dinner meetings.	Portner
8/28/75	Assignment of Best & Noelcke.	Puffer/Clayton
8/28/75	What's our Military Computer strategy? (written report by 8/14)	Clayton
9/04/75	(30 min.) Product Managers Green Sheet and job classifications.	Puffer/Portner/ Clayton
* 9/04/75	10:30 Is DEC System 20 group doing the right thing by changing to MOS.	Lemaire/Leng/Fagerquist

*Leng & Lemaire
couldn't make it
today. Hughes asked to get on.*

01704

9/04/75	Business Plan Review Procedure.	Laut
9/04/75	Review of the role of OOD Staff secretary (and rotation).	All
9/04/75	QCMS Defect Reporting System	Smith/Pecore
9/11/75	OOD-Marketing Committee interface.	Laut/All
9/18/75	What is the three year serial bus strategy (15 min.).	Clayton/Bastiani
9/18/75	Approval of OOD Space Guidelines (30 min.).	Laut
September	Report on in-house PDP-11 usage.	Computer Resources Committee
	Is there a Field Integration Plan yet?	Smith/Shields/ Clayton/Puffer
	Honararia Policy.	Bell

SUBJ: VAX-11 SPEC REVIEW

DATE:
FROM:
EX:
MS:

PAGE 1
09-16-75
GORDON BELL
2236
ML12/A51

* * * * *
TO: DISTRIBUTION
* * * * *

Subj: REVIEW OF FIRST REVISION OF VAX-11 SPECIFICATION

The first revision of the VAX-11 specification will be distributed September 26. It is written in the form of the System Reference Manual. See attached table of contents and introduction. This memo describes how we will conduct the review of the System Reference Manual. It will help you plan for allocating people and time during the first two weeks in October.

* Please look over the distribution list *
* and circulate this memo to people in *
* your group who will be able to *
* contribute to the review. *

Reviewers will have one week to read the document (29 Sep - 3 Oct) and one week to make written responses for VAXA (6 Oct - 10 Oct) to Gordon Bell. VAXA will sort and distribute these comments as agenda for the review meetings. In order to obtain the most meaningful comments, we are asking the following groups to meet separately to go over the document. Each group should write up a JOINT SET OF COMMENTS, which represents its inputs. Consensus is desired, but is not necessary. The individual named is responsible for calling his group's meetings and appointing someone to write up the comments. Individual comments will be accepted, but group inputs will carry greater weight.

Note, these comments due to Gordon Bell by 10 Oct.

01753

Group

 Components
 CSS
 Business Products
 LDP
 Trad. + Typset
 OEM
 DECCOMM
 EPG/ECP
 Industrial
 DECsystem 10
 PDP-15
 Hardware Implementation
 Software Architecture
 Star Marketing PSC
 Operating System Design
 R&D
 Languages & Data Management
 Applied Programming
 Software Development Methods
 -11 Compatibility
 Diagnostics
 Field Service
 Manufacturing

Individual

 Bill Hosan
 John Holman
 Irwin Jacobs
 Ed Kramer
 Bob Lane
 Bill Long
 Julius Marcus
 Charlie Spector
 Brad Vachon
 Tom Campbell
 Dick Devlin
 Len Hushes
 Pete Conklin
 Al Avery
 Dave Cutler
 Dick Eckhouse
 Ron Ham
 Ed Favvre
 Bill Slack
 Tom Rarich
 Ed Kenney
 Rex Bursess
 Kent McNaughton

In order to distribute the document to the proper people on September 26, we need to make up the distribution list of people who will read the 250 page document and write comments. Please fill out the stub below if you want a copy.

GB:mjf
 Attachment

 Please send me VAX-11 System Reference Manual, Rev. 1:

Name:-----
 Mail Stop:-----
 Group:-----

I prefer: !! Fiche
 !! Hard copy

Return this stub to: Mary Jane Forbes, ML12-1/A51

CONTENTS

01754

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CHAPTER 2	BASIC ARCHITECTURE
2.1	Addresses
2.2	Data Types
2.3	Processor State
2.4	Instruction Formats
2.5	I/O Structure
2.6	Arithmetic and Logical Operations
CHAPTER 3	INSTRUCTION FORMATS AND OPERAND ADDRESSING MODES
CHAPTER 4	INSTRUCTION SET
4.1	Notation
4.2	Summary
4.3	Integer and Logical
4.4	Floatings
4.5	Address
4.6	Variable Bit Field
4.7	Control
4.8	Strings
4.9	Decimal
4.10	Special
CHAPTER 5	MEMORY MANAGEMENT
CHAPTER 6	EXCEPTIONS AND INTERRUPTS
CHAPTER 7	PROCESS STRUCTURE
CHAPTER 8	INPUT-OUTPUT
CHAPTER 9	COMPATIBILITY MODE
APPENDIX A	GLOSSARY
APPENDIX B	ASSEMBLER CONVENTIONS
APPENDIX C	PROCEDURE CALL CONVENTIONS
APPENDIX D	PROGRAMMING EXAMPLES

CHAPTER 1

INTRODUCTION 14 SEP 75--REV 1

1.1 INTRODUCTION

The VAX-11 represents a significant extension of the PDP-11 family architecture. It shares with the PDP-11 byte addressing, similar I/O and interrupt structures, and identical data formats. Although the instruction set is not bit level compatible with the PDP-11, it is very similar, and can be mastered by a PDP-11 programmer without retraining. Likewise the similarity enables simple manual conversion of existing PDP-11 programs to VAX-11. Existing user mode PDP-11 programs which do not need the extended features of VAX-11 can run unchanged in the PDP-11 compatibility mode provided in VAX-11.

As compared to the PDP-11, VAX-11 offers a greatly extended virtual address space; additional instruction and data types; and new addressing modes. Also provided is a sophisticated memory management and protection mechanism, and hardware provided process scheduling and synchronization.

A number of specific goals guided the VAX-11 design:

1. Maximal compatibility with the PDP-11 consistent with a significant extension of the virtual address space, and a significant functional enhancement.
2. High bit efficiency. This is achieved by a wide range of data types and new addressing modes. PDP-11 programs naively translated to VAX-11 should not grow significantly in size; while programs redesigned to exploit VAX-11 should get significantly smaller.
3. A systematic, elegant instruction set with orthogonality of operators, data types, and addressing modes. This enables the instruction set to be exploited easily, particularly by high level language processors.
4. Extensibility. The instruction set is designed so that new data types and operators can be efficiently included in a manner consistent with the currently defined operators and

01756

data types.

5. Range. The architecture should be suitable over the entire 1000 to 1 range of computer system implementations currently sold by DEC. This broad range is achieved by high bit efficiency, enough power and generality for high end systems, and well defined mechanisms to enable software interpretation of complex operations on low end systems. Part of this range will be achieved by multiprocessing and suitability for multiprocessing has been factored into all VAX-11 design decisions.

The VAX-11 Preliminary System Reference Manual describes the the architecture of VAX-11 and holds for all implementation of VAX-11 systems.

\A note on the manual format: At certain points in the manual text comments on why certain decisions were made, unresolved issues, etc., are included. These are included between a pair of back slashes.\

ALUSIC, DON PK3-1/M10
ARMSTRONG, BOB ML1-2/E65
ARULPRAGASAM, JEGA ML5-5/E54
ATTERBURY, GERRY MR
BARNETT, TOM PK3-1/M33
BASTIANI, VINCE ML5-3/E43
BEAN, BOB ML5-5/E76
BELL, GORDON ML12-1/A51
BELL, JIM ML3-4/E41
BENEDICT, GORDON PK3-1/E15
BICCHEERE, FRANK PK3-1/M12
BRENDER, RON ML3-5/E40
BROOKS, BUZ PK3-1/M33
BUCKLEY, JOHN PK3-1/M56
BURNESS, JACK ML1-2
BUSIEK, DON PK3-2/S17
CADY, ROGER PK3-1/M29
CAMPBELL, ART PK3-1/M12
CAMPBELL, TOM MR1-1
CANE, DAVE ML1-2/E65
CASABONA, RICK ML3-5/E35
CHRISTY, PETER ML12-2/A62
CLAYTON, DICK ML5-2/E71
CONKLIN, PETE ML12-2
CUDMORE, JIM ML1-4
CUTLER, DAVE ML3-5/E40
DELAGI, BRUCE ML5-5/E35
DEMHER, BILL ML5-5/E67
DEPEYROT, MICHAEL ML21-4
DEVLIN, DICK MR1-1/M42
DICKMAN, LLOYD ML3-5/E35
DONOVAN, TOM PK3-1/E15
DURR, BRUNO PK3-1/S44
ELLSON, KEN ML5-5/E40
FAUVRE, ED ML21-4
FEHSKENS, LEN ML3-5/E35
FERNALD, DAVE ML5-5/E40
FINN, DICK ML5-2/M11
FISHER, JOHN ML12-1/A51
FORBES, MJ ML12/A51
FREIDRICH, JOHN ML21-4
FROST, DON MR2-4/M16
GILMORE, JACK PK3-1
GOURD, ROGER ML5-5/E35
GROVE, RICH ML5-5/E40
HAM, RON ML5-5/E40

HASSETT, FRANK ML5-5/E40
HASTINGS, TOM ML12-1/A51
HINDLE, WIN ML5-2/A53
HOGAN, BILL MR2/M19
HOLMAN, JOHN PK1/P84
HOROVITZ, MARV ML21-4/E20
HUGHES, LEN ML1-2/E35
JACKS, MARTY ML3-5/E40
JACOBS, IRWIN PK3-1/M33
JENKINS, STEVE ML5-5/E54
JOHNSON, BILL ML5/E77
JOHNSON, TED PK3-2/A55
JOHNSTON, MALCOLM ML5-2/E71
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KELLY, BILL ML5-5/M40
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LACROUTE, BERNIE ML5-2/M46
LANDER, BOB PK3-2/F33
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LARY RICH ML5-5/E76
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LAUT, PHIL ML12-1/A16
LEMAIRE, HENRY ML1-2/E61
LENG, JOHN MR/A65
LEONARD, JUD MR1-2/E47
LEROYD, CHARLES ML3-5
LEVY, JOHN ML5-5/E54
LEWINE, DON MR1-2
LIPMAN, PETER ML3-5/E35
LONG, BILL PK3-1/A60
MANTER, WALTER ML21-4/E10
MARCUS, JULIUS PK3-1/M10
MCBRIDE, BILL MR2/E14
MEANY, JOE PK3-1/M12
MENDELSON, GARY ML5-5/E67
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MIKULSKI, STEVE ML5-2/M46
MILESKY, JOHN ML5-5/E37
MOORE, GERRY PK3-2/A55
MUCCI, JOHN MR2-4/M16
MUDGE, CRAIG ML5-5/E54
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NELSON, DAVE ML3-4/E41

O'CONNOR, DENNIS ML21-3/E48
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OLSEN, STAN PK3-1/A57
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FLOWMAN, GEORGE ML21-4/E20
POONEN, GEORGE ML3-4/E40
PORTNER, LARRY ML12-2/A62
PUFFER, BOB ML1-3/E38
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ROTHMAN, STEVE ML5-5/E54
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SLACK, BILL ML21-4
SMITH, JACK WM/A75
SMITH, SHARON ML5-5/E54
SPECTOR, CHARLIE ML5-2/M40
SPIER, MIKE ML5-5
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STRECKER, BILL ML3-4/E41
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THOMPSON, BILL PK3-2/F41
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WECKER, STU ML12-2/A62
WHITE, PAT ML5-5/E39
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WITMORE, GERRY WA
WONG, JOHN ML5-5/E54
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WULF, BILL CMU
ZINS, ART ML21-4/S17

SUBJ: AGENDA/MINUTES OOD

DATE:
FROM:

PAGE 3
09-04-75
DICK CLAYTON

01763

SUBJ: MINUTES FOR OOD MEETING OF 8/28/75

Present: Dick Clayton, Phil Laut, Henry Lemaire, Julius Marcus,
Larry Portner, Bob Puffer

Guests: John Leng, Ulf Fagerquist, Brian Croxon, Mike Gutman,
Vince Bastiani, Bill Avery

1. Review of minutes--no comment.

2. Corporate Woods (Sept.)

Gordon and Larry directed to strongly push to hold Central Engineering a constant percent of FY76 revenue (assuming an increase is expected).

3. Fire Prevention

Julius mentioned a DEC 10 fire the night before at an AEC site. It was felt that it may well be smart to devote one or more full OOD sessions to the topic of product design and product liability (are we doing enough?).

4. Communications Strategy

Vince Bastiani

A general discussion centered on some of the key implications of our communications development. Some of the major topics were:

A. IO--the bipolar MSI microprocessor used in the implementation of the interprocessor link has several important possibilities most of which need to be better understood. The IOP seems to be a good bit banging processor to hang on the UNIBUS (do we need, or can we stand, another computer architecture?). The system implications of IOP for partitioning of hardware and more importantly partition of software, are very great. These seem to not yet be answered.

In four weeks Vince will report back on their formal recommendations for IOP usage by the product groups.

In four weeks Vince and Mike will address the software system architecture strategy question as they relate to our overall communications strategy.

SUBJ: AGENDA/MINUTES OOD

PAGE 4
DATE: 09-04-75
FROM: DICK CLAYTON

In 6-8 weeks, a formal statement of total systems architecture strategy will be forthcoming from Bastiani, Bell, Clayton, Lauck, Corbin, Xenakis, etc.

- B. LSI Communication Strategy--a sync line interface and 4 line ASYNC MUX is being done for LSI-11.
- C. Business Plans for most communications projects will be done in 6-8 weeks by Tony.
- D. (Editorial: it is clear we, OOD, must spend more time to help insure Vince sets a total communications strategy happening!)

5. Serial Bus

There seems to be a reasonably good bus spec that allows for single or multiple masters. Julius, Vince and Bill Avery believe this bus spec and its support should be a significant part of future systems architectures.

Bastiani and Avery will push the present product analysis further to show the technology and cost assumptions that are necessary to make this the preferred system architecture for most peripherals.

Clayton will push the issue to become part of the basic systems architecture (assuming it continues to look like the way to go).

6. Memory for DEC 20

John Leng, Henry Lemaire and their troops discussed the various considerations for the next DEC system 20 memory product. It seems the DEC 20 plans are to move to 4K MOS based memories for shipment by late FY77. This seems primarily motivated by uncertainty in the in house 64K memory development and the expectation that the 4K based design would allow quick transition to the 16K chip in the FY78 time frame (thereby much lower product cost).

Brian and Henry are concerned that the industry 4K MOS capacity is strained and the proposed DEC 20 strategy may incrementally cost DEC much more than the projected DEC system 20 savings.

John and Henry agreed to further JOINTLY refine their

SUBJ: OOD AGENDA==9/18/75

DATE:
FROM:PAGE 3
09-17-75
GORDON BELL

To: Distribution

SUBJ: SEPTEMBER BUDGET MEETING HOT ISSUES FOR OOD
(or Primate Positioning)Hot issues from the September budget (and elsewhere) meetings
for us:

0. Redbook 6 months update (OOD) to MC==software is there already? This is needed about the time we go to OC for budget increase.
1. Budget increase* request (Phil)==in line with P/L budget increase to OC.
2. Commercial P/L Eng, Mgr, (Stan/Gordon)==we need an eng, manager for commercial products that would report to us both and worry about these products. There is a significant component of software and this engineering would do the integration of plans for this. Possibly other activities (e.g. Word processing Products) would be integrated. How does this relate to engineering within COMM, Bus Products, and Typesetting?
3. System configurations ordering problem (?)==we need to tighten up systems in a top-down fashion to include memories of all kinds (core, disk, tape) and terminals.
4. Configuring Problem (?)==it takes a really bright person 1-2 hours. How can this be sped up? what about the program? Is someone still working on it?
5. VAX and other project reporting to OC (GB, LP, BD)==Ken wants increased visibility of VAX vis a vis reporting on it (attached).
6. Field Service and software support/Design Tradeoffs (OOD/Bruno, Ted, Jack)==we're not really making giant strides in the philosophy of designing products so that they can be serviced differently. With a significant unplanned, increase in FS cost of labor, reflecting either extremely poor planning or a misunderstanding of the labor supply, it's clear we can't grow like we have and still build products in the same old way. Software Support has a similar problem. We have to come up with some joint goals here. How? Jack and Dick were going to report on possibilities. The RK06 design problems are symptomatic of something not happening. When? It's time for another meeting this time with Ted after there's some preliminary work.

SUBJ: ENG, PRESENTATIONS OF 11/70

DATE:
FROM:
EX:
MS:

PAGE 1
10-01-75
GORDON BELL
2236
ML12/A51

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TO: FILE
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TO: Distribution

Bob did an admirable job presenting the 11/70 to NASA (Godard) on Tuesday. I hope others from the engineering team can get into the field to interact with customers and sales in a similar fashion.

Perhaps I led him astray, but I suggested he not mention the 11/70 as being based on the 11/45. We still have vestiges of 16 versus 32 haunting us--(does the attached paper help?). I still wish we'd put in a 32-bit integer type and a 32-bit console to cool this. We need to talk bytes, words (16-bit), long word (32-bit), etc, a la VAX, and to introduce these as such. Putting everything in bytes may be the best way, although our instructions are multiple 16-bit words in the same way the 360/370 is. We clearly have to have a better party line.

I suspect we're all going to put a set of slides together to explain the 11/70...I am. Is there anything to be gained by making a set for engineering presentation (I've never used any of the 35mm ones, which I assume exist and are prepared for sales)?

My set (which I presume I'll have to make up) will have the benchmark tables and graphs, Bill Strecker's graphs (properly acknowledged) on our choice of cache size, details on the machine (PMS) structure with datapath widths and information rates, some charts giving key statistics: #IC's, technology, words of microcode, boards, speed, possibly prices. These might even be compared with some other models (I have most of data). IAS graphs hopefully give performance. Some key features on what is significant about machine: i/o throughput, RAS, floating-point, and IAS. Also, we could relate it to 11/45 (and its data) if this would be wise. We need a slide to summarize it re 32-bitness.

What youse think?

GB:mjf

Distribution

1184

000554

SUBJ: WHITE PAPER NEEDED ON 32 BITS

PAGE 1
08-16-74
FROM: GORDON BELL

01778

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SUBJ: WHITE PAPER NEEDED ON 32 BITS, USER-MICROPROGRAMMING,
AND US

TO: Distribution

We keep getting asked about these issues; questions won't diminish. Let's understand what we're going to say. The problems seem to be: 16 vs 32; data-types; concern over implementation; larger programs; user microcode; and education/pr.

The Issues seem to be;

1. 16 vs 32 (or possibly 24), We were wrong before in not coming around faster to the issue of word length when the 12 bit machine was competing with the 16 bitters. I don't think 32-bits is the same fundamental issue. In the previous case, IBM had turned on to 8-bit characters, and people didn't think they could pack characters efficiently in 2 12-bit words. Also, whereas the 12-bit machine is really optimal for 4K memories, memory sizes are now larger, and users thought they were losing some efficiency on greater than 4K systems.
2. What do you mean a 32-bit machine? PDP-11 is not word length sensitive in the same way that older machines were, because it is really variable length in both data types and instructions.

Instructions are 1, 2, or 3 16-bit words long, with the usage being 1.6 to 2.0 words/instruction.

As for data types, we provide 8-bit bytes (used as characters, bit-vectors, and integers), 16-bit words (used as bit vectors and integers), 32 bit floating point (with 25-bit integers mantissa and an 8-bit exponent), and 64-bit floating point for high precision operations. In some of the applications, I've seen the 11 misapplied by using programmed double precision arithmetic, where the customer needed 24 bits of

SUBJ: WHITE PAPER NEEDED ON 32 BITS

DATE:
FROM:PAGE 2
08-16-74
GORDON BELL

01779

precision, instead of using the floating point. The reason presumably is the cost of the floating point, but our miseducation of him loses in these ways: It's slower; it takes more instructions to handle the scaling; and it takes longer to program because of the care needed in the scaling of numbers; also with improper care, accuracy can be lost easily.

3. Implementation versus the user instruction-set. A user should not care how we implement a machine, unless it affects his use in some way. As long as a machine has the proper facilities, it could be implemented in any word length (including 1-bit serial), and the buyer is free to pay his money and take a choice of performance. In essence, the sophisticated user only worries about whether a machine has the right data-types for his job; the speed a given implementation interprets (operates on) these data-types (or higher level language); and how a program fits into the facilities we provide.

In essence, users should have stopped worrying about implementation long ago.

4. Real Issues. The issues of a 32-bit or larger implementation seem to be:

Cost	Generally larger, but if error correction must be in memory, it's a cheaper memory.
Band width for I/O, etc.	2X
Band width for 32-bit integers, floating point	2X
Performance for Instruction-set	Perhaps 1.5

or conversely, for a given performance level a wider word machine might be cheaper.

Data-types for an 11 must solve addressing and data-

SUBJ: WHITE PAPER NEEDED ON 32 BITS

DATE:
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08-16-74
GORDON BELL
01781

- A. Implementation--32 bit memories (who cares)
- B. Data-types--we are currently only remiss in 32-bit integers, but he should probably be using floating point (maybe important for address arithmetic too).
- C. Address-space (logical address)--some competitors don't do any better than PDP-11, e.g. Modcomp (except they do provide full 65K words). In the future, we may have to adopt a different solution to increase task sizes beyond 65K bytes or 65K + 65K if we utilize I and D space.
- D. Memory Management--they don't understand that large memories doesn't don't solve this problem, but creates it. Having a large, linear address space while solving a small problem (physical memory size) just creates a bigger problem (how are multiple programs or multiple tasks placed in the memory with protection and sharing?)
- E. Physical memory size--easy to increase. Our processors have been probably overpowered for the small memory size. IBM believes 1 instruction/sec, requires 1 byte of memory. By this token an 11/40 would need about 256K words, and a 45 could take maybe 2-3 times this. A slow KA10 performs at about 11/45 speed and is relatively balanced at a user space of about 400K bytes.
- F. 32-bits as a memory bandwidth solution--it helps a bit. This can be solved by higher speeds and more parallelism in the structure (e.g. multiport memories).
5. The 11/55 is a 32-bit machine by any reasonable criteria. The 11/55 has 32-bit data-types, instructions, and most data paths. The fact that it has a 16-bit UNIBUS for some I/O is irrelevant unless it affects performance of some I/O. It shouldn't, because the high performance I/O is handled direct to memory through other MASSBUS controllers.

By increased physical memory, systems can be balanced with proper I/O, and physical memory to absorb the processor capacity. While we may not support I and D space to give the user somewhat larger programs, more programs and/or tasks can be run in parallel because memory can hold them. Our monitors are all multiprogrammed and/or multitasking and have overlays. These address the large program issue in many respects better than competitive monitors.

000556 types for this implementation.

A buyer may thusly emphasize:

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SUBJ: WHITE PAPER NEEDED ON 32 BITS

DATE:
FROM:PAGE 4
08-16-74
GORDON BELL

01782

6. The 11/55 cache as an answer to problem of getting performance automatically without user microprogramming. Also it finds important time consuming a parts of program without user analysis and program movement,

7. User microprogramming and the 11/45 bipolar. We've done an abysmal job of selling the 11/45 bipolar here as the answer to user microprogramming. The microprogrammers fall into 2 camps; experimenters with concept; and people who see it as a fast machine they need. A reasonable sales/promotion strategy can win them both.

Performance increase through microprogramming is predicated on the fact that a small physical part of the program is executed most of the time, hence can be placed in a small memory.

The Issues I see:

- A. Speed. 11/45 bipolar generally faster than user microcoded machine.
- B. Speed for floating point. Both 40 and 45 are faster than general purpose microcode machines.
- C. Programming use. User microcode requires different assemblers, compilers, etc. For high performance unencoded microprogramming (i.e. horizontal microprogramming, as it has been erroneously named), it is possible to affect the machine part.
- D. Program size--small for user microprogram scheme.
- E. Analysis of what to microprogram is difficult and maybe counter intuitive. User must always be re-coding program. With the 11/45 the same, PDP-11 instruction-set is used for bipolar and regular memory, hence the decision is not a major one requiring a different program, programming techniques, system software, etc.
- F. Applicability to higher level programs. The 11/45 scheme works for FORTRAN, COBOL, etc. programs. Namely, one finds the part of program that needs to be fast, and proceeds to place it in the bipolar part.
- G. Memory management is created if user microprogramming really works. Suppose you multitask or multiprogram, then each

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SUBJ: WHITE PAPER NEEDED ON 32 BITS

DATE:
FROM:

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08-16-74
GORDON BELL

01783

program has corresponding microprograms. How do you segment, protect, etc, the micro-programs?

In general, I believe the user wants and needs user micro-programming like a hole in the head. He does want performance, but a second instruction-set, associated programming problems, with special memory to manage seems like a high price to pay.

H. User education, what do the brochures look like for the 55? Can we replace 45 bipolar and target user microprogramming and/or sell the 45 performance?

How is the 45 promoted now that the PL disappears?

GBimjk

Distribution

PRODUCT LINE MANAGERS

Moore, Putnam, Hogan, Holman, Jacob, Lane, Long,

- John Buckley
- Janice Carnes
- Dick Clayton
- Bruce Delagi
- Bill Demmer
- Robin Frith
- Bob Gray
- Len Hughes
- Ted Johnson
- John Jones
- Bill McBride
- John Mistalek
- Craig Mudge
- Al Ryder
- Bill Strecker
- Pete Van Roekens
- Larry Wade

Long, Marcus,

Michels, Shields

Spector, Vachon

D I G I T A L

INTEROFFICE MEMORANDUM

SUBJ: EXTENDING VA SIZE

DATE:
FROM:
EX:
MS:

PAGE 1
10-01-75
GORDON BELL
2236
ML12/A51

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TO: FILE
* * * * *

Subj: EXTENDING VA SIZE ON 11'S VIA MACRO AND FORTRAN

To: Distribution

Is it totally impossible to modify either RSX-11/M or D in such a way (which would impair memory protection) so that the user could change the address=space, thereby getting access to large arrays? In effect, a user would write in 1 or more of the KT registers so as to change what is mapped into his segment.

This could for certain well behaved programs temporarily alleviate the VA problem till VAX arrives.

GB:mjk

Distribution

-
- Ron Brender
- Janice Carnes
- Dick Clayton
- Dave Cutler
- Bill Demmer
- Ron Ham
- John Levy
- Al Ryder
- Pete Van Roekens

SUBJ: STAR SOFTWARE NOTEBOOK

DATE: 10-02-75
FROM: GORDON BELL
EX: 2236
MS: ML12/A51

PAGE 1

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TO: FILE
* * * * *

Subj: COMMENTS ON STAR SOFTWARE NOTEBOOK AND CONKLIN'S
CONCEPT FILE

To: Distribution F/U 10/10

Great! I'm delighted to see this written down, and like context. Already I'm confused. How do the 2 relate? I didn't see the Conklin document referred to in software notebook.

On notebook:

1. Can we really not support FPP or FIS in hardware in CM?
2. All documentation tends to be inefficient (redundant) and misleading resulting in much noise to user. Ideally, one would have a common set of modules which are put together to form manuals. In some cases these modules would be translated so that they could be read by the different users.

Already this writing has the problem. There are multiple, redundant sections and conflicts (inevitably) between the sections. Can't you use more pointers in the text? I don't know how to deal with this, but with modern editors, computers, etc., we don't have the excuses we once had. Can we use all this technology to help us? Where is the hardware reference manual?

Also, I would push to have Soft. Eng. do as part of its effort, all the standard stuff (e.g. Command Language, BASIC) reference manuals!

In general, I believe low level language training manuals are outside STAR scope.

3. Demand paging policy maybe right since we feel comfortable with it. The interesting thing is that according to many studies, demand paging performs better than human controlled paging, and only 10-20% worse than the best possible page allocation to the working set.

SUBJ: STAR SOFTWARE NOTEBOOK

DATE:
FROM:PAGE 2
10-02-75
GORDON BELL

(conklin's levels of support seem somewhat in conflict...but I agree with him).

It seems we should really stress proper measurement and specify the working set so that it can be managed by the system. These parameters would be given to the system to manage by. Thus, there are 3 levels of working-set management: properly measured + specified; human-guess (RSX as we do now); and demand--system has to decide.

4. I'd like to see a goal that different languages can communicate with one another in some way.

5. Some accounting schemes:

Account for Virtual Memory space, not real memory space. Which is better?

Conklin's Concepts:

1. I like the definitions of Sect 3.18. They're not in front or called that. I would like to take all the definitions to a module that might eventually be a manual. Any manual that needed specific definitions could use them. This way we'd avoid double meanings and not getting a good set of defs! This would be a simple way to start using the module concept outlined above.
2. Facility--by using this name precisely are we over using a word?
3. Will there be static binding of some procedures? In this way, we have something that's really (almost) an opcode. The code would be globally shared.
4. Subset handlers, etc., by conditional assembly. Will there be an effort to do this? Should there? Or as we make smaller systems, do we just rewrite the code leaving a function out?

GB:mjk

Distribution

Dick Clayton
Pete Conklin
Bruce Delagi
Roger Gourd
Len Hughes

01836

digital

INTEROFFICE MEMORANDUM

TO: Dick Clayton
Steve Teicher

DATE: October 13, 1975

FROM: Gordon Bell

DEPT: 00D

EXT: 2236 LOC: ML12/A51

SUBJ: UNCONTROLLERS ON LSI-11 BUS

F/U 10/17

I'm really distressed at the planning part of LSI-11. It seems we're well on our way to competing with all PDP-11's at what, I fear could be higher basic prices. As you've successfully worked the problem of getting boards into production, it seems like all groups (disks, tapes, COMM, Clarke) are off inventing new options.

For many peripherals, e.g. the RK05, TS03, the bus cost differential doesn't justify a new controller. On these larger peripherals, why not use the UNIBUS control and an LSI/UNIBUS connector? How can we bound this problem?

GB:mjf

SUBJ: VAX-11 REVIEW

DATE: PAGE 1
FROM: 10-15-75
GORDON BELL
EX: 2236
MS: ML12/A51

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TO: FILE
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SUBJ: REVIEW OF REMAINDER OF VAX-11

To: VAX System Reference Manual Holders

The first revision of the remaining chapters of the VAX-11 system reference manual are attached. They are the operating system interface chapters. Please understand that they are not in as final form as the user interface chapters, which we sent out 29 September. However, we think it is important to get them out for review and feedback. The chapters and status are:

- 5 Memory Management Correct except for MUT but not polished
- 6 Exceptions and Interrupts Correct and polished.
- 7 Process Structure Not correct.
- 9 Input/Output Correct

Please replace your existing table of contents and index with the attached and insert chapters 5-9 in the proper place.

* Confidentiality of the document is most *
* important. To this end, please send back the *
* attached receipt to indicate that you have your *
* COPY. *

We are asking for written feedback to me by 31 October. In order to obtain the most meaningful comments, we are asking the same groups to review the document. However, the review of these chapters will occur after a second revision is distributed.

SUBJ: VAX-11 REVIEW

DATE:
FROM:

PAGE 2
10-15-75
GORDON BELL

Group	Individual
-----	-----
Components	Bill Hosan
CSS	John Holman
Business Products	Irwin Jacobs
LDP	Ed Kramer
Trad. + Typeset	Bob Lane
OEM	Bill Long
DECCOMM	Julius Marcus
EPG/ECP	Charlie Spector
Industrial	Brad Vachon
DECsystem 10	Tom Campbell
PDP-15	Dick Devlin
Hardware Implementation	Len Hushes
Software Architecture	Pete Conklin
Star Marketing PSG	Al Avery
Operating Sys. Design	Dave Cutler
R&D	Dick Eckhouse
Languages & Data Mst.	Ron Ham
Applied Programming	Ed Fauvre
Software Dev. Methods	Bill Slack
-11 Compatibility	Tom Rarich
Diagnostics	Ed Kenney
Field Service	Res Bursess
Manufacturing	Ken McNaughton

01852

Gb:mjf

To: Mary Jane Forbes

ML12/A51

P100
99P9999

I have received the additional chapters (5,6,7,9) of the
VAX System Reference Manual for review.

Signed

Copy #

10/16/75

01853

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ANTON, ED	ML3-5/E35	106	
ARMSTRONG, BOB	ML3-5/E35	#1	
AVERY, AL	ML3-5/E35	2	
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BELL, GORDON	ML12-1/A51	4	
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WONG, JOHN	ML3-5/E35	91	
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ZINS, ART	ML21-4/S17	93	

01854

SUBJ: BUSSES

DATE: 11-04-75
FROM: GORDON BELL
EX: 2236
MS: ML12/A51

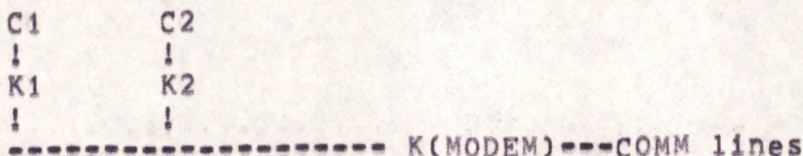
PAGE 1

TO: FILE

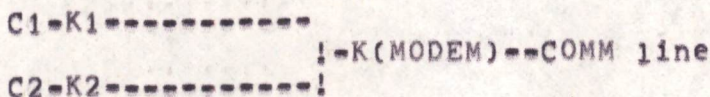
SUBJ: DESIGN OF PERIPHERAL BUSSES TO ATTACH TO MULTIPLE CONTROLLERS FOR HIGH RELIABILITY SYSTEMS-----FU 11/10

To: Distribution

BEN Barker of BBN described an interconnection mechanism they used on their high speed IMP. Here, they wanted two paths to the same communications line (modem) from two separate computers (C1, and C2), and their respective controller K1 and K2. They accomplished it by regarding the modem input cable to be either a bus, or two radial lines feeding from the modem (essentially a bus). Either one of two controllers (K1 or K2) could drive the modem (as long as they both didn't and they both could sense the modem's signals. The schemes:



and



The second scheme had the advantage that a controller could be taken out and worked on without interfering with the other controller to modem link (transmission). This scheme would (should) work fine for our systems--given that the bus and controllers are designed properly. Note, nearly all our busses (e.g. Sercon, Massbus, Serial Bus, RSL Bus, and modems) could operate this way.

How many busses can operate this way? Should we? On what?

FORM 89-10
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SUBJ: BUSSES

DATE:
FROM:

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11-04-75
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01939

By doing so, we automatically get redundancy w/o extra hardware (aside from second controller).

GB:mjf

Distribution
Armstrong, Bob
Avery, Bill
Bastiani, Vince
Bauer, Paul
Cady, Roger
Clayton, Dick
Demmer, Bill
Eckhouse, Dick
Fagerquist, Ulf
Feindeisen, Heinz

SUBJ: BUSSES

DATE:
FROM:

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01939

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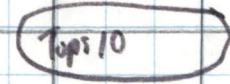
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Holman, John
Hughes, Len
Lignos, Demetrios
Marcus, Julius
Peyton, Bob
Rodgers, Dave
Saviers, Grant
Teicher, Steve
Wilhelm, Fred

Comput. Interactive RT

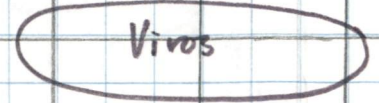
Comp. Int. RT

Comp Int. RT.

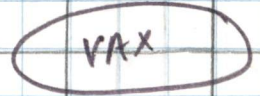
10-series
(incl KL10)



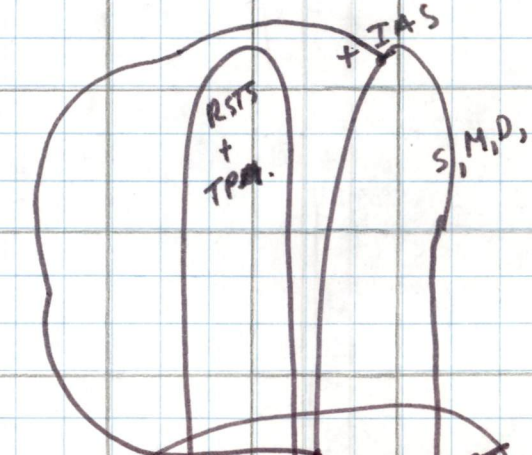
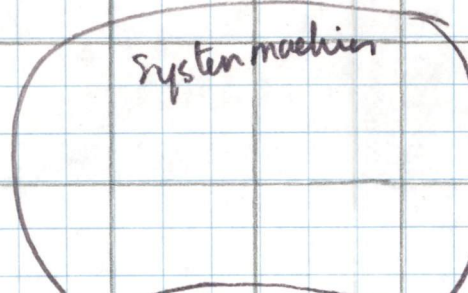
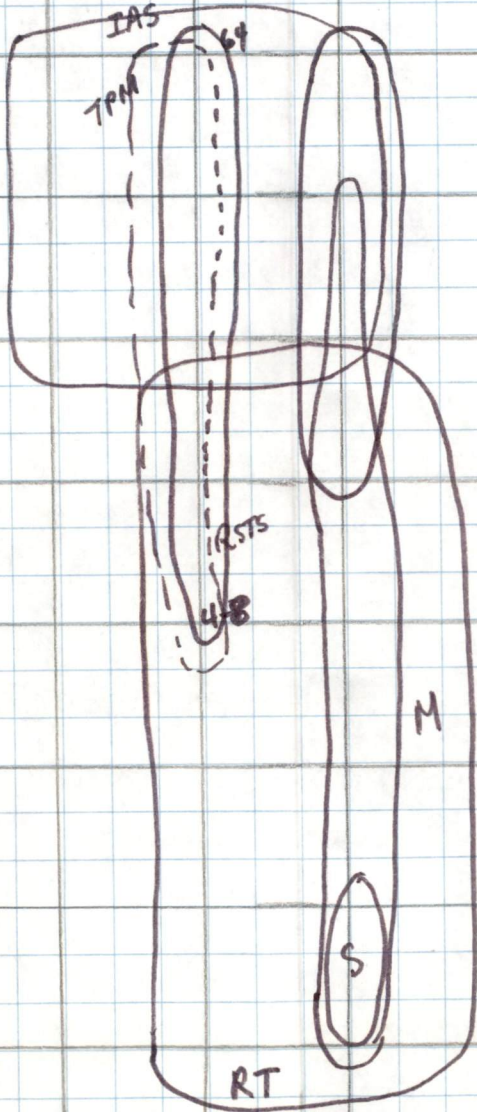
20-series
(incl KL20)



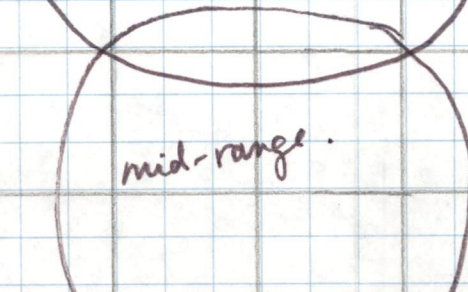
VAX 1st
ship



70

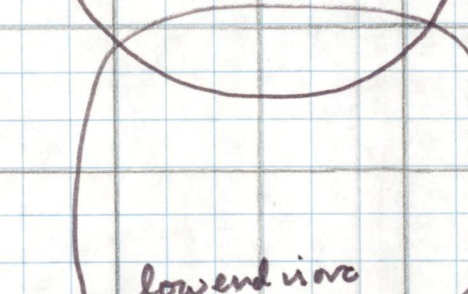


45



PDX

40



34

05

04

03

Personal-Satellite system
Hardware - ~~is~~ Oriented

Software - ~~is~~ Oriented

02030

From: GIDEON YUVAL (C300GY20)
Date: 30 Dec 1975 1726 EST
Subject: for your comment
To: GORDON BELL, DAN SIEWIOREK

G.Yuval,CMU,15213

REPEAT

In the good old days, every other computer had a 'repeat' instruction (i.e. a hardware 'do'). These repeats are all gone; I don't know who killed them (the interrupt? but I think the repeat is a very good thing to have;

Computers spend 70-95% of their time fetching instructions, on any microprogrammed machine with an instruction register (e.g. 11/40, eclipse) a repeat can be implemented by inhibiting the fetch. Therefore, a repeat should beat cache memory in both speed and cost.

The usefulness of a single-instruction repeat depends on the ISP architecture; a PDP-11 repeat can do Gaussian elimination, while a NOVA repeat can have logic decisions in it (if the 'skip' field is interpreted appropriately), a two-instruction repeat is likely to be much more powerful, but it needs special micro-hardware.

TO: VAXA Delagi, Hughes
I agree. Even better on VAX now.

JBell

+ return

02094

DIGITAL INTEROFFICE MEMORANDUM -->FILE COPY

SUBJ: BLISS

DATE: 16-Jan-76
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51

PAGE 1

To: Larry Portner

ABSTRACT: Re your BLISS memos on programming language.

F/U 1/16

Great!

1. I've come at this independently due to the prodding from Bruce on transportability of code from the 11 (especially diagnostics) to VAX. It's not clear yet how easy it is, nor how much Compatibility Mode will get us. Since Compatibility Mode will ultimately go, we have a problem to not support it for new code.
2. With 3 major product lines to support, I get terrified (Intel 8080, 10, 11, VAX). We need a policy!
3. There are 4 potential levels of programming: microprogramming, assembly (including the Intel 8080 microprocessor), BLISS, and Applications Language. The situation (problem) is outlined in the attached sketch, which might ultimately show a crystal clear policy (whatever it is).

I don't care particularly what it is, given that it makes sense, but I would favor something along the lines we came up with about 3 years ago (also attached):

0. Specify overall availability of tools plus where we're headed to improve them.
1. Standard Microprocessor (Intel 8080). Programming in the Intel supported language PL/M (a PL/1 subset) to specify the algorithm, debug the problem and finally document the design. If the program speed is unsatisfactory, recode that portion (estimated at less than 5%) to speed it up. If space is a problem, recode to increase space efficiency. For low volume products, there should be no recoding to save space. (At some point, if the semiconductor industry standardizes on PL/M, we may want a superset on the LSI-11 to capture their users!)
2. Microprogramming. (e.g. IMP, WD-chip set, 11/04 microcode) Use only the standard microassembler developed by the programming department. The microprograms that define our machines have to be better designed, documented, maintained, etc. (Also make programmers available to work on microprograms as needed.)

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3. New programs in assembly programming languages should be minimized. (There is a dangling issue here of the syntax for the VAX assembler.) I assume there is a conventional syntax looking assembly language for VAX, which can take programs which have been coded in PDP-11 by the proper coding conventions and assembled to run (not in compatibility Mode) on VAX. Right now, we need a statement on this so that we change 11 assembly language conventions to give us VAX assembly output...with no diddling in VAX mode.
4. BLISS subset. The bulk of all systems programs, operating systems, language compilers, interpreters, file systems, will be done in the BLISS 10/11 VAX subset, unless otherwise specified. There needs to be a fast, simple code producing compiler to avoid using large machines so heavily--and to produce less obscure code.
5. Applications programs. Only in the subset available on all DEC machines. In essence this should become the preferred programming level and in the future clearly the most used. If there are language deficiencies (e.g. strings in FORTRAN) that would greatly enhance our productivity, and ability, then consider as such. This is the preferred level of programming and it should be done for all applications, utilities, and source system programs.

I would like to get a completely global policy from you soon that encompasses all programming from microprogramming, microprocessors, systems, and applications programs which has been generally agreed to everywhere (including diagnostics, PL's) so that the troops know where we're headed (i.e. I understand where the troops are headed).

Let's set a date to bounce off OOD staff soon.

GB:mjf

Attachments

cc: Bruce Delagi, Ed Fauvre, Roger Gourd, Ron Ham, George Plowman, Larry Wade

Language	Target Machine	CM-compat. mode ?- need <u>statement</u> .	I - identity by design No - no plan or effort.
OLD			VAX Q142
Macro-10	I	No - very different due to registers	No - at least same # of registers
11	No - somewhat possible by hand	I	CM + Reassembly with hand recoding ?
BLISS 10	I	No - hard due to # registers & data structures.	?
11	No - is it easy?	I	} Goal to do - at least using CM.
10/11	I (none exist)	I yet, although proposed	
Applic. 10	I		
(?) - use language as vehicle	11	I	
New			
Macro 10	I	No - VAX not worthwhile	? no could be useful migration to VAX.
11	No - not worthwhile migrate upward	I	(avoid CM) →
(??) VAX	No - not worthwhile migrate upward	← Establish NOW!!	this as a constraint → I
BLISS - 10	I		
Combine as one standard? VAX	11	No - ?	Establish as a constraint now) → I
	VAX	No - ?	
(Preferred) 10/11/VAX	I	I	I
See Portner policy. 10/VAX	I	?	I
Applic 10	I		
? - use language to standardize VAX	11	I	I urgent!

SUBJ: CODE SHARING

PAGE 1
DATE: 20-Jan-76
FROM: GORDON BELL
EX: 2236
MS: ML12/A51

ABSTRACT: CODE (PROCEDURE) SHARING WITHIN VAX

To: Distribution

F/U 1/25

A key goal we had when designing the hardware: programs would be shared widely within the VAX environment.

1. On a long term basis by eliminating much of the machine registers idiosyncrasies by the call mechanism...hence, a procedure would be easily shareable. (Hopefully ever across some languages.)
2. Within a single operating environment by properly positioning it in the right access level so that it could be used by another program.

What is being done in the first category to make this sharing really happen? Should we look at these procedures as being extensions to the instruction set?

What is being done about the second category?

What is the policy or goal now? How is it being implemented?

GB:mjf

Distribution

Peter Conklin
Dave Cutler
Roger Gourdcc: Vax A, Bruce Delagi, Ed Fauvre, Ron Ham,
George plowman, Larry portner, Larry WadeFORM 8310
HO
PRINTED IN U.S.A.

SUBJ: MULTIPROCESSOR GOALS

DATE: PAGE 1
 29-Jan-76
 FROM: GORDON BELL
 EX: 2236
 MS: ML12-1/A51

ABSTRACT: Multiprocessor Goals for RAS and Performance for
 FY77 Red Book (Draft) for Comment

To: Distribution

The following document outlines broad goals for the design of certain existing and new systems. It is meant to be used as a request to assess impact on budgets, schedules, manufacturing and field service costs for new products as the Red Book is updated.

Background

The Multi-processor Task Force has been investigating our past history, current feasibility, desirability and strategy for multi processors. Although there is not yet a clear strategy, we have explored alternatives based on our findings, but generally concentrating on the short term. The market, technical, and what they provide aspects are given in the appendix.

Although the strategy is far from complete, I want to establish broad goals as we go into the Red Book update process.

Applicability

1. RSX-11/M+S - ASAP, especially to support CSS multi-port primary (i.e., multiprocessors) and secondary memories. (F.C.S within year on 11/40, 45 and 11/70 when available)
2. RSX-11/D and IAS - ASAP, to support CSS multiport 11/70 (FCS approx 2 years).
3. RSTS - ASAP.
4. VAX - 1 Bus, multiprocessor system, and basic design for multi-bus (multiprocessor) systems when multiport memories are available.
5. RT-11 - Assess possibility/applicability - but mainly for performance.
6. Hardware configurations support implied

Model

Processors

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29-Jan-76
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03,04,05	1
34	3-(on 1 Unibus)
	8-(on 4-part memory)
40,45,50,55	4 (on 4-part memory)
PDQ	2/Unibus
	8/4-part memory
70	4-(on new CS 4-part 32-bit memory)

7. Other hardware support implied

4-part memories (implied above)
2-part Massbus peripherals
DT03 Switch
Bus window (withdraw)
Links (covered by DECNET)

Goals

0. The key aspect of availability must come from the detection of failures. This in turn implies data errors will at least be detected (e.g., simple parity), but the goal should be to add sufficient data redundancy such that these errors are corrected. Overall, in the future it will be easier to detect all failures by redundancy, including the construction of checking processors. There should be no storage processing or transmission of data without checking.
1. Assume all components must be operational to be available as the basic system (Fig. 1). All single bus systems can be configured for high availability by supporting n+1 running (powered) spare components for each type (Fig. 2). The component types, in order of decreasing failure rates for the subsystem (before redundancy is added) are:
- Terminals - the ability to ignore faulty terminals, and provide on-line diagnosis and repair.
 - Secondary and tertiary memories (i.e., disks and tapes) should include ability to ignore bad data blocks, remap them, and ignore complete.
 - Primary memories (MOS or core) - ECC should be added to all MOS systems, subject to low end cost compromises.

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This can, at the low end, take the form of remapping of words to avoid hard failures as detected by simple parity. Overall, the goal should be to first correct at the word level, then to ignore a block, and finally to ignore a module.

- d. Processors - The processor is usually the highest single failure rate after the electro-mechanical equipment, and as such should be backed up bus-type structure (e.g., Unibus or SBC busses)
- e. Redundant Controllers on single bus for controlling bussed secondary, tertiary and terminals (communications). The capability should be included, though undoubtedly may not be supported on single bus systems.

2. Multiple Bus-Type Systems

In general, the single bus systems have limited reliability which is bounded by the reliability of the single bus and its shared power supply (Fig. 2) cables and package. Multiple bus systems (Fig. 3) should include the following additional capabilities:

- a. Shared memories with their own power permitting (b):
- b. Multiple processors with at least one processor per bus.
- c. Controllers for secondary and tertiary memory and communications links (terminals) such that there are two independent controllers for these devices, although still a single point of failure in the shared bus (which, for some requirements, may be sufficient).
- d. Dual port secondary and tertiary memories which eliminates single bus as a point of failure. This also permits system repartitioning for diagnosis and repair of a single unit.
- e. Completely redundant subsystems (e.g., controller + disks).
- f. Switches to single sub-systems. In some cases a single point of failure might exist (e.g., a single comm. controller). The multiple bus structure necessitates a switching structure to avoid faults of a single bus and to permit reconfiguration for diagnosis and repair.

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3. Transparency to User - In the case of the file system for example, the operating system would manage the writing of redundant information on 2 independent disks.
4. Knowledge of R, A, S numbers by: designers, manufacturers, marketers, sellers, users. This would take many forms, including:
 - a. Calculated, and measured MTBF's, MTTR's for all components.
 - b. Calculated availability for all systems which the users would have as basis of configuration design.

5. Cache Structures

Design all subsequent multiprocessors with a cache structure on the basis that there can be differences in data among the various processors. That is, these multiprocessors should not be structured to have either a central cache or $n/2 \times (n+1)$ interconnections among the caches since these designs ultimately fail by only providing the performance of 3 or 4 processors, independent of the number of processors actually used. There must be proper instructions in the ISP (e.g., lock, B and V, access of shared segments), and design of the operating systems to permit correct operation.

SUBJ: MULTIPROCESSOR GOALS

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GORDON BELLAppendix: Market, Technical, and What They Provide

1. Market -

Of the 100+ multi-computer systems we sell per year, 75% are for high availability and 25% are for high performance. Already some of these systems are true symmetrical, multiprocessor structured (versus multi-computers)...this only reflects the unavailability and non-support of hardware, not a technical issue. We would expect a switch for other reasons - see below.

- a. About 10% of the PDP-10 systems are multi-processors. These are sold for: incremental performance improvement, maximum performance (i.e., compete with larger machines on the basis of total throughput), and for increased availability.
- b. There are several "new competitor" companies introducing high availability computers. We would expect this, as new ideas tend to originate in smaller, new companies.
- c. The recent Honeywell mini is multiprocessor based.
- d. Many old line companies are there (e.g., Univac and Burroughs).
- e. IBM is clearly going to base their next product on this technique.
- f. Our users, the field and several products lines are pushing.
- g. There is no training for users as most of the systems we sell are multiprogrammed. Multiprocessing doesn't present a different change in use or understanding.

2. Technical

- a. There is no technical risk in the area of interest (2 to 8 processors) because of the current systems use. The addition of physical processors does not increase any dimension of risk or understanding.
- b. All multi-process operating and multi-user systems (e.g., RSTS) are conceptually able to accept multi-processors,

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although only RSX 11M provides for them with little or no modifications.

- c. The hardware technology to permit multiprocessors is clearly here. The lower percentage of the system cost being concentrated in the processor while the largest part of the design cost argues strongly for multiprocessors. The 1 chip processors will force everyone to multiprocessor-based structures, and this is already occurring from various microcomputer structures being built.
 - d. The software technology has been proved countless times (e.g., Burroughs, Univac, Honeywell, IBM, Bell Labs, CMU, DEC10, RSX-11/M (Eckhouse version)).
3. What we expect multiprocessors to provide (to users) that current systems don't:
- a. Availability - Ability to configure systems with arbitrarily high availability and base for servicing on line. The goals outlined are oriented substantially toward high availability (performance is a side benefit).
 - b. Incremental performance improvement in the field permitting the user to balance a system. A user can relatively dynamically determine the performance for a given system. A processor is merely a simple extension of the inherent ability already provided to extend memory, disks, tape, terminals and other resources to operate a balanced system.
 - c. Higher performance - Given that we make a certain, high end processor, using up to 8 of them, increases the performance in almost a linear fashion.
 - d. Decreased inventory - Giving better corporate performance and user availability we make less parts and cover a wider range. Ironically, of the processors we sell now, the same performance range can be provided with about half the number.
 - e. Better fundamental processor designs by less designs...I would hope.

GB:lp

Attachment

02193

SUBJ: MULTIPROCESSOR GOALS

DATE:
FROM:

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29-Jan-76
GORDON BELL

Distribution

OOD

MP Task Force

Jega Arulpragasam

Bill Bazemore

Bill Demmer

Clay Neal

Mike Tomasic

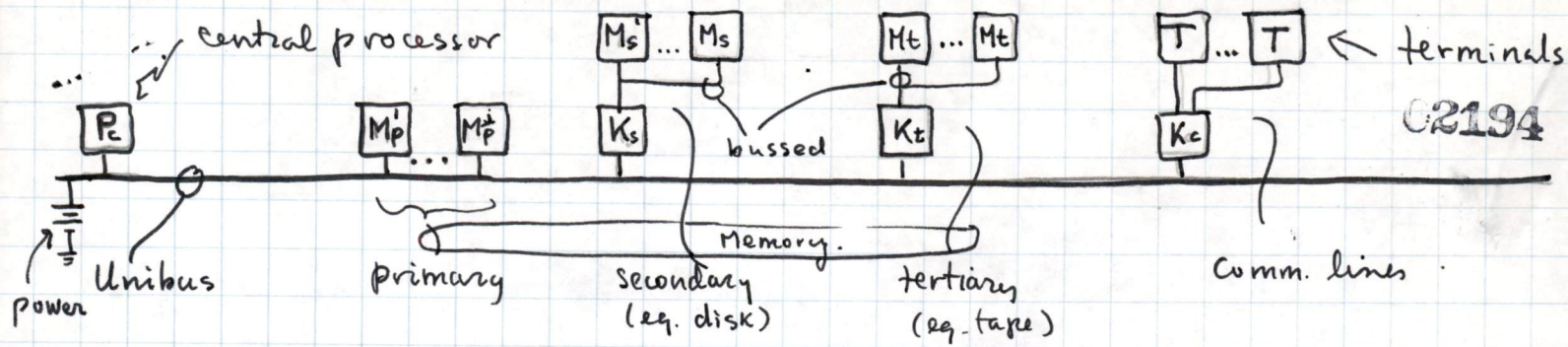


Fig. 1. Basic system: all ~~xy~~ components required for system to ~~ky~~ operate

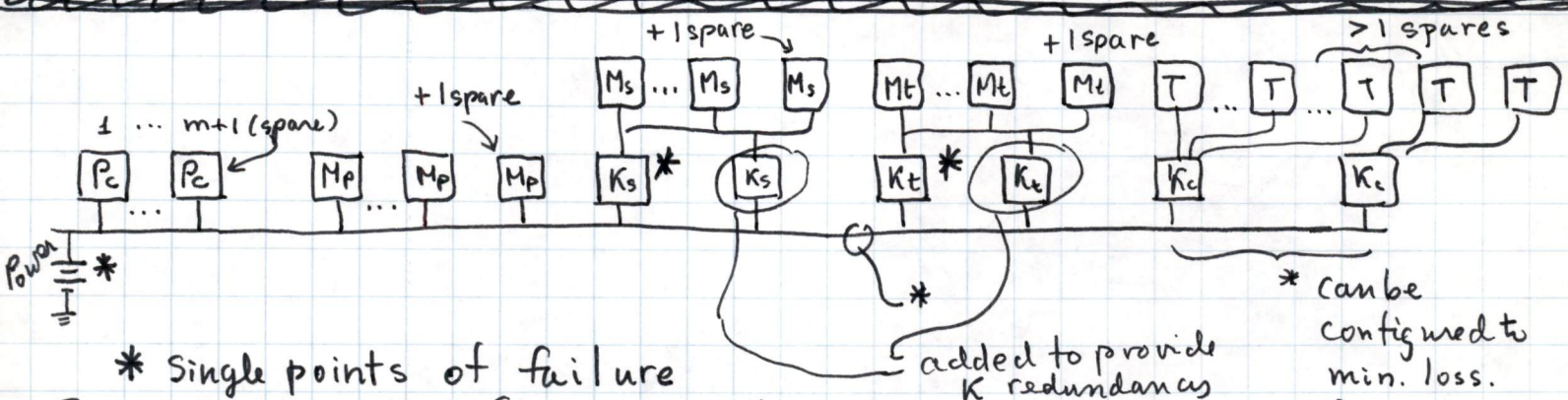


Fig. 2 Basic 1 Bus System with $n+1$ running spares for all sub-systems

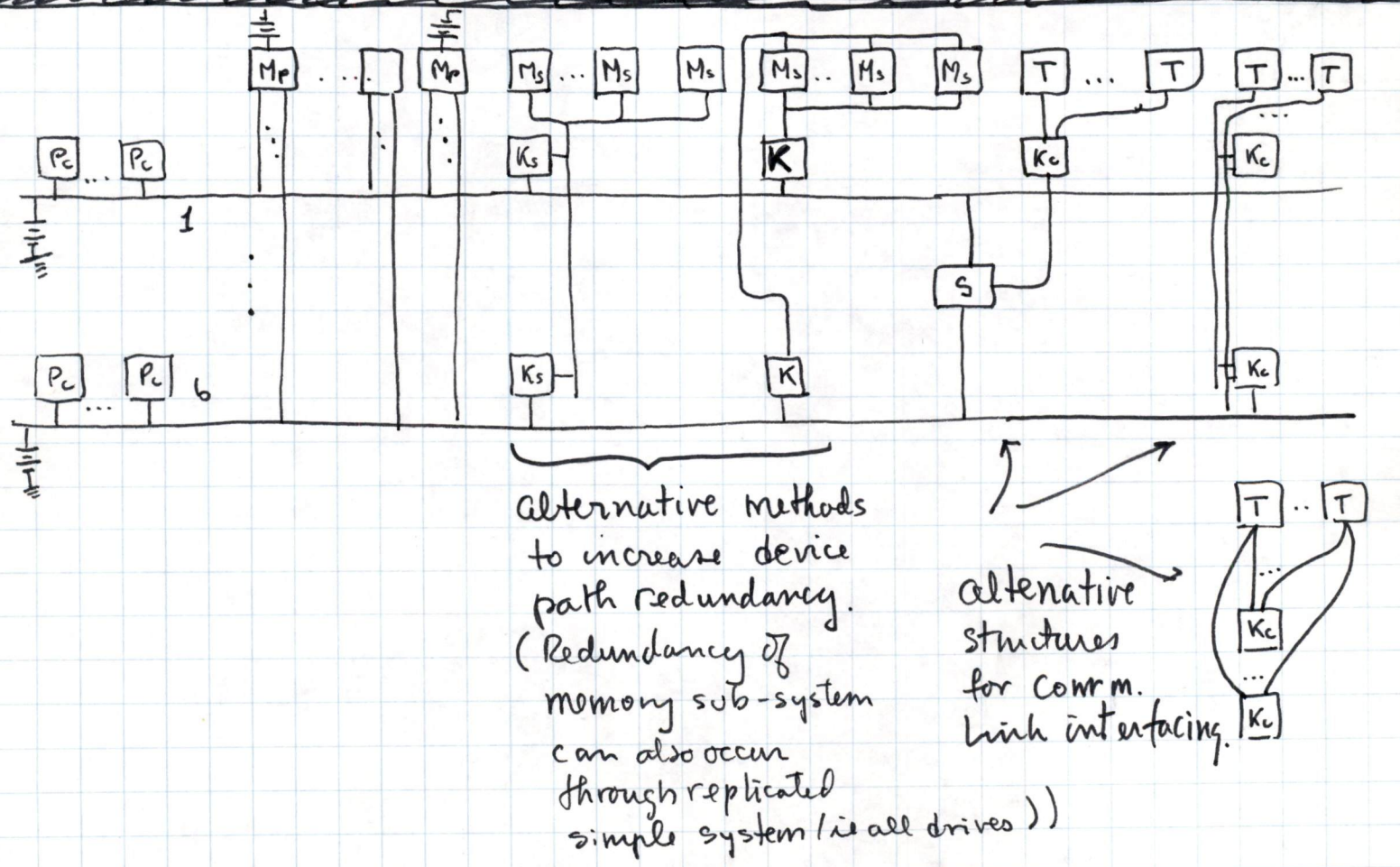


Fig. 3. Multi-bus System with $n+1$ running spares and no single point of failure

SUBJ: MULTIPROCESSOR GOALS

PAGE 1
DATE: 03-Feb-76
FROM: GORDON BELL
EX: 2236
MS: ML12-1/A51ABSTRACT: Multiprocessor Goals for RAS and Performance for
FY77 Red Book

To: Distribution

Current Mode of Operation

This document outlines broad goals for the design of certain existing and new systems. It is meant to be used as a request to assess impact on budgets, schedules, manufacturing and field service costs for new products as the Red Book is updated.

John Holz is assuming the role of Program Manager and will coordinate planning/budget issues.

Mark Uhrich of CSS is establishing a multiprocessor marketing group.

The Multiprocessor Task Force will continue to coordinate product direction within Central Engineering and CSS. (Charter available upon request.)

Background

The Multiprocessor Task Force has been investigating our past history, current feasibility, desirability and strategy for multiprocessors. Although the strategy will be refined and change, we have explored alternatives based on our findings, but generally concentrating on the short term. The market, technical, and what they provide aspects are given in the appendix.

Although the strategy is far from complete, this is an attempt to establish broad goals as we go into the Red Book update process.

MULTIPROCESSOR STRATEGY (Mark Uhrich-author)

Central Engineering and CSS are working closely together to implement such systems for both the long range and shorter term future. The general goal is that as multiprocessors become well established and higher volume, they will become standard products and the focal point will shift to Central Engineering. Thus CSS will be out of the business it currently supports by approximately 1979.

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Digital will implement PDP-11 based multiprocessor systems for both high availability systems and high performance systems. To date, the majority of CSS multiprocessors have been for high availability systems. Multiprocessors are also used to extend upward the power of the CPU family. Both market areas are expected to grow significantly in the future.

Central Engineering will be the focal point for implementing high performance multiprocessors for a long range goal. High performance multiprocessors using these systems are anticipated for the FY79 time frame.

CSS will continue to be the focal point for the implementation and marketing of high availability systems, until these become "available" as standard products. These systems are of lower volume and have specialized support requirements. CE is working on these systems as a long range goal. Thus, CS must start now.

CSS will also continue to be the focal point for the implementation and marketing of high performance systems prior to the implementation by Central Engineering. The CPU's involved include the PDP-11/35, 40, 45/FP11-C, 11/70 and near future processors. The strategy will be to identify specific processors for multiprocessing based on ability to implement, market need, and market impact.

Central Engineering, in conjunction with CSS, will work to implement software support for both high availability and hardware and systems. The RSX/IAS family of operating systems is initially targeted for this effort. Wherever possible, this software support will be included in the standard operating system releases.

CSS committed to strengthen and expand the family of multiprocessor products. This includes standardization of the production, use and support of the existing devices and the development of new products needed as part of the family.

The goal is to have these products and systems appear as much as possible like normal DEC products.

CSS will be working to give DEC multiprocessors greater visibility to the sales force and marketplace so as to enhance our ability to penetrate this marketplace. This effort will include advertising and may include specifically identifiable model numbers and marketing packages.

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Detailed Applicability

- 1. RSX-11/M+S - ASAP, especially to support CSS multi-port primary memories (i.e., multiprocessors) and secondary memories. (F.C.S within year on 11/40, 45 and 11/70 when available)
- 2. RSX-11/D and IAS - Highly desirable? ASAP, to support CSS multiport 11/70 (FCS approx 2 years).
- 3. RSTS - Highly desirably. ASAP. Assess.
- 4. VAX - 1 Bus, multiprocessor system at FCS; with basic design for multi-bus (multiprocessor) systems when multiport memories are available.
- 5. RT-11 - Assess possibility/applicability - but mainly for performance.
- 6. Hardware configurations support implied

Model	# Processors
-----	-----
03,04,05	1
34	3-(on 1 unibus)
	8-(on existing CSS 4-port memory)
40,45,50,55	4 (on existing CSS 4-port memory)
PDQ	2/Unibus
	8/4-port memory
70	4-(on new CSS 4-port 32-bit memory)

- 7. Hardware and its implied support.

4-port memories (implied above)
 2-port Massbus peripherals
 DT03 switch (redo to increase reliability).
 Bus window (withdraw)
 Links (covered by DECNET)
 Secondary Memories:
 A. Multiple controls can access a single RSL or RK06 bus providing computer and/or controller backup.
 B. Tertiary Memories--yes:

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C. Dual port RK06 support via two independent controllers.
COMM controllers--access to a modem by 2 controllers.

Goals

0. The key to availability is the detection of failures. This in turn implies data errors will at least be detected (e.g., simple parity), but the goal should be to add sufficient data redundancy such that these errors are corrected. Overall, in the future it will be easier to detect all failures by redundancy, including the construction of checking processors. There should be no storage, processing or transmission of data without checking in certain future systems.
1. Single Bus Systems (including multiprocessors sharing a common bus)--Assume all components must be operational to be available as the basic system (Fig. 1). All single bus systems can be configured for high availability by supporting n+1 running (powered) spare components for each type (Fig. 2). The component types (and priorities), in order of decreasing failure rates for the subsystem (before redundancy is added) are:
 - a. Terminals - the ability to ignore faulty terminals, and provide on-line diagnosis and repair.
 - b. Secondary and tertiary memories (i.e., disks and tapes) should include ability to ignore bad data blocks, remap them, and ignore complete.
 - c. Primary memories (MOS or core) - ECC should be added to all MOS systems, subject to low end cost compromises. This can, at the low end, take the form of remapping of words to avoid hard failures as detected by simple parity. Overall, the goal should be to first correct at the word level, then to ignore a block, and finally to ignore a module.
 - d. Processors - The processor is usually the highest single failure rate after the electro-mechanical equipment, and as such should be backed up bus-type structure (e.g., Unibus or SBC busses)

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- e. Redundant Controllers on single bus for controlling bussed secondary, tertiary and terminals (communications). The capability should be included, though they may not be supported on single bus systems.

2. Multiple Bus-Type Systems

In general, the single bus systems have limited reliability which is bounded by the reliability of the single bus and its shared power supply (Fig. 2) cables and package. Multiple bus systems (Fig. 3) should include the following additional capabilities:

- a. Shared memories with their own power permitting (b):
- b. Multiple processors with at least one processor per bus.
- c. Controllers for secondary and tertiary memory and communications links (terminals) such that there are two independent controllers for these devices. Although there is still a single point of failure in the shared bus, for some requirements, this may be sufficient.
- d. Dual port secondary and tertiary memories which eliminates single bus as a point of failure. This also permits system repartitioning for diagnosis and repair of a single unit.
- e. Completely redundant subsystems (e.g., controller + disks).
- f. Switches to single sub-systems. In some cases a single point of failure may exist (e.g., a single comm. controller). The multiple bus structure necessitates a switching structure to avoid faults of a single bus and to permit reconfiguration for diagnosis and repair.

3. Transparency to User - In the case of the file system for example, the operating system would manage the writing of redundant information on 2 independent disks. The goal is to permit a user to write programs with no knowledge of multiprocessors, and to be able to specify a level of availability independently.

4. Knowledge of R, A, S numbers by: designers, manufacturers, marketers, sellers, users. This would take many forms, including:

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- a. Calculated, and measured MTBF's, MTR's for all components.
- b. Calculated availability for all systems which the users would have as basis of configuration design. This will take the form of a standard program that a designer, user, salesperson, etc. can run which gives availability, cost, etc. data.

5. Cache Structures

Design all subsequent multiprocessors with a cache structure on the basis that there can be differences in data among the various processors. That is, these multiprocessors should not be structured to have either a central cache or interconnections among all the caches since these designs ultimately fail by only providing the performance of 3 or 4 processors (independent of the number of processors actually used). There must be proper instructions in the ISP (e.g., lock, P and V, access of shared segments), and design of the operating systems to permit correct operation.

In summary, we will not and should not design multiprocessor hardware assuming all caches "know" about each other's data. Hardware-assisted software will handle the interlocking of data such that "stale-data" in a cache does not give incorrect results.

- 6. Pays your money and takes your choice. In essence, we want to provide user with ability to design systems that are transparent to multiprocessors in such a fashion that he can independently buy performance and availability without reprogramming.

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Appendix: Market, Technical, and What They Provide

1. Market -

Of the 100+ multi-computer systems we sell per year, 75% are for high availability and 25% are for high performance. Already some of these systems are true symmetrical, multiprocessor structured (versus multi-computers)...this only reflects the unavailability and non-support of hardware, not a technical issue. We would expect a switch for other reasons - see below.

- a. About 10% of the PDP-10 systems are multi-processors. These are sold for: incremental performance improvement, maximum performance (i.e., compete with larger machines on the basis of total throughput), and for increased availability.
- b. There are several "new competitor" companies introducing high availability computers. We would expect this, as new ideas tend to originate in smaller, new companies.
- c. The recent Honeywell mini is multiprocessor based.
- d. Many old line companies are there (e.g., Univac and Burroughs).
- e. IBM is clearly going to base their next product on this technique.
- f. Our users, the field and several products lines are pushing.
- g. There is no training for users as most of the systems we sell are multiprogrammed. Multiprocessing doesn't present a different change in use or understanding.

2. Technical

- a. There is no technical risk in the area of interest (2 to 8 processors) because of the current systems use. The addition of physical processors does not increase any dimension of risk or understanding.

Although these systems will provide significant performance and availability over what we now have,

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it will be sometime before we fully understand how the inherent capability can be used to provide extremely high availability systems. We must take this first step to gain experience.

- b. All multi-process operating and multi-user systems (e.g., RSTS) are conceptually able to accept multi-processors, although only RSX 11M provides for them with little or no modifications.
 - c. The hardware technology to permit multiprocessors is clearly here. The lower percentage of the system cost being concentrated in the processor while the largest part of the design cost argues strongly for multiprocessors. The 1 chip processors will force everyone to multiprocessor-based structures, and this is already occurring from various microcomputer structures being built.
 - d. The software technology has been proved countless times (e.g., Burroughs, Univac, Honeywell, IBM, Bell Labs, CMU, DEC10, RSX-11/M (Eckhouse version)).
3. What we expect multiprocessors to provide (to users) that current systems don't:
- a. Availability - Ability to configure systems with arbitrarily high availability and base for servicing on line. The goals outlined are oriented substantially toward both high availability and high performance. It will be sometime before we fully understand or can specify the availability gains.
 - b. Incremental performance improvement in the field permitting the user to balance a system. A user can relatively dynamically determine the performance for a given system. A processor is merely a simple extension of the inherent ability already provided to extend memory, disks, tape, terminals and other resources to operate a balanced system.
 - c. Higher performance - Given that we make a certain, high end processor, using up to 8 of them, increases the performance in almost a linear fashion.
 - d. Decreased inventory - Giving better corporate performance and user availability we make less parts and cover a wider range. Ironically, of the processors we sell

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now, the same performance range can be provided with about half the number.

- e. Better fundamental processor designs by less designs...I would hope.

GB:lp

Attachment

Distribution

OOD

MP Task Force
Jega Arulpragasam
Bill Bazemore
Bill Demmer
Malcolm Johnston
Clay Neal
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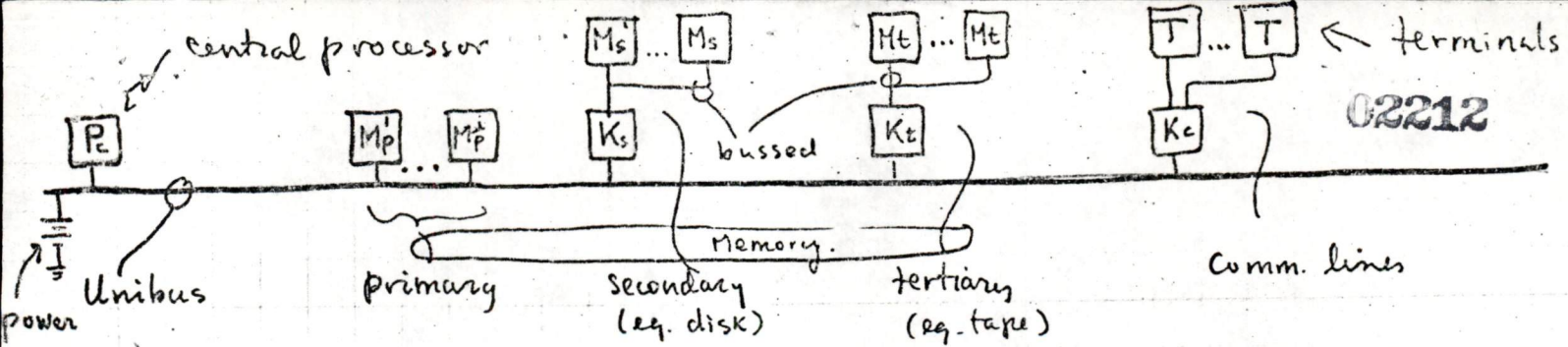
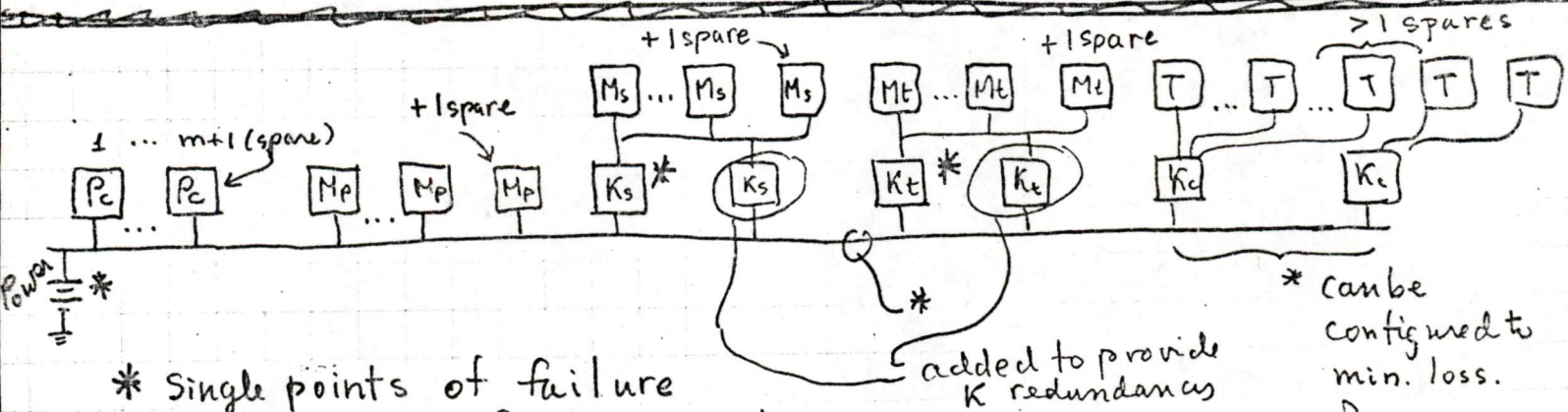
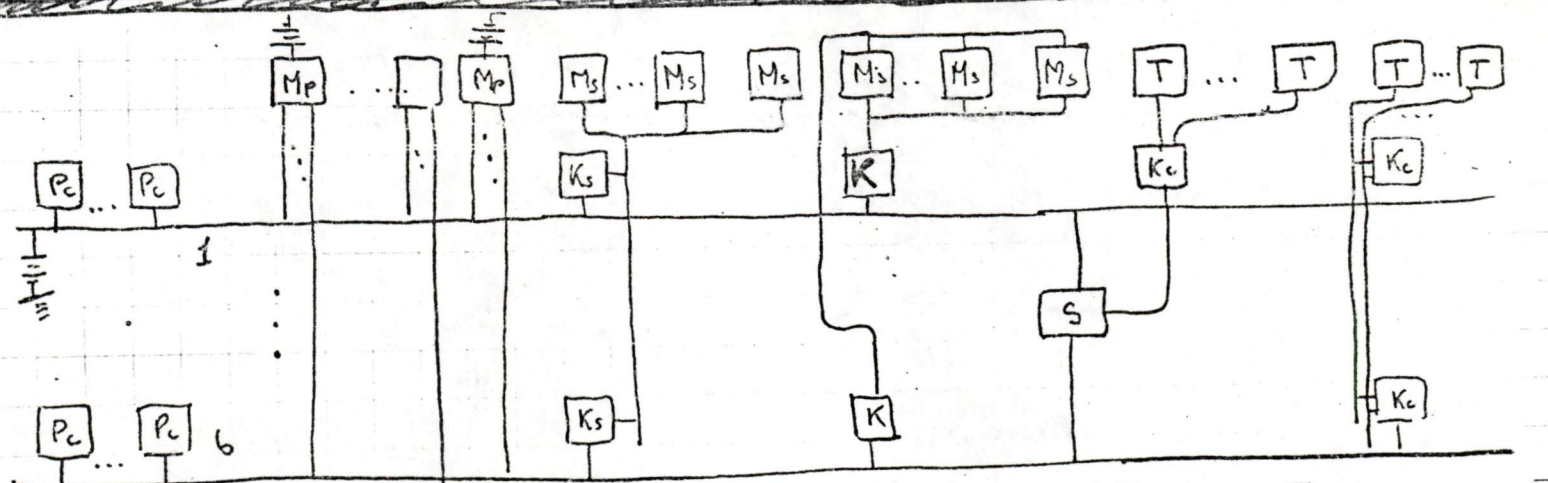


Fig. 1. Basic system: all ~~sky~~ components required for system to ~~ky~~ operate



* Single points of failure
 Fig. 2 Basic 1 Bus System with $n+1$ running spares for all sub-systems
 * can be configured to min. loss.
 * added to provide K redundancies



Alternative methods to increase device path redundancy. (Redundancy of memory sub-system can also occur through replicated simple system (i.e. all drives))

Alternative structures for comm. link interfacing.

Fig. 3. Multi-bus System with $n+1$ running spares and no single point of failure