TX-0, A Transistor Computer with a 256 by 256 Memory

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Synopsis: TX-0 is a high-speed digital computer which was built at Lincoln Laboratory to demonstrate and operationally test 5-megapulse transistor circuitry and a 65,536-word magnetic-core memory. The word length is 19 bits; 1 bit is a parity check bit for memory, 16 bits are assigned to memory addressing, and the 2 remaining bits are used to select among three memory-reference instructions and one micro-programming instruction. The logic is performed by standardized packages using surface barrier transistors. Fig. 1 shows TX-0 with the arithmetic element just beyond the console and the memory on the far left. Part I of this paper covers the TX-0 memory, and Part II the TX-0 circuitry.

Part I, The TX-0 Memory

THE TX-0 MEMORY, Fig. 2, is a high-speed, random-access, coincident-current magnetic-core unit with a storage capacity of 65,536 19-bit words. The bits in the word are read out in parallel, and the cycle time is 7.0 μsec (microseconds). (Cycle time is defined as the time between successive read operations.) Two 256-position magnetic-core switches are used to supply the read and write current pulses to selection lines. The memory system contains 425 dual triodes and 625 transistors. It is interesting to note that the presently available 4,000-register magnetic-core memories use almost as many active elements as are used in this 65,000-register memory. The memory was designed both electrically and mechanically so that the word length can be expanded to 37 bits. Two co-ordinates are used to select a register during the read operation, and three co-ordinates are used for writing. A 2 to 1 current selection ratio is used. A block diagram of the memory system and the timing diagram is shown in Fig. 3. The basic operation of this type of memory system has been adequately described in the literature and will not be repeated here.[1]

Memory Array

The memory array contains $1^1/_4$ million ferrite cores which were manufactured at the Lincoln Laboratory. The outside diameter of the core is 80 mils, the inside diameter 50 mils, and the height 22 mils. When driven with an 820-milliampere current pulse, the cores switch in 1 μsec and give a peak output voltage of 100 millivolts. The cores used in this memory have a somewhat greater signal-to-noise ratio than available commercial cores. The cores are wired into 64 by 64 subassemblies, each subassembly being a complete operating memory plane with its own sense and digit winding. The same winding configurations are used in the 64 by 64 subassemblies as were used in the previous memories built at the Lincoln Laboratory.[2] Sixteen 64 by 64 subassemblies are assembled in a square array and connected together to form each 256 by 256 plane.[3] The choice of a 64 by 64 subassembly size was a compromise between the number of soldered connections in the 256 by 256 plane and the ease of construction and test of the subassemblies.

The digit-plane winding in each 256 by 256 plane is divided into quarters, each quarter being made up of the digit winding of four subassemblies connected in series as shown in Fig. 4. Each quarter looks like a delay line with a characteristic impedance of 150 ohms

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Fig. 1. TX-0 computer

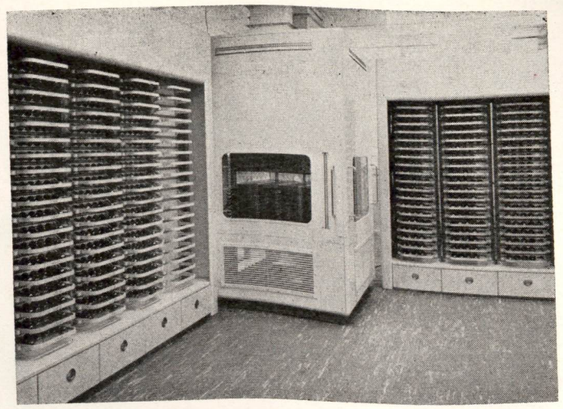


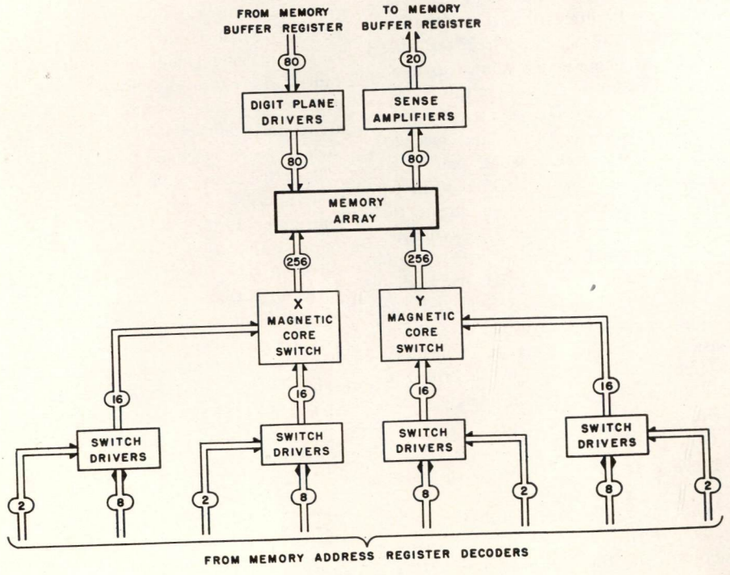
Fig. 2. TX-0 memory

and a delay time of 0.4 μsec. The choice of connecting only four subassemblies in series is a compromise between delay time and equipment. Any increase in digit-plane winding delay would result in an increased memory cycle time; for example, using one digit-plane winding per 256 by 256 plane would add 2 μsec to the cycle time.

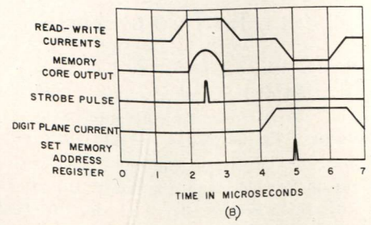
It should be noted that during the operation of the memory, it is practical to drive only one of the digit-plane winding quarters in a given 256 by 256 plane at any one time. When a pulse of current is supplied to the digit-plane winding the resultant voltages cause transient currents to flow through the interwinding capacities from the digit winding to the X, Y, and sense windings. If the quarters of all the planes are driven at once, the currents flowing through the interwinding capacities are of sufficient magnitude to cause distortion of the digit-plane current pulse, and to create undesirable transients on the sense winding. When only one of the digit-plane winding quarters is pulsed at a given time, these effects are not harmful.

The sense winding in a 256 by 256 plane is also broken up into four sections, each section consisting of the sense windings from four 64 by 64 subassemblies. The subassemblies on a given sense winding are connected in such a manner that no two subassemblies on the same sense winding section are common to the same X or Y drive line; see Fig. 5. It should be noted that with this method of connection the voltage induced in the sense winding by the half-selected cores is equal to that induced in a 64 by 64 memory.[4] Each sense winding is also a delay line. To reduce the delay and resultant signal distortion, the four subassemblies on a given sense winding section are connected in series parallel as shown in Fig. 3 rather than in series. Of course, this type of connection halves the signal amplitude seen at the output terminals of the sense winding section.

Twenty 256 by 256 planes are stacked on 1/2-inch centers and the X and Y wires are connected in series to form the complete memory array; see Fig. 6. Nineteen of the planes are used, and the 20th plane is retained as a spare. The total dimensions of the memory array are 31 by 31 by 10 inches. The X and Y windings are also delay lines, with a characteristic impedance of 150 ohms and a delay of 0.15 μsec. It is interesting to note that the delay time for each



(A)



(B)

Fig. 3(A). Block diagram, 256 by 256 Memory. 3(B). Memory timing chart

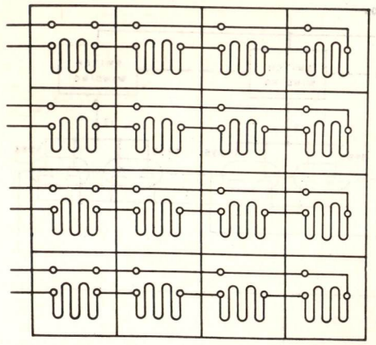


Fig. 4 (left). Digit-plane winding connection schematic, 256 by 256 memory plane

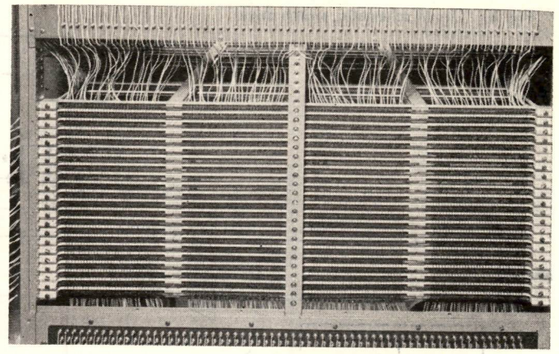


Fig. 6 (right). Memory array

of the various types of winding in the memory is roughly 0.1 μsec per 4,000 cores.

Magnetic-Core Switches

Each magnetic-core switch is made up of 256 tape-wound cores, each core containing 100 wraps of 4-79 Mopermalloy tape 1/4-mil thick and 1/4-inch wide, wound on a bobbin with an inside diameter of 1/4 inch. Four windings are placed on each core: two 12-turn drive windings, a 16-turn output winding, and a 2-turn bias winding. These cores are connected into a square array to form a 2-co-ordinate switch. The operation of the switch is shown in Fig. 7. All the cores in the switch are biased to point A with a d-c bias current. The application of either the u or v current pulses alone does not switch a core. The application of u and v together to a given core causes the core to switch and generate a 410 milliampere read current pulse at the secondary. When the u and v pulses end, the bias current switches the previously selected core back to point A, generating the write pulse. The selected core is allowed to switch completely. The cores in the switch were selected for uniformity of open-circuit output voltage and switching time. The switch was wound as a current step-down device in order to match the characteristics of the driver tubes to that of the 150-ohm X and Y selection lines. All current outputs from the switch are uniform within 5%.

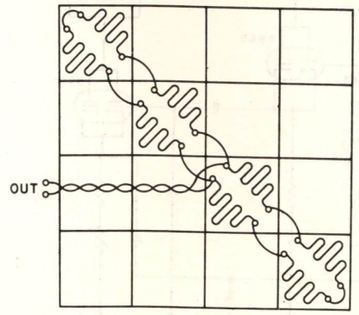


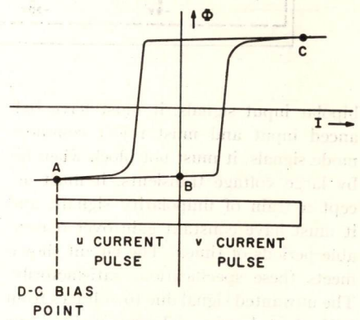
Fig. 5. Sense-winding connection schematic for one sense-winding section, 256 by 256 memory plane

Circuits

The switch driver circuit used to drive one co-ordinate of a switch is shown in Fig. 8. A particular line in the switch is selected by first grounding one of the grid input lines and then pulsing one of the current regulators. For example, to select line O, grid input O is grounded and current regulator input O is pulsed. The current regulators hold the current constant to within 3% over the life of the tubes.

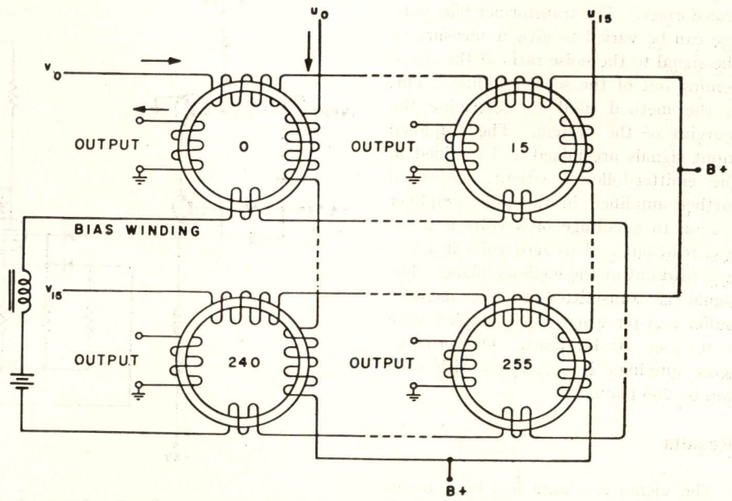
The digit-plane driver circuit is shown in Fig. 9, and it is similar to the current regulator in the switch drive circuit. Four such circuits are associated with each 256 by 256 plane, one for each quarter of the digit winding.

The sense amplifier circuit is shown in Fig. 10. The specifications on the sense amplifier are as follows: it must accept



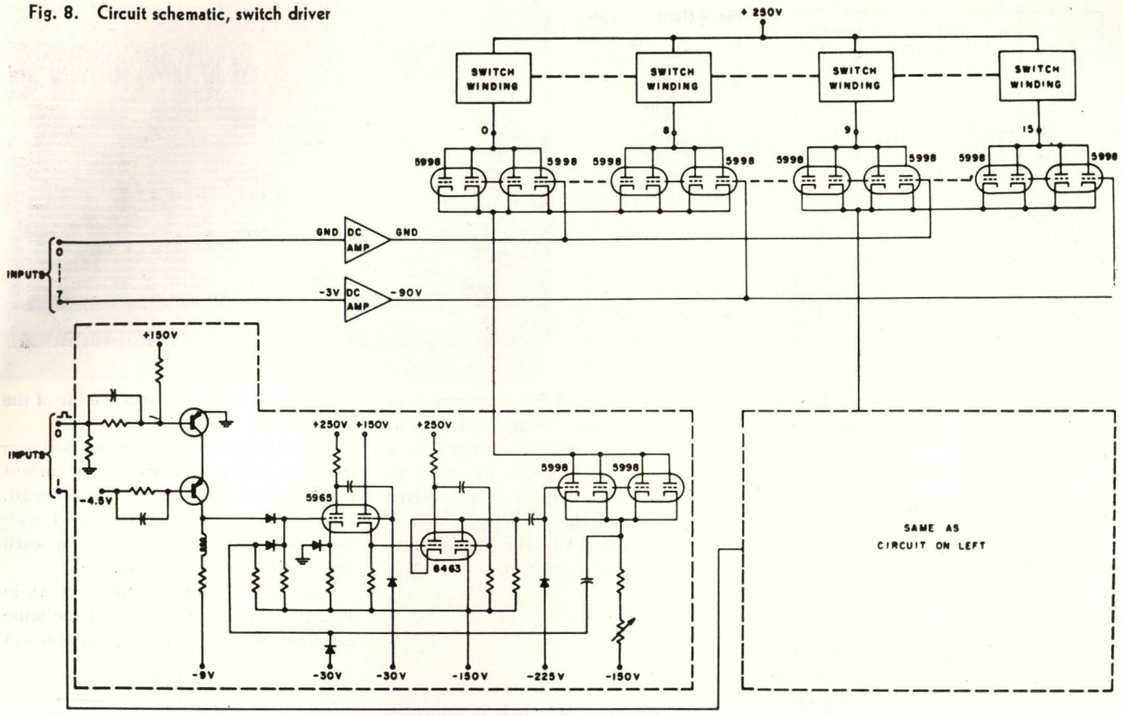
(A)

Fig. 7(A) (right). Operation of switch core. 7(B) (below). Schematic, magnetic-core switch



(B)

Fig. 8. Circuit schematic, switch driver



bipolar input signals, it must have balanced input and must reject common-mode signals, it must not block when hit by large voltage transients, it must accept a train of unipolarity signals, and it must have constant gain over reasonable periods of time. The circuit shown meets these specifications satisfactorily. The unwanted signal due to voltages from half-selected cores and *zeros* is sliced out by applying the proper bias voltage to the center tap of the secondary of the transformer. The transformer bias voltage can be varied to give a measure of the signal to the noise ratio of the signal coming out of the sense winding. This is the method used to determine the margins of the system. The amplified input signals are mixed and rectified in the emitter-follower circuit, and then further amplified in the pulse-amplifier section to a voltage of 3 volts if a *one* was read out and to zero volts if a *zero* was read out of the memory plane. The signal is transmitted to the memory buffer register where it is sampled with a 0.1-μsec strobe pulse. One 4-input sense amplifier is associated with each 256 by 256 plane.

Results

The memory system has been under test in the TX-0 computer for several months with very satisfactory results. A number of the parameters of the system have been plotted versus the sense-amplifier transformer bias voltage. One of the most important plots is shown in Fig. 11. In this test the current in one switch-driver current regulator was varied, and the sense amplifier transformer bias voltage to all 19 sense amplifiers was varied until an incorrect readout occurred. The test program used shifts itself through all memory addresses. It is as "tough" on the memory margins as an average program. When the switch drive current is varied, the amplitude of the read current pulse and the amplitude and shape of the write current pulse are changed; the switch drive current is therefore one of the most

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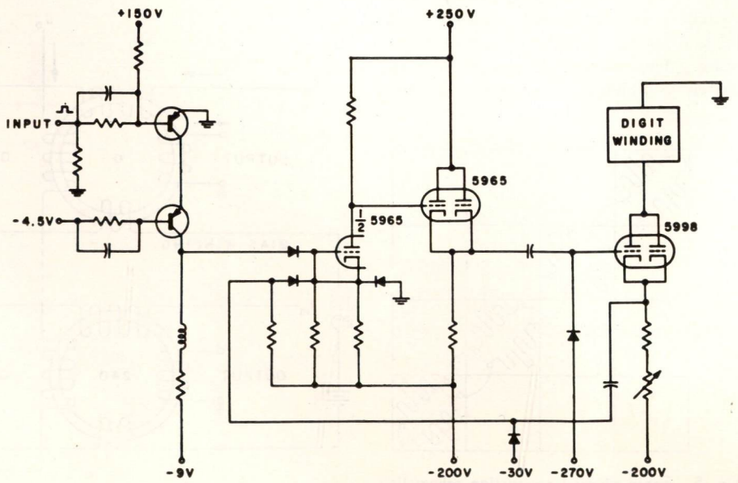
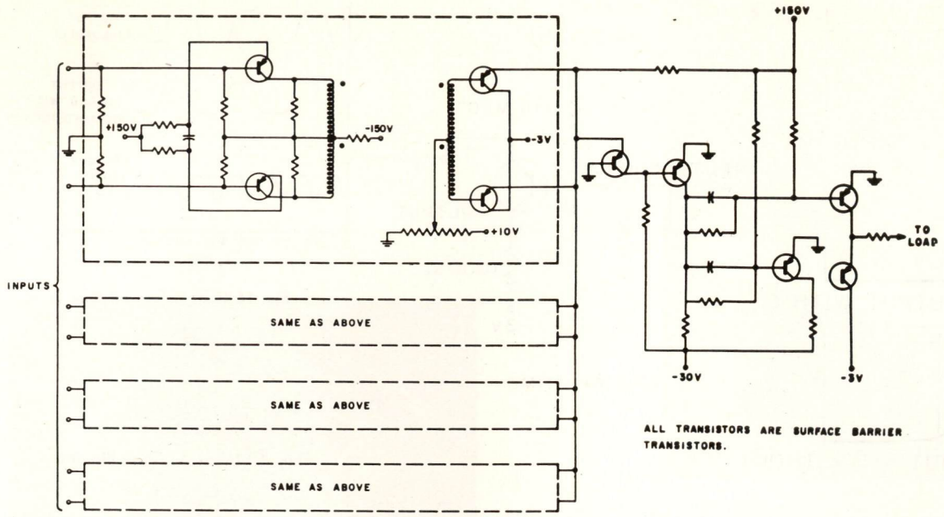


Fig. 9. Circuit schematic, digit plane driver

Fig. 10. Circuit schematic, sense amplifier



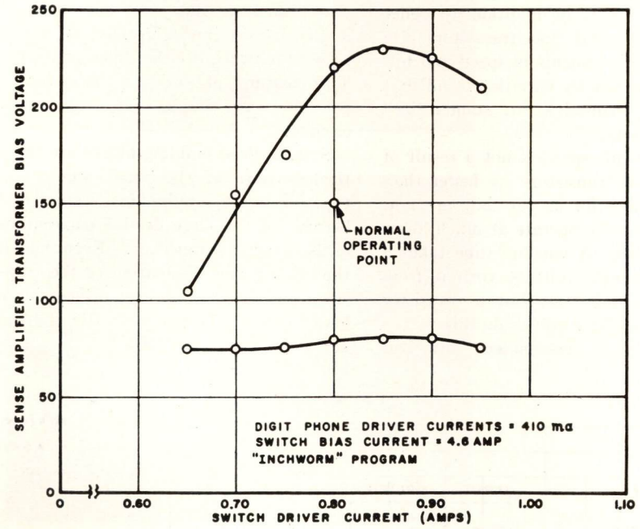


Fig. 11. Switch driver current margins

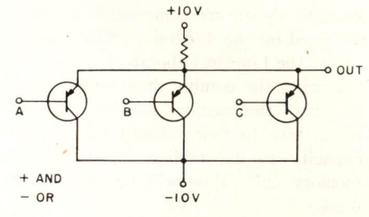


Fig. 13. Parallel emitter followers

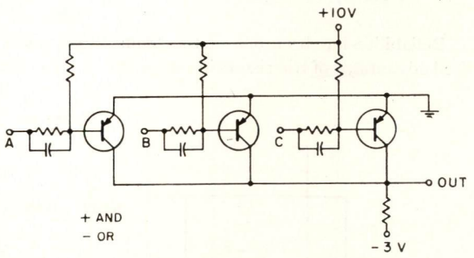


Fig. 14. Parallel inverters

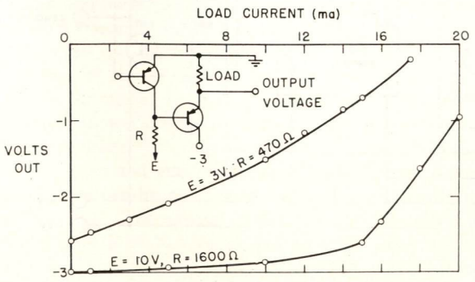


Fig. 12 (left). Saturated emitter follower

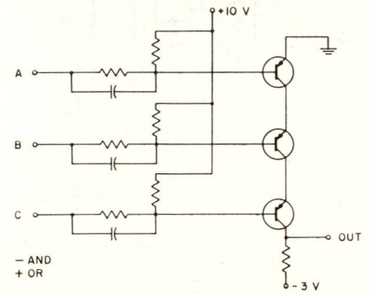


Fig. 15 (right). Series inverters

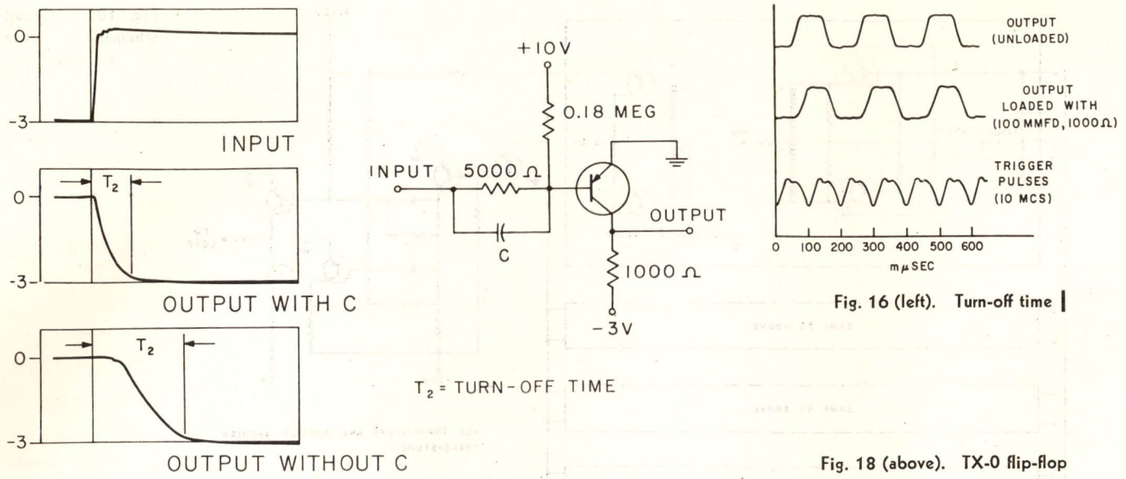


Fig. 18 (above). TX-0 flip-flop

Fig. 16 (left). Turn-off time

critical in the system. The upper curve in Fig. 9 corresponds to failure to read out a *one* and the lower curve represents failure to read out a *zero* correctly. The margins shown are comparable to those obtained on the 4,096-word MTC memory at the Lincoln Laboratory.

During the coming months the word length of the memory will be increased to 37-bits to bring the total storage capacity to 2.5 million bits, and the memory cycle time will be reduced to 6 μsec.

Part II, TX-0 Circuitry

Reliability has been one of the promised advantages of transistors in computer circuits, and indeed it has proved to be so. Reliability has come largely from the gross reduction in the number of parts, and from the expected long life of the transistors. But, in addition to reliability, it is found that transistors also can give improvements in speed and tolerance to parameter variations, and that they lend themselves to standardized building blocks.

Faster circuit speed is not a result of the fact that transistors are faster than vacuum tubes, for as yet they are not, but because they operate at much lower voltage levels. A vacuum tube takes a signal of several volts to turn it from fully ON to fully OFF but a transistor takes less than one volt to do this.

Tolerance to parameter variations is the result of being able to saturate the transistor. Unlike vacuum tubes, which always need an appreciable voltage across them for operation, an ON transistor can have almost no voltage across it. In fact, it can be usually considered as a switch that is either open or closed. This feature of the transistor makes possible very simple and very stable circuits.

Standardized building blocks are practical because of the small number of types of circuits required in a system, and because of the large driving capabilities of the saturated transistor. Even though the rated power dissipation of the transistor may be low, it can drive a large load because there is so little voltage across a saturated transistor.

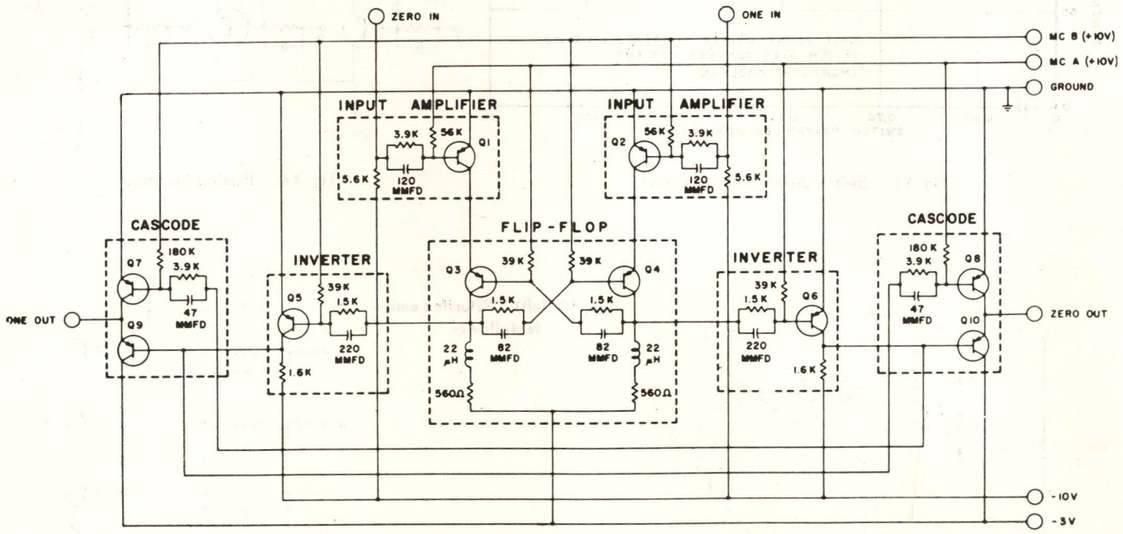


Fig. 17. TX-0 flip-flop

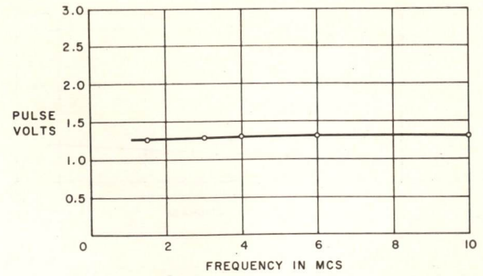


Fig. 19 (left). Trigger sensitivity

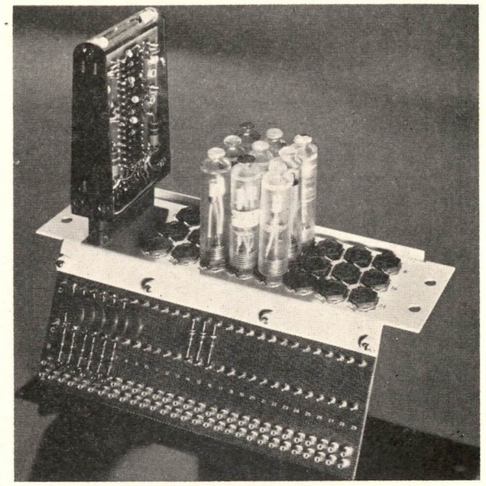


Fig. 22 (right). TX-0 mounting panels

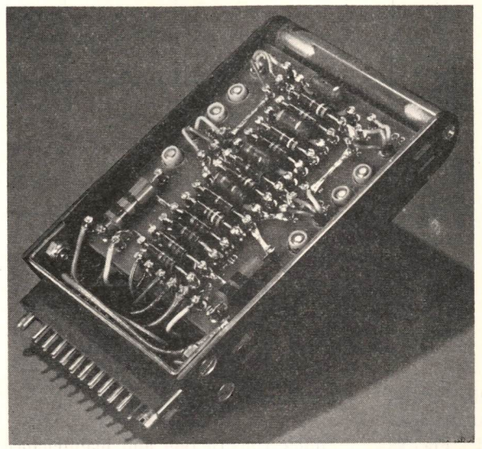


Fig. 20 (left). TX-0 flip-flop

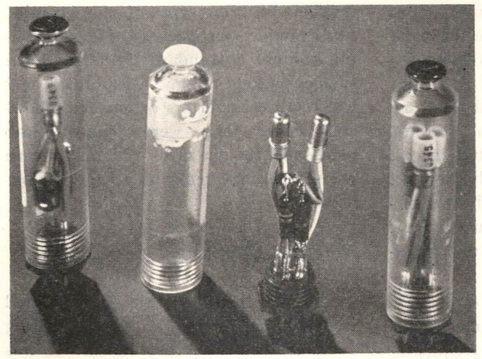


Fig. 21 (right). TX-0 logic units

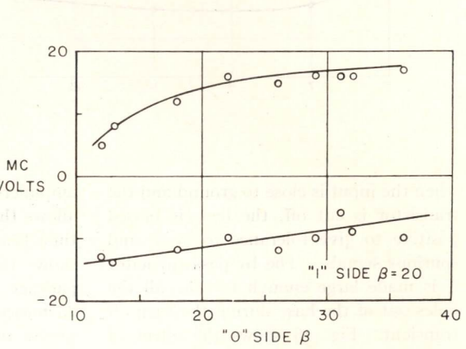


Fig. 23 (right). Beta margins

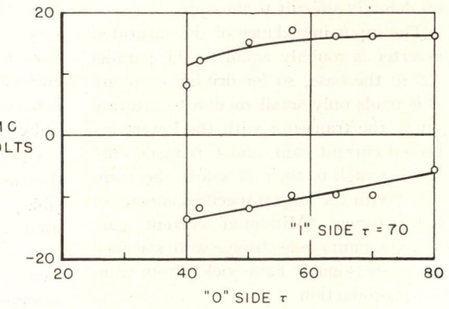


Fig. 24 (right). Tau margins

Circuit Types

There are two general circuit configurations in TX-0: the saturated inverter, and the saturated emitter follower. When a transistor in these circuits is saturated or ON there is only about 0.1 volt across it, so that an ON inverter clamps its output to ground and an ON emitter follower clamps its output to the supply voltage.

The saturated emitter follower is, in general, driven by an inverter as shown in Fig. 12. The output voltage as a function of load current is plotted first with R returned to the −3 supply to show the characteristic of an unsaturated emitter follower, and then with R returned to −10 to show that the output voltage remains almost constant with load variations for a saturated emitter follower. R was changed to keep the inverter current the same in both cases.

Transistor networks are used to perform logical operations. Emitter followers are combined in parallel to form noninverting AND circuits for positive signals and OR circuits for negative signals, as in Fig. 13. Inverters are combined in parallel and in series, as in Figs. 14 and 15, and series-parallel combinations for other operations. The output of a logical network is combined with a sensing pulse to set a flip-flop.

In the schematic of the saturated inverter shown in Fig. 16 the input resistor is selected so that in the ON condition, enough current, plus a safety factor, flows from the base to keep the transistor saturated with less than 100 millivolts, collector to emitter. The resistor to the +10 supply voltage is chosen so that

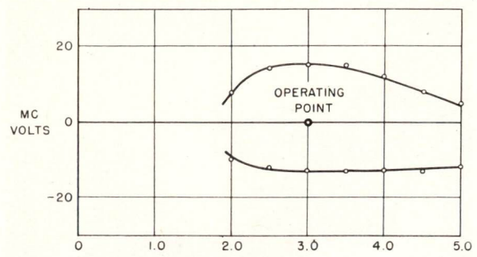


Fig. 25 (left). −3-volt supply margins

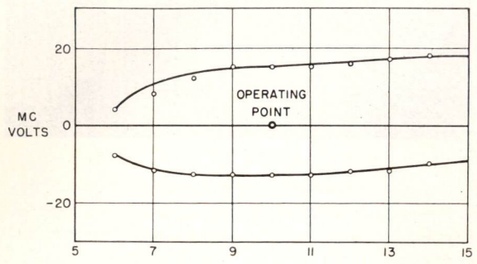


Fig. 26 (left). −10-volt supply margins

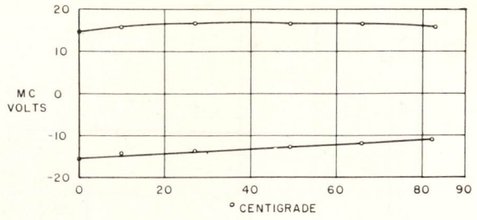


Fig. 27 (right). Temperature margins

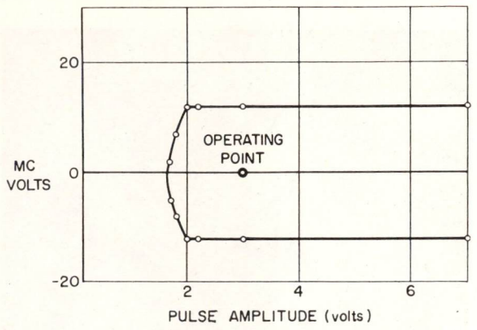


Fig. 28 (right). Pulse margins

when the input is close to ground and the transistor is cut off, the base is biased positive to give tolerance to noise and spurious signals. The by-pass capacitor C is made large enough to take all the holes out of the base during the turn off transient. Fig. 16 shows the effect of this capacitor on the turn-off time. With surface barrier transistors, the holes are removed so fast that the turn-off delay is difficult to measure.

The input impedance of the saturated inverter is roughly equal to the parallel RC in the base, so for driving economy R is made only small enough to saturate safely the transistor with the lowest expected current gain, and C is made only large enough to turn off safely the transistor with the largest specified amount of hole storage. Minimum current gain and maximum hole storage were specified to give reasonably large yields from transistor production.

Flip-Flop

In designing TX-0 it was decided that the advantages of having one standard flip-flop would be worth the cost of some complication in the circuitry. The circuit diagram of the flip-flop package in Fig. 17 shows an Eccles-Jordan flip-flop followed by a 3-transistor amplifier on each side. The output amplifiers give excellent rise time. Input amplifiers isolate the pulse input circuits and raise the input impedance. Also these amplifiers act as a delay line which allows the flip-flop to be set at the same time that it is being sampled. Fig. 18 shows the wave forms of this flip-flop package. The rise and fall times, about 25 mμsec, are faster than one normally sees in an inverter or emitter follower because on each output there is an inverter that pulls to ground and an emitter follower that pulls to −3 volts. Fig. 19 shows the pulse amplitude necessary to complement the flip-flop at various frequencies. Although this circuit will operate at a 10-megapulse rate, it is normally run at a maximum of 5 megapulses per second.

Circuits which are repeated often were designed with as few components as possible. In the case of less frequently used circuits, added components and even redundancy were incorporated when they could simplify the system. For example, the number of flip-flops in a system like TX-0 is quite small compared to the gates which transfer information from one group of flip-flops to another. So the TX-0 transfer gates were made very simple. A transfer gate is in fact only a single inverter; the emitter is connected to the output of the flip-flop being read, and the collector is connected to the input of the flip-flop being set. The output impedance of the flip-flop is so low that when the output is at the ground level, a pulse on the base of the transfer gate sets the other flip-flop.

Packaging

Simple construction and maintenance of TX-0 was accomplished by using large numbers of a few types of plug-in units. For example, one package, Fig. 20, contained only a standard flip-flop. Even smaller packages, Fig. 21, contained only one to three inverters or emitter followers. These then were plugged into panels like the one in Fig. 22, and in turn were interconnected with solderless connectors.

Marginal Checking

Marginal checking was incorporated in these circuits to locate deteriorating components before they failed. It was also useful for locating the design center of the various parameters, and for indicating the tolerance of circuits to these parameters. In addition, marginal checking was used after the TX-0 system was operating to find noise and other system faults which were not serious enough to cause failure, but which would have decreased the reliability.

Operating conditions of the circuits can be indicated by varying the inverter bias. In the flip-flop schematic in Fig. 17, the inverters were divided into two groups for marginal checking, and the two leads labeled MCA and MCB are varied one at a time for most critical checking of the circuit.

Sample plots of margins as a function of various parameters are shown in the figures. Fig. 23 shows the tolerance to the transistor current gain, and how marginal checking will indicate its deterioration.

Fig. 24 shows the tolerance to τ, a measure of hole storage. Margins to supply voltages, temperature, and pulse amplitude are shown in Figs. 25 through 28.

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TX-0, A Transistor Computer with a 256 by 256 Memory

J. L. MITCHELL K. H. OLSEN

Synopsis: TX-0 is a high-speed digital computer which was built at Lincoln Laboratory to demonstrate and operationally test 5-megapulse transistor circuitry and a 65,536-word magnetic-core memory. The word length is 19 bits; 1 bit is a parity check bit for memory, 16 bits are assigned to memory addressing, and the 2 remaining bits are used to select among three memory-reference instructions and one micro-programming instruction. The logic is performed by standardized packages using surface barrier transistors. Fig. 1 shows TX-0 with the arithmetic element just beyond the console and the memory on the far left. Part I of this paper covers the TX-0 memory, and Part II the TX-0 circuitry.

Part I, The TX-0 Memory

THE TX-O MEMORY, Fig. 2, is a high-speed, random-access, coincident-current magnetic-core unit with a storage capacity of 65,536 19-bit words. The bits in the word are read out in parallel, and the cycle time is 7.0 μsec (microseconds). (Cycle time is defined as the time between successive read operations.) Two 256-position magnetic-core switches are used to supply the read and write current pulses to selection lines. The memory system contains 425 dual triodes and 625 transistors. It is interesting to note that the presently available 4,000-register magnetic-core memories use almost as many active elements as are used in this 65,000-register memory. The memory was designed both electrically and mechanically so that the word length can be expanded to 37 bits. Two co-ordinates are used to select a register during the read operation, and three co-ordinates are used for writing. A 2 to 1 current selection ratio is used. A block diagram of the memory system and the timing diagram is shown in Fig. 3. The basic operation of this type of memory system has been adequately described in the literature and will not be repeated here.[1]

Memory Array

The memory array contains $1^1/_4$ million ferrite cores which were manufactured at the Lincoln Laboratory. The outside diameter of the core is 80 mils, the inside diameter 50 mils, and the height 22 mils. When driven with an 820-milliampere current pulse, the cores switch in 1 μsec and give a peak output voltage of 100 millivolts. The cores used in this memory have a somewhat greater signal-to-noise ratio than available commercial cores. The cores are wired into 64 by 64 subassemblies, each subassembly being a complete operating memory plane with its own sense and digit winding. The same winding configurations are used in the 64 by 64 subassemblies as were used in the previous memories built at the Lincoln Laboratory.[2] Sixteen 64 by 64 subassemblies are assembled in a square array and connected together to form each 256 by 256 plane.[3] The choice of a 64 by 64 subassembly size was a compromise between the number of soldered connections in the 256 by 256 plane and the ease of construction and test of the subassemblies.

The digit-plane winding in each 256 by 256 plane is divided into quarters, each quarter being made up of the digit winding of four subassemblies connected in series as shown in Fig. 4. Each quarter looks like a delay line with a characteristic impedance of 150 ohms

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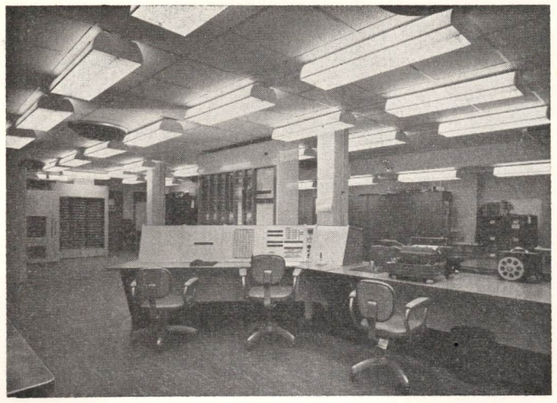


Fig. 1. TX-0 computer

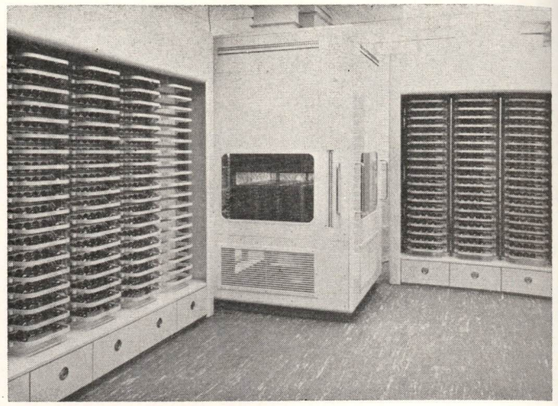


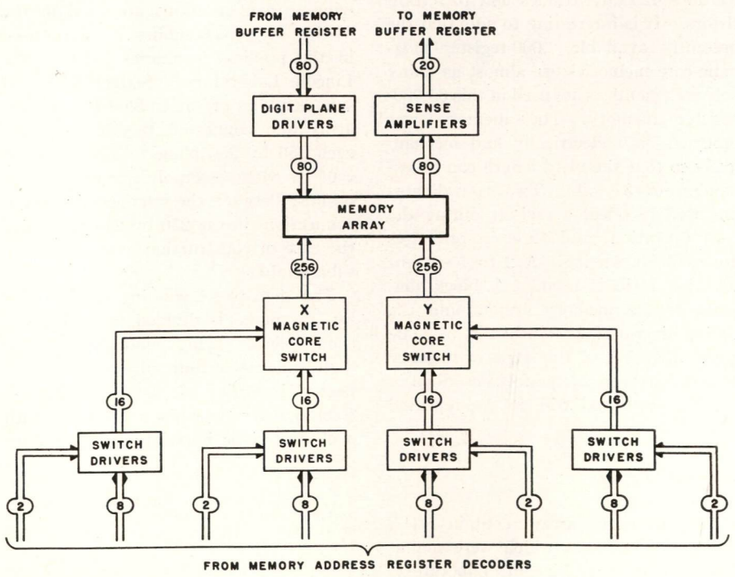
Fig. 2. TX-0 memory

and a delay time of 0.4 μsec. The choice of connecting only four subassemblies in series is a compromise between delay time and equipment. Any increase in digit-plane winding delay would result in an increased memory cycle time; for example, using one digit-plane winding per 256 by 256 plane would add 2 μsec to the cycle time.

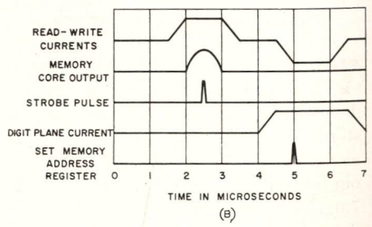
It should be noted that during the operation of the memory, it is practical to drive only one of the digit-plane winding quarters in a given 256 by 256 plane at any one time. When a pulse of current is supplied to the digit-plane winding the resultant voltages cause transient currents to flow through the interwinding capacities from the digit winding to the X, Y, and sense windings. If the quarters of all the planes are driven at once, the currents flowing through the interwinding capacities are of sufficient magnitude to cause distortion of the digit-plane current pulse, and to create undesirable transients on the sense winding. When only one of the digit-plane winding quarters is pulsed at a given time, these effects are not harmful.

The sense winding in a 256 by 256 plane is also broken up into four sections, each section consisting of the sense windings from four 64 by 64 subassemblies. The subassemblies on a given sense winding are connected in such a manner that no two subassemblies on the same sense winding section are common to the same X or Y drive line; see Fig. 5. It should be noted that with this method of connection the voltage induced in the sense winding by the half-selected cores is equal to that induced in a 64 by 64 memory.[4] Each sense winding is also a delay line. To reduce the delay and resultant signal distortion, the four subassemblies on a given sense winding section are connected in series parallel as shown in Fig. 3 rather than in series. Of course, this type of connection halves the signal amplitude seen at the output terminals of the sense winding section.

Twenty 256 by 256 planes are stacked on 1/2-inch centers and the X and Y wires are connected in series to form the complete memory array; see Fig. 6. Nineteen of the planes are used, and the 20th plane is retained as a spare. The total dimensions of the memory array are 31 by 31 by 10 inches. The X and Y windings are also delay lines, with a characteristic impedance of 150 ohms and a delay of 0.15 μsec. It is interesting to note that the delay time for each



(A)



(B)

Fig. 3(A). Block diagram, 256 by 256 Memory. 3(B). Memory timing chart

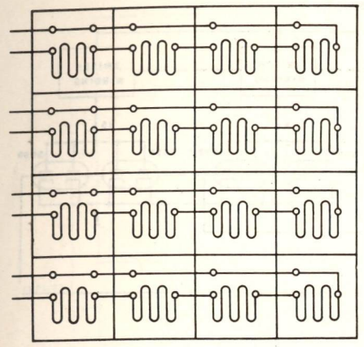


Fig. 4 (left). Digit-plane winding connection schematic, 256 by 256 memory plane

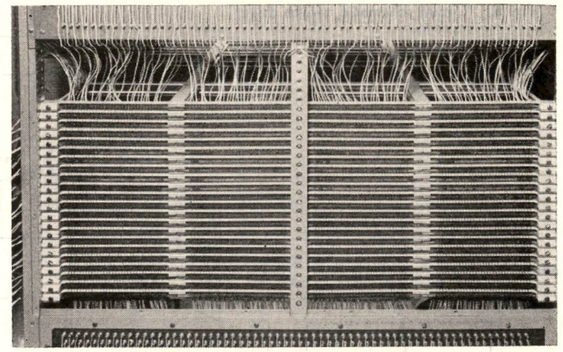


Fig. 6 (right). Memory array

of the various types of winding in the memory is roughly 0.1 μsec per 4,000 cores.

Magnetic-Core Switches

Each magnetic-core switch is made up of 256 tape-wound cores, each core containing 100 wraps of 4-79 Mopermalloy tape 1/4-mil thick and 1/4-inch wide, wound on a bobbin with an inside diameter of 1/4 inch. Four windings are placed on each core: two 12-turn drive windings, a 16-turn output winding, and a 2-turn bias winding. These cores are connected into a square array to form a 2-co-ordinate switch. The operation of the switch is shown in Fig. 7. All the cores in the switch are biased to point A with a d-c bias current. The application of either the u or v current pulses alone does not switch a core. The application of u and v together to a given core causes the core to switch and generate a 410 milliampere read current pulse at the secondary. When the u and v pulses end, the bias current switches the previously selected core back to point A, generating the write pulse. The selected core is allowed to switch completely. The cores in the switch were selected for uniformity of open-circuit output voltage and switching time. The switch was wound as a current step-down device in order to match the characteristics of the driver tubes to that of the 150-ohm X and Y selection lines. All current outputs from the switch are uniform within 5%.

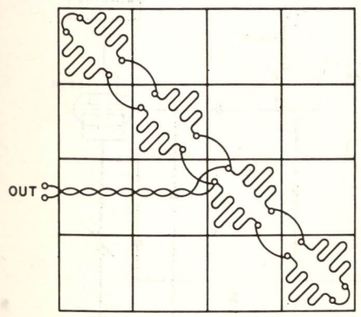


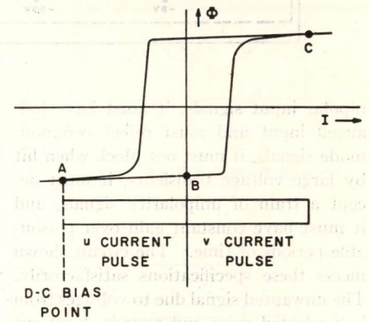
Fig. 5. Sense-winding connection schematic for one sense-winding section, 256 by 256 memory plane

Circuits

The switch driver circuit used to drive one co-ordinate of a switch is shown in Fig. 8. A particular line in the switch is selected by first grounding one of the grid input lines and then pulsing one of the current regulators. For example, to select line O, grid input O is grounded and current regulator input O is pulsed. The current regulators hold the current constant to within 3% over the life of the tubes.

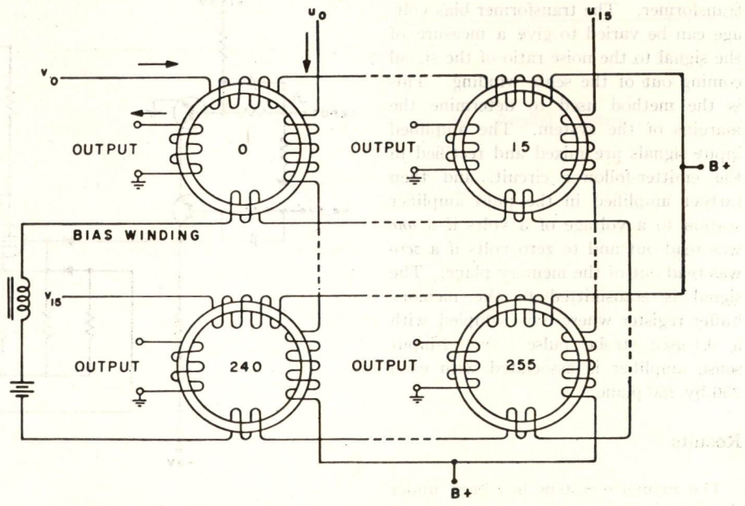
The digit-plane driver circuit is shown in Fig. 9, and it is similar to the current regulator in the switch drive circuit. Four such circuits are associated with each 256 by 256 plane, one for each quarter of the digit winding.

The sense amplifier circuit is shown in Fig. 10. The specifications on the sense amplifier are as follows: it must accept



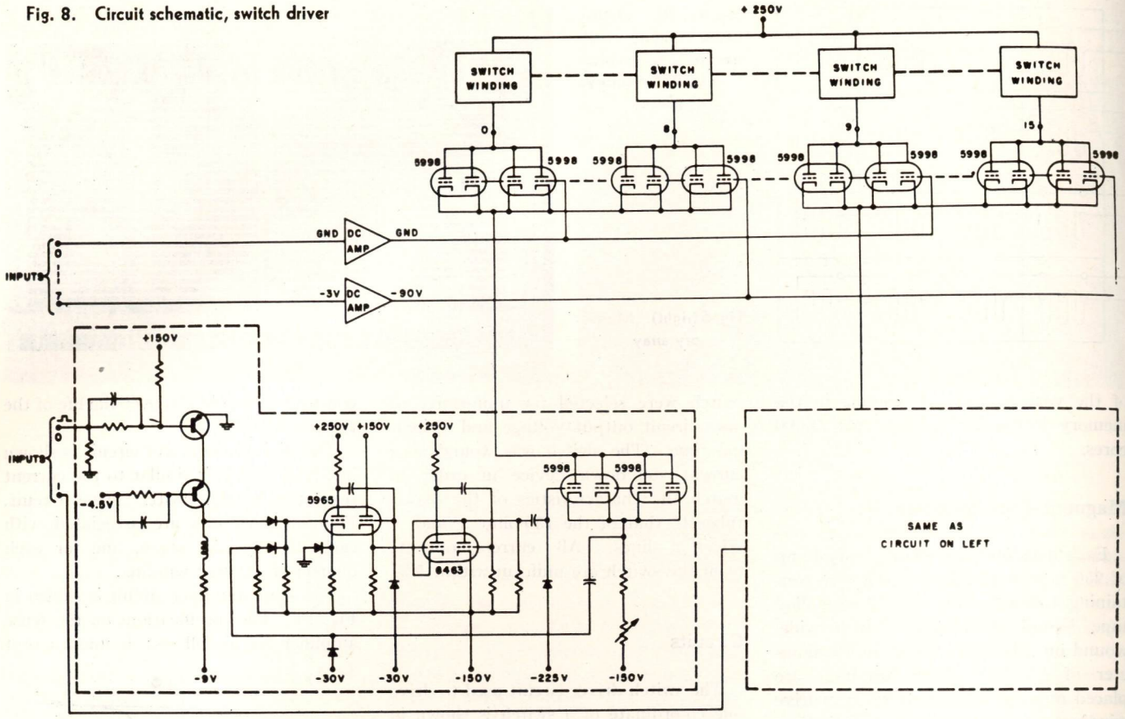
(A)

Fig. 7(A) (right). Operation of switch core. 7(B) (below). Schematic, magnetic-core switch



(B)

Fig. 8. Circuit schematic, switch driver



bipolar input signals, it must have balanced input and must reject common-mode signals, it must not block when hit by large voltage transients, it must accept a train of unipolarity signals, and it must have constant gain over reasonable periods of time. The circuit shown meets these specifications satisfactorily. The unwanted signal due to voltages from half-selected cores and *zeros* is sliced out by applying the proper bias voltage to the center tap of the secondary of the transformer. The transformer bias voltage can be varied to give a measure of the signal to the noise ratio of the signal coming out of the sense winding. This is the method used to determine the margins of the system. The amplified input signals are mixed and rectified in the emitter-follower circuit, and then further amplified in the pulse-amplifier section to a voltage of 3 volts if a *one* was read out and to zero volts if a *zero* was read out of the memory plane. The signal is transmitted to the memory buffer register where it is sampled with a 0.1-μsec strobe pulse. One 4-input sense amplifier is associated with each 256 by 256 plane.

Results

The memory system has been under test in the TX-0 computer for several months with very satisfactory results. A number of the parameters of the system have been plotted versus the sense-amplifier transformer bias voltage. One of the most important plots is shown in Fig. 11. In this test the current in one switch-driver current regulator was varied, and the sense amplifier transformer bias voltage to all 19 sense amplifiers was varied until an incorrect readout occurred. The test program used shifts itself through all memory addresses. It is as "tough" on the memory margins as an average program. When the switch drive current is varied, the amplitude of the read current pulse and the amplitude and shape of the write current pulse are changed; the switch drive current is therefore one of the most

(*Continued on p. 98*)

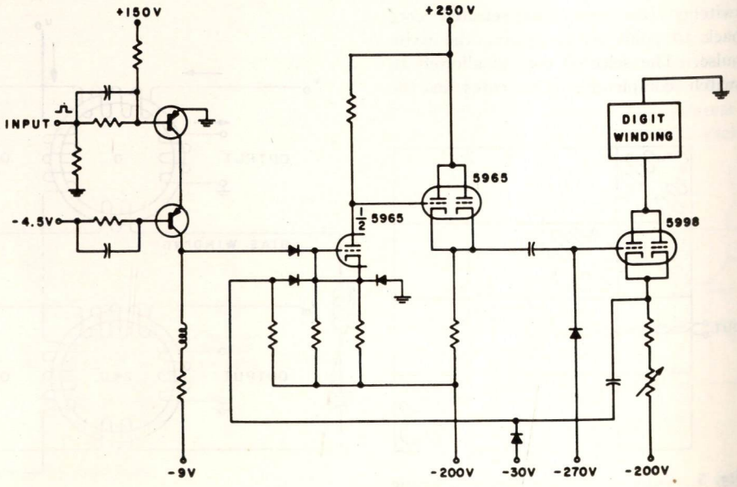


Fig. 9. Circuit schematic, digit plane driver

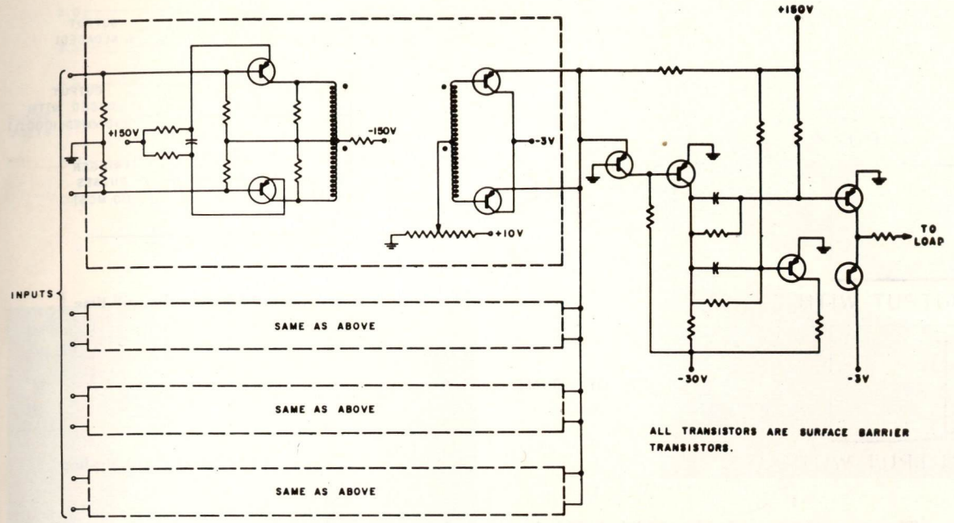


Fig. 10. Circuit schematic, sense amplifier

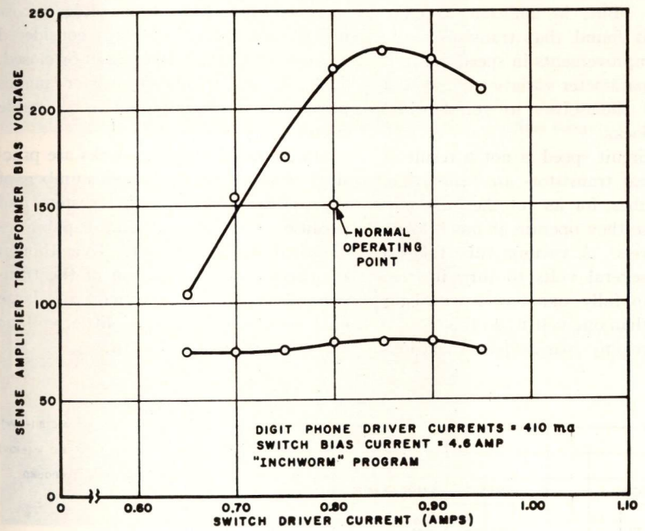


Fig. 11. Switch driver current margins

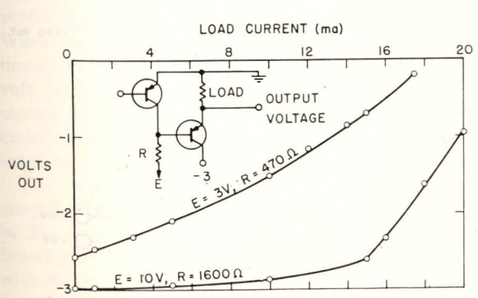


Fig. 12 (left). Saturated emitter follower

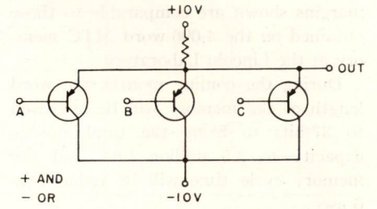


Fig. 13. Parallel emitter followers

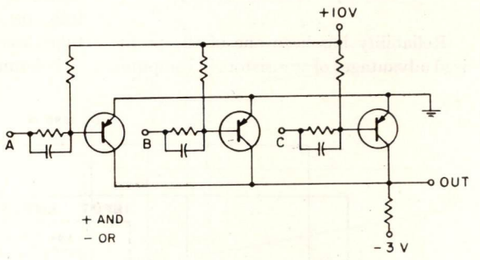


Fig. 14. Parallel inverters

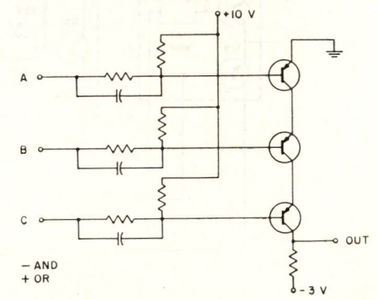


Fig. 15 (right). Series inverters

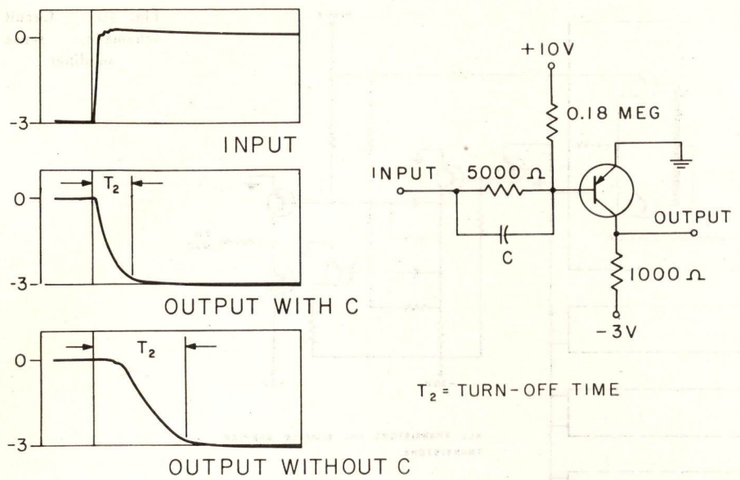


Fig. 18 (above). TX-0 flip-flop

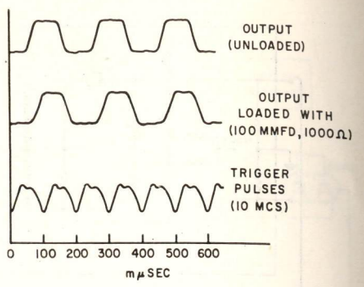


Fig. 16 (left). Turn-off time

critical in the system. The upper curve in Fig. 9 corresponds to failure to read out a *one* and the lower curve represents failure to read out a *zero* correctly. The margins shown are comparable to those obtained on the 4,096-word MTC memory at the Lincoln Laboratory.

During the coming months the word length of the memory will be increased to 37-bits to bring the total storage capacity to 2.5 million bits, and the memory cycle time will be reduced to 6 μsec.

Part II, TX-0 Circuitry

Reliability has been one of the promised advantages of transistors in computer circuits, and indeed it has proved to be so. Reliability has come largely from the gross reduction in the number of parts, and from the expected long life of the transistors. But, in addition to reliability, it is found that transistors also can give improvements in speed and tolerance to parameter variations, and that they lend themselves to standardized building blocks.

Faster circuit speed is not a result of the fact that transistors are faster than vacuum tubes, for as yet they are not, but because they operate at much lower voltage levels. A vacuum tube takes a signal of several volts to turn it from fully ON to fully OFF but a transistor takes less than one volt to do this.

Tolerance to parameter variations is the result of being able to saturate the transistor. Unlike vacuum tubes, which always need an appreciable voltage across them for operation, an ON transistor can have almost no voltage across it. In fact, it can be usually considered as a switch that is either open or closed. This feature of the transistor makes possible very simple and very stable circuits.

Standardized building blocks are practical because of the small number of types of circuits required in a system, and because of the large driving capabilities of the saturated transistor. Even though the rated power dissipation of the transistor may be low, it can drive a large load because there is so little voltage across a saturated transistor.

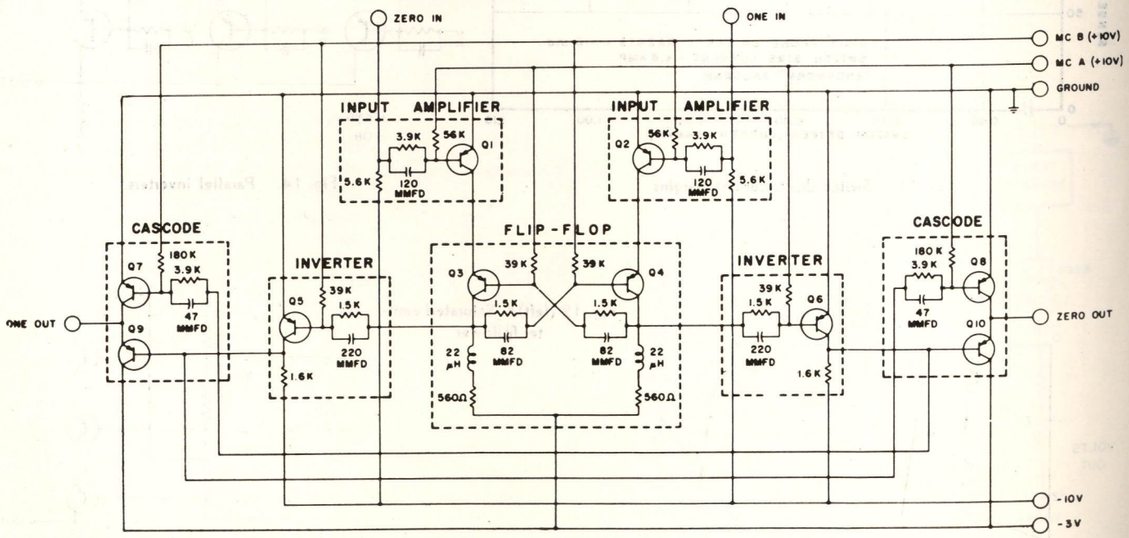


Fig. 17. TX-0 flip-flop

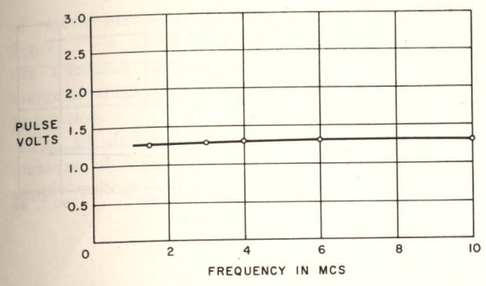


Fig. 19 (left). Trigger sensitivity

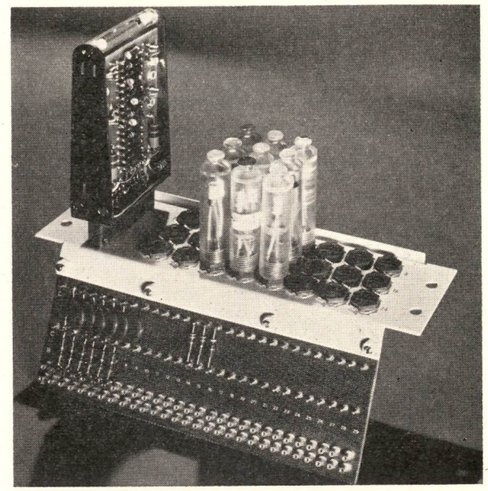


Fig. 22 (right). TX-0 mounting panels

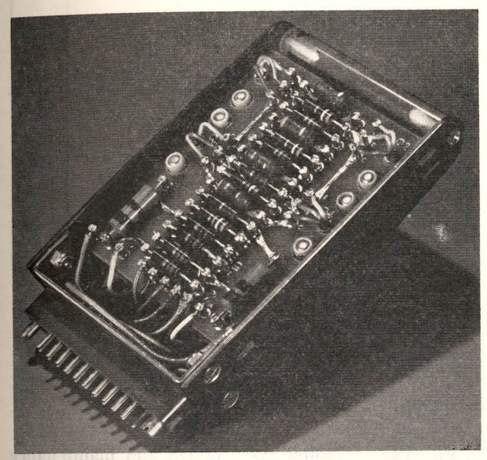


Fig. 20 (left). TX-0 flip-flop

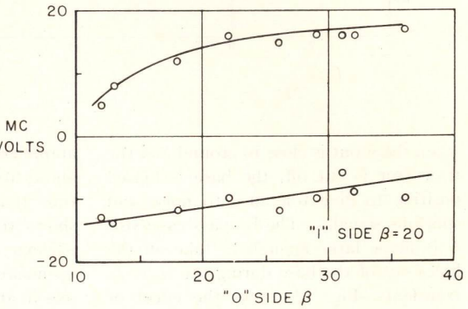


Fig. 23 (right). Beta margins

Fig. 21 (right). TX-0 logic units

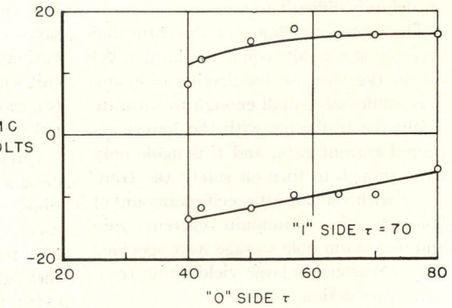


Fig. 24 (right). Tau margins

Circuit Types

There are two general circuit configurations in TX-0: the saturated inverter, and the saturated emitter follower. When a transistor in these circuits is saturated or ON there is only about 0.1 volt across it, so that an ON inverter clamps its output to ground and an ON emitter follower clamps its output to the supply voltage.

The saturated emitter follower is, in general, driven by an inverter as shown in Fig. 12. The output voltage as a function of load current is plotted first with R returned to the −3 supply to show the characteristic of an unsaturated emitter follower, and then with R returned to −10 to show that the output voltage remains almost constant with load variations for a saturated emitter follower. R was changed to keep the inverter current the same in both cases.

Transistor networks are used to perform logical operations. Emitter followers are combined in parallel to form non-inverting AND circuits for positive signals and OR circuits for negative signals, as in Fig. 13. Inverters are combined in parallel and in series, as in Figs. 14 and 15, and series-parallel combinations for other operations. The output of a logical network is combined with a sensing pulse to set a flip-flop.

In the schematic of the saturated inverter shown in Fig. 16 the input resistor is selected so that in the ON condition, enough current, plus a safety factor, flows from the base to keep the transistor saturated with less than 100 millivolts, collector to emitter. The resistor to the +10 supply voltage is chosen so that

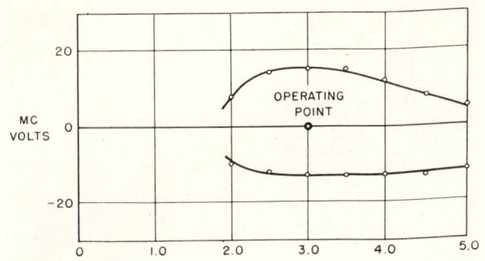


Fig. 25 (left). −3-volt supply margins

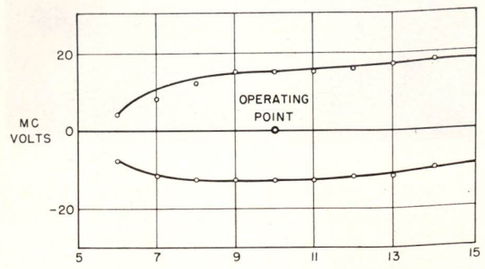


Fig. 26 (left). −10-volt supply margins

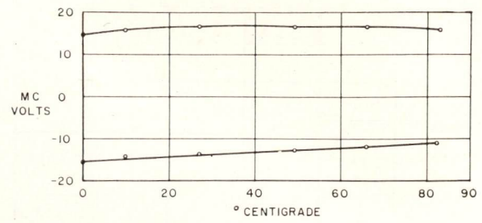


Fig. 27 (right). Temperature margins

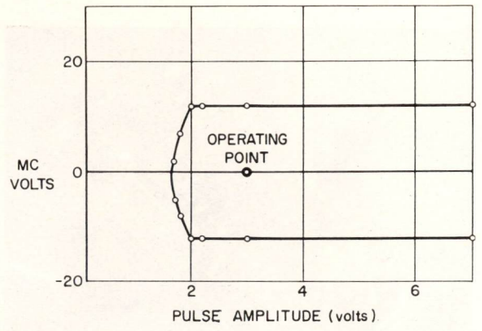


Fig. 28 (right). Pulse margins

when the input is close to ground and the transistor is cut off, the base is biased positive to give tolerance to noise and spurious signals. The by-pass capacitor C is made large enough to take all the holes out of the base during the turn off transient. Fig. 16 shows the effect of this capacitor on the turn-off time. With surface barrier transistors, the holes are removed so fast that the turn-off delay is difficult to measure.

The input impedance of the saturated inverter is roughly equal to the parallel RC in the base, so for driving economy R is made only small enough to saturate safely the transistor with the lowest expected current gain, and C is made only large enough to turn off safely the transistor with the largest specified amount of hole storage. Minimum current gain and maximum hole storage were specified to give reasonably large yields from transistor production.

Flip-Flop

In designing TX-0 it was decided that the advantages of having one standard flip-flop would be worth the cost of some complication in the circuitry. The circuit diagram of the flip-flop package in Fig. 17 shows an Eccles-Jordan flip-flop followed by a 3-transistor amplifier on each side. The output amplifiers give excellent rise time. Input amplifiers isolate the pulse input circuits and raise the input impedance. Also these amplifiers act as a delay line which allows the flip-flop to be set at the same time that it is being sampled. Fig. 18 shows the wave forms of this flip-flop package. The rise and fall times, about 25 mμsec, are faster than one normally sees in an inverter or emitter follower because on each output there is an inverter that pulls to ground and an emitter follower that pulls to −3 volts. Fig. 19 shows the pulse amplitude necessary to complement the flip-flop at various frequencies. Although this circuit will operate at a 10-megapulse rate, it is normally run at a maximum of 5 megapulses per second.

Circuits which are repeated often were designed with as few components as possible. In the case of less frequently used circuits, added components and even redundancy were incorporated when they could simplify the system. For example, the number of flip-flops in a system like TX-0 is quite small compared to the gates which transfer information from one group of flip-flops to another. So the TX-0 transfer gates were made very simple. A transfer gate is in fact only a single inverter; the emitter is connected to the output of the flip-flop being read, and the collector is connected to the input of the flip-flop being set. The output impedance of the flip-flop is so low that when the output is at the ground level, a pulse on the base of the transfer gate sets the other flip-flop.

Packaging

Simple construction and maintenance of TX-0 was accomplished by using large numbers of a few types of plug-in units. For example, one package, Fig. 20, contained only a standard flip-flop. Even smaller packages, Fig. 21, contained only one to three inverters or emitter followers. These then were plugged into panels like the one in Fig. 22, and in turn were interconnected with solderless connectors.

Marginal Checking

Marginal checking was incorporated in these circuits to locate deteriorating components before they failed. It was also useful for locating the design center of the various parameters, and for indicating the tolerance of circuits to these parameters. In addition, marginal checking was used after the TX-0 system was operating to find noise and other system faults which were not serious enough to cause failure, but which would have decreased the reliability.

Operating conditions of the circuits can be indicated by varying the inverter bias. In the flip-flop schematic in Fig. 17, the inverters were divided into two groups for marginal checking, and the two leads labeled *MCA* and *MCB* are varied one at a time for most critical checking of the circuit.

Sample plots of margins as a function of various parameters are shown in the figures. Fig. 23 shows the tolerance to the transistor current gain, and how marginal checking will indicate its deterioration.

Fig. 24 shows the tolerance to τ, a measure of hole storage. Margins to supply voltages, temperature, and pulse amplitude are shown in Figs. 25 through 28.

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Transistor Circuitry in the Lincoln TX-2*

KENNETH H. OLSEN†

CIRCUIT CONFIGURATIONS

ONLY TWO BASIC circuits are needed to perform most of the logical operations in the TX-2 computer; a saturated transistor inverter and a saturated emitter follower. To the logical designer who works with them, these circuits can be considered as simple switches which are either open or closed.

The schematic diagram of an emitter follower and the symbol used by the logical designers is shown in Fig. 1.

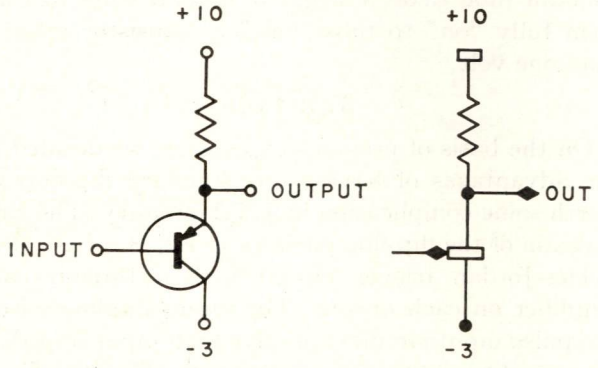

Fig. 1—Emitter follower.

* This work was supported jointly by the U. S. Army, Navy, and Air Force under contract with Mass. Inst. Tech.

† Lincoln Lab., M.I.T., Lexington, Mass.

With a negative input, the output is "shorted" to the −3-volt supply as through a switch. When several of these emitter followers are combined in parallel, as in Fig. 2, any one of them will clamp the output to −3 v.

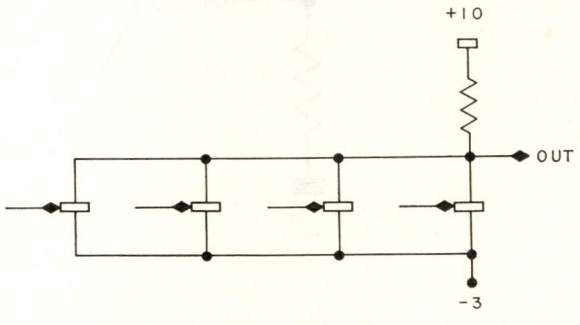

Fig. 2—Parallel emitter follower.

We have then an OR circuit for negative signals and an AND circuit for positive signals. The transistor inverter is shown in Fig. 3 (next page) with its logic symbol. Basic AND, OR circuits result from the connection of these simple switches in series or parallel (Figs. 4 and 5). More complex networks like the TX-2 carry circuit use these elements arranged in series-parallel (Fig. 6).

In Fig. 3 the resistor R_1 is chosen so that under the worst combinations of stated component and power

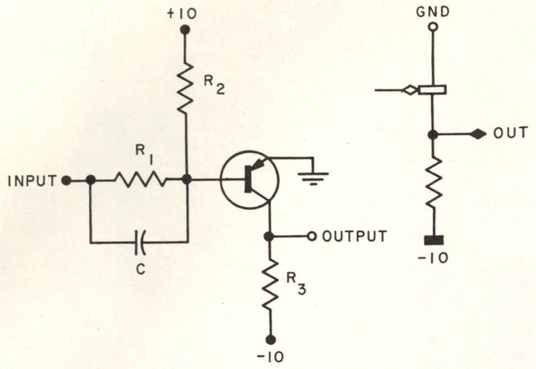

Fig. 3—Inverter.

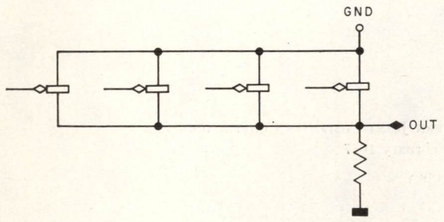

Fig. 4—Parallel inverters.

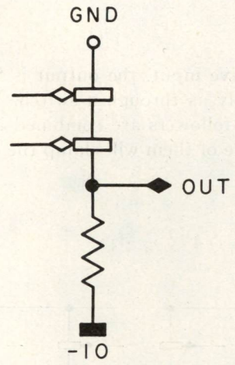

Fig. 5—Series inverters.

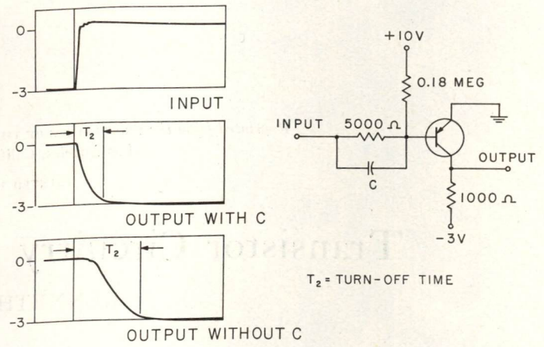

Fig. 7—Turn-off time.

supply variations, the drop across the transistor will be less than 200 millivolts during the "on-condition." R_2 biases the transistor base positive during the off condition to provide greater tolerance to noise, I_{co}, and signal variations. Capacitance C was selected to remove all of the minority carriers from the base when the transistor is being turned off. The effect of C on a test circuit driven by a fast step is shown in Fig. 7. Note that the delay due to hole storage is only a few millimicroseconds.

We run the circuits under saturated conditions to achieve stability and a wide tolerance to parameters without the need for clamp diodes. Unlike vacuum tubes which always need an appreciable voltage across them for operation, a transistor requires practically no voltage across it. In spite of the delay in turning off saturated transistors, these circuits are faster than most vacuum tube circuits. Faster circuit speed is not due to the fact that the transistors are faster than vacuum tubes, but because they operate at much lower voltage levels. A vacuum tube takes a signal of several volts to turn it from fully "on" to fully "off;" a transistor takes less than one volt.

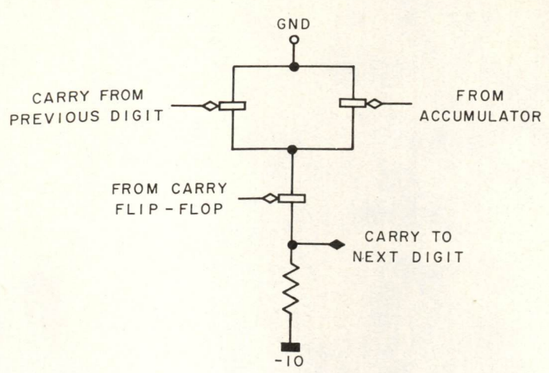

Fig. 6—TX-2 carry circuits.

Flip-Flop

On the basis of previous experience, we decided that the advantages of having one standard flip-flop were worth some complication in TX-2 circuitry. The circuit diagram of the flip-flop package in Fig. 8 is basically an Eccles-Jordan trigger circuit with a three-transistor amplifier on each output. The input amplifiers isolate the pulse input circuits and give high input impedance. The amplifiers give enough delay to allow the flip-flop to be set at the same time that it is being sensed. Fig. 9 shows the waveforms of this flip-flop package when complemented at a 10-megapulse rate. The rise and fall

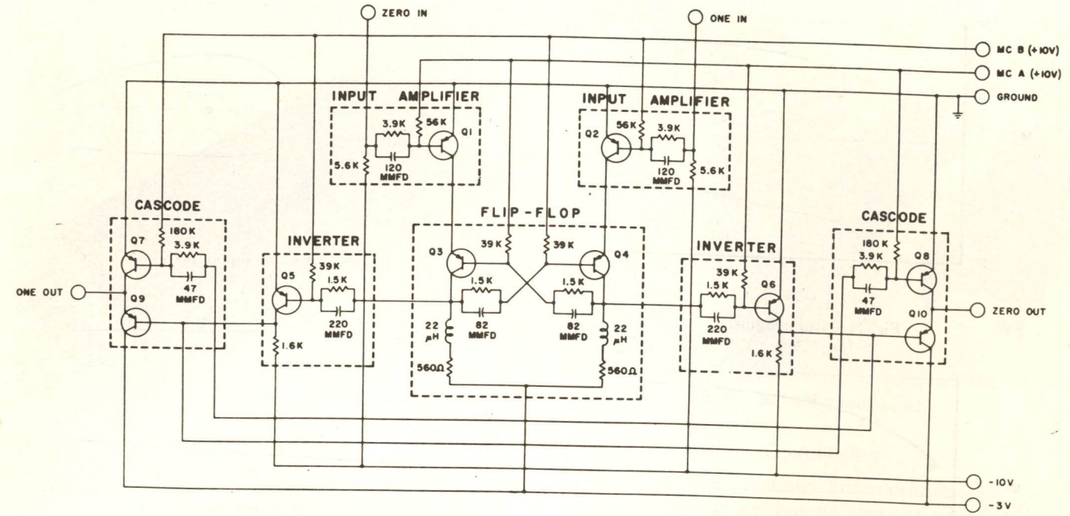

Fig. 8—TX-2 flip-flop.

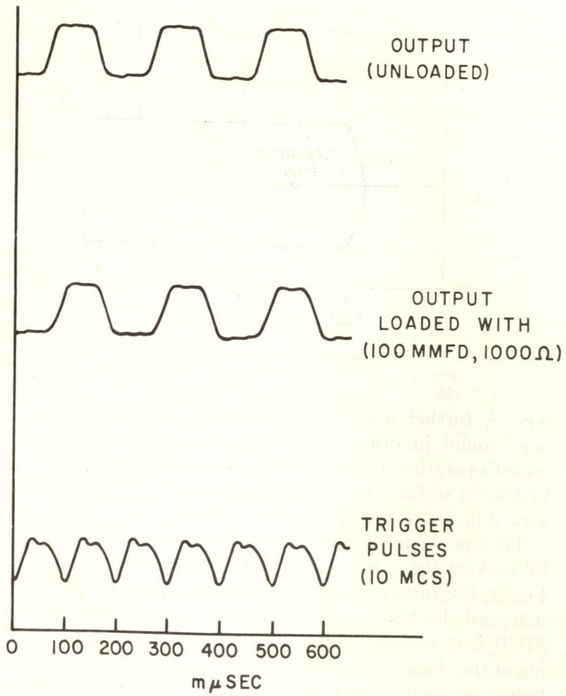

Fig. 9—Flip-flop waveforms.

times, about 25 millimicroseconds, are faster than one normally sees in a single inverter, or an emitter follower because on each output there is an inverter that pulls to ground and an emitter follower that pulls to −3 v.

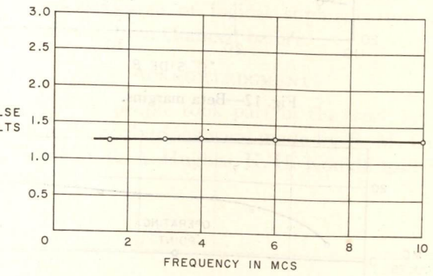

Fig. 10—Trigger sensitivity.

Fig. 10 is a plot of the pulse amplitude necessary to complement the flip-flop at various frequencies. Note the independence of trigger sensitivity to pulse repetition rate. This circuit will operate at a 10-megapulse rate, twice the maximum rate at which it will be used in TX-2.

The TX-2 circuits reproduced most often were designed with a minimum number of components to achieve economies in manufacture and maintenance. The design of less frequently reproduced circuits made liberal use of components—even redundancy to achieve long life and broad tolerance to component variations. The goal was system simplicity and high performance with a lower total number of components than might otherwise be possible. For example, the number of flip-flops in the TX-2 is small compared to the gates which transfer information from one group of flip-flops to another; so the flip-flops were allowed to be relatively complicated but the TX-2 transfer gates were made very simple. A transfer gate is only a single inverter. The emitter is connected to the output of the flip-flop be-

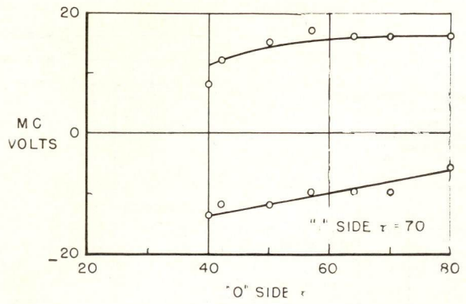

Fig. 11—Tau margins.

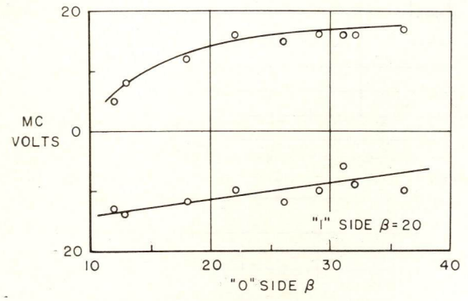

Fig. 12—Beta margins.

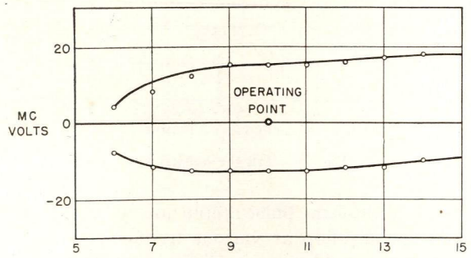

Fig. 13——10-volt supply margins.

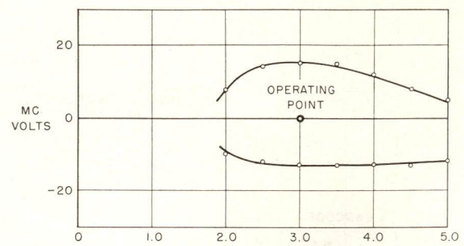

Fig. 14——3-volt supply margins.

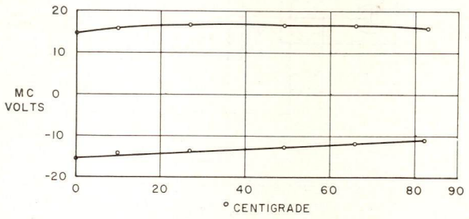

Fig. 15—Temperature margins.

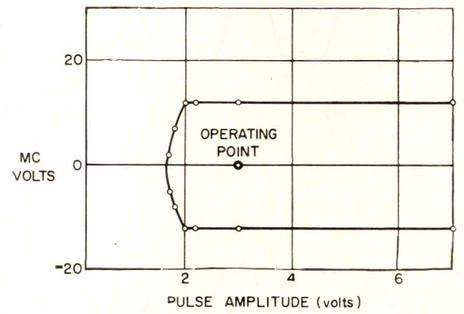

Fig. 16—Pulse margins.

ing read and the collector is connected to the input of the flip-flop being set. The output impedance of the flip-flop is so low that, when the output is at the ground level, a pulse on the base of the transfer gate shorts the input of the other flip-flop to ground and sets its condition.

Marginal Checking

We planned, of course, to incorporate marginal checking in the design of these circuits so that, under a program of regularly scheduled maintenance, deteriorating components could be located before they caused failure in the system. We also found it practical to use the technique during the design of the circuits to locate the design center of the various parameters and to indicate the tolerance of circuit performance to these parameters. A further application of marginal checking has been found in other systems during shakedown and initial operation to pin point noise and other system faults not serious enough to cause failure and therefore very difficult to isolate by other means.

The operating condition of the inverters is indicated by varying the +10-v bias. In the flip-flop schematic in Fig. 8, the inverters were divided into two groups for marginal checking, and the two leads labeled MCA and MCB were varied one at a time for most critical checking of the circuit. The following curves show the locus of failure points for various parameters as a function of the marginal checking voltage. Fig. 11 shows the tolerance to tau, a measure of hole storage and Fig. 12 shows the tolerance to beta, the current gain. Operating margins for supply voltages, temperature, and pulse amplitude are shown in Figs. 13 through 16.

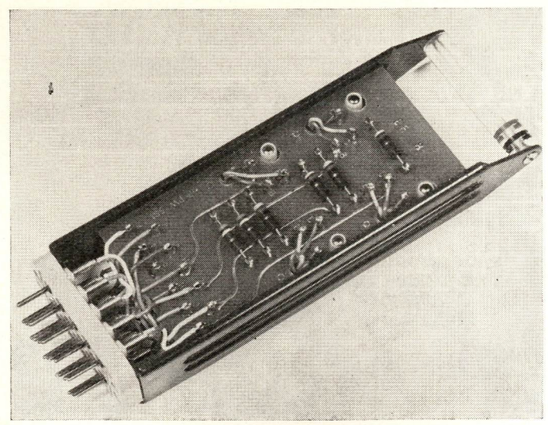

Fig. 17—TX-2 plug-in unit.

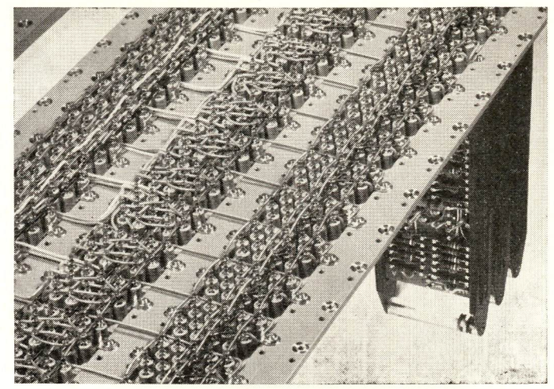

Fig. 18—TX-2 back panel.

Packaging

The number of types of plug-in units was kept small for ease of production and to keep the number of spares to a minimum. The circuits are built on dip soldered etched boards and the components are hand soldered to solid turret lugs. The boards are mounted in steel shells shown in Fig. 17 to keep the boards from flexing. The male and female contacts are machined and gold plated. The sockets are hand wired and soldered in panels as in Fig. 18.

Conclusion

The result of these design considerations is a 5-megapulse control and arithmetic element which will take less than 40 square feet of space and dissipate less than 800 watts of power. The simplicity of the circuits has encouraged a degree of logical sophistication which would not have been chanced before.

Acknowledgment

A number of people took part in the work reported here. Major contributions were made by B. M. Gurley, J. R. Fadiman, R. A. Hughes, K. H. Konkle, and M. E. Petersen.

Discussion

R. D. Gloor (Ramo-Wooldridge Corp.): What is the estimate of the expected mean-free-time between component failures for TX-2?

Mr. Olsen: The TX-0 Computer, which has been running eight hours a day since last April, has lost no transistors. So our experience with the TX-0 is that we expect the transistor portion of the machine to go for weeks without an error.

John Hayes (U.S.N.E.L.): What type of transistors are used in the flip-flops?

Mr. Olsen: The Philco Service Barrier Transistor was a key part of this development. It is tested to computer specifications.

We also use two or three thousand Micro-alloy transistors. We would like to use 100 per cent Micro-alloy transistors, but there were only two or three thousand available at the time we needed them. They have higher gains, particularly higher current, and appear to be much better transistors.

L. P. Retzinger (Litton): What is the propagation time per carry digit?

Mr. Olsen: About 40 millmicroseconds per digit. We made no effort to speed this up. This is a straightforward cascaded inverter, and it was the simplest type carrier we felt we could make. Even though it is slow compared to the rest of the circuits, in the over-all system it contributes very little to it in time or calculations.

Win Soule (Digital Techniques): How do you obtain visual indication of flip-flop position?

Mr. Olsen: We drive incandescent bulbs with a jumping transistor—a hardly satisfactory way of doing it: 400 transistors drive 400 incandescent bulbs. This is probably the best system as a whole, because it is not too expensive. We have been looking for less expensive ways for getting information.

L. H. Crandon (Autonetics): Are there any other sensitive parameters, different from voltage, which are used in marginal checking?

Mr. Olsen: One of course, can spend a lifetime comparing every parameter with every other parameter. Marginal checking gives you very good measure of most sensitive areas, and this is the one we concentrated on, and we feel that this is a reasonable approach to it, when one is limited by a limited length of time.

R. O. Barnes (Boeing): How much circuitry is represented in one plug-in unit (as shown in the figure) *i.e.*, how many flip-flops per unit?

Mr. Olsen: The figure shows that it contained one of the ten transistor flip-flops, plus three volume transistors. Three is in one package of cross section of one by two inches, one flip-flop plus a little logic; eight to twelve converters, or eight to twelve interfollowers.

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The schematic diagram of an emitter follower and the symbol used by the logical designers is shown in Fig. 1.

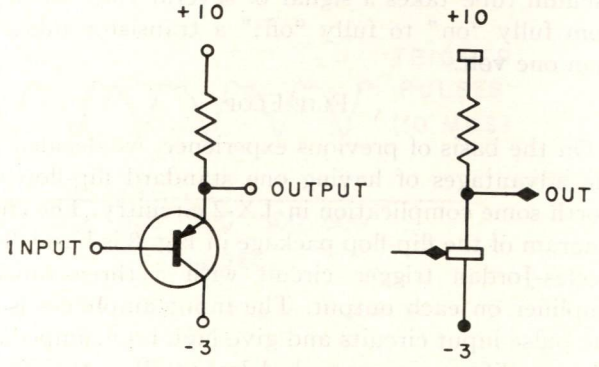

Fig. 1—Emitter follower.

* This work was supported jointly by the U. S. Army, Navy, and Air Force under contract with Mass. Inst. Tech.

† Lincoln Lab., M.I.T., Lexington, Mass.

With a negative input, the output is "shorted" to the −3-volt supply as through a switch. When several of these emitter followers are combined in parallel, as in Fig. 2, any one of them will clamp the output to −3 v.

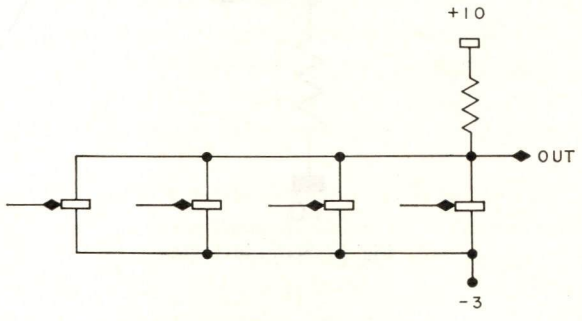

Fig. 2—Parallel emitter follower.

We have then an OR circuit for negative signals and an AND circuit for positive signals. The transistor inverter is shown in Fig. 3 (next page) with its logic symbol. Basic AND, OR circuits result from the connection of these simple switches in series or parallel (Figs. 4 and 5). More complex networks like the TX-2 carry circuit use these elements arranged in series-parallel (Fig. 6).

In Fig. 3 the resistor R_1 is chosen so that under the worst combinations of stated component and power

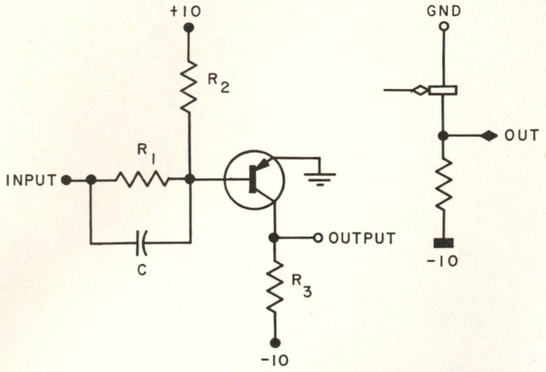

Fig. 3—Inverter.

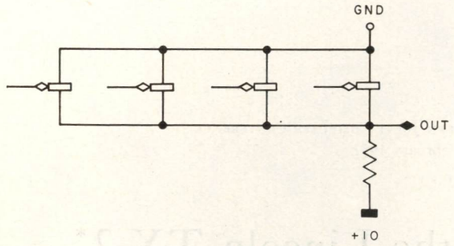

Fig. 4—Parallel inverters.

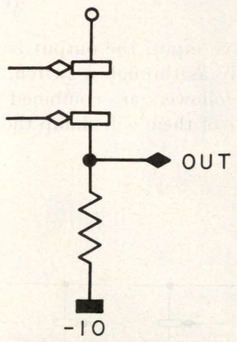

Fig. 5—Series inverters.

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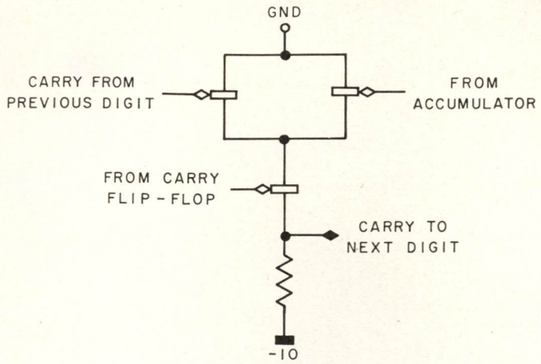

Fig. 6—TX-2 carry circuits.

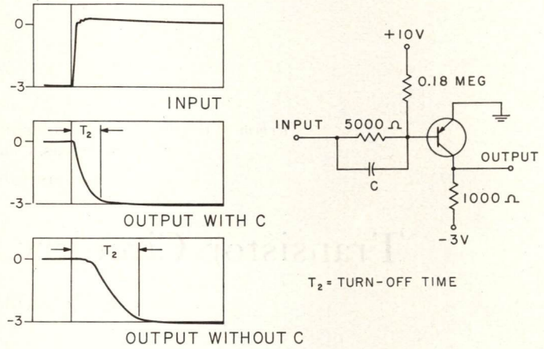

Fig. 7—Turn-off time.

without the need for clamp diodes. Unlike vacuum tubes which always need an appreciable voltage across them for operation, a transistor requires practically no voltage across it. In spite of the delay in turning off saturated transistors, these circuits are faster than most vacuum tube circuits. Faster circuit speed is not due to the fact that the transistors are faster than vacuum tubes, but because they operate at much lower voltage levels. A vacuum tube takes a signal of several volts to turn it from fully "on" to fully "off;" a transistor takes less than one volt.

Flip-Flop

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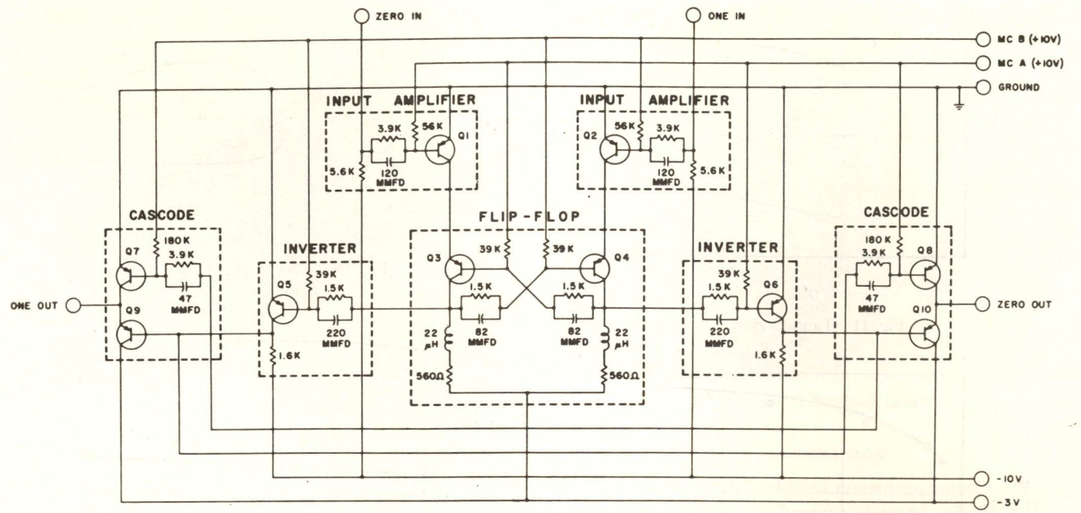

Fig. 8—TX-2 flip-flop.

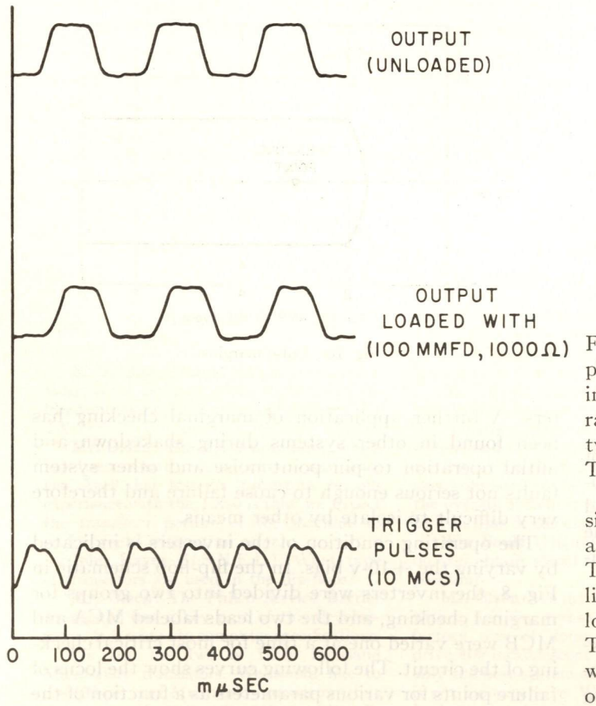

Fig. 9—Flip-flop waveforms.

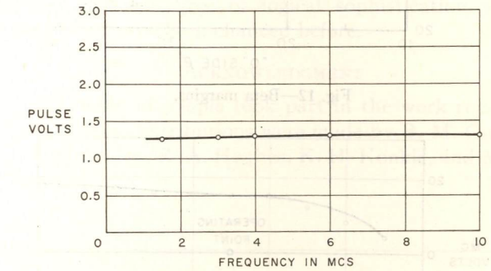

Fig. 10—Trigger sensitivity.

times, about 25 millimicroseconds, are faster than one normally sees in a single inverter, or an emitter follower because on each output there is an inverter that pulls to ground and an emitter follower that pulls to −3 v.

Fig. 10 is a plot of the pulse amplitude necessary to complement the flip-flop at various frequencies. Note the independence of trigger sensitivity to pulse repetition rate. This circuit will operate at a 10-megapulse rate, twice the maximum rate at which it will be used in TX-2.

The TX-2 circuits reproduced most often were designed with a minimum number of components to achieve economies in manufacture and maintenance. The design of less frequently reproduced circuits made liberal use of components—even redundancy to achieve long life and broad tolerance to component variations. The goal was system simplicity and high performance with a lower total number of components than might otherwise be possible. For example, the number of flip-flops in the TX-2 is small compared to the gates which transfer information from one group of flip-flops to another; so the flip-flops were allowed to be relatively complicated but the TX-2 transfer gates were made very simple. A transfer gate is only a single inverter. The emitter is connected to the output of the flip-flop be-

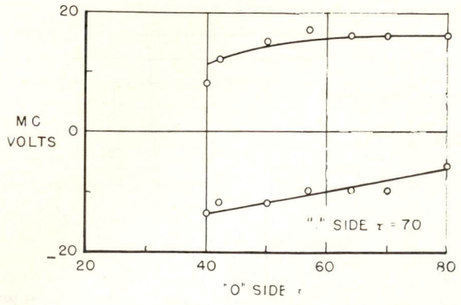

Fig. 11—Tau margins.

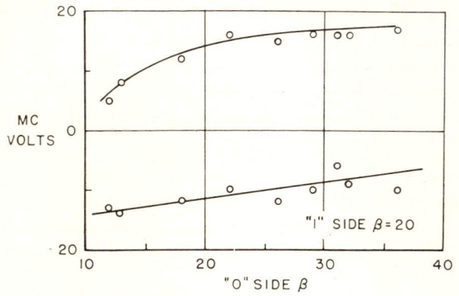

Fig. 12—Beta margins.

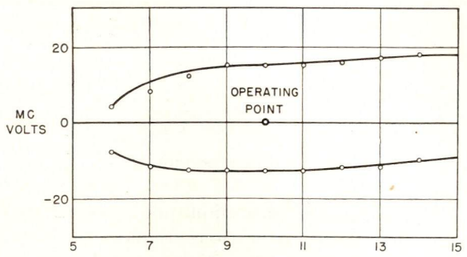

Fig. 13——10-volt supply margins.

ing read and the collector is connected to the input of the flip-flop being set. The output impedance of the flip-flop is so low that, when the output is at the ground level, a pulse on the base of the transfer gate shorts the input of the other flip-flop to ground and sets its condition.

Marginal Checking

We planned, of course, to incorporate marginal checking in the design of these circuits so that, under a program of regularly scheduled maintenance, deteriorating components could be located before they caused failure in the system. We also found it practical to use the technique during the design of the circuits to locate the design center of the various parameters and to indicate the tolerance of circuit performance to these parameters. A further application of marginal checking has been found in other systems during shakedown and initial operation to pin point noise and other system faults not serious enough to cause failure and therefore very difficult to isolate by other means.

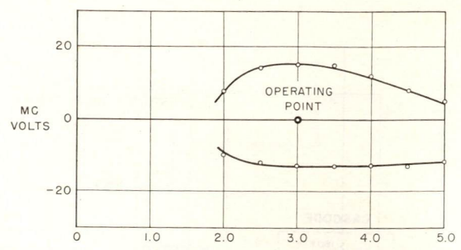

Fig. 14——3-volt supply margins.

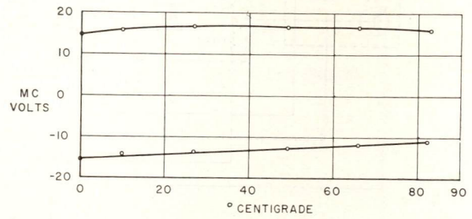

Fig. 15—Temperature margins.

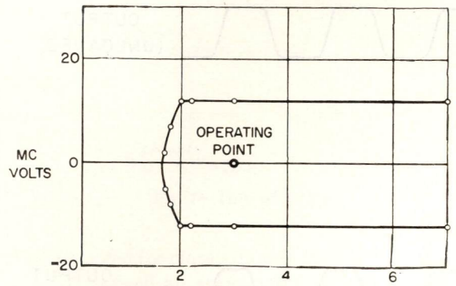

Fig. 16—Pulse margins.

The operating condition of the inverters is indicated by varying the +10-v bias. In the flip-flop schematic in Fig. 8, the inverters were divided into two groups for marginal checking, and the two leads labeled MCA and MCB were varied one at a time for most critical checking of the circuit. The following curves show the locus of failure points for various parameters as a function of the marginal checking voltage. Fig. 11 shows the tolerance to tau, a measure of hole storage and Fig. 12 shows the tolerance to beta, the current gain. Operating margins for supply voltages, temperature, and pulse amplitude are shown in Figs. 13 through 16.

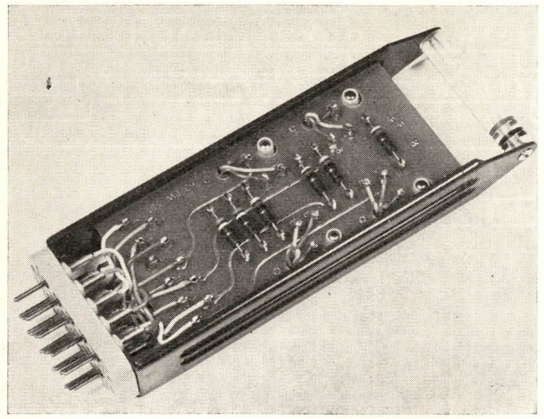

Fig. 17—TX-2 plug-in unit.

Packaging

The number of types of plug-in units was kept small for ease of production and to keep the number of spares to a minimum. The circuits are built on dip soldered etched boards and the components are hand soldered to solid turret lugs. The boards are mounted in steel shells shown in Fig. 17 to keep the boards from flexing. The male and female contacts are machined and gold plated. The sockets are hand wired and soldered in panels as in Fig. 18.

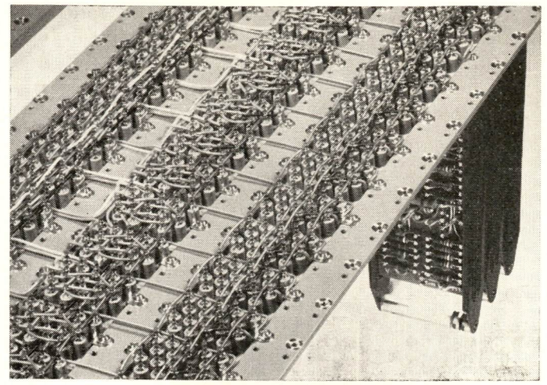

Fig. 18—TX-2 back panel.

Conclusion

The result of these design considerations is a 5-megapulse control and arithmetic element which will take less than 40 square feet of space and dissipate less than 800 watts of power. The simplicity of the circuits has encouraged a degree of logical sophistication which would not have been chanced before.

Acknowledgment

A number of people took part in the work reported here. Major contributions were made by B. M. Gurley, J. R. Fadiman, R. A. Hughes, K. H. Konkle, and M. E. Petersen.

Discussion

R. D. Gloor (Ramo-Wooldridge Corp.): What is the estimate of the expected mean-free-time between component failures for TX-2?

Mr. Olsen: The TX-0 Computer, which has been running eight hours a day since last April, has lost no transistors. So our experience with the TX-0 is that we expect the transistor portion of the machine to go for weeks without an error.

John Hayes (U.S.N.E.L.): What type of transistors are used in the flip-flops?

Mr. Olsen: The Philco Service Barrier Transistor was a key part of this development. It is tested to computer specifications.

We also use two or three thousand Micro-alloy transistors. We would like to use 100 per cent Micro-alloy transistors, but there were only two or three thousand available at the time we needed them. They have higher gains, particularly higher current, and appear to be much better transistors.

L. P. Retzinger (Litton): What is the propagation time per carry digit?

Mr. Olsen: About 40 millmicroseconds per digit. We made no effort to speed this up. This is a straightforward cascaded inverter, and it was the simplest type carrier we felt we could make. Even though it is slow compared to the rest of the circuits, in the over-all system it contributes very little to it in time or calculations.

Win Soule (Digital Techniques): How do you obtain visual indication of flip-flop position?

Mr. Olsen: We drive incandescent bulbs with a jumping transistor—a hardly satisfactory way of doing it: 400 transistors drive 400 incandescent bulbs. This is probably the best system as a whole, because it is not too expensive. We have been looking for less expensive ways for getting information.

L. H. Crandon (Autonetics): Are there any other sensitive parameters, different from voltage, which are used in marginal checking?

Mr. Olsen: One of course, can spend a lifetime comparing every parameter with every other parameter. Marginal checking gives you very good measure of most sensitive areas, and this is the one we concentrated on, and we feel that this is a reasonable approach to it, when one is limited by a limited length of time.

R. O. Barnes (Boeing): How much circuitry is represented in one plug-in unit (as shown in the figure) *i.e.*, how many flip-flops per unit?

Mr. Olsen: The figure shows that it contained one of the ten transistor flip-flops, plus three volume transistors. Three is in one package of cross section of one by two inches, one flip-flop plus a little logic; eight to twelve converters, or eight to twelve interfollowers.

Ken Olsen

High St.

INSTRUCTION CONTROL FRAME

TESTING

Abstract

This report contains a description of how the Instruction Control Frame will be tested and is written to familiarize new men in the group and any other interested parties in the test procedure planned as of now for testing the Instruction Control Frame.

The frame will be divided into two sections. Group "A," which will be assigned to Section one, will proceed to get the time pulse distributor and associated controls working. Group "B," which will be assigned to Section two, will proceed to get the command decoder operating. As it is planned now, each group will be able to work independently of each other. If one group falls behind schedule, the other group can switch over to help. A definite sequence of pluggable unit insertions in the frame has been listed for each group. The list includes sequence, type, and a short logical description of the pluggable unit use in the frame. This list is included in this report.

It is desirable that all who test the frame should use the log book in a manner that can be followed by any member of the Instruction Control Frame group, or any other interested party. In order to expedite this difficult task, Figure 1 illustrates how the framelog book will be kept.

The time pulse distributor and associated controls are almost entirely located at the left side of the frame. The command decoder is located at the right side of the frame. Each of these units can work independently of each other. This allows

a double barrel attack for testing the frame. When both these sections are working satisfactorily, the time pulses and +10 or -30 levels are at the correct pins of the command generators pluggable units for each instruction, then the command generators pluggable units will be inserted. The insertion of the command generators will be in an ordered sequence by registers or controls. Each will be checked out before the succeeding register or control is inserted. This will be done by putting the 48 instructions associated with XD-1 in the operation register and checking output points for commands associated with the instruction in the operation register.

With the command generators inserted and operating, another incomplete check will be made to be sure pulses associated with commands occur on the correct instructions. Next, the push button operations will be tested.

To facilitate the elimination of excess thumbing through block diagrams, a chart has been made for each of the 48 XD-1 instructions. These charts have pulse pin numbers, supressor grid pin numbers, tube numbers, locations, and driving circuits, etc. for each command associated with an instruction. Charts have also been made up for time pulses and instruction pulses which will indicate the destination of these pulses and what operation they perform.

In order to perform the tests indicated above, Figure 2 and Figure 3 show how test equipment will be wired to the frame.

It should be pointed out that it is very difficult to foresee all problems that will develop as testing of the frame progresses. The above procedure of testing may have to be changed. However, it is felt that our plan of attack will allow us to

proceed with testing in the quickest possible way with a maximum amount of reliability of data. Any suggestions for improvement of our test procedure will be welcomed.

R. W. Shur

LOG BOOK

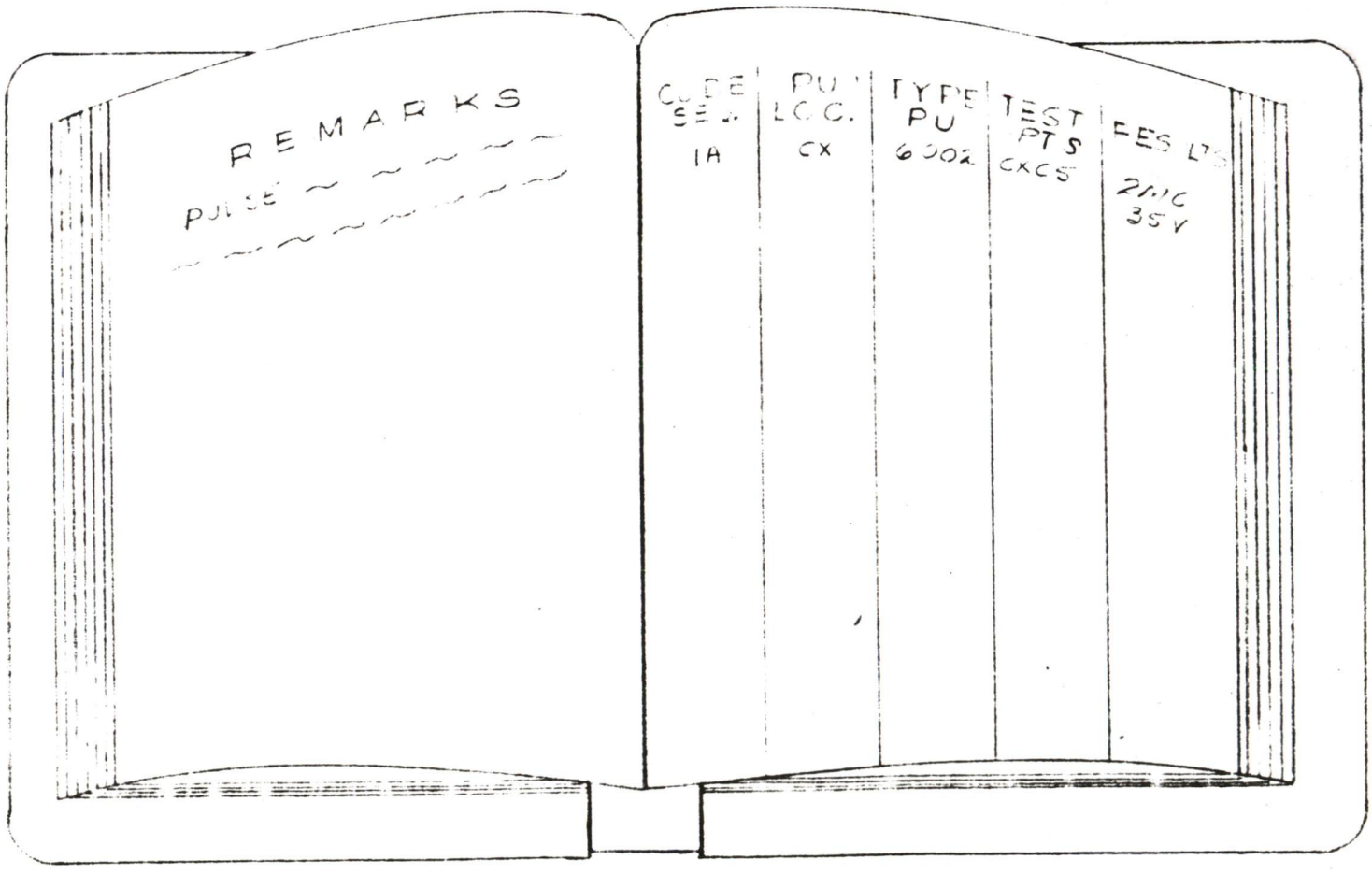

Fig. 1

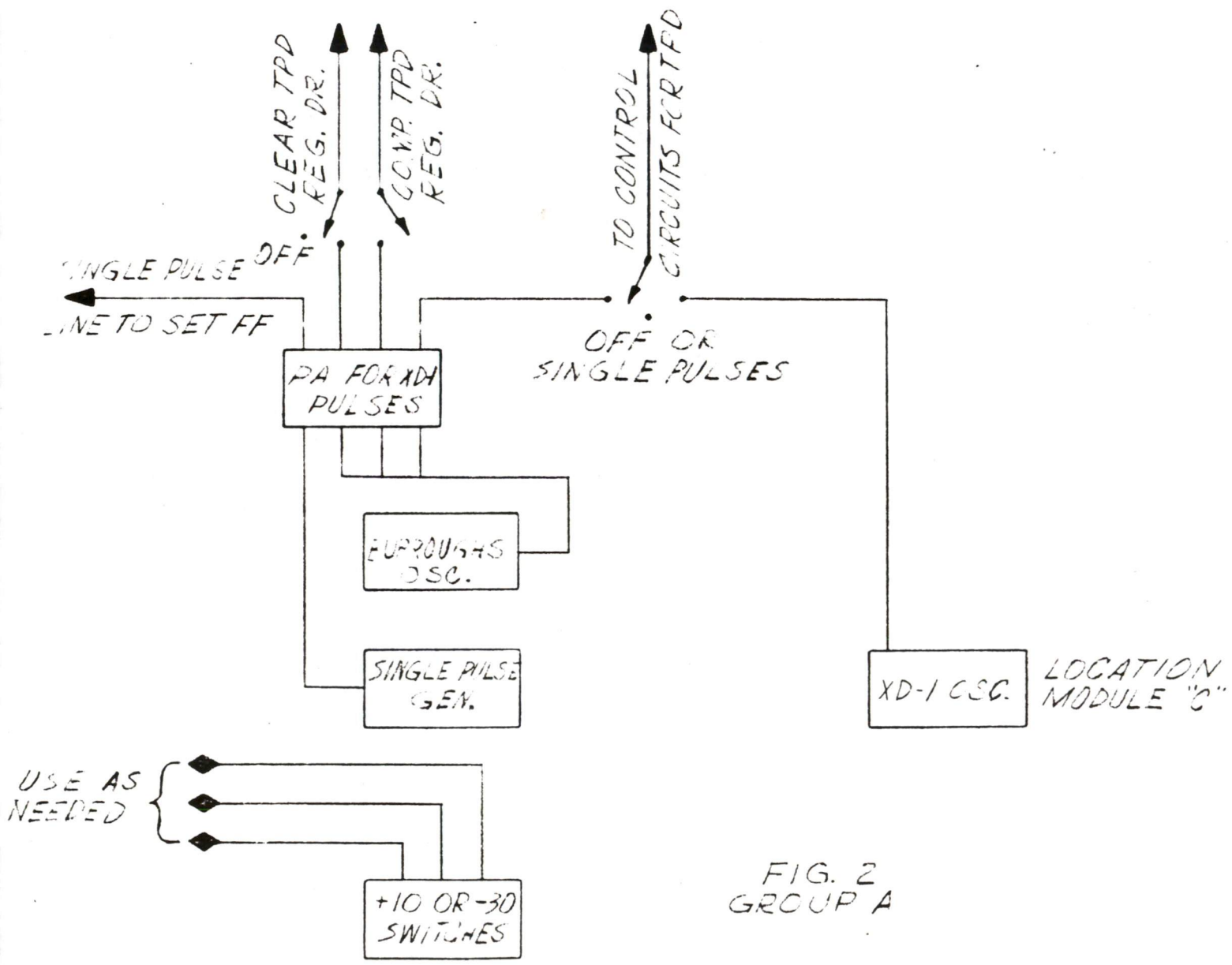
CLEAR TPD REG. DR.
COMP. TPD REG. DR.
TO CONTROL CIRCUITS FOR TFD
SINGLE PULSE OFF
LINE TO SET FF
OFF OR SINGLE PULSES
PA FOR XDA PULSES
EUPROUGHS OSC.
SINGLE PULSE GEN.
XD-1 OSC.
LOCATION MODULE "C"
USE AS NEEDED
+10 OR -30 SWITCHES

FIG. 2
GROUP A

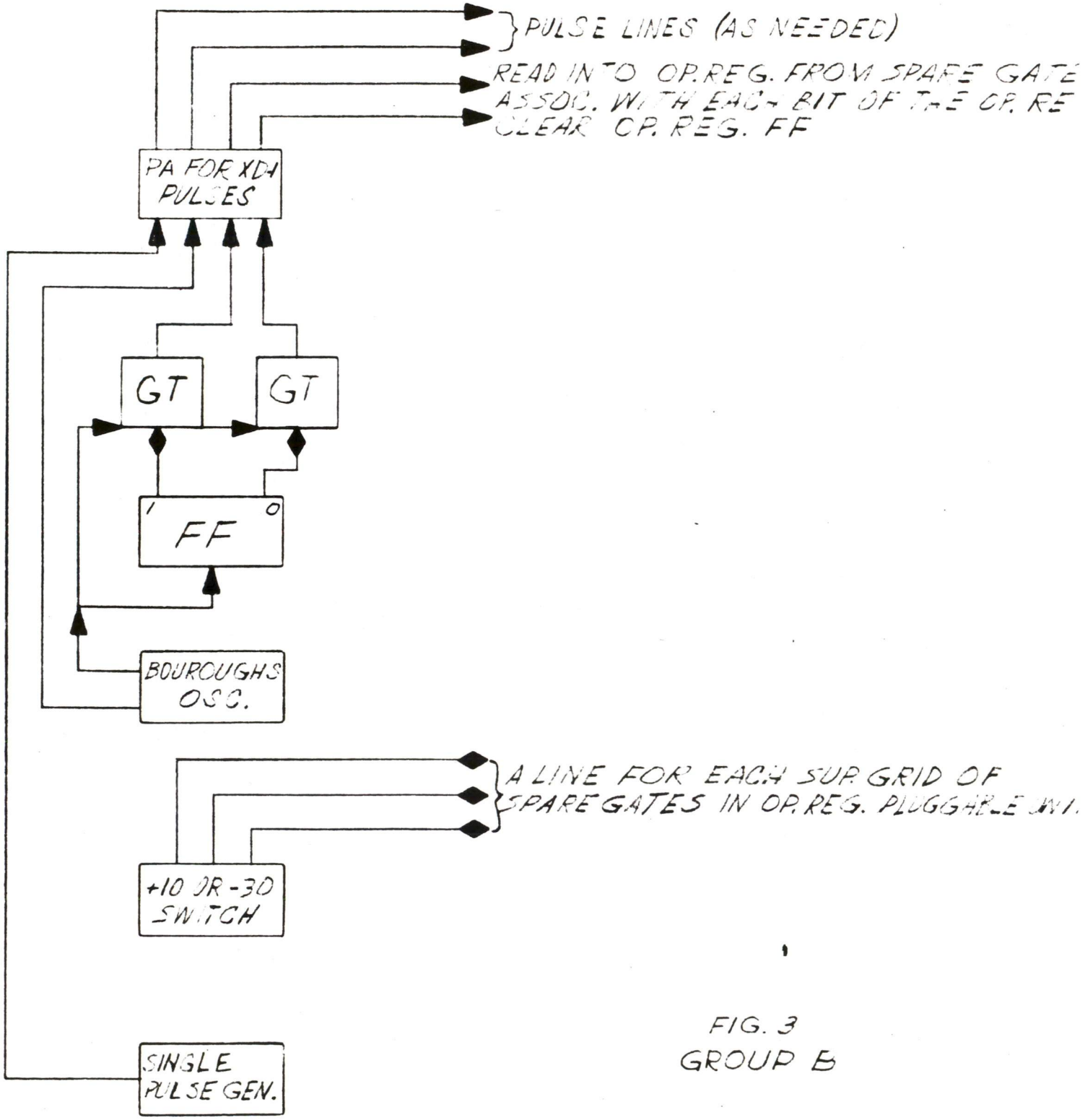
PULSE LINES (AS NEEDED)
READ IN TO OP. REG. FROM SPARE GATE
ASSOC. WITH EACH BIT OF THE OP. RE
CLEAR OP. REG. FF
PA FOR XDA PULSES
GT
GT
1
FF
0
BOUROUGHS OSC.
A LINE FOR EACH SUB GRID OF
SPARE GATES IN OP. REG. PLUGGABLE UNIT
+10 OR -30 SWITCH
SINGLE PULSE GEN.

FIG. 3
GROUP B

GROUP "A"

Pluggable Unit Sequence Insertion List

Sequence Code	Type	Location	Logical Definition
1 A	6002	4 CX	Oscillator
2 A	6020	4 BM	TPD Control FF Continue FF
3 A	6001	4 BG	Gate Tubes: TPD ON Continue No Break IO Interlock
4 A	6007	4 BF	P. A. - IP Driver 2 mc pulses Clear, comp. FF
5 A	6005	4 BN	2 mc FF Inst. Step. FF Memory Cycle FF
6 A	6007	4 BK	P. A. - TP Driver Clear, Comp. FF
7 A	6016	4 CD	R. D. - TP Register Driver IP Register Driver Clear Comp. TPD Register Driver
8 A	6008	4 CE	TPL - 0
9 A	6024	4 CF	TPL 1
10 A	6024	4 CG	TPL 2
11 A	6024	4 CH	TPL 3
12 A	6024	4 CJ	TPL 4
13 A	6024	4 CK	TPL 5
14 A	6024	4 CL	TPL 6

Sequence Code	Type	Location	Logical Description
15 A	6024	4 CM	TPL 6 A
16 A	6008	4 CN	TPL 7
17 A	6024	4 CP	TPL 8
18 A	6024	4 CR	TPL 8 A
19 A	6024	4 CS	TPL 9
20 A	6024	4 CT	TPL 10
21 A	6024	4 CU	TPL 11
22 A	6024	4 CV	TPL 11 A
23 A	6024	4 CW	TPL 11 B
24 A	6016	4 EC	IP 9 Driver IP 10 Driver IP 7 Driver IP 0 Driver IP 8 Driver Comp. DVTPD; Step Counter, and Mem. Sel. FF's
25 A	6016	4 FC	2 mc Driver IP 5 Driver IP 6 Driver IP 11 Driver
26 A	6016	4 ED	IP 3 Driver IP 1 Driver IP 2 Driver IP 4 Driver Clear Step Counter DVTPD, Mem Sel. FF
27 A	6005	4 CD	DVTPD 0, 1, 2
28 A	6005	4 DC	DVTPD 3, 4
29 A	6007	4 DD	P. A. Drivers for DVTPD 0, 1 2, 3, 4 Clear Step Counter and DVTPD - PT 6 Add one to Step Counter

Sequence Code	Type	Location	Logical Description
30 A	6010	4 BJ	Pause FF
31 A	6010	4 BE	Break FF
32 A	6001	4 BD	Gate Tubes; Pause ff On (Clear Sync)
33 A	6018	4 BH	Pause "&" No Break Break "OR" No pause
34 A	6001	4 FM	Instruction Control Command Generator
35 A	6007	4 FN	"
36 A	6001	4 FP	"
37 A	6007	4 FR	"
38 A	6001	4 EE	Index Command Generator
39 A	6007	4 ED	Index Command Generator
40 A	6001	4 EH	Program Control Command Generator
41 A	6001	4 EK	"
42 A	6007	4 EJ	"
43 A	6001	4 DX	Memory Buffer Command Generator
44 A	6007	4 DY	Memory Buffer Command Generator
45 A	6001	4 EL	A Register Command Generator
46 A	6001	4 EP	A Register Command Generator
47 A	6007	4 EM	A Register Command Generator
48 A	6007	4 EN	A Register Command Generator

Sequence Code	Type	Location	Logical Description
49 A	6001	4 ER	Adder Command Generator
50 A	6001	4 EU	Adder Command Generator
51 A	6007	4 ESq	Adder Command Generator
52 A	6007	4 ET	Adder Command Generator
53 A	6001	4 FH	B Register Command Generator
54 A	6001	4 FL	B Register Command Generator
55 A	6007	4 FJ	B Register Command Generator
56 A	6007	4 FK	B Register Command Generato r
57 A	6001	4 FS	Accumulators Command Generato:
58 A	6001	4 FT	Accumulators Command Generato:
59 A	6001	4 FW	Accumulators Command Generato:
60 A	6001	4 FX	Accumulators Command Generato:
61 A	6001	4 GX	Accumulators Command Generato:
62 A	6007	4 FU	Accumulators Command Generato:
63 A	6007	4 FV	Accumulato rs Command Generato:
64 A	6007	4 GX	Accumulators Command Generator
65 A	6007	4 GY	Accumulators Command Generator
66 A	6001	4 EW	Input-Output Command Generator
67 A	6007	4 EX	Input-Ou tput Command Generator
68 A	6001	4 FD	Selection Control Command Generator
69 A	6001	4 FF	Selection Control Command Generator
70 A	6007	4 FE	Selection Control Command Generator

GROUP "B"

Code Sequence for Pluggable Unit Insertion

Sequence Code	Type	Location	Logical Description
1 B	6007	4 HX	P. A. - Clear and Comp. Cycle Control and Operation Register
2 B	6016	4 HY	R. D. - Drivers for Clear and Comp. Cycle Control and Operation Register
3 B	6010	4 HU	A, B FF
4 B	6010	4 HT	PT, OT, FF
5 B	6010	4 JY	Bits 1-10 of Operation Register
6 B	6010	4 JY	Bits 1-10 of Operation Register
7 B	6010	4 JW	Bits 1-10 of Operation Register
8 B	6010	4 JV	Bits 1-10 of Operation Register
9 B	6010	4 JU	Bits 1-10 of Operation Register
10 B	6010	4 JT	Bits 1-10 of Operation Register
11 B	6010	4 JS	Bits 1-10 of Operation Register
12 B	6010	4 JR	Bits 1-10 of Operation Register
13 B	6010	4 JP	Bits 1-10 of Operation Register
14 B	6010	4 JN	Bits 1-10 of Operation Register
15 B	6017	4 JM	Mult - OT Mult - PT
16 B	6017	4 J	Mult
16 B	6017	4 JL	Shift Misc - OT Misc - PT Misc

Sequence Code	Type	Location	Logical Description
17 B	6017	4 JK	Add - OT Add - PT IO - OT IO - PT
18 B	6017	4 JJ	Reset Store - OTB Store - OTA Store - PT
19 B	6017	4 JH	Branch - OT Branch - PT
20 B	6017	4 JG	Shift - fcl IO - rds Reset - adx IO - wrt
21 B	6017	4 JF	Mult- Mul Store - ech Branch - blm Mult - tmu Reset - xin Branch - brm Add - can Mult - dvd Shift - del Store - dep Add - din Mult - tdv Reset - xac
22 B	6017	4 JE	Add - csu Misc - ldb Store - lst Add - sub Store - rst Add - tsu Store - sta Shift - lsr Branch - bfz

Sequence Code	Type	Location	Logical Description
			Store - aor Shift - rsr Branch - bfm
23 B	6017	4 JD	Add - adb Branch - bsn IO - Sel Misc - csw Shift - asl Misc - slr Store - fst Shift - asr
24 B	6017	4 JC	IO - lde Misc - hit Add - cad Shift - jsl Misc - ctr Add - add Shift - dsr Misc - per Branch - bpx IO - sdr Add - tad
25 B	6017	4 HP	Index Selection Matrix
26 B	6010	4 DE	Step Counter and Controls
27 B	6010	4 DF	Step Counter and Controls
28 B	6010	4 DG	Step Counter and Controls
29 B	6010	4 DH	Step Counter and Contrds
30 B	6010	4 DJ	Step Counter and Controls
31 B	6010	4 DK	Step Counter and Controls

Sequence Code	Type	Location	Logical Description
32 B	6025	4 DL	Step Counter and Controls
33 B	6005	4 DM	Step Counter and Controls
34 B	6012	4 HC	In-out Class Instruction Matrix
35 B	6012	4 HE	In-out Class Instruction Matrix
36 B	6013	4 HD	In-out Class Instruction Matrix
37 B	6012	4 HF	Add Class Instruction Matrix
38 B	6012	4 HH	Add Class InstructionMatrix
39 B	6011	4 HG	Add ClassInstruction Matrix
40 B	6013	4 HJ	Add Class Instruction Matrix
41 B	6012	4 HK	Shift Class Instruction Matrix
42 B	6012	4 HN	Shift Class Instruction Matrix
43 B	6011	4 HL	Shift Class Instruction Matrix
44 B	6012	4 GC	Misc. Class Instruction Matrix
45 B	6012	4 GE	Misc. Class Instruction Matrix
46 B	6012	4 GF	Misc. Class Instruction Matrix
47 B	6013	4 GD	Misc. ClassInstruction Matrix
48 B	6012	4 GG	Branch Class Instruction Matrix
49 B	6012	4 GJ	Branch Class Instruction Matrix
50 B	6013	4 GH	Branch Class Instruction Matrix
51 B	6012	4 GK	Reset Class Instruction Matrix
52 B	6018	4 GL	Reset Class Instruction Matrix
53 B	6012	4 GM	Mult. Class Instruction Matrix
54 B	6012	4 GR	Mult. Class Instruction Matrix

Sequence Code	Type	Location	Logical Description
55 B	6011	4 GP	Mult. Class Instruction Matrix
56 B	6012	4 GS	Store Class Instruction Matrix
57 B	6012	4 GT	Store Class Instruction Matrix
58 B	6012	4 GV	Store Class Instruction Matrix
59 B	6011	4 GU	Store Class Instruction Matrix
60 B	6010	4 DN	Memory Unit Selection Controls
61 B	6010	4 DP	Memory Unit Selection Controls
62 B	6010	4 DS	Memory Unit Selection Controls
63 B	6023	4 DR	Memory Unit Selection Controls

SPECIFICATIONS OF THE
INSTRUCTION CONTROL FRAME
XD-1 INSTRUCTION EXECUTION

By

H. L. Kurkjian

January 7, 1954

ABSTRACT-- This report states the specifications of the Instruction Control Frame. It describes the basic computer memory cycles, and the functions of the circuits associated with the execution of the instructions. The report also describes in some detail the execution of each instruction associated with the XD-1 computer, and representative traffic diagrams are provided. A listing of the instruction traffic diagrams with logical and IBM numbers is given.

TABLE OF CONTENTS

INTRODUCTION

The purpose of this report is to describe the execution of the 49 instructions associated with the XD-1 computer. The specifications for the execution of the instructions by the circuits of the Instruction Control Frame. The instructions are described in some detail with representative traffic diagrams for each class of instruction. These representative traffic diagrams illustrate several instructions within the class. Traffic diagrams of instructions that are "unique" in a class are also attached. However, a listing of all the traffic diagrams is made and logical and IBM numbers are specified.

Whenever information is inserted or extracted from the computer memory, a memory cycle is required. The choice of the length of the memory cycle was based on considerations of fastest speed at which magnetic core memory can function. The length of the memory cycle presently is considered to be between 6 and 8 microseconds. Six microseconds represent the fastest speed at which magnetic core memory can operate reliably. The 6-microsecond interval is dictated by the speeds selected for the drum operations. The choice of the basic machine frequency was determined by the fastest reliable operation of the flip-flop which requires 0.5 usec. settling time. This represents a frequency of 2 megacycles. All circuits of the central computer are designed to function with a 6-microsecond memory cycle.

BASIC MACHINE CYCLES

There are two basic machine cycles referred to as program cycle and operation cycle. Each machine cycle consists of a group of 12, 0.1 usec. pulses spaced 0.5 usec. apart for a 6-usec. memory cycle. For memory cycles longer than 6 usec., additional time gaps are provided between time pulses 6 and 7, 8 and 9, 11 and 0. These additional time gaps are multiples of 0.5 usec.

In order to generate the 12 timed pulses, it was decided to provide a timed pulse distributor of the closed ring counter type. The TPD consists of 16 flip-flops arranged in a counter circuit which is advanced every 0.5 usec. and is therefore capable of generating 16 pulses, only 12 of which are used within a memory cycle. Thus, any variation of the length of the memory cycle from 6 microseconds will be in multiples of 0.5 microsecond. For every 0.5 microsecond reduction in the length of the memory cycle, one flip-flop would be removed from the TPD by appropriate changes of wiring.

The instructions (see references 1 and 7) of the XD-1 may be grouped in three categories, depending upon whether one, two, or three memory cycles are required for the execution of the instruction. In those instructions, which require one memory cycle for execution, the reference to memory is initiated and the instruction is decoded and executed. This category also includes instructions of the shift class which require additional time, but do not require an additional memory cycle since no

reference to memory is made. This additional time is referred to as "pause." During a pause, the time pulse distributor is stopped and 2 mc. clock pulses are supplied directly for the execution of 2 mc. operations. The duration of the pause is controlled by a counter, known as the step counter. When the counter is reduced to zero, an indication is given of the completion of 2 mc. operation, the TPD is restarted, and the generation of 2 mc. clock command pulses is stopped.

In those instructions requiring two memory cycles, timed pulses of the first memory cycle (program time) are used to start memory, to extract from memory the instruction to be executed, and to decode that instruction. During the following memory cycle (operation time) the operand is extracted from memory and the required arithmetic or logical operations are executed. In this category are also grouped the instructions which require a pause at the end of the two memory cycles. Again, during the pause 2 mc. operations take place. Instructions requiring the pause are those of the multiply and divide types. The duration of the pause is again controlled by the step counter.

Instructions which require three memory cycles for execution use one memory cycle for program time followed by two operation time memory cycles, operation time A and B. The operand is extracted from memory during the first operation time (OTA), an elementary arithmetic operation is performed on this operand, and then the result is returned to a specified memory address during the following memory cycle (OTB). The Store class

of instructions contains instructions of this type. It is to be noted that whenever an operation time memory cycle (without further identification) is mentioned, operation time A is to be understood.

TRAFFIC DIAGRAMS

The traffic diagrams represent in graphical form the means by which an instruction is executed and the time within the memory cycle when a particular command is executed. A command may be defined as an elementary operation on a register or on a control flip-flop. A number of typical traffic diagrams are included in this report. The traffic diagrams show several memory cycles on a sheet, each memory cycle being divided into twelve equal spaces, each division representing a 0.5 microsecond time interval. These diagrams, therefore, show the total time necessary to execute an instruction. It should be borne in mind that these diagrams represent memory cycles of six microseconds, since this is the minimum memory cycle length.

MEMORY CYCLES

A memory cycle starts with timed pulse zero (TP-0) and ends with timed pulse eleven (TP-11). At TP-3 of a program time memory cycle, memory is initiated by a "start memory" pulse. This pulse is fed into various delay lines to cause memory to cycle through a sequence of read, write and disturb actions. The 33-bit word is read out of the magnetic cores into the memory buffer registers at or before TP-6. The signal

levels of these flip-flop registers are used to write the same word back into the magnetic cores at TP-8. This action is required because the read out process is destructive. The address of the word read out of memory is indicated by the program counter.

At TP-7 a parity count is performed in the memory buffer registers. This operation takes 2.6 microseconds to complete. The count takes 33 x 0.035 = 1.16 microseconds where 33 represents the number of gate tube per word through which the parity check pulse must travel and 0.035 represents the delay per gate tube. An additional 0.5 microsecond is necessary for the parity flip-flop to settle, and the remaining 0.34 microsecond represents a safety factor.

The output pulses of the TPD are gated as instruction pulses (IP) or as timed pulses (TP). The instruction pulses are further gated in the command generators as either program time or operation time pulses e.g., PT-5 or OT-6.

The instruction cycle starts with PT-7 when the contents of the memory buffer register are transferred to the instruction register which was cleared at PT-6. The 32 bits from the memory buffer registers consist of left and right half words. The left half word is transferred to the operation register which contains circuits to decode the operation bits of the instruction to be executed. The right half word, which indicates the address in memory of the operand, is placed in the address register. The other functions of these two registers will be described later.

At PT-9, the decoding is completed and the necessary d.c. levels are generated to gate the 12 instruction pulses from the TPD for execution of the instruction. The interval from PT-7 to PT-9 is not available for the execution of commands.

On certain instructions it is necessary to modify the address part of the operand before it is extracted from memory. This process is referred to as "indexing an address" (see Reference 4), and the operation occurs at PT-9. At PT-11 a parity check is performed to determine the correctness of the parity bit associated with the instruction word. If at the end of this check the parity flip-flop indicated "1," a parity alarm signal is generated. This action completes the program time memory cycle. If the instruction requires an operation time memory cycle to follow, the operation time-program time (OT-PT) flip-flop is set to "operation time." During the execution of any given instruction, the program counter is advanced by one to indicate the memory address of the next instruction. During each operation time memory cycle, the contents of the address register are transferred to the memory address register at OT-1.

At TP-11 of every memory cycle, the computer senses whether any one of the input-output units has requested a memory break. If such a break has been requested, the computer control circuits assign a memory cycle for the transfer of a word. As a result of a break request, the logical and arithmetic operations in process cease, and memory is made available

to the input-output unit. During 2 mc operation (the pause condition) the computer senses for such breaks at a 2 mc rate.

Break cycles are further distinguished as break in and break out. A break in cycle is associated with the transfer of information from the selected input-output unit to the computer memory, a "read" operation. A break out cycle is associated with the transfer of information from the computer memory to an input-output unit, a "write" operation. A break cycle starts with TP-0 and ends with TP-11. The pulses of this type of cycle are referred to as break pulses, BP. The number of words to be transferred during any input-output operation is controlled by the IO word counter. Appropriate type breaks are requested until the requested number of words are transferred. It should be noted that an IO break does not interfere with the execution of an instruction except to delay its completion.

INSTRUCTION REGISTER

The other functions of the instruction register are the following:

Operation Register (left-half of instruction register):

1. Index indicator (bits 1 through 3) is used to select one of two index registers or the right accumulator register. These registers are used in instruction indexing operations (see Reference 4).

2. Instruction code (bits 4 through 10) is used to identify the instruction to be performed. The instructions of the XD-1 are grouped in eight classes. Within a class instructions are distinguished by variation. Bits 4 through 6 of the operation code indicate the class and bits 7 through 10 indicate the variation (see Reference 1).

3. Index interval (bits 10 through 15) is used with the instructions "Sense," "Select," "Operate," and "Branch and Index" (see Reference 4). Other functions performed by these bits are:

   a. Bits 14 and 15 are used to indicate the mode of operation on the "overflow" feature.

   b. Bits 13 through 15 are used to indicate the mode of interleave operation to be used in reading or writing on the magnetic drums.

Address Register (right-half of instruction register)

1. Memory unit selector (bits 1 through 3) is used to select one of the following:

   a. Magnetic core memory 1 or 2.

   b. Test storage consisting of 16 registers. Fifteen of these registers are set up on a

plug board, and one is a flip-flop register. Test storage is used for testing memory and for testing other portions of the computer without the use of magnetic-core memory (see Reference 2).

c. Mechanical clock to obtain real time measurements (see Reference 3).

2. Address part (bits 4 through 15) is used to specify the addresses of the 4096 registers in magnetic core memory. Bits 5 through 13 specify the drum addresses, and bits 12 through 15 specify test storage addresses.

DESCRIPTION OF INSTRUCTIONS

There are 49 instructions associated with the XD-1 computer. These instructions are grouped in eight classes (see References 1 and 7). In describing the operations of these instructions, it shall be assumed that the program time memory cycle has been executed up to PT-9, and that the instruction has been decoded.

The choice of the airthmetic process for the XD-1 was based on selecting the process with the fastest multiplication time. As a result, the synchronized version of the asynchronous add-and-shift scheme was chosen. In this scheme, addition results in the displacement of the sum one position to the right a correction shift left must follow.

MISCELLANEOUS CLASS

The miscellaneous class of instructions contain those instructions which do not fit the other classes particularly well. The Shift Left and Round (slr) instruction was placed in this class because the circuits of the shift class became unnecessarily complicated if the slr instruction had to be accomodated there. Extract (et) Program Step (ps), Operate (op) and Load B Registers (ldb) take two memory cycles for execution. Clear and subtract word counter (csw) takes one memory cycle and Shift Left and Round requires one memory cycle and a pause.

The Operate instruction is executed in two memory cycles to reduce the number of cathode followers required to drive the 64-way matrix. At OT-9 an "operate" pulse initiates the selected operate unit.

The Extract instruction (et) is indexable; therefore, at PT-9 the address part is modified if required (see Reference 4). At PT-11 the cycle selector is set to operation time. at OT-1 the contents of the address register are transferred to the memory address register. At OT-7 the contents of the memory buffer registers are transferred to the A registers, and at OT-9 the logical multiply command is executed, i.e., if bit "X" of the A registers is zero, bit "X" of the accumulator registers is set to zero. If bit "X" of the A registers is one, bit "X" of the accumulator registers is left unchanged.

The Load B Registers instruction (ldb) is indexable. Prior to OT-7 the word specified by the address part of this instruction was extracted from memory and placed in the memory buffer registers. At OT-7, the contents

of the memory buffer registers are placed in the B registers which were previously cleared at OT-6.

The execution of the Program Stop Instruction (ps) is delayed if the IO interlock is ON. The IO interlock is sensed at PT-11. No commands are generated during the following operation time memory cycle. On PT-6 of the following memory cycle the computer stops. At PT-6 also the operation register has been cleared and the program counter has been advanced by one. On restarting, the computer will resume at PT-7 with the instruction whose address was held in the program counter.

The Shift Left and Round instruction (slo) is a shift left operation followed by a round operation whenever the necessary conditions are met. The number of times to shift is specified by the step counter which is set during program time to the value indicated by the address part of the instruction. The shift operation starts at PT-10 by initiation of 2 mc command pulses. The TPD is stopped at PT-11. A one is added to the step counter for every 2 mc operation. When the step counter is reduced to zero, the 2 mc shift operation is completed the TPD is restarted, and memory cycle is resumed with PT-0. It is apparent that if the number of shifts is less than two, the TPD need not stop. At PT-1, the A registers are cleared and both the left accumulator register and left B register are complemented by the "make positive" command pulse provided the left accumulator register sign bit equals one. Similar operations to those described are being executed by the right arithmetic element.

At PT-2 a round-off command is executed provided the left B register sign bit is one. The "left carry one" line of the left adder is pulsed to begin the addition. The addition requires 1.5 microseconds. The process of addition is described below. The carry operation is followed at PT-5 by a shift operation. At PT-6 the left B register is cleared and the left accumulator register is complemented if the left sign control flip-flop is indicating a one. This completes the execution of the instruction.

The purpose of the Clear and Subtract Word Counter instruction (csw) is to clear the right accumulator register and to replace its contents with the contents of the IO word counter. (It should be noted that the IO word counter is loaded with the one's complement of the contents of the address register on a Read or Write instruction. Thus at any time the IO word counter contains the one's complement of the number of words remaining to be transferred as a result of the Read or Write instruction which effected the setting of the counter.

In order to accomplish the csw instruction it is only necessary to clear the right accumulator register and to transfer the contents of the IO word counter to the right accumulator register. However a complication arises from the fact that the IO word counter is stepped from the drum controls by any synchronized oscillator pulse. There is a small finite possibility that the csw instruction will be executed while the IO word counter is in transition from one number to the next higher number. For this reason, two exclusive transfer commands are provided. If the IO word counter is

not being stepped at time one, the first transfer at PT-1 will be conditioned and the second transfer at PT-5 will be deconditioned. If however the B word counter is being stepped when PT-1 occurs, the first transfer is deconditioned, and the second transfer is conditioned.

ADD CLASS

The ADD class contains nine instructions. All of these instructions require two memory cycles to complete. This class is indexable. The normal entrance to the accumulator registers from the A registers is through the adders. The twin-type instructions involve the transfer of a left half word in memory to both accumulator registers, while the NOT-twin-type instructions the left half word from memory is transferred to the left accumulator register and the right half word to the right accumulator register. The process of subtraction involves addition of complements; consequently in any add-type instruction the contents of the A registers is added to the accumulator registers and the sums are placed in the accumulator registers.

The clear-type of add instructions are Clear and Add (ca), Clear and Subtract (cs) and Clear and Add Magnitudes (cm). In these instructions the accumulator registers are cleared at OT-6. At OT-7 the operand is extracted from memory and placed in the A registers. On the Clear and Add Magnitudes instruction the separate A registers are complemented if the sign bit of the particular A register is equal to one. On subtract-type of instructions the following operations described for only the left element, take place in both

arithmetic elements. The left A register is complemented by OT-9. The "left carry zero" command is generated at OT-10. Addition takes 1.25 microseconds to complete. Of this total time 16 x 0.035 or 0.56 microsecond is the time for the pulse to traverse 16 gate tubes; 0.5 microsecond is the additional time required for the last flip-flop to settle, and the remaining time is the safety factor. At PT-11 the PT-OT flip-flop is set to operation time. At OT-1 a shift command is given to correct the sums in the accumulator registers. In order to reduce equipment it was felt that the additional commands shown on timing diagrams 04.10.16, 04.10.24, 04.10.28 occuring on operation time should not be suppressed. These commands are required for the remaining instructions in the Add class and the commands have no harmful effect on the instructions just described.

The operations of the twin instructions, Twin and Add (tad) and Twin and Subtract (tsu) are similar to the Add and Subtract instructions, respectively. The operand is extracted at OT-7. In the subtract instructions the A registers are complemented at OT-9 and at OT-10 the carry zero lines to each of the adders are pulsed. On the following program time memory cycle, the A registers are cleared at PT-1 and a shift left command is executed. At OT-2 the end carry command is generated. This command takes 1.25 microseconds to complete. The end carry correction is followed at OT-5 with another shift left command. At OT-6 a "record overflow" command is given. This pulse examines the auxiliary overflow flip-flops. If either the left or right auxiliary overflow flip-flop is equal to one (indicating

overflow), the corresponding overflow flip-flop is set to an indicating condition and both auxiliary overflow flip-flops are cleared.

In order to execute the Add B registers to Accumulators instruction (ab) the contents of the B registers are placed in the A registers at OT-9, and the "carry in zero" command to begin addition is generated at OT-10. However, in order not to add additional equipment it was decided not to block the execution of OT-7 which operated on the A registers since these registers could be cleared at OT-8 before the contents of the B registers are transferred. The remainder of the instruction is similar to the Add instruction described above.

The difference between the instruction Difference Magnitudes (dm) and other add-type instructions is the conditions which must be met before the add process occurs. After extracting the operand from memory at OT-7, the A registers and the sign control flip-flops are complemented at OT-8 if the corresponding A register sign flip-flop is equal to one. Also at OT-8 the contents of both accumulator registers are transferred to the B registers which were previously cleared at OT-6. This transfer is made in order to retain the original contents of the accumulator registers. At OT-9 the A registers are complemented unconditionally. Both accumulator registers and sign control flip-flops are complemented provided the corresponding accumulator register sign bit is equal to one. These are the operations required before the computer may proceed with the normal add operation described above.

MULTIPLY CLASS

The multiply class contains four instructions: Multiply (mu), Twin and Multiply (tmu), Divide (dv) and Twin and Divide (tdv). The difference in operation between the twin and not-twin instructions has been described in the section on Add-type instructions. The basic arithmetic processes of multiply and divide have been described in reference 2.

In the multiply-type instructions the operand as usual is extracted from memory at OT-7. Also at OT-7 the step counter is set to 15 to indicate that 15 multiplication steps must be performed. The following description pertains to only one of the elements but it should be assumed that both elements are performing similar operations. The accumulator register holds the multiplier and is examined for its sign. If the accumulator sign flip-flop equals one, the accumulator register and sign control flip-flop (SCIF 04.10.32 04.10.33) are complemented. At OT-8 the contents of the accumulator register are placed in the B register and the accumulator register is cleared. The multiplicand which was placed in the A register at OT-7 is examined for sign. If the A register sign equals one the A register is complemented and the sign control FF is complemented again. Thus, by OT-9 the both multiplicand and multiplier are positive and the sign of the product is stored in the sign control flip-flop. Now 2 mc operation is started. At OT-11 the TPD is stopped, and the PT-OT flip-flop is set to program time. At each 2 mc operation the step counter is reduced by one. When the step counter is equal to five the TPD is restarted and the memory cycle is resumed

with PT-0. Multiplication is completed within this memory cycle. The end of 2 mc operation is indicated by the step counter being reduced to zero. This overlap operation results in a time saving since the time interval between PT-0 and PT-6 is utilized. By PT-5 multiplication is completed and the step counter controls are cleared. The remaining command pertains to the correction of sign at PT-5. In this operation, the sign control flip-flop is examined. If the flip-flop indicates one, the accumulator register and B register are complemented and the sign control flip-flop is cleared. Both accumulator and B registers enter into the complementation process, because these registers together hold the signal 32-bit product.

On divide-type instructions, the dividend is contained in the combined accumulator and B registers. Again the description will be given as though only one arithmetic element were operating. At OT-7 the dividend is examined for sign. If the accumulator register sign bit is one the accumulator register B register and the sign control flip-flop (SCFF 04.10.34 04.10.35) are complemented. At OT-7 the step counter is set to 17 and the divisor is placed in the A register. At OT-8 the sign of the divisor is examined. If the A register sign flip-flop is indicating a one, the A register and the sign control flip-flop are complemented. The 2 mc operation is started at OT-9. A basic divide 2 mc operation consists of 4 steps which are controlled by the divide timed pulse distributor. The step counter is advanced once for each divide cycle. Therefore, to execute

a divide-type instruction 16 x 5 = 80 pulses are required. One of the five pulses is used only to obtain a necessary delay. As soon as the step counter is reduced to zero, the TPD is restarted and program time memory cycle is resumed with PT-0. The remaining commands deal with the correction of the remainder at PT-2 and correction of signs at PT-6. To correct the remainder, the A register sign flip-flop is examined. If this flip-flop indicates zero the "carry zero" line is pulsed. This is followed at PT-5 by a shift left command. Final correction of signs was described as a part of the multiply instructions.

STORE CLASS

The Store Class contains 7 instructions. This class is indexable. All the instructions, except the Store (st) instruction, require 3 memory cycles to complete. In general, the computer control circuits begin with program time, at PT-11. This cycle is followed by OTA, and memory cycle OTB follows. The store instruction requires two memory cycles. It is unlike the other instructions that require 2 memory cycles in that program time is followed by OTB instead of OTA.

In all the instructions of this class, except Store, following commands are executed: At OTA-0 the memory address register is cleared, and at OTA-1 the contents of the address register are transferred to the memory address register. At this time the memory buffer registers are cleared in preparation for the transfer of the operand from the memory register. At

OTA-6, the A registers are cleared, and at OTA-7 the contents of the memory buffer registers are transferred to the A registers. When executing the Deposit instruction, the A registers are not cleared at OTA-6. The new word from the memory buffer registers is read into the A register at OTA-7 on top of the word already there. When executing the Store Address instruction, the commands at OTA-6 and OTA-7 concern only the left A register instead of both A registers. At OTB-1 the contents of the address register are once more transferred to the memory address register which was cleared at OTB-0. The memory buffer registers are cleared in preparation for subsequent transfers of information. In all the instructions of this class, the "record overflow" command is executed. This command is unconditional and causes no harmful affect on any of the instructions of this class. The commands peculiar to each instruction will now be described.

The Left Store instruction (lst) is completed when at OTB-2 the contents of the right A register are transferred to the right memory buffer register and the contents of the left accumulator register are transferred to the left memory buffer register. The contents of the right A register represent the half-word originally stored in memory. This half-word was transferred from the right memory buffer register to the right A register at OTA-7 to prevent the destruction of this word through the occurrence of an IO break between the A and B operation time memory cycles.

The Right Store instruction (rst) is similar to the instruction described above except that at OTB-2 the contents of the left A register are transferred

to the right memory buffer register.

The Store Address instruction (sta) is similar to the Right Store instruction, except that the contents of the A registers are transferred to the memory buffer registers at OTE-2 time.

The purpose of the Add One instruction (rao) is to add a one to the least significant digit of the right half of the specified memory register. In order to accomplish this action, the accumulator register and the adder circuits must be used. Consequently, at OTA-6 the right accumulator register is cleared. At OTA-8, that is, after the word has been placed in the A registers, the "right carry one" line is pulsed to cause a one to be added to the contents of the right A register and the right accumulator register. This sum is placed in the right accumulator, but displaced one position to the right. Hence, at OTA-11 a shift left command is executed. In the following memory cycle at OTB-1 time, a "right end carry after add one" command is executed if the right carry flip-flop is equal to one. In the particular case in which an end carry would occur, it is only necessary to set the fifteenth bit of the right accumulator to one. An actual addition for this correction is not required. The right carry flip-flop is cleared. At the completion of this sequence of commands a one has been added to the least significant digit of the number obtained from the specified right memory register. At OTB-2 the contents of the right accumulator register are transferred to the right memory buffer register, and the contents of the left A register are transferred to the left memory buffer register.

In the Exchange instruction (ec), the contents of the specified memory register and the contents of the accumulator registers are interchanged. In the execution of this instruction the contents of the accumulator registers are transferred to the memory buffer registers at OTB-2 time. Previous to this time, it was necessary to transfer the original contents of the specified memory register to the A registers via the memory buffer registers. After the original contents of the accumulator registers are transferred to the memory buffer registers at OTB-2 time, the accumulator registers are cleared at OTB-6. At OTB-10 the "carry zero" lines are pulsed to cause the addition of the contents of the A registers and the cleared accumulator registers. This action is followed at PT-1 by a shift left operation and at PT-6 by "record overflow." The timing of the above "add type" commands was made consistent with the regular Add class instructions.

Deposit -dep 04.10.52

The Deposit instruction (dep) is described in reference 7. In the execution of this instruction the A registers are cleared at OTA-1 time. At OTA-2 the contents of the accumulator registers are complemented. At OTA-4 the contents of the B register are transferred to the A registers and at OTA-5 the "logical multiply" command is executed. (See description of Extract instruction in the miscellaneous class.) The result of the logical multiply command is now in the accumulator registers. The new word is extracted from memory at OTA-7 and placed in the A registers. This transfer combines with the previous information of the A registers. At OTA-7 the

the accumulator registers are complemented once again, followed by another "logical multiply" command at OTA-9. Thus, the contents of the B registers have determined what binary positions of the specified word in memory are to be replaced by the corresponding binary positions of the accumulator registers. The contents of the B registers are not affected, however, the contents of the accumulator registers are transferred to the memory buffer registers for storage in the magnetic-core memory.

The Store instruction (st) requires that the contents of the accumulator registers be transferred to the memory buffer registers for storage in the magnetic-core memory. The contents of the accumulator registers are unchanged; however, the original contents of the indicated memory register are lost.

SHIFT CLASS

The Shift class contains eight instructions, each of which is similar to either the Shift Left or the Shift Right instruction. The execution of the instructions in this class requires the accumulator registers and the B registers to be connected in several ways (see reference 6). Both registers are capable of shifting their contents one position to the right or one position to the left. In the accumulator registers, the bit in position 1 is lost when left shifts are executed. This bit is not lost on cycle instructions. Similar statements apply to the bit in position 15 or other of the instructions of this class.

In all these instructions the address part of the instruction specifies the number of times to shift, and a maximum of 64 shifts is provided. At

At PT-10 the shift operation is started. For every 2 mc shift operation the step counter which contains the number of times to shift is reduced by one. At PT-11 the TPD is stopped, and only 2 mc shift command pulses are now available. When the step counter has been reduced to 5, the TPD is restarted and the regular program time memory cycle is resumed with PT-0. When the step counter has been reduced to zero 2 mc command pulses are stopped since the shift operation is completed. The TPD is restarted and the memory cycle is resumed when the step counter is reduced to five to save time. Six 0.5 microsecond intervals are available between PT-0 and PT-6, at which time the operation register is cleared and the instruction is lost. Six shift operations could therefore be accommodated. However, only four shift operations are performed to make the operation consistent with the Multiply instructions. If the specified number of shifts is five or less, the TPD need not be stopped. The "A" and "B" notes on all the traffic diagrams of this class indicate the type of accumulator register and B register operations respectively.

BRANCH CLASS

The Branch Class contains six instructions. This class is not indexable. The Sense and Branch on Zero instructions require two memory cycles. Branch on Minus, Branch and Index, Branch on Left Minus, and Branch on Right Minus are one-memory-cycle instructions. The Sense instruction was made a two-memory-cycle instruction to reduce the number of cathode

followers required to drive the selection matrix.

The execution of the Branch on Minus, Branch on Left Minus, and Branch on Right Minus instructions are very similar, only the conditions to be met are different. In these instructions, the normal execution of instructions from sequential addresses is interrupted if the numbers in the left and right accumulator registers are both negative, or if the number in the left accumulator register is negative, or if the number in the right accumulator register is negative, respectively. At PT-9 the right A register is cleared and the appropriate accumulator register sign bits are examined. If the appropriate sign bits are equal to one, the branch flip-flop is in an indicating condition, the contents of the address register are transferred to the program counter on the following PT-0 pulse. Thus, the program counter is set to the address of the next instruction to be executed. The branch flip-flop is cleared at PT-6 time. If the sign conditions had not been met, the branch flip-flop remains in a cleared condition, and the contents of the program counter are not altered.

The Sense instruction (su) determines the status of a selected electrical terminal, and an unconditional branch of control is executed if a suitable electrical signal exists at the terminal. At OT-9, a sense command is generated which causes the status of the "sense terminal" to be examined. If the condition is met, the branch flip-flop is set to an indicating condition at OT-9. Consequently, at OT-11 the program counter is transferred to the right A register, which was cleared at PT-9 of the previous memory cycle.

The program counter is cleared on OT-11. At PT-0 of the following memory cycle, the contents of the address register are transferred to the program counter. The branch flip-flop is cleared at PT-6, since the instruction is completed.

The Branch on Zero instruction (bs) causes the A register to be cleared unconditionally the contents of the program counter to be transferred to the right A register, and the address of the next instruction to be placed in the program counter, provided the contents of the accumulator registers are plus or minus zero.

At OT-1 the A registers are cleared. The sign bit of each accumulator registers is examined. The accumulator register having its sign bit equal to one is complemented, and the sign control flip-flop is complemented. At OT-2 the accumulator registers are both complemented again; this makes both accumulator registers negative. At OT-3 the "carry one" lines are pulsed, and a carry will result if all of the bits of accumulator registers are one, i.e., negative zero. This action is followed at OT-6 by a correction shift left operation. The restoring operation begins at OT-7, and is conditional on the status of the sign control flip-flops of the respective accumulator registers. If a sign control flip-flop is zero, the corresponding accumulator register is complemented at OT-7. At OT-8 the sign bits of the accumulator registers are examined. If both sign bits are qual to one, the branch flip-flop is set to an indicating position. Also at this time the "carry one" lines are pulsed followed by the shift left commands at OT-11. If the branch flip-flop

is in an indicating condition, the contents of the program counter are transferred to the right A register and the program counter is cleared at OT-11 time. At PT-0 of the following memory cycle, the contents of the address register are placed in the program counter. At PT-6 the sign control flip-flops are examined; if either flip-flop is in the one-condition the corresponding accumulator register is complemented. Both sign control flip-flops are cleared at PT-6 time.

The execution of the Branch and Index instruction (bi) is contingent on the sign of the specified index register. At PT-9 the sign bit of the specified index register is examined. If it is equal to zero the branch flip-flop is set to an indicating condition and the right A register is cleared. At PT-11 the contents of the program counter are transferred to the right A register, and the program counter is cleared. At PT-0 of the following memory cycle, the contents of the address register are placed in the program counter, and the address register is cleared. The new contents of the program counter provide the address of the next instruction to be executed. At PT-1 the complement of the index interval is transferred to the address register, and the contents of the specified index register are added to the contents of the address register at PT-2. The process of addition including the propagation of the carry is completed by PT-6. Thus, the contents of the specified index register are reduced by the value specified by the index interval. However, if no index register were specified or if the right accumulator (which may under certain circumstances be used as an index register) is specified,

the result is an unconditional branch. In this case contents of the index interval are meaningless.

INPUT-OUTPUT CLASS

The Input-Output class contains five instructions, and all instructions of the class are indexable. These instructions are associated with the execution of a break-in or a break-out cycle when the computer makes memory available to a selected in-out unit. The execution of the instructions of this class is contingent upon the input-output interlock being in an off-condition. If the IO interlock is in an on-condition, the execution of these instructions are delayed until the interlock is cleared. The Load Address Counter, Read, and Write instructions require one memory cycle, and the Select and Select Drums instructions require two memory cycles.

The Load IO Address Counter instruction (lac) is used to indicate the address of the first magnetic core memory location involved in a subsequent read or write operation. At P T-11 the IO interlock is sensed. If the interlock is in an on-condition, the pause flip-flop is set to an indicating condition. The TPD is stopped by the pause condition. During the pause condition, sensing for an IO break are made at a 2 mc rate. When the IO interlock is cleared, indicating completion of the IO break previously in progress, the computer proceeds with the instruction. At P T-2 the IO address counter is cleared, and at P T-3 the contents of the address register are transferred to the IO address counter. The contents of the address register at this time indicate the address in the magnetic-core memory from which or to which the first word of the

following input-output operation will be transferred.

The Select instruction(se) indicates the input-output unit, other than drums, which is to function during the following IO break operation. The IO unit is identified by the last six bits, 10 through 15, of the operation register. These are the same bits which are used as the index interval on other instructions. Two memory cycles are required for the execution of this instruction, since with this arrangement the number of cathode followers necessary to drive the matrix are reduced. The execution of this instruction is contingent on the IO interlock being in an off-condition. The interlock is sensed at OT-11. If the interlock is in an off-condition, the PT-OT flip-flop is set to PT, and the computer proceeds with the instruction. If the interlock is in an on-condition, the PT-OT flip-flop is set to PT and the pause flip-flop is set to the pause-condition, which causes the break request flip-flop to be sensed at a 2 mc rate. During the execution of the Select instruction, a deselect pulse is generated at PT-1. This pulse resets the selection flip-flops associated with the previously selected input-output units. At PT-3 the contents of the address register are transferred to the drum control register, which had been cleared at PT-2. This transfer causes no harm and is permitted to make the Select instruction consistent with the Select Drums instruction. At PT-5, a select command is executed. This command examines the SeOpCn matrix to see which input- output unit has been selected. As a result of this operation the selection flip-flops associated with the desired input-output unit are set to an indicating condition.

The Select Drums instruction is similar to the Select instruction. It is used to select a particular drum field associated with the drum system of the XD-1. The distinction between selecting drums and input-output devices other than drums became necessary when the total number of addresses required by the IO units exceeded 64. The execution of this instruction is contingent upon the IO interlock being in an off-condition. At PT-3 the contents of the address register are transferred to the drum control register which was cleared at PT-2. The drum control register now contains the starting address of the selected drum field. This command is also executed in those drum operations which require no starting address. At PT-5 the contents of the index interval are transferred to the drum selection register located in the Drum Frame. The necessary conditions for the execution of a break-in or break-out operation will be provided by the circuits of the Selection Control Element.

The Write instruction (wr) provides the necessaryconditions to effect the transfer of information from the magnetic-core memory at the computer to the selected output unit. The execution of the instruction is contingent on the IO interlock being in an off-condition. At PT-1 the IO interlock is set to its on-condition, and the IO word counter is cleared. At PT-2 the contents of the address register are transferred to the IO word counter, and the IO register is cleared. The IO word counter now indicates the number of words to be transferred. At PT-3 the IO word counter is sensed. If the contents of the counter are equal to zero, the IO word counter status flip-flop is set to

"equal to zero" and the IO interlock is cleared at PT-5. The operation of sensing the IO word counter requires 16 x 0.035 or 0.56 microseconds. Since the settling time of the status flip-flop is 0.5 microseconds, a total time of 1.5 microseconds is allotted. At PT-6 the write flip-flop is set to an indicating condition, and the index interval bits are sensed for the interleave mode.

The execution of the Read instruction (rd) is very similar to that of the Write instruction. The only difference in the two instructions being that in this instruction the read flip-flop is set to an indicating condition at PT-6 time, instead of the Write flip-flop. Again, the control of the actual reading operation is performed by circuits of the Selection Control Element.

RESET CLASS

The Reset Class contains three instructions. All of these instructions deal with the index register specified by the index indicator, bits 1 to 3 of the operation register. The instructions are not indexable. All of the instructions in this class require one memory cycle to complete.

The Reset Index Register instruction (ria) sets the specified index register to the value indicated by the address part of the ria instruction. At PT-4 the specified index register is cleared. At PT-6 the contents of the address register are transferred to the specified index register.

The Reset Index Register from the Right Accumulator instruction (rir) sets the specified index register to the value indicated by the contents of the right accumulator register. In the execution of this instruction the contents of the right accumulator register are first transferred to the address register

at PT-10, the address register having been cleared at PT-9. As in the ris instruction, during the following program time memory cycle the specified index register is cleared at PT-4, and the contents of the address register are transferred to the specified index register at PT-6. The reason why PT-4 and PT-6 were chosen in the above two instructions was to make these commands consistent with the commands of the Branch and Index instruction.

In the Add Index Register instruction (ais) the contents of the specified index register are added to the contents of the address register at PT-9. At PT-10 the carry operation is started (the "adder" circuit used here is not the same as that used in the arithmetic element). The carry operation may take a maximum of 16 x 0.033 or 0.56 microseconds, so the operation is certainly complete by PT-0 of the following memory cycle. At PT-3 the right A register is cleared, and at PT-5 the modified contents of the address register are transferred to the right A register. At this point the value specified by the contents of the address register is the sum of the address specified by the ais instruction and the contents of the specified index register. If no index register is specified, then the original contents of the address register are transferred unmodified to the right A register.

TRAFFIC DIAGRAMS

A. Miscellaneous Class	
Program Stop	04.10.01
*Extract	04.10.02
Load B Register	04.10.03
Operate	04.10.04
*Clear & Subtract Word Counter	04.10.08
*Shift Left & Round	04.10.65
B. Add Class	
Clear & Add	04.10.24
*Add	04.10.16
Twin & Add	04.10.27
Clear & Subtract	04.10.26
*Subtract	04.10.18
Twin & Subtract	04.10.19
*Clear & Add Magnitudes	04.10.28
Add B Register to Acc	04.10.23
C. Multiply Class	
*Multiply	04.10.32
Twin & Multiply	04.10.33
*Divide	04.10.34
Twin & Divide	04.10.35
D. Store Class	
Store	04.10.48
Left Store	04.10.49
Right Store	04.10.50
*Store Address	04.10.51
*Add One	04.10.54
Exchange	04.10.56
*Deposit	04.10.52
E. Shift Class	
*Shift Left	04.10.64
*Shift Right	04.10.66
Shift Accumulators Left	04.10.68
Shift Accumulators Right	04.10.70
Left Element Shift Right	04.10.79

* The traffic diagrams indicated with an asterisk are enclosed in this report.

Right Element Shift Right	04.10.74
Cycle Left	04.10.72
Cycle Accumulator Left	04.10.76
F. Branch Class	
*Branch & Index	04.10.80
Sense	04.10.81
*Branch on Minus	04.10.82
Branch on Left Minus	04.10.82
Branch on Right Minus	04.10.83
*Branch on Zero	04.10.84
G. Input-Output Class	
Load IO Address Counter	04.10.96
Select	04.10.98
Read	04.10.10
*Write	04.10.11
*Select Drums	04.10.97
M. Reset Class	
*Reset Index Register	04.10.12
Reset Index Register from Right Accumulator	04.10.13
*Add Index Register	04.10.14

* The traffic diagrams indicated with an asterisk are enclosed in this report.

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Instruction Control, Module 'C' Test Results

During the past two months, the Instruction Control group has carried out an extensive testing program which has included engineering design testing of the 18 pluggable unit types used in Instruction Control, and the preliminary testing and successful operation of one Module (C) used in the Instruction Control Frame. Members of the Instruction Control group and others have felt that a resume of our findings would be of interest to other groups whose schedule is not as advanced as ours. It was felt that a listing of the problems we encountered and the possible explanation and solution, if any, for these would be of great value to all concerned. Therefore, this report is written from a construction rather than a critical standpoint. In reading of the various problems mentioned here, one should not lose sight of the overall picture, which we feel to be very encouraging.

This report will consist of listing the various circuit, component, mechanical and wiring problems encountered at various periods during the testing which has been completed to date. It is realized that many of the facts and theories presented may be common knowledge. In order that nothing of importance be missed, it is meant to be as comphrensive as possible in the short space allotted.

The Instruction Control group would like to acknowledge the efforts of many others who have helped make the testing program a success.

The A Flip Flop Circuit

The A flip-flop is the only type used in the instruction frame. Five pluggable unit types containing this circuit were design tested. In addition, module C, which consists mainly of a 16 position ring, was operated successfully. Extensive

data, including marginal checking, was taken on the circuit during both types of testing. In general, the A flip-flop performed quite satisfactorily. All circuits were found to complement with a standard input pulse whose minimum amplitude ranged between 10 and 15 v. Several flip-flops were found to have an output whose upper level was +14 v. This is undesirable in most circuit application. A rough check indicated that the probable cause of this bias buildup was due to high forward resistance in the +10 v catcher diodes in the flip-flop circuit. The upper level of the grid of the cathode follower in the flip-flop was found to be +12v, rather than +10.5.

Marginal checking data on the A flip-flop was taken at a 200 KC P. R. F. A comparison of this data with marginal checking data taken at a 2 mc P. R. F., showed narrower margins at the high frequency. The decision to marginal check at the lower frequency was made in order to find possible unbalances in a flip-flop circuit which would tend to make it favor one state. This condition could be detected more readily at the lower P. R. F.

Mention should be made of the spurious pulse obtained on the output of the "off" side of a flip-flop when the "on" side is hit by consecutive pulses. This may approach 16 v in magnitude with 40 v input to flip-flop and is a 0.2 microsecond pulse. It seemed possible, in synchronizing flip-flop logical applications present in the instruction frame, that a gate tube could be triggered at an improper time by this spurious pulse appearing on the gate tube suppressor grid. A pluggable unit having an A flip-flop with a gate on the "O" side was pulsed consecutively with the "1" side "on," and at the same time the control grid of the gate tube was hit by the

same pulse. With a 40 volt pulse applied, a 16 volt pulse appeared on the gate tube suppressor grid. The output of the gate tube showed only one volt of noise operating under this condition. It would appear that there is no reason to suspect that a gate tube could be pulsed under these conditions.

In all other respects, the A flip-flop appears to operate satisfactorily in accordance with specifications.

The A Gate Circuit

The A gate tube is used extensively in the instruction frame. Considerable pluggable unit testing data and module test data was taken on this particular circuit. In most respects, data obtained on the gate tube was quite satisfactory! In some circuits it was possible to get as much as 43 volts out with a 40 volt pulse input and 100 ohms output termination. Since this output pulse was larger than the specified amplitude, further investigation was carried on. Several tests were run on the gate circuit driving one unit of load and an output termination of 100 ohms. In none of these tests was it possible to get 40 volts out with 40 in, the average being on the order of 32 to 34 volts. Several gate tube suppressors in the instruction frame are conditioned directly from APCF circuits. It was feared that the high upper level of the APCF on the gate tube suppressor might result in excessive amplitude in the output pulse from the gate circuit. The bias buildup through A flip-flop and PCF stage can reach +18 v at the upper level. Data was taken on a gate tube driven by a flip-flop through an APCF and compared with data obtained on a gate tube driven by a flip-flop through a conventional cathode follower. The results showed that the higher level on the suppressor grid caused a maximum

increased pulse amplitude from the gate circuit of 3 volts.

Several gate circuits were checked for outputs with the suppressor held at -15 volts, and standard 40 volt pulses on the control grid. In no case were more than 2 - 3 volts of noise discernible on the output.

The B Pulse Amplifier

The B Pulse Amplifier was also thoroughly tested under both pluggable unit and frame operation. Test data showed this circuit to perform entirely according to specifications.

Due to lack of confidence in the A pulse amplifier at the time the layout of the instruction frame was prepared, B pulse amplifiers are used in all pulse amplifier applications in the frame. This means that in many circuits, B pulse amplifiers are driving lighter loads than they were designed for. In cases where the B pulse amplifier is lightly loaded, the intention is to terminate the output of the B pulse amplifier with a low value to prevent exceeding unity gain at a 40 volt pulse input. Recently the point was raised, that by so doing one might shift the gain curve of the B pulse amplifier enough to prevent getting unity gain with a 20 volt input pulse. Test data was run on a B pulse amplifier driving a single A gate tube unit of load. The B pulse amplifier was operated first at 200 KC driving the single load unit. Forty volts were applied to the input of the B pulse amplifier and a sampling of terminating resistors indicated that 40 ohms would give 40 volts out at this input. Readings were taken at 30 volts and 20 volts input and the 40 ohms output termination. With 30 and 20 volts in, 35 and 22 out were obtained, respectively. The same sampling of readings was then taken at both ~~one~~ 1 mc and 2 mc,

40, 30, and 20 volts in gave 38, 33 and 21 volts out, respectively. The sampling of data taken would seem to indicate that the B pulse amplifier is only slightly frequency sensitive, and that unity gain is not lost at the lower amplitude pulse, with the output terminated in a sufficiently low value to prevent more than unity gain at the higher amplitudes. The circuit should be satisfactory for driving a single unit of load. Of course, one would recommend that an A pulse amplifier be used for such an application.

Pulsed "OR" Circuits

Pulsed "or" circuits are used extensively in the instruction control frame. In all applications they are used directly at the inputs of A flip-flops or B pulse amplifiers and are located next to the unit of load driven by them. Data taken on pulsed "or's" during pluggable unit testing indicate that the average drop in the pulse amplitude across a diode would be 2 - 3 volts. It was noted that the diode can widen the pulse which posses through it by as much as 0.04 microseconds. In other words a 0.1 microsecond pulse applied to the input to a pulsed "or" could become a 0.14 microsecond pulse on the output. When this output of the pulsed "or" passed through the B pulse amplifier, it was driving, it was again narrowed to a 0.1 microsecond pulse, presumably by the B pulse amplifier transformer. At any rate, the combined "or" and B pulse amplifier circuit gives a pulse output well within specifications.

Investigation of the spreading of the pulse through the "or" diode indicated that excessive open wire on the pluggable unit tester contributed no small amount to the pulse widening; but was not the full story.

The "yankdown" circuit at the output of the pulsed "or" circuit fell under
"yank-down"

suspicion. This consists of a series choke, resistor combination to aid the recovery of the output pulse. It was decided to experimentally change these values and note the effect on the output pulse. Trial and error showed that a decrease of the resistor value or an increase in the inductance of the "yank-down" circuit would give a pulse width from the "or" circuit which was within specifications. The simplest change would be to decrease the resistance to an optimum value, which would probably be about half of its present value. Since the pulse spreading caused no particular problems in the instruction frame, it was decided that no component changes would be made in existing circuits at the present time.

Register Driver Model A

The A register driver is used to drive many instruction pulse lines to gate circuits and to clear flip-flops in the instruction frame. Pluggable unit test data were taken on the circuit, which exists in two pluggable unit types. In addition, the circuit was used to drive pulses into the gate tubes of the time pulse distributor in module C, during testing. No particular difficulty was encountered, and testing data shows the circuit to be satisfactory. In one instance, it was noted that the output pulse of an ARD driving 16 gate tubes was not quite recovering. This was an isolated case and no explanation has yet been uncovered.

Register Driver Model B

This circuit is used to complement flop-flops and drive instruction pulses, in one instance at 2 mc. The BRD is always driven by a BPA. In all

applications, the combination of the BPA and BRD must be considered a package circuit. This means that the circuit is to be checked by measuring the input to the BPA and the output of the BRD. This was not known by the persons doing the pluggable unit testing in the instruction frame, and as a result unsatisfactory data was obtained on the circuit. The BRD was used to complement 16 flip-flops in module C. Operation of the circuit in the module testing was unsatisfactory. Part of the difficulty was due to the master oscillator circuit located in module C. This circuit was puttingoout an undesirably low output pulse to drive the BPA section of the BRD package. Operation was switched to a Burroughs unit test oscillator. Data was taken with 20, 30 and 40 volt pulse inputs to the BPA's driving the BRD's. Outputs from the BRD's were satisfactory at a P. R. F. of 200 KC, but outputs were too low at 2 mc. Experimentation indicated that changing the component values of the terminating network at the secondary of the BRD input transformer improved the PRF response of the circuit considerably. See Table 1.

Table 1

P. R. F.	Input to BPA	Output of BRD	Terminating Network	Load on BRD
200 KC	20	25	L=33 uh, R=560Ω	33 ohms
2 MC	20	16	L=33 uh, R=560Ω	33 ohms
200 KC	20	28	L=33 uh, R=100Ω or L=8.2 uh, R=560Ω	33 ohms
2 MC	20	25	L=33 uh, R=100Ω or L=8.2 uh, R=560Ω	33 ohms

"5965" Cathode Follower

Three types of conventional cathode follower circuits are used in the instruction frame. These are BCF, CCF, ~~B, G,~~ and F CF. The BCF is used exclusively to drive the suppressor grids of gate tubes. Test data ~~was~~ were taken using a decade precision capacitor to simulate wiring and gate tube input capacitance loads. ~~AT~~ At best, these capacitances could only be estimated. However, in all cases it is felt that the simulated loads were on the pessimistic side. All BCF circuits were able to drive the specified loads assigned [redacted] in the proper switching time. A flip-flop output to switch the CF's was obtained from a test flip-flop. Further tests were run on the actual conditioning of gate tube suppressor grids by BCF's. In one instance, a gate tube suppressor was conditioned by one BCF triode while the gate was being pulsed. In another instance, two gate tubes being pulsed simultaneously were conditioned by two BCF triodes in paralled. Both tests were successful, but a unique effect was noted on the output of the BCF's. A positive spike appeared on the trailing edge of the upper level of the BCF output when driving a gate with the control grid of the gate being pulsed. When only one suppressor was being driven by one triode, the magnitude of the positive spike was only on the order of three volts. However, in the case of two parallel triodes, driving two suppressor grids and the two control grids pulsed simultaneously, the spike approached 10 voltsiin magnitude. An experiment was conducted, and it was fairly well determined that this effect was due to feedblock, from the plate to suppressor grid in the gate circuit, of current to the cathode

follower due to interelectrode capacitive coupling. This effect was not noted on the input level of the B CF. The general consensus of opinion seemed to establish that this feedback could cause no forseeable difficulties in circuit applications.

All diode circuit driving cathode followers were tested with Thevinin equivalent diode loads and estimated capacitance loads. Carbon resistors were used to simulate the equivalent diode circuit resistance with "and" and "or" current being supplied by a D-C power supply.

In general, F CF's were used to drive diode "or" circuits in the instruction matrix. The worst combination of "or" current and capacitance driven by each F CF was simulated and data taken. All F CF circuits were able to drive their specified load in the proper switching time.

In a few applications C CF's were used to drive diode "and" circuits in the frame, but all matrices are now driven by A PCF's. The few C CF's tested were loaded with simulated diode "and" current and capacitance loads. It did not seem that the cathode circuits of the cathode followers were accepting as much "and" current as design criteria would lead one to believe and still fall in the proper time. Fortunately, the circuits used were sufficiently over-designed to allow circuit specifications to be met. No reason for the poorer than expected fall time of the C CF has yet been established. It is known that some "hot" 5965's have been placed in the prototype pluggable units used in testing. It may be possible that these tubes are being used in C CF circuits and as a result are not being driven far enough into the cutoff region, allowing

too much tube current to flow into the cathode resistor. This could reduce the "and" current which could be accepted. Poor cutoff characteristics in the "5965" triodes could produce the same effect.

The "5965" cathode follower in test was a very stable circuit. The +150 volts marginal checking could always be lowered to +50 volts or less before any effect was noted on CF output. Below 50 volts the circuit had difficulty in reaching the +10 volt upper level.

A large number of -30 volt protector diodes have failed during circuit operation. The exact cause has not been definitely established, but there are theories which seem to merit mentioning.

One possibility, which will be mentioned in more detail under components, is that some undetected low back resistance diodes are in the pluggable units.

The upper limit on the steady-state forward current that should be passed through a "y" diode is 16 ma. At present, when several cathode followers models are paralleled, only one diode is used to clamp the output to -30 v. This diode may be required to pass from 20 -30 ma to clamp to -30 volts depending on the model and number of cathode followers in parallel. There is some question as to how long a "protector" diode of this sort would be required to pass the 20 - 30 ma. If no case occurs where a diode is required to clamp for more than one second, then the present design is satisfactory since a "y" diode is rated to pass 100 ma for a second or less. Under present test conditions, the +150 v was turned off inadvertantly in a few instances for several minutes and as a result some protection diodes were found with nearly zero back resistance. ~~It is undesirable to parallel~~ protector

~~diodes with nearly zero back resistance.~~ It is undesirable to parallel protector diodes, since this also parallels the back resistances. This effective lower back resistance would defeat the original purpose, since more current would flow through the lower resistance. This would also increase the load on the driving circuit.

Power Cathode Follower Model A

The A PCF is used primarily in the instruction control as a matrix driver with one microsecond switching time. Test data obtained shows the bias ~~buildup~~ build-up in the upper level of this circuit to be higher than anticipated. A typical value would be +18 out for +12 in. This undesirable in at least two respects.

When the A PCF output is at +18 and drives an "and" circuit with at least one input at -30 v, there will be approximately 48 volts across the "down" diode.

When the A PCF drives an "and " circuit whose output is caught at +10 volts there will be a delay, which has been measured at about .05 microseconds, between the time the output of the A PCF starts to fall and the time the diode "and" circuit starts to fall. This is due to the fact that the output of the "and" circuit will not begin to fall until its input reaches +10. This delay would accumulate where more than one level of PCF's is used in tandem with "and" circuits. In the instruction matrix a time allowance of .05 microseconds had been made for such delay. However, two levels of A PCF's are used in tandem here making it possible to lose a total of 0.1 microsecond in delay from this source. It is believed

that the circuits are sufficiently overdesigned to compensate for this unexpected delay, and that it will not create any timing problems in these applications.

Due to a lack of information on the A PCF circuit when the instruction frame logic was laid out, two circuit applications whose switching time was 0.5 microseconds had been set up utilizing the A PCF circuit. Testing revealed that the A PCF circuit would not satisfactorily follow a 2 mc switching rate. The output fails to reach its upper and lower level and resembles a sawtooth wave. Modifications will be made in these two cases, and the A PCF will be replaced by a different circuit.

Master Oscillator Model A

A 33 volt pulse is presently being obtained from the cathode circuit of the oscillator tube via a 1:1 transformer. However, the secondary of the transformer is biased at -30 volts and a small additional bias is developed resulting in a pulse whose lower level is at -32 volts. When this pulse is applied to the output BPA's the grid of the BPA's are only brought to positive +1 volts, instead of a minimum of +5 volts. This results in a low output from the BPA's which drive the oscillator pulses to other circuits. An investigation of the circuit is being carried out by the basic circuits group.

A Pulse Generators

An attempt was made to obtain pluggable unit test data on the APG circuit. A square wave generator operating at 20 cps was fed into a relay inverter which switched a relay in its plate circuit. An APG was driven from a pair of normally open contacts on the relay.

However, an attempt to monitor the output of the pulse generator on the test scope failed. The pulse was not sufficiently clear to take any data on it.

The output of the pulse generator was fed into the complement input of a flip-flop, and the blinker neons indicated that the flip-flop complemented properly. This indicates only that the pulse generator was producing a pulse, and not that it was operating within specifications.

Some reasonable test procedure will have to be set up for this circuit; before it is determined whether or not is is satisfactory.

Relay Inverter

A few of these circuits were tested. It was only necessary that they switch a relay. All circuits were approved on this basis. These circuits will draw about 0.5 ma of current from the driving source.

Components

With the exception of tubes, all component failures recorded during the pluggable unit and module testing program were "y" diodes. The high failure rate which was incurred may be the result of a combination of factors, or may be rooted in one of a number of theories which have been suggested. These are probably worth mentioning here.

1. Testing procedures may not be ~~comphrensive~~ comprehensive enough.
2. Shelf life from the time of testing until the actual placement in pluggable units may cause deterioration.
3. ~~Slip~~ DIP soldering of cards may cause excessive heating of the diodes and resulting deterioration.

4. Circuit operation combined with poor power regulation and shutdown may have placed undue strain on the diodes, during the testing period.

In all fairness, it must be noted that all these failures occurred in the first few prototype models. In these first few units one would expect inexperience in testing and dip soldering as well as in actual circuit testing procedures. The factors which contributed to the diode failures may not be present by this time. However, sufficient low back resistance and high forward resistance diodes were detected in these first few models to cause considerable alarm concerning this component.

It is difficult to check diodes properly once they are on the cards in the pluggable unit. At best, only a rough check can be made. By this time, procedures probably have been set up to test diodes on the card between the time that cards are dipped and placed in the pluggable units.

Tubes

A few tube failures occurred during the testing program. In some cases uncertainty exists as to the cause, but it is believed that most failures were a result of improper testing procedures on the part of those testing the pluggable units. Two cases can be traced to defective tubes, for certain. In one 5965, the getter was shorting out the [redacted] control grids. One 1782 A was found to be O.K. when checked D-C wise, but failed pulsewise.

The 1782 A tube fits very tightly in its socket and must be rocked when removed. In one case, the tube base was cracked as a result of such removal. On

six other tubes, keyways were cracked and broken off as a result of removing them from the socket. This would indicate that the tube bases are too fragile, or that handling techniques were not gentle enough in these instances.

Wiring

Most of the trouble shooting done during the testing period of pluggable units and the module led ultimately to wiring errors. This was to be expected on the prototype pluggable units and module, since many of the personnel concerned were inexperienced and techniques were still undergoing refinement. This was borne out by the noticeable decrease in wiring errors in later units.

The types of wire used in the pluggable units and module seemed satisfactory with the exception of the microdot wire now in prototype module C. The insulation of this wire was found to have low abrasive resistance and improved microdot will appear in forthcoming modules.

In an isolated instance filaments in module C were found to be shorted to chassis. Investigation showed that this was occurring in one of the pluggable units. The unit was removed and the filament wire checked. When the filament wire was moved from touching the pluggable unit chassis, the short disappeared. However, no visible break could be found in the insulation of the wire.

The wiring of module C illustrated that using microdot wire between points 8 to 12 inches apart seems unnecessary. In these cases, nearly as much yellow wire is used in tying in the ends of the coax as would be used in jumpering the points together with open wire.

In module C wiring, it was noted that in terminating signal wires the wire is always sent to the terminating resistor on the board before being sent to the last unit of load. In many places, wiring could be shortened by 3 to 4 inches and made somewhat neater if the signal pin of the last load unit were connected and then jumpered to the terminating resistor.

Mechanical Features

By far, the larger portion of mechanical failures occurred because of failures of the male plugs in pluggable unit bases to ~~made~~ make proper contact with the opposite member in pluggable unit testers and in module C. In many instances, pluggable units which made contact in one female base would not make contact in another. This would evidently be due to a buildup of tolerances on the part of both male and female. These failures occurred in the prototype pluggable unit models. Since then the pins have been redesigned, and it is hoped that failure from this cause will be eliminated. No data is yet available on the redesigned bases.

In some instances pluggable units bases did not float properly in the pluggable unit frame. As far as is known, this has occurred in only the first few prototype units, whose frames may not be entirely within specifications. It is felt that this difficulty should be eliminated in forthcoming units.

In prototype module C, pluggable units could not be put into the module without considerable force being applied. In some cases where units were forced in, wires were torn off card edges in the pluggable units. It became necessary to remove the "ladders" from the module in order to facilitate entrance of the unit

into the module. Module C has been operated throughout without these "ladders," whose main purpose is to hold the pluggable units firmly in position. This particular difficulty has been under investigation by the mechanical design group.

On the filament busses in module C it was noted that the male connector of the wires leading to the buss seems to fall out too easily. The male connector on the end of the lead in wire has no room for expansion and as a result is being compressed to some extent. Perhaps this difficulty could be overcome by use of the edge connector principle where expansion is provided for.

The stamping of pluggable unit type numbers on each unit and of pluggable unit locations on the back of each module would facilitate testing and help eliminate the possibility of placing a wrong type of unit in the wrong module location. No permanent identification procedure was used on module C or its prototype units.

During testing it was found that the handles on the pluggable unit camshafts work loose and fall off quite easily. This is due to failure of the set screw to remain tight against the flat part of the shaft.

It is felt that the soldering lugs used on the card assemblies in the prototype units are to fragile. During troubleshooting, several lugs were broken off by only a small amount of bending. Once a lug is broken off it cannot be replaced with the card still in the pluggable unit. The card must be removed from the units and an attempt made to remove the remaining portion of the lug from the card. This can only be accomplished with great difficulty, if at all. Quite often the result is a broken card.

The instruction control group invites comments, corrections and questions concerning any of the material found in this report.

H. G. Hickey

ISSUE 1

INSTRUCTION CONTROL DAILY LOG

June 10, 1954

1. The -30 breaker on module G and the +150 marginal check breaker for G, H were tripping every five minutes. An ammeter was placed in series with the +150 (3 amp) breaker and read only 1 amp. The ammeter did not climb just before the breaker tripped, so we assumed that the breaker was defective and it was replaced. The -30 (3 amp) breaker still kept tripping. An ammeter in series with the breaker read 1.3 amps and the reading started to climb just before the breaker tripped. The breaker was assumed to be all right and the trouble was traced to PU-GD. The plates on 5965 (tube 1 and GD) were glowing red. The unit was pulled and the plate decoupling resistors were sliced in half although they still must have been making contact. The excessive current was traced to a -30 clamping diode in the cathode with only 3K back resistance.
2. While tracking down the trouble in (1) above, it was found that the B CF's in P. U. type 6013 had -30 clamping diodes. Since these CF's drive only gates, clamping diodes are not needed. We checked the prototype and saw that the -30 lead had been clipped on that unit, but the engineering change did not get through to the production units. The engineering change has now been sent in.
3. Grid resistors in register drivers which work at 2 mcps are being changed from 10 ohms 1/2 w to 1000 ohms 1/2 w to limit grid current.
4. F J (3rd group) and F S (1st group) filaments not lighted. Tapered pins do not seem to be making contact with the filament bus.

5. PU - ET will not plug in.

6. PU - GG Tube 6 looked gassy and was replaced.

7. The TPD was changed from an 8 microsecond to a 6 microsecond ring. Timing is very tight in many instances and impossible in others. Part of memory selection will have to be done in the program element instead of the instruction control frame. Cable delays and transformer delays may dictate other changes in the logical design as well as in a few pluggable unit types.

8. Time level zero and time level one are being interchanged. The "Break" flip-flop is cleared on TP-11 supposedly. However, because of delays, etc., the pulse does not get to the flip-flop until much after TP-11. Therefore, the "Break" flip-flop has not settled down by zero time. Now if you are in a Pause and Break condition and then change to a Pause and No Break, you do not want TP-0 to get through and start up the ring. However, as mentioned above, the Break flip-flop does not settle down by zero time. So the machine will be stopped in the future in TP-1 by which time the Break flip-flop will definately have settled down.

A. H.

ISSUE 2

INSTRUCTION CONTROL DAILY LOG

June 11, 1954

1. With all "1" being read into the operation register the +90 line has the following noise:

   J. Beesley suggests that all future PCF's have their +90 decoupled and that we just hang a 1 uf capacitor on the line.

2. PU - CD tubes 1 and 2 have 1 K resistors in the grid circuit. These are ARD's hit at 2 mcps. The output voltage was the same with the 1 K resistor as with the previous 10 ohm resistor. However, the grid current was cut from 14 ma to 5 ma.

3. PU - FC tubes 4 and 5 have 470 ohm resistors in the grid. This is a BRD hit at 2 mcps. The input transformer has a 100 ohm resistor on the primary to cut down the drive since the output of the BRD is lightly loaded. Without the 100 ohm input terminating resistor and with the 10 ohm grid resistor the grid current per tube was 6.5 ma. With the 100 ohm resistor and 10 ohm resistor the grid current per tube was 3.5 ma. With the 100 ohm resistor and 470 ohm resistor the grid current per tube was 2.8 ma.

4. Tubes 7, 8 and 9 in PU - HG were not lighted. The filament pins on the pluggable unit looked burnt and scorched. There was no apparent reason for this. After the pins were cleaned, the filaments lighted up.

5. PU - ET could be plugged in after the terminal board mounting bracket was moved.

6. PU - CF tube 9 was not lighted at 2 p.m. After jiggling the tube, the filaments lighted.
7. PU - CX tube 9 (same as 6)
8. ON FJ (3rd group) and F S (1st group) of tubes the wire inside the tapered pin is not making contact with the taper pin. Yesterday it was reported erroneously that the pins were not making contact with the filament bus.
9. PU - DL card 9, the +10 catcher diode was found open and replaced.
10. PU - DL card 9, the signal diode H2 had 1.5 K back resistance and was replaced.
11. PU - CD tube 1 was not lighted at 5 p.m. See 6.

A. H.

ISSUE 3

INSTRUCTION CONTROL DAILY LOG

June 14, 1954

1. One per cent resistors in the power cathode follower circuits have been opening up and one has changed value. In particular, the 47 K and 51 K resistors in parallel in the plate circuit of the difference amplifier have been opening up. The 68 K resistor which is also part of this parallel group has not gone bad. A 300 K resistor in one unit has changed value to 1 megacycle. The three resistors in parallel should be 18 K. Here are readings that were taken yesterday on some pluggable units that were bad. The last three were fresh from stock and measured just to make sure that defective components were not getting into the pluggable units.

6010 - type	# X226	Card 4 - 18 K	Card 10 - 26 K
	X227	Card 4 - 21 K	Card 10 - 19 K
		also Card 10	300 K Resistor was 1 meg.
	X 220	Card 10 - 68 K	Card 4 - 18 K
	X 206	Card 10 - 30 K	Card 10 - 30 K
6017 - type	X 225	Card 1 - 68 K	Card 7 - 18 K
		Card 8 - 18 K	Card 14 - 18 K
	X 224	Card 1 - 66 K	Card 7 - 62 K
		Card 8 - 66 K	Card 14 - 62 K
	X 229	Card 1 - 18 K	Card 7 - 25 K
		Card 8 - 28 K	Card 14 - 52 K

Fresh From Stock

6010 - type	X 221	Card 4 - 18K	Card 10 - 18K'
	X 228	Card 4 - 18K	Card 10 - 18K
	X 231	Card 4 - 18K	Card 10 - 18K

We have at times lost just the +150, the +90 or the -300 supply. Tests and calculations indicate that loss of any of these supplies should not cause resistors to fail. A few times we have run the machine without air-conditioning and then turned it on suddenly. There is some chance that this might be causing the damage. The actual cause has not been verified yet.

2. Yesterday in item 10 it was mentioned that a signal diode was replaced. The symptoms leading to its discovery should be mentioned as they are of interest. A number was set into the step counter to indicate the number of desired shifts and a shift instruction was carried out over and over. The add "one" pulses to the step counter were observed to see if the order was being performed properly. If we set 8 in the step counter and watched the scope, we would see 8 "add one" pulses for a second or so, but then we could see a decaying action and only "1" add one pulse would be seen. The trouble was traced to a bad diode. The point being made is that in actual machine operation the shift order would actually have been performed correctly once or more since it took time for the error to occur. Yet if many orders using the step counter were performed in the same program, it is conceivable that eventually errors would have occurred. This may be of interest to diagnostic programmers and maintenance people.

A. H.

ISSUE 4

INSTRUCTION CONTROL DAILY LOG

1. A 6010 pluggable unit that has never worked was finally debugged today after about 12 engineering man hours. The symptoms were: one side of A FF always stuck in the +10 condition; the other side switching from -30 to +10 but returning to -30 before the next pulse came along. The trouble was that pins 2 and 3 (grid - cathode) of the cathode follower in the +10 output side of the flip-flop were soldered together inadvertently.
2. On PU - 6001 X1 a pulse transformer on card 7 (of a gate tube) was bad. The resistance measurements seemed to indicate that nothing should be wrong. The primary measured about 3 ohms, the secondary 1 ohm and secondary to primary are open circuit. When the transformer was replaced the circuit worked. With the original transformer a pulse was developed in the primary, but even with the secondary unsoldered from the card there was no output. The transformer is being sent to the components people as are all other components that seem to be bad.
3. It has been ascertained that leads in tapered pins that have been crimped by hand can be pulled loose without too much trouble. Leads in tapered pins that have been crimped on a machine are impossible to pull loose. Unfortunately, quite a few leads on Instruction Control seem to have been crimped by hand, if not all of them. This is probably why we have been having trouble with them. All future leads are being crimped by machine.

A. H.