R. Best

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

GT-5965

SUBJECT: HIGH-SPEED (5965) FLIP-FLOP

To: Group 62 Engineers and Group 63 Engineers

From: Hal Boyd

Date: February 24, 1953

Abstract: In this E-Note is presented a collection of data taken on the preliminary circuit of a high-speed, high-reliability, 5965 duo-triode flip-flop, that was designed to drive 7AK7 gate tubes. The procedure used in the design of this flip-flop is explained in E-525 entitled "The Normalized Flip-Flop Chart." A circuit schematic of the flip-flop, from which all data was taken, is shown in Figure 1, attached.

1.0 P.R.F. Response Characteristics

The curves shown in Figure 2 were obtained by complementing the flip-flop with a continuous train of 0.1 μsec pulses with various loads on both flip-flop outputs. The lower curves define the transition from the region of either inoperation or frequency division, to the region of absolute operation. The upper curve (45° line at 5 megacycles) defines the transition from the region of operation to the region in which both output levels coincide. In this latter region the flip-flop's memory is destroyed and the flip-flop assumes a third stable state in which counting is not reliable.

For 20-volt triggers with a range from 13 to 30 volts, the flip-flop can drive up to 100 μμf/side (6-7, 7AK7 gate tubes per side) up to a maximum continuous p.r.f. of 4 megacycles.

2.0 Counting Characteristics

Figure 3 was read directly from the output waveforms of the flip-flop while complementing at 1 Kc with 0.1 μsec pulses. 15-volt and 25-volt negative triggers were used for complementing the flip-flop, and the output waveforms were observed with no load and with a load of 100 μμf on each output of the flip-flop. Note that no additional delay would be necessary for use of the flip-flop in counting applications.

3.0 Variation of critical voltages with low I_b tubes

The worst combination of tube sides for the flip-flop tube is with one side of high I_b and the other of low I_b. The most critical voltages are the output levels, E_{o1} and E_{o2}, the flip-flop tube's cathode voltage, E_k, the "on" tube's grid voltage, E_{gon}, and the "off" tube's grid voltage, E_{goff}. The manner in which these voltages vary as one tube side's I_b varies is shown in Figure 4.

The I_b of the tube side in question was varied by its filament voltage. In the experiment, provision was made for switching the tube side from a tube testing circuit to the flip-flop circuit. Hence, at each filament voltage the I_b at 120 volts E_b and $E_c = 0$ was measured, and, at that same filament voltage, the behavior of the tube in the flip-flop was noted and the critical voltages were measured. The results were verified when, later, low I_b 5965's were available.

4.0 Supply Voltage Variations

Nominal Voltage	Limits	% Change	Output Levels
+150	+210	40%	+5 to -25
	0	100%	0 to -48
	-|>300|	100%	+.5 to -50
-150	-125	16.7%	+2.5 to -25
	-100	33.3%	+2.5 to -15

The above data is presented in terms of output voltage levels because failure of the flip-flop was arbitrarily taken as the point at which either output level falls within the range of from 0 to -25 volts; whereas flip-flop failure with respect to gate tubes defines a range of from 0 to -15 volts.

5.0 Resistor and diode tolerances

Tolerances on resistors and diodes were taken one at a time, and the limits were defined by the point at which either output level falls within a range of from 0 to -25 volts. Figure 5 gives the maximum tolerance of each component, all others being held constant and within the tolerances shown on Figure 1.

6.0 Marginal Checking

Various components of the flip-flop were varied one at a time, and marginal checking voltages were determined for a number of values of

each component. The marginal check voltage was inserted in the flip-flop at the spot marked "marginal check voltage" on Figure 1. The marginal checking voltage is centered, or has its base line, at -150 volts, and is taken to be the displacement from -150 volts. The manner in which the marginal checking voltage varies with percentage variations of each component is shown in Figures 6-12 inclusive. The solid curves indicate the picking up of a component on the same side of the flip-flop as the marginal checking voltage; whereas, the dotted curves are for components on the opposite side of the flip-flop.

Drawings:

SA-53718-1
SA-54002
SA-48396-G to
48405-G incl.

Signed H. W. Boyd
Hal Boyd

Approved R. L. Best
R.L. Best, Section Leader

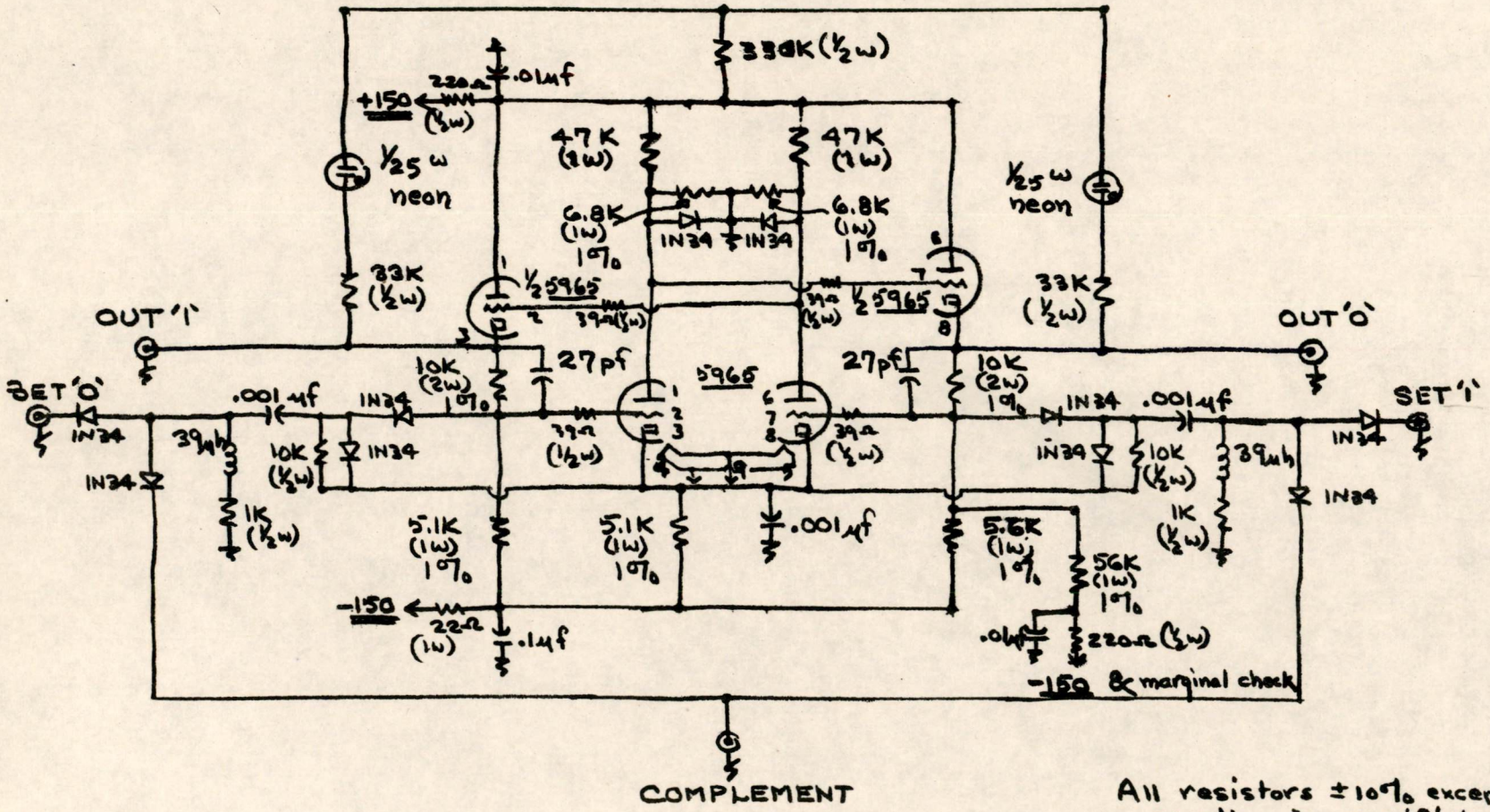
Approved N. H. Taylor
N.H. Taylor, Group Leader

HB/cs

SA-53718-1

4 MEGACYCLE 5965 FLIP-FLOP for GATE TUBE LOADING

20 volt negative 0.1msec trigger, nominal; range: 13-30 volts
Output levels: upper — 0 to +8, lower — -25 to -35
Maximum loading (for 20v triggers at 4mc): 100 pf/side (6-7, 7AK7 GT's)



All resistors ±10% except as otherwise specified

MASSACHUSETTS INSTITUTE OF TECHNOLOGY SERVOMECHANISMS LABORATORY		
DIC NO.	DR. 1-29-53 H W Boyd	CK. R L Best
ENG. 1-29-53 Harold W. Boyd	SA-53718-1	

SA-54002

RESISTOR & DIODE TOLERANCES

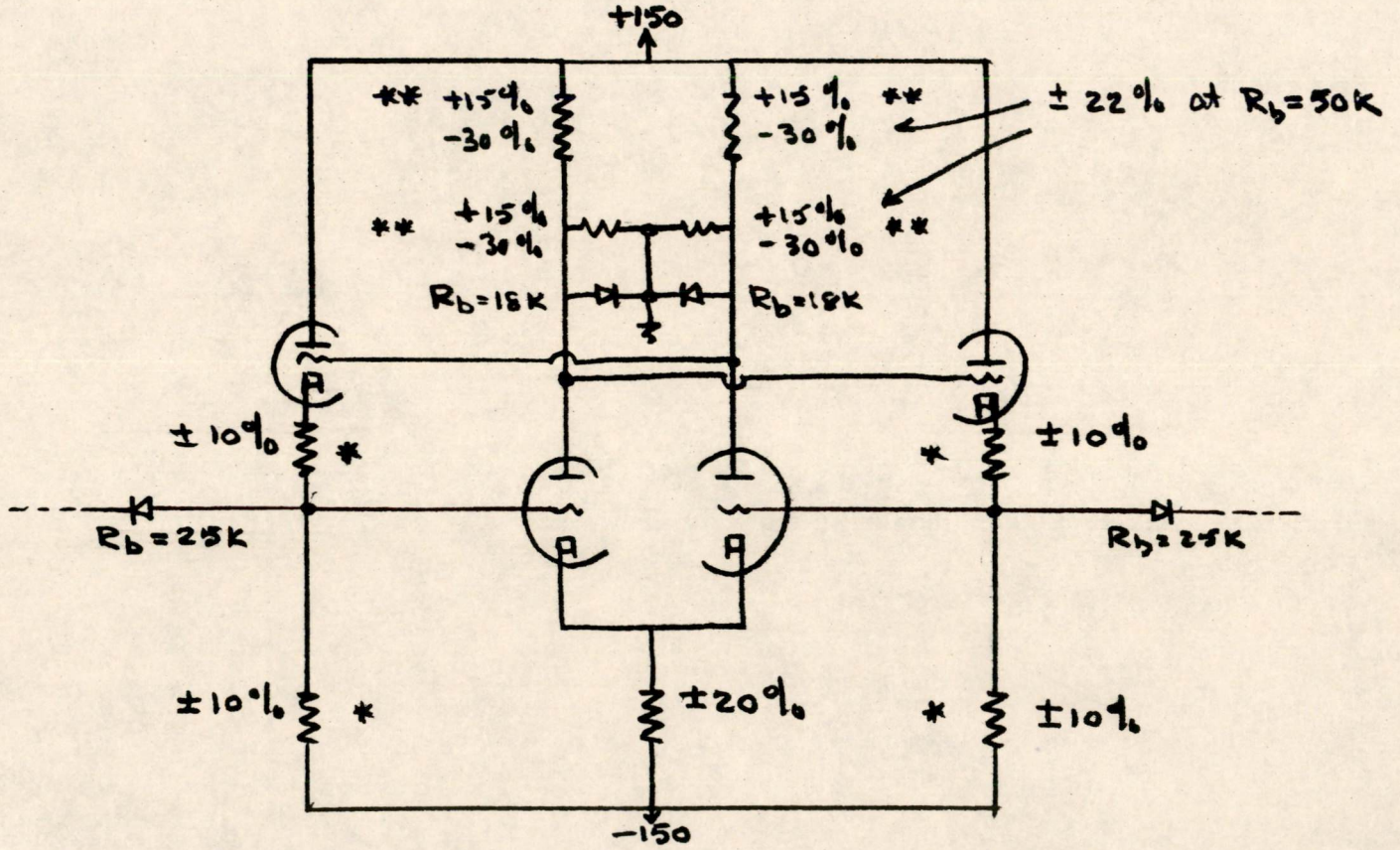


FIGURE 5

FIGURE 5

NOTES: (*) If all four resistors vary in the worst directions, then each can vary 2.5% before failure.

(**) These limits (as are all others) are defined by output levels of 0 to +3, and/or -25 to -35 volts. If -40 volts were taken as one of the limits instead of -35, then the +15% tolerance would be increased to +60%. Also, as the plate-circuit-diode's back resistance decreases, the upper limit increases and the lower limit decreases.

Hal Boyd
SA-54002 20 Feb 53

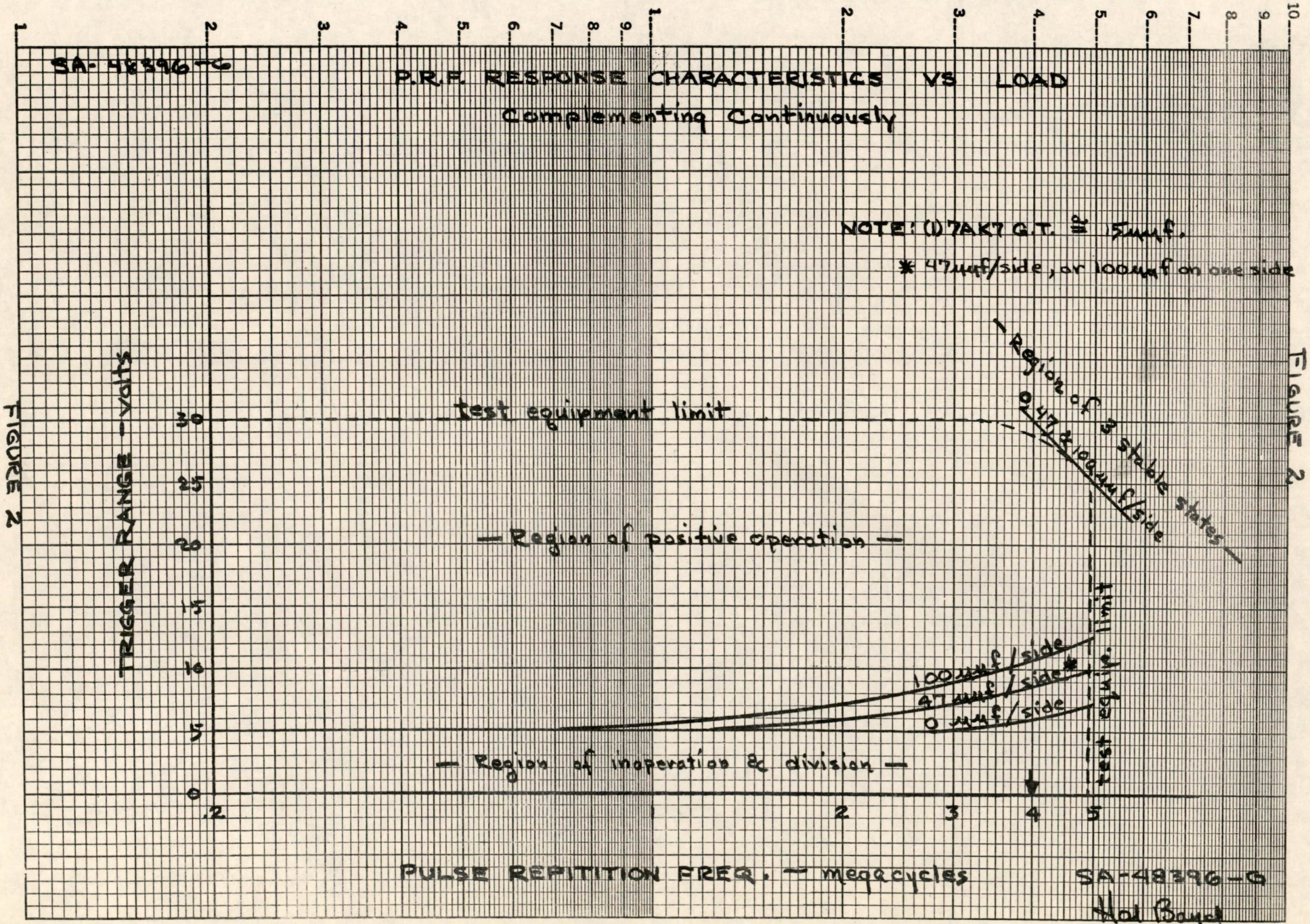


FIGURE 2

FIGURE 2

SA-48397-G

COUNTING CHARACTERISTICS

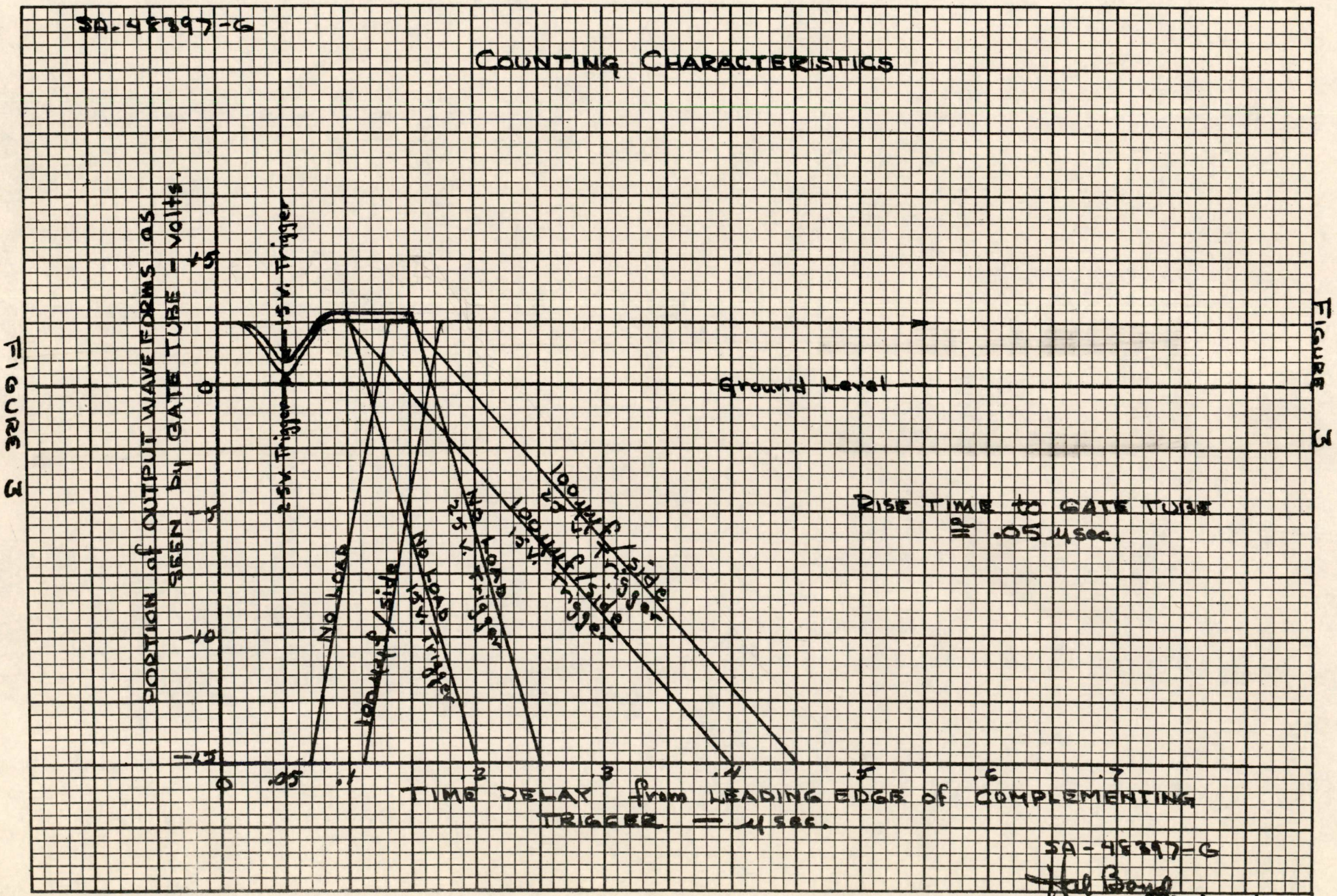


FIGURE 3

FIGURE 3

RISE TIME to GATE TUBE
= .05 μsec.

SA-48397-G

Hal Boyd
24th Feb '53

SA-48398-9

FLIP-FLOP BEHAVIOR with POOR TUBES

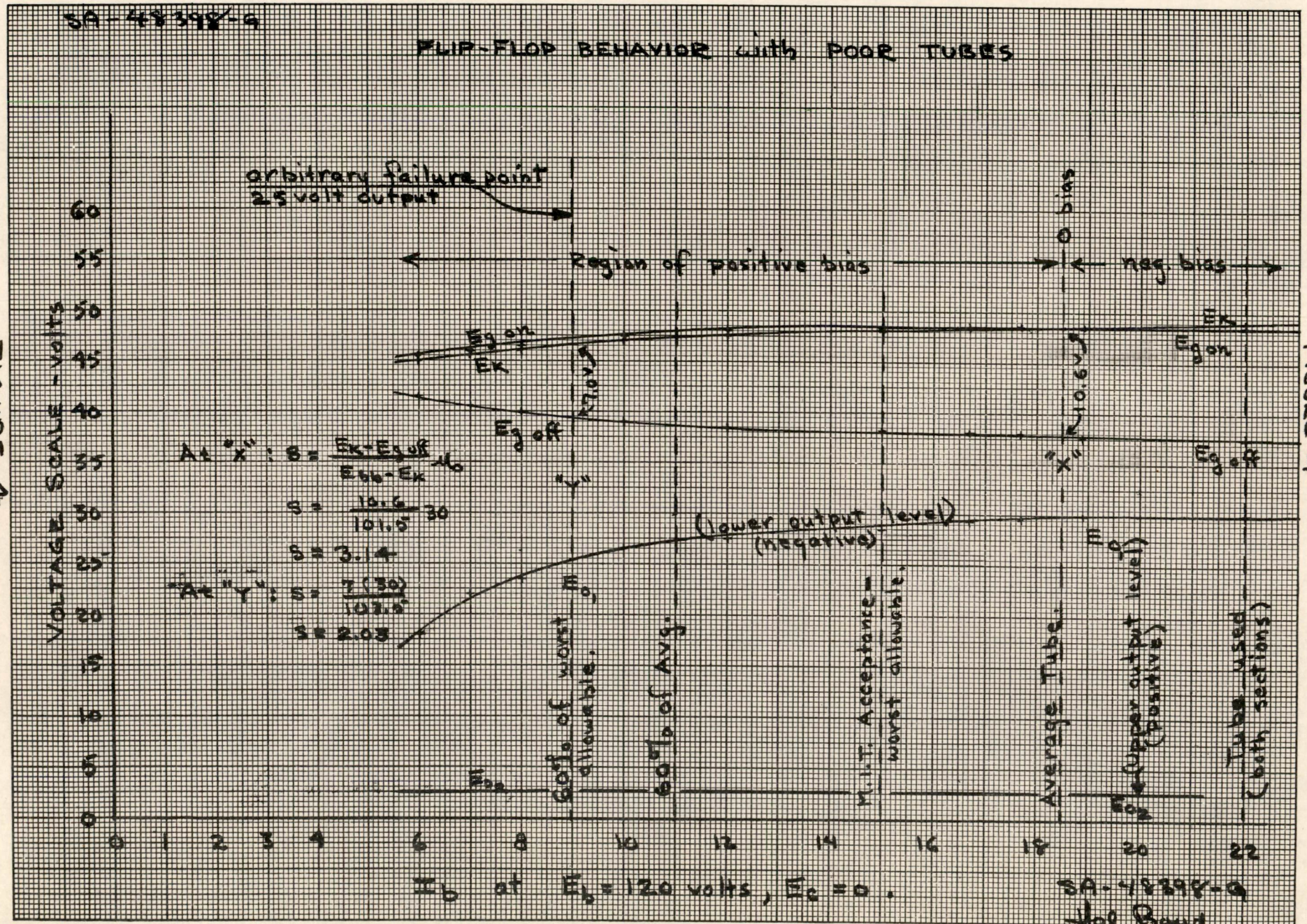


FIGURE 4

FIGURE 4

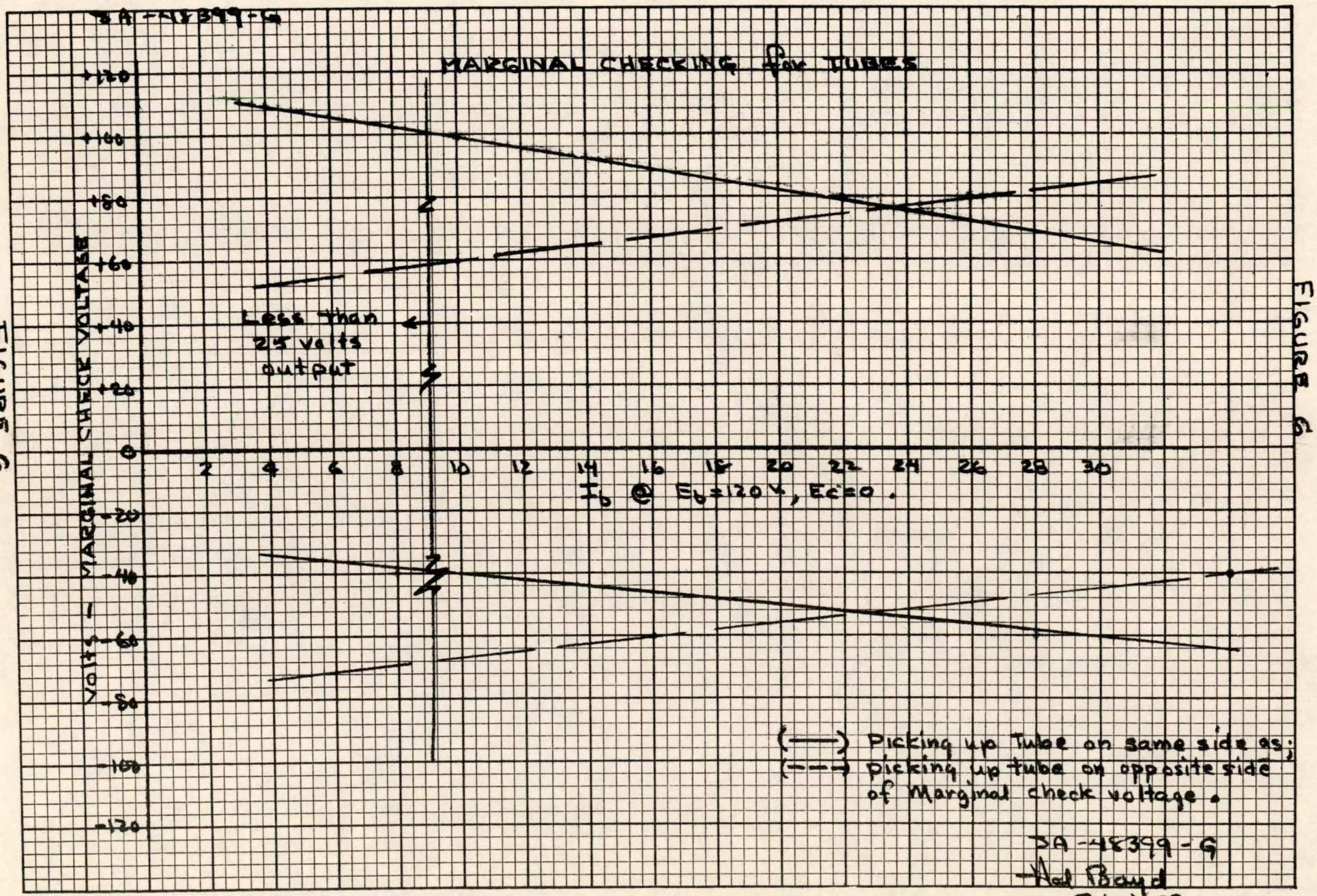


FIGURE 6

FIGURE 6

SA-418400-G

MARGINAL CHECKING THE DIVIDER RESISTORS

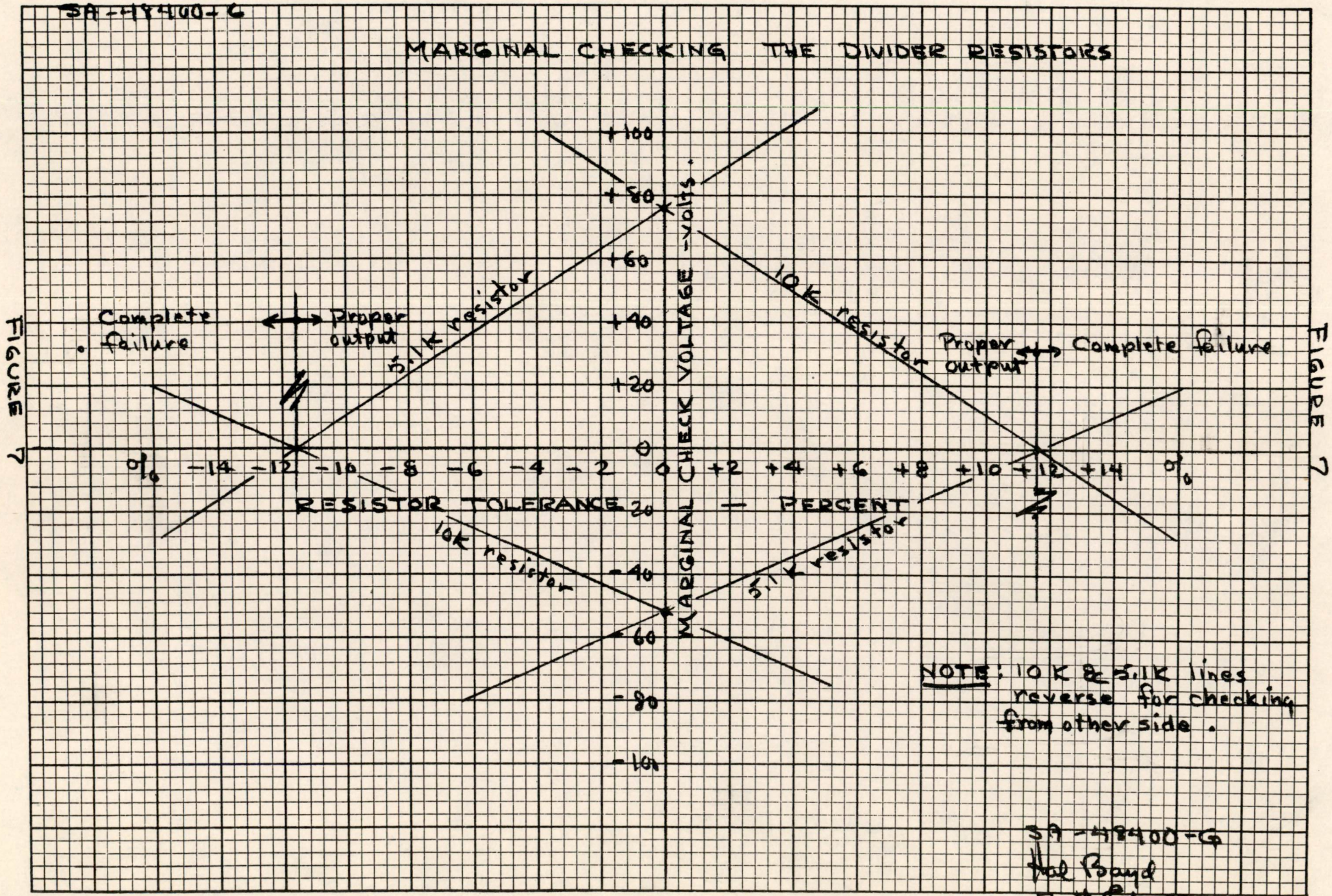


FIGURE 7

FIGURE 7

NOTE: 10K & 5.1K lines reverse for checking from other side.

SA-418400-G
Hal Boyd
20 Feb 53

SA-48401-G

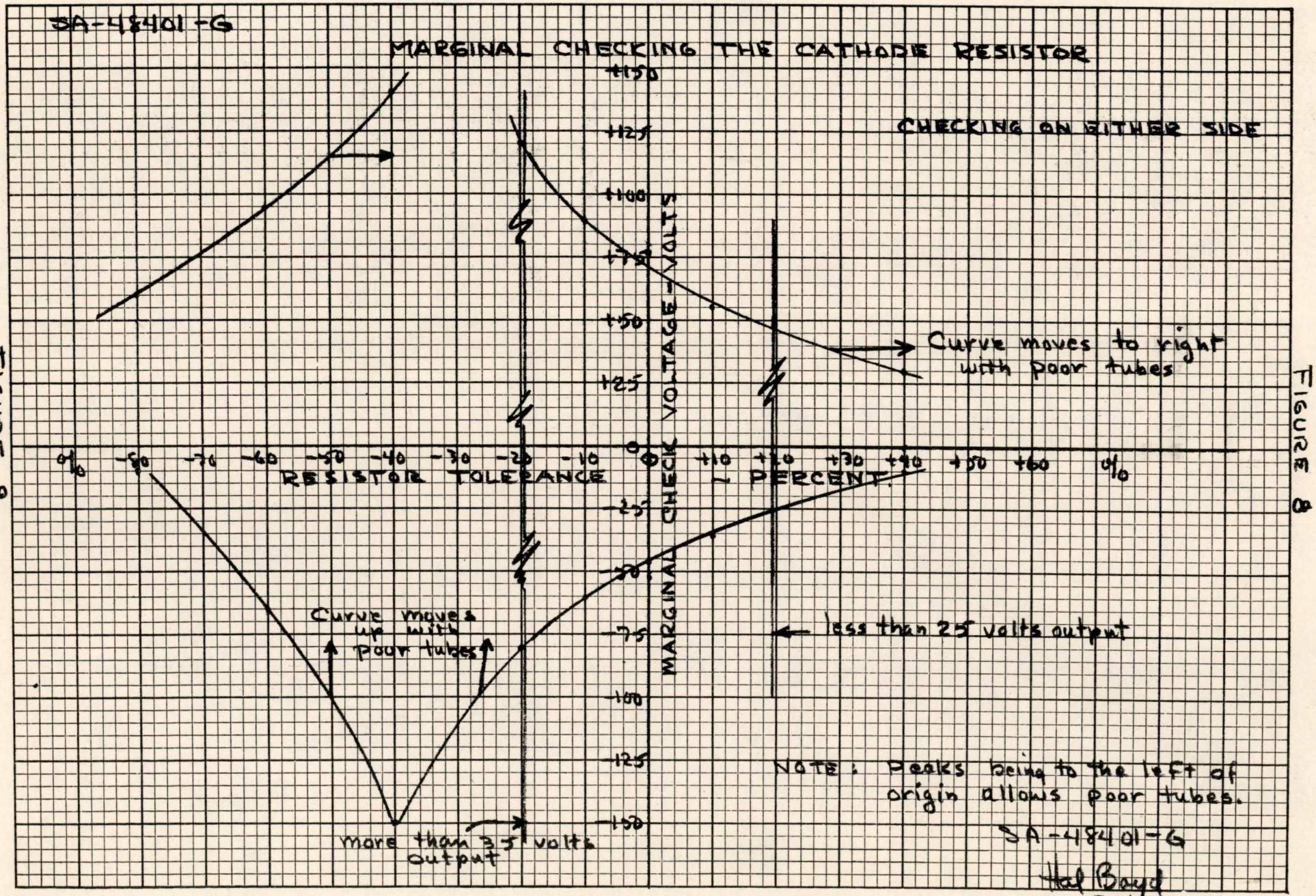


FIGURE 8

FIGURE 8

NOTE: Peaks being to the left of origin allows poor tubes.

SA-48401-G

Hal Boyd

20 Feb. '53

SA-48402-G

MARGINAL CHECKING THE 6.8K PLATE RESISTOR

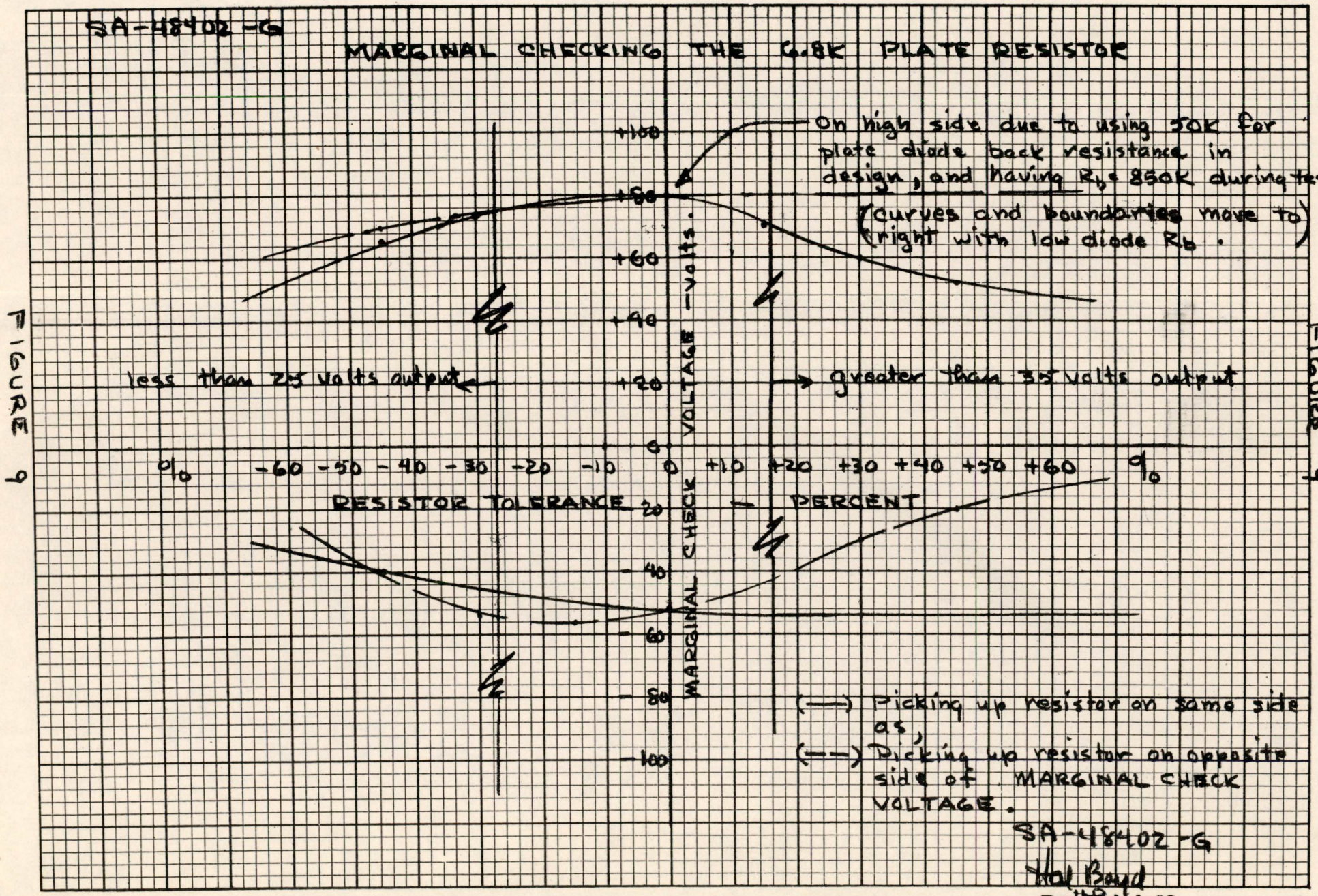


FIGURE 9

FIGURE 9

SA-48402-G

Hal Boyd

20th Feb. '53

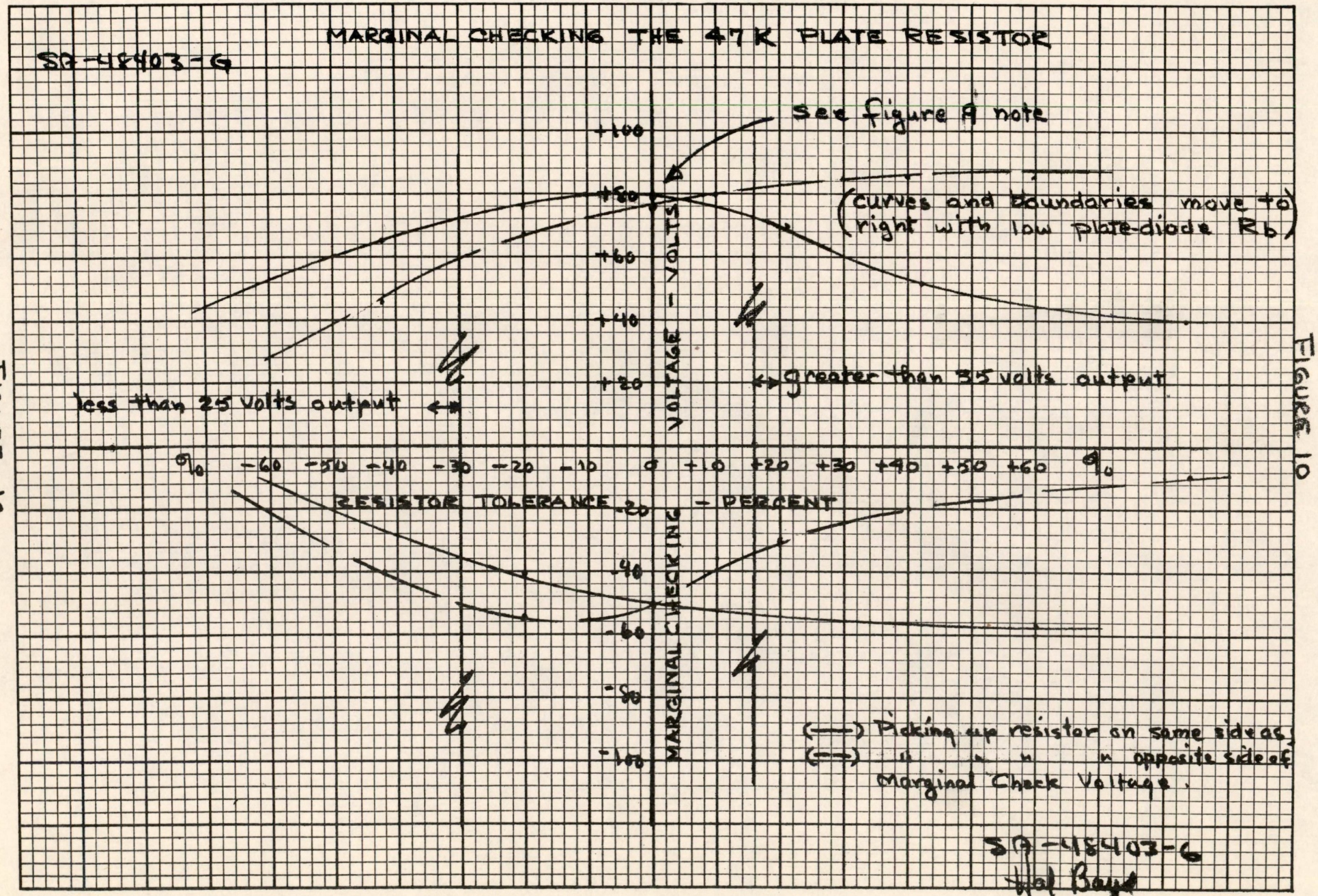


FIGURE 10

FIGURE 10

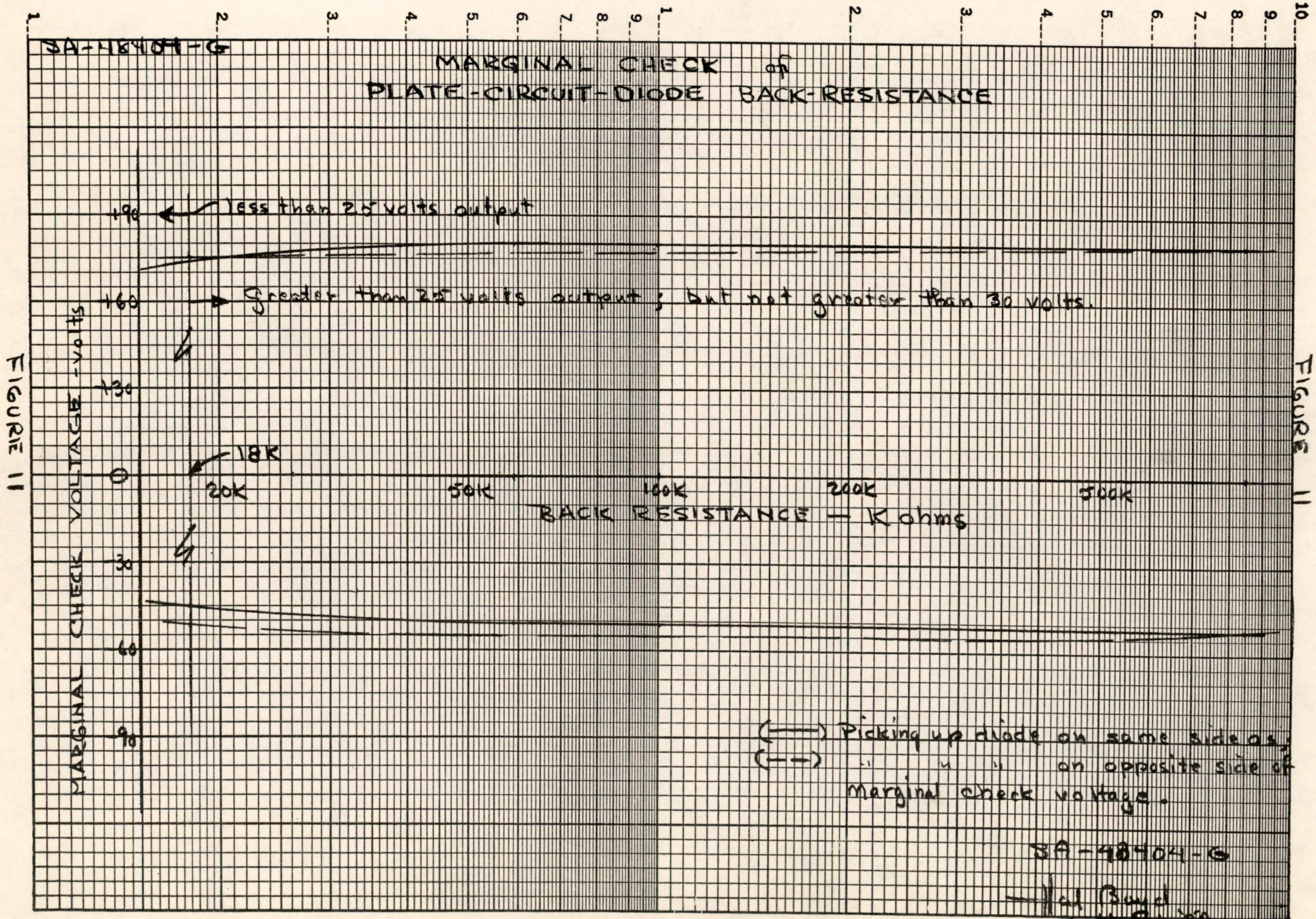


FIGURE 11

FIGURE 11

FIGURE 12

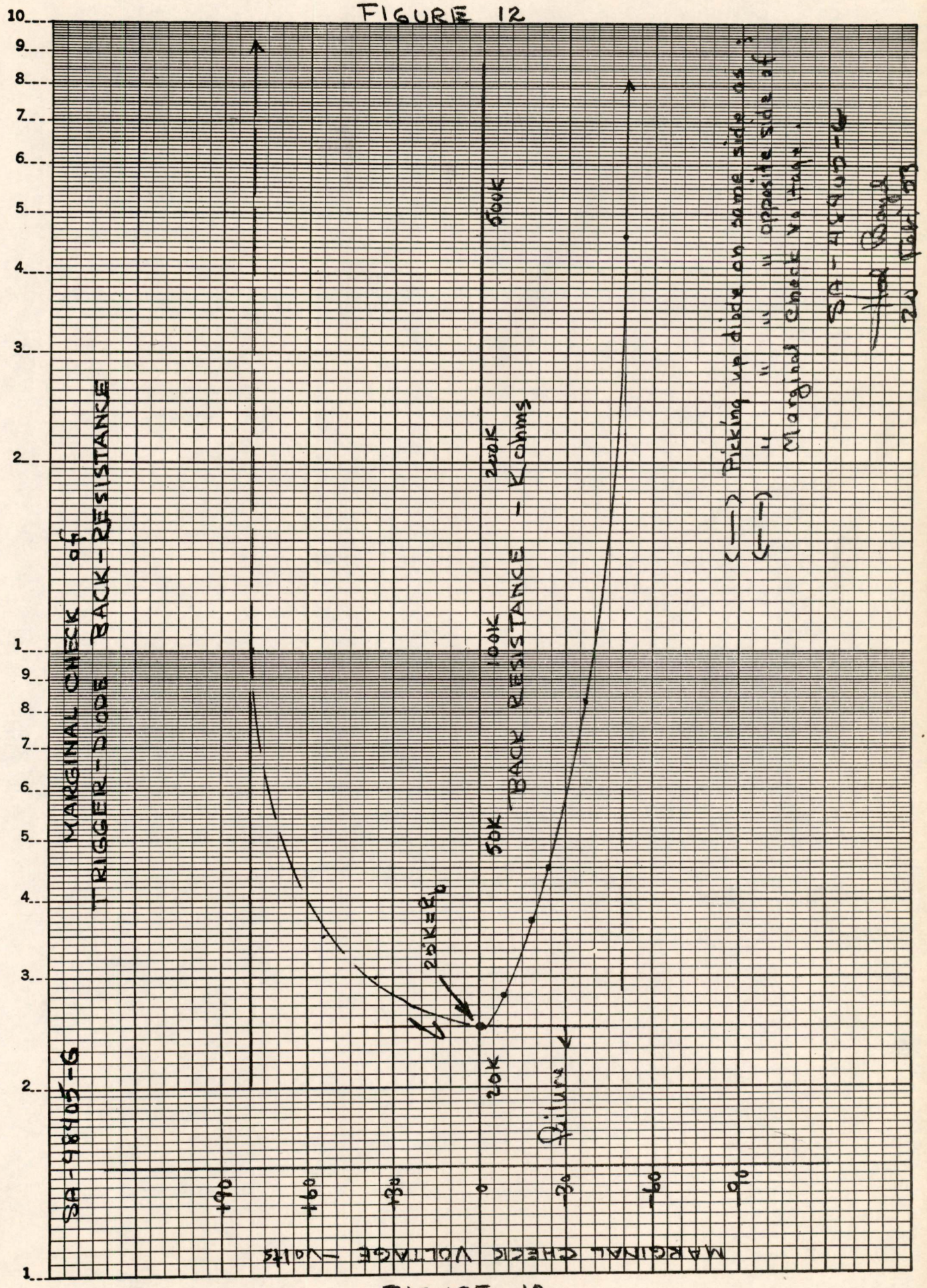


FIGURE 12

K. Olsen

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: HIGH-SPEED (5965) FLIP-FLOP

To: Group 62 Engineers and Group 63 Engineers

From: Hal Boyd

Date: February 24, 1953

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For 20-volt triggers with a range from 13 to 30 volts, the flip-flop can drive up to 100 μμf/side (6-7, 7AK7 gate tubes per side) up to a maximum continuous p.r.f. of 4 megacycles.

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Drawings:

SA-53718-1
SA-54002
SA-48396-G to
48405-G incl.

Signed H. W. Boyd
Hal Boyd

Approved R. L. Best
R.L. Best, Section Leader

Approved N. H. Taylor
N.H. Taylor, Group Leader

HB/cs

SA-53718-1

4 MEGACYCLE 5965 FLIP-FLOP for GATE TUBE LOADING

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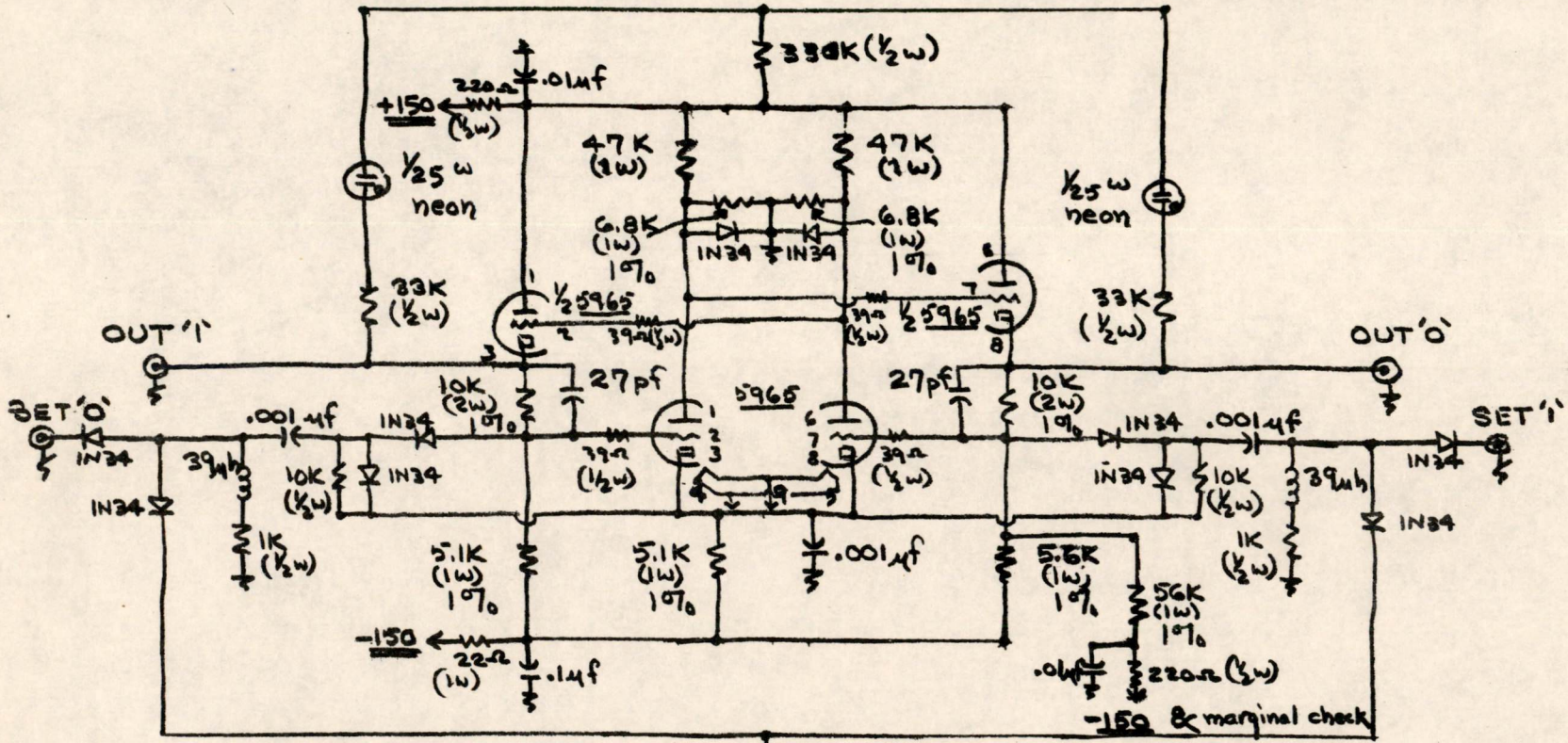
Maximum loading (for 20 v triggers at 4 mc): 100 pf/side (6-7, 7AK7 GT's)



All resistors ±10% except as otherwise specified

MASSACHUSETTS INSTITUTE OF TECHNOLOGY SERVOMECHANISMS LABORATORY		
DIC NO.	DR. 1-29-53 H W Boyd	CK. R L Best
ENG. 1-29-53 Harold W. Boyd	SA-53718-1	

SA-54002

RESISTOR & DIODE TOLERANCES

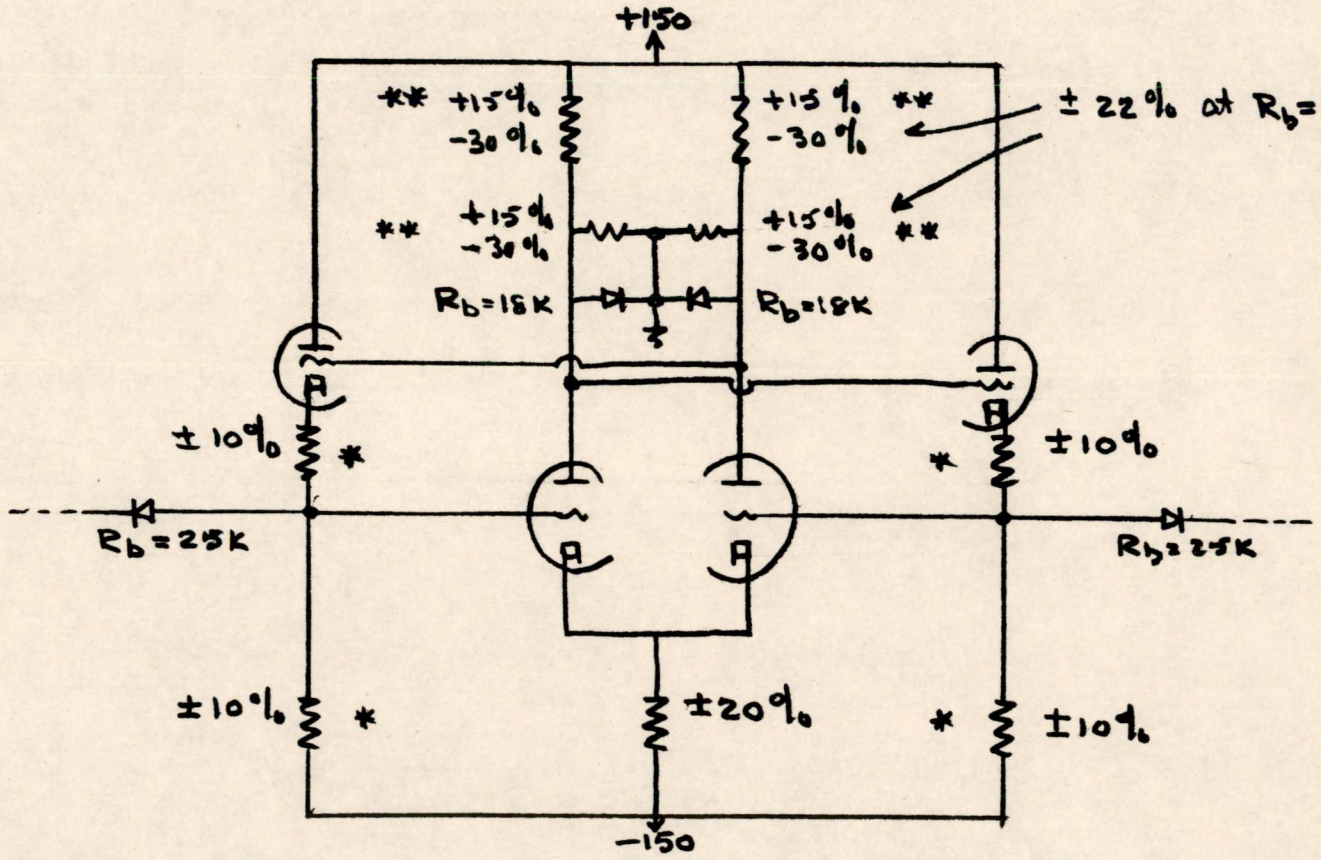


FIGURE 5

FIGURE 5

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Hal Boyd
20 Feb 53

SA-54002

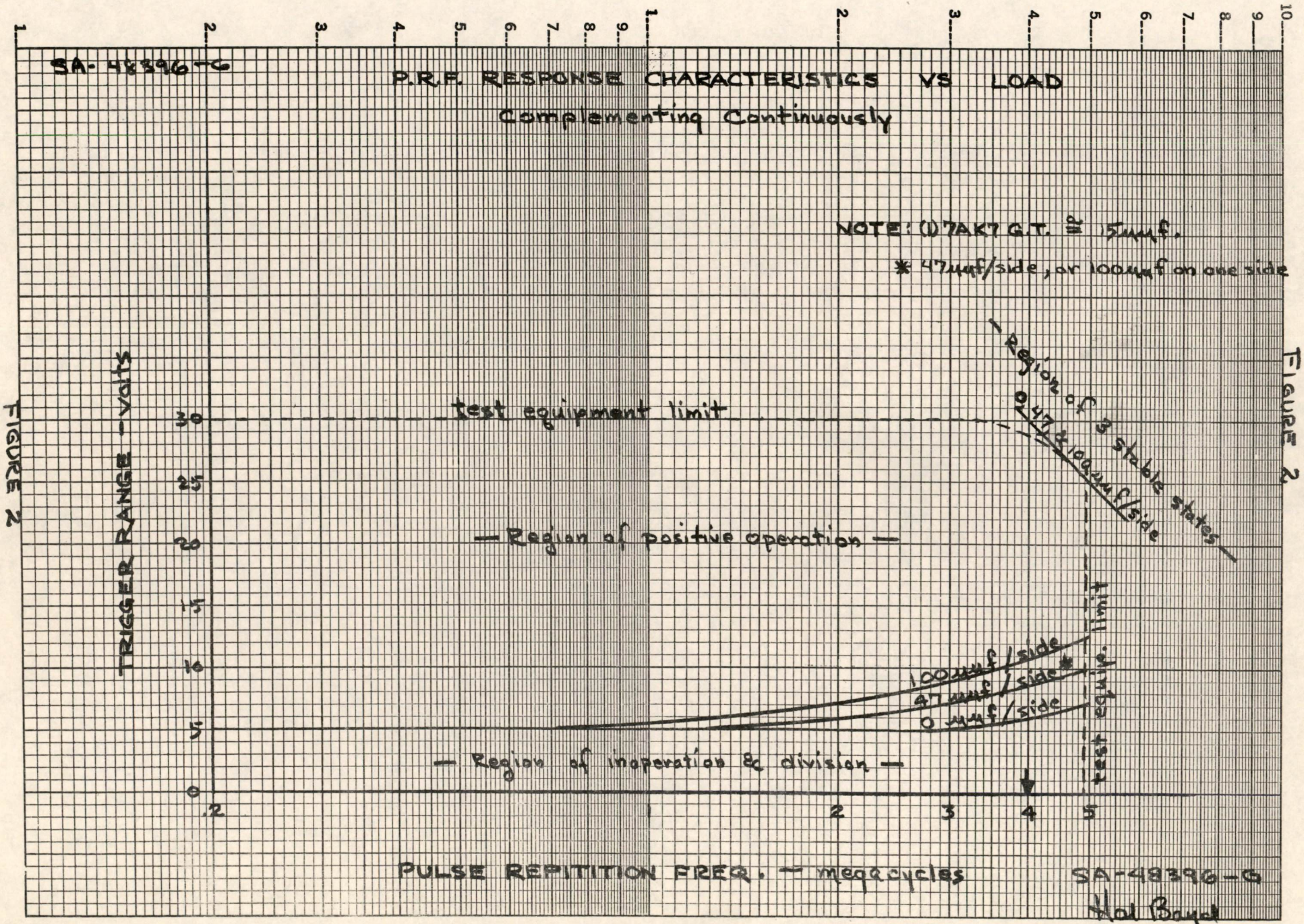


FIGURE 2

FIGURE 2

SA-48397-G

COUNTING CHARACTERISTICS

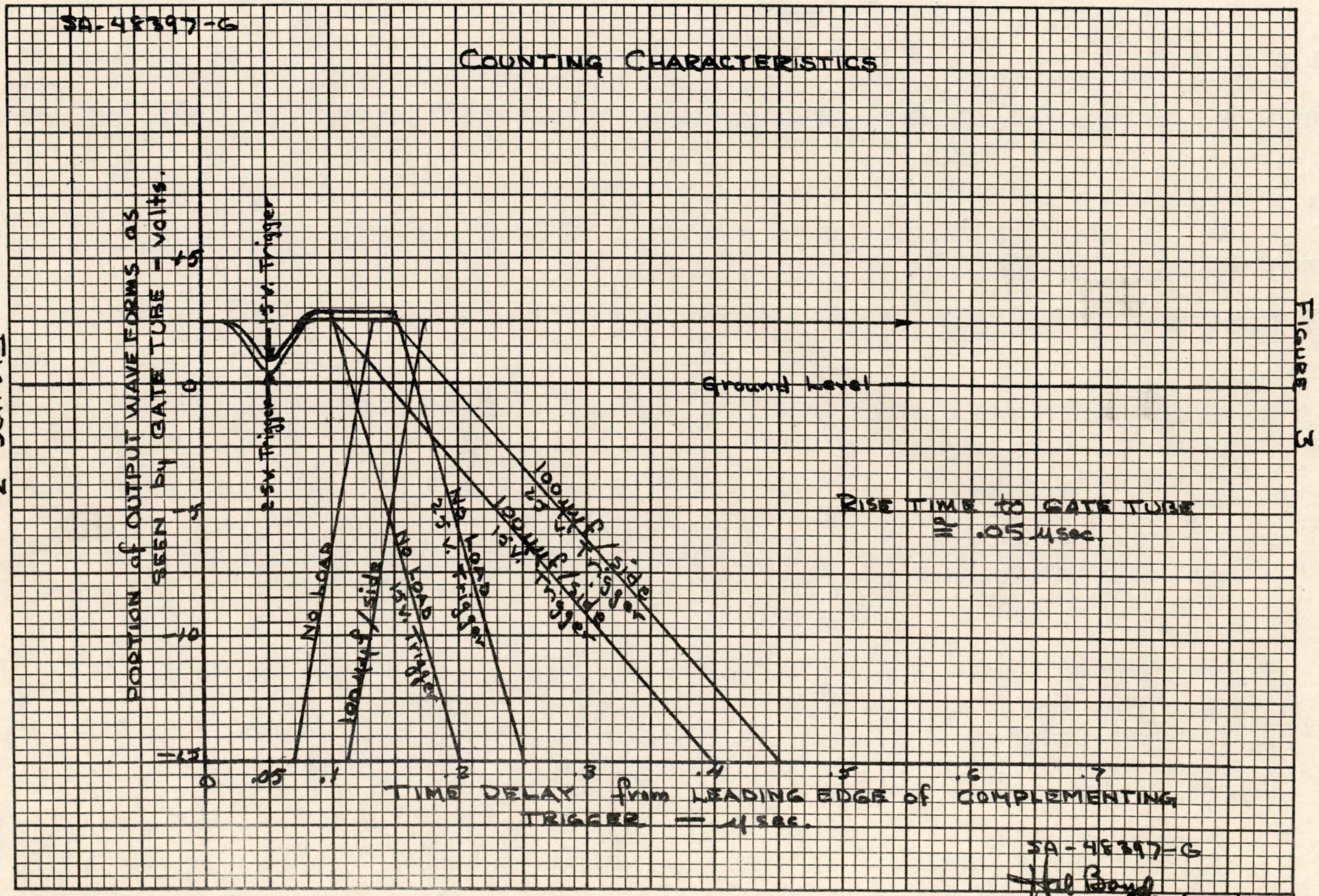


FIGURE 3

FIGURE 3

SA-48397-G

Hal Boyd

24th Feb '53

SA-48398-9

FLIP-FLOP BEHAVIOR with POOR TUBES

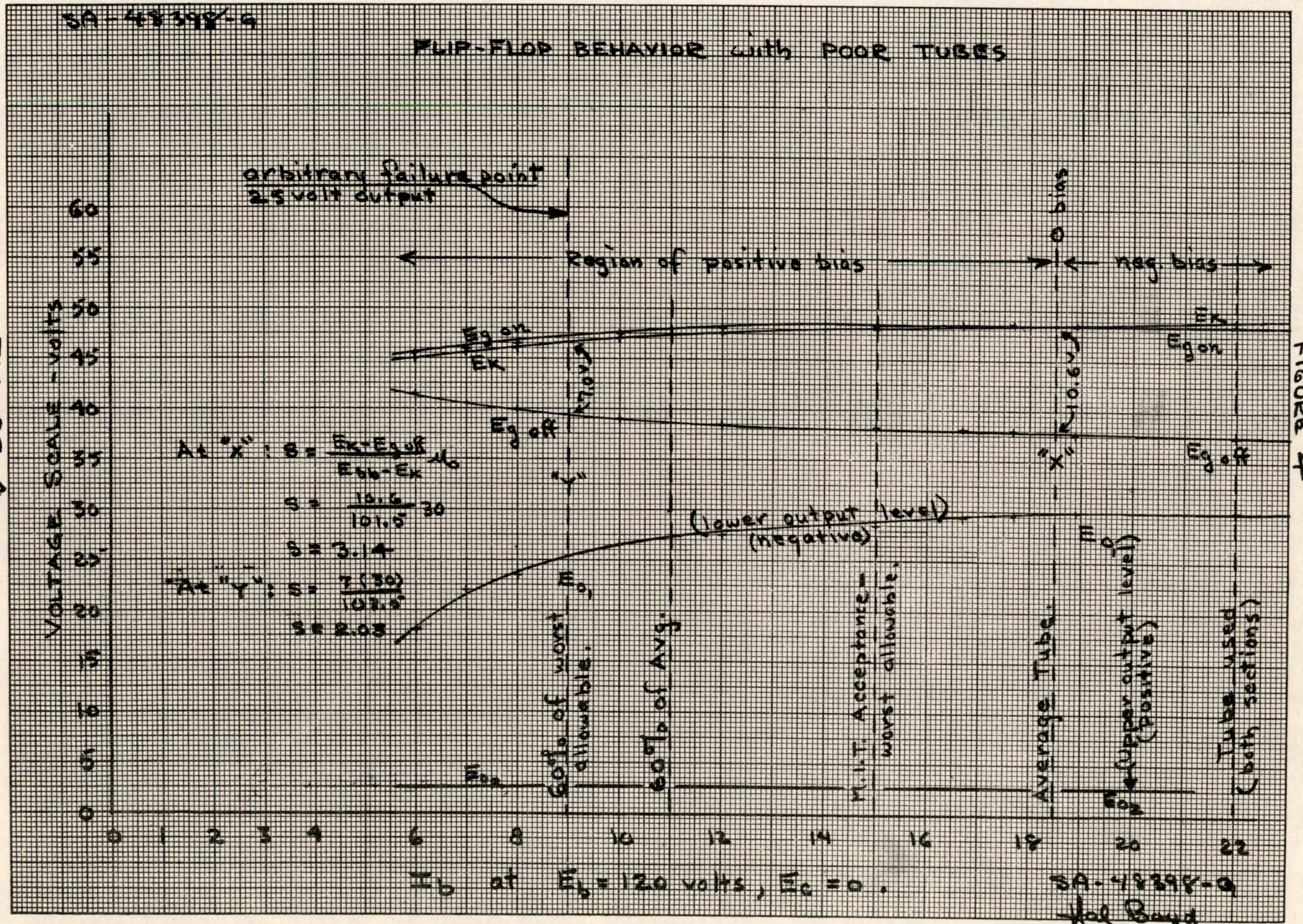


FIGURE 4

FIGURE 4

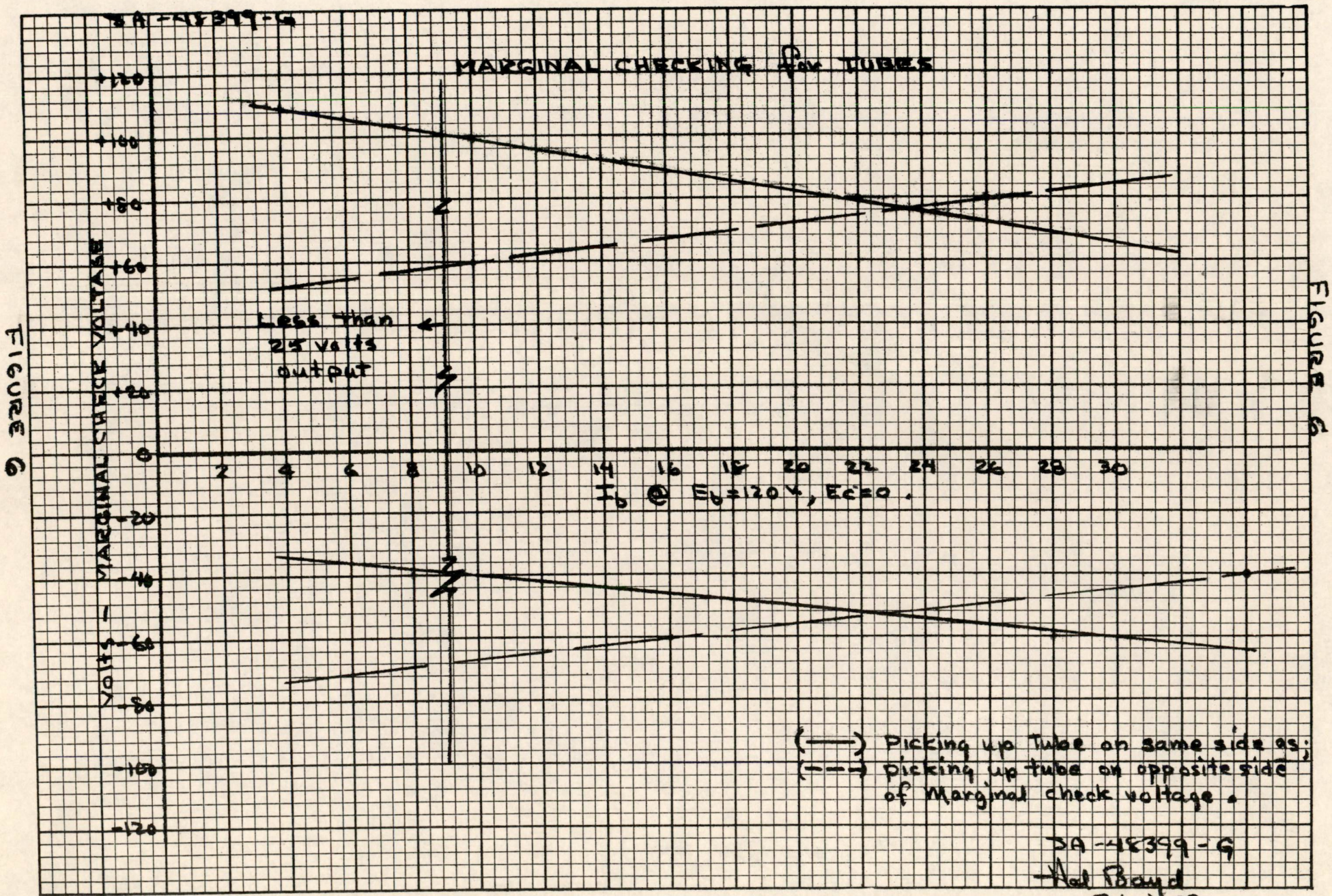


FIGURE 6

FIGURE 6

SA-418400-C

MARGINAL CHECKING THE DIVIDER RESISTORS

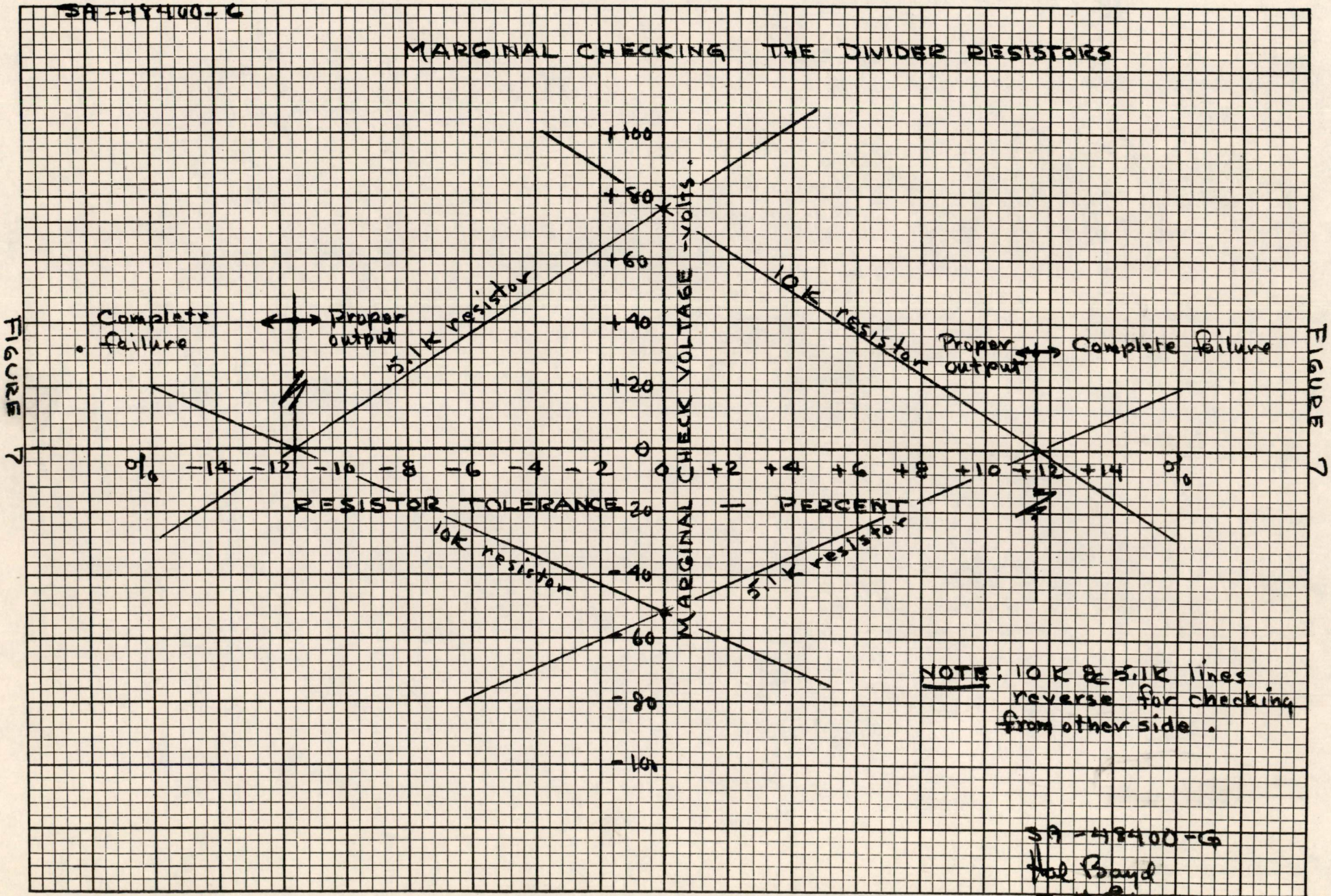


FIGURE 7

FIGURE 7

NOTE: 10K & 5.1K lines reverse for checking from other side.

SA-418400-C
Hal Boyd
20 Feb 53

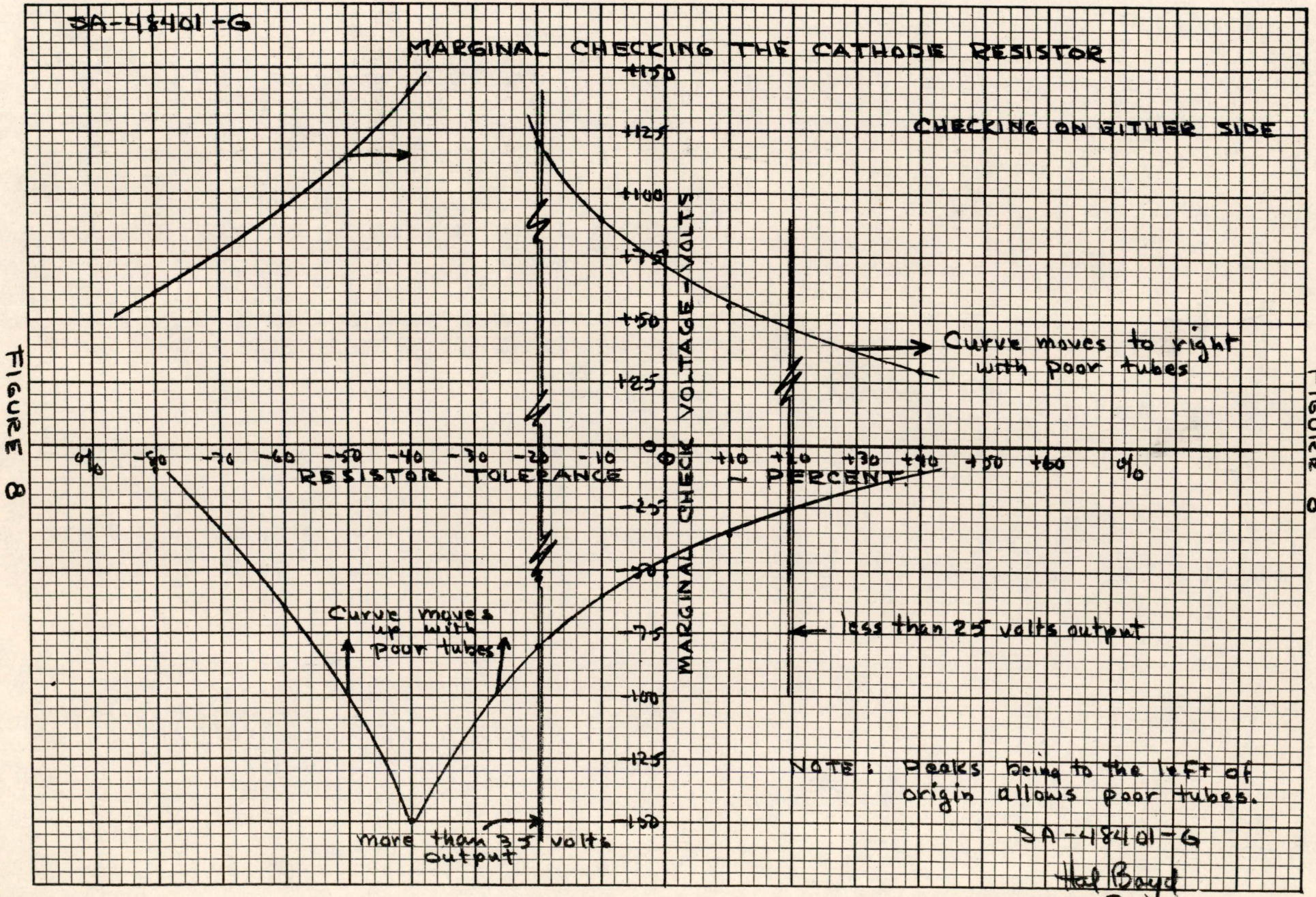


FIGURE 8

FIGURE 8

SA-48402-G

MARGINAL CHECKING THE 6.8K PLATE RESISTOR

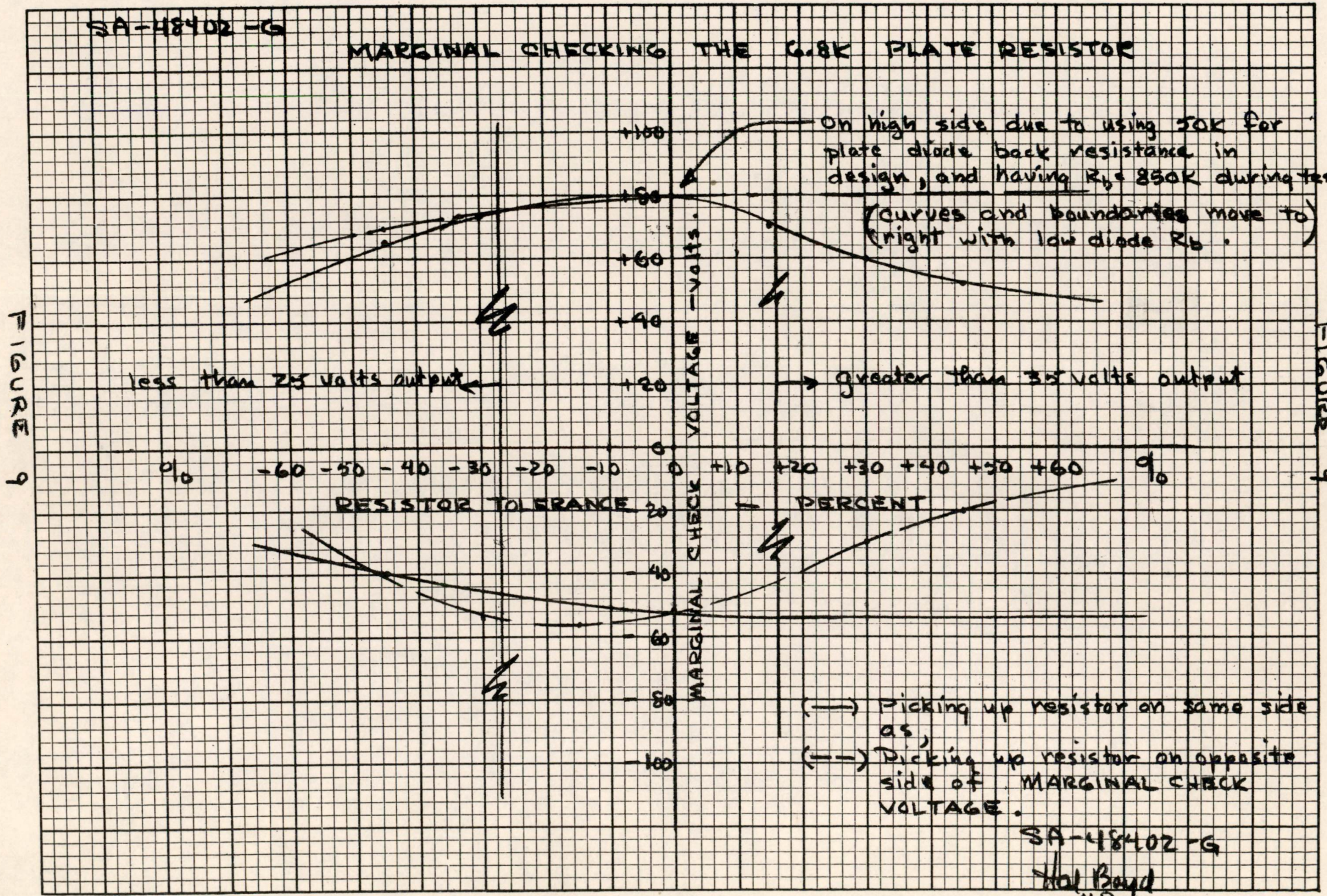


FIGURE 9

FIGURE 9

SA-48402-G

Hal Boyd

20th Feb. '53

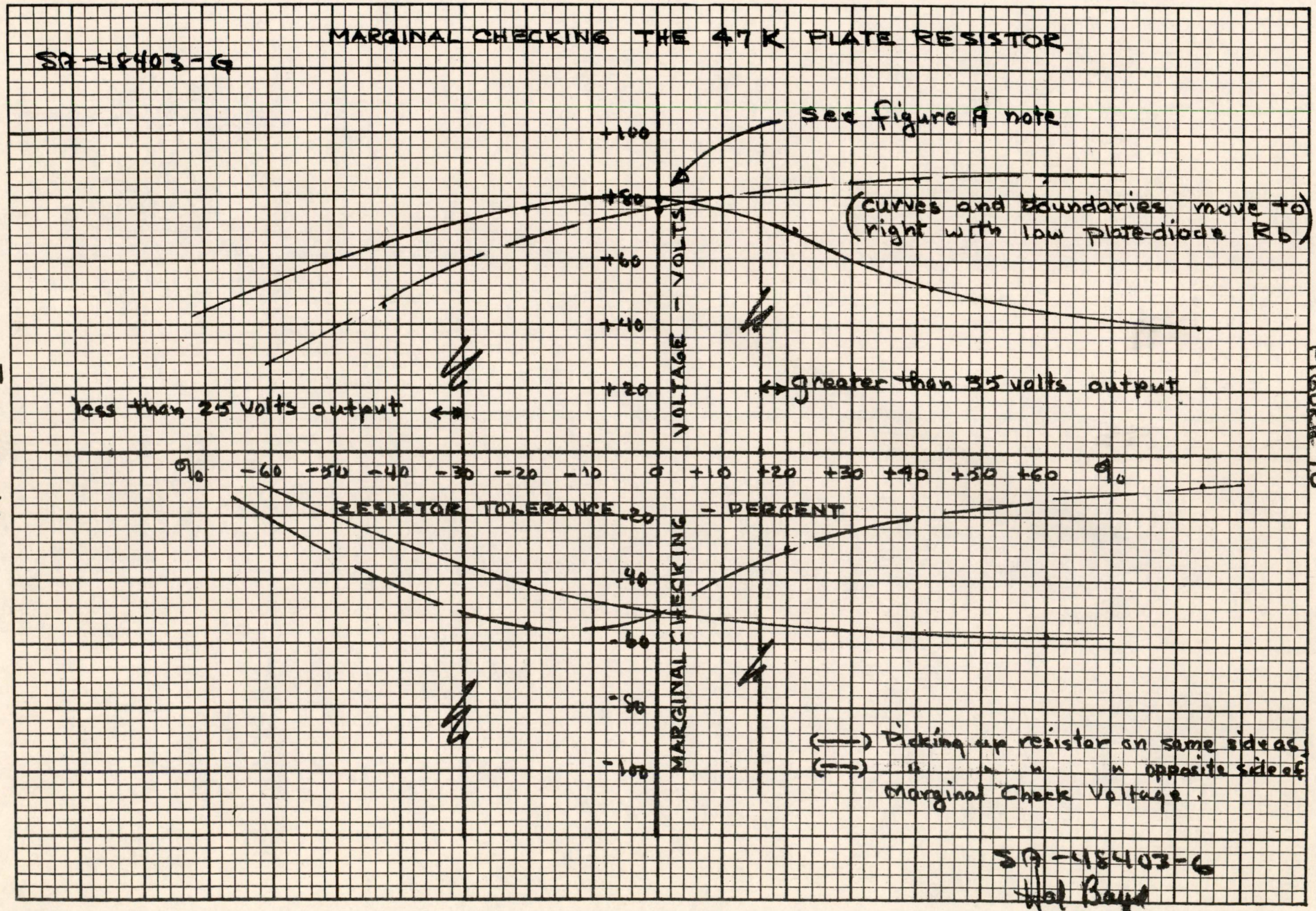


FIGURE 10

FIGURE 10

FIGURE 11

FIGURE 11

SA-48405-6

MARGINAL CHECK of
TRIGGER-DIODE BACK-RESISTANCE

+90
+6°
+3°
0
-3°
-6°
-9°

MARGINAL CHECK VOLTAGE — Volts

25K = R_p

20K 50K 100K 200K 500K

BACK RESISTANCE - K ohms

Failure

(——) Picking up diode on same side as ·
(- - -) " " " " opposite side of
Marginal Check Voltage.

SA-48405-6

Hot Boys
20 Feb 58

FIGURE 12

FIGURE 12

R. Buck

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: MATRIX DRIVING WITH UNIDIRECTIONAL PULSES

To: Jay W. Forrester

From: Dudley A. Buck

Abstract: Modification of the driving scheme during either the READ or the WRITE part of the READ-WRITE cycle would allow unidirectional current pulses in the rows and columns of a magnetic-matrix memory. This modification involves driving of all but the selected row and column during the modified part of the cycle. It requires additional low-level switching equipment and much larger total driving current, but with a tube-driven array, it eliminates half of the row and column wires and driver tubes.

The proposed modifications amount to adding a half-amplitude current to each row and to each column of a matrix memory array and then subtracting a full-amplitude current from every core via the z-plane winding. Each core is thus left with the same net mmf as in the unmodified driving scheme; the extra contribution of row and column is exactly cancelled out by the negative contribution of z-plane.

PROPOSED MODIFICATION I

The first proposed modification (see Figure) leaves WRITE ONE and WRITE ZERO unchanged.

READ is modified by subtracting a half-amplitude current from each row and each column and adding a full-amplitude current to the z-plane winding. The READ current in the selected row and column is then zero, the current in the unused rows and columns is minus one-half, and the z-plane current is plus one. The READ currents are now of the same polarities as the WRITE currents. A given row or column is driven once each cycle--either during READ or during WRITE. The z-plane current is plus one during READ, zero during WRITE ONE, and plus one-half during WRITE ZERO. The plus one would probably be made up of two plus one-half pulses.

The noise considerations during READ should be approximately the same as in the unmodified scheme as far as contributions due to flux changes in the cores are concerned. Stray coupling between the driven wires and the sensing winding, however, might cause greater noise pickup during READ.

PROPOSED MODIFICATION II

The second modification, suggested by R. R. Everett, leaves READ unchanged. WRITE is modified by adding plus one-half to each row and column and subtracting plus one from the z-plane winding. Once again, the row, column, and planar currents are of the same polarities during READ and WRITE.

The z-plane current is minus one during WRITE ONE and minus one-half during WRITE ZERO.

DISADVANTAGES OF NEW DRIVING SCHEME

1. Additional low-level switching equipment is required to drive all but one row and column.

2. With an n x n array, (n-1) times as much total pulse current is required during the modified part of the cycle.

3. Three values for z-plane current are required, namely, z = 0, 1/2, or 1.

ADVANTAGE OF NEW DRIVING SCHEME

1. With a tube-driven array, half of the row and column wires can be eliminated along with half of the heavy-current driver tubes.

Signed Dudley A. Buck
Dudley A. Buck

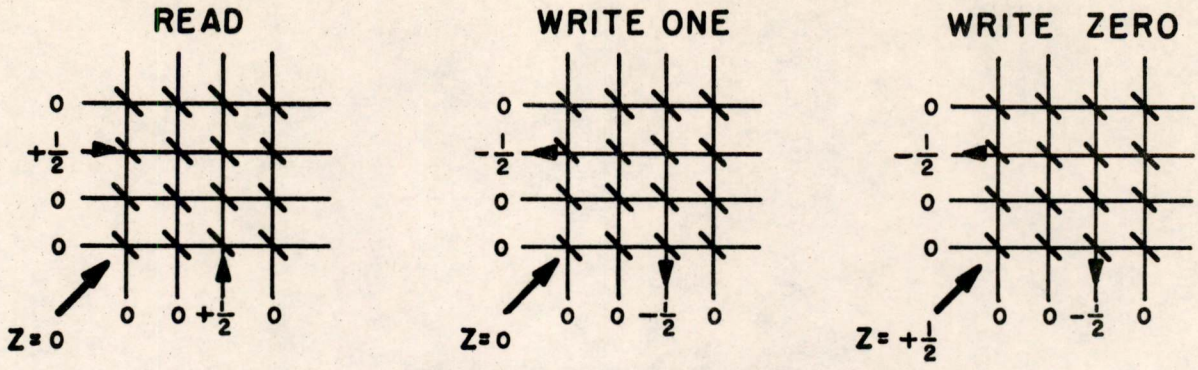
Approved William N. Papian
William N. Papian

DAB/jk

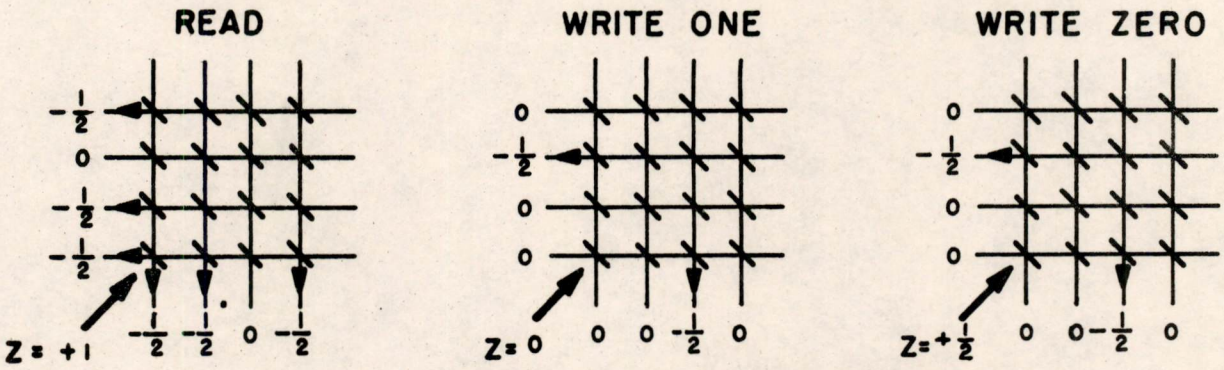
Drawings Attached:

Figure 1 A-53980

cc: Group 62
Group 63
R. R. Everett
IBM (6)



PRESENT DRIVING SCHEME



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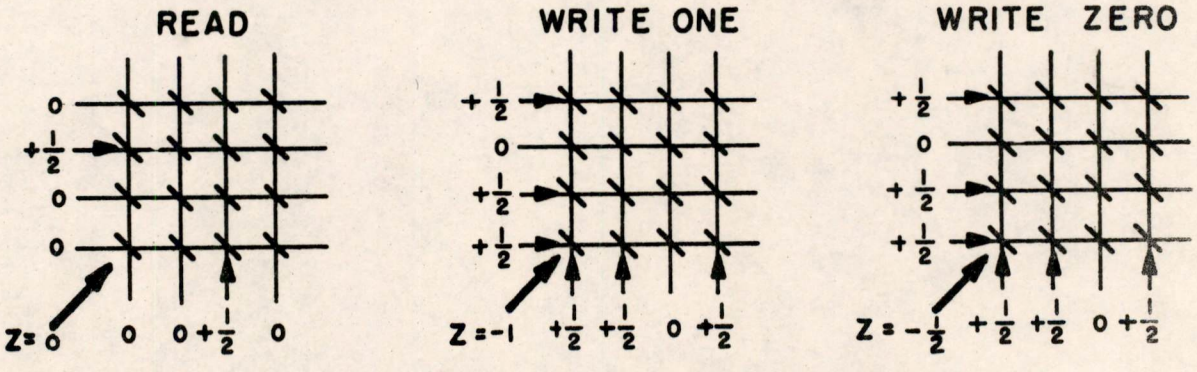

PROPOSED MODIFICATION II

MODIFIED DRIVING SCHEMES TO ALLOW UNI-DIRECTIONAL CURRENT PULSES IN THE ROWS AND COLUMNS OF A MAGNETIC MEMORY ARRAY

R. Olsen

6889
Engineering Note E-531

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: DRIVING CURRENT MARGINS ON MEMORY TEST SETUP I*

To: N.H. Taylor

From: S. Fine

Date: March 6, 1953

Abstract: The sources of noise in an array consist of inductive and capacitive coupling between driving lines and sensing winding, the outputs of half-selected cores and the differences in magnetic properties of the cores. The margins on driving currents are determined by these factors. The lower current limit is dependent mainly on the amplitude of disturbed-ONE and the upper limit by the amplitude of disturbed-ZERO and the half-selected outputs. Experimental results check the validity of a derived equation for determining current margins.

A. Noise sources

Difficulty has recently been experienced with discrimination of signal from noise in the Metallic Array Model I. Some noise signals have been large enough to cut ONES down to the size of noisy ZEROS when the constellation of stored information yielded noises of certain polarities and magnitudes.

There are four sources of noise. Two of these are due to capacitive and inductive coupling between the driving lines and the sensing winding. These sources of noise would be present in the absence of cores in the array. The third type of noise originates from the cores themselves and is due to the half-amplitude current pulses flowing

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* Widrowitz, B., "16 x 16 Metallic Memory Array Model I", R-216, Digital Computer Laboratory, M.I.T., September 25, 1952

through the cores on the selected X and Y driving lines. Differences in magnetic properties of the cores produce considerable variations in the cores' readout signals. The deviations about a mean may also be defined as noise, and this presents a fourth possible source.

B. Inductive and Capacitive Coupling

1. Discussion of noise mechanism.

If the sensing winding were fabricated with precise symmetry, the mutual inductance between the sensing winding and any driving line, including the XY windings, would be zero. This is not quite mechanically possible, however, and the actual value of this parameter may be unpredictable within a power of ten. The range of unpredictability may be controlled by careful construction. Perfection in construction will not eliminate noise due to capacitive coupling between the sensing winding and a driving winding, and the usual geometric aberrations will produce only second-order effects on this coupling. When a di/dt is applied to a driving line, that line is not an equipotential because of its distributed self-inductance. The unavoidable voltage gradient of the driving line is in part transferred to the sensing winding by means of the distributed mutual capacity.

2. Measurements of the noises.

The noises due to inductive and capacitive coupling were indistinguishable, both being roughly proportional to the di/dt of the drivers. There was no advantage in separating these effects, for their sum was the factor of interest. This was measured by writing all ONES into the array and driving the memory lines separately. Since the sensing winding links every other core in the opposite sense, the core noises should cancel except for core variations. Present are uncancelled core noises and coupling noise. A dummy array, identical to the original except that the metallic cores are replaced by fiber washers, was pulsed in the same manner. Less variation and somewhat smaller amplitudes of noises were found in the dummy array. As would be expected only coupling noises were present.

C. Delta Noise*

1. Source of delta noise.

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* Guditz, E.A., "Delta$_{ns}$ in Ceramic Array #1", Engineering Note E-488 Digital Computer Laboratory, M.I.T., October 14, 1952

In order to deliver excitation to a selected core in a coincident-current memory plane, the cores along the selected coordinate lines must be disturbed. This is unavoidable. When these cores are disturbed, they experience internal $d\theta/dt$ while following minor loops on the B-H plane. They are capable of inducing signals in the sensing winding which is threaded through every core in the memory plane. If the sensing winding linked the rows of cores parallel to the driving lines, the noise outputs of the non-selected cores would superpose in reinforcement. If, however, the sensing winding were passed through every other core in the same direction, the alternation from core to core would allow noise bucking.

There are several reasons for the imperfect cancellations that have been observed. Chief among these are the variations in magnetic properties of individual cores, and the differences in noise outputs of cores storing ZERO and those storing ONE. The latter is much more significant and gives rise to "delta noise." If the signal induced in a single-turn pickup winding by a core storing a ONE when driven by a half-amplitude switching current is called HSI, and the corresponding output of a core containing a ZERO is called HSO, then

δ = HSI - HSO is the delta noise.

Several methods have been employed to measure the size and effects on current margins of delta. A single delta is small, usually much smaller than a ONE, and has to be measured indirectly. It was found that a given constellation of ONES and ZEROS along a set of selected lines will not always yield a given amount of delta noise. As one might expect, the noise outputs of these half-selected cores depend upon the history of disturbances of each core from the times when the individuals were most recently switched. The half-selected output of an undisturbed ONE, HSI_1, is much smaller than the size of the corresponding ONE readout. It is due to a half-amplitude current pulse applied in a direction tending to switch that ONE; it does not decay to a null until the driving current is removed if the driving current is left on only long enough to switch a core. This suggests that some form of slow switching is taking place, most likely a departure from the saturation hysteresis loop onto some minor loop that is not very different from the major loop. Subsequent half-selected readouts after the first are all almost identical and turn out to have amplitudes that are much less than HSI_1 at the optimum sensing time.

$$HSI_1 > HSI_2 \approx HSI_3 \ldots\ldots\ldots$$

The HSO, the half-selected output of a core containing ZERO, is hardly affected by disturbance at low and medium driving currents and is very much smaller than HSI_1.

$$HSO_1 \approx HSO_2 \approx HSO_3 \ldots\ldots\ldots$$

Let HSO be the non-selected output of a ZERO after any number of disturbs. Then,

$$\delta_1 = HSI_1 - HSO, \delta_2 = HSI_2 - HSO, \delta_3 \approx HSI_2 - HSO \quad \text{etc.}$$

At lower currents, since $HSI \gg HSO$,

$$\delta_1 \approx HSI_1, \delta_2 \approx HSI_2 \approx \delta_3 \approx \delta_\infty$$

so that the noise of a single delta is approximately equal to the output of a half-selected core containing a ONE.

2. Measurement of delta noise.

Several methods have been employed to measure the size of delta, and to estimate its effects upon current margins. A single delta is small, usually much smaller than a ONE. In order to get this quantity, it was found necessary to measure the cascaded effect of many cores and thence to arrive at an average figure. This was achieved by writing a pattern into the memory so that all cores whose sensed output is positive held ONES and the others held ZERO. A single half-current pulse was applied to the Z-plane winding so that all cores were half-selected in the read direction. The resulting sensed output is the sum of 128 deltas. The Z-plane winding was pulsed a second time to obtain the sum of 128 second deltas. As expected, the second, third, and later deltas did not change in amplitude.

A second method of measuring delta is with the single-core pulse tester. The results of both methods compared favorably.

D. Core Variations

Because of manufacturing difficulties, the variation in core

switching time and voltage amplitude in different cores is great, and it is necessary to test each core carefully and to select only cores within an allowable percentage deviation. This variation or spread in ONES can be considered as a noise in the calculation of probable current margins. The lowest core output is a factor determining the lowest allowable driving current. The variation in delta is the major factor in current margins. Since it will be assumed that the amplitude distribution of the HSI output is the same as the distribution of the ONES and that delta is approximately equal to HSI, then delta will have the same amplitude variations as ONE output.

The output voltage amplitude variation among the curves of Memory Plane 1 is 20% about a mean value. For the present plane, Memory Plane 6, it is 12% about a mean value. (During the year of operation of Memory Plane 1, no noticeable change in core variation was detected.)

E. Current Margins

1. Definition and measurement

Current margins are to be defined as the mean limits of driving current that can be tolerated without interruption of the normal operation of the memory. It is necessary to know the current margins so that a satisfactory method of marginal checking can be incorporated into a computer. Current margins are also a convenient means of judging the qualities of cores.

At present the only means of determining the current margins is by single or multi core testing or by building a magnetic-core memory plane and varying the driving currents until normal operation fails. Obtaining current margins by single-core testing is not as inclusive as the other method in that certain factors encountered in the operation of an array of cores, such as the effects of a first and second delta, are not present to affect the current margins.

2. Determination of lower current margin

A method of calculating current margins from known core characteristics will be derived. It was noticed through experimentation that the lower current margin is determined by the smallest ONE output. This output, amplified, has to be equal to or greater than the bias voltage used to keep the "and" gate cut off at the sensing amplifier output. If the current is reduced too far, the ONE output is not above the gate level, and the ONE is lost. Also, in any memory plane using two-to-one

selection and always a complete read-write cycle there can be only two first deltas. Using these two facts, the smallest ONE output at the lowest current margin can be determined.

The worst operating condition should be considered in determining the lowest current margin. It is understood that in coincident-current operation, the sensed output of a selected core consists of the summation of all the voltages induced in the sensing winding, i.e., disturbed-one voltage plus all half-selected voltages. The worst pattern at the lowest current margin therefore must have the selected core holding ONE and all other cores in the selected lines alternating ONE and ZERO, the polarity of the disturbed ONE being opposite the half-selected ONE output. See Figure 1-a. The resulting signal output is the disturbed ONE minus two first deltas. The second-delta signals have a small amplitude at the lowest current margin and can be disregarded. The resulting output after amplification must be equal to the gate bias voltage.

$$V_g = (1_{D_S} - 2\delta_{1_S})\, G$$

V_g = gate bias voltage

G = sensing amplifier gain at normal operation

δ_{1_S} = (HSI - HSO) average value of first delta at lowest current

1_{D_S} = smallest disturbed-ONE at the lowest current = $1_{A_S}(1-c_1)$

1_{A_S} = average value of 1_D at lowest current

c_1 = percentage distribution of disturbed-ONE about a mean value

$$\frac{V_g}{G} = 1_{A_S}(1-c_1) - 2\delta_{1_S}$$

The distribution of delta is not being considered at the lowest current margin because the average delta magnitude is small.

From single-core pulse tests enough points to plot a distribution curve of ampere-turns against voltage output for the disturbed-ONE output and first and second delta were obtained. See Figure 2. Near the lower current margin region the first delta output is small and the

amplitude of the disturbed-ONE has the most effect on the margin. A straight-line relationship can be approximated near this region with reasonable accuracy. From this assumption the equation for 1_D is,

$$1_D = K_1 I_s + K_2$$

and for the first delta is,

$$\delta_1 = K_3 I_s + K_4$$

Substituting the above values in the preceding equation and solving for I_s, the lowest current

$$I_s = \frac{V_g/G + 2K_4 - K_2(1-C_1)}{K_1(1-C_1) - 2K_3}$$

3. Calculation of largest operating current.

Increasing the driving current to a large value moves the mmf applied to a given core out to a point near the knee of its B-H loop. Increasing the current a small amount after this point has been reached will cause a great change in the half-selected output voltage. The core starts to switch, and its distrubed-ONE output drops. Increasing the current still further will allow the half-selecting pulses to switch the core, and the disturbed-ONE output will drop toward zero. The largest operating current is reached long before this occurs. The highest current margin therefore is determined mainly by the delta outputs.

As in the case of the lower current margin, the worst operating condition must again be assumed, that is, the condition where an operational error occurs and a ONE is rewritten in place of ZERO. This will happen when the summation of the disturbed-ZERO plus all half-selected outputs becomes as large as a ONE. For this case the worst pattern consists of the selected core holding ZERO while half of the remaining cores in the selected lines hold ONE. The half-selected outputs of these cores should be of the same polarity as the disturbed-ZERO output. See Figure 1b. The equation of the resultant signal output is,

$$V_g = (0_{D_L} + 2\delta_{1L} + (N-2)\delta_{2L})G$$

δ_{1L} = first delta at largest current

δ_{2L} = second delta at largest current

O_{DL} = disturbed ZERO at largest current

N = number of cores in a given line

The amplitude of the first delta is large now, and its distribution must be considered. If the assumption is made that its percentage distribution is the same as the distribution of disturbed-ONE, then the largest first delta,

$$\delta_{1L} = \delta_{AL}(1 + C_1)$$

δ_{AL} = average first delta at the largest current

C_1 = percentage distribution in cores

The distribution of the second delta will not be considered because the magnitude of the second delta is small compared to the first delta.

A linear relationship of delta and current can be approximated at the higher current range.

$$\delta_1 = K_5 I_L + K_6 \quad ; \quad \delta_2 = K_7 I_L + K_8$$

A linear relationship of disturbed-ZERO and current can likewise be approximated.

$$O_D = K_9 I_L + K_{10}$$

If the distribution in disturbed-ZERO and disturbed-ONE are assumed the same,

$$O_D = (K_9 I_L + K_{10})(1 + C_1)$$

The critical output voltage is now,

$$V_{s/G} = (K_9 I_L + K_{10})(1+C_1) + 2(K_5 I_L + K_6)(1+C_1) + (N-2)(K_7 I_L + K_8)$$

Solving the equation for I_L, the largest current,

$$I_L = \frac{V_g/G - (1+C_1)(2K_6 - K_{10}) - K_8(N-2)}{(1+C_1)(2K_5 + K_9) + K_7(N-2)}$$

For exceptionally good cores, the second delta is very low in amplitude and may be disregarded, even at I_L, that is, K_7 and K_8 may be taken as zero is value.

$$I_L = \frac{V_g/G - (1+C_1)(2K_6 - K_{10})}{(1+C_1)(2K_5 - K_9)}$$

The percentage of current margins about a mean value can be found by the equation -

$$\pm \left(\frac{I_L - I_S}{I_L + I_S} \right) \times 100\%$$

4. Obtaining equation constants.

C_1, the core distribution, is determined by the final selection of cores. The value should be kept as low as possible. From single or multi-core tests, a plot of disturbed-ONE, disturbed-ZERO, first delta and second delta against ampere-turns for average cores can be obtained. Equations for the above factors can be determined from the plotted curves and all K constants found.

E_g, the bias voltage of the sensing gate tube, is a circuit parameter. G is the sensing amplifier gain at normal operating conditions. Increasing or decreasing the gain will not change the percentage of current margins but will affect the maximum and minimum driving currents.

F. Validity of Derived Equations

1. Memory Plane #1.

Figure 2 is a plot of disturbed ONE, disturbed ZERO, first and second delta outputs against driving currents. Linear relationships of voltage output and driving current can be approximated from the plotted

curves. All constants needed are then obtained from the linear equations.

As indicated on Figure 2, the disturbed ZERO and the first and second delta outputs are finite, even at low driving currents. By using simplified equations, it will be shown that this plane cannot hold a "worst" type of pattern at normal operating currents, and therefore it will not hold a "worst" pattern at a higher or lower driving current.

"Worst" type pattern with a disturbed ONE output.

The output signal is the smallest disturbed ONE less 2 largest possible first deltas and less 14 largest second deltas. This, amplified, must be equal to or greater than the bias voltage V_g.

$$V_g \leq [1_D(1-C_1) - 2\delta_1(1+C_1) - (N-2)\delta_2(1+C_1)]\,G$$

$V_g = 25$ volts

$G = 7000$

$C_1 = \pm 20\%$

$1_D = 7$ mv
$0_D = 0.6$ mv
$\delta_1 = 0.5$ mv
$\delta_2 = 0.1$ mv

} From fig. 2 at $I_m = 240$ ma.

$$25 \leq [7(.8) - 2(.5)(1.2) - 14(.1)(1.2)] \times 10^{-3} \times 7000$$

$$25 > 19.04$$

This indicates that the output signal from the sensing amplifier is below the 25-volt gate needed to rewrite the ONE.

"Worst" type pattern with disturbed ZERO output.

The output signal consists of the largest disturbed ZERO plus 2 largest first deltas plus 14 largest second deltas. This signal, amplified, should be less than the gate biasing voltage.

$$V_g > [O_D(1+C_1) + 2\delta_1(1+C_1) + (N-2)\delta_2(1+C_1)]\,G$$

$$25 > [0.6(1.2) + 2(.5)(1.2) + 14(.1)(1.2)]\times 10^{-3}\times 7000$$

$$25 < 25.2$$

This indicates that the output signal is larger than the 25-volt gate level and would cause a ONE to be rewritten in place of a ZERO.

These types of errors did indeed occur at normal operating currents for plane #1. At higher and lower currents, the situation was worse; current margins were "less than $\pm$ 0%."

2. Memory Plane #6

From data taken on Memory Test Setup I using plane #6, the curves of Figure 3 were plotted. It was found that the magnitude of the second delta was too small to be measured accurately and so would be assumed zero throughout the useful current range. Also, the magnitude of the first delta and disturbed ZERO were small at the lower driving currents and could be assumed zero at this margin. Linear equations were approximated for the disturbed ONE at the lower current limit and the disturbed ZERO and first delta at the upper limit. The constants needed were determined from these equations.

Lower Current Margin.

$$I_S = \frac{V_g/G + 2K_4 - K_2(1-C_1)}{K_1(1-C_1) - 2K_3}$$

$\delta_1 \approx 0$ therefore $K_3 = K_4 = 0$

$$I_S = \frac{V_g/G - K_2(1-C_1)}{K_1(1-C_1)}$$

$V_g = 25$ Volts

$C_1 = 12\%$ distribution in amplitude of cores

$G = 1500$

$K_1 = 0.74$

$K_2 = -0.103$

$$I_S = \frac{25/1500 - (-.103)(1-.12)}{(.74)(1-.12)} = 0.164 \text{ Amperes}$$

Upper Current Margin.

Equation for exceptionally good cores will be used.

$$I_L = \frac{V_g/G - (1+C_1)(2K_6 + K_{10})}{(1+C_1)(2K_5 + K_9)}$$

$K_5 = .25$

$K_6 = -.06$

$K_9 = .21$

$K_{10} = -.05$

$$I_L = \frac{25/1500 - (1+.12)[2(-.06) + (-.05)]}{(1+.12)[2(.25) + (.21)]} = 0.260 \text{ Amperes}$$

The current margins are:

$$\pm \left(\frac{I_L - I_S}{I_L + I_S} \right) \times 100\%$$

$$\pm \left(\frac{.26 - .164}{.26 + .164} \right) \times 100\% = \pm 22\%$$

The actual current margins of Memory Test Setup I using plane #6 were determined by varying the driving currents until an error occurred. The current margin percentage was approximately ± 20%.

Unfortunately, complete curves like those of Figures 2 and 3 were never taken for these cores in a single-core test setup. However, the few points that were recorded fall close to the curves in the figures.

Signed S. Fine
S. Fine

Drawings:

A-54187
A-54186
A-54177

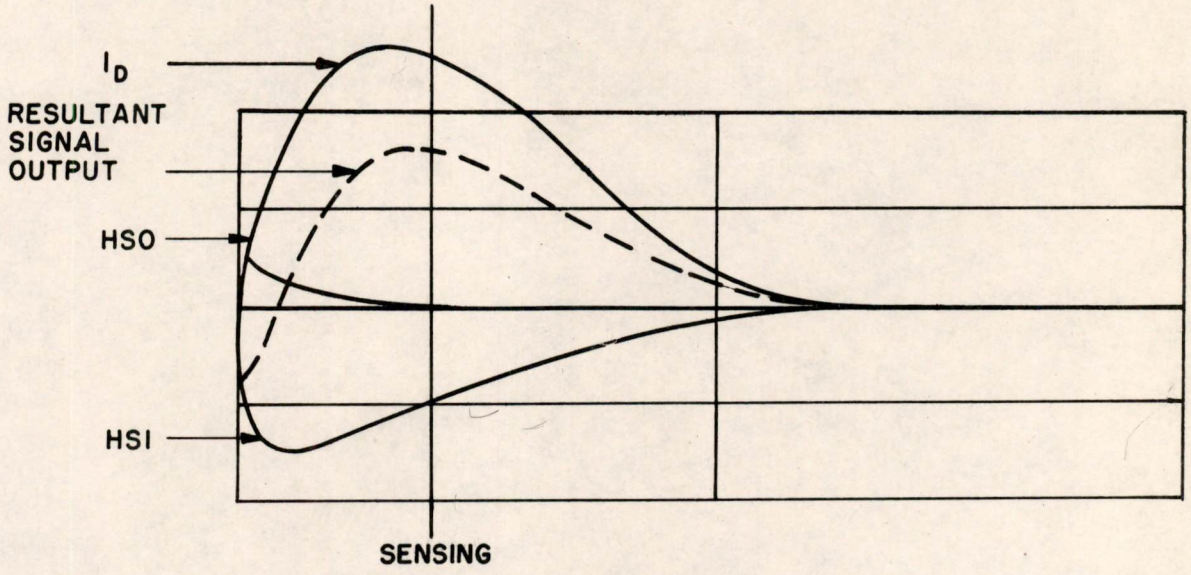
Approved
W.N. Papian

Approved
N.H. Taylor

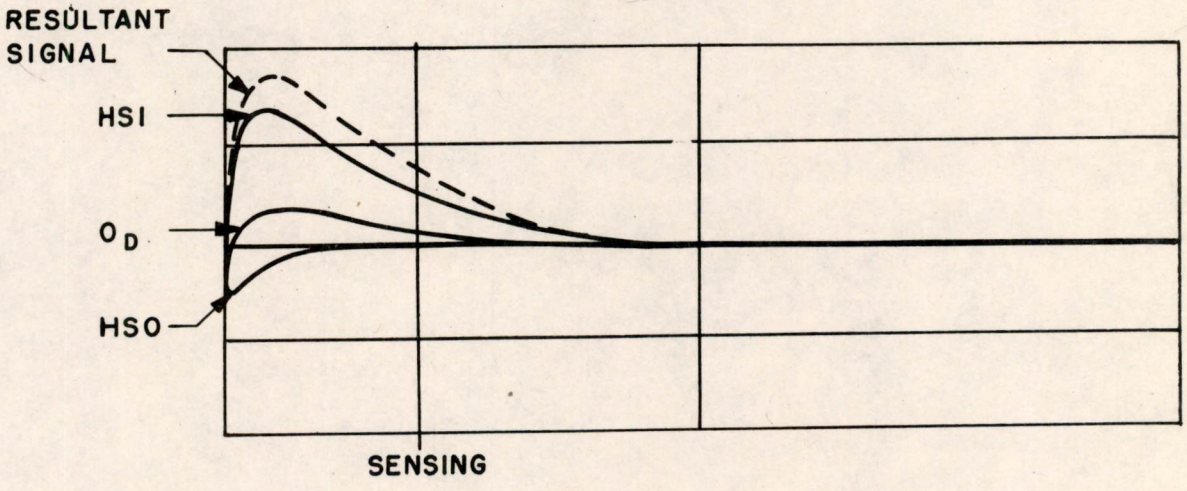
SF/cs

Drawings attached:

A-54187
A-54186
A-54177



A. DISTURBED "ONE" OUTPUT



B. DISTURBED "ZERO" OUTPUT

FIG. 1

A-54187

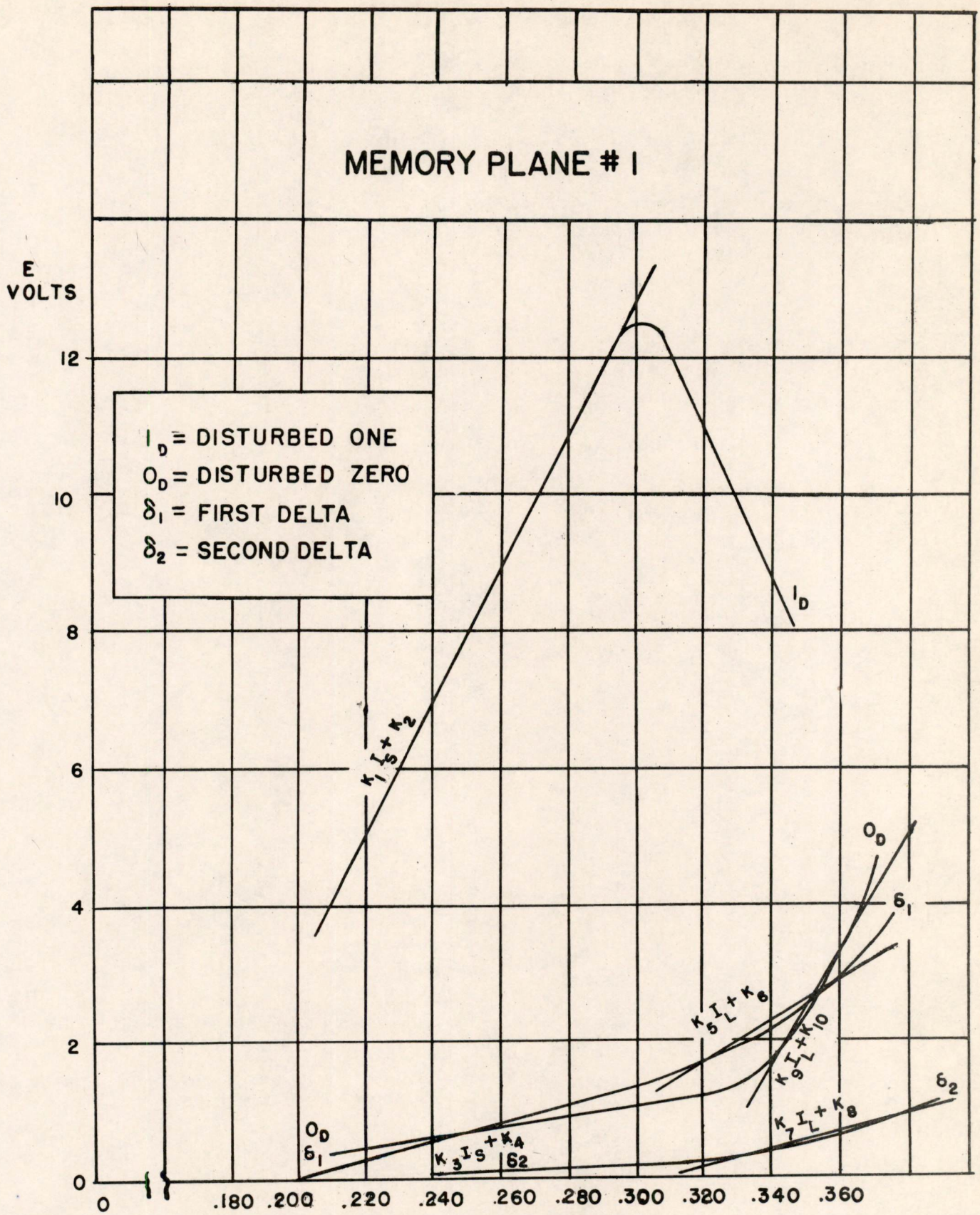

MEMORY PLANE # 1
E
VOLTS
12
10
8
6
4
2
0
I_D = DISTURBED ONE
O_D = DISTURBED ZERO
δ_1 = FIRST DELTA
δ_2 = SECOND DELTA
I_D
$K_1 I_S + K_2$
O_D
δ_1
$K_5 I_L + K_6$
$K_9 I_L + K_{10}$
δ_2
$K_7 I_L + K_8$
O_D
δ_1
$K_3 I_S + K_4$
δ_2
0
.180
.200
.220
.240
.260
.280
.300
.320
.340
.360
I_M DRIVING CURRENT — AMPS.

FIG. 2

A-54186

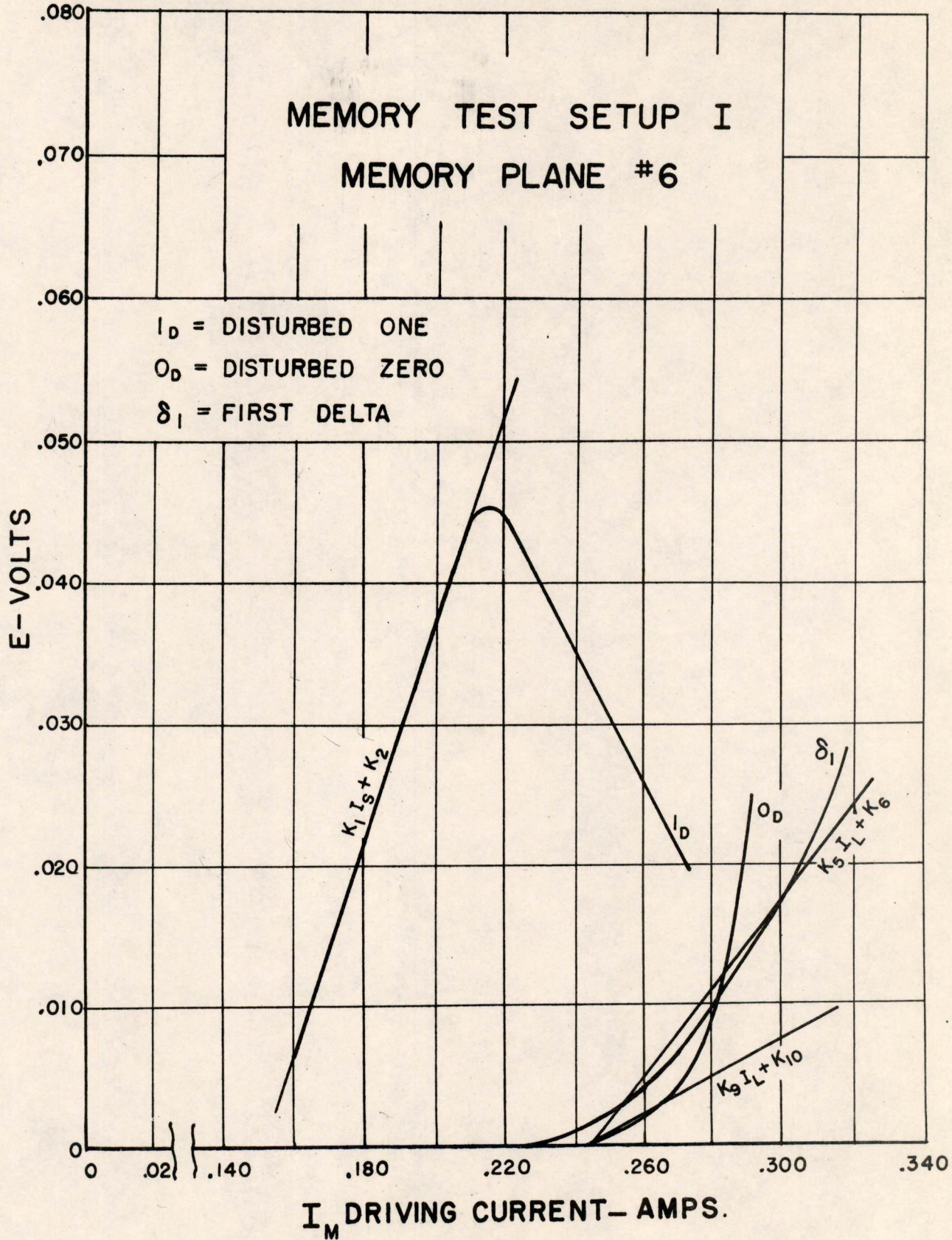

MEMORY TEST SETUP I
MEMORY PLANE #6
I_D = DISTURBED ONE
O_D = DISTURBED ZERO
δ_1 = FIRST DELTA
E-VOLTS
.080
.070
.060
.050
.040
.030
.020
.010
0
$K_1 I_S + K_2$
I_D
O_D
δ_1
$K_5 I_L + K_6$
$K_9 I_L + K_{10}$
0
.02
.140
.180
.220
.260
.300
.340
I_M DRIVING CURRENT- AMPS.

FIG.3

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: EFFECT OF CURRENT PULSE DURATION ON THE PULSE RESPONSE OF M.T.C. MEMORY CORES

To: Group 62 and 63 Engineers

From: P. K. Baltzer

Date: March 10, 1953

Abstract: The pulse response of ferrite memory cores, that will be used in M.T.C., has been found as a function of Current Pulse Duration. It has been found that reduction of Current Pulse Duration to 1.5 microseconds is the practical limit for best operation. Calculations made concerning signal discrimination of memory arrays indicate that discrimination of signals from 64 x 64 arrays of M.T.C. cores will be marginal--even using a Post-Write disturbing pulse when writing ones in the memory.

The "access time" of a computer memory is of utmost importance concerning its integration into the computer as a whole. The access time of a coincident current memory will be a function of the number of necessary current pulses for a given operation, the current pulse duration, and unavoidable "red tape" time. An investigation has therefore been made on the effect of current pulse duration on the pulse response of the cores that will make up the M.T.C. memory.

When cores are used in a coincident memory plane the Delta output is cumulative as noise and thus is increasingly important as the size of a memory plane is increased. This is shown in E-488[1] where Delta is also defined. Due to the extremely high ratio of the Undisturbed One output to the Delta output (of the order of 1000 for long current pulse lengths) considerable difficulty has been experienced in measurement of Delta. This difficulty is the effect of the Read-Write output which tends to paralize the scope pre-amplifier during measurement of the Delta output. The difficulties just described have been overcome by measuring Delta for this investigation using the circuit shown in Figure 1, where groups of cores connected in series are indicated as a single large core. Standard pulse output response is sensed from Group A. Delta is measured as the output of Group A, B and C which are so connected as to give Delta from Group A and B while the Read-Writes from Groups A and B are cancelled by those of Group C. The information obtained from this experiment is

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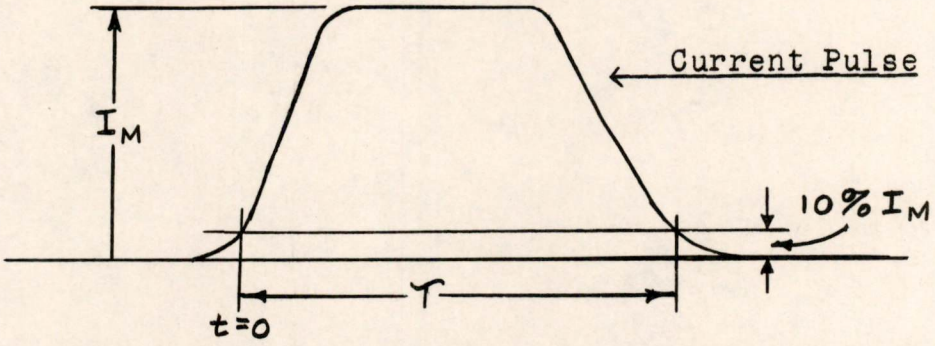
1 Engineering Note E-488 $Delta_{NS}$ In Ceramic Array #1 by E. A. Guditz

therefore an average for 100 cores.

The cores tested were a General Ceramic ferrite, body MF-1326B - die F-291. These cores were taken from Lot #4 and had already been selected, by the Production Test Group, for M.T.C. with a Disturbed One output of 0.11 and 0.12 volts at .57 μsec.

The Current Pulse Duration (τ) is defined as the time from 10% of maximum current on the rise of the pulse to 10% of maximum current on the fall of the pulse. The rise time of the



current pulse was 0.2 μsec. from 10% to 90% of maximum current and the fall time 0.3 μsec. from 90% to 10% of maximum current.

The complete test cycle for a given measurement consisted of 40 Read-Write pulses and then 40 Half-Selecting pulses, with a P.R.F. of 5,000 cycles. The actual sequence of pulses for each particular group of cores indicated in Figure 1 is shown in Figure 2 for each measurement made.

The Undisturbed One output has been found as a function of Current Pulse Duration (see Figure 3). The output is a maximum at τ = 1.2 μs for all driving forces. This can be attributed to the fact that, as the current Pulse Duration (τ) is decreased from 4 μsec to 1.2 μsec, a different hysteresis loop is traversed in the two cases.

Typical Undisturbed One output pulses and the corresponding Hysteresis Loops are shown in Figure 4 for the same driving force (ampere turns), but different values of Current Pulse Duration. Output pulse "α" is the result of the core being driven by 10 μsec. pulses, and "β" is the result of being driven by 1.2 μsec. pulses. The output pulses correspond to the following travel on the Hysteresis Loops, for pulse "α" the core is changed from the state at point 1 to that at point 2, whereas for pulse "β" the core is changed from the state at point 3 to that at point 4. The flux change for pulse "β" is about 85% of that for pulse "α" as is found by integration over the positive portion of each. Output pulse "γ" is the result of the core being driven by 1.2 μsec. pulses before being sensed and then read by pulsing the core with a 10 μsec. pulse. Pulse "γ" exactly duplicates pulse "β" except as indicated. The difference

in the wave forms is of course indicative of the reason for the different hysteresis loops. Insufficient energy is available for short current pulse duration to switch domains that have higher resistance to change, caused either by the geometry of sample or variations within the material itself. Hence, there is an increase of the number of domains of reverse magnetization present at the remanent point 3 as compared to those present at point 1. These additional domains of reverse magnetization at point 3 are also in areas that were hard to magnetize from the point 1. Hence, the total effect of short pulse duration is not only to shorten the pulse output, but also to increase the initial rate of change of flux to the extent that the maximum for the case where τ = 1.2 μs is greater than that for longer current pulse excitation. As the current pulse duration is further reduced of course the core is no longer able to switch and the Undisturb Output falls off rapidly.

Curves of the Disturbed One output are shown as a function of Current Pulse Duration in Figure 5. The effectiveness of Half-Selecting Pulses is heightened as the Current Pulse Duration is reduced, since a smaller effective Hysteresis Loop is involved. For NI_m = 90 amp turns the half amplitude pulse evidently does not greatly exceed the knee of the basic hysteresis loop even for the entire range of Current Pulse Duration from 4 μsec down to 1.2 μsec. Therefore, for the case of NI_m = 90 amp turns the Half-Selected output pulse is very short, as compared to those for the higher driving forces, at low values of Current Pulse Duration. If the number of Half-Selecting Pulses were increased sufficiently the full disturbing effect would be realized even for the higher driving forces. Hence, to duplicate this worst situation as far as possible the length of the Half-Selecting pulses was kept a constant of 20 μsecs for the measurement of both the Disturbed One and the Disturbed Zero. The effect of the disturb overcame the effect discussed concerning the increase of the Undisturbed One at τ = 1.2 μs for the case of NI_m = 90 A-T but for higher driving forces even this large number of disturbs (40) and the long duration of the Half-Selecting current pulses was not sufficient to offset the effect causing the maximum previously discussed for the Undisturbed One.

Since it is planned to sense the output of a core in time, all other measurements of output voltages have been made at the time to the maximum value of the Disturbed One Output. This time has been found as a function of Current Pulse Duration (see Figure 6). There is a reduction of almost 40% as Current Pulse Duration is reduced from 4 μsecs. to 1.2 μsecs.

The Disturbed Zero increases greatly for shorter Current Pulse Duration (see Figure 7), with τ = 1.5 μsecs being marginal. This is caused by two effects. Firstly, the Disturbed Zero is measured at the time to the maximum of the Disturbed One output, which falls off rapidly as τ is decreased (Figure 6). Secondly, the actual magnitude of the output signal also increases since the Half-Selecting pulses become increasingly more effective

in disturbing the state of the core as the actual hysteresis loop traversed becomes smaller and smaller. As was mentioned previously the length of the Half-Selecting current pulses was kept a constant of 20 μsecs for measurement of the Disturbed Zero; thus greatly increasing the effective number of Half-Selecting current pulses for short values of Current Pulse Duration.

The First Half-Selected One, First Half-Selected Zero, First Delta and Second Delta output voltages were all measured with all current pulses in the test sequence having the same Current Pulse Duration (see Figures 9 to 11). All these voltages are defined in E-488, in which their importance concerning the use of cores in a coincident current memory is also explained. All of the above mentioned output voltages increase sharply at low values of Current Pulse Duration with τ = 1.5 μsecs again being marginal. The reasons for this are the same as those given for the similar increase of the Disturbed Zero for the same values of Current Pulse Duration.

It should be noted that pulse data was also taken for the Current Pulse Duration of 10 μs and was found in all cases to be identical with data taken at τ = 4 μs.

With reference to E-488, the worst output of a core containing a One in the memory or containing a Zero is as follows:

$$I_D - 2NS_1^1 - (n-2)\delta_2$$

and

$$O_D - 2NS_0^1 + 2\delta_1 + (n-4)\delta_2$$

where I_D = Disturbed One Output
O_D = Disturbed Zero Output
NS_1^1 = First Half-Selected One
NS_0^1 = First Half-Selected Zero
δ_1 = First Delta
δ_2 = Second Delta
n = Number of coordinate lines in memory plane

For the case where a Post-write Half-Selecting pulse is added to the writing sequence in a memory the corresponding worst conditions become:

$$I_D + 2NS_0^2 - n\delta_2$$

and

$$O_D - 2NS_0^2 + (n-2)\delta_2$$

where NS_0^2 is the Second Half Selected Zero
Since neither a NS_1^1 or a NS_0^1 are now not possible with each core in a disturbed state.

The Discrimination Ration (R_D) of a memory will be defined as follows for the case without a Post-Write Disturb.

$$R_D{}^U \equiv \frac{I_D - 2NS_1{}^1 - (n-2)\sigma_2}{O_D - 2NS_0{}^1 + 2\sigma_1 + (n-4)\sigma_2}$$

and for the case with a Post-Write Disturb

$$R_D{}^D \equiv \frac{I_D + 2NS_0{}^2 - n\sigma_2}{O_D - 2NS_0{}^2 + (n-2)\sigma_2}$$

$R_D{}^U$ and $R_D{}^D$ are shown in Figure 12 for a 32 x 32 array with NI_m = .950 amp turns and in Figure 13 for a 64 x 64 array with NI_m = .950 amp turns. In general the post-write disturb increases R_D by about a factor of 2. For the 64 x 64 array the R_D at 1.5 μs is increased from 2 to 3.5 which is still very low and R_D does reach a value of 8 until τ = 2.5 μs using the Post-Write Disturb pulse. Hence the expedient of breaking up a 64 x 64 plane into 4 - 32 x 32 sensing quadrants may become necessary if low values of Current Pulse are deemed necessary.

It should be noted that the pulse response obtained in this experiment is an average for 100 cores and as such the Discrimination Ratio calculated from these values is also an average value. Some distribution is to be expected about the mean value, therefore the Discrimination Ratio as calculated is optimistic to this extent.

Signed P. K. Baltzer
P. K. Baltzer

Approved DRB
David R. Brown

PKB/djd
A-54127
A-54128
A-54160
A-54109
A-54159
A-54110
A-54161
A-54111
A-54164
A-54165
A-54166
A-54172
A-54171

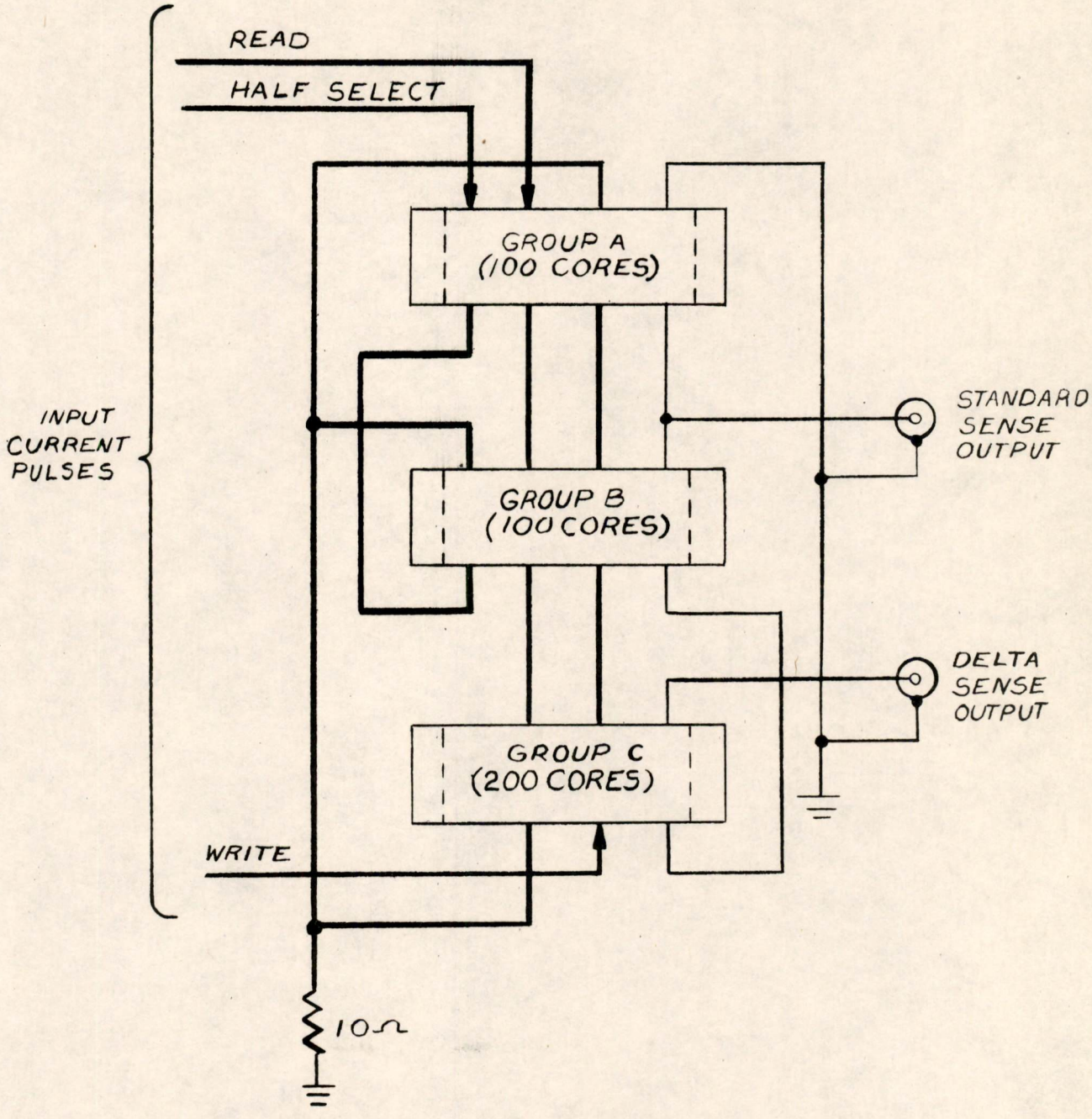


FIG. 1

TEST BOARD SCHEMATIC
FOR
DELTA MEASUREMENT

A-54127

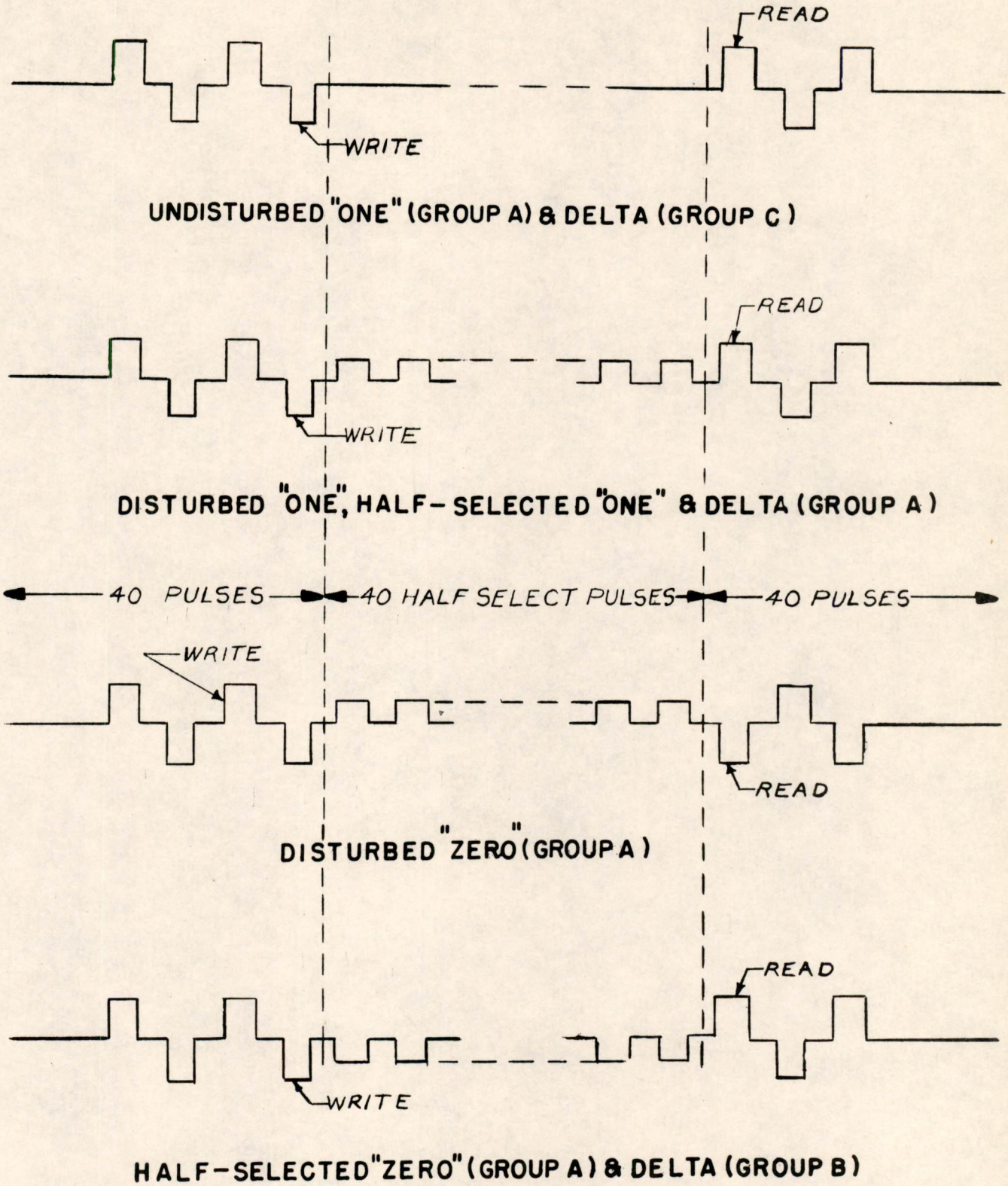


FIG. 2

INPUT CURRENT PULSE SEQUENCE

A-5412

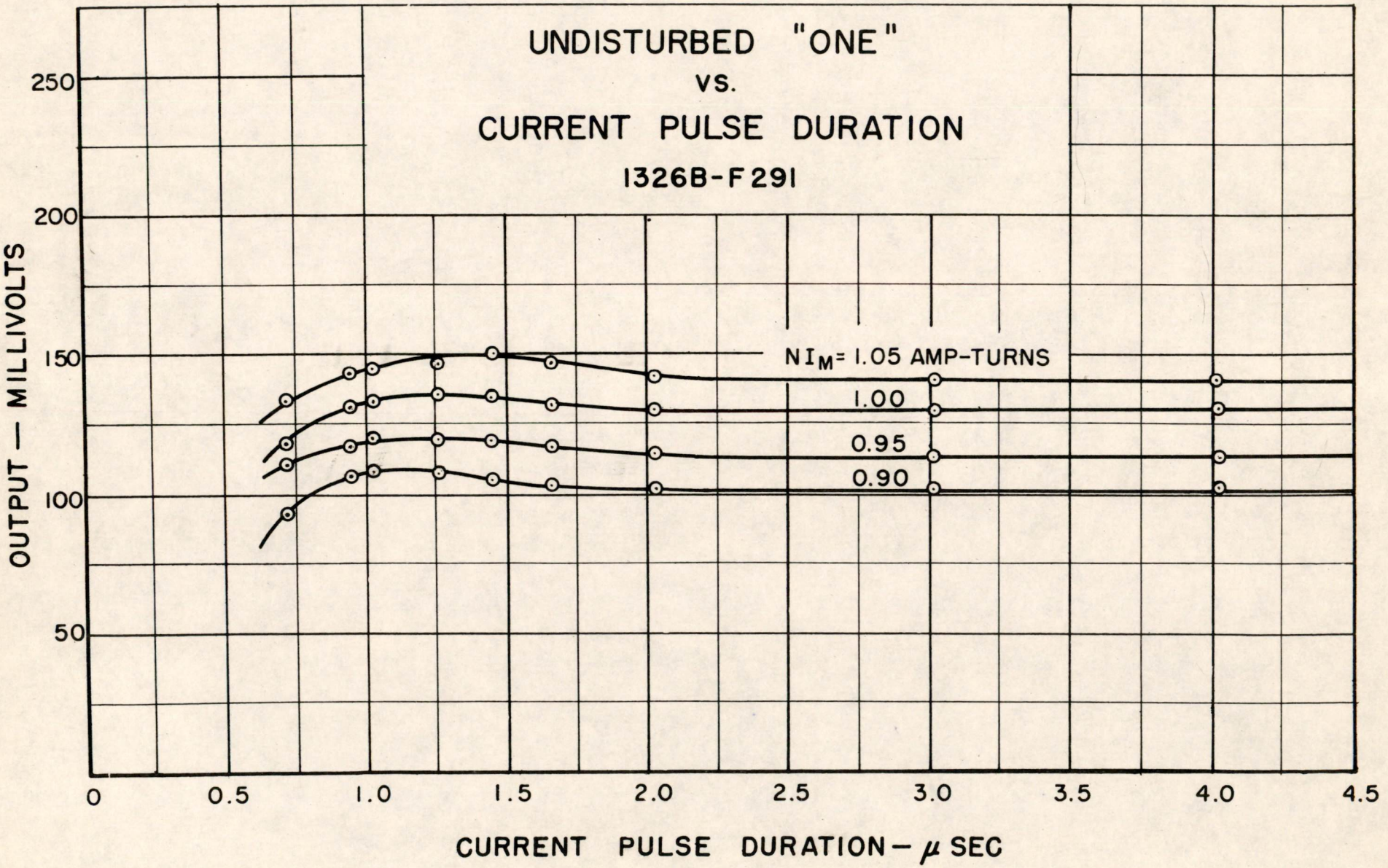
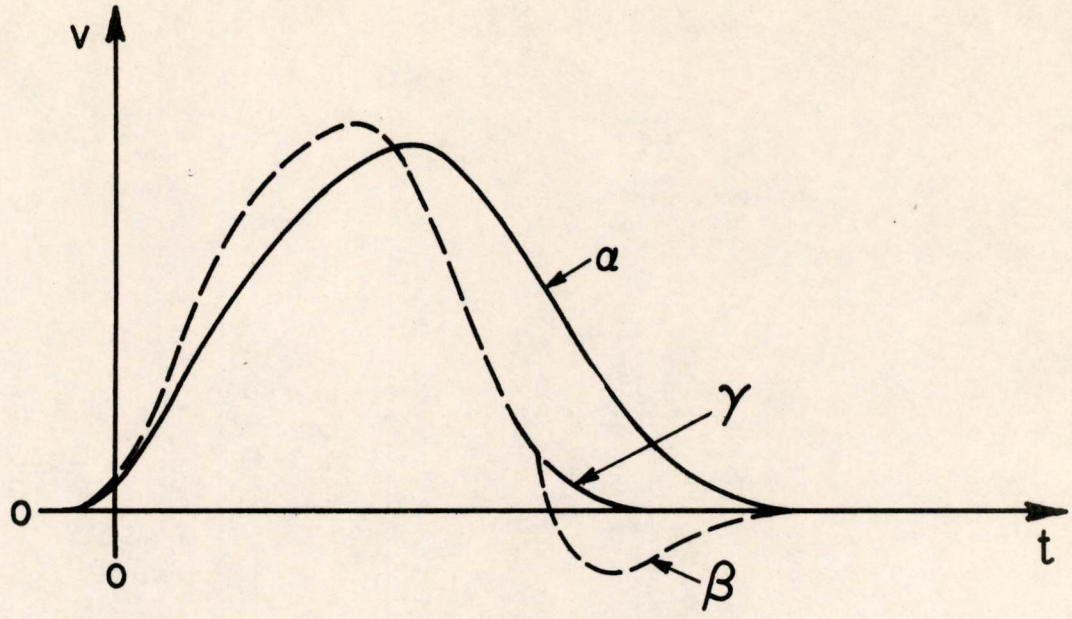
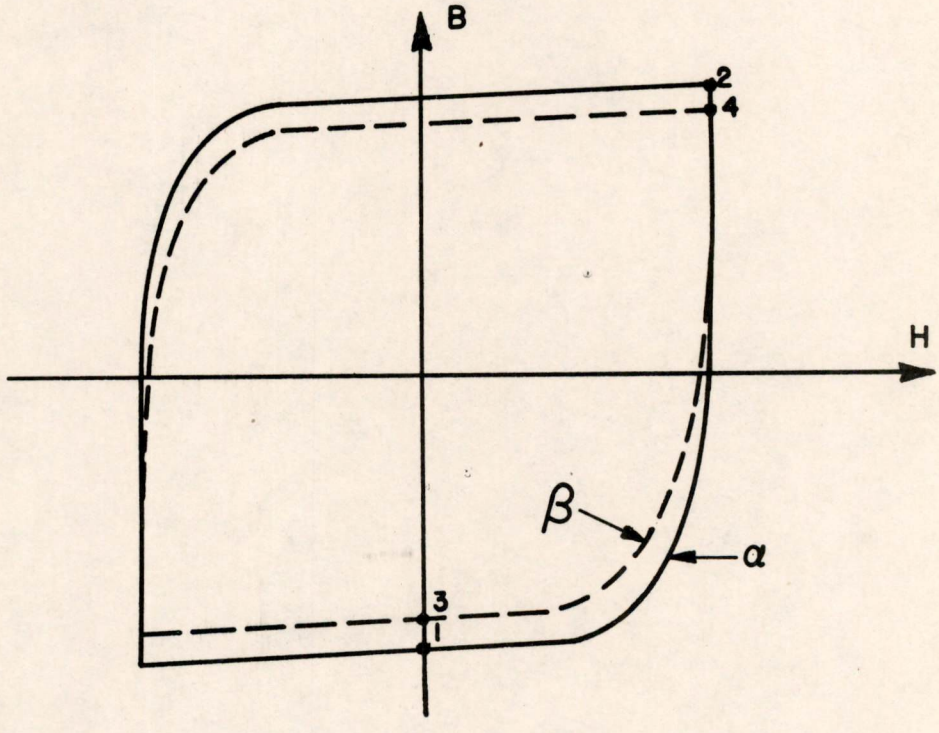

UNDISTURBED "ONE"
vs.
CURRENT PULSE DURATION
1326B-F291
NI_M = 1.05 AMP-TURNS
1.00
0.95
0.90
OUTPUT — MILLIVOLTS
250
200
150
100
50
0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
CURRENT PULSE DURATION — μ SEC

FIG. 3



TYPICAL UNDISTURBED "ONE" OUTPUT



TYPICAL DYNAMIC HYSTERESIS LOOP

FIG. 4

A-54109

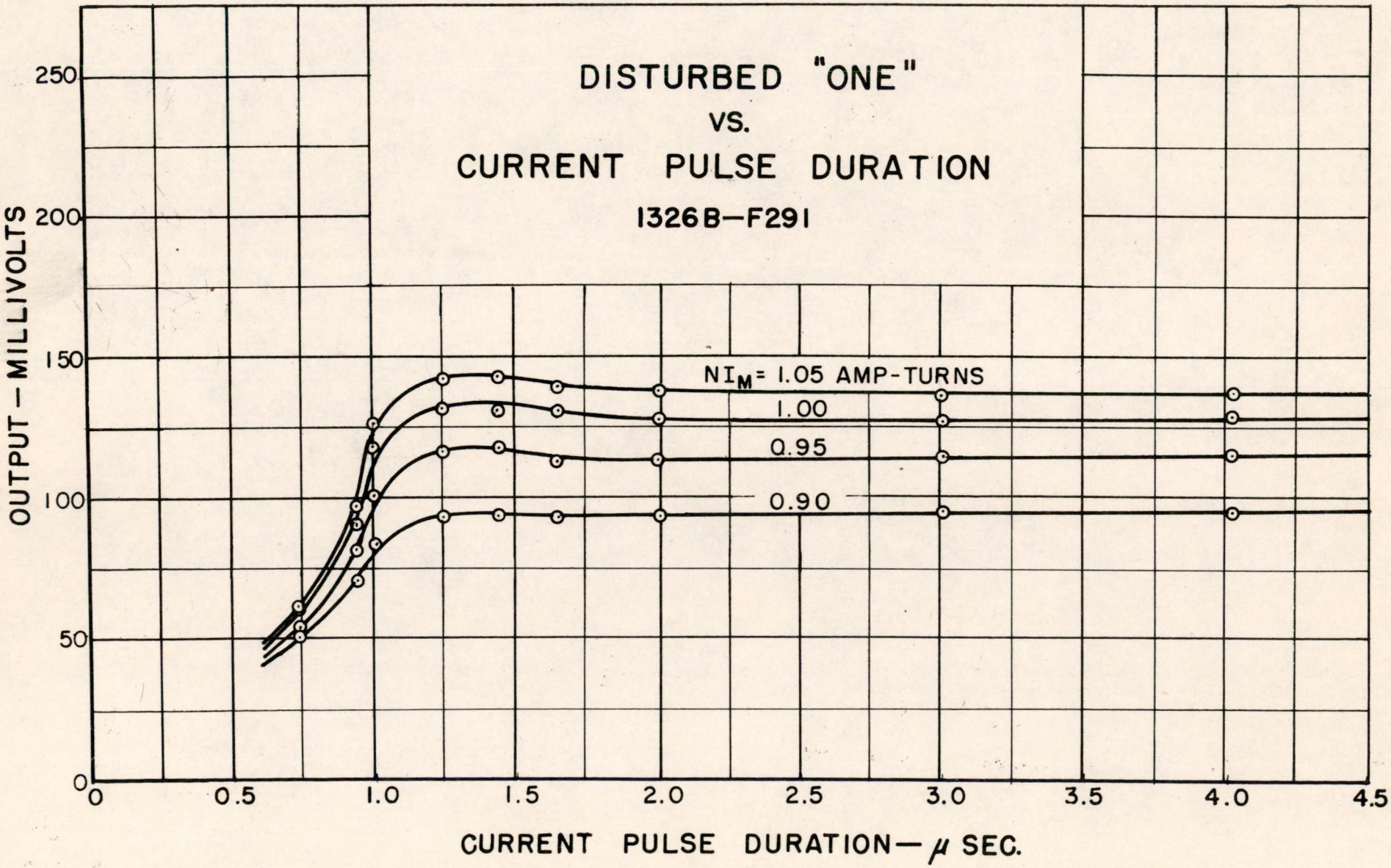

DISTURBED "ONE"
VS.
CURRENT PULSE DURATION
1326B–F291
OUTPUT – MILLIVOLTS
250
200
150
100
50
0
0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
CURRENT PULSE DURATION – μ SEC.
NI_M = 1.05 AMP-TURNS
1.00
0.95
0.90

FIG. 5

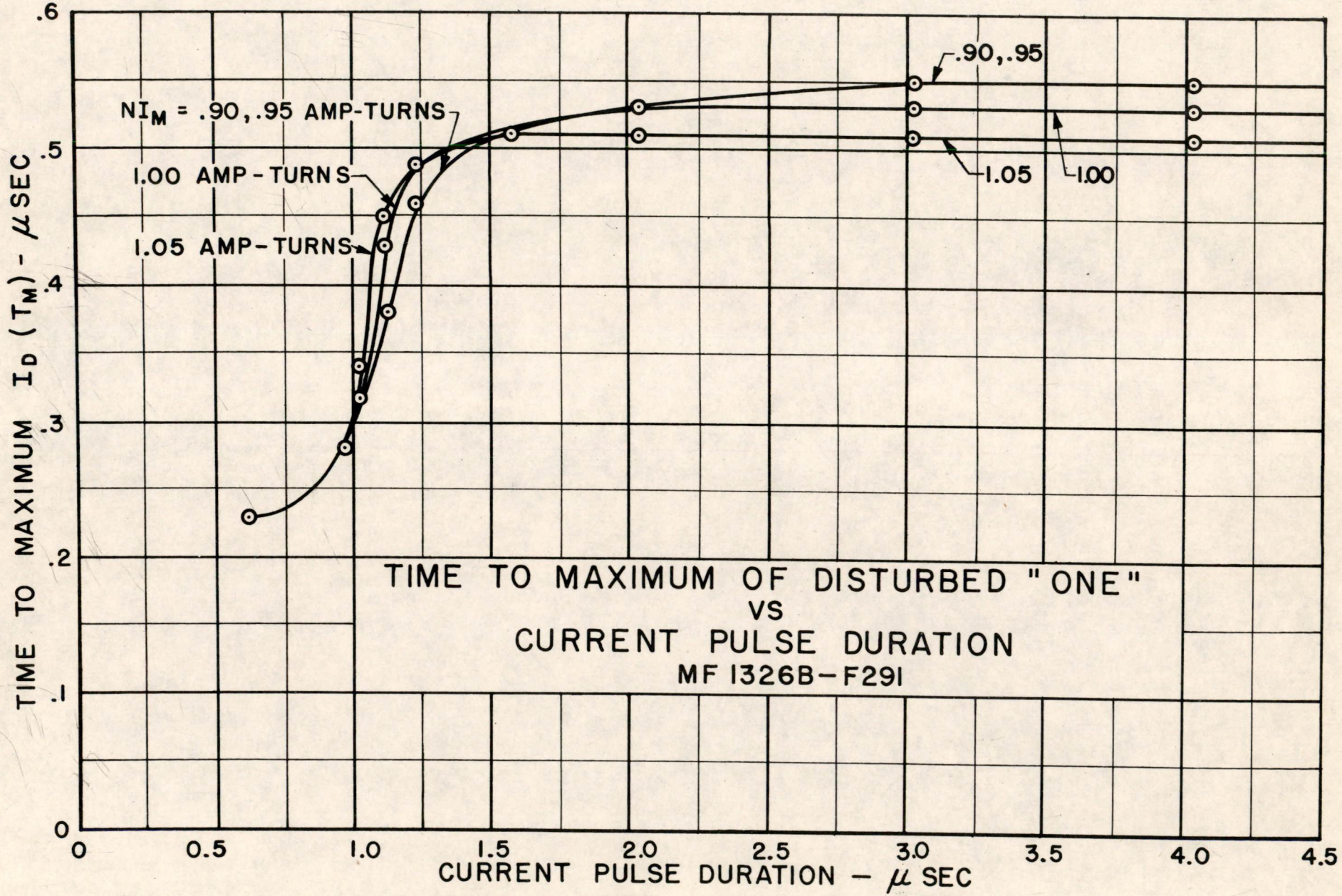

.6
.5
.4
.3
.2
.1
0
TIME TO MAXIMUM I_D (T_M) - μSEC
NI_M = .90, .95 AMP-TURNS
1.00 AMP-TURNS
1.05 AMP-TURNS
.90, .95
1.05
1.00
TIME TO MAXIMUM OF DISTURBED "ONE"
VS
CURRENT PULSE DURATION
MF 1326B-F291
0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
CURRENT PULSE DURATION - μ SEC

FIG. 6

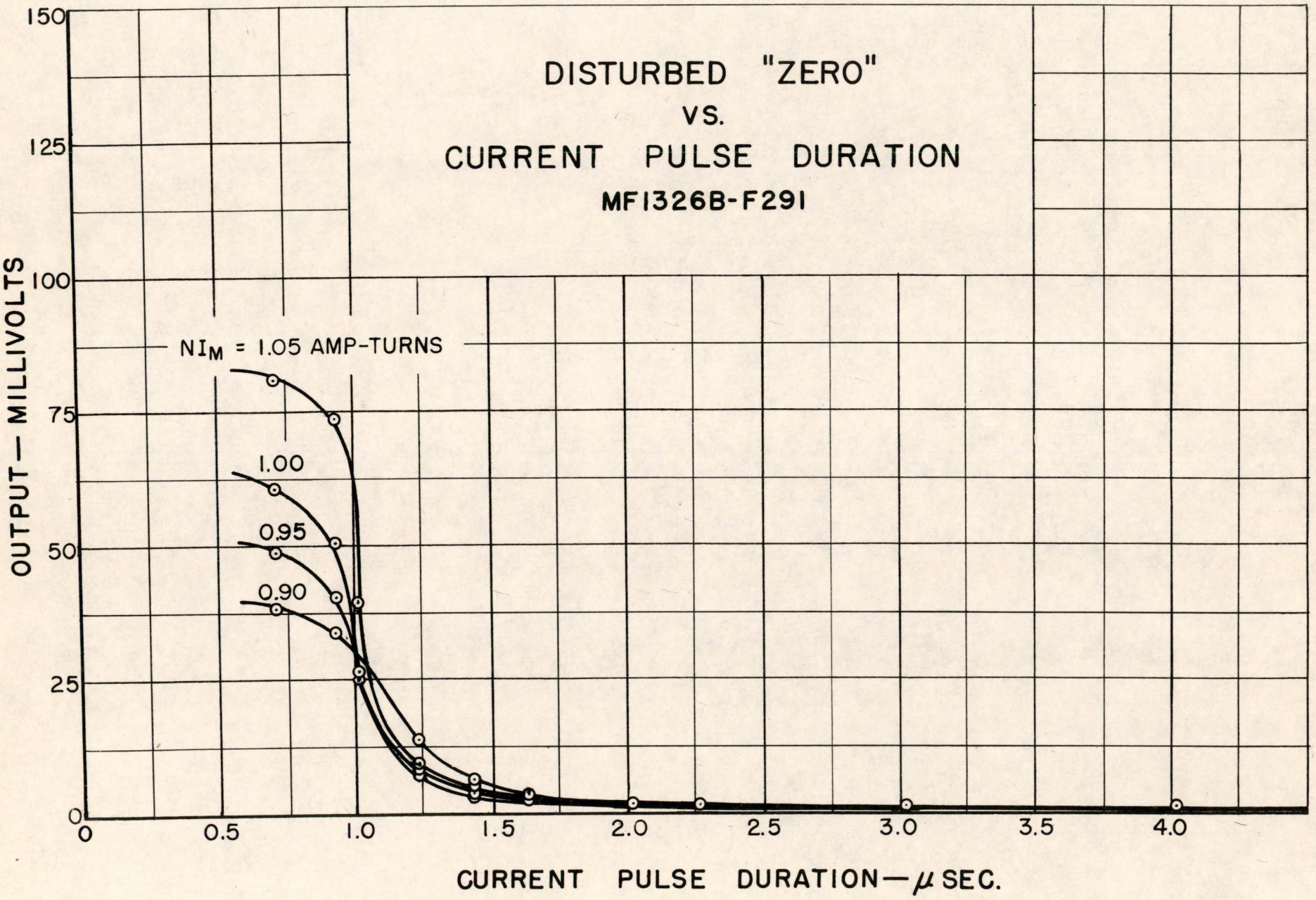

DISTURBED "ZERO"
VS.
CURRENT PULSE DURATION
MF1326B-F291
NIM = 1.05 AMP-TURNS
1.00
0.95
0.90
OUTPUT — MILLIVOLTS
150
125
100
75
50
25
0
0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
CURRENT PULSE DURATION — μ SEC.

FIG. 7

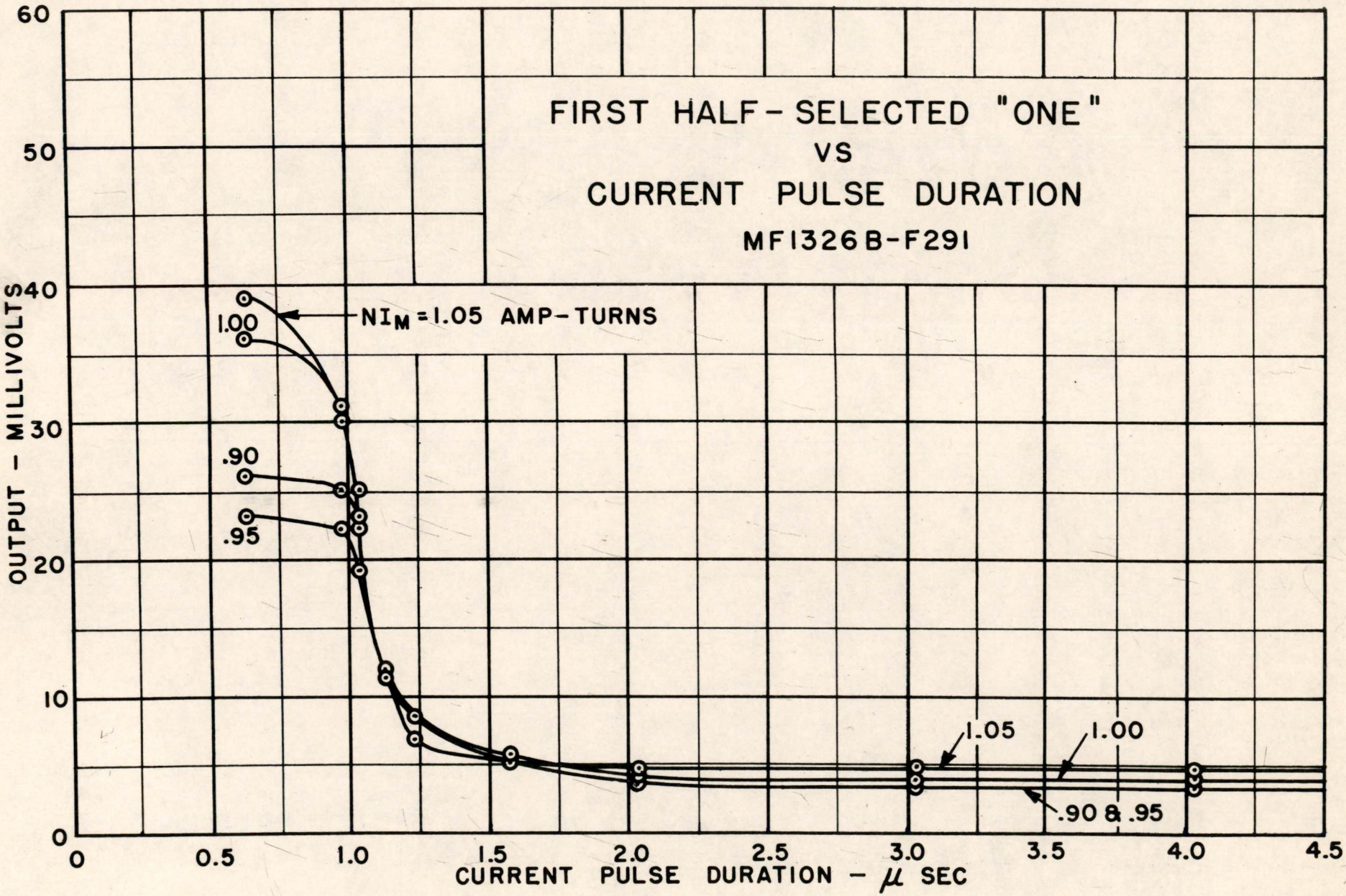

FIRST HALF-SELECTED "ONE"
VS
CURRENT PULSE DURATION
MF1326B-F291
NIM = 1.05 AMP-TURNS
1.00
.90
.95
1.05
1.00
.90 & .95
OUTPUT - MILLIVOLTS
CURRENT PULSE DURATION - μ SEC
0
10
20
30
40
50
60
0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5

FIG. 8

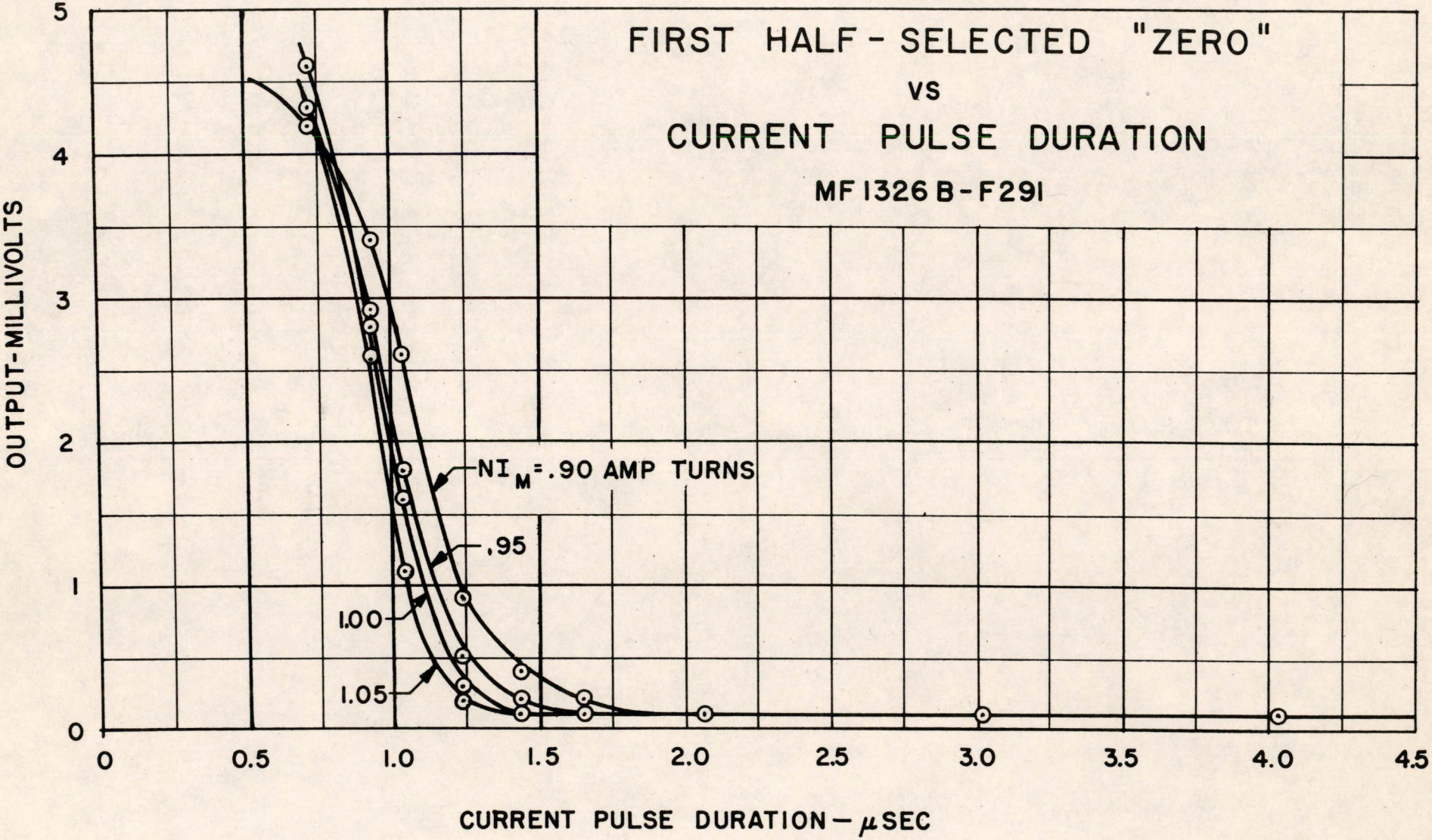

FIRST HALF-SELECTED "ZERO"
VS
CURRENT PULSE DURATION
MF1326B-F291
OUTPUT-MILLIVOLTS
CURRENT PULSE DURATION — μSEC
NI M = .90 AMP TURNS
.95
1.00
1.05
0
1
2
3
4
5
0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5

FIG. 9

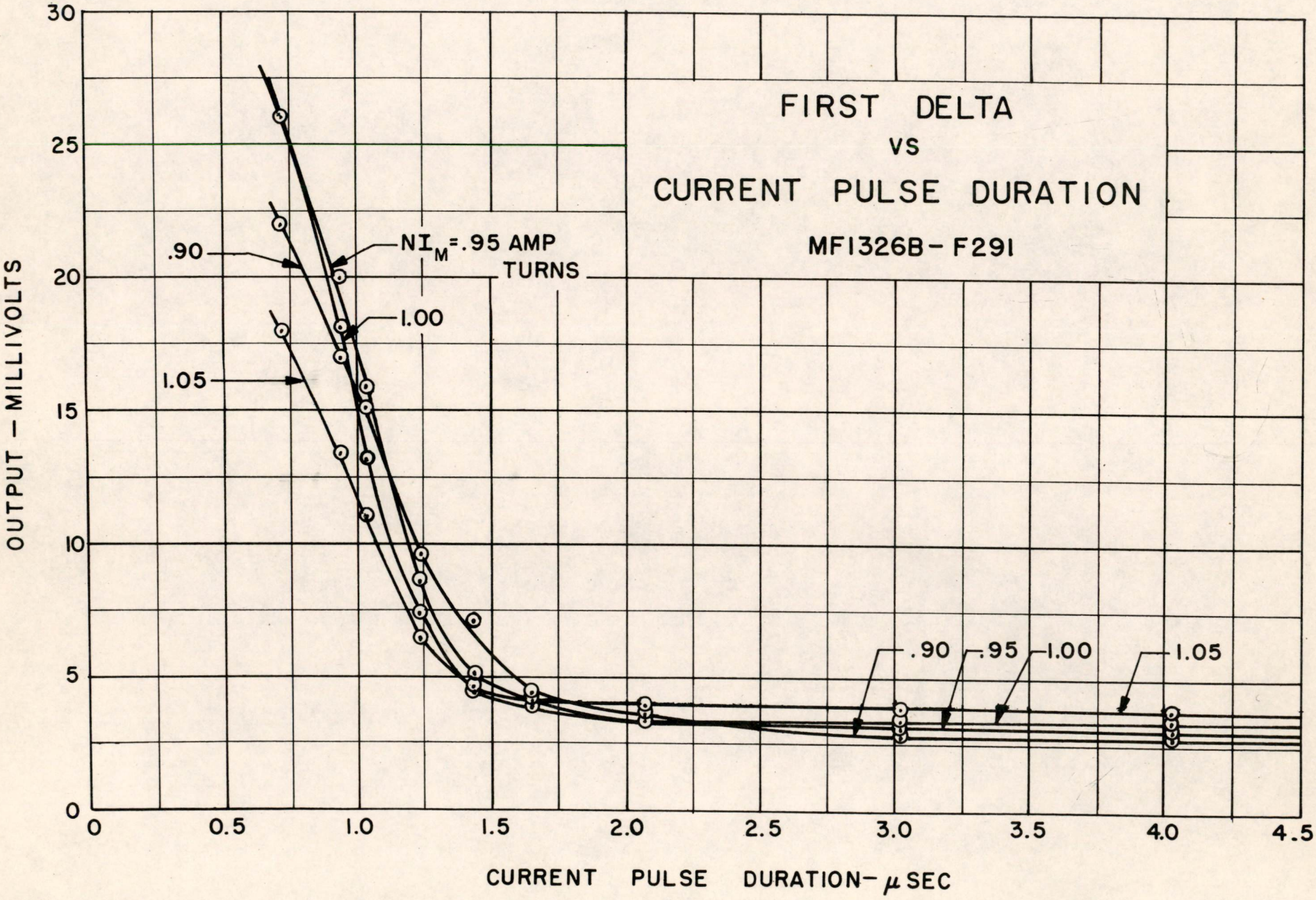

FIRST DELTA
VS
CURRENT PULSE DURATION
MF1326B-F291
NI$_M$=.95 AMP TURNS
.90
1.00
1.05
.90
.95
1.00
1.05
OUTPUT — MILLIVOLTS
CURRENT PULSE DURATION — μSEC
0
5
10
15
20
25
30
0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5

FIG. 10

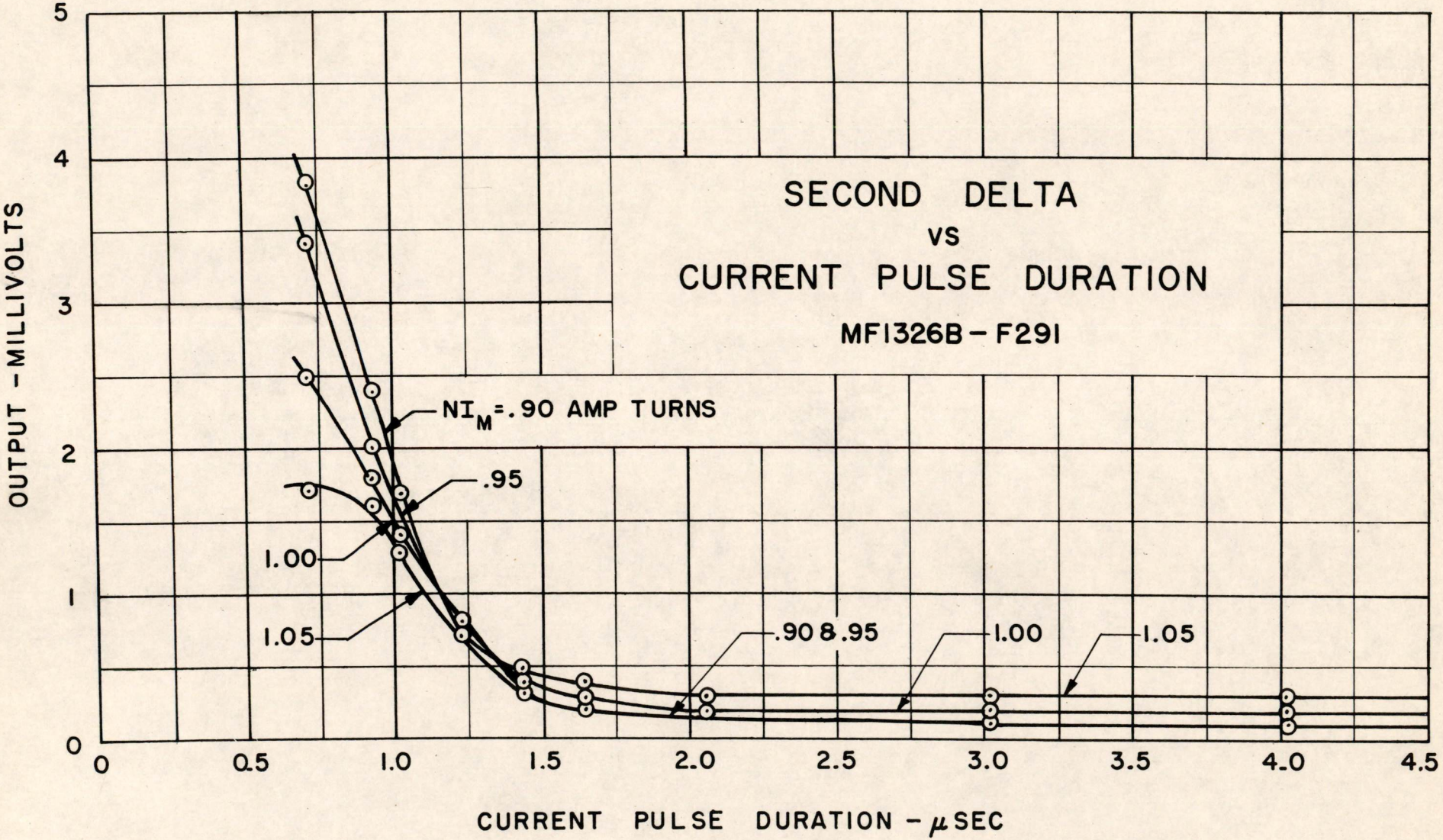

SECOND DELTA
VS
CURRENT PULSE DURATION
MF1326B-F291
NI$_M$=.90 AMP TURNS
.95
1.00
1.05
.90 & .95
1.00
1.05
OUTPUT - MILLIVOLTS
CURRENT PULSE DURATION - μSEC
0
1
2
3
4
5
0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5

FIG. 11

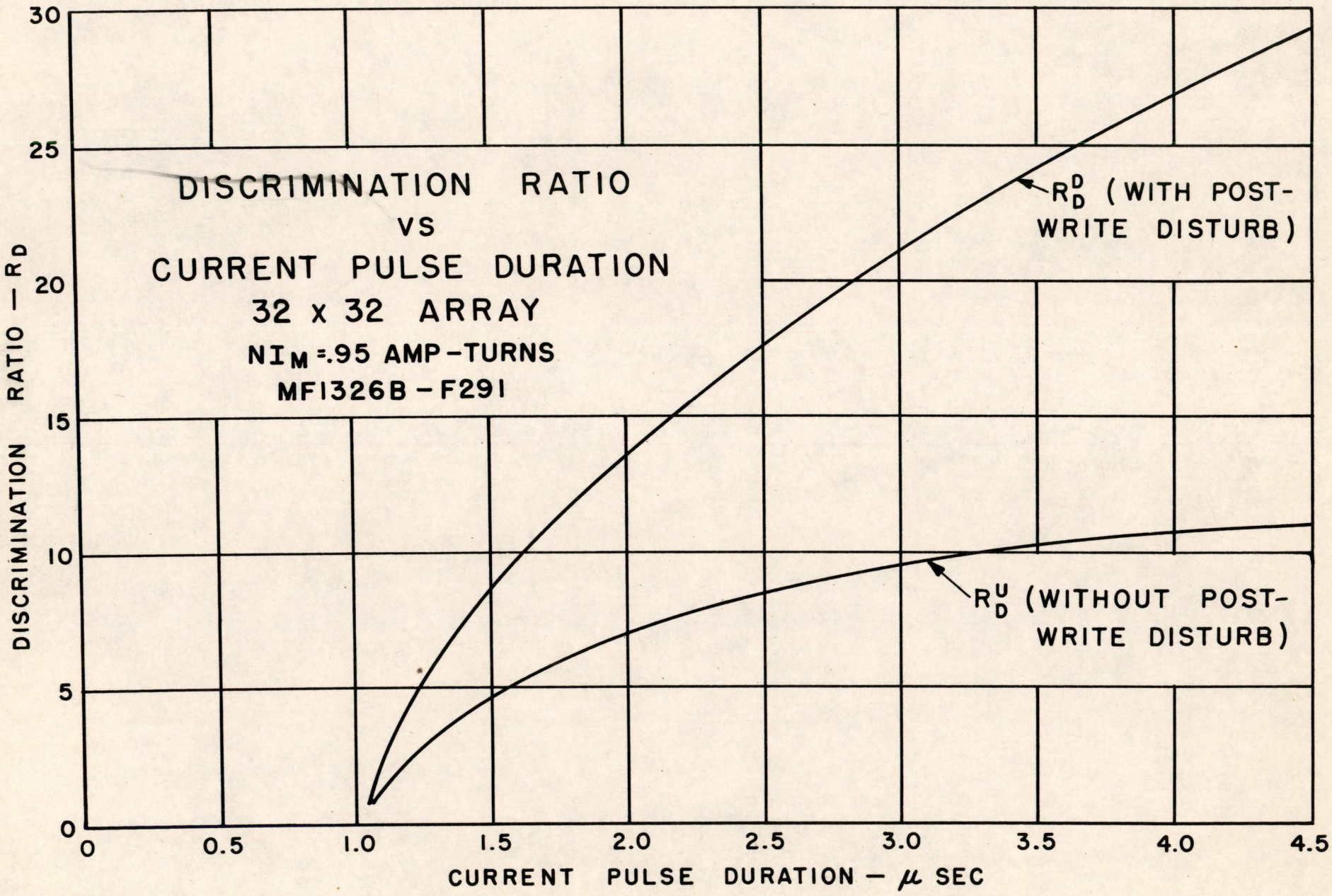

DISCRIMINATION RATIO
VS
CURRENT PULSE DURATION
32 x 32 ARRAY
NI M =.95 AMP-TURNS
MF1326B-F291
R_D^D (WITH POST-WRITE DISTURB)
R_D^U (WITHOUT POST-WRITE DISTURB)
DISCRIMINATION RATIO — R_D
CURRENT PULSE DURATION — μ SEC
0
5
10
15
20
25
30
0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5

FIG. 12

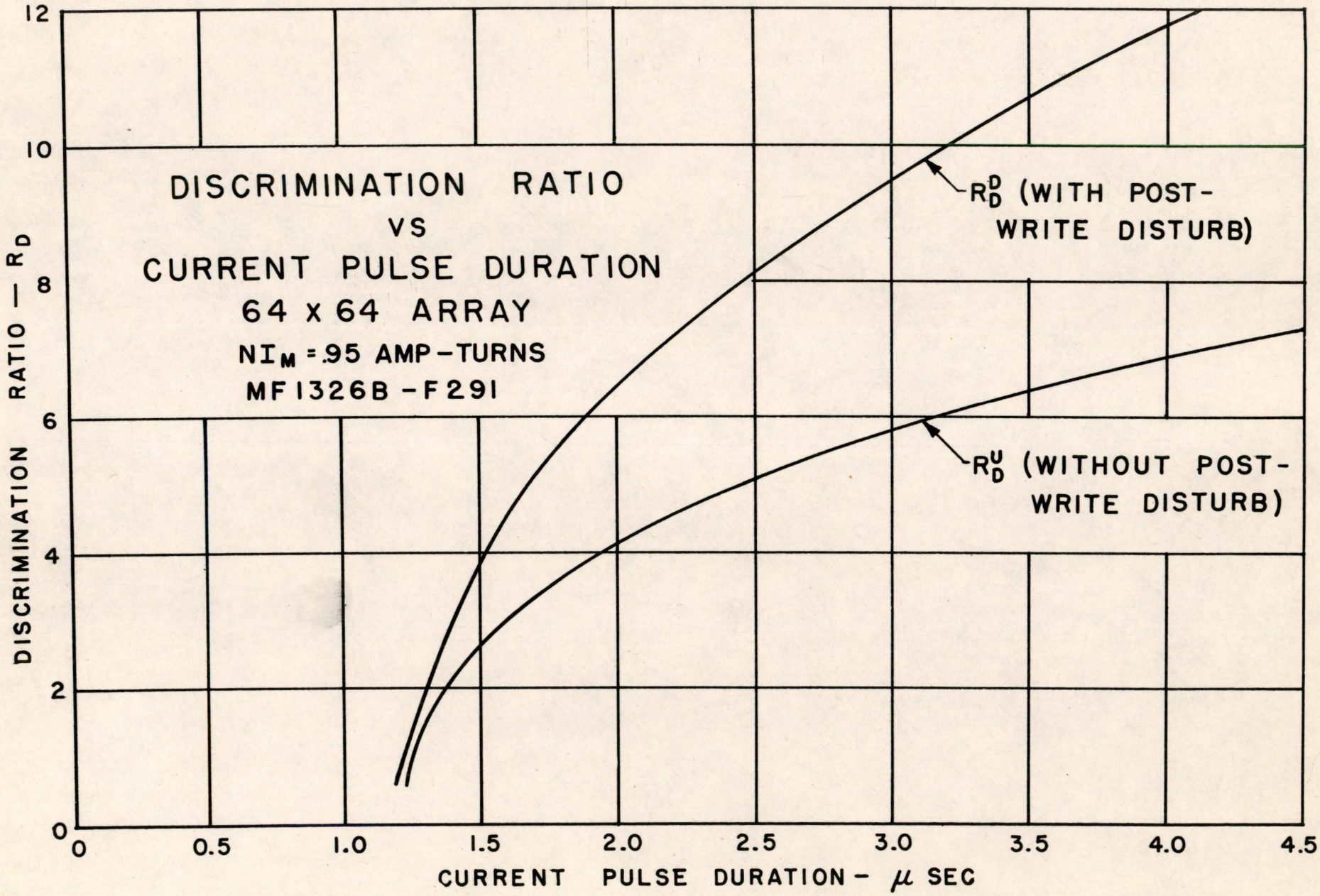

DISCRIMINATION RATIO
VS
CURRENT PULSE DURATION
64 x 64 ARRAY
NI_M = .95 AMP-TURNS
MF1326B-F291
R_D^D (WITH POST-WRITE DISTURB)
R_D^U (WITHOUT POST-WRITE DISTURB)
DISCRIMINATION RATIO — R_D
CURRENT PULSE DURATION - μ SEC
0
2
4
6
8
10
12
0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5

FIG. 13

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: A FAST CORE-TUBE REGISTER

To: Norman H. Taylor

From: Kenneth H. Olsen, R. Pfaff

Date: April 27, 1953

The circuit to be described was developed for use in MTC, but was not used for lack of time. Its purpose is to serve as temporary storage thus taking the place of a flip-flop and two gate tubes.

A circuit diagram is given in Figure 1. The core of T_1 is a square-looped material. V_1 is used to write information into the core when hit by a "write" pulse. V_2 is used to read the information contained in the core. If a "1" is contained in the core a positive pulse appears at the output. If the core contains a zero, a small negative pulse appears at the output. Without the compensating network, R_1 and L_1, a "0" in the core would produce a small positive output. However, the effect of this compensating network is to subtract a small pulse from both the "1" and "0" output pulses. The "1" output is slightly reduced but "0" output is completely cancelled out. In fact, the "0" output may be slightly negative.

Figure 2 gives experimental results for the circuit shown in Figure 1. The output was photographed while "0's" and "1's" were read in and out alternatively. The photograph was then traced on the drawing. Many extensions and variations of this basic circuit are possible.

Signed K. H. Olsen
K. H. Olsen

R. Pfaff
R. Pfaff

Approved
N. H. Taylor,
Group Leader

KHO/RP:jrt

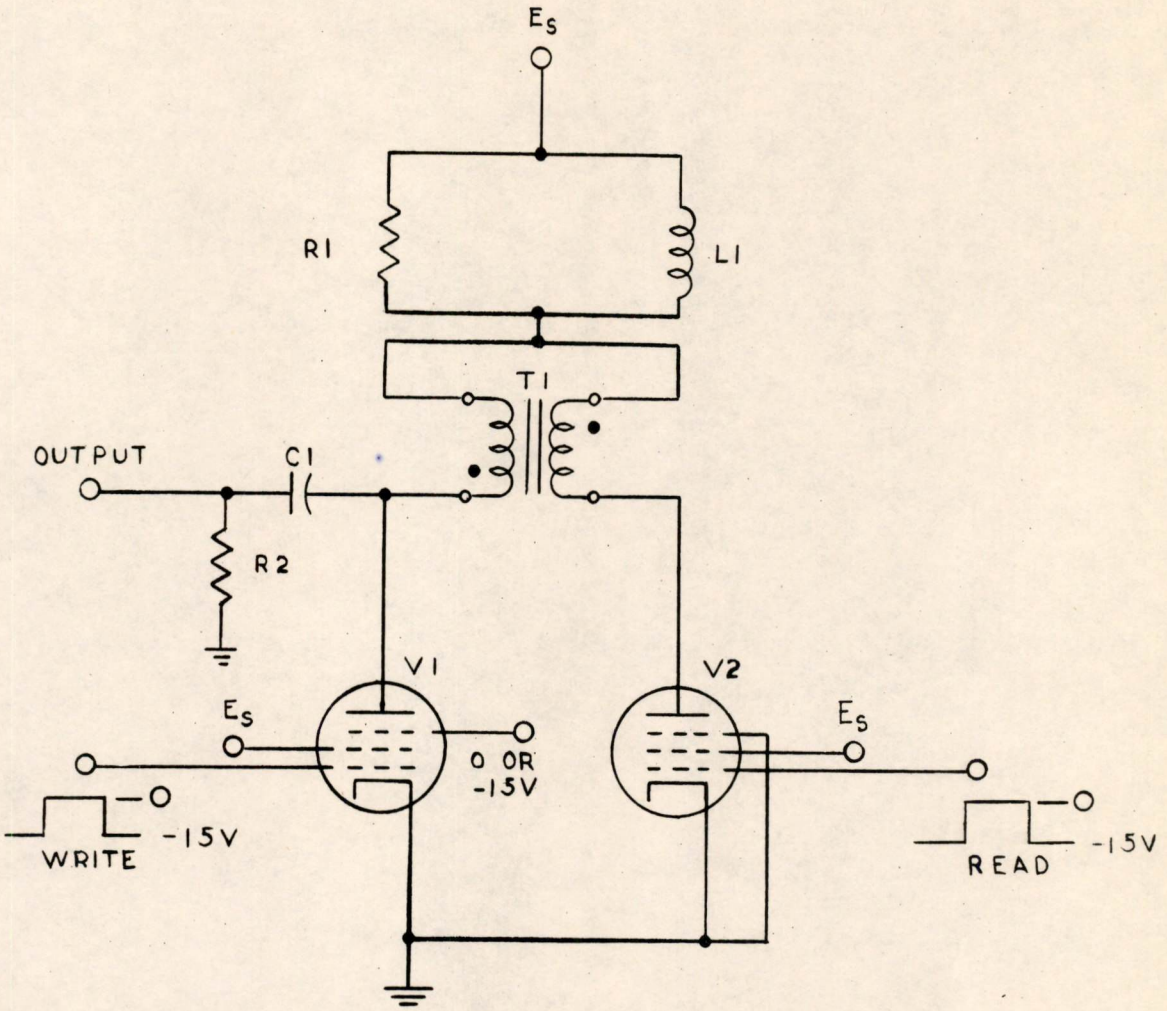
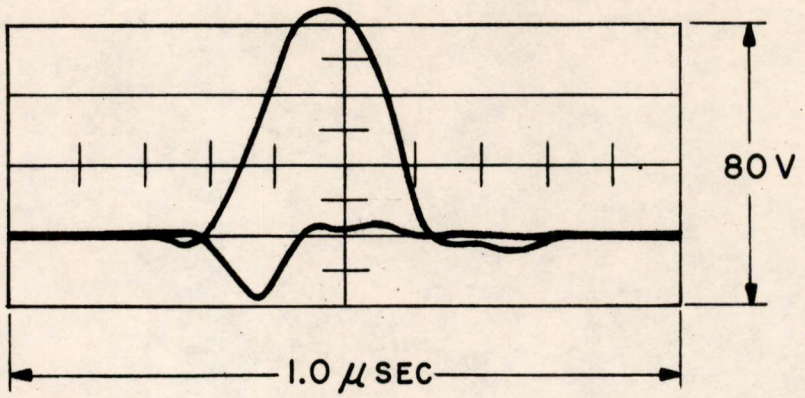


FIG. 1

A FAST CORE—TUBE REGISTER

A—54763



V_1, V_2 = 7AK7

T_1 = 1/4 MIL, MO-PERMALLOY, 40 WRAP TOROID; 1/8" BOBBIN, EACH WINDING 30 TURNS.

R_1 = 1000Ω

R_2 = 100 K

L_1 = 56 μH

C_1 = 56 MMFD

E_s = 250 V

READ AND WRITE PULSES 15V, 0.4 μ SEC WIDE.

FIGURE 2

EXPERIMENTAL RESULTS

A-54807

Olsen

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: TIMING DIAGRAMS FOR MTC CONTROL

To: N. H. Taylor

From: R. C. Hopkins

Date: May 5, 1953

Abstract: Memory Test Computer control is of the circulating pulse type. Newly conceived timing diagrams which show flow of pulses through control and the resultant register contents are given for program timing and for each possible operation. The diagrams are designed primarily to permit an easily understandable explanation of control operation and, secondarily, to assist to a limited degree in trouble shooting and to serve as a simple traffic diagram.

1. Introduction

1.1 The Memory Test Computer control is built up of standard test components along with a few special panels specifically designed for MTC. Since MTC is primarily intended as a testing unit for the magnetic memory, design has stressed maximum use of available components and circuits and simplicity of logic. Sufficient flexibility has been achieved to permit necessary variety of test programs and the inclusion of additional instructions, if required. Operations and coding are described in Memorandum M-1881-1. A block diagram of MTC Control is contained in sketch SD-37376.

1.2 The need was felt for a combination timing diagram, pulse flow chart and traffic diagram which would outline in a simple and easily understandable form the logical operations of the computer. To that end, the attached diagrams were designed. Preliminary experience with the diagrams has demonstrated their helpfulness in permitting easily understandable explanations of control logic and operation and, for certain types of faults, in quickly locating the general area of trouble. It is anticipated that elapsed times will also be useful to those planning to run the computer as a test device. The diagrams are particularly addressed first, to the relatively inexperienced person as an introduction to the operation and logical design of MTC Control in particular and as an example of logical design of computer control in general; second, to the experienced person who is not working with MTC or who is new to this computer and who desires a quickly-acquired understanding of its logical design; and third, to those of higher echelons who desire to have at hand a quick reference or reminder of MTC logical design.

2. General Description

2.1 The diagrams include only those logical elements of control and the CPO lines which are concerned in each operation. Possible alternate pulse paths which may be called for by other than the operation portion of the instruction are shown where applicable. A pulse flow chart of the block diagram type appears on the left of the diagram and the contents of the significant registers, counters, and switches, along with elapsed time, are tabulated on the right. Actual elapsed times are not given in the diagrams since delays have not, in all cases, been permanently determined. It is expected that the elapsed times will be given from actual measurements rather than from calculations. It was not possible, before elapsed times were measured and delays permanently established, to adhere to exact chronological order in each detail of the operation. This can be adjusted after timing measurements have been made. The charts do, however, permit a realistic estimate of elapsed times.

2.2 In the pulse flow chart, broken circles joined at the break by the straight lines indicating the pulse path are used to designate time delays. The magnitude of the delay is given in microseconds within the broken circle. Where a Greek letter is used instead of a number, it indicates a variable delay, the magnitude of which has not been finally determined. In this case present value or probable order of magnitude of the delay is given in parenthesis adjacent to the symbol.

2.3 The rectangular boxes on the pulse flow chart indicate that the actions indicated therein occur simultaneously and that the CPO lines, indicated by the numbers in parenthesis, connect at that point in the "logical" circuit. The dotted timing line which leads to the tabulations on the right is placed at the top of the block of operations concerned and applies to all within the box.

3. Explanatory Comments on each Diagram

The diagrams are largely self-explanatory; however, brief comments are given below where clarification seems desirable.

3.1 Start Over and Program Timing (SB-54412-5). The upper part of the chart down to "Restart" is concerned only when "Start Over" is used. The "Start Over" button is used to initiate a program or start it over from the beginning. The "Restart" button will start the computer at any point of the program at which it was interrupted. Thus the "Restart" permits cycling through a program one-half instruction at a time whenever the "Half Instruction" switch is thrown and the return pulse is thus interrupted. Only one-half of an instruction is performed at a time in this case since the control pulse must circulate through control twice for each instruction: once for program timing, and once for operation timing.

3.1.1 An arrangement is included which employs a low frequency pulse generator to start over the computer automatically at a given repetition frequency in the event of computer inactivity before the repetition period expires. This permits the running of programs over and over at a given frequency. Connection to a synchronizing source is also provided to facilitate signal tracing and trouble shooting.

3.1.2 An arrangement shown in the lower portion of the diagram permits an automatic display on the memory oscilloscope wherein the address in the memory switch is displayed depending upon whether or not there is a "one" in a selected digit of the number stored at that address. This is used only when operation timing is suppressed and works as follows: the stored number is read into the A-Register from the memory address indicated by the program counter. A given digit of the A-Register is selected (this actually selects a memory plane) to control the gates connected to CPO lines 177 and 178. Thus if a "one" occurs, a spot will be displayed at the appropriate address location on the scope. If a "zero" occurs, no spot is displayed. For normal operation both the "zero" and the "one" selection gates are "off". It is seen that this arrangement makes it possible to display the contents of a selected memory plane in a raster on the memory scope. One should note that when operation timing is suppressed, the gate controlled by CPO line 106A is "on" and that controlled by 106B is "off". FX is hence held in the "one" position.

3.2 Halt (SB-54413-5). This operation is very similar to program timing with the exception that the first flip-flop of the control switch (FO) is not complemented until too late for the end return pulse to pass through. During an operation cycle the flip-flop FX is in the "one" position and the gate controlled by the "zero" side is therefore "off", and FO is hence not complemented where it was during program timing. Thus the pulse circuit is broken at the gate controlled by the "one" side of FO, and an end return is prevented.

3.3 Display (SB-54421-4). This order displays on the scope a point whose abscissa is contained in the left 10 digits of the A-Register and whose ordinate is contained in the left 10 digits of the Accumulator. The decoders (digital to analog converters) for the respective registers are permanently connected to the deflection system of the scope. Thus for a display of the point it is necessary only to furnish an "intensify" pulse to the scope tube.

3.4 Identity Check (SB-54568-3). The identity check provides a pulse for test or alarm and adds one to the program counter if the quantity in the Accumulator is not identical to the number chosen from one of the storage registers. In addition, the Accumulator will retain "one's" in those digits where the two numbers are not identical.

3.5 Store (SB-54459-2). It may be seen that the read portion and its associated parity check of this operation have no significance, but are retained in the cycle for the sake of uniformity and simplicity in design of control.

3.6 Replace Address (SB-54476-2). This instruction extracts a number from storage and, while in the A-Register, replaces the right 11 digits of that number with the right 11 digits of the number in the Accumulator. It is then replaced in its memory register.

3.7 Clear and Add, and Add (SB-54480-2 and SB-54487-2). It will be noted that these two operations are identical with the exception that in the latter the gate controlled by the "zero" side of control switch flip-flop F4 is "off", and hence the Accumulator is not cleared before it is read into. Addition is accomplished in the conventional manner of reading into the Accumulator on its complement line and using a carry register.

3.8 Clear and Subtract, and Subtract (SB-54500-2 and SB-54524-2). In MTC the subtract operation is performed in a round-about fashion since the A-Register is complemented only for marginal checking purposes and not during any control operations. Thus for clear and subtract, the number is added into the cleared Accumulator and there complemented. In order to effect a subtraction the minuend in the Accumulator is first complemented. The subtrahend in the A-Register, which has been read from a storage register, is added and the Accumulator is again complemented. Thus we accomplish a subtraction by adding the subtrahend to the negative of the minuend and complementing the result. $N_1 - N_2 = - (-N_1 + N_2)$.

3.9 Transfer (SB-54529-2). This operation merely changes the number in the program counter from what it would normally be to the number given in the address portion (right 11 digits) of the instruction.

3.10 Transfer/Pulse (SB-54530-2). This operation is identical to the previous one with the exception that a test or alarm pulse is provided in the cycle.

3.11 Transfer on Negative (SB-54540-2). This operation is similar to Transfer--the address portion of the instruction is read into the program counter--with the exception that the pulse has only one path through which it can clear the program counter and add in the address. This path is through a gate controlled by the "one" side of the first flip-flop (AC0) of the Accumulator. Thus transfer will occur only when the number in the Accumulator is negative.

3.12 Transfer on Negative/Pulse (SB-54541-2). Here again the operation is identical to the previous one except a test or alarm pulse is provided in the cycle.

3.13 Memory Address Display (SB-54539-1). This is the simplest of all operations since the abscissa and ordinate of the memory scope are permanently connected to decoders on the memory address switch. All that is necessary therefore, is to intensify the memory scope after reading into the memory address switch the appropriate address included in the instruction.

3.14 Cycle Right (SB-54564-1). In this operation the right 5 digits of the instruction signify the number of times the Accumulator and B-Register will be cycled. This number is read into the step counter (as is the case on all operation cycles) and one is then subtracted from the step counter for each shift accomplished until an end-return pulse is obtained from the step counter when it reaches zero. The CR→AC pulse on CPO 33 reads the right-end digit of the B-Register into the left-end digit of the Accumulator. If the first digit of the address is a "one" the B-Register is cleared after the cycle is completed.

3.15 Shift Right (SB-54565-1). This operation is exactly like the preceding one except the right end digit in the B-Register is not read into the left end digit of the Accumulator. Hence the digits shifted out of the right end of the B-Register are lost.

3.16 Print (SB-54566-1). This operation includes provision for first cycling right the number of times specified in the right 5 digits of the instruction. This is provided in order that the number to be printed may be positioned properly for being read out of the right 6 digits of the Accumulator into the output register and hence into the Flex-o-writer or other read-out device. It will be noted that the operation proceeds exactly as the cycle right operation except that a read-out-and-print pulse is furnished the output equipment and an end-return pulse is obtained when the print operation is completed.

3.17 Read In (SB-54567-1). In this case the contents of the input register, which receives the output of the Flex-o-writer or other read-in equipment, is read into the right 6 digits of the B-Register. After an end-return pulse is obtained from the input equipment, AC and BR are cycled right the number of positions indicated in the address portion of the instruction.

4. General Explanatory Comments

4.1 End-Return Pulses. It will be noticed that all operations of the type that may involve reading out of and/or writing into magnetic memory require two end-return pulses. On diagrams for Store and Replace Address this may not appear immediately evident since one of the end return pulses is lumped together with AR Parity count simply as a "Complement FO" pulse. The double-end-return system was adopted in order that, regardless of length of time required for write into the memory, other actions could be taken simultaneously without fear of proceeding to the next instruction before a portion of the operation was completed. Hence when a portion of the operation is performed simultaneously with writing

into storage, the write operation furnishes an end pulse and the other portion furnishes another end pulse. The first pulse to reach the gate controlled by the "one" side of F0, through which the end pulse returns to the beginning of the next cycle, cannot pass through the gate but complements F0 in order that the next pulse may pass through and act as the end return. This system increases considerably the flexibility of the computer as a memory tester and, at the same time, saves time on the operations involved.

4.2 Parity Count and Parity Check. A seventeenth digit in the A-Register and the Memory registers is used for a simple rough check as to whether the number read out of a given memory register is probably the same as that written into the register. A one is used in this 17th digit to indicate that the 16-digit number in the register contains an even number of ones. A zero indicates an odd number of ones. The parity count to determine the 17th digit is made in the A-Register.

4.2.1 When a number is read out of memory, a parity count is made in the A-Register. If the resulting 17th digit is not identical with the one read out of memory, an alarm is given upon Parity Check and the computer is stopped.

4.2.2 It may be noticed that a parity count and check are made for each operation involving reading from storage, immediately after read-out is completed. If the number to be read into storage is different from the one which was read out, as in the cases of Store and Replace Address, another parity count is made just before writing into storage in order that the correct parity indication will be stored in the 17th digit.

Signed R.C. Hopkins
R. C. Hopkins

Approved K Olsen

RCH:jrt

Diagrams attached :

SD-37376	SB-54480-2	SB-54541-2
SB-54412-5	SB-54487-2	SB-54539-1
SB-54413-5	SB-54500-2	SB-54564-1
SB-54421-4	SB-54524-2	SB-54565-1
SB-54568-3	SB-54529-2	SB-54566-1
SB-54459-2	SB-54530-2	SB-54567-1
SB-54476-2	SB-54540-2	

SD-37376

117 ← DISTURB GATE
116 ← WRITE GATE MINUS
118 ← WRITE GATE PLUS
115 ← READ GATE
70A ← MEMORY READ OUT
MISC FF COMP
MISC FF CLEAR
104 ← SUPPRESS READ END PULSE
24 ← AR CLEAR 5-16
61 ← OVERFLOW CHECK
20 ← AR CLEAR 0-4
418 ← SC READ IN
72 ← MC READ IN
47 ← SC CLEAR
71 ← MB CLEAR
60 ← PARITY FF CLEAR
43 ← PC READ OUT
42 ← PC ADD ONE
FX COMP
106A ← SUPPRESS OPERATION TIMING I
106B ← SUPPRESS OPERATION TIMING II
101 ← RESTART
103 ← HALT INSTRUCTION
168 ← MASTER FF ZERO
65 ← CLEAR ALARMS
100 ← START OVER
45A ← SET PC 14

FD, FW, FR, FX, F0, F1, F2, F3, F4, F5, FS

11 READ END PULSE
110 READ GATE
112 WRITE END PULSE
11B FO COMP
10C F1 COMP
11 CS-PS READ IN
12 CS-PS CLEAR

LR DETECTION → 185
LR READ IN → 83
LR CLEAR → 82
LR READ OUT → 84A
TOGGLE SW READ OUT → 86
AC OP READ OUT → 34A
AC ADDR READ OUT → 34B
PARITY CHECK → 62
AR PARITY CHKT → 21
AC CLEAR → 30
AC COMP → 36
AC ADD → 31
AC CARRY → 35
AC CARRY CLEAR → 37
AC NOT ZERO → 131
TEST OR ALARM → 01
1 FROM DIGIT SELECTOR → 177
0 FROM DIGIT SELECTOR → 178
INTENSIFY → 58
MEM. SCOPE INTENSIFY → 55
SCOPE END PULSES → 150
PRINTER END PULSE → 157
PC READ IN → 41
PC CLEAR → 40
AC0 - 1 SIDE → 130
AC SHIFT RIGHT → 32
BR SHIFT RIGHT → 93
AC CYCLE RIGHT → 33
PRINT → 52
SC SUBTR. ONE → 49
READER END PULSE → 152
READ FLEXO → 67
BR CLEAR → 90

ALSO TO PS
CS COMPLEMENT → 10A
AR 1 OUT BUS
SC END CARRY → 149

11 FLIPFLOPS
30 DELAYS
50 GATES

= "AND" GATE
= "OR" GATE
= DELAY

AUTO. MEMORY DISPLAY, MEMORY CHECK, PROGRAM TIMING, & HALT

MEMORY | PARITY | STORE | ADD & SUBTRACT | TRANSFER | SHIFT & FLEXO | CONTROL SWITCH | DISPLAY

GRADED BY: DATE: THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:
GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN

CHG.	CN#	DATE	APPD.
-20			
-19			
-18			
-17			
-16			
-15			
-14			
-13			
-12			
-11	C-SCD-1166	11-5-53	RCB
-10	C-SCD-1166	11-5-53	RCB
-9	C-SCD-1166	11-5-53	RCB
-8	C-SCD-1166	11-5-53	RCB
-7	C-SCD-1166	11-5-53	RCB
-6	C-SCD-1166	11-5-53	RCB
-5	C-SCD-1166	11-5-53	RCB
-4	C-SCD-1166	11-5-53	RCB
-3	C-SCD-1166	11-5-53	RCB
-2	C-SCD-1166	11-5-53	RCB
-1	C-SCD-1166	11-5-53	RCB

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING — D. I. C. PROJECT NO.

BLOCK DIAGRAM, CONTROL, MTC

SCALE: | DR. BAGLEY 3-3-53 | ENG. 3-3-53 | CK. 3-26-53 | APPD. | SD-37376

START OVER & PROGRAM TIMING MTC

SD-SMH12-5

ABBREVIATIONS:

PC - PROGRAM COUNTER
SC - STEP COUNTER
CS - CONTROL SWITCH
PS - PANEL STORAGE SWITCH
MS - MAGNETIC MEMORY SWITCH
MM - SELECTED REGISTER OF MAGNETIC MEMORY
LR - LIVE REGISTER
AR - A REGISTER
AC - ACCUMULATOR
BR - B REGISTER
FX - PROGRAM/OPERATION TIMING FLIP FLOP
F0 TO 5 - CONTROL SWITCH FLIP FLOPS

0 - CLEAR
N_P - PROGRAM ADDRESS
N_A - ADDRESS PORTION OF A NUMBER
N_O - OPERATION PORTION OF A NUMBER
N_R - ANY RANDOM NUMBER
N - $N_O + N_A$

L.F. PULSE GEN
1 → FS
G ◆ FS(1)
SYNC SOURCE
START OVER (100)
0 → ALARMS (65)
0 → PC (40)
0 → AC (30)
0 → FX
0 → BR (90)
0 → AC CARRY (37)
0 → FR
0 → FW
0 → FD
0.5
RESTART (101)
2 → PC (45A)
1 → FX
0.5
✳ REENTRY OF PULSE FOR OPERATION TIMING
0 → SC (47)
0 → CS (12)
0 → PS (12)
0 → MS (71)
0 → FS
0 → PARITY ALARM (60)
FX(1) ◆ G
0 → AR (20) E (24)
G → 1 → FX
◆ 106A (SUP. OPN TMG) (NORM. OFF)
G → COMP FX (TO 0)
◆ 106B (SUP. OPN TMG) (NORM. ON)
0.5
PC → AR (43)
1.0
0.1
AD 1 → PC (42)
AR → SC (48)
AR → CS (11)
AR → PS (11)
AR → MS (72)
0.8
G ◆ F0 (0)
0 → AR (20) E (24)
(CHOOSES MAGNETIC MEMORY) F5 (1) ◆ G
G ◆ F5 (0) (CHOOSES PANEL STORAGE)
START READ PULSE (1 → FR)
(2.4) ϵ
γ (1.5)
F2 (0) ◆ G
MM → AR (70A)
α_S (2)
185 (LR DET.)
TSS → AR (86)
G → LR → AR (89A)
STOP READ PULSE (0 → FR)
0.1
F5 (1)
G ◆ 104 (SUP. READ END PULSE)
0 → LR (82)
AR PARITY COUNT (21)
1.0
G ◆ F1 (0) (0000 - DIODE "AND" GATE)
◆ F2 (0)
◆ F3 (0)
F5 (1) ◆ G
G → COMP → F0 (TO 1)
(0.5) ρ
0.5 FX (0)
PARITY CHECK (62)
(1 DIGIT SEL.) 177 ◆ G
(CHOOSES MAGNETIC MEMORY) F5 (1) ◆ G
G ◆ F5 (0) (CHOOSES PANEL STORAGE)
185 (LR DET) ◆ G
178 (0 DIGIT SEL) ◆ G
START WRITE PULSE (1 → FW)
G → AR → LR (83)
F2 (0) ◆ G
INT. (58)
MEM 100 SCOPE (15A)
β_S (2)
F0 (1) ◆ G
COMP → F0 (TO 0)
STOP WRITE PULSE (0 → FW)
(1) θ
G ◆ A ◆ 168 (MASTER ALARM 0)
◆ 103 (OFF FOR HALF INSTR.)
START DISTURB PULSE (1 → FD)
(1.5) δ
STOP DISTURB PULSE (0 → FD)
RETURN TO ✳ FOR OPERATION TIMING

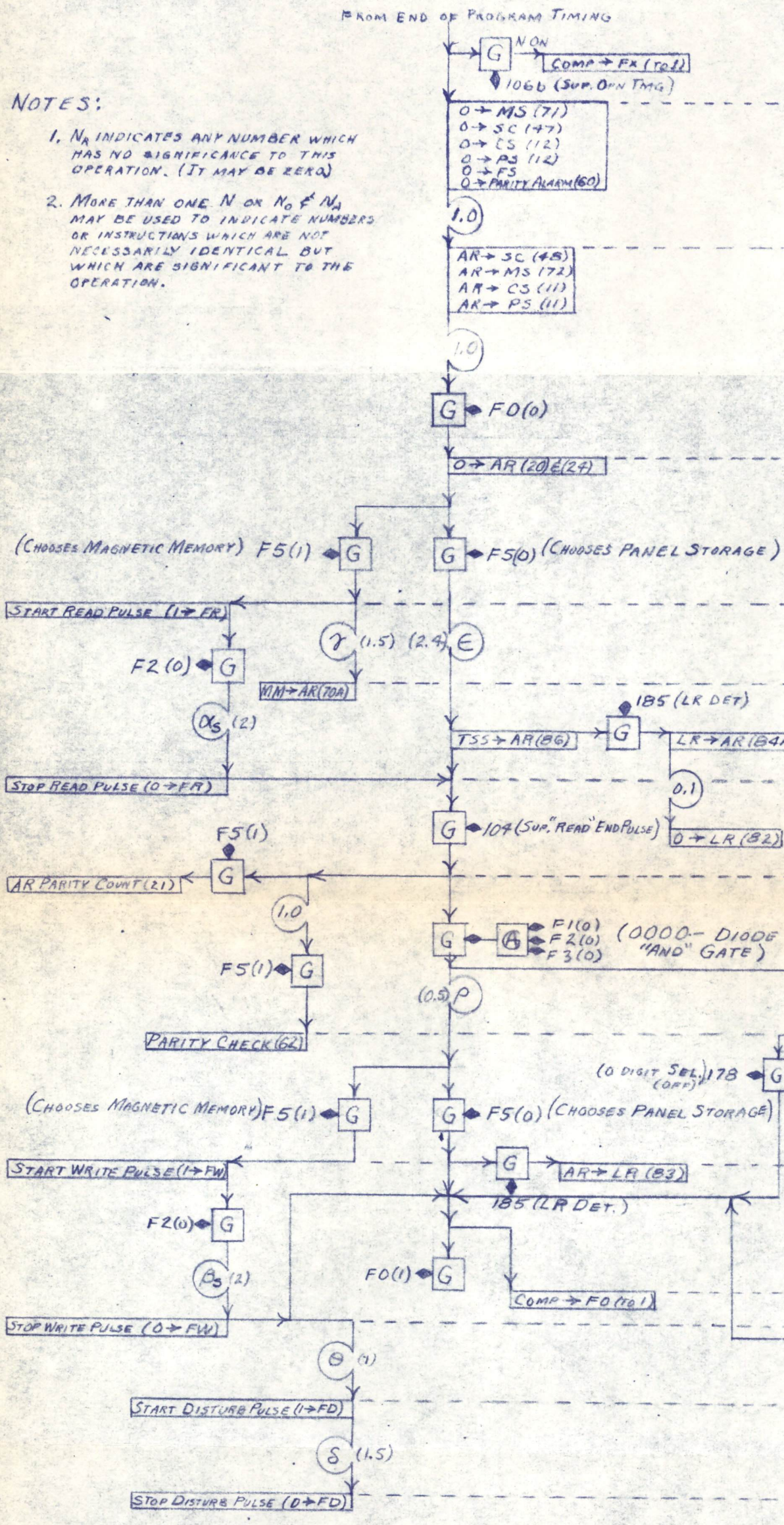
ELAPSED TIME	PC RT 11	SC RT 5	CS LFT 6	PS RT 5	MS RT 11	SEL. REG. MM	LR	AR LFT 5	AR RT 11	AC LFT 5	AC RT 11	BR
	N_R	N_R	N_R	N_R	N_R	N_R OR N	N OR N_R	N_R	N_R	N_P	N_R	N_R
0	0									0	0	0
	2 OR N_P	0	0	0	0	N_R OR N	N OR N_R	N_R	N_R	N_R OR N_O (FROM PREVIOUS OPN.)	N_R OR N_A	0 OR N_R
								0	0			
								0	N_P			
	N_P +1	N_P	0	N_P	N_P	N_R OR N	N OR N_R	N_O	N_A	0 OR N_O	0 OR N_A	N_R
								0	0			
								0	0			
								N_O	N_A			
						N_R OR 0	0 OR N_R					
									16			
							N OR N_R					
									0			
						N_R OR N						
	N_P +1	N_P	0	N_P	N_P	N_R OR N	N_R OR N	N_O	N_A	0 OR N_O	0 OR N_A	N_R

HALT
#0 (00000) ha
OPERATION TIMING
MTC

ABBREVIATIONS:
O - CLEAR
N_P - PROGRAM ADDRESS
N_O - LEFT 5 DIGITS
N_A - RIGHT 11 DIGITS
N_R - ANY RANDOM NO.
N - $N_O + N_A$ (N). OR INST.)

NOTES:

1. N_R INDICATES ANY NUMBER WHICH HAS NO SIGNIFICANCE TO THIS OPERATION. (IT MAY BE ZERO)
2. MORE THAN ONE N OR N_O & N_A MAY BE USED TO INDICATE NUMBERS OR INSTRUCTIONS WHICH ARE NOT NECESSARILY IDENTICAL BUT WHICH ARE SIGNIFICANT TO THE OPERATION.



ELAPSED TIME	PC RT 11	SC RT 5	CS LFT 6	PS RT 5	MS RT 11	SEL REG MM	LR	AR LFT 5	AR RT 11	AC LFT 5	AC RT 11	BR
0	N_P +1	N_P	0	N_P	N_P	N_R	N_R	N_O (0)	N_A (N_R)	N_R	N_R	N_R
		0	0	0	0							
		RT 5 OF N_A (N_R)	N_O (0)	RT 5 OF N_A (N_R)	N_A (N_R)							
								0	0			
								0 OR N_R	0 OR N_R			
								N_R	N_R			
							N_R OR 0					
							0 OR N_R					
							N_R					
						N_P +1						
						RT 5 OF N_A (N_R)						
						16						
						RT 5 OF N_A (N_R)						
						N_A (N_R)						
						N_R						
						N_R						
						N_R						
						N_R						
						N_R						
						N_R						
						N_R						

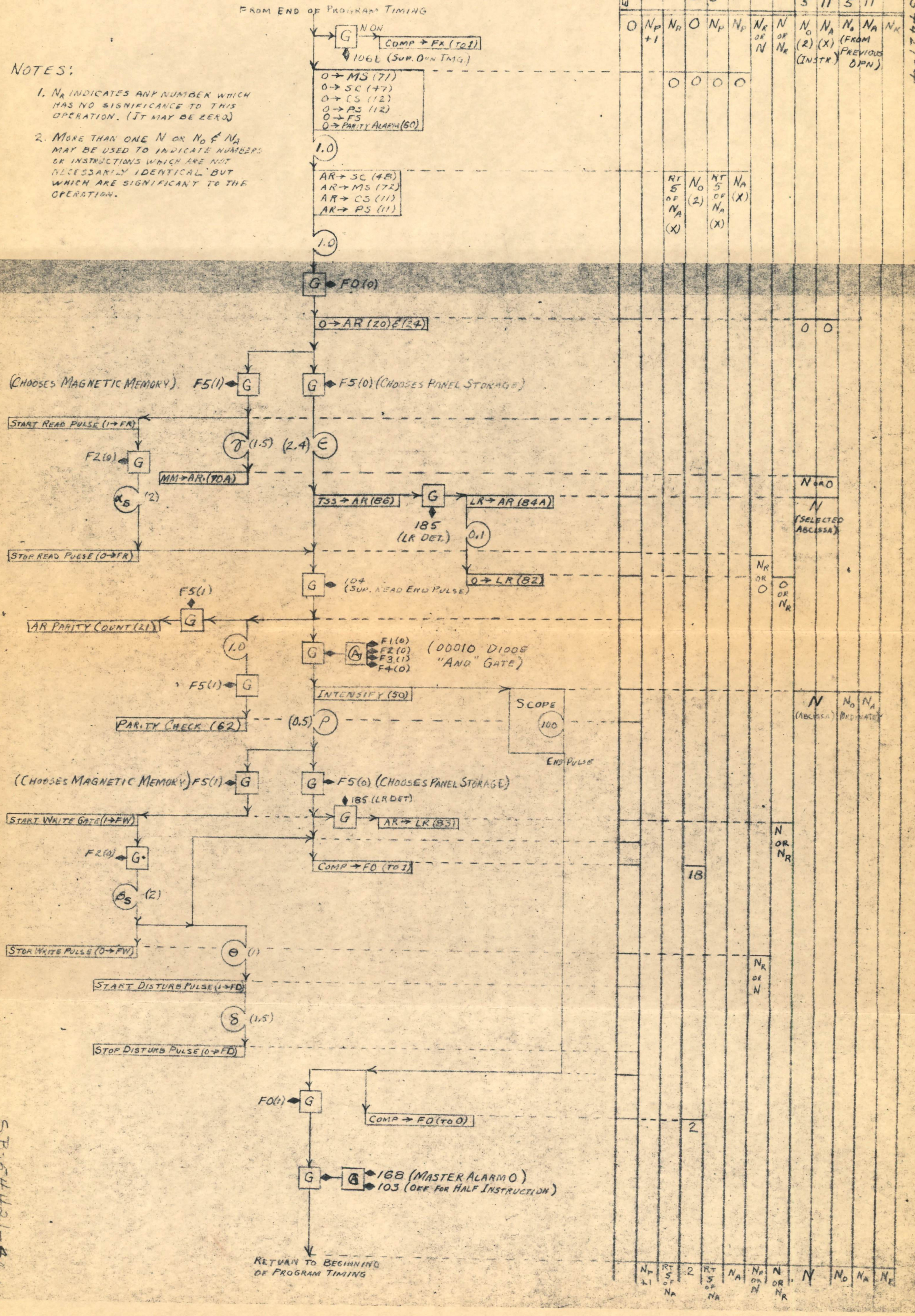
SB-54413-5

DISPLAY
#2 (00010) ds x
OPERATION TIMING
MTC

ABBREVIATIONS:
O - CLEAR
N_P - PROGRAM ADDRESS
N_O - LEFT 5 DIGITS
N_A - RIGHT 11 DIGITS
N_R - ANY RANDOM No.
N - N_O + N_A (No. OR INST.)

NOTES:

1. N_R INDICATES ANY NUMBER WHICH HAS NO SIGNIFICANCE TO THIS OPERATION. (IT MAY BE ZERO)
2. MORE THAN ONE N OR N_O & N_A MAY BE USED TO INDICATE NUMBERS OR INSTRUCTIONS WHICH ARE NOT NECESSARILY IDENTICAL BUT WHICH ARE SIGNIFICANT TO THE OPERATION.



SB-5442/-4

SB-5442/-4

IDENTITY CHECK #3 (00011) id x
OPERATION TIMING
MTC

SB-54568-3

ABBREVIATIONS:
O - CLEAR
N_P - PROGRAM ADDRESS
N_O - LEFT 5 DIGITS
N_A - RIGHT 11 DIGIT
N_R - ANY RANDOM NO.
N - $N_O + N_A$ (N. OR ENTER)

NOTES:

1. N_R INDICATES ANY NUMBER WHICH HAS NO SIGNIFICANCE TO THIS OPERATION. (IT MAY BE ZERO)
2. MORE THAN ONE N OR N_O & N_A MAY BE USED TO INDICATE NUMBERS OR INSTRUCTIONS WHICH ARE NOT NECESSARILY IDENTICAL BUT WHICH ARE SIGNIFICANT TO THE OPERATION.

	ELAPSED TIME	PC RT 11	SC RT 5	CS LFT 6	PS RT 5	MS RT 11	SEL. REG. MM	LR	AR LFT 5	AR RT 11	AC LFT 5	AC RT 11	BR
FROM END OF PROGRAM TIMING													
G — N ON → COMP → FX (TO 1)	0	N_P +1	N_P	0	N_P	N_P	N_R OR N	N OR N_R	N_O (3) (INSTR.)	N_A (X)	N (FROM PREVIOUS OPN.)		N_R
106 (SUP. OPN TMG.)													
0 → MS (71); 0 → SC (47); 0 → CS (12); 0 → PS (12); 0 → FS; 0 → PARITY ALARM (60)			0	0	0	0							
1.0													
AR → SC (48); AR → MS (72); AR → CS (11); AR → PS (11)			RT 5 OF N_A (X)	N_O (3)	RT 5 OF N_A (X)	N_A (X)							
1.0													
0 → AR (20) & (24)									0	0			
(CHOOSES MAGNETIC MEMORY) F5(1) G ; G F5(0) (CHOOSES PANEL STORAGE)													
START READ PULSE (1 → FR)													
F20 G ; τ (1.5) ; (2.4) ε													
MM → AR (70A)													
α_S (2)													
185 (LR DET.)													O OR N
TSS → AR (86) ; G → LR → AR (84A)													N
STOP READ PULSE (0 → FR)													
0.1													
0 → LR (82)							N_R OR O	O OR N_R					
G — 104 (SUP. "READ" END PULSE)													
F5(1) G — AR PARITY COUNT (21)													
1.0													
F5(1) G ; G — A: F1(0), F2(0), F3(1), F4(1) (00011 DIODE "AND" GATE)													
PARITY CHECK (62) ; AR → AC (31)													N+N (PARTIAL SUM — WILL BE 0 IF IDEN)
(CHOOSES MAGNETIC MEMORY) F5(1) G ; G (CHOOSES PANEL STORAGE) F5(0)													
1.0													
START WRITE PULSE (1 → FW)													
G — AR → LR (83)													
0 → AC CARRY (37)													
185 (LR DET)													
131 (AC NOT 0 "OR" GATE)								IV OR N_R					
F2(0) G — COMP → FO (TO 1 OR 0) ; G — TEST OR ALARM (01) +1 → PC (72)													
β_S (2)													
0.5													
STOP WRITE PULSE (0 → FW)													
θ (1) ; G — FO (1)							N_R OR N						
COMP FO (TO 0 OR 1)				19									
START DISTURB PULSE (1 → FD) ; G — A: 168 (MASTER ALARM 0), 103 (OFF FOR HALF INSTRUCTION)				3									
δ (1.5)													
STOP DISTURB PULSE (0 → FD)													
RETURNS TO BEGINNING OF PROGRAM TIMING		N_P +1 OR +2 IF ERR	RT 5 OF N_A (X)	3	RT 5 OF N_A (X)	N_A (X)	N_R OR N	N OR N_R	N	1'S IN DIGITS WHERE NOT IDEN.			N_R

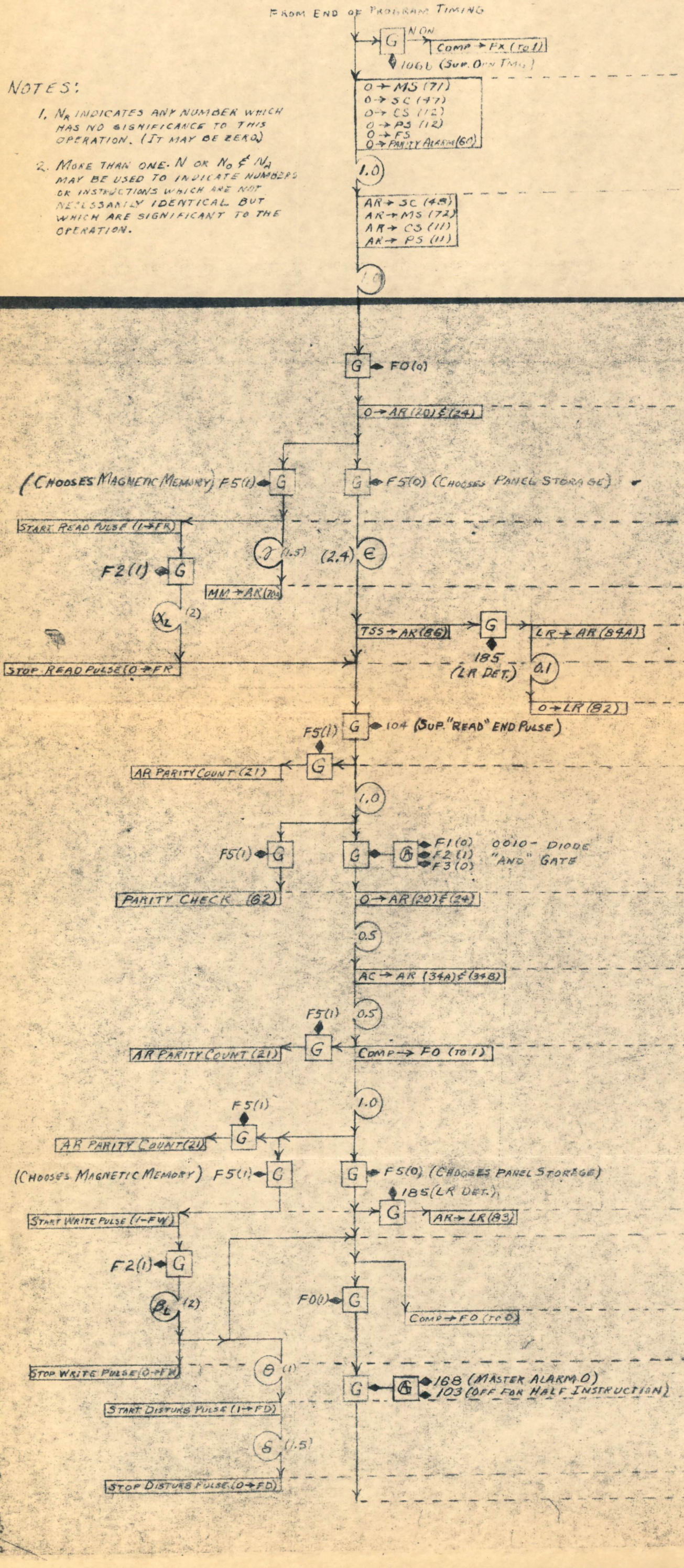
SB-54568-3

STORE #4 (00100) ST X
OPERATION TIMING
MTC

ABBREVIATIONS:
O - CLEAR
N_P - PROGRAM ADDRESS
N_O - LEFT 5 DIGITS
N_A - RIGHT 11 DIGIT
N_R - ANY RANDOM NO.
N - N_O + N_A (N1 OR LN-1)

NOTES:

1. N_R INDICATES ANY NUMBER WHICH HAS NO SIGNIFICANCE TO THIS OPERATION. (IT MAY BE ZERO)
2. MORE THAN ONE N OR N_O & N_A MAY BE USED TO INDICATE NUMBERS OR INSTRUCTIONS WHICH ARE NOT NECESSARILY IDENTICAL BUT WHICH ARE SIGNIFICANT TO THE OPERATION.



ELAPSED TIME	PC RT 11	SC RT 5	CS LEFT 6	PS RT 5	MS RT 11	SEL REG MM	LR	AR LFT 5	AR RT 11	AC LFT 5	AC RT 11	BR
0	N_P +1	N_P	0	N_P	N_P	N_R	N_R	N_O (4) (INSTR.)	N_A (X)	N_O (FROM PREVIOUS OPN)	N_A	N_R
		0	0	0	0							
		RT 5 OF N_A (X)	N_O (4)	RT 5 OF N_A (X)	N_A (X)							
								0	0			
								0 OR N_R				
							N_R					
						N_R OR 0						
							0 OR N_R					
								0	0			
										N_O	N_A	
			20									
							N OR N_R					
			4									
						N_R OR N						
	N_P +1	RT 5 OF N_A	4	RT 5 OF N_A	N_A	N_R OR N	N OR N_R	N_O	N_A	N_O	N_A	N_R

SB-54459-2

SB-54459-3

REPLACE ADDRESS #6 (00110) ra x

OPERATION TIMING

MTC

ABBREVIATIONS:
O - CLEAR
N_P - PROGRAM ADDRESS
N_O - LEFT 5 DIGITS
N_A - RIGHT 11 DIGITS
N_R - ANY RANDOM NO.
N - $N_O + N_A$ (NO. OR INSTR.)

NOTES:

1. N_R INDICATES ANY NUMBER WHICH HAS NO SIGNIFICANCE TO THIS OPERATION. (IT MAY BE ZERO)
2. MORE THAN ONE N OR N_O & N_A MAY BE USED TO INDICATE NUMBERS OR INSTRUCTIONS WHICH ARE NOT NECESSARILY IDENTICAL BUT WHICH ARE SIGNIFICANT TO THE OPERATION.

* N_1 REPRESENTS THAT NUMBER THE ADDRESS OF WHICH IT IS DESIRED TO REPLACE

N_2 REPRESENTS THAT NUMBER COMPOSED OF THE LEFT 5 DIGITS OF N_1 AND THE RIGHT 11 DIGITS OF THE NUMBER IN AC

ELAPSED TIME	PC RT 11	SC RT 5	CS LFT 6	PS RT 5	MS RT 11	SEL. REG. MM	LR	AR LFT 5	AR RT 11	AC LFT 5	AC RT 11	BR
0	N_P +1	N_P	0	N_P	N_P	N_R OR N_1	N_1* OR N_R	N_O (6) (INSTR)	N_A (X)	N_O (FROM PREVIOUS OPTN.)	N_A	N_R
		0	0	0	0							
1.0		RT 5 OF N_A (X)	N_O (6)	RT 5 OF N_A (X)	N_A (X)							
1.0								0	0			
								0 OR N_{O_1}	0 OR N_{A_1}			
								N_{O_1}	N_{A_1}			
						N_R OR 0						
							0 OR N_R					
1.0												
								N_{O_1}	0			
0.5												
								N_{O_1}	N_A			
0.5			22									
1.0												
							N_2* OR N_R					
			6									
						N_R OR N_2						
	N_P +1	RT 5 OF N_A	6	RT 5 OF N_A	N_A	N_R OR N_2	N_2 OR N_R	N_{O_1}	N_{A_1}	N_D	N_A	N_R

FROM END OF PROGRAM TIMING

G — NON → COMP → FX (TO 1)
1060 (SUP. OPN TMG.)

0 → MS (71)
0 → SC (47)
0 → CS (12)
0 → PS (12)
0 → FS
0 → PARITY ALARM (60)

1.0

AR → SC (48)
AR → MS (72)
AR → CS (11)
AR → PS (11)

1.0

G — 10 (0)

0 → AR (20) E (24)

(CHOOSES MAGNETIC MEMORY) F5(1) — G — START READ PULSE (1 → FR)

F2(1) — G — α (2) — STOP READ PULSE (0 → FR)

γ (1.5) — MM → AR (10A)

G — F5(0) (CHOOSES PANEL STORAGE)

ε (2.4)

185 (LR DET.)

TSS → AR (86) — G — LR → AR (84A)

0.1 — 0 → LR (82)

F5(1) — G — 104 (SUP. "READ" END PULSE)

AR PARITY COUNT (21) — G

1.0

F5(1) — G — G — G — F1(0), F2(1), F3(1) (0011 - DIODE "AND" GATE)

PARITY CHECK (62)

0 → RT 11 OF AR (24)

0.5

RT 11 OF AC → AR (34B)

0.5

AR PARITY COUNT (21) — G — COMP → F0 (TO 1)

1.0

AR PARITY COUNT (21) — G

(CHOOSES MAGNETIC MEMORY) F5(1) — G — G — F5(0) (CHOOSES PANEL STORAGE)

185 (LR DET.)

START WRITE PULSE (1 → FW)

F2(1) — G — β (1)

F0(1) — G — COMP → F0 (TO 0)

STOP WRITE PULSE (0 → FW)

START DISTURB PULSE (1 → FD)

G — 168 (MASTER ALARM 0), 103 (OFF FOR HALF INSTRUCTION)

δ (1.5)

STOP DISTURB PULSE (0 → FD)

RETURN TO BEGINNING OF PROGRAM TIMING

SB-5447-2

SB-5447-2 M

CLEAR AND ADD #8 (01000) ca x
OPERATION TIMING
MTC

ABBREVIATIONS:
O - CLEAR
N_P - PROGRAM ADDRESS
N_O - LEFT 5 DIGITS
N_A - RIGHT 11 DIGITS
N_R - ANY RANDOM NO.
N - $N_O + N_A$ (NO. OR INSTR.)

NOTES:

1. N_R INDICATES ANY NUMBER WHICH HAS NO SIGNIFICANCE TO THIS OPERATION. (IT MAY BE ZERO)
2. MORE THAN ONE N OR N_O & N_A MAY BE USED TO INDICATE NUMBERS OR INSTRUCTIONS WHICH ARE NOT NECESSARILY IDENTICAL BUT WHICH ARE SIGNIFICANT TO THE OPERATION.

ELAPSED TIME	PC RT 11	SC RT 5	CS LFT 6	PS RT 5	MS RT 11	SEL REG MM	LR	AR LFT 5	AR RT 11	AC LFT 5	AC RT 11	BR
0	N_P +1	N_P	0	N_P	N_P	N_R OR N	N OR N_R	N_O (8) (INSTR)	N_A (X)	N_R	N_R	N_R
		0	0	0	0							
		RT 5 OF N_A (X)	N_O (8)	RT 5 OF N_A (X)	N_A (X)							
								0	0			
								N_O OR 0	N_A OR 0			
								N_O	N_A			
						N_R OR 0						
							0 OR N_R					
										0	0	
										N_O	N_A	
										N_O	N_A	
						N_R OR N				N_O	N_A	
										N_O	N_A	
		24										
		8										
	N_P +1	RT 5 OF N_A (X)	8	RT 5 OF N_A (X)	N_A (X)	N_R OR N	N OR N_R	N_O	N_A	N_P	N_A	N_R

SB-54480-2

SB-54480-1

SB-54480-2A

ADD
#9 (01001) ad x
OPERATION TIMING
MTC

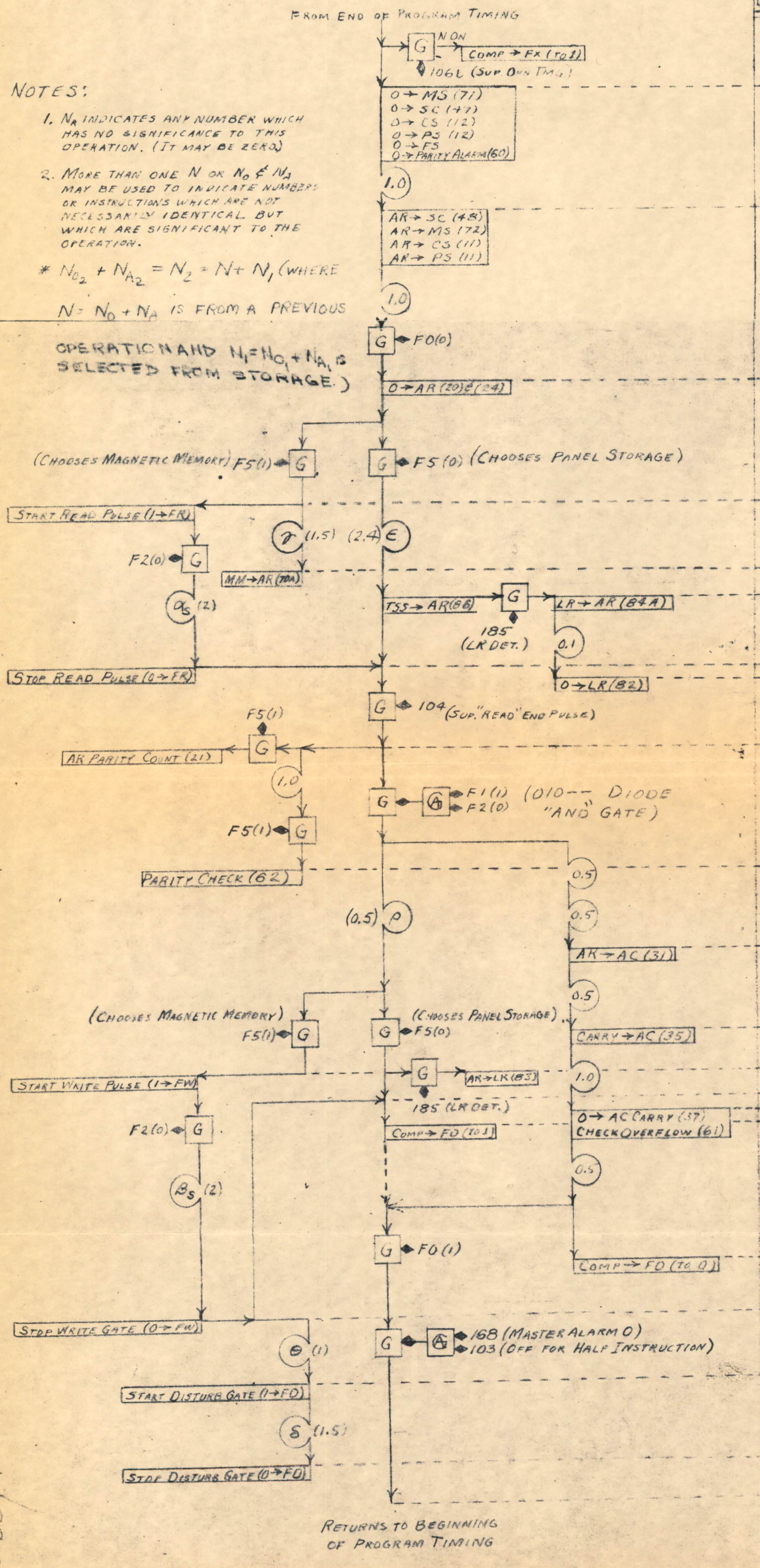
ABBREVIATIONS:
O - CLEAR
N_P - PROGRAM ADDRESS
N_O - LEFT 5 DIGITS
N_A - RIGHT 11 DIGITS
N_R - ANY RANDOM NO.
N - $N_O + N_A$ (NO. OR INSTR.)

NOTES:

1. N_R INDICATES ANY NUMBER WHICH HAS NO SIGNIFICANCE TO THIS OPERATION. (IT MAY BE ZERO)

2. MORE THAN ONE N OR N_O & N_A MAY BE USED TO INDICATE NUMBERS OR INSTRUCTIONS WHICH ARE NOT NECESSARILY IDENTICAL BUT WHICH ARE SIGNIFICANT TO THE OPERATION.

* $N_{O_2} + N_{A_2} = N_2 = N + N_1$ (WHERE $N = N_O + N_A$ IS FROM A PREVIOUS OPERATION AND $N_1 = N_{O_1} + N_{A_1}$ IS SELECTED FROM STORAGE.)



ELAPSED TIME	PC RT 11	SC RT 5	CS LFT 6	PS RT 5	MS RT 11	SEL. REG. MM	LR	AR LFT 5	AR RT 11	AC LFT 5	AC RT 11	BR
O	N_P +1	N_P	O	N_P	N_P	N_R OR N_1	N_1 OR N_R	N_O (9) (INSTR)	N_A (X)	N_O (FROM PREVIOUS OPN)	N_A	N_R
		O	O	O	O							
		RT 5 OF N_A (X)	N_O (9)	RT 5 OF N_A (X)	N_A (X)							
								O	O			
								O OR N_1				
								N_1				
						N_R OR O	O OR N_R					
										N_O + N_{O_1}	N_A + N_{A_1} (PARTIAL SUM)	
										N_{O_2}	N_{A_2} *	
							N_1 OR N_R					
			25									
			9									
						N_R OR N_1						
	N_P +1	RT 5 OF N_A (X)	9	RT 5 OF N_A (X)	N_A (X)	N_R OR N_1	N_1 OR N_R	N_{O_1}	N_{A_1}	N_{O_2}	N_{A_2}	N_R

SB-54487-2

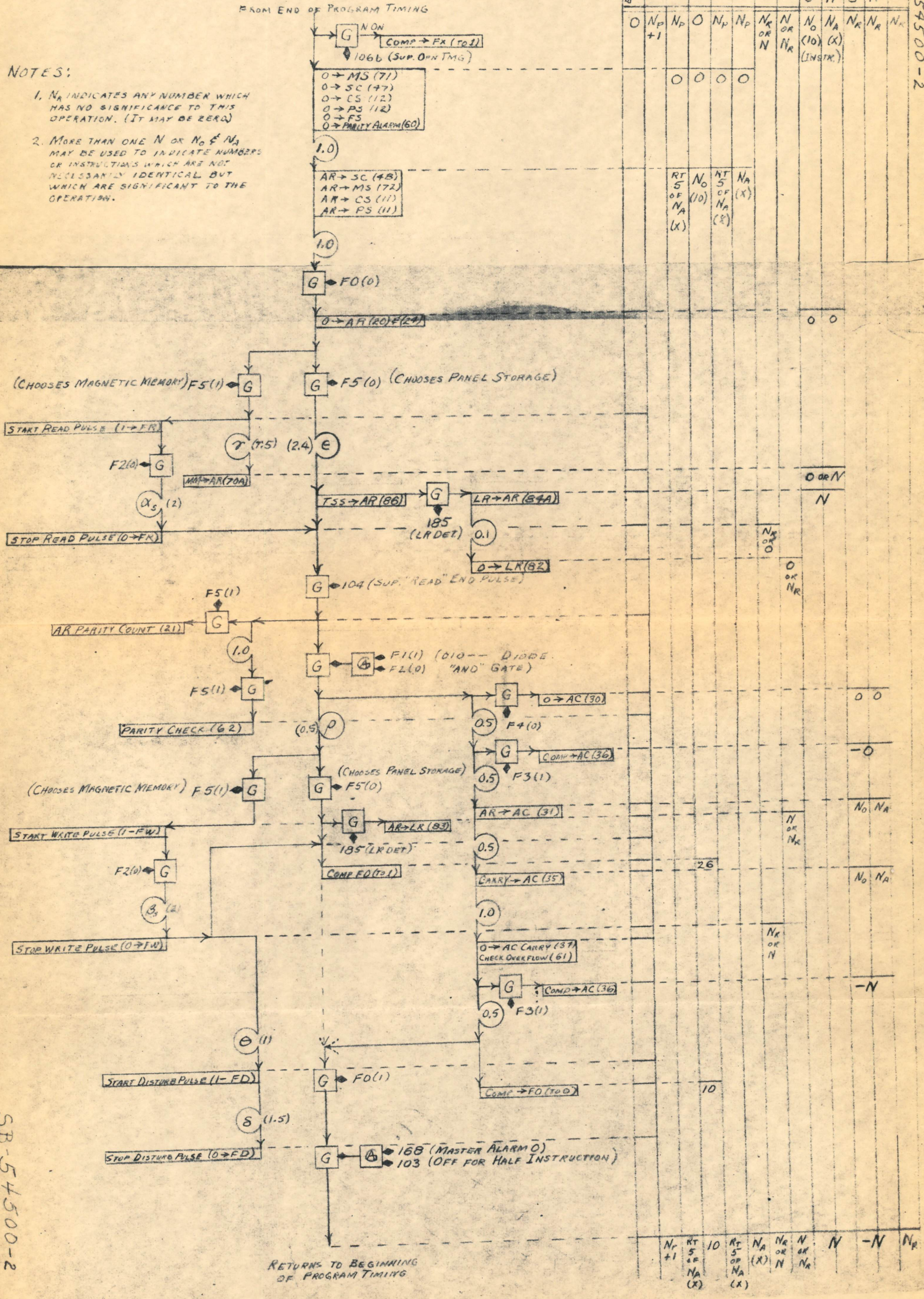
SB-54487-2

CLEAR AND SUBTRACT
#10 (01010) CS X
OPERATION TIMING
MTC

ABBREVIATIONS:
O - CLEAR
N_P - PROGRAM ADDRESS
N_O - LEFT 5 DIGITS
N_A - RIGHT 11 DIGITS
N_R - ANY RANDOM NO.
N - $N_O + N_A$ (NO. OR INST.)

NOTES:

1. N_R INDICATES ANY NUMBER WHICH HAS NO SIGNIFICANCE TO THIS OPERATION. (IT MAY BE ZERO)
2. MORE THAN ONE N OR N_O & N_A MAY BE USED TO INDICATE NUMBERS OR INSTRUCTIONS WHICH ARE NOT NECESSARILY IDENTICAL BUT WHICH ARE SIGNIFICANT TO THE OPERATION.



SB-54500-2

SB-54500-2

SUBTRACT #11 (01011) SU X
OPERATION TIMING
MTC

SB-54524-2

ABBREVIATIONS:
O - CLEAR
N_P - PROGRAM ADDRESS
N_O - LEFT 5 DIGITS
N_A - RIGHT 11 DIGITS
N_R - ANY RANDOM No.
N - $N_O + N_A$ (No. OR INSTR.)

NOTES:

1. N_R INDICATES ANY NUMBER WHICH HAS NO SIGNIFICANCE TO THIS OPERATION. (IT MAY BE ZERO)
2. MORE THAN ONE N OR N_O & N_A MAY BE USED TO INDICATE NUMBERS OR INSTRUCTIONS WHICH ARE NOT NECESSARILY IDENTICAL BUT WHICH ARE SIGNIFICANT TO THE OPERATION.

* $N_{O_2} + N_{A_2} = N_2 = N - N_1$

	ELAPSED TIME	PC RT 11	SC RT 5	CS LEFT 6	PS RT 5	MS RT 11	SEL REG MM	LR	AR LFT 5	AR RT 11	AC LFT 5	AC RT 11	BR
FROM END OF PROGRAM TIMING	0	N_P +1	N_P	0	N_P	N_P	N_R OR N_1	N_1 OR N_R	N_O (11) (INSTR.)	N_A (X)	N_O (FROM PREVIOUS OPN.) (N)	N_A	N_K
G N ON — COMP → FX (TO 1) — 1061 (SUP. OWN TMG.)													
0 → MS (71); 0 → SC (47); 0 → CS (12); 0 → PS (12); 0 → FS; 0 → PARITY ALARM (60)			0	0	0	0							
1.0													
AR → SC (48); AR → MS (72); AR → CS (11); AR → PS (11)			RT 5 OF N_A (X)	N_O (11)	NT 5 OF N_A (X)	N_A (X)							
1.0													
G ◆ F0(0)													
0 → AR (20) & (24)									0	0			
(CHOOSES MAGNETIC MEMORY) F5(1) G — G ◆ F5(0) (CHOOSES PANEL STORAGE)													
START READ PULSE (1 → FR) — F2(0) G — γ (1.5) — MM → AR (70A)													
(2.4) ∈ — TSS → AR (86) — G — 185 (LR DET.) — LR → AR (84A)													
α_3 (2) — STOP READ PULSE (0 → FR) — 0.1 — 0 → LR (82)							N_R OR 0	$\overline{OR}$ N_{O_1} N_{A_1}					
G ◆ 104 (SUP "READ" END PULSE)								0 OR N_R					
F5(1) G — AR PARITY COUNT (21) — 1.0													
G — G ◆ F1(1) F2(0) (010 — DIODE "AND" GATE) — F5(1) G													
PARITY CHECK (62) — (0.5) P — 0.5 — G → COMP → AC (36) — F3(1)												-N	
(CHOOSES MAGNETIC MEMORY) F5(1) G — G ◆ F5(0) (CHOOSES PANEL STORAGE) — 0.5 — F3(1)													
START WRITE PULSE (1 → FW) — G → AR → LK (83) — AR → AC (31)								N_1 OR N_R				-N+N₁ (PARTIAL SUM)	
185 (LR DET.) — 0.5													
F2(0) G — COMP → F0 (TO 1) — CARRY → AC (35)										27		-N+N₁	
β_3 (2) — 1.0							N_R OR N_1						
STOP WRITE PULSE (0 → FW) — 0 → AC CARRY (37) CHECK OVERFLOW (61)													
G → COMP → AC (36) — F3(1) — 0.5												N-N₁	
θ (1)													
START DISTURB PULSE (1 → FD) — G ◆ F0(1) — COMP → F0 (TO 0)										11			
S (1.5) — STOP DISTURB PULSE (0 → FD)													
G — G ◆ 168 (ON FOR MASTER ALARM 0) ◆ 103 (OFF FOR HALF INSTRUCTION)													
RETURN TO BEGINNING OF PROGRAM TIMING		N_P +1	RT 5 OF N_A (X)	11	RT 5 OF N_A (X)	N_A (X)	N_R OR N_1	N_1 OR N_R	N_{O_1}	N_{A_1}	N_{O_2}	N_{A_2} *	N_R

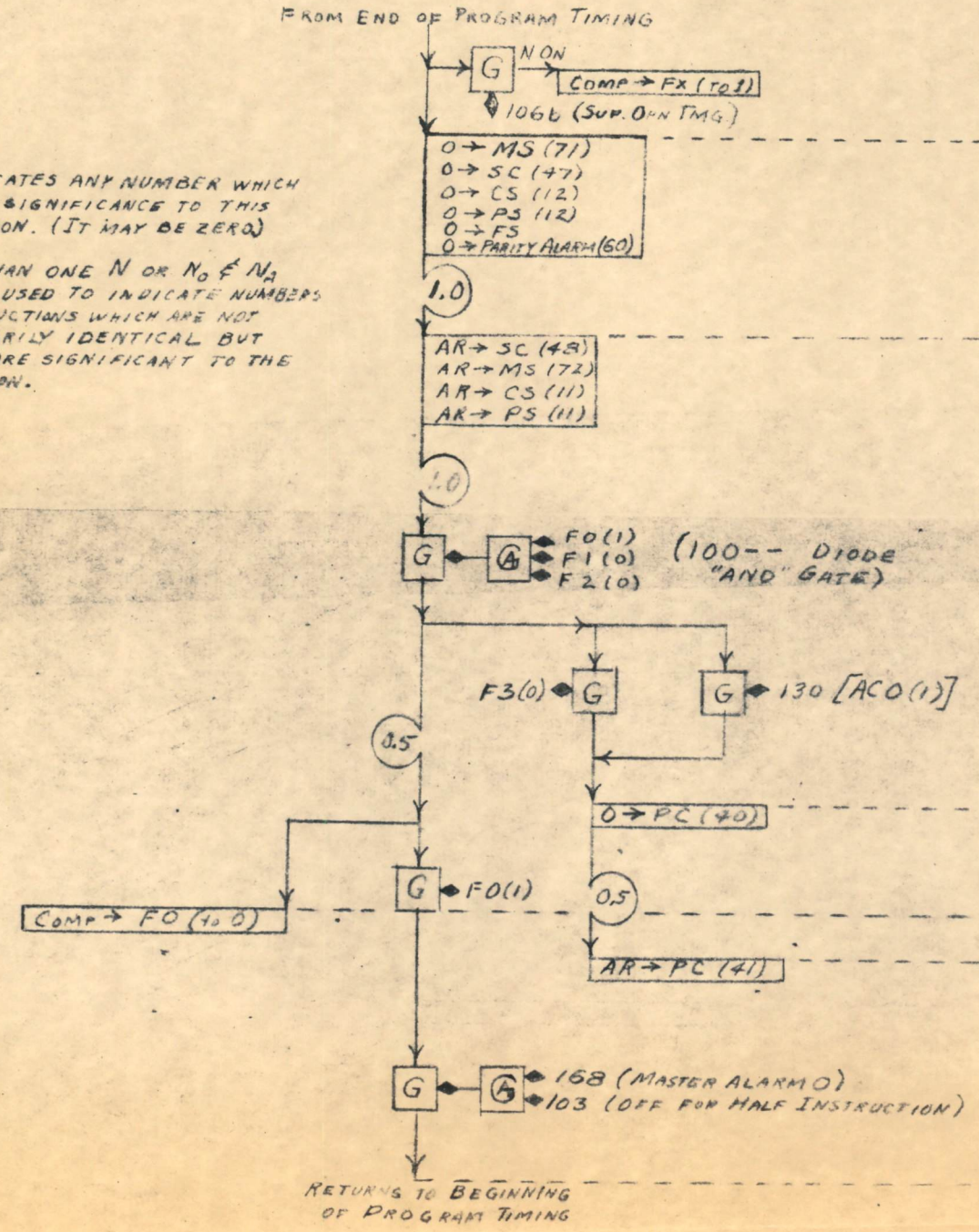
SB-54524-2

TRANSFER #16 (10000) +r x OPERATION TIMING MTC

ABBREVIATIONS:
O - CLEAR
N_P - PROGRAM ADDRESS
N_O - LEFT 5 DIGITS
N_A - RIGHT 11 DIGITS
N_R - ANY RANDOM No.
N - $N_O + N_A$ (No. OR INSTR.)

NOTES:

1. N_R INDICATES ANY NUMBER WHICH HAS NO SIGNIFICANCE TO THIS OPERATION. (IT MAY BE ZERO)
2. MORE THAN ONE N OR N_O & N_A MAY BE USED TO INDICATE NUMBERS OR INSTRUCTIONS WHICH ARE NOT NECESSARILY IDENTICAL BUT WHICH ARE SIGNIFICANT TO THE OPERATION.



ELAPSED TIME	PC RT 11	SC RT 5	CS LFT 6	PS RT 5	MS RT 11	SEL. REG. MM	LR	AR LFT 5	AR RT 11	AC LFT 5	AC RT 11	BR
0	N_P +1	N_P	0	N_P	N_P	N_K	N_R	N_O (16) (INSTR.)	N_A (X)	N_R	N_R	N_R
		0	0	0	0							
		RT 5 OF N_A (X)	N_O (16)	RT 5 OF N_A (X)	N_A (X)							
	0											
	N_A (X)	RT 5 OF N_A (X)	0	RT 5 OF N_A (X)	N_A (X)	N_R	N_R	N_O (16)	N_A (X)	N_R	N_R	N_R

SB-54529-2

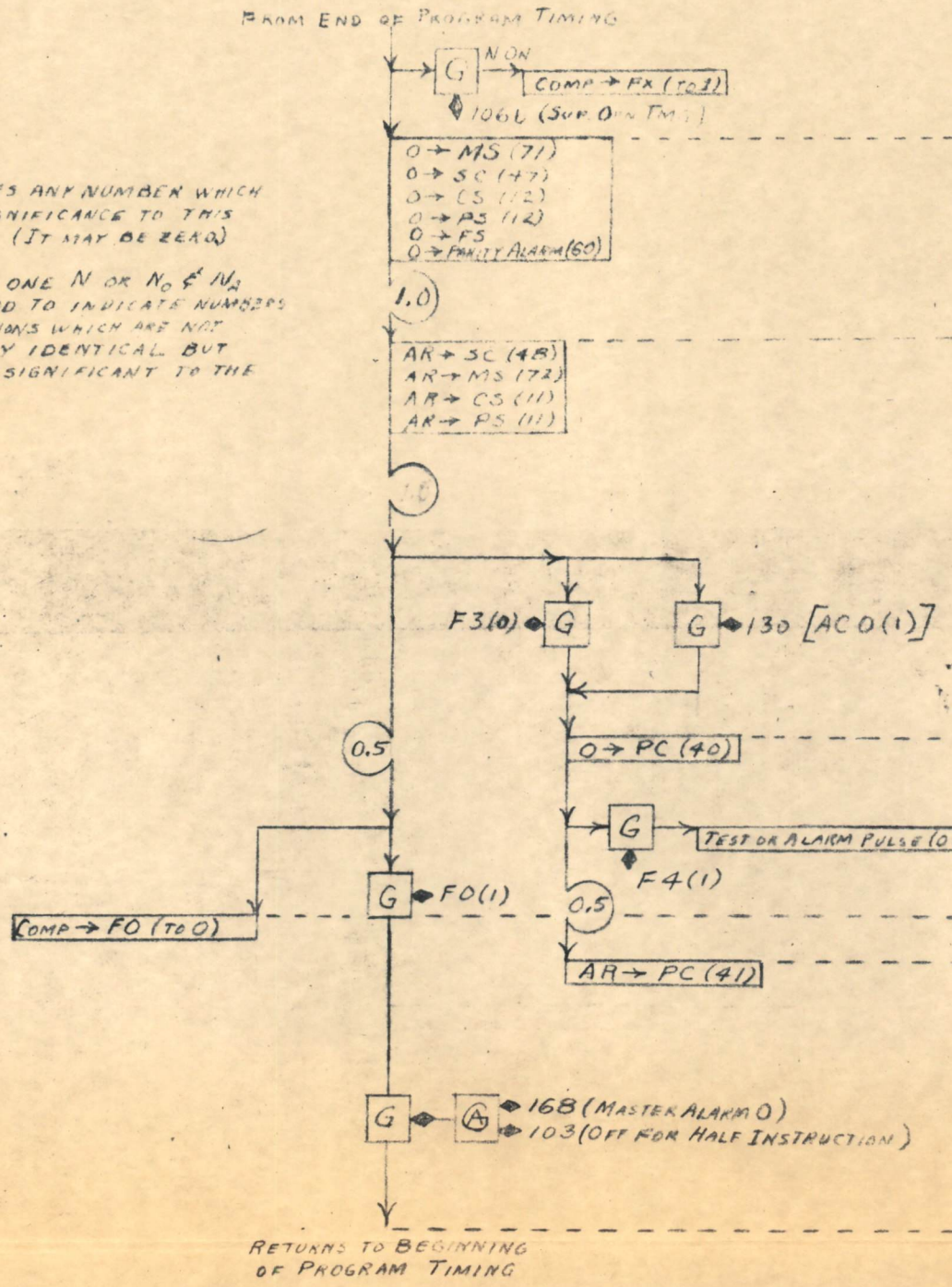
SB-54529-2

TRANSFER/PULSE
#17 (10001) tp x
OPERATION TIMING
MTC

ABBREVIATIONS:
O - CLEAR
N_P - PROGRAM ADDRESS
N_O - LEFT 5 DIGITS
N_A - RIGHT 11 DIGITS
N_R - ANY RANDOM NO.
N - $N_O + N_A$ (NO. OR INST.)

NOTES:

1. N_A INDICATES ANY NUMBER WHICH HAS NO SIGNIFICANCE TO THIS OPERATION. (IT MAY BE ZERO)
2. MORE THAN ONE N OR N_O & N_A MAY BE USED TO INDICATE NUMBERS OR INSTRUCTIONS WHICH ARE NOT NECESSARILY IDENTICAL BUT WHICH ARE SIGNIFICANT TO THE OPERATION.



ELAPSED TIME	PC RT 11	SC RT 5	CS LFT 6	PS RT 5	MS RT 11	SEL REG MM	LR	AR LFT 5	AR RT 11	AC LFT 5	AC RT 11	BR
0	N_P +1	N_P	0	N_P	N_P	N_R	N_R	N_O (17) (INSTR.)	N_A (X)	N_R	N_R	N_R
		0	0	0	0							
		RT 5 OF N_A (X)	N_O (17)	RT 5 OF N_A (X)	N_A (X)							
	0											
	N_A (X)	RT 5 OF N_A (X)	1	RT 5 OF N_A (X)	N_A (X)	N_R	N_R	N_O (17)	N_A (X)	N_R	N_R	N_R

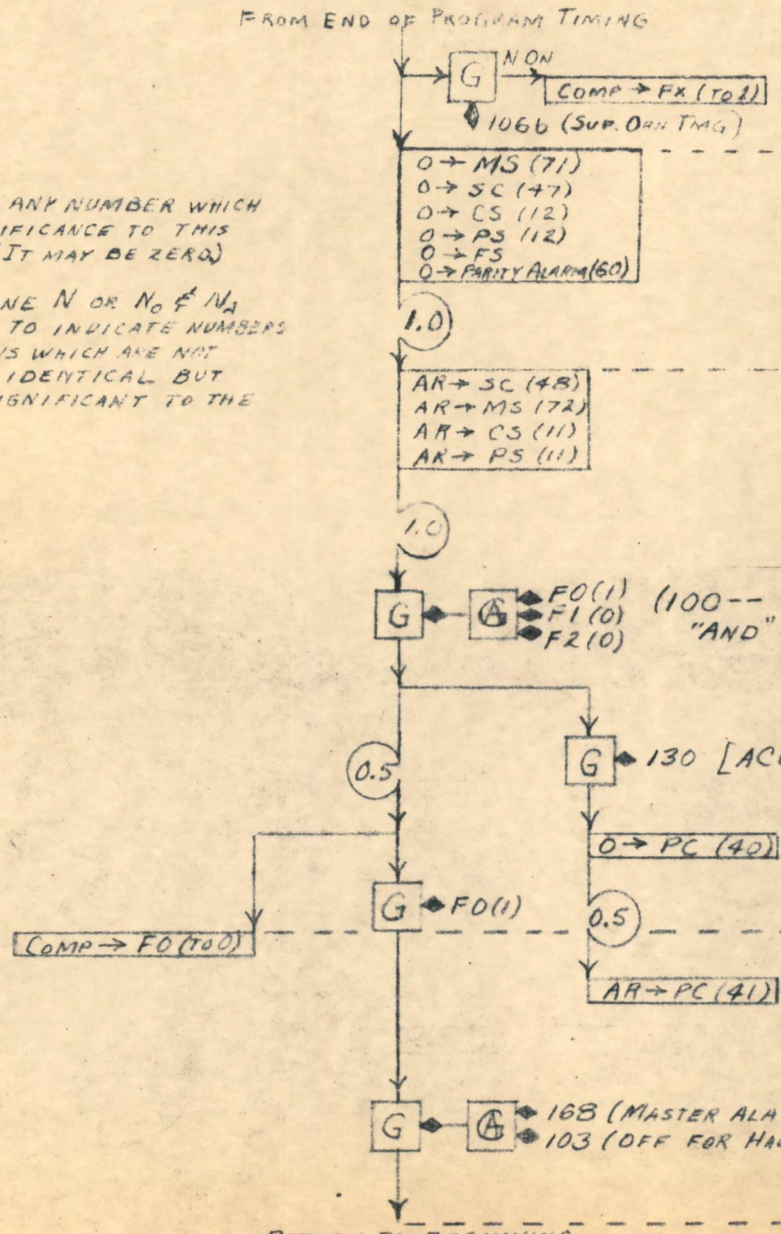
SB-54530-2 V

TRANSFER ON NEGATIVE #18 (10010) tn x OPERATION TIMING MTC

ABBREVIATIONS:
O - CLEAR
N_P - PROGRAM ADDRESS
N_O - LEFT 5 DIGITS
N_A - RIGHT 11 DIGITS
N_R - ANY RANDOM NO.
N - $N_O + N_A$ (N^1 OR INSTR.)

NOTES:

1. N_R INDICATES ANY NUMBER WHICH HAS NO SIGNIFICANCE TO THIS OPERATION. (IT MAY BE ZERO)
2. MORE THAN ONE N OR N_O & N_A MAY BE USED TO INDICATE NUMBERS OR INSTRUCTIONS WHICH ARE NOT NECESSARILY IDENTICAL BUT WHICH ARE SIGNIFICANT TO THE OPERATION.



ELAPSED TIME	PC RT 11	SC RT 5	CS LEFT 6	PS RT 5	MS RT 11	SEL REG MM	LR	AR LEFT 5	AR RT 11	AC LEFT 5	AC RT 11	BR
0	N_P +1	N_P	0	N_P	N_P	N_R	N_R	N_O (18) (INSTR)	N_A (X)	N_R	N_R	N_R
		0	0	0	0							
		RT 5 OF N_A (X)	N_O (18)	RT 5 OF N_A (X)	N_A (X)							
	0											
	N_A (X)		2									
	N_A (X)	RT 5 OF N_A (X)	2	RT 5 OF N_A (X)	N_A (X)	N_R	N_R	N_O (18)	N_A (X)	N_R	N_R	N_R

SD-54540-2

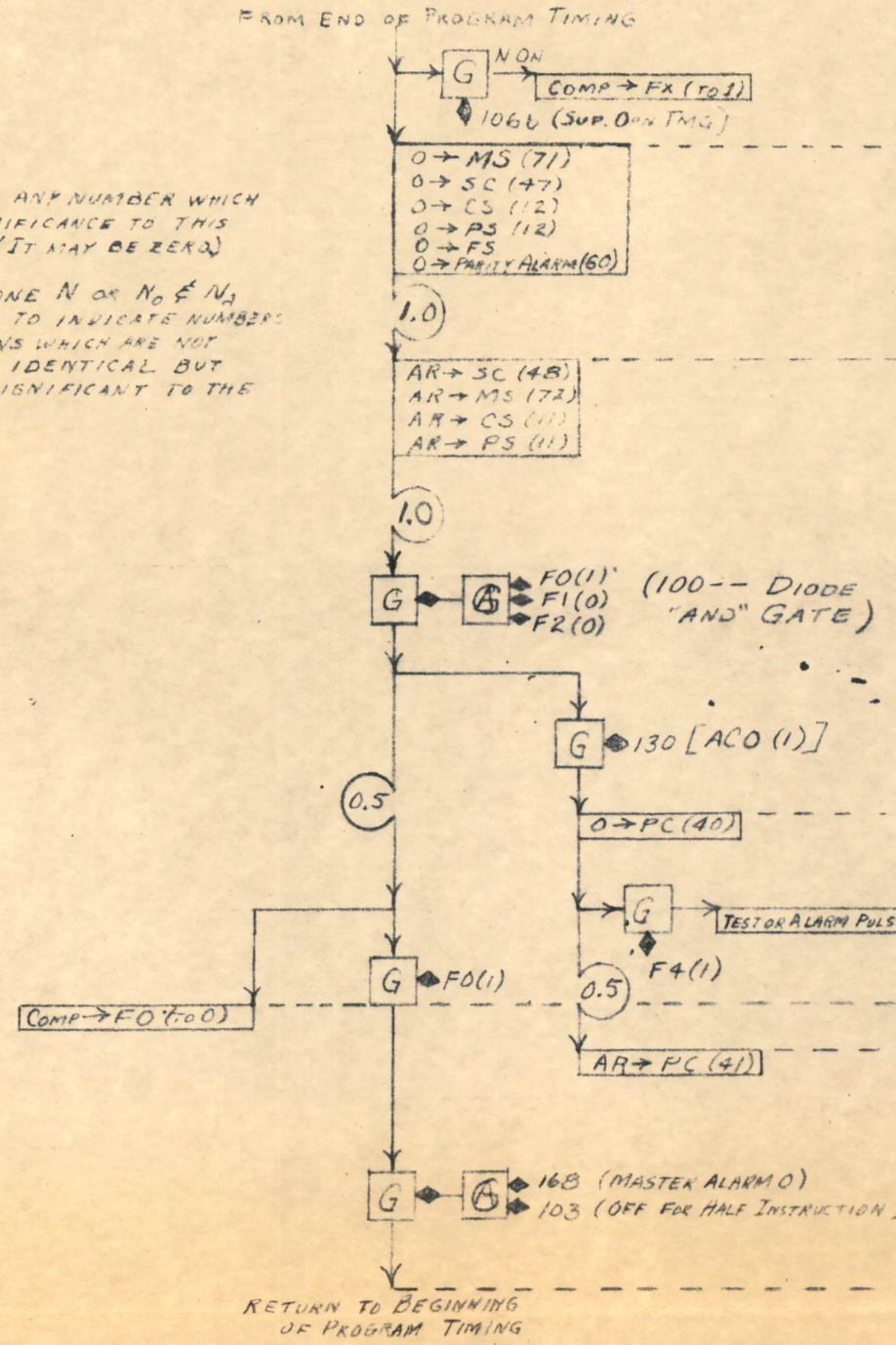
SD 54540-2V

TRANSFER ON NEGATIVE/PULSE
#19 (10011) npx
OPERATION TIMING
MTC

ABBREVIATIONS:
O - CLEAR
N_P - PROGRAM ADDRESS
N_O - LEFT 5 DIGITS
N_A - RIGHT 11 DIGITS
N_R - ANY RAM LOCATION No.
N - $N_O + N_A$ (N_O OR INSTR.)

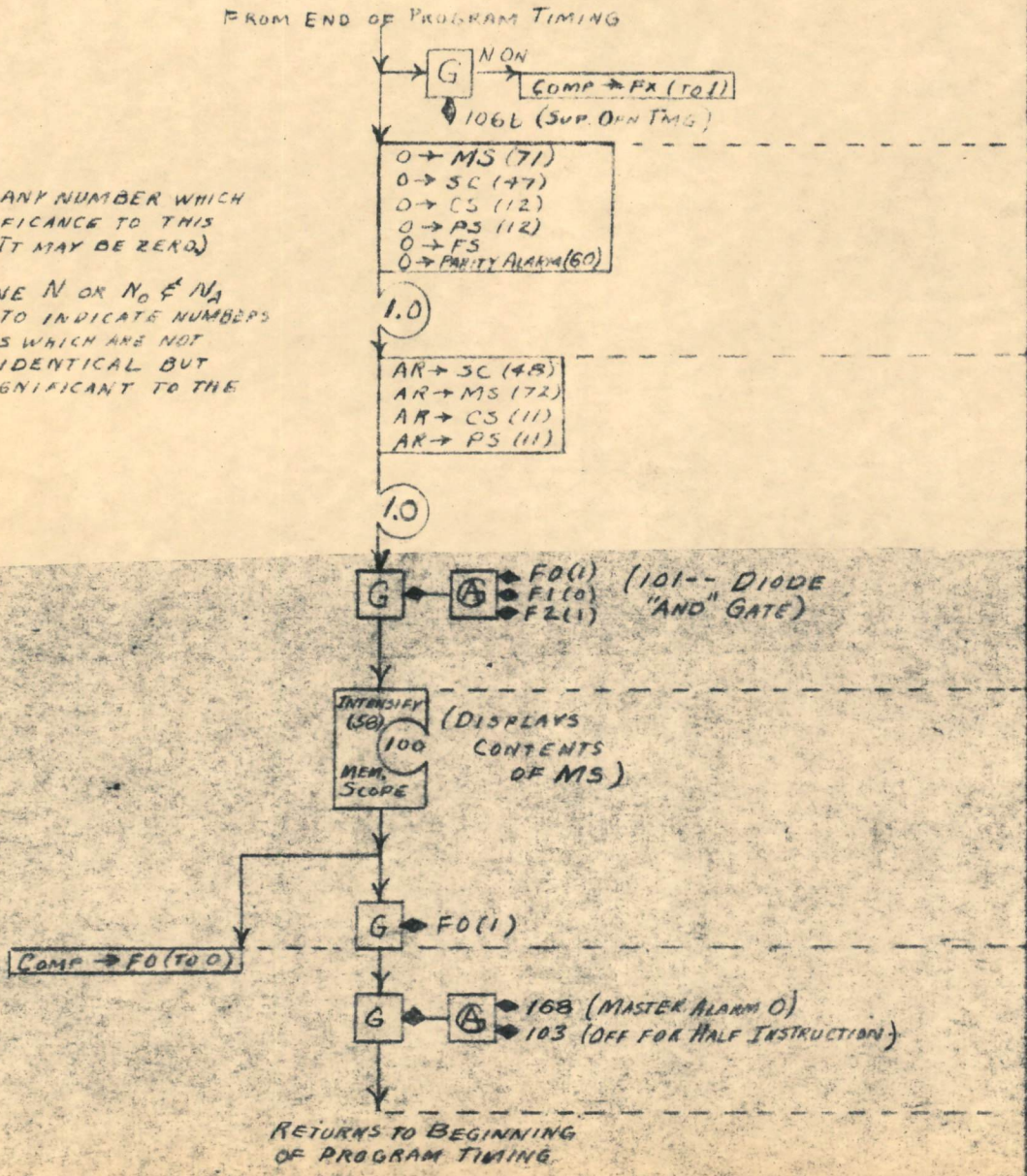
NOTES:

1. N_R INDICATES ANY NUMBER WHICH HAS NO SIGNIFICANCE TO THIS OPERATION. (IT MAY BE ZERO)
2. MORE THAN ONE N OR N_O & N_A MAY BE USED TO INDICATE NUMBERS OR INSTRUCTIONS WHICH ARE NOT NECESSARILY IDENTICAL BUT WHICH ARE SIGNIFICANT TO THE OPERATION.



ELAPSED TIME	PC RT 11	SC RT 5	CS LFT 6	PS RT 5	MS RT 11	SEL. REG. MM	LR	AR LFT 5	AR RT 11	AC LFT 5	AC RT 11	BR 1
0	N_P +1	N_P	0	N_P	N_P	N_R	N_R	N_O (19) (INSTR.)	N_A (X)	N_R	N_R	N_R
		0	0	0	0							
		RT 5 OF N_A (X)	N_O (19)	RT 5 OF N_A (X)	N_A (X)							
	0											
	N_A (X)	RT 5 OF N_A (X)	3	RT 5 OF N_A (X)	N_A (X)	N_R	N_R	N_O (19)	N_A (X)	N_R	N_R	N_R

MEMORY ADDRESS DISPLAY
#20 (10100) m d x
OPERATION TIMING
MTC



NOTES:

1. N_R INDICATES ANY NUMBER WHICH HAS NO SIGNIFICANCE TO THIS OPERATION. (IT MAY BE ZERO)
2. MORE THAN ONE N OR N_O & N_A MAY BE USED TO INDICATE NUMBERS OR INSTRUCTIONS WHICH ARE NOT NECESSARILY IDENTICAL BUT WHICH ARE SIGNIFICANT TO THE OPERATION.

ABBREVIATIONS:
O - CLEAR
N_P - PROGRAM ADDRESS
N_O - LEFT 5 DIGITS
N_A - RIGHT 11 DIGITS
N_R - ANY RANDOM NO.
N - $N_O + N_A$ (NO. OR INST.)

ELAPSED TIME	PC RT 11	SC RT 5	CS LFT 6	PS RT 5	MS RT 11	SEL. REG. MM	LR	AR LFT 5	AR RT 11	AC LFT 5	AC RT 11	BR
0	N_P +1	N_P	0	N_P	N_P	N	N_R	N_O (20) (INSTR)	N_A (X)	N_R	N_R	N_R
		0	0	0	0							
1.0		RT 5 OF N_A (X)	N_O (20)	RT 5 OF N_A (X)	N_A (X)							
1.0												
			4									
	N_P +1	RT 5 OF N_A (X)	4	RT 5 OF N_A (X)	N_A (X)	N	N_R	N_O (20)	N_A (X)	N_R	N_R	N_R

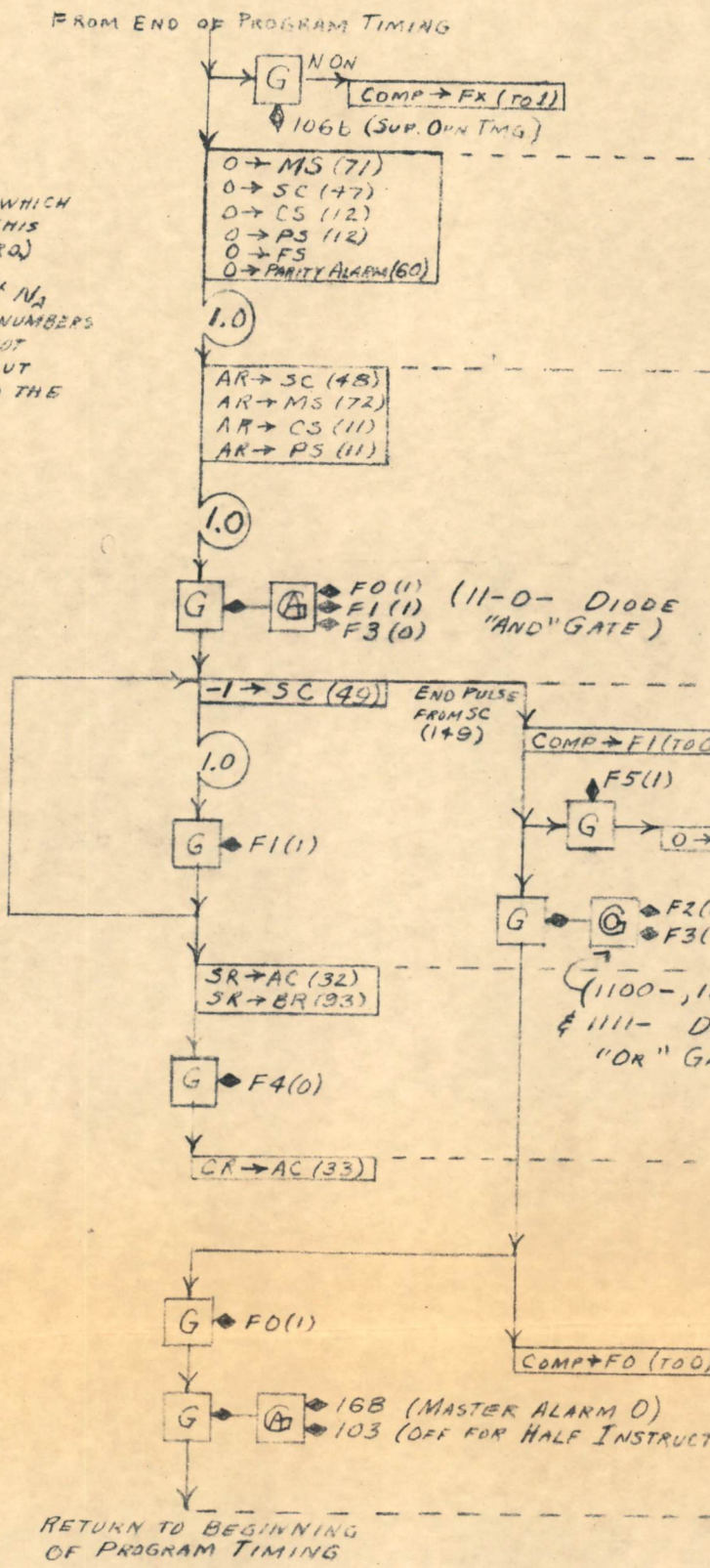
SB-5453-9-1

CYCLE RIGHT #24 (11000) CR n OPERATION TIMING MTC

ABBREVIATIONS:
O - CLEAR
N_P - PROGRAM ADDRESS
N_O - LEFT 5 DIGITS
N_A - RIGHT 11 DIGITS
N_R - ANY RANDOM NO.
N - N_O + N_A (N1 OR IN SEC.)

NOTES:

1. N_R INDICATES ANY NUMBER WHICH HAS NO SIGNIFICANCE TO THIS OPERATION. (IT MAY BE ZERO)
2. MORE THAN ONE N OR N_O & N_A MAY BE USED TO INDICATE NUMBERS OR INSTRUCTIONS WHICH ARE NOT NECESSARILY IDENTICAL BUT WHICH ARE SIGNIFICANT TO THE OPERATION.



ELAPSED TIME	PC RT 11	SC RT 5	CS LFT 6	PS RT 5	MS RT 11	SEL REG MM	LR	AR LFT 5	AR RT 11	AC LFT 5	AC RT 11	BR
0	N_P +1	N_P	0	N_P	N_P	N_R	N_R	N_O (24) (INSTR.)	N_A (n)	N_1		N_2
		0	0	0	0							
		RT 5 OF N_A (n)	N_O (24)	RT 5 OF N_A (n)	N_A (n)							
		n-1 TO 0	16 ON LAST CYCLE									
												0 IF F5(1) ON ON LAST CYCLE
												$N_1 \times 2^{-i}$ ($1 \le i \le n$) $N_2 \times 2^{-i}$ & RTi* DIGITS OF N_1
												RTi* DIGITS OF N_2
			0									
	N_P +1	0	0	RT 5 OF N_A (n)	N_A (n)	N_R	N_R	N_O (24)	N_A (n)	$N_1 \times 2^{-n}$ & RT n DIGITS OF N_2		$N_2 \times 2^{-n}$ & RT* DIGITS OF N_1

* THE DIGITS OF N_1 SHIFT OUT THE RT. END OF AC & INTO LEFT END OF BR.

THE DIGITS OF N_2 SHIFT OUT THE RT END OF BR & INTO LEFT END OF AC UPON CR → AC.

SB-5456-1

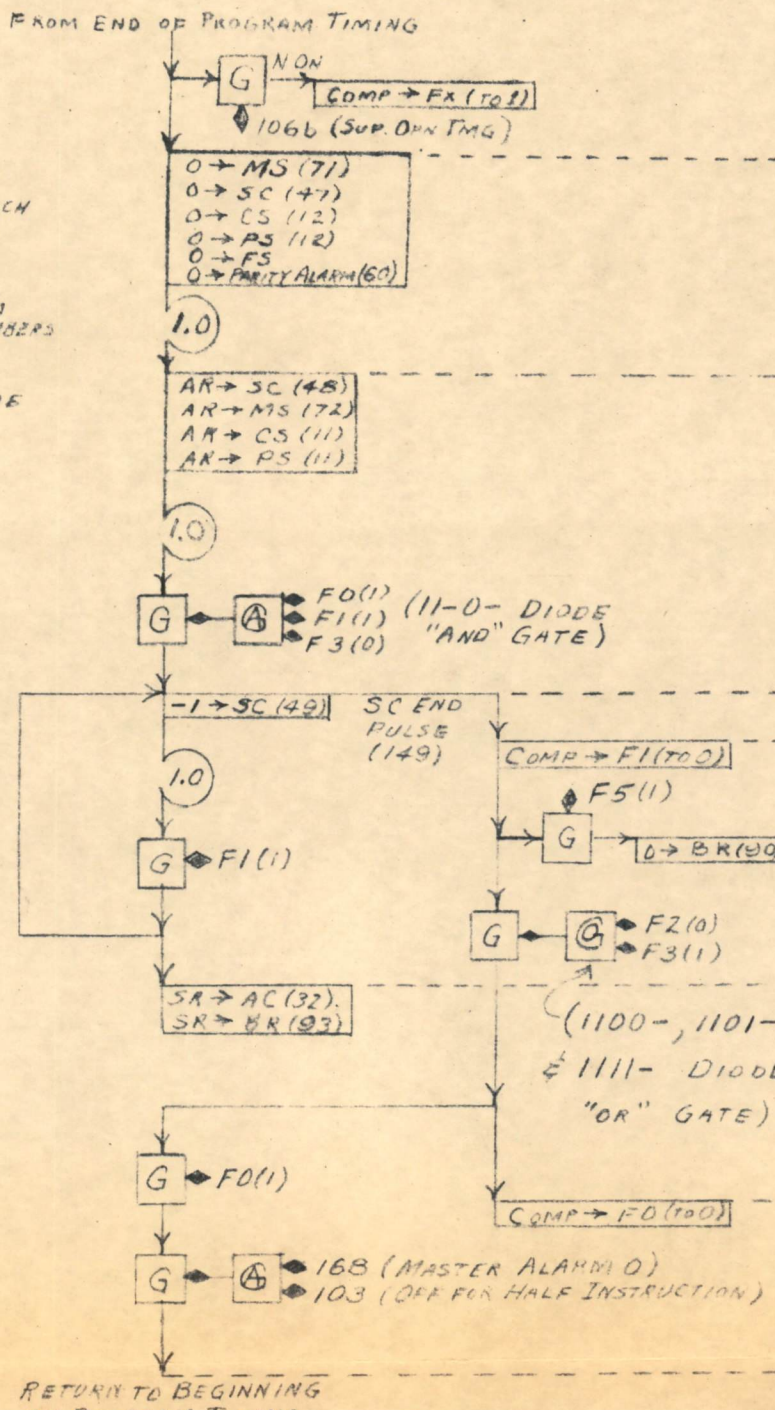
SB-5456-1

SHIFT RIGHT #25 (11001) SR n OPERATION TIMING MTC

ABBREVIATIONS:
O - CLEAR
N_P - PROGRAM ADDRESS
N_O - LEFT 5 DIGITS
N_A - RIGHT 11 DIGITS
N_R - ANY RANDOM NO.
N - $N_O + N_A$ (NO. OR INSTR.)

NOTES:

1. N_R INDICATES ANY NUMBER WHICH HAS NO SIGNIFICANCE TO THIS OPERATION. (IT MAY BE ZERO)
2. MORE THAN ONE N OR N_O & N_A MAY BE USED TO INDICATE NUMBERS OR INSTRUCTIONS WHICH ARE NOT NECESSARILY IDENTICAL BUT WHICH ARE SIGNIFICANT TO THE OPERATION.



ELAPSED TIME	PC RT 11	SC RT 5	CS LFT 6	PS RT 5	MS RT 11	SEL. REG. MM	LR	AR LFT 5	AR RT 11	AC LFT 5	AC RT 11	BR
0	N_P +1	N_P	0	N_P	N_P	N_R	N_R	N_O (25) (INSTR.)	N_A (n)	N_1		N_2
		0	0	0	0							
		RT 5 OF N_A (n)	N_O (25)	RT 5 OF N_A (n)	N_A (n)							
		n-1 TO 0	17 ON LAST CYCLE									0 IF F5(1) ON ON LAST CYCLE
										$N_1 \times 2^{-i}$ $(1 \le i \le n)$		$N_2 \times 2^{-i}$ & IFT * DIGITS OF N_1
	N_P +1	0	1 ...	RT 5 OF N_A (n)	N_A (n)	N_R	N_R	N_O (25)	N_A (n)	$N_1 \times 2^{-n}$ & SIGN DIGITS AT LEFT		$N_2 \times 2^{-n}$ & RT * DIGITS OF N_1

* THE DIGITS OF N_1 SHIFT OUT THE RT. END OF AC AND INTO LEFT END OF BR.

THE DIGITS OF N_2 SHIFT OUT THE RT. END OF BR AND ARE LOST

SB-54565-1

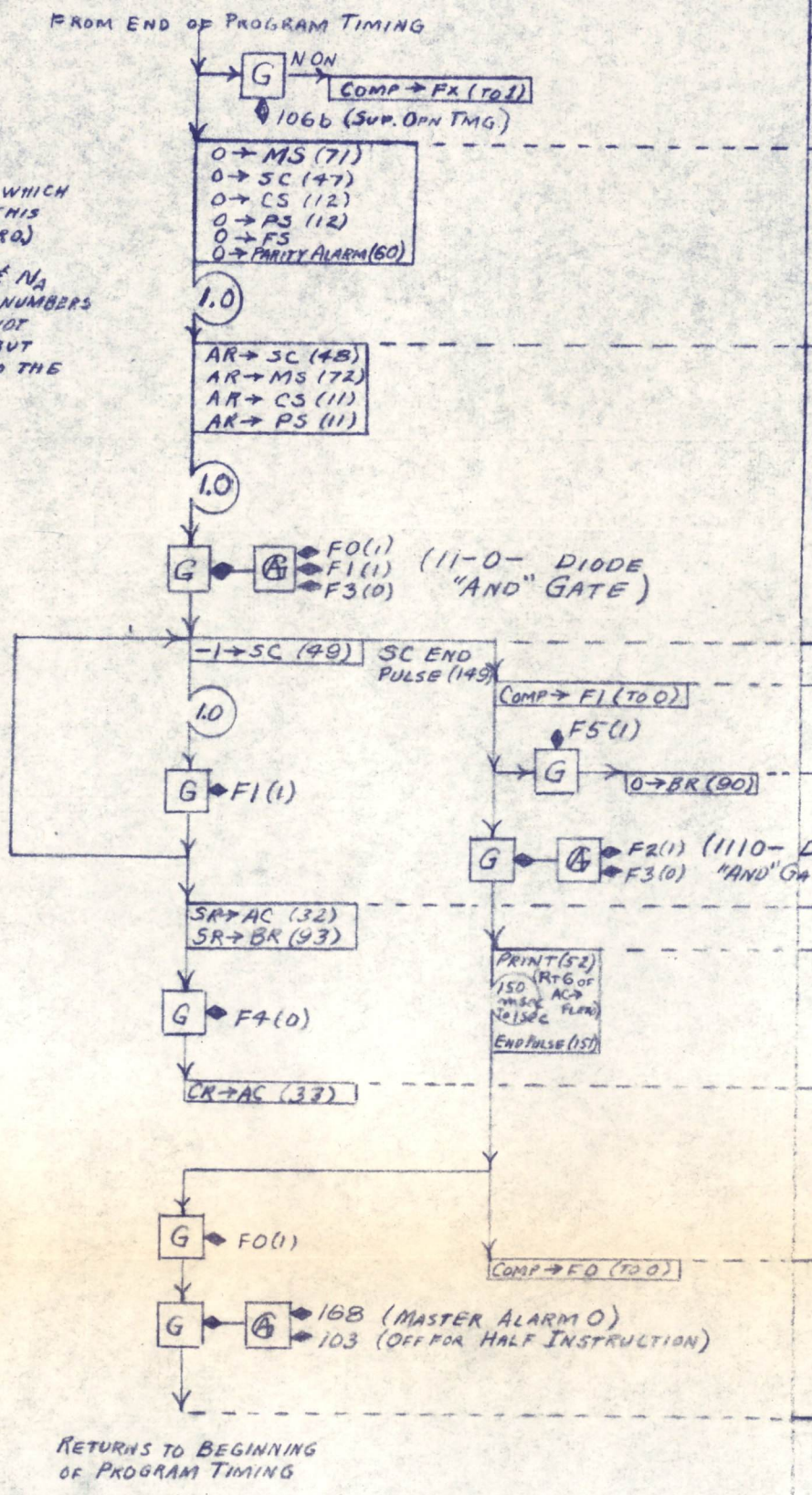
PRINT

#28 (11100) pr n
OPERATION TIMING
MTC

ABBREVIATIONS:
O - CLEAR
N_P - PROGRAM ADDRESS
N_O - LEFT 5 DIGITS
N_A - RIGHT 11 DIGITS
N_R - ANY RANDOM N_0:
N - $N_O + N_A$ (NO. OR INST.)

NOTES:

1. N_R INDICATES ANY NUMBER WHICH HAS NO SIGNIFICANCE TO THIS OPERATION. (IT MAY BE ZERO.)
2. MORE THAN ONE N OR N_O & N_A MAY BE USED TO INDICATE NUMBERS OR INSTRUCTIONS WHICH ARE NOT NECESSARILY IDENTICAL BUT WHICH ARE SIGNIFICANT TO THE OPERATION.



ELAPSED TIME	PC RT 11	SC RT 5	CS LFT 6	PS RT 5	MS RT 11	SEL REG MM	LR	AR LFT 5	AR RT 11	AC LFT 5	AC RT 11	BR
0	N_P +1	N_P	0	N_P	N_P	N_R	N_R	N_0 (28) (INSTR.)	N_A (11)	N_1		N_2
		0	0	0	0							
		RT 5 OF N_A (11)	N_0 (28)	RT 5 OF N_A (11)	N_A (11)							
		n-1 → 0										
			20 ON LAST CYCLE									0 IF F5(1) ON ON LAST CYCLE
										$N_1 \times 2^{-L}$ (16 ≤ n)		$N_2 \times 2^{-L}$ & RT L * DIGITS OF N_1
										RT L * DIGITS OF N_2		
			4									
	N_0 +1	0	4	RT 5 OF N_A (11)	N_A (11)	N_R	N_R	N_0 (28)	N_A (11)	$N_1 \times 2^{-n}$ & RT n DIGITS OF N_2		$N_2 \times 2^{-n}$ & RT n * DIGITS OF N_1

* THE DIGITS OF N_1 SHIFT OUT THE RT. END OF AC AND INTO THE LEFT END OF BR.

THE DIGITS OF N_2 SHIFT OUT THE RT. END OF BR AND INTO THE LEFT END OF AC UPON CR → AC.

SB-54566-1

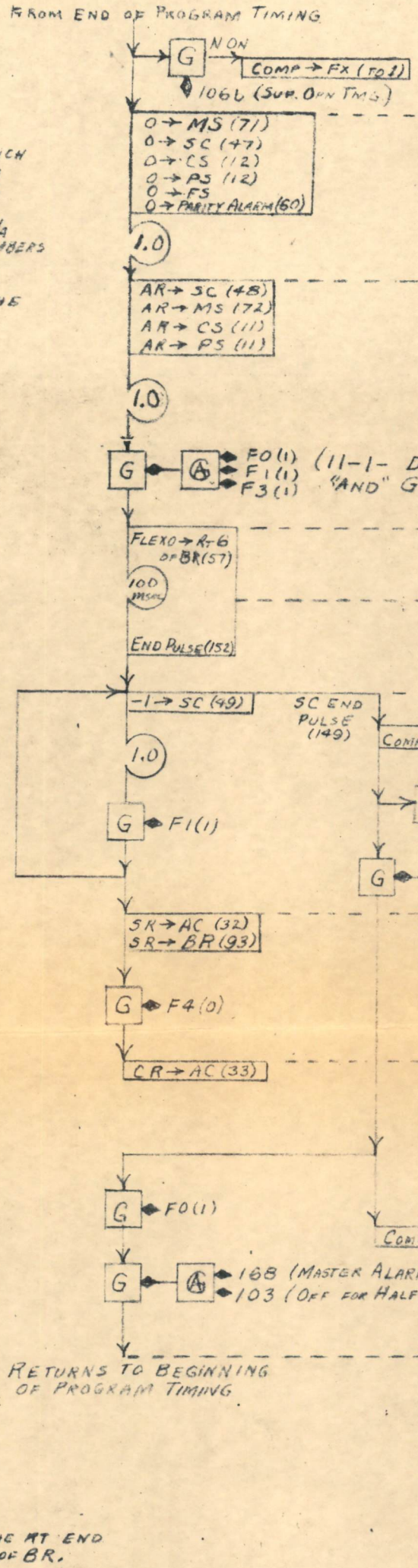
SB-54566-1

READ IN #30 (11110) 'ri m OPERATION TIMING MTC

ABBREVIATIONS:
O - CLEAR
N_P - PROGRAM ADDRESS
N_O - LEFT 5 DIGITS
N_A - RIGHT 11 DIGITS
N_R - ANY RANDOM NO.
N_{R_L} - LEFT N_R CONTENT

NOTES:

1. N_A INDICATES ANY NUMBER WHICH HAS NO SIGNIFICANCE TO THIS OPERATION. (IT MAY BE ZERO)
2. MORE THAN ONE N OR N_O & N_A MAY BE USED TO INDICATE NUMBERS OR INSTRUCTIONS WHICH ARE NOT NECESSARILY IDENTICAL BUT WHICH ARE SIGNIFICANT TO THE OPERATION.



ELAPSED TIME	PC RT 11	SC RT 5	CS LEFT 6	PS RT 5	MS RT 11	SEL Hdg MM	LR	AR LEFT 5	AR RT 11	AC LEFT 2	AC RT 11	BR	
0	N_P +1	N_P	0	N_P	N_P	N_R	N_R	N_O (30) (INSTR.)	N_A (n)	N_R	N_R		5671-1
		0	0	0	0								
		RT 5 OF N_A (n)	N_O (30)	RT 5 OF N_A (n)	N_A (n)								
													N
										$N_R \times 2^{-L}$ ($1 \le L \le n$)			N $\times 2^{-L}$ & RT L * DIGITS OF N_R
													O (FS MUST BE 0 TO AVOID THIS)
										RT L * DIGITS OF N			
	N_P +1	0	6	RT 5 OF N_A (n)	N_A (n)	N_R	N_R	N_O (30)	N_A (n)	$N_R \times 2^{-n}$ & RT n DIGITS OF N			N $\times 2^{-n}$ & RT n DIGITS OF N_R

n-1 TO 0

22 ON LAST CYCLE

6

* THE DIGITS OF N_R SHIFT OUT THE RT END OF AC AND INTO THE LEFT END OF BR.

THE DIGITS OF N SHIFT OUT THE RT END OF BR AND INTO THE LEFT END OF AC UPON CR → AC.

SB-5456 71-1

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: FINAL SPECIFICATIONS OF THE HIGH-SPEED FLIP-FLOP

To: All Group 62 Engineers

From: Hal Boyd

Date: May 12, 1953

Abstract: In this E-note is presented a collection of data serving to define the operating characteristics of the WWII High-Speed Flip-Flop. The flip-flop was designed from the "Normalized Flip-Flop Chart" (E-525) and a "Flip-Flop tolerance Chart" (yet unpublished) for high-speed high-reliability operation to drive either or both diode logic and gate-tubes. A circuit schematic of the High-Speed Flip-Flop is shown in Figure 1, attached.

1.0 Output Waveform Specifications

Figure 2 shows the output waveform specifications that are required of the High-Speed Flip-Flop to drive gate-tubes and diode-logic. Due to diode back-voltage limits, and the need for large voltage swings for diode-logic speed, both output levels of the flip-flop have to be guaranteed within tight limits. The voltage levels chosen for diode-logic applications are +10 and -30 volts.

It has been recently demonstrated that positive suppressor voltages (about +10) yield better performance from 7AK7 gate-tubes than a zero suppressor voltage. As the cut-off of the 7AK7 gate-tube is about -15 volts, and the flip-flop's lower level is -30 volts, the flip-flop is fairly universal for WWII applications. When driving gate-tubes, moreover, powerful cathode-followers can be used since climbing of levels can be tolerated.

As the maximum speed of operation in WWII will be 2 megacycles, the total transition time to -15 volts or -30 volts, depending on the load, cannot exceed 0.5 μsec. For gate-tube counting applications, however, it is desirable that the flip-flop have a delay equal to or greater than the pulse width before the upper level (+10 volts) is changed, and the lower level climbs to cut-off of the gate tube (-15 volts). Diode applications, on the other hand, dictate rise and fall times between .2 and .3 μsec. There

exists, moreover, another complication inasmuch as the upper-level delay is a function of trigger amplitude and pulse-width. As 10 to 40 volt .08 to .12 μsec triggers are desirable the delay for 10 volt triggers must be at least .12 μsec and the delay for 40 volt triggers must not exceed a value that, together with a fall time between .2 and .3 μsec, would cause a total transition time greater than .5 μsec.

Delays in a flip-flop of this type are inherent and are a function of rise time, stability factor, cathode-stiffness, and trigger amplitude and width (output levels being constant). The delay to -15 volts cannot be made sufficiently greater than the pulse width, without contradicting the other specifications, unless a low stability factor is used, which will result in poor reliability. There is but one unique flip-flop of this type that will satisfy all requirements fully. By proper choice of rise-time and cathode-stiffness, all requirements were met without sacrificing reliability, although the delay to -15 volts is just equal to the nominal (.1 μsec) pulse width. For greater pulse widths (.12 μsec) there should not be sufficient noise output, if any at all, from the 7AK7 gate-tube due to its low transconductance in the suppressor bias neighborhood of -15 volts, and due to the pulse being small at that time.

2.0 P.R.F. Response Characteristics (vs pulse width)

The curves shown in Figure 3 were obtained by complementing the flip-flop with a continuous train of positive half-sine pulses of variable width, amplitude, and repetition frequency, and observing at different frequencies the minimum amplitude of .08, .1, and .12 μsec pulses that would allow successful operation of the flip-flop. The curves define the transition from the region of either inoperation or frequency division to the region of proper operation under continuous operation at that frequency. Although there is a slight rise in the curves from 1 mc up to 2 mc, it requires 4 to 5 μsec bursts to acquire the total rise.

The point labeled "-15 volt noise level" defines the maximum noise pulse of trigger width that can be considered to be "ignored" by the flip-flop. With this pulse amplitude (with a .12 μsec width), the lower output-voltage level of the flip-flop climbs to -15 volts (cut-off of 7AK7 gate-tubes) without triggering the flip-flop. For shorter pulse widths the flip-flop will "ignore" larger pulse amplitudes.

The curves suggest that the trigger area or pulse-width-amplitude product necessary for operation is constant at any given frequency; i.e., the pulse width-amplitude product is .8 volt-μsec up to 1 mc, and 1 molt-μsec at 2 mc. For short 2 mc bursts the product would be between .8 and 1 volt-μsec.

3.0 P.R.F. Response Characteristics (vs load)

The response curves in Figure 4 were taken in much the same manner as those of Figure 3, except that .1 μsec pulses were used, and both flip-flop outputs were capacitively loaded. Applying the pulse width-amplitude product rule, prf curves for pulse-widths differing from .1 μsec can be approximated.

4.0 Capacitive Load Characteristics

The criteria determining the maximum capacitive load of which the flip-flop is capable of driving, in this case, is the transition time to -15 volts and/or -30 volts depending upon whether only gate-tubes or both gate-tubes and diode-logic are to be driven. The transition time cannot exceed .5 μsec to whichever level is the limiting factor, under the most adverse input conditions of 40 volt .12 μsec complement triggers.

The curves shown in Figure 5 show that the maximum gate-tube load when driving gate-tubes only is about (6) 7AK7 gate-tubes per side [(1) 7AK7 gate tube $\cong$ 15 μμf]. For driving both gate-tubes and diode-logic, on the other hand, the flip-flop can drive no more than (2) gate-tubes per side, when the whole swing is required.

5.0 "And" Gate Load Characteristics

The Figure 6 curves define the output waveform characteristics of the flip-flop when driving & gates, and is for universality plotted against the & gate current delivered to the flip-flop during the time its output level is down. The maximum & gate current per flip-flop side is about 3 ma, both from a standpoint of transition time and overall flip-flop stability. Again, these curves were taken under the most adverse input conditions, although the marginal checking parameter curve was taken at trigger inputs of 20 volts.

6.0 Low I_b Tube Characteristics

The worst combination of tube sides for the flip-flop tube is with one side of high I_b and the other of low I_b. The most critical effects of a low I_b tube are the output voltage levels, E_o, the flip-flop tube's cathode voltage, E_k, the "on" tube's grid voltage, $E_{g\ on}$, and the "off" tube's grid voltage, $E_{g\ off}$, when the low I_b side is conducting. These voltages affect the overall stability of the flip-flop. The manner in which these voltages vary as one tude side's I_b varies is shown in Figure 7, where all but E_o is measured from the negative supply level.

The I_b of the tube side in question was varied by its filament voltage. In the experiment, provision was made for switching the tube side from a tube testing circuit to the flip-flop circuit, while switching appropriate voltages. At each filament voltage the I_b of the tube side at 120 volts E_b and 0 volts E_c was measured, and, at that same filament voltage setting, the behavior of the tube in the flip-flop was noted and the critical voltages were measured.

Note that the flip-flop behaves like a "one-horse-shay" with respect to tubes, and doesn't fall apart until tubes having but 40% of average I_b (60% down) are used.

7.0 Marginal Checking Curves and Tolerances

Figures 8 through and including 15 were obtained by varying, one at a time, all components of the flip-flop and measuring and plotting the variations in the marginal checking parameters necessary to cause failure of the flip-flop to count at an audio rate (2 Kc) with 20 volt complement triggers.

While varying any one component, all others were held within the limits specified in Figure 1. The marginal checking voltages were taken with respect to the negative (-150 v.) supply. The curves labeled "ss" (same side) were obtained by inserting the marginal checking parameter at the grid of the flip-flop tube side whose compenent was varied, while those labeled "os" (opposite side) are for the opposite grid.

For large voltage changes in the marginal checking parameter, its effect on the circuit was divided down by inserting the marginal check voltage through a resistor to the flip-flop tube's grids. The resistor was of such a size that in parallel with the divider's grid-resistor and returned to the negative supply, the combination yields the design center divider grid resistor (see Figure 1). In this experiment a 50 volt marginal checking voltage change inserts a change of 7.4 volts on the flip-flop tube's grid.

The marginal checking curves contain notes and legends which should make themselves self-explanatory. In addition, component tolerances are indicated on the charts. Figure 16 shows the effect of trigger amplitude on the marginal checking parameters, which together with day to day supply variations and initial unbalances accounts for some of the slight differences between charts. These differences however, are not important as the basic purpose of the charts is to demonstrate the effectiveness of the method of marginal checking, and to show the manner in which failure is reached. Failure points were determined independent of the marginal checking parameters.

8.0 Divider tolerance vs trigger amplitude

Figure 17 shows the manner in which divider-resistor tolerances vary with the input trigger amplitude. The flat horizontal portions of the curves define the resistor values that, without input triggers, cause the flip-flop to switch from one state to another. These so-called d-c tolerances cannot be exceeded. The sharp transition to the flat portions can probably be best explained by the tendency of the flip-flop to reach its apparent stability factor of about 7 but is caught at a stability factor of about 4.7. Thus as the stability factor is clamped, the tolerances are clamped.

The experimentally determined flat-portion tolerances check very closely with the calculated values. The calculations are shown below using formulas derived by the author some time ago and not derived again due their simplicity.

$$+\frac{\Delta R_g}{R_g} = \frac{S-1}{S} \cdot \frac{S + \mu_o E_o'}{(1 + \mu_o) - (S + \mu_o E_o')} \qquad (1)$$

$$-\frac{\Delta R_g}{R_g} = \frac{S-1}{S} \cdot \frac{S + \mu_o E_o'}{S + \mu_o E_o' + \mu_o} \qquad (2)$$

$$+\Delta R/R = \frac{(-\Delta R_g/R_g)}{1 - (-\Delta R/R_g)} \qquad (3)$$

$$-\Delta R/R = \frac{(+\Delta R_g/R_g)}{1 + (+\Delta R_g/R_g)} \qquad (4)$$

where R_g is the bottom divider resistor,

R is the top divider resistor,

S is the stability factor (see E-525), and is 4.65 for this flip-flop,

E_o' is the Normalized Output (see E-525), and is .25 for this flip-flop

and μ_o is the cutoff μ of the flip-flop tube, and is about 30 for Bogie 5965's.

Inserting the proper values of S, μ_o and E_o' in equations 1 and 2 yields tolerances of 50% and -23% respectively for the lower resistor. Inserting these tolerances in equations 3 and 4 yields tolerances of 30% and -33% respectively for the upper resistor.

Signed H. W. Boyd
H. W. Boyd

HWB/cs

Approved R. L. Best
R. L. Best, Section Leader

Drawings Attached:

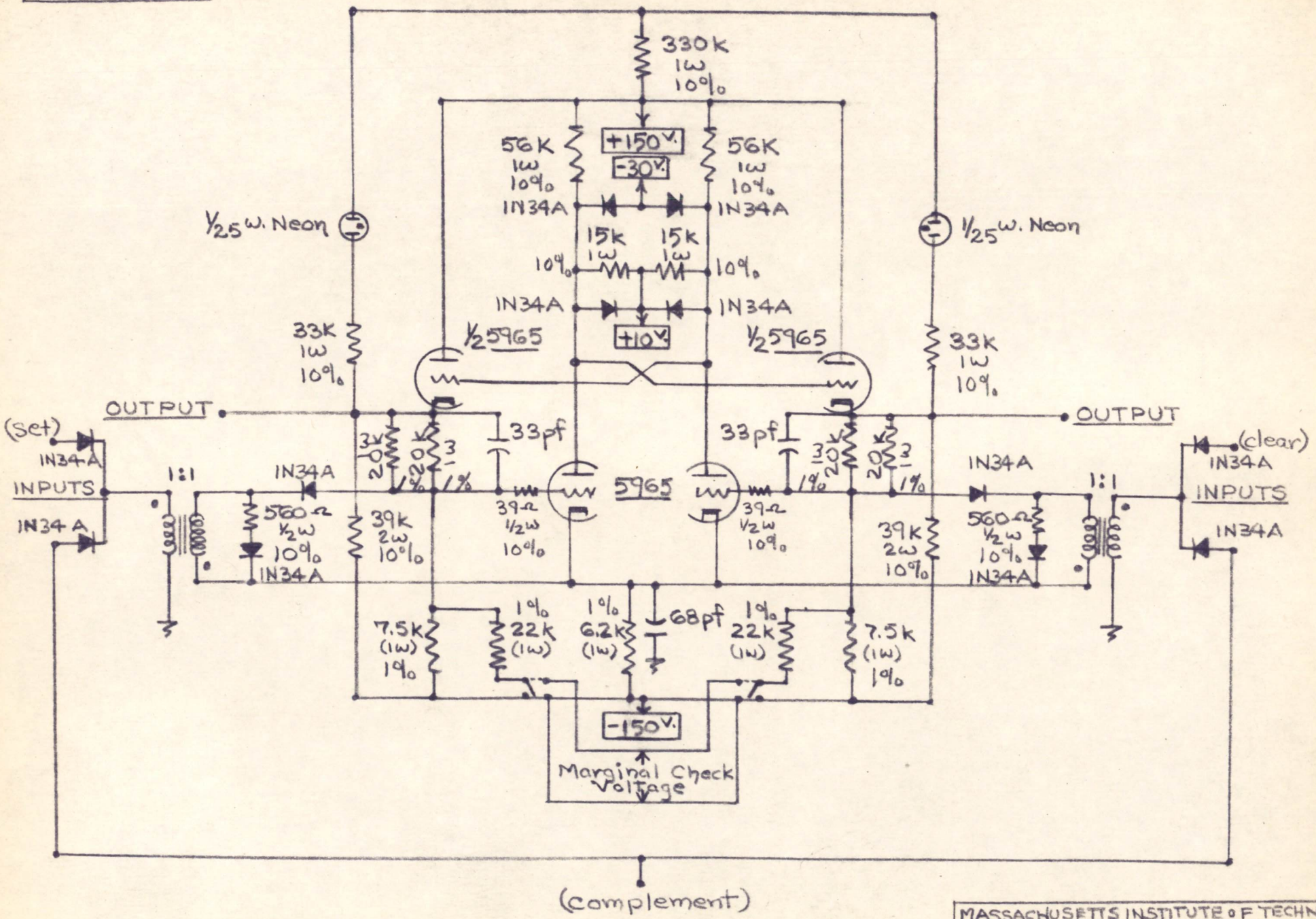
SA-54947
SA-48421-G to
SA-48435-G inclusive
SA-48441-G

Approved N. H. Taylor
N. H. Taylor, Group Leader

cc: (vellum copies) to D.J. Crawford, N.P. Edwards, and H. Ross at IBM via Kromer.

SA-54947

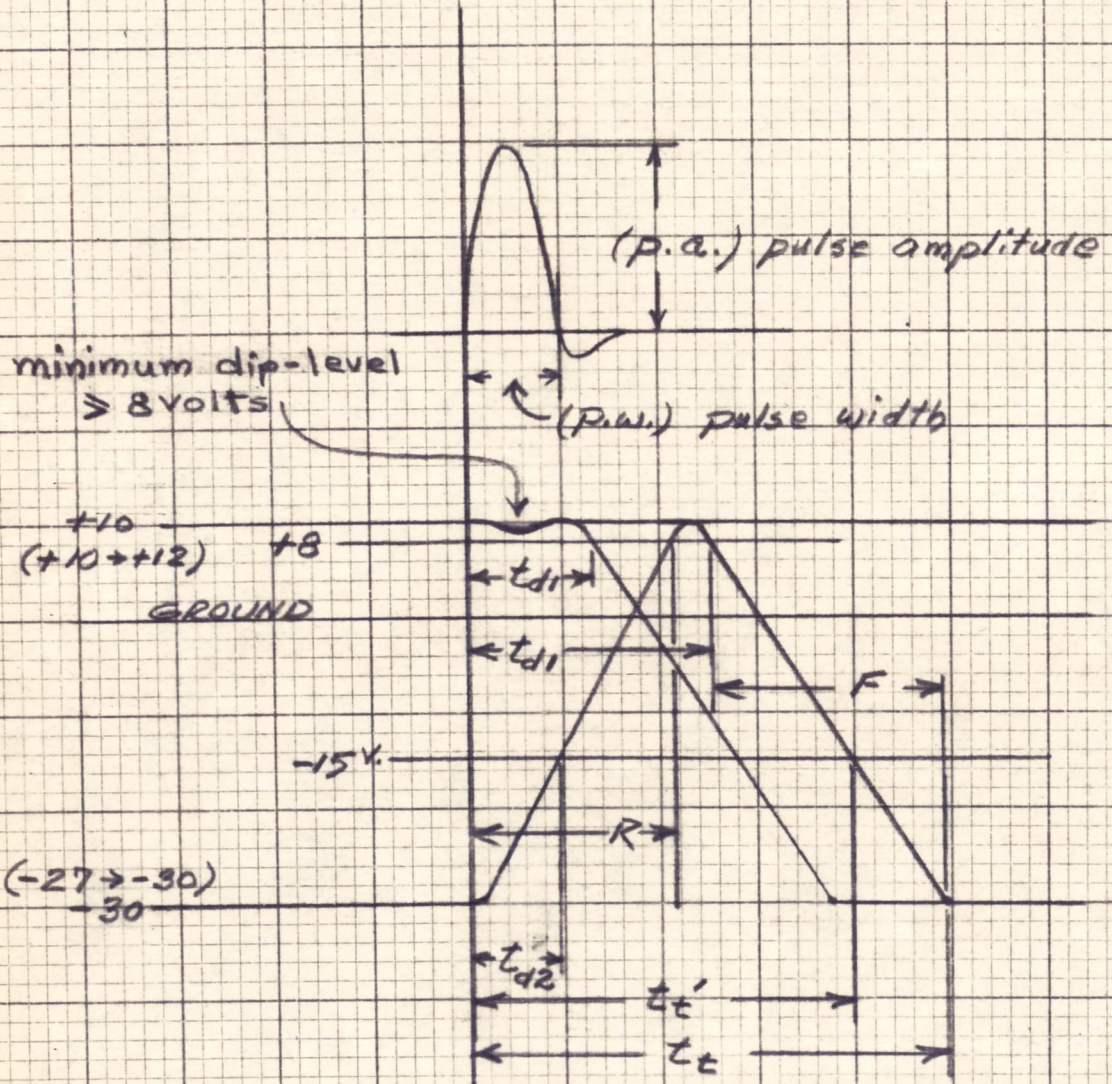
HIGH-SPEED WWII FLIP-FLOP



MASSACHUSETTS INSTITUTE OF TECHNOLOGY PROJECT LINCOLN		
DIC. NO.	DR. 5-15-53 Hal. Boyd	CK.
ENG. 5-15-53 Hal. Boyd	APP.	SA-54947

SA-48421-6

FIGURE 2 - OUTPUT WAVEFORM SPECIFICATIONS



1) For this input range:

≈ 10 V. $\leq$ p.a. $\leq$ 40 V.
.08 μs. $\leq$ p.w. $\leq$ .12 μsec.

2) The output shall be within the following:

p.w. $\leq t_{d_1} \leq$ .25 μs. (complement)
p.w. $\leq t_{d_1} \leq$ .20 μs. (set & clear)

$t_{d_2} \cong$ p.w.

$T_t \leq$ .5 μsec. } depending on kind of load
$T_t' \leq$ .5 μsec. }

$\approx .2 \leq F$ } depending on load & consistent with above specs.
$\approx .2 \leq R$ }

HJB

SA-48421-6

1/1

359-61G KEUFFEL & ESSER CO.
Semi-Logarithmic, 2 Cycles × 10 to the inch.
5th lines accented.
MADE IN U. S. A.

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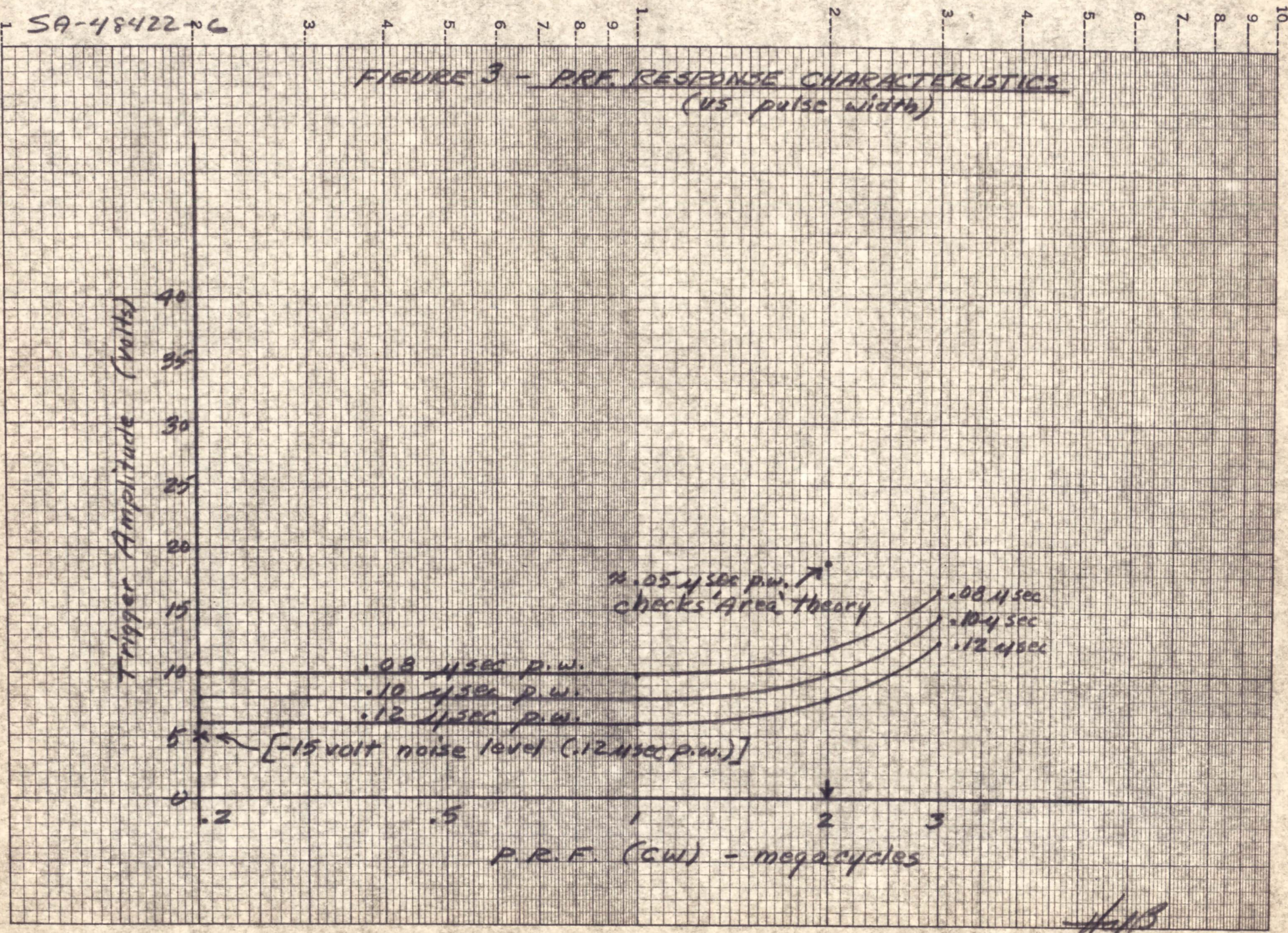
FIGURE 3 - PRF. RESPONSE CHARACTERISTICS (VS pulse width)



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SA-18423-6

FIGURE 4 - PRF RESPONSE CHARACTERISTICS (vs load)

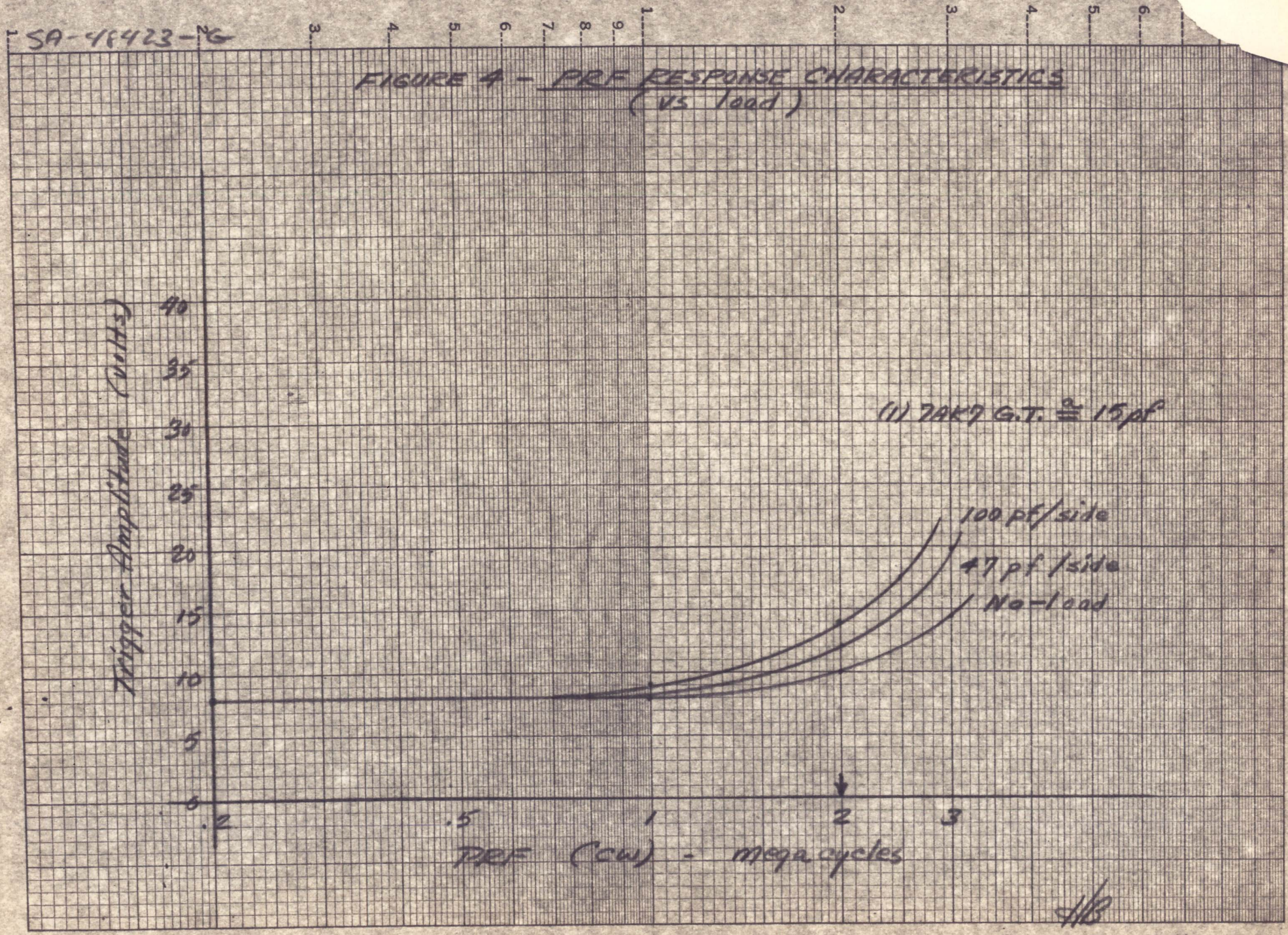

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FIGURE 5 – CAPACITIVE LOAD CHARACTERISTICS

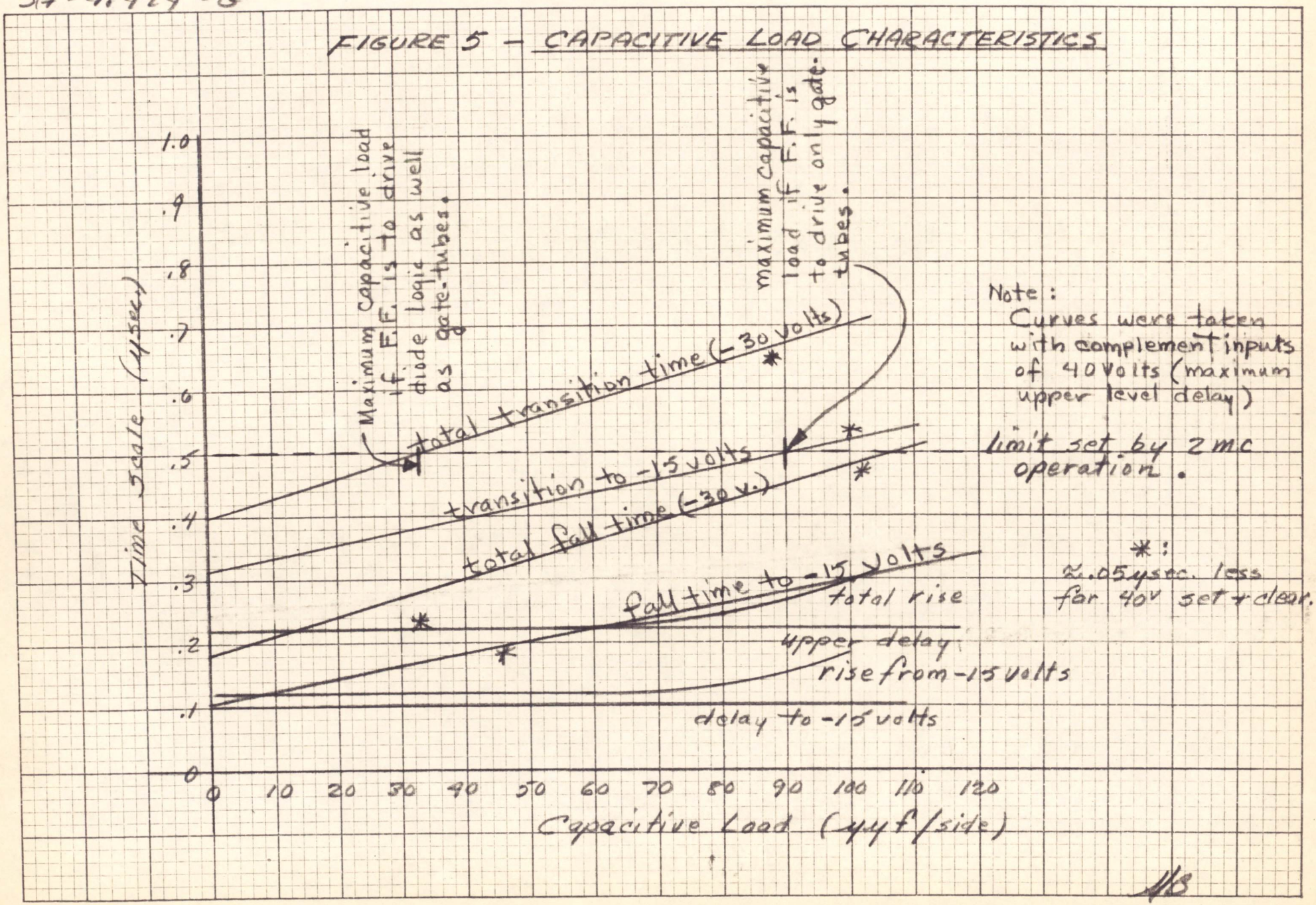

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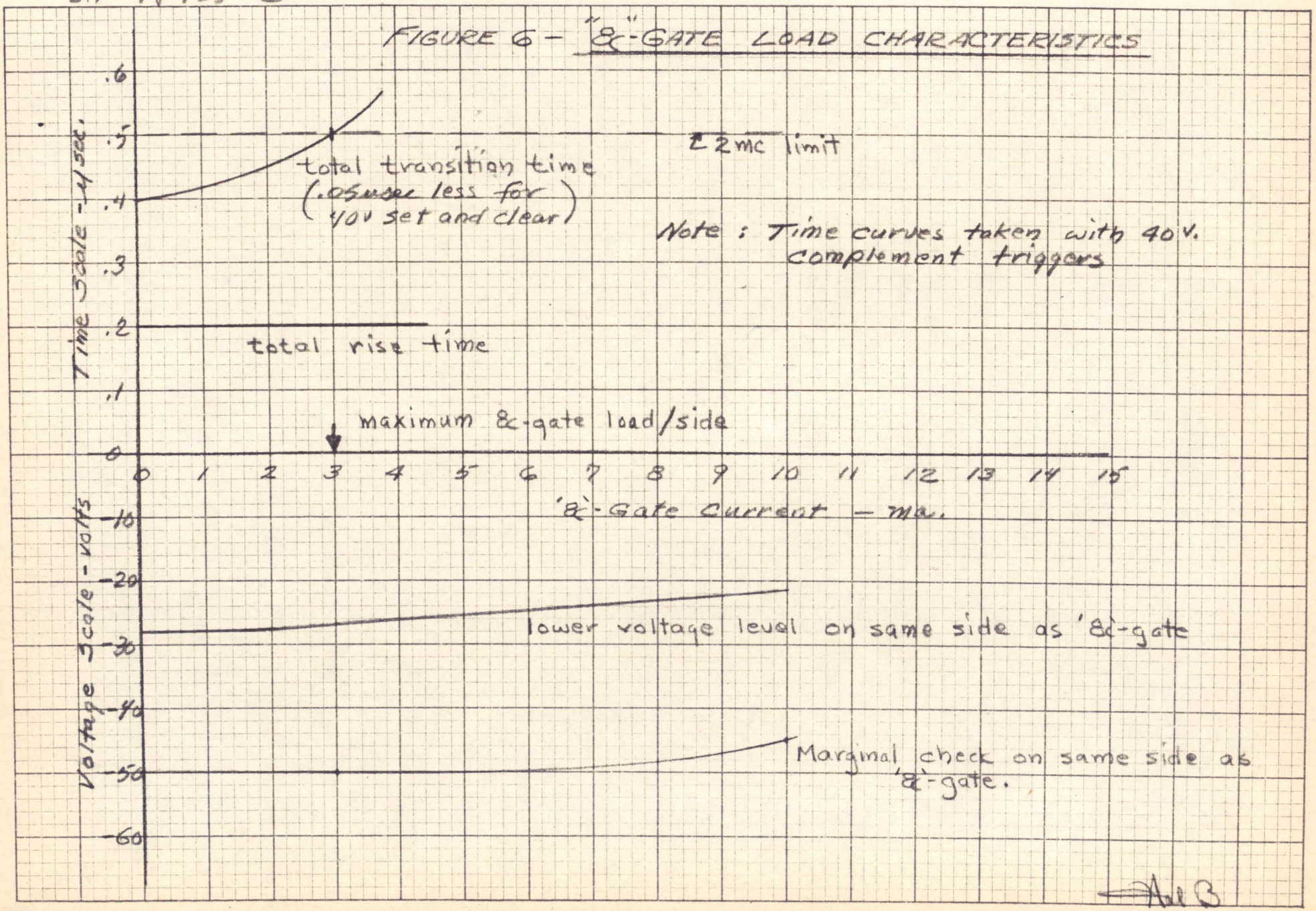
FIGURE 6 - "&"-GATE LOAD CHARACTERISTICS



Ad B

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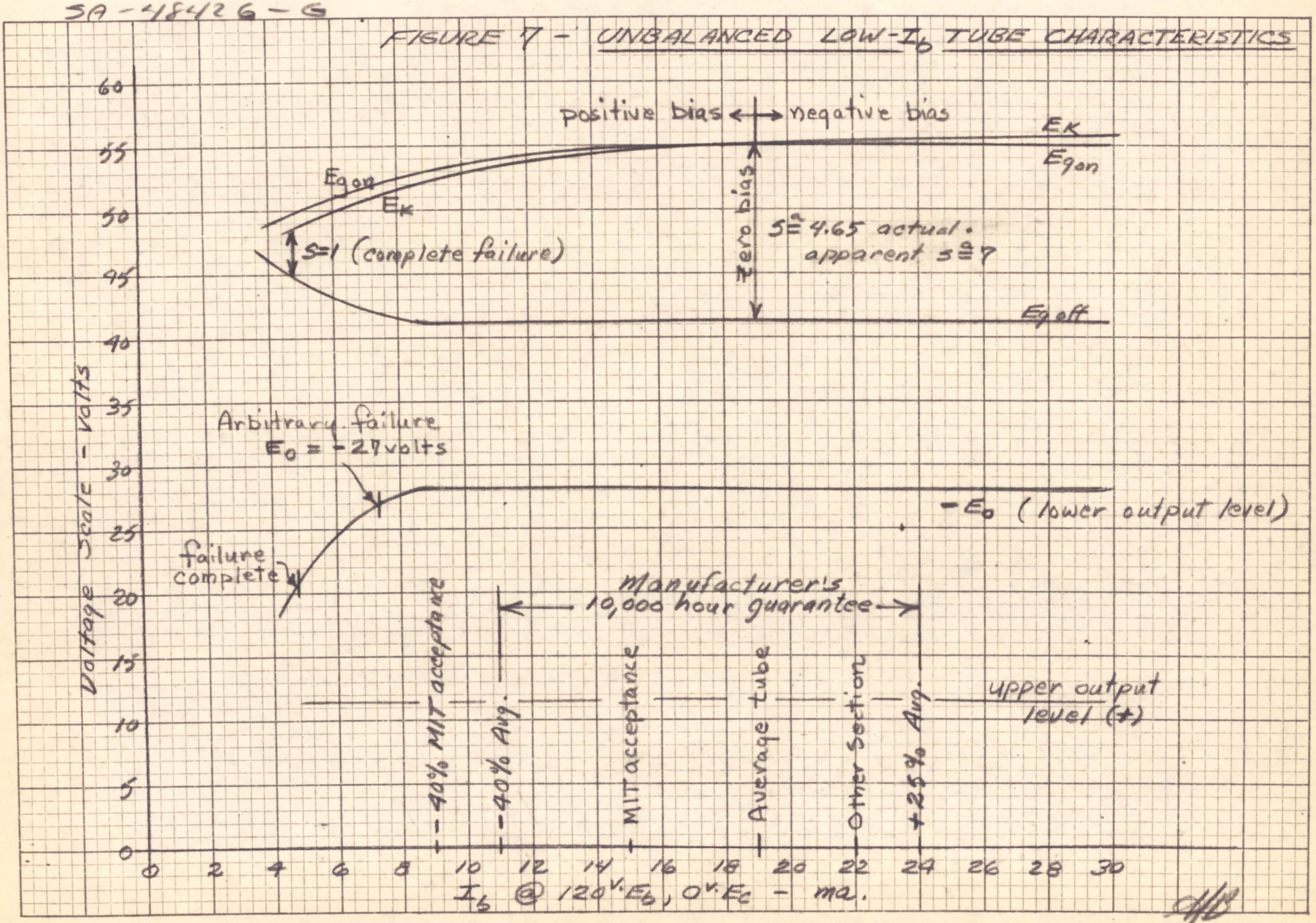
FIGURE 7 - UNBALANCED LOW-I_b TUBE CHARACTERISTICS



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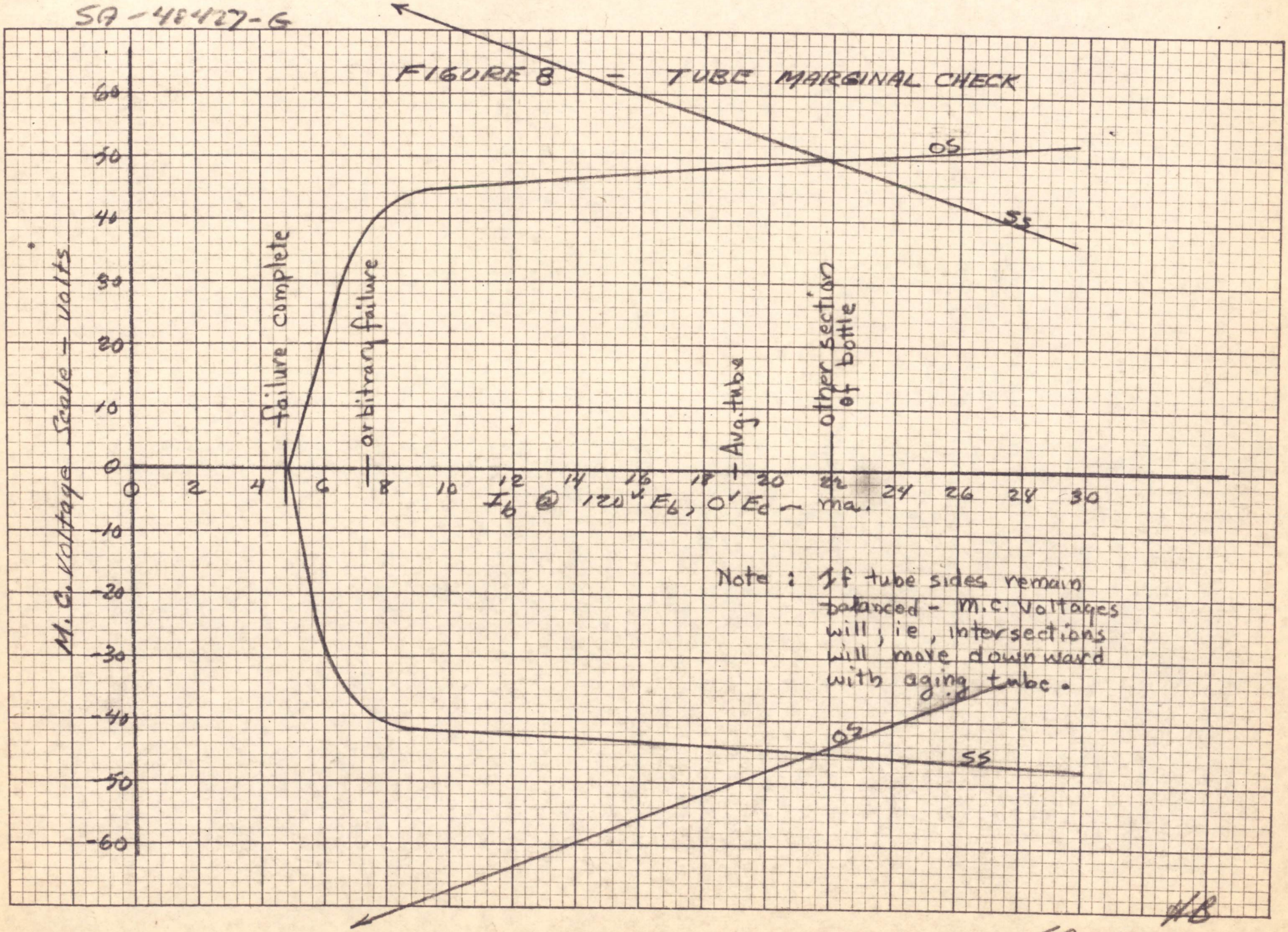

#8

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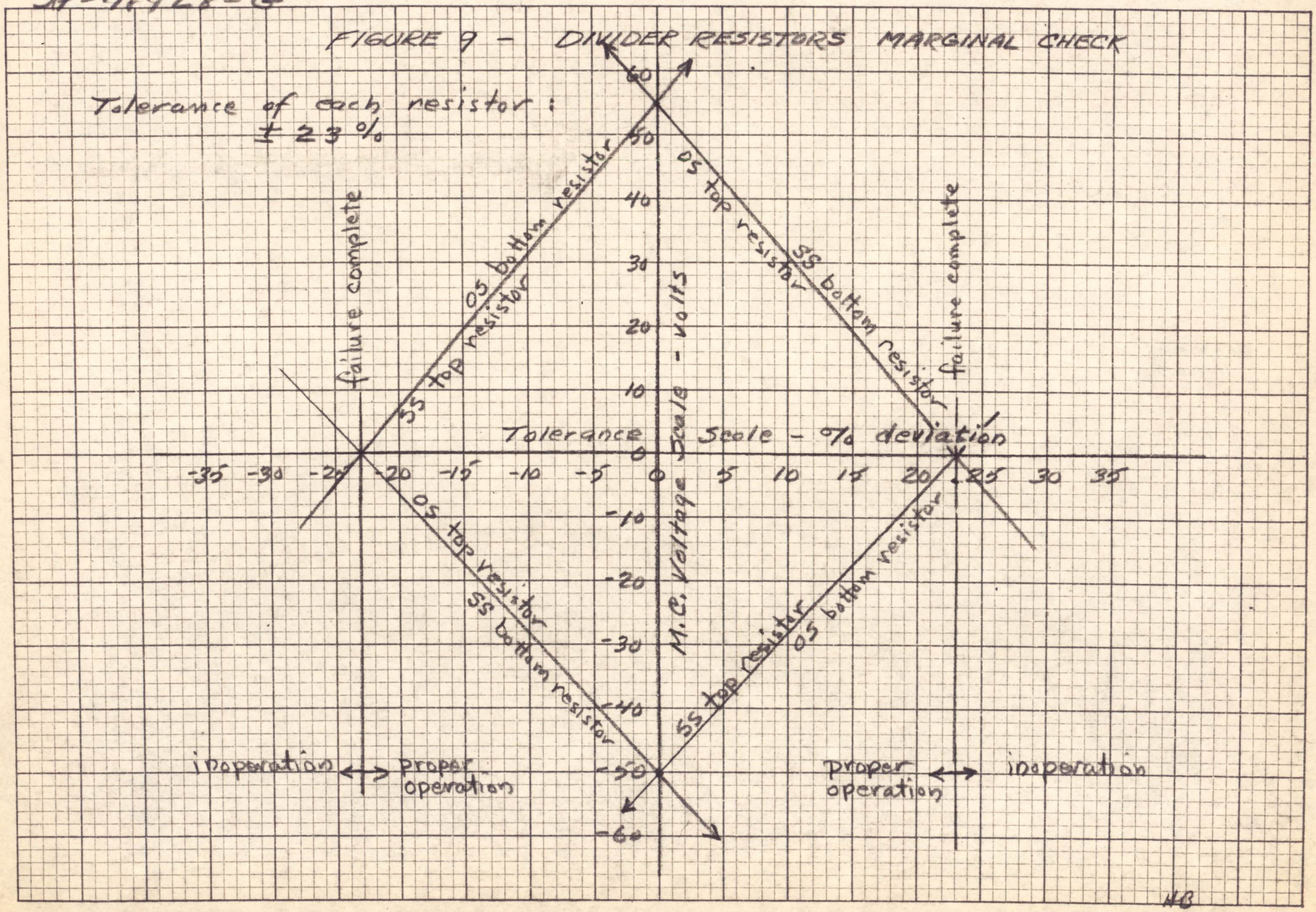
V1

SA-48428-G



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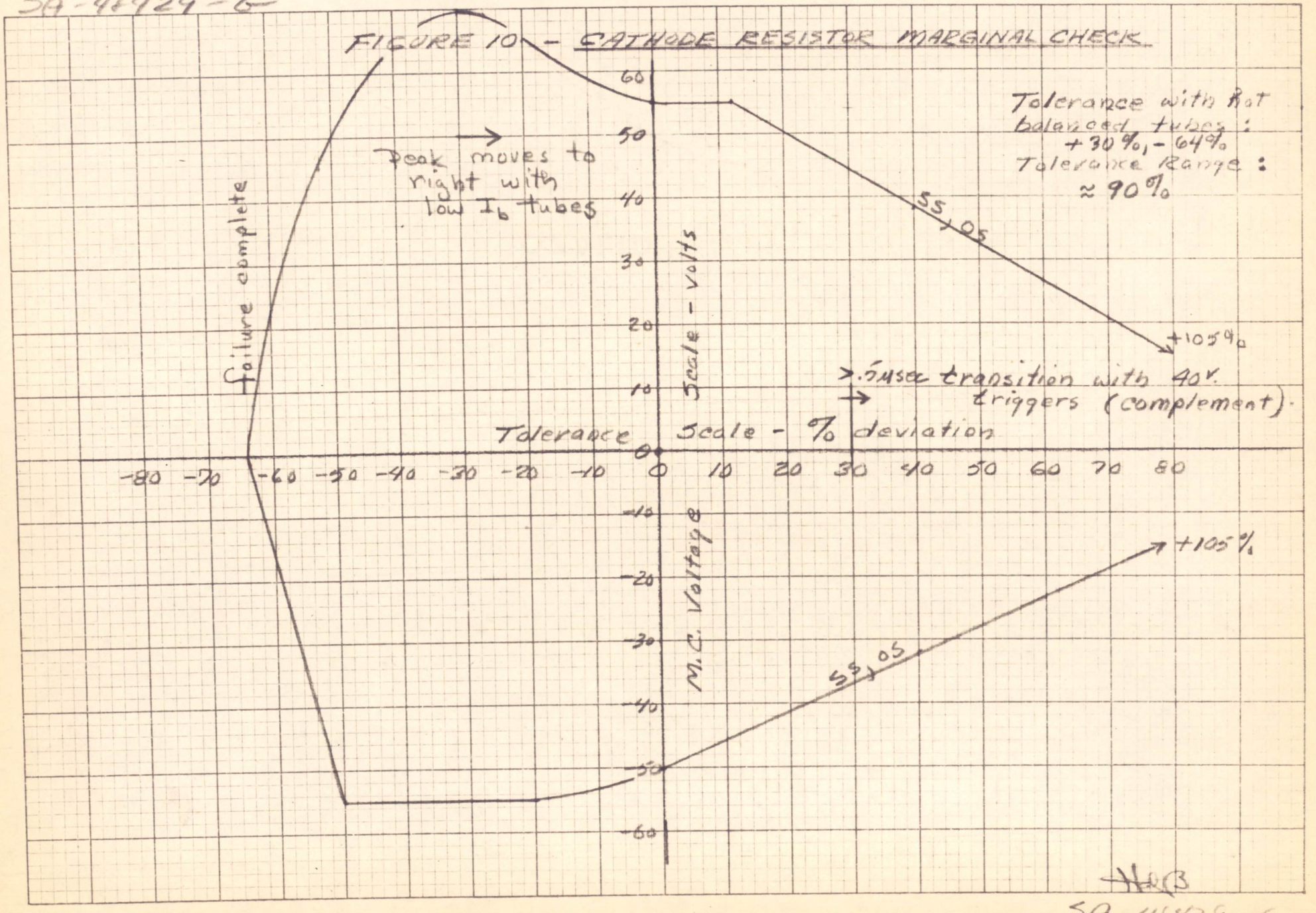
SA-4429-G

FIGURE 10 - CATHODE RESISTOR MARGINAL CHECK



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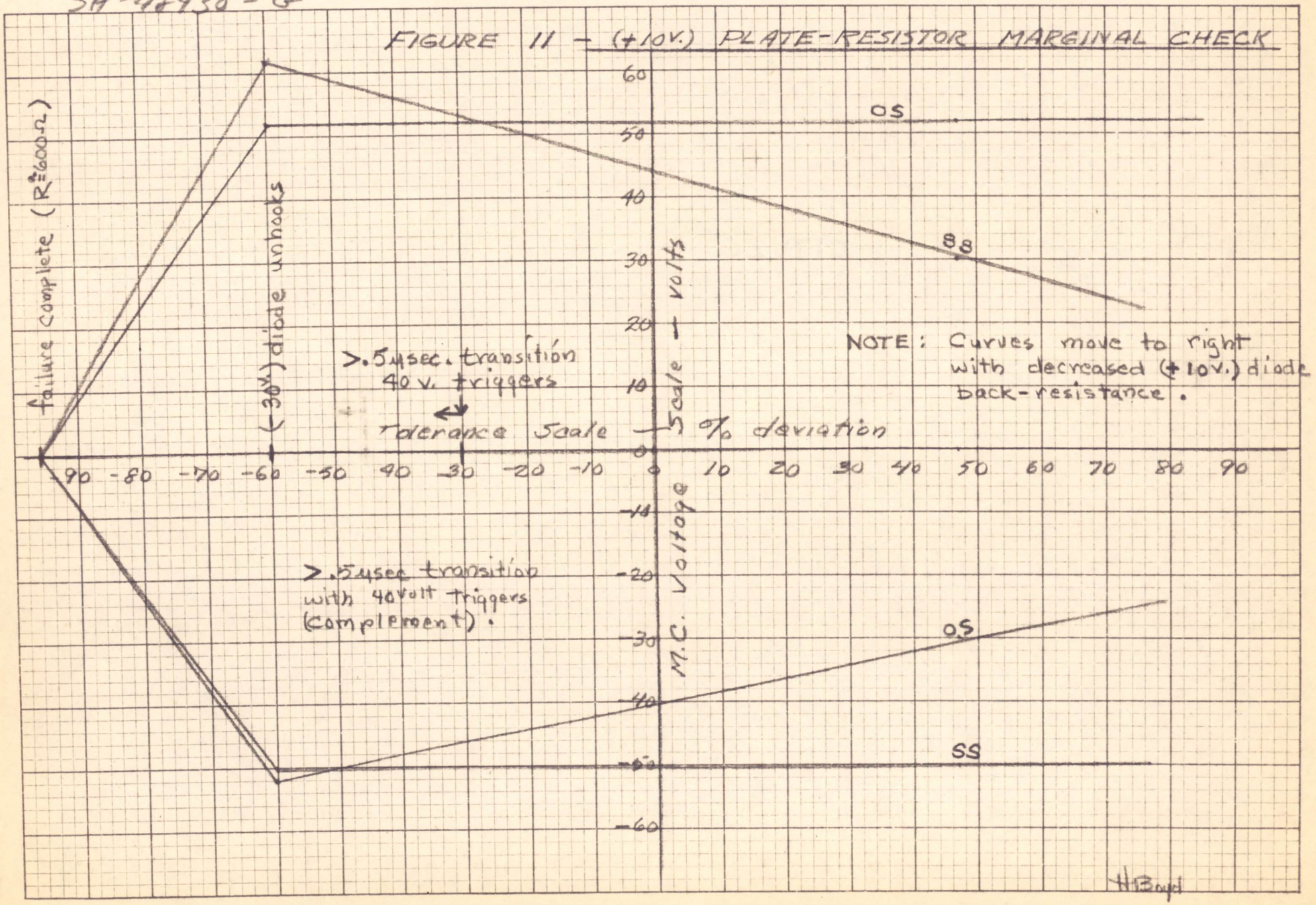

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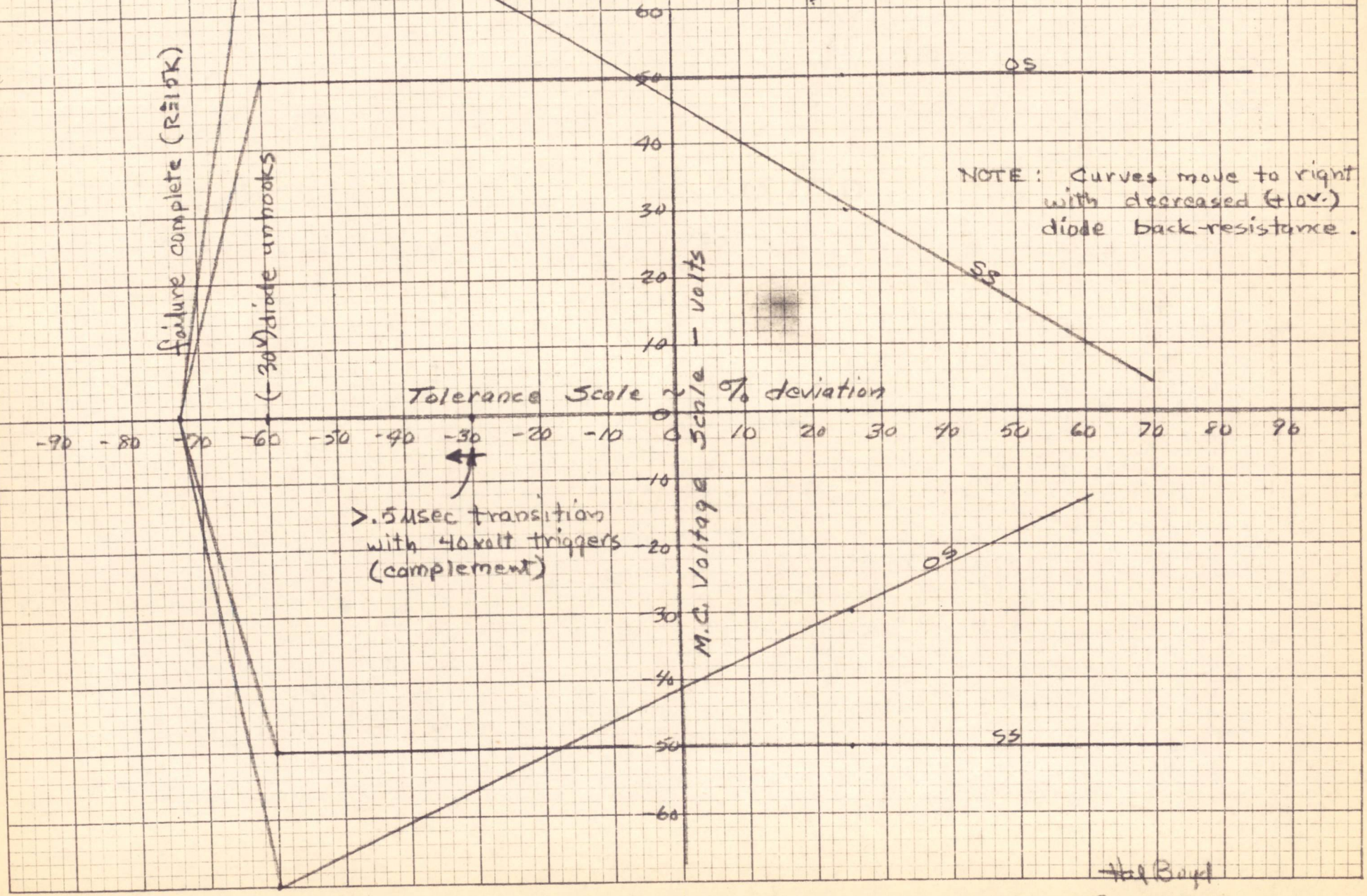
SA-41431-G

FIGURE 12 - (+150V) PLATE-RESISTOR MARGINAL CHECK



NOTE: Curves move to right with decreased (+10V.) diode back-resistance.

Hal Boyd

SA-41431-G

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Semi-Logarithmic, 3 Cycles × 10 to the inch,
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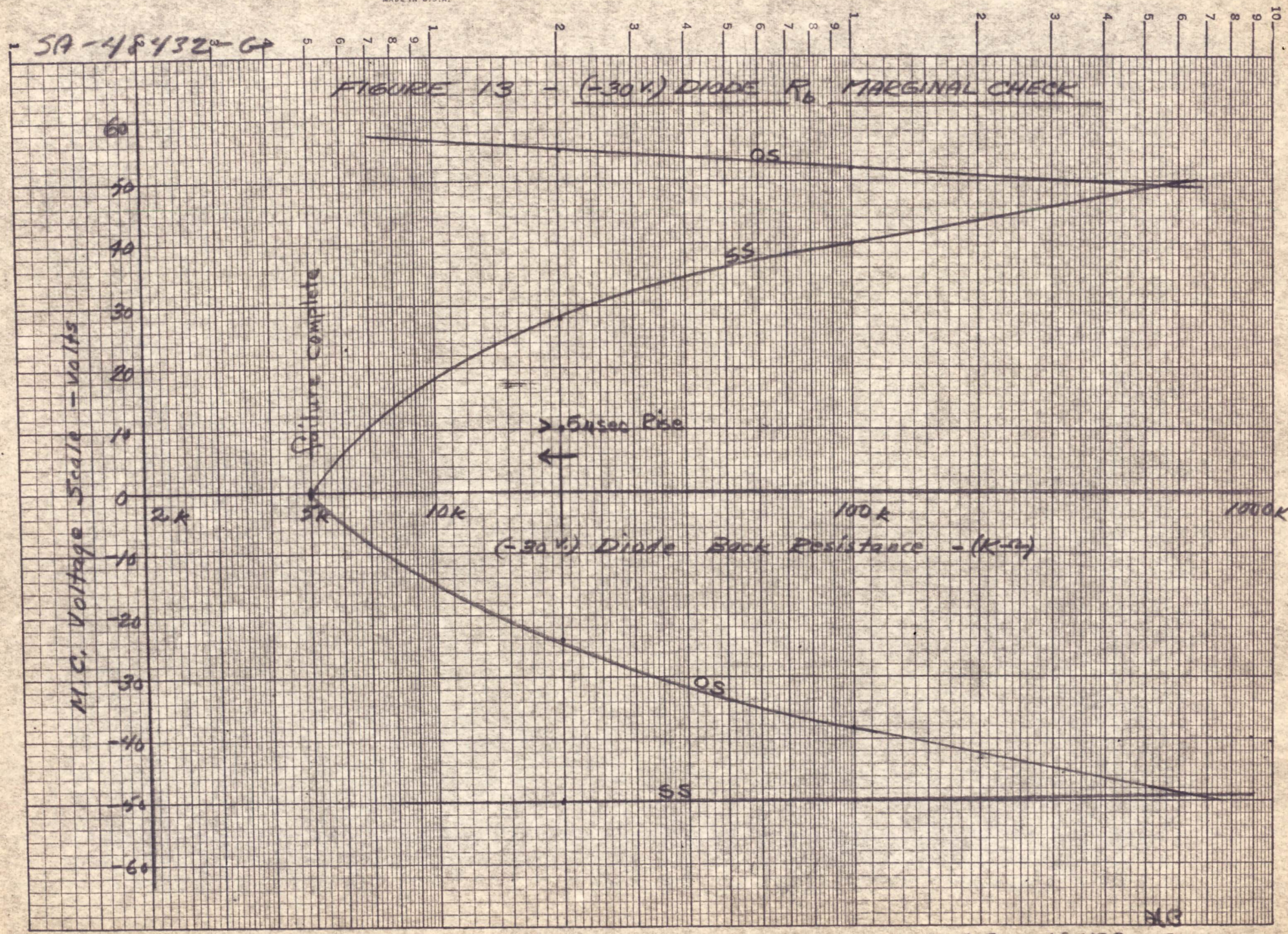
FIGURE 13 - (-30 V.) DIODE R_b MARGINAL CHECK



NLB

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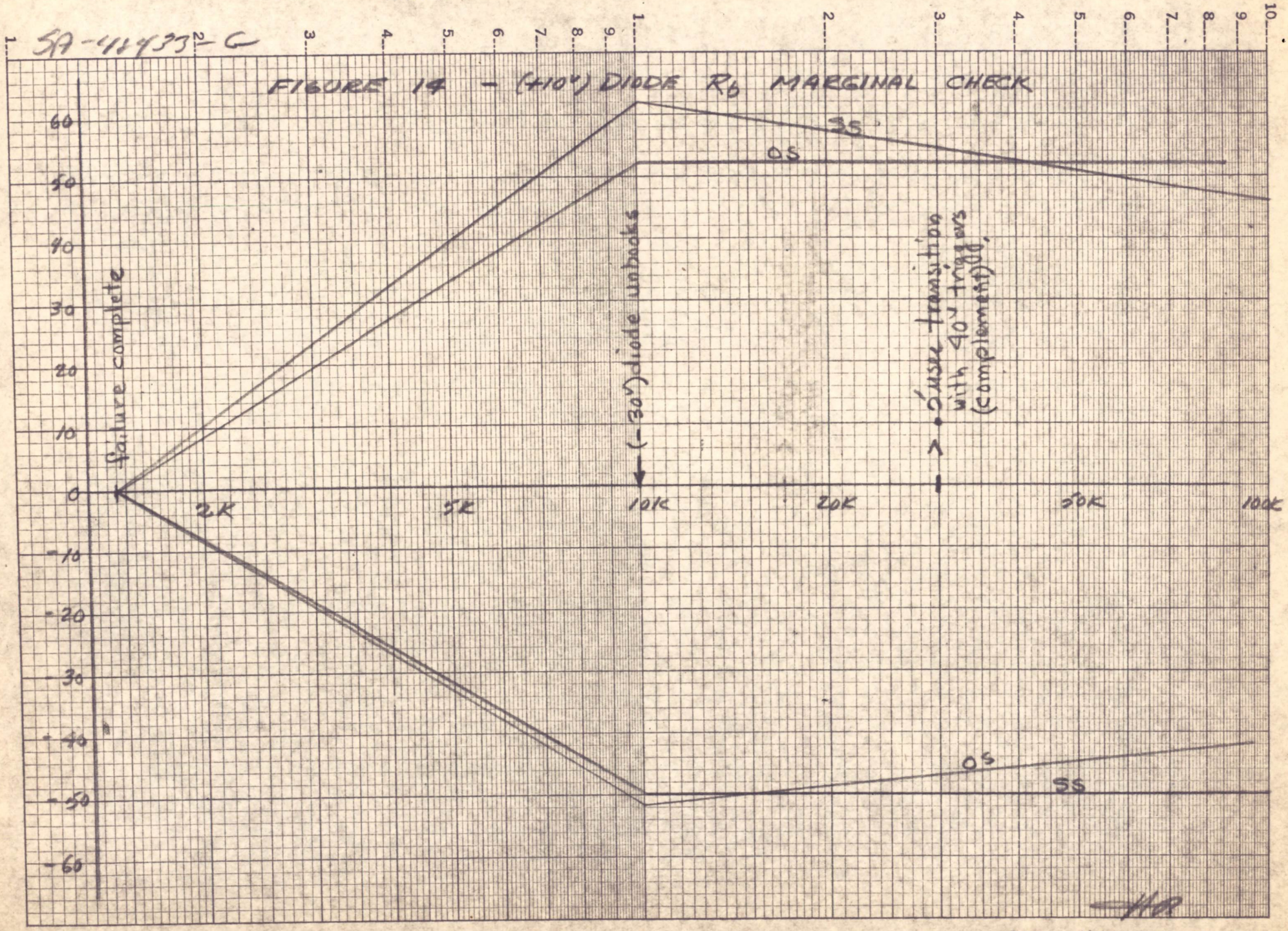

SA-11433-G

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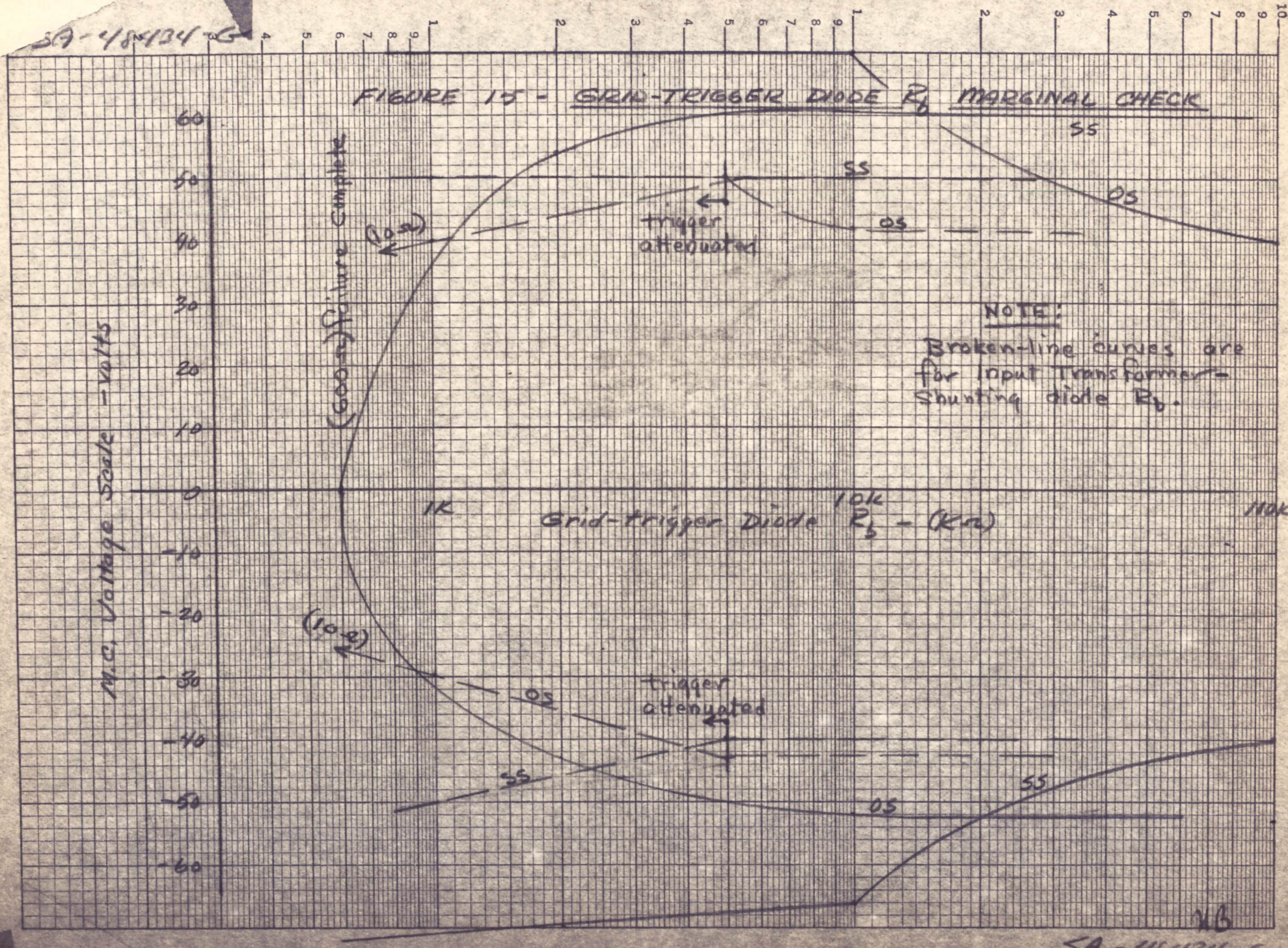

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FIGURE 16 - MARGINAL CHECK VOLTAGE - VS - INPUT-TRIGGER AMPLITUDE

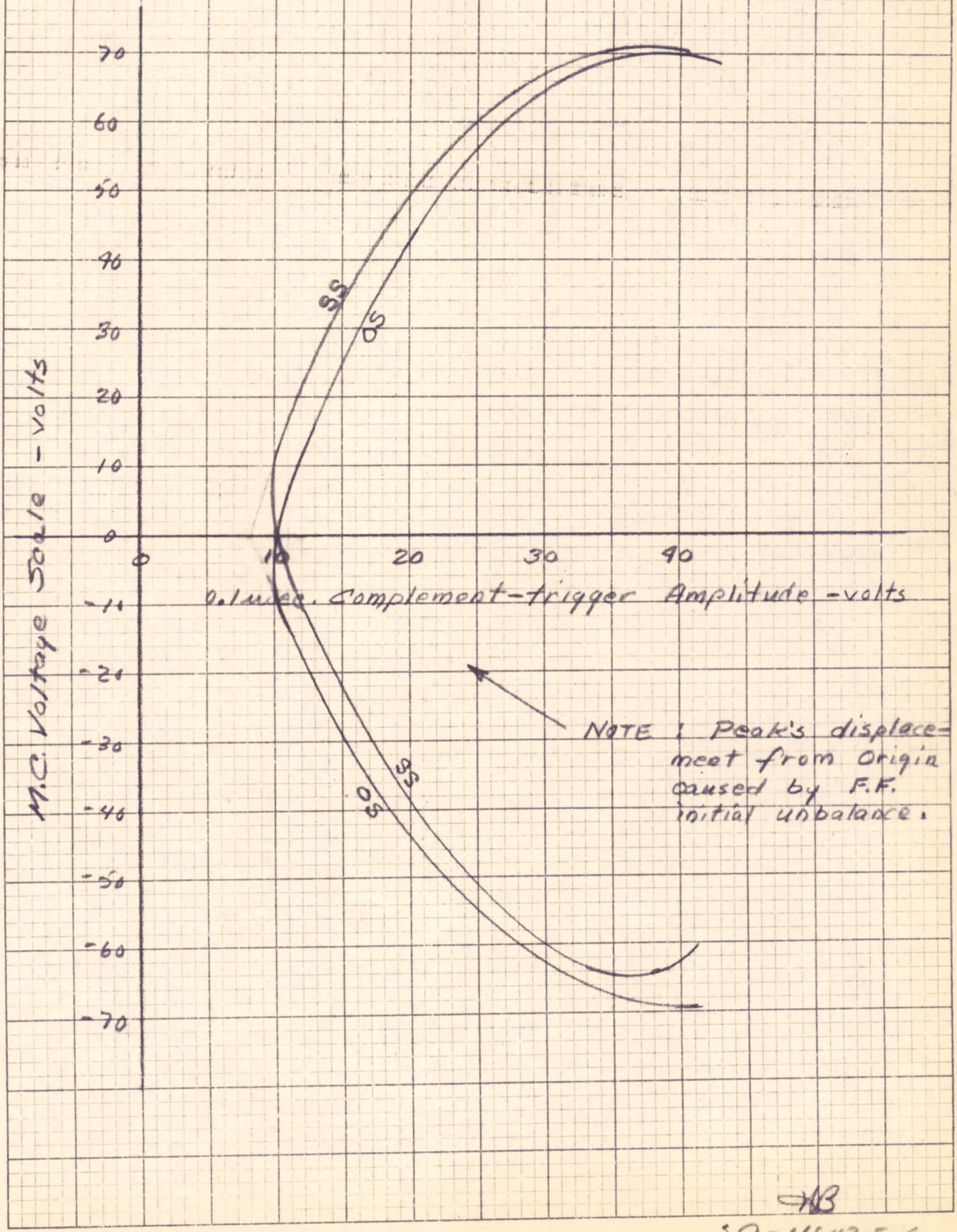

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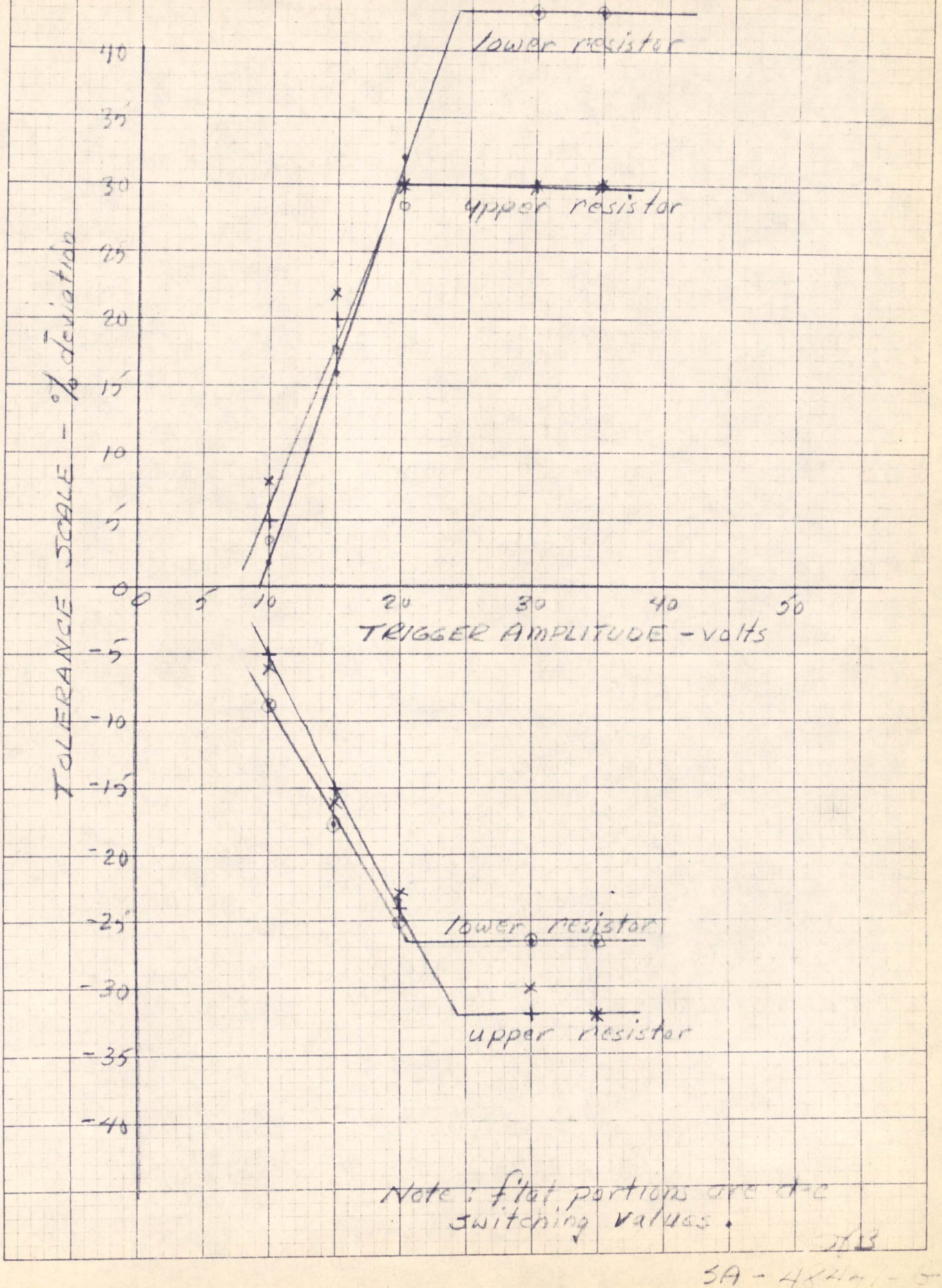
FIGURE 17 - DIVIDER TOLERANCE VS. TRIGGER



Note: flat portions are d-c switching values.

II-15

SA-4K441-5

K. Olsen

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: PROPOSED HIGH INPUT-IMPEDANCE TRIGGER CIRCUITRY FOR HIGH-SPEED WWII FLIP-FLOP

To: N. H. Taylor, R. A. Nelson, and Group 62 Section Leaders

From: Basil R. Remis

Date: May 22, 1953

Abstract: Two basic forms of input circuits used to Trigger a high-speed 5965 flip-flop are the capacitative circuit shown in Figure 1, and the transformer circuit shown in Figure 3. Figure 1 is best when negative pulses are available, and Figure 3 when positive pulses are available. This report outlines the results of a circuit modification, applicable to either trigger circuit, which decreases the load seen by a trigger pulse. The reduction in load is obtained by isolating the low impedance divider in the cathode circuit of the output cathode follower (10 K in parallel with 5.6 K, together with the 33 μμf speed-up capacitor) from the rest of the trigger circuitry. The proposed high input-impedance circuits are shown in Figures 2 and 4.

I. CIRCUITS

A. Capacitative Trigger Circuit

The initial investigation was concerned with the capacitative circuit in Figure 2. At first it was felt that this circuit, together with its corresponding coupling circuit, Figure 5, could be operated from the "level output" of logical diode circuitry without an intervening buffer stage. This would be a material advantage over the transformer trigger circuit which uses a 7AK7 gate tube in its coupling circuit. However, this advantage proved to be only illusory since R4 the "negative and" circuit resistance in Figure 5, had to be made as low as 27 K to drive satisfactorily the remaining trigger circuitry. This necessitates a cathode follower section after the output of any logical diode circuitry.

1. Low Impedance Circuit (Figure 1)

The triggering of the 5965 flip-flop is accomplished by negative trigger pulses reaching the grid of the "on", or conducting flip-flop tube. In Figure 1 the incoming negative trigger pulse closes CR-1 and opens CR-2, thus appearing across the back resistance of CR-2 directly between the grid and cathode.

2. High Impedance Modification (Figure 2)

This circuit is identical to the preceding one except for the addition of CR-3, R2 and R3. The negative trigger pulse in addition to closing CR-4 and opening CR-5 (as in the previous case) now opens CR-3, effectively disengaging the 3.6 K, 33 μμf divider circuit. CR-3 does not block the positive switching transient reaching an "off" flip-flop grid via the divider circuit from the opposite flip-flop plate. It does, however, block the low impedance source of current from the flip-flop divider circuit. To enable rapid switching of the grid potential, the substitute source of current, R3, has been added. It was the grid current available from the divider which permitted proper circuit operation even when the flip-flop tube has aged 60%. Although R3 can only supply 1.36 ma, of which about 1/3 is by-passed from the grid circuit by the forward resistances of CR-4 and CR-5, the effect of the more limited grid current source is only to reduce the permissible aging of the flip-flop tube from 60 to 40%.

The three components CR-3, CR-4 and R3 may be considered as a diode "and" gate, with the output, c, following the lower of the two inputs, a and b. If for some reason the level of point a has fallen below cathode potential, the divider is unable to lift up the grid of the flip-flop tube to the "full on" condition. This has the same effect as a further aged flip-flop tube. In the absence of a negative trigger pulse, current from R2 will insure the closure of CR-5, and will place point a at cathode potential. However, when the flip-flop tube is in the "off" condition, CR-4 will draw off some of the current available from R2 as back current. When the back resistances of CR-4 has fallen to 50 K, all of the available current will be drawn from R2. Any further decrease in back resistance will draw back current through CR-5, and point a will be pulled more negative than cathode potential. Now when the divider tries to turn the flip-flop tube to the "on" condition, the grid cannot get up to cathode potential until point a has risen, i.e., until the coupling capacitor C1 has recharged. The effect is thus an initially weak flip-flop tube, with the possibility of slower plate fall times in the case of a marginal tube. However, the 10 K shunt, R1, limits the loss of potential of point a to less than a volt for a back resistance in CR-4 as low as 35 K.

3. Input Coupling Circuit (Figure 5)

The diode gate coupling circuit shown in Figure 5 allows negative triggers either from the multiple input "negative Or" gate (CR-10 etc.) or from the"negative And" gate (CR-6, CR-7) to pass through to the input trigger circuit. Any trigger pulse which appears at the multiple input negative or gate will pass through directly to set or clear the flip-flop, while a command trigger pulse to the "negative and" gate will be effective only if the "level output" (the second input to the diode gate) is down or negative.

Referring to Figure 2, the following currents flow into the right side of C1 during the negative trigger pulse: the back currents from CR-3 and CR-5, and the currents from R2 and R3, totalling about 2.5 ma. This current partially discharges C1. To prevent p.r.f. trigger sensitivity, C1 must be recharged during the interval between pulses. The recharging current is supplied from R5 of the diode coupling circuit. For a trigger pulse width of 0.2 μsec, the maximum value of R5 to permit recharging for a p.r.f. of 1 mc/sec was experimentally determined to be 180 K.

The value of R4, the "negative and" gate resistor, must be low enough to accept the 2.5 ma from the input trigger circuitry, the 0.83 ma from R5, and the back current from CR-9, and still pull down point d at an acceptably fast rate. When the "level" input to CR-7 is up or positive, it must supply enough current to hold up point d. An attempt to make R4 pull down point d fast enough to follow a 0.1 μsec command pulse led to so low a value of resistance that more than a single cathode follower section was required in the level input line. As a compromise, a 0.2 μsec trigger pulse and a 27 K resistor were chosen.

B. Transformer Trigger Circuit

1. Low Impedance Circuit (Figure 3)

The 1:1 pulse transformer in the input circuit permits the use of incoming positive 0.1 μsec pulses to trigger the flip-flop tube.

2. High Impedance Modification (Figure 4)

This circuit is identical to the preceding one except for the addition of CR-3 and R3. The discussion on the capacitative circuit concerning the isolating action of CR-3 and the substitution of

a limited source of grid current for the low impedance divider source applies to this circuit also. This circuit differs from the capacitative one is that point a now has a low impedance path to the cathode through the transformer winding, by means of which back current can be supplied to CR-4. This path eliminates both the necessity for the 0.28 ma source through R2 in the other circuit, and the possible effective weakening of the flip-flop tube due to point a having fallen below cathode potential. CR-4 is thus less critical as to back resistance in this circuit than in the capacitative circuit.

3. Input Coupling Circuit (Figure 6)

The 7AK7 gate tube coupling circuit shown in Figure 6 allows positive triggers either from the multiple input "or" gate (CR-8, etc.) or from the gate tube (effective "and" gate) to pass through to the input trigger circuit. It may be noted that the resistor of the multiple input "or" gate is missing. It's function, to pull down the output after the pulse has passed, is supplied by the ringing of the transformer primary winding. Since the gate tube has enough power to drive 0.1 μsec pulses no recourse to wider trigger pulse widths is needed in this circuit, as in the diode coupling circuit.

II. MARGINS AND TOLERANCES

The only circuit investigated for margins and tolerances was the high impedance capacitative circuit together with its diode coupling circuit. In Figure 2 the investigation showed CR-4 to be the only critical component. CR-5, already shunted by 10 K can do no worse than cause a small attenuation in trigger amplitude, even when its back resistance has deteriorated past 10 K. The effect of a poor back resistance in CR-3 is to increase the trigger pulse load. An increase in resistance of R3 further limits the grid current, and hence the life of the flip-flop tube. However, an increase of 20% in R3 does not limit the allowable tube aging by more than about 3%. The effect of low back resistance in CR-4 is discussed in the section on the high-impedance capacitative circuit. With R2 at 330 K, CR-4 can age to 50 K back resistance before any effect will be noticed. If it is desired to increase the allowable aging of this crystal diode, R2 must be lowered.

In the diode coupling circuit, Figure 5, R5 has been chosen low enough so that with a 15% decrease in the +150 volt supply and a 15% increase in resistance, R5 will still pass enough current to recharge the capacitor C1 within the period available between pulses. Since the amount of current required for recharging is a function of the trigger pulse width (the time during which C1 is discharging), the

value of R5 is similarly dependent upon command pulse width. The proposed value of 180 K is adequate for recovery between 1 mc/sec pulses when 0.2 μsec pulse widths (or smaller) are used.

As mentioned previously, R4 must be made small enough to accept all of the currents flowing into it from the input circuitry and still pull point d acceptably fast. The proposed value of 27 K, in a circuit where the negative supply has dropped 15% and where its own resistance has increased 15% beyond the nominal value, will still pull down point d to meet the following condition: the resulting output trigger pulse will be greater than twice the minimum 0.2 μsec pulse required for setting or clearing the flip-flop.

IV. CONCLUDING REMARKS

Of the two circuits discussed in this report, the transformer input circuit uses the additional components necessary for a high input-impedance modification in a less critical fashion. The low impedance path through the transformer winding considerably relaxes the back resistance requirements upon CR-4, the only critical component in the capacitative circuit. The ability to use positive rather than negative trigger pulses gives the transformer circuit a second advantage over the capacitative circuit, since the generation of positive pulses is already demanded by the use of gate tube circuitry.

The use of the proposed high input-impedance circuits in an application requiring complementing the flip-flop is not recommended. In a complement operation, negative triggers pull down both grids, temporarily cutting off both tubes. In the normal or low impedance circuit the previously "off" tube grid rises fastest, due to coupling of the rising plate transient through the 33 μμf "memory" capacitor. However, in the proposed high-impedance circuit (Figure 2 or 4) point b (pulled up by the rising plate transient) is always more positive than point c (first pulled down by the trigger and then relatively slowly lifted by R3), resulting in CR-3 on both sides of the flip-flop being open during the switching transient. The grids, being isolated from the "memory" capacitors by the back resistances of the diodes CR-3, are pulled up equally fast by the resistors R3. Thus the selection of the grid to reach cutoff first is random, and the circuit is unable to complement.

Signed Basil R. Remis
Basil R. Remis

BRR/cs

Drawings Attached:

A-55170
171
172

Approved R L Best
Richard L. Best

Approved N H T
N. H. Taylor

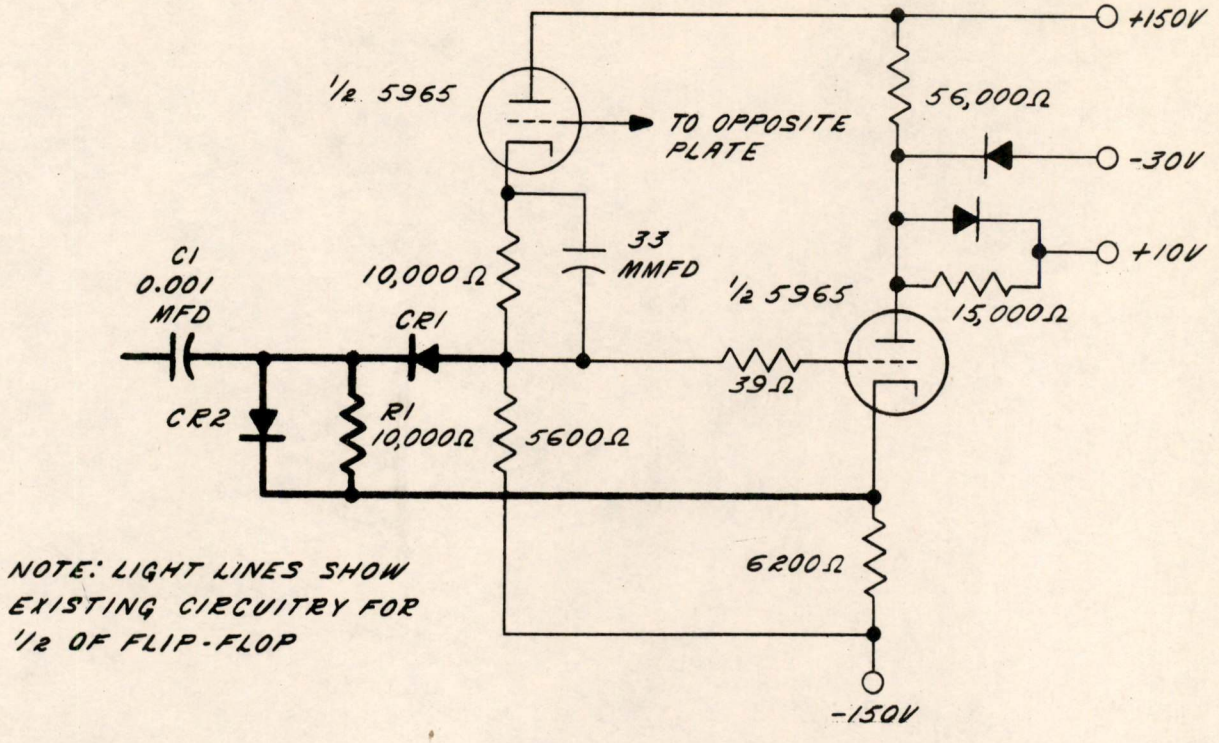


FIG. 1

TRIGGER CIRCUITRY FOR 4 MEGACYCLE 5965 FLIP-FLOP

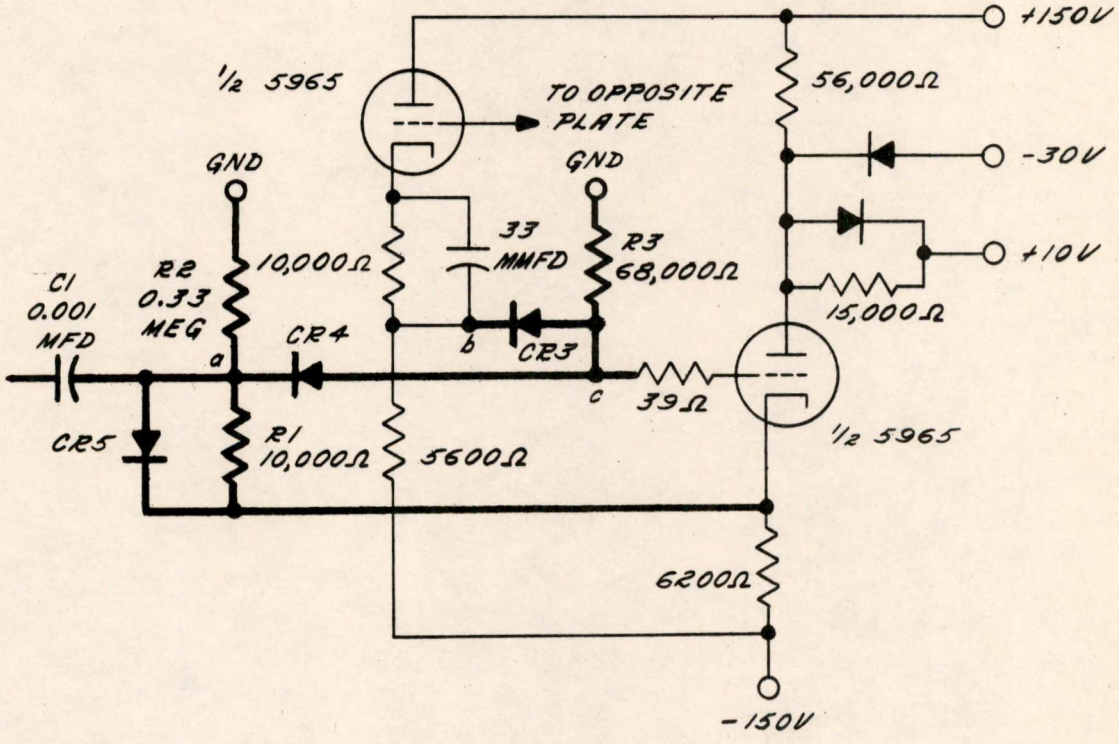


FIG. 2

HIGH INPUT IMPEDANCE MODIFICATION OF TRIGGER CIRCUIT FOR 4 MEGACYCLE 5965 FLIP-FLOP

A-55170

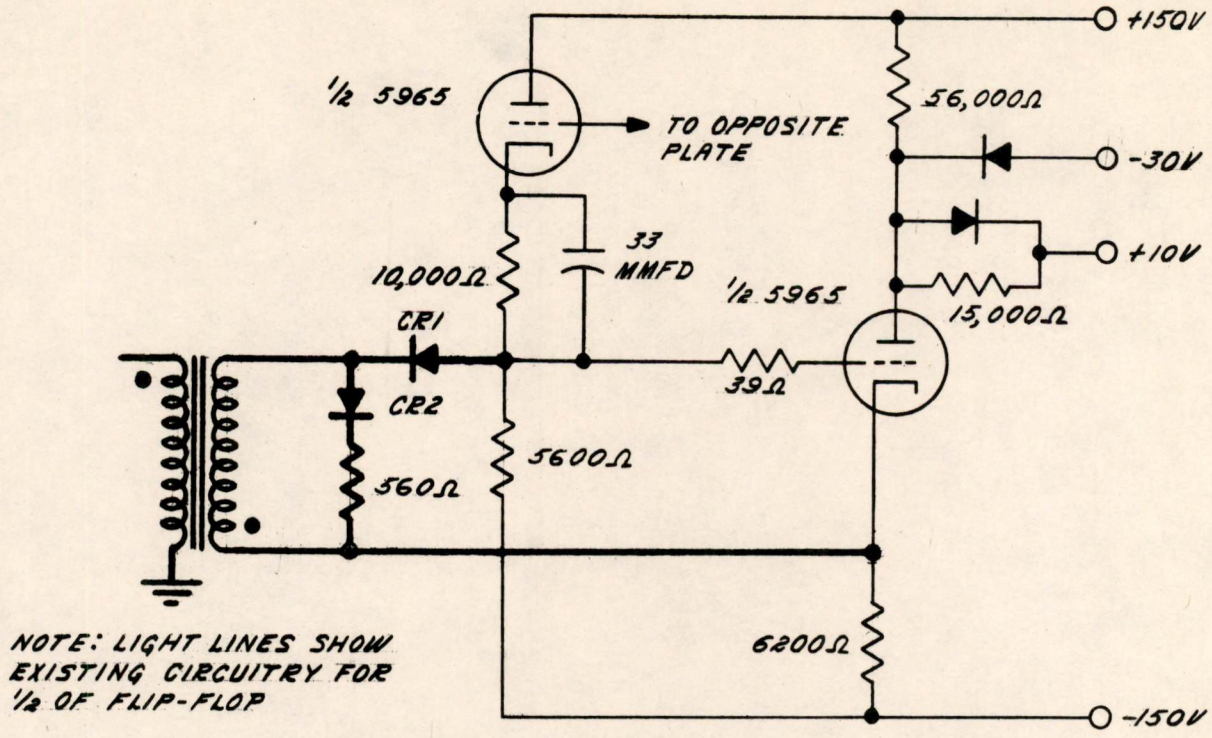


FIG. 3

TRIGGER CIRCUITRY FOR HIGH SPEED WWII FLIP-FLOP

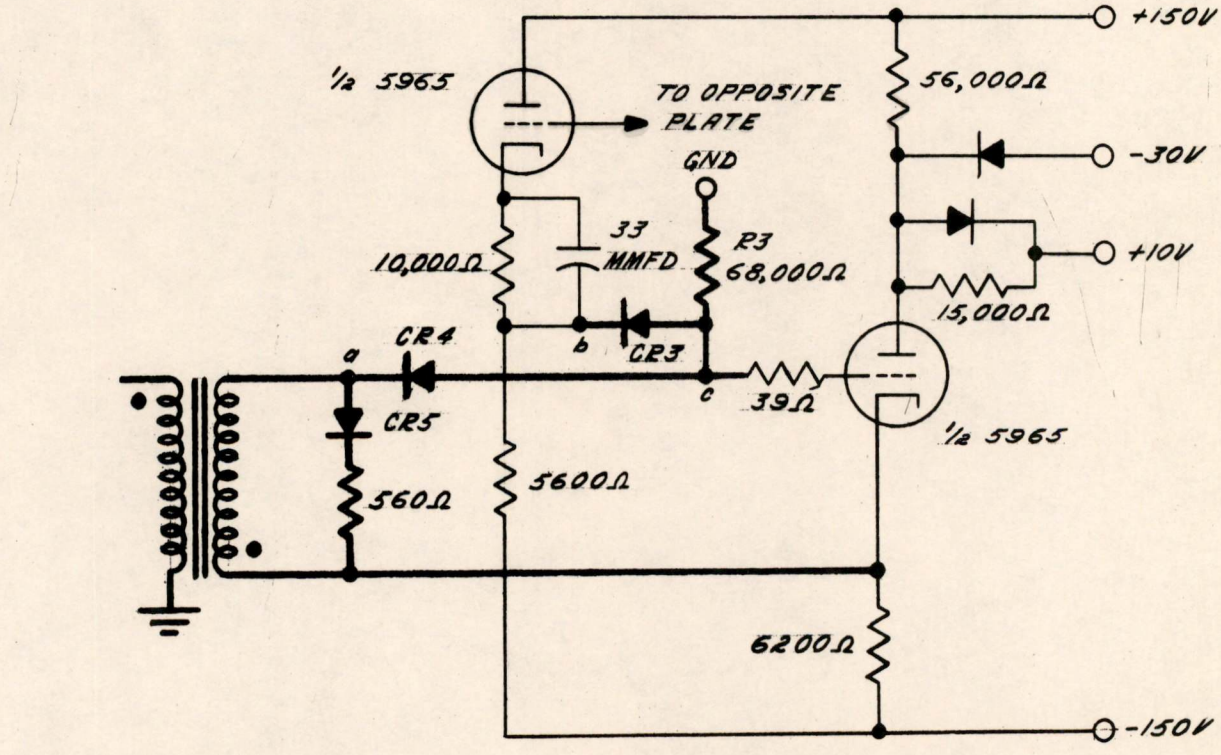


FIG. 4

HIGH INPUT IMPEDANCE MODIFICATION OF TRIGGER CIRCUIT FOR HIGH SPEED WWII FLIP-FLOP

A-55171

A-55172

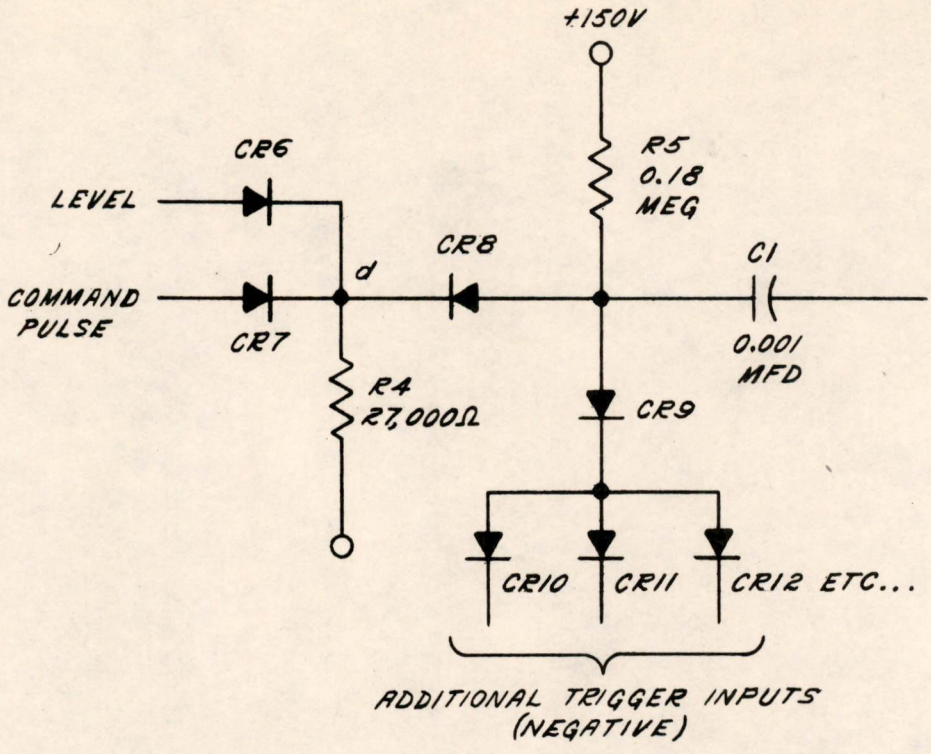


FIG. 5

INPUT COUPLING CIRCUITRY FOR 4 MEGACYCLE 5965 FLIP-FLOP

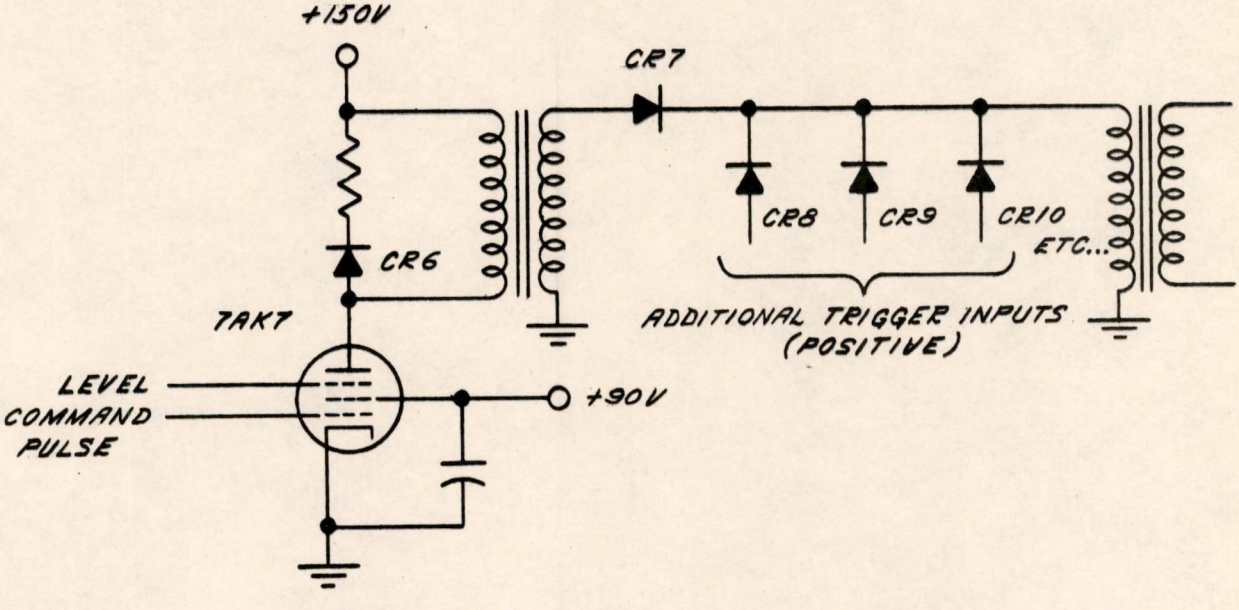


FIG. 6

INPUT COUPLING CIRCUITRY FOR HIGH SPEED WWII FLIP-FLOP

P. Best

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: PRELIMINARY REPORT — TEMPERATURE EFFECTS IN MTC-TYPE FERRITE CORES

To: D. R. Brown

From: James D. Childress

Date: June 26, 1953

Abstract: The curves given in this note show the effect of temperature on ferrite core operation. For a particular driving current amplitude, there is a point (or range) in temperature beyond which core operation degenerates rapidly. For the MTC cores used in this test, the temperature coefficient is about 1 mv/degree C; the Critical Point at 1.00 amp is 40° C; at 0.95 amp 50° C; at 0.90 amp 60°; at 0.80 amp 70° C.

The equipment and experimental method used is much the same as described in E-533, "Effect of the Current Pulse Duration on the Pulse Response of MTC Memory Cores," by P. K. Baltzer.

At first, plans for this study were to take data for current pulse durations of 1.2 μs, 1.5 μs, and 2.0 μs. This variation in pulse duration had little effect, so the pulse duration was standardized at 2.0 μs.

The test mode was six "read-write" cycles followed by (1) thirty "disturbs" for the "delta" measurements or (2) six "disturbs" for the "one" and"disturbed one" measurements. This number was too small to give accurate values of the "disturbed one" beyond the Critical Temperature Point.

Other experimental inaccuracies were caused by unreliable logic and variations in the supply voltages. Therefore, the data given here have only qualitative value. Since these data were taken, the equipment has been improved and plans are to take new data.

Data: Figure 1 shows $_{u}V_{1}$ (undisturbed one) and V_{1} (disturbed one) vs. temperature for current-pulse amplitudes of 1.00 amp, 0.95 amp, 0.90 amp, and 0.80 amp. The sampling time was the time of the $_{u}V_{1}$ peak, roughly 0.6 μs.

There is a positive temperature coefficient of $_{u}V_{1}$ so that $_{u}V_{1}$ might be expressed as:

$$_{u}V_{1} = c_{1} (1 + \alpha T) + c_{s} I$$

Early work by McCusker and Schallerer indicated that α would vary from lot to lot.

Note also that V_1 increases (negligibly different from ${}_uV_1$), reaches a maximum at a point in temperature, then decreases rapidly. Operation beyond this maximum does not seem feasible. Note that the point of the maximum shifts upward in temperature as the current pulse amplitude is decreased.

Figure 2 gives the variation of δ_1 and δ_2 vs Temperature for current pulse amplitudes of 1.00 amp, 0.95 amp, 0.90 amp, and 0.80 amp.

The "deltas" are defined as*

δ_1 = "first half-selected one" - "first half-selected zero"

δ_2 = "second half-selected one" - "second half-selected zero"

These are the "deltas" given in Figure 2, sampling time 0.6 μs.

Note that δ_1 is constant below a point in temperature, then increases rapidly. Also, δ_2 is negligibly different from zero below a temperature point but increases rapidly above that point.

Roughly, the point in temperature at which V_1 has its maximum is the same point at which δ_1 and δ_2 begin to increase. This point (or range) may be called the Critical Temperature Point for Core Operation. Note that the Critical Point depends on the current pulse amplitude--lower current pulse amplitude, higher Critical Point.

Since these measurements were made, the "deltas" have been re-defined. New measurements will be made of the proper "delta" vs temperature. Until then, Figure 2 indicates what type of variation might be expected.

From the data in Figures 1 and 2, conclusions are as follows:

1. Temperature has an important effect on core operation.
2. Temperature is one of the variables which should be closely controlled in ferrite-core evaluation. From Figure 1, a ten-degree change in temperature produces about a fifteen-percent change in ${}_uV_1$ or V_1. This is as wide as the limits for acceptability of cores. Therefore, for accuracy in production testing, the temperature of the cores need be accurately controlled.

Further measurements are being made and others are being planned. Plans are to measure the following:

1. Temperature Coefficients for different lots.
2. Critical Points for different lots.
3. Hysteresis Loops vs. Temperature.
4. Physical dimensions vs. Temperature Coefficients vs. Critical Point.

---

* E. A. Guditz, E-448, "Delta$_{ns}$ in Ceramic Array #1," Digital Computer Laboratory, MIT.

Signed James D. Childress
James D. Childress

Approved JRB
David R. Brown

JDC/jk

Drawings attached:

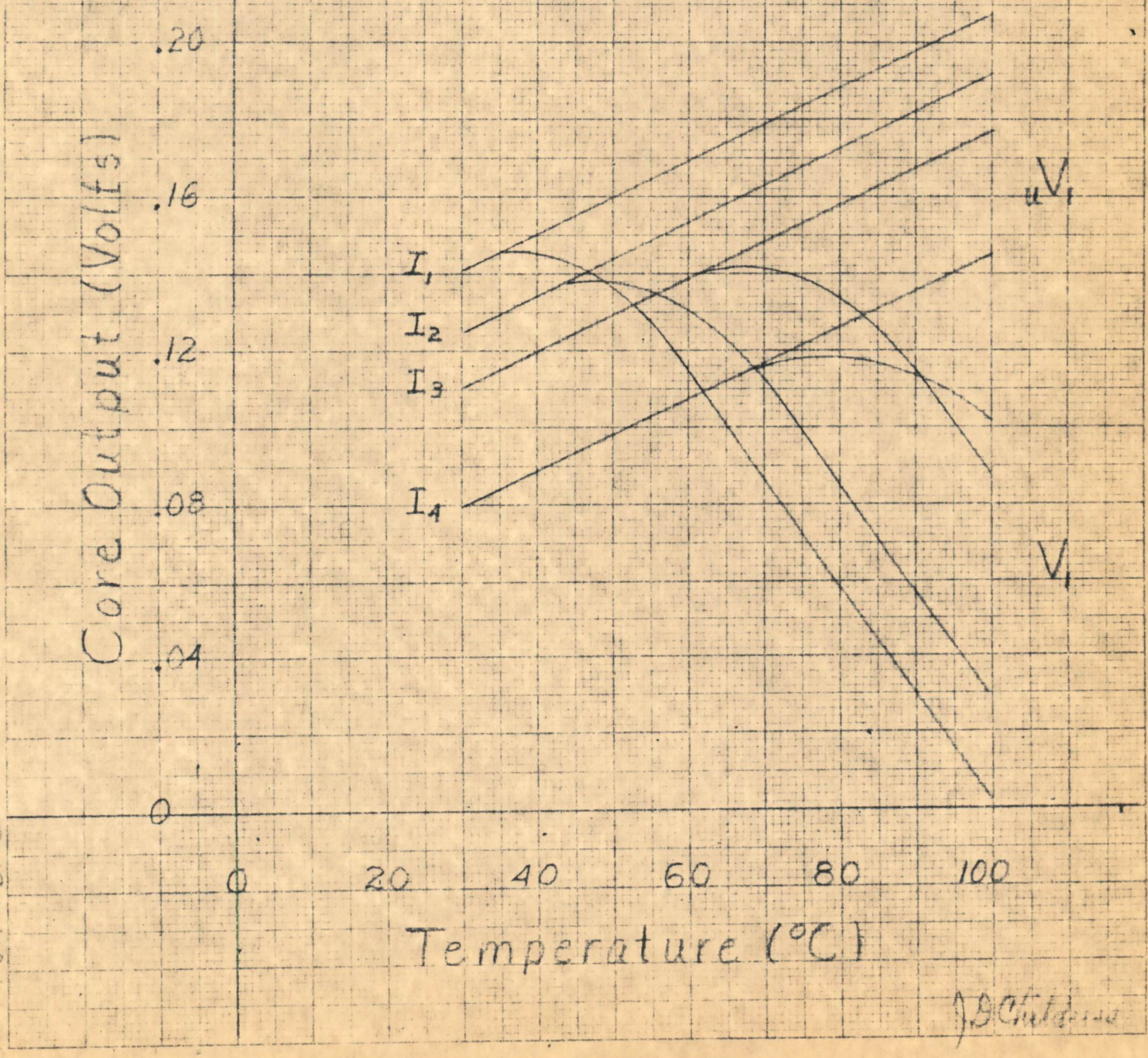
Figure 1 SA-48446-G
Figure 2 SA-48447-G

cc: Group 63 Staff
N. H. Taylor
Group 62 Memory Section
IBM

"One" and "Disturbed One" vs. Temperature

MF 19268, F291

I_1 = 1.00 amp
I_2 = 0.95 amp
I_3 = 0.90 amp
I_4 = 0.80 amp

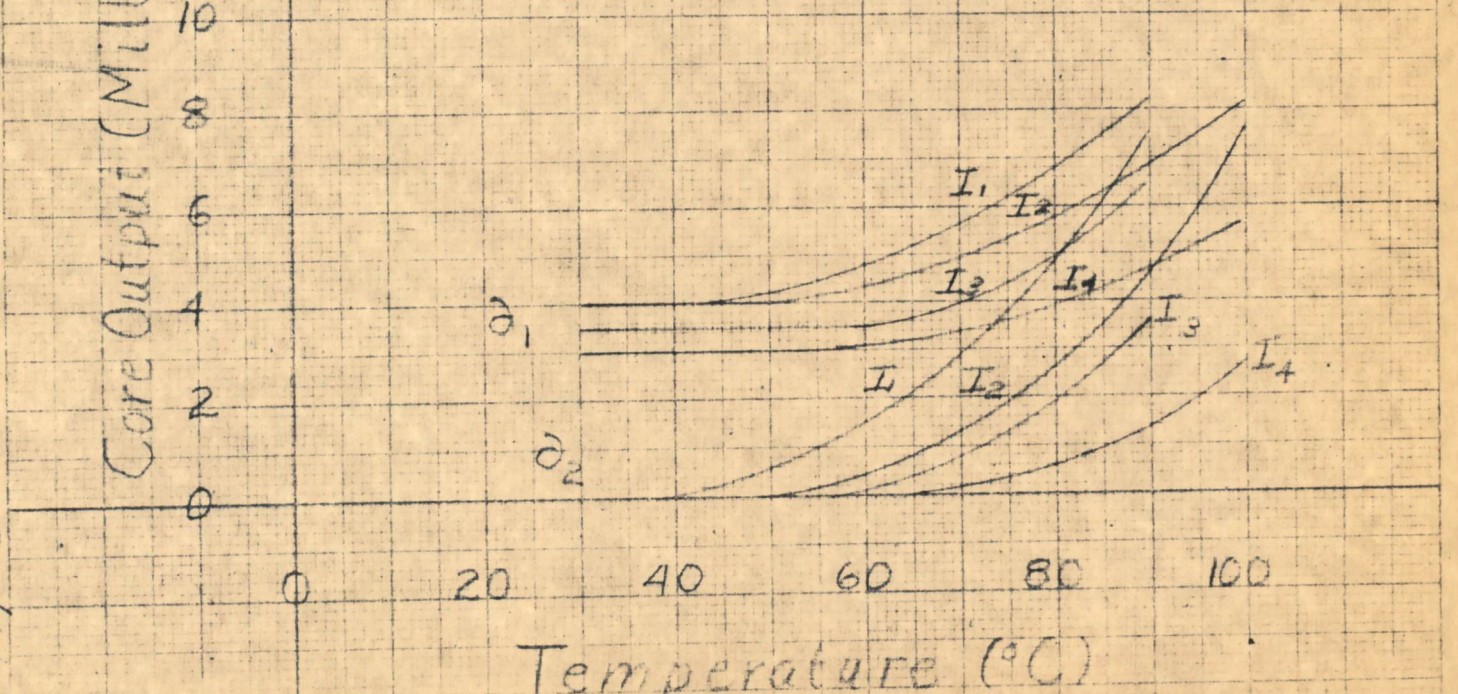


SH 46446-5

"Delta One" and "Delta Two" vs. Temperature

MF 1326 B, F 291

I_1 = 1.00 amp
I_2 = 0.95 amp
I_3 = 0.90 amp
I_4 = 0.80 amp



R. Best

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: OPEN-CIRCUIT IMPEDANCE REPRESENTATION OF TRANSISTORS*

To: Norman H. Taylor

From: Nolan T. Jones

Date: July 9, 1953

Abstract: Five transistor equivalent circuits, expressed in terms of open-circuit impedances, are presented. Two are general active network equivalent circuits with voltage and current generators as the active elements, two are "T" equivalent circuits with similar voltage and current generators, and the fifth is the two-diode large-signal equivalent circuit. Approximation of the frequency response of the current gain and inclusion of collector capacity are discussed with respect to use of the equivalent circuits at high frequencies. Procedure and equipment for the measurement of dynamic characteristics, parameters at a given operating point, and large-signal parameters are reviewed, as well as the difficulties encountered with short-circuit unstable units and the design of measuring equipment. Both point-contact and junction transistors are considered with emphasis on the advantages of good representation and ease of measurements for the point-contact units in large-signal circuits.

INTRODUCTION

The subject of transistor equivalent circuits in terms of open circuit impedances has been covered extensively in the current technical literature. Several such articles have been listed in the bibliography. The approach has been to deal with the transistor as a general two terminal-pair device, and then to specialize these general parameters to better represent the transistor. This same approach is used here with additional descriptions of the two diode large-signal equivalent circuit, and a cursory discussion of the open circuit impedance measurement problems.

THE TRANSISTOR AS A FOUR TERMINAL ACTIVE NETWORK

The terminal voltages may be considered functions of the terminal currents in any general two terminal-pair device. This fact is represented by equations 1 and 2 for a grounded base transistor circuit.

1) $V_e = f(I_e, I_c)$

2) $V_c = g(I_e, I_c)$

---

* Paper presented at AIEE Summer Convention, Atlantic City, New Jersey, June 17, 1953.

Differentiation of each of these equations leads to equations 3 and 4. Each of the partial differential coefficients has the dimension of resistance. These coefficients are defined in equations 5 through 8.

3) $$dV_e = \frac{\partial V_e}{\partial I_e}\, dI_e + \frac{\partial V_e}{\partial I_c}\, dI_c$$

4) $$dV_c = \frac{\partial V_c}{\partial I_e}\, dI_e + \frac{\partial V_c}{\partial I_c}\, dI_c$$

5) $$\left.\frac{\partial V_e}{\partial I_e}\right]_{I_c \text{ constant}} \triangleq r_{11},$$ open circuit input resistance*

6) $$\left.\frac{\partial V_e}{\partial I_c}\right]_{I_e \text{ constant}} \triangleq r_{12},$$ open circuit feedback or reverse transfer resistance

7) $$\left.\frac{\partial V_c}{\partial I_c}\right]_{I_e \text{ constant}} \triangleq r_{22},$$ open circuit output resistance

8) $$\left.\frac{\partial V_c}{\partial I_e}\right]_{I_c \text{ constant}} \triangleq r_{21},$$ open circuit forward or forward transfer resistance

TWO TERMINAL-PAIR EQUIVALENT CIRCUITS

Using small letters for incremental voltages and currents and the definitions of 5, 6, 7 and 8, equations 3 and 4 may be rewritten as equations 9 and 10.

9) $$v_e = r_{11}\, ie + r_{12}\, ic$$

10) $$v_c = r_{21}\, ie + r_{22}\, ic$$

---

* $\triangleq$ means "equal by definition."

These lead to Equivalent Circuit A in illustration A-55268.

By Thevenin's Theorem the series voltage generator in the collector circuit, $r_{21}\, i_e$, can be replaced by a shunt current generator. Substitution of equation 11, produces Equivalent Circuit B, A-55260.

$$11)\quad \alpha = \frac{r_{21}}{r_{22}} = -\left[\frac{\partial I_c}{\partial I_e}\right]_{V_c \text{ constant}}$$

"T" EQUIVALENT CIRCUITS

Equivalent Circuits A and B may be converted into the widely used "T" equivalent circuits by the relationships 12 through 16. The magnitudes of these parameters observed experimentally make the approximations reasonable. These equivalent circuits represent the transistor physically as well as electrically.

$$12)\quad r_{12} = r_b \qquad r_b = \text{base resistance}$$

$$13)\quad r_{11} = r_e + r_b \qquad r_e = \text{emitter resistance}$$

$$14)\quad r_{21} = r_m + r_b \cong r_m \qquad r_m = \text{mutual resistance}$$

$$15)\quad r_{22} = r_c + r_b \cong r_c \qquad r_c = \text{collector resistance}$$

$$16)\quad a = \frac{r_m}{r_c} \cong \alpha \qquad a = \text{current gain}$$

The two "T" equivalent circuits are shown in A-55261.

LARGE-SIGNAL TWO-DIODE EQUIVALENT CIRCUIT

The development of the equivalent circuits so far has been done on a small signal basis. Each of the four parameters varies with operating point, especially at small emitter currents and low collector voltages.

If the signals reach switching circuit magnitudes as used in computer circuitry then the diode characteristics of the emitter and collector become apparent. This leads to the two-diode large-signal equivalent circuit of A-55286. This equivalent circuit will represent either point contact or junction transistors if diodes of the corresponding type and proper polarity are used. Capital letters for the voltages and currents denote large signals. In computer circuitry the emitter current may flow in either direction during the operation of most circuits. For this reason the restriction on "a" is noted.

Frequency Response*

Ideally the equivalent circuit should represent the transistor at all desired operating frequencies. It has been determined that the emitter, base, and collector resistances are essentially constant with frequency. But α, being dependent on the movement of charge carriers from the emitter to the collector, is a function of frequency. Internal capacities also limit frequency response.

The frequency at which α^2 falls to one half the low frequency value is defined as the alpha cutoff frequency, abbreviated by various groups as f_c, $f_{c\alpha}$, and f_a. This occurs when the magnitude of α becomes 0.707 of its magnitude at low frequencies.

The magnitude and phase of α may be approximated by equation 17.

17) $$a \tilde{=} \alpha = \frac{\alpha_o}{1 + j\frac{f}{f_c}}$$

α_o = low frequency value of α

f_c = cutoff frequency of α

f = the desired operating frequency

Lead to case capacities and the shunt capacities of the emitter and collector diodes tend to limit the high frequency capabilities also. In point contact units these capacities are generally of sufficiently small magnitude to be negligible compared to the fall off of response of the current gain, α.

In the junction transistor the lead to case capacities can be neglected, but diode capacities are troublesome. In some circuits the collector capacity limits the frequency response of the circuit long before the alpha cutoff frequency is approached. This collector capacity then must be included in the equivalent circuit, A-55262, in parallel with the collector resistance. Variation of collector space charge layer thickness[10] causes the collector capacitance to divide the base resistance as shown.

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* The material presented under this subtitle is largely based on items 5, 6, 7, and 9 in the bibliography.

10 Item 10 in the bibliography.

Measurements

The equipment necessary to take a complete set of four dynamic characteristics includes five basic units: emitter and collector current sources, emitter and collector sweepers, and an oscilloscope or other indicator.

Practical current sources should have internal dynamic resistances of the order of 100 times the maximum impedance of the load. The emitter current source, working into the low input resistance of 1000 ohms or less, can be simply a large resistance in series with a voltage source. Collector current sources, however, must have internal resistances of a few megohms for point contact transistors and hundreds of megohms for junction transistors. In addition such collector current sources should include some self voltage-limiting to prevent excessive collector dissipation.

The emitter current source, collector sweeper and indicator are used to plot the output collector and the base feedback characteristics. The collector current source and emitter sweeper are used in plotting the forward and input characteristics. Analysis of these families of characteristics shows that the information in each is duplicated in one of the others, so that two may be discarded without loss of data. The selection of the collector and base pair of characteristics keeps measuring equipment complexity at a minimum by eliminating the need for a collector current source.

For exact quantitative results in small signal work the parameters must be measured at the desired operating point. This can best be done with two current sources, but it may also be done using combinations of emitter current sources, series resistance collector loads, and voltage sources.

In large signal or switching circuitry the average values of the parameters over the region of operation are desired. Direct currents and voltages may be read at discreet points in such a way that average values may be determined with sufficient accuracy to give good quantitative results in circuit analyses. In addition, this scheme is particularly convenient for handling large numbers of point contact transistors by semi-skilled personnel.

If a transistor is short circuit unstable, then open circuiting either pair of terminals results in stable operation. Since all measurements of these parameters use at least one current source, short circuit unstable units are measurable. It must be pointed out that in some measuring circuits, particularly the measurement of α, care must be taken to minimize the capacity shunting the current sources to insure stable operation of the equipment.

SUMMARY

Summarizing briefly, the open circuit impedance representation of junction transistors is good at low frequencies, but somewhat more complicated at high frequencies as illustrated. In addition measurement equipment, namely collector current sources, may be difficult to engineer. For the point contact transistor, measuring equipment can be simple in design. These parameters well represent the point contact transistor in both large and small signal circuitry at all frequencies of interest.

Signed Nolan T. Jones
Nolan T. Jones

Approved D. J. Eckl
D. J. Eckl

Approved
N. H. Taylor

NTJ:jrt

Attached drawings: A-55268
A-55260
A-55261
A-55266
A-55262

Distribution 3

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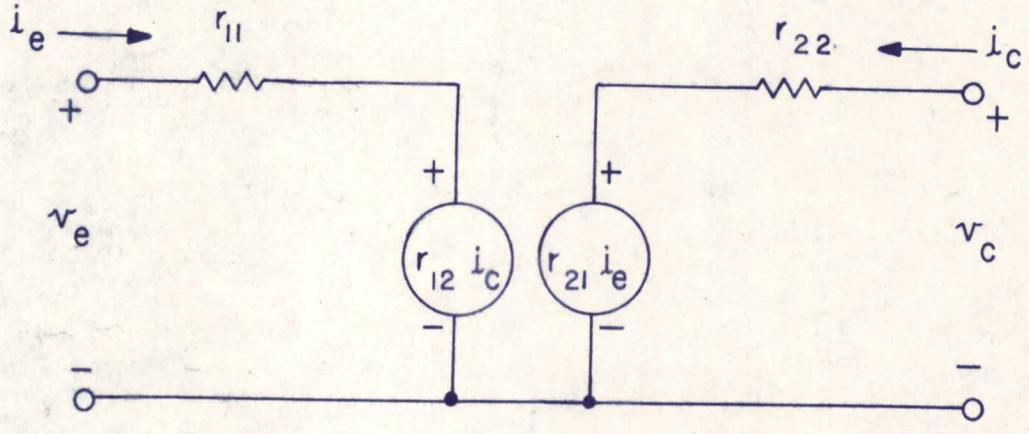
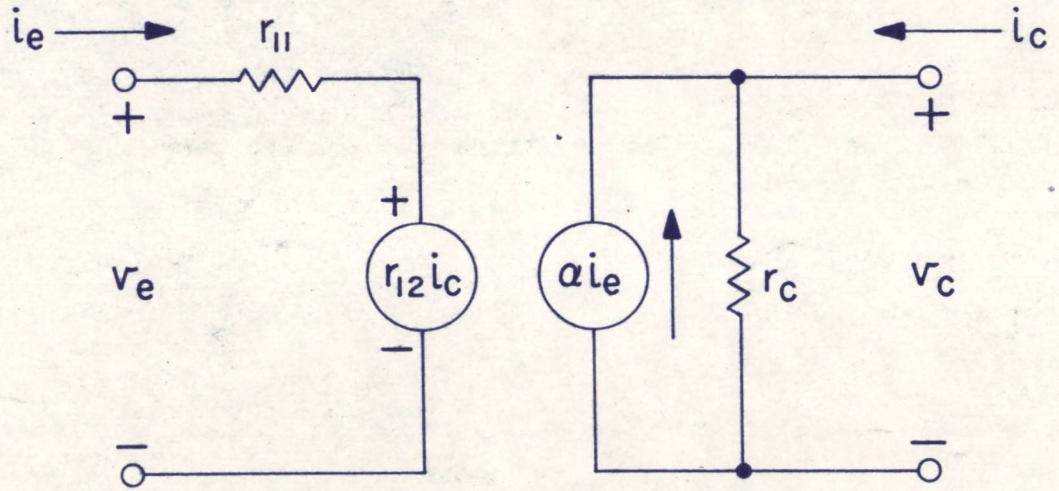
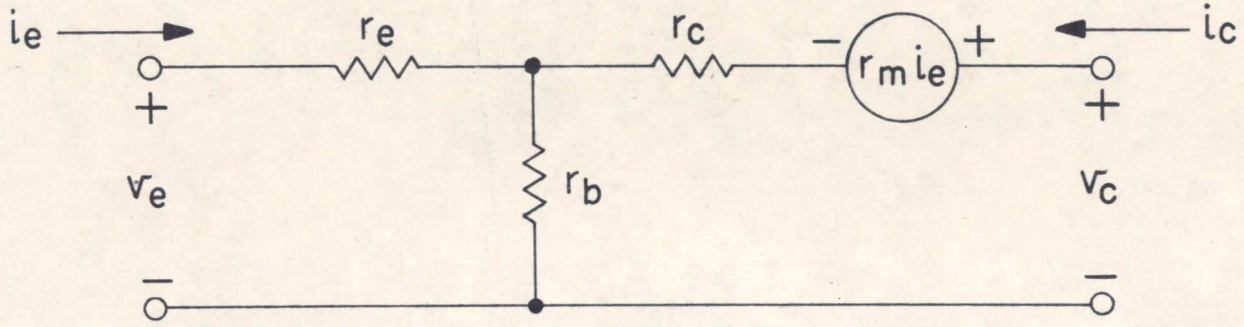


EQUIVALENT CIRCUIT A

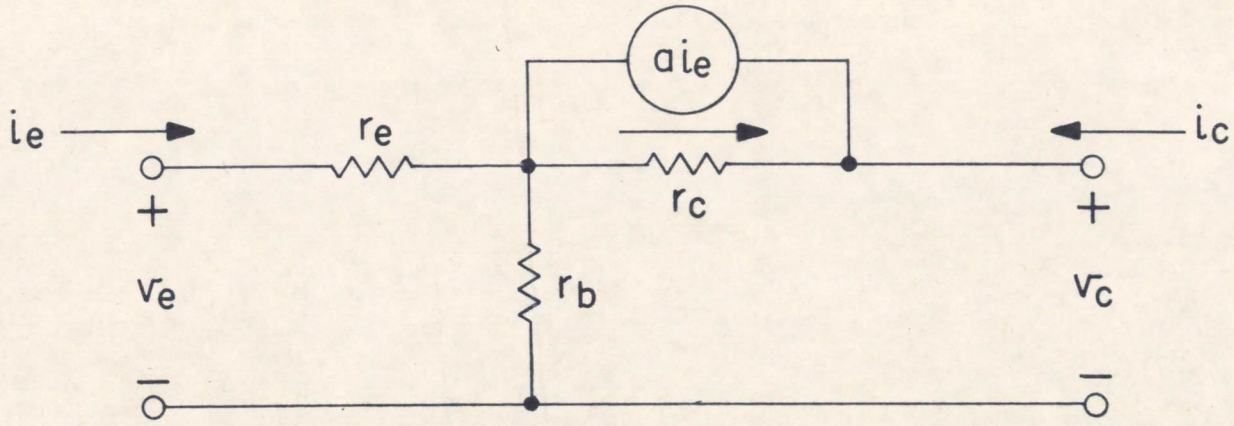
A-55260 Jones
F-1945
SN-575



EQUIVALENT CIRCUIT B

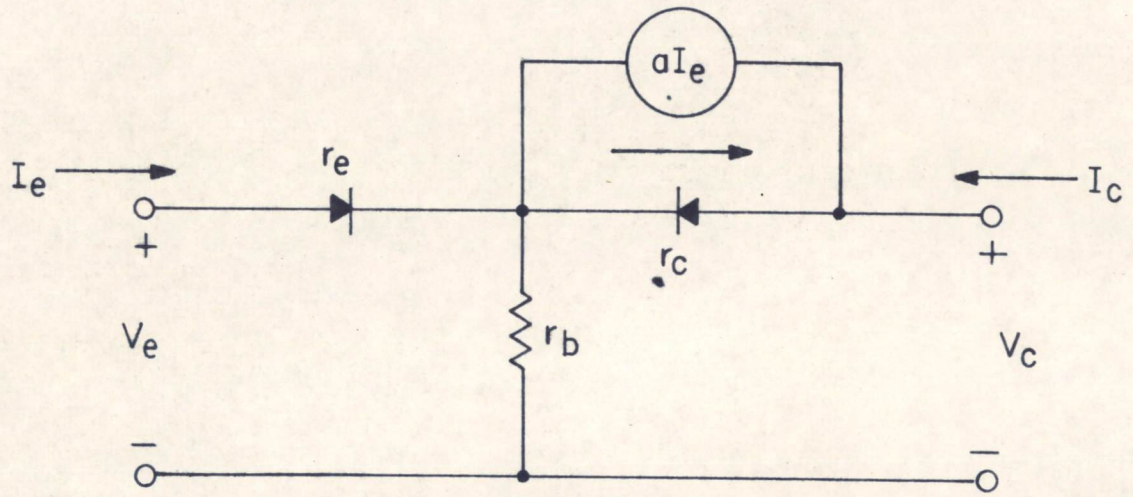


"T" EQUIVALENT CIRCUIT A



"T" EQUIVALENT CIRCUIT B

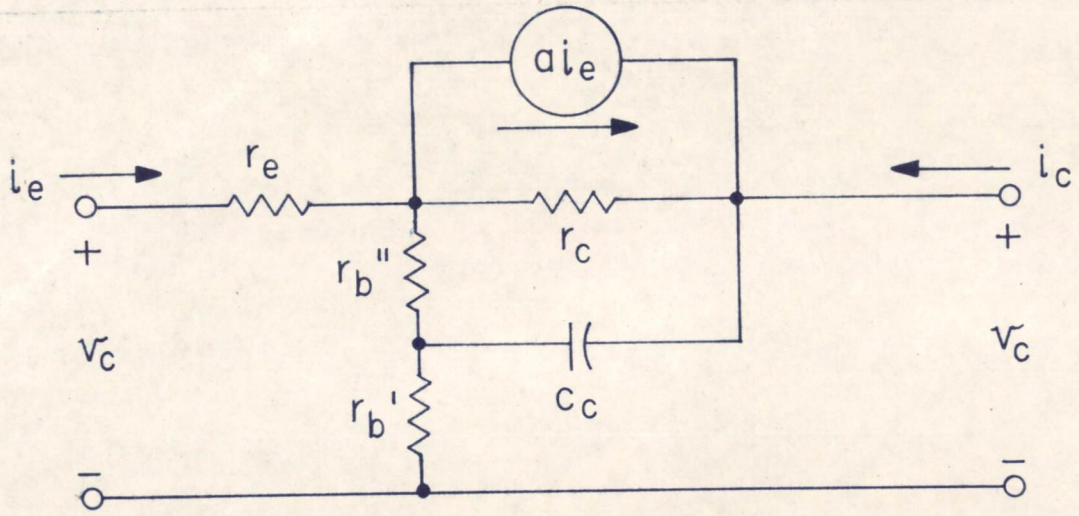
A-55266 Jones
F-1949
SN-579



$a \cong \alpha \quad I_e > 0$

$a \cong 0 \quad I_e < 0$

LARGE SIGNAL EQUIVALENT CIRCUIT



$$a \cong \frac{\alpha_o}{1 + j\frac{f}{f_c}}$$

"T" EQUIVALENT CIRCUIT

JUNCTION TRANSISTORS AT HIGH FREQUENCIES