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Subject: NOTES ON THE LOGICAL DESIGN OF THE IBM 701 COMPUTER

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From: R. P. Mayer

Date: October 8, 1952

Abstract: The IBM 701 computer has logical characteristics similar to WWI except for terminology, the use of half-words, the use of a slightly different central control system, the use of diode logical circuits for handling both voltage "levels" and pulses, etc.

IMPORTANT NOTE:

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1.* Introduction.**

The general physical outline of the 701 computer is shown in the floor plan of Figure 1. Actually, only the control unit is designated by the number 701, while the other units have other numbers. The over-all system has no number, but is called an Electronic Data Processing Machine (EDPM). The title "Defense Calculator" is obsolete.

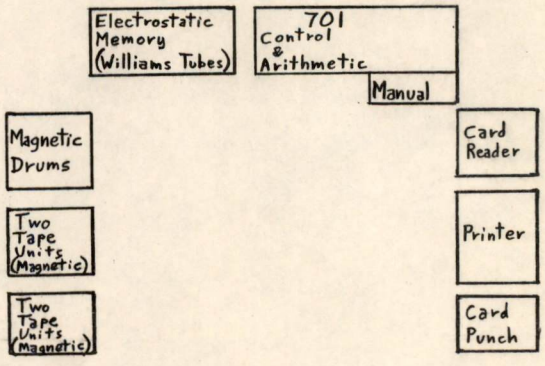


Fig. 1. Physical Outline (Floor Plan)

* Appendix F is a table of contents.

** This paper has not been fully checked by IBM and may contain some errors.

1.1. Drawings

The system drawings for the "701 and associated equipment" are bound in two volumes. These are indexed by block outlines which show a system number for each block, and these numbers correspond roughly to the page numbers in the books. These system drawings are called block diagrams, but they are almost exactly equivalent to our block schematics. The 701 system has no drawings like our block diagrams.

1.2. Characteristics.

The general logical characteristics of the 701 system are tabulated in Appendix A, which should be studied at this point. Details on the circuit of the "Havens delay unit" may be obtained from Dick Best.

1.2.1. Word Length.

Each half-word is 18 bits long and has its own address. All instructions, and any numbers, are stored as half-words. In this sense, the half-word is almost exactly like the WWI "word".

The arithmetic registers normally work with words 36 bits long. Such a word is called a "full-length word", or just "word". A half-word is always treated as the left half of a full word whose right half is all zeros. Most of the 701 system handles each number (not instruction) as a single, full-length, parallel word.

1.2.2. Addresses.

The address of each instruction refers to the location of a half-word. If the sign digit of the instruction is positive, then the addressed half-word is referred to. If the sign digit of the instruction is negative, then the full-length word referred to is the one made up of the two half-words whose addresses are obtained by making the units digit of the specified address first zero and then one.

1.2.3. Storage Tube Layout vs. Addresses.

The Williams tubes are laid out much like the MIT Electrostatic storage tubes. Each shielded box is called a "drawer", and contains two ES tubes (one from each bank) and associated logical circuitry. Each drawer represents one digit of a full-length word,

so there are 36 drawers. (See Figure 2.) Each tube holds 512 spots (dots or dashes). There are two banks, so memory contains 1024 full-length words, each one with an even-numbered address. There are consequently 2048 half-length words, numbered consecutively. An eleven-bit address is necessary, but a twelve-bit

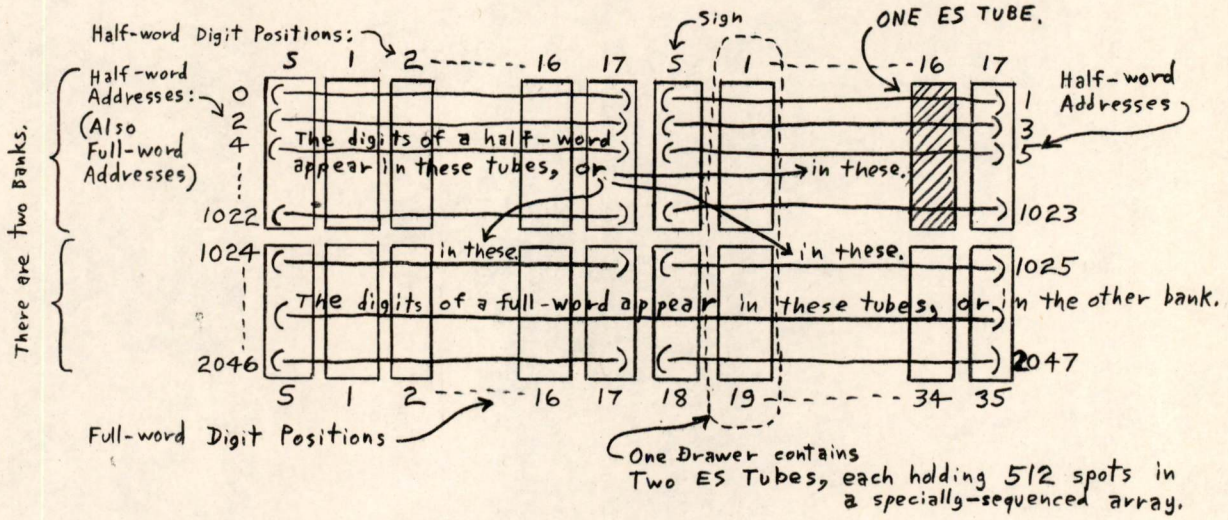


Figure 2. ES Addresses.

address is provided so that an additional storage block can be plugged in.

1.2.4. Signs and Negative Numbers.

The sign digit of a number does not enter into arithmetic operations, but is manipulated independently, as discussed in sections 3.2.3 and 3.2.7. The physical location of the sign digit with respect to other digits has no significance. Thus a full-length number is said to contain 35 bits plus sign; a half-word, 17 plus sign.

1.2.4.1. Interpretation.

The numerical digits are always of positive magnitude, and the sign digit indicates whether the whole number should be negative or positive. Thus, the blank part of a half-word is represented by zeros regardless of whether the number is positive or negative.

1.2.4.2. Location of Sign Digit.

Although the sign position is not associated with any digit position of a number, it must be stored in some position in storage and other registers. This position is, as in WWI, at the left end of the number. Also, as mentioned above, the sign digit does not enter into the numerical part of the calculation. If it is desired to manipulate on the sign digit numerically, it can be stored in an odd-numbered half-register, as shown in Figure 2. It can then be brought into ACC as the middle digit of a full-length number.

1.3. Terminology.

The terminology for the 701 computer is tabulated, and compared with WWI terminology, in Appendix B. An attempt has been made to use 701 terminology throughout most of this note. Where both the 701 and WWI terms are used, the 701 term is written in ALL CAPITALS (which is standard for much of the 701 literature), and the WWI term is placed in /brackets/. Particularly troublesome terms are mentioned below.

AC - The 701 AC is either arithmetic-control or else the ADDRESS COUNTER (which is sometimes called the INSTRUCTION COUNTER or the PROGRAM COUNTER).

The 701 accumulator is called ACC.

Block Diagram - The 701 BLOCK DIAGRAM is like the /block schematic/.

The 701 has no /block diagram/.

Delay Unit - The 701 DELAY UNIT is also called the HAVENS UNIT, and is described in section 1.4.

The 701 has no /delay element/.

Memory Register - The 701 MEMORY REGISTER is like the /PR/ and /AR/ because it acts as a buffer out of storage (but not into storage) and adds directly into ACC.

The 701 /memory register/ is called a MEMORY LOCATION.

Reset - The 701 RESET is like /clear/, but sometimes is like /set/.

The 701 /reset/ (to some number, α) is called SET.

Switch - The 701 SWITCH is like a set of /read in gates/.

The 701 /switch/ is called a MATRIX, or DECODER.

Transfer - The 701 TRANSFER is like /sp/ or /cp/.

The 701 /transfer/ is called STORE, or COPY. (The COPY instruction is like /rd or rc/.)

Trigger - The 701 TRIGGER is like /FF/, and is abbreviated "T".

The 701 /trigger/ is also called "trigger" (verb) (in lower case).

1.4. Symbols.

The symbols used in the 701 BLOCK DIAGRAMS are shown (and compared with WWI /block diagram/ symbols) in Appendix C. There is little neeed to follow these symbols when drawing /block diagrams/ of the 701 circuits, and so WWI /block diagram/ symbols will be used in 701 /block diagrams/ except where 701 BLOCK DIAGRAM symbols will give a clearer picture (as in multiple-input AND /gate/ circuits, or negative AND circuits, etc.). Note that the major differences that will result from this technique are: replacing OR circuits with /arrowhead mixers/, and using a /FF/ whose inputs and outputs might be mixed up with respect to those of the corresponding "T".

1.4.1. TRIGGER.

Notice (Appendix C) that the TRIGGER circuit is like the /FF/, but that the lines to the box are considered to behave just as if a circuit schematic were inside the box. Thus, a positive pulse on the righthand side, or a negative pulse on the lefthand side, will cause the righthand tube to conduct and make the righthand outputs "low". The upper output comes directly from the plate, while the side output comes from a voltage divider connected to the plate. The TRIGGER is not labeled with a 0 or a 1, but a convention has been established: if the righthand outputs are "up", the TRIGGER is said to be "on" and is said to contain "1", and vice versa. Notice that the "TWEAKER" is simply a convenient terminal for manually changing a T, and has no logical significance.

1.4.1.1. Read in to a TRIGGER.

A number is usually read into a TRIGGER register by first RESETTING /clearing/ it and then /pulsing the opposite sides/. An exception is the input to the MDR (MEMORY DEFLECTION REGISTER) /ESD/.

One digit of this is shown in Figure 3. The operation of this circuit can be deduced from the symbols of Appendix C. The T is pulsed either negative or positive, depending on whether the input digit is high or low.

1.4.2. DELAY UNIT (HAVENS DELAY).

Notice (Appendix C) that the DELAY UNIT is the only kind of delay unit used in the 701, and that its output is a "level" which changes to the value applied at the input only at the time that the clamp signal appears. This time coincides with the end of the sync gate, which has admitted the input level. Thus the output of such a unit does not change until just as the input becomes no longer significant.

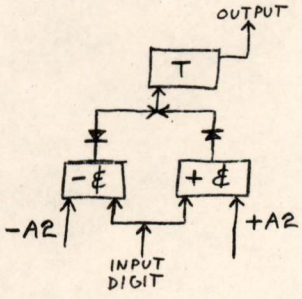


Figure 3. Input to MDR.

1.4.2.1. Read in to a DELAY UNIT.

A typical DELAY UNIT SWITCHING circuit is shown in Figure 4. Notice that the unit "looks at its own tail" when no control signal is applied, and therefore acts like a /dynamic FF/. If a control signal makes it "look at" some other unit, then it is prevented from looking at its own tail. It then assumes the value of the specified input number, whenever a clamp signal (not shown) appears.

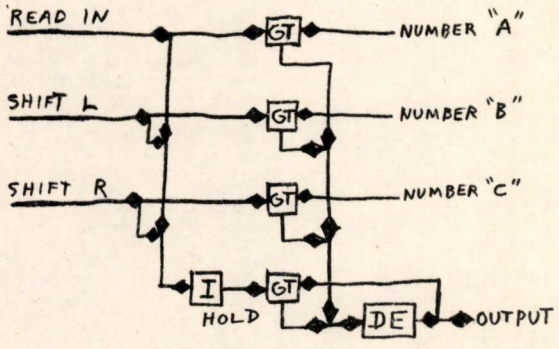


Figure 4. Input to DU.

2. General Logical Design.

Appendix D lists the 701 order code and compares each operation with the equivalent WWI operation, with only a short note to explain the difference. It is hoped that anyone familiar with WWI operation will get a reasonably accurate picture of 701 operations by looking at Appendix D. It may be necessary to refer to sections 2.1 and 2.2 (on Block Outline, and Timing) in order to understand the operations.

2.1 Block Outline.

The over-all logical organization of the 701, shown in figure 5, is very much like WWI. The major differences are as follows:

Stored spots are not [held] all at once, but a group of spots is REGENERATED whenever possible. The REG. COUNTER keeps track of which spots must be regenerated next. Each regeneration regenerates a spot in every tube (i.e., four addresses at once). Thus, it is necessary to include (in the memory drawers) a TRIGGER for each storage tube. These T's form two registers, each much like our [PR]. But, as they play no part in the logic of the machine, they have no special name.

The MEM. REG. acts like [PR] when reading out of storage, except that addresses also go through INSTR. REG. before going to MEM. DEFL. The MEM. REG. also acts like [AR] when doing arithmetic. After a half-length number is placed in MEM. REG. (see section 1.2.1., and note on figure 5) it is handled as if it were a full-length number.

MEM. REG., ACC, and MQ use DELAY UNITS. A "D" cannot be complemented directly, so ACC is complemented by running its contents through the complement part of the TRUE/COMPLEMENT (T/C) circuit and the adder (adding in Zero). (See section 3.2 for arithmetic details).

The MQ (Multiply/Quotient) is most like [IOR], but is also used for [BR]. While tape is using [IOR], care must be taken to prevent any other use of MQ.

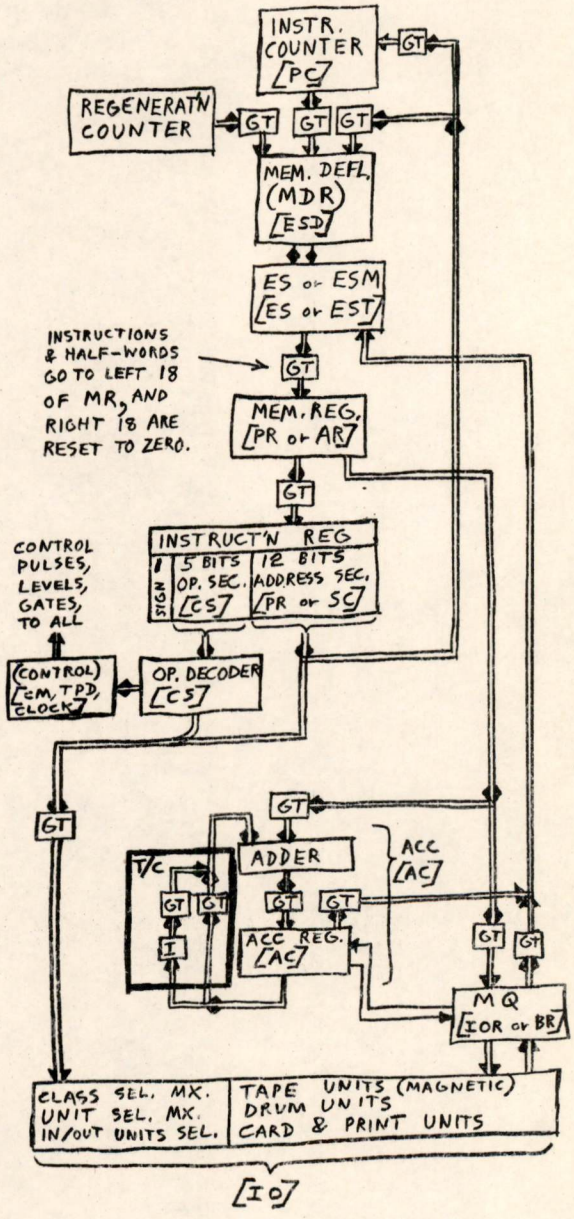


Figure 5.
701 BLOCK OUTLINE

2.2 Timing Outline.

A general outline of the timing for ADD is shown in figure 6. The general outline for other instructions may have more cycles or less. There are two kinds of signals sent throughout the computer to indicate the point in the timing of a single instruction: time pulses (0 through 11) and CYCLES (I,E,E/R,R). Each cycle refers to a complete processing of one word of storage. (Each R or E/R refers to four addresses. See section 2.1.) Notice that any part of [operation timing] which does not need to use storage allows storage to regenerate, and so is made an E/R cycle. The R cycles do nothing but regenerate storage, and can be omitted if storage is in good shape, as discussed below. If they can not be omitted, an ADD takes 60μs, as shown. (Regeneration is "safe", and the programmer never needs to think about it.)

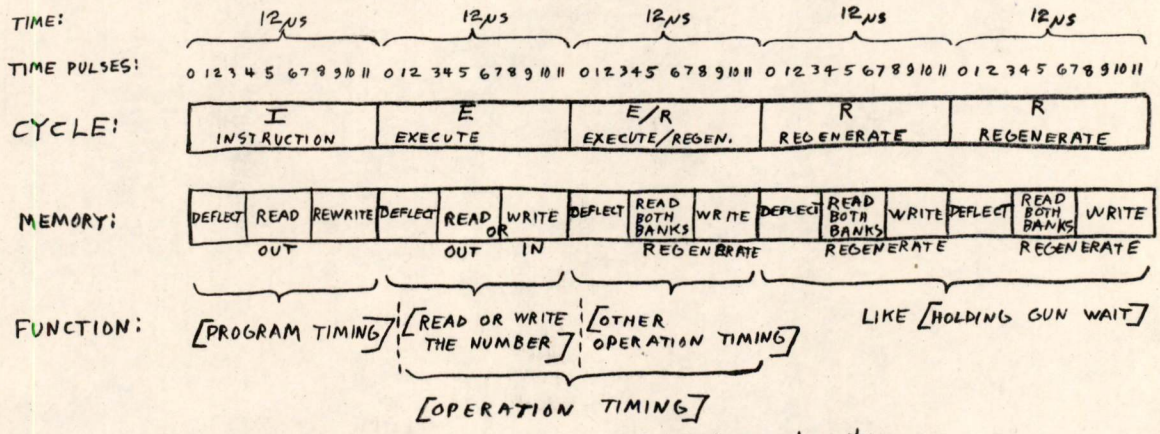


FIGURE 6. Outline of a typical ADD instruction.

2.2.1 "Free games" technique.

One E/R cycle is used for each step of multiply or divide. Thus, one of these operations regenerates a great deal of storage, and it is safe to omit the R cycles on the next twelve instructions of a program. Whenever a MULTIPLY, MULTIPLY-ROUND, or DIVIDE is performed, a counter starts counting instructions as they are performed and allows twelve to occur without any R cycles. This counter is popularly called the "free games" counter. A single multiply or divide takes quite a long time, but if it is followed by twelve ADD's (for instance) then the apparent multiply or divide time is about as short as a single ADD time.

2.2.2. Traffic Outline.

Figure 7 shows a rough outline of the flow of information from register to register during an ADD instruction. The vertical axis shows the registers laid out as in Figure 5. The horizontal axis is "time", as in Figure 6. A dotted line shows the influence of MEM. DEFL. on ES. At the "end of operation", the I cycle line comes on, but is suppressed until R cycles are completed. The two inputs to the adder are actually applied throughout the transient period and until the result is read to ACC.

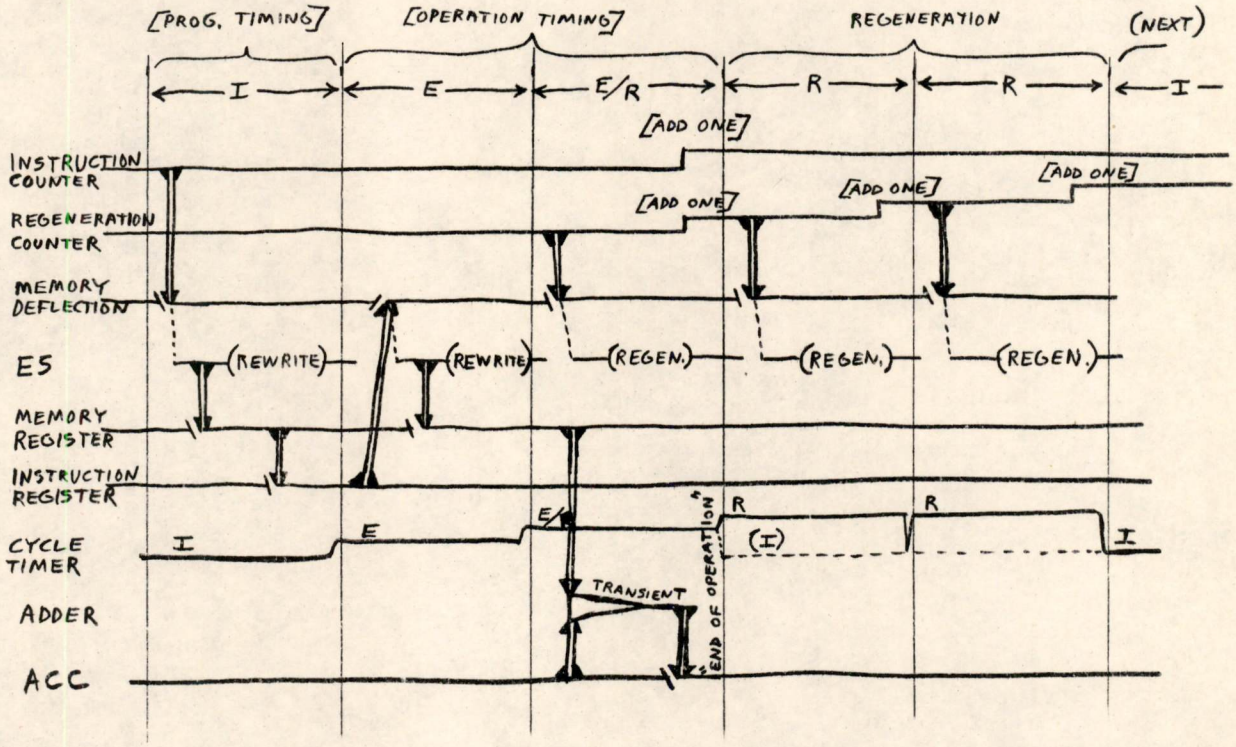


Figure 7. Traffic Outline for a Typical ADD.

3. Some Details.

The following sections provide a little more detail on some aspects of the 701 system.

3.1. Control.

The general outline of [central control] is shown in Figure 8. A clock distributes 12 time pulses. A cycle timer determines the kind of cycle, with the regeneration control telling whether an R is needed or not. The INSTRUCTION REGISTER [CS] tells what operation to perform. These three kinds of signals are combined with other conditions within the machine to provide control signals.

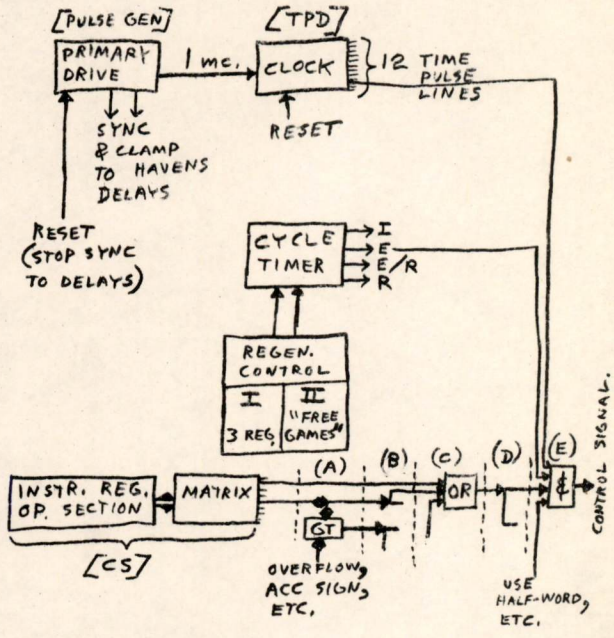


Figure 8. Outline of Control.

3.1.1. Primary Drive and CLOCK.

The primary drive [pulse generator] supplies 1mc. pulses to the CLOCK [TPD]. It also supplies sync and clamp pulses to the delay units, which can be [cleared] RESET by stopping the sync pulse.

The CLOCK never stops, because regeneration must take place if nothing else. It contains 12 T's, only one of which is ON at a time. When it goes OFF it forces the next one ON. The odds and evens are alternately pulsed OFF by a 13th T. The ON consequently progresses around the ring. The CLOCK is "stopped" if more or less than one T is ON. It is "reset" by holding the number zero T ON until all the others are OFF, and then letting it go.

3.1.2. Regeneration Control.

The regeneration control is sketched in the bottom half of Figure 9. The counter on the left side counts to make sure that each instruction has three regenerations, and if so, "R-completed" line is ON, allowing the cycle timer to go to the I cycle. If the R cycles are not completed, the "R-required" line is ON, keeping the cycle timer in the R cycle. The counter on the right is the "free games" counter, which is RESET [cleared] at the beginning of operations like "multiply". It counts once on every instruction until 13 instructions have been started, and during this time the "R-completed" line is turned ON, indicating that no R is required at the ends of the twelve intervening instructions.

3.1.3. Cycle Timer.

Part of the cycle timer is sketched in the top half of Figure 9. It has four T's. At the end of an operation (see also Figure 7) the I TRIG is turned ON. But if an R is required, the R TRIG is also turned ON, and this suppresses the I output line. As soon as enough R cycles have been completed, the R TRIG is turned OFF, allowing the I line to come ON. This same sort of arrangement is used (not shown) when the computer is operated in a manual fashion, so that the R line is on when you have manually stopped the computer, and yet the other TRIGGERS remember what cycle the instruction is in when you want more pulses in the computer.

A negative AND gate (not shown) in each of the top three TRIG inputs allows a negative pulse to turn OFF the TRIGGERS which are not being turned on. Thus, the setting of one TRIG /clears/ the others (but the R TRIG is special, as described above).

3.1.4. Control Signals.

The general method of obtaining control signals was mentioned in section 3.1, and sketched in Figure 8. Notice that the output lines from the MATRIX /cs/ do not go to a /control matrix/ but to a system of AND and OR gates, called EXECUTION CONTROLS and EXECUTION CONTROL MIXERS. Roughly five sections to these circuits can be recognized: (A) a MATRIX line is combined, if necessary, with other conditions in the computer to find out what kind of instruction is called for. (B) The resultant signal is sent to the various OR circuits which control the kinds of /commands/ required.

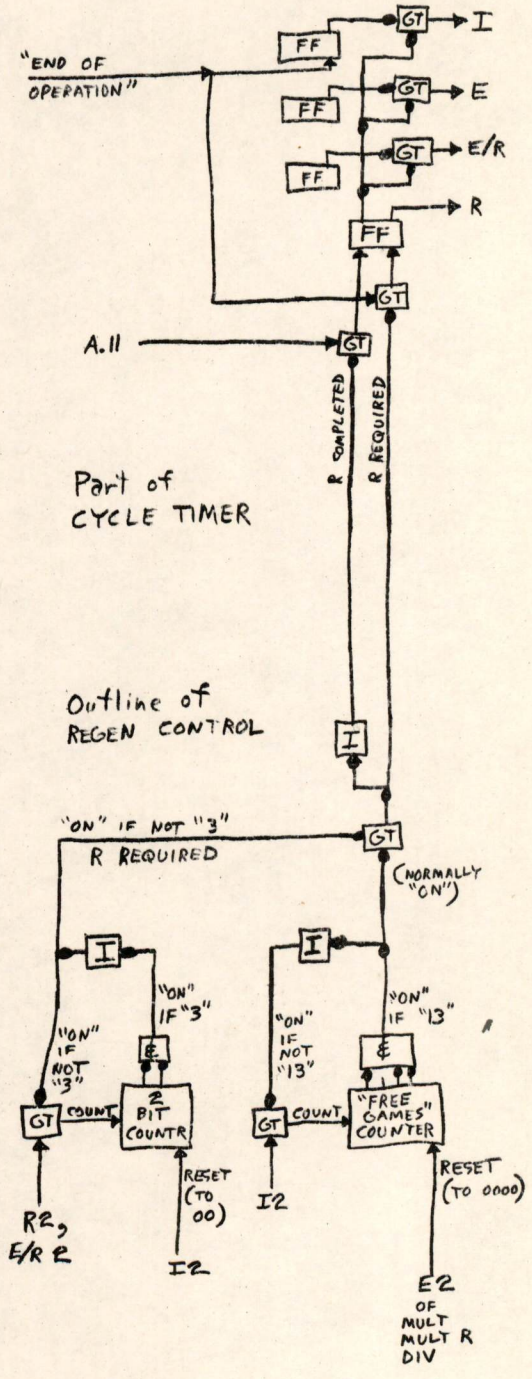


Figure 9. Simplified Sketches of CYCLE TIMER & REGEN. CONTROL.

(C) The OR circuits activate these /commands/ regardless of the instruction which calls for them (Sections B and C are roughly equivalent to the inputs and outputs of the /control matrix/).
(D) The signal is then split up, if necessary, into several AND circuits in order to combine with other conditions in the computer.
(E) A control signal appears if its AND circuit finds that conditions, cycle, and time pulse are correct (this section is roughly equivalent to the /cpo units/).

3.2. Arithmetic.

Arithmetic in the 701 is much like that in WWI except for the method of handling overflow and signs, and except for the adder circuits.

3.2.1. Digits in ACC.

The ACC has two digits which never appear anywhere else. (See Figure 10). They are called P and Q (pints and quarts) and represent the digits 2^0 and 2^{+1}. These digits are added and shifted along with the remaining digits of the number so that double-length numbers can be added simply by letting the overflow go into the P and Q digits and then later shifting these digits to the least significant end of the ACC and adding in the most significant part of the double-length number.

The binary point of the 701, as with WWI, can be considered anywhere for addition and either at the extreme right or at the left (between P and 1) of single-length multiplicands and their double-length product. An attempt is made not to think of any particular location for the binary point of the 701 system, but when confusion must be avoided the same convention as WWI is usually used.

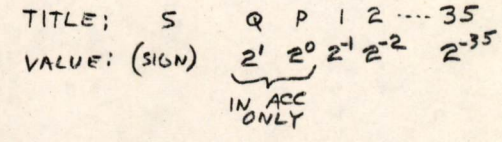


Figure 10. Digits of ACC.

3.2.2. Overflow.

Whenever an overflow occurs into the P digit (when adding, rounding, or shifting left) an overflow T is turned ON. This T remains ON (lighting a light on the operator's panel, but not influencing the operation of the computer) until a TRANSFER OVERFLOW instruction is performed, which senses the overflow, TRANSFERS CONTROL if necessary, and RESETS the overflow T.

3.2.3. Sign Control for Add.

Because of the method of representing negative numbers (see section 1.2.4.1), a subtract instruction is the same as an add except that the sign digit (but not the number digits) is considered to be complemented. The adding and sign-handling circuits are (with the above slight exception) not concerned with whether a positive number is being subtracted or a negative one is being added. Thus, the analysis of ADD describes SUBTRACT as well.

3.2.3.1. The Simple Cases.

If the two numbers being added have the same sign, we wish to let one magnitude increase the other, and we know the sign of the result must be the same as that of the original numbers. Thus the two numbers are simply added and the ACC sign is not touched.

3.2.3.2. The Other Cases.*

If the two numbers being added have unlike signs, we wish to let one magnitude decrease the other. We must then decide what the resultant sign should be. The result will have the same sign as the original ACC if the magnitude of ACC is large enough to nullify the magnitude of MR.[AR](See Figure 11.)

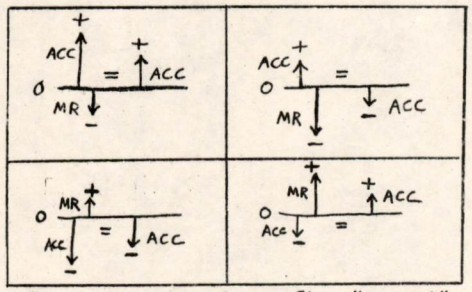


Figure 11. ACC Sign after "subtract".

Since a magnitude smaller than zero can not be represented directly, the decreasing of magnitudes can not be done unless one of the numbers is complemented. As in WWI, the 9's complement is used, thus letting "111111---111" represent "0" [minus zero] (or [-0]). (Notice, however, that ACC sign is not involved in this complementing.) Therefore, the complement of the magnitude of ACC is added (by way of the T/C circuit of Figure 5) to the magnitude of MR. This accomplishes the decreasing of one magnitude by the other with respect to [-0], as shown in Figure 12. (The brackets show the relationship between the ACC magnitude and its negative-magnitude-with-respect-to [-0], and show also the resultant magnitude-with-respect-to [-0].) The magnitude

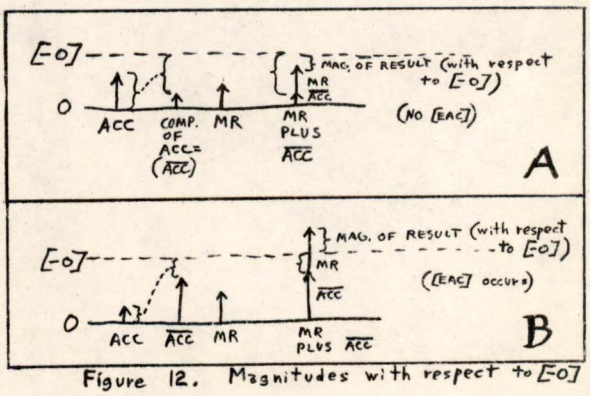


Figure 12. Magnitudes with respect to [+0]

*An explanation not used by IBM, but presumably giving the correct results.

must then be returned to its correct form. In Figure 12B, the magnitude is above ⌈-0⌋, so an ⌈EAC⌋ (end around carry) (as in the WWI system) has occurred, and the magnitude is in correct form. In Figure 12A, however, no ⌈EAC⌋ has occurred, so the ACC must be complemented again (by sending it alone through the T/C and adder of Figure 5) to arrive at the correct magnitude.

So far, our addition of unlike signs has produced the correct magnitude. (An overflow can not arithmetically occur, so it is not sensed.) All that remains is to find the correct ACC sign. As in Figure 11, the sign digit of ACC must not be changed if the magnitude of ACC is large enough to nullify the size of MR. This occurs in the case of Figure 12A. Thus, if no end around carry occurs, the ACC sign digit is not changed, and vice versa as in Figure 12B.

As in WWI, a result of "zero" produces no end around carry. But unlike WWI, the above rule says that in this case ACC sign is not changed, but the magnitude is complemented. So the sign of a "zero" remainder is always the same as the original sign of ACC, and the number digits are all zero.

3.2.3.3. Rule for Sign Control on ADD.

Signs same: add magnitudes; leave sign alone; set overflow T if necessary.

Signs different: add complement of ACC magnitude to magnitude of MR; forget overflow.
Then: - - if no ⌈EAC⌋: (|ACC| ≥ |MR|; Figure 12A); complement ACC, but not ACC sign.
- - if ⌈EAC⌋: (|ACC| < |MR|; Figure 12B); complement ACC sign, but not ACC.

3.2.4. Adder.

The circuit for the passive adder is shown in Figure 13. Only one digit is shown. A "sum" output appears if all three of the inputs are ON, or if any of them is ON and there is no "carry out". The "carry out" is turned ON if any two or more of the three inputs are ON. Thus, when the input gates are turned ON for 6 μsec, the circuit outputs eventually stabilize. It takes the carry levels about 3.5 μsec to become stabilized from one end of the complete adder to the other. Thus a safety margin is included, since the pulse "sum to ACC" occurs 5 μsec after the start of the read-in gate. The sum is then fed to the ACC DELAY UNITS,

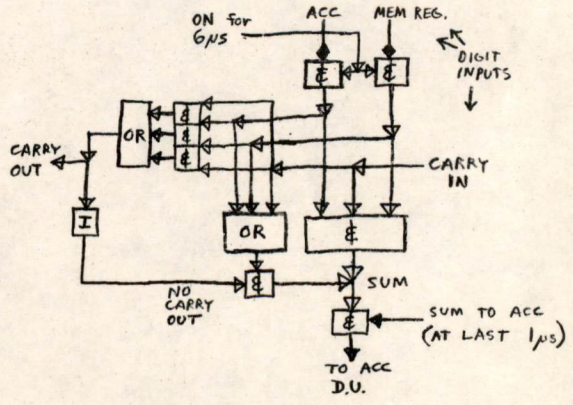


Figure 13. ADDER DIGIT

and they eventually become set to the correct sum.

3.2.5. Shift Counter.

The ADDRESS SECTION OF THE INSTRUCTION REGISTER receives the address section of all instructions and is therefore used as the [step counter] for shifting and also for multiply and divide. A shift of up to 255 can be programmed, and any shift over 72 will clear both ACC and M/Q. The reason for allowing such large numbers of shifts is that a calculated scale factor can be inserted as the address of a shift instruction with some assurance that large numbers of shifts will clear the register instead of simply producing small numbers of shifts (i. e., a shift of 128 would result in a shift of 0 if this feature were not provided).

3.2.6. Shifting.

Shifting is accomplished by making each DELAY UNIT of ACC (including P and Q) and M/Q "look at" its neighbor instead of "its own tail" (see section 1.4.2.1.). A shift of one place per μsec. occurs as long as they look at their neighbors, so the shift line is merely turned ON for the length of time determined by the [SC] Actually, no more than 8 shifts occur on any E/R cycle. See Appendix D for long and short shifts, and sign control for shifts.

3.2.7. Sign Control for Multiply and Divide.

The sign control for multiply and divide is similar to that of WWI except that the numbers themselves are already in positive magnitude form, and except for the fact that both ACC and MQ have sign digits which must be correct. (The "divide" leaves a quotient in MQ with its sign, and the remainder in ACC with its sign. See section 3.2.8.)

3.2.8. Dividing.

In the "divide" operation, the adder is sensed to discover whether a subtraction was too much, and if so, the sum is simply not copied into ACC. Thus, ACC always contains a regular remainder, rather than the plus-or-minus remainder found in WWI, and no corrective add is required.

3.3 In-Out.

As with WWI, the in-out system has so many variables that it is not as easy to describe as the rest of the system. The following notes, therefore, are even less complete than the preceding notes.

To operate an in-out unit, the general procedure is to use an instruction READ or WRITE, like /si/, followed by any number of COPY instructions. The /si/ used selects the type, mode, and unit to use, while each COPY actually copies a word into or out of ES depending on whether READ or WRITE was used as /si/. If a COPY is not programmed in time, the in-out unit in use at the moment usually simply disconnects itself from the computer and eventually stops. If a COPY occurs too early in the program, the computer simply waits. See Appendix D.

3.3.1. Card Characteristics.

Standard IBM cards can be punched in binary fashion under a program of control from the computer. When punched in this way, each 80-bit row of the card will contain two full-length words, or 72 bits. There are 24 full-length words, or 48 instructions, on each card. These cards read into ES under the control of a program in much the same way that paper tape reads into WWI. Standard alphanumeric cards can also be read in by way of a special program.

3.3.1.1. Card Read-in Program.

A special loading card can be read in by means of three simple instructions programmed by pushing the LOAD BUTTON. One of these instructions is a COPY, which brings in the first word (2 instructions) from the card. One of these new instructions brings in another word, and so the card pulls itself into ES by its own boot straps. The remainder of this loading card has on it a program much like our read-in programs, and allows reading-in the remainder of the cards in a deck. The remaining cards of the deck each have a check number, a starting address, and a number indicating how many registers should be loaded from the card. The last card in the deck tells where to start the program that has just been read in, and is called the TRANSFER card. The cards between the load and the TRANSFER card can be in any sequence, since each has its own starting address.

3.3.1.2. Reader, Punch, and Printer.

The reader can read cards at a maximum of 150 cards/minute.
The punch can punch cards at a maximum of 100 cards/minute.
The printer can follow cards at a maximum of 150 cards/minute, and prints one line for each card. (It cannot follow binary-punched cards.)

In order to operate the punch and printer, these devices must receive information as if it were coming from a standard IBM card. This usually means that the information has to be calculated beforehand, and placed in storage as a "card image". This card image can then be copied half-row by half-row into the punch or printer.

3.3.2. Drum.

The following paragraph is to be considered HIGHLY COMMERCIALLY CONFIDENTIAL.

The drum circuit involves the use of a single counter, and the address of the desired drum register is placed in this counter by a special instruction. This counter does not count until the specified drum passes the zero mark. The counter then counts down until it is empty, at which time the drum is at the proper address. Thus it takes on the average half a revolution to start counting and half a revolution to reach the specified address, so that the average time is one complete drum revolution to find an address. The average time will be only half a revolution if addresses near the zero mark are specified, and these addresses are multiples of 32. There are four "drums" contained on two separate cylinders.

3.3.3. Tape (magnetic).

The magnetic tape contains blocks of information, of any length, with blank spaces between them. A single COPY instruction pulls in a full word length, which involves six lines, each six bits long. When reading, the tape will stop only at blank spaces. The program has full control of what is recorded where, and so must manufacture its own addressing system if one is desired. The tape moves at 75 inches/second, and contains 100 bits/linear inch.

4. Further Information.

Some further information can be obtained from publications in the Whittemore Building Library: Library number 2077, "Defense Calculator Memos", contains memos on the 701, only some of which are concerned with logical design (see list in Appendix E). Library number 2076, "701 Operator's Reference Manual", is a preliminary manual which is largely obsolete. However, the descriptions of operations (beginning in page 54) should be up to date except for the description of the "read backward" (and of COPY after "read backward"). Pages 47 to 51 might also be of interest, though possibly out of date.

Appendix A

Logical Characteristics of 701 System (see section 1.2.)

		(Footnotes)
Type	General-purpose, high-speed.	
Design	Electronic, digital.	
Number system	Binary.	1.
Register length (basic, or full word)	36 Binary digits.	2.
(basic instruction, or ½-word)	18 Binary digits.	2.
Method of handling numbers	Parallel digital transmission, addition, and storage.	
Type of internal storage	Williams electrostatic memory tubes. (2 banks, 512 spots per tube.)	3.
Capacity of internal storage	2048 half-words, numbered consecutively.	4.
Access time to internal storage	12 μ sec. read-rewrite.	5.
Basic functional design	Pulses (usually one μ sec. long) and outputs from basic memory devices are switched via crystal circuits to determine new states for the memory devices.	6.
Basic memory devices	TRIGGER (like WWI FF), and HAVENS DELAY unit.	6.
Crystal switching circuits	AND circuits (like gates), and OR circuits (like mixers).	6.

---

1. See section 1.2.4.1.
2. See section 1.2.1.
3. See section 1.2.3.
4. See section 1.2.2.
5. See section 2.2.
6. See section 1.4.

Appendix B

Terminology (see section 1.3.)

Note: 701 NAMES ARE IN CAPITALS, and /WWI names are in brackets/.
Abbreviations are listed at the end.
(Some names are popular, but not official.)

ADDRESS COUNTER = INSTRUCTION COUNTER = /PC/
BLOCK DIAGRAM = /block schematic/ = SYSTEM DRAWING = LOGICAL BLOCK DIAGRAM
/block diagram/ = 701 HAS NONE
DELAY UNIT = HAVENS UNIT = /see sections 1.4. and 1.4.2./
/delay element/ = 701 HAS NONE
GLITCH = /a botherless negative spike on an ON line/
MEMORY REGISTER = /PR or AR/ (see sections 1.3. and 2.1.)
/memory register/ = MEMORY LOCATION
MULTIPLY/QUOTIENT = /IOR or BR/ (see section 2.1.)
REGENERATE = /hold spots in DS, one spot in each tube at a time/
RESET = /clear/ or sometimes /set/
/reset/ = SET (to some number, x)
SLIVER = /a bothersome spike/
SPIKE = /spike: botherless positive noise on an OFF line/
/step counter/ = 701 USES PART OF ADDRESS REGISTER /PR/
SWITCH = /rather like read-in gates/ (see section 1.4.2.1.), or /diode circuit/
/switch/ = MATRIX or DECODER
TRANSFER = /cp/ or /sp/
/transfer/ = STORE or COPY
TRIGGER = /FF/ or /trigger/(verb)
TRUE NUMBER = /a number in "magnitude-with-sign" form/
TWEAKER = /a convenient terminal for "screwdriver" setting of a FF/
= MANUAL "OFF" (or "ON") PIN CONNECTION.
UNIT RECORD = CARD, or A BLOCK ON TAPE

Some abbreviations:

A = ALL CYCLES, or AMPLIFIER
AC = ARITHMETIC & CONTROL UNIT, or ADDRESS COUNTER
ACC = ACCUMULATOR
D = DELAY UNIT, or DURATION OF SIGNAL (as in "A2(D1)" the duration is 1μ sec.)
E = "EXECUTE" CYCLE
E/R = "EXECUTE/REGENERATE" CYCLE
I = INVERTER, or "INSTRUCTION" CYCLE
MQ = M/Q = MULTIPLIER/QUOTIENT REGISTER /IOR or BR/
MR = MEMORY REGISTER /PR or AR/
OR = OR circuit /mixer/
R = "REGENERATE" CYCLE
T = TRIGGER
T/C = TRUE/COMPLEMENT CIRCUIT

$\&$=&= AND circuit /gate/

Appendix C

Symbols (see section 1.4.)

Time notation:

Example: + E 3 (D 2)

- (D 2) → Signal has duration of 2 μs.
- E 3 → It starts with time pulse 3
- E → CYCLE (I, E, E/R, R. A = ALL CYCLES.)
- + → Polarity at time shown (nothing = plus).

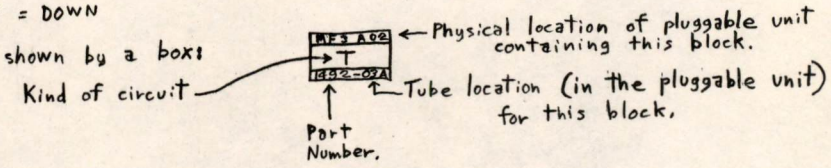
(An input to a T which is not labelled with the time is usually just a TWEAKER, unless it comes from some other circuit.)

Other notations on lines are pin numbers, [System numbers] PAGE NUMBERS, etc.

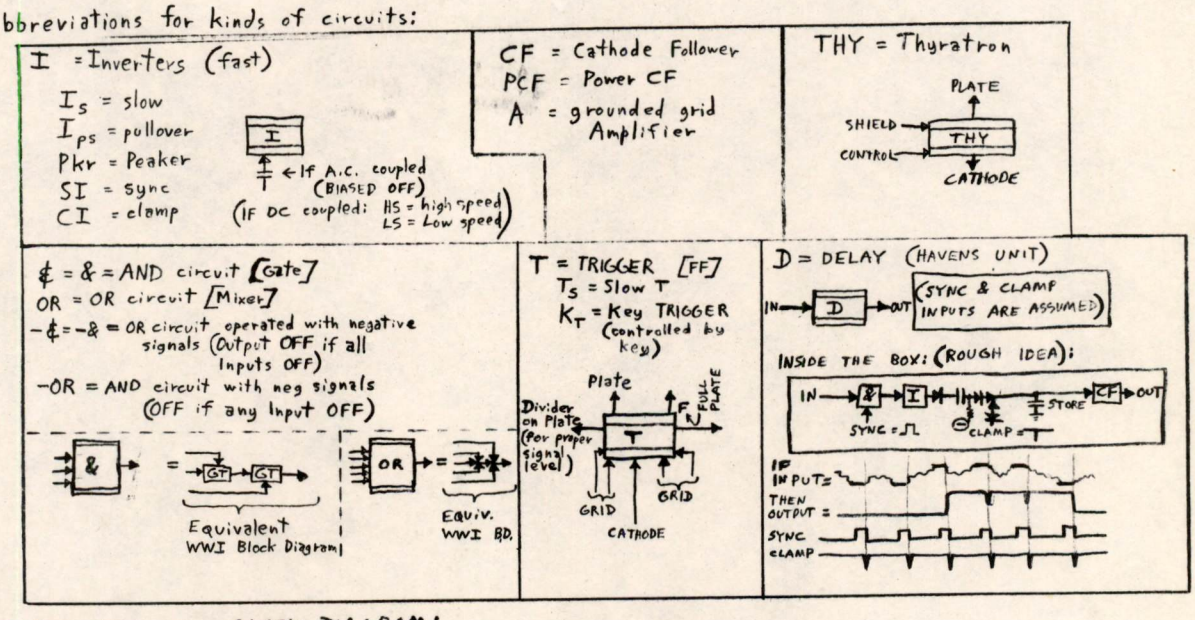
An attempt is made to have information flow from left to right.
So counters count from left to right.

Signal voltages are standard:
+10 (clamped) = ON = UP = HOT = PULLED
from -30 to -15 = OFF = DOWN

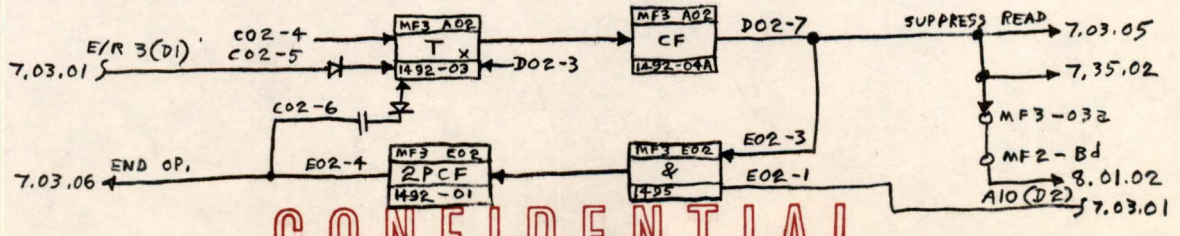
Each standard circuit is shown by a box:



Abbreviations for kinds of circuits:



SAMPLE LOGICAL BLOCK DIAGRAM:



Appendix D - Order Code (see section 2.)

Deci #	Short Name	Symbol	Closest WWI Equivalent	Explanatory notes (see section 1.2.2.)
0	STOP & TR	STOP	sp/rs, stop	(Old & NEW [pc] address is displayed while stopped).
1	TRANSFER	TR	sp	(Old [pc] address is not remembered in [AR]).
2	TR OVERFLOW	TR OV	(cp on overflow)	(This is the only way to sense or to [clear] the overflow TRIGGER.).
3	TR ON PLUS	TR +	(cp +)	
4	TR ON ZERO	TR 0	(cp 0)	
5	SUBTRACT	SUB	su	ZERO RESULT HAS SAME SIGN AS PREVIOUSLY IN ACC. OVERFLOW SIMPLY GOES INTO P & Q AS IF THEY WERE REGULAR DIGITS, BUT ALSO SETS OVERFLOW TRIGGER, WHICH can be cleared only by TR OV.
6	RESET & SUB	R SUB	cs	(RESETS [clears] P & Q DIGITS OF ACC).
7	SUB ABSOLUTE	SUB AB	sm (su magnitude)	
8	NO OPERATION	NO OP	rs, no stop	
9	ADD	ADD	ad	
10	RESET & ADD	R ADD	ca	(RESETS P & Q).
11	ADD ABSOLUTE	ADD AB	am	(ad magnitude).
12	STORE	STORE	ts	
13	STORE ADDRESS	STORE A	td	(12 digits).
14	STORE MQ	STORE MQ	(ts from BR)	
15	LOAD MQ	LOAD MQ	(ca direct to BR)	(No change in ACC).
16	MULTIPLY	MPY	mh	MUST HAVE NUMBER IN MQ (by LOAD MQ), NOT IN ACC, which is lost. PRODUCT SIGN GOES TO BOTH ACC SIGN & MQ SIGN.
17	MPY ROUND	MPY R	mr	(NO [Clear BR]).
18	DIVIDE	DIV	dv	SIGN OF MQ IGNORED, ASSUMED SAME AS ACC SIGN. COMBINED, DOUBLE-LENGTH ACC→MQ divided by MR. QUOTIENT IN MQ; REMAINDER IN ACC with previous ACC sign. (see section 3.2.8.)
19	ROUND	ROUND	srr 0	THIS DOES NOTHING BUT ROUND-OFF. IT DOES NOT CLEAR MQ. SIGN & ADDRESS OF ROUND INSTR. CAN BE ANYTHING.
20	LONG S L	L LEFT	slh	ACC SIGN IS MADE SAME AS MQ SIGN. P, Q, ACC, MQ ARE SHIFTED. OV TRIG IS SET IF "1" GOES FROM DIGIT 1 TO DIGIT P.
21	LONG S R	L RIGHT	srh	MQ " " " " " ACC ".
22	ACC S L	A LEFT	slr	ACC, P, & Q ARE SHIFTED, BUT NOT MQ. LIKE LONG SHIFTS EXCEPT MQ NOT TOUCHED, AND SIGNS NOT TOUCHED. (i.e. OV TRIG.)
23	ACC S R	A RIGHT	srr	(NO ROUND-OFF) (NO MQ [CLEAR]).
24	PREP TO RD	READ	(si read)	USE WITH PRINTER FOR ECHO [FEEDBACK] CHECK, AND ALL INPUTS EXCEPT READ B. (SEE SECTION 3.3). SETS IO INTERLOCK, WHICH IS [CLEARED] ONLY WHEN A UNIT DISCONNECTS. IF INTERLOCK IS SET, IT WAITS FOR DISCONNECT.
25	PREP RD BKWD	READ B	(si rd. backw.)	
26	PREP TO WRT	WRITE	(si write)	
27	WRT END FILE	WRITE EF	(si blank tape)	CLEARS SECTION OF TAPE IF UNIT IS NOT IN READ MODE.
28	REWIND	REWIND	(si rewind)	USE WRITE EF FIRST.
29	SET DRUM ADR	SET DR	(si drum address)	USE AFTER READ (DRUM) OR WRITE (DRUM). ADDRESS = DRUM STARTING ADDRESS. ZERO, IF SET DR NOT PROGRAMMED.
30	SKIP, CONTROL	SENSE	(si light, or cp on manual)	ADDRESS = LIGHT TO TURN ON, (OR TURN ALL OFF), KEY TO SENSE; ON = SKIP ONE INSTRUCTION OF PROGRAM. (ONE SENSE ADDRESS = WAIT FOR IO INTERLOCK TO GO OFF)
31	COPY & SKIP	COPY	(rd or rc)	SKIP ONE INSTR. IF NO MORE CARDS, ETC. (END OF FILE). SKIP TWO " IF NO MORE WORDS ON CARD, ETC. (END OF RECORD).

APPENDIX E (see section 4.).

List of IBM Memos

Memo Number	Description
*116	Some Symbols
117	Regeneration
(120	Checking)
125	Clock, etc.
131	Regeneration Control
*132	NOMENCLATURE
(138	ACC includes adder and T/C circuit)
(140	"Add-to-Memory" instruction does not exist)
150	Symbols (especially page 6). (See also 157).
*151	Drawing block diagrams. (See also 152 and 158)
(152	See 151)
155	Tape nomenclature
157	(See 150)
*158	Title boxes; labels. (See also 151)
(162	Neon bulbs)
(163	Labels and diode circuits)
183	Order "+ copy"
(184	Octal-decimal manual table)

* - of basic importance.

( ) - of lesser importance.

Appendix F

Index

Signed Rollin P. Mayer
Rollin P. Mayer

Approved
Norman H. Taylor

RPM/bs

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: DELTA$_{ns}$ IN CERAMIC ARRAY #1

To: N. H. Taylor

From: E. A. Guditz

Date: October 14, 1952

Abstract: It is possible to obtain two values of output voltage from a half-selected memory core depending on whether it holds a ONE or a ZERO. This fact places a limit on the size of a memory plane or, more specifically, the number of cores on one sensing winding which may be half-selected during a read operation.

Consider the memory core hysteresis loop shown in Figure 1. I_m is the magnetizing current required to switch the core. $I_m/2$ is the magnetizing current to which the core is subjected while switching another memory core in its row or column. ϕ_1 and ϕ_0 are the flux states arbitrarily considered to be a disturbed ONE and a disturbed ZERO respectively. If a current of $I_m/2$ is applied to the core while it holds a ONE, a flux change of NS_1 (non-selected ONE) is produced. If, instead, the same current is applied while the core holds a ZERO, a different flux change, NS_0 (non-selected ZERO) is produced. The difference, $NS_1 - NS_0$, has been named δ_{ns}.

Figure 2 shows the sensing winding geometry for Ceramic Array #1. Note that the sensing winding links every core in the memory plane. Note, also, the plus and minus signs associated with each core. These refer to the polarity of output voltage induced in the sensing winding when a core is fully or partially switched by the application of coordinate driving currents in the directions indicated by the arrows at the ends of the driving lines. Since there are equal numbers of positive and negative outputs on each coordinate line almost complete cancellation of the half-selecting signals results. (One of the outputs is from the selected core).

Figure 3a shows two selected coordinate lines of memory cores in a 16 x 16 array. The plus and minus signs indicate the polarity of voltages induced in the sensing winding with the application of $I_m/2$ (Figure 1) in the positive direction in each coordinate driving line. Note that the selected core receives the full switching durrent while the other thirty cores receive but half switching current. However, since the sensing winding links all the cores, the thirty half-selected core outputs add

to or subtract from the selected core output depending on their polarities. If all the half-selected outputs were equal in magnitude then two cases would result:

a. Selected core output positive

b. Selected core output negative

For (a) the net output becomes,

+ selected core output + 14NS - 16NS = + selected core output - 2NS.

For (b) the net output becomes,

- selected core output + 16NS - 14NS = - selected core output - 2NS.

The 2NS terms may be ignored temporarily as not significantly affecting array size. Since it has been shown that half-selecting a core which holds a ONE results in a larger output than half-selecting a core which holds a ZERO, it can be seen that there exists two "worst patterns" and two "best patterns" for a given pair of coordinate lines. Examples of these are shown in Figures 3a, 3b, 4a and 4b.

Suppose that the selected core in Figure 3a contains a ONE. Reading this core results in a negative output signal on the sensing winding. To construct a "worst pattern", the net half-selecting signal from the thirty half-selected cores must be positive in order to subtract from the negative ONE. This means that those cores which will contribute positive half-selecting signals must contain ONES and those cores which will contribute negative half-selecting signals must contain ZEROS. This condition will yield the largest net difference, the sum of all the $\int_{ns}$, which will be called Δ_{ns}.

Suppose again that the selected core in Figure 3b contained a ZERO. Reading this core would result in a negative output signal on the sensing winding. To construct a "worst case", the net half-selecting signal from the thirty half-selected cores must be negative in order to add to the negative ZERO. This means that those cores which contribute negative half-selecting signals must contain ONES and those cores which contribute positive half-selecting signals must contain ZEROS. Thus it is seen that a ONE can be made smaller and a ZERO larger by the contribution of Δ_{ns} to the net sensing winding output.

Conversely, Δ_{ns} can in some instances be of such value as to make the ONES larger and the ZEROS smaller resulting in a "best pattern " or one which gives the largest "ONE-ZERO" ratio. This situation results from patterns shown in Figures 4a and 4b.

For any array, the worst conditions exist for a ONE output signal when the net output is composed as follows:

$$ONE - (n - 2)\ \delta_{ns} - 2NS_1$$

where n = number of cores on a coordinate line.

The worst condition for a ZERO exists when the output consists of:

$$ZERO + (n - 2)\ \delta_{ns} - 2NS_0.$$

Furthermore, since the amplitude of an NS_1 is greatest on a core which holds an undisturbed ONE, and is lower and relatively constant after that, it is possible to get a large δ_{ns}^{1} which can be defined as:

$$\delta_{ns}^{1} \equiv NS_1 \text{ (undisturbed)} - NS_0.$$

For 2- to -1 selection in a memory plane, there may exist two undisturbed ONES ready to contribute to the above effect and the worst conditions may become:

$$ONE - \quad 2\delta_{ns}^{1} \quad - (n - 4)\ \delta \quad -2NS_1$$

$$ZERO + \quad 2\delta_{ns}^{1} \quad + (n - 4)\ \delta \quad -2NS_0$$

The NS signals from fourteen cores in Ceramic Array #1 were recorded photographically during normal operation while they held the "worst pattern". The results yielded an average δ_{ns} of two millivolts.

Measurement of δ_{ns} on seven individual cores by first half-selecting the core while it contained a ZERO and then while it contained a ONE gave an average δ_{ns} of about 2 1/2 millivolts.

Another measurement of delta was obtained by putting a "worst pattern" into the entire array. In this case all cores with outputs of positive polarity held ONES and all cores with outputs of negative polarity held ZEROS. With the pattern inserted, all excitation was removed except a half-selecting current on a winding which linked every core (Z-plane winding). The sensing winding output voltage then consisted solely of δ_{ns} from 128 pairs of cores. This value, therefore, is approximately the same as would be generated by a 128 x 128 array using 2:1 selection. This total Δ_{ns} was 130 millivolts or a δ_{ns} of approximately one millivolt.

These values may be compared to the following signal values:

Normal operation of the 16 x 16 Ceramic Array #1 gives peak-amplitude of ONE-ZERO ratios of 4:1 with ONES of approximately 250 millivolts and ZEROS of approximately 60 millivolts.

An average value for a disturbed NS_1 signal (over 30 cores) is 25 millivolts and for a disturbed NS_0 signal is 23 millivolts.

The "first NS_1 can be as much as ten times greater than a "second" or "third" NS_1 signal.

Documented photographic records of these data on the "delta problem" for Ceramic Array #1 are in Notebook #4 (3/28/52) on pp. 117-120, 125-136 and in Notebook #5 (6/30/52) on pp. 102-108, 123-124, of E. A. Guditz.

Signed Elis A. Guditz
E. A. Guditz

Approved W. N. Papian
W. N. Papian

EAG:jmm

Drawing attached:
A-51628 Figure 2

$NS_1 > NS_0$

$\delta_{ns} \equiv NS_1 - NS_0$

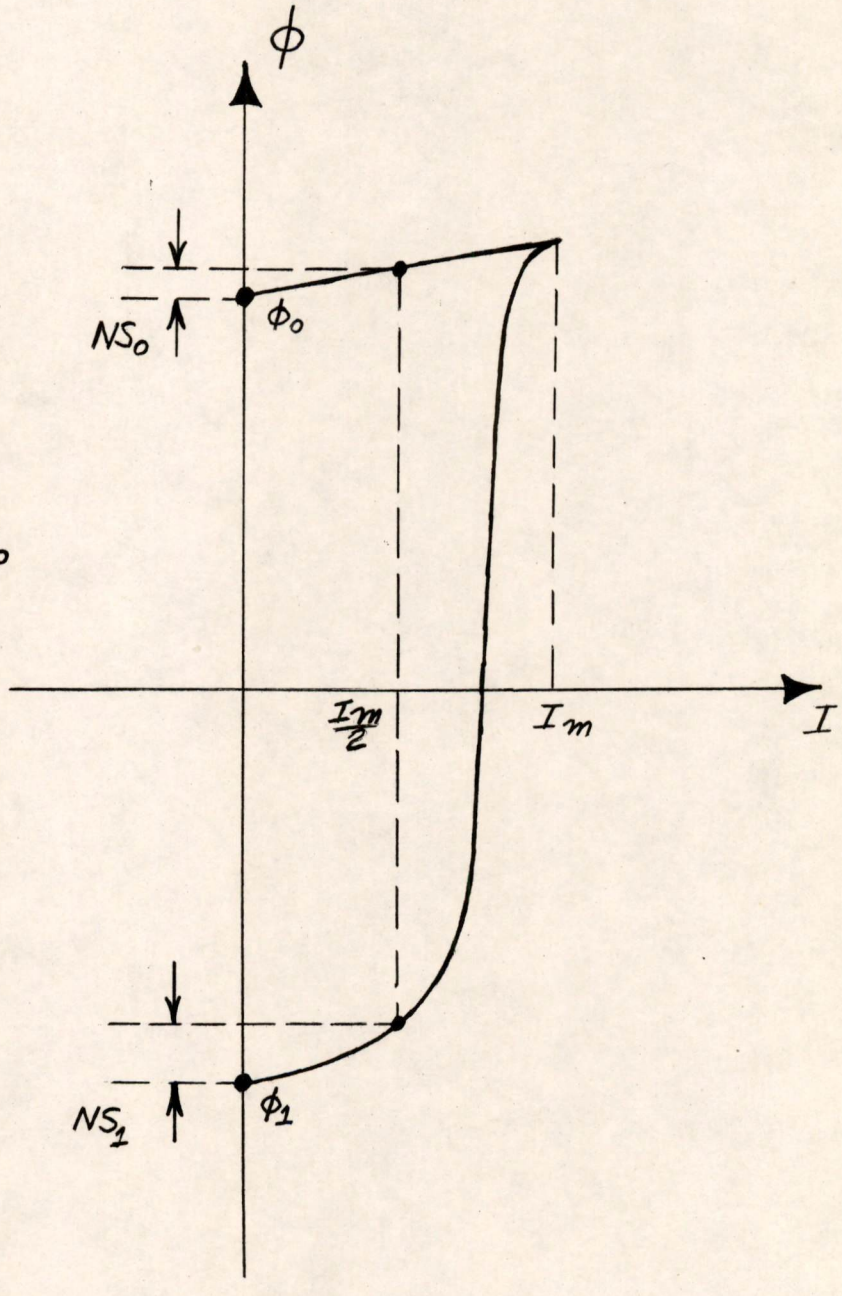
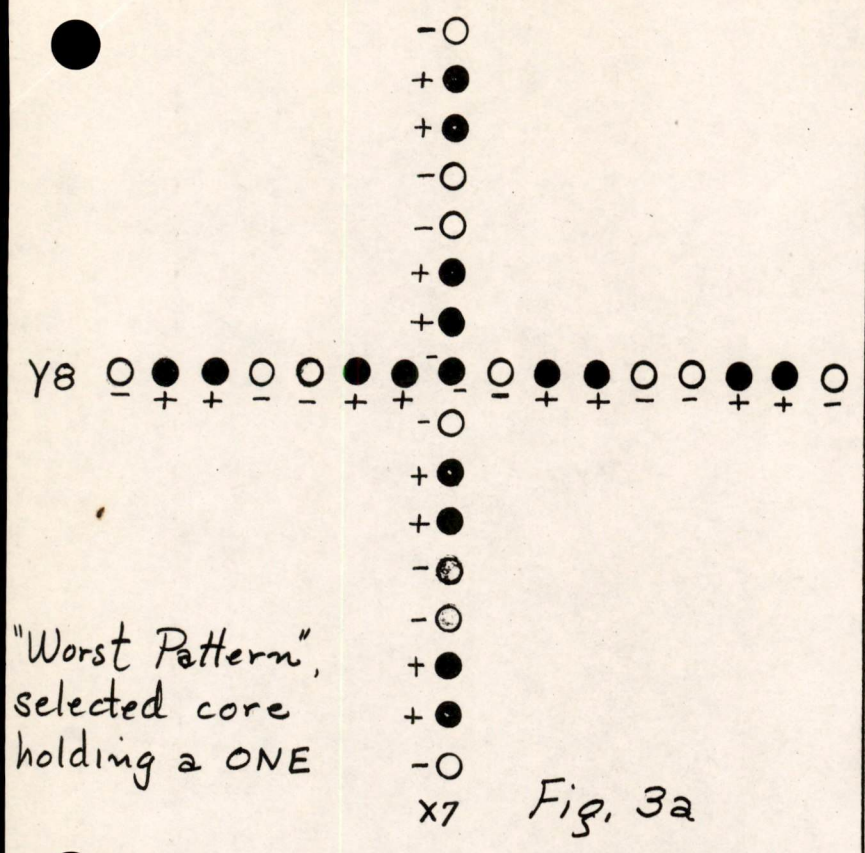


Fig. 1

Key

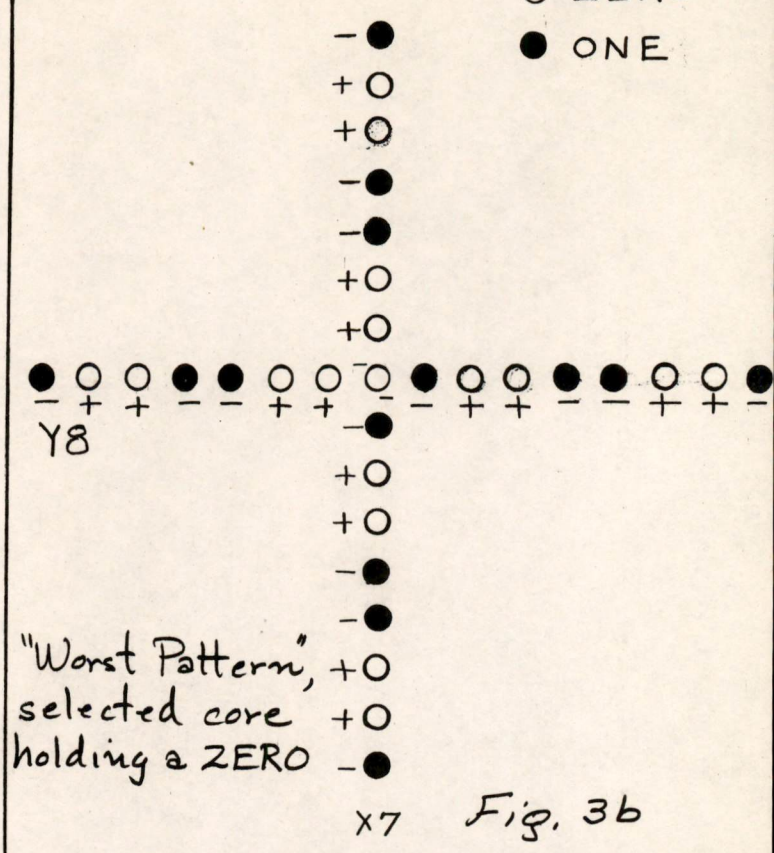
○ ZERO

● ONE



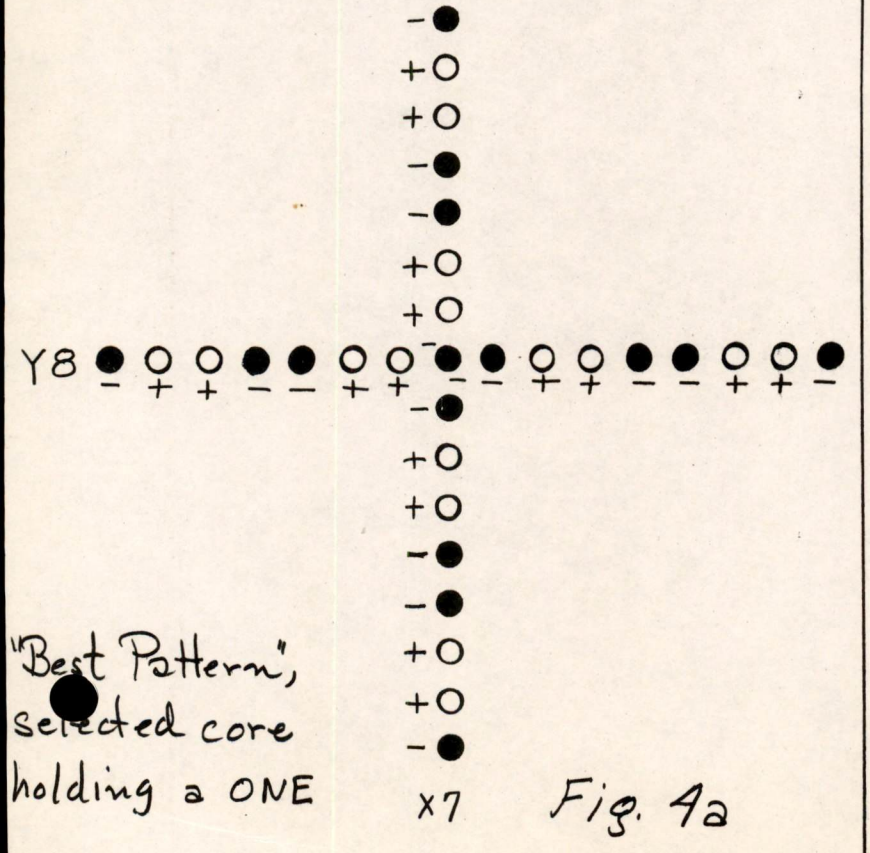
"Worst Pattern", selected core holding a ONE

Fig. 3a



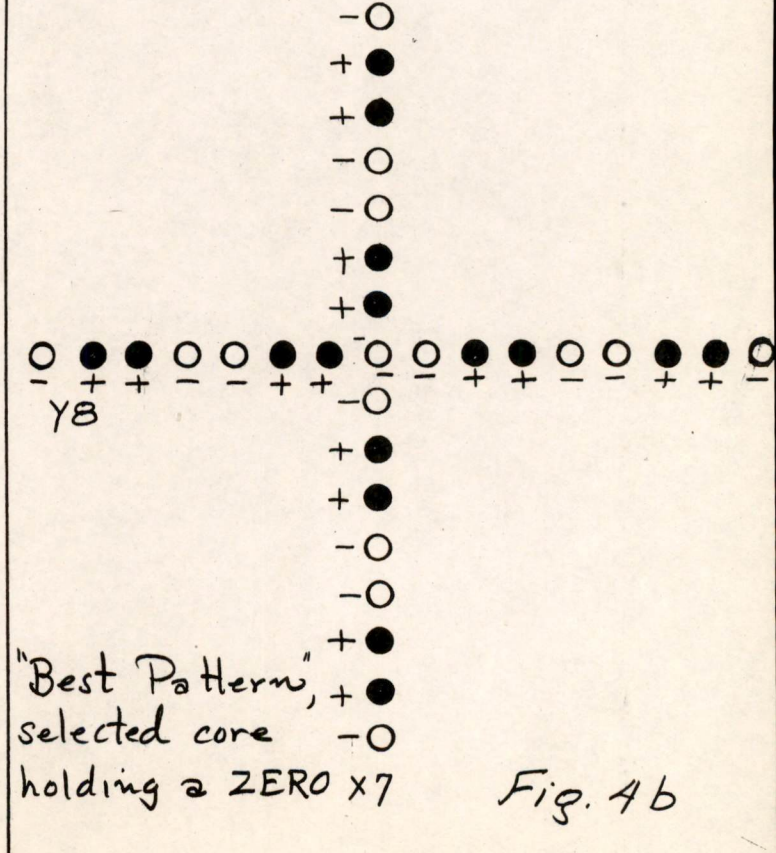
"Worst Pattern", selected core holding a ZERO

Fig. 3b



"Best Pattern", selected core holding a ONE

Fig. 4a



"Best Pattern", selected core holding a ZERO

Fig. 4b

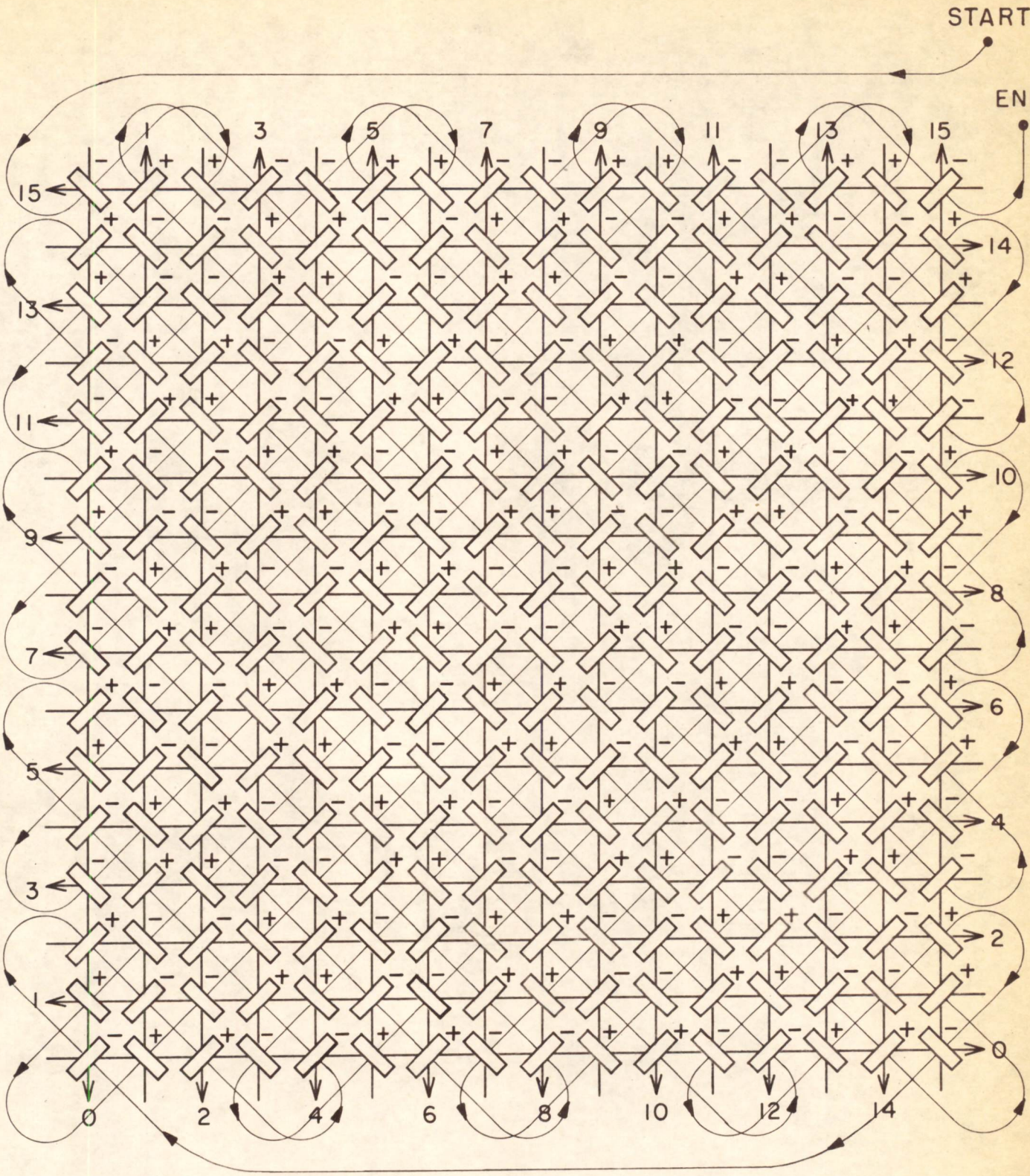


FIG. 2

WINDING GEOMETRY-CERAMIC ARRAY #1

R. Best

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: HYSTERESIS LOOP CHARACTERISTICS OF MF-1118 FOR DIFFERENT TEMPERATURES

To: Group 63 Staff

From: Channing Morrison

Date: October 16, 1952

Abstract: The hysteresis loops were obtained in a temperature range from -196 degrees Centigrade to +305 degrees Centigrade. The Curie point of MF-1118 was reached at approximately 305 degrees Centigrade, and the maximum Squareness Ratio occurred at approximately 30 degrees Centigrade. The flux density and the coercivity were both a maximum at -196 degrees Centigrade and both decreased with increasing temperature.

Type of Cores: The cores used were MF-1118 (F-259, 1-14-52). Four cores were wound together to provide enough output voltage to facilitate taking readings on the hysteresograph. This was made necessary since the wire used was #29 glass-insulated enameled wire and a total of only 18 secondary turns could be wound on the cores.

Type of Magnet Wire: A special type of magnet wire had to be found for this experiment because the insulation on Formex and Teflon wire could not withstand the high temperatures of the experiment (305° C). The wire used was a single glass enameled, #29, with a diameter of .0113 mils.

Temperature Control Material: The heating apparatus consisted of a small stove, a pyrex beaker, some Dow-Corning #550 Silicon Fluid, and some asbestos paper insulation.

The cooling apparatus consisted of ice, dry ice, a combination of dry ice and alcohol, dry ice and acetone, and liquid nitrogen.

Procedure: The apparatus was set up so that the heating equipment could be used for both the saturation loop and the squareness ratio tests.

For the squareness test, the temperature was raised to 255° C, and readings were taken at that temperature. Then the liquid was allowed to cool down and more readings were taken at 20-degree intervals. The lowest temperature taken without coolants was 26° Centigrade.

Then the saturation loop test was started and at room temperature enough ampere turns were impressed on the cores so that a hysteresis loop far into saturation was made. This loop was calibrated so that both the flux and

coercivity could be read off the scope. The gain controls were set at this calibration and pictures were then taken at room temperature. The temperature was then increased in increments of twenty degrees and pictures were taken at these points. This procedure was continued until a temperature of 305° C was reached. This concluded the high-temperature part of the test.

The cooling apparatus was set up and ice was used to cover the interval between 26° and 0° Centigrade. Three points were taken for the maximum squareness curve in this interval. For the next lower temperature range, dry ice with acetone was used and a temperature of -55 degrees Centigrade was reached. Finally liquid nitrogen was used and a temperature of -196° C was reached.

This same cooling material was used for the saturation loops and readings were taken at 0°, -6°, -58° and -196° C. However, for the last two temperatures, the scale for the flux and coercivity had to be changed because the core was no longer into saturation at those temperatures and more ampere turns had to be added.

The data were read off the pictures and tabulated. Then the cores were unwound and the dimensions of the four cores were taken with a Vernier Caliper. From the dimensions of the four cores, an average was computed. Using this average core, the mean path length and cross-sectional area was determined. With these dimensions, the approximate coercivity in oersteds and flux density in gauss was computed and finally all the data were plotted in three curves: Coercivity vs. Temperature, Squareness Ratio vs. Temperature and Flux Density vs. Temperature. These curves are shown in Figures 3, 4, and 5. An arrangement of the pictures of the Saturation Hysteresis Loops are found in Figures 1-1, 1-2, 1-3; and pictures of the Maximum Squareness Loops are in Figures 2-1 and 2-2.

Signed Channing D. Morrison
Channing D. Morrison

Approved DRB
David R. Brown

CDM/jk

Drawings Attached:

Figure 1-1	A-52702
Figure 1-2	A-52714
Figure 1-3	A-52715
Figure 2-1	A-52736
Figure 2-2	A-52737
Figure 3	A-52684
Figure 4	A-52685
Figure 5	A-52686

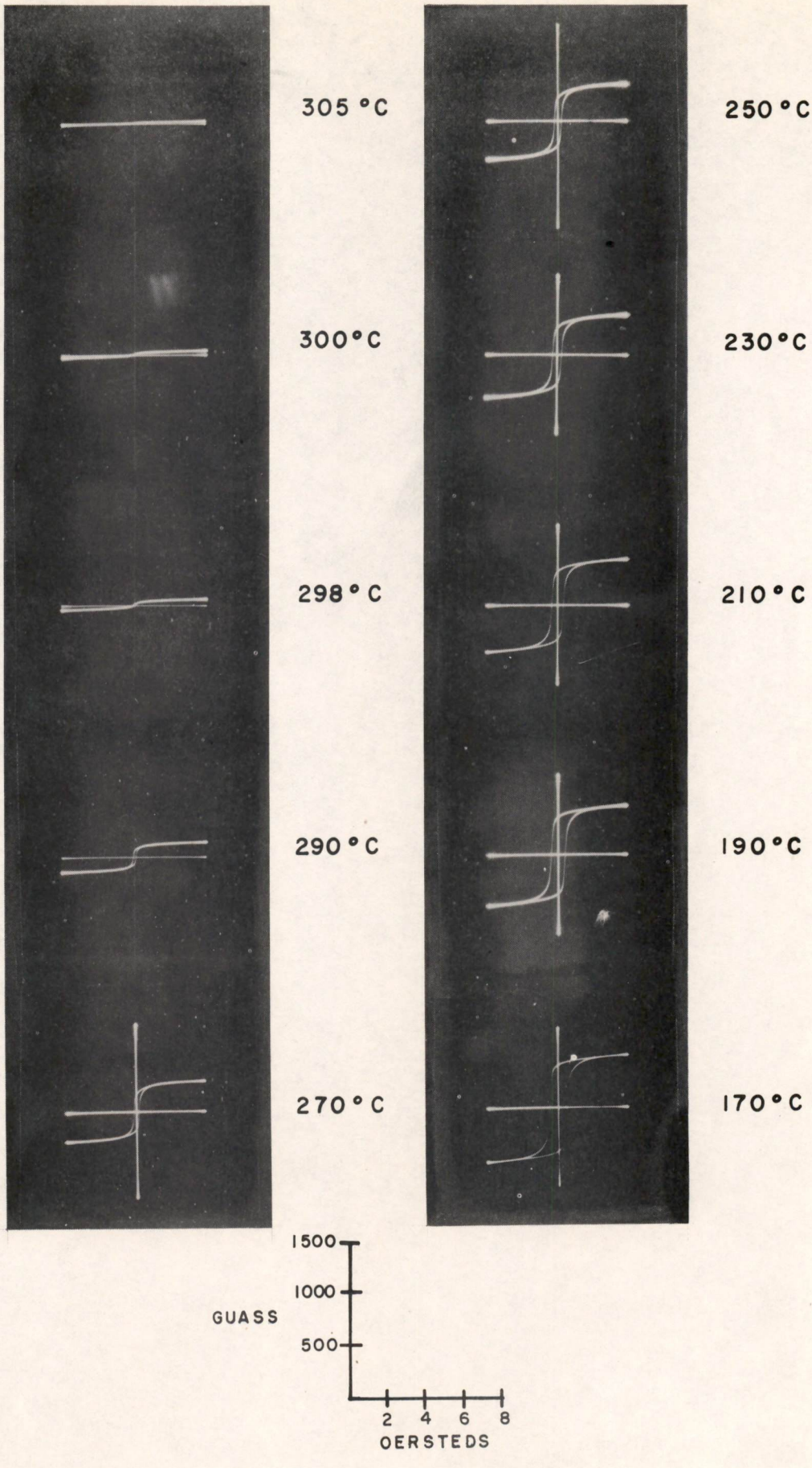


FIG. 1-1

SATURATION HYSTERESIS LOOPS OF MF-1118 [F-259, 1-14-52]
AS A FUNCTION OF TEMPERATURE

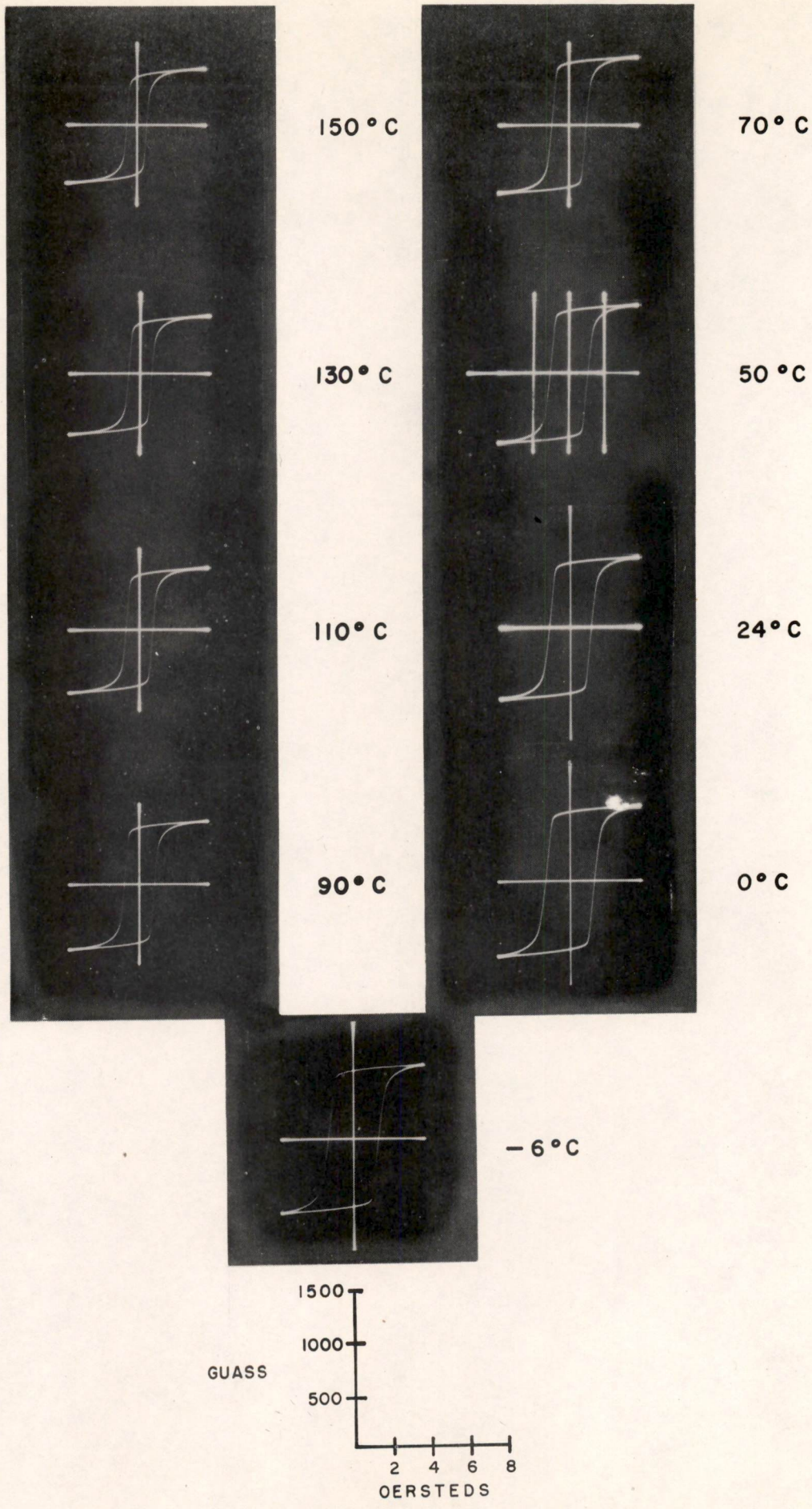
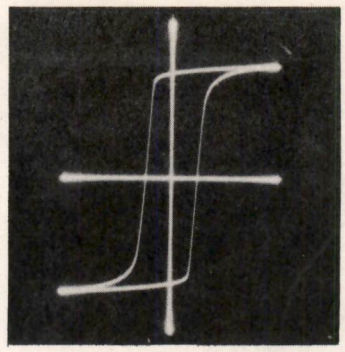
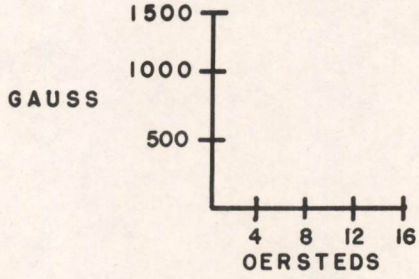


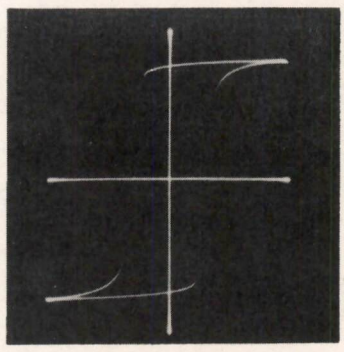
FIG. 1-2

SATURATION HYSTERESIS LOOPS OF MF-1118 [F-259, 1-14-52]
AS A FUNCTION OF TEMPERATURE



−58°C





−196°C

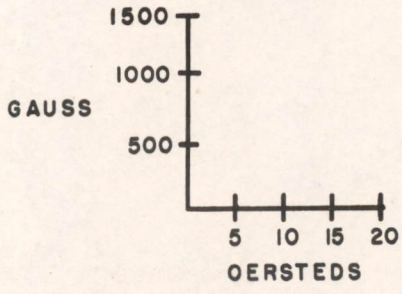
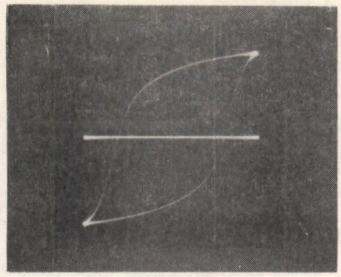
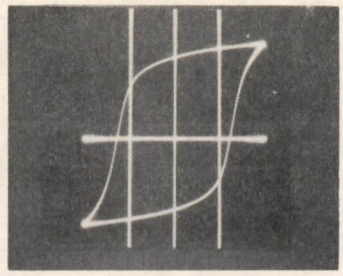


FIG. 1-3

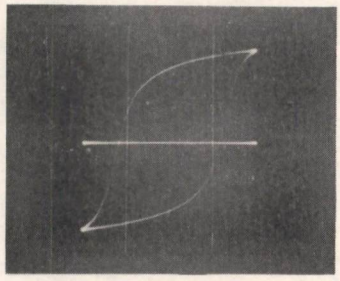
SATURATION HYSTERESIS LOOPS OF MF-1118 [F-259, 1-14-52]
AS A FUNCTION OF TEMPERATURE



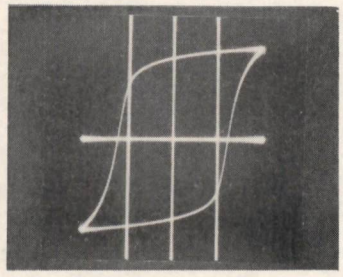
255°C



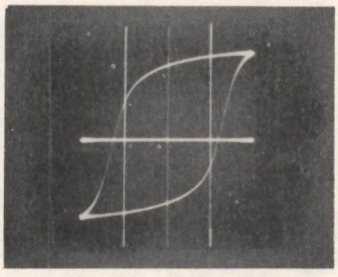
150°C



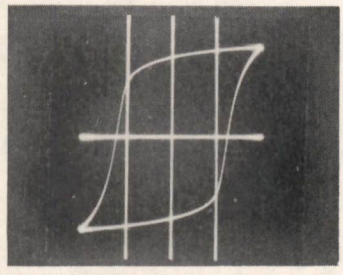
234°C



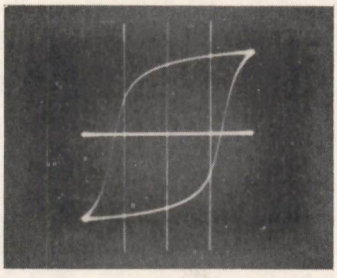
125°C



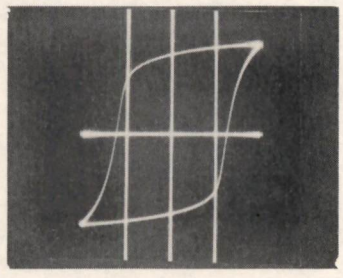
220°C



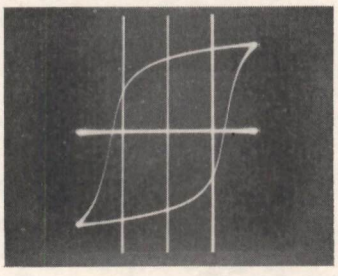
105°C



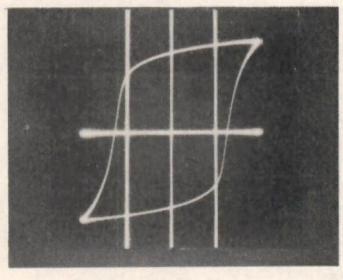
192°C



81°C



172°C

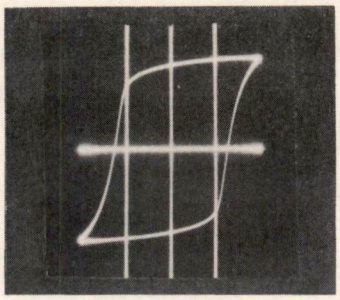


64°C

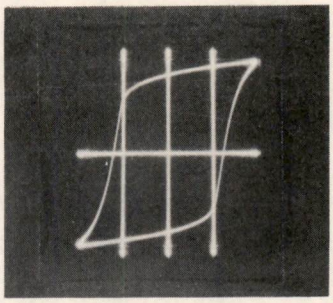
FIG. 2-1

MAXIMUM SQUARENESS RATIO OF MF-1118 [F-259,1-14-52]
AS A FUNCTION OF TEMPERATURE

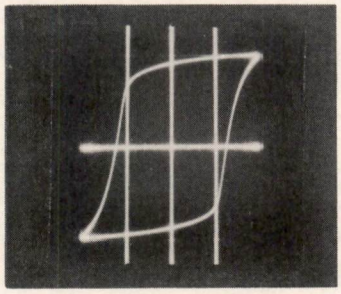
A-52736



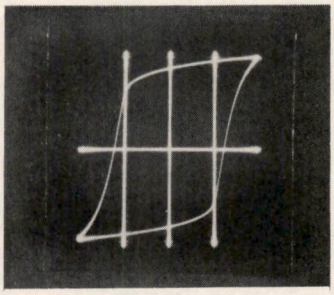
36°C



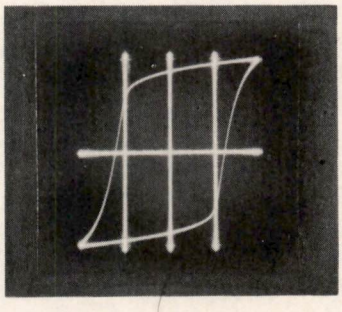
10°C



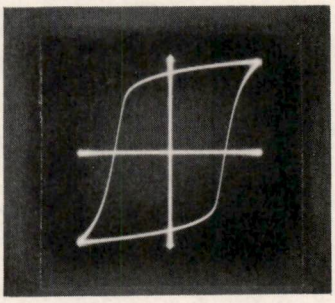
26°C



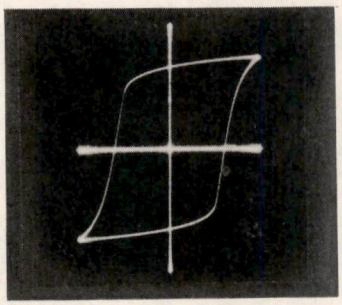
0°C



15°C



-55°C



-196°C

FIG. 2-2

MAXIMUM SQUARENESS RATIO OF MF-1118 [F-259, 1-14-52]
AS A FUNCTION OF TEMPERATURE

A-52684

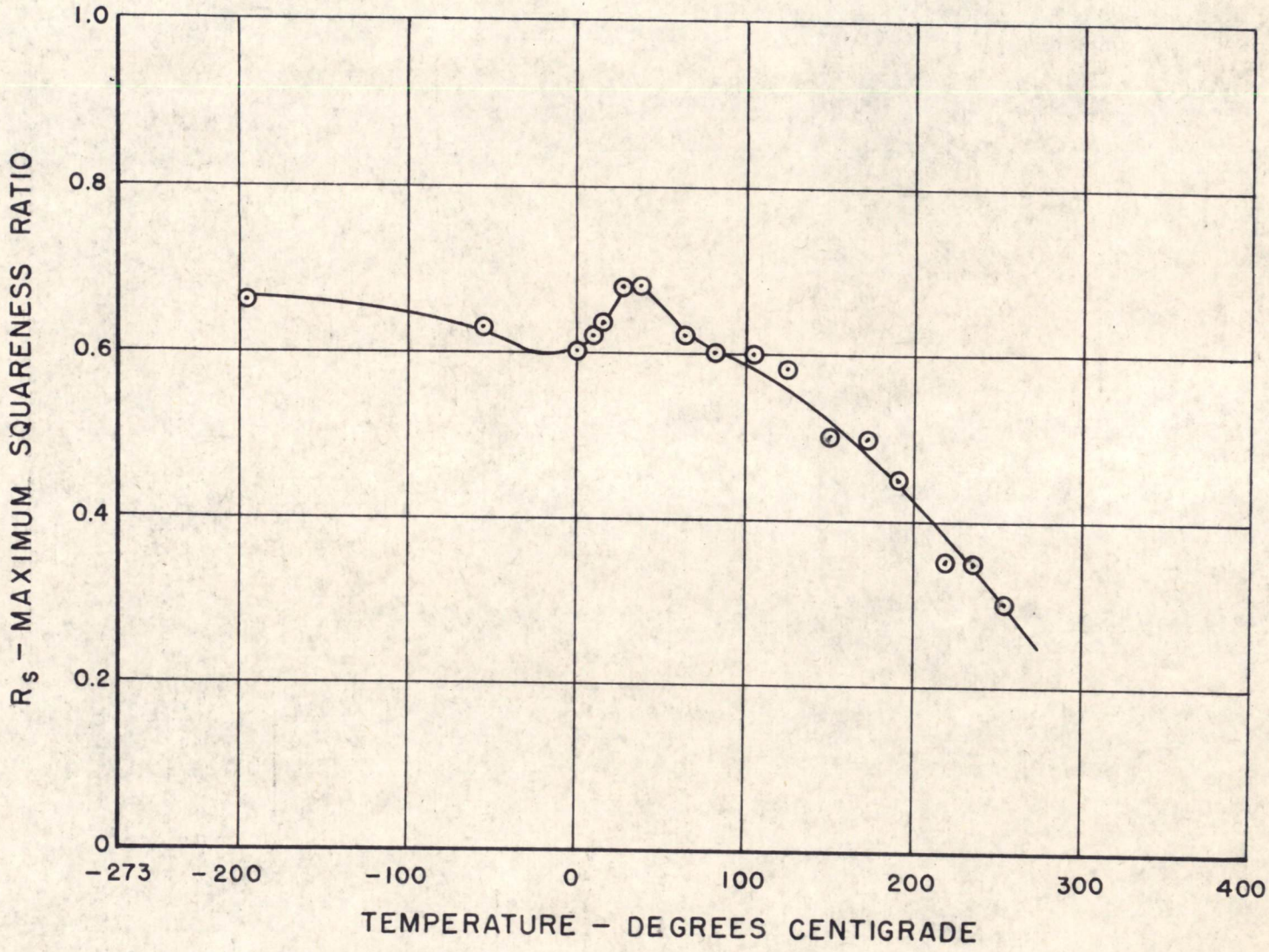


FIG. 3

MAXIMUM SQUARENESS RATIO VS. TEMPERATURE

4 CORES, MF-1118, F-259, 1-14-52

A-52685

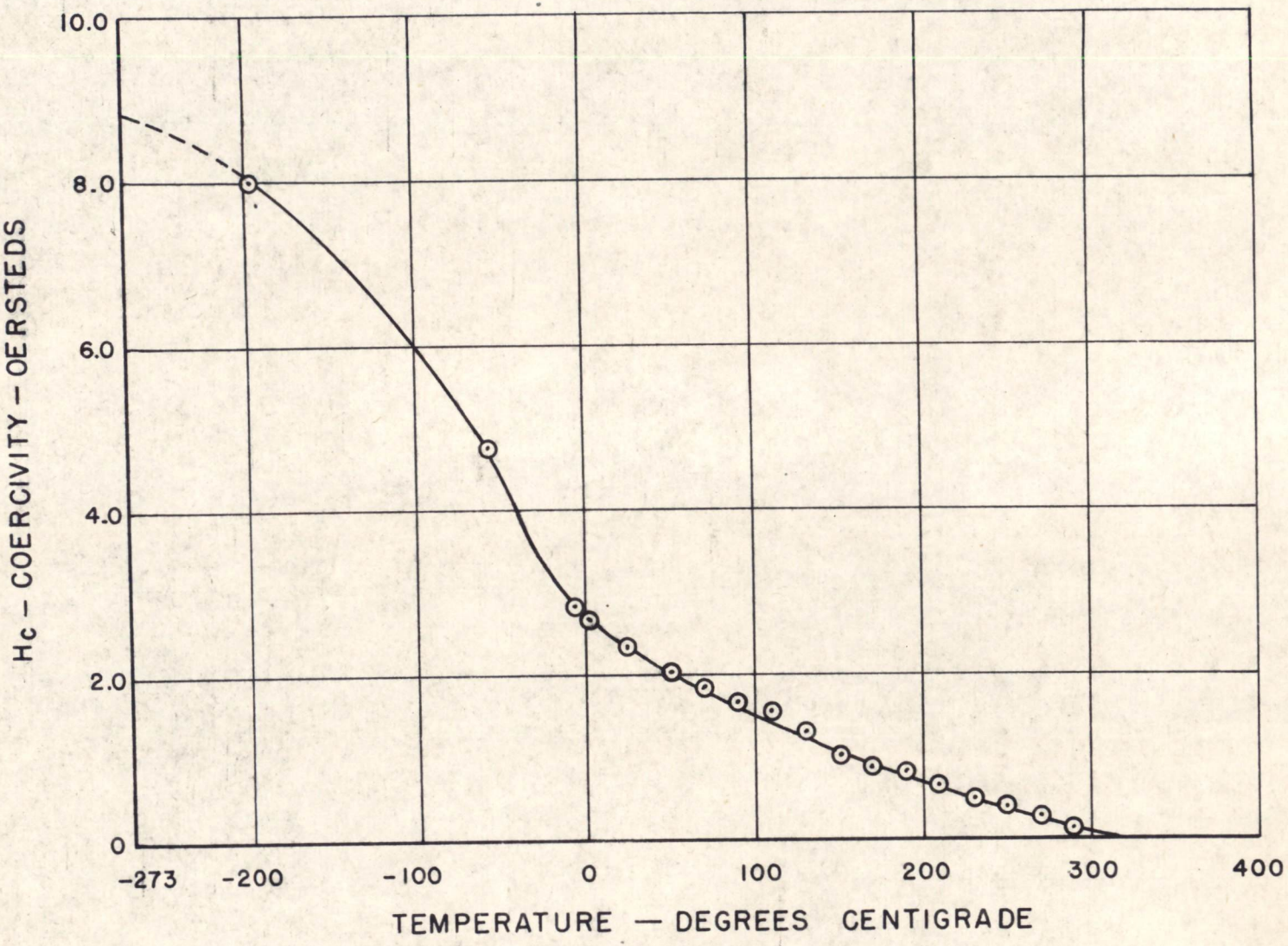


FIG. 4

COERCIVITY VS. TEMPERATURE

4 CORES, MF-1118, F-259, 1-14-52

A-52686

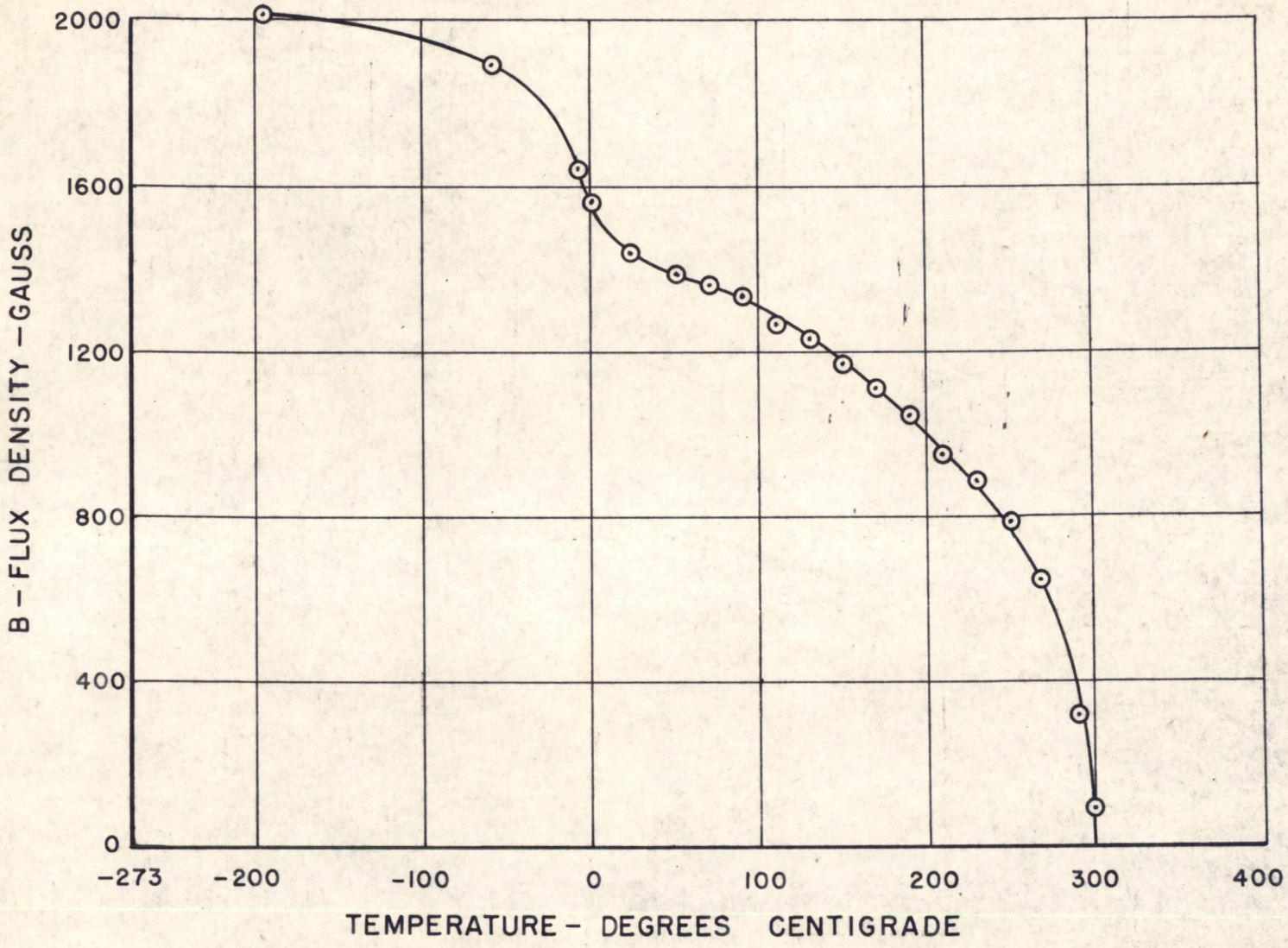


FIG. 5

FLUX DENSITY VS. TEMPERATURE

4 CORES , MF-1118 , F-259, 1-14-52

R. Beat

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: INTRODUCTION TO THE THEORY OF SEMICONDUCTORS IV, QUANTUM STATES IN CRYSTALS. THE BOUND ELECTRON CASE.

To: Transistor Group

From: Donald J. Eckl

Date: October 22, 1952

Abstract: This is the fourth note dealing with the physics of semiconductors. The field-free model for metals was discussed in E-474. This model is useful in providing an approximate explanation of conduction, thermionic emission, contact potential, etc. However, the discussion of the properties of semiconductors requires a knowledge of the situation in crystalline solids when the atomic fields are not neglected. The more accurate and complete treatment thus entailed leads to allowed and forbidden energy bands. It is this treatment of the problem and its results which are the subjects of the present discussion.

4.0 Introduction. The Single Potential Well

The idea of a potential well was mentioned briefly in E-463. It was pointed out that only discrete energy levels were allowed for an electron moving within such a well. For the case of an infinite well shown in Figure 1a, the permitted energy levels are given by the relation,

$$E = \frac{n^2 h^2}{8md^2} \qquad n = 1,2,3\text{---}. \qquad (4.0)$$

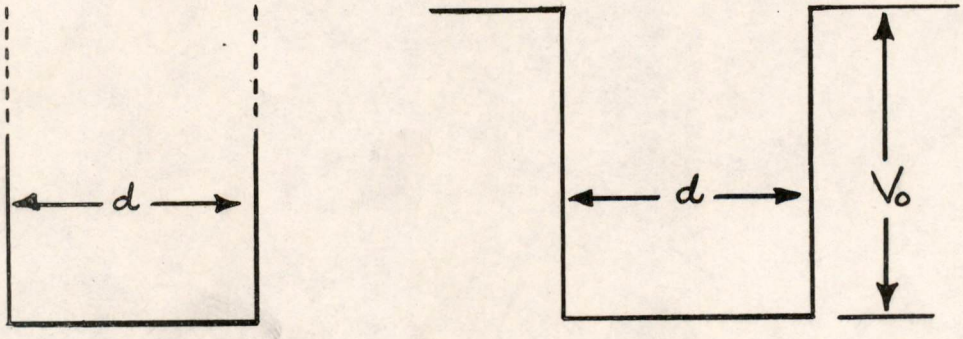


Figure 1

In the case where the well has a finite depth as shown in Figure 1b, the situation is more complicated. The permitted energy levels are now given by the solutions of the transcendental equation,

$$\phi = \tan d\sqrt{\frac{8\pi^2 mE}{h^2}} = \frac{2\sqrt{E(V_o-E)}}{2E-V_o} . \qquad (4.1)$$

These solutions are shown graphically in Figure 2 for particular values of V_o and a.

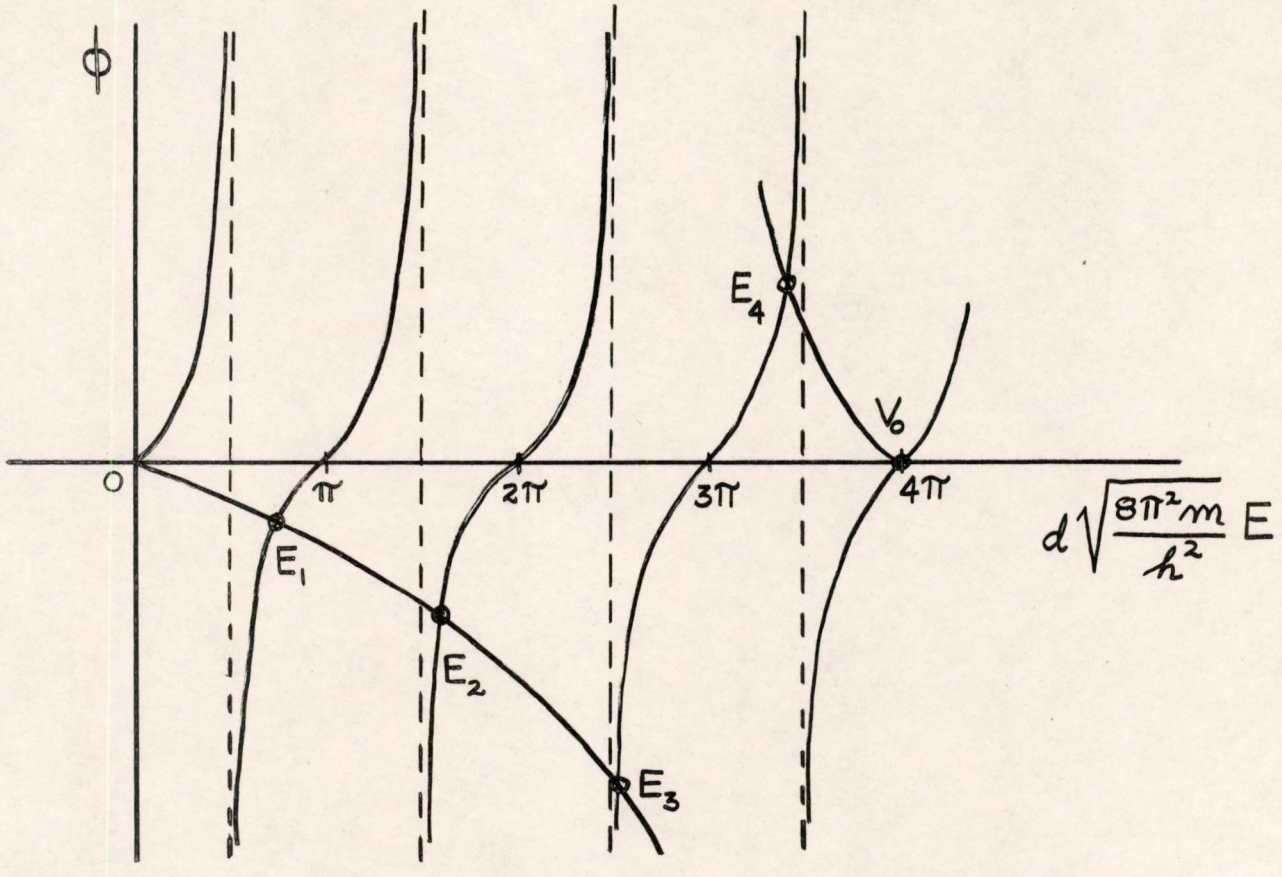


Figure 2

In this particular case, there are four allowed values of energy between zero and V_o and they have the values

$$E_1 = .05V_o; \; E_2 = .20V_o; \; E_3 = .44V_o; E_4 = .74V_o$$

It can also be shown that above V_o all energies are permitted. Therefore the substitution of a finite well for the simple case of the infinite well has modified the energy level scheme as shown in Figure 3.

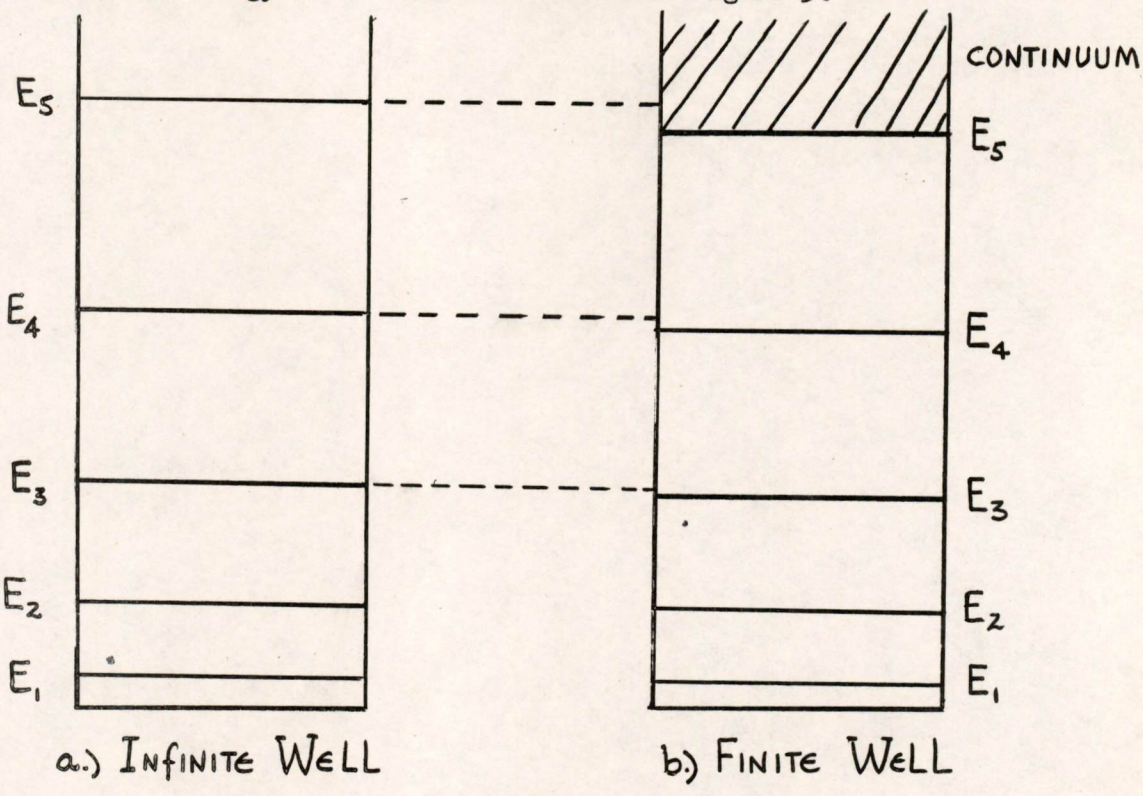


Figure 3

The form of the Schroedinger ψ function for each of these four energy values in the case of the finite well is shown in Figure 4.

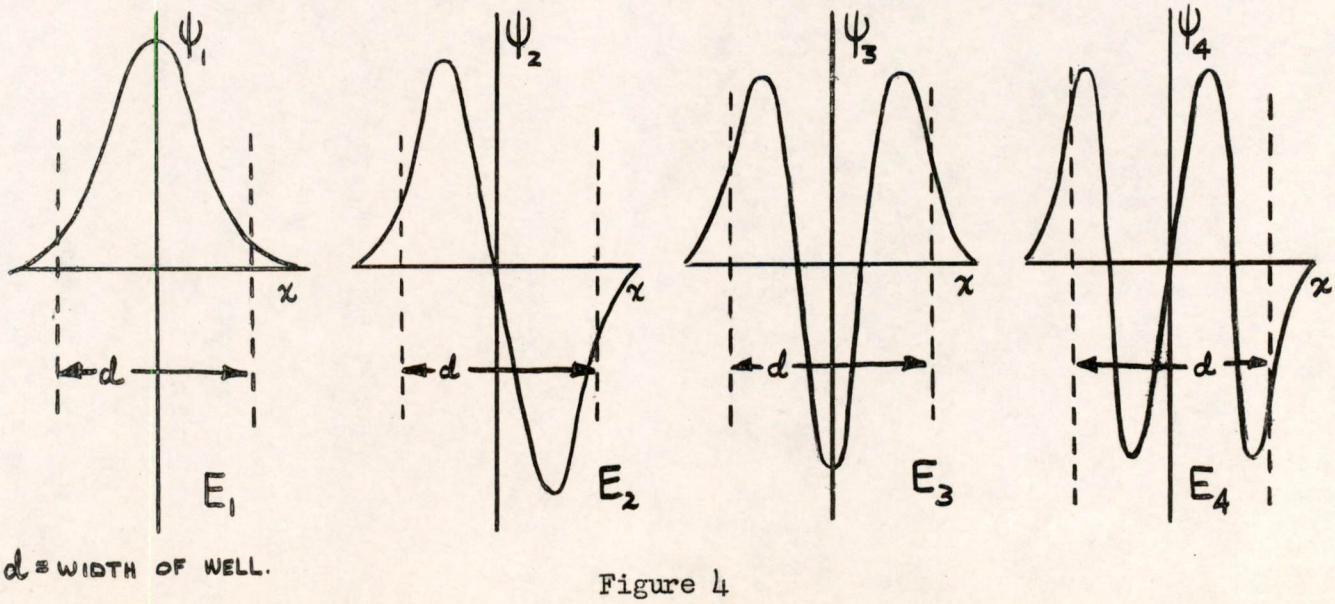


Figure 4

The important point to note is that the more nodes or zeros a ψ function has the higher is the energy to which it belongs. It might be worth restating here that these ψ functions are the solutions of the Schroedinger amplitude equation with a particular potential function. Also the expression $\psi\psi^* d\tau$ gives the probability of finding the electron in a volume element $d\tau$. (See E-463.)

4.1 The Case of the Crystalline Solid. Qualitative Picture where Solid is Built Up One Atom at a Time.

In E-474 the potential function for an electron inside a crystalline solid was discussed. The form of this potential is shown in Figure 5. Each minimum represents the nucleus on an atom. This is simply a series of potential wells. In the previous section the allowed energy

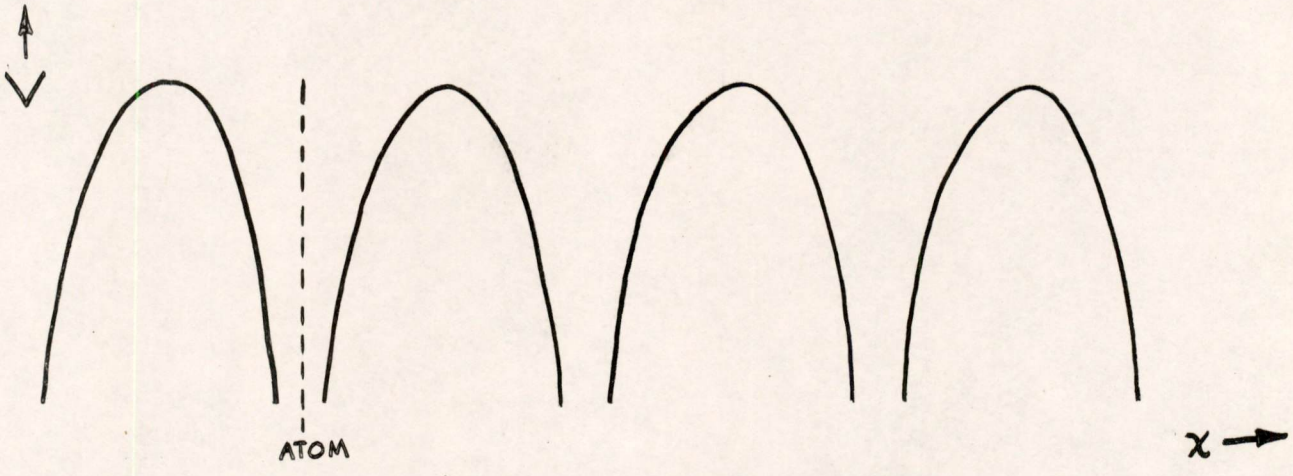


Figure 5

values for a single potential well were discussed. This represents the case of an electron in the potential field of a single isolated atom. Now consider the case where a second atom is brought close enough that the ψ functions for the two wells overlap. This situation is shown in Figure 6a. The resultant ψ functions for the case of the two potential wells are shown in Figures 6b and 6c. Both are solutions of the required Schroedinger equation. Since the antisymmetrical function has more zeros than the symmetrical one, it must be associated with a higher energy. Therefore, the lowest energy E_1 of the single well has now been split into two levels. This is true of each level belonging to the single well. The separation between these levels increases exponentially as the distance between atoms decreases.

Atoms may be added until the total number N is reached. For N atoms or N potential wells every original level is split into N levels, each of which can accommodate two electrons of opposite spin. Thus the energy spectrum now consists of a group of bands of allowed energies. These bands provide a sufficient number of levels to take care of the valence electrons of the N atoms and still allow them to satisfy the Pauli Exclusion Principle.

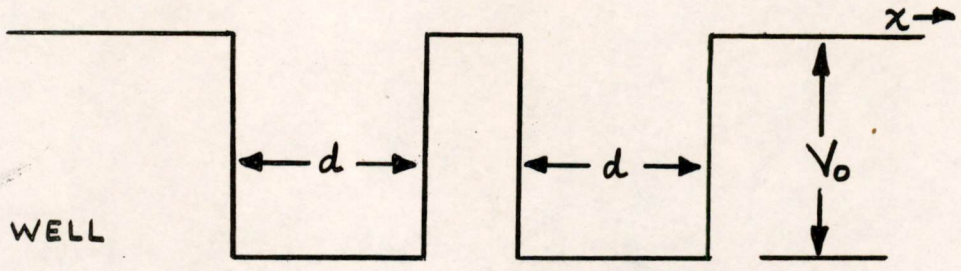


FIG. 6a.
DOUBLE
POTENTIAL WELL

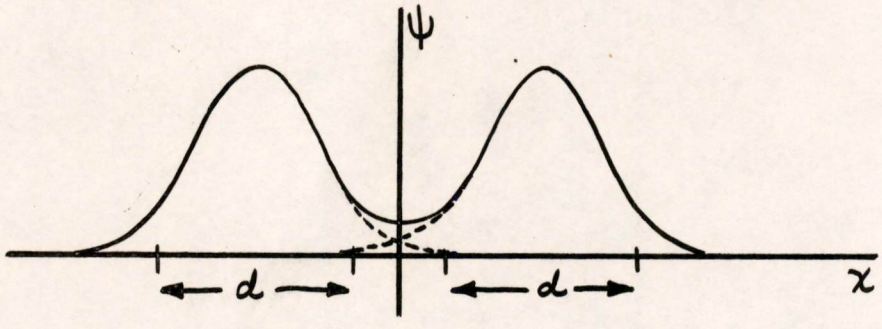


FIG. 6b.
SYMMETRIC ψ

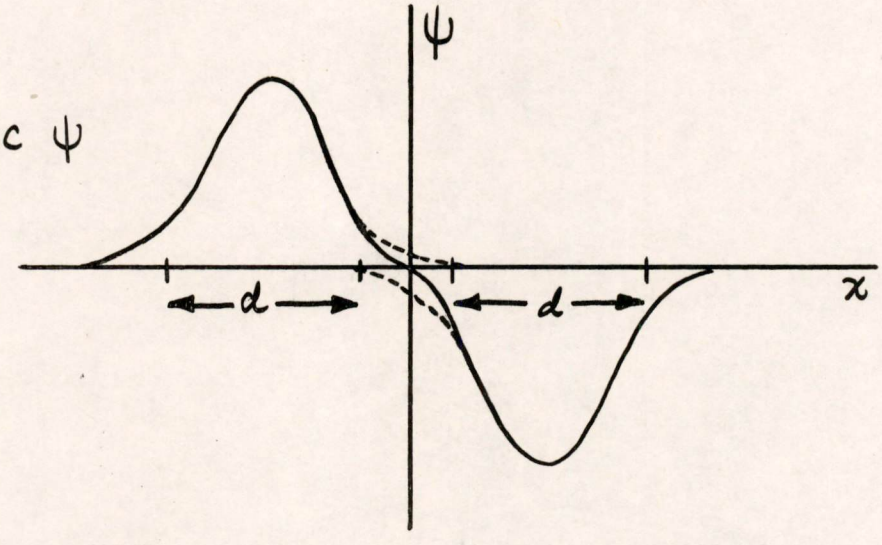


FIG. 6c.
ANTISYMMETRIC ψ

Figure 6

The spreading of the energy levels of an atom as other atoms are brought into close proximity is shown for the case of sodium in Figure 7. At 2 r_o the first four levels which accommodate all the electrons in sodium are at the positions found in the free atom. Even at this large separation, however, the $n = 3, \ell = 1$ level has spread into a band. At r_o, the normal atomic spacing in the metal, both the fourth and fifth levels have become bands. The first three levels are still unaffected,

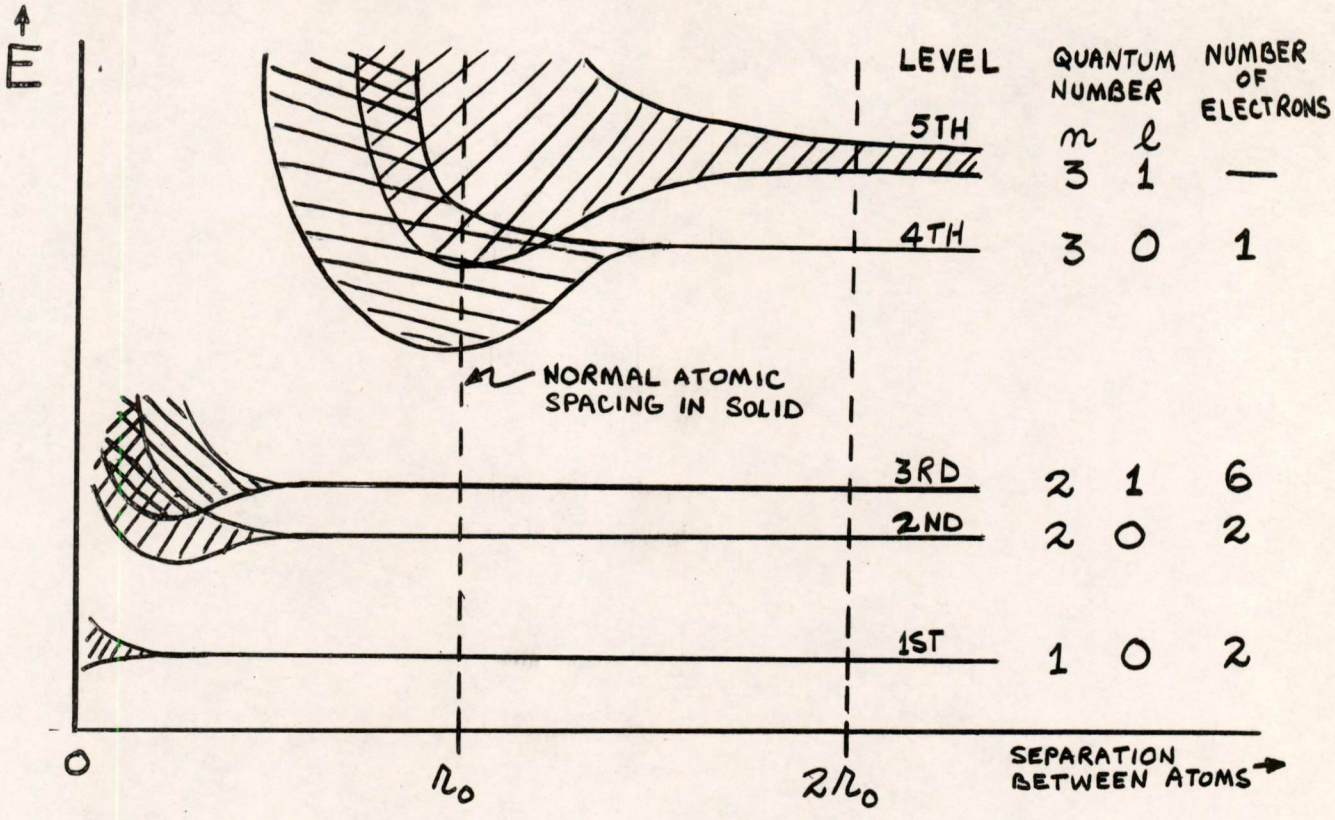


Figure 7

indicating that the electrons in these levels are still bound to a particular nucleus and are unaffected by the close proximity of other atoms. Experimental evidence of the overlapping of the fourth and fifth bands is found in the x-ray transition of the valence electron to replace an ejected lower level electron. Since such a transition from the fourth level is forbidden, the electron must be able to be in the fifth level as well.

The case of magnesium is another point in question. Being the next higher element in the periodic table, magnesium has two valence electrons. These completely fill the fourth level. Therefore, if there were no overlap and resultant possibility of easy transition to the next upper level, magnesium would be an insulator, since the valence electrons would be unable to jump the gap to the next permitted level.

4.2 The Crystalline Solid. Periodic Potential Treatment

The previous section gives a qualitative picture of the situation in a crystalline solid but a more complete and quantitative result requires the solution of the Schroedinger equation with a periodic potential function. Such a function is shown in Figure 8. It is an approximate repre-

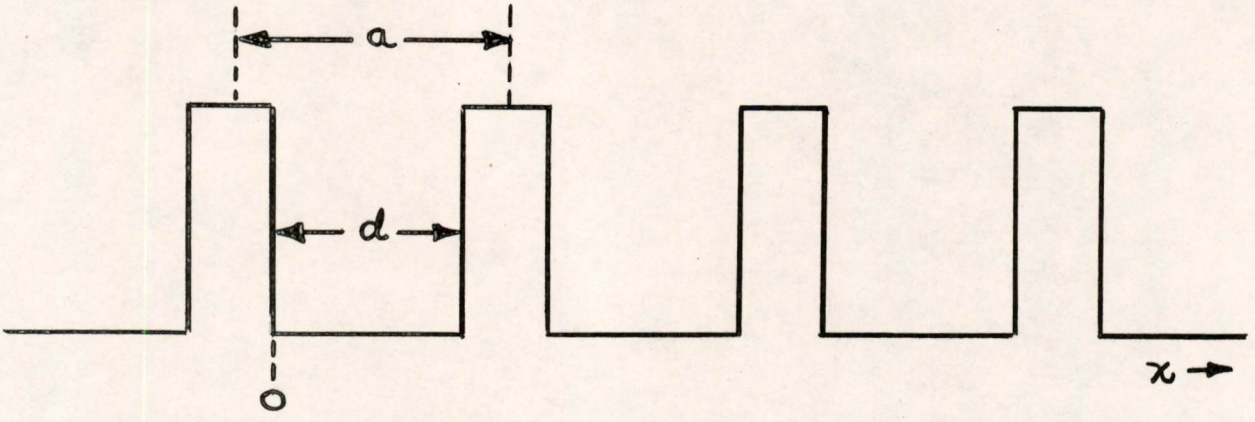


Figure 8

sentation of the potential structure inside a solid already shown in Figure 5. Assume first of all the case of an infinite lattice. The solutions of the Schroedinger equation in this case, known as Bloch Wave Functions, have the form:

$$\Psi(x,t) = v(x)e^{(ikx-ict)} \qquad (4.2)$$

where, $v(x + a) = v(x)$ i.e., v is periodic of period a.

and $c = \nu\lambda$, the velocity.

The amplitude function is

$$\psi(x) = v(x)e^{ikx} \qquad (4.3)$$

The solution (4.2) is a travelling wave and as such the value of k is given by

$$k = 2\pi/\lambda \qquad (4.4)$$

where λ is the wave length of the ψ function. At this point it is possible to draw an analogy between the Bloch waves in a periodic potential lattice and the current and voltage waves on a periodic lumped-constant transmission line. Mathematically the methods of solution are the same, although, of course, the wave function in each case is different. k is the propagation

constant, and if it is real, the ψ waves are very rapidly attenuated in the lattice. Since the probability of finding an electron in a given volume is associated with the value of ψ in that volume, a zero ψ means no electrons. Thus, the energies for which ψ is attenuated are those not permitted to electrons in the crystal. We will not pursue this analogy any further.

In the solution of the Schroedinger equation it can be shown that the condition for well-behaved ψ-functions is that,

$$\cos ka = \cosh (a-d)\sqrt{B\,(V_o-E)}\cos d\sqrt{BE} + \frac{V_o-2E}{2\sqrt{E\,(V_o-E)}} \sinh (a-d)\sqrt{B\,(V_o-E)}\sin d\sqrt{BE}. \qquad (4.5)$$

where $B = 8\pi^2 m/h^2$.

The right-hand side of this expression is plotted as a function of E in Figure 9.

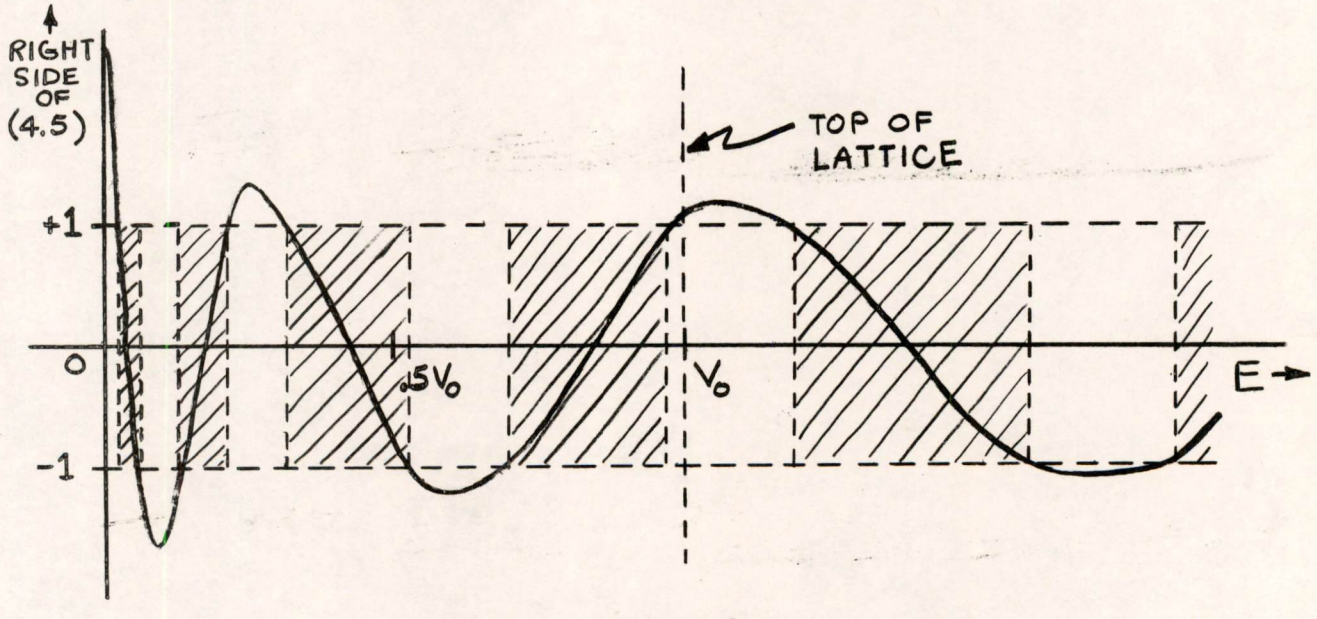


Figure 9

This function can be equal to cos ka only in the interval -1 to +1. Outside of this region there can be no ψ waves. Thus, the values of E where the curve has an absolute magnitude greater than unity are forbidden energy values. Therefore, as before, we find that the bound

electron has allowed and forbidden energy bands. These values can be obtained from a plot like that in Figure 9. A comparison of allowed energies for the single well and the infinite periodic lattice is given in Figure 10.

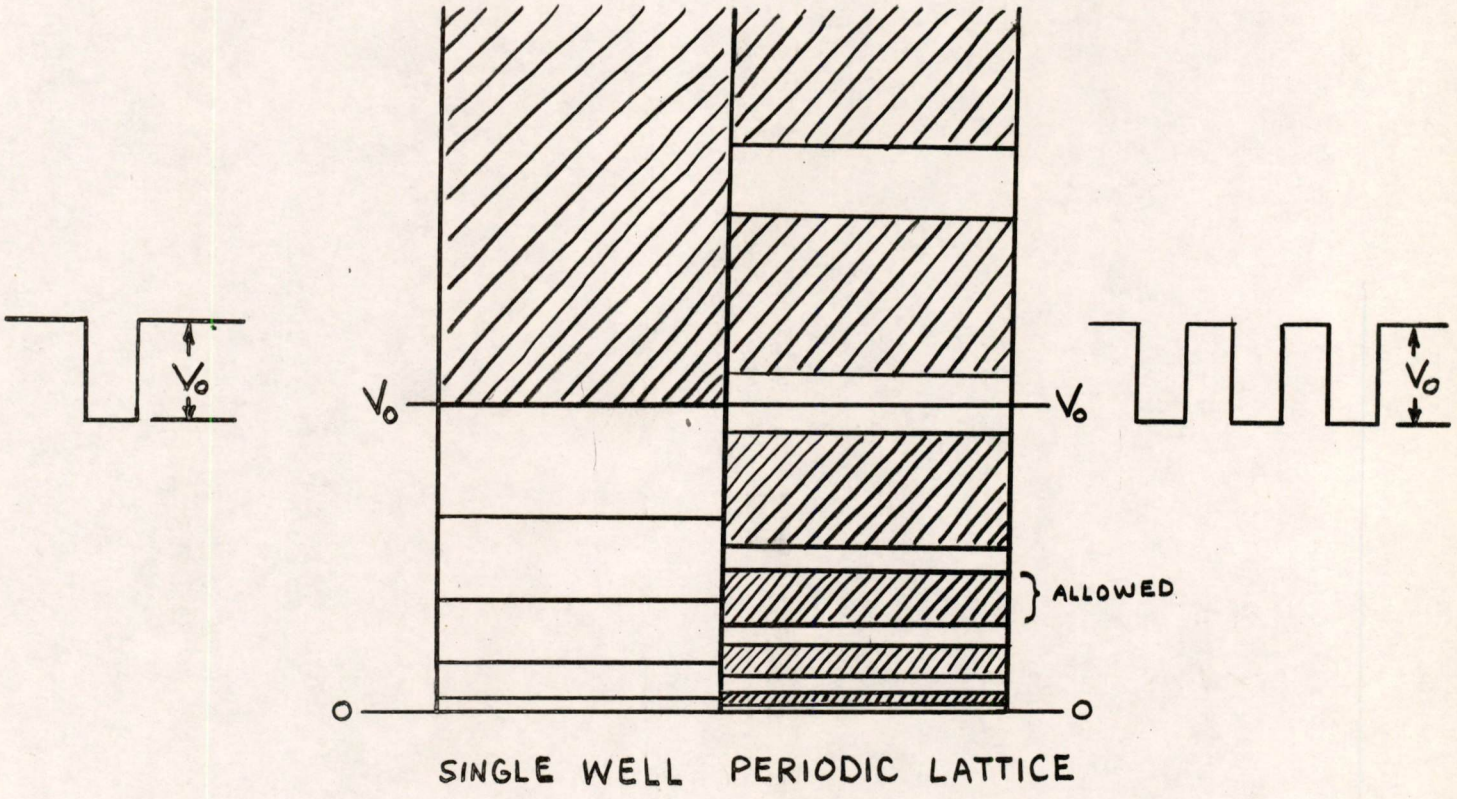


Figure 10

If actual calculations of the allowed energy values are made it is found that these energies are periodic functions of k. A plot of the allowed energy functions against k is given in Figure 11. At this point, we are still dealing with the infinite lattice and all values of E in a given band are allowed. It is interesting to note that the case of the free particle where $V_o = 0$ is given by

$$E = \frac{h^2}{8\pi^2 m} k^2 = \frac{1}{B} k^2. \qquad (4.6)$$

This parabola is shown in Figure 11. It lies close to one of the branches of E vs. k in each energy band.

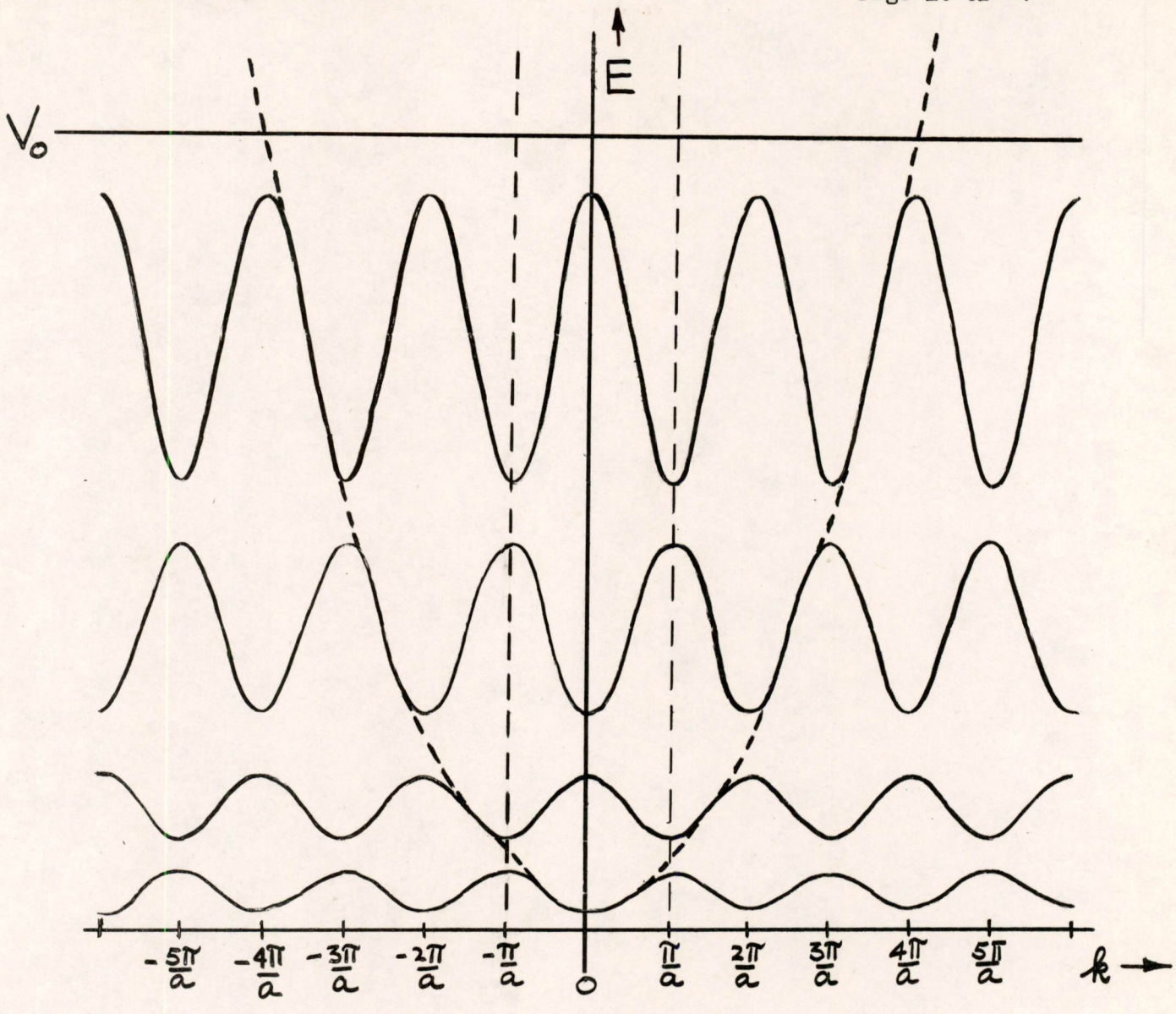


Figure 11

The period of the energy function (and also of the Ψ-function) is $2\pi/a$. It is convenient to divide the k axis into unit cells of this length. This unit cell is referred to as a Brillouin Zone and it suffices to give a complete picture of energy and Ψ as a function of k.

So far we have been concerned with an infinite lattice. Now consider the case of a crystal of N_x unit cells of length "a" such that the length of the crystal,

$$A_x = N_x a. \qquad (4.7)$$

N_x is the number of atoms in the x-direction. In dealing with a crystal of finite length, we now have the problem of determining appropriate boundary conditions. The problem may be simplified by assuming periodic boundary conditions for ψ, i.e. - by assuming that

$$\psi(x) = \psi(x + A_x). \qquad (4.8)$$

This type of boundary condition is artificial (i.e. - it means that the crystal is bent around into a circle so that the left and right sides become identical) but it gives the same results as the correct boundary conditions. From Equation (4.8) above we get

$$v(x)e^{ikx} = v(x + N_x a)e^{ik(x + A_x)}$$

Since $v(x)$ is periodic in "a" this means that

$$e^{ikx} = e^{ik(x + A_x)}$$

or

$$e^{ikA_x} = 1$$

$$\therefore \quad ikA_x = 2\pi i n_x \quad \text{where } n_x = 0,1,2, \text{---}$$

Therefore the condition on k is

$$k = \frac{2\pi n_x}{A_x}. \quad n_x = 0,1,2,3, \text{----} \qquad (4.9)$$

i.e. - k is quantized and has only certain allowed values. This means that E is also quantized as shown in Figure 12 which is drawn for $N_x = 8$ atoms.

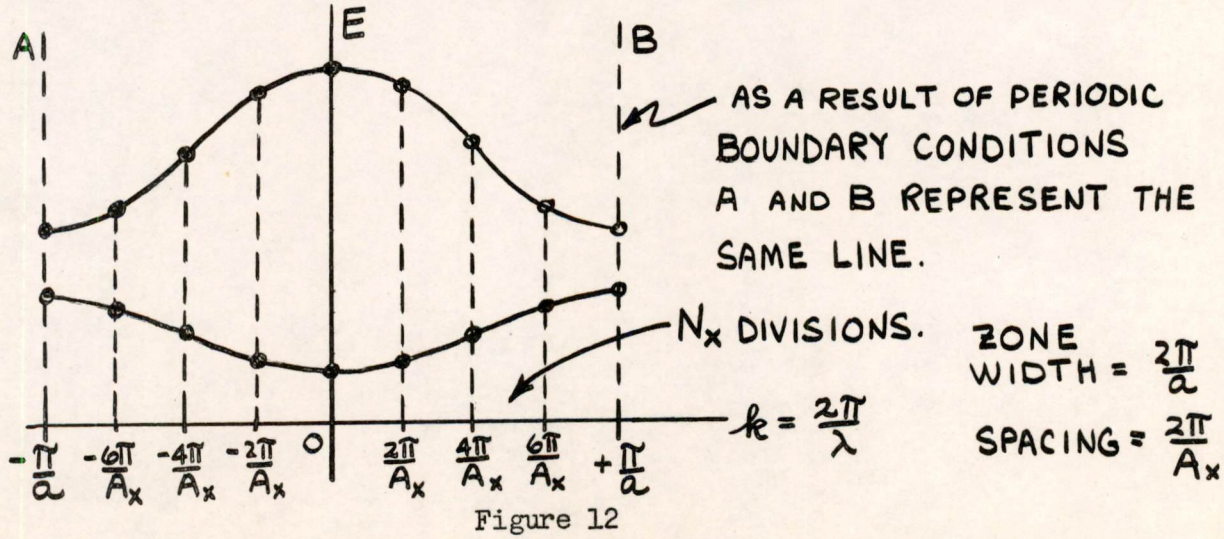


Figure 12

There are N_x allowed values of k in the Brillouin Zone for the case where there are N_x atoms in the crystal. This means that each energy band will have N_x allowed states, each of which can contain two electrons of opposite spin, or $2N_x$ electrons in all.

Note that the width of the Brillouin Zone, is inversely proportional to the lattice constant, a, of the crystal. Also the spacing in the Brillouin Zone is inversely proportional to the width, A_x, of the crystal.

At this point it should be pointed out that Shockley defines a quantity called the CRYSTAL MOMENTUM, P, as

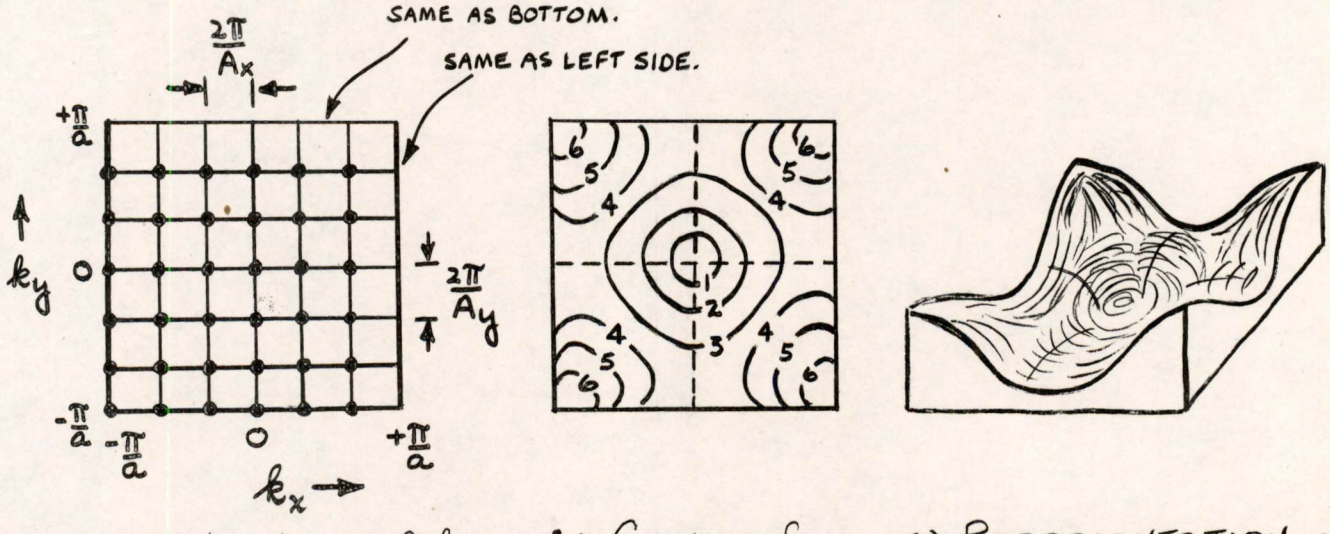
$$P = h/\lambda \qquad (4.10)$$

where λ is the wave length of the Ψ function representing the electron in the crystal. This quantity is related to the propagation constant k we have been using by the expression

$$P = \left(\frac{h}{2\pi}\right) k \qquad (4.11)$$

Therefore with the proper scale factor, all the figures showing the energies in the Brillouin Zone could be redrawn using a P-space.

The previous discussion has been for a one-dimensional crystal. The argument is similar but slightly more complicated for three-dimensional crystals. To use the type of diagram shown in Figure 12 would now require four-dimensional space with k_x, k_y, k_z, and E axes. The picture can be presented as shown in Figure 13 by looking only at the $k_z = P_z = 0$ plane.



a.) ALLOWED VALUES OF k IN k_z=0 PLANE OF BRILLOUIN ZONE.

b.) CURVES OF E = CONST. IN k_z = 0 PLANE.

c.) REPRESENTATION OF ENERGY SURFACE IN BRILLOUIN ZONE.

Figure 13

The allowed states in the Brillouin Zone are shown in Figure 13a. An energy surface is shown superimposed in contour form on this zone in Figure 13b, and a sketch of the surface is given in Figure 13c. This is a simple case similar to the lower curve in the two-dimensional Figure 12. The number of allowed points in a Brillouin Zone is equal to the number of unit cells in a crystal. In most cases, these cells will contain two atoms. Therefore, there will be more than two electrons available per point, necessitating the reuse of the same points in the zone for each energy level.

The discussion above assumed a simple cubic lattice and produced a cubic Brillouin Zone. In general, the picture is not so simple, and the geometrical structure of these zones may become much more complicated. It should also be noted that, while in the one-dimensional crystal the energy levels had definite gaps, it would be quite possible for an energy surface above that shown in Figure 13c to extend down into the central valley in such a way that, although there was no intersection, still every value of energy was available for some value of the propagation constant k.

The advantage of this Brillouin Zone treatment is that it allows a comparatively simple method of representing the allowed electronic energy states and showing the effects of external forces on the electrons.

4.3 Distribution of Energy Levels.

For the case of the one-dimensional crystal, there is one permitted k value for every interval of $2\pi/A_x$ along the axis. In the three-dimensional case, this means one allowed value of k for each volume of

$$\frac{(2\pi)^3}{A_x A_y A_z} = \left(\frac{2\pi}{V}\right)^3 \qquad (4.12)$$

where V is the volume of the crystal. The problem is to determine the number of allowed states in a system of maximum energy E, corresponding to a maximum propagation constant value of k. Therefore, the problem becomes that of finding how many k-points can fit into a spherical volume of radius k. The number of such points is

$$\frac{\text{volume of k space}}{\text{volume containing single point}} = \frac{4/3\pi k^3}{8\pi^3/V^3} \qquad (4.13)$$

There are two electrons of opposite spin in each state so that the number of electrons which can be accommodated in these states is

$$N(E) = 2 \times \frac{k^3 V}{6\pi^2} = \frac{k^3 V}{3\pi^2}. \qquad (4.14)$$

To carry this calculation further, it is necessary to know the relation between E and k. Consider the simple free-electron case where the relationship is

$$E = \frac{h^2}{8\pi^2 m} k^2. \qquad (4.15)$$

This gives the number of electrons with levels below E in a crystal of volume V as

$$N(E) = \frac{8\pi}{3} \frac{(2mE)^{3/2}}{h^3} V. \qquad (4.16)$$

The number in the energy range between E and E +dE per unit volume is then,

$$\frac{dN}{dE} dE = 4\pi \frac{(2m)^{3/2}}{h^3} \sqrt{E}\, dE. \qquad (4.17)$$

The energy level distribution for free electrons is given in Figure 14.

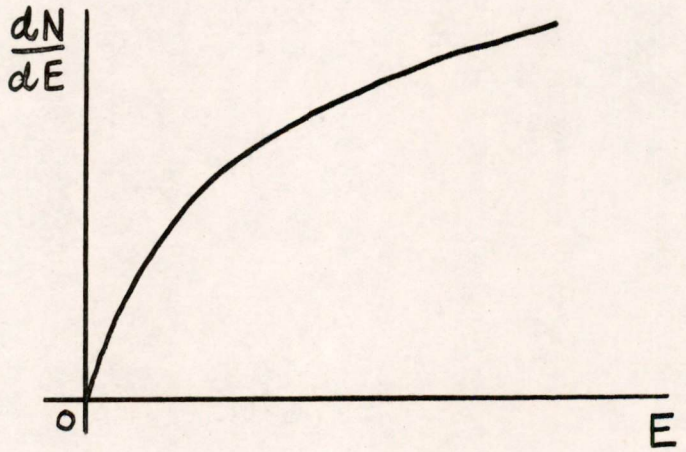


Figure 14

This result (4.17) has already appeared in conjunction with the Fermi-Dirac distribution function in two previous notes*. Also the expression for the zero-point energy given previously** is derived from (4.16).

For the bound electron case where there are allowed and forbidden energy bands (4.17) becomes

$$\frac{dN}{dE}\,dE = 4\pi \frac{(2m)^{3/2}}{h^3}\sqrt{E-E_o}\,dE \qquad (4.18)$$

where E_o is the energy at the bottom of the allowed band. This expression is true only near the bottom of the allowed band. Near the top of such a band a similar result is also obtained and the expression for the distribution of energy levels becomes

$$\frac{dN}{dE}\,dE = 4\pi \frac{(2m)^{3/2}}{h^3}\sqrt{E_1-E}\,dE \qquad (4.19)$$

where E_1 is the energy at the top of the band. The distribution curve in such a band is that shown in Figure 15.

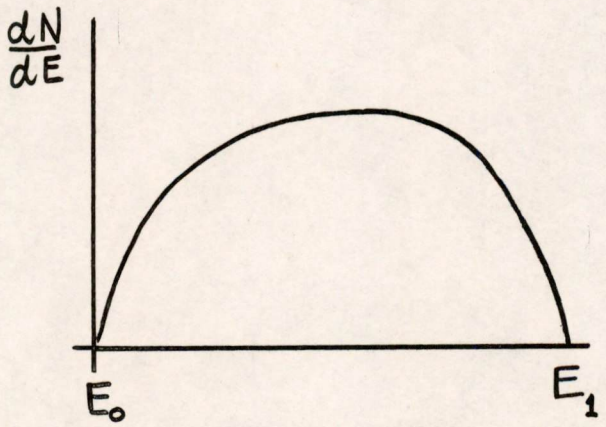


Figure 15

* Equations (2.17) in E-468 and (3.2) in E-474.

** Equation (3.0) in E-474

With this brief introduction to the notion of energy bands, we are now in a position to discuss the properties of semiconductors.

Signed Donald J. Eckl
Donald J. Eckl

Approved John F Jacobs
John F. Jacobs

Approved
Norman H. Taylor

DJE/cs

Distribution 1.

References

1. "The Quantum Theory of Matter", Chapter 10, J. C. Slater (McGraw-Hill 1951)

2. "Electrons and Holes in Semiconductors", Chapters 5, 9.1, W. Shockley (Van Nostrand 1950)

3. "The Theory of the Properties of Metals and Alloys", N.F. Mott and H. Jones (Oxford, Clarendon Press 1936)

4. "Semi-Conductors", Chapter 2, D.A. Wright (Methuen 1950)

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: MODIFICATION OF THE DUMONT 304-H OSCILLOSCOPE TO REDUCE DRIFT ENCOUNTERED IN WWI DISPLAY

To: 6889 Engineers

From: Dee J. Neville

Date: October 29, 1952

Abstract: The DuMont 304-H scopes show erratic drift of the electron beam. This drift in most of the scopes is undesirable for WWI display. The drift appears to be due to non-linear tube characteristic changes in the scope amplifiers, and is initiated by line voltage fluctuations. Without extensive modification, the drift can be reduced effectively by tube replacement and the removal of two stages in the Y amplifier.

1.0 STATEMENT OF THE PROBLEM

In some of the DuMont 304-H display scopes a shift as much as 1/4 inch, mainly in a vertical direction, has been observed.

The aim of the work on the scopes was to reduce drift as much as possible without making an extensive modification. Also the modification was worked out principally with the WWI display problem in mind. The direct cause of the electron beam drift is instability in the amplifiers, the Y amplifier being the most intolerable as is brought out in paragraph 4.1.

2.0 OPERATION OF THE Y AMPLIFIER

The Y amplifier schematic is at the end of report (dwg. SA-52898). An explanation of the main features of operation follows.

2.1 Theory

The balanced push-pull arrangement of the tubes is designed to give great stability.

A d-c balance adjustment (R10) is provided so that with no input signal the gain control (R7) can be moved without changing the position of the spot on the screen.

D-c positioning is obtained by use of R20. This changes the plate voltages of V2 in opposite directions, resulting in positioning of the electron trace. Centering of the electron beam, when Position Control is at its center, is accomplished by R16.

This type of positioning control requires that the variable resistor (R20) be small compared to the plate load resistors (R12 and R13), since the plate load resistors are in effect varied as the plate voltage is varied and non-linearity results. The degree of non-linearity due to positioning is proportional to the ratio of R20 to R12 and R13.

R24 provides a variable partial short between the push-pull plates of V3 for sensitivity adjustment. This is normally set to give 10mv/in. deflection sensitivity.

The screens and plates of the last stage are operated from the unregulated supply, so that the sensitivity of the system rises with an increase in line voltage, due to increased amplifier gain. This essentially compensates for the reduction in CRT sensitivity which is experienced at higher accelerating potentials resulting from higher line voltages. R36 varies the screen resistance in this stage to provide for linearity adjustment when the top and bottom of the CRT screen show a different sensitivity than the middle.

The peaking coils (L1 and L2) help maintain the high-frequency response of the amplifier. Additional high-frequency compensation is obtained by means of degenerative feedback through the 1-megohm resistors, R22 and R26.

As is the requisite for direct coupled amplifiers the grid d-c voltages cascade upward from one stage to the next. To obtain proper bias in the final stage, the cathodes are connected to the regulated 110 volts.

2.2 Measurements

The test conditions for the following data on the Y amplifier are: no feedback, gain control set maximum, sensitivity maximum, and the input signal of the particular stage just below the point of noticeable distorted output.

Stage Number	1	2	3	4	5&6
Input signal (pk to pk)	14v	10v	7v	5.5v	8v
Output signal (pk to pk)	10v	33v	60v	22v	250v
Approx. gain*	0.7	3.3	8.6	4.0	31.2

The over-all gain when sensitivity is adjusted for 10mv/in. deflection is 5,500.

---

* These values of gain are lower than would be experienced when normally small signals are amplified. This is due to the large signals causing the tubes to be operating out onto the non-linear portions of the characteristic curves.

3.0 ANALYSIS OF THE DRIFT

It seems that drift is largely due to line voltage fluctuation. Even though a scope is plugged into a supply regulated to within 1%, the input voltage variation may be as great as 1 volt.

3.1 Tube Characteristic Changes

Because of a fluctuating line voltage, the B+ and the filament voltages in the amplifiers vary some small amount. This means that the operating conditions of the tubes vary, and that the tube characteristics also change.

Duo-tubes or tube pairs selected to be balanced ($I_{b1} = I_{b2}$) at one operating point do not necessarily remain balanced over a range of operating points. Thus it appears that the tubes in the scope amplifier do not remain balanced when the fluctuating line voltage changes their operating conditions. This can mean that the plate currents of a push-pull stage do not increase or decrease at the same rate with a fluctuating line voltage, and a consequent off balance or output d-c signal can occur. This effect can be visualized in the first stage of the Y amplifier for example. Assume the d-c balance is adjusted for an average line voltage. Then let the line voltage increase and say that the #1 plate current has increased more than the #6 plate current. This will put an increased d-c level on grid #2 of the second stage. Though the effect here may be small, it is amplified through the rest of the amplifier and can give a noticeable drift of the electron beam.

It can be seen from this analysis that tubes having the best possible balance over a range of operating conditions should be placed in the first stages of the amplifiers.

3.2 Measurements

From the output of the amplifiers (directly connected to deflection plates) an average of 55 volts d-c is required to deflect the electron beam one inch. On a typical scope it was found that a 1-volt line change varied the Y amplifier output as much as 11 volts d-c which gave a vertical drift of .2 inches. The X amplifier drifted as much as 2.7 volts, or about .05 inches.

4.0 SOLUTION OF THE PROBLEM

4.1 Tube Replacement

Theoretically, tube replacement with all perfectly balanced tubes (balanced over all possible operating conditions) would solve the drift problem. However, this is an impossible desire to meet as it is even difficult to obtain tubes closely balanced at one operating point.

By replacing the amplifier tubes with as nearly balanced tubes as could be obtained (best balanced tubes placed in first stages), the drift was improved by a factor of 4 in the Y amplifier and by a factor of 2 in the X amplifier. This amount of drift in the X amplifier can be tolerated, so only the Y amplifier was modified.

4.2 Reduction of Sensitivity

The computer decoder output amplifiers feed signals of from +2 to +22 volts into the deflection lines.* With this amplitude of input signals the high gain of the Y amplifier is obviously not needed. Stability can be increased then, by reducing gain. It is important to note that the actual gain of the amplifier (V2 through V6) remains constant regardless of the gain control setting. This means that little improvement in drift can be realized by supplying larger input signals since such signals would merely be attenuated in the gain controls ahead of the amplifier.

The positioning system as explained in paragraph 2.1 is such that even with a vertical deflection equivalent to 4 times full-screen diameter, any 5-inch portion of the 20-inch vertical deflection may be centered on the CRT screen. This condition is desired for WWI display. A reduction of sensitivity either by means of the sensitivity adjust, or by increased negative feedback from stage 4 to stage 3, reduces the effect of the positioning control, which is undesirable.

4.3 Modification

The desired reduction in sensitivity was obtained by removing stages 3 and 4 as shown in the Modified Y-Amplifier schematic of drawing SA-52899. To obtain proper operating bias for tubes V5 and V6, a 3900 ohm common cathode resistor was used for this stage. Also, to provide adequate positioning control a dual-potentiometer was connected as shown in place of potentiometer R20 in the original circuit.

This modification removes two sources of tube drift, besides cutting down the gain of the amplifier and allowing larger signals to be fed into stages 1 and 2.

The amount of voltage on the deflection plates of a CRT has an effect on the focus of the electron beam. For sharpest focus, the value for the scopes tested was found to be about 210 volts. The cathode circuit change in V5 and V6 made it necessary to change the load resistors for these tubes in order to obtain a voltage close to this optimum value.

A list of the components needed to make the modifications described and an outline of the detailed steps involved are given in the attached appendix.

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* Specifications as given on drawing SA-36905. Amplifier designed by R. Best.

5.0 COMPARISON OF CHARACTERISTICS BEFORE TUBE REPLACEMENT AND AFTER MODIFICATION

After modification, the drift is improved, the Y amplifier sensitivity and frequency response are reduced. The high-frequency response could probably be improved but this is not required for WWI display purposes.

5.1 Drift	before	after
Y amplifier	11v d-c (.2 in)	.5v d-c (.009 in)*
X amplifier	2.7v d-c (.05 in)	1.5v d-c (.027 in)**

5.2 Sensitivity	before	after
Y amplifier	10mv/in. (adjustable)	100mv/in.
X amplifier	70mv/in.	60mv/in.

5.3 Frequency Response	before	after
Y amplifier	10% response point at 100 kc	10% response point at 70 kc

5.4 Rise Time

The rise time of the Y amplifier is approximately 2 μseconds.

---

* Approximately equal to 1/5 the diameter of a finely focused spot.

** Approximately equal to 1/2 the diameter of a finely focused spot.

SIGNED Dee J. Neville
Dee J. Neville

APPROVED E S Rich
E. S. Rich

DJN/cp
Drawings attached: SA-52898
SA-52899

Appendix attached
cc: A. R. Curtiss, N. L. Daggett, S. H. Dodd, R. H. Gould, L. L. Holmes, W. A. Karlsen, H. J. Kirshner, A. P. Kromer, J. A. O'Brien, B. B. Paine, E. S. Rich, A. V. Shortell, C. R. Wieser

APPENDIX

COMPONENT PARTS LIST FOR MODIFICATION

Tubes

3	12AU7 or 5963	(duo-triode, plate current balanced)
2	6J6	(duo-triode, plate current balanced)
2	6AQ5	(pair, plate current balanced)

Resistors

1	10,000 ohm dual potentiometer - 2 watt
2	33,000 ohm 1/2 watt 10%
2	20,000 ohm 10 watt 10% *
1	120,000 ohm 1 watt 10%
1	3,900 ohm 2 watt 10%

MODIFICATION INSTRUCTIONS

Stages V_2, V_3, and V_4

A. Remove tubes V_3 and V_4.

B. Remove feedback resistors R22 and R26 (this now allows grid pin connections to be used as terminals).

C. Remove Y position potentiometer R20, and connect the three leads removed from potentiometer, together.

D. Replace R14 and R19 with the dual potentiometer mounted in Y positioning control position. Connect center taps to pins 7 of V_5 and V_6.

E. Replace R15 and R18 with the 33,000-ohm resistors.

Stages V_5 and V_6

A. Remove R33 and disconnect C8-A from pins 2 of V_5 and V_6. Reconnect the 47-ohm resistor and 10 µfarad capacitor in series to the regulated 110 volts.

B. Connect 3,900-ohm resistor from pins 2 of V_5 and V_6 to ground.

C. Replace R32 and R35 with 20,000-ohm resistors.

D. Replace R34 with 120,000-ohm resistor.

---

* 20,000-ohm, 10 watt resistors not standard stock. These resistors are in WWI stock.

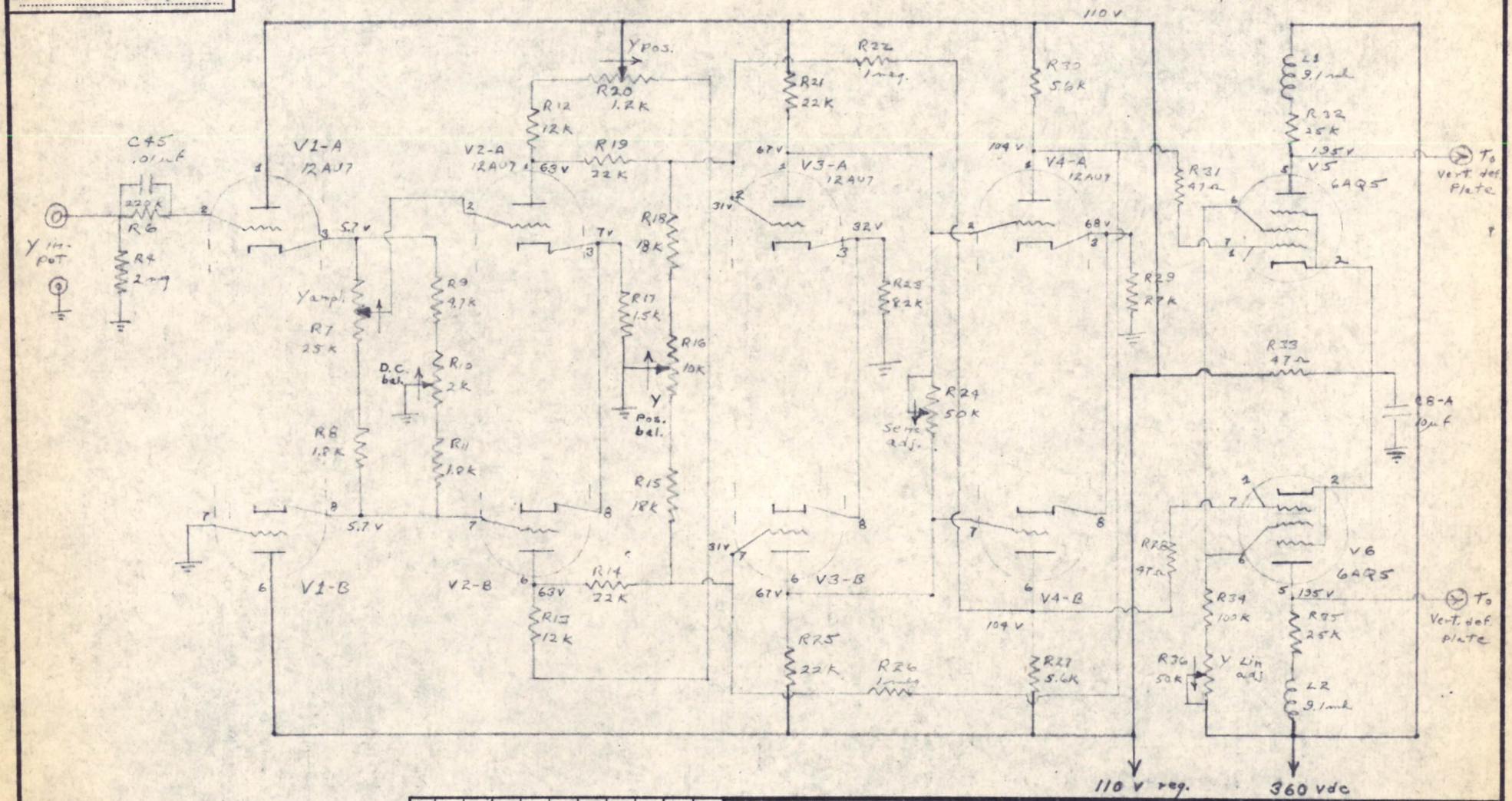
Both Amplifiers

Replace tubes V_1, V_2, V_5, V_6, V_{11}, V_{12}, and V_{13}.

Adjustments

The d-c balance, position balance, and linearity adjust on both amplifiers will require readjustment as instructed in DuMont 304-H manual.

SA-52898



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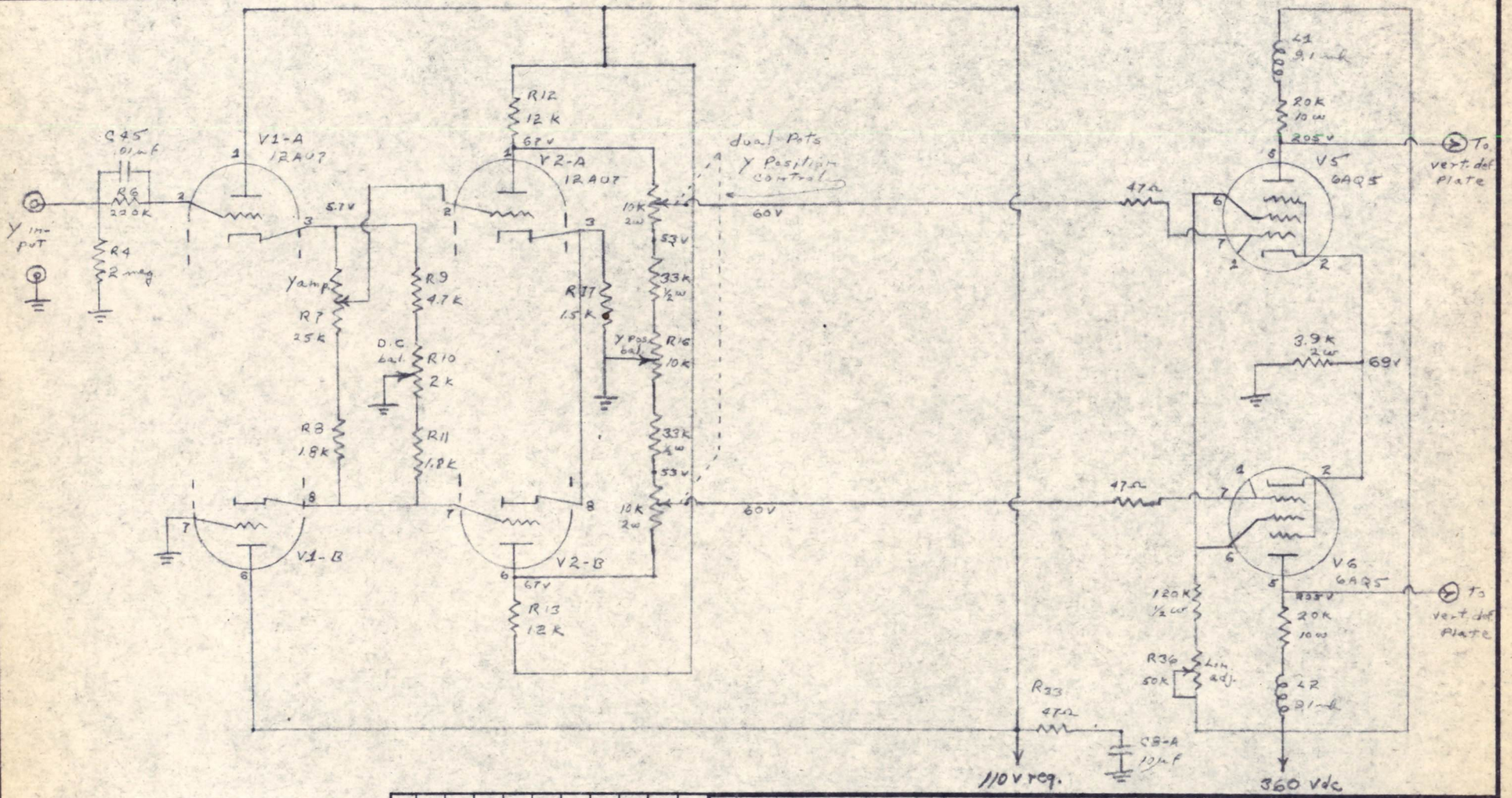
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING — D. I. C. PROJECT NO.

Y Amplifier Schematic — DuMont 304-H

SCALE:	DR. DJ 7/1	SA-52898
ENG.	CK.	APPD.

SA-52899



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MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING – D. I. C. PROJECT NO.

Modified Y Amplifier Schematic – DuMont 304H

SCALE:	DR. DJ	SA-52899
ENG. DJ	CK.	APPD.

CORRECTION SHEET

Engineering Note E-496

On page 1

1.1, Section 2

Reads: Ferramic H rings, F-262
$500.00/1,000

Should read: Ferramic H rings, F-262
$180.00/1,000

Signed Robert E. Hunt

REH:jrt

Copies to:

F. F. Manning
R. Bradley
N. Taylor
C. Watt
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Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: INSTRUCTIONS AND SPECIFICATIONS FOR THE MANUFACTURE OF 3:1 AND 1:1, 0.1 MICROSECOND PULSE TRANSFORMERS ON FERRITE RING CORES.

To: Production Control

From: R. E. Hunt

Date: November 3, 1952

Abstract: This paper was written to serve as a guide to the manufacture of toroidal pulse transformers. It includes detailed construction specifications, and enough information to permit a cost analysis to be made.

1.0 Cores:

1.1 Procurement: The cores used are toroidal, with rectangular cross section, 3/16" I.D., 3/8" O.D., 1/8" deep. See Fig. 1. Two suppliers currently approved are:

1. The Stackpole Carbon Co.
   St. Mary's, Pennsylvania

   Ceramag 5N material (specify ring size)
   Cost: $50.00/1,000; plus $200.00 tooling charge.

2. General Ceramics & Steatite Corp.
   Keasbey, New Jersey

   Ferramic H rings, F-262
   $500.00/1,000

1.2 Deburring: The rings as received have very sharp edges that will strip the insulation from the magnet wire during the winding operation. These edges must be removed. We use a small tumble mill revolving at 22 RPM. See Fig. 2. Place in the tumble mill a mixture of equal parts of:

1. Cores to be deburred
2. 1/4" dia. balls
3. 1/8" dia. balls
4. 1/8" dia. diagonals
5. "Norbide" #50-#70 grit abrasive

The cores should be tumbled from 2-6 hours; however, the vendor should experiment with the tumbling operation to secure the optimum proportions of the mix and the optimum load. A cascading, equally mixing operation should be obtained, and care should be taken not to tumble too long, as the cores will flake under these circumstances. Tumbling equipment may be purchased from the following source:

Manning and Manning, Inc.
202-208 Emmet Street
Newark, New Jersey

Tumble mill: Belfor model, large enough for 500 cores/operation---$110.00
1 lb. each of 1/8" dia., 1/4" dia. balls, and 1/8" dia. diagonals---$10.00

1.3 Painting: After deburring, the cores must be given a protective coating. The ferrites are very abrasive compounds and also are conductors. The windings must be protected from abrasion and electrical shorting to the core. This is accomplished by priming the core, finishing with a complete coating of white lacquer, and then baking. Currently the vendor used for this operation is:

Nye's Japenamelac Shop
98 Brookline Avenue
Boston, Mass.

The cost is approximately $15.00/1,000 cores.

2.0 Winding:

The 1:1 and 3:1 transformers are wound as per MIT drawings SA-52032 and SA-52033, respectively. Formex double-coated wire should be used. They are wound on a specially designed toroidal core winder. See Fig. 3. This winder may be procured at a cost of about $1750, or drawings may be obtained from M.I.T, either of the two alternatives only by permission of M.I.T. and the U. S. Air Force.

The machine would require less than 4.5 minutes per core for the 3:1's, and slightly longer for the 1:1's. The transformers may also be economically hand wound for small runs. Care should be exercised that the turns of the windings of one coil do not overlap one another.

To secure the windings and prevent unraveling, we recommend melted beeswax. The core coils are to be secured individually, one on each side of the core. See Fig. 4. This wax may be kept molten in a solder pot on a very low heat. The pot must be modified or driven by a variable auto-transformer. The wax may be applied by a small thermally insulated probe, the metal tip of which is shown in Fig. 5. The metal tip is five inches long, and 1/8" in diameter. The end is drilled 1/8" deep with a 1/16" hole, and tapered to 1/16". The metal tip is mounted in a penholder, with 3" showing.

Care should be taken to use only a bare minimum of staking wax as excesses may hinder the plastic casting process to follow.

3.0 Assembly:

3.1 Terminal board: The initial assembly consists of inserting 4" #20 AWG. pigtails into the terminal board shown in A-51424-1 and bending the terminals up. Leave the terminals about 3/16" - 1/4" high. See Fig. 6.

3.2 Procurement: Terminal boards for these transformers can be obtained from:

Precision Metal Products Co.
41 Elm Street (Rear)
Stoneham, Mass:

Terminal Boards, M.I.T. DWG #A51424-1 ---$100.00/1,000.

3.3 Stripping wire: The wound core should then have its leads stripped back to within 1/16" of the core, using "X-Var" remover. "X-Var" remover can be obtained from:

The Fidelity Chemical Products Corp.
470-474 Frelinghuysen Ave.
Newark, New Jersey

The remover should be applied by inserting the wire into a medicine dropper filled with the X-Var. See Fig. 7. If any X-Var gets onto the core or the windings, the core and windings should be immediately discarded, unless the core is cleaned of paint, repainted, and rewound.

After allowing a few seconds for the X-Var to set, it should be wiped using a clean piece of toilet tissue dipped in denatured ethyl alcohol. See Fig. 8. It is important that each wiping be done with a clean wiper. If the cleaning has to be done twice to remove all X-Var, the second wiping should be done with a clean, new wiper. Thus we use strips of toilet tissue for economy and convenience. The alcohol, of course, cleans and stops the action of the X-Var.

3.4 Soldering: The windings of the core are then attached to the terminal board so that terminals 1 and 3 are of the same polarity. The details of terminal numbers and winding sense are shown in drawing nos. SA-52032-1 and SA-52033-2.

A 60 watt soldering iron or smaller, or soldering tweezer should be used, and a #18 resin core, 60% tin, 40% lead, solder. Great care should be exercised not to let the soldering iron or heated terminal come into contact with the core or its windings. Thus, we clamp our terminal board in a horizontal plane on a vise, and support the core so that the top of the core is 1/8" below the bottom of the terminal board. We wrap the wires at least twice around the bottom of the terminal wires with the core in this position. See Fig. 9. Thus, when the wire is soldered, there is little

chance of contact between heat and the core. See Fig. 10. In the case of the 3:1 transformer, bend the end of #1 pigtail for future reference.

After soldering, cut the terminal wire down to 1/32 to 1/16" long. A clean, effective soldering job must have been done. See Fig. 11. Then press the core into the terminal board, making sure the service loops thus formed are free. See Fig. 12.

4.0 Interim Inspection:

The finished assembly must be minutely inspected under a magnifying glass, or jeweler's eyepiece. The following defects should be looked for:

1. Poorly soldered terminals.
2. Incorrect orientation of leads.
3. Damaged windings: nicked insulation.
4. Damaged cores, lacquer chipped to core at winding.
5. Excess of staking wax.

Only perfect assemblies may be passed. M.I.T. will insist on credit for any transformer whose failure in test or in use can be traced to inadequate workmanship.

5.0 Casting:

5.1 Mold: Finished assemblies should be placed in transformer mold D-51634. Each assembly should be flush on the side opposite the terminals: the core should not protrude from the bottom. After being placed in the mold, the assembly should be inspected for clearance, and in the case of the 3:1, for correct orientation. The terminals should always be facing up from the bottom of the mold: (the part of the mold with pins.) See Fig. 17.

5.2 Plastic: Now the plastic may be mixed. It should be mixed to the proportions of 3/4 of casting resin 1030CM to 1/4 of casting resin 4030CM. The plastics must be slowly but thoroughly stirred individually and as a mixture; i.e., they must be thoroughly mixed but with a minimum of air bubbles. See Figs. 13-14. Six (6) to ten (10) drops of catalyst #7 per fluid ounce must be added to the mixture. The catalyst can best be measured by a medicine dropper. See Fig. 15. The source of these plastics and this catalyst and their prices are:

Emerson & Cuming, Inc.
126 Mass. Ave.
Boston, Mass.

Casting resin 4030 CM	$22.00/gal.
Casting resin 1030 CM	$23.00/gal.
Catalyst #7	$7.00/1/2 pint

Each transformer requires about 1/4 fluid oz. of the prepared mixture. Mix about 2 fluid ounces for a 9 unit mold. Do not mix more than can be used in five minutes, as this mixture will start to solidify in this period. We find that mixing in paper cups with glass stirring rods result in saving time and utensils. See Figs. 13-15.

5.3 Vacuum treatment: The mold, after being poured (See Fig. 18), should be placed in a vacuum system for the purpose of eliminating entrapped air bubbles. The vacuum system should be brought to 20" of mercury 2 or 3 times, following which the vacuum should be broken rapidly. Care should be taken not to go above 20", as the mixture will boil between 20"-30" at room temperature. In lieu of a machine vacuum system, a dessicator jar driven by a water aspirator is entirely adequate.

5.4 Baking: After being evacuated the mold should be left at room temperature for 1/2 hour then baked in an oven at 80° C. (176 F.) for 1 hour. The mold may then be stripped and repoured.

5.5 Finishing: The assembly should be sanded smooth on the poured side (but not on the side with the numbers), and then stamped on the numbered side with coding lacquer 1:1 or 3:1 whichever the case may be. See Fig. 16.

6.0 Final Incoming Inspection:

Upon delivery M.I.T. will perform the following tests:

1. Pulse test to determine correct polarity and performance.

2. Hi-pot test, 1000 volts will be applied between primary and secondary.

Complete details of these tests and specifications are given in M.I.T. Engineering Note E-495. If the vendor is unable to perform these tests he should make suitable allowances for units not passing these tests.

Drawings Enclosed:

A-53031 Fig. 1 thru 5
A-53032 Fig. 6 thru 10
A-53035 Fig. 11 thru 16
A-52955 Fig. 17 & 18
A-52032-1
A-52033-2
A-51424-1
D-51634

Signed R. E. Hunt

Approved Cwwatt, Jr.

REH:jrt

Copies to:

F. F. Manning
R. Bradley
N. Taylor
C. Watt
D. Brown
H. Morley
W. Papian
W. Linville
E. Gates
B. Paine

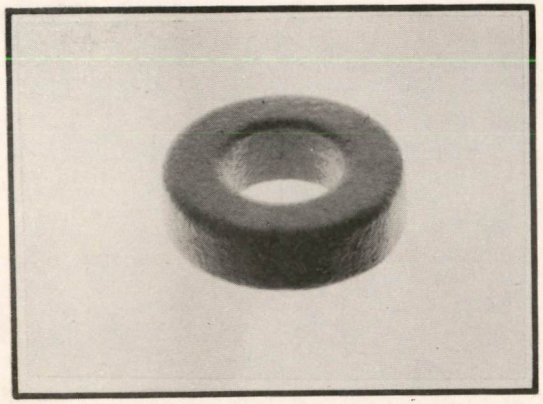


FIG. 1
FERRITE CORE

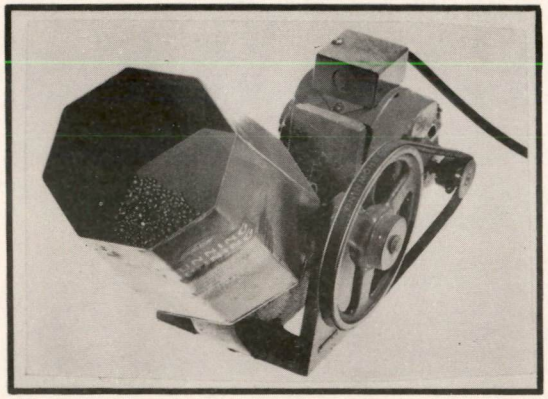


FIG. 2
TUMBLING MACHINE

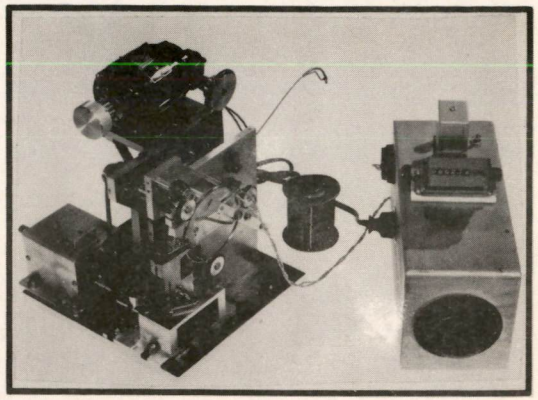


FIG. 3
TOROIDAL CORE WINDER

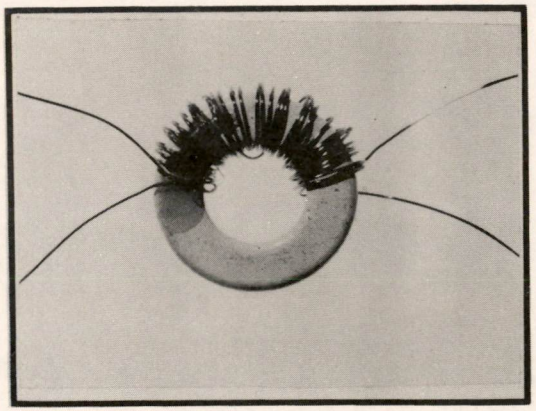


FIG. 4
WOUND CORE,
SECURED WITH BEESWAX

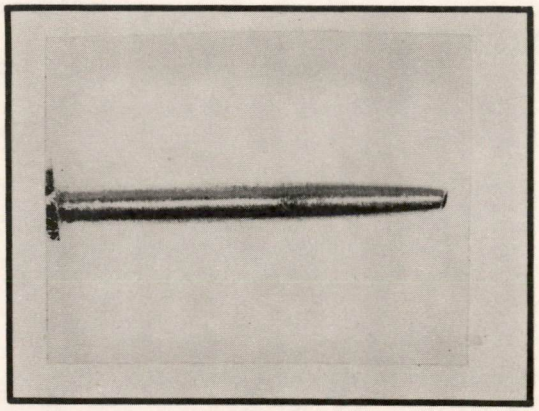


FIG. 5
BEESWAX APPLICATOR

CONSTRUCTION, 1:1 AND 3:1 PULSE TRANSFORMERS

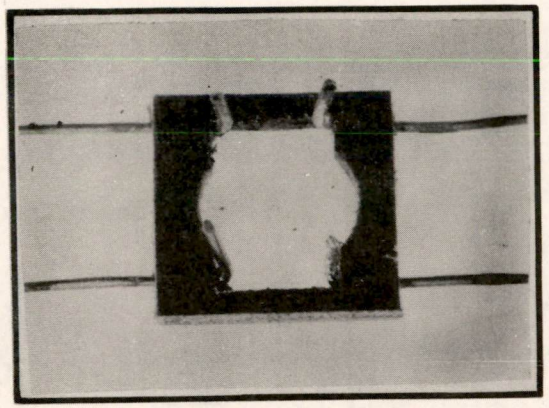


FIG. 6
TERMINAL BOARD WITH PIGTAILS

FIG. 7
APPLYING X-VAR

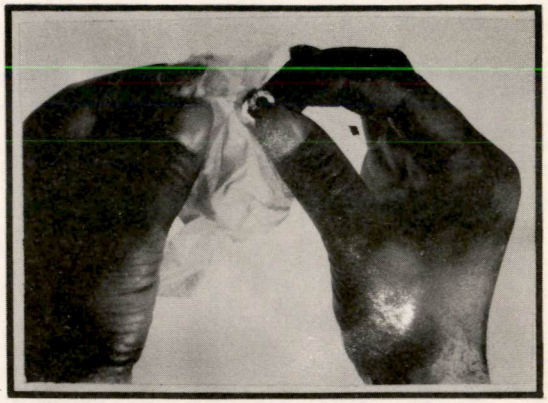


FIG. 8
WIPING COIL LEADS
WITH ETHYL ALCOHOL

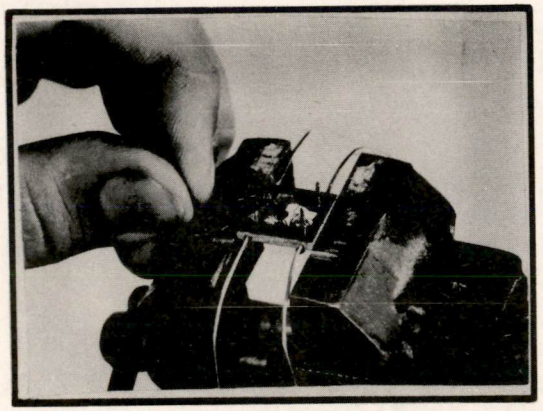


FIG. 9
WRAPPING COIL LEADS

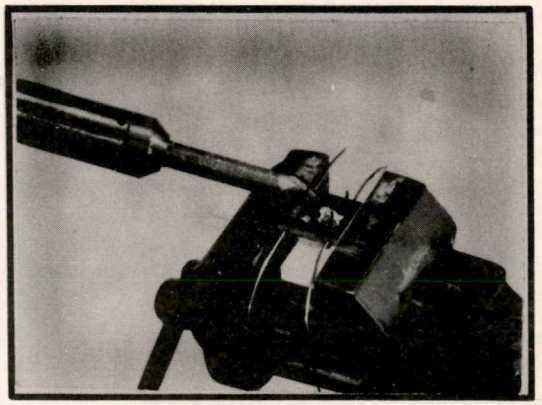


FIG. 10
SOLDERING COIL LEADS

CONSTRUCTION, 1:1 AND 3:1 PULSE TRANSFORMERS

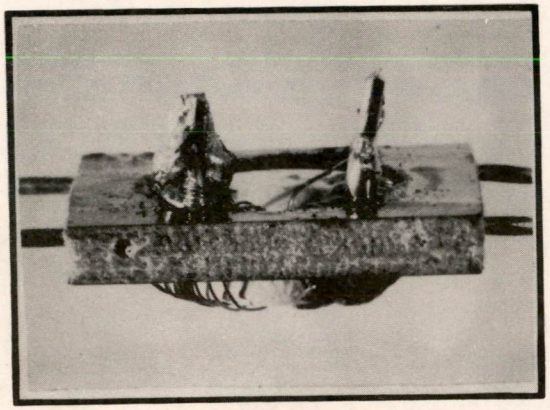


FIG. 11
GOOD AND BAD SOLDER JOINTS

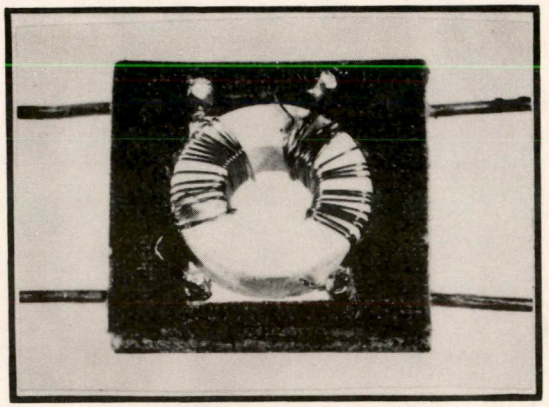


FIG. 12
A FINISHED ASSEMBLY

FIG. 13
STIRRING PREPARED RESIN MIXTURE

FIG. 14
POURING MIXTURE INTO CONTAINER

FIG. 15
ADDING CATALYST

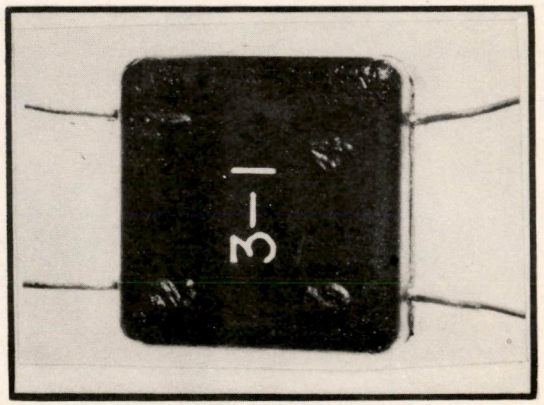


FIG. 16
A MOULDED ASSEMBLY

CONSTRUCTION, 1:1 AND 3:1 PULSE TRANSFORMERS

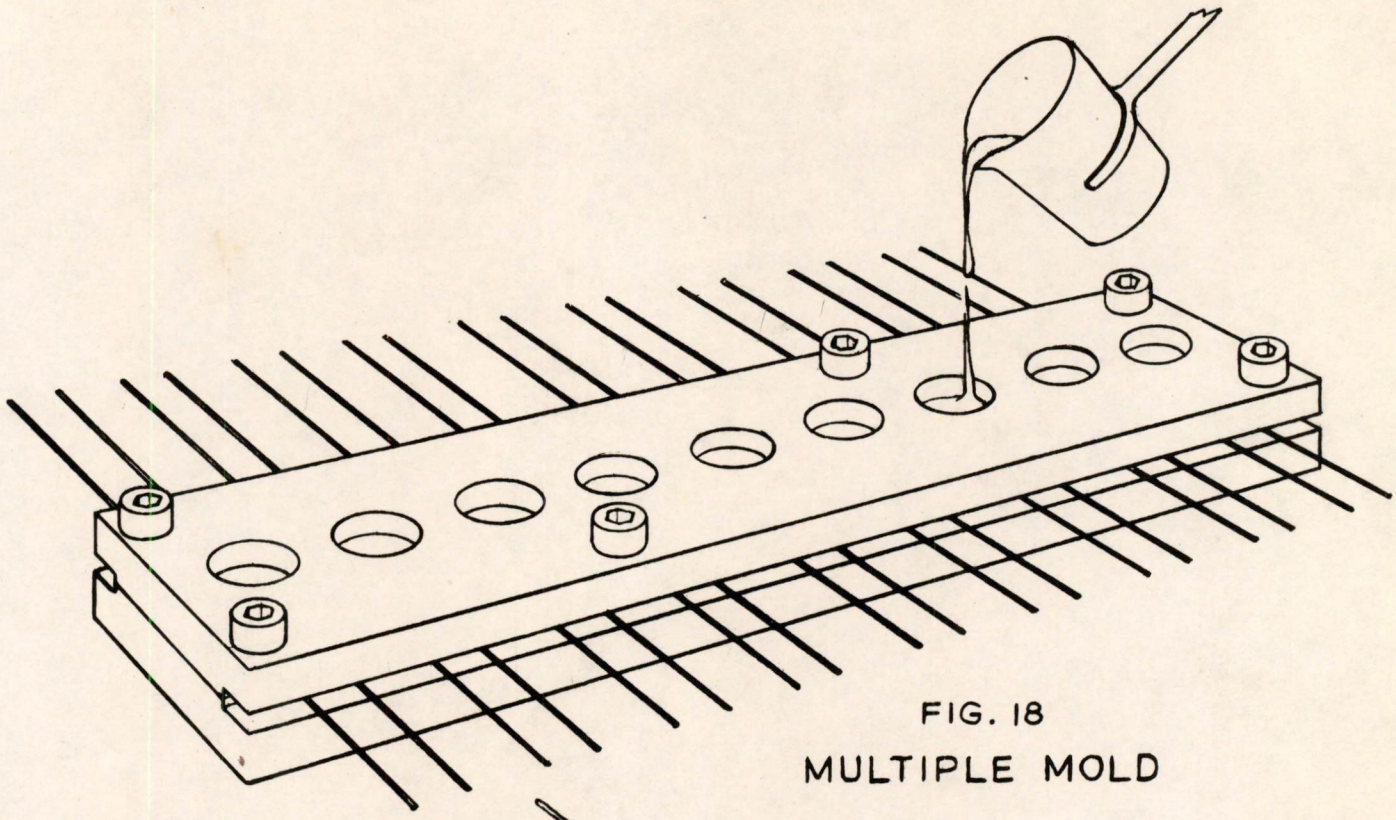


FIG. 18
MULTIPLE MOLD

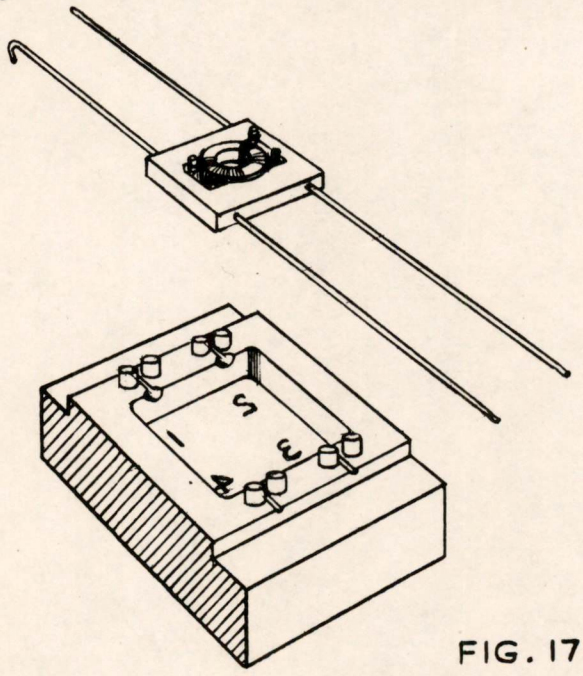
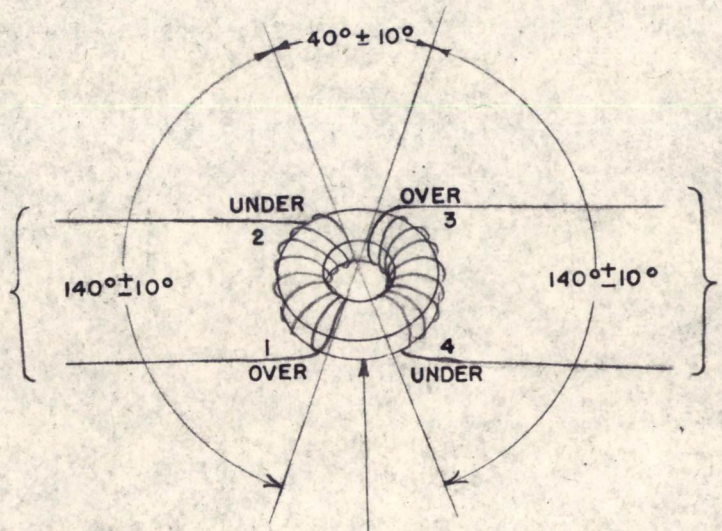


FIG. 17
DETAIL SHOWING
SECTION OF MOLD 1:1

MOLD FOR PULSE TRANSFORMER

A-52032-2

GRADED BY:	DATE:	THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:
		GRADE I FOR REFERENCE ONLY
ARB	11-25-52	GRADE II PRELIMINARY DESIGN
		GRADE III FINAL DESIGN

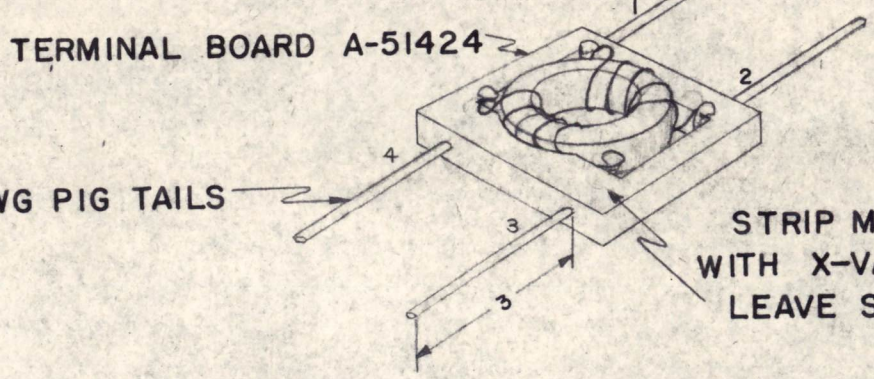


PRIMARY
24 TURNS
OF #37 AWG

SECONDARY
24 TURNS
OF #37 AWG

$\frac{3}{8}$" OD X $\frac{3}{16}$" ID FERAMIC H CORE
DEBURRED AND WHITE LACQUERED

LEAVE LOOP
TO IDENTIFY
LEAD #1

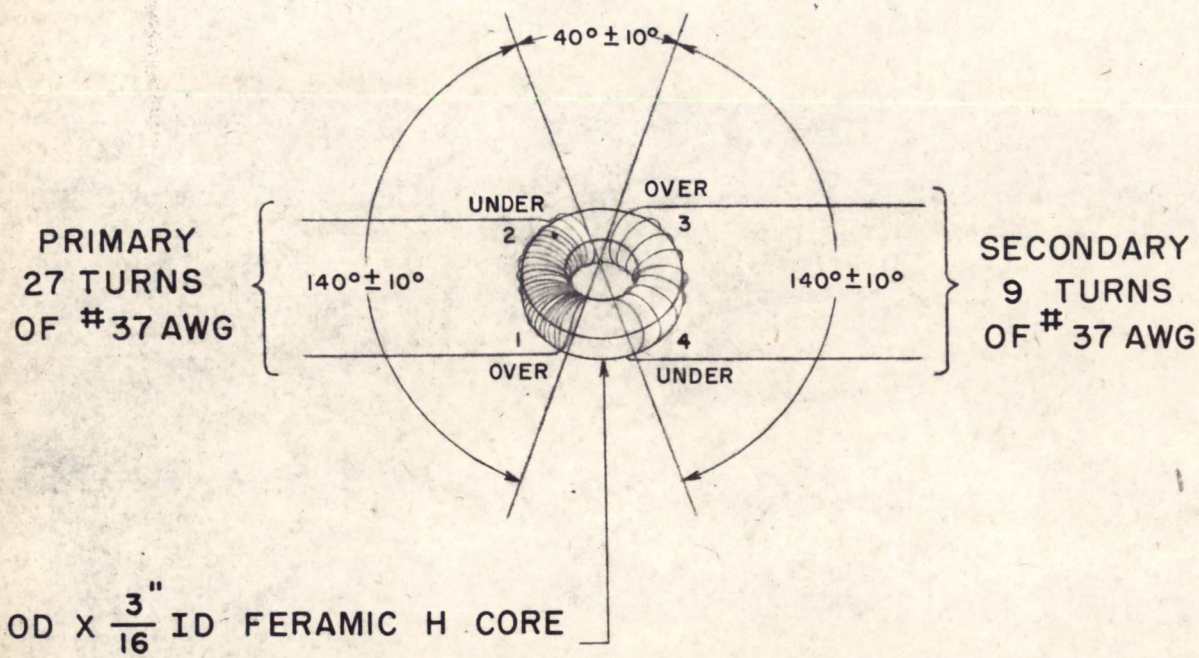


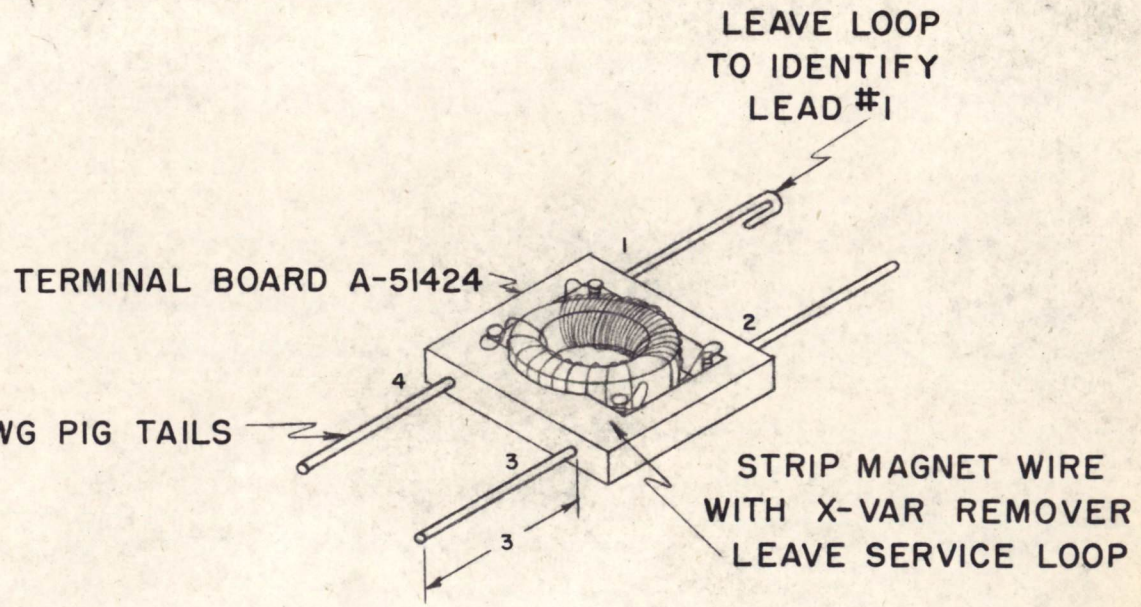
#20 AWG PIG TAILS

STRIP MAGNET WIRE
WITH X-VAR REMOVER
LEAVE SERVICE LOOP

1:1 TOROIDAL PULSE TRANSFORMER

A-52033



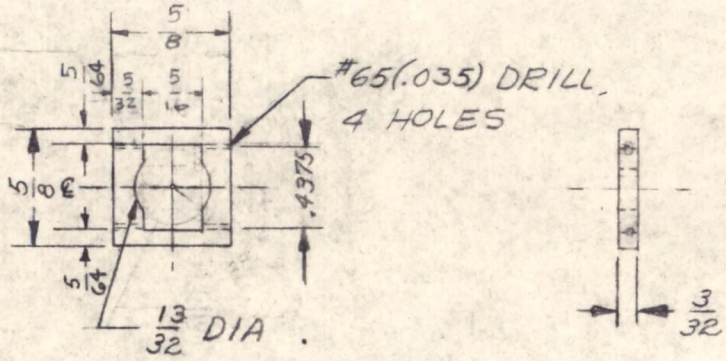


3:1 TOROIDAL PULSE TRANSFORMER

A-51424

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°

DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY



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GRADE I FOR REFERENCE ONLY
Ves 9-16-52 GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.
—	PHENOLIC, LINEN BASE 3/32 THK.	TYPE LE	—

CHG.	CN#	DATE	APPD.
-10			
-9			
-8			
-7			
-6			
-5			
-4			
-3			
-2	4155	11-7-52	R.E.F.
-1	NONE	9-8-52	R.E.F.

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING — D. I. C. PROJECT NO. 6889

EXPERIMENTAL TERMINAL BOARD FOR FERRITE CORE PULSE TRANSFORMERS

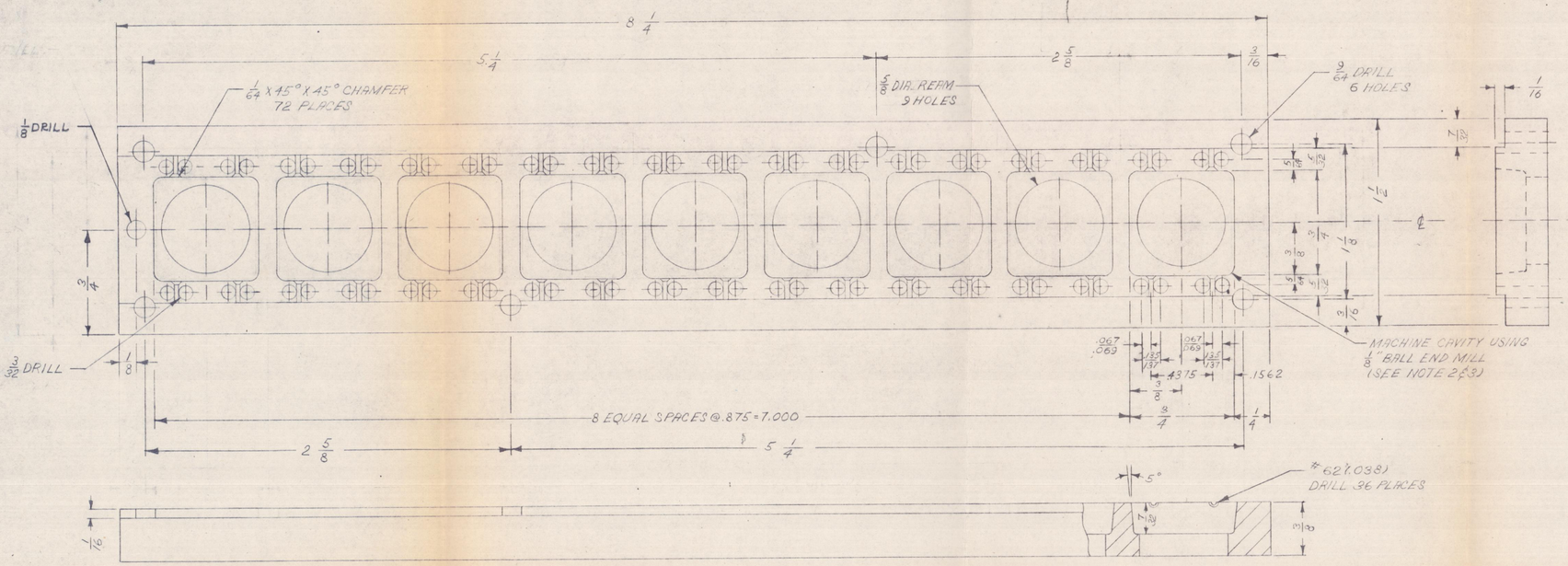
SCALE: 1:1 DR. A.D.A. 5-1-52

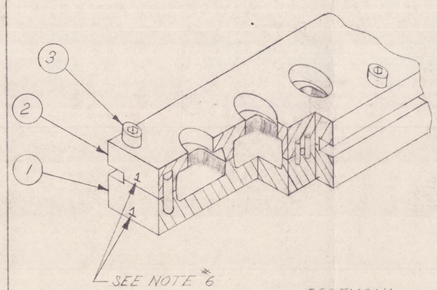
ENG. 5-2-52 R.E. Frost CK. 5-2-52 V Davis APPD.

A-51424

D-51634

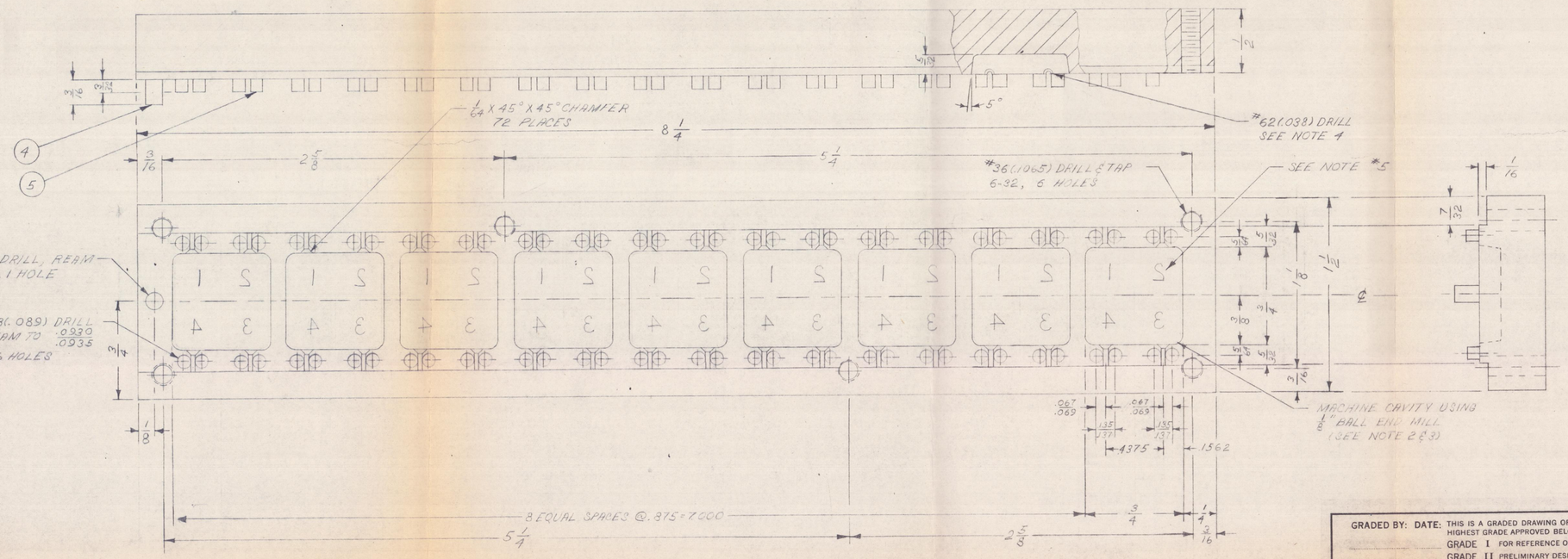
TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± 1/2°
DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY





ASSEMBLY
SCALE 1:1

ITEM 2



ITEM 1

NOTES:
1. REMOVE ALL BURRS & SHARP EDGES.
2. POLISH ALL INSIDE SURFACES.
3. COAT ALL INSIDE SURFACES WITH G.E. TEFLON PLASTIC.
4. SECURE TWO HALVES TOGETHER & DRILL #44 (.086) DIA. HOLES FOR 3/32 DOWELL PINS THRU TOP & INTO BOTTOM HALF. MAKE 1/32 A.015 DEEP SAWCUTS IN BOTTOM HALF AS PILOTS FOR .038 DIA. HOLES. REAM .086 DIA. HOLES AND SET 3/32 DIA. DOWELL PINS IN BOTTOM HALF. WITH HALVES SCREWED TOGETHER DRILL .038 DIA. HOLES IN 36 PLACES DOWN 1/32 SAWCUTS.
5. ENGRAVE MARKINGS, SHOWN IN ITEM #1, 1/8 INCH HIGH, 1/32 DEEP & IN POSITION SHOWN.
6. AFTER ASSY STAMP IDENTIFICATION NUMBER ON BOTH SECTIONS OF CAVITY AS SHOWN.

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.
5	PIN, ALIGNMENT ROD	3/8 DIA x 3/16	72
4	PIN, POLARIZING ROD	1/8 DIA x 7/16	1
3	SCREW, ALLEN CAP SST NON MAG	6-32 x 5/8	6
2	CAVITY (TOP SECTION) CRS STOCK	3/8 X 1 1/2 X 8 1/4	1
1	CAVITY (BOTTOM SECTION) CRS STOCK	1/2 X 1 1/2 X 8 1/4	1

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING — D. I. C. PROJECT NO. 6889

ASSEMBLY, MOLD FOR 0.1 MICROSECOND TOROIDALLY WOUND PULSE TRANSFORMERS

SCALE: 2:1 DR. JAYNES 9-17-52
ENG. 9-27-52 R.E. Hunt CK. 9-26-52 V. Zaroni APPD.

D-51634

GRADED BY: DATE: 9-29-52
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GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN

CHG.	DATE	APPD.
1	9/11/52	RE H

J. W. Forrester

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: AN ELECTRONIC HOLDING CIRCUIT

To: All Engineers

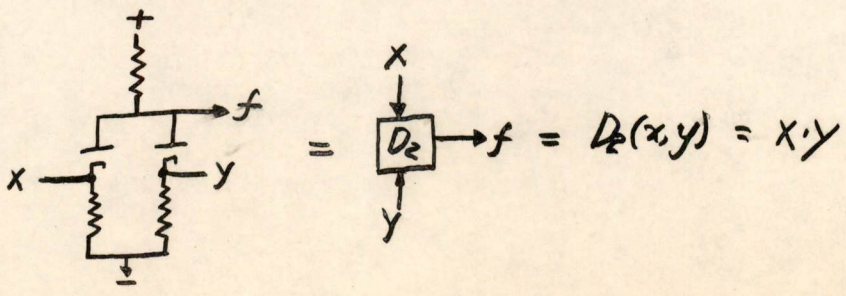
From: J. A. O'Brien

Date: November 12, 1952

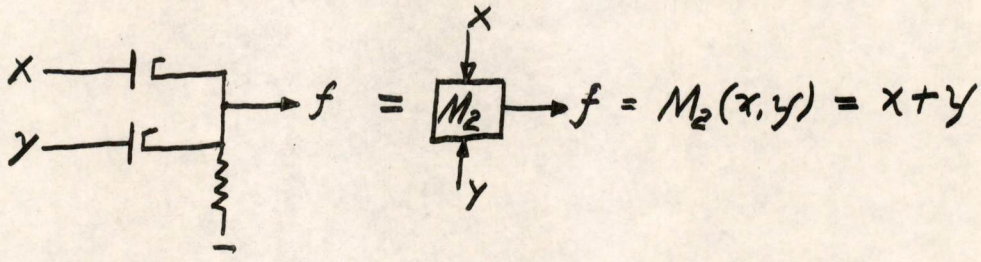
Abstract: An electronic holding circuit, analogous to a relay holding circuit, has been tried and seems to have promise of being a useful device. The device consists of a two-input crystal "and" gate with a grounded-grid triode-amplifier as the gate load. The output of the amplifier drives a cathode-follower output tube. The two inputs of the crystal gate are (1) the holding voltage, (2) the input, or set, signal. The output of the circuit is mixed with the input voltage, so that once the set signal has operated the circuit the output signal can take over the function of the input signal and the input signal can then be removed. The circuit is returned to the cleared state by momentarily removing the holding voltage, thus breaking the path through the gate.

Some time ago this writer, while studying the application of Boolean algebra to electronic circuits, derived an electronic equivalent of a relay circuit with a holding contact. It consisted of a non-inverting crystal gate with the output fed back to the input. Briefly the equation is $f = h(s + f)$ where f, s and h are the output, input and holding voltages respectively. These quantities are assumed to have a value of either 1 or 0 where (using the convention shown in the recent E-note by Jeffrey and Reed, E-458), 1 indicates a high or positive voltage and 0 indicates a low or negative voltage. If we assume that initially $f = s = 0$, and $h = 1$, and then make $s = 1$, f becomes 1 and remains high as long as h equals 1 independent of s.

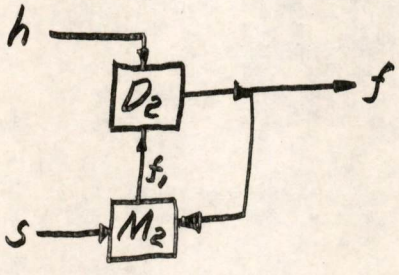
If we define a two-input diode gate as follows:



and further a two-input mixer



we can put them together as shown below,



where $f_1 = M_2(s,f) = s + f$

and $f = D_2(f_1 h) = hf_1 = h(s + f)$.

If it were desirable that the circuit pick up independent of h, and yet still require h to hold, then the equation could be $f = s + hf$. This is the expression for f_1 in the above circuit: $f_1 = s + f = s + hf_1$

Although the algebra shows this circuit to be feasible, it is obvious that it will not operate because, primarily, of the lack of gain in the feedback loop. Recently there has been a great deal of interest in various types of memory circuits, and it was felt that it might be worthwhile to put an amplifier in the circuit and see if it would work. Since the amplifier had to be non-inverting, had to have a minimum number of stages, and a low impedance output, a grounded grid triode amplifier was selected. The output of the amplifier was divided down through a potential divider and applied to the grid of a cathode follower. The first circuit constructed is shown in the attached drawing, SA-53034. The grounded grid amplifier is the anode load of the crystal gate circuit. The circuit shown is by no means a well designed circuit; it was constructed merely to test the principle. The amplifier load was made large to insure that there would be plenty of gain and the limits would be in the right

regions. The output of the circuit shown varies from -32 volts in the "cleared" condition to +20 volts in the "set" condition. The circuit as shown will operate with 0.1 μsec pulses, but it will probably work much better with wider pulses. The rise time of the output is about 0.8 μsec and the total fall time is about 1 μsec, although it is initially very steep. These figures are for no additional load. With a 100 μμfd capacitor across the output, a 0.1 μsec pulse will set the circuit, but will not clear it, presumably because the cathode follower will not fall fast enough with the circuit values shown.

Considering the circuit of SA-53034 it would appear that the circuit could be set by applying a negative pulse to the grid of V1, or it could be cleared by a positive pulse at this grid. Testing showed both of these cases to be true. Upon further consideration it became apparent that, due to the nature of the holding signal, the grid and cathode of the amplifier could be made the gating elements. To test these thoughts, the circuit was modified as shown in drawing SA-53033.

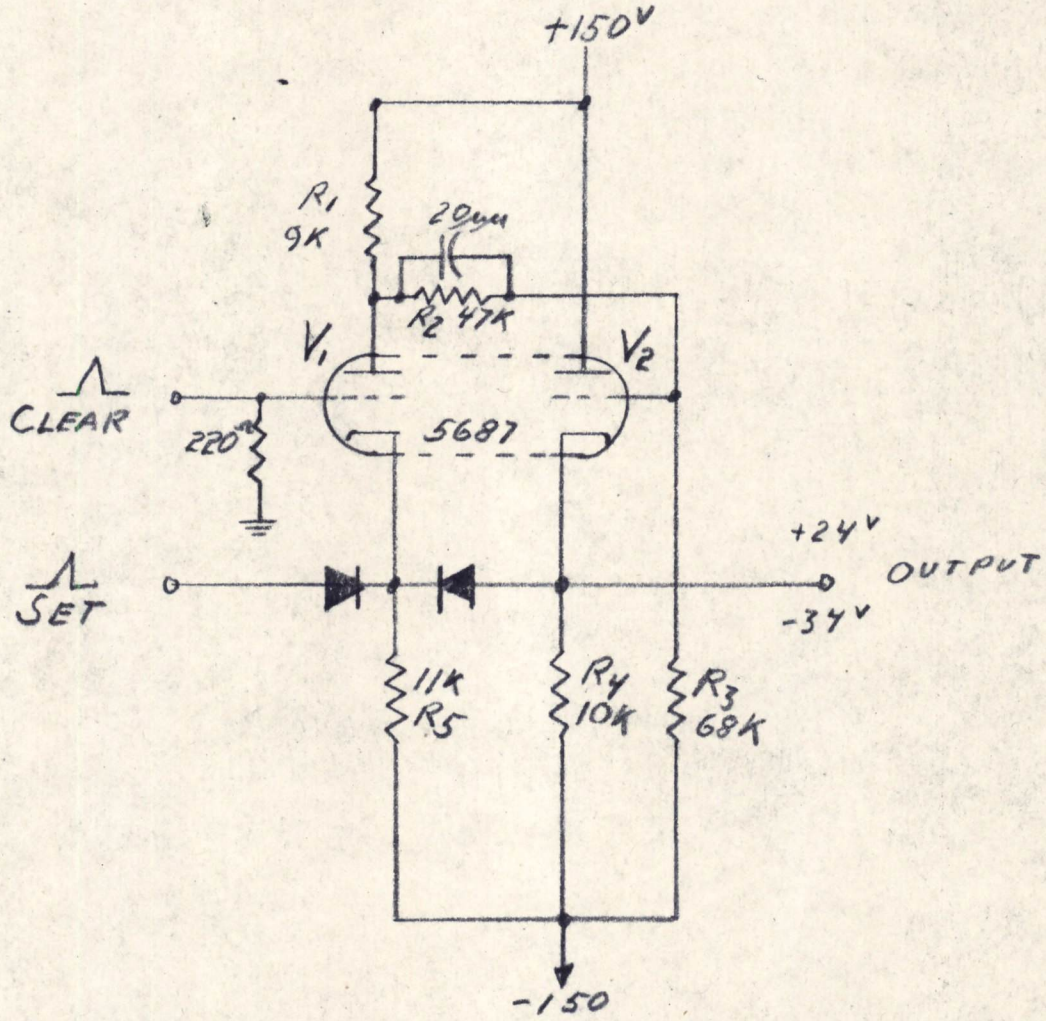
The modified circuit uses only two supply voltages, fewer components, and works better. R4 was reduced to 10K to decrease the output fall time, and R5 was raised to 11K (10K added in series) and returned to -150 volts to reduce the amount of current supplied to R5 by V2 to cut off V1 when the circuit is in the set condition. This also reduced the amount of change in the current through R5 and should increase the circuit stability. The clear pulse is now applied to the grid of V1, and both the set and clear pulses are positive pulses d-c coupled at ground voltage. The output voltage is about the same as previously. The circuit will drive at least 100 μμfds load with a rise time of 0.5 μsec and a total fall time of 0.5 μsec.

The voltage swing of the output is controlled primarily by R5, and the upper limit of the output is controlled by resistors R1, R2, and R3. R1 will also affect the output swing.

No testing was done from the point of view of marginal checking the circuit, but it would appear that this could be accomplished by varying either or both of the supply voltages.

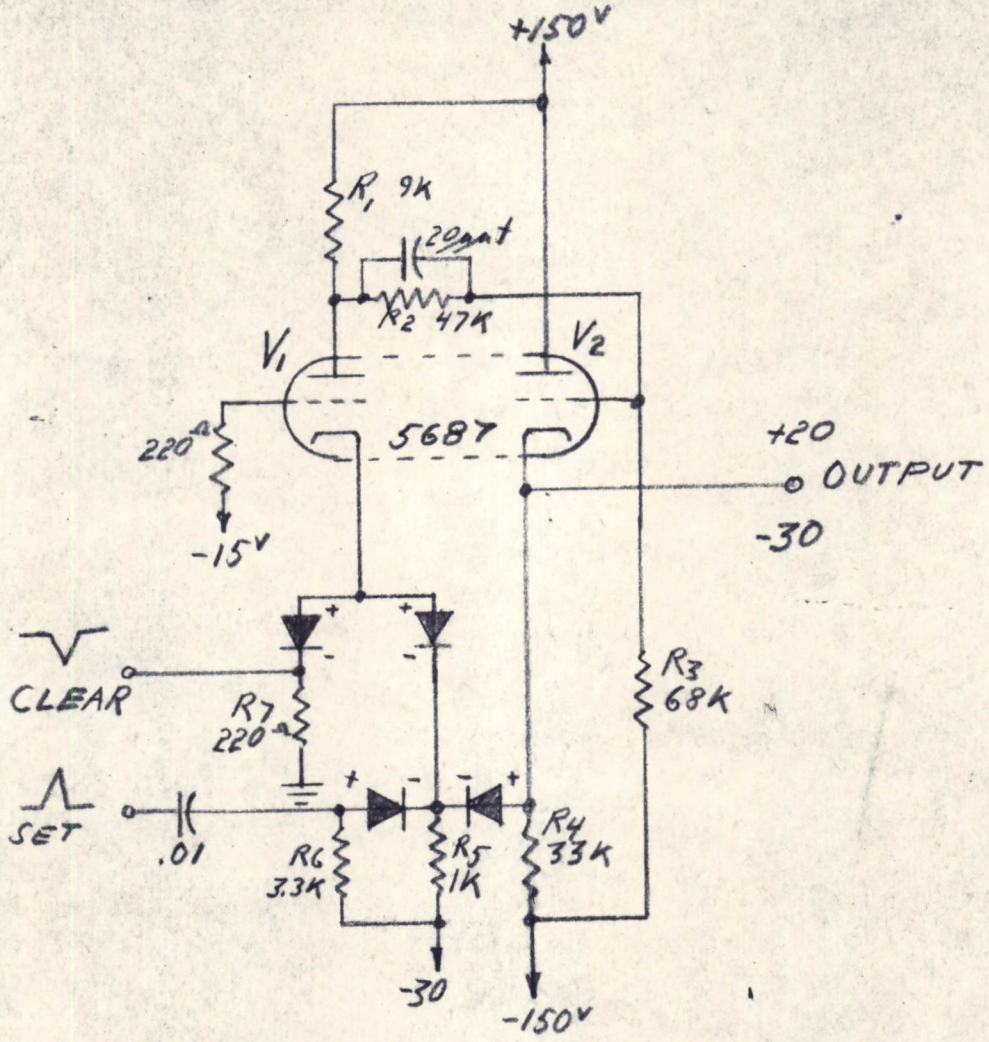
SIGNED J. A. O'Brien

JAOB/cp
Drawings attached: SA-53033
SA-53034



MODIFIED ELECTRONIC HOLDING CIRCUIT

SA-5-30 34



AN ELECTRONIC HOLDING CIRCUIT

SA-53034

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: SWITCH-CORE ANALYSIS I

To: N. H. Taylor

From: A. Katz and E. A. Guditz

Date: November 4, 1952

Abstract: Data derived from an experimental study of ferritic switch-cores is interpreted in terms of linear coupled-circuit theory. Despite the over-simplification resulting from assumptions of linear, time-invariant behavior and of negligible eddy-current and capacitive effects, it is found that such a model enables one to explain reasonably well the empirical results. Evident from the analyses, both experimental and theoretical, is the fact that simplicity of construction and effectiveness of transformer action place mutually contradictory constraints on the design of a magnetic-matrix switch. Whereas the former requires "few" turns per switch-core winding (one, if possible), the latter requires "many" turns so that the winding impedances will be large compared to that of the load.

1.0 Introduction

A considerable effort has been devoted, both at the Laboratory and elsewhere, to experimental studies of the responses of ferromagnetic core materials to various signal inputs. Interest in such materials stems from the fact that they possess those properties, non-linearity and hysteresis, which are essential to memory and switching applications. However, it is these same properties which render difficult any quantitative description of the behavior of circuit elements depending on these properties. Hence, experimental studies are a necessary preliminary to an understanding of such elements.

In this note we present and interpret experimental data derived from a grossly macroscopic, or "black-box" investigation of the behavior of certain ferritic cores operated as elements in a magnetic-core memory system. It should be noted that the results presented herein are based on a relatively small number of cores, and, hence, any conclusions derived should be accepted with circumspection.

2.0 Experimental Results

2.01 General Remarks

Before describing the experiments performed, we remark that the ultimate objective of this research is a semi-rigorous procedure for the design of a magnetic-matrix switch for use as a selection device for a magnetic-core memory

system. Figure 1 is a diagram of one form of such a matrix switch. Since the principles of operation of this switch have been adequately described elsewhere (1), we need merely remark that only one of the 2^n cores in the switch is not biased to saturation, and hence capable of producing an output when excited by the driver. A useful by-product of this research would be some sort of equivalent-circuit representation for the magnetic core elements used in the switch.

The environment in which the matrix switches operate is shown in Figure 2, which is a diagram of a selection system for a single digit plane of a magnetic-core memory array. Corresponding to the particular states of the n X-address (or Y-address) flip-flops, a certain set of drivers will so actuate the switch that only one, S_i (or S_j), of its 2^n cores is capable of transmitting energy to its load. In this way each switch selects one line of each of the two sets of co-ordinate lines, say X_i and Y_j, along which to apply a magnetomotive force of amplitude equal to half that required to switch a memory core. Only the memory core, M_{ij}, lying at the intersection of X_i and Y_j, will experience sufficient mmf to be switched-- provided that no inhibiting pulse is simultaneously applied by the Z-plane driver.

By abstracting to essentials we arrive at Figure 3 from which the scope of the design problem is evident. In this figure the following quantities are defined:

R_{g1} = Impedance of X and Y vacuum-tube (v.t.) drivers

R_{g2} = Impedance of Z-plane v.t. driver

L_1 = Network linking the X or Y v.t. drivers with switch cores S_i or S_j respectively. This includes the impedances reflected into the primary windings of S_i and S_j by other cores in their respective matrices.

L_2 = Network linking switch core S_i (or S_j) to the memory core M_{ij}. This includes the impedance of the unselected memory cores on the co-ordinate line X_i (of Y_j).

L_3 = Network linking the Z-plane v.t. driver with memory core M_{ij}. This includes the impedance of the remaining memory cores in the digit plane.

L_4 = Network linking memory core M_{ij} with the sensing unit. This includes any impedances reflected into the sensing winding as well as various noise sources (e.g., "delta" noise).

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1. Olsen, K. H., "A Magnetic-Matrix Switch and Its Incorporation Into a Coincident Current Memory", Digital Computer Laboratory Report R-211.

2.01 General Remarks (Cont.)

Even if the switch and memory cores were characterized by linear transfer functions, the design of the system shown would hardly be a trivial problem. When the cores are characterized by the flux-mmf relation shown in Figure 4 (as indeed they must be for these applications), then it is evident that the design of such saturable-core transformers must be preceded by much experimental study.

2.02 Description of Experiments

Although the research described here is still in progress, it is felt that a publication of partial results at this time would serve as a basis for drawing tentative conclusions and as a stimulus to further thought. This research might be divided roughly into the following sets of experiments:

(1) a study of switch cores wound with relatively large numbers of turns,

(2) a study of switch cores wound with relatively small numbers of turns, and

(3) a study of the static hysteresis curves for ferritic core types MF-1118 (F259) and MF-1131 (F262).

The first two sets were conducted under essentially the same conditions. In each case an MF-1131 (F262) core, wound with N_1 primary turns and N_2 secondary turns, was used as a link between the Z-plane v.t. driver and the Z-plane winding which threaded all of the MF-1118 (F259) cores in memory plane No. 2 of Memory Test Set-up No. 2. A simplified diagram of the set-up used is shown in Figure 5. A "rectangular" pulse of current of amplitude I_1, with duration of 1.5 microseconds and rise-time of 0.15 to 0.30 microseconds is applied to the primary winding of the switch core. A pulse of current of peak amplitude I_2 from the secondary then drives, through the Z-plane winding, the entire digit plane of memory cores from state A (at $-\phi_r$ in the flux-mmf plane in Figure 4) to state B. The X and Y drivers remain de-energized throughout these experiments. It has been experimentally determined that the plane of 256 cores, when operated in this mode, may be approximated reasonably well by an equivalent load of a 1 ohm resistor in series with a 2-microhenry inductor. Although this set-up does not represent a realistic application of a saturable-core transformer, it does provide valuable information relating to its use for driving large numbers of memory cores.

The distinction between these two sets of experiments shall arbitrarily be defined as follows: if N_1 or N_2 is greater than 10 turns, then the cores have windings with "large" numbers of turns; otherwise, "small" numbers of turns.

2.02 Description of Experiments (Cont.)

Such a distinction is necessary because simplicity of construction of a matrix switch requires "few" turns per winding, while effective transformer action requires "many" turns per winding.

The first set of experiments involved the study of an MF-1131 ferritic transformer with its primary winding tapped at 10-turn intervals over the range ($10 \leq N_1 \leq 100$), and its secondary tapped at 1-turn intervals over the range ($1 \leq N_2 \leq 5$) and at 5-turn intervals over the range ($5 \leq N_2 \leq 50$). The amplitude of the primary current pulse (I_1) was held constant at 400 milliamperes while N_1 and N_2 were varied, and the peak amplitude of the secondary current pulse (I_2) was measured. These data are plotted in various forms in Graphs I through IV. The interpretation of these data is given in Section 3.0.

It is evident that when the three variables -- N_1, N_2, and I_1 -- are fixed, then the fourth variable, I_2, is determined. In view of the fact that co-incident current operation of a memory array using MF-1118 (F259) cores requires about 1.5 amperes per selected coordinate line, it is also evident that not every combination of the first three variables provides the required current drive, I_2, for the array. It was therefore decided (on the basis of the first experiments) to select certain favorable combinations of N_1 and N_2, and then vary I_1 while measuring I_2. The particular combinations chosen were:

(a) $N_1 : N_2 = 20 : 5$
(b) $N_1 : N_2 = 25 : 5$
(c) $N_1 : N_2 = 30 : 5$

and I_1 was varied over the range of 0.2 to 2 amperes. The results of these tests are shown in Graphs V and VI.

Although attention thus far has been centered primarily on the peak amplitude of the current pulses (or mmf pulses), it is obvious that the shapes and durations of these pulses are of equal importance. In order to observe the effect of variations in driving magnetomotive force on the secondary current pulse, photographs were taken of the outputs of the three cores listed above for the same range of I_1 as was used in the peak amplitude measurements. These results are also discussed in Section 3.0.

After conducting these experiments with saturable-core transformers having "many-turn" windings, we then investigated similar phenomena for the "few-turn" case. Seven MF-1131 ferritic cores were wound with different numbers of primary turns: ($N_1 = 4, 5, \ldots, 10$). For each of these cores, the number of secondary turns was varied in 1-turn steps over the range ($1 \leq N_2 \leq 10$), the amplitude of the primary current pulse was varied over $0.5 \leq I_1 \leq 2$ amperes, and the peak amplitude of the secondary

2.02 Description of Experiments (Cont.)

current pulse was then measured. Some of these results are presented in various forms in Graphs VII through XII. In the course of these experiments, some cursory estimates were made of changes in shape and duration of the output pulse of the switch-core with changes in N_2 and I_1.

The third set of experiments consisted merely of the tracing (by B. Frackiewicz) of the static hysteresis curves for the two core types mentioned.

3.0 Interpretation of Experimental Results

3.01 Linear Analysis of the Coupled-Circuit Problem

In attempting to analyze physical systems one frequently postulates an idealized model, the behavior of which can be described quantitatively. The validity of the model may then be tested by using the equations which govern the idealized system to predict the behavior of the real system. If the correlation between experimental and predicted behavior is reasonably good, then one is justified in continuing the use of the model in further studies -- provided, of course, that the simplifying assumptions underlying the model are never violated.

In our case, the physical system to be analyzed consists of a toroidal core of ferritic material on which three windings are wrapped. Two of these correspond to the conventional transformer windings, while the third is used to reset the core to its "normal" remanent state at $-\phi_r$ (see Figure 4). The similarity between the switch-core and the conventional transformer suggests that the same sort of analysis might apply to both. The major obstacles to this approach are (a) the distorting effects of eddy currents on the hysteresis curve, and (b) the non-linear relation between flux and mmf as the core material moves along the path ACDE from $-\phi_r$ to $+\phi_m$. Fortunately, each of these obstacles may be bypassed without too much difficulty.

The first we may dispose of by noting that the volume resistivities of the ferrites are extremely high compared to those of the metallic ribbons. This so restricts the flow of eddy currents that their effects, to a first approximation, may be neglected in ferritic cores. If we further assume that the magnetizing component of the primary current is small compared to the load component, then the instantaneous operating point in the flux-mmf plane may be determined by entering Figure 4 along

$$(NI)_{net} = N_1 I_1 - N_2 I_2. \qquad (3.1)$$

In doing so, one must bear in mind the magnetic history of the core.

3.01 Linear Analysis of the Coupled-Circuit Problem (Cont.)

Replacing the non-linear flux-mmf relation by one which is linear may be justified on the following basis. Preliminary investigation of switching time as a function of the amplitude of the net driving mmf has indicated that, if enough mmf has been applied to drive a ferritic core beyond the second "knee" of the hysteresis loop, there are only small decreases in switching time and small increases in peak secondary current with increasing mmf. This behavior was observed over a range of net mmfs of $2 \leq H_{net} \leq 14$ oersteds in three MF-1131 (F262) cores (for which the coercive force is about one oersted). This anomalous behavior with respect to switching time was observed under the conditions of an essentially constant load (Z-plane winding plus 0.5 ohms) and of constant rise-time (about 0.8 μsec) of the primary current pulse. If these facts are corroborated by further experiments, then there appears to be little reason for driving the core far into saturation since this will cost heavily in large vacuum-tube drivers, yet will buy little. If, on the basis of these considerations, the switch core is operated so as to minimize driver requirements (and at small attendant loss in efficiency of utilization), then we may replace the actual core by the ideal one shown in Figure 4. For our purposes we require that the slopes in the saturated regions be small (not necessarily zero as shown) compared to those in the unsaturated regions.

To recapitulate, our basic assumptions are:

(a) Eddy currents negligible,

(b) Linear flux-mmf relation, and

(c) Magnetizing current small.

To these we add, for simplicity of analysis only,

(d) Capacitive effects negligible.

(e) Winding resistances negligible.

It will now be shown that a fairly good correlation exists between the experimental results and those derived from a linear analysis based on these assumptions.

Referring to the iron-core coupled circuit of Figure 6, we can write the following voltage equations:

$$\left.\begin{aligned} e(t) &= R_s i_1 + L_1 \frac{di_1}{dt} - M \frac{di_2}{dt} \\ 0 &= -M \frac{di_1}{dt} + L_2 \frac{di_2}{dt} + R_L i_2 \end{aligned}\right\} \qquad (3.2)$$

Laplace-transforming these equations, we obtain (if initial conditions are zero):

$$\left.\begin{aligned} E(s) &= (R_s + sL_1) I_1(s) - sMI_2(s) \\ 0 &= -sM I_1(s) + (R_L + sL_2) I_2(s) \end{aligned}\right\} \qquad (3.3)$$

3.01 Linear Analysis of the Coupled-Circuit Problem (Cont.)

From the second of equations 3.3, we see that the relation between loop currents is

$$\frac{I_2(s)}{I_1(s)} = \frac{sM}{sL_2 + R_L} \tag{3.4}$$

If leakage flux is small, then the self-inductance of a winding on a toroid may be written as:

$$L = \frac{2\mu_d A}{r} N^2 = K_1 N^2 \tag{3.5}$$

where $\mu_d = \frac{dB}{dH}$ = differential permeability

r = mean radius of toroid

A = cross-sectional area of toroid

N = number of turns in winding.

Similarly, the mutual inductance between windings 1 and 2 of a transformer is

$$M_{12} = \frac{2\mu_d A^*}{r^*} N_1 N_2 = kK_1 N_1 N_2 \tag{3.6}$$

where k = coefficient of coupling

Substituting these expressions into equation 3.4, we obtain

$$\frac{I_2(s)}{I_1(s)} = \frac{skK_1 N_1 N_2}{sK_1 N_2^2 + R_L} \tag{3.7a}$$

For $R_L \ll sL_2$

$$\frac{I_2(s)}{I_1(s)} \approx \frac{skK_1 N_1 N_2}{sK_1 N_2^2} = \frac{kN_1}{N_2} \tag{3.7b}$$

and for $R_L \gg sL_2$

$$\frac{I_2(s)}{I_1(s)} \approx \frac{skK_1 N_1 N_2}{R_L} = kK_2 N_1 N_2 \tag{3.7c}$$

Note that equation 3.7b may also be derived by summing mmfs around the closed magnetic loop of the toroid. If exciting current is small and the core is operated in the linear unsaturated region of the hysteresis curve, then equation 3.1 becomes

$$(NI)_{net} = N_1 I_1 - N_2 I_2 \approx 0$$

3.01 Linear Analysis of the Coupled-Circuit Problem (Cont.)

When the core is driven into saturation the net mmf will be non-zero and positive.

In order to apply the approximate equations 3.7b and 3.7c to the analysis of the experimental curves, one must know the magnitudes of the impedances of the load and of the secondary winding of the switch core. As previously indicated the load appears to be one ohm in series with two microhenries. To this we now add the 1/2 ohm current-measuring resistor. For the frequency corresponding to a rise-time of 0.3 microseconds, the impedance of the load is

$$Z_L = \sqrt{(X_L)^2 + (R_L)^2}$$
$$= \sqrt{(10.45)^2 + (1.5)^2} \approx 10.5 \text{ ohms}$$

It will later be shown that, to a reasonable approximation, the self-inductance of the secondary is

$$L_2 = K_1 N_2^2 = 2.52 N_2^2 \text{ microhenries}$$

For the same frequency the load and secondary impedances will be equal when

$$N_2^2 = \frac{Z_L}{\omega K_1} = \frac{10.5}{13.1}$$

or $N_2 \approx 1$ turn.

In order to define regions of N_2 in which equations 3.7b and 3.7c are separately valid, we shall arbitrarily set the dividing lines as

$Z_2 \ll Z_L$, when $N_2 \leq 1$ turn

$Z_2 \gg Z_L$, when $N_2 \geq 4$ turns.

3.02 Interpretation of Data

With the aid of these approximate equations, we now attempt to predict what the experimental results depicted in Graph I* should be. There the peak secondary current (I_2) is plotted as a function of secondary turns (N_2) with primary current (I_1) constant and various values of primary turns (N_1). For N_2 small, equation 3.7c predicts (under these conditions) that

$$I_2 = (kK_2 N_1 I_1) N_2$$
$$= K_a N_2 ;$$

* All graphs appear in sequence following Figure 8.

3.02 Interpretation of Data (Cont.)

while for N_2 large, equation 3.7b predicts that

$$I_2 = \frac{kN_1 I_1}{N_2} = \frac{K_b}{N_2}$$

The composite curve for Graph I should, as does Figure 7, show

(a) for small N_2, a linear relationship between I_2 and N_2,

(b) for large N_2, a hyperbolic relationship,

(c) for intermediate N_2, a compromise relationship as the two curves of a. and b. fair together.

Examination of Graph I shows that the experimental curves do indeed bear a marked resemblance to the composite curve for Figure 7. Since the leakage inductance and shunt capacitance increases with the number of turns in the winding, one should expect deviations of the actual from the theoretical results to increase with increasing N_1 and/or N_2. Although this fact is evident in Graph I, it is displayed even more conspicuously in Graphs II and III.

In the first is shown a plot of peak secondary current I_2 versus N_1 with I_1 constant and various values of N_2. From equation 3.7b

$$I_2 = \frac{kI_1}{N_2} N_1 = K_c N_1 \quad \text{(for a given } N_2\text{)}$$

is the theoretical relation between I_2 and N_1. Since the families of curves in Graph II involve $N_2 > 4$ turns, this relation would hold were it not for the increase in leakage with increasing primary turns.

In Graph III a different aspect of the same data is shown. There is a plot of I_2 versus N_2 with I_1 constant and various values of the turns ratio -- $a = N_1 : N_2$.

For $Z_L \gg sL_2$ equation 3.7c gives

$$I_2 = kK_2 I_1 N_1 N_2 = \left(kK_2 I_1 \frac{N_1}{N_2}\right) N_2^2 = K_d N_2^2 \quad \text{for a given } \frac{N_1}{N_2},$$

3.02 Interpretation of Data (Cont.)

and for $Z_L \ll sL_2$ equation 3.7b gives

$$I_2 = \frac{kN_1}{N_2} I_1$$

$$= K_e \quad \text{for a given } \frac{N_1}{N_2} .$$

Although insufficient data was collected to check the parabolic relation for small N_2, the second relation between I_2 and N_2 may be observed. However, only over a limited region is the secondary current independent of secondary turns; only for small values of the turns ratio is there any good correspondence between the actual and the theoretical curves.

Graph IV illustrates the fact that the net driving ampere-turns is non-zero when the core is driven into saturation. For the MF-1131 (F262) core, an $(NI)_{net}$ of three ampere-turns suffices to drive the core from the remanent state at $-\phi_r$ to that of positive saturation at $+\phi_m$. The importance of this variable stems from the fact that, for the ferritic core, it determines the degree of switching.

Before interpreting the data for the three selected switch-core transformers, it is necessary that we derive a few more relations. Noting that both N_1 and N_2 are greater than four, one would expect that equation 3.7b would govern the relation between I_2 and I_1 so long as the core is not driven to saturation. In the saturated region, a different relation should be expected since in that region the two windings of the core are virtually decoupled. Referring to the usual definition of the coefficient of coupling, we see that

$$k = \frac{M}{\sqrt{L_1 L_2}} \qquad (3.8)$$

In the unsaturated region, equation 3.7b states

$$\frac{I_2}{I_1} = \frac{M}{L_2}$$

$$= \frac{k\sqrt{L_1 L_2}}{L_2}$$

$$= k \frac{N_1}{N_2} = ka$$

or

$$k = \frac{N_2 I_2}{N_1 I_1} \qquad (3.9)$$

3.02 Interpretation of Data (Cont.)

A first-order approximation one might make is that the behavior of the core is governed by two linear relations between I_2 and I_1 -- one holding when the core is unsaturated; the second, when saturated. The transfer characteristic, $i_2(t) : i_1(t)$ of the core (with "many" turns) might then be represented by the polygonal line shown in Figure 8. For I_1 less than that required for saturation (with a given N_1), the characteristic is a straight line with slope $\underline{k_\alpha a}$ where $k_\alpha \approx 0.95$; while for I_1 sufficient for saturation, one with slope $\underline{k_\beta a}$ where $k_\beta \approx 0.05$.

At this point we may remark that the polygonal line of Figure 8 does resemble the curves of the average plate characteristics of a pentode. It was this resemblance that prompted D. A. Buck to suggest that one might utilize this characteristic in developing a magnetic-core constant-current generator.

Referring now to equation 3.1 we see that this may be written

$$(NI)_{net} = (1 - k_\beta) N_1 I_1 \qquad (3.1a)$$

when the core material is saturated. Thus for a given value of N_1, there should be a linear relation between the net driving mmf and the primary current.

Applying the analytic relations to the experimental curves of Graphs V and VI, we note that these show plots of I_2 and of $(NI)_{net}$, respectively, as functions of I_1 for the selected combinations of N_1 and N_2. In the first graph, the actual and the ideal curves very nearly coincide over a limited range of I_1. In this region, the coefficient of coupling is approximately unity. For the turns used, $\underline{k_\alpha}$ varies between 0.94 and 0.99. When the core is driven into saturation however, $\underline{I_2}$ increases very slightly with increasing I_1. In this region, where the two windings are nearly independent of each other, the coefficient of coupling is nearly zero. The experimental data indicates that $\underline{k_\beta}$ is no greater than 0.075 for any of the turns used.

Graph VI also shows close agreement between theoretical and experimental results. Each of the three cores shows a linear relation between the net driving mmf and primary current when the core material is in a saturated state. If these lines are extrapolated linearly to the zero I_1 axis, they appear to intersect at a common point: --at $(NI)_{net} = -N_2 I_2 \approx -15$ ampere-turns.

With this background of the behavior of saturable-core transformers with "many" turns, we can now examine the case with "few" turns. Since construction of a matrix switch is greatly simplified when the core elements have windings with relatively few turns, it is important to determine whether such a switch will work and, if so, what constraints are imposed on the vacuum tube drivers by going to "few" turns. The investigations in the second of our three sets of experiments were meant to provide some of the answers to these questions.

3.02 Interpretation of Data (Cont.)

Since it is neither desirable nor necessary to present all of the data collected, we include only that portion which will indicate trends. Thus, in Graphs VII and IX are shown plots of peak secondary current versus secondary turns and primary current respectively, when primary turns are held constant at $N_1 = 4$ turns; while in Graphs VIII and X are shown the same plots for $N_1 = 8$ turns.

From Graphs VII and VIII, we see that the forms of the curves are similar to those predictable from equations 3.7b and 3.7c. However, we note that rather heavy currents are required from the v.t. drivers preceding the cores if we are to have appreciable output current. Instead of the 400 milliamperes primary current which sufficed in the earlier experiments, we now require that the v.t. driver supply currents of the order of amperes.

In Graphs IX and X we observe that, although a linear relation still exists between I_2 and I_1, there are serious discrepancies between the actual and the ideal curves. These discrepancies decrease as either N_1 or N_2 are increased. It should be noted that by "ideal" we mean that equation 3.7b holds between I_2 and I_1. The actual data conforms more nearly to that of equation 3.7c.

The discrepancies noted thus far are brought home even more forcibly by Graphs XI and XII. There are depicted plots of I_2 versus I_1 with N_2 held constant and various values of turns ratios. In the first we see the case when $N_2 = 1$ turn; in the second, $N_2 = 4$ turns. From these it is apparent that going to few turns per winding results in a gain in simplicity of construction at the expense of a loss in effectiveness as a transformer.

The last set of experiments, involving static hysteresis loop measurements, derives its importance from the fact that this loop indicates the path of state of the material in the absence of eddy currents. To facilitate analysis, we might replace the actual "half-loop" (from the remanent flux density at $-B_r$ to positive saturation at $+B_m$) by a polygonal line of three segments. The first, at $H = 0$, has a slope

$$\mu_1 = \left.\frac{dB}{dH}\right|_{H=0} ;$$

The second, at $H = H_c$ (coercive force), has a slope

$$\mu_2 = \left.\frac{dB}{dH}\right|_{H=H_c} ;$$

and the third, for saturation mmf, has the same slope as at $H = 0$. Below is shown a table of typical slopes for the saturation loops of the ferritic materials under discussion.

3.02 Interpretation of Data (Cont.)

Core Material	μ_1 (gauss/oersted)	μ_2 (gauss/oersted)
MF1131(F262)	60	3000
MF1118(F259)	40	2000

The self inductance of a toroidal core is, by equation 3.5,

$$L_a = \frac{2\mu_2 A}{r} N^2 = K_1 N^2$$

For an MF-1131 (F262) core operating in the vicinity of $H = H_c$,

$\mu_2 = 3000$ gauss/oersted
$r = 0.333$ cm
$A = 0.14$ cm^2 ;

so that

$L_a = 2.52\ N^2$ microhenries.

For an MF-1118 (F259) core operating in the vicinity of $H = 0$,

$\mu_1 = 40$ gauss/oersted
$r = 0.214$ cm
$A = 0.0154$ cm^2 ;

so that

$L_b = 0.00575\ N^2$ microhenries/core

When operated in the memory array (in the mode used throughout our experiments), these memory cores are connected, all 256 in series, by a single wire. Hence the equivalent inductance of the array due to the cores alone is

$$L_{eq} = 256\ (0.00575\ \mu h/\text{core})$$
$$= 1.47\ \mu h$$

When one adds to this the leakage inductance of the wire between cores (which is probably of the order of one microhenry), one sees that this result is in good agreement with that empirically derived by W. Ogden and E. Guditz. Using inductors with nominal ratings, they matched the response of a dummy load with that of the Z-plane of the array and found that a one ohm resistor in series with a two microhenry inductor gave a good match.

4.0 Conclusions

From the results presented above, some rather important conclusions may be drawn:

(a) If ferritic core material is used for switching applications and if the core is not driven far into saturation, then the

4.0 Conclusions (Cont.)

behavior of the switch elements may be described in terms of linear coupled-circuit theory. Although a more adequate model (at pulse frequencies) should include capacitive effects, it is encouraging to observe that a rather simple model may be used to interpret experimental results.

(b) Simplicity of construction of a matrix switch can be obtained only at a loss in effectiveness of transformer action. The overriding importance of simplicity of construction may constrain the design to relatively few turns per winding (at least on the primary windings). Since the trend in memory cores is toward a smaller core body (e.g., die size F-291) with the attendant smaller current requirements, this loss in effectiveness may be one which we are willing to accept.

(c) The near absence of eddy currents suggests that the static hysteresis loop may be used to describe the path of magnetic state of the material even at pulse frequencies, and hence to facilitate the analytical work involved in a matrix switch design.

Signed: A. Katz
A. Katz

Signed: Elias A. Guditz
E. A. Guditz

Approved: WNP
W. N. Papian

AK:EAG/aik

Please attach these drawings to your copy of E-500.

"Switch-Core Analysis I" by A. Katz and A. Guditz.

Thank You.

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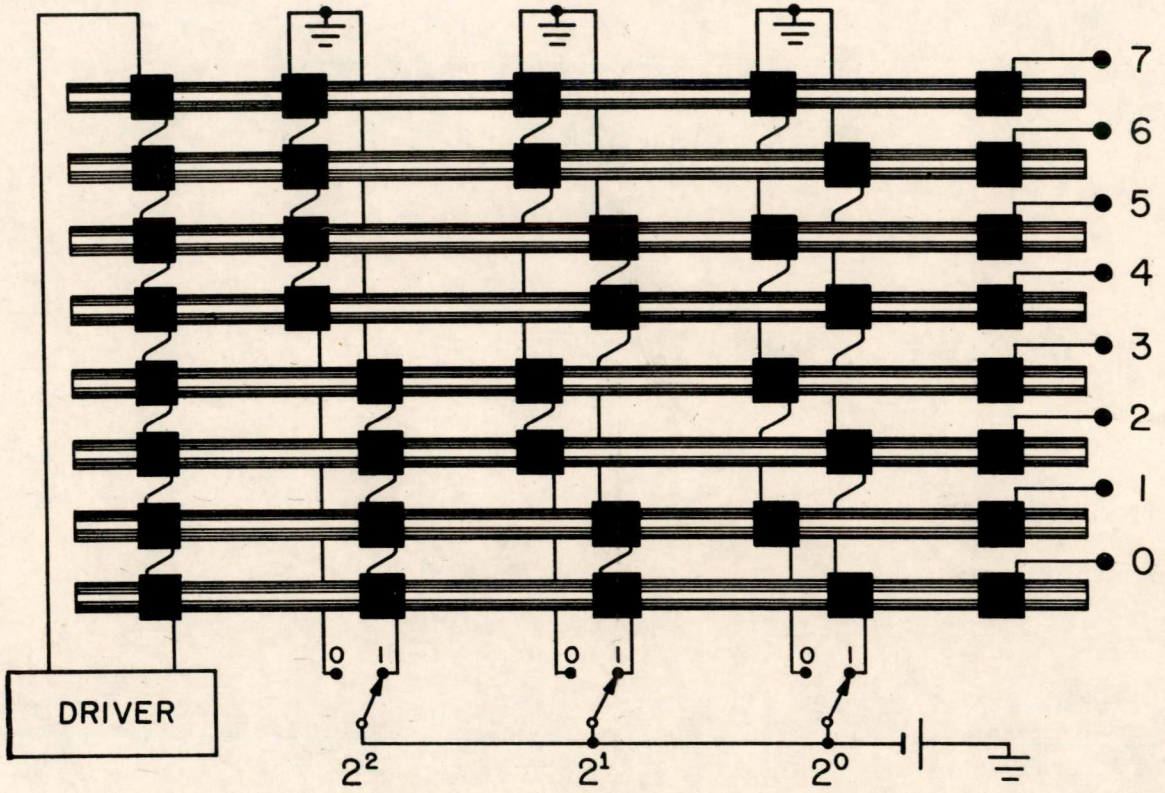


8-POSITION MAGNETIC-MATRIX SWITCH

FIG. 1

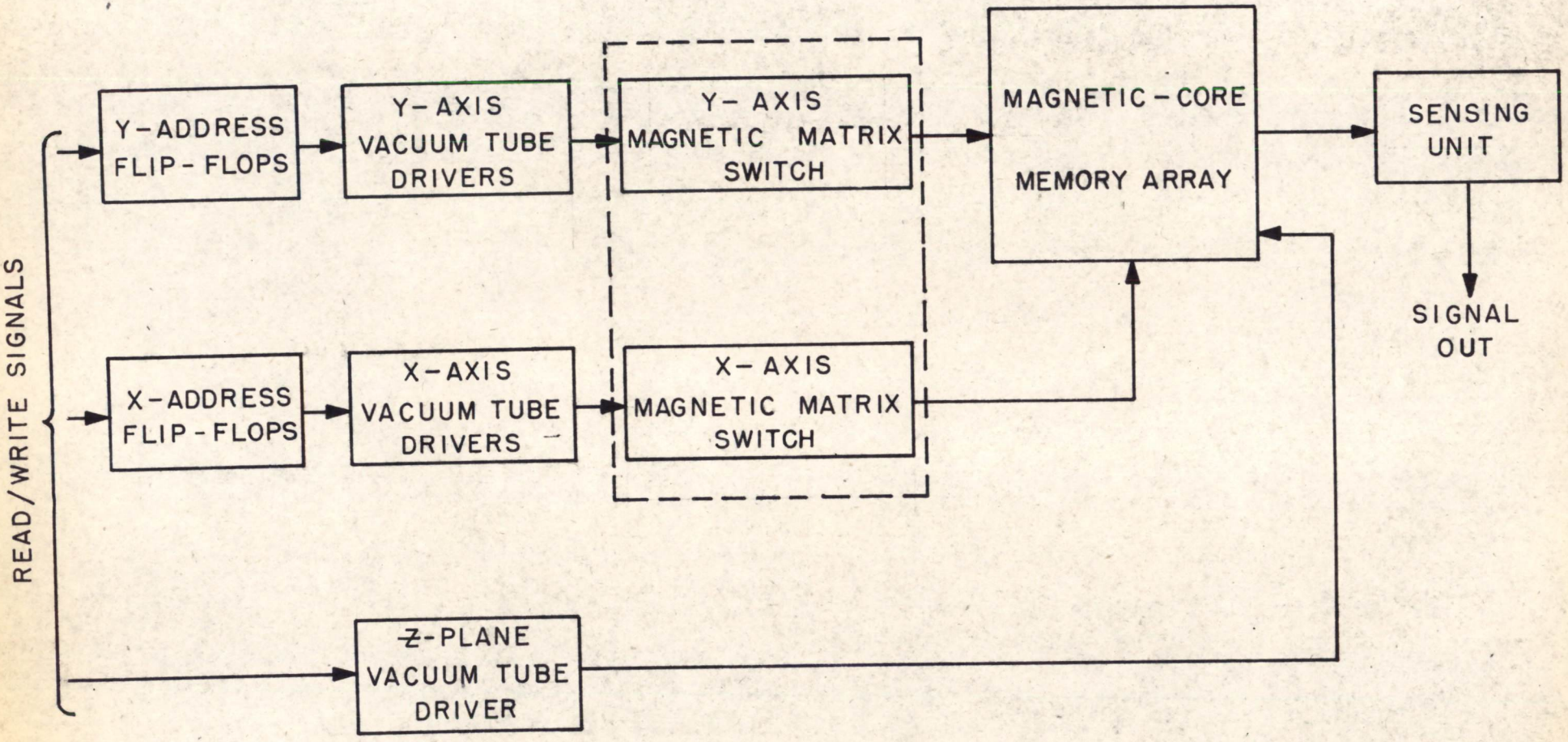


FIG. 2

A SELECTION SYSTEM FOR A MAGNETIC-CORE MEMORY ARRAY

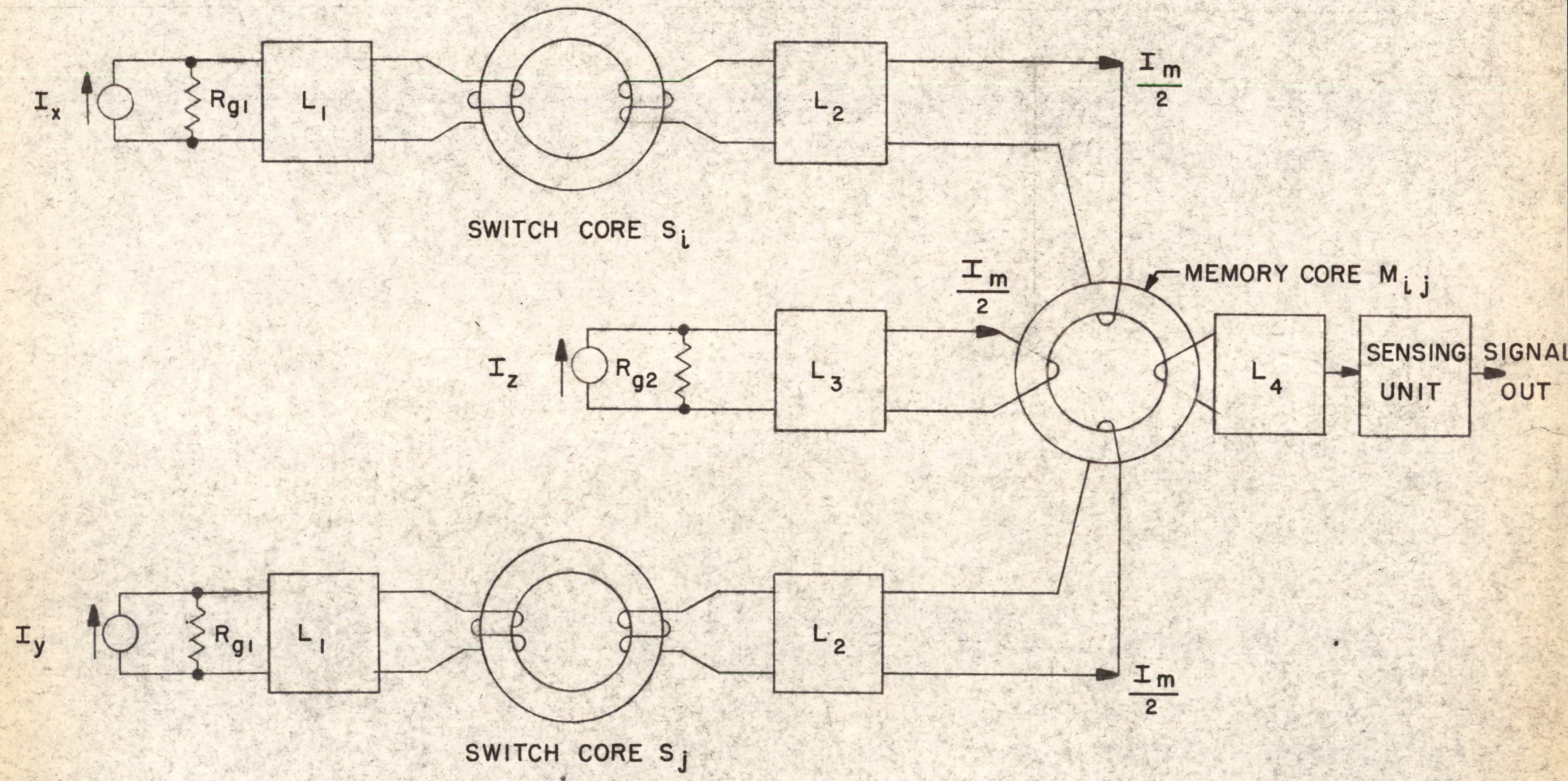
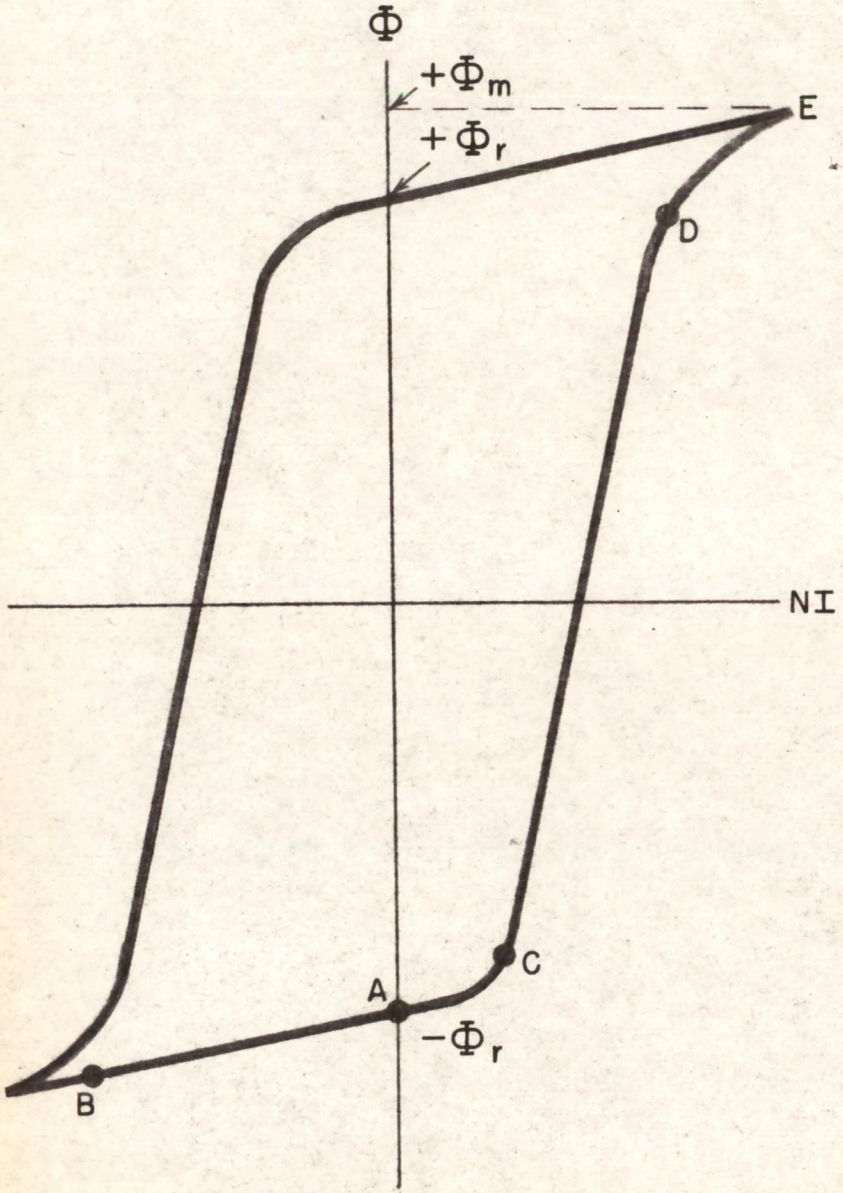
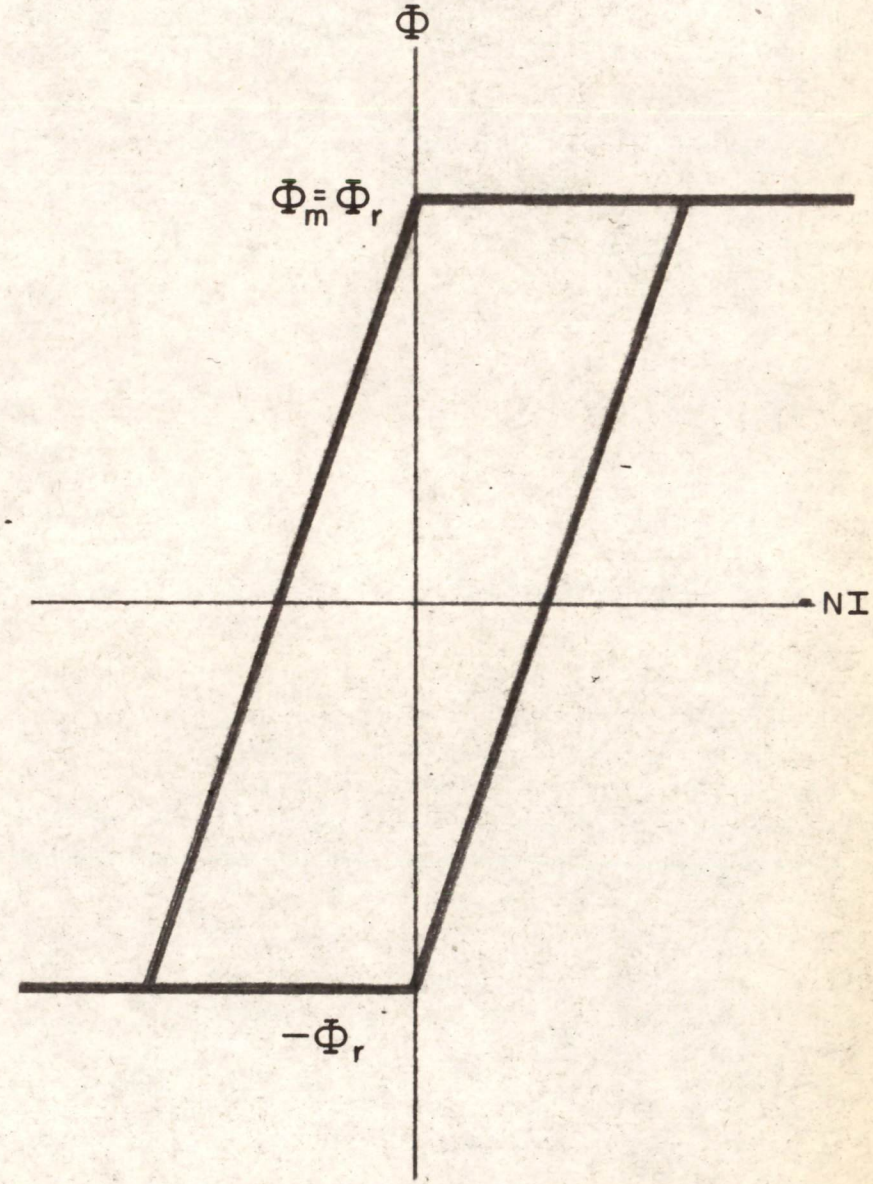


FIG. 3

ESSENTIAL ELEMENTS OF A SWITCH-CORE DRIVEN MAGNETIC MEMORY ARRAY



a) ACTUAL SWITCH CORE



b) IDEAL SWITCH CORE

FIG. 4

STATIC HYSTERESIS CURVES FOR RECTANGULAR-LOOP CORE MATERIALS

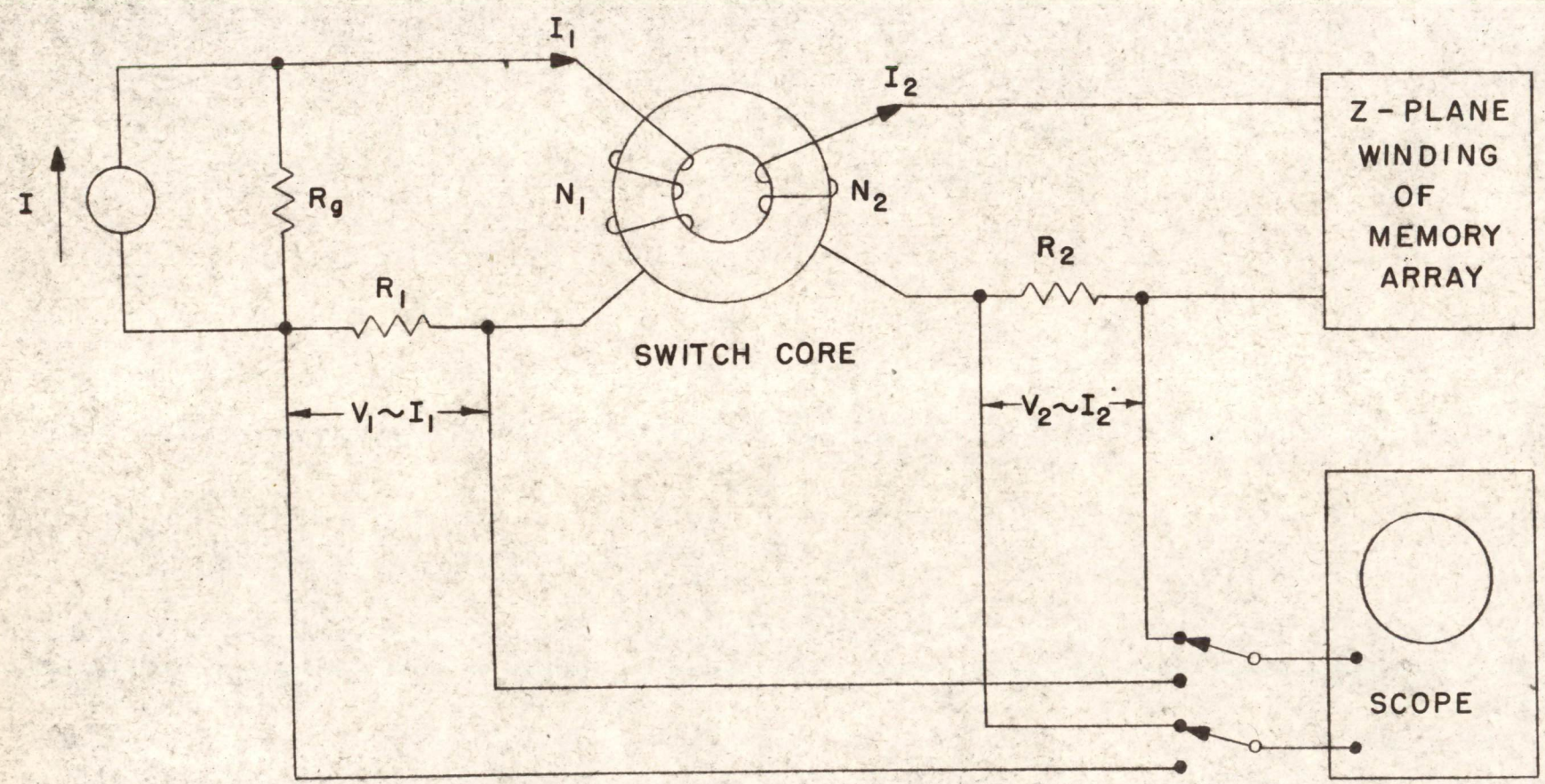
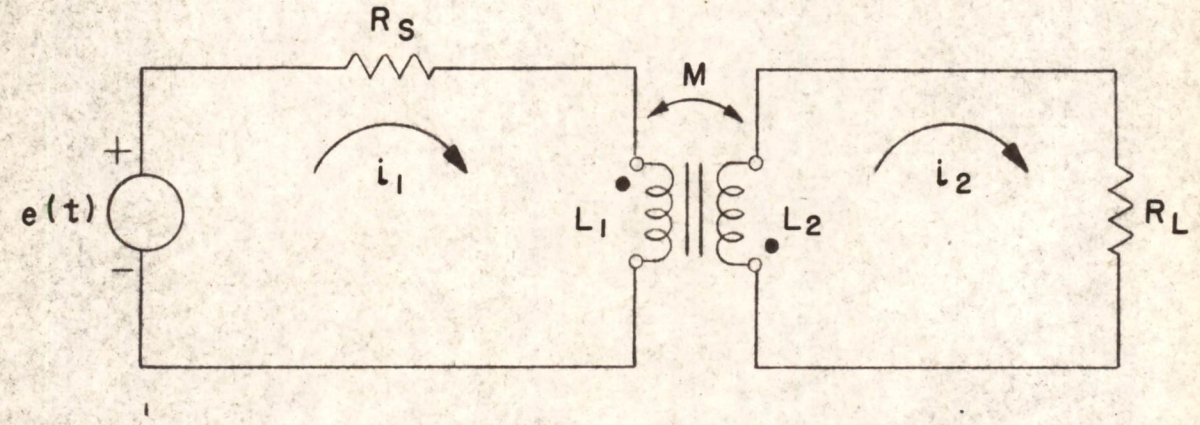


FIG. 5

TEST SET-UP FOR STUDY OF SWITCH CORES



L_1 = PRIMARY SELF-INDUCTANCE
L_2 = SECONDARY SELF-INDUCTANCE
M = MUTUAL INDUCTANCE
R_S = SOURCE RESISTANCE
R_L = LOAD RESISTANCE

FIG. 6

IRON-CORE COUPLED CIRCUIT

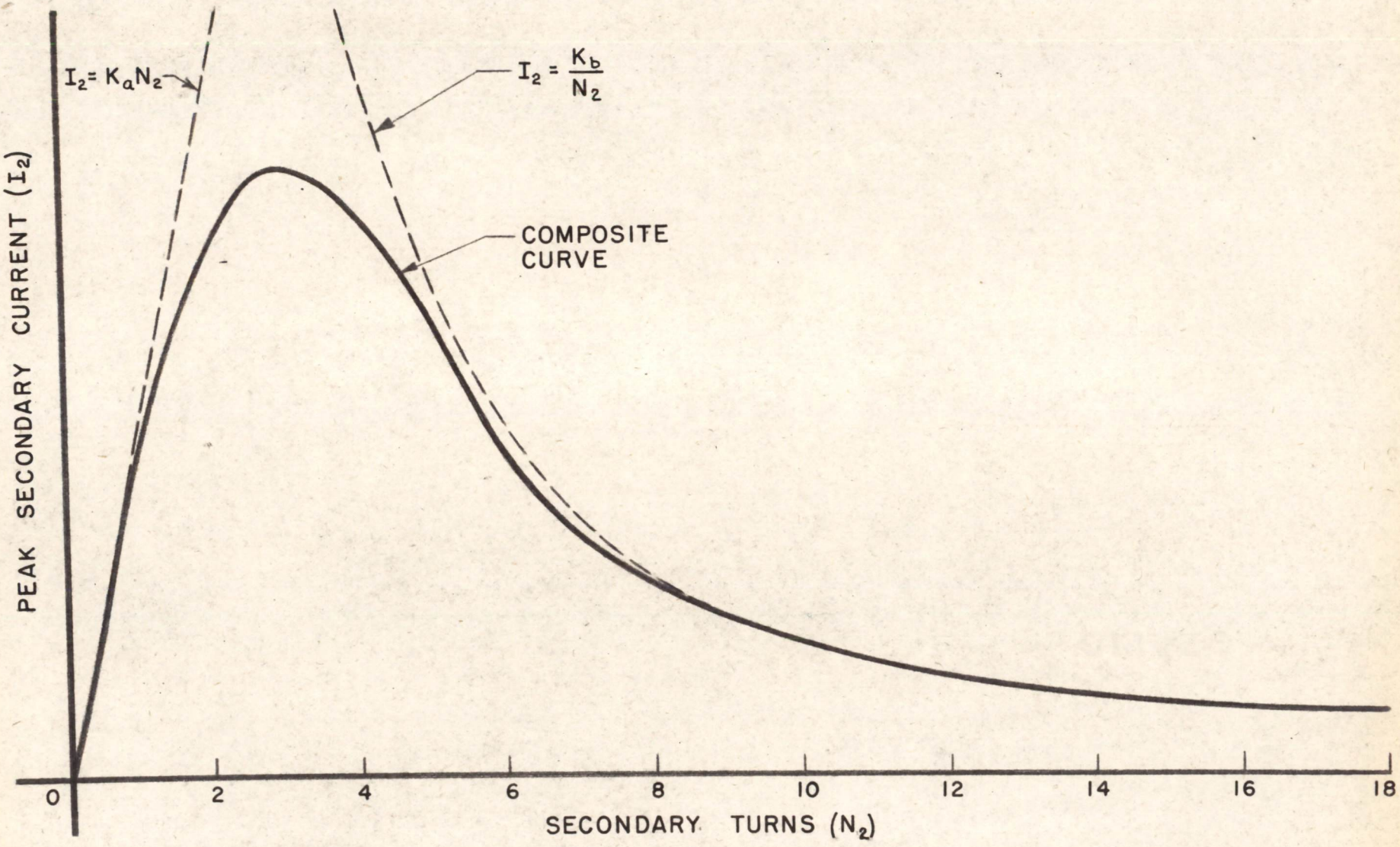


FIG. 7

PREDICTED CURVE OF PEAK SECONDARY CURRENT VERSUS SECONDARY TURNS FOR CONSTANT PRIMARY AMPERE-TURNS

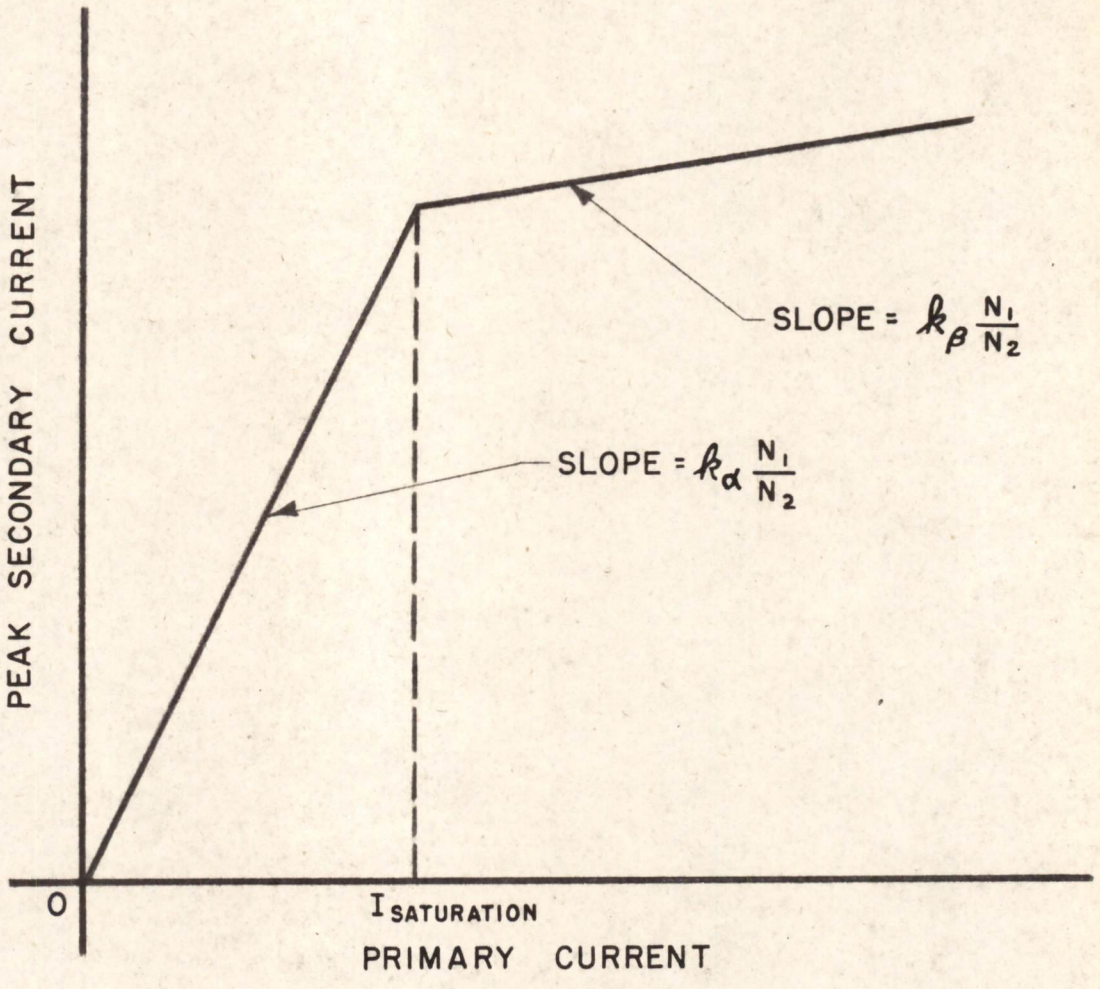


FIG. 8

APPROXIMATE TRANSFER CHARACTERISTIC FOR SWITCH-CORE WITH "MANY" TURNS

SA-48378-G

359T-6G KEUFFEL & ESSER CO.
5 × 5 to the ½ inch.
MADE IN U. S. A.

Graph I - Secondary Current as a Function of Secondary Turns with Primary Current Constant and Various Values of Primary Turns.

Core: MF1131 (F262)
I_1 = 400 ma.
Load = Z-plane + ½-Ω
Actual ———
Ideal - - - -

N_1=30
N_1=70
N_1=30
N_1=50
N_1=10

Peak Secondary Current (amp.)

1.25
1.00
0.75
0.50
0.25

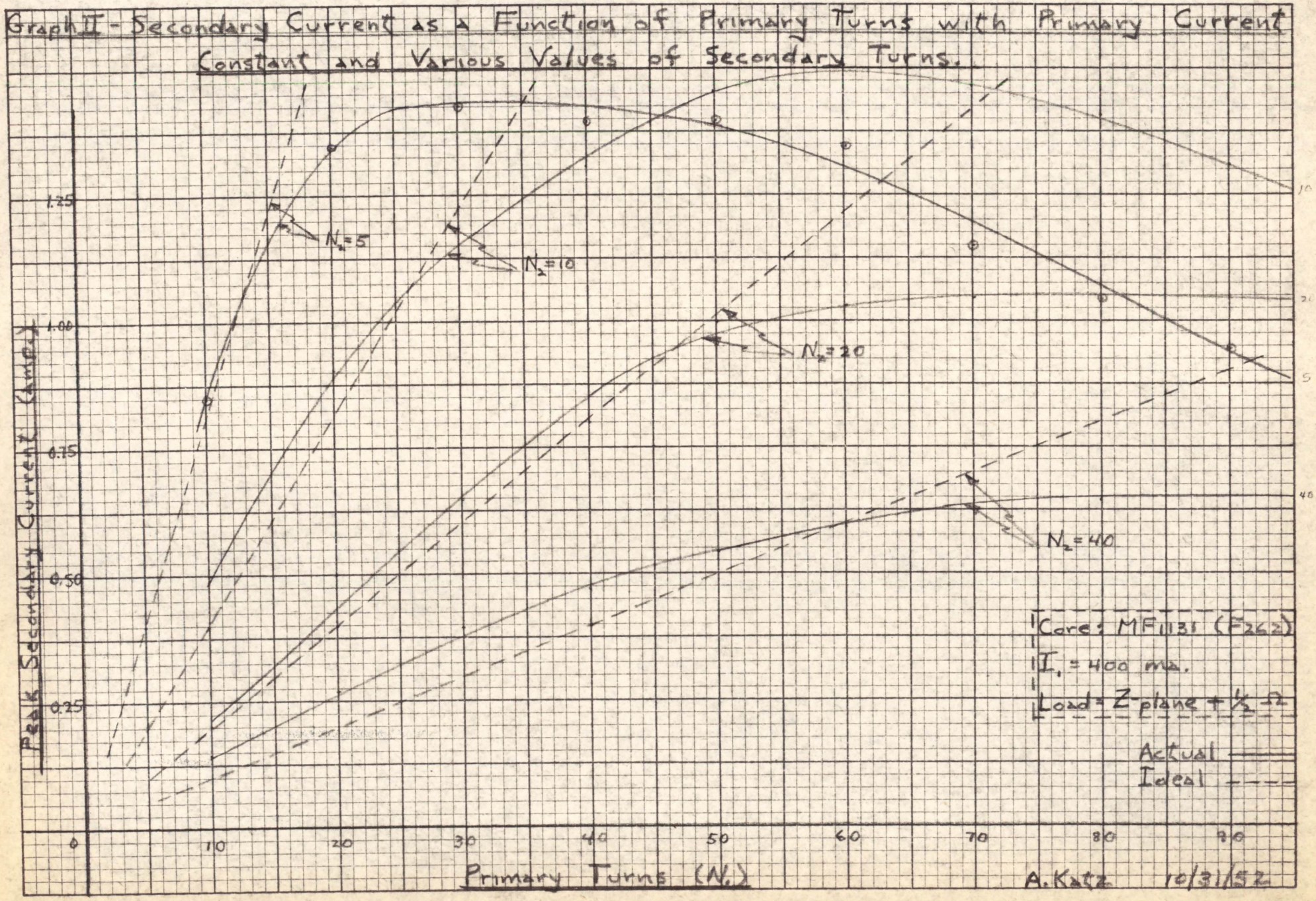
0 5 10 15 20 25 30 35 40 45

Secondary Turns (N_2)

A. Katz 10/31/52

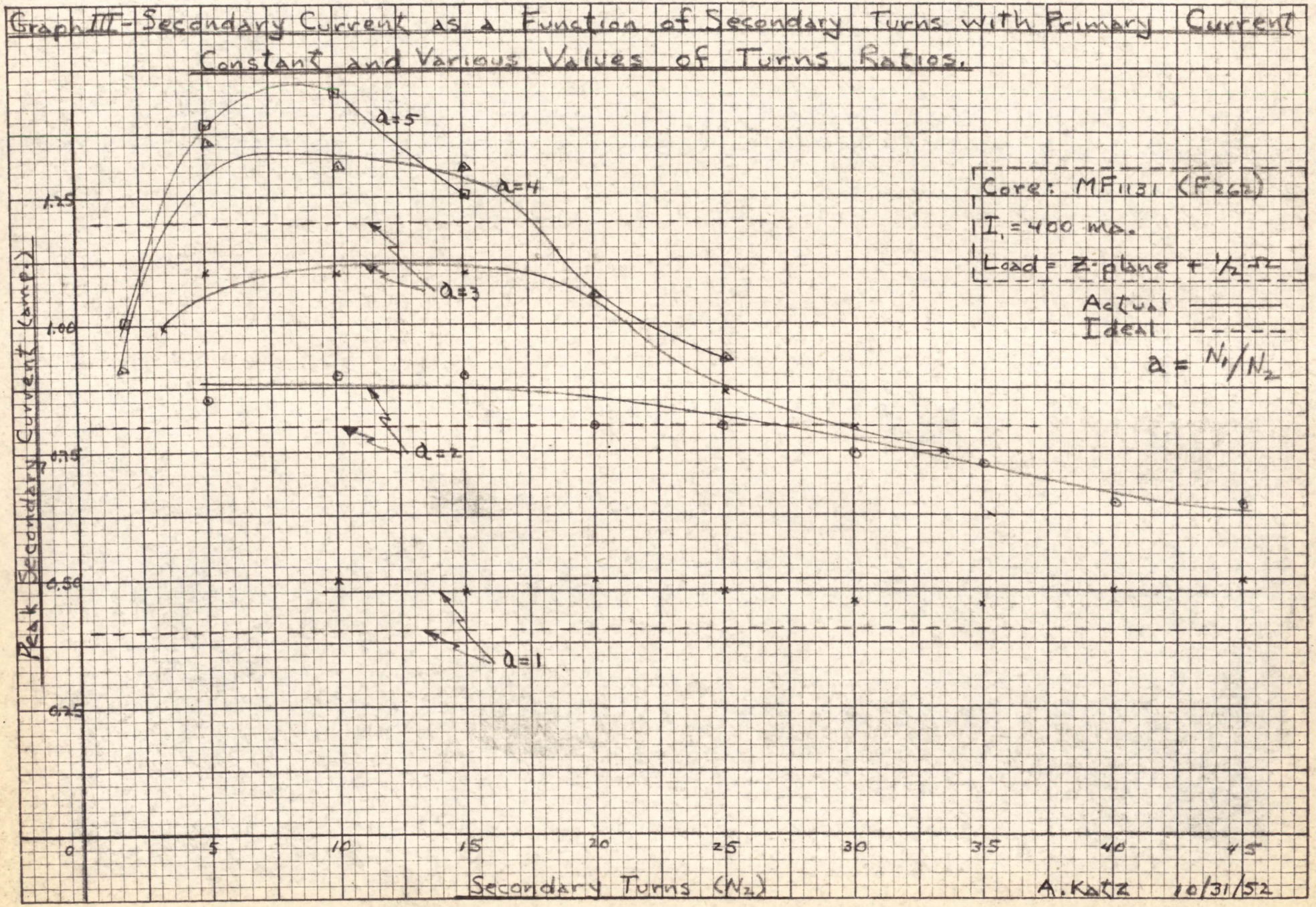
SA-48379-G

359T-6G KEUFFEL & ESSER CO.
5 × 5 to the ½ inch.
MADE IN U. S. A.



SA-48380-G

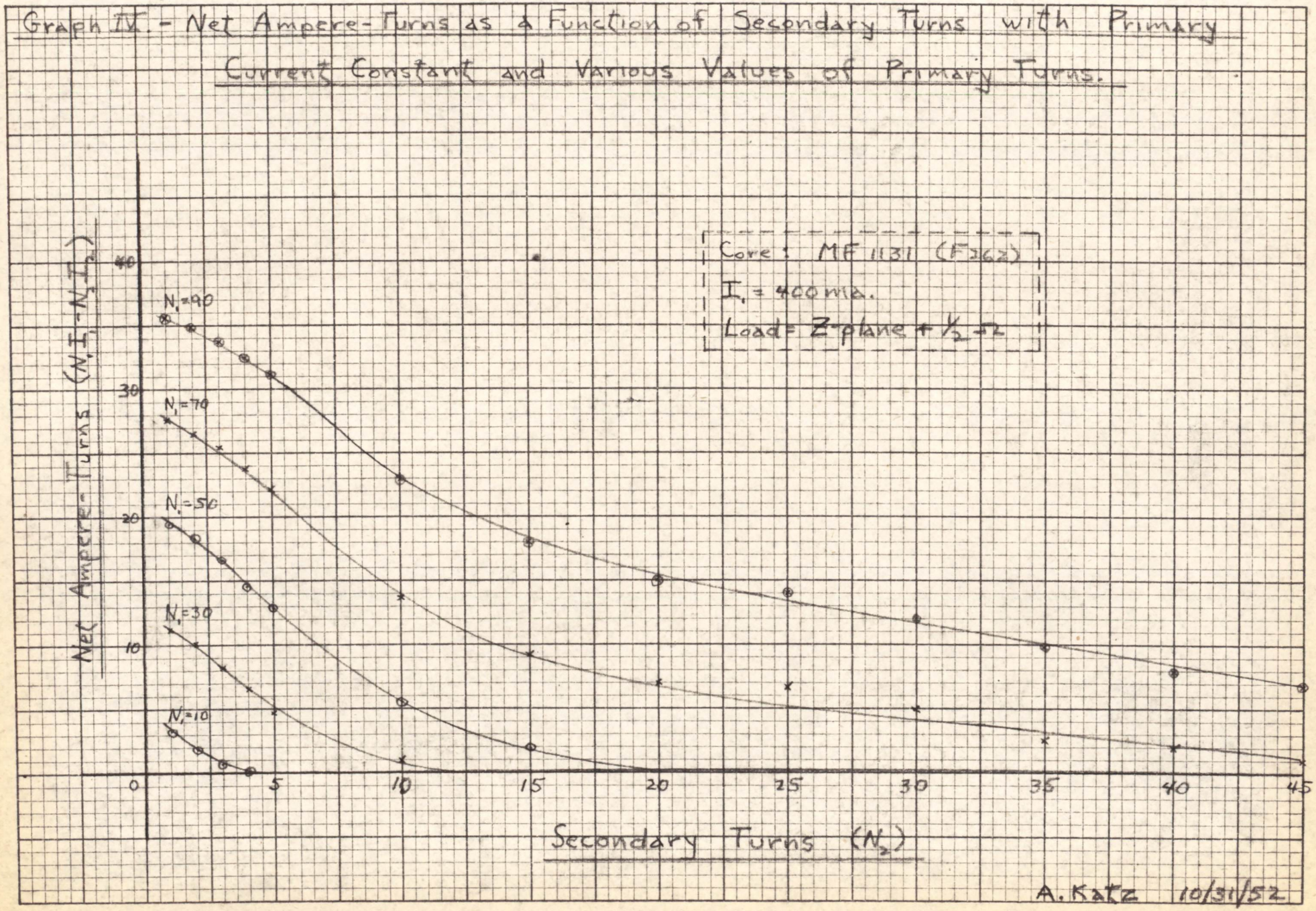
359T-6G KEUFFEL & ESSER CO.
5 × 5 to the ½ inch.
MADE IN U. S. A.



SA-48381-G

359T-6G KEUFFEL & ESSER CO.
5 × 5 to the ½ inch.
MADE IN U. S. A.

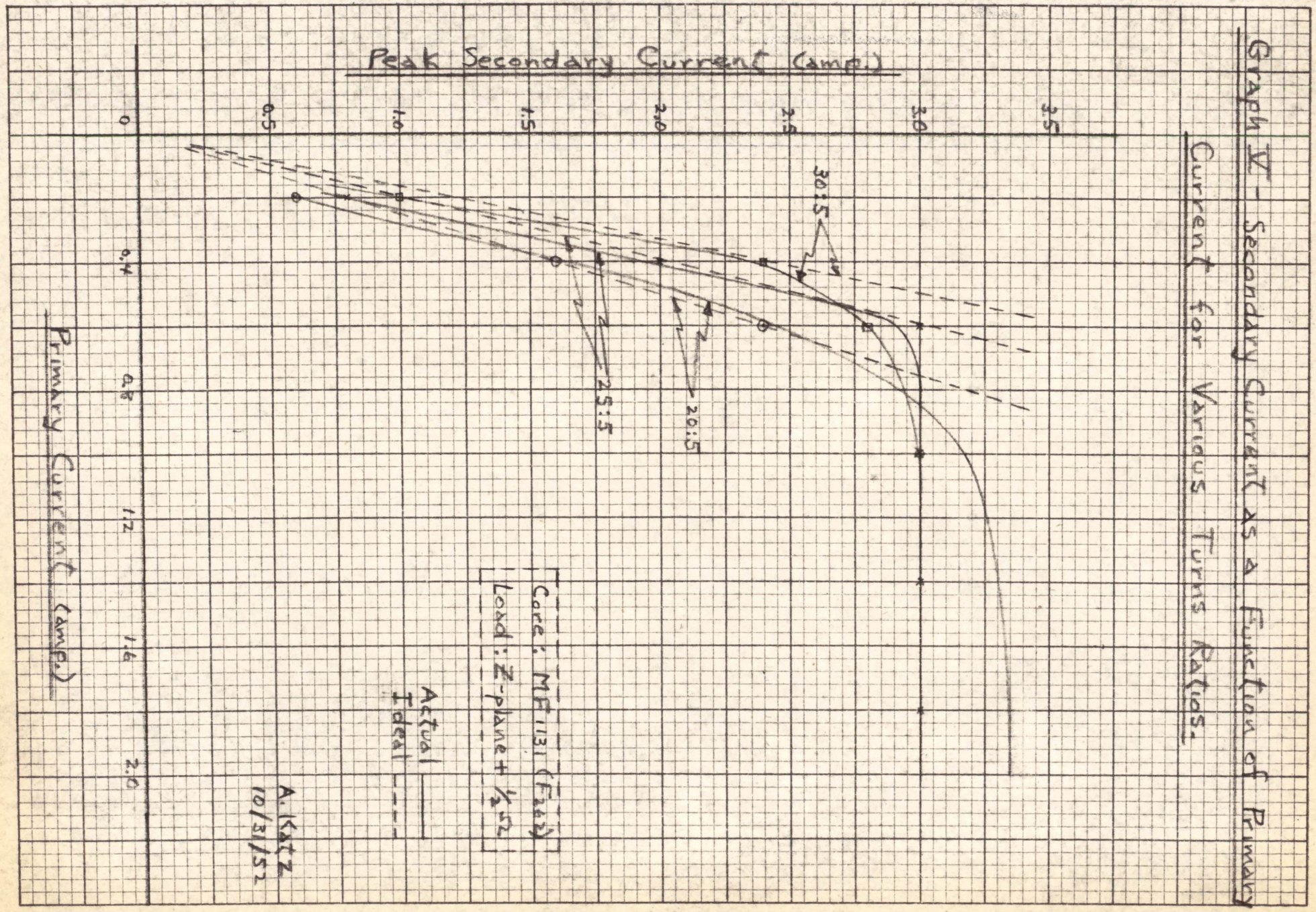
Graph IV. - Net Ampere-Turns as a Function of Secondary Turns with Primary Current Constant and Various Values of Primary Turns.



A. Katz 10/31/52

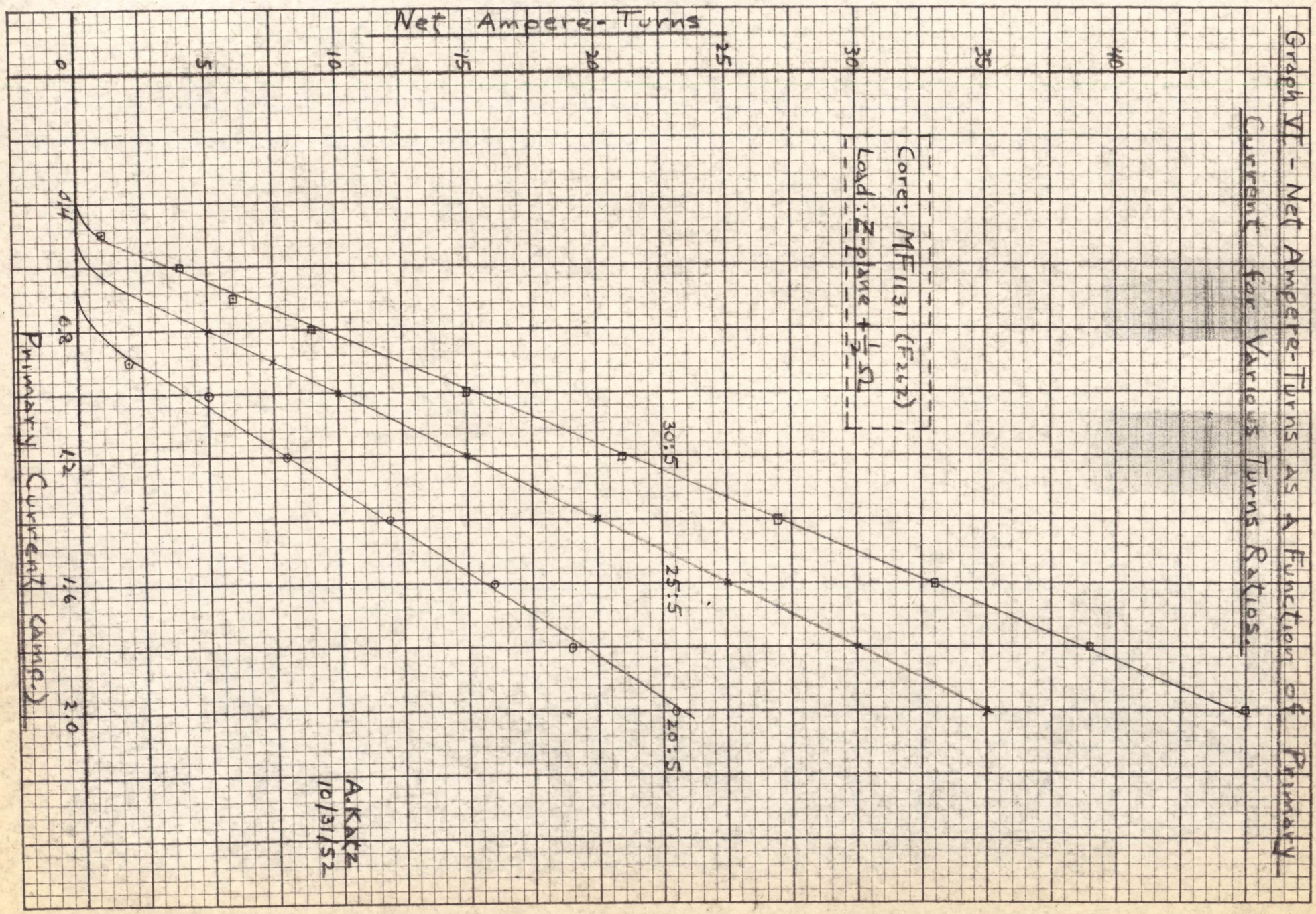
SA-48382-G

359T-6G KEUFFEL & ESSER CO.
5 × 5 to the ½ inch.
MADE IN U. S. A.



SA-48383-G

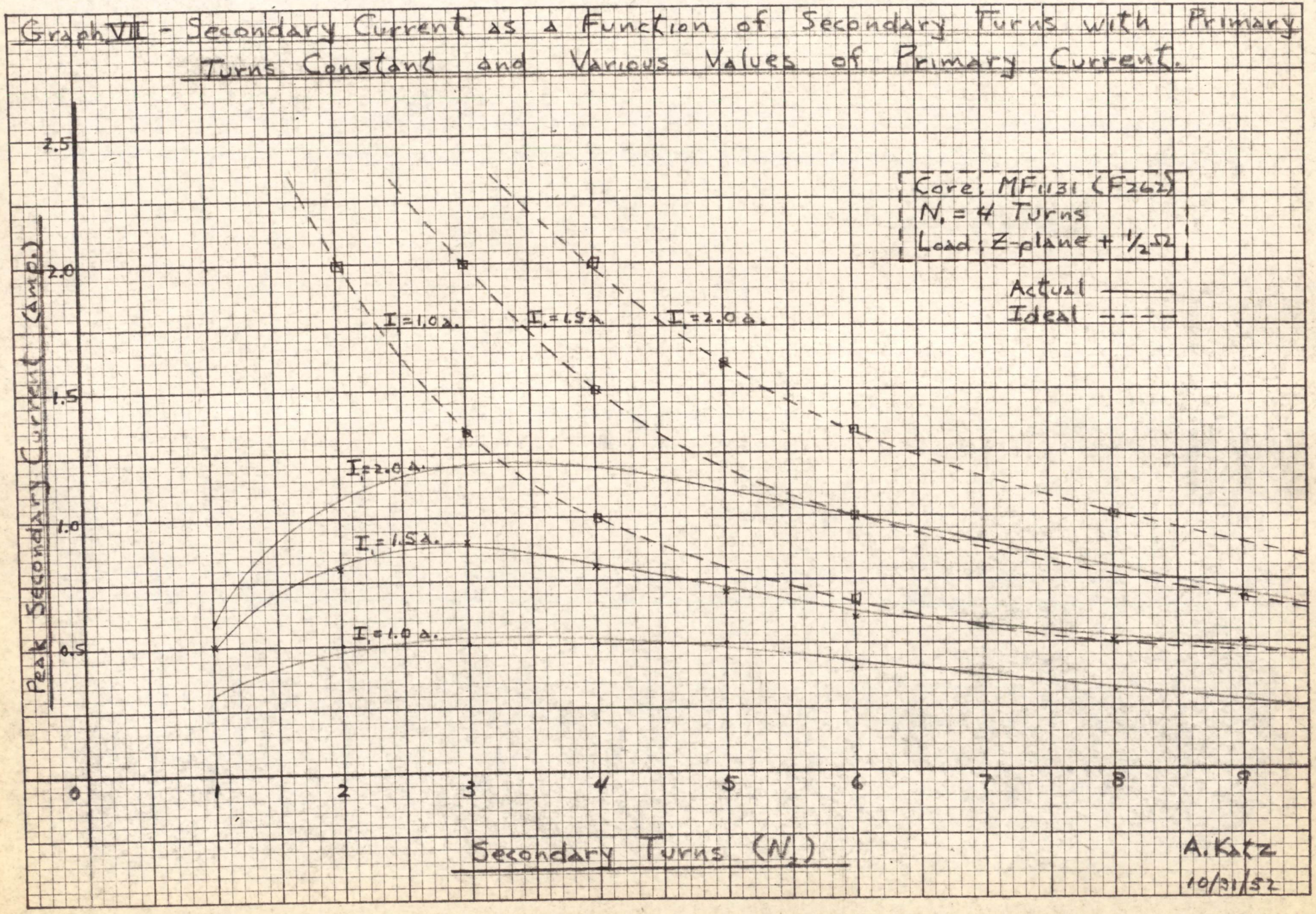
359T-6G KEUFFEL & ESSER CO.
5 × 5 to the ½ inch.
MADE IN U. S. A.



SA-48384-G

359T-6G KEUFFEL & ESSER CO.
5 × 5 to the ½ inch.
MADE IN U. S. A.

Graph VII - Secondary Current as a Function of Secondary Turns with Primary Turns Constant and Various Values of Primary Current.

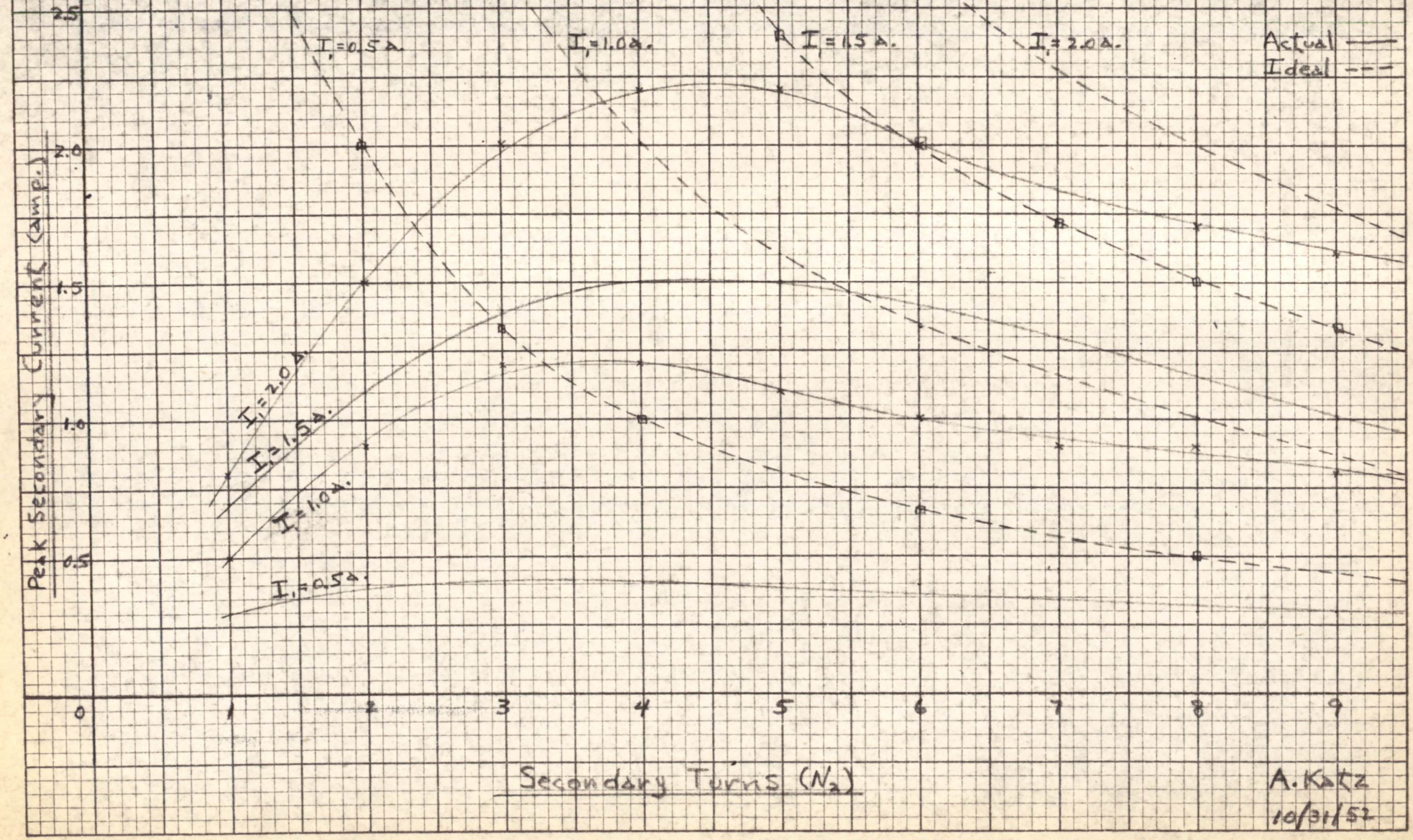


A. Katz
10/31/52

SA-48385-G

359T-6G KEUFFEL & ESSER CO.
5 × 5 to the ½ inch.
MADE IN U. S. A.

Graph VIII. - Secondary Current as a Function of Secondary Turns with Primary Turns Constant ($N_1 = 8$), and Various Values of Primary Current.

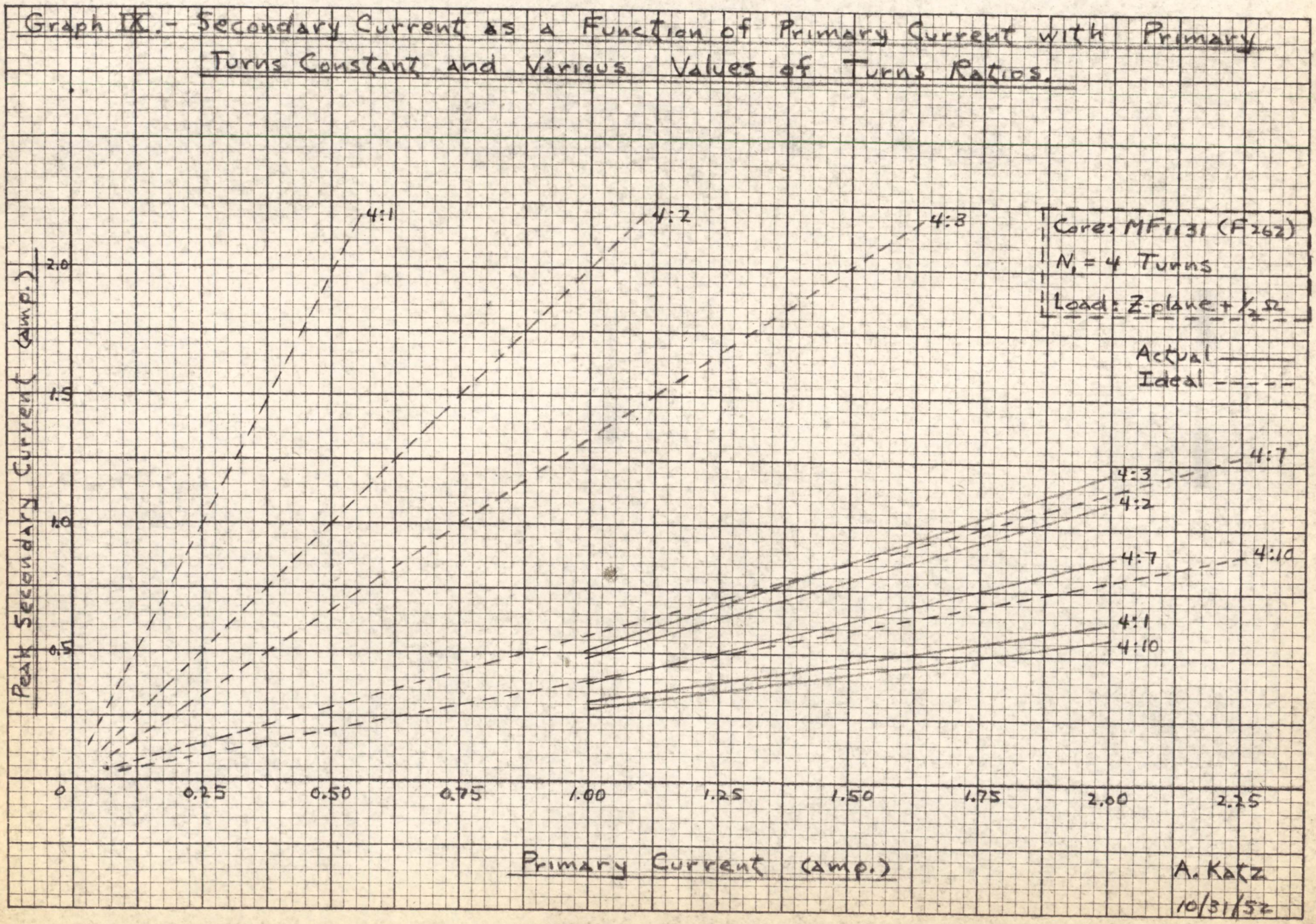


A. Katz
10/31/52

SA-48386-G

359T-6G KEUFFEL & ESSER CO.
5 × 5 to the ½ inch.
MADE IN U. S. A.

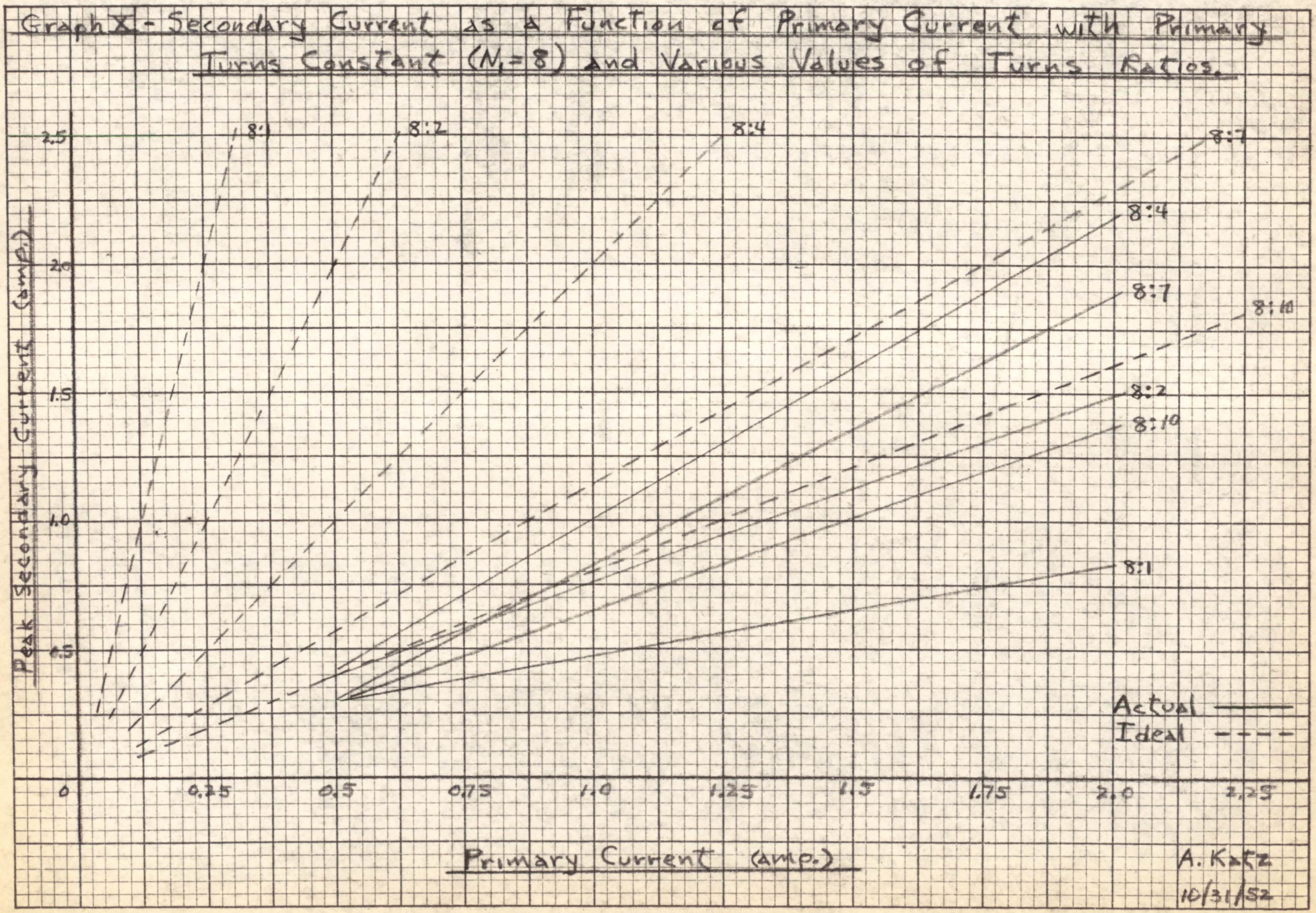
Graph IX.- Secondary Current as a Function of Primary Current with Primary Turns Constant and Various Values of Turns Ratios.



A. Katz
10/31/52

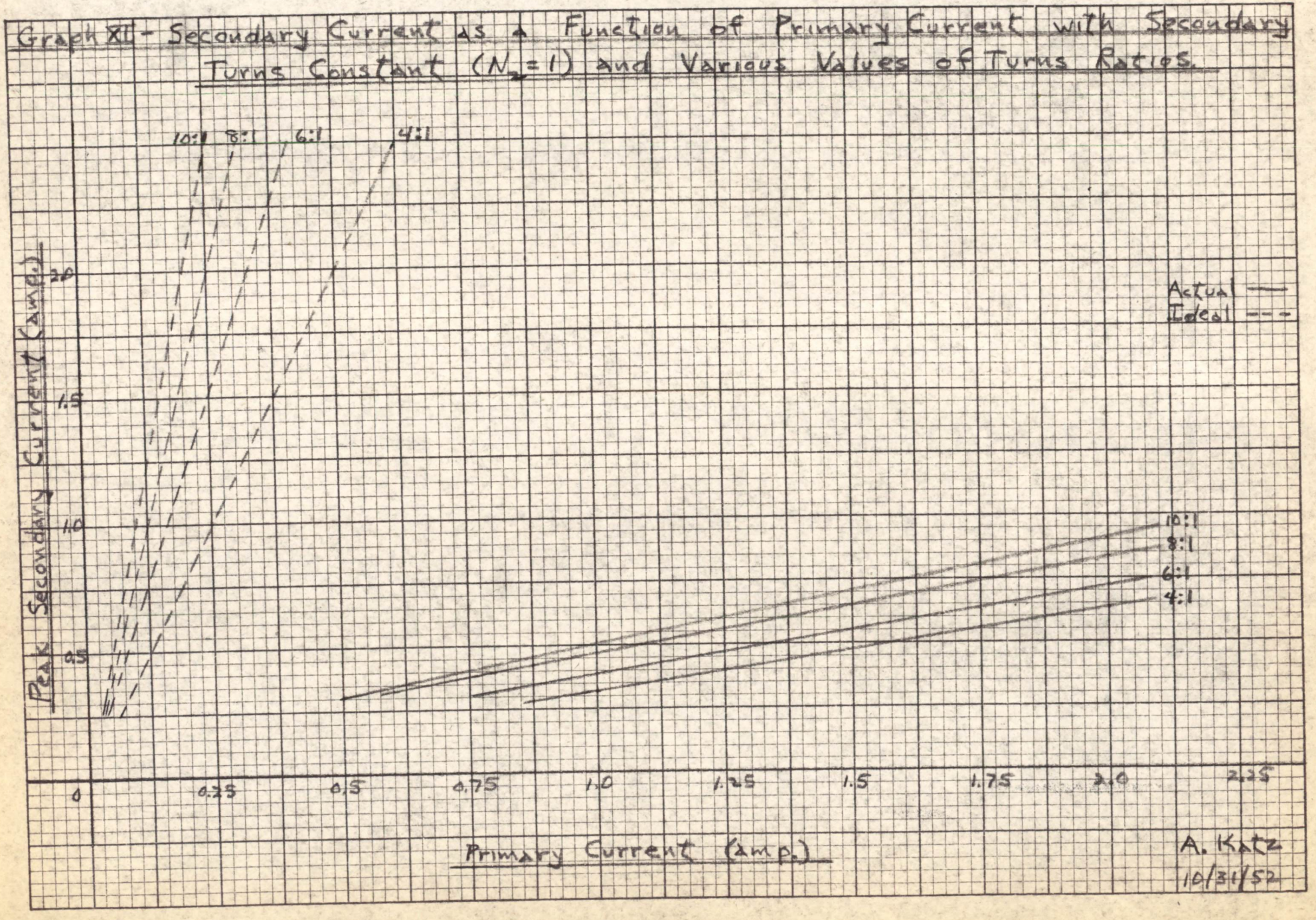
SA-48387-G

359T-6G KEUFFEL & ESSER CO.
5 × 5 to the ½ inch.
MADE IN U. S. A.



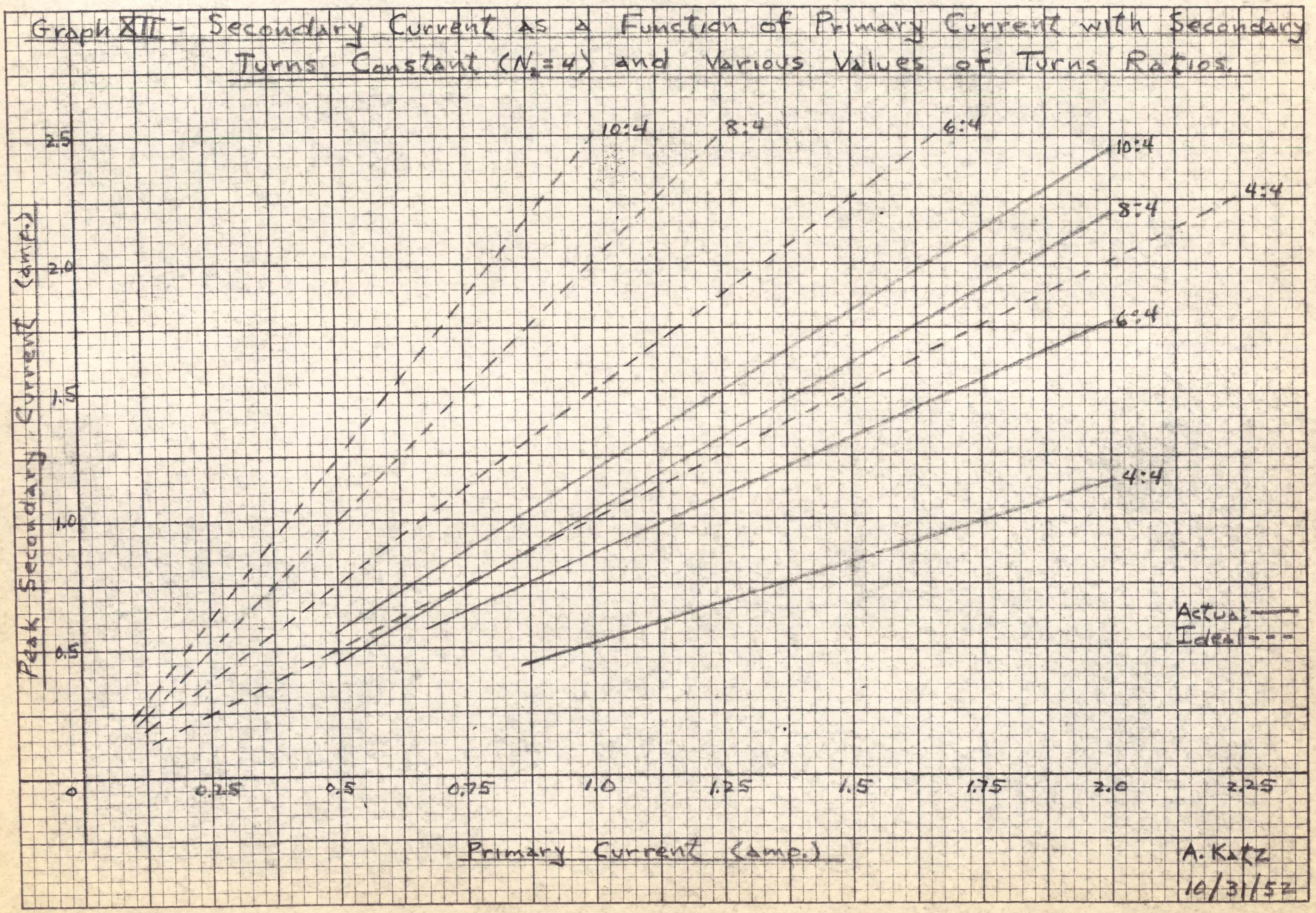
SA-48388-G

359T-6G KEUFFEL & ESSER CO.
5 × 5 to the ½ inch.
MADE IN U. S. A.



SA-48389-G

359T-6G KEUFFEL & ESSER CO.
5 × 5 to the ½ inch.
MADE IN U. S. A.



R. Best

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: A METHOD FOR ACCEPTANCE TESTING OF FERRITE CORE PRODUCTION LOTS

To: Group 63 Staff

From: P. K. Baltzer

Date: December 4, 1952

Abstract: A method for screening the Production Lots of ferrite cores to be tested for MTC is required because of testing limitations and large variations found between Production Lots. It is proposed that a sample of 100 cores be taken from each lot and tested at the factory. The mean of the sample must be between the Screening Limits specified for the lot to be accepted, from the manufacturer, for complete testing. The Per Cent Yield of the total number of cores to be tested individually has been calculated as a function of Screening Limits (see Figure 1).

Problem Defined

The urgent need for memory cores for MTC has placed considerable pressure on those involved in testing and selecting them. Two independent production lots of ferrite cores have been tested. The material and core size were different in each case. It was found that both production lots of 1,000 had the same relative distribution about their respective mean value of "Disturbed One" output voltage. Therefore, as long as the method of manufacture is not grossly changed, the information gained from the testing of these two batches of 1,000 cores can be utilized for statistical calculations concerning future production.

In the very near future, the cores needed for MTC will be in the process of being tested here. Regardless of what testing mechanism is used, the yield percentagewise of the cores tested is an important factor. Therefore, a preliminary selection of production lots is necessary at the factory.

Method Proposed

It is proposed that each Production Lot be accepted or rejected at the factory on the basis of testing a random sample of fixed size. The "Disturbed One" output voltage of the sample cores should be measured in the same way that all the cores will be tested before being placed in the memory. The arithmetic mean of the sample must lie within specified "Screening Limits" for a production lot to be accepted.

The accepted Production Lot must still be completely tested at MIT. Each core that will be used must satisfy the specifications given; that is, the "Disturbed One" output of an individual core must lie within specified "Tolerance Limits."

"Screening Limits" therefore must apply only to sample means, for the purpose of screening Production Lots. Whereas "Tolerance Limits" apply only to individual cores and are not necessarily equal to the "Screening Limits."

Tolerance Limits will remain constant, however, the Screening Limits may have to be varied to suit the manufacturer's ability to maintain uniformity between production lots. The size of the Screening Limits will determine the total number of cores necessary to test individually to obtain a given number of useful cores. Per Cent Yield will be defined as:

$$\% \text{ Yield} = \frac{\text{Number of Useful Cores}}{\text{Number Tested Individually}} \times 100$$

Hence, it is necessary to know the relationship between Per Cent Yield and Screening Limits. This relationship was found by calculations based on the two production lots already tested, and is shown in Figure 1. This curve will enable us to know what Percentage Yield is sacrificed for any expansion that might be necessary in the Screening Limits.

Sampling

The sample taken from each Production Lot of about 2,000 cores must be large enough to truly represent the lot, and yet not be unwieldy. The mean of a random sample of 30 cores has a standard error from the mean of the production unit of 0.003 volts. However, the manufacturer has found that a sample of 100 cores is necessary to obtain a representative sample. This large size is necessary because of difficulty in obtaining a truly random sample of a smaller size. Therefore, since the present testing methods permit a larger sample, it is proposed that a sample of 100 cores be used. The standard error of the mean of a 100 core sample would be 0.002 volts.

Calculations

All calculations have been based on the assumption that the distribution within a lot is normal and that the sample is random. The expression for the normal distribution is given by the following function:

$$f(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{x^2}{2\sigma^2}}$$

where x is measured from the mean of the distribution, and σ is the standard deviation.

The probability (P_1) that a lot with a given mean will contain desired cores will simply be the area under distribution curve enclosed by the Tolerance Limits (T.L.) (see Figure 2a).

Hence:

$$P_1 = \int_{M-T.L.}^{M+T.L.} f(x - M - \sigma_L)\, dx$$

where σ_L is Lot Deviation and defined as the variation of Lot Mean from the Desired Mean (M).

Therefore P_1 can be found as a function of σ_L (see Figure 2b). σ_L is plotted in σ (Standard Deviation) units since the distribution involved in the calculations was the total distribution within a lot. The Standard Deviation found, for the two lots of 1,000 cores tested, was (0.15)M or 0.016 volts for a mean of 0.11 volts. This curve indicates the fractional yield of desired cores that can be expected from any lot, when the Lot Mean is known.

Since the true mean of any lot is not known until the lot is completely tested, we must sample and base our screening process on the mean of the sample. It is known that the distribution of the Sample Mean of random samples of a given size will be normal about the lot mean, with a Standard Error (S.E.) of S.E. = $\sigma/\sqrt{N}$ where N is the number in sample.

The probability (P_2), that a lot will pass the screening process, is the area under the distribution curve of Sample Means between the Screening Limits (see Figure 3a).

Hence:

$$P_2 = \int_{M-S.L.}^{M+S.L.} f(x - M - \sigma_L)\, dx$$

Therefore P_2 can be found as a function of σ_L for any given value of Screening Limits (see Figure 3b). σ_L is plotted in S.E. units since the distribution involved is that of Sample Means.

Now we have the probability (P_1) that a lot will contain desired cores and the probability (P_2) that a lot will pass screening process. The final objective is to obtain the Percentage Yield from total cores tested individually as a function of the Screening Limits, for a given size sample. This is given by:

$$\% \text{ Yield} = \frac{\int_{-\infty}^{\infty} P_1 P_2\, d(\sigma_L)}{\int_{-\infty}^{\infty} P_2\, d(\sigma_L)} \times 100$$

Unfortunately, it is no longer possible to keep the calculations general concerning Sample Size (see Figure 1). P_1 was found using σ units and P_2 using S.E. units; and to find Per Cent Yield, they must be combined.

Thus a factor of $\sqrt{N}$ is involved. It was assumed in the calculation of P_2 that each Lot Mean was equally probable. Therefore since the manufacturer will attempt production control, the curve of Per Cent Yield vs. Screening Limits is more likely to be pessimistic than optemistic.

Signed P. K. Baltzer
P. K. Baltzer

Approved DRB
David R. Brown

PKB/jk

Drawings attached:

A-53282
A-53272
A-53273

cc: W. Papian
W. Ogden

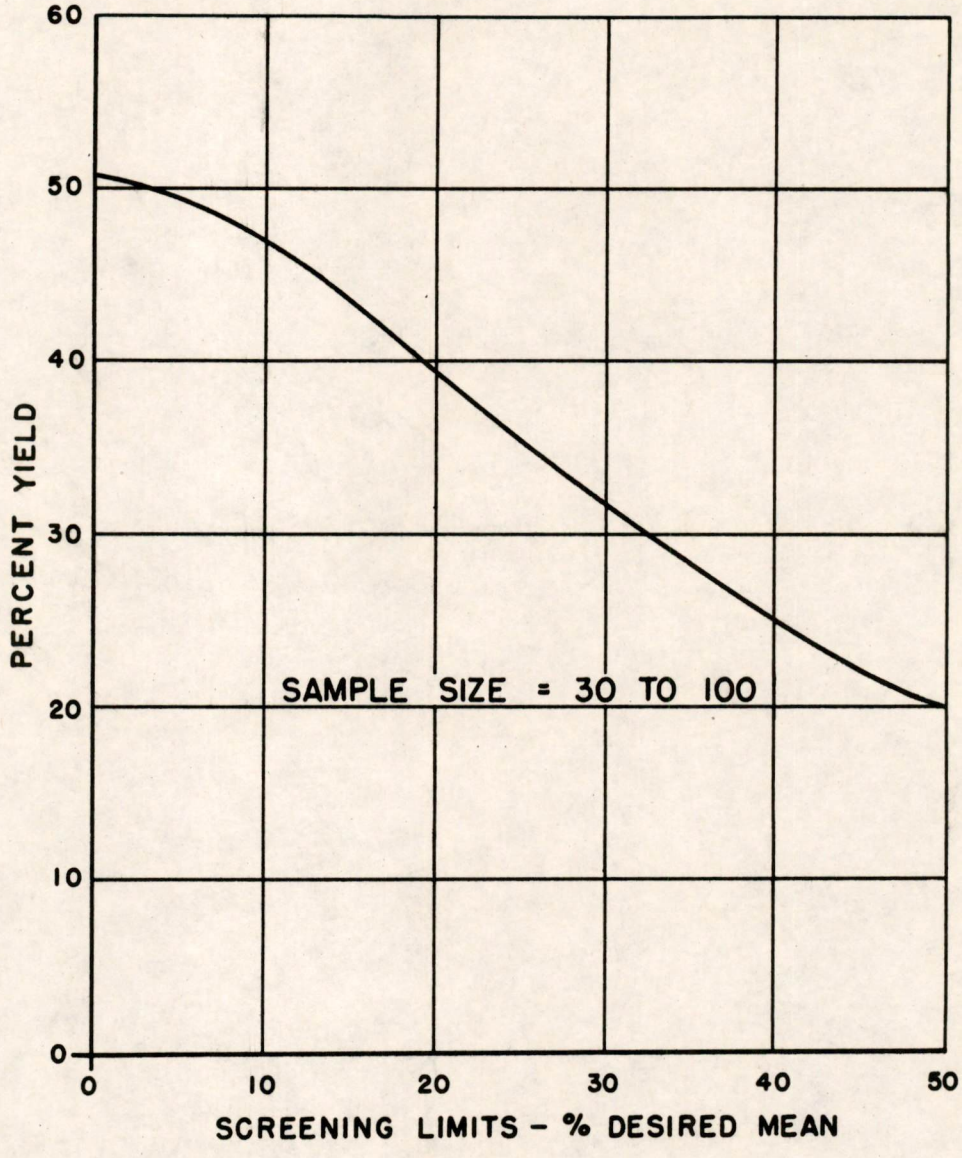


FIG. 1

PERCENT YIELD

VS.

SCREENING LIMITS

A-53282

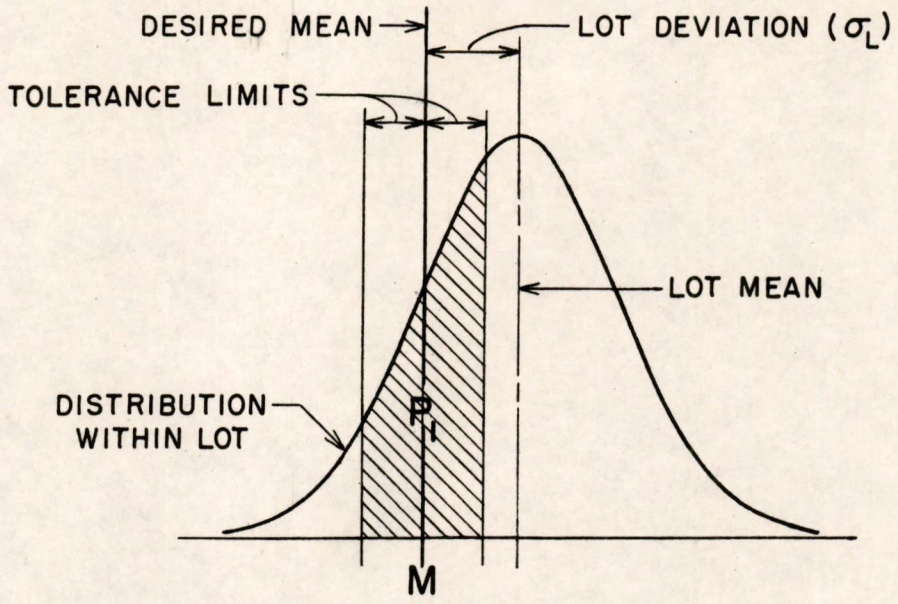


FIG. 2a

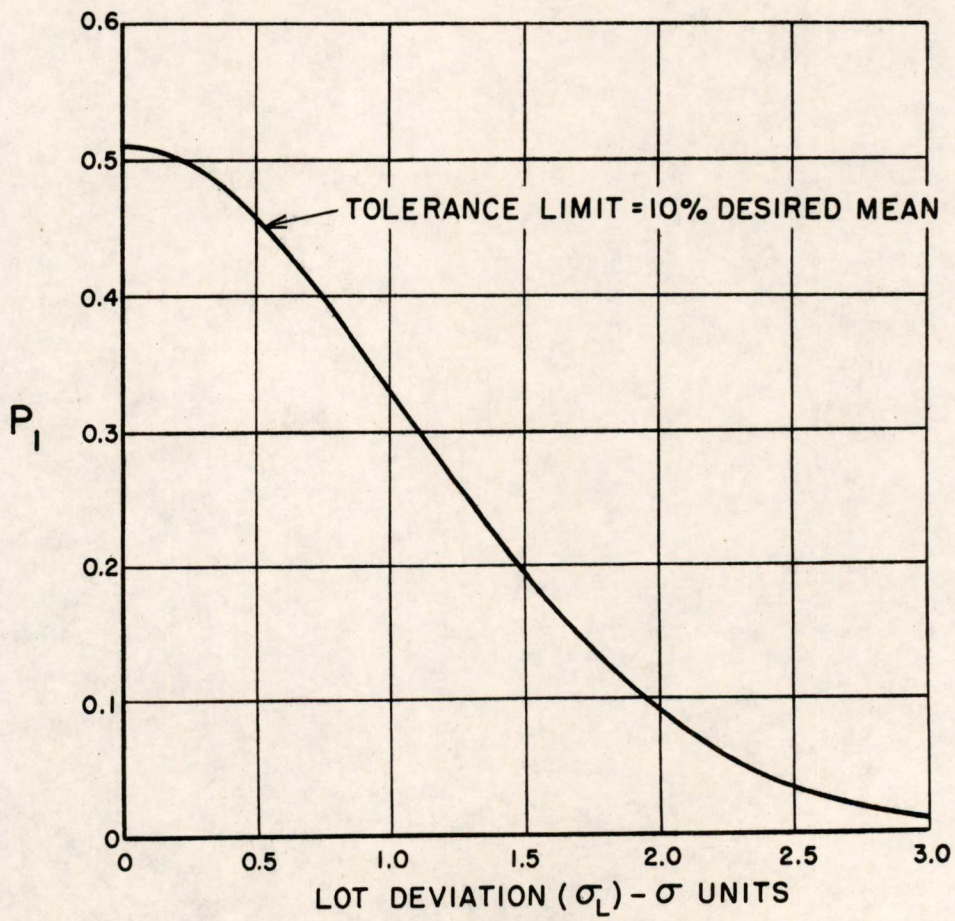


FIG. 2b

A-53272

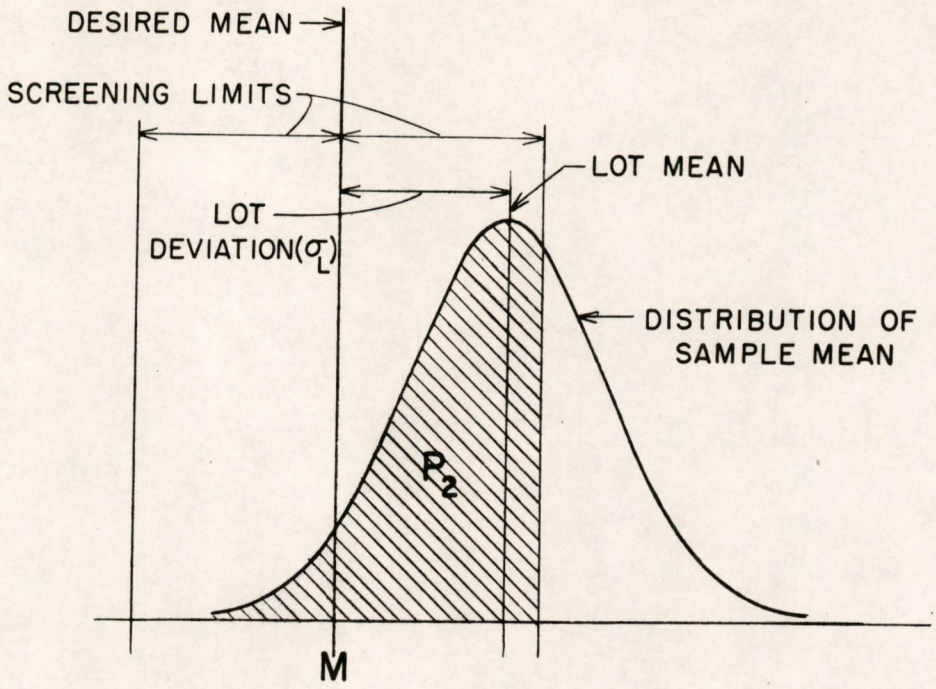


FIG. 3a

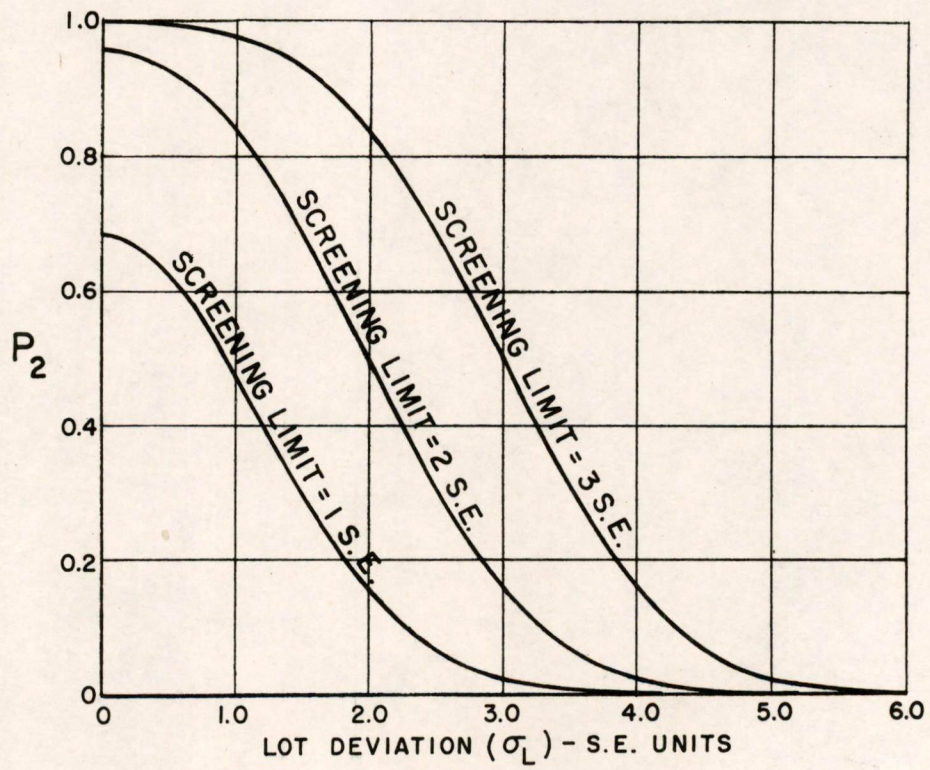


FIG. 3b

A-53273

R. Best

Core Drivers V + VI

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: CORE DRIVERS -- MODEL V AND MODEL VI

To: Group 62, 63, and Test Equipment Committee

From: Harold W. Boyd

Date: February 10, 1953

Abstract: The Model V and Model VI Core Drivers are standard test units which can deliver rectangular wave current pulses of variable amplitude, rise time, and duration. Model V supplies negative-going pulses, whereas Model VI supplies positive-going pulses, both from a ground level.

1.0 SPECIFICATIONS

Dimensions: 5-1/4 x 5 x 19 inches for rack mounting.

Circuits:
Mono-bi-stable multivibrator (5965)
Amplifier (1/2, 5687)
Cathode follower (1/2, 5687)
Current Amplifier (4, 6CD6's)

Input: Standard .1 μsec pulses, negative, 13-30 volts.

Output:
Shape - rectangular
Amplitude - variable from 0 to greater than 1.6 Amps.
Rise Time - less than 0.15 μsec, and .2 to 1.0 μsec in 2 overlapping ranges
Duration - 1 - 40 μsec in two overlapping ranges (monostable).
.6 - 40 μsec (bi-stable).

Duty Factor:
Limited by multivibrator to no more than:
40% in monostable
75% in bistable
Limited by dissipation in output tubes to no more than:
20% at 2.0 amps output
25% at 1.6 amps output

40% at 1.0 amps output
50% at 0.8 amps output
75% at 0.53 amps output

Resolution Time: 0.5 μsec at maximum output amplitude.
(May be complemented in "bistable" from 12.5 KC to 2 Mc by tying J1 and J2 together)

Power Requirements: (approximate during pulse)

	Model V	Model VI
+150		.03 - 2.03 A.
-150	.03 - 2.03 A.	.04 A.
-300	.04 A.	
6.3 V a-c		10.6 A.

2.0 OPERATION

The Core Drivers (schematics C-52170 (Model V) and C-52643 (Model VI)) consist of four stages; these are in turn: a monostable multivibrator, inverter-amplifier, cathode follower, and current amplifier.

The monostable multivibrator is for convenience labeled mono-bi-stable. The name arises from the two options in the use of this stage. The multivibrator favors one side as its conducting side to insure the current amplifier stage of being normally cut-off. In monostable operation the multivibrator is set to its unfavored state by a pulse fed into J1-set and there remains for a duration determined by the time constant of the timing network.* The duration of the multivibrator in the selected state determines the pulse width of the output current squarewave. The pulse width is variable from less than 1 to greater than 40 μsec in two overlapping regions as selected by the Duration Coarse and Duration Fine controls.

---

* Timing network -- C-2 or C-3, and R_2 and CR3 in both C-52170 and C-52643.

In bi-stable operation the multivibrator is set to its unfavored state by a pulse fed into J1-set and there remains (up to above 40 μsec) until cleared by a pulse fed into J2-clear. In this mode of operation, therefore, the multivibrator appears to be bi-stable, and the output pulse width is determined by the time delay between the two input triggers (J1 and J2).

The output gate of the multivibrator stage cuts off the normally conducting inverter-amplifier which follows it. The rate at which the voltage rises at the plate of this tube is determined by the value of capacitance between its plate and ground. This rate in turn determines the rate of rise in the output current pulse. With the Rise Time Coarse set on "short," the rise time is .15 μsec or less, but is not variable in this position. With the Rise Time Coarse set on "medium" or "long" the rise time can be varied by the Rise Time Fine control from less than .2 μsec to greater than 1 μsec in two overlapping ranges.

The upper level of the output voltage of the inverter-amplifier is varied by a diode and potentiometer which afford a variable clamp. The lower level of voltage output is sufficient at all times to insure cut-off of the current amplifiers. The upper level can be varied by the output Amplitude control (variable clamp) from a value sufficient to insure cut-off of, to a value sufficient to produce slightly positive bias on the 6CD6's . Thus, the output amplitude can be varied from 0 to about 2 Amperes. If all 4-- 6CD6's are marginal the maximum current would be about 1.6 Amperes. If all 4 - 6CD6's are average more than 2 Amperes may be obtained.

The current output of the Core Drivers, although variable up to about 2 Amperes, is limited by the screen dissipation of the 6CD6's that comprise the current amplifier stage. A measure of the screen dissipation is afforded by the screen current warning lamp and for safety's sake should not be allowed to glow. When driving cores at 2 Amperes, a duty factor of about 20% can be obtained without excessive screen dissipation. At a duty factor of 50%, driving cores, a maximum of about 0.8 Amperes of output current may be safely obtained.

If it is desired not to use more than 1 Ampere output pulses, two 6CD6's (of the normal complement of 4) may be used to obtain faster rise times. The duty factor, however, should not be allowed to exceed 20% at 1 Ampere -- even though the screen warning lamp will not glow till a 40% duty factor is reached.

The model VI core driver has, in addition to the above controls, a zero current adjustment potentiometer located in the back of the unit. With this control the quiescent (no-trigger) output current can be brought to zero for all or any setting of the output Amplitude control. This is accomplished by adjusting the potential at the 6CD6's cathodes to ground.

3.0 PRECAUTIONS

To avoid excessive heater-to-cathode voltages on the tubes, the use of either a separate filament supply or an isolation transformer is required for Model V. Since, however, both models V and VI require 10.6 Amperes at 6.3 volts, a separate filament supply is advisable.

It is suggested that whenever the Core Driver is turned on, the output amplitude control be fully counter-clockwise (down) at first. The output can then be brought up to the desired value or to a value limited by the glow of the screen current warning lamp. This is merely to protect the tubes in case the initial combination of duty factor, amplitude setting, and trigger amplitudes, are such that screen dissipation would be excessive.

Signed H. W. Boyd
Harold W. Boyd

Drawings:

Model V - C-52170

Model VI - C-52643

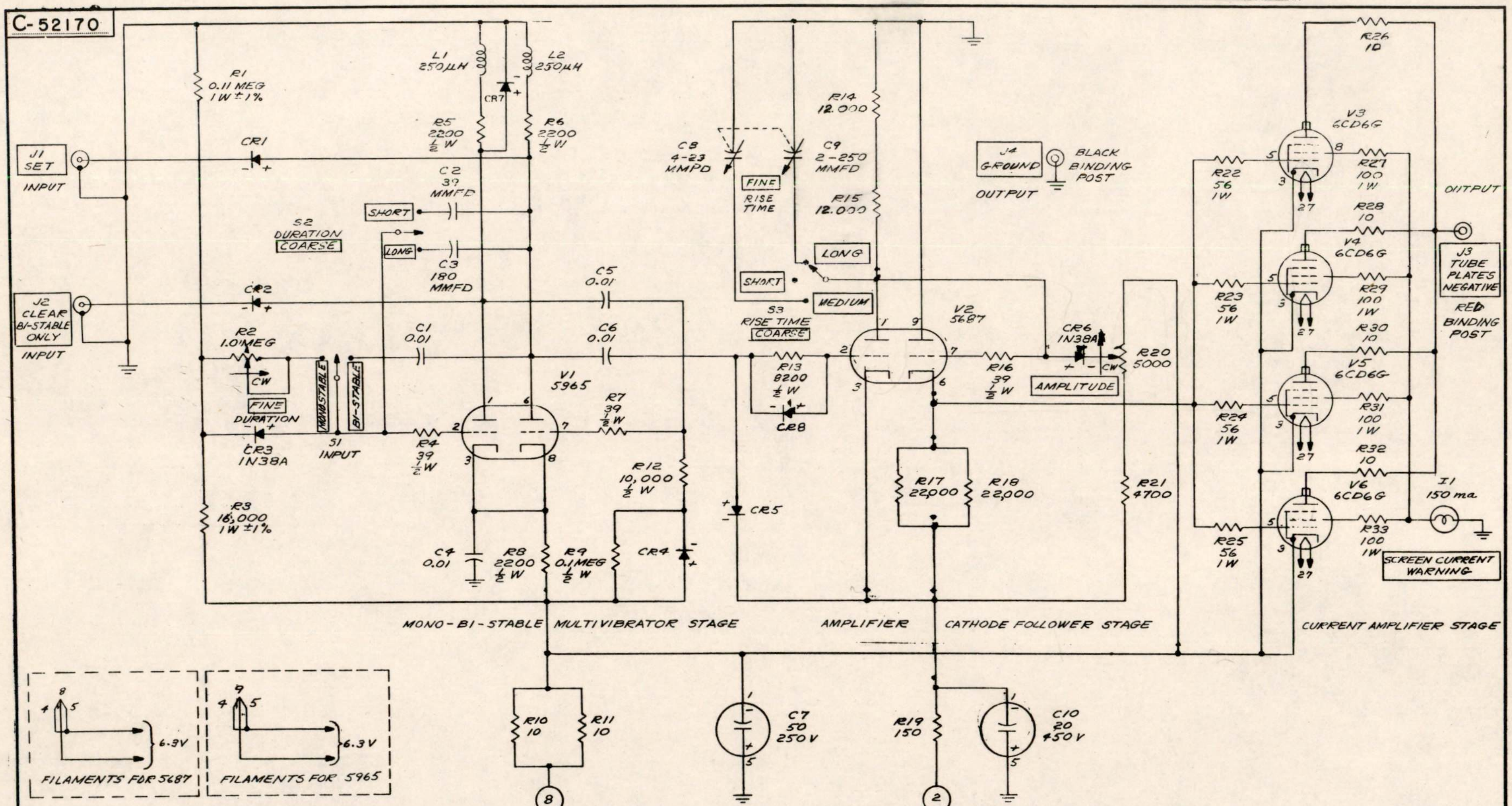
Approved R. L. Best
R. L. Best

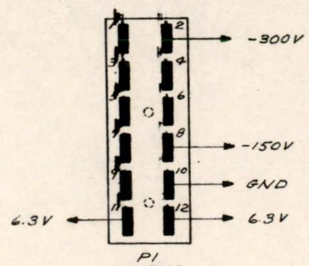
Approved DRB
D. R. Brown

HWB/cs

Drawings attached:
C-52170
C-52643

C-52170





P1
12 PIN
JONES PLUG
(MALE)

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTORS ARE IN OHMS; 2W.
   B. RESISTORS ARE ±10%.
   C. CAPACITORS ARE IN MICROFARADS.
   D. VIDEO CONNECTORS J1 & J2 ARE JAN UG-290/U
   E. CRYSTAL RECTIFIERS ARE SYLVANIA TYPE 1N34A.
2. USE SEPARATE FILAMENT SUPPLY OR ISOLATION TRANSFORMER
3. CONNECT SHAFTS OF C8 & C9 TOGETHER WITH SLEEVE. CONNECT FRAMES TOGETHER FOR RIGIDITY.
4. THIS DRAWING IS SIMILAR TO C-52643 (CORE DRIVER MOD VI) — EXCEPT OUTPUT & SUPPLY VOLTAGES.

DRAWING REFERENCES:
1. ASSEMBLY: D-52622
2. PARTS LIST: PL-52622

GRADED BY: DATE: THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:
GRADE I FOR REFERENCE ONLY
DKB 10-9-52 GRADE II PRELIMINARY DESIGN
DKB 1-5-53 GRADE III FINAL DESIGN

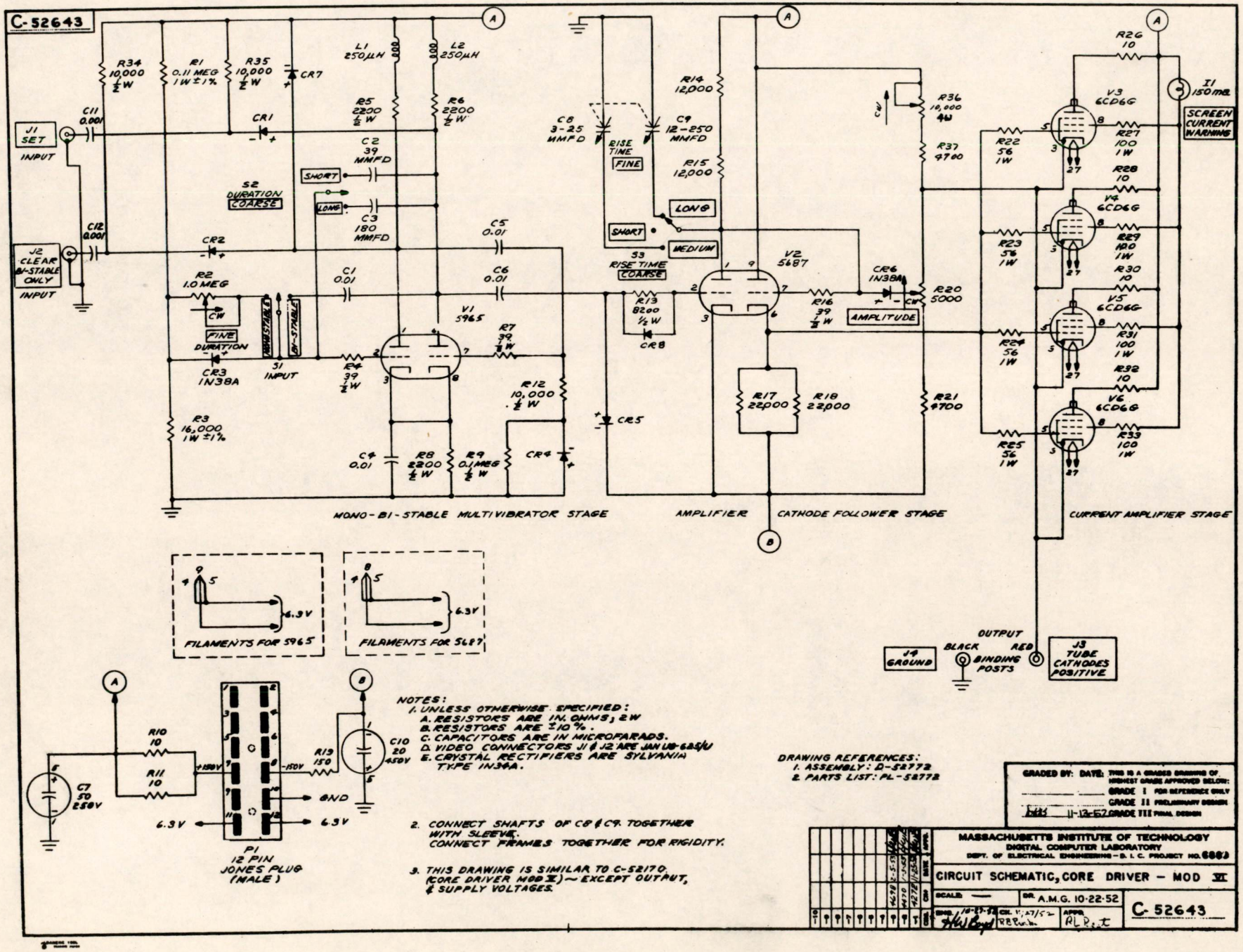
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING — D. I. C. PROJECT NO. 6889

CIRCUIT SCHEMATIC, CORE DRIVER-MOD V, TE

SCALE: — DR. CRD 9/25/52
ENG. 9/25/52 H W Boyd CK. 9/29/52 P P Burke APPD. R L Best

C-52170

K+E ALBANENE 1961


C-52643
J1 SET INPUT
J2 CLEAR BI-STABLE ONLY INPUT
S1 INPUT
S2 DURATION COARSE
S3 RISE TIME COARSE
FINE DURATION
FINE
SHORT
LONG
MEDIUM
AMPLITUDE
CW
MONO-BI-STABLE MULTIVIBRATOR STAGE
AMPLIFIER
CATHODE FOLLOWER STAGE
CURRENT AMPLIFIER STAGE
SCREEN CURRENT WARNING
FILAMENTS FOR 5965
FILAMENTS FOR 5687
J4 GROUND
OUTPUT BLACK RED BINDING POSTS
J3 TUBE CATHODES POSITIVE
P1 12 PIN JONES PLUG (MALE)
NOTES:
1. UNLESS OTHERWISE SPECIFIED:
A. RESISTORS ARE IN OHMS, ½W
B. RESISTORS ARE ±10%.
C. CAPACITORS ARE IN MICROFARADS.
D. VIDEO CONNECTORS J1 & J2 ARE JAN UG-625/U
E. CRYSTAL RECTIFIERS ARE SYLVANIA TYPE 1N38A.
2. CONNECT SHAFTS OF C8 & C9 TOGETHER WITH SLEEVE. CONNECT FRAMES TOGETHER FOR RIGIDITY.
3. THIS DRAWING IS SIMILAR TO C-52170 (CORE DRIVER MOD II) — EXCEPT OUTPUT, & SUPPLY VOLTAGES.
DRAWING REFERENCES:
1. ASSEMBLY: D-52772
2. PARTS LIST: PL-52772
GRADED BY: DATE: THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:
GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
11-13-57 GRADE III FINAL DESIGN
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
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Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: NORMALIZED FLIP-FLOP CHART

To: N. H. Taylor

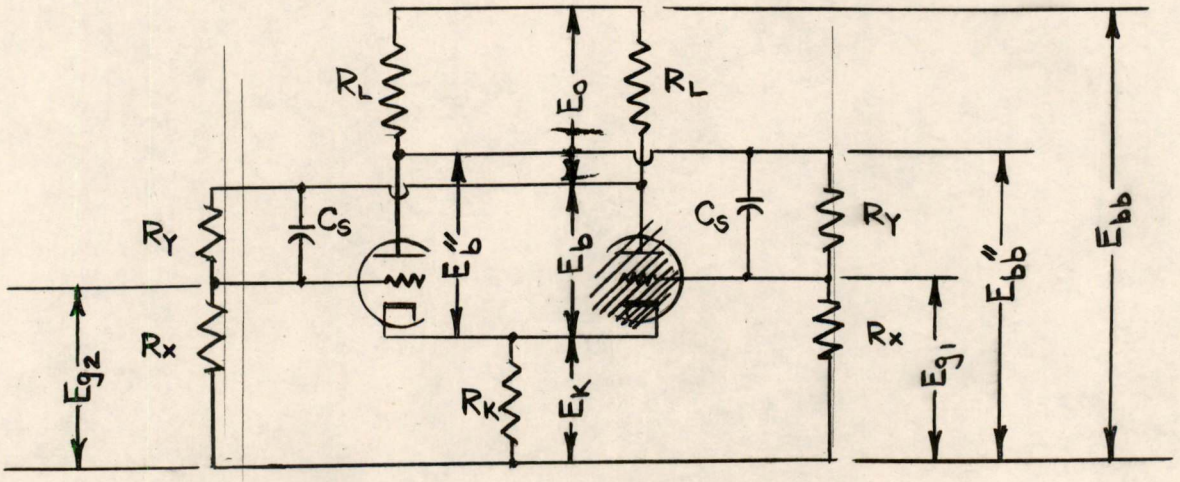
From: Hal W. Boyd

Date: February 17, 1953

Abstract: A fast and accurate method of designing and analyzing triode flip-flops is described. This method requires the use of only the Normalized Flip-Flop Chart (attached) and the plate characteristics of the tube to be used. A study of the Normalized Flip-Flop Chart makes it possible to visualize the behavior of a flip-flop for any combination of parameters, and to visualize the results of changing any one or a combination of parameters.

1.0 Derivation:

In order to understand more fully the limits to which the chart can be used and tested, its derivation is given below. The notations used in the derivation are either shown in Figure 1 or are defined in the test.



(cross hatched tube is conducting)

Figure 1

Let stability, s, be defined as the ratio of the grid swing available, E_s, to that required to cut either tube off, E_{co}. Then

$$s = E_s/E_{co} \tag{1}$$

where, from Figure 1, $$E_s = E_{g1} - E_{g2} \tag{2}$$

Defining the cut-off, μ, μ_o, as the magnitude of the ratio, at cut-off, of the plate-to-cathode voltage, E_b'', to the grid-to-cathode voltage, E_{co}, then:

$$E_{co} = E_b''/\mu_o \tag{3}$$

Assuming that the grid bias on the conducting tube is zero, then:

$$E_{g1} = E_k \tag{4}$$

substituting (4) into (2):

$$E_s = E_k - E_{g2} \tag{5}$$

From (1) and (5):

$$E_k - E_{g2} = s\, E_{co} \tag{6}$$

From Figure 1:

$$E_b'' = E_{bb} - E_k \tag{7}$$

For simplicity and to make the chart more general, assume that $R_L \ll R_y$ so that R_L is negligible in comparison to R_y. Hence from the figure:

$$E_k = \frac{R_x}{R_x + R_y} E_{bb} \tag{8}$$

Inserting (3), (7), and (8) into (6):

$$\frac{R_x}{R_x + R_y} E_{bb} - E_{g2} = s \frac{E_{bb}}{\mu_o} - \frac{R_x}{R_x + R_y} \frac{E_{bb}}{\mu_o} \qquad (9)$$

But from Figure 1:

$$E_{g2} = \frac{R_x}{R_x + R_y} (E_{bb} - E_o) \qquad (10)$$

Combining (9) and (10):

$$\frac{R_x}{R_x + R_y} E_{bb} - \frac{R_x}{R_x + R_y} \left(E_{bb} - E_o \right)$$

$$= s \left[\frac{E_{bb}}{\mu_o} - \frac{R_x}{R_x + R_y} \frac{E_{bb}}{\mu_o} \right] \qquad (11)$$

Simplifying:

$$E_o = (s/\mu_o) (R_y/R_x) E_{bb} \qquad (12)$$

From Figure 1:

$$E_b = E_{bb} - E_o - E_k \qquad (13)$$

Normalizing E_o, E_k, and E_b from equations (12), (8), and (13) with respect to E_{bb}, and letting primes denote the normalized E_o, E_k, and E_b:

$$E_o' = E_o/E_{bb} = (s/\mu_o) (R_y/R_x) \qquad (14)$$

$$E_k' = \frac{E_k}{E_{bb}} = \frac{R_x}{R_x + R_y} \qquad (15)$$

$$E_b' = \frac{E_b}{E_{bb}} = 1 - E_o' - E_k' \qquad (16)$$

From equations (1) and (3):

$$s/\mu_o = E_s/E_b'' \qquad (17)$$

Inserting (5) for E_s:

$$s/\mu_o = \frac{E_k - E_{g2}}{E_b''} \qquad (18)$$

Combining (10) and (7) in (18):

$$s/\mu_o = \frac{\frac{R_x}{R_x + R_y}(E_{bb} - E_o)}{E_{bb} - E_k} \qquad (19)$$

Normalizing (19) and substituting (15):

$$s/\mu_o \quad \frac{E_k' - E_k'(1 - E_o')}{1 - E_k'} \qquad (20)$$

but, $1 - E_o' = E_b' + E_k'$, hence:

$$s/\mu_o \quad \frac{E_k' - E_k' E_b' - (E_k')^2}{1 - E_k'} \qquad (21)$$

To find the maximum s/μ_o with respect to E_k' at a fixed E_b', let $\partial \frac{s}{\mu_o} / \partial E_k' = 0$, and solve for E_k' ; hence:

$$\frac{\partial s/\mu_o}{\partial E_k'} = \frac{(1 - E_i')(1 - E_b' - 2E_k') + \left[E_k' - E_k' E_b' - (E_k')^2\right]}{(1 - E_k')^2} = 0 \qquad (22)$$

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Solving for E_k': $E_k' = 1 \pm \sqrt{E_b'}$; but, as $E_k' < 1$,

$$E_k' = 1 - \sqrt{E_b'} \qquad (24)$$

From equations (14), (15), and (16) plots can be made for constant values of s/μ_o which relate E_k' to E_o' and E_b' to E_o'. Also, by letting $R_d = R_x/R_y$, a plot of R_d vs. E_k' can be made.

From equation (24) a plot of E_k' for maximum s/μ_o at fixed E_b''s can be made vs. E_o', thus completing the normalized flip-flop chart.

2.0 Use of the Chart.

For fast operation it is desirable to switch large currents; i.e., to use high tube currents. In general, this may be interpreted on the Normalized Flip-Flop Chart to mean operating the flip-flop near the origin where the higher tube drops are located. The characteristics of the tube, its plate dissipation rating, over-all flip-flop reliability or stability, triggering characteristics, output voltage requirements, wattage ratings of components, and power supplies serve to define and limit the freedom of moving the operating point on the chart.

For high flip-flop reliability it is desirable to have a sufficiently high stability factor. With respect to the Normalized Flip-Flop Chart, this means operating the flip-flop away from the origin of the chart. Again such things as tube characteristics, triggerability, output requirements, etc. serve to define and limit the range over which the operating point can be moved.

For the fastest operation at the highest stability, the flip-flop should be operated on the "line of maximum s/μ_o with fixed E_b'". The tube characteristics, supply voltages, output swing, etc. determine whether or not operating on a point on this line is desirable. Operation below and to the right of the "line of maximum s/μ_o with fixed E_b'" at either a fixed E_b' or s/μ_o, yields a larger normalized output swing than operation above and to the left of the line. Two advantages are realized by operating in this region. These are: better triggering characteristics and, if the output swing is more than needed, isolation of the flip-flop from its load by tapping the plate resistor for the desired output swing.

The reason that triggering characteristics are better in this region is that the lower operating point corresponds to a lower normalized

E_k which, in turn, determines a lower ratio of R_x to $R_y(R_d)$. The combination of greater normalized output voltage swing and smaller divider arm ratio allows a greater difference in charge on the memory or speeding up capacitors (labelled C_s in Figure 1). This allows better complementing characteristics, and allows larger triggers before destroying the memory. A larger ratio of a-c to d-c gain in the divider arm also follows, which allows easier triggering. In addition to the extended trigger amplitude range, the resolution time is decreased, allowing faster operation.

The Normalized Flip-Flop Chart can be used for synthesizing as well as analyzing almost any type of triode flip-flop. To enter the chart one must know or determine at least two of the following:

1. μ_o of the tube.
2. s
3. E_o
4. E_k
5. E_b
6. R_d
7. E_{bb}

For design applications of the chart, some modifying considerations might be:

1. Resolution time.
2. Qualitative reliability.
3. Triggering characteristics
4. Tubes plate dissipation, I_b, or E_b.
5. Wattage ratings of components.
6. Available power supplies.

The more of the above that are known, providing there are no contradictions, the more rapid the solution.

In designing flip-flops by the Normalized Flip-Flop Chart method, synthesizing is the first step. After the synthesis of the flip-flop to meet its requirements, the nearest RMA size components are computed. Which side of the ideal is more desirable can be determined from the chart. The flip-flop with RMA components can then be resolved by the chart and an analysis made to determine whether further trials are needed.

If the plate resistor, R_L, cannot be considered negligible with respect to R_y, as the derivation assumes, then a correction may be applied. For computations on the chart, substitute E_{bb}" (Figure 1) for E_{bb} for the normalizing factor; hence, in converting from absolute to normalized and vice-versa, E_{bb}" is to be used. The only values thus affected are E_o, E_b, and E_k. E_o, instead of being the voltage across R_L, is now, however, the output voltage swing. The resistance at the plate of the flip-flop is now the parallel combination of R_L and the R_x, R_y sum.

If the "on" tube's bias is not zero, no corrections need be applied to the chart. In designing for a negative "on" tube bias, the values of the resistances R_L and R_k are determined by E_o ' E_{bb} and E_k ' E_{bb}, and by the I_b of the tube at the E_b 'E_{bb} and the negative bias desired.

3.0 Example

An example in the use of the chart in designing a fast operating, high-reliability, flip-flop to drive heavy 7AK7 gate tube loads is given below.

For fast operation large switching currents are required, the amount being limited by the plate dissipation of the tube to be used and the stability required. The supply voltages are limited by the output voltages required, the tube and component wattage ratings, and the stability required.

Since large tube currents are wanted, it would be advantageous to operate the tube close to zero bias up to the allowable plate dissipation. Since, however, tube reliability is a must, if the tube is operated in that region then some provision for grid current must be made for low I_b tubes. In the type of circuit shown in Figure 1, if grid current were to be drawn, the high impedance divider arm would collapse, resulting in flip-flop failure.

A low-impedance cathode-follower divider (Figure 2) would, on the other hand, provide a grid-current source for low I_b tubes. In addition to allowing positive bias on an "on" tube, the cathode-follower isolates the flip-flop from the load, allows heavier loading, and yields faster resolution times.

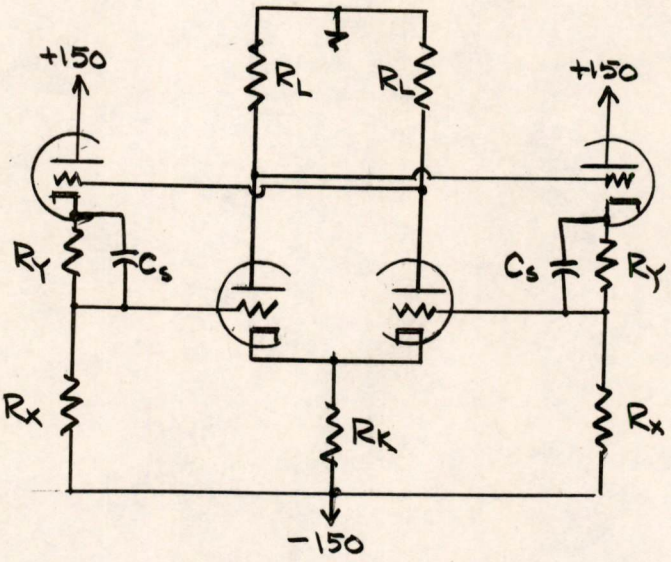


Figure 2

The required output voltage swing of the flip-flop, if it is to drive 7AK7 gate tubes, is at least 0 to -15 volts (d-c coupled). To allow poor tubes, and large component and supply voltage tolerances, an output swing of from a slightly positive value to around -30 volts should be sufficient. Allowing for a bias of about -5 volts at the cathode follower on the low side of the flip-flop, the drop across R_L should be about 35 volts, hence $E_o \cong 35$ volts.

A 5965 duo-triode is very adaptable to reliable high-speed flip-flop applications due to its high plate dissipation, high transconductance, high cut-off μ (μ_o), and liberal internal spacing. For these reasons it will be used for both the flip-flop tube and cathode-follower tube.

The allowable plate dissipation of each triode section was given as 1.5 watts. If the cathode follower output is to be as high as ground, and 2 watt or less resistors are to be used, the supply voltages could be as high as +150 and -150 volts. Thus the plate dissipation at 10 ma. would be 1.5 watts, and 1.5 watts will be dissipated in the divider.

Since the output voltage is to go negative from ground, the plate resistors are returned to ground. E_{bb}, is, therefore, 150 volts.

For supply voltage variations of around 20% or more, large resistor tolerances, and poor tube tolerability, a stability factor of about 3 should be sufficient. The larger the stability factor, the larger

the over-all flip-flop tolerances.

Summarizing: $E_{bb} = 150$ volts

$s \triangleq 3$

$E_o \triangleq 35$

tube type = 5965

From the plate characteristics of the 5965:

$$\mu_o = 150/5 = 30$$

Hence s/μ_o for $s = 3$ would be

$$s/\mu_o = 3/30 = .1$$

As the fastest operation at this stability factor is desired, the flip-flop operating point should be on or near the "line of maximum s/μ_o with fixed E_b' ".

With $E_o = 35$:

$$E_o' = E_o/E_{bb} = 35/150 = .23$$

At the intersection of $s/\mu_o = .1$, and $E_o' = .23$ the following can be read from the chart: (Note that the intersection is slightly below the "line of maximum s/μ_o for fixed E_b' ".)

$$E_k' = .3$$

$$E_b' = .47$$

$$R_d = .43$$

Hence:

$$E_k = .3\ (150) = 45 \text{ volts}$$

$$E_b = .47\ (150) = 70 \text{ volts}$$

At $E_c = 0$, $E_b = 70$, an average 5965 (from characteristics) can deliver 10.5 ma.

Therefore:

$$R_k = 45/10.5 = 4.3 \text{ K (RMA)}$$

$$R_L = 35/10.5 = 3.34 \text{ k} \cong 3.3 \text{ k (RMA)}$$

The minimum value of $R_x + R_y$, for 150 volts drop at 10 ma cathode-follower current, would be 15k.

If $R_d = .43$, then:

$$R_d = R_x/R_y = .43 \qquad R_x + R_y \geq 15k$$

$$R_x = .43\ R_y \qquad 1.43\ R_y \geq 15k$$

$$R_y \geq 15/1.43 = 10.5k$$

The nearest higher RMA size to 10.5k is 11k, hence:

$$R_y = 11k$$

$$R_x = .43\ (11k) = 4.74K$$

$$\cong 4.7K \text{ (RMA)}$$

Now

$$R_x + R_y = 15.7k$$

And

$$R_x/R_y = .427 \cong .43$$

Solving this circuit for s, taking into account the cathode-follower biases, results in an s of 3.02.

Note, however, that by moving the operating point of the flip-flop up to the "line of maximum s/μ_o with fixed E_b' " only changes E_b' by .04, and gives a gain in stability. The change in E_b by this movement is only

$$\Delta E_b = .04\ (150) = 6 \text{ volts}$$

At E_b = 64 volts, E_c = 0, an average 5965 could deliver 10 ma. Hence, moving the operating point to the intersection of $E_o' = .23$ with "the line of maximum s/μ_o with fixed E_b'" yields the following:

$$E_k' = .34$$
$$E_b' = .43$$
$$R_d = .51$$

At 10 ma I_b, then:

$$R_k = (.34)\ 150/10 = 5.1K \text{ (RMA)}$$

$$R_L = 34/10 = 3.5k \overset{a}{=} 3.6k \text{ (RMA)}$$

$$R_d = .51 = R_x/R_y \quad \text{but again } R_x + R_y \overset{\geq}{=} 15k$$

hence,

$$R_x = 5.1k,\ R_y = 10k \text{ (both RMA)}$$

Solving this circuit for s, taking into account the cathode-follower biases, results in an s of 3.7. The chart gives an s/μ_o of .12, and therefore an s of 3.6.

The former circuit is not as reliable as the latter, although the former would have better triggering characteristics. Preferring the latter for its higher reliability, the flip-flop as it now stands is shown in Figure 3 below.

Although this completes the demonstration of the use of the chart in designing a high-reliability, fast-operating, heavy-loading flip-flop, I should like to take advantage of the opportunity here afforded to give better operating characteristics to the flip-flop.

For faster rise times and sharper output waveforms, the plate resistors may be brought to a higher voltage and clamped to ground. To keep the same flip-flop operating point, however, the plate resistors

would have to be made sufficiently larger to yield the same equivalent circuit at the plates of the flip-flop tube; i.e., same voltage and current at the plates.

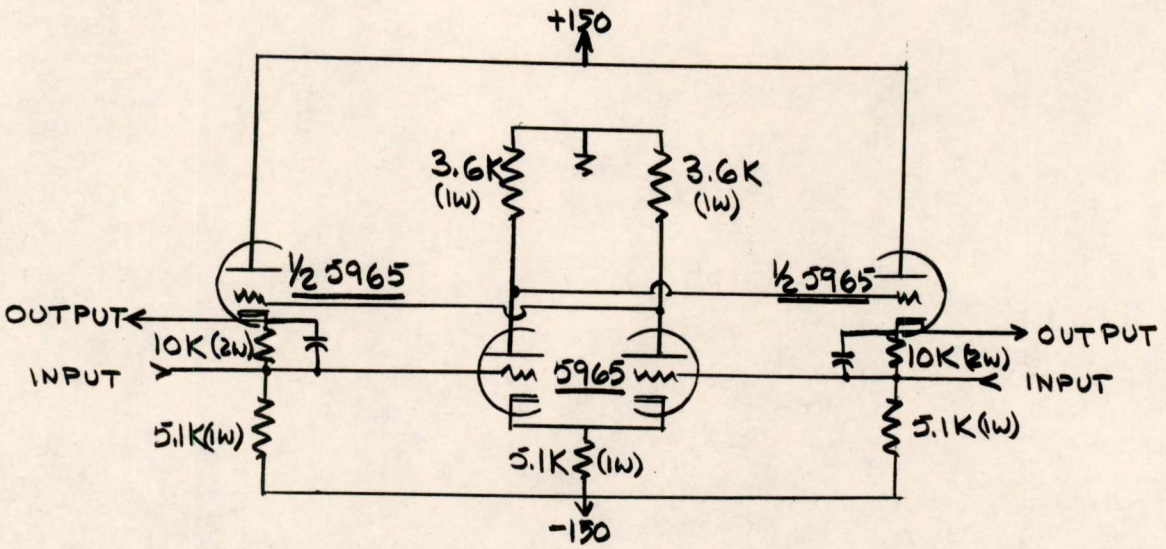


Figure 3

Hence, if +150 is to be used for this purpose, Figure 4a should be made equivalent to Figure 4b.

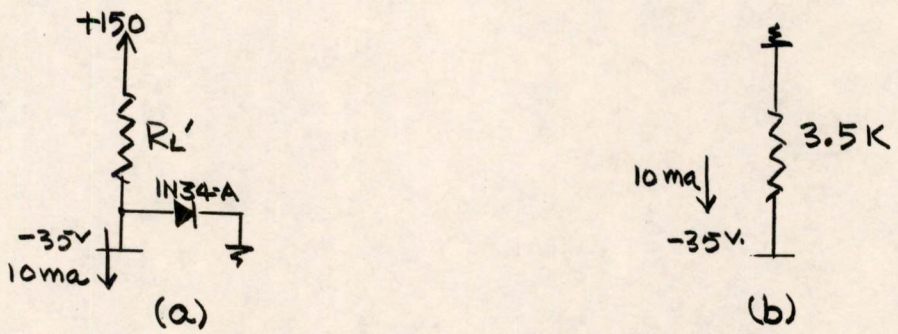


Figure 4

If the back resistance of the diode in Figure 4a can be as low as 50k, then to make the circuits equivalent:

$$150 + 35 = R_L' \left(10 - \frac{50}{36}\right)$$

or

$$R_L' = 185/8.6 = 21.5k$$

In which case, the "on" tube would have to deliver 7 ma (150/21.5) before there would be any output change. An inherent danger in this particular arrangement is that both diodes can be closed concurrently. The flip-flop would then have three stable states; i.e., either tube on, and both tubes partly on.

To alleviate this possibility, the diode switching current should be made sufficiently low, so that the poorest tube allowable is just sufficient when "on" to let the "off" tube conduct no more than switching current. Thus there will be only two distinct output levels.

From these considerations, the following plate load was derived, (Figure 5). This plate circuitry allows the output to start to +19 volts,

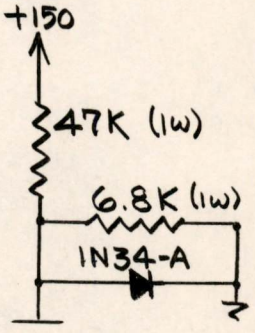


Figure 5

but clamps it at ground, yielding fast rise times and sharp corners in the output waveform. A diode-switching plate current of 3.2 ma allows up to 3.2 ma grid-current for the cathode followers, and allows the "off" tube to deliver 3.2 ma before affecting any output change on that side. In addition to these advantages is another not quite as noticeable. If negative triggers are to be inserted at both flip-flop tubes' grids, for complementing, and the flip-flop plates were not clamped, relatively large negative pips would be seen in the upper output waveform before its

transition. Clamping the plates of the flip-flop tube to ground, clamps the cathode-followers' grids to ground and allows less change on the cathode, and hence output, during the complementing trigger. Complementing on the grids with negative triggers has the distinct advantage of causing a delay in the transition of the flip-flop relative to the trigger. This is mostly due to the triggers' attempting to hold both tubes off, although secondary delays are present. The delay in switching the output levels is approximately equal to the trigger pulse width, and thus affords good counting characteristics. Additional delay and less output pip could be accomplished by inserting a small choke in the plate of each cathode-follower tube, although this would tend to increase the rise and fall times.

Signed H W Boyd
Hal W. Boyd

Drawings:
SA-48395-G

Approved R. L. Best
R.L. Best, Section Leader

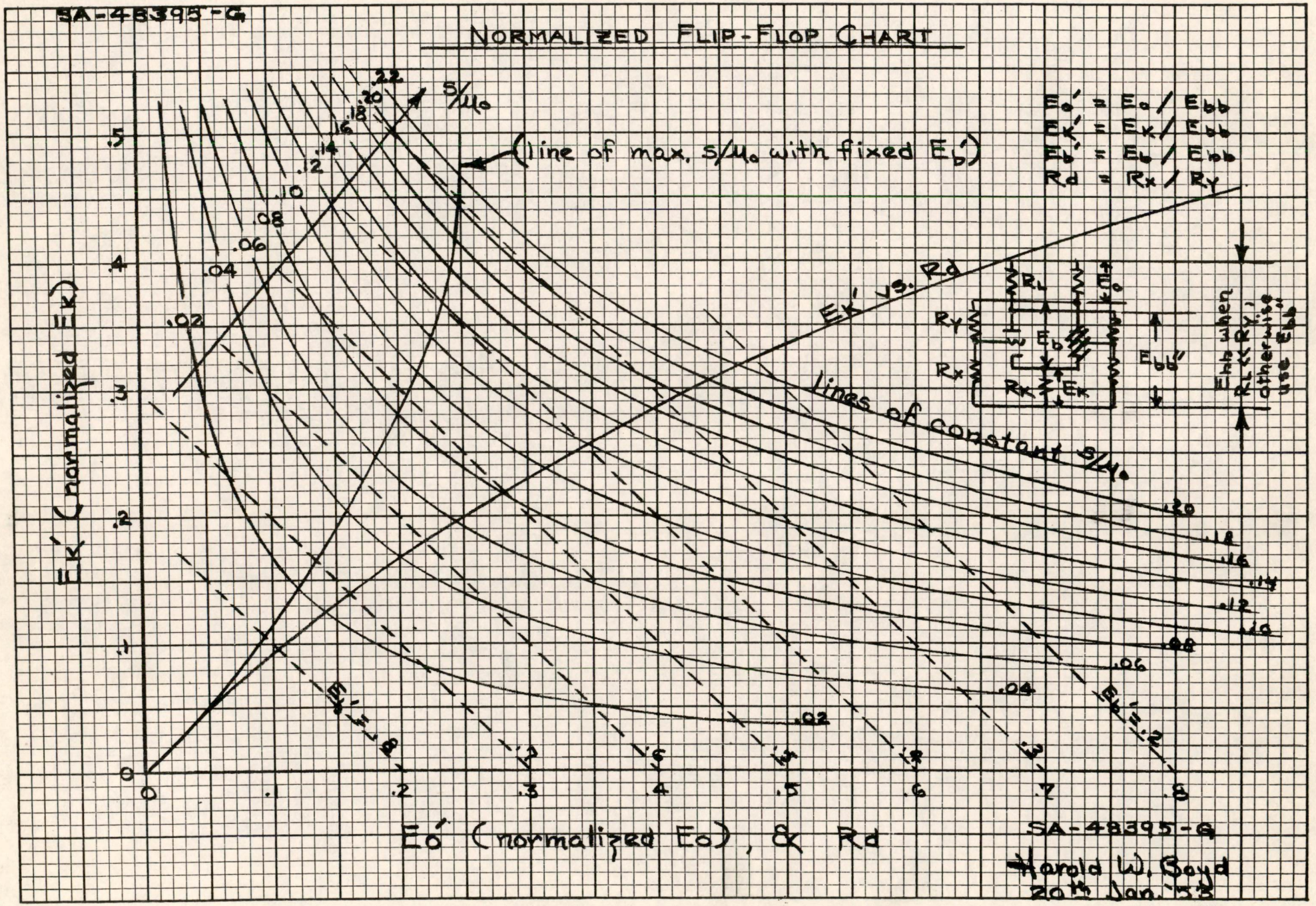
Approved N H Taylor
N.H. Taylor, Group Leader

HWB/cs

Drawing attached:
SA-48395-G

SA-48395-G

NORMALIZED FLIP-FLOP CHART



F. Best

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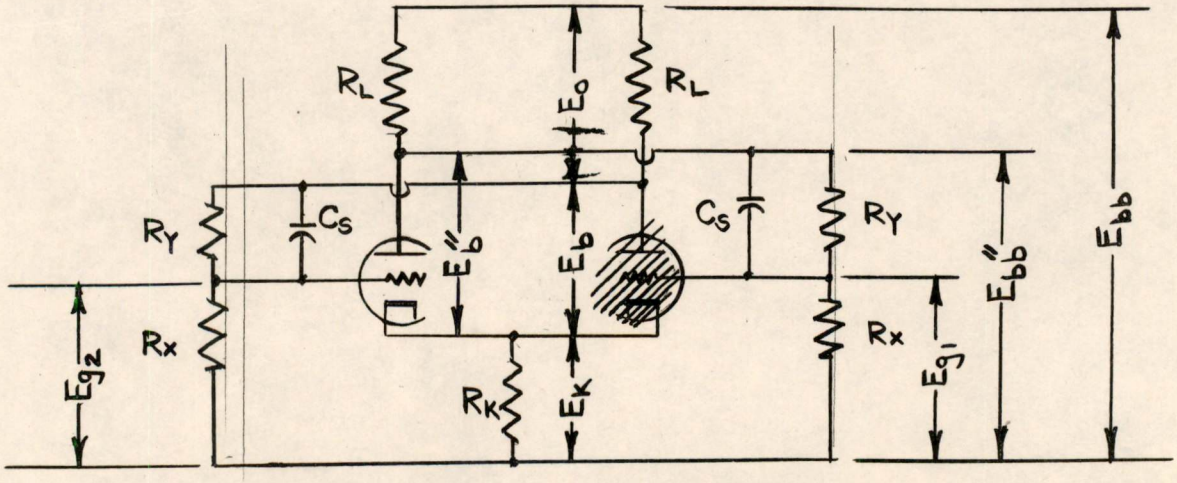

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2.0 Use of the Chart.

For fast operation it is desirable to switch large currents; i.e., to use high tube currents. In general, this may be interpreted on the Normalized Flip-Flop Chart to mean operating the flip-flop near the origin where the higher tube drops are located. The characteristics of the tube, its plate dissipation rating, over-all flip-flop reliability or stability, triggering characteristics, output voltage requirements, wattage ratings of components, and power supplies serve to define and limit the freedom of moving the operating point on the chart.

For high flip-flop reliability it is desirable to have a sufficiently high stability factor. With respect to the Normalized Flip-Flop Chart, this means operating the flip-flop away from the origin of the chart. Again such things as tube characteristics, triggerability, output requirements, etc. serve to define and limit the range over which the operating point can be moved.

For the fastest operation at the highest stability, the flip-flop should be operated on the "line of maximum s/μ_o with fixed E_b'". The tube characteristics, supply voltages, output swing, etc. determine whether or not operating on a point on this line is desirable. Operation below and to the right of the "line of maximum s/μ_o with fixed E_b'" at either a fixed E_b' or s/μ_o, yields a larger normalized output swing than operation above and to the left of the line. Two advantages are realized by operating in this region. These are: better triggering characteristics and, if the output swing is more than needed, isolation of the flip-flop from its load by tapping the plate resistor for the desired output swing.

The reason that triggering characteristics are better in this region is that the lower operating point corresponds to a lower normalized

E_k which, in turn, determines a lower ratio of R_x to $R_y(R_d)$. The combination of greater normalized output voltage swing and smaller divider arm ratio allows a greater difference in charge on the memory or speeding up capacitors (labelled C_s in Figure 1). This allows better complementing characteristics, and allows larger triggers before destroying the memory. A larger ratio of a-c to d-c gain in the divider arm also follows, which allows easier triggering. In addition to the extended trigger amplitude range, the resolution time is decreased, allowing faster operation.

The Normalized Flip-Flop Chart can be used for synthesizing as well as analyzing almost any type of triode flip-flop. To enter the chart one must know or determine at least two of the following:

1. μ_o of the tube.
2. s
3. E_o
4. E_k
5. E_b
6. R_d
7. E_{bb}

For design applications of the chart, some modifying considerations might be:

1. Resolution time.
2. Qualitative reliability.
3. Triggering characteristics
4. Tubes plate dissipation, I_b, or E_b.
5. Wattage ratings of components.
6. Available power supplies.

The more of the above that are known, providing there are no contradictions, the more rapid the solution.

In designing flip-flops by the Normalized Flip-Flop Chart method, synthesizing is the first step. After the synthesis of the flip-flop to meet its requirements, the nearest RMA size components are computed. Which side of the ideal is more desirable can be determined from the chart. The flip-flop with RMA components can then be resolved by the chart and an analysis made to determine whether further trials are needed.

If the plate resistor, R_L, cannot be considered negligible with respect to R_y, as the derivation assumes, then a correction may be applied. For computations on the chart, substitute E_{bb}" (Figure 1) for E_{bb} for the normalizing factor; hence, in converting from absolute to normalized and vice-versa, E_{bb}" is to be used. The only values thus affected are E_o, E_b, and E_k. E_o, instead of being the voltage across R_L, is now, however, the output voltage swing. The resistance at the plate of the flip-flop is now the parallel combination of R_L and the R_x, R_y sum.

If the "on" tube's bias is not zero, no corrections need be applied to the chart. In designing for a negative "on" tube bias, the values of the resistances R_L and R_k are determined by E_o ' E_{bb} and E_k ' E_{bb}, and by the I_b of the tube at the E_b 'E_{bb} and the negative bias desired.

3.0 Example

An example in the use of the chart in designing a fast operating, high-reliability, flip-flop to drive heavy 7AK7 gate tube loads is given below.

For fast operation large switching currents are required, the amount being limited by the plate dissipation of the tube to be used and the stability required. The supply voltages are limited by the output voltages required, the tube and component wattage ratings, and the stability required.

Since large tube currents are wanted, it would be advantageous to operate the tube close to zero bias up to the allowable plate dissipation. Since, however, tube reliability is a must, if the tube is operated in that region then some provision for grid current must be made for low I_b tubes. In the type of circuit shown in Figure 1, if grid current were to be drawn, the high impedance divider arm would collapse, resulting in flip-flop failure.

A low-impedance cathode-follower divider (Figure 2) would, on the other hand, provide a grid-current source for low I_b tubes. In addition to allowing positive bias on an "on" tube, the cathode-follower isolates the flip-flop from the load, allows heavier loading, and yields faster resolution times.

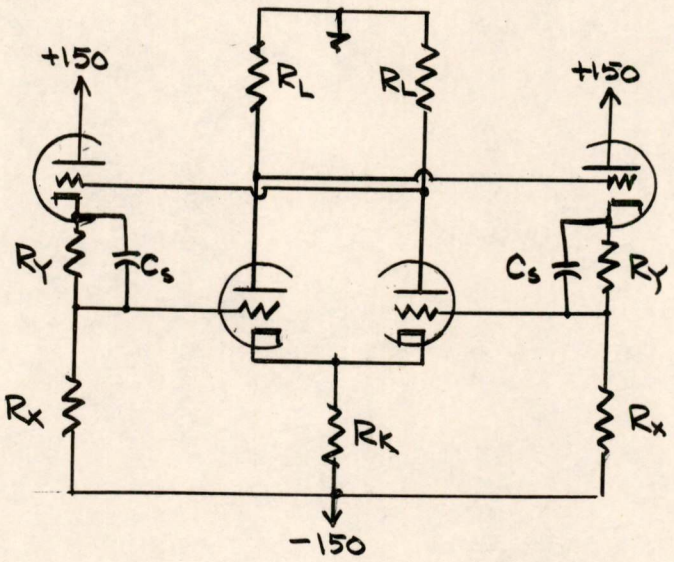


Figure 2

The required output voltage swing of the flip-flop, if it is to drive 7AK7 gate tubes, is at least 0 to -15 volts (d-c coupled). To allow poor tubes, and large component and supply voltage tolerances, an output swing of from a slightly positive value to around -30 volts should be sufficient. Allowing for a bias of about -5 volts at the cathode follower on the low side of the flip-flop, the drop across R_L should be about 35 volts, hence $E_o \cong 35$ volts.

A 5965 duo-triode is very adaptable to reliable high-speed flip-flop applications due to its high plate dissipation, high transconductance, high cut-off μ (μ_o), and liberal internal spacing. For these reasons it will be used for both the flip-flop tube and cathode-follower tube.

The allowable plate dissipation of each triode section was given as 1.5 watts. If the cathode follower output is to be as high as ground, and 2 watt or less resistors are to be used, the supply voltages could be as high as +150 and -150 volts. Thus the plate dissipation at 10 ma. would be 1.5 watts, and 1.5 watts will be dissipated in the divider.

Since the output voltage is to go negative from ground, the plate resistors are returned to ground. E_{bb}, is, therefore, 150 volts.

For supply voltage variations of around 20% or more, large resistor tolerances, and poor tube tolerability, a stability factor of about 3 should be sufficient. The larger the stability factor, the larger

the over-all flip-flop tolerances.

Summarizing: $E_{bb} = 150$ volts

$s \cong 3$

$E_o \cong 35$

tube type = 5965

From the plate characteristics of the 5965:

$$\mu_o = 150/5 = 30$$

Hence s/μ_o for $s = 3$ would be

$$s/\mu_o = 3/30 = .1$$

As the fastest operation at this stability factor is desired, the flip-flop operating point should be on or near the "line of maximum s/μ_o with fixed E_b' ".

With $E_o = 35$:

$$E_o' = E_o/E_{bb} = 35/150 = .23$$

At the intersection of $s/\mu_o = .1$, and $E_o' = .23$ the following can be read from the chart: (Note that the intersection is slightly below the "line of maximum s/μ_o for fixed E_b' ".)

$$E_k' = .3$$

$$E_b' = .47$$

$$R_d = .43$$

Hence:

$$E_k = .3\ (150) = 45 \text{ volts}$$

$$E_b = .47\ (150) = 70 \text{ volts}$$

At $E_c = 0$, $E_b = 70$, an average 5965 (from characteristics) can deliver 10.5 ma.

Therefore:

$$R_k = 45/10.5 = 4.3 \text{ K (RMA)}$$

$$R_L = 35/10.5 = 3.34 \text{ k} \cong 3.3 \text{ k (RMA)}$$

The minimum value of $R_x + R_y$, for 150 volts drop at 10 ma cathode-follower current, would be 15k.

If $R_d = .43$, then:

$$R_d = R_x/R_y = .43 \qquad R_x + R_y \geq 15k$$

$$R_x = .43\ R_y \qquad 1.43\ R_y \geq 15k$$

$$R_y \geq 15/1.43 = 10.5k$$

The nearest higher RMA size to 10.5k is 11k, hence:

$$R_y = 11k$$

$$R_x = .43\ (11k) = 4.74K$$

$$\cong 4.7K \text{ (RMA)}$$

Now

$$R_x + R_y = 15.7k$$

And

$$R_x/R_y = .427 \cong .43$$

Solving this circuit for s, taking into account the cathode-follower biases, results in an s of 3.02.

Note, however, that by moving the operating point of the flip-flop up to the "line of maximum s/μ_o with fixed E_b' " only changes E_b' by .04, and gives a gain in stability. The change in E_b by this movement is only

$$\Delta E_b = .04\ (150) = 6 \text{ volts}$$

At $E_b = 64$ volts, $E_c = 0$, an average 5965 could deliver 10 ma. Hence, moving the operating point to the intersection of $E_o' = .23$ with "the line of maximum s/μ_o with fixed E_b' " yields the following:

$$E_k' = .34$$
$$E_b' = .43$$
$$R_d = .51$$

At 10 ma I_b, then:

$$R_k = (.34)\ 150/10 = 5.1K \text{ (RMA)}$$

$$R_L = 34/10 = 3.5k \overset{a}{=} 3.6k \text{ (RMA)}$$

$$R_d = .51 = R_x/R_y \text{ but again } R_x + R_y \overset{\geq}{=} 15k$$

hence,

$$R_x = 5.1k,\ R_y = 10k \text{ (both RMA)}$$

Solving this circuit for s, taking into account the cathode-follower biases, results in an s of 3.7. The chart gives an s/μ_o of .12, and therefore an s of 3.6.

The former circuit is not as reliable as the latter, although the former would have better triggering characteristics. Preferring the latter for its higher reliability, the flip-flop as it now stands is shown in Figure 3 below.

Although this completes the demonstration of the use of the chart in designing a high-reliability, fast-operating, heavy-loading flip-flop, I should like to take advantage of the opportunity here afforded to give better operating characteristics to the flip-flop.

For faster rise times and sharper output waveforms, the plate resistors may be brought to a higher voltage and clamped to ground. To keep the same flip-flop operating point, however, the plate resistors

would have to be made sufficiently larger to yield the same equivalent circuit at the plates of the flip-flop tube; i.e., same voltage and current at the plates.

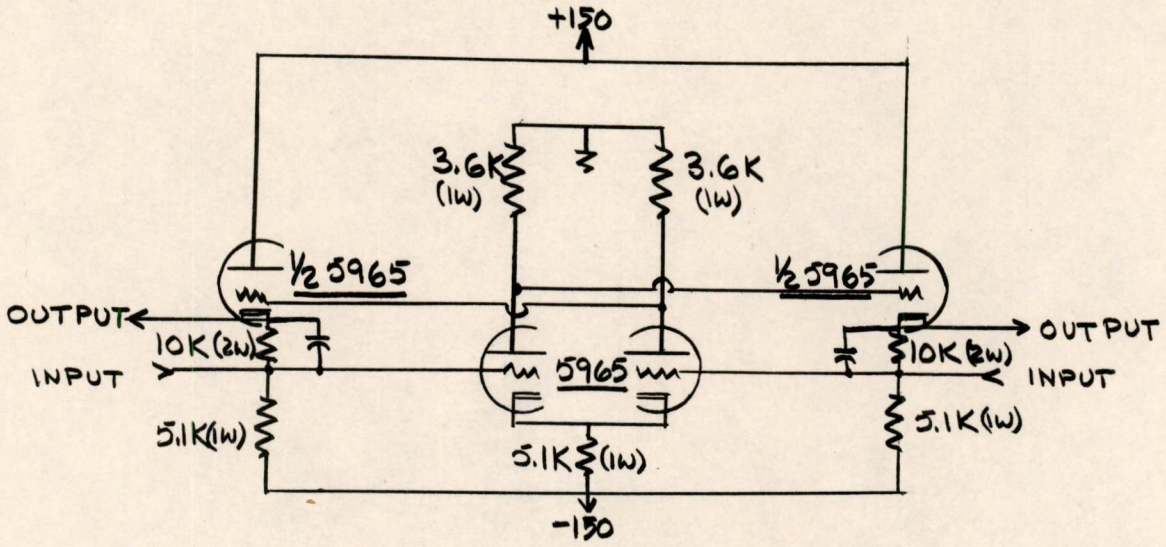


Figure 3

Hence, if +150 is to be used for this purpose, Figure 4a should be made equivalent to Figure 4b.

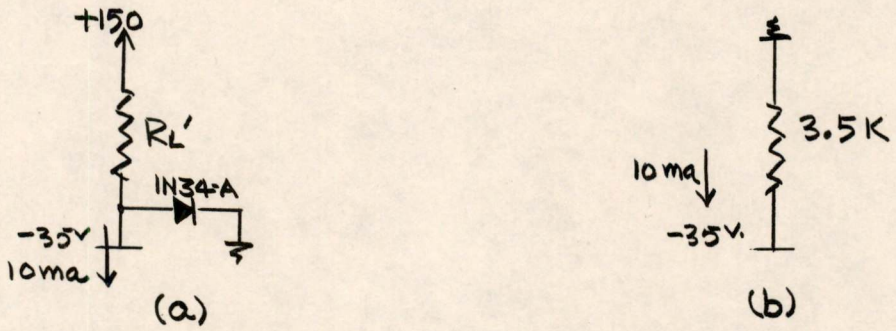


Figure 4

If the back resistance of the diode in Figure 4a can be as low as 50k, then to make the circuits equivalent:

$$150 + 35 = R_L' \left(10 - \frac{50}{36}\right)$$

or

$$R_L' = 185/8.6 = 21.5k$$

In which case, the "on" tube would have to deliver 7 ma (150/21.5) before there would be any output change. An inherent danger in this particular arrangement is that both diodes can be closed concurrently. The flip-flop would then have three stable states; i.e., either tube on, and both tubes partly on.

To alleviate this possibility, the diode switching current should be made sufficiently low, so that the poorest tube allowable is just sufficient when "on" to let the "off" tube conduct no more than switching current. Thus there will be only two distinct output levels.

From these considerations, the following plate load was derived, (Figure 5). This plate circuitry allows the output to start to +19 volts,

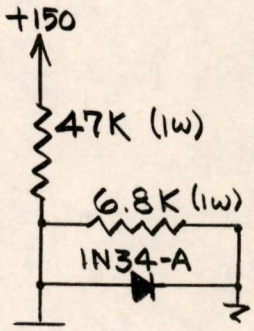


Figure 5

but clamps it at ground, yielding fast rise times and sharp corners in the output waveform. A diode-switching plate current of 3.2 ma allows up to 3.2 ma grid-current for the cathode followers, and allows the "off" tube to deliver 3.2 ma before affecting any output change on that side. In addition to these advantages is another not quite as noticeable. If negative triggers are to be inserted at both flip-flop tubes' grids, for complementing, and the flip-flop plates were not clamped, relatively large negative pips would be seen in the upper output waveform before its

transition. Clamping the plates of the flip-flop tube to ground, clamps the cathode-followers' grids to ground and allows less change on the cathode, and hence output, during the complementing trigger. Complementing on the grids with negative triggers has the distinct advantage of causing a delay in the transition of the flip-flop relative to the trigger. This is mostly due to the triggers' attempting to hold both tubes off, although secondary delays are present. The delay in switching the output levels is approximately equal to the trigger pulse width, and thus affords good counting characteristics. Additional delay and less output pip could be accomplished by inserting a small choke in the plate of each cathode-follower tube, although this would tend to increase the rise and fall times.

Signed H W Boyd
Hal W. Boyd

Drawings:
SA-48395-G

Approved R. L. Best
R.L. Best, Section Leader

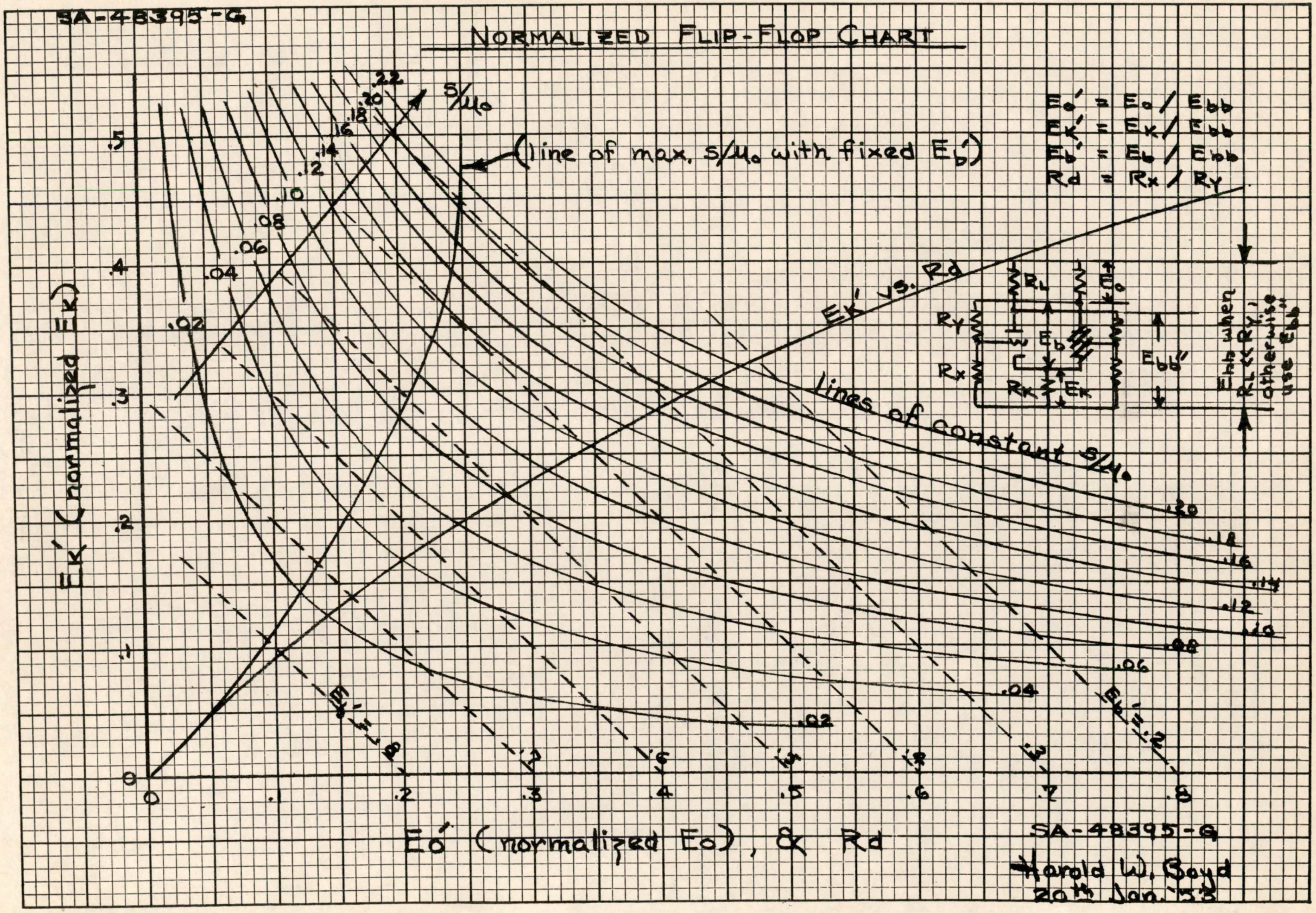
Approved N H Taylor
N.H. Taylor, Group Leader

HWB/cs

Drawing attached:
SA-48395-G

SA-48395-G

NORMALIZED FLIP-FLOP CHART



SA-48395-G

Harold W. Boyd
20th Jan. '33