

Project Whirlwind  
Servomechanisms Laboratory  
Massachusetts Institute of Technology  
Cambridge, Massachusetts

SUBJECT: PRELIMINARY TESTS ON THE FOUR-CORE MAGNETIC-MEMORY ARRAY

To: 6345 Engineers

From: W. N. Papian

Date: June 18, 1951

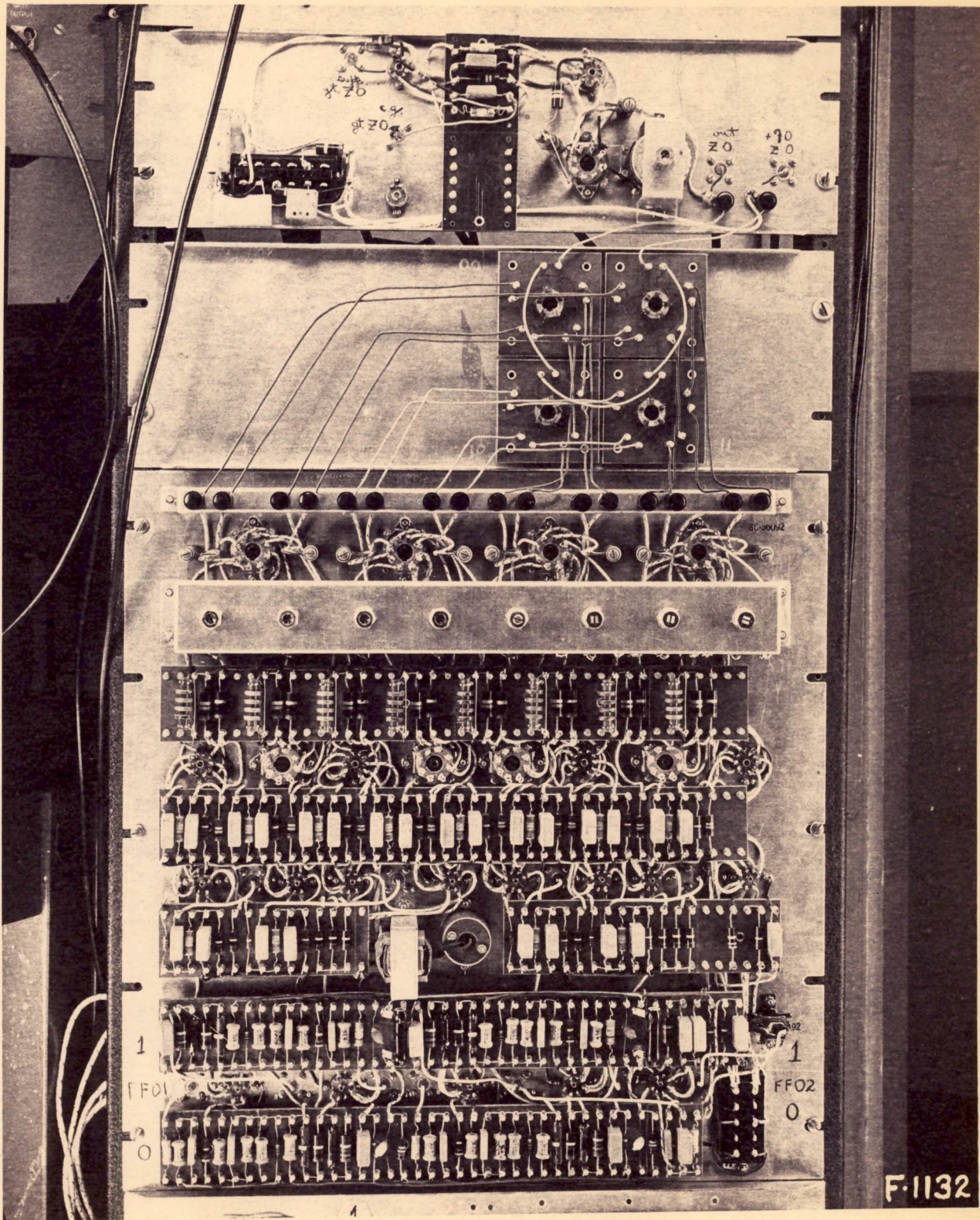
Abstract: Successful operation of a four-core magnetic-memory array indicates the soundness of a multi-coordinate storage and selection scheme. The ability of one core to retain information in the face of an unlimited amount of disturbing activity was tested, and current-variation margins determined.

Brief Description

A four-core magnetic-memory array was built to demonstrate the principle of multi-coordinate storage and selection. It consists of four cores arranged in a square, with cores selected by the choice of x and y coordinates. The windings which determine whether a binary ONE or ZERO is written in the selected core are, like the sensing windings, connected together in the four-core plane and act, to some extent, like a z coordinate of a three-coordinate array.

The surrounding equipment consists of some more-or-less standard test equipment, two specially built panels containing the x and y flip-flops and the gating and driving circuitry associated with the coordinate axes, and some miscellaneous panels adapted for this problem. Figure 1 is a photograph of the cores and part of the rest of the equipment.

Two basic modes of operation have been tried. The first, in which an information pattern was cycled indefinitely around the four cores, was successfully run but has been abandoned in favor of the present mode. The operating mode now in use resembles an elementary spot-interaction test as used by the storage-tube group. It consists of writing a binary digit in a given core, then operating around the other cores for a large number of cycles in a manner intended to "disturb" (tending to destroy) that information, finally returning to read the contents of the given core. This mode has also been run successfully.



F-1132

FOUR CORE, TWO-DIMENSIONAL  
MAGNETIC MEMORY TEST SETUP

FIG. 1

### Logical Design

In the logical layout of the equipment as used in the first basic mode of operation, a given information pattern was cycled around the four cores. It was possible for the oscilloscope to "look at" the sensing output from the array (or any portion of the array) (1) each time a selected piece of information was being handled, or (2) each time a selected core handled information. The piece of information in (1), or the core in (2), could be selected by push button while any pattern of information was cycling around the array.

The limited value of a test which renews the information in a core after only two or three disturbances (caused by activity elsewhere in the array) made it desirable to drop this first basic operating mode (information cycling) and subject the cores, instead, to a spot-interaction type of test which assessed their ability to retain information in the face of an unlimited amount of disturbance.

Refer to Figure 2 (by R. P. Mayer) for the present scheme of operation. With the switch positions as shown, the setup is ready to test the ability of core 00 to hold a ONE. The multivibrator frequency divider is allowed to run free and becomes a source of synchronous high- and low-frequency pulses. After corrective short time delays, the pulses are fed into the system. The low-frequency pulse first goes to gate and delay unit 3a and thence to trigger the oscilloscope. It then passes through coder 1 to preset flip-flops 1, 2, 3, 5, and 6 to ZERO, ZERO, ZERO, ONE, and ZERO respectively. The first of the block of high-frequency pulses emanating from the pulse-block former passes through switch 2 and gate 2 and sets FF4 to a ZERO. One read-write cycle is performed on core 00 from read-write control (gate 8 is on), after which FF3 is set to a ONE (turning off gate 8), to remain that way until the major cycle is over and another low-frequency pulse comes along. The skip circuit sees to it that core 00 is not selected again for the rest of the major cycle, and gate 8 prevents any writing activity for the same period. The opening of switch 7 momentarily during operation ensures that a ONE is written into core 00. This core may be selected either once for every low-frequency pulse (once each major cycle - binary counter set to  $2^0$ ), every 2 or 4 major cycles (binary counter set to  $2^1$  or  $2^2$ ), or once each time a button on the push button synchronizer is pushed (switch 1 open).

The ability of core 00 to hold a ZERO is tested by reversing switches 2 and 3 and momentarily closing switch 6 during operation. The selected test core may be other than 00, as determined by the settings of switches 4 and 5.

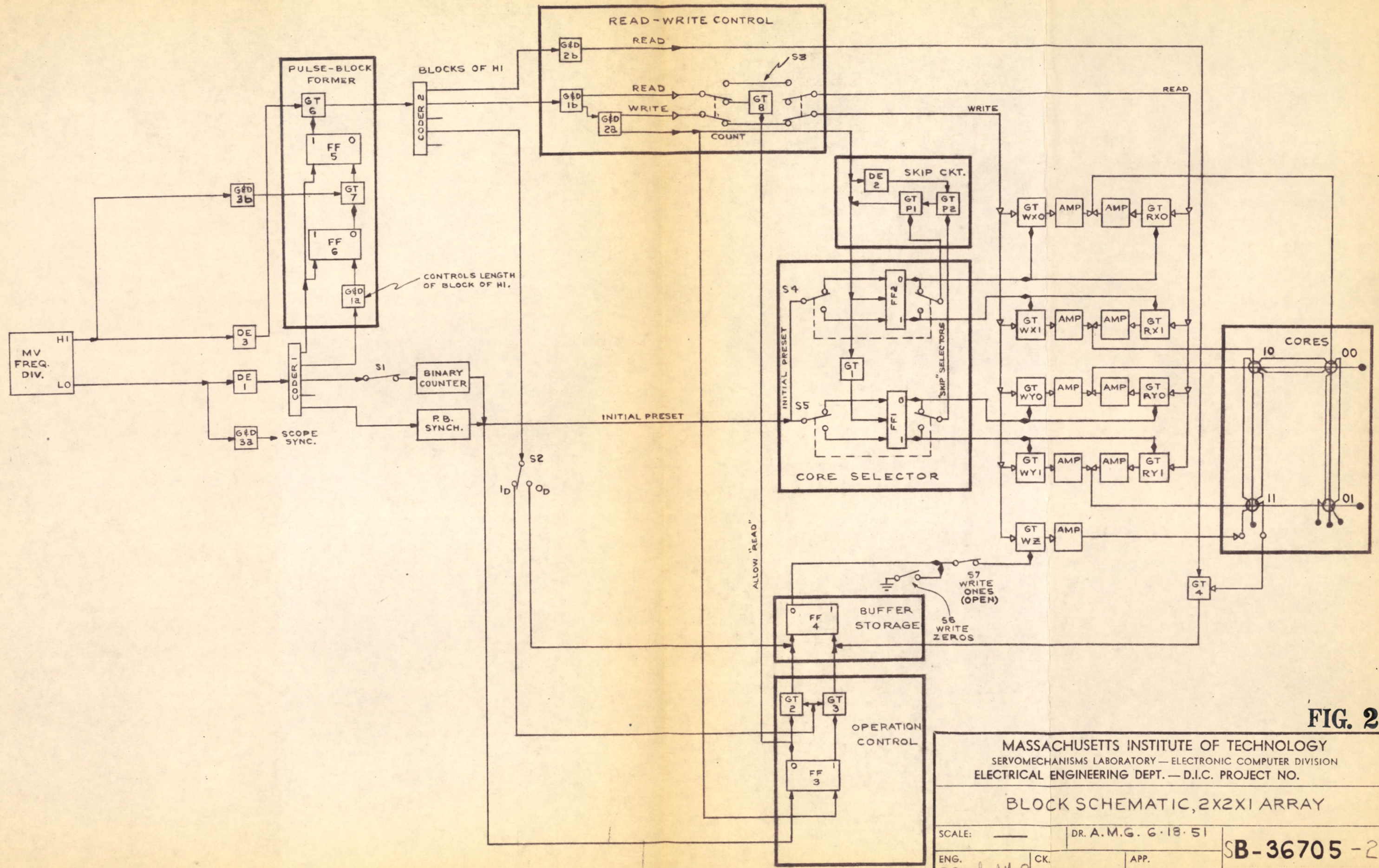


FIG. 2

MASSACHUSETTS INSTITUTE OF TECHNOLOGY  
 SERVOMECHANISMS LABORATORY — ELECTRONIC COMPUTER DIVISION  
 ELECTRICAL ENGINEERING DEPT. — D.I.C. PROJECT NO.

BLOCK SCHEMATIC, 2X2X1 ARRAY

SCALE: \_\_\_\_\_ DR. A.M.G. 6-18-51

ENG. RPM by WHP CK. APP. SB-36705-2

### The Cores

The cores now in this array are designated as MTS 6464 by the supplier, the Allegheny Ludlum Steel Corp. They consist of 10 turns of Silectron tape 1 mil thick and 1/8 inch wide; the resultant rings have a mean length of 4.24 cm, a cross-sectional area about 0.01 sq cm, and an inside diameter of 1/2 inch. They are encased in slightly oversized plastic containers, and wound with five 25-turn windings and one 10-turn winding of #30 magnet wire.

The material Silectron is a standard electrical sheet steel with a special anneal designed to produce the B-H characteristic of Figure 3. The successful metallic core used in the experimental work on individual cores (see Report R-192) was made of the same material.

### Circuitry

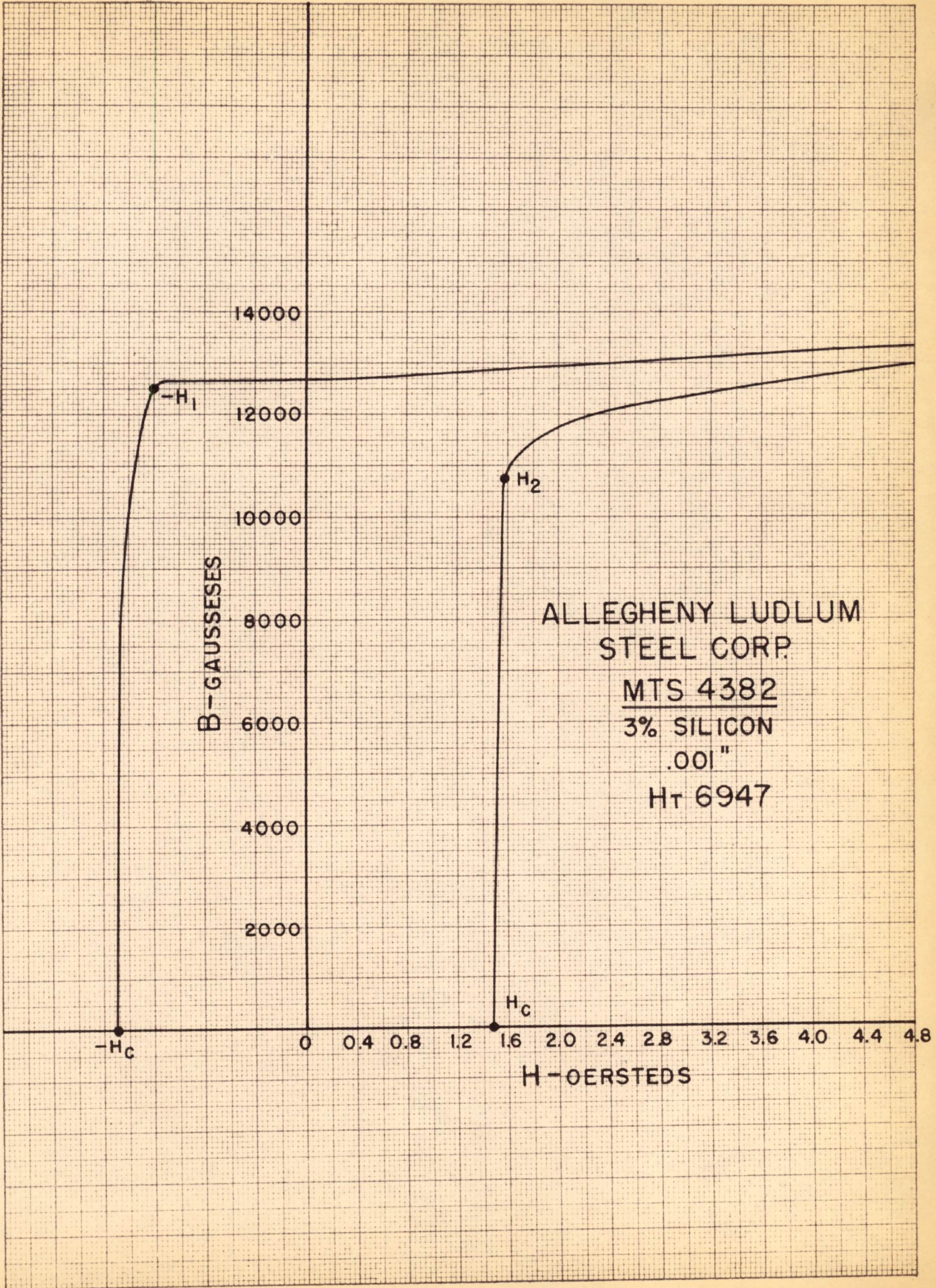
The 25-turn magnetizing windings on the two cores comprising one selecting coordinate are connected in series with a 100-ohm resistor as the plate load of one section of a 6AS7. The resistor makes it possible to "look at" the current flowing through the windings. A 500-ohm rheostat in the cathode circuit of the 6AS7 section is used to vary that current. The 6AS7 section is driven by one section of a 2C51 which inverts the waveform coming from the 6AS6 gate tube. Figure 4 shows one channel of the nine in use. The 6AS7 section puts from about 40 ma to just under 1/4 amp. through the core windings, depending on the cathode rheostat setting. The rise time of the current waveform is well under 1/2 microsecond; it may be lengthened by shorting the choke in the plate load of the 2C51 and adding some capacitance.

The fifth 25-turn winding on each core is the sensing winding; the four of them are connected in series-aiding to deliver the output from the array. The 10-turn windings are connected with alternating polarities for a special test.

### Results and Conclusions

In general, operation was stable and with good margins.

The adjustment for optimum operation was decided in an arbitrary manner as the compromise between signal ratios and response times that seemed most promising. Figure 5 summarizes these results. It shows the effect of disturbing activity (interaction) on information retention. Disturbed-signal ratios, for different amounts of disturbance, may also be derived from these scope traces.

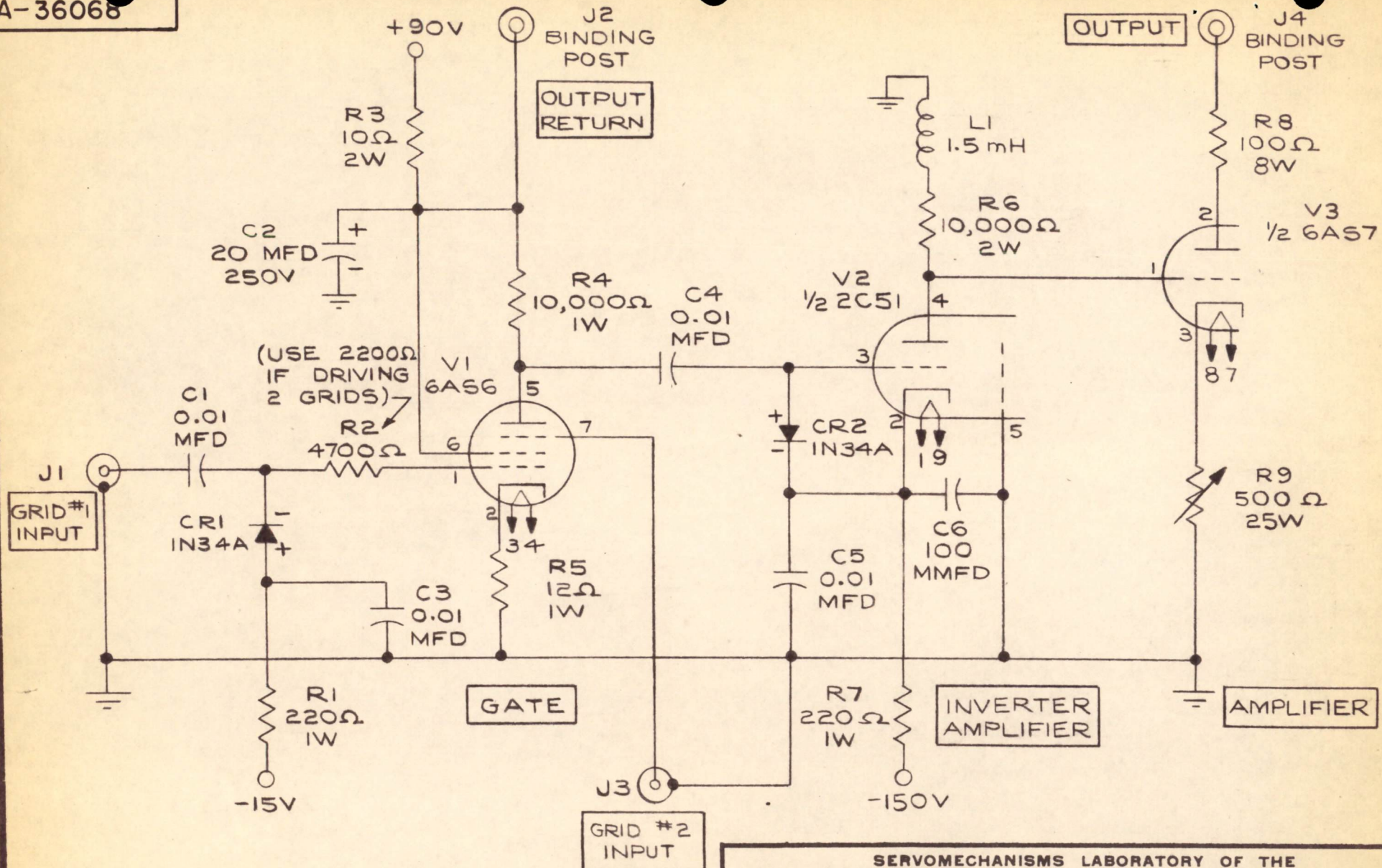


KEUFFEL & ESSER CO., N. Y. NO. 8887-140  
Millimeters, 3 mm. tubes accepted. cm. lines heavy.  
MADE IN U. S. A.

A-38999 - G

FIG. 3

A-36068

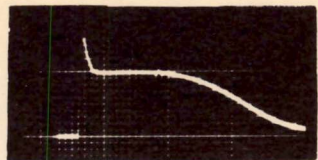


SERVOMECHANISMS LABORATORY OF THE  
**MASSACHUSETTS INSTITUTE OF TECHNOLOGY**  
 DIVISION OF INDUSTRIAL COOPERATION PROJECT NO. 6345

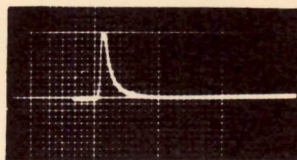
**CHANNEL OF 2x2x1 ARRAY**

SCALE: —	DR. M.M. 5-15-51	<b>A-36068</b>
ENG. <i>whp</i>	CK.	

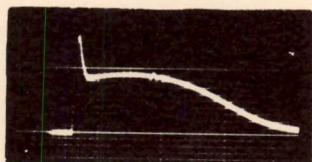
FIG. 4



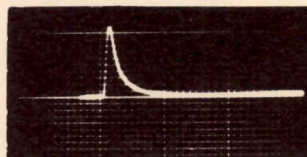
(a) AFTER 0 READ CYCLES



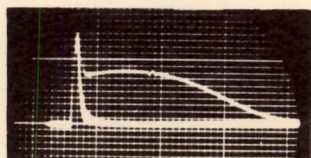
(d) AFTER 0 READ CYCLES



(b) AFTER 50 READ CYCLES

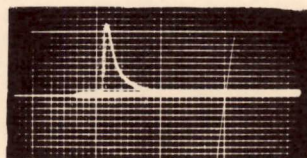


(e) AFTER 50 READ CYCLES



(c) AFTER 400 READ CYCLES

5μs



(f) AFTER 400 READ CYCLES

ONE-RETENTION

ZERO-RETENTION

(THE OUTPUT SIGNAL FROM THE ARRAY UPON SELECTION OF CORE 00 — AFTER A NUMBER OF READ CYCLES AROUND THE REMAINING THREE CORES)

(THE OUTPUT SIGNAL FROM THE ARRAY UPON SELECTION OF CORE 00 — AFTER A NUMBER OF WRITE-ONE CYCLES AROUND THE REMAINING THREE CORES)

EFFECTS OF DISTURBING ACTIVITY ON INFORMATION RETENTION

A-36886  
F-1349



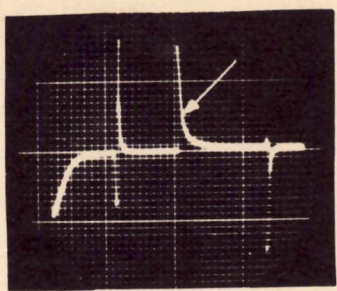
Most of the deterioration of information occurs in the first few cycles of disturbing activity; as much reduction in the output of a ONE occurs during the first 50 cycles as during the following 350 cycles (compare a, b, and c of Figure 5); almost all of the increase in the output of a ZERO occurs in the first 50 cycles (d, e, and f). When the setup was operated by push button, there was no significant deterioration beyond 400 cycles of disturbing activity.

The disturbed-signal ratio, as taken on an area basis from Figure 5, is about 7; taken on an amplitude basis at 6 or 7 microseconds after the start of the pulses, it is much higher and becomes difficult to determine because the ZERO output has dropped by then to too low a value to measure.

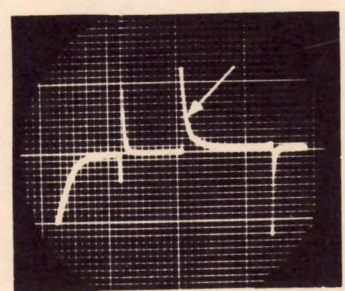
Figure 6 indicates the results of using alternating-polarity sensing coils for the reduction of non-selecting noise. This noise is just the output from those cores which are in the same row or column as the selected core, and, consequently, receive half-value magnetizing-force pulses. When the windings are connected in series (aiding) the non-selecting pulses all add to the output from the selected core, the most serious effect being to increase the size of the ZERO output. The difference in amplitude of the ZERO output pulses (indicated by small arrows) is a measure of the effectiveness of alternating the polarities of sensing windings. The difference would be much larger in a large array.

One form of marginal check on the stability of operation of the array was made. It consisted of lowering and raising the amplitudes of the currents through the selecting windings, and observing signal ratios. It was found that all coordinate currents could be raised above an arbitrary optimum setting by 20% before signal ratios became marginal, and by 25% before the information patterns became completely unstable. Currents could be lowered to 20% below the optimum setting, at which point operation became unstable in the surrounding equipment and response times became about 35 microseconds. It was possible to hold the coordinate currents to within  $\pm 5\%$  of each other during these tests.

The main result of the preliminary tests on the four-core array is verification that the scheme of multi-coordinate storage and selection with magnetic cores is fundamentally sound. The unit is not as basic a tool as the single-core (coincident-current) tester, but it makes a fair demonstrator for the scheme. Design, development, and operation of a significantly larger array (at least 64 cores) is needed



(a) SERIES AIDING




(b) SERIES ALTERNATING

20  $\mu$ s

PARTIAL CANCELLATION  
OF NON-SELECTING NOISE

A-36885  
F-1348

in order to assess the ultimate practicability of arrays containing thousands of cores. Such work should be done on a design level aimed at Whirlwind standards in order to assure that pertinent problems will be uncovered and solved.

Signed.....  
W. N. Papian

Approved.....  
R. R. Everett

WNP:ap

Drawings:

- A-50015
- SB-36705-2
- A-38999-G
- A-36068
- A-36886
- A-36885

Olsen

6345  
Engineering Note E-409

Project Whirlwind  
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SUBJECT: RATIONAL SELECTION OF VACUUM TUBE TYPES FOR COMPUTER APPLICATIONS

To: Electronics Group

From: H. B. Frost

Date: July 6, 1951

Abstract: A primary object of computer design is reliability. To obtain reliability, the proper kind of vacuum tubes must be used. To this end, a factor of merit, which relates plate current steps to grid voltage steps, has been developed to aid in selecting tube types. Oxide cathode current limitation must be considered when designing circuits and selecting tube types. Grid current, which may be caused by emission, gas, or leakage is also important in determining designs. Other factors to be considered are envelope temperature, type of circuit, general ruggedness, and life test experience. Because of the great difficulty in determining the best tube types for computer use, standardization is imperative.

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## 1.0 General Design Criteria and Introduction

For computer applications, the criteria for good system design may be stated very simply. Completed circuitry should be as reliable as possible consistent with a reasonable power consumption. In general, this criteria implies that the design be relatively simple, without excess numbers of tubes and components. Moreover, conservative operation of the vacuum tubes and components also follows, as does the requirement that the circuits be operable with a wide variety of tubes of the types for which the circuits are designed. The foundations for these considerations lie in the slow variation of the characteristics of vacuum tubes and components when properly operated. If the permissible variations are great and the rates of variation slow, a long period of trouble-free operation may be expected. Other things being equal, simple designs are preferred over complex designs because of the smaller number of random absolute failures of any given kind of component. Such failures may be reduced, but not completely eliminated. Increased complexity brings an increased number of components, which probably will bring an increase in these random failures. Thus, the ideal design is simple, allows wide variations in components, and operates the components at conservative ratings.

Selection of vacuum tube types for computer use depends on two general characteristics of the vacuum tubes to be used; these are the ability of a new tube to do the job required and the length of time a given tube will last. While these characteristics are considerably affected by the skill of the circuit designer, they are even more affected by the vacuum tubes used. One important characteristic of new tubes is the relative amount of plate current which can be switched by a given grid pulse. As this characteristic is not ordinarily tabulated in characteristic sheets, a table has been prepared. Good design dictates that a vacuum tube not be overloaded; cathode life may be seriously shortened if overloading is practiced. In miniature and sub-miniature tubes which normally have a rather hot bulb under rated conditions, overloading can be particularly serious.

Consideration of grid return impedance in circuit design requires knowledge of the tube to be used. Every tube has a critical value of grid return impedance; if this impedance is exceeded, instability results. In pulse amplifiers where low frequency response must be very good to prevent tilt of gate tops, consideration of grid circuit impedance may be very important in the circuit design.

It might be thought that operation in a stationary computer would not require particularly strong tubes; however, this is not so. Tubes must be handled without damage, and shorts must be absolutely prevented. Thus, rather stringent requirements are placed on close-spaced, high-performance, computer tubes. For computer tubes similar to the 6SN7 and other low-performance types, requirements may be relaxed somewhat, thanks to the increased spacings.

## 2.0 A Factor of Merit for Tubes in Switching Applications

### 2.1 Factors of Merit in General

The use of factors of merit for the selection of vacuum tubes for use in certain circuits is very well known. The  $\mu$  of a triode for audio amplifier use is very well known as a factor of merit, as is the  $G_m$  of a pentode for the same application. Somewhat more subtle is the gain-bandwidth product commonly used to describe wide-band amplifier tubes. Another ratio which may be used as a factor of merit is  $\frac{G_m}{I_b}$

which determines the ultimate gain obtainable in a pentode amplifier at audio and sub-audio frequencies. None of these are of great use when selecting vacuum tube types for current-switching applications, where one desires to control the maximum amount of current with a minimum grid swing.

### 2.2 The Step-current Factor of Merit

A factor of merit ordinarily permits the comparison of the most important parameters for any given application, thus the first thing to be established is the exact ratio of parameters to be calculated. In computer circuits of the type used in Whirlwind, the tube capacities are frequently not the governing capacitive elements in the circuit. At any rate, the circuit strays must always be considered when calculating total capacity. Thus, in establishing this factor of merit, the tube capacities will not be considered. Given the amount of plate current which can be obtained when the grid is driven a fixed amount above cut-off, voltages can then be calculated using known tube capacities and capacities peculiar to the circuit.

To a reasonable approximation, the plate current of a triode may be described by

$$1) \quad I_b = \frac{G}{(1 - \mu)^{3/2}} (E_b - \mu E_c)^{3/2}$$

where  $I_b$  is the plate current;  $G$ , the perveance;  $E_b$ , the plate voltage;  $\mu$ , the grid one mu-factor, and  $E_c$ , the voltage on the grid.

If one calculates from (1) the current available when a given pulse  $\Delta E$  is applied to the control grid with the tube in a nominally cut-off condition

$$2) \quad I_b = \frac{G \mu^{3/2}}{(1 \neq \mu)^{3/2}} (\Delta E)^{3/2}$$

The product  $G \left( \frac{\mu}{\mu \neq 1} \right)^{3/2}$  is defined as the step-current factor of merit and is tabulated for various tube types in Tables 1 and 2. These tables also show  $\mu$ ,  $\frac{G}{\mu \neq 1}$  and tube capacities for ready reference when needed. Triodes are listed in Table 4; pentode and tetrode types are included in Table 2. For pentodes and tetrodes, the  $\mu$ -factor is that of grid 1 to grid 2, and the influence of the plate voltage on plate current is assumed negligible. While this approximation is by no means satisfied completely, the errors introduced are not so great as to invalidate the factor of merit calculations.

Differentiating with respect to  $E_b$  and back-substituting to eliminate the parenthesis,

$$3) \quad \frac{G}{(1 \neq \mu)^{3/2}} = \frac{\left( \frac{2}{3} \frac{\partial I_b}{\partial E_b} \right)^{3/2}}{I_b^{1/2}}$$

Similarly,

$$4) \quad G_m = \frac{3}{2} G^{2/3} \frac{\mu I_b^{1/3}}{\mu \neq 1}$$

The use of (3) allows easy evaluation of  $\frac{G}{(\mu \neq 1)^{3/2}}$ , as the partial derivative  $\frac{\partial I_b}{\partial E_b}$  can be determined readily either directly or graphically from characteristics. For pentodes and tetrodes,  $E_{c2}$  should be substituted for  $E_b$ .

The limitations on this factor of merit are the same as those on equation (1). In the first place, there is always a contact potential which enters (1) inside the parenthesis. Initial emission velocity is also important. The effect of this contact potential and other imperfections in (1) make the grid appear to be about 0.5 to 1 volt more positive than the actual potential. This effect does not change the factor of merit in any way, but must be considered when calculating plate currents.



A second and more serious effect is the change in  $\mu$  as the space current varies. As the space current of a vacuum tube is reduced by increasing the grid bias, the plate and screen voltage remaining fixed, the  $\mu$  of the tube is also reduced, although at a much slower rate than the space current. This effect is especially pronounced in vacuum tubes with spacings of 10 mil or less between grid and cathode, and it is these tubes which are of the greatest interest to anyone interested in a maximum increment of plate current with a given grid swing. This change in  $\mu$  is caused by a variation in the location of potential minimum (virtual cathode) between the grid and the cathode. For low currents, the minimum moves nearer the grid plane.

A basic limitation imposed by thermodynamic considerations exists on the ratio of  $G_m/I_b$ . For vacuum tubes operating with cathode temperatures near  $1000^\circ$  K (oxide cathodes), this limit is about 11,000  $\mu$ hos/ma. However, (4) which was derived from (1) implies

$$5) \quad \frac{G_m}{I_b} = \frac{2}{3} G^{2/3} \frac{\mu}{\mu - 1} I_b^{-2/3}$$

Equation (5) predicts that the ratio  $G_m/I_b$  will be infinitely high at zero plate current, and that the slope with respect to reciprocal plate current will be  $2/3$  on a log-log plot. While this ratio increases in all tubes as  $I_b$  is reduced (in the normal range of  $I_b$ ), the slope is not  $2/3$ , but somewhat less. The limit of 11,000  $\mu$ hos/ma is not approached very closely; the best values are about  $1/3$  this limit, and many types of tubes do not approach within  $1/10$  of the limit. Therefore, the cutoff is somewhat more remote than predicted by equation (1), and currents predicted for the application of a specified pulse to grid one while the tube is cut-off will be greater than the currents actually observed. "Cut-off" as used above means that bias at which the plate current has just stopped flowing for all practical purposes, recognizing the fact that this point is very much dependent upon the kind of measuring instruments used to indicate the plate current.

In addition practical limitations are imposed by the inevitable variations of actual vacuum tube geometry from the designed geometry. Such imperfections as bent grid turns, bowed cathodes, and non-uniform spacing all place limits upon how closely a given vacuum tube will conform to the ideal characteristics for its type.

### 3.0 General Limitations on Oxide-coated Cathodes

In order to obtain the high performance which is required in vacuum tubes for an electronic computer of the WWI type, uni-potential oxide-coated cathodes are necessary. To apply these tubes intelligently, some understanding of cathode limitations is desirable.

One of the more important limitations on oxide-coated cathodes is the limit on d-c drain. Ordinarily 50 to 100 ma/cm<sup>2</sup> is the maximum allowable continuous current density. (The cathode area of a 7AD7 is approximately one cm<sup>2</sup>.) As diode life tests have been run for many thousand hours at current densities of 500 ma/cm<sup>2</sup>, it is reasonable to believe that this limitation is not inherent in the oxide-coated cathode, but that it is the result of contamination of tubes with films on various electrodes and residual gases. As a consequence of the construction and processing methods used, it is very nearly impossible to obtain excellent vacua in receiving tubes; the nickel and copper parts which are always present will not stand rigorous outgassing procedures.

However, if average currents are kept down, the current density during 0.1 microsecond pulses may be very much higher than the permitted d-c currents. No difficulty has been experienced in 7AD7 buffer amplifiers which may have pulse current loadings of 0.5 amp or a little more in some circuits. In many tube types, cathode current densities of 0.5 amp/cm<sup>2</sup> can not be put to good use at permitted screen and plate voltages; where these currents can be obtained and used within rated voltages, there appears to be no reason to expect that 0.1 microsecond pulses at low duty factors will damage a cathode.

While oxide-coated cathodes are subject to many ills, only two have been recognized as causing trouble in receiving tubes used by this project. Perhaps the most serious type of trouble is the formation of a cathode interface resistance. This resistance forms in tubes using cathodes with "active" nickel cathode-base material, which contains more than 0.05% silicon. Formation is an aging process which begins to be important after about a thousand hours, more or less. Although interface resistance formation can not be avoided completely if the cathode base is active nickel, the size of the interface resistance may be minimized by operating the cathode at relatively heavy d-c loadings and by avoiding excessive cathode temperatures. However, it appears that even cathodes which have been operated with a heavy d-c drain for several thousand hours will develop a high interface resistance

if operated with no drain for a few hundred hours. Only one way is known to prevent the formation of troublesome interface resistance under all conditions of operation; that is the use of vacuum tubes with passive, low silicon (0.01% or less) cathode-base material. Even passive cathode-base material may not be sufficient when high cathode temperatures (1200°K) are used.

One other serious cathode trouble has appeared in some types of tubes. This is patch poisoning of the cathodes. This trouble is indicated when it is found that, although the cathode current of an afflicted tube is low, the cathode current is not greatly influenced by variations of the cathode temperature. Thus, parts of the cathode retain normal activity, while other parts have very little activity. This type of cathode deterioration has been observed mostly in tubes with heavy d-c cathode loadings. Uniform poisoning of vacuum tube cathodes will also cause low cathode current, but the cathode current is then very sensitive to cathode temperature. Moreover, tests made at conditions which normally show relatively small cathode currents may indicate very little deviation if the cathode has been uniformly poisoned to a higher work function material. These behavior differences enable one to differentiate between these two types of poisoning.

It is very possible that cathode poisoning is hastened by improper operation of the afflicted tube. Manufacturers' ratings of plate voltage, screen voltage, and electrode dissipation should be strictly observed in order that cathode life be as long as possible. Data presented by Dr. McNally of Bell Laboratories at the recent Atlantic City Conference on Vacuum Tubes for Computers indicated that operation below these maximum ratings frequently will extend vacuum tube life. Conservative operation pays off.

It is well known that the life of oxide-coated cathodes is critically dependent upon the operating temperature. If operated too hot, cathodes will lose material too rapidly by sublimation and evaporation; if operated too cool, they very likely will be poisoned by residual gases and decomposition products. For any given vacuum tube operating condition, an optimum cathode temperature exists; this temperature is somewhat different for different operating conditions. Because vacuum tube characteristics are subject to greater change at low temperatures than at high temperatures for a given cathode condition, most tubes which are allowed a 10% variation in heater voltage will have cathodes which run somewhat hotter than necessary at design center in order to maintain good performance when the heater voltage is 10% low. Since

a cathode which is run hotter than necessary will have shorter life than a cathode which is operated at the correct optimum voltage, it appears reasonable that tubes with a wide tolerance of heater voltage will have longer life if the heater is operated at a voltage two to five percent below rated mean heater volts. To verify this statement for a particular tube type would require very extensive life tests lasting over a period of years; life tests of this type are best made in operating equipments rather than in life racks.

#### 4.0 Grid Current in Vacuum Tubes

Grid current in standard vacuum tubes is usually due to one or more of three things: gas, primary grid emission, or leakage. Whatever the cause, grid current places a limit on the value of grid return impedance which may safely be used. Electron capture by the grid is also important when a tube is operated at zero bias; this current opposes those mentioned above. As a vacuum tube is aged, shifts in the contact potential of the grid and other changes cause electron capture to become unimportant unless the grid is driven positive.

Gas ion current to a negative vacuum tube grid is approximately proportional to the space current in the tube and to the gas pressure. As a tube is aged, the gas pressure increases. In a well-gettered tube, the residual gas is likely to be mostly helium with some nitrogen; other gases will be removed by the getter or the cathode. Gas currents in tubes such as the 7AD7 at normal class "A" conditions will be somewhere near  $5 \times 10^{-8}$  amps after the tube has operated for a few hundred hours, but will rise as the tube is aged until they may be somewhere near  $5 \times 10^{-7}$  amps after 5000 hours.

Leakage and primary grid emission are extremely variable sources of grid current which are important in some types of tubes, in particular the 6AN5. For primary grid emission to exist, two conditions must be present; the grid must be hot and it must be contaminated. A hot grid is usually found in a tube with close spacing between the grid and a flat cathode and with relatively long grid laterals of small diameter which prevents cooling by conduction. Ordinarily, a cathode is very good source of barium contamination, especially when the cathode is based on active nickel. Grid emission may be reduced by gold-plating grid one; this is done in practically all close-spaced tubes ( $G_1 - K$  0.005" or less). If grid emission current is important, the grid-cathode impedance must be reduced to prevent runaway circuits.

Leakage within a vacuum tube is almost always a symptom of contamination. The contaminated part may be the header or the mica. Two important sources of contamination exist in the getter flash and the cathode, but both may be controlled by proper vacuum tube design. To prevent getter contamination, it is necessary to locate properly and to shield the getter. As this is well known, leakage from getter contamination is rare. Contamination from the cathode is generally sublimed material, barium and nickel. Magnesium in the active-type cathode-base materials has been found to be very serious in inducing sublimation. Use of normal and passive cathode-base materials usually reduce sublimation to a low level. Passive materials in particular have been found effective in this respect when sublimation is critical. In receiving-type vacuum tubes, it is frequently possible to slot the micas between adjacent elements to lengthen the leakage paths and thus to reduce leakage.

Grid circuit impedance must be watched in particular when close-spaced miniature tubes such as the 6AN5, 6AK5, and 6AH6 are being used. Grid currents are also apt to be very high when the 7L5B is considered. To use excessive grid return resistance is to invite instability as tubes age and gas pressure increases.

#### 5.0 Some Consideration of the Effects of High Bulb Temperature

There are several harmful effects of high envelope temperatures which are important in vacuum tube applications. In the first place, high temperatures will cause the glass to become more active, and gases may be liberated by diffusion from within the glass more easily. Surface-adsorbed gases may also be liberated. Power tubes operating at frequencies of about 50 mc and higher must have relatively cool envelopes between output electrode seals to prevent high dielectric loss in the glass and runaway heating. Occasionally, extreme hot spots are formed on the envelopes of high voltage rectifiers (2X2A) due to electron bombardment. Envelopes may be punctured in this way.

The above considerations are not all-or-none, but merely relative. Because of differences in the glass used, miniature vacuum tubes may operate at higher temperatures than standard T-9 (GT size) tubes without damage. However, it is easier to overload a miniature than it is a T-9 sufficiently to cause excessive bulb heating. Miniature power tubes, for example the 5687 (T-6 $\frac{1}{2}$ ) and the 6AN5 (T-5 $\frac{1}{2}$ ) operate at bulb temperatures of 150°C or better at rated load. Only small increases in these temperatures

are sufficient to induce trouble. For this reason, it is very important not to shield a miniature power tube with the RMA standard shields used for r-f tubes, as these shields raise the bulb temperature very considerably. Some checks on 5687 tubes showed an increase from 160° C to 230° C when shields were installed.

It has been found that even 160° C is too high for 5687 tubes when one side is operated on and the other off. The "on" side retains its normal cathode condition during this type of operation and the "off" side retains very nearly normal pulse emission when checked occasionally. However, a d-c test of the normally "off" side after 500 hours of operation causes very rapid poisoning of its cathode and a consequent reduction in plate current. The cathode will reactivate if current is drawn for a period of time (less than 500 hours, but not definitely established). If the bulb is cooled with a fan during operation, so that the maximum temperature is not more than 135° C, this poisoning does not occur. Because of this poisoning effect, the use of 5687 tubes for flip-flop operation is not recommended. Operation in circuits where one section may be cut off for long periods of time is not recommended unless tubes can be kept well cooled. Cathode followers and other circuits where tubes are not cut off completely should not be affected by this poisoning.

The cause of the poisoning effect is presumed to be a deposit on the normally "off" anode which is decomposed by electron energy when the anode is caused to draw current. The decomposition products then poison the cathode.

When subminiatures are used, proper cooling is even more important. Difficulty has been experienced with oxidation of leads in the SC-968B tubes used in video probes even though the bulb temperatures appear to be reasonable for this type of tube. Convection cooling is ordinarily not enough for subminiatures; conduction to close-fitting shields which may dissipate their heat into large radiating areas of metal is a preferred condition.

It should be mentioned that no trouble has been experienced in 6AN5 tubes operated on JAN life and in a d-c flip-flop. It seems that envelope temperature is not a limiting condition in this tube type as normally operated. Plate current remains normal after 8000hours.

## 6.0 Consideration of Kind of Tube For Certain Applications

There sometimes exist circuits where either a triode or a tetrode could be used. In general, triodes with grid input-plate output are not suitable for wide band circuits; Miller effect capacitive loading is apt to be intolerable. However, some cathode follower circuits demand a decision between a triode and a triode-connected tube. Where there are a large number of cathode-follower sockets to be filled, a triode is preferred to a triode-connected tube (provided that a triode of suitable ratings exists), since the simpler construction will probably give less trouble, quality factors being equal. Where only a few cathode-follower sockets are to be filled, standardization considerations indicate that a triode-connected pentode or tetrode is preferred, unless a suitable triode is already used in a moderate number of other sockets.

It is very desirable that an amplifier for 0.1 usecond pulses in many computing circuits be a quasi-standardizing circuit, so that, as long as the input pulse is above a certain value, the output will be constant. This is a particularly desirable condition in an amplifier which drives gate tubes. One of the best ways to obtain such a condition is to drive the amplifier to saturation, using plate limiting. There is then no sensitivity to input amplitude within a reasonable range, nor is there sensitivity to any tube characteristic other than the plate limiting characteristic. For this type of service, a pentode is not suitable. A good plate limiting characteristic demands a very sharp knee in the plate current-voltage characteristic at high values of plate current -- 200 ma and more. Only tetrodes such as the 6AN5, the 6Y6G and the 3E29 possess suitable characteristics. However, recent tests have shown that a 7AD7 may be tetrode-connected (suppressor to plate) to obtain a suitably-sharp plate-current knee for plate limiting. As usually pentode-connected, a 7AD7 is very unsuited for pulse amplifier work with a very uncertain knee at high values of plate voltage.

It should be pointed out that the knee of the plate current-voltage characteristic is not usually controlled in production, except that it must not rise above a certain maximum plate voltage at a given plate current. The control is ordinarily on plate resistance. Because of this lack of production control, it is desirable that tubes used as plate-limiting amplifiers have as low-voltage knees as possible. If low-voltage knees are used, variation in knee position will cause less change in amplifier output than the same percent variation at higher knee voltages.

Since the knee is determined by the gross geometry within the tube, very little change can be expected with life, so that a plate-limited should be stable for long periods of time.

In some cases, screen degeneration is attempted to stabilize circuit characteristics with tube aging changes and with different vacuum tubes. This is a very poor idea. In most vacuum tubes, the ratio of plate to screen current is controlled very loosely, with maximum and minimum values on both plate and screen current, but with no specification of the ratio. Moreover, there is no guarantee that the ratio will remain constant throughout life. Aligned-grid tubes (6L6G, 6Y6G, 3E29, and 7AK7) are particularly poor, both with respect to initial uniformity and changes with life. In 6L6G's and 6Y6G's, the ratio of plate to screen current may cover a range of three to one for normal new tubes. When degeneration is required, coupling around the tube or use of cathode degeneration may be expected to give much better results in the long run.

#### 7.0 General Ruggedness and Construction of Vacuum Tubes

If a vacuum tube could be installed in a vibrationless computer and removed only when failure had occurred, general ruggedness and strength would be no problem. However, this is not the case. Even under the best circumstances, some vibration is present. Moreover, marginal checking techniques are not infallible, so that occasionally good vacuum tubes will have to be tested and returned to service. Tubes must be strong enough to stand handling without developing shorts, broken welds, and gas. Shorts can be so much of a problem in a computer that it is desirable that all tubes to be used are given rigorous shorts and leakage tests before being installed. Rugged tubes reduce the losses at this stage of testing.

A comparison of the 6AG7 and the 7AD7 constructions might be somewhat informative. These two types are quite similar, with the 6AG7 having higher perveance and the 7AD7 having higher  $\mu$ . The step-current factor of merit for both is 2.9, which is the highest available in small pentode power tubes.

A recent cathode change has been made in the 6AG7 which has not been fully evaluated. This change should improve 6AG7 life and reduce the tendency to leakage in old 6AG7's. However, the 7AD7 has slotted micas, which has been noted above as a method for increasing leakage resistance. The 7AD7 uses larger grid side rods and laterals and has an extra control grid radiator. Active elements are built into a rugged close-fitting shield which is connected very directly to the external pin connection. In



the 6AG7, the shell is connected to pin one only through a small getter tab, which adds considerable inductance. Although shown on old 6AG7 drawings, no internal shield is used in new tubes. The fact that the shell and suppressor are tied together in the 6AG7 reduces the possible connections which may be made to the suppressor, since the shell must be near ground for safety reasons. In cases where the suppressor can not be grounded, as in many cathode follower and flip-flop applications, the 6AG7 shell also can not be grounded. The 7AD7 is not so restricted, so that the internal shield, corresponding to the 6AG7 shell, may be at any potential not more than a few volts positive to the cathode. This flexibility proved important when it was necessary to ground this shield to remove overshoot from flip-flop plate waveforms.

There are two respects in which the 7AD7 is inferior to the 6AG7. In the first place, the zero-bias plate current of the 7AD7 is lower than that of the 6AG7 because of somewhat greater grid spacings. This plate current deficiency would not have been important if circuits had been designed for the characteristics of actual production tubes; however, the circuit designs were made originally for 6AG7 tubes and modified for pilot production of 7AD7 tubes. Changes were made in putting the tube into production which reduced the zero-bias plate current without changing the primary design characteristic for television,  $G_m$ . Circuits designed to work with 32 ma tubes are not so good when 25 ma tubes must be used. In the second place 7AD7 tubes as received have a relatively large number of tap shorts, most of which appear to be associated with lint.

It is expected that both of these defects will be corrected in the SR 1407, which is being developed as a replacement for the 7AD7 in computer applications.

For some applications, it is desirable to use miniature tubes to save space or, occasionally, to obtain performance not otherwise available. Miniatures are very desirable for use in high-performance low-level amplifiers where capacities must be low and transconductance high. Another possible application might be to non-critical applications where space is a factor. At the present time premium miniature tubes are available in ARINC types; however, these are expensive and procurement is difficult. Notwithstanding difficulties, the advantages of these ARINC types are sufficient that they should be used in new design whenever applicable. Although electrical performance life is not well known, reports indicate that shorts and opens in these ARINC types are practically non-existent.

Miniatures by their very nature are apt to be fragile in two places, pins and tips. These troubles may be alleviated to a great extent by proper engineering. Pin troubles have been attacked during the years since the war, and very few tubes made recently are troublesome in this respect. Tips are fragile if long and extenuated; proper tipoff will produce short stubby tips which are not so easily broken. Reducing breaking tendencies is particularly important when tubes must be handled for repeated testing. Miniatures are at an advantage when strength of internal structures is considered; short, compact, mounts firmly fixed to the button header make them relatively rugged.

Numerous studies of heater burnout have shown that high-voltage, low-current heaters such as those used in tubes designed for series operation across the line are much more prone to burnout than the heaters used in standard 6.3 volt tubes. To minimize heater troubles, it is desirable that receiving types with standard heaters rather than high-voltage heaters be used.

Although very little information is readily available about the heaters used in oxide-coated cathodes, the heater is a very important part of the tube and frequently may be the limiting factor on life. Heaters are made of tungsten wire coated with alumina to prevent contact with the cathode. Heaters may be folded with four or six legs, or they may consist of one or more double helices. Since heater-cathode shorts, one of the most important types of heater failure, are more likely in tubes using folded heaters, the coiled helix type is preferred, but is seldom used except in power tubes and in some kinds of premium tubes. Heater-cathode shorts and some heater opens may be encouraged by the large relative motion which occurs when folded-type heaters are turned on. One company (Bendix) is now using ceramic tubes in addition to alumina to insulate the heater from the cathode. This special construction is restricted to rectifier tubes with very high heater-cathode voltages. Experience with Whirlwind has indicated that heater troubles can be reduced to a very low incidence by slow application of heater power, which reduces thermal shock.

## 8.0 Summary and Conclusions

It has been seen that many factors should be considered before vacuum tube types may be selected with confidence for computer use. Moreover, with a little care, various circuits may be divided into groups, each of which has similar tube requirements. When this is done, it is then possible to select a relatively small group of tubes which will satisfy almost all the circuit requirements of a computer. This is the philosophy which was used when WWI was designed; it is a very good one when

carried through completely. The result of the above procedure, of course, is standardization of vacuum tube types.

Standardization on as broad a base as possible is very important. Almost all computers have internal standardization, but there has been extremely little standardization between computers as yet. Selection of tube types for computers which will both satisfy circuit requirements and give reliable performance is a difficult job. Once a good type for a given job has been found, it is desirable to concentrate on that type, encouraging the manufacturer to remedy minor defects. Cleaning up one or two tube types is much, much easier than cleaning up ten or a dozen, and manufacturers are much more willing to attempt the former, because of the higher potential demand per type. At the present time, practically every power tube of the receiving-tube lists is being used by one or another computer; this chaotic situation is not designed to encourage manufacturers to improve tubes for computer use.

Even though external standardization between different development groups can not be attained at present, there are many benefits to be derived from internal standardization within a group such as the Whirlwind Project. If a large number of tubes of a single type are used, it is much easier to persuade a manufacturer to devote some effort to cleaning up this type, both for project use and for sale to others. This is particularly so if the project is in a position to assist the manufacturer in his development efforts for their mutual benefit. If a large number of types are involved, neither the project nor the manufacturer can concentrate efforts sufficiently to obtain improvements. Stocking, testing, and procurement procedures are considerably simplified when only a minimum number of types are involved.

Incidentally, "premium" vacuum tubes costing up to about ten times the cost of corresponding receiving types are very likely to be bargains in the long run. Savings occur in two places -- because of lower testing costs and less down-time in the computer. Testing costs are of three types; direct costs of testing a tube before installation, costs of testing tubes which prove defective before installation, and costs of testing questionable tubes from the computer. When tubes of poor quality or out of specification are involved, the cost of testing tubes which can not be used may be more than the cost of testing the tubes actually used. This is the case with production 7AD7 tubes at the present time, where three or four tubes must be tested to find one suitable for the standard flip-flop. Computer down-time costs are not

known to the author, but it seems that removal of a tube, even when marginal checking is used, may well cost several dollars. These dollars might better be spent on tubes with twice or three times the life of standard tubes, if such premium tubes are available.

Up to very recently, premium tubes have not been available. Only one series of so-called premium tubes has been available for any length of time, the RCA RED Series. These tubes are not suitable for high-speed computer applications because of the low performance of the prototypes. However, a few of the 5692 type (6SN7 prototype) have been used in some test equipment applications. These tubes were defective in life because of leakage and interface resistance troubles. (Changes have since been made which should eliminate these troubles.)

Premium miniature tubes are being manufactured under the ARINC program by both Raytheon and General Electric; other companies may also be working on these types. While these types are very desirable, (prototypes of interest are 6AK5, 6AL5, 12AU7, 2C51) they are not readily available at this time. The RCA computer series (5915, 5963, and 5964, based on 6BE6, 12AU7, and 6J6) is also interesting. Of the above types, only the ARINC 5654 (6AK5 prototype) can be regarded as a high-performance (low capacity, high factor of merit) tube useful in high-speed computers. However, the 6AN5 made by Raytheon, and the 5687, made by Tungsol, may both be regarded as premium high-performance miniature types. The 5687, when received, is extremely well balanced as to plate current and cutoff between the two sections of the tube. However, there is no reason why the two sections should stay balanced for a long period of operation. While this tube will make an excellent triode flip-flop, poisoning considerations mentioned earlier indicate that a 5687 flip-flop left in one position for a long period of time would become unstable. Life tests have shown that the 6AN5 makes an excellent flip-flop. A rugged and long-lived 6AN5 would be a premium tube indeed for computer applications; life seems quite satisfactory when compared to most standard types, but the structure is prone to shorts, and to some changes in characteristics.

If the complement of WWI is examined, it is seen that standardization has been applied reasonably well. Only a few slips stand out. In the first place, six different beam tetrode types are used (6V6GT, 6Y6G, 6L6G, 3E29, 3D21A and 715B). While these types are by no means interchangeable, it would seem that careful design could have eliminated one or more of these

types. Then there are a hundred-odd 6AG7 tubes, along with nearly two thousand 7AD7's. From the differences in these two types, it is somewhat difficult to justify the presence of 6AG7's in WWI. Then there are the pairs, where both the standard and its miniature equivalent are used. Examples are 6X4-6X5GT, 6AC7-6AH6, 6AU6-6SH7, and OA2-OD3. Five 6J5's go along with nearly five hundred 6SN7GT's. Wasting a few half-sections is greatly preferred to adding another tube type. In fairness to designers, it should be realized that many of these duplications of equivalent types are found in purchased equipment which was not designed by project engineers. All in all, there are about forty tube types used in WWI and its associated input-output equipment and power supplies. Better design co-ordination might have reduced this number. Use of less than twenty tube types would seem to make the design of an extremely fast computer rather difficult, but careful selection of types with an idea of the necessary circuit performance might allow this substantial reduction.

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TABLE 1

STEP CURRENT FACTOR OF MERIT AND OTHER CONSTANTS FOR TRIODES

Type	$\mu$	$\frac{G}{(\mu-1)^{3/2}}$	$\frac{\mu}{\mu-1} \frac{3}{2} G$	$C_{gd}$	$C_{pk}$	$C_{gk}$	$P_p$
		<u>ma/volt<sup>3/2</sup></u>	<u>ma/volt<sup>3/2</sup></u>	<u>μuf</u>	<u>μuf</u>	<u>μuf</u>	<u>watts</u>
2C51	30	0.012	2.0	1.3	1.0	2.25	1.6
6AS7G	2	0.53	1.5	-	-	-	14.0
6BL7GT	14	0.032	1.7	4.2	1.1	4.4	10.0
6SN7GT	20	0.009	0.8	3.8	1.0	2.9	2.75
6J4	50	0.019	6.7	4.0	0.24	5.5	2.5
6J6	38	0.009	2.0	1.6	0.4	2.2	1.6
6S4	19	0.02	1.6	-	-	-	7.5
7F8	55	0.045	1.8	1.2	1.4	2.8	3.5
12AT7	65	0.006	3.1	1.6	0.4	2.25	2.8
12AU7	20	0.009	0.8	1.5	0.4	1.6	3.0
12BH7	21	0.0165	1.6	2.4	0.8	3.0	3.5
5687	17	0.035	2.6	3.1	0.45	4.0	4.2

Factor of Merit

TABLE 2

STEP CURRENT FACTOR OF MERIT AND OTHER CONSTANTS FOR PENTODES

Type	$\mu$	$\frac{G}{(\mu-1)^{3/2}}$	$\frac{\mu^{3/2}}{\mu-1} G$	$C_{out}$	$C_{in}$	$P_{G2}$	$P_p$
		<u>ma/volts</u> <sup>3/2</sup>	<u>ma/volts</u> <sup>3/2</sup>	<u><math>\mu\mu f</math></u>	<u><math>\mu\mu f</math></u>	<u>watts</u>	<u>watts</u>
6AC7	44	0.015	4.4	5.0	11.0	0.45	3.3
6AG7	22	0.028	2.9	7.5	13.0	1.5	9.0
6AH6	44	0.015	4.4	3.4	10.0	0.45	3.3
6AK5	30	0.01	1.6	2.85	3.9	0.55	1.85
6AN5	11	0.065	2.5	4.5	9.0	1.55	4.6
6AQ5	10	0.03	0.9	6.0	7.6	2.2	13.2
6AU5G	5.9	0.14	2.0	7.0	11.3	2.5	10.0
6AU6	43	0.0075	2.1	5.0	5.5	0.65	3.0
6BG6G	8.0	0.055	1.5	6.5	11.0	3.5	25.0
6CD6G	3.8	0.27	2.0	10.0	26.0	3.0	15.0
6L6G	8.0	0.048	1.1	9.5	11.5	2.75	21.0
6V6GT	10.0	0.03	0.9	9.6	9.5	2.2	13.2
6Y6G	5.7	0.12	1.6	15.0	11.0	2.0	14.0
7AD7	25.0	0.023	2.9	7.5	11.5	1.2	10.0
404A	37.5	0.031	7.1	2.9	7.1	0.75	3.0
715B,C	6.5	0.21	3.5	12.0	37.0	-	-
807	8.0	0.05	1.1	7.0	12.0	3.5	25.0
829B	9.0	0.07	1.7	6.95	14.5	3.5	20.0

Factor  
of Merit

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Project Whirlwind  
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Massachusetts Institute of Technology  
Cambridge, Massachusetts

SUBJECT: SELECTION SYSTEMS FOR MAGNETIC CORE STORAGE

To: William N. Papian

From: Robert R. Everett

Date: August 7, 1951

Abstract: Several core-selecting systems can be devised that offer better selection ratios than the standard 3-dimensional array. Improved selection ratios result in reduced storage access time but at the cost of considerably increased complexity of the driver circuits.

INTRODUCTION

A storage system using a 3-dimensional array of magnetic cores has been under study in the laboratory for some time.<sup>1,2</sup> It is assumed that the reader is familiar with the system as described in the above references.

Very promising progress has been made, especially recently. It is still essentially true that neither the steel nor the ceramic cores now available present a satisfactory solution to the storage problem:

- a. The steel cores have the proper rectangularity but switch too slowly.
- b. The ceramic cores switch rapidly but are not sufficiently rectangular.

Both situations can be improved if the ratio of selecting to non-selecting  $H$ 's can be increased.

- 
1. R-187, "Digital Information Storage in Three Dimensions Using Magnetic Cores" by J. W. Forrester.
  2. R-192, "A Coincident Current Magnetic Memory Unit" by W. N. Papian

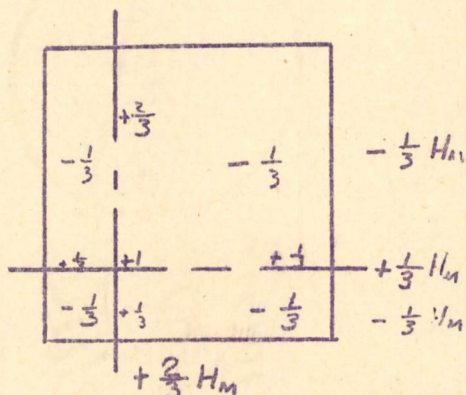
- a. For the steel cores the non-selecting H can remain as is and the selecting H increased to decrease the switching time.
- b. For the ceramic cores the switching H can remain as is and the non-selecting H reduced to improve signal-noise ratio, etc.

The switching system described by JWF is simple, elegant and "best possible" 3-dimensional in a sense to be defined later. Nonetheless it appears worthwhile to consider switching systems that result in improved selecting ratios even though they may result in more selecting equipment.

A 2-Dimensional System with a 3:1 Selecting Ratio

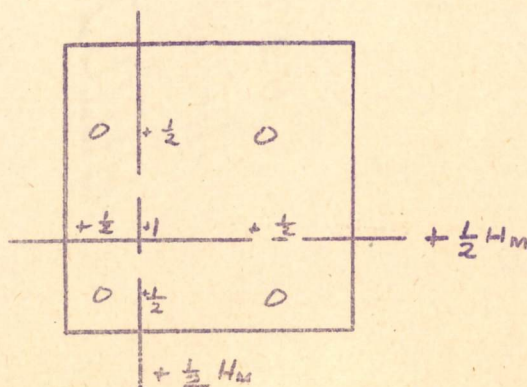
A 2-dimensional system can be arranged to give a 3:1 selecting ratio. The currents to be applied in the two coordinates are as follows when  $H_M$  is the drive required to switch:

X coordinate selected	apply $+2/3 H_M$
" " unselected	" 0
Y coordinate selected	" $+1/3 H_M$
" " unselected	" $-1/3 H_M$



X	Y	$H_X$	$H_Y$	H
0	0	0	$-\frac{1}{3}$	$-\frac{1}{3}$
0	1	0	$+\frac{1}{3}$	$+\frac{1}{3}$
1	0	$+\frac{2}{3}$	$-\frac{1}{3}$	$+\frac{1}{3}$
1	1	$+\frac{2}{3}$	$+\frac{1}{3}$	+1

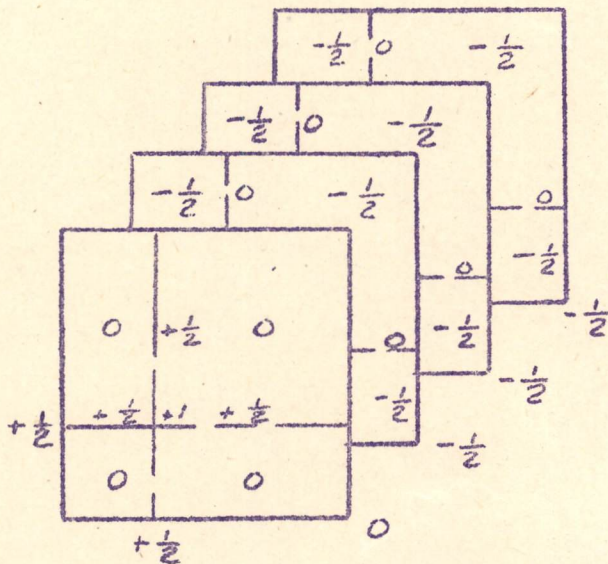
Comparing this system with the present one described in R-187:



X	Y	$H_X$	$H_Y$	H
0	0	0	0	0
0	1	0	$+\frac{1}{2}$	$+\frac{1}{2}$
1	0	$+\frac{1}{2}$	0	$+\frac{1}{2}$
1	1	$+\frac{1}{2}$	$+\frac{1}{2}$	+1

3-Dimensional 2:1

The virtue of the last mentioned system appears when another coordinate is added:



X	Y	Z	H <sub>X</sub>	H <sub>Y</sub>	H <sub>Z</sub>	H
0	0	0	0	0	$-\frac{1}{2}$	$-\frac{1}{2}$
0	0	1	0	0	0	0
0	1	0	0	$+\frac{1}{2}$	$-\frac{1}{2}$	0
1	0	0	$+\frac{1}{2}$	0	$-\frac{1}{2}$	0
0	1	1	0	$+\frac{1}{2}$	0	$+\frac{1}{2}$
1	0	1	$+\frac{1}{2}$	0	0	$+\frac{1}{2}$
1	1	0	$+\frac{1}{2}$	$+\frac{1}{2}$	$-\frac{1}{2}$	$+\frac{1}{2}$
1	1	1	$+\frac{1}{2}$	$+\frac{1}{2}$	0	+1

One way of looking at this system is to say that selection is made in all Z planes and then the unwanted planes are overridden or inhibited by a negative H.

There is no equivalent inhibition scheme for the 3:1 system. This lack is a serious restriction since the minimum usable switching system for a parallel computer is 3-dimensional. The absolute minimum is 2-dimensional, one dimension along the digits in a register, the other along the registers. For large numbers of registers the register selection, which is one-dimensional, becomes prohibitive. Note that digit column selection is necessary to allow arbitrarily writing 0's or 1's in each column. The present 3-dimensional system is satisfactory from this point of view since it allows selecting any combination of cores along the Z axis and not just one.

A 3-dimensional system allows 2-dimensional selection of the register number thus reducing the number of drivers to a reasonable level for moderate storage capacities. For very large storage capacities it may be desirable to go to 4- or more-dimensional systems. This possibility lies well in the future.

N-Dimensional Switching

We will consider the problem of selecting a single element from an n-dimensional array of such elements. The selection will be made in the following manner:

1. The selection will be made by n independent linear selections, one in each coordinate.
2. Each linear selection will be of an n-1 dimensional-array.
3. Each element will be at the intersection of n selecting leads, one for each coordinate.
4. The particular selecting arrangement that results in maximizing the ratio of selecting to non-selecting switching signals will be defined as a "best-possible" n-dimensional switching system.

(These restrictions hold for what may be termed "non-redundant" selection systems. Some systems with "redundant" selection are described in the next section.)

Let the selecting amplitude ( $H_M$  in Papian's terminology) be taken here as unity drive, and let p be the largest non-selecting amplitude at any core. Now consider a selected core, and then unselect it in one coordinate only; according to restriction (1), above, the other coordinates remain unaffected. Since unselecting must remove a part of the selecting amplitude at least equal to 1-p, unselecting in n coordinates will remove at least n(1-p). As stated, the remaining amplitude of 1-n(1-p) must not exceed p in amplitude; It must not therefore be less than -p since negative disturbance is as bad as positive disturbance. Then:

$$1 - n(1 - p) \geq -p$$

$$1 - n + (n+1)p \geq 0$$

$$(n+1)p \geq n-1$$

$$p \geq \frac{n-1}{n+1}$$

$$P_{Min} = \frac{n-1}{n+1}$$

$$\left(\frac{1}{P_{Max}}\right) = \frac{n+1}{n-1} = R_{Max} = \text{Maximum Selecting Ratio}$$

A tabulation of  $R_{Max}$  and  $P_{Min}$  vs n follows:

$n$	$R_{Max} = \frac{n+1}{n-1}$	$P_{Min} = \frac{n-1}{n+1}$
2	3	1/3
3	2	1/2
4	5/3	3/5
5	3/2	2/3
6	7/5	5/7
etc.		

The present system has a  $p$  of 1/2 and is "best-possible" 3-dimensional but not "best-possible" 2-dimensional. The 3:1 system described above is "best-possible" 2-dimensional.

A 4-dimensional system according to the above criterion would be, for example:

		<u>Coordinates</u>			
		$X_1$	$X_2$	$X_3$	$X_4$
H	=	+.4	+.2	+.2	+.2
or	H =	+.4	+.4	-.4	+.2

These two systems are equivalent; of the two, the latter is preferable since the driving equipment is simplified.

In general for an  $n$ -dimensional system the coordinate values are:

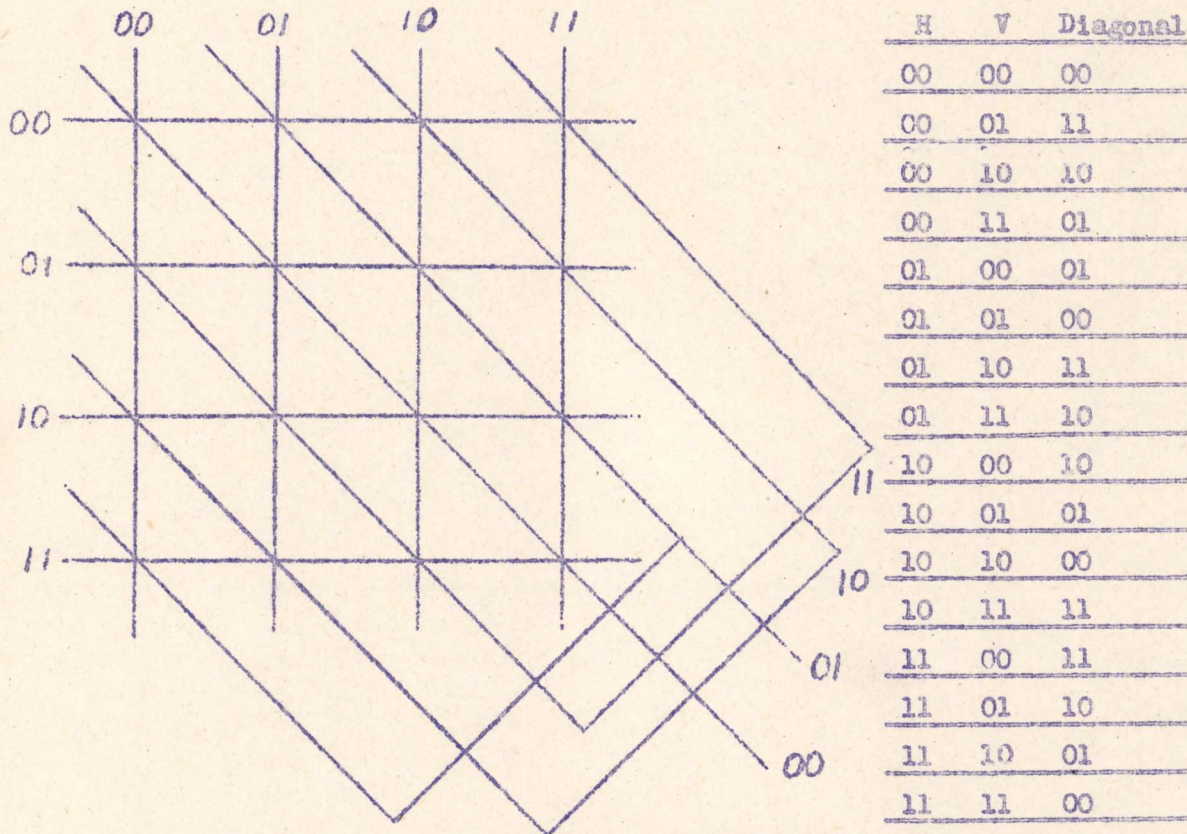
$$\begin{aligned}
 & \begin{matrix} & X_1 & X_2 & X_3 & \dots & X_n \end{matrix} \\
 H = & \quad + \frac{2}{n+1} \quad + \frac{1}{n+1} \quad + \frac{1}{n+1} \dots + \frac{1}{n+1} \\
 \text{or } H = & \quad + \frac{2}{n+1} \quad + \frac{2}{n+1} \quad - \frac{2}{n+1} \dots - \frac{2}{n+1} \quad (n \text{ odd}) \\
 & \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad + \frac{1}{n+1} \quad (n \text{ even})
 \end{aligned}$$

Redundant Selection - 2-dimensional

If the restrictions mentioned at the head of the previous section are disregarded, it is possible to devise selection systems that will give selection ratios higher than 3:1. If a ratio of  $M$  is desired, a system is needed in which the selected element lies at the intersection of  $M$  lines or planes or other configurations which must not otherwise intersect. Since the intersection of just two of these define the element, the

the other  $M-2$  figures are redundant. Moreover, it is in general possible to apply plus or minus voltages to the figures and thus obtain better than an  $M$  to 1 selection ratio.

Consider first a 2-dimensional array. Customarily an element is selected at the intersection of one horizontal and one vertical, not-otherwise-intersecting lines. A third group of not-otherwise-intersecting lines are the diagonals.



The diagonal line cannot be chosen arbitrarily but is a function of the horizontal and vertical lines already chosen. See the table.

The diagonal column may be easily derived from the horizontal and vertical columns by (in this case) subtracting the vertical from the horizontal modulo 4. A physical procedure for this derivation would be:

1. Set the diagonal decoder by the horizontal address digits.
2. Add the complement of the vertical address.
3. Add 1 (corrects for 9's complement).

Since all selected lines are non-intersecting except at one element, a selecting amplitude of  $1/3$  may be used giving an amplitude at the selected element of 1 and non-selecting amplitudes of at most  $1/3$ .

A better system is possible. All unselected elements in the horizontal and vertical lines must be intersected by the non-chosen diagonal lines (they do not intersect with the chosen diagonal and the diagonal lines pass through all elements). Therefore, a negative signal on the non-chosen diagonals will reduce the non-selecting amplitudes. As a result:

X coordinate	chosen	+ 2/5
"	" non-chosen	0
Y	chosen	+ 2/5
"	" non-chosen	0
Diagonal	chosen	+ 1/5
"	non-chosen	- 1/5

The largest non-selecting amplitude is  $1/5$  resulting in a selecting ratio of 5:1.

There are other 2-dimensional redundant systems. Through the selected element may be drawn a large number of lines of different slopes (the number depends on the size of the array) all of which will pass through  $1/n$  th of the elements, but not all of which are non-intersecting with pre-chosen groups of selecting lines. As an example -- for an array with even  $n$ , lines with slope of  $3$  (up 3 rows for each column) will intersect with X, Y, and diagonal lines only at the mutually selected element. Rules can be worked out for choosing such lines. The resulting selecting ratios are  $2m-1:1$  where  $m$  is the number of groups of lines.

Redundant line selection is also possible in 3 or more dimensional arrays but a selection among an  $n-1$  dimensional array of lines is necessary in each group.

In 3 dimensions, the groups could be the 3 coordinates plus the 4 major diagonals. The selected element will be at the intersection of 7 lines. By a method analogous to that described above a selecting ratio of 13:1 may be achieved. The necessary selecting equipment is very complicated and inefficient.

Redundant Selection - 3-Dimensional

Redundant selection is not necessarily restricted to groups of lines. Groups of n-1 dimensional figures may be used in an n-dimensional system.

In 3 dimensions a fourth plane skewed with respect to the major 3 may be used. This plane should intersect with more than one other plane only at the selected element. A plane intersecting the other 3 at  $45^\circ$  fulfills the requirements.

X coordinate	chosen	+ 1/3
"	non-chosen	0
Y	chosen	+ 1/3
"	non-chosen	0
Z	chosen	+ 1/3
"	non-chosen	0
Diagonal	chosen	00
"	non-chosen	- 1/3

Applied Signals

Selected element	1
Intersection of any 2 planes	+ 1/3
All planes except at intersections	0
All other elements	- 1/3

Although this is a 3-dimensional system it has the disadvantage that only a single element can be selected and not an arbitrary group of elements along one dimension.

Redundant selecting 3-dimensional systems using more than 4 planes can be devised. The methods can be extended to any number of dimensions.



The Driving Problem

Any reference to the form of storage under consideration has two parts:

1. A "read" or "write minus", the two being equivalent.
2. A "write plus" in selected columns.

Since the read is destructive a rewrite plus in the columns that readout plus is necessary.

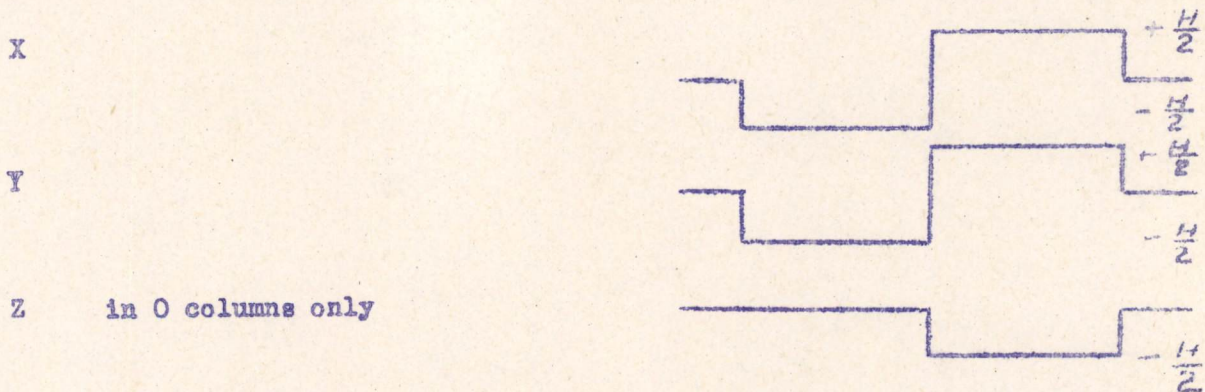
Since writing minus requires signals of opposite polarity on all planes from those required when writing plus, write minus must be carried out at a different time than write plus. This difference can most conveniently be obtained by writing minus or clearing all columns prior to the write plus. This write minus is equivalent to reading. It would be possible to write minus only in the columns that are to end up minus but there seems little advantage to such complication.

3-Dimensional Driving

The chosen drivers in the X and Y dimensions always first write minus and then write plus without exception. The drivers in the Z or digit dimension, which are inhibiting drivers, never drive plus (inhibit minus) since all columns are always written negative. Selected Z dimension drivers drive negative driving the write plus of the cycle to inhibit the columns that are not being written plus.

Dimension

Waveform



These waveforms can be obtained with single tubes. The driving sections need not even be push-pull.

As a first approximation a normally "ON" tube may be used with an LC circuit in the plate. An incoming negative gate long enough to allow one complete sine wave on the plate is then applied to the grid. Clipping would be needed to square up the waveform. It may prove desirable to use double-ended drivers to hold constant pulse currents.

A driver of the X, Y kind will be called an s-type driver for sequence-type.

A driver of the Z kind will be called an O-type driver for one-shot type.

A driver which must put out both plus and minus signals but not in fixed order will be called an n-type driver for non-sequenced type. Such a driver would have to be double-ended and is probably more complicated than an s-type driver.

A best-possible 3-dimensional storage of  $n^2$  registers each  $d$  digits long requires

$2n$ s-type drivers	$nd$ cores/driver
$d$ O-type drivers	$n^2$ " "

### 2-Dimensional Driving

Consider now a storage made out of best possible 2-dimensional arrays. One such array will be needed for each digit column.

The chosen X-coordinate drivers first drive negative to write minus but drive positive only in the digit columns to be written plus. It seems reasonable, however, that such a driver should be no more complicated than an s-type, the complication appearing in the control circuits. The

Y-coordinate drivers must put out opposite polarities on selected and unselected lines and are therefore of n-type. If a complete set of drivers is provided on each column we need:

nd s-type drivers	n cores/driver
nd n-type drivers	n " "
If an s-type driver requires	3 tubes
" O-type " "	2 tubes
" r-type " "	4 tubes

and we consider a storage of  $32^2 = 1024$  registers of 16 digits each then -

The 3-dimensional array requires	$64 \times 3 = 192$
	$+ 16 \times 2 = \underline{32}$
	224 tubes
The 2-dimensional array requires	3584 tubes

1  
224  
16  

---

3584

This is a substantial price to pay for the improved selection ratio. No consideration has been given to the fact that the 3-dimensional drivers drive more cores and therefore must be larger than the 2-dimensional drivers. This size difference partially compensates for the different complexity of the two systems.

Fortunately it is not necessary to go to complete separation of digit columns. For example, X-selection can be made in each column, the Y-selections in all columns at once. This arrangement requires

nd s-type drivers	n cores/driver
n n-type drivers	nd " "

For the hypothetical storage we now need 1669 tubes.

It is possible to omit the n-type drivers completely by biasing the entire 3-dimensional array with a single  $1/3$  H s-type driver, plus when writing minuses, and minuses when writing plus. Both x and y drivers can then be s-type also. The same number of x and y drivers as before are required.

2-Dimensional Redundant

This system requires 3 signals in each column, x, y, and diagonal. Two of these can be s-type with an amplitude of  $2/5 H$ , the other is n-type with an amplitude of  $1/5 H$ . A biasing driver such as mentioned above can be used with another set of s-type drivers instead of the n-types. In either event only the  $\pm 1/5$  can be common to all columns. The requirements are:

2nd	s-type	or	2nd	s-type	n	cores/driver
n	n-type		n	s-type	nd	" "
			1	s-type	$n^2 d$	" "

For the hypothetical storage we now need 3200 tubes.

3-Dimensional Redundant

Any two planes can be common to all columns, the others must be separate. There will be a 3-dimensional array in each column. Therefore we require:

$2 n^{2/3}$	s-type	$n^{4/3} d$	cores/driver
$2 n^{2/3} d$	n-type	$n^{4/3}$	" "

The array should be cubical, i.e., 512, 4096, 32768, etc. registers. It may well be that this type of system will be important for very large amounts of storage where 4-dimensions arrays become desirable but where the 5:3 switching ratio of the true 4-dimensional system may be unworkable.

Considering a storage of  $16^3 = 4096$  registers of 16 digits each, we require:

32	s-type	=	$32 \times 3$	=	96 tubes	4096 cores/driver
512	n-type	=	$512 \times 4$	=	$\frac{2048}{2144}$ tubes	256 cores/driver
					2144 tubes total	

The 2-dimensional best-possible requires 4288 tubes for this size storage or twice as many.

The 3-dimensional best-possible requires 416 tubes or about one-fifth as many.

Conclusions

It appears possible, at a substantial cost in increased complexity of the associated circuitry, to effectively improve the operating characteristics of any core material by improving the selection ratio. Some preliminary tests made by W. N. Papias show that the response time of a steel core may be approximately halved by using a 3:1 ratio instead of 2:1 and may be halved again by going to 5:1. Some of the recent steel cores are almost fast enough for use in Whirlwind at 2:1. The decision as to whether to use one of the more complicated systems must wait until more information on core characteristics and driver design become available.

Signed



R. R. Everett

RRE:bmb

cc: J.W. Forrester  
N.H. Taylor  
S.H. Dodd  
R.L. Best  
D.A. Buck  
B. Widrowitz  
H. Fahnestock  
C.L. Corderman  
J.A. O'Brien  
E.S. Rich

Olsen  
120

Electronic Computer Division  
Servomechanisms Laboratory  
Massachusetts Institute of Technology  
Cambridge, Massachusetts

SUBJECT: RECTANGULAR-LOOP MAGNETIC CORE MATERIALS

To: N. H. Taylor

From: W. N. Papian

Date: September 4, 1951

Abstract: There are ferromagnetic cores on the market today which are suitable for use in high-speed multi-dimensional storage arrays and in fast stepping registers. Tests made here indicate the high promise of Armco Mo-Permalloy-216, a metal, and Ferramic A, a ceramic. Gradual improvements in the characteristics of pertinent core materials are expected to continue.

A. INTRODUCTION

Three general classes of ferromagnetic materials are on the market today. They are:

1. Metallic materials
2. Ceramic materials
3. So-called powder or dust materials

The last mentioned class will not be discussed here because powder cores cannot now be made which combine rectangularity characteristics along with reasonable freedom from eddy-currents.

The metallic and ceramic classes both contain pertinent and promising materials for applications which require rectangular B-H loops and the freedom from eddy-currents which allows quick changes of magnetic flux to occur.<sup>1,2</sup>

---

1. W. N. Papian, "Ferromagnetic Materials for Applications Requiring Rectangular Hysteresis Loops and Short Response Times," M.I.T. E.E. Seminar Paper, Jan. 1950.

2. W. N. Papian, "A Coincident-Current Magnetic Memory Unit," Project Whirlwind Report R-192, M.I.T., August 1950.

B. METALS

For the particular purposes of the group working on magnetic-core storage at this Project only ribbon-wound ring-shaped cores have been of significant interest in the metallic class. The materials will be discussed in a more or less chronological order, that is, in the order in which they came to our attention.

1. Deltamax

This material is a grain-oriented, 50% nickel-iron alloy made by the Allegheny-Ludlum Steel Corp. and marketed in special shapes by a subsidiary, the Arnold Engineering Co. Deltamax has an extremely rectangular B-H loop (see Fig. 1), very low coercivity, high maximum-flux density, and low resistivity; it is available in ribbon thicknesses as low as 1/4 mil.

Interest in Deltamax is low here largely because of its extremely long switching times under low and medium excitations, and because of the large percentage of input energy which is lost in eddy currents under high excitations. As an example, a Deltamax core made of 1-mil ribbon takes of the order of 5 milliseconds to reverse its magnetic flux under an excitation which is about twice its coercivity. The same core can be switched in about 40 microseconds, but it requires an excitation value about 10 times its coercivity.

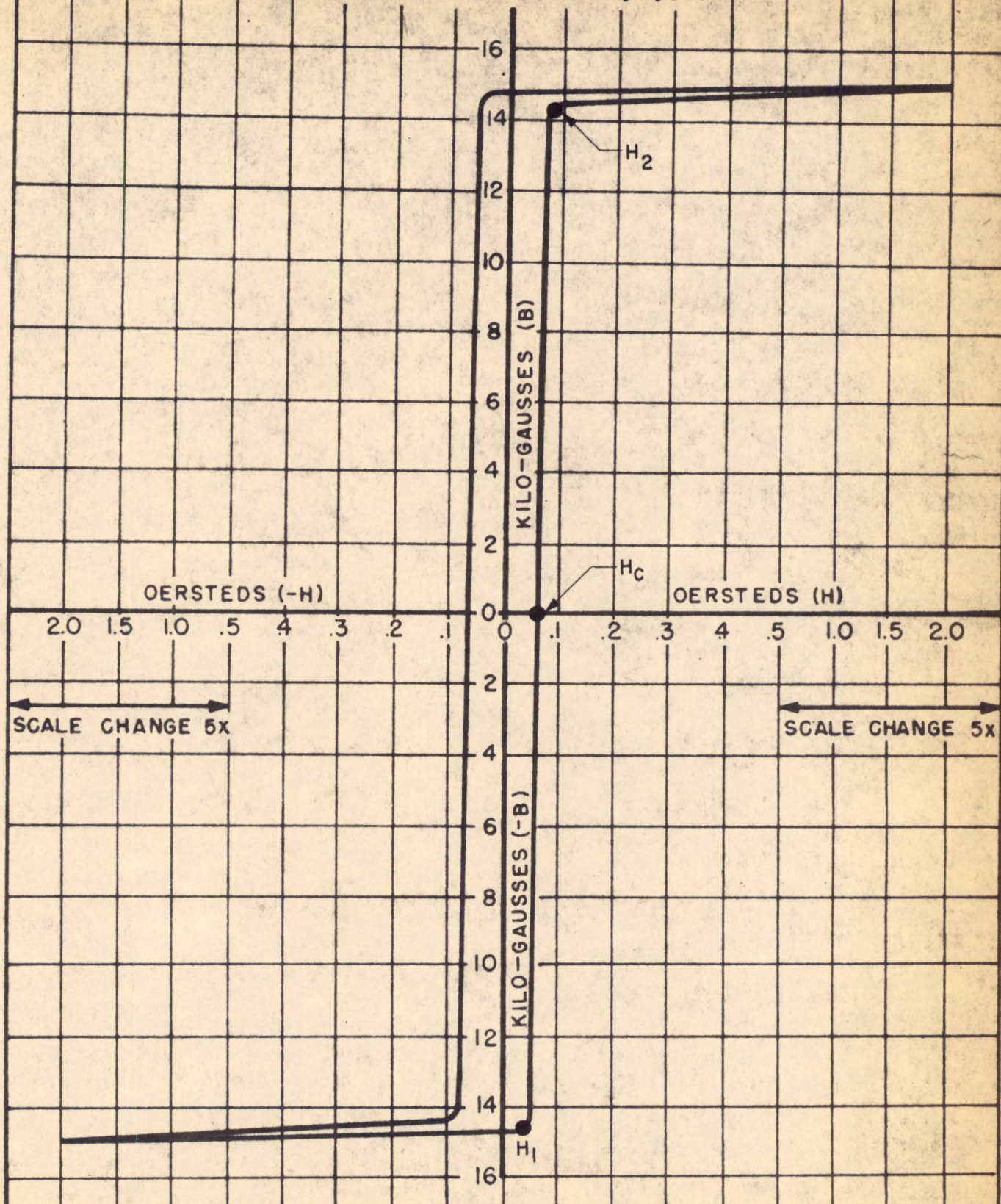
1-mil Deltamax is the material now being used in the Harvard, Alden, Wang, and Burroughs stepping-register (Static Magnetic Delay Line) cores.

2. Silectron

This is the familiar 3% silicon-iron alloy known as electrical sheet, but with a partial grain and domain orientation produced for us by Allegheny Ludlum. It has the very rectangular B-H characteristic shown in Fig. 2. Coercivity and maximum-flux density are high, resistivity is low and the material was available to us in the 1-mil thickness.

The very successful metallic core used in the early experiments and the cores used in the experimental 2 x 2 x 1 array were made of this material. Resultant speeds were good (about 20 microseconds with a 2:1 selection ratio) and signal ratios were very high. The main disadvantage of Silectron is the high coercivity which calls for high driving ampere-turns, and the rather high switching energy as indicated by its large B-H loop area. Silectron was the most promising metal until a few months ago when the material to be discussed below appeared on the scene.

# DELTAMAX



THE ARNOLD ENGINEERING CO.  
CHICAGO, ILLINOIS

FIG. 1

A-48019-G



KEUFFEL & ESSER CO., N. Y. NO. 8987-14G  
Millimeters, 5 mm. lines accented, cm. lines heavy.  
MADE IN U. S. A.

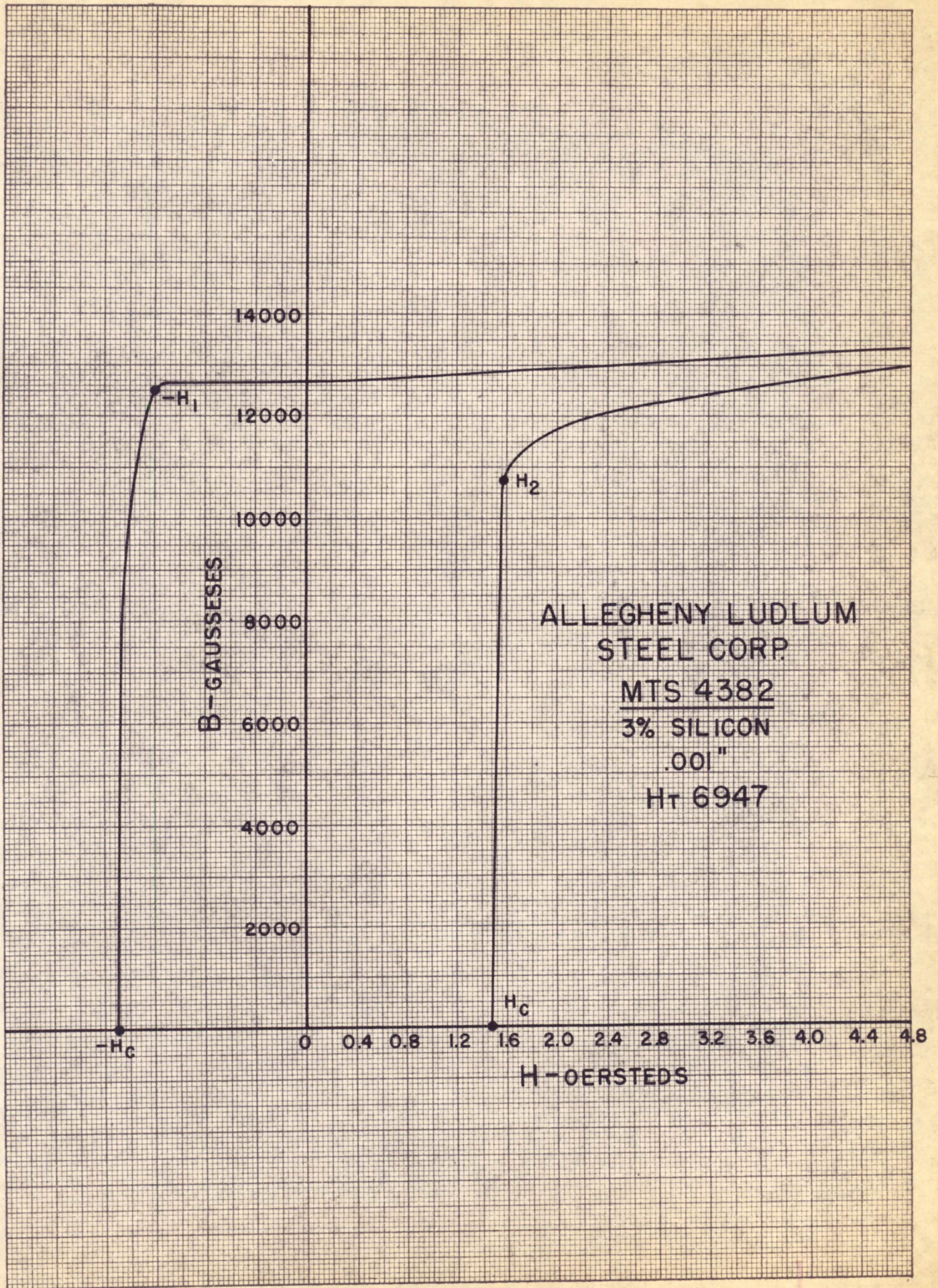


FIG. 2

A-38999 -G

### 3. Mo-Permalloy-216

Mo-Permalloy-216 is Armco Steel Corporation's special version of that 79% nickel, 4% molybdenum iron alloy. They obtain the good rectangular B-H loop shown in Fig. 3 by a special magnetic anneal. Coercivity and maximum flux density are low, resistivity average, and it is available in thicknesses down to 1/6 mil.

Interest in Mo-Permalloy-216 is high; it has virtues for application either as a coincident-current unit in a multi-dimensional array or as a memory unit in a stepping register. Mo-Permalloy-216 cores switch rapidly at all excitations due in part to the following characteristics: availability of extremely thin material, low flux densities, not-too-high maximum-differential permeabilities, and an apparent freedom from fractional-second lags in magnetization at very low excitations. The small loop area also accounts for the low switching energies required.

Small cores of this material will be used in the 16 x 16 array now in design. They are also being considered by ourselves, and by Burroughs at our urging, for use in faster, lower-energy versions of the stepping register.

The material is relatively new so that production and uniformity difficulties are being experienced by our core supplier, Magnetics, Inc., and by others. There is, however, perfectly reasonable expectation that these difficulties will be ironed out in a short time.

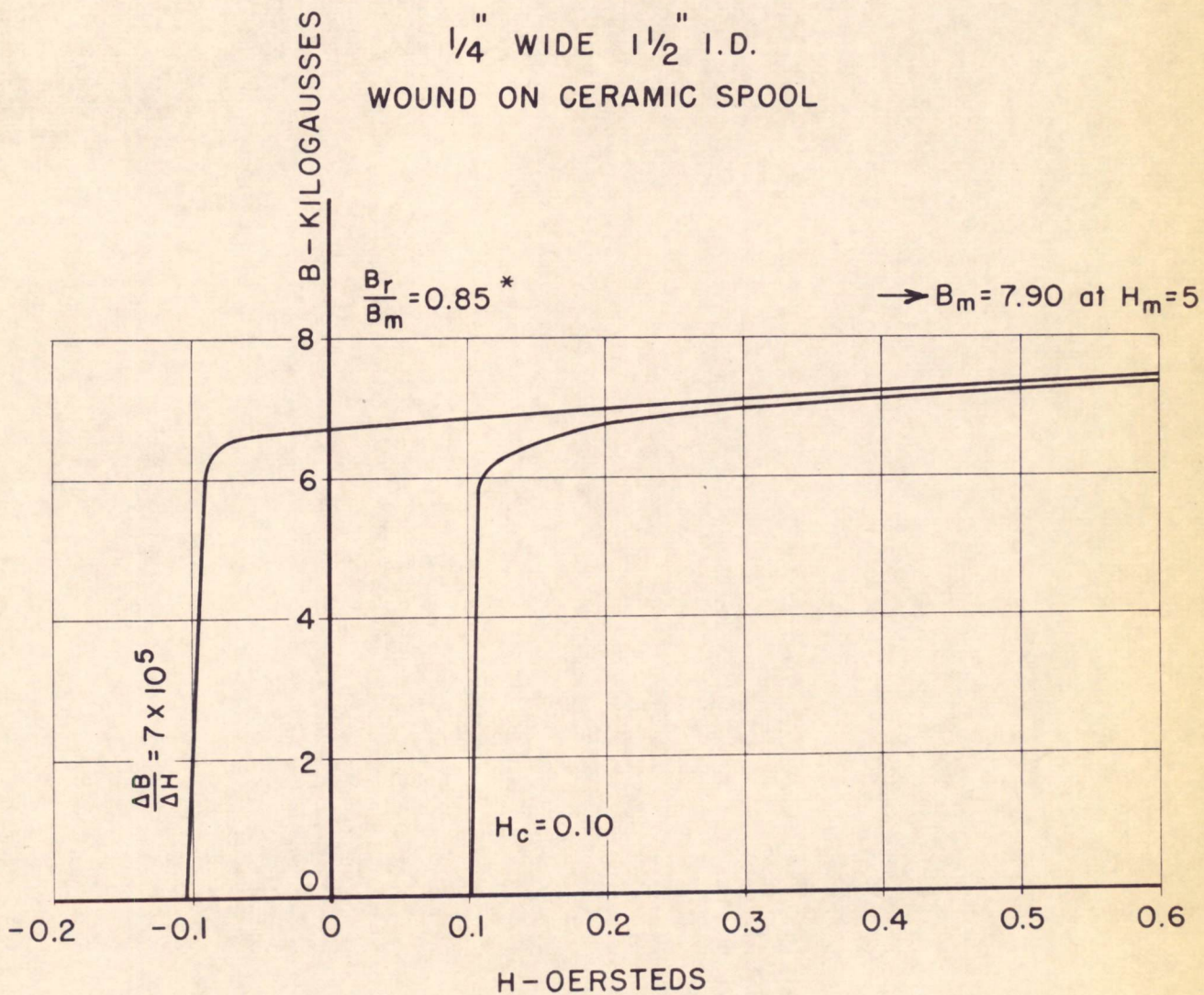
### C. CERAMICS

Where fractional-microsecond switching times are needed, the metals in their present form are unsuitable, largely due to eddy currents. The development during this last decade of a group of semi-insulator ceramics which have ferromagnetic characteristics answers the above need. These materials are called magnetic ferrites by some and ferrosinels by others. They are homogeneous compounds of various metal oxides (not metals) with resultant mechanical properties resembling those of dry-process porcelain.

In general, the ceramic materials have low B-H rectangularity, high coercivities, low flux densities, but phenomenally high resistivities. Quite a few materials have been considered, but only two are worth mentioning.

D-C HYSTERESIS LOOP  
CORE NO. 216

79-4 PERMALLOY  
0.26 MILS  
1/4" WIDE 1 1/2" I.D.  
WOUND ON CERAMIC SPOOL



\*  $\frac{B_r}{B_m} = 0.915$  for  $B_m = 7.45$

CURVE NO. 5112  
ARMCO RESEARCH LABORATORIES  
4-13-51

FIG. 3

### 1. Ferroxcube IV

This material was the first ceramic to exhibit any rectangularity. However, it did so to any marked extent only when it was under some applied mechanical strain. Because of this, and its not-too-high resistivity, interest in it waned early.

### 2. Ferramic A

Ferramic is the smart trade name which the General Ceramics and Steatite Corp. gives to its magnetic ferrites. Although there are nearly ten different Ferramics, only the A material has thus far shown sufficient rectangularity to operate as a coincident-current memory unit.

This material has a B-H loop shape as shown in Fig. 4. Coercivity is high and maximum flux density low, even relative to the other ceramics. Its resistivity is extremely high, and it appears to have no significant magnetization time lags in the microsecond region.

Interest in this material is also high. It is a potential candidate for use in high-speed multi-dimensional arrays and stepping registers. Improvements in the material's characteristics are desirable in the two directions of lower coercivity (reduced driving ampere-turns) and better B-H rectangularity. It is also desirable, but difficult, to get cores made in very small shapes and sizes. Development work in these and other directions is going on and is being encouraged by the laboratory. Some slightly improved versions of this core material have been received and tested, and other improved samples are expected in the future.

Ferramic A cores have been operated here as coincident-current units with 2:1 and 3:1 selection ratios at switching speeds of about 1/2 microsecond. They have also been operated by Buck and Guditz in a 4-core stepping register at speeds over 100,000 digit-transfers per second, using outside cores and other parameters not truly optimized for the job.

### D. CONCLUSION

Presently available rectangular-loop ferromagnetic cores for high-speed storage and pulse applications contain a few which show a great deal of promise. Armco's Mo-Permalloy-216 is, at the moment, the most interesting among the metals; the most promising ceramic is a slightly improved Ferramic A core. Both materials are useful as they stand, and continued improvements are expected.

Signed by

W. N. Papien  
W. N. Papien

Approved by

N. H. Taylor  
N. H. Taylor

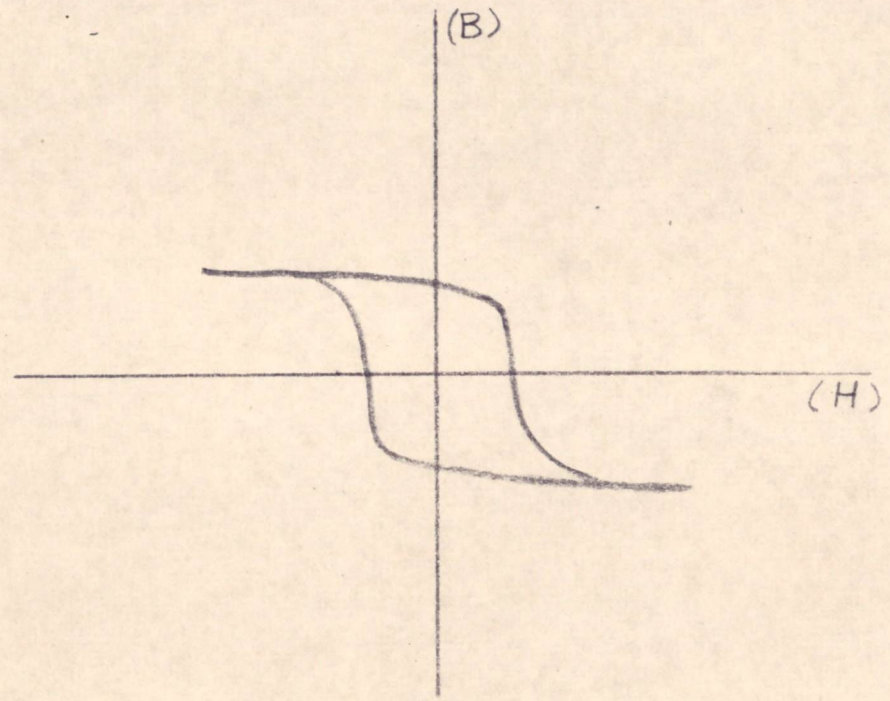
WNP:kst

#### Drawings Attached:

- Fig. 1 - Drawing No. A-48019-G, Page 3
- Fig. 2 - Drawing No. A-38999-G, Page 4
- Fig. 3 - Drawing No. A-50265, Page 6
- Fig. 4 - Drawing No. SA-50264, Page 8

SA-50264

SKETCHED FROM OSCILLOGRAPHIC PRESENTATION AT 60 ~



SERVOMECHANISMS LABORATORY OF THE <b>MASSACHUSETTS INSTITUTE OF TECHNOLOGY</b> DIVISION OF INDUSTRIAL COOPERATION PROJECT NO.			
B-H LOOP SHAPE - IMPROVED FERRAMIC A			CORE #1
SCALE:		DR. B.W.	
ENG. B.W.	CK.	APP.	SA-50264

FIG. 4

Digital Computer Laboratory  
Massachusetts Institute of Technology  
Cambridge 39, Massachusetts

SUBJECT: THE CADAC COMPUTER

To: J. W. Forrester

From: E. A. Emerson, A. M. Werlin

Date: February 15, 1952

Abstract: The CADAC is a slow speed general purpose digital computer designed and built by the Computer Research Corporation of Hawthorne, California. It is an automatic-sequence-controlled, serial machine having a magnetic drum memory. It operates with a word length of 42 binary digits and requires an average of about 70 milliseconds to carry out one command. Fourteen different commands are provided. To avoid conversion problems, all numbers are handled in octal form throughout the machine. Program instructions must be prepared in this form for insertion on a special keyboard and results also are obtained in this form through an output typewriter. Plans were made for future addition of a magnetic tape input and output device.

A goal set for the design of this machine was to minimize the number of vacuum tube circuits used. A large reduction in the number of tubes required was achieved by the use of recirculating registers on the magnetic drum and the use of crystal diode circuits for the logical networks. From an operational standpoint, it appears that the advantages of a fewer number of vacuum tube circuits are offset to some extent by the potential weaknesses in the extensive crystal diode networks. The CADAC has only 195 vacuum tubes but about 2500 crystal diodes.

A unique approach to the system design problem was applied in the development of the CADAC. All operations to be accomplished were first described in logical equations using the notations of Boolean algebra. The set of equations obtained defined the input conditions for each flip-flop and each drum-memory channel for all steps of a command. They, therefore, also defined the configurations of "and" and "or" circuits needed to control the states of the memory elements, so it was a straightforward matter to synthesize the crystal diode networks. The technique of using equations to describe

the system operation not only proved successful in the machine design but it also has been found useful in maintenance and trouble-shooting work.

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  - 2.2 Applications
    - 2.21 Number Representation
    - 2.22 CADAC Order Code
    - 2.23 Operating Instructions
  - 2.3 Internal Characteristics
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  - 4.1 Methods of Trouble-Shooting
  - 4.2 Difficulties in Trouble-Shooting

## 1.0 INTRODUCTION

The CADAC is a general purpose slow speed automatic sequence controlled computer designed and built by the Computer Research Corporation of Hawthorne, California, for the Air Force Cambridge Research Laboratories. At the inception of this machine the general attitude of computer engineers was that electronic computers could not be designed with fewer than thousands of electronic tubes without sacrificing useful word length. The Computer Research Corporation departed from this philosophy and has succeeded in building a relatively inexpensive (Fortune magazine quote: "\$80,000"), very compact machine. The designs and design techniques that overcame the engineering obstacles met in this computer deserve considerable respect, and the CADAC, as a practical product of these motives and techniques, is of interest to personnel associated with other computer projects.

## 2.0 LOGICAL CHARACTERISTICS AND DESIGN

### 2.1 External Characteristics

CADAC, properly programmed, will perform arithmetic and logical manipulations on digital quantities within the range  $-(1-8^{-12}) < x < (1-8^{-12})$ . It operates with serial techniques on words fourteen octal digits (forty-two binary digits) long with a fixed binary point. There are fourteen three-address commands with a mean operating time of seventy milliseconds per command (about 15 commands per second).

The magnetic drum memory has a capacity for 1023\* words with a mean access time of 14 milliseconds. There are 16 channels, each of which contains 64 words around the circumference of the drum.

The input device now associated with the computer is an eight key keyboard on the control panel. These keys are used for entering octal numbers. The output typewriter prints one to four columns of octal figures across a page. Either the contents or the address and contents of any memory register may be printed out. These accessories do not lend themselves readily to decimal computation and the input is both tedious and slow. However, the machine has been wired with internal circuits which will enable it to read in from and read out to an external magnetic tape unit although none was provided with this model.

---

\* Because of the nature of the multiplication and division process register #0 is not used for a memory location.



## 2.2 Applications

This machine by virtue of its long word length is capable of obtaining results to a precision of about 11 decimal digits. The three-address-code system, while seemingly redundant to Whirlwind programmers, is necessary to a machine with no arithmetic registers. It also equips the machine to perform certain operations with a saving in the number of registers required for commands. This long word length and economical use of register space, combined with a main storage consisting of 1023 consecutive registers yields a computer potentially adapted to most types of general computation, and with proper external equipment to some types of slow speed control operations.

### 2.21 Number Representation

Positive and negative numbers,  $N$ , are represented with a 2 octal digit sign followed by  $N \times 8^{-12}$ . The sign convention is:

- 00 negative number
- 01 positive number
- 02 negative number indicating arithmetic overflow
- 03 positive number indicating arithmetic overflow

The machine interprets all commands as positive numbers when they are modified by arithmetic processes.

### 2.22 CADAC Order Code

The command is divided into four sections, an instruction consisting of 2 octal digits, and three addresses ( $m_1$ ,  $m_2$  &  $m_3$ ) of four octal digits each.

These instructions perform the following functions:

<u>Octal Code</u>	<u>Instruction and Abbreviation</u>
37	Halt: (H) Stop the computer
35	Fill: (F) Read from an external unit during program operation. As yet this order is not defined in either logical design or circuitry.
33	Write addresses and associated words on external tape unit: ( $P_1$ ) Start with register $m_1$ and continue for the next $n$ registers where $n$ is $m_3$ . The logical designs and circuitry are complete, but the external unit has not been provided with this model.

- 31 Type addresses and associated words: ( $P_2$ )  
The address convention is the same as in the tape order.
- 27 Write word only on external tape unit: ( $P_3$ )  
The address convention is the same as above.
- 25 Type word only: ( $P_4$ )  
The address convention is the same as above.
- 23 Test overflow: ( $T_0$ )  
Investigate the contents of register  $m_1$ .  
If the sign indicates an arithmetic overflow, set the control number to  $m_3$ .
- 21 Test difference: (T)  
If the contents of register  $m_1$  is greater than the contents of register  $m_2$  set the control number to  $m_3$ .
- 17 Extract: (E)  
From the contents of register  $m_1$ , extract those digits which are in coincidence with the binary "ones" of the contents of register  $m_2$  and insert those digits into register  $m_3$ , leaving the rest of the contents of register  $m_3$  unchanged.
- 15 Subtract: (S)  
Subtract the contents of register  $m_2$  from the contents of register  $m_1$  and put the difference in register  $m_3$ . If the absolute difference exceeds one, indicate an arithmetic overflow.
- 13 Add: (A)  
Add the contents of register  $m_1$  to the contents of register  $m_2$  and put the sum in register  $m_3$ . If the absolute sum exceeds one, indicate an arithmetic overflow.
- 11 Shift: (Sh)  
Shift the contents of register  $m_1$ , left if the contents of register  $m_2$  is positive or right if the contents of register  $m_2$  is negative, the number of binary digits indicated in the magnitude of the contents of register  $m_2$  (this model will shift as often as the contents of  $m_2$  indicate, extraneous shifts included) and put the shifted result in register  $m_3$ . If any

significant digits are shifted off the left end indicate an arithmetic overflow.

- 7            Multiply: (M)  
Multiply the contents of register  $m_1$  by the contents of register  $m_2$  and put the product rounded off to 12 significant octal digits with its proper sign into register  $m_3$ . No provision has been made for double register multiplication.
- 5            Divide: (D)  
Divide the contents of register  $m_1$  by the contents of register  $m_2$  and put the quotient rounded off to 12 octal digits with its proper sign in register  $m_3$ . If the absolute quotient exceeds one, indicate an arithmetic overflow.

### 2.23 Operating Instructions

There are sixteen switches, buttons and keys on the control panel.

- (1) AC power switch
- (1) Drum motor power switch
- (1) B~~/~~ power on button
- (1) B~~/~~ power off button
- (1) Start computation key
- (1) Clear key
- (8) Octal digit keys
- (1) Tab key which fills octal number in storage
- (1) Space key which selects storage position for filling and starting computation

The machine is cycled on in the order: AC Power; Drum motor power; when the drum reaches speed, the stop button is held down and the "B~~/~~ on" button is pressed. The typewriter motor is turned on by its own switch at any time.

To fill a program the first storage address is set up by entering the address on the octal keyboard and pushing the "space" button. The contents of the first register is then entered on the octal keyboard and the "tab" button pushed. The machine automatically steps one storage register for each push of the "tab" button so that it is necessary to set up the address of only the first storage register. Any error on the octal keyboard before the "tab" button is pushed can

be remedied by reentering the correct number right on top of the old number, then tabbing. Any error after tabbing can be remedied by setting up the address of the incorrect storage register and replacing the contents with the correct value, then continuing.

To start a computation enter the control number (address of order to be operated on) followed by four zeros and push the space button, then push the "start" button. The "clear" button will halt any operation at any time.

A specimen program is included in the appendix.

## 2.3 Internal Characteristics

### 2.31 Building Blocks and Stable States

The two binary states are represented in the machine as two separate dc voltage levels, each of which is maintained by diode clamping throughout the machine. The higher voltage level,  $E_H$ , is used to represent a "1" and the lower level,  $E_L$ , is used to represent a "0". Four component combinations are used for the logical building blocks utilized by the machine to maintain the logical voltage levels:

- (1) The bistable flip-flop which can be set to "0" or "1" but cannot be complemented. It has cathode follower drivers whose outputs are clamped to either of the two voltage levels (see Figure 1).
- (2) The logical product circuit ("and" gate), i.e., both inputs must be at the high voltage level for the output to be at the high voltage level. (Figure 2)
- (3) The logical sum circuit ("or" gate), i.e., if either input is at the high voltage level then the output will be at the high voltage level. (Figure 3)
- (4) The logical negative circuit, i.e., the output voltage is at the high level if the input voltage is at the low level and vice versa. (Figure 4)

Every logical voltage level starts as the output of one side of a flip-flop. These voltage levels are returned through combinations of the sum, product and negative circuits to the inputs of the various flip-flops in the machine. These inputs are termed "propositions", being in effect true or false (one or zero, plus or minus etc.) logical propositions. As the various flip-flops in the machine assume different

combinations of their bistable states, different configurations of voltage levels appear at the various inputs. The table of Figure 5 shows the results obtained from the basic logical operations.

### 2.32 Clock Pulses and Flip-Flop Triggers

A combination of components of the type indicated in the last paragraph becomes practical when a new stable configuration of voltage levels can be derived from the preceding configuration as a function of it. If a square clock waveform fluctuating between the two logical voltage levels with some standard frequency is introduced, time boundaries between the desired configurations can be developed and defined. The flip-flops can then be triggered by logically multiplying the proposition voltage levels on the inputs of the "one" and "zero" sides of a flip-flop by the clock waveform and passing this through the proper differentiating circuit. If the input proposition is false, i.e., at the lower voltage level, the clock rise and fall will have no effect on the grid of the particular side of the flip-flop in question, but if the input proposition is true, i.e., at the higher voltage level, as the clock pulse falls, the flip-flop will be triggered. Thus the clock provides both a timing system and a dynamic trigger on the grid of a flip-flop tube controlled by the propositions from the network of sum and product circuits.

### 2.33 Elements Governing Design

The major factors governing the design of the computer were the decisions to use serial operation and magnetic drum storage. The main memory is the magnetic drum 12 inches in diameter rotating on a vertical axis at about 40 rps. It has 22 useful channels: 16 storage channels capable of holding 64 words each, 3 channels associated with three recirculating arithmetic registers, and three channels permanently recorded: the clock pulse channel, a word reference channel, and a start synchronizing pulse channel. Access to the memory is through read-record heads mounted within 0.001 inches of the drum. A channel is selected by means of a flip-flop controlled matrix and the time position identified by comparing the contents of a group of flip-flops against the word reference channel. The permanent channels can only be read from, not read into.

The three recirculating registers each consist of record head and a read head on the same channel located so that a point on the spinning drum passes the record head first. They are spaced and interconnected so that a particular signal, when recorded, will be carried by the drum to the read head,

passed through the circuitry, and rerecorded 42 clock pulses later (Figure 6). The circuitry controlling the record head inputs is the logical diode net which is in turn controlled by the outputs of the read heads of the recirculating registers and of the main storage, and also by the outputs of the control panel. When an arithmetic operation is complete the answer is contained in a recirculating register whence it is immediately transferred to storage and the register cleared. There are no arithmetic registers in the Whirlwind sense; all results must be placed in some storage register immediately. The recirculating registers are used in all arithmetic, searching, and control operations, blending strings of data 42 pulses long as a spinning machine twists many strands into a thread.

## 2.34 Control

### 2.341 Nature of Operation Sequences

The execution of a particular coded command consists of several separate operations performed in order: the command must be looked up and identified, memory registers referred to, arithmetic processes completed, and results returned to storage. These operations, logically arranged in a minimum order, take the form of a flow diagram when described pictorially. (Figure 7)

When a program has been filled into storage a control number set, and the start button pushed, the machine proceeds serially through the separate operations as indicated in the flow diagram, first looking up the command, then testing it serially to determine which order to execute, then following through the execution until finished, and finally searching for the next command.

Most of the operations take many separate steps of one word-time (the time it takes 42 clock pulses to pass through a recirculating register, or one sixty-fourth of one revolution of the drum), and for the actual design of the computer a more elaborate flow diagram was drawn indicating each separate operation as a group of steps one word time long. Each separate step is shown as a small box which describes the function it performs and also contains a reference to the configuration of switching necessary in that word time. These steps are numbered consecutively and grouped by operation. At the end of one operation, the operation

starting with the next consecutive step is performed unless the control is transferred to an operation starting with a step having a known, but not consecutive number. This resembles the flow diagram of a normal coded program for a computing machine with commands, conditional subprograms, and subprograms.

### 2.342 Control of Sequences

As any computer requires a counter to keep track of the address of the next instruction, the CADAC requires a counter to keep track of the process by which it carries out a command. The designers of CADAC called this internal counter a "program counter" and constructed it from eight presettable flip-flops. Most of the  $2^8$  possible configurations (some are not used) of these flip-flops refer to a step in the master flow diagram, and each configuration can be used to produce a "true" voltage level at any point in the machine. Thus any portion of the diode net can be gated in for one certain step, or for steps which perform identically. However, each step lasts one word time which allows 14 octal digits of three pulses each to pass by. It is necessary to split the words into octal digits in order to isolate the orders from addresses and the signs from magnitudes. Therefore, a four flip-flop counter (the "O" counter) is employed which counts octal digits from 0 to 13, then resets itself again to zero. From this it is possible to gate in any portion of the logical net for any particular octal digit or any group of octal digits of a word time. It is also often necessary to select a particular binary digit in an octal digit. A two flip-flop pulse counter (the "P" counter) is employed which counts pulses from 0 to 2, then resets itself again to zero. From this it is possible to gate in any portion of the logical net to a particular pulse of an octal digit.

### 2.343 Control in a Specific Operation

For an example of the computer control mechanism, let us see how the machine knows when to use the process which determines the sign of a product. The product sign is a function of the sign digits of the two factors. The logical circuit for this process is synthesizing the function for every pair of pulses that pass through two of the recirculating registers. However, this function is gated further into the net only on the first pulse ( $P_0$ ) of each octal digit. The function is then gated

to the next level of the net only on the 13th octal digit ( $O_{12}$ ) of each word time. And finally it is gated onto the record head of the recirculating register which contains the product only during the 52nd (PC #52) step of the master flow diagram, the roundoff step of the multiplication operation.

### 2.35 Outlining the Circuits

CADAC was designed to be physically small, so a saving in equipment at the expense of requiring the components to serve more than one purpose was feasible. Certain overlapping of components' uses is obvious, since the machine is never printing, selecting a channel, shifting, adding, etc. simultaneously. This necessarily led to very complicated interconnections of the diode network and the flip-flops.

For convenience in determining what interconnections were required, the notation and laws of Boolean algebra were applied to define the inputs of each flip-flop and of each record head in terms of the outputs of the logical flip-flops, the outputs of the three sets of counter flip-flops (P counter, O counter and Program Counter), and the clock pulses. No block diagrams were used at any stage. Equations were written for the inputs of each side of every logical flip-flop and record head for each step in the entire master block diagram. Certain equations reappeared frequently throughout the machine, so each equation was number coded for reference and written on an "operations numbers chart". The separate equations for the inputs of each flip-flop and record head were then combined and reduced to final equations of the apparently most electronically feasible form. Care was taken that no flip-flop was ever pulsed on both grids simultaneously.

From the above mentioned equations an outline of the diode network circuit could be drawn immediately without hesitation. A more complete discussion of this method is "Techniques in the Design of Digital Computers" by Richard E. Sprague of the Computer Research Corporation. A copy is available in the Digital Computer Lab library. Such an outline indicates the relative location of all logical crystals, diodes, resistors, and flip-flop units. Then for the actual circuit design, it is necessary to calculate the proper resistance values and to insert power amplification where needed. This is discussed in section 3.4 of this report.

The equations, combined with the flow diagram, give a complete picture of how the computer operates and, because of their convenient cataloging, they facilitate the location of errors. It is difficult for a person weaned on block diagrams



and their proximity to circuit schematics to appreciate this at first, but only a small amount of familiarization with the technique enables a beginner to apply the method to the building blocks of the CADAC.

### 3.0 MECHANICAL AND ELECTRONIC CHARACTERISTICS OF CADAC

#### 3.1 Physical Description

The CADAC computer occupies a space of approximately 35 cubic feet and weighs about 500 pounds; it is divided into two sections. The lower section consists of the main power supply, the fan motor, the drum motor, and a smaller selenium-rectifier power supply to deliver the 100 v. D.C. required by the drum motor. A variac on the input to this power supply serves as the motor speed control. The upper section of the computer consists of the 12" diameter magnetic drum, with its associated heads, read-record amplifiers, read-out flip-flop, circulating register flip-flops and clock pulse generator. These circuits are mounted in sub-assemblies located around the drum. Also in this section are the input-typewriter relays. On four large phenolic boards surrounding the upper section of the machine are mounted all the crystal diodes used in the logical diode networks as well as those used for clamping. There are approximately 2500 crystal diodes mounted on these boards. All of the flip-flops and driver tubes not associated with the memory are mounted horizontally around the top of these boards. Most of these tubes are in the circuits of the three counters and their associated drivers. The "logical" voltages for the computing system and those which exist throughout the diode nets are  $\sqrt{125}$  v. ( $E_H$ ) for "true" (one) and  $\sqrt{100}$  v. ( $E_L$ ) for "false" (zero). It must be remembered that the computer operates on a non-return-to-zero basis, and that voltage remains constant at  $\sqrt{125}$  v. as long as there is a serial group of one's and  $\sqrt{100}$  when there is a serial group of zero's. These voltages are D.C. coupled throughout the diode nets. If the output of the net is true or at  $\sqrt{125}$ , it will gate the negative going edge of a clock pulse, permitting it to trigger one side of a flip-flop.

#### 3.2 Power Supply

The computer requires a power input of 3KVA, 110 v. A.C., 60 cycles. This is non-regulated and comes directly from the power line. All of the inputs to the power transformers are fused with the conventional cartridge type fuses. The power transformers have tapped primaries, and by choice of the proper tap, the system can be operated with any line voltage that falls in the range from 105 volts to 125 volts. The main power supply is of the bridged-

selenium-rectifier type; it delivers  $\pm 300$  v. d.c. unregulated. From this voltage, the following regulated d.c. voltages are derived:  $-300$  v. (400 ma.),  $\pm 225$  v. (2.6 a),  $\pm 125$  (450 ma.),  $\pm 100$  (1 a). Operation of the two power switches turns on the filaments of all tubes and energizes the drum and fan motors. Throwing the "d.c. on" switch energizes the master time delay relay which applies the voltages to the computer in the sequence listed above. Incorporated in this power supply is an 884 control circuit which does not permit the time delay relay to energize unless all the voltages are present and are within 5 v. of their proper values with reference to the  $-300$  v. The supplies have conventional series regulators using 6AS7's for the current control tube and a 6AU6 and a VR-105 for voltage control. There is a small additional power supply which supplies  $-240$  v. to a balanced inverter-cathode-follower stage which feeds the drivers for the read-out flip-flops.

The supply for the drum motor is nominally  $\pm 100$  v. D.C. which draws a starting current of 3.8 a and a running current of 1.8 a. The A.C. input to the supply is variac controlled to control the speed of drum rotation. The speed is nominally 40 rps but is not especially critical since the 100 kc clock pulses are derived from the permanently recorded clock channel on the drum. The lower limit of drum speed is reached when the amplitude of the read signal is too low to trigger the read-out flip-flop. The upper limit of speed is reached when the frequency of the read-out pulses is so high that flip-flops will not reach their stable states before they are triggered again.

### 3.3 Vacuum Tubes

There are 195 vacuum tubes in the CADAC, about 30 of which are in the power supply, 65 in the memory circuits and 100 in the arithmetic center. There are 31 flip-flops in this machine for which 12AT7's are used exclusively. Below is a chart of the tube count in the arithmetic unit:

8 decision flip-flops	12AT7
6 decision flip-flop drivers	5687
6 pulse and digit counter flip-flops	12AT7
6 pulse and digit counter flip-flop drivers	5687
5 extra pulse and digit counter flip-flop drivers	5687
8 program counter flip-flops	12AT7
18 program counter flip-flop drivers	50L6
5 typewriter relay drivers	5687
1 memory flip-flop	12AT7
1 memory flip-flop driver	5687
1 carry flip-flop	12AT7
1 carry flip-flop driver	5687
10 cathode follower drivers	12AT7

12 recirculating register flip-flops	12AT7
7 recirculating register flip-flop drivers	5687 and 12AT7
4 phase inverters	12AT7
4 clippers	12AT7
1 start F.F.	12AT7
3 drivers (clock etc.)	5687

The 12AT7 was chosen for use as a flip-flop because it has a high  $G_m$ , hence a small grid swing from zero bias to cut-off (0 to -4.5 v.) which makes it quite easy to trigger, and also because it is a miniature. The 5687 was chosen for drivers because it will supply more current with  $\approx 100$  v. on the plate at zero bias (42 ma.) than any other miniature type. For the program counter output, which must deliver more current to the diode nets than the 5687 can provide, the 50L6 was used. This tube will deliver 106 ma. at 100 v. and zero bias. The tubes for the flip-flops and drivers listed above are not especially selected or matched. There is no provision for marginal voltage tests nor are there any particular acceptance tests for tubes. A conventional tube tester is used for determining when tubes should be replaced. The heater voltages for all tubes are applied directly with no warm-up time. With the exception of the 50L6 and 50C5 tubes, nominal values of heater voltage are used. The 50 volt heaters are wired in series-parallel across the line and are operated at about 45 v. Little trouble has been experienced from filament burn-out from these high-voltage-filament type tubes. There has been no data on the reliability of these tubes since the computer has not been operating long enough to gather such data.

The list of tubes associated with the memory is tabulated below:

32 record tubes - main memory	50C5
6 record tubes - E,F,G, one word circulating registers	50C5
19 pre-amps - main memory	6AS6
4 pre-amps - E,F,G, recirculating registers and main memory	12AT7
2 amplifiers for clock	12AT7

Since push-pull recording is employed on every drum channel, the choice of the 50C5's is the most critical. They are carefully selected as a matched pair for both plate current at zero bias and for cut-off voltage. All circuits have been designed so that they will still operate with about 25% decrease in tube emission. Most of the flip-flops feed 5687 drivers whose plates are returned to  $\approx 225$  through their plate load resistance. Since the driver plates are clamped at  $\approx 100$  and  $\approx 125$  volts by means of crystal diodes, the variation in plate current can be quite wide before the plate circuit will fail to switch from one clamped voltage to

the other. Flip-flops are well within their plate dissipation. The 12AT7 flip-flop "on" side with a 12K plate load to  $\sqrt{225}$  v. will normally dissipate about 1 watt and the tube is rated for 2.5 watts per section. The 5687's, however, when conducting, have their plates clamped at  $\sqrt{100}$  v. Under this condition, their dissipation is close to the rated value of 4 watts.

### 3.4 Crystals and Crystal Nets

#### 3.41 Use of Crystals

Type 1N52 crystal diodes are used almost exclusively throughout the computer both for the logical net and for clamping of driver plate circuits. They are all carefully selected for minimum back current and low forward drop. All diodes are checked and must have less than 3 v. forward drop at 25 ma. For all logical diodes the back current must be less than  $100 \mu\text{a}$  at 25 v. while the clamping diodes are unacceptable unless they pass less than  $200 \mu\text{a}$  back current at 25 v. There is no consideration for crystal noise. The action of the diodes and how they are used can best be shown by an example. In the product circuit (Figure 2) the voltages  $P_1$  and  $P_2$  must both be high or at 125 v. for the output to be high. If either  $P_1$  or  $P_2$  is at  $\sqrt{100}$  v. one of the net diodes will conduct more heavily, lowering the output to  $\sqrt{100}$  v. In the sum circuit (Figure 3) either  $P_1$ , or  $P_2$ , or both can be high and the output will rise to  $\sqrt{125}$  v.

The logical network of Figure 8, which is a combination of the sum and product nets shown in Figures 2 and 3, expresses the logical proposition  $(P_1 P_2 / P_3) C$  as its output. If the proposition  $(P_1 P_2 / P_3)$  is true, i.e., if point  $\underline{Y}$  is at  $\sqrt{125}$  v., point  $\underline{Z}$  will follow the clock input, C, as indicated by the waveforms. The voltage at point  $\underline{Z}$  is differentiated so that a negative pulse coincident with the trailing edge of the clock pulse is obtained to trigger a flip-flop. In considering the forward drop of the diodes in the above circuit, it can be seen that there is just as much gain in d.c. level as there is loss. For example, assuming a 2 v. forward drop, point  $\underline{X}$  will be at 127 v. Point  $\underline{Y}$  will drop again to 125 v. and so forth. From a static point of view at least, it appears that an indefinite string of sum and product terms are possible. For a string of just products, or just sums, however, there will be a definite signal deterioration, depending upon the forward resistance of the diodes and the current permitted to flow through them. In the CADAC, the average forward current is from 5-10 ma. and not more than 7 or 8 terms are used in any one net.

### 3.42 Computation of Resistor Values

The selection of  $R_1$  (Figure 8) is based on the input capacitance of the following stage and the required time necessary to allow the d.c. level to rise to its final value. When the clock voltage rises from 100 v., it immediately cuts its diode off and the voltage at the junction will rise exponentially toward 225 v.; the time at which it reaches 125 v. is determined by the value of  $R_1$  and the shunt capacitance. For driving one flip-flop, with an assumed input capacitance of 10  $\mu\text{f}$ , it is found that for  $R_1 = 1$  meg, the output voltage reaches its final level in about 3  $\mu\text{s}$ . The worst load condition (when the value of  $i_1$  is greatest) is when the voltages at all the junctions are low. Then  $i_1 = \frac{225-100}{R_1} / i_{b1}$ . In this respect the back current of the

clock diode is critical, so that this diode is chosen for the minimum back current at 25 v. It is assumed to be 100  $\mu\text{a}$  as a safety factor.  $R_2$  is now selected on the basis that the drop across it should not exceed 100 v. with  $i_1$  flowing through it. Therefore,  $R_2 = \frac{100}{i_1}$ . The greatest  $i_2$  will flow into the

sum network when the point  $X$  is high so that  $i_2 = \frac{125}{R_2} / i_{b2}$ .

Now since  $R_2$  is less than  $R_1$  the back resistance of the diode through which  $i_{b2}$  flows need not be as high as that of the clock diode. Here again the crystal back current is also assumed to be 100  $\mu\text{a}$ . As before,  $R_2$  cannot have a drop of more than 100 v. so  $R_1 = \frac{100}{I_2}$ . The equations for  $R_1$  and  $R_2$

are similar because the values of 125 v. and 100 v. were chosen to be symmetrical between 225 v. and ground. In the same manner currents in the clamping diodes are calculated.

### 3.5 Other Components

All of the low wattage carbon resistors in the CADAC are 5% Allan-Bradley units. However, in the places where d.c. coupling occurs, such as from a flip-flop to its associated driver, and in cathode follower inputs, 1% Nobelay precision resistors are used. Standard commercial components are used throughout the computer, including electrolytic capacitors for power supply filters and decoupling networks. The coupling capacitors to flip-flops and those in the memory circuits are mica postage-stamp type. Paper capacitors are also used in several places for decoupling. The relays in the power supply are specialized timing relays, and the typewriter relays are standard 150 v. d.c. Spark suppression across the typewriter relays is necessary, and these relays must

be carefully adjusted to eliminate bouncing of the contacts. No twin contacts on relays or any redundant circuits are used to increase reliability.

### 3.6 Circuits

#### 3.61 Flip-Flop Circuits

There are 31 flip-flops used in this computer. The circuit diagram of one with its associated driver is shown in Figure 9.

The only load on a flip-flop is a high current driver, which feeds into the diode net. The output of the driver is clamped between  $\pm 125$  and  $\pm 100$  volts. After differentiation and clipping, the input to the grids is a 13-14 volt negative pulse. The  $\pm 3$  v. return of the differentiating circuit is employed to clip out any hash or noise which might be generated in the nets. This reduces the effective negative driving voltage by a few volts, but there is still plenty of amplitude available. The grids are clamped at -8 v. to inhibit negative overshoot in the grid circuit and bring about rapid recovery to its stable state. The plate swing is from  $\pm 90$  to  $\pm 160$  volts, causing the on tube to draw grid current, which tends to stabilize the circuit. With the d.c. coupling employed, the grid swing on the driver is from -40 v. to  $\pm 0.5$  v. There is not much consideration for switch-over time since there will be a minimum of  $10 \mu$  s before it is necessary for flip-flops (in combination with other propositions) to gate the trailing edge of the clock pulse. No steps have been taken to insure matched sections in the flip-flop tubes, nor have there been any data taken on tube deterioration and how much unbalance is allowable before failure of the flip-flop occurs.

#### 3.62 Read-Record Circuits

The main memory employs center tapped heads and push-pull recording, with the one's being recorded by one miniature pentode (50C5) and the zero's by the other. Since the record currents are too large to switch, two record tubes are required for each of the 16 main storage channels. The read signals are taken off the same heads by capacitance coupling to one side of the recording winding. The signals obtained (about 0.4 volt amplitude) are amplified, and gated in 16 6AS6's, all of which have a common plate connection. The read signal is then applied to the "M" (memory) flip-flop which reconstructs the d.c. signal level as recorded on the drum. The read-record circuit is shown in Figure 10. The 50C5's are critical and are a matched pair, so that the "one" and "zero" record currents are equal. The current is sufficient to

saturate the drum in either direction. If one of the 50C5's becomes weak there is danger of not erasing the old information on the drum.

Since the fall of the clock pulse initiates both the one and zero record pulses, a delay equivalent to half the length of a clock pulse is necessary in the read-out circuit. Without a delay, the trailing edge of the clock pulse might occur while the "M" flip-flop is switching.

The reading amplifier can tolerate a 10% reduction in gain before the drive to the "M" flip-flop is affected. The bandwidth of the reading amplifier is in the order of 300KC. Most of the plate supply decoupling, shielding, etc. is done in the memory read-out circuit. There is no problem here of p.r.f. sensitivity since d.c. coupling is used in the channel whenever there are unidirectional pulses.

### 3.63 Cathode-Follower Circuits

In many places throughout the diode net cathode-followers were inserted so as not to invert the logic as does the driver (Figure 11). It has a high impedance input so can be economically used in circuits already working at a high impedance level. It is inherently self-clamping, and when returned to the large negative voltage, the amplitude loss is negligible.

### 3.64 Permanently Recorded Channels

Special equipment is required in the initial construction of the machine to record the three permanent channels on the drum. The most elaborate of these is the word channel, since the octal digits from 0 to 63 must be recorded circumferentially around the drum. It is also necessary to permanently record the clock channel on the drum. This is done in the following way: a 100 kc sine wave from an accurately calibrated source is fed into a counter which gives an end-carry pulse each 2688th cycle. The speed of the drum is then carefully adjusted to obtain one revolution per end-carry from the counter. When the speed is properly adjusted, the 100 kc signal is recorded for one revolution of the drum. In operation in the computer, the clock pulse is sensed, amplified and applied to a Schmitt circuit which provides the 100 kc square wave as a common "proposition" throughout the logical net.

The other permanently recorded channel is called the start-pulse channel. It gives a pulse at the beginning of every word time. It is used to synchronize the pulse and octal digit counters on the beginning of a word time when the machine is started. Thus the proper timing propositions can be utilized to select any pulse in any given word time, as has been described previously.

#### 4.0 TESTING AND TROUBLE-SHOOTING

##### 4.1 Methods of Trouble-Shooting

It is very difficult in this machine to use standard signal tracing techniques in tracking down trouble. Checking is done by means of the logical equations, from which it can be determined what voltage level must be present at a certain point in the machine at a specific time. For example, if the program counter "hangs up" at a particular block in the flow diagram, one can tell from the equations what sequence of gating is necessary and where the gates should come from, in order for program counter to continue its normal sequence. By referring to the schematic diagram, and by judicious pulling of key crystal diodes on the board, portions of the logical net and circuits can be isolated and the trouble traced.

It is possible to observe what happens, to some extent, by continually repeating a part of the program and watching the waveform of the suspected circuit with an oscilloscope, or one can check voltage levels throughout a part of the net. Suspected diodes can be checked by the crystal checker to see if any deterioration had occurred and if the diodes meet the required standards. Incorporated on the diode board are a group of switches which will permit the program to "jump" into a particular program count, or go on to its completion. By setting another group of switches, the program can be made to jump back into the rest position. In this way any section or step of the flow diagram can be isolated and a cycle can be made to repeat so the action can be observed on an oscilloscope. No push-button pulse checking in this machine is possible as it is in Whirlwind I; the trouble-shooting must be done dynamically. There is no alarm indication in CADAC, and generally speaking, improper functioning of the computer is indicated when no or wrong answers to test programs are typed out on the output typewriter, or unintelligible answers come out, or, of course, when smoke starts pouring out of the machine.

##### 4.2 Difficulties in Trouble-Shooting

The complexity of interconnections among the logical circuits caused the wiring of the diode boards to become rather messy and inaccessible. A technique of using the diode-net resistances to support the bus wire which delivers  $B_1$  to the net was used in many places. There was no consistent color coding of the interconnecting wires; this makes them difficult to trace. Vector turret miniature sockets upon which the components associated with the tubes are mounted were used throughout the machine. Although this method assures the rigidity of the components, it does make the tube socket pins and the components inaccessible. The memory and circulating register components were mounted in the form of sub-assemblies which are subject to vibration of the drum rotation.



Loose and intermittent connections of the diodes in their clips  
have given rise to some trouble.

SIGNED Everett A. Emerson  
Everett A. Emerson

Arnold M. Werlin  
Arnold M. Werlin

APPROVED E. S. Rich  
E. S. Rich

EAE/AMW/cp

Appendix, Page 21

Drawings: A-50870

A-50871

A-50872

A-50873

A-50874

cc: R. R. Everett  
C. W. Adams

APPENDIXSample CADAC Program

Attached is an example of a CADAC program and the form in which the output typewriter prints results.

I. PROGRAM

The Program is designed to convert a table of coded decimal numbers to octal and to print the address of the coded decimal number with the number, followed by the octal equivalent. The first address of the table is in the  $m_1$  position of register 0410, note 0500. Those positions crossed out are immaterial to the proper operation of the program. The program is started at register #0404.

II. TABLE OF DECIMAL NUMBERS

The table consists of eight numbers coded so that the decimal value is represented by two octal digits according to the following convention.

<u>Decimal #</u>	<u>Coded Equivalent</u>	<u>Decimal #</u>	<u>Coded Equivalent</u>
0	00	5	05
1	01	6	06
2	02	7	07
3	03	8	53
4	04	9	54

The eight values are:

<u>Register</u>	<u>Value</u>	<u>Register</u>	<u>Value</u>
0500	<del>/.999999</del>	0504	<del>/.30103</del>
0501	<del>-.5</del>	0505	<del>/.47712</del>
0502	<del>/.875</del>	0506	<del>/.60206</del>
0503	<del>-.0625</del>	0507	<del>/.69897</del>

III. REQUIRED RESULTS; TABLE OF CODED DECIMAL NUMBERS AND THEIR OCTAL EQUIVALENTS

The CADAC performed the computation according to the program and typed out the required results in about 100 seconds of total operating time.

All of the numbers on the attached page were typed by the CADAC typewriter on the reproducing master. Tables I and II were printed by using a print out from storage routine. Table III is the required results printed from the program. The printed headings were added afterward.

I. PROGRAM

0404-17041004430405	0405-17051004440435	0406-15043504550442	0407-23044200000411
0410-37050000000000	0411-17040504430430	0412-17040504430431	0413-13044604460436
0414-13044604500442	0415-13044604460440	0416-15044604470441	0417-17043504450437
0420-07044204370454	0421-13045404360436	0422-11043504470435	0423-13044104470441
0424-21044704410417	0425-07044204510442	0426-13044004470440	0427-21045204400416
0430-17050704460436	0431-31050700000000	0432-25043600000000	0433-13040504530405
0434-21044704460405	0435-01000000000000	0436-01545676625256	0437-01000000000000
0440-01000000000022	0441-01000000000003	0442-01777777777777	0443-00777700000000
0444-02777777777777	0445-01700000000000	0446-01000000000000	0447-01000000000003
0450-01631463146314	0451-01063146314632	0452-01000000000020	0453-01000100000000
0454-01000000000000	0455-00777777777777		

II. TABLE OF CODED DECIMAL NUMBERS

0500-01545454545454	0501-00050000000000	0502-01530705000000	0503-00000602050000
0504-01030001000300	0505-01040707010200	0506-01060002000600	0507-01065453540700

III. TABLE OF CODED DECIMAL NUMBERS AND OCTAL EQUIVALENTS

0500-01545454545454	01777777571622	0501-00050000000000	00400000000000
0502-01530705000000	01700000000001	0503-00000602050000	00040000000000
0504-01030001000300	01232101152522	0505-01040707010200	01364222112305
0506-01060002000600	01464202325244	0507-01065453540700	01545676625256

# ELECTRONIC BUILDING BLOCKS

FIGURE 1: FLIPFLOP & DRIVERS

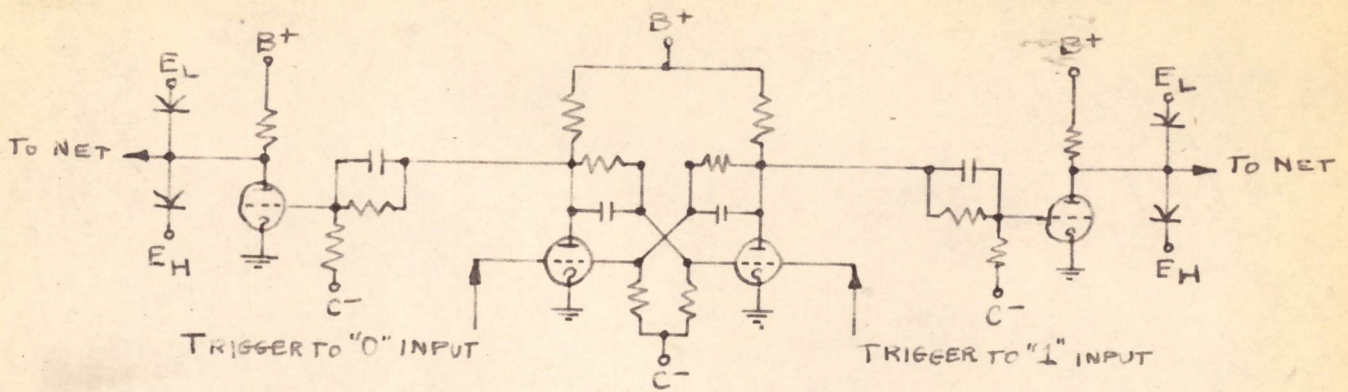


FIGURE 2: PRODUCT

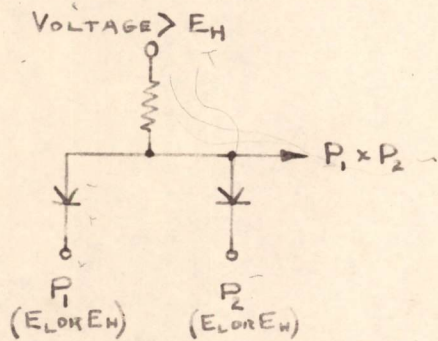


FIGURE 3: SUM

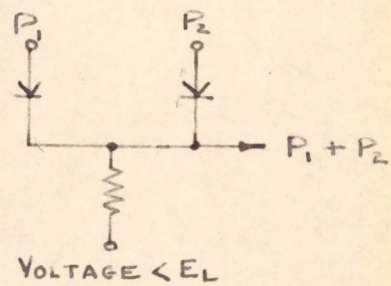


FIGURE 4: NEGATIVE

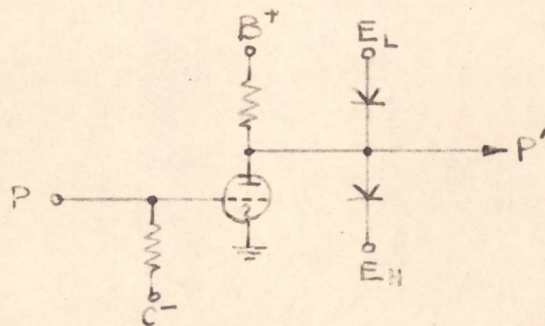
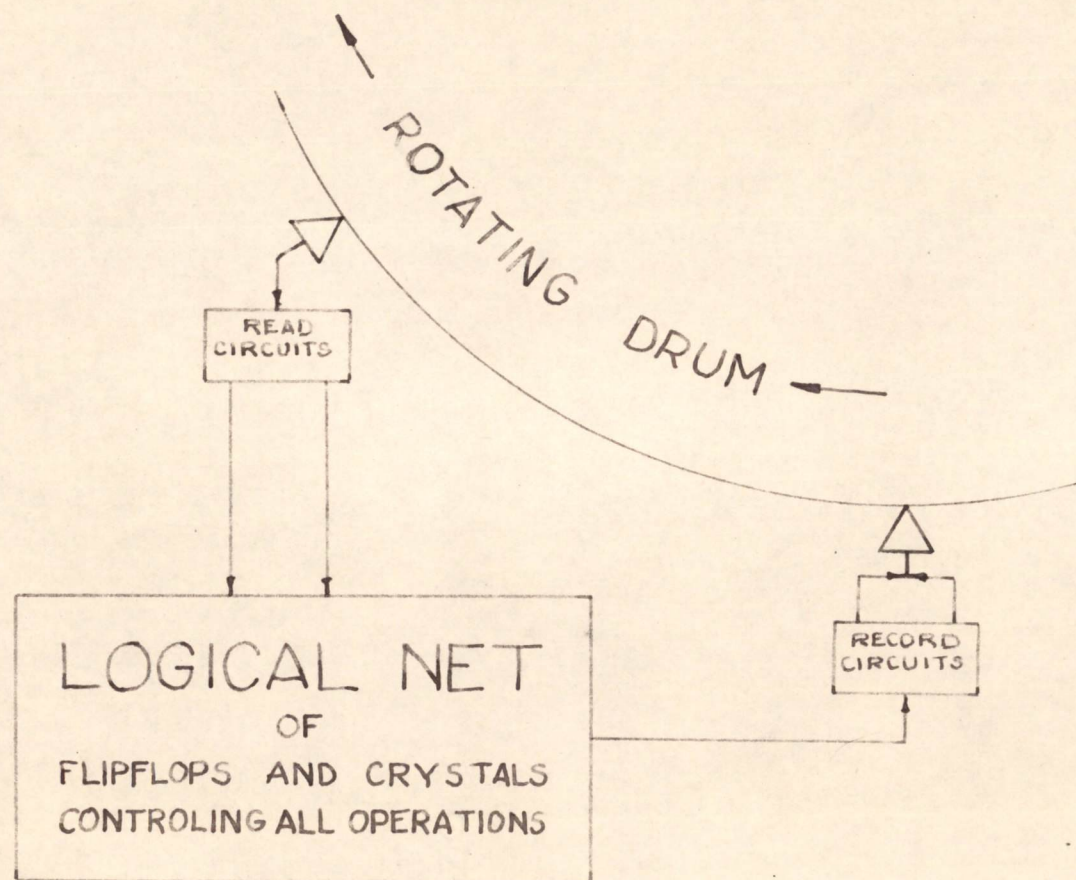


FIGURE 5: TRUTH TABLES OF LOGICAL OPERATIONS

$P_1$	$P_2$	$P_1 \times P_2$	$P_1 + P_2$	$P_1'$
0	0	0	0	1
1	0	0	1	0
0	1	0	1	1
1	1	1	1	0

FIGURE 6: DESCRIPTIVE DIAGRAM OF A RECIRCULATING REGISTER

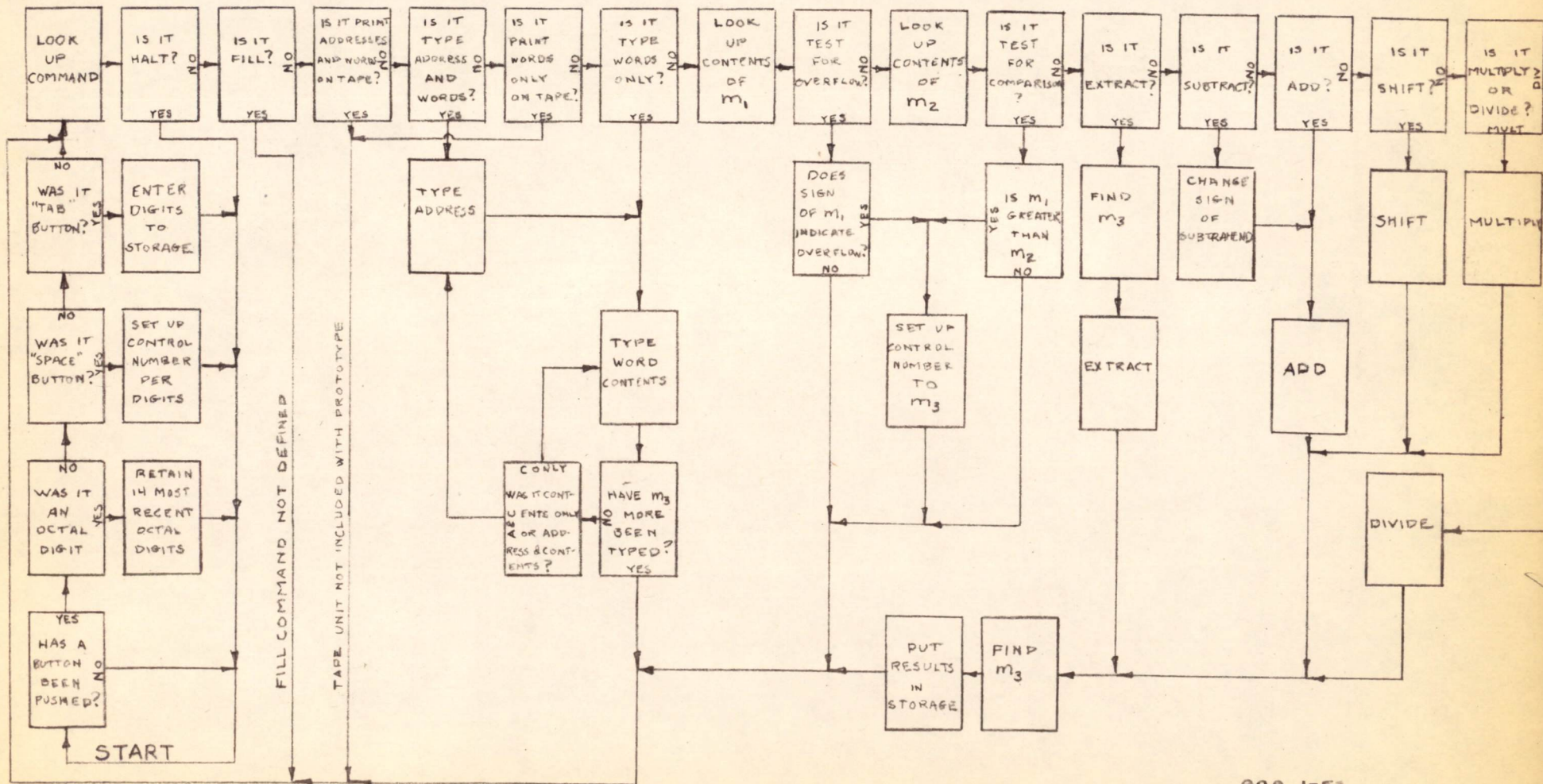


eae 1-52

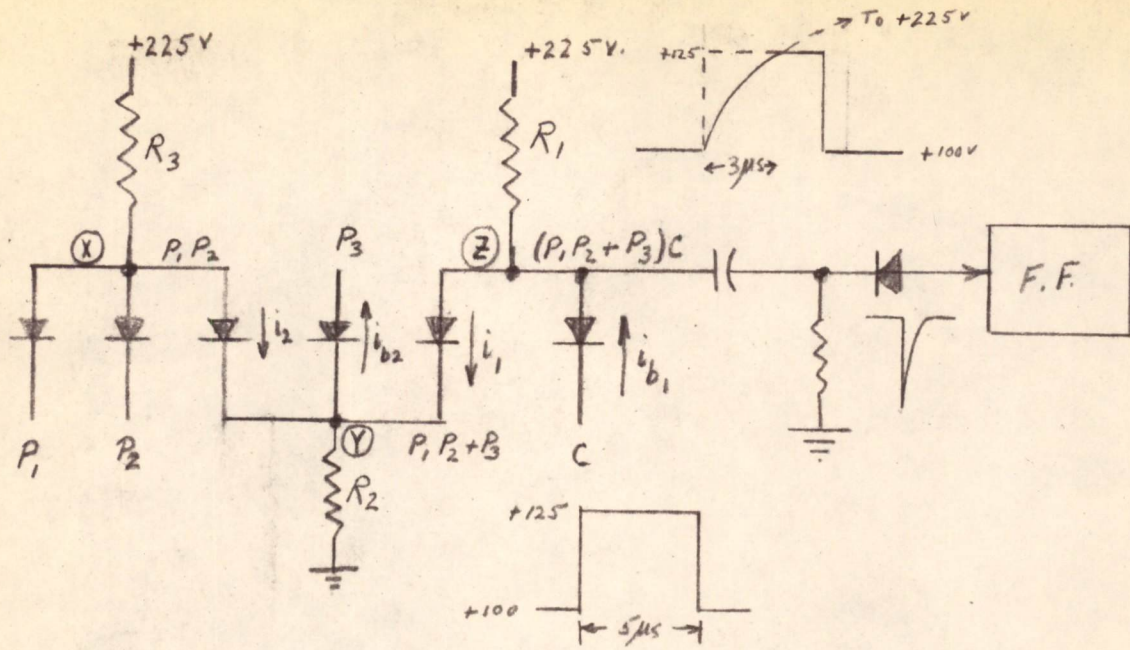
# FLOW DIAGRAM OF INTERNAL OPERATIONS (ABRIDGED)

FROM COMPUTER RESEARCH CORPORATION  
QUARTERLY PROGRESS REPORT NUMBER 2

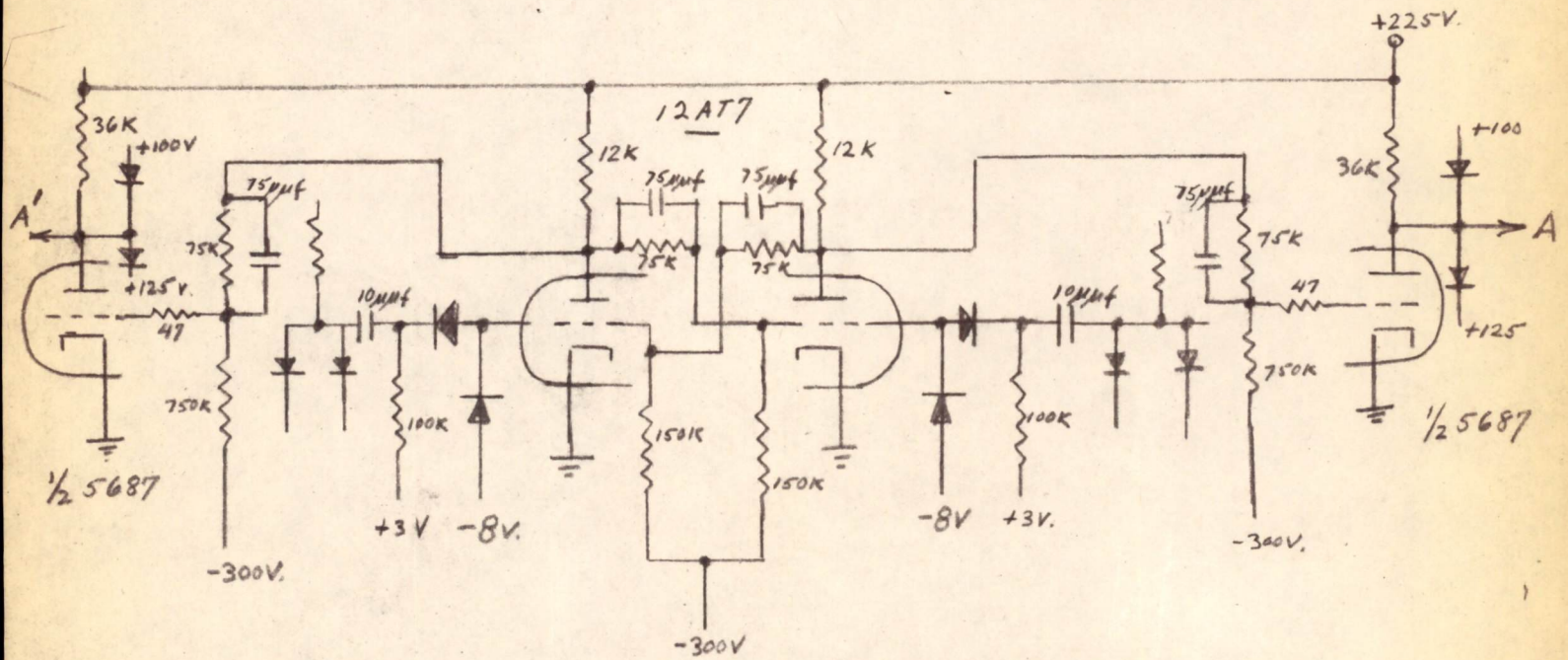
FIGURE 7:



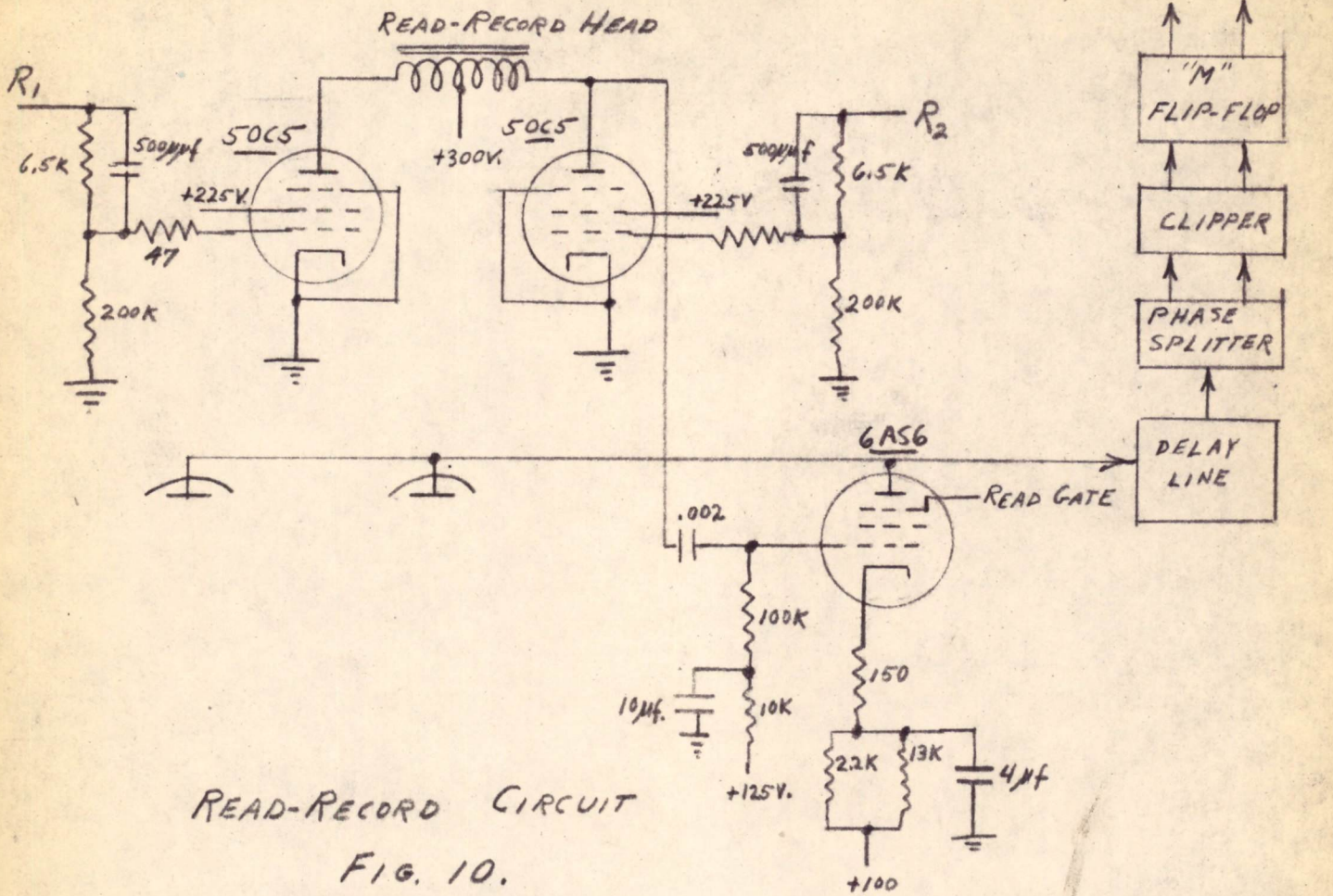
eqe 1-52



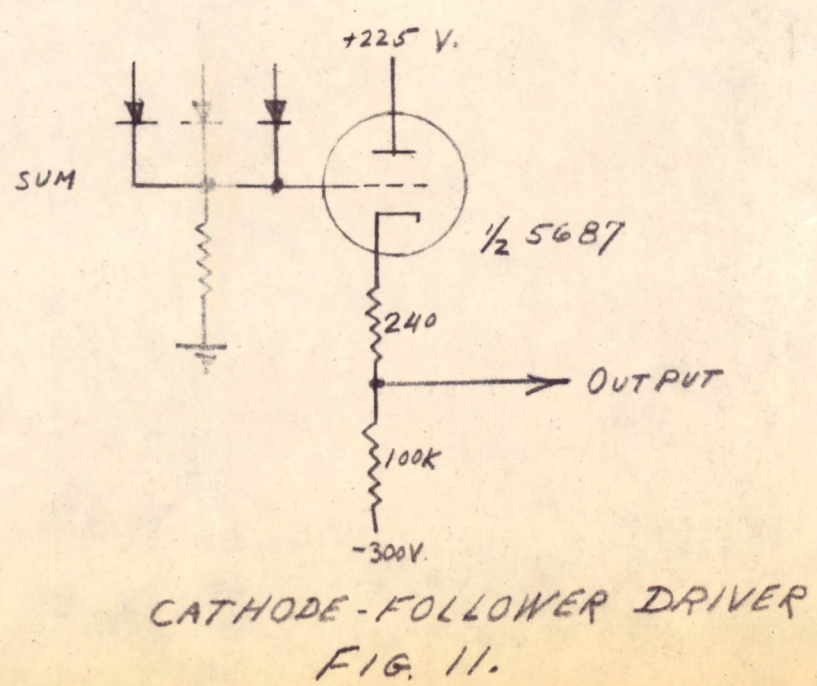
TYPICAL DIODE NET  
FIG. 8.



CADAC FLIP-FLOP  
FIG. 9.



READ-RECORD CIRCUIT  
FIG. 10.



CATHODE-FOLLOWER DRIVER  
FIG. 11.



*J. H. Foxworth*

6889

Engineering Note E-451

Page 1 of 3

Digital Computer Laboratory  
Massachusetts Institute of Technology  
Cambridge, Massachusetts

SUBJECT: VARIATION OF TRANSISTOR COLLECTOR RESISTANCE WITH COLLECTOR VOLTAGE

To: 6889 Engineers

From: Nolan T. Jones and Robert J. Callahan

Date: March 3, 1952

Abstract: The variation of collector resistance with collector voltage has been observed for most of the available transistors. The minimum values of collector resistance differ widely from that obtained at the value of collector voltage used for the standardized D-C point measurement;<sup>1</sup> while the maximum values differ generally by not more than 20%.

Introduction:

The value of  $r_{CO}$  measured at  $V_C = -15$  volts has been tentatively defined as a meaningful value of the collector back resistance.<sup>1</sup> However, non-linearities of this parameter have been apparent, making an analysis of the variation desirable.

Detailed investigation of the collector characteristic was also made in the region of small negative values of  $V_C$  for a few of the transistors.

Deviation of  $r_{CO}$ :

Table 1 lists the values of  $r_{CO}$  for  $V_C = -15$  volts (the standardized point measurement) and the maximum and minimum values of  $r_{CO}$ . Most of the minimum values of  $r_{CO}$  occur at small values of  $V_C$ . The maximum values of  $r_{CO}$  are generally within 20% of the value obtained for the D-C point test measurement. The major exceptions to both of these generalizations are Raytheon transistors #56, 58, 59 and 24. These units all have low current gain ( $\alpha < 1$ ). Plots of  $r_{CO}$  vs.  $V_C$  are shown in drawings SA-48309G to SA-48315G.

Because of the relatively large differences between the minimum and D-C test point values, it was felt that a more complete investigation of the  $I_{CO} - V_C$  characteristics for low values of  $V_C$  might show enough curvature to warrant

---

1. Jacobs, John F. and Jones, Nolan T., Standard Transistor Parameter Measurements, E-441.

a resistance and current generator as a representation of  $r_{co}$ . The results of this investigation indicate that in most cases this curvature is not serious enough to require such a representation. Characteristics of the transistors investigated are shown in drawings SA-48316G to SA-48318G.

Signed R. J. Callahan  
R. J. Callahan

Nolan T. Jones  
Nolan T. Jones

Approved John F. Jacobs  
John F. Jacobs

Approved Norman Taylor  
Norman Taylor

RJC:NTJ:jk

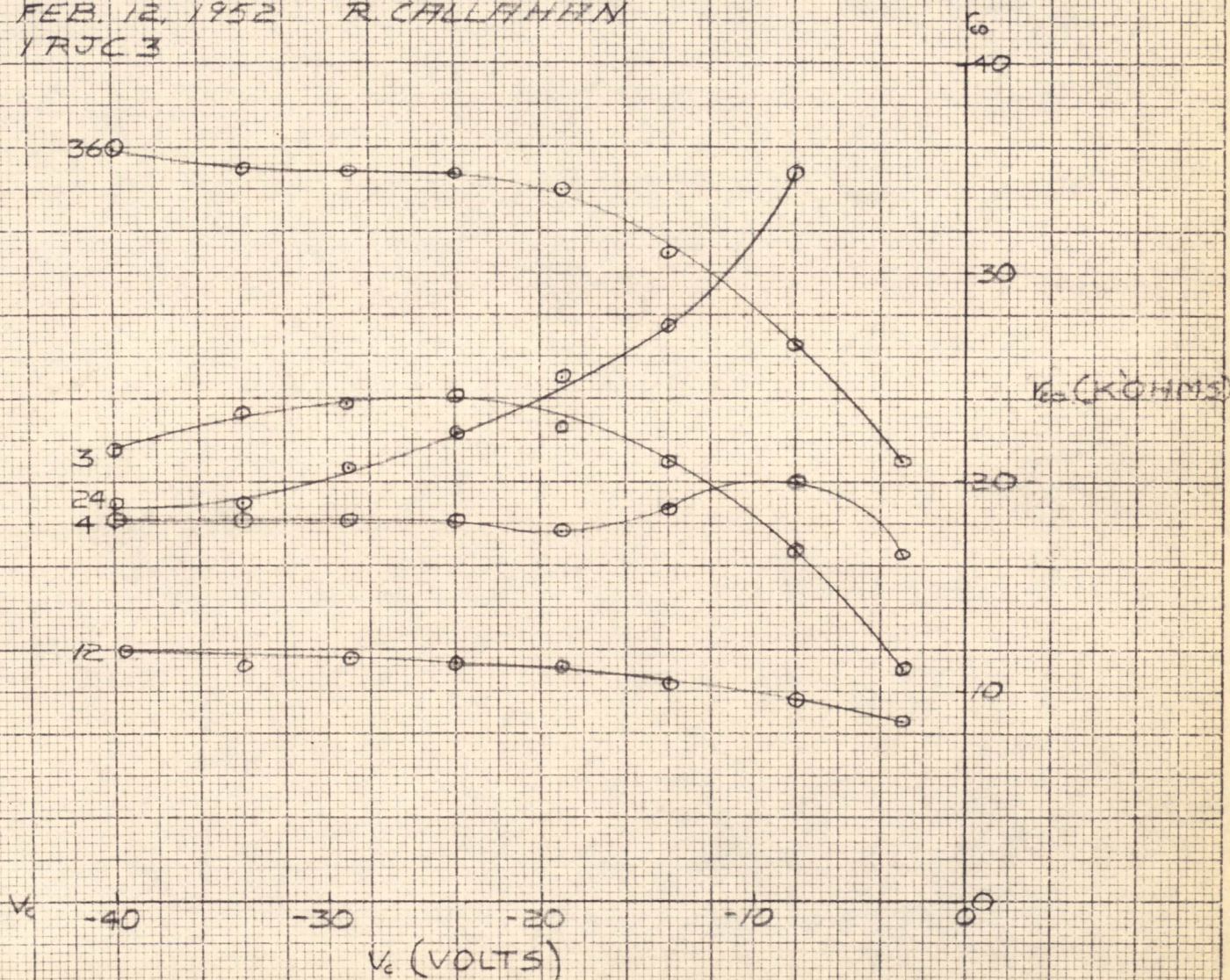
Illustrations:

SA-48309G  
SA-48310G  
SA-48311G  
SA-48312G  
SA-48313G  
SA-48314G  
SA-48315G  
SA-48316G  
SA-48317G  
SA-48318G  
Table 1

cc: Standard Transistor Dist. (15)

SA-48309-G

VARIATION OF  $K_0$   
 $K_0$  vs  $V_c$  AT  $I_c = 0$   
RAYTHEON CK716 Nos 3, 4, 12, 24, 36  
FEB. 12, 1952 R. CALLAHAN  
1RJC3



SA-48309-G ✓

SA-48310-G

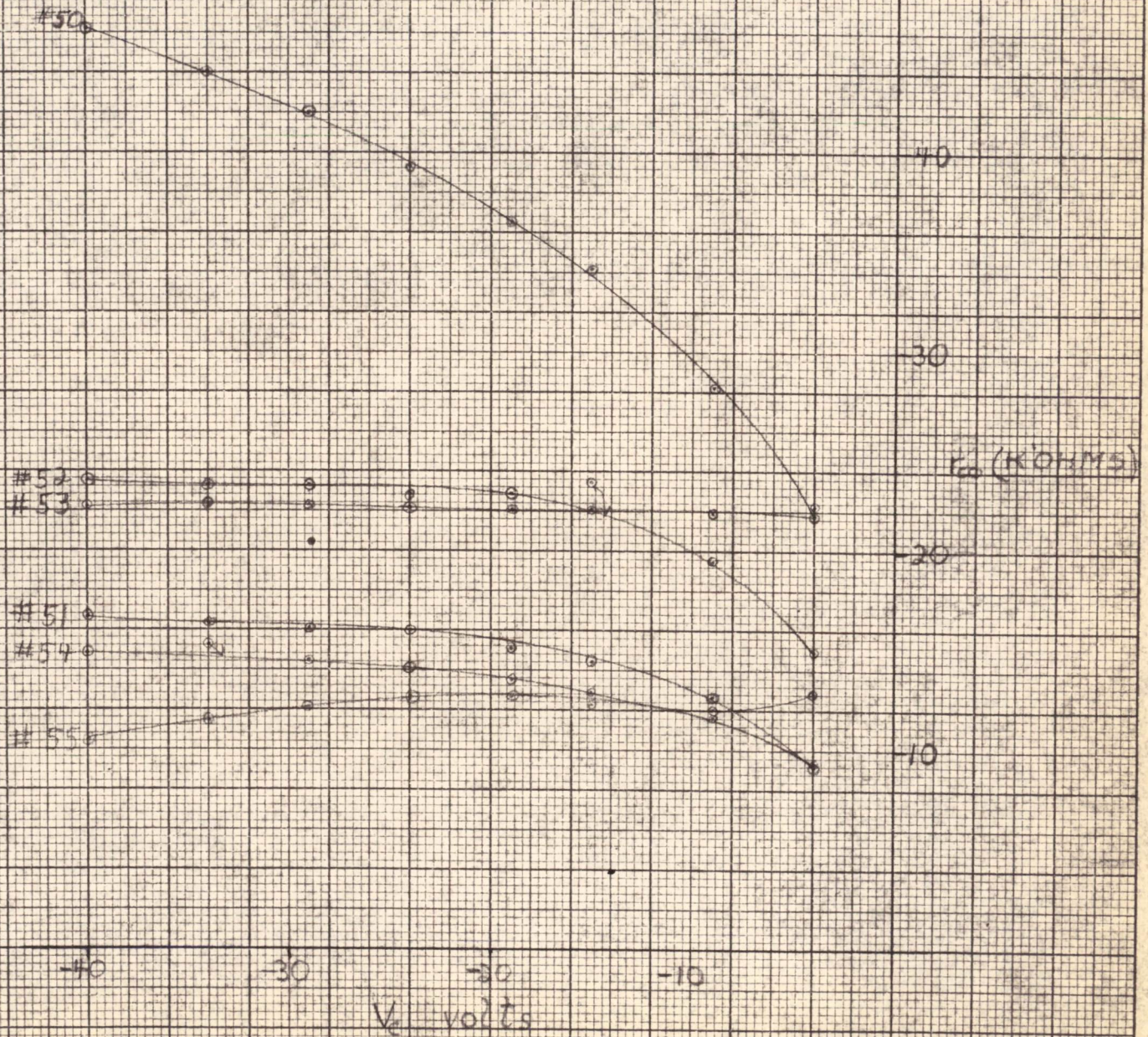
### VARIATION OF $Y_{co}$

$Y_{co}$  vs  $V_c$  at  $I_c = 0$

Raytheon Type CR716

Feb. 2, 1952 N. Presbiter

IRJC3



SA-48310-G

SA-48311-G

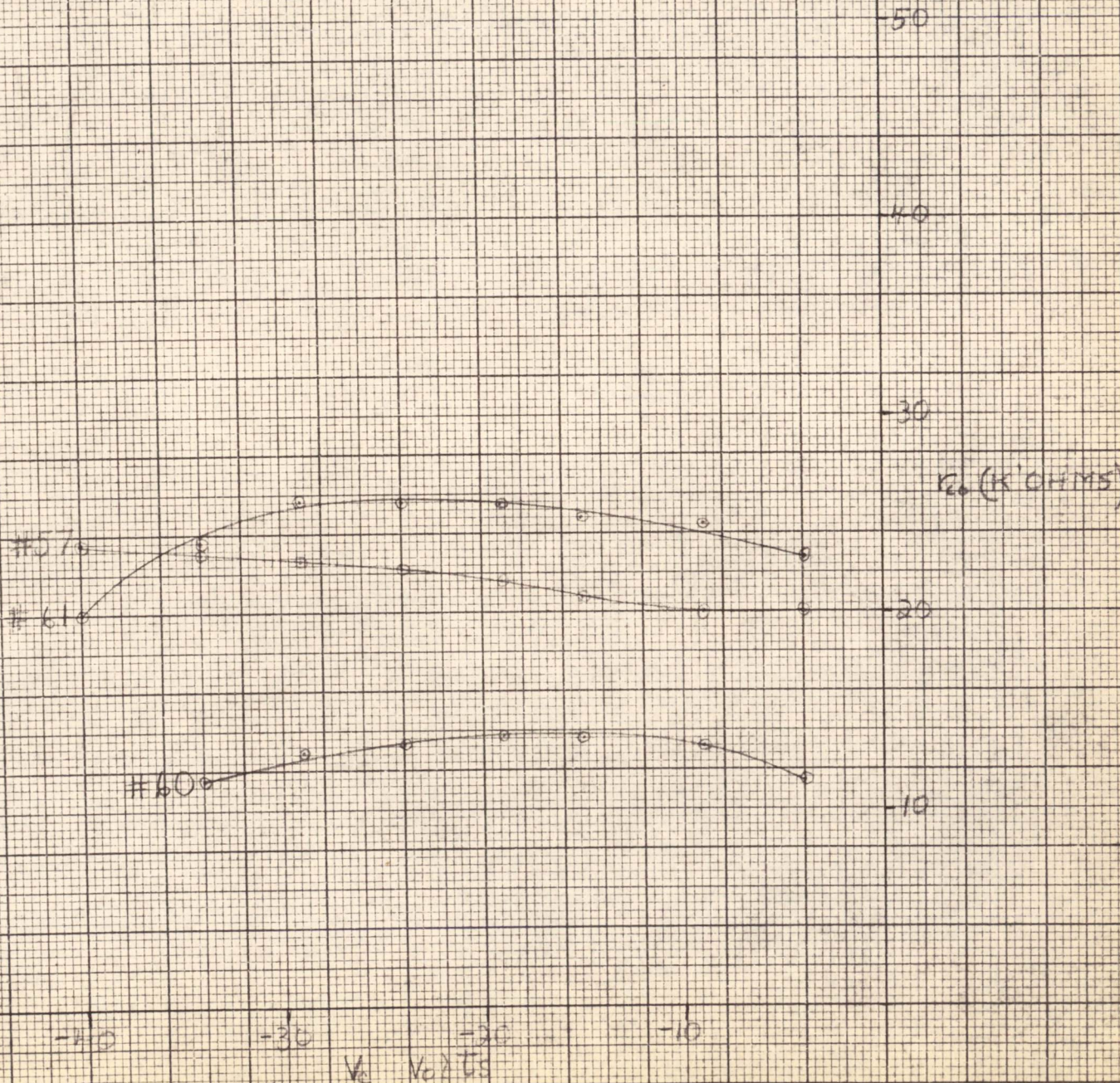
### VERIFICATION OF $r_{cb}$

$r_{cb}$  vs.  $V_c$  at  $I_c = 0$

Playtron Type CK-716

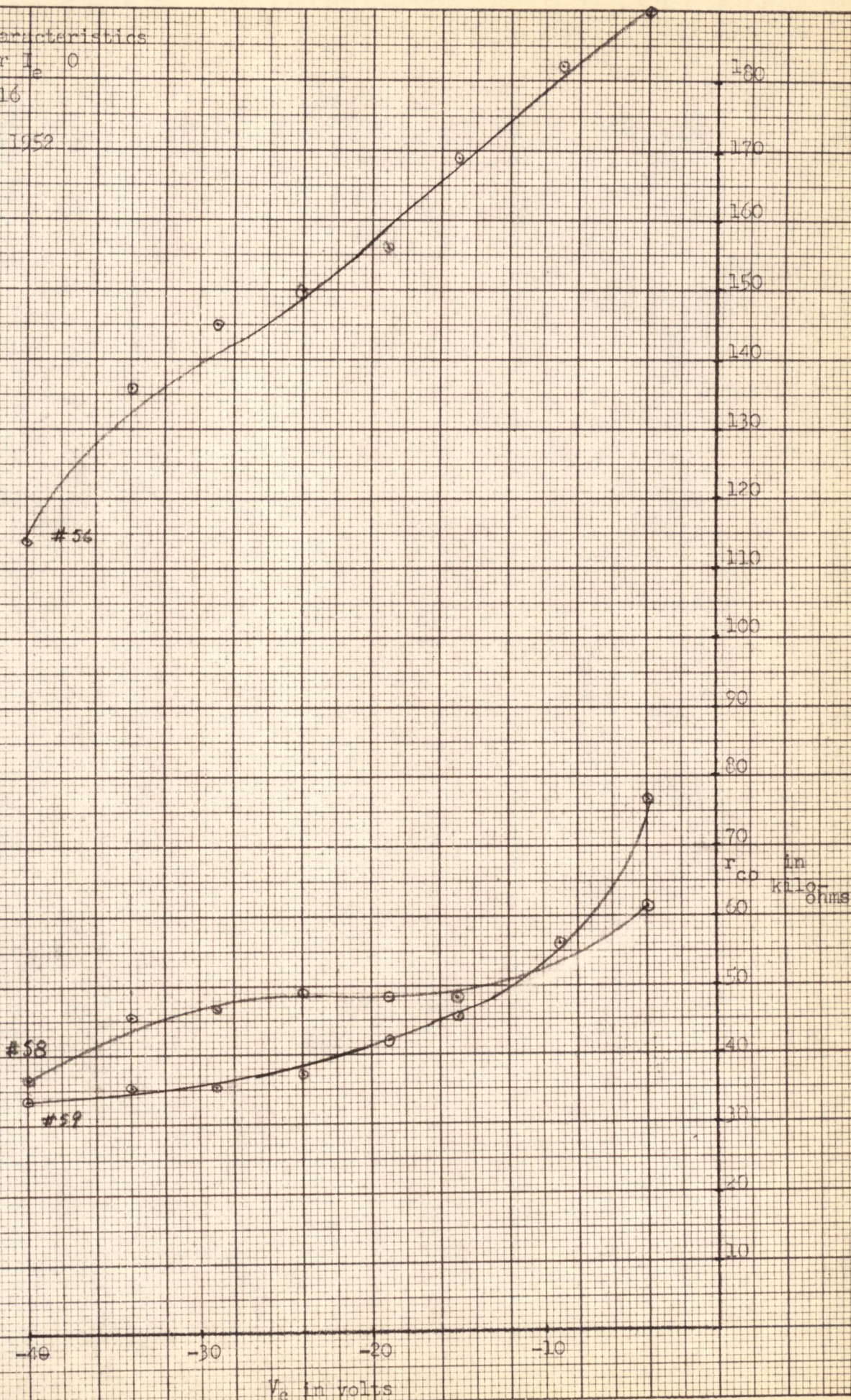
Feb 21, 1952 N. Prizbick

IRSC-3



SA-48311-G-✓

Collector Characteristics  
 $r_{co}$  vs  $V_c$  for  $I_e = 0$   
 Raytheon CK716  
 #56, 58, 59  
 February 23, 1952  
 n. Pribble



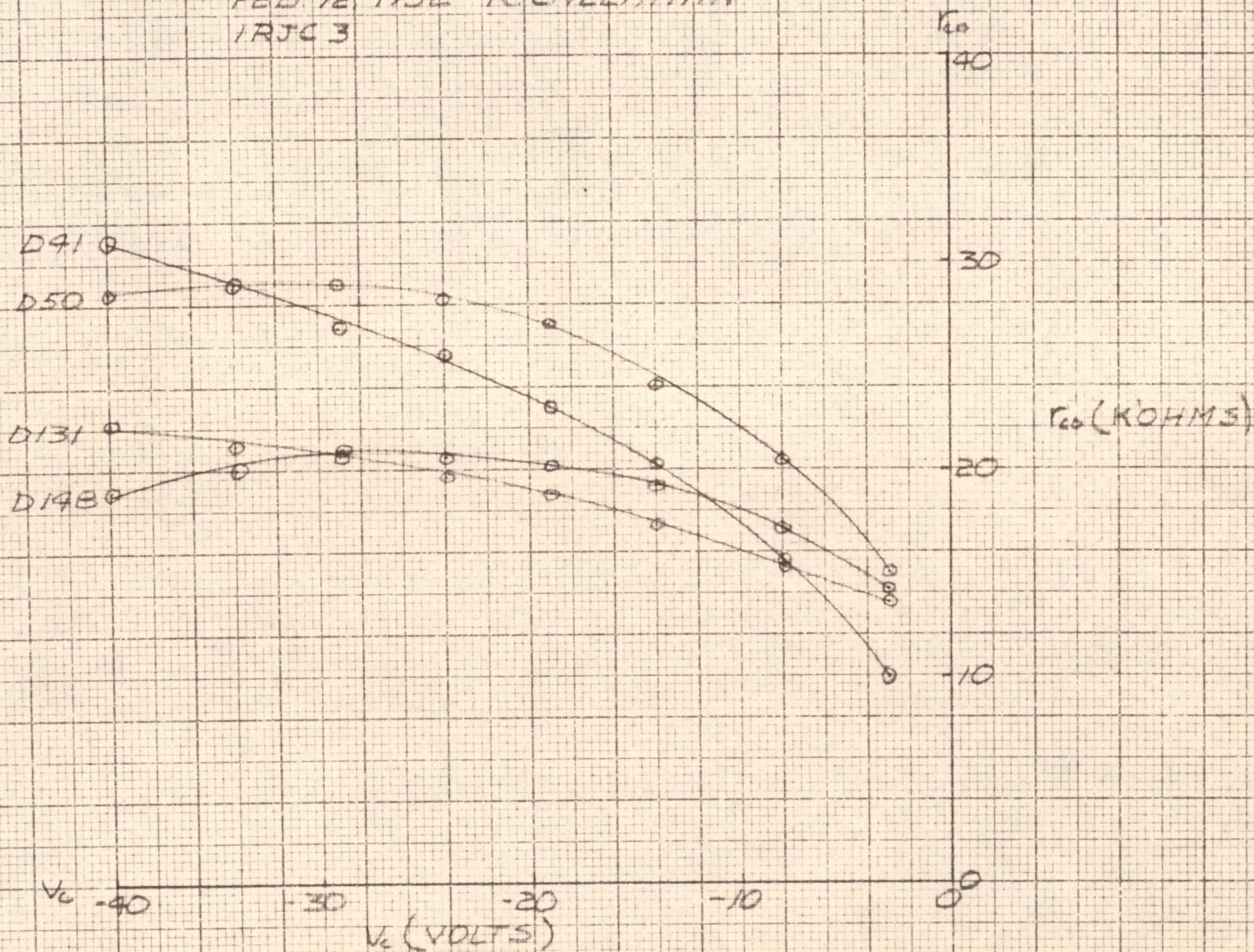
359T-12G KEUFFEL & ESSER CO.  
 10 X 10 to the 1/2 inch, 5th lines accented.  
 MADE IN U. S. A.

SA-48312-G

SA-48312-G

SA-48313-G

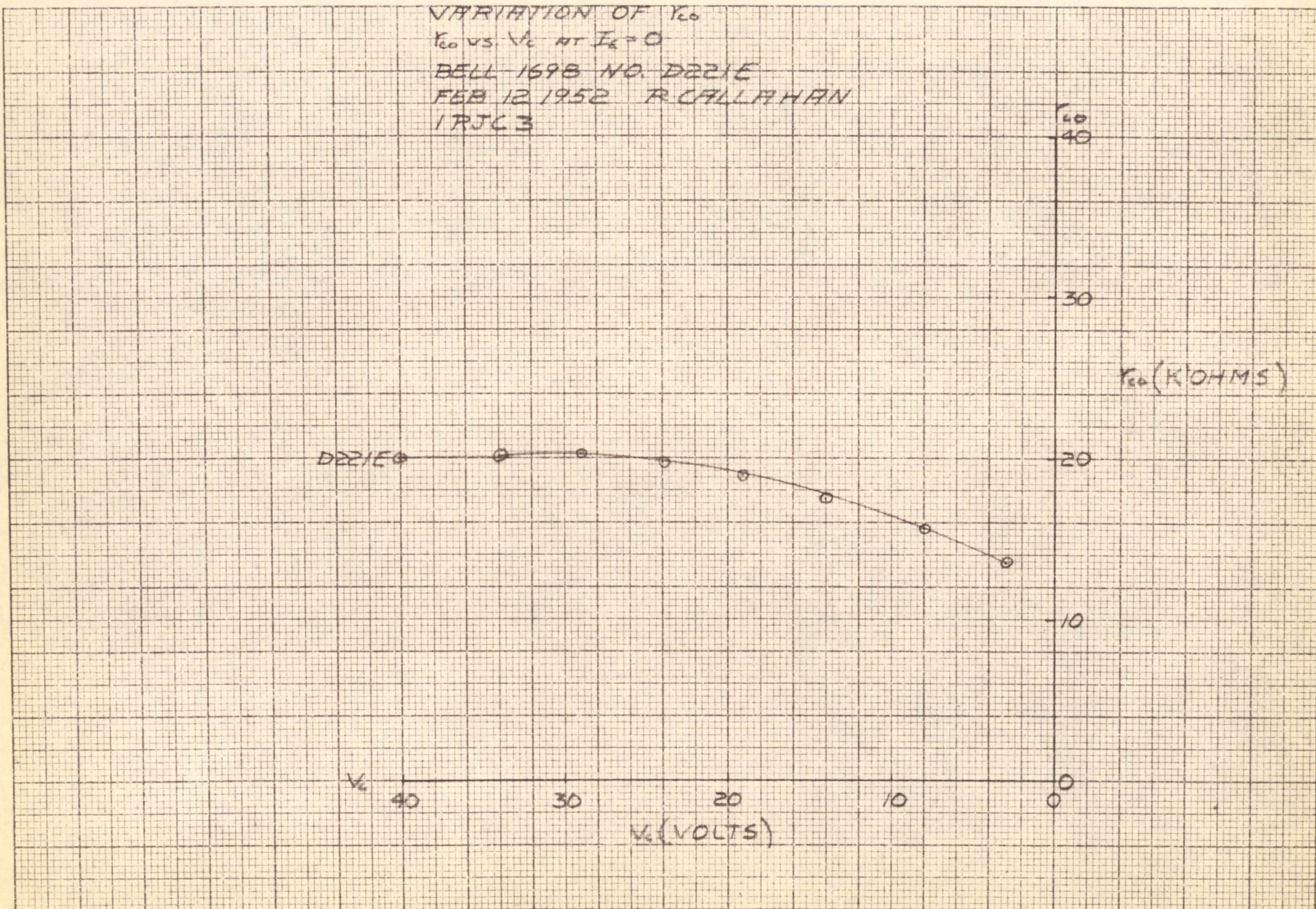
VARIATION OF  $r_{co}$   
 $r_{co}$  vs.  $V_c$  at  $I_c = 0$   
GE GIUR NOS D91, D50, D131, D148  
FEB 12, 1952 R. CALLAHAN  
IRJC 3



SA-48313-G ✓

SA-48314-G

VARIATION OF  $r_{co}$   
 $r_{co}$  vs.  $V_c$  AT  $I_c = 0$   
BELL 1698 NO. D221E  
FEB 12 1952 R. CALLAHAN  
1RJC3

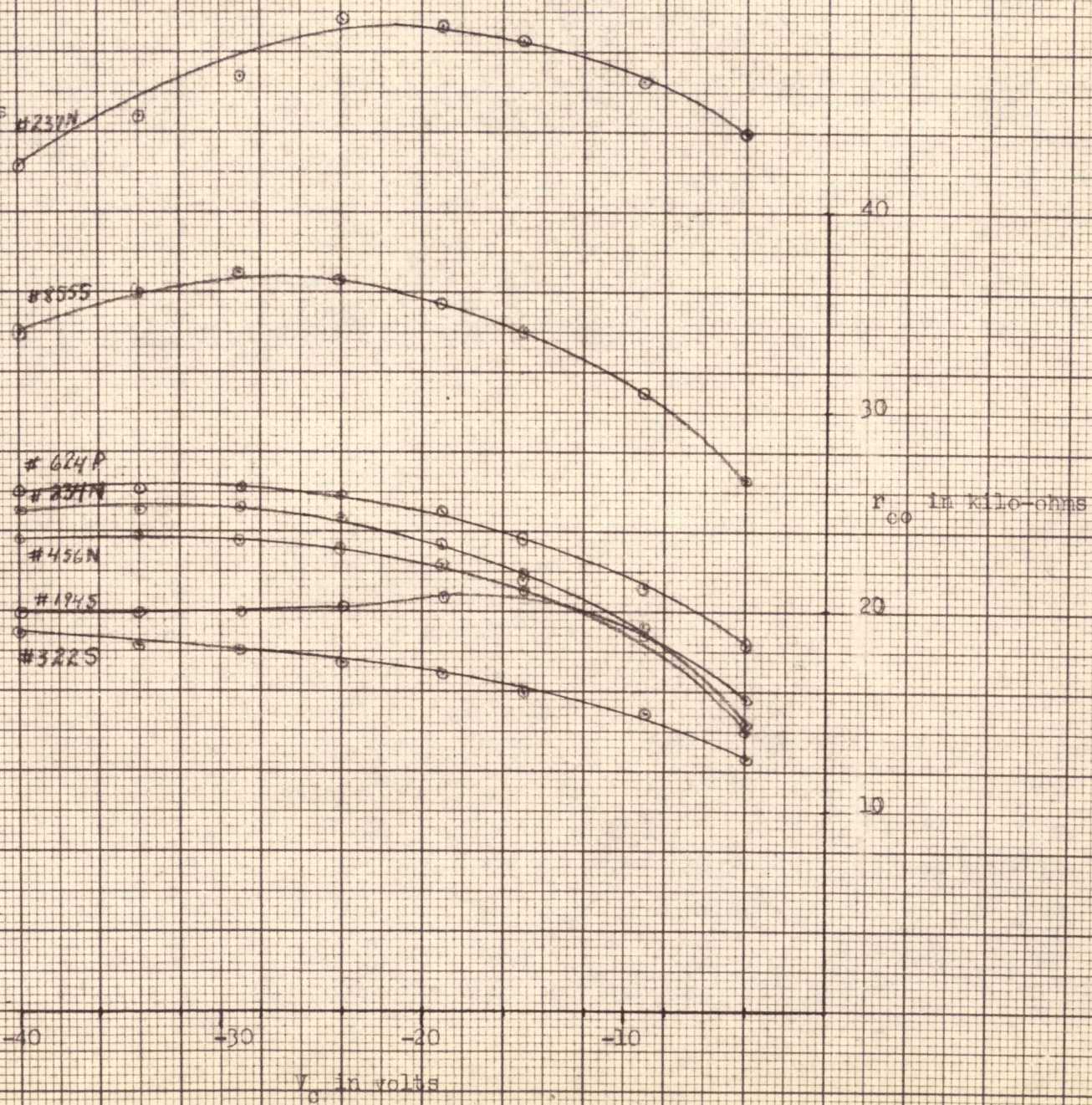


SA-48314-G-✓



SA-48315-G

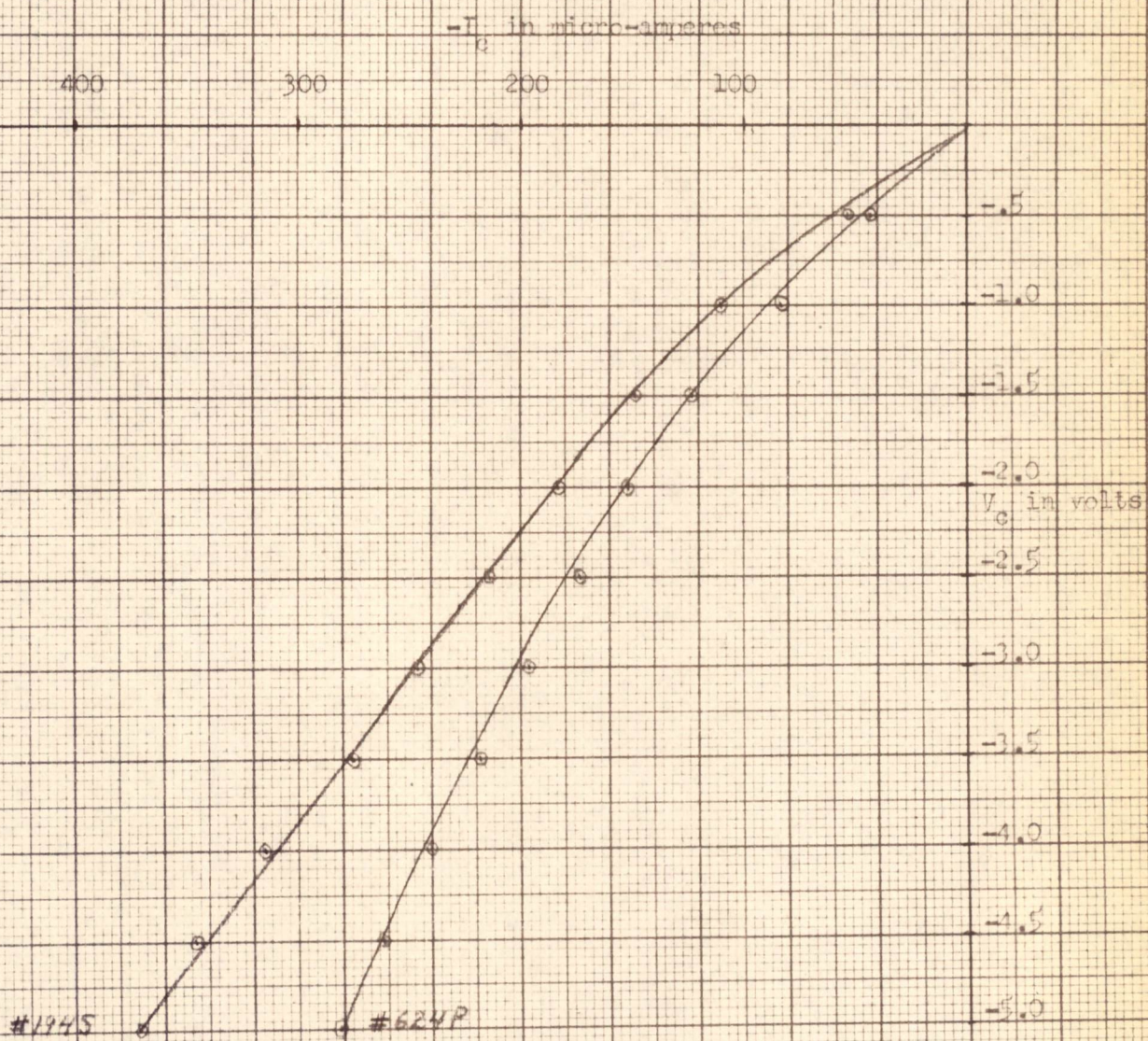
Collector Characteristics  
 $r_{co}$  vs  $V_c$  for  $I_e = 0$   
Bell 1698 #D237N, D855S,  
D424P, D234N, D456N, D194B,  
D322S,  
February 22, 23, 1952  
S. W. Teicher



SA-48315-G ✓

SA-48316-G

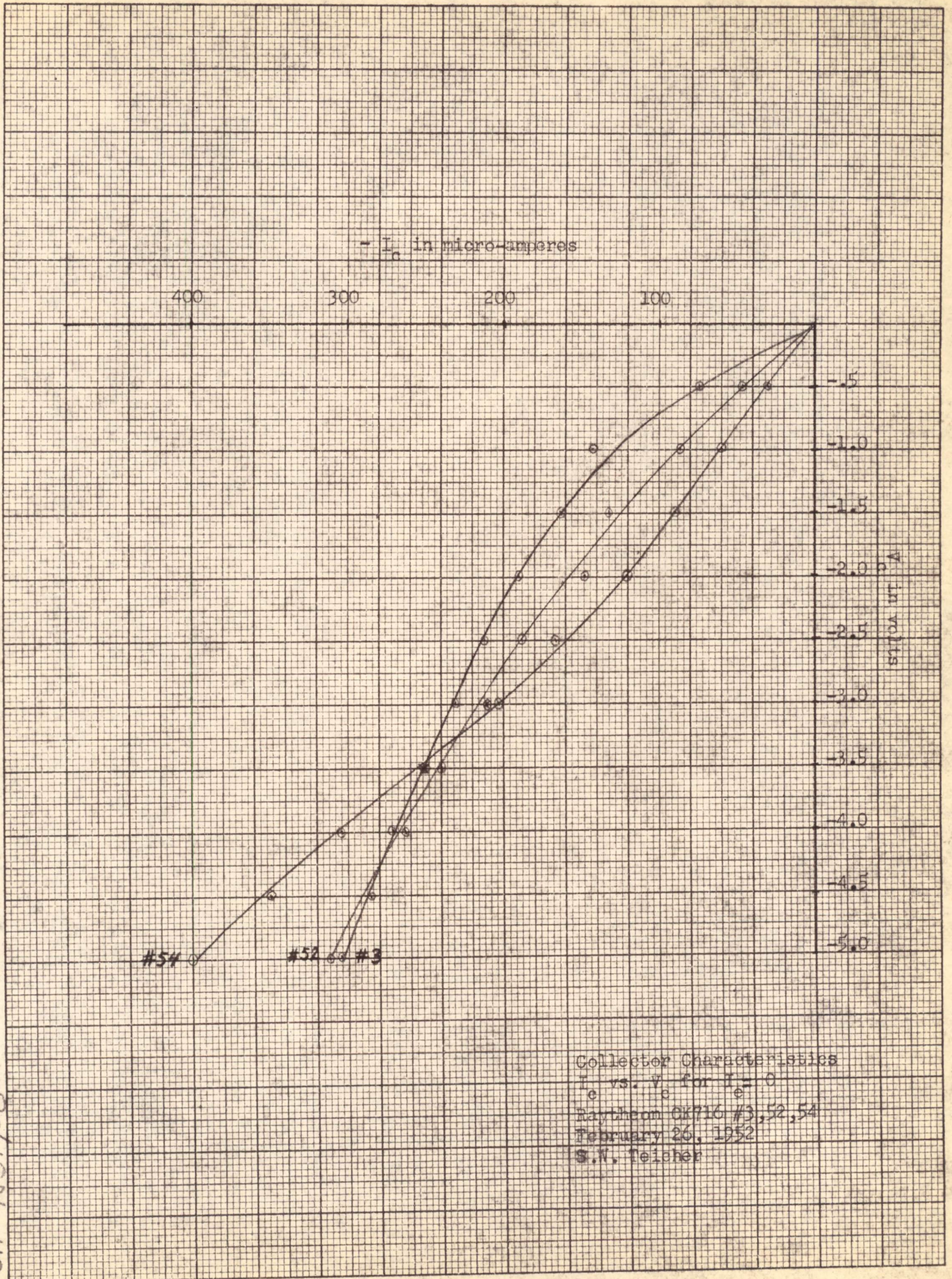
SA-48316-G



Collector Characteristics  
 $I_c$  vs  $V_c$  for  $I_b = 0$   
Bell 169B #D624P, D194S  
February 20, 1952  
S.W. Teicher

SA-48317-G

SA-48317-G

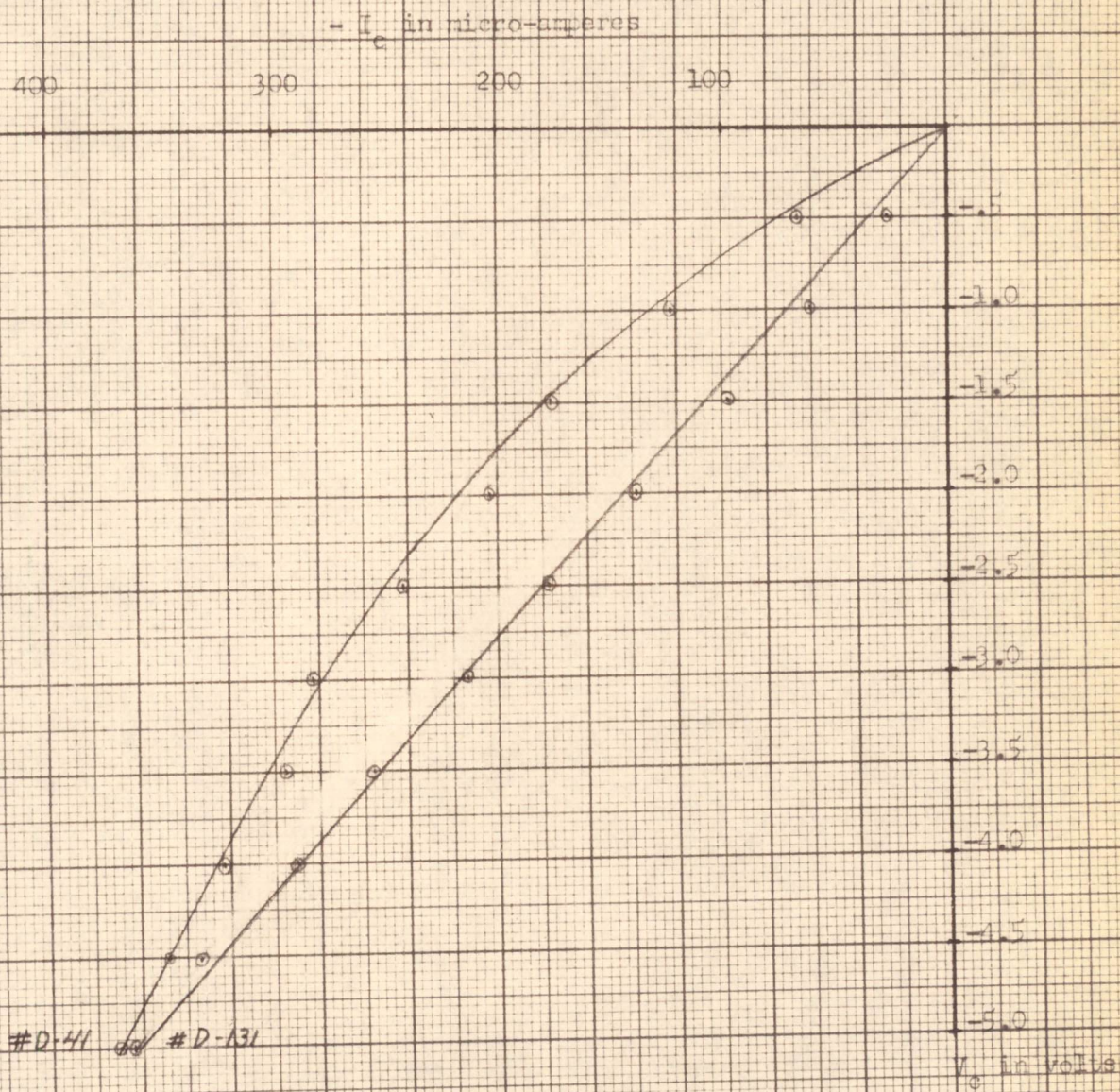


Collector Characteristics  
 $I_c$  vs.  $V_c$  for  $I_e = 0$   
Raytheon CK716 #3, 52, 54  
February 26, 1952  
S.N. Teicher

359T-12G KEUFFEL & ESSER CO.  
10 X 10 to the 1/2 inch, 5th lines accented.  
MADE IN U. S. A.

SA-48318-G

SA-48318-G



Collector Characteristics  
 $I_c$  vs  $V_c$  for  $I_e = 0$   
G.E. GLA #D41, D131  
February 26, 1952  
S.W. Fechner

Table 1  
Deviation of  $r_{co}$  from the D-C Point Test Value

Transistor

Manufacturer	Type	Serial No.	D-C Point Test Value ( $V_c = -15$ volts) K' ohms	Maximum K' ohms	Minimum K' ohms
Raytheon	CK716	3	21.6	24	11
Raytheon	CK716	4	18.4	20	16.6
Raytheon	CK716	12	9.9	12	9.6
Raytheon	CK716	24	26.8	34.8	19
Raytheon	CK716	36	32	36	21
Raytheon	CK716	50	34.2	44	22.2
Raytheon	CK716	51	14.4	9.2	16.6
Raytheon	CK716	52	22	15	23.4
Raytheon	CK716	53	22	19.8	22.4
Raytheon	CK716	54	12.8	9.2	14.8
Raytheon	CK716	55	12.4	12.8	10.6
Raytheon	CK716	56	169	200	114
Raytheon	CK716	57	20.8	23.5	20
Raytheon	CK716	58	48.5	61.5	36.5
Raytheon	CK716	59	45.5	77	33.2
Raytheon	CK716	60	13.6	13.8	11.4
Raytheon	CK716	61	22.8	23.7	20
G. E.	G11A	D41	20.8	31	10
G. E.	G11A	D50	25	29	15
G. E.	G11A	D131	17.7	20.2	13.6
G. E.	G11A	D148	19.6	21	14.2
Bell	1698	D221E	18	20.4	13.5
Bell	1698	D234N	21.8	25.2	14
Bell	1698	D237N	48.5	42	49
Bell	1698	D456N	21.6	23.9	15.6
Bell	1698	D624P	23.8	26.3	16.4
Bell	1698	D194S	21.2	21.2	14.4
Bell	1698	D322S	16	19	12.7
Bell	1698	D855S	34	37.2	28.6

R. Buck

Digital Computer Laboratory  
Massachusetts Institute of Technology  
Cambridge, Massachusetts

SUBJECT: A NON-DESTRUCTIVE READ SYSTEM FOR MAGNETIC CORES

To: N. H. Taylor  
From: Dudley A. Buck  
Date: March 24, 1952

Abstract: A non-destructive read system for magnetic cores is proposed which involves a quadrature field and which promises to be fast.

The process of recalling information stored in the M. I. T. coincident-current magnetic-core memory is called destructive. The reading process destroys the information stored in a memory core, leaving that core in the "cleared" state regardless of whether it contained, just prior to reading, a ONE or a ZERO. The information which was destroyed during reading is re-written in the core as a routine part of the memory's operating cycle.

A non-destructive read system is proposed which would allow magnetic cores to be read repeatedly without loss of information. The system involves the use of a second magnetic flux path at the right angles to the first. When pulsed, the flux in the second path causes a momentary drop in the residual flux in the first path. If the residual flux is positive, the drop represents a negative change of flux; if, on the other hand, the residual flux is negative, the drop represents a positive change of flux. These changes are coupled to a sensing circuit via the write winding or via a separate sensing winding. A more detailed description of the proposed system follows.

Ring-shaped cores (Fig. 1a) of highly grain-oriented Molybdenum Permalloy are used as the memory cores in one of the M. I. T. memories. As a result of the rolling and magnetic annealing steps in the fabrication of these cores, their hysteresis loops are nearly rectangular, and they behave, in many respects, like single ferromagnetic crystals with easy directions of magnetization in the direction of rolling. A crystal of the material (Fig. 1b) is a cube with easy directions of magnetization along the cube edges. The magnetization vector of the crystal will, in the absence of an external field, lie along one of the cube edges.

Between any two directions of easy magnetization there is a hard direction (Fig. 1c). If the magnetization vector of the crystal were pulled to a hard direction by an external field, and then the external field were removed, the magnetization vector would snap back to the closest easy direction. This is the process that takes place on the upper and lower parts of the hysteresis loop for a magnetic material with a not-too-rectangular hysteresis loop. As one goes from the residual induction point to saturation (A to A' in Fig. 1d), the magnetization vectors of the domains in the material rotate into alignment with the applied field, increasing the induction. When the field is removed, each vector drops back to its closest easy direction

and the material is once again at the residual induction point. In the grain-oriented metal cores, easy directions of magnetization already lie along the direction in which the field is applied, so that the hysteresis loop is almost perfectly flat on top.

If a field is applied at right angles to the residual induction vector (Fig. 2a), the vector will be rotated away from its residual direction toward a hard direction. If the  $90^\circ$  field is not too strong, the vector will snap back to its residual induction position when the  $90^\circ$  field is removed. When the vector is rotated out of position, its component along the residual induction path drops in magnitude. The read/write winding on this path will see a change of induction and therefore it will send a voltage to the sensing circuit. As already mentioned, the drop in residual induction represents a negative change if the residual induction is positive (Fig. 2b) and a positive change if the residual induction is negative (Fig. 2c). The polarity of the voltage induced in the read/write winding will tell the sensing circuit in which residual state the core is resting, and therefore, whether it contains a ONE or a ZERO.

A hollow toroid (Fig. 3a) is one possible geometrical arrangement for using this system. The read/write winding occupies the same position as it does on presently used toroids while the  $90^\circ$ -field winding lies circumferentially inside the hollow. When the  $90^\circ$ -field winding is pulsed, the residual induction vectors on the inside circumference of the toroid are deflected in a direction opposite to that in which the residual induction vectors on the outside circumference of the toroid are deflected. Similarly, the vectors on the top and bottom of the toroid are deflected in opposite directions. The net effect is a drop in the magnitude of the component of the residual induction around the toroid as the vectors are twisted (Fig. 3b). If the toroid is sliced length-wise, as shown, to facilitate putting in the  $90^\circ$ -field winding, the air gap thus introduced does not affect the rectangularity of the main hysteresis loop; it merely dilutes the  $90^\circ$  field.

The maximum value of the  $90^\circ$  field is that value not quite large enough to pull the magnetization vector up to a hard direction of magnetization. The maximum change in residual induction is seen to be (Fig. 4):

$$\begin{aligned} dB_{\max} &< B_s (1 - \cos 45^\circ) \\ &< .293 B_s \end{aligned}$$

It is interesting to note that when using a material having a rectangular hysteresis loop, this system is a unidirectional transformer. A signal inserted in the  $90^\circ$ -field winding will appear across the read/write winding but a signal fed into the read/write winding will not appear across the  $90^\circ$ -field winding. The  $90^\circ$ -field circuit will not load the core during writing; nor will writing transients feed back into the  $90^\circ$ -field circuit.

Finally, the sensing operation does not involve the destruction and formation of domain boundary walls. Therefore, there is no hysteresis

loss associated with this system; the  $90^\circ$  field does not have to supply any energy in the form of hysteresis loss because switching of the material does not take place. For this reason the scheme promises to make possible a non-destructive read system which is fast.

Signed Dudley A. Buck  
Dudley A. Buck

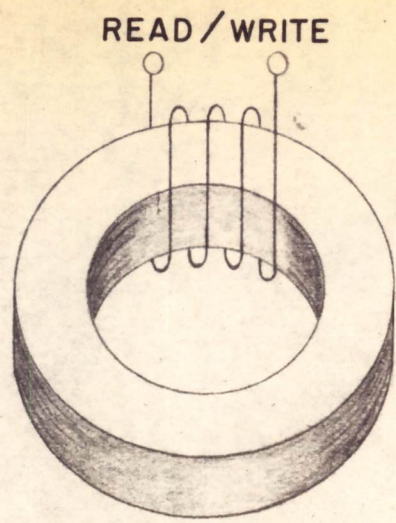
Approved William N. Papian  
William N. Papian

DAB/jk

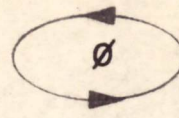
Drawings attached:

- A-51080 Fig. 1
- A-51081 Fig. 2
- A-51082 Fig. 3
- A-51083 Fig. 4

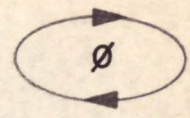




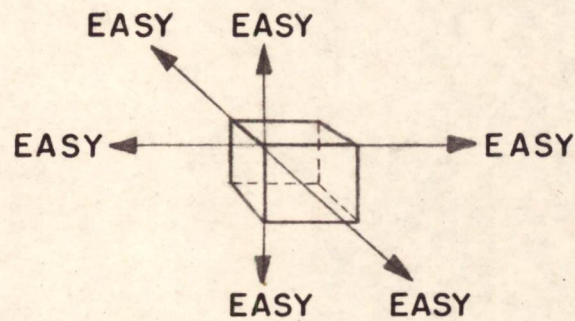
(A)



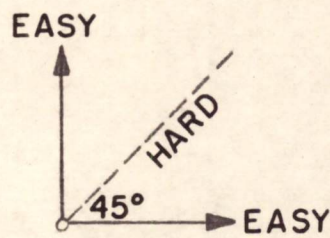
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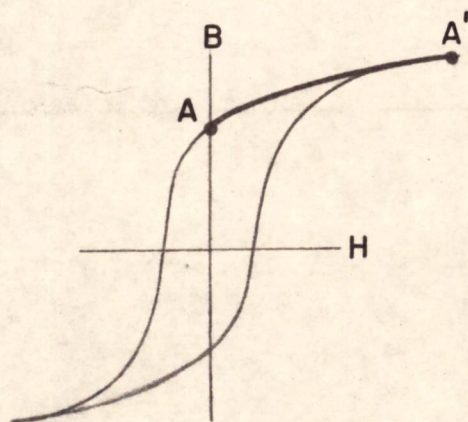
"0"



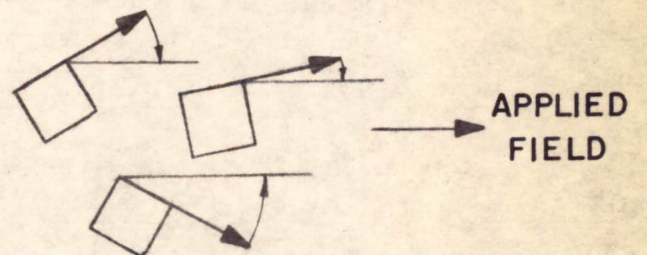
(B)



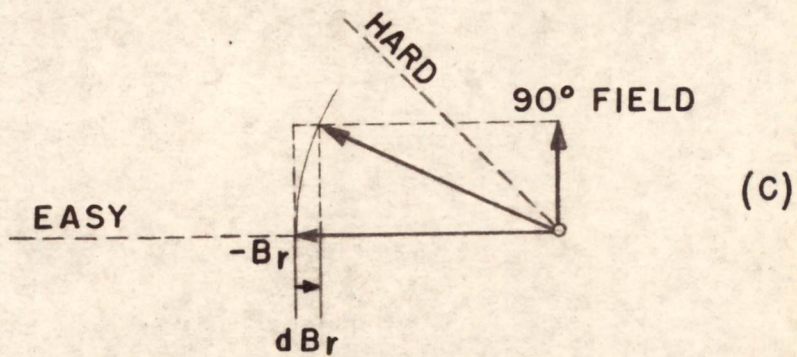
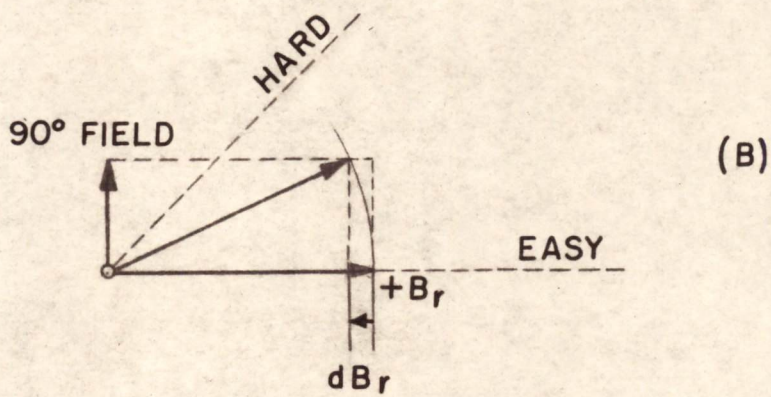
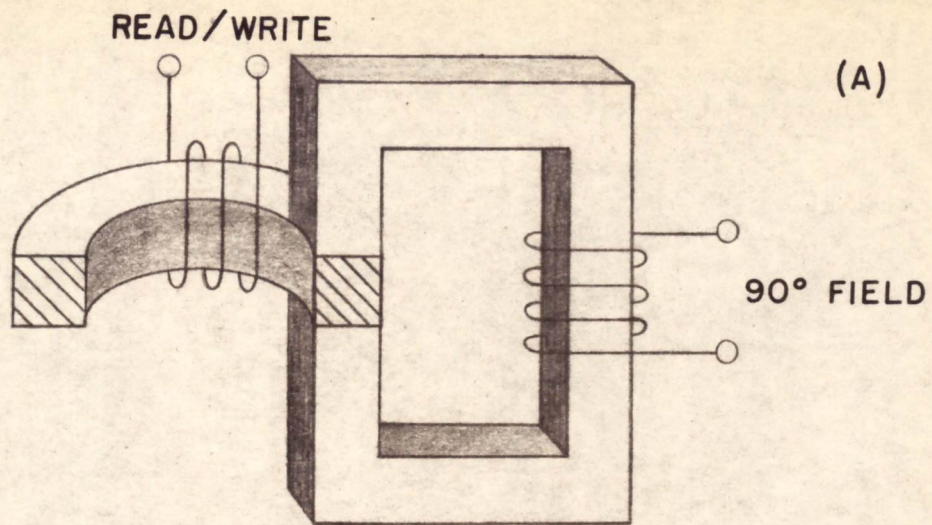
(C)



(D)

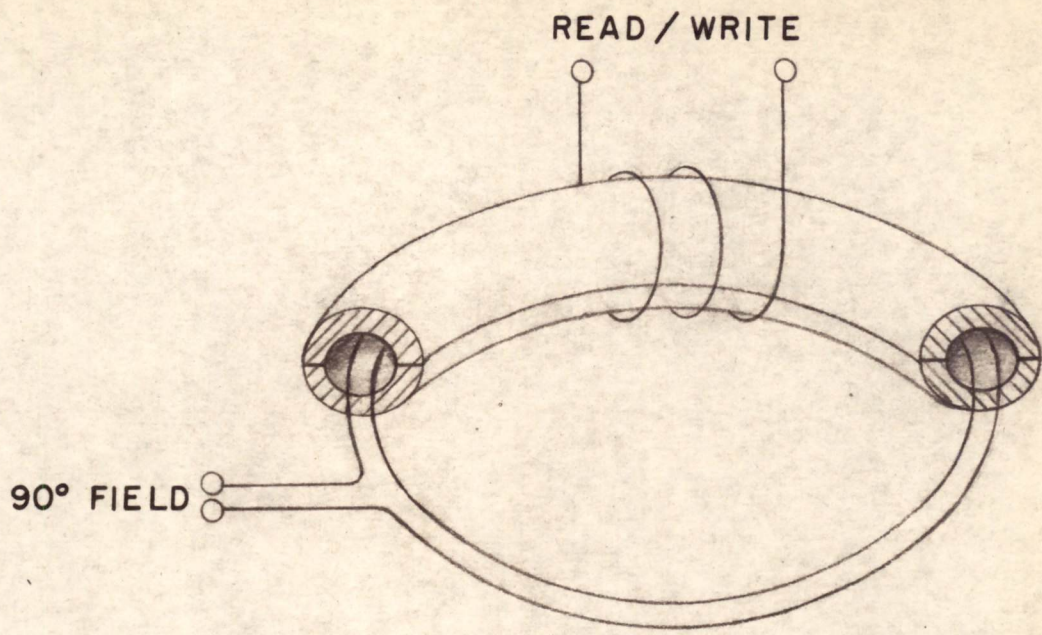


NON-DESTRUCTIVE READ  
(DOMAIN MAGNETIZATION VECTORS)

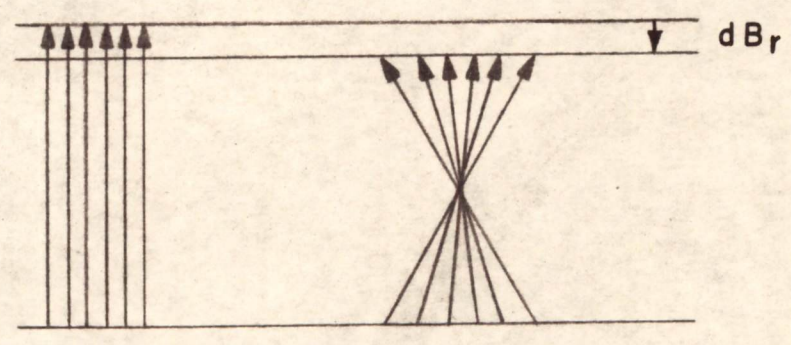


NON-DESTRUCTIVE READ  
(90° FIELD WINDING)

FIG. 2

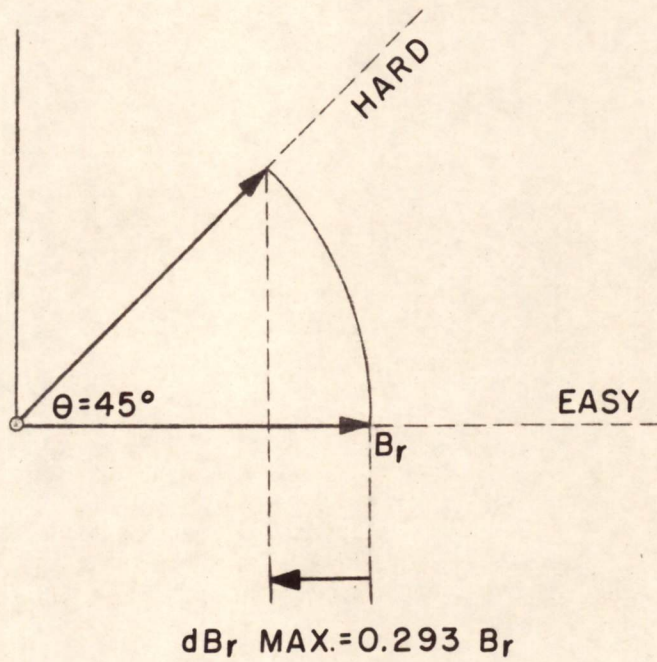


(A)



(B)

NON-DESTRUCTIVE READ  
(HOLLOW TOROID)



NON-DESTRUCTIVE READ  
(ANALYSIS)

Digital Computer Laboratory  
Massachusetts Institute of Technology  
Cambridge, Massachusetts

SUBJECT: THE USE OF BOOLEAN ALGEBRA IN LOGICAL DESIGN

To: N. H. Taylor

From: R. C. Jeffrey, I. S. Reed

Date: April 15, 1952 (Revised April 28, 1952)

Abstract: This note is a practical description of Boolean algebra and its application to the analysis and synthesis of digital computers. It is argued that knowledge of the theory and methods described here is equivalent in value to considerable experience and ingenuity in the logical design of computers, and that it provides a way of bringing a novice in the field up to the point where he can make contributions considerably more quickly than this is done at present.

## 1.0 INTRODUCTION

To a first approximation we can describe a binary computer as a set of 2 state memory devices functionally connected by an information processing network. This first approximation to any particular computer represents its logical design; if it has been well engineered and well constructed, the approximation will be useful: for example, we may then ignore the fact that the voltages at critical points in the machine may assume any one of a continuous range of values.

It is customary to represent the logical structure of a machine by block diagrams. Unfortunately, you cannot calculate with block diagrams: they are merely expository devices. Everyone will agree that it would be helpful to be able to represent machines by sets of equations for which we know simple rules of transformation. Much would then become routine which now requires more or less experience and ingenuity, leading the designer more quickly to the important decisions.

There exists a system of mathematics within which such calculation is possible. Its mechanical rules are simpler than those of ordinary algebra, as will be seen in the next section. With a very little practice at it, a novice in the field of digital computers can solve, with understanding, a large class of non-trivial problems. For example, the following problem is solved later in the text.

Design a three bit "counter" with the following "loops":

FF1	FF2	FF3	
1	1	0	
0	1	1	
1	1	0	(alternates between 110 and 011)
0	0	0	
0	1	0	(passes from 000 into its
1	0	0	cycle, but 000 is not
0	0	1	included in the cycle)
0	1	0	
1	1	1	
1	0	1	
1	0	1	(sticks on 101)

Such devices might be used as operation counters.

We do not by any means suggest that facility at Boolean algebra will supercede experience and ingenuity in the logical design of computers. Rather

(1) the algebra provides a way of efficiently channeling the experience and ingenuity of the novice: a unified theory accelerates and deepens learning.

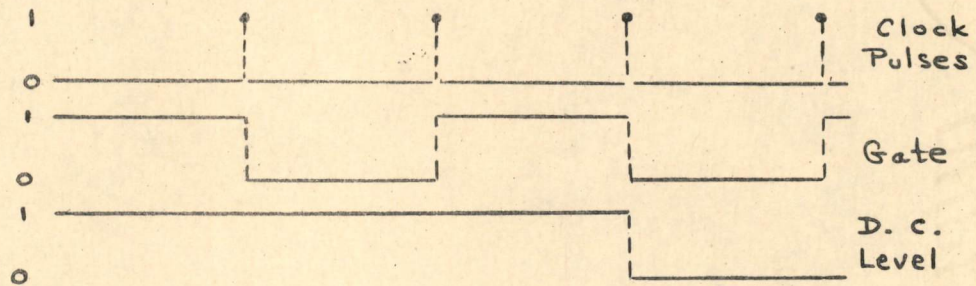
(2) it allows the practicing designer immediate access to the important, non-routine problems: they allow him to use his skill where it counts.

## 2.0 BOOLEAN ALGEBRA

Boolean algebra is most often developed as an abstract mathematical system, the interpretation being left open. Here, however, we parallel each step in the exposition of the theory with its counterpart in terms of the familiar block diagrams in the hope of promoting a sense of confidence and familiarity with the new technique.

The voltage (or current or whatever physical magnitude represents information) at any logically important point in a machine may be represented to a first approximation as a function of time which, for every value of  $t$ , is either 0 or 1. Any change in such a function will then be a jump discontinuity.

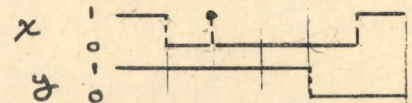
Examples



The elements of our algebra are such Boolean functions of time.

We define four operations on such functions: ways of compounding from  $x(t)$  and  $y(t)$  new Boolean functions. For conciseness we shall omit the time variable in the following table, in which, for example, " $\bar{x}$ " is an abbreviation for " $x'(t)$ ", and " $x + y$ " abbreviates " $x(t) + y(t)$ ".

Under "Graph" we show the output waveform when the inputs,  $x(t)$  and  $y(t)$ , are:



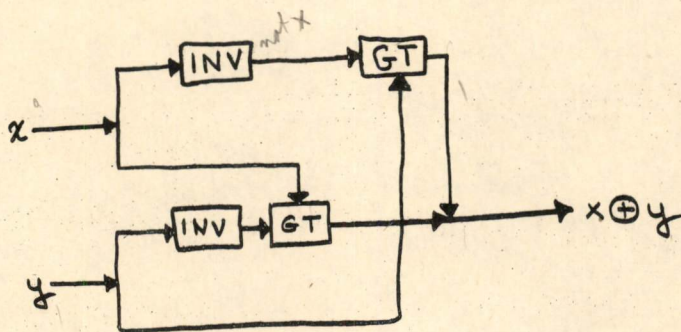
Name	Table	One Physical Realization	Block Diagram	Graph
Not; - Complement	$x \quad x'$ 0 1 1 0		$x \rightarrow \text{INV} \rightarrow x'$	
And; Logical Product	$x \quad y \quad xy$ 0 0 0 0 1 0 1 0 0 1 1 1		$x \rightarrow \text{GT} \rightarrow xy$ or $x \cdot y$	
Or; Logical Sum	$x \quad y \quad x+y$ 0 0 0 0 1 1 1 0 1 1 1 1		$x \rightarrow \text{OR} \rightarrow x+y$	
Partial Sum; Cyclic Sum; Symmetric Difference	$x \quad y \quad x \oplus y$ 0 0 0 0 1 1 1 0 1 1 1 0	See P. 4	Proposal: $x \oplus y$	

DIF. FROM  
BINARY  
ADDITION

Since there are a finite number of different ways of assigning 0 and 1 as values to  $n$  variables, it will always be possible to completely describe any Boolean function by a table as we have done for the four above.

For  $n$  inputs there are  $2^{2^n}$  Boolean functions, any one of which might be realized electronically in some simple way. The algebra is neutral on this issue: new physical realizations of functions which previously had to be built up out of others have algebraic representations waiting for them and can be integrated, without changing the algebra, into the data of the design problem.

To proceed with the formalism: there are  $2^n$  ways of assigning one of the two values, 0, 1, to each of  $n$  variables. Then it is practical to check any presumed theorem of our algebra by substituting (in tabular form) each possible combination of values for the variables on each side of the equation. Thus we can prove that the cyclic sum,  $\oplus$ , is represented by this combination of gates, mixers and inverters:



$$x \oplus y = (x \cdot y') + (x' \cdot y)$$

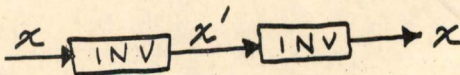
0 0 0	0 0 1	0	1	0	0
0 1 1	0 0 0	1	1	1	1
1 1 0	1 1 1	1	0	0	0
1 0 1	1 0 0	0	0	0	1

↑  
by definition

identical for all  $x, y$

Note that once the 4 pairs of values of  $x, y$  are listed, the values of  $x'$  and  $y'$  are determined, and from these,  $x \cdot y'$ ,  $x' \cdot y$  and  $x y' + x' y$ .

By the same tabular method each of the following theorems of the algebra can be proved. Again, for conciseness, we have omitted time variables.

Law of Double Negation:  $(x')' = x$ . 

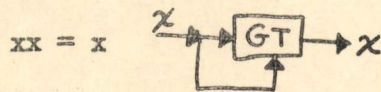
Dual Theorems (The result of interchanging '0' and '1', '+' and '.' in an expression is the complement of that expression. The result of that interchange in a theorem is another theorem.)



For Products

For Sums

No Powers

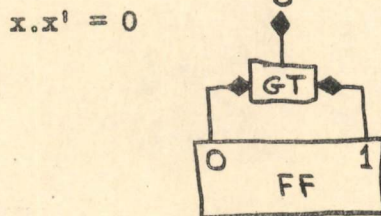
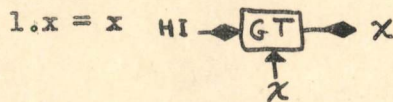
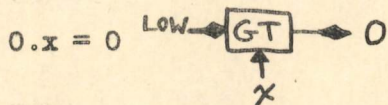


No Numerical Coefficients:

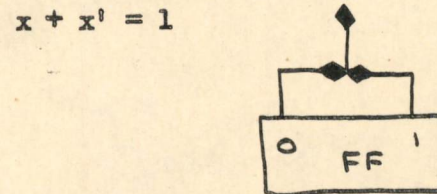
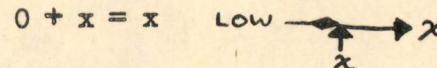
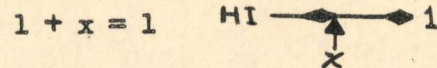
$x + x = x$



Multiply by a constant as in arithmetic:



Addition of a constant:



Associative and Commutative Laws: Ignore grouping and order

in pure products:

$x(yz) = (xy)z = xyz$

$xy = yx$

in pure sums:

$x + (y + z) = (x + y) + z = x + y + z$

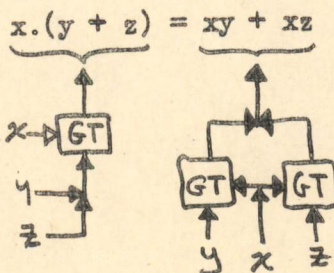
$x + y = y + x$

De Morgan's Theorem:  $(x + y)' = x'y'$

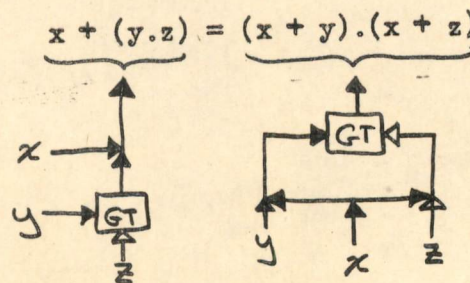
$(xy)' = x' + y'$

Distributive Laws

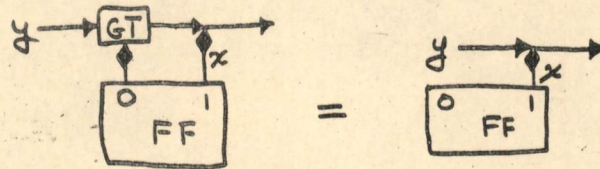
"Multiply through" and factor as in arithmetic:



Unlike arithmetic: you may also "add through" a product:



A very handy simplification:  $x + x'y = x + y$



Theorems of more purely theoretical interest:

Expansion of 'I'

I is the sum of all  $2^n$  possible products of  $n$  variables and their primes.

$$\begin{aligned}
 I &= x + x' \\
 &= xy + x'y + xy' + x'y' \\
 &= xyz + x'yz + xy'z + x'y'z + xyz' + x'yz' + xy'z' + x'y'z' \\
 &= xyzw + \dots (14 \text{ terms}) \dots + x'y'z'w' \\
 &=
 \end{aligned}$$

Each function of  $n$  variables can be represented by dropping some of the terms of the above sum:

$$\begin{aligned}
 f(x) &= f(1)x + f(0)x' \\
 f(x,y) &= f(1,1)xy + f(0,1)x'y + f(1,0)xy' + f(0,0)x'y' \\
 f(x,y,z) &= f(1,1,1)xyz + \dots + f(0,1,0)x'yz' + \dots + f(0,0,0)x'y'z' \\
 &\text{etc.}
 \end{aligned}$$

Note the relation between zeros in the argument places and primes on the corresponding variables.

This last theorem is of special importance since it allows us to write an algebraic expression for a function directly from its table:

x	y	f(x,y)
1	1	1
0	1	0
1	0	1
0	0	1

The table is an abbreviation of 4 statements:

$$\begin{aligned}
 f(1,1) &= 1 \\
 f(0,1) &= 0 \\
 f(1,0) &= 1 \\
 f(0,0) &= 1
 \end{aligned}$$

$$\begin{aligned}
 \therefore f(x,y) &= f(1,1)xy + f(0,1)x'y + f(1,0)xy' + f(0,0)x'y' \\
 &= 1 \cdot xy + 0 \cdot x'y + 1 \cdot xy' + 1 \cdot x'y' \\
 &= xy + 0 + xy' + x'y' \\
 &= xy + xy' + x'y'
 \end{aligned}$$

A further example:

x	y	z	$g(x,y,z)$
1	1	1	0
0	1	1	0
1	0	1	1
0	0	1	0
1	1	0	1
0	1	0	0
1	0	0	0
0	0	0	1

$$g(x,y,z) = xy'z + xyz' + x'y'z'$$

As an exercise, note that in the first example,  $f(x,y)$  can be further simplified to  $x + y'$ . (Factor, and use the theorems:  $a + a' = 1$ ;  $1 \cdot a = a$ ;  $a + a'b = a + b$ )

### 3.0 APPLICATION TO PASSIVE NETWORKS

We may now illustrate the technique of reducing networks which do not contain memory elements. It is assumed that all pulses occur at the same time, so the time variable will be dropped.

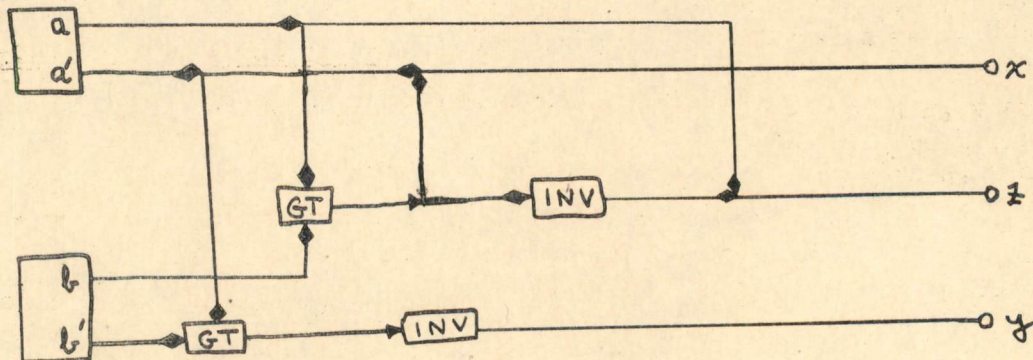
#### Example of translation of equations into block diagram

$$x = ab + a' = a' + b$$

$$y = (a'b')' = (a + b)$$

$$z = a + (ab)' = 1$$

Here regard  $a$  and  $b$  as inputs,  $x$ ,  $y$  and  $z$  as outputs and assume that  $a$  and  $b$  are obtained from FF's so that both  $a$ ,  $b$  and  $a'$  and  $b'$  are available.



Simplification: This design contains redundancies in the sense that fewer gates and inverters may be used to get the same outputs for each input:

Since  $x + x'y = x + y$

$x = a' + b$

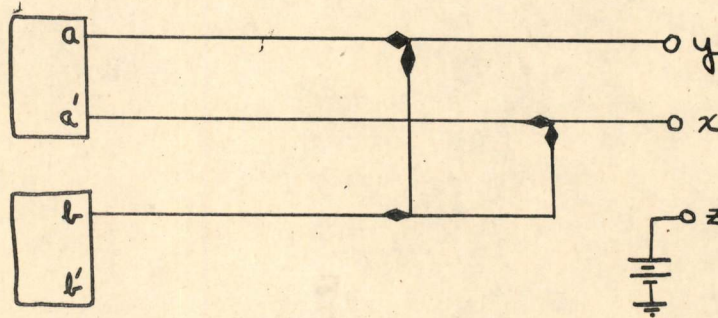
By De Morgan's theorem

$y = a + b$

$z = a + a' + b' = 1 + b' = 1$

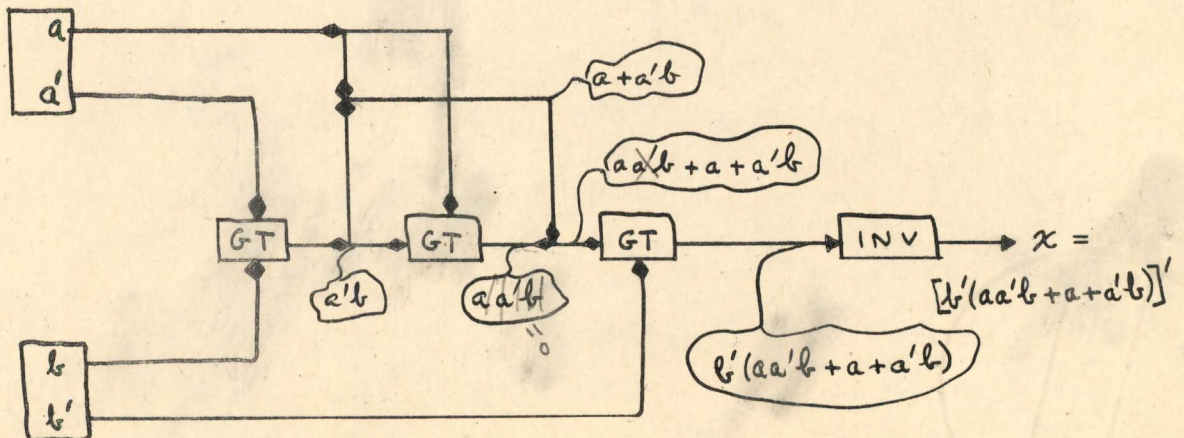
Thus z is simply a point which is permanently at, say, high voltage.

This gives as a simpler equivalent block design



Example of translation of block diagram into symbols:

We may analyze the circuit following and simplify it by first translating it into equations:



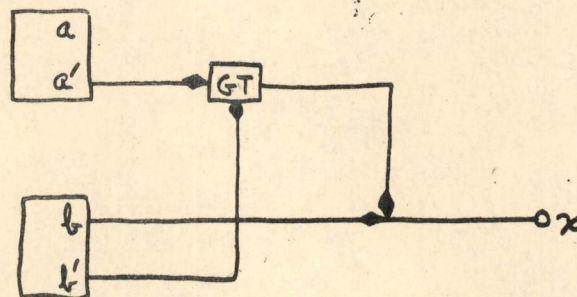
Now we simplify:  $aa' = 0$  and  $0.b = 0$ . Then the  $aa'b$  term vanishes.

$a + a'b = a + b$ . Hence  $x = [b'(a + b)]'$ . By De Morgan's theorem,

$x = b + (a + b)'$  and by another application

$$x = b + a'b' = b + a'$$

Simplified block diagram:



A further simplification, which will eliminate the gate, is left as an exercise.

Translation of tables into equations

It is desired to construct a circuit with the properties given by the table:

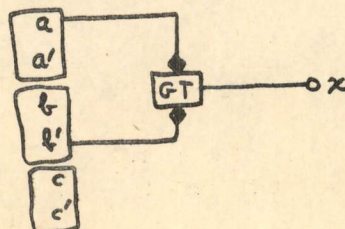
a	b	c	x
1	1	1	0
0	1	1	0
1	0	1	1
0	0	1	0
1	1	0	0
0	1	0	0
1	0	0	1
0	0	0	0

which tells, for each possible triad of input values, the desired output.

We find the desired  $x = f(a,b,c)$  as a sum of the products associated with the 1's in the table.

$$x = ab^1c + ab^1c^1 = ab^1(c + c^1) = ab^1(1) = ab^1$$

Then  $c$  is superfluous:



The devices indicated above have their analogies in the methods of Aiken and Shannon. However, the treatment of flip-flops in the next section is new, and represents a radical advance over other methods.

#### 4.0 THE FLIP-FLOP EQUATIONS

At this point it becomes necessary to explicitly indicate the dependence on time of the variables in our discussion. Expressions like 'A(t)' represent voltage (or current or whatever physical quantity is used as the realization of our 0 and 1) at particular points in the machine at time t. If 'A(t)' is such an expression, 'A(t + T)' will be the voltage (or whatever) at the same point in the machine T seconds later.

For definiteness, let us assume we are dealing with a clocked machine, i.e., a machine in which any changes in state of the FF's must occur at discrete times, the times at which the clock pulses occur. Call the period of the clock T.

We shall analyze, under the name 'flip-flop' an Eccles-Jordan multivibrator with 2 inputs, a clear and a set, with a cross-over circuit such that when both inputs are 'on' simultaneously, triggering action occurs and the FF is complemented. This is somewhat different (superficially) from the WWI sort of FF which is provided with 3 inputs, no 2 of which may be 'on' at once. However, the transformation to the WW variety is simple, once the equation for the present type is established.

We know that the state of the FF after the inputs have been pulsed depends only on (1) which input has been pulsed (has value 1) and (2) the state of the FF at the time the input was pulsed:  $A(t+T) = f \begin{bmatrix} a(t) \\ a(t) \end{bmatrix}, A(t)$

For example, if neither input is pulsed, i.e., if  $a(t) = a(t) = 0$ , then the FF state doesn't change:  $A(t + T) = A(t)$ . If only the clear side is pulsed  $\begin{bmatrix} a(t) = 1 \\ a(t) = 0 \end{bmatrix}$  the state of the FF goes to 0 regardless of what it was before:  $A(t + T) = 0$ . And if the FF is complemented by pulsing both inputs ( $a(t) = a(t) = 1$ ) then  $A(t + T) = A'(t)$ . These characteristics of the FF may be summarized by the following table.

A(t + T)	$\begin{bmatrix} a(t) \\ a(t) \end{bmatrix}$	a(t)	A(t)	Explanation
0	$\begin{bmatrix} 1 \\ 1 \end{bmatrix}$	1	1	Complement
1	$\begin{bmatrix} 0 \\ 1 \end{bmatrix}$	1	1	Set
0	$\begin{bmatrix} 1 \\ 0 \end{bmatrix}$	0	1	Clear
1	$\begin{bmatrix} 0 \\ 0 \end{bmatrix}$	0	1	No change
1	$\begin{bmatrix} 1 \\ 1 \end{bmatrix}$	1	0	Complement
1	$\begin{bmatrix} 0 \\ 1 \end{bmatrix}$	1	0	Set
0	$\begin{bmatrix} 1 \\ 0 \end{bmatrix}$	0	0	Clear
0	$\begin{bmatrix} 0 \\ 0 \end{bmatrix}$	0	0	No change

This table determines  $A(t + T)$  as a function of the inputs and the state at time  $t$ . To get an equation for the FF we represent the table in the form

$$A(t + T) = f \left[ \begin{matrix} a(t), a(t), A(t) \end{matrix} \right] = f(1,1,1) a(t)a(t)A(t) + \dots + f(0,0,0) a'(t)a'(t)A'(t),$$

that is, as a sum of those products which correspond to the '1's under " $A(t + T)$ ".

$$A(t + T) = a'(t)a(t)A(t) + a'(t)a'(t)A(t) + a(t)a(t)A'(t) + a'(t)a(t)A'(t)$$

Factoring " $a'(t)A(t)$ " from the 1st 2 terms and " $a(t)A'(t)$ " from the 2nd 2 terms:

$$A(t + T) = a'(t)A(t) \left[ a(t) + a'(t) \right] + a(t)A'(t) \left[ a(t) + a'(t) \right]$$

and since  $x + x' = I$  and  $x.I = x$

$$A(t + T) = a'(t)A(t) + a(t)A'(t)$$

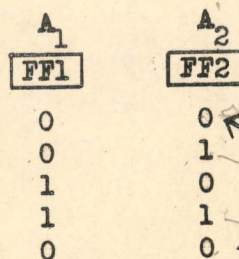
This is the flip-flop equation, which describes the action of a FF the way  $x(t) \oplus y(t) = x(t)y'(t) + x'(t)y(t)$  describes the action of a partial sum circuit. Here, however, we deal essentially with a difference in time (it is this fact which made the analysis of the FF come later than that of "instantaneous" networks in Boolean algebra).

Now the problem of designing a circuit using flip-flops is simply that of connecting the proper network onto the two inputs. That is, if we know  $a(t)$  and  $a'(t)$  as functions of the ultimate inputs to the circuit we can draw block diagrams for the inputs to the flip-flops and hence have the circuit.

Illustrations of Circuit Design via Flip-Flop Equations

2 Stage Binary Counter

(This example is chosen because the result is familiar. In the next example we illustrate the use of this method in analyzing a more difficult problem.) We wish the counter to be cyclic, i.e., the successive states of the flip-flop are as shown. The flip-flop will progress from each state to the next after a count command ( $P(t)$ ).



Apparently we need to clear FF1 in only one case: when  $A_1$  and  $A_2$  are both 1 and there is a count pulse.

$$\text{Thus } a_1(t) = A_1(t)A_2(t)P(t)$$

In other cases where  $A_1 = 0$  the previous state was also 0, so no pulse is required to maintain the state. Note that we are designing in terms of the changes in state of the flip-flops, and not in terms of the states themselves.

We must set  $A_1$ , when  $A_1 = 0$ ,  $A_2 = 1$  and there is a count pulse:

$$a_1(t) = A_1'(t)A_2(t)P(t)$$

Similarly for  $A_2$ :

$$\text{Clear: } a_2(t) = A_1'(t)A_2(t)P(t) + A_1(t)A_2(t)P(t)$$

i.e., we wish to clear  $A_2$  when either of these two conditions exist:

$$A_1 = 0, A_2 = 1, \text{ pulse}$$

$$A_1 = 1, A_2 = 1, \text{ pulse}$$

Now we can factor:  $A_1'(t)A_2(t)P(t) + A_1(t)A_2(t)P(t)$

$$= [A_1'(t) + A_1(t)] A_2(t)P(t) = [1] A_2(t)P(t)$$

$$\therefore a_2(t) = A_2(t)P(t)$$

Thus we wish to clear  $A_2$  on the next pulse whenever it holds a 1, a fact which might have been read directly from the table (regardless of what is in the left hand column, the successor of any '1' under ' $A_2$ ' is a 0).

Finally, to set  $A_2$ :

$$\begin{aligned} a_2(t) &= [A_1'(t)A_2'(t) + A_1(t)A_2'(t)] P(t) \\ &= [A_1'(t) + A_1(t)] A_2'(t)P(t) \\ &= A_2'(t)P(t) \end{aligned}$$

which means that  $A_2$  is to be cleared on the next pulse whenever it holds a '0' regardless of what  $A_1$  holds. This also might have been seen from the table.



We now have, for the equations for the changes to the grids of the flip-flop, the following (abbreviated by dropping the 't'):

$$o a_1 = A_1 A_2 P$$

$$a_1 = A_1' A_2 P$$

$$o a_2 = A_2 P$$

$$a_2 = A_2' P$$

These may be reduced by replacing 'A<sub>2</sub>P' in the first equation by 'o a<sub>2</sub>' (from the third) and ditto in the second:

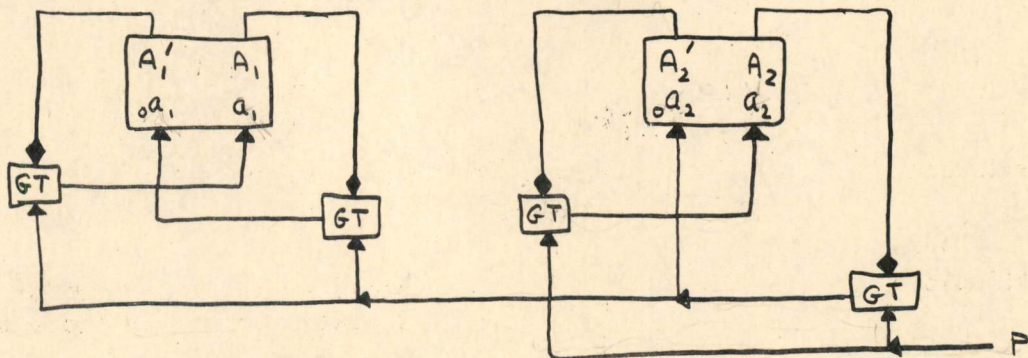
$$o a_1 = A_1 o a_2$$

$$a_1 = A_1' o a_2$$

$$o a_2 = A_2 P$$

$$a_2 = A_2' P$$

Thus we have eliminated several gates. The block diagram is unfamiliar because of the use of two-input flip-flops.



Using only the trigger inputs of flip-flops results in a simpler circuit:

Here  $o a = a = c a$ . The flip-flop equation becomes

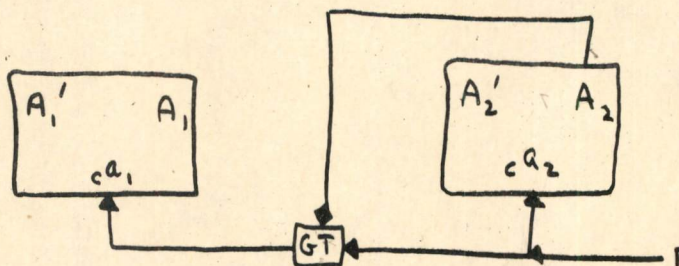
$$A(t + T) = c a(t) A'(t) + c a'(t) A(t) = c a(t) \oplus A(t)$$

Returning to the table,  $A_1$  should be complemented whenever  $A_2 = 1$ :

$$c^{a_1} = A_2 P$$

and for  $A_2$ :  $c^{a_2} = P$  (complemented on every pulse)

The Block Diagram



Note that the delay necessary so that  $A_2$  will change after  $P$  has tried to pass the gate is assumed to exist in the FF. This was implicit in our original FF equation.

We now indicate, without much comment, the solution of the less familiar problem proposed in the introduction. We shall use only the complement input to the flip-flops (except for reading in numbers, a simple process which we won't include in the problem). The "counter" changes state when it receives a command pulse,  $P(t)$ .

$A_1$	$A_2$	$A_3$
1	1	0
0	1	1
1	1	0
0	0	0
0	1	0
1	0	0
0	0	1
0	1	0
1	1	1
1	0	1
1	0	1

(stick)

$$A(T) = c^a \oplus A$$

(abbreviated form of the full equation:

$$A(t + T) = c^a(t) \oplus A(t))$$

We are concerned only with the changes in the states of the flip-flops.

For  $A_1$ : 
$$c_{a_1} = (\underline{A_1 A_2 A_3'} + A_1' A_2 A_3 + A_1' A_2' A_3' + \underline{A_1 A_2' A_3'}) P$$

$$= \boxed{A_1 A_3' (A_2 + A_2') + A_1' A_2 (A_3 + A_3')} P$$

$$c_{a_1} = \boxed{(A_1 A_3' + A_1' A_2)} P$$

For  $A_2$ : 
$$c_{a_2} = (\underline{A_1' A_2' A_3'} + A_1' A_2 A_3 + \underline{A_1' A_2' A_3} + A_1 A_2 A_3) P$$

$$= \boxed{A_1' A_2' (A_3' + A_3) + A_2 (A_1' A_3' + A_1 A_3')} P$$

$$c_{a_2} = \boxed{A_1' A_2' + A_2 (A_1' A_3' + A_1 A_3')} P$$

For  $A_3$ : 
$$c_{a_3} = (\underline{A_1 A_2 A_3'} + A_1' A_2 A_3 + A_1 A_2' A_3' + \underline{A_1' A_2' A_3}) P$$

$$= \boxed{A_1 A_3' (A_2 + A_2') + A_1' A_3 (A_2 + A_2')} P$$

$$c_{a_3} = \boxed{A_1 A_3' + A_1' A_3} P$$

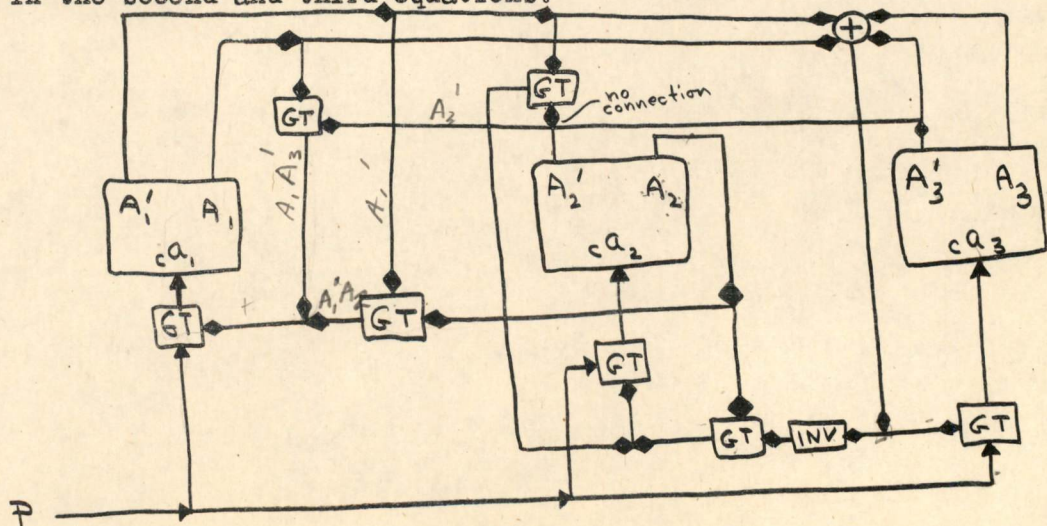
In order to simplify the block diagram for this counter, let us assume that we have available a "package" realization of  $x \oplus y$ .

$c_{a_1} = (A_1 A_3' + A_1' A_2) P$  as before

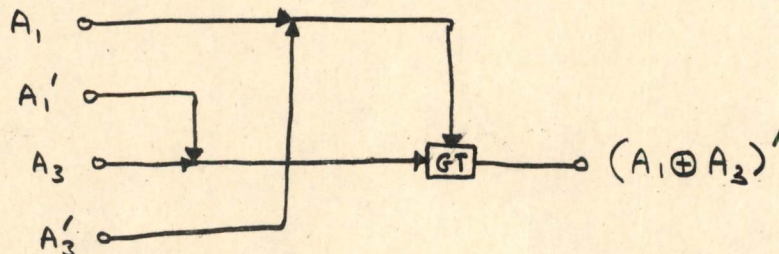
$c_{a_2} = \boxed{A_1' A_2' + A_2 (A_1 \oplus A_3)'} P$

$c_{a_3} = (A_1 \oplus A_3) P$

We may now (assuming that inverters are cheap) use the same circuit for  $A_1 \oplus A_3$  in the second and third equations.



In case inverters are more expensive than gates, we might synthesize  $(A_1 \oplus A_2)'$  directly



[Note that this is the dual of the circuit for  $\oplus$ : we interchanged gates(.) and mixers (+)].

As a final example of the use of the algebra in synthesizing circuits we shall design an adder.

Let  $A_i$  and  $B_i$  be the digits to be added in stage #i, and let the carry into this stage be  $C_i$ . Then the carry out will be  $C_{i+1}$  and the well known table governs the action of the stage:

$A_i(t)$	$B_i(t)$	$C_i(t)$	$C_{i+1}(t)$	$A_i(t+T)$
1	1	1	1	1
0	1	1	1	0
1	0	1	1	0
0	0	1	0	1
1	1	0	1	0
0	1	0	0	1
1	0	0	0	1
0	0	0	0	0

Note that we require the carry to be instantaneous: there is to be no cumulative delay from stage to stage. Also note that the sum is to be stored in  $A_i$ . This time our table does not represent the successive states of a counter! We are interested in successive states of  $A_i$ . These are indicated row by row by looking first at column one and then at the parallel entry in the last column. Use complementable FF: (we wish to complement in cases 3, 4, 5, 6). Note that these are just the cases in which  $B_i(t) = C_i'(t)$ , i.e.,  $B_i(t) \oplus C_i(t) = 1$

$$c_{a_i}(t) = \overline{B_i(t)} \oplus C_i(t) \quad P(t)$$

We have introduced the add command:  $P(t)$ .

Now we need to know how to get  $C_{i+1}(t)$  as a function of the three parameters on the left. Apparently

$$C_{i+1} = (A_i B_i C_i + A_i' B_i C_i + A_i B_i' C_i + A_i B_i C_i') P$$

which can be factored:

$$C_{i+1} = \overline{B_i C_i + (B_i \oplus C_i) A_i} P$$

or in unabbreviated form:

$$C_{i+1}(t) = \overline{B_i(t) C_i(t) + (B_i(t) \oplus C_i(t)) A_i(t)} P(t)$$

Note that because of the delay presumed inherent in the flip-flop  $C_{i+1}$  will depend on the original  $A(t)$ , before complementing.

Further reduction: Since  $B_i(t) \oplus C_i(t)$  appears in both equations:

$$c_{a_i}(t) = \overline{B_i(t) \oplus C_i(t)} P(t)$$

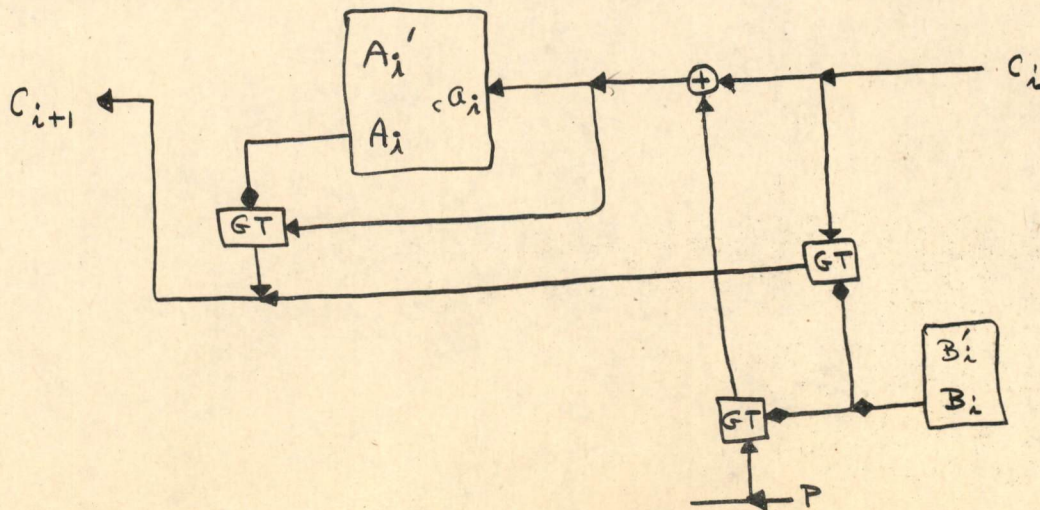
$$C_{i+1}(t) = B_i(t) C_i(t) P(t) + c_{a_i}(t) A_i(t)$$

Now  $C_i(t)$  is a result of gating various inputs from previous stages with the command pulse,  $P(t)$ . Therefore, we need not multiply it again by  $P(t)$ :

$$c_{a_i}(t) = B_i(t) P(t) \oplus C_i(t)$$

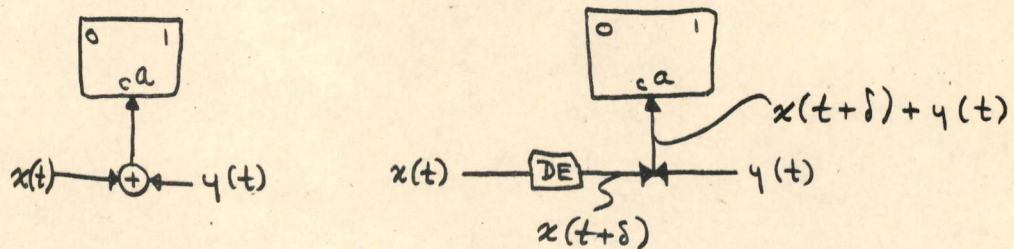
$$C_{i+1}(t) = B_i(t) C_i(t) + c_{a_i}(t) A_i(t)$$

Block Diagram



5.0 DELAY ELEMENTS

To illustrate our method of treating delay elements, consider the following device for realizing  $x \oplus y$  on the trigger input to a flip-flop.



It has already been noted that the realization of  $\oplus$  with ordinary electronic components requires two gates, two inverters (unless the complements of the inputs are also available) and a mixer; it is advantageous to trade for all this a delay element and a single mixer. The action of the second circuit is simple: if  $x$  and  $y$  both occur, the flip-flop is complemented twice, resulting in no change, whereas if one but not the other occurs it is complemented only once.

We can easily derive the equivalence of the two circuits in our formalism, but we have as yet no mechanical way of determining where it would be judicious to introduce delays. In this respect our treatment of delays parallels that of flip-flops: the introduction of both flip-flops and delays is a problem of planning. The design problem takes those elements as data together with their operation cycle, and asks for the most economical connecting network which meets the "boundary conditions". (The analogy between flip-flops and delay elements has as its theoretical basis the fact that any delay element can be represented as a flip-flop gated with a clock of appropriate frequency and phase.)

6.0 OTHER PROBLEMS AND APPLICATIONSMagnetic Devices

Ceramic and ferromagnetic cores act as memory devices in such a way that there is generally no continuous signal output indicating that the core holds a '0' or a '1'. It has already been proposed that such devices be interpreted as flip-flops with built-in gates.

The main apparent difficulty in applying this algebra to magnetic devices is that from a 2 state core, three outputs are possible: a pulse of "+" polarity, a pulse of "-" polarity and no pulse. We wish, if possible,

to avoid going over to a three-valued algebra for the analysis of these devices, first because of the complexity of such a formalism, and second because the cores are themselves devices which have only two states of magnetization in current applications.

It would be easy enough to resort to some such device as lumping together two of the three outputs from a core for the purposes of analysis; but it remains to be seen whether such a device will result in a theory which ignores important logical possibilities in circuits using magnetic cores. For further remarks, see Appendix III.

### Probability in the Boolean Machine

When a computer is interpreted as a physical realization of a set of Boolean equations it becomes possible to apply probability theory in such a way that we obtain information about the density of information in critical registers. The application to input-output problems (buffer storage, etc.) is apparent. (See articles by Reed in Bibliography.)

### Combinatorial Problems; Planning vs. Design

We have shown a method whereby, given the desired cycle, a logically optimum counter may be designed (relative to existing "packaged" realizations of logical functions). But this theory sheds no direct light on the problem: what is the most desirable cycle for a given application? Rather, we have suggested that the theory, in reducing the actual design to a routine process, leads the designer more quickly to that crucial question.  $N$  flip-flops are capable of  $2^N$  different configurations, and there are  $2^{2^N}$  different "counting" cycles which might be obtained. The optimum electronic realizations of these are not all of the same complexity; and often, in a particular application (say where arbitrary meanings are assigned to the various stages of the count) any one of a number of these cycles would be equally useful. The problem is then not: "What, for the given cycle, is the optimal realization?", but rather, "Comparing a number of usable cycles and their optimal realizations, which of these is optimum?" (which of a number of relative minima is least?)

We might call such decisions combinatorial rather than logical. The algebra, as developed here, provides no complete solutions to such problems. However, it appears that the problem may be soluble by further analysis. (One possibility is this: formulate a set of fully mechanical rules for deciding between two circuits on grounds of relative complexity in terms of available components; then program a computer to work out all optimal designs (relative minima) and decide between them as to the absolute minimum.)

In general, the broader questions of computer planning are illuminated but not solved by the present theory. It is entirely possible that further theoretical development, incorporating combinatory, statistical and information-theoretic elements with the present theory may lead to a mathematical treatment of the broader questions concerning the organization of computing machinery.

The present theory gives something like the following general picture of digital computers. Any particular analog computer may be regarded as a physical realization or analyzer of a set of differential equations. Similarly we may regard any digital computer, general purpose or otherwise, as a physical realization or analyzer of a set of Boolean difference equations.

The equations analyzed by a machine may be studied in a perfectly abstract way (this has not been done here) just as the machine may be studied as a physical entity. Then two points of view are possible:

- (1) The Boolean difference equations describe the working of the machine.
- (2) The machine realizes or analyzes the equations.

It is the validity of the second point of view which motivates the building of any machine.

#### History of this Theory and Relation to Other Theories

The English mathematician, George Boole, presented, in 1847, the first workable but cumbersome predecessor of the present sort of formalism. He was interested in its interpretation as an algebra of logic and of probability, and it was the application to logic which inspired the investigations of his successors, W. S. Jevons, C. S. Peirce, E. Schroeder and others in increasing the power and simplicity of the algebra.

One logical interpretation of the present algebra is this: let the variables (dropping the time arguments altogether) represent sentences such as " $3 > 2$ ", " $3 > 5$ " and "Water boils at  $100^{\circ}\text{C}$ ." The two values 0 and 1 are interpreted respectively as falsity and truth, so that  $3 > 2 = 1$  but  $3 > 5 = 0$ . " $x'$ " is the sentence which is true when " $x$ " is false, and vice versa: (the contradictory of " $x$ ") "it is not the case that  $x$ " or briefly "not  $x$ ". Therefore,  $(3 > 5)' = 1$ . " $x.y$ " is the sentence " $x$  and  $y$ ", which is true only when both  $x$  and  $y$  are true:  $(3 > 5).(3 > 2) = 0$ .  $x + y$  is  $x$  and/or  $y$  (briefly:  $x$  or  $y$ ), which is true if  $x$  is true or  $y$  is true or both are true:  $(3 > 5) + (3 > 2) = 1$ . Similar interpretations may be found for the other Boolean functions, and it will be seen that, on this interpretation, the theorems of the system are those laws of logic which apply to propositions and their combinations.

When we drop the assumption that the variables may have only the two values 0 and 1 there results a formalism which has as one of its interpretations a logic of classes containing the classical theory of syllogisms.

It was, as far as we know, Claude Shannon who, in 1938, first published an interpretation under which the algebra becomes a theory of relay and switching circuits. Shannon's interpretation led the way to an



application of the algebra to static information-processing networks of all kinds, including those used in present-day electronic digital computers. However, Shannon's theory took no account of the dependence on time of the states of a computer. Therefore, while it led to an analysis of networks of gates, mixers, inverters and the rest, it did not permit an analysis of flip-flops. That theory was no substantial help in designing counters, adders and so on.

After Shannon, the principal development of algebraic methods in this field came from Burkhart, Kalin and Aiken of the Harvard Computation Laboratory. In the form in which it was published in 1951, their algebra (which shared with Shannon's a lack of adequate means for representing time variables) was an arithmetic of 0 and 1.

<u>Boolean Algebra</u>	<u>Aiken's Formulation</u>
( + and . have the meanings used in this text)	( + and . have their ordinary arithmetical meanings)
$x'$	$1 - x$
$xy$	$xy$
$x + y$	$x + y - xy$

Superficially, the Aiken algebra is easier to use than Boolean algebra, since it is merely ordinary arithmetic restricted to 0 and 1. However, for every new law which one must learn in order to use Boolean algebra, one must learn an arithmetical trick to use the Aiken algebra. Consider, for example, the transformation which in Boolean algebra is accomplished by De Morgan's theorem:

$$(xy)' = x' + y'$$

In Aiken's algebra it becomes necessary to delicately introduce 1's and parentheses in order to go from  $1 - xy$  (our " $(xy)'$ ") to  $(1-x) + (1-y) - (1-x)(1-y)$  (our " $x' + y'$ "). Then Aiken's arithmetic is at least as hard to handle as Boolean algebra. Furthermore, it has the disadvantage that while an entire expression such as ' $x + y - xy$ ' (our ' $x + y$ ') is always either 0 or 1, yet such expressions often contain parts which are neither 0 nor 1, and hence meaningless. Thus if  $x = y = 1$ ,  $x + y - xy = 1$ , but part of it,  $x + y$ , is 2, which is meaningless in the interpretation. We have examined this matter here in some detail in order to justify our use of a simple but unfamiliar formalism rather than a familiar but unexpectedly complicated one.

The present theory, with its use of time variables throughout, is the work of Irving S. Reed. To our knowledge it is the first analysis of computing machines powerful enough to provide a general method for synthesizing flip-flop circuits such as accumulators by straightforward calculation. Furthermore, by designing not in terms of the sequence of states of the flip-flops, but rather in terms of the changes in their states, we are led directly to a minimal design, without the use of such cumbersome devices as "minimization charts".

It should be stressed that the present report is an account of the most direct and easily used practical outcomes of the theory. For a rigorous mathematical account of the theory the reader is referred to the papers by Reed in the Bibliography. The introduction of time variables makes possible an extension of Boolean algebra into analysis. The theoretical background of the results presented here is an analogue of the calculus and theory of ordinary differential equations, based, not on ordinary arithmetic, but rather on Boolean algebra.

These methods were used, in a restricted form, in the design of the MADDIDA and CADAC computers, beginning in the winter of 1947. One of the results of the theoretical studies has been that the present method is applicable to pulse circuits in general, and not only to computers using a special sort of clock waveform.

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Appendix I, Page 23  
Appendix II, Page 27  
Appendix III, Page 29

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APPENDIX ISummary

x	y	$x'$	$x + y$	$xy$	$x \oplus y$	$x \downarrow y$	$x y$
1	1	0	1	1	0	0	0
0	1	1	1	0	1	0	1
1	0	0	1	0	1	0	1
0	0	1	0	0	0	1	1

There are  $2^{2^n}$  distinct functions of  $n$  variables, some of which are repetitions of functions of  $n - 1, n - 2, \dots, 1, 0$  variables. E.g.,  $x'$  appears above as a function of two variables (its value is defined for all 4 values of  $x, y$ ; but since it is actually definable in terms of  $x$  alone, it is really a function of 1 variable). The two functions of 0 variables are 0 and 1.

There are an infinite number of functions in terms of which all functions can be defined. The two such functions of 2 variables are  $\downarrow$  and  $|$ . For example:

$$x|x = x'$$

$$(x|y)|(x|y) = xy$$

It follows that all other functions are definable in terms of  $|$ , since all functions are definable in terms of not and and:

$$x + y = (x'y')'$$

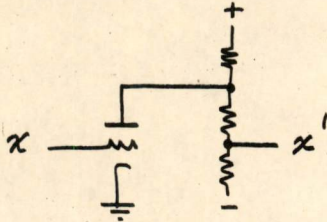
$$x \oplus y = xy' + x'y$$

etc.

Physical Realizations of Functions:

(The list is not complete) (In the magnetic circuits current in the indicated directions represents 1; no current represents 0; diodes might be necessary to prevent back flow and for clamping.)

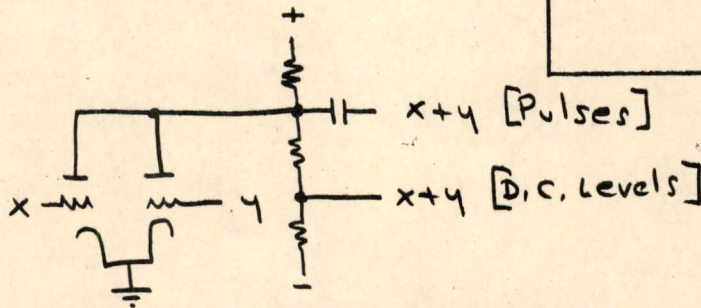
Complement



(Bias and voltage dividing network are such that when the grid goes positive, the  $x'$  point goes down to zero.)

Sum

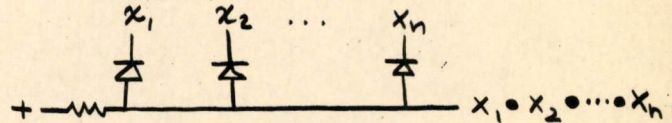
all circuits may be used with  $n$  inputs; shown here with  $n=2$ .



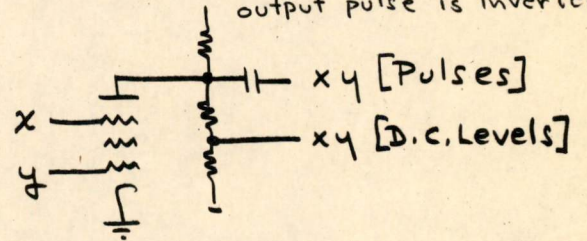
Provides Amplification; output pulse is inverted.

Product

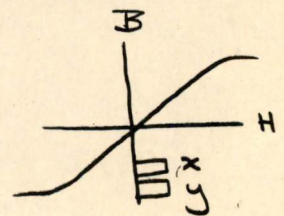
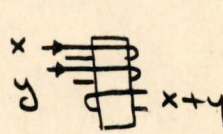
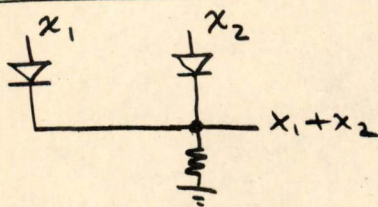
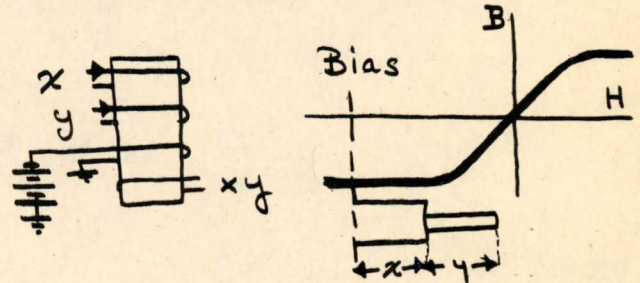
For  $n$  inputs:



For 2 inputs; gives amplification; output pulse is inverted.

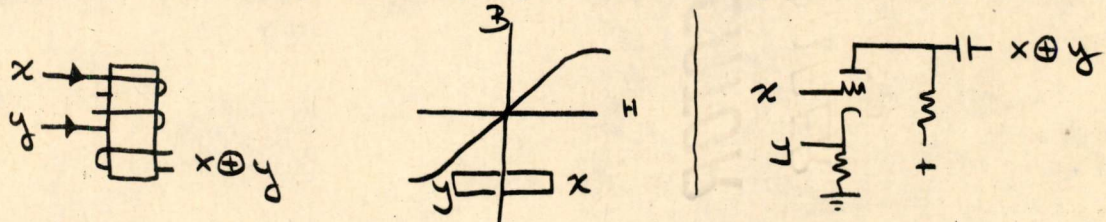


For  $n$  inputs (shown with  $n=2$ ):



Partial Sum

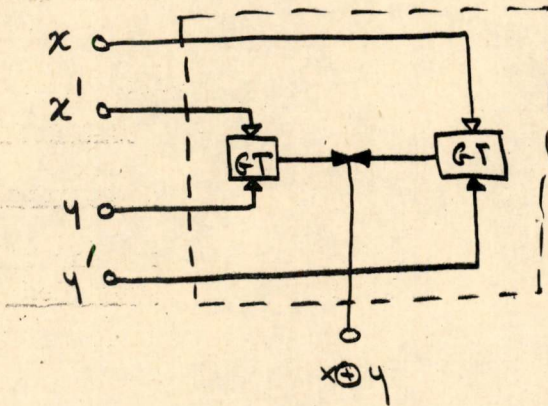
If you can ignore the polarity of the output and depend on the coincidence in time, duration, amplitude and shape of  $x$  and  $y$  -----



Otherwise

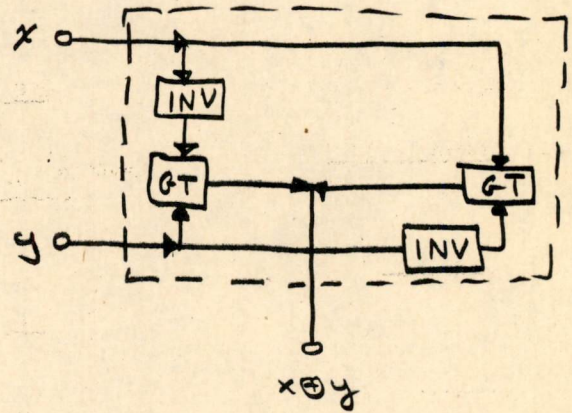
Black Box #1

(If the variables and also their primes are available.)



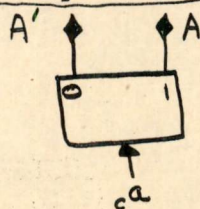
Black Box #2

(If the variables, but not their primes, are available.)

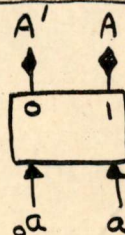


It follows from the statements on the previous page that, given realizations of not and and, black box realizations of all other functions can be constructed. And given realizations of or, all needed black boxes can be constructed.

Flip-Flops



$$A(t + \epsilon) = {}_c a(t) \oplus A(t)$$



Triggers when both inputs are pulsed at once.

$$A(t + \epsilon) = a(t)A'(t) \oplus {}_o a'(t)A(t)$$

(Reduces to the first case when  $a = {}_o a$ )

Magnetic  
Memory Core

${}_0a(t)$	$a(t)$	$A(t)$	$A(t + \epsilon)$	$d_+(A)$	$d_-(A)$	$R(t)$
1	1	1	1	0	0	0
0	1	1	1	0	0	0
1	0	1	0	0	1	1
0	0	1	1	0	0	0
1	1	0	0	0	0	0
0	1	0	1	1	0	0
1	0	0	0	0	0	0
0	0	0	0	0	0	0

currents as shown  
represent 1. No  
current represents 0.

Value of A:  $\uparrow = 1, \downarrow = 0$

$$R = d_-(A)$$

$$A(t + \epsilon) = [{}_0a'(t) + a(t)] A(t) + [{}_0a'(t) \cdot a(t)] A'(t)$$

$$R(t) = {}_0a(t)a'(t)A(t)$$

This can be set and cleared; read out by clearing (if the core held a 1 there will be a pulse out). However: it won't trigger as shown, and the readout is a single pulse, rather than a D.C. level.

DUPLICATOR  
 COPY PAPER

APPENDIX IISome Theorems of Boolean Algebra

Ignore order and grouping in pure sums and pure products.

"Multiply through" and factor as in ordinary algebra, and : "add through" a product.

$$a(b + c) = ab + ac$$

$$a + (b.c) = (a + b).(a + c)$$

$$0 + x = x \quad 0.x = 0 \quad x + x = x \quad x + x' = 1$$

$$1 + x = 1 \quad 1.x = X \quad x . x = X \quad x . x' = 0$$

Expansion of a Function

$$\begin{aligned} f(x,y,z) &= f(0,0,0)x'y'z' + f(1,0,0)xy'z' + \dots + f(1,1,1)xyz \\ &= [f(0,0,0) + xty+z] [f(1,0,0) + x'ty+z] \dots [f(1,1,1) + x'ty'+z'] \end{aligned}$$

In particular, for the constant function  $f(x,y,z) = 1$  for all  $x,y,z$ , we get

$$1 = x'y'z' + xy'z' + \dots + xyz \quad (\text{all 8 terms are present})$$

and for the constant  $f(x,y,z) = 0$  we get

$$0 = (xty+z).(x'ty+z).\dots.(x'ty'+z') \quad (\text{all 8 factors are present})$$

De Morgan's Law:  $(xy)' = x' + y'$  ;  $(x+y)' = x'y'$

Elimination of a factor:  $x + x'y = x + y$

Theorems relating to  $\oplus$  :

$$x \oplus (y \oplus z) = (x \oplus y) \oplus z = x \oplus y \oplus z$$

$$x \oplus y = y \oplus x$$

$$x \oplus y = xy' + x'y$$

$$x \mp y = x \oplus \bar{y} \oplus xy$$

$$(x \oplus y)' = x' \oplus y = x \oplus y'$$

$(x \oplus y)'$  is an interesting function: it is 1 exactly when x and y have the same value.

$$x(y \oplus z) = xy \oplus xz$$

If  $x \oplus y = z$ ,  $x' = y \oplus z$  (Permits solution of equations)

$$x \oplus 1 = x'$$

$$x \oplus 0 = x$$

$$x \oplus x = 0$$

For a more complete list of theorems, see works of Couturat and Whitehead listed in Bibliography.

Any expression can be put in the form:

$$Ax + Bx'$$

e.g., the equation for the FF with 2 inputs is in that form.

To complement such an expression it is sufficient to complement the "coefficients":

$$(Ax + Bx')' = A'x + B'x'$$



APPENDIX III

Core Analysis with 3 Valued Logic

$\circ a(t)$	$a(t)$	$A(t)$	$A(t + \epsilon)$	$R(t)$
-1	-1	-1	-1	0
0	-1	-1	-1	0
1	-1	-1	-1	0
-1	0	-1	1	1
0	0	-1	-1	0
1	0	-1	-1	0
-1	1	-1	1	1
0	1	-1	1	1
1	1	-1	-1	0
-1	-1	0	0	0
0	-1	0	-1	-1
1	-1	0	-1	-1
-1	0	0	1	1
0	0	0	0	0
1	0	0	-1	-1
-1	1	0	1	1
0	1	0	1	1
1	1	0	0	0
-1	-1	1	1	0
0	-1	1	-1	-1
1	-1	1	-1	-1
-1	0	1	1	0
0	0	1	1	0
1	0	1	-1	-1
-1	1	1	1	0
0	1	1	1	0
1	1	1	1	0

$a(t) = +1$  has same effect

as  $\circ a(t) = +1$

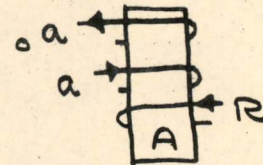
R is wound so that when the state of the core is moving toward 1,  $R = 1$ , i.e.,

$$R(t) = 1 \iff A(t) < A(t + \epsilon)$$

$$R(t) = 0 \iff A(t) = A(t + \epsilon)$$

$$R(t) = -1 \iff A(t) > A(t + \epsilon)$$

" $\iff$ " means if and only if



State of the core:

$-1 = \downarrow$ ;  $+1 = \uparrow$ ;  $0 =$  no magnetization.

Currents in the windings are positive as shown by arrows. Opposite current:  $-1$ . No I:  $0$ .

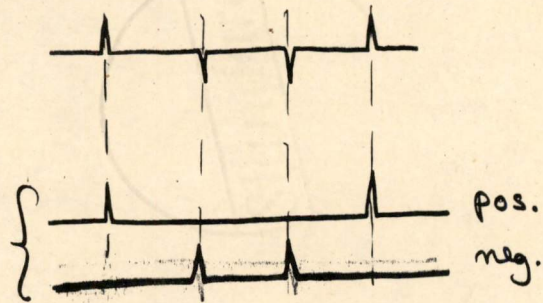
The rules of 3 valued algebra are more cumbersome than those of the present theory.

Note that cores require a 3 valued analysis only to the same extent that vacuum tube circuits do. In vacuum tube circuits, too, there are three possible inputs and outputs: positive, negative and zero pulses. In trying to account for such circuits in terms of 0 and 1 alone, we are somewhat farther from reality than when we use -1, 0 and 1. But the three valued analysis is itself a high-order abstraction from the real situation with its continuum of infinitely many values.

The point is that we pay for the additional simplicity of each higher order of abstraction in faithfulness of the resulting black-and-white picture of the real situation.

We believe that a 3 valued analysis would be of use, but the use would be a better evaluation of the limitations of the two valued approach. There may exist combinations of elements whose utility depends on the polarities of the pulses involved. Such designs could be "cranked out" of a 3 valued analysis. But it may be that, having recognized them, they can be introduced into the two valued analysis by special devices. One such device is translating a single-pulse-train:

into two:



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SUBJECT: THE USE OF BOOLEAN ALGEBRA IN LOGICAL DESIGN

To: N. H. Taylor

From: R. C. Jeffrey, I. S. Reed

Date: April 15, 1952 (Revised April 28, 1952) (Revised October 21, 1952)

Abstract: This note is a practical description of Boolean algebra and its application to the analysis and synthesis of digital computers. It is argued that knowledge of the theory and methods described here is equivalent in value to considerable experience and ingenuity in the logical design of computers, and that it provides a way of bringing a novice in the field up to the point where he can make contributions considerably more quickly than this is done at present.

## 1.0 INTRODUCTION

To a first approximation we can describe a binary computer as a set of 2 state memory devices functionally connected by an information processing network. This first approximation to any particular computer represents its logical design; if it has been well engineered and well constructed, the approximation will be useful: for example, we may then ignore the fact that the voltages at critical points in the machine may assume any one of a continuous range of values.

It is customary to represent the logical structure of a machine by block diagrams. Unfortunately, you cannot calculate with block diagrams: they are merely expository devices. Everyone will agree that it would be helpful to be able to represent machines by sets of equations for which we know simple rules of transformation. Much would then become routine which now requires more or less experience and ingenuity, leading the designer more quickly to the important decisions.

There exists a system of mathematics within which such calculation is possible. Its mechanical rules are simpler than those of ordinary algebra, as will be seen in the next section. With a very little practice at it, a novice in the field of digital computers can solve, with understanding, a large class of non-trivial problems. For example, the following problem is solved later in the text.

Design a three bit "counter" with the following "loops":

FF1	FF2	FF3	
1	1	0	
0	1	1	
1	1	0	(alternates between 110 and 011)
0	0	0	
0	1	0	(passes from 000 into its
1	0	0	cycle, but 000 is not
0	0	1	included in the cycle)
0	1	0	
1	1	1	
1	0	1	
1	0	1	(sticks on 101)

Such devices might be used as operation counters.

We do not by any means suggest that facility at Boolean algebra will supercede experience and ingenuity in the logical design of computers. Rather

(1) the algebra provides a way of efficiently channeling the experience and ingenuity of the novice: a unified theory accelerates and deepens learning.

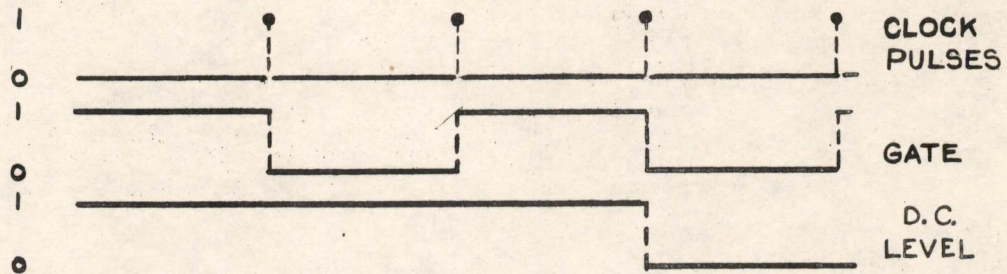
(2) it allows the practicing designer immediate access to the important, non-routine problems: they allow him to use his skill where it counts.

## 2.0 BOOLEAN ALGEBRA

Boolean algebra is most often developed as an abstract mathematical system, the interpretation being left open. Here, however, we parallel each step in the exposition of the theory with its counterpart in terms of the familiar block diagrams in the hope of promoting a sense of confidence and familiarity with the new technique.

The voltage (or current or whatever physical magnitude represents information) at any logically important point in a machine may be represented to a first approximation as a function of time which, for every value of  $t$ , is either 0 or 1. Any change in such a function will then be a jump discontinuity.

Examples



The elements of our algebra are such Boolean functions of time.

We define four operations on such functions: ways of compounding from  $x(t)$  and  $y(t)$  new Boolean functions. For conciseness we shall omit the time variable in the following table, in which, for example, "x" is an abbreviation for " $x(t)$ ", and " $x + y$ " abbreviates " $x(t) + y(t)$ ".

Under "Graph" we show the output waveform when the inputs,  $x(t)$  and  $y(t)$ , are:

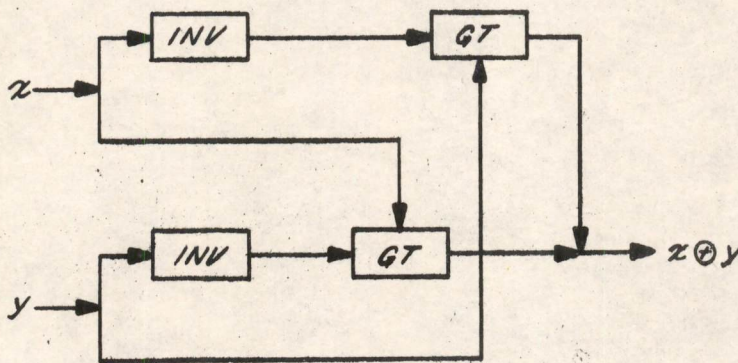


Name	Table	One Physical Realization	Block Diagram	Graph
Not; Complement	$x \quad x'$ 0 1 1 0			
And; Logical Product	$x \quad y \quad xy$ 0 0 0 0 1 0 1 0 0 1 1 1			
Or; Logical Sum	$x \quad y \quad x+y$ 0 0 0 0 1 1 1 0 1 1 1 1			
Partial Sum; Cyclic Sum; Symmetric Difference	$x \quad y \quad x \oplus y$ 0 0 0 0 1 1 1 0 1 1 1 0	See P. 4	Proposal: 	

Since there are a finite number of different ways of assigning 0 and 1 as values to  $n$  variables, it will always be possible to completely describe any Boolean function by a table as we have done for the four above.

For  $n$  inputs there are  $2^{2^n}$  Boolean functions, any one of which might be realized electronically in some simple way. The algebra is neutral on this issue: new physical realizations of functions which previously had to be built up out of others have algebraic representations waiting for them and can be integrated, without changing the algebra, into the data of the design problem.

To proceed with the formalism: there are  $2^n$  ways of assigning one of the two values, 0, 1, to each of  $n$  variables. Then it is practical to check any presumed theorem of our algebra by substituting (in tabular form) each possible combination of values for the variables on each side of the equation. Thus we can prove that the cyclic sum,  $\oplus$ , is represented by this combination of gates, mixers and inverters:



$$x \oplus y = (x \cdot y') + (x' \cdot y)$$

0 0 0	001	0	1	0 0
0 1 1	000	1	1	1 1
1 1 0	111	1	0	0 0 0
1 0 1	100	0	0	0 0 1

↑  
by definition

↑  
identical for all x,y

Note that once the 4 pairs of values of  $x, y$  are listed, the values of  $x'$  and  $y'$  are determined, and from these,  $x \cdot y'$ ,  $x' \cdot y$  and  $x y' + x' y$ .

By the same tabular method each of the following theorems of the algebra can be proved. Again, for conciseness, we have omitted time variables.

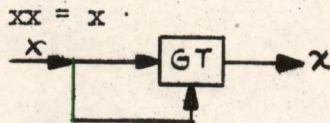
Law of Double Negation:  $(x')' = x$ .

Dual Theorems (The result of interchanging '0' and '1', '+' and '.' in an expression is the complement of that expression. The result of that interchange in a theorem is another theorem.)

For Products

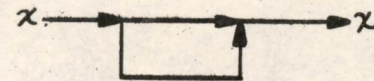
For Sums

No Powers

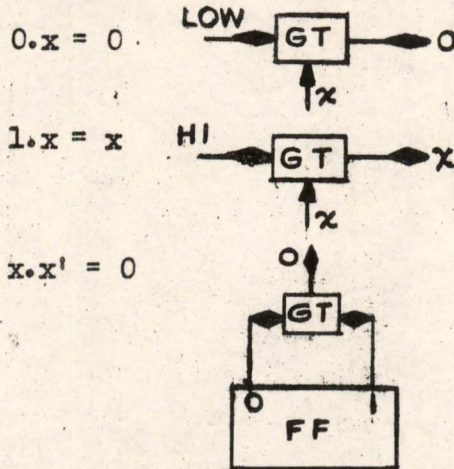


No Numerical

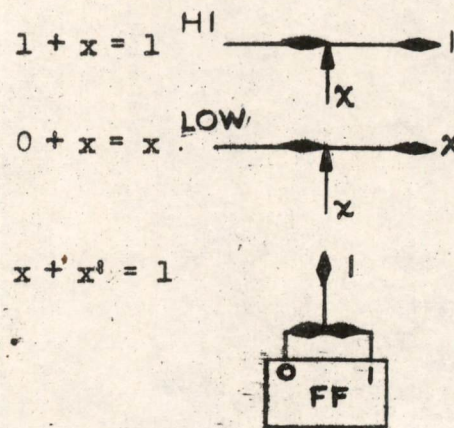
Coefficients:  $x + x = x$



Multiply by a constant as in arithmetic:



Addition of a constant:



Associative and Commutative Laws: Ignore grouping and order

in pure products

$x(yz) = (xy)z = xyz$

$xy = yx$

in pure sums

$x + (y + z) = (x + y) + z = x + y + z$

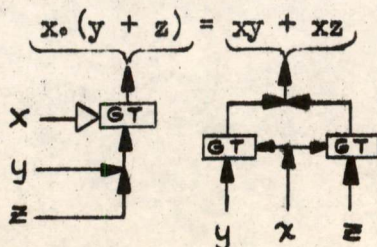
$x + y = y + x$

De Morgan's Theorem:  $(x + y)' = x'y'$

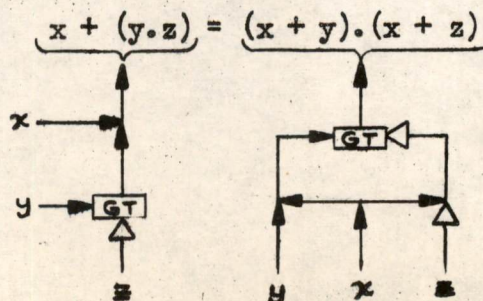
$(xy)' = x' + y'$

Distributive Laws

"Multiply through" and factor as in arithmetic:

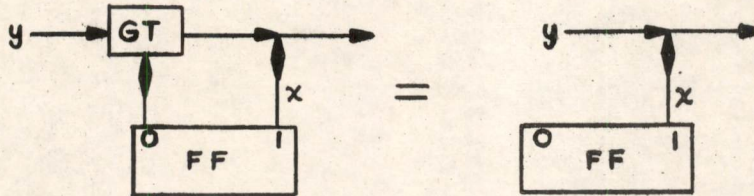


Unlike arithmetic: you may also "add through" a product:





A very handy simplification:  $x + x'y = x + y$



Theorems of more purely theoretical interest:

Expansion of 'I'

I is the sum of all  $2^n$  possible products of  $n$  variables and their primes.

$$\begin{aligned}
 I &= x + x' \\
 &= xy + x'y + xy' + x'y' \\
 &= xyz + x'yz + xy'z + x'y'z + xyz' + x'yz' + xy'z' + x'y'z' \\
 &= xyzw + \dots (14 \text{ terms}) \dots + x'y'z'w' \\
 &= \dots
 \end{aligned}$$

Each function of  $n$  variables can be represented by dropping some of the terms of the above sum:

$$\begin{aligned}
 f(x) &= f(1)x + f(0)x' \\
 f(x,y) &= f(1,1)xy + f(0,1)x'y + f(1,0)xy' + f(0,0)x'y' \\
 f(x,y,z) &= f(1,1,1)xyz + \dots + f(0,1,0)x'yz' + \dots + f(0,0,0)x'y'z' \\
 &\text{etc.}
 \end{aligned}$$

Note the relation between zeros in the argument places and primes on the corresponding variables.

This last theorem is of special importance since it allows us to write an algebraic expression for a function directly from its table:

x	y	f(x,y)
1	1	1
0	1	0
1	0	1
0	0	1

The table is an abbreviation of 4 statements:

$$\begin{aligned}
 f(1,1) &= 1 \\
 f(0,1) &= 0 \\
 f(1,0) &= 1 \\
 f(0,0) &= 1
 \end{aligned}$$

$$\begin{aligned}
 \therefore f(x,y) &= f(1,1)xy + f(0,1)x'y + f(1,0)xy' + f(0,0)x'y' \\
 &= 1 \cdot xy + 0 \cdot x'y + 1 \cdot xy' + 1 \cdot x'y' \\
 &= xy + 0 + xy' + x'y' \\
 &= xy + xy' + x'y'
 \end{aligned}$$

A further example:

x	y	z	$g(x,y,z)$
1	1	1	0
0	1	1	0
1	0	1	1
0	0	1	0
1	1	0	1
0	1	0	0
1	0	0	0
0	0	0	1

$$g(x,y,z) = xy'z + xyz' + x'y'z'$$

As an exercise, note that in the first example,  $f(x,y)$  can be further simplified to  $x + y'$ . (Factor, and use the theorems:  $a + a' = 1$ ;  $1 \cdot a = a$ ;  $a + a'b = a + b$ )

### 3.0 APPLICATION TO PASSIVE NETWORKS

We may now illustrate the technique of reducing networks which do not contain memory elements. It is assumed that all pulses occur at the same time, so the time variable will be dropped.

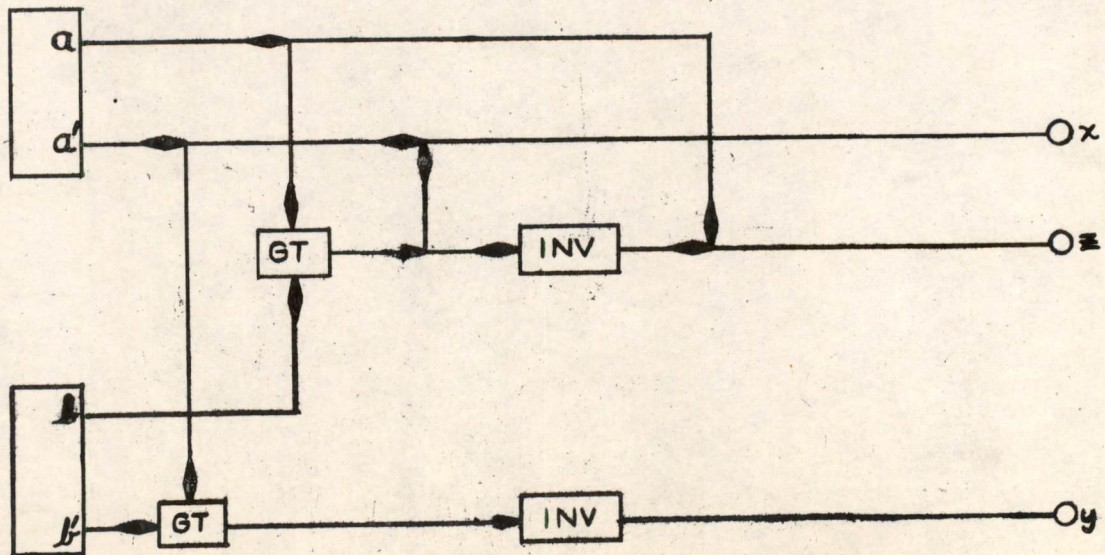
#### Example of translation of equations into block diagram

$$x = ab + a'$$

$$y = (a'b')'$$

$$z = a + (ab)'$$

Here regard  $a$  and  $b$  as inputs,  $x$ ,  $y$  and  $z$  as outputs and assume that  $a$  and  $b$  are obtained from FF's so that both  $a$ ,  $b$  and  $a'$  and  $b'$  are available.



Simplification: This design contains redundancies in the sense that fewer gates and inverters may be used to get the same outputs for each input:

$$\text{Since } x + x'y = x + y$$

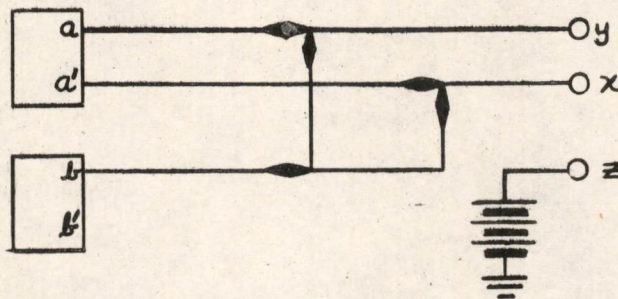
$$x = a' + b$$

By De Morgan's theorem

$$y = a + b'$$

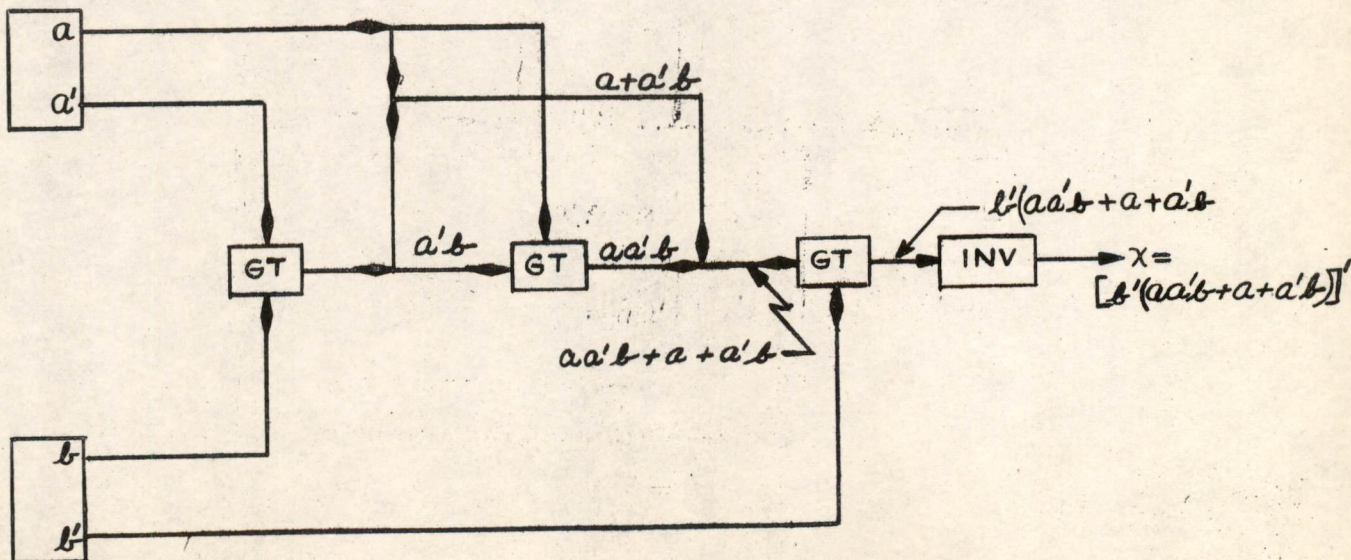
$$z = a + a' + b' = 1 + b' = 1$$

Thus z is simply a point which is permanently at, say, high voltage. This gives as a simpler equivalent block design



Example of translation of block diagram into symbols:

We may analyze the circuit following and simplify it by first translating it into equations:



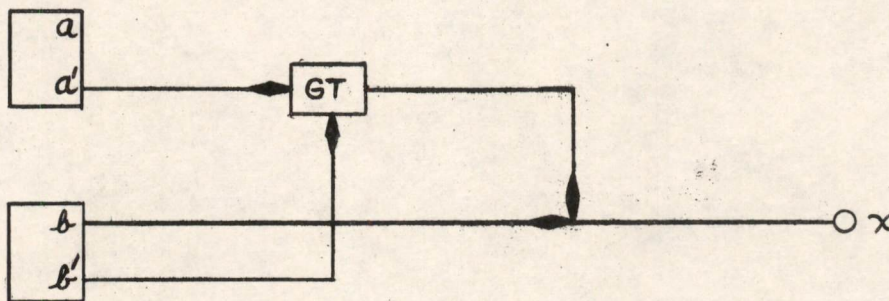
Now we simplify:  $aa' = 0$  and  $0.b = 0$ . Then the  $aa'b$  term vanishes.

$a + a'b = a + b$ . Hence  $x = [b'(a + b)]'$ . By De Morgan's theorem,

$x = b + (a + b)'$  and by another application

$x = b + a'b'$

Simplified block diagram:



A further simplification, which will eliminate the gate, is left as an exercise.

Translation of tables into equations

It is desired to construct a circuit with the properties given by the table:

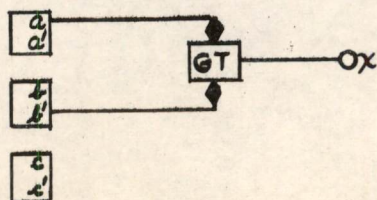
a	b	c	x
1	1	1	0
0	1	1	0
1	0	1	1
0	0	1	0
1	1	0	0
0	1	0	0
1	0	0	1
0	0	0	0

which tells, for each possible triad of input values, the desired output.

We find the desired  $x = f(a,b,c)$  as a sum of the products associated with the 1's in the table.

$$x = ab'c + ab'c' = ab'(c + c') = ab'(1) = ab'$$

Then  $c$  is superfluous:



The devices indicated above have their analogies in the methods of Aiken and Shannon. However, the treatment of flip-flops in the next section is new, and represents a radical advance over other methods.

#### 4.0 THE FLIP-FLOP EQUATIONS

At this point it becomes necessary to explicitly indicate the dependence on time of the variables in our discussion. Expressions like 'A(t)' represent voltage (or current or whatever physical quantity is used as the realization of our 0 and 1) at particular points in the machine at time t. If 'A(t)' is such an expression, 'A(t + T)' will be the voltage (or whatever) at the same point in the machine T seconds later.

For definiteness, let us assume we are dealing with a clocked machine, i.e., a machine in which any changes in state of the FF's must occur at discrete times, the times at which the clock pulses occur. Call the period of the clock T.

We shall analyze, under the name 'flip-flop' an Eccles-Jordan multivibrator with 2 inputs, a clear and a set, with a cross-over circuit such that when both inputs are 'on' simultaneously, triggering action occurs and the FF is complemented. This is somewhat different (superficially) from the WWI sort of FF which is provided with 3 inputs, no 2 of which may be 'on' at once. However, the transformation to the WW variety is simple, once the equation for the present type is established.

We know that the state of the FF after the inputs have been pulsed depends only on (1) which input has been pulsed (has value 1) and (2) the state of the FF at the time the input was pulsed:  $A(t+T) = f \left[ \begin{matrix} \text{clear} \\ \text{set} \end{matrix} a(t), a(t), A(t) \right]$

For example, if neither input is pulsed, i.e., if  $\text{clear}(t) = a(t) = 0$ , then the FF state doesn't change:  $A(t + T) = A(t)$ . If only the clear side is pulsed  $\left[ \begin{matrix} \text{clear} \\ \text{set} \end{matrix} a(t) = 1, a(t) = 0 \right]$  the state of the FF goes to 0 regardless of what it was before:  $A(t + T) = 0$ . And if the FF is complemented by pulsing both inputs ( $\text{clear}(t) = a(t) = 1$ ) then  $A(t + T) = A'(t)$ . These characteristics of the FF may be summarized by the following table.

A(t + T)	$\begin{matrix} \text{clear} \\ \text{set} \end{matrix} a(t)$	a(t)	A(t)	Explanation
0	1	1	1	Complement
1	0	1	1	Set
0	1	0	1	Clear
1	0	0	1	No change
1	1	1	0	Complement
1	0	1	0	Set
0	1	0	0	Clear
0	0	0	0	No change

This table determines  $A(t + T)$  as a function of the inputs and the state at time  $t$ . To get an equation for the FF we represent the table in the form

$$A(t + T) = f \left[ \begin{matrix} a(t), a(t), A(t) \end{matrix} \right] = \\ f(1,1,1) \circ a(t)a(t)A(t) + \dots + f(0,0,0) \circ a'(t)a'(t)A'(t),$$

that is, as a sum of those products which correspond to the '1's under " $A(t + T)$ ".

$$A(t + T) = \circ a'(t)a(t)A(t) + \circ a'(t)a'(t)A(t) + \circ a(t)a(t)A'(t) + \circ a'(t)a(t)A'(t)$$

Factoring " $\circ a'(t)A(t)$ " from the 1st 2 terms and " $a(t)A'(t)$ " from the 2nd 2 terms:

$$A(t + T) = \circ a'(t)A(t) \left[ a(t) + a'(t) \right] + a(t)A'(t) \left[ \circ a(t) + \circ a'(t) \right]$$

and since  $x + x' = I$  and  $x \cdot I = x$

$$A(t + T) = \circ a'(t)A(t) + a(t)A'(t)$$

This is the flip-flop equation, which describes the action of a FF the way  $x(t) \oplus y(t) = x(t)y'(t) + x'(t)y(t)$  describes the action of a partial sum circuit. Here, however, we deal essentially with a difference in time (it is this fact which made the analysis of the FF come later than that of "instantaneous" networks in Boolean algebra).

Now the problem of designing a circuit using flip-flops is simply that of connecting the proper network onto the two inputs. That is, if we know  $\circ a(t)$  and  $a(t)$  as functions of the ultimate inputs to the circuit we can draw block diagrams for the inputs to the flip-flops and hence have the circuit.

### Illustrations of Circuit Design via Flip-Flop Equations

#### 2 Stage Binary Counter

(This example is chosen because the result is familiar. In the next example we illustrate the use of this method in analyzing a more difficult problem.) We wish the counter to be cyclic, i.e., the successive states of the flip-flop are as shown. The flip-flop will progress from each state to the next after a count command ( $P(t)$ ).

$A_1$	$A_2$
<span style="border: 1px solid black; padding: 2px;">FF1</span>	<span style="border: 1px solid black; padding: 2px;">FF2</span>
0	0
0	1
1	0
1	1
0	0

Apparently we need to clear FF1 in only one case: when  $A_1$  and  $A_2$  are both 1 and there is a count pulse.

Thus 
$${}_0a_1(t) = A_1(t)A_2(t)P(t)$$

In other cases where  $A_1 = 0$  the previous state was also 0, so no pulse is required to maintain the state. Note that we are designing in terms of the changes in state of the flip-flops, and not in terms of the states themselves.

We must set A, when  $A_1 = 0$ ,  $A_2 = 1$  and there is a count pulse:

$$a_1(t) = A_1'(t)A_2(t)P(t)$$

Similarly for  $A_2$ :

Clear: 
$${}_0a_2(t) = A_1'(t)A_2(t)P(t) + A_1(t)A_2(t)P(t)$$

i.e., we wish to clear  $A_2$  when either of these two conditions exist:

$$A_1 = 0, A_2 = 1, \text{ pulse}$$

$$A_1 = 1, A_2 = 1, \text{ pulse}$$

Now we can factor: 
$$A_1'(t)A_2(t)P(t) + A_1(t)A_2(t)P(t)$$

$$= [A_1'(t) + A_1(t)] A_2(t)P(t) = [1] A_2(t)P(t)$$

$$\therefore \boxed{{}_0a_2(t) = A_2(t)P(t)}$$

Thus we wish to clear  $A_2$  on the next pulse whenever it holds a 1, a fact which might have been read directly from the table (regardless of what is in the left hand column, the successor of any '1' under ' $A_2$ ' is a 0).

Finally, to set  $A_2$ :

$$a_2(t) = [A_1'(t)A_2'(t) + A_1(t)A_2'(t)] P(t)$$

$$= [A_1'(t) + A_1(t)] A_2'(t)P(t)$$

$$= A_2'(t)P(t)$$

which means that  $A_2$  is to be set on the next pulse whenever it holds a '0' regardless of what  $A_1$  holds. This also might have been seen from the table.

We now have, for the equations for the changes to the grids of the flip-flop, the following (abbreviated by dropping the 't'):

$$o^a_1 = A_1 A_2 P$$

$$a_1 = A_1^1 A_2 P$$

$$o^a_2 = A_2 P$$

$$a_2 = A_2^1 P$$

These may be reduced by replacing 'A<sub>2</sub>P' in the first equation by 'o<sub>2</sub><sup>a</sup>' (from the third) and ditto in the second:

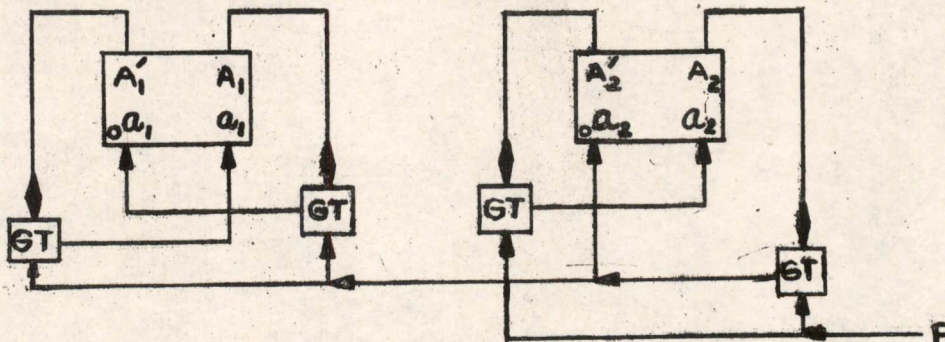
$$o^a_1 = A_1 o^a_2$$

$$a_1 = A_1^1 o^a_2$$

$$o^a_2 = A_2 P$$

$$a_2 = A_2^1 P$$

Thus we have eliminated several gates. The block diagram is unfamiliar because of the use of two-input flip-flops.



Using only the trigger inputs of flip-flops results in a simpler circuit:

Here  $o a = a = o a$ . The flip-flop equation becomes

$$A(t + T) = o a(t)A'(t) + o a'(t)A(t) = o a(t) \oplus A(t)$$

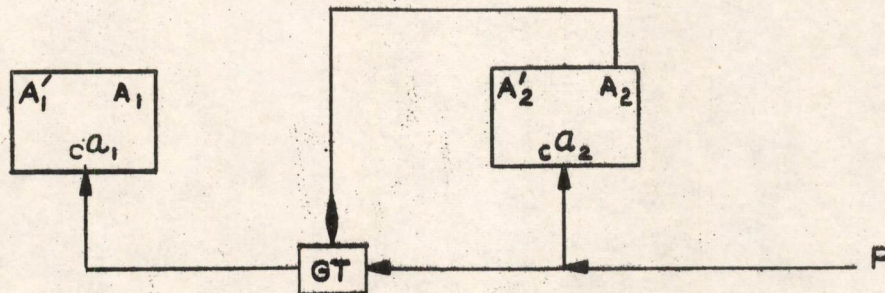


Returning to the table,  $A_1$  should be complemented whenever  $A_2 = 1$ :

$$ca_1 = A_2P$$

and for  $A_2$ :  $ca_2 = P$  (complemented on every pulse)

The Block Diagram



Note that the delay necessary so that  $A_2$  will change after P has tried to pass the gate is assumed to exist in the FF. This was implicit in our original FF equation.

We now indicate, without much comment, the solution of the less familiar problem proposed in the introduction. We shall use only the complement input to the flip-flops (except for reading in numbers, a simple process which we won't include in the problem). The "counter" changes state when it receives a command pulse,  $P(t)$ .

$A_1$	$A_2$	$A_3$
1	1	0
0	1	1
1	1	0
0	0	0
0	1	0
1	0	0
0	0	1
0	1	0
1	1	1
1	0	1
1	0	1

(stick)

$$A(T) = ca \oplus A$$

(abbreviated form of the full equation:

$$A(t + T) = ca(t) \oplus A(t))$$

We are concerned only with the changes in the states of the flip-flops.

For  $A_1$ :  $c^{a_1} = (\underline{A_1 A_2 A_3} + A_1 A_2 A_3 + A_1 A_2 A_3 + \underline{A_1 A_2 A_3})P$   
 $= [A_1 A_3 (A_2 + A_2) + A_1 A_2 (A_3 + A_3)]P$

$$c^{a_1} = (A_1 A_3 + A_1 A_2)P$$

For  $A_2$ :  $c^{a_2} = (\underline{A_1 A_2 A_3} + A_1 A_2 A_3 + \underline{A_1 A_2 A_3} + A_1 A_2 A_3)P$   
 $= [A_1 A_2 (A_3 + A_3) + A_2 (A_1 A_3 + A_1 A_3)]P$

$$c^{a_2} = [A_1 A_2 + A_2 (A_1 A_3 + A_1 A_3)]P$$

For  $A_3$ :  $c^{a_3} = (A_1 A_2 A_3 + A_1 A_2 A_3 + A_1 A_2 A_3 + A_1 A_2 A_3)P$   
 $= [A_1 A_3 (A_2 + A_2) + A_1 A_2 (A_2 + A_2)]P$

$$c^{a_3} = [A_1 A_3 + A_1 A_2]P$$

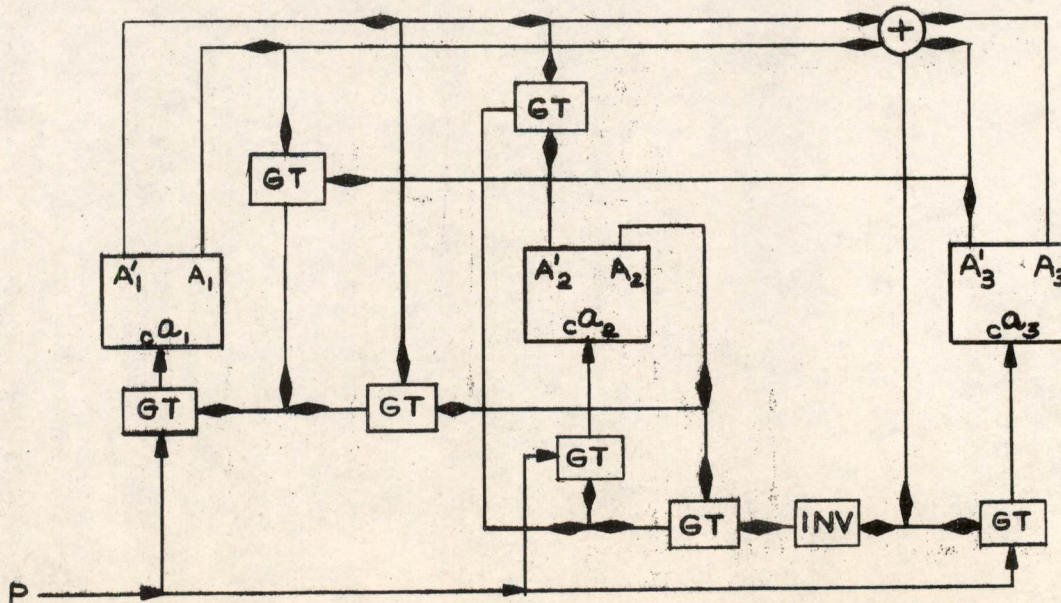
In order to simplify the block diagram for this counter, let us assume that we have available a "package" realization of  $x \oplus y$ .

$$c^{a_1} = (A_1 A_3 + A_1 A_2)P \text{ as before}$$

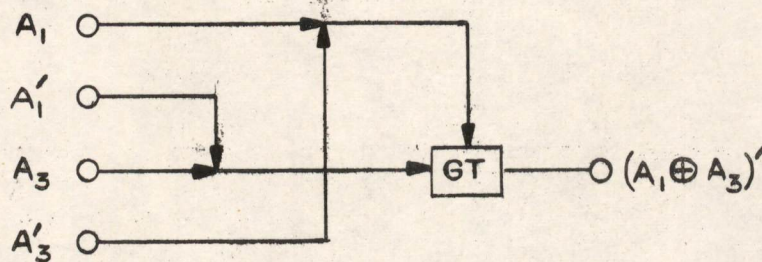
$$c^{a_2} = [A_1 A_2 + A_2 (A_1 \oplus A_3)]P$$

$$c^{a_3} = (A_1 \oplus A_3)P$$

We may now (assuming that inverters are cheap) use the same circuit for  $A_1 \oplus A_3$  in the second and third equations.



In case inverters are more expensive than gates, we might synthesize  $(A_1 \oplus A_3)'$  directly



[Note that this is the dual of the circuit for  $\oplus$ : we interchanged gates (.) and mixers (+)].

As a final example of the use of the algebra in synthesizing circuits we shall design an adder.

Let  $A_1$  and  $B_1$  be the digits to be added in stage #1, and let the carry into this stage be  $C_1$ . Then the carry out will be  $C_{1+1}$  and the well known table governs the action of the stage:

$A_1(t)$	$B_1(t)$	$C_1(t)$	$C_{1+1}(t)$	$A_1(t + T)$
1	1	1	1	1
0	1	1	1	0
1	0	1	1	0
0	0	1	0	1
1	1	0	1	0
0	1	0	0	1
1	0	0	0	1
0	0	0	0	0

Note that we require the carry to be instantaneous: there is to be no cumulative delay from stage to stage. Also note that the sum is to be stored in  $A_1$ . This time our table does not represent the successive states of a counter! We are interested in successive states of  $A_1$ . These are indicated row by row by looking first at column one and then at the parallel entry in the last column. Use complementable FF: (we wish to complement in cases 3, 4, 5, 6). Note that these are just the cases in which  $B_1(t) = C_1(t)$ , i.e.,  $B_1(t) \oplus C_1(t) = 1$

$$c_{a_i}(t) = [B_i(t) \oplus C_i(t)] P(t) \quad \text{[We have introduced the add command: } P(t)\text{].}$$

Now we need to know how to get  $C_{i+1}(t)$  as a function of the three parameters on the left. Apparently

$$C_{i+1} = (A_i B_i C_i + A_i' B_i C_i + A_i B_i' C_i + A_i B_i C_i') P$$

which can be factored:

$$C_{i+1} = [B_i C_i + (B_i \oplus C_i) A_i] P$$

or in unabbreviated form:

$$C_{i+1}(t) = [B_i(t) C_i(t) + (B_i(t) \oplus C_i(t)) A_i(t)] P(t)$$

Note that because of the delay presumed inherent in the flip-flop  $C_{i+1}$  will depend on the original  $A(t)$ , before complementing.

Further reduction: Since  $B_i(t) \oplus C_i(t)$  appears in both equations:

$$c_{a_i}(t) = [B_i(t) \oplus C_i(t)] P(t)$$

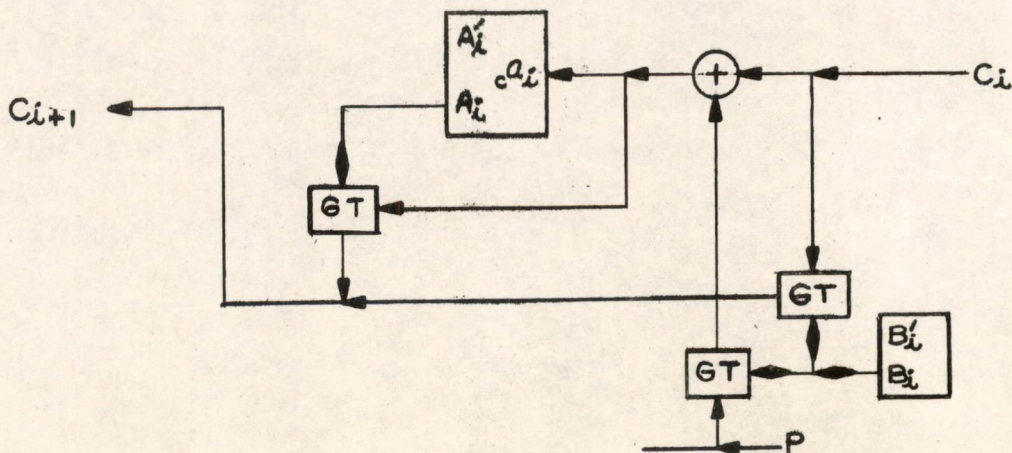
$$C_{i+1}(t) = B_i(t) C_i(t) P(t) + c_{a_i}(t) A_i(t)$$

Now  $C_i(t)$  is a result of gating various inputs from previous stages with the command pulse,  $P(t)$ . Therefore, we need not multiply it again by  $P(t)$ :

$$c_{a_i}(t) = B_i(t) P(t) \oplus C_i(t)$$

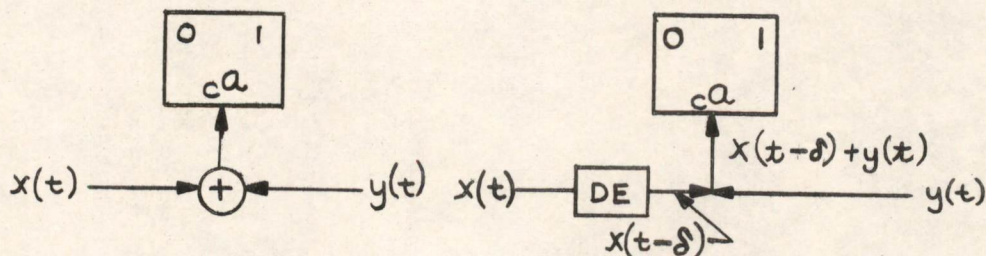
$$C_{i+1}(t) = B_i(t) C_i(t) + c_{a_i}(t) A_i(t)$$

Block Diagram



### 5.0 DELAY ELEMENTS

To illustrate our method of treating delay elements, consider the following device for realizing  $x \oplus y$  on the trigger input to a flip-flop.



It has already been noted that the realization of  $\oplus$  with ordinary electronic components requires two gates, two inverters (unless the complements of the inputs are also available) and a mixer; it is advantageous to trade for all this a delay element and a single mixer. The action of the second circuit is simple: if  $x$  and  $y$  both occur, the flip-flop is complemented twice, resulting in no change, whereas if one but not the other occurs it is complemented only once.

We can easily derive the equivalence of the two circuits in our formalism, but we have as yet no mechanical way of determining where it would be judicious to introduce delays. In this respect our treatment of delays parallels that of flip-flops: the introduction of both flip-flops and delays is a problem of planning. The design problem takes those elements as data together with their operation cycle, and asks for the most economical connecting network which meets the "boundary conditions". (The analogy between flip-flops and delay elements has as its theoretical basis the fact that any delay element can be represented as a flip-flop gated with a clock of appropriate frequency and phase.)

### 6.0 OTHER PROBLEMS AND APPLICATIONS

#### Magnetic Devices

Ceramic and ferromagnetic cores act as memory devices in such a way that there is generally no continuous signal output indicating that the core holds a '0' or a '1'. It has already been proposed that such devices be interpreted as flip-flops with built-in gates.

The main apparent difficulty in applying this algebra to magnetic devices is that from a 2 state core, three outputs are possible: a pulse of "+" polarity, a pulse of "-" polarity and no pulse. We wish, if possible,

to avoid going over to a three-valued algebra for the analysis of these devices, first because of the complexity of such a formalism, and second because the cores are themselves devices which have only two states of magnetization in current applications.

It would be easy enough to resort to some such device as lumping together two of the three outputs from a core for the purposes of analysis; but it remains to be seen whether such a device will result in a theory which ignores important logical possibilities in circuits using magnetic cores. For further remarks, see Appendix III.

#### Probability in the Boolean Machine

When a computer is interpreted as a physical realization of a set of Boolean equations it becomes possible to apply probability theory in such a way that we obtain information about the density of information in critical registers. The application to input-output problems (buffer storage, etc.) is apparent. (See articles by Reed in Bibliography.)

#### Combinatorial Problems; Planning vs. Design

We have shown a method whereby, given the desired cycle, a logically optimum counter may be designed (relative to existing "packaged" realizations of logical functions). But this theory sheds no direct light on the problem: what is the most desirable cycle for a given application? Rather, we have suggested that the theory, in reducing the actual design to a routine process, leads the designer more quickly to that crucial question.  $N$  flip-flops are capable of  $2^N$  different configurations, and there are  $2^{2^N}$  different "counting" cycles which might be obtained. The optimum electronic realizations of these are not all of the same complexity; and often, in a particular application (say where arbitrary meanings are assigned to the various stages of the count) any one of a number of these cycles would be equally useful. The problem is then not: "What, for the given cycle, is the optimal realization?", but rather, "Comparing a number of usable cycles and their optimal realizations, which of these is optimum?" (which of a number of relative minima is least?)

We might call such decisions combinatorial rather than logical. The algebra, as developed here, provides no complete solutions to such problems. However, it appears that the problem may be soluble by further analysis. (One possibility is this: formulate a set of fully mechanical rules for deciding between two circuits on grounds of relative complexity in terms of available components; then program a computer to work out all optimal designs (relative minima) and decide between them as to the absolute minimum.)

In general, the broader questions of computer planning are illuminated but not solved by the present theory. It is entirely possible that further theoretical development, incorporating combinatory, statistical and information-theoretic elements with the present theory may lead to a mathematical treatment of the broader questions concerning the organization of computing machinery.

The present theory gives something like the following general picture of digital computers. Any particular analog computer may be regarded as a physical realization or analyzer of a set of differential equations. Similarly we may regard any digital computer, general purpose or otherwise, as a physical realization or analyzer of a set of Boolean difference equations.

The equations analyzed by a machine may be studied in a perfectly abstract way (this has not been done here) just as the machine may be studied as a physical entity. Then two points of view are possible:

- (1) The Boolean difference equations describe the working of the machine.
- (2) The machine realizes or analyzes the equations.

It is the validity of the second point of view which motivates the building of any machine.

#### History of this Theory and Relation to Other Theories

The English mathematician, George Boole, presented, in 1847, the first workable but cumbersome predecessor of the present sort of formalism. He was interested in its interpretation as an algebra of logic and of probability, and it was the application to logic which inspired the investigations of his successors, W. S. Jevons, C. S. Peirce, E. Schroeder and others in increasing the power and simplicity of the algebra.

One logical interpretation of the present algebra is this: let the variables (dropping the time arguments altogether) represent sentences such as " $3 > 2$ ", " $3 > 5$ " and "Water boils at  $100^{\circ}\text{C}$ ". The two values 0 and 1 are interpreted respectively as falsity and truth, so that  $3 > 2 = 1$  but  $3 > 5 = 0$ . " $x'$ " is the sentence which is true when " $x$ " is false, and vice versa: (the contradictory of " $x$ ") "it is not the case that  $x$ " or briefly "not  $x$ ". Therefore,  $(3 > 5)' = 1$ . " $x \cdot y$ " is the sentence " $x$  and  $y$ ", which is true only when both  $x$  and  $y$  are true:  $(3 > 5) \cdot (3 > 2) = 0$ .  $x + y$  is  $x$  and/or  $y$  (briefly:  $x$  or  $y$ ), which is true if  $x$  is true or  $y$  is true or both are true:  $(3 > 5) + (3 > 2) = 1$ . Similar interpretations may be found for the other Boolean functions, and it will be seen that, on this interpretation, the theorems of the system are those laws of logic which apply to propositions and their combinations.

When we drop the assumption that the variables may have only the two values 0 and 1 there results a formalism which has as one of its interpretations a logic of classes containing the classical theory of syllogisms.

It was, as far as we know, Claude Shannon who, in 1938, first published an interpretation under which the algebra becomes a theory of relay and switching circuits. Shannon's interpretation led the way to an

application of the algebra to static information-processing networks of all kinds, including those used in present-day electronic digital computers. However, Shannon's theory took no account of the dependence on time of the states of a computer. Therefore, while it led to an analysis of networks of gates, mixers, inverters and the rest, it did not permit an analysis of flip-flops. That theory was no substantial help in designing counters, adders and so on.

After Shannon, the principal development of algebraic methods in this field came from Burkhart, Kalin and Aiken of the Harvard Computation Laboratory. In the form in which it was published in 1951, their algebra (which shared with Shannon's a lack of adequate means for representing time variables) was an arithmetic of 0 and 1.

<u>Boolean Algebra</u>	<u>Aiken's Formulation</u>
(+ and . have the meanings used in this text)	(+ and . have their ordinary arithmetical meanings)
$x'$	$1 - x$
$xy$	$xy$
$x + y$	$x + y - xy$

Superficially, the Aiken algebra is easier to use than Boolean algebra, since it is merely ordinary arithmetic restricted to 0 and 1. However, for every new law which one must learn in order to use Boolean algebra, one must learn an arithmetical trick to use the Aiken algebra. Consider, for example, the transformation which in Boolean algebra is accomplished by De Morgan's theorem:

$$(xy)' = x' + y'$$

In Aiken's algebra it becomes necessary to delicately introduce 1's and parentheses in order to go from  $1 - xy$  (our " $(xy)'$ ") to  $(1-x) + (1-y) - (1-x)(1-y)$  (our " $x' + y'$ "). Then Aiken's arithmetic is at least as hard to handle as Boolean algebra. Furthermore, it has the disadvantage that while an entire expression such as ' $x + y - xy$ ' (our ' $x + y$ ') is always either 0 or 1, yet such expressions often contain parts which are neither 0 nor 1, and hence meaningless. Thus if  $x = y = 1$ ,  $x + y - xy = 1$ , but part of it,  $x + y$ , is 2, which is meaningless in the interpretation. We have examined this matter here in some detail in order to justify our use of a simple but unfamiliar formalism rather than a familiar but unexpectedly complicated one.



The present theory, with its use of time variables throughout, is the work of Irving S. Reed. To our knowledge it is the first analysis of computing machines powerful enough to provide a general method for synthesizing flip-flop circuits such as accumulators by straightforward calculation. Furthermore, by designing not in terms of the sequence of states of the flip-flops, but rather in terms of the changes in their states, we are led directly to a minimal design, without the use of such cumbersome devices as "minimization charts".

It should be stressed that the present report is an account of the most direct and easily used practical outcomes of the theory. For a rigorous mathematical account of the theory the reader is referred to the papers by Reed in the Bibliography. The introduction of time variables makes possible an extension of Boolean algebra into analysis. The theoretical background of the results presented here is an analogue of the calculus and theory of ordinary differential equations, based, not on ordinary arithmetic, but rather on Boolean algebra.

These methods were used, in a restricted form, in the design of the MADDIDA and CADAC computers, beginning in the winter of 1947. One of the results of the theoretical studies has been that the present method is applicable to pulse circuits in general, and not only to computers using a special sort of clock waveform.

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Appendix I, Page 23  
Appendix II, Page 27  
Appendix III, Page 29

APPENDIX ISummary

x	y	x'	x + y	xy	x ⊕ y	x ↓ y	x   y
1	1	0	1	1	0	0	0
0	1	1	1	0	1	0	1
1	0	0	1	0	1	0	1
0	0	1	0	0	0	1	1

There are  $2^{2^n}$  distinct functions of  $n$  variables, some of which are repetitions of functions of  $n - 1$ ,  $n - 2$ , ..., 1, 0 variables. E.g.,  $x'$  appears above as a function of two variables (its value is defined for all 4 values of  $x$ ,  $y$ ; but since it is actually definable in terms of  $x$  alone, it is really a function of 1 variable). The two functions of 0 variables are 0 and 1.

There are an infinite number of functions in terms of which all functions can be defined. The two such functions of 2 variables are  $\downarrow$  and  $|$ . For example:

$$x|x = x'$$

$$(x|y)|(x|y) = xy$$

It follows that all other functions are definable in terms of  $|$ , since all functions are definable in terms of not and and:

$$x + y = (x'y')'$$

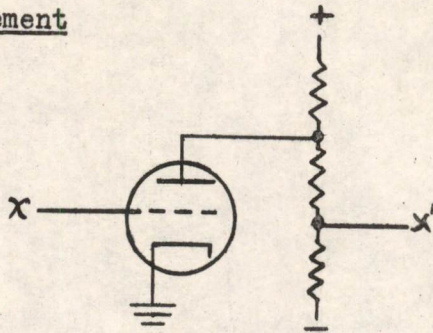
$$x \oplus y = xy' + x'y$$

etc.

Physical Realizations of Functions:

(The list is not complete) (In the magnetic circuits current in the indicated directions represents 1; no current represents 0; diodes might be necessary to prevent back flow and for clamping.)

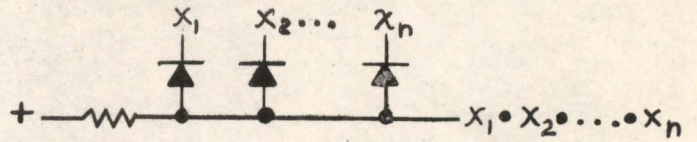
Complement



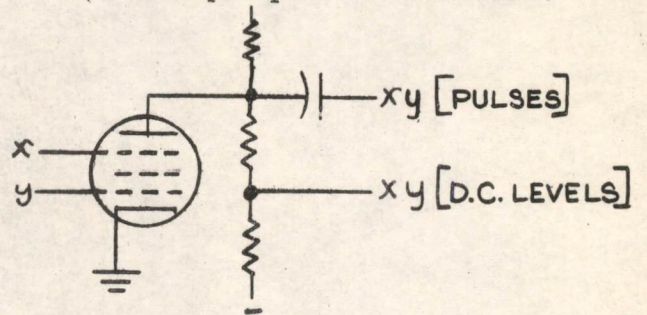
(Bias and voltage dividing network are such that when the grid goes positive, the  $x'$  point goes down to zero.)

Product

For  $n$  inputs:

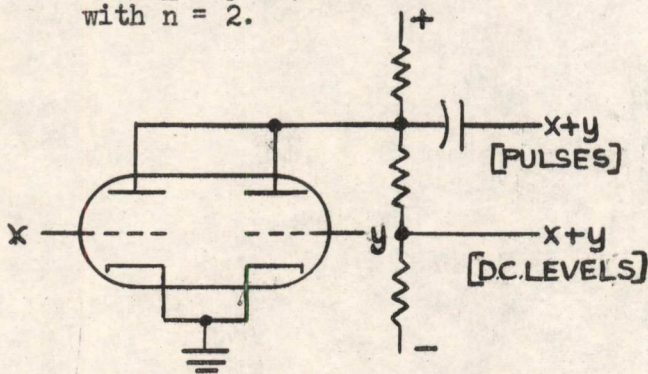


For 2 inputs; gives amplification:  
output pulse is inverted.



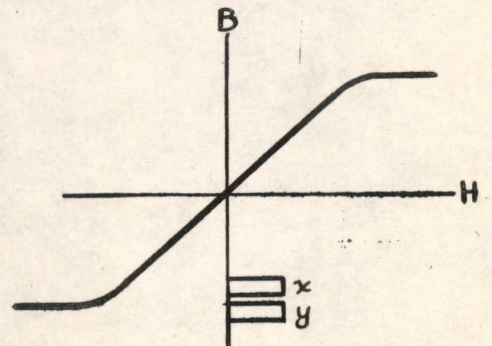
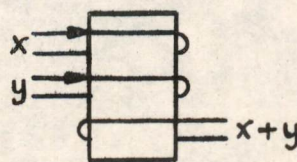
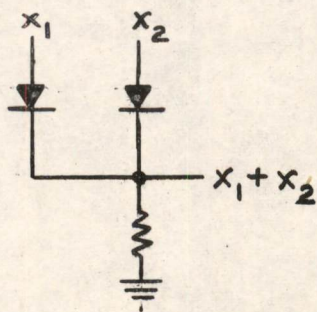
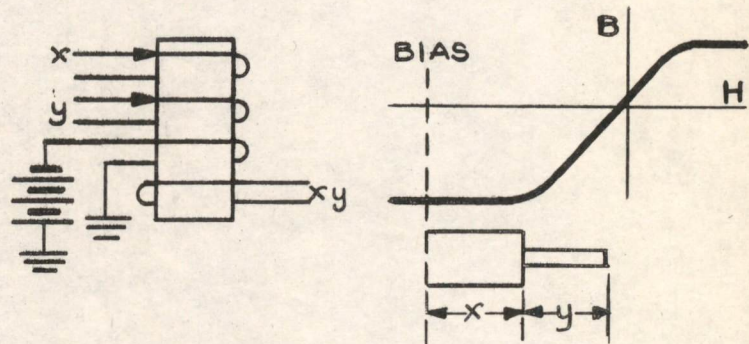
Sum

All circuits may be used with  $n$  inputs; shown here with  $n = 2$ .



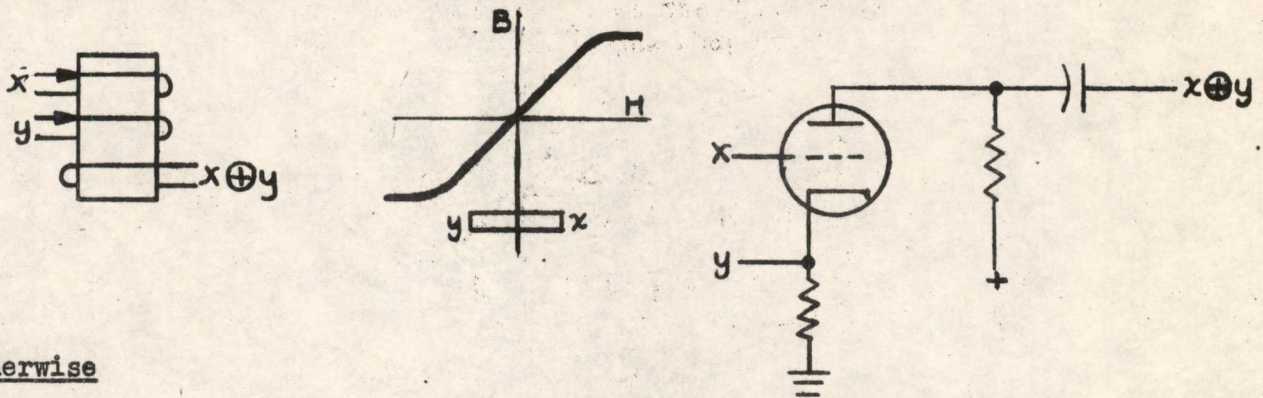
Provides Amplification;  
output pulse is inverted.

For  $n$  inputs (shown with  $n=2$ ):



Partial Sum

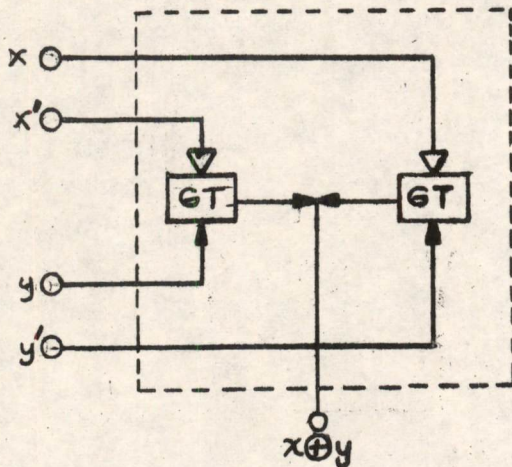
If you can ignore the polarity of the output and depend on the coincidence in time, duration, amplitude and shape of  $x$  and  $y$  -----



Otherwise

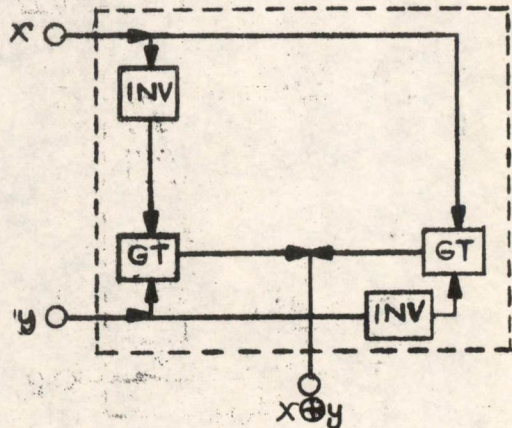
Black Box #1

(If the variables and also their primes are available.)



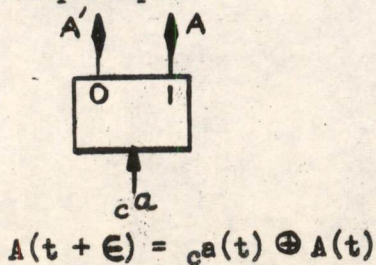
Black Box #2

(If the variables, but not their primes, are available.)



It follows from the statements on the previous page that, given realizations of not and and, black box realizations of all other functions can be constructed. And given realizations of ↓ or |, all needed black boxes can be constructed.

Flip-Flops

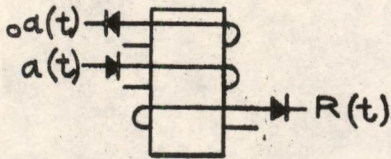


Triggers when both inputs are pulsed at once.

$A(t + \epsilon) = a(t)A'(t) + a'(t)A(t)$

(Reduces to the first case when  $a = a'$ )

Magnetic  
Memory Core



currents as shown represent 1. No current represents 0.

$\circ a(t)$	$a(t)$	$A(t)$	$A(t + \epsilon)$	$R(t)$
1	1	1	1	0
0	1	1	1	0
1	0	1	0	1
0	0	1	1	0
1	1	0	0	0
0	1	0	1	0
1	0	0	0	0
0	0	0	0	0

Value of A:  $\uparrow = 1, \downarrow = 0$

$$A(t + \epsilon) = [\circ a'(t) + a(t)] A(t) + [\circ a'(t) \cdot a(t)] A'(t)$$

$$R(t) = \circ a(t) a'(t) A(t)$$

This can be set and cleared; read out by clearing (if the core held a 1 there will be a pulse out). However: it won't trigger as shown, and the readout is a single pulse, rather than a D-C level.

APPENDIX IISome Theorems of Boolean Algebra

Ignore order and grouping in pure sums and pure products.

"Multiply through" and factor as in ordinary algebra, and: "add through" a product.

$$a(b + c) = ab + ac$$

$$a + (b.c) = (a + b).(a + c)$$

$$0 + x = x \quad 0.x = 0 \quad x + x = x \quad x + x' = 1$$

$$1 + x = 1 \quad 1.x = X \quad x . x = X \quad x . x' = 0$$

Expansion of a Function

$$\begin{aligned} f(x,y,z) &= f(0,0,0)x'y'z' + f(1,0,0)xy'z' + \dots + f(1,1,1)xyz \\ &= [f(0,0,0) + xty+z] [f(1,0,0) + x'ty+z] \dots [f(1,1,1) + x'ty'+z'] \end{aligned}$$

In particular, for the constant function  $f(x,y,z) = I$  for all  $x,y,z$ , we get

$$I = x'y'z' + xy'z' + \dots + xyz \quad (\text{all 8 terms are present})$$

and for the constant  $f(x,y,z) = 0$  we get

$$0 = (xty+z) \bullet (x'ty+z) \bullet \dots \bullet (x'ty'+z') \quad (\text{all 8 factors are present})$$

De Morgan's Law:  $(xy)' = x' + y'$  ;  $(xty) = x'y'$

Elimination of a factor:  $x + x'y = x + y$

Theorems relating to  $\oplus$  :

$$x \oplus (y \oplus z) = (x \oplus y) \oplus z = x \oplus y \oplus z$$

$$x \oplus y = y \oplus x$$

$$x \oplus y = xy' + x'y$$

$$x + y = x \oplus y \oplus xy$$

$$(x \oplus y)' = x' \oplus y = x \oplus y'$$

$[(x \oplus y)']$  is an interesting function: it is 1 exactly when  $x$  and  $y$  have the same value.]

$$x(y \oplus z) = xy \oplus xz$$

If  $x \oplus y = z$ ,  $x = y \oplus z$  (Permits solution of equations)

$$x \oplus I = x'$$

$$x \oplus 0 = x$$

$$x \oplus x = 0$$

For a more complete list of theorems, see works of Couturat and Whitehead listed in Bibliography.

Any expression can be put in the form:

$$Ax + Bx'$$

e.g., the equation for the FF with 2 inputs is in that form.

To complement such an expression it is sufficient to complement the "coefficients":

$$(Ax + Bx')' = A'x + B'x'$$

APPENDIX III

Core Analysis with 3 Valued Logic

$\circ a(t)$	$a(t)$	$A(t)$	$A(t + \epsilon)$	$R(t)$
-1	-1	-1	-1	0
0	-1	-1	-1	0
1	-1	-1	-1	0
-1	0	-1	1	1
0	0	-1	-1	0
1	0	-1	-1	0
-1	1	-1	1	1
0	1	-1	1	1
1	1	-1	-1	0
-1	-1	0	0	0
0	-1	0	-1	-1
1	-1	0	-1	-1
-1	0	0	1	1
0	0	0	0	0
1	0	0	-1	-1
-1	1	0	1	1
0	1	0	1	1
1	1	0	0	0
-1	-1	1	1	0
0	-1	1	-1	-1
1	-1	1	-1	-1
-1	0	1	1	0
0	0	1	1	0
1	0	1	-1	-1
-1	1	1	1	0
0	1	1	1	0
1	1	1	1	0

$a(t) = +1$  has same effect

as  $\circ a(t) = +1$

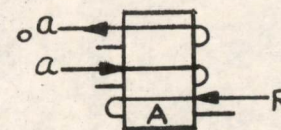
R is wound so that when the state of the core is moving toward 1,  $R = 1$ , i.e.,

$$[R(t) = 1] \Leftrightarrow [A(t) < A(t + \epsilon)]$$

$$[R(t) = 0] \Leftrightarrow [A(t) = A(t + \epsilon)]$$

$$[R(t) = -1] \Leftrightarrow [A(t) > A(t + \epsilon)]$$

" $\Leftrightarrow$ " means if and only if



State of the core:

$-1 = \downarrow$  ;  $+1 = \uparrow$  ;  $0 =$  no magnetization.

Currents in the windings are positive as shown by arrows. Opposite current:  $-1$ . No I:0.

The rules of 3 valued algebra are more cumbersome than those of the present theory.

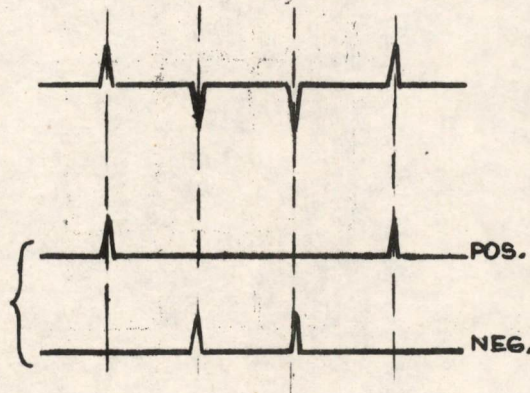
Note that cores require a 3 valued analysis only to the same extent that vacuum tube circuits do. In vacuum tube circuits, too, there are three possible inputs and outputs: positive, negative and zero pulses. In trying to account for such circuits in terms of 0 and 1 alone, we are somewhat farther from reality than when we use -1, 0 and 1. But the three valued analysis is itself a high-order abstraction from the real situation with its continuum of infinitely many values.



The point is that we pay for the additional simplicity of each higher order of abstraction in faithfulness of the resulting black-and-white picture of the real situation.

We believe that a 3 valued analysis would be of use, but the use would be a better evaluation of the limitations of the two valued approach. There may exist combinations of elements whose utility depends on the polarities of the pulses involved. Such designs could be "cranked out" of a 3 valued analysis. But it may be that, having recognized them, they can be introduced into the two valued analysis by special devices. One such device is translating a single pulse-train.

into two:



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