To Test Control

Ec

ScopeEndCarry

Arithmetic Check

Intensify

CopyOutEndCarry

CopyInEndCarry

Parity Check

Write On or Off

Read Off

cF5

DE

Parity Count

CopyOut

Copy In

.5

Sense Address

Sense Operation

Sense Panel Storage

(op+adr?)

0 → AR

AR → SS

0 → SS

Add "1" to PC

Pc → AR

Reset AR

(Clear?

Parity Clear

From Test Control

FTPD

F0

F1

F2

F3

F4

ca, ad
cs, su

hv
sa.

co

ci

.7

1.0

sa

hv
ho

co, ci

No Storage

Storage →

AR → CS

0 → CS

In or Out

Shift

Right

Left

From Ac0

From AR

Sc EndCarry

Carry
Add Ar → Ac
(- Ac)? C → Ac ?
0 → Ac

Ac → Ar (Operation)

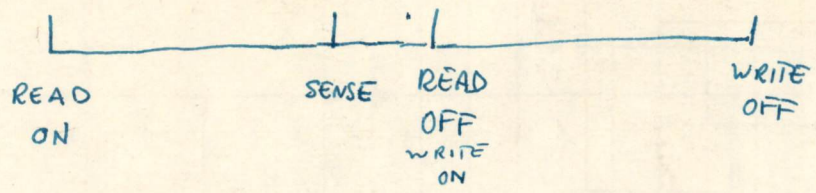
Ac → Ar (Address)

Carry
0 → Ac
Add
Check Over.
Sub "1" from Sc
C → Ar (?)
0 → Ar
Shift Right
Cycle Right
Read Out
Read In
Check Alarm

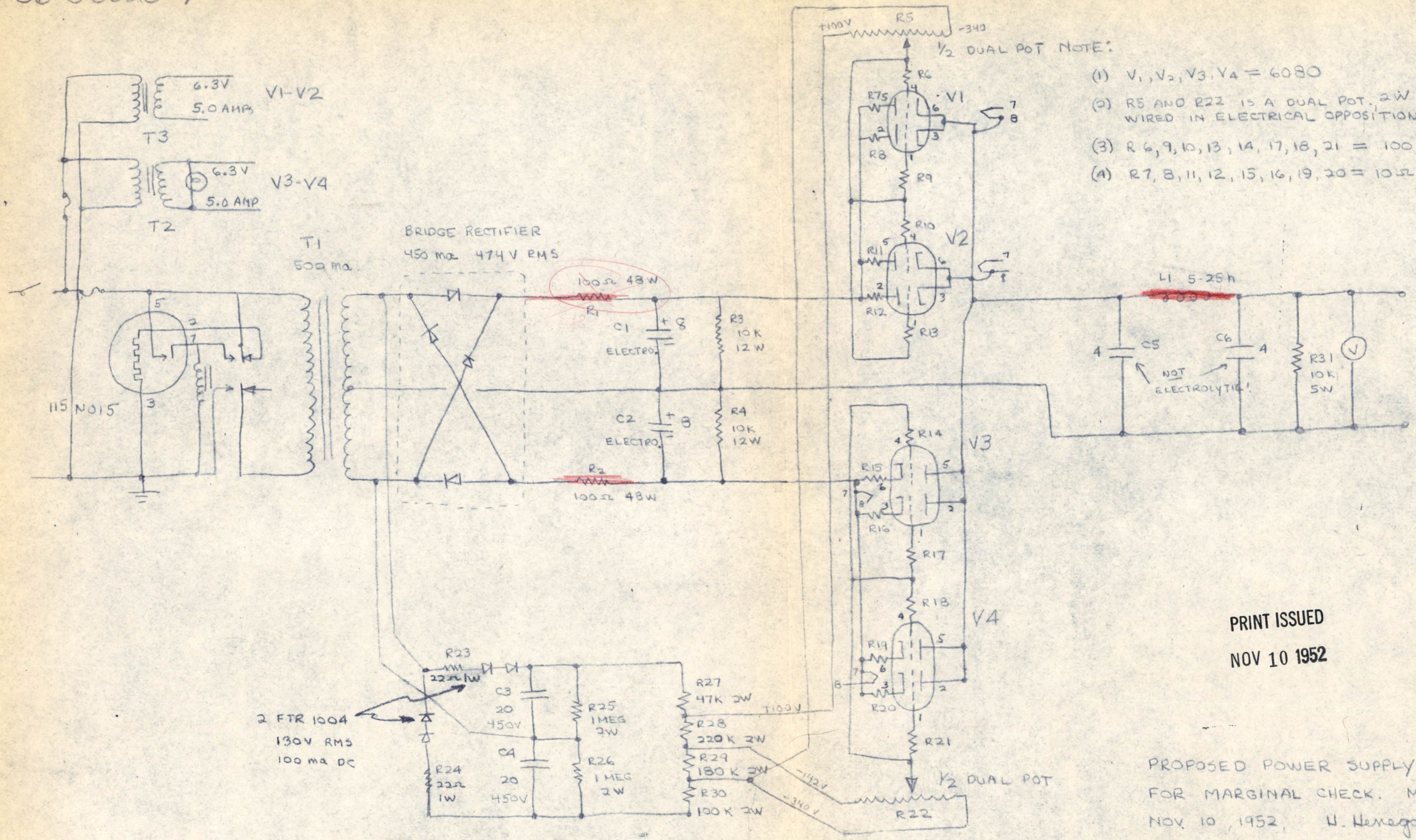
Ar → Pc
0 → Pc

M.T.C. Proposed
Control Switch
H. E. Anderson
10/27/52

Might be helpful to show the way the listed delays enter into the memory cycle:



SB-53025-1



(1) $V_1, V_2, V_3, V_4 = 6080$

(2) R5 AND R22 IS A DUAL POT. 2W WIRED IN ELECTRICAL OPPOSITION

(3) R 6, 9, 10, 13, 14, 17, 18, 21 = 100K 2W

(4) R 7, 8, 11, 12, 15, 16, 19, 20 = 10Ω 2W

PRINT ISSUED

NOV 10 1952

PROPOSED POWER SUPPLY FOR MARGINAL CHECK. MTC. NOV. 10, 1952, W. Henegar

SB-53025-1

FROM AR

17

G

LIVE REGISTER #1

LIVE REGISTER #2

LIVE REGISTER #3

LIVE REGISTER #4

17

G G

G G

G G

G G

F

.7

C F2°

F

READ T.S.

G

.2

.7

G

G

SENSE ADDRESS

SENSE OPERATION

CF5°

CF3'

2.0

PLUG PANEL

32

TOGGLE SWITCHES

PLUG

SS

TOG

17

OPERATION

ADDRESS

TO AR

G

17

32

PANEL STORAGE SWITCH

0 → SS

ON

5

FROM AR

0 → AR

.5

INV. DIFF.

PROPOSED M.T.C. TEST STORAGE

H.E. ANDERSON OCT. 16, 1952

PRINT ISSUED

OCT 28 1952

M. T. C. Proposed Order Code

Storage Orders

00000	hv	= Display V=N(AR) H=N(AR)
00001	ho	= " V=0 H=N(AR)
00010	sa	= special add (Overflow in alarm FF)
00011	—	
00100	td	
00101	—	
00110	ts	
00111	ci	= copy into Reg. X from In-Out Equip. via AR
01000	su	
01001	cs	
01010	ad	
01011	ca	
01100	td	
01101	—	
01110	ts	
01111	co	= copy from Reg X to In-Out Equp. via AR

Non-Storage Orders

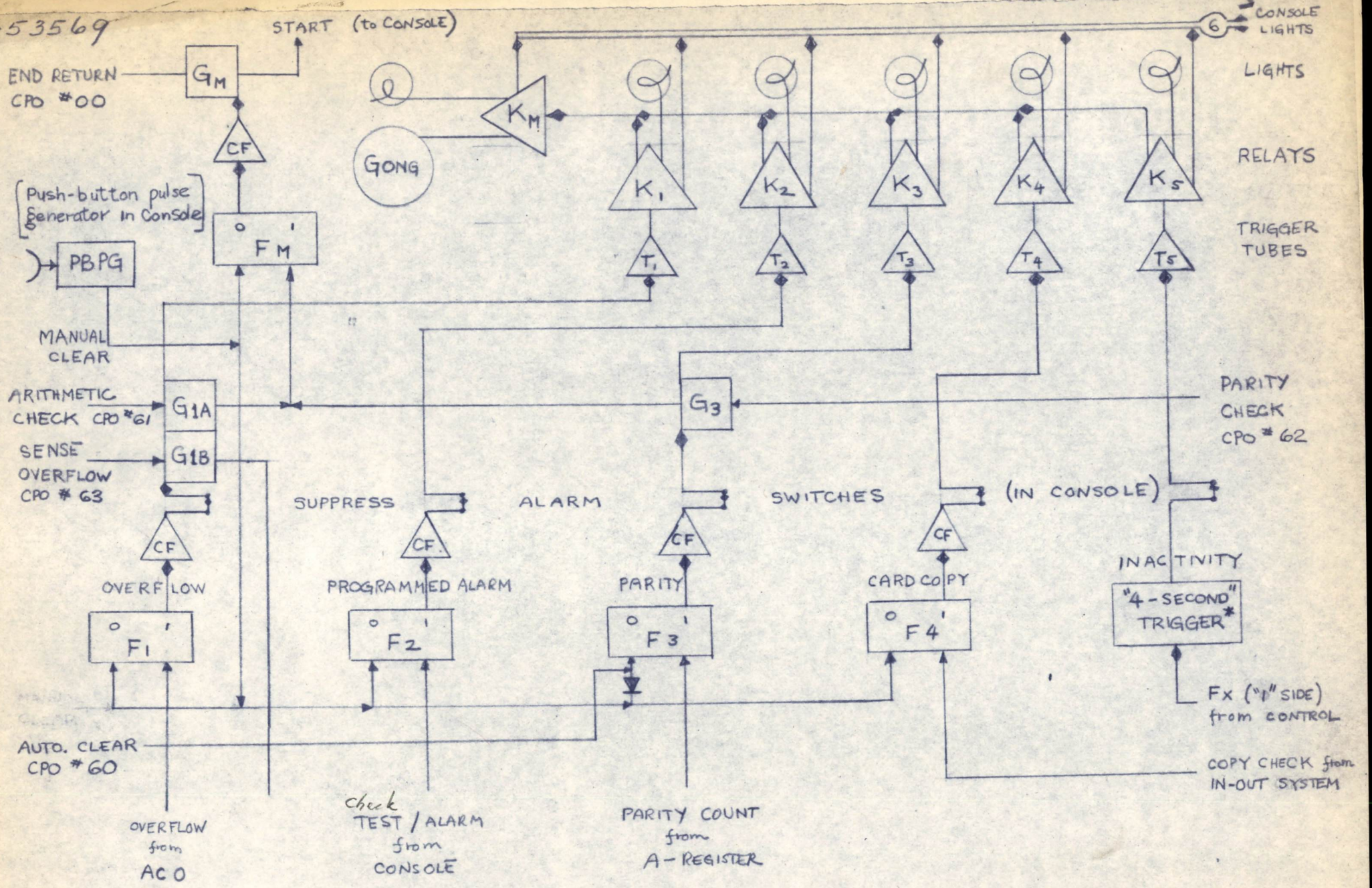
10000	th	= sp, check or alarm, halt
10001	tp	= sp, check or alarm
10010	kh	= cp, check or alarm, halt
10011	ck	= cp, check or alarm
10100	sh	= sp, halt
10101	sp	
10110	ch	= cp, halt
10111	cp	
11000	sl	= shift left arithmetically
11001	sl	
11010	cr	
11011	sr	
11100	ro	= read out (Prepare to punch a new card)
11101	ro	= " " " " " " " " "
11110	ri	= " in (" " read " " ")
11111	ri	= " " " " " " " " "

Note:
N(Ar) ≡ Number in Ar

PRINT ISSUED
OCT 28 1952

H.E. Anderson
10/27/52..

SA-53569



* The "4-second" trigger is restored once per instruction cycle and does not fire T_5 unless an interval of something like 4 seconds occurs between instructions.

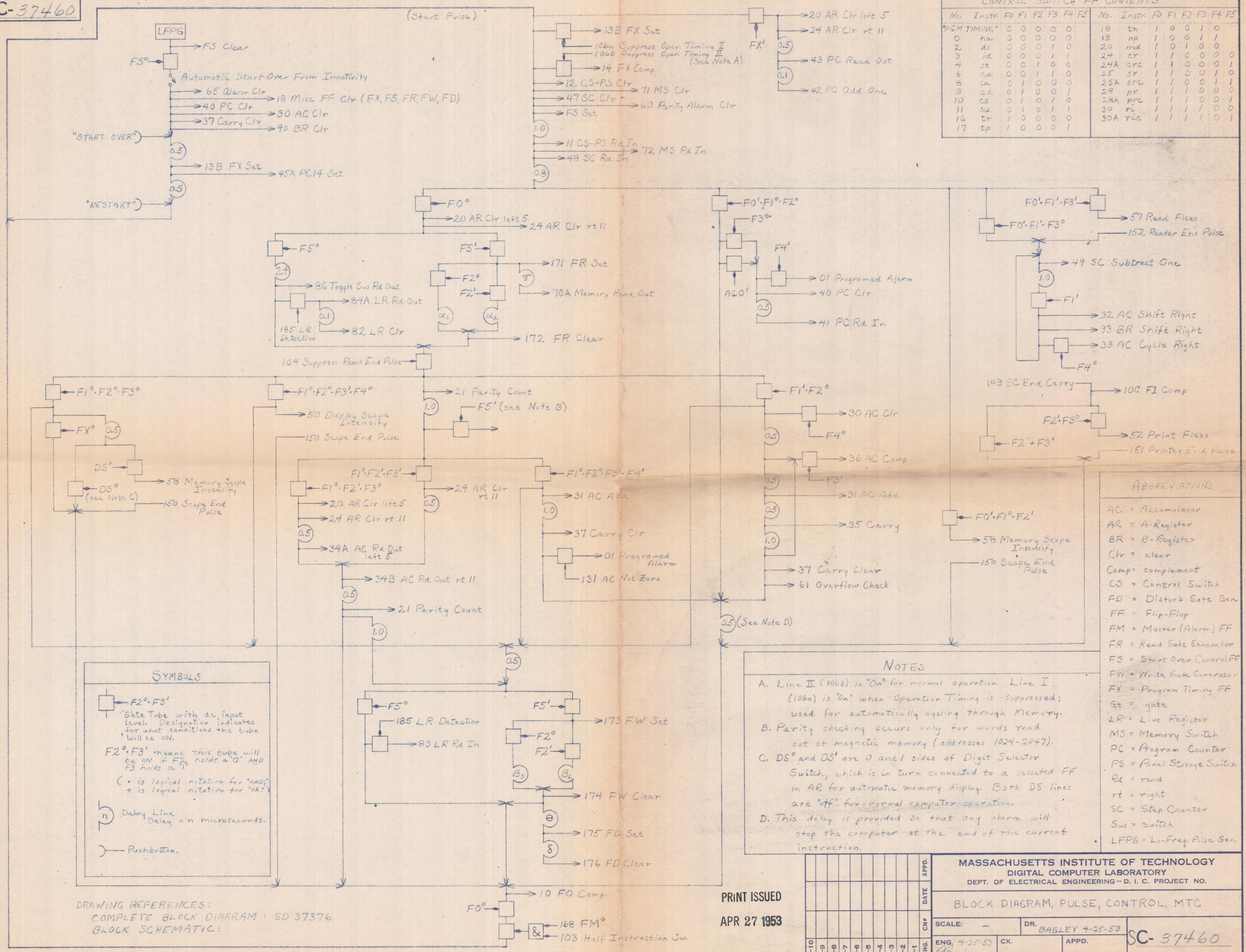
Suppress gang switch; suppress shut down / clear comp. lines

BLOCK SCHEMATIC MTC ALARM SYSTEM, K

W. A. Hosier Jan. 8, 1953

SA-53569

SC-37460



CONTROL SWITCH FF CONTENTS

No.	Instr.	F0	F1	F2	F3	F4	F5	No.	Instr.	F0	F1	F2	F3	F4	F5
"PGM TIMING"		0	0	0	0	0		18	tn	1	0	0	1	0	
0	ha	0	0	0	0	0		18	np	1	0	0	1	1	
2	ds	0	0	0	1	0		20	md	1	0	1	0	0	
3	id	0	0	0	1	1		24	cr	1	1	0	0	0	0
4	st	0	0	1	0	0		24A	crc	1	1	0	0	0	1
6	ra	0	0	1	1	0		25	sr	1	1	0	0	1	0
8	ca	0	1	0	0	0		25A	src	1	1	0	0	1	1
3	ad	0	1	0	0	1		28	pr	1	1	1	0	0	0
10	cs	0	1	0	1	0		28A	prc	1	1	1	0	0	1
11	su	0	1	0	1	1		30	ri	1	1	1	1	0	0
16	tr	1	0	0	0	0		30A	ric	1	1	1	1	0	1
17	tp	1	0	0	0	1									

ABBREVIATIONS

AC = Accumulator
AR = A-Register
BR = B-Register
Clr = clear
Comp = complement
CS = Control Switch
FD = Disturb Gate Gen.
FF = Flip-Flop
FM = Master (Alarm) FF
FR = Read Gate Generator
FS = Start Over Control FF
FW = Write Gate Generator
FX = Program Timing FF
Gt = gate
LR = Live Register
MS = Memory Switch
PC = Program Counter
PS = Panel Storage Switch
Rd = read
rt = right
SC = Step Counter
Sw = switch
LFPG = Lo-Freq. Pulse Gen.

SYMBOLS

F2°·F3' — "Gate Tube with dc input level. Designation indicates for what conditions the tube will be ON.

F2°·F3' means this tube will be ON if F2 holds a "0" AND F3 holds a "1."

(· is logical notation for "AND;" + is logical notation for "OR.")

n — Delay Line. Delay = n microseconds.

Pushbutton.

NOTES

A. Line II (106b) is "On" for normal operation. Line I (106a) is "On" when Operation Timing is suppressed; used for automatically cycling through Memory.

B. Parity checking occurs only for words read out of magnetic memory (addresses 1024-2047).

C. DS° and DS' are 0 and 1 sides of Digit Selector Switch, which is in turn connected to a selected FF in AR for automatic memory display. Both DS lines are "off" for normal computer operation.

D. This delay is provided so that any alarm will stop the computer at the end of the current instruction.

DRAWING REFERENCES:
COMPLETE BLOCK DIAGRAM : SD 37376
BLOCK SCHEMATIC:

PRINT ISSUED
APR 27 1953

	APPD.	DATE	CN#	CHG.
-10				
-9				
-8				
-7				
-6				
-5				
-4				
-3				
-2				
-1				

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING — D. I. C. PROJECT NO.

BLOCK DIAGRAM, PULSE, CONTROL, MTC

SCALE: —	DR. BAGLEY 4-25-53	SC-37460
ENG. 4-25-53	CK.	APPD.

SD-53580

Control Sw. FF Contents						
No.	Instn.	F0	F1	F2	F3	F4	F5
Pow	Time	0	0	0	0	0	
0	ha	0	0	0	0	0	
2	ds	0	0	0	0	1	0
3	id	0	0	0	1	1	
4	st	0	0	1	0	0	
6	ha	0	0	1	1	0	
8	ca	0	1	0	0	0	
9	od	0	1	0	0	1	
10	cs	0	1	0	1	0	
11	su	0	1	0	1	1	
16	tr	1	0	0	0	0	
17	tp	1	0	0	0	1	
18	tn	1	0	0	1	0	
19	np	1	0	0	1	1	
20	md	1	0	1	0	0	
24	cm	1	1	0	0	0	0
24a	cde	1	1	0	0	0	1
25	sr	1	1	0	0	1	0
25a	src	1	1	0	0	1	1
28	pu	1	1	1	0	0	0
28a	pue	1	1	1	0	0	1
30	ri	1	1	1	1	0	0
30a	ric	1	1	1	1	0	1

401	F0°	F0'	F1°	F1'	F2°	F2'	F3°	F3'	F4°	F4'	F5°	F5'
250	251	252	253	254	255	256	257	258	259	260	261	
525B	305B	305B	408	414A	527B	210B	406A	305A	318A	227A	229B	
	318B	305A	405A	305A	527A	321A	305A	213A	323B	229A	229B	
	405A	210B	405B	318B	418B	405B	213B	412A			412B	
	405B	318A	210A	318A	305B	418B	318A				525A	
	515B	318B		210B	124B	529B	414A					
		527B		210A	116A		527A					
		527A		116B								
				124A								

Read down for order of cabling

Misc. FF's

730A, 730B → 203 FF 1 → 201J → 314B (pt, ha); 201K → 508B

510*, 814 → 816 FS 1 → 515A

208B, 805B, 208A → 203 FR 1 → 201A → Read Gate. 115

208D, 805B, 208C → 203 FW 1 → 201G → Write Gate minus. 116; 201D → " " plus. 118

208F, 805B, 208E → 203 FD 1 → 201F → Disturb Gate. 117

Key (unless otherwise noted)

- → Gate (V.T.)
- "or" gate (xtal)
- ▷ = Buffer Amp.
- ⊳ = Cable fall.
- "and" Gate (xtal)
- PG = Pulse Gen.
- ○ = Push Button pulse generator
- ∩ = Delay

Numbers on lines from B.A.'s refer to C.P.'s

No crossing lines connect

PRINT NO. 9
MAY 14 1953
ISSUED TO K. Olsen

GRADED BY: DATE: THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:
GRADE I FOR REFERENCE ONLY
5/21/53 GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING — D. I. C. PROJECT NO.

Block Schematic, Control, MTC

SCALE: DR. B. Farley

ENG. 5-13-53 C. Farley | CK. R. A. G. | APPD. 5-13-53 W. Bradley | SD-53580

CHG.	CNP	DATE	APPD.
-10		5/May/53	B.G.F.
-9			
-8			
-7			
-6			
-5			
-4			
-3			
-2			
-1			

H-E ALBANENE 1951

SD-53580

Control Sw. FF Contents						
No.	Instr.	F0	F1	F2	F3	F4	F5
Pgm. Time		0	0	0	0	0	
0	ha	0	0	0	0	0	
2	ds	0	0	0	0	1	0
3	id	0	0	0	0	1	1
4	st	0	0	1	0	0	
6	ra	0	0	1	1	0	
8	ca	0	1	0	0	0	
9	ad	0	1	0	0	1	
10	cs	0	1	0	1	0	
11	su	0	1	0	1	1	
16	tr	1	0	0	0	0	
17	tp	1	0	0	0	1	
18	tn	1	0	0	1	0	
19	np	1	0	0	1	1	
20	md	1	0	1	0	0	
24	cm	1	1	0	0	0	0
24a	cac	1	1	0	0	0	1
25	sh	1	1	0	0	1	0
25a	shc	1	1	0	0	1	1
28	pr	1	1	1	0	0	0
28a	pro	1	1	1	0	0	1
30	ri	1	1	1	1	0	0
30a	ric	1	1	1	1	0	1

F0°	F0'	F1°	F1'	F2°	F2'	F3°	F8'	F4°	F4'	F5°	F5'
250	251	252	253	254	255	256	257	258	259	260	261
525B	305B	305B	408	414A	527B	210B	405A	305A	318A	227A	229B
	318B	305A	405A	305A	527A	321A	305A	213A	323B	229A	229B
	405A	210B	405B	318B	418B	405B	213B	412A			412B
	405B	318A	210A	318A	305B	417B	318A				525A
	515B	318B		210B	124B	529B	414A				826A
		527B		210A	116A		527A				
		527A		116B							
				124A							

Read down for order of cabling

Misc. FF's

517³ 790A, 730B → 203G FX → 201J → 314B (pt, ha); 201K → 508B

517⁴, 814 → 816 FS → 515A

517³ 208B, 805B, 208A → 209A FR → 201A → Read Gate, 115

517³ 208D, 805B, 208C → 203B FW → 201C → Write Gate minus. 116; 201D → " " plus. 118

517³ 208F, 805B, 208E → 203C FD → 201F → Disturb Gate, 117

Key (unless otherwise noted)

- Gate (V.T.)
- "and" Gate (xtal)
- "or" gate (xtal)
- P.G. = Pulse Gen.
- = Buffer Amp.
- = Push Button pulse generator
- = Cathode fl.
- = Delay

Numbers on lines from B.A.'s refer to C.P.a's

No crossing lines connect

PRINT NO. 7
JUN 18 1953
ISSUED TO K. Olsen

GRADED BY: DATE: THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:
GRADE I FOR REFERENCE ONLY
5/2/53 GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN

CHG.	DATE	APPD.
-10		
-9		
-8		
-7		
-6		
-5		
-4		
-3	S258 6-4-53	JWF
-2	12 May 53	E.F.
-1		

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING — D. I. C. PROJECT NO.

Block Schematic, Control, MTC

SCALE:
DR. B. Farley
ENG. 5-12-53 G. Farley
CK. E. M. G.
APPD. 5-13-53 J. W. Forrester
SD-53580

K-E ALBANENE 1905

to ACCUMULATOR (16)

to CONTROL SWITCH (5)

AR "0" BUS OUT

to { MEMORY Z-AXIS (17) / STORAGE SWITCH (11) }

AR "1" BUS OUT

to PROGRAM COUNTER (11)

Parity Count

G7 G16 G7 G17 G6 G16 G6 G16 G7 G17 G6 G16 G7 G17 G6 G7

CF2 CF1 CF2 CF1 CF2 CF1 CF2 CF1 CF2

Horiz Deflection

DECODER DECODER (Decoders on AR 0-9 only)

0 1 F1 0 1 F1 0 1 F1 0 1 F1 0 1 F1

to Parity Chm KF4

CLEAR CPO 20

COMPLEMENT from M.C. Control

from ACCUMULATOR (16)

AR "1" BUS IN

from { MEMORY (operation & address separately) (17) / PROGRAM COUNTER (11) }

AR 0 AR 1 AR 14 AR 15 (PARITY) AR 16

PRINT ISSUED
OCT 15 1952

BLOCK SCHEMATIC MTC
A-REGISTER, AR

WAH 10.15.52

SC-52836

Ac 0 | Ac 9 | Ac 10 | Ac 15

Ac → AR (Address) (Ac 5-15 only) CPO 34b

Ac → AR (Operation) (Ac 0-4 only) CPO 34a

Vertical Deflection (Ac 0-9 only)

CP Gate (Ac 0 only)

Overflow Pulse

Carry CPO 35

0 → Carry FF

C → Carry FF

C → Partial Sum FF

Add CPO 31

0 → Partial Sum FF CPO 30

Cycle Right (Ac 0 only) CPO 33

Shift Right (Ac 1-15 only) CPO 32

From AR

16 To AR

G10 · V. Decoder · G8 · F2 · B9 · G5 · G6 · B2 · F1 · B1 · G7 · G1 · G2

overflow

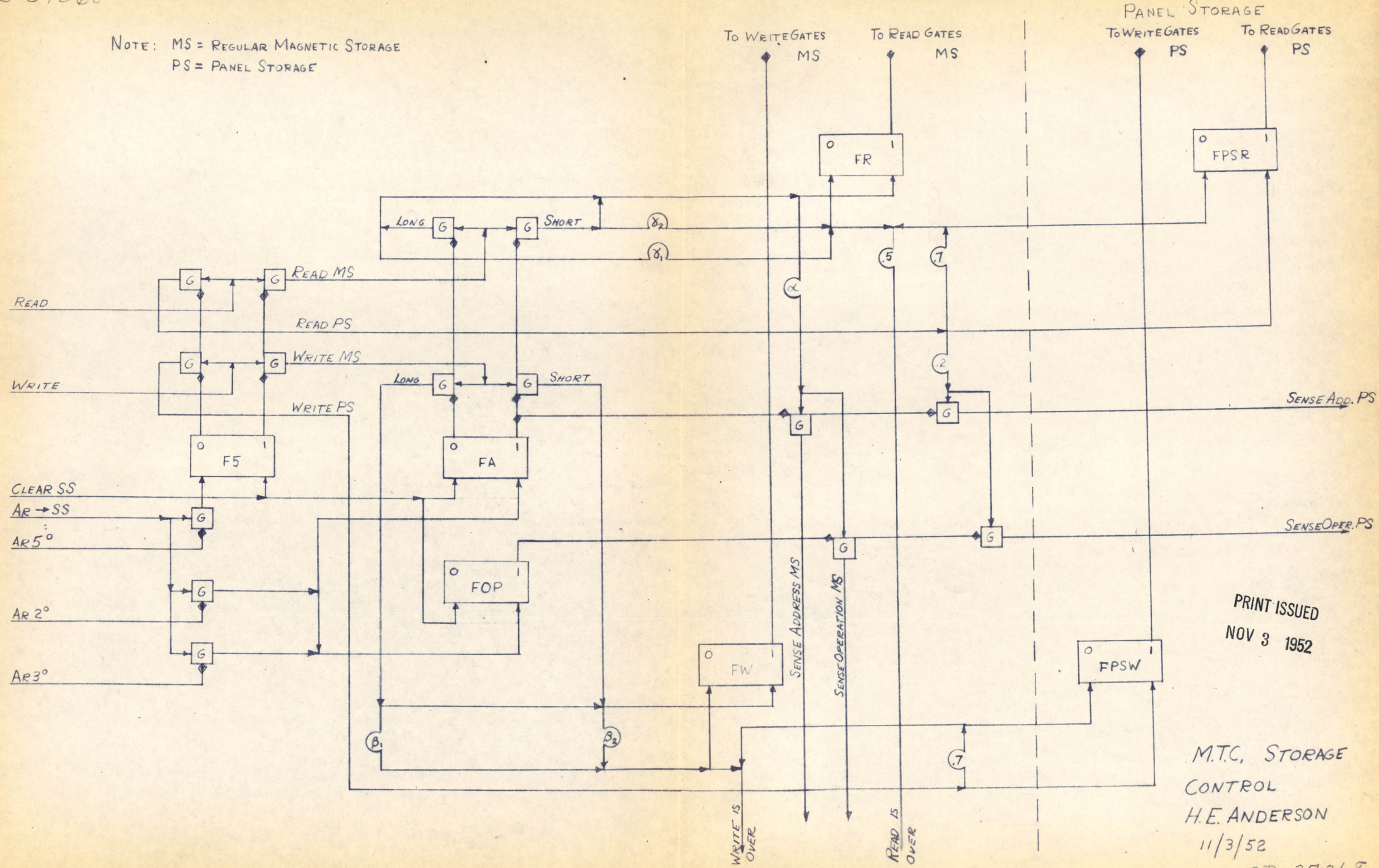
PRINT ISSUED
OCT 28 1952

Block Schematic
MTC Accumulator, Ac
H.E.A. Oct. 9, 1952

SC-52836

SB-37368

NOTE: MS = REGULAR MAGNETIC STORAGE
PS = PANEL STORAGE

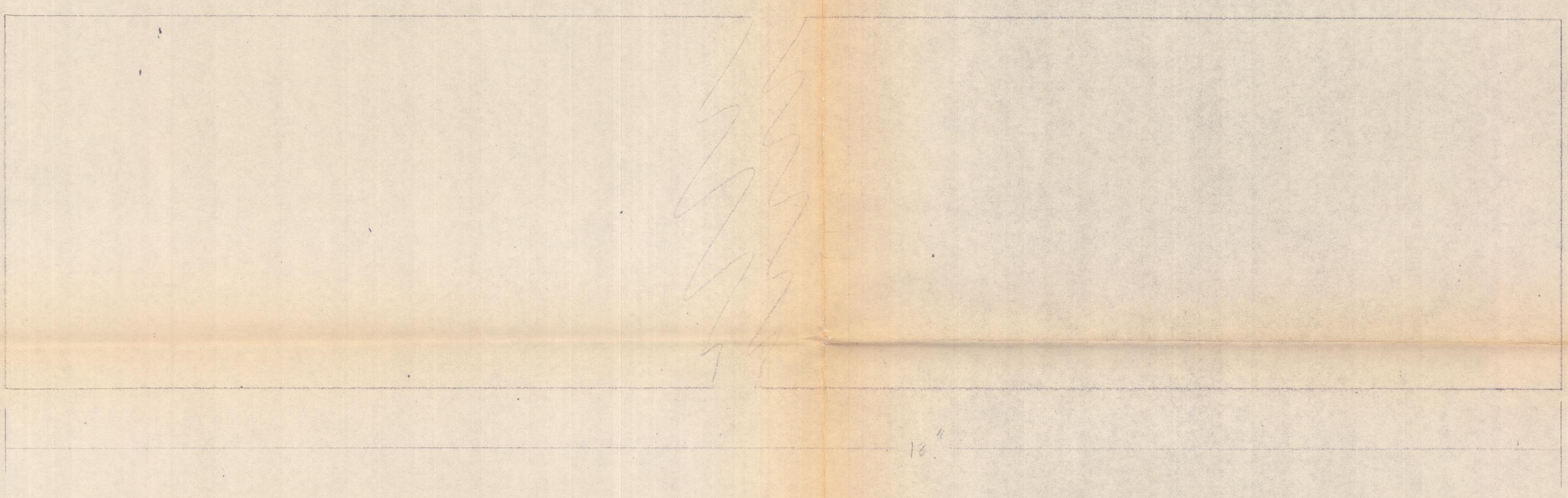


PRINT ISSUED
NOV 3 1952

M.T.C. STORAGE
CONTROL
H.E. ANDERSON
11/3/52

SB-37368

SC-58159



1/8" aluminum
no holes
gray hammertone paint
make one

PRELIMINARY PRINT
NOT TO BE USED FOR CHECKING OR FOR MANUFACTURE

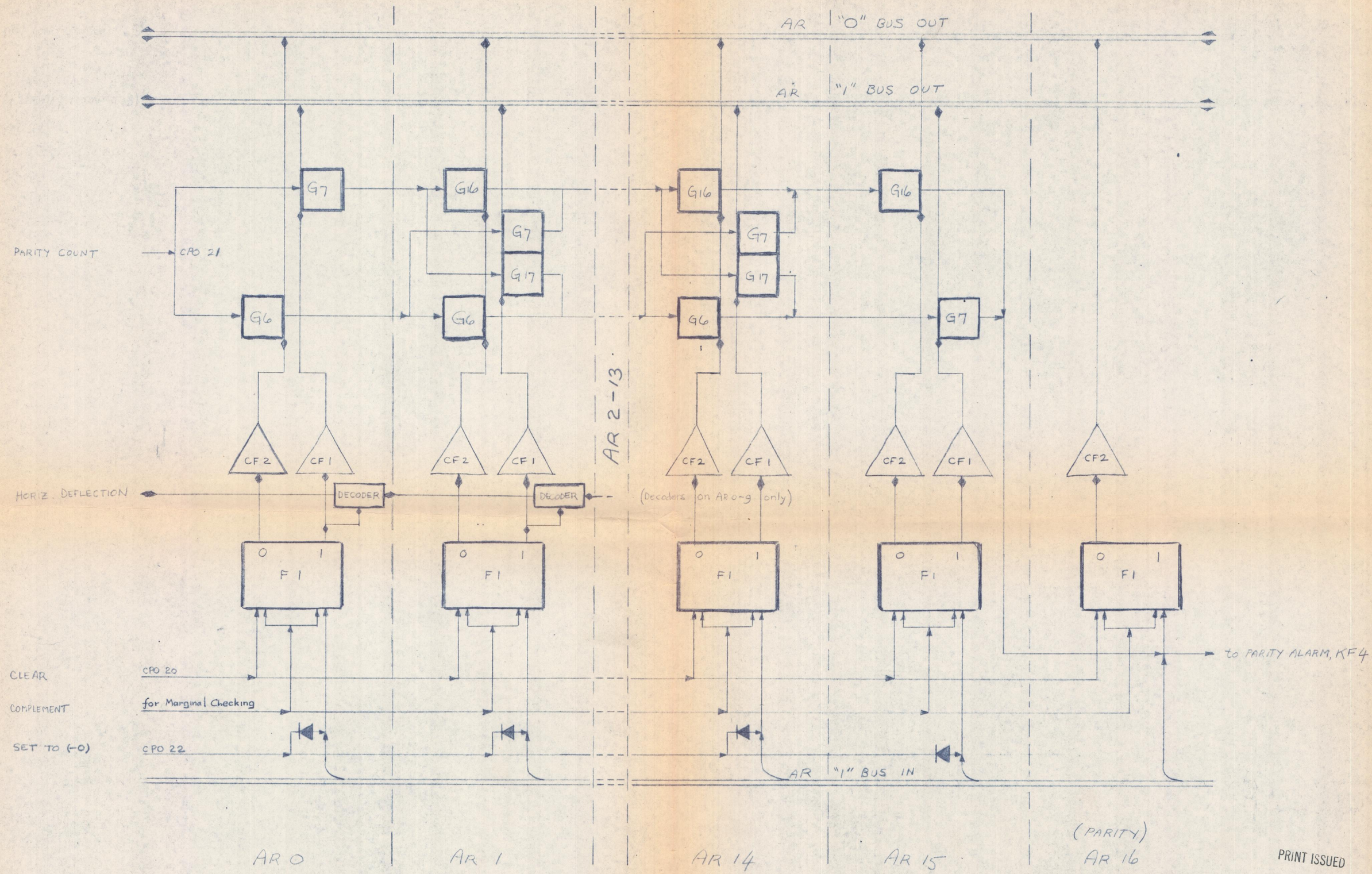
PRINT ISSUED
MAR 16 1954

Experimental Rock Filter

K Ole 15 March 1954.

SC-58159

SC-52834-1

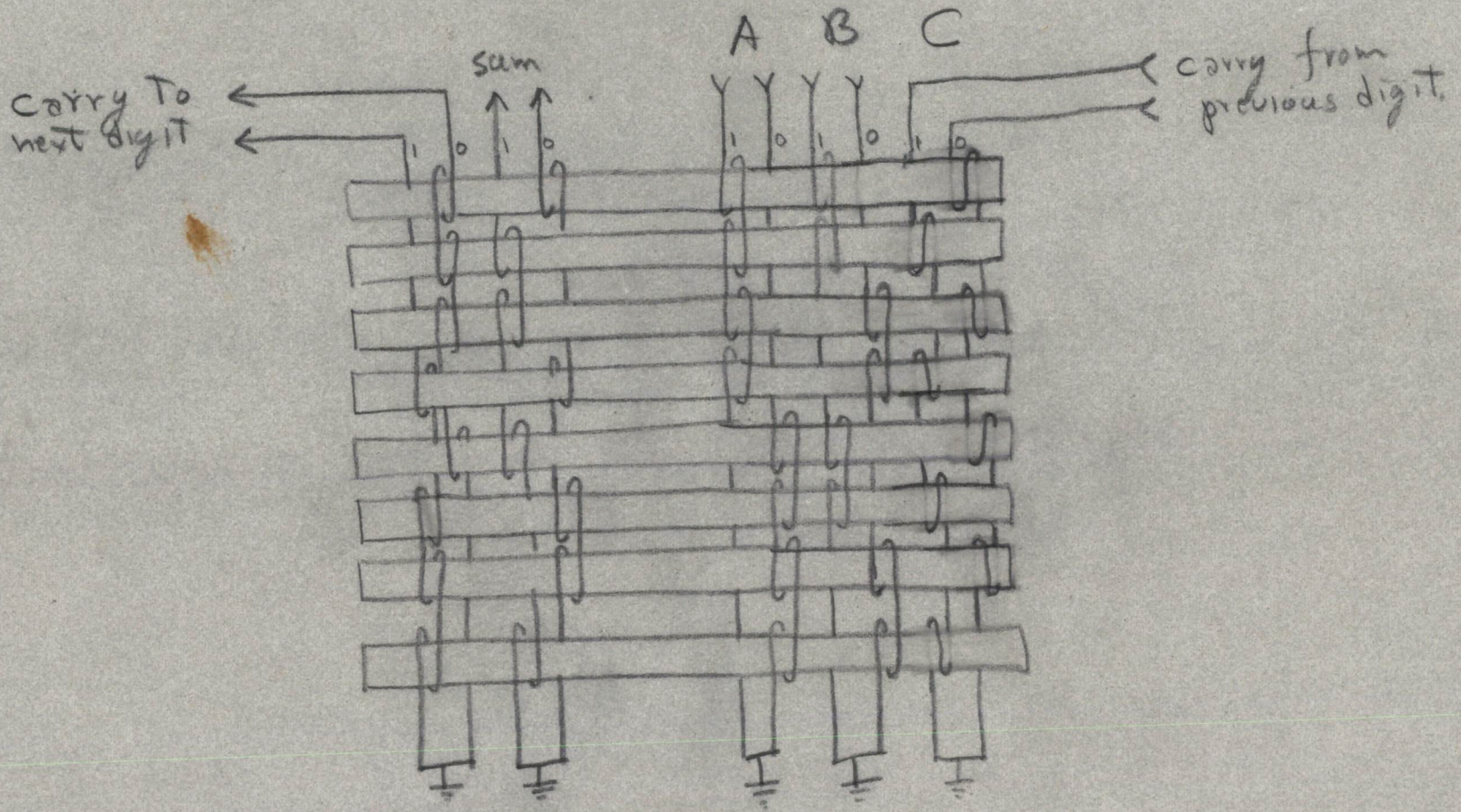


PRINT ISSUED
NOV 6 1952

BLOCK SCHEMATIC MTC
A-REGISTER, AR

WAH 10.15.52

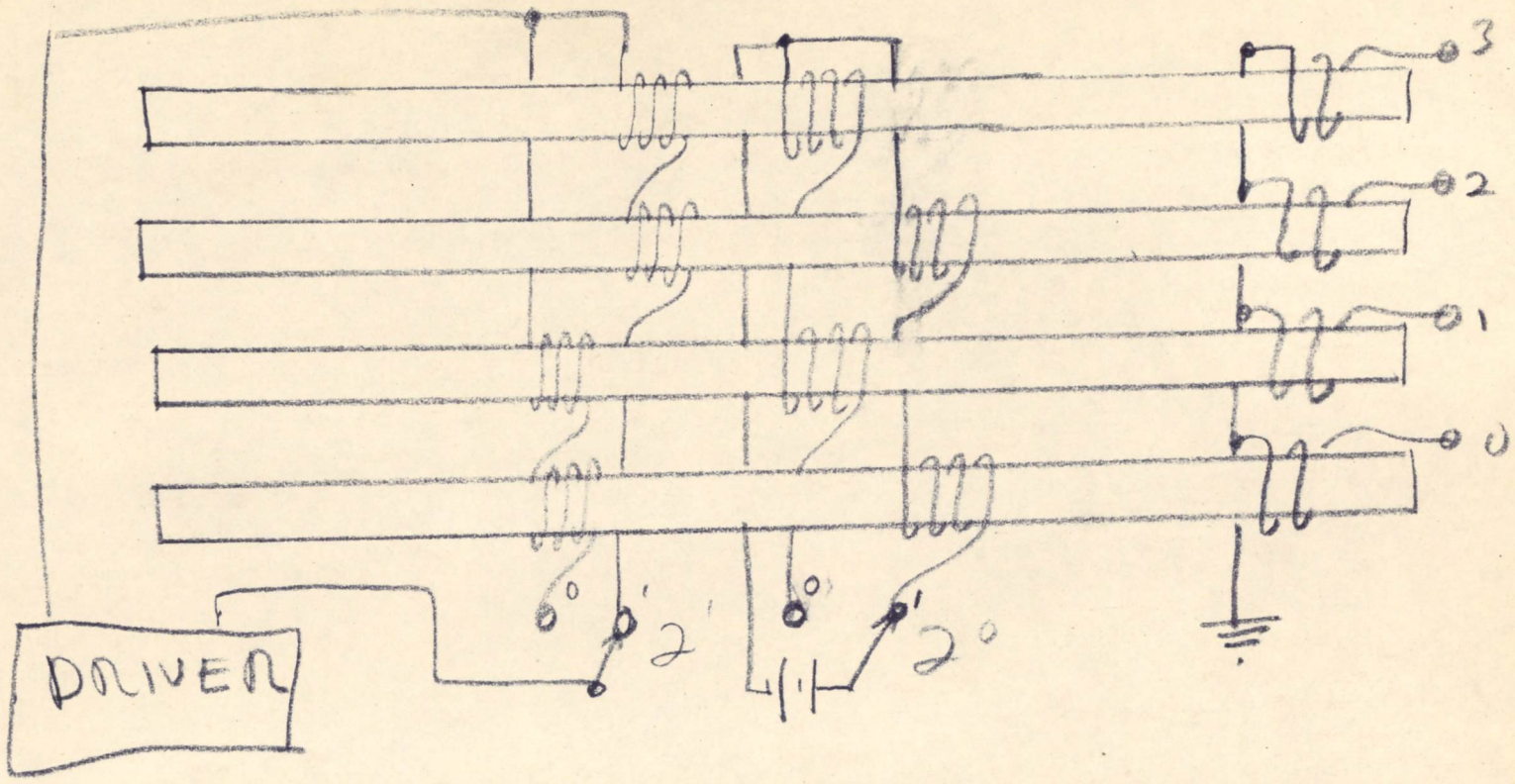
SC-52834-1



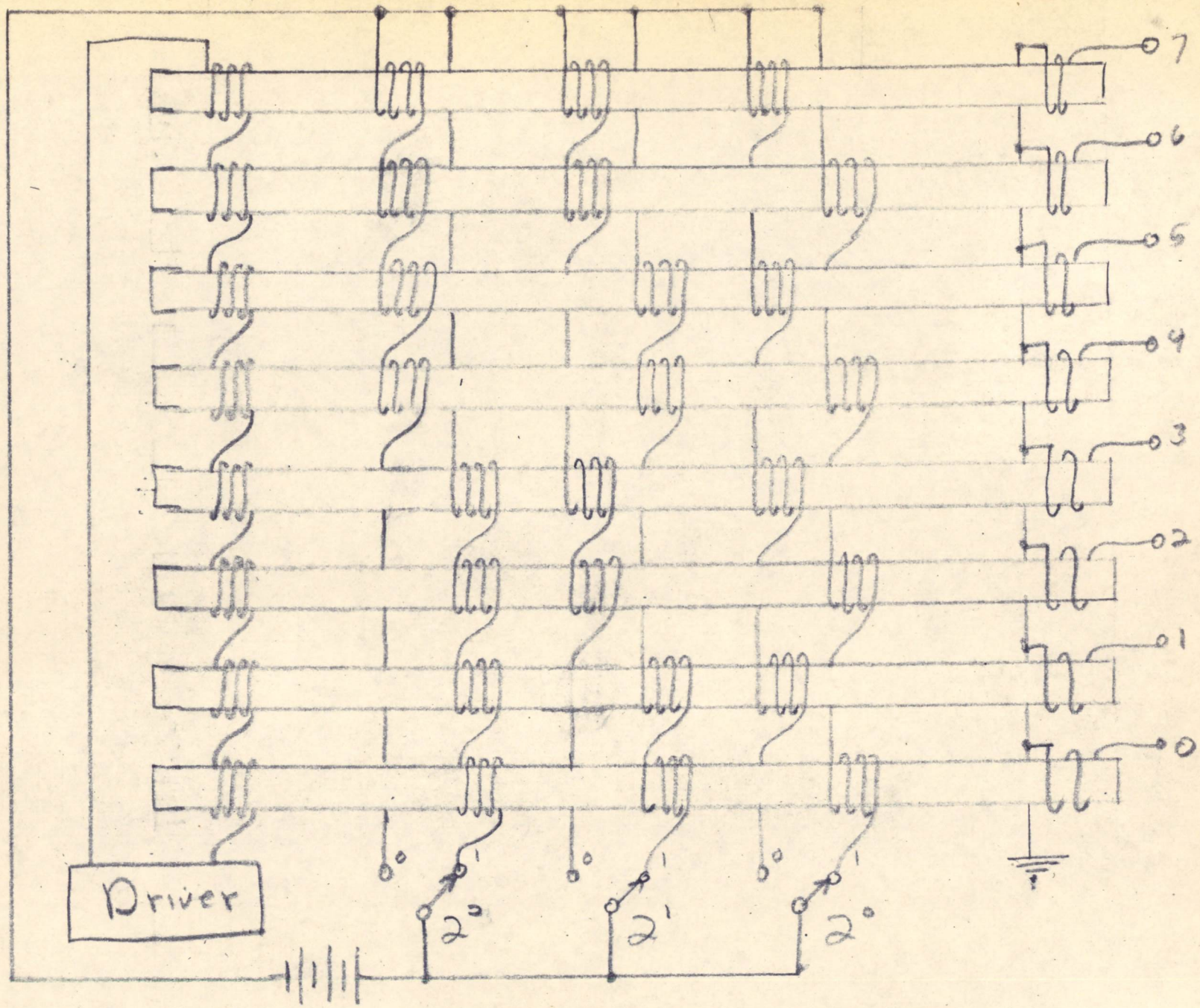
Single-Digit Adder

fig 9

Olsen 18 Feb 52

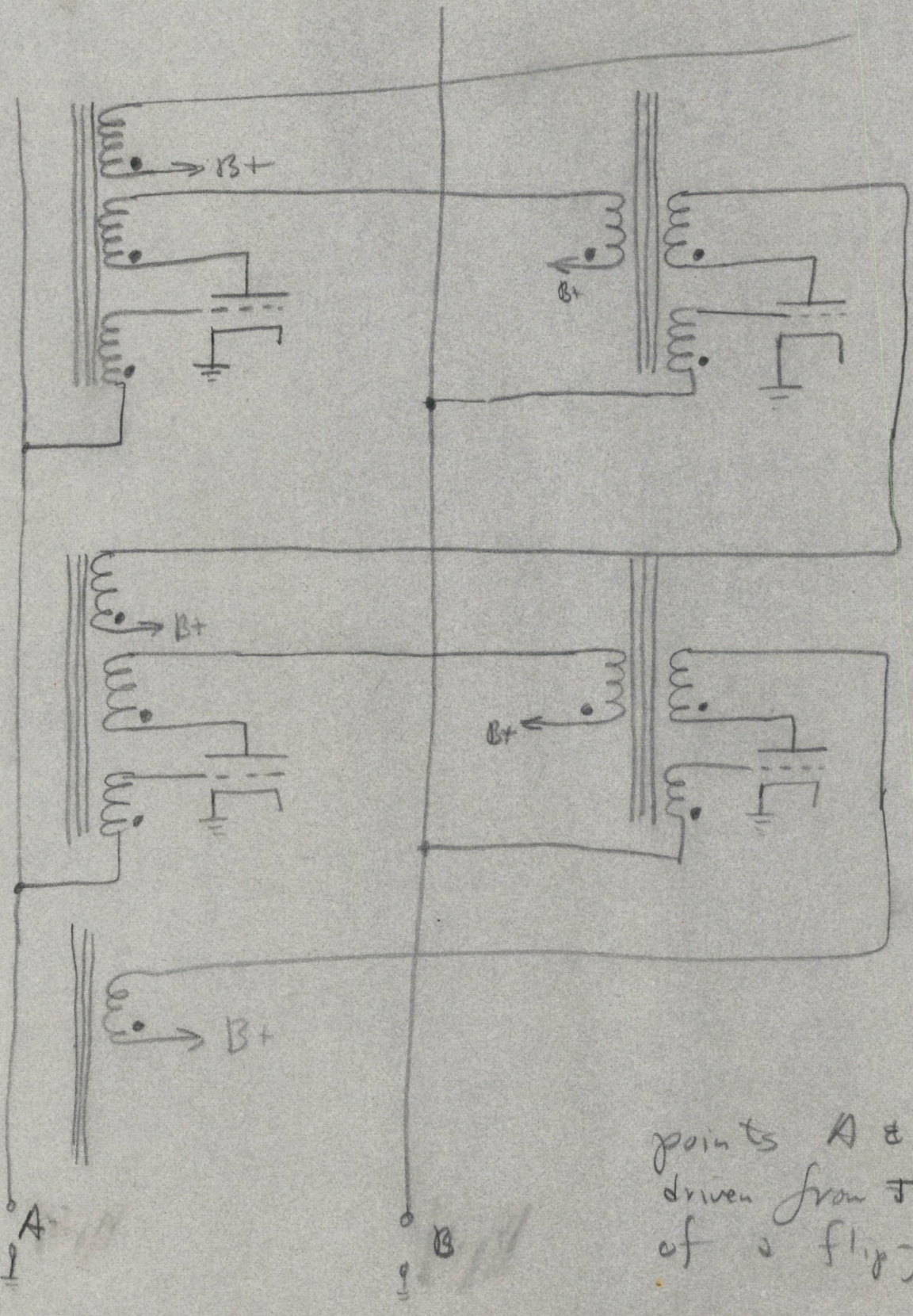


4 POSITION MAGNETIC MATRIX SWITCH (alternate)



8 POSITION Magnetic Matrix Switch

K Olsen 25 Feb

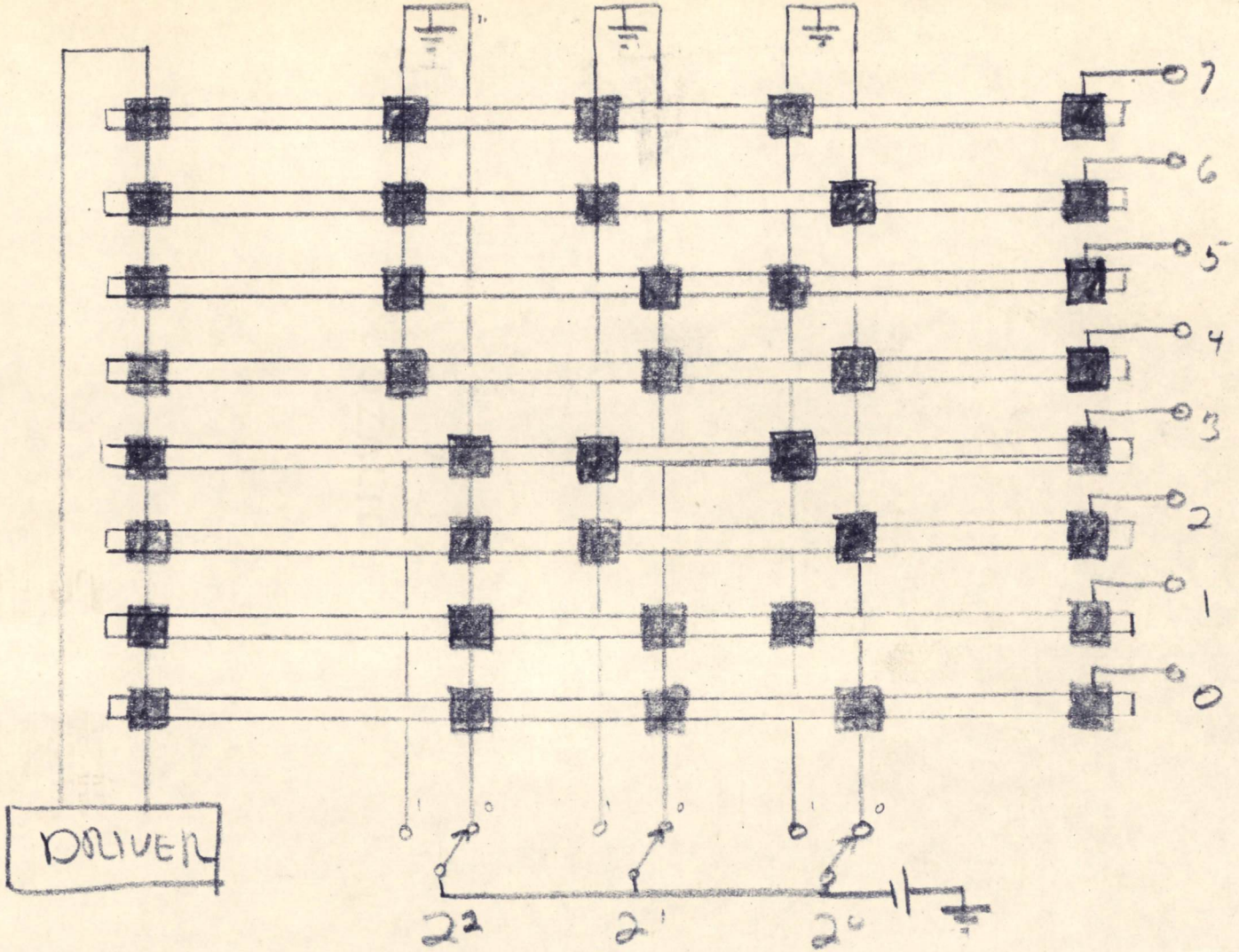


points A & B are driven from the plates of a flip-flop

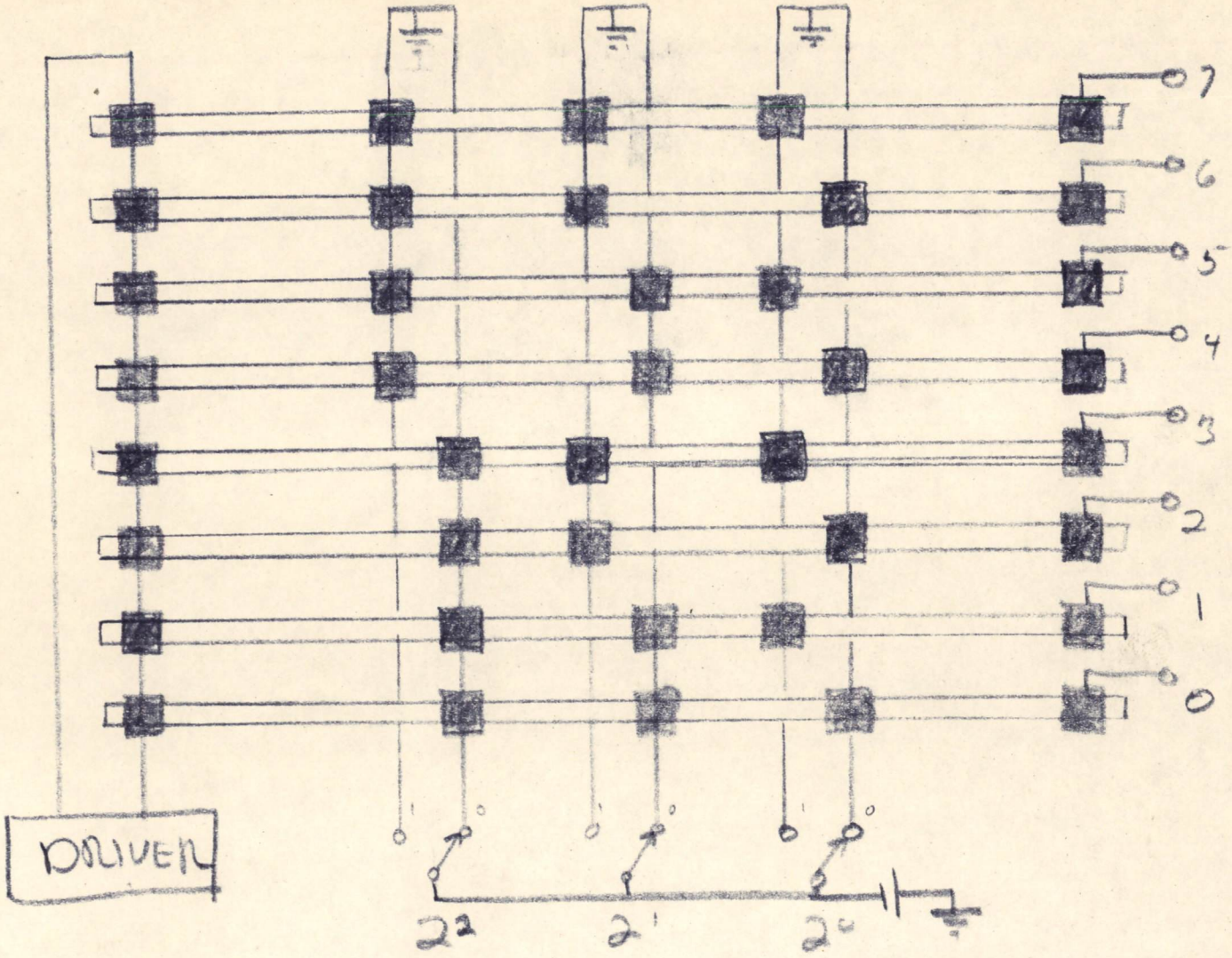
Blocking Oscillator Staging Register

K. Oka 27, June 1952

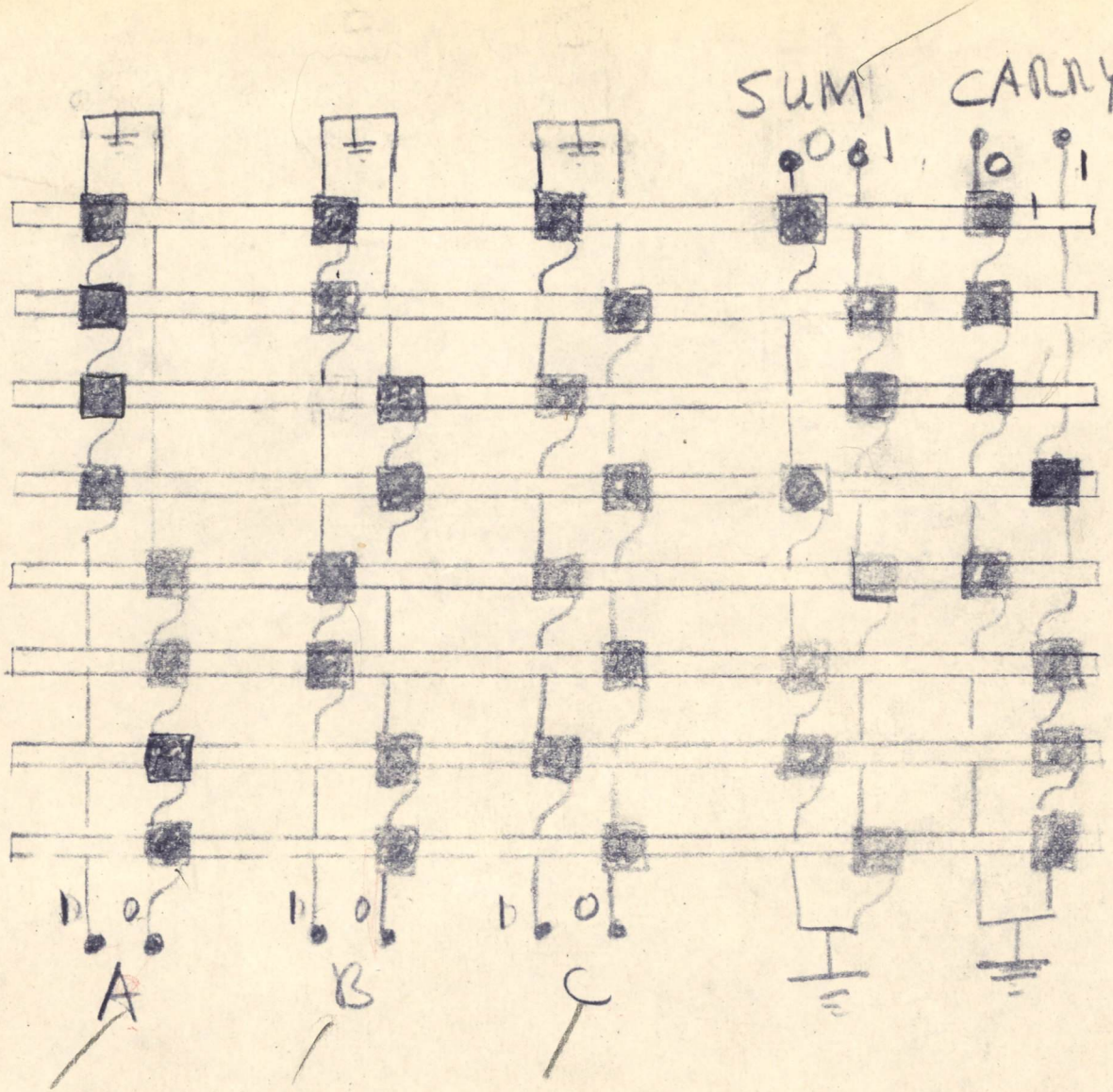
SA



8-POSITION MAGNETIC MATRIC SWITCH.

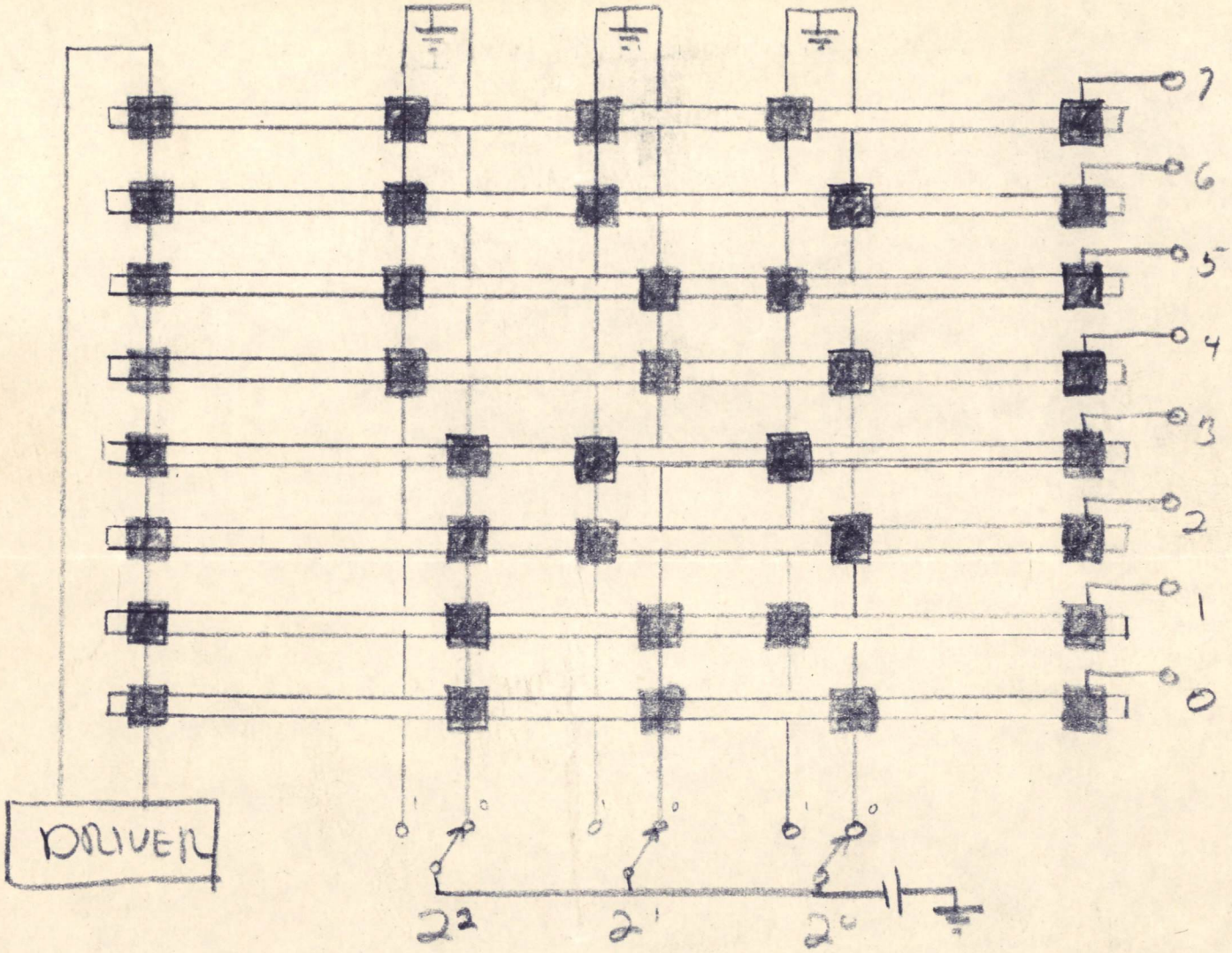


8-POSITION MAGNETIC MATRIC SWITCH.

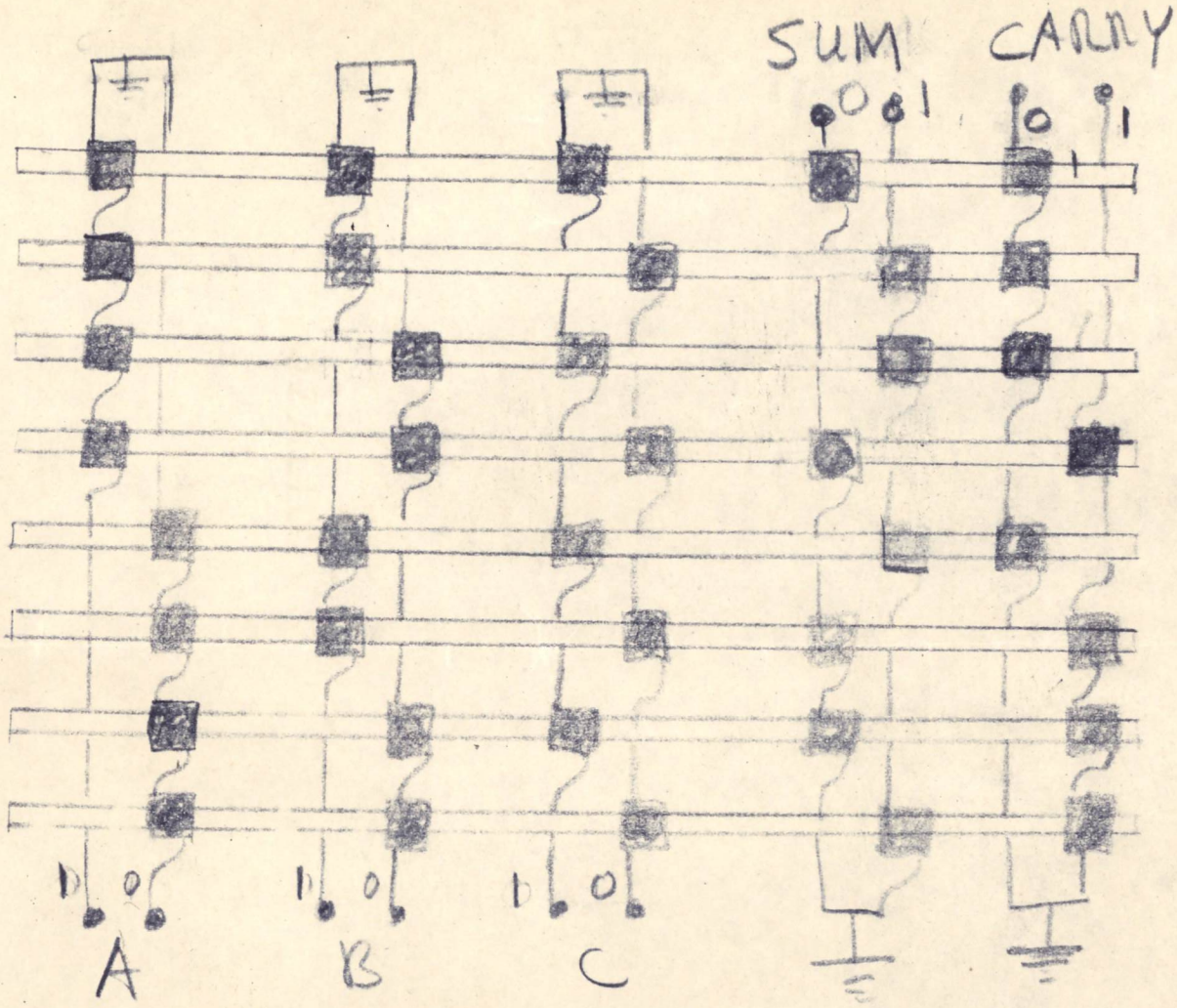


SINGLE DIGIT ADDER

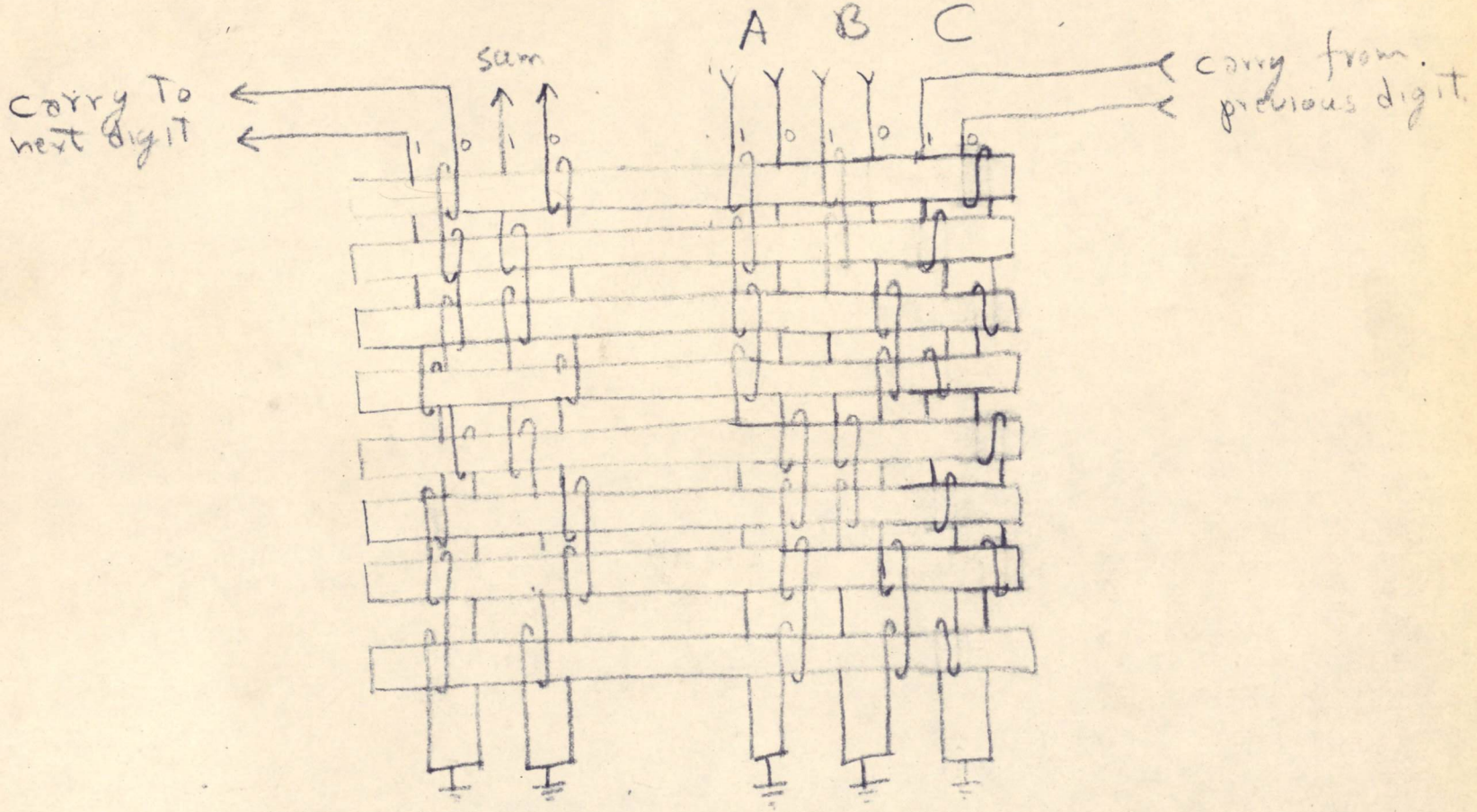
50919



8-POSITION MAGNETIC MATRIC SWITCH.



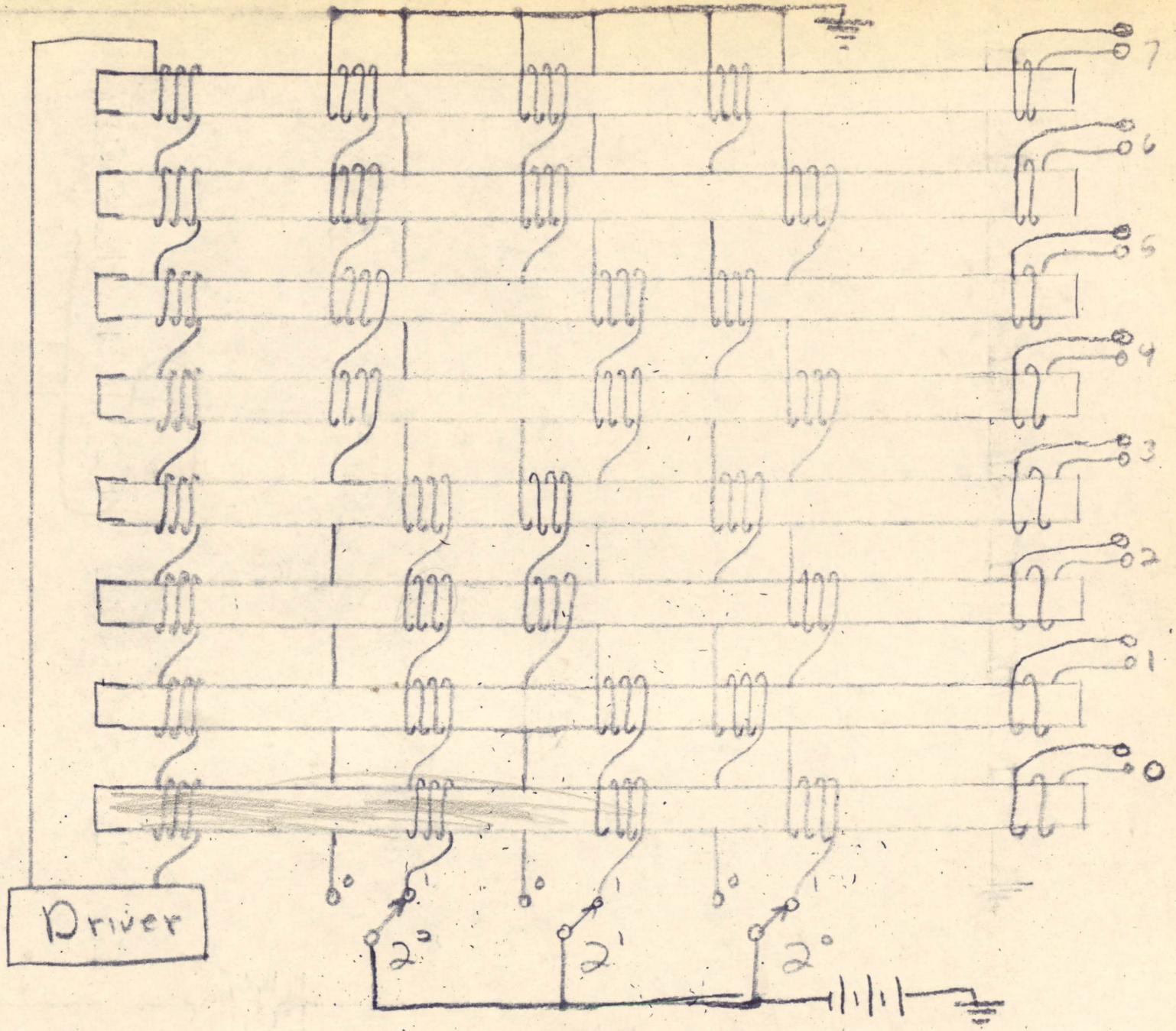
SINGLE DIGIT ADDER



Single Digit Adder

Fig 9

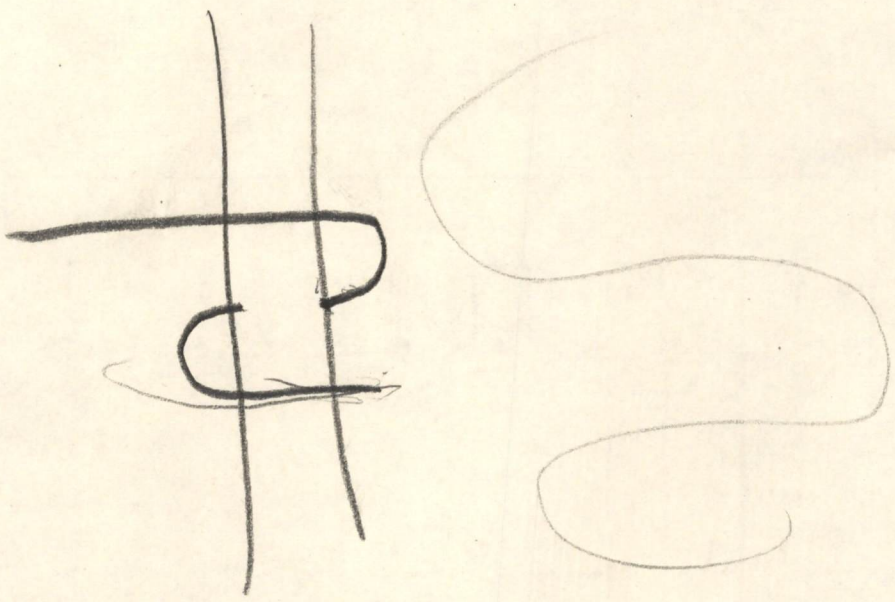
K Olsen 16 Feb 52

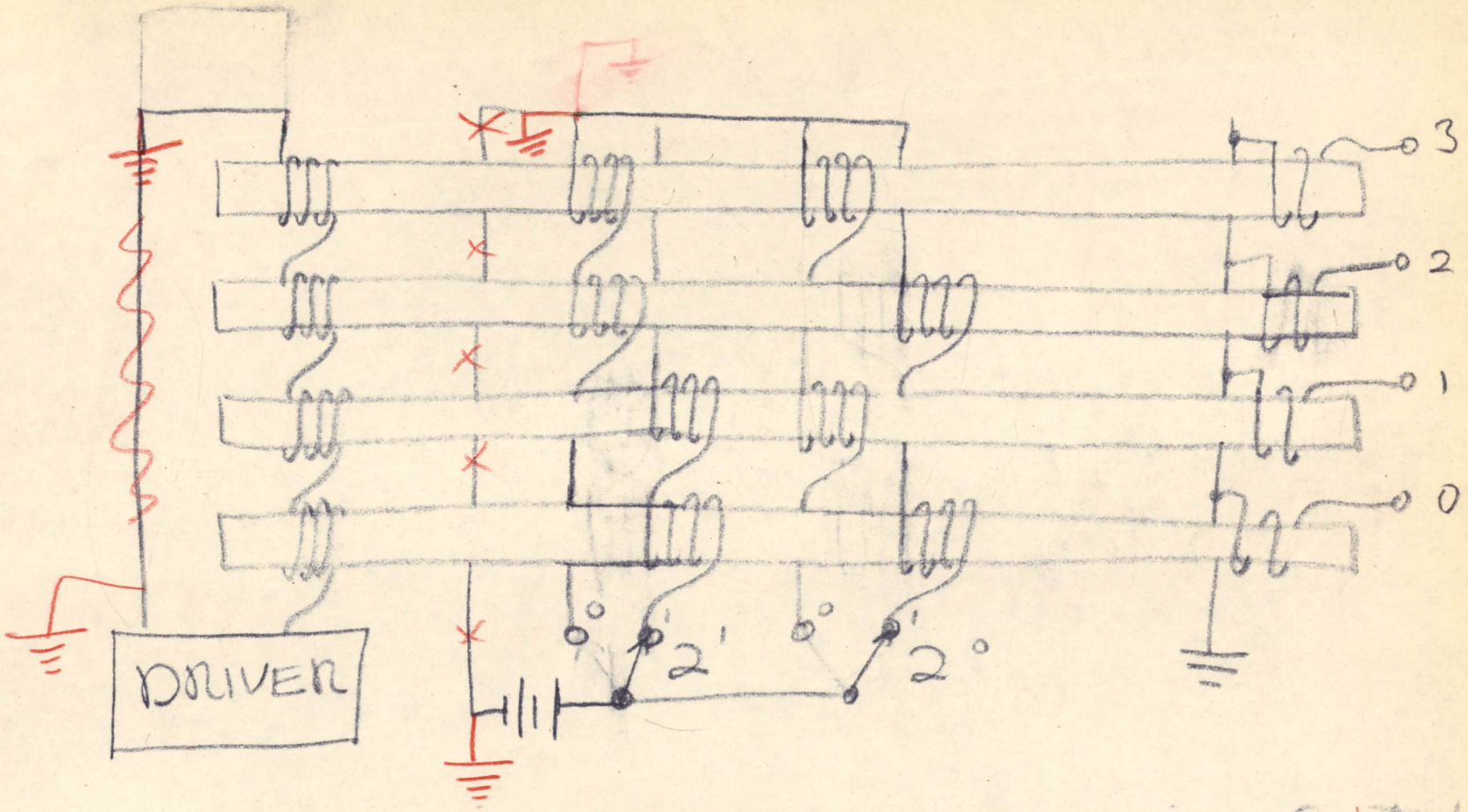


FEB 26 1952

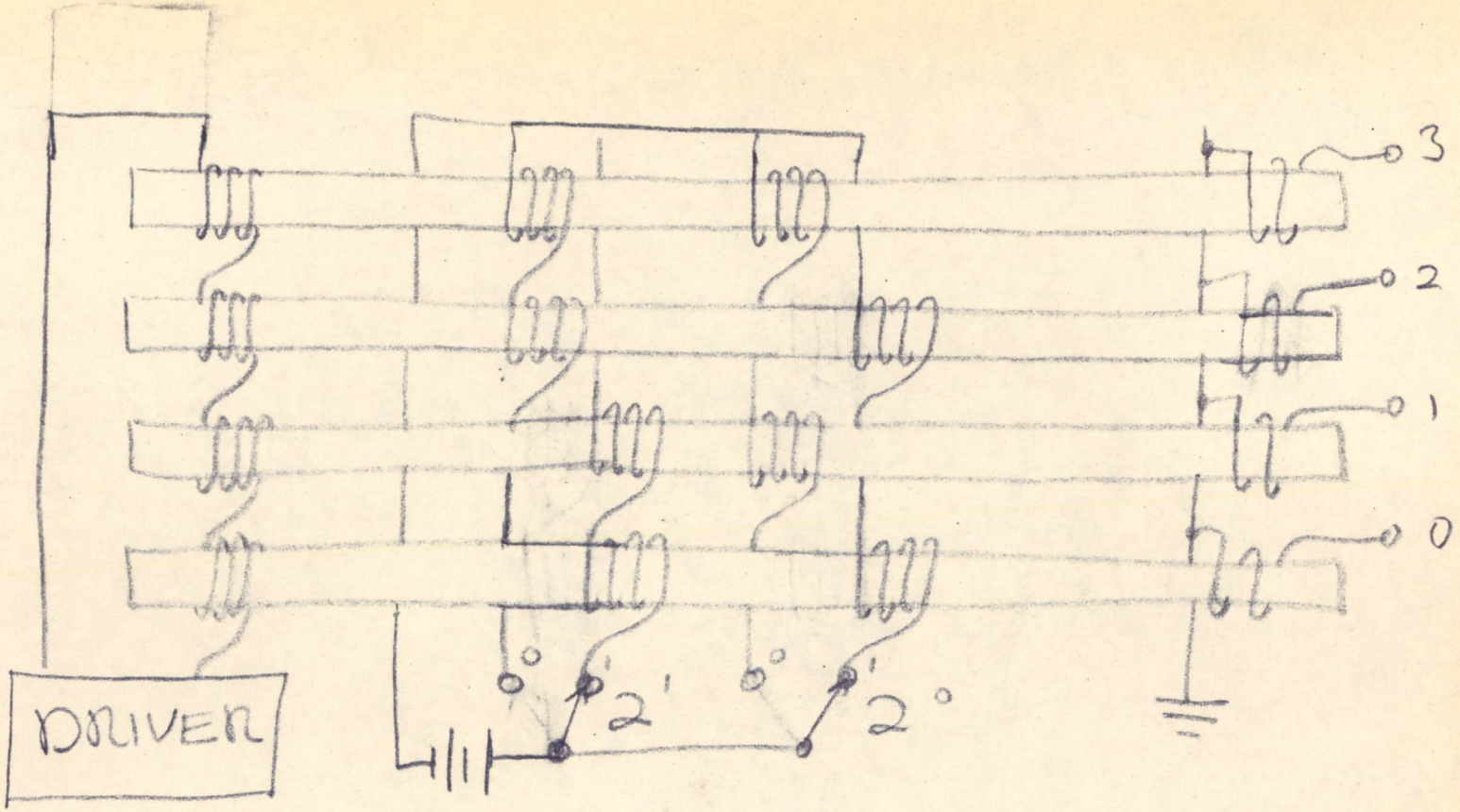
8-POSITION · Magnetic-Matrix Switch

K Olsen 25 Feb

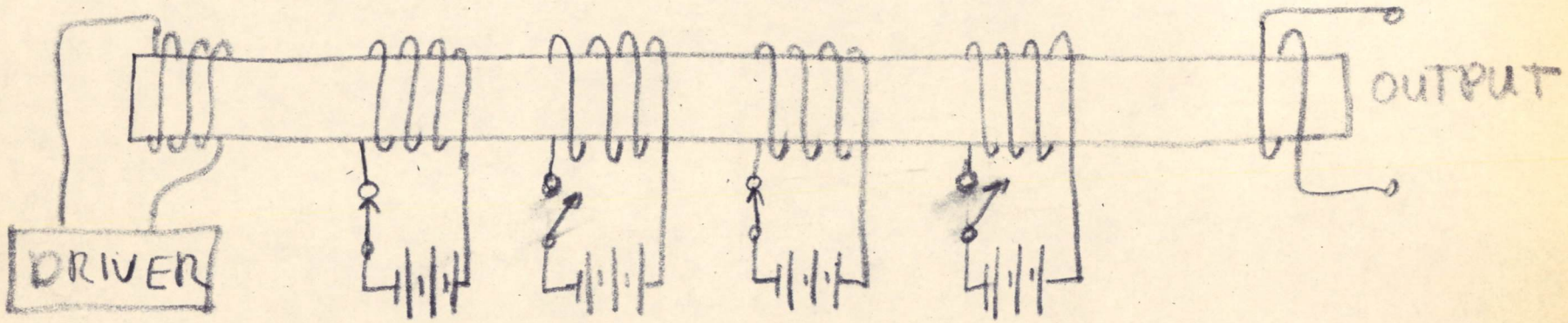




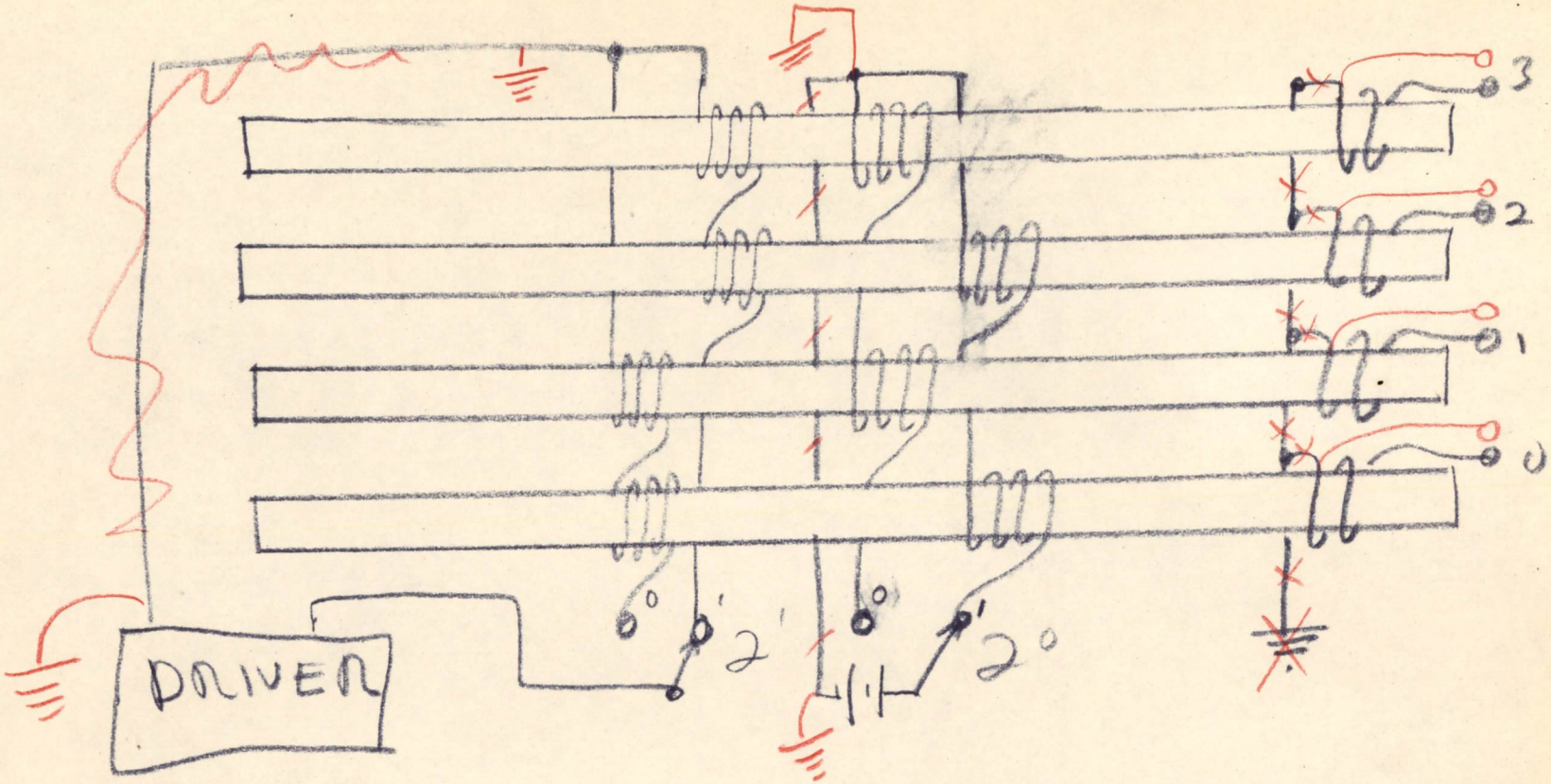
4-POSITION MAGNETIC-MATRIX SWITCH



4 POSITION MAGNEIC MATRIX Switch

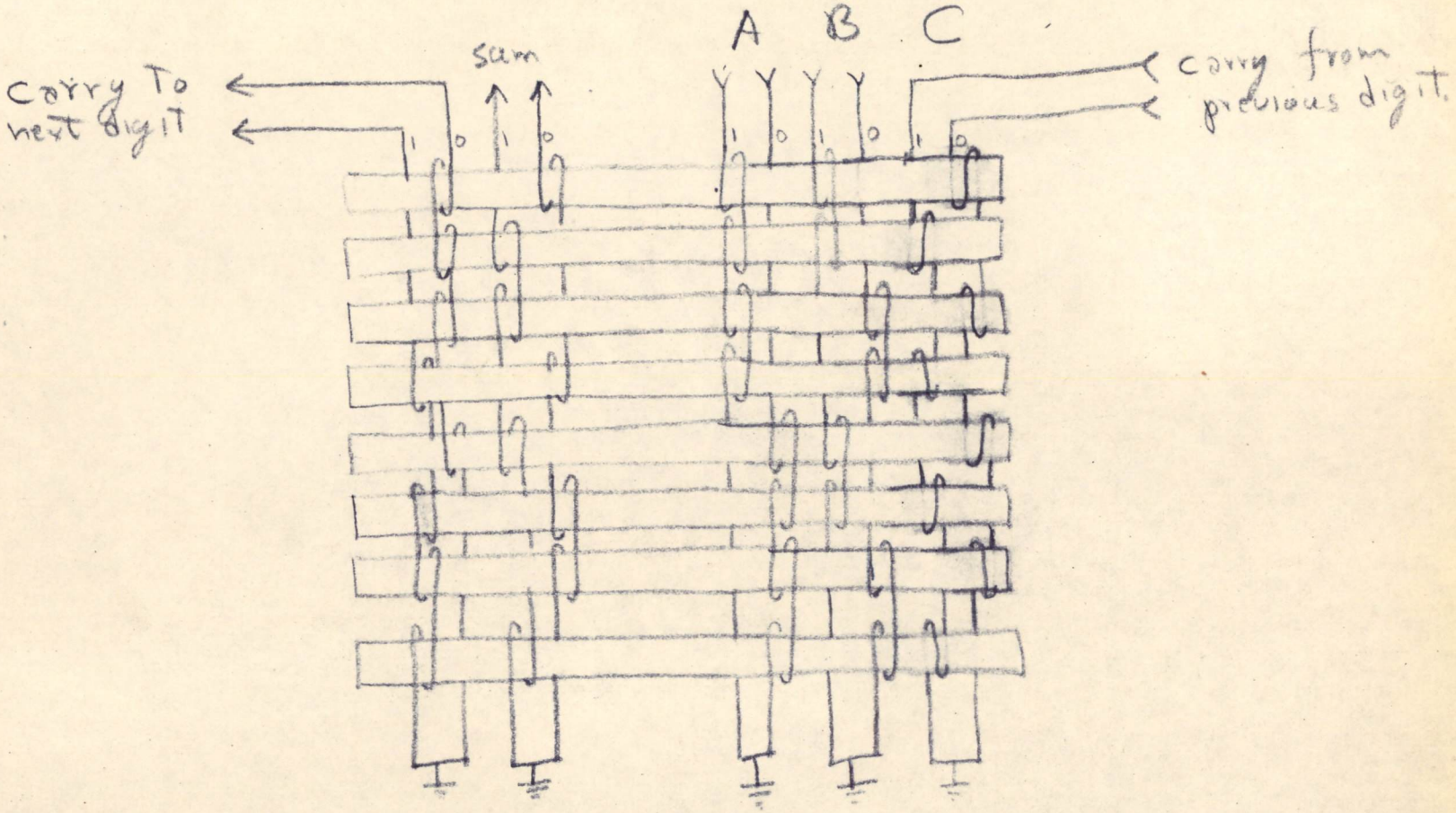


SATURABLE TRANSFORMER WITH SEVERAL CONTROL WINDINGS.



4-POSITION MAGNETIC-MATRIX SWITCH (alternate)

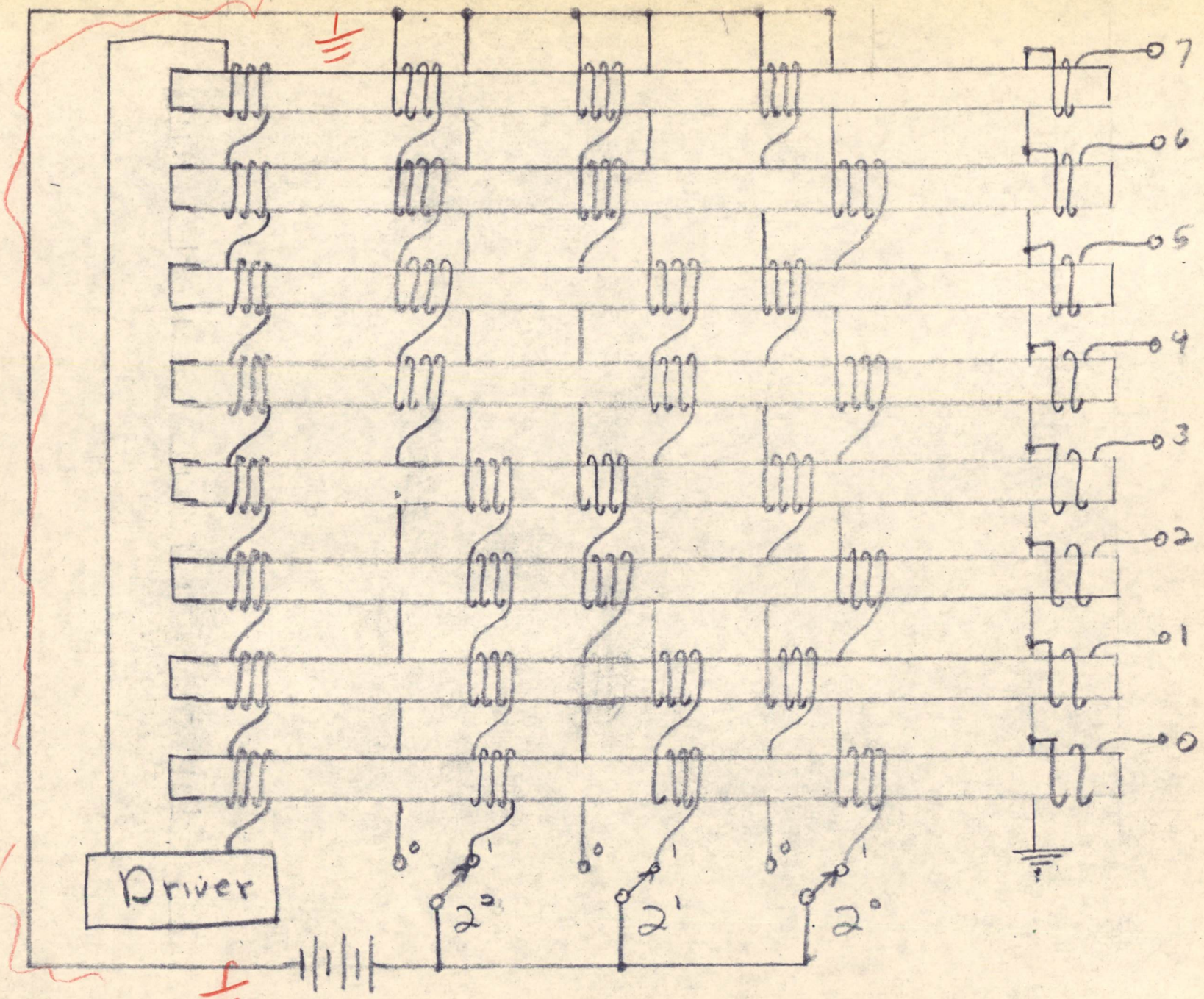
Kalan Feb 20



Single Digit Adder

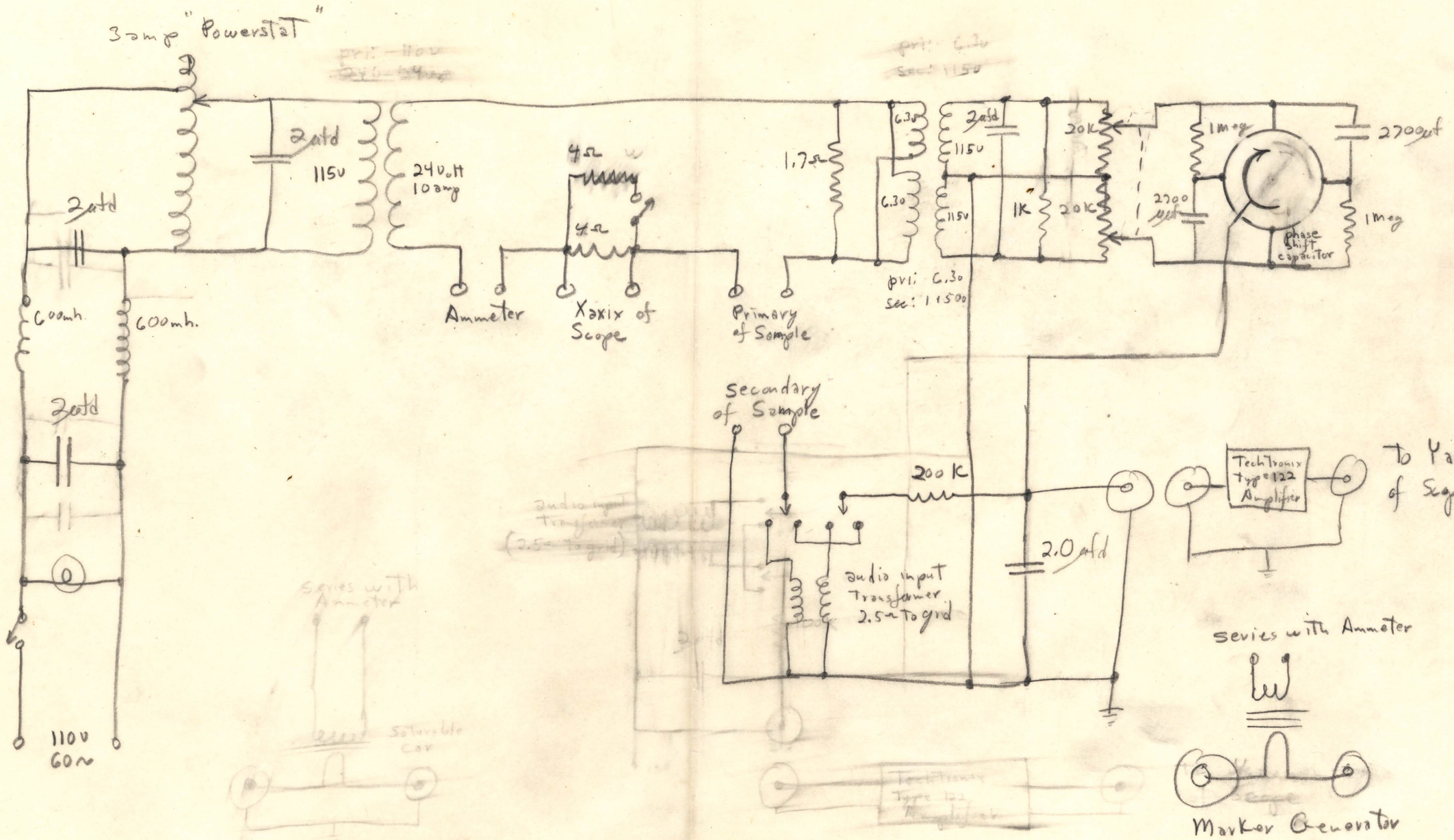
fig 9

L Olsen 16 Feb 52



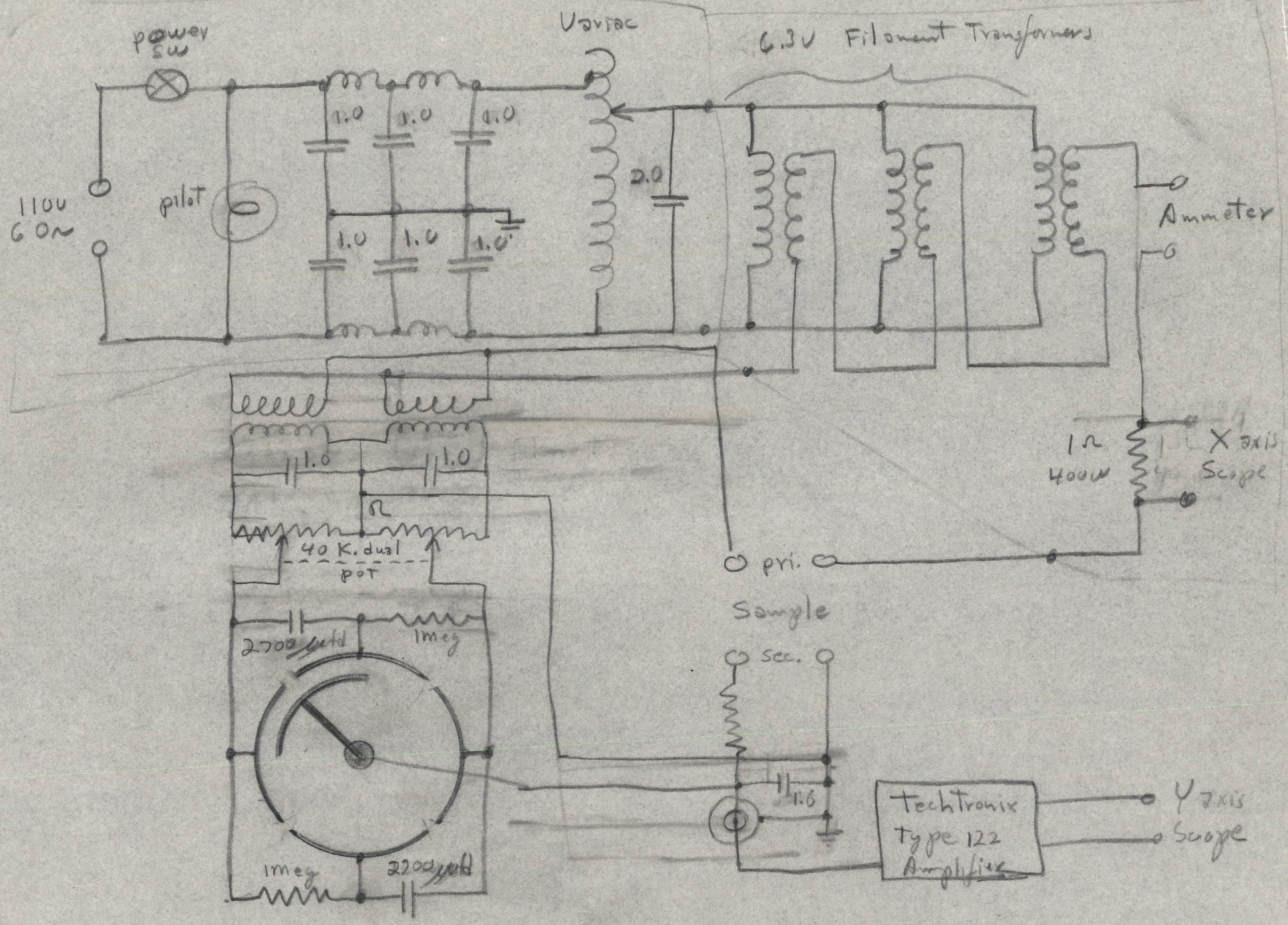
8-POSITION Magnetic-Matrix Switch

Olsen 25 Feb

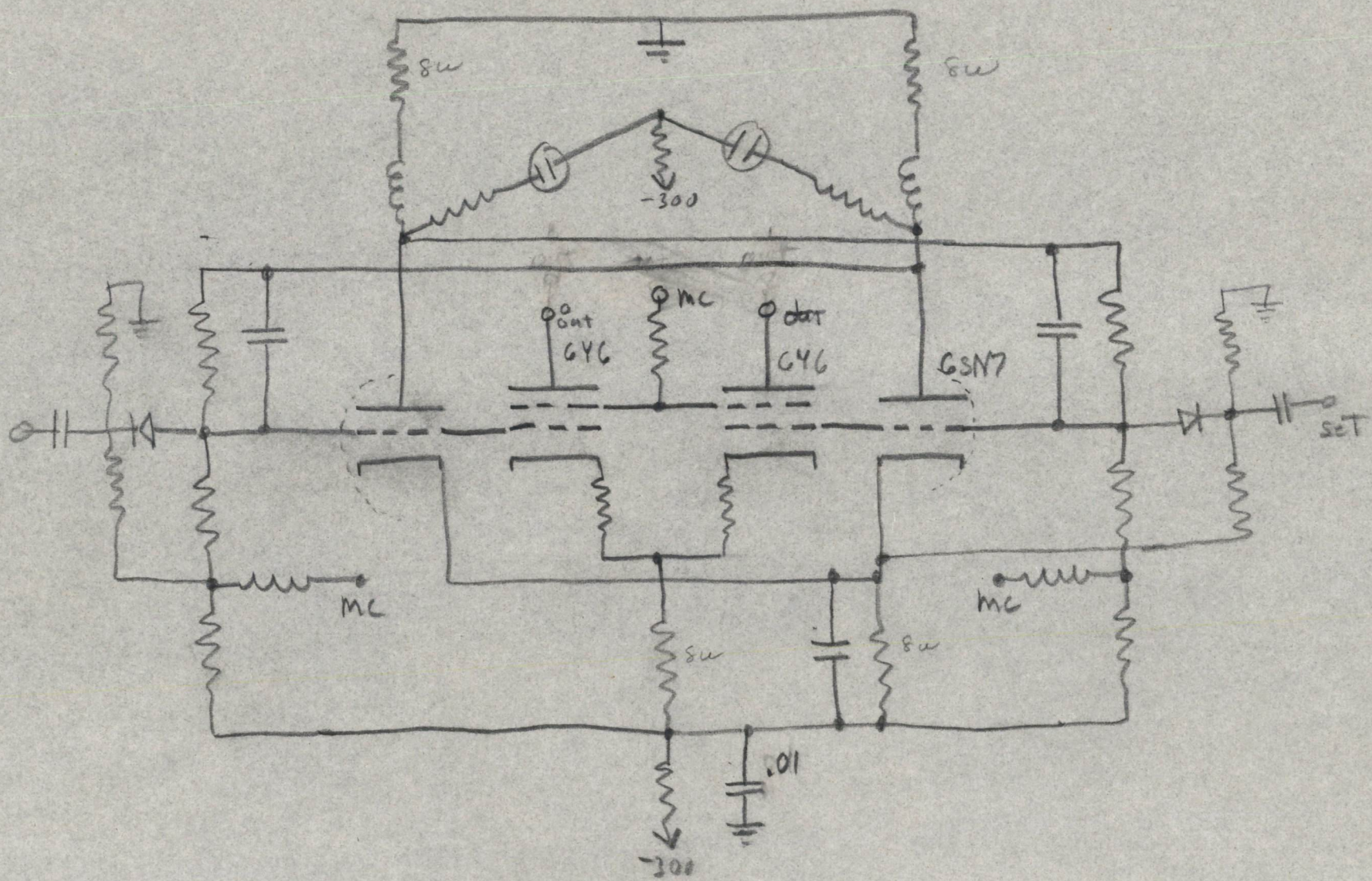


Flux-Current Plotter

19 Aug. 1952 K Oplan

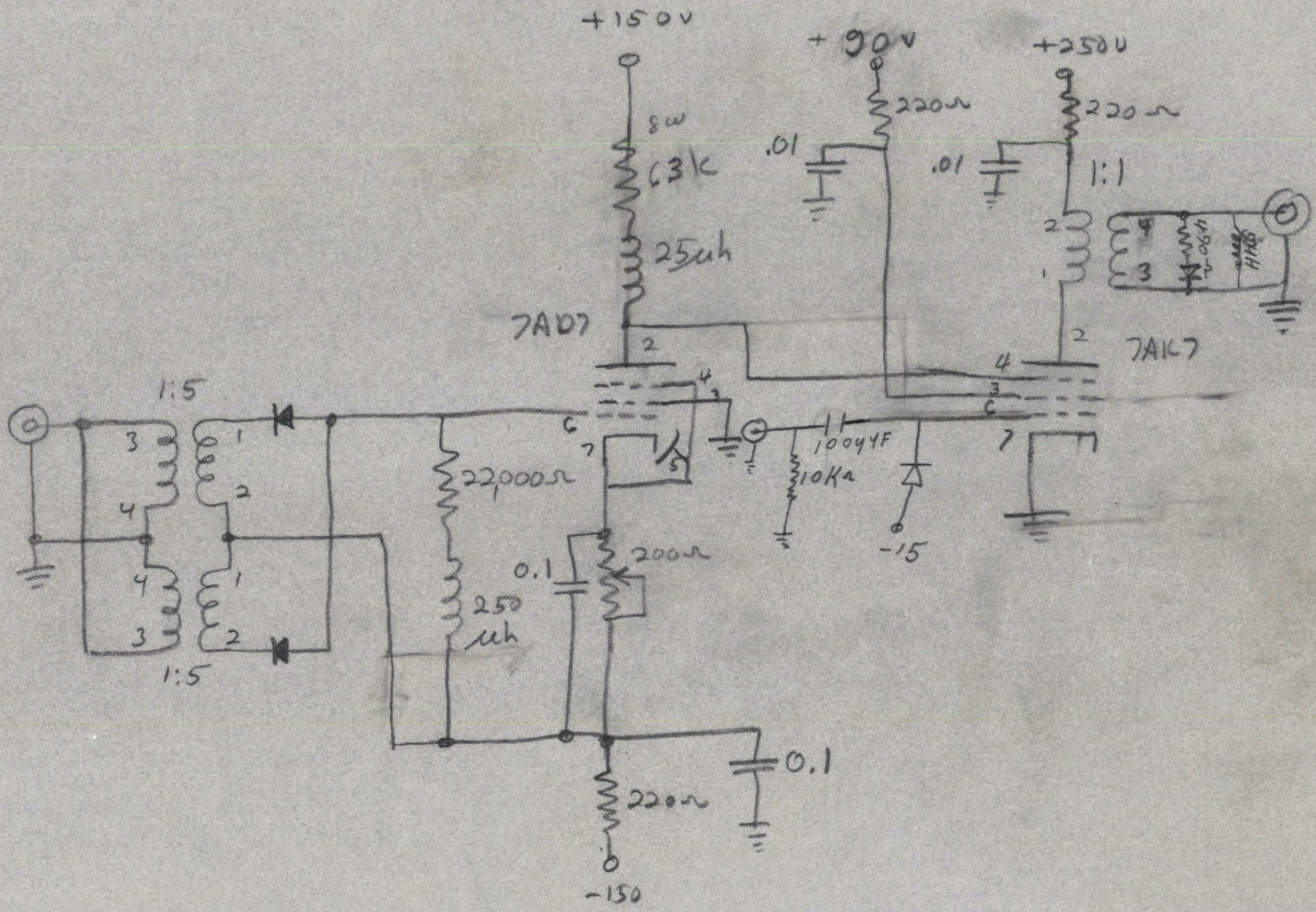


Flux-Current- Plotter 19 April 1952 K Olsen



Core Driving Flip-Flop

K Olsen 23 June '52



Circuit Schematic, Sensing Amplifier, Ceramic Array II

Kaiser May 19, 1952

Z Axis Driver

Memory Array

FF9

SENSING AMPLIFIER

X Switch

Y Switch

DISPLAY SCOPE

Z

Y

X

Decoder out

Decoder out

FF1

GT1

FF2

GT2

FF3

GT3

FF4

GT4

X Gated Driver Panel

Y Gated Driver Panel

Skip circuit

Skip circuit

GT 9

GT 10

S3

DE 7

FF8

GT8

FF7

GT7

FF6

GT6

FF5

GT5

Read

Bias

Write

Read

Bias

Write

MIXER

light gun

MIXER

pulse Generator

push button pulse gen.

S2

pulse generator

DE1

pulse distributer

DE 2

FF10

FF 11

FF 12

FF 13

DE 4

DE 3

DE 5

DE 6

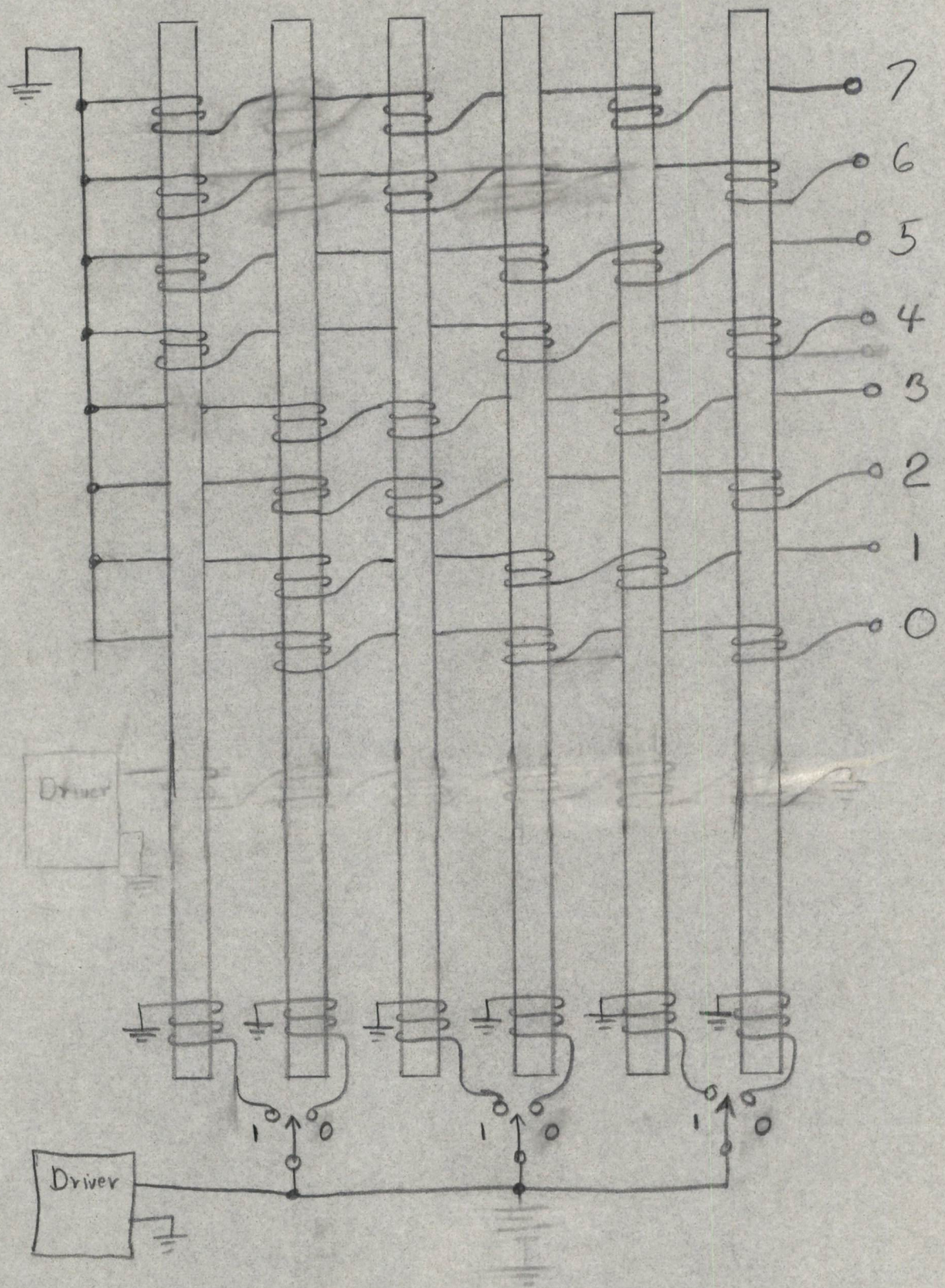
SYNC SCOPE

DE

S1

Block Diagram. Ceramic Memory Array II

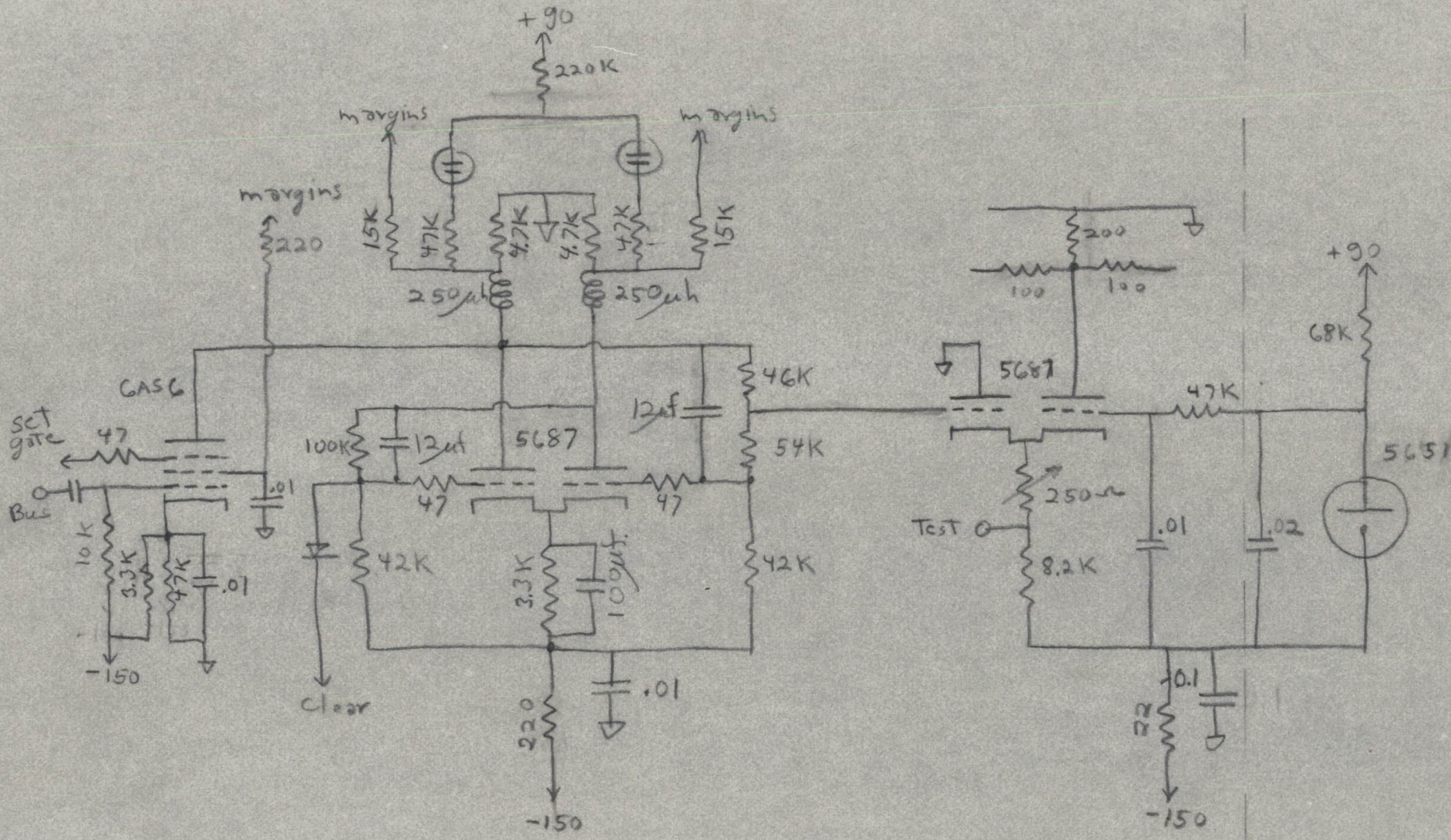
Koken 4 April 1952



Magnetic Matrix Switch II

(Alternate)

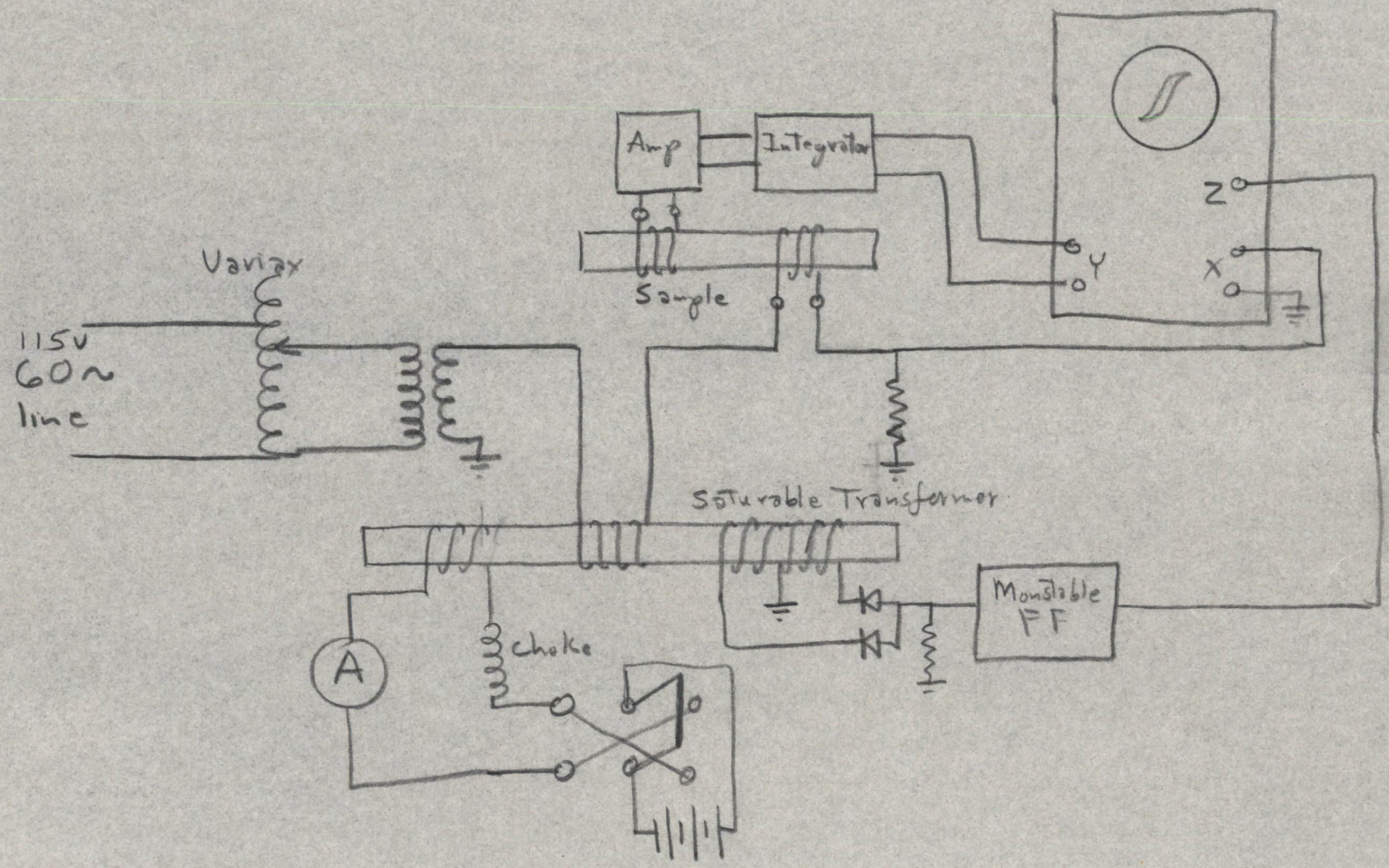
K. Olsen Ap. 4, 1952



D.C. Decoder #4

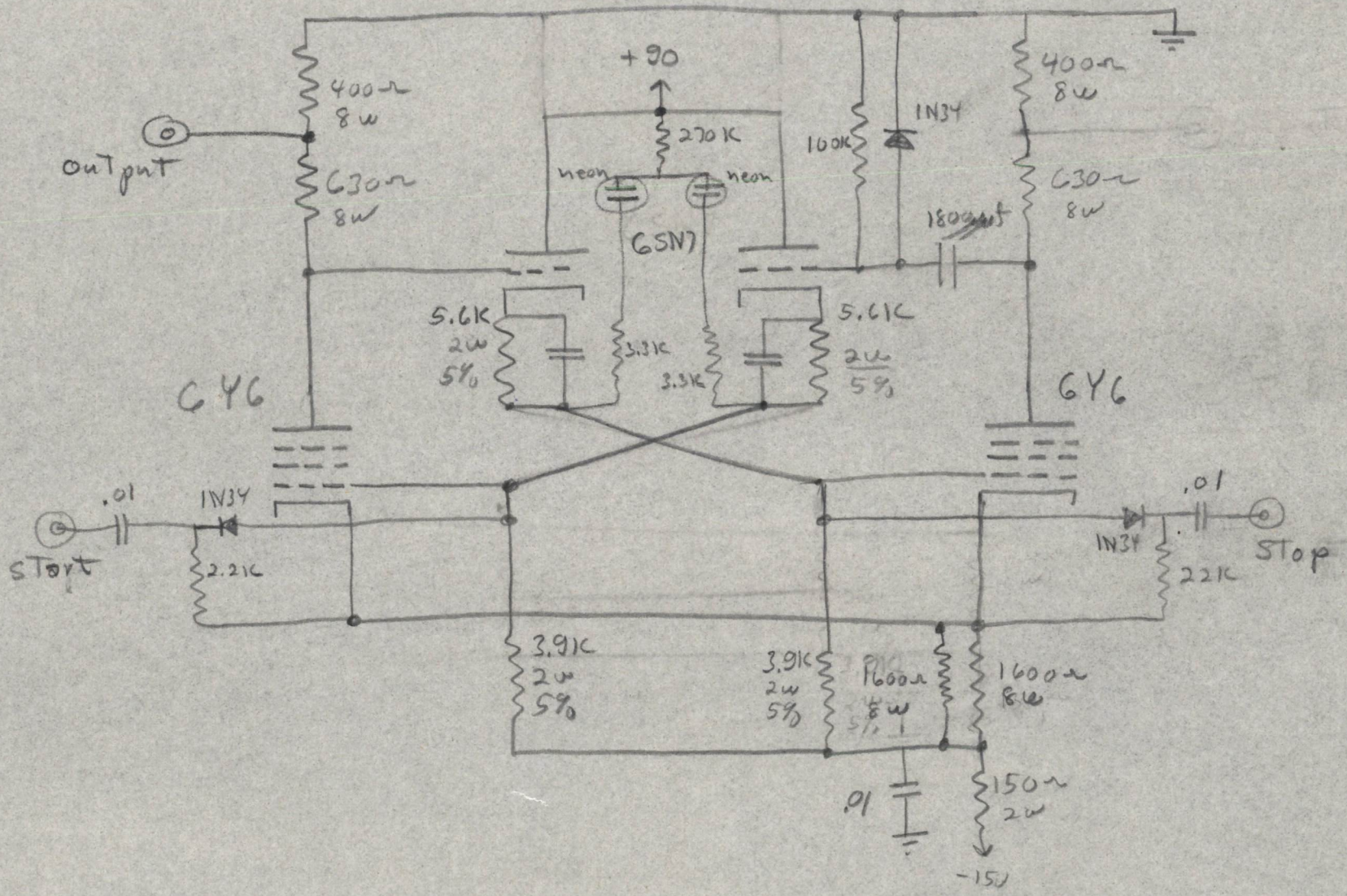
K.H.O.

1 March 51



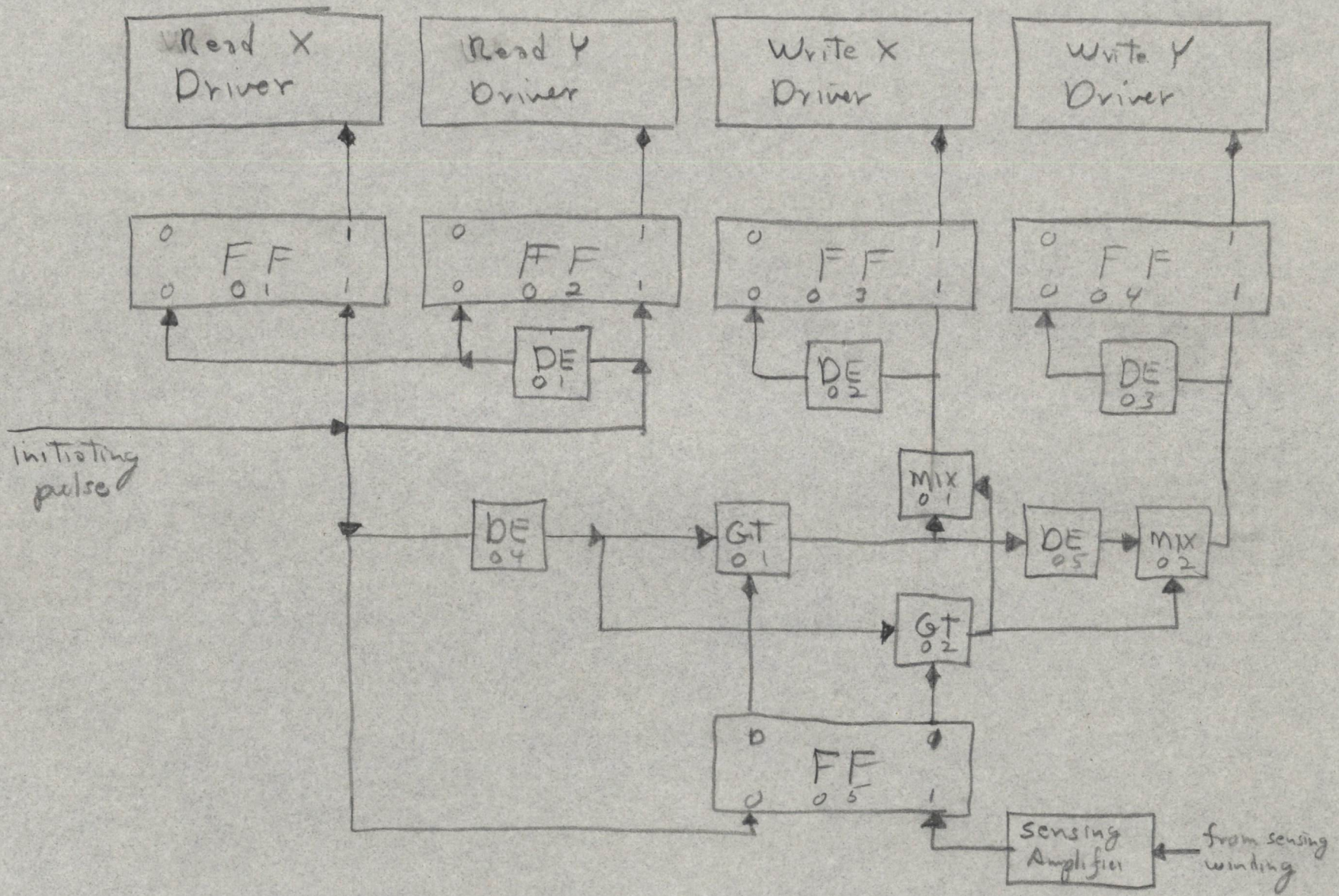
Calibrated Flux-Current Plotter

K Olsen Aug. 4 1952



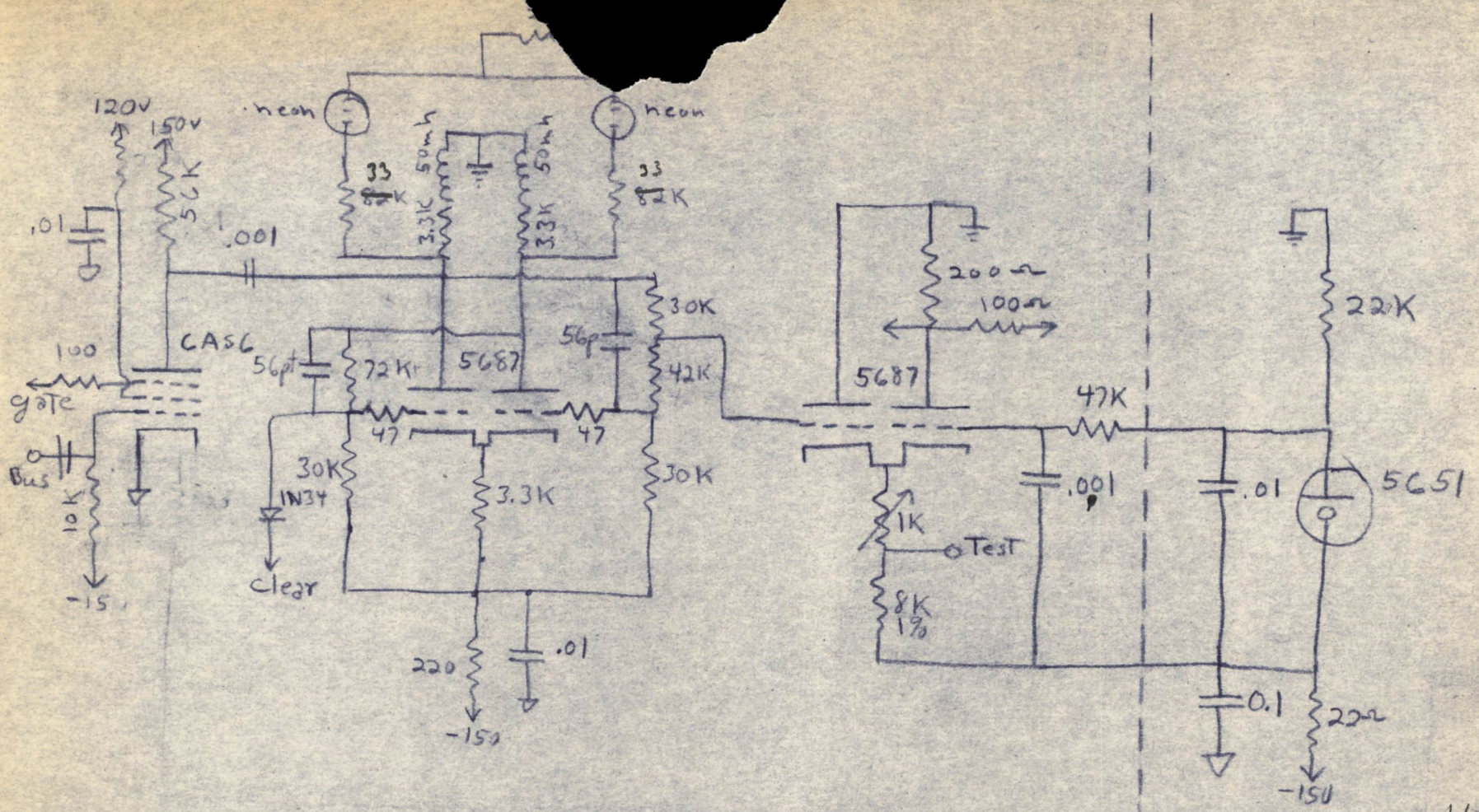
Monostable Flip-Flop.

Kaiser



Scheme for Writing "ZERO"
Without a "Z" Winding

Kaiser
April 4 '52

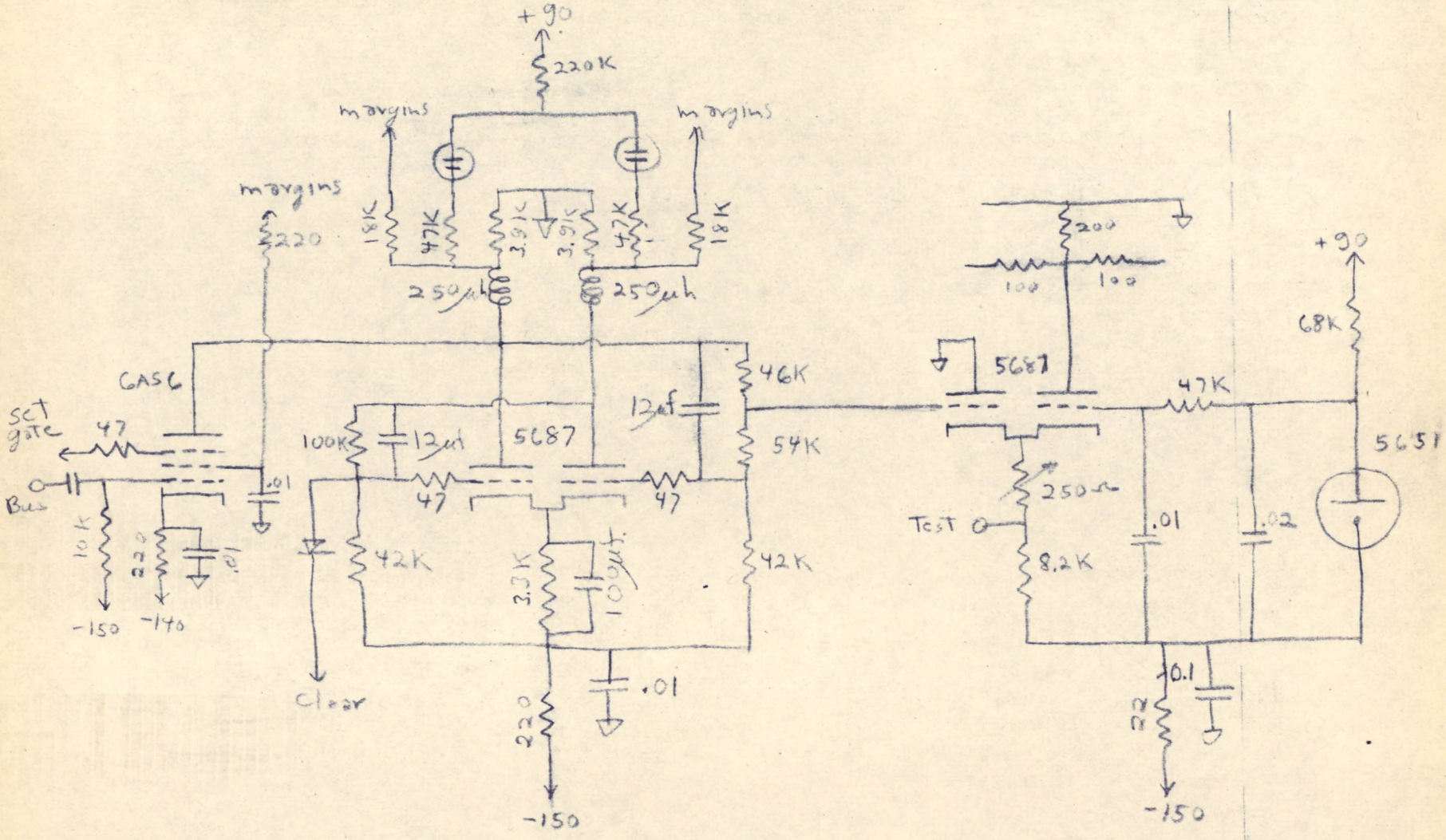


#1

DC Decoder

K.H.O.

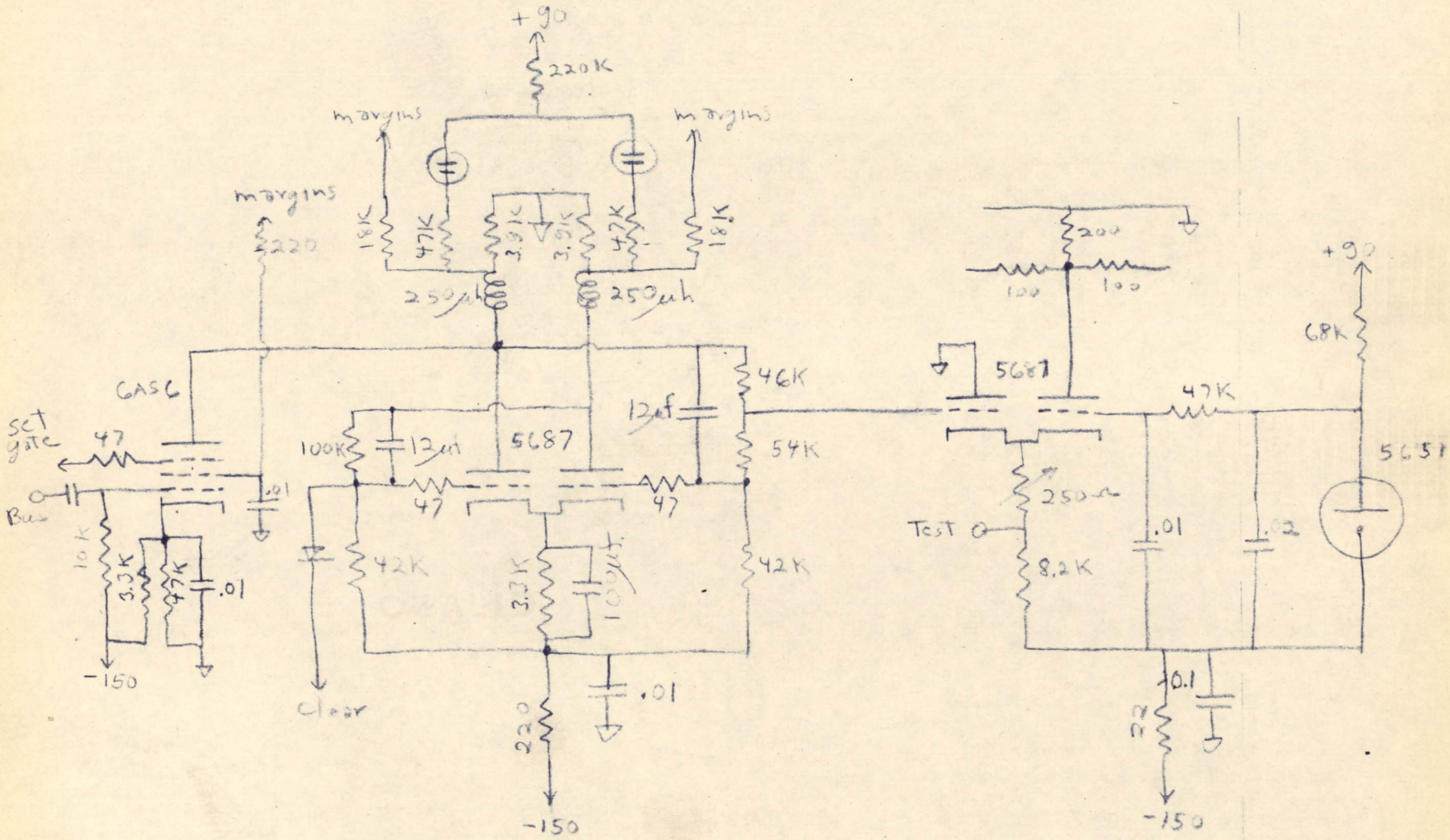
21 Feb '51



D.C. Decoder #2

K.H.O.

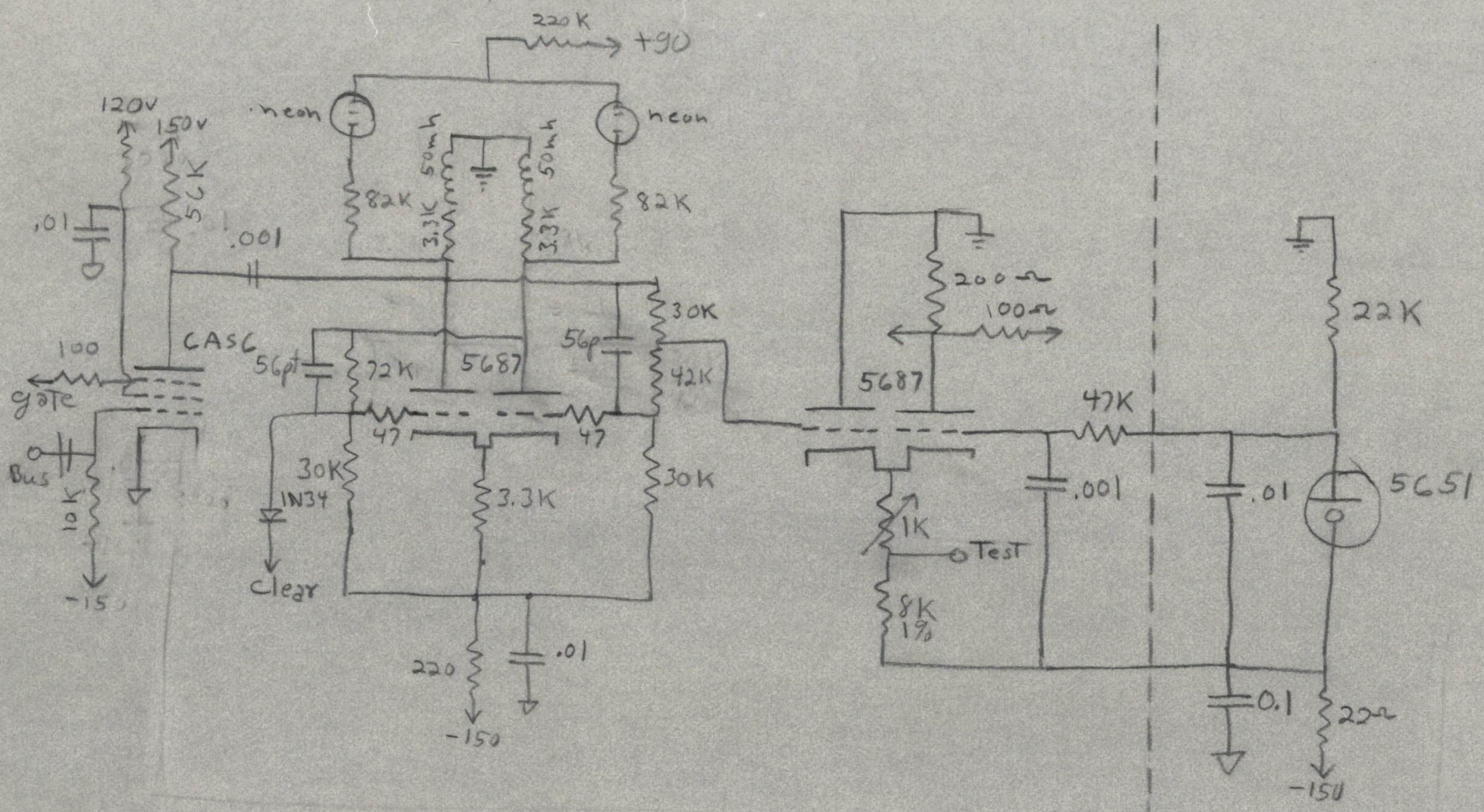
28 Feb 51



D.C. Decoder #3

K.H.O.

1 March 51

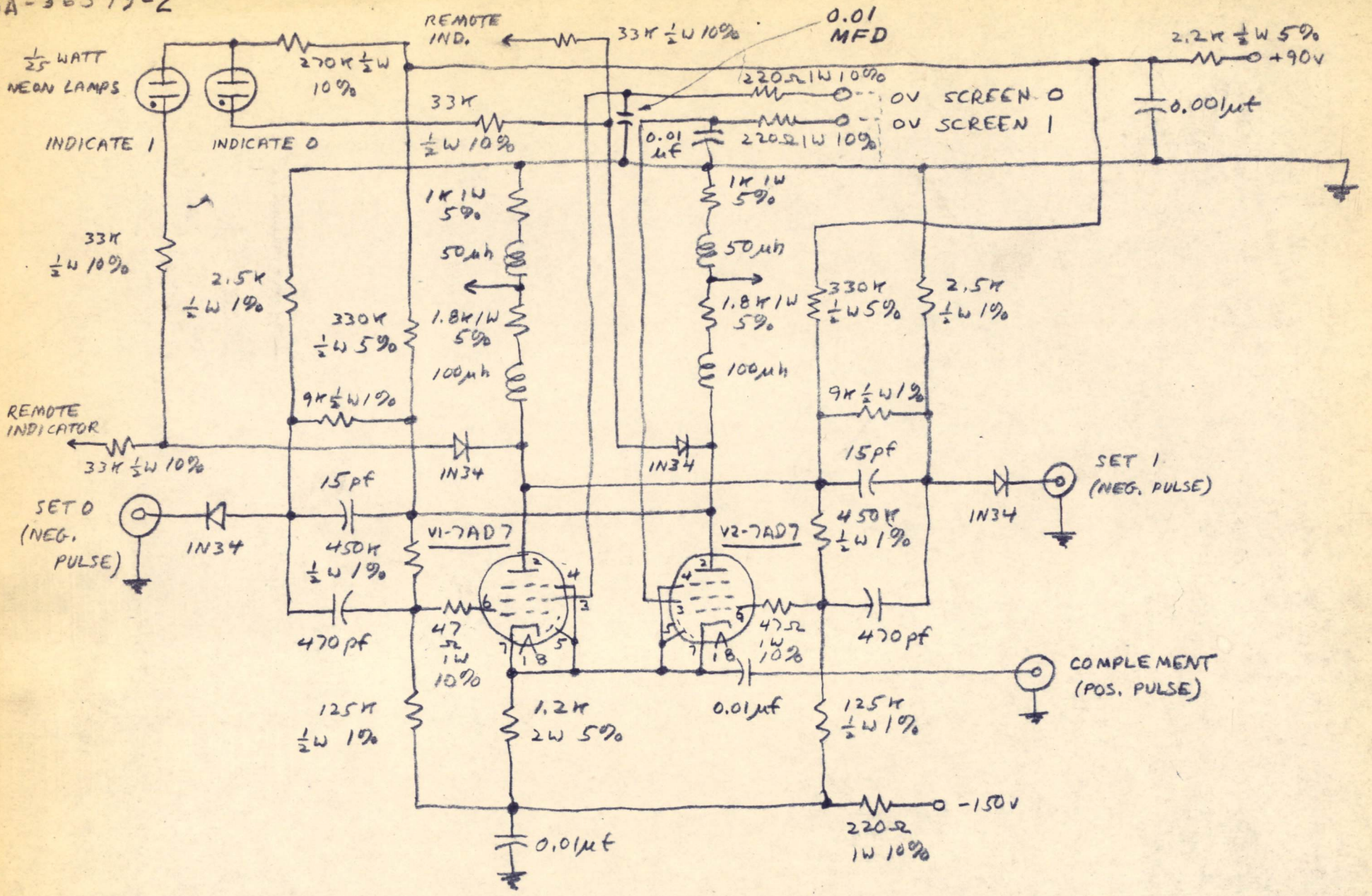


DC Decoder #2

K.H.O.

21 Feb '51

SA-36579-2

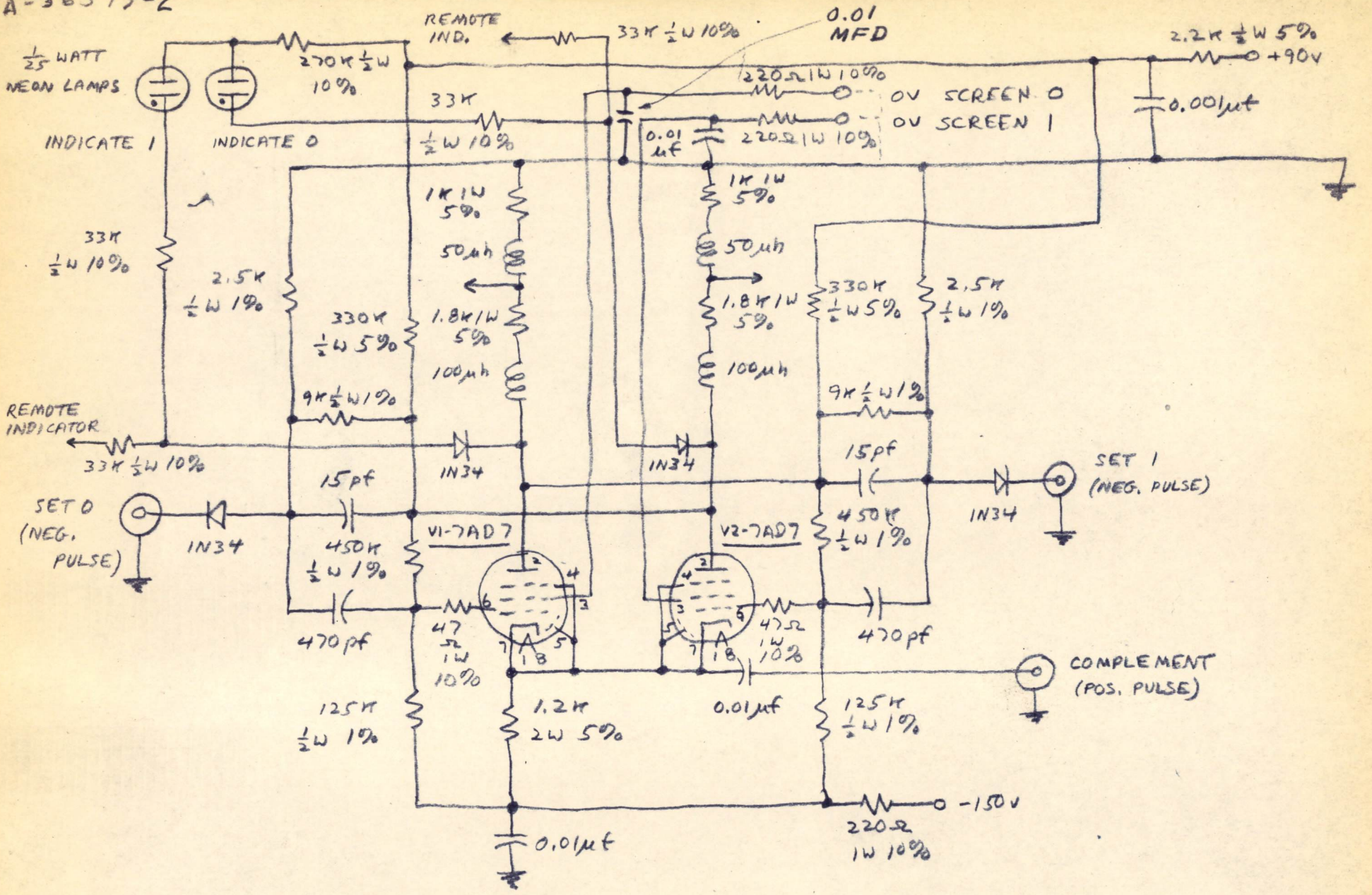


APR 24 1951

7AD7 D-C FLIP FLOP D-C COUPLED TO ITS LOAD

MASSACHUSETTS INSTITUTE OF TECHNOLOGY SERVOMECHANISMS LABORATORY		
DIC NO. 6345	DR. R Best	CK.
ENG. R Best	SA-36579-2	

SA-36579-2

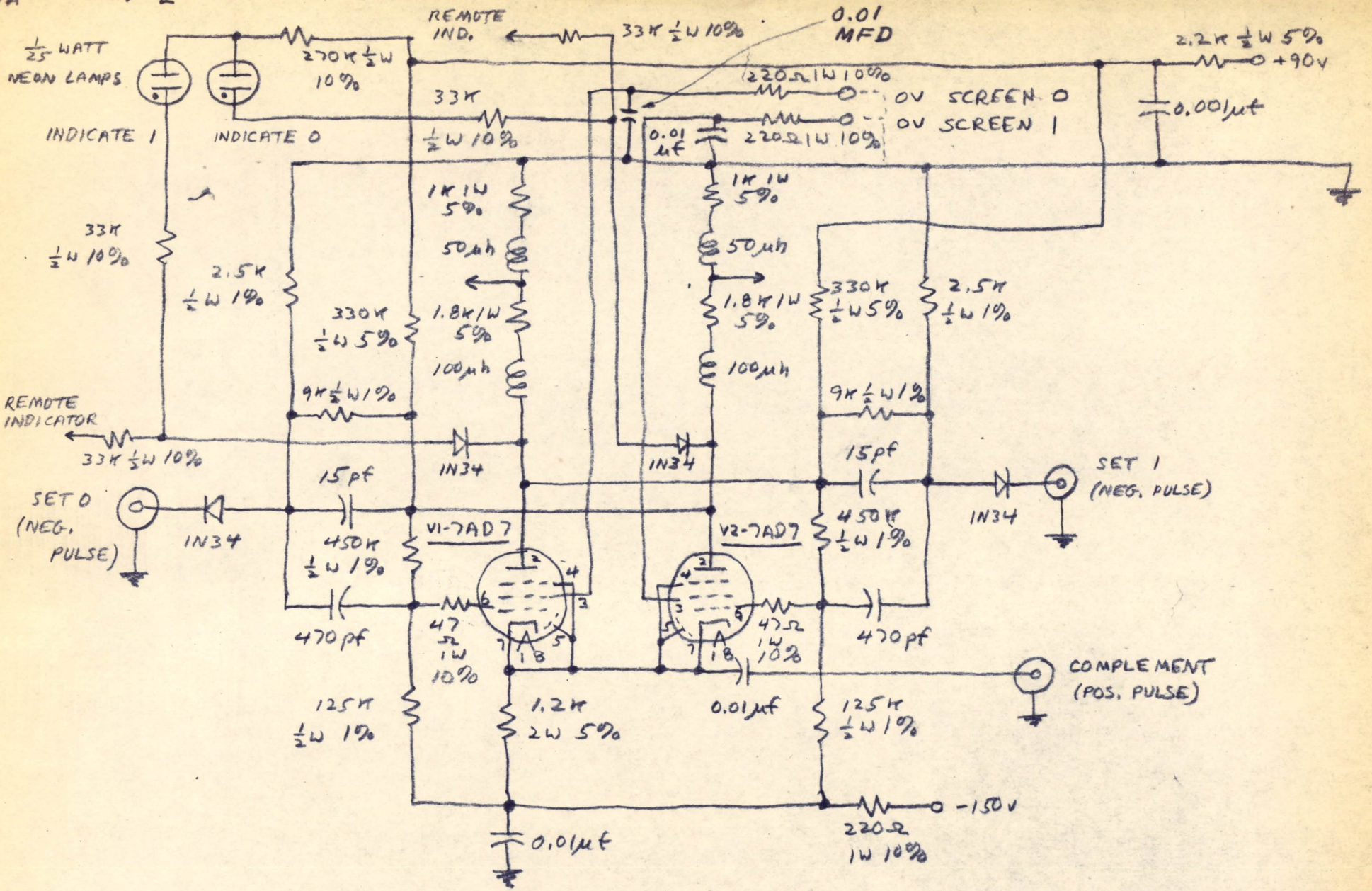


7AD7 D-C FLIP FLOP D-C COUPLED TO ITS LOAD

APR 24 1951

MASSACHUSETTS INSTITUTE OF TECHNOLOGY SERVOMECHANISMS LABORATORY		
DIC NO. 6345	DR. R Best	CK.
ENG. R Best	SA-36579-2	

SA-36579-2



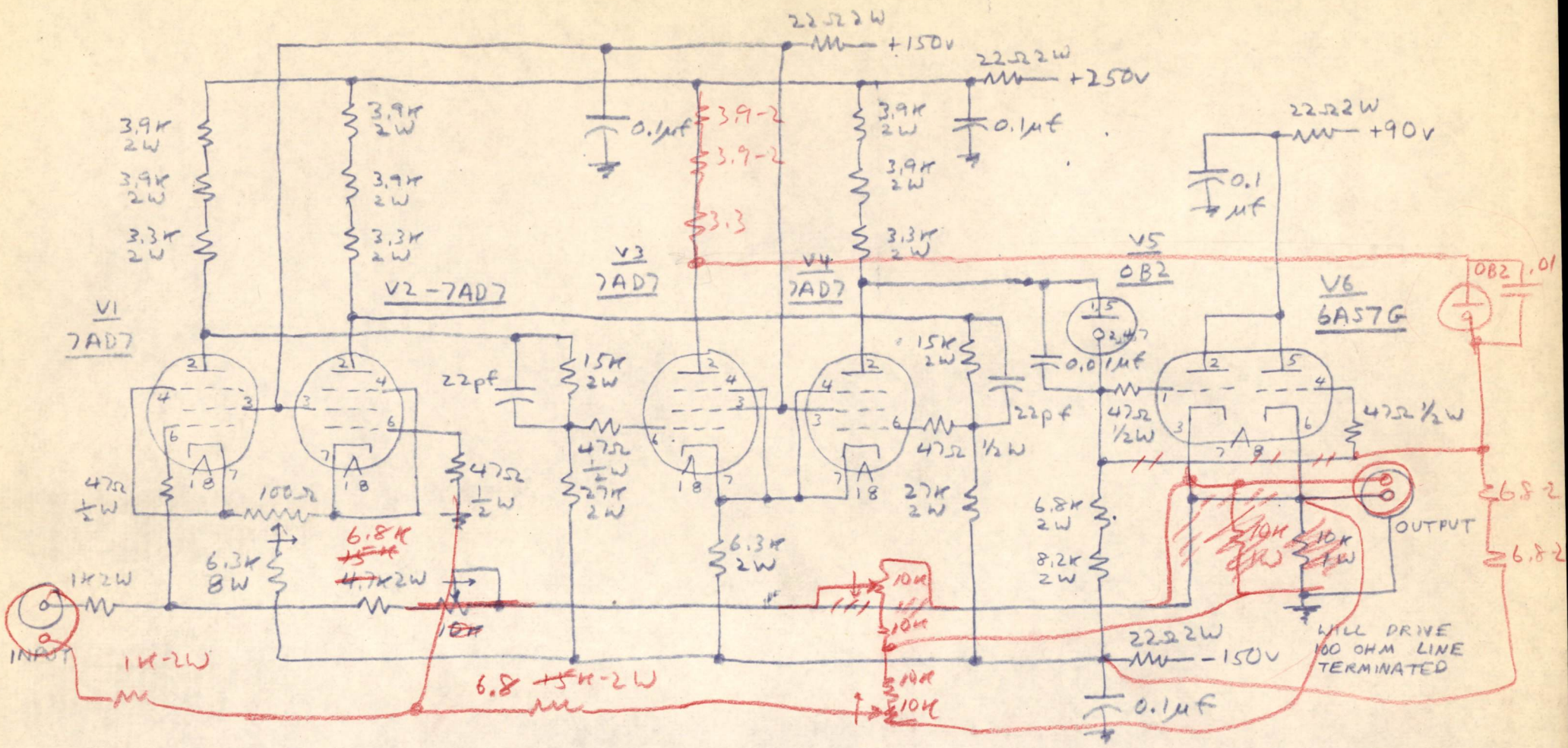
7AD7 D-C FLIP FLOP D-C COUPLED TO ITS LOAD

APR 24 1951

MASSACHUSETTS INSTITUTE OF TECHNOLOGY SERVOMECHANISMS LABORATORY		
DIC NO. 6345	DR. R Best	CK.
ENG. R Best	SA-36579-2	

SA-36905

DECODER OUTPUT AMPLIFIER

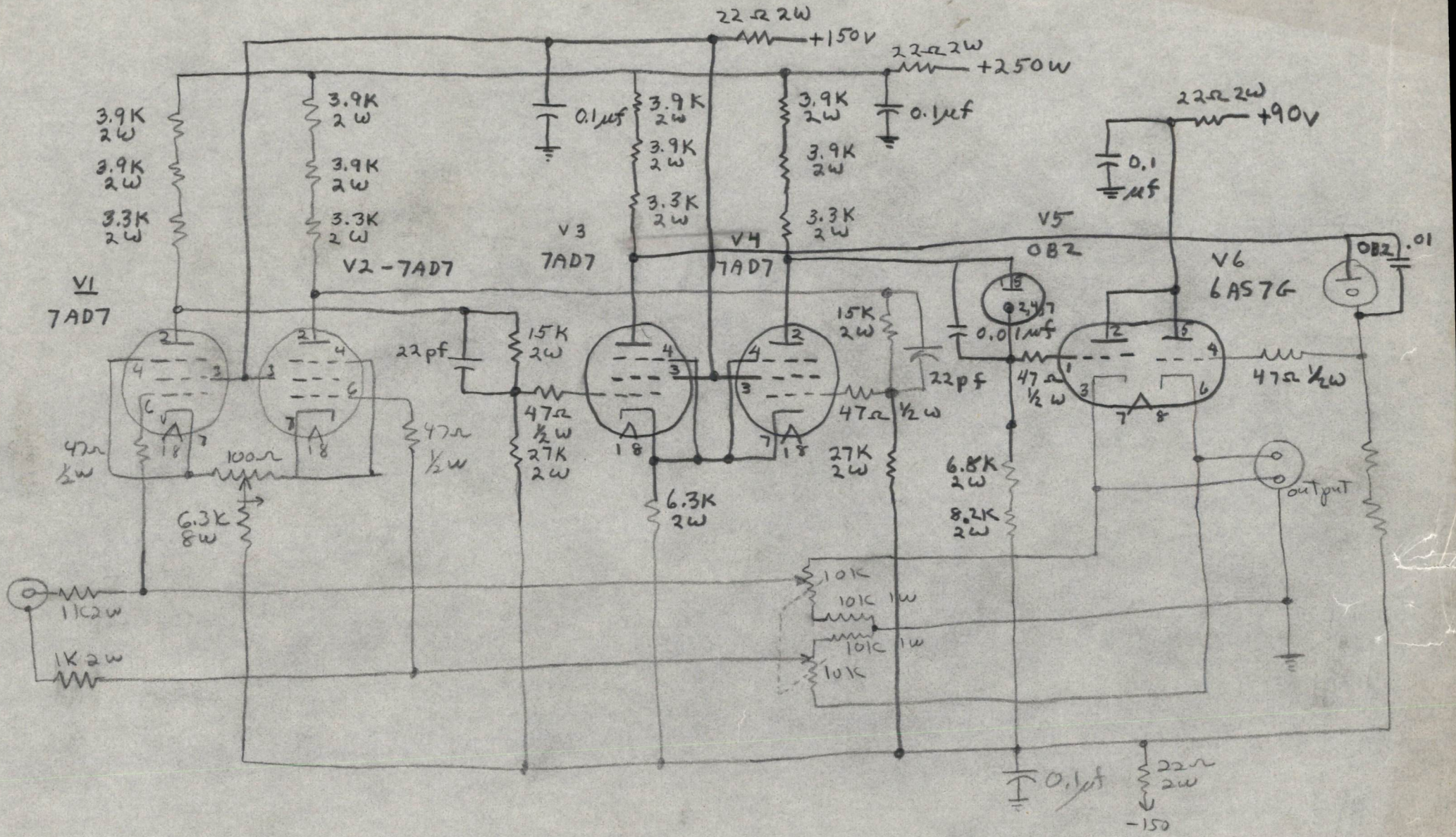


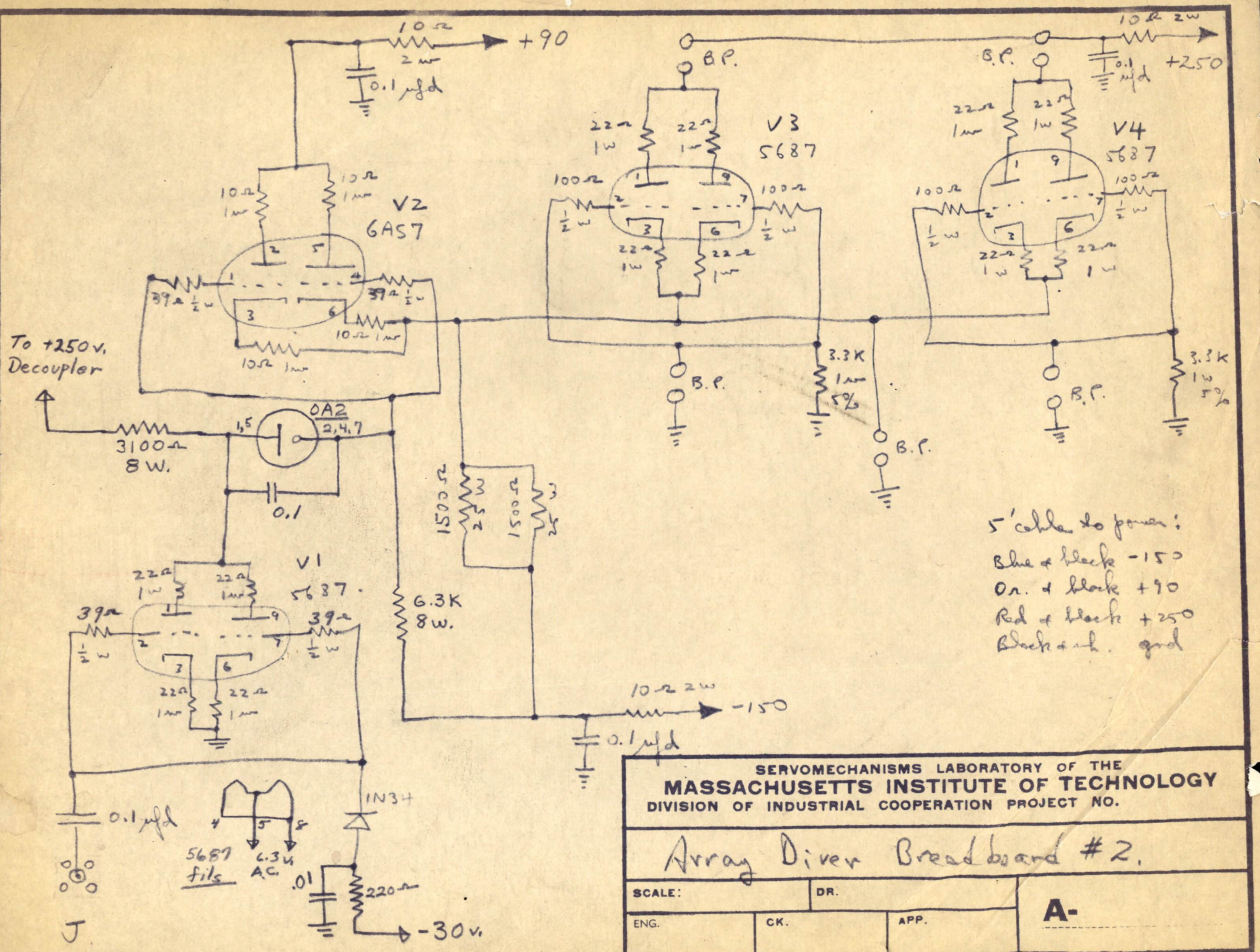
100 OHM POT. SHOULD BE VARIED SO THAT OUTPUT IS +2 VOLTS WHEN THE INPUT IS GROUNDED.
10K POT. " " " " " " " +22 VOLTS " " " " AT ITS MOST NEGATIVE VOLTAGE.

PRINT ISSUED
MAR 17 1953

MASSACHUSETTS INSTITUTE OF TECHNOLOGY SERVOMECHANISMS LABORATORY		
DIC NO. 6345	DR. R Best	CK. —
ENG. R Best	SA-36905	

MTC DECODER OUTPUT AMPLIFIER





D-50058-1

SECTIONS 2 THRU 10 ARE IDENTICAL WITH SECTION 1 EXCEPT FOR COMPONENT NUMBERS

R2 IS A 100Ω, W-W, IRC, ±1% RESISTOR IN SECTION 10 ONLY (R2-10)

SECTION 1

FROM BUS — J1-1 — P100 (5), P100 (19)

TO CHECK BUS — J2-1 — (1) E2, (4) P100

P1-1 — FF (SET 1) — (7) P100

P2-1 — E1 (4), P100 (19), P100 (7), E3 (3), P100 (3)

(2) P100, (1) E3, (23) P100, (3) E1

RG-1 0.4 MEG ±1%

R7-1 220Ω ½W

(1) FF OUTPUT

(0) FF PLATE

P3-1 — (0) FF OUTPUT — (19) P100, E4 (3)

(1) E4, (22) P100

R1-1 100Ω, W-W, IRC ±1%

R2-1 200Ω W-W, IRC ±1%

R3-1 5000Ω W-W, IRC ±1%

R4-1 5000Ω W-W, IRC ±1% — CW — R5-1 100Ω W-W, IRC, 2W

TEST POINT (RED)

SECTION 0

FROM BUS — J1-0 — P100 (5), P100 (19)

TO CHECK BUS — J2-0 — (1) E2, (4) P100

P1-0 — FF (SET 1) — (7) P100

GATE PLUG-IN UNIT SECTION (B-36958)

J100 — READ TO CHECK BUS

J101 — READ IN

J102 — CLEAR

P2-0 — E1 (2), P100 (19), P100 (7), E3 (3), P100 (3)

(2) P100 FF SCR (0), (1) E3, (23) P100, (1) E1

RG-0 0.4 MEG ±1%

R7-0 220Ω ½W

(1) FF OUTPUT

(1) FF PLATE

D-C FLIP FLOP PLUG-IN UNIT SECTION (C-36957)

P3-0 — P100 (19) — (1) E4, (22) P100

E4 (3)

SWITCH TUBE PLUG-IN UNIT SECTION (B-36959)

R1-0 100Ω W-W, IRC ±1%

R2-0 200Ω W-W, IRC ±1%

R3-0 5000Ω W-W, IRC ±1%

R4-0 5000Ω W-W, IRC ±1% — CW — R5-0 100Ω W-W IRC, 2W

TEST POINT (RED)

-150V (REFERENCE VOLTAGE)

J103 — COMPLEMENT

J104 — OUTPUT

C103 0.1 MFD

P100 (20)

R100 0.27 MEG

TEST POINT (RED)

REF. VOLTAGE

R101 0.27 MEG

C100-A 0.1 MFD

C100-B 0.1 MFD

R102 33,000Ω ±5%

R103 0.47 MEG ±5%

R104 1000Ω W-W, 2W — CW

R105 5000Ω ±1%, W-W

R106 5000Ω ±1%, W-W

TEST POINT (BLACK)

P100 (5)

C102 0.01 MFD

R108 220Ω

R109 82,000Ω ±1%

V100 7AD7

V101 5651

R107 2.2 MEG ½W

C101 0.01 MFD

E1

P2-0 (22), P2-0 (3) — FF-0

P2-1 (22), P2-1 (3) — FF-1

P2-2 (22), P2-2 (3) — FF-2

P2-3 (22), P2-3 (3) — FF-3

P2-4 (22), P2-4 (3) — FF-4

P2-5 (22), P2-5 (3) — FF-5

P2-6 (22), P2-6 (3) — FF-6

P2-7 (22), P2-7 (3) — FF-7

P2-8 (22), P2-8 (3) — FF-8

P2-9 (22), P2-9 (3) — FF-9

P2-10 (22), P2-10 (3) — FF-10

(E1 CONSISTS OF A 10 TERMINAL & 12 TERMINAL JONES STRIP) (PINS 1 THRU 22 ARE EXTERNAL FLIP-FLOP INDICATOR CONNECTIONS.)

P100 — 29 PIN IPC D-122 (NON STANDARD CONNECTIONS)

PIN 2, P2-0 THRU P2-10 → F-F SCREEN (0), 0V.

PIN 23, P2-0 THRU P2-10 → F-F SCREEN (1), 0V.

PIN 8, P1-0 THRU P1-10 → G-T PLATE, +250V.

PIN 3, P1-0 THRU P1-10 → READ OUT G-T SCREEN, +90V.

PIN 6, P1-0 THRU P1-10 → G-T CONTROL BIAS, -15V.

PIN 22, P1-0 THRU P1-10 → READ IN G-T SCREEN, +90V.

E2 — GATE TUBE 7AK7 — 6.3V. FIL.

E3 — FLIP-FLOP 7AD7 — 6.3V. FIL.

E4 — SWITCH TUBE 7AD7 AND V100 — 6.3V. FIL.

GROUND

TO CENTER TAP OF SWITCH TUBE FILAMENT TRANSFORMER

PIN 18, P3-0 THRU P3-10 → SWITCH TUBES, -150V.

PIN 18, P2-0 THRU P2-10 → FLIP-FLOP, -150V.

DRAWING REFERENCES:

1. AL. PANEL: E-50057.
2. ASSEMBLY: E-50059.
3. PL-50059.

NOTES:

1. UNLESS OTHERWISE SPECIFIED, THE FOLLOWING SHALL APPLY TO ALL COMPONENTS ON THIS DRAWING:
   a. RESISTORS ARE JAN SPEC., 1W, ±10%.
   b. CAPACITORS ARE JAN SPEC., MICA, ±5%.
   c. VIDEO CONNECTORS ARE TYPE UG-290/U.
   d. E2, E3 & E4 ARE 4 PIN JONES STRIP.
2. ● SOLID CIRCLE ON CONNECTORS INDICATES CONNECTION IN VIDEO CIRCUIT.

PRINT NO. 3 DATE 1-8-52
ISSUED TO K. Olsen

GRADED BY: DATE: 1-9-51

THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:
GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN

SERVOMECHANISMS LABORATORY OF THE
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIVISION OF INDUSTRIAL COOPERATION PROJECT NO. 6345

CIRCUIT SCHEMATIC,
DISPLAY DECODER, WWI.

SCALE: —
DR. M.M. 7-3-51
ENG. K. H. Olsen
CK. 7/6/51
APP. 8/7/51

D-50058-1

D-50058-2

SECTIONS 2 THRU 10 ARE IDENTICAL WITH SECTION 1 EXCEPT FOR COMPONENT NUMBERS

R2 IS A 100Ω, W-W, IRC, ±1% RESISTOR IN SECTION 10 ONLY (R2-10)

SECTION

SECTION 0

GATE PLUG-IN UNIT SECTION (B-36958)

D-C FLIP FLOP PLUG-IN UNIT SECTION (C-36957)

SWITCH TUBE PLUG-IN UNIT SECTION (B-36959)

E1 (E1 CONSISTS OF A 10 TERMINAL & 12 TERMINAL JONES STRIP) (PINS 1 THRU 22 ARE EXTERNAL FLIP-FLOP INDICATOR CONNECTIONS.)

P100 29 PIN IPC D-122 (NON STANDARD CONNECTIONS)

DRAWING REFERENCES:

1. AL. PANEL: E-50057.
2. ASSEMBLY: E-50059.
3. PL-50059.

NOTES:

1. UNLESS OTHERWISE SPECIFIED, THE FOLLOWING SHALL APPLY TO ALL COMPONENTS ON THIS DRAWING:
   a. RESISTORS ARE JAN SPEC., 1W, ±10%.
   b. CAPACITORS ARE JAN SPEC., MICA, ±5%.
   c. VIDEO CONNECTORS ARE TYPE UG-290/U.
   d. E2, E3 & E4 ARE 4 PIN JONES STRIP.
2. ● SOLID CIRCLE ON CONNECTORS INDICATES CONNECTION IN VIDEO CIRCUIT.

PRINT NO. 3 DATE 1-29-52
ISSUED TO W. Olsen

SERVOMECHANISMS LABORATORY OF THE MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIVISION OF INDUSTRIAL COOPERATION PROJECT NO. 6345

CIRCUIT SCHEMATIC, DISPLAY DECODER, WWI

D-50058

GRADED BY: DATE. THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW.
GRADE 1 FOR REFERENCE ONLY
GRADE 2 FOR LIMITED DESIGN
GRADE 3 FOR [illegible]

SC 50795

Clear

Comp

Set

FF 02

FF 03

FF 04

Set comp clear

Decoder Out

Read gate

digits to IC

SERVOMECHANISMS LABORATORY OF THE
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIVISION OF INDUSTRIAL COOPERATION PROJECT NO.

Array Driver

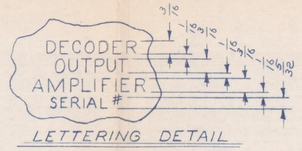
SCALE:	DR.	
ENG.	CK. 31 Aug 51	APP.

SC- 50795

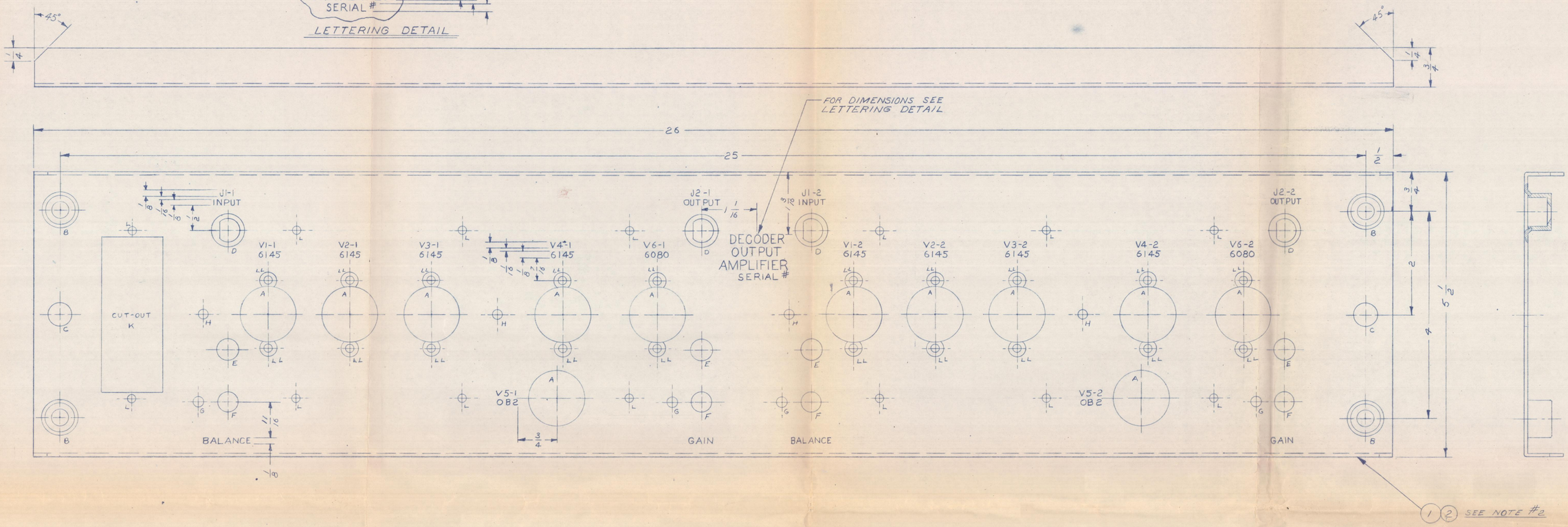
D-54098

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS .000 FOR REFERENCE ONLY

USED ON ASSY: D-55119



LETTERING DETAIL



HOLE DATA CHART

LETTER	SIZE OF HOLE	NO. OF HOLES	REMARKS
A	1 1/16 DIA.	12	
B	5/8 DIA.	4	DIMPLE AS SHOWN.
C	7/16 DIA.	2	
D	7/8 DIA. (WITH FLAT)	4	USE STD DCL UG 62 5/8 PANEL PIERCING TOOL. SPOTFACE TO 5/8 DIA. ON THIS SIDE OF PANEL AS SHOWN. SEE NOTE #3.
E	13/32 DIA.	4	
F	3/8 DIA.	4	
G	3/16 DIA.	4	
H	#15 (.180) DRILL	4	
K	CUT-OUT. 1 5/32 X 3	1	USE STD 12 PIN JONES PLUG PIERCING TOOL.
L	#24 (.152) DRILL	34	SPOTFACE TO 5/16 DIA. "LL" HOLES ON THIS SIDE OF PANEL AS SHOWN. SEE NOTE #3. 20 REQ'D.

NOTES:
1. REMOVE ALL BURRS & SHARP EDGES.
2. TO ITEM #1, SWAGE ITEM #2 (CAPTIVE SCREW RECEPTACLE) AS SHOWN.
3. FOR ALL HOLE LOCATIONS NOT DIMENSIONED OR OTHERWISE SPECIFIED, USE DRAWING AS TEMPLATE.
4. PANEL SHALL BE FINISHED PER DCL SPEC. S7.507-1.
5. AFTER PANEL IS FINISHED, SPOTFACE HOLES AS SPECIFIED IN HOLE DATA CHART.
6. MARKING SHALL BE IN ACCORDANCE WITH DCL SPEC. S7.508, WHITE & CENTERED AS SHOWN.

This drawing has not been checked
V.J.S.

ITEM	MATERIAL-DESCRIPTION	PART NO.	QTY.
2	RECEPTACLE (CAPTIVE SCR.) SYLVANIA	R60H015	4
1	AL. SHEET, 1/16 THK	2S-H14	—

FOR CHECKING PURPOSES ONLY
JUN 23 1953

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING — D. I. C. PROJECT NO. 6889

SUB-ASSY & DETAIL, DECODER OUTPUT AMPLIFIER, WWI

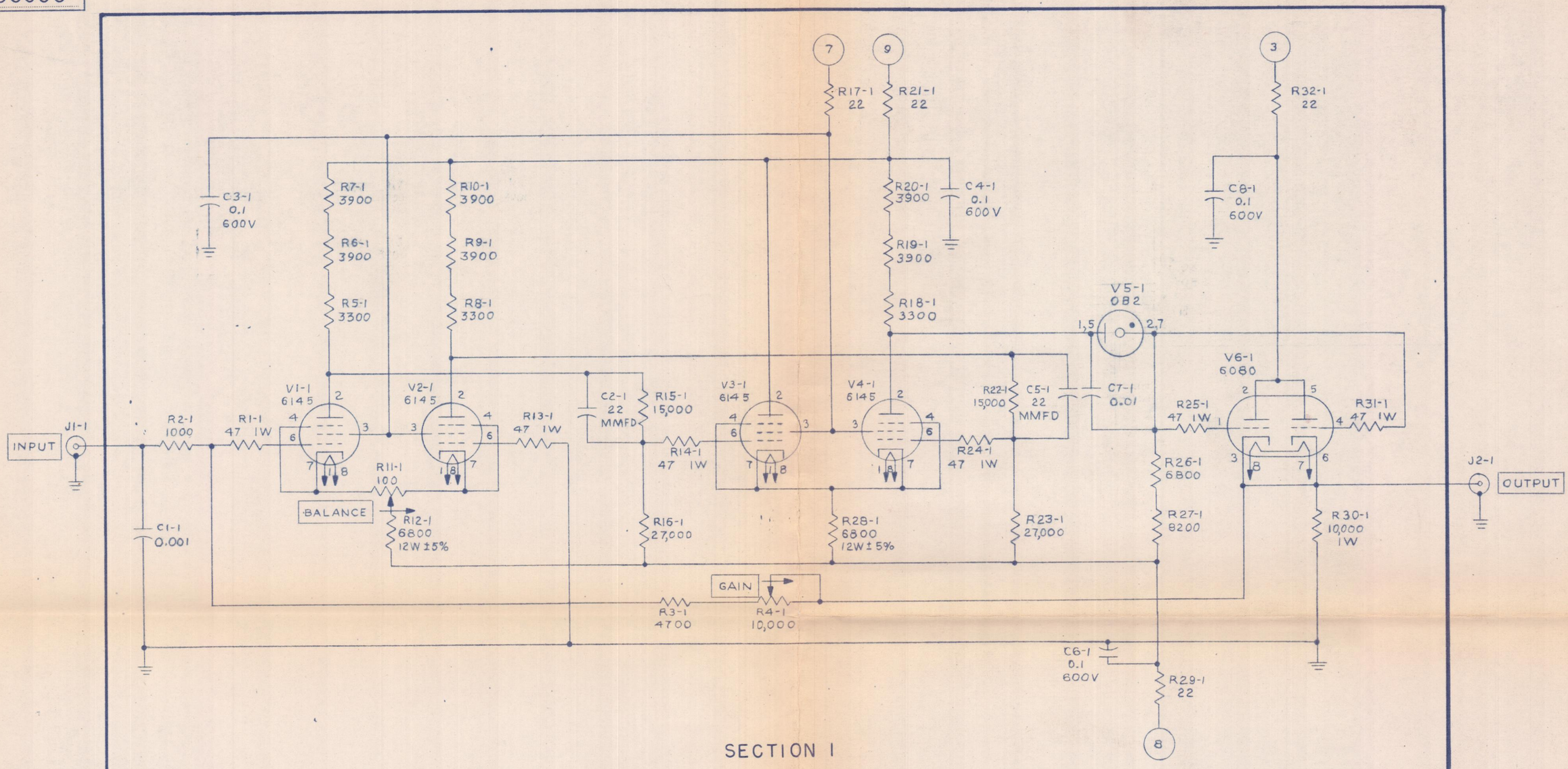
SCALE: 1:1 DR. TI 5-27-53
ENG. CK. APPD.
D-54098

GRADED BY: DATE:
THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:
GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN

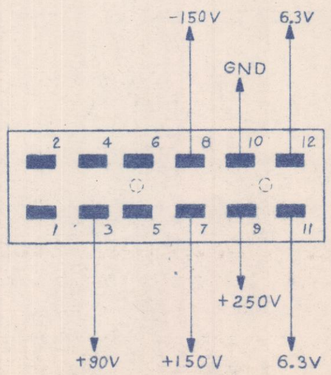
CHG. -10 -9 -8 -7 -6 -5 -4 -3 -2 -1 CHK. DATE APPD.

K&E PHOENIX N188 TRACING CLOTH

C-36905



P1
12 PIN
JONES PLUG
(MALE)
P-2412-SB



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTORS ARE IN OHMS: 2W ±10%
   B. CAPACITORS ARE IN MICROFARADS.
   C. VIDEO CONNECTORS ARE JAN UG-625/U
2. R11-1, & R11-2, 100Ω POT. SHOULD BE VARIED SO THAT OUTPUT IS +2V WHEN THE INPUT IS GROUNDED.
3. R4-1, & R4-2, 10,000Ω POT. SHOULD BE VARIED SO THAT OUTPUT IS +22V WHEN THE INPUT IS AT ITS MOST NEGATIVE VOLTAGE.

DRAWING REFFERENCES: *
1. ASSEMBLY: D-55119
2. PARTS LIST: PL-55119

PRINT NO. 6
JUN 23 1953
ISSUED TO K. Olsen

GRADED BY: DATE: THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:
SHD 6/3/53 GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN

CHG.	CN#	DATE	APPD.
-10			
-9			
-8			
-7			
-6			
-5			
-4			
-3			
-2			
-1			

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING — D. I. C. PROJECT NO. 6889

CIRCUIT SCHEMATIC
DECODER OUTPUT AMPLIFIER, WWI

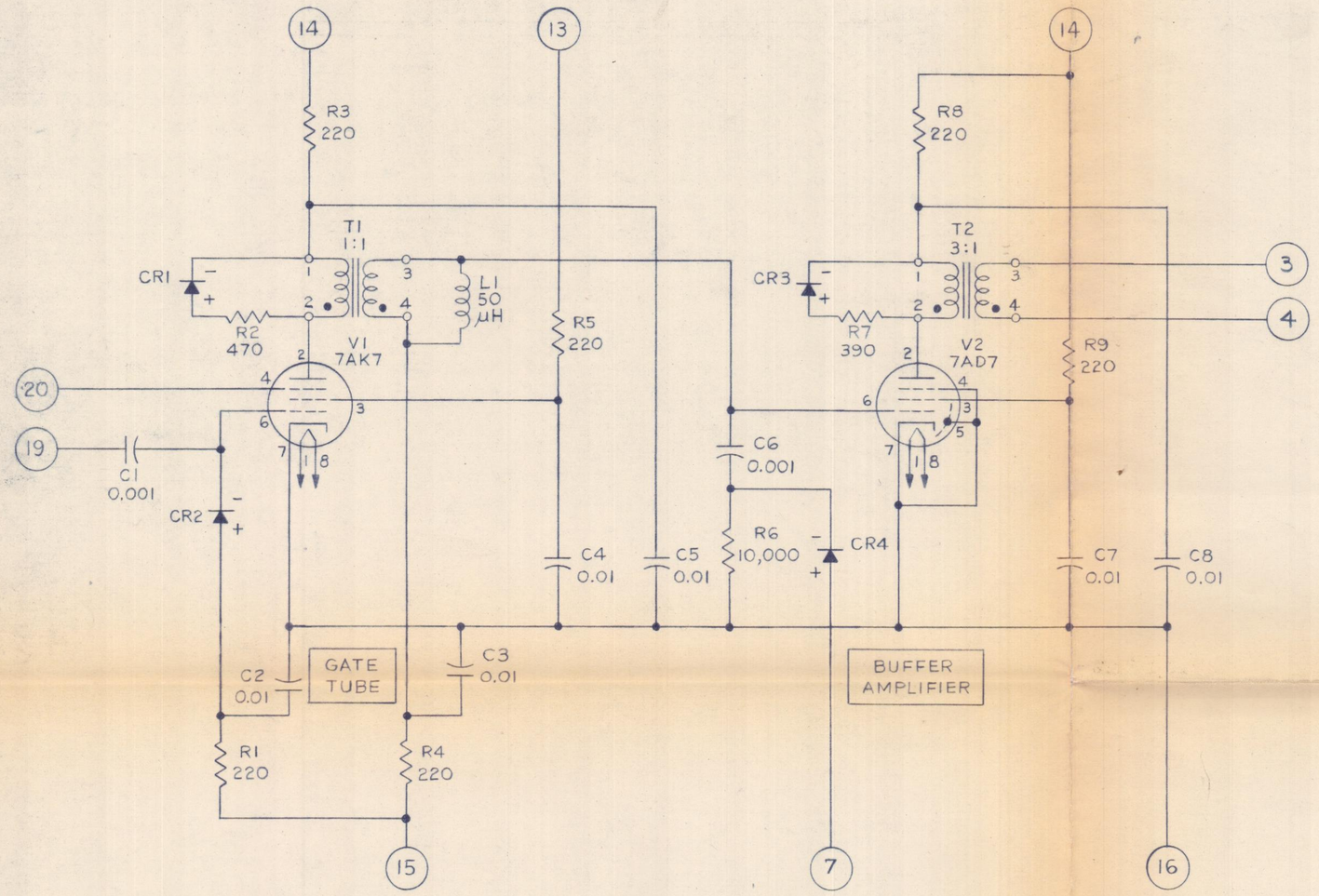
SCALE: ——— DR. B. PETRELIS 5-23-53

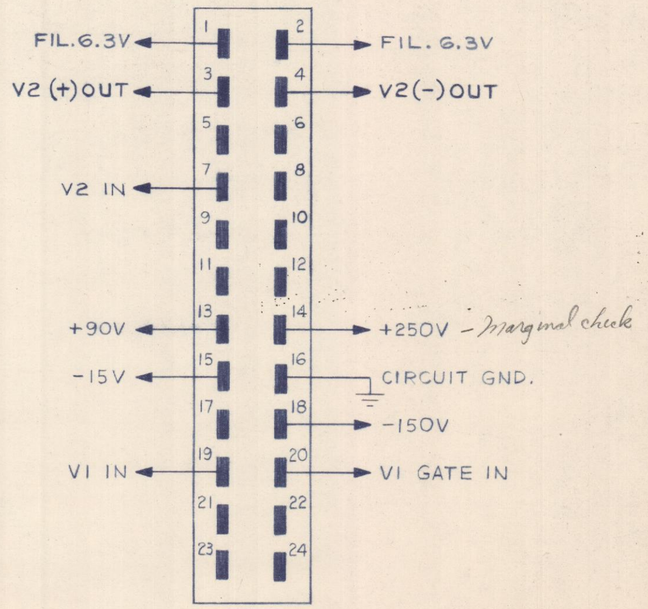
ENG. 6-2-53 ARC | CK. 6/4/53 | APPD. 6-2-53

C-36905

K+E ALBANENE 1951 TRACING PAPER

C-50827





P1
RADIO TERMINAL
CONNECTOR
#16824-15
CANNON ELEC. CO.

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   - A. RESISTORS ARE IN OHMS; JAN SPEC. COMPOSITION TYPE, ½W, ±10%
   - B. CRYSTAL RECTIFIERS ARE SYLVANIA TYPE 1N34A
   - C. ALL 0.01 MFD CAPACITORS ARE CERAMIC DISC, 600V
   - D. ALL OTHER CAPACITORS ARE MFD; JAN SPEC., MICA, ±10%

DRAWING REFERENCES:

1. ASSEMBLY: C-50831
2. BLOCK SCHEMATIC:
3. PARTS LIST: PL-50831

PRINT NO. 17 DATE 7-18-52
ISSUED TO Ken Olsen

GRADED BY: DATE: THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:
GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
3/4/52 GRADE III FINAL DESIGN

CHG.	CN#	DATE	APPD.
-10			
-9			
-8			
-7			
-6			
-5			
-4			
-3			
-2			
-1			

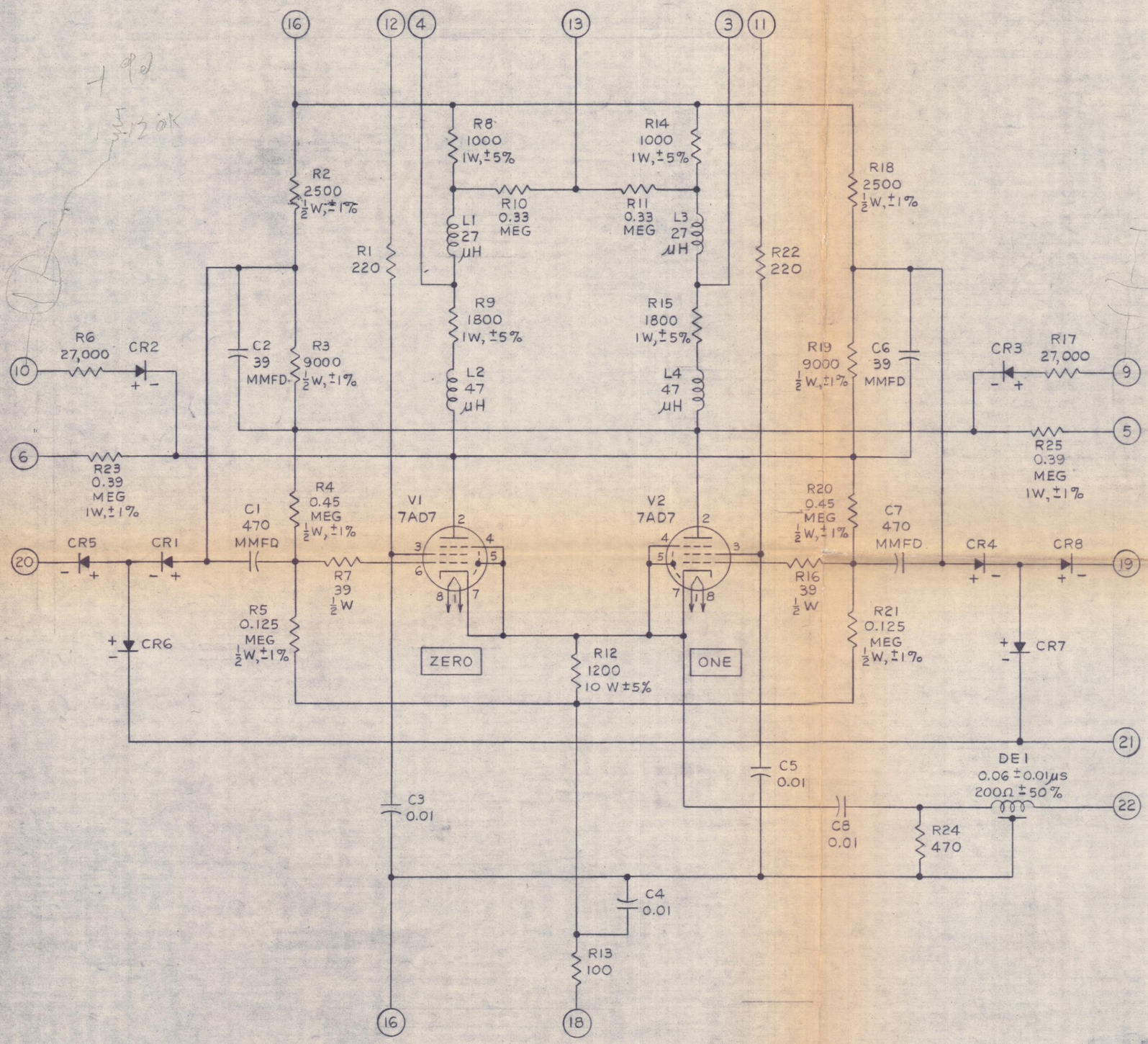
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING – D. I. C. PROJECT NO. 6889

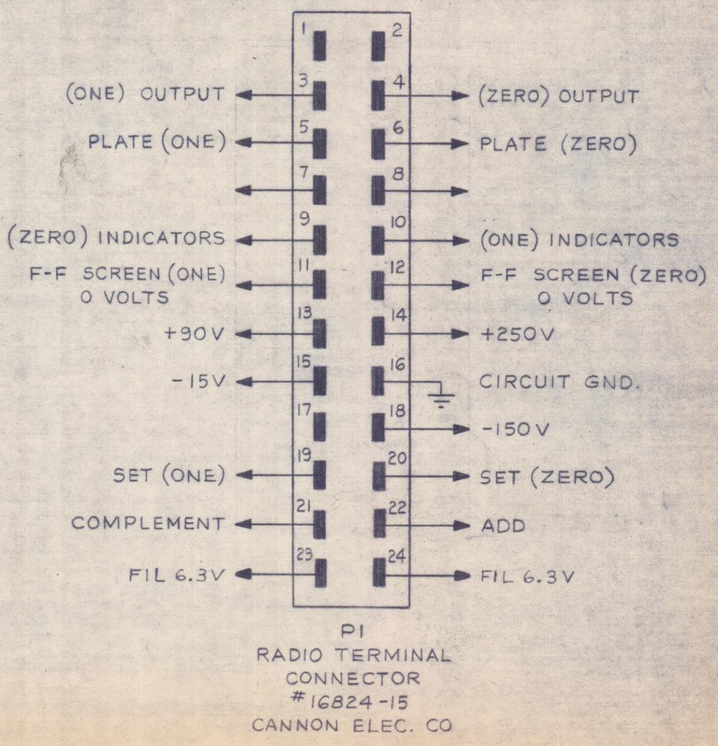
CIRCUIT SCHEMATIC
PLUG-IN GATE-BUFFER AMPLIFIER, MOD II, WWI

SCALE: ~ | DR. F.B. Feb, 6 '52 | C-50827

ENG. [illegible] 2/22/52 | CK. 2-26-52 J. Davis | APPD. 3-4-52 [illegible]

C-50825





P1
RADIO TERMINAL CONNECTOR
#16824-15
CANNON ELEC. CO

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTORS ARE IN OHMS; JAN SPEC. COMPOSITION TYPE, ½W, ±10%
   B. RESISTORS R2 THRU R5, AND R18 THRU R21 ARE CONTINENTAL CARBON "NOBLELOY" NF ½ OR THE EQUIV.
   C. CRYSTAL RECTIFIERS ARE SYLVANIA TYPE 1N34-A
   D. ALL 0.01 MFD CAPACITORS ARE CERAMIC DISC, 600V
   E. ALL OTHER CAPACITORS ARE MFD; JAN SPEC., MICA, ±10%
2. FOR FURTHER SPECIFICATION OF SPECIAL DELAY LINE (DE1) SEE ASSEMBLY DRAWING D-51068

DRAWING REFERENCES:
1. ASSEMBLY: C-50838
2. BLOCK SCHEMATIC:
3. BLOCK DIAGRAM:
4. PARTS LIST: PL-50838

PRINT NO. #2
SEP 22 1952
ISSUED TO K. Olsen

GRADED BY: DATE:
THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:
GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
3HD 4/22/52 GRADE III FINAL DESIGN

CHG.	CN#	DATE	APPD.
-10			
-9			
-8			
-7			
-6			
-5			
-4			
-3	3925	5/1/52	
-2	3821	6-27-52	
-1	3443	4/9/52	

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING – D. I. C. PROJECT NO. 6889

CIRCUIT SCHEMATIC
PLUG-IN D-C FLIP-FLOP, MOD. II, WWI

SCALE: ~ DR. F.B. Apr 8 '52
ENG. a.w 4/5/52 CK. RBB-4/9/52 APPD. 4/22/52
C-50825
MN

C-36359-1

R1 220Ω

R2 220Ω

C1 0.01 MFD

C2 0.01 MFD

V1 5687

J1 GT2 & READER GT

J2 GT1 & RECORDER GT

CR11 CR12 CR13 CR14 CR23 CR24

CR3 CR9 CR19 CR4 CR7 CR20

R3 0.1 MEG CR27 D357

R4 0.1 MEG CR28 D357

R5 0.1 MEG CR29 D357

R6 0.1 MEG CR30 D357

V2 5687

V3 5687

J3 J4 PRINTERS

J5 J6 PUNCHES

CR35 CR1 CR36 CR2

FLEXO J17

CR5 CR10 CR15 CR25 CR16 CR21 CR6 CR8 CR17 CR26 CR18 CR22

R7 0.1 MEG CR31 D357

R8 0.1 MEG CR32 D357

R9 0.1 MEG CR33 D357

R10 0.1 MEG CR34 D357

V4 5687

V5 5687

J7 J8 READERS

J9 J10 READERS

V1 +150V.

V2-V5 +90V.

5687'S 6.3V

E1 140-6 JONES STRIP

J16 J15 IN-OUT DIGIT 13

J14 J13 DIGIT 11

J12 J11 DIGIT 12

DRAWING REFERENCES:
1. ASSEMBLY: D-36488
2. AL. PANEL DETAIL: D-36489
3. BLOCK SCHEMATIC: SD-36186

PRINT NO. 9 DATE 8-13-51
ISSUED TO K. Olsen

FOR FURTHER SPEC. OF COMPONENTS SEE PL-36488

NOTES: UNLESS OTHERWISE SPECIFIED, THE FOLLOWING SHALL APPLY TO ALL COMPONENTS IN THIS SCHEMATIC:
1. ALL CRYSTAL RECTIFIERS ARE TYPE IN38A.
2. ALL RESISTORS ARE JAN. SPEC. COMPOSITION TYPE, ½W. ±10%
3. ALL VIDEO CONNECTORS ARE TYPE BNC-290/U.

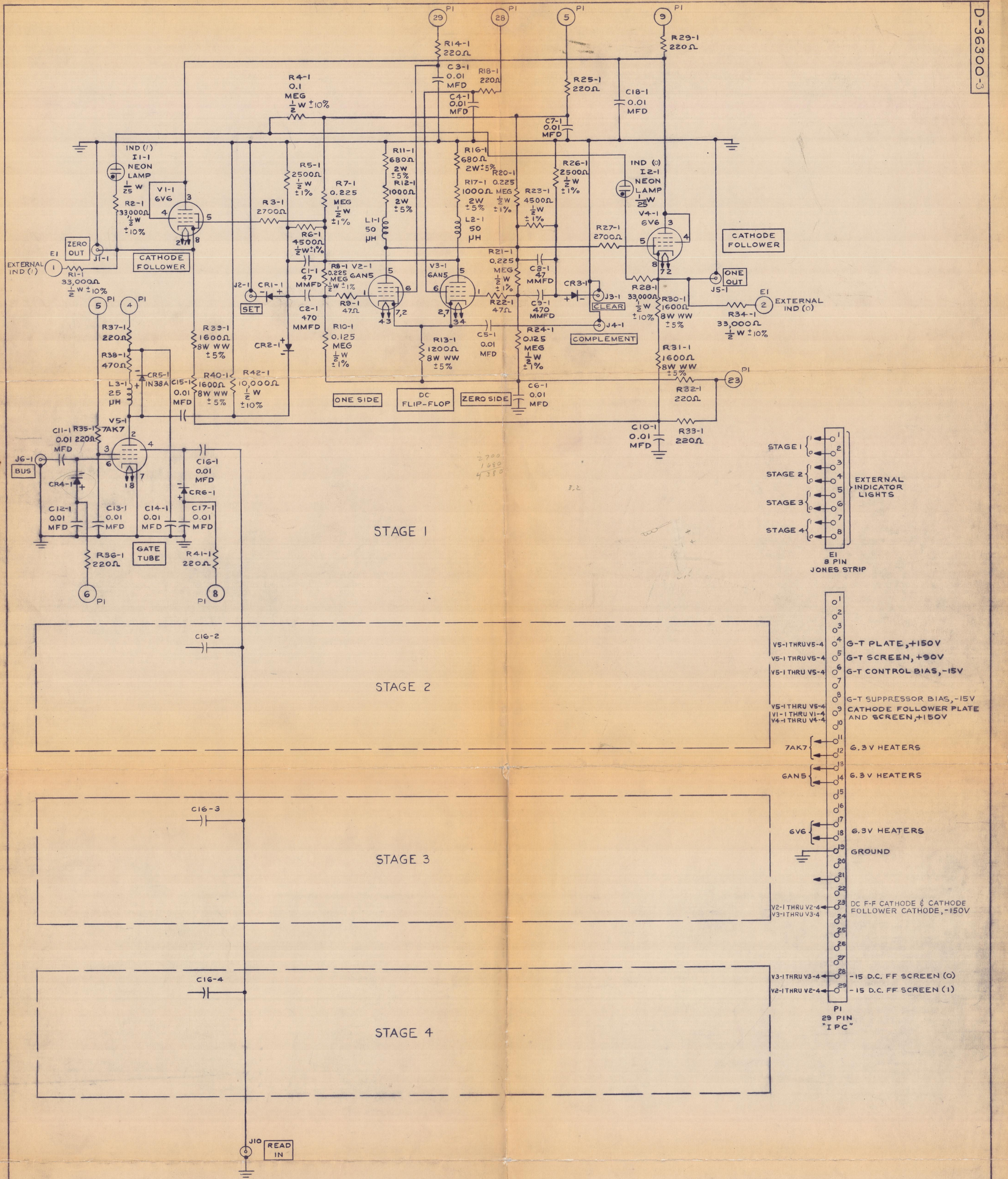
GRADED BY: DATE: THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:
GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
JTK 12-12-50

SERVOMECHANISMS LABORATORY OF THE
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIVISION OF INDUSTRIAL COOPERATION PROJECT NO. 6345

CIRCUIT SCHEMATIC, 420, IN-OUT SWITCH, FLEXOWRITER MATRIX, WWI

SCALE: —— DR. D.L.S. 12-11-50
ENG. 12-12-50 JAOB CK. 12-12-50 V.Bawio APP.
C-36359-1

D-36300-3



NOTES:

1. UNLESS OTHERWISE SPECIFIED, THE FOLLOWING SHALL APPLY TO ALL COMPONENTS IN THIS SCHEMATIC:
   1. STAGES 2, 3, AND 4 ARE IDENTICAL WITH STAGE 1 EXCEPT FOR DASH NUMBERS OF COMPONENTS. FOR INSTANCE, ONE OF THE CHOKES IN STAGE 4 IS L1-4.
   2. RESISTORS ARE JAN SPEC., COMPOSITION TYPE, 1W, ± 5 %.
   3. CAPACITORS ARE JAN SPEC., MICA, ± 5 %.
   4. VIDEO CONNECTORS ARE UG-290/U.
   5. CRYSTAL RECTIFIERS ARE TYPE D-357.
2. FOR SPECIFICATION OF COMPONENTS SEE PL-36378

DRAWING REFERENCES:

1. BLOCK SCHEMATIC: B-36330.
2. ASSEMBLY: D-36378.
3. ALUMINUM PANEL: D-36382.

PRINT NO. 10 DATE 5-1-51
ISSUED TO R. Olsen

GRADED BY:	DATE:	THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:
		GRADE I FOR REFERENCE ONLY
		GRADE II PRELIMINARY DESIGN
11?	12-1-50	GRADE III FINAL DESIGN

SERVOMECHANISMS LABORATORY OF THE
[M]ACHUSETTS INSTITUTE OF TECHNOLOGY
OF INDUSTRIAL COOPERATION PROJECT NO. 6345

CIRCUIT SCHEMATIC, 420
INPUT-OUTPUT SWITCH, SWITCH PANEL, WWI

DR. A.M.G. 11-24-50
11-29-50
11-29-50

D-36300-3