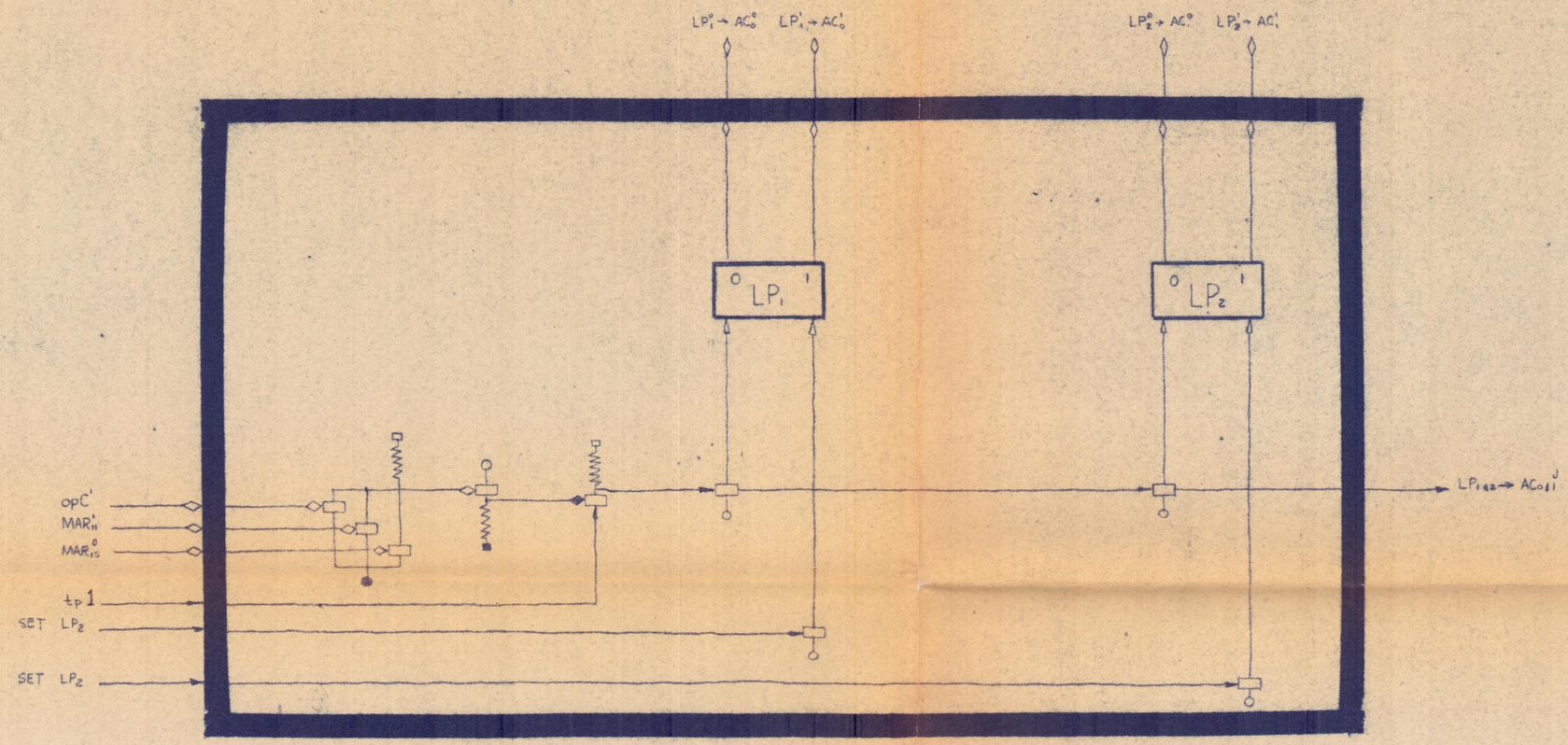
C-67874

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY



7 LOGIC BOTTLES
6 INPUTS
5 OUTPUTS
29 SBT'S
2 GE'S

PRINT ISSUED
OCT 16 1956

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE:

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.

LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

LIGHT PEN CONTROL, TX-0 BLOCK SCHEM.

SCALE:
DR. C NORMAN 5/10/56
ENG. 11-10-56 C.G. Norman
CK.
APPD. 10-10-56 C.G. Norman

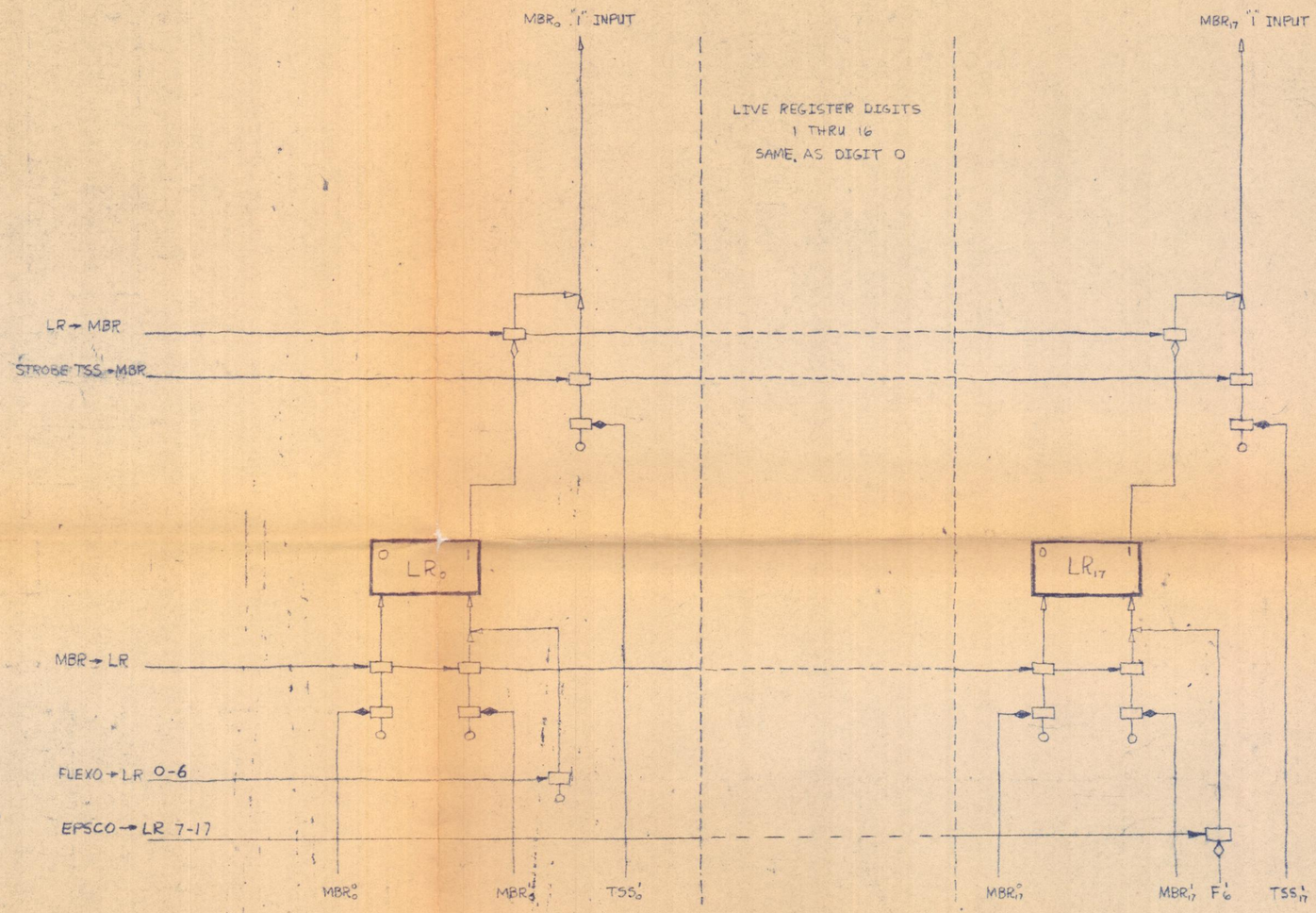
C-67874

CHG.	CN#	DATE	APPD.
-20			
-19			
-18			
-17			
-16			
-15			
-14			
-13			
-12			
-11			
-10			
-9			
-8			
-7			
-6			
-5			
-4			
-3			
-2			
-1			

4M-7-54-Boston Blue Print

C-67870

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY



PRINT ISSUED
JUN 17 1957

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE:

K. Olsen

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.

LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

LIVE REGISTER, TX-0 BLOCK SCHEMATIC

SCALE:
DR. C NORMAN 5-8-56
ENG. CA Norman
CK. 6-12-57 R. ORO
APPD. 10- CA Norman

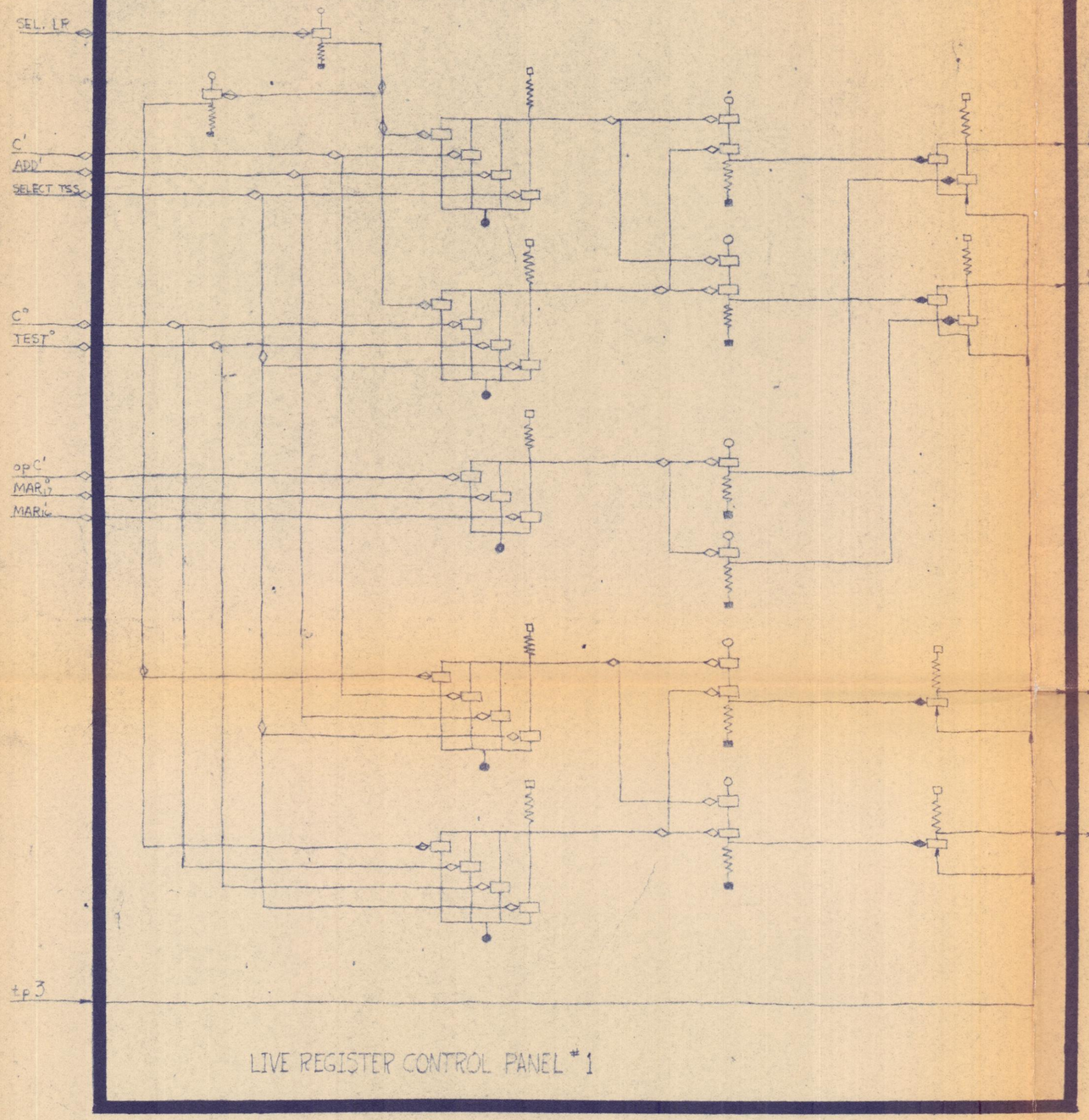
C-67870

CHG.	CN#	DATE	APPD.
-1	8901	5-24-57	CAN
-2			
-3			
-4			
-5			
-6			
-7			
-8			
-9			
-10			
-11			
-12			
-13			
-14			
-15			
-16			
-17			
-18			
-19			
-20			

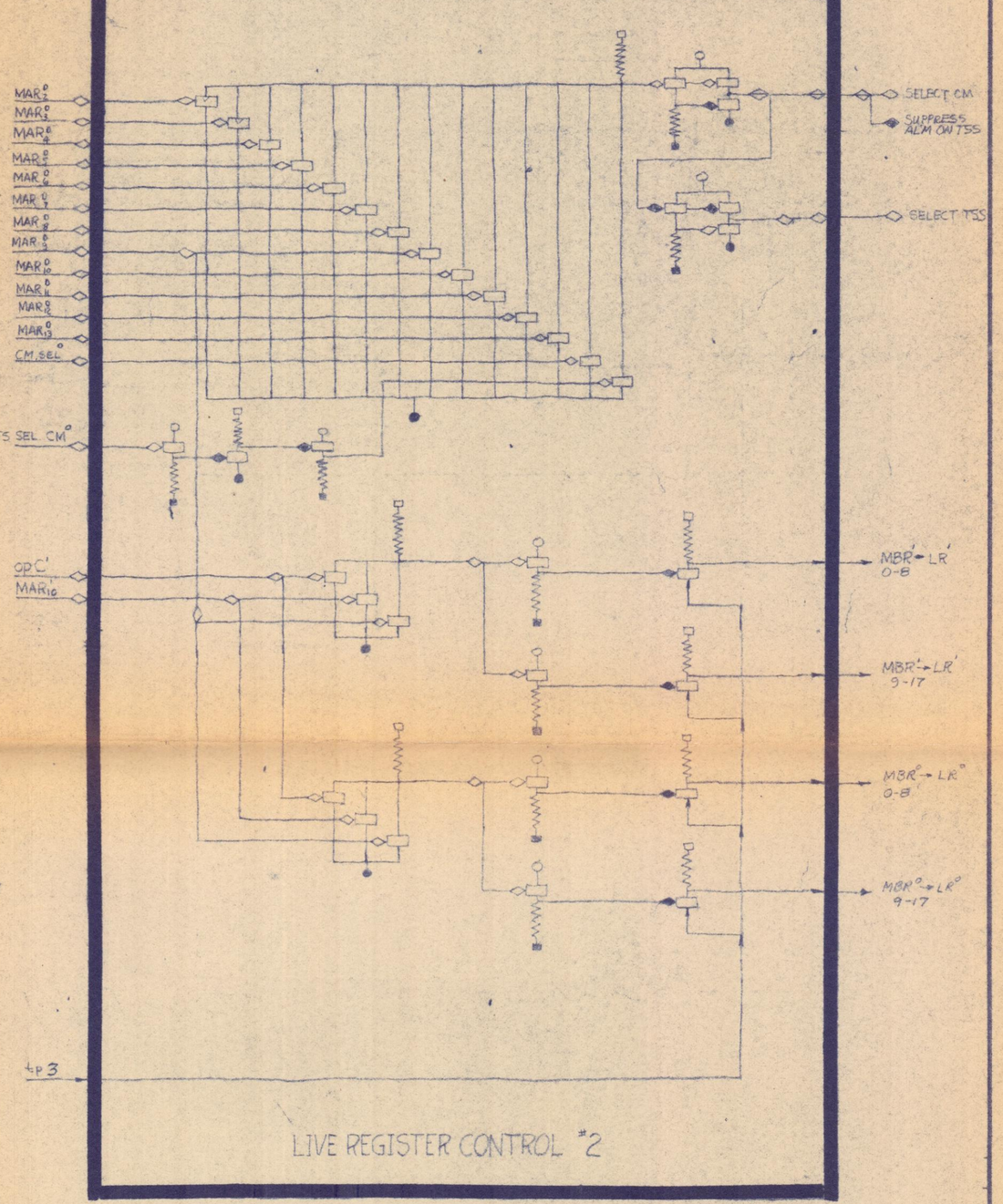
4M-7-54-Boston Blue Print

C-67885

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY



LIVE REGISTER CONTROL PANEL #1



LIVE REGISTER CONTROL #2

PRINT ISSUED
OCT 16 1956

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE: 10-16-56

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.

CHG.	CN#	DATE	APPD.
-20 -19 -18 -17 -16 -15 -14 -13 -12 -11 -10 -9 -8 -7 -6 -5 -4 -3 -2 -1			

LINCOLN LABORATORY, DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

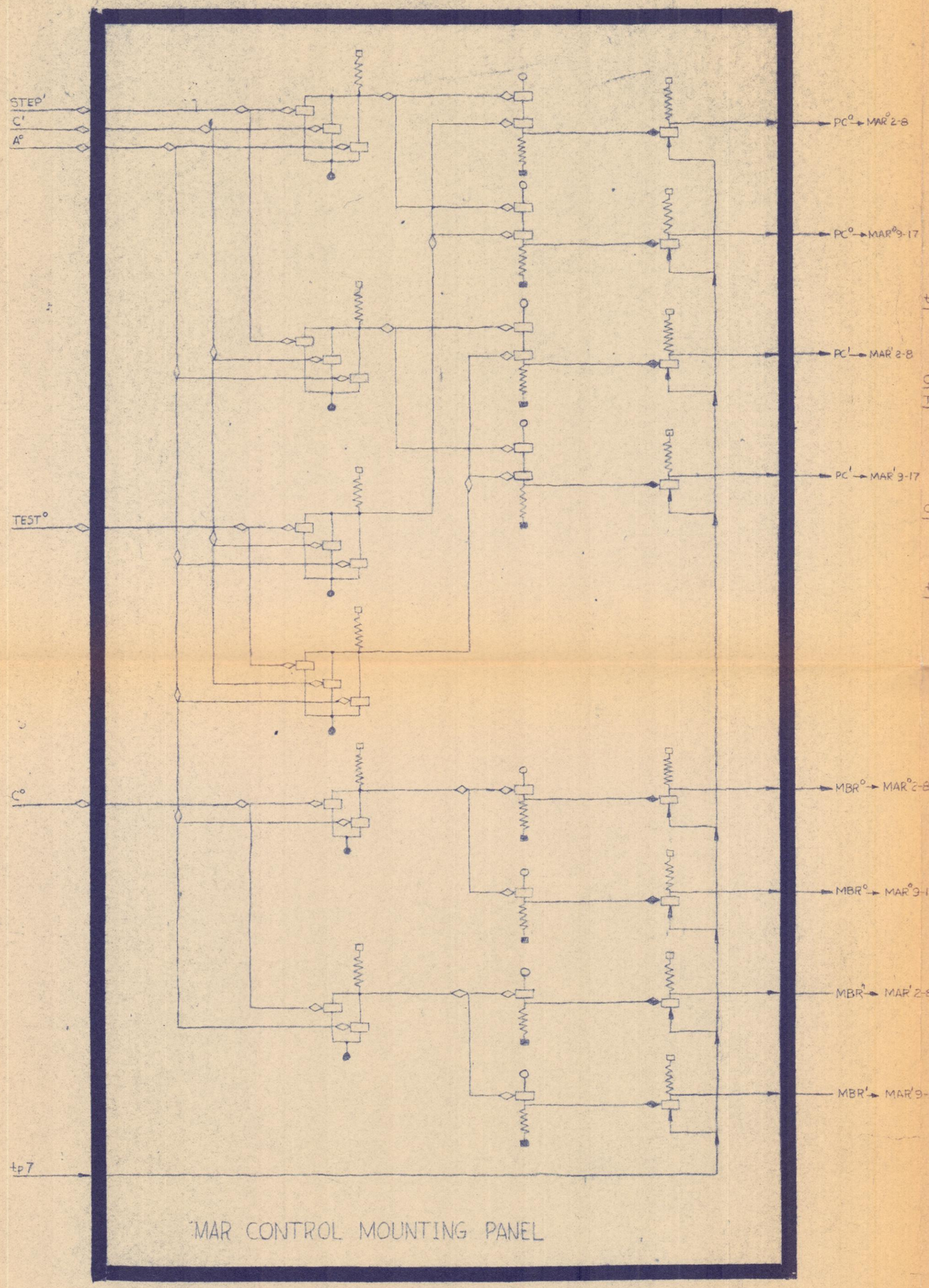
LIVE REGISTER CONTROL, BLOCK SCH., TX-0

SCALE:
DR. C NORMAN 9-5-56
ENG. 10-10-56 C A Norman
CK.
APPD. 10-10-56 C A Norman

C-67885

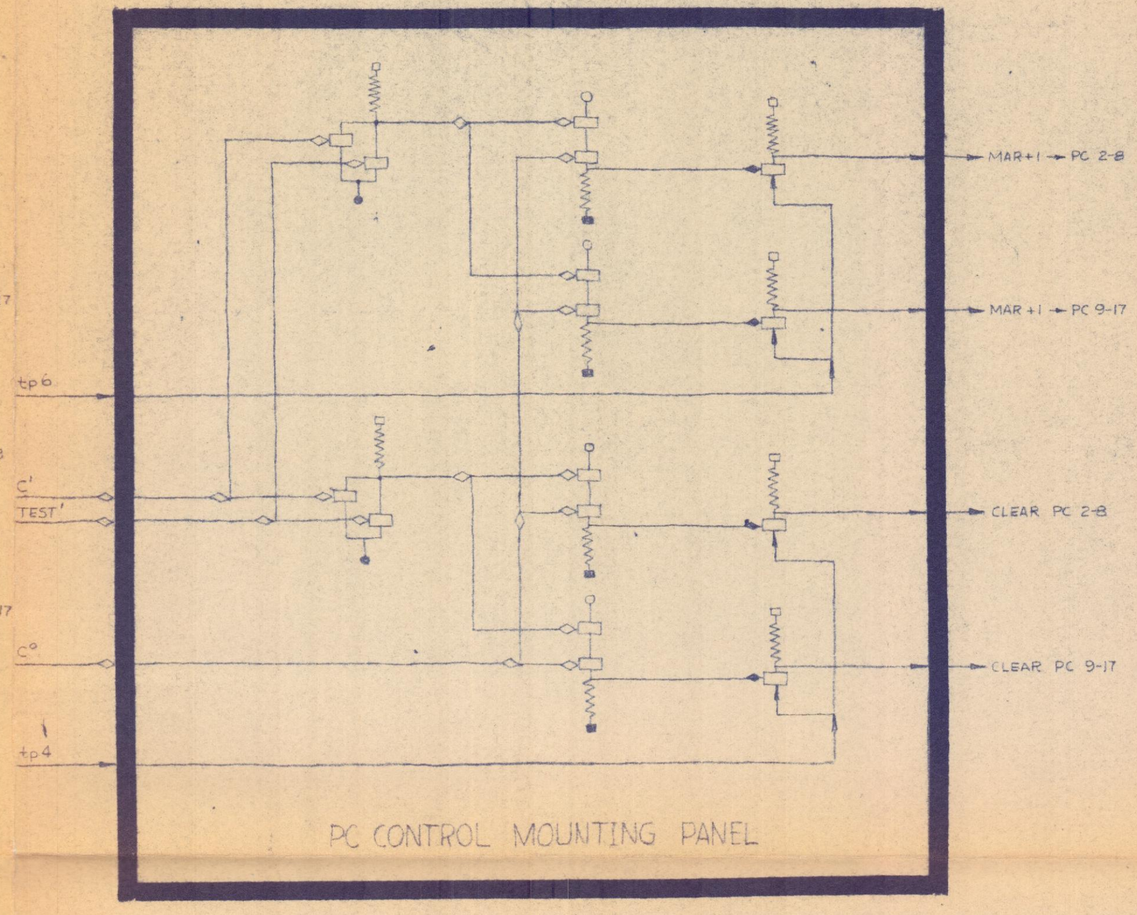
C-67879

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY



MAR CONTROL MOUNTING PANEL

22 LOGIC BOTTLES
8 OUTPUTS
6 INPUTS
TRANSISTORS
36 SBT'S



PC CONTROL MOUNTING PANEL

12 LOGIC BOTTLES
4 OUTPUTS
6 INPUTS
TRANSISTORS
16 SBT'S

PRINT ISSUED
OCT 16 1956

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE:

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.

CHG.	CN#	DATE	APPD.
-20			
-19			
-18			
-17			
-16			
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-14			
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-4			
-3			
-2			
-1			

LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

MAR & PC CONTROL, TX-0 BLOCK SCHEMATIC

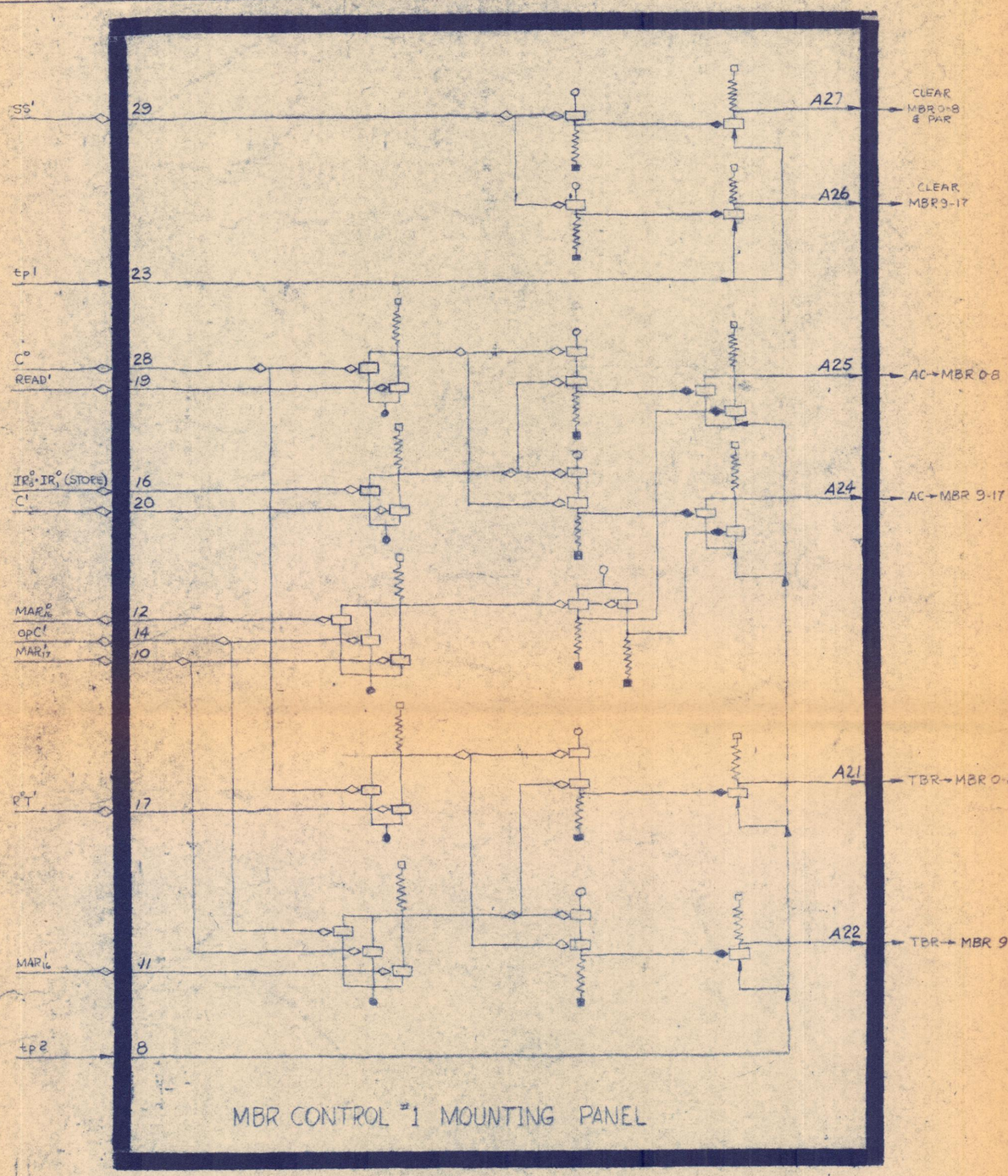
SCALE: | DR. C A NORMAN 1/23/56 | C-67879

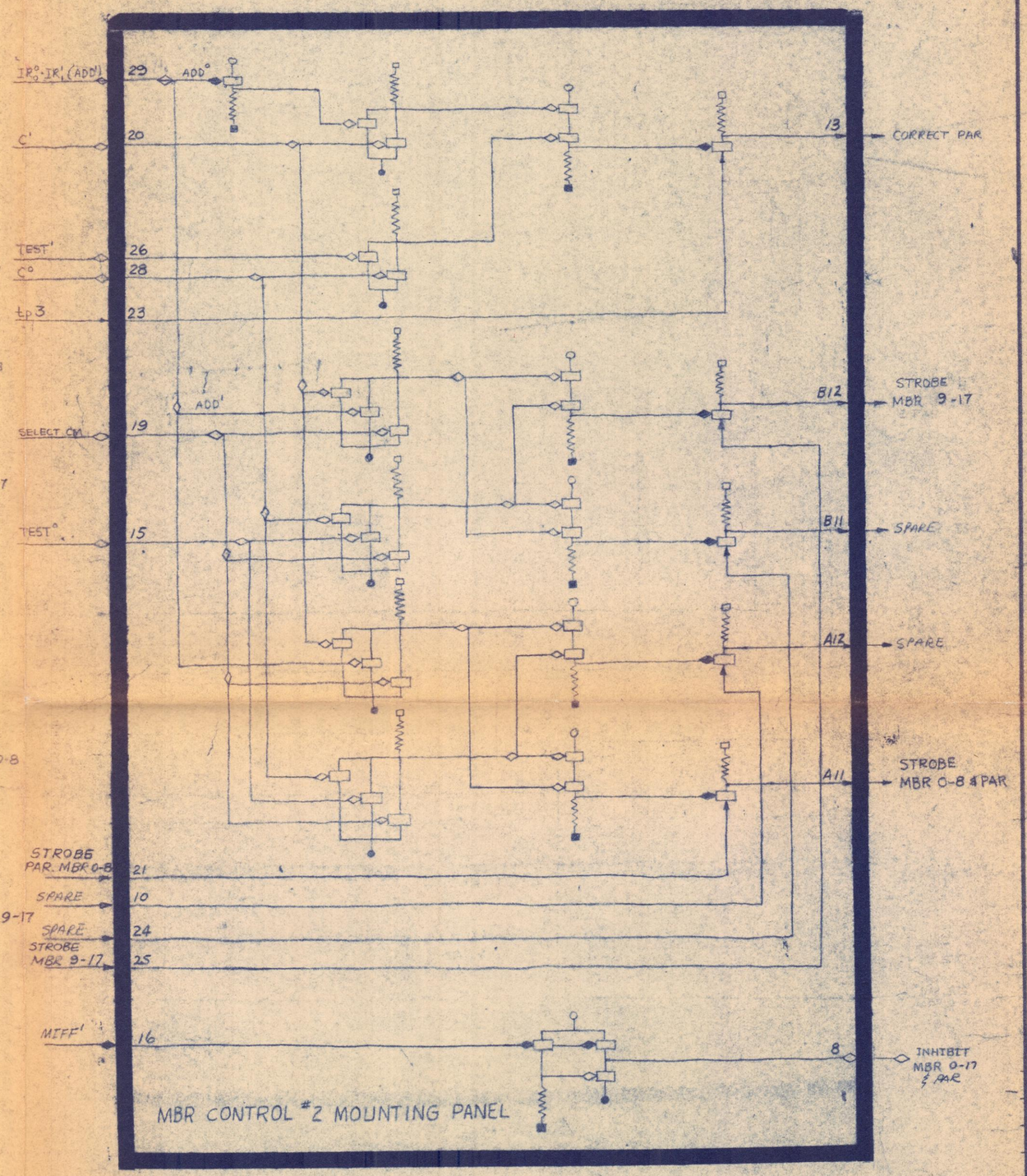
ENG. 10-10-56 C A Norman | CK. | APPD. 10-10-56 C A Norman

4M-7-54-Boston Blue Print

C-67884

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY





GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE:

K. Olsen

PRINT IS SUED JUN 17 '57

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.

CHG.	CN#	DATE	APPD.
-20			
-19			
-18			
-17			
-16			
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-14			
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-7			
-6			
-5			
-4			
-3			
-2	8849	5-24-57	CAN
-1	8907	12-14-56	CAN

LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

MBR CONTROL, TX-0 BLOCK SCHEMATIC

SCALE:
DR. CA NORMAN 9-8-56
ENG. 10-10-56 C.A. Norman
CK. 6-12-57 R. ORO
APPD. 10-10-56 CA Norman

C-67884

4M-7-54-Boston Blue Print

C-67871

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005' FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY

READ
MAR DIGITS 6 & 14

READ
MAR DIGITS 2 & 10

INHIBIT
MBR 0-8 & PAR

MBR 9-17

MEMORY READ FF MOUNTING PANEL

°MRFFv'

°MRFFu'

tp 2A
tp 5

C°
TEST°

C'
IR°

tp 1
tp 1A

MEMORY INHIBIT MOUNTING PANEL

T&S MAR SEL

°MIFF'

CLEAR IFF

tp 6

C°
TEST°

INHIBIT

C'
IR°

tp 4

8 LOGIC BOTTLES
1 IND " "
3 OUTPUTS
6 INPUTS
TRANSISTORS
20 SBT'S
1 GE

PRINT ISSUED
MAY 28 1957

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE:

K. Olsen

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.

LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

MEMORY CONTROL, TX-0 BLOCK SCHEMATIC

SCALE:
DR. C.A. NORMAN 9/5/56
ENG. 10-10-56 C.Q. Norman
CK.
APPD. 10-10-56 C.Q. Norman

C-67871

CHG. | CK'd | DATE | APPD.
-1 8896 5-23-57 EW

4M-7-54-Boston Blue Print

C-67878

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY

TO S/S FF

PBS FF MOUNTING PANEL

PBS

PB RESTART
PB TEST
PB READ IN
PB STOP
STOP ON AL'M
STOP ON C°
C°
STOP ON C'
C'
R°T°
REPEAT°
ORC'
MAR'4
MAR'5
IR'5·IR'4 (ADD')
READ'
tp 6

19 LOGIC BOTTLES
1 IND. " "
6 OUTPUTS
18 INPUTS
TRANSISTORS
28 SBT'S
1 GE

TO S/S FF

IOS FF MOUNTING PANEL

IOS

PETR COMP.
PUNCH/
PRINT COMP.
EPS00 COMP.
DISPLAY COMP.
CONTROL STOP
C'
READ'
A°OP·C°
MAR'4
MAR'5
C°
IR'0·IR'1 (SIDRE')
tp 8

IO STOP
CLEAR
S/S FF

15 LOGIC BOTTLES
1 IND. " "
3 OUTPUTS
15 INPUTS
TRANSISTORS
31 SBT'S
1 GE

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE:

K. Olsen
PRINT ISSUED
JUN 17 1957

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.

CHG.	CN#	DATE	APPD.
-1	8702	5-24-57	PAK

-20 -19 -18 -17 -16 -15 -14 -13 -12 -11 -10 -9 -8 -7 -6 -5 -4 -3 -2 -1

LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

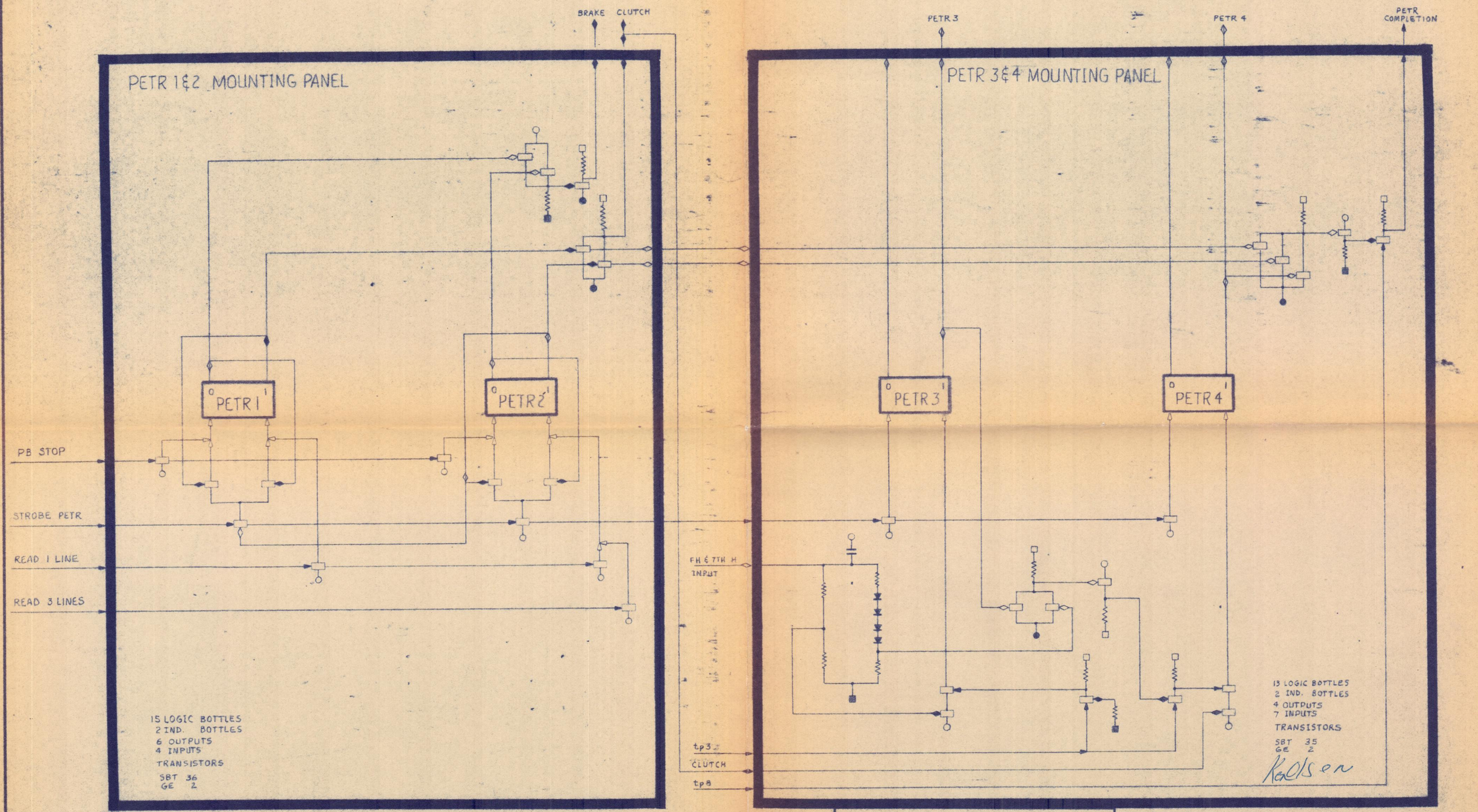
PBS, IOS CONTROL, TX-0 BLOCK SCHEM.

SCALE:
DR. C.A. NORMAN 1/10/56
ENG. 10-10-56 C.A. Norman
CK. 6-12-57 R. ORO
APPD. 10-10-56 C.A. Norman

C-67878

C-67882

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY



GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
K Olsen 10/26/56 GRADE III FINAL DESIGN
GRADED BY: DATE:

CHG.	CN#	DATE	APPD.
-1	8814	4-30-57	CAH
-2			
-3			
-4			
-5			
-6			
-7			
-8			
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-10			
-11			
-12			
-13			
-14			
-15			
-16			
-17			
-18			
-19			
-20			

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.

LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

PETR CONTROL, TX-0, BLOCK SCHEMATIC.

SCALE: DR. DARFENUK

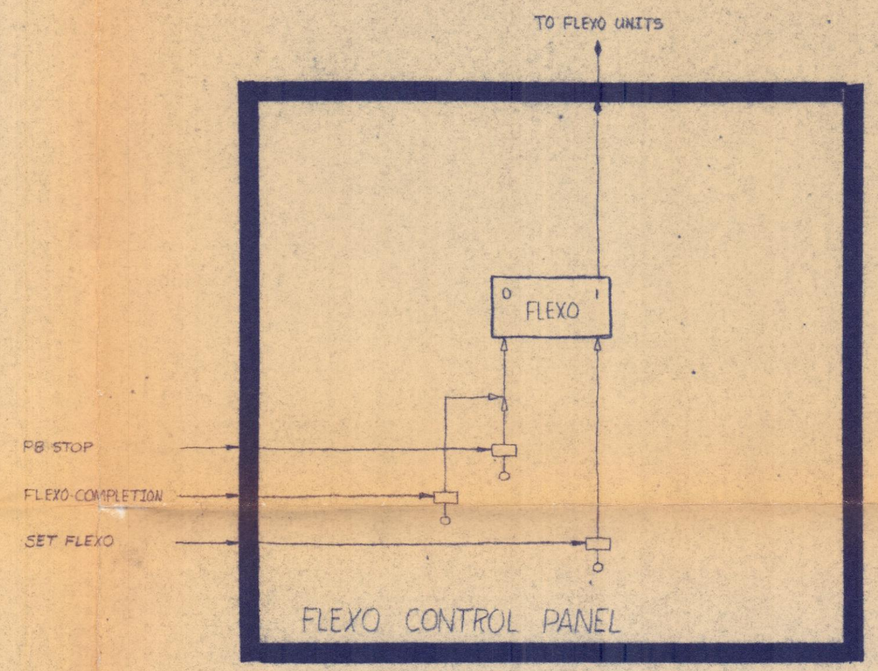
ENG. 10-10-56 C G Norman | CK. 5-9-57 A. GRIFFIN | APPD. C G Norman 10-10-56

C-67882

PATENT ISSUED MAY 20 1957

C-67875

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY



3 LOGIC BOTTLES
1 INDICATION BOTTLE
3 INPUTS
1 OUTPUTS
13 SBT's
1 GE

PRINT ISUED
OCT 16 1956

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE: 10/15/56

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.

LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

FLEXO CONTROL PANEL, TX-0 BLOCK SCHEM.

SCALE: DR. C.A. NORMAN 5-10-56
ENG. 10-10-56 C.A. Norman CK. APPD. 10-10-56 C.A. Norman
C-67875

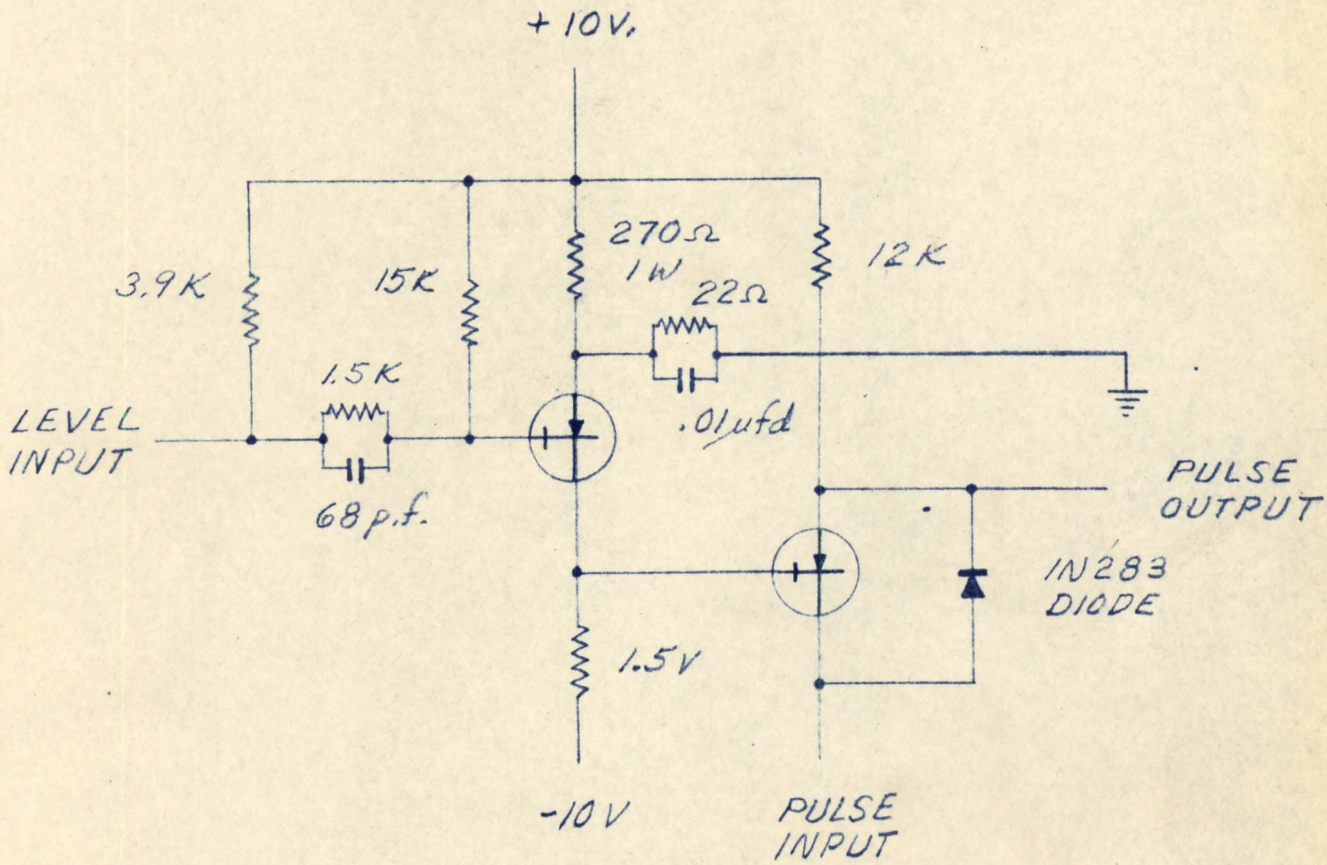
CHG.	CN#	DATE	APPD.
-20			
-19			
-18			
-17			
-16			
-15			
-14			
-13			
-12			
-11			
-10			
-9			
-8			
-7			
-6			
-5			
-4			
-3			
-2			
-1			

4M-7-54-Boston Blue Print

SA 65105

CIRCUIT SCHEMATIC.

REGISTER DRIVER.



INPUT FROM E.F. GATE ONLY.

PRINT ISSUED
JAN 24 1956

12-20-55

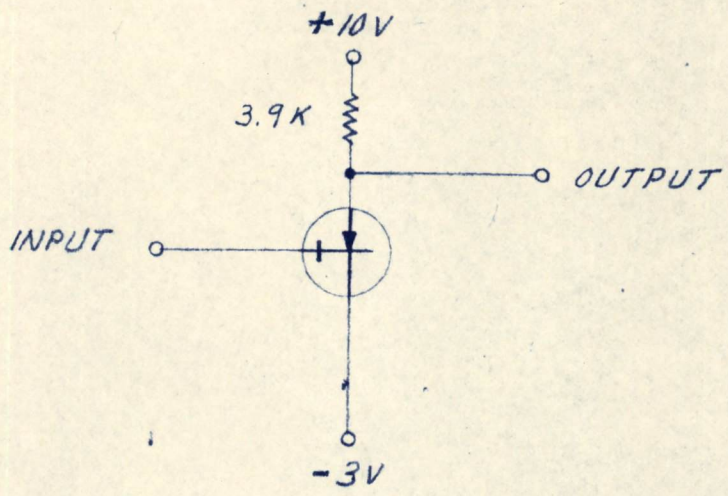
SA 65105

SA-65106

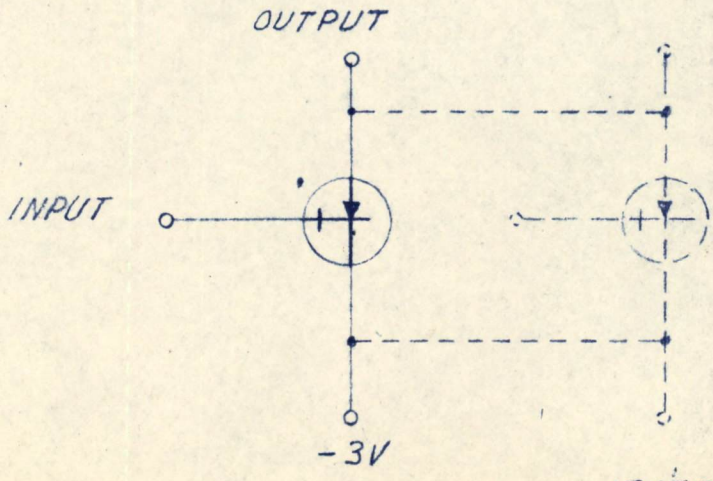
CIRCUIT SCHEMATIC.

EMITTER-FOLLOWER.

TYPE A. AMPLIFIER.



TYPE B. GATE.



OTHER E.F.s

PRINT ISSUED
JAN 24 1956

12-20-55 DP

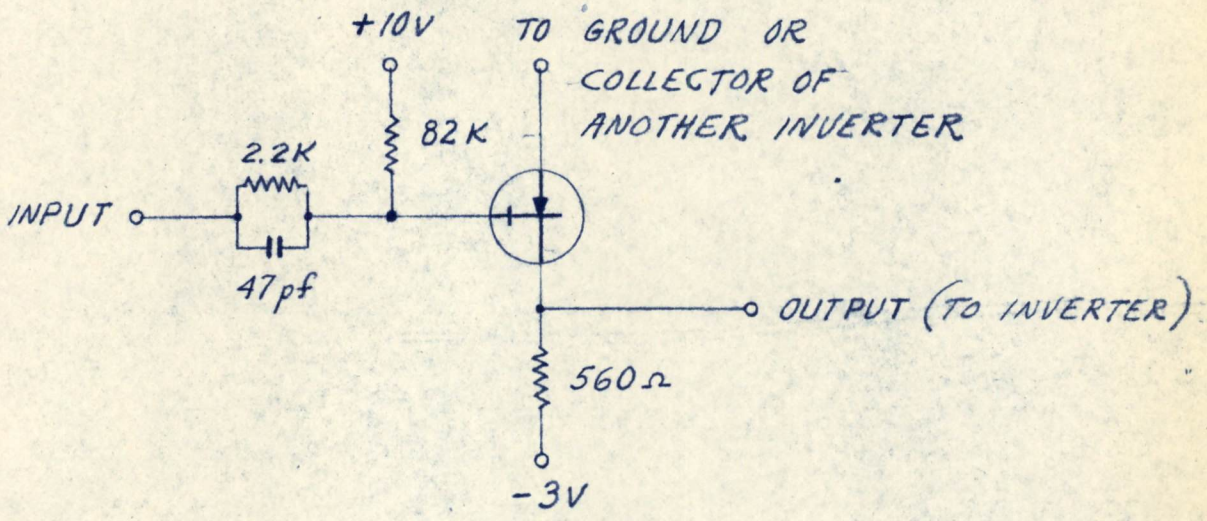
SA-65106

SA-65107

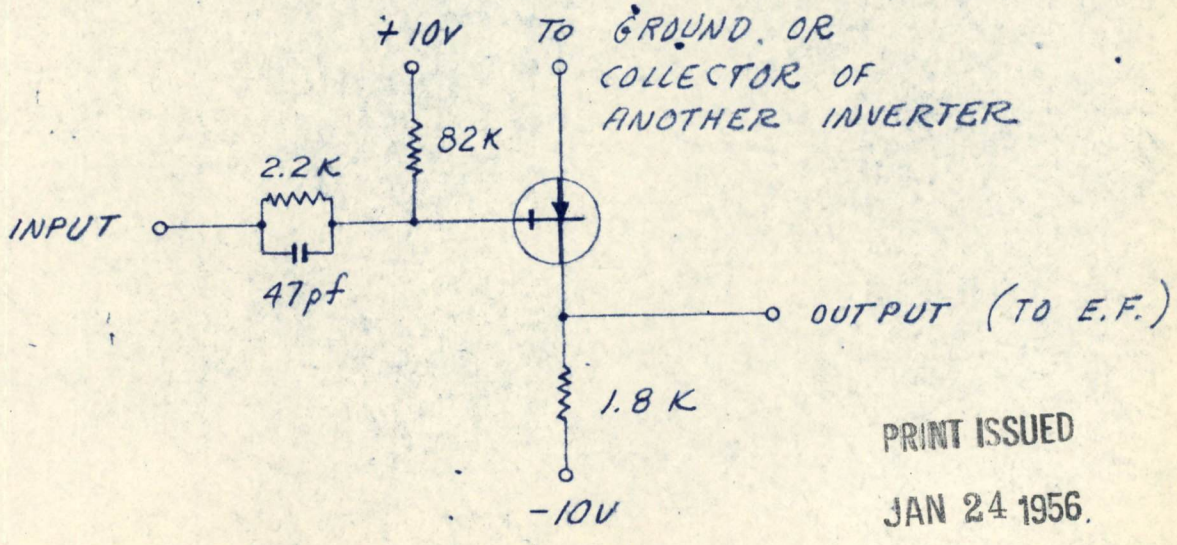
CIRCUIT SCHEMATIC.

INVERTER.

TYPE A.



TYPE B.



PRINT ISSUED
JAN 24 1956.

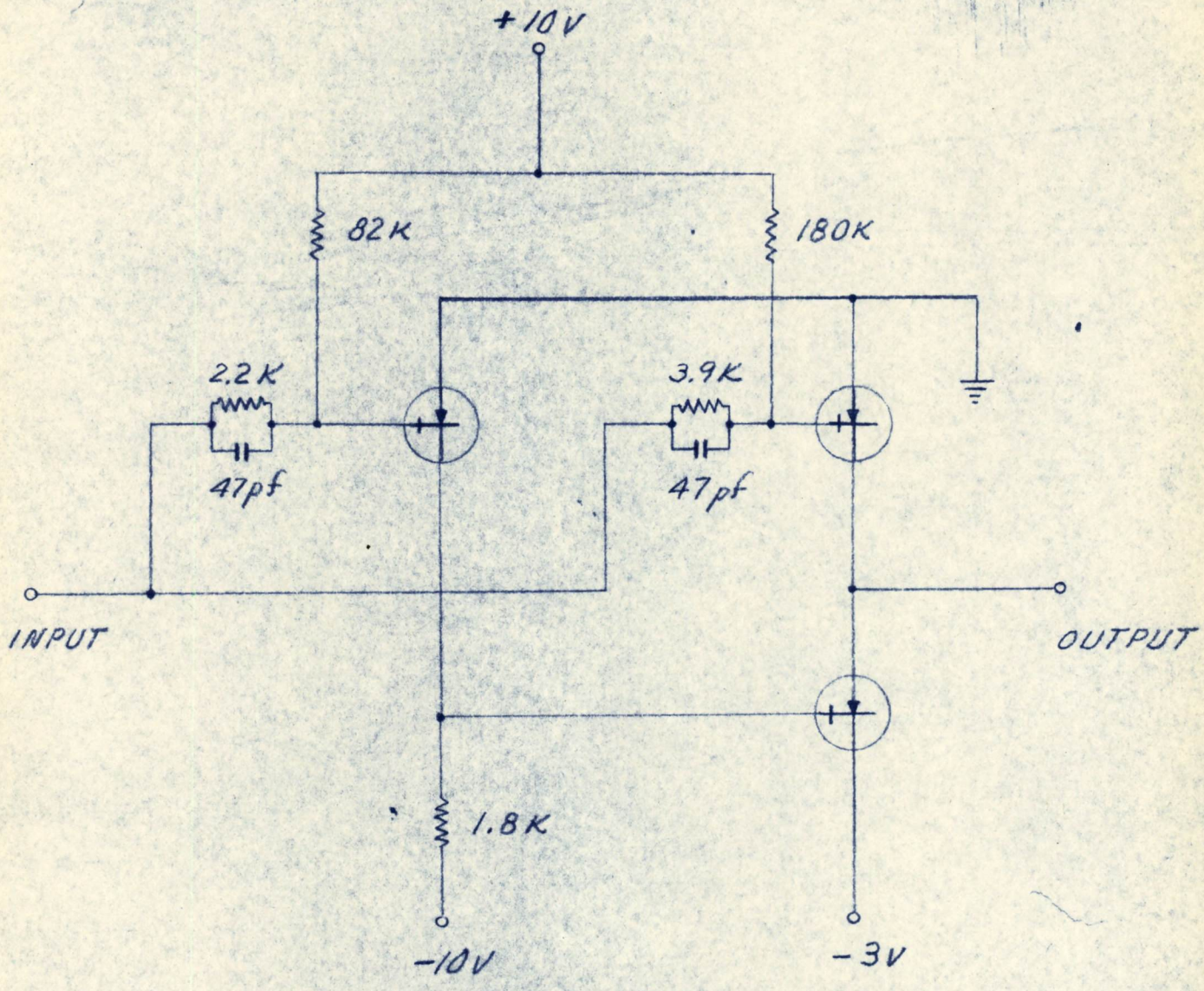
12-20-55 80

SA-65107

SA-65108

CIRCUIT SCHEMATIC

INVERTING CASCODE.



PRINT ISSUED
JAN 24 1956

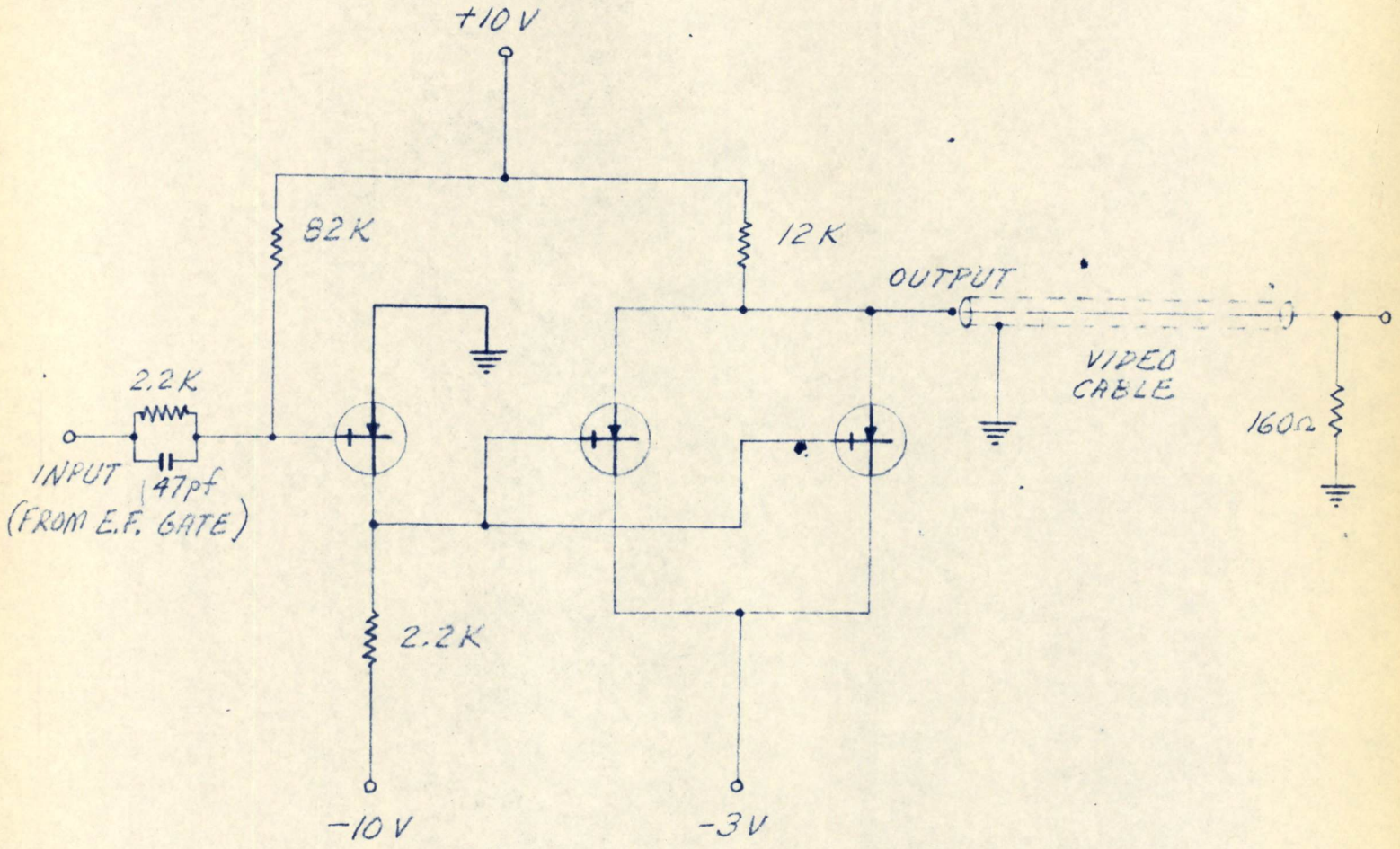
12-20-55 dsp

SA-65108

SA-65109

CIRCUIT SCHEMATIC.

CABLE DRIVER.



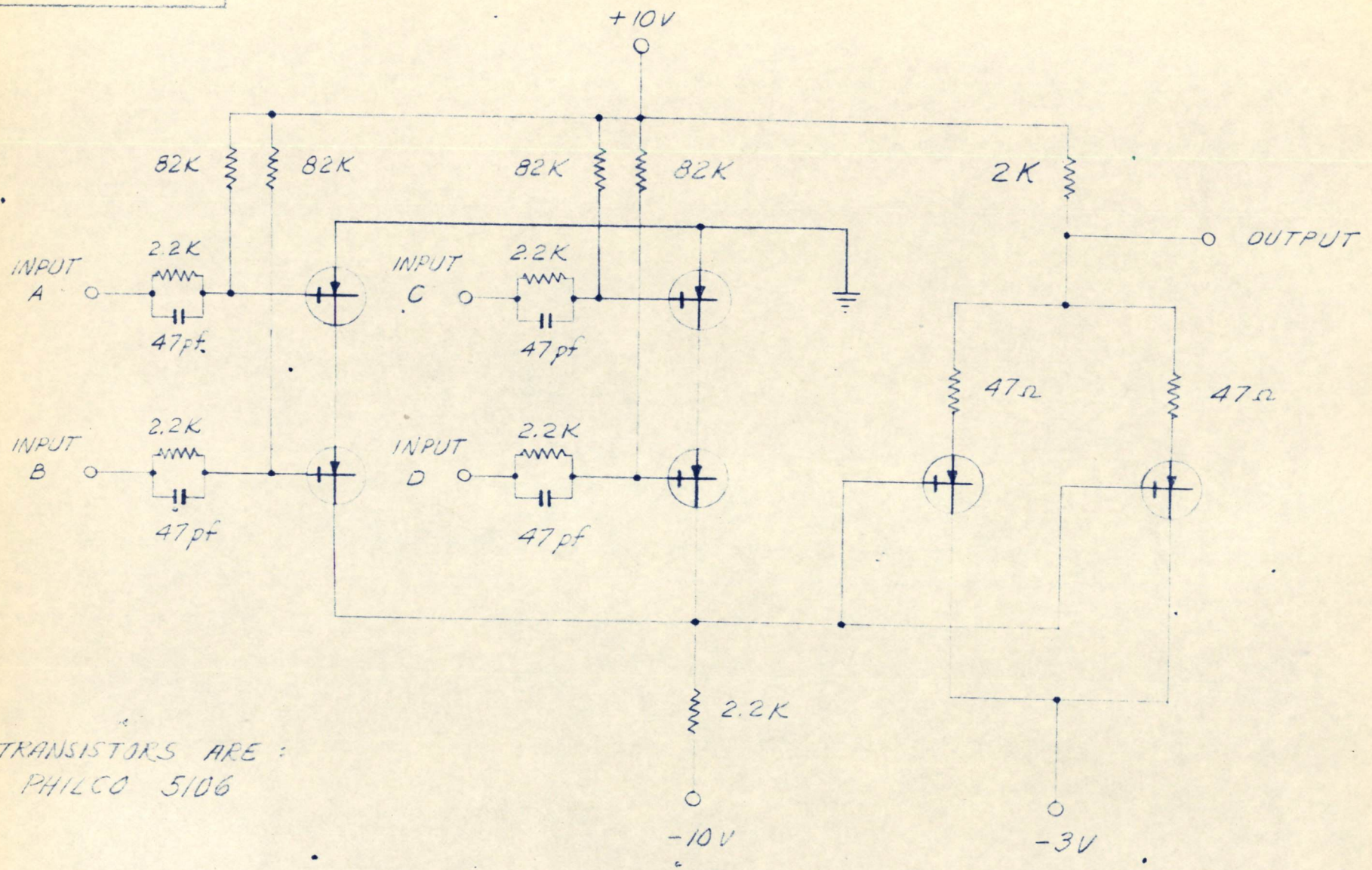
N.B. TERMINATE CABLE IN 160Ω
POSITIVE BIAS RES. AT LEVEL AMPLIFIER = 68K

PRINT ISSUED
JAN 24 1956

12-30-55 dd

SA-65109

SA-65 110



TRANSISTORS ARE :
PHILCO 5106

PRINTED
JAN 24 1956

INVERTER CARRY-CHAIN
CIRCUIT FOR ACCUMULATOR

J. FAIMAN 1-20-56

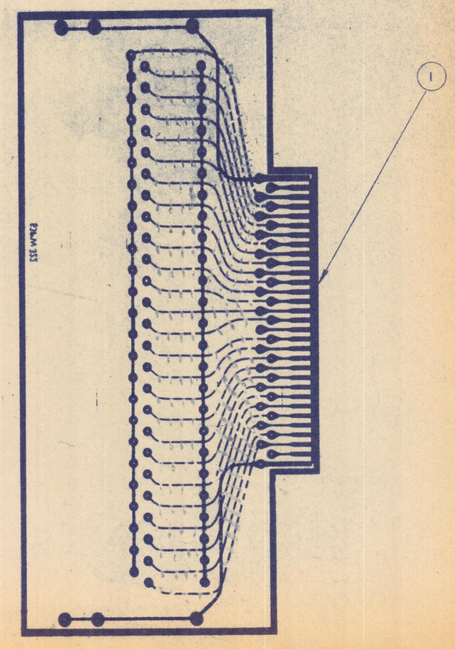
SA-65 110

D-74021

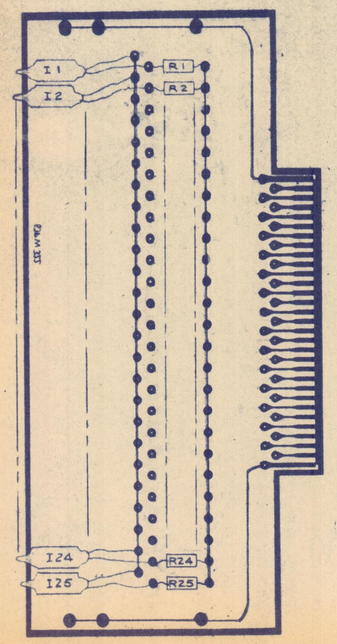
TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± 1°
DIMENSIONS ENCLOSED THUS (.000) FOR REFERENCE ONLY

USED ON ASSY., E-65497

COMPOSITE

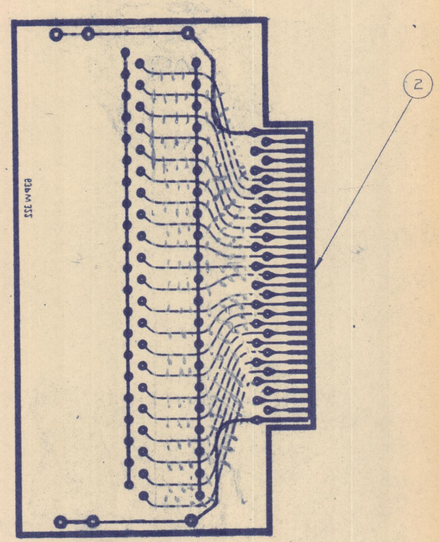


COMPONENT

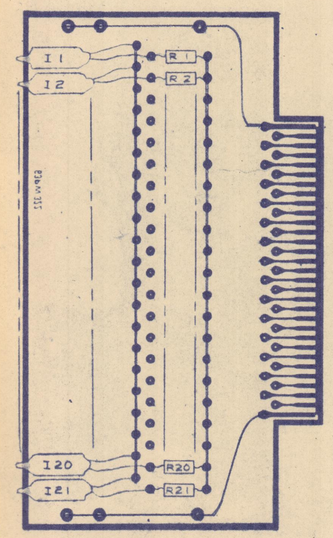


DETAIL "A"
SCALE 1:1

COMPOSITE

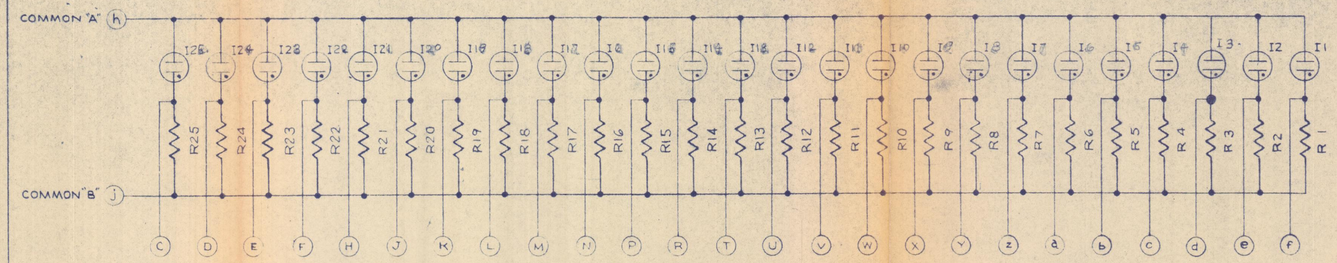


COMPONENT



DETAIL "B"
SCALE 1:1

SCHEMATIC



(A). INDICATORS ARE NE2A
(B). RESISTORS ARE 47,000 OHM ½ WATT

PART (1) AS SHOWN IN DETAIL "A"

PART (2) AS SHOWN IN DETAIL "B".

PART (3) AS SHOWN IN DETAIL "B" WITH INDICATOR LIGHTS # 1, 4, 5, 6, 10, 11, 12, 13, 17, 18, 19, 21 OMITTED.
PART (4) AS SHOWN IN DETAIL "B" WITH INDICATOR LIGHTS # 1, 3, 6, 7, 10, 11, 15, 16, 21 OMITTED.

PRINT ISSUED
MAR 20 1957

K. Olsen

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: K Olsen DATE: 3/19/57

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY
2	DETAIL, ETCHED IND. LT. PANEL LL		
1	DETAIL, ETCHED IND. LT. PANEL LL		

CHG: 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
CHG | DATE | APPD

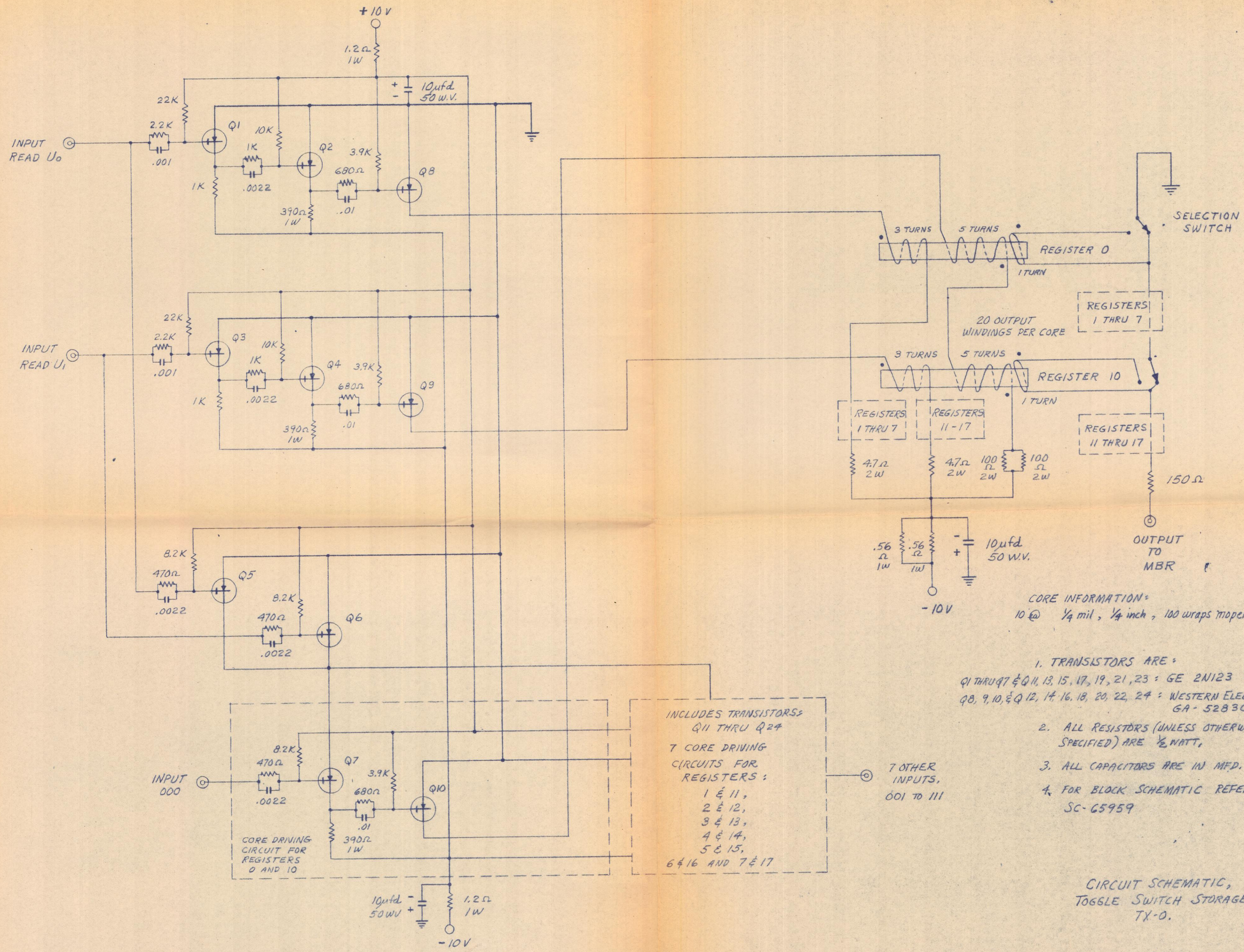
LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

SUB-ASSY., & WIRING DIAGRAM, COMPOSITE & COMPONENT, PIU INDICATOR LIGHT PANEL, TX0

SCALE: 1:1 | DR. V. PARZIALE 12/20/56
ENG. 3-19-57 C.A. Norman | CK. G.F. Heller 3-13-57 | APPD. 3-19-57 C.A. Norman

D-74021

Sc 65932



CORE INFORMATION:
10 @ ¼ mil, ¼ inch, 100 wraps moperm

1. TRANSISTORS ARE:
Q1 THRU Q7 & Q11, 13, 15, 17, 19, 21, 23: GE 2N123 (14)
Q8, 9, 10, & Q12, 14, 16, 18, 20, 22, 24: WESTERN ELECT. GA-52830. (10)
2. ALL RESISTORS (UNLESS OTHERWISE SPECIFIED) ARE ½ WATT.
3. ALL CAPACITORS ARE IN MFD.
4. FOR BLOCK SCHEMATIC REFER TO: SC-65959

CIRCUIT SCHEMATIC,
TOGGLE SWITCH STORAGE,
TX-0.

JOHN ACKLEY 4-25-56

Sc 65932

C-67880

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY

TO S/S CONTROL PANEL

CYCLE COUNTER MOUNTING PANEL

°CYCLE'

PB TEST

PB READ IN

'REPEAT' or C'

SET TO CC°

'READ' C'

'TEST°

IR'₀

IR°₀

C°

SET TO NORMAL

AC°₀

SET TO CC'

IR'₁

IR°₁

tp 8

20 LOGIC BOTTLES
1 IND. "
6 OUTPUTS
14 INPUTS
TRANSISTORS
42 SBT'S
1 GE

TO CONTROL

°READ'

°TEST'

R°T'

11 LOGIC BOTTLES
2 IND. " "
7 OUTPUTS
3 INPUTS
TRANSISTORS
33 SBT'S
2 GE'S

READ-TEST FF MOUNTING PANEL

PRINT ISSUED
APR 23 1957

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: K. Olsen DATE: 11/6/56

K-Olsen

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.

LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

CYCLE, READ & TEST CONTROL, TX-0 BLOCK SCHEM

SCALE: DR. C A NORMAN 2/9/56
ENG. 10-10-56 C.A. Norman CK. APPD. 10-10-56 C.A. Norman

C-67880

CHG.	CN#	DATE	APPD.
-1	8691	4-13-57	

67873
C-

TOLERANCES ◇ TO CONTROL ◇ UNLESS OTHERWISE SPECIFIED

DIMENSIONS ENCLOSED THUS .000 FOR REFERENCE ONLY

◇ TO CONTROL ◇

30 LOGIC BOTTLES
11 OUTPUTS
5 INPUTS
TRANSISTORS
41 SET'S

IR CONTROL MOUNTING PANEL

$IR_0^0 \cdot IR_1^0$ (STORE)

$IR_0^0 \cdot IR_1^1$ (ADD)

$IR_0^1 \cdot IR_1^0$ (tn)

C^1 23

C^0 25

tp 5 18

A^0 13

$PC_2 EC$ 21

SADEC 22A

17 20 13 16 15 12

27 IR_0^0 IR$_1^0$ STORE

11 $IR_0^0 \cdot IR_1^1$ (ADD)

10 $IR_0^1 \cdot IR_1^0$ (tn)

8 OP·C^1

9 A^0·OP·C^0

TO CONTROL

17 22 21 14 13 12

15 LOGIC BOTTLES
2 INQ " "
6 OUTPUTS
10 INPUTS
TRANSISTORS
37 SET'S
2 GE'S

IR FF MOUNTING PANEL

^{0}IR 0^1

^{0}IR 1^1

COMPLEMENT IR

PB READIN 27

SET TO tn

MBR→IR^1

C^0 25

10 11 8 9 23 15

MBR_0^0 MBR_0^1 MBR_1^0 MBR_1^1 READ^1 tp 6

PRINT ISSUED
MAY 28 1957

K. Olsen

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN

CHG.	CN#	DATE	APPD.
1	8898	5-23-57	CN

MATERIAL - DESCRIPTION	PART NO.	QTY.

LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

IR CONTROL, TX-0 BLOCK SCHEMATIC

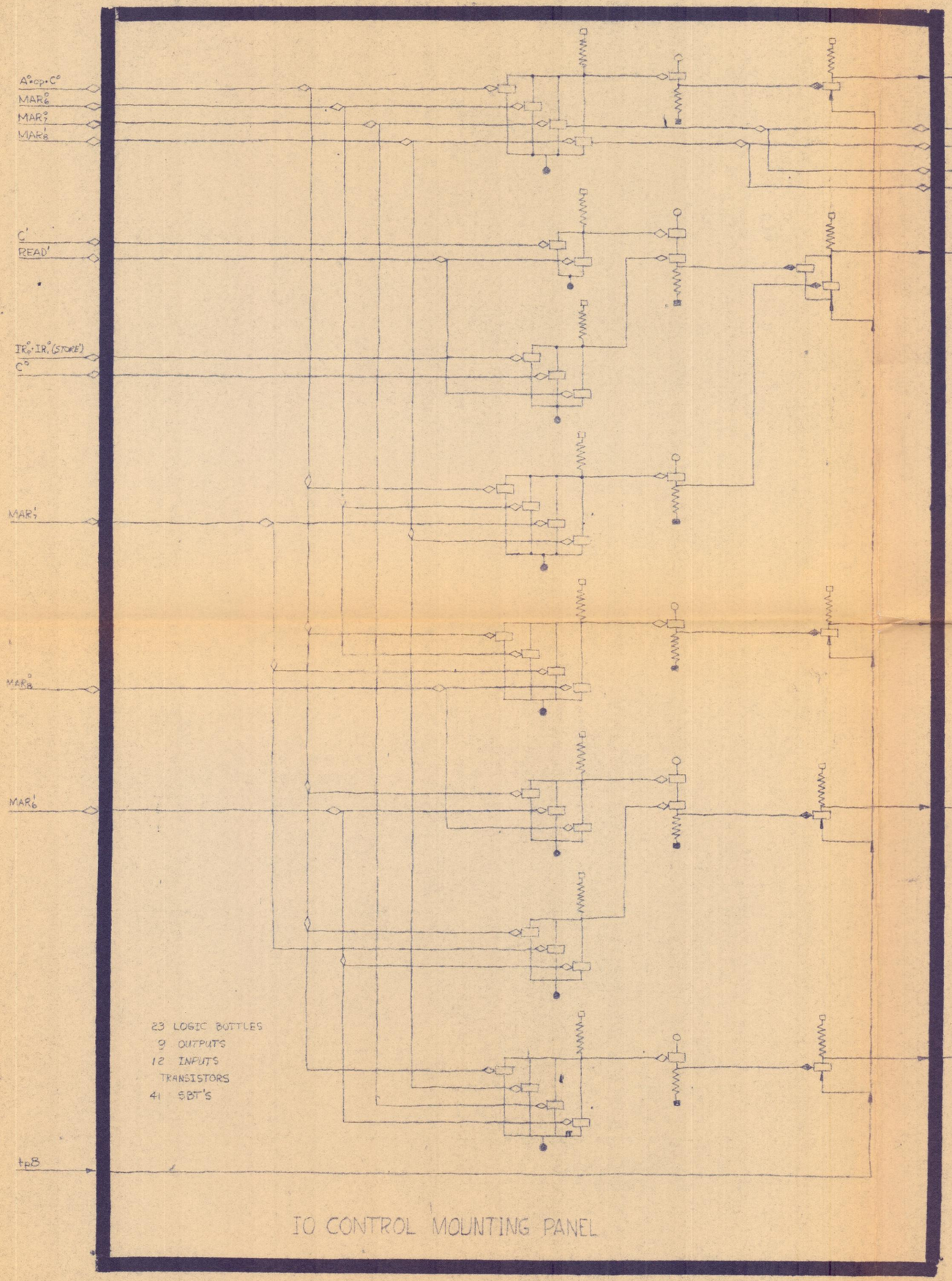
SCALE:
DR. C A NORMAN 5-10-56
ENG. 10-10-56 CG Norman
CK.
APPD. 10-10-56 CG Norman

C-67873

4M-7-54 Boston Blue Print

C-67876

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY



IO CONTROL MOUNTING PANEL

PRINT ISSUED
OCT 16 1956

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE: 10-16-56

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.

LINCOLN LABORATORY DIV. 6.
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

IO CONTR PANEL, TX-0 BLOCK SCHEMATIC

SCALE: DR. C.A. NORMAN 9/1/56
ENG. 10-10-56 C.A. Norman CK. APPD. 10-10-56 C.A. Norman

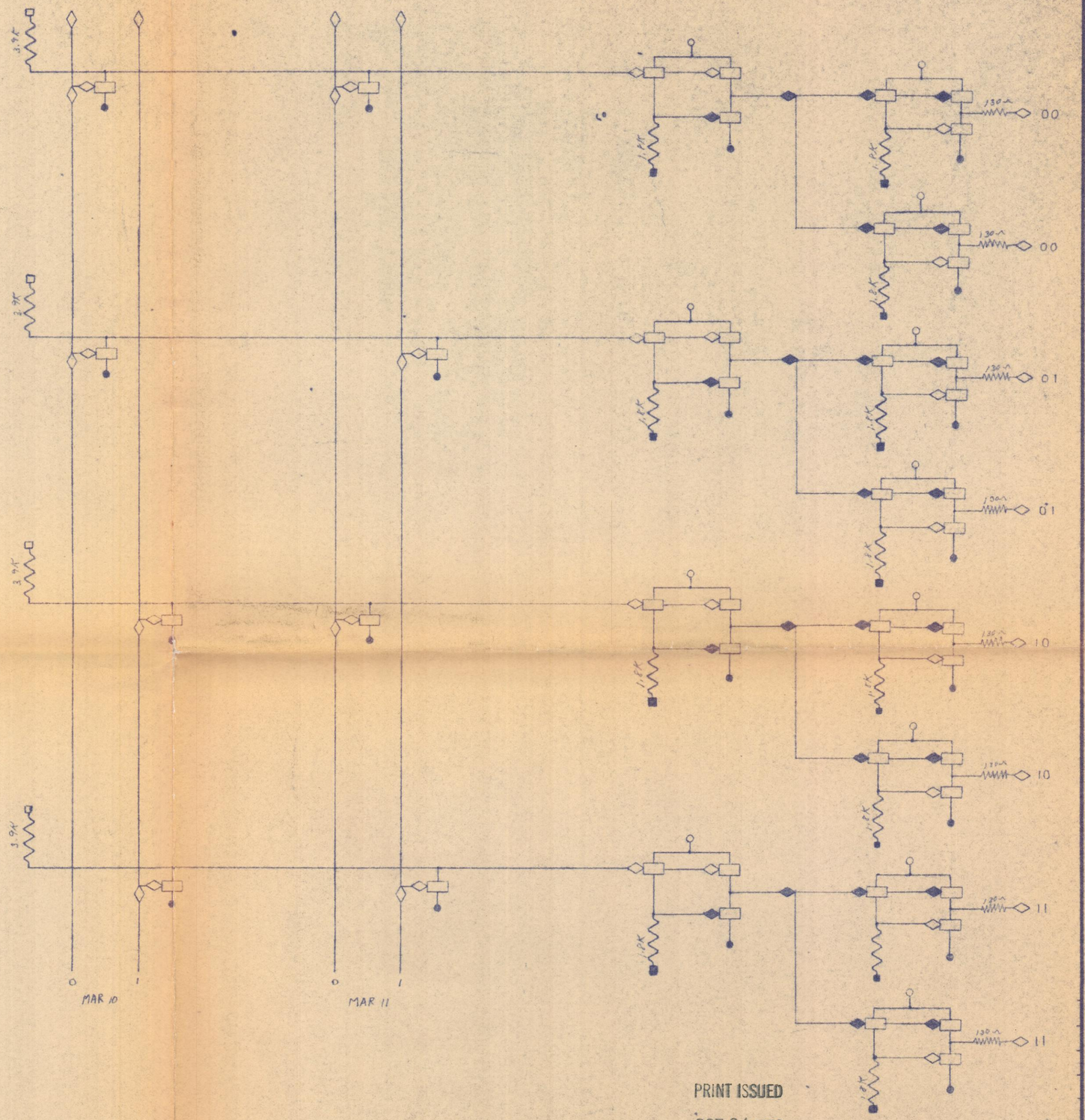
C-67876

CHG. | CN# | DATE | APPD.
-20 -19 -18 -17 -16 -15 -14 -13 -12 -11 -10 -9 -8 -7 -6 -5 -4 -3 -2 -1

4M-7-54-Boston Blue Print

SC-68025

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY



PRINT ISSUED
OCT 24 1956

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE:

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.

CHG.	-20	-19	-18	-17	-16	-15	-14	-13	-12	-11	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1
CN#																				
DATE																				
APPD.																				

LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

INHIBIT SELECT. PANEL, TX-0 BLOCK SCHEMATIC

SCALE:	DR. E. Harwood 10-23-56	
ENG. 10-23-56 E. Harwood	CK. 10-23-56 C A NORMAN	APPD. 10-23-56 C A NORMAN

SC-68025

4M-7-54-Boston Blue Print

RESTRICTED

PROPOSAL FOR BLOCK SYMBOLS AND DIAGRAMS

These Diagrams will be called "Block Diagrams".

1.0 A decimal classification system will be used similar to those used on the 701 and WWI computers.

1.1 Each page will cover one logical division.

1.2 It is extremely important to avoid having any pluggable unit partly on one page and partly on another. Where a pluggable unit must be split between several pages, notes must be added to show, on each such page, the pages where the rest of the pluggable unit is found. All blocks in a given pluggable unit will be shown on one page and enclosed by a line composed of alternate long and short dashes. The type and location of the pluggable unit will be shown only once within this broken line. Pluggable unit pin conections will be shown wherever a signal line crosses a broken line. Each line coming in or going out of a page will be identified by a functional name and a page on which the source or destination of the line may be found. Only one page number will be shown on incoming lines but each destination page will be shown on outgoing lines. Where the number of destinations is great they may be shown in a table.

1.3 Each major division of the transition system equipment will be assigned a two digit number for numbering the circuit pages.

The following numbers have been assigned.

01. Memory
02. Arithmetic Element
03. Program Control
04. Arithmetic Control
05. In-Out Control
06. Maintainence Control
07. Central Power Supply
10. Input Buffer System
11. Output Buffer System
12. Display Generation
13. Display Buffer System and Auxiliary Memory
14. Scope Consoles
15. S.D.V. Input
16. Magnetic Tape Unit

Numbers have not been assigned to Input-Output equipment for operations room and computer room and to remote transmitter.

A further breakdown of these numbers will be made by the person in charge of each group.

For example, page number 02. will show a breakdown of the Arithmetic Element

Page 02.01 may show one register of the Arithmetic Element.
Page 02.01.01 may show a part of this register.

2.0 Diagrams using block symbols will evolve through three phases by successive changes. Depending upon the particular circumstances, these phases may be combined.

2.1 In the first phase diagrams will be drawn showing only the elements which are necessary for a logical understanding of the circuit. Items such as cathode followers and buffer amplifiers are ordinarily omitted from this phase. These diagrams will correspond to the block diagrams on WWI. At IBM they are normally known as logical block diagrans.

2.2 The second phase diagrams will be created by redrawing the first phase and inserting blocks which were previously omitted. At this point the first phase diagrams will be rendered obsolete and will not be maintained thereafter. Variations of circuit will be decided upon such as load resistors of cathode followers.

2.3 The third phase will consist of dividing up the diagram into pluggable units and adding pin numbers.

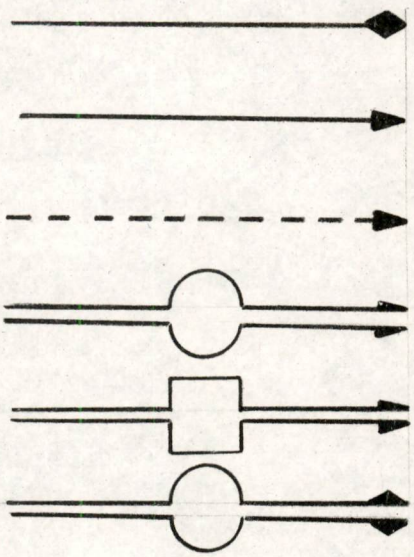
Phases 2 and 3 correspond to IBM System Diagrams, or WWI block schematics

3.0 There has been some discussion as to whether or not it will be necessary to have circuit diagrams of the individual pluggable units in either block or schematic form. The two alternatives are presented here and comments or opinions are requested.

3.1 Since, as mentioned in paragraph 1.2, all blocks in a given pluggable unit will be shown on one page, this page could be used for finding troubles within a unit. This would require the third phase diagrams to show the location of each block within the pluggable unit and the particular variation of circuit. For instance, instead of indicating that a certain block is a cathode follower, it would be necessary to show the type of cathode follower and location of the tube within the pluggable unit. This proposal would make separate diagrams of the pluggable units unnecessary.

3.2 If separate block or schematic diagrams of the pluggable units are provided, the systems diagrams will be much simpler because it will be possible to leave off the location of a circuit within a pluggable unit and other notations which indicate variations within circuits. There is an added fact that the Air Force may require schematic diagrams of pluggable units. In this case, the two types of diagrams might be called 'System Diagrams" and "Pluggable Unit Diagrams".

4.0 Signal Lines

4.1 

Single Channel Line (D C Level Signal)

Single Channel Line (Information Pulse Signal

Single Channel Line (Command Pulse Signal)

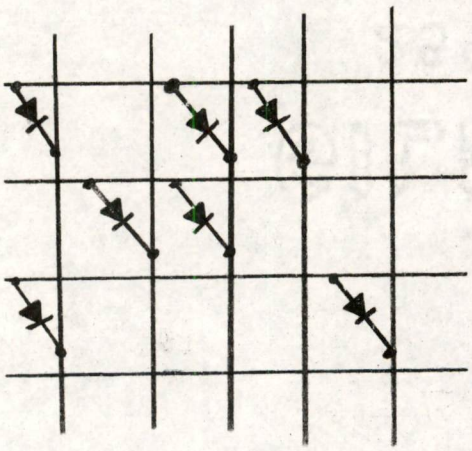
Multiple Channel Lines (Pulse Signal)

Same as above, but pulsed at different times

Multiple Channel Line (D C Level)

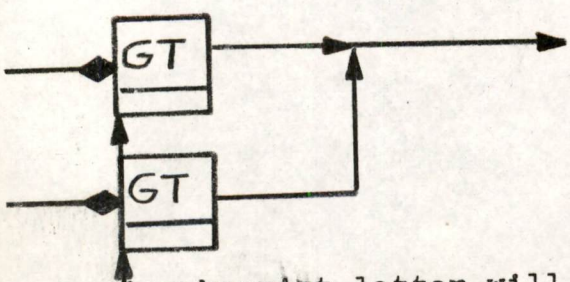
Signal lines shall be seperated by at least 1/4 inch.

4.2 All AND and OR switches will be shown as blocks. In case of a complicated matrix which is too involved to be easily resolved into combinations of AND and OR circuits, diodes will be drawn in to show the connections between lines of information.

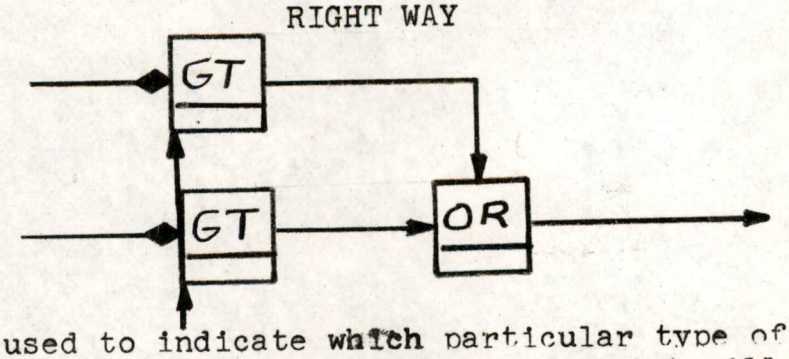


Any logical OR function will be shown as a block regardless of whether it is a diode switch or simply a connection of the out-puts of two circuits

WRONG WAY



RIGHT WAY

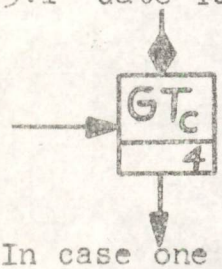


A subscript letter will be used to indicate which particular type of a given basic circuit is to be used. For diode switching, the subscript will refer to the value of the load resistor

5.0 Block Symbols and Dimensions

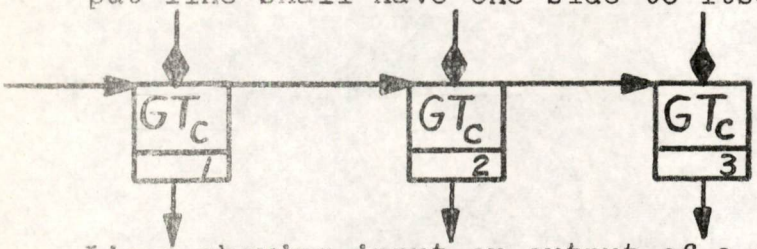
In this proposal it is assumed that diagrams of pluggable units are not to be drawn. If it is decided to provide these diagrams, the same symbology will be used except that the location of the circuit within the unit (and perhaps the subscript indicating the type of circuit) will be omitted.

5.1 Gate Tube



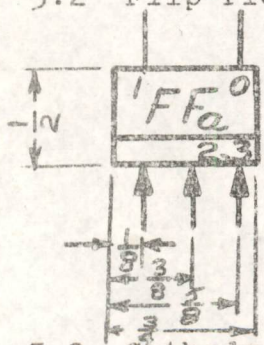
The block shall be 1/2" by 1/2". The letters GT shall be 3/16" high. The lower case subscript C indicating a certain type of gate tube will be 1/8" high. The number 4, indicating that this circuit uses tube #4 in the pluggable unit, is 1/8" high.

In case one input line feeds into several gate tubes, the input line shall be drawn coincident with one side of the block as shown below. The output line shall have one side to itself and it shall be centered on that side.



Lines showing input or output of a gate tube may be shown on top, bottom or either side.

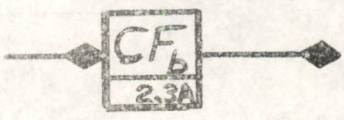
5.2 Flip-flop - The dimensions of the flip-flop will be as shown.



The output indicated by a zero is the output of the side which is rendered non-conducting by a "clear" pulse.

The letters FF are 3/16" high. The numbers indicating which tubes are used are 1/8" high, as well as the 1 and 0 and lower case subscript.

5.3 Cathode Follower



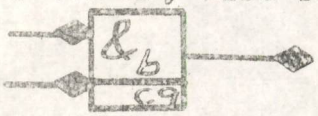
Letters CF will be 3/16" high. Lower case letter indicating type of cathode follower will be 1/8" high. Tube location numbers will be 1/8" high. Number of cathode followers in parallel will be indicated by number of locations. (e.g. 2,3A indicates three half tubes or three cathode followers in parallel.)

5.4 AND Switches

"&" shall be 3/16"high. Lower case letter indicating type of AND circuit shall be 1/8" high. Length of block depends on number of inputs. Inputs shall be 1/4" apart and 1/8" from either edge. Minimum block dimensions shall be 1/2" x 1/2".

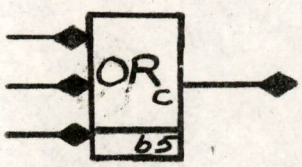
Letter and number in lower part of block are 1/8" high and indicate location of junction of diodes and load resistor in pluggable unit.

Block may also be shown vertically.



Inputs may enter on from one to three sides of a block. Output must have a side to itself.

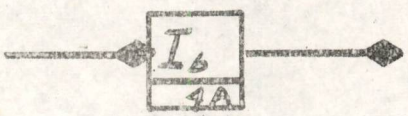
5.5 OR switches - Same dimensions and rules as listed for AND switches.



5.6 Buffer Amplifier

5.7 Delay

5.8 Inverter



Input may be on any side of block. Output must have a side to itself.

K. Olsen

February 10, 1954

S-6747

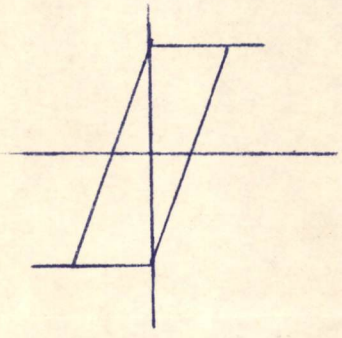
PROPOSAL FOR MEMORY SELECTION SYSTEM

Consider the problem of performing the selection for a magnetic core memory completely external to the memory itself.

1. Such a memory would require at least as much switch capacity as storage.

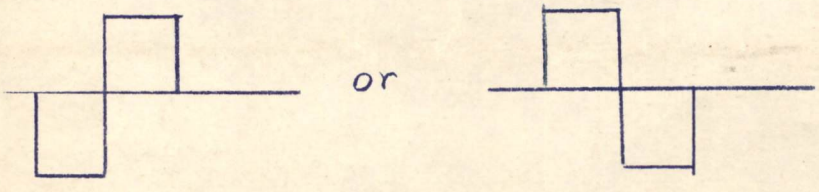
2. There would be no coincident-current limitations on the excitation a selected core could receive.

   a) Restrictions on the hysteresis loop of the core material are reduced. i.e., the loop below would be useable.



   b) The cycle time and read-out voltage are no longer limited to those of coincident-current operation.

3. Since a switch core cannot store information, (outside the limits of a single Read-Write cycle) we must always get a symmetrical sequence so that at the end of the cycle the core is restored to its original state. The cycle is then either:



4. Let us now consider a memory with external selection. The two possible sequences a core may be subjected to are:

   1) Read-Write$_1$

   2) Read-Write$_0$

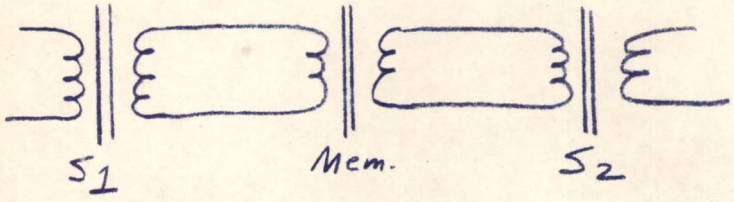
SA-5747

SA-5784S

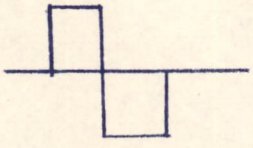
5. If we define plus excitation as being in the read direction, and minus as in the write, then sequency 1) requires a first pulse plus and a last pulse minus; sequence 2) requires a first pulse minus and a last pulse plus.

Based on the above, the following scheme then appears reasonable.

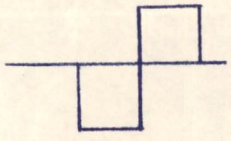
6. Consider a single digit plane consisting of switch planes and a memory plane. The secondaries of the switch cores each drive the memory core as below.



7. S_1 puts out

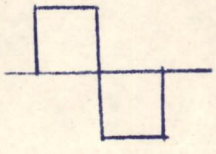


S_2 puts out

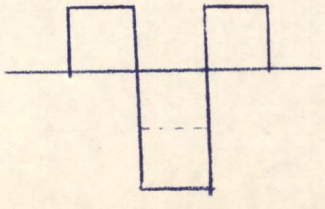


(polarity is with respect to memory core)

Then for sequence 1) $(R\text{-}W_1)$ we excite S_1 and leave S_2 inactive yielding net excitation



for sequence 2) $(R\text{-}W_0)$ we excite S_1 and follow it with S_2 yielding net of

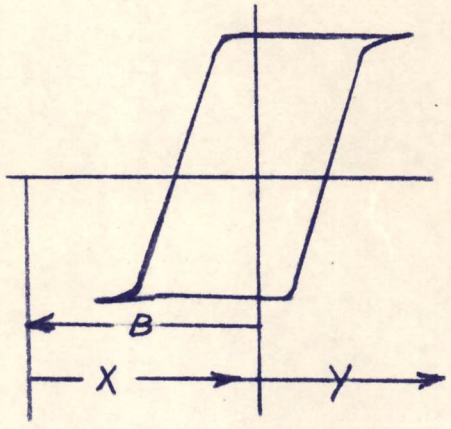


if we overlap for minimum time.

SA-5784S

SA-57747

8. Each of the switches could be of the same form as the present WW memory planes, (without a sense winding) the digit winding being used for putting on a d-c bias as shown below.

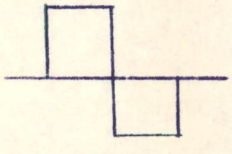


9. In order to R-W_0 we excite first S_1 and then S_2 .

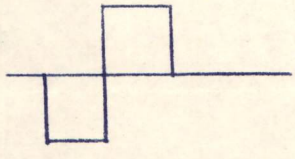
   To R-W_1 we prevent the switching of the digit by biasing the switch core$_2$ further off into saturation with a dynamic bias, thus preventing the second half of the cycle.

10. To save drivers it might be possible to put switches 1 and 2 in series and bias one off when the other is on but probably this is impractical. The coupling link between switch core and memory core should probably have enough resistance so that we can properly switch cores.

11. Another possibility is to have two register switches. One supplying



and the other supplying



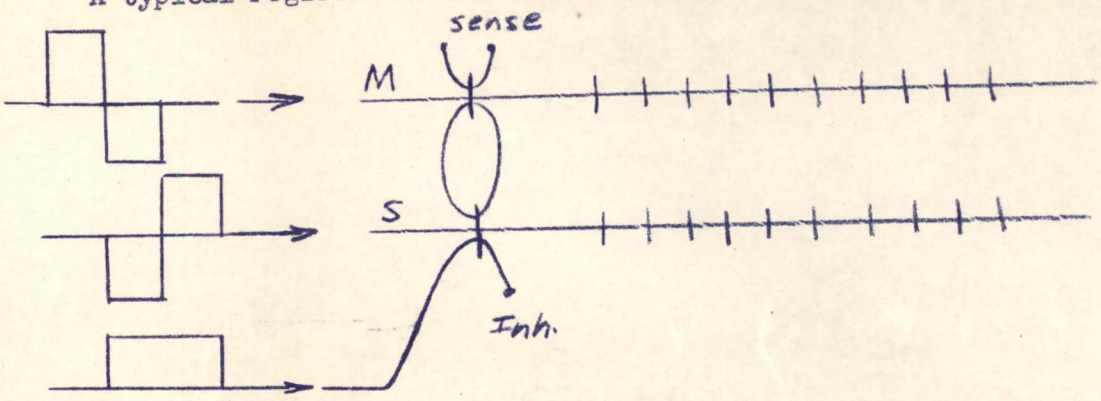
immediately after.

We can then have 2 planes (one containing switch cores and one memory cores) for each digit, connected by a coupling loop.

SA-57748

SA-5784

A typical register is shown below with the excitations on its lines



One register switch drives the memory plane which has only a sense winding. The other register switch drives the switch plane which has only an inhibit winding. Each memory core is then coupled to its corresponding core in the switch plane by a coupling loop.

In order to R-W_0 we turn on the register switches in succession and to R-W_1 on a particular core we merely inhibit on the appropriate digit switch plane and prevent the second register switch from affecting the state of the memory core.

This effectively gives us the same excitation cycles on the memory core as shown in 7.

Signed Jack Raffel
Jack Raffel

Read and Understood J L Mitchell

JR:cs

SA-5784

May 27, 1954

To: W. L. Jackman

From: J. E. MacDonald

Subject: Progress of Frame Testing - Instruction Control Element

1. The TPD has been installed and is running. This includes delivery of pulses to command generators. Only the parts of the TPD Control essential to this action have been checked out. The Operation Register, Class-Cycle Matrix, and Variation Matrix and Instruction Matrix are partially installed. This operation has been hampered by a lack of 6010, 6017, and 6013 Pluggable Units. Some rise and fall times from set of the Op Reg to Command Generator suppressor grids have been measured. A couple of these seem unsatisfactory but should be rechecked before starting to worry. With the present instruction list, only a few of these level shifts are critical.

2. A peculiar occurrence in the 6020 PU was noted. This PU consists of 2 [AFF driving 2CCF and 3CCF]. The catching diodes (to -30) on outputs of CCF's and the decoupling and parasitic resisters of CCF's were blown. +10 and -30 circuit breakers were found out after this happened. The same thing happened while Design Testing this unit. No explanation is offered as yet.

3. A possible explanation of 2, and a general problem in its own right is the fact that Power Module and Power System have no provision for sensing for lack of voltage.

4. The 6020 unit containing the TPD Ctrl FF has been observed to flip with no apparent trigger pulse. This will be subjected to further observation and reported on again.

5. It was decided to tag and store faulty components for possible future use by Components Group. A brief history will be noted where possible.

6. In several instances, The 1782A tube has to be wiggled in its socket to make contact. This appears to be a tube fault rather than a socket or socket mounting fault. We need desperately some replacement 1782A's for this and possibly other reasons.

7. In several instances, the taper pin which is inserted in the filament bus did not make contact with its wire. This is corrected by dropping solder into the joint between wire and pin, but could be caught by a continuity check of these wires before assembly.

8. PU 6024, X27, Loc CJ (TPD) has peculiar fall waveshape in that it tapers and does not fall sharply. This unit will be inspected on the Design Tester. It has been used as is because we have no spares.

9. Some TPD ring failures seem to be associated with moving the scope probe from one output point to another. This will be checked more thoroughly.

10. When the TPD and the 2mc command line are both running, the negative undershoot of every 16th output of the 2mc line is cut down significantly. This pulse is synched with IP-6. This of itself causes no trouble, but should be explained if possible.

11. In some Pluggable Units, the cam can be rotated 360°. This should be checked by PU inspector.

12. It has been decided to tie all unused diodes to +10 (8 circuits) or -30 (or circuits).

13. We understand the problem of unused pulse or diodes is being investigated by basic circuits.

14. A 5948 tube was found to have large mica or glass particles rattling loose in its envelope. Has been replaced.

15. Several pluggable units have been found with filament wire shorted to frame of PU. This occurs when card holding bracket screws are inserted and pierce filament wire insulation. Production Testers agreed verbally to check this with ohmmeter test but it could be eliminated by special care in assembly.

16. A diode in a PU Type 6013 (prototype) was found to be shorted (the diode itself).

17. The BPA which drives the 2mc command line (to a BRD) was driven for a time at 2mc with no tube load and, as per basic circuit specs, no terminating resistor. The pulse transformer (output of BPA) experienced severe overheating and deterioration of waveform. It is therefore recommended to all groups that BPA not be driven at 2mc without terminating. At lower frequencies the heating will obviously not be as severe but just what is a safe frequency under these conditions has not been determined. When the tube load (BRD) was inserted, the wave shape improved, but high amplitudes were observed. 38v into BPA gave 80v out (into BRD) Terminating BPA in 100Ω dropped output amplitude of BPA to 50v. Output of BRD under these conditions was:

1st output (7 units of load) First load 39v Last load 30v.

2nd output (9 units of load) " " 35v " " 30v.

Termination of BPA this way (when driving RD's) has tentative approval of Ray Nienburg.

18. In a few cases the Resistor Board mounting clamps have to pried out of the way in order to insert PU's. This could be avoided by more careful assembly of boards on panel.

19. In one instance, PU male plug did not make contact on all pins. It was necessary to scrape these pins to get contact.

20. Work schedule for next two weeks is

1st shift Shur, Muller; Heineck, Girgenti

2nd shift Hickey, Potocko

21. Indoctrination talks on frame for group leaders and others begin June 1.

22. Block schematics should go to Zappia June 1 for release.

23. We are still short 16 units. This will be critical soon.

J. F. MacDonald

COPIES: H. D. Ross
K. Olsen
" "

J.I.Raffel
8/13/56

KEN OLSEN

PROPOSAL FOR A MAGNETIC MEMORY USING THIN FILMS

Tests on thin magnetic films indicate that any memory system utilizing them to full advantage will have to overcome the following difficulties:

1. High selection currents at extremely short rise-times.
2. Large magnetically coupled noise pulses.

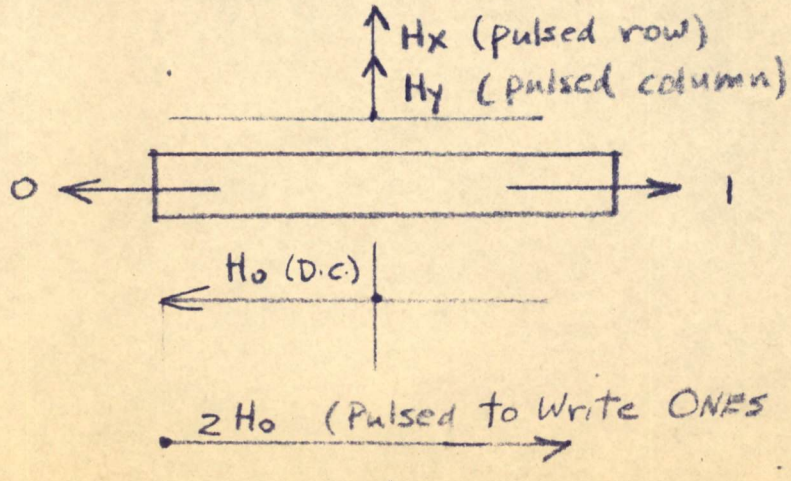
In designing a memory system, the following characteristics should be kept in mind:

1. The "read" requires no discrimination among digits, whereas the "write" does.
2. Noise output is only of importance during the "read" time.

Utilizing the fast switching characteristics of thin permalloy films when subjected to transverse fields, it may be possible to design a system which tends to minimize the noise problem, at the same time reducing the requirements for large quantities of high-current, high-speed selection circuitry.

Consider a three-dimensional array of small deposited film spots, all of which are subjected to a DC field of magnitude H_o along the easy axis of magnetization which will be arbitrarily designated as the "read" or "zero" direction. Each digit plane of this array is supplied with a current pulser capable of applying a field of $2H_o$ in the opposite or "write" direction, thus yielding a net excitation of magnitude H_o in this direction. Two other sets of fields are applied to the array. As in the conventional magnetic-core-memory of the Whirlwind type, pulsed excitations are applied to a single row, and a column of all planes in the array. The fields of these coordinate excitations X and Y are applied in the transverse magnetic direction and are of amplitudes H_x and H_y respectively. The limitations on amplitudes of applied fields are that $\vec{H}_o + \vec{H}_x$ and $\vec{H}_o + \vec{H}_y$ must be insufficient to reverse the magnetization of the film, whereas $\vec{H}_o + \vec{H}_x + \vec{H}_y$ must be sufficient to switch the film. Operation of such a memory is as follows:

Initially all films are subjected to a DC excitation in the "read" direction which is insufficient to cause all the cores to switch to the "zero" state.



Single Bit with Applied Fields

Simultaneous application to a row of a field $\vec{H}_x$ in the transverse direction and a column of H_y also in a transverse direction provide an excitation of $\vec{H}_o + \vec{H}_x + \vec{H}_y$ to the single spot at the intersection of the selected coordinate. This spot is switched to the zero state if it held a ONE, and its state is unchanged if it previously held a ZERO. During the "write" cycle, those digits in which a ONE is to be written are pulsed with a field of value $-2H_o$ thus subjecting a selected spot to an excitation of $-\vec{H}_o + \vec{H}_x + \vec{H}_y$ which switches it to the ONE state. In those digits in which ZERO will be written, the selected spot receives an excitation of $\vec{H}_x + \vec{H}_y$ and remains therefore in the ZERO state.

The detection of signals from such a Memory is accomplished by linking the spots with tightly coupled loops whose areas are perpendicular to the flux in the easy directions of magnetization.

The features of the system described above are:

1. The circuitry for bit selection (X + Y) supply only a fraction of the total switching field.

2. Only one set of coordinate drivers is used for both "read" and "write" (because these fields are applied in the transverse direction)

3. While there is considerable noise during the "write" cycle (all the cores are excited) during the "read" only the transverse transients are active, and since these fields are parallel to the direction of the pick-up loop, the coupling due to air at least is not present. (This does not take care of the flux change in material due to rotation.)

4. Since there is no need to turn on X and Y drivers between "read" and "write", the transient times normally associated with turn-off of "read" and turn-on of "write" are eliminated.

5. There is no need for pulse transformers since excitations on any one line are unidirectional.

Jack Raffel
8/13/56

jir:rs

Instruction Control Element

I Nomenclature

A. Signal Levels

1. Flip-flops are named for the positive action they condition and the positive condition is obtained from the 1 side of the flip-flop. e.g. "Pause" flip-flop is on 1 (1 side is at +10) for Pause condition; flip-flop is on 0 (0 side is at +10) for No Pause condition. For this reason, a few flip-flops are set to 1 when the "clear control FF's" is executed.

   These are: 1st wd ctr tnfr } 0.4.5.2
   2nd wd ctr tnfr }
   Time Level 0 – 0.4.7.2
   Divide Time Level 0 – 0.4.14.1

   A few flip-flops have "positive" action on both sides and here the 0 side is arbitrarily chosen as the side which should be up when "clear control FF's" is executed.

   These are: Program Time^0 - Operation Time$'$
   A^0 - B$'$

2. Conditions or signal levels for the command generators are obtained from several sources:

   a.) Directly from control FF's
   e.g. PT, B, etc.

   b.) Directly from CLASS lines
   e.g. MISC, MULT

   c.) "&" combinations of control and CLASS lines
   e.g. STORE OT A (read STORE & OT & A)

   d.) "&" combinations of control and CLASS and VARIATION lines e.g. tad PT (read tad & PT)
   Note: tad infers an "&" combination of ADD class and the particular VAR code which makes up the "twin and add" instruction.
   Note 2: A VAR output is never used directly to condition a command.

   e.) CLASS codes are as follows:
   MISC - Miscellaneous
   ADD - Add
   MULT - Multiply
   STORE - Store
   SHIFT - Shift
   BRANCH - Branch
   IO - Input - Output
   RESET - Reset

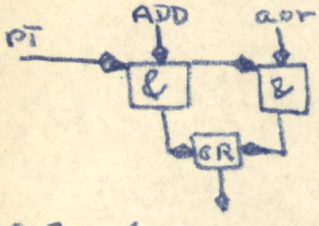
f.) Instruction codes are written in lower case letters using codes of H-106

e.g. hlt - program stop
add - add
aor - right add one

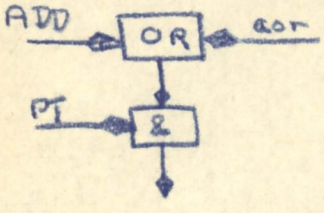
g.) Frequently, a condition to a command generator is obtained from an "OR" combination of conditions.

e.g. ADD PT, aor PT (Read ADD class & program time or right add one & program time)

Note: This nomenclature infers circuitry as follows:



Note 2: (ADD, aor)PT infers circuitry as follows:



Both types are found in the ICE but the first is usually preferred.

h.) Control condition nomenclature (not all inclusive)

SC ≠ 0 - step counter not equal to 0.
SC > 6 - Step counter greater than 6.
Ix, & bpx - "Branch and index" instruction & Index Reg # 1 selected
BRANCH & BR FF ON - Branch class & Branch Flip Flop ON. (on 1).

B. Pulses

1. Controls are provided in JPN Control (0.4, 7.2) to distinguish a Break cycle from a no Break cycle. Two sets of time pulse outputs are provided.

a) TP - Time Pulses - these are provided whenever the ring is running and are in fact used to step the ring. In other words they are available on a Break cycle or a no break cycle. They are sent also to the Selection & IO Control Element where they are further conditioned to become Break In (BI) pulses or Break Out (BO) pulses

Instruction Control Element

a Break cycle is called for by IO equipment.

b) IP - Instruction Pulses - These are actually no Break pulses. They are occasionally used directly to execute commands but more often are conditioned in the command generators.

Examples: ① IP 7 - a pulse occuring every 7 time as long as a Break is not in process.

② TPO - a pulse occuring every 0 time

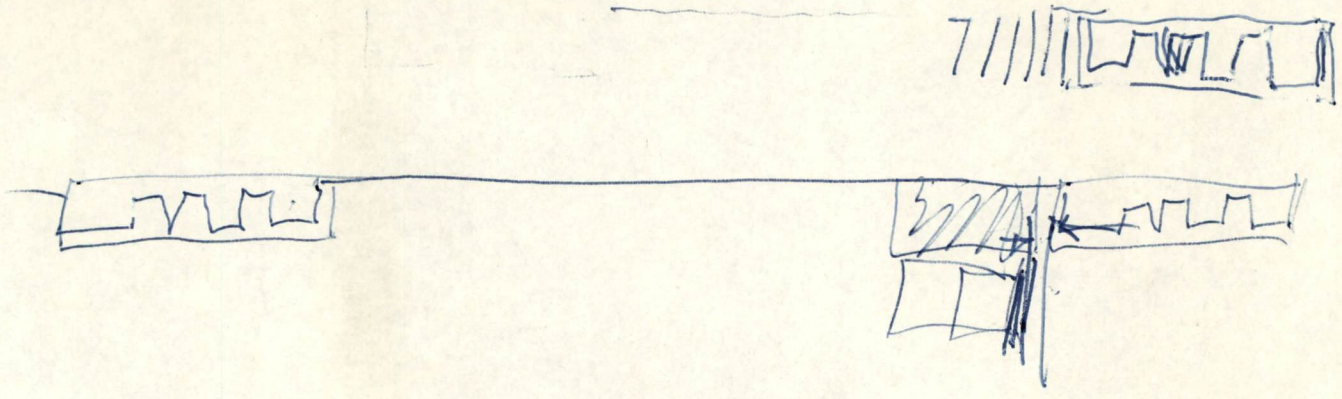
③ PT 6 - a pulse obtained from a command generator by applying IP 6 to the control grid and PT to the suppressor grid of a gate tube in the command generator.

④ aor OT 2 - a pulse obtained from a command generator by applying aor OT to the suppressor grid and IP 2 to the control grid

Note: It should be noted that since a gate tube is a special form of "and" circuit, the above notation is consistent with that used for signal level & circuits.

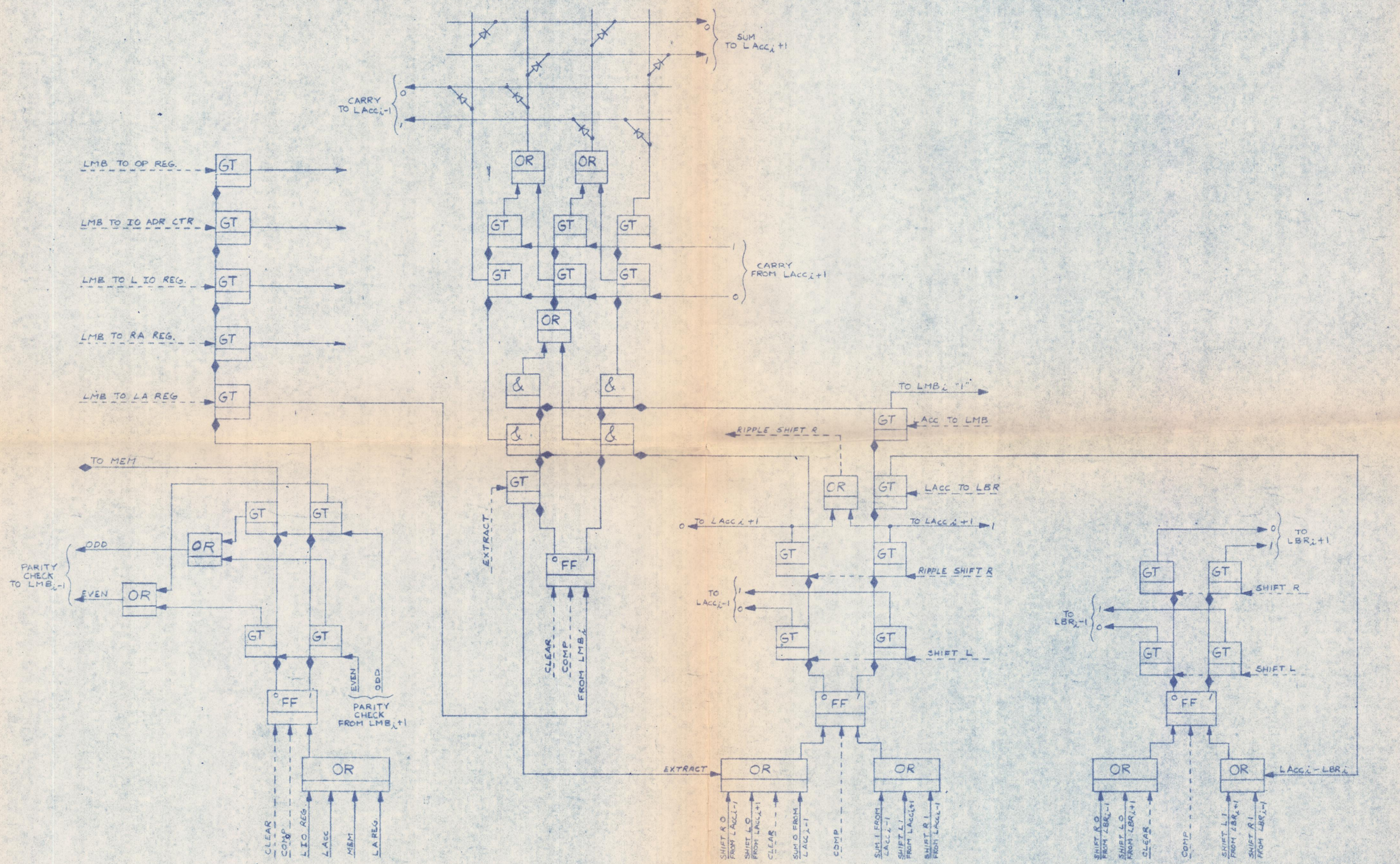
C. Commands

A command is in general a pulse output of the command generator. These commands have been numbered and described in other lists but the numbers have lost significance and may now be considered arbitrary. The now appear on timing diagrams and can be understood by reference to Command Descriptions if necessary.



STANDARDS CODE	RELEASED FOR ASSEM.	QTY.

PHASE I



PHASE I

NOTE X PRINT TO ENG. SPEC. NO.	DATE	CHANGE NO.	DATE	CHANGE NO.	DATE	CHANGE NO.	DRAW	UBL	6-9-53
							CHECK		
							APPRO.		
							REDRAW		
							CHECK		

INTERNATIONAL BUSINESS MACHINES CORP.

MACH. | MODEL

NAME: LEFT ARITHMETIC ELEMENT
ONE DIGIT COLUMN

DEFIANCE NO. 167H 10500

CHANGE No.	SYM.	REVISIONS	DATE	APPRO.

De

PA + B.R.D.

RESET CURRENT DRIVER

2 μs P.S.

BRIGHT

DIM

FF

FF

RESET

INDIVIDUAL CONSOLE

GT

GT

TO OTHER 73 POS

TO OTHER 73 POS.

56 CAT. SELECT C.F. CURRENT DR.

1007 μs

56

50 μsec

4

4-2 WAY "AND" CKTS & DIODES

4 RD CURR DR.

CX

CY

41

&

CFX

AUX. CURR. DRIVER

&

CFY

AUX. CURR. DRIVER

POWER CURRENT DRIVER

+10

-15

12K

FX

FY

25 μs

7

7

7 - 2 WAY "AND" CKTS. 14 DIODES

7 FS CURRENT DRIVERS

TO OTHER 73 P.OS.

2 μs P.S.

UNBLANK PULSE AT 17.5 TIME

NOTE: Control windings on non-selectable feature cores will be permantly wired in series to +10 v.

Approx. 460 cathodes incl. GT + CF

318 diodes

550 EK

1600
868
288
2752 cores

ALL CORES ARE METALLIC TAPE WOUND TYPE

ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART

UNLESS OTHERWISE NOTED		
BREAK CORNERS	MIN.	MAX.
OUTSIDE		
INSIDE		

			TOT.	MAT'L SPEC.	NO.
				CASE DEPTH	
				HARDNESS	
				SURFACE TREATMENT	
NEXT ASSY.	MODEL TYPE	NEXT ASSY.			
USED ON		QTY. REQ'D		GROSS WT. LBS.	MAT'L. SPEC. APPRO.

ALIGNMENT WITHIN	NOTE I
CONCENTRIC WITHIN	TOT. IND. READING NOTE II
FLAT WITHIN	NOTE III
PARALLEL WITHIN	NOTE IV
STRAIGHT WITHIN	NOTE V
SQUARE WITHIN IN INCHES	NOTE VI

TOLERANCE UNLESS OTHERWISE NOTED		
DECIMALS		
FRACTIONS		
ANGLES		
DRAW.	R&L	1/20/54
CHECK.		
APPRO.		

INTERNATIONAL BUSINESS MACHINES CORP.
POUGHKEEPSIE, N. Y.

NAME CONSOLE SELECTION UNIT

SCALE

DRAWING No.

DRAWING No.

REV.

DEFIANCE NO. 167H 3316

STANDARDS CODE	RELEASED FOR ASSEM.	QTY.

PHASE II

LM B TO OPR REG — GT — TO OP REG$_{i+1}$

LMB TO IO ADR CTR — GT — TO IO ADR CTR$_{i-1}$

LMB TO LIO REG — GT — TO LIOR$_{i-1}$

LMB TO RA REG — GT — TO RAR$_{i-1}$

LMB TO LA REG — GT — TO LAR$_{i-1}$

LMB$_{i-1}$

CLEAR LAR

COMP LAR

FF

CF CF

EXTRACT

GT GT — LAR TO LMB

TO LMB$_{i}$

TO MEM.

PARITY CHECK TO LMB$_{i-1}$ — ODD / EVEN

GT GT GT GT

OR OR

CF CF

EVEN ODD — PARITY CHECK FROM LMB$_{i+1}$

FF

CLEAR LMB

COMP LMB

LIO REG.

LACC$_{i}$

MEM

LA REG$_{i}$

OR

LM BUF$_{i}$

L A REG$_{i}$

L ADDER

SUM TO L ACC$_{i+1}$ — 0 / 1

CARRY TO L ADD$_{i-1}$ — 0 / 1

OR OR

GT GT GT

GT GT GT

CARRY FROM L ADD$_{i+1}$ — 1 / 0

CF OR CF

CF CF

& & & &

TO LMB$_{i}$ "1"

GT — LACC TO LMB

TO LBR$_{i}$ "1"

GT — LACC TO LBR

RIPPLE LACC RIGHT TO L ACC$_{i-1}$

OR

TO LACC$_{i+1}$ 0 — TO LACC$_{i+1}$ 1

GT GT — RIPPLE LACC RIGHT

TO LACC$_{i-1}$ 1 / 0

GT GT — LACC (2-15) TO (1-14)

CF CF

FF

LAR$_{i}$ 0

OR OR

SHIFT R 0 FROM LACC$_{i-1}$

SHIFT L 0 FROM LACC$_{i+1}$

SUM 0 FROM LACC$_{i-1}$

CLEAR LACC

COMP LACC

SUM 1 FROM LACC$_{i-1}$

SHIFT R 1 FROM LACC$_{i-1}$

SHIFT L 1 FROM LACC$_{i+1}$

L ACC$_{i}$

TO LBR$_{i+1}$ 1 / 0

GT GT — SHIFT LBR R

TO LBR$_{i-1}$ 1 / 0

GT GT — SHIFT LBR L

CF CF

FF

OR OR — LACC$_{i}$ 1

SHIFT R 0 FROM LBR$_{i-1}$

SHIFT L 0 FROM LBR$_{i+1}$

CLEAR LBR

COMP LBR

SHIFT L 1 FROM LBR$_{i+1}$

SHIFT R 1 FROM LBR$_{i-1}$

L B REG$_{i}$

PHASE II

NOTE X PRINT TO ENG. SPEC. NO.	DATE	CHANGE NO.	DATE	CHANGE NO.	DATE	CHANGE NO.	DRAW		
							CHECK		
							APPRO.		
							REDRAW		
							CHECK		

INTERNATIONAL BUSINESS MACHINES CORP.

MACH. MODEL

NAME LEFT ARITHMETIC ELEMENT ONE DIGIT COLUMN

DEPARTMENT NO. 1674 10100

STANDARDS CODE	RELEASED FOR ASSEM.	QTY.

PHASE III

UNIT TYPE LOCATION

LM B TO OPR REG
LMB TO IO ADR CTR
LMB TO LIO REG
LMB TO RA REG
LMB TO LA REG

TO OP REG
TO IO ADR CTR
TO LIOR
TO RAR
TO LAR

TO MEM.

PARITY CHECK TO LMB -1

UNIT TYPE LOCATION

EXTRACT DC

CLEAR LMB
COMP LMB
TO REG.
LACC
MEM
LA REG.

UNIT TYPE LOCATION

CLEAR LAR
COMP LAR

LMB

LAR TO LMB

TO LMB

UNIT TYPE LOCATION

SUM TO L ACC -1

CARRY TO L ADD -1

CARRY FROM L ADD +1

UNIT TYPE LOCATION

TO LMB -1

LACC TO LMB

TO LBR -1

LACC TO LBR

RIPPLE LACC RIGHT TO L ACC -1

TO LACC +1

RIPPLE LACC RIGHT

TO LACC -1

LACC (2-15) TO (1-14)

UNIT TYPE LOCATION

LAR

SHIFT R 0 FROM LACC -1
SHIFT L 0 FROM LACC +1
SUM 0 FROM LACC -1
CLEAR LACC
COMP LACC
SUM 1 FROM LACC -1
SHIFT R 1 FROM LACC +1
SHIFT L 1 FROM LACC +1

UNIT TYPE AND LOCATION

TO LBR +1

SHIFT LBR R

TO LBR -1

SHIFT LBR L

UNIT TYPE LOCATION

SHIFT R 0 FROM LBR -1
SHIFT L 0 FROM LBR +1
CLEAR LBR
COMP LBR
SHIFT L 1 FROM LBR +1
SHIFT R 1 FROM LBR -1

LACC 1

LM BUF i LA REG i L ADDER LACC i LB REG i

PHASE III

NOTE X
PRINT TO
ENG. SPEC. NO.

DATE	CHANGE NO.	DATE	CHANGE NO.	DATE	CHANGE NO.

DRAW			
CHECK			
APPRO.			
REDRAW			
CHECK			

INTERNATIONAL BUSINESS MACHINES CORP.

MACH. | MODEL

NAME LEFT ARITHMETIC ELEMENT ONE DIGIT COLUMN

FOR CHECKING
PURPOSES ONLY
AUG 20 1956

S MEM. $256^2 \times 37$

16 S MAR

T MEM. $64^2 \times 37$

16 T MAR

37 M MBR

PAR

37 N MBR

PAR

PAR

18 R INDEX ADDER

18 (y)

4 (F)

19 X MBR

18 P PROGRAM COUNTER

36 A ACCUM.

36 B B REG.

36 C CARRY

36 D DATA

36 E EXCHANGE BUFFER

36 F FRACTURE

6 J MAR

X MEM 64 x 19

6 U

BFR

6 K STEP CNTR

INSTRUCTION REGISTER

CONTROL

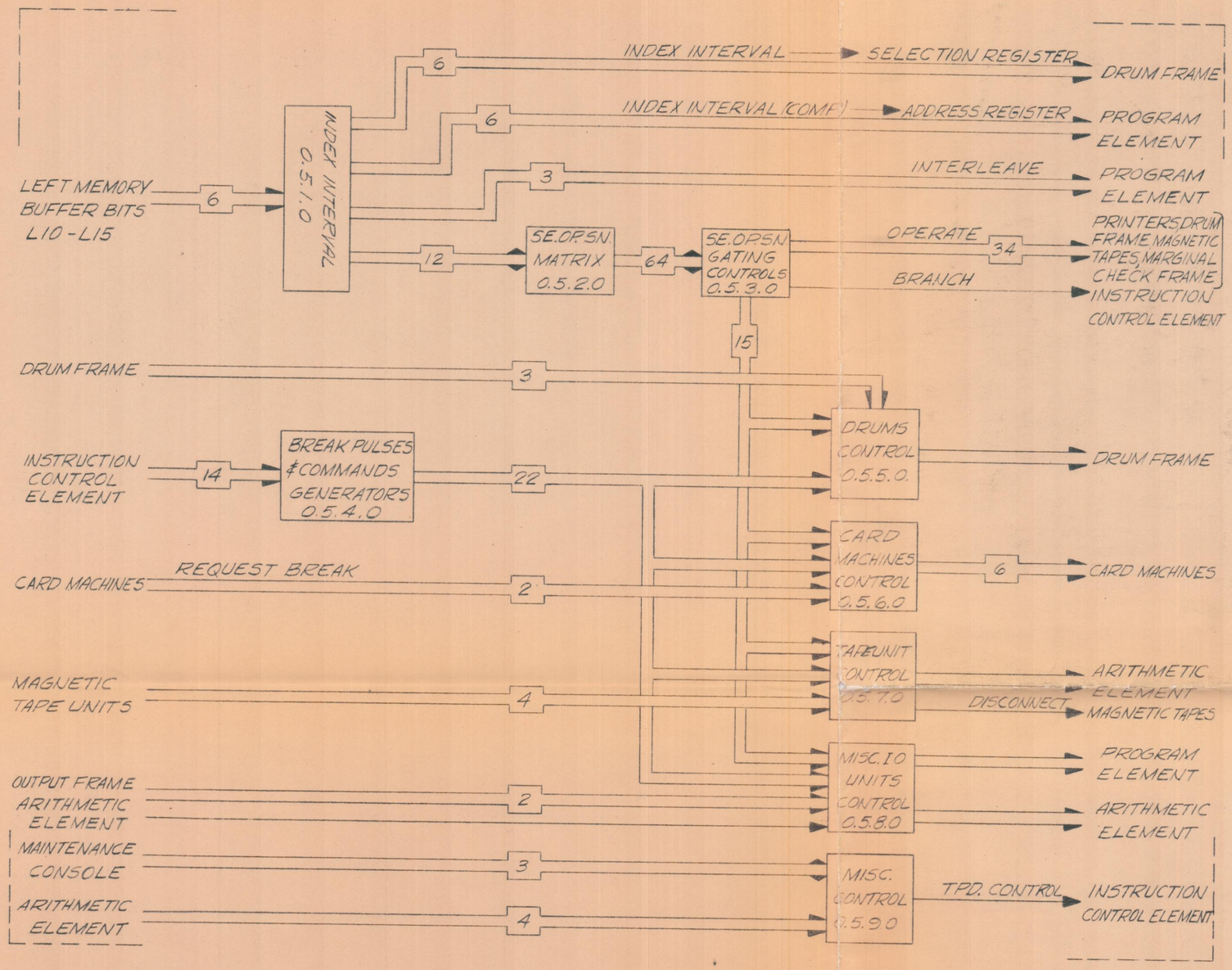
I.O.E IN-OUT EQUIP.

GOOD Boy

LITMUS —
LINCOLN TRANSISTORIZED
MULTIPLE SEQUENCE
COMPUTER.

AUG. 20, 1956

CHANGE No.	SYM.	REVISIONS	DATE	APPRO.



DRAWING No. 0.5.0.0

REV.

ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART

UNLESS OTHERWISE NOTED		
BREAK CORNERS	MIN.	MAX.
OUTSIDE		
INSIDE		

			TOT.	MAT'L SPEC.	NO.
				CASE DEPTH	
				HARDNESS	
				SURFACE TREATMENT	
NEXT ASSY.	MODEL TYPE	NEXT ASSY. QTY. REQ'D			
USED ON				GROSS WT. LBS.	MAT'L. SPEC. APPRO.

ALIGNMENT WITHIN	NOTE I
CONCENTRIC WITHIN TOT. IND. READING	NOTE II
FLAT WITHIN	NOTE III
PARALLEL WITHIN	NOTE IV
STRAIGHT WITHIN	NOTE V
SQUARE WITHIN IN INCHES	NOTE VI

TOLERANCE UNLESS OTHERWISE NOTED		
DECIMALS		
FRACTIONS		
ANGLES		
DRAW.	J.P.H.	3-9-54
CHECK.		
APPRO.		

INTERNATIONAL BUSINESS MACHINES CORP.
POUGHKEEPSIE, N. Y.

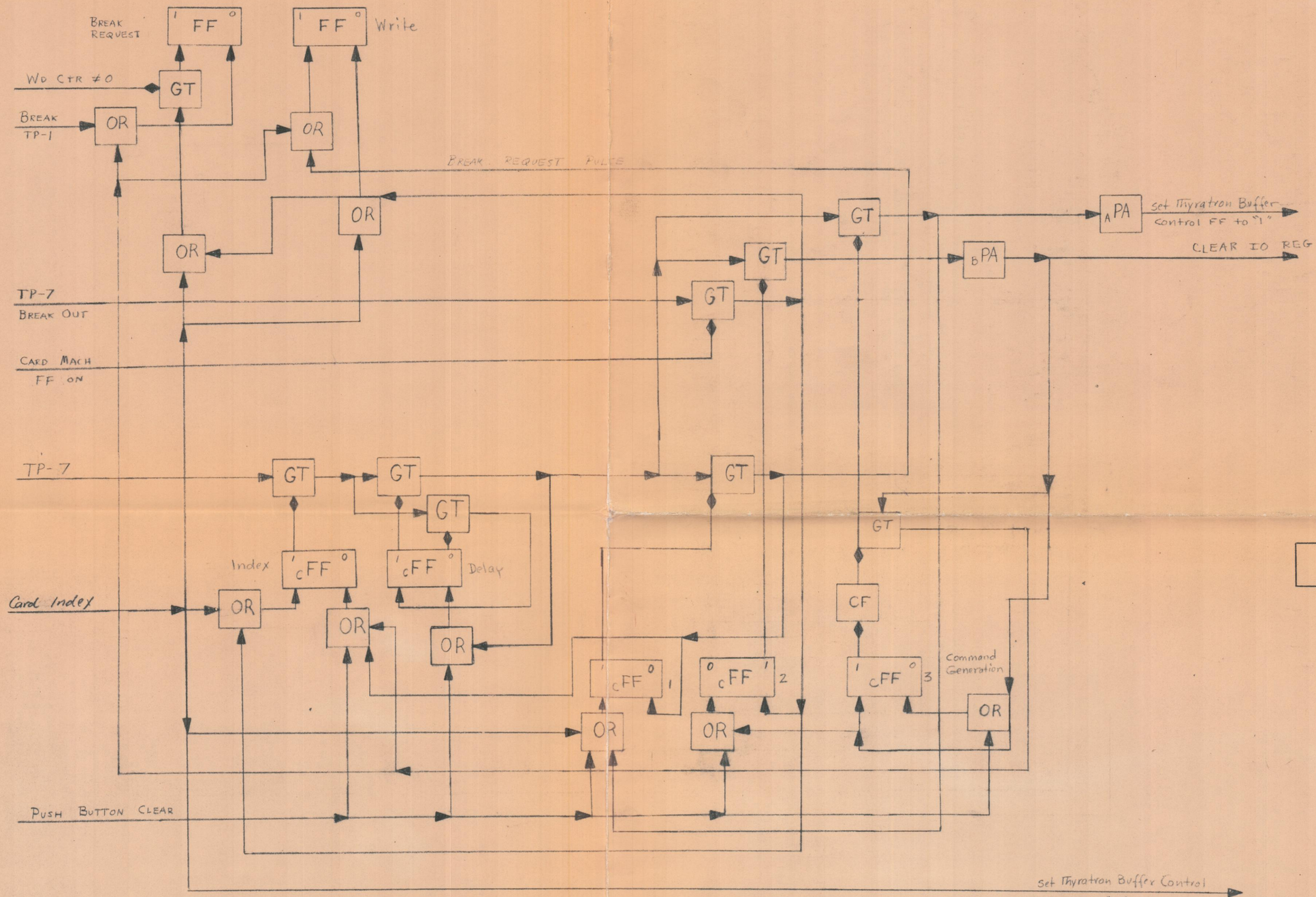
NAME SECTION 10 CONTROL ELEMENT DIAGRAM

SCALE NONE

0.5.0.0
DRAWING No.

DEFIANCE NO. 167H 3316

CHANGE No.	SYM.	REVISIONS	DATE	APPRO.



DRAWING No.

REV.

ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART

UNLESS OTHERWISE NOTED		
BREAK CORNERS	MIN.	MAX.
OUTSIDE		
INSIDE		

		TOT.	MAT'L SPEC.	NO.	ALIGNMENT WITHIN	NOTE I	TOLERANCE UNLESS OTHERWISE NOTED
					CONCENTRIC WITHIN	TOT. IND. READING NOTE II	DECIMALS
			CASE DEPTH		FLAT WITHIN	NOTE III	FRACTIONS
			HARDNESS		PARALLEL WITHIN	NOTE IV	ANGLES
			SURFACE TREATMENT		STRAIGHT WITHIN	NOTE V	DRAW. EGW 2/25/54
NEXT ASSY.	MODEL TYPE	NEXT ASSY.			SQUARE WITHIN IN INCHES	NOTE VI	CHECK.
USED ON		QTY. REQ'D	GROSS WT. LBS.	MAT'L. SPEC. APPRO.			APPRO.

INTERNATIONAL BUSINESS MACHINES CORP.
POUGHKEEPSIE, N. Y.

NAME: Card Machines
Write Operation

SCALE

DRAWING No.