THE LOGICAL DESIGN OF

A DIGITAL AVERAGE RESPONSE COMPUTER

by

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ABSTRACT

The Digital Average Response Computer is a special purpose transistorized computer for performing on line analysis of neuro-electric phenomena. The input is an amplified neuro-electric signal in analog form and the principle mode of operation is response averaging. Auxiliary modes, for compilation of amplitude, time, and interspike histograms, are built into the computer to illustrate its flexibility.

The logical design is based on commercially available packaged circuit modules manufactured by Digital Equipment Corporation. The timing characteristics and loading requirements have been taken into account so that the design shown here can be implemented directly as shown.

The design philosophy is based on obtaining the maximum flexibility while making use of the inherent speed of an internally programmed computer.

CHAPTER I

INTRODUCTION

The Digital Average Response Computer (DARC) is a small, special purpose computer for on line recording and analyzing of neuro-electric phenomena. Designed principally for the determination of the evoked response to a sensory stimulus, the DARC is also useful for other types of bio-medical experiments requiring average response computation or other similar types of data processing methods. Alternate modes, for compilation of amplitude, time, and interspike histograms, have been built into the DARC to illustrate its flexibility.

The DARC is completely transistorized with a magnetic core memory. The logical design is based on a commercial line of package circuit modules manufactured by Digital Equipment Corporation (DEC) of Maynard, Massachusetts. The computer accepts the amplified neuro-electric signal in analog form. The output is available from a cathode ray display tube (CRT). A special counter with indicator lights continuously displays the number of responses which have been processed.

When operating in its principle mode, average response computation, the DARC records and sums brain potentials as a function of time, in order to determine the evoked

response to a sensory stimulus. The brain potentials recorded immediately after the application of a stimulus are assumed to be the sum of an evoked response and a random noise signal. By taking an average, which is time locked to the stimulus, the signal to noise ratio may be increased by a factor $\sqrt{N}$, where N equals the number of responses which have been averaged.

To perform this averaging, the DARC samples the input signal at periodic time intervals with reference to a separate stimulus input signal. Each sample is converted to a digital number and is added to the sum of all samples taken at corresponding times during previous responses. A total of 256 samples may be taken during each response. The time between samples may be varied from 28 microseconds to 0.917546 seconds. The time between the occurrence of the stimulus and the first sample may be varied up to 0.917504 seconds.

The sum of the responses is continuously displayed on the output CRT screen. This allows the experimenter to check for any irregularities while the data is being taken.

A constant display mode is available for photographing the processed data. This mode is automatically entered when the desired number of responses have been processed,

or it may interrupt the regular data processing mode upon command by the experimenter. This break is initiated only at the beginning of a data processing cycle, and returns in a similar manner, assuring that all responses will contain the same number of samples and all samples will be in phase.

The flexibility of the DARC is illustrated by including three typical alternate processing modes. These modes require a certain amount of additional gating circuitry, but essentially no changes in the other parts of the computer.

The amplitude histography mode measures the variation in signal amplitude at a given time after the occurrence of the stimulus. The input signal is sampled once after each new stimulus and the number of samples taken are recorded as a function of the amplitude of the input signal at sample time.

The time at which the sample is taken may be varied from approximately 14 microseconds to 0.9175 seconds after the occurrence of the stimulus.

The time and interspike histography modes are used to measure a single unit activity. The presence of this unit (spike) is defined as that time when the input signal exceeds a certain threshold voltage level. The threshold

voltage level is inserted into the computer manually and may have any value from 0 to full scale.

In the time histography mode, the method of computation is almost identical to the response averaging mode. However, instead of summing the amplitude of the input signal during corresponding time intervals, the computer will sum the number of spikes which occur during corresponding time intervals. The output then, shows the number of spikes as a function of time.

The interspike histography mode is a simple extension of the time histography mode, in which the occurrence of a spike resets the time scale of the computer in the same manner as the stimulus does in previous examples. Thus, the result of this mode is a display of the number of spikes as a function of the time between spikes.

The histography modes do not include provisions for continuous display. In the amplitude histography mode such a display would be essentially meaningless; in the time and interspike histography modes, the continuous display is left out in order to allow faster data processing time. When the experimenter desires to observe the processed data, the computer may be switched temporarily to the display mode. The computer may then be returned to the data processing mode without interfering with the regular timing. The computer will also go automatically into the display mode at the completion of the data processing.

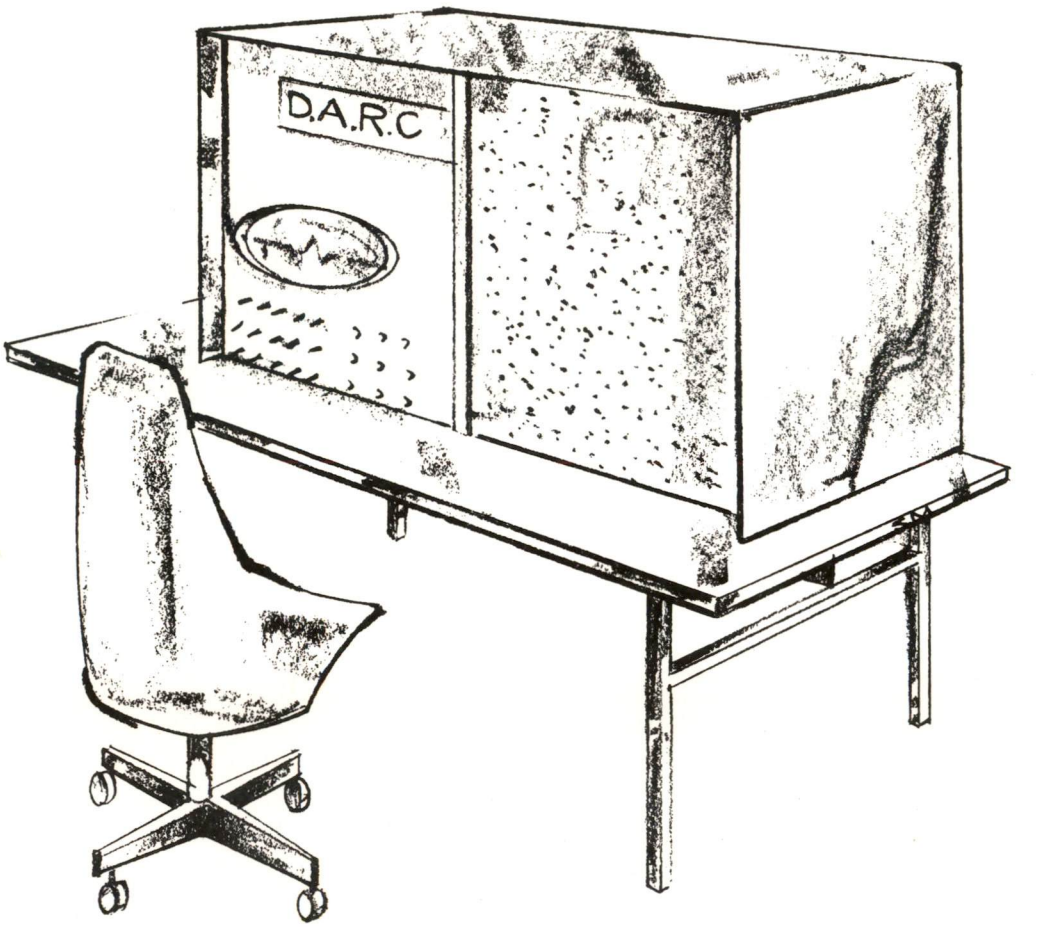
CHAPTER II

GENERAL DESCRIPTION

Figure 2.1 shows the author's conception of how the DARC might appear after being built. The circuit modules, control panel, CRT, and power supplies are mounted together in a small, two bay, mounting rack. The power supplies are located at the bottom of the two bays and a working table is extended from the mounting rack just above these power supplies. The system is raised from the floor sufficiently far to allow the operator to sit at the work table within easy reach of the controls and easy view of the CRT.

The plug-in units are mounted in standard 19" mounting panels with the wiring at the front of the computer and the modules accessible from the back. The cover panels on the front of the system may be removed for easy access to the circuit wiring. The back of the computer has doors for easy access to the modules. The part of the system above the working area is 28" high, 40" wide and 24" deep.

Other physical arrangements are, of course, possible. The total space required in any arrangement is 66" of vertical space in standard 19" mounting racks, with a depth of 24".

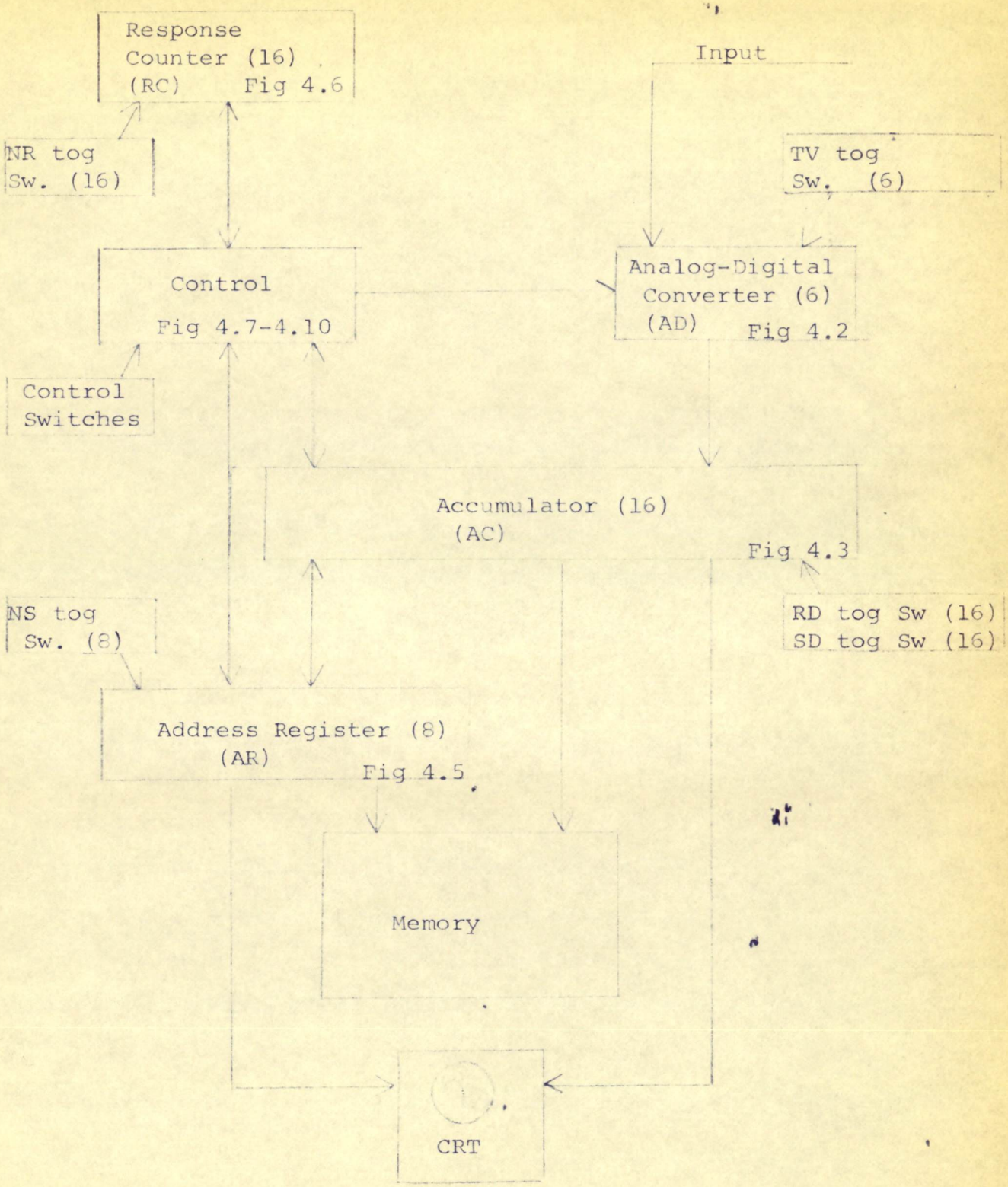


ARTISTS CONCEPTION OF DARC

FIG. 2.1

Figure 2.2 shows a block diagram of the DARC. The functional portions of the computer, as shown on the diagram, are: the analog-to-digital converter, the accumulator, the memory and associated driving and sensory circuitry, the address register, the response counter, and the control circuitry. A brief discussion of the purpose and capabilities of these functional portions is given in Sections 2.1 through 2.6.

The control panel is shown in Figure 2.3. Five toggle switch registers are available for varying the parameters: the number of responses to be processed, the number of samples per response, the delay between samples, the response delay between the stimulus and the first sample, and the threshold voltage which the input signal must surpass in order to be defined as a spike. Switches are available for power on-off, start, mode control, start display, stop display and scale display. The contents of the response counter, accumulator, and address register are displayed on the control panel. Lights also indicate when the computer is operating in the setup or the display modes. Input plugs are available for the neuro-electric signal and the stimulus. Sections 2.7 through 2.10 discuss the purpose of each mode and the variable parameters which are applicable. These sections also include a brief



DARC

Block Diagram

Figure 2.2

DARC CONTROL PANEL

Figure 2.3

description of the operation of the mode.

Section 2.1 Functional Portions of the Computer

Section 2.11 Analog-to-Digital Converter (AD)

The analog-to-digital converter serves two functions. In the response averaging and amplitude histography modes, the converter accepts the analog input signal and converts it to a digital number. In the time and interspike histography modes, the converter serves as a spike detector by determining when the input analog voltage exceeds a threshold level.

The converter consists of a 6 flip-flop buffer, a ladder network, a difference amplifier, and associated gating. It will accept inputs in the range of 0 to -10 volts. Its digital output is fed to the accumulator.

The total conversion time is 20 microseconds. This makes the analog-to-digital converter the slowest part of the computer during the averaging and amplitude histography modes. However, the time required for sampling and processing one piece of information is almost half of the shortest time considered desirable at present. If, in the future it should appear desirable to have a faster processing time, or to add another input channel, this part of the machine could be readily changed.

In the time and interspike histography modes the analog-to-digital converter is used to determine when the input voltage is greater than a threshold level. This threshold voltage is set into the converter register via a toggle switch register (TV). When the input voltage exceeds the number in this flip-flop register, a signal is generated by the difference amplifier.

Section 2.12 Accumulator (AC)

The accumulator is the arithmetic element of the computer, and it communicates with all flip-flop registers except the response counter. For this reason the major portion of the work is done in the accumulator.

The accumulator consists of a six bit adder with a ten bit carry which operates in the ONEs complement number system. It can be read into from the memory and the AD register. It can read out into the memory, the address register and the cathode ray tube (CRT). The contents of the buffer can be compared with the number in either of two toggle switch registers (RD and SD).

During the memory cycle, the accumulator is used to add the appropriate number to memory and to provide the Y coordinate to the CRT. When it is desired to have a delay in the program, the accumulator will count out this delay

increasing by one count every 14 microseconds. When the accumulator has reached the desired number, as contained in the appropriate toggle switch register, then the main program will be resumed. In addition, the accumulator is used to transfer information from the AD to the address register.

Section 2.13 Memory

A coincident current magnetic core memory is to be used in the DARC. The DARC plans are based on the memory of 256 words of 16 bits each. However, since the size of the memory required will depend primarily on the particular type of experiments which the machine is to be used with, the computer is designed so that the size of the memory is not a prime factor.

A memory cycle time of 5 microseconds has been assumed, but this can also be varied.

Section 2.14 Address Register (AR)

The address register is an eight bit counter. Although the main purpose of the address register is to address the appropriate word in memory, it is also used to perform some logic.

During all modes of operation, except the amplitude histography mode, the address register serves to keep

track of the number of intervals which have been sampled, processed and recorded. The contents of the address register can be compared with the NS toggle switch register to determine when the desired number of intervals have been processed. At this time the regular program is stopped until another stimulus is received.

During the amplitude histography mode the address register receives information from the AD by way of the accumulator.

The address register provides the X coordinate for the CRT display.

Section 2.15 Response Counter (RC)

The response counter is a 16 bit counter which records the number of responses which have been processed. The output of the response counter is indicated by lights on the front panel. The output is also compared with the NR toggle switch register to determine when the desired number of responses have been processed.

Section 2.16 Control

The control circuitry, as the name implies, governs the sequence of operations of the computer. Each mode has its own built-in sequence which is modified in accordance with the setting of the parameter and control

switches. A more detailed description of the control circuitry is given in Chapters III and IV.

Section 2.2 Modes of Operation

Section 2.21 Response Averaging

When a sensory stimulus is presented to a subject, the brain potentials recorded immediately after the stimulus are assumed to be the sum of an evoked response and a random noise signal. Mathematics predict that the averaging process, if time locked to the stimulus, will increase the signal to noise ratio by a factor $\sqrt{N}$, where N equals the number of responses which have averaged.

The averaging mode begins with the memory and all flip-flop registers cleared. After the occurrence of the first simulus, the response will be sampled at periodic time intervals. The magnitude of the response at each time interval will be recorded in the memory word corresponding to that time. When the desired number of samples have been taken the computer will wait for the next stimulus signal.

After each succeeding stimulus, the response will be sampled at the same time intervals as before and the magnitude of the response at each time will be added to the memory register corresponding to that time. A continuous plot of the growing sum will be displayed on the CRT.

The X coordinate, time, will be controlled by the address register and the Y coordinate, sum of the amplitudes, will be controlled by the accumulator.

The number of responses to be processed is controlled by the NR toggle switch register. The maximum number which may be set to this register is $2^{16}-1$ or 65,536. The number of processed responses is indicated by the row of lights next to the NR toggle switches. When this number exceeds 2^{10} or 1024, the experimenter should monitor the data via the CRT to make sure that the memory registers do not overflow.

The number of samples to be taken within a response are controlled by the contents of the NS toggle switch register. This may be set for a maximum value of $2^{8}-1$ or 255.

The RD toggle switch register determines the delay between the occurrence of the stimulus and the first sample. This delay is adjusted in steps of 14 microseconds; that is, if RD equals 1, the delay will be 14 microseconds; if RD equals 2, the delay will be 28 microseconds, etc. Since the stimulus may appear asynchronously, there may be an additional delay of up to 14 microseconds, even if RD is zero.

The sample processing time requires 28 microseconds.

Additional delay may be inserted between sample points by means of the SD toggle switches. As additional delay will be equal to 14 microseconds times the number inserted in the SD toggle switch register plus an additional 14 microseconds or 14SD+14.

Care should be taken that the stimulus is never allowed to come before the processing of the previous response has been completed. This response processing time, governed by the inserted parameters, may be calculated as follows:

Total time = 14RD+14+(14SD+28)NS.

The TV toggle switches are not applicable in this mode and should be set to 0 to allow proper operation of the analog-to-digital converter.

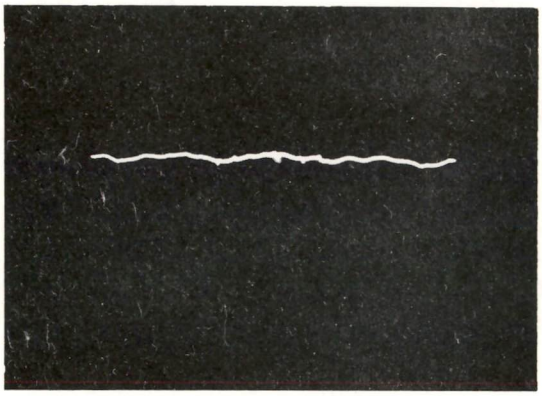
A constant display is available whenever desired. This is controlled by the start display and stop display switches. The actual starting of this display will always occur at the end of a response processing cycle, therefore it may require some time before the computer goes into the display mode. However, when the display mode is operating, the display indicator will be lit. The scale factor switch allows the display size to be increased or decreased.

Figure 2.4

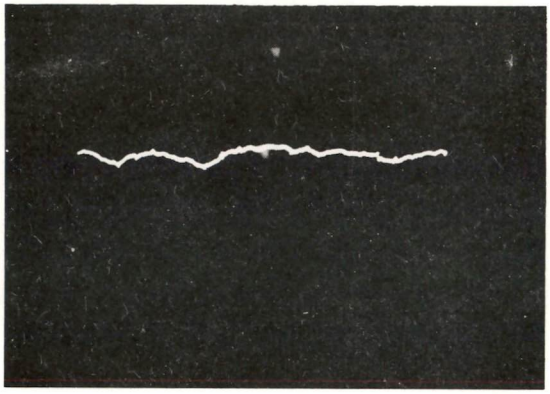
Average Responses to Acoustical Clicks

Experiment performed by Dr. C. D. Geisler on August 2, 1960

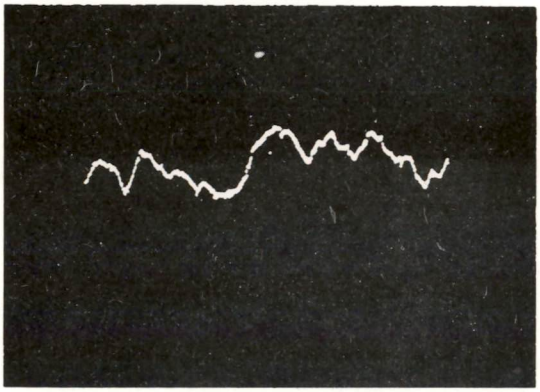
Averaging performed by the DEC Programmed Data Processor - 1



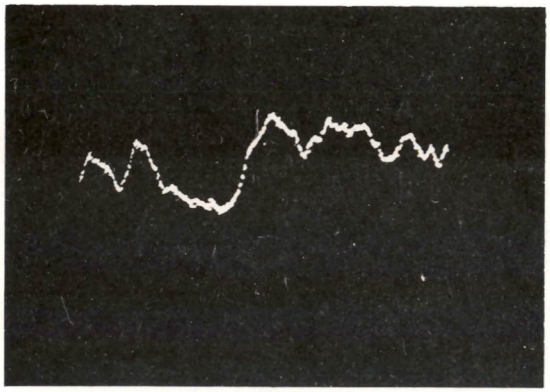
4 Responses



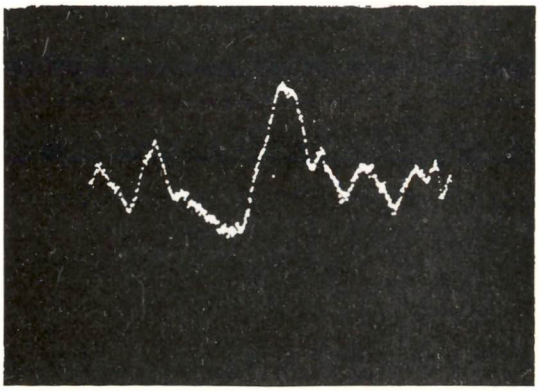
16 Responses



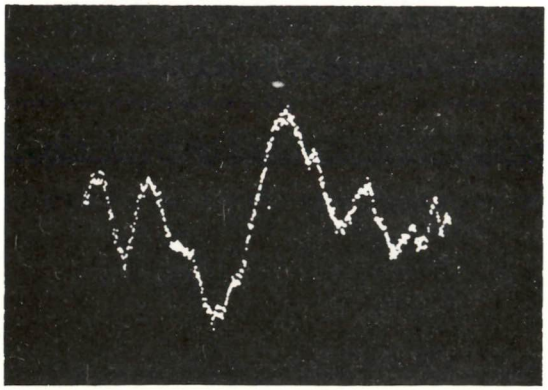
64 Responses



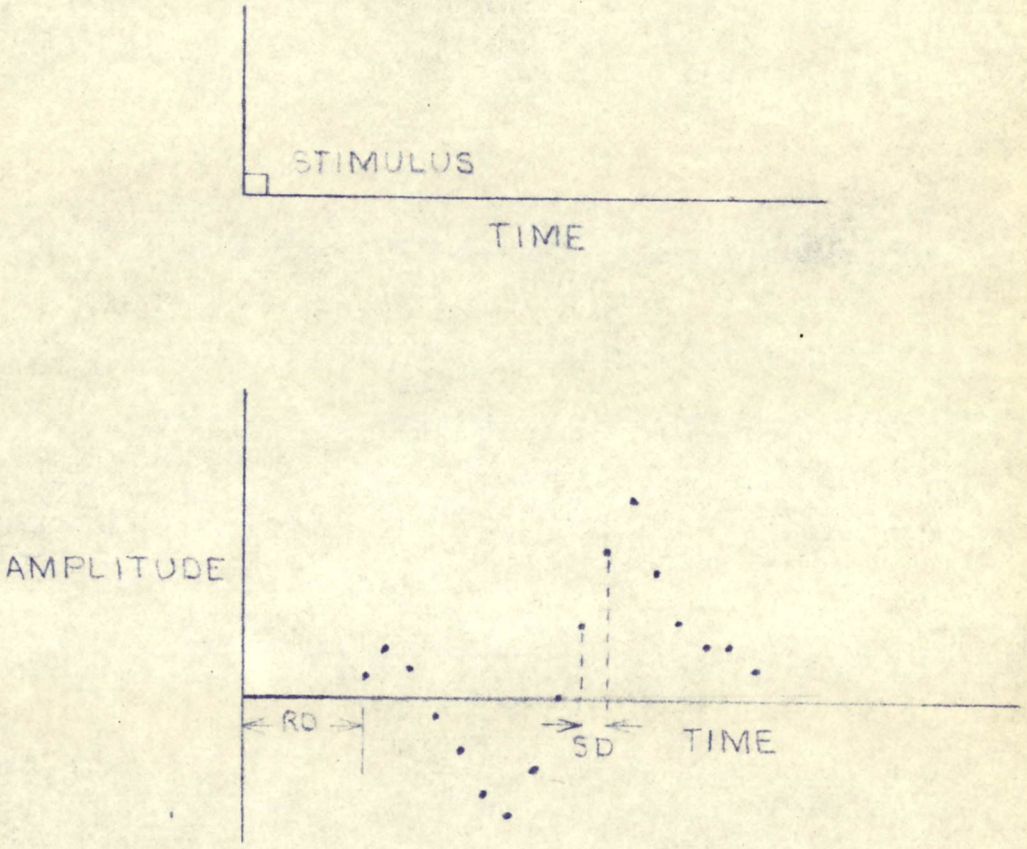
128 Responses



256 Responses



512 Responses



DRAWING OF AVERAGE RESPONSE

FIGURE 2.5

Section 2.22 Amplitude Histography

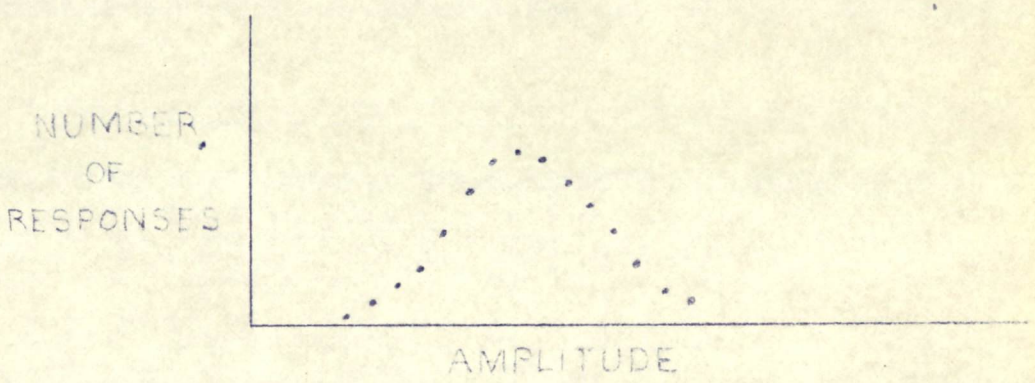
The amplitude histography mode is used to measure the variation in amplitude at a given time after the occurrence of a stimulus. Only one sample is taken per response.

The mode begins with the memory and all flip-flop registers cleared. After the arrival of the stimulus an initial delay, RD, is counted out in the accumulator. At the sample time, the amplitude of the response is converted to a digital number by the AD and transferred to the address register. This address will then be called out of memory and a ONE will be added to it. This indicates that one sample with a particular amplitude has occurred.

A maximum of 64 memory registers will be used since this is the maximum number of amplitude divisions available from the AD.

When the desired number of responses have been processed the computer will automatically go to the display mode. The CRT will be driven by the accumulator and address register and the output will show the number of samples as a function of amplitude.

The sample time is controlled by the toggle switch register RD. The number of responses to be sampled is controlled by the NR toggle switch register. The values of the parameters are the same as in the averaging mode,



DRAWING OF AMPLITUDE HISTOGRAM

FIGURE 2.6

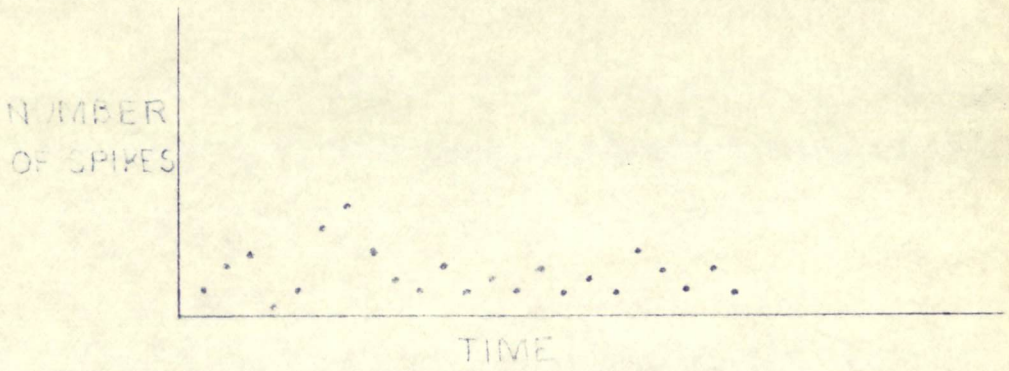
except that the SD and NS switches are not used. The operation of the indicator lights on the control panel, the method of switching to the display mode, and the requirement for setting the TV switches to zero are also the same as for averaging.

Section 2.23 Time Histography

The time histography mode measures the number of occurrences of a unitary weighted event (spike) as a function of time. The mode begins with the memory and all flip-flop registers, except the AD, cleared. The AD register is set to the number in the TV toggle switch register. This number indicates the threshold voltage used to determine when a spike has occurred. The number is in the ONEs complement notation with the most positive number (011111) corresponding to 0 volts and the most negative number (100000) corresponding to -10 volts.

The operation of this mode is similar to the averaging mode. After the occurrence of a stimulus, the response is divided into periodic time intervals. If the difference amplifier of the AD indicates that a spike has occurred during a particular time interval, then a ONE is added to the corresponding word in memory.

The response delay, sample delay, number of samples,



DRAWING OF TIME HISTOGRAM

FIGURE 2.7

and number of responses is controlled by the toggle switch registers in the same manner as in the averaging mode. However, the basic sample processing time, without artificial delay, is only 14 microseconds, therefore:

Total time = 14RD+14+(14SD+14)NS

When the desired number of responses have been processed, the display switch is set, the computer enters the display mode. The CRT shows the number of spikes as a function of time.

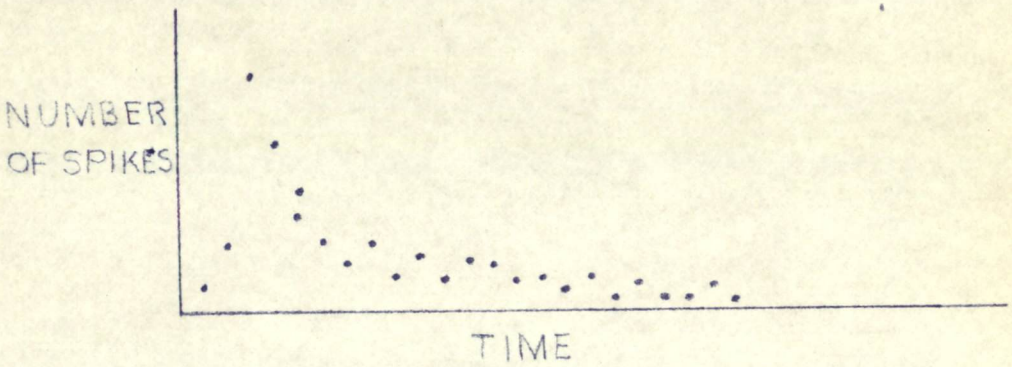
Indicator lights from the response counter show the number of processed responses.

Section 2.24 Interspike Histography

The interspike histography mode is a simple extension of the time histography mode with each spike also serving as a stimulus signal. Thus, this mode measures the variation in time between successive spikes.

The operation of the computer, use of the parameters and control switches, and the timing are basically the same in this mode as in the time histography mode. The number of responses, of course, refers to the number of interspike intervals, and the response delay indicates the duration of the first time interval.

The CRT output represents the number of spikes as a function of the time between spikes.



DRAWING OF INTERSPIKE HISTOGRAM

FIGURE 2.8

CHAPTER III

TECHNICAL DESCRIPTION OF DARC TIMING

The DARC has four operating cycles. Each cycle has a duration of 14 microseconds and contains 9 time pulses. The cycle control is a two bit counter which is decoded into four states (CY0-CY3). The time pulses are produced by a delay loop. The time pulse, cycle, and mode determine the operation taking place in the computer. For example: in the averaging mode, during cycle one, on time pulse 7 (AV1 TP7) the display is started.

Very often groups of operations in different modes and cycles will overlap. For example: in all modes, during cycle zero, a memory word is read into the accumulator and a new word is written in the memory. To gate these operations separately is obviously an excessive use of gates. Hence, various modes and cycles are gated together to form common cycles. A common cycle may be made up of any combination of individual modes and cycles, such as AV1 and AH2.

There are six common cycles. Three of these control the operation of the analog-to-digital converter only and are designated CC0, CC1, and CC2. The other three common cycles control the operations in other parts of the computer. These are designated BC0, BC1, and BC2.

Each operation, then, is controlled by the time pulse gated with a common cycle or with a mode and cycle.

Figure 3.1 shows a complete timing diagram.

Section 3.1 The Common Cycles

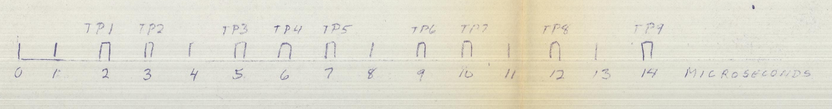
BC0 is the combination of all modes during cycle zero and controls the reading and writing of the memory.

BC1 is a sequence determination cycle which is used in the averaging and time histography modes at the completion of the processing of each data sample. It determines whether to take another sample, introduce an artificial delay, wait for a new stimulus, or transfer to the display mode.

BC2 is used in all modes, but during different cycles. The purpose of the common cycle is to introduce an artificial delay or provide a waiting period. Once in this cycle, the computer will remain until the end of the delay of waiting period. This is done simply by not indexing the cycle counter.

The computer waits for the stimulus signal in BC2. On time pulse 1, it investigates to determine if the stimulus has appeared. If so, the response counter is indexed and the address register is cleared. The SE flip-flop is cleared, in order to allow the artificial

CYCLE	TIME PULSE	BUFFER COMMON (BC)	CONVERTER COMMON (CC)	SET UP (SU) ENTER CY0 WITH SE=1, AD=TV RC=C=ST=D=0	RESPONSE AVERAGING (AV) ENTER CY2 WITH SE=1, C=10 AC=AR=AD=RC=ST=D=0	AMPLITUDE HISTOGRAPHY (AH) ENTER CY1 WITH SE=1, C=01 AC=AR=AD=RC=ST=D=0	TIME HISTOGRAPHY (TH) ENTER CY1 WITH SE=1, C=01, AD=TV AC=AR=RC=ST=D=0	INTERSPIKE HISTOGRAPHY (IH) ENTER CY1, WITH SE=1, C=01, AD=TV AC=AR=RC=ST=D=0	DISPLAY (D)	TIME PULSE	CYCLE
CYCLE 0	1	START READ		BC0	BC0, CC0, CC2	BC0	BC0 READ SP	BC0 READ SP	BC0	1	CYCLE 0
	2	M → AC								2	
	3	STOP READ				INDEX AC	SP ⇒ INDEX AC, CLEAR SP	SP ⇒ INDEX AC, CLEAR SP, SET ST		3	
	4									4	
	5			CLEAR AC	CARRY				START D	5	
	6		START CONVERT							6	
	7	START WRITE			START DISPLAY					7	
	8	STOP WRITE	CONVERT 1	INDEX AR AR* · $\overline{AV}$ ⇒ INDEX C AR* · AV ⇒ SET C=10				CLEAR AC		8	
	9				INDEX C	INDEX C, CLEAR AC, SET SE READ D, NR ⇒ SET D	CLEAR AC	ST ⇒ CLEAR AR, READ D, INDEX R*C, C; ST · NR ⇒ SET D ST · $\overline{AD}$ ⇒ INDEX AR; ST · $\overline{GA}$ ⇒ INDEX C	INDEX C	9	
CYCLE 1	1				BC1, CC0	BC2, CC0	BC2	BC2 READ SP,		1	CYCLE 1
	2		CONVERT 2							2	
	3							SP · SE ⇒ SET ST, CLEAR SP, SET IR INDEX RC		3	
	4		CONVERT 3							4	
	5									5	
	6		CONVERT 4							6	
	7									7	
	8	STOP DISPLAY, INDEX AR, CLEAR AC	CONVERT 5						STOP DISPLAY, INDEX AR, CLEAR AC, READ D	8	
	9	NR · NS ⇒ SET D; $\overline{NS}$ · GA ⇒ CLEAR C, NS ⇒ INDEX C, CLEAR AR; $\overline{GA}$ ⇒ INDEX C NR · NS ⇒ SET SE, READ D							$\overline{D}$ · SI ⇒ INDEX C; NS ⇒ CLEAR AR $\overline{D}$ · SI ⇒ INDEX C	9	
CYCLE 2	1	READ ST	CONVERT 6		BC2, CC0	CC1					
	2										
	3	ST · SE ⇒ CLEAR AR, SET INDEX RC	AD ⇒ AC								
	4										
	5	$\overline{SE}$ ⇒ INDEX AC									
	6										
	7										
	8										
	9	$\overline{SE}$ · $\overline{ST}$ · SD + ST · RD ⇒ CLEAR AC, SET INDEX C				INDEX C					
CYCLE 3	1					CC2					
	2										
	3										
	4										
	5					AC → AR					
	6										
	7										
	8										
	9				INDEX C	CLEAR AC, INDEX C					



TIMING DIAGRAM

FIGURE 3.1

delay to be counted out. The computer remains in this cycle, indexing the accumulator once each time until the contents of the accumulator equal the contents of the RD toggle switch register. The computer then advances to the next cycle.

When an artificial delay is introduced between samples, the computer enters the BC2 between samples, with the SE flip-flop previously cleared. The process of counting out the delay begins immediately and advances as with the response delay. When the contents of the accumulator equal the contents of the SD toggle switch register then the computer advances to the next cycle.

The converter common cycles are used only in the averaging and amplitude histography modes. The converter requires a start signal and 6 convert signals. The start signal and the first convert signal are produced by CC0. CC1 produces the second through the fifth convert signals. CC2 proudces the last convert signal and also transfers the contents of the converter register to the accumulator.

Section 3.2 Set-Up Mode

When the start button is pressed all control flip-flops (except SE), the address register and the response counter are cleared. The SE flip-flop, is set and a pulse is inserted into the delay loop.

The computer enters the set-up mode (SU), defined as cycle zero with set and D cleared (CY0 SE D). The computer advances through the memory, clearing all the cores. To do this, it utilizes BC0 and clears the accumulator between the memory read and the memory write.

When the entire memory is cleared, the cycle counter is set for entering the desired mode in the proper cycle.

Section 3.3 Response Averaging Mode

The average mode is entered in cycle two. Here it utilizes BC2, the waiting cycle. Since SE is set, the computer will continue going through this cycle, but will perform no operations until a stimulus signal is received. After occurrence of the stimulus, the accumulator is indexed once per cycle until the response delay is counted out.

At the same time, CC0 is beginning conversion. Since the start convert signal always clears the converter register, no harm is done by repeating the operation.

After the cycle counter is indexed, the computer advances to CY3, where the analog-to-digital conversion process is continued with CC1.

The computer advances to CY0 where the analog-to-digital conversion process is completed and the contents

of the AD register are added to the contents of address zero in the memory, the display is intensified, and a new analog-to-digital conversion is started.

The computer advances to CY1, where the display and conversion process are continued. On time pulse 8, the display is halted and the accumulator is cleared. The address register is indexed to give the number of samples which have now been processed and the location of the memory register to which the next sample will be added.

On time pulse 9, the computer determines the next sequence of operations. If comparison of the address register with the NS toggle switch register shows that all samples in the response are not yet processed, the computer will normally advance to CY2 in order to count down the artificial delay between samples. If there is to be no artificial delay before the next sample, the computer will immediately return to CY0. If the desired number of samples have been processed, but the desired number of responses have not yet been processed, then the computer will normally set the SE flip-flop and advance to CY2 to await the new stimulus. (Setting the SE flip-flop is what determines that the computer will wait for a new stimulus rather than begin counting an artificial delay as above.) However, if the response is completed and the start display

switch is set, the computer will transfer to the display mode. The computer also will switch to the display mode if both the desired number of samples and the desired number of responses have been processed.

Section 3.4 Amplitude Histography Mode

The amplitude histography mode is entered in cycle one. This cycle combines BC2, the waiting cycle and CC0, the first converter cycle. This is identical to the operation of the averaging mode in cycle two. The computer waits until a stimulus signal appears. It then counts down the response delay, simultaneously beginning conversion of the input signal to a digital number. When the desired delay time is passed, the computer advances to cycle two where the conversion process is continued.

The computer advances to cycle three to complete the conversion process. The digital number, representing the amplitude of the input analog signal, is transferred from the AD register to the accumulator and then from the accumulator to the address register. The accumulator is cleared and the computer advances to cycle zero.

In cycle zero, the memory word, with the address corresponding to the amplitude of the input signal, is read into the accumulator. The acccumulator is indexed to indicate

that one sample with this amplitude has been received. The contents of the accumulator are read back into the memory and the processing of one response has been completed.

If the desired number of responses have now been processed, or if the start display switch has been set, the computer will go to the display mode. Otherwise the computer will continue to cycle one to wait for a new stimulus.

Section 3.5 Time Histography Mode

The time histography mode is entered in cycle one. This utilizes BC2 and corresponds to the average mode cycle two or the amplitude histography mode cycle one, except that the analog-to-digital converter does not operate. The computer waits for the stimulus then counts down the response delay. When the contents of the accumulator are equal to the RD toggle switch register, then the cycle counter is indexed and the computer advances to cycle zero.

The contents of memory register zero is read into the accumulator and the accumulator is indexed if a spike has occurred during the response delay. The contents of the accumulator are then read back into the memory and the accumulator is cleared. The address register is indexed

to indicate that the first time interval has passed.

The decision is then made to sample again with no delay by returning to CY0, to continue to CY1 for an artificial delay between samples, to continue to CY1 to await a new stimulus or to go to the display mode.

Section 3.6 Interspike Histography Mode

The interspike histography mode is entered in cycle one with BC2, the waiting cycle, controlling the operation of the computer. Since there is no external stimulus in this mode, the first spike is used to set the ST flip-flop and begin the response delay count. When the response delay is completed, the computer will advance to cycle zero. If a spike has occurred during the response delay, then the SP flip-flop will be set. The contents of the memory register zero is read into the accumulator and, if SP is set, the accumulator will be indexed. The contents of the accumulator are read back into the memory and the accumulator is cleared.

The computer decides what path of operation is to be taken next. If a spike has not occurred, then the computer must remain in cycle zero to look for a new spike or continue to cycle one to count down the interval delay. The address register must be indexed to indicate

that one time interval has gone by. (If the address register has reached the point of overflowing, then it will not be indexed.)

If a spike has occurred, the address register is cleared, the response counter is indexed, and the computer proceeds to cycle one in order to count down the next response delay. However, if all the responses have been processed, or if the start display switch is set, then the computer will proceed to the display mode.

Section 3.7 Display Mode

The display mode may be entered in any cycle. The only action which occurs during the display mode is in cycles zero and one. In cycle zero, the contents of the memory register indicated by the AR are read into the accumulator, then written back into the memory with no change. The register is cleared, the address register is indexed, and a new read write display cycle begins.

If the stop display switch is set, the computer will return to its original data processing mode at the end of the display mode cycle one. When the computer returns to its normal data processing mode, it enters the mode in the same manner as the mode is entered after set up.

CHAPTER IV

TECHNICAL DESCRIPTION OF THE LOGICAL CIRCUITRY OF THE DARC

The DARC is divided into function sections as shown in the DARC diagram (Figure 2.2). Input signals in each group are labeled with their logical function and point of origin, except time pulses and control gating matrix outputs, which are labeled with their logical function only. Darkened arrow or pulses indicate signals which are negative (-3 volts) for the corresponding logical state. Open arrows or diamonds indicate a ground or positive signal for the corresponding logical state.

The logical elements are based on a commercially available line of packaged circuit modules manufactured by Digital Equipment Corporation (DEC). The notation used for these modules (Appendix A) corresponds to that used by the manufacturer. Timing and loading restrictions for these modules have been taken into account. Therefore, using the DEC Modules, the computer may actually be constructed from the drawings shown here.

DEC model numbers corresponding to the logical elements used are shown with each drawing. The logical and electrical characteristics of the most frequently used modules are briefly described as follows:

The transistor inverter is the principle gating element. When the emitter is grounded, the inverter amplifies and inverts the signal applied to the base, i.e., when the base is at -3 the collector will be at ground and vice versa. If the emitter is used for gating, the collector output will be at ground only if the emitter is at ground and the base is negative, thus forming an AND gate. Either a negative emitter or a grounded base will cause the collector output to be at a negative voltage, thus forming an OR gate. The inverter may be used as either a pulse gate or a level gate. If the inverter collector is not connected to another load, such as a flip-flop input or the emitter of another level gate, a clamp load resistor is attached to assure the proper negative output signal.

Diode gates are simply inverters with a number of diodes attached to the gate input to allow multiple input signal isolation. These units are used to form AND gates and OR gates which present a lighter load at the input than the standard inverter.

The unbuffered flip-flops are used in the counting circuits. They employ a differentiating level type of carry propagation which requires that the capacitive

loading be relatively light and output leads be kept short. However, the flip-flops have a carry propagate time of only 50 nanoseconds per stage and are available four to a single package. Each flip-flop has two output terminals, a complement input terminal, and a direct clear input terminal. The clear signal is a 1 microsecond positive level which is made either from a delay unit or from another flip-flop. The flip-flops may be individually set by grounding the ZERO output terminal with a 2 input diode gate.

The buffered flip-flops have a considerably higher output driving ability than the unbuffered flip-flops. Each flip-flop includes ONE and ZERO outputs, two set inputs, two clear inputs, two complement inputs, and two P pulse outputs. Inputs may come from inverter pulse gates, or they may be positive pulses from a pulse amplifier. Whenever a complement input terminal is pulsed, a standard DEC negative pulse will appear at the corresponding P pulse terminal. This pulse, gated with the ZERO level output, is used for carry propagation. (The level output has a built in delay to assure that it will not be changing while the P pulse is present.) Buffered flip-flops in dual circuit packages, such as used in the AD, are not as elaborate as the above, but operate in the same manner.

The pulse amplifier shapes and amplifies DEC standard pulses. Either positive or negative pulses are available from the output.

The pulse generator produces a standard DEC negative or positive pulse from a negative going level change or a push button.

The delay one shot is used for delaying pulses or for producing specified duration levels. The level output will produce -3 volt signal for the duration of the delay. The pulse output will produce either positive or negative pulses at the completion of the delay.

Section 4.1 Analog-to-Digital Converter

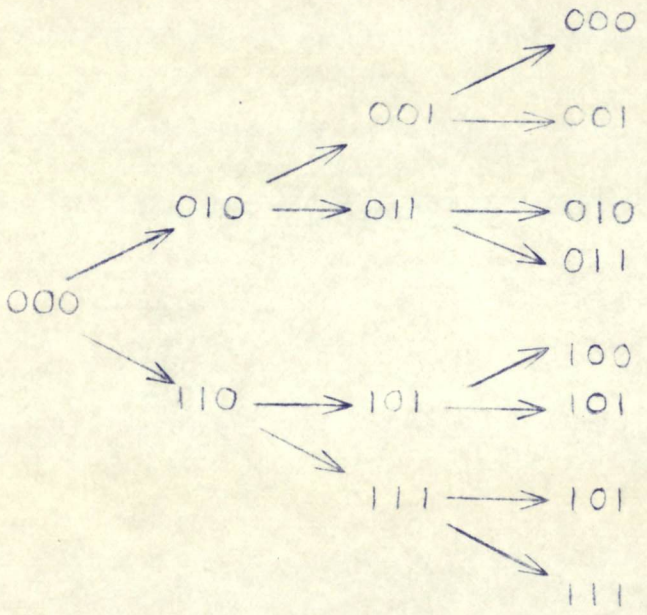
The analog-to-digital converter receives the neuroelectric input signal. In the averaging and amplitude histography modes, it converts this signal to a six bit, ONEs complement binary number. In the time and interspike histography modes, the converter determines when the input signal exceeds a threshold voltage level.

The converter consists primarily of a 6 flip-flop register, a weighted ladder network for digital-to-analog conversion, and a difference amplifier for comparison of the ladder network output voltage with the input analog signal.

In the interspike and time histography modes, the converter register is set to the number indicated by the TV (threshold voltage) toggle switch register. This number is converted to an analog voltage by the ladder network and is constantly compared to the input analog signal. When the analog signal exceeds the ladder network output, a pulse goes to the spike synchronizer flip-flops in the control circuitry.

In the averaging and amplitude histography modes, the AD will convert the input analog signal into a digital number, using a successive approximation method. The converter register is preset to the first approximation by the start convert pulse. This digital number is converted to an analog signal and compared with the input voltage. If the analog equivalent of this number is greater than the input voltage, then the first convert pulse will decrease the number in the converter. If the analog equivalent of the digital number is less than the input signal, then the second convert pulse will increase the number in the register. This process is repeated five more times.

Figure 4.1 illustrates the successive approximation method for conversion to a 3 bit binary number. The



SUCCESSIVE APPROXIMATION CONVERTER METHOD

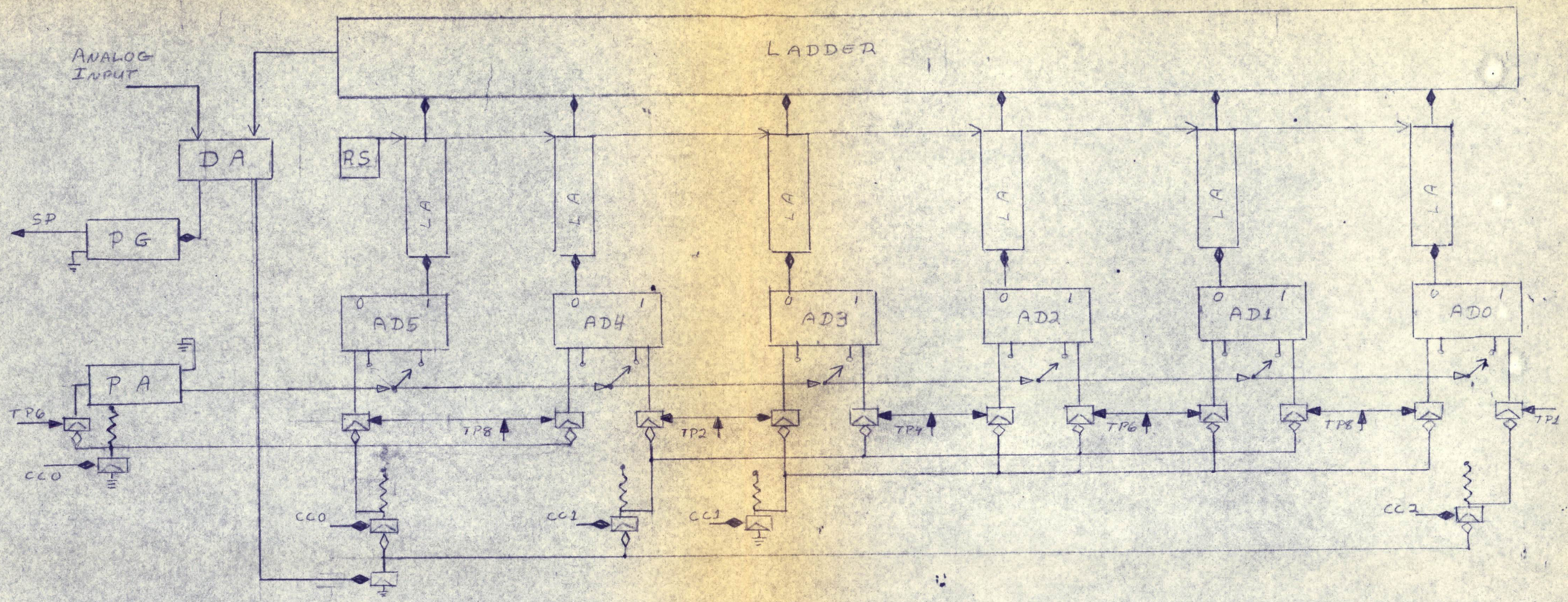
FIGURE 4.1.

reader can easily extrapolate to the case of the six bit converter.

Since digital circuitry does not use voltage levels of the accuracy required for analog circuitry, level amplifiers are placed between the flip-flop outputs and the inputs to the ladder network. The level amplifiers, driven by a reference power supply, produce very precise 0 and -10 volt outputs, depending on the state of the corresponding flip-flops.

Since the D to A converter is a completely passive resistor network, the analog output voltage will be in the range of 0 to -10 volts. The input analog signal should be amplified to produce a total voltage swing of 10 volts and should be biased to -5 volts. However, the input signal will still be converted to the proper positive or negative number in the ONEs complement number system. The digital ZERO, will correspond to -5 volt analog signal. This is accomplished by connecting the ladder network to the ONE output of the sign flip-flop and to the ZERO outputs of all other flip-flops.

The converter requires 3 microseconds between conversion pulses and 2 microseconds after the last pulse for settling. Should it be desired at any time to increase the speed of the converter, the flip-flops and inverters may be placed by their DEC high speed equivalents



3	Dual Flip Flops	Type	4209
1	Pulse Generator	"	4410
1/3	Pulse Amplifier	"	4603
2	Inverters	"	4106
1	Difference Amp.	"	1547
1	Ladder Network		1561
1½	Level Amplifier	"	4677
1	Reference Supply	"	1562

Analog to Digital Converter

Figure 4.2

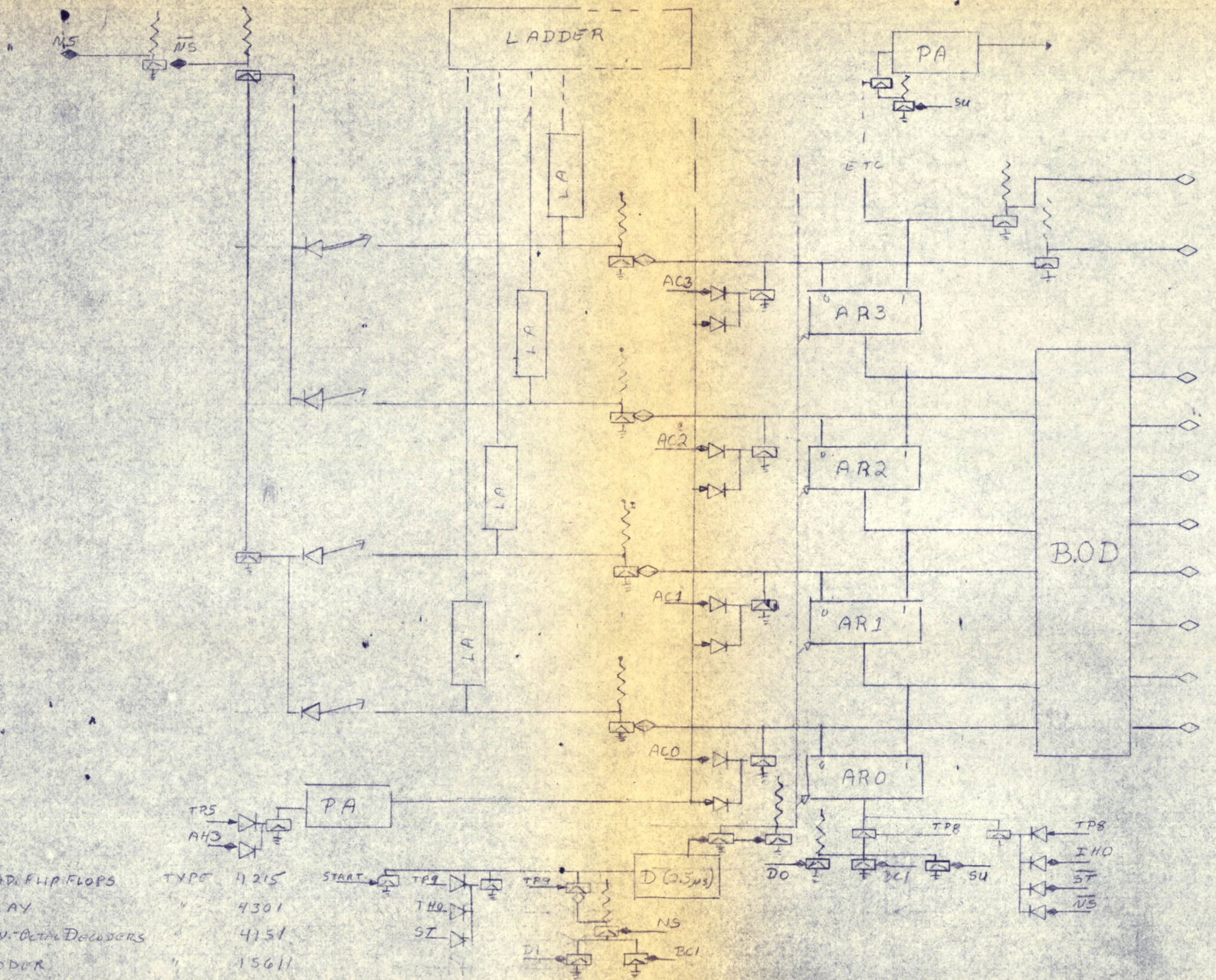
(flip-flops Type 1209 and inverters Type 1103 or 1105). The converter will then require only 1.8 microseconds between pulses and .2 microseconds after the last pulse.

Section 4.2 Address Register

The address register is used to select the proper word in memory and to determine when the desired number of samples have been processed. The register is an 8 flip-flop counter with provisions for parallel read in from the accumulator.

To avoid overloading the flip-flop outputs, buffer inverters are used at the ZERO output terminals. These inverters supply indicator drivers, level amplifiers, and a diode gate. The level amplifiers are used with a ladder network to supply the analog output signal for the X coordinate of the CRT. The diode gate, connected to the inverter buffers through the NS toggle switches, is used in determining when the desired number of samples have been processed. The ONE outputs of the AR flip-flops are fed to binary-to-octal decoders, and buffer inverters for connection to the memory drive circuitry.

Read in to the AR from the accumulator is a two step process. All flip-flops are cleared and then ONEs are read in, via the two input diode gates. At present, this



2	QUAD. FLIP-FLOPS	TYPE	4215
2	DELAY	"	4301
2	BIN.-OCTAL DECODERS	"	4151
1	LADDER	"	15611
2	LEVEL AMPLIFIERS	"	4677
1	PULSE AMPLIFIER	"	4603
3	INVERTERS	"	4106
½	DIODE GATES	"	4111
1	DIODE GATES	"	4113
1	DIODE GATES	"	4115
3/9	INDICATOR DRIVER	"	1669

ADDRESS REGISTER

FIGURE 4.3

feature is used only in the amplitude histography mode. Since the number read in originates at the AD, it would, be equally feasible to read this number directly from the AD. However, this circuitous method involves little extra cost and greatly increases the flexibility of the machine for incorporating other modes at a later date.

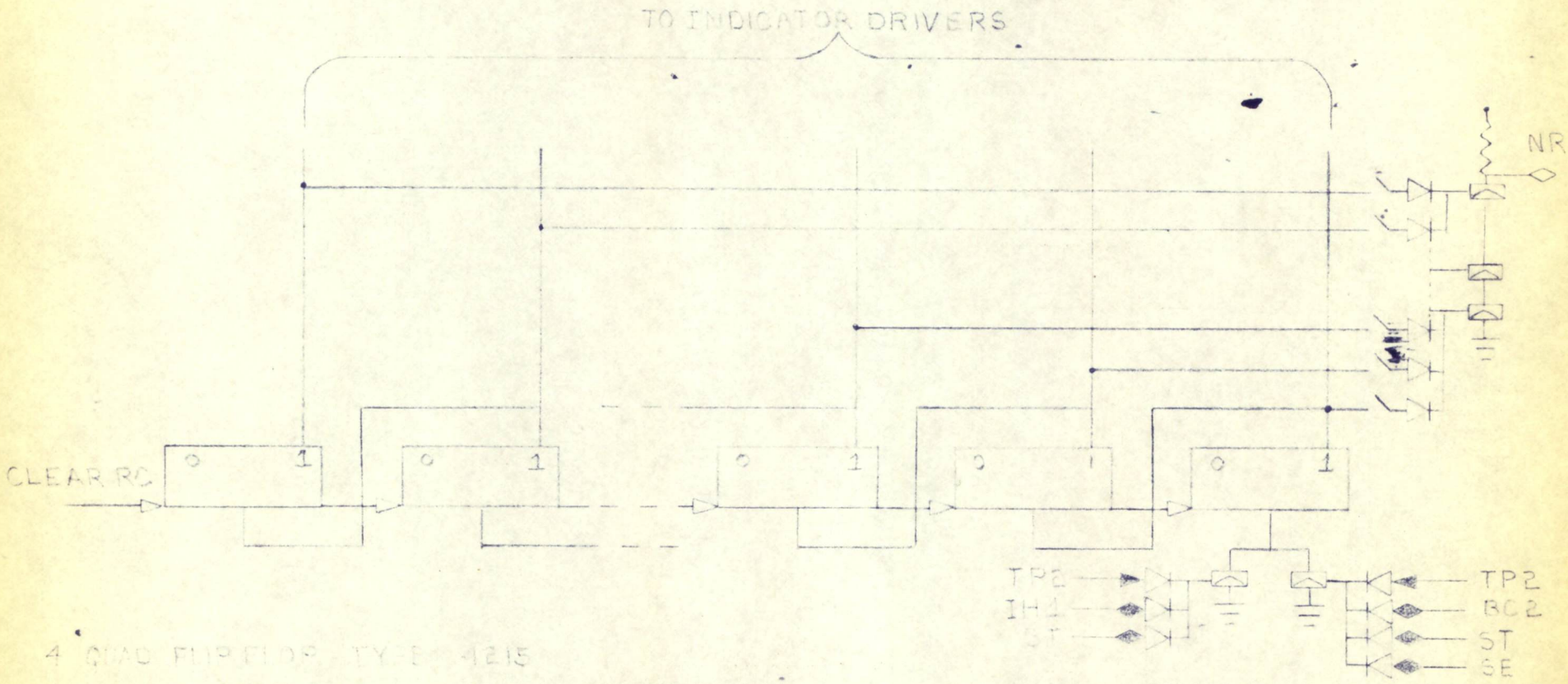
The AR clear signal is provided by a delay unit set for its minimum delay of 2.5 microseconds. This may be decreased to 1 microsecond; if the delay is replaced by its high speed equivalent, DEC Model 1304.

Section 4.3 Response Counter

The response counter serves simply to count the number of responses which have been processed and determine when the desired number is reached. The number of processed responses is indicated by lights on the control panel.

The RC is a simple 16 bit counter with a set of diode gates connected, through the NS toggle switches, to the flip-flop outputs to determine when the preset number of responses have been processed. Indicator lights are included to drive the visual display on the control panel.

The indicator drivers and toggle switch register should be located in close proximity to the counter in order to avoid excessive capacitive loading.



4 QUAD FLIP FLOP, TYPE 4215
1 DIODE GATE " 4111
1 DIODE GATE " 4115
1⅛ INDICATOR DRIVER " 4169

RESPONSE COUNTER

FIGURE 4.4

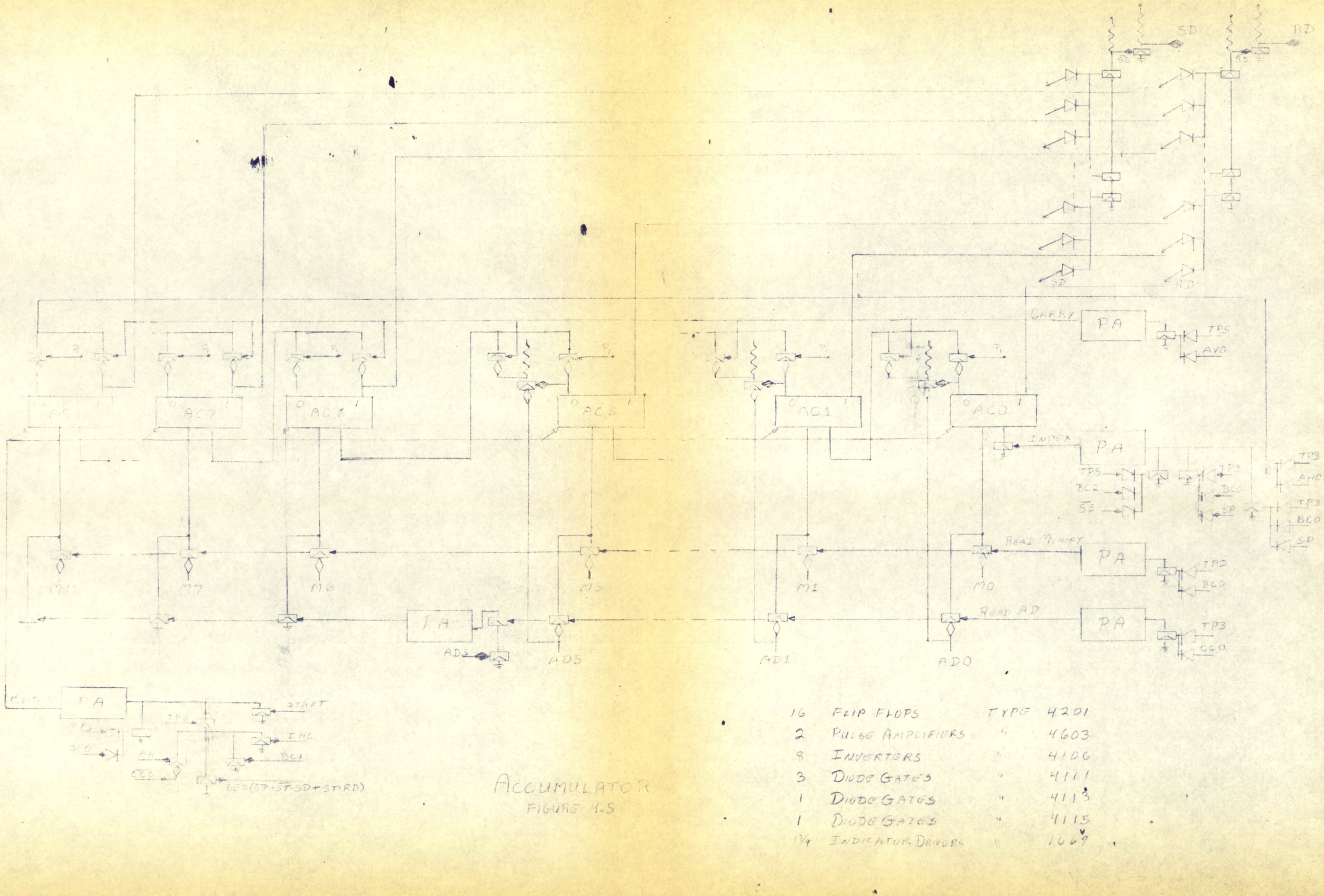
Section 4.4 The Accumulator

The accumulator is used for summing two numbers, transferring information, and counting out artificial delays.

The first six stages include complete addition circuitry, including, of course, carry propagation circuitry. The last ten stages include a modified addition circuitry.

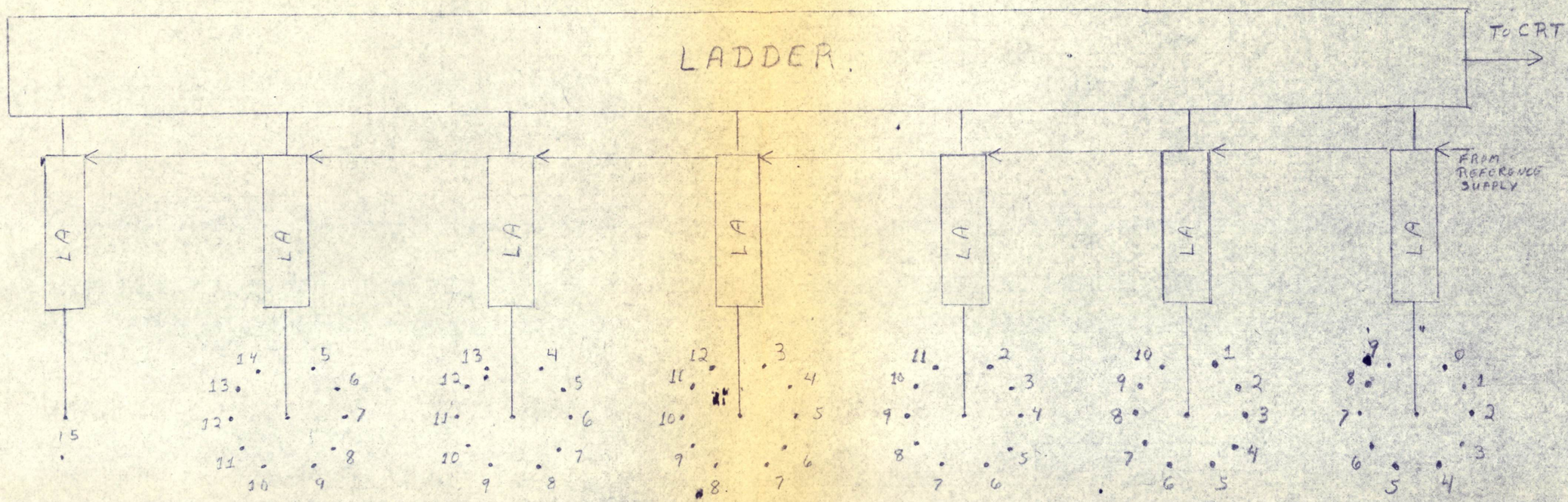
The accumulator is indexed by pulsing the C_1 input terminal of the first flip-flop. The carry is propagated by the coincidence of the P_1 pulse and a ground output signal from the ZERO terminal of the flip-flop. This circuitry is employed for all 16 flip-flops in the accumulator.

Read in from the memory or the AD register is done by complementing the C_2 input terminals of the flip-flops. If the accumulator has been previously cleared, the read-in action will transfer to the accumulator, the same number as was in the memory or the AD. If the accumulator has not been previously cleared, a partial add will be implemented. Since the six bit AD register may contain a negative number, special provisions have been included for complementing all of the most significant ten bits of the



ACCUMULATOR
FIGURE 4.5

16	FLIP FLOPS	TYPE	4201
2	PULSE AMPLIFIERS	"	4603
8	INVERTERS	"	4106
3	DIODE GATES	"	4111
1	DIODE GATES	"	4113
1	DIODE GATES	"	4115
1½	INDICATOR DRIVERS	"	1669



2 LEVEL AMPLIFIERS TYPE 4677
1 LADDER NETWORK " 1561

NUMBERS INDICATE CONNECTIONS FROM ZERO OUTPUT TERMINALS OF CORRESPONDING ACCUMULATOR FLIP FLOPS (EXCEPTION— 15 FROM ONE OUTPUT OF AC15)

SCALE FACTOR SWITCH

FIGURE 4.6

accumulator, if the most significant bit of the AD is a ONE.

Complete addition is implemented by reading both M and AD, then pulsing the carry line. The carry line will generate a carry pulse whenever a bit in the AC is in the ZERO state and the corresponding bit of the AD is in the ONE state. This carry pulse will enter the C_1 input terminal of the next most significant bit and will continue to propagate in the same manner as in the indexing operation.

The outputs of the accumulator go to indicator drivers for driving a visual display, to the address register, through the RD toggle switch register to a diode gate, and through the SD toggle switch register to another diode gate. The two diode gates are used to determine when the necessary artificial delay has been counted out.

The accumulator outputs are also connected, through the scale factor switch, to level amplifiers, then to a ladder network for supplying the Y coordinate to the CRT.

Section 4.5 Control Timing

The control timing governs the sequence of operation of the entire computer. The control is divided into three sections as shown in dotted lines on the control block diagram, Figure 4.7.

Figure 4.8 shows the delay loop, the set-up flip-flop, and the cycle counter. When the start button is pushed, a standard pulse is generated by the start pulse generator. This is used to clear all flip-flops except the SE, which is set, and to insert a pulse into a delay loop. The delay loop provides flexible timing. This may be adjusted to compensate for desired changes in other sections, such as decreasing the memory cycle time.

Time pulse 9 is used for indexing, clearing, or presetting the cycle counter. The outputs of the two flip-flops in the cycle counter are gated together to produce the four cycles. These are also gated with the outputs of the setup flip-flop for use by the control gating circuitry.

The gated outputs of the cycle and setup flip-flops are shown entering the control gating circuitry in Figure 4.9. Here they are gated with signals from the mode switch and the display flip-flop in order to produce signals indicating the mode and cycle. These are further gated together to produce the common cycles.

All outputs from the control gating matrix are negative for asseration; i.e., negative for the logical state indicated.

Figure 4.10 shows the spike, stimulus and display flip-flops. The spike and stimulus signals occur at random with respect to the main machine timing and are synchronized to the main machine timing. For example, the randomly occurring spike signal sets SP1, producing a randomly changing level. Flip-flop SP2 converts the randomly changing level into a level that changes at known times only. The output of SP2 is then sampled at a time when it is known that the conditioning level is constant.

The first display flip-flop is gated in such a way that it can be set only at the end of the data processing cycle. The display mode begins immediately when D1 is set and continuous as long as D1 or D2 are in the ONE state.

The process of leaving the display mode is somewhat ackward, since it is necessary to ascertain when the display mode is about to end. This is to insure that the cycle counter will be properly preset for returning to the data processing mode. Hence, the stop display switch is read by time pulse 7. If the display is to end, D1 will go to the ZERO state, but D2 will remain in the ONE state until time pulse 9. This produces a special D* signal which is available for conditioning the input to the cycle counter on time pulse 9.

FIGURE 4.9

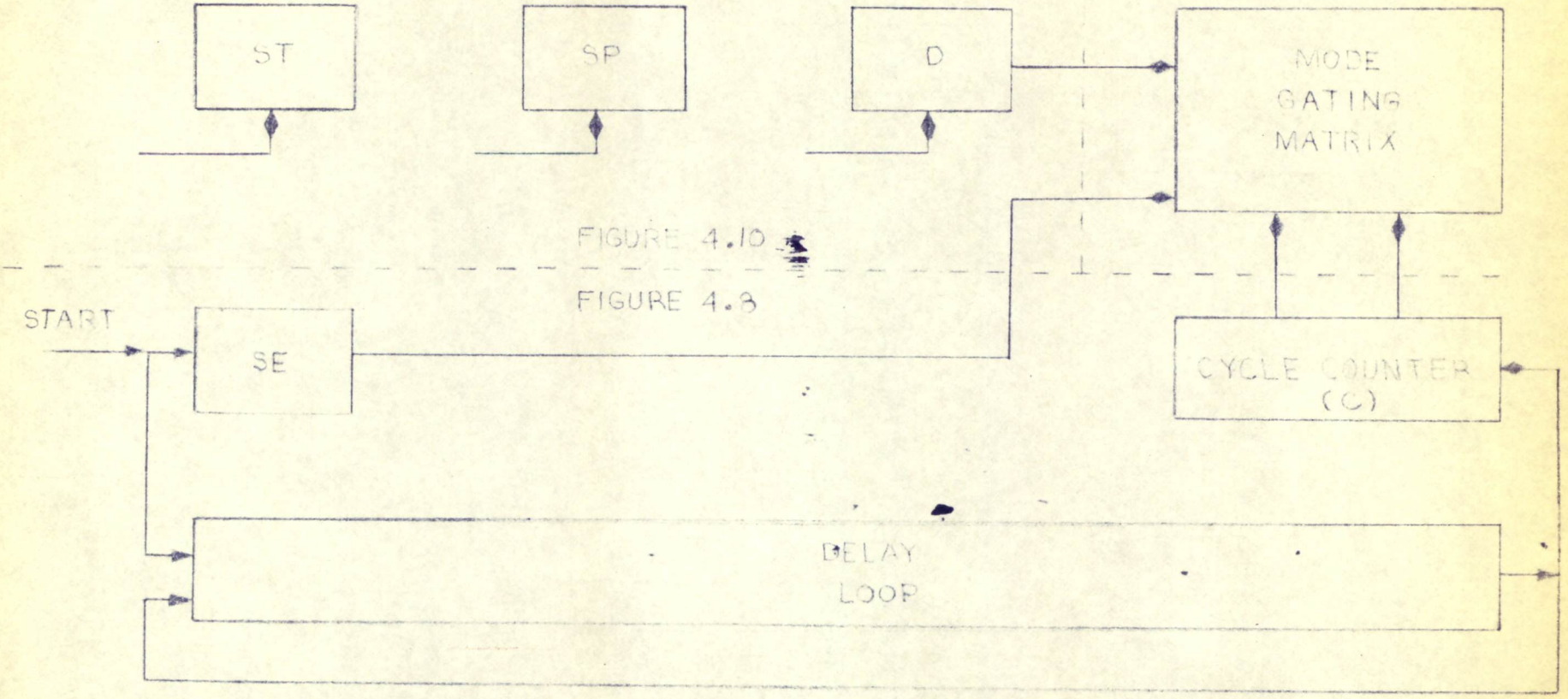
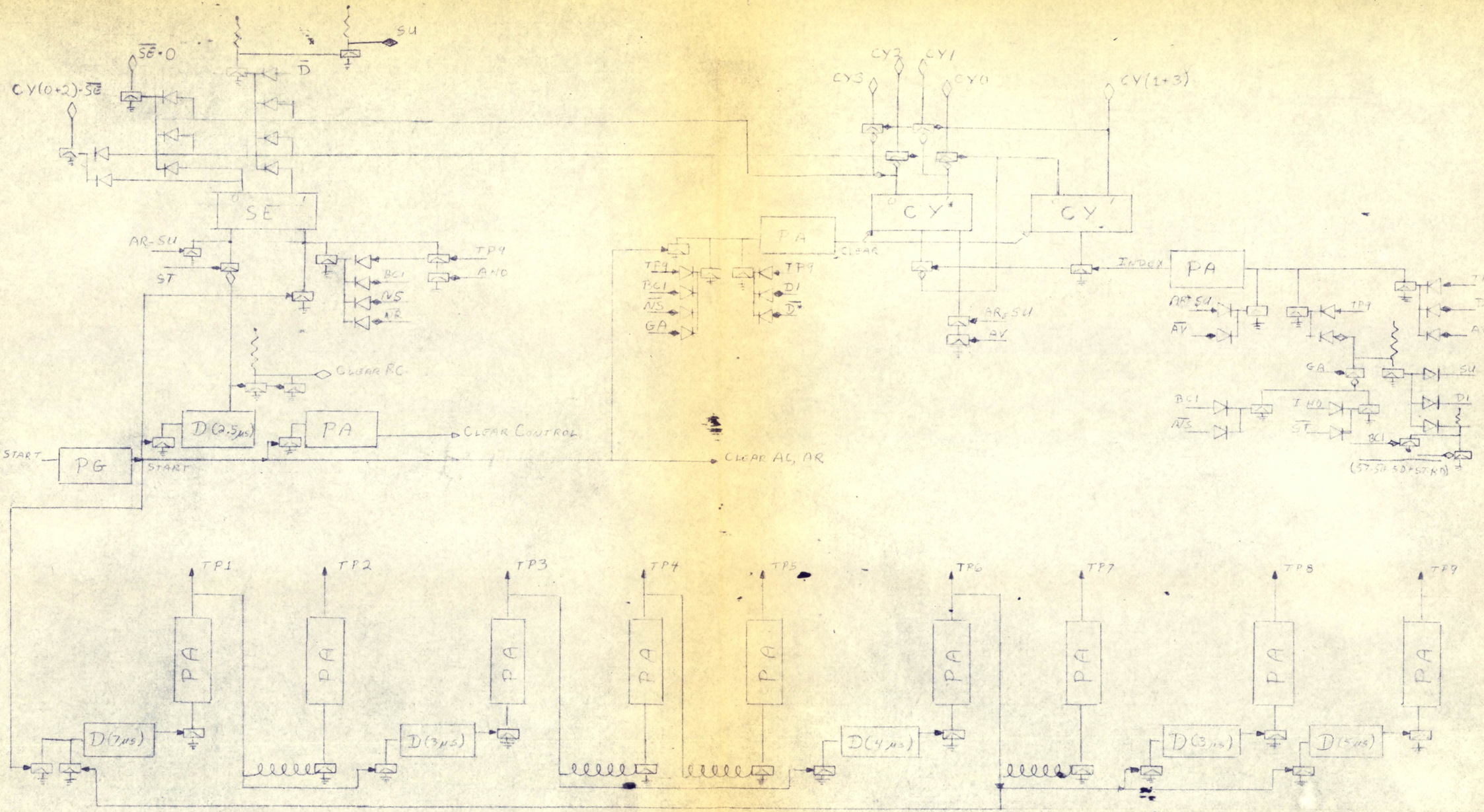


FIGURE 4.10

FIGURE 4.8

CONTROL
BLOCK DIAGRAM

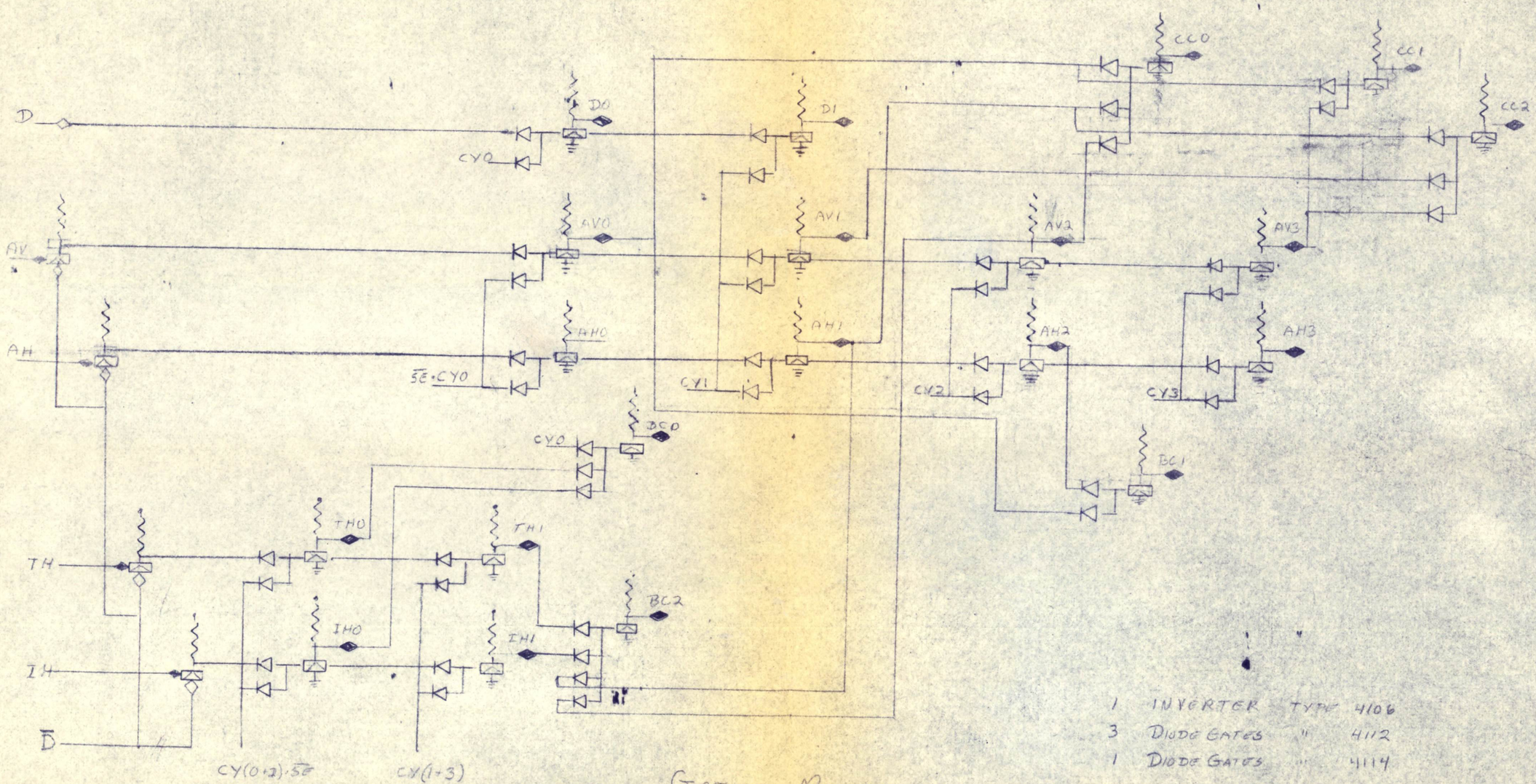
FIGURE 4.7



1	PULSE GENERATOR TYPE	4410
4	PULSE AMPLIFIER "	4603
6	DELAY ONE SHOT "	4301
4	DELAY LINES "	1310
2	DUAL FLIP FLOPS "	4209
2	INVERTERS	4106
2	DIODE GATES	4115
1	DIODE GATES	4113
¼	INDICATOR DRIVER	1649

CONTROL
(SE, CY, AND DELAY LOOP)

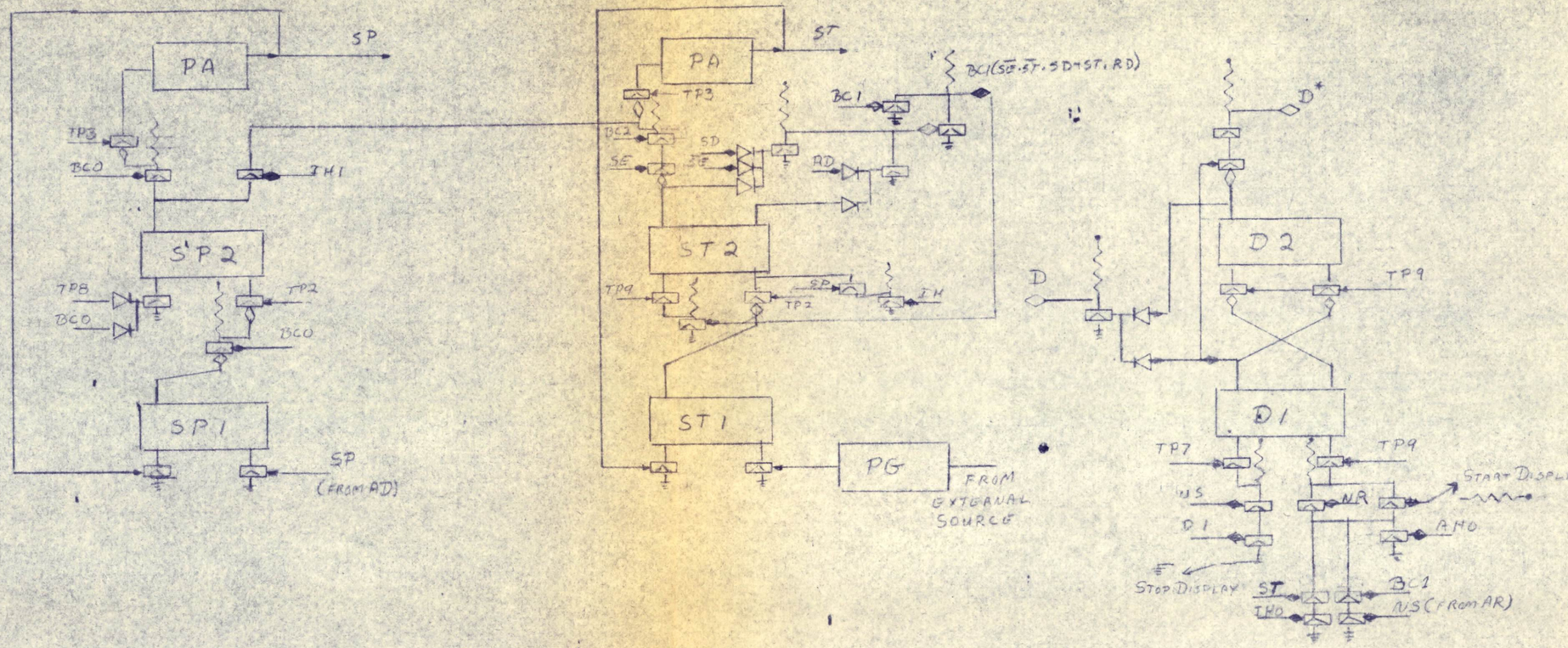
FIGURE 4.8.



1	INVERTER	TYPE	4106
3	DIODE GATES	"	4112
1	DIODE GATES	"	4114

GATING MATRIX

FIGURE 4.9



3	DUAL FLIP FLOPS	TYPE	4209
2/3	PULSE AMPLIFIER	"	4603
1	PULSE GENERATOR	"	4410
1	DIODE GATE	"	4113
4	INVERTER		4105
1/4	INDICATOR DRIVER		1649

CONTROL
(ST, SP, D)

FIGURE 4.10

CHAPTER V

CONCLUSIONS

The advantages of the DARC for doing bio-physical research are manifold. Perhaps the foremost advantage is its ability to be used on line. In the averaging mode, the average can actually be viewed on the CRT while the data is being received and processed. In all modes, provision is made to break into the program for a constant display. This allows the experimenter to photograph the data at various stages, and also to check for any irregularities.

The DARC is an extremely fast computer. In the averaging mode, the input may be sampled, processed, and recorded and the results displayed in 28 microseconds. In the amplitude, time, and interspike histography modes, a sample may be taken, processed and recorded in 14 microseconds.. Should the experimenter desire to increase the speed of the averaging mode, for multi-channel inputs or other reasons, he may do so by simply changing the analog-to-digital converter and adding a flip-flop buffer to drive the display.

The DARC will do all necessary data processing from analog input to CRT output. The only auxiliary equipment required is the sensing equipment, and the preamplifiers

to increase the neuro-electric signal from the millivolt range to the volt range.

The packaged circuit modules, on which the design of the DARC is based, are highly reliable. Past experience with systems constructed from these modules has revealed an unusually low amount of down time. By going through a simple maintenance routine once a week, the experimenter should be able to foresee and easily find the source of any possible difficulties.

The cost of the DARC is quite attractive. The cost of the logic modules used in this design is $7,898. The cost of the mounting panels to house these units and the power supplies is approximately $1,470. The estimated cost of the memory and memory drive circuitry is $6,290. To this must be added the cost of the CRT, the cabinets and control panel, and assembly cost.

The DARC is a very flexible special purpose computer. Although the addition of alternate data processing modes must, of course, involve some additional circuitry and wiring; the use of packaged circuit modules and the common modes keeps this at a minimum. The three examples of alternate modes shown here required only some additional gating circuitry, one pair of synchronizer flip-flops, and

one extra set of read-in gates. By allowing extra space in the cabinet, it would be possible to add alternate modes such as these to the basic DARC at any later date.

The logical design described herein is intended to serve as a generalized pattern for a specific machine. The basic design is intended to be as independent as possible of the various parameters. Thus using this as a guide, the bio-medical experimenter can actually construct a DARC which will fit his particular requirements. Most parameters have been assumed for ease of description; however, word size, memory size, analog-to-digital converter size, and memory cycle time, can be altered without changing the basic design. Additional features such as multi-channel inputs or alternate read-out methods could also be incorporated.

Appendix A

DARC NOTATION

Block Notations

M = Memory

AC = Accumulator (Memory Buffer)

AR = Address Register

AD = Analog-to-Digital Converter

RC = Response Counter

CRT = Cathode Ray Tube

Modes

AV = Response Averaging Mode

AH = Amplitude Histography Mode

TH = Time Histography Mode

IH = Interspike Histography Mode

SU = Set-Up Mode

D = Display Mode

Control Flip-flops

C = Cycle Counter

D = Display Control

SE = Set-Up Control

ST = Stimulus Synchronizer

SP = Spike Synchronizer

Other Control Signals

NR = Number of Responses to Be Processed

NS = Number of Samples Per Response

RD = Response Delay (between stimulus and first sample)

SD = Sample Delay (between samples)

GA = No Sample Delay (Go Ahead)

AR* = Address Register Full

Timing Notation

TP1 - TP9 = Time Pulses

CY0 - CY3 = Cycle Times

AV0 - AV3 = Average Mode Cycles

AH0 - AH3 = Amplitude Histogram Cycles

TH0 - TH1 = Time Histogram Cycles

IH0 - IH1 = Interspike Histogram Cycles

SU = Set-Up Cycle

D0 - D1 = Display Cycles

D* = Temporary Display (About to Return to Principle Mode)

BC = Memory Buffer Common Cycles

CC = Analog-to-Digital Converter Common Cycles

Module Notation

FF	=	Flip-Flop
PA	=	Pulse Amplifier
PG	=	Pulse Generator
DA	=	Difference Amplifier
D	=	Delay One Shot
BOD	=	Binary-to-Octal Decoder
LA	=	Level Amplifier
RS	=	Reference Supply

DARC SYMBOLOGY

Signals

-3 volt level for logical assertion

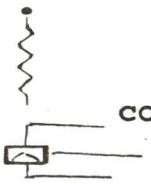
Ground level for logical assertion

Standard negative pulse

Standard positive pulse

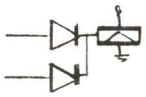
Switch or nonstandard level

Circuit Elements

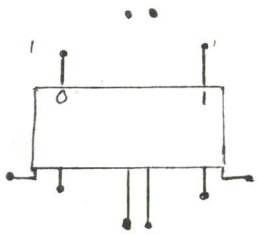


Clamped load resistor

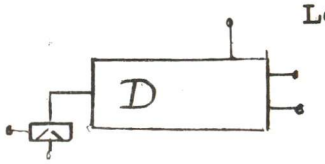
Inverter



Diode Gate



Flip-flop



Level output

Pulse output

Delay one shot

Delay line

Others as labeled

Appendix B

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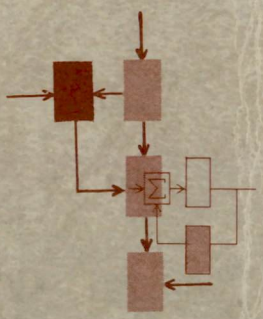

A HIGH-SPEED ANALOG-TO-DIGITAL ENCODER

by

Donald Allen Savitt

August, 1957

Servomechanisms Laboratory

MASSACHUSETTS INSTITUTE OF TECHNOLOGY, CAMBRIDGE 39, MASSACHUSETTS

Department of Electrical Engineering

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S.B., Illinois Institute of Technology
(1956)

SUBMITTED IN PARTIAL FULFILLMENT OF THE

REQUIREMENTS FOR THE DEGREE OF

MASTER OF SCIENCE

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

August, 1957

Signature of Author _____
Department of Electrical Engineering, August 19, 1957

Certified by _____
Thesis Supervisor

Accepted by _____
Chairman, Departmental Committee on Graduate Students

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DONALD ALLEN SAVITT

Submitted to the Department of Electrical Engineering on August 19, 1957, in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering.

ABSTRACT

An electronic encoder for converting an analog voltage to a seven binary digit parallel representation at a 50 kc encoding rate has been designed, constructed, and tested. The encoder operates on voltages in the zero to fifty volt range and is capable of being time-shared by a multiplicity of inputs. Use of the cascade encoder technique permits a design requiring no timing circuits.

The encoder was designed for use as an input device for a proposed analog-digital flight simulator.

Thesis Supervisor: Alfred K. Susskind

Title: Assistant Professor of Electrical Engineering

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Completion of this project was only possible because of the assistance of technician P. Snow who did most of the construction, Miss M. Bruno who completed the typing in record time, and the Servomechanisms Laboratory drafting room which did all of the figures.

This work was sponsored by the U.S. Naval Training Devices Center under D.S.R. Project 7591.

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CHAPTER I

INTRODUCTION

1.1 ENCODER PERFORMANCE

An electronic encoder has been developed which converts an analog voltage to the corresponding parallel seven binary digit representation at a 50 kc encoding rate. The encoder is capable of being time-shared by a multiplicity of 0-50 volt inputs.

Performance tests indicate that it may be possible to achieve eight binary digit conversions at encoding rates as high as 80 kc with the present design.

1.2 PURPOSE OF THE ENCODER

The encoder was developed for use with the analog-digital computer designed by DSR Project 7591 under the sponsorship of the U. S. Naval Training Device Center.[1] The computer is suitable for the real-time simulation of complex non-linear physical systems, the particular application being an operational flight trainer.

The computer performs all mathematical operations except integration in the digital domain. This makes it easier to generate non-linear functions, to make changes in the functions being generated, and to obtain the desired accuracy.

Integration is performed in the analog domain because the resultant abbreviation of the digital computer program assists in the achievement of real-time simulation.[1] Analog integration has the added advantage of smoothing the data.

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[1] Superscripts refer to references listed in the bibliography.

The operational flight trainer instruments and controls and the integrators operate in the analog domain. Hence, both an analog-to-digital encoder and a digital-to-analog decoder are required to tie-in the computer and trainer. The decoder converts digital variables into analog voltages for the purpose of performing integration, or for the purpose of operating the trainer.

The encoder is needed to convert analog voltages from the integrators into digital form for further mathematical operations and to supply the computer with information from the analog flight trainer. One encoder is time-shared by the various analog inputs. The computer sends a command for a particular analog variable to the encoder in a manner similar to the way the computer addresses its own memory.

The computer requires an eight binary place (including sign) output from the encoder. The output must be available 10 microseconds after the computer has given the encode command and the minimum interval between commands is 32 microseconds. The encoder will be multiplexed between approximately 20 input voltages whose frequency components are less than 5 cps.

1.3 TYPES OF ENCODERS

Analog-to-digital encoding techniques are of two types: electro-mechanical and electronic.

Electro-mechanical encoders convert an angular shaft position to a digital representation.[2] This is commonly accomplished by mounting code discs on the shaft. The discs are made with a pattern of either conductive material on a non-conductive disc for brush pick-off, or opaque coating on

a glass disc for photo-electric pick-off. The pattern is designed so that brush or photo-tube signals correspond to the digital representation of the instantaneous or the incremental change in shaft position.

Shaft encoders have been built with resolution as high as one part in 65,536.[2] The encoding rate can be made very high since it is dependent only upon the rate at which brush or photo-tube current can respond. However, the mechanical limitations of the shaft position system prevent its usage when multiplexing inputs and limit the frequency range of variables which can be encoded.

Electronic encoders are classified into three general types:

a. Time encoders

b. Space encoders

c. Voltage encoders

a) Time domain encoders convert the voltage to be encoded into a corresponding period of time.[3,4,5] Clock pulses are gated into a counter during this period of time, resulting in a final count proportional to the analog input. Voltage-to-time period conversion is accomplished by a linear sweep generator and a comparator circuit.

The linear sweep circuit produces a pulse at the beginning of the sweep, opening a gate and allowing clock pulses into the counter; this gate remains open until the sweep voltage becomes equal to the input, at which time the comparator produces a pulse closing the gate.

Time domain encoders can be made arbitrarily precise, but their accuracy is limited by sweep linearity and comparator accuracy. Encoding rates are restricted by the time required for the counter to count to its

maximum contents ($2^n - 1$ for an n-bit encoder).

b) Space domain encoders utilize a modified cathode ray tube.[6] The voltage to be encoded controls the vertical deflection at which the electron beam sweeps a code plate in the screen end of the tube. An anode plate is placed behind and parallel to the code plate. A pattern of apertures is cut in the code plate so that the electron beam may strike the anode and produce output pulses which are the serial binary representation of the vertical deflection of the sweep.

The accuracy of this encoder is determined by the precision with which the code plate is made and the electron beam cross-sectional dimensions. The encoding rate is mainly dependent upon the sweep rate and can be made in the megacycle region.[6] High cost and fragile nature of the special cathode ray tube and code plate are the main disadvantages.

c) Voltage domain encoders compare the voltages to be encoded with the decoded contents of a digital register; the sign of the error determines whether the register contents are increased or decreased. When the error is thus""servoed" to zero, the register contains the parallel binary representation of the voltage to be encoded.

The incremental encoder uses a backward-forward counter instead of a digital register.[7,8] The sign of the error determines whether clock pulses are used to count up or down. This type of encoder can follow rapidly changing input voltages as long as the counter can keep up. However, when time-shared by a number of inputs, the encoding rate must be slowed down to allow for a possible incremental counter change of full scale. In this case, the encoding rate will be determined by the time it takes the counter to count to full scale just as it was in the time domain

encoder.

The successive comparison encoder[9,10,14,16,25] starts the encoding cycle with an empty register; each flip-flop in the register is turned on in succession, starting with the one representing the largest bit. Whenever comparison indicates the decoded register contents to be larger than the voltage being encoded, the last flip-flop turned on is turned off again before the next bit is tried. Since only n operations are required to encode n binary bits, the encoding rate can be increased considerably over that of the time domain encoder. Rates as high as 40 kc for eleven bits have been achieved commercially.[11,16,25] Accuracy is limited chiefly by the register decoding and comparator circuits.

The cascade encoder[12,13,14] accomplishes encoding to n bits by use of n one-bit encoders in series. Each successive stage quantizes its input to the next smallest bit, produces a binary output of ONE or ZERO, and transmits the quantization error to the input of the next stage. The binary outputs constitute the parallel binary representation of the voltage being encoded with the most significant bit appearing at the first stage. Quantization error is the difference between the signal being encoded by a stage and the decoded value of the bit produced by that stage.

Cascade encoders are also designed so that each successive stage, instead of quantizing to the next smallest bit, multiplies its input by two and quantizes to the same largest bit.[12,13] In this way, each stage can be made identical.

Cascade encoders have the advantage that no timing, synchronization, or re-setting operations are required. Encoding rates are determined by the

speed at which a stage consisting of amplifier, comparator, and one-bit decoder can be made to operate and by the number of stages. Accuracy limitations result from accumulated drift (because of d.c. coupled stages) and non-linearity in the successive stages.

A variation of the cascade encoder technique time-shares one stage for the complete encoding.[12,15] The stage output is sampled, stored, and used after a short delay as the new input. Considerable savings in equipment are achieved over the n-stage cascade encoder, but timing and sampling now become necessary.

1.4 THE CASCADE ENCODER

1.4.1 Reason for Choosing the Cascade Encoder

A study of the encoding techniques discussed in Section 1.3 indicates that the voltage domain encoders show the most promise for attainment of higher speed and accuracy when used on a time-shared basis. Of the various types of voltage domain encoders, the cascade type was chosen for investigation because its lack of internal timing circuitry results in the highest encoding rates and least complexity for a given accuracy.

1.4.2 Transfer Characteristic of the Cascade Encoder Stage

The type of cascade encoder chosen is the one with identical stages (see 1.3). Since each identical stage produces one binary digit, it is possible to repeat the same circuit as many times as is required to obtain the necessary binary output precision (as long as the stage accuracy is not exceeded).

The function of each stage is to encode its input to one binary

digit, multiply the resultant quantization error by two, and transmit the result to the input of the next stage. Encoding to one binary digit is accomplished by comparing the stage input to the analog value of the most significant binary digit (one-half of full-scale input). If the input is larger than one-half of full scale, the binary output is a ONE; otherwise, the binary output is a ZERO. The quantization error is equal to the input if the binary output is a ZERO, and equal to the input minus one-half of full scale if the binary output is a ONE. Accordingly, the stage transfer characteristic may be expressed as follows:[12]

$$V_{n+1} = 2\,(V_n - A\,D_n)$$
$$D_n = 1 \quad \text{if} \quad V_n > A \qquad (1.1)$$
$$D_n = 0 \quad \text{if} \quad V_n < A$$

where V_n is the input to the nth stage, V_{n+1} the input to the $(n+1)$th stage, A the analog value of the most significant binary digit, and D_n the binary output of the nth stage.

1.4.3 Encoder Block Diagram

To achieve the above stage transfer characteristic, an inverter, a summing amplifier, and a Schmitt discriminator[17,18,19] are used. The encoder block diagram is shown in Fig. 1.

Operation is as follows: A read pulse opens a linear transmission gate (G), and gates in a positive variable voltage (X) for a period of time (T), long enough to perform the complete encoding operation. Each Schmitt circuit (S_1, S_2, ... S_8) is biased to discriminate against input voltages greater than A (one-half of full-scale input). If a Schmitt input is less

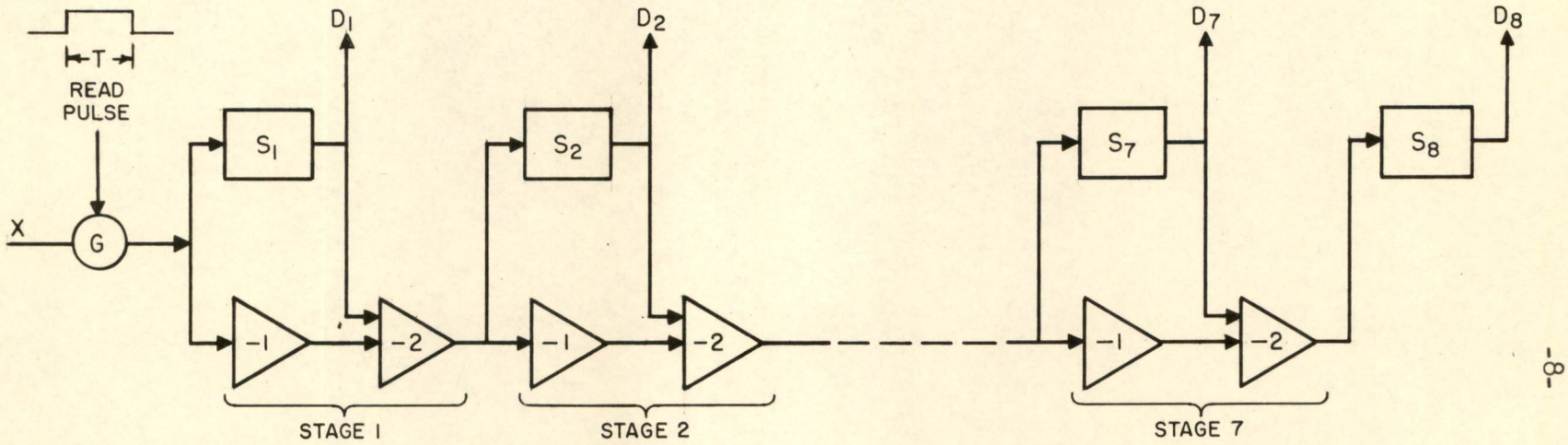


Fig. 1 Encoder Block Diagram

than A, the Schmitt output is zero and D_n is defined as a ZERO; if the input is greater than A volts, the Schmitt output is a positive-going step of A volts and D_n is a ONE. The positive stage input is multiplied by plus two in going through the cascaded inverter and summation amplifiers. However, if the stage input is greater than A volts, the discriminator supplies the summing amplifier with a signal A volts in magnitude and of opposite polarity from the signal from the inverter. The effect, then, is that A volts is subtracted from the stage input if the input is larger than A, and zero volts is subtracted if it is less than A. The stage output may thus be seen to be related to the stage input by Eq. 1.1.

Each stage operates on its input in an identical manner. The voltage level of the output of each Schmitt (zero or A volts) indicates the stage digital output (ZERO or ONE). The binary output of the first stage is the most significant digit, that of the second stage the next most significant digit, etc. The digital output of each stage is available as soon as its input arrives from the previous stage and its discriminator has operated.

To avoid the problem of amplifier drift, which would become a serious restriction on encoder accuracy as the number of cascaded stages is increased, the encoder components are capacitive coupled. The read pulse, in holding open the linear transmission gate for the interval T and then closing the gate, chops the input voltage X and presents the encoder stages with a square-wave input. Since the amount of time allowed for performing the encoding operation is 10 microseconds (see 1.2), this is the duration of the read pulse and input square wave. The period of the

complete encode cycle is the time between the arrival of successive encode commands from the computer (32 microseconds).

As the period of the highest frequency component in the input signals (X), is very large compared to the period of time that the linear gate samples the input, the amplitude of each individual square wave is essentially constant. If this were not the case, the linear gate would have to be replaced by a sample and hold circuit.[2]

Each of the quantities in Eq. 1.1 represent square wave amplitudes. The digital outputs, D_n, are therefore correct only for the duration of the input square wave. A means has been devised for reading out the digital outputs at the correct (see Chapter V).

It was found necessary to restrict the range of inputs to voltages of one polarity, in order that the square waves within the encoder would also be of one polarity. This permits clamping at the inputs of the Schmitt circuits, preventing a shift in discrimination bias due to accumulation of charge on the input coupling capacitor (see 2.2.3f). If the original variables to be encoded have a range of $\pm$ E volts, it is necessary to add $+$ E volts to the variable voltages at the input of the linear gates. The correct digital output can be calculated easily in the computer by subtracting the most significant digit from the encoder output.

The present encoder operates on an input range of 0 to 50 volts. The value of A in Eq. 1.1 is therefore 25 volts.

Photographs of the encoder are shown in Figs. 14 and 15 at the end of this report.

CHAPTER II

SCHMITT DISCRIMINATOR

2.1 REASON FOR CHOICE OF THE SCHMITT CIRCUIT

The Schmitt circuit[17,18,19] was chosen as the discriminator because its output exhibits a step discontinuity as the input passes the discrimination level, but is otherwise independent of input variations.

Simpler discriminator circuits utilize the non-linear on-off characteristic of a diode or multi-element tube.[17] The voltage input level with respect to some reference controls the conduction of the device. For inputs either above or below this critical value, the tube is cut off; for inputs on the other side of the critical value, the tube conducts. These circuits are undesirable for this application because their output is a function of the input in one of the two states and, in addition, does not exhibit a sufficiently sharp discontinuity at the discrimination level.

The Schmitt circuit consists of two stages in cascade, with positive feedback from output to input. Inputs above the discriminating level cut off the output tube; inputs below this level cut off the input tube. As a result, the Schmitt output is isolated from input variations while in either of these states. The Schmitt circuit utilizes positive feedback to cause an abrupt switching of output level when the input passes the discrimination level.

2.2 SCHMITT CIRCUIT THEORY

2.2.1 General Operation

The Schmitt discriminator operates in the following manner: (See Fig. 2).

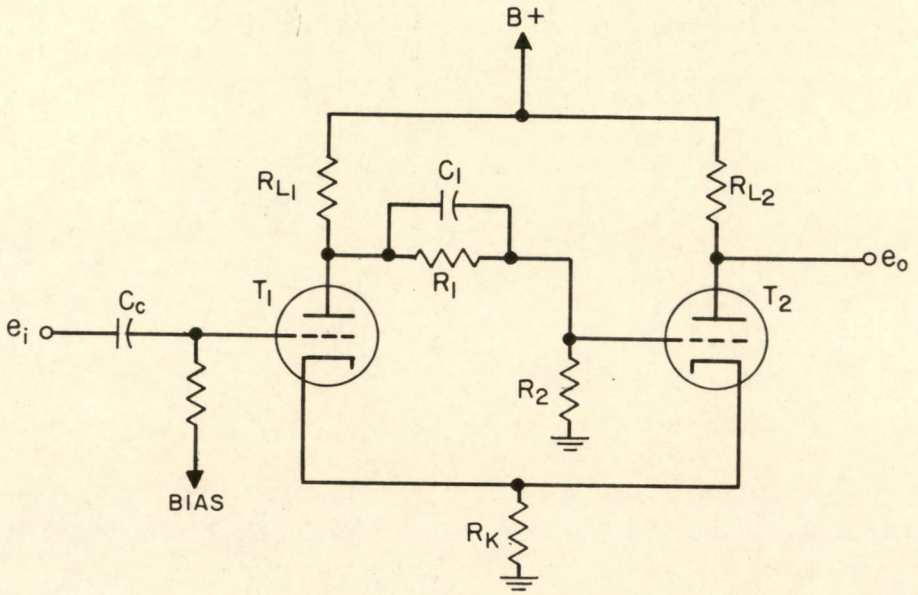


Fig. 2 Basic Schmitt Discriminator Circuit

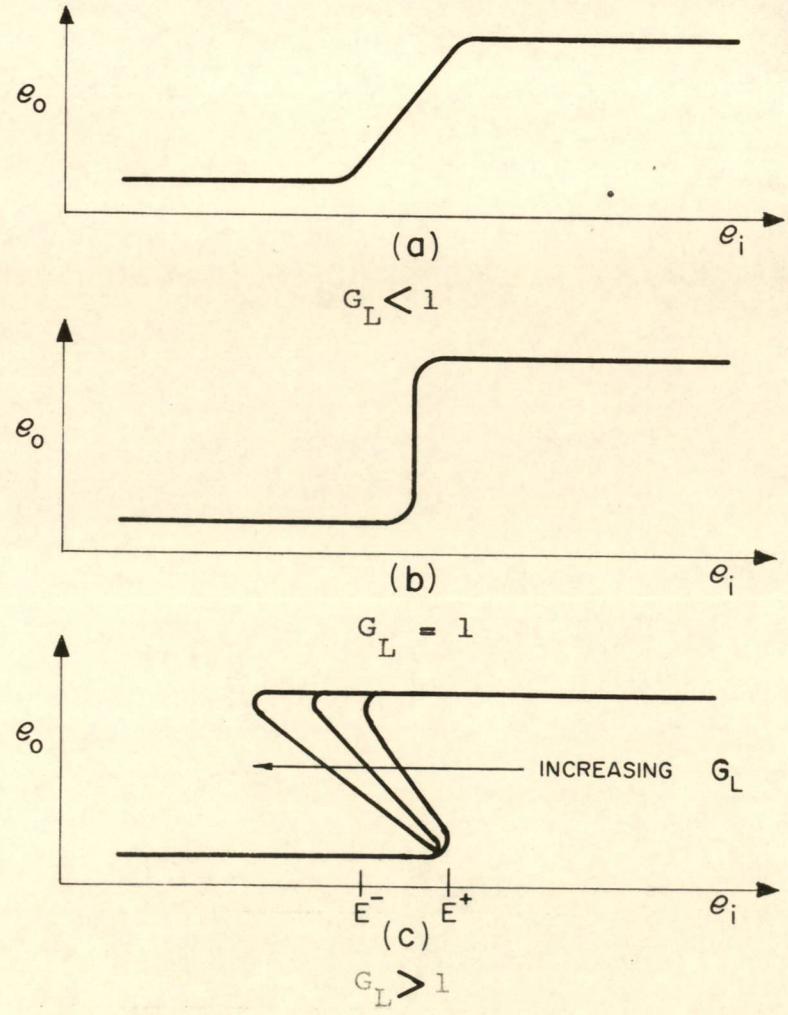


Fig. 3 Schmitt Input-Output Characteristic

For inputs, e_i, less than the discriminating (or triggering) level, T_2 is conducting and T_1 is biased below cut-off. The output, e_o, is at its lower value in this off state. A sufficiently large signal e_i will cause T_1 to conduct. The plate of T_1 will then drop, decreasing the voltage on the grid of T_2. As a result, the cathode potential decreases, causing an increase in the grid-cathode potential on T_1. The effect of this common-cathode positive feedback is to drive T_1 rapidly into conduction and T_2 into cut-off. The output, e_o, is then at its higher value in this on state.

2.2.2 Hysteresis

The value of input voltage e_i which causes the Schmitt circuit to change state depends upon whether e_i is increasing or decreasing through the discrimination level. This phenomena is referred to as "hysteresis." The following examination of the Scmitt input-output characteristic analyzes the causes of hysteresis. (See Fig. 3).

The gain of the Schmitt circuit is:

$$\frac{e_o}{e_i} = \frac{a\, G_1\, G_2}{1 - k\, a\, G_1\, G_2} \tag{2.1}$$

where:

$G_1 \triangleq$ gain of T_1 with plate load R_{L1} and cathode load R_K

$G_2 \triangleq$ gain of T_2 with plate load R_{L2} and cathode load R_K

$a \triangleq$ gain of coupling attenuator consisting of R_1, R_2, and C_1 (2.2)

$k \triangleq$ fraction of e_o fedback positively to T_1 through the common cathode R_K.

The loop gain is defined as:

$$G_L \triangleq k\, a\, G_1\, G_2 \tag{2.3}$$

For loop gains less than one, the Schmitt circuit is a linear amplifier in the region where both T_1 and T_2 are conducting. Curve (a) of Fig. 3 illustrates this characteristic.

For a loop gain exactly equal to one, Eq. (2.1) indicates an infinite Schmitt circuit gain. The characteristic is as shown in Fig. 3b.

As the loop gain is increased above one, Eq. (2.1) indicates a negative Schmitt circuit gain. This characteristic is plotted in Fig. 3c. The negative slope region of the characteristic is one of unstable equilibrium. As e_i is increased from zero, the Schmitt remains in the off state until $e_i = E^+$. At this point, transition to the on state takes place. Once the Schmitt is in the on state, however, e_i must be decreased to the value E^- before the Schmitt will reset back to the off state. The difference $(E^+ - E^-)$ is a quantitative measure of hysteresis.

The reason for the hysteresis phenomena is that the grid to cathode potential of T_2 which exists for $e_i = E^+$ depends upon the state of the Schmitt circuit. This can be best seen by examining the circuit waveforms for a particular input waveform.[17]

As Fig. 3 indicates, the amount of hysteresis can be controlled by varying the loop gain G_L. For a G_L of one, the hysteresis is zero. However, a loop gain of one results in a Schmitt circuit which may oscillate or become a linear amplifier with slight drift in the circuit values. Therefore, at least a small amount of hysteresis is generally desired.

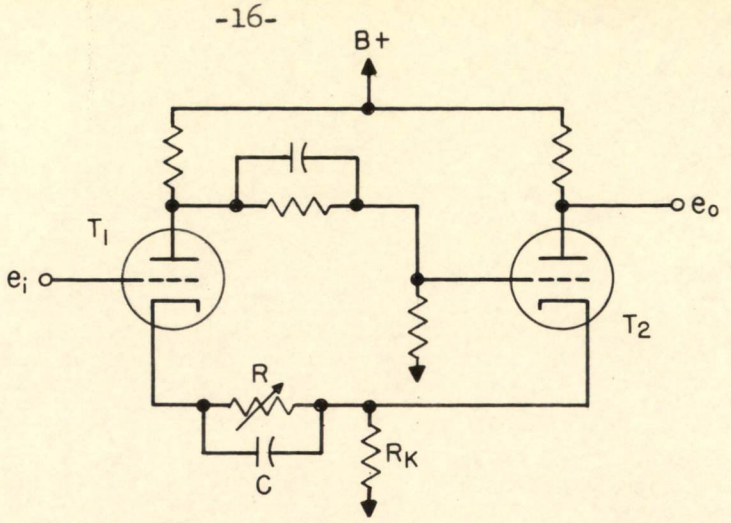
Reduction in hysteresis is generally accomplished by decreasing the factors a or k in G_L. Varying the ratio of R_1 to R_2 will change the value of a. The k value may be reduced by putting a voltage divider in the cathode circuit. A resistor is placed in series with R_k and the cathode of either T_1 or T_2. This resistor is generally by-passed by a small capacitor to decrease the degeneration effect of the voltage divider during the transition between states.

2.2.3 Choice of Circuit Parameters for Optimum Performance

a) The capacitor C_1 is chosen to compensate for C_{in2}, the grid to ground capacitance of T_2. For undistorted signal transmission between the plate of T_1 and the grid of T_2, C_1 should be chosen so that the time constants $R_1 C_1$ and $R_2 C_{in2}$ are equal. However, the time constant determined by C_1 and the resistance of its charging path determines the recovery time of the Schmitt circuit. Recovery time is the time required before the Schmitt will be able to trigger on the next input pulse. As the resistance values must be chosen mainly from other considerations, care must be taken to not make C_1 too large. The minimum length of time between input pulses will determine the maximum value of C_1.

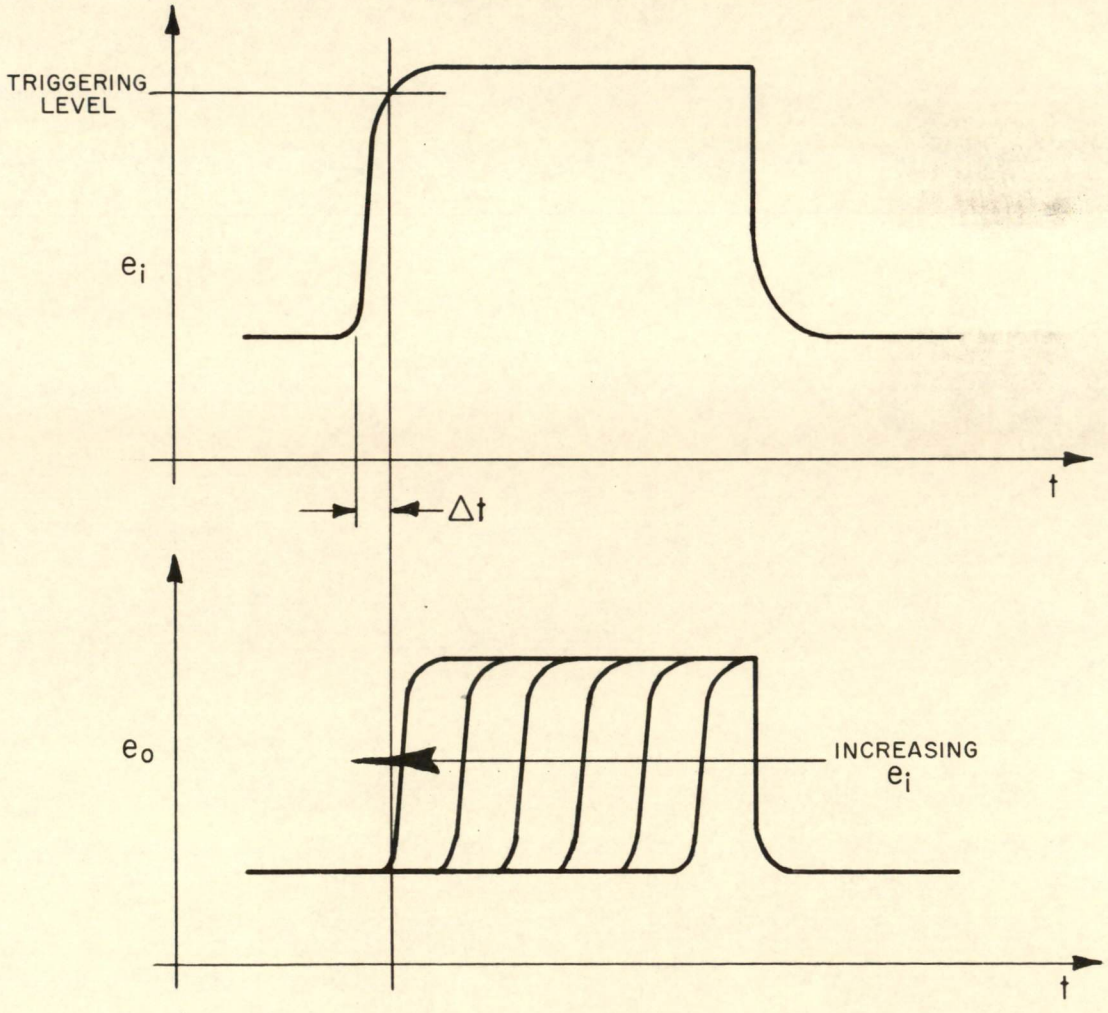
b) A parallel R-C circuit in series with the cathode of T_1 or T_2 and the common cathode resistor R_k has been mentioned as a means of controlling hysteresis. (See Fig. 4). The value of this resistor for a particular value of hysteresis will vary with the tube characteristics and is best found for each Schmitt by trial and error.

The capacitor by-passing this resistor can be chosen to minimize an undesirable phenomena known as "late triggering." It is found that for



(a)

Hysteresis Control



(b)

Late Triggering Phenomena

Fig. 4 Hysteresis and Late Triggering

pulse amplitudes just equal to the triggering level the Schmitt will often not trigger (i.e., begin the transition to the on state) until the end of the input pulse duration. As the input amplitude is increased above the triggering level, the Schmitt triggers with less delay after the initiation of the input pulse. (See Fig. 4b).

Late triggering is due partially to the fact that the input pulse has an exponentially rising leading edge. The Schmitt circuit cannot be expected to trigger until the input amplitude reaches the triggering level. This factor in late triggering (Δt) is dependent upon the input rise time and final amplitude; it can be minimized only by reducing the input rise time. (See Fig. 4b).

However, there is still an interval between the time that the input reaches the triggering level and the time when the Schmitt triggers. This is due to time constants within the Schmitt circuit itself which determine the rate at which conduction in T_1 can increase. Initially T_1 is cut-off and the loop gain is zero. An input above the triggering level will cause T_1 to conduct sufficiently to increase the loop gain to one, which will then cause the Schmitt to trigger. The time required for the loop gain to reach one is dependent upon how much the input amplitude exceeds the triggering level.

By-passing the hysteresis control resistor with a capacitor results in a loop gain which drops rapidly as T_1 begins to conduct and the capacitor begins to charge. The result is that the loop gain tends to increase as T_1 increases conduction but, at the same time, tends to decrease as the by-pass capacitor charges. It is possible to approximately balance

these two effects experimentally. The late triggering is then minimized. If the Schmitt is going to trigger at all during the input pulse duration, it must do so almost immediately after the input reaches the triggering level and before the capacitor can charge sufficiently to stop the triggering action.

c) The values of R_{L1}, R_1 and R_2 should be kept as small as possible to minimize the time constants that determine the time required for the transition between states to take place. The value of R_{L2} is determined by the desired output waveform. Larger values of R_{L2} will result in larger output swing and a greater output rise time. The output rise time has no effect on the Schmitt transition time.

d) There are several reasons for desiring a large cathode resistor R_K. The ability of the Schmitt to accept very large input pulses without drawing grid current is due to the cathode follower action of T_1 which is improved by the use of a larger R_K. Grid current would result in an undesirable shift in the Schmitt bias level. A large value of R_K helps to maintain constant plate voltages independent of tube parameter changes. The effect of a large cathode resistance is often obtained by using a constant current source such as a pentode or a triode with a large resistor in its cathode.[17,19] Besides minimizing the effect of heater voltage variation on the cut-off voltages of T_1 and T_2, the cathode tube allows the use of a technique which compensates for the grid-cathode capacitance of T_1.[17] This compensation technique is used to prevent coupling of small spikes resulting from differentiation of the input pulse through R_K to the Schmitt output.

e) To obtain a stable output voltage swing either the grid or the plate of T_2 should be clamped when T_2 is conducting. The grid may be clamped by driving it slightly positive with respect to the cathode, but this results in a triggering level dependent upon the slope of the input pulse.[17] Since any drift in the clamping action at the grid appears at the output amplified by T_2, it is more desirable to clamp the output plate itself.

Clamping the Schmitt output may be desired for another reason. There is always a small range of input pulse amplitudes which are sufficiently large to cause T_1 to conduct slightly, but too small to bring the gain of T_1 to the point where the loop gain is one. In this range of inputs the Schmitt acts as an amplifier and its output plate rises a small amount. This effect can be eliminated by clamping the plate of T_2 slightly above its normal swing. The appearance of the spikes resulting from coupling of the differentiated input pulse through R_K to the plate of T_2 can also be prevented this way.

Clamping also decreases the output rise and decay time. The output voltage tends to follow an exponential curve in making the transition between its two stable levels. The diodes conduct, however, and limit the transition to the steep slope region of the exponential curve.

f) Decay in the top of the input square pulses must be minimized by choice of a sufficiently large coupling capacitor, C_c. A pulse just above the triggering level would turn the Schmitt back <u>off</u> during the pulse period if the decay were larger than the discriminator's hysteresis.

The grid of T_1 must be clamped to the bias level to prevent a shift in the d.c. voltage across C_c as the input pulse amplitudes vary. This is feasible because the encoder uses only positive-going pulses.

2.3 SCHMITT CIRCUIT DESIGN AND PERFORMANCE

2.3.1 Circuit

The Schmitt discriminator circuit is shown in Fig. 9. The 6AK5 tube was chosen for its low interelectrode capacitances and its relatively sharp cut-off.

The difference in output clamping levels is approximately 25 volts, the analog value of the most significant binary digit. The particular values were picked because they corresponded to standard batteries, and hence did not necessitate use of voltage dividers. The variable resistor on the Schmitt input to the summing amplifier is used to adjust its gain to compensate for the fact that the Schmitt output swing is less than 25 volts.

The capacitive coupling into the discriminator causes a 0.1% decay in the top of the input square wave. For a triggering amplitude of 25 volts, this amounts to only 0.025 volts, which is considerably less than the Schmitt hysteresis. The percent decay is calculated from the relation

$$P \approx \frac{100T}{RC} \ \% \quad (T \ll RC) \tag{2.4}$$

where T is the input pulse duration of 10 microseconds, R the input resistance of approximately 100K, and C the 0.1 microfarad coupling capacitor.

The clamping diode has a forward resistance of 250 ohms with one

volt across it. This reduces the input time constant enough for negative-going overshoots to prevent a significant accumulation of charge on the coupling capacitor.

There are a number of final adjustments which must be made on each individual Schmitt circuit. The variable capacitor C_1 is adjusted to reduce the recovery time sufficiently to enable the Schmitt to follow a one megacycle square wave input. This is necessary, as will be shown later, because the discriminator in every stage after the first must be able to follow inputs containing spikes of duration as long as 0.5 microsecond. No later readjustment of C_1 will normally be needed.

The potentiometer R_a, in the coupling attenuator, is used to control the conduction of the output tube. The output voltage is adjusted to be approximately two volts below the lower clamping level (before the clamping potential is applied) when the output tube is conducting. This adjustment was found to be unnecessary in practice and the potentiometer could be replaced by a 50K fixed resistor.

The R_H potentiometer is used to control the Schmitt hysteresis. If R_H is adjusted to insert too much resistance in the circuit, the Schmitt will turn itself on and off, acting as a free-running oscillator, for inputs just at the triggering level. The resistance R_H is increased until this action is observed and then decreased just sufficiently to prevent the oscillations. Once the correct value of resistance is found for each discriminator, the potentiometer may be replaced with a fixed resistor.

Discrimination bias is controlled with the R_B potentiometer. There is a finite range of input amplitudes for which Schmitt triggering is

uncertain. R_B is adjusted so that a 25 volt square wave input is in the center of this range. In practice the R_B control was found to be over-sensitive. The present potentiometer should be replaced by one of smaller resistance (between two fixed resistors) to decrease the voltage variation per degree of rotation.

2.3.2 Performance

a) The uncertain triggering range varies between Schmitts, with a maximum of 0.1 volt. Over a period of two hours of continuous operation (with no drift in the B^- supply voltage), the center of this range drifted a maximum of 0.1 volt.

The input pulse amplitude at which the Schmitt triggers was found to vary in direct proportion to variations in B^-. This is due to the fact that the discriminator bias is supplied from a voltage divider across B^-. Drift in B^- has a negligible effect on the absolute potential required to trigger the discriminator because the conducting tube is a negative feedback amplifier which tends to keep the Schmitt cathode potential constant.

The uncertainty range was found by measuring the maximum input for which the Schmitt refused to trigger and the minimum for which it always triggered. The discriminators were each driven directly from a square-wave generator to make possible the use of the measuring circuit described later in the discussion on encoder performance.

b) With R_H adjusted as described previously, the hysteresis is 1.4 volts. A 50 kc sine wave input was used for the measurement. Using a dual trace oscilloscope, with its sweep triggered by the sine wave, both input and output waveforms were observed simultaneously in their correct

time relation. The difference in amplitudes of the sine wave at which the Schmitt triggered on and off is the value of hysteresis.

R_H could be adjusted for zero hysteresis, but then the Schmitt oscillated for square wave inputs just large enough to trigger it.

c) The maximum amount of late triggering is less than 0.5 microseconds. This is the interval between the time that the input reaches the triggering level and the time that the Schmitt begins to trigger. As the input was increased above the triggering level, the late triggering rapidly decreased.

Measurements were made by observing Schmitt input and output on a dual trace oscilloscope with its sweep triggered by the discriminator input.

d) Rise time (10-90%) of the discriminator is 0.14 microsecond.

e) Recovery time is less than 0.5 microsecond, as the Schmitt is able to follow a one megacycle square-wave input.

f) Stability of the output swing is dependent upon the plate clamping voltages. These voltages were supplied by batteries whose drift over several hours of encoder operation was negligible.

CHAPTER III

AMPLIFIER

3.1 INTRODUCTION

The encoder stage design requires amplifier circuits to perform two operations: 1) summation and multiplication by minus two, 2) signal inversion.

The first of these operations could be performed by a resistance summing network followed by an amplifier of appropriate gain, or by an operational amplifier with closed-loop gain of minus two.

The difficulty with the resistance summing network is that it attenuates the signals being summed, hence the amplifier following the network would reqire a gain greater than minus two. It will be shown later that feedback in an amplifier stabilizes its gain and increases its bandwidth. Both of these effects become more pronounced as the closed-loop is decreased. Use of an operational amplifier in this application (see Fig. 5) allows a minimum closed-loop gain of minus two.

Signal inversion could be accomplished by following an amplifier of any particular gain with an appropriate voltage divider. For the same reasons cited above, however, it is best to use an amplifier with a closed-loop gain of minus one and dispense with the voltage divider entirely.

Figure 5 shows an amplifier with an open-loop gain of -K used as an operational amplifier.[17] The amplifier output, e_o, is correctly given in terms of the input by Eq. (3.1) as long as the open-loop gain, -K, is sufficiently large.[17]

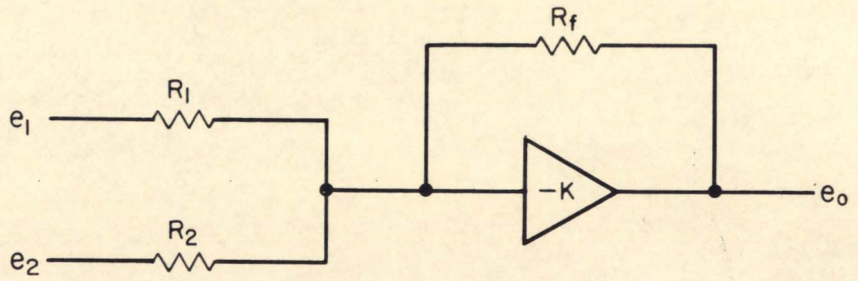


Fig. 5 Operational Amplifier

$$e_o \approx \frac{R_f}{R_1} e_1 + \frac{R_f}{R_2} e_2 \qquad (3.1)$$

In the summation and multiplication by minus two operation, e_1 is the output of the inverter and e_2 is the Schmitt circuit output. Resistance values are chosen such that:

$$R_f = 2R_1 = 2R_2 \qquad (3.2)$$

In the signal inversion operation only one voltage, the stage input, is operated on. In this case, the feedback resistor, R_f, is equal to the input resistor, R_1.

3.2 AMPLIFIER THEORY

3.2.1 Analysis of Gain Stability

A major difficulty encountered in using amplifiers for precision applications is their drift in gain due to variations in plate supplies and in tube and circuit parameters. One of the reasons for using feedback in amplifiers is to minimize the effect of these variations and thereby stabilize the amplifier gain.

This stabilization effect may be examined by referring to Fig. 5 with e_2 and R_2 neglected. The nodal equation at the input grid can be solved for the closed-loop gain, G_{CL}:

$$G_{CL} = \frac{e_o}{e_1} = -\left(\frac{R_f}{R_1}\right) \frac{1}{1 + \frac{1}{K}\left[1 + \frac{R_f}{R_1}\right]} \qquad (3.3)$$

The percent change in closed-loop gain as a function of the percent change in open-loop gain is:

$$\frac{\Delta G_{CL}}{G_{CL}} = \frac{1}{1 + \frac{K}{\left[1 + \frac{R_f}{R_1}\right]}} \left(\frac{\Delta K}{K}\right) \qquad (3.4)$$

The conclusion is that the open-loop gain, -K, should be made as large as possible to minimize closed-loop gain variations resulting from changes in -K.

3.2.2 Desired Open-Loop Gain and Bandwidth

Information is transmitted through the encoder stages in the form of pulse amplitudes. Ideally these would be perfectly square pulses; actually they are pulses with finite rise time and finite decay in their pulse amplitude.

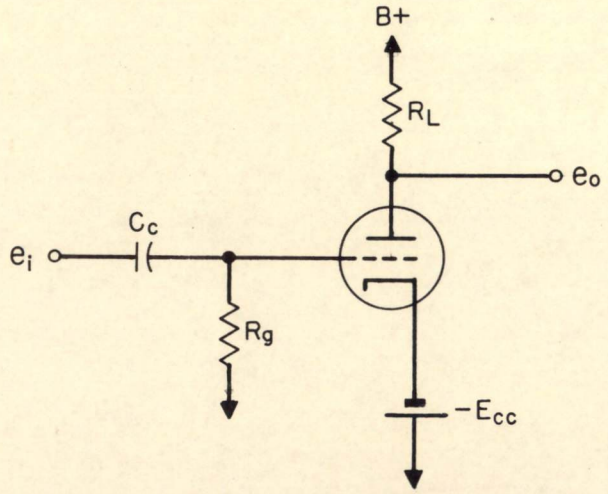
Each stage must be allowed enough time for its input pulse to rise sufficiently close to the discrimination level to trigger its Schmitt circuit. Therefore, the pulse rise times are important in determining the minimum time for completing the encoding operation.

However, during the time that a pulse is presented to a stage, the cumulative decay in the pulse amplitude from previous stages must not be great enough to turn a discriminator previously turned on back off. Therefore, the pulse decay will determine the maximum amount of time allowable to complete the encoding operation.

Both rise time and pulse decay can be related to the amplifier frequency response.[17] The purpose of relating the frequency response is to aid in designing the amplifier and in investigating multiple-stage, closed-loop stability with respect to oscillations.

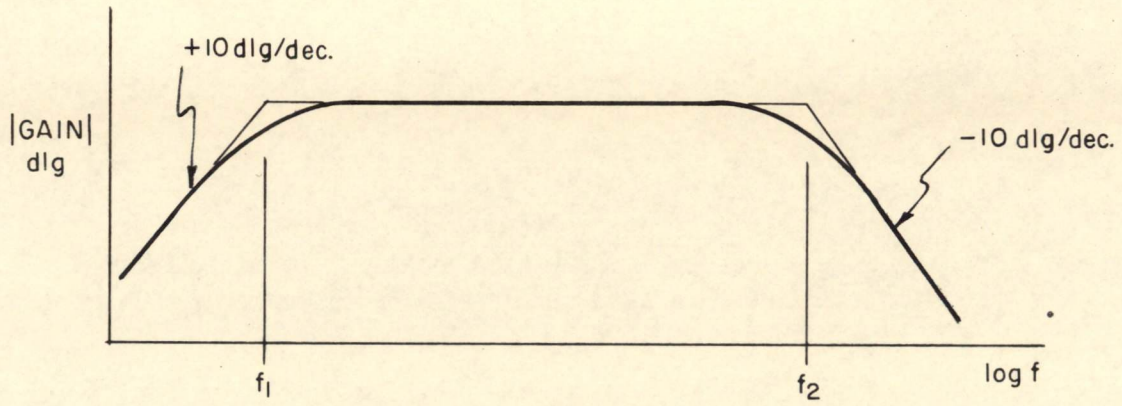
The simple one-stage R-C coupled amplifier of Fig. 6a has the gain magnitude frequency characteristic shown in Fig. 6b.[17,20,21]

The low frequency gain cut off is due to the coupling capacitor C_c. The high frequency cut off is due to tube interelectrode capacitances,



(a)

Amplifier Circuit



(b)

Gain Magnitude vs. Frequency Characteristic

Fig. 6 Simple Single Stage R-C Coupled Amplifier

parasitic capacitance across R_L, and unavoidable wiring capacitance. These capacitances may all be grouped under the term C^1. The low frequency characteristic is that of a high-pass R-C network. Application of a square wave to such a network results in an output with an exponential decay.[17] (See Fig. 7a).

The percent decay in amplitude during the pulse duration T can be shown to be (for $T \gg R_1 C_c$)[17]:

$$P \approx \frac{100\ T}{R_1\ C_c}\ \% \tag{3.5}$$

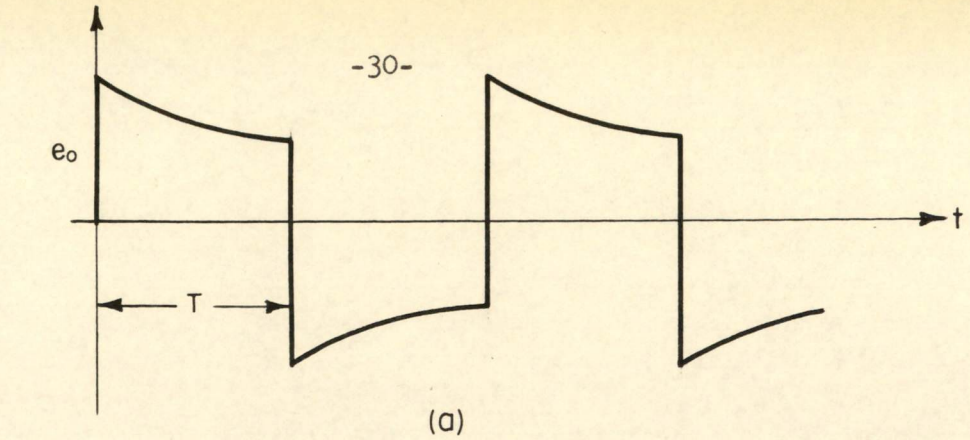
where R_1 is the amplifier input resistance and C_c the coupling capacitance. As R_1 and T will be chosen from other considerations, C_c must be chosen sufficiently large so that the decay will have negligible effect on encoder accuracy.

The high frequency characteristic is that of a low-pass R-C network.[17] The effect of such a network on a square-wave input is to cause the leading and trailing pulse edges to follow exponential curves of time constant $R_L C^1$. (See Fig. 7b).

Rise time, τ_r, is defined as the time required for a pulse to go from 10% to 90% of its final value. Rise time can be shown to be related to the $R_L C^1$ time constant and therefore to the upper break-point frequency, f_2, as shown in Eq. (3.6).[17,21]

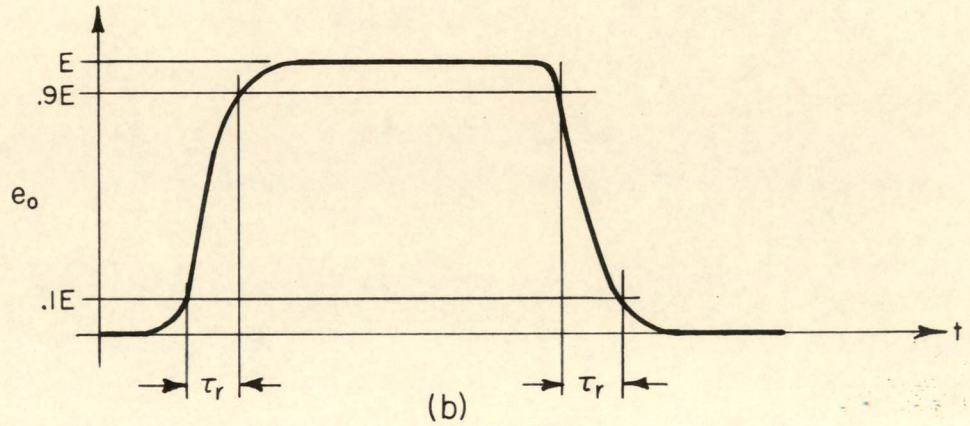
$$\tau_r = 2.2\ R_L C^1 = \frac{2.2}{2\pi f_2} = \frac{0.35}{f_2} \tag{3.6}$$

Equation (3.6) makes it obvious that increasing the upper break-point frequency f_2 will decrease the rise time. Using feedback around the simple amplifier discussed above will have the desirable effect of shifting



(a)

High-Pass Network Response



(b)

Low-Pass Network Response

Fig. 7 Network Response to Square Wave Input

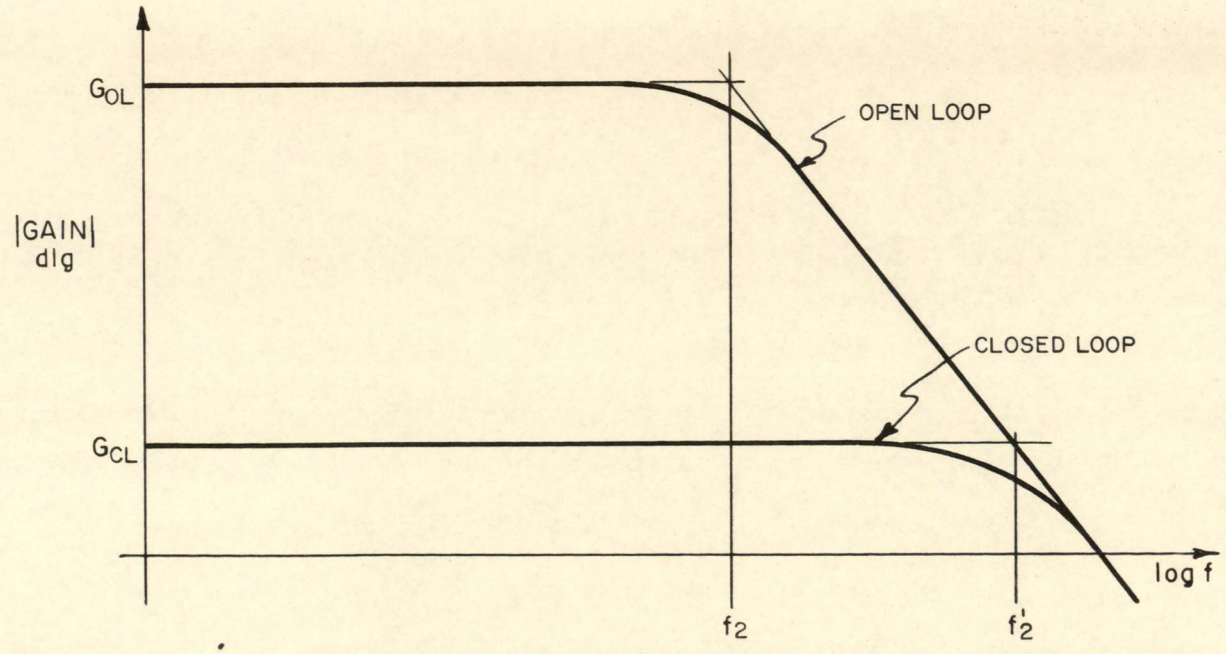


Fig. 8 Open and Closed Loop
Gain Magnitude vs. Frequency Characteristics

this break-point to f_2' as Fig. 8 shows.

The upper break-point frequency may be defined here as the bandwidth. (Bandwidth generally refers to $f_2 - f_1$, but as $f_1 \ll f_2$, the former definition will be used.)

Figure 8 indicates that the increase in bandwidth resulting from using the amplifier in a closed-loop feedback configuration is directly related to the ratio G_{oL}/G_{cL}. The closed-loop gains G_{cL} are fixed by the stage requirements at minus two and at minus one.

The conclusion is that the rise time may be minimized by maximizing both the open-loop gain G_{oL}, and the bandwidth f_2.

3.2.3 Gain-Bandwidth Limitations

Due to the limited g_m or μ and the inherent interelectrode capacitance of a vacuum tube, there is a limit to the obtainable gain-bandwidth product.[17,21] Considering the case of a pentode stage in cascade with an identical stage, the product of mid-band gain and bandwidth may be shown to be[17]:

$$|A_o| \quad f_2 = \frac{g_m}{2\pi (C_o + C_i)} \tag{3.7}$$

where $C_o + C_i$ is the sum of the input and output capacitances of the tube. This product, or its alternate

$$\left|\frac{A_o}{\tau_r}\right| = \frac{g_m}{2.2 (C_o + C_i)} \tag{3.8}$$

may be used as a figure of merit in choosing the optimum vacuum tube. Although this figure of merit, as defined above, indicates triodes to be far superior to pentodes, it must be remembered that the effective value

of $C_o + C_i$ is so increased by the Miller effect as to negate this apparent advantage. In any practical circuit, it will be found that this figure of merit will be reduced by a factor of at least two to three due to unavoidable wiring capacitances.

The conclusion is that the open-loop bandwidth can only be increased by decreasing the open-loop gain. As pointed out above, however, a minimum open-loop gain will be determined by the amount of gain stabilization needed to assure accuracy and dependability in the value of closed-loop gain. The best that can be done with a single-stage amplifier is to choose a tube with the largest figure of merit and to wire the circuit with a minimum of parasitic capacitance.

3.2.4 Multiple Stage Amplifiers

The gain-bandwidth product can be increased over that of the single-stage amplifier by using multiple stages in cascade inside the feedback loop. In this case, the simple bandwidth-rise time relations used before will no longer apply.

The possibility of closed-loop amplifier oscillations must now be considered. Nyquist's stability criterion must be utilized to prevent the design of an amplifier which will oscillate.[20,22]

To obtain a signal to feed back to the input which is 180° out of phase with the input, an odd number of stages will be required. In order to meet the stability criterion, the high-frequency breakpoints of the stages must be staggered.

The lowest upper breakpoint will be that which would have been used in the single-stage amplifier. The breakpoints of the additional

stages must be at higher frequencies. Because of the gain-bandwidth product limitation on the tubes used, the additional stages will therefore have successively lower gains.

The conclusion is that additional stages will improve the rise time but that the amount of additional improvement obtained decreases with the number of stages. At the expense of increased complexity, then, some improvement in performance is possible.

3.3 AMPLIFIER DESIGN AND PERFORMANCE

3.3.1 Amplifier Design

The circuit diagrams of the inverter and summing (multiplication by -2) amplifiers are shown in Fig. 9. Single-stage amplifiers were chosen to minimize the encoder complexity. It was found possible to meet the encoder specifications without going to multiple-stage amplifiers.

The 6CB6 tube was chosen for its high figure of merit and its relatively linear characteristics.[17]

The closed-loop amplifier gain may be calculated from Fig. 9. The result is

$$G_{cL} = -\left(\frac{R_2}{R_1}\right) \frac{1}{1 - \frac{1}{K}\left[1 + \frac{R_2}{R_g} + \frac{R_2}{R_1}\right]} \tag{3.9}$$

where:

$R_1 \triangleq$ resistance between input signal and grid

$R_2 \triangleq$ feedback resistance

$R_g \triangleq$ grid leak resistance

$R_L \triangleq$ plate load resistance (3.10)

$$r_p \triangleq \text{tube plate resistance}$$

$$g_m \triangleq \text{tube transconductance}$$

$$R' \triangleq \frac{r_p R_L}{r_p + R_L} \tag{3.10}$$

$$K \triangleq -g_m R' \frac{R_2}{R_2 + R'} + \frac{R'}{R_2 + R'}$$

For the parameter values used, this may be approximated by

$$G_{cL} \approx \left(-\frac{R_2}{R_1}\right) \frac{1}{1 + \frac{1}{g_m R_L}\left[1 + \frac{R_2}{R_g} + \frac{R_2}{R_1}\right]} \tag{3.11}$$

The mid-band open-loop gain, $g_m R_L$, is approximately 125. Since 5% resistors were used in the circuit, the R_1 resistors were made variable. The R_G potentiometer is used to adjust the overall gain of the inverter and summing amplifier to plus two. This is done with the aid of an oscilloscope with a difference pre-amplifier displaying the difference between one-half of the stage output and the stage input.

The R_s potentiometer is used to adjust the gain of the summing amplifier so that its output is a 50 volt step when the Schmitt changes state. Since the Schmitt output is less than 25 volts, the gain for this amplifier input will actually be greater than two.

The effect of feedback in minimizing variations in closed-loop gain as a result of variations in the tube transconductance may be derived from Fig. 9. The equation relating the fractional changes in closed-loop gain and g_m may be shown to be

$$\frac{\Delta G_{cL}}{G_{cL}} \approx \frac{1}{\left[\frac{g_m R_L}{1 + \frac{R_2}{R_g} + \frac{R_2}{R_1}}\right] + 1} \left(\frac{\Delta g_m}{g_m}\right) \tag{3.12}$$

Using this equation, the effect of a 10% change in g_m is found to be a .17% change in G_{cL} for the inverter and .27% change for the summing amplifier.

The closed-loop amplifier input resistance (at either input terminal in the case of the summing amplifier) can be shown to be

$$R_{IN} \approx R_1 + \frac{R_2 + R'}{g_m R_L} \tag{3.13}$$

For both the inverter and summing amplifier R_{IN} is calculated to be approximately 100K. Using Eq. (3.5), the percent decay in square-wave amplitude due to the capacitive coupling is 0.1% in each amplifier.

3.3.2 Amplifier Performance

a) The inverter rise times (10-90%) vary between 0.1 and 0.15 microsecond. The summing amplifier rise times vary between 0.2 and 0.3 microsecond. It was found that the wiring of the amplifiers, especially of the input and feedback series R-C networks, was very critical in obtaining fast rise times.

b) Linearity was measured using pairs of amplifiers. This procedure was followed because it allowed the use of an oscilloscope with a difference pre-amplifier for accurate direct measurements of the difference between inputs and outputs. Since the encoder also uses the amplifiers in series, this technique is particularly suitable.

The encoder accuracy is specified in terms of percent of the full-scale input. Accordingly, the measure of amplifier linearity of interest is the deviation in output from the ideal output as a percent of full scale (50 volts). Accordingly, the actual input-output characteristic was approximately centered about the ideal characteristic by adjusting the

amplifier gains to their correct value at mid-scale (25 volts). It was found that the percent deviation from linearity

$$D = (100)\,\frac{\text{ideal output - actual output}}{\text{50 volts}}\ \% \qquad (3.14)$$

was a maximum at the full-scale output of 50 volts. The maximum deviation varied in the different pairs of amplifiers tested due to small differences in quiescent operating points and variations in tube characteristics, ranging from 0.5 to 1.6%. By testing different series combinations of amplifiers, it was possible to determine approximately the deviation from linearity of individual amplifiers. The maximum deviation was found to vary from 0.2 to 0.8%.

c) By the same technique used above, the effects of drift in B^- on amplifier gain were measured. The percent change in amplifier gain was found to be approximately 1/25th of the percent drift in B^-. The measurements were taken for changes in B^- as great as 10%.

CHAPTER IV

THE ENCODER STAGE

4.1 CIRCUIT DESIGN

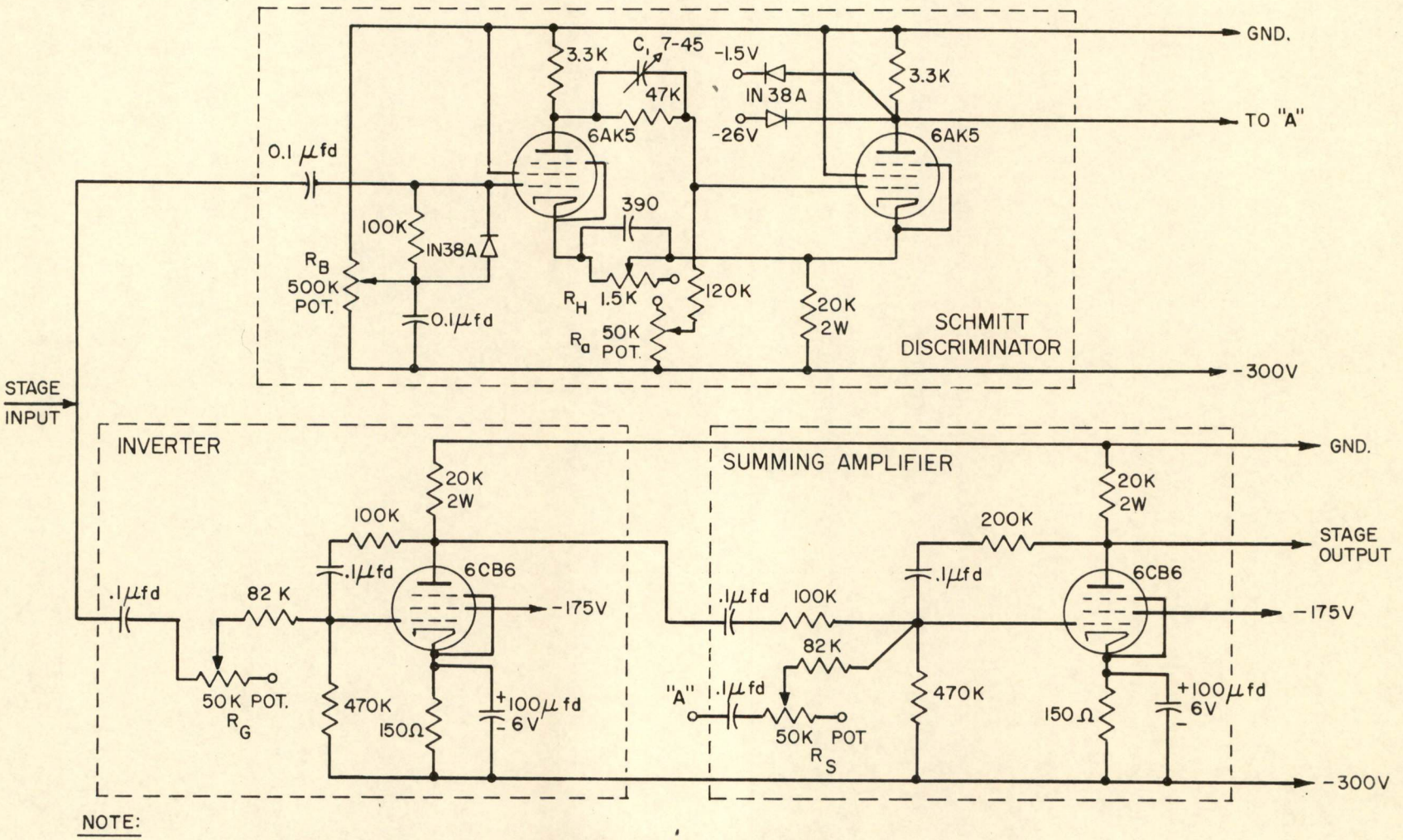
A single encoder stage consisting of a Schmitt discriminator, inverter, and summing amplifier of gain -2, is shown in Fig. 9.

The purpose and method of adjusting each of the potentiometers have been given in the previous two chapters. The sequence followed in adjusting each stage is as follows: The C_1 and R_a adjustments are made for each stage; these do not need any further adjustment in normal operation. The bias of each discriminator is adjusted with R_B for triggering on a 25 volt input square wave. Next the R_G potentiometer is adjusted for a stage gain of plus two. Finally, each stage is supplied with a 25 volt input square wave, causing the Schmitt to trigger, and the R_S potentiometer is adjusted for zero stage output. No readjustment of the R_B, R_G, or R_S potentiometers was found to be necessary in several hours of continuous operation.

4.2 STAGE WAVEFORMS

The oscilloscope photographs in Fig. 10 show typical single-stage outputs (e_o) for square-wave inputs (e_i) of different amplitudes. The voltage scale on the input photographs is 10 volts per division and on the output 20 volts per division. The time scale is two microseconds per division in all photographs.

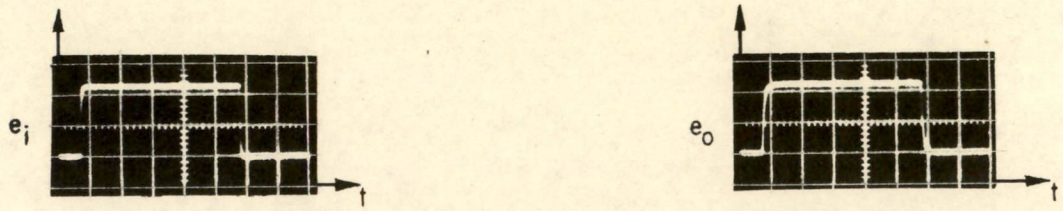
For input square-wave amplitudes of less than 25 volts, the stage performs as a linear amplifier with a gain of two. The stage output is a square wave of twice the input amplitude and a somewhat slower rise time. (See Fig. 10a).



NOTE:

1. ALL RESISTORS 5% 1/2WATT, UNLESS OTHERWISE MARKED
2. ALL CAPACITORS IN μμfd, UNLESS OTHERWISE MARKED
3. 6AK5 FILAMENTS AT GROUND; 6CB6 FILAMENTS AT -300V

Fig. 9 One Stage of Encoder



(a)

Input < 25V

(b)

Input = 25V

(c)

Input > 25V

Fig. 10 Waveforms of Single Stage

For a square-wave input amplitude exactly equal to the 25-volt triggering level, the stage output is zero, except for a 50 volt, 0.5 microsecond spike which appears at the leading edge of the output waveform. This spike is due to the inherent delay in the triggering of the discriminator and the time required for its output to reach its final value. For a 25-volt stage input, the summing amplifier inputs from the inverter and the triggered discriminator effectively balance, producing a zero stage output. However, until the discriminator triggers, the only input to the summing amplifier is the inverter output. Therefore, the stage initially performs as a linear amplifier producing an output of twice the input amplitude until the discriminator triggers and reduces the output to zero. (See Fig. 10b).

For square-wave inputs greater than 25 volts, the stage output initially begins to rise to twice the input amplitude. The discriminator then triggers, reducing the stage output to its final value, namely, twice the difference between the input voltage and the discriminator output. A spike still appears at the leading edge of the output waveform, but its duration and height above the final amplitude decrease as the stage input increases. (See Fig. 10c).

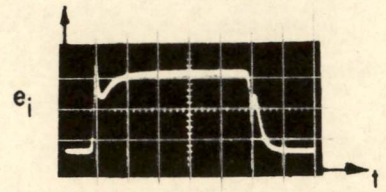
Because of these spikes or overshoots in the stage outputs, the discriminator hysteresis must be minimized. A stage receiving an input from a previous stage of the form of Fig. 10b or Fig. 10c must be able to follow such a waveform. The leading edge overshoot may be great enough to trigger the next discriminator, but if the steady state portion of the waveform is less than 25 volts, the discriminator must turn off again.

A particular stage may receive an input containing spikes contributed by some or all of the preceding stages. The discriminator will

trigger on each input spike, but it must be able to end up in the state determined by the final input amplitude.

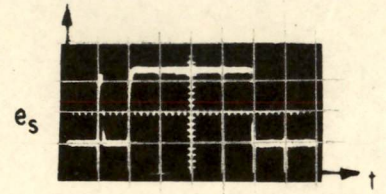
Photographs of a typical set of waveforms at the sixth stage are shown in Fig. 11. The voltage scale is 10 volts per division in (a) and (b), and 20 volts per division in (c). The time scale in each photograph is 2 microseconds per division. In this example, the discriminator turned on and off before reaching its final on state.

The final state attained by the discriminator within the duration of the input square wave is the stage digital output. The on state corresponds to ONE and the off state to ZERO. In the example shown in Fig. 11, the sixth binary digit can be seen to be a ONE for the particular analog encoder input used in taking the photographs.



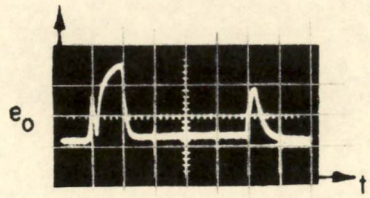
(a)

Stage Input



(b)

Schmitt Output



(c)

Stage Output

Fig. 11 Typical Waveforms at Stage #6

CHAPTER V

ENCODER SYSTEM

5.1 INTRODUCTION

The eight cascaded encoder stages, together with the necessary analog input and digital output circuitry, constitute the encoder system. A block diagram of the system is shown in Fig. 12. The design of digital gates, pulse delays ("D" in Fig. 12), and flip-flops is not covered in this report because these are standard digital computer components. The design of the linear transmission gate is covered in two other reports of this project.[23,24]

Other system configurations may be devised for different encoder applications. The system discussed here is for use with the special-purpose digital computer[1] described in Chapter I.

5.2 SYSTEM OPERATION

5.2.1 Input Read-In

The analog input circuitry enables the encoder stages to be multiplexed between the desired analog input voltages (E_x, E_y, E_z, etc.).

A linear transmission gate is required for sampling each analog input voltage. A flip-flop is used to hold the gate open (conducting) for the 10 microseconds.required for the eight bit analog-to-digital conversion. Each flip-flop is controlled by a pair of pulses (P_x, P_y, P_z, etc.), arriving on its input line. The first pulse puts the flip-flop in the ONE state, opening the linear gate which transmits the chosen analog voltage to the encoder. The second pulse arrives on the same line 10 microseconds later, returns the flip-flop to the ZERO state, closing the gate and cutting

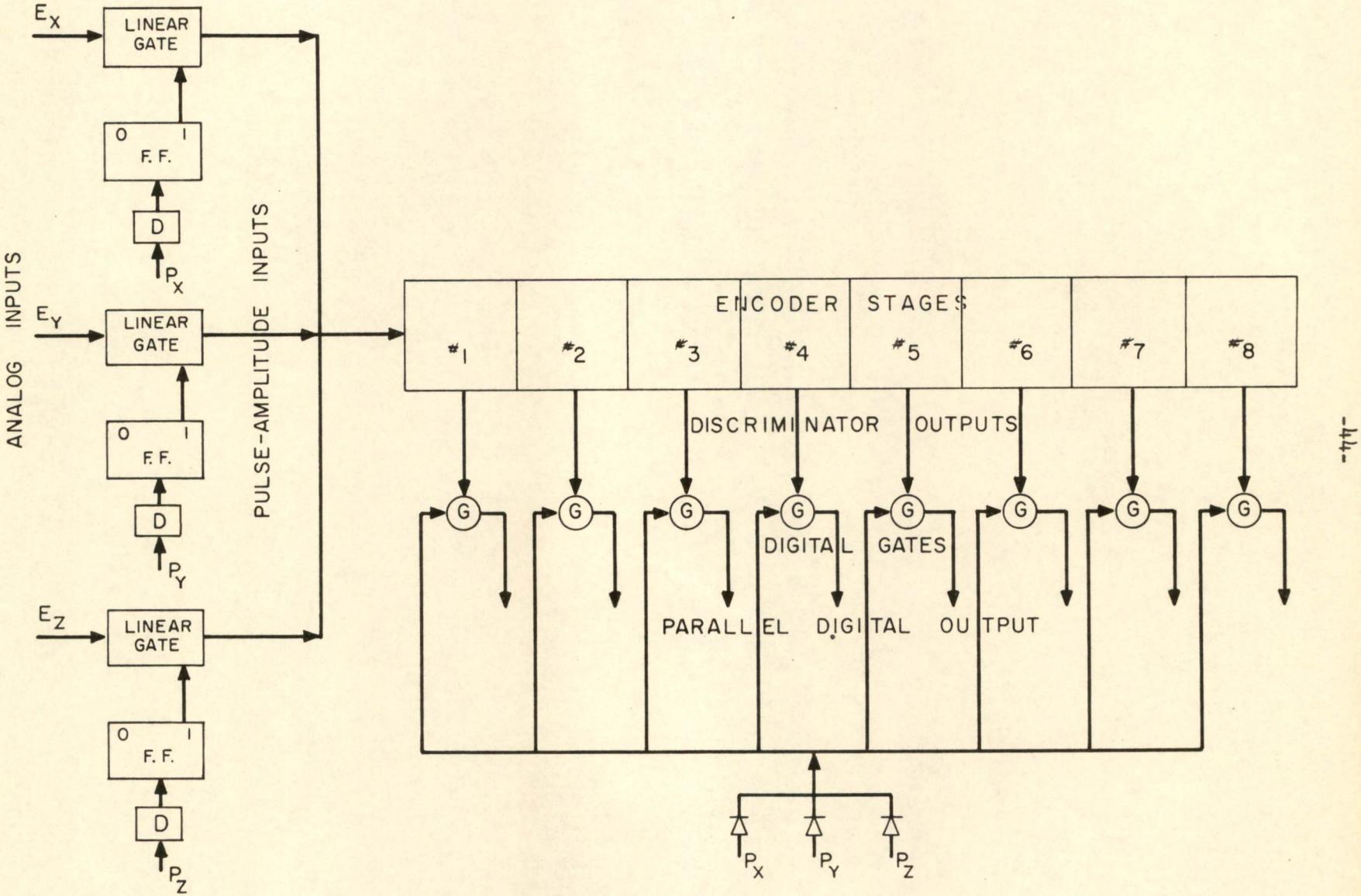


Fig. 12 Encoder System

off the analog voltage to the encoder.

When the encoder is used in conjunction with the special-purpose analog-digital computer, a delay of twenty-two microseconds occurs before another pair of pulses, spaced 10 microseconds apart, arrive on the line corresponding to the next analog voltage to be encoded.

The input analog voltages may range between zero and 50 volts. The encoder input receives a positive-going square wave of 10 microsecond duration whose amplitude represents the analog quantity to be encoded. There is a 22 microsecond interval between input square waves.

Analog voltages in the range of 25 volts can be encoded by adding a fixed bias of 25 volts to each input. The computer can then be programmed to convert the eight bit digital output to seven bits plus sign.

5.2.2 Read-Out

The discriminator output plate of each stage controls a digital gate. In the discriminator off state (signifying a ZERO), the output plate is at -26 volts and the digital gate is closed. In the on state (signifying a ONE), the plate is at -1.5 volts and the gate is open.

The discriminator states in the last two microseconds of the input square wave correspond to the correct digital output. (Section 4.2 explains why the correct discriminator states are not reached sooner.)

The same pair of pulses which control the read-in operation are inputs to the set of digital gates. A diode mixing circuit prevents the pulses on one line from appearing on any other line in the read-in circuitry.

The delay D prevents the digital pulses (P_x, P_y, P_z) from arriving at the flip-flops before arriving at the digital gates. Therefore, the first of the pair of pulses arrives at the gates before the beginning of the

encoding operation. At this time all discriminators are in their normal off state, the digital gates are all closed, and the first pulse is prevented from reaching the encoder digital output.

The second of the pair of pulses arrives at the digital gates before the input linear gate can be closed. At this time, the discriminators are in their final state, corresponding to ONE or ZERO. The gates tied to discriminators which are in the ONE state permit the pulse to pass, while those in the ZERO state do not. As a result, the parallel digital encoder output appears on the digital gate output lines.

After being delayed sufficiently by D for this read-out operation, the second of the pair of pulses complements the input flip-flop which in turn choses the linear gate.

5.3 SPECIFICATIONS ON READ-IN AND READ-OUT COMPONENTS

a) The linear gates must be able to transmit a 0-50 volt signal with a rise time of approximately 0.2 microsecond and a percent deviation from linearity (Eq. 3.14) of less than 0.39% (see Chapter VI). A slower rise time would result in a slower encoding rate. Poorer linearity would reduce the encoder accuracy.

The encoder input resistance of approximately 50K and the number of linear gates must be considered in designing the input circuitry.

b) The input flip-flop plate swing will be determined by the linear gate design. The output rise time must be no more than 0.1 microsecond to be able to open the gate sufficiently fast. The flip-flop must operate on the standard digital pulses supplied by the computer.

c) The delay D must be great enough to allow a pulse to pass through the diode mixing circuit and the digital gates, before the flip-flop

can be turned off.

d) The digital gates must be open with an input of -1.5 volts and closed with an input of -26 volts.

In practice, it may be necessary to isolate the discriminator outputs from the digital gate inputs with cathode followers to prevent slowing up of the encoding operation.

The gates must be able to pass the standard digital pulses supplied by the digital computer.

CHAPTER VI

ENCODER PERFORMANCE

6.1 ENCODER TESTING

6.1.1 Test Procedure

For test purposes, the encoder input was supplied by a Tektronix Type 105 Square-Wave Generator. The generator was used instead of the linear gates called for in the encoder system (see Chapter V), so that the encoder accuracy could be evaluated independently of any non-linear effect in the gates.

The generator has an output range from 6.7 to 100 volts with a rise time of approximately 0.15 microsecond when its cable is connected directly to the encoder input. When the cable is properly terminated, the output range is 1 to 15 volts with a 0.02 microsecond rise time.

The encoder square-wave input amplitudes were measured with the peak-reading circuit shown in Fig. 13.

As there was insufficient time to construct the read-out circuitry, the discriminator outputs were observed directly on an oscilloscope. The encoder input was displayed on one trace of a dual-trace oscilloscope. It was also used to trigger the scope sweep so that the discriminator outputs displayed on the other trace could be observed in the correct time relation to the encoder input.

The procedure followed was to measure the encoder input amplitude and then to examine on the oscilloscope the discriminator outputs of each of the stages. The state of each discriminator output in the last two microseconds of the encoder input pulse corresponds to the digital output of that

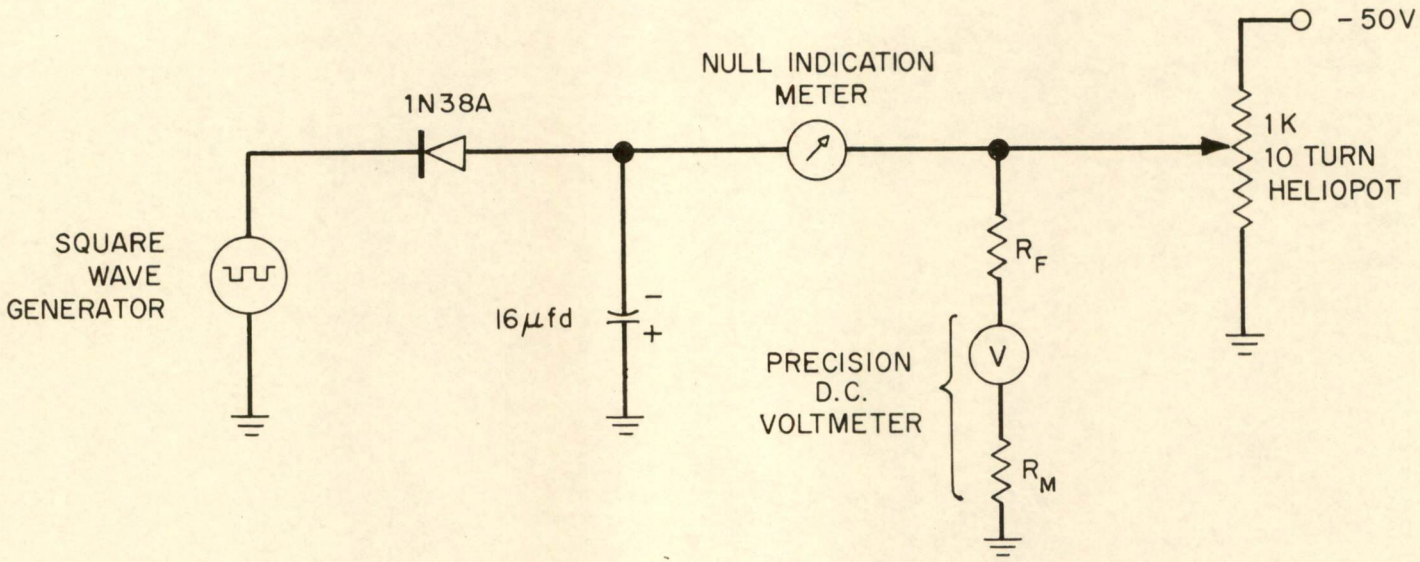


Fig. 13 Square Wave Measuring Circuit

stage. A discriminator output of -1.5 volts indicates a ONE; an output of -26 volts indicates a ZERO.

The square-wave generator was operated at 50 kc. This allowed 10 microseconds for encoding and 10 microseconds between encoding operations. This is a faster encoding rate than required for use with the special-purpose digital computer (10 microseconds for encoding and 22 microseconds between encoding operations).

6.1.2 Measurement of Encoder Input Amplitude

The amplitude of the input square waves was measured with the circuit shown in Fig. 13. The capacitor charges to the peak amplitude of the negative-going generator output through the diode. A time constant of approximately one second (the resistance of the null indication meter is 60K) prevents any appreciable decay in the capacitor voltage between the 50 kc square waves.

The Heliopot is adjusted until the null indication meter needle is zeroed. A Simpson voltmeter was used on the three volt scale for the null meter as this application does not call for high accuracy.

When the Simpson meter indicates zero, the precision d.c. voltmeter is read. The square wave peak amplitude is then

$$E = \frac{R_F + R_M}{R_M} \text{ (d.c. voltmeter reading)} \qquad (6.1)$$

where R_M is the resistance of the meter and R_F a precision resistor in series with the meter. This voltage divider arrangement was used in order to obtain sufficient accuracy from the meter which has only a 15 and 150 volt scale, each accurate to $\pm$ 1/4% of full scale. On the 15 volt scale the meter is therefore accurate to $\pm$ 0.375 volts. It was possible to read the meter to

0.01 volts.

The meter and R_F resistance values were measured with a Wheatstone bridge to four-place accuracy. Using these resistance values the voltage divider factor in Eq. 6.1 was calculated to be 1.996 for the value of R_F used for measuring square-wave amplitudes in the 0-30 volt range. For the value of R_F used for measurements in the 30-45 volt range, the factor was computed to be 2.996.

Square-wave amplitude measurements in the 0-30 volt range are accurate to within $\pm$ .075 volts (1.996 x $\pm$ .0375). Measurements in the 30-45 volt range are accurate to within $\pm$ .113 volts (2.996 x $\pm$ .0375).

6.2 TEST RESULTS

6.2.1 Method of Evaluating Data

The accuracy test data consists of analog input voltage measurements and the corresponding digital outputs. Comparison was accomplished by manually converting the input voltages to eight digit binary numbers.

As previously mentioned, the amplitude measurements are known to be accurate to within $\pm$ 0.075 volts on the 0-30 volt range and within $\pm$ 0.113 volts in the 30-45 volt range. This uncertainty in a particular voltage reading may be referred to as $\pm$ e volts.

For a voltage measurement of E volts, the actual voltage may be anywhere in the E $\pm$ e volt range. Therefore, there is a corresponding uncertainty in the manually computed binary representation of the voltage.

Encoding is a quantization operation, since a continuous range of input voltages are converted into a finite number (256) of digital outputs. Due to quantization, a binary number can be accurate at most to within $\pm$ 1/2

of its least significant digit. This quantization error of $\pm$ q may be expressed in terms of the voltage at the encoder input:

$$q = \frac{1}{2} \frac{\text{full scale input voltage}}{\text{number of quantization levels}} \qquad (6.2)$$

The full-scale input is 50 volts and in encoding to eight binary digits, there are $2^8 = 256$ quantization levels. From Eq.(6.2), q is 0.098 volts. Therefore, each of the possible 256 binary numbers corresponds to a precise analog voltage $\pm$ 0.098 volts.

Since e < q (the uncertainty in voltage measurement is less than the quantization error) in the 0-30 volt range, the calculated digital representation of E + e and E - e can at most differ in the least significant digit. For values of E close enough to the exact analog value of a binary number, the calculated digital representation for all voltages E $\pm$ e will be the same number to eight digits. In this case, the correct digital value of the encoder input is known exactly to eight binary places; otherwise, the encoder input is known accurately to only seven places.

In the 30-45 volt range, e is 0.113 volts. Therefore, e is 0.015 volts larger than q. Since e < 2q, it is possible for both E and either E + e or E - e to have the same eight place binary representation; the other of these voltages' representation will then differ in the least significant digit. In this case, the input voltage is known to only seven binary places. As e is only slightly larger than q, if E, E + e, and E - e have three different eight place binary representations, it is very probable that the one computed from E is correct.

Because of the limited d.c. voltmeter accuracy, the value of e for readings in the 45-50 volt range can at most allow computation of digital

values to six binary places.

The conclusion is that some readings in the 0-30 volt range can be used to establish if the encoder is accurate to eight binary places, while other readings can only prove its accuracy to seven places. Some readings in the 30-45 volt range can be used to determine if the encoder has seven place accuracy, while other readings can only establish six place accuracy and a probability of the existence of eight place accuracy.

6.2.2 Results of Accuracy Tests

Two test runs were taken. Each test was conducted over a period of several hours of continuous operation.

On the first run the digital outputs were accurate to six to eight binary places, with the best accuracy obtained at the low end of the input range. However, the erroneous outputs were all on the high side and consistently repeatable during the several hours test. This indicated a systematic error in the encoder due possibly to faulty adjustment of one or more of the potentiometer settings.

The encoder was then readjusted and the second run taken. This run proved the encoder to be definitely accurate to seven binary places and very probably accurate to eight binary places. (See 6.2.1). In the 0-30 volt range, when E + e and E - e had the same digital value this value agreed with the encoder to eight binary places; when the E + e and E - e digital representations differed in the least significant digit, the encoder output was consistently equal to one of these numbers, usually the smaller. In the 30-45 volt range, the data proved the encoder to be accurate to at least seven binary places.

Due to insufficient time, it was not possible to develop a more

accurate measuring circuit or to take any more runs with the present circuit.

6.2.3 Encoding Rate

All tests were run with a symmetrical 50 kc square-wave input. This proves that the encoder can operate to the established accuracy at a 50 kc encoding rate.

Observation of the discriminator waveforms during the accuracy test runs showed that all discriminators were in their final state in approximately 8 microseconds after the beginning of the input square wave. (See Chapter IV). Operation at the 50 kc rate allowed 10 microseconds for the encoding operation. The extra 2 microseconds should allow sufficient time for the read-out operation. (See Chapter V).

Observation of the waveforms during the test runs also showed that all transients in the system have died out approximately 2 microseconds after the end of the input square wave. Therefore, the encoder should be able to operate with approximately a 2.5 microsecond delay between the input square waves.* With a 10 microsecond square wave duration and a 2.5 microsecond spacing between square waves, the encoder would be operating at an encoding rate of 80 kc. Unfortunately, due to limited symmetry control, it was not possible to operate the square-wave generator with much less than 10 microsecond spacing between the 10 microsecond square waves to test the possibility of 80 kc encoding operation.

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* It may be found that operation with such an unsymmetrical input waveform would necessitate redesign of the clamping circuit at the Schmitt input to prevent excessive accumulation of charge on the coupling capacitor.

CHAPTER VII

CONCLUSIONS AND SUGGESTIONS FOR FURTHER WORK

7.1 IMPROVEMENTS ON THE PRESENT ENCODER

7.1.1 Component Improvements

Tests on the present encoder prove it to be accurate to seven binary places and indicate a possibility of eight place accuracy. The tests were run at 50 kc, but observation of the encoder waveforms indicate a possibility of encoding at 80 kc. (See Chapter VI).

a) These tests were run over a period of several hours of continuous operation. A number of improvements should be made to insure maintenance of the present accuracy over longer periods of operation.

Drift in the B^- supply voltage was found to have a negligible effect on amplifier gain (see 3.3.2c) and on the absolute potential at which the discriminators triggered (see 2.3.2a). However, since the discriminator bias is derived from a voltage divider across the B^- supply, drifts in B^- have a direct effect on the square-wave amplitude at which the discriminator triggers. Therefore, the discriminator bias should be obtained from a separate, stable voltage supply.

The stability of the discriminator clamping voltages directly effects the encoder stage accuracy (see 2.3.2f). These two voltages must also be derived from a very stable supply.

To compensate for any small drift in the discriminator bias and the two clamping levels, all three should be derived from the same supply. If this supply drifts a small amount, the square-wave amplitude which triggers the discriminator and the Schmitt output will then both drift in

the same direction. As a result, the discriminator will tend to continue to supply a square-wave output whose magnitude is equal to the other input to the summing amplifier for stage inputs just equal to triggering level.

Resolution of the control potentiometers were found to be too coarse. As a result, chassis vibration and operating temperature variations affect the control settings. This difficulty may be greatly minimized by replacing each potentiometer by one of smaller resistance in series with a fixed resistor of larger resistance. The use of other types of variable resistors should be investigated.

b) Tests of linearity on the various amplifiers showed some to be more linear than others (see 3.3.2b). This may be due to small differences in quiescent operating points or variations in characteristics between tubes. Each amplifier should be individually adjusted for best linearity. The most linear amplifiers should be used in the first stages.

c) Tests of discrimination ability indicated better performance in some Schmitt circuits than in others. This was found to be largely a function of the particular tubes used. Tubes which result in better performance should be used in the first stages.

7.1.2 Improvement of Encoder Accuracy

To improve encoder accuracy beyond seven or eight binary places, it will be necessary to improve the discriminator accuracy and the amplifier linearity.

a) To improve the amplifier linearity, the analog voltage range (presently 0-50 volts) should be reduced. However, this will necessitate the use of a more accurate discriminator to maintain even the present encoding accuracy.

b) The Schmitt circuit by itself has limited discrimination accuracy.[19] Performance tests showed an uncertainty range in triggering of as much as 0.1 volts and a drift in triggering level of 0.1 volts over several hours of operation (see 2.3.2a). Since the voltage quantization in encoding a 50 volt input range to eight binary places is approximately 0.2 volts (see Eq. 6.2), this is the best encoder accuracy which can be expected using the Schmitt circuit alone.

Improved discrimination ability may be achieved with the Schmitt if it is preceded by another discriminator. Unfortunately, this may increase the time required for encoding.

One technique used is a biased diode discriminator followed by an amplifier in series with the Schmitt circuit input.[19] Input pulses to the diode discriminator above the bias level cause the diode to conduct. The portion of the input pulse above the bias level is amplified and used to trigger the Schmitt discriminator.

Since the volt-ampere characteristic of the diode has a finite curvature at the conduction point, the uncertainty and drift in the Schmitt triggering level still affect the discrimination ability of the circuit. However, their effect at the circuit input are now reduced because the diode non-linearity is amplified by the intermediate amplifier. The sharper the non-linearity of the diode discriminator, the larger the voltage variation in its output for a given input voltage variation. The amplifier gain increases the ratio of diode output variation to diode input variation. As a result, the effective magnitude of the triggering uncertainty range and drift in the Schmitt, referred to the diode discriminator input, is greatly reduced.

Comparison of the volt-ampere characteristics of various diodes with the transfer characteristics of some multi-electrode tubes indicates that a diode connected tube has the sharpest discrimination characteristic.[19,26] A diode discriminator similar to the one described above has been reported to have a long-term drift in discrimination of only 0.05 volt.[19,27]

A difference amplifier can also be used to precede the Schmitt circuit. By greatly amplifying the diffference between the input signal and the reference and using this as the Schmitt input, the discrimination ability of the Schmitt, in terms of the original signal, can be increased. The difficulty with this technique is in accurately obtaining the difference quantity.

Use of the multiar circuit as the voltage discriminator should be investigated. The multiar is an accurate diode-controlled regenerative amplitude comparitor.[17,26] The circuit consists of a diode discriminator in series with the grid of a normally conducting tube. Input pulses that are more negative than the diode reference voltage cause the diode to conduct, lowering the tube grid potential. The resultant decrease in tube conduction is positvely fed back to the diode input through a pulse transformer.

c) For each additional binary place desired, two more cascade amplifiers are required. As a result of the additional amplifiers and increased accuracy requirements, the capacitive coupling time constants must be increased to prevent excessive square-wave amplitude decay.

If the time required for operation by each stage is not reduced, the addition of more stages will increase the total encoding time, also necessitating an increase in the coupling capacitance. One disadvantageous effect of the larger capacitive coupling would be to increase gain for 60 cycle hum in the system.

7.1.3 Improvement of Encoding Rate

The amount of time required for the encoding operation can be reduced if the amplifier and discriminator rise times and the late triggering of the discriminator can be reduced.

A small improvement in rise times may be made by more careful circuit wiring to reduce stray capacitances and by a small amount of inductive peaking. Excessive inductive peaking must be avoided to prevent overshoot in the amplifier response to square-wave inputs. Amplifier rise times could also be improved by the use of a tube with a higher figure of merit (see 3.2.3).

It may be possible to further decrease the discriminator late triggering by additional investigation of the compensating R-C network in the cathode circuit.

One advantage of the cascade encoder is that if less encoding precision is required fewer stages may be used, which decreases the time required for encoding.

As mentioned previously (see 6.2.3), it may be possible, on the present encoder, to reduce the time interval between encoding operations to two microseconds. This was not attempted due to lack of time and an appropriate pulse generator.

7.2 OTHER CASCADE ENCODER DESIGNS

7.2.1 Binary Code

a) A variation of the present encoder design which should be investigated, eliminates an inverter in each stage. This would reduce the number of required amplifiers by half and could possibly result in greater

accuracy and higher encoding speeds.

The summing amplifier and Schmitt discriminator are retained in each stage. However, the Schmitt output to the summing amplifier must now be obtained from the input plate of the Schmitt circuit to obtain the correct polarity swing because the stage input is no longer being inverted.

The stage gain is negative (-2), accordingly the square-wave inputs at successive stages are of opposite polarity. If the encoder input is a positive-going square wave, the discriminators in all odd-numbered stages are biased to be normally in the off state. Discriminators in the even-numbered stages are biased to be normally on.

In order that the digital output ONE is always indicated by a Schmitt plate at zero volts, it is necessary to derive the digital outputs of odd-numbered stages from the Schmitt output plates and the digital outputs of even-numbered stages from the input tube plates.

Operation is similar to that of the present encoder except for the reversal of signal polarities and normal Schmitt states in the successive stages.

The disadvantage of this system is that outputs must be taken from the Schmitt input tube plates. This may seriously affect the time required for transition between states and the stability of discrimination of the Schmitt.[17]

b) The inverter may also be eliminated by replacing the summing amplifier by a difference amplifier. There is no saving in the number of tubes required, however, and the accuracy may not be improved as in (a) because of the common-mode effect in the difference amplifier.[17]

c) Considerable savings in size and number of tubes may be

achieved by using double triodes instead of pentodes. It is possible to use one double triode for the Schmitt circuit and one for both the inverter and summing amplifier.[1] This reduces the number of tubes to two per stage; with 16 tubes, it would then be possible to encode to eight binary places.

However, use of triodes would reduce the encoding rate due to their high effective interelectrode capacitance.

7.2.2 Gray Code[2]

The advantage of designing a cascade encoder to produce a Gray code output is that inputs to successive stages do not depend upon whether the preceding stages are in the ONE or ZERO state. This may allow significantly higher encoding rates because the different stages do not have to wait for the discriminators of preceding stages to settle to their final state as in the binary code encoder. (See Chapters IV and V).

It may be shown that the state transfer characteristic for a Gray code encoder is[2,12]

$$\begin{aligned} V_{n+1} &= A - 2V_n \\ D_n &= 1 \qquad\qquad V_n > 0 \\ V_{n+1} &= A + 2V_n \\ D_n &= 0 \qquad\qquad V_n < 0 \end{aligned} \tag{7.1}$$

where V_n is the input to the nth stage, V_{n+1} the analog output of the nth stage, D_n the digital output of the nth stage, and A the analog value of the most significant digit.

The transfer characteristics may be realized by use of a rectifier circuit. Two experimental five-stage encoders of this type have been constructed and operated satisfactorily, one with an encoding rate of

5 kc.[12,13]

For most encoder applications it will be necessary to convert the parallel Gray code output to binary code form.[2]

7.2.3 Single-Stage Encoder[12,15]

As an alternative to the present encoder, the entire encoding operation may be accomplished with only one encoder stage. The technique is to feed the stage analog output through a delay back to the stage input, and thus use the same stage repeatedly. The binary output will be produced by the single stage in serial form with the most significant digit first.

Several methods for mechanizing the required feedback delay have been suggested.[12,15] One method utilizes two storage capacitors, and a number of linear transmission gates. The encoder input is sampled by a gate, stored on one of the capacitors, and used as the stage input. Another gate samples the stage output and stores it on the second capacitor. The role of the two storage capacitors is then reversed. The second capacitor supplies the stage input through a gate, and the first capacitor samples and stores the new stage output. A timing scheme is used to repeat the above procedure until the desired number of binary digits has been generated.

The linear gates and capacitor storage units required have been designed, and the circuits are discussed in another report.[23]

The advantage of the single-stage encoder is the considerable savings in equipment. However, it is now necessary to introduce a timing circuit. The encoding rate and accuracy may be reduced due to the

capacitor storage units.

7.3 CONCLUSIONS

Experience with the present encoder indicates that the cascade type encoder is suitable for moderate accuracy (eight to ten binary places) and high-speed (50 to 100 kc encoding rate) applications. It has the advantage that accuracy and speed can easily be interchanged to suit a particular requirement by simply varying the number of identical stages.

This type of encoder has the further advantages of requiring only one reference voltage (the discriminators' bias), and no internal timing circuits.

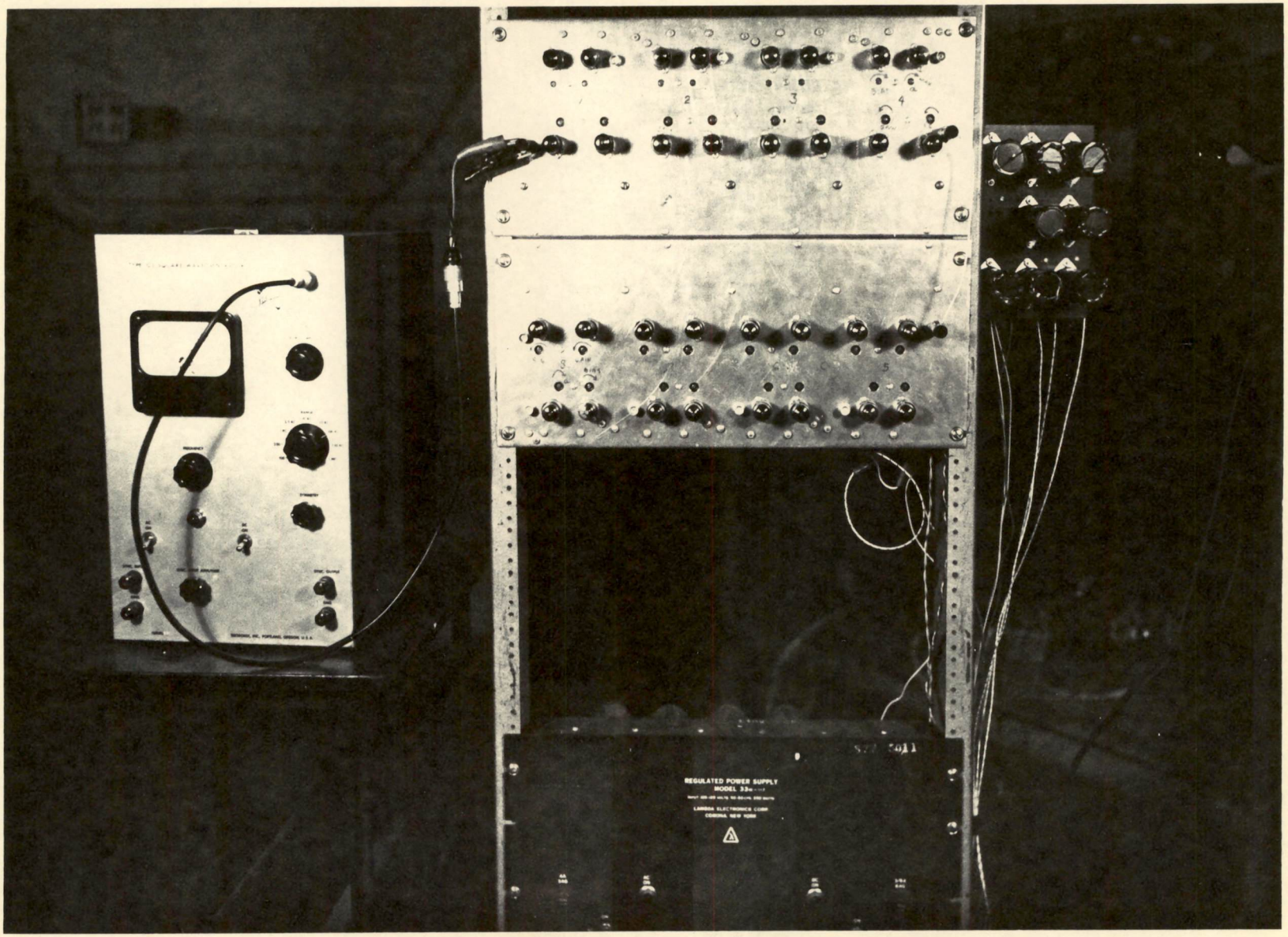

FIG. 14 FRONT VIEW OF ENCODER AND SQUARE WAVE GENERATOR

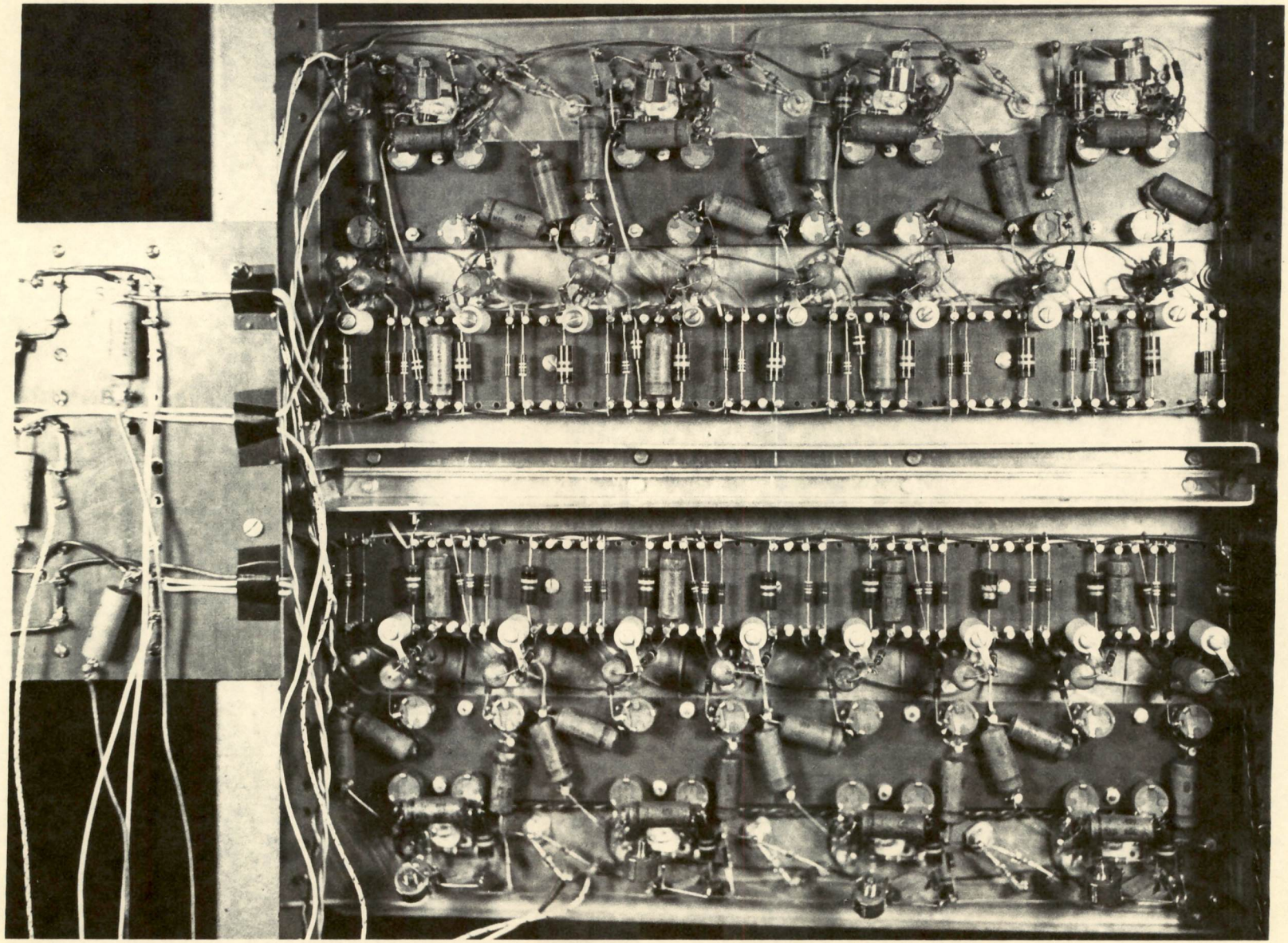

FIG. 15 REAR VIEW OF ENCODER

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