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SURVEY OF MEMORY TECHNIQUES USING TRANSISTORS

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DIGITAL EQUIPMENT CORPORATION

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## ABSTRACT

The ferrite core has made the storage of digital information a practical reality. Previous methods of storage were limited in capacity and reliability and temporarily answered the memory problems. The development of the ferrite core allowed a single bit of information to be stored in a small discreet cell in a manner that seems to be the classical answer to the problem.

Present memories impose close tolerances on the core characteristics which in effect reflects on the ultimate future of the cores. If for a moment we ignore this problem the natural advantages and unique properties of the device appear more promising. Fundamentally the core retains its basic properties even at temperatures of 600 to 800°C. The initial core characteristics are unaffected by time and environment. The core geometry or physical make-up is unique among electronic devices because of its simplicity. It is because of these excellent basic properties that core manufacturers have been able to achieve close tolerances of the core characteristics. The present core-memory design techniques have contributed to the strict tolerances required of cores. It is the purpose of this report to investigate memory design methods that allow a reduction of the core tolerances.



## SURVEY OF MEMORY TECHNIQUES USING TRANSISTORS

By

R. E. McMahon

A memory is peculiar from most electronic devices in that it is expected to be error-free for long periods of time. Memory errors may be listed in the following categories:

1. Errors attributed to poor circuit design.
2. Errors attributed to complete circuit failures.
3. Random errors attributed to temporary tube short and temporary component failures.

If we assume that proper circuit design will eliminate or minimize the first and second cause of errors, then random errors become an important consideration. If the random errors are to be reduced, then completely reliable passive components must be used. The use of transistors as the active circuit elements allows the memory to be a completely solid-state device and intuitively suggests the reduction of random errors.

The transistor and core provide a natural combination. They are both solid-state devices and are compatible in size. The core requires a current drive and the transistor is a natural current source. It is, of course, desirable to keep the impedance that the current source drives as low as possible. This is a condition required by any current source and especially important when transistors are to be used as the current driver. The cores to be driven reflect as the load and the maximum back voltage they reflect on the driver is equal to the product of the number of cores and the output voltage of the cores.

In Fig. 1,  $I_e$  is the current applied to the emitter of the transistor and  $I_c$  is the resulting collector current. The voltage peak  $V_p$  may be calculated as  $n \times \Delta V$  where  $n$  is the number of cores and  $\Delta V$  is the output voltage of the cores. Also  $V_p$  is affected by any wiring inductance  $L_w$ . The applied current width is longer than the switching time of the cores and so the collector voltage falls to a lower value before the current pulse is finished. The voltage level  $V_L$  is simply the product of the current  $I_c$  and  $R$ . The overshoot voltage  $V_o$  is a result of the circuit inductance.



In order to ensure that the current  $I_c$  is accurately maintained, the base voltage  $V_b$  of the transistor must be set greater than  $V_p$ .  $V_p$  is a maximum when all the cores are being switched from one state to another and  $V_b$  must be chosen for this case. During the time the cores are being switched, the collector-to-base voltage difference is a minimum and the power dissipation of the transistor is low. When the collector voltage falls to the voltage level ( $V_L$ ) the power dissipation is maximum. At the time the overshoot  $V_o$  occurs, the transistor current is zero. However, the collector-to-base voltage is at a maximum value. Voltage and power dissipation limits are important in designing the driver stage and the current required is an additional consideration.

In designing a memory, speed and capacity dominate the ultimate limits that can be achieved. The speed limitation is influenced in part by the ferrite cores. The fastest presently-available core is the so-called  $S_1$  core. The  $S_1$  core characteristics may be listed as follows:

1. Total switching current required, 820 ma.
2. Current rise time, 0.5 to 0.7  $\mu s$ .
3. Current width (flat top portion),  $> 1 \mu s$ .
4. Core output voltage  $\approx 100$  mv.
5. Core switching time  $\tau_s$ , 1  $\mu s$ .

At this point it is necessary to investigate transistor characteristics relative to the above requirements. Most switching transistors of the alloy type are capable of handling large currents without a serious reduction of current gain. Output pulse currents in the order of 400 ma (a half current for the  $S_1$  core) require less than 15 ma of input current to the transistor. The current rise time is dependent on the frequency response of the transistor and a 4-Mc response is necessary to supply the required 0.5 to 0.7  $\mu s$  current rise time for the  $S_1$  core. The current and rise time requirements can be met rather easily with present transistors.

In order to provide large memory capacity, the driving transistor must be capable of withstanding the back voltage reflected by the cores. A rather serious conflict occurs at this point. The maximum voltage capabilities of a transistor are inversely proportional to maximum frequency response attainable. It has been noted that a 4-Mc transistor is needed for the



$S_1$  core drive and the transistor physical relationships show that the maximum voltage possible is about 50 volts. Referring to Fig. 1, it has been found experimentally that wiring inductance averages 0.006  $\mu$ h per core in most conventionally wired arrays. This inductance affects the back voltage  $V_p$  and also accounts for most of the overshoot voltage  $V_o$ . The back voltage may be expressed as:

$$V_p = n_s \Delta V + n_t L \frac{di}{dt}$$

where  $n_s$  = number of cores switched  
 $n_t$  = number of cores threaded  
 $\Delta V$  = core output voltage  
 $\frac{di}{dt}$  = drive current rise time  
 $L$  = wiring inductance

If the transistor maximum voltage is 50 volts, we can divide this between back voltage and overshoot in an appropriate manner. The overshoot voltage is:

$$V_o = n_t L \frac{di}{dt}$$

where  $\frac{di}{dt}$  = drive current fall time. If we assume the current rise and fall times are equal, then  $n_s$  may be found from,

$$V_p + V_o = 50V$$

$$n_s \Delta V + n_t L \frac{di}{dt} + n_t L \frac{di}{dt} = 50V$$

The memory type determines the  $di/dt$  term. If the memory is a coincident-current type, then  $di$  equals 400 ma, for  $S_1$  cores and if the memory is a linear-selection type,  $di$  equals 800 ma and  $n_s = n_t$ . In a coincident-current memory the  $n_t L (di/dt)$  term becomes the predominant factor since the ratio of threaded cores to switched cores is usually very large. For example, a stack of 60 planes each having 64 x 64 cores results in the following read-driver, back-voltage components.

$$\begin{aligned} V_p + V_o &= n_s \Delta V + n_t L \frac{di}{dt} + n_t L \frac{di}{dt} \\ &= 6 + 20 + 20 \\ &= 46V \end{aligned}$$

Fig. 2 indicates the component parts of the back voltage and overshoot. The base voltage would normally be set at +28 volts to avoid saturation and hence current loss to the cores. The total collector-to-base voltage during the



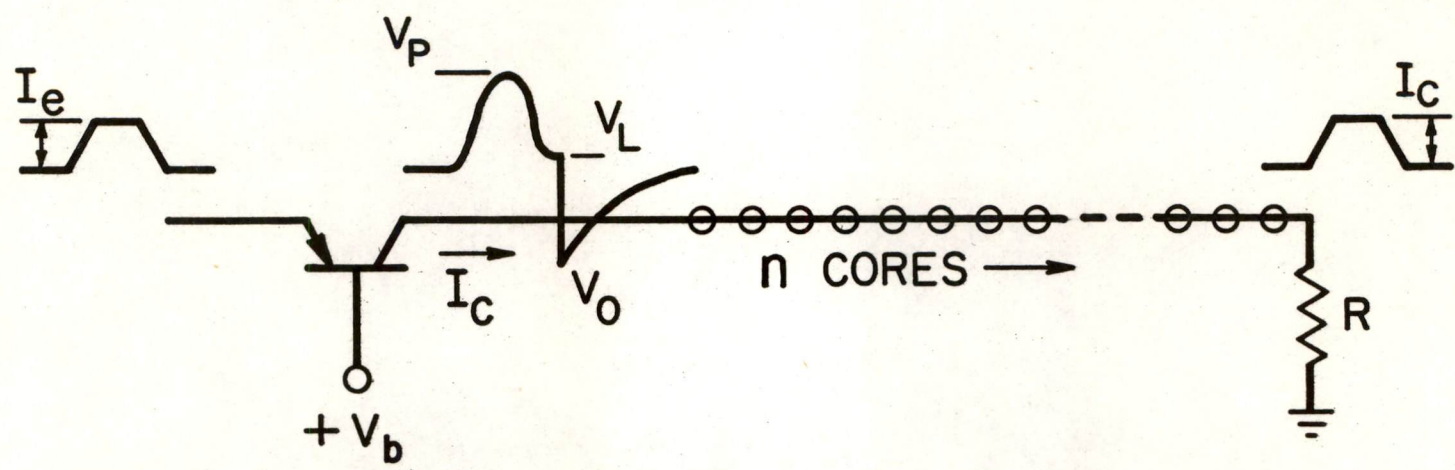


FIG. 1.

LINEAR-SELECTION DRIVER AND DRIVE LINE

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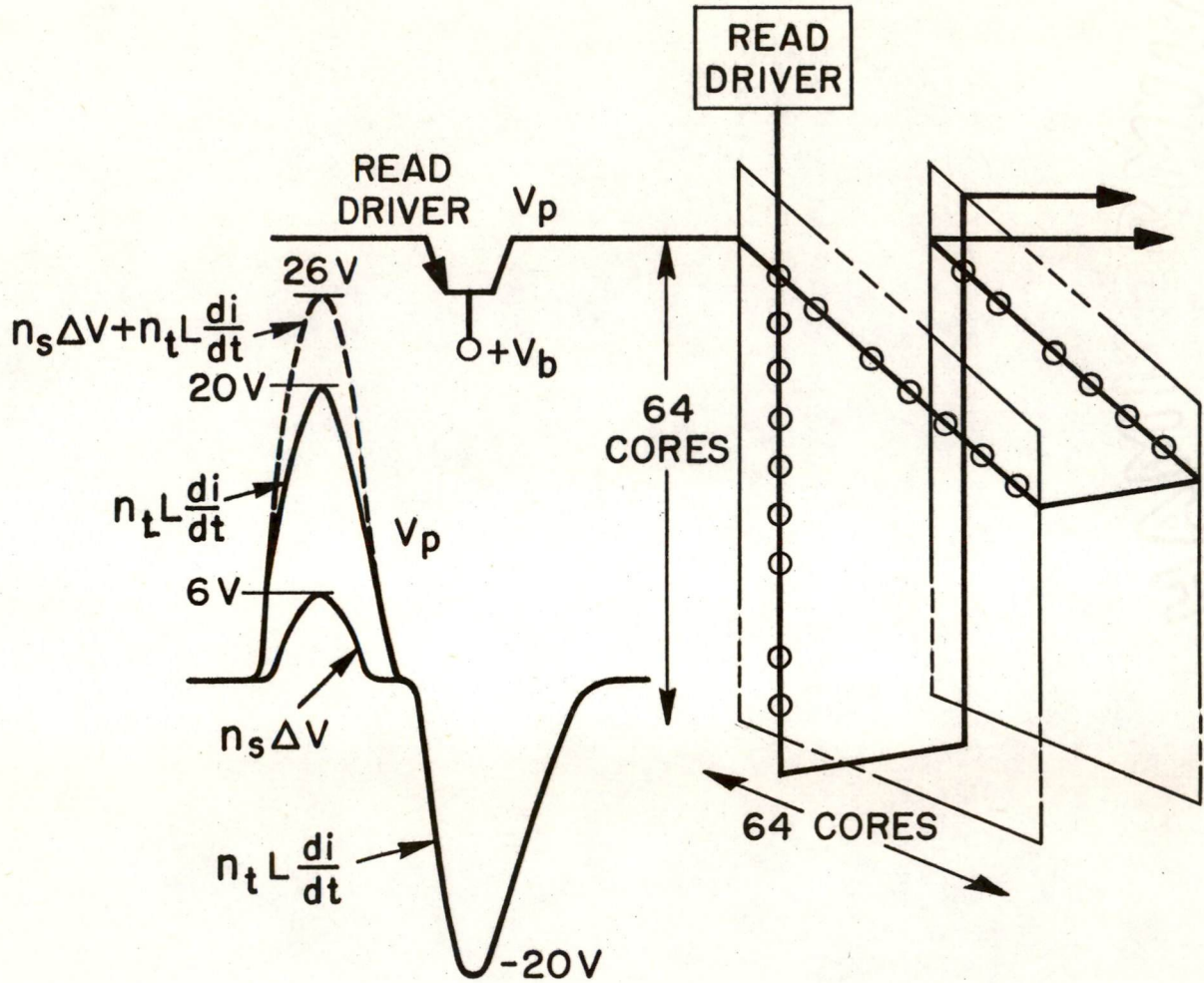


FIG. 2

COINCIDENT-CURRENT DRIVER BACK VOLTAGE COMPONENTS

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overshoot period is 48 volts. This is very close to the maximum tolerable voltage of the transistor. If a measure of efficiency were based on the ratio of back voltage due to switched cores and the back voltage due to inductance, the coincident-current memory would not appear to be very efficient.

Another type of memory system referred to generally as linear selection<sup>†</sup> or end fire drive will be described and compared with the coincident-current system. As the term end fire drive implies the memory has a drive wire for each word. When a word is selected a single drive line must supply a full current. There are no read half-selected cores in this memory system. The fact that each drive wire threads only selected cores allows longer word length to be driven without an increase in driver-back voltage.

For a linear-selection type memory, the back voltage components are calculated for a memory 400 cores in length.

$$\begin{aligned} V_p + V_o &= n_t \Delta V + n_s L \frac{di}{dt} + n_s L \frac{di}{dt} \\ &= 40 + 4 + 4 \\ &= 48V \end{aligned}$$

<sup>†</sup>1. Olsen, K., "A Linear-Selection Memory Using An Anticoincident-Current Switch", May 8, 1953, 6M-2110.

2. Raffel, J., "A Large Planar Switch For Register Selection In A Magnetic-Core Memory Thesis Proposal", August 31, 1953, 6M-2384.

3. Rawson, E., "Linear-Selection Memory", March 1955, M24-47.

4. Whitney, G. E., Linear Selection, IBM Report IM-5.

5. Best, R., Linear-Selection Memory, Western Joint Computer Conference proceeding.

6. McNamara, F. L., Group 24 Quarterly Progress Report, October 1956.

7. Rachman, J., "Ferrite Apertured Plate For Random-Access Memory", IRE, March 1957.



Fig. 3 shows the back voltage and overshoot. The selected cores produce a back voltage of 40 volts and the inductance associated with the threaded cores (which are selected cores) is only 4 volts. If the same rule for efficiency is applied here, it is obvious that this memory system is considerably more efficient than the coincident-current method. What then is the disadvantage of the linear-selection method? In Fig. 2, for the  $64 \times 64 \times 60$  planes, it would require 128 drivers of the type shown to complete the memory read-drive arrangement. The coincidence of an x- and y-driver current switches a single core in each plane. Each driver current need be only half that required to switch the core. In Fig. 3, if the same number of words is taken so that 4096 cores are required, the word length (or number of cores switched) may be much greater for the linear-selection method relative to the coincident-current method with no additional back voltage burden on the driver. However, 4096 read drivers are required and each driver must supply full current. By using a 2:1 transformer to step up the current, the linear-selection driver current may be reduced to a half current. This, of course, means that the back voltage reflected from the cores is doubled, and a maximum of 400 cores can no longer be driven. However, 200 cores can be driven and this still represents a word length advantage over the coincident-current memory.

There are techniques to reduce the number of drivers in both the linear-selection and coincident-current memories and these will be investigated. Fig 4 shows a coincident-current arrangement with 64 read drivers on each axis. Fig. 5 shows two drivers on each axis and 32 switches on each side for the same  $64 \times 64$  plane.

If switch  $x_1$  and  $y_1$  are closed and driver  $x_A$  and  $y_A$  are turned on, then core line  $x_1$  and  $y_1$  receives a current and the core common to both lines receives a full current. By selecting particular combinations of switches and drivers, any core may be selected. The drivers and switches can be minimized further to reduce the system. The chart shown as Table I indicates the various arrangements. It must be noted here that the switches will have a small but finite resistance when in the on condition. This resistance will increase the back voltage and hence reduce the maximum number of cores that can be driven.



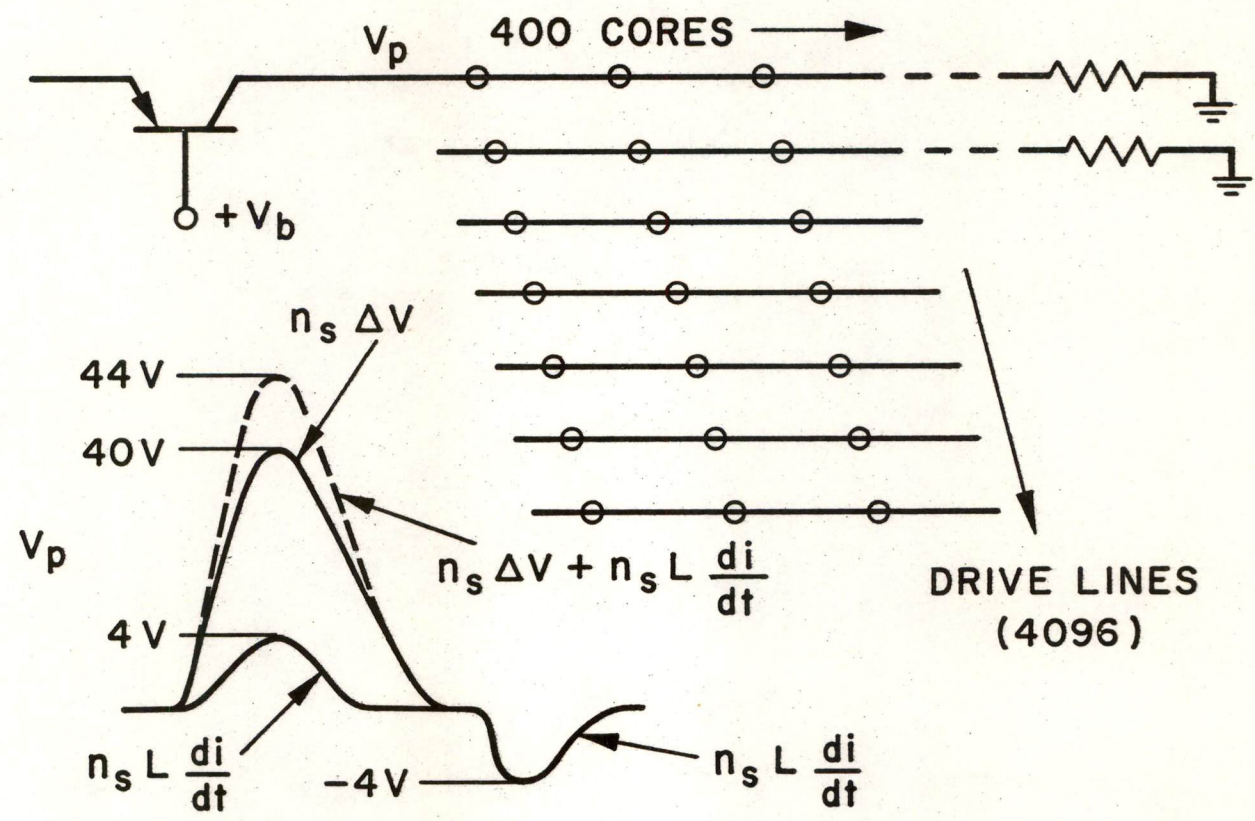


FIG. 3

LINEAR-SELECTION DRIVER BACK VOLTAGE COMPONENTS

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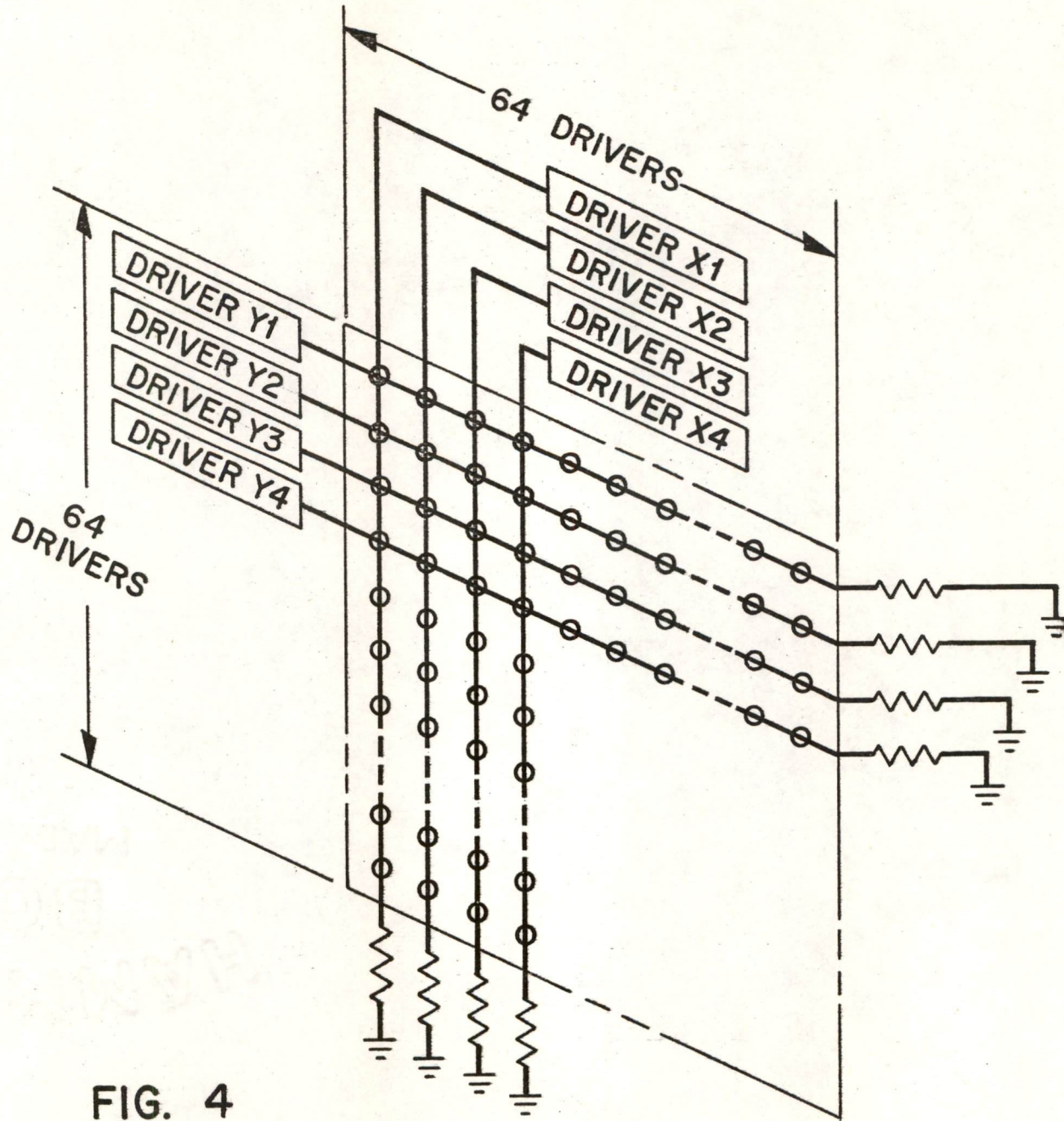


FIG. 4

COINCIDENT-CURRENT MEMORY USING ALL DRIVERS

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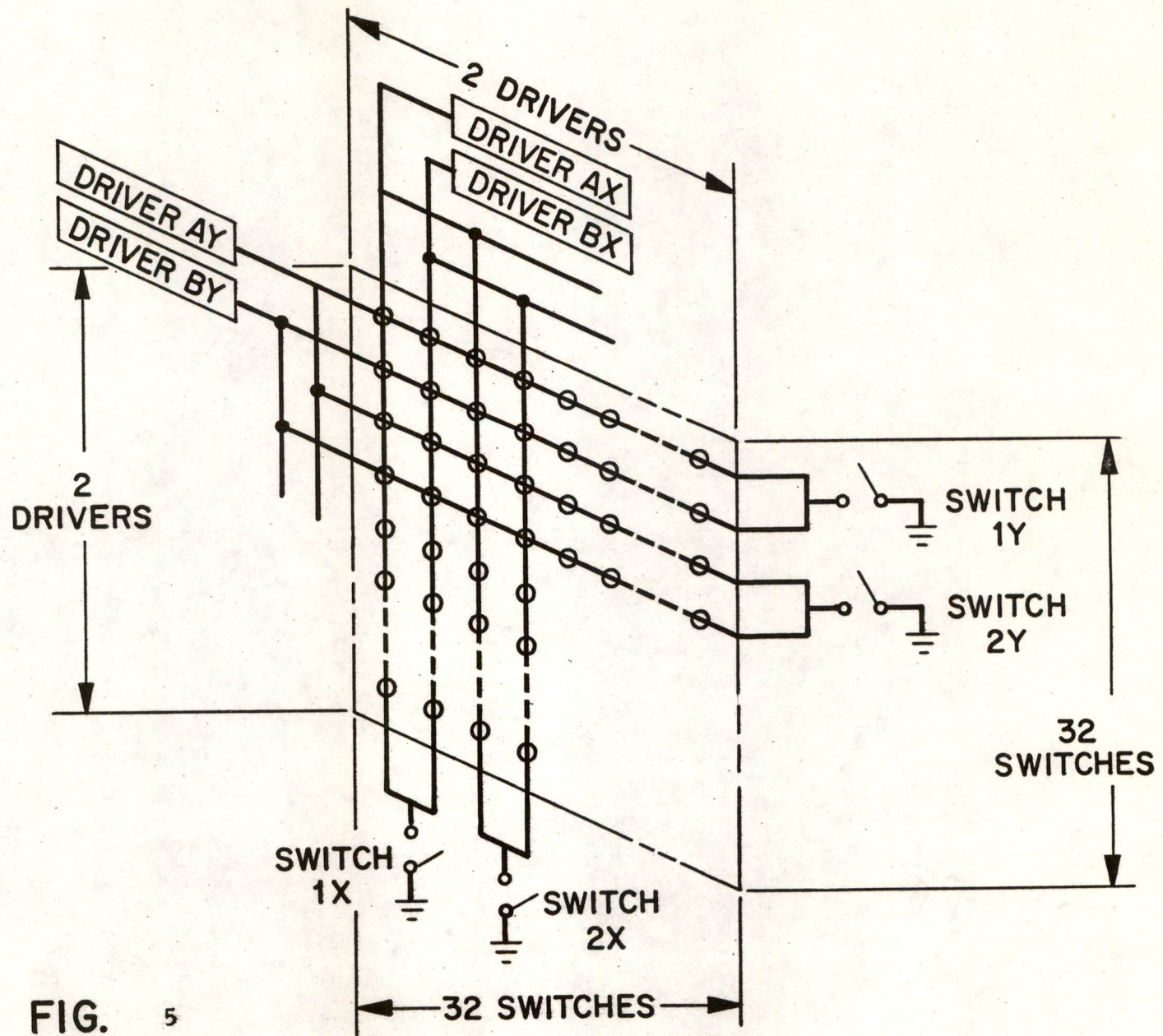


FIG. 5

COINCIDENT-CURRENT MEMORY WITH DRIVERS AND SWITCHES

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	<u>No. of x or y Drivers</u>	<u>No. of x or y Switches</u>
1.	64	0
2.	32	2
3.	16	4
4.	8	8
5.	4	16
6.	2	32

Fig. 4 is case 1 while Fig. 5 is case 6. Since the switches must be able to accept the current supplied by the drivers, they will in general be equal in complexity to the drivers. On this basis, case 4 with 8 drivers and 8 switches gives a minimum design.

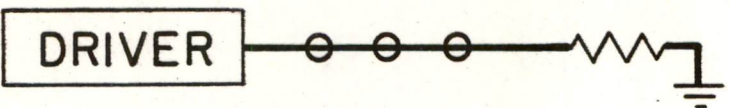
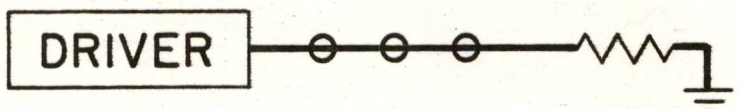
Fig. 6a shows a section of a linear-selection memory having the same number of words (64 x 64) as the previous coincident-current memory example. There is a driver for each word or 4096 drivers. Fig. 6b shows an arrangement of two switches and 2048 drivers.

Table II shows the possible switch and driver arrangements.

	<u>No. of Drivers</u>	<u>No. of Switches</u>
1.	4096	0
2.	2048	2
3.	1024	4
4.	512	8
5.	256	16
6.	128	32
7.	64	64
8.	32	128
9.	16	256
10.	8	512
11.	4	1024
12.	2	2048

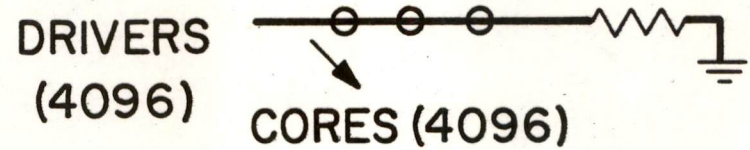
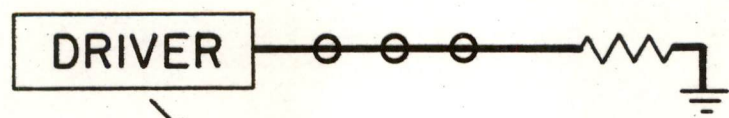
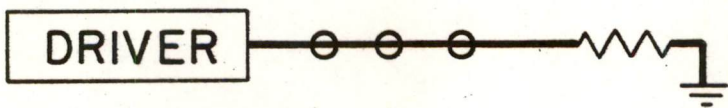
The switches in the linear-selection memory have to accept the full current and not half currents as in the coincident-current memory. However, it is generally advantageous to use transformer coupling from the driver to the

op. 2



LINEAR-SELECTION DRIVER ARRANGEMENT USING ALL DRIVERS

6a.

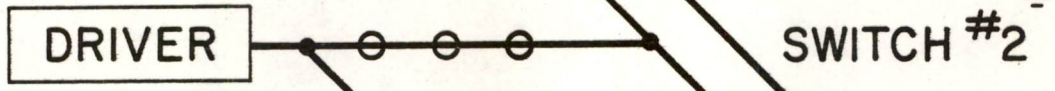


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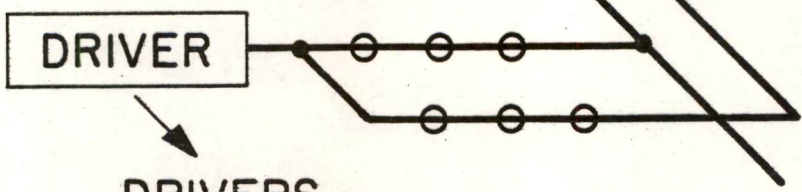
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LINEAR-SELECTION USING DRIVER AND SWITCHES



6b.



DRIVERS (2048)

FIG. 6.



core line in both memory types. This allows the switch to be placed in the transformer primary as shown in Fig. 7. We have reduced the current required of the driver in the linear-selection memory by using a 2:1 transformer. This makes the linear-selection driver requirements equal to the coincident-current driver requirements. Both drivers are required to supply a half current. Since the switch is in the transformer primary for both methods, the switch must accept only a half current. The drivers and switches will be comparable then in complexity in the linear-selection memory and so 64 drivers and 64 switches (case 7) would be a minimum system.

In comparing both memory types, the linear-selection memory requires about four times as many drivers and switches. The logic circuitry needed to operate the switches and drivers will not necessarily be four times more complex since there are minimization techniques in this area also. There are several advantages in linear selection that perhaps compensate for the size problem. The selected core in each digit in the coincident-current memory receives a full current and other cores common to the selected x- and y-drive lines receive half currents. These half currents produce a small amount of noise in each of these half-selected cores. In a large memory, the noise from these cores can be additive and large enough in some cases to reduce the signal-to-noise ratio to zero. The noise is generally of such a nature that it occurs before the peak output of the selected core. A strobing technique is used to sample the signal after the noise has subsided. In the linear-selection system there are no half-selected cores so that noise is at an absolute minimum.

The core peaking times must be controlled very closely by the manufacturer at present since the strobing technique used in coincident-current memories will not tolerate variations on the core peaking time. The linear-selection memory does not require a strict control of peaking time.

Very accurate control of the drive current in the coincident-current memory must be maintained since any unbalance may cause half-selected core noise to increase or, at worst, may switch half-selected cores. The linear-selection memory will tolerate large current changes because there are no half-selected cores. The low noise and current margins of the linear-selection memory outweighs the size advantage of the coincident-current

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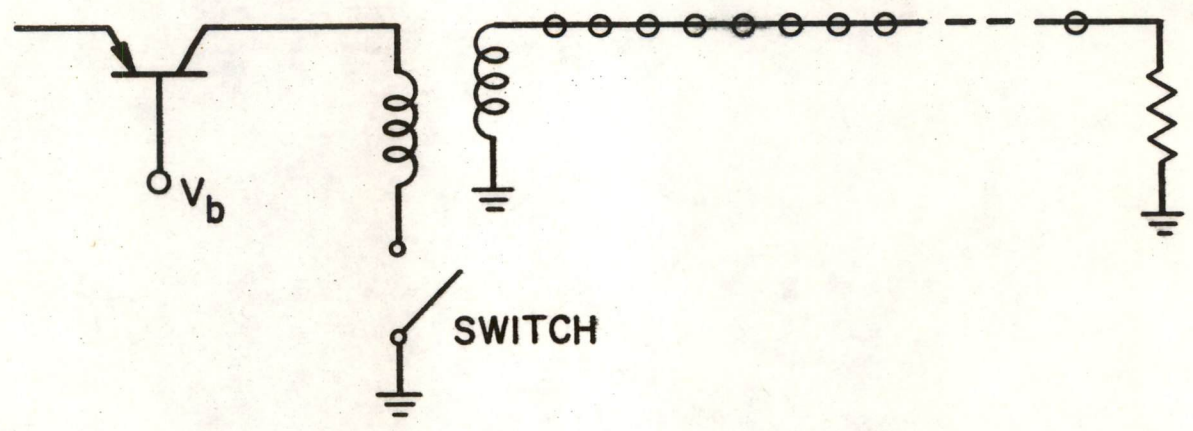


FIG. 7

DRIVER TRANSISTOR AND PRIMARY SWITCH



memory for small memories. Where the line is drawn depends to a large degree on other conditions. Table III lists the various characteristics of each memory type.

Table III

	<u>Coincident Current</u>	<u>Linear Selection</u>
Driver and switch size	Small	Large
Noise	Inherently large	Inherently small
Sense amplifier	Complex	Small
Core wiring	Complex	Simple
Relative memory word length	Small	Large
Memory words	Large	Small
Core characteristics	Close tolerances	Large tolerances

A coincident-current memory has been built containing 4096 words 28 bits long. The memory has a cycle time of less than 6  $\mu$ s. The complete use of transistors in the memory has not sacrificed speed or versatility and has provided at the same time complete reliability and minimum error rate. The memory uses 32 switches for each of the x and y axes and two sets of x and y drivers. Each set of drivers has a read driver and write driver. The current rise time is 0.6  $\mu$ s and although the driver is capable of faster rise time, this is an optimum rise time. It has been found that the memory has unexpectedly good margins. The transistor current drivers have provided currents that are more nearly suited for core driving than any existing tube drivers and this is partially responsible for the excellent margins.

The memory timing is shown in Fig. 8.

If speed is a primary consideration, it can be seen from the timing diagram that the coincident-current memory has several inherent delays. The core cannot be overdriven to reduce its peaking time ( $\delta_1$ ) because of the current limitation of the half-selected cores. The strobe time delay ( $\delta_2$ ) cannot be reduced because of the half-select noise that occurs earlier. These two delays total about 1.6  $\mu$ s and represent a rather large percentage of the total cycle time. In this respect, a linear-selection memory has speed capabilities greater than the coincident-current memory.

A small linear-selection memory has also been built to establish its operational characteristics and also to obtain a practical size relationship

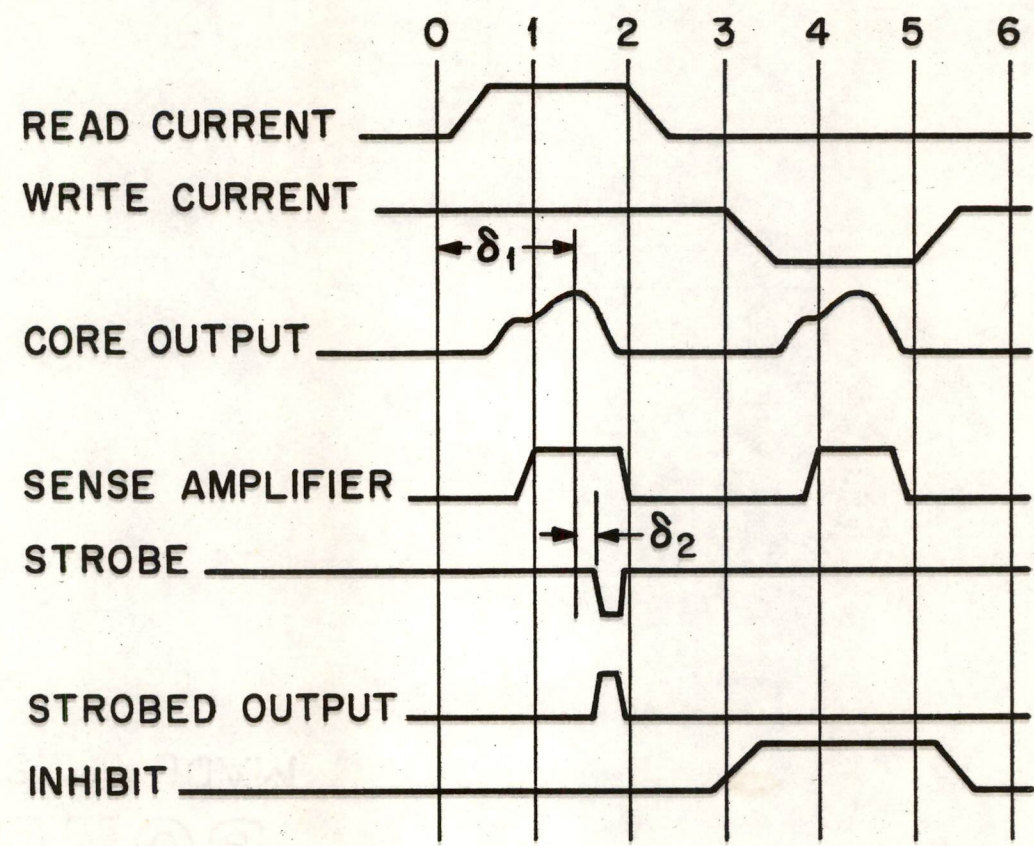


FIG. 8 MEMORY TIMING DIAGRAM

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between linear selection and coincident current. At present, the results indicate that the linear-selection drivers, switches and sense amplifiers are three or four times smaller than the same coincident-current circuits. As noted before, the current regulation and wave-shape requirements may be relaxed for linear selection and hence the circuitry may be simpler. In addition, the low noise that is characteristic of linear selection allows the sense amplifier to be simple. This means that as the memory word length becomes longer, linear selection is more efficient in terms of transistors per bit.

Fig. 9 shows the relationship between number of words, word length, and the regions best suited for linear selection and coincident current. The graph is drawn assuming that the coincident-current drivers, switches and sense amplifier circuits have twice as many transistors as the linear-selection circuits. It also shows that any memory having 256 words or less for any word length will have fewer transistors if linear selection is used. The region that results in excessive back voltage for coincident-current memories (based on the 50-volt transistor breakdown) is shown as the diagonal line at the upper left. The voltage limit is shown for linear selection as the vertical line on the right. The linear-selection memory type may operate in the region where excessive back voltage limits coincident current.

In preparing this graph it was assumed that both a read and write driver is used in the linear-selection system. Present circuit techniques allow a single driver to be used for both the read and write operation. This technique is not possible in coincident current because of the strict current regulation required.

If the increased margins, reliability and the reduced complexity of core wiring for linear selection is taken as an added factor, the linear-selection region is extended as shown by the dotted line.

There are many circuit techniques that can be used in designing a linear-selection memory. The design depends on the operational characteristics desired. For example, a small memory of 256 words having only 40 bits and a  $6\mu\text{s}$  access time might use a simple read-write driver as shown in Fig. 10.

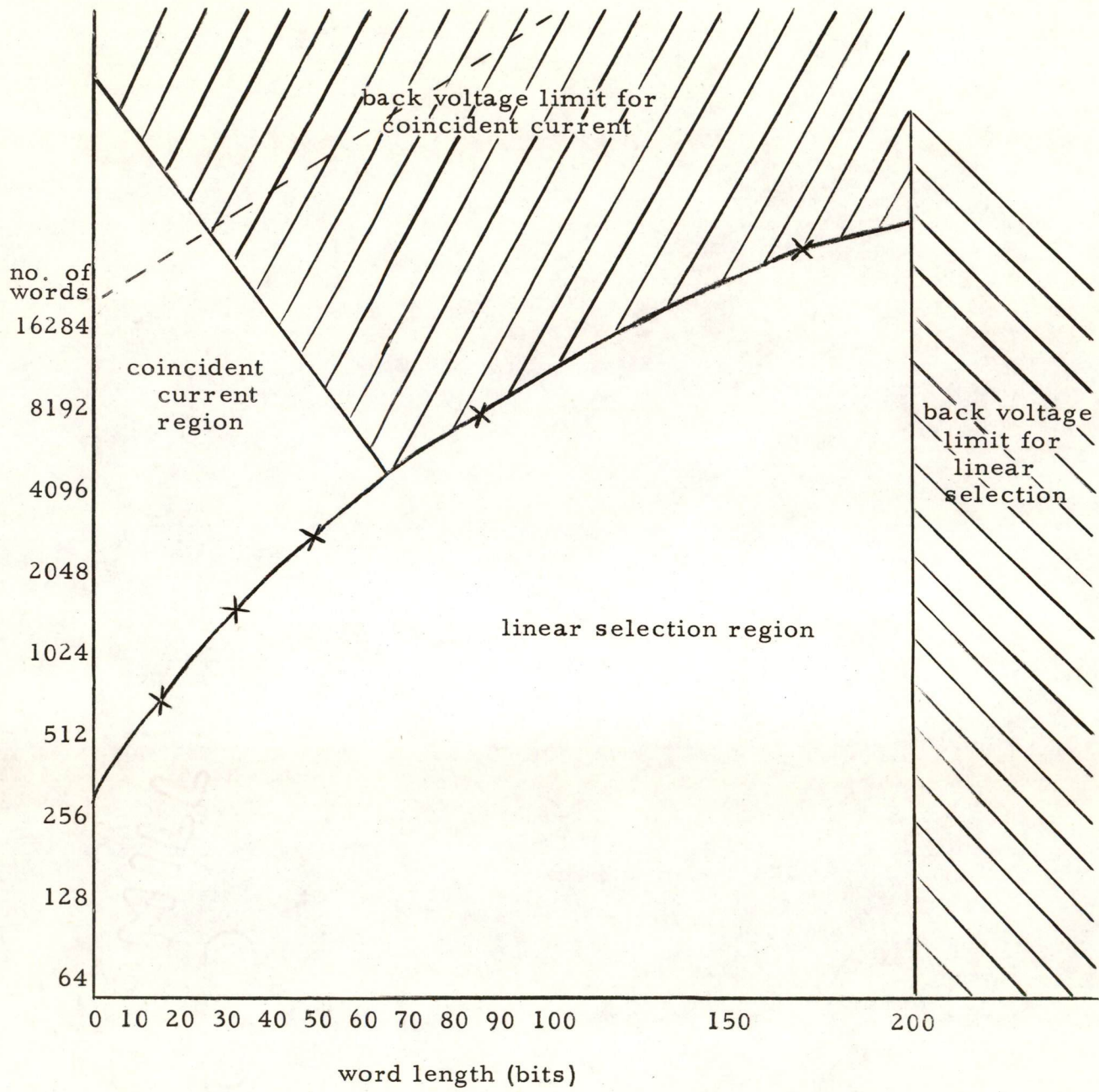


FIG. 9  
COINCIDENT-CURRENT AND LINEAR-SELECTION REGIONS



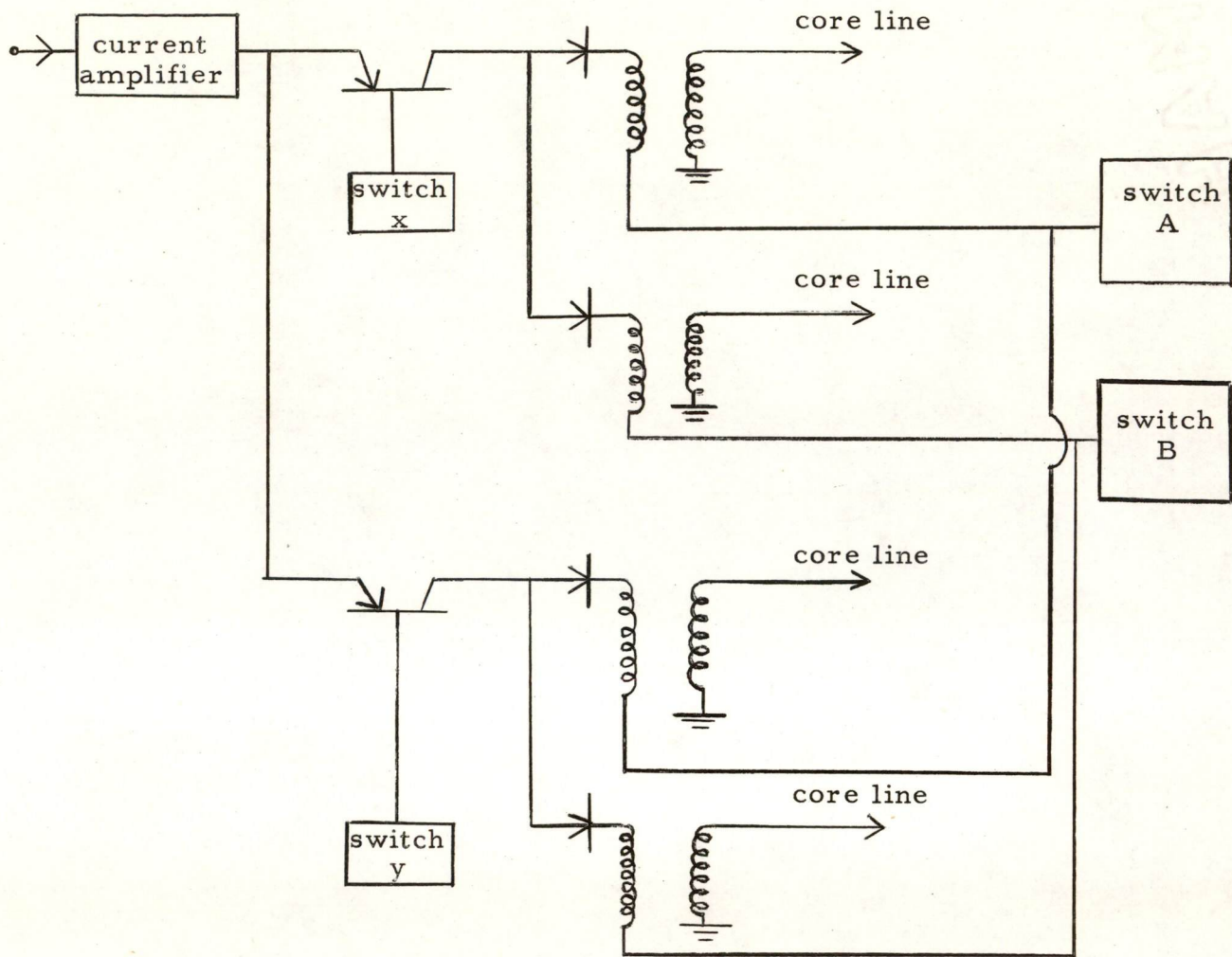


FIG. 10

## SIMPLE LINEAR-SELECTION SYSTEM

The switches A, B located in the primary circuit of the transformer allow the total number of drivers to be reduced to a reasonable number. The relation between these switches and drivers is given in Table II. The switches x, y in the base circuit allow the logic inputs to the driver to be reduced. In the 256-word memory only two of these switches might be used, since this reduces the logic inputs by one-half. The transformer is so selected that its magnetizing inductance is about twice that of the core line. (It should be noted that for reasonable word lengths the transformer has very low inductance and can be a low cost item.) The overshoot that results is used as

the write current for the core lines. Since the core-line impedance is not constant, the current regulation is not perfect. However, only a 15 per cent current variation exists for a 40-bit word length under the worst conditions. If the emphasis is on reliability increased margins, and non-critical circuits, this technique is applicable. If extreme speed is important then more sophisticated circuitry is needed. In any event, the total circuit count for the memory described is as follows:

1. Read drivers 16 units
2. Switches A, B 16 units
3. Switches x, y 2 or more
4. Transformers 256
5. Diodes 256
6. Logic inputs to drivers 8 or less
7. Logic inputs to switches A, B 16

Another example of a linear-selection memory will be given for a type that requires very fast access time. This memory requires 1024 words 150 bits in length and has a 3- $\mu$ s access time. If 1- $\mu$ s core material is to be used, it is obvious that more will be required of the circuitry than shown in the previous memory example. A driver has been designed that uses a switch core to obtain a more accurate write current than can be obtained with a transformer. The circuit is shown in Fig. 11.

The inverter circuit is used to establish a fixed voltage so that the input current to the actual driver  $T_3$  can be accurately determined. There may be only one inverter circuit common to all the driver transistors. This would require switches at the bases of the driver transistors, but the current level is low and the switches would be small. The switch core has a 2:1 ratio, and if 150 cores are driven, the back voltage at the driver collector due to the cores is about 20 volts. In order to reduce the number of drivers, switches are placed at the end of the core lines. Previous examples showed these switches in the primary of the transformer. The switches are required to accept only half currents when placed in the primary assuming a transformer ratio of 2:1. In this example the switches are placed at the end of the core lines and must accept the full current. However, using this method allows the number of switch cores used to be reduced from 1024 to 32. Diodes must be used to prevent sneak paths, but these are cheaper and



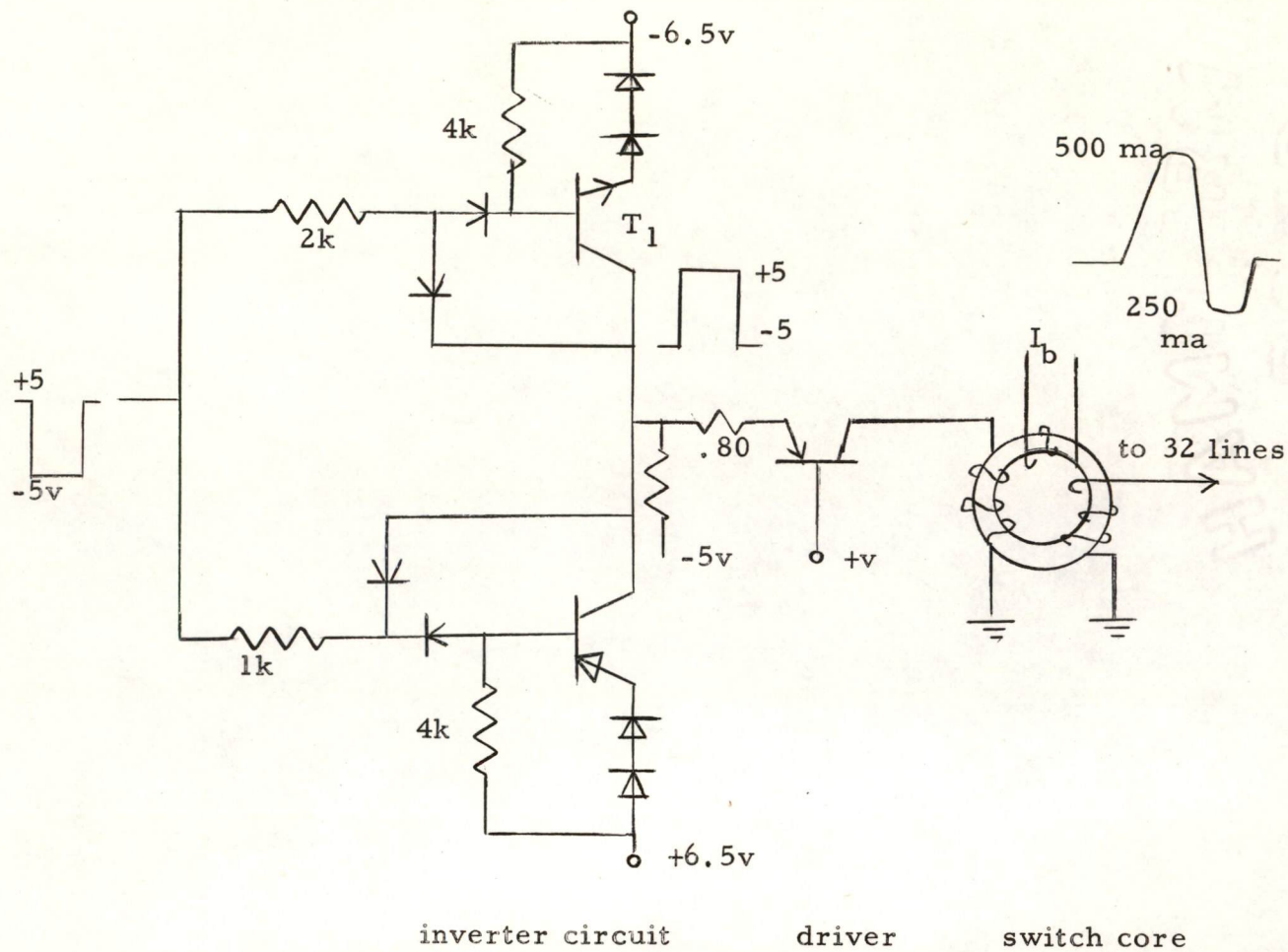


FIG. 11  
LINEAR-SELECTION DRIVER

smaller than the switch cores. The switch circuit is shown in Fig. 12. The complete memory driving system is shown in Fig. 13.

The total circuit count is as follows:

	<u>Circuits</u>		<u>Transistors</u>
Read-write drivers	32		3
Switches type A, B	32		5
Switch cores	32		
Sense amplifiers	150		5
Digit drivers	150		3

Total 1456

The read current is such that the cores are overdriven to reduce their switching time. An alternate method is also being investigated and that is to operate the cores on a minor hysteresis loop. This of course requires low current drive and some simplification of the circuits will result. For the 3- $\mu$ s access time required of this memory, the increased switching time of the cores when the low current drive is used may rule out its use. For a linear-selection memory operating with a reasonable access time this technique may be a useful one.

The linear-selection memory described has been designed for speed and economy of transformers or switch cores. The speed and word length are such that present coincident-current transistor memories cannot be used without using a split-word method.

The coincident-current memory would require 24 drivers and 12 switches for a minimum system to drive 1024 words 70 bits long. The number must be doubled for the complete memory. The driver currents are less here but the current wave-shape requirements are more severe than the linear-selection memory. Assuming that the present coincident-current memory (64 x 64 x 32) gives some practical numbers, a reasonable transistor count for this memory would be about 3200.

dfd



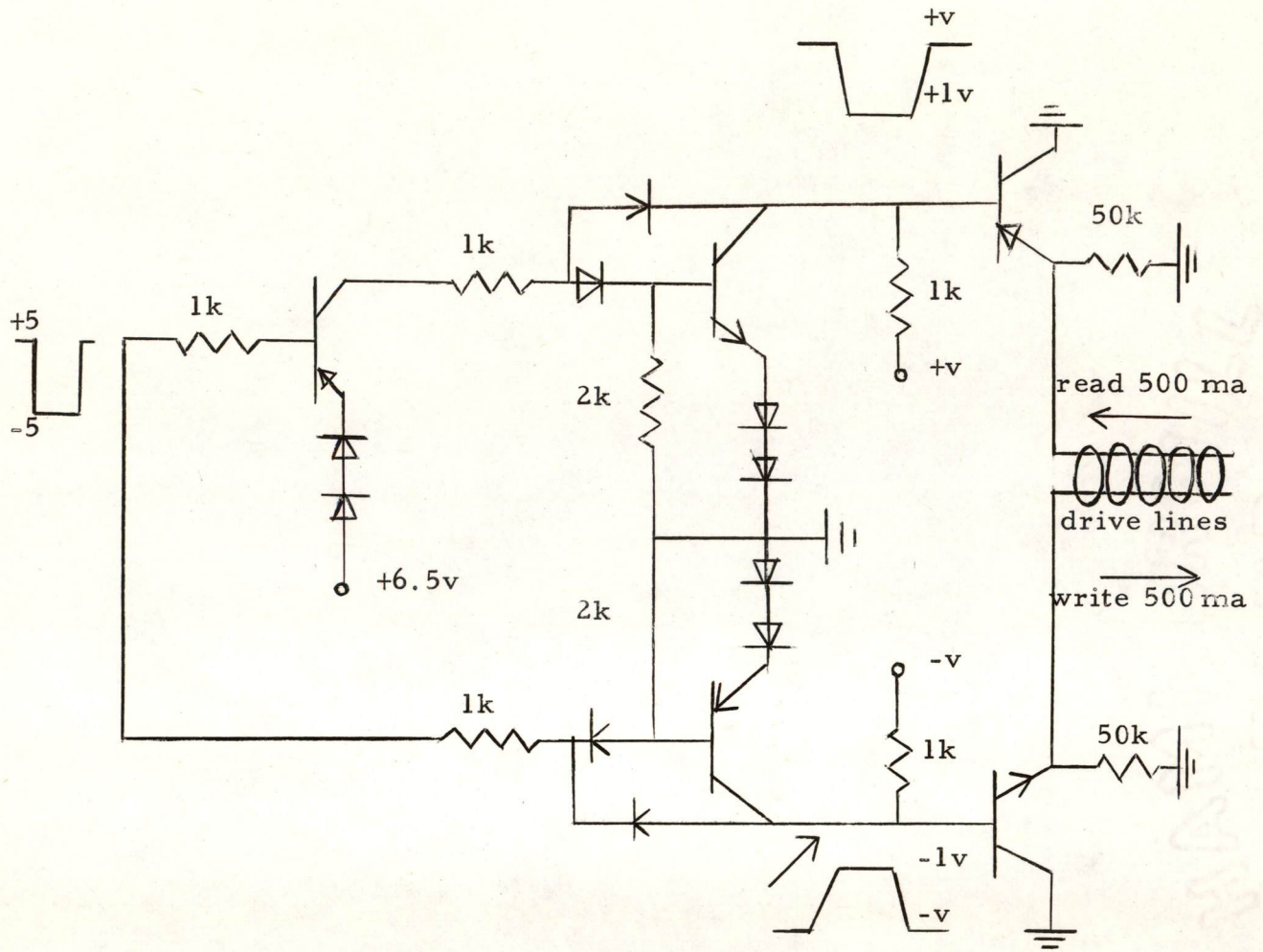


FIG. 12

LINEAR-SELECTION SWITCH

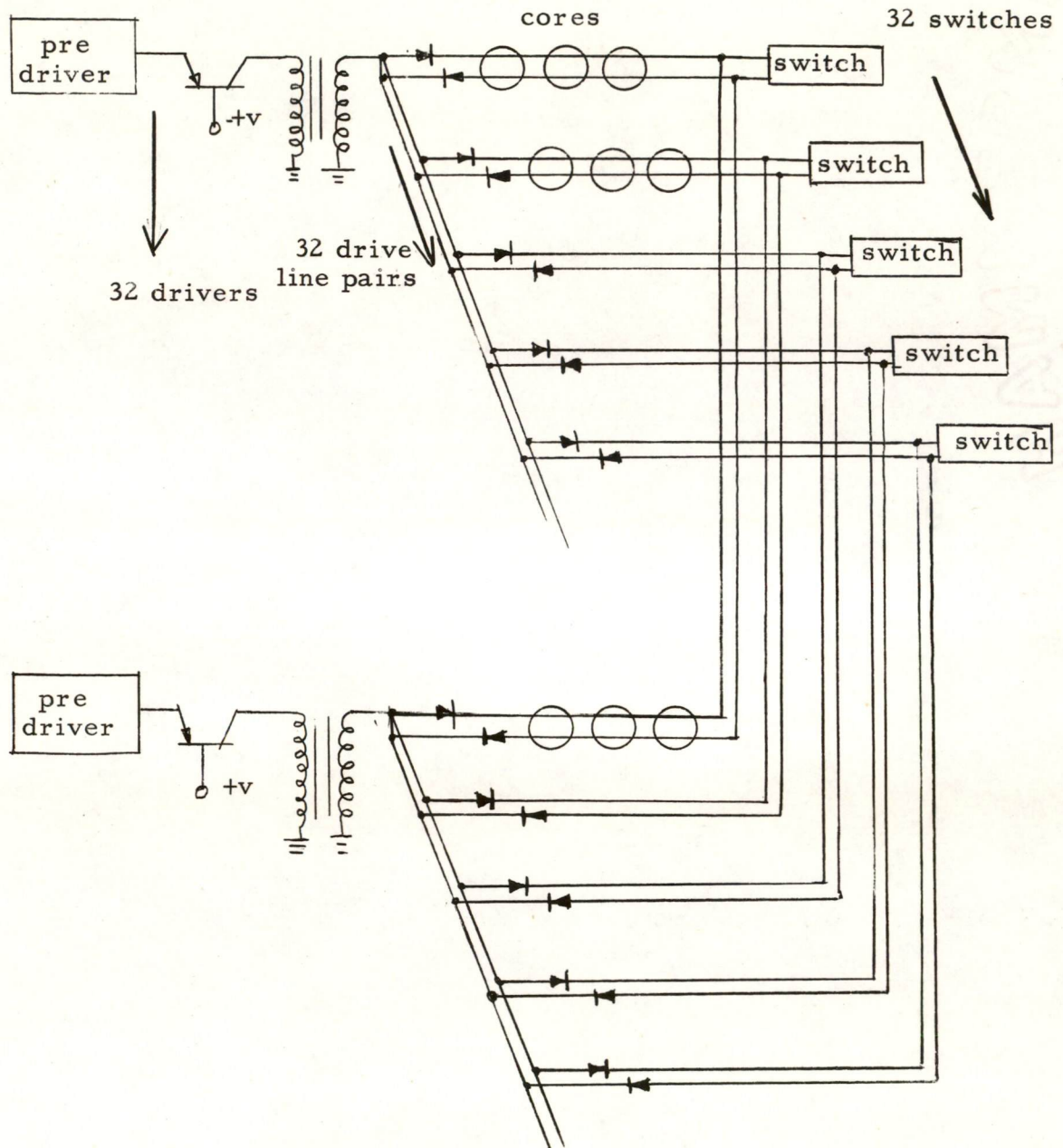


FIG. 13

LINEAR-SELECTION MEMORY DRIVE SYSTEM



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## Preliminary Draft

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William N. Papian  
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### THE MIT MAGNETIC-CORE MEMORY

One recent development which is significantly raising the reliability of today's high-speed automatic digital computer is the multicoordinate magnetic-core memory. Two banks of 32 by 32 by 17 magnetic-core memory have been in full-time computer operation at the MIT Digital Computer Laboratory for some months. A description of the units and of the tests and operational data available on them will be preceded by a short review of the operating principles of this type of memory.

#### 1. OPERATING PRINCIPLES<sup>1</sup>

Each binary digit is stored in the stationary magnetic field of a small, ring-shaped, ferromagnetic core. Two aspects of the core's rectangular flux-current characteristic are utilized:

- a. The flux remanence of the core is utilized for the storage operation;<sup>2</sup>
- b. The extreme nonlinearity of the flux-current characteristic is utilized to advantage in the selection operation.<sup>3,4</sup>

Fig. 1 shows the flux-current loop for a ferrite core. The remanent flux points are arbitrarily designated as ZERO and ONE. Note that the loop is sufficiently nonlinear so that the application of  $I_m/2$  cannot switch the core, whereas the full  $I_m$  can. Fig. 2 illustrates how this nonlinearity may be used to select one core out of many by the coincidence of two half-currents in a 2-coordinate scheme. The extension to three coordinates may be accomplished by stacking planes like those of Fig. 2 behind each other and connecting respective x and y coordinate lines in common to obtain a "volume" of cores as sketched in Fig. 3.

The application of a half current to the coordinate  $x_0$  results in the half excitation of a "selection plane" through the volume.



The same is true for the coordinate  $y_m$ , and the result is full-current excitation of the line of cores at the intersection of these two selection planes. The internal memory for a parallel type of machine might well resemble Fig. 3, and the selected line of cores might well represent the selected memory register, or word. A read-out or sensing winding threaded through every core in each  $xy$ , or digit, plane would bring out the signal representing the stored digit. This part of the read operation is destructive, and the word must be rewritten. For the rewrite part of the operation the selection technique remains the same, except that the half currents on the selection planes are now in the write polarity, which would result in the writing of ONE's into all the cores of the selected register; this writing is controllable for each  $xy$ , or digit, plane by the use of a digit-plane winding on which may be applied a half current of an effective polarity opposite to the write currents. The presence of this "inhibit" current in any digit during the write operation leaves a ZERO; absence of the inhibit current leaves a ONE.

R. R. Everett of MIT showed that these techniques may be extended into any number of coordinates but that the 2-coordinate read and 3-coordinate write system just described is one of the most desirable for the Whirlwind type of machine.

## 2. DESCRIPTION OF MEMORY

The capacity of each memory bank is  $1024$  registers, with 16 digits (plus 1 parity digit) per register. The basic operating mode, or sequence, consists of setting the memory-address register to the new address and applying the read-current pulses, followed by the write currents for rewriting the information just removed. The information is stored in a memory-buffer register. The speed of the machine may be judged from the timing diagram (Fig. 4). Note that the read-rewrite, or cycle, time is approximately 9 microseconds and that there are no restraints on how frequently this cycle may be applied to the memory. It is capable, therefore, of a basic repetition rate of over 100 kilocycles per second. Note also that the information can be available to the machine approximately 2.5 microseconds from the beginning of the cycle.

### 2.1 Block Schematic

Fig. 5 shows a block schematic of one bank of memory. Each half of the binary address in the Address Register is translated to a 1-out-of-32 selection by a crystal-diode Matrix and sets up a pair of "AND" gates for  $x$  and a pair for  $y$ . The Read Flip-Flop forms the 1.5-microsecond pulse and sends it to the two selected Read Drivers which supply the 0.5-ampere currents to two selection planes. The output signal voltages from each digit plane are amplified in the Sense Amplifiers and applied to "AND" gates which are strobed at the optimum time by a short (0.1-microsecond) pulse. ONE's then go off to set the Buffer Register to the just-extracted number. At the end of the read



currents the rewrite part of the operation starts in the same manner, except that the write currents have to be safely overlapped by the inhibit currents at those digit planes where ZERO's are to be written. This is accomplished by having the "on" time of the Inhibit Flip-Flop overlap slightly that of the Write Flip-Flop. Short (1 microsecond) currents may be applied to all digit planes after the rewrite; they are called Post-Write Disturb (PWD) currents and are used to improve the ONE-to-ZERO signal ratios. The PWD Flip-Flop forms this pulse and applies it to all 17 of the Digit-Plane Drivers through "OR" inputs.

## 2.2 The Cores

The cores are made of General Ceramics material MF-1326B. The first bank contains their core size F-291 which has an outside diameter of 90 mils. A smaller core was used in the second bank; this is F-394, 80 mils in outside diameter. Single-turn switching currents are approximately 950 and 850 milliamperes, and single-turn output voltages (at optimum strobe time) are about 110 and 90 millivolts, respectively. Switching time, under these conditions, is approximately 1.5 microseconds.

Core selection (a tedious and expensive operation) was made on the basis of a series of pulse tests, approximately four per core, and resulted in a yield for the first bank of approximately 30 per cent of those shipped to us by the producer. The selection criterion was fundamentally that of an upper and lower limit on the voltage output from each core when the core was excited by a sequence of current pulses devised to resemble computer operation. Fig. 6 shows typical output-voltage pulse shapes, the nominal limits within which cores were considered acceptable, and the strobe time at which these amplitudes were taken. The yield improved somewhat for the second bank of cores.

## 2.3 Basic-Circuit Types

The selection planes of the memory are driven directly from vacuum-tube plates. A single type-6080 vacuum tube, with its sections paralleled, is used to drive a given selection plane in the read direction. Another such tube drives the same plane in the write direction. The control grids of the 6080's are driven through 6BL7 amplifiers from the crystal-matrix output lines. The cathodes of all of the 6080 tubes in the x-read group are connected together, then through a large resistor to a negative-voltage supply. The cathodes of the three other groups of 6080's (x-write, y-read, z-write) are all connected in a similar manner. Each group of cathodes is normally held at a relatively high potential by a power amplifier and is allowed to drop at the proper time. Thus, each 6080 acts not only as a cathode follower but as the logical "AND" gate shown separately in the block schematic. The large amount of degeneration caused by the high common-cathode resistor compensates for nonuniformity and aging changes in the characteristics of the tubes. As a result, selection-plane currents remain within very close tolerances (approximately plus or minus 2 or 3 per cent).

The output signal from the sensing, or read-out, winding is linearly amplified from the 100-millivolt level up to approximately



a 30-volt level in a single-sided, a-c coupled, wide-band feedback amplifier. The signal is then rectified and applied to the suppressor grid of a 7AK7 gate tube on a bias level of about 30 volts. The control grid of the gate tube is pulsed with a 0.1-microsecond pulse at the optimum moment so that a "standard" Whirlwind pulse issued from the gate to indicate when a ONE is being read.

The digit-plane driver consists of a 6080 dual triode driven from two amplifier stages and incorporating sufficient negative feedback from the output to the input to keep the current amplitude within plus or minus 3 per cent over expected tube, component, and power-supply variations.

#### 2.4 Layout and Packaging

A finished memory plane is shown in Fig. 7. The frame's outside dimensions are approximately 9.5 by 9.5 inches. All the windings consist of 32-gauge magnet wire with quadruple-Formex insulation. Fig. 8 shows the cores and wires in some detail. The x and y pairs run vertically and horizontally, the sense winding runs along the diagonals, and the digit-plane winding runs horizontally (but is obscured in the shadow around the y pairs). Wiring time for one plane was about one man-week, including an intermediate test and final inspection. The intermediate test was performed when all the cores and x and y wires were in place but before the digit-plane and sense windings were installed. The test consisted of applying a sequence of current pulses to a given x line and observing the response of each of the 32 cores on that line by manually stepping the observing-scope probe from one y line to the next. This test was repeated for subsequent x lines, until the 1024 cores were completed. Cores which displayed abnormally high or low outputs were marked for replacement. About 3 cores per plane were replaced.

The 17 finished planes were mounted in a stack or array, as shown in Fig. 9. Plane-to-plane connections are made by means of the vertical busses soldered into the slotted lugs. Digit-plane and sense-winding connections were made from the same corner of each plane to a mounting board of connectors for coaxial connection to another rack. Selection-plane-driving connections fan out horizontally at the top and bottom of the array. It takes 3 to 4 hours to replace either the entire array or any single plane.

Fig. 9 includes a view of part of the four-posted stall, or rack, in which the array is mounted. Figs. 10 and 11 show fuller views of the stall (and the Memory Test Computer room). Selection-plane-driver panels are mounted on the four faces of the stall with tubes pointing outward. Visible in the stall above and below the selection-plane-driver panels are the two crystal-matrix switches. The general arrangement is such that temperature-sensitive components, such as cores and crystal diodes, are inside the stall, and large heat-dissipating components, such as tubes and power resistors, are on the outside of the stall.

The sense amplifiers and digit-plane drivers are in plug-in chassis stacked in a vertical rack next to the memory stall.



### 3. TESTS AND PERFORMANCE

Ultimate judgment on the reliability of this particular core memory must rest on its performance over the next year or two. Tentative evaluation may be made, however, from observations of performance during the 4 months that one bank operated in the Memory Test Computer and the 3 months of 2-bank operation in Whirlwind. In addition, much may be determined from the results of tests made on the memory to ascertain its tolerance to variations in the parameters significant to its operation.

#### 3.1 Parameter Variations

Many conditions, or parameters, affect the operation of a core memory; driving currents (x, y, read, write, inhibit, and disturb), sense-amplifier gains, strobe time, ambient temperature, memory-information pattern, and repetition rate are good examples. These parameters are not all equally significant or equally easy to manipulate, and so some of them have, as yet, been examined in only a cursory manner. Because sense-amplifier gains have a simple, nearly linear, effect on operation they were adjusted and held at one setting during the tests. Ambient temperature is expected to be held within close tolerances in any operating machine, and a fair amount of information is available on the subject from the core-testing work; temperature was not controlled during the tests but recorded readings were kept. Memory-information pattern and repetition rate were controllable to some degree by the program being run; a program which seemed to give the most adverse pattern and rate was designed and used during most of the testing.

The tests were made on the Memory Test Computer, a high-speed, 16-digit, parallel machine of the Whirlwind type. The machine has a parity checking system which computes whether each 16-digit word to be stored contains an odd or an even number of ONE's, stores the result of this "parity count" in the 17th digit, recomputes the count when the word is read out, and rings an alarm if the result does not check with the contents of the 17th digit. Although major reliance was placed on parity checking for detecting memory malfunction, there was also some programmed identity checking used.

The bias bounds of the sense-gates suppressor grids were chosen as a very convenient measure of the quality of the memory output. The upper bound (least bias) is the point at which errors occur because the gate is mistaking the largest ZERO output for a ONE; at the lower bound (most bias) errors occur because the gate mistakes the smallest ONE output for a ZERO. The bias difference, in volts, is a direct measure of the voltage difference at strobe time between the smallest ONE and the largest ZERO.

Fig. 12 shows the bias bounds for all 17 sense gates as a function of the selection-plane driving-current amplitudes (x, y, read, and write). The program used was the so-called "inchworm" in which 16 words of instructions "bootstrap" themselves around the 1024 registers of the memory. The ambient temperature was recorded at approximately 88 degrees Fahrenheit, about 15 degrees higher than what is now believed



to be optimum. Two curves are shown, one for digit-plane currents set at 400 milliamperes and the other at 450 milliamperes. The enclosed areas indicate how much the safe operating point of the memory bank may wander; recent circuit and adjustment improvements have enlarged these enclosed areas somewhat. Fig. 13 shows the bias bounds as a function of the timing of the strobe pulse. Time is measured, on this graph, from the instant the Read Flip-Flop is pulsed by the Start Read pulse. The three curves are for three values of selection-plane driving current, two extremes and one near optimum. A wide operating region is again indicated.

### 3.2 Computer Operation

The first bank of memory has been in use in Whirlwind since mid-August, the second since 5 September. There has been a steady improvement in their operation as the installation, which was an extremely hurried one, has been gradually cleaned up and made permanent and, also, as the process of debugging these relatively new equipments proceeded. The two banks have not, as yet, been brought to an equal degree of reliability; this may be due, in part, to the fact that the cores in the first bank were not selected as carefully as those in the second so that output ONE/ZERO ratios are not as large. The demands on the Whirlwind computer are heavy, and only a few hours a month are available for further development work on the memory.

The memory bank which has been in Whirlwind since 5 September is giving approximately one parity alarm per week. (Note that a parity check is performed every time the memory is queried.) On the average, this amounts to one detected memory error in about 115 hours of useful operation or, assuming a 30-microsecond average order time, one detected memory error per 14-billion average orders, each average order requiring slightly over two accesses to memory. This comes, roughly, to one detected memory error per 30 billion word accesses or, since there are 16 bits per word, one error per 480 billion bit accesses.

The exact nature of these errors is, as yet, not known. It is hoped that further work on the system will shed more light on the problem as well as reduce the error rate.

## 4. CONCLUSION

The test results and experience obtained thus far on the two 32 by 32 by 17 banks of magnetic-core memory now operating as the internal memory of the Whirlwind machine indicate high promise for this type of storage. Reasonable engineering extrapolations of the results are being used in present work on a 64 by 64 by 17 bank which is expected to be in operation in the Memory Test Computer by January 1954.



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LINCOLN LABORATORY

TRANSISTOR REGULATED POWER SUPPLIES

F. G. POPP

19 JANUARY 1956

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MASSACHUSETTS INSTITUTE OF TECHNOLOGY  
LINCOLN LABORATORY

TRANSISTOR REGULATED POWER SUPPLIES

F. G. Popp

Group 24

Technical Report No. 106

19 January 1956

ABSTRACT

A method of designing power supplies utilizing power transistors as series-regulating elements and silicon diodes as voltage references is described. Information is given on efficiency, output impedance, regulation, ripple reduction and limits on output voltage and output power. Several variations of circuit design are given as well as circuit schematics for power supplies already in operation.

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## TRANSISTOR REGULATED POWER SUPPLIES

The aim of the present research is to show the feasibility of building a light-weight power supply for aircraft use that is capable of delivering high currents at the low voltages needed for transistorized equipment. The design utilizes power transistors as series-regulating elements and silicon diodes as voltage references. Filament transformers and chokes can thereby be eliminated. Since it is desirable that the supply be put under actual operating conditions in equipment that will be continuously operated in the laboratory, the circuits were designed for 60-cps line voltage and with outputs suitable for the transistorized magnetic core memory.

None of the basic circuit features need be changed for 400-cps operation. In fact, in this case, the cooling of the power transistors (which presents a major problem in this type of supply) can possibly be done more effectively by using small fans blowing directly on the transistors. The use of fans is impractical at 60 cps, since all types presently available are too large and too heavy. The filter capacitors (which take up a large amount of space in the present design) need be only one-sixth as large for 400-cps operation and the use of small tantalum electrolytics is possible.

The transistor type used for the main series-regulating element is the Minneapolis-Honeywell P-11. This is the highest power transistor presently available. It is still made under laboratory conditions and is not available in large quantities. The XH-25 (being developed under military sponsorship) will eventually replace the P-11. The internal thermal resistance from junction to mounting stud is 3°F per watt for the P-11 and 2°F per watt for the XH-25. The manufacturer's recommended maximum junction temperature is 200°F. The transistor will still operate satisfactorily with a junction temperature of 250°F but its life is shortened and we do not, as yet, have any life-test data showing the maximum temperature practical for continuous use.

The largest heat dissipator used with the P-11 had a thermal resistance of approximately 2°F per watt. Consequently, the maximum dissipation allowable for the P-11 is about 25 watts. The maximum collector current is 5 amp.

The basic regulating circuit is shown in Fig. 1.

All load current flows through the P-11 transistor; a fraction of this enters the emitter of the H-2, which in turn sends part through R1. The resistor R1 provides a return path for both the diode current and the base current of H-2. The emitter-to-base voltage of P-11 and of H-2 will vary with load current but will usually be small in comparison with the output voltage. The following typical values are presented.

P-11	$I_e = 2$ amp	$V_{eb} = 0.6$ volt
H-2	$I_e = 0.1$ amp	$V_{eb} = 0.25$ volt

Changes in the input voltage cause a change in the base-to-collector voltage of P-11 and H-2.

An increase in load current (i.e., emitter current) causes an increase in base current; an increase in input voltage (i.e., collector voltage) causes a decrease in base current. For low-voltage supplies the latter effect is small, but can be quite troublesome for high-voltage supplies. A built-in load should be provided for both transistors if there is a chance of the base



current reversing under minimum-load, high input-voltage conditions. An increase in H-2 base current causes a decrease in the reverse diode current. The value of R1 must be such that the diode is not cut off with maximum load and minimum input voltage and that the diode is not overloaded with minimum load and maximum input voltage.

Silicon diodes are usually rated at 125 mw in an ambient of 25°C, and derated at a 1 mw/°C rise in the ambient temperature. The reverse saturation voltage increases with current and ambient temperature. The latter effect is small (0.1 per cent/°C) but the decrease in impedance with increasing temperature is quite large. The impedance varies considerably from diode to diode and is greater for diodes with higher reverse saturation voltages. No exact information can be given concerning the impedance to be expected for a diode with a given saturation breakdown voltage, but typical values are:

9 volt breakdown	10 ohms
19 volt breakdown	100 ohms
35 volt breakdown	300 ohms
75 volt breakdown	1000 ohms

The basic circuit shown above uses two transistors. The number used depends on the maximum base current change that can be handled by the silicon diode. Each transistor can be thought of as a current transformer. A given change in P-11 emitter current (no load to full load) causes a correspondingly smaller change in H-2 emitter current. A third transistor would have a still smaller emitter current change, and its base current change would be very small. If  $B = \Delta I_e / \Delta I_b$ , a satisfactory design value for B is 20. This, of course, will vary considerably for different transistors and different operating voltages and currents. Thus, with three transistors a load change of 5 amp may produce a diode current change of less than 1 ma.

Two undesirable features increase, however, with an increase in the number of transistors used; namely, an increase in diode current change due to changing input voltage and an increase in the output impedance of the power supply. A typical value of output impedance is 0.25 ohm.

The unregulated DC input to the above basic circuit has been obtained from full-wave bridge-germanium rectifier units and a low-pass filter.

Each regulating transistor (p-n-p) must have its collector at a negative voltage with respect to its base at all times during the ripple voltage cycle. To meet this condition, the DC level of the collector must be at least one-half the peak-to-peak ripple voltage (with respect to the base). The dissipation at the collector, however, is proportional to the collector-to-base voltage. Consequently, it is necessary for the ripple output of the filter to be small so that the collector dissipation is kept as low as possible.

In the present design, the peak-to-peak ripple output of the filter has been kept below 1 volt. The collector-to-base voltage will increase for increasing line voltages and decreasing load current, depending on the regulation of the input circuit. Obviously, a choke input filter would be best, insofar as obtaining minimum heating of the regulating transistors is concerned. But since the elimination of heavy components was one of the goals undertaken by the present work, all but one of the power supplies were built with capacitor-input RC filters. This imposes



a severer condition than is necessary on the transistors. However, excellent results have been obtained from all the circuits shown in this report, except that of the 150-volt DC output. For high-voltage outputs (100 volts or more), it is therefore desirable to use choke input filters unless the filter output variation is kept small by the use of constant voltage transformers or constant load currents. The collector-to-base voltage of the P-11 transistor (and H-2) can be as high as 60 volts if the impedance in the base circuit is kept relatively small. Some difficulty was encountered in the 150-volt supply when the collector-to-base voltage exceeded 30 volts due to the relatively high impedance in the base circuit. For low-voltage outputs this trouble would not be present since the input variations can be kept small.

Figure 2 uses the same basic circuit of Fig. 1 but shows additional circuit details.

The capacitors C1 through C6 and the resistors R9 through R13 comprise the input filters. The resistors R10 through R13 are chosen so that the base-to-collector voltages of the various transistors are in the vicinity of 1 volt for maximum load and minimum input voltage. The main load current flows through P-11 and R13. The P-11 and H-2 transistors are used as in Fig. 1. Three silicon diodes are used to provide a reference voltage of 92 volts. Resistors R8 and R9 provide a return for the 10-volt diode current and the H-2 base current. The resistance must be large enough to keep the diode current change small for changing input voltage, but small enough so that the diode is not cut off for maximum load and minimum line voltage. If the current in the diode is too large for no load and maximum line voltage, several matched diodes may be placed in parallel. Resistors R6 and R7 provide emitter current for H-2 and P-11 under no-load conditions. Resistor R14 provides a return path for the CK750 base current and the two 41-volt diodes. This resistor can be connected to the negative input lead; however, since the negative output lead is negative with respect to the CK750 base, the connection shown eliminates a diode current change due to changing line voltage. A potentiometer R5 provides a means of changing the output voltage. The current through R4 and R5 must be large compared with the maximum 10-volt diode current (about 20 to 1) so that the 2N57 transistor receives a relatively constant emitter current. Resistors R1 and R2 are used to give better starting characteristics when diodes are used in series. Resistor R3 is usually not required but may be used to provide a more constant emitter current.

Capacitors can be placed across the output leads if the load contains high-frequency switching transients.

Figure 3 shows a different regulating circuit. The portion shown on the left is a constant-current generator (approximately). A mercury cell maintains a constant voltage between emitter and base of each transistor (P-11, H-2, 2N43). The potentiometer R1 provides a means of adjusting the output over a limited range. This method works best on low-voltage supplies since all the variation in input voltage occurs across the collectors of the three transistors. A large variation of collector voltage will cause a considerable change in base current which tends to defeat the constant current output desired. Best results are obviously obtained if  $R1 = 0$ , for then a change in base current in the 2N43 will not change the emitter-to-base voltage.

There are two main paths for the output of the current generator: (a) through the load and (b) through the P-11 (on the right) and a dummy load R5. The right side of Fig. 3,



showing the P-11, H-2 and CK750 transistors and the 19-volt silicon diode, is a regulating circuit similar to that in Fig. 1; however, in this case the load current does not flow through the P-11 transistor. As the load current increases, the current through the dummy load decreases and vice versa. In the method shown in Fig. 1, an increase in load current causes an increase in the base-to-emitter voltages of the regulating transistors and the output voltages decrease. If the H-4 part of the circuit were removed, Fig. 3 would give similar results; i.e., an increase in load current causes a decrease in dummy-load current producing a smaller base-to-emitter voltage and a decrease in output voltage. The H-4 transistor is added to give a rising characteristic just sufficient to counteract the falling characteristic. As the load current increases, the magnitude of the voltage drop across R5 decreases causing an increase in emitter current; the current in R8 increases and an increasing voltage is inserted in series with the 19-volt diode. The potentiometer R7 provides a means of adjusting the current in H-4, while the potentiometer R8 provides a means of changing the voltage inserted in series with the diode to give an accurate zero set. By adjusting both potentiometers to an optimum value, a very flat output characteristic is obtained.

Figure 4 shows how the basic circuit of Fig. 1 may be modified to regulate load voltages where the power is supplied from some external source. Only sufficient power need be supplied internally to keep the circuit in regulation for the no-load condition. Since this is small, it can be derived from some other voltage source.

Figures 5 through 9 show the complete circuit schematics for the magnetic core-memory power supply. The outputs for the core-memory power supply are presented in Table I.

TABLE I CORE-MEMORY POWER-SUPPLY OUTPUTS		
	Volts	Amperes
Unit 1	+ 90	1.25
	+ 33 to + 43	0.8
	+ 22 to + 32 (Load)	0.6
	+ 10	1.5
	+ 2	0.5
Unit 2	- 24	10
Unit 3	- 150	0.5
	- 30	2.0
	- 10	2.0
Unit 4	+ 20	2.5
	+ 10 (Load)	1.2
Over-all Efficiency: Approximately 50 per cent Line-Voltage Variation: 105 volts to 125 volts		



Table II gives an indication of performances.

TABLE II PERFORMANCE DATA FOR POWER SUPPLY			
	Load Current (amperes)	Output Voltage (volts)	Efficiency (per cent)
-24-volt supply (adjustable over a 3-volt range)	0	-25	-
	1	-24.8	53
	2	-24.5	56
	3	-24	58
	4	-23.7	59
	5	-23.2	58
	6.4	-22.8	60
	8	-21.8	60
	10	-21	59
	20-volt supply	0	20.1
1		20.0	22
2		20.0	42
+ 90-volt supply	0	91.0	-
	0.6	90.6	60
	1.0	90.	59
	1.25	89.8	61
+ 10-volt supply	0	10.0	-
	0.5	9.8	41
	1.0	9.5	35
	1.5	9.3	36

#### CONCLUSIONS

The designs described above demonstrate the feasibility of building light-weight power supplies giving adequate regulation without the use of chokes for output voltages less than 100 volts DC. For higher voltages, choke input filters should be used. Satisfactory operation cannot be expected at ambient temperatures much higher than 110°F unless forced cooling is used for the regulating transistors. Some difficulty has been experienced in the fusing of the outputs. If a short circuit is placed externally across the output leads, the P-11 regulating transistor is destroyed before a standard fuse blows. It does appear that a quick-blowing (8AG type) fuse is rapid enough to prevent destruction of the transistor.

If lightness in weight is not a requirement, a constant voltage transformer should be used on the input. In this way, the collector dissipation can be held to a minimum resulting in greater efficiency and higher permissible ambient operating temperatures. In this case, the chief purpose of the circuit is to regulate against output voltage changes due to changing loads.

Although the design is not satisfactory for high output voltages, there is no difficulty in obtaining large load currents, since parallel operation of the regulating transistors is practical. In general, one P-11 transistor can supply a load of 100 watts when regulating for both load changes and line-voltage changes.



For loads not presenting rapid current changes (high frequencies) the output impedance is of the order of 0.1 to 1 ohm, without the use of output capacitors. If high-speed switching circuits constitute the load, sufficient capacitance must be used to keep the instantaneous output impedance low. When used, these capacitors should be placed before the output fuse. Thus, if the output leads are short circuited at any time, the capacitor discharge current will flow through the fuse, helping it to blow before the regulating transistor receives too much current.

If a constant voltage transformer is used on the input, efficiencies of the order of 60 to 70 per cent can be achieved. If the supply must regulate against a  $\pm 10$  per cent line-voltage variation, the efficiency will range from 50 to 60 per cent for high output voltages (20 volts or higher). For low output voltages the efficiency may drop to below 40 per cent. The efficiency of the design shown in Fig. 3 is proportional to the load and will vary from zero to 50 per cent.

The regulation with load can be made almost perfect with the design shown in Fig. 3. No attempt was made to achieve optimum conditions but it was possible to obtain a voltage change of less than one-half per cent from no load to full load. For the other designs, the regulation is a function of the output voltage and the load. For a 100-volt 1-amp supply, the voltage variation is about 1 per cent. For a 10-volt 1-amp supply, the voltage variation is about 5 per cent. For a 24-volt 10-amp supply the voltage variation is about 16 per cent.

The regulation for line-voltage change depends on the design of the transformer and the input filter. With a capacitor input filter the output voltage variation can be held to  $\pm 2$  per cent for a line variation of  $\pm 10$  per cent. About half of this variation can be attributed to the regulator.

The 120-cps ripple voltage in the output (without output capacitors) is about 1 per cent of the ripple output of the filter. The ripple output is proportional to the load current and does not depend on output voltage.

If the dissipation for the P-11 transistor is kept below 10 watts, it can be mounted directly on a standard chassis. For dissipation up to 15 watts, the transistor should be mounted on a 4 inch  $\times$  4 inch  $\times$  1/4 inch aluminum plate that is separated from the chassis by a 0.002 inch thick sheet of mica. For higher dissipations, a special heat dissipator consisting of a number of plates or fins must be used (see Fig. 9).



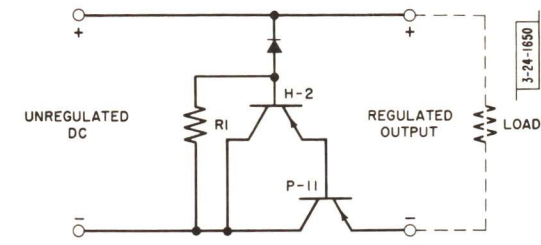


Fig.1. Basic regulating circuit.

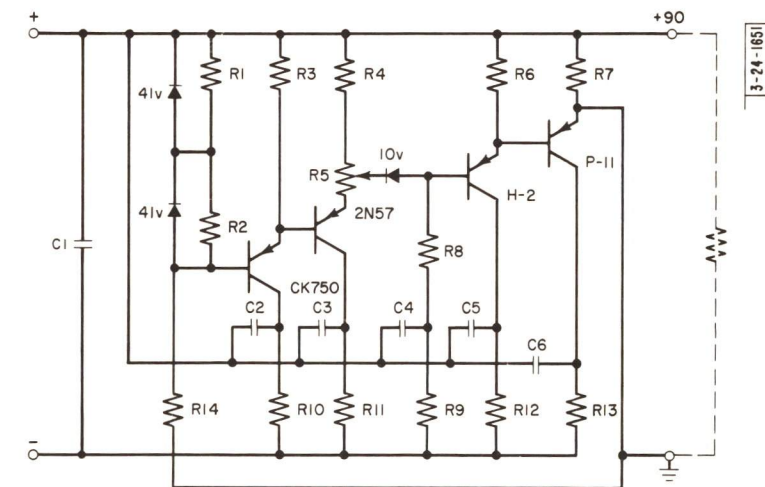


Fig.2. Complete basic regulating circuit.



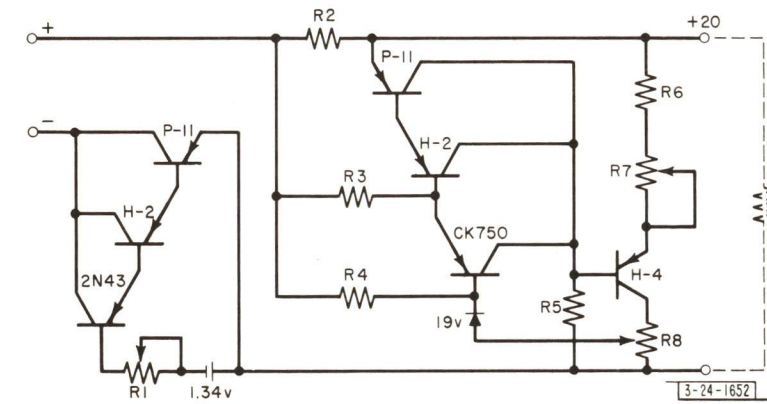


Fig.3. Constant-current generator form of regulating circuit.

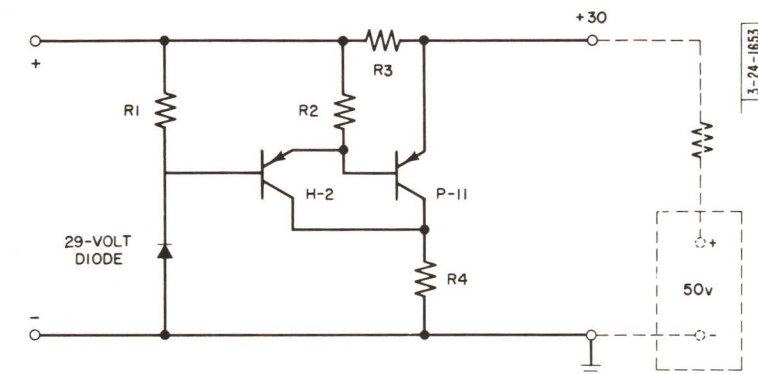


Fig.4. Basic circuit for regulating load voltages.



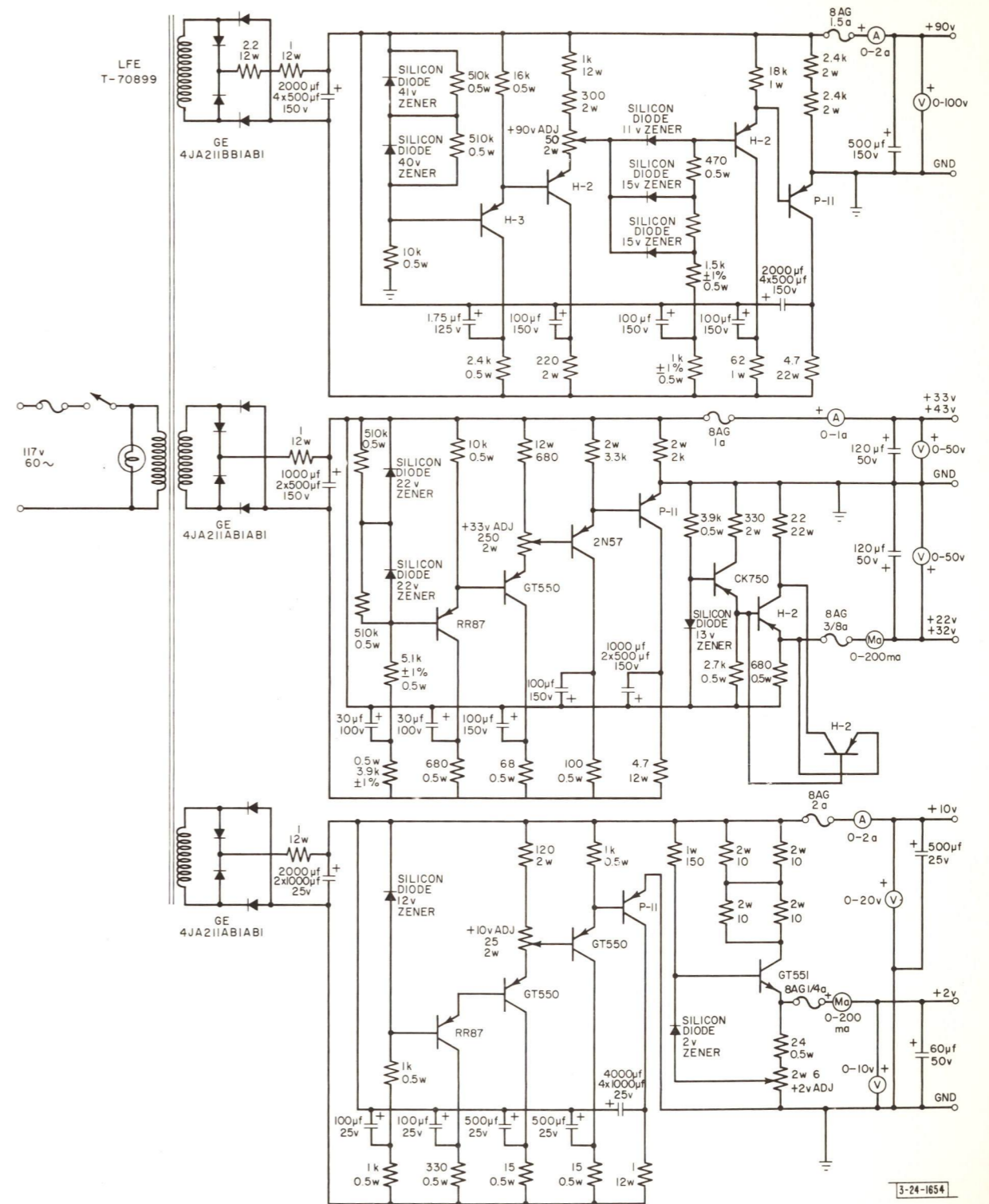


Fig.5. Schematic of regulated power supply for magnetic core memory.







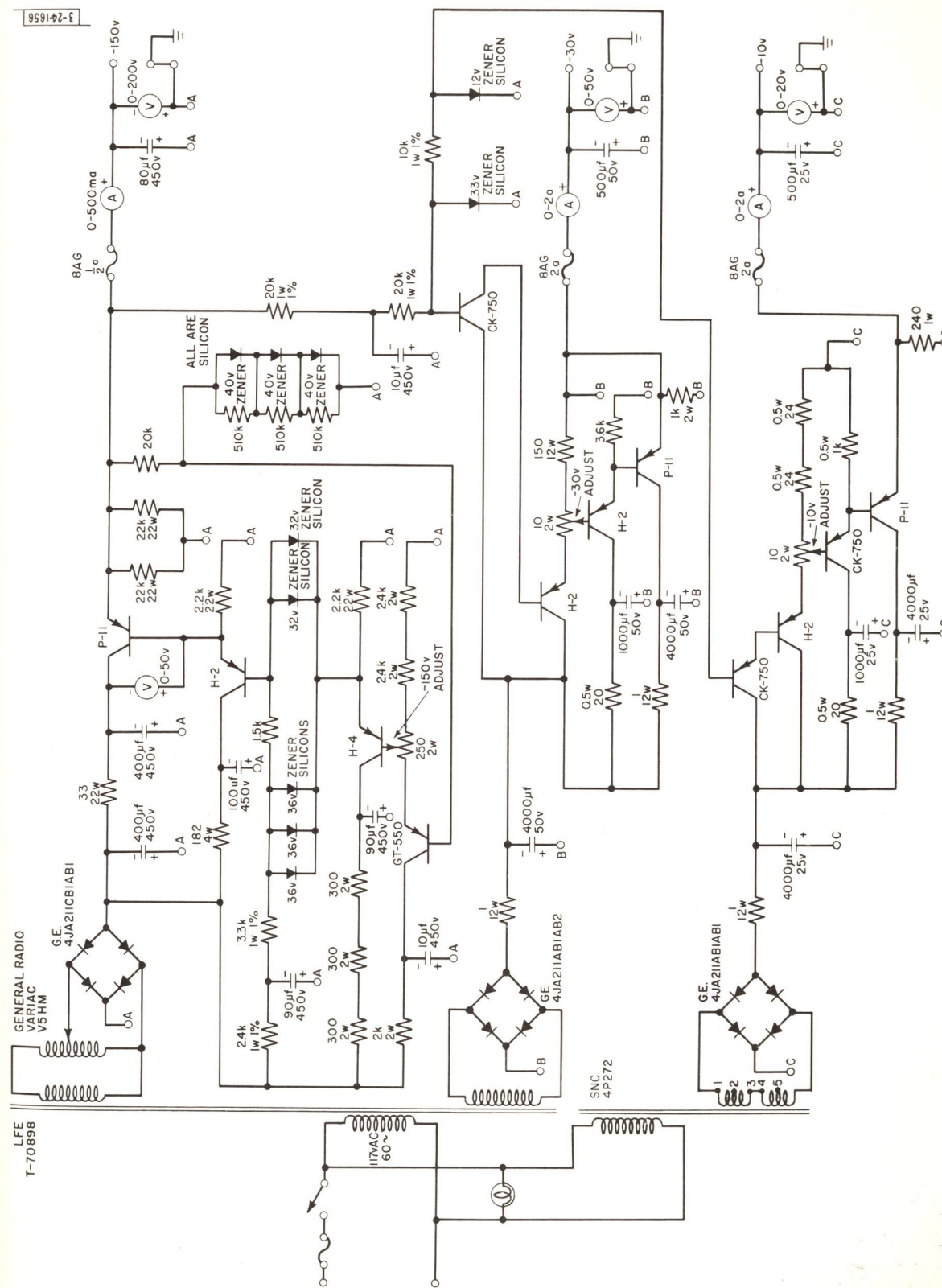


Fig.7. Schematic of regulated power supply for magnetic core memory.



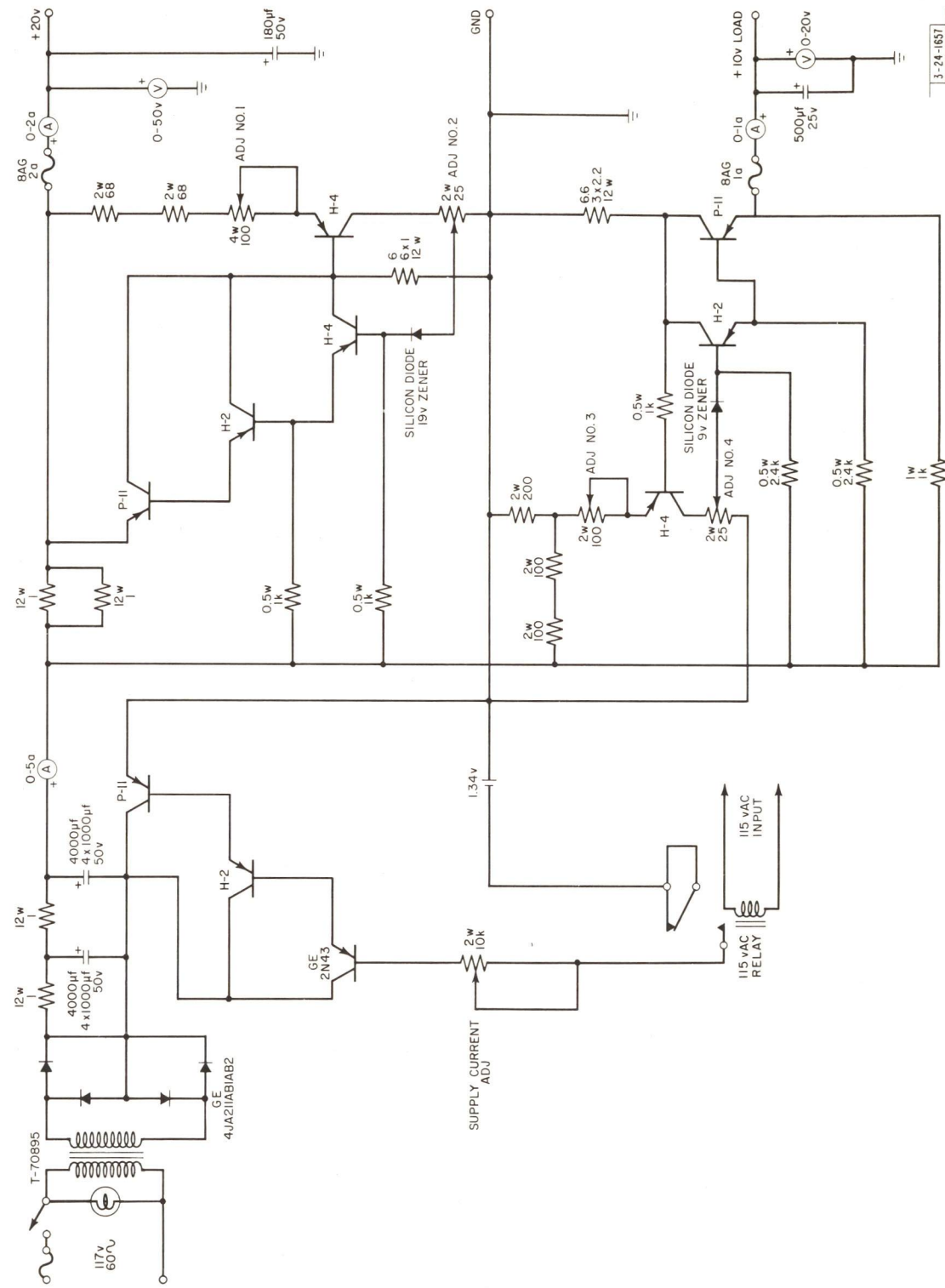


Fig. 8. Schematic of regulated power supply for magnetic core memory.



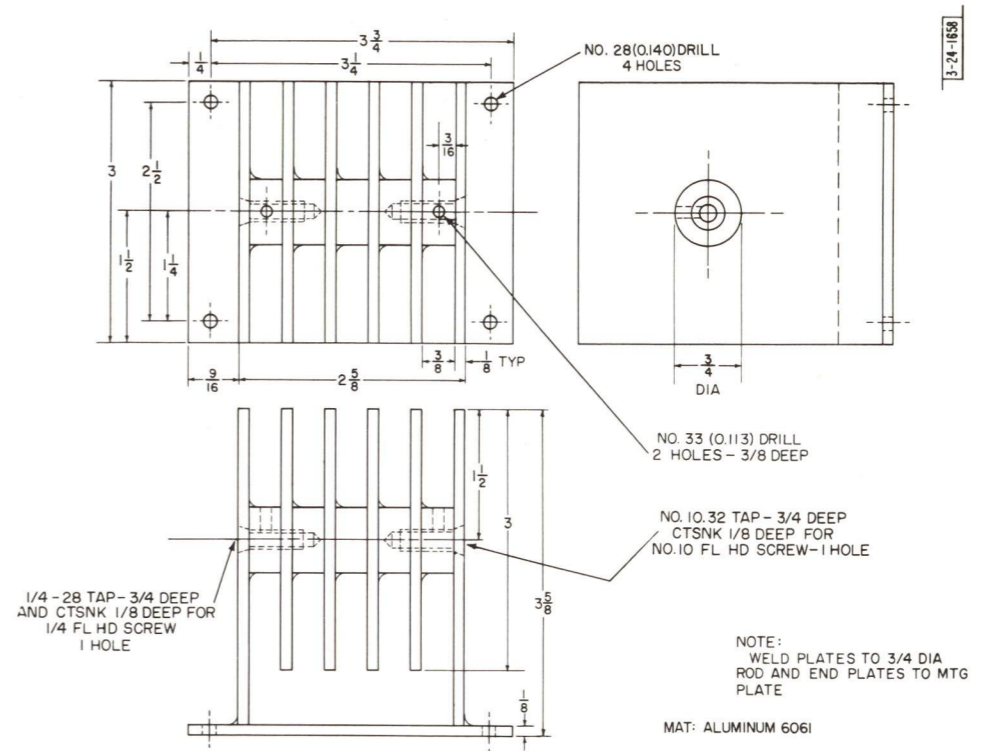


Fig.9. Heat dissipator.



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LINCOLN LABORATORY

DESIGNING FOR RELIABILITY

N. H. TAYLOR

DIVISION 6

9 DECEMBER 1955

TECHNICAL REPORT NO. 102

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MASSACHUSETTS INSTITUTE OF TECHNOLOGY  
LINCOLN LABORATORY

DESIGNING FOR RELIABILITY

N. H. Taylor

Division 6

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Technical Report No. 102

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FOREWORD

The material in this report highlights the work on reliability of digital computer technology at the Digital Computer Laboratory and Division 6 of Lincoln Laboratory from 1948 to 1956. The report reflects the work of so many Staff members that it is, in fact, a joint effort of the whole Division.

In the preparation of this report, particular contributions are those of R. L. Best in the section on Basic Circuit Criteria and Marginal Checking Techniques, and W. J. Canty in typical tube computer circuitry. Transistor Circuitry was contributed by K. H. Olsen and his section. The Transistor as a component has been reported by Dr. D. J. Eckl. The component work has been reported by B. B. Paine.

Nolan Jones has carried the burden of collecting and clarifying the text. The Publications group of the Laboratory has made many helpful suggestions as to methods of organization and expression.

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ABSTRACT

Lincoln Laboratory has achieved impressive results in the application of the design philosophy described in this report. A typical circuit including its tube has an operating lifetime of over 100,000 hours. A routine maintenance scheme in which the marginal-checking principle is properly exploited can predict failures of over 90 per cent of the total to be expected. System operating efficiency (useful time/total time) over 95 per cent is attainable even in systems where 20,000 circuits are employed.

The achievement of reliability is a goal that must be pursued from the very beginning of the system design project. The first step is to consider each individual component to be used in the system and to critically analyze its capabilities and limitations. The second step in the design project is to determine the applications of these components that tend to take advantage of the best capabilities of these components and avoid their worst limitations. This report lists analyses of components and the resulting component applications that have been made by the staff of Lincoln Laboratory over a period of several years.

The third and final phase of the design project is the actual electronic circuit design, based on the component analyses and applications notes derived earlier and predicated on the achievement of high reliability. The thorough design method developed by Lincoln Laboratory is described in detail. This method provides reasonable component tolerances and adequate safety margins, and incorporates marginal checking throughout the design process.

The method is illustrated in a detailed example of a high-speed vacuum-tube flip-flop. Additional tube and transistor basic building-block circuits are described and discussed in the last section of this report. These basic circuits have been used in the assembly of large data-processing systems in the laboratory.

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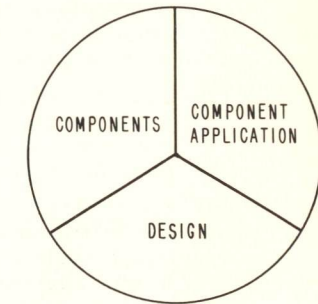
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## DESIGNING FOR RELIABILITY

## I. INTRODUCTION

In approaching the problem of reliability in control systems, the concept changes considerably from the commonly accepted rules of the radio, television, and home appliance field. In the area of automatic control, the system under control is often a very costly one. It places a premium on its controlling parts; and, in military operations, human life itself is sometimes dependent on the reliability of the controlling electronics.

With such a target of reliability, the electronic designer is faced with a design requirement more stringent than he usually faces, and is forced to make every design decision with reliability as his prime objective. He no longer designs a system and then, as an afterthought, "makes it reliable." He must "design for reliability" from the start, even changing the systems concept, if necessary, to insure the desired result.



Reliability is an evasive goal. It depends on three major factors each of which is dependent on the others. Failure to consider any of these usually results in an inadequate system. The diagram to the right illustrates the three vulnerable areas - components, component application, and design - that contribute to reliability.

Components

The choice of components can certainly have a first-order effect on system reliability. Two factors in component manufacture must be considered:

Component Stability:- Components are never absolutely stable. They drift in value with time, temperature, humidity and altitude. Stability factors must be known and considered before design work is undertaken.

Component Reproducibility:- This is a factor of production tolerances. The 1% resistor is now common, but the tube with 1% tolerance in plate current has never been built. Tolerances must be known to the circuit designer and taken into account before design work is started.

Component Application

The way in which a component is used - taking into consideration the problems of stability and reproducibility - is the second major factor contributing to reliability. In this area it is difficult to resort to the explicit scientific approach; the matter is one of judgment and is therefore subject to controversy. The successful system is one where components are used in applications that suit their characteristics. Ideally, the natural properties of the component are exploited and its inherent weaknesses are avoided or bypassed by careful design.

Design Considerations

The design of a specific circuit can be faced after the component problems and the application or use of the components have been considered. Of the three factors in reliability, the design phase is the more difficult, because it must encompass the decisions and account for the boundary conditions imposed by the other two factors.



## II. COMPONENTS AND CIRCUIT DESIGN

A. Component Applications

A good method of appraising a particular application of a component is an evaluation based on the four types of failures that are most troublesome. These are: deterioration, sudden failures, intermittents, and maladjustments.

- (1) Deterioration:- Deterioration is a disease that the designer must face. Man seldom makes anything that does not deteriorate; almost everything we manufacture wears out. In fact, any component more than a hundred years old is rare. Thus, one must ask: "How fast is this component going to wear out in this application?" This question, while not always easy to answer, must be faced squarely.
- (2) Sudden Failures:- Sudden failure needs no description. A vacuum tube losing its vacuum, a resistor opening up, a fuse blowing - these are complete, sudden failures. How susceptible is a component to this type of failure? How often will it happen? What are the consequences?
- (3) Intermittent Failures:- These are the hard ones. It has been said, "If you really know how to get rid of the intermittents, all the other failures in the system are easy to find and easy to fix." Present electronic design is now approaching a point where this is indeed the case; means are available for coping with almost all types of failures except intermittents. Against these latter, safeguards must be provided. Eventually, intermittents must be designed out of the components wherever possible.
- (4) Maladjustments:- These failures are related to proper maintenance. The best possible solution is to create a design that does not require adjustments. This, of course, is not always possible, but attention must be given to which adjustments should be allowed and which procedures should be followed. If maladjustment of a system is possible, it is usually a factor contributing to poor reliability.

A good example of a component application that stands up well under the conditions described above is the memory core in a magnetic memory plane.

- (1) The component deteriorates slowly; in fact, present data indicate practically no change in characteristics with time.
- (2) Sudden failures are rare, limited to broken cores and usually occurring only in assembly.
- (3) Intermittents are rare; adequate insulation on the wires through the cores is all that is required.
- (4) No adjustments are necessary.

In addition, cores are stable with respect to temperature and humidity, and are reproducible to close tolerances.

It is obvious that the core memory itself is not useful without driving and sensing circuits. However these auxiliary circuits cannot be made as reliable as the cores themselves. (As it happens, magnetic-core storage units have run for weeks and even months with complete freedom from error. They are presently the most reliable part of high-speed computers.)

Although, as shown by this example, a core approaches the ideal as a component, 1955 techniques do not allow systems - particularly those with requirements of high-speed arithmetic units, cathode-ray-tube displays, and associated controls - to be built entirely from cores. Accordingly,

the designer is faced with the choice and use of many other components that are more subject to deterioration, intermittents, sudden failures, maladjustments, instability, and limitations in reproducibility. The following list\* suggests an order of vulnerability, with the most vulnerable components at the head of the list:

- (1) Vacuum Tubes,
- (2) Diodes,
- (3) Connectors,
- (4) Relays,
- (5) Resistors,
- (6) Condensers,
- (7) Transformers,
- (8) Inductors,
- (9) Cores,

A reliability program must reach back to the actual design and fabrication of the components listed above. An examination of life-test results and equipment-failure reports will yield data on the particular faults to be expected.

The individual characteristics of tubes and other components as these affect reliability are discussed in detail in Appendix A, and notes on applications of these components are also included there. Transistors are treated, briefly, in Appendix B.

B. Circuit Design1. Safety Margins

The electronic designer has been several decades behind designers in other engineering activities in providing safety margins adequate to allow for the various disturbances that may occur in a circuit during its lifetime. Designers of bridges and power stations habitually allow safety factors of 400 to 600 per cent; the systems they are designing must withstand excessive strain, and failure may result in loss of human life or expenditure of large sums. However, the electronic designer has not, until recently, been confronted with the possibility of such catastrophic consequences if his circuit should fail under stress. The increasing use of electronic controls in larger and more critical areas forces the circuit engineer to pay greater attention to incorporating safety margins in his designs.

When the circuit engineer is confronted with a design problem, he is usually asked to make a circuit perform some specific function as a portion of a system. In the computer field, such a requirement may be for a high-speed switch; the designer may be given, as performance specifications, the limits on the speed of switching, the voltage swing that such a switch should deliver, the resolution time, and perhaps some power limitation. Whether or not reliability and long life are included in these specifications, the circuit engineer must design with these goals in mind. He cannot foist unrealistic demands for tolerances and stability on the component

\*Transistors have not been included since there is not the backlog of use of the other elements in this list. On the basis of present units, they probably rank either above or below diodes.



engineer - specifying 1% resistors and tubes with close tolerances on plate current and trans-conductance - and then glibly say, "My circuit will be as reliable as the components." It is the circuit designer who must know about component stability and tolerances, and who must build his design around such knowledge.

Thus the problem that really confronts the circuit designer becomes one of designing highly reliable and stable circuitry made up of components that are neither reproducible nor stable, but subject to deterioration, intermittents, maladjustment and sudden failure.

## 2. Design Criteria

With recognition of the importance of including adequate safety margins in his design, the circuit engineer must answer certain questions regarding the component tolerances of his circuit. How much tolerance should be expected? How does the designer make provision for deviation in the components? Three criteria listed below are suggested as effective guides for the circuit designer.

- (1) The circuit must meet its performance specifications with all components\* at their worst initial tolerances, and with any component at its worst end-of-life tolerance.

By "worst" is meant deviation of the components in whatever direction is least favorable for the circuit. Usually, several worst combinations of components must be evaluated.

The initial tolerance of a component is that to be expected when it is new; the end-of-life tolerance is wider. For example, the initial tolerance on a composition resistor might be  $\pm 5\%$ , and end-of-life  $\pm 15\%$ . The numbers to use for these tolerances must be the result of a component study, as discussed in Appendix A.

In some simple circuits, it might be possible to have all components deteriorate to end-of-life at once, and still have satisfactory performance; this capability is desirable only if it requires no increase in circuit complexity. To make all circuits continue to meet their specifications when all components are at end-of-life would, in general, require the addition of more components and an increase in circuit complexity. More components result in a greater probability of intermittents; the increased complexity results in more difficult servicing. Statistically, one of a group of components will reach end-of-life while most of the others are still good; therefore, criterion (1) above is suggested as being a good engineering compromise in the search for circuit longevity.

When a circuit geometry has been found that shows promise of meeting (1) above, criteria (2) and (3) must be considered and met.

- (2) The circuit must be able to withstand the loss of any one of the supply voltages in itself or in any circuit connected to its input or output without component damage.

\*"Components," as used above, include power-supply voltages, diode characteristics, tube characteristics, resistors, etc. - anything that can change to the detriment of circuit performance.

When diode logic is used, criterion (2) will usually necessitate use of protection diodes to prevent excessive back voltages.

- (3) Since all components (especially vacuum tubes) degenerate with life, circuit design should include means for detecting significant changes in component values during use of the circuit, and soon enough to insure replacement of the component before failure occurs.

Provision of means for detecting deterioration allows near-failures of components to be discovered and eliminated during routine, scheduled maintenance periods. Costly, unscheduled downtime can be minimized. Slow deterioration of tubes and other components may be observed over a period of time, and replacement can be predicted and even scheduled.

Criteria (2) and (3) make it necessary to have two different specifications on the components, one for normal use and the other for low-duty-cycle marginal checking or emergency conditions. For example, if a resistor has a normal allowed dissipation of one-half the manufacturer's rating, its marginal checking or emergency dissipation might be equal to the manufacturer's rating.

This section has touched briefly on the underlying principles of a basic design philosophy to achieve electronic reliability. The following section will describe the application of this philosophy in a method for checking circuits. Special emphasis will be given the application of this method in the design phase to ascertain if the design will meet performance specifications.



### III. MARGINAL CHECKING

#### A. Introduction

To determine whether or not a circuit design meets the given performance specifications with the desired reliability, there is need for a method of evaluation that will:

- (1) Make graphically clear, in an explicit quantitative way, what tolerance a given circuit has to variations in its components.
- (2) Provide a method, usable in the later systems phase, of preventive maintenance that will adequately cope with the problems of component deterioration.

Such a method – called "marginal checking" – was developed by Lincoln Laboratory; it has been extensively used in the design phases of large real-time control systems, as well as in day-by-day operation of such systems.

This section discusses the use of marginal checking in the design phase. The allowable variation of a component is determined as a function of a selected circuit parameter, usually a supply voltage. This measures the margins of circuit performance in terms of the marginal-checking parameter.

In practice, the tolerance of one of the components in the circuit is plotted against the variation in this marginal-checking parameter, as illustrated in Fig. 1. The intersection of mean-value

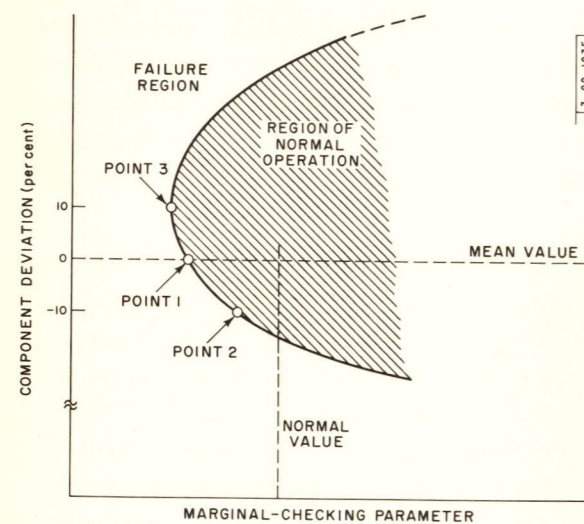


Fig. 1. Locus of failure points in a typical circuit.

and normal marginal-checking parameter lines near the center of the parabola indicates the operating point of the circuit – normal voltage on the circuit and normal value of the components. By considering the supply voltage as the marginal-checking parameter and lowering it, a point is plotted on the contour line where the circuit fails to perform. This failure can be defined as the point at which the function of the circuit deviates from that prescribed in the specification. In an oscillator, for instance, the point at which the frequency shifts out of tolerance can be considered failure; in a flip-flop, the point at which some standard pulse fails to switch the position may be failure. Changing the tolerance on the component by some factor such as 10 per cent in a negative direction and again varying the marginal-checking voltage will result in a different failure point, such as Point 2 on the curve. Raising the tolerance of the component 10 per cent, another failure point, Point 3, can be plotted. Continuing this study, a contour line representing the locus of the failure point of the circuit to tolerance in componentry, as a function of some marginal-checking parameter, can be drawn enclosing an area of reliable operation. This sort of study often results in finding that the contour is not symmetrical about the operating point, and that wide safety margins occur on one side but very narrow margins occur on the other.

It is interesting to note that such contours change radically with the type of circuit. In most cases, the contour would be a closed loop if the marginal-checking parameters could be varied far enough without damaging the components.

It is probably evident that plotting the curves and varying each of the components in even a moderately complex circuit represents a rather long and tedious study. However, the reader should remember that the circuits under discussion are to be subjected to all sorts of variations; failure in such circuits may cause losses of life or of large sums of money. With these factors in mind, the designer can hardly afford to be ignorant of how much margin a circuit has before it will fail. The acceptability of the circuit to the system can be based only on such knowledge.

#### B. Marginal Checking – Components

The application of marginal-checking procedures to components involves a variety of techniques which can be tailored for the particular problem at hand. Several of these are described in subsequent pages.

The discussion in the introduction to this section assumed a one-dimensional tolerance plot; whereas, of course, in reality there are many dimensions that vary simultaneously. Therefore, and because of the nonlinear relationships involved, numerous experiments are needed in most cases to verify the initial paper studies.

Ideally, one would like to plot a curve for each component of the circuit, with the component's deviation from nominal value on one axis and the marginal-checking parameter on the other, resulting in points on the curve that represent the boundary between satisfactory and unsatisfactory operation. To prevent this job from being endless in practice, engineering judgment must be used to determine which data shall be taken. Enough data must be taken so that the effect of change in each component may be deduced.

All the component variations (or branch supply voltages where applicable) must be plotted against the marginal-checking voltage to determine that the required component tolerance is not prohibitive, and that the normal operating point is centered in the area of operation. If a component tolerance turns out to be +1% and -30%, clearly the design is not centered, and a different nominal value for the component is indicated. Common sense indicates that all margins will not be symmetrical. The plate supply voltage of a cathode follower can be lowered only until grid current loads the input circuit too much, but it may be possible to raise it until arc-over occurs. The positive excursion naturally stops where the marginal-checking or emergency component ratings are exceeded.

##### 1. Resistors and Tubes

The effect of change of characteristics in resistors and in tubes may often be determined by varying the supply voltage for individual branches of the circuit, and plotting this branch supply voltage against the marginal-checking voltage to determine the area of satisfactory operation. In the case of resistive voltage dividers, a variation of the supply voltage for the divider may be converted to an equivalent change in the divider resistors.

Consider the direct-coupled amplifier in Fig. 2. The output voltage is a function of the input,  $B+$ ,  $C-$ ,  $R1$ ,  $R2$ , and  $R3$ , so that a change of any one of these parameters will affect the output level.



If the permissible excursion of  $C -$  is determined experimentally (other parameters held fixed), the resulting change in the output level may be calculated. From this change in output, it is possible to calculate the equivalent change in any of the other parameters that would cause this same

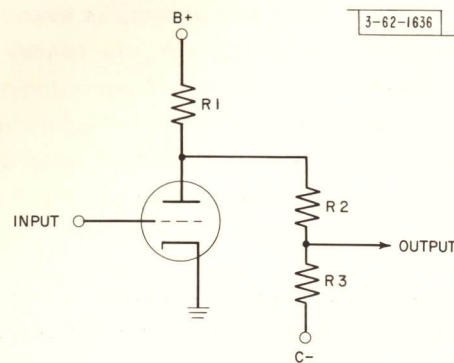


Fig. 2. Direct-coupled amplifier.

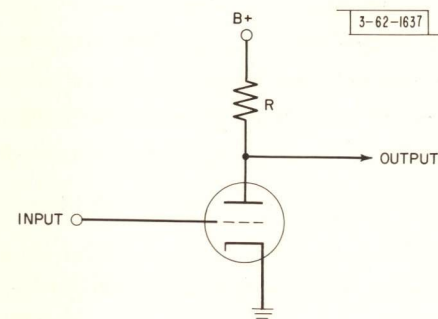


Fig. 3. Plate-loaded amplifier.

limiting change in output level. Using this principle, one set of data can be used to determine the required tolerance of many components.

## 2. The Pentode

The effect of a pentode's losing emission can be simulated by reducing the screen voltage - a drop in screen voltage being equivalent to a drop in available zero-bias plate current. A rise in screen voltage will increase the cut-off voltage required, and is useful for checking the adequacy of the bias provided.

## 3. The Triode

Aging in triodes is much more difficult to simulate. The principle used is to reduce the plate-supply voltage which, in effect, asks the tube to pass the same current at less plate voltage. Consider the circuit in Fig. 3, where the input will be either at ground or cut-off, and the output voltage swing will be dependent on the current the tube draws at zero bias.

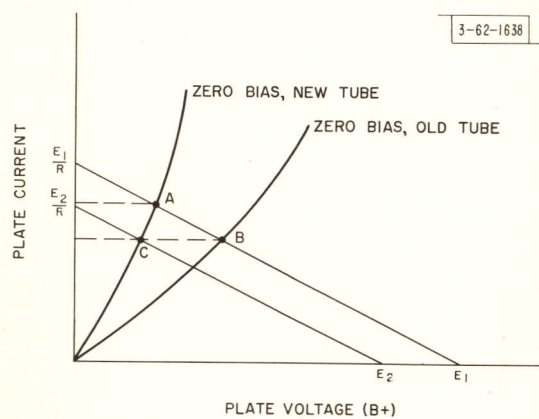


Fig. 4. Load-line chart of circuit of Fig. 3.

The load line is shown in Fig. 4 along with the zero-bias lines for both a new and an end-of-life tube. A new tube would operate at Point A and an end-of-life tube at Point B. An end-of-life tube is not generally available for checking the circuit's operation at this point, so the supply voltage is reduced from  $E_1$  to a voltage  $E_2$  such that with the new tube the operating point shifts to Point C. The output voltage swing for an end-of-life tube with  $B +$  at  $E_1$  is the same as that for a new tube with  $B +$  at  $E_2$ , since the same plate current is switched into the load resistor for each case. This type of analysis may be used to evaluate the supply-voltage variations observed in a circuit,

in order to determine the adequacy of a design. If the magnitude of the supply variation alone were considered in comparing two competing circuits, the circuit chosen might be the one that is the least tolerant of an old tube. An analysis similar to that given above will enable the engineer to make the better choice.

One does not generally have on hand tubes representing a cross section of a given tube type, particularly tubes at the end-of-life portion of the specifications. It is often possible to substitute a different type that will normally have characteristics close to those that would be expected from an end-of-life tube of the type to be used in the circuit. For example, a 6072 or a 12AY7 has approximately the same  $\mu$  as a 5965, but about one-third the zero-bias current. If a 6072 works in circuits designed for 5965's, one knows then that the circuit will tolerate an end-of-life 5965 tube.

## 4. The Semiconductor Diode

In general, diodes may deteriorate in the direction of lower back resistance or higher forward resistance. A diode with low back resistance may be simulated by a shunt resistor across a good diode. High forward resistance may be simulated by series resistors.

## 5. L and C Components

The variations in inductors and capacitors generally must be determined by replacing them with different values or with series-parallel combinations. Every variation that might affect the circuit should be tried.

## C. Marginal Checking - Circuits

To illustrate the application of marginal checking to circuit design, it has seemed worth while to describe the techniques in terms of an example - a high-speed flip-flop designed for use in a large, high-speed digital computer. The complete treatment of this circuit includes performance and component specifications, and an evaluation of the performance, including plots of pertinent margins of operation.

### 1. High-Speed Flip-Flop

The circuit for the high-speed flip-flop is shown in Fig. 5. Its complete specifications follow.

#### a. Performance Specifications

Input: 0.08 to 0.12- $\mu$ sec half-sine wave positive pulses, 20 to 40 volts amplitude, 0 to 2 Mcps prf, set, clear, or complement.

Output: Upper level, +10 to +12.5 volts; lower level, -27 to -30.5 volts. Total transition time, less than 0.5  $\mu$ sec (measured from the beginning of the pulse until the new level is reached), and a delay suitable for counting. (The same pulse is used to complement the flip-flop and to sense a gate tube connected to its output.)

Load That Can Be Driven: 90  $\mu$ mf maximum per output, with a total load of no more than 100  $\mu$ mf.

Marginal Checking: It must be possible to marginal-check the circuit from a remote point so that drift in the components can be detected before they cause failure of the circuit during system use.



b. Component Specifications

**Resistors:** Composition resistors used were nominal 1- and 2-watt size, had no more than 50% of the manufacturer's rated dissipation, an initial tolerance of  $\pm 5\%$ , and an end-of-life tolerance of  $\pm 15\%$ ; no more than 500 volts rms applied. Nominal half-watt composition resistors had no more than 25% of the manufacturer's rated dissipation, an initial tolerance of  $\pm 5\%$  and an end-of-life tolerance of  $\pm 15\%$ , and no more than 350 volts rms applied. Values were restricted to the 5% RMA series.

Precision film resistors had no more than 50% of the manufacturer's rated dissipation, an initial tolerance of  $\pm 1\%$  and an end-of-life tolerance of  $\pm 5\%$ , and no more than 500 volts rms for the nominal 1-watt size or 750 volts rms for the nominal 2-watt size. Values were restricted to the 5% RMA series.

**Capacitors:** Capacitors were ceramic-dielectric,  $\pm 5\%$  initial and  $\pm 15\%$  end-of-life tolerance, 50% of the manufacturer's rated voltage (which is 500), and available in the 10% RMA series from 12  $\mu\text{mf}$  to 330  $\mu\text{mf}$ .

**Pulse Transformers:** A small hermetically sealed canned transformer, designed to pass the standard 0.1  $\mu\text{sec}$  pulses, was used.

**Germanium Diodes:** A special group of diodes was specified. The high points of these specifications follow.

Type W-diode (intended for pulse mixing and clamping): with a low duty factor 0.1- $\mu\text{sec}$  half-sine 50-ma current pulse, the forward drop was not to exceed 3 volts; acceptance back resistance was to be at least 500k between -10 and -50, 100k design value back resistance, except 50k design value for the first 0.5  $\mu\text{sec}$  after applying back voltage; for reverse recovery, after 5 ma forward for 1  $\mu\text{sec}$ , 40 volts reverse was to be applied, through a series resistance of 2k and the back current was to be less than 0.5 ma in 0.3  $\mu\text{sec}$ ; forward current was not to exceed 150 ma peak for 0.1  $\mu\text{sec}$  or 60 ma rms; reverse voltage was not to exceed 60 volts.

Type Y-diode (a less expensive general-purpose diode): at 1 volt forward voltage, the current was to be between 5 and 20 ma; back resistance specification was the same as for Type W above, except reverse current need decay to only 0.8 ma 0.3  $\mu\text{sec}$  after applying back voltage, and forward current was not to exceed 45 ma peak or 16 ma rms.

**Tubes:** Only tubes that are acceptable as reliable types by manufacturers were specified. Triodes were preferred to pentodes since the triode has a simpler structure, and is less prone to intermittent shorts. Twin triodes were preferred over single triodes since fewer tube sockets are needed. Very-high-performance types were avoided due to their inherent close internal spacing and attendant high probability of intermittents.

**Power supplies:** Only centralized power supplies were used; for this system, the voltages available were +250, +150, +90, +10, -15, -30, -150, and -300. All supplies had  $\pm 1\%$  regulation with  $\pm 1\%$  additional due to line drops, giving a total specification of  $\pm 2\%$ . The end-of-life figure used was  $\pm 5\%$ .

c. Circuit Description

The feature of the circuit of the high-speed flip-flop (Fig. 5) is low-performance triodes with cathode followers isolating the plates from both the external load and the capacitance of the opposite grid. The relatively high-speed circuit with the low-performance tube types meets the requirement of using reliable tubes. The plate circuits are clamped through diodes to both +10 and -30, stabilizing both the output swing and the signal transmitted to the opposite grid. This feature makes the circuit less sensitive to variations in plate current of the triodes. The bias return of one grid divider is the marginal-checking point; this is moved above and below its nominal voltage of -150 to determine the circuit's margin. This simulates drift in the four voltage-divider resistors directly (R 7 through R 10).

d. Performance Data

Figures 6 and 7 define the performance of the flip-flop for system timing analysis. Figure 6 shows output and input waveforms; the time taken for the output to reach -15 is of interest since that is the level required to cut off a gate tube (described later). Figure 7 shows the maximum amount of capacitance and/or AND current\* that the flip-flop can handle and still fall to the indicated voltage level within 0.5  $\mu\text{sec}$ . Rise time is inherently faster than fall time.

Figure 8 shows the minimum complement trigger amplitude plotted against prf for various pulse-widths, and Fig. 9 shows how the minimum complement trigger amplitude varies with prf for different capacitive loads.

e. Reliability Data

Figures 10 through 16 show reliability data, obtained by marginal checking, that indicate the component tolerances and safety margins of the circuit. In these diagrams, "OS" means that the curve represents circuit behavior when the component concerned was on the opposite side of the circuit from which the marginal-checking input was located; "SS" means the same side.

Figure 10 shows how critical voltages in the circuit vary as the tube ages. These data were taken by reducing the filament voltage to simulate the weak tube, a very touchy method. The tube was connected to a 3-pole 2-position switch, switched to a test position until the plate current stabilized, and then switched into the flip-flop circuit; the DC voltages were then measured.

Figure 11 shows the circuit margins plotted against the test plate current of one tube while the other is held fixed. The tube was "aged" by filament variations as described above.

Figure 12 shows circuit margins plotted against the variations of the four voltage-divider resistors, R 7 through R 10. This linear relationship is expected, and could have been obtained analytically.

Figure 13 shows margins plotted against tolerance of the cathode resistor, R 11. A note on the curve explains how it shifts with low-current tubes, so that the apparent unbalance in tolerance is not objectionable.

Figure 14 shows how the margins vary with the plate-load resistors, R 1 and R 2.

\*AND current is current drawn by a load connected to a positive voltage, measured when the flip-flop output is at its lower level.



NOTES:  
UNLESS OTHERWISE SPECIFIED:  
(1) RESISTORS ARE IN OHMS, 1% ± 5%  
(2) V1 & V2 ARE 5965 TUBES

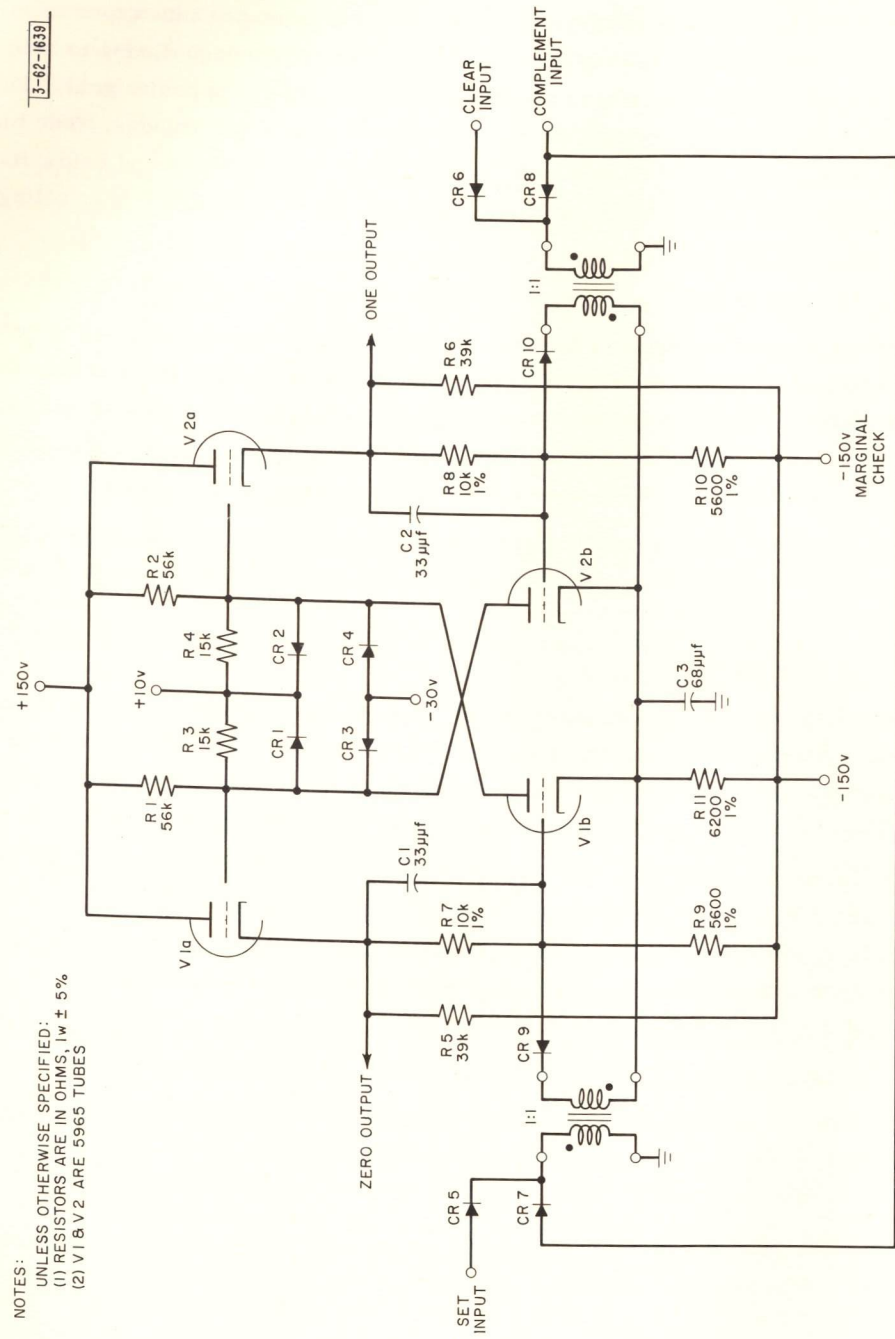
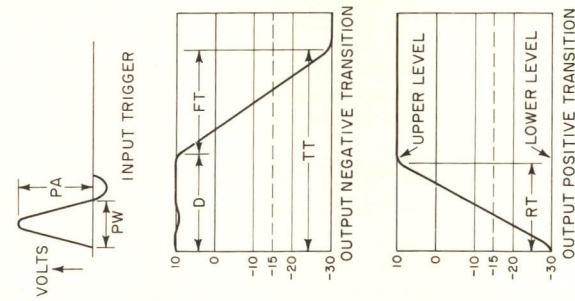


Fig. 5. High-speed flip-flop.



- PA — Pulse Amplitude  
20 v ≤ PA ≤ 40 v
- PW — Pulsewidth  
0.08 μsec ≤ PW ≤ 0.12 μsec
- D — Circuit Delay  
PW ≤ D ≤ 0.20 μsec
- TT — Transition Time from +10 v to -30 v  
TT ≤ 0.5 μsec
- FT — Fall Time  
0.2 μsec ≤ FT ≤ 0.3 μsec
- RT — Rise Time  
0.2 μsec ≤ RT ≤ 0.5 μsec

Fig. 6. Output waveforms.

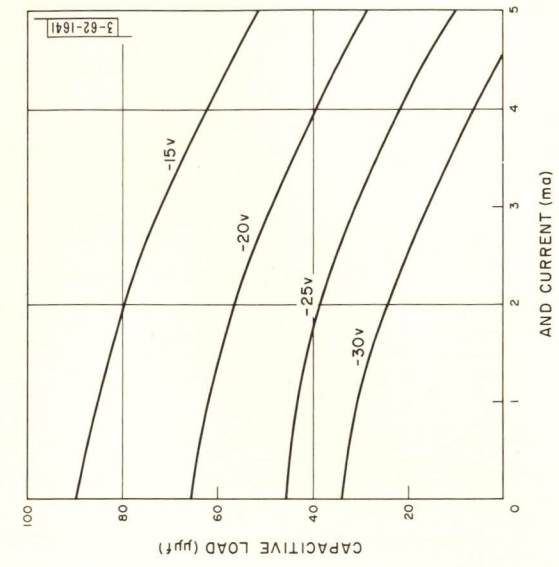


Fig. 7. Maximum load for less than 0.5 μsec fall time.



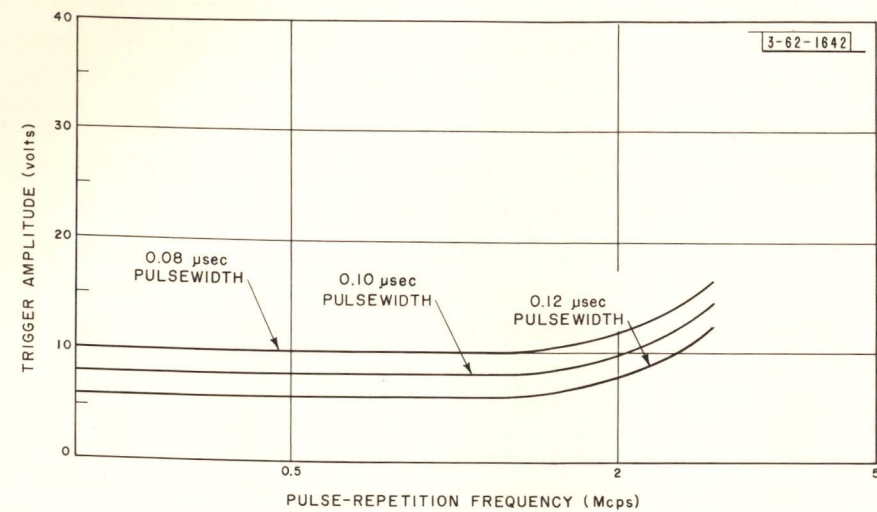


Fig. 8. Pulse-repetition-frequency response characteristics vs pulsewidth.

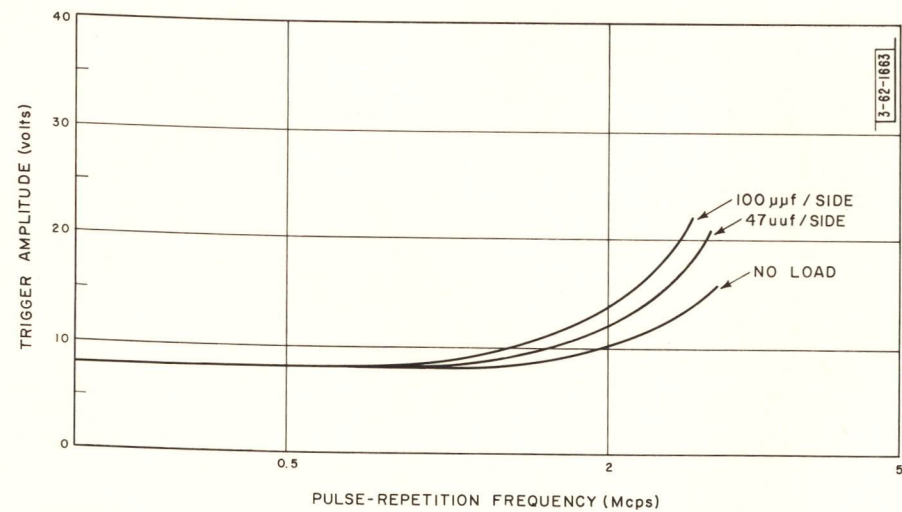


Fig. 9. Pulse-repetition-frequency response characteristics vs load.

Figure 15 shows the effect on margins of low back resistance in the -30 volt clamp diodes, CR 3 and CR 4.

Figure 16 shows margins as a function of trigger amplitude. This plot is the most useful one for optimizing the final circuit, especially when the data are taken for both low and high (2-Mcps) prf's, maximum and minimum loads, unbalanced tubes, etc.

Other data were taken to show margins vs the back resistance of the trigger diodes (CR 9 and CR 10), cathode-follower plate voltage, memory capacitors (C 1 and C 2), cathode by-pass capacitor (C 3), forward drop of input diodes (CR 5 through CR 8), etc.

The detailed analysis illustrated in this example gives the circuit designer quantitative figures for component tolerances and safety margins in his circuit. Using this information, the designer can extrapolate the effect of simultaneous change in several components. Only through such detailed analyses can the circuit engineer meet his design requirements for highly reliable electronic circuitry.

A large electronic system is made up of a number of basic circuits of which the high-speed flip-flop is one such circuit. Each of these basic circuits must be designed with the same thoroughness with respect to its performance, component tolerances and safety margins.

In the next section, several other basic circuits are described. However, to avoid unnecessary repetition, these treatments do not cover all the details of the analyses that were included in the example of the high-speed flip-flop. Only the most important features of these basic circuits are illustrated in the diagrams and discussed in the text for each of these circuits.

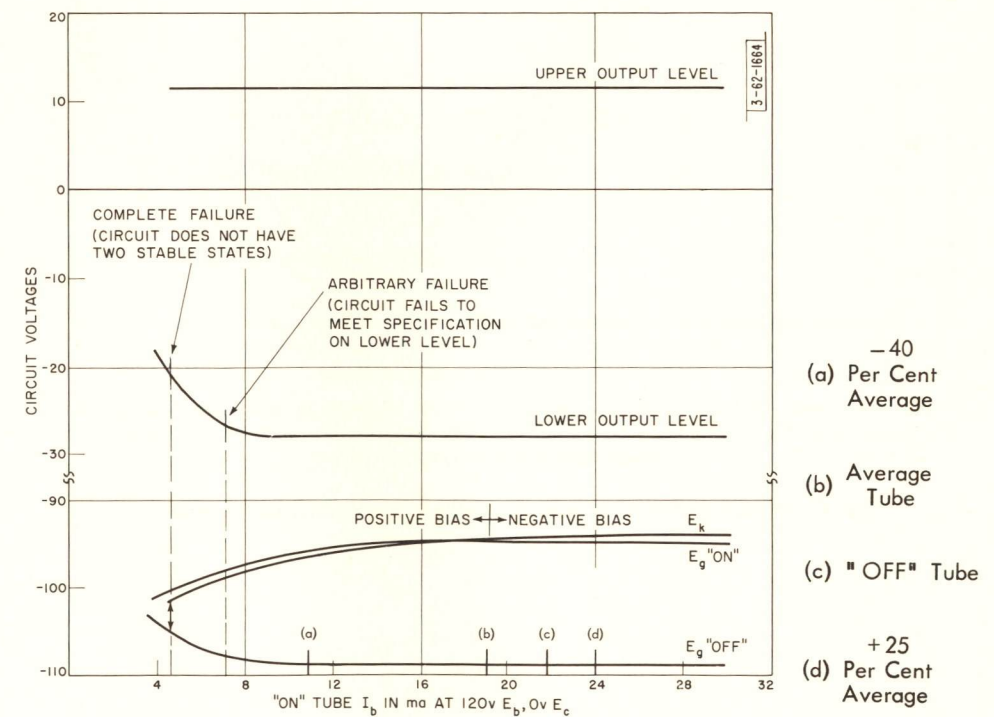


Fig. 10. Circuit voltages vs tube characteristics.



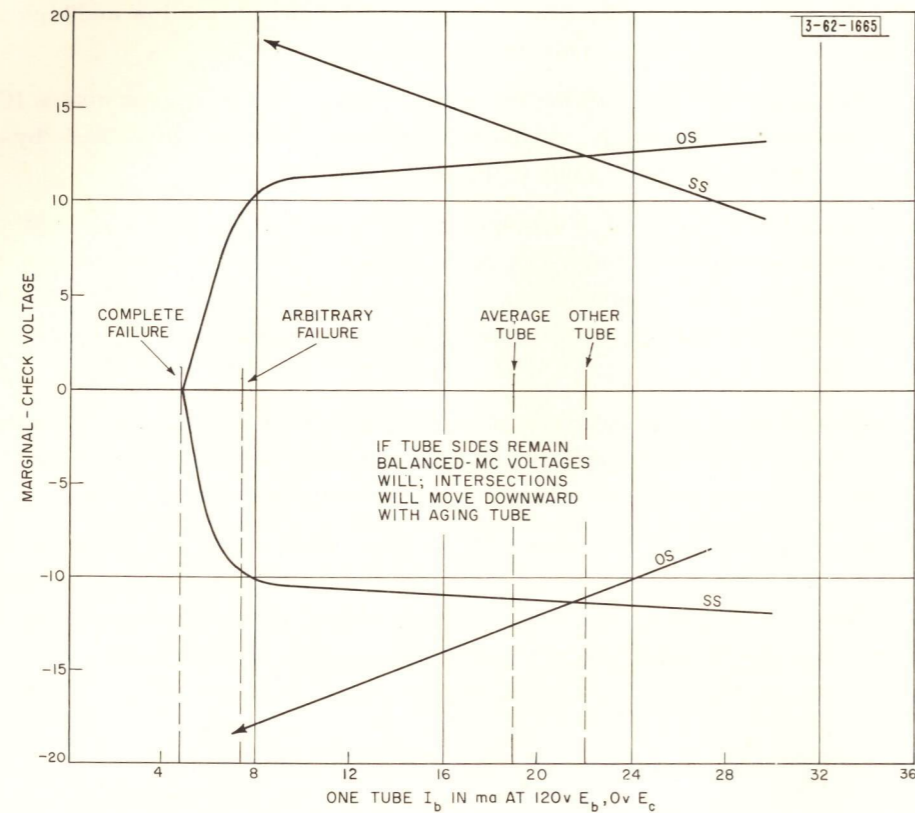


Fig. 11. Marginal-check voltages vs tube characteristics.

Notes:

1. Circuits are marginal-checked by varying one of the supply voltages to the circuit. In all these curves the marginal-check scale indicates deviation from the normal value of the marginal-check supply voltage.
2. SS denotes deviation of the marginal-check voltage on the same side of the circuit as the component being checked; OS denotes deviation of the marginal-check voltage on the other side of the circuit.

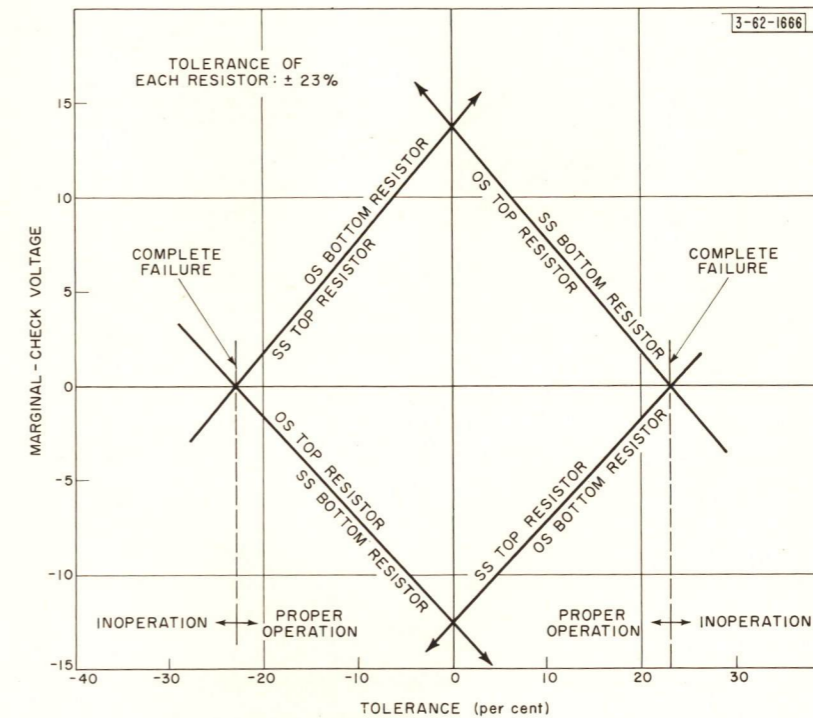


Fig. 12. Marginal-check voltages vs divider-resistor tolerance.



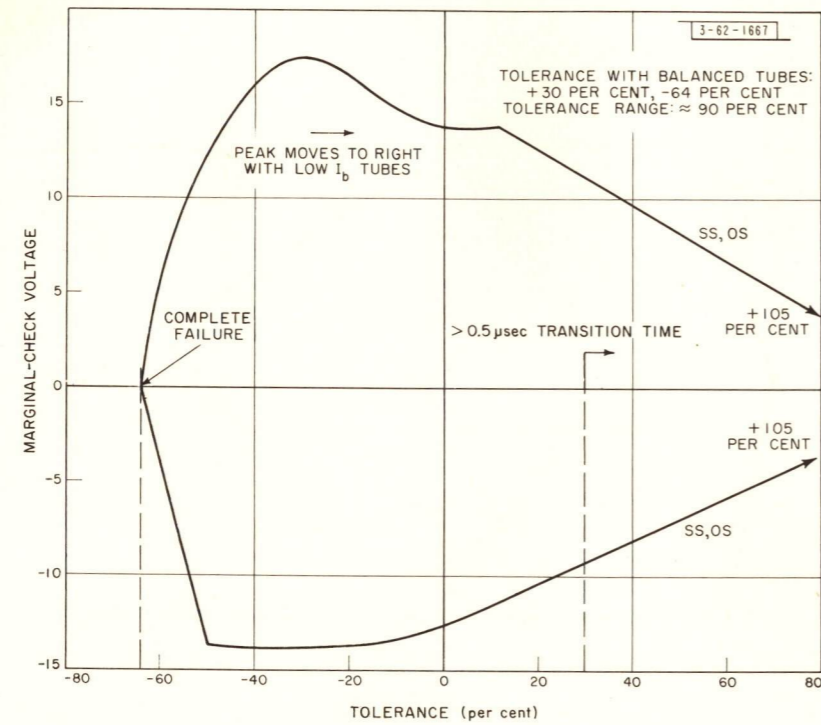


Fig. 13. Marginal-check voltages vs cathode-resistor tolerance.

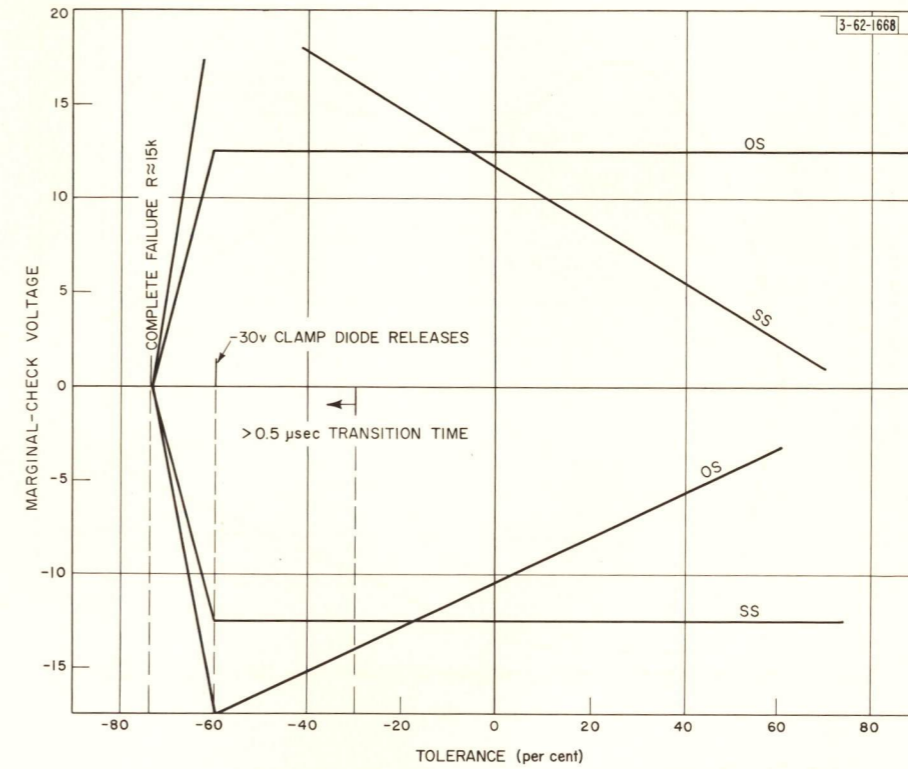


Fig. 14. Marginal-check voltages vs +150v plate-resistor tolerance.



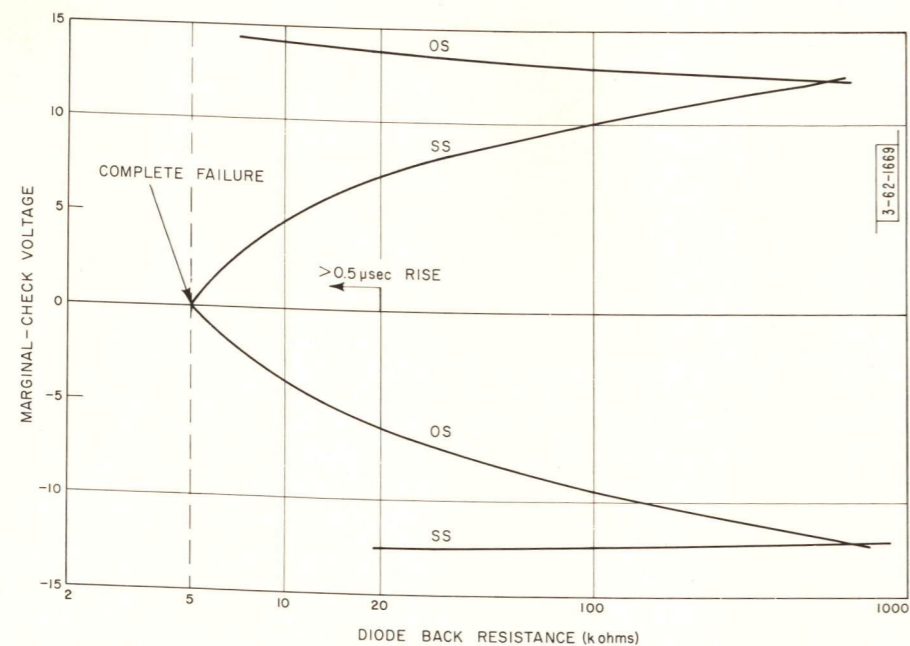


Fig. 15. Marginal-check voltage vs back resistance of -30v clamp diode.

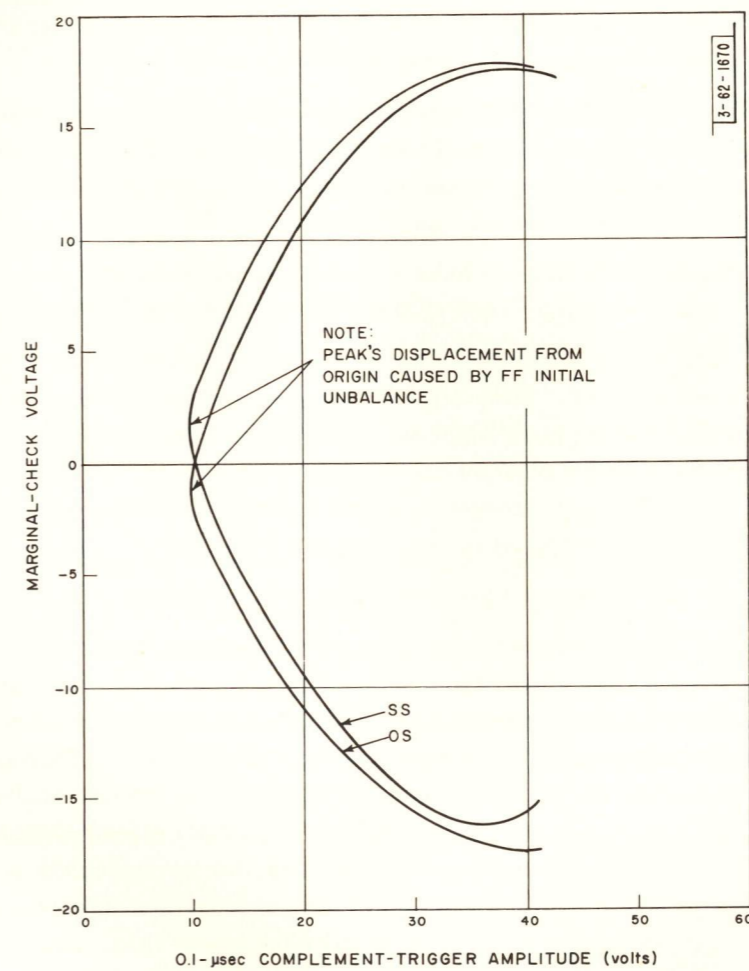


Fig. 16. Marginal-check voltage vs input-trigger amplitude.



## IV. RELIABLE COMPUTER CIRCUITS

A group of typical and compatible computer circuits is presented to illustrate applications of design philosophy expounded in earlier sections of this report. Each of the tube circuits was designed with the same care and study as the high speed flip-flop example of the previous section. The design of the transistor circuits has been slightly less rigorous because of the newness of the transistor. In general, the treatment of these basic circuits is brief.

The group of circuits includes Pulse Sources, Pulse Amplifiers, Logical Gate Circuitry, Flip-Flops, Cathode Followers, Indicators and Blocking Oscillators. These basic units can be interconnected to perform most logical functions. Together with a memory system, this circuitry is adequate for reliable high-speed computer applications.

In a large system, signal levels must, whenever possible, conform with a standard to make possible the interconnection of circuits, such as those listed below, in building-block fashion.

The use of a set of centralized DC power supplies in a large system offers many advantages over the use of several small supplies. With only one set of supplies to build, it is advantageous to devote a sizable effort to making good supplies. Greater potential reliability accrues from the use of fewer components. Trouble-detection equipment (such as low-voltage and overvoltage detectors), control circuitry, and emergency-supply switch gear is far less extensive than the composite of analogous equipment used for many smaller supplies.

## A. Vacuum-Tube and Associated Semiconductor Diode Circuits

The circuits to be described are designed to operate in a system using positive, nominally half-sinusoid (between triangular and square) pulses between 0.08 and 0.12  $\mu\text{sec}$  duration, and between 20 and 40 volts in amplitude, as standard control pulses. The prf can be between 0 and 2 Mcps. Figure 17 shows such a standard 0.1- $\mu\text{sec}$  pulse. Circuits such as flip-flops generate outputs at +10 v or -30 v DC levels, and are designed to be triggered by standard 0.1- $\mu\text{sec}$  pulses. Gate-tube circuits used as AND gates are designed for standard 0.1- $\mu\text{sec}$  pulse inputs to control grids and for levels to the suppressor grids of more positive than +10 v (for selection) or more negative than -15 v (for nonselection). Since the flip-flops generate +10 v and -30 v and the gate tubes require only +10 v and -15 v, the signal level from the flip-flop may be allowed to climb and be attenuated through cathode followers and diode logic on its way to a gate tube, without the necessity for restandardization of the level.

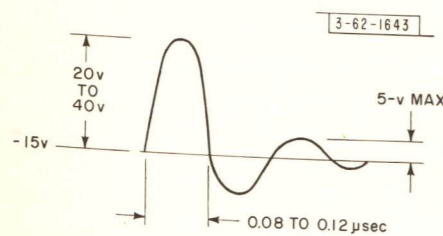


Fig. 17. Standard pulse.

Whenever possible, gate tubes and pulse amplifiers are designed to have less than unity gain with pulse inputs of less than 5 volts; greater than unity gain but less than 40 volts output for inputs between 20 and 25 volts; and, for inputs of from 25 to 40 volts, to have outputs of 25 to 40 volts (see Fig. 18). This transfer characteristic creates a tendency towards standardization of pulse amplitudes, alleviating the need for restandardization of pulses traveling through chains of gate tubes and pulse amplifiers. Marginal-checking facilities are included in each circuit to aid in detection of failing or deteriorating components.

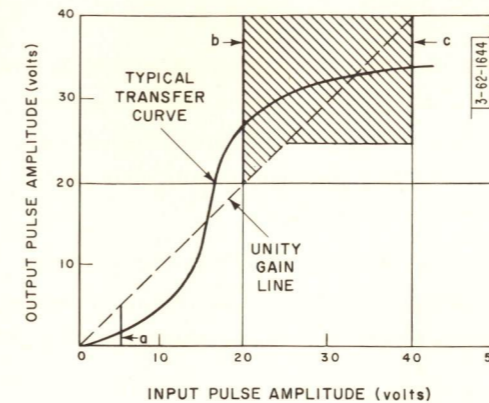


Fig. 18. Transfer characteristics. Specifications require that the transfer curve intersect vertical lines a, b and c. Shading indicates normal operating region.

The circuits described here have been designed to operate from centralized power supplies with outputs of -300, -150, -30, -15, +10, +90, +150, and +250 volts. Particular attention has been paid to decoupling of supply voltages to prevent interaction between circuits.

## 1. Pulse Source

The circuit of Fig. 19 is a typical clock-pulse (standard 0.1  $\mu\text{sec}$ ) generator. This circuit is designed to supply 0.1  $\mu\text{sec}$  pulses into a 93-ohm load at a 2-Mcps rate. The 2-Mcps sine-wave output from the first stage is clipped in Stage 2 and amplified (now as 2-Mcps pulses), and re-clipped and standardized in Stage 3. The ability of Stage 3, and circuits like it, to standardize pulses to 0.1- $\mu\text{sec}$  width is described in succeeding paragraphs.

Marginal checking of each stage is accomplished by decreasing screen-grid voltage and sensing the output for failure.

## 2. Pulse Amplifiers

In many computer applications, relatively large loads (long lines or many stages) must be driven, requiring the use of pulse amplifiers.

Two typical pulse amplifiers are shown in Figs. 20 and 23. The general-purpose pulse amplifier of Fig. 20 has an output relatively independent of load and input voltage when load resistance is greater than 91 ohms and input greater than 20 volts. Figure 21 shows the transfer characteristics of this circuit for various loads. Partial amplitude "standardization" of output pulses is accomplished by "plate bottoming," whereas width standardization is accomplished by the characteristics of the pulse transformer. Pulswidth standardization by this type of circuit is illustrated by Fig. 22 which shows the relationship between input pulse (width and amplitude) and output pulswidth. It should be noted from the transfer characteristics (Fig. 21), that this circuit performs standardization well for a load resistance of 91 ohms and above.

The input capacitor C1 is large enough to cause negligible loss of the input signal in spite of the grid current. L1 presents a high shunt impedance to the input source and low impedance to DC, and R1 critically damps the circuit. Since the pulses are generated by a transformer, the area of the pulse equals the area of the overshoot, and therefore they may be passed through such an AC-coupling circuit with no shift in relative baseline. The 4:1 pulse transformer matches the high-impedance plate circuit to a 91-ohm load. At this impedance level, pulses can be efficiently carried through coaxial cables.

The applications where greater pulse amplitudes are desired (such as driving long lines) or where larger loads must be driven, the high-power pulse amplifier of Fig. 23 is used. None of the transfer curves (Fig. 24) of this amplifier satisfy the standard transfer-characteristic illustrated in Fig. 18. However, this high-power pulse amplifier ordinarily drives large numbers of gate tubes



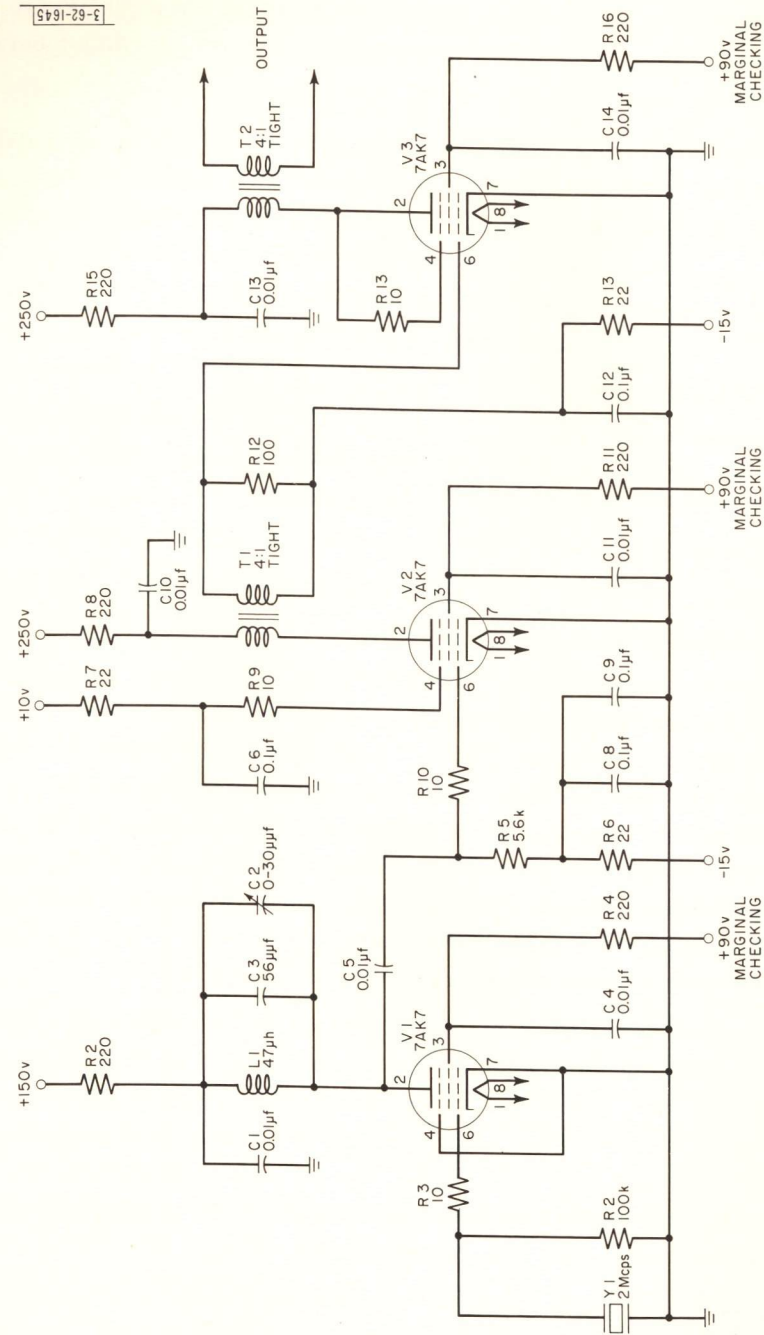


Fig. 19. Clock-pulse generator.

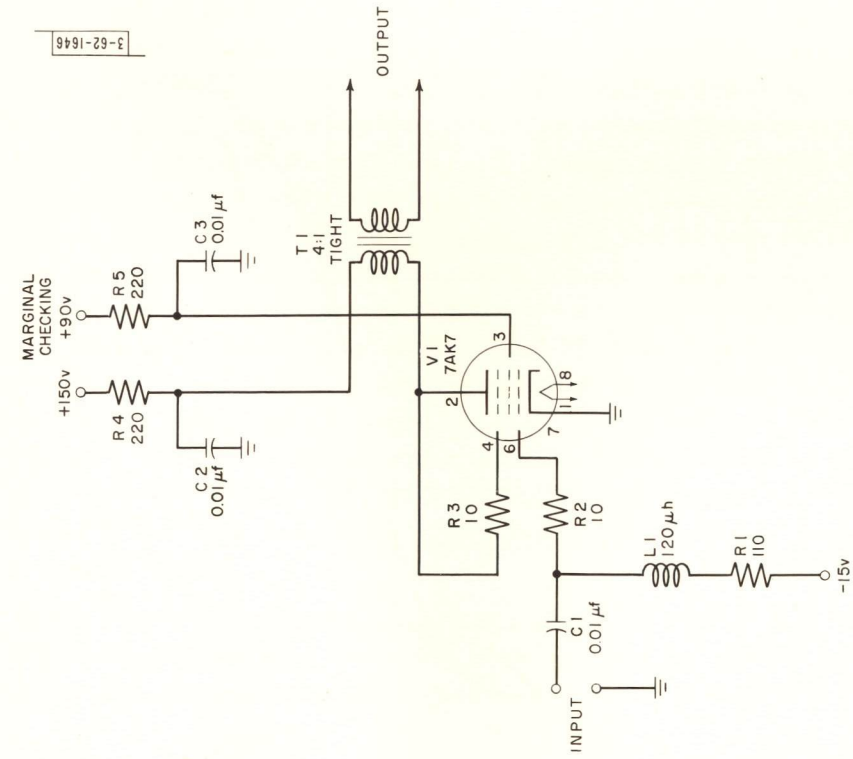


Fig. 20. General-purpose pulse amplifier.

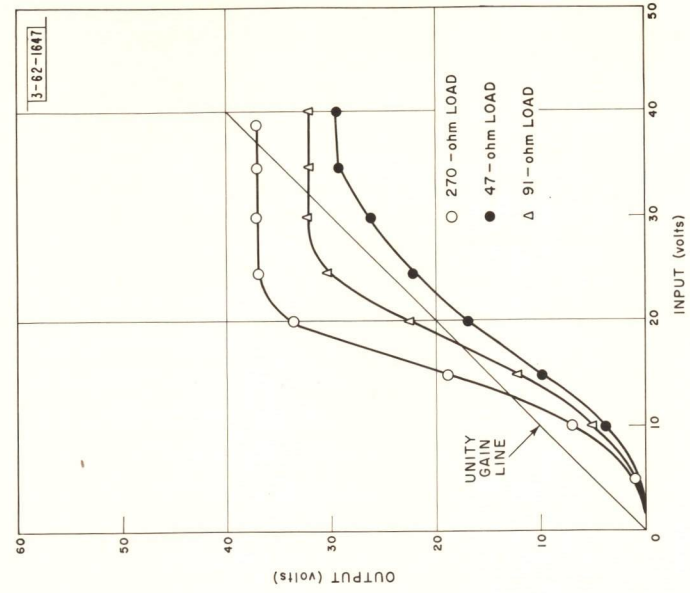


Fig. 21. Transfer characteristics, general-purpose pulse amplifier.

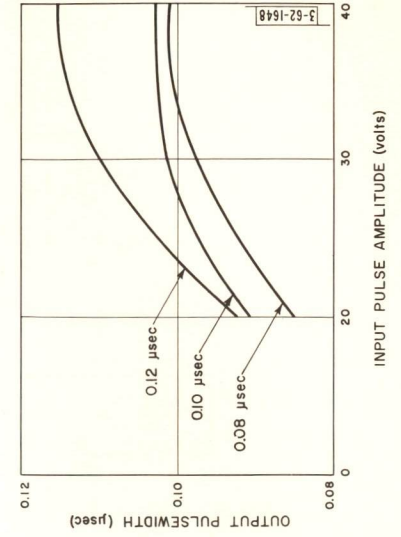


Fig. 22. Relationship between input and output pulse widths for typical pulse amplifier.



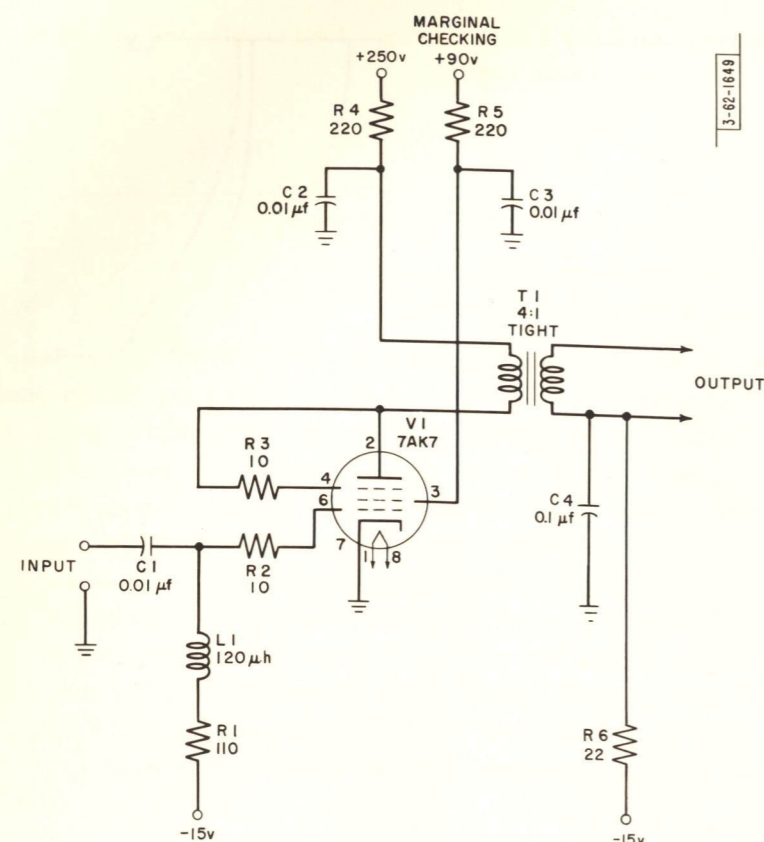


Fig. 23. High-power pulse amplifier.

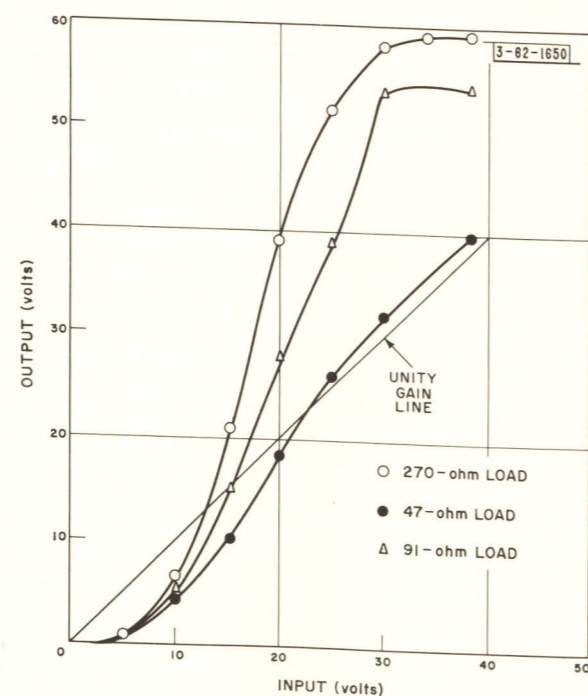


Fig. 24. Transfer characteristics, high-power pulse amplifier.

or pulse amplifiers, which represent very nonlinear loads; this type load enables the circuit to meet the standard transfer-characteristic requirement easily.

### 3. Gate Circuits

#### a. Vacuum-Tube Gate

The circuit for a gate tube is shown in Fig. 25. Inputs to this circuit are:

G1: 0.1- $\mu$ sec pulses, 20 to 40 v amplitude.

G3: +10 v for selection, -15 v for nonselection.

This gate-tube circuit, like the pulse-amplifier circuits mentioned above, is capable of partially standardizing pulses. Standardization of pulse amplitude is not so good as in the general-purpose amplifier, as can be seen from the transfer characteristics for this circuit (Fig. 26). Selection in the gate tube is accomplished by applying a voltage greater than +10 at the suppressor-grid input. Nonselection (that is, prevention of pulses applied to control grid from "getting through" to the plate circuit) is accomplished by applying a voltage more negative than -15 v to the suppressor grid. By using +10 as the selection voltage, enough power can be delivered from the gate-tube circuit to drive 4 flip-flops, or 4 gate tubes, or any combinations of these, without intermediate buffering. Under applications of light load to the gate tubes, the output of gates should be resistance-loaded to give pulses of standard amplitudes. Marginal checking of the circuit is accomplished by varying the screen voltage: a drop in screen voltage makes the tube look older, and a rise in screen voltage detects dangerously high noise pulses at its input.

#### b. Diode-Capacitor Gate

A passive-element pulse gating circuit is shown in Fig. 27(a). Whereas the setup time of a vacuum-tube gate is determined only by the transition time of its suppressor-grid input, the diode-capacitor circuit setup time (assuming a step-function selection input) is determined by the charging time of the capacitor, C1. If there is to be no feed-through of pulses when the selection input is at -30 v, care must be exercised to keep input pulses always below 40 v in amplitude. This can be achieved by always driving sets of diode-capacitor gates with the general-purpose pulse amplifier mentioned earlier. Since no pulse regeneration or partial standardization takes place within this type of gating circuit, long chains of these gates are not practical except when they are broken up by pulse amplifiers. In Fig. 27, L1 is chosen to give a high impedance to 0.1- $\mu$ sec pulses to isolate the pulse source from shunt capacitance of a possible long lead between R1 and L1. R1 is large enough to isolate the source for the selection input (usually a flip-flop) from the same shunt capacitance, as well as from C1. At the same time, R1 must be small enough to charge C1 in the time required and to drive the minimum back resistance of the diode. C1 is large enough to prevent loss of pulse amplitude, but small enough to allow reasonable values for R1.

An alternate termination for the gate is shown in Fig. 27(b). L2, R2, and the stray capacitance comprise a damped RLC circuit that reshapes the pulse. The resulting pulse is then AC-coupled to the grid, where a clamp diode is used to establish a baseline.



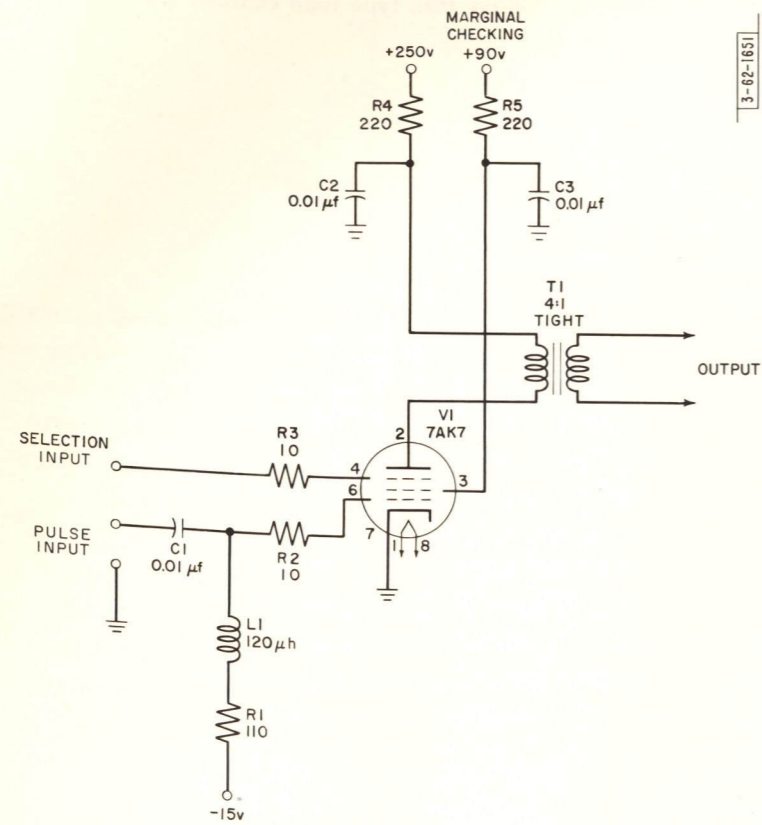


Fig. 25. Gate-tube circuit.

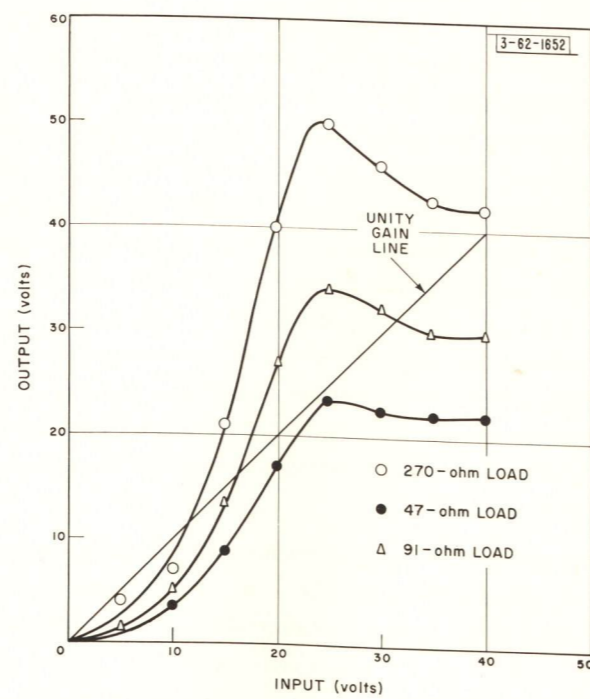


Fig. 26. Transfer characteristics, gate tube.

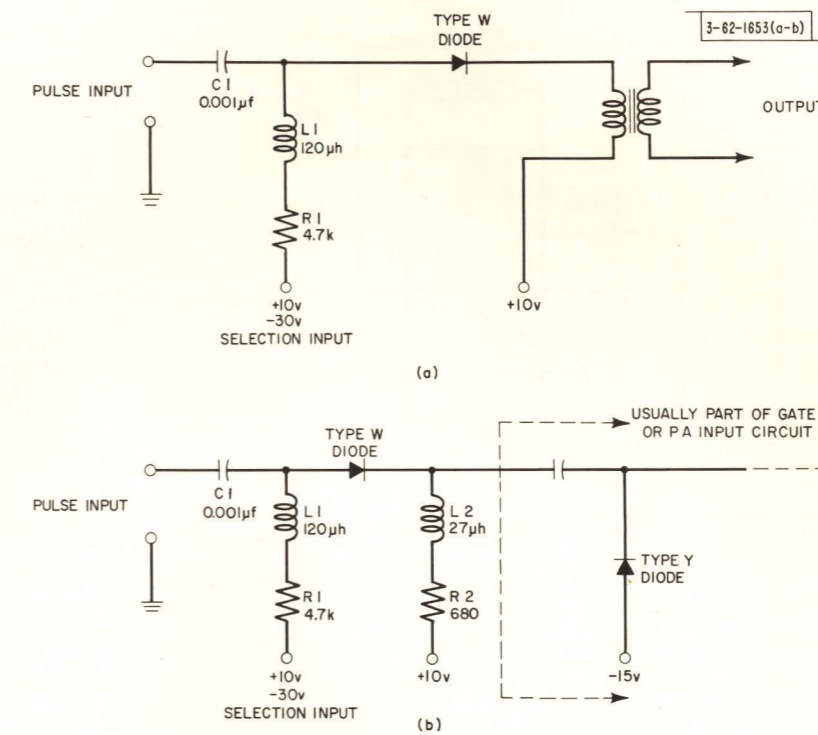


Fig. 27. Diode capacitor gate circuits.



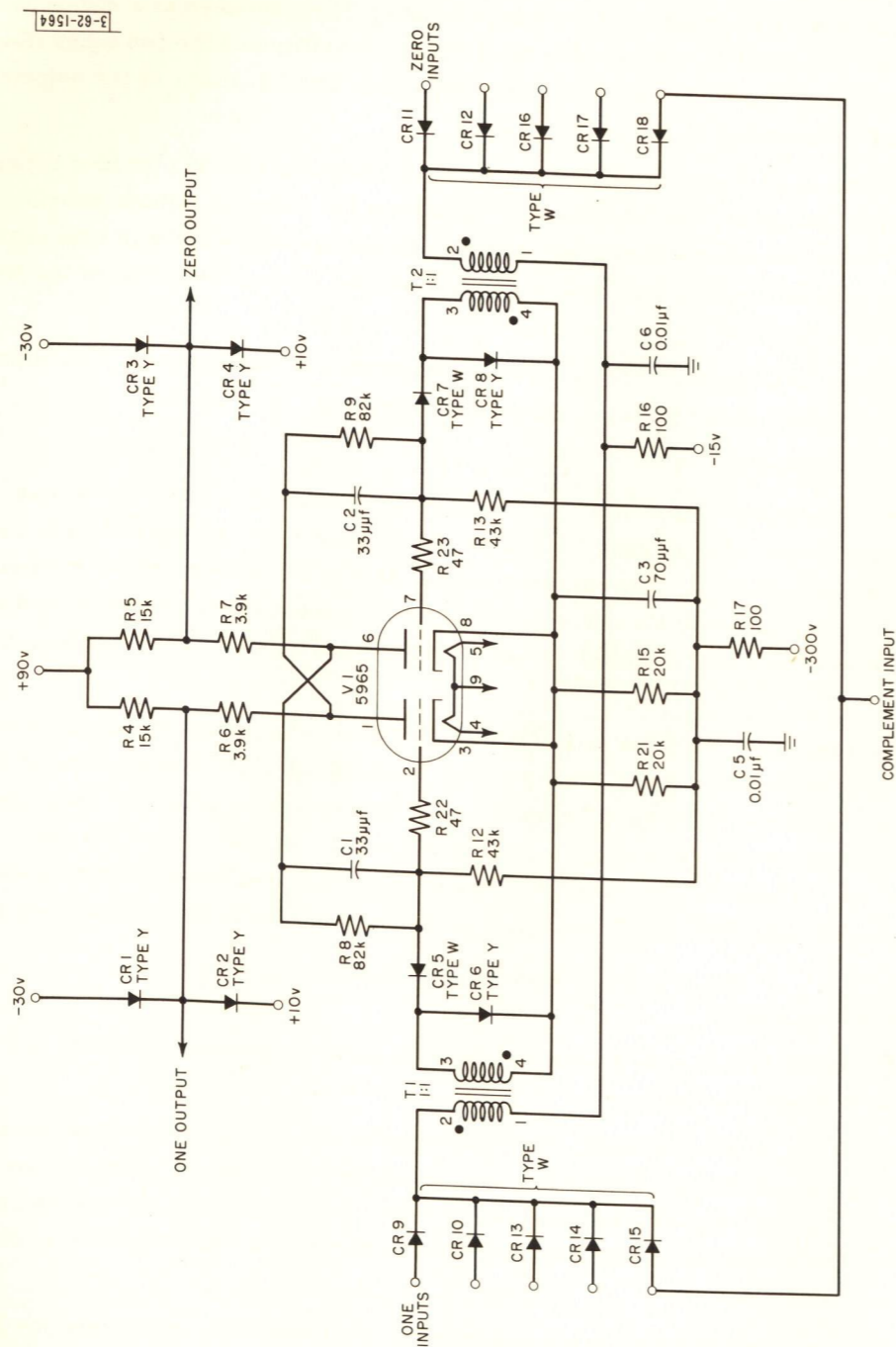


Fig. 28. Low-speed flip-flop.

#### 4. Low-Speed Flip-Flop

In many applications, where compactness is desirable and high speed is unnecessary, a flip-flop such as that shown in Fig. 28 finds use. It is capable of being complemented at a 200-kcps rate, and has one tube (two cathodes) as compared to the 2-Mcps capability and the two tubes (four cathodes) of the high speed flip-flop described in Sec. III. Rise and fall times of the outputs are on the order of 5  $\mu$ sec (depending on the load).

Basically, this flip-flop is an Eccles-Jordan circuit. A DC-coupling path is provided between each plate and the opposite grid. The 10,000-ohm resistor in the common cathode provides a large amount of DC degeneration and thus stabilizes the circuit against changes in tube characteristics. A 70- $\mu$ mf cathode condenser stabilizes cathode voltage during transition of the flip-flop from one state to another.

The circuit is capable of driving up to 320  $\mu$ mf of load capacitance on each output. Transformers are provided at each input to invert pulses for flip-flop triggering.

#### 5. Cathode Followers

The limited load-driving capabilities of most flip-flops restrict loading to little more than a few gate tubes or their equivalent. Diode logic (if it is at all extensive) or long coaxial lines require the use of flip-flop output buffering. The cathode follower of Fig. 29 is adequate for moderate loads. (Naturally, little can be said about rise and fall times without specification of loading impedance.) Variations of this circuit could include paralleling of this circuit for driving heavier loads.

For applications involving heavy loads or where cathode-follower bias build-up must be kept to a minimum, the circuit of Fig. 30 is used. It features a feedback circuit. Comparison of input and output levels and amplification of the difference signal takes place in Stage 1. Unity gain can be achieved by attenuating the feedback signal. With an input rise or fall time of 0.3  $\mu$ sec, output rise or fall time will be 0.7  $\mu$ sec for the nominal +10 v to -30 v signal. Power output capabilities of this circuit may be increased by paralleling other sections of 5998's to the present half-section of 5998.

#### 6. Flip-Flop Indicators

Indicator neon lamps on flip-flops serve a useful purpose in general systems operation and are particularly valuable in trouble-shooting.

The indicator circuit of Fig. 31 is often used. The operation of this circuit depends on the difference between the outputs of the flip-flop to fire the appropriate neon lamp. The indicators may well be separated from the flip-flop by hundreds of feet. In such a case, the 56k resistors are located in the flip-flop to prevent loading the flip-flop by the interconnecting cable to the neon lamps in a remote indicator unit.

A circuit providing one neon per flip-flop saves space in the indicator unit, since only one lamp is necessary for each flip-flop, and saves cable since only one line is required from each flip-flop to the indicator unit (see Fig. 32). The pulse power supply is an integral part of the indicator



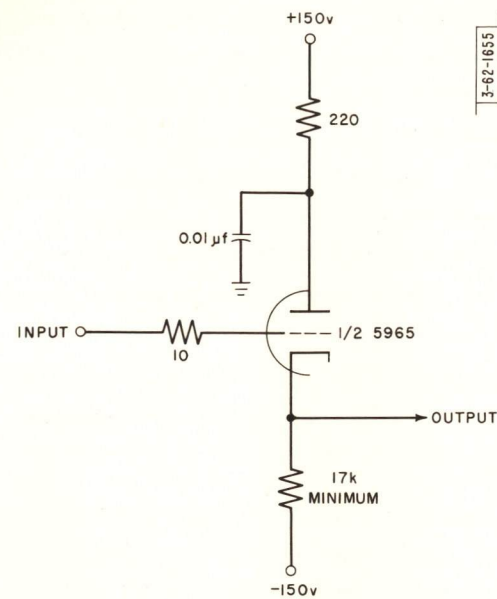


Fig. 29. Cathode follower.

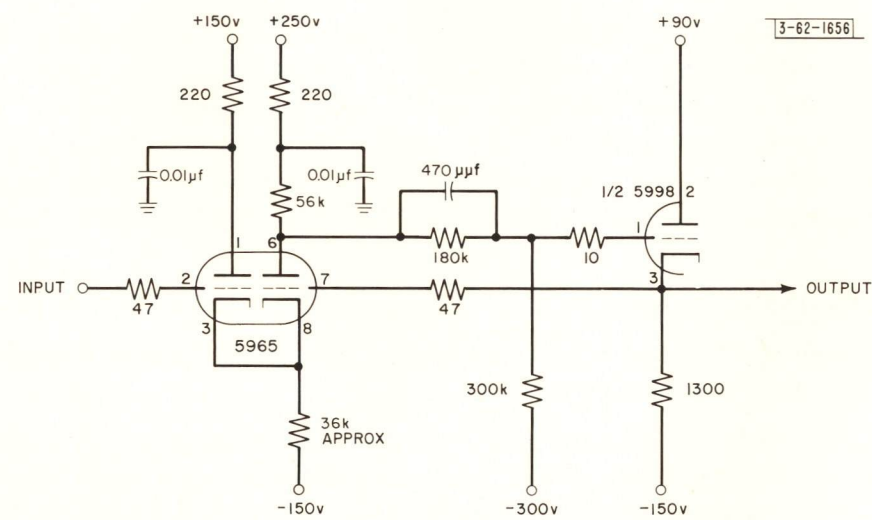


Fig. 30. Power cathode follower.

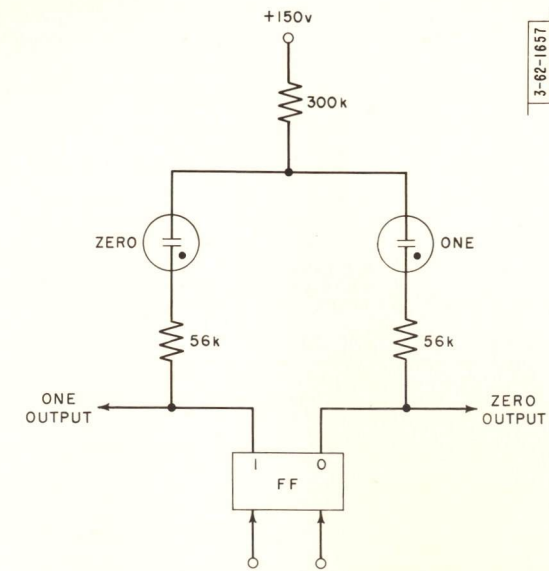


Fig. 31. Twin-neon flip-flop indicator.

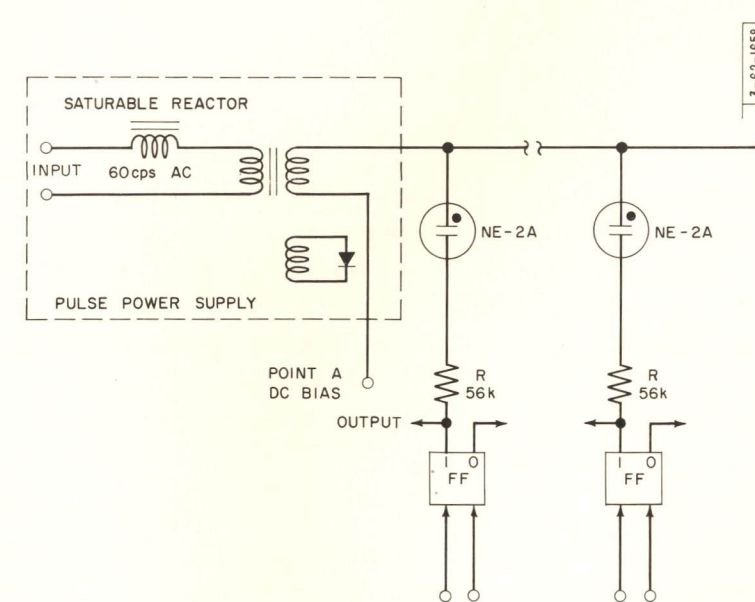


Fig. 32. Single-neon indicator circuit.



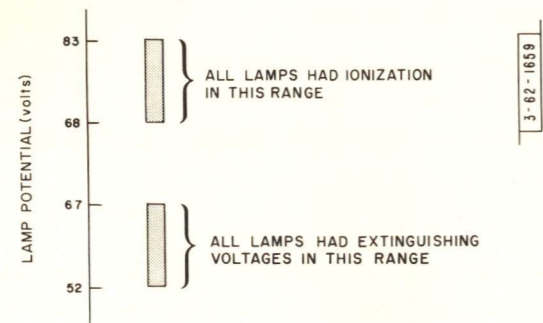


Fig. 33. Summary of measurements on NE-2A.

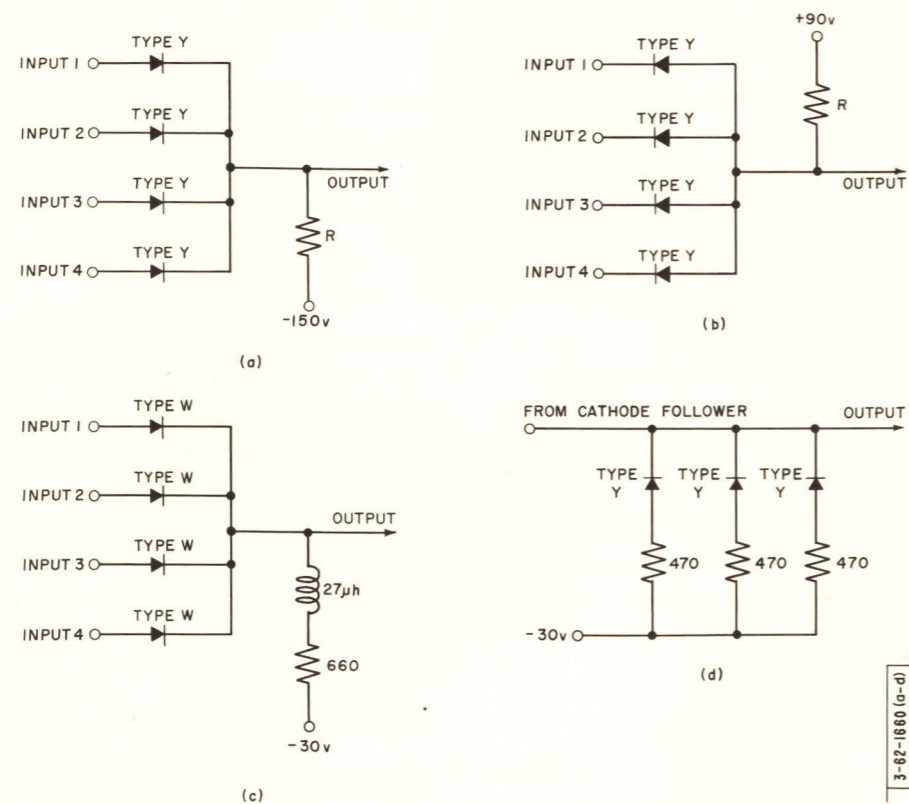


Fig. 34. Diode logic: (a) diode OR circuit; (b) diode AND circuit; (c) pulsed OR circuit; (d) diode protection.

unit assembly. The pulse ignites all neons regardless of the states of the flip-flops. By proper adjustment of the DC bias (Point A in Fig. 32), the neons may be made to remain ignited or to turn off according to the states of the flip-flops.

Recent measurements have shown the ranges of ignition and extinction voltages of a large sample of new and aged NE-2A indicator lamps to be as shown in Fig. 33. The single-neon indicator system of Fig. 32 depends on the fact that a 15-volt change will bring any lamp from conduction to below extinction.

7. Diode Logic

Circuits of nonlinear passive elements such as diodes can perform many of the logical OR and AND functions in computing systems. The circuit of Fig. 34(a) is an OR circuit. Its inputs are mixed such that its output is +10 v if any one of the inputs is at +10. The value of R is chosen to give the circuit adequate fall time. (The smaller the R, the closer the output will follow input fall time.) The circuit of Fig. 34(b) is a diode AND circuit. Output level will be +10 v (as opposed to -30 v) if and only if all inputs are at +10. The choice of R here is governed by the desired rise time of the circuit output.

The circuit of Fig. 34(c) is an OR circuit similar to that of Fig. 34(a). This circuit is designed to mix 0.1-μsec pulses. Although only 4 inputs are shown, any number of inputs (up to the point where back resistance of the diodes loads the driving circuits) can be used. The shape of the leading edge of the output pulse is determined by that of the input, while the shape of the trailing edge is determined by R, L, and the shunt (stray) capacitance. R and L are so chosen that the trailing edge of the pulse returns to the baseline, with no overshoot.

These diode logic circuits are usually driven by cathode followers such as that shown in Fig. 29. If the tube is pulled from its socket in this circuit, the output line would drop to -150 volts, thereby applying a large back voltage to diodes connected to this particular cathode follower. Failure of a tube, removal of a plug-in unit, or loss of certain supply voltages can similarly damage diodes such as those of the circuits of Figs. 34(a) and 34(b). Figure 34(d) shows a protection circuit that prevents the output of the cathode follower from going very much below -30 volts (which is normal back voltage for the diodes in the logic circuits). Enough diode-resistor combinations must be used to clamp the cathode follower output near -30 volts without exceeding the current rating of the protection diodes. The 470-ohm resistors insure equitable current distribution through the diodes.

8. Blocking Oscillators

Blocking oscillators subject tubes to extremely hard usage - for example, high peak cathode current. For this reason, it has not been easy to design blocking-oscillator circuits that are reliable. The circuit of Fig. 35 has been designed to provide near-standard 0.1-μsec pulses from an input waveform of 20 v rise at the minimum rate of 100 volts/μsec. This circuit will operate between 0 and 100 kcps prf. Marginal checking of the circuit is performed by varying the 90 v screen-supply voltage. Degeneration supplied by the load in parallel with R 7 limits cathode current of the 7AK7 to a safe value.



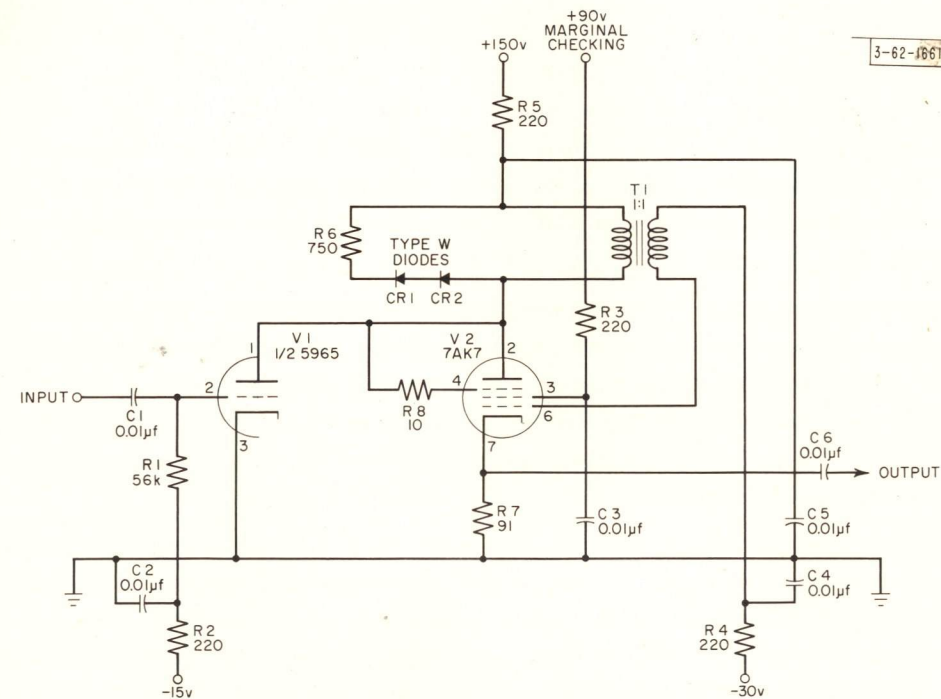


Fig. 35. Blocking oscillator.

## B. Transistor Circuits

The reliability of transistor circuits is affected by basically the same factors that determine reliability in tube circuits. Since the transistor itself is a relatively new component, it is undergoing rapid and continuous improvement. Circuit designers are now learning how to take advantage of the properties of the device in order to emphasize its strong points and to bypass its weaknesses.

Since the transistor resembles the vacuum tube in a number of respects, some of the techniques of tube circuit design are adaptable to transistor circuits. (This parallel must not be carried too far - in no case can a transistor be "plugged" into a circuit in place of a tube and have the circuit operate equally well with either component.) In general, transistor circuits operate at an impedance level an order of magnitude below that of similar tube circuits. This reduces the problem of accidental triggering from external noise but magnifies the problem of driving several parallel stages from a single transistor stage.

### 1. Problem of Transistor Circuit Design

The problems of practical transistor circuit design involve, in order of ease of solution: (a) static operating margins; (b) dynamic operating margins; (c) temperature stability; (d) transient response.

#### a. Static Operating Margins

Design of transistor circuits with large static operating margins follows essentially the same procedures used with tubes. In general, the problem is easier with transistors since power consumption is so low compared to tube circuits that the power efficiency of the resulting network is less critical.

#### b. Dynamic Operating Margins

The achievement of acceptable dynamic margins is aided by the very sharp cutoff characteristics of transistors which may be utilized to fix limits on pulse amplitudes. However, the problem is complicated by the fact that the transistor is a low-input-impedance, high-output-impedance device and, therefore, susceptible to loading effects.

#### c. Temperature Stability

Both the static and dynamic circuit margins are affected by temperature. The current gain and frequency response vary slowly with temperature, but the leakage current has an exponential variation such that it approximately doubles for each 8°C temperature increment.

In general, a large dynamic margin may be designed into the circuitry by taking into consideration the effects of static operating point drift with temperature. Stabilizing devices, such as emitter degeneration resistors and heavy bleeder networks, should be used. The effects of temperature on the frequency response of the input and output networks, as well as on the gain and frequency response of the transistor, must be considered.

#### d. Transient Response

The major adverse influence on circuit transient response results from temperature-induced



transistor impedance variations which load the input network and alter the available "drive" power at the input to the transistor. The causes of temperature variations include both external ambi-ents and internal self-heating caused by power dissipation at the transistor junctions and in the bulk material. Since present-day units have fairly high thermal resistance (0.2 - 0.5°C per mw), the circuit must be designed to guard against the effects of power dissipation.

The group of transistor circuits to be discussed were designed around the high-speed Philco Sur-face Barrier Transistor (SBT). These circuits are intended for use in a system with standard-ized supply voltages of +10 v, -3 v, and -10 v, negative pulses of 3-volt amplitude and 80-millimicrosecond duration, and flip-flop output levels of 0 and -3 volts.

2. High-Speed Flip-Flop Group

The basic flip-flop and its associated circuits are illustrated in Fig. 36. Transistors Q 3 and Q 4 are the flip-flop transistors; Q 1 and Q 2 are input pulse amplifiers for the two sides of the flip-flop; Q 5 and Q 6 are buffer inverter amplifiers; Q 7 - Q 9 and Q 8 - Q 10 are cascode power amplifiers which drive the output lines. This group of circuits is usually constructed on two etched cards, mounted together in one miniature pluggable unit, to minimize lead lengths between the individual circuits.

The circuits are marginal-checked with the two +10 v supply buses as indicated in Fig. 36. The +10 v lines for the individual circuits may be separated if it is desired to marginal-check the cir-cuits independently.

The basic flip-flop is a direct-coupled Eccles-Jordan circuit in which triggering is done with in-put pulse amplifiers in series with the emitters of transistors Q 3 and Q 4, as shown in Fig. 36.

The circuit layout of the flip-flop is similar to the circuit layout of the tube flip-flop of Fig. 28.

The input amplifiers Q 1 and Q 2 are grounded-emitter pulse amplifiers that are normally saturated or turned ON. A positive pulse at the input terminal is coupled to the base of the input amplifier, turning this pulse amplifier OFF. The output is directly coupled from the collectors of the am-plifiers to the emitters of the flip-flop transistors.

The inverters are grounded-emitter amplifiers that serve as buffers between the flip-flop tran-sistors and the output cascode power amplifiers.

The designs of the flip-flop, input amplifier, and inverter are conventional and straightforward transistor circuit design, but the cascode power amplifier is unique. Transistor Q 10 in the zero-side cascode amplifier is basically an emitter follower which drives the zero-output line in the negative direction. Since these are saturating circuits with the inherent difficulties with "hole storage," the rise time of these circuits would deteriorate if these emitter followers were re-quired to drive the output lines in the positive direction as well. Hole storage in the emitter fol-lower and succeeding stages has the same effect on the output rise time as line capacity. Tran-sistor Q 8 serves as a positive driver in this cascode circuit to make it possible to drive greater true or "hole storage" capacity. These cascode power amplifiers work so well that the rise time from 10 to 90 per cent on unloaded output lines is about 20 millimicroseconds, whereas the fall time is about 30 millimicroseconds unloaded.

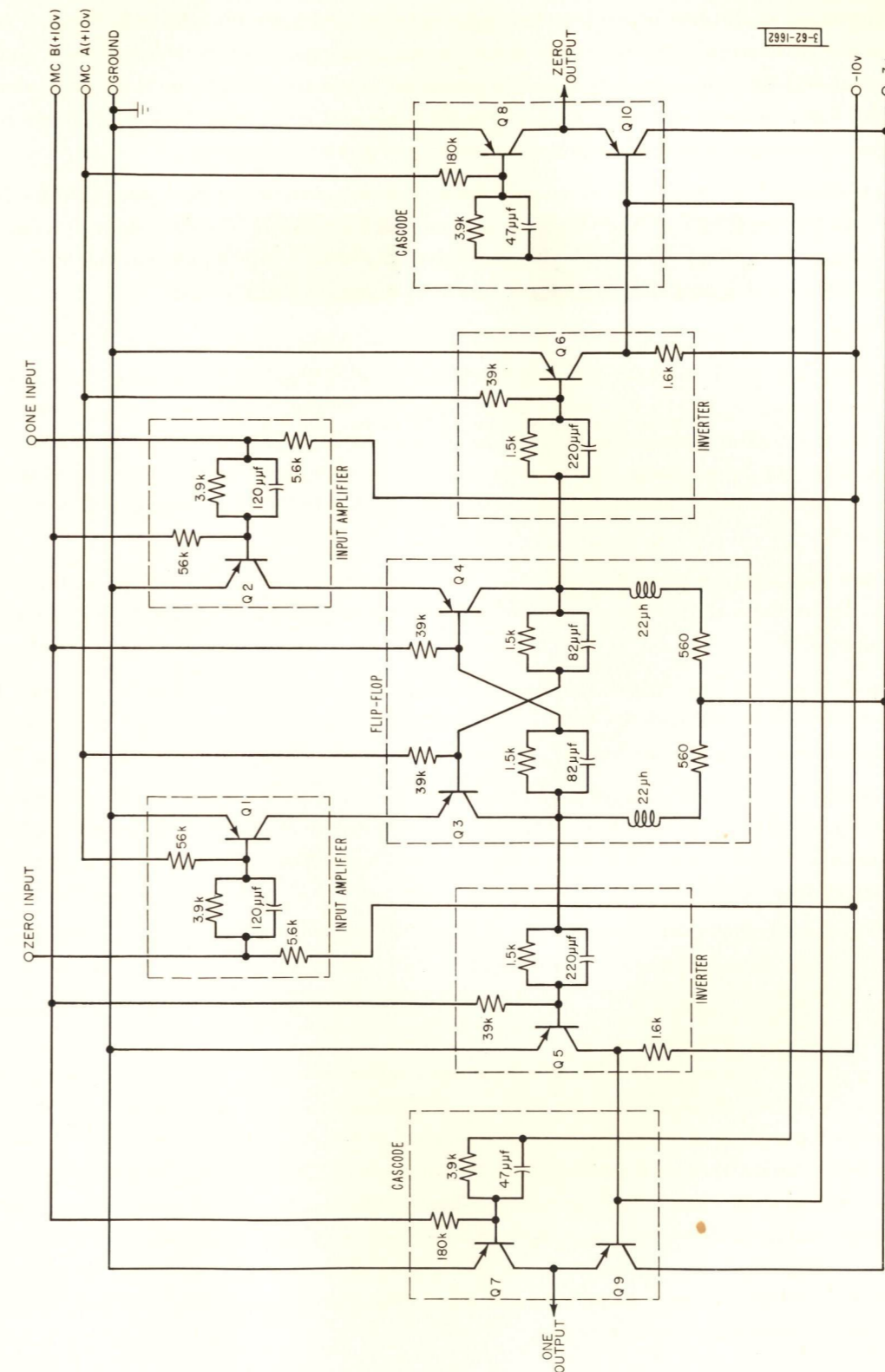


Fig. 36. High-speed transistor flip-flop.



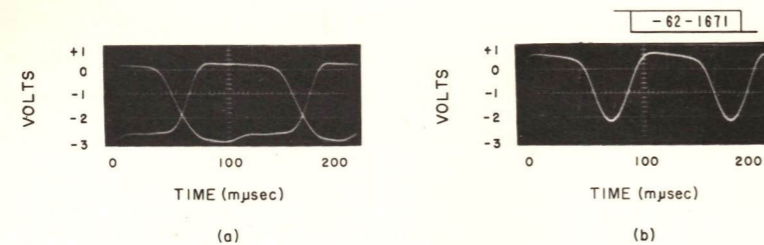


Fig. 37. High-speed flip-flop waveforms; (a) output, (b) trigger input.

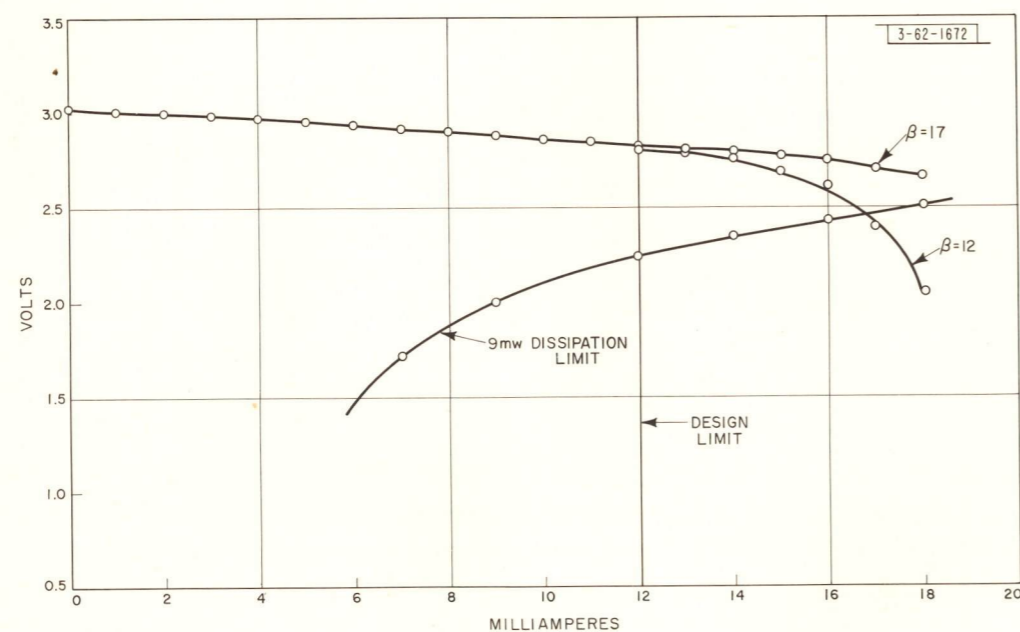


Fig. 38. Cascode DC output characteristic.

Input and output waveforms of the flip-flop group are shown in Fig. 37. Using 50-millisecond trigger pulses as illustrated in the figure, the maximum prf of the flip-flop group is approximately 10 Mcps. Maximum prf and minimum pulsewidths are limited primarily by the lack of ability to generate and handle very narrow pulses. The circuit operates very reliably at the design goal of 5 Mcps prf.

The DC output characteristic of the cascode circuit is shown in Fig. 38. The maximum output current is 16.8 ma at the intersection of the characteristic curve for  $\beta$  near end-of-life and the 9-mw transistor dissipation limit. Design maximum for the output current is 12 ma. The slope of the output characteristic or the internal equivalent resistance of the circuit is about 16 ohms.

The capacity-driving capability of the cascode is shown in Fig. 39. More than 400  $\mu\text{f}$  of output capacity can be driven at a rise time of 0.1  $\mu\text{sec}$ . One cascode can drive up to 8 inverter circuits with a normal amount of interconnecting wiring.

The specifications for these SBT transistors are summarized as follows:

$$I_{CO} = 0.2 \text{ to } 3 \mu\text{a}$$

$$I_{EO} = 0.2 \text{ to } 3 \mu\text{a}$$

$$\begin{array}{l|l} \text{Initial } \alpha > 0.94 & \text{End of life } \alpha = 0.92 \\ \text{or } \beta > 15.6 & \text{or } \beta = 11.5 \end{array}$$

$$V_{\text{max}} (\text{punch-through}) = 6 \text{ to } 20 \text{ volts}$$

$$V_{CE} (\text{saturation}) \leq 0.1 \text{ volt at } I_{\text{base}} = 2.5 \text{ ma } I_C = 8 \text{ ma}$$

$$\tau = 30 \text{ to } 70 \text{ millimicroseconds}$$

The factor  $\tau$  is a measure of hole storage in a standard circuit. A low  $\tau$  indicates low hole storage.

The marginal-checking curves for the flip-flop group are illustrated in Figs. 40, 41, 42 and 43. Variation of the marginal-checking voltage from its nominal +10 v value as a function of input pulse amplitude is shown in Fig. 40. The margins with respect to the output of the -10 v supply are shown in Fig. 41. The margins with respect to the output of the -3 v supply are given in Fig. 42. The margins in pulse amplitude are plotted in Fig. 43 for variations in  $\beta$  and  $\tau$  in one of the basic flip-flop transistors. For normal values, the curve is symmetrical about the marginal-check axis. For either low  $\beta$  or high  $\tau$ , the curve is asymmetrical, thereby indicating variation of these transistor parameters.

### 3. High-Speed Pulse Gate

A pulse-level AND gate for use with the high-speed flip-flop, described above, is shown in Fig. 44. This gate is equivalent in function to the vacuum-tube gate of Fig. 25 in which a pulse input and a level input are gated together. The output of the pulse gate is usually connected directly to one of the inputs to the flip-flop group. The components in these inputs constitute collector load and supply for the pulse gate.



The emitter of transistor Q 2 may be returned directly to ground to make Q 2 a simple pulse amplifier instead of a pulse-level AND gate. The outputs of several such gates and/or such pulse amplifiers may be tied directly together at flip-flop inputs for logical OR functions.

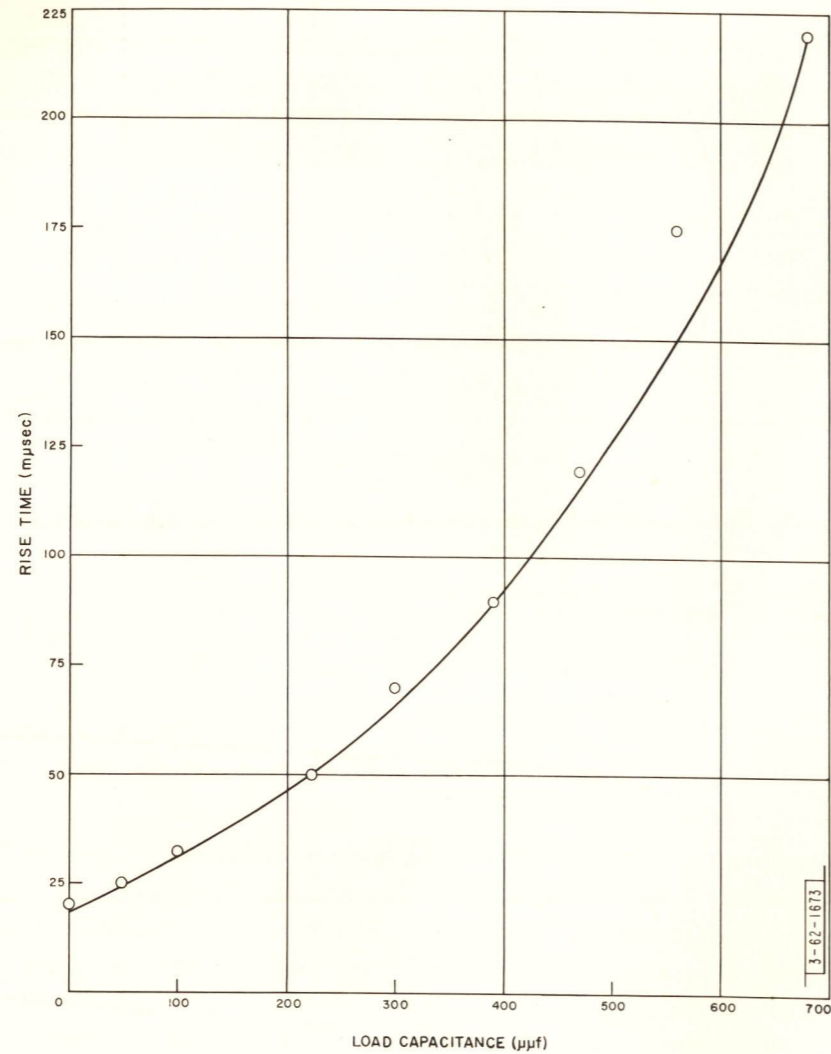


Fig. 39. Cascode output rise time vs load capacitance.

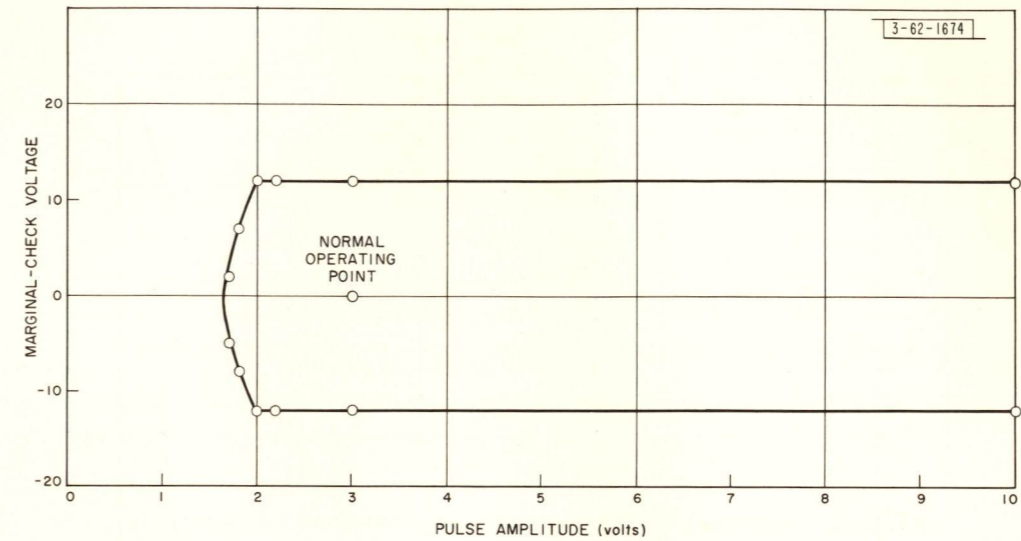


Fig. 40. High-speed flip-flop marginal-check voltage vs input pulse amplitude.

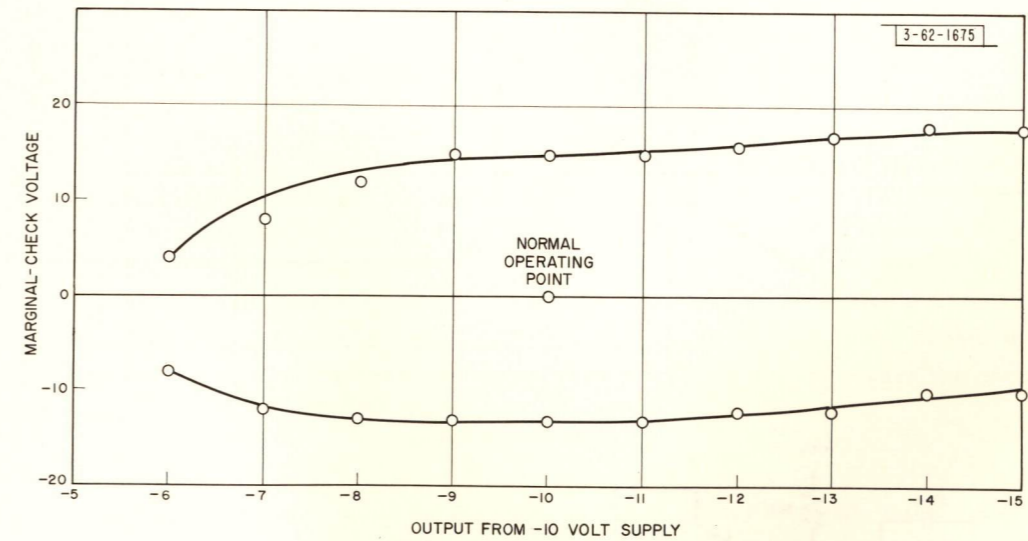


Fig. 41. High-speed flip-flop marginal-check voltage vs -10v supply.



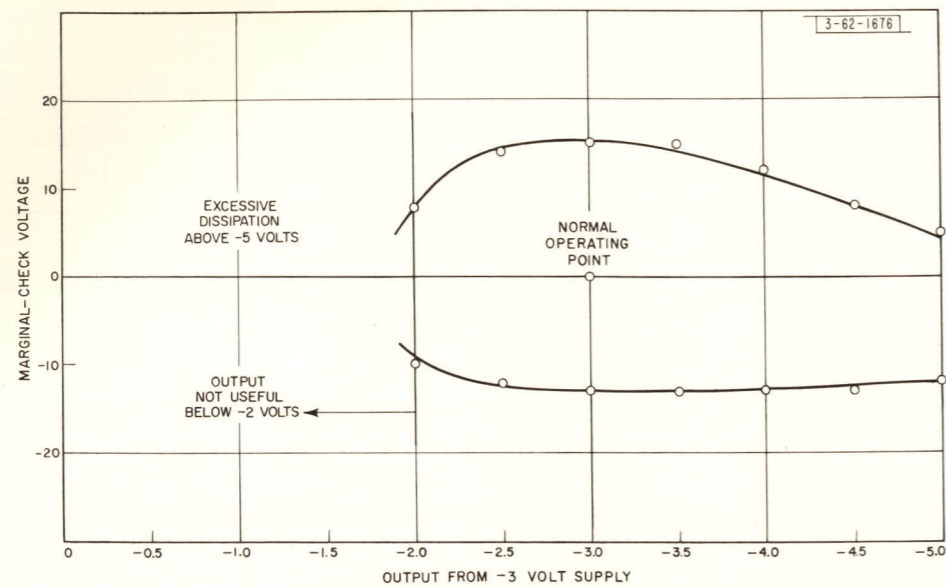


Fig. 42. High-speed flip-flop marginal-check voltage vs -3v supply.

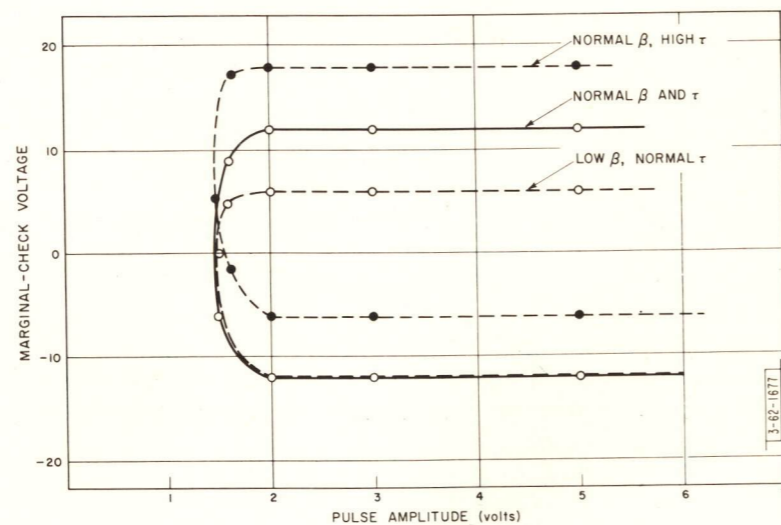


Fig. 43. Margins vs pulse amplitude for variations in  $\beta$  and  $\tau$  in one of the flip-flop transistors.

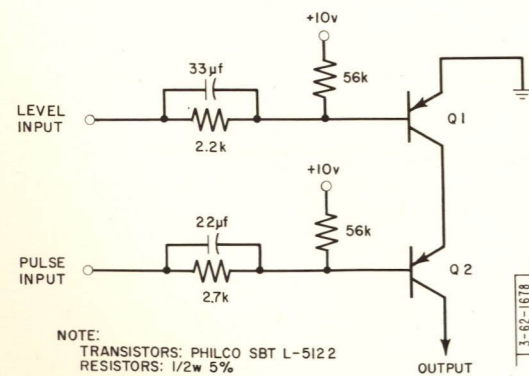


Fig. 44. Transistor pulse gate.

NOTE:  
TRANSISTORS: PHILCO SBT L-5122  
RESISTORS: 1/2w 5%

APPENDIX A  
CHARACTERISTICS AND APPLICATIONS OF COMPONENTS

The discussion of design methods in the body of the report has specified many components and their applications in particular circuits. Certain component characteristics and notes on applications that have led to reliable electronic design are discussed in this appendix.

A. TUBES

The best tubes are assembled in air-conditioned, lint-free rooms, since the cause of many intermittent shorts has proved to be carbonized particles of lint and foreign matter within the tube envelope. Residual gases in the tube are reduced by a better-than-average vacuum. A tube designed for simplicity and ease of assembly will be more dependable than a complex construction.

Metal evaporated from the cathode and deposited on the structural mica insulators tends to lower the leakage resistance between the electrodes. To counter this, slots are cut in the insulators to lengthen these leakage paths.

Grid wires are plated to minimize secondary emission. Plates are designed to maximize the heat-radiating area, and are made of materials with minimum gas content.

1. Design Features

a. Grid Spacing:— A short, rugged mount structure with a minimum of 0.005 to 0.006 inch interelectrode spacing will minimize the incidence of shorts and troubles resulting from rough handling. For mount structures longer than one inch, even wider spacings are necessary. A requirement for high transconductance is basically opposed to the requirement for high tube reliability.

b. Cathode Temperature:— The operating temperature of the cathode must be chosen as a best compromise among several factors that affect tube life. Lower cathode temperature may reduce emission below usable levels early in life, may increase the susceptibility of the cathode to poisoning by gases, and may increase cathode interface (an impedance that develops between the cathode base and the emitting material). High cathode temperature increases the evaporation of the coating and sublimation of the base metal (with consequent increase in grid emission and depositing of metal coatings on structural insulators), increases the probability of heater burnout, and may accelerate the growth of cathode interface.

2. Notes on Applications

Vibration and shock must be avoided during tube operation, since long-life pulse tubes are not usually designed to minimize microphonics. Bulb temperature must be reduced to 80 to 100°C by forced-air circulation or air conditioning, to avoid evolution of gas from the glass envelope and to reduce the incidence of electrolysis of the glass between base pins under the influence of DC potential.

Heater voltage regulation within 2 per cent of rated value has been demonstrated to give increased tube life. DC cathode current should be limited to 50 to 60 milliamperes per square centimeter



of active cathode area. Pulse cathode current should be limited to about 10 times this value, for short pulses (under 1  $\mu$ sec) and low duty factors (under 10%). Although these numbers have been proved safe in operation, they are not presented as limiting boundary values.

For longest tube life, design ratings for plate current and dissipation may have to be reduced from those given in manufacturers' literature. It is well to remember that manufacturers base their ratings both on the demand for particular tube characteristics and on the results of extensive life tests. For any particular tube application, the components engineer should work with the manufacturer's applications engineer to determine the basis for the tube's ratings, and the life that can be expected from the tube in this application.

Tests to determine compliance with specifications must be performed by the manufacturer, the user, or both. The manufacturer should give a pre-burning test to every tube to detect weak heaters. Tests to pick up transient shorts are particularly important if intermittent failures in service are to be minimized; these tests should be sufficiently sensitive to detect shorts of as little as one-microsecond duration. Pulse and steady-state life tests on a sample basis, if continued sufficiently long, will give an indication of expected life. Manufacturers' tests should weed out potentially unserviceable tubes.

Standardization on a minimum number of tube types, and cooperation with the manufacturer's tube-applications engineer to assure best use of these types, will materially reduce the incidence of interrupting tube failures.

## B. SEMICONDUCTOR DIODES

### 1. Characteristics

Semiconductor diodes are most often used as switching networks or as blocking or clamping devices, to hold DC levels in the presence of pulses, and to clip unwanted tails from pulses. All these applications presuppose that the diode will have nearly perfect rectifier characteristics — an open circuit in one direction, and a short circuit in the other. Every realizable diode falls short of this ideal in several respects. Further, the diode acts differently when subjected to pulses than it does under static DC conditions.

The principal characteristics of diodes that are of importance to the pulse-circuit designer are the following: (1) static (DC) forward voltage drop, (2) static back current, (3) reverse voltage breakdown, (4) forward recovery, and (5) reverse recovery. The first three of these are relatively self-explanatory, but forward recovery and reverse recovery are important factors that may be overlooked.

a. Static (DC) Forward Voltage Drop:- The diode volt-ampere curve is nonlinear, and electrical description of this characteristic should include a maximum value (or a tolerable range of values) of voltage drop at a specified forward current.

b. Static Back Current:- A maximum value of back current should be specified at a fixed back voltage.

c. Reverse Voltage Breakdown:- At high reverse voltages, the back resistance of semiconductor diodes decreases rapidly, so much so that the diode may destroy itself. This reverse

breakdown voltage should be well above the highest back voltage that will be applied to the diode in any circuit application.

d. Forward Recovery:- When a forward current is suddenly forced through some diodes, the voltage drop across them initially is as much as 200 per cent greater than the steady-state value, decaying to the steady-state value in a fraction of a microsecond.

e. Reverse Recovery:- The reverse resistance of a diode requires a finite time to build up after the diode has been switched from the forward to the back direction. In some junction diodes, the back resistance immediately after switching may be as low as the forward resistance before switching, and the recovery time may be hundreds of microseconds. In fast whisker diodes, the initial back resistance is often not less than one-tenth the static back resistance and has a time constant of the order of 0.1  $\mu$ sec.

The characteristics described above should be specified at values close to those existing in the circuit application. If a diode is to be used under conditions different from those in the diode manufacturer's specifications, the tests performed should duplicate as much as possible the actual operating conditions. (An ohmmeter does not give a valid indication of either back resistance or forward resistance.)

Since diode characteristics are adversely altered by the effects of moisture and other contaminants, a sealed housing should be specified. Glass-enclosed diodes have been proved more satisfactory than diodes that depend for moisture resistance upon some waxy filling compound.

### 2. Notes on Applications

Silicon and tungsten-whisker germanium diodes do not exhibit the very low forward-pulse voltage drop needed for core driving and other high-current applications. Gold-bonded and indium-plated whisker diodes are better suited for such uses.

Junction diodes, and some gold-bonded and some tungsten-whisker diodes exhibit long switching time (slow reverse recovery). Diodes for use in fast-pulse computers should be specified for fast reverse recovery.

If a diode is exposed to high temperatures during soldering, its characteristics may change, and life may be impaired. It is wise to solder quickly, and to use a heat shunt (a copper alligator clip would do) on the diode lead while heat is being applied.

The back resistance of a diode may change markedly during life, particularly when traces of contaminants introduced during manufacture remain within the diode case. For circuits intended to give long service, the designer should use for back resistance a design figure that is considerably less than the one given in the manufacturer's specifications. A factor of 5 for degradation of back resistance from initial to end-of-life specifications has been used successfully.

Diodes should not be used indiscriminately in series to increase the back-voltage rating, or in parallel to increase current-handling ability. In series connection, a larger fraction of the applied back voltage will appear across the diode with the higher back resistance, increasing the probability of failure. Likewise, in the parallel connection, the diode with lower forward resistance will carry most of the current. Balancing resistors, across each diode in the series



connection, and in series with each diode in the parallel connection, will help to equalize the voltages and currents. The effect of the balancing resistors is to reduce back resistance, and to increase effective forward resistance, respectively.

### C. CONNECTORS

Connectors often give rise to intermittent-contact troubles. These usually result from inadequate contact pressure, which allows oxide or other insulating films to develop on the contact surfaces. After being flexed many times, spring members of the contact may become fatigued or distorted, reducing the contact pressure. If plugs are left disengaged for long periods, oxide or other insulating layers may develop on contact surfaces. The following suggestions may help prevent these difficulties:

- (1) Contact spring members should be relatively long, to avoid stress concentration when the spring is bent, and should be made of a non-fatiguing material such as beryllium-copper.
- (2) When a plug is mated with its socket, one contact surface should wipe over the mating surface for a considerable distance, to break down any insulating films.
- (3) Contacts should be plated with a non-tarnishing metal. Gold and rhodium have been satisfactory.
- (4) Contact pressure from surface to mating surface should be high, while the force required to mate the connector should be moderate to avoid damaging the connector parts during mating.

### D. RELAYS

Relays have been major troublemakers in both military and civilian equipment for many years. The difficulties center around contact erosion, failure to make contact through oxide or foreign matter on contacts, and mechanical failure of contact springs and armature supports.

For low-current, signal-handling relays, the following suggestions apply:

- (1) Extreme miniaturization should be avoided. Relatively long spring members will prevent stress concentration. A relatively large, conservatively rated coil should be used to avoid overheating and burnout.
- (2) Bifurcated (twin) contacts on each contact spring will ensure that if one contact of the pair is blocked by dust or foreign matter the other one will still provide continuity.
- (3) A dust cover with a gasket seal should be provided.
- (4) Cotton, paper, or other such organic insulations will, under the influence of DC potential and moisture, contribute to electrolytic corrosion of the windings. Nylon, cellulose acetate, and similar synthetic insulations are satisfactory. The potential of the coil should be negative with respect to the relay frame.
- (5) Arc-suppression networks across contacts that break current-carrying circuits should be provided to absorb the inductive voltage produced when the contacts open.

There is considerable controversy concerning the merits of hermetically sealed relays. In high-altitude, moist or salty applications, and those where tampering can occur, the hermetically sealed relay is essential. However, since the products of arcing, or varnish products produced when the coil overheats, may collect within the relay case and interfere with contact operation,

sealing is not a cure-all. Further, the relay cannot be adjusted if its parts should fatigue after many operations, and it must therefore be discarded. Where expert maintenance personnel are available, as is the case at a large computer installation, relays can be equipped with removable dust covers and thus be accessible for servicing.

There is always a time delay between application of voltage to the relay coil and the actual closing of the contacts. Likewise, there is a delay between the removal voltage and the actual openings of the contacts. This timing may change during the life of the relay, as a consequence of fatigue of spring members. The initial timing, and that after a large number of operations on a repetitive life test, should be studied if close timing is required by the circuit application.

Various means are used to increase the delay in the closing or opening of a relay, including mounting copper slugs on the relay core (which act as a short-circuited turn to delay the build-up or decay of the magnetic field), provision of fluid-filled or air dashpots, and use of external RC timing circuits.

Relay operation may create power-supply transients in other parts of the system when large currents are interrupted. Such transients may be minimized in some cases by operating the relays when minimum current is flowing through their contacts. In other cases, it is necessary to resort to decoupling networks or filters.

### E. RESISTORS

If intelligently selected and applied, resistors are a particularly dependable class of components. To assure long life, all standard resistors should be derated from their nominal power and voltage ratings.

#### 1. Composition Carbon Resistors

These resistors are not prone to open-circuit failure unless they are seriously overloaded. Available in 5, 10, and 20% initial tolerances, they are not so stable as other types of resistors during long life. A resistor considered by the manufacturer as a  $\pm 5\%$  unit may vary as much as  $\pm 20\%$  during several years' use. The nominal power ratings of these resistors should be cut by 50% to assure stability and long service.

#### 2. Film Resistors

These include deposited-carbon, precious-metal, and electrically conductive glass film types. They are considerably more stable than composition resistors, but a resistor nominally of 1% tolerance should be considered to have a 5% end-of-life tolerance. An additional safety factor should be included in the power rating of deposited-carbon types: they should be derated to 50% of nominal power rating. The metal and glass films are not so critical. If deposited-carbon resistors are used, they should be hermetically sealed. Varnish coatings have been shown to admit moisture, causing early failures. Glass housings, and ceramic housings with solder-sealed ends, are satisfactory.

#### 3. Precision Wire-Wound Resistors

These resistors are quite reactive, and thus are not highly useful in fast-pulse circuitry. They may be of great value in digital-to-analog decoders, since they are more stable than any other



kind of resistor. A 1% tolerance resistor will stay within 5% during life if it is properly derated (50% of nominal rating) and is not subjected to violent temperature excursions. Wire smaller than 0.002 inch should not be used in critical equipment. The construction that employs a cast or molded plastic bobbin, with an outer housing of the same plastic, is far superior to the older ceramic-bobbin, paper-wrap, varnish-impregnated construction.

#### 4. Power Wire-Wound Resistors

These are useful in power-supply bleeder and other high-power applications. Only the vitreous-enamelled (shiny coating) varieties are recommended. Power dissipated in the resistor should not exceed 50% of the nominal power rating. Resistance wire smaller than 0.002 inch should not be used. A metal mounting bracket to conduct heat to a metal panel or chassis should be used to carry off most of the heat dissipated in the resistor.

#### 5. Potentiometers

For low-power non-critical uses, the carbon potentiometer using a molded resistance element is satisfactory. As with composition carbon resistors, potentiometers should be derated, and consideration should be given to end-of-life tolerances. Vitreous-enamelled power rheostats have proved reliable in values up to 5000 ohms.

### F. CAPACITORS

If adequately specified and properly applied, capacitors need cause little trouble in electronic equipment. Capacitor failures result principally from poor construction techniques and from application of excessive voltage.

#### 1. Paper Capacitors

These should be hermetically sealed in metal cans, should have at least 3 layers of dielectric paper, and use a fluid impregnant such as mineral oil or one of the complex hydrocarbons marketed under trade names (not a wax). Applied voltage should not exceed 50% of the manufacturer's rated voltage, and should be even less for use at temperatures greater than 55°C. AC ripple voltage impressed on the capacitor may cause dielectric heating, which would require further derating. The capacitance can vary by 12% over the initial tolerance during life. Paper capacitors should not be used in circuits where day-to-day stability of capacitance is important. Tubular, bathtub, and rectangular can cases are popular.

#### 2. Mica Capacitors

Mica capacitors, particularly those using silver paint as the electrode material, are quite stable and trouble-free. Silvered micas, though, are subject to migration of the silver across insulating boundaries under the influence of moisture and DC voltage. Ordinary molded-phenolic housings are not sufficiently moisture-proof to prevent silver migration. The design tolerance should be taken as  $\pm 10\%$  beyond the nominal purchase tolerance for non-silvered units, and  $\pm 5\%$  beyond purchase tolerance for silvered micas; 50% voltage derating should be applied. Some trouble has been encountered in capacitors where the termination of the pigtail lead is only crimped in a slot in the end-plate inside the body. It should be specified that this joint be soldered.

#### 3. Ceramic Capacitors

These, in the disc and tubular forms, are quite dependable. Units over 0.001  $\mu\text{mf}$  use ceramic with high dielectric constant, and are quite unstable; these should be used only for bypass and decoupling applications where exact values of capacitance are of no concern. In smaller values, the design tolerance should be considered to be  $\pm 10\%$  beyond the purchased tolerance.

#### 4. Electrolytic Capacitors

These have been major troublemakers in consumer electronic equipment. The best electrolytic capacitors are "telephone quality," originally developed and produced by several suppliers for the Bell System; they are intended to give 10 years or more service life, and 2 years non-operating shelf life. A 10% voltage-derating factor should be applied, and surge voltages seen by the capacitor should never exceed the manufacturer's rated operating voltage. Capacitors that have been out of service for some time should be re-formed by connecting each in series with a 1000-ohm resistor to a source sufficient to develop rated voltage across the capacitor, for a period of one hour.

### G. TRANSFORMERS AND INDUCTORS

The principal troubles encountered in transformers stem from the effects of moisture. Electrolytic corrosion, plating away the copper wire on to the transformer frame in the presence of DC potential and moisture, may cause open-circuit failures. Decomposition of insulation, as evidenced by low insulation resistance, is also caused by moisture.

Such troubles can be remedied by insisting upon adequate varnish impregnation of the winding, and hermetically sealing the case. Very small wires, used to miniaturize transformers, may also be subject to failure from corrosion. High operating temperature of the windings may accelerate failure of the insulation. The maximum operating temperature of the windings recommended for long, reliable service is 70°C.

Small pulse transformers using toroidal ferrite cores have been most satisfactory for short-pulse circuits. When hermetically sealed with glass-to-metal terminal seals, and operated within the manufacturer's DC ratings, they have proved extremely dependable.

RF chokes have given very little trouble in service. Vacuum-varnish impregnated coils, wound on ferrite, powdered-iron, or passive cores, have been most satisfactory.



APPENDIX B  
TRANSISTORS

The transistor is a new device, dating back only to 1948 and, as such, does not have the long history of use accruing to most other electronic components. The transistor field is a fast-moving one in which the picture is continually changing; this means that practices and procedures may change as the units themselves change. Although various revolutionary devices are now on the horizon, this Appendix is concerned with devices presently available in production quantities.

The original transistors were point-contact devices, and the theory of these was not completely developed. Mechanical and electrical stability of early units was poor, and this led to difficulties and poor acceptance in some quarters.

The appearance of the junction transistor in 1950-1951 brought about the big break-through of the transistor into equipment design. Mechanically, it is a rugged unit, and can be made to handle power of the order of a few watts.

Most of the problems of transistor reliability can be traced to contamination in manufacture and leakage of water vapor into the device after fabrication. After receiving its final clean-up etch, the transistor must be handled under extremely clean conditions and well-controlled humidity, to prevent accidental contamination of the surfaces before or during encapsulation. For long life, a hermetic seal is a "must."

Potting compounds - solid, liquid or gaseous - may be used for protection against welding vapors or soldering fluxes, or they may be used to fix the surface potential at a stable point. Different treatments may be required for different types of units.

Junction transistors are basically very small sandwiches of p-type and n-type semiconductor material. These sandwiches may be arranged as p-n-p or n-p-n in structure in which these layers are, respectively, the emitter-base-collector electrodes of the transistor. The sandwich structure may be built up by either an alloying process (alloy junction transistor) or a crystal growing process (grown junction transistor).

The existence of the junction transistor in the two forms, n-p-n and p-n-p, using bias supplies of opposite polarity, makes possible some very useful circuits. The alloy junction transistor makes a very good switch, having OFF resistance of about a megohm and an ON or saturated resistance of about 10 ohms.

Most of the present-day transistors are made from germanium. Silicon transistors, however, are available and can be used at temperatures above 100°C.

A number of improved high-frequency junction transistors will be available in the next year or so. These should be capable of operation up to 300 Mcps with good efficiency.

## A. JUNCTION-TRANSISTOR CHARACTERISTICS

Since transistors have not yet been widely used in computer circuits, little life data have been accumulated. Therefore, transistor types can not be selected on the basis of proven reliability.



If transistors are to be used in large numbers, the types chosen should be those that can be manufactured with reasonable yields by present fabrication techniques. Characteristics that are important in the design of reliable transistor circuits are frequency response, power dissipation, and storage time.

### 1. Frequency Response

The frequency response of a junction transistor is inversely proportional to the square of the base width. Unfortunately, in an alloy junction transistor, the maximum emitter-collector voltage - the punch-through voltage - varies directly as the square of the base width. Therefore, as the frequency response is raised, the maximum operating voltage is decreased. This punch-through voltage relationship does not hold in a grown junction transistor. However, with present methods of fabrication, it is difficult to obtain high production yields of conventional, high-frequency, grown junction transistors (15 to 20 Mcps).

Special jet-etching and plating techniques make possible extremely accurate base-width control in the surface-barrier transistor. These units are in the 60- to 70-Mcps cutoff range. Maximum voltage is usually 6 to 20 volts, with recommended operating voltage 4 to 5 volts.

### 2. Power Dissipation

The power-handling capability of a transistor depends on good thermal design. Heat must be conducted away from the collector junction which, in a germanium transistor, cannot be allowed to exceed about 85°C. Provision for external connection to a heat sink is desirable for high-power units.

Since maximum voltages are normally limited to less than 50 volts, high-power transistors must be capable of passing high currents. The tendency for current gain to decrease with emitter current (alpha crowding) can be alleviated by double-doping the emitter. The problem of self-cutoff for the center region of the emitter is eliminated by the use of an elongated rectangular emitter.

Most high-power units will have poor frequency response (in the audio range) because the large electrode area necessary for high currents means high junction capacities and wider base widths (to allow for the possibility of uneven alloying). Most high-frequency transistors tend to have low power ratings. The surface-barrier transistor is rated at 10 mw.

### 3. Storage Time

The collector current of a transistor that has been saturated or turned ON does not stop flowing the instant a turn OFF signal is applied. The transistor remains at a low impedance for a short period of time until it recovers from the saturated condition. This delay or storage time is of considerable importance in high-speed saturating-type switching circuits. Storage time can be reduced by making the base width small - that is, by designing a high-frequency transistor.

## B. NOTES ON APPLICATIONS

Temperature limits must be rigidly observed and units should be operated close to or below room temperature if possible. High temperatures cause accelerated deterioration. Transistors good for tens of thousands of hours at room temperature may fail in hundreds of hours at 100°C. Since

high power dissipations cause internal temperatures to rise, circuits must be designed to keep power dissipation low. Silicon transistors should be used where high temperatures are unavoidable.

In general, as transistors age, collector leakage current will increase, current gain will decrease, and breakdown voltage will decrease. Circuits must be designed to allow for these gradual variations in parameters.

For best reliability, transistors should probably be soldered into circuits. A heat sink should be used to prevent excessive junction temperatures. The leakage in ordinary 110 v AC soldering irons may be sufficient to damage certain types of low-power transistors (such as the surface-barrier transistor). Irons with on-off switches have been found to develop large momentary transients capable of destroying these units. A small 6-volt iron is recommended and will eliminate many of these difficulties.

Transistors should be tested individually in the grounded-emitter configuration. An automatic curve plotter is useful for this purpose. Grounded-emitter displays magnify most of the important irregularities by the factor of the current gain,  $\beta$ . The avalanche breakdown voltage occurs at a lower value for this configuration.

For saturating switching applications, the alloy junction transistor is usually superior to the grown junction transistor since it has a lower emitter-collector impedance.

Life tests made under conditions similar to those of the contemplated use are helpful in predicting reliability. These tests may possibly be accelerated by operation at increased ambient temperatures (with considerable reservations about the validity of such a practice since additional failure mechanisms may occur at elevated temperatures). This procedure is not recommended if reasonable time is available for room-temperature tests.



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LINCOLN LABORATORY

Memorandum No. 2G-24-76

To: E. W. Bivans  
From: K. E. Perry and E. J. Aho  
Subject: A Fourier Synthesis Character Generator

**ABSTRACT**

An analog device has been developed for displaying alphanumeric or numeric characters on a cathode-ray tube face by deflecting the spot so that it traces out the character smoothly and continuously. The necessary "x" and "y" deflection voltages are obtained by a Fourier synthesis technique that involves combining various harmonic frequencies of a fundamental frequency. A single character is displayed in about thirty microseconds.

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## A FOURIER SYNTHESIS CHARACTER GENERATOR

A number of schemes has been devised in the past for scribing numeric and alphabetic characters on a scope face by spot deflection. Digital as well as analog deflection has been employed. A new analog circuit recently developed in Group 24 for this purpose has some advantages in both simplicity and versatility.

Consider the Arabic numerals zero through seven. Each of these may be represented as a segment of a continuous closed curve given in Cartesian coordinates by the equation  $y = f(x)$ . In general,  $y$  is a multi-valued function of  $x$ , but we can also represent the curve by two parametric equations:

$$\begin{aligned} y &= f_1(t) \\ x &= f_2(t) \end{aligned} \quad t_0 \leq t \leq t_1$$

where  $f_1$  and  $f_2$  are single-valued functions of  $t$ . If  $t$  is the time, then these functions define the continuous motion of a point along the curve. They must clearly be single-valued functions, since the spot cannot be in two different positions at the same time. If the tangential speed of the point is known at all times (specifically if it is constant), then the parametric equations are defined by the equation  $y = f(x)$ . Thus, if  $f_1(t)$  and  $f_2(t)$  represent the voltage waveforms that are applied to the  $y$  and  $x$  deflection amplifiers, the desired curve will be traced on the scope face. Since most of the symbols are not closed curves, an unblanking function must be provided to intensify the desired segment.

The functions  $f_1$  and  $f_2$  are defined in the interval  $t_0 \leq t \leq t_1$  where  $(t_1 - t_0)$  is the time required for the spot to trace the entire closed curve. A function of this type can be expanded, according to Fourier's theorem, into a series of terms of sines and cosines, thus:

$$f_1(t) = A_0 + A_1 \sin \omega t + B_1 \cos \omega t + A_2 \sin 2\omega t + \dots$$

where  $\omega = 2\pi / (t_1 - t_0)$  and  $t_0 = 0$ . The procedure for finding the coefficients  $A_n$ ,  $B_n$  is as follows: The desired character is drawn on graph paper, including a retrace segment which closes the curve.<sup>†</sup> Twenty-four

---

<sup>†</sup>In order that all characters can use the same unblanking function, closed figures like "zero" and "eight" have redundant retrace segments tacked on as an appendix.



points are laid off along the curve at roughly equal intervals. (The number of points used is arbitrary.) These points divide the time ( $t_1 - t_0$ ) into twenty-four equal intervals. The x and y coordinates of each point are tabulated with  $t_0$  taken as the center of the retrace segment (Fig. 11). These tabulated values represent the two functions  $f_1(t)$  and  $f_2(t)$ . These functions may be analyzed by any one of several graphical and numerical integration methods. The method we now use is a purely graphical one where each x or y value is laid off as a vector at an angle equal to  $(n\omega t)$ . These vectors are added head to tail and the projections of the resultant vector give the coefficients  $A_n, B_n$ . (See Bibliography, Reference 1.)

A circuit has been developed for synthesizing the desired voltage waveforms  $f_1(t)$  and  $f_2(t)$  from artificially generated sine and cosine waveforms. Five harmonics are used with fundamental frequency of 30 kc. Ten tuned circuits (5 sine and 5 cosine) are simultaneously shock-excited into oscillation by a gate 33  $\mu$ s wide. Thus are generated one cycle of 30 kc, two cycles of 60 kc, three of 90 kc, four of 120 kc and five of 150 kc. These ten signals are fed through emitter-follower buffers to the primaries of ten toroidal transformers. Secondaries are wound on these toroids with direction of winding and number of turns determined by the sign and magnitude of the Fourier coefficients determined above. When these secondaries are connected in series and one end of the series circuit grounded, the desired voltage waveforms appear at the other end.

Fig. 1 is a complete block diagram of the prototype system. The circuit as depicted here will display the numerals 0 through 7, four rows deep (32 characters). This can be displayed on any oscilloscope which is provided with "x" and "y" inputs and an external unblanking connection.

A 120-kc sine wave is fed into a clock generator (Fig. 3) which shapes the signal into a square wave. The prime side of the clock generator output is commutatively coupled to Flip Flop  $C_1$ , the first of a chain of eight serial counters.<sup>†</sup> The unblanking function is generated in the intensity flip flop, controlled by  $C_1, C_2, C_3$  and the clock generator. Referring to the master timing diagram (Fig. 2), we see that the intensity pulse (waveform No. 12) starts one-half a clock cycle (about 4  $\mu$ s) after the prime side of Flip Flop  $C_3$  (pin No. 10) goes up, and ends 4  $\mu$ s

<sup>†</sup>For a description of the type of flip flop circuitry used, see Bibliography Reference 2.



before the same point goes down. This, it will be seen, unblanks that segment of the lissajous pattern which forms the desired character. One fourth of this continuous closed curve is blanked out.

Flip Flop  $C_3$  which shock-excites the ringing circuits in the harmonic generator (Fig. 8) is operating at exactly one-half the rate of the fundamental frequency used in the synthesis. The ringing period of the shock-excited oscillators occurs during the time the prime side of Flip Flop  $C_3$  is high. Since the fundamental frequency (30 kc) is twice the frequency of Flip Flop  $C_3$ , we get one complete cycle into the slot before the ringing is terminated by a change of state in  $C_3$ .

In like manner, we have two cycles of the second harmonic, three of the third, four of the fourth and five of the fifth, all initiated and terminated at the same time (Fig. 12). The sine waves and the cosine waves are generated in parallel-resonant and series-resonant circuits respectively. Input A (Fig. 8) which is connected to five sine-wave ringing circuits is controlled by Flip Flop  $C_3'$ . When  $C_3'$  goes up, the five input transistors connected to point A are cut off and the parallel resonant circuits composed of  $L_1$ ,  $C_1$  and  $C_2$  ring at their respective frequencies (30, 60, 90, 120 and 150 kc). The output is a positive sine wave. Damping of oscillations is small due to the high "Q" powdered iron cores used for  $L_1$  and  $L_2$ . Input B which is connected to five cosine-wave series ringing circuits is controlled by Flip Flop output  $C_3$ . These circuits oscillate at their resonant frequencies when the input transistor is on (point "B" low). The output is a negative cosine wave. See Fig. 12.

It is interesting to note that since these ringing circuits are cut off at a point in the cycle exactly corresponding to the turn-on point, there is no damping transient and the operation is not duty-cycle sensitive. In other words, at the instant of turn-off the voltage on the capacitor and the current through the inductor are very near to the quiescent values. This would be exactly true except for the losses during ringing. It is only necessary to leave the circuit turned off long enough for this small amount of lost energy to be replaced.

The values of L and C are determined by setting  $\sqrt{L/C} = R$  where R is the critical damping resistor (the R value arbitrarily chosen as 1 k) and L and C are unknown. Then solving first for L in terms of C and substituting this result in the equation  $\sqrt{LC} = 1/2\pi f$  and solving for C, L



can then be found from either equation. The trimmer condenser  $C_2$  has a range of from 100  $\mu\mu\text{f}$  to 500  $\mu\mu\text{f}$  and is adequate for adjusting the ringing circuit for any LC inconsistencies.

Each ringing circuit is followed by an emitter-follower amplifier buffer which also serves to drive the base of a power transistor in an emitter-follower amplifier configuration. The output of the power transistor is coupled through a 1- $\mu\text{f}$  capacitor to the primary of a toroidal transformer. Referring to both Fig. 1 and Fig. 8, we see that  $X_0$  and  $X_0'$ ,  $X_1$  and  $X_1'$ , etc., or  $Y_0$  and  $Y_0'$  or  $Y_1$  and  $Y_1'$ , etc., on the harmonic generator block (Fig. 1) are the terminals to the series secondary windings on the toroidal transformers. Every time that Flip Flop  $C_3$  cycles, these circuits have  $f_1(t)$  and  $f_2(t)$  waveforms on them. These secondary waveforms will not, however, be passed through the "or" diodes to the scope unless the X and Y inputs are high. The d-c level of the unprimed ends of the secondary windings ( $X_N$  and  $Y_N$  -- Fig. 1) are controlled by the state of their associated switches (Figs. 6 and 7). When a switch output is high, the corresponding "or" diode (Fig. 1) is forward-biased and the signal on that particular secondary winding is transferred to the scope.

The switches (Figs. 6 and 7) are PNP transistors in a grounded-emitter configuration. The collector controls the d-c level of the associated secondary winding in the harmonic generator. The base inputs have two states. When the base is high the collector is at -6.5 volts and its associated secondary winding sees an open diode in the "or" circuit preceding the scope (Fig. 1). When the base is low, the collector will be at ground or some small negative voltage above -6.5 volts, determined by the fixed resistor at the emitter. The purpose of this resistor is to adjust the level of the synthesized waveform  $f_1(t)$  and  $f_2(t)$ . In the original graphical analysis for  $f_1(t)$  and  $f_2(t)$ , no attempt was made to compute the d-c Fourier coefficient  $A_0$  since the zero frequency cannot be accommodated in the transformers. Therefore, some of the numerals would be displaced from their proper relative positions on the scope face. It is this discrepancy in d-c level that is adjusted by the resistors.

The diode matrix (Fig. 5) selects the number to be displayed under control of Flip Flops  $C_4$ ,  $C_5$  and  $C_6$ . A different number will be displayed



during each unblanking pulse. Only one output is low at any time. This voltage turns on a pair of switching transistors in the selection-switch package. (Figs. 6 and 7.)

The four resistors on the X input of the scope (Fig. 1) are used to generate an eight-step ladder of voltages at the same rate as the unblanking function, thus displacing each numeral consecutively.

The three resistors on the Y input in conjunction with the slower running Flip Flops  $C_7$  and  $C_8$  displace the whole row of eight numbers vertically four times.

A simulation device was built to try the effect of various combinations of coefficients in generating various characters. The circuit is shown in Fig. 10. The toroid primaries are substituted for the toroids in the harmonic generator, and the 250-ohm potentiometers are adjusted to the proper coefficient values. The resulting character can then be observed.

Fig. 9 is a tabulation of the coefficients (number of turns) for the numerals "zero" through "seven" and Figs. 12 and 13 show the circuit waveforms. Fig. 14 shows the type of octal tabular display obtainable. Fig. 15 shows a miscellaneous assortment of characters generated with the simulator and demonstrates the versatility of this device. In Fig. 16 the harmonic generator is shown in the center with the control circuitry beneath. The simulator is on the left.

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## LIST OF FIGURES

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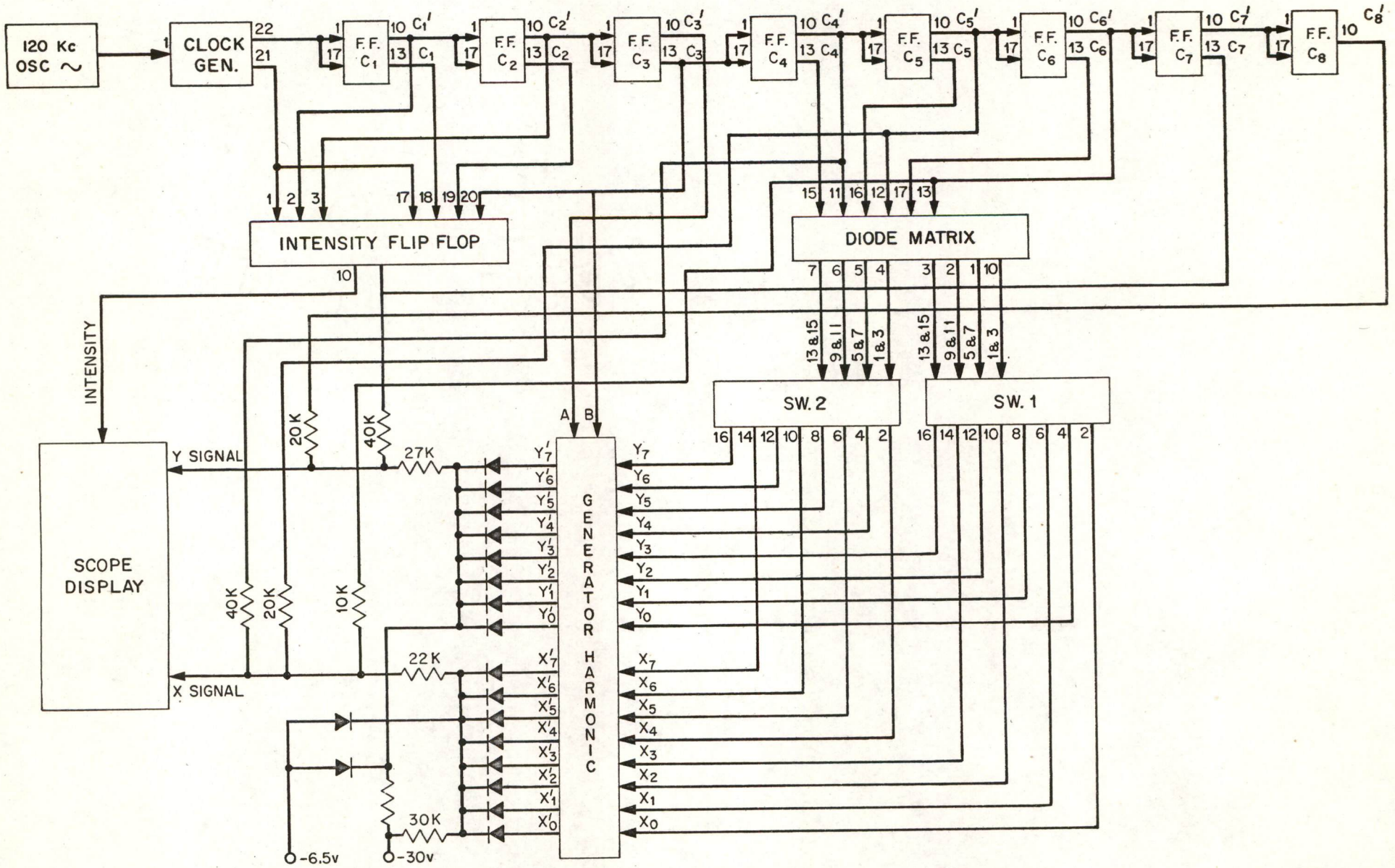


FIG. 1. FOURIER SYNTHESIS CHARACTER GENERATOR BLOCK DIAGRAM



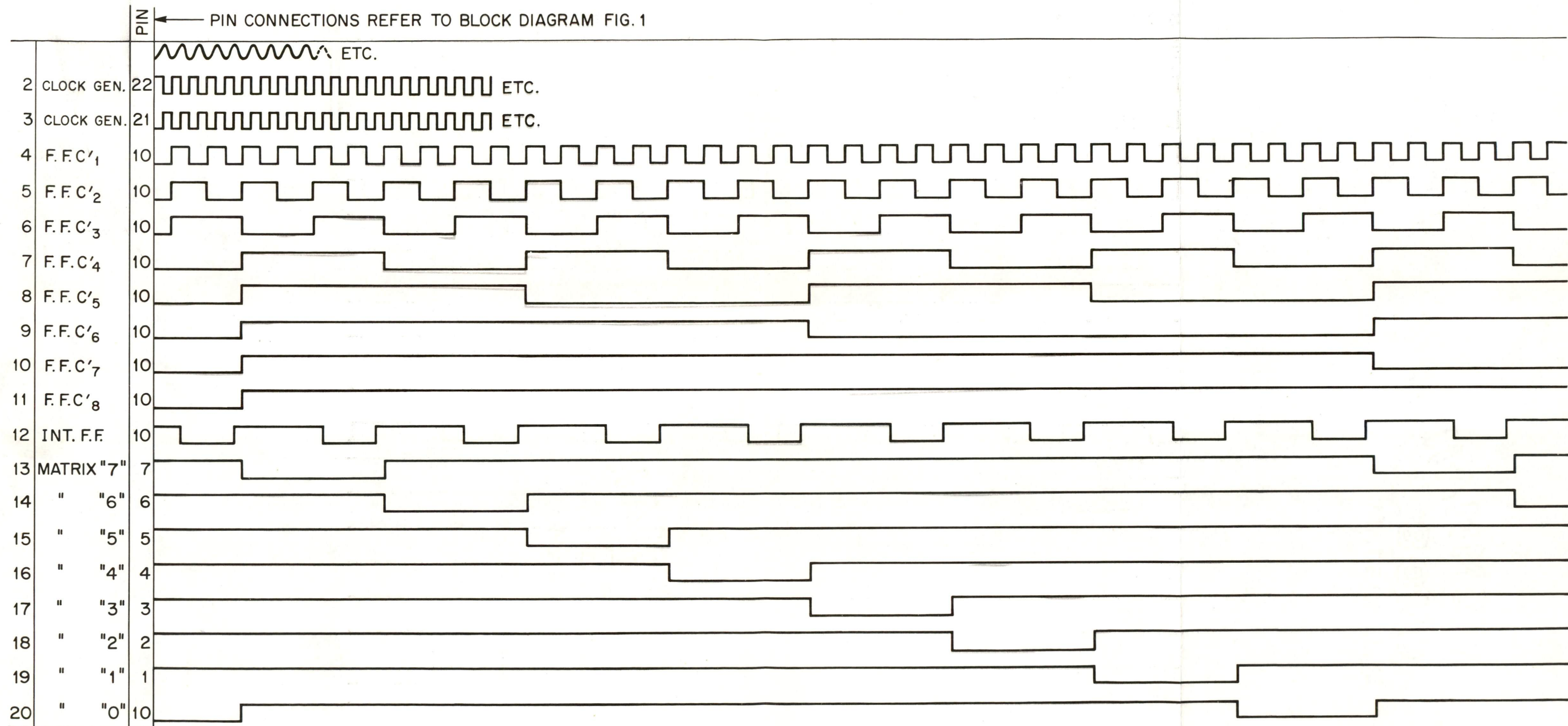
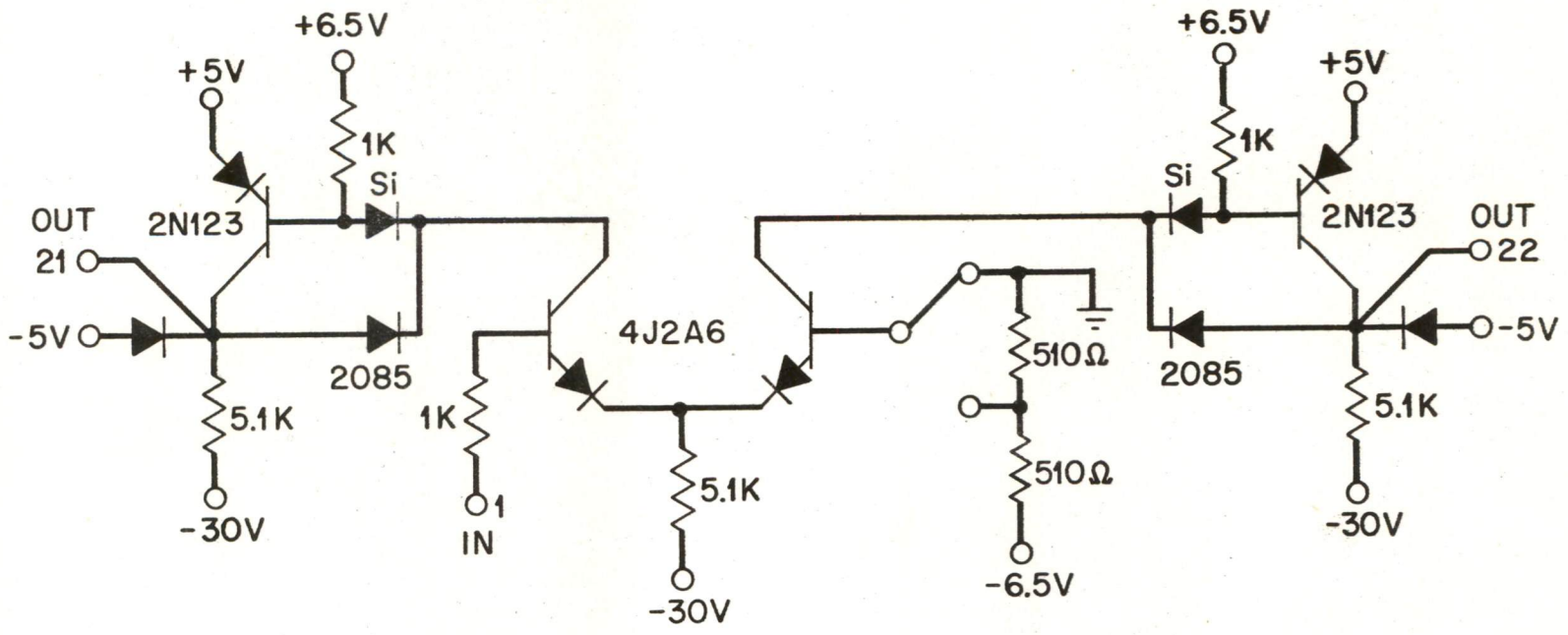


FIG. 2. F.S.C.G. MASTER TIMING DIAGRAM

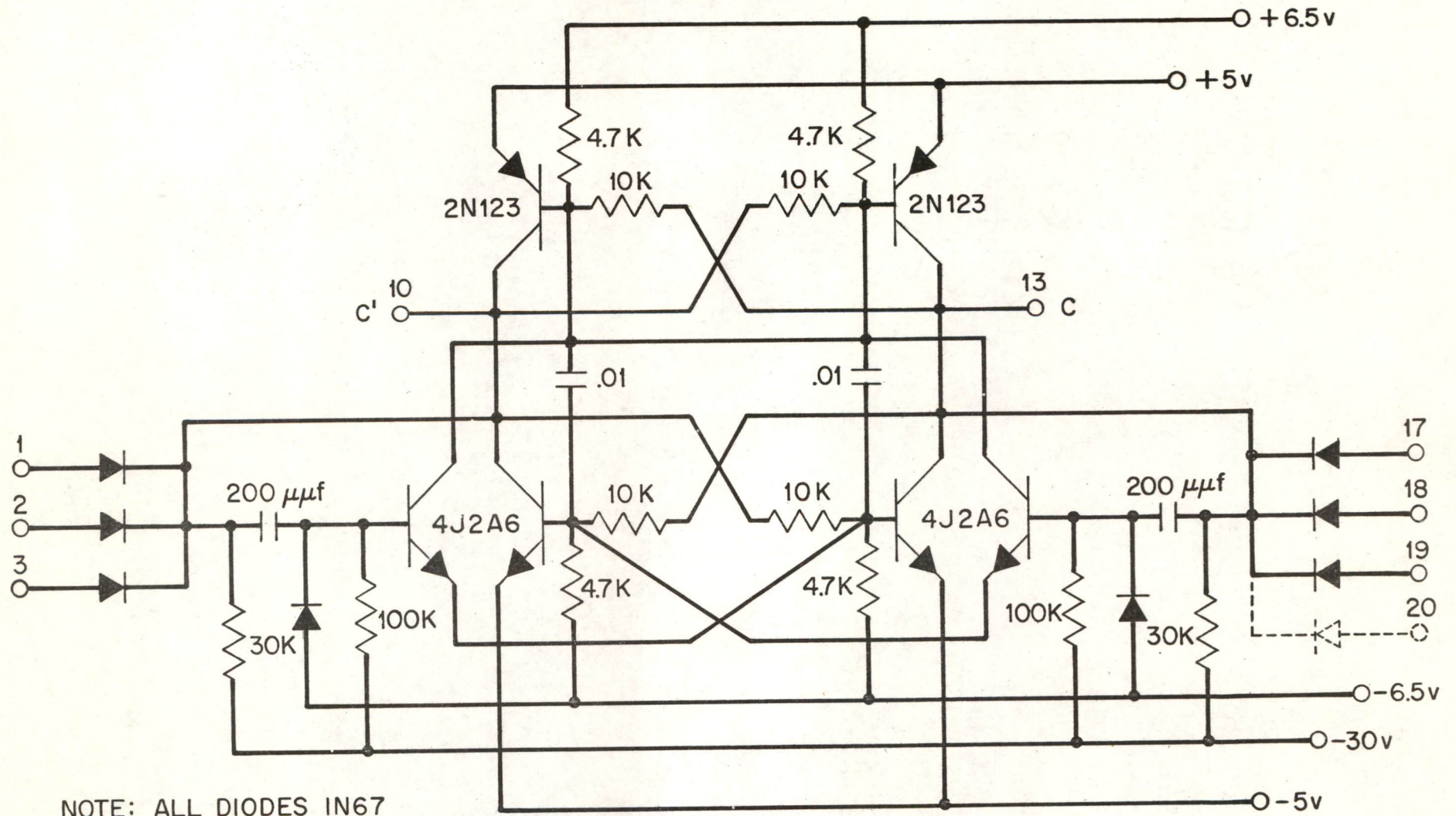




- NPN = 4JD2A6
- PNP = 2N123 OR 4JD1A23
- Si = SG22
- DIODES = 1N67

FIG. 3. CLOCK GENERATOR.





NOTE: ALL DIODES IN67  
 PIN #20 USED ONLY IN INTENSITY F.F.

FIG. 4. FLIP FLOP 100 Kc NEGATIVE LOGIC



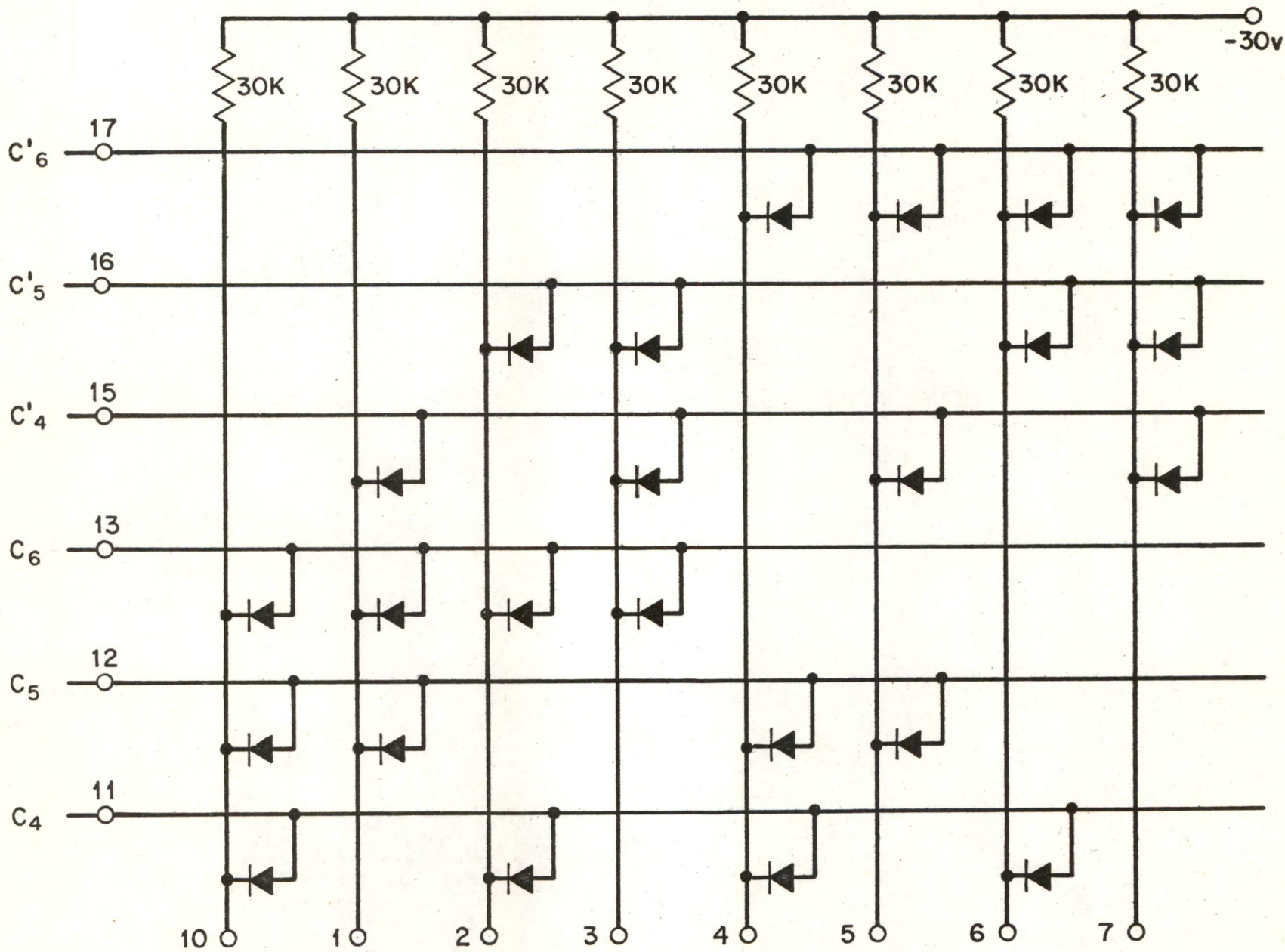


FIG. 5. F. S. C. G. MATRIX



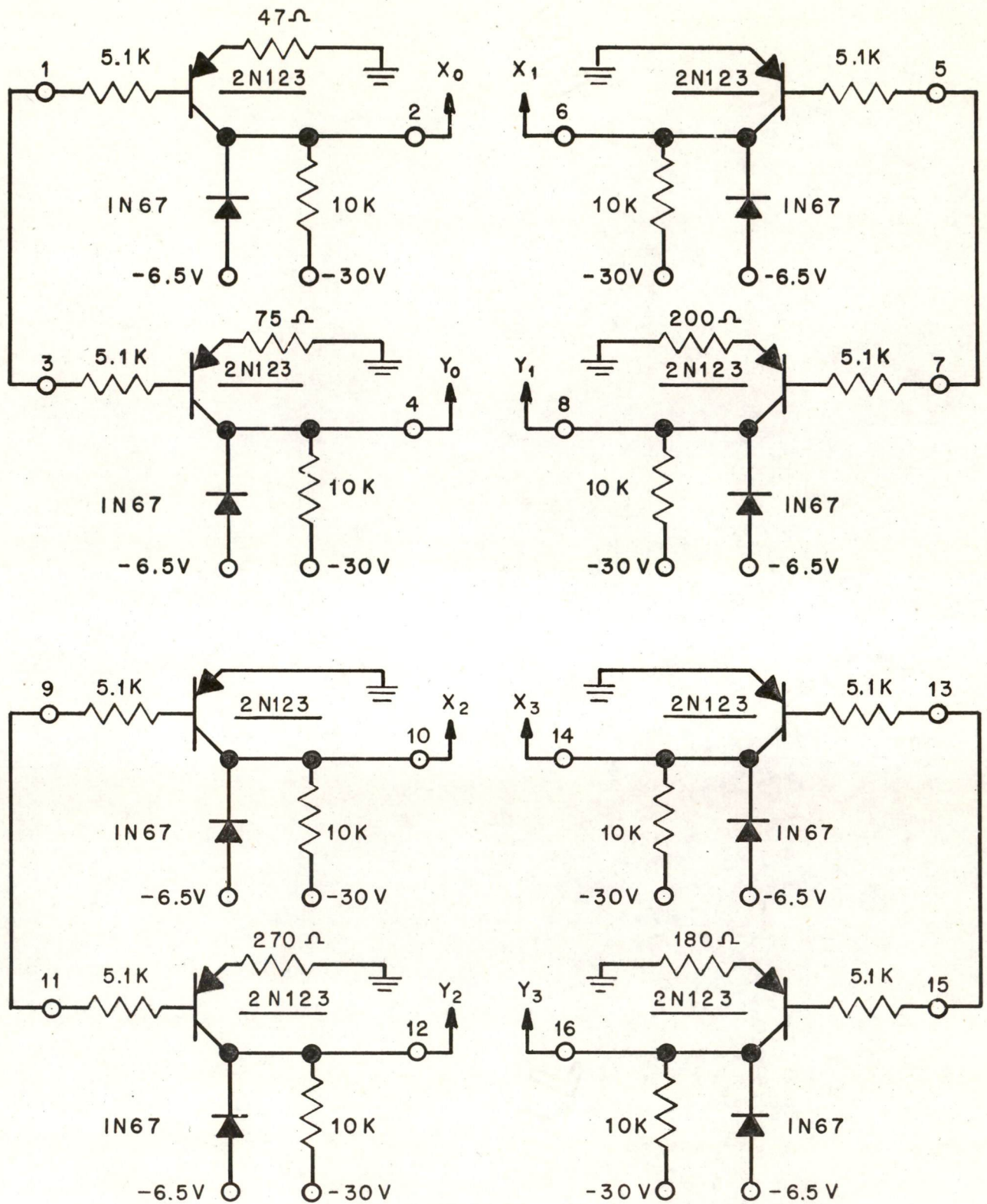


FIG. 6. F.S.C.G. CHARACTER SELECTION SWITCH NO. 1

Lapierre Fig. AHO A-6903



A-6903-2

Lapierre Fig.

AH0

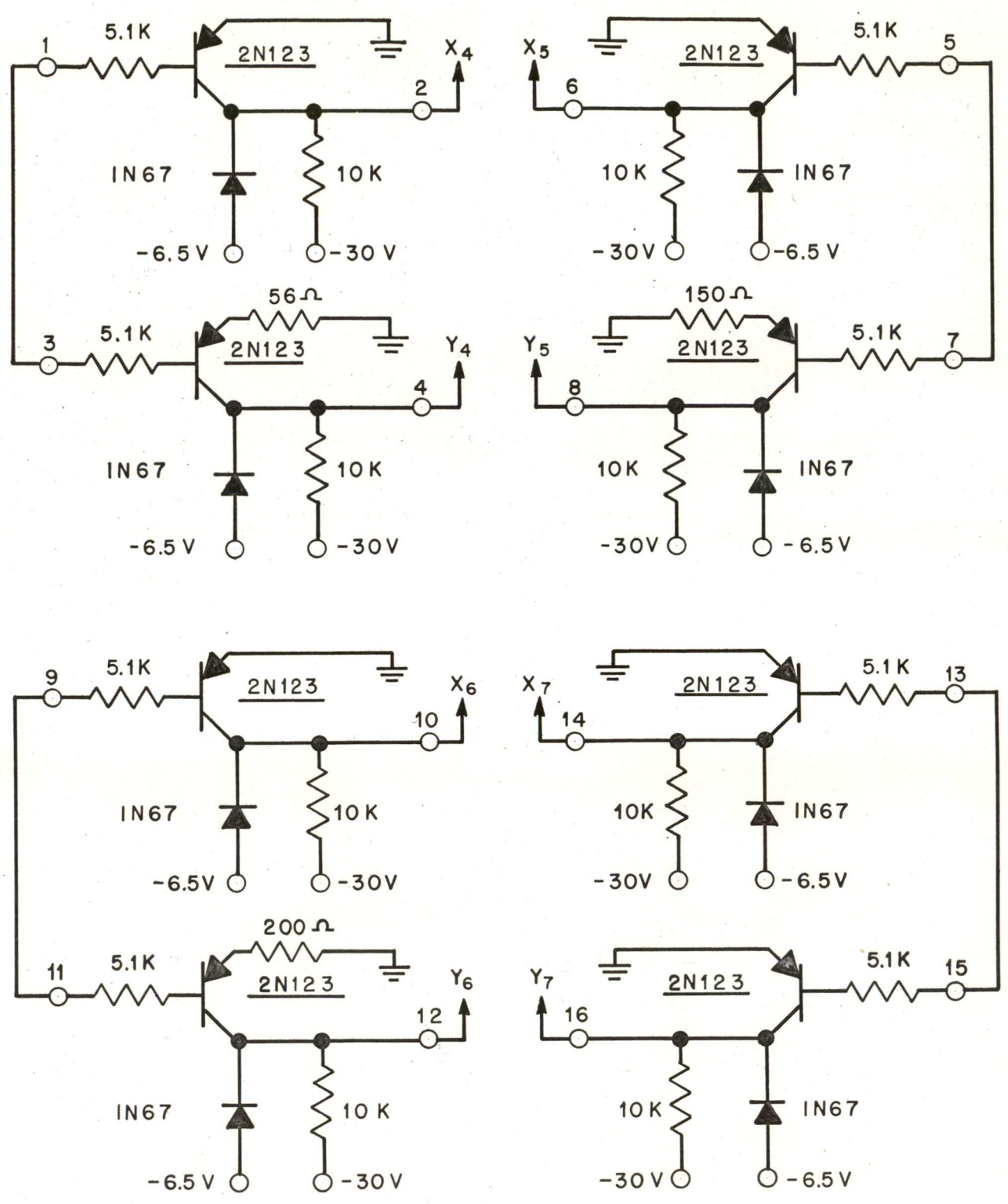


FIG. 7. F.S.C.G. CHARACTER SELECTION SWITCH NO. 2.



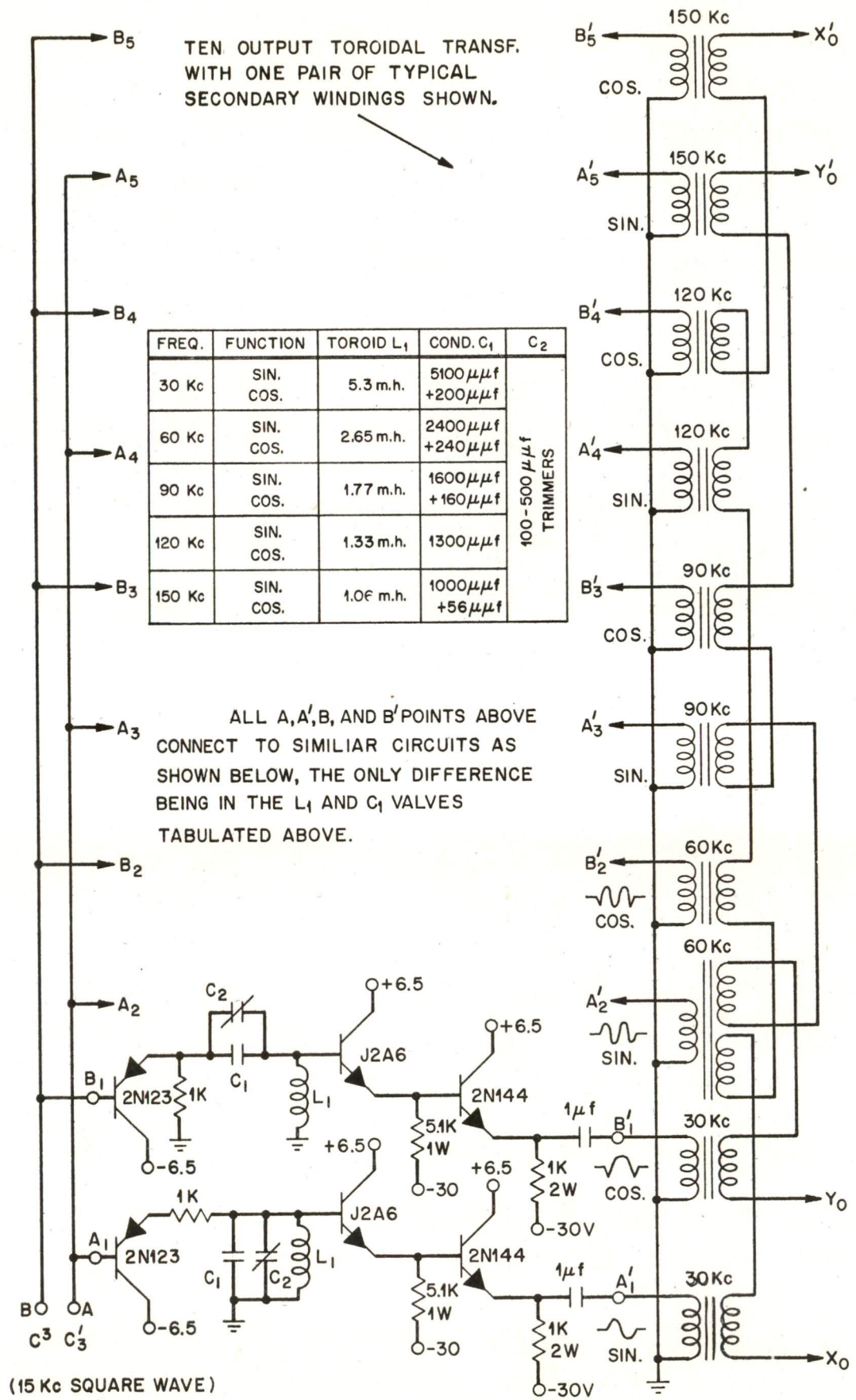


FIG. 8. HARMONIC GENERATOR.



FIG. 9. A TABULATION OF THE NUMBER OF ACTUAL TURNS TAKEN ON THE TOROIDAL TRANSFORMER SECONDARIES TO GENERATE THE REQUIRED WAVEFORMS ON X AND Y FOR EACH NUMERAL.

X (0)		Y (0)	
$a_1 + 28$	$b_1 - 8$	$a_1 \ 0$	$b_1 + 40$
$a_2 - 20$	$b_2 \ 0$	$a_2 \ 0$	$b_2 - 20$
$a_3 \ 0$	$b_3 \ 0$	$a_3 \ 0$	$b_3 \ 0$
$a_4 \ 0$	$b_4 \ 0$	$a_4 \ 0$	$b_4 \ 0$
$a_5 \ 0$	$b_5 \ 0$	$a_5 \ 0$	$b_5 \ 0$

X (1)		Y (1)	
$a_1 \ 0$	$b_1 \ 0$	$a_1 \ 0$	$b_1 \ 0$
$a_2 \ 0$	$b_2 \ 0$	$a_2 \ 0$	$b_2 \ 0$
$a_3 \ 0$	$b_3 \ 0$	$a_3 \ 0$	$b_3 \ 0$
$a_4 \ 0$	$b_4 \ 0$	$a_4 \ 0$	$b_4 \ 0$
$a_5 \ 0$	$b_5 \ 0$	$a_5 \ 0$	$b_5 + 47$

X (2)		Y (2)	
$a_1 - 3$	$b_1 \ 0$	$a_1 + 43$	$b_1 + 9$
$a_2 - 39$	$b_2 \ 0$	$a_2 \ 0$	$b_2 \ 0$
$a_3 \ 0$	$b_3 \ 0$	$a_3 - 2$	$b_3 + 6$
$a_4 \ 0$	$b_4 \ 0$	$a_4 \ 0$	$b_4 + 6$
$a_5 \ 0$	$b_5 \ 0$	$a_5 \ 0$	$b_5 \ 0$

X (3)		Y (3)	
$a_1 + 6$	$b_1 - 22$	$a_1 - 37$	$b_1 - 7$
$a_2 - 8$	$b_2 - 5$	$a_2 - 6$	$b_2 \ 0$
$a_3 - 6$	$b_3 + 22$	$a_3 + 7$	$b_3 \ 0$
$a_4 - 9$	$b_4 \ 0$	$a_4 \ 0$	$b_4 \ 0$
$a_5 \ 0$	$b_5 \ 0$	$a_5 \ 0$	$b_5 \ 0$

X (4)		Y (4)	
$a_1 - 15$	$b_1 + 21$	$a_1 + 4$	$b_1 - 37$
$a_2 + 18$	$b_2 + 7$	$a_2 + 24$	$b_2 - 3$
$a_3 \ 0$	$b_3 - 5$	$a_3 + 2$	$b_3 - 1$
$a_4 \ 0$	$b_4 + 1$	$a_4 + 3$	$b_4 \ 0$
$a_5 - 1$	$b_5 \ 0$	$a_5 + 1$	$b_5 \ 0$

X (5)		Y (5)	
$a_1 - 9$	$b_1 + 4$	$a_1 + 41$	$b_1 + 1$
$a_2 + 37$	$b_2 + 2$	$a_2 + 6$	$b_2 + 8$
$a_3 + 4$	$b_3 + 11$	$a_3 - 6$	$b_3 \ 0$
$a_4 + 3$	$b_4 - 1$	$a_4 + 3$	$b_4 \ 0$
$a_5 - 1$	$b_5 + 6$	$a_5 - 3$	$b_5 - 2$

X (6)		Y (6)	
$a_1 - 4$	$b_1 - 16$	$a_1 \ 0$	$b_1 + 28$
$a_2 + 15$	$b_2 + 32$	$a_2 + 21$	$b_2 + 7$
$a_3 + 6$	$b_3 + 6$	$a_3 \ 0$	$b_3 \ 0$
$a_4 \ 0$	$b_4 \ 0$	$a_4 \ 0$	$b_4 \ 0$
$a_5 \ 0$	$b_5 \ 0$	$a_5 \ 0$	$b_5 \ 0$

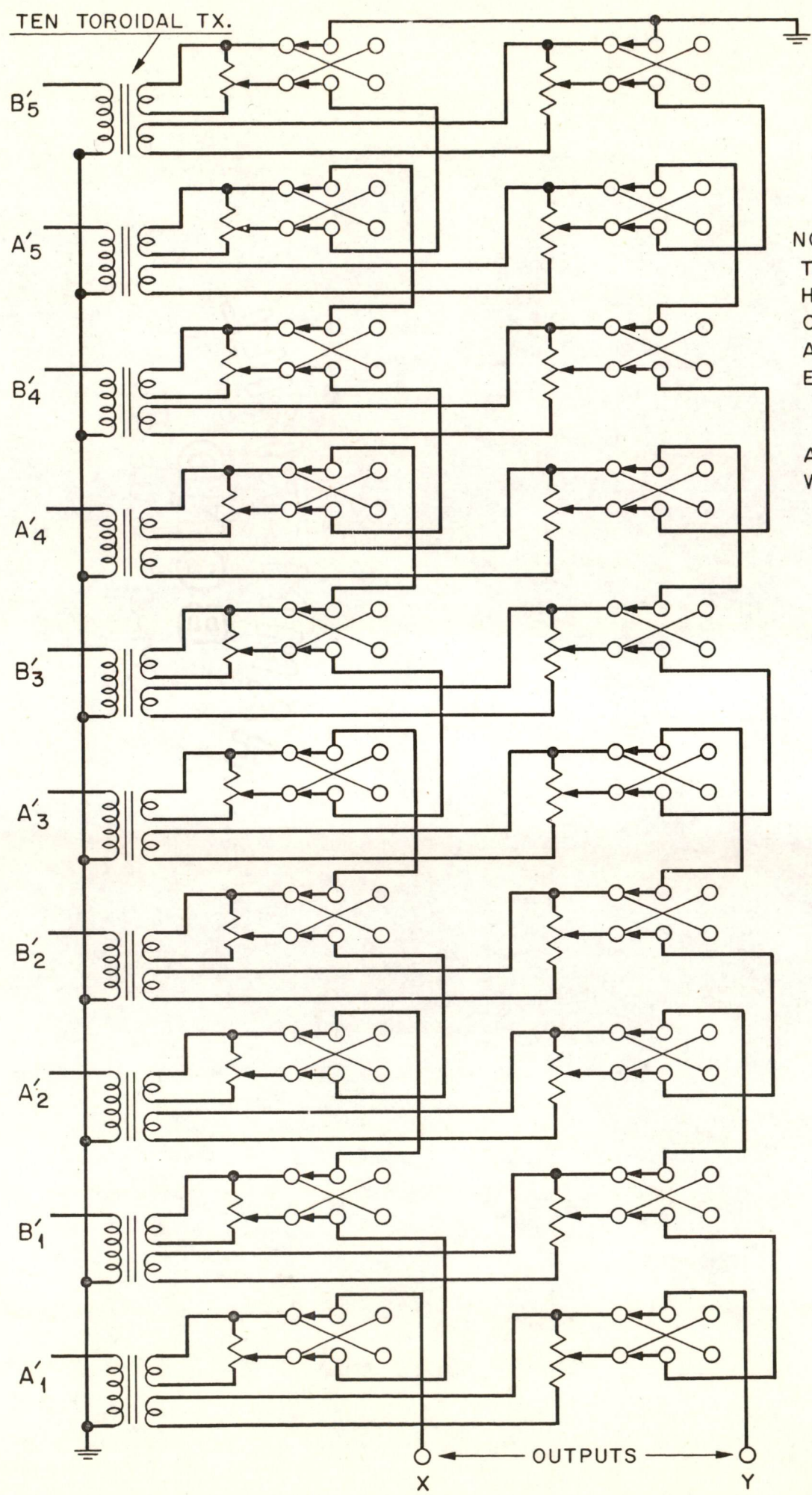
X (7)		Y (7)	
$a_1 \ 0$	$b_1 - 21$	$a_1 + 1$	$b_1 + 24$
$a_2 \ 0$	$b_2 - 19$	$a_2 \ 0$	$b_2 - 32$
$a_3 + 1$	$b_3 + 20$	$a_3 - 1$	$b_3 + 9$
$a_4 \ 0$	$b_4 + 13$	$a_4 - 1$	$b_4 - 10$
$a_5 \ 0$	$b_5 \ 0$	$a_5 \ 0$	$b_5 - 4$

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Lapierre Fig. AH0



A - 6903 - 10



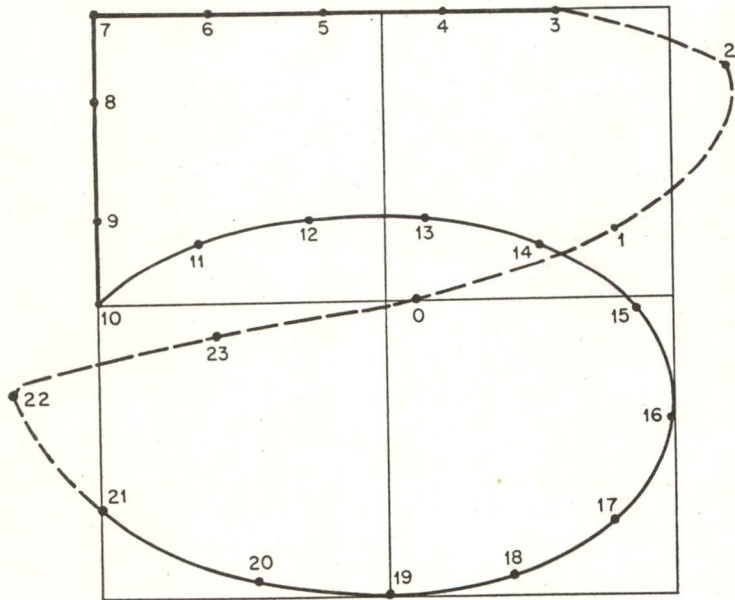
NOTE: THE TEN TOROIDAL TRANSF. HAVE 100 TURNS ON THE PRIMARY AND 30 TURNS ON EACH SECONDARY.

ALL POTS. ARE 250  $\Omega$  WIRE WOUND.

FIG. 10  
F.S.C.G.  
SIMULATOR

Compton - Fig. - AHO -





COORDINATES		
t	X	Y
0	+ .11	0
1	+ .80	+ .25
2	+1.20	+ .80
3	+ .60	+1.00
4	+ .20	+1.00
5	- .20	+1.00
6	- .60	+1.00
7	-1.00	-1.00
8	-1.00	+ .70
9	-1.00	+ .30
10	-1.00	0
11	- .65	+ .20
12	- .25	+ .29
13	+ .15	+ .29
14	+ .53	+ .20
15	+ .87	- .03
16	+ .99	- .40
17	+ .79	- .73
18	+ .43	- .93
19	0	-1.00
20	- .46	- .95
21	-1.00	- .70
22	-1.30	- .30
23	- .60	- .10

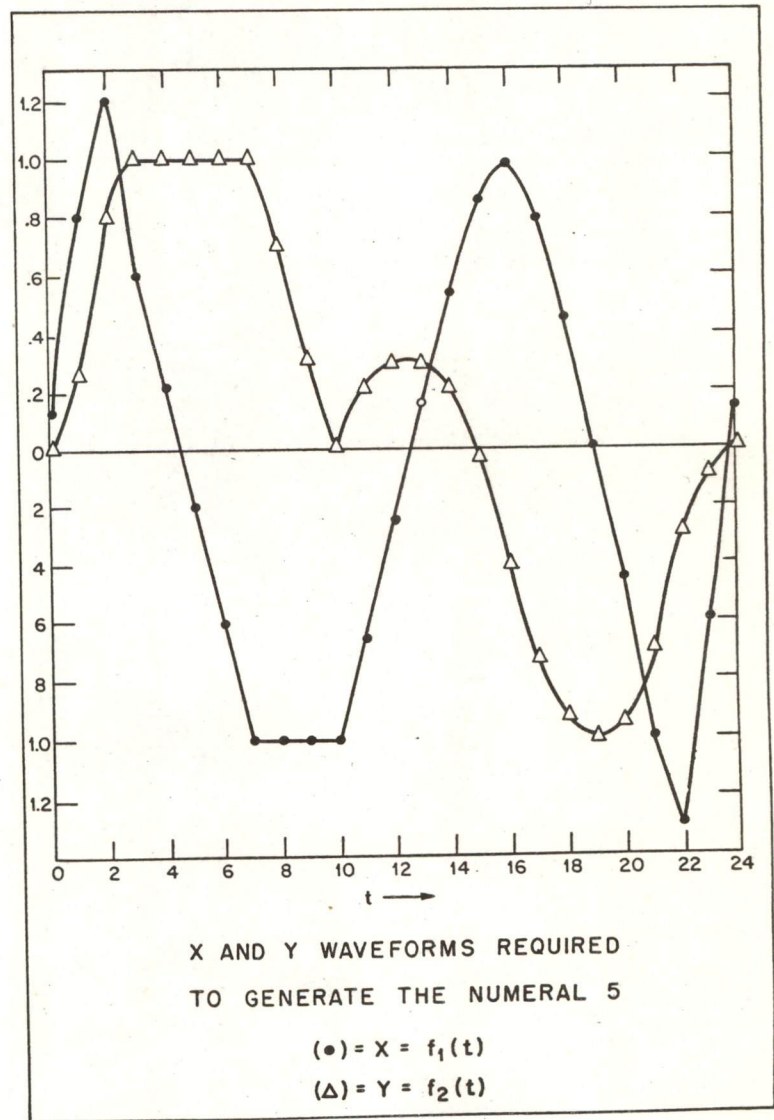


FIG. 11. ANALYSIS OF NO. 5



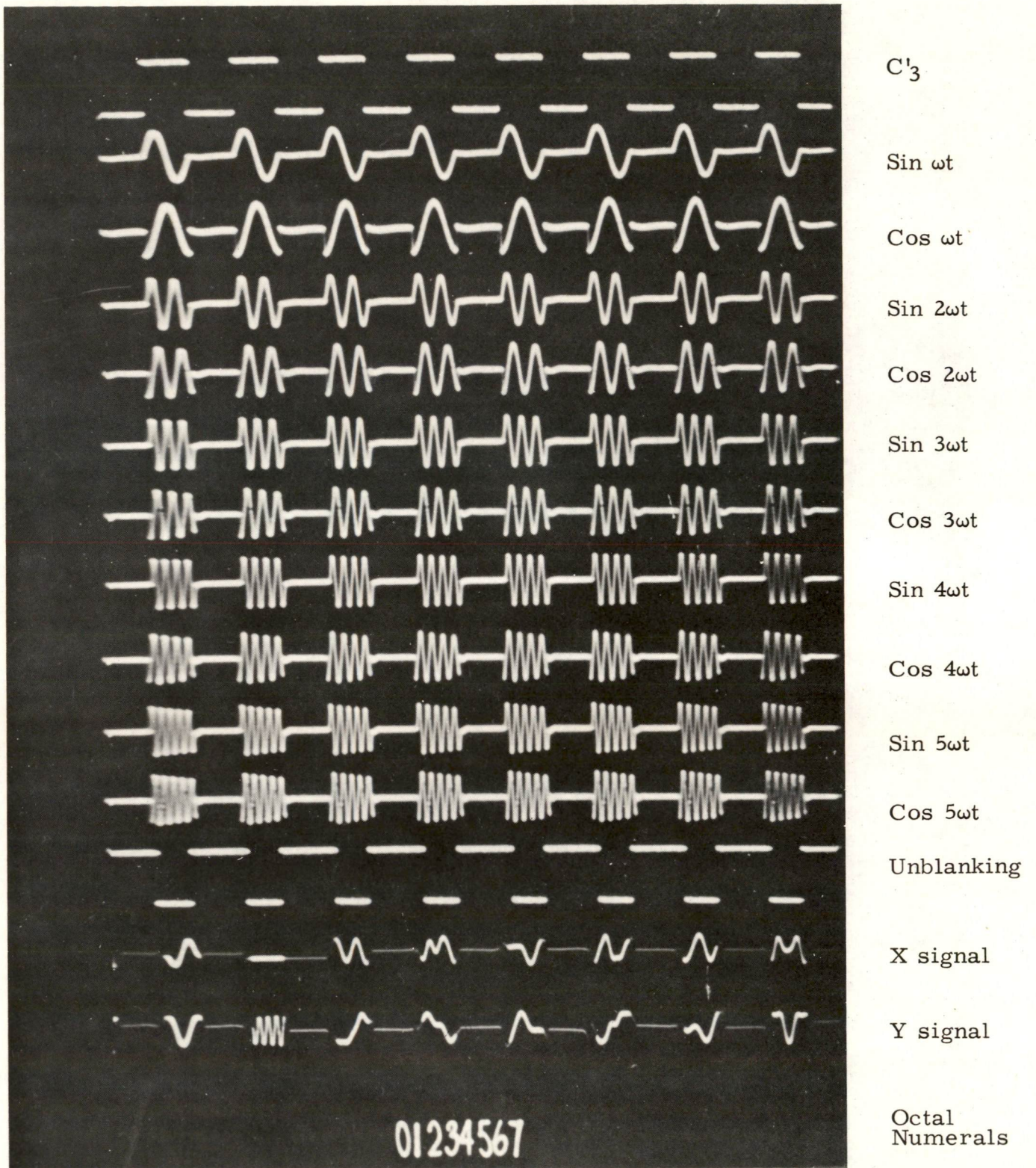


Figure 12. Waveforms



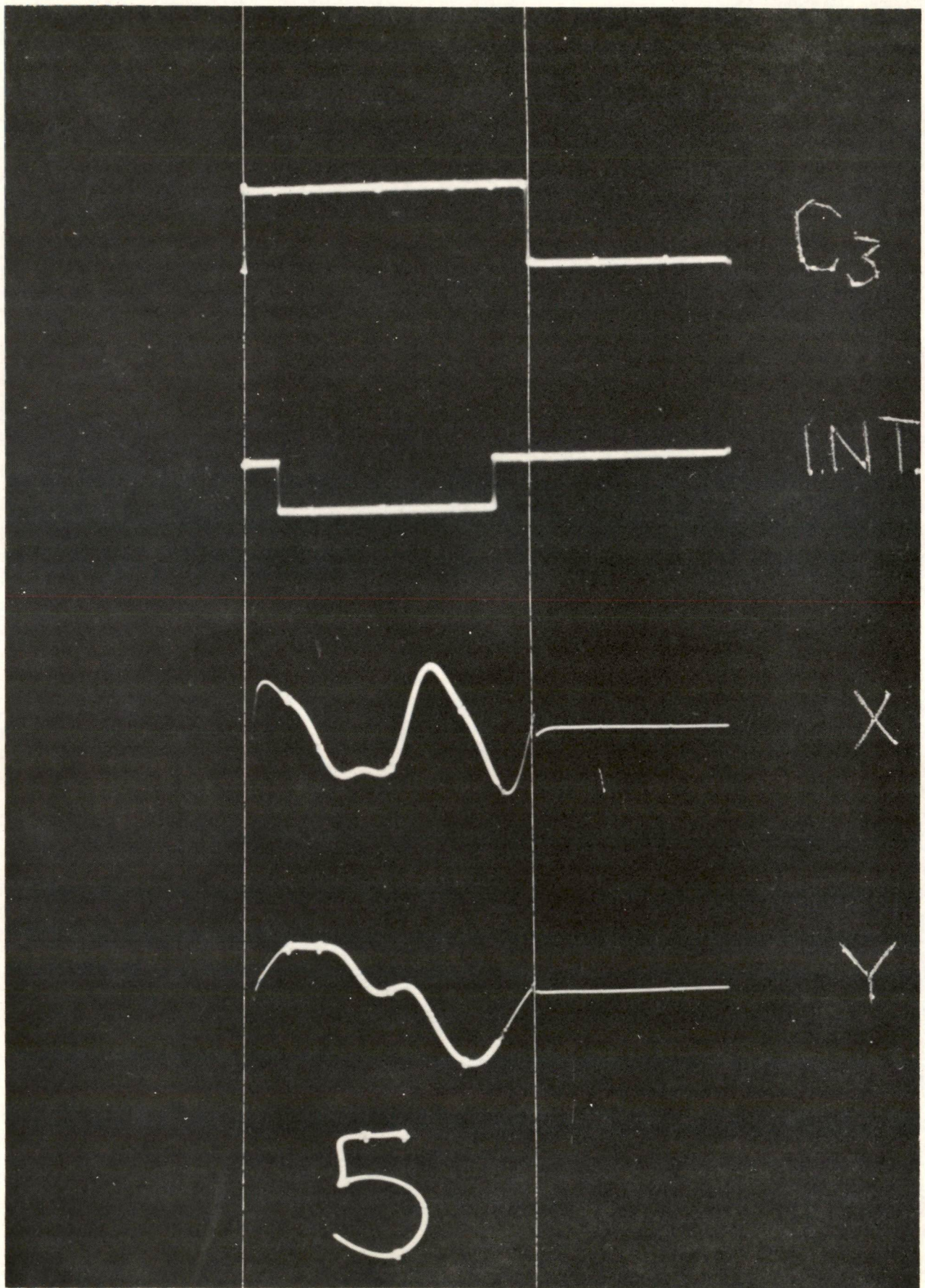


Figure 13. Enlarged Waveforms for No. 5.



01234567 01234567  
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01234567 01234567

Figure 14. Octal Numerals Tabular Display.



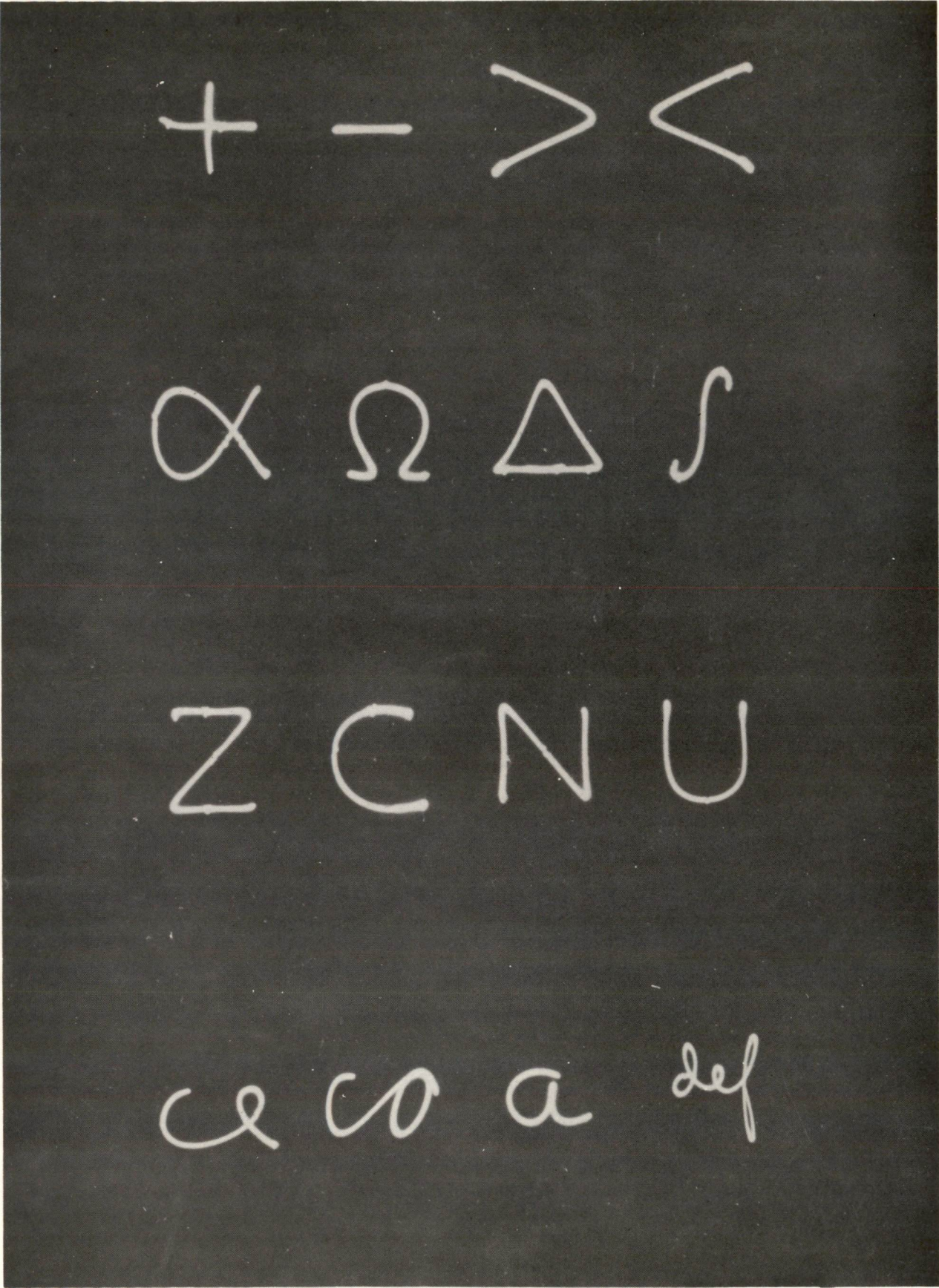


Figure 15. Miscellaneous Characters.



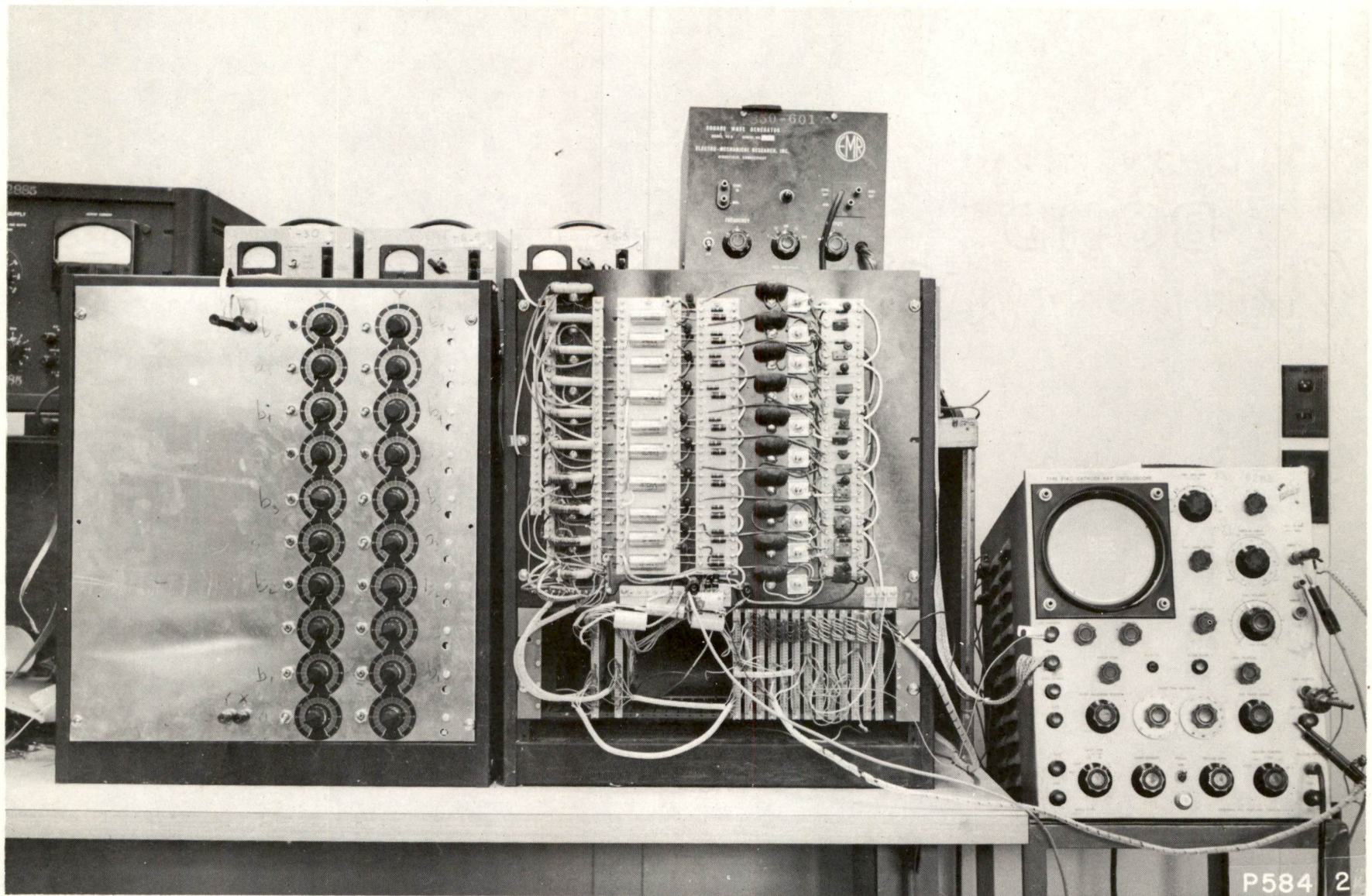


Figure 16. Photograph of Equipment.



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