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PLATED COMPONENT CONNECTIONS FOR MICRO-MINIATURE CIRCUITS

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LEXINGTON MASSACHUSETTS

PLATED COMPONENT CONNECTIONS FOR MICRO-MINIATURE CIRCUITS

by

Elis A. Guditz

ABSTRACT

A method of plating component connections is being developed which has application in etch-wired electronic circuits. Aside from the advantages of low weight and volume, and high temperature tolerance, plated connections are produced as a part of the circuit wiring itself.

Test samples have carried currents of a few microamperes to several amperes d-c while being subjected to temperature cycling for thirty five days. In other tests, units with plated component connections carried 3-amps d-c while the ambient temperature was increased, at a rate of 8°C per minute to 380°C, over twice the melting point of tin-lead eutectic solder.

Encapsulated transistor circuits with plated component connections were found to occupy considerably less volume than the same circuit produced on conventional print-wired boards.

I. Introduction

This paper is concerned principally with the evaluation of electrical connections made with chemically deposited copper.[1] Although the test samples to be described are not "microminiature," the use of the term in the title is justified by the fact that connection densities achievable by this technique are limited only by component size and the resolution obtainable from photolithographic processes.[2] During the course of the discussion an attempt will be made to answer the following questions:

(a) What constitutes a plated or deposited connection?
(b) How is copper chemically deposited?
(c) How good is a plated connection?
(d) What are some possible applications of plated connections?

II. The Plated Connection

Figure 1 is a dual flip-flop unit, a circuit type commonly used in digital computers. Its dimensions are 1" x 1 7/8" x 3/4". The 28 components, transistors, resistors, diodes, and capacitors were first coated with a resilient plastic and then encapsulated in epoxy resin. Of principle interest is the plated, or deposited, junction between each component lead and the etched wiring.

Figure 2 illustrates, more clearly, the composition of the connection. The component lead makes contact to a thin (under 50 micro-inches) layer of chemically deposited copper and, through this, to a thicker (approximately 0.001 inch) layer of electroplated copper. These copper layers are deposited on both faces of the unit and are later selectively etched to become the printed wiring. The electroplated junction between the the two layers of copper is commonly accepted as being a reliable electrical bond; the junction between the component lead and the chemically deposited copper is the subject of this evaluation.

III. Copper Deposition

Copper is deposited chemically, by procedures based on the early work of Narcus[3,4] from commercially available solutions.[5,6] The sample

to be plated is lightly sandblasted, cleaned in acid, then exposed to a sensitizing solution (such as tin chloride), followed by an activating solution (a noble chloride), and finally a copper-reducing solution. The resulting deposit is a fine-grained coating of high-purity copper which adheres well to both the component leads and the encapsulating plastic. Typical bond strengths of 25 lbs. per inch-wide peel are obtained. Deposition time is 15 to 20 minutes and temperatures do not exceed 100°C. A laboratory setup for deposition is shown in Fig. 3.

The copper adheres to properly cleaned and prepared component leads by chemical as well as mechanical bonds. The junction between the component lead and the chemically deposited copper resembles boundaries which exist between individual grains in polycrystalline metals. Figure 4 is a photomicrograph of a plated connection showing the component lead and the chemically and electrolytically deposited layers of copper. For comparison, a soldered connection is shown in Fig. 5.

Connections have also been made in which the initial contact layers consisted of chemically deposited silver, gold, or nickel.[7] Still another type of connection[8] requires oxidation of the component lead ends prior to copper deposition; the oxide is reduced to metallic copper during the deposition step and results in a connection of exceptionally high bond strength (over 100 lbs. per inch-wide peel). All of the methods produced satisfactory connections. Chemically-deposited copper was chosen for the initial contact layer because subsequent etching is simplified when only one metal is involved.

IV. Tests and Applications

Figure 6 shows one of the first test specimens, a 2" x 2" x 1/4" phenolic-laminate board with 16 copper pins (1/16" dia.) pressed into holes. An initial contact layer of copper was deposited over the bottom surface (pins flush), followed by electroplating to bring the total copper thickness to about 0.001". Conventional printing and etching procedures removed the unwanted copper leaving eight pairs of pins connected by 16 plated connections and a set of printed wires. These were then series

connected by wires (AWG #18) soldered to the pin projections on the reverse side. A Kelvin bridge measured the total resistance of wires and connections (soldered and plated) at 0.049 ohms (at 30°C) or an average maximum value of 0.003 ohms per plated connection (neglecting wires and soldered connections).

Stability of connection resistance with respect to temperature cycling was verified by heating the sample from 22 to 60°C four times in 60 hours. After the test, no change in resistance could be measured. After thirteen months of shelf life the unit was again temperature cycled. A direct current of 3 amperes flowed through the connections which were monitored by relays. If the resistance of any connection increased beyond 3 ohms the associated relay would close, shorting the connection and recording the failure. The maximum temperature reached during the five-day test was 180°C, just under the melting temperature for eutectic tin-lead solder. Again, there was no measurable change in total connection resistance at the conclusion of the run. A few days later the sample was run to failure in a test in which the temperature was increased at a rate of 8°C per minute to a maximum temperature of 382°C. Clamp-type inter-pin connections were substituted for the solder connections on the back of the sample to withstand the high temperature, and again 3 amperes d-c was the test current. The test was interrupted on the second cycle, at a temperature (decreasing) of 240°C, when a copper pin expanded above the surface of the board, tearing a conductor; however, the plated connection remained intact. Figure 7 shows the sample after the test along with a similar untested sample.

Another test specimen is illustrated in Fig. 8. It consists of four wires encapsulated in a 1/2 inch cube of epoxy resin. Conductors are deposited on two faces of the cube, joining the wires as shown. Pairs of connections are monitored by soldering wires midway on the printed conductors, at the lettered points, and connecting them to the monitoring relays.

In all, a total of ten temperature tests were performed on the three test specimens. The first test has been discussed. The others were

similar except for the number of specimens and the duration of tests. Numbers of connections per test ranged from 4 to 120 and the tests lasted from 8 hours to 840 hours (35 days). Test currents ranged from 10 micro-amperes to 3 amperes.

In each test the temperature was increased until several connections opened. Examination revealed that connections failed at elevated temperatures because the expanding plastic tore the deposited conductor from the encapsulated wire. This is to be expected because the coefficient of expansion of unfilled epoxy resin is considerably greater than that of copper wire. This kind of failure is not relevant to the characteristic of the plated bond under investigation but it indicates a temperature restriction imposed by the choice of encapsulating material. By adding a non-conducting filler to the epoxy, such as talc or mica (15% by volume), expansion is reduced and the operating temperature is increased.

Significant connection failures, in these tests, were those in which impurities present at the junction of the wire and deposited copper did not permit the junction to follow the normal resistivity function of temperature for pure copper. In all but a few cases the plated connections did act as pure copper. Photomicrographic examination of some high resistance and open connections clearly indicated a lack of proper cleaning of the wires prior to copper deposition.

Four connections which survived temperature cycling were placed on life test carrying 3 amperes d-c continuously at room temperature. One connection has an initial contact layer of chemically deposited nickel, another gold, and two copper. This test has been running for over 4,000 hours without failure.

Additional data on plated connections are being obtained from their operation in the Lincoln Laboratory TX-2 computer. Transistors, packaged as in Fig. 9 have been soldered into several of the computer plug-in units. Each transistor is potted in a plastic cylinder along with three new lead wires. Two plated connections and a deposited wire join each transistor lead to a new lead wire. Nine of these transistors have each accumulated 432 hours of successful operation. The conductors in

this transistor package lie in grooves engraved in the plastic. After copper was deposited, the surface was abraded leaving the metal only in the grooves, thus eliminating the need for applying acid resist, exposing, and etching as in the photographic process.

One of the first complete circuit assemblies to be made with plated connections was the transistor emitter-follower shown in Fig. 10. The resistor and transistor leads and the terminals were pressed into holes drilled in the phenolic-laminate board and cut off flush with the bottom surface. Copper was deposited, coated with acid resist, and selectively exposed, developed and etched to produce the required connections and wiring.

The dual flip-flop of Fig. 1 differs from the emitter-follower in that the components are completely encapsulated in plastic. Phenolic-laminate boards provide surfaces for the etched wiring and holes to position the component leads. Later, the boards were eliminated and the wiring deposited directly on the plastic. Holes in the encapsulating mold positioned the component leads.

A tester was built to supply power and operating pulses to the flip-flop and to count and record the number of times it failed to respond properly to the driving pulses. Exclusive of power failures and one intermittent plug, the flip-flop has been operating successfully for over six months.

The flip-flop package has been vibrated while monitored by the tester. Vibration was in a direction normal to the etched wiring at frequencies from 10 to 3200 cps for 5-g increments of force until a value of 60 g was reached. Maximum peak-to-peak displacement during the 5 1/2 hour test was 0.2 inch at 75 cps. No errors in operation occurred and the flip-flop was undamaged.

Figure 11 is a drawing of a plug-in unit presently under construction. An important requirement of this unit is that the mobility of the plug pins be retained after encapsulation. The back of the plug is cast in a volume of resilient plastic which is later cast in solid plastic along with the electrical components. Lead wires from the plug

are brought up to the surface and treated as component leads. Copper, chemically deposited over both faces, forms plated connections to the component leads. This is followed by an electroplated layer to the thickness required for conductors. Conventional etched wiring procedures produce the desired inter-connections. Development plans include the use of foam plastics to reduce weight.

The four views of Fig. 12 represent consecutive steps in processing another form of plated connection. To the board shown at the upper left has been added a deposited and electroplated "ground plane" which is connected to a corner pin by a plated connection (upper right). All other pins have been isolated from the ground plane by a photo-etch operation. A thin layer of epoxy resin over the ground plane supports a set of deposited photo-etched conductors which join pairs of pins together by plated connections (lower left). A second layer of resin supports additional deposited photo-etched conductors which join the unconnected pairs of pins to form a two-level series circuit over the copper ground plane (lower right). A finished board was cut, sanded, and polished to show half-pins and 4 layers of conductors and connections (Fig. 13). This technique makes possible the deposition of strip "transmission line" in which the characteristic impedance is a function of the conductor width and the thickness of the insulating plastic. Layers of epoxy resin 0.015 inch thick have been laid down on a 10" x 12" board with thickness controlled to plus or minus 0.001 inch. Each consecutively cured layer consists of a measured weight of fluid resin poured onto the board (surrounded by a fence) while it rests on a level stand in an oven.

A proposed application of multi-layer transmission-line wiring with plated connections is pictured in Fig. 14. Shown are encapsulated units plugged into a wiring board module containing two separate levels of transmission line wiring. Plug receptacles extend to the rear of the board as pins of sufficient length to accommodate any number of wiring levels required. Each layer of ground plane, dielectric, and conductors, is processed and tested consecutively. A proposed assembly for an electronic computer would consist of approximately 1-ft.^{2} frame-mounted

modules of deposited wiring (and associated plug-in units) interconnected by plugs and cables.

V. Conclusions

This work represents an effort to evaluate plated connections by comparing them functionally to soldered connections. As such, it is far from complete; however, a beginning has been made and results of the several tests indicate the potential usefulness of the technique.

Plated connections can withstand high temperatures provided consideration is given to the materials supporting circuit components and wiring. They are well suited for use in rugged, encapsulated circuit assemblies where the achievable high connection densities enhance the possibilities of miniaturization. The fact that plated connections can be made without subjecting components to temperatures above 100°C is an advantage when low-wattage components are used.

Future work should include determination of the low-temperature capability of the connection, as well as more high-temperature testing. Data on quality uniformity among large numbers of plated connections is needed and more extended life tests under conditions of actual equipment operation should be made. Also, a better understanding is desired concerning the nature of the bond between the component lead and the copper deposit. And, not least, consideration should be given to new approaches to packaging, made possible by this new technique, at both the circuit and system levels.

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8. E. B. Murphy, Massachusetts Institute of Technology, Lincoln Laboratory, (unpublished work).

LIST OF FIGURE CAPTIONS

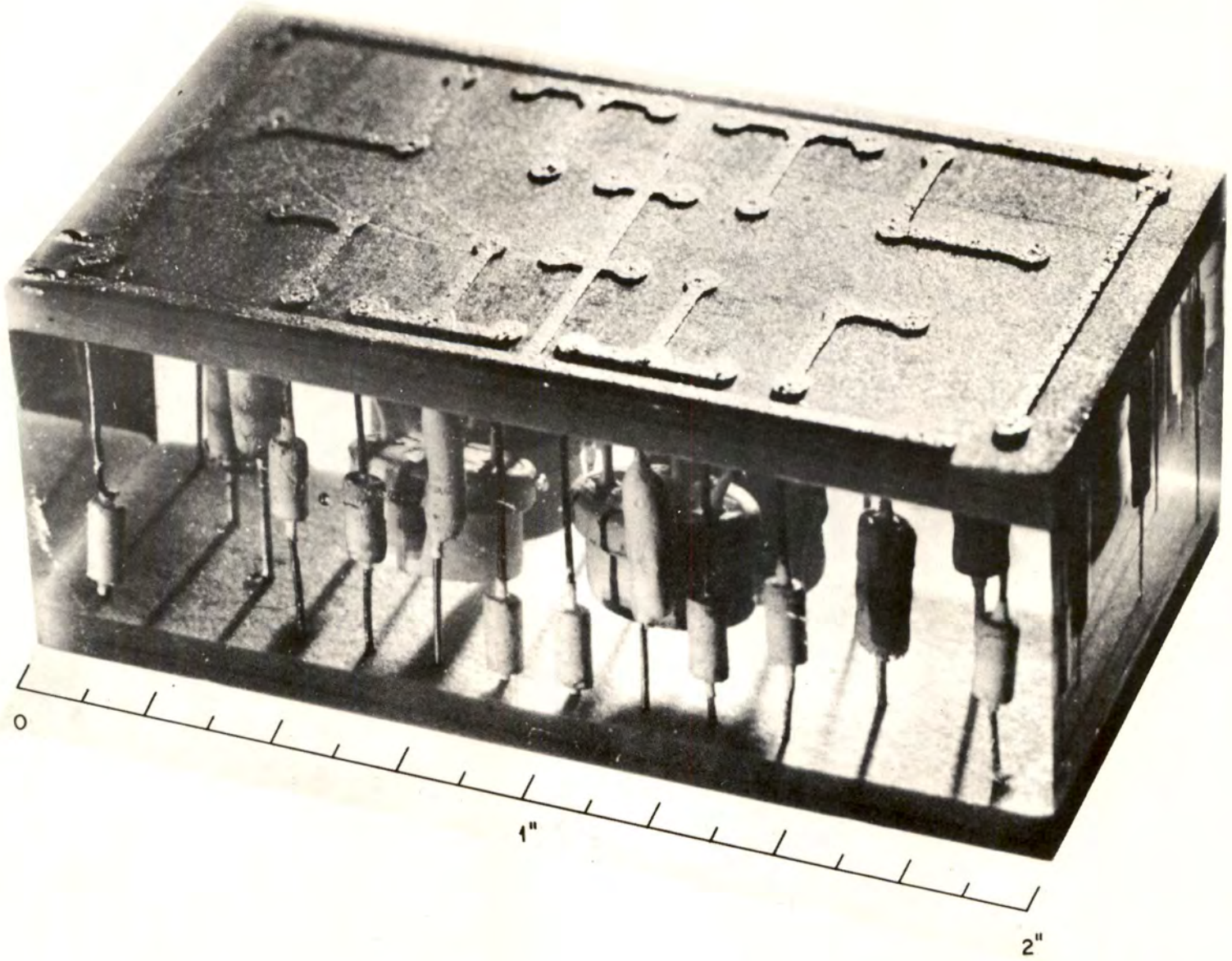

Fig. 1 - Encapsulated electronic circuit with components interconnected by plated connections and etched wiring.

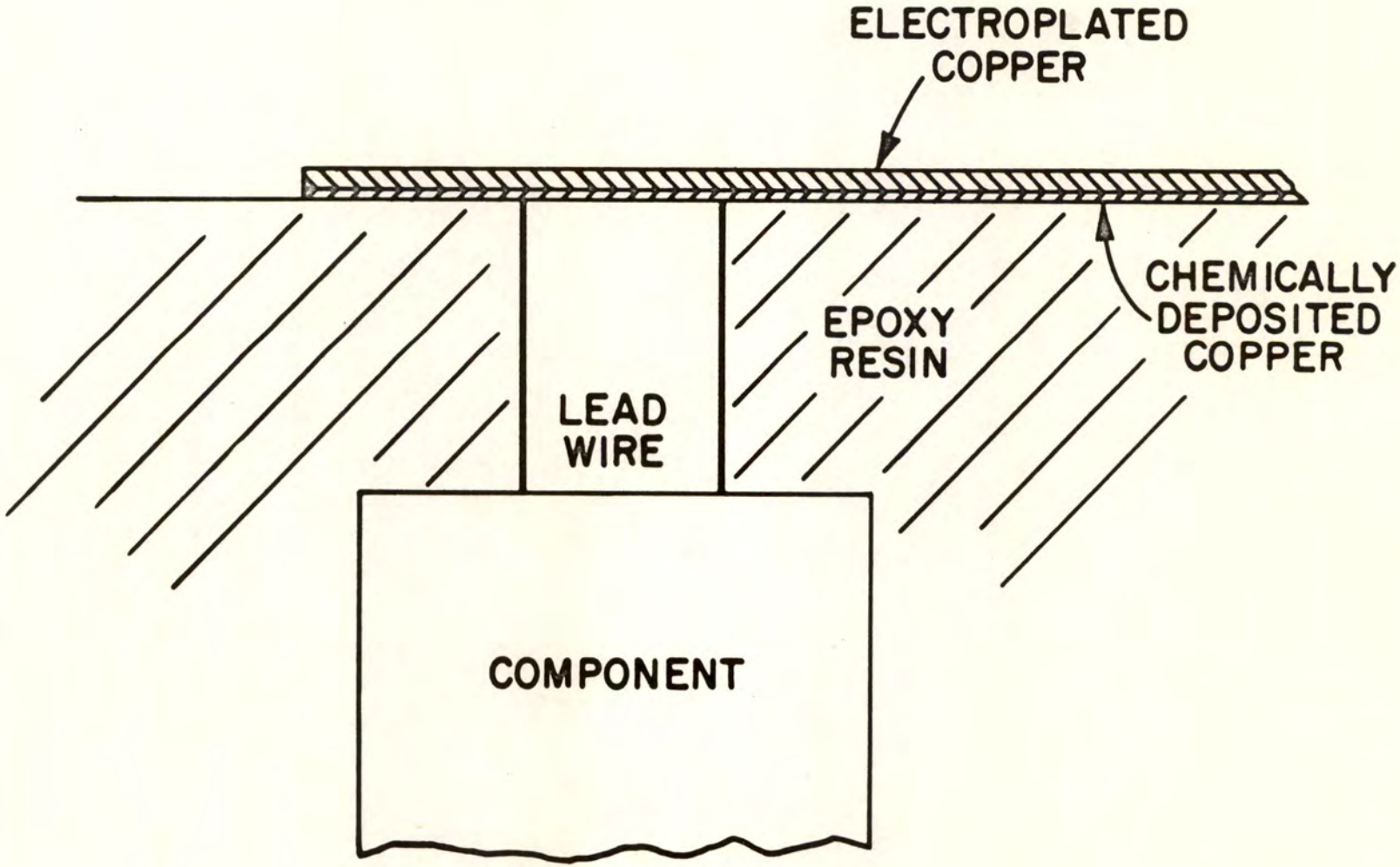

Fig. 2 - Composition of a plated connection.

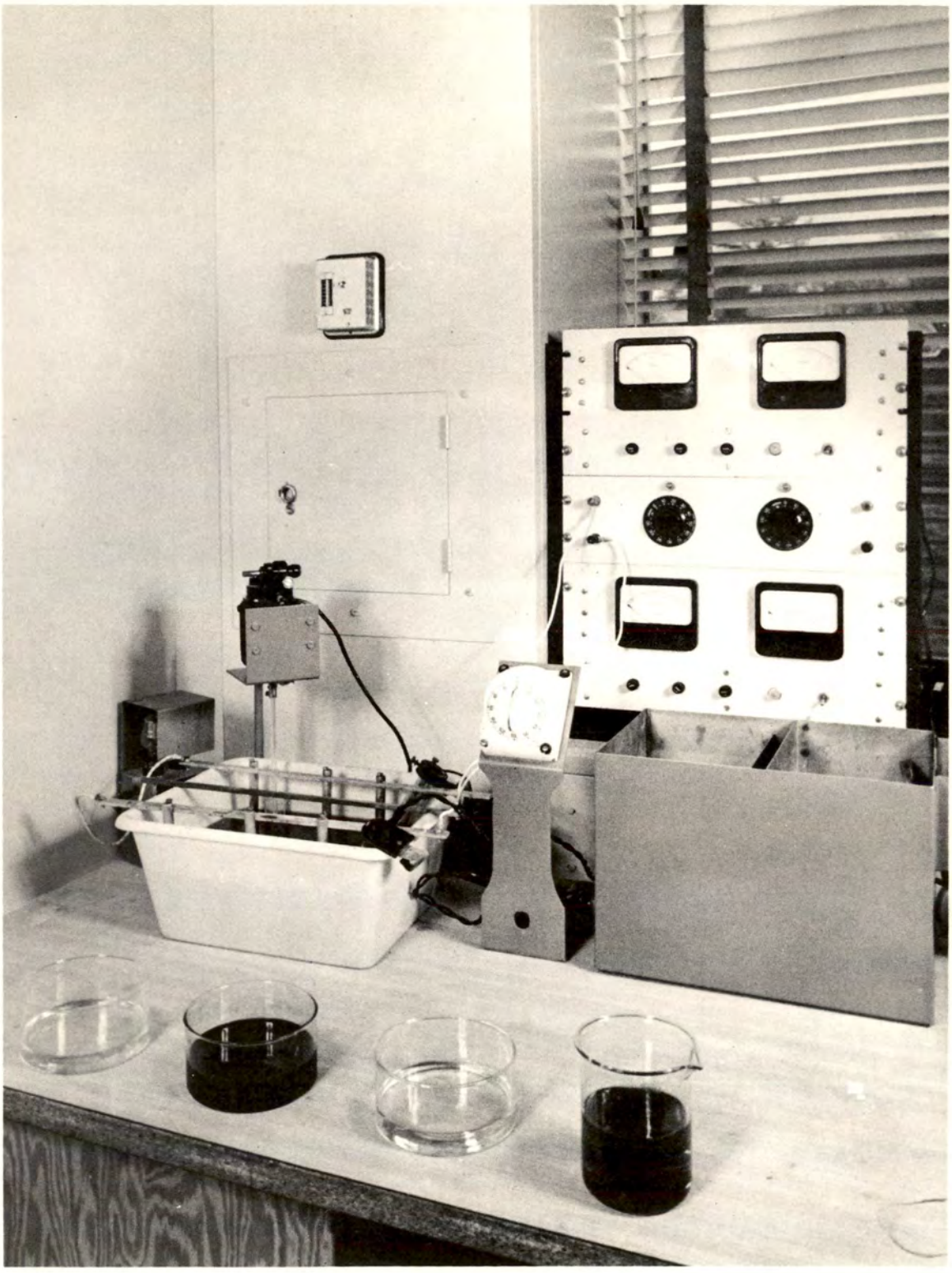

Fig. 3 - Laboratory setup for making plated connections.

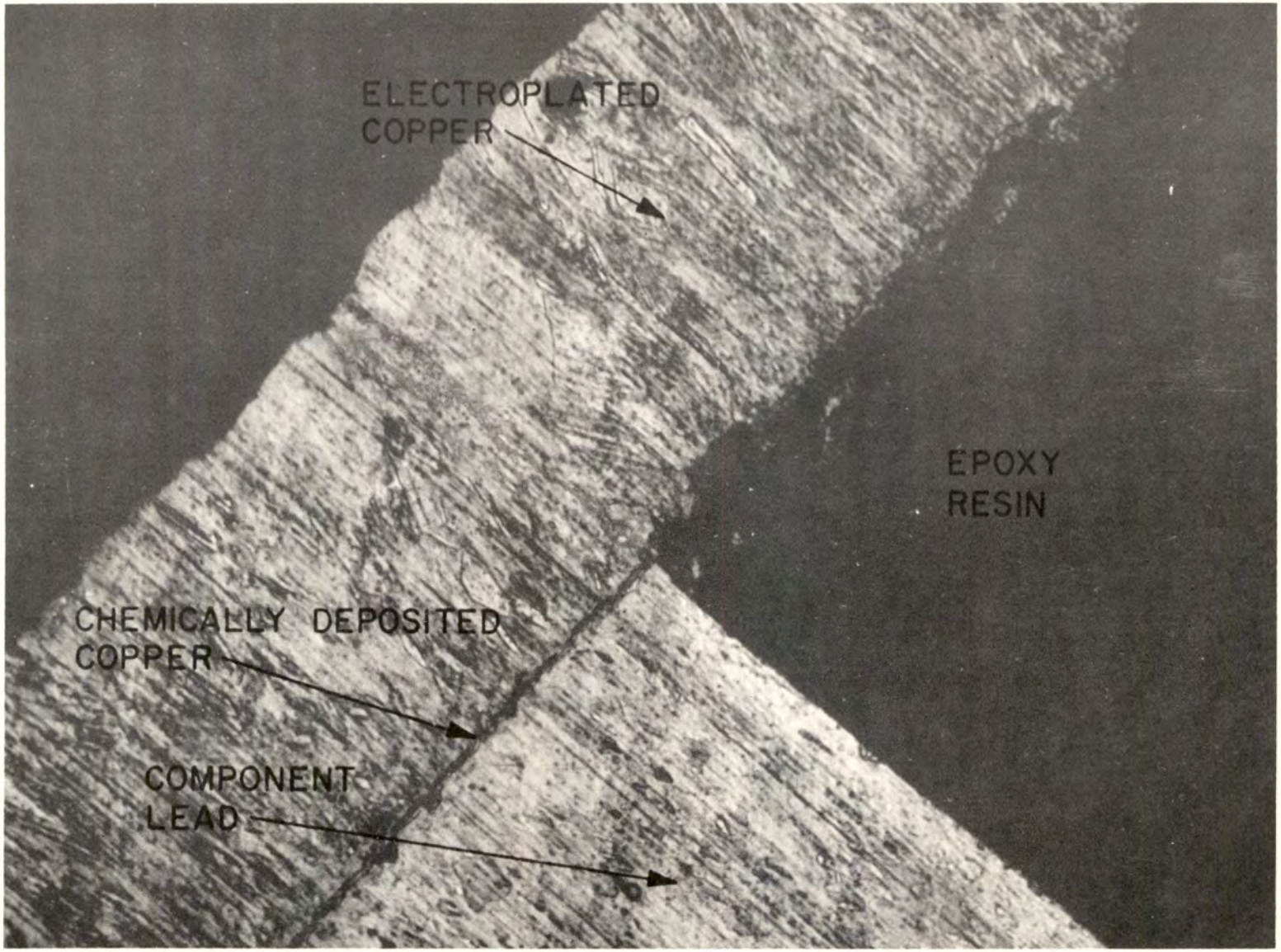

Fig. 4 - Photomicrograph of a plated connection at 315X magnification (on 4" x 5" plate).

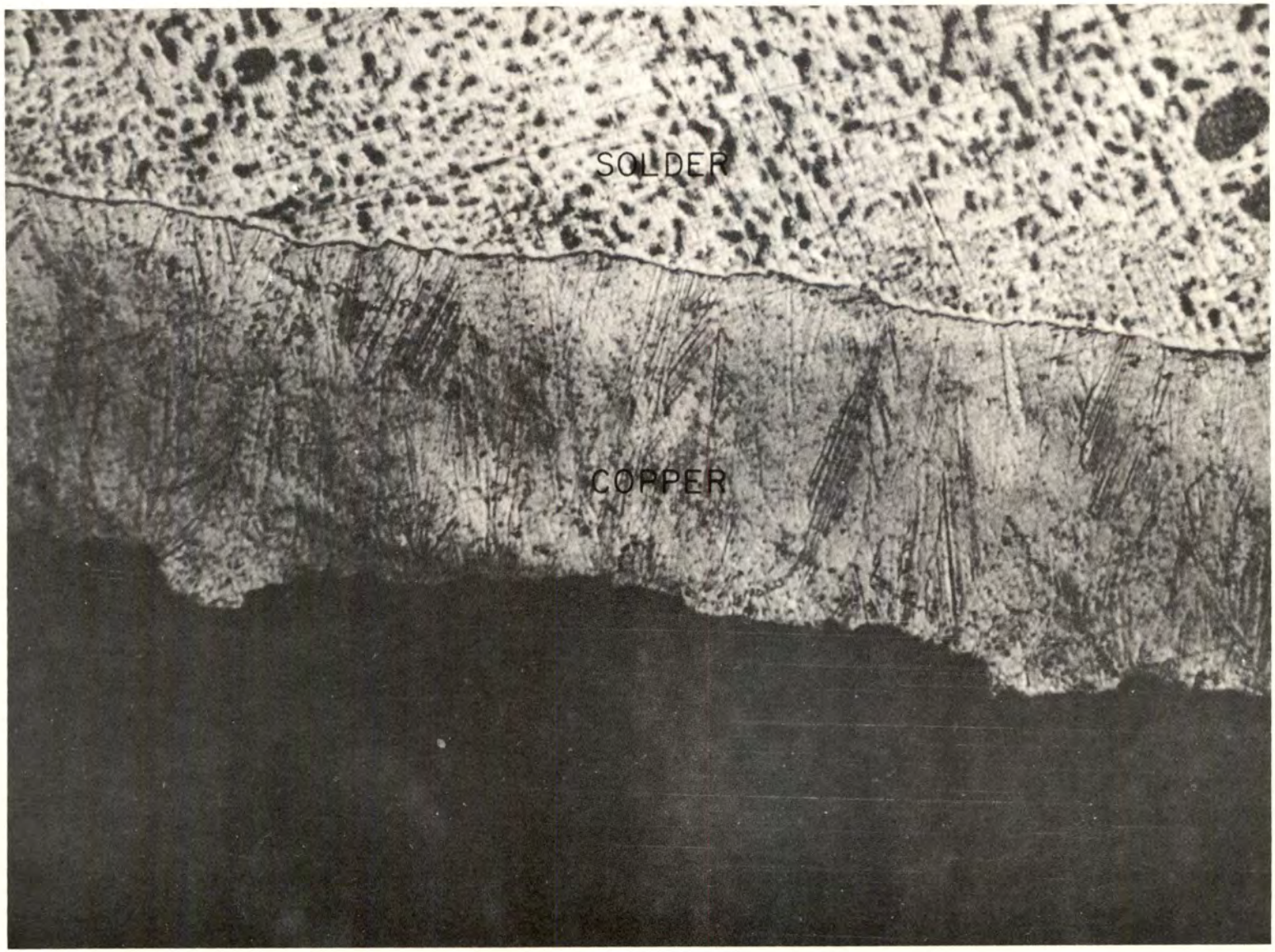

Fig. 5 - Photomicrograph of a soldered connection at 315X magnification (on 4" by 5" plate).

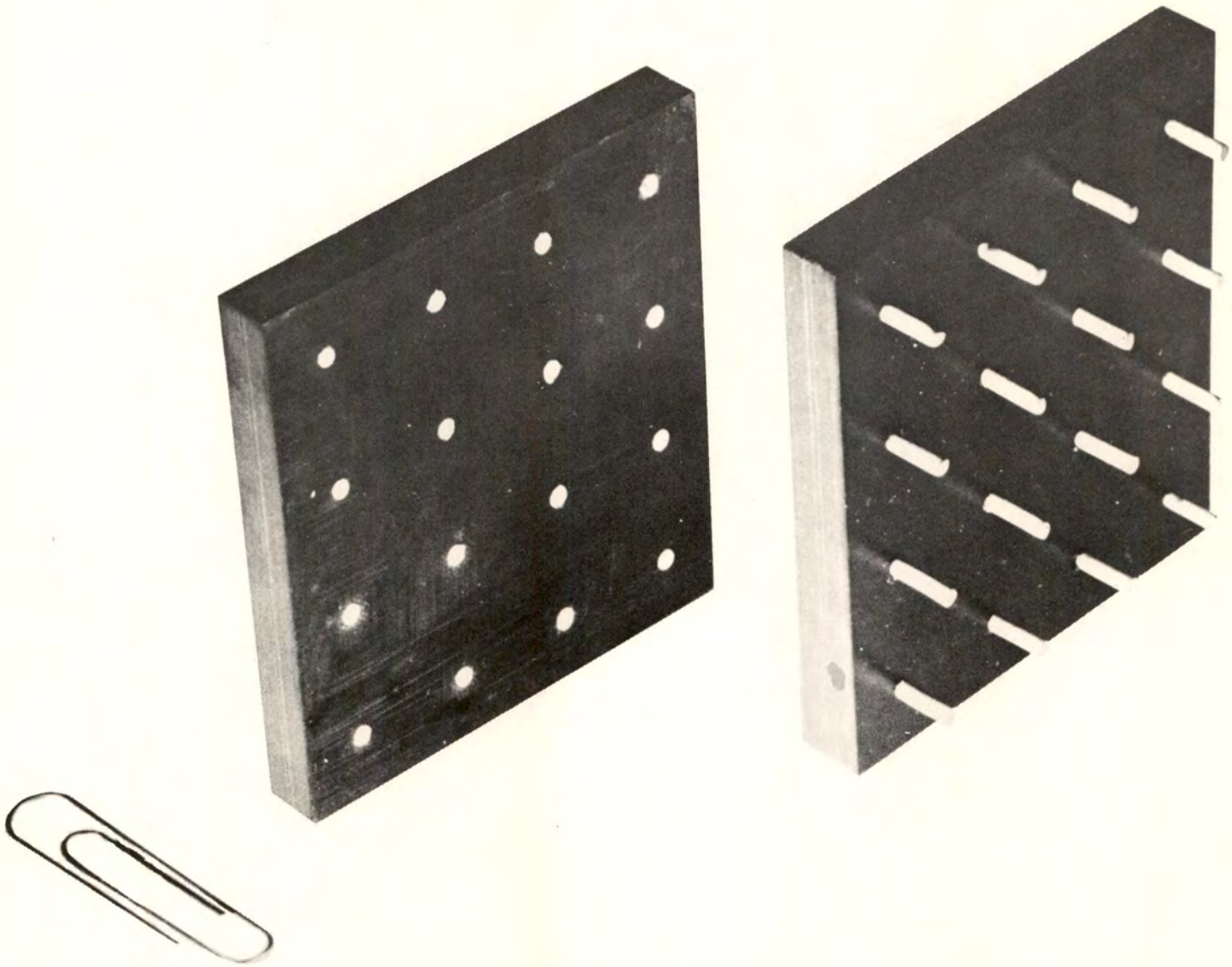

Fig. 6 - Sixteen-connection test sample before copper deposition.

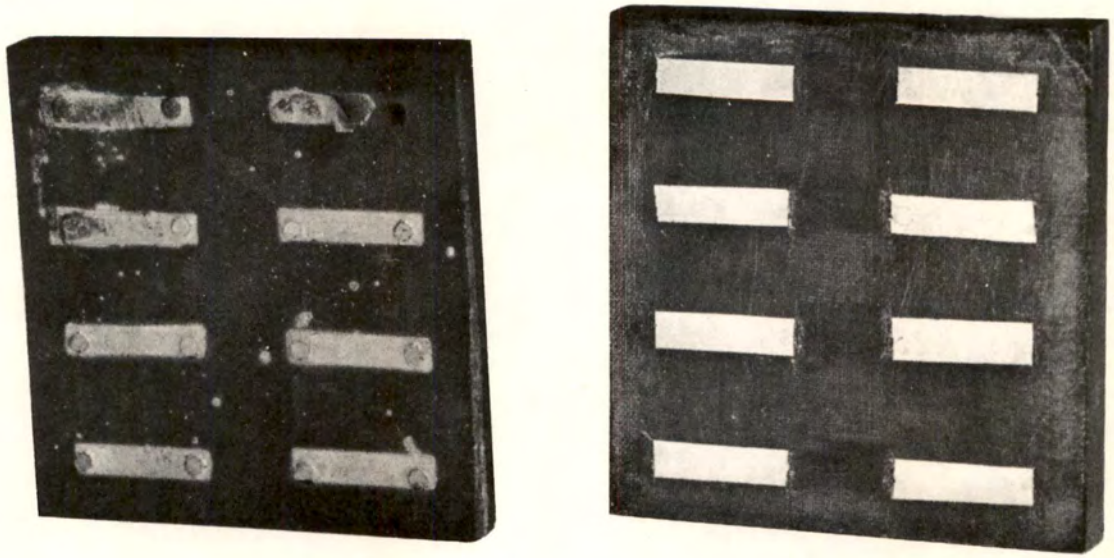

Fig. 7 - Sixteen-connection sample after 382°C. temperature test (left)
Similar sample, untested (right).

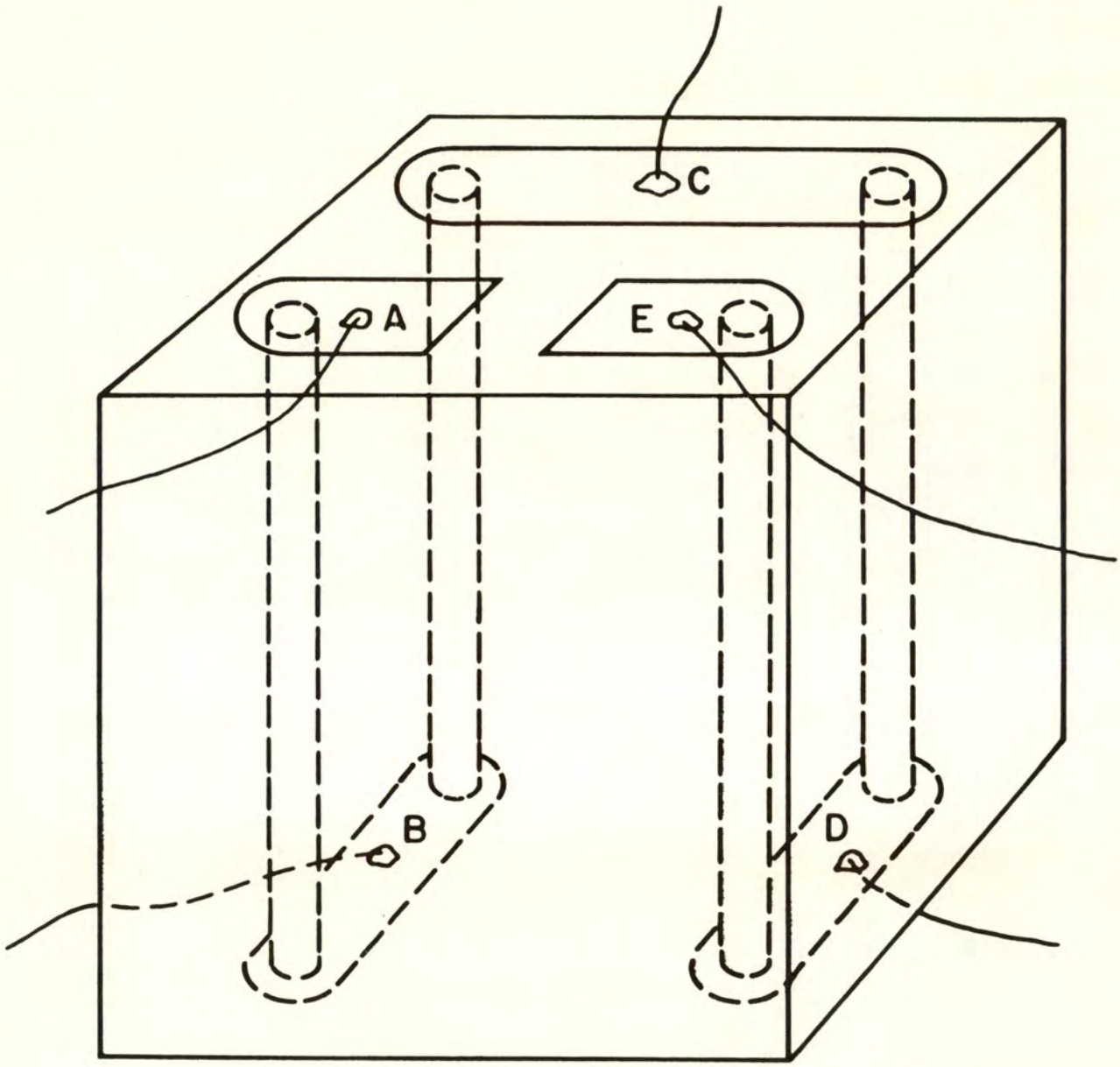

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Fig. 8 - Plastic test cube with four encapsulated wires and eight plated connections.

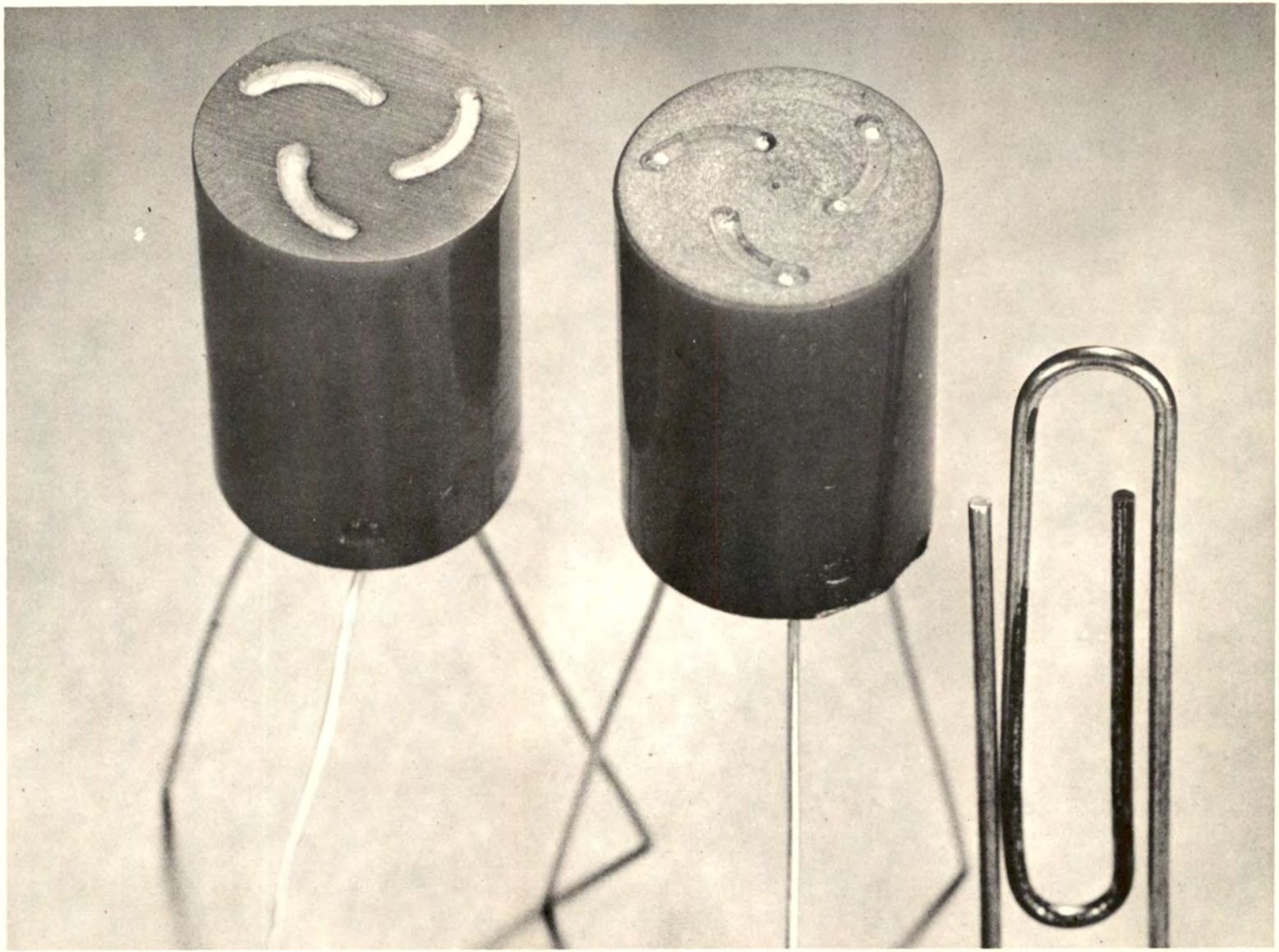


Fig. 9 - Transistor potted with extra leads (right). Plated connections and wires join lead wires for test of plated connections (left).

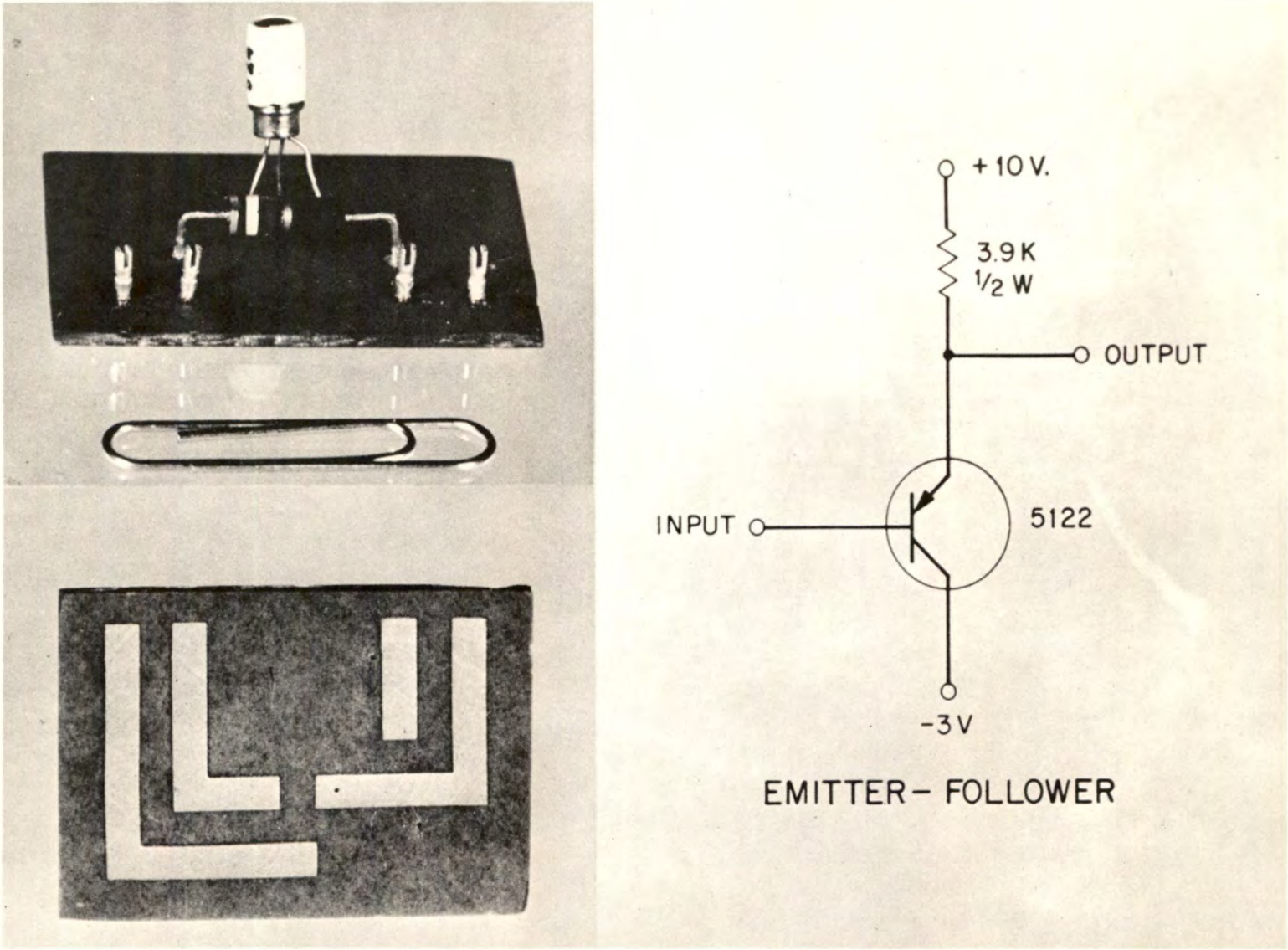


Fig. 10 - Components of emitter-follower circuit interconnected by plated connections and etched wiring.

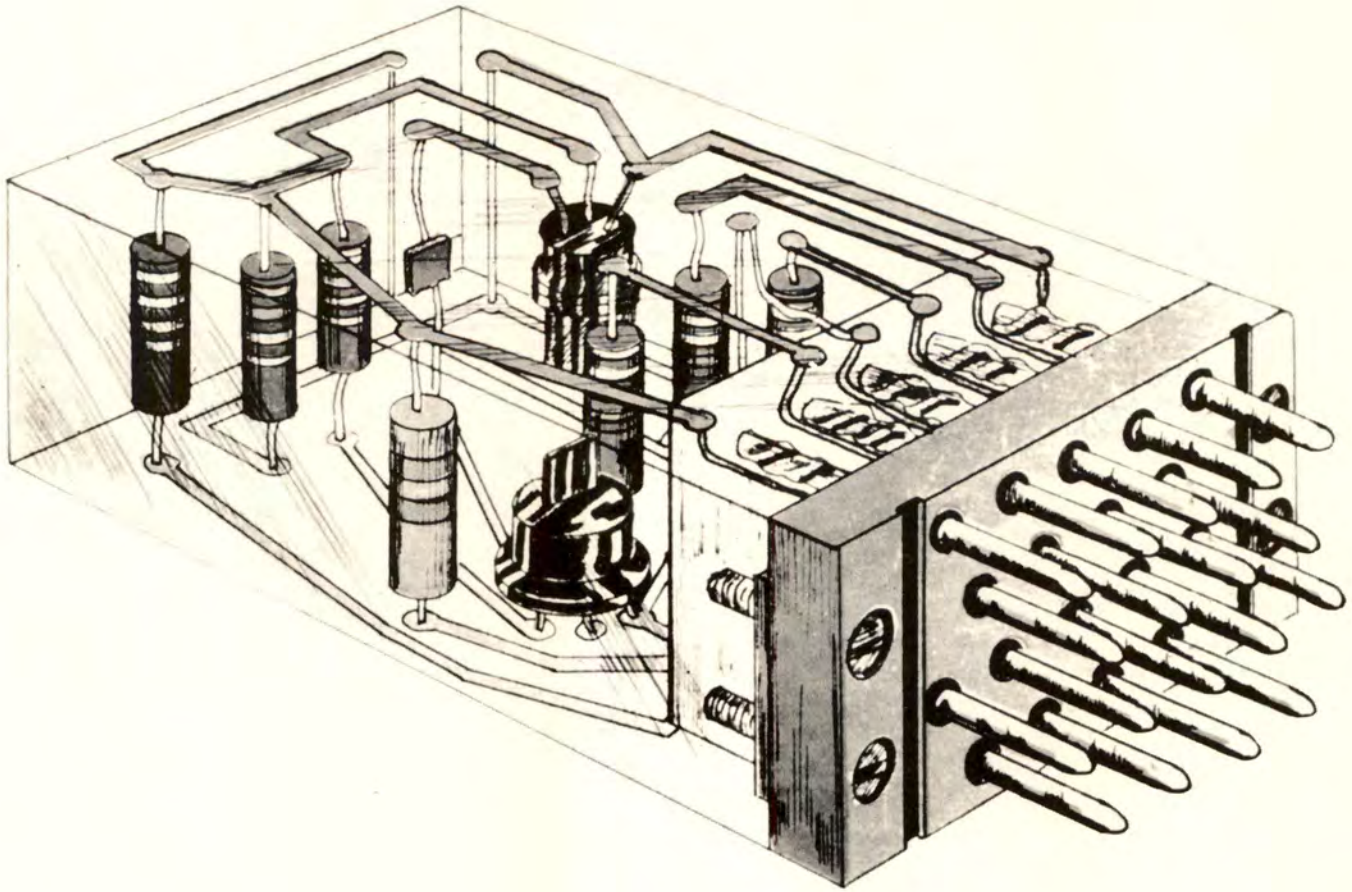


Fig. 11 - Drawing of proposed plug-in unit employing plated connections.

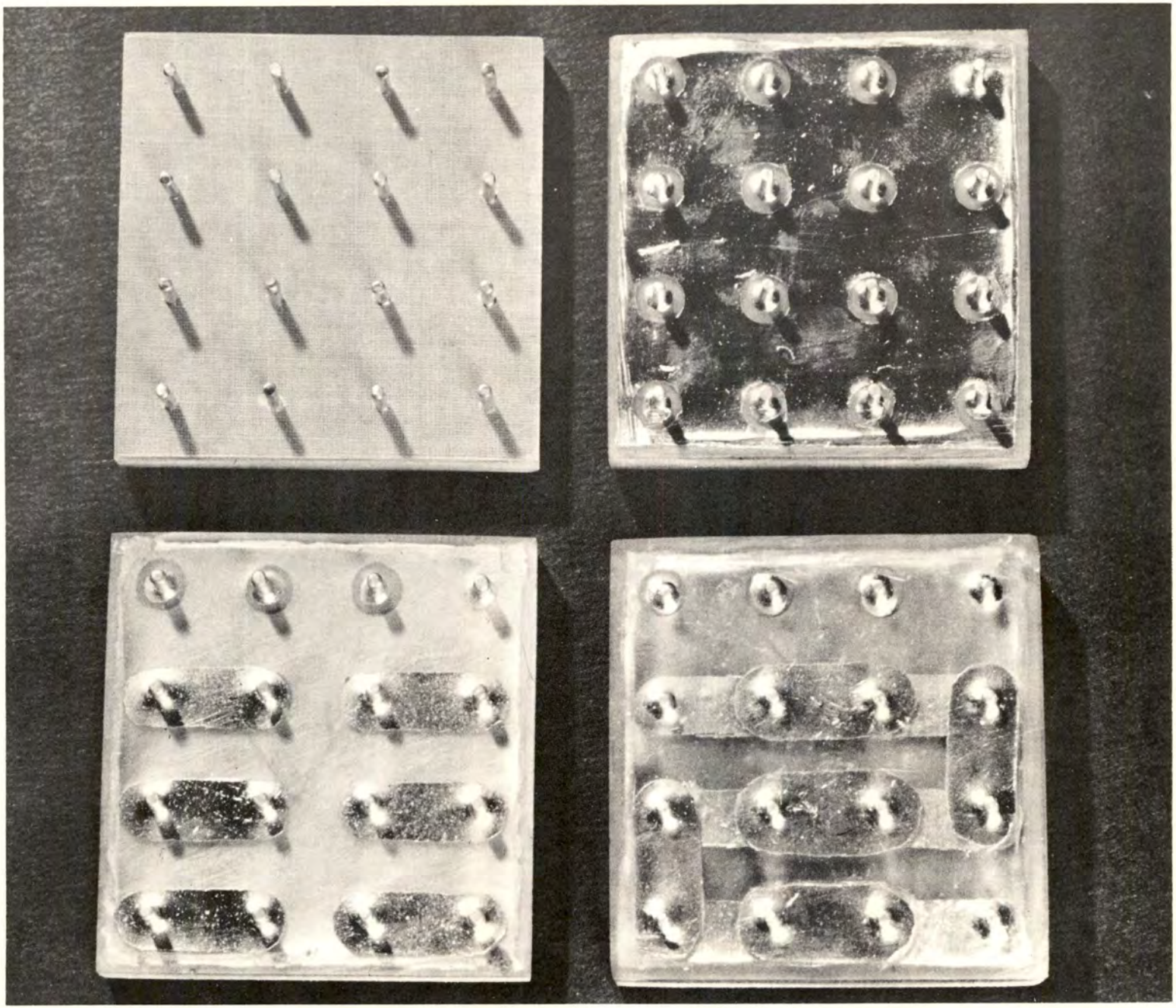


Fig. 12 - Successive stages in production of multi-layer deposited wiring with plated connections to copper pins (upper left to lower right).

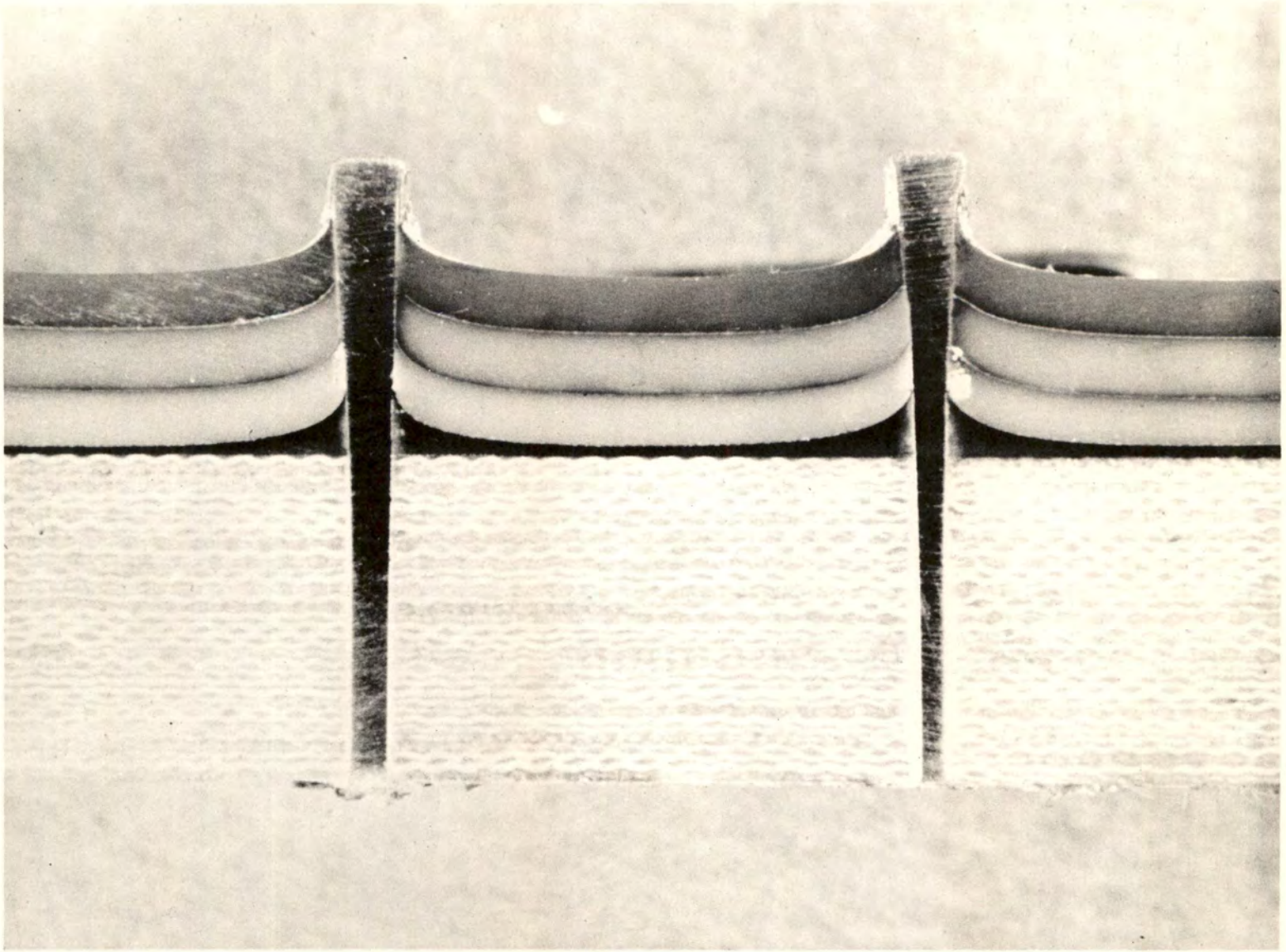


Fig. 13 - Section view of multi-layer deposited wiring with plated connections to copper pins 0.5 inch apart.

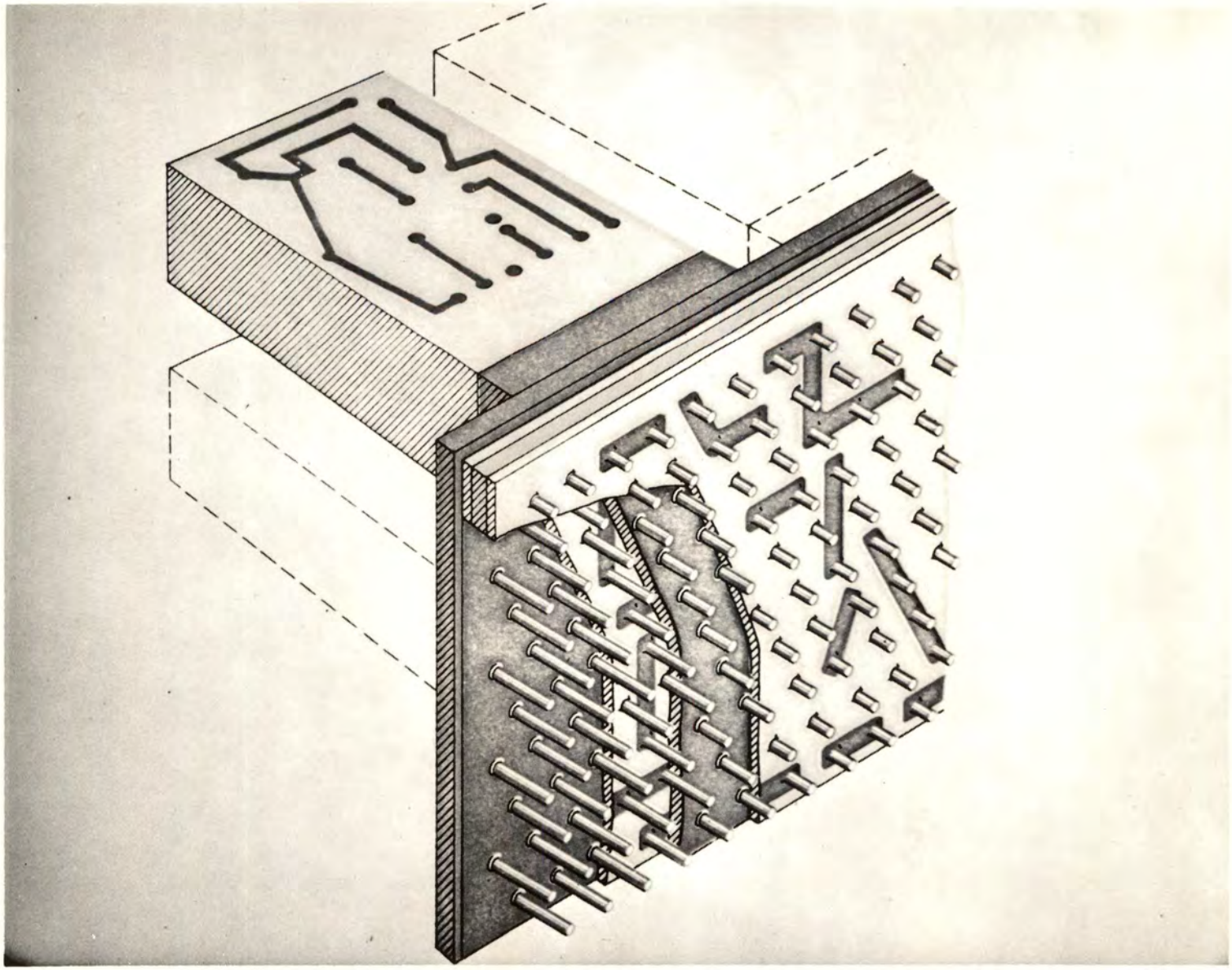
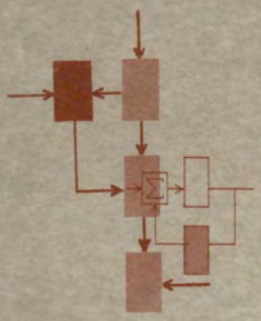


Fig. 14 - Proposed wiring board of multi-layer "transmission line" wiring with plated connections to metal pins.



THE DESIGN OF HIGH SPEED ANALOG SAMPLE AND STORAGE GATES

by

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MS Thesis August, 1959

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THE DESIGN OF HIGH SPEED ANALOG SAMPLE AND STORAGE GATES

by

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(1958)

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(1959)

Signature of Author_____
Department of Electrical Engineering, August 24, 1959

Certified by_____
Thesis Supervisor

Accepted by_____
Chairman, Departmental Committee on Graduate Students

THE DESIGN OF HIGH SPEED ANALOG SAMPLE AND STORAGE GATES

by

RONALD ERIC GOCHT

Submitted to the Department of Electrical Engineering on August 24, 1959 in partial fulfillment of the requirements for the degree of Master of Science.

ABSTRACT

A pulsed analog computer has been proposed which requires the use of analog gates. In order to solve the real time flight simulation problem it has been estimated that components with a maximum deviation from linearity of 1% are required. The computer would operate at 100 KC with a program which is repeated at a 50 cps rate. The purpose of this thesis is to demonstrate that the construction of analog gates capable of meeting the requirements of this system is within the realm of present day technology.

An organized procedure is developed whereby sample gates (impulse modulators) are analyzed. Several diode and several transistor gates are analyzed in great detail, including a prediction of gate linearity from a non-linear model of the gating elements. Several sample gates are found which would be capable of meeting our requirements, the simplest of which is the two bilateral transistor gate. A method for including the sample gate in a closed loop with an operational amplifier to improve linearity is demonstrated. Measurements of sample gate linearity are made in both DC and pulsed situations.

A similar procedure is developed whereby storage gates (clampers) are analyzed. Several storage gates are analyzed but only one, the four diode bridge gate, is found to be capable of pulsed analog applications. An interesting result of the discussion of storage gates is the fact that a certain class of these gates are perfectly linear. Measurements of a storage gates abilities are made by several methods, including a closed loop method which multiplies gate errors until they are easily measured.

Thesis Supervisor: George C. Newton

Title: Associate Professor of Electrical Engineering

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CHAPTER I

INTRODUCTION AND SUMMARY

1.1 ANALOG GATES, APPLICATIONS AND DEFINITIONS

The use of pulsed or time sharing schemes with analog computing equipment is becoming more popular and more practical each day. In some cases this analog equipment may consist of only an analog output tied to a digital computer.[1] In other digital computers analog equipment may be a part of the computing loop, in which case both input and output to and from the analog world are demanded.[2] Techniques in which analog equipment is conserved by time sharing have been developed. A pulsed analog computer has been proposed in which all arithmetic operations are performed in the analog domain but whose program is controlled digitally.[3,4] In all of these systems high speed analog gates are either required or could be profitably used.

There are two basic types of analog gates; the sample gate and the storage gate. Both of these gates are three terminal pair devices as shown in Fig. 1-1. These gates have two states; the enabled state and the disabled state. E_T is a trigger voltage which is bivalued. E_i is a continuous input voltage. E_o, the output voltage, depends on the state of the gate. The ideal sample gate will have an output voltage E_o equal to the input voltage E_i during the enabled periods and will have an output voltage of zero during disabled periods. An ideal storage gate will assume an output voltage equal to the input voltage during enabled periods and will retain this voltage during the following

[1] Superscript numbers refer to references listed in the Bibliography.

disabled period regardless of the value of E_i. Real gates, as we shall see, vary from these ideal characteristics in many ways.

1.2 THE PULSED ANALOG COMPUTER

As these gates are to be designed for use in a pulsed analog computer it would be worthwhile to briefly discuss this computer. From this discussion of the pulsed analog computer we can determine the specifications to which the gates must be designed. The pulsed analog computer combines analog and digital computing techniques. Where a digital computer performs discrete operations on discrete variables, and an analog computer performs continuous operations on continuous variables; the pulsed analog computer performs discrete operations on continuous variables. From this point of view it is a digital computer with arithmetic operations performed in the analog domain. A set of differential equations will be solved by a repetitive procedure similar to techniques now employed in obtaining a digital solution.

A block diagram of a simple example of a pulsed analog computer is shown in Fig I-2. The inverter, summer, multiplier, and integrators are standard analog equipment, except that they are capable of operation at high speeds. The inputs to these arithmetic elements are connected to the outputs of storage gates. The outputs of these arithmetic elements are connected to the inputs of sample gates. The sample gates outputs are actually connected to summing resistors which form the input to the inverter, and not to a common bus as the block diagram would indicate. The gates are triggered from the digital control unit. An instruction in the computer program will trigger two gates simultaneously; a sample gate and a storage gate. This operation will

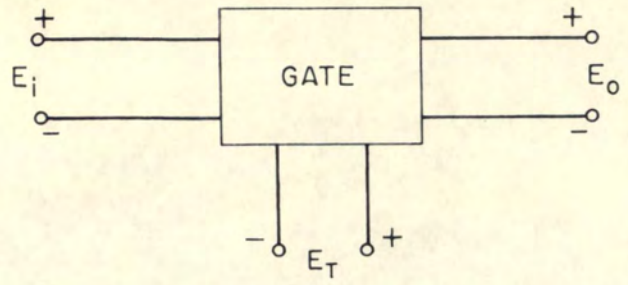


Fig. 1-1 A Gate is A Three Terminal Pair Device

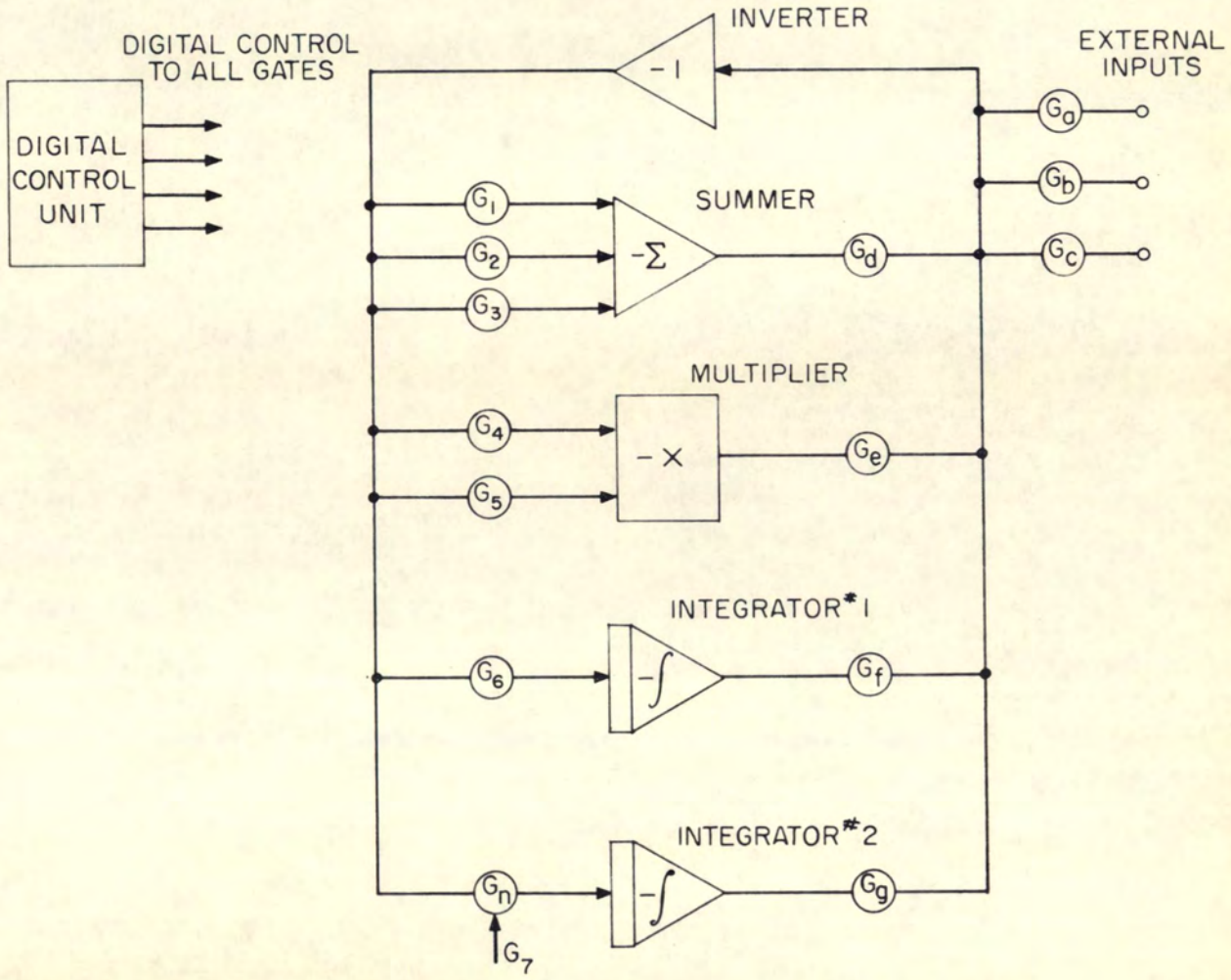


Fig. 1-2 A Pulsed Analog Computer

transfer the input voltage of the sample gate to the output of the storage gate.

To better demonstrate the operation of the pulsed analog computer it will be instructive to follow through a sample program. For example we may want to solve the second order differential equation $\ddot{x} + b\dot{x} + w^2x = f(t)$. The program can be written by following a procedure similar to those employed in drawing a block diagram for an analog computer program. That is, the equation is first solved for the highest derivative, and then, assuming that we know this highest derivative we can proceed to compute the quantity $-w^2x - b\dot{x} + f(t)$. The equality is completed by routing this computed quantity back to the point where we started with $\ddot{x}$. Fig. I-3 is the block diagram for the analog computer solution of this equation.

A program for the pulsed analog computer is written by following the same procedure. The input to integrator number 1 will be assumed to be $\dddot{x}$. By performing the instruction G_fG_7 the guantity $\ddot{x}$ is placed at the input to integrator number 2 and we now have available both $-\dot{x}$ and $-\dot{x}.b$, w^2, and $-f(t)$ are available through sample gates G_a, G_b and G_c respectively. The next step in the program will be to compute $b\dot{x}$ by the following pair of instructions, G_fG_4 and G_aG_5. The quantity + bx is now available at the output of the multiplier and will be gated to the first input of the summer in preparation for the addition which must be performed. By continuing this process we arrive at the following complete program. The last step in the program has completed the equality. Note that this program is not unique for the solution of this equation, but that several steps could

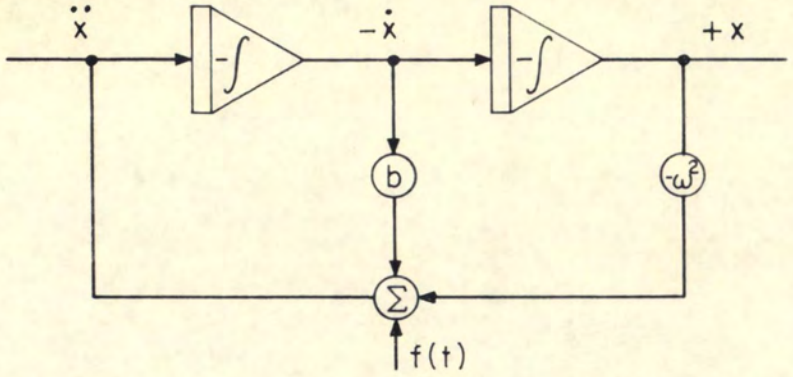


Fig. 1-3 Analog Computer Solution of $\ddot{x} + b\dot{x} + \omega^2 x = f(t)$

STEP #	INSTRUCTION	COMMENTS
1	$G_f\ G_7$	$\int \dot{x} = x$
2	$G_f\ G_4$	$b\dot{x}$
3	$G_a\ G_5$	
4	$G_e\ G_1$	$-b\dot{x} - \omega^2 x + f(t)$
5	$G_g\ G_4$	$\omega^2 x$
6	$G_b\ G_5$	
7	$G_e\ G_2$	
8	$G_c\ G_3$	
9	$G_d\ G_7$	COMPLETES EQUALITY

Fig. 1-4 Program for pulsed analog solution of $\ddot{x} + b\dot{x} + \omega^2 = f(t)$

have been interchanged. This program has illustrated how analog equipment can be time shared. The multiplier computed both the products bx and $\omega^2 t$. While not very apparent from this simple example, in a more elaborate problem this sharing of analog elements would result in a considerable saving of equipment.

1.3 GATE SPECIFICATIONS

In both the all-digital and the pulsed analog case, both the length of time required for one instruction and the number of instructions in the program are important when real time solutions are demanded. There is an error introduced into the total solution because of the discrete manner in which the pulsed analog computer has produced the solution. The steps of the program must be run through many times for each cycle in the solution of the differential equation in order to obtain an accurate answer. An exact analysis of this effect is difficult even for this simple case. Nevertheless it has been estimated that for the real time simulation of high performance aircraft (which is the motivating force in designing this computer) to a reasonable degree of accuracy, about 5%, a 2000 step program would have to be run through 50 times a second. This means that single instruction will have to be completed in 10×10^{-6} seconds. In terms of gates this means a 10×10^{-6} second enabled period and a possible 20×10^{-3} second disabled period.

In addition to errors introduced in computation due to the discrete operation of the computer, there is an error introduced because of the inaccuracies of the computing elements and gates. In order to maintain solution error to a reasonably small value

the computing elements and gates must maintain a corresponding accuracy. Again even in our simple problem the exact effect of component inaccuracies is difficult to analyze. For the purposes of flight simulation it is estimated that .1% components are needed.[4] In order to use these gates with existing arithmetic components a voltage range of ± 20 volts will be required. This outlines the basic specifications on the gates to be designed. All design work will be carried out with these specifications and the pulsed analog computer in mind.

1.4 SAMPLE GATE DESIGN

Any design procedure for sample gates must take into account the important quantities; gain, effect of trigger voltage on output, range of operation, enabled linearity and speed. A simplified schematic for the sample gate (Fig. 1-5) will allow us to get a first estimate of gate gain. The enabled gain will be

$$\left.\frac{E_o}{E_{io}}\right|_E = \frac{R_{LE}}{R_s + R_{LE} + Z_{gE}} \qquad 1.1$$

The disabled gain will be

$$\left.\frac{E_o}{E_i}\right|_D = \frac{R_{LD}}{R_s + R_{LD} + Z_{gD}} \qquad 1.2$$

where R_s is the input source resistance, Z_g is the impedance of the gates series element, and R_L is the impedance of the gates shunt element. R_L may include the gates load resistance. The subcsripts E and D refer to the enabled and disabled value of the quantity respectively. In a shunt gate $Z_{gE} = Z_{gD}$. In a series gate $R_{LE} = R_{LD}$.

Three types of trigger sources can be distinguished. These are the grounded trigger, the balanced trigger and the floating trigger. The effect of the trigger voltage can often be estimated

by assuming the triggered elements to be a single node when enabled.

A sample gate is usable over a limited range of input voltages. By using a piecewise linear model for the gating elements the breakpoints in the gates characteristics can be determined. At this point it is often useful to plot E_o vs E_i. This plot will include the gate gain, effect of trigger voltage and break points.

Linearity of the enabled gate becomes a problem largely because Z_{gE} may be a function of gate current. In order to predict these non-linearities a more elaborate model than the piecewise linear model for the gating element is required. Even non-linearities in the trigger source can appear as non-linearities in the gate output. It would now be appropriate to make a plot of $E_{oE} - KE_i$. K is a reference gain chosen commonly to be the gate gain near the point where $E_i = 0$.

The switching speed of a gate is largely determined by the switching speeds of the particular components used in the gate. The design work here can only attempt to make best use of the gating components. As a final step in this design procedure we must assure ourselves that the gates operation is consistant with the input source, output load, and trigger source characteristics.

The steps outlined have been called a design procedure while they are in reality an analysis procedure. However when applied to a given gating configuration many opportunities will be found for design. Several compromises will become apparent for example, switching speed can often be traded for gate linearity.

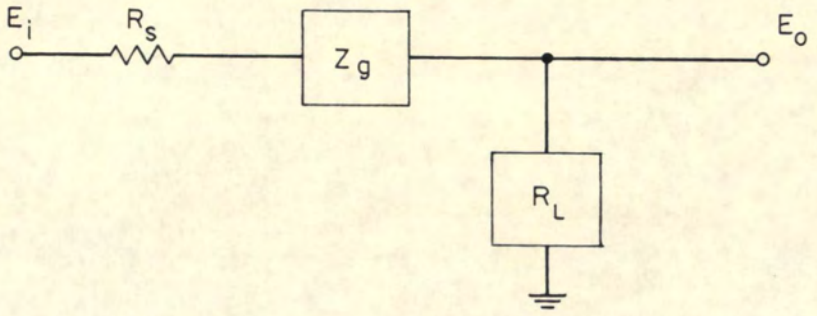


Fig. 1-5 A Simplified Sample Gate

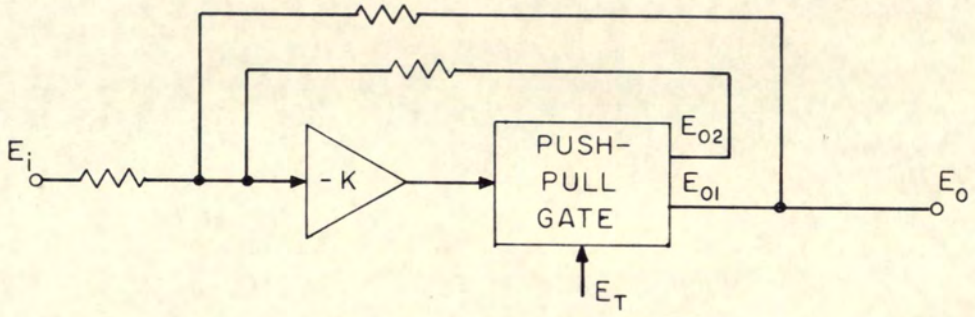


Fig. 1-6 Push Pull Sample Gate and Feedback

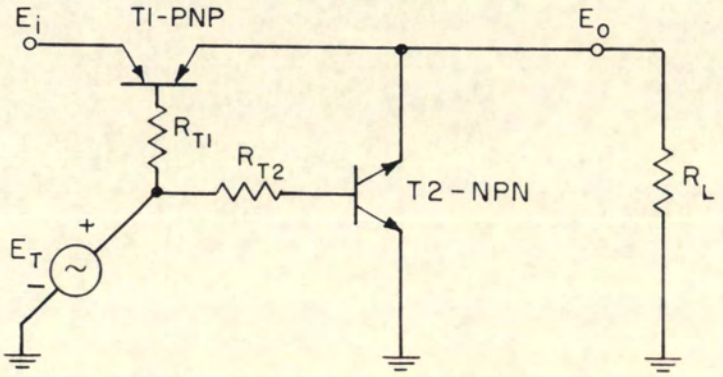


Fig. 1-7 A Series-Shunt Transistor Sample Gate

Improvements in sample gate linearity can be obtained by including the sample gate in a closed loop. Fig. 1-6 shows how this might be accomplished. The push-pull sample gate has two outputs one of which is exactly the same as an ordinary sample gate. The other output will have an output of zero during the enabled periods and a output equal to the input during disabled periods. By feeding back both outputs the operational amplifier is assured of continued closed loop operation, which makes this scheme usable with any operational amplifier.

1.5 A TRANSISTOR SAMPLE GATE

Among the several sample gates analyzed, the bilateral transistor series-shunt gate (Fig. 1-7) best meets the requirements for pulsed analog uses. The design procedure previously outlined can be applied to this gate. This gate is enabled with a negative trigger voltage $-E_{TE}$ which saturates T1 and cuts of T2. The gate is disabled with a positive trigger voltage E_{TD} which cuts off T1 and saturates T2. This gate is to be used between two analog feedback amplifiers and therefore has an input source resistance of almost zero and an external output load resistance, R_L, of 100KΩ. The enabled gain of the gate will be $\frac{R_L}{R_L + R_{SAT}}$ and the disabled gain of the gate will be zero, where r_{SAT} is the saturation resistance of the transistor, and it is assumed the cut off transistor resistance is much greater than R_L. Note also that any leakage current from the cutoff transistor will always flow through a very small resistance. By replacing the enabled element with a single node and completely neglecting the disabled element, the first order effect of trigger voltage on the output

is seen to be zero. The transistor models of Fig. 1-8 are usable in calculating the linear range of this gate. Using the model, with D1 and D2 taken to be ideal diodes, the break points in the E_o vs E_i plots can be determined. In Fig. 1-9 the gain, effect of trigger voltage, and breakpoints of this gate have been plotted.

A very realistic non-linear model for the transistor is obtained by replacing the diodes of Fig. 1-8 with the diode function

$$e_d = K_1 \ln\left\{1 + \frac{i_d}{I_{co}}\right\} \qquad 1.3$$

From this model the saturation resistance, which is defined to be $\frac{\partial V_c}{\partial I_c}\Big/ I_c = o$ in the grounded emitter characteristics, can be shown to vary as $1/I_\beta$.

$$r_{SAT} = \frac{2K_1(1-\alpha)}{I_\beta}$$

Non-linearities due to the fact that r_{SAT} varies with base current are the important non-linearities in a transistor sample gate. Errors due to unbalance in the transistors operation are generally small (less than 1×10^{-3} volts). Errors due to the curvature of the grounded emitter characteristics of the transistor are easily eliminated by design. For the gate of Fig. 1-7 the non-linearities due to r_{SAT} varying with trigger current can be expressed by Equ. 1-5.

$$E_o - KE_i = \frac{2(1-\alpha)\, K_1\, R_{T1}\, (E_i)^2}{R_L\, E_{TE}\, (E_i + E_{TE})} \qquad 1.5$$

where K is the gain of the gate at E = 0. The complete derivation of this expression is included in Chapter IV.

Since the base current of T1 varies with E_1, the switching speed of this gate will vary with input voltage. As the linearity of the gate is improved longer switching speeds will result.

A General Transistor 2N593 or 2N594 may have a value of $2(1-\alpha)\ K_1$ of about 2.5×10^{-3} volts. With R_{T1} selected to be 250KΩ, R_L given to be 100KΩ, and E_{TE} selected to be + 25 volts, the maximum gate non-linearity will be .1% or 20×10^{-3} volts. It should be noted that the cutoff transistor will be back biased by as much as 45 volts. Transistors must be selected to be certain that they are capable of withstanding this large voltage. Fig. 1-10 is a plot of gate linearity.

1.6 STORAGE GATE DESIGN

The basic considerations which must be taken into account in the design of a storage gate are: set time, hold time, range of operation and switching transients. A simplified schematic for a storage gate is shown in Fig. 1-11. The actual storage is accomplished by holding charge on a capacitor C. The set time is defined to be the maximum time required for the output of the enabled gate to change from one value to another. Since the final value may never by reached an allowable error must be specified. The disabled gate will maintain the correct voltage within an allowable discharge error for a finite time τ_d. The minimum value of τ_d is called theh old time.

A floating trigger source is often used with the storage gate. This will allow us to include the gating elements and the trigger source in a two terminal series element. The characteristics of this element can be shown by a plot of e_g vs i_g.

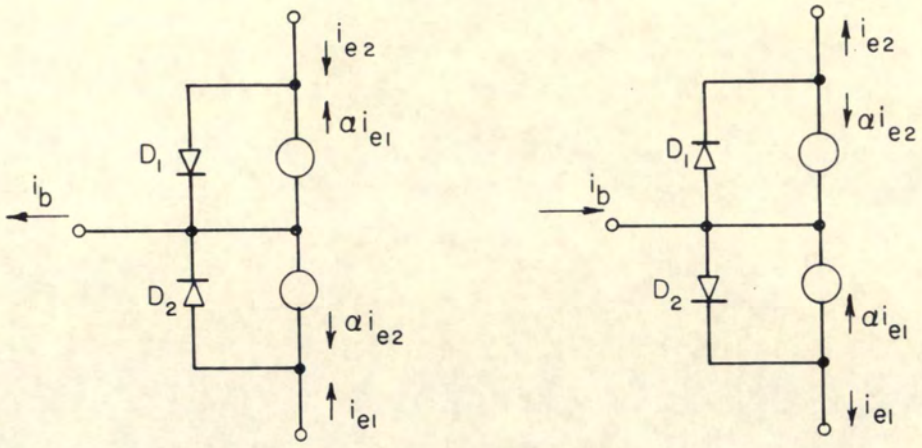


Fig. 1-8 Models for Transistors

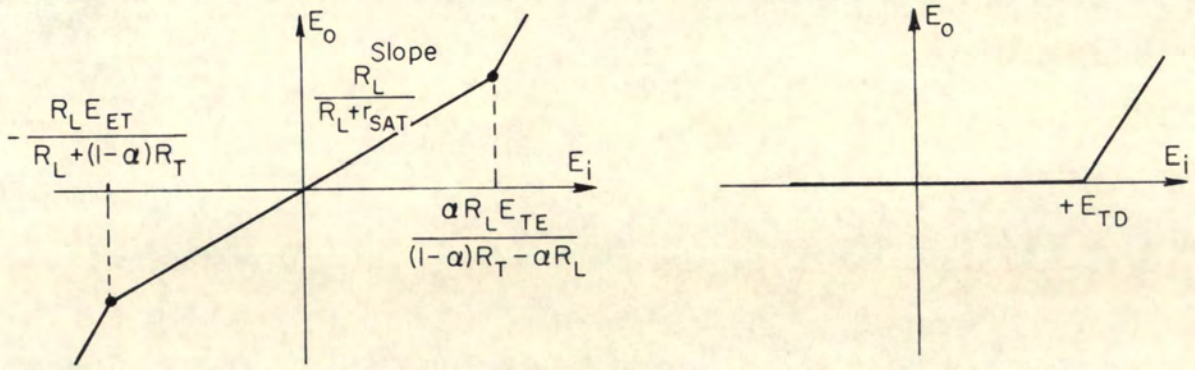


Fig. 1-9 Transistor Gate Characteristics

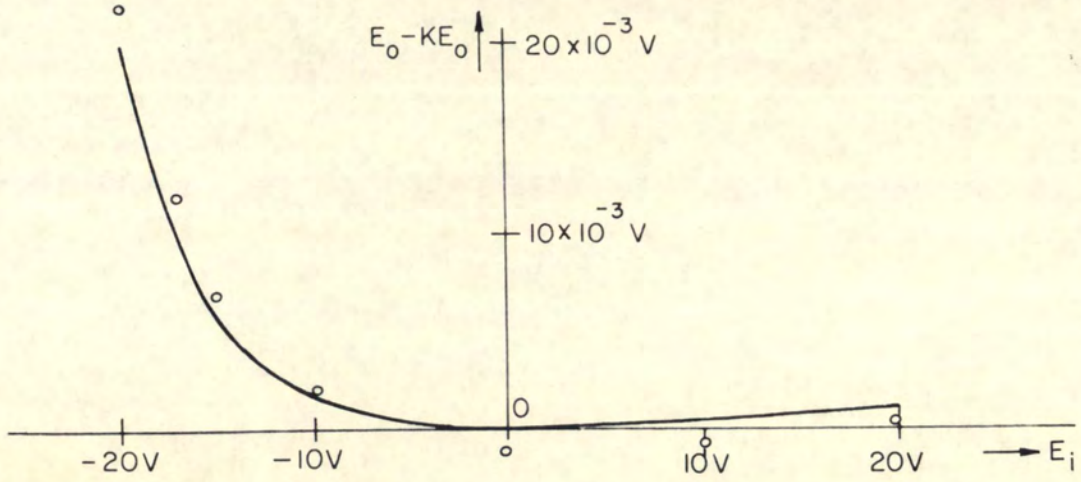


Fig. 1-10 Transistor Gate Linearity

Non-linearities in the enabled e_g vs i_g plot will affect set time but will not affect gate linearity. A gate of this type will have a linear gain of unity. The disabled e_g vs i_g plot will show a maximum difference which can occur between input and output voltage before the leakage current becomes excessive. The gate which we will attempt to build will have a maximum difference of 40 volts.

The exact nature of the off-switching transients in a storage gate are important because these transients may introduce permanent errors in the output voltage. The operation of a storage gate is much more limited by the characteristics of the input and output circuits than is the sample gate. Current limitations in the input source become of immediate importance when calculating set time. Similarly leakage currents into the output circuitry will lessen hold time. And of course no gate is complete without a properly designed trigger source.

1.7 THE FOUR DIODE STORAGE GATE

The four diode bridge gate (Fig. 1-12)has often been used for a storage gate[6] and, despite the attempt to use several other novel gating arrangements, it remains the best storage gate available. This gate is enabled with a positive trigger voltage and disabled with a negative trigger voltage. Assuming that the diodes are identical and have a forward resistance r_f and a reverse resistance r_b, the eg vs ig plots can be easily obtained and are shown in Fig. 1-13. However before any conclusions can be reached about the four diode gate a more realistic model must be chosen for the diodes. If the diode curve

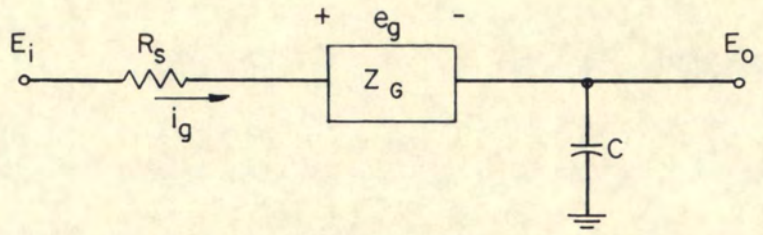


Fig. 1-11 A Simplified Storage Gate

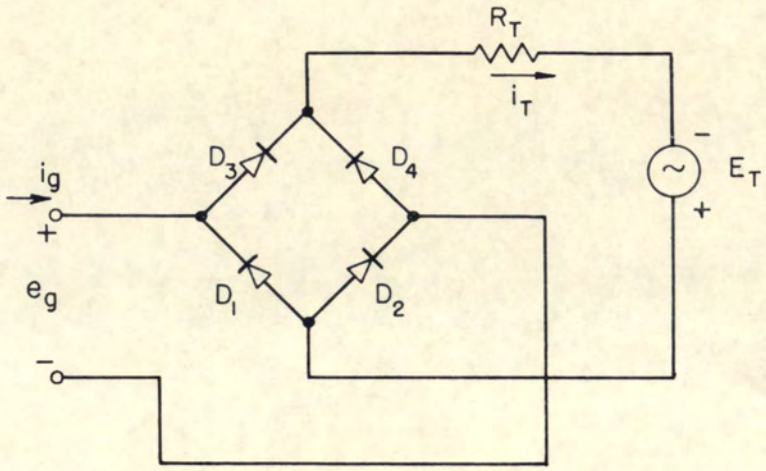


Fig. 1-12 Four Diode

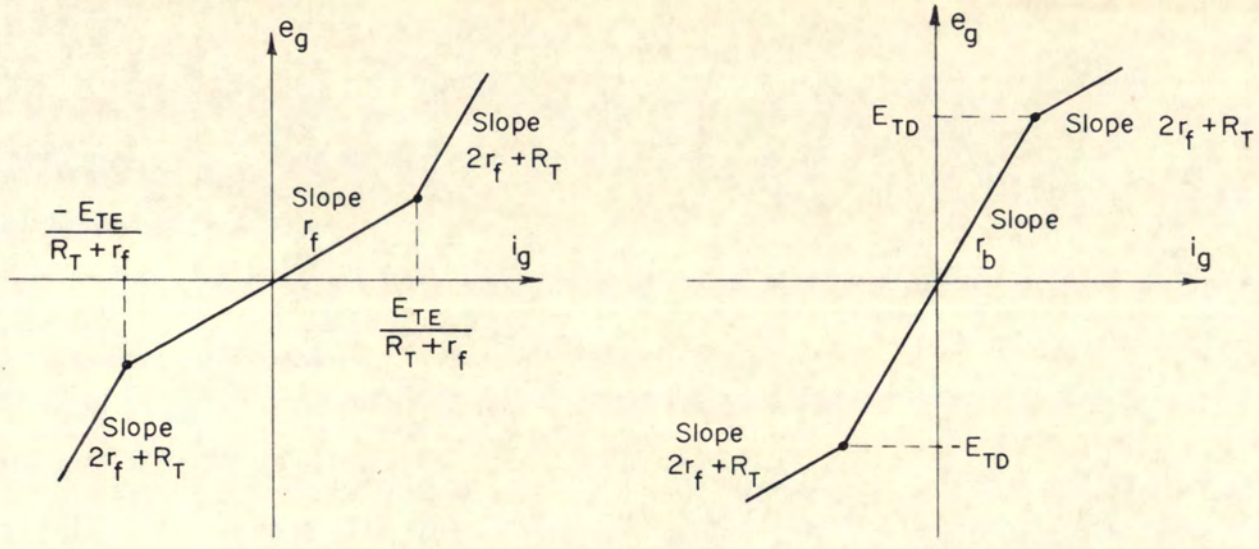


Fig. 1-13 Four Diode Bridge Characteristics

$e_d = f(i_d)$ is given and the diodes are identical the following set of equations can be derived.

$$E_T - i_T R_T = f\left[\left(\frac{i_T - i_g}{2}\right)\right] + f\left[\left(\frac{i_T + i_g}{2}\right)\right] \qquad 1.6$$

$$e_g = f\left[\left(\frac{i_T + i_g}{2}\right)\right] - f\left[\left(\frac{i_T - i_g}{2}\right)\right] \qquad 1.7$$

From these equations the plot of e_g vs i_g can be obtained either graphically or even perhaps analytically. Many interesting results can be obtained from this analysis. For example if the trigger source is a current source of value i_T the maximum possible value of i_g will be i_T.

Silicon diode characteristics are often approximated as

$$e_d = K_1 \ln \left\{ 1 + \frac{i_d}{I_{co}} \right\} \qquad 1.8$$

For a current source trigger the resistance of the gate r_g (which is defined to be $\left.\frac{\partial e_g}{\partial i_g}\right|_{i_g = 0}$) can be shown to be

$$r_g = \frac{2K_1}{i_T} \qquad 1.9$$

Therefore the current capabilites of the gate increase with trigger current not only because its linear range is extended but also because its conducting resistance is decreased. A typical value of 2K1 is .13 volts.

The expotential diode model shows that the true character of a back biased diode is closer to a current source then to a resistor. Fig. 1-14 shows the back biased diodes of the disabled gate replaced with current sources. This circuit would be ambiguous since four independent current sources are arranged such that

$I_2-I_4 = I_3-I_1$. Therefore the four dotted resistors have been added. However we can use the current source model to demonstrate the point that leaky diodes can be used to build a gate which has a leakage current much lower than any diode in the gate. This is due to the fact that these currents subtract before they leave the gate. If four equal diodes are used a gate can be built in which the very steep slope of the diode characteristic plays the important role in the disabled gates characteristics. The Transistron SG-222 diode, for example, has a leakage current of about $.25 \times 10^{-6}$ amps. By carefully selecting and matching these diode the gate leakage current can be reduced to $.01 \times 10^{-6}$ amps.

Now that we know that abilities of the series element, the value of the capacitor and the input source can be designed. Assume that the diodes for the gate have been carefully selected and a leakage current of $.01 \times 10^{-6}$ amps obtained. In order to secure a hold time of 20×10^{-3} seconds within an allowable error of 20×10^{-3} volts a $.01 \times 10^{-6}$ farad capacitor is required. Now turning to the enabled period a 40 volt change across this capacitor in 10×10^{-6} seconds will require an average charging current of 40 ma. Or if the capacitor is to charge exponentially to within 20×10^{-3} volts of final value a 130Ω resistance and peak current of .3 amps are demanded. A vacuum tube circuit which is capable or 150 ma output currents and which has a linear output resistance of $\frac{r_p}{2}$ has been developed for use with this gate[7] (Fig. 1-15). This circuit will replace the usual cathode follower output stage of the operational amplifier which drives the gate.

Special care must be taken to assure that the enabled gate

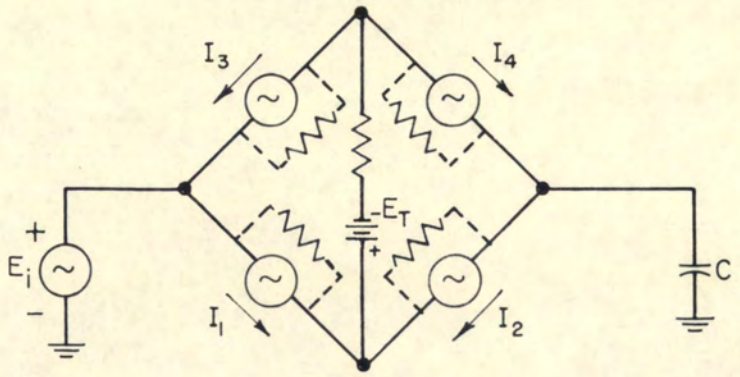


Fig. 1-14 Back Biased Diodes are Current Sources

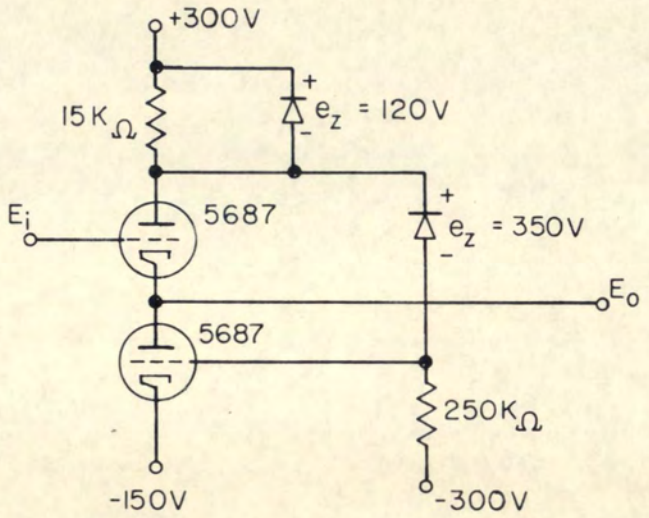


Fig. 1-15 The White Cathode Follower

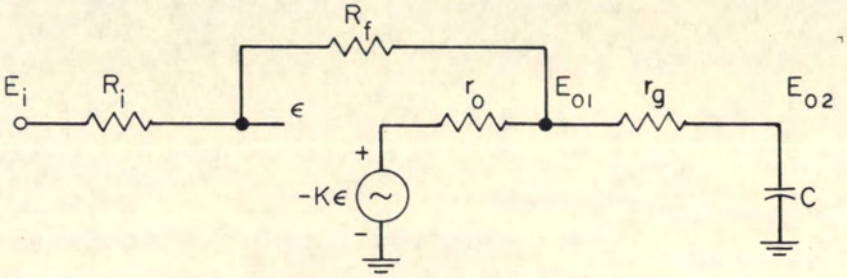


Fig. 1-16 Feedback Amplifier with Enabled Storage Gate

does not place a load on the operational amplifier which would cause it to oscillate. Fig. 1-16 illustrates the situation and Fig. 1-17 is a block diagram for this closed loop system. It is assumed that the unloaded feedback amplifier is designed to be very stable. The addition of the lag term $\frac{r_g CS + 1}{(r_o + r_g)CS + 1}$ could introduce enough additional phase shift to cause instability. However if r_g is greater than r_o this term can be made to have little effect. r_o which is equal to $\frac{r_p}{\mu^2}$ will typically be about 5Ω. By adjusting r_g the system can be stabilized while still maintaing a set time of 10×10^{-6} seconds.

1.8 MEASUREMENTS

Measurement of a gate capabilities should be made under conditions similar to those it will experience in actual use. The important measurements to be made on a sample gate are enabled linearity, disabled gain and switching speed. A circuit used for making direct measurement of sample gate linearity is illustrated in Fig. 1-18. Adjustments are provided to eliminate any bias which the gate may have and to normalize the gain before measurements are taken. The measuring instrument can be a high gain DC oscilloscope for making pulsed measurements. The input and output of the feedback gate are already of opposite sign and therefore a simple resistive summing network will make the gate error immediately available. The disabled gain can be determined by simply measuring the gate output when typical inputs are applied to the gate.

In a storage gate we must measure set time and hold time. Set time can be measured by using the circuit of Fig. 1-19.

The input voltage is made equal to say + 20 and a large resistor is connected from the capacitor to -20 volts. The time between pulses is adjusted to allow the capacitor to reach its final value. The set time is completed when the gate error is within its allowed limits. The hold time of a storage gate must be measured with a pulsed input. For example if the input of the storage gate is +20 volts during the enabled perios it should be switched to -20 volts immediately following the enabled period to simulate the input which a storage gate may actually experience. If this is not done any resistive component in Z_{gD} will not make its presence felt. At the end of the hold time the input will return to +20 volts and the capacitor will recharge to its proper value again. To measure the discharge error we need only measure this recharge, which can be done with a sensitive AC oscilloscope.

A closed loop system has been designed which consists of two sample gates and two storage gates and allows these components to operate under conditions similar to those experienced in actual pulsed analog use. This system, which is illustrated in Fig. 1-19, can also be used to make measurements of disabled gate discharge. The system operates by starting with the switch in position number 1 and applying a pulse E_{T1}. This will trigger sample gate number 1 and storage gate number 1 and in so doing will transfer the input voltage to the output. The next step is to trigger E_{T2} which transfer this voltage to the output of storage gate number 2. By this time the switch has moved into position number 2 and the program will continue to circulate the input

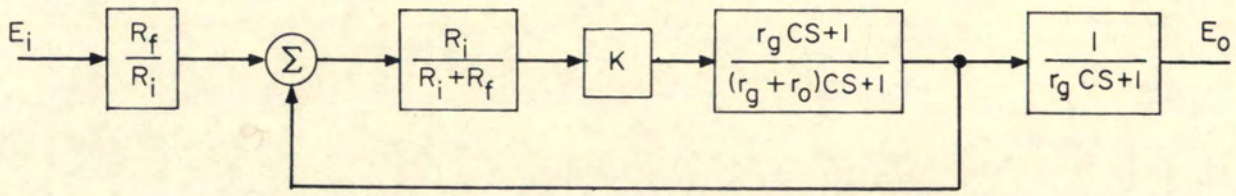


Fig. 1-17 Block Diagram Used to Determine Storage Gate Stability

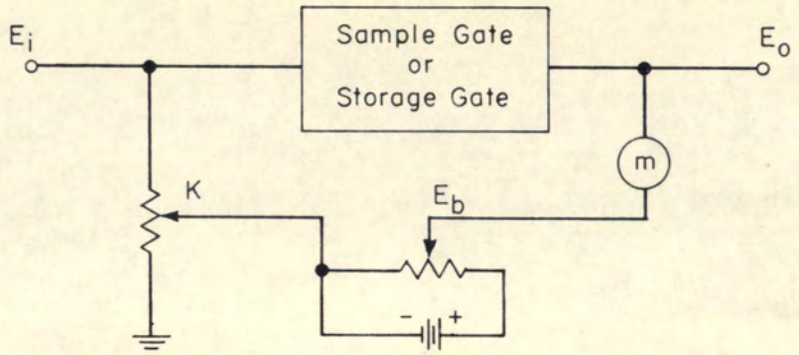


Fig. 1-18 Circuit Used to Measure Sample Gate Linearity

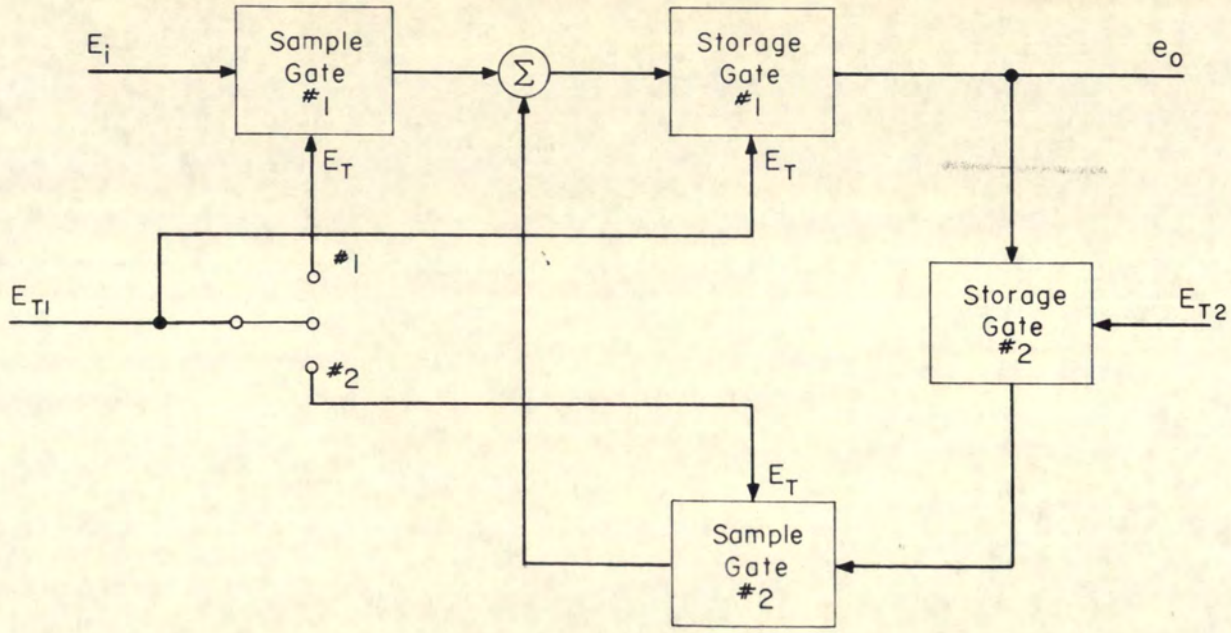


Fig. 1-19 Circuit Used to Test Gate Under Actual Operating Conditions

voltage by applying a pulse E_{T1}. The trigger pulses continue to repeat at regular intervals. After many cycyles are completed the switch is returned to position number 1 and the process started over again. The switching and counting is accomplished by a simple digital circuit.

If the loop gain is positive a difference equation can be written for the (n + 1) th output.

$$e(n+1) = K\,e(n) + E_b \qquad 1.10$$

where K is the loop gain and E_b is a bias voltage accumulated in making one excursion around the loop. The solution to this equation is

$$e(n) = e(o) - \frac{E_b}{1-K}\,(K)^n + \frac{E_b}{1-K} \qquad 1.11$$

or in the special case when K = 1.

$$e(n) = e(o) + E_b\,n$$

By looking at the output on the scope we can adjust the loop gain and bias until K = 1 and E_b = 0. Now by changing the time between trigger pulses E_{T1} and E_T2 an additional bias term will appear due to the fact that an additional discharge time has been allowed for storage gate number 1. This error is multiplied by the number of cycles n. By this method the small values of discharge error can be readily measured. This method is, however, limited by non-linearities in loop gain and by amplifier drift.

1.9 CONCLUSIONS AND RECOMMENDATIONS

The simple and important conclusion that can be drawn from this thesis is that analog gates to meet the pulsed analog requirements can be built. In the sample gate which was built

transistors had to be selected for high voltage breakdown. In the storage gate diodes had to be selected for low leakage current. While these selection procedures do not lend themselves to mass production techniques, the fact that the required analog gates can be built has nevertheless been demonstrated.

There remains many opportunities for the further improvement of analog gates. Several immediate approaches can be suggested for both the sample and storage gate. Better symmetrical transistors may be presently available on the market for use in the sample gate. Often the fact that a transistor is symmetrical is not even mentioned in the transistor specifications. A careful study may uncover several usable transistors. There is also the possibilty that non-symmetrical transistors can be used in this gate. The same model configuration which was used for the bilateral transistor can also be used for the non-symmetrical transistor. The model will however have a numerical unbalance. From this model the important gate properties could be established in terms of the transistors parameters. This will give some criterion for chosing a transistor to be used in the gate. By this approach a transistor with a high voltage break down and faster switching speed may be selected. In a sample gate, trigger source complexity and gate performance can be traded. By using a separate trigger source for each element of the series shunt transistor gate a better gate can be built. In this manner the trigger requirements of each element can be better satisfied. All of these approaches could serve to further improve the sample gate.

It is needless to say that the search fo better diodes to

be used in the storage gate should continue. Another fundamental problem connected with the storage gate concerns itself with the properties of the capacitors dielectric. An effect called dielectric absorption can cause gate errors. A theoretical or experimental assurance that this effect can be made negligibly small, by selecting the proper dielectric, would be welcomed. The transistor blocking oscillator which was designed for use with the storage gate has the limitation that it can only be pulsed at a 20KC rate. The use of better pulse transformers, which are now available on the market, could possible extend this to 50KC. Or perhaps a monostable multivibrator with high current capabilities could be built. Finally the output stage of the storage gate requires some special attention. Since this stage operates completely open loop, it is subject to drift and non-linearites. These disadvantages could possibly be eliminated by a more careful design.

CHAPTER II

THE SAMPLE GATE

2.1 BASIC DESIGN

The basic considerations which must be taken into account in the design of a sample gate are the enabled gain, the disabled gain, operating range, linearity and speed. A simplified schematic for a sample gate is shown in Fig. 1-5. R_s is the internal resistance of the source. Z_g will take on two values; Z_{gE}, the impedance of the disabled series element and Z_{gD}, the impedance of the disabled series element. R_L is the shunt element of the gate and may also include gate load resistance. The value of R_L can also be changed by the trigger pulse and can take on two values; R_{LE}, the shunt resistance for the enabled gate and R_{LD}, the shunt resistance for the disabled gate. The trigger voltage which is omitted from this diagram simply determines the state of Z_g and R_L. The subscript E will always refer to the enabled quantity while the subscript D refers to the disabled quantity. Expressions for the gate transimissions can now be written. When the gate is enabled the transmission will be

$$\left.\frac{E_o}{E_i}\right|_E = \frac{R_{LE}}{R_{LE} + Z_{ge} + R_s} \qquad 2.1$$

If this transmission is to be near one, $R_s + Z_{gE}$ must be very much less than R_{LE}. The disabled gain, which for an ideal gate is zero, is for this more realistic model

$$\left.\frac{E_o}{E_i}\right|_D = \frac{R_{LD}}{R_{LD} + Z_{gD} + R_s} \qquad 2.2$$

From this we arrive at the criterion the $Z_{gD} + R_s \gg R_{LD}$. It is

not necessary that both Z_g and R_L be triggered. In a series gate only Z_g is triggered. In a shunt gate only R_L is triggered. In a series-shunt gate both are triggered.

There are essentially three methods of wiring the trigger source to the gating elements (Fig. 2-1). In the grounded trigger arrangement the trigger voltage causes a current i_T to flow. The return path to ground for this current is through the terminals of the gating element to the connected circuits and to ground. The incremental equation $i_T = i_{T1} + i_{T2}$ applies. These currents can cause an error at the output of the gate. The first effect of trigger voltage on enabled gate output can often be calculated by assuming that the gating element becomes a single node during the enabled period. If the by Eq. 2-3.

$$\left.\frac{E_o}{E_{TE}}\right|_E = \frac{R_s R_L}{R_T R_s + R_T R_L + R_s R_L} \qquad 2.3$$

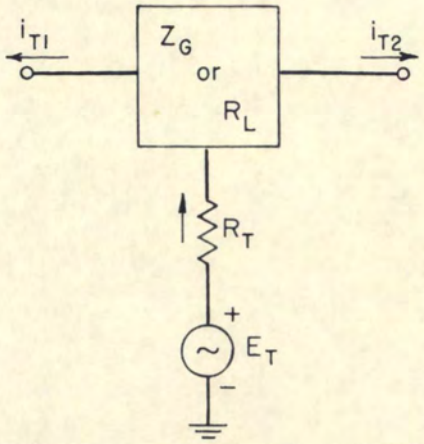
We can also see that the trigger resistance R_T will affect the gate gain. The balanced trigger offers the possibility of circulating the trigger current without introducing an error due to currents from the terminals of the gating element. The value of R_T does however enter the expression for gate enabled gain. Similar to the balanced trigger source is the floating trigger source of Fig. 2-1c. In the floating trigger case the value of R_T does not necessarily enter into the expressions for gate gain. In any case, the trigger voltage will introduce an additional term in the expression for enabled and disabled output. For an ideal gate this term will be zero.

A sample gate will be usable only over a limited range of

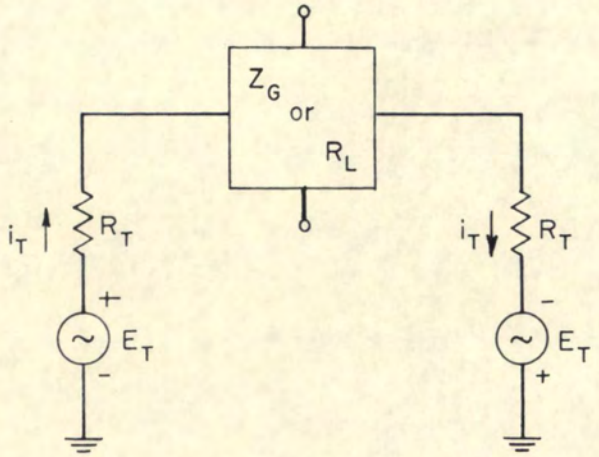
input voltages. A complete model for the gate will permit us to approximate the extent of this useful range. If piecewise linear models are used for the gates components, then piecewise linear gate transmission characteristics can be calculated. The graph of E_o vs E_i for both the enabled and disabled gate will be of particular interest. These plots should also include the gate gain and effect of trigger voltage as calculated so far. From these plots we will be able to determine many of the gates abilities and disabilities.

Linearity of the enabled gate becomes a problem largely because Z_{ge} may be a function of gate current. Also in many cases the major non-linearities are introduced by the driving source resistance R_s. However, these will affect the linearity only when $Z_{ge} + R_s$ becomes large enough to affect the expressions for enabled gain. In gates in which the trigger current changes with input voltages non-linearities in the trigger source can be reflected into gate output. The speed of the gate or the time it takes the output voltage to change from zero to its new value when enabled, is mainly a property of the switching speed of the particular components used in the gate. Of course the switching speed of the trigger voltage source is also of considerable importance in determining gate switching speed.

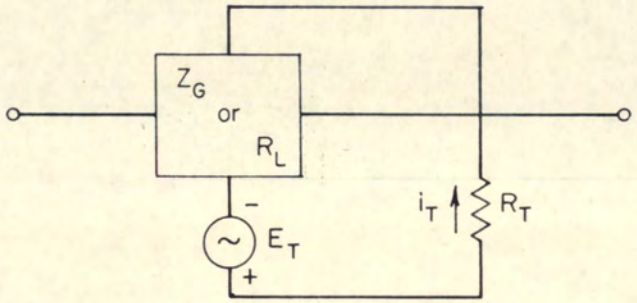
The question of a model for the gates elements is an important one. The more realistic the model, the more realistic will be the calculations for gain, linear range, etc. The general method of analysis for any gate will be to first look at the gross effects using a gross model, and then as the picture becomes clearer



(a) The Grounded Trigger



(b) The Balanced Trigger



(c) The Floating Trigger

Fig. 2-1 Three Basic Triggering Methods

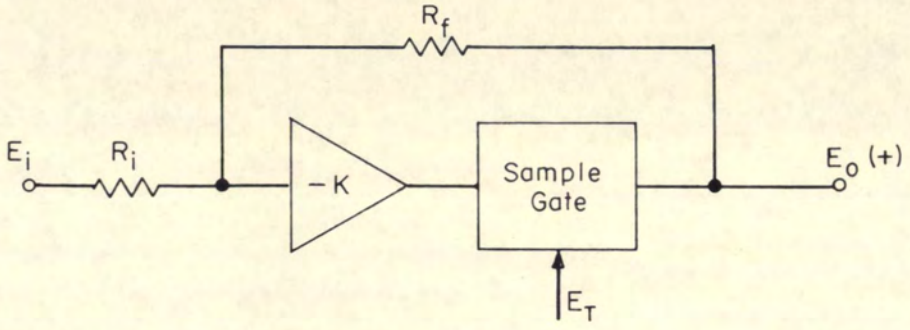


Fig. 2-2 Feedback Can Improve the Linearity of the Sample Gate

to add in the more subtle and more refined aspects of the gates operation. Actually, different models may be used for different calculations. For example, if a gate uses diodes we may first assume these diodes to be ideal. If this model shows that the gate has the, proper enabled and disabled gain and linear range, a more elaborate model for the diodes, perhaps a piecewise linear diode with a forward conducting resistance r_f and a back resistance r_b, will allow us to get a better estimate of enabled and disabled gain. Finally, if an estimate of gate linearity is desired, a non linear diode curve will have to be used. In this thesis no attempt is made to associate a model chosen for a device with the physics of the device.

As in the design of any equipment the input and output conditions are important. The input current requirements of a sample gate must be consistant with the driving sources capabilities. Similarly the load which the gate faces should be of proper magnitude. Finally, no sample gate is complete without a carefully designed trigger source. This completes the fundamentals of sample gate design. Below is a list which summaries the important steps which are taken in analyzing a gate.

1) Get rough picture of gates operation by inspection
2) Choose model for gating elements for each calculation
3) Calculate enabled gain; Calculate disabled gain
4) Determine range of operation, enabled and disabled
5) consider effect of trigger voltage on output, both states
6) calculate or measure linearity
7) Estimate gate speed

8) Consider or design in more detail input source, output load, and trigger source.

2.2 SAMPLE GATES AND FEEDBACK

The linearity of a sample gate can be improved by the use of feedback. By inserting a sample gate after the final output stage and before the feedback point of an operational amplifier all the benefits of the high gain amplifier and negative feedback can be obtained. Fig. 2-2 illustrates in this method. This feedback arrangement adapts very easily to pulsed analog uses. The operational amplifier can for example be the same amplifier which is used for a summer. The output stage of a multiplier is very likely to be an operational amplifier used as a summer, which can therefore incorporate this gating arrangement.

One disadvantage of this closed loop arrangement is the fact that the amplifier is open loop when the gate is disabled. An operational amplifier which is operated open loop will saturate, resulting in large output voltages and long recovery time. This difficulty can be overcome by the use of a push-pull gate. The push-pull gate is a sample gate with two outputs. One output is exactly like the ordinary sample gate. The other output is zero during the enabled period and is equal to the input during the disabled period. By feeding back both outputs the amplifier is always in a closed loop state. Ideally the switching time of the gate should be fast when compared to the response time of the amplifier. This is to prevent any large transients from being introduced during the switching.

2.3 MEASUREMENTS

Three important quantities must be measured in the sample gate. These are; enabled linearity, switching speed, and disabled gain. Because we are interested in errors of about .1% or 20×10^{-3} volts any method of measurement must avoid a comparison of large quantities. For example we could not measure the input voltage of a gate, measure the output voltage of the gate, and then subtract these two voltages to obtain an accurate estimate of gate error. Fig. 1-18 is a schematic of a circuit used to directly measure gate non-linearity. Adjustments are provided whereby the gate gain and any gate bias can be removed before making these measurements. In this measurement the voltage drop across the source resistance R_s has neccessarily been neglected. Unless E_1 is readily attainable some independent measurement would have to be made to determine input source linearity. The measuring instrument can be either a millivolt meter for D C measurements or, to be more realistic, an oscilloscope for pulsed measurements. Switching time can be easily observed when making pulsed measurements. The disabled gain can be obtained by simply measuring the output of the disabled gate with a high gain oscilloscope while some typical inputs are applied to the gate.

The input and output of a sample gate with feedback are of opposite sign. The error in this arrangement can be measured after constructing a resistive summing network. Since much care was taken to design the gate with a particular load in mind, the measuring resistors should simulate this load. If R_1 and R_2 are adjusted to be equal and the gain from E_1 to E_o carefully adjusted

the error measuring meter will indicate $\frac{E_o - E_i}{2}$. Again DC or pulsed measurements can be made.

CHAPTER III

DIODE SAMPLE GATES

3.1 A DIODE SERIES GATE

The series diode gate with a grounded trigger of Fig. 3-1 will serve as a first example of a sample gate. This gate, which is enabled with a positive trigger voltage and disabled with a negative trigger voltage, can be roughly analyzed by considering the diodes to be ideal. In the enabled state the complete expression for gate output voltage (that is,iincluding the effect of trigger voltage) can be easily written.

$$E_o = \frac{R_s R_L \quad E_{TE}}{R_s R_T + R_L R_T + R_s R_L} + \frac{R_T R_L \quad E_i}{R_s R_L + R_s R_T + R_T R_L} \qquad 3.1$$

Still using the ideal diode model the disabled gain is truly zero. The range of input voltage over which the diodes will remain conducting when the gate is enabled can be determined by writting expressions for the current in the diodes.

$$i_1 = \frac{R_s E_{TE} + R_T E_i}{R_s R_L + R_s R_T + R_L R_T} \qquad 3.2a$$

$$i_2 = \frac{-(R_s + R_L)E_i + R_L E_{TE}}{R_s R_L + R_s R_T + R_L R_T} \qquad 3.2b$$

As neither of these currents can be negative, the range of voltages for E_i is $-\frac{R_s}{R_T} E_{TE} \leq E_i \leq \frac{R_T E_{TE}}{R_L + R_T}$. When the gate is disabled there is no value of input voltage which will make the output other than zero. Therefore, the disabled gain is always zero. Fig. 3-2 summarizes the gates characteristics.

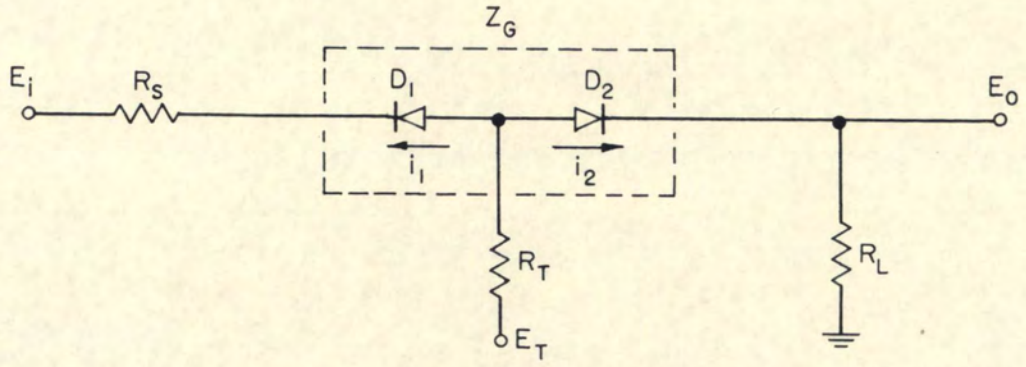


Fig. 3-1 Series Diode Gate with Grounded Trigger

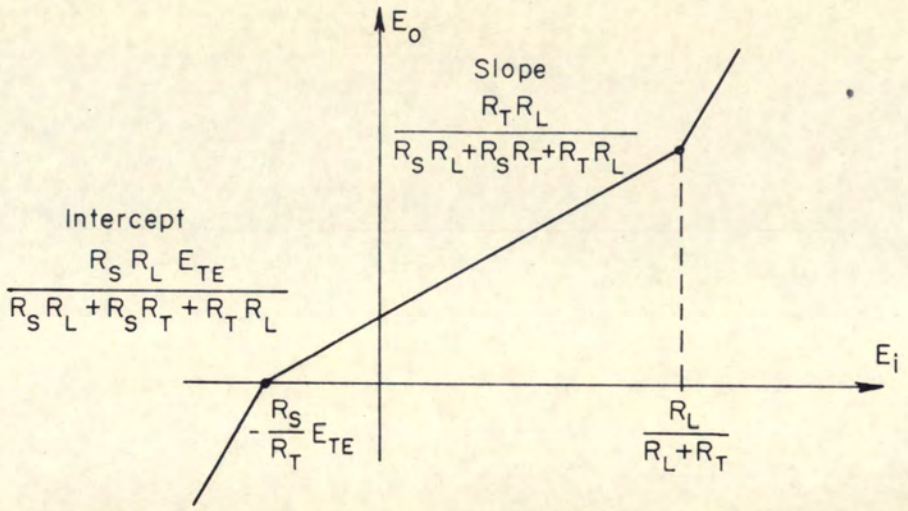


Fig. 3-2 Enabled and Disabled Transmissions of Series Diode Gate

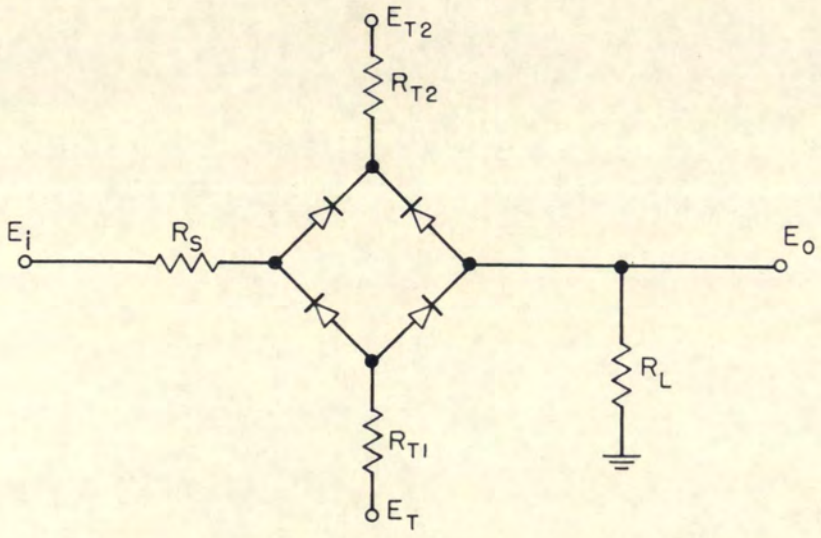


Fig. 3-3 The Four Diode Balanced Trigger Series Sample Gate

Applying typical numbers to the equations for enabled gain and linear range will give us a better feeling for the capabilities of this gate. R_s = 500r, R_L = 2 Kr, R_T = 20Kr and E_{TE} = 40V are all values which one might choose. This allows us to calculate that

$$E_o = .785 + .785\ E_i$$

and that

$$1 \leq E_i \leq 36.3.$$

Even at this point many difficulties which would be encountered when applying this gate to the pulsed analog computer are apparent. The gate lacks unity gain. However, upon returning to the schematic for the pulsed analog computer (Fig. 1-2) we see that this can be compensated for by a change in the input resistor of the following inverter. A real difficulty with this gate is its limited linear range. This gate is good only for positive input and positive output voltages. Of course, we could add 20 volts to the input and then subtract 20 volts from the output to obtain the proper range; but this becomes awkward. In other words we can stop here for it is hardly likely that this gate would be used in our application. It has served well however, as a first illustration of a sample gate and the types of difficulties which are encountered in its design.

3-2 THE DIODE SERIES GATE WITH BALANCED TRIGGER

By paralleling the gating element of the previous gate with a symmetric element, the balanced trigger four diode bridge gate is constructed. (Fig. 3-3) The newly added gating element is symmetric in that the diodes are reversed and the polarity of the

trigger voltage is reversed. This gate will be enabled when E_{T1} is positive and E_{T2} is negative. It is disabled when E_{T1} is negative and E_{T2} is positive. Again considering that during the enabled state the diodes are all short circuits we can calculate the enabled gain and the effect of the trigger voltages in one step. All currents in the gate can be calculated. Fig. 3-4 shows the circuit and Eq. 3-3a to Eq. 3-3f are the results. Of course, $i_c R_L$ is the output voltage.

$$\begin{bmatrix} E_{T1E} - E_i \\ E_{T1E} \\ E_{T2E} \\ 0 \end{bmatrix} = \begin{bmatrix} R_s & R_{T1} & 0 & 0 \\ 0 & R_{T1} & R_L & 0 \\ 0 & 0 & R_L & -R_{T2} \\ 1 & -1 & 1 & 1 \end{bmatrix} \begin{bmatrix} ia \\ ib \\ ic \\ id \end{bmatrix} \qquad 3.3a$$

$$D = R_s R_{T1} R_L + R_s R_{T1} R_{T2} + R_s R_L R_{T2} + R_{T1} R_{T2} R_L \qquad 3.3b$$

$$Dia = -(R_{T1} R_L + R_{T1} R_{T2} + R_L R_{T2}) E_i + R_L R_{T2} E_{T1E} + R_L R_{T1} E_{T2E} \qquad 3.3c$$

$$Dib = -R_L R_{T2} E_i + (R_L R_{T2} + R_L R_s + R_s R_{T2}) E_{T1E} - R_s R_L E_{T2E} \qquad 3.3d$$

$$Dic = R_{T1} R_{T2} E_i + R_{T2} R_s E_{T1E} + R_s R_{T1} E_{T2E} \qquad 3.3e$$

$$Did = R_{T1} R_L E_i + R_s R_L E_{T1E} - (R_s R_{T1} + R_s R_L + R_{T1} R_L) E_{T2E} \qquad 3.3f$$

To determine the operating range of this gate, current in each diode of the four diode bridge must be calculated. If the diodes are of very low resistance or of zero resistance, the currents i_a, i_b, i_c, and i_d will appear as current sources with values as determined by Eq. 3-5a to Eq. 3-5e. Fig. 3-5 illustrates

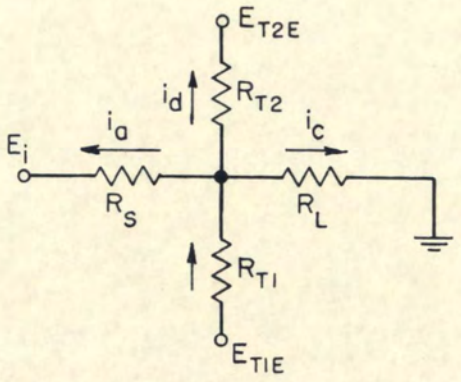


Fig. 3-4 In the Enabled Gate All Diodes Are Shorts

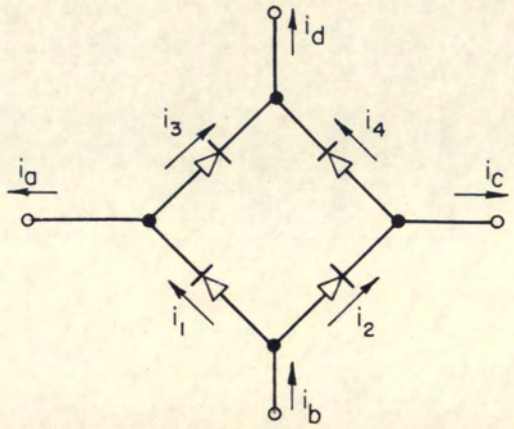
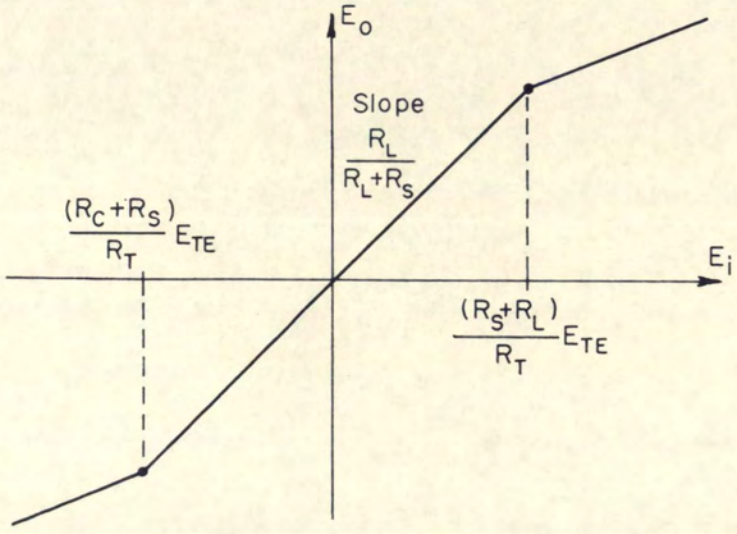


Fig. 3-5 The Four Diode Bridge



$$\left.\frac{E_o}{E_i}\right|_{\text{Disabled}} = 0$$

Fig. 3-6 Four Diode Gate with Balanced Trigger

this bridge. If the diodes are all short circuits and the four currents i_a, i_b, i_c and i_d are given, the diode currents i_1, i_2, i_3 and i_4 cannot be uniquely determined. However, if the diodes have a resistance Ra the following equation applies.

$$0 = i_1 R_a + i_3 R_a - i_4 R_a - i_2 R_a \qquad 3.6a$$

$$0 = i_1 + i_3 - i_4 - i_2 \qquad 3.6b$$

Eq. 3-6b willhhold for any R_a however small, provided $R_a = 0$. Three current summing equations and Eq. 3-6b provide enough information to calculate all diode currents. These expressions are summarized in Eq. 3-7

$$\begin{bmatrix} i_a \\ ib \\ ic \\ 0 \end{bmatrix} = \begin{bmatrix} 1 & 0 & -1 & 0 \\ 1 & 1 & 0 & 0 \\ 0 & 1 & 0 & -1 \\ 1 & -1 & 1 & -1 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} \qquad 3.7$$

The solution to these equations are given in Eq. 3-8.

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} = \frac{1}{4} \begin{bmatrix} 1 & 2 & -1 & 0 \\ -1 & 2 & 1 & 0 \\ -3 & 2 & -1 & 0 \\ -1 & 2 & -3 & 0 \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \\ 0 \end{bmatrix} \qquad 3.8$$

The next step is to calculate i_1, i_2, i_3 and i_4 in terms of E_i and E_{TE}. This is not very difficult and the results are shown below. It is apparent

$$i_1 = \frac{-(R_L R_T + 1/2\ R_T^2)}{D} E_i + 1/2\left(\frac{E_{TE}}{R_T}\right) \qquad 3.9a$$

$$i_2 = \frac{1/2\ R_T^2}{D} E_i + 1/2\ \frac{E_{TE}}{R_T} \qquad 3.9b$$

$$i_3 = \frac{R_L R_T + 1/2\ R_T^2}{D} E_i + 1/2\ \frac{E_{TE}}{R_T} \qquad 3.9c$$

$$i_4 = -\ 1/2\ \frac{R_T^2}{D} E_i + 1/2\ \frac{E_{TE}}{R_T} \qquad 3.9d$$

from Fig. 3-3 and from the above equations that the linear range is symmetric with respect to E_i. For large positive E_i the current in D_1 is the first to go negative. This will occur when

$$E_i = \frac{\pm 1/2\ R_L R_T + R_L R_s + 1/2\ R_T R_s}{R_T R_L + 1/2\ R_T^2} E_{TE} \qquad 3.10$$

As in the previous gate there is no value of E_i which make E_o other then zero when the gate is disabled.

In the interest of large enabled gain the trigger voltage and its associated resistor are often made to appear as a current source to the enabled gate. With the modification that R_T is very large or that E_{TE}/R_T appears as a current source, we can rewrite the equations for enabled gain, disabled gain, enabled linear range and current in the diodes.

The enabled and disabled gains become

$$\left.\frac{E_o}{E_i}\right|_E = \frac{R_L}{R_L + R_s} \qquad 3.11$$

$$\left.\frac{E_o}{E_i}\right|_D = o \qquad 3.12$$

$$i_1 = \frac{-(R_L R_T + 1/2\ R_T^2)}{D} E_i + 1/2\left(\frac{E_{TE}}{R_T}\right) \qquad 3.9a$$

$$i_2 = \frac{1/2\ R_T^2}{D} E_i + 1/2\ \frac{E_{TE}}{R_T} \qquad 3.9b$$

$$i_3 = \frac{R_L R_T + 1/2\ R_T^2}{D} E_i + 1/2\ \frac{E_{TE}}{R_T} \qquad 3.9c$$

$$i_4 = -\ 1/2\ \frac{R_T^2}{D} E_i + 1/2\ \frac{E_{TE}}{R_T} \qquad 3.9d$$

from Fig. 3-3 and from the above equations that the linear range is symmetric with respect to E_i. For large positive E_i the current in D_1 is the first to go negative. This will occur when

$$E_i = \frac{\pm 1/2\ R_L R_T + R_L R_s + 1/2\ R_T R_s}{R_T R_L + 1/2\ R_T^2} E_{TE} \qquad 3.10$$

As in the previous gate there is no value of E_i which make E_o other then zero when the gate is disabled.

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The enabled and disabled gains become

$$\left.\frac{E_o}{E_i}\right|_E = \frac{R_L}{R_L + R_s} \qquad 3.11$$

$$\left.\frac{E_o}{E_i}\right|_D = o \qquad 3.12$$

Similarly, the linear range is modified to take into account this approximation.

$$E_i = \pm (R_L + R_s)\left[\frac{E_{TE}}{R_T}\right] \qquad 3.13$$

In this case the diode bridge behaves very symmetrically. Eq. 3-14a to Eq. 3-14d show that the diodes on opposite legs of the bridge have identical currents in them. There is a superposition which applies to this bridge and its currents. The trigger source causes a current $I_T/2$ to flow in each diode.

$$i_1 = -1/2 \frac{E_i}{R_s + R_L} + 1/2 \left(\frac{E_{TE}}{R_T}\right) \qquad 3.14a$$

$$i_2 = 1/2 \frac{E_i}{R_s + R_L} + 1/2 \left(\frac{E_{TE}}{R_T}\right) \qquad 3.14b$$

$$i_3 = 1/2 \frac{E_i}{R_s + R_L} + 1/2 \left(\frac{E_{TE}}{R_T}\right) \qquad 3.14c$$

$$i_4 = -1/2 \frac{E_i}{R_s + R_L} + 1/2 \left(\frac{E_{TE}}{R_T}\right) \qquad 3.14d$$

The input voltage causes a current $\frac{E_i}{2(R_s + R_L)}$ to flow in each diode. These currents will add in two opposite diodes and subtract in the other two. Remember that this is only true when $R_T \gg R_s + R_L$.

Fig. 3-6 is a summary of the gates characteristics as discussed so far.

As a numerical example, let us assume that we are to design a diode gate of the balanced trigger type and that we are given the input source resistance as 500 ohms and the output load as 2000 ohms. The linear range of this gate is to be ± 20 volts. It remains for us to design a trigger source. Recognizing that we

cannot build a perfect current source, we can, however, use the equations derived for this case as a guide. Let us vary R_T and calculate E_{TE}, maximum trigger current, and $\frac{E_o}{E_i}\Big|_E$ with the constraint that the linear range remain a constant ± 20 volts. By turning back to the appropriate equation and putting in the known values the following three equations can be written.

$$E_{TE} = .02 \frac{2000 R_T + .5 R_T^2}{1000 + 1.25 R_T}$$

$$i_{dmax} = \frac{60 + .01 R_T}{1000 + 1.25 R_T}$$

$$\frac{E_o}{E_i}\Big|_E = \frac{2 R_T}{2000 + 2.5 R_T}$$

In Fig. 3-7 the above equations are plotted. From these graphs the right combination of R_T and E_{TE} can be chosen. i_{dmax} gives the maximum current required of this source and $\frac{E_o}{E_i}\Big|_E$ is the resulting gate gain.

3-3 THE DISABLED SERIES GATE

Before continuing with the floating trigger four diode gate, we might pause to investigate in general one of the main disadvantages of the series sample gate when applied to the pulsed analog computer. This difficulty originates in the fact that Z_{GD} contains a capacitive component. The resistive component of Z_{GD} is generally large enough to be of no consequence when compared to this capacitive component. Fig. 3-8 is an illustration of the circuit with which we are now concerned. Let us assume that the input voltage is a ramp $\frac{\Delta E}{\Delta t} t$ and that this ramp lasts for a long time compared to the time constant $\tau = (R_s + R_L)C$. The problem is to

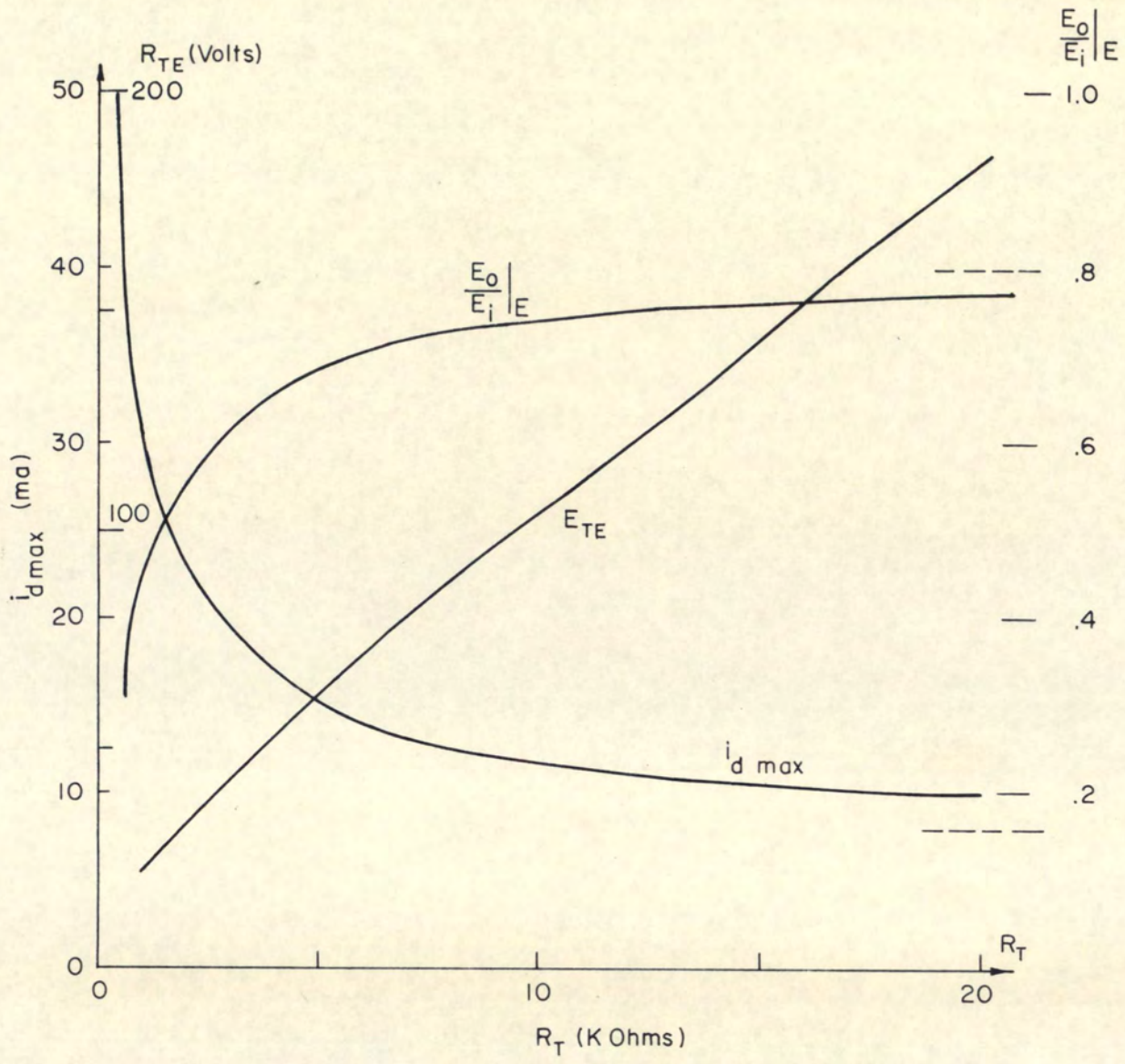

Fig. 3-7 The Design of a Balanced Trigger Source

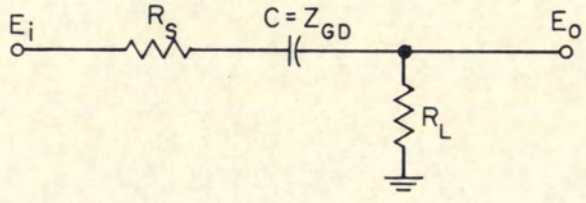

Fig. 3-8 A Disabled Series Gate

compute the final value of the output voltage due to this ramp, and then to adjust the variables to keep this error below a predetermined minimum. Eq. 3-14 is an expression for the disabled gain. Eq. 3-15 is an expression for the actual output. And lastly, Eq. 3-16 is the final value of the output.

$$\left.\frac{E_o}{E_i}\right| D = \frac{R_L C_s}{(R_s + R_L) C_s + 1} \qquad 3.14$$

$$E_o = \frac{R_L C_s}{(R_s + R_L)C_s + 1} \times \left(\frac{\Delta E}{\Delta t}\right) \frac{1}{S^2} \qquad 3.15$$

$$e_{omax} = \lim_{S \to o} S E_o = \left(\frac{\Delta E}{\Delta t}\right) R_L C \qquad 3.16$$

For a numerical example, let us assume that the disabled gate appears as a capacitor of value 25×10^{-12} farads (which is typical for a diode gate), and that the input voltage changes 40 volts in 10×10^{-6} seconds. If the maximum allowed voltage read through is .02 volts, what is the largest value of R_L which we can use? The R_L to satisfy Eq. 3-16 is 2,000 ohms. This or a lower value of R_L will reduce the disabled gain to an allowable value. Most calculations which are made for the enabled gate favor a large value of R_L. The difficulties are then encountered in attempting to use this resistor in the enabled gate and still maintain enabled gain, linear range and linearity.

3.4 THE DIODE SERIES GATE WITH FLOATING TRIGGER

The next gate which we will consider is the logical extention of the diode series gate to the floating trigger case (Fig. 3-9). The analysis of the balanced trigger gate when E_{TE} and R_T are very large is similar in many respects to this gate. The gate of Fig. 3-9 is enabled with a positive

trigger voltage and disabled with a negative trigger voltage. A model a little more elaborate than the ideal diode can easily be used for this gate.

If the diodes are assumed to have a forward or conducting resistance of r_f and a back resistance of r_b, the results as illustrated in Fig. 3-10 can be obtained for gate gain and linear range. Unlike the previous gates the disabled range of this gate is not infinite. This is not due to the fact that a different model is being used for the gating elements, but is a property of the configuration.

An alternative approach can be used to calculate E_o vs E_i plots for the floating trigger gate. The gating elements, including the trigger source can be considered to be a two terminal impedance. This impedance, Z_G, is non-linear. A plot of e_g vs i_g can be calculated once the model for the diodes has been chosen. On this same graph the load line $E_i = (R_s + R_L)\, i_g + e_g$ can be drawn. The intersection of these two curves determines the operating point of the gate. By varying E_i and recording corresponding values of i_g the plots of E_o vs E_i can be obtained. This method of analysis will be used to find an estimate of the linearity of the floating trigger four diode series gate.

The first step in determing this linearity is therefore to find the e_g vs i_g plots for the enabled series element. Let us assume that the four diodes of the gate are equal and that some diode curve $e_d = f(i_d)$ is given. Fig. 3-11 illustrates the circuit which we are now interested in. Many equations can be immediately written down by inspection.

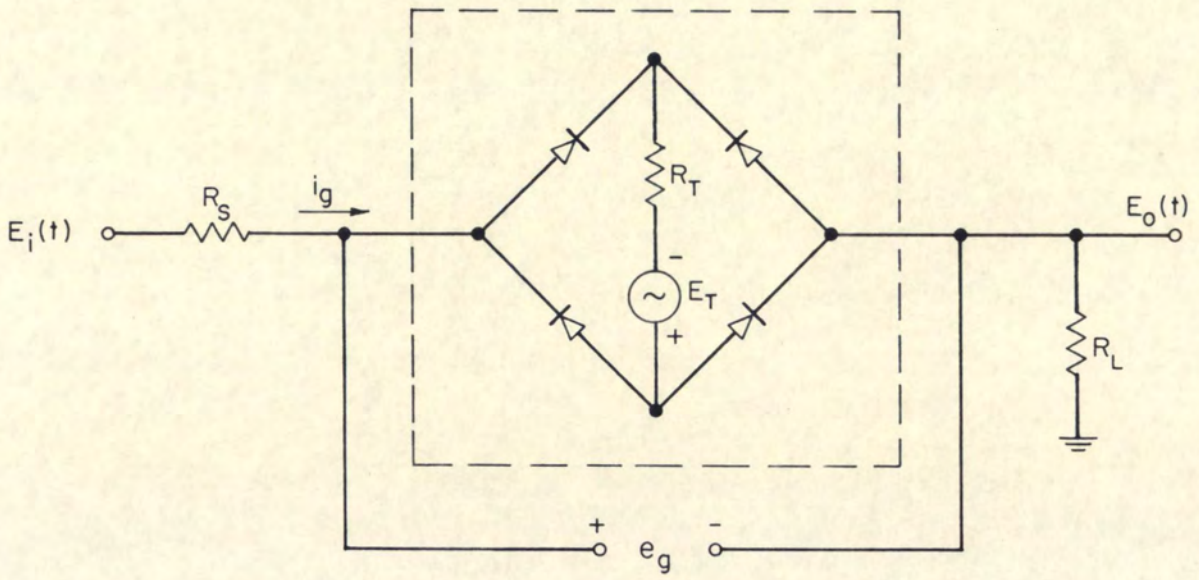

Fig. 3-9 Four Diode Bridge Gate with Floating Trigger

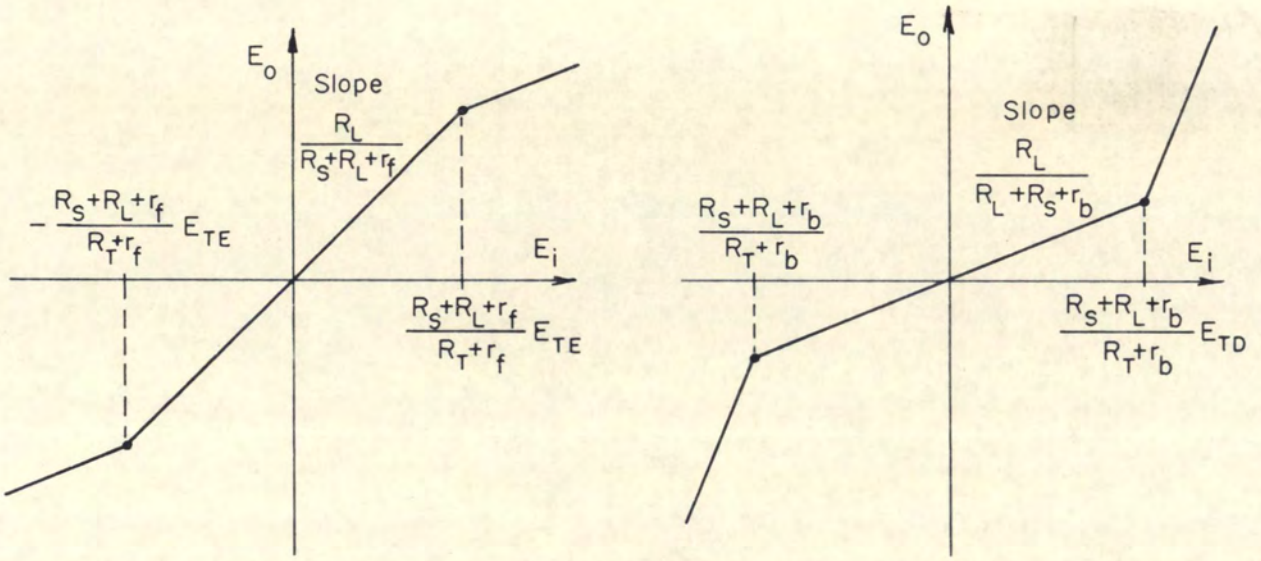

Fig. 3-10 Trigger Four Diode Gate's Enabled Floating and Disabled Gain

$$E_T = e_1 + e_3 + i_T R_T \qquad 3.17a$$

$$E_T = e_2 + e_4 + i_T R_T \qquad 3.17b$$

$$e_g = e_3 - e_4 \qquad 3.17c$$

$$e_g = e_2 - e_1 \qquad 3.17d$$

$$i_g + i_1 = i_3 \qquad 3.17e$$

$$i_3 + i_4 = i_T \qquad 3.17f$$

$$i_1 + i_2 = i_T \qquad 3.17g$$

$$i_4 + i_g = i_2 \qquad 3.17h$$

If we interchange subscripts 1 with 4 and 2 with 3 the set of equations remains unchanged. This symmetry plus the fact that the diodes are equal proves that $e_1 = e_4$ and $e_2 = e_3$ and of course $i_1 = i_4$ $i_2 = i_3$. This reduces the eight equations above to the four below.

$$E_T = e_1 + e_2 + i_T R_T \qquad 3.18a$$

$$e_g = e_2 - e_1 \qquad 3.18b$$

$$i_g + i_1 = i_2 \qquad 3.18c$$

$$i_1 + i_2 = i_T \qquad 3.18d$$

The voltages e_1 and e_2 are replaced with $f(i_1)$ and $f(i_2)$ respectively.

$$E_T = f(i_1) + f(i_2) + i_T \qquad 3.19a$$

$$e_g = f(i_2) - f(i_1) \qquad 3.19b$$

$$i_g + i_1 = i_2 \qquad 3.19c$$

$$i_1 + i_2 = i_T \qquad 3.19d$$

From Eq. 3-19c and Eq. 3-19d we can solve for i_1 and i_2 in terms of i_g and i_T.

$$i_1 = \frac{i_T - i_g}{2} \qquad 3.20a$$

$$i_2 = \frac{i_g + i_T}{2} \qquad 3.20b$$

These expressions are substituted into Eq. 3-19a and Eq. 3-19d to give Eq. 3-21

$$E_T = f\left[\frac{i_T - i_g}{2}\right] + f\left[\frac{i_T + i_g}{2}\right] + i_T R_T \qquad 3.2.a$$

$$e = f\left[\frac{i_T + i_g}{2}\right] - f\left[\frac{i_T - i_g}{2}\right] \qquad 3.21b$$

In order to proceed any further the function $e_d = f(i_d)$ must be specified. It can be given graphically or analytically. If $e_d = f(i_d)$ is given graphically the e_g vs i_g plot can be obtained by a procedure outlined in Appendix I. If it is given analytically there is the possibility that i_T can be eliminated from Eq. 3-21. Then e_g is known as, at least, an implicit function of i_g.

For an example let us assume that we have a square law diode as illustrated in Fig. 3-12. As long as all diodes are conducting a $\sqrt{i_d}$ can be substituted for $f(i_d)$ in Eq. 3-21. After a little algebra, including the elimination of i_T, the following equation results.

$$R_T e_g^4 - 2a^2 E_T e_g^2 + 2a^4 i_g e_g + a^4 R_T i_g^2 = 0 \qquad 3.22$$

For large positive i_g, the diodes D1 and D2 will be nonconducting. An equation for e_g vs i_g can be found by an inspection of the circuit. (Eq. 3-23

$$e_g = e_3 + i_g R_T - E_T + e_2 \qquad 3.23a$$

$$e_g = 2a\sqrt{i_g} + i_g R_T - E_T \qquad 3.23b$$

Eq.3-21 shows us that $e_g = h(i_g)$ is symmetric with respect to the origin, and therefore we need only consider positive i_g. Some terms of equation 3-22 and 3-23b are extraneous to the actual curve we are seeking. However, upon plotting these curves the unused portion can be removed by inspection.

Before plotting these curves a few special properties can be observed. Since a beeak point in $f(i_d)$ occurs at $i_d = 0$, a break point will occur in $e_g = h(i_g)$ when $i_g = i_T$ (from Eq. 3-21). Eq. 3-21a reduces to Eq. 3-24 at the break point. Eq. 3-24a applies as long as $f(i_d = 0) = 0$,

$$E_T - i_g R_T = f(i_g) \qquad 3.24a$$

$$E_T - i_g R_T = a\sqrt{i_g} \qquad 3.24b$$

and Eq. 3-24b applies for our example.

Another interesting and useful property of the gate is the incremental resistance of the gating element near the origin. By converting Eq. 3-22 to polar coordinates (r,θ) and solving for $\tan\theta$ when $= 0$ the resistance can be found (Eq. 3-25.)

$$r_g\Big|_{\substack{i_g = 0 \\ i_g = 0}} \triangleq r_g = \frac{R_T}{\sqrt{1 + \frac{2 E_T R_T}{\partial 2}} - 1} \qquad 3.25$$

This resistance could also be found by solving first for the current in the diodes when $i_g = 0$. This current, which is the same for all diodes, determines an operating point or an incremental resistance of the diodes. This incremental resistance of one diode is the incremental resistance of the gate near the origin.

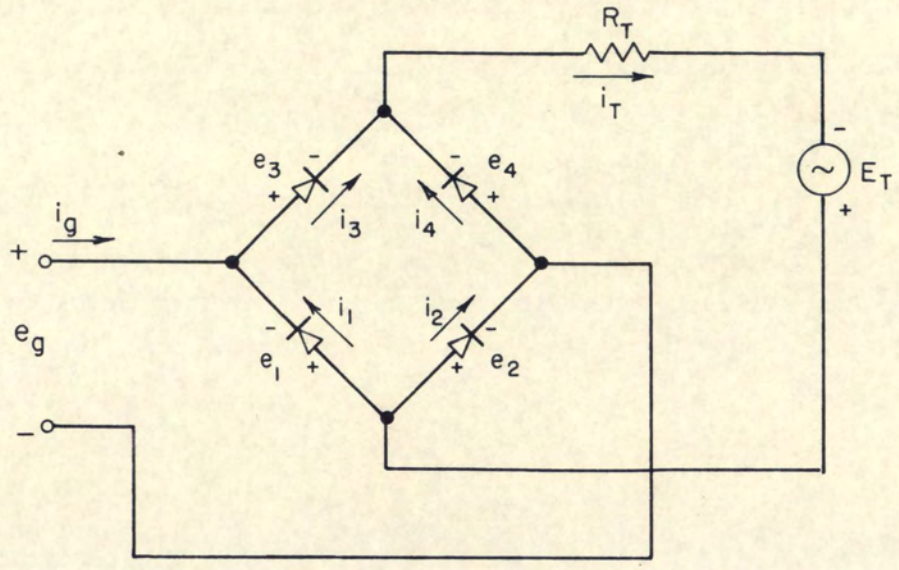

Fig. 3-11 Four Diode Series Element with Floating Trigger

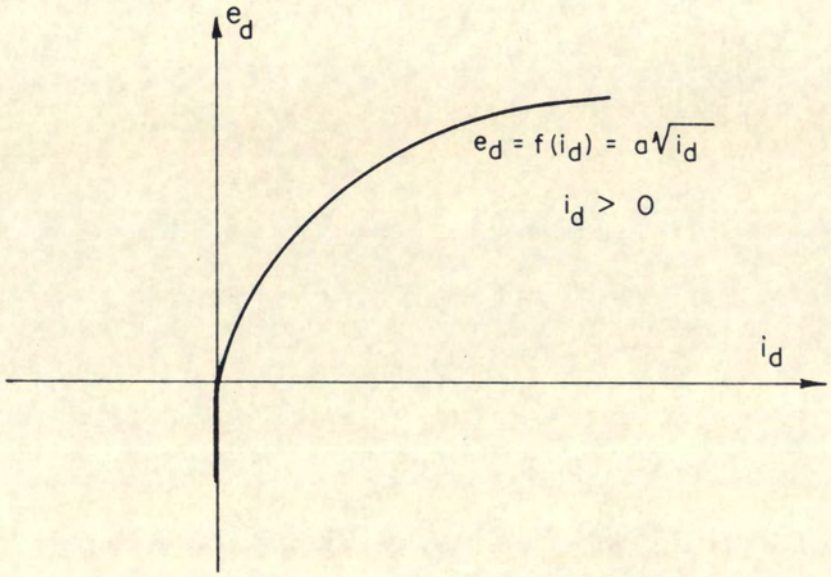

Fig. 3-12 Square Law Diode

Fig. 3-13 contains plots of e_g vs i_g for a few extreme combinations of trigger voltage and resistance. The value of a has been taken to be 10 $\frac{\text{Volts}}{(\text{amps})^{1/2}}$. The trigger source is a 10 ma current source for curve I. The resistance at the origin is 50 $\sqrt{2}$ ohms. All combinations of E_t and R_T which result in 50 $\sqrt{2}$ ohms of incremental resistance near the origin will lie between curve Iand curve II. Curve II is the other extreme case, where the trigger source is a pure voltage source. In actually building a trigger source the current requirements placed on this source are important. Therefore the trigger current has been plotted for each trigger source. If we vary E_T and R_T such that the break point or maximum trigger current required remains at a constant 10 ma, we will vary from curve I to curve III. It has been obvious from the start that non-linearities in the input source resistance R_s result in gate transmission non-linearities. In the gate which we are now considering non-linearities in R_T also contribute to non-linearities in gate transmission.

The smaller the value of R_T, the closer to perfect linearity is this ideal gate. The current source trigger represents the extreme case of non linearity and the deviation from linearity has been plotted in Fig. 3-14. The resistance of the gate near the origin has been taken as a reference in order to compute ideal gate gain. This curve has been plotted for $R_s = 0$ and $R_L = 2000$ ohms.

While these results are realistic in that non linear diode curves have been used, they are not realistic in that the four

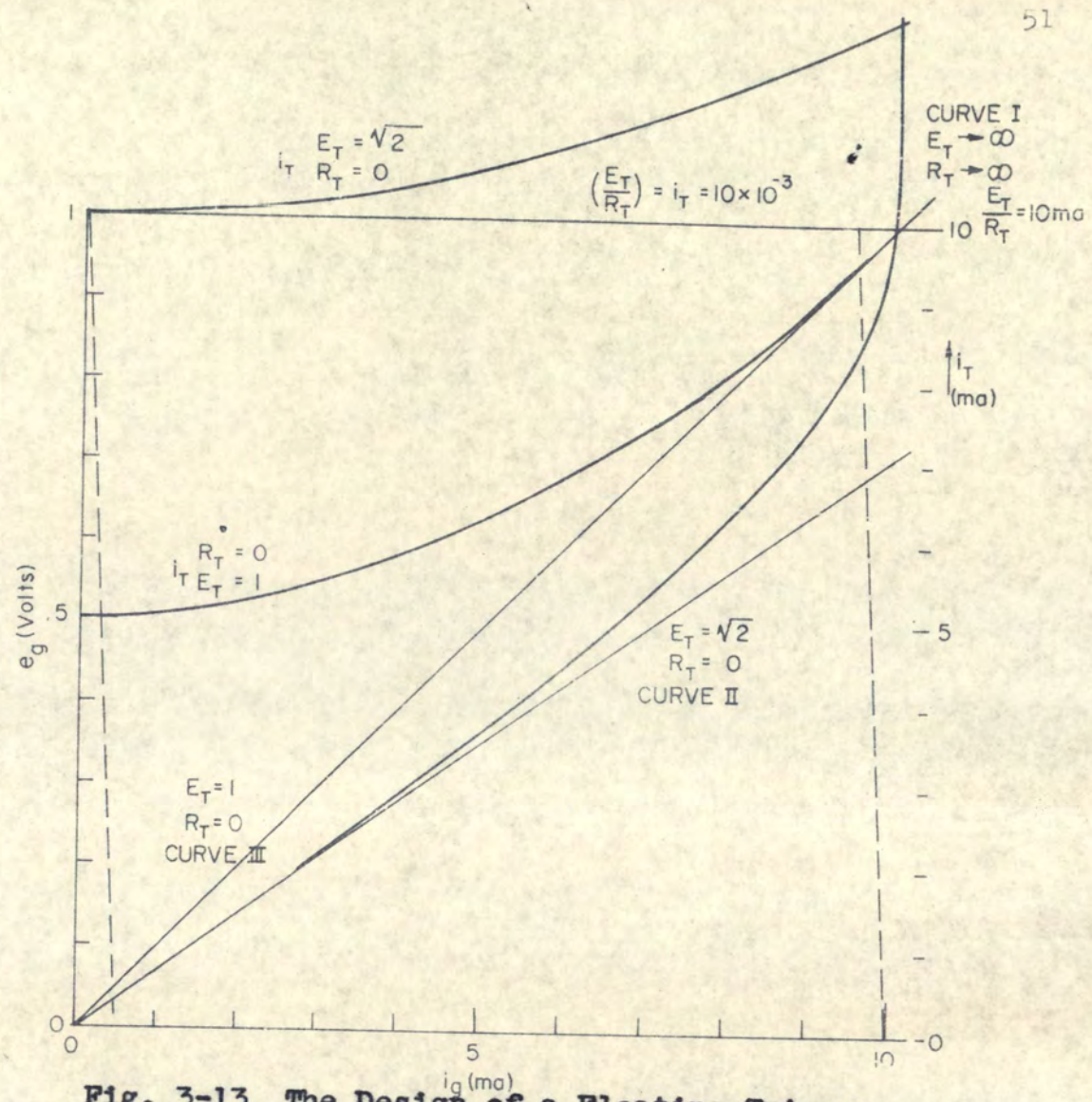

Fig. 3-13 The Design of a Floating Trigger Source for Four Diode Gate. Square law Diodes ($e_d = 10\ i_d$) Are Used in This Gate.

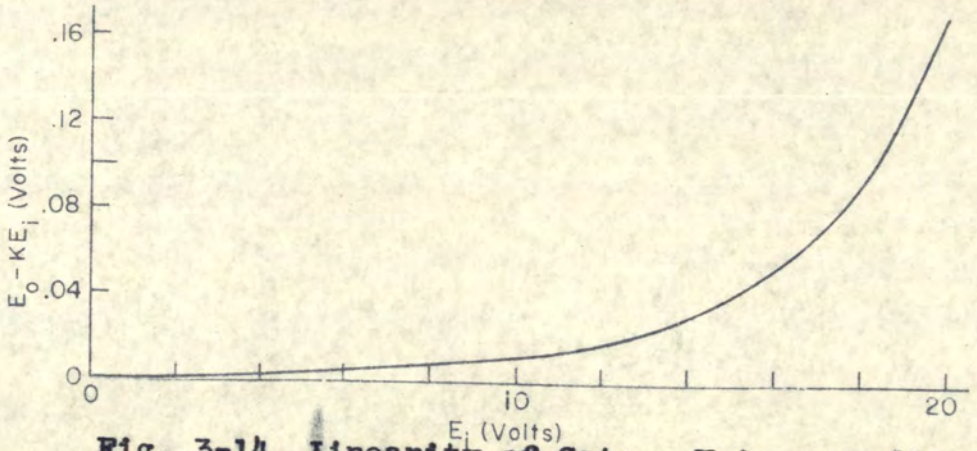

Fig. 3-14 Linearity of Gate. K is normalized to be 2000 ÷ 2000 + 50 2

diodes have been assummed to be identical. The most important effect of an unbalance in the diodes is to shift the $e_g = h(i_g)$ plot from the origin $i_g = o$, $e_g = 0$. In practice this voltage is rather unpredictable but may be brought to a reasonably small value by either an offset bias or by carefully matching diodes.

In order to make any statements about the switching speed of the four diode gate we must establish a model for the diode which includes switching effects. The diode D of Fig. 3-15 is statically the same as the diode in Fig. 3-10. As the trigger voltage in any gate is assummed to change in a step fashion our model need only apply for step changes in voltage E_T. When the voltage E_T changes from $-E_{TD}$ to E_{TE} the current in the diode will go from $i_{dD} = -\frac{E_{TD}}{R_T + r_b}$ to $i_{dE} = -\frac{E_{TD}}{R_T + r_b}$ in zero time. That is, our diode will go from the non conducting to the conducting state as fast as the trigger voltage. However when the voltage changes from E_{TE} to $-E_{TD}$ the resistance of the diode will remain at r_f for an interval of time, T_s. This switching time depends on both the enabled current i_{dE} and on the reverse current $i_{dR} = -\frac{E_{TD}}{R_T + r_f}$. For our purposes $T_s = +K\frac{i_{dE}}{i_{dR}}$, where K is a property of the diode construction. Fig. 3-15 illustrates this switching.

If this diode model is inserted in the bridge of Fig. 3-9 the switching speed of the gate and the transients introduced upon switching depend upon the input voltage E_i. Let us consider two extreme cases. When the value of E_i is zero, the positive trigger voltage will cause an equal current to flow in each diode. An instananeous change in E_T from E_{TE} from E_{TE} to $-E_{TD}$ will

similarly cause an equal reverse current to flow in each diode. Because the diodes have all been subjected to identical conditions they will all become non conducting at the same instant. A different situation exists when E_1 is some large positive voltage. The currents in the diodes of the enabled gate are now unbalanced. In order to simplify an already over simplified argument let us assume that diodes D_1 and D_4 are conducting zero current. Diodes D_2 and D_3 are therefore conducting full trigger current. When the trigger voltage changes sign D_1 and D_4become high resistances instantly. An estimate of the reverse current in the diodes which are left conducting can be calculated from Fig. 3-16.

$$i_{dR} = \frac{(E_{TD} - E_1)}{R_s + 2r_f + R_L + R_T} \qquad 3.26$$

After a time $T_s = K \frac{i_{dE}}{i_{dR}}$ the gate will be completely disabled. During this switching a transient has been introduced at the output of the gate. This transient is illustrated in Fig. 3-17.

Since a crude model has been used for diode switching, we can only come to some crude conclusions about gate switching. A transient appears at the output of the four diode gate while switching from the enabled to the disabled state, which depends on E_1. This transient is a property of the gate configuration and switching characteristics of the diodes which can only be completely eliminated by using zero switching time diodes. While this transient may not be very aesthetic it is of no consequence in pulsed analog work provided it is sufficiently short. The storage gate which follows this sample gate need only come to the end of its enabled period before this transient starts.

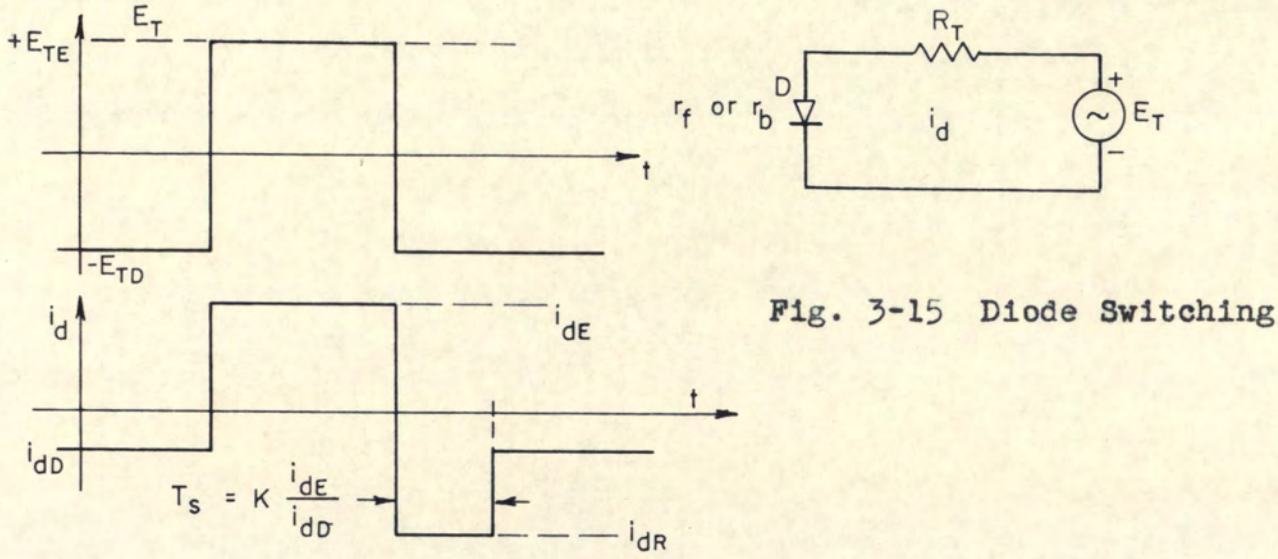

Fig. 3-15 Diode Switching

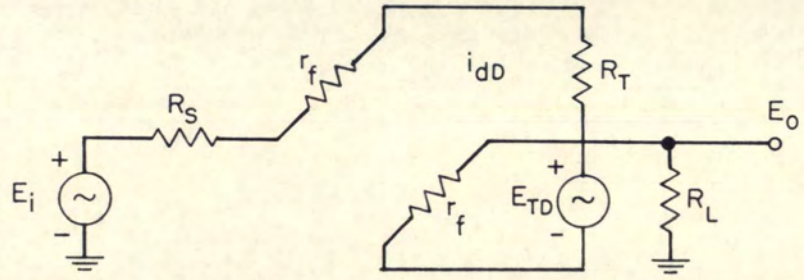

Fig. 3-16
Switching of Four Diode Gate

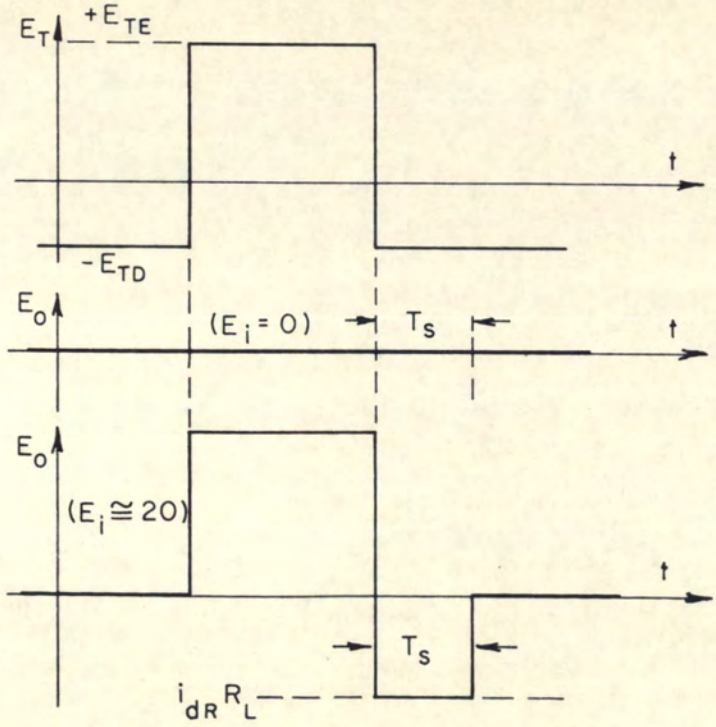

Fig. 3-17
Trigger Voltage and Output Transients

A four diode bridge gate can be built which meets the pulsed analog requirements. The gate has the disadvantage that an unpredictable bias, caused by an unbalance in diode characteristics, will have to be canelled out. Also in a series gate the linearity of the input source may be strained. In a series-shunt gate this difficulty could be eliminated. Using the four diode bridge as both a series and a shunt element a sample gate can easily be built to meet pulsed analog requirements. The transistor gate of Chapter 4 will also meet our requirements and offers some advantages over this diode gate.

CHAPTER IV

BILATERAL TRANSISTOR SAMPLE GATES

4.1 INTRODUCTION

In this chapter we will investigate the use of bilateral transistors as gating elements. A basic configuration is shown in Fig. 4-1. Once this basic element is understood special cases and more elaborate combinations can be considered. The transistor will operate in either the saturated or in the cutoff state. Fig. 4-2 adopts a simple model for the saturated transistor. When the trigger voltage E_T is large negative the diodes are conducting and have a resistance r_f. Expressions for i_{e1} and i_{e2} can be calculated (Eqs. 4-1, 4-2).

$$i_{e1} = \frac{\left[R_{12} - R_{22}\right] E_T + R_{22} E_1 - R_{12} E_2}{R_{11} R_{22} - R_{12} R_{21}} \qquad 4.1$$

$$i_{e2} = \frac{\left[R_{21} - R_{11}\right] E_T - R_{21} E_1 + R_{11} E_2}{R_{11} R_{22} - R_{12} R_{21}} \qquad 4.2$$

where

$$R_{11} \triangleq R_1 + r_{f1} + R_T$$

$$R_{22} \triangleq R_2 + r_{f2} + R_T$$

$$R_{12} \triangleq R_T + \alpha 1\, r_{f1}$$

$$R_{21} \triangleq R_T + \alpha 2\, r_{f2}$$

The value of the current in the diodes is important when we are calculating the point at which the transistor leaves saturation. Eq. 4-3 and Eq. 4-4 should satisfy this need.

$$Di_{d1} = \left\{ R_{22} - R_{12} + \alpha_1 R_{11} - \alpha_1 R_{21} \right\} E_T \qquad 4.3$$

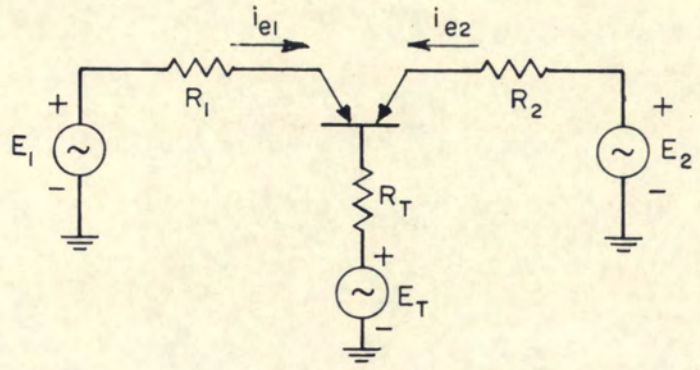

Fig. 4-1 A Basic Bilateral Transistor Configuration

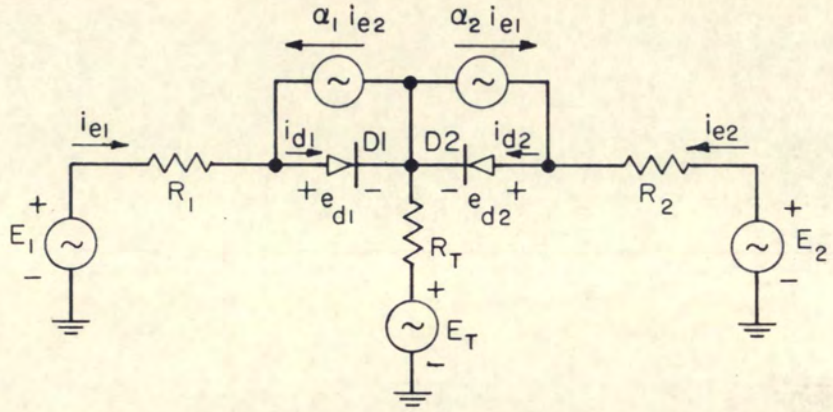

Fig. 4-2 Basic Configuration with Transistor Model

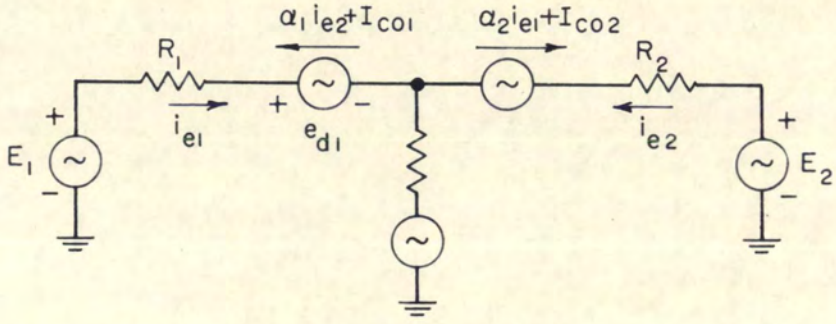

Fig. 4-3 Basic Configuration with Cutoff Transistor

$$+\left\{-R_{22}+\alpha_1 R_{21}\right\} E_1+\left\{R_{12}-\alpha_1 R_{21}\right\} E_2$$

$$Di_{d2} = \left\{R_{11}-R_{21}+\alpha_2 R_{22}-\alpha_2 R_{12}\right\} E_T$$

$$+\left\{R_{21}-\alpha_2 R_{22}\right\} E_1+\left\{-R_{11}+\alpha_2 R_{12}\right\} E_2 \qquad 4.4$$

where $D \triangleq R_{11} R_{22} - R_{12} R_{21}$

If in the reverse direction the diodes appear as resistances r_b, Eqs. 4-1 to 4-2 apply to the cutoff transistor simply be substituting r_b for r_f. A different model, which has been incorporated in Fig. 4-3,is often used for the cut off transistor. With this model all the currents of the circuit can be determined independent of the voltages and resistors. (Eq. 4-5, 4-6). The transitor will remain cutoff as long as the diode voltages e_{e1} and e_{12} remain negative. In practice the currents i_{d1} and i_{d2} are so small that

$$i_{e1} = \frac{\alpha_1 I_{co2} - I_{co1}}{1-\alpha_1 \alpha_2} \qquad 4.5$$

$$i_{e2} = \frac{\alpha_2 I_{co1} - I_{co2}}{1-\alpha_1 \alpha_2} \qquad 4.6$$

the voltage drops which they cause across the resistors are insignificant when computing linear range. Neglecting leakage currents in this way is identical to using ideal diodes in the model of Fig. 4-2. The diode voltages are then simply

$$e_{d1} = -E_T + E_1 \qquad 4.7$$

$$e_{d2} = -E_T + E_2 \qquad 4.8$$

4-2 THE SERIES TRANSISTOR GATE

Fig. 4-4 illustrates a bilateral transistor series sample gate

with a grounded trigger. This gate is the basic configuration with the modification that $E_2 = 0$. The output of the gate can be written down from Eq. 4-1, with the appropriate substitutions as indicated in Fig. 4-4. In many

$$E_{oE} = -i_{e2} R_L = \frac{\left\{R_{11}-R_{21}\right\} R_L (-E_{TE})}{R_{11}R_{22} - R_{12}R_{21}} + \frac{R_{21} R_L E_1}{R_{11}R_{22} - R_{12}R_{21}} \quad 4.9$$

cases the trigger resistance will be very large compared to the other resistances of the gate. With this approximation and using a perfectly symmetrical transistor Eq. 4-10 can be written. The term $2(1 - \alpha)\, r_f$

$$E_{oE} = \frac{\left\{R_s + (1-\alpha)r_f\right\} R_L}{R_s + R_L + 2(1-\alpha)r_f}\left[-\frac{E_{TE}}{R_T}\right] + \frac{R_L E_1}{R_s + R_L + 2(1-\alpha)r_f} \quad 4.10$$

is often referred to as the transistor saturation resistance r_{SAT}. The DC output of the disabled gate will be caused by the leakage current of Eq. 4-6.

$$E_{OD} = \frac{I_{co}}{1 + \alpha} RL \quad 4.11$$

An estimate of the linear range of this series gate can be obtained by using Eq. 4-3, 4-4. When in the enabled state we can, for this calculation, assume that $r_f = 0$. Eq. 4-12 and 4-13 are the expressions for the currents in the diodes.

$$Di_{d1} = -(R_L + \alpha R_s) E_{TE} - (R_L + (1-\alpha)(R_T)E_1 \quad 4.12$$

$$Di_{d2} = -(R_s + \alpha R_L) E_{TE} + (-\alpha R_L + (1-\alpha) R_T)E_1 \quad 4.13$$

where the value of D, which is positive, is of no consequence, i_{d1} will change sign for large negative E_1. The point at which this will occur

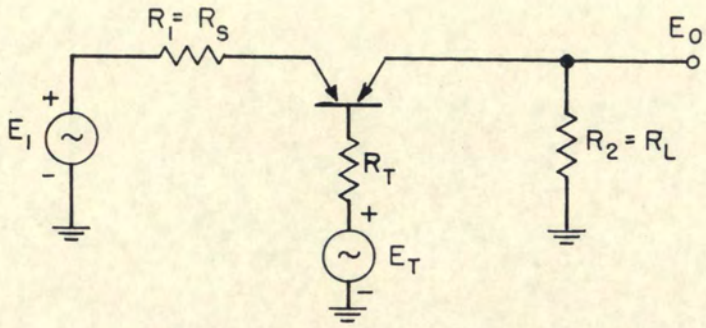

Fig. 4-4 Series Bilateral Transistor Gate with Grounded Trigger

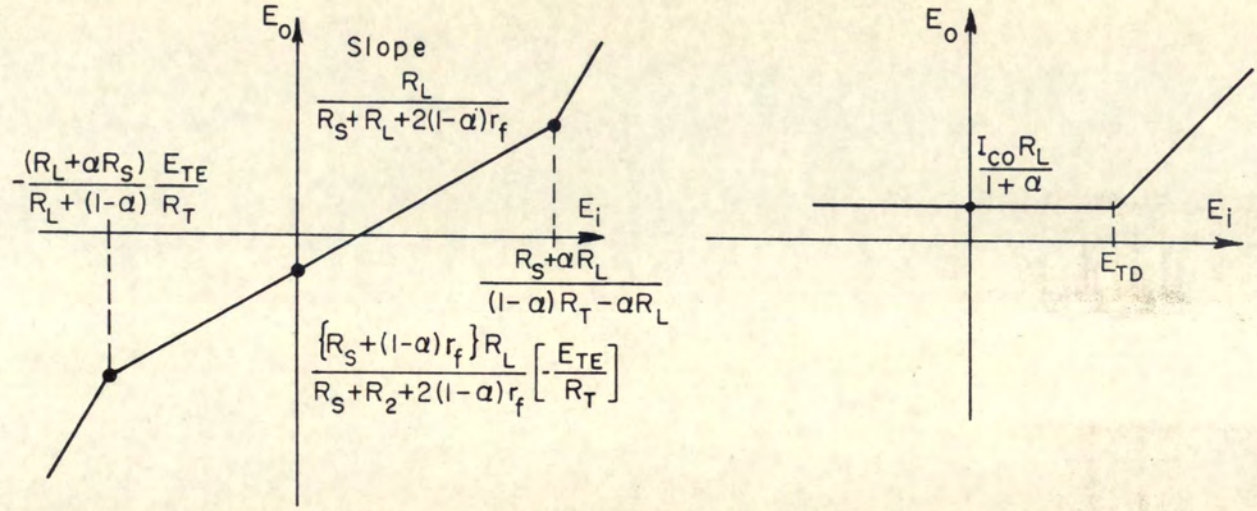

Fig. 4-5 Series Transistor Sample Gate

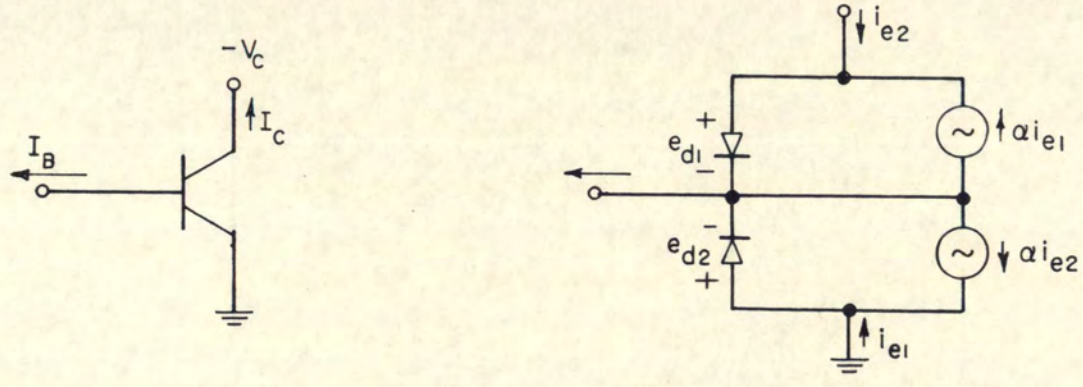

Fig. 4-6 The Grounded Emitter Transistor

is given in Eq. 4-14. The sign of the coefficient of E_1 in Eq. 4-13 can

$$E_{1B} = - \frac{(R_L + \alpha R_s)}{R_L + (1-\alpha)R_T} E_{TE} \qquad 4.14$$

be either positive of negative depending on the relative magnitudes of R_L, R_T and α . The break point can therefore be either positive or negative. This break point will occur when

$$E_{1B} = - \frac{(R_s + \alpha R_L)}{\alpha R_L - (1-\alpha)R_T} E_{TE} \qquad 4.15$$

If E_1 as calculated in Eq. 4-14 is negative than E_1 can go no more negative than this value. If the calculated value of E_1 is positive than E_1 can go no more positive. If Eqs. 4-14 and 4-15 both demand a negative break point, the smallest one obviously applies. If the trigger source is a current source both breaks are roughly equal in magnitude but opposite in sign (Eq. 4-16, 4-17).

$$E_{1B} = - \frac{(R_L + \alpha R_s)}{(1-\alpha)} \left[\frac{E_{TE}}{R_T}\right] \qquad 4.16$$

$$E_{1B} = \frac{R_L + \alpha R_s}{1-\alpha} \left[\frac{E_{TE}}{R_T}\right] \qquad 4.17$$

From Eq. 4-8 the transistor of the disabled gate will leave the cutoff condition when

$$E_1 = + E_{TD} \qquad 4.18$$

The disabled gate will remain linear for all negative input voltages. All break points for this gate have now been determined using ideal diodes in the transistor model. The gates transmission characteristics, with a current source enabled trigger, are

summarized in Fig. 4-5.

A non-linear and more realistic model for the bilateral transistor can be obtained by replacing the two diodes in the model used in Fig. 4-2 with non-linear diodes $e_d = f(i_d)$.[8,9] This diode function can be determined by direct measurement. The transistor curves for the grounded emitter configuration, V_c vs I_c with I_b as a parameter, are often given or can be easily measured. From our model, Fig. 4-6b, we should be able to predict these curves. By writing down all the equations associated with Fig. 4-6 and making a few appropriate substitutions we can arrive at the grounded emitter characteristics (Eq. 4-19). The saturation resistance which appears

$$V_c = f\left\{I_B + (1-\alpha)I_c\right\} - f\left\{\alpha I_B - (1-\alpha)I_c\right\} \qquad 4.19$$

directly on the grounded emitter curves is defined to be

$$r_{SAT} \triangleq \left.\frac{\partial V_c}{\partial I_c}\right|_{I_c = 0} \qquad 4.20$$

The is consistant with our previous example of a transistor in which $f(i_d) = i_d r_f$ and $r_{SAT} = 2(1-\alpha)r_f$.

It is rather difficult to use this model which we have established in the general series gate of Fig. 4-4. However a few special but useful cases can be discussed. For example if i_{TE} is fixed, a load line

$$E_1 = -R_s I_c - V_c - (i_{TE} + I_c) R_L \qquad 4.21$$

can be drawn and a plot of gate linearity easily obtained.

The diode function is very likely to be of the form

$$e_d = K_1 \ln\left\{1 + \frac{id}{I_{co}}\right\} \qquad 4.22$$

in which case we case we can compute the grounded emmitter characteristics to be

$$V_c = K_1 \ln \left\{ \frac{I_{co} + I_B + (1-\alpha)I_c}{I_{co} + \alpha I_B - (1-\alpha)I_c} \right\} \qquad 4.23$$

The saturation resistance is then

$$r_{SAT} = \left. \frac{\partial V_c}{\partial I_c} \right|_{I_c = 0} = \frac{2K_1(1-\alpha)}{I_B} \qquad 4.24$$

Eq. 4.24 includes the approximation that $I_B \cong \alpha I_B$ and $I_B \gg I_c$. Close to the origin of the V_c vs I_c plot Eq. 4-23 can be approximated as Eq. 4-25.

$$V_c = \frac{2(1-\alpha)K_1}{I_B} I_c \qquad 4.25$$

Small but important errors in the enabled transmission of this gate can be predicted analytically using the non-linear transistor model. In this method certain assumptions are made whose validity must be checked after the final results have been obtained. The assumptions which we use amount to using a different transistor model to make different calculations. The trigger current, for example, is calculated using the ideal diode model. In the pulsed analog case, where R_s is the output impedance of an operational amplifier and R_L is the input impedance of an operational amplifier, Eq. 4-25 will determine i_{TE}. Two voltages are neglected because of their small value.

$$i_{TE} = \frac{E_i + E_{TE}}{R_T} \qquad 4.25$$

The trigger current will flow mainly through the source resistance, R_s. The resulting voltage drop, at its maximum value, is assumed to be small (less than 1×10^{-3} volts). A voltage drop will

develop across the collector of the transistor due to the unbalance in i_{e1} and i_{e2}. This voltage can be computed from the grounded emitter characteristics (Eq. 4-27.) This

$$V_c = + K_1 \ln \left\{ \frac{1}{\alpha} \right\} \qquad 4.27$$

voltage is also assumed to be negligibly small.

The next gate error is caused by the fact that r_{SAT} varies with I_b. The gain of the gate is now

$$\left. \frac{E_o}{E_i} \right| E = \frac{R_L}{R_L + r_{SAT}} \qquad 4.28$$

where R_s has been neglected because it is small and it is constant. Combining Eq. 4-24, 4-26 and 4-28 we can arrive at Eq. 4-29. This equation

$$\left. \frac{E_o}{E_i} \right| E = \frac{R_L}{R_L + \frac{2(1-\alpha)K R_T}{E_i + E_{TE}}} \qquad 4.29$$

is then the non-linear gain of the series sample gate, where the non-linearities are caused by the fact that r_{SAT} varies with I_b. $E_o - K E_i$ is the error caused by this gate, where K is selected to be the value of $\left. \frac{E_o}{E_i} \right| E$ when $E_i = 0$. By performing this subtraction a direct expression for gate error is obtained (Eq. 4-30). If K is assumed to be unity the gate error is given by Eq. 4-31. The more gross non-linearities, those caused by the

$$E_o - K E_i = \frac{2 (1-\alpha) K_1 R_T E_i^2}{R_L E_{TE} (E_i + E_{TE})} \qquad 4.30$$

$$E_o - E_i = \frac{2 (1-\alpha) K_1 R_T E_i}{R_L (E_i + E_{TE})} \qquad 4.31$$

curvature of the V_c vs I_c characteristics, have not yet come to play an important role in the gates operation. To show that this

is true, the errors predicted by Eq. 4-30 or 4-31 should be compared with the maximum deviation between Eq. 4-23 and 4-25.

4.3 THE SHUNT TRANSISTOR GATE

If the study of transistor gates were to parallel the study of diode gates the next gate which we would consider would be the balanced trigger gate of Fig. 4-8. Following this we would study the floating trigger gate. However we shall take a little different point of view and proceed with the study of a shunt transistor gate. The gate which we shall discuss is illustrated in Fig. 4-9. This gate is disabled with a positive trigger which saturates the transistor, and is enabled with a negative trigger which cuts off the transistor. A basic configuration similar to Fig. 4-1 but which has the PNP transistor replaced by a NPN is shown in Fig 4-10. A model for the NPN transistor which corresponds to the model of the PNP of Fig. 4-2 can be inserted in this figure. Eq. 4-1 to Eq. 4-8 will then apply exactly to this configuration. By making the proper identifications the enabled and disabled outputs of the gate can be established. (Eq. 4-32, 4-33). With the usual approximations that

$$E_{OE} = E_i + \frac{\alpha_1 I_{co2} - I_{co1}}{1-\alpha_1 \alpha_2} (R_s + R_G) \qquad 4.32$$

$$E_{OD} = E_i - \frac{(R_{22}-R_{12}) E_{TD} + R_{22} E_i}{R_{11}R_{22} - R_{12}R_{21}} (R_s + R_G) \qquad 4.33$$

the transistor is perfectly symmetrical and the assumption that R_T is very large, Eq. 4-32 and 4-33 are modified to give Eq. 4-34 and 4-35.

$$E_{OE} = E_i - \frac{I_{co}}{1-\alpha} (R_s + R_G) \qquad 4.34$$

$$E_{OD} = \frac{E_i\left\{2(1-\alpha)r_f\right\}}{R_s + R_G + 2(1-\alpha)r_f} - \frac{(1-\alpha)r_f\,(R_s + R_G)}{R_s + R_G + 2(1-\alpha)r_f}\left[\frac{E_{TD}}{R_T}\right] \quad 4.35$$

The linear range can similarly be established. The enabled range will end when the diodes of the transistor are no longer back biased. This break will occur when

$$E_i = -E_{TE} \quad 4.36$$

No break will occur for negative Ei. The diodes of the disabled gate must remain conducting. The positive and negative break point in the disabled linear range will occur as mentioned in Eq. 4-37 and 4-38. This shunt gate's characteristics are summarized in Fig. 4-11.

$$E_{iB} = \frac{\alpha(R_s + R_G)}{1-\alpha}\ \frac{E_{TD}}{R_T} \quad 4.37$$

$$E_{iB} = -\frac{(R_s + R_G)}{1-\alpha}\ \frac{E_{TD}}{R_T} \quad 4.38$$

The trigger current for the shunt gate will remain constant over the entire range of operation due to the fact that one collector of the transistor is grounded. If the non-linear transistor which was used for the series gate is used in the shunt gate, the enabled characteristics are unaltered. The grounded emitter characteristics will apply directly in computing the gates disabled output voltage.

One of the main disadvantages of the shunt gate is the fact that in its design a compromise has to be made in adjusting the value of R_G. If R_G is made small the disabled element must remain linear over a large current range. If R_G is made large the output resistance of the enabled gate becomes correspondingly large. The

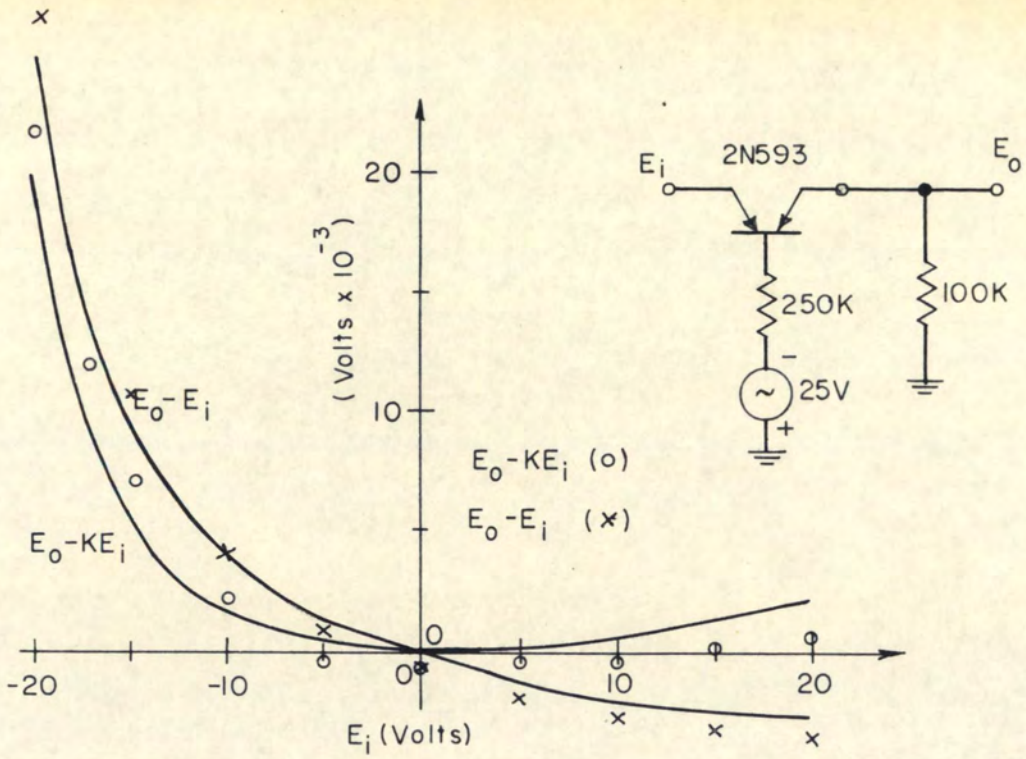

Fig. 4-7 Transistor Gate Linearity

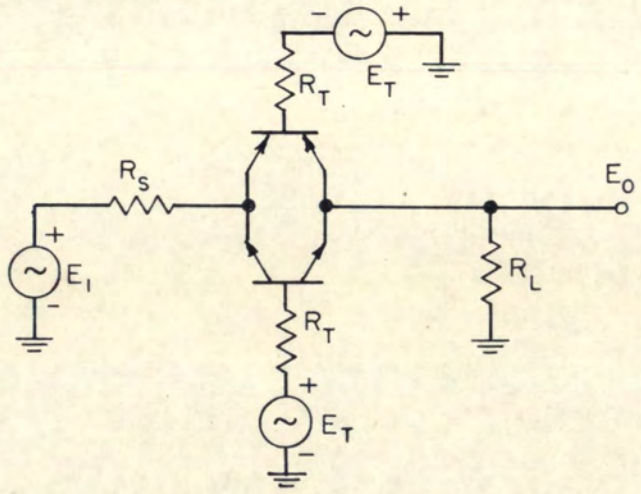

Fig. 4-8 Balanced Trigger Transistor Series Gate

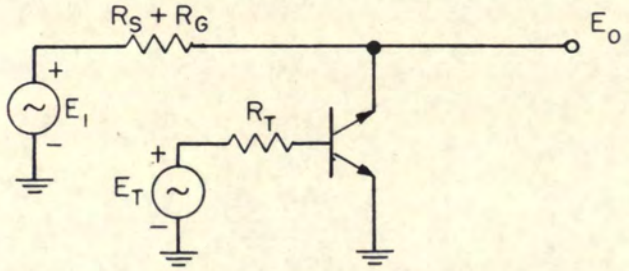

Fig. 4-9 Shunt Transistor Sample Gate

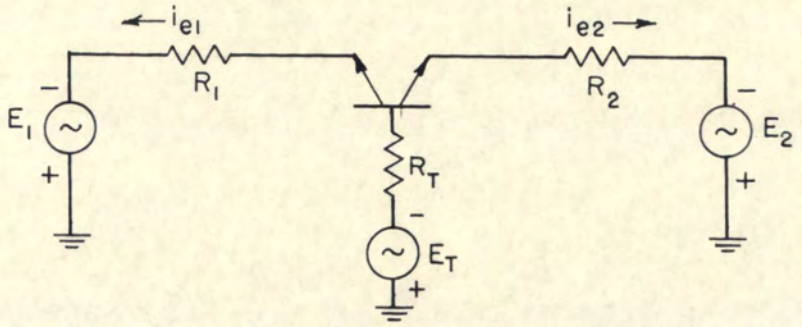

Fig. 4-10 General Configuration with NPN Transistor

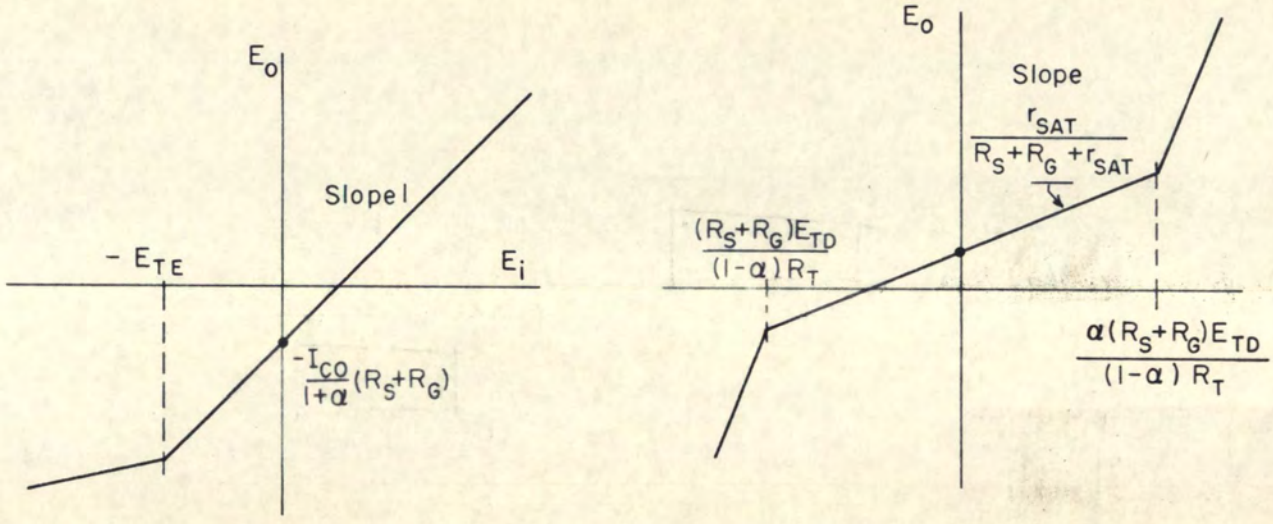

Fig. 4-11 Shunt Transistor Gate Characteristics

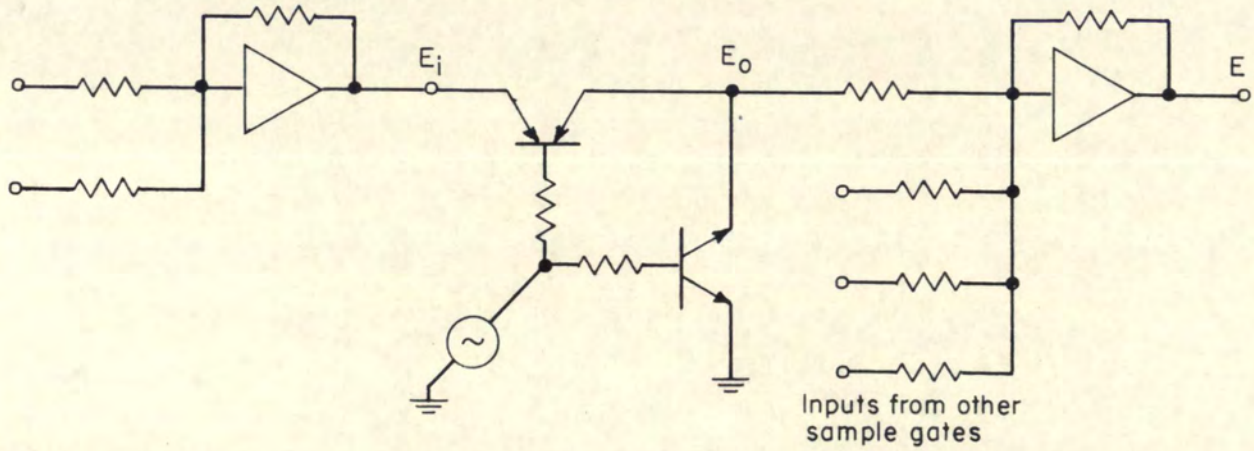

Fig.4-12 The Series-Shunt Gate and its Reverse Environment

series-shunt gate eliminates this difficulty. The series-shunt gate also eliminates the major disadvantage of the series gate, which is capacity read through.

4.4 THE SERIES-SHUNT TRANSISTOR SAMPLE GATE

In this section we will become very practical and complete the design of a series-shunt gate which can be used in the pulsed analog computer. For a series gating element we will use the PNP symmetrical transistor. For a shunt element we will use the NPN symmetrical transistor. The gate and its enviorment are illustrated in Fig. 4-12. R_s, the output resistance of the first operational amplifier is assumed to be less than 1 ohm. The load resistance is assumed to be 100KΩ . Now that we have decided upon a gate configuration and the gates input and output conditions have been specified, little remains to be designed. Once the transistors have been selected from the limited number which are immediately available, only the two trigger source resistors and the trigger voltage remain to be specified. Our previous experience with transistor gates will prove valuable in designing this gate.

The first model which we shall use for the gating element is the transistor model with the ideal diodes. In the enabled state, with E_T positive, the equations which were developed separately for the series gate and shunt gate can be used. The cut off transistor T2 can be completely ignored, provided both diodes are always back biased. The cutoff transistor T2 can be continued to be ignored as more elaborate models for the saturated transistor are adopted. All previous analysis for the series enabled gate can be used. Finally a realistic leakage current model for the cut

off transistor can be inserted to show that it does not affact the gate output.

The series enabled gate which was given as an example previously applies exactly to our gate. Experimental curves for the diodes in the transistor model are given in Fig 4-13 and 4-14. The diode function $e_d = f(i_d)$ can be approximated analytically as

$$i_d = 3\times10^{-6}\left\{e^{\left\{\frac{e_d}{3.75\times10^{-2}}\right\}} - 1\right\} \qquad 3.39$$

With the value of measured to be .967 our model for the transistor is complete.

The saturation resistance of the transistor can now be calculated. Fig. 4-15

$$r_{SAT} = \frac{2.5\times10^{-3}}{I_b} \qquad 4.40$$

compares measured and calculated values of r_{SAT}. The maximum value of r_{SAT} in our gate will be 125Ω . The maximum value of leakage current from the cut off transistor is 6×10^{-6} amps. The maximum voltage error which this could produce is less than 1×10^{-3} volts and can therefore be neglected. Fig. 4-7 is a theoretical and measured plot of this gate errors. This plot was actually made with and without the series element to show that the disabled shunt element does not effect gate output.

In the disable gate, with E_T negative, the non-linearities due to curvature of the V_c vs I_c characteristics and non-linearities due to saturation resistance varying with base current are not important and we must look to the small errors due to leakage current and base current. Fig. 4-16 is an illustration of the

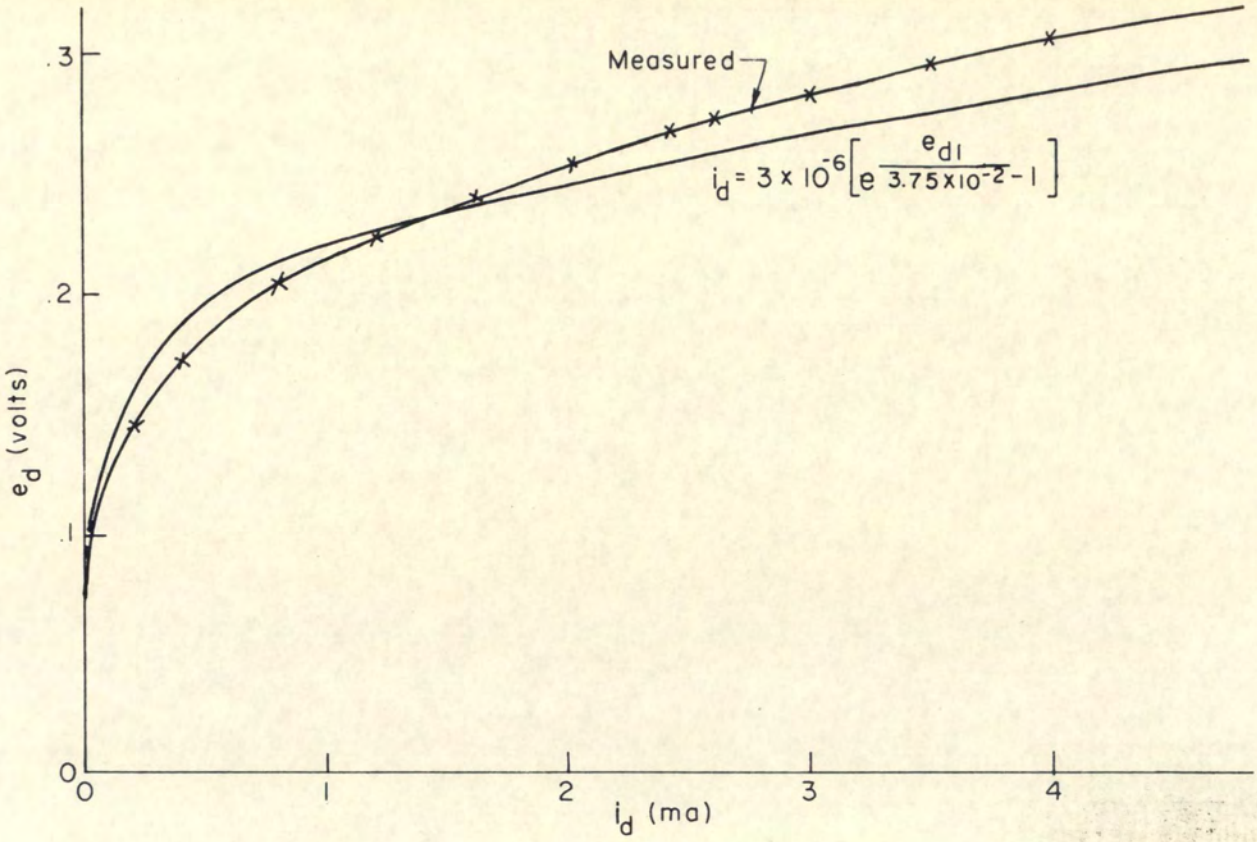

Fig. 4-13 Transistor Diode Forward Characteristics

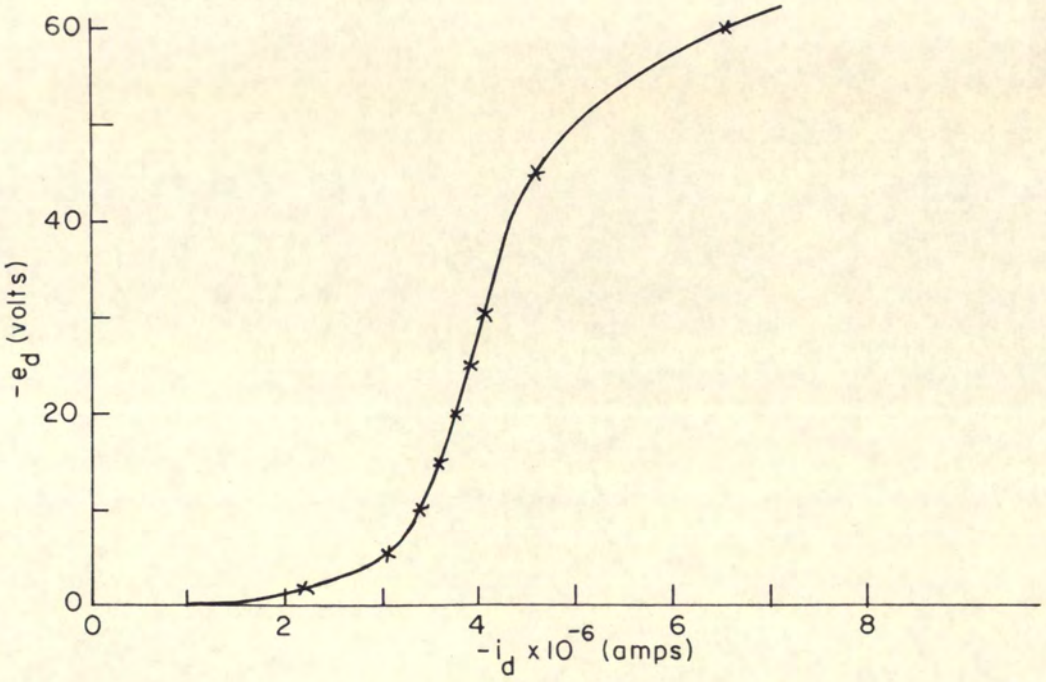

Fig. 4-14 Transistor Diode Reverse Characteristics

circuit which we are now considering. The voltage E_o will be

$$E_{OD} = V_c - r_{SAT} I_c \qquad 4.41$$

V_c can be computed from the grounded emitter characteristics to be approximately $K_1 \ln(1/\alpha)$. An exagerated value of E_{OD} would be less than 1×10^{-3} volts. While not important for a single gate this voltage does place become important when several of these gates form the inputs to a summer. It does place one type of limit on the number of inputs which can be applied to one summer. A value of R_{T2} of 1×10^{-6} would result in a saturation resistance of 100 Ω. Smaller values of R_{T1} and R_{T2} would further improve linearity but would increase switching speed. The complete gate, including a monostable multivibrator[10] which was designed for use with this gate, are shown in Fig. 4-18. Simple speed up techniques have been used to assure switching in less than 1 μ second.

One advantage of this gate is its simple trigger source. However, by using a separate trigger source for each element of the gate a more linear and a faster switching gate can be built. Eq. 4-30 shows that as the trigger source approaches a current source, the non-linearities due to r_{SAT} varying with base current becomes smaller. This could not be done with a single trigger source since the maximum back voltage of the shunt transistor is soon exceeded. Also if trigger current does not vary with input voltage, switching transients will not vary with input voltage. While it is very impractical to build a good current source trigger with transistors, an enabled trigger voltage of about 40 volts is very possible.

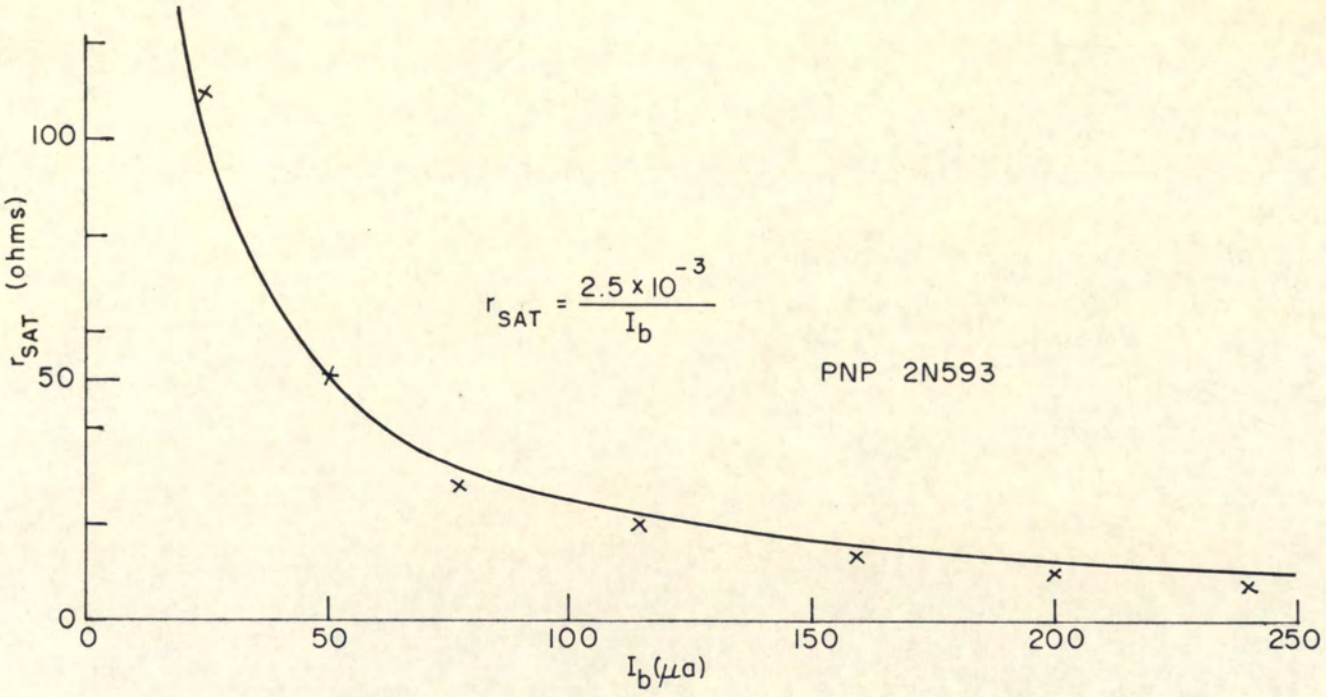

Fig. 4-15 Saturation Resistance VS Base Current

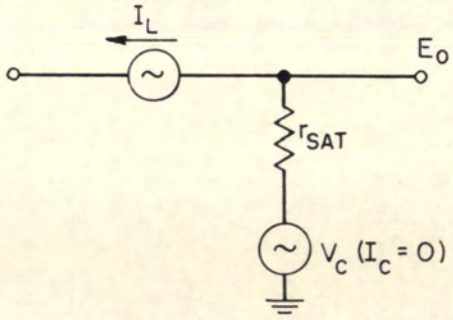

Fig. 4-16 The Disabled Series Shunt Gate

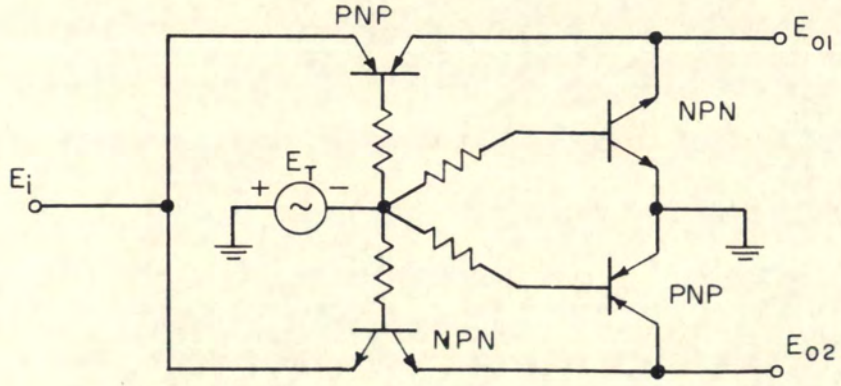

Fig. 4-17 The Monostable Multivibrator and Sample Gate

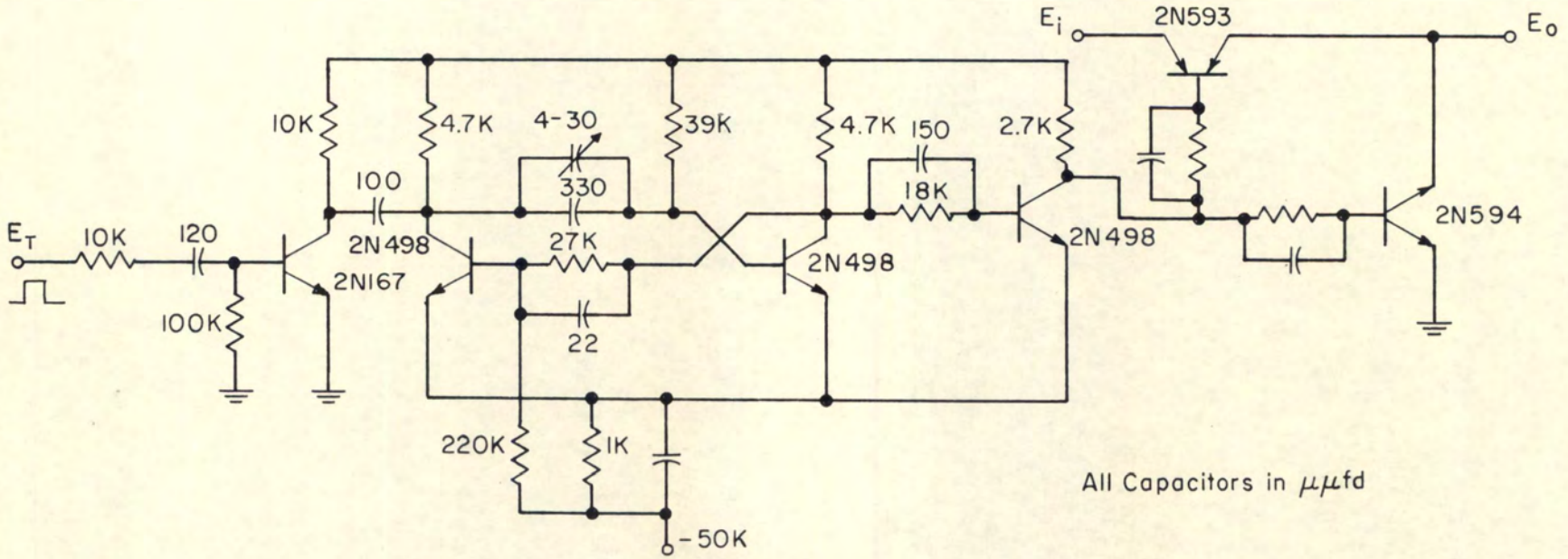

Fig. 4-18 Push-Pull Transistor Gate

Two more transistors can be easily added to the series-shunt gate which we have now built to construct a push-pull sample gate. (Fig. 4-17). One trigger source is still required to build this gate. This gate can now be included in a closed loop with an operational amplifier. While improvements in gate linearity can be achieved by this method a test set up found that amplifier noise and drift could not be separated from gate non-linearity. Switching transients also become more difficult to control due to the fact that amplifier response time was comparable to gate switching speed.

CHAPTER V

THE STORAGE GATE

5.1 BASIC DESIGN

The basic considerations which must be taken into account in the design of a storage gate are; set time, hold time, linear range of gating element, allowable error, and switching transients. A simplified schematic for a storage gate is shown in Fig. 5-1. R_s is the internal resistance of the source. Z_g is the gate impedance which as before takes on two values; Z_{gE}, the impedance of the enabled element, and Z_{gD}, the impedance of the disabled element. The actual storage is accomplished by holding charge on a capacitor C after the gate is disabled. R_o is the input impedance of the device which measures E_o. The storage gate is similar to the series sample gate in that any gating element used in the series sample gate can be used as a gating element of the storage gate.

The set time of a storage gate is defined as the maximum time required for the output of the enabled gate to change from its previous value to its new value. The set time for the linear and resistive circuit of Fig. 5-1 can be computed by assumming that at the beginning of the enabled period E_i is a maximum voltage + V_{max} and that E_o is a minimum voltage-V_{max}. The capacitor will charge expoentially toward V_{max} (Eq. 5-1). The large resistor

$$E_o(t) = + V_{max} - 2 V_{max} e^{\frac{-t}{(R_s + Z_{gE})C}} \qquad 5.1$$

R_o is neglected in this calculation. As E_o will never exactly reach + V_{max} an allowable enabled error must be specified in order to determine set time.

After the gate has become disabled the capacitor will retain the desired voltage within an allowable discharge error for a finite time τ_d. The minimum value of τ_d is called the hold time. If Z_{gD} and R_o are pure resistive, the maximum discharge current will occur when $E_i = -V_{max}$ and $E_o = +V_{max}$. The value of this current is given in Eq. 5-2. The voltage change during the period

$$i_d = \frac{2V_{max}}{Z_{gD}} + \frac{V_{max}}{R_o} \qquad 5.2$$

of interest will be so small that a constant discharge current will be assumed. The voltage change at the end of the holding period will then be

$$E_o = \frac{i_d}{C} \tau_d \qquad 5.3$$

The value of R_o is determined by an independent design and is neglected in a first consideration of a gates abilities. Usually the value of i_d is determined by the components used in the gate and little remains to be designed. Therefore Eq. 5-3 can be used to determine a minimum value of C.

The same three triggering methods as have been used previously can be used in the storage gate. Similarly the trigger voltage can effect the gates output. The current from the grounded trigger must flow back to ground through R_s and C. This will cause at least a constant bias error. The balanced trigger offers the possibility of eliminating this error. In both of these cases, if the trigger source is not a current source, a gate gain of less than unity will result. The floating trigger can circulate trigger current without necessarily introducing an error and also assures unity gain. For this reason, and the fact that it is easier to

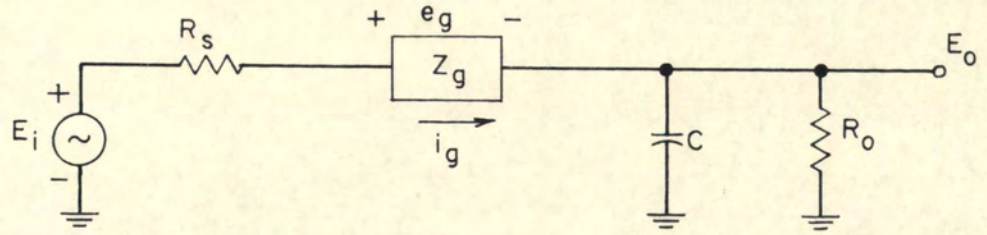

Fig. 5-1 A Simplified Storage Gate

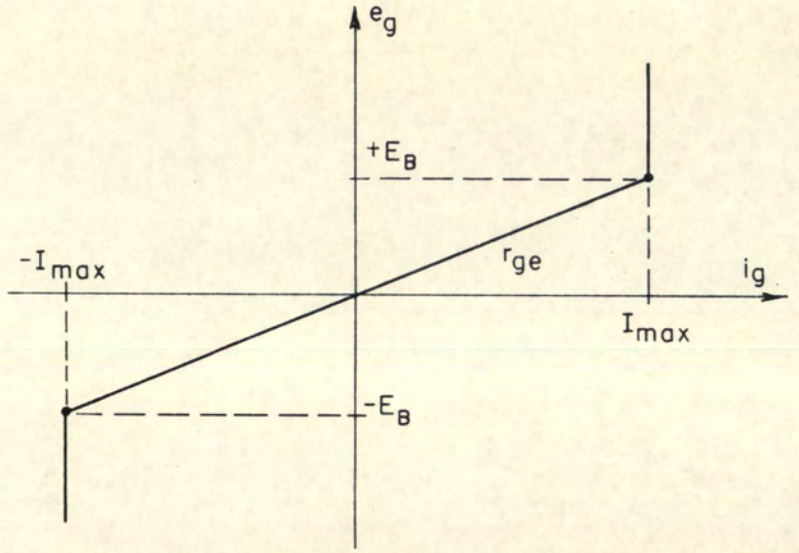

Fig. 5-2 An Extreme Case of Current Limiting in the Gating Element

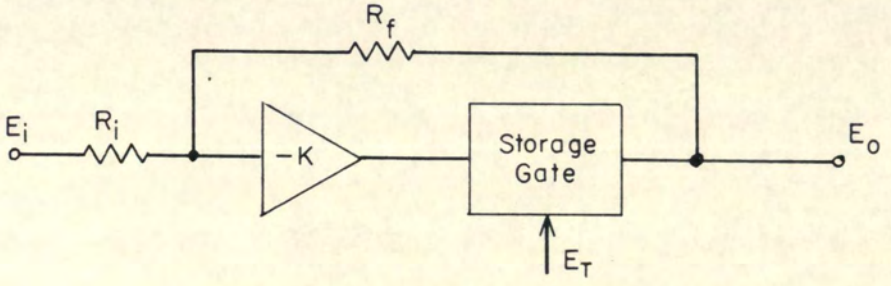

Fig. 5-3 Closed Loop Storage Gate

analyze, the floating trigger will be used in the remainder of this general design procedure.

In Fig. 5-1 the two terminal gating element can be thought of as including the trigger voltage and trigger resistor as well as including the gating elements. As we are using a floating trigger, there need be no other terminals to this box. The gates impedance can how be more accurately described by a plot of e_g vs i_g. In the enabled e_g vs i_g plot we will look for limitations on the current conducting ability of the series element, which will effect set time. In the disabled e_g vs i_g plot we will look for increases in the discharge current which will effect hold time.

Even in a simplified design procedure, the effect of current limiting in the enabled gating element cannot be neglected. This is because the value of C as chosen by Eq. 5-2 is often rather large. An extreme case of current limiting is illustrated in Fig. 5-2. The set time of this gate is effected by this non-linearity. If at the start of the enabled period the capacitor voltage if $-V_{max}$ and the input voltage has been set to $+ V_{max}$, the capacitor will charge linearly.

$$E_o(t) = - V_{max} + \frac{I_{max}}{C} t \qquad 5.4$$

This saturation will last until the break point of the e_g vs i_g plot is reached. This will occur when

$$\frac{E_o(t) - V_{max}}{R_s + Z_{ge}} = I_{max} \qquad 5.5$$

Following this the remainder of the charge will be completed exponentially with a time constant $(r_{ge} + R_s)C$.

Non-linearities in the series element of a floating trigger

storage gate do not contribute to the non-linearities of the gate output. This can be seen be considering Fig. 5-1 and the enabled e_g vs i_g plot. At the end of the set period i_g has been reduced to essentially zero. While e_g may not be zero when $i_g = o$, it will, at the end of each charging period, take on the same value. Therefore no non-linearity is introduced in the gates output due to non-linearities in Z_{ge}. An exception occurs in the case in which e_g is not single valued for $i_g = 0$.

Errors introduced upon switching from the enabled to the disabled state are very important in the storage gate. Special care must be taken to reduce these errors or to compensate for them.

The storage gates operation is even more dependent upon the external circuitry (input source, trigger source, and output buffer) than is the sample gate. Non-linearities in the input source and trigger source are reflected into the gates output behavior, not necessarily as a non-linear output voltage but as a limitation on the charging current available to the capacitor. The e_g vs i_g plot, which already includes the effect of trigger source voltage and resistance, can also include the effect on non-linearities in this source. A plot of the input capabilities is also appropriate and important. Non-linearities in R_s do not cause non-linearities in E_o since the current in R_s is always zero at the end of the set time. The output buffer stage also requires special design in that discharge current from the capacitor during the disabled period is very important. This completes the fundamentals of storage gate design. Below is a list which summarizes the important steps which are taken in the design of a storage gate.

1)) Get rough picture of gates operation by inspection

2) Choose model for gating element for each calculation

3) Determine e_g vs i_g plot

4) Choose value of C from hold time considerations

5) Calculate set time.

6) Estimate gate switching properties

7) Consider of design in more detail input source, output load and trigger source.

5.2 THE STORAGE GATE AND FEEDBACK

In the pulsed analog system the input to a storage gate is a feedback type amplifier. Two methods of using this amplifier have been proposed. Fig. 5-3 is a closed loop method, where, by including the gate in the loop, it is hoped that we can improve linearity and speed.[11] There are several reasons why this method has not proved to be practical. First the storage gate is already linear and needs no improvement of linearity. The system is rather difficult to stabilize due to the additional time constant which has been introduced. During much of the time the amplifier operates open loop and special design problems arise. Delays in the output buffer may also effect stability. Switching transients become more difficult to control and finally in a pulsed analog system this arrangement would require a separate input unit for each gate. The open loop system of Fig. 5-4 does not solve all the problems mentions above, but it is generally easier to use. First let us consider the additional stability problems introduced by the capacitive load. Fig. 1-16 illustrates the situation with which we are now concerned. R_d is the output resistance of the open

loop operational amplifier. R_g is the conducting resistance of the gate near $i_g = 0$. K includes all the time constants of the operational amplifier. Fig. 1-17 is a block diagram for Fig. 1-16. Fig. 1-17 shows that the addition of R_g and C amounts to a lag term in the closed loop amplifier. The problem is to correctly locate this lag filter and at the same time maintain proper set time and hold time. The factor K may also have to be modified. The smaller the value of R_d the easier will we be able to stabilize the system. In fact a little negative feedback could be used in the open loop amplifier final output stages to assure low open loop output impedance.

There also exists the possibility that low frequency oscillations can be introduced due to the non-linearities of the system. The current capabilities of the output driver are admittedly limited. If the output current i_o is symmetrically limited to $\pm I_m$, the block diagram of Fig. 5-5. can be drawn. Fig. 5-6 rearranges this block diagram and assumes that $k \gg 1$ and that the RC time constants are very small. These approximations only apply at low frequencies. The non-linearity of the system is symmetrical and therefore introduces no additional phase shift. It's describing function lies along the -180° line and above the 0dlg line on the Nichols chart. Any phase shift in K greater than 90° will cause the open loop transfer function to cross this describing function and the system will oscillate. Therefore low frequency lag compensation cannot be used in this system. The effect of any low frequency oscillation on the output of a storage gate with a 10×10^{-6} second enabled period would be difficult to predict. To avoid the problem of

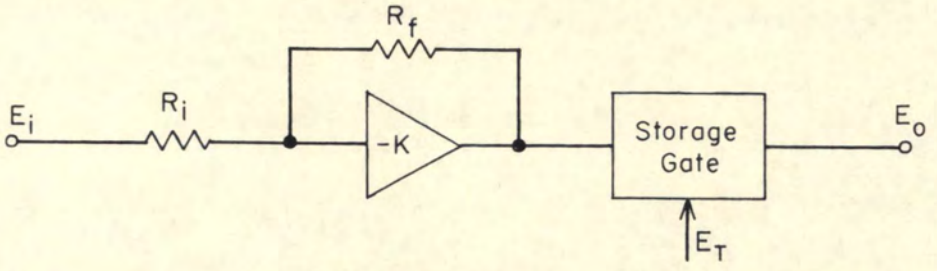

Fig. 5-4 Open Loop Storage Gate

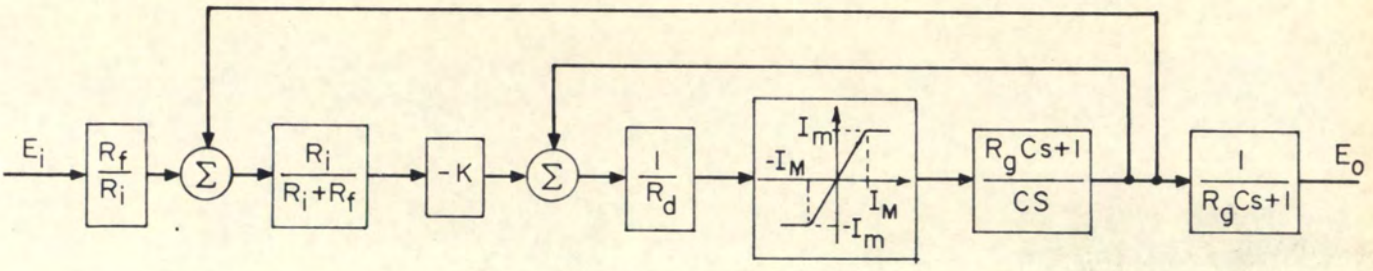

Fig. 5-5 Block Diagram of Feedback Amplifier with Storage Gate Load and Non-Linear Current Driver

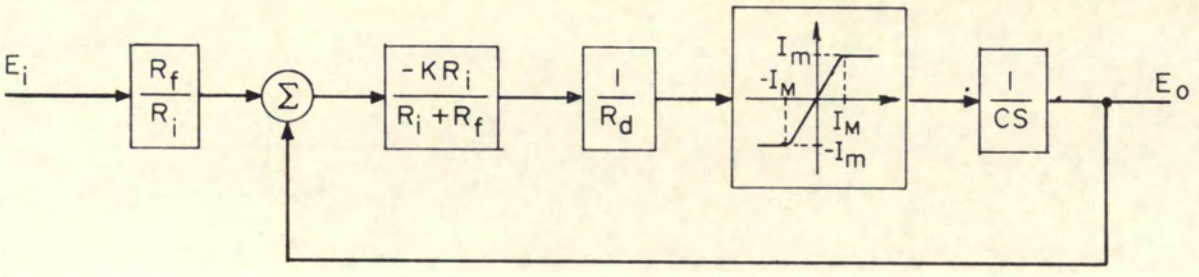

Fig. 5-6 Block Diagram Used to Explain Possibility of Low Frequency Oscillations

predicting this effect we will eliminate the oscillations.

CHAPTER VI

SEVERAL STORAGE GATES

6.1 INTRODUCTION

In this chapter we shall study several storage gates which were considered for possible pulsed analog use. These gates are very interesting and could be used as storage gates in many applications. However none of these gates are usable for pulsed analog purposes. The important properties of these gates will be summarized. The reasons why these gates can not be used in the pulsed analog system will be pointed out. All of the gates considered will be of the floating trigger type.

6.2 THE BILATERAL TRANSISTOR STORAGE GATE

The bilateral transistor storage gate will make a good first example. This gate, which is illustrated with a positive trigger and disabled with a negative trigger, is illustrated in Fig. 6-1. The basic operating characteristics of this gate can be illustrated using a fairly simple model for the transistor. The model chosen for the NPN transistor is shown in Fig. 6-2. The diodes have a forward conducting resistance of r_f and a reverse resistance of r_b. r_b is assumed to be much greater than r_f. This model and a perfectly matched PNP transistor can be incorporated into the series gating element. It should be noted that is non-symmetrical transistors were used in this gate the same model configuration, but with a numerical unbalance, could be used. The resulting enabled e_g vs i_g plot is illustrated in Fig. 6-3.

The enabled gate has many useful properties. The enabled resistance is made low and the linear range of the gate greatly extended by the active current generators of the transistor. After

the break point in the enabled characteristics the transistor becomes active. This fact keeps the conducting resistance of the gate low even after the break point. However these same active current generators also succeed in lowering the gates disabled resistance. As is the case with most gates which we attempt to use to meet our desired specifications it is this low back resistance or leakage current which is their most severe limitation. The diodes of the disabled gate are back biased at times by 40 volts or more.A transistor capable of this voltage range, with a back resistance high enough for pulsed analog uses is not available on the market at this time. Because of these limitations the transitor gate must be disqualified for pulsed analog applications.

6.3 THE FOUR-LAYER DIODE GATE

Included among the many novel semiconductor devices which have appeared in recent years is the Shockley four-layer diode. The d-c. characteristics of this device are illustrated in Fig. 6-4. The four-layer diode has two stable states. If the voltage exceeds V_B it goes into a low resistance state. It will remain in this low resistance state until the current drops below I_H, at which time it will return to a high resistance state. A gate which uses these diodes has been suggested by Nyder and Given. Fig. 6-5 illustrates this gate. A large positive trigger voltage will enable this gate by causing the diodes to conduct. A negative trigger voltage will attempt to reverse the current in the diodes and thereby return them to the high resistance state.

The enabled and disabled e_g vs i_g plots for the four layer diode gate are shown in Fig. 6-6. Note that the enabled characteristics contain a hysteresis effect. This characteristic of the

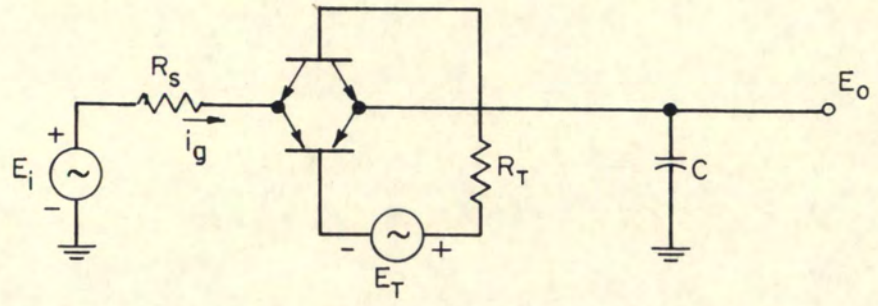

Fig. 6-1 The Bilateral Transistor Gate

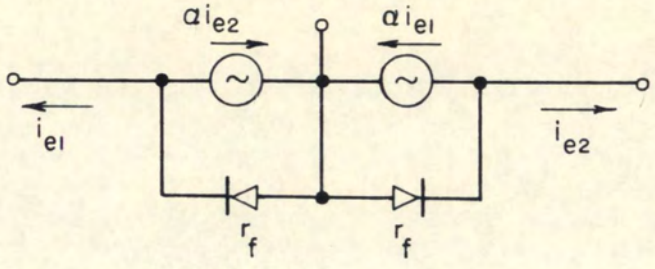

Fig. 6-2 NPN Bilateral Transistor Model

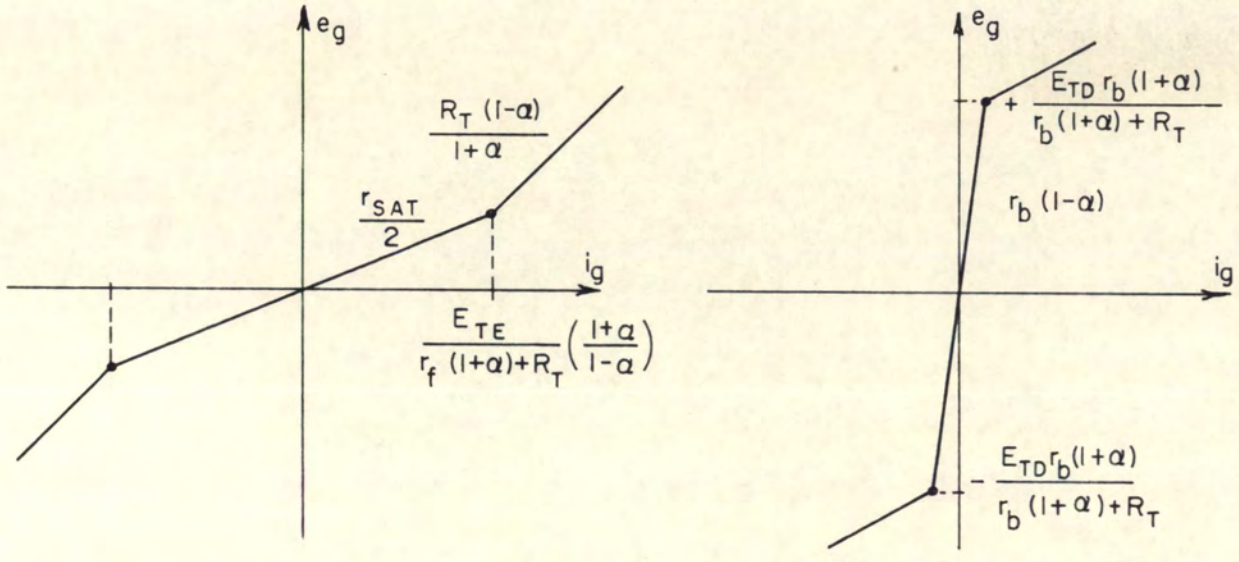

Fig. 6-3 Bilateral Transistor Series Element

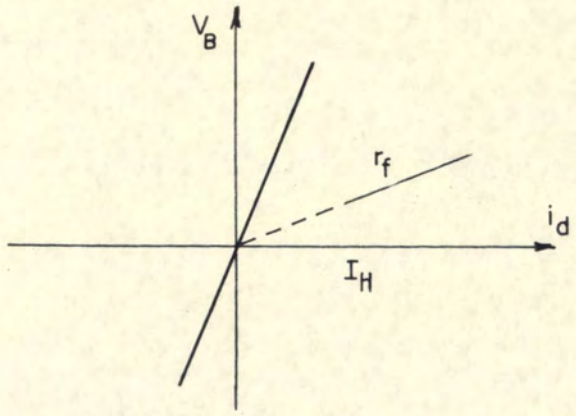

Fig. 6-4 4-Layer Diode d.c. Characteristics

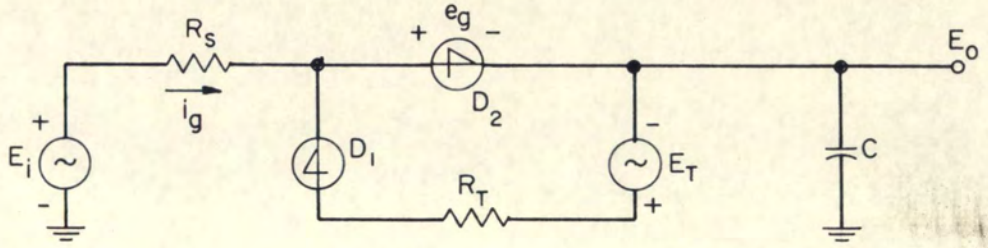

Fig. 6-5 A Four-Layer Diode Gate

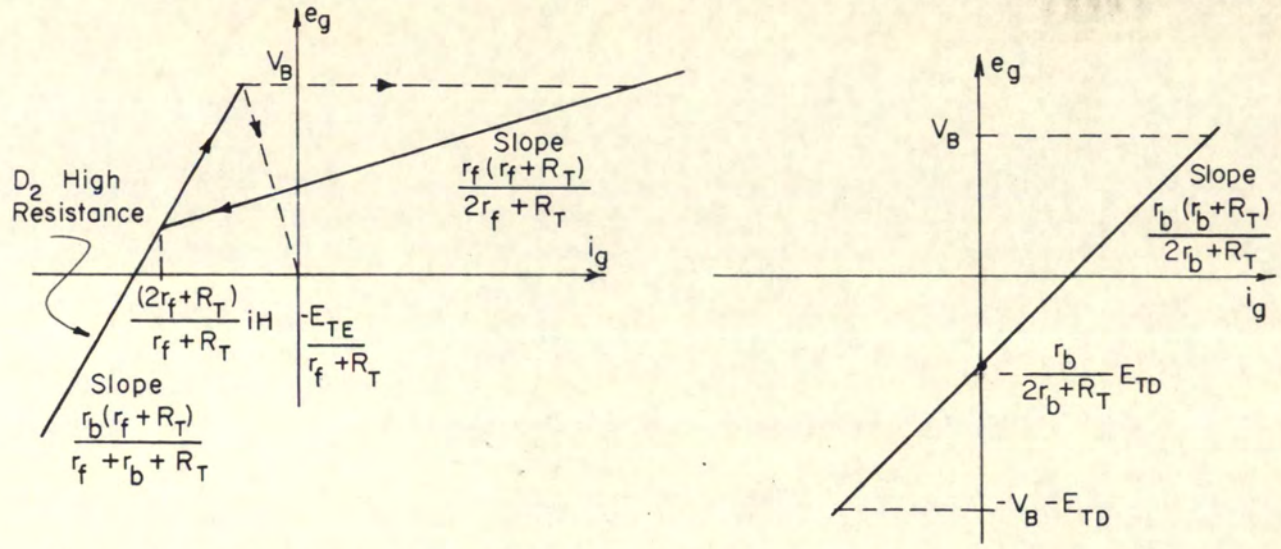

Fig. 6-6 Four-Layer Diode Gate's Characteristics

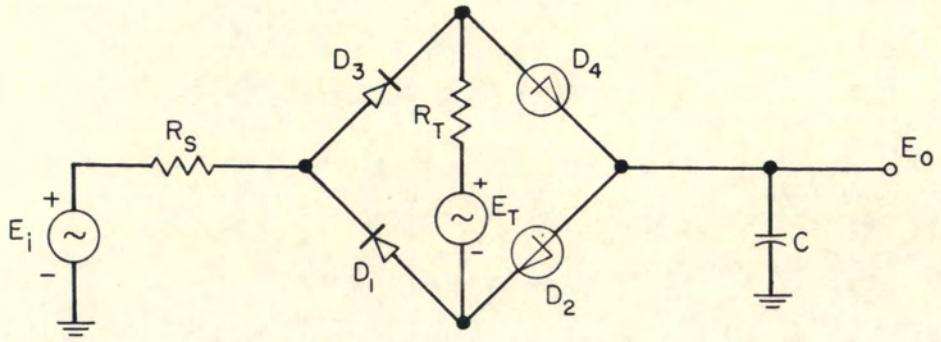

Fig. 6-7 The Connelly Gate

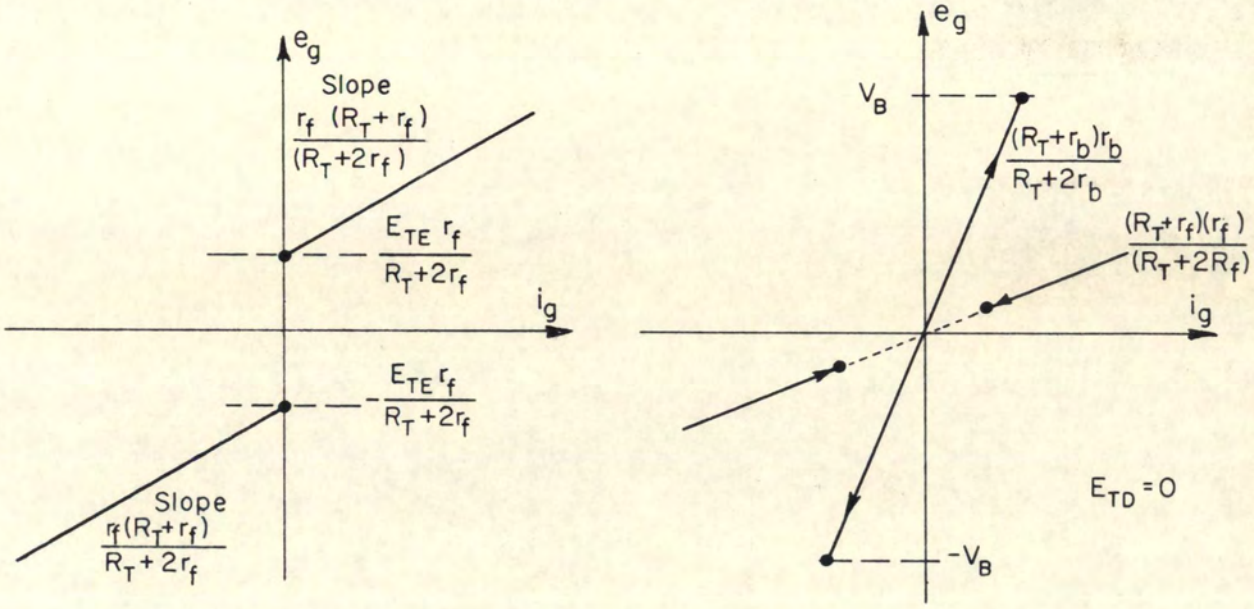

Fig. 6-8 The Connelly Gate's Characteristics

four layer diode gate is not only not very aesthetic it also results in rather awkward switching. If E_o is much greater than E_i at the beginning of the enabled period, or if the voltage across D2 does not become large enough to break down D2 at the beginning of the enabled period, the gate will operate on the high resistance portion of the characteristics. This will continue until the capacitor discharges sufficiently to allow D2 to break down. At this time the gate will become completely enabled. The disabled characteristics of this gate are much more straight forward. However if for some reason the disabled gate should break down a similar hysteresis effect will be exhibited. The literature on four-layer diodes claims that the resistance r_b can be as high as 1000×10^6 ohms. Therefore, by selecting these diodes carefully, resonable disabled characteristics for this gate can be obtained. It is, however, the peculiar enabled characteristics of this gate which make it unusable in our application.

6-4 THE CONNELLY GATE

Another gate which makes use of the four layer diode is the Connelly gate. This gate is illustrated in Fig. 6-7. During the enabled state both four layer diodes are in the conducting state due to the positive trigger voltage. A difference in E_i and E_o will then cause a current to flow in one ordinary diode or D3. There is no need to make E_T negative during the disabled periods since this voltage will simply be shorted by the two diodes D1 and D3. When E_T is made equal to zero the four layer diodes become high resistances and the gate is disabled.

To determine the highlights of the enabled series element, ideal

diodes can replace the diodes D1 and D3. The four layer diode whose characteristics are illustrated in Fig. 6-4 will be assumed to have an infinite non-conducting resistance. Using these models the enabled e_g vs i_g plot is shown in 6-8. Still using ideal diodes, but now taking into account the four layer diode back resistance r_b, the disabled characteristics can be plotted. A unique property of this series element is seen in the enabled e_g vs i_g plot. Its use in a storage gate will result in a non-linear storage gate. This is due to the fact that e_g is not single valued when $i_g = 0$. In this dead zone both diodes D1 and D3 are back biased. The magnitude of this dead zone is greater than $2I_H r_f$. In practice this can vary from a few millivolts to as high as 2 volts. While diodes can be selected to a maintain a small dead zone, it is very difficult to select these diodes for both small dead zone and large back resistance. The probability of finding the right combination is very small.

Each of these three gates investigated can be used as a storage gate. However with each of these gates extreme difficulty is found in attempting to meet the exact specifications which have been established for the pulsed analog storage gate.

CHAPTER VII

THE FOUR DIODE STORAGE GATE

7.1 INTRODUCTION

In this chapter we will become very practical and complete the design of a storage gate which can be used in the pulsed analog computer. The right combination on gate leakage current and input charging current will be obtained through the use of a four diode bridge gate and a White cathode follower input driver. The four diode bridge gate will be shown to have the lowest leakage current of any gate discussed. This low leakage current permits us to use a capacitor which requires a reasonable charging current. The design of the input source assures a low output resistance from the driver. This low output resistance helps solve the stability problem. A trigger source and a special output stage have also been built for use with this gate.

7.2 THE FOUR DIODE BRIDGE SERIES ELEMENT

The use of the four diode bridge as a series gating element has been discussed previously in Chapter II. The application of this element to the storage gate however requires a little special attention. Eqs. 3-21a and 3-21b can be used directly in determining the gates e_g vs i_g plot. These equations are repeated here for convenience. A commonly used diode function is the linear

$$E_T - iT\,R_T = f\left[\frac{i_T + i_g}{2}\right] + f\left[\frac{i_T - i_g}{2}\right] \qquad 3.21a$$

$$e_g = f\left[\frac{i_T + i_g}{2}\right] - f\left[\frac{i_T - i_g}{2}\right] \qquad 3.21b$$

resistive model, with a forward resistance r_f and a reverse resistance r_b Using this $f(i_d)$ in Eqs. 3-21 the e_g vs i_g plots of

Fig. 1-13 are obtained. Theseplots assume that r_b r_f and r_b R_T.

A more realistic model is needed for the diode before we can come to any conclusions about the four diode bridge gate. Either the exponential diode, which is a very good represenation, or perhaps an actual plot of the diodes characteristics could be used. Using an exponential diode and a current source

$$e_d = K_1 \ln \left[1 + \frac{i_d}{I_{co}} \right] \qquad 7.1$$

enabled trigger, we can come to a few important conclusions about this gate. Since the current source is a trigger source Eq. 3-21b will give us the gates characteristics directly. Making the appropriate substitutions we arrive at an equation for e_g as a function of i_g.

$$e_g = K_1 \ln \left[\frac{2 I_c + I_T + i_g}{2 I_c + I_T - i_g} \right] = K_1 \ln \left[\frac{I_T + i_g}{I_T - i_g} \right] \qquad 7.2$$

This equation shows that the maximum value of i_g is I_T. That is, the gate can conduct no more current than the trigger source delivers. A gate resistance r_g is defined by Eq. 7-3.

$$r_g = \left. \frac{\partial e_g}{\partial i_g} \right|_{i_g = 0} \qquad 7.3$$

For the gate described by Eq. 7-2 this calculates to be

$$r_g = \frac{2 K_1}{2 I_{co} + I_T} \cong \frac{2 K_1}{I_T} \qquad 7.4$$

It is very unlikely that a floating current source trigger would be built. However if R_T is 100 or more times greater than r_g the current source approximation will apply very well. It should be recalled that we do not need an extremely accurate plot of e_g vs

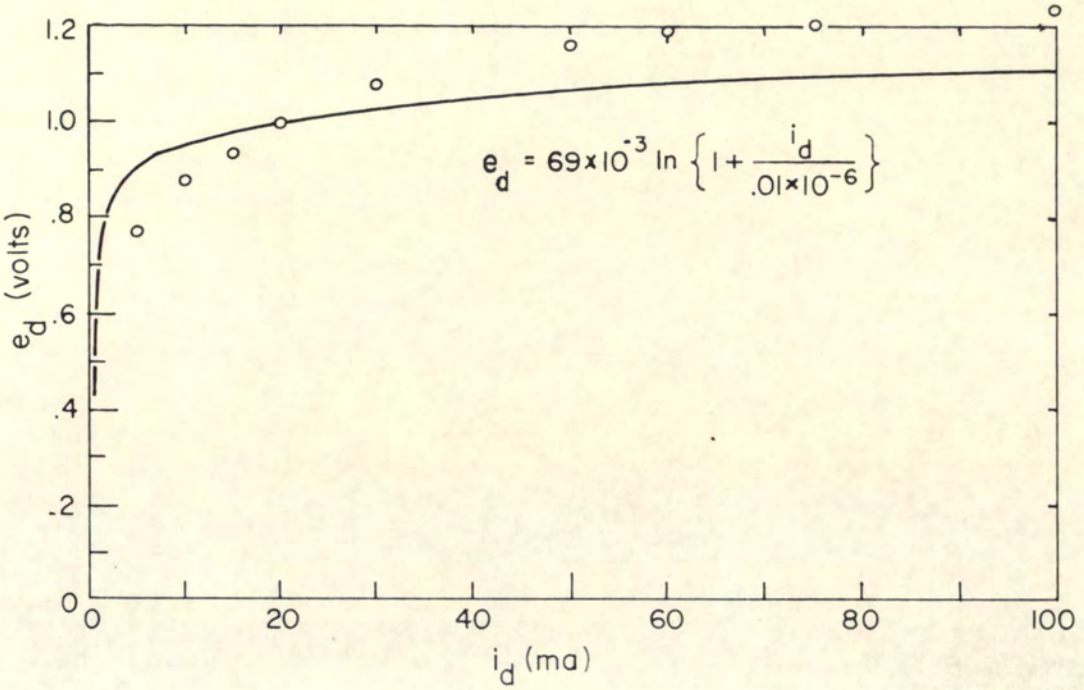

Fig. 7-1 A Silicon Diode's Forward Characteristics

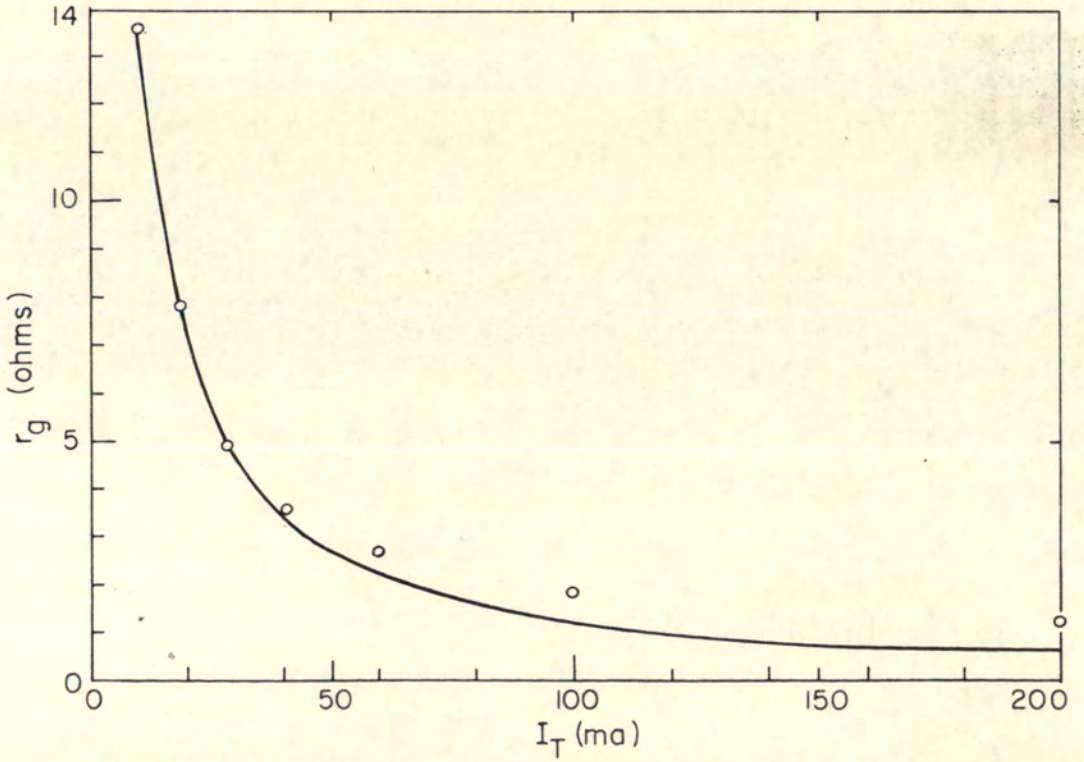

Fig. 7-2 Gate Resistance VS Trigger Current

i_g, but only need an estimate of the gates current conducting abilities. If any question arises, however, the graphical procedure of Appendix I can be used.

Fig. 7-1 illustrates a typical silicon diode forward characteristic. This real diode deviates from the exponential due to an additional resistive term in the diode function. Four similar diodes were used to build a gate and the gates resistance plotted (Fig. 7-2) for several values of trigger current. Pulsed techniques were used to make all measurements since the currents used exceeded the diodes d.c. limitaions. The value of K_1 used in calculating theoretical gate resistance was 69×10^{-3} volts.

The exponential model shows that the reverse characteristics of a diode are similar to a current source. Four current sources can be inserted in the four diode gate (Fig. 1-14). The resulting circuit is ambigous since four independnet current sources are arranged such that $I_1 + I_2 = I_3 + I_4$. Therefore in order to relieve this ambiguity a high resistance r_b has been added in parallel with each diode. If diodes are selected such that all leakage currents currents are equal the gate will have a disabled resistance of r_b. That is, a gate can be built which has a lower leakage current then the leakage current of any diode in the gate. Experience has shown that it is not practical to match diodes to more than a second significant figure. This however assures an improvement by a factor of 10 over the diode itself. The resistive component of back biased Transitron SG222 may run as high as 4×10^9 ohms. While diodes cannot be matched exactly they can be arranged in the gate to give a minimum gate leakage current. The diodes can be first

matched in pairs, with D2 and D4 forming one pair and D1 and D3 the other pair. If D4 has a larger leakage current than D2 this pair will tend to cause a positive gate current i_g. If D3 has a larger leakage current than D1 this pair will tend to cause a negative gate current. These positive and negative gate currents will cancel causing an even further reduction in gate current. In summary then in order to construct a gate with a resistance comparable to the back resistance of the diodes an attempt should be made to eliminate the effect of the current source by satisfying the equations $I_1 + I_2 = I_3 + I_4$.

This technique is illustrated in Fig. 7-3 and Fig. 7-4. Fig. 7-3 illustrates the reverse characteristics of four selected Transitron SG222 diodes. For the data plotted in Fig. 7-4 these diodes have been arranged to give a minimum leakage current. When $e_g = 0$ each diode is back-biased by 20 Volts. Therefore the current in each diode is about 15×10^{-9} amps.

It should be pointed out that the diodes used in this example were very carefully selected. They were selected first for low leakage current and high back resistance. Secondly they were carefully matched to construct the best possible gate. A very small percentage of SG222 diodes could be used in this gate. If diodes are selected such that leakage current is less than $.05 \times 10^{-6}$ amps and the back resistance is greater than 20000×10^{-6}r, about 20% of the SG222 diodes will be usable. This will, however, require at least a $.02 \times 10^{-6}$ farad capacitor. The charging of this capacitor cannot be accomplished by any circiut designed in this thesis. An operational amplifier which can be used for charging this capacitor is the subject of another thesis sponsored by this project[16].

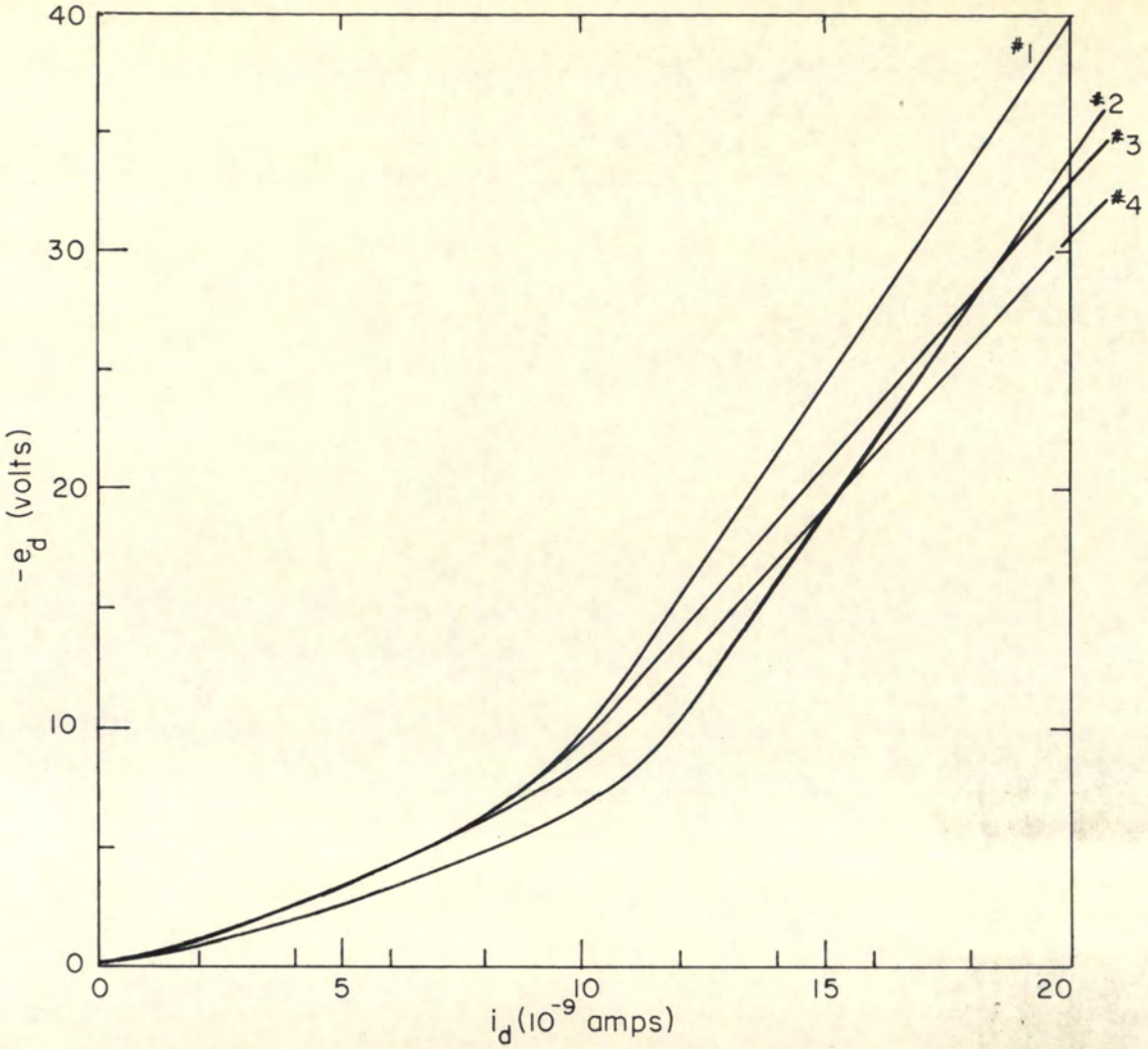

Fig. 7-3 Selected SG222 Reverse Characteristics

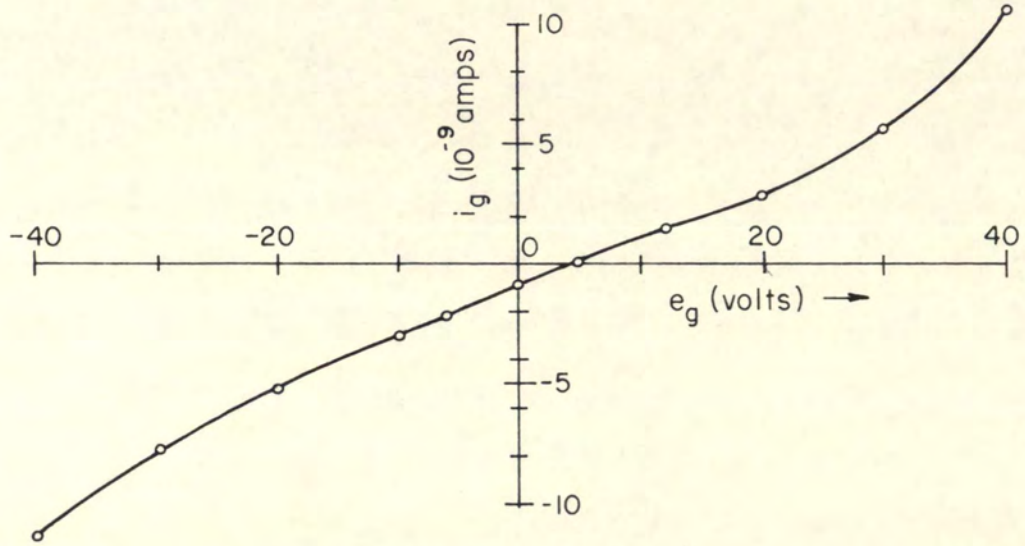

Fig. 7-4 Disabled Gate's Characteristics

A switching transient and the resulting error are anaviodable in the four-diode storage gate. This is due to the unbalance in the diodes switching characteristics. At the end of all gating periods, however, the gate will always be in exactly the same condition regardless of the present value of E_i. Therefore the switching transient will not be dependent of E_i but will be the same for all values of input. This fact will allow us to use a bias voltage to compensate for gate switching error.

The leakage current of the silicon diodes used in this gate are sensitive to temperature.[13] Eq. 7-4 describes this sensitivity. I_{co} is the leakage

$$I_{co} = I_o e^{b (T_j - T_o)} \qquad 7.4$$

current at the junction temp T_j. I_o is the leakage current at a reference temperature T_o. b is a constant and a property of the diode construction. Two problems arise due to this variation of leakage current with temperature. One is obvious. If the room temperature rises the leakage current of the gate will increase. The only solution to this problem is to use diodes which are insensitive to temperature or to keep the room cool. The other harmful effect of temperature variation is less obvious. When the gate is conducting heavily two diodes are conducting full current and two diodes are non-conducting. Under this pulsed load the two conducting diodes will heat up. When the gate returns to its disabled state the two heated diodes will gave a larger leakage current then previously. This unbalance will cause gate leakage current. However numerical calculation of this effect show that it can be neglected.[13]

Care should also be taken in selecting the dielectric of the

capacitor to be used in the storage gate. In general it is not dielectric leakage current which is important, but it is a phenomena called dielectric absorption.[14] This property of the capacitor dielectric results in an equivalent circuit as shown in Fig. 7-5. When a pulse of current is applied to the capacitor, C_o will charge immediately. C_1 will not charge immediately because of the resistance R_1. When the current pulse is removed e_c will change value due to the charging of C_1. After a 40×10^{-3} amp current pulse has been applied to a $.01 \times 10^{-6}$ farad paper capacitor for 10×10^{-6} second a voltage drop as high as 2 volts can be observed. This effect is greatly reduced by using a mica capacitor. However, no numerical calculation or experimental measurements have been made to justify neglecting this phenomena.

7.3 WHITE CATHODE FOLLOWER

A vacuum tube circuit which is capable of about $\pm$ 150 ma output currents and which has a very low incremental output impedance has been designed for use with the four diode bridge gate. This circuit which has a non-linear plate load resistance is illustrated in Fig. 7-6. The combination of the zener diode D1 is and resistance R_L form the non-linear plate load. The other zener diode D2 is used to couple the plate of T1 with the grid of T2. A complete piecewise linear analysis of this circuit is included in Appendix II. The important results can be easily summarized. The circuit is capable of a positive output current of $\frac{E_b - E_z}{r_p}$. The negative output current can be as high as $\frac{E_c}{r_p}$. Both of these currents are maximum currents outputs calculated without driving any grid positive. The incremental output resistance near the point where $i_g = 0$

is given in Eq. 7-5.

$$r_d = \frac{r_p^2 + r_p R}{R(1 + \mu + \mu^2) + r_p(2 + \mu)} = \frac{r_p}{\mu^2} \qquad 7.5$$

The approvimation assumes $R \gg r_p$ and $\mu \gg 1$. There is a breakpoint in the output resistance for comparatively small positive values of output current. To prevent this breakpoint from interfering with the systems stability it has been shifted by applying a current bias to the output. The experimental output characteristics of the unbiased White cathode follower are shown in Fig. 7-7.

7-4 Blocking Oscillator

7.6

7.8

A blocking Oscillator was built for use with the four diode bridge gate. The circuit diagrams for this trigger source is shown in Fig. 7-8. The output pulse on the collector of T2 is a 75 Volt pulse with rise and fall times of about .2 μ seconds. This output stage can deliver up to 800ma of current through the enabled gate. A very limited pulse width adjustment is provided for this circuit. The pulse width can be varied from 5 to 9 μ seconds. The real disadvantage of this blocking oscillator is it limited pulse repetition rate. The resistor and diode in parallel with the windings of each transformer are used to prevent inductive overshoot. By allowing this overshoot to increase the pulse repetition rate can also be increased. By decreasing the output current of the output transformer the pulse repetition rate can also be increased.

7-5 Output Buffer

The output buffer for the storage gate must drain very little current from the storage capacitor. A special purpose tube Raytheon

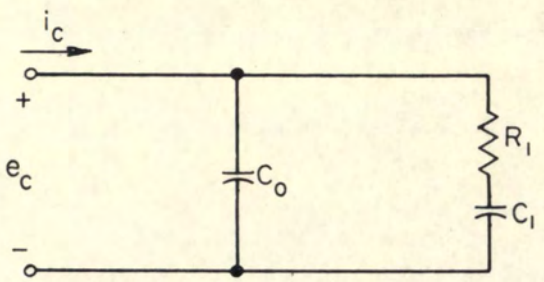

Fig. 7-5 A Real Capacitor

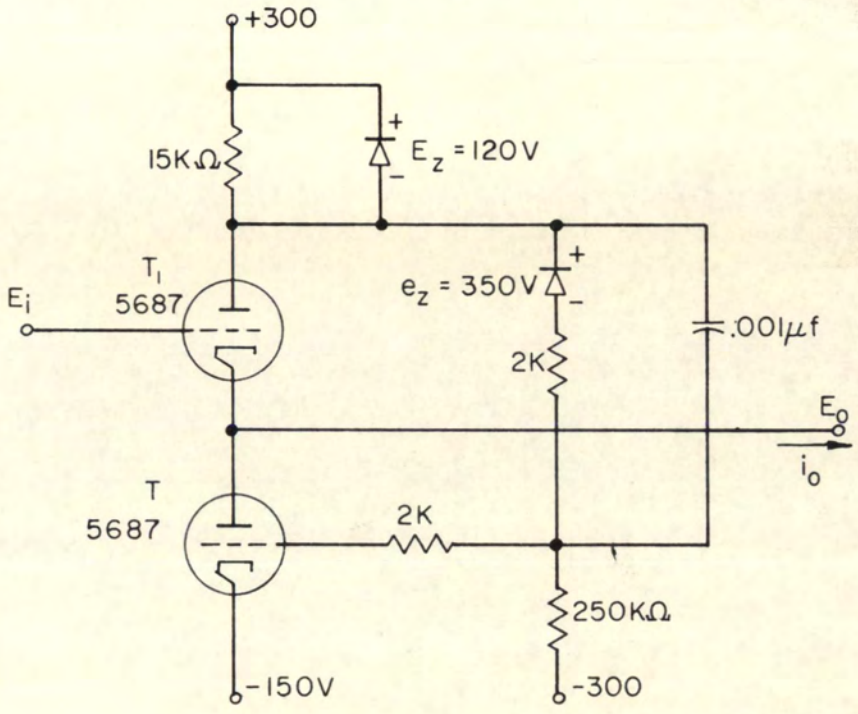

Fig. 7-6 White Cathode Follower with Non-Linear Plate Resistance

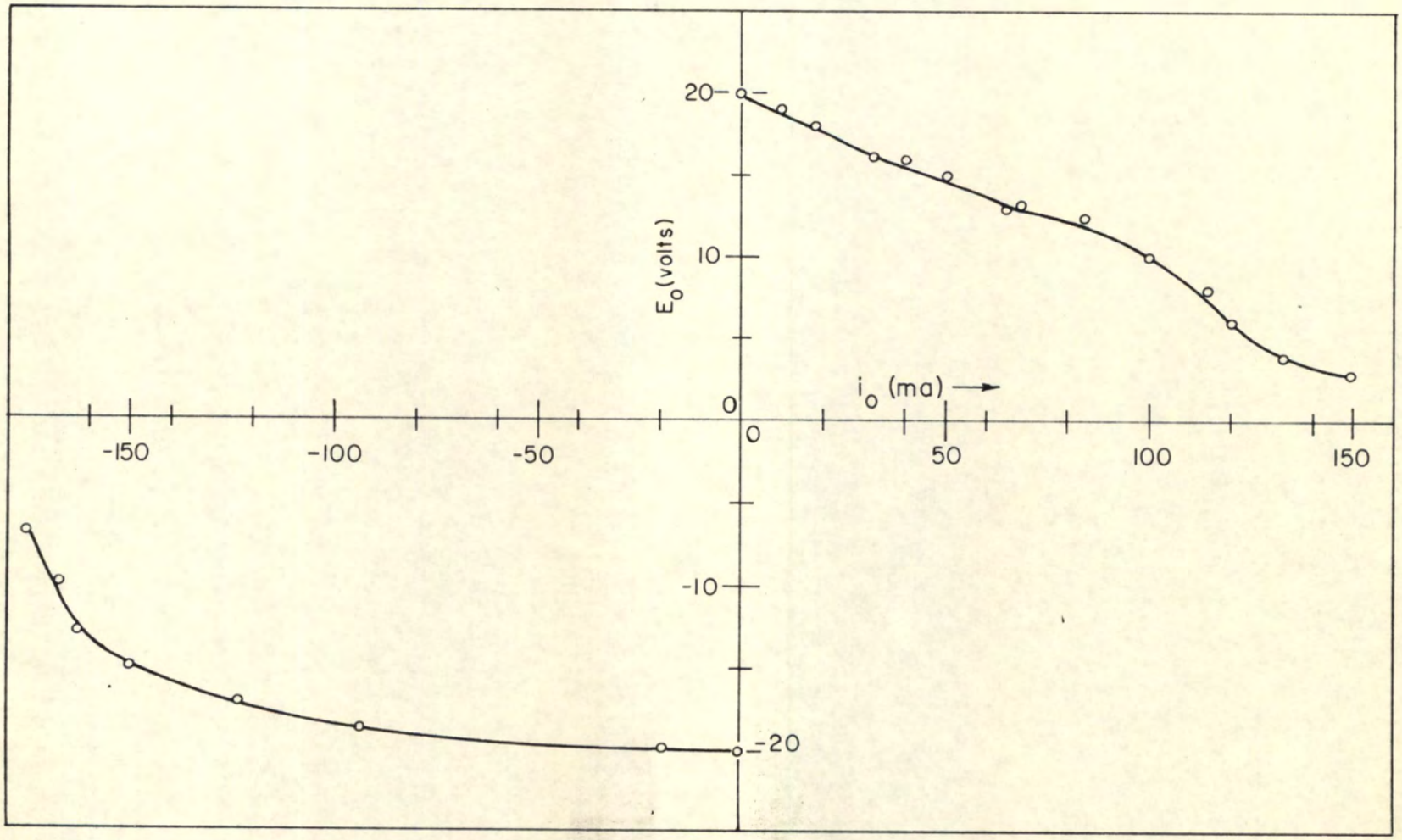

Fig. 7-7 White Cathode Follower's Output Characteristics

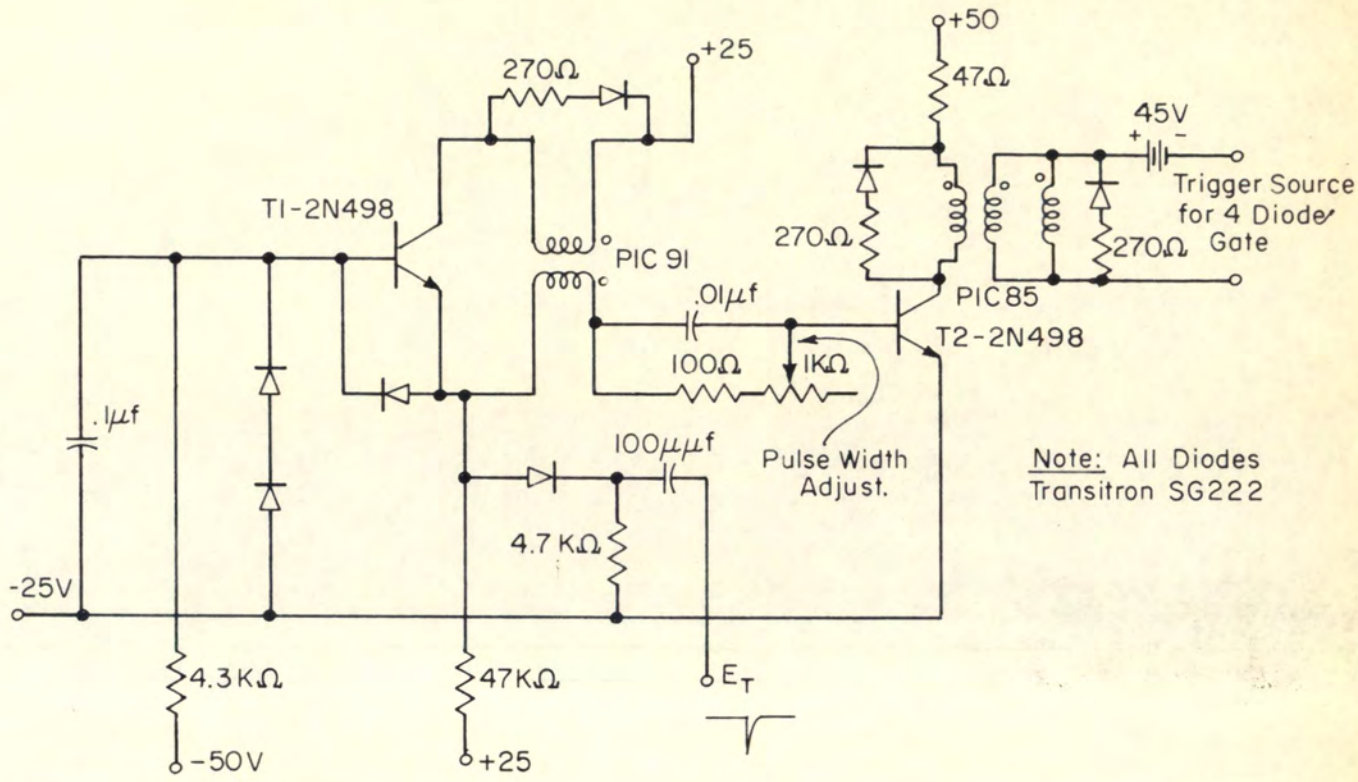

Fig. 7-8 Transistor Blocking Oscillator

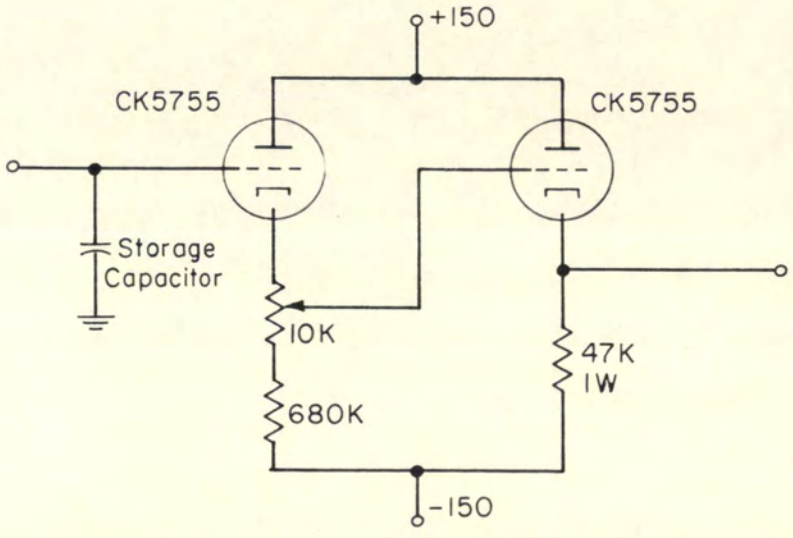

Fig. 7-9 Output Buffer

CK5755 is especially designed to keep grid leakage current at about 10^{-9}amps. This current is less than the current through the gate. This tube is used as a cathode follower in the output buffer. The cathode resistor of the cathode follower must be kept high (about 1 meg) in order to take advantage of the tubes special properties. This high resistnace in the cathode follower prevents the circuit from being loaded down. Another cathode follower follows this first cathode follower in order to make the output of this stage more usable. A bias adjustment is also provided in the circuit.

APPENDIX I

The e_g vs i_g plot for the four diode bridge gate can be obtained by a graphical procedure [6]. Eqs. 3-21a and 3-21b from which this procedure is derived are repeated here for convenience.

$$E_T - i_T R_T = f\left[\frac{i_T - i_g}{2}\right] + f\left[\frac{i_T + i_g}{2}\right] \qquad 3.21a$$

$$e_g = f\left[\frac{i_T + i_g}{2}\right] - f\left[\frac{i_T - i_g}{2}\right] \qquad 3.21b$$

The steps below are followed to determine a single point on the e_g vs i_g plot.

1) plot $f\left[\frac{i_T + i_g}{2}\right]$ vs i_g for an arbitrary i_T
2) plot $f\left[\frac{i_T - i_g}{2}\right]$ vs i_g
3) add 1) and 2)
4) plot $E_T - i_T R_T$ (include here trigger source non linearities)
5) insersection of 3) and 4) are possible operating points.
6) compute e_g by subtracting 1) and 2)
7) plot e_g vs i_g (one point, with i_T as a parameter)
8) try again for another i_T (ie. go back to 1)

If in following this procedure 3) and 4) don't intersect, the value which was arbitrarily chosen for i_T can never occur. While this procedure may seem rather time consuming at first glance, a good estimate of e_g vs i_g can actually be obtained rather quickly in practice. If i_T is a current source only the subtraction of Eq. 3-21b need be performed.

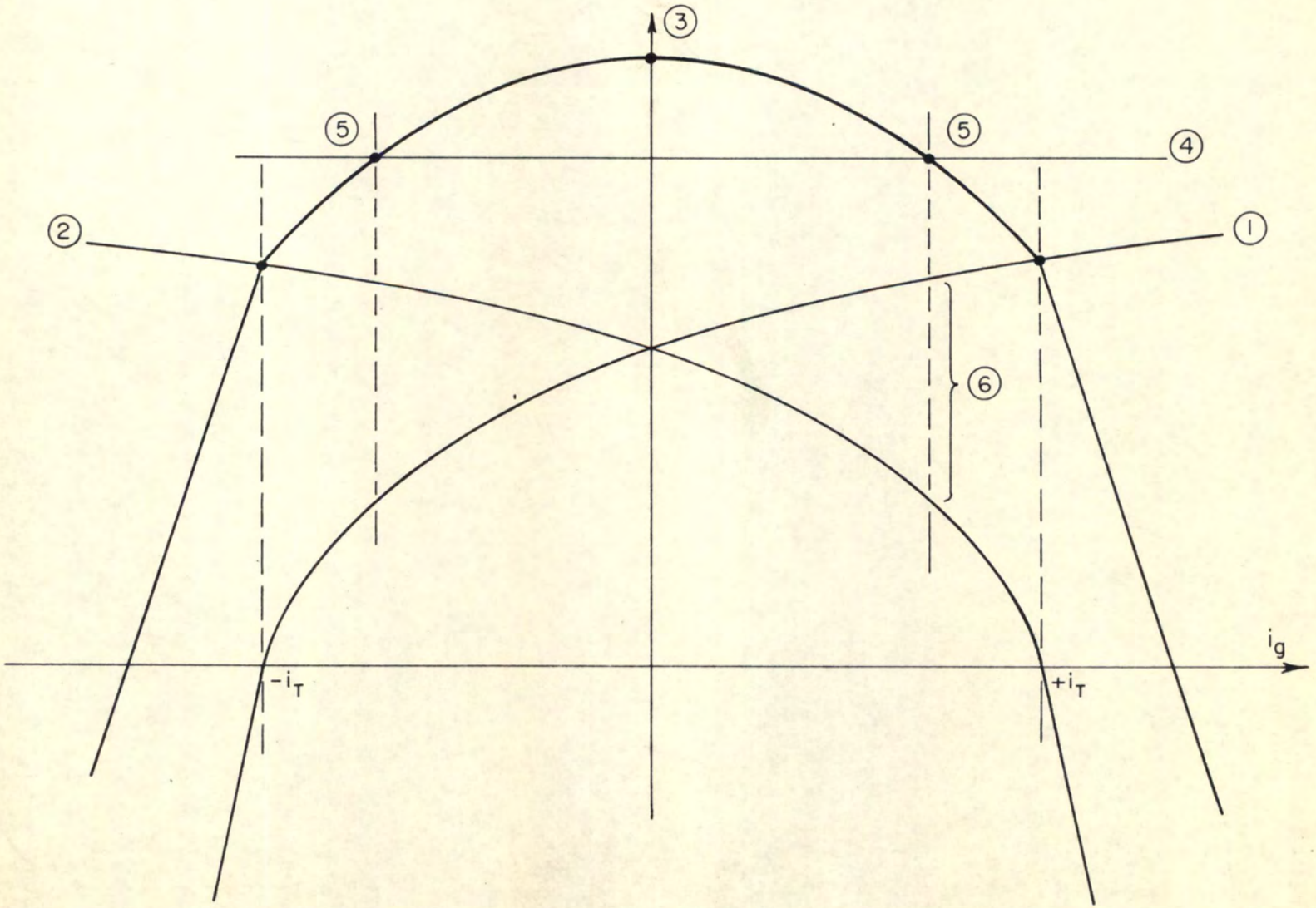

Fig. A1-1 Graphical Construction Used to Find e_g vs. i_g Plot for Four-Diode Bridge

APPENDIX II

The piecewise linear analysis of the White Cathode Follower is outlined below. It is always assumed that the current through D_2 is a small percentage of the current through T_1. This approximation allows us to neglect the bias resistor which goes from the grid of T_2 to the -300 Volt supply.

Equations for Both tube in linear range and D_1 non conducting.

$$e_{b1} = i_{b1} r_p - \mu e_{c1}$$

$$e_{b2} = i_{b2} r_p - \mu e_{c2}$$

$$E_b = i_{b1} R + e_{b1} + e_{b2} - E_c$$

$$E_b = i_{b1} R + e_z + e_{c2} - E_c$$

$$E_{in} = e_{c1} + e_{b2} - E_c$$

$$i_{b2} + i_o = i_{b1}$$

given E_{in}, i_o find e_{b2}, e_{b2}, i_{b2}, i_{b2}, e_{c1}, e_{c2}

$$\begin{bmatrix} 0 \\ 0 \\ E_b + E_c \\ E_b + E_c - e_z \\ E_{in} + E_c \\ i_o \end{bmatrix} = \begin{bmatrix} r_p & 0 & -1 & 0 & -\mu & 0 \\ 0 & r_p & 0 & -1 & 0 & -\mu \\ R & 0 & 1 & 1 & 0 & 0 \\ R & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 1 & 1 & 0 \\ 1 & -1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{b1} \\ i_{b2} \\ e_{b1} \\ e_{b2} \\ e_{c1} \\ e_{c2} \end{bmatrix}$$

Listed below are the total equations for the White Cathode follower's currents and voltages

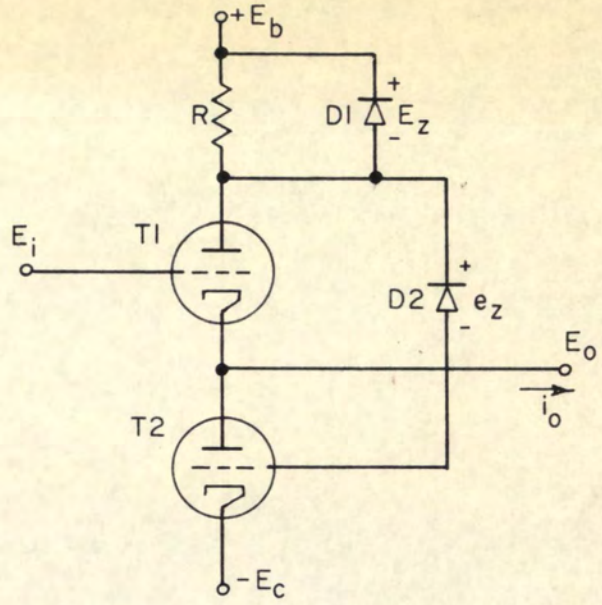

Fig. A2-1 The White Cathode Follower

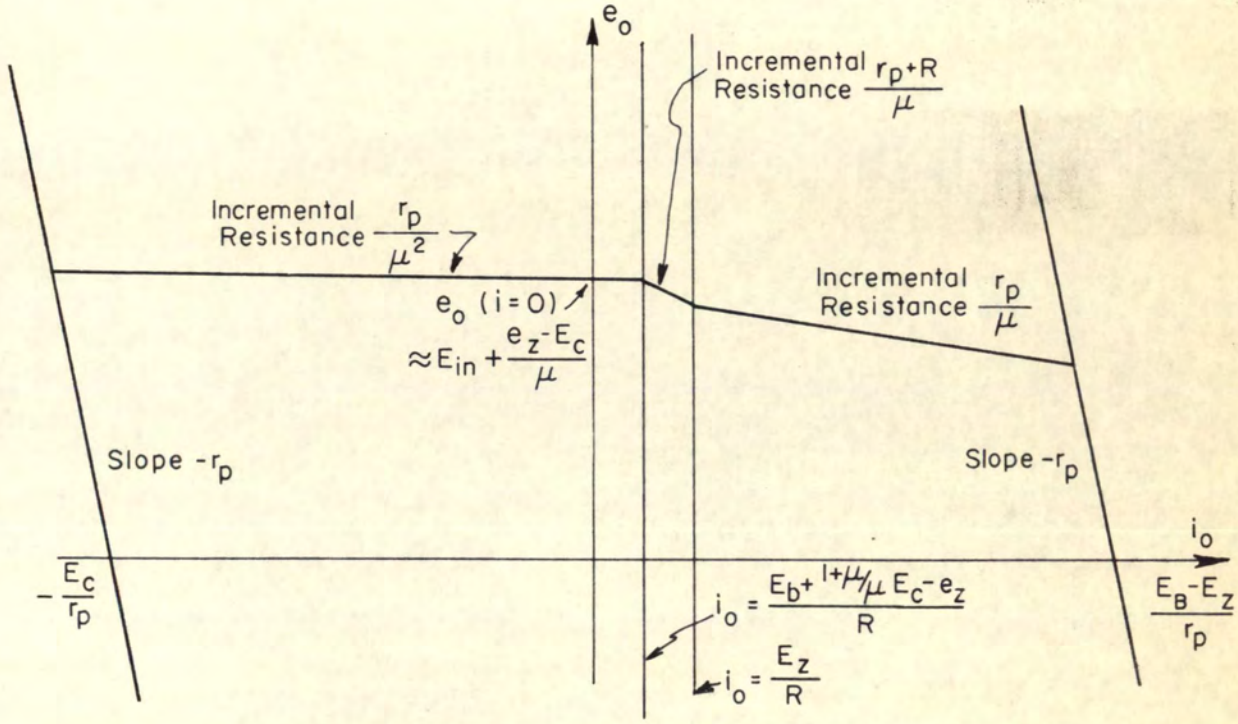

Fig. A2-2 White Cathode Follower's Theoretical Output Characteristics

$$D = R\left[1 + \mu + \mu^2\right] + r_p\left[2 + \mu\right]$$

$$Di_{b1} = D_1 = i_o\left[(1 + \mu)r_p\right] + \mu E_{in} + \left[1 + \mu + \mu^2\right]E_b + \left[1 + 2\mu + \mu^2\right]E_c + \left[-\mu-\mu^2\right]e_z$$

$$Di_{b2} = D_2 = \left[-r_p - (1 + \mu + \mu^2)R\right]i_o + \mu E_{in} + \left[1 + \mu + \mu^2\right]E_b + \left[1 + 2\mu + \mu^2\right]E_c + \left[-\mu-\mu^2\right]e_z$$

$$De_{b1} = D_3 = \left[r_p^2 - \mu r_p R\right]i_o + \left[-\mu r_p - \mu R - \mu^2 R\right]E_{in} + \left[r_p + 2\mu r_p\right]E_b + \left[r_p + \mu r_p - \mu R - \mu^2 R\right]E_c + \left[-\mu r_p + \mu^2 R\right]e_z$$

$$De_{b2} = D_4 = \left[-r_p^2 - r_p R\right]i_o + \left[\mu^2 R + \mu r_p\right]E_{in} + \left[r_p - \mu r_p\right]E_b + \left[r_p + \mu^2 R\right]E_c + \left[\mu R + \mu r_p\right]e_z$$

$$De_{c1} = D_5 = \left[r_p^2 + r_p R\right]i_o + \left[2r_p + R + \mu R\right]E_{in} + \left[-r_p + \mu r_p\right]E_b + \left[R + \mu R + r_p + \mu r_p\right]E_c + \left[-\mu r_p - \mu R\right]e_z$$

$$De_{c2} = D_6 = \left[-r_p R - \mu r_p R\right]i_o - \mu R E_{in} + \left[2r_p + \mu r_p\right]E_b + \left[2r_p + \mu r_p - \mu R\right]E_c + \left[-R - \mu r_p - 2r_p\right]e_z$$

When T_2 cuts off the following equations apply $i_{b2} = 0$

$$i_o = \frac{\mu}{D_1}E_{in} + \left[\frac{1 + \mu + \mu^2}{D^1}\right]E_b + \left[\frac{1 + 2\mu + \mu^2}{D^1}\right]E_o - \left[\frac{\mu + \mu^2}{D^1}\right]ez$$

$$e_o = \frac{\mu^2 R}{D^1}E_{in} - \frac{\mu r_p}{D^1}E_b - \frac{\left[r_p + R\right]\left[1 + \mu\right]}{D^1}E_c + \frac{\mu\left[r_p + R\right]}{D^1}e_z$$

$$D^1 = r_p + (1 + \mu + \mu^2)R$$

Eliminating E_{in}

$$\mu R i_o - e_o = \mu E_b + (1 + \mu)E_c - \mu e_z$$

The equation with T_2 cut off is then

$$e_o = \frac{E_b}{1+\mu} - i_o \frac{(R + r_p)}{1+\mu} + \frac{\mu}{1+\mu} E_{in}$$

The equation below applies only at the point of cutoff.

$$e_o = \frac{\mu^2 R}{D^1} E_{in} - \frac{\mu_p}{D^1} E_b - \left[\frac{r_p + R}{D^1}\right]\left[\frac{1+\mu}{}\right] E_c + \frac{\mu\left[r_p + R\right]}{D^1} e_z$$

The next break point will occur when D_1 begins to conduct at

$$i_o = \frac{E_z}{R}$$

$$e_o = - \frac{(r_p + R)E_z}{(1+\mu)R} + \frac{E_b}{1+\mu} + \frac{\mu}{1+\mu} E_{in}$$

$i_o > \frac{Ez}{R}$

$$e_o = - \frac{r_p}{1+\mu} i_o + \frac{(E_b - E_z)}{1+\mu} + \frac{\mu}{1+\mu} E_{in}$$

$$e_{c_1} = \frac{r_p}{1+\mu} i_o + \frac{E_{in}}{1+\mu} - \frac{E_b - E_z}{1+\mu}$$

These equations are good until e_{c1} goes positive

$$\text{at } e_c = 0 \qquad i_o = \frac{E_b - E_z - E_{in}}{r_p}$$

$$e_o = E_{in}$$

A break point will occur for negative i_o when the grid of T_2 goes positive. $e_{c1} = 0$

$$i_o = \frac{-\mu R}{r_p R + \mu r_p R} E_{in} + \frac{2r_p + \mu r_p}{r_p R + \mu r_p R} E_b$$

$$\frac{2\, r_p + \mu r_p - \mu R}{r_p R + \mu r_p\, R} E_c - \frac{R + \mu r_p + 2r_p}{r_p R + \mu r_p R} e_z$$

$$De_{b2} = \frac{\mu}{1+\mu} D\, E_{in} - \frac{r_p}{R\ 1+\mu}\, ^D E_b$$

$$\frac{- r_p^2 (2 + \mu) + \mu R^2 (1 + \mu + \mu^2) + r_p R (\mu - 1)}{R (1 + \mu)} E_c$$

$$+ \frac{R^2 (1 + \mu + \mu^2) + r_p^2 (2 + \mu) + r_p R (\mu^2 + 2\mu + 3)}{R (1 + \mu)}$$

The results of these calculations are summarized in Fig. A-2.

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