PROJECT GRIND REPORT

ON

THE HIGH SPEED GATE CIRCUIT

Eugene Breiding
Robert Lindsay

6/30/53

PROJECT GRIND REPORT ON THE HIGH SPEED GATE

Circuit Parameters

Vacuum Tube: The circuit now under test uses a 7AK7 pentode as the gate tube. Life tests made by MIT on the 7AK7's in WW-1 indicate that the tube has long life characteristics and is therefore a suitable choice. However, characteristic curves and life data in the regions where the tube is to be operated for WW-2 applications is not yet available. Preparations are now being made by Dave Crawford's group at IBM to run 7AK7 characteristic curves in the positive regions, but no data has yet been obtained.

Pulse Transformers: Input and output transformers are being used in the bench test units, although the circuitcan be operated without an input transformer when driven by the secondary of the output transformer of the driving stage.

The input transformer is the standard MIT 1:1 transformer. The effect of this transformer upon input pulse amplitude is shown by the curve on page 5 . It should be noted that the transformer increases pulse width due to the relatively high leakage inductance. Shunt inductive compensation can be used to reduce pulse width, but this also reduces available amplitude. Low leakage transformers are being constructed, and these units will be used for the final tests.

The output transformer is a special 7:1 transformer with tight coupling between windings. Tests have been made on transformers with ratios of 1:1, 3:1, 5:1, 6:1, 7:1, and 8:1, and these tests have indicated that the 7:1 ratio is the most suitable choice. The load line with this ratio for a 93 ohm load is kept below the knee of the Ep-Ip curve to obtain less variation of output voltage with load changes. Gain curves for the 5:1, 6:1, and 7:1 ratios are shown on pages 6,7 and 8 .

Transformer Termination: The output transformer termination has been chosen to be 93 ohms because of the following reasons:

1. 93 ohm cables will be used in WW-2.
2. A 93 ohm termination does not require shunt primary diodes.
3. Load capacity may be very large before transformer loading is appreciably changed.
4. 93 ohm loading helps to hold line pick-up to a minimum.

Suppressor Grid Resistance: The effect of simulating a cathode follower resistance by placing a resistor in series with the suppressor grid is

shown in the curve on page 8 . It is seen that this resistance tends to flatten the top section of the gain curve. This is desirable in order to maintain a more constant output over the range of grid input amplitude.

Parasitic Suppressor Resistance: Verbal reports from Herb Platt of MIT indicates that the parasitic suppressor is instrumental in holding up output amplitude. No investigation has yet been made by IBM, but tests are being planned to determine the optimum value of this resistance.

Decoupling Networks: Optimum values of decoupling parameters have not been determined, although satisfactory results have been observed with 0.5 uf and 22 ohms in the -15 volt lines, 0.1 uf and 22 ohms in the +90 volt lines, and 0.01 uf and 220 ohms in the +250 volt lines. It is thought that these values are somewhere close to optimum values. Tests to be made will determine the minimum values.

Driving Voltages and Currents

Suppressor: The DC level is supplied to the suppressor which constitutes one input of the "plus AND" circuit. This level has been established at +10 or -30 volts. The +10 volts has been selected in order to obtain higher amplitude output. It also shows less deviation of output amplitude with respect to a change in the suppressor level as shown on curve # 9 . The input capacity of the suppressor grid without stray capacity is approximately 4uuf. The current requirements (during a pulse on the control grid) is approximately 50 ma peak. This grid cuts off at about -10 volts.

Control Grid: 0.1 microsecond pulses are supplied to this grid and these constitute the other input of the "plus AND" circuit. This pulse has been tentatively standardized at 20 to 40 volts in amplitude, 0.08 to 0.12 microseconds in width, a maximum of 0.4 microseconds recovery time, and maximum of 5 volts positive overshoot. This pulse basically is a half sine wave but may be flat on top. The input capacity is 12 uuf. The current required to drive this grid is approximately 50 ma peak with 24 ohms in series and is 20 ma peak with 470 ohms in series with the control grid.

Supply Voltages

Plate: The plate requires +250 volts with a maximum average current of approximately 15 ma.

Screen: The screen requires +90 volts with a maximum average current of

approximately 6 ma.

Bias: The bias is set at -15 volts.

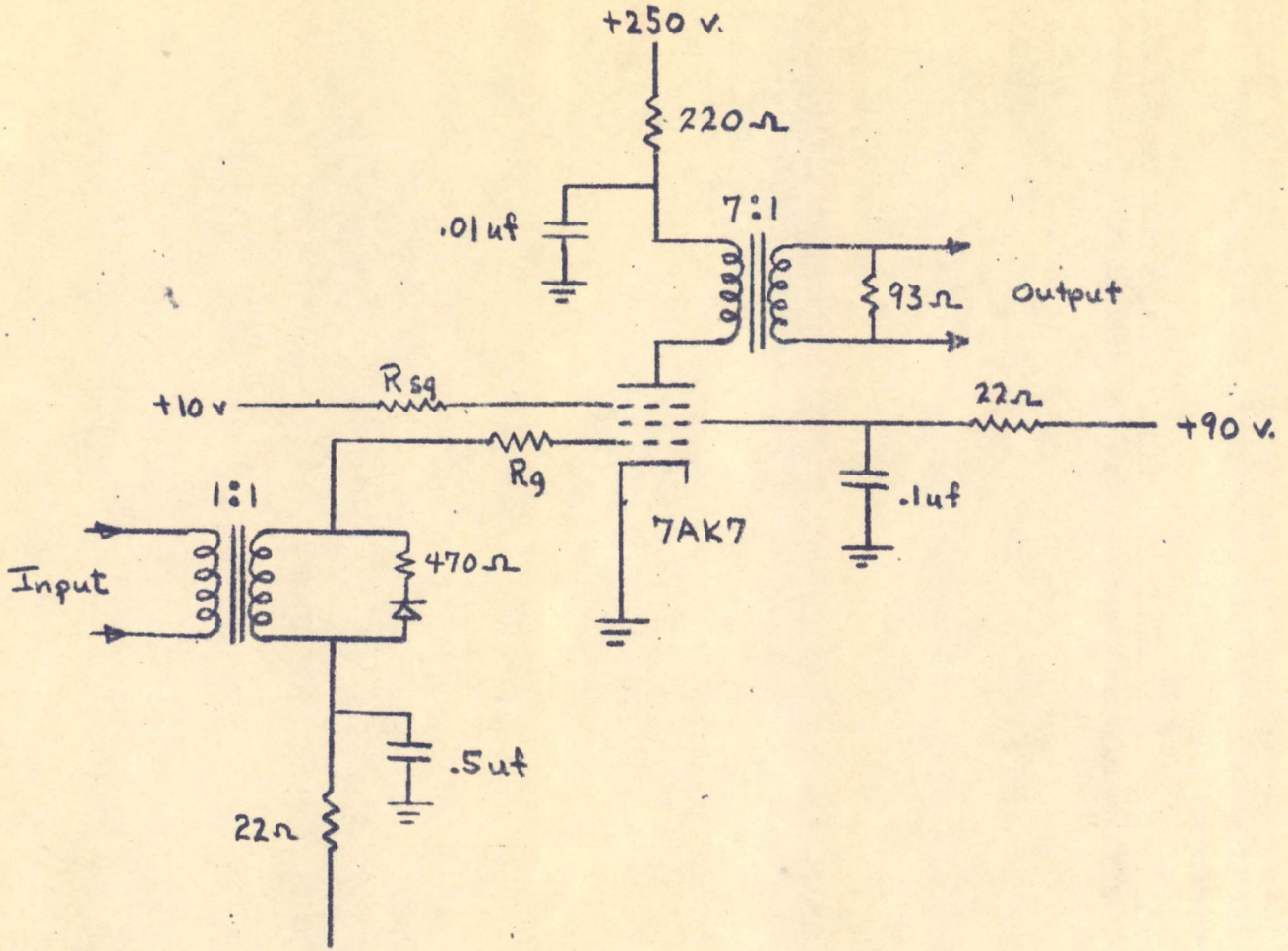
Marginal Checking

No marginal checks have been made to date, since it was felt that the circuit should be completed and in final form before this type of testing was attempted.

Work to be Done

A series of final tests have been set up to determine the performance of the final gate circuit under wide conditions of loading and driving applications. These tests will be started as soon as the bench test unit is completed and the required special transformers constructed to required specifications. These transformers are now on order and should be received within a week.

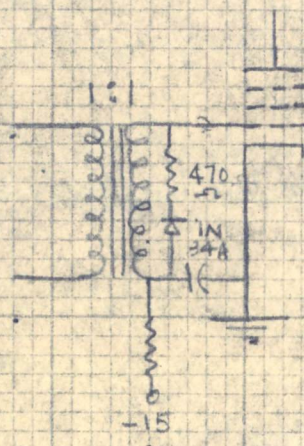
6-30-53



Gate Circuit Diagram

RLL
6/30/53

INPUT - OUTPUT CHARACTERISTICS OF A 1:1 TRANSFORMER IN THE CONTROL GRID CIRCUIT OF A GATE TUBE



E_{OUT} ~ VOLTS

40
30
20
10
0
10
20
30

UNITY GAIN

WITH 33μh CHOKE ACROSS SECONDARY FOR PULSE SHAPING

EJB 6/10/63

5

E_{IN} ~ VOLTS

TRANSFORMERS ON TEST

GT-10

5:1 TRANSFORMER, 40 to 8 TURNS on FERRAMIC H BODY F262 CORE.

GT-11

6:1 TRANSFORMER, 42 to 7 TURNS ON FERRAMIC H BODY F262 CORE.

GT-12

7:1 TRANSFORMER, 42 to 6 TURNS ON FERRAMIC H BODY F262 CORE.

GT-13

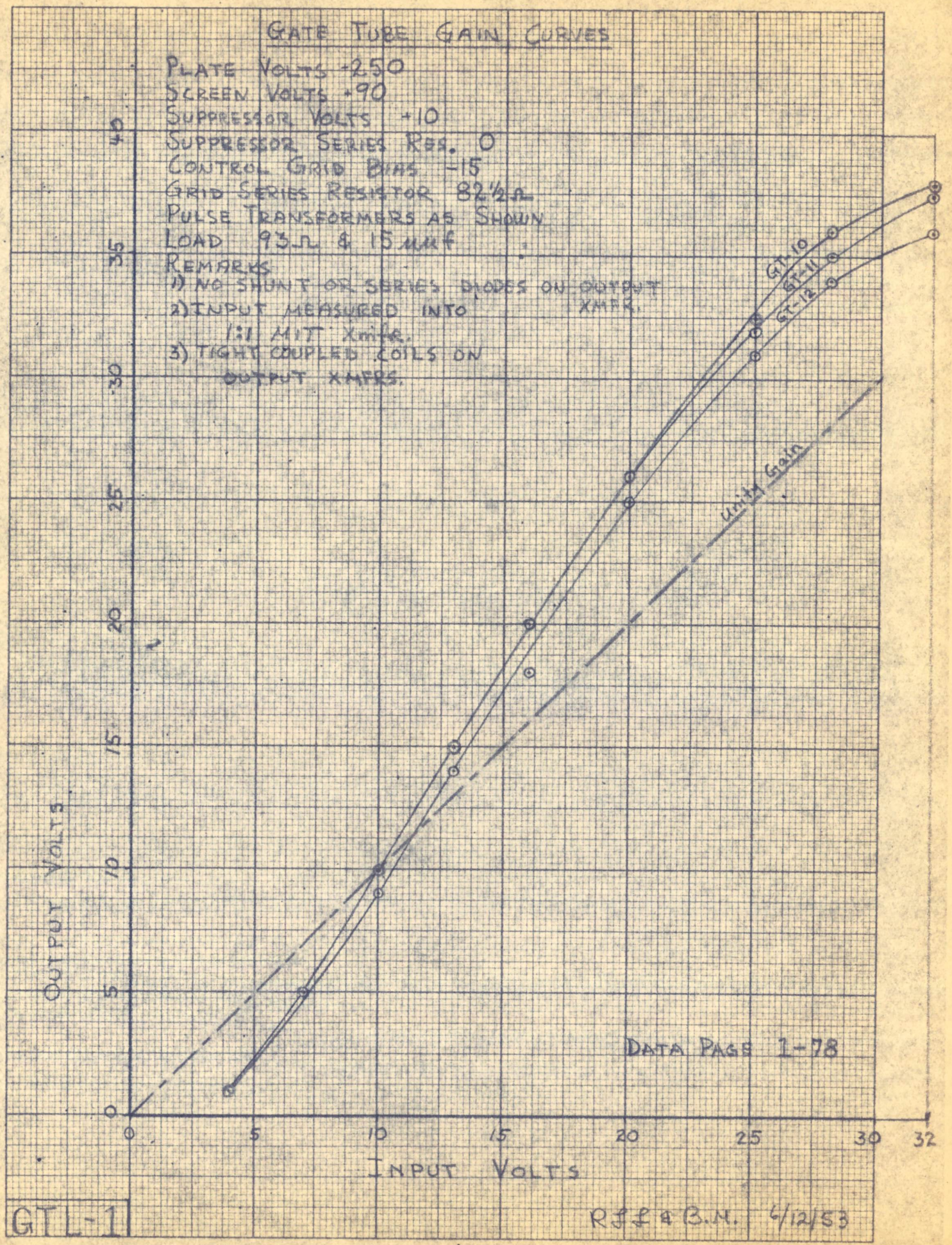
REPLACEMENT FOR GT-11. GT-11 DEVELOPED AN OPEN PRIMARY DURING TESTS.

R.L.L.
6/29/53

GATE TUBE GAIN CURVES

PLATE VOLTS +250
SCREEN VOLTS +90
SUPPRESSOR VOLTS +10
SUPPRESSOR SERIES RES. 0
CONTROL GRID BIAS -15
GRID SERIES RESISTOR 82½Ω
PULSE TRANSFORMERS AS SHOWN
LOAD 93Ω & 15 mmf

REMARKS
1) NO SHUNT OR SERIES DIODES ON OUTPUT XMFR.
2) INPUT MEASURED INTO 1:1 MIT Xmfr.
3) TIGHT COUPLED COILS ON OUTPUT XMFRS.



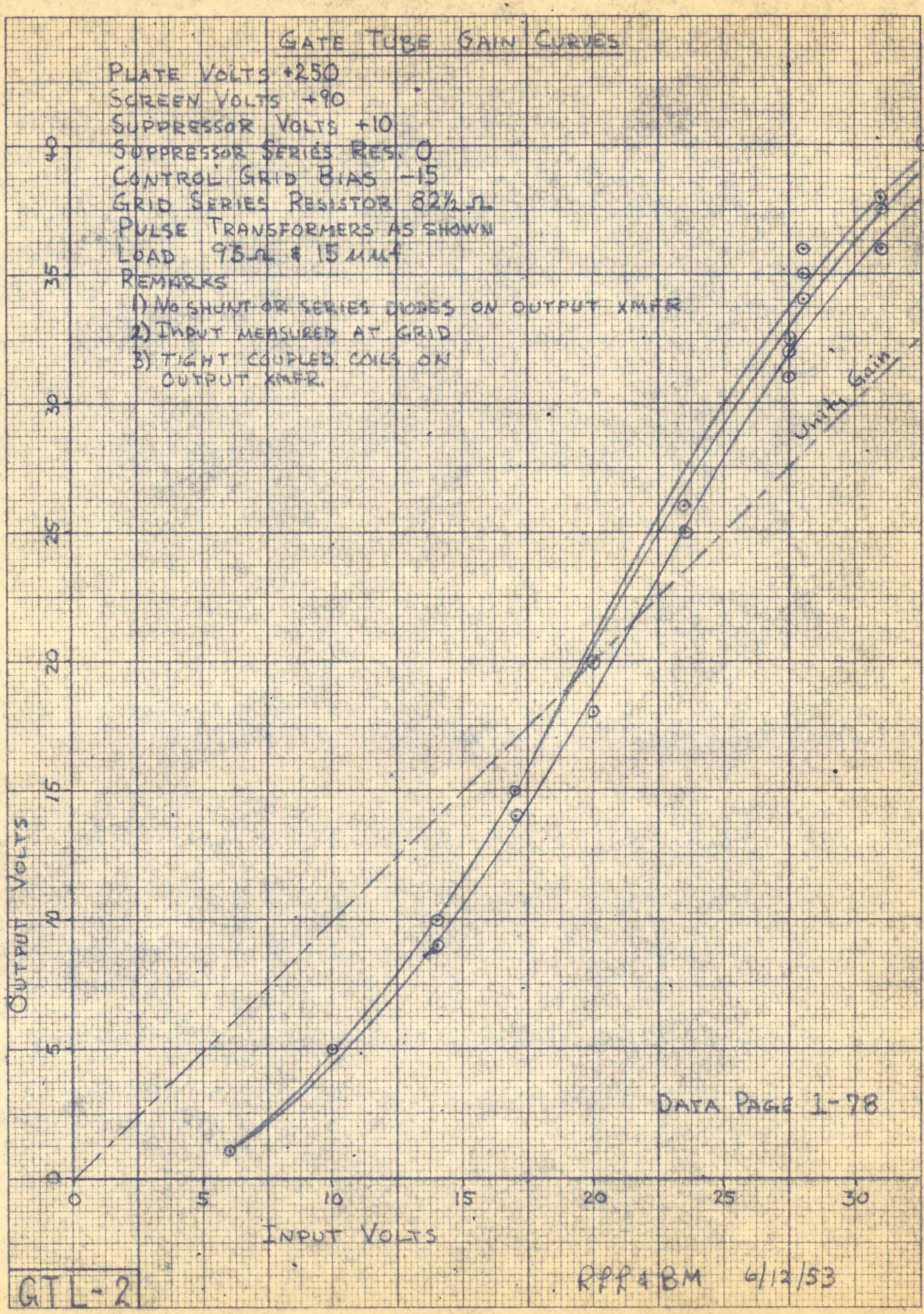
DATA PAGE 1-78

GTL-1

R.F.& B.M. 6/12/53

GATE TUBE GAIN CURVES

PLATE VOLTS +250
SCREEN VOLTS +90
SUPPRESSOR VOLTS +10
SUPPRESSOR SERIES RES. 0
CONTROL GRID BIAS -15
GRID SERIES RESISTOR 82½ Ω
PULSE TRANSFORMERS AS SHOWN
LOAD 93 Ω & 15 MMF
REMARKS
1) NO SHUNT OR SERIES DIODES ON OUTPUT XMFR.
2) INPUT MEASURED AT GRID
3) TIGHT COUPLED COILS ON OUTPUT XMFR.



DATA PAGE 1-78

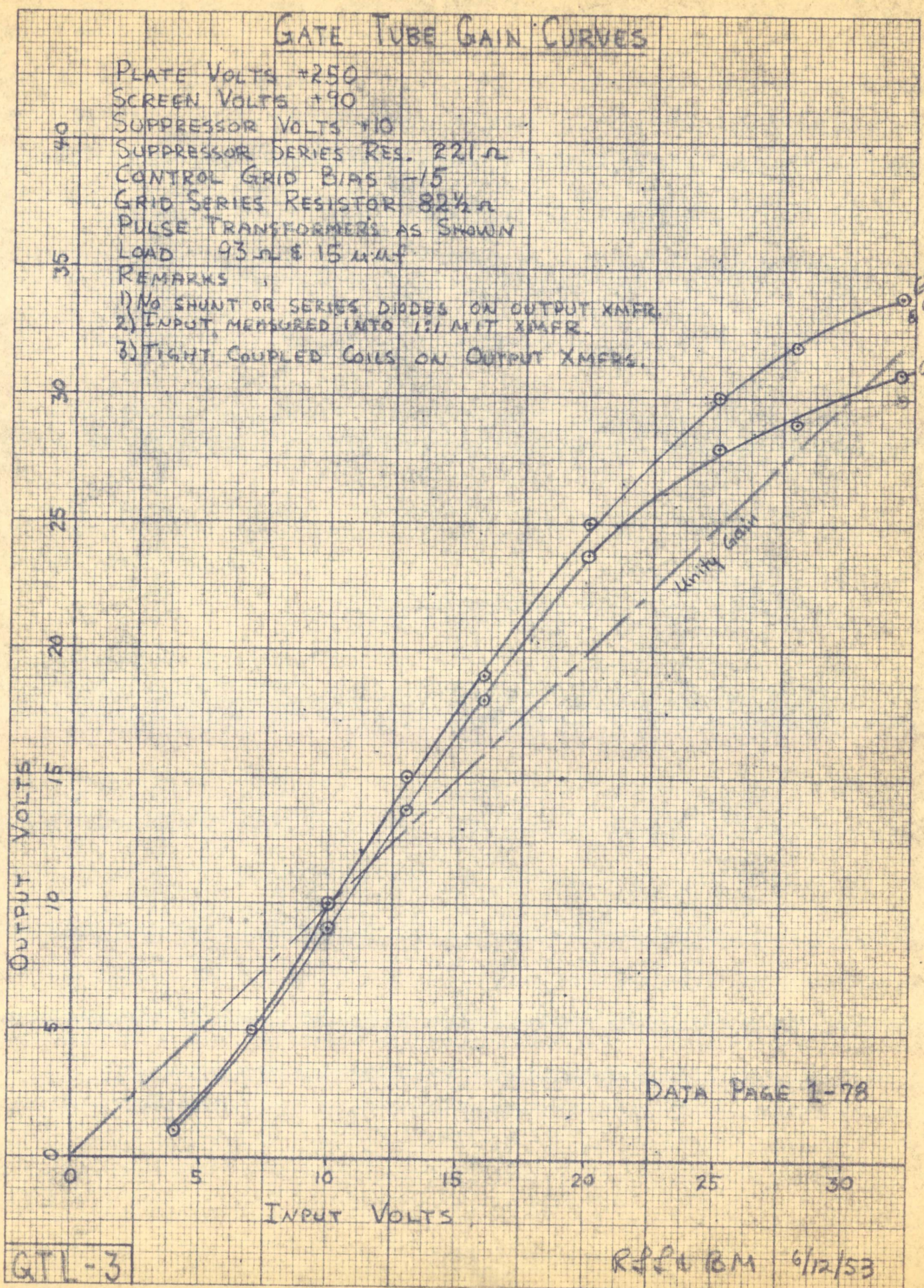
GTL-2

RPP & BM 6/12/53

GATE TUBE GAIN CURVES

PLATE VOLTS +250
SCREEN VOLTS +90
SUPPRESSOR VOLTS +10
SUPPRESSOR SERIES RES. 221 Ω
CONTROL GRID BIAS -15
GRID SERIES RESISTOR 82½ Ω
PULSE TRANSFORMERS AS SHOWN
LOAD 93 Ω & 15 mmf

REMARKS:
1) NO SHUNT OR SERIES DIODES ON OUTPUT XMFR.
2) INPUT MEASURED INTO 1:1 MIT XMFR.
3) TIGHT COUPLED COILS ON OUTPUT XMFRS.

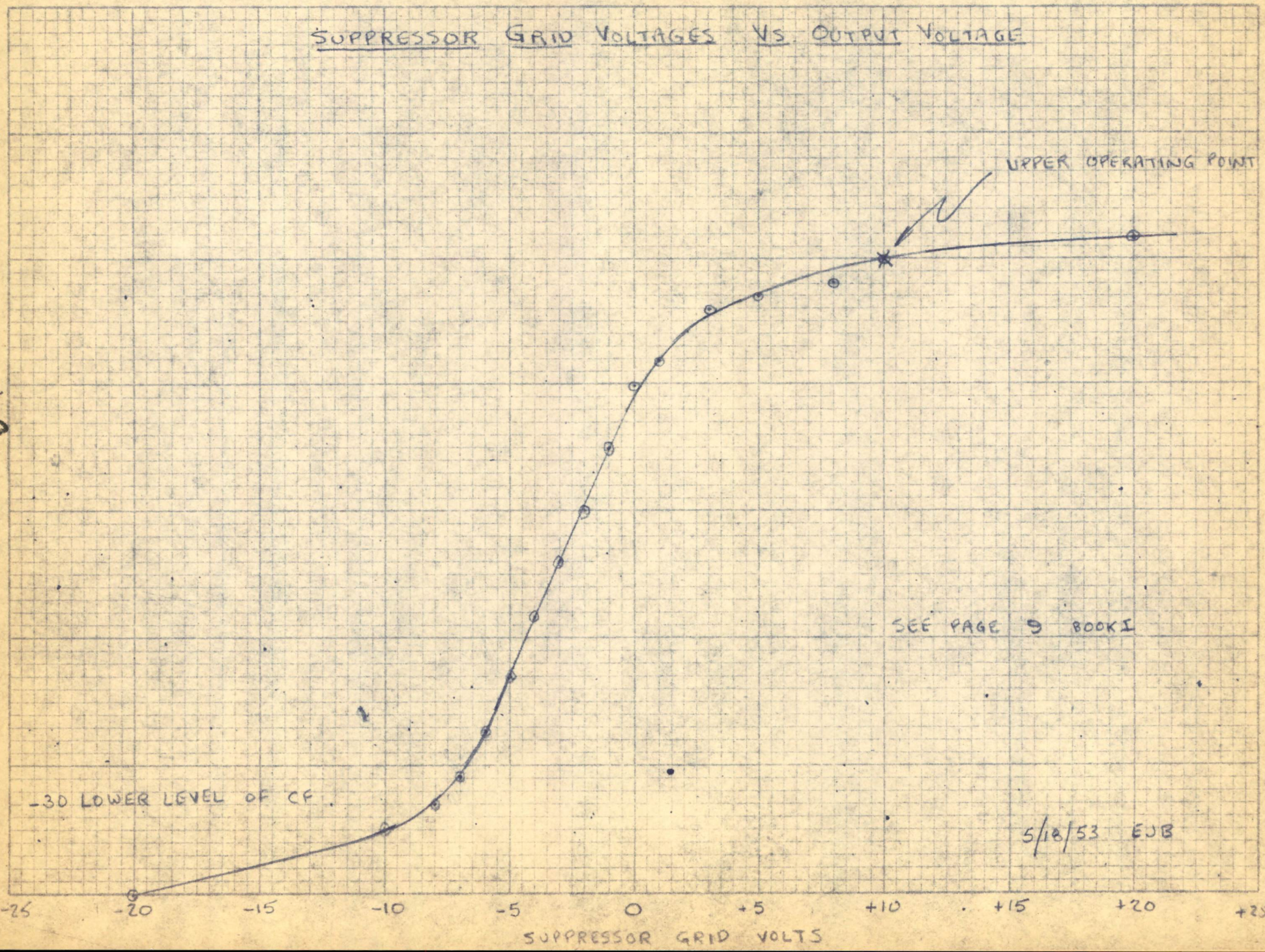


DATA PAGE 1-78

GTL-3

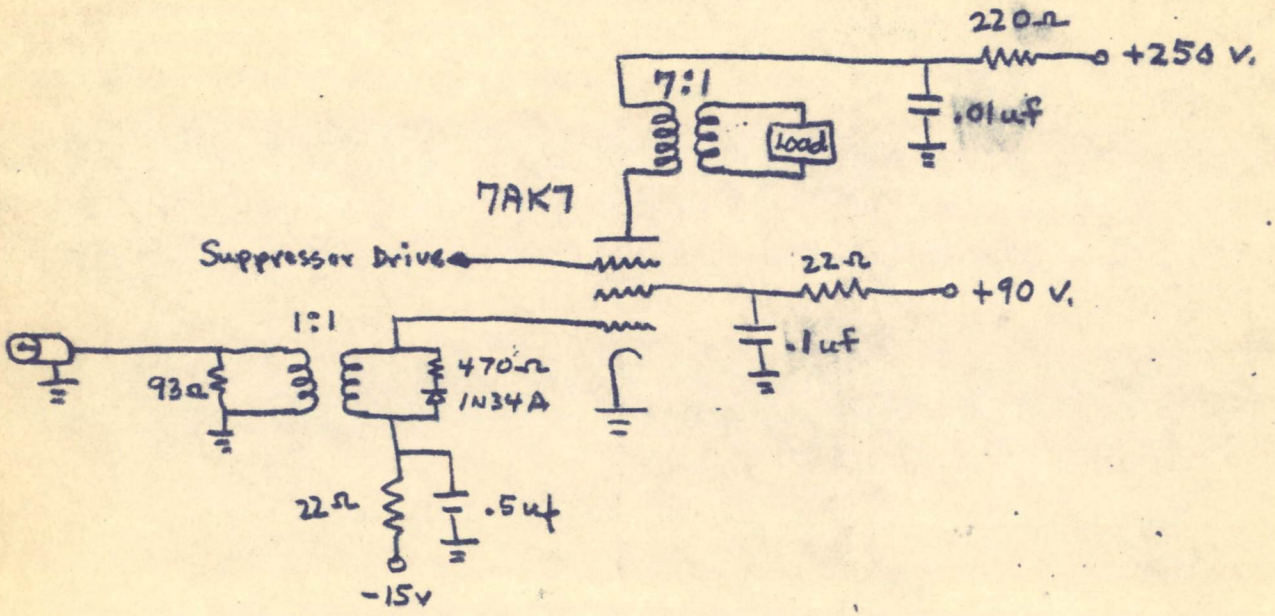
RPH BM 6/12/53

Form No. 893 — 10 Squares to Inch
AMERICAN PAD & PAPER CO., HOLYOKE, MASS.



7AK7 CIRCUIT AND TESTS

Gate Tube Circuit:



Gate Tube Tests:

Data should be taken to plot the following curves:

1. Curves of input amplitude versus output amplitude, pulse width versus input amplitude, and recovery time versus input amplitude for the following cases.
   (a) Resistance loads - 93, 82, 75, 68, 62, and 51 ohms
   (b) 93 ohms and various capacity loads until output falls off in amplitude.
   (c) Repeat (a) and (b) with 40 feet of RG62/U coax between transformer and loads.
   (d) Load of 3 gate tubes and 1 flip-flop under the following conditions:
      (1) Direct to GT & thru xmfr to FF
      (2) Direct to GT & thru diode logic to FF xmfr
      (3) Thru xmfr to each GT and flip-flop diode logic
      (4) Thru common xmfr to GT and diode logic to FF
   (e) Two 7AK7's as an OR circuit with common output transformer. max rep rate of 1 Mc.
   (f) GT driving GT with no xmfr on second GT. Curves should be plotted for second GT by transfer characteristics.
   (g) Repeat steps (d) to (f) with 40 feet RG62/U coax between gate tube and loads.

2. Curves of amplitude output, pulse width and recovery time versus marginal check voltage for plate, screen and control grid voltage marginal checks.

Gene Breiding
Don Thompson
Bob Lindsay
6/22/53

Copy 9

A MAGNETIC-CORE MEMORY WITH EXTERNAL SELECTION

by

Sydney Bradspies

A MAGNETIC-CORE MEMORY WITH EXTERNAL SELECTION

by

Sydney Bradspies

B.E.E. College of the City of New York

(1953)

SUBMITTED IN PARTIAL FULFILLMENT OF THE

REQUIREMENTS FOR THE DEGREE OF

MASTER OF SCIENCE

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

January, 1955

Signature of Author _____
Department of Electrical Engineering, January 17, 1955

Certified by _____
Thesis Supervisor

Accepted by _____
Chairman, Departmental Committee on Graduate Students

ACKNOWLEDGMENT

I wish to thank Professor W. K. Linvill, my Thesis Supervisor, and W. N. Papian and J. I. Raffel of the Lincoln Laboratory for their assistance throughout the course of my investigations and during and after the writing of this report. Without their criticism and encouragement, it is doubtful that the job would have been completed.

I must also express my thanks to the large number of secretaries who have had some part in the physical preparation of my thesis, and to the many other people at the Lincoln Laboratory who aided me so freely during the course of the work.

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A MAGNETIC-CORE MEMORY WITH EXTERNAL SELECTION

by

Sydney Bradspies

Submitted to the Department of Electrical Engineering on January 17, 1955, in partial fulfillment of the requirements for degree of Master of Science.

ABSTRACT

A 3-core magnetic-memory cell was built, tested, and analyzed. One of the three cores is exclusively for the retention of information (memory); the other two cores are involved in the selection process, one during "read," the other during "write." The characteristics observed in this memory suggest the satisfactory response that may be expected:

A complete read and write cycle was completed successfully in 0.5 microsecond.

Voltage outputs from a single memory core were as large as 2.5 volts.

The ONE-to-ZERO ratios were found to be about 20 to 1. ONE to noise ratios were several hundred to one.

These results compare favorably with those encountered in present coincident-current memories.

Some drawbacks were encountered in this external-selection memory. To obtain the requisite high operating speed, the switch cores must be driven very heavily; also, to obtain maximum efficiency the cores should not switch before the currents have risen to their final values. These conditions require a source of large currents with very fast rise and fall times. In driving a large-scale memory, it is difficult to obtain fast rise and fall times because of the inductance of partially selected cores and because of the long leads required. Furthermore, the voltages induced in the selected switch cores are large; a number of these cores in series might well present an excessive back voltage to the core driver. These and many other problems must be solved before it is possible to realize the fullest capabilities of a magnetic-core memory utilizing external selection.

Thesis Supervisor: William K. Linvill
Title: Associate Professor of Electrical Engineering

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LIST OF ILLUSTRATIONS

CHAPTER 1

INTRODUCTION

The memory function of a digital computer may be provided by a set of cores which can be magnetized in one of two possible directions. There is a correspondence between the identity of the core involved and an address which locates the core. The state of a core is made to correspond to the value (ONE or ZERO) of a digit in a number whose address corresponds to the core. To be useful in a computer, the core must be written into (magnetized) and read from (sensed) and it must hold (remember) a given state until it is changed. Since it is necessary to single out one core for a reading or writing operation, this location of the single core (selection) is an important problem. The present Whirlwind memory system combines the processes of selection and memory into one set of cores (one core per bit). The two processes have conflicting requirements and to divorce the two functions appears to be profitable. The function of this thesis is to analyze a scheme in which one set of cores is used for memory, and another set is used for selection.

In order to fully understand and appreciate the potential advantages offered by a memory with external selection, it is necessary to discuss the properties of the coincident current type memory system which is now in use, and which combines memory and selection in a single core per bit.

A. The Coincident-Current Memory

The operation of the coincident current, two-to-one selection

system is explained in Figure 1.1 and 1.2.[1,2]

A core will rest in equilibrium either at ϕ_o (arbitrarily called a ZERO) or at ϕ_1 (ONE). The point at which a core rests is determined by its recent history. At the intersection of each X and Y line (Figure 1.2), there is a magnetic core. Both a Z (inhibiting winding used for writing ZEROs) winding and a sensing winding (used for reading out of the memory) are threaded through each core.

The "read" operation passes $+ I_m/2$ through the selected X and Y coordinates, exciting the selected core by $X + I_m$. If the core holds a ONE, its flux state is reversed, and a large voltage is induced in the sensing winding. If, on the other hand, the core holds a ZERO, there is a relatively small change of flux in the core, and little voltage is induced, provided that the ratio $\phi_o/\phi_m = 1$ (Figure 1.1). The read operation is destructive; that is, when reading has been finished, the core holds a ZERO, regardless of its original contents.

A number of cores lie on either the selected X coordinate or the selected Y coordinate. These cores are excited by $+I_m/2$ (that is, they are half selected). At the time of the read operation, the information held by these cores is of no interest; furthermore the information that they hold should not be destroyed. For these reasons, the half-selected cores should not even be partially switched. As a consequence (referring to Figure 1.1), the ratio ϕ_d/ϕ_1 must be close to unity.

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[1] Numbered references refer to correspondingly numbered references in the Bibliography.

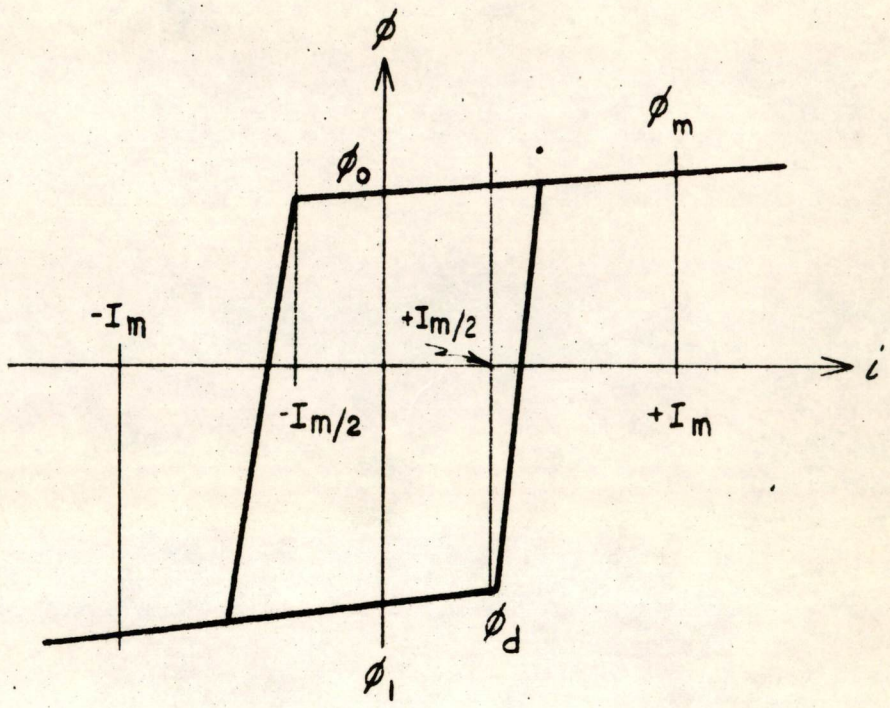


FIG. 1.1

RECTANGULAR HYSTERESIS LOOP OF FERROMAGNETIC MEMORY CORE

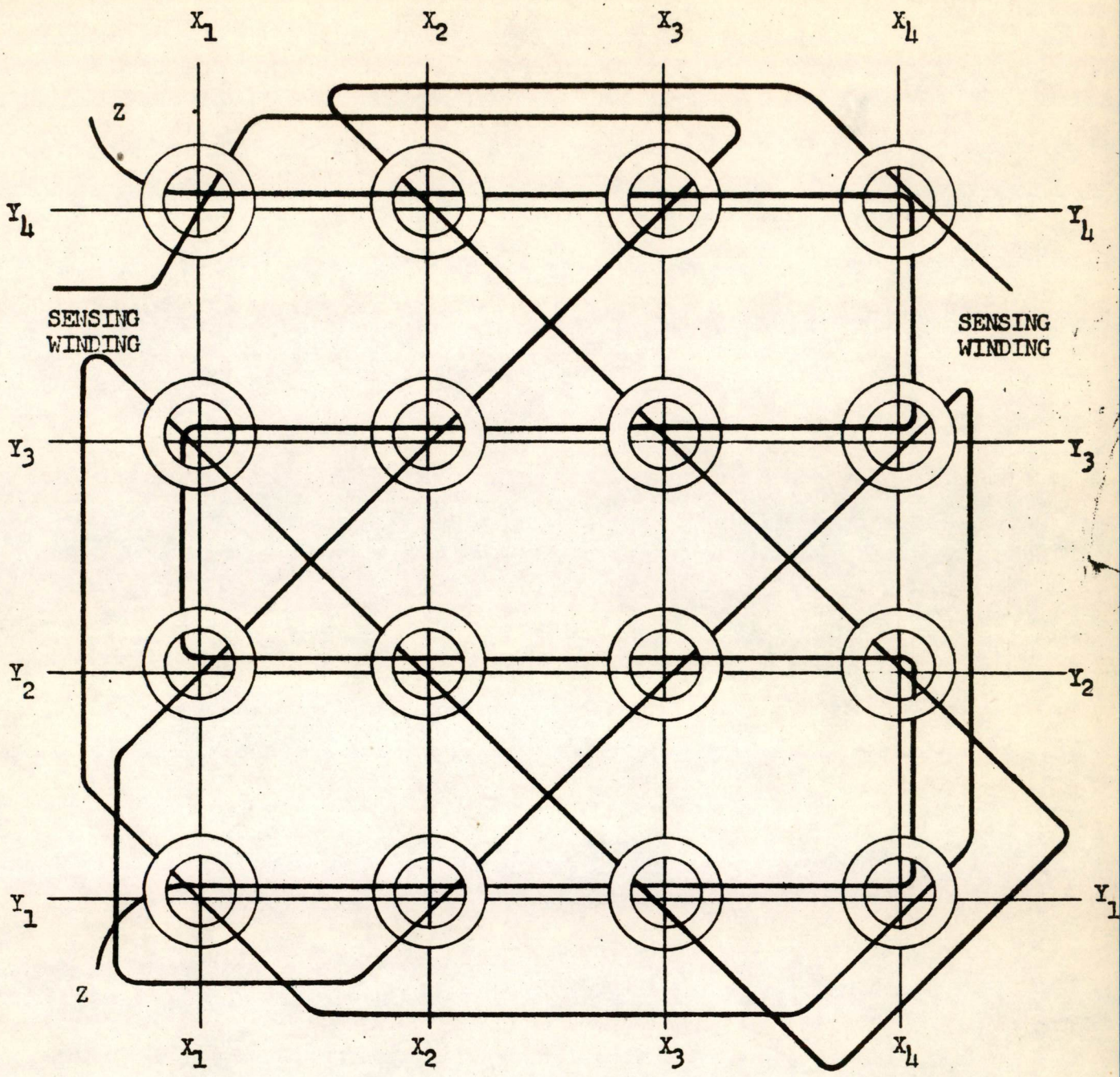


FIG. 1.2

A FOUR-BY-FOUR PLANE OF FERROMAGNETIC MEMORY CORES

These, then, are the requirements for a core in the coincident current magnetic memory - the ratios ϕ_o/ϕ_m and ϕ_d/ϕ_1 must each be close to one. Because of symmetry, $\phi_1 = -\phi_o$. Therefore, these conditions may be combined and restated: $|\phi_d/\phi_m|$ must be close to unity if the memory is to operate (1) with a minimum of output signals from half-selected cores and from the selected core (if it holds a ZERO); and (2) with a certainty that the information is not being destroyed. The ratio $|\phi_d/\phi_m|$ is called the squareness ratio,[3,4] and it is generally somewhat less than unity.

Writing is accomplished in one of the following manners:

To write a ONE, pass currents of $-I_m/2$ down the chosen X and Y coordinates.

To write a ZERO, pass currents of $-I_m/2$ down the chosen X and Y coordinates, and a current of $+I_m/2$ through the Z (inhibiting) winding.

Block diagrams of operation of a memory may be found in the memorandum "Description of Memory Test Setup V1."[5]

The core performs two functions in the coincident-current magnetic memory just described: primarily it stores information, but its rectangular hysteresis loop also provides the nonlinearity which is required for selection - that is, discrimination between excitations of $I_m/2$ and I_m. Because the core must be used for selection, it must have a rectangular hysteresis loop with $|\phi_d/\phi_m| \cong 1$, and the magnitudes of the switching currents are severely limited because $I_m/2$ must not even partially switch a core.

For a given switching core, the change of flux is independent of the switching time, τ, and the voltage induced in the sensing winding is inversely proportional to τ. Thus, shortening τ increases the output voltage and also increases the speed of the memory. It has been found [4] that τ is inversely proportional to the net exciting current (the net current is $I_{net} = i - \frac{I_m}{2}$ and $H_{net}\,\tau = S_w$, a constant of the core material). The total exciting current may not under any circumstances exceed I_m because of the coincident-current restrictions. This, of course, immediately imposes an upper limit to the switching speed of the cores.

There are two methods that can be used to descrease τ. One is to decrease S_w. This is essentially a problem of trying to improve the magnetic materials of which the cores are made. It has been found that S_w of metals is generally lower than that of the ferrites. But the coercive force of the metals is considerably lower than that of the ferrites, and so the metals switch more slowly than the ferrites, under the restrictions of the coincident-current memory. A second method is to increase H_{net}. For coincident current operation this requires a material with very high coercive force.

B. The Memory With External Selection

A system that does not use the memory cores for selection would avoid the restrictions on exciting current, which could be made very large, thereby significantly reducing the switching time, and it would reduce the rectangularity requirements on the hysteresis loops of the cores to some extent. Such systems have been proposed independently by J. Raffel[6] and Dr. R. Slutz[7]. The system that will be considered in this report is the

one introduced by the former.

In this memory system, switch cores A and B (Figure 3.1) are used for selection. Memory core M is used solely for the retention of information. This system requires three cores for each bit of information as compared to one core in the present memory.

The principal characteristics that are essential are nonlinearity in the switch cores and remanence in the memory core.

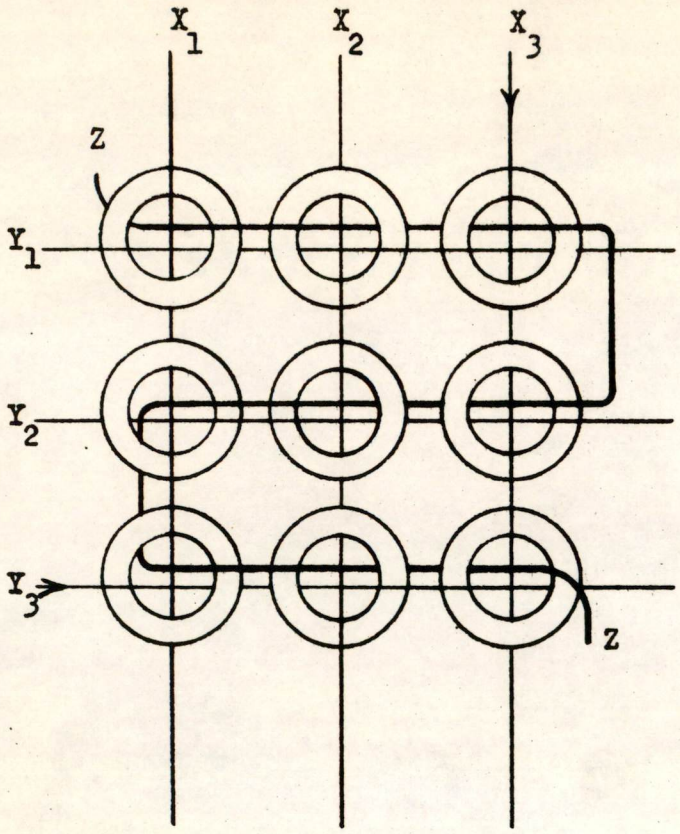
Consider the operation of the 9-core (3x3) memory plane flanked by two 9-core switch planes (Figure 1.3).

The cores of Switch Plane A are for the read operation, and the cores of Switch Plane B are for writing. The Z-winding (Figure 1.3a) carries the bias current I_{Za} in plane A, and I_{Zb1} in plane B.

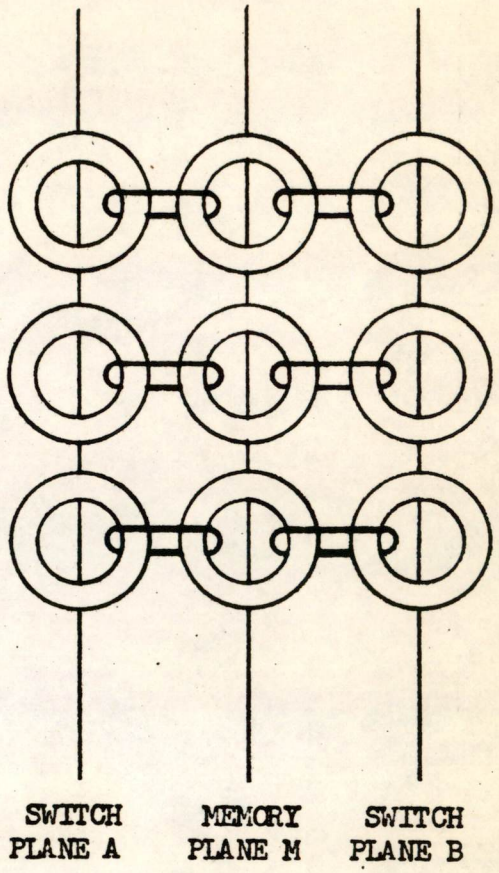
The read operation sends currents $\frac{I_{in}}{2}$ ($= I_{xa} = I_{ya}$) along the selected X and Y coordinates. The selected switch core in the A plane is switched from Z_a to $Z_a + X_a + Y_a$ (Figure 3.2). When the excitation of lines X and Y is removed, switch core A reverts to Z_a. The output of core A (Figure 1.4) is coupled to the memory core, M, and the information is read out; at the completion of the read cycle, the selected memory core holds a ONE.

If a ONE is to be written no further excitation is necessary and switch core B is not excited during the write cycle.

If a ZERO is to be written, $\frac{I_{in}}{2}$ ($= I_{xb} = I_{yb}$) is passed along the selected X and Y coordinates in switch plane B. The output of core B (Figure 1.5), produces first a negative and then a positive pulse. The negative pulse merely moves core M (which is already in the ONE position)



a. SWITCH CORE PLANE (EITHER A OR B)
TOP VIEW



b. SIDE OF 9-BIT MEMORY

FIG. 1.3

NINE BIT MEMORY "PLANE", CONSISTING OF 9 MEMORY CORES AND 18 SWITCH CORES

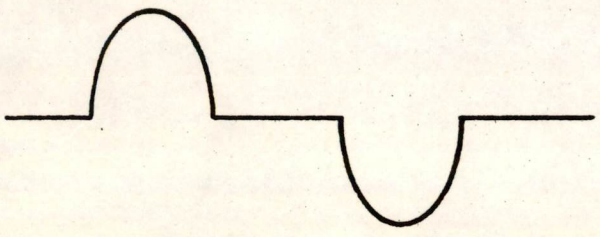


FIG. 1.4

READ OUTPUT OF CORE A

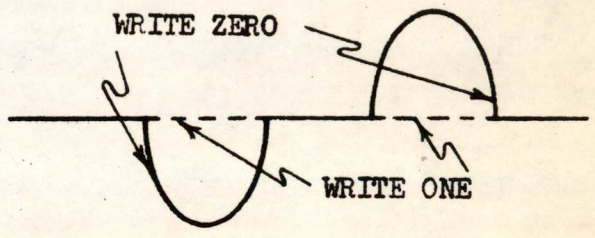


FIG. 1.5

WRITE OUTPUT OF CORE B

towards saturation. The positive pulse switches the memory core to the ZERO state, and leaves it there.

The advantages that may be derived from the memory unit just described are listed below:

1. Speed. The switch cores are not required to retain information. Thus, it is permissible to bias these cores, and drive them very heavily when they are fully selected. They will switch rapidly and their output voltages will be large. The large voltages are used to drive the memory cores, and consequently, the memory cores are also rapidly switched. Complete read and write cycles were finished successfully in less than 0.5 microsecond.
2. Large Signals. The high switching speeds discussed above lead directly to the fact that the output voltages are very large. Because of this, the problem of amplifying the signals is greatly simplified. ONES were generally greater than two volts high, when a standard memory core was used as the storage element.
3. Low Noise Levels. The memory system using external selection cascades two nonlinear elements. The noise outputs that result from partially selected switch cores are found to be extremely small compared to full select outputs. The ratio of a fully selected ONE to a half selected output is considerably larger in the system using external selection than is the same ratio in the coincident current memory.

They were several hundred to one. The ONE to ZERO ratios were about the same in the two systems -- about 20 or 30 to 1.

4. Relaxation of Requirements on Core Characteristics. The cores are not as critical in a system using external selection as they are in the coincident current scheme. The essential characteristics are a nonlinear switch core, and a memory core with remanence.

5. No Destruction of Information. The noise outputs from partially selected switch cores are extremely small, and so there should be no tendency to destroy information stored in the memory cores.

The memory using external selection has several drawbacks, some of which may be extremely serious. All of the disadvantages are listed here:

1. Three cores are required per bit of information. The coincident current memory system uses only one core per bit.

2. Construction Difficulties. The coincident current memory is laid out in a very simple plane (Figure 1.2). It is not possible to construct the memory using three cores in this manner; the difficulty may be appreciated by imagining an attempt to build the memory as shown in Figure 1.3. Other methods of putting the memory together must be conceived.

3. The Driving Problem. Large driving currents are required, and these currents must rise very rapidly so that the cores are not switched during the current rise time. The induc-

tance of partially selected switch cores, plus the inductance of the driving lines, plus the back voltages of fully selected switch cores present a load that will make it very difficult for the source output to rise rapidly to a large value of current. There are several ways in which to reduce the magnitude of this problem. The memory should not be large. A small sized memory will lower the inductance that must be driven. The switch cores should be as small as possible (memory core size) in order to reduce the back voltage induced in a switched core.

4. Memory Core Size. If, as indicated above, the switch cores are to be of standard memory core size, then the memory cores must be far smaller than the standard memory core. The reason is that it has been found that the switch core must be five or six times larger than the memory core in order to successfully operate the three core memory. It is not possible to make cores physically smaller than the standard memory core size, and so some other method of reducing the memory core must be introduced. It should be noted that none of the problems just discussed have been successfully solved yet.

5. Core Heating. The memory should be driven heavily and a possible result is that the cores will overheat, and their characteristics deteriorate.

The purpose of this thesis is to analyze, test, and evaluate the memory system just described.

Chapter 2 gives an analysis of the switch and memory cores to be used in the three-core-per-bit memory. The characteristics of these cores are approximated by linearized equivalent circuits which greatly aid the solution of some problems encountered in the memory unit.

Chapter 3 shows a detailed account of the characteristics of the cell comprised of the switch cores and the loop of wire coupling them to the memory core. The results expected from the linearized memory unit are given graphically and algebraically for various operating conditions. Finally, the experimental results obtained using various combinations of parameters in the memory unit are described. Chapter 4 gives the conclusions and the difficulties that may be expected in attempting to put the results of Chapter 3 to use in a practical system.

The appendices contain the derivations of some of the equations encountered in the body of the thesis. One appendix is devoted to a description of the high speed core driver that was developed in order to carry out the tests performed.

CHAPTER 2

THE NATURE OF THE SWITCH AND MEMORY CORES

The characteristics of the cores needed for both of the memory systems described in Chapter 1 will be discussed in this chapter.

The properties of the switch cores to be used in the memory with external selection are presented in Section A. Section B contains a discussion of the memory core, and an algebraic solution of the coincident current memory core outputs. In Chapter 3, these results will be compared to a similar set of equations derived for the memory unit using three cores per bit.

A. The Switch Core

Much of the material to be presented here concerning the switch core has been known for some time.[6,8] A brief summary of these results and a method of regarding the switch core which leads to an easy analysis of the three-core memory will be given.

The ideal switch core has the magnetization curve shown in Fig. 2.1. A more realistic approximation is shown in Fig. 2.2. The hysteresis loops of the actual switch cores used for this thesis are shown in Fig. 2.3. It is noted that the pictures shown in Fig. 2.2 and 2.3 are essentially the same. The ideal core differs from the actual cores in two immediately evident manners; (1) the actual core has a hysteresis loop, and (2) the real cores do not saturate as well as the ideal core does.

The first difference is of little or no consequence here. The operation of the switch core is not greatly impaired by the fact that it has a finite coercive force.

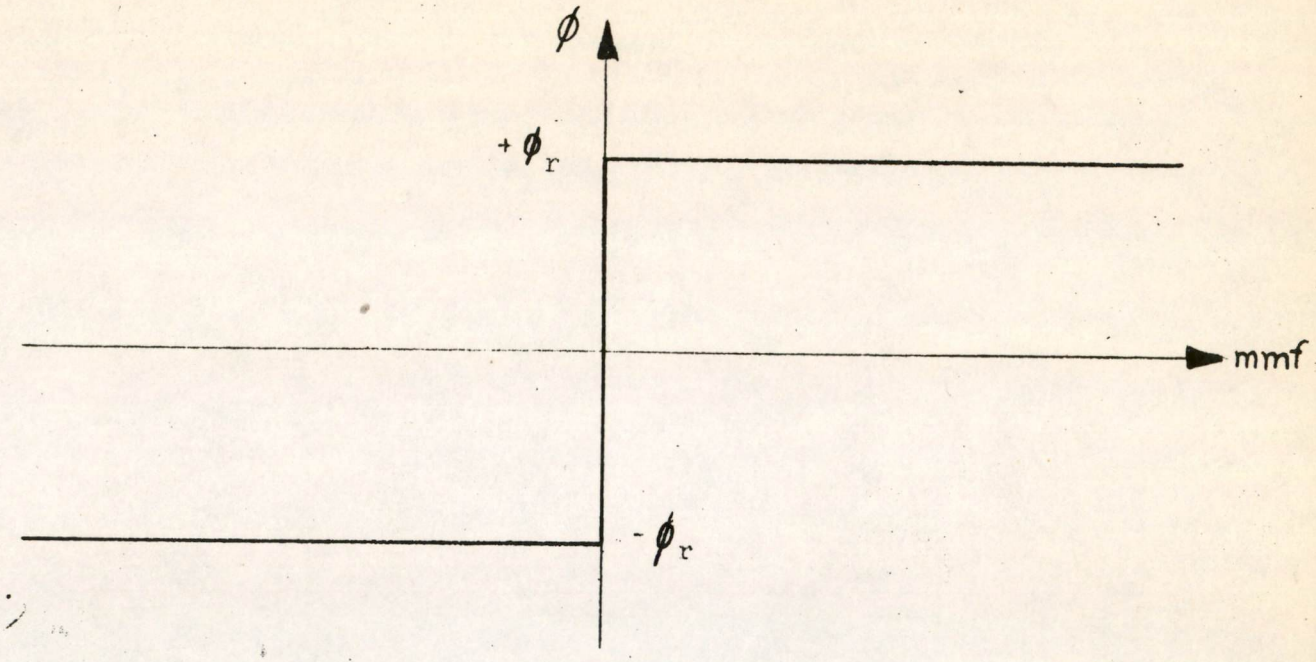


FIG. 2.1

IDEALIZED SWITCH CORE MAGNETIZATION CURVE

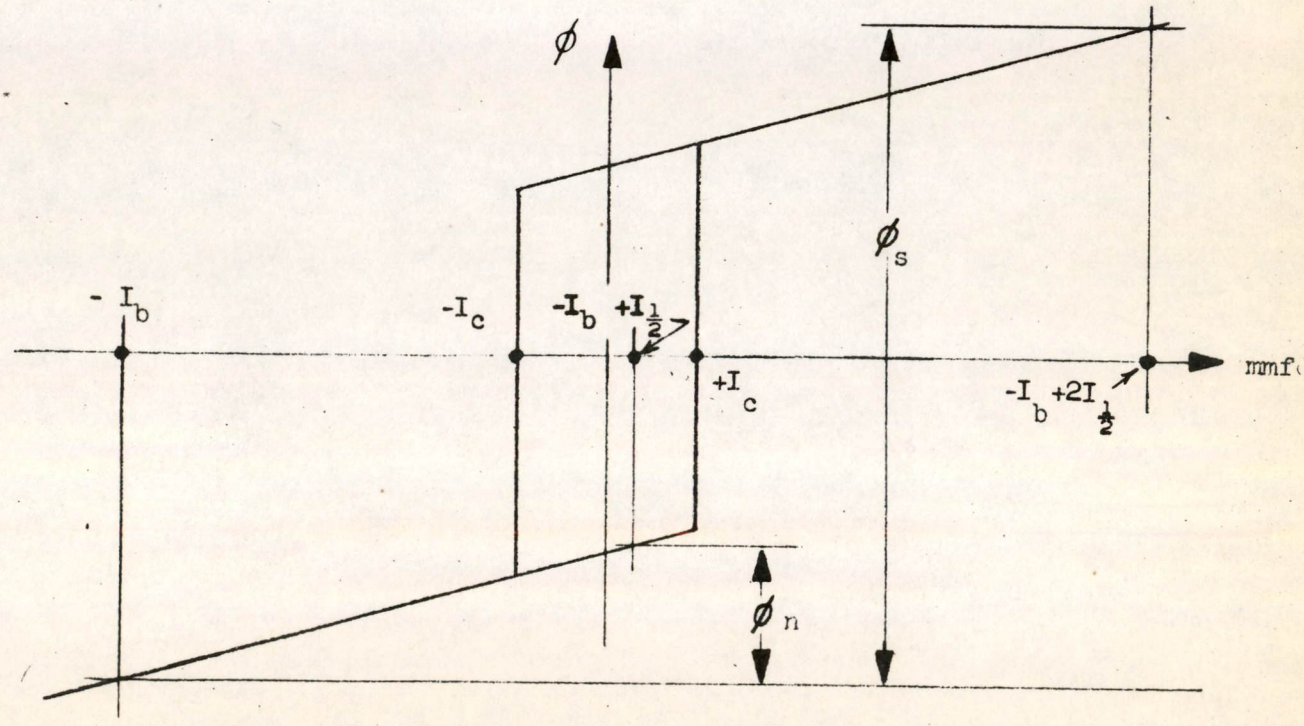
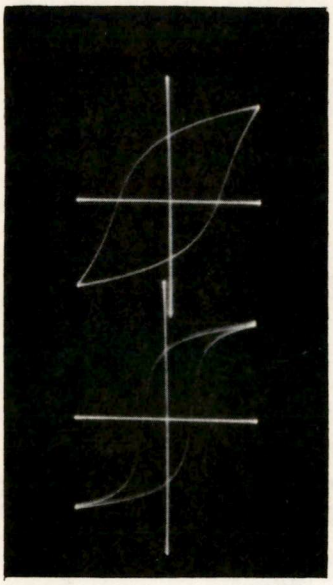


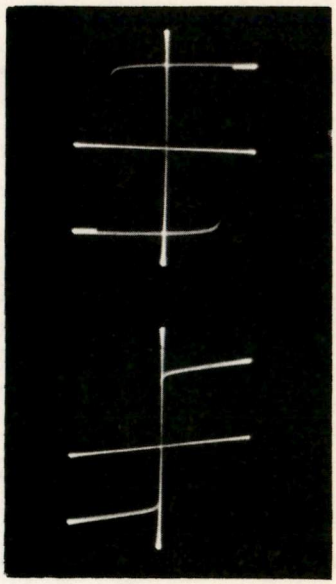
FIG. 2.2

MORE REALISTIC SWITCH CORE MAGNETIZATION CURVE



c- DCL-3-44
SIZE 1F397

$B_{SATURATION}$ = 3.2 MAXWELLS
H_c SATURATION = 1.8 AMP-TURNS
SQUARENESS RATIO = 0.030



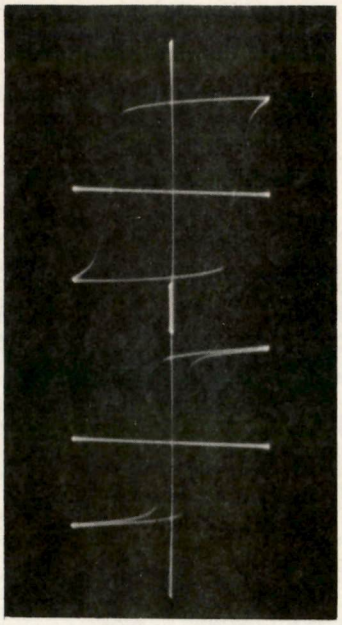
d- MOLYBDENUM PERMALLOY
SIZE: $\frac{1}{8}$ MIL x $\frac{3}{4}$" DIAMETER
x $\frac{1}{8}$" WIDE x 20 WRAPS
$B_{SATURATION}$ = 1.68 MAXWELLS
H_c SATURATION = 0.36 AMP-TURNS
SQUARENESS RATIO = 0.835

NOTE:
TOP PICTURE SHOWS MAXIMUM SQUARENESS LOOP.
BOTTOM PICTURE SHOWS SATURATION LOOP.

FIG. 2.3

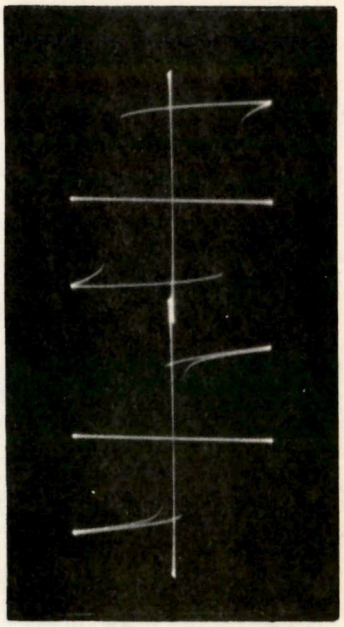
ACTUAL CORE MAGNETIZATION CURVES

A-61332



a- 11DCL-2-720H2L-1
SIZE 1D264

$B_{SATURATION}$ 27.2 MAXWELLS
$H_{c\ SATURATION}$ 2.35 AMP-TURNS
SQUARENESS RATIO 0.815



b- 11DCL-2-720H2L-1
SIZE 1F395

$B_{SATURATION}$ 4.8 MAXWELLS
$H_{c\ SATURATION}$ 1.56 AMP-TURNS
SQUARENESS RATIO 0.830

NOTE:
TOP PICTURE SHOWS MAXIMUM SQUARENESS LOOP
BOTTOM PICTURE SHOWS SATURATION LOOP

FIG. 2.3

ACTUAL CORE MAGNETIZATION CURVES

A-61333

The second difference, however, is of no little importance. The manner in which these cores are operated requires that flux changes in the saturated region be as small as possible.

1. Operation of the Switch Core

It is possible to build a plane of switch cores. At first glance, it might appear as though the switch plane of Fig. 2.4 and the memory plane of Fig. 1.2 are the same. This is not the case, for there are two differences; (1) the operation of the switch plane is not at all like the operation of the memory plane because of the fact that the switch plane serves a different function, and (2) the sense winding must be removed, for each core has its own load, and each load is driven individually; the switch core is not selected and switched in order to determine its information content, but rather, this operation is carried out in order that the core output may do some work. Thus, a switch core plane is as shown in Fig. 2.4.

In the memory matrix, discussed in Chapter 1, the Z winding was used only when it was desired to write a ZERO into the selected core. The current passed through this "inhibit" winding was utilized in preventing a selected core from switching.

In the switch matrix (Fig. 2.4), however, the Z winding is not necessarily an inhibiting winding, but is always used for the purpose of biasing. (Actually, in switch planes which require inhibition there may be two Z-windings if it is desired to isolate the inhibition (which may or may not be applied) and the bias (which is always applied during the operating cycle).) There are two switch planes required for each digit in the three-core-per-bit memory, which is to be discussed. One plane does not require inhibiting pulses and the other does. Both, of course,

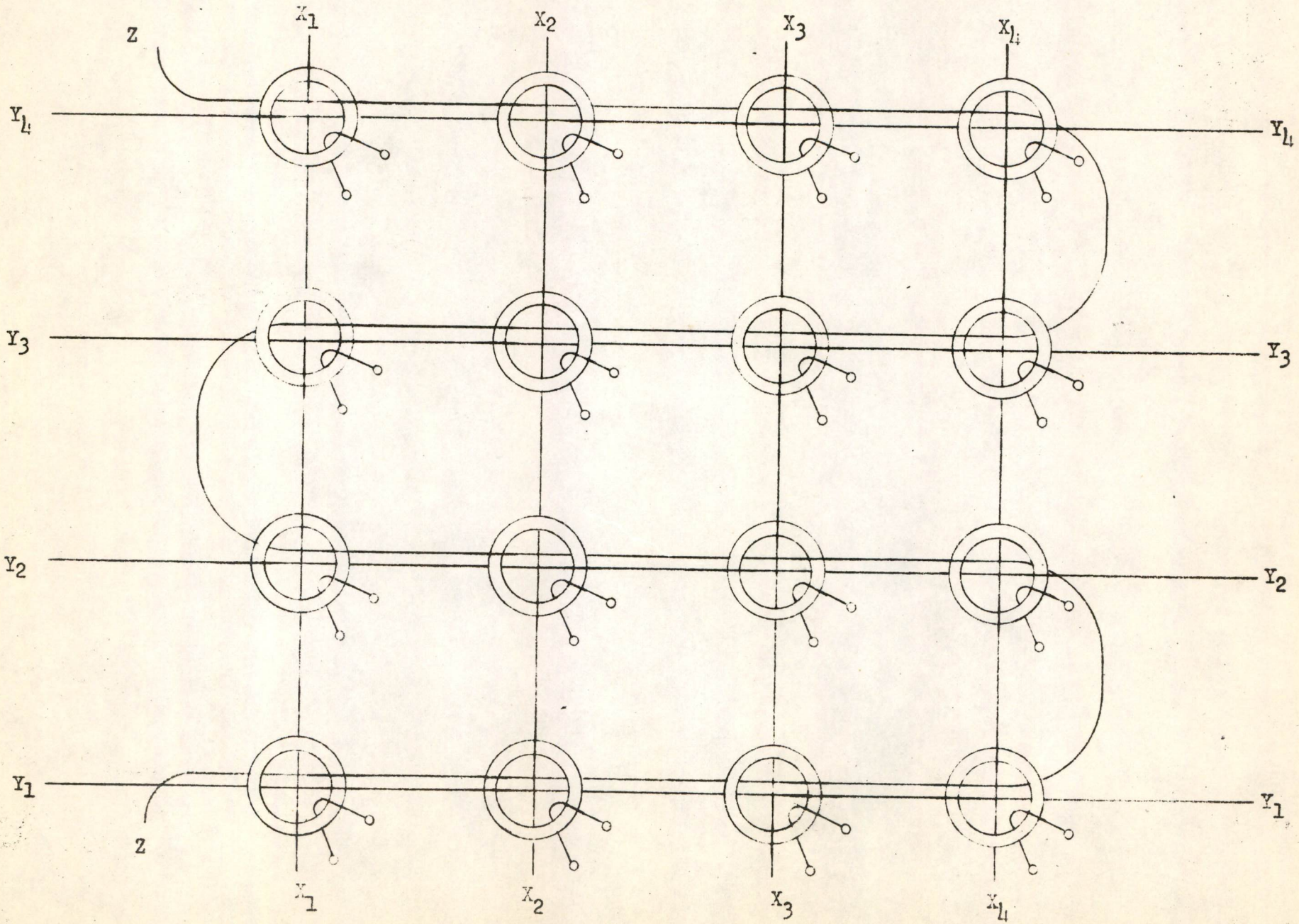


FIG. 2.4

A FOUR-BY-FOUR PLANE OF THIN MAGNETIC SWITCH CORES

require bias. The bias should consist of a steady direct current. During the course of this work, pulsed d.c. was used for bias because of the equipment available at Lincoln Laboratories. The operation of the memory unit is unaffected by the nature of the bias currents.

The core whose operation is to be described has the "Realistic Magnetization Curve" of Fig. 2.2. Bias is applied to all cores in the plane by means of the Z winding and it is I_Z amp-turns. The X and Y coordinate of the selected core are excited with $\frac{I_{in}}{2}$ $(=I_X = I_Y)$ amp-turns. The net driving mmf applied to the selected core is $I_{in} - I_Z$; a number of cores are partially selected and the excitation that they receive is $\frac{I_{in}}{2} - I_Z$; the remainder of the cores are unexcited and they only receive the bias current, I_Z.

The excitation experienced by the selected core must exceed the coercive force, and so

$$I_{in} - I_Z > I_C \qquad (2.1)$$

The excitation driving the partially selected cores must not exceed the coercive force, and so

$$\frac{I_{in}}{2} - I_Z \leq I_C \qquad (2.2)$$

In Chapter I, it was noted that when a core switches,

$$H_{net}\,\tau = Sw \qquad (2.3)$$

where H_{net} is the mmf corresponding (in the case under discussion) to a driving current of $I_{in} - I_Z - I_C$ (the amount of current by which the coercive force is exceeded), τ is the switching time and Sw is a constant of the material.

As has been pointed out before, in order to switch a core of a given material as rapidly as possible, it is necessary to raise H_{net}.

Assume, for convenience, that equation (2.2) is satisfied by the equal sign. Then the net current through a selected core is $\frac{I_{in}}{2}$, and the larger this current is, the faster the core will switch. Although it is true that the most favorable operation, as regards speed, is obtained by employing driving currents as large as possible and adjusting the bias so that equation (2.2) is satisfied, there is a practical difficulty encountered. The core drivers have finite rise times. If the driving current is made excessively large, the result is that the core switches during the rise of the current pulse. The remainder of the current is wasted. This result will be observed in Fig. 2.15 and 2.16, in which the peak open circuit output voltages of several switch cores are plotted as functions of the driving current. This point is discussed in Section A.2c of Chapter 2.

It must also be noted that there is a noise output received from half-selected cores. The greater $\frac{I_{in}}{2}$ is, the greater the noise flux, ϕn (Fig. 2.2) is. The relative increase in ϕs is slight. The outputs of the partially selected cores could conceivably become large enough to do the job that only a fully selected core should do and this is undesirable. The conclusions that must be drawn, then, are that the allowable amount of excitation of the cores is limited by the rise time of the drivers, and by the desire to keep the noise outputs low.

2. Analysis of Switch Core Operation

A single switch core is shown in Fig. 2.5. The X, Y and Z windings each have N_1 turns (X and Y are shown as one winding) and the output winding (secondary) has N_2 turns.

The hysteresis loop of this core is shown in Fig. 2.6. It is essentially the same as that of Fig. 2.2, but the variables have been changed.

a. The Half Selected Switch Core

When the switch core is only half selected, it is driven from $N_1 I_Z$ to $N_1\left(\frac{I_{in}}{2} - I_Z\right)$, and it is not switched. The operating path is along a straight line in the ϕ - $N_1 i$ plane, and this corresponds to a linear inductance. (In an actual case, the departure from linearity is not great; Hughes[8] has shown that for the core used in his work that the relative change in inductance in going from N_1 i = 0 to saturation is less than a ratio of 2:1.) An equivalent circuit is drawn in Fig. 2.7. The parameters are derived in Appendix A.

The rise time of the current output of the core driver that was developed for this thesis (Appendix B) is independent of the current amplitude. It is also found that this current rises from zero in very nearly linear fashion. These two facts are very useful in the analysis of the partially selected core because the voltage induced in an inductor is,

$$V_L = L \frac{di}{dt} \qquad (2.4a)$$

In the light of the aforementioned current characteristics, equation (2.4) becomes,

$$V_L = L \frac{\Delta i}{\Delta t} = L \frac{i}{T} = \frac{L}{T} i \qquad (2.4b)$$

Equation (2.4b) is extremely useful as it stands, for L/T is a constant. This constant may be abbreviated by allowing L/T to equal R_{HS}. It is to be understood that R_{HS} is <u>not</u> a resistor. The symbol was chosen because the volt-ampere characteristic of a half-selected switch core is linear.

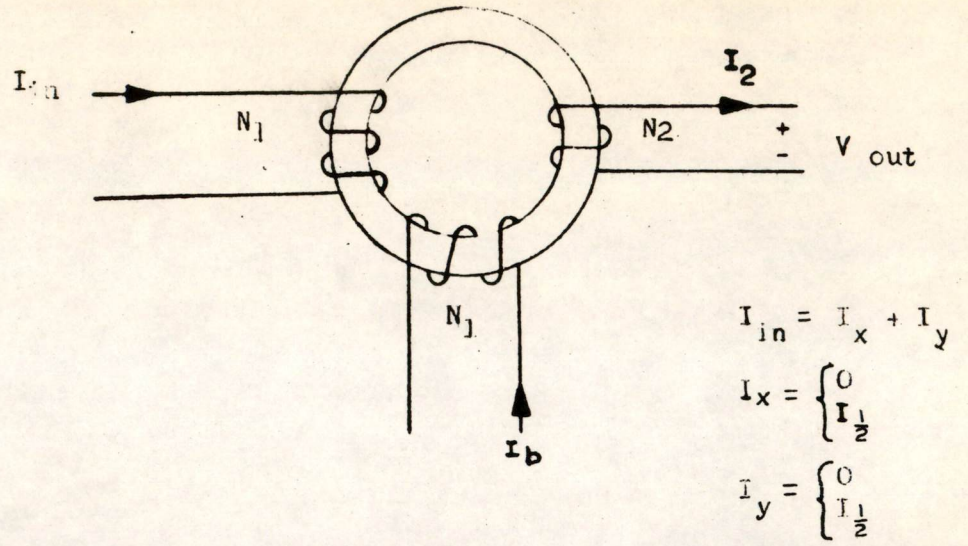


FIG. 2.5

SINGLE SWITCH CORE, WITH X AND Y DRIVING LINES COMBINED

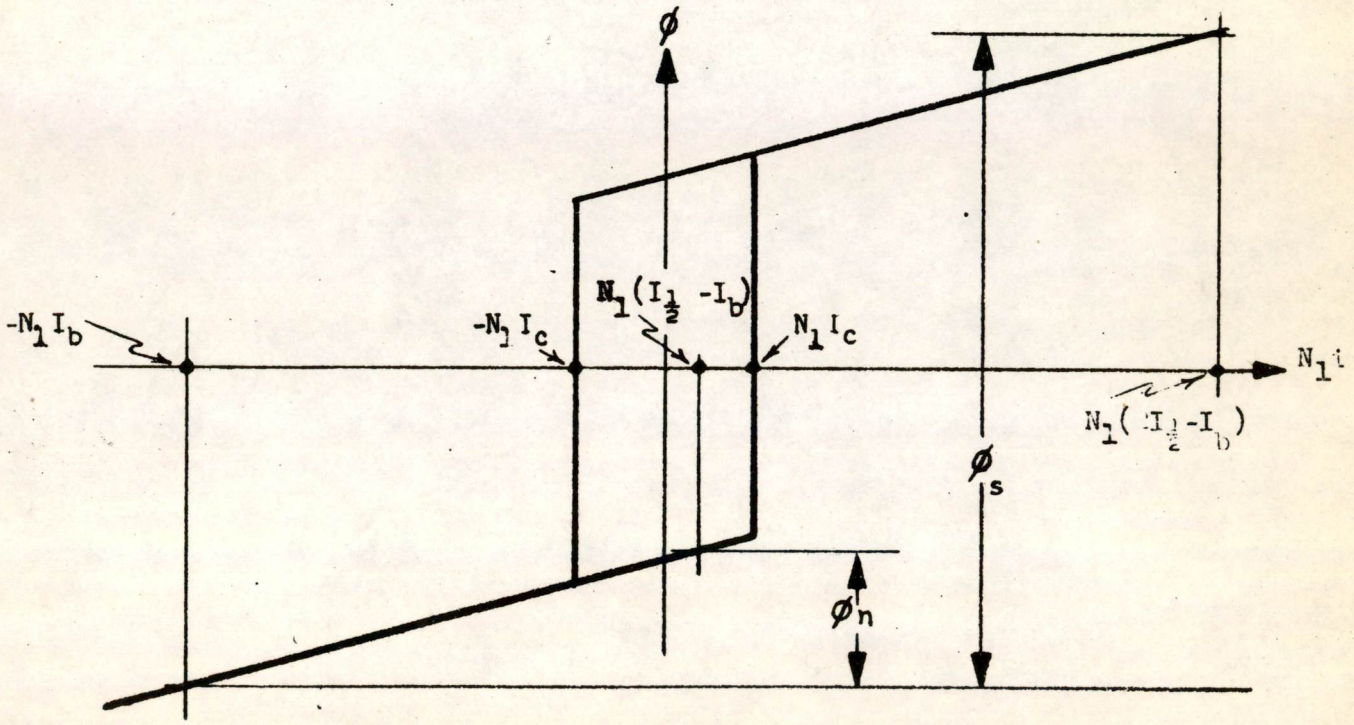


FIG. 2.6

HYSTERESIS LOOP OF CORE SHOWN IN FIG 2.5

Although it is a fallacy, it is convenient to think of R_{HS} as a pulsed resistance (that is, a resistor whose value is a function of time, but is not dependent upon the driving current). The usefulness of this assumption will be brought out later in this chapter, and also in Chapter 3.

Thus, the relationship between the real constants, L and T, and the Fictitions constant, R_{HS}, is

$$R_{HS} = \frac{L}{T} \tag{2.5}$$

The net result of these maneuvers is that the equivalent circuit of Fig. 2.7 (which is valid for all time, provided that the core is never fully selected), may be replaced by the circuit shown in Fig. 2.8. The new equivalent circuit (Fig. 2.8) is valid only during the rise and fall of the input currents, and is useful only for obtaining the peak output voltages. However, it turns out that the only item of interest is the peak output voltage. Thus, Fig. 2.8 satisfies the present need.

Half-selected switch core output voltages and the corresponding driving currents are shown in Fig. 2.9, for the switch consisting of 1D264, of the material 11DCL - 2 - 720H2L-1. The results are tabulated in Table I, for cores of various materials and sizes, and they are plotted in Fig. 2.14, 2.15, 2.16 and 2.17.

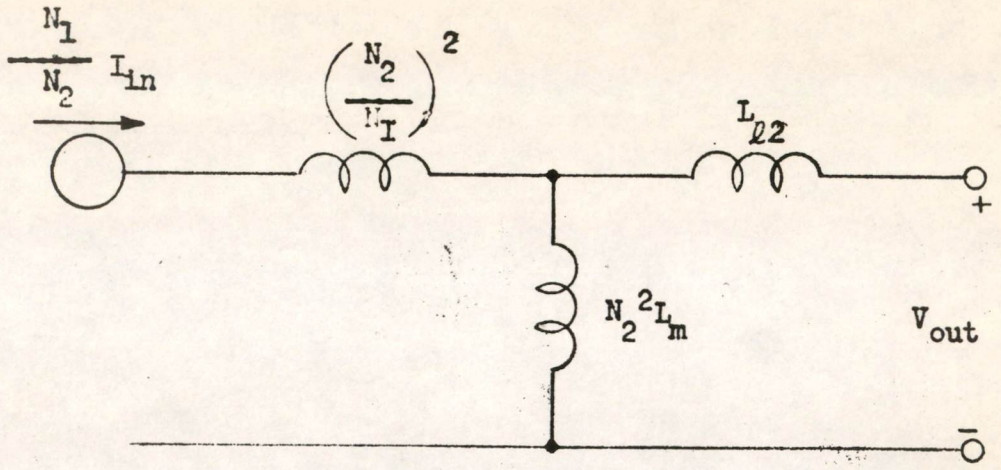


FIG. 2.7

EQUIVALENT CIRCUIT OF HALF-SELECTED SWITCH CORE

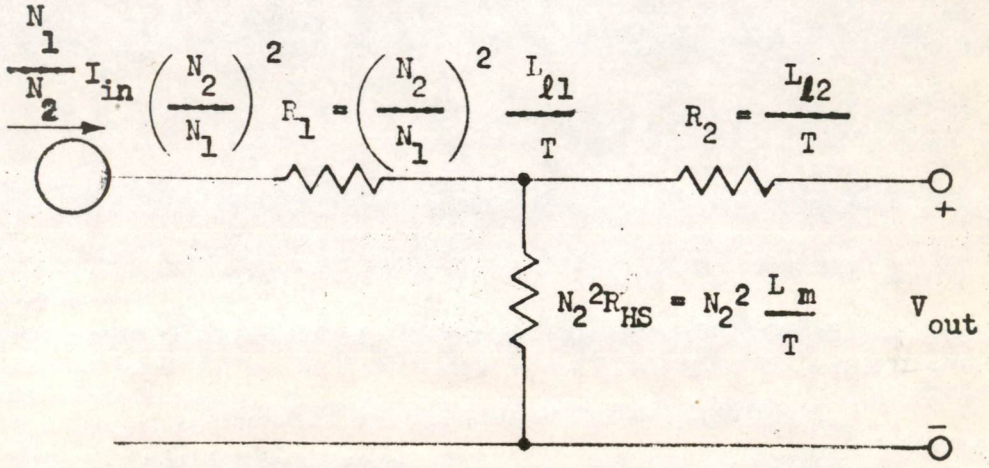
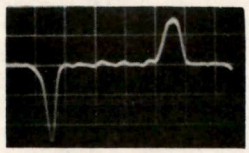
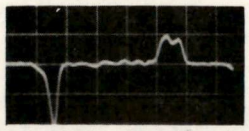
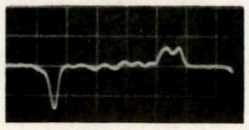
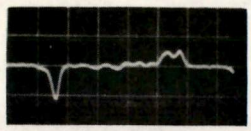
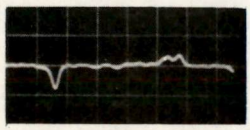
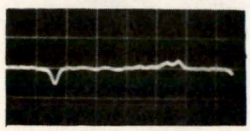


FIG. 2.8

REVISED EQUIVALENT CIRCUIT OF HALF-SELECTED SWITCH CORE

DRIVING EXCITATION (AMPERE-TURNS)	VOLTAGE OUTPUT (VOLTS)
8.5	1.35
7.5	0.99
6.5	0.76
5.5	0.53
4.5	0.37
3.5	0.24

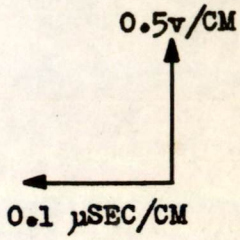


FIG. 2.9

OPEN CIRCUIT-OUTPUT OF HALF-SELECTED SWITCH CORE
(11DCL-2-720H2L-1, SIZE 1D264) FOR VARIOUS EXCITATIONS
BIAS = 9.5 AMP-TURNS. SIZES OF SECOND PULSES RECORDED IN VOLTS

TABLE I

Driving Current (ampere turns)	Peak Open Circuit Half Selected Switch Core Output Voltage (bias = 9.5 amp.turns) 11 DCL - 2 - 720 1D264 3F395	H2L-1 6F395	DCL-3-44 6F397
3.5	0.24	0.43	0.4
4.5	0.37	0.54	0.5
5.5	0.53	0.78	0.7
6.5	0.76	1.0	0.9
7.5	0.99	1.6	1.1
8.5	1.35	1.9	1.5
Peak Resistance of Open Circuit, Half Selected Switch Core	0.2	0.24	0.21
	0.17		

b. The Fully Selected Switch Core

It has been pointed out that the relationship between the net field strength, H_{net}, and the switching time of the core, τ, is

$$H_{net}\,\tau = Sw \tag{2.6}$$

where Sw is a constant of the core material.

The core that is to be discussed is shown in Fig. 2.5 and its hysteresis loop is drawn in Fig. 2.6. If the core saturates reasonably well, the flux switched ϕ_s, when the core is fully selected is virtually independent of the driving current. The shape of the voltage output pulse is generally independent of the driving current (provided that it is driven hard enough); it somewhat resembles a half sine wave. The expected output voltage waves, plotted against time,

for various driving currents are shown in Fig. 2.10. Fig. 2.11 shows the actual output pulses of a 11DCL-2-720H2L-1, size 1D264 switch core. The results are tabulated in Table II, for this and other cores, and are plotted in Figs. 2.14, 2.15, 2.16, and 2.17

TABLE II

Peak Open Circuit, Fully Selected, Switch Core Output Voltage (bias = 9.5 amp. turns)

Driving Current (ampere turns)	11 DCL - 2 - 720 H2L-1			DCL-3-44
	1D264	3F395	6F395	6F397
10		1.5	3.4	
11	2.7	3.3	6.0	
12	3.6	4.3	8.0	2.2
13	5.2	6.0	10.4	3.4
14	6.9	7.6	12.2	4.5
15	8.4	8.6	13.8	5.6
16	9.3	9.2	14.2	6.1
17	10.4	10.0	15.2	7.5
Peak Resistance of Open Circuit, Fully Selected Switch Core	1.3	1.5	2.2	1.1

The area under each voltage time curve must equal the switches flux, ϕ_s. This requires that the product

$$\frac{V_{out}}{N_2} \tau = a \phi_s \qquad (2.7)$$

where a is a constant of proportionately, and V_{out} is the peak output voltage.

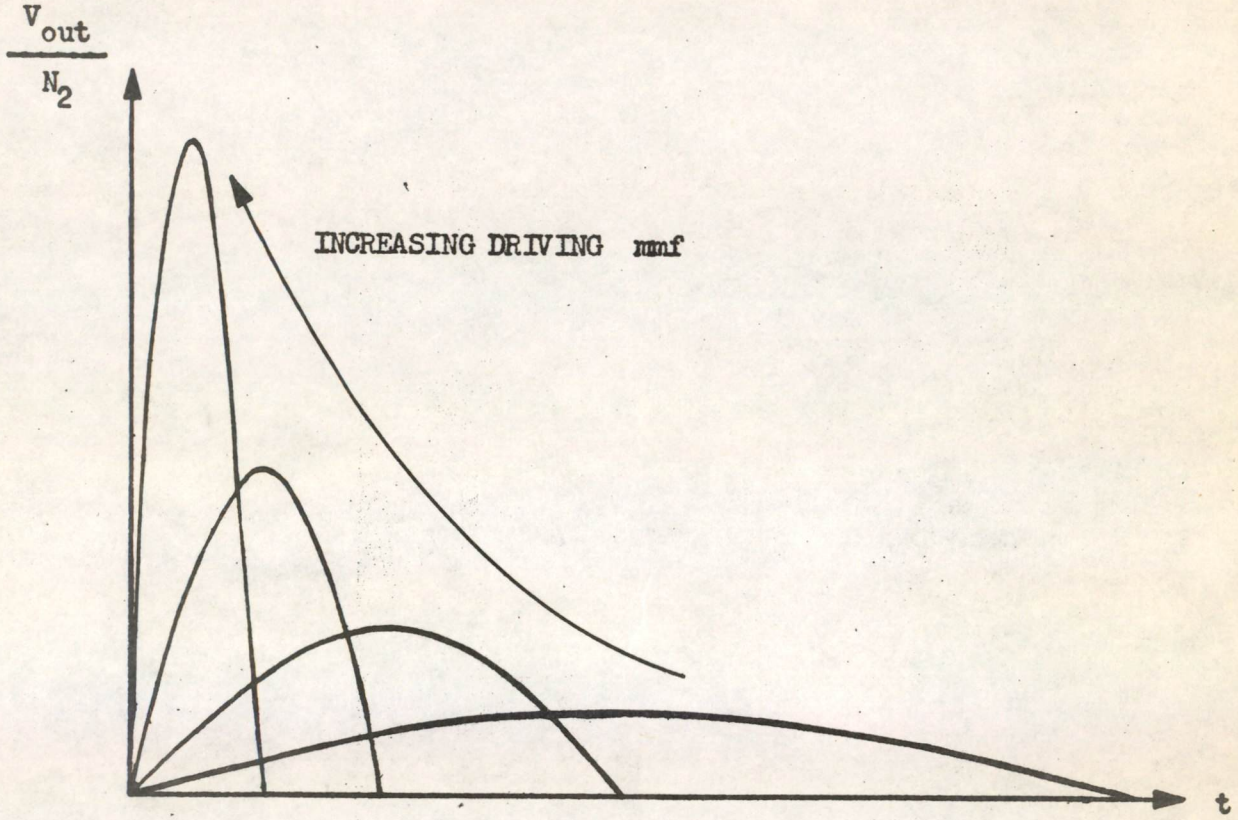
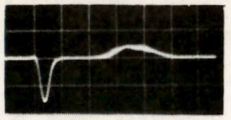
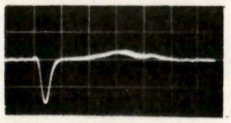


FIG. 2.10

IDEALIZED VOLTAGE OUTPUTS OF SWITCH CORES
AS A FUNCTION OF TIME FOR VARIOUS EXCITATIONS

	DRIVING EXCITATION (AMPERE-TURNS)	VOLTAGE OUTPUT (VOLTS)
	17.0	10.4
	16.0	9.3
	15.0	8.4
	14.0	6.9
	13.0	5.2
	12.0	3.6
	11.0	2.7
	10.0	DOES NOT SWITCH

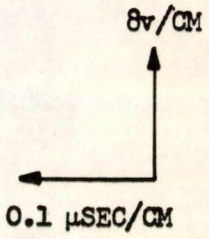


FIG. 2.11

OPEN CIRCUIT OUTPUTS OF FULLY SELECTED SWITCH CORES
(11DCL-2-720H2L-1, SIZE 1D264) FOR VARIOUS EXCITATIONS
BIAS = 9.5 AMP-TURNS SIZE OF FIRST PULSE RECORDED IN VOLTS

Furthermore, H_{net} (= H drive - H coercive) is directly proportional to the net current, I net (= I drive - I coercive), driving the core. The equation used to relate H and i is

$$H = \frac{0.4\ N_1\ i}{\bar{d}} \qquad (2.8)$$

in which N_1 is the number of primary turns on the core and $\bar{d} = \frac{O.D. - I.D.}{I_n(O.D./I.D.)}$, where O.D. is the outside diameter of the core, and I.D. is its inside diameter.

If equations (2.7) and(2.8) are substituted into equation (2.6), the result is

$$V_{out} = \frac{.4a\ N_1 N_2\ \phi_s}{\bar{d}\ Sw}\ I_{net}$$

$$= \frac{.4a\ \phi_s}{\bar{d}\ Sw}\ N_1 N_2\ (I_{in} - I_Z - I_C)$$

$$= z\ N_1\ N_2\ (I_{in} - I_Z - I_C) \qquad (2.9)$$

The constant z has the dimension ohms per turns squared. It is a property of the core; it is independent of the manner in which the core is used (so long as the core is switched) and of the number of turns wrapped on the core.

Equation (2.9) expresses the linear relationship between the peak open circuit secondary voltage, V_{out} and the drive current, I_{in}, when the core is switched.

If this output of the core of Fig. 2.5 is short-circuited, then the net ampere turns through it, when switching, must be $N_1 I_C$. This requires that

$$N_1(I_{in} - I_Z) - N_2 I_2 = N_1 I_C$$

or

$$I_2 = \frac{N_1}{N_2} (I_{in} - I_Z - I_C) \tag{2.10}$$

where I_2 is the short circuit current flowing in the secondary. Thevinin's Theorem may be applied to equation (2.9) and (2.10) to leading to the output impedance of the core,

$$Z_{out} = \frac{V_{out}}{I_2} = N_2^2 z \tag{2.11}$$

The leakage inductances appear in this equivalent circuit in the same way that they appeared in the equivalent circuit of the half-selected core. (See Appendix A and Fig. 2.7). The equivalent circuit of the fully selected switch core is shown in Fig. 2.12.

c. The Combined Switch Core Characteristics

The similarity between the Revised Equivalent Circuit of Half Selected Switch Core (Fig. 2.8) and the Equivalent Circuit of Fully Selected Switch Core (Fig. 2.12) is evident.

If a current source drive is assumed, the leakage inductance L_{L_1}, may be neglected. The equivalent circuits can then be redrawn as in Fig. 2.13.

The data of Tables I and II are plotted, and the graphs of Fig. 2.14, 2.15, 2.16, and 2.17 are the results.

The departures from linearity of these curves at large driving currents are not properties of the cores, but are due to the core drivers. When the driving currents are exceedingly large, the cores switch during the current rise times. Because it is quite difficult to determine what the actual current exciting the core is, during switching, the easiest way out was taken - the driving current was assumed to be the

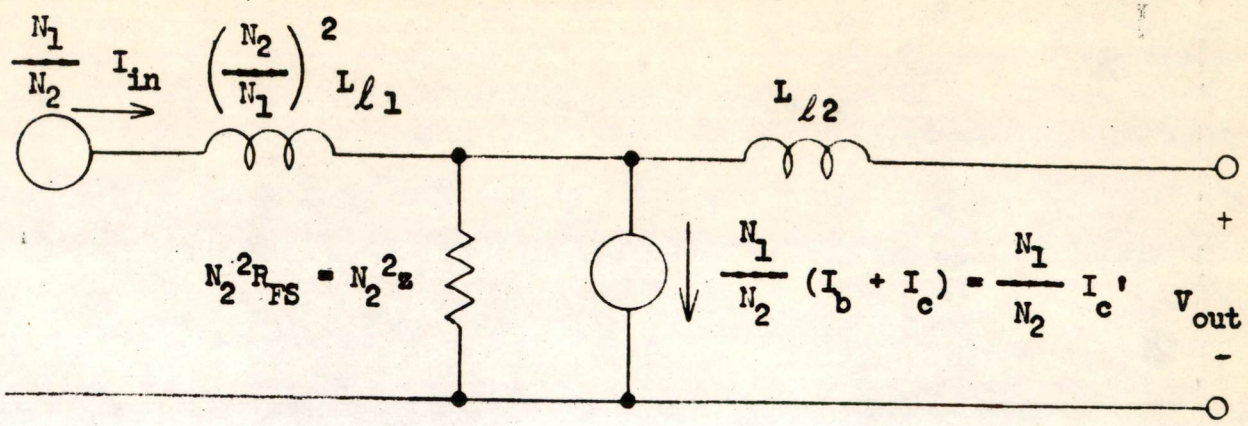
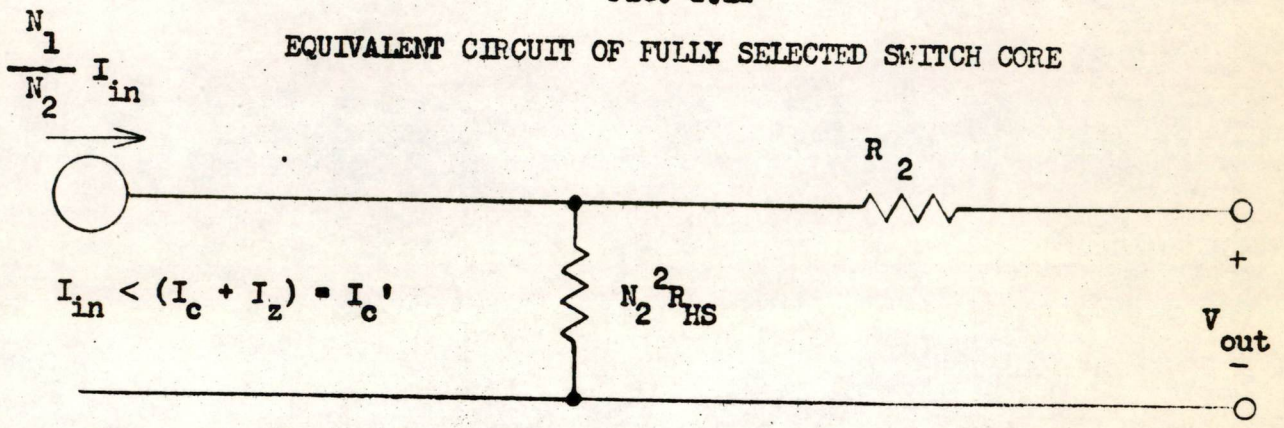
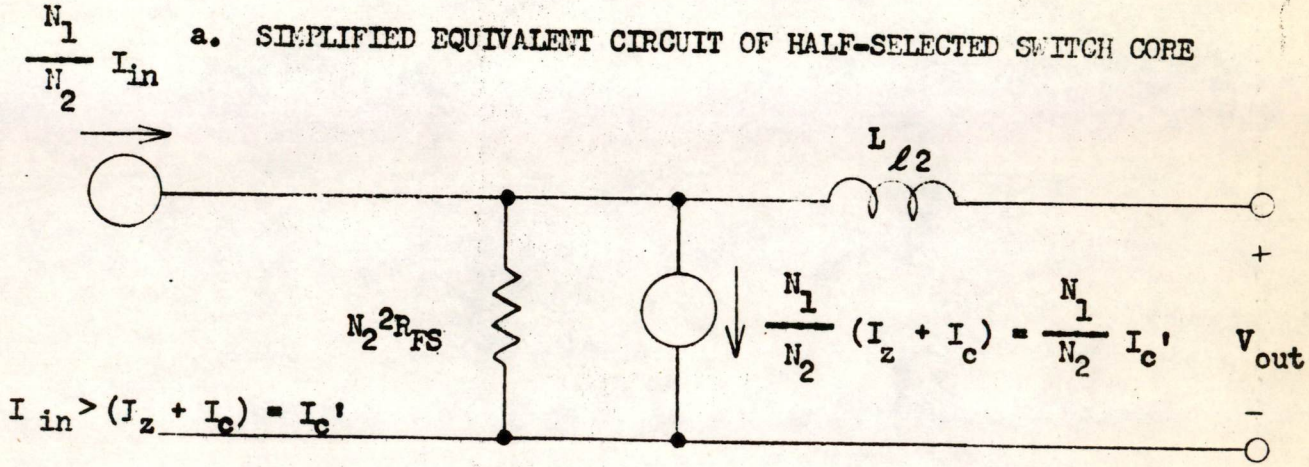


FIG. 2.12

EQUIVALENT CIRCUIT OF FULLY SELECTED SWITCH CORE



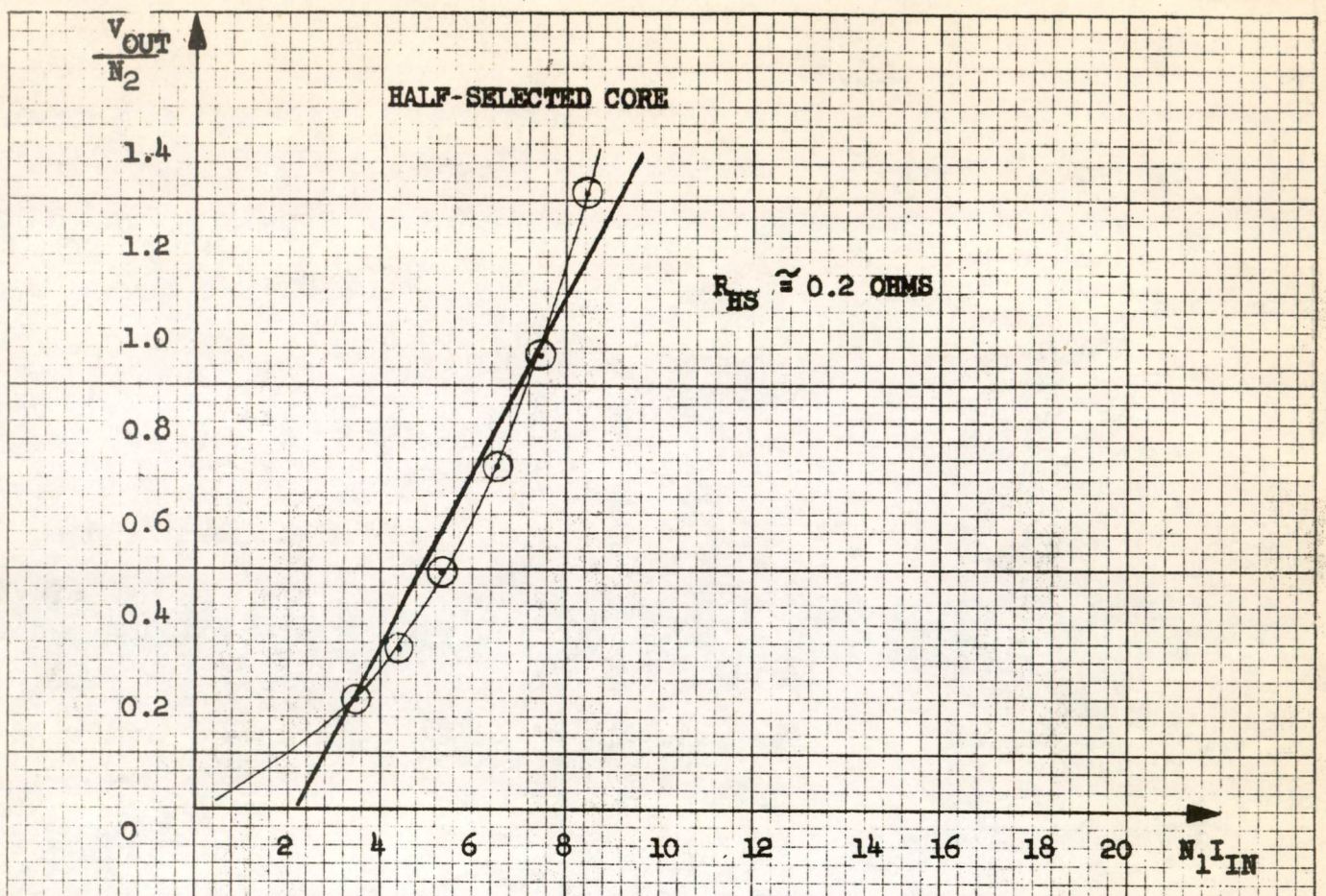
a. SIMPLIFIED EQUIVALENT CIRCUIT OF HALF-SELECTED SWITCH CORE



b. SIMPLIFIED EQUIVALENT CIRCUIT OF FULLY SELECTED SWITCH CORE

FIG. 2.13

SIMPLIFIED SWITCH CORE EQUIVALENT CIRCUITS
(I_{in} IS CONSIDERED TO BE EITHER THE X OR Y DRIVE OR BOTH; THE BIAS IS CONSIDERED TO BE A PART OF THE COERCIVE FORCE)



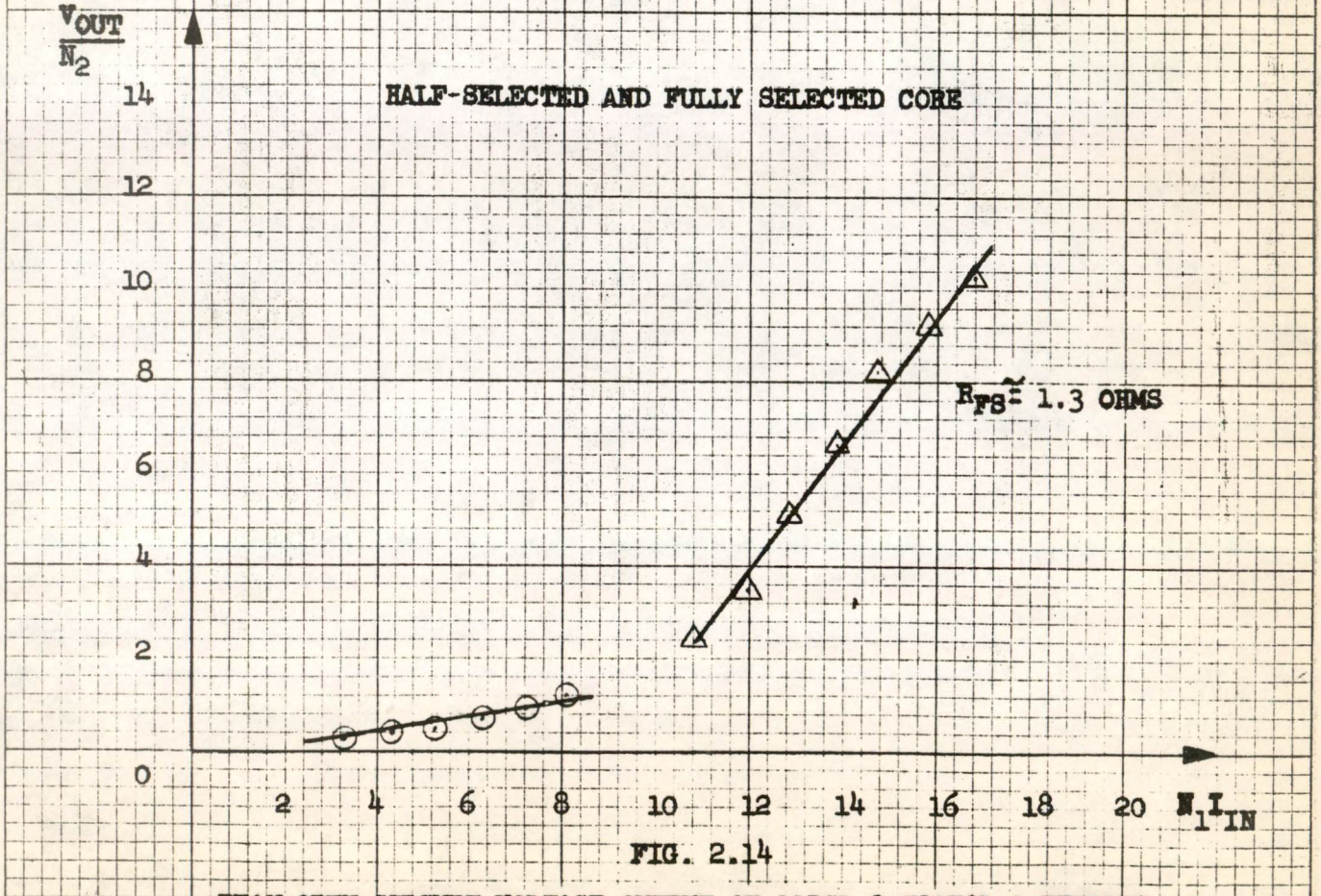


FIG. 2.14

PEAK OPEN CIRCUIT VOLTAGE OUTPUT OF 11DCL-2-720H2L-1 FERRITE SWITCH CORE (SIZE 1D264) VERSUS EXCITATION, BIAS = 9.5 AMP. TURNS

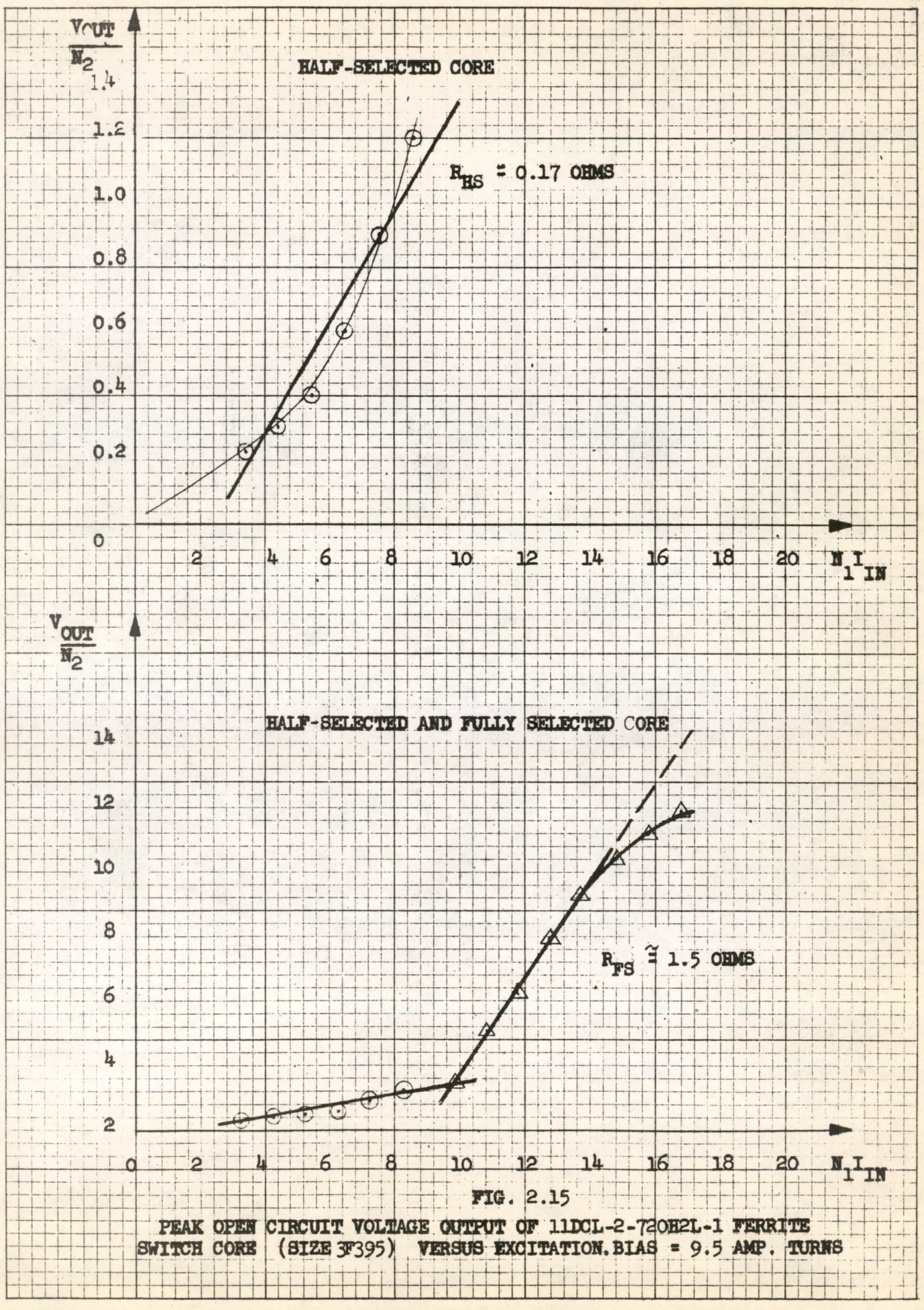


FIG. 2.15

PEAK OPEN CIRCUIT VOLTAGE OUTPUT OF 11DCL-2-720H2L-1 FERRITE SWITCH CORE (SIZE 3F395) VERSUS EXCITATION. BIAS = 9.5 AMP. TURNS

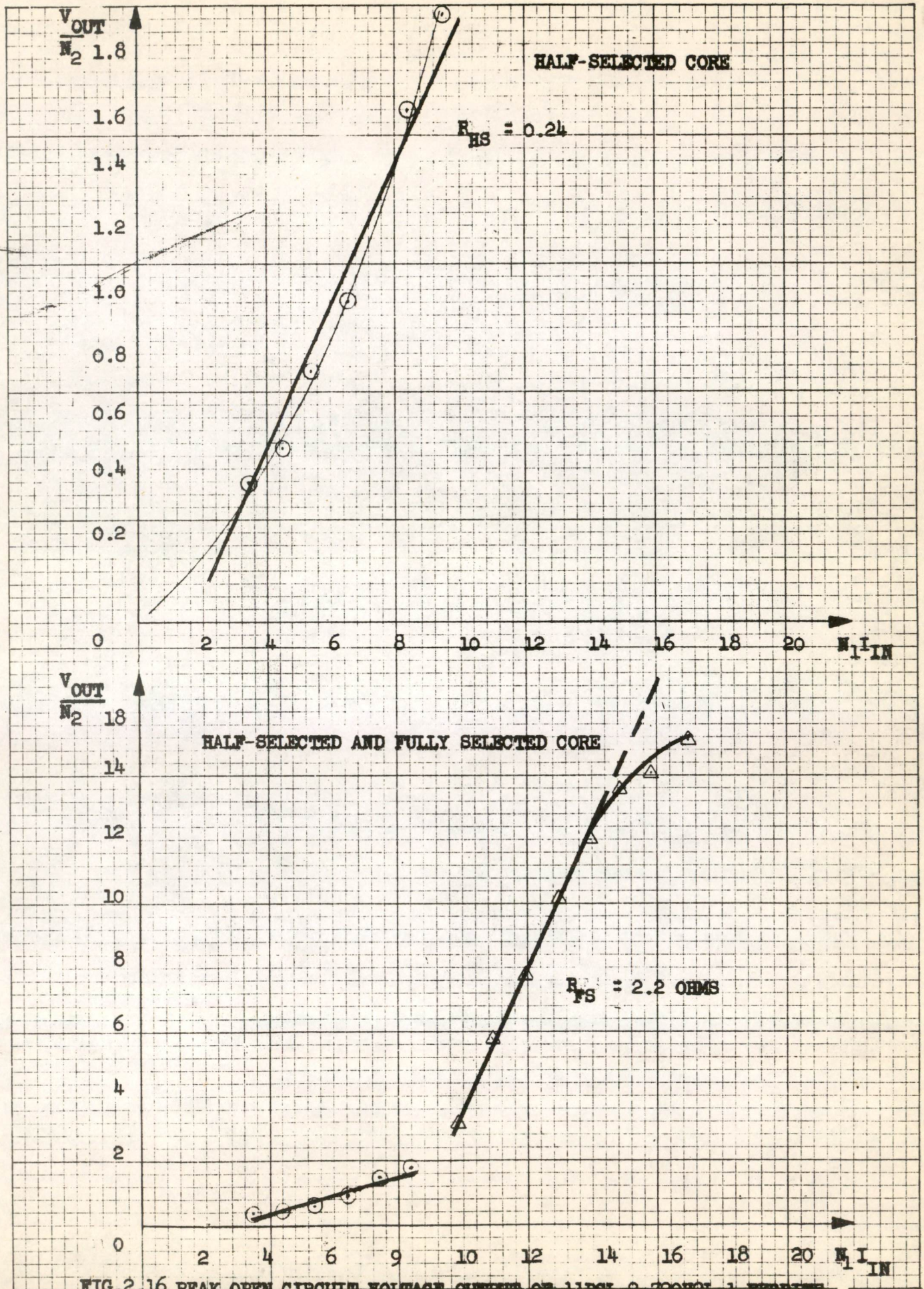


FIG. 2.16 PEAK OPEN CIRCUIT VOLTAGE OUTPUT OF 11DCL-2-720H2L-1 FERRITE SWITCH CORE (SIZE 6F395) VERSUS EXCITATION, BIAS 9.5 AMP. TURNS

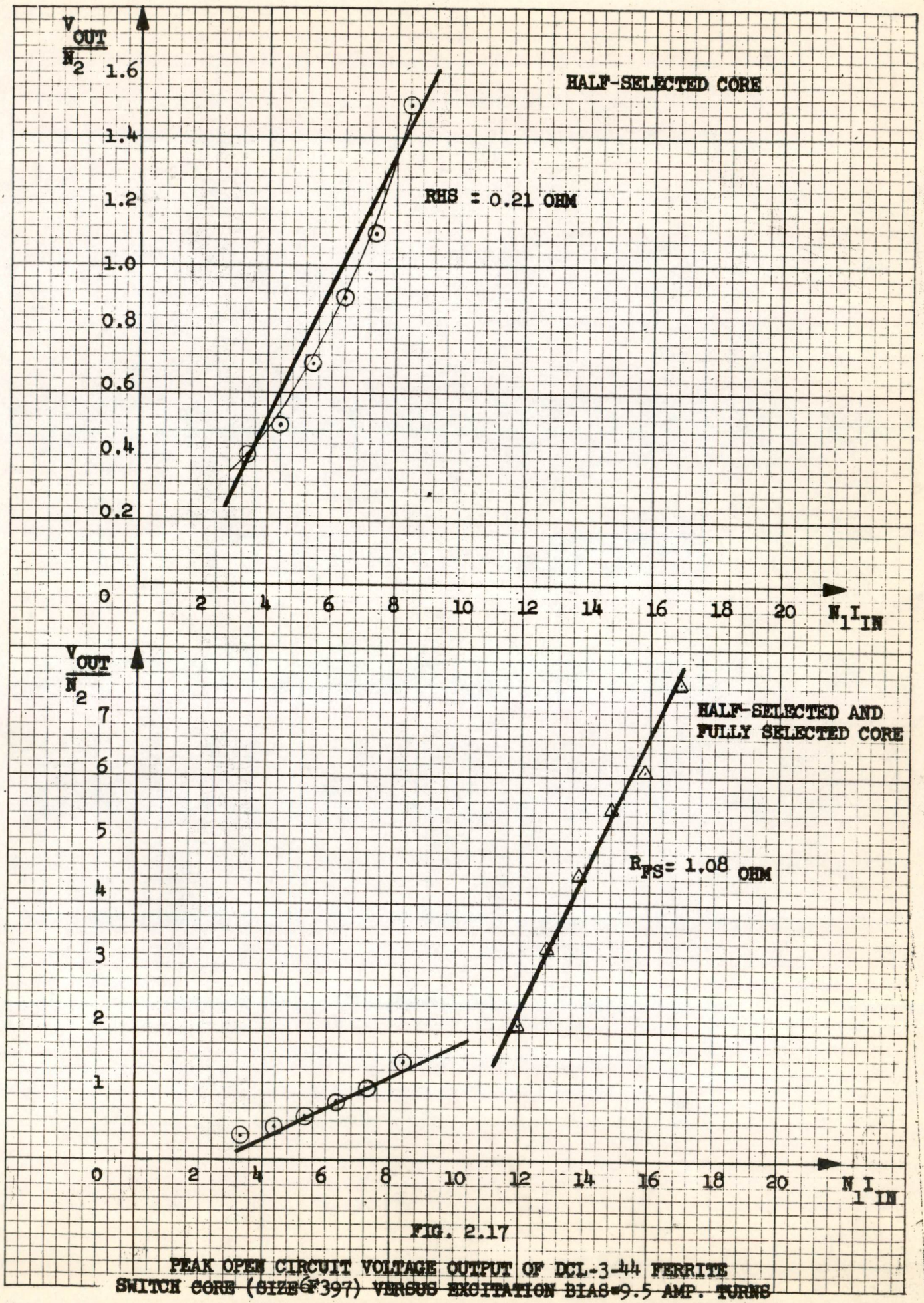


FIG. 2.17

PEAK OPEN CIRCUIT VOLTAGE OUTPUT OF DCL-3-44 FERRITE SWITCH CORE (SIZE 397) VERSUS EXCITATION BIAS=9.5 AMP. TURNS

final value of the current output. The result is that the actual excitation of the core, during switching, is somewhat less than what is indicated. The broken line indicates what the expected curves should look like.

Figure 2.23 idealizes the above results and gives a piece-wise linear characteristic which can be dealt with analytically for the purpose of performing computations in order to predict the operation of the three core per bit memory unit.

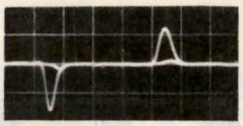
Figure 2.18 illustrates the fact that the open circuit switch core outputs are independent of the length of time that the core sets in one state, provided that the core is allowed to complete its switching in one direction before it is switched back.

B. The Memory Core

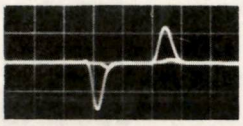
The idealized memory core has the hysteresis loop shown in Fig. 2.19. Figure 2.20 shows a more realistic core loop. Figures 2.3b and 2.3c show the loop of the memory core actually used in this thesis investigation.

The operating characteristics of the memory core are essentially the same as those of the switch cores. The equivalent circuits for the memory core are the same as those for the switch core (Fig. 2.7 or Fig. 2.8 for the Half Selected Core, and Fig. 2.12 for the Fully Selected Core). The difference in operation results from the fact that a memory core is not permitted any bias and so, $I_Z = 0$. The result is that I_c' of Fig. 2.12 is merely I_c of the core in question. Figure 2.21 shows output voltages obtained when the memory held ONEs and was driven by various currents. (It is to be noted that a bias was applied to the core in order to determine information concerning the core in the partially selected state. The core was driven as if it were a switch

ON TIME
MICROSECONDS



0.5



0.3

0.2

0.15

FULL SELECTS = 9.6 VOLTS
HALF SELECTS = 0.8 VOLTS

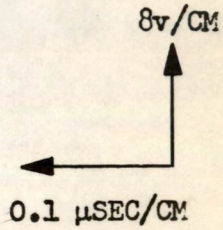


FIG. 2.18

OPEN CIRCUIT OUTPUT OF FULLY SELECTED SWITCH CORE
11DCL-2-720H2L-1, SIZE 1D264 FOR VARIOUS LENGTHS OF ON TIME
EXCITATION REMAINS FIXED. BIAS = 9.5 AMP-TURNS. DRIVE = 17.0 AMP-TURNS

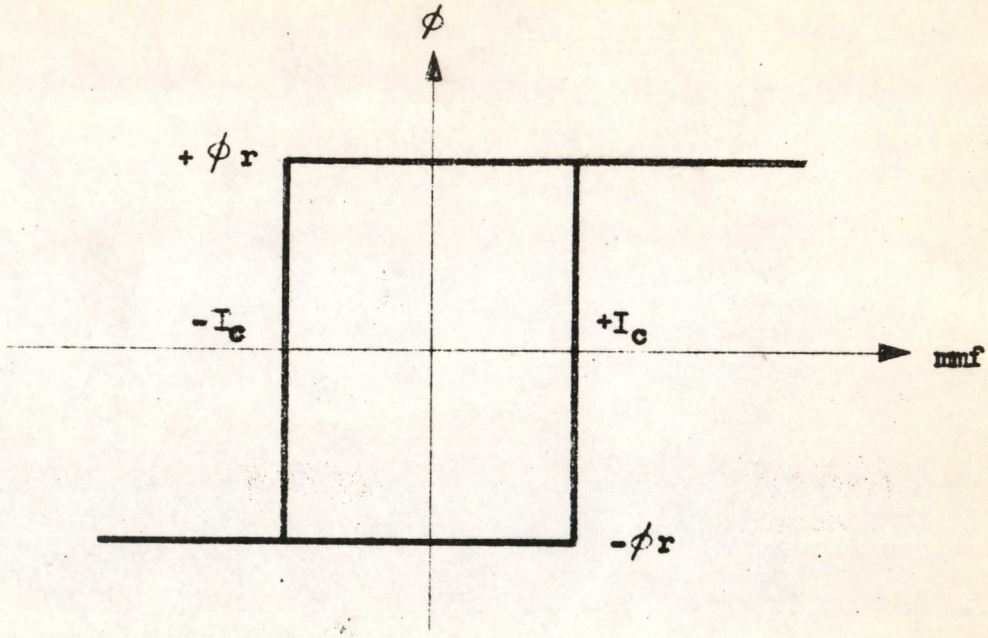


FIG. 2.19

IDEALIZED MEMORY CORE HYSTERESIS LOOP

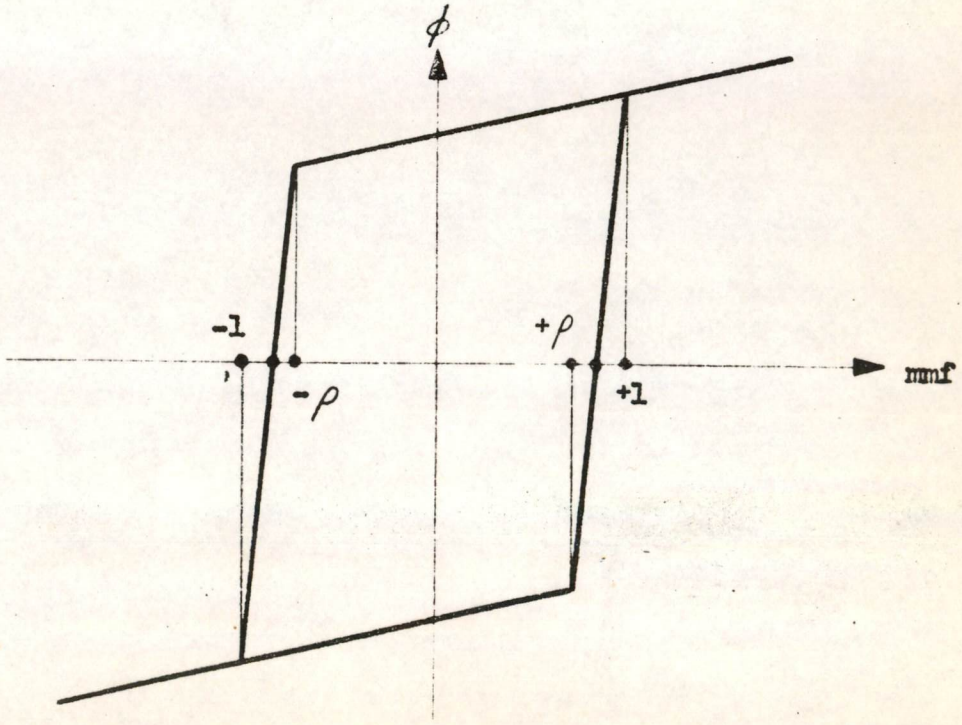


FIG. 2.20

HYSTERESIS LOOP OF MORE REALISTIC MEMORY CORE

	DRIVING EXCITATION (AMPERE-TURNS)	VOLTAGE OUTPUT (VOLTS)
	8.5	0.47
	7.5	0.39
	6.5	0.30
	5.5	0.23
	4.5	0.16
	3.5	0.10

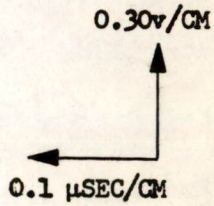
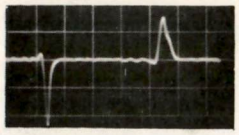
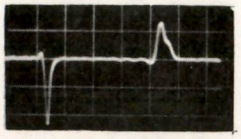
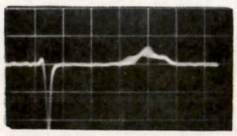
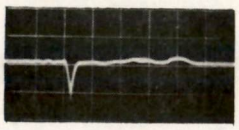


FIG. 2.21a

OPEN CIRCUIT OUTPUT OF HALF-SELECTED MEMORY CORE
(11DCL-2-720H2L-1 SIZE 1F395) OPERATED AS A SWITCH CORE FOR VARIOUS EXCITATIONS
BIAS = 9.5 AMP-TURNS. SIZE OF SECOND PULSE IS RECORDED

	DRIVING EXCITATION (AMPERE-TURNS)	VOLTAGE OUTPUT (VOLTS)
	17.0	3.1
	16.0	2.5
	15.0	2.3
	14.0	1.7
	13.0	1.2
	12.0	0.5
	11.0	DOES NOT SWITCH

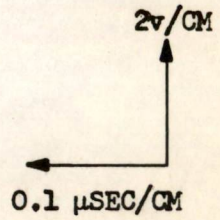


FIG. 2.21b

OPEN CIRCUIT OUTPUT OF FULLY SELECTED MEMORY CORE (11DCL-2-720H2L-1, SIZE 1F395) OPERATED AS SWITCH CORE FOR VARIOUS EXCITATIONS. BIAS = 9.5 AMP-TURNS. SIZE OF FIRST PULSE IS RECORDED

core). This data is presented in Table III, and plotted in Fig. 2.22. Figure 2.24 shows the linearized characteristic with the bias removed. No data was taken for the operation of the memory core holding a ZERO in these tests. In line with the other linearized assumptions made, it is assumed that the volt-ampere characteristic of a memory core holding a ZERO is merely a continuation of the half-selected characteristic.

TABLE III

Driving Current (ampere turns)	Peak Open Circuit Memory Core Output Voltage (operated as Switch Core) bias = 9.5 amp-turns 11 DCL - 2 - 720 H2L-1 1F395
Half Selects	
3.5	0.10
4.5	0.16
5.5	0.23
6.5	0.30
7.5	0.39
8.5	0.47
Peak Resistance of Open Circuit, Half Selected Memory Cores	0.074 Ω
Full Selects (core holds ONE)	
12	0.5
13	1.2
14	1.7
15	2.3
16	2.5
17	3.1
Peak Resistance of Open Circuit, Fully Selected Memory Cores (for ONE)	0.52 Ω

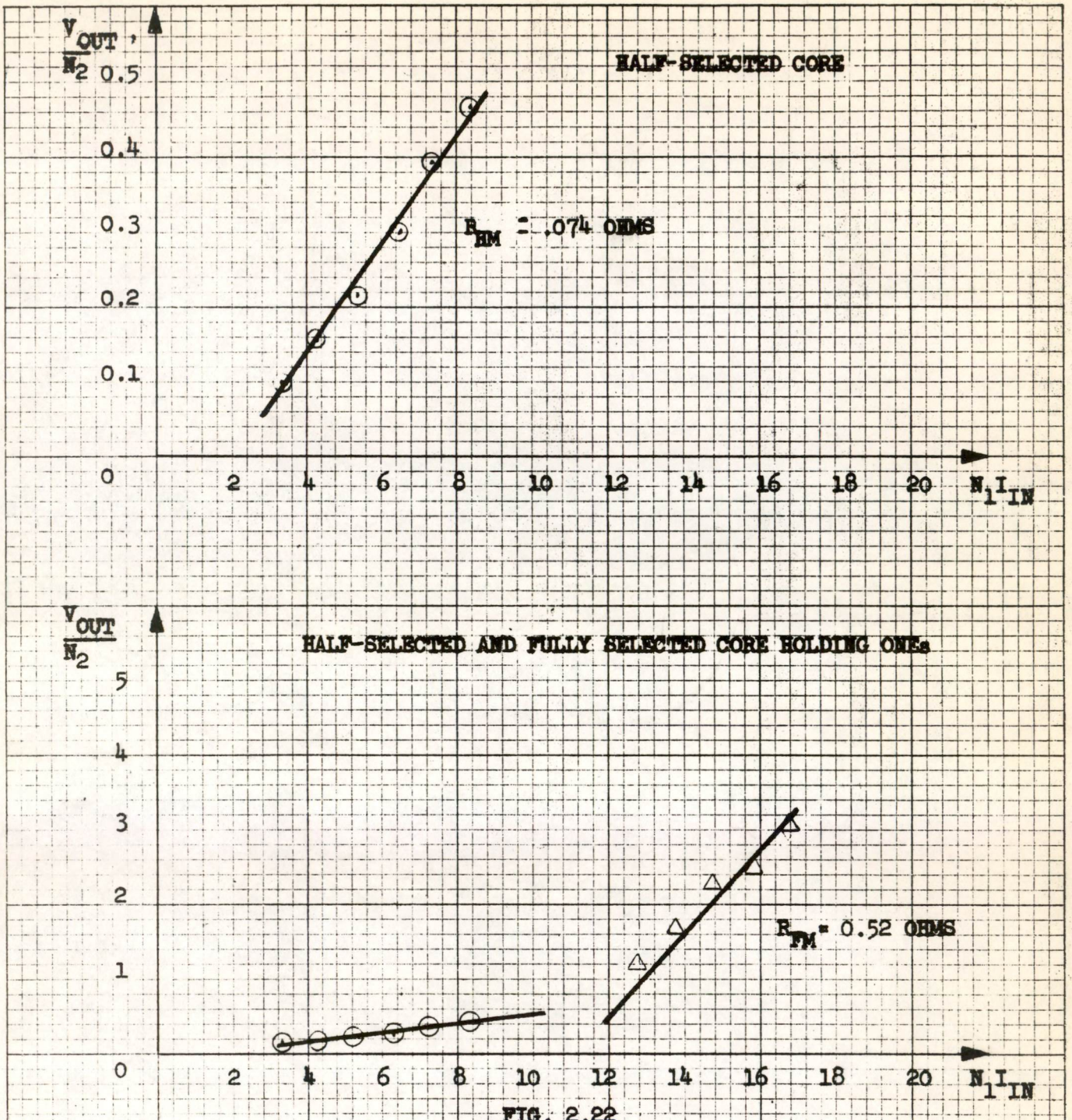


FIG. 2.22

PEAK OPEN CIRCUIT VOLTAGE OUTPUT OF 11DCL-2-72OH2L-1 FERRITE MEMORY CORE (SIZE 1F395) TESTED AS SWITCH CORE BIAS = 9.5 AMP. TURNS VERSUS EXCITATION

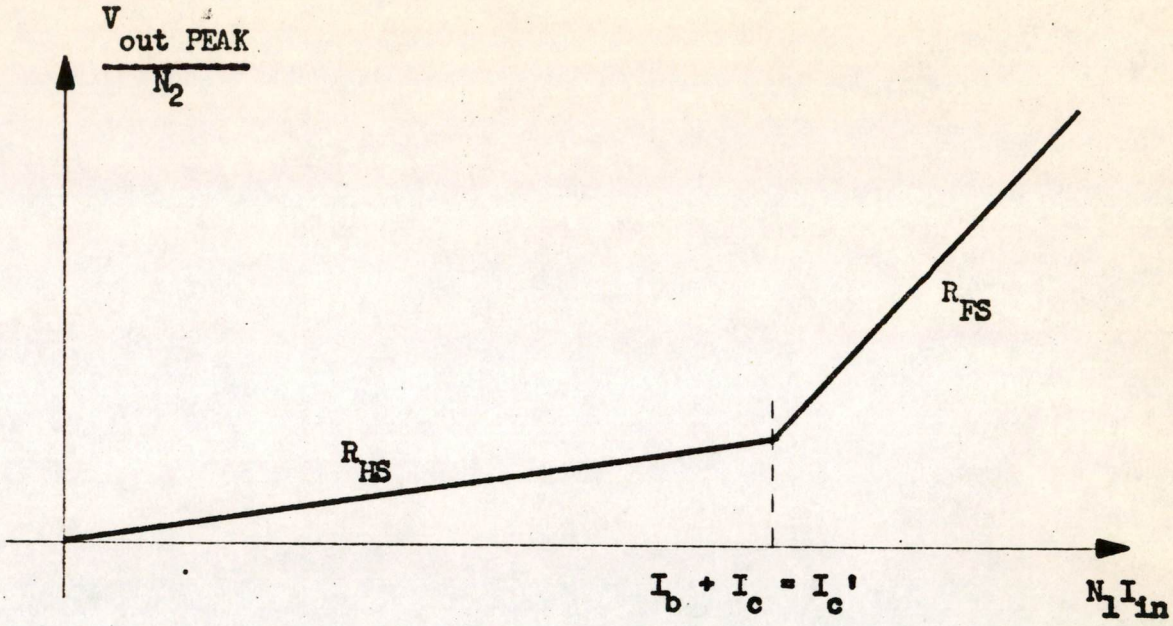


FIG. 2.23

LINEARIZED IDEALIZATION OF OPEN CIRCUIT SWITCH CORE CHARACTERISTICS

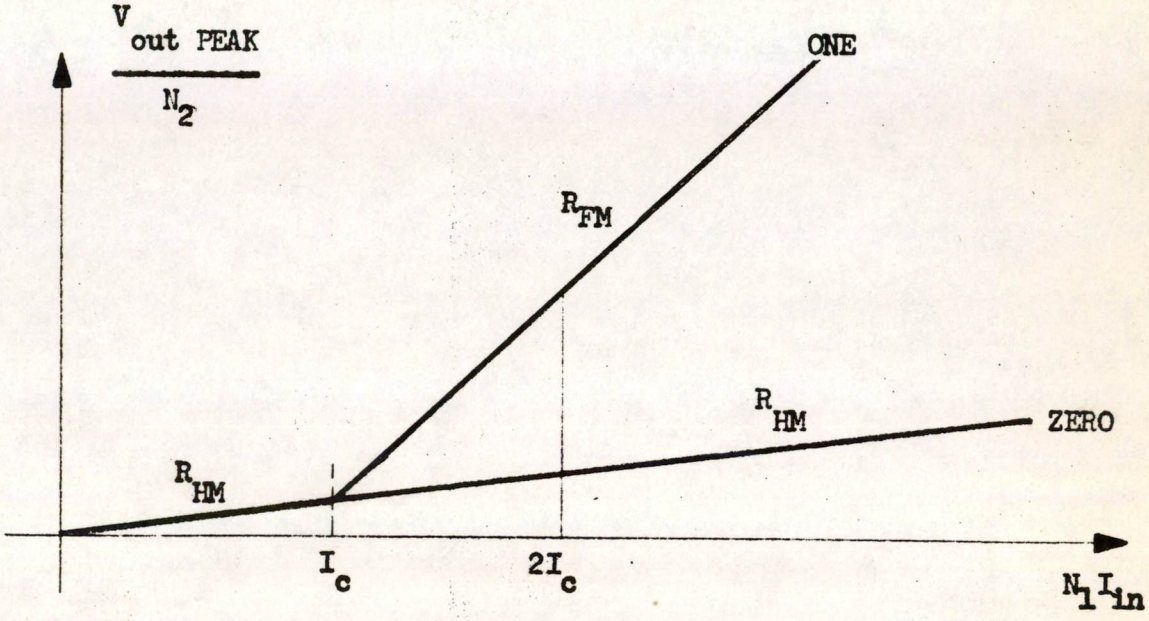


FIG. 2.24

LINEARIZED IDEALIZATION OF MEMORY CORE CHARACTERISTICS

The selection ratio (R) is defined as the excitation applied to a selected core divided by the maximum excitation applied to any unselected core. R. S. DiNolfo[9] has shown that if an n dimensional selection scheme is employed, that

$$R_{max} = \frac{1}{P_{min}} = \frac{n+1}{n-1} \qquad (2.12)$$

The smaller the p of the core is (i.e. - the poorer the core is, Fig. 2.20), the larger the selection ratio must be. But, R_{max} is limited by the number of dimensions used.

The coincident-current memory has a two-dimensional read (X and Y) and a three-dimensional write (X, Y, and Z). In order to obtain symmetrical operation, it is necessary to employ the same excitations during the read and write operations, and so the system is used as if it were three-dimensional. Thus, $R_{max} = 2$, and $P_{min} = 1/2$. As has been pointed out in Chapter 1, this fact limits the allowable excitation applied to the core.

A large amount of information can be obtained from Fig. 2.24. The maximum half-select current in the coincident-current memory scheme is I_c. The result is that the maximum full-select current is $2I_c$. Utilizing Fig. 2.24 and the computations in Appendix C, the following results are obtained:

$$V_{out\ half\text{-}select} = R_{HM}I_c \qquad (2.13)$$

$$V_{out\ ZERO} = 2\,R_{HM}I_c \qquad (2.14)$$

$$V_{out\ ONE} = (R_{HM} + R_{FM})I_c \qquad (2.15)$$

It is necessary that the ONE to ZERO, and ONE to half-select ratios be as large as possible. These ratios are:

$$\frac{V_{out\ ONE}}{V_{out\ ZERO}} = \frac{R_{HM} + R_{FM}}{2\ R_{HM}} = 1/2(1 + \frac{R_{FM}}{R_{HM}})$$

$$= 1/2(1 + \mu), \qquad (2.16)$$

and

$$\frac{V_{out\ ONE}}{V_{out\ half\text{-}select}} = \frac{R_{HM} + R_{FM}}{R_{HM}} = 1 + \frac{R_{FM}}{R_{HM}} = 1 + \mu \qquad (2.17)$$

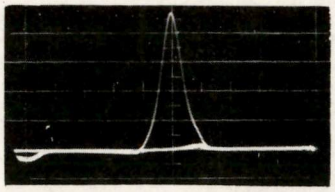
The factor μ is the ratio of the incremental full selected memory core peak resistance to the incremental half selected peak resistance. It is desirable to use cores in which μ is as large as possible. In order to obtain maximum discrimination between wanted and unwanted signals.

The outputs of 50 MTC memory cores (General Ceramics S-1, Lot E-85) driven with coincident current excitation are shown in Fig. 2.25. This picture shows the size of ONEs compared to ZERO and half selects.

The sizes of the outputs are tabulated below.

TABLE IV

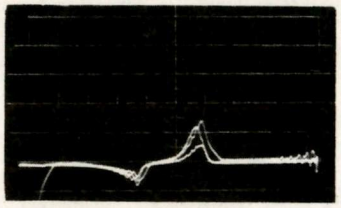
	Voltage Output From 50 Cores	Voltage Output Per Core	Ratio of ONE to —
ONE	7.0	0.140	
ZERO	0.26	0.0052	27
Half Select ONE	0.24	0.0048	29
Half Select ZERO	0.12	0.0024	58



1.5v/CM

0.5 μSEC/CM

FULL SELECT AND
HALF SELECT ONES
AND ZEROS SUPERIMPOSED



0.2v/CM

0.5 μSEC/CM

HALF SELECT ONE AND ZERO
AND FULL SELECT ZERO
SUPERIMPOSED

FULL SELECT ONE = 7.0 VOLTS
FULL SELECT ZERO = 0.26 VOLTS
HALF SELECT ONE = 0.24 VOLTS
HALF SELECT ZERO = 0.12 VOLTS

FIG. 2.25

VOLTAGE OUTPUTS FROM COINCIDENT CURRENT TYPE SELECTION.
50 GENERAL CERAMICS MEMORY CORES NO BIAS
HALF SELECT EXCITATION = 0.410 AMP-TURNS

The complete cycle is not shown, but it requires about 6 microseconds to completely read and write. About 1 microsecond is require to switch the core completely.

A one-dimensional read and write would remove all restrictions on the allowable drive and would, incidentally, eliminate partial select noises. The necessary core characteristics could be relatively slack — p could approach zero. The operating speed could be made extremely rapid, limited merely by how hard the selected cores were driven. The factor μ introduced would be of no interest.

In its essence, the three-core-per-bit memory unit described in Chapter 3 is a one-dimensional memory. Actually, it does not quite achieve this mark because of noise outputs from partially selected switch cores.

CHAPTER 3

THE THREE-CORE-PER-BIT MEMORY

The memory unit utilizing two switch cores and one memory core per bit of information that has been proposed by J. Raffel[6] will be discussed in this chapter.

The cores employed are those described in Chapter 2. The basic, simplified, memory unit is shown in Fig. 3.1. The current pictured driving switch core A ($I_{in\ a}$) is actually composed of the X_a and Y_a drives superimposed on the bias. The current driving core B ($I_{in\ b}$) consists of the X_b and Y_b and bias excitations; in addition an inhibit pulse may or may not be applied.

A. The Operation of the Cycle

The operation of the system may be explained by referring to the hysteresis loops of the cores (Fig. 3.2) and to the pulse sequences (Fig. 3.3).

At the beginning of the cycle the only current flowing through core A is the bias, I_{za}, and the core is at the point za on its hysteresis loop (Fig. 3.2). At the time t_1, I_{Xa} and I_{Ya} are applied, and the result is that core A switches from Z_a to $Z_a + X_a + Y_a$. The output voltage of this core induces a large pulse of current in loop A and core M is driven to point $\propto$ on its hysteresis loop. When the current pulse dies away, core M rests at the ZERO point. If the memory core had originally held a ZERO, its voltage output would have been relatively small because of the small flux change. However, if the core previously held a ONE, a large output would be induced on its sense winding. This difference in core outputs provides a ready means for determining the original state

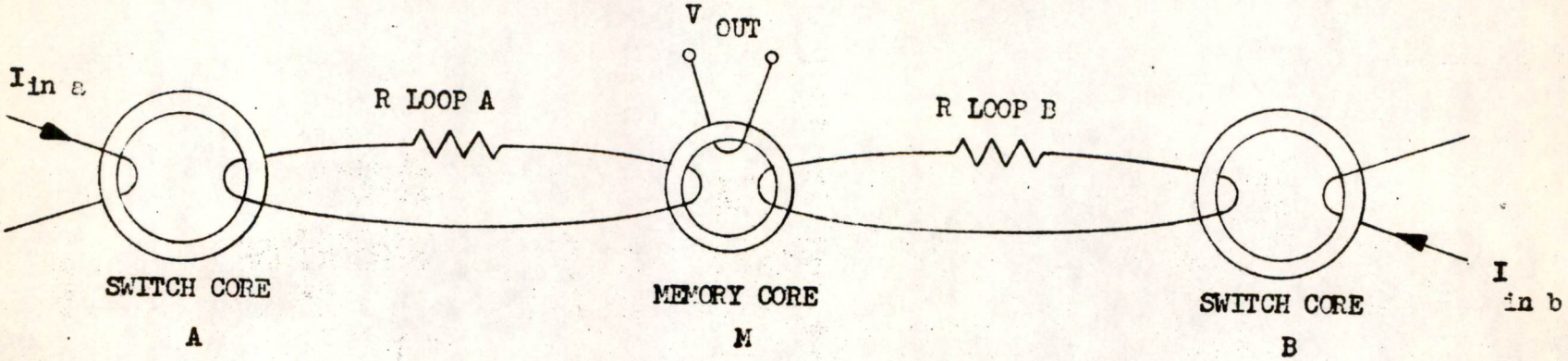


FIG. 3.1

ONE DIGIT OF THE THREE CORE PER BIT MEMORY UNIT, SIMPLIFIED

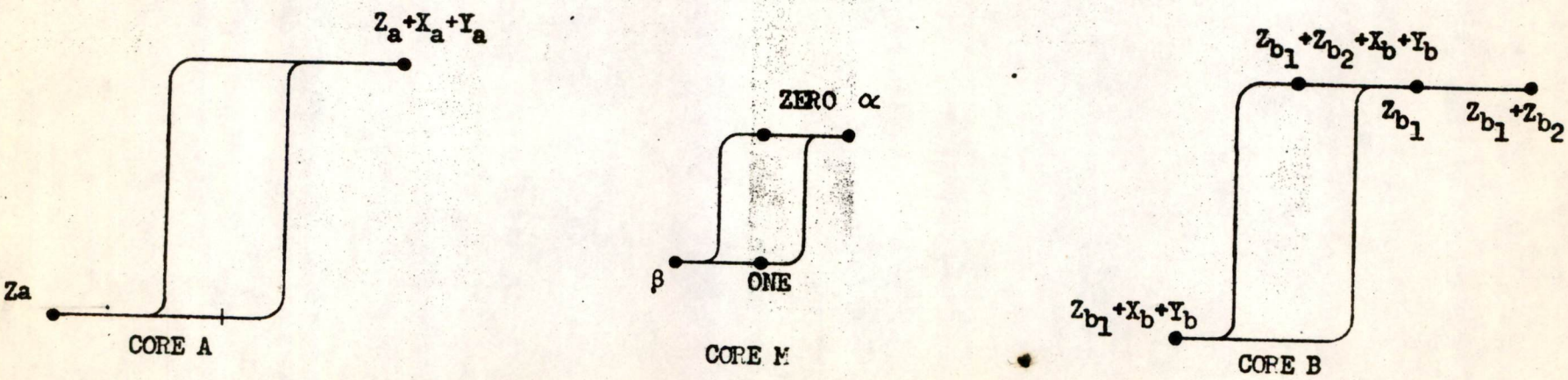


FIG. 3.2

HYSTERESIS LOOPS OF THE CORES IN THE MEMORY UNIT

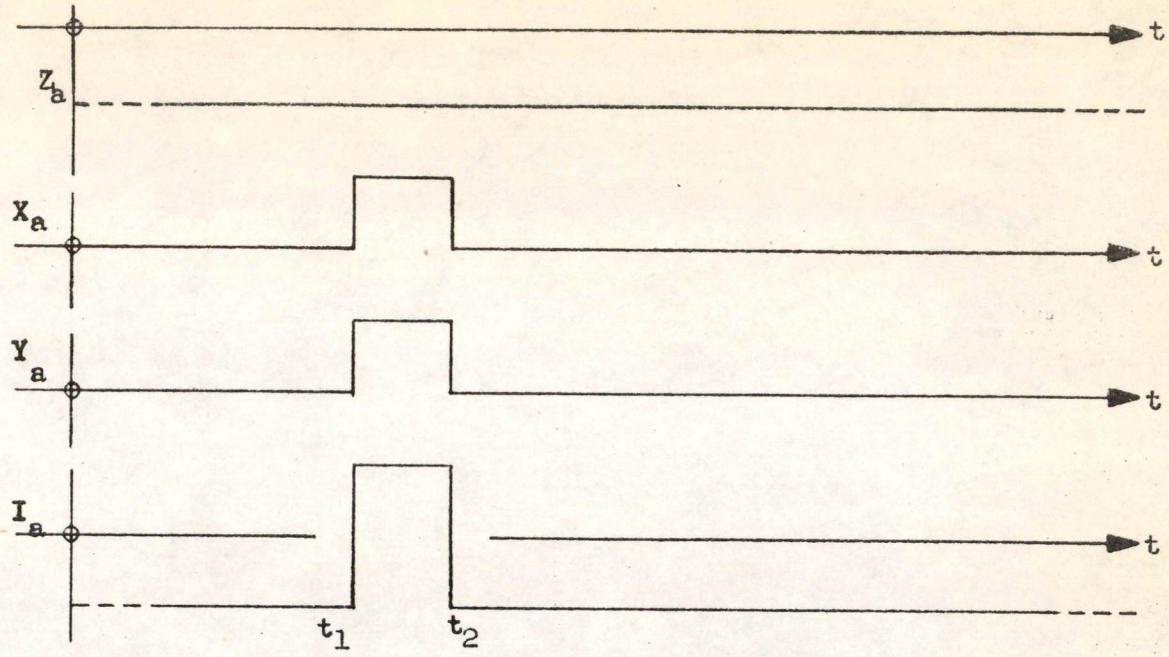


FIG. 3.3a

CURRENT PULSES APPLIED TO SWITCH CORE A, WHEN FULLY SELECTED

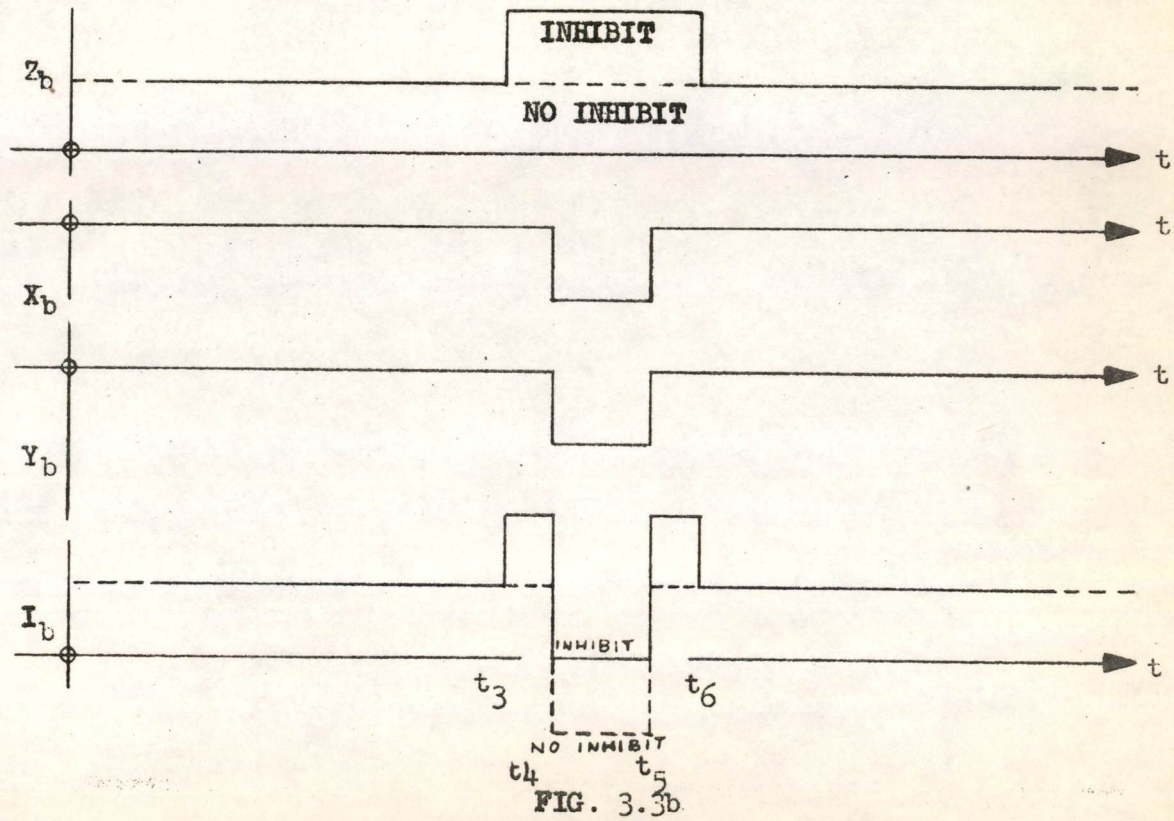


FIG. 3.3b

CURRENT PULSES APPLIED TO SWITCH CORE B, WHEN FULLY SELECTED

ILLUSTRATING THE RESULT OF THE PRESENCE OR ABSENCE OF THE INHIBITING PULSE.

of the core.

At the time t_2, I_{Xa} and I_{Ya} are removed, and core A reverts to point Z_a on its loop. This induces a current in loop A which drags the memory core to point β on its loop, and the memory core eventually settles at point ONE. At the conclusion of the read operation, the memory core is found to repose in the ONE position, regardless of its original information content.

The purpose of the second switch core, B, is to write the required information into the memory core. If it is desired to write a ZERO, it is apparent that core B must be used to move memory core M from the ONE state. On the other hand, the simplest way of writing a ONE, is to prevent this action of core B.

At the beginning of the write cycle only the bias current, I_{Zb_1}, is passed through core B. When a ONE is to be written, an inhibit pulse, I_{Zb_2} is added to I_{Zb_1}. At time t_4, I_{Xb} and I_{Yb} are turned on, but because of the inhibiting current, core B is not switched. Little or no current flows through loop B, with the result that there is little or no disturbance of core M. At t_5, $I_{in\ a} = I_{Xb} + I_{Yb}$ is removed returning core B to point $Z_{b1}+Z_{b2}$ on the magnetization curve. At t_6, the cycle is completed with the return to Z_{b1}. It is to be noted that during the write ONE cycle, core B is merely moved back and forth between $Z_{b1}+Z_{b2}+X_b+Y_b$ and $Z_{b1}+Z_{b2}$. It does not switch. If the noise output from the core is low enough, then the effect on core M is negligible and it is left in the ONE state. It is also important to realize that the inhibiting pulse must start before I_{Xb} and I_{Yb} are turned on and must stay on until after I_{Xb} and I_{Yb} are turned off. If this condition is

not observed, core B will be switched.

A ZERO is written by omitting the inhibit pulse. In this case, the application of I_{Xb} and I_{Yb}, at t_4, switches core B from Z_{b1} to $Z_{b1}+X_b+Y_b$. The resulting current induced in loop B drives core M from ONE to β and when this current subsides, M returns to point ONE. This first pulse out of core B does not really have any effect on core M, provided that the second pulse out of core A has done its job. At t_5, I_{Xb} and I_{Yb} are removed and core B returns to point Z_{b1}. Its output during this time switches core M up to point α, and when all of the currents have decayed to ZERO, core M is left at point ZERO.

B. The Nature of the Coupling Loop

In Chapter 2, the switch and memory cores were described. The remaining basic component of the memory system under investigation is the loop of wire coupling the memory and switch cores.

This wire is mainly inductive, having extremely low resistance. However, when the loop is driven by a core that is switching, it has been found that the loop current rises rapidly and falls slowly. The reasons for this behavior are fairly straightforward. During the loop current rise time, the switch core is a resistance (it varies with time, it is true, but it still is an element which dissipates energy). If an effective value of this resistance is assumed to be R_{rise}, then the linearized time constant is $\tau_{rise} = L_{loop\ rise}/ R_{rise}$ in which R_{rise} is relatively large. After the core has switched, the loop current begins to decay, but in the process of decaying, there is no tendency to switch either core. The result is that there is no large resistance placed in

loop; the cores merely appear to be inductive. The only resistance in the loop (R_{fall}) then, is the incidental loss in the wire, and this is small. It is found, then, that

$$\tau_{fall} = \frac{L_{loop\ fall}}{R_{fall}} > \tau_{rise}. \qquad (3.1)$$

In order to insure proper operation of the memory, it is essential that the current in a loop dies out before a current pulse is sent through the loop in the opposite direction. The result is that the memory may be slowed considerably if the loop current is not able to decay rapidly. The current decay can be speeded by increasing R_{fall}, and this is accomplished by placing a resistor in the coupling loop. If the resistor (henceforth called the loop resistance, R_{loop}) is increased (to about one ohm), the effect on the current rise time, τ_{rise} is small because of the large core resistance already in the circuit, but the decay is speeded greatly. Fig. 3.4 shows the loop currents for the same drive but for different values of loop resistance. Unfortunately, it is not possible to show the loop current when there is no loop resistance, but the first derivative of this current can be shown (by looking across a section of the loop wire, which has little resistance and is essentially inductive). In order to complete the picture, the derivatives of the loop currents are shown for the cases in which $R_{loop} \neq 0$, also.

The pictures of the loop currents and the known values of loop resistance allow the calculation of τ_{fall} in each case, and from this, the loop inductance during the fall time may be computed.

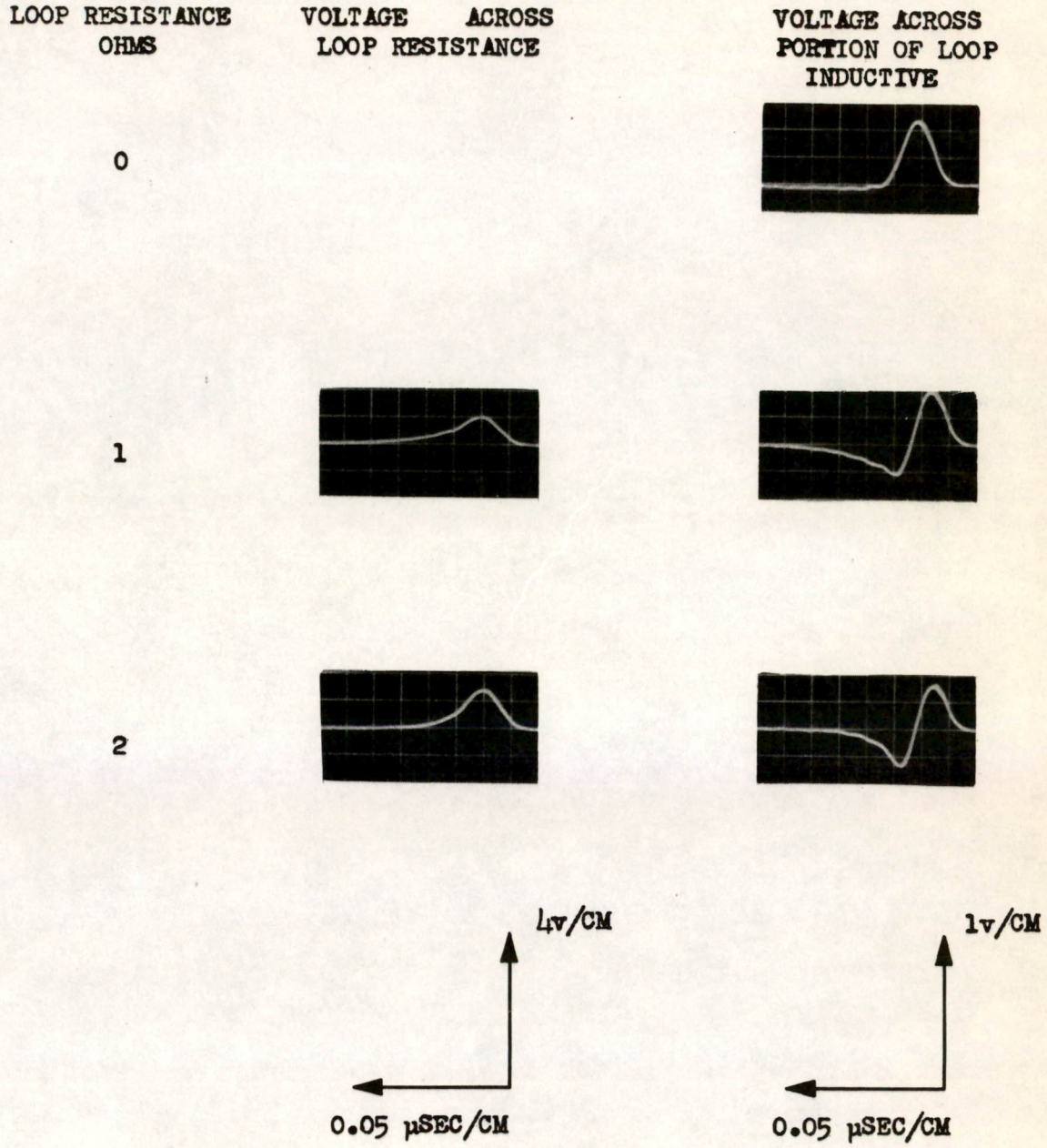


FIG. 3.4

LOOP CURRENTS, AND FIRST TIME DERIVATIVE OF LOOP CURRENTS.
FOR VARIOUS LOOP RESISTANCE VALUES 11DCL-2-720H2L-1 SIZE 1D264
SWITCH CORE DRIVING DUMMY CORE
BIAS = 9.5 AMP-TURNS; EXCITATION = 17.0 AMP-TURNS

TABLE V

Calculation of L_{loop}

R_{loop} (ohms)	Time Required to fall from full current to 1/3 current (microseconds)	$\tau_{fall} = \frac{L_{loop}}{R_{loop}}$ (μsec)	L_{loop} (μhenries)
1	0.10	0.0909	0.09
2	0.06	0.0545	0.11

It has been stated that is it necessary to wait for the first current pulse from a switch to have died away before switching the core a second time, in order to insure proper operation of the memory. The reasons for this will now be demonstrated. If sufficient time is allowed to elapse between the switching of the cores, then the current pulses in the various loops will look like those shown in Fig.3.5. If it is desired to write a ONE in the core, the cycle excludes the pulses from loop B. The first pulse in loop A has completely disappeared by the time the second pulse is applied and so the write operation should be successful. When a ZERO is to be written, the currents shown for loop B are also applied and as these do not interfere with each other, the write operation should be successful in this case, also.

If R_{loop} is too small to do its job properly, or if an attempt is made to run the memory too rapidly, a situation such as that pictured in Fig. 3.6 may occur. When attempting to write a ONE, the first pulse in loop A cycle carries the memory core to the ZERO position; the second pulse may not be large enough to pull the memory core to the ONE position when added to the excitation from core A which has not died out yet. Similarly if a ZERO is to be placed in the memory core, the first

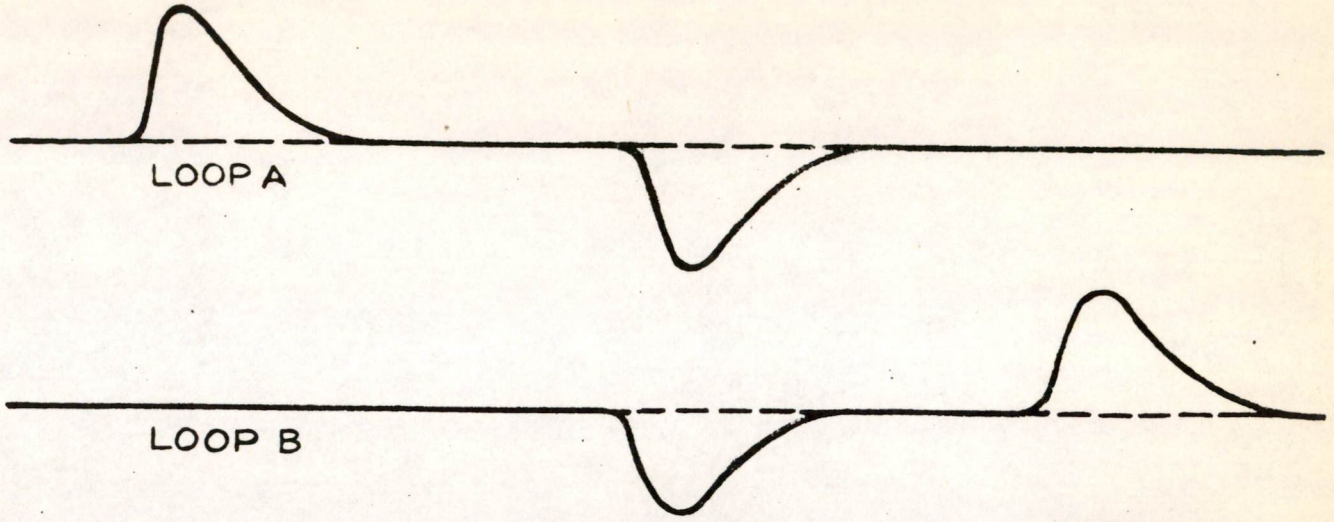


FIG. 3.5

CURRENT PULSES IN LOOP A AND B, WHEN THE LOOP RESISTANCES EMPLOYED ARE LARGE ENOUGH TO END THE CURRENTS BEFORE THE SECOND PULSES ARE APPLIED

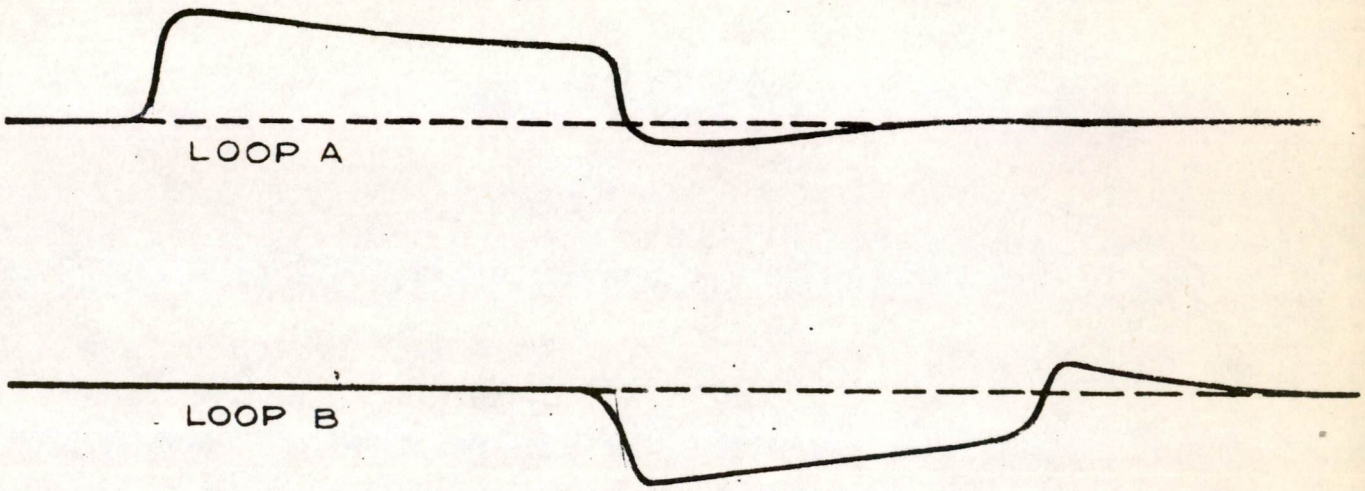


FIG. 3.6

CURRENT PULSES IN LOOPS A AND B, WHEN THE LOOP RESISTANCES EMPLOYED ARE NOT LARGE ENOUGH TO END THE CURRENTS BEFORE THE SECOND PULSES ARE APPLIED

current pulse in loop B will carry the core to the ONE position, but the second pulse may not be able to drag the core to the ZERO position. It would seem reasonable then, that when an attempt is made to write a ONE under these conditions, a ZERO is actually written; and vice versa. It has been found experimentally, in every case, that if the cycle time is made too short, it has become difficult to store ZEROs. These results are demonstrated in Table VII. It is possible, therefore, that with this type of operation the core may be in some peculiar position on the hysteresis loop. For instance, refer ring to the hysteresis loop shown in Fig. 3.7, when attempting to write a ONE, the first pulse circulating in loop A drives the memory core to point 1 on the loop. By the time the second pulse is applied to loop A, the excitation has decayed to point 2 on the loop. The second pulse succeeds only in carrying the core only as far as point 3. The core finally settles at point 4. This represents a ONE, but will lead to a low output when read out. In the same way a ZERO could be made to reside at some point just positive on the flux axis rather than at the normal ZERO position.

An important fact that has not been discussed concerning the nature of the loop is that it is very much dependent upon the geometry of the loop. Thus, if a different wiring scheme were employed, the nature of the loop would probably be considerably altered; but this fact does not change the basic results drastically. No matter what the winding geometry is, some loop resistance will always be required to speed up the fall of the loop current and thereby, the operating speed of the memory.

It is desirable to determine the nature of the pulsed impedance of the loop, in order to determine whether it is much larger, much smaller

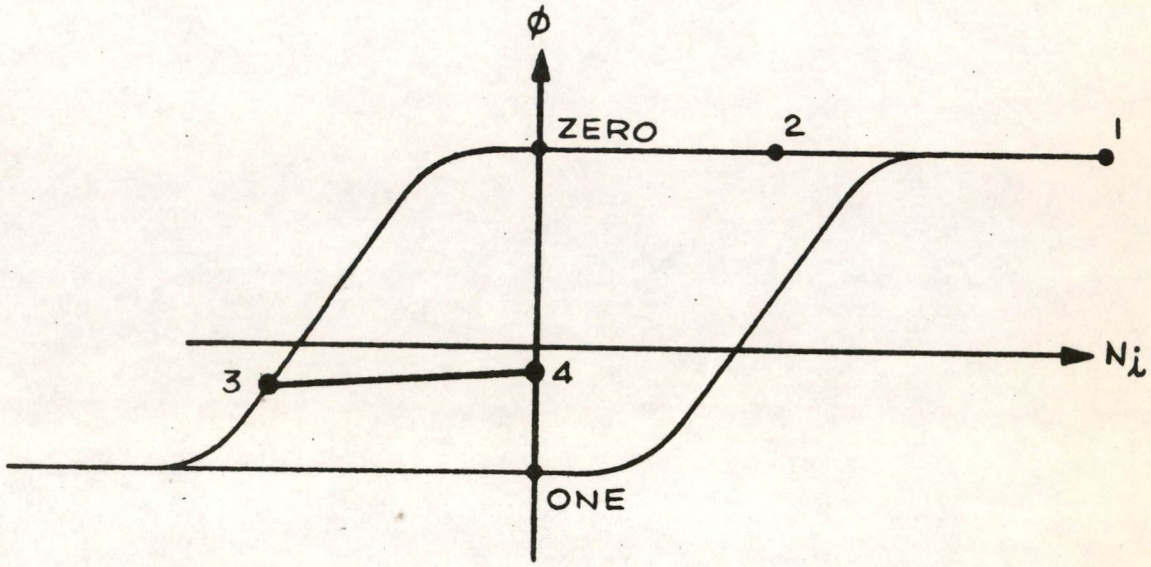
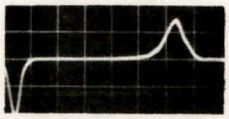
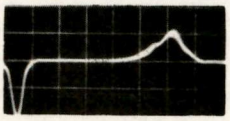
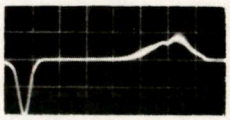
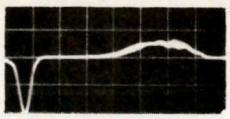
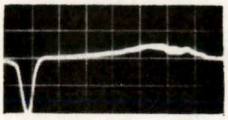


FIG. 3.7

HYSTERESIS LOOP ILLUSTRATING POSSIBLE OPERATION OF MEMORY CORE WHEN ATTEMPTING TO WRITE A ONE, IF R_{LOOP} IS TOO SMALL

or approximately the same as the pulsed impedance of the cores. In Chapter 2, the open circuit volt-ampere characteristics of various switch cores were found. This data gave the peak resistance of the cores in question. The reading may be repeated with the loop shunting the switch core. The memory core must be in place in order that the loop shape and size be correct, but it is not desired to have the memory core affect the data to be recorded. This problem is solved by winding a "dummy" memory core - one which is the same size as an ordinary core but which is non-magnetic. The result is that the loop, and only the loop, shunts the switch core. The nature of the loop may then be determined by comparing the open circuit characteristics of the cores, to the shunted characteristics. The photographs of Fig. 3.8 show the volt-ampere characteristics, for various driving currents, of the 1D264 switch core paralleled by the coupling loop (R_{loop} = 1 ohm). (Only full selects are recorded.)

The data for several cores is presented in Table VI, and this data is plotted graphically in Fig. 3.9.

	DRIVING EXCITATION (AMPERE-TURNS)	VOLTAGE OUTPUT FIRST PULSE (VOLTS)
	17.0	6.4
	16.0	5.8
	15.0	4.4
	14.0	3.7
	13.0	2.6
	12.0	2.0

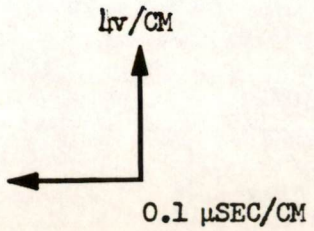


FIG. 3.8

FULLY SELECTED OUTPUT VOLTAGES FOR VARIOUS EXCITING CURRENTS OF 11DCL-2-720H2L-1, SIZE 1D264 SWITCH CORE PARALLELED BY THE COUPLING LOOP AND DUMMY CORE (R LOOP = 1 OHM) BIAS = 9.5 AMP-TURNS

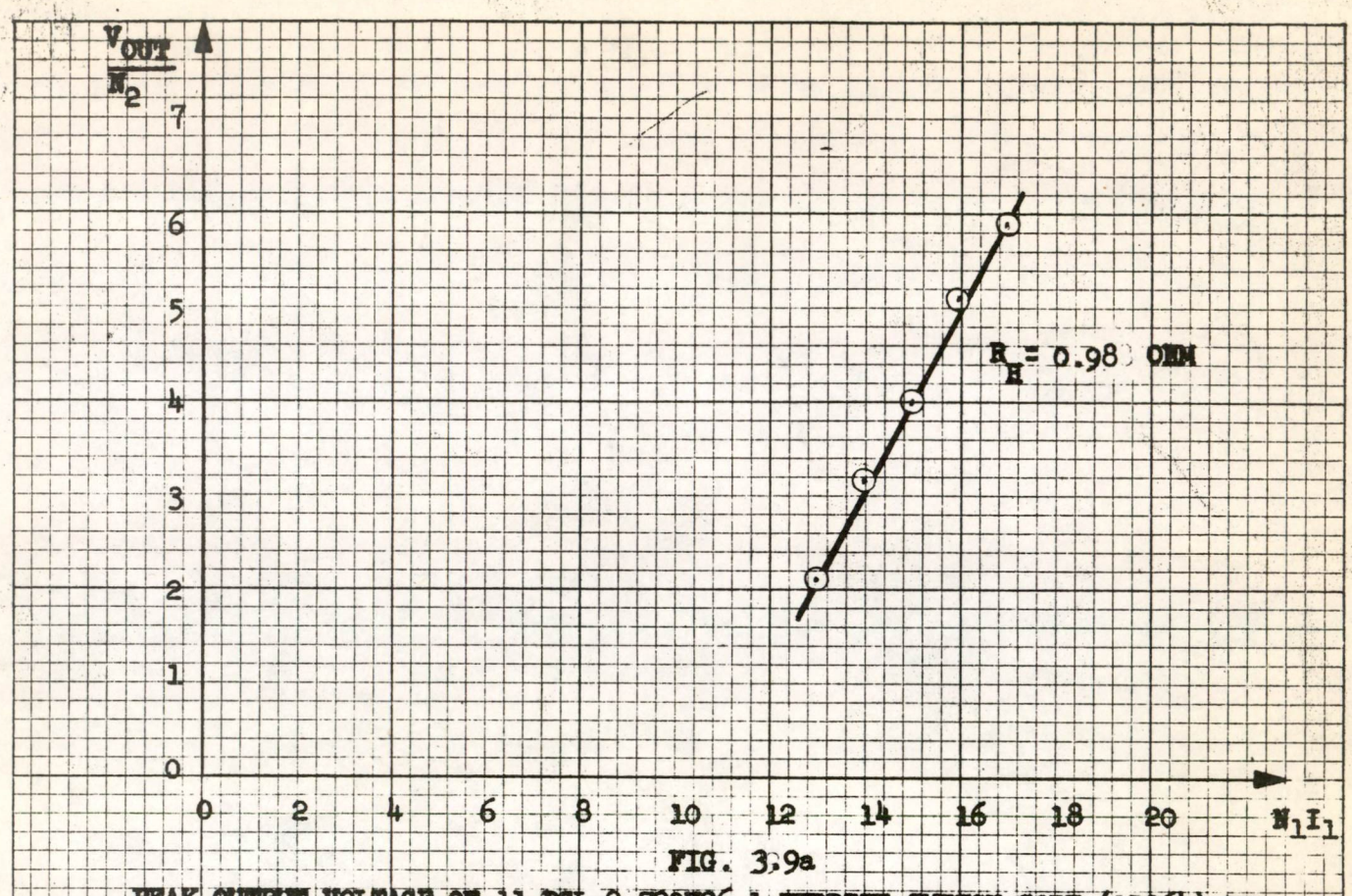


FIG. 3.9a

PEAK OUTPUT VOLTAGE OF 11 DCL-2-720H26-1 FERRITE SWITCH CORE (1D264) IN PARALLEL WITH LOOP AND DUMMY CORE R LOOP = 0 OHM BIAS = 9.5 AMP. TURNS

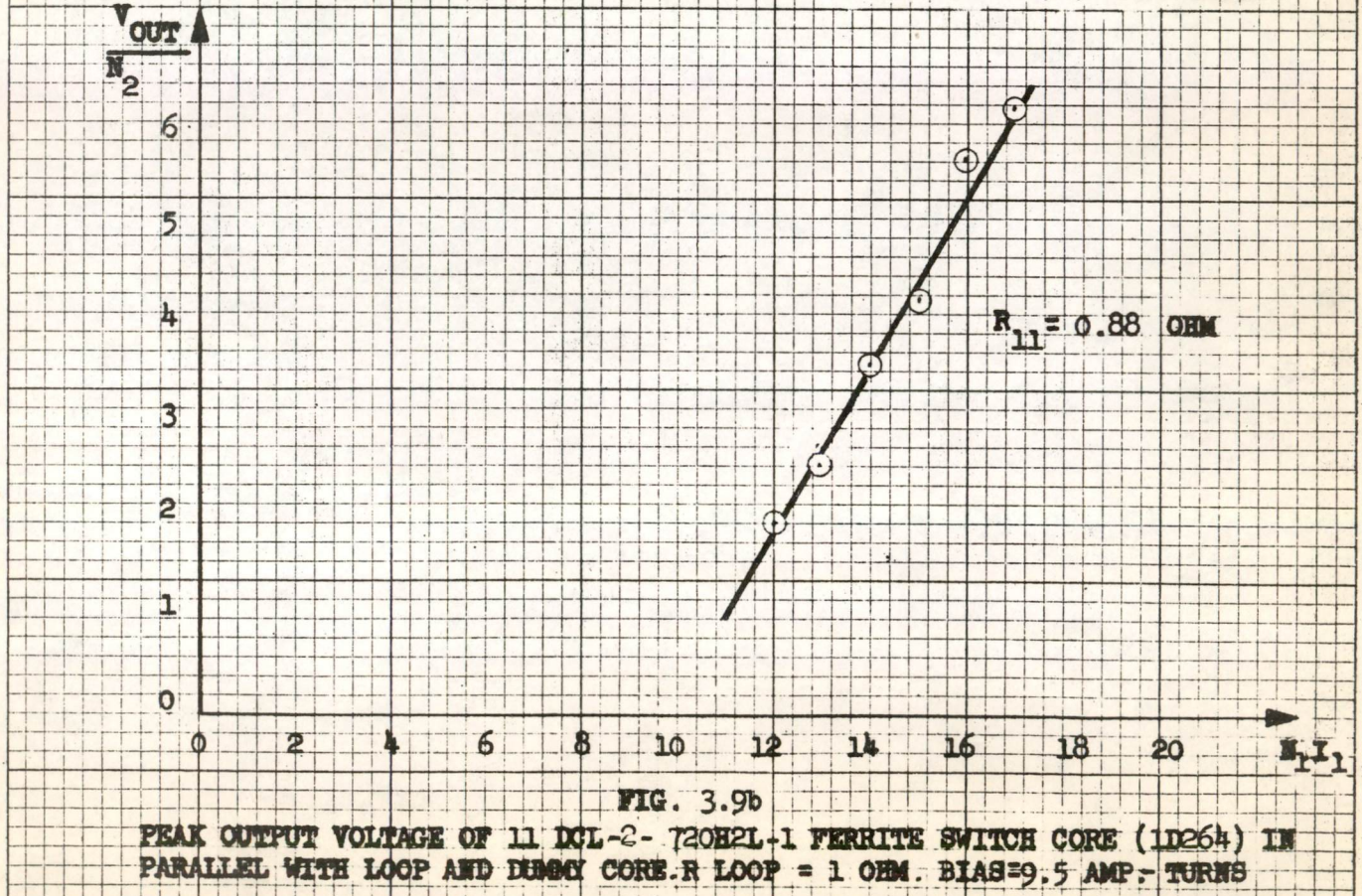


FIG. 3.9b

PEAK OUTPUT VOLTAGE OF 11 DCL-2- 720H2L-1 FERRITE SWITCH CORE (1D264) IN PARALLEL WITH LOOP AND DUMMY CORE.R LOOP = 1 OHM. BIAS=9.5 AMP.- TURNS

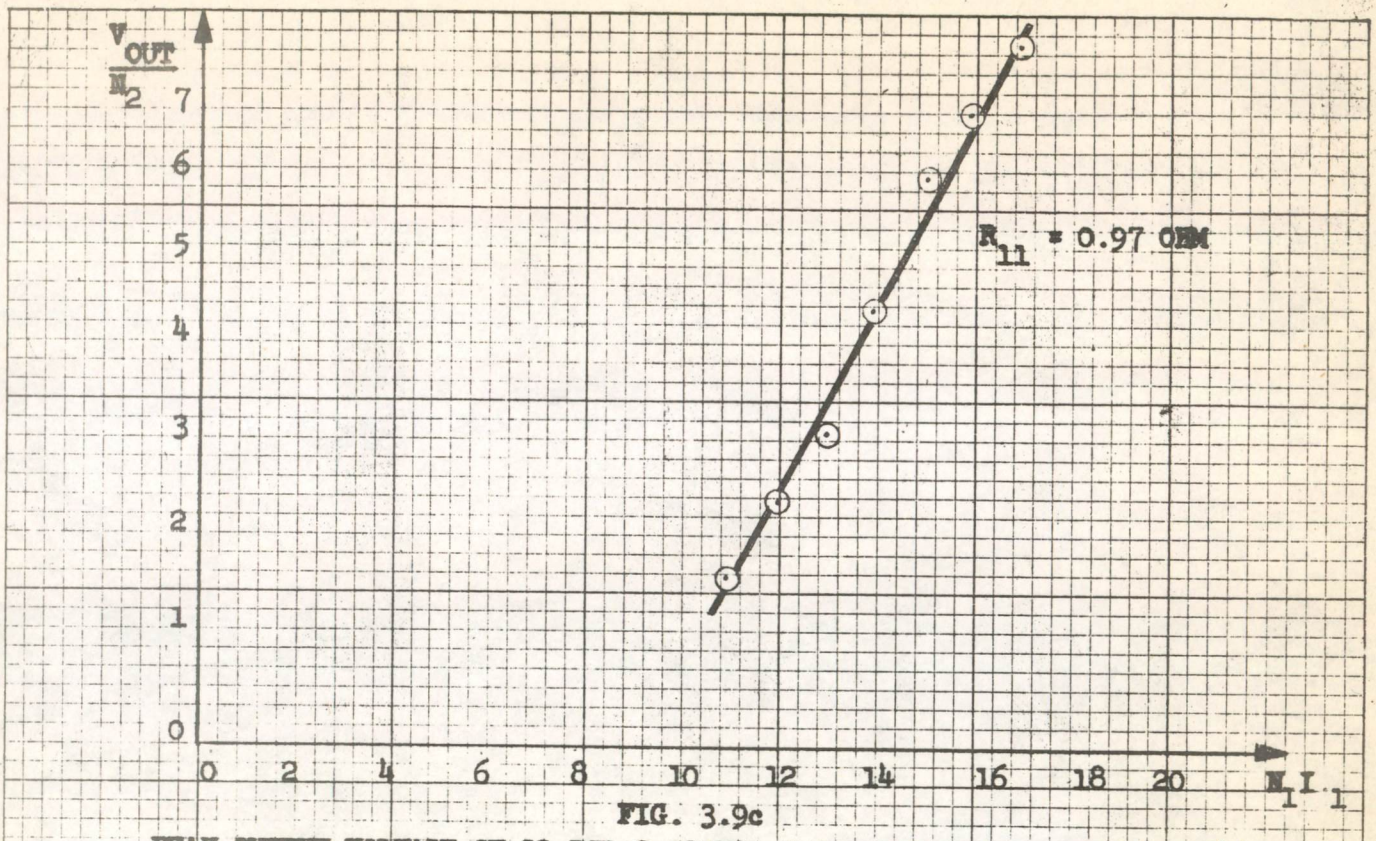


FIG. 3.9c

PEAK OUTPUT VOLTAGE OF 11 DCL-2-720H2L-1 FERRITE SWITCH CORE (1D264)
IN PARALLEL WITH LOOP AND DUMMY CORE. R LOOP = 2 OHM. BIAS=9.5 AMP.TURNS

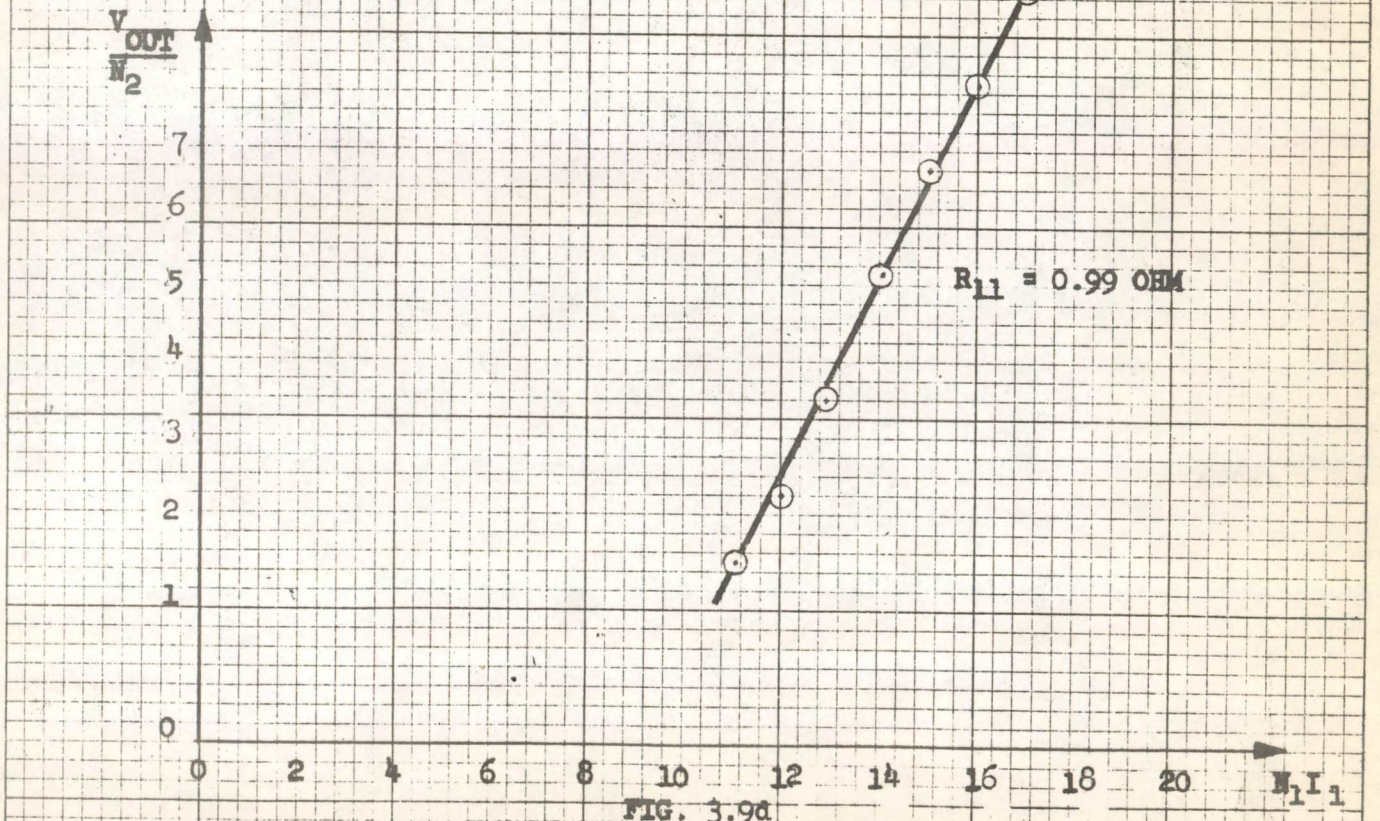


FIG. 3.9d

PEAK OUTPUT VOLTAGE OF 11 DCL-2-720H2L-1 FERRITE SWITCH CORE (3F395)
IN PARALLEL WITH LOOP AND DUMMY CORE R LOOP =1 OHM. BIAS = 9.5 AMP.- TURNS

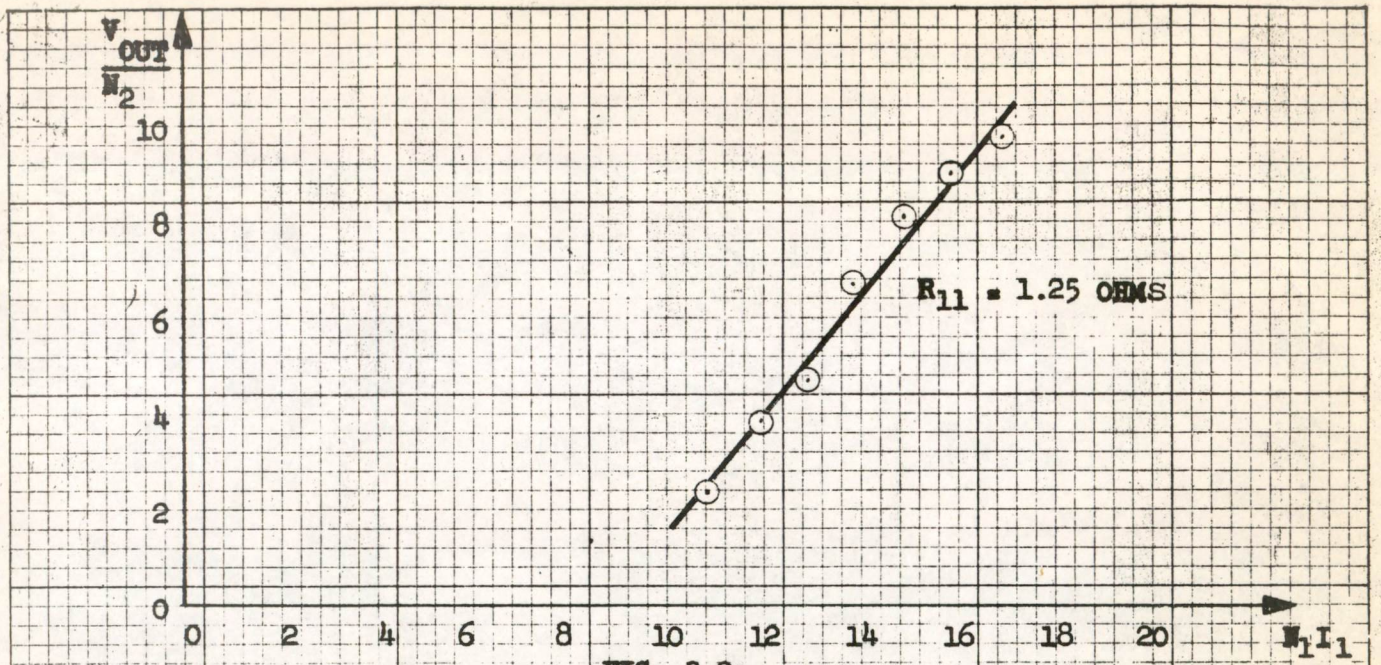


FIG. 3.9e

PEAK OUTPUT VOLTAGE OF 11 DCL-2-720H2L-1 FERRITE SWITCH CORE (6F395) IN PARALLEL WITH LOOP AND DUMMY CORE. R LOOP = 1 OHM. BIAS = 9.5 AMP. TURNS

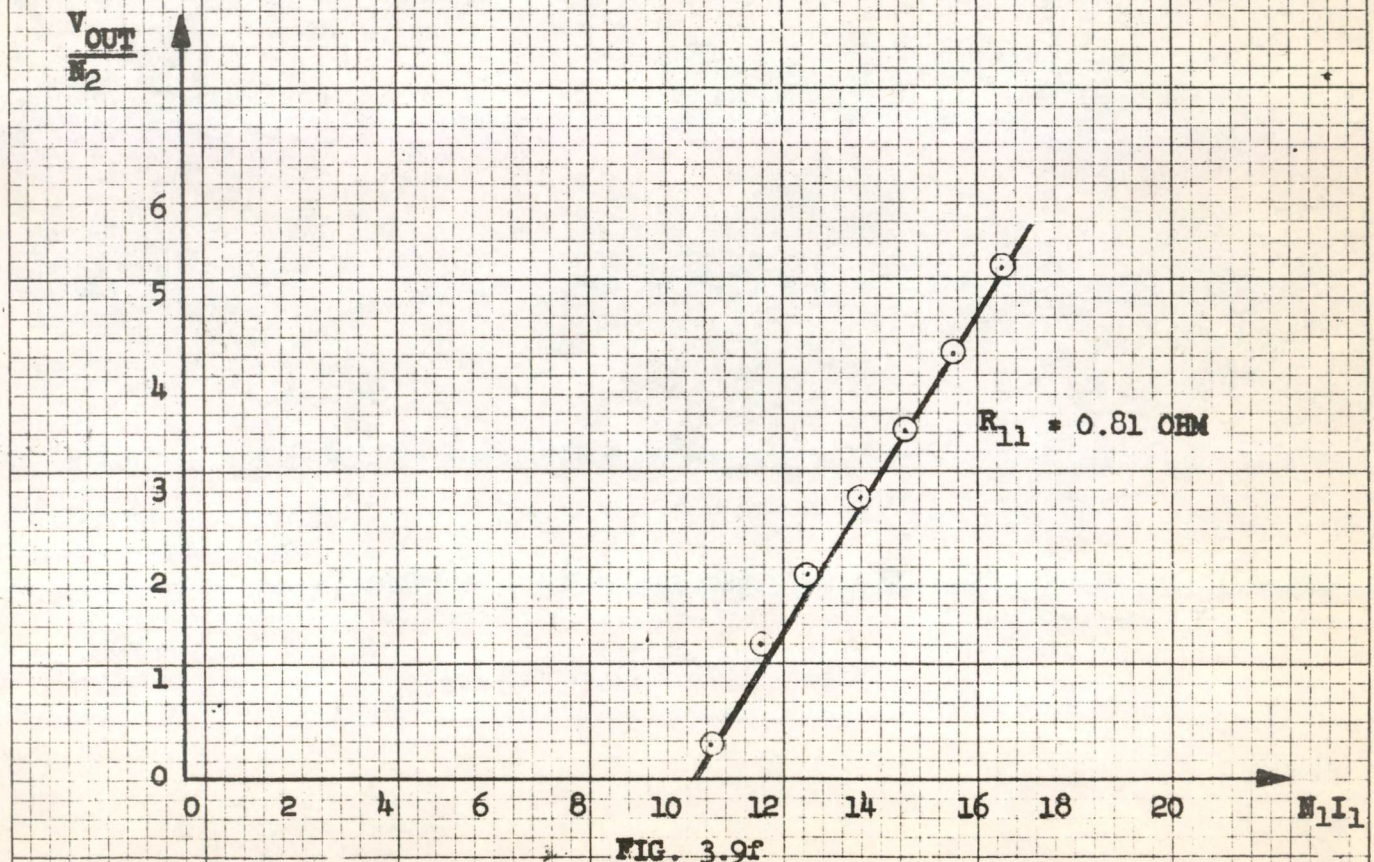


FIG. 3.9f

PEAK OUTPUT VOLTAGE OF DCL-3-44 FERRITE SWITCH CORE (6F397) IN PARALLEL WITH LOOP AND DUMMY CORE. R LOOP=31 OHM, BIAS = 9.5 AMP.- TURNS

TABLE VI

Peak Switch Core Output Voltages for Various Driving Currents when Shunted by Coupling Loop

Driving Current (Ampere Turns)		Peak Switch Core Output Voltages 11DCL - 2 - 720H2L - 1					DCL-3-44
		1D264	1D264	1D264	3F395	6F395	6F397
		$R_{loop}=0\Omega$	$R_{loop}=1\Omega$	$R_{loop}=2\Omega$	$R_{loop}=1\Omega$	$R_{loop}=1\Omega$	$R_{loop}=1\Omega$
	11			1.8	1.9	2.4	0.36
	12		2.0	2.6	2.6	3.9	1.4
	13	2.1	2.6	3.3	3.6	4.8	2.1
	14	3.2	3.7	4.6	4.9	6.8	2.8
1	15	4.0	4.4	6.0	6.0	8.1	3.6
	16	5.2	5.8	6.7	6.8	9.1	4.4
17	17	5.9	6.4	7.3	7.8	9.8	5.3
Peak Resistance of Core and Loop in Parrallel in ohms (Full Selected)		0.98	0.88	0.97	0.99	1.25	0.81
Peak Resistance of Core open Circuited in ohms (Full Selected)		1.3	1.3	1.3	1.5	2.2	1.1
Effective Loop Impedance in ohms		4.0	2.6	3.8	2.9	2.9	3.1

The results geven in Table VI demonstrate that the pulsed impedance of the coupling loop is approximately 3 ohms. Table V shows that the loop inductance is about 0.1 microhenries. The loop current rise time is 0.5 microsecond - this corresponds to a fundamental frequency of 5 megacycles. The expected loop impedance is, therefore, $2\pi \times 5 \times 10^{6} \times 0.1 \times 10^{-6} = \pi \cong 3$ ohms. The results obtained are observed to support each other.

C. An Analytical Approach to the Problem

Chapter 2 attempted to point out the fact that ferromagnetic cores may be represented, approximately, by piece-wise linear volt-ampere characteristics (see Figs. 2.23 and 2.24). The results shown in section B of this chapter demonstrate that the nature of the loops coupling the switch cores to the memory core are essentially linear impedances.

Two methods of attacking this problem of the behavior of the memory unit may be employed - one is graphical and the other is algebraic. The advantage of the graphical method is that it is valid even if the characteristics of the elements are not linear. Answers may be obtained graphically no matter what the elements look like; all that is required is that the nature of the elements be known. The advantage of the algebraic attack is that a set of equations may be written that covers the operation of any set of loops and cores. All that is necessary to solve a particular problem is to substitute the data obtained by testing the various parts of the memory unit into these equations. The algebraic method may be used to determine what the ratios amongst the various parameters must be in order to obtain the best operation. The disadvantage encountered in using algebra, is that the equations become cumbersome in the absence of simplyfying assumptions; and if the element characteristics are not piece-wise linear, the problem becomes too complicated to warrant any attempted solution.

In setting the problem up for solution, use is made of the circuit of Fig. 3.1, and of the core equivalent circuits of Figs. 2.13. The impedance elements, R_2 and L_{L2} are merely included in the loop impedances as are the primary leakage inductances of the memory core. The complete loop impedance is lumped together and is called Z_{loop}. Z_{loop}

is not to be confused with R_{loop}, which is the resistance added to the loop in order to speed the operation of the memory. It should also be noted that each loop has one turn, as does the sensing winding. The driving lines (which carry I_a and I_b) have five turns each. Use is made of these facts in simplifying the equivalent circuit shown in Fig. 3.10. Another simplification is the fact the core impedances include biases and coercive forces. Thus, parallel current drivers are omitted. The currents I_a and I_b include only the X and Y currents exciting the switches. The volt-ampere characteristics of the switches are shown in Fig. 2.23; that of the memory core is shown in Fig. 2.24. These elements cannot really be thought of as resistors in the usual sense, because of the piece-wise linear characteristic they exhibit. The loop impedance, Z_{loop} is assumed to be linear.

If the pulse sequences are considered, it is seen that the first pulse delivered by core A and acting on core B through the memory are in the direction that tends to drive core B further into saturation; the second pulse out of A tries to switch B. Similarly, the first pulse out of B tends to drive A toward saturation and the second pulse tries to switch A.

Reading is accomplished during the first pulse from A, and this is the time at which measurements of ONE to ZERO ratios, and ONE to half-select ratios are made. Thus, it can be seen during the read operation, core B appears as a linear inductance (meaning that it has no break point) in the light of the approximations that have been made concerning the operation of the cores.

(1) <u>The Graphical Solution (Including the Loading of Loop B)</u>

The problem that is to be solved in this section is the one of

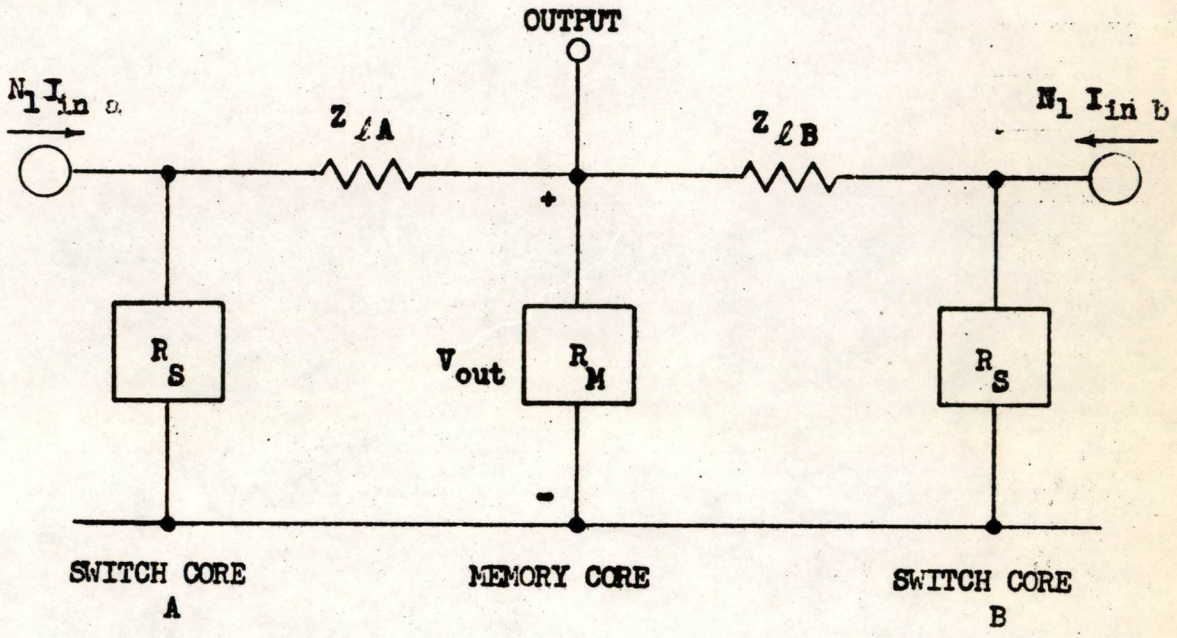


FIG. 3.10

EQUIVALENT CIRCUIT OF MEMORY UNIT SHOWN IN FIG. 3.1

predicting the sizes of ONEs, ZEROs, and half-selected outputs graphically. The loading of loop B and switch core B upon the memory core is taken into account in this solution. The equivalent circuit is shown in Fig. 3.10. The volt-ampere characteristics of the loop impedances Z_{1A} and Z_{1B}) are linear. The volt-ampere characteristics of the switch and memory cores are shown in Figs. 2.23 and 2.24. The symbols used are defined here:

S_A = volt-ampere characteristic of Switch core A;

S_B = volt-ampere characteristic of Switch core B;

L = volt-ampere characteristic of the loop; and

M = volt-ampere characteristic of the memory core.

Fig. 3.11 shows the transfer characteristic (output voltage versus input current) when the memory core holds a ONE. This curve is labelled output. Fig. 3.12 gives the transfer characteristic (output) when the memory core holds a ZERO.

The method used in constructing these curves is outlined in Appendix E.

It is observed that, in general, the input and output characteristics of the memory unit have two break points each -- one occurs when switch core A switches, and the other when the memory core switches. If the memory core holds a ZERO, the input and output curves have only one break which occurs when core A switches.

2. The Graphical Solution (Omitting the Loading of Loop B)

The constructions presented in Figs. 3.11 and 3.12 have been complicated by taking the loading of loop B and core B upon the memory core into account. A great simplification in the work may be realized by

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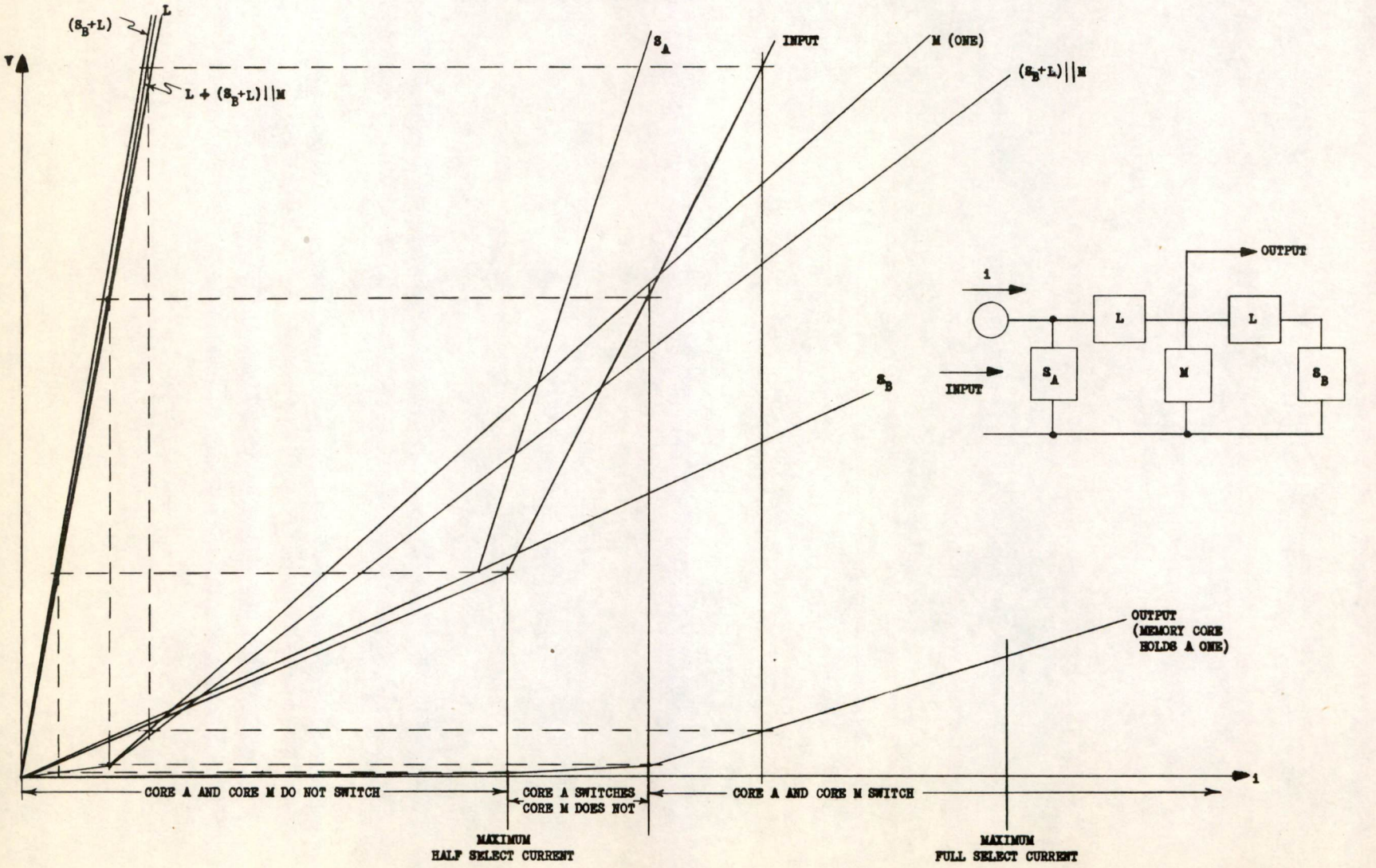


FIG. 3.11

GRAPHICAL SOLUTION OF MEMORY CORE OUTPUT AS A FUNCTION OF EXCITATION
(LOADING OF MEMORY CORE BY LOOP B IS INCLUDED) MEMORY CORE HOLDS A ONE

MODE A OPERATION
(SWITCH CORE SWITCHES BEFORE
MEMORY CORE DOES)

B-61405

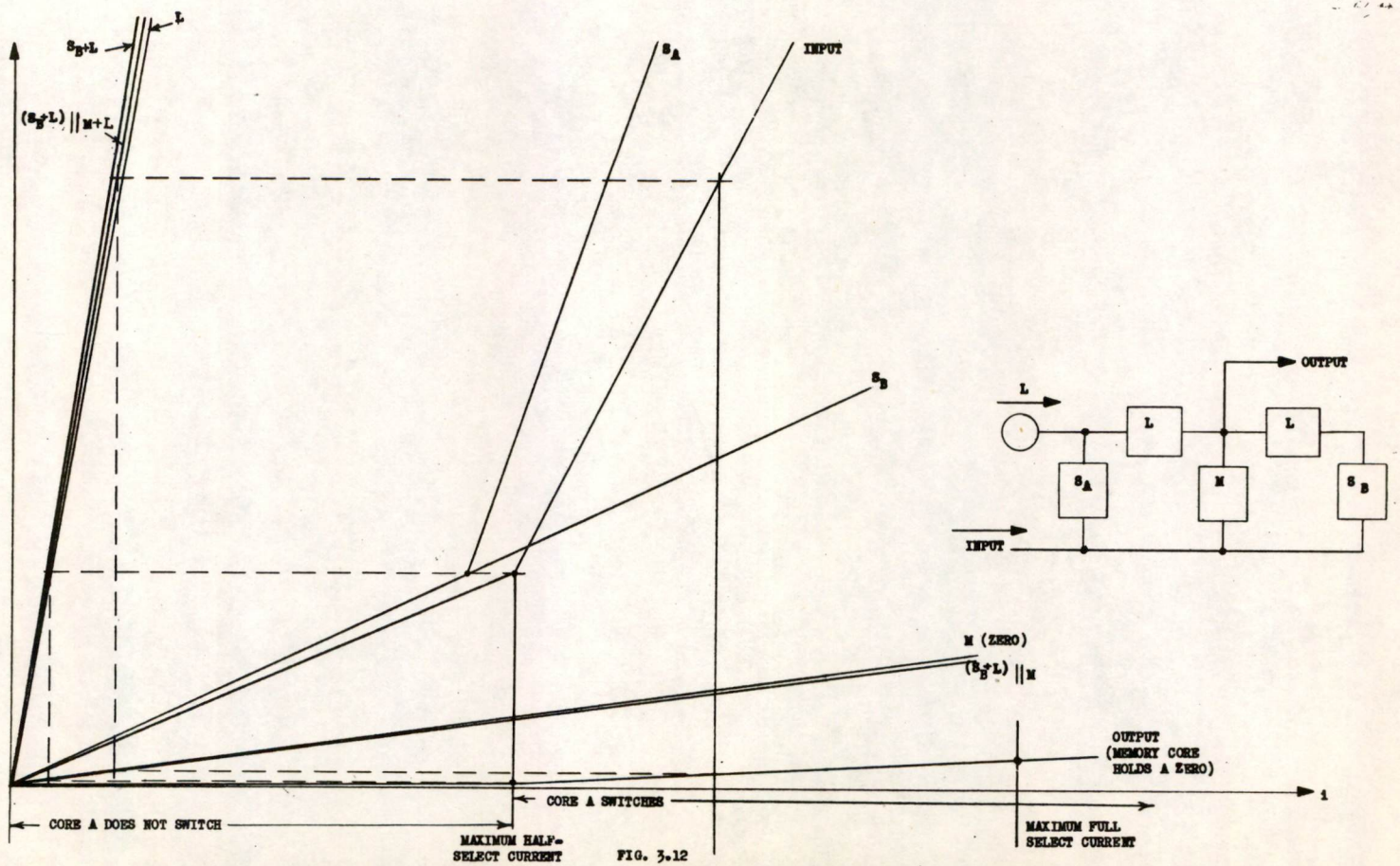


FIG. 3.12

GRAPHICAL SOLUTION OF MEMORY CORE OUTPUT AS A FUNCTION OF EXCITATION (LOADING OF MEMORY CORE IN LOOP B IS INCLUDED) MEMORY CORE HOLDS A ZERO

neglecting loop B. It has been found that the partially selected memory core has an incremental resistance that is less than 0.1 ohms. The 3 ohm loading of loop B in this case is negligible. The fully selected memory core is about 0.5 ohms. If the shunting 3 ohms is forgotten, the error is about 15 per cent. This error certainly will not invalidate the results obtained.

Fig. 3.13 illustrates the transfer characteristic of the unit (labelled output) when the memory core holds a ONE. When the memory core holds a ZERO, the transfer characteristic is shown in Fig. 3.14.

These constructions follow the same principles described in Appendix E, but they are simpler because of the omission of loop B.

It is noted that in the operation illustrated in Figs. 3.11 and 3.13 that the switch core switches at a lower driving current than is required to switch the memory core. It is possible, by choosing elements of the proper size, to cause the memory core to switch at a lower current than that at which core A is switched. In either case the absolute maximum allowable half-select current is that which just tends to switch the most easily disturbed core. The reasoning behind this statement is apparent.

Suppose that core A is the first core to be switched (Mode A) and the excitation with which it is disturbed is enough to switch it, but is too small to switch the memory core. When the half-select current is removed, only bias is applied to core A and the result is that A is vigorously switched back to its original condition, and it drags the memory core with it. This, of course, destroys the information content of the memory. In Mode B, the memory core tends to switch first,

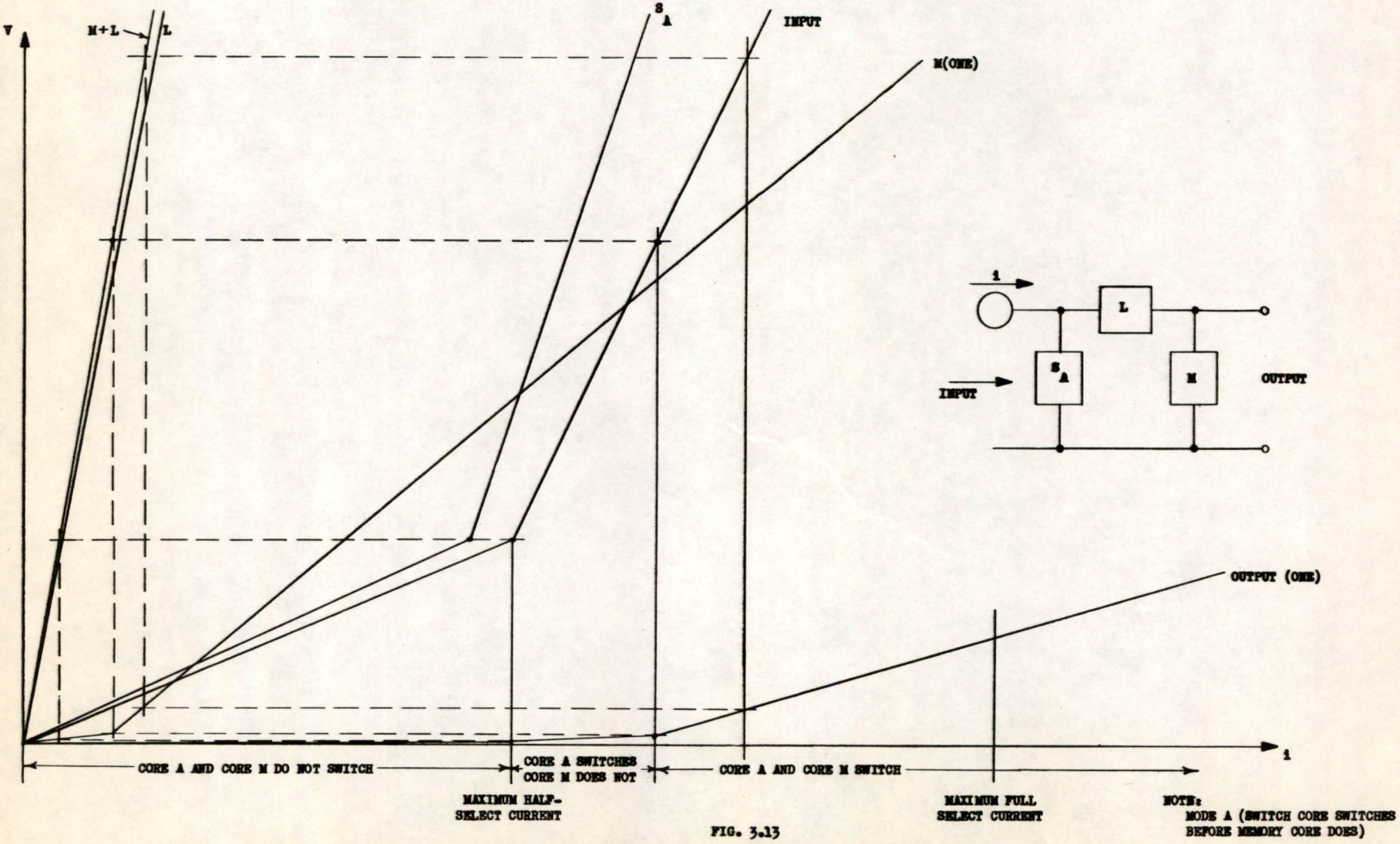


FIG. 3.13

GRAPHICAL SOLUTION OF MEMORY CORE OUTPUT AS A FUNCTION OF EXCITATION
(LOADING OF MEMORY CORE BY LOOP B OMITTED) MEMORY CORE HOLDS A ONE

B-61372

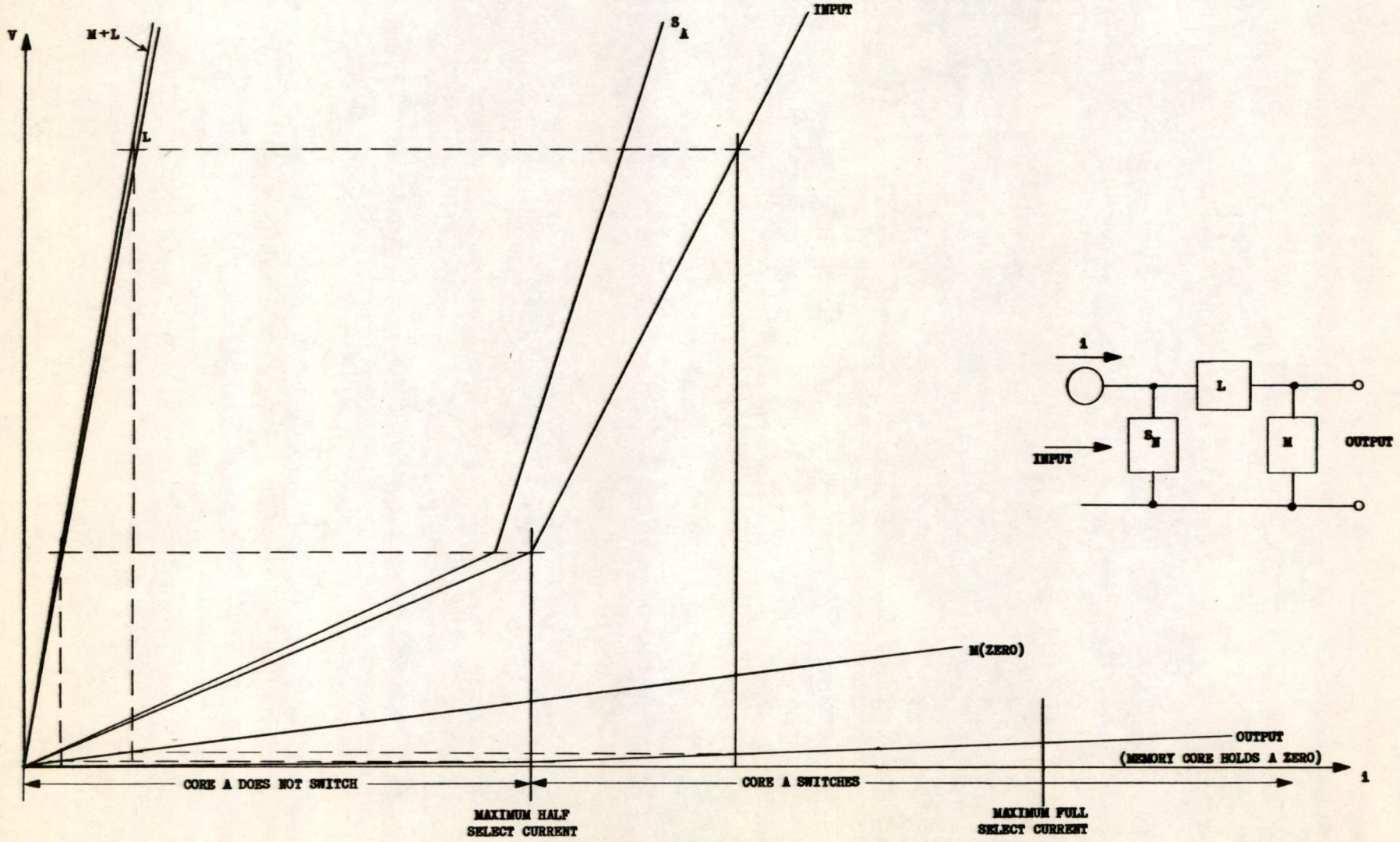


FIG. 3.14

GRAPHICAL SOLUTION OF MEMORY CORE OUTPUT AS A FUNCTION OF EXCITATION
(LOADING OF MEMORY CORE BY LOOP B OMITTED) MEMORY CORE HOLDS A ZERO

and the half-select excitation must not be large enough to read out of an unselected core. It is readily observed that this condition limits how heavily the cores may be driven. It is obvious that the larger the bias applied to a switch core is, the harder it may be driven on half selects. But the output voltage of a half-selected core has been found to be virtually proportional to the half-selecting current. If this voltage is allowed to become large enough to select an unwanted memory core, then operation has failed. The conclusion is that the coercive force of the memory core is a major factor in limiting the amount of drive that the switch core may be subjected to.

A problem encountered concerns the time at which Core B should be excited. Should the excitation of B begin at the same time that the excitation of core A ends (as pictures in Figs. 3.5 and 3.6), or should the driving of B be held back until the effects of core A on the memory core have been extinguished by losses (as indicated in Figs. 3.3)? Either method has its disadvantages.

An investigation of each driving method must be made qualitatively Quantitative analysis of the problem will be given later, when the problem is solved algebraically (section C3 of this chapter and Appendix D).

If the excitation of B begins coincidentally with the end of A's excitation, then the last pulse from A and the first pulse from B drive the memory core simultaneously, (Fig. 3.5). The result is that the memory is hit very hard at this time and consequently it switches rapidly. Furthermore, operation is speeded by the fact that there is no waiting period between read and write cycles. Unfortuantely, if this

operation is employed, the cores may not be driven very heavily, for one must take into account the result of half-selected noises.

If the half-selected noise currents sent out by cores A and B are each I_{noise}, then: when A is disturbed, a current of I_{noise} is driven through loop A; when A is unselected and B is disturbed, the total current exciting the memory core is $2I_{noise}$ (it tends to place a ONE in the memory core); and when B is unselected the current in loop B is again I_{noise}. It is assumed, here, that the current drives behave in the same manner when they fall as when they rise.

The weak link in the system is the center pulse. The half-select excitations of cores A and B must not be allowed to be so large that $2I_{noise}$ exceeds the coercive force of the memory core. This immediately eliminates the possibility of operating in Mode B (memory core switches before switch core does). The reason is that the maximum half-select output current of a single switch core is one-half the coercive force of the memory core. If the operation is in Mode B, then by definition, the half-select input current must be somewhat less than one-half the effective coercive force (including bias) of the switch core. This operation is demonstrated in Fig. 3.15. In that event, a fully selected switch core does not switch (and the memory core just manages to switch). This operation is intolerable for the switch cores must switch if the memory unit is operated correctly.

The characteristics shown in Figs. 3.11 and 3.13 are Mode A. When the unit is half-selected the memory core is less than half-selected, and so it may successfully be operated when the last pulse from core A coincides with the first pulse from core B, even though the switches are

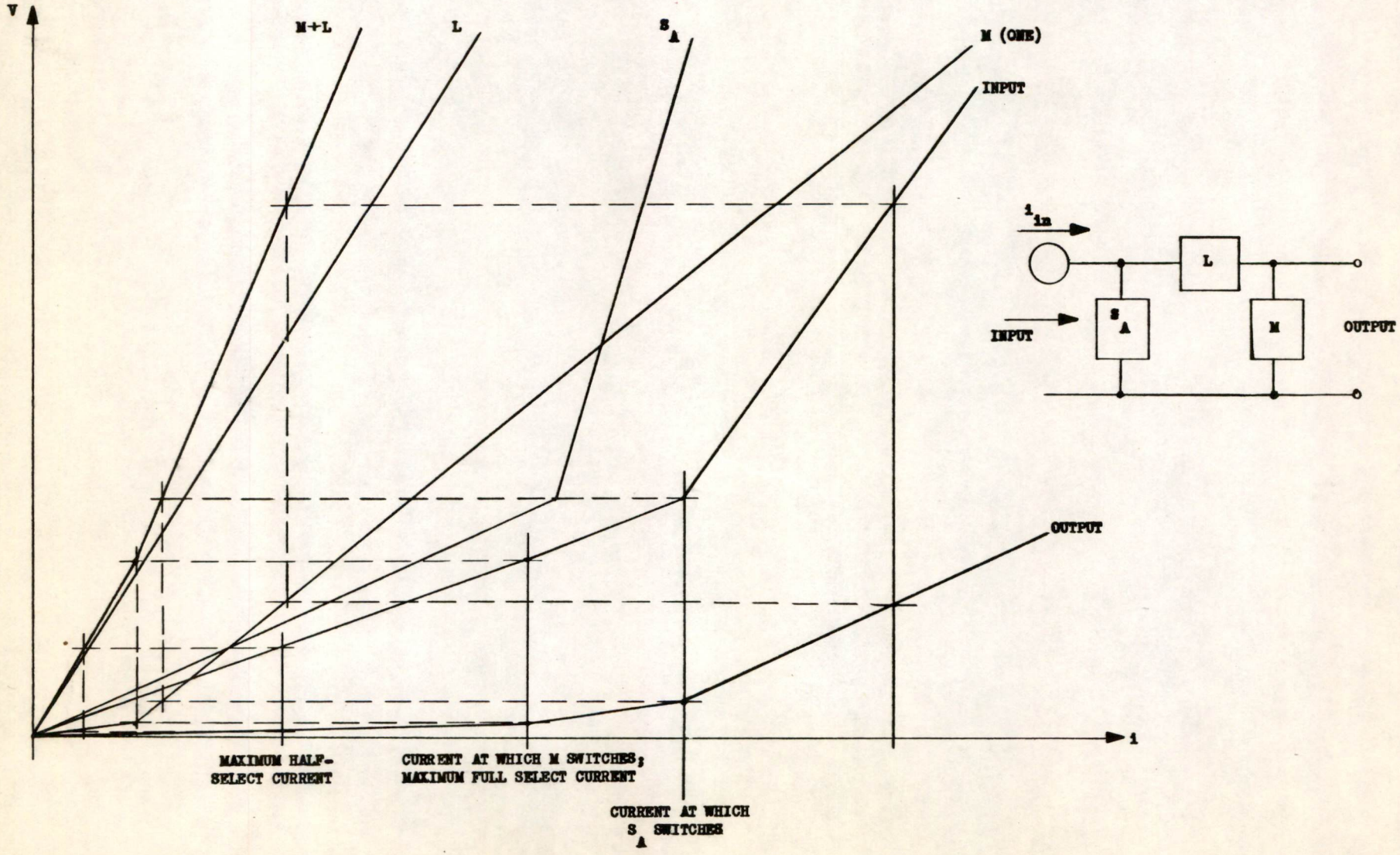


FIG. 3.15

GRAPHICAL SOLUTION OF MEMORY UNIT OPERATION IN MODE B (MEMORY CORE SWITCHES BEFORE SWITCH CORE DOES)
LOADING OF MEMORY CORE BY LOOP B OMITTED OPERATION SHOWN IS WHEN CORE A IS TURNED OFF COINCIDENTLY WITH THE TURNING ON OF CORE B

driven as heavily as possible. In fact, the switches could be driven harder and safely in that case. However, it should be realized that the setup shown in those figures is not nearly the best possible.

If core B is required to wait for the excitations caused by core A to die out before it is excited, excitations may be doubled. In this case, there is no time when two noise currents add to double unwanted excitations.

The best type of operation is that under which both the switch and memory cores just begin to switch simultaneously for a given value of input current to the cell (Fig. 3.16). This is considered to be optimum because the ONE to ZERO, and ONE to noise ratios should be the largest that can be obtained using the given cores. The reason is that there are not three states but only two. The state that has been eliminated is the one in which one core switches and the other does not. This state contributes little to the output voltage of a fully selected ONE, but it uses up driving current.

The difficulty encountered in this operation is the fact that the cycle time is slowed down by the necessity of waiting for the current in loop A to have decayed before the write cycle can commence.

3. The Algebraic Solution (Omitting Loading of Loop B)

The algebraic solution of the problem merely consists of writing the piece-wise linear equations of the graphs shown in Figs. 3.13 (when M holds a ONE) and 3.14 (when M holds a ZERO). The derivation of these equations is tedious and is presented in Appendix D.

Two symbols -- μ and σ are introduced in Appendix D. These are defined by equations (D.72) and (D.73) which are repeated below.

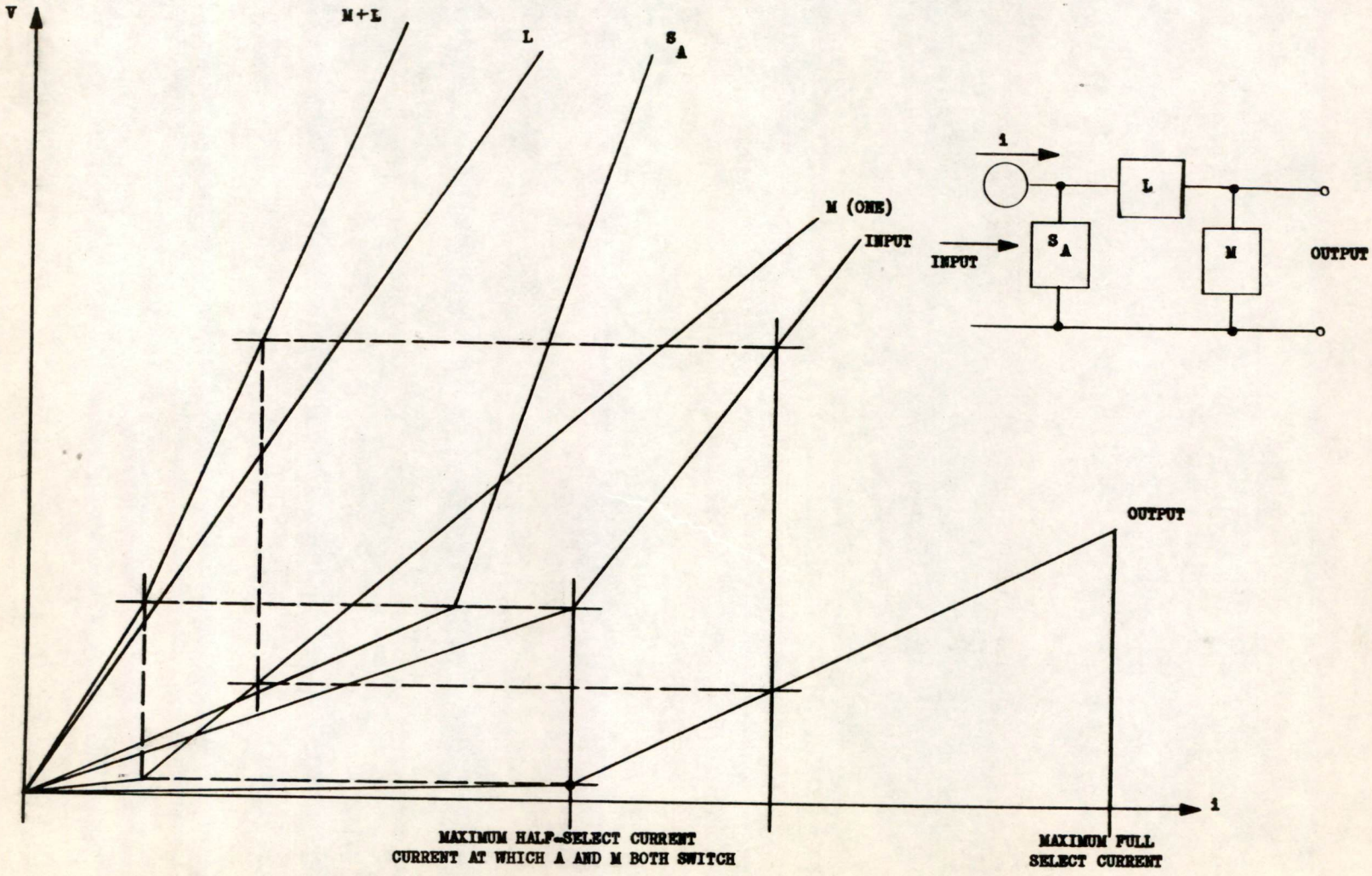


FIG. 3.16

GRAPHICAL SOLUTION OF MEMORY UNIT WHEN MEMORY CORE AND SWITCH CORE ARE SWITCHED AT THE SAME DRIVING CURRENT
LOADING OF MEMORY CORE BY LOOP B OMITTED OPERATION IS POSSIBLE ONLY WHEN LOOP CURRENT A IS ALLOWED TO EXPIRE BEFORE B IS EXCITED

$$\mu = \frac{FM}{HM} \qquad (3.2)$$

$$\sigma = \frac{FS}{HS} \qquad (3.3)$$

These constants have been found to be about 10 each. The results of Appendix D may be stated in terms of these constants. It is found for the memory system using external selection, that the ONE to ZERO ratio is approximately μ, and the ONE to half-select ratio is approximately $\mu\sigma$.

It was found (Chapter 2) that in a coincident current memory system, the ratio of ONE to ZERO is about $\mu/2$, and the ONE to half-select ratio is about μ.

This data demonstrates that when the memory system using three cores is compared to the coincident memory, the ONE-to-ZERO ratio is better by a factor of 2, and the ONE-to-half-select ratio is better by a factor of σ(or about 10).

4. The Experimental Set-Up

All of the experimental data were taken from a one bit memory, consisting merely of two switch cores and one memory core. The equipment used in driving the memory unit is shown schematically in Fig. 3.17 (it is somewhat simplified; all logically unnecessary units having been removed). Fig. 3.18 is a photograph of the equipment racks used, and Fig. 3.19 shows the front and back views of the memory unit. The cores are mounted on the plug-in units.

The logical arrangement of Fig. 3.17 may be explained as follows: The core driver outputs labelled "a" are used to drive core A,

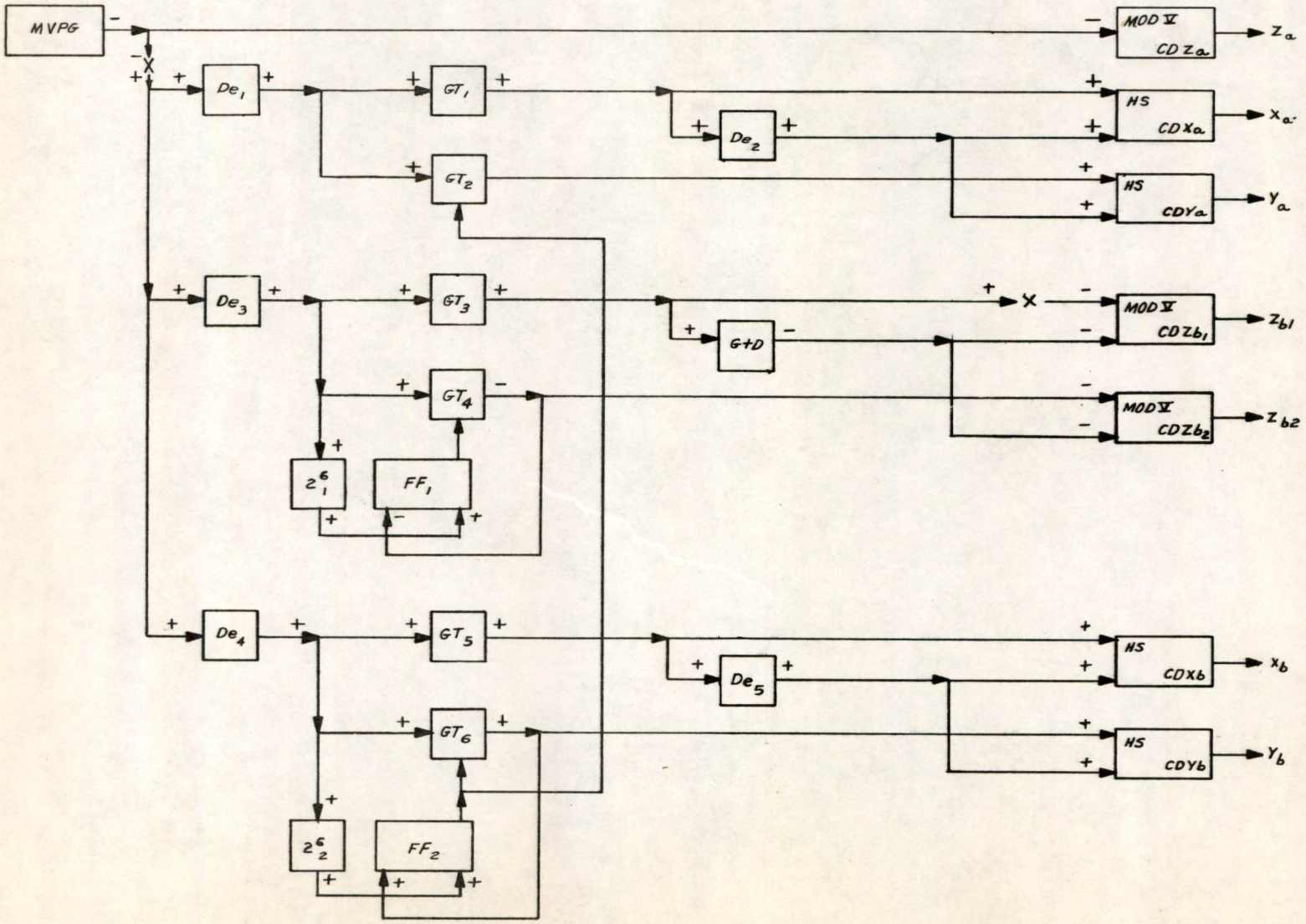


FIG. 3.17

SCHEMATIC DIAGRAM OF EQUIPMENT USED IN DRIVING THE ONE BIT MEMORY

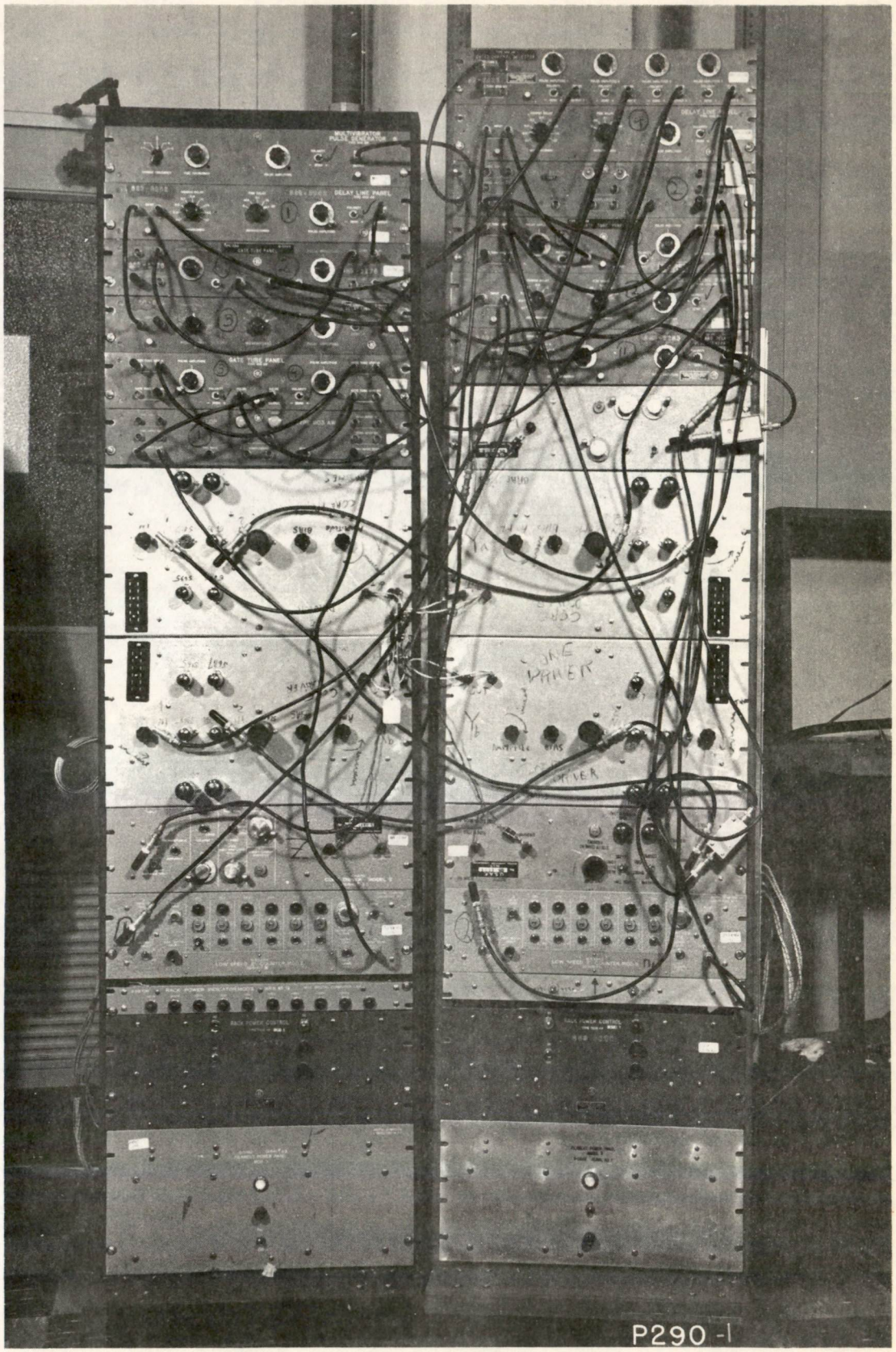
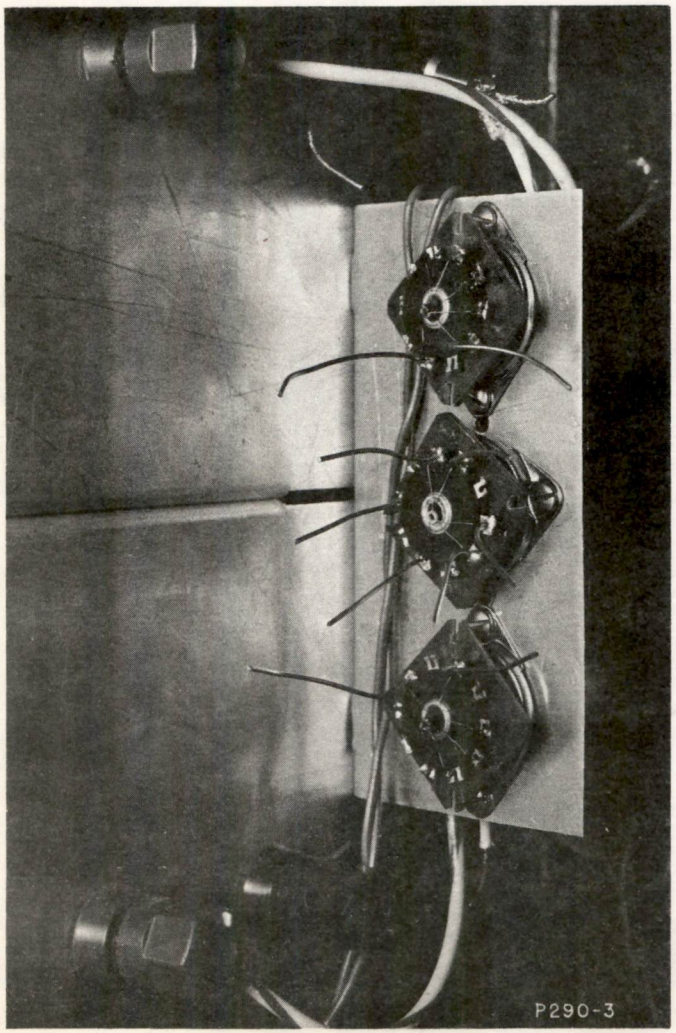
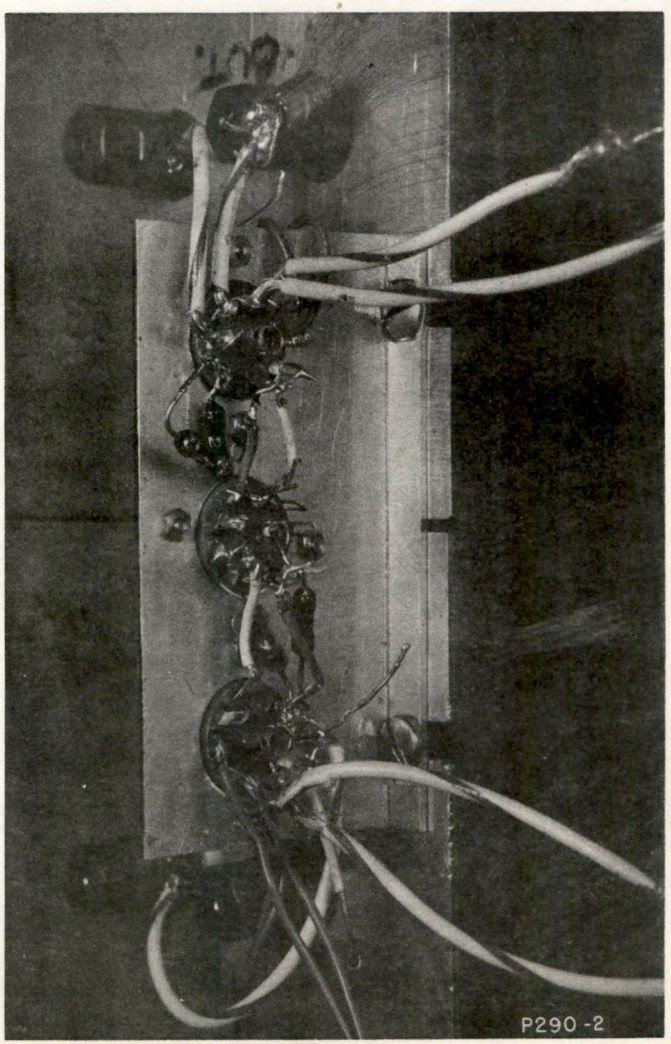


FIG. 3.18

PHOTOGRAPH OF EQUIPMENT



FRONT VIEW



BACK VIEW

FIG. 3.19

PHOTOGRAPHS OF MEMORY UNIT

and those labelled "b" drive core B. A pulse from the generator (MVPG) turns the core driver CD Za on. This is the bias on core A. The pulse is delayed by De, so that the bias may reach its steady state value, before the X and Y drivers are turned on. Gate tube 1, (GT_1) passes all pulses and turns CD Xa on. The other gate tube, GT_2, passes a pulse only if its third grid is high. If GT_2 is off, core A is half-selected; if GT_2 is on, core A is fully selected. Both core drivers are turned off by the delayed pulse from De_2. The delay, De_2, determines the length of time that the read cycle is on.

The generator pulse is delayed by De_3. The bias on core B, Zb_1, is turned on when the pulse passes GT_3. The setting of the counter 2^6, determines whether or not a pulse is delivered to core driver Zb_2. If Zb_2 is not turned on a ZERO may be written; otherwise a ONE may be written.

Delay panel, De_4, passes the pulse that turns on core driver, CD Xb, and may turn Yb on, if a full select is desired. Drivers Ya and Yb are connected so that if Ya is allowed to go on, Yb must also be turned on; likewise, if Ya is not allowed to go on, Yb cannot be driven either.

It should be noted that the diagram shown in Fig. 3.17, will not yield the pulse sequences illustrated in Fig. 3.3 The equipment used in Fig. 3.17 requires that the decision as to whether a ONE or a ZERO is to be written into the memory core be made before the read out begins. The only driver available for inhibiting purposes was a Mod. V, and this is too slow to use in a place as critical as the inhibiting position normally is in. This, of course, would not be the case in an

actual memory device, where it is generally necessary to know what the core held before deciding what shall be put into it. Although this system is somewhat unrealistic, it is useful in determining the nature of the memory system. The time at which the decision is made as to what information shall be stored does not affect the memory operation for these experiments.

5. The Experimental Results

The method of driving the memory unit used is that described in section C3a of Chapter 3 -- that is, the write cycle is started at the same time that the read cycle ends.

Actually, no attempt is made to obtain the optimum outputs described in section C3a, because of the fact that the core drivers used were not able to supply enough current, and the coercive forces of these cores are not as clearly defined as has been indicated. The knee of the hysteresis loops of the cores is bent, and this can cause undesirable noise outputs if operation is carried too close to the knee.

Equation (3.7) expresses the ideal relationship between the core and loop parameters. It states that

$$I_{2S} = \frac{I_M}{2} \quad \frac{L + HM}{HS} \qquad (3.7)$$

If the switch core and memory core are both of the 11DCL-2-720H2L-1 material, and the switch size is 1D264 and the memory core size 1F395, then from the results of Chapter 2 it is found that HM = .074 ohms, HS = 0.20 ohms. It has been found in Chapter 3 that L $\cong$ 3 ohms. The

hysteresis loop data of the 1F395 shows that the coercive force of the memory core, I_{IM}, is 1.56 amp. turns.

The required value of I_{2S} for ideal operation is then

$$I_{2S} = \frac{1.56}{2} \times \frac{3.07}{.2} \simeq 12 \text{ amp-turns.}$$

The coercive force of the 1D264 core is 2.35 amp-turns. The Mod V core Driver is capable of supplying 1.9 amperes. There are five turns wound on the switch core, and so the value of I_2 is

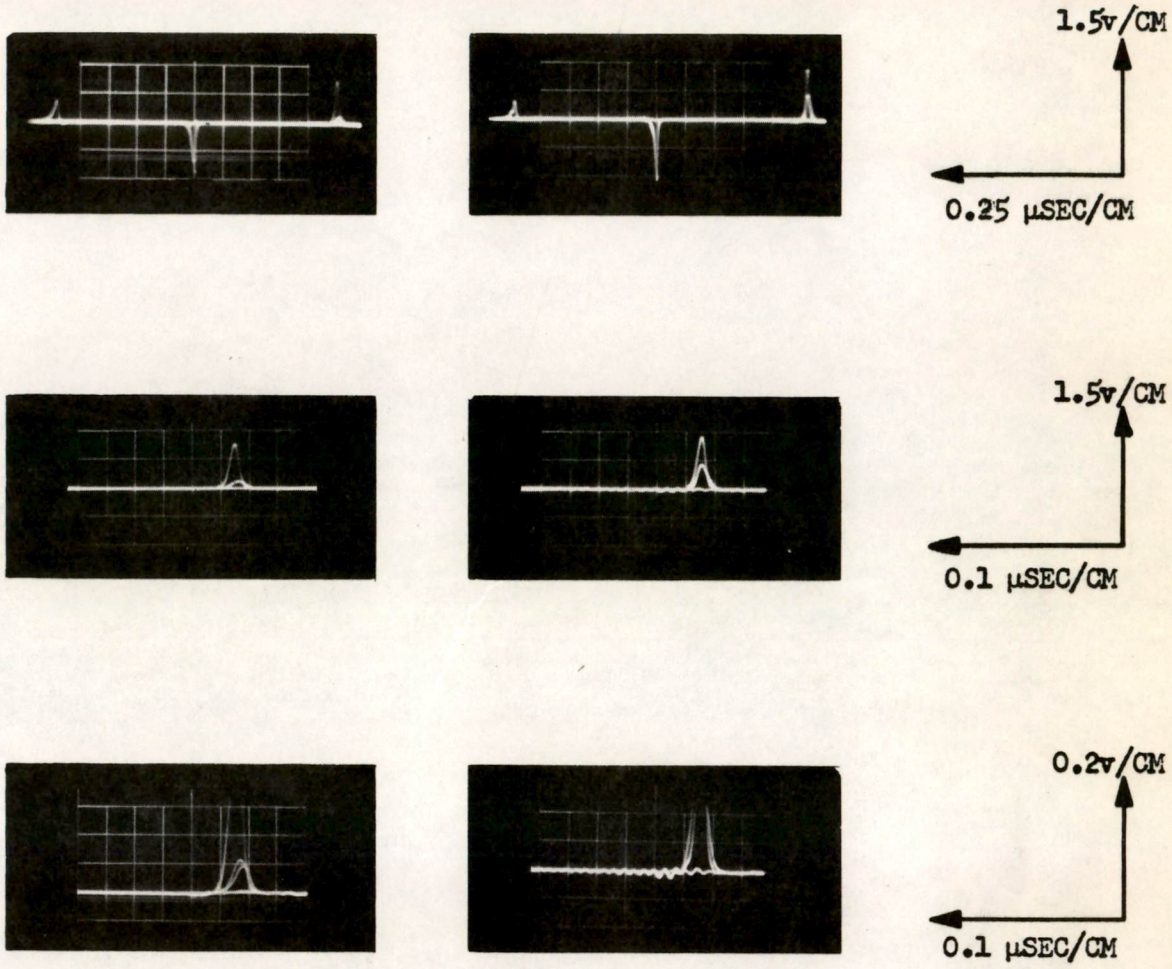
$$I_{2S} = (1.9)\ (5) + 2.35 \simeq 11.9 \text{ amp-turns.}$$

The High Speed Core Driver was capable of supplying only 1.7 amperes, or 8.5 amp-turns. This allowed safe operation although not, perhaps, the best possible operation.

The switch cores used were 11DCL-2-720H2L-1, sizes 1D264, 6 cores of F395 and 3 cores of F395. A switch with a very poor hysteresis loop, DCL-3-44 was used also; its size was 6F397.

The photographs of Figs. 3.20 to 3.25 show the memory core outputs obtained using various combinations of switch cores, loop resistances and cycle times. Table VII below, lists these outputs, and the output of combinations that are not shown pictorially.

The photographs and the tabulated results demonstrate that the ratios of ONE to half-select are, in general, extremely large. The values are about 200 to 1. This compares favorably to the ratio of about 60 to 1 obtained using the coincident current memory scheme

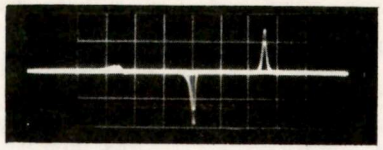


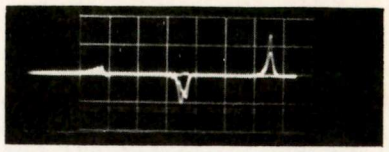
a. SWITCH CORE IS
11DCL-2-720H2L-1
SIZE 1D264
LOOP RESISTANCE = 0 OHMS
CYCLE TIME = 2.8 µSEC

b. SWITCH CORE IS
11DCL-2-720H2L-1
SIZE 6F395
LOOP RESISTANCE = 0 OHMS
CYCLE TIME = 2.8 µSEC

FIG. 3.20

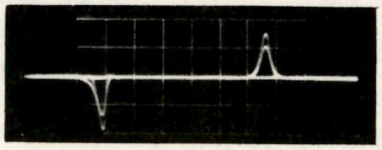
MEMORY CORE OUTPUTS
MEMORY CORE IS 11DCL-2-720H2L-1 SIZE 1F395
SWITCH CORE BIASES = 9.5 AMP-TURNS
SWITCH CORE EXCITATIONS ARE 8.5 AMP-TURNS FOR HALF-SELECT;
17.0 AMP-TURNS FOR FULL SELECT
ONE, ZERO, AND HALF-SELECTS ARE SUPERIMPOSED

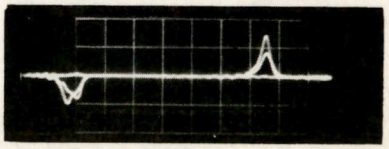




1.5v/CM

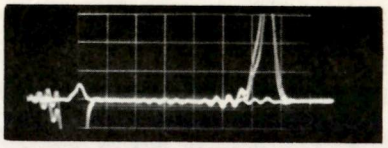
0.25 μSEC/CM





1.5v/CM

0.1 μSEC/CM



0.2v/CM

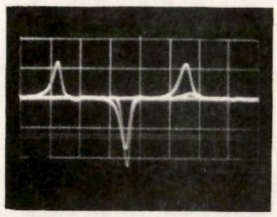
0.1 μSEC/CM

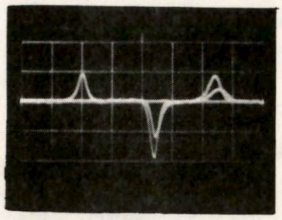
a. SWITCH CORE IS
11DCL-2-720H2L-1
SIZE 1D264
LOOP RESISTANCE = 0 OHMS
CYCLE TIME = 1.4 μSEC

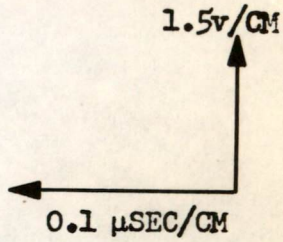
b. SWITCH CORE IS
11DCL-2-720H2L-1
SIZE 3F395
LOOP RESISTANCE = 0 OHMS
CYCLE TIME = 1.5 μSEC

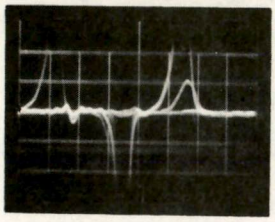
FIG. 3.21

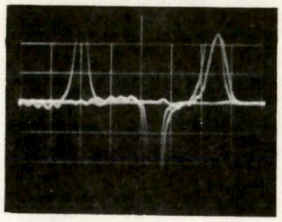
MEMORY CORE OUTPUTS
MEMORY CORE IS 11DCL-2-720H2L-1 SIZE 1F395
SWITCH CORE BIASES = 9.5 AMP-TURNS
SWITCH CORE EXCITATIONS ARE 8.5 AMP-TURNS FOR HALF-SELECT;
17.0 AMP-TURNS FOR FULL SELECT
ONE, ZERO, AND HALF-SELECTS ARE SUPERIMPOSED

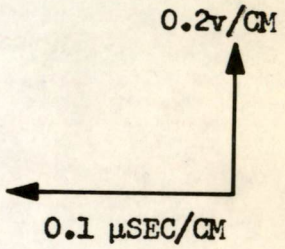










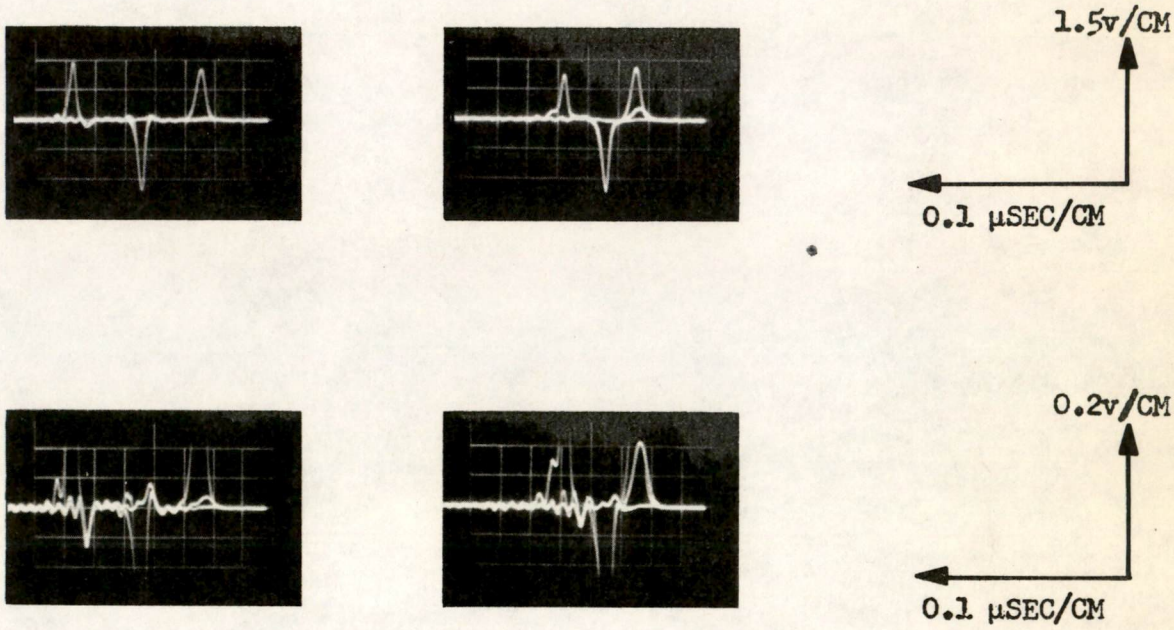


a. SWITCH CORE IS
11DCL-2-720H2L-1
SIZE 1D264
LOOP RESISTANCE = 1 OHM
CYCLE TIME = 0.5 μSEC

b. SWITCH CORE IS
11DCL-2-720H2L-1
SIZE 1D264
LOOP RESISTANCE = 2 OHMS
CYCLE TIME = 0.5 μSEC

FIG. 3.22

MEMORY CORE OUTPUTS
MEMORY CORE IS 11DCL-2-720H2L-1 SIZE 1F395
SWITCH CORE BIASES = 9.5 AMP-TURNS
SWITCH CORE EXCITATIONS ARE 8.5 AMP-TURNS FOR HALF-SELECT;
17.0 AMP-TURNS FOR FULL SELECT
ONE, ZERO, AND HALF-SELECTS ARE SUPERIMPOSED

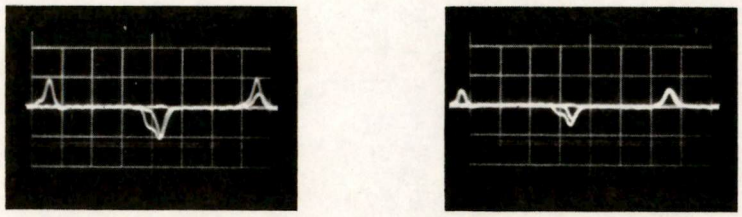


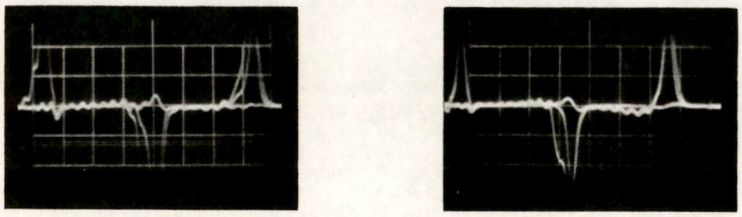
a. SWITCH CORE IS
11DCL-2-720H2L-1
SIZE 6F395
LOOP RESISTANCE = 1 OHM
CYCLE TIME = 0.5 μSEC

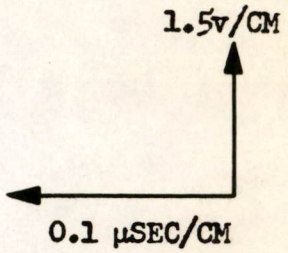
b. SWITCH CORE IS
11DCL-2-720H2L-1
SIZE 6F395
LOOP RESISTANCE = 1 OHM
CYCLE TIME = 0.3 μSEC

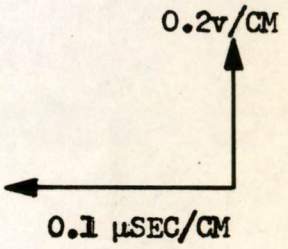
FIG. 3.23

MEMORY CORE OUTPUTS
MEMORY CORE IS 11DCL-2-720H2L-1 SIZE 1F395
SWITCH CORE BIASES = 9.5 AMP-TURNS
SWITCH CORE EXCITATIONS ARE 8.5 AMP-TURNS FOR HALF-SELECT;
17.0 AMP-TURNS FOR FULL SELECT
ONE, ZERO, AND HALF-SELECTS ARE SUPERIMPOSED







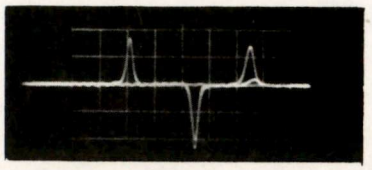


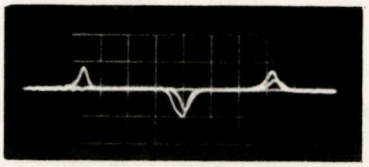
a. SWITCH CORE IS
11DC1-2-720H2L-1
SIZE 3F395
LOOP RESISTANCE = 1 OHM
CYCLE TIME = 0.8 μSEC

b. SWITCH CORE IS
11DC1-2-720H2L-1
SIZE 3F395
LOOP RESISTANCE = 2 OHMS
CYCLE TIME = 0.8 μSEC

FIG. 3.24

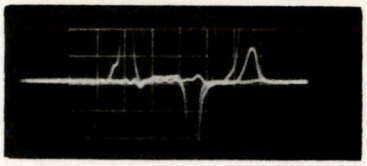
MEMORY CORE OUTPUTS
MEMORY CORE IS 11DC1-2-720H2L-1 SIZE 1F395
SWITCH CORE BIASES = 9.5 AMP-TURNS
SWITCH CORE EXCITATIONS ARE 8.5 AMP-TURNS FOR HALF-SELECTS;
17.0 AMP-TURNS FOR FULL SELECTS
ONE, ZERO, AND HALF-SELECTS ARE SUPERIMPOSED

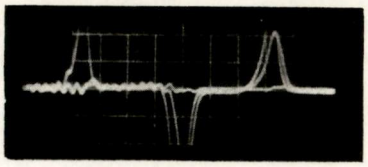




1.5v/CM

0.1 μSEC/CM





0.2v/CM

0.1 μSEC/CM

c. SWITCH CORE IS
11DCL-2-720H2L-1
SIZE 6F395
LOOP RESISTANCE = 2 OHMS
CYCLE TIME = 0.5 μSEC

b. SWITCH CORE IS
DCL-3-44
SIZE 6F397
LOOP RESISTANCE = 1 OHM
CYCLE TIME = 0.8 μSEC

FIG. 3.25

MEMORY CORE OUTPUTS.
MEMORY CORE IS 11DCL-2-720H2L-1 SIZE 1F395 SWITCH CORE BIASES = 9.5 AMP-TURNS
SWITCH CORE EXCITATIONS ARE 8.5 AMP-TURNS FOR HALF-SELECTS;
17.0 AMP-TURNS FOR FULL SELECTS
ONE, ZERO, AND HALF-SELECTS ARE SHOWN SUPERIMPOSED

TABLE VII

Memory Core Outputs as a Function of Switch Core, Loop Resistance and Cycle Time

Switch Core Material **	Loop Resistance ohms	Cycle Time μsec.	Full Select Voltage ONE	Full Select Voltage ZERO	Approximate Half Select Voltages ONE	Approximate Half Select Voltages ZERO	Ratios ONE/ZERO	Ratios ONE/Half-Select	Fig.
1 D264, 11DCL -2-720	0	2.8*	2.3	0.61	0.03	0.03	3.8	76	3.20
		1.4*	2.2	1.1	0.035	0.025	2.0	73	3.21
H2L-1	1	1.0	1.8	0.12	0.01	0.01	15	180	-
		0.5	1.8	0.24	-	-	7.5	-	3.22
		0.4	1.7	0.37	0.01	0.01	4.6	170	-
	2	0.8	1.2	0.6	0.01	0.01	2.0	120	-
		0.5	1.2	0.6	0.02	0.02	2.0	60	3.22
		0.4	1.2	0.6	0.02	0.02	2.0	60	-
6 F395, 11DCL- 2-720H	0	2.8*	2.7	1.4	0.015	0.015	1.9	60	3.20
		1.4*	2.8	1.8	0.03	0.03	1.6	94	-
2L-1	1	0.8	2.5	0.05	0.01	0.01	50	250	-
		0.5	2.6	0.09	0.01	0.01	29	260	3.23
		0.4	2.5	0.17	0.01	0.01	14.7	250	-
		0.3	2.6	0.5	0.02	0.02	5.2	130	3.23
	2	0.8	2.1	0.27	0.02	0.02	7.8	105	-
		0.5	2.1	0.3	0.02	0.02	7.0	105	3.25
		0.3	2.1	0.5	0.025	0.025	4.2	84	-
3 F395, 11DCL- 2-720	0	2.4*	2.1	0.7	0.02	0.01	3.0	140	-
		1.5*	2.1	1.2	-	-	1.8	-	3.21
H2L-1	1	0.8	1.4	0.7	0.01	0.01	2.0	140	3.24
		0.5	1.4	0.8	0.005	0.005	1.8	280	-
		0.3	1.4	1.1	0.005	0.005	1.3	280	-
	2	0.8	0.8	0.8	0.01	0.01	1.0	80	3.24
6 F397, DCL-3- 44	1	0.8	1.0	0.5	0.015	0.015	2.0	67	3.25
		0.5	1.0	0.6	0.01	0.01	1.7	100	-
		0.4	1.0	0.7	0.01	0.01	1.4	100	-

* ZERO's are disturb sensitive

** Digit before core size indicates the number of core bodies composing switch cores (e.g. 6F395 means 6 size F395 cores are one switch core).

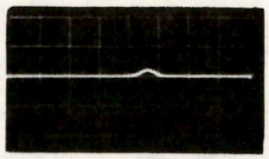
\- no picture shown

(in Chapter 2).

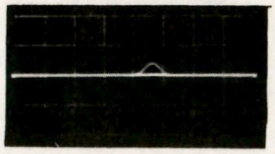
The ONE to ZERO ratios obtained using three cores per bit vary from 1.0 to 50. If the switch core used is 11DCL-2-720H2 L-1, size 6F395, the ratio is about 30 to 1, when the cycle time (read and write) is 0.5 microseconds. This is almost the same as the ONE to ZERO ratio found in the coincident current memory system. It should be realized that an improvement is possible utilizing the three core memory, if the cores are driven somewhat harder.

Table VII discloses the fact in each and every case, the ZEROs were disturb sensitive when there was no loop resistance. (The ONEs have never been found to be subject to this malady). The reason for this behavior is clear. The read cycle is brought to a conclusion at the same time that the write cycle is begun. The half-select currents in the two loops add and tend to push the memory core into the ONE state. When there is some loop resistance, the half-select currents are small and have no discernible effect on the memory core information content. However, with no loop resistance, these currents apparently are large enough, when added together, to move the core from the ZERO state. Fig. 3.26 shows the progressive deterioration of a ZERO as it is disturbed various numbers of times. This result was predicted in section C2 of this chapter. It was found that if the write pulses are delayed long enough, this disturb sensitivity is eliminated.

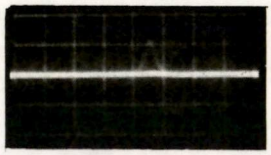
Reference is again made to Table VII and Figs. 3.20 to 3.25. It is observed that it is virtually impossible to obtain successful operation if R loop = 0 - for, aside from the fact that ZEROs deteriorate, the cycles must be long, and the ONE to ZERO ratios are never really



ZERO NO DISTURBS



ZERO 7 DISTURBS



ZERO 63 DISTURBS

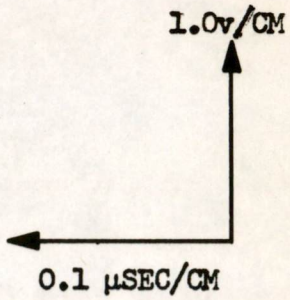


FIG. 3 .26

DESTRUCTION OF ZEROs BY HALF SELECT EXCITATIONS
SWITCH CORE IS 11DCL-2-720H2L-1, SIZE 1D264
MEMORY CORE IS 11DCL-2-720H2L-1, SIZE 1F395
LOOP RESISTANCE = 0 OHMS. BIAS = 9.5 AMP-TURNS
HALF SELECT EXCITATION = 8.5 AMP-TURNS;
FULL SELECT EXCITATION = 17.0 AMP-TURNS

good.

The results obtained when R loop = 2 ohms were satisfactory, but the loop currents are too small to obtain really outstanding results. When the switch core is very small (3F395), the memory core cannot be driven successfully. It was possible to obtain useful results when the cycle time is 0.5 microseconds.

The best results were obtained when R loop = 1 ohm, with excellent results for cycle times if in the range of 0.3 - 0.4 microseconds (Fig. 3.23). If the switch core is 6F395, and the cycle time is 0.4 microseconds a ONE to ZERO ratio of about 15 was obtained, the ONE to half-select ratio was 250. There was no evidence of disturb sensitivity. In general it was found that the ratio of desirable to undesirable outputs improves as the cycle time is lengthened.

Data obtained on the size of ONEs as a function of current driving the switch core is presented in Table VIII.

TABLE VIII

Fully Selected ONEs as a Function of Switch Core Driving Current. Cores are 11DCL-2-720 H2L-1; Switch Core = 1D264; Memory Core = 1F395 Loop Resistance = 1 ohm.

Driving Current Ampere-turns	Full Select ONE output Voltage volts
13	0.75
14	1.1
15	1.5
16	1.9
17	2.2

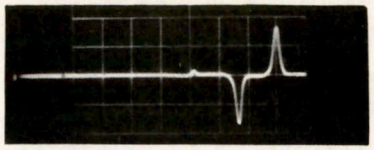
The data of Table VIII results in a straight line whose slope,

$$\frac{\Delta V_{out}}{\Delta N_1 \, i_{in}} = 0.37 \text{ ohms}$$

(Core B was removed from the circuit.) This data tends to show that connecting two piece-wise linear cores by a loop results in a piece-wise linear system. The output impedance of this connection should be $\frac{(FM)\,(FS+L)}{FM+FS+L}$. It has been found that FM = 0.5 ohms, FS = 1.3 ohms, and L = 3 ohms. This means that the expected output impedance should be $\frac{(.5)\,(4.3)}{.5+4.3} = 0.45$ ohms. The error observed is not excessive, considering the nature of the elements which are in the circuit.

An attempt was made to drive a metallic memory core (Molybdenum Permalloy: 1/8 mil x 3/16" diameter x 1/8" wide x 20 wraps), and the results were unsuccessful. The reason is that it was impossible to write a ZEROinto the core -- that is, the memory core held a ONE, independent of the information placed in it (Fig. 3.27). A study of these photographs discloses a long negative overshoot following the write ZERO pulse. Apparently, when an attempt is made to insert a ZERO into the core, the core is soon switched back to the ONE state. An investigation of this phenomenon revealed that the cause of this behavior was the fact that when the memory core was switched, a current was induced in the secondary, and it was this current that switched the memory core slowly back to the ONE state.

A detailed analysis follows in which reference will be made extensively to Figs. 3.28 and 3.29. Assume that an attempt is made to write a ZERO into core M. The read cycle has been completed, and the

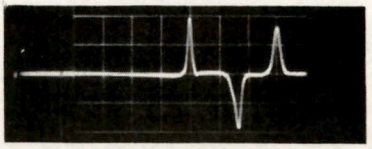


READ AND WRITE ONE

ONE = 2.5 VOLTS

1.5v/CM

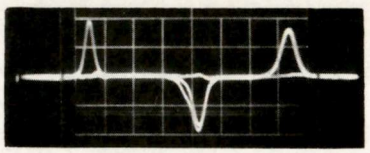
0.25 μSEC/CM



READ AND WRITE ZERO

ZERO = 2.4 VOLTS

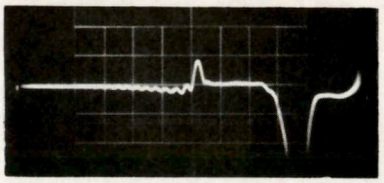
(NOTE OVERSHOOT AFTER LAST PULSE)



1.5v/CM

0.1 μSEC/CM

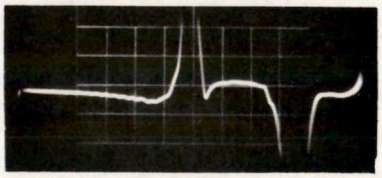
READ AND WRITE ONE AND ZERO SUPERIMPOSED.



WRITE ONE

0.2v/CM

0.1 μSEC/CM



WRITE ZERO

(NOTE LONG OVERSHOOT)

FIG. 3.27

READ AND WRITE ONE AND ZERO IN A MOLYBDENUM PERMALLOY MEMORY CORE (1/8 MIL x 3/16" DIAMETER x 1/8" WIDE x 20 WRAPS) SWITCH CORE IS 11 DCL-2-720H2L-1, SIZE 1D264. R LOOP = 1 OHM, BIAS=9.5 AMP.- TURNS

A-61338

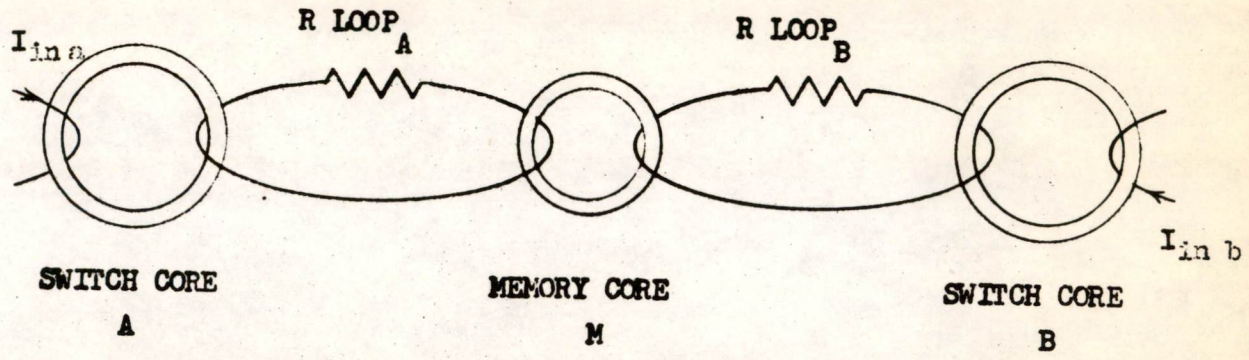


FIG. 3.28

THE ALLIGNMENT OF THE CORES IN THE BASIC MEMORY UNIT

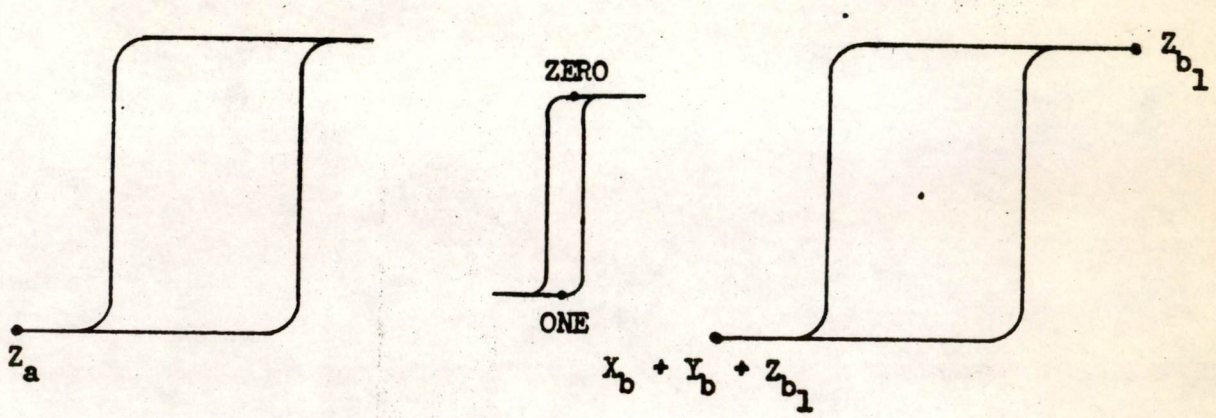


FIG. 3.29

HYSTERESIS LOOPS OF THE CORES USED IN THE MEMORY UNIT

memory core rests in the ONE state (assume the pulse sequence of Fig. 3.5 is used). Core B rests at point $X_b + Y_b + Z_{b1}$ on its hysteresis loop, and core A is at Z_a on its loop. When the excitation driving core B is turned off, it switches to Z_{b1}, inducing a clockwise current in loop B which switches core M to the ZERO state. The switching of core M induces a clock-wise current in loop A. This current drives core A in the direction towards switching, but it is too feeble to have much effect on A. For some reason, the current in loop B dies out very rapidly, whereas the current in loop A does not. The current in loop A continues to circulate and it switches core M from the ZERO state back to the ONE state. This result is possible only because a metallic memory core has been used -- a property of the material is its extremely low coercive force. It may well be that this behavior was caused by some difference between the two loops themselves -- loop B may have a shorter time constant than loop A has. If there was some other reason, then an attempt to write a ONE should yield a ZERO. This was not observed.

The important conclusion to be drawn from the above is that the memory cores should not be driven so heavily that the current induced in the secondary exceeds the coercive force of the memory core. It does not seem probable that any difficulty would be encountered if the two loops were identical. However, it is unlikely that two exactly equivalent loops, each containing highly nonlinear elements, could be easily constructed. This same result is also possible if the memory core is a ferrite core, but it must be driven much more heavily than the Mo Perm core was driven (because of its high coercive force) in order

to achieve the same undesirable result. It was not possible to do this using the equipment on hand.

CHAPTER 4

CONCLUSIONS

The data and photographs presented in Chapter 3 show that a memory unit based on the principles of external selection can be expected to operate satisfactorily.

Several safeguards must be taken in order to assure successful operation. The loops of wire coupling the switch cores to the memory core must have some resistance in them in order to lessen the half-select switch currents that excite the memory core, and in order to hasten the decay of the loop currents. The switch cores should not be driven so heavily that half-select outputs switch the memory core. The cycle time should not be made so short that a current pulse does not have an opportunity to decay before a second current pulse is applied to the same loop. The switch core must be large enough to control the memory core, but it must not be so large that noise outputs switch the memory core.

The three-core-per-bit memory compares with the existing coincident-core memory as follows.

a. With present core materials, the new memory is considerably faster than the coincident-current model. Much, or all of this speed advantage might, however, be overcome should very fast cores for the coincident-current application be developed and put into use; such faster cores could be produced at the cost of increased coercivities and consequent increases in required driving currents.

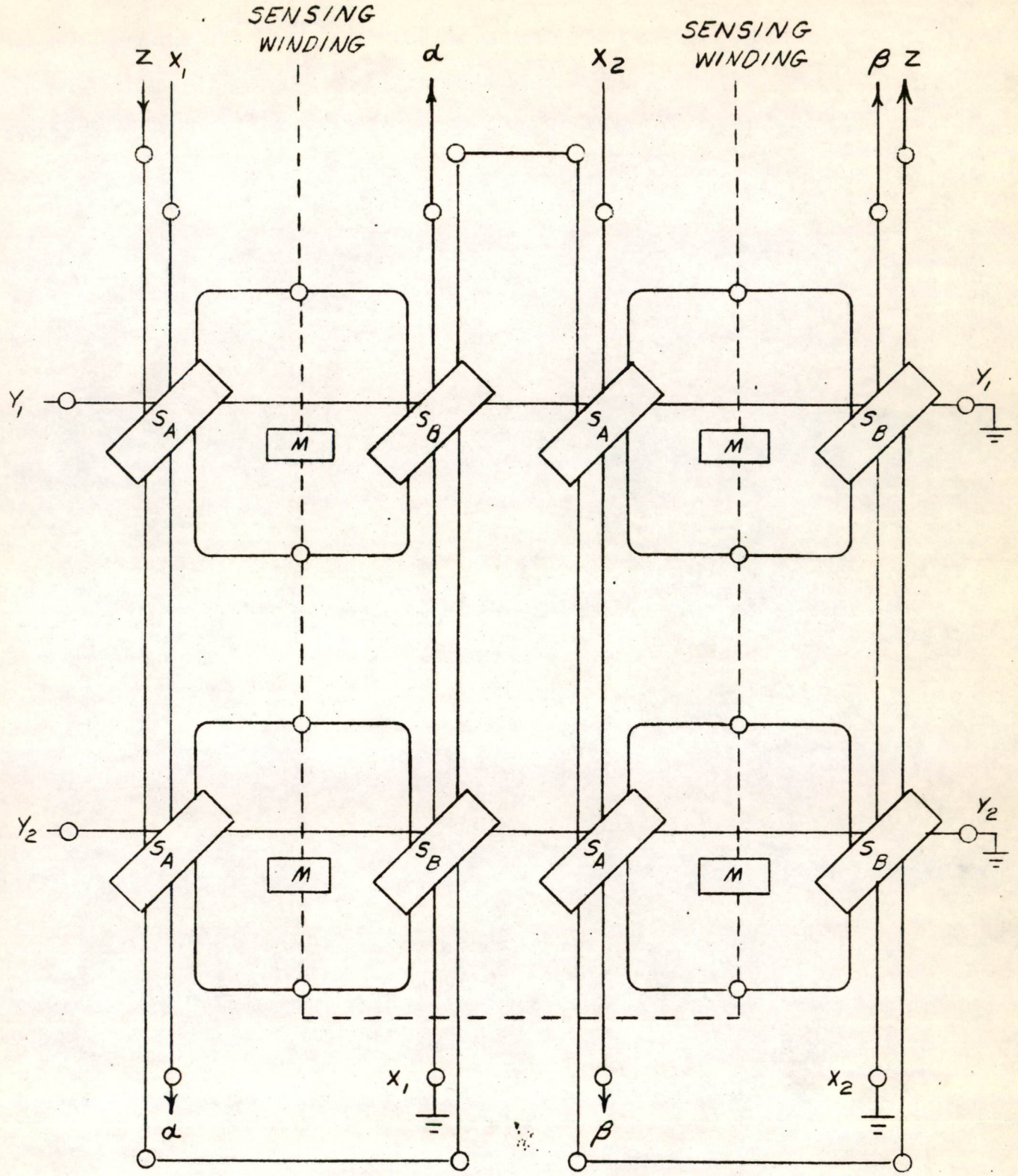
b. An improved selection-current ratio exists in the new memory; it may be as high as 10:1 as compared to 2:1 in the coincident-current system. The result is a slightly improved ONE-to-ZERO

signal ratio, a greatly improved ONE-to-half select ratio, wider operating margins, or wider tolerances on core characteristics. Wider temperature margins may allow higher peak operating frequencies for the memory.

c. The increased number of cores (by a factor of 3) and the extra construction problems represent distinct disadvantages for the new system, while a very rough estimate indicates that the amount of surrounding electronic equipment is about the same.

To put the ideas discussed in this report into practice by building a memory based on the external selection principle presents a large number of problems, many of which have not yet been solved. One of these is the manner in which the memory is to be constructed. A memory plane using three cores per bit cannot be built in the same way that a coincident-current memory plane is built. Each memory plane would require two adjoining switch-core planes and it would be necessary to couple each memory core to its corresponding switch cores. (Figure 1.3) The difficulties that would be encountered in this type of construction are overwhelming. Using a different approach, a memory "plane" consisting of 256 bits of information (3 x 256 = 768 total cores) is now being built at the laboratory. The construction method is illustrated by the four-bit (two-by-two) memory "plane" shown in Figure 4.1. The lugs are mounted on a phenolic board. The switch cores and the lines driving them are mounted on the upper side of the board, but the memory cores and sensing winding are below it. This is done to minimize confusion. There are some interesting aspects to this design, and Figure 4.1 will be referred to again.

Study of any one bit of the memory plane of Figure 4.1 reveals that



NOTE:
ALL COMPONENTS ARE MOUNTED ON PHENOLIC BOARD.
ALL DRIVING LINES ARE ABOVE THIS BOARD. MEMORY CORE, M AND SENSING WINDING ARE BELOW BOARD.

FIG. 4.1

TWO-BY-TWO MEMORY "PLANE" DEMONSTRATING THIS WIRING TECHNIQUE TO BE USED IN BUILDING A 16 BY 16 PLANE

only one X winding is to be used for both switch cores; likewise, only one Y winding is to be used for both switches. This winding scheme is possible if the different driving lines carry both positive and negative current pulses. The proposed method of driving the memory is shown symbolically in Figure 4.2. The three-winding driving transformers serve two purposes -- they are used to step up the current available for driving the switch cores, thereby relaxing the current output requirements of the read and write drivers, and they make it possible to obtain both positive and negative pulses on the lines that actually drive the switches. (Note, in Figure 4.1, that in order to switch any of the cores, S_A, the current in the X lines must flow upwards and the Y current must flow from right to left. These currents will not switch core S_B, but will merely drive it further into saturation. When S_B is to be switched, the X current must flow downward, and the Y current must flow from left to right. These currents will move S_A further into saturation.)

It has been found, in Chapter 3, that it is necessary to place some resistance in the loops of wire coupling the switch cores to the memory core. In the experimental arrangement it was convenient to use actual resistors that could be readily connected in and out of the coupling loops. In an actual memory unit resistors would be awkward. An attempt is being made to build the first plane using resistance wire encircling the memory core, and passing through the two switch cores. In Figure 4.1, the loop of wire encircling the memory core, and passing through the two switch cores is the resistance wire.

In the design to be tried out, the sensing winding serves a dual purpose. It is not only used to detect memory-core output voltages, but it also serves to carry the loop currents through the memory core. All,

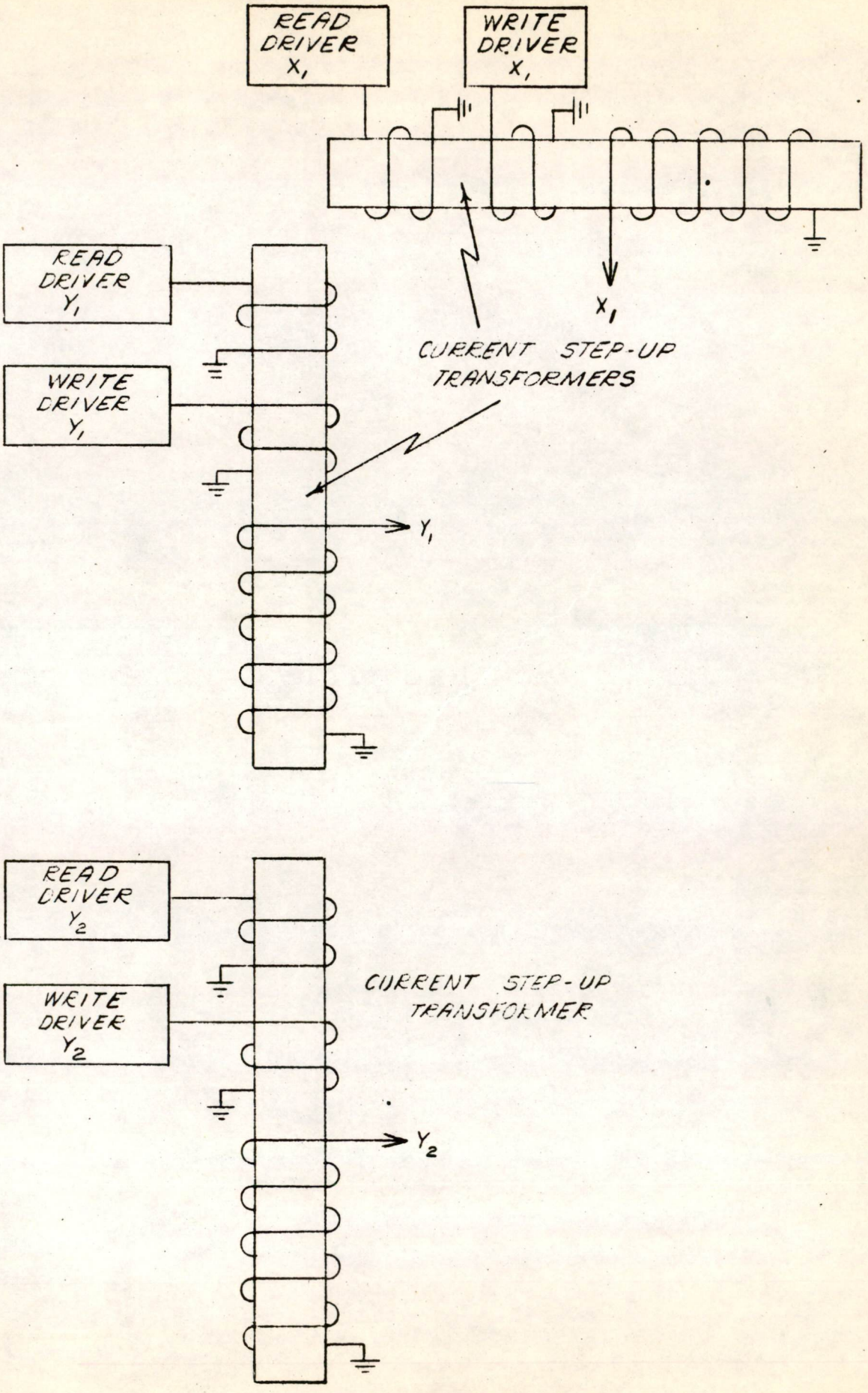


FIG. 4.2

PROPOSED METHOD OF DRIVING SWITCH CORES SHOWN IN FIG. 4.1

or nearly all, of the loop current should pass through the memory core; very little current from loop A should flow into loop B, and vice versa. This requirement means that the sensing winding should not be made of resistance wire. It should be noted that the sensing winding used in Figure 4.1 is not of the cancelling type that is used in the coincident-current memory planes. That is, the winding is not arranged so that memory-core outputs due to "noise" currents from half-selected switch cores tend to cancel each other. It is hoped that the extremely small memory-core "noise" voltages will permit a non-cancelling sensing winding to be used. In the event that this is not satisfactory, it would not cause an undue amount of trouble to revise the plane so that the sensing winding is of the cancelling type.

It was discovered in Chapter 2 that about 10 volts is induced in the driven winding of a heavily selected switch core such as 11DCL-2-720H2L-1, size 1D264 or 6F395 (the only switch cores which were able to satisfactorily drive the memory core size 1F395). In a memory with a 16-digit word length a driver must switch 16 cores, and the back voltage that would result is 16 x 10 = 160 volts. This is too much to expect of a current source. In order to overcome this difficulty it is necessary to use much smaller switch cores. If these small switch cores are to successfully operate the memory, the memory cores themselves must be reduced, fluxwise, to a size such that present-size memory cores may be used in the switch. A heavily driven small switch core has a back voltage of 3 volts; 16 of these switch cores would induce a total voltage of 16 x 3 = 48 volts. This is an improvement over the figure required when large switches were used, and makes it easier to build a driver capable of driving the load.

Output voltages would be considerably smaller than those obtained during the course of the experiments run in Chapter 3, but it is probable that outputs would still be larger than those obtained in the coincident-current memory.

The core memory utilizing external selection is essentially a high-speed memory. In attempting to put this feature into practice it will be necessary to read and write often. A core dissipates energy when it is switched; the more frequently it is excited, the greater is the average power lost in it. The average power lost in an ideal switch core (Figure 2.1) that has no load may readily be expressed in terms of its properties. Let it be assumed that the residual flux is ϕ_r, that the input current is a square wave of amplitude I_{in}, that T is the time between successive cycles of operations, and that τ is the switching time of a core. The flux change during switching is

$$2\,\phi_r = \int_0^{\tau} v\,dt \qquad (4.1)$$

where v is the output voltage of the core. The average power dissipated in a switching core is

$$P_{av} = \frac{2}{T} \int_0^{\tau} v\,i\,dt = \frac{2\,I_{in}}{T} \int_0^{\tau} v\,dt$$

$$= \frac{4\,I_{in}\,\phi_r}{T} \qquad (4.2)$$

Equation (4.2) demonstrates that the power lost in a core is directly proportional to the product of the input current and the residual flux. In order to switch the core rapidly, I_{in} must be kept large. However, it is possible to reduce ϕ_r and, therefore, P_{av}, by using small switch cores, as has been suggested previously.

No extensive tests were run on the behavior of the core when it is "batted" back and forth rapidly, but the results that were obtained were encouraging. A memory core was switched at a repetition frequency of 100 kilocycles, and it was driven very heavily. There was no evidence of any failure due to heating. The core driver (Appendix B), was not capable of being used at a rate exceeding 100 KC.

If a memory of 256 words is built, and the word length is 16 bits, the length of the driving leads would be great. The inductance of these wires and of the partially selected cores would be very large, and because of the induced back voltage, it might be impossible to achieve large driving currents that rise in 0.05 microseconds. Let it be assumed, for example, that the inductance of the wires and cores is about 10 microhenries. If an attempt is made to drive the cores with 5 amperes on the X and Y lines, with rise and fall times of 0.05 microsecond, then the back voltage peak seen at the transformer secondary would be $10 \times 10^{-6} \times \frac{5}{.05 \times 10^{-6}} = 1000$ volts; at the primary the voltage would be even higher. This is a problem that will require a great deal of serious thought and hard work before it can be solved.

The successful operation of a full-size, fast, magnetic-core memory with external selection depends upon solution of the aforementioned problems.

Appendix A

Equivalent Circuit of Partially Selected Switch Core.

The core of Fig. 2.5 is put through two tests -- an open circuit test and a short circuit test (Fig. A.1 and A.2) -- in order to help determine its parameters. The piecewise linear hysteresis loop is shown in Fig. 2.6, and this characteristic insures the fact that the partially selected core has an equivalent circuit in which all elements are linear. Actually, this equivalent circuit (Fig. 2.7) consists merely of the leakage inductances L_{L1} and L_{L2} and of the magnetizing inductance, L_m. It is desired to find L_A, and L_C and L_C in terms of these parameters and the turns on the core.

L_A is the primary leakage inductance referred to the secondary, and so $L_A = \left(\frac{N_2}{N_1}\right)^2 L_{L1}$

L_B is the secondary leakage inductance, and it is equal to L_{L2}.

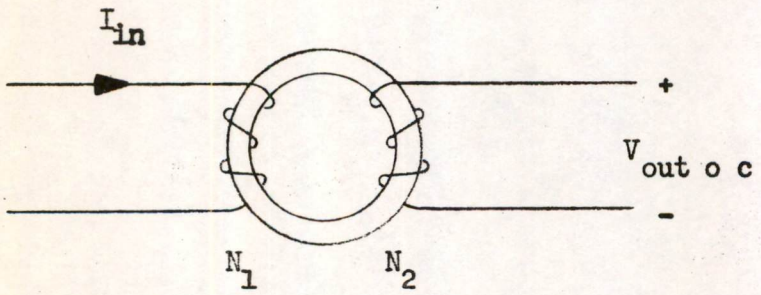
L_C may be determined in terms of the magnetizing inductance, L_m, by neglecting the leakage inductances (which are relatively small), and performing the open circuit and short circuit tests.

The open circuit test reveals that

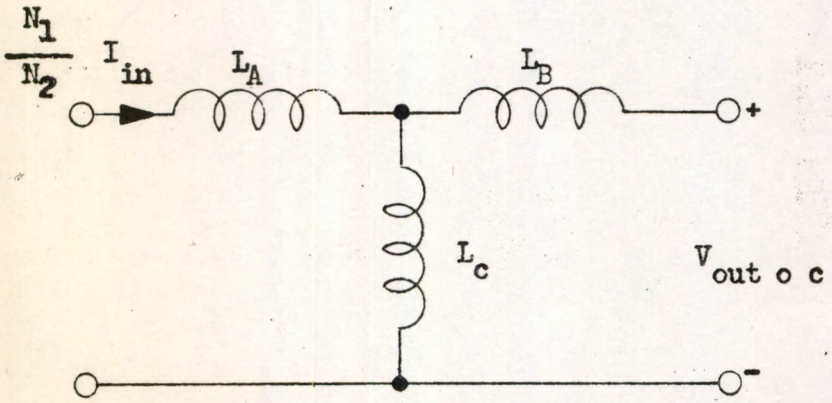
$$\frac{V_{out\ o.c.}}{N_2} = L_m S (N_1 I_{in}) \qquad (A.1)$$

Whereas the short circuit test leads to

$$N_1 I_{in} = N_2 i_{s.c.} \qquad (A.2)$$



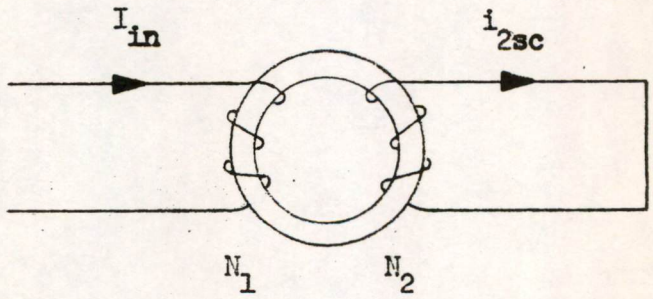
a. CORE CIRCUIT



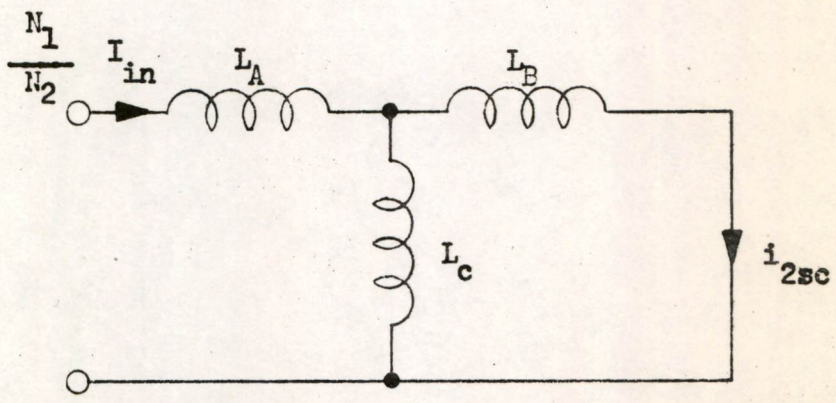
b. EQUIVALENT CIRCUIT

FIG. A.1

OPEN CIRCUIT TEST OF SWITCH CORE



a. CORE CIRCUIT



b. EQUIVALENT CIRCUIT

FIG. A.2

SHORT CIRCUIT TEST OF SWITCH CORE

The Thevenin equivalent output impedance is

$$Z_{out} = \frac{V_{out\ o.c.}}{i_{2\ s.c.}}$$

From equations (A.1) and (A.2) it is found that

$$Z_{out} = L_c S = N_2^2 L_m S \qquad (A.3)$$

or

$$L_c = N_2^2\ L_m$$

The driving current is $(N_1/N_2)\ I_{in}$ when reflected to the secondary.

APPENDIX B

HIGH SPEED CORE DRIVER

Work on this thesis using the Mod V Core Driver was frustrating, partially due to the relatively slow rise time of this driver, but mainly because of its extremely slow fall time. It was found that the cores were switched before the current through them had risen to its final value. The result was the inability to take any quantitative data on the operation of the memory system. The solution attempted was to build a driver capable of rising and falling more rapidly than the Mod V does.

Fig. B.1 shows a block diagram of the core driver. The first pulse is applied to Pulse Amplifier 1, which has two outputs from its three-winding output transformer - one positive and one negative. This sets the slave flip-flop whose output rises as rapidly as the rise time of the applied pulse. The second pulse applied to Pulse Amplifier 2 clears the flip-flop in the same manner. A trapezoidal wave is applied to a buffer amplifier which has the ability to rise and fall rapidly. The low impedance output of the buffer amplifier is used to drive four 6CD6's in parallel. The output is taken from the plates of the 6CD6's and is greater than 1.5 amps in the negative direction; it rises and falls in less than 0.1 microsecond. This current amplifier stage is very much like that found in the Mod V core driver.[10, 11]

The outputs of the flip-flop and the buffer amplifier (Figs. B.4 and B.6) are trapezoidal in order to achieve a rectangular current output. The reason for this situation is the RC combination in the cathodes of the current amplifier tubes (time constant = 0.1 microsecond). If the flip-flop output were rectangular then the current amplifier would have

an overshoot (Fig. B.9). The RC combination is required to prevent oscillations in the output.

1. Slave Flip-Flop[12]

The fast operation of the high-speed core driver (Fig. B.2) is due to the ability of the slave flip-flop to change states as rapidly as the rise times of the input pulses (for 0.1 microsecond input pulses, the flip-flop can be set in 0.05 microsecond).

In the quiescent condition V2A is on and V2B is off. The output voltage is taken from the plate of V2A, which is normally clamped at -215 volts (in order to hold the current amplifier stage cut off).

The application of a positive 0.1 μsec pulse at input 1 of pulse amplifier 1, results in the application of a positive pulse at point A and a negative pulse at point B (Figs. B.1, B.2, B.3). The diodes, CR4 and V3, pass these pulses and turn V2A off and V2B on rapidly, but only partially. The switching operation finishes slowly by means of the feedback loops. The reason for this peculiar mode of operation has already been explained - - in order to achieve a rectangular current output, the flipflop output must be trapezoidal.

The waveform at the cathode of V3 (flip-flop output) is shown in Fig. B.4 (the d.c. level is -215 volts). The waveform at the plate of CR4 is shown in Fig. B.5 (d.c. level is -140 volts). This waveform has a dent in it because the diode's recovery time is not zero (i.e. - some time is required before the crystal diode can switch from the low forward resistance to the high back resistance). A dent such as this could not be tolerated in the output, and so a vacuum diode, V3, rather than a crystal is used. The capacitance from plate and grid to cathode of the 5965 is large compared to that of a germanium diode, however, and this could cause

a dent in the output waveform caused by coupling of the pulse's trailing edge (from A) through this capacitance to the output. Two sections in series minimize this effect, and the addition of C15 at their junction helps further to eliminate the dent.

The flip-flop is switched back to its original (steady) state by the application of a positive pulse at input 2 (Figs. B.3C and D show the pulses at points C and D). In this case, a dent in the output of the flipflop (Fig. B.4) is of no consequence, due to the fact that the current amplifier stage is well cut off when the flip-flop is down. Thus CR5 may be a germanium rather than a vacuum diode.

The current output is shown in Fig. B.8. The amplitude is 1.8 amps and the rise and fall times are each about 0.05 μsec.

The amplitude of the output is controlled by varying the upper clamp voltage of V2A from -150 (maximum output) to -215 (no output). Unfortunately the amplitude control problem is not solved as simply as the above indicates. In order to obtain a rectangular output pulse, the size of the input pulse at point A must be carefully controlled. If the pulse at A is too large, the output appears like Fig. B.9; if it is too small, the output is like Fig. B.10. The reason for these distorted waveforms follows: The leading edge of the trapezoidal flip-flop output is almost the same height as the pulse at A. The output then approaches the clamp voltage almost linearly. If the slope is too small (pulse at A too large) then the grids of the 6CD6's do not rise as rapidly as their cathodes and, as time progresses, the current output decreases to its steady value (Fig. B.9). If the slope is too large (pulse at A too small), then the grids of the 6CD6's rise more rapidly than the cathodes and the current output slowly increases to its final value after the initial jump (Fig. B.10). In the

ideal case (Fig. B.8), the slope of the trapezoid allows the 6CD6 grids to rise just as rapidly as the cathodes rise, resulting in a rectangular output.

Thus, the method of varying the amplitude of the output wave is to observe it and vary both the "amplitude control" (which sets the upper d.c. level of the flip-flop output), and the "input 1 control" (which varies the sizes of the pulses at points A and B).

Fig. B.11 shows a 0.1 μsec, 2.1 ampere pulse output from the core driver. This demonstrates the speed with which this circuit operates, for the slave flip-flop has been set and cleared in about 0.1 μsec.

Fig. B.12 shows a 1.8 μsec, 1.8 ampere square wave output. This demonstrates the ability of the circuit to hold a fixed output for a relatively long period of time, despite the necessity for using a peculiarly shaped output from the flip-flop.

2. Buffer Amplifier

The output voltage of the buffer amplifier used in this core driver rises and falls rapidly (Fig. B.6). When the flip-flop output is down (-215 volts), both the upper and lower tubes (V4) conduct fairly heavily. The plate waveform of the upper tube is shown in Fig. B.7.

Upon the application of the rapidly rising edge of the trapezoidal wave to the grid of the upper tube, a large slug of current is drawn, dropping the plate voltage of the upper tube to about -73 volts (Fig. B.7); the lower tube is immediately cut off by the feedback arrangement. This means that all the current drawn is used to charge stray wiring capacity and so the cathode follower output rises rapidly. Following this there is an increase in bias on the upper tube, and a resulting increase in its plate voltage, turning the lower tube on again, but not heavily. Part of

the current now drawn continues to charge the capacity (resulting in the steadily increasing voltage of Fig. B.6); the rest flows through the lower tube.

When the input to the buffer amplifier suddenly drops, the upper tube tried to go off, but the following circumstances prevent this from happening. The plate voltage of upper tube rises and this results in a large current flowing through the lower tube, whose grid is capacitatively coupled to the plate of the upper tube. This current discharges the wiring capacity, and so the output of the buffer amplifier is forcibly pulled down. The upper tube cannot turn off completely because its cathode falls almost as fast as its grid does.

The remainder of the circuit, the pulse amplifiers[13] and the current amplifier[10, 11], present no material that is not well-known, and so no description is given of their operation.

It is to be noted that all waveforms shown were made using a Tektronix 514 oscilloscope in which the input was taken directly to the vertical deflection plates of the scope.

A-47175

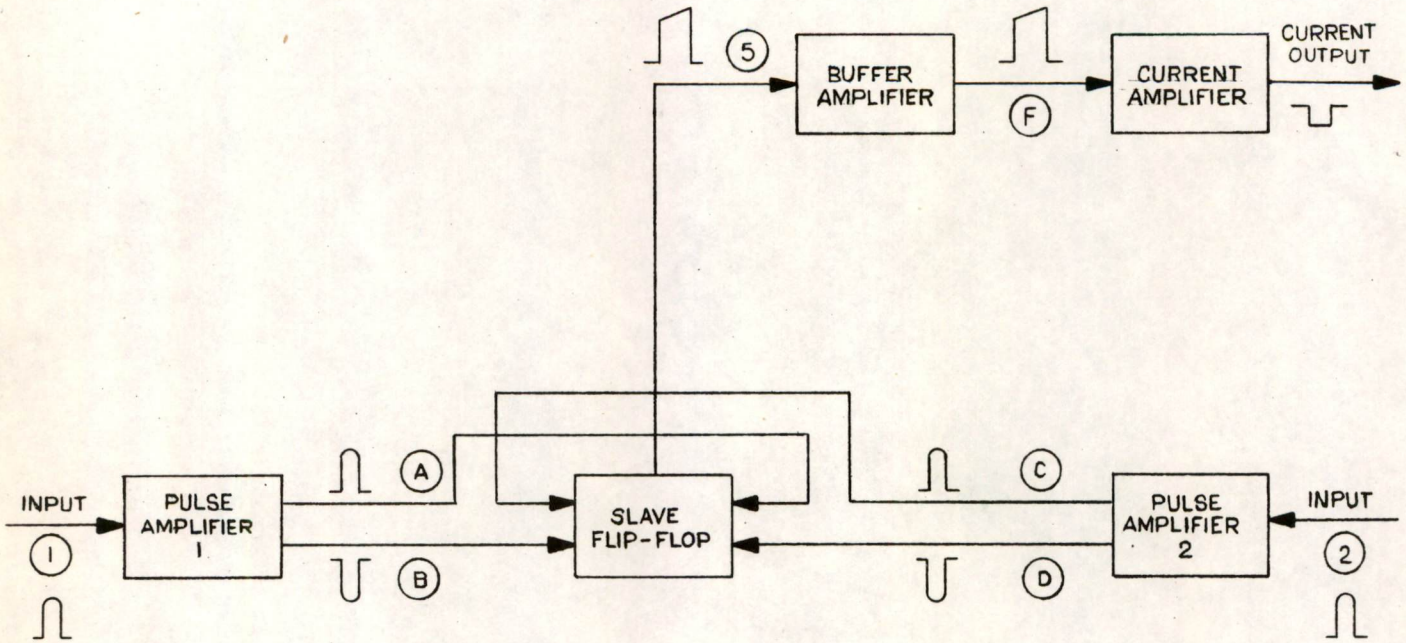


FIG. B1

BLOCK DIAGRAM OF HIGH SPEED CORE DRIVER

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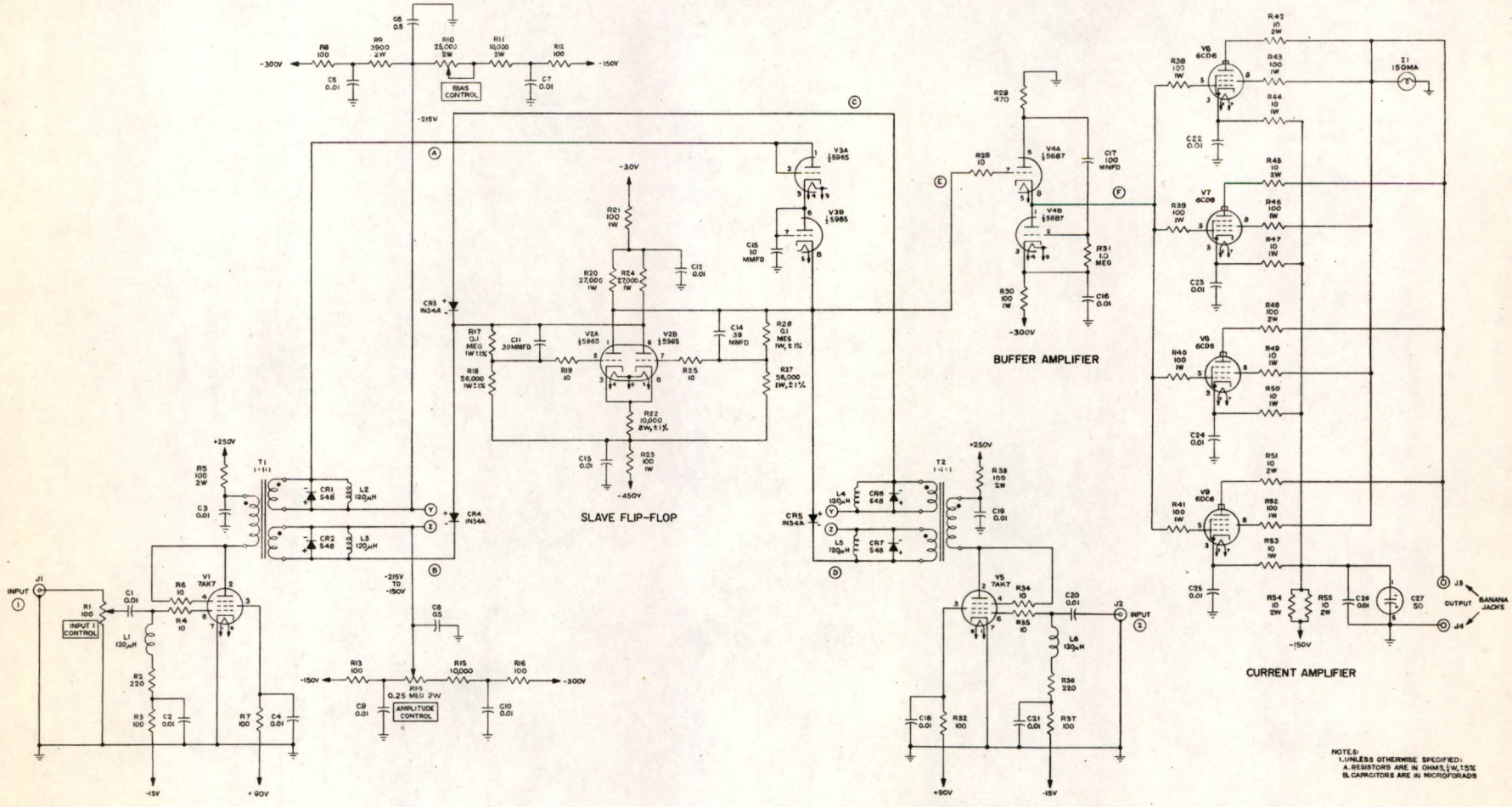


FIG B2

SCHEMATIC OF HIGH SPEED CORE DRIVER

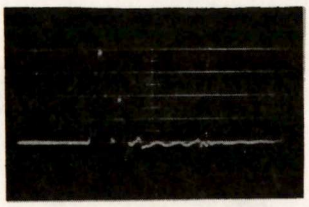


FIG. B3A
VOLTAGE AT POINT A
CORRESPONDING TO FIG. B8

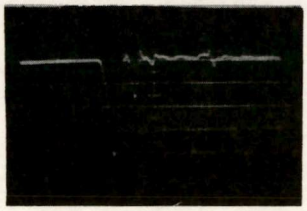


FIG B3B
VOLTAGE AT POINT B
CORRESPONDING TO FIG. B8

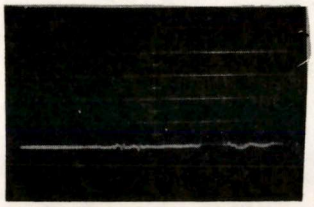


FIG. B3C
VOLTAGE AT POINT C
CORRESPONDING TO FIG. B8

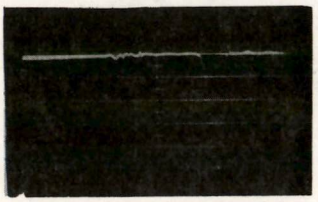
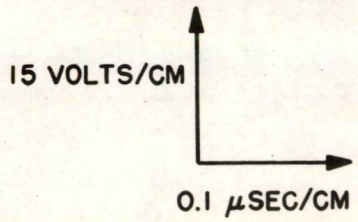


FIG. B3D
VOLTAGE AT POINT D
CORRESPONDING TO FIG. B8



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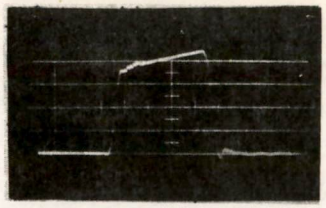


FIG. B4
FLIP-FLOP OUTPUT
(WAVEFORM AT CATHODE OF V3)
CORRESPONDING TO FIG. B8
DC LEVEL = -215 VOLTS

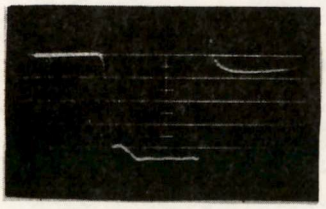


FIG. B5
WAVEFORM AT PLATE OF CR4
CORRESPONDING TO FIG B8
DC LEVEL = -140 VOLTS

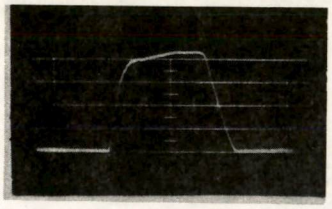


FIG. B6
BUFFER AMPLIFIER OUTPUT
CORRESPONDING TO FIG. B8
DC LEVEL = -210 VOLTS

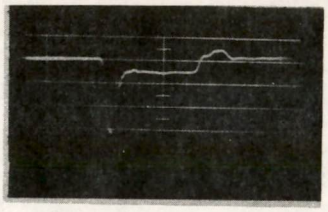
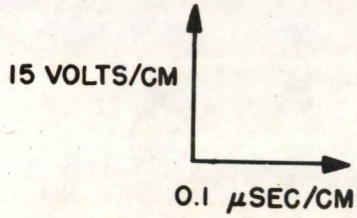


FIG. B7
BUFFER AMPLIFIER PLATE
WAVEFORM
CORRESPONDING TO FIG. B8
DC LEVEL = -27 VOLTS



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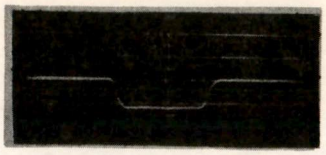


FIG. B8
BEST CORE DRIVER OUTPUT CURRENT (THROUH 10Ω LOAD)

FIG. B9
CORE DRIVER OUTPUT CURRENT (THROUGH 10Ω LOAD) WHEN INPUT PULSE AT 1 IS TOO LARGE

FIG. B10
CORE DRIVER OUTPUT CURRENT (THROUGH 10Ω LOAD) WHEN INPUT PULSE AT 1 IS TOO SMALL

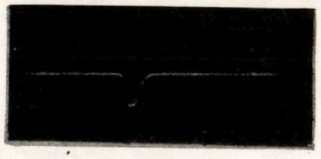


FIG. B11
0.1μSEC CORE DRIVER OUTPUT CURRENT PULSE

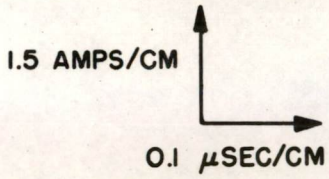
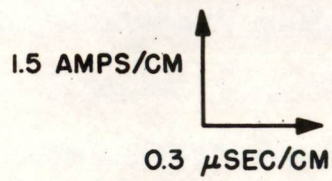


FIG. B12
1.8μ SEC CORE DRIVER OUTPUT PULSE



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Appendix C

The Linearized Coincident Current Memory Cell

The linearized memory core volt-ampere characteristic of Fig. 2.25 will be referred to throughout this derivation. It will be assumed that both N_1 and N_2 are unity.

In the region below the break in the curve the core is half selected, and the relation between input current and output voltage from a memory core is

$$V_{\text{out half-select}} = R_{HM}\, i_{\text{in H}} \quad (i_{\text{in H}} \leqq I_e) \tag{C.1}$$

If the memory core holds a ZERO, then in the region beyond the break(when the core is fully selected), the voltage output is

$$V_{\text{out ZERO}} = R_{HM}\, i_{\text{in F}} \quad (i_{\text{in F}} \geqq I_c) \tag{C.2}$$

If the memory core holds a ONE, and is fully selected, the output voltage assumes the form

$$V_{\text{out ONE}} = R_{HM}\, I_c + R_{FM}\, (i_{\text{in F}} - I_c) \quad (i_{\text{in F}} \geqq I_c) \tag{C.3}$$

It is noted that $i_{\text{in F}} = 2\, i_{\text{in H}}$. In order to obtain the best possible operation, i_{in} should be made as large, within its assign-constraints. The maximum value of $i_{\text{in H}}$ is I_c, and so the maximum value of $i_{\text{in F}}$ is $2I_c$.

These conclusions lead to the following results:

$$V_{out\ half\text{-}select} = R_{HM}\, I_c \qquad (C.4)$$

$$V_{out\ ZERO} = 2R_{HM}\, I_c \qquad (C.5)$$

$$V_{out\ ONE} = (R_{HM} + R_{FM})\, I_c \qquad (C.6)$$

APPENDIX D

THE ALGEBRAIC SOLUTION OF THE LINEARIZED THREE CORE PER BIT MEMORY UNIT

This solution neglects the loading of Loop B upon the memory core. The characteristics of the elements encountered are shown in Fig. D.1, and the method in which they are connected is shown in Fig. D.2.

The symbols listed in the two figures are explained below:

L = Z loop = slope of v - i curve of the coupling loop;

HS = R_{HS} = slope of v - i curve of the half selected switch core;

FS = R_{FS} = slope of v - i curve of the fully selected switch core;

HM = R_{HM} = slope of v - i curve of the half selected memory core;

= slope of v - i curve of fully selected memory core containing a ZERO

FM = R_{FM} = slope of v - i curve of fully selected memory core containing a ONE;

$I_{1M} = I_{CM}$ = current through memory core at threshold of switching;

$I_{2S} = I_Z + I_{CS}$ = current through switch core at threshold of switching;

i_m = current through the memory core;

i_s = current through the switch core;

i_{in} = driving current;

V_s = voltage across switch core;

V_{out} = voltage out of memory core.

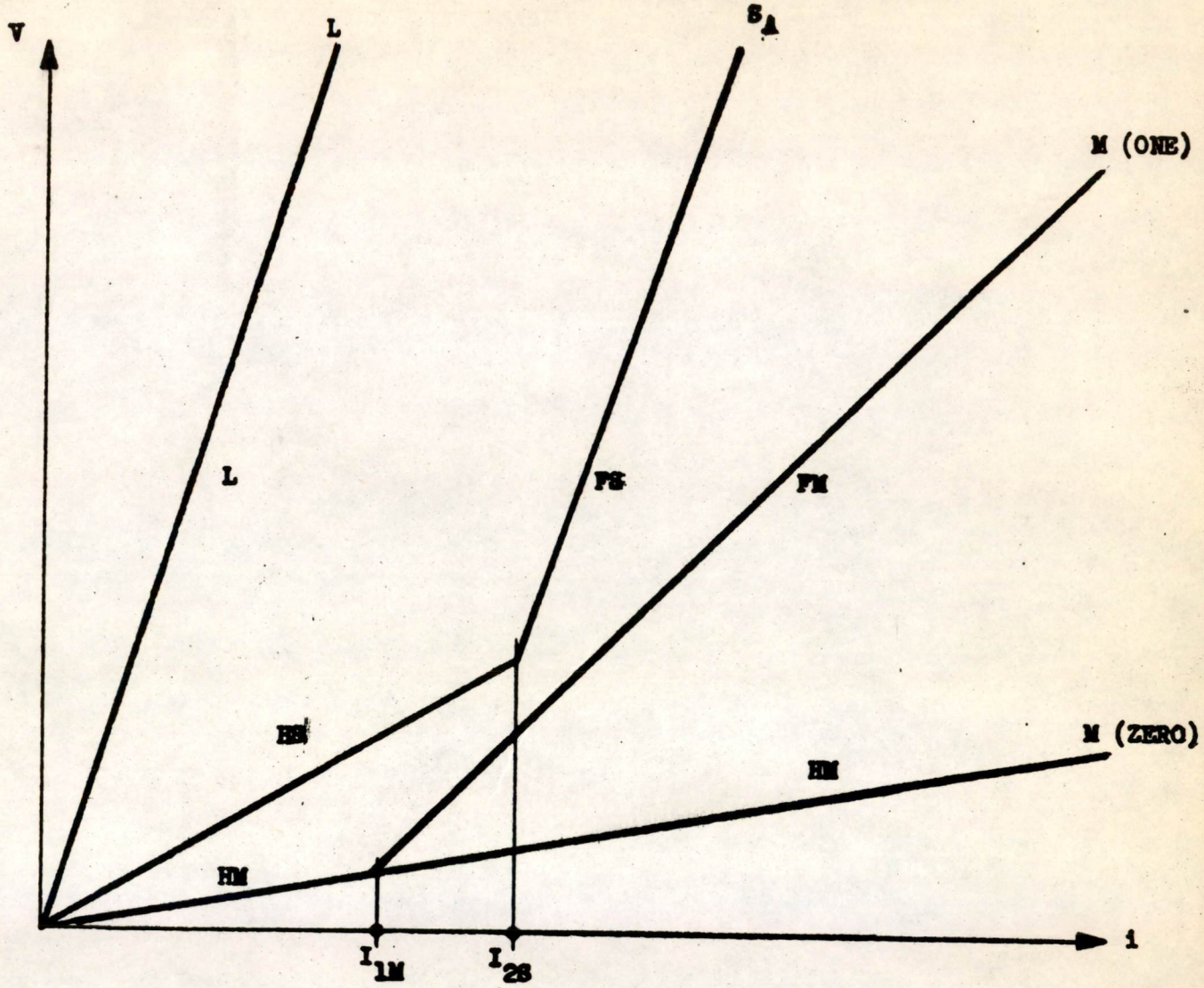

FIG. D.1

CHARACTERISTICS OF CORES AND OF LOOP A

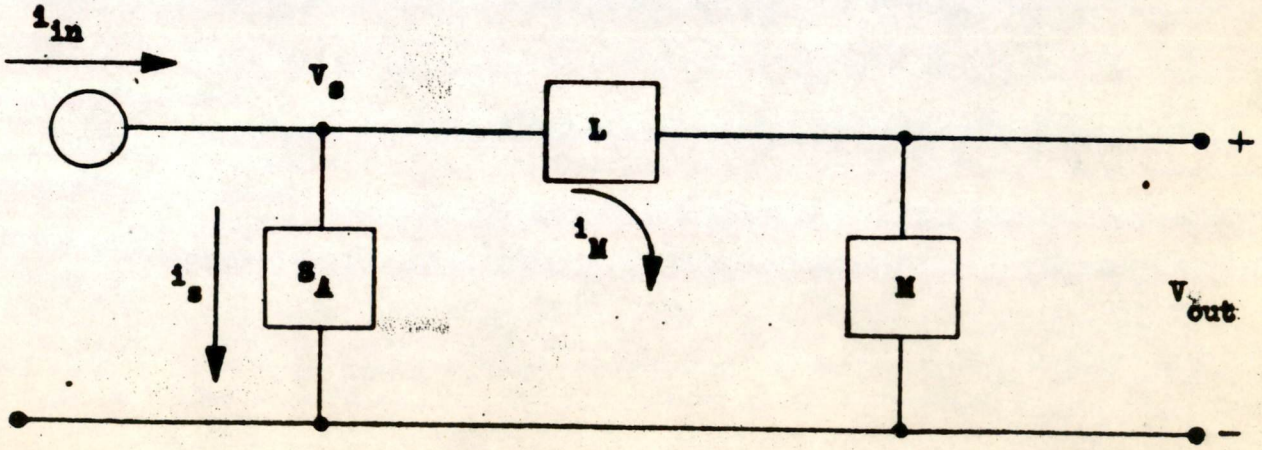

FIG. D.2

CONNECTION OF THE ELEMENTS SHOWN IN FIG. D.1

There are two distinct possible modes of operation when the memory core holds a ONE:

Mode A - the switch core switches before the memory core does;

Mode B - the memory core switches before the switch core does.

In each mode there are three states of being:

State 1 - neither core switches;

State 2 - one core switches and the other does not;

State 3 - both cores switch.

These various operating conditions may best be seen by arranging them in tabular form:

	Mode A	Mode B
State 1	$i_m < I_{1M}$; $i_s \leqq I_{2S}$	$i_m \leqq I_{1M}$; $i_s < I_{2S}$
State 2	$i_m \leqq I_{1M}$; $i_s \geqq I_{2S}$	$i_m \geqq I_{1M}$; $i_s \leqq I_{2S}$
State 3	$i_m \geqq I_{1M}$; $i_s > I_{2S}$	$i_m > I_{1M}$: $i_s \geqq I_{2S}$

If the memory core holds a ZERO, there are only two states:

State 1 - neither core switches; and

State 2 - switch core switches and memory core does not.

1. Algebraic Expressions for the ONE

The various modes and states encountered when the memory core holds a ONE shall be attacked first:

Mode A, State 1

From Figs. D.1 and D.2 it is seen that the voltage across the switch is either

$$V_s = i_m (HM + L) \qquad i_m < I_{1M} \qquad (D.1)$$

or

$$V_s = i_s\,(HS) \qquad i_s \leqq I_{2S} \qquad (D.2)$$

Equation (D.2) is critical because in Mode A the switch core switches first.

By combining (D.1) and (D.2) it is observed that,

$$i_m\,(HM+L) = i_s\,(HS),$$

or

$$i_m = i_s \quad \frac{HS}{HM+L} \qquad (D.3)$$

$$i_{in} = i_m + i_s = i_s \quad \frac{HS}{HM+L} + i_s$$

$$= i_s \quad \frac{HS+HM+L}{HM+L} \qquad i_s \leqq I_{2S} \qquad (D.4)$$

Equation (D.4) may be solved for i_s to get

$$i_s = i_{in} \quad \frac{HM+L}{HS+HM+L} \qquad (D.5)$$

Substitute (D.5) into (D.3) to obtain

$$i_m = i_{in} \quad \frac{HS}{HS+HM+L} \qquad (D.6)$$

From Fig. D.2, it is apparent that

$$V_{out} = i_m\,(HM) = i_{in} \quad \frac{(HM)(HS)}{HS+HM+L} \qquad (D.7)$$

Equation (D.4) may be rewritten as

$$i_{in} \leqq I_{2S} \quad \frac{HS+HM+L}{HM+L} \qquad (D.8)$$

Thus Mode A, State 1 is the operating region as long as Equation (D.8) is satisfied. In this region Equation (D.7) expresses the output voltage as a function of the input current.

When Equation (D.8) is no longer satisfied, the operation enters Mode A, State 2.

Mode A, State 2

The voltage across the switch core is now

$$V_s = (i_s - I_{2S})(FS) + I_{2S}\,(HS)$$

$$= i_s\,(FS) + I_{2S}\,(HS-FS) \qquad i_s \geqq I_{2S} \qquad (D.9)$$

$$V_s = i_m\,(HM+L) \qquad i_m \leqq I_{1M} \qquad (D.10)$$

Equation (D.10) is the critical equation, for State 2 ends when i_m no longer satisfies it. Combine (D.9) and (D.10) to get

$$i_s\,(FS) + I_{2S}\,(HS-FS) = i_m\,(HM+L)$$

or

$$i_s = \frac{i_m\,(HM+L) + I_{2S}\,(FS-HS)}{FS} \qquad (D.11)$$

$$i_{in} = i_m + i_s = i_m + \frac{i_m\,(HM+L) + I_{2S}\,(FS-HS)}{FS}$$

$$= \frac{i_m\,(HM+L+FS) + I_{2S}\,(FS-HS)}{FS} \qquad i_m < I_{1M} \qquad (D.12)$$

Equation (D.12) may be solved for i_m,

$$i_m = \frac{i_{in}\,(FS) + I_{2S}\,(HS-FS)}{(HM+L+FS)} \qquad (D.13)$$

From Fig. D.2 it is apparent that

$$V_{out} = i_m\,(HM) = (HM)\,\frac{i_{in}\,(FS) + I_{2S}\,(HS-FS)}{HM+L+FS} \qquad (D.14)$$

Equation (D.14) is subject to the condition that core S_a switch. This requires that

$$i_{in} \geqq I_{2S}\,\frac{HS+HM+L}{HM+L} \qquad (D.15)$$

Another requirement is that Equation (D.12) hold. It is rewritten to find that

$$i_{in} \leqq \frac{I_{1M}\,(HM+L+FS) + I_{2S}\,(FS-HS)}{FS} \qquad (D.16)$$

If Equation (D.16) is not satisfied, operation transfers from Mode A, State 2 to Mode A, State 3.

Mode A, State 3

In State 3, both cores switch. Thus,

$$V_s = (i_s - I_{2S})(FS) + I_{2S}\,(HS)$$
$$= i_s\,(FS) + I_{2S}\,(HS-FS) \qquad i_s > I_{2S} \qquad (D.17)$$

$$V_s = (i_m - I_{1M})(FM) + I_{1M}\,(HM) + i_m\,(L)$$
$$= i_m\,(FM+L) + I_{1M}\,(HM-FM) \qquad i_m \geqq I_{im} \qquad (D.18)$$

Combine (D.17) and (D.18) and then solve for i_s,

$$i_s\,(FS) + I_{2S}\,(HS-FS) = i_m\,(FM+L) + I_{1M}\,(HM-FM)$$

$$i_s = \frac{i_m\,(FM+L) + I_{1M}\,(HM-FM) + I_{2S}\,(FS-HS)}{FS} \qquad (D.19)$$

$$i_{in} = i_m + i_s = i_m + \frac{i_m\,(FM+L) + I_{1M}\,(HM-FM) + I_{2S}\,(FS-HS)}{FS}$$

$$i_{in} = \frac{i_m\,(FS+FM+L) + I_{1M}\,(HM-FS) + I_{2S}\,(HS-FS)}{FS} \quad . i_m > I_{1M} \qquad (D.20)$$

Solve Equation (D.20) for i_m. Thus,

$$i_m = \frac{i_{in}\,(FS) + I_{1M}\,(FM-HM) + I_{2S}\,(HS-FS)}{(FS+FM+L)} \qquad (D.21)$$

From Figs. D.1 and D.2 it is observed that

$$V_{out} = (i_m - I_{1M})(FM) + I_{1M}\,(HM)$$

$$= i_m\,(FM) + I_{1M}\,(HM-FM)$$

$$= (FM)\,\frac{i_{in}\,(FS) + I_{1M}(FM-HM) + I_{2S}\,(HS-FS)}{(FS+FM+L)} + I_{1M}\,(HM-FM)$$

$$= \frac{i_{in}(FS)(FM)+I_{1M}\left[(FS)(HM)+L(HM)-L(FM)-(FS)(FM)\right]+I_{2S}(FM)(HS-FS)}{(FS+FM+L)}$$

$$V_{out} = \frac{i_{in}(FS)(FM)+I_{1M}(FS+L)(HM-FM)+I_{2S}(FM)(HS-FS)}{(FS+FM+L)} \qquad (D.22)$$

This equation holds in State 3, and it is required that core M switch. Thus,

$$i_{in} \geq \frac{I_{1M}\,(HM+L+FS) + I_{2S}\,(FS-HS)}{FS} \qquad (D.23)$$

The three states of Mode A are described completely in each region by the equation listed:

Mode A, State 1 - Equation (D.7) and (D.8);

Mode A, State 2 - Equations (D.14), (D.15) and (D.16); and

Mode A, State 3 - Equations (D.22) and (D.23).

The description of the operation in Mode A has been completed and the derivation of the equations governing the behavior of the memory unit in Mode B shall be carried out.

Mode B, State 1

When neither core switches

$$V_s = i_m (HM+L) \qquad i_m \leqq I_{1M} \tag{D.24}$$

$$V_s = i_s (HS) \qquad i_s < I_{2S} \tag{D.25}$$

Equation (D.24) is critical because core M is the first one to switch.

Combine (D.24) and (D.25) and solve for i_s to get

$$i_m (HM+L) = i_s (HS)$$

$$i_s = \frac{i_m (HM+L)}{HS} \tag{D.26}$$

$$i_{in} = i_s + i_m = \frac{i_m (HM+L)}{HS} + i_m$$

$$= \frac{i_m (HM+L+HS)}{HS} \qquad i_m \leqq I_{1M} \tag{D.27}$$

Solve equation (D.27) for i_m to obtain

$$i_m = \frac{i_{in} (HS)}{HM+L+HS} \tag{D.28}$$

$$V_{out} = i_m (HM) = i_{in} \frac{(HS)(HM)}{HM+L+HS} \tag{D.29}$$

Equation (D.29) is valid so long as (D.27) holds. Rewriting (D.27) leads to the condition that

$$i_{in} \leqq \frac{I_{1M} (HM+L+HS)}{HS} \tag{D.30}$$

Mode B, State 2

The memory core is the only one to switch in State 2. The voltage across the switch core is

$$V_s = (i_m - I_{1M})(FM) + I_{1M}(HM) + i_m(L)$$
$$= i_m(FM+L) + I_{1M}(HM-FM) \qquad i_m \geq I_{1M} \qquad (D.31)$$

$$V_s = i_s(HS) \qquad i_s \leq I_{2S} \qquad (D.32)$$

Equation (D.32) is critical for State 2 is ended when the current no longer satisfies the inequality.

Combine (D.31) and (D.32) to get

$$i_m(FM+L) + I_{1M}(HM-FM) = i_s(HS)$$

$$i_m = \frac{i_s(HS) + I_{1M}(FM-HM)}{FM+L} \qquad (D.33)$$

$$i_{in} = i_m + i_s = \frac{i_s(HS) + I_{1M}(FM-HM)}{FM+L} + i_s$$
$$= \frac{i_s(HS+FM+L) + I_{1M}(FM-HM)}{FM+L} \qquad i_s \leq I_{2S} \qquad (D.34)$$

Solve equation (D.34) for i_s. The result is

$$i_s = \frac{i_{in}(FM+L) + I_{1M}(HM-FM)}{HS+FM+L} \qquad (D.35)$$

Substitute (D.35) into (D.33) to get (after some simplifications)

$$i_m = \frac{i_{in}(HS) + I_{1M}(FM-HM)}{HS+FM+L} \qquad (D.36)$$

$$V_{out} = (i_m - I_{1M})(FM) + I_{1M}(HM) = i_m(FM) + I_{1M}(HM-FM)$$
$$= (FM)\frac{i_{in}(HS) + I_{1M}(FM-HM)}{HS+FM+L} + I_{1M}(HM-FM)$$

$$V_{out} = \frac{i_{in}\,(HS)(FM) + I_{1M}\,(HM-FM)(L+HS)}{HS+FM+L} \qquad (D.37)$$

Equation (D.37) requires that the memory core switch, and that the switch core does not.

The memory core will switch if

$$i_{in} \geq \frac{I_{1M}\,(HM+L+HS)}{HS} \qquad (D.38)$$

The switch core will not switch if Equation (D.34) is satisfied. Thus

$$i_{in} \leq \frac{I_{2S}\,(HS+FM+L) + I_{1M}\,(FM-HM)}{FM+L} \qquad (D.39)$$

When the input current is so large that (D.39) is no longer satisfied, the operating region shifts to Mode B, State 3.

Mode B, State 3

Both cores switch in this state, and so the switch core voltage is

$$V_s = (i_m - I_{1M})(FM) + I_{1M}\,(HM) + i_m\,(L)$$
$$= i_m\,(FM+L) + I_{1M}\,(HM-FM) \qquad i_m > I_{im} \qquad (D.40)$$

$$V_s = (i_s - I_{2S})(FS) + I_{2S}\,(HS)$$
$$= i_s\,(FS) + I_{2S}\,(HS-FS) \qquad i_s \geq I_{2S} \qquad (D.41)$$

Set (D.40) equal to (D.41) and solve for i_s

$$i_m\,(FM+L) + I_{1M}\,(HM-FM) = i_s\,(FS) + I_{2S}\,(HS-FS)$$

$$i_s = \frac{i_m\,(FM+L) + I_{1M}\,(HM-FM) + I_{2S}\,(FS-HS)}{FS} \qquad (D.42)$$

$$i_{in} = i_s + i_m = \frac{i_m\,(FM+L) + I_{1M}\,(HM-FM) + I_{2S}\,(FS-HS)}{FS} + i_m$$

$$= \frac{i_m\,(FS+FM+L) + I_{1M}\,(HM-FM) + I_{2S}\,(FS-HS)}{FS} \qquad (D.43)$$

Solve Equation (D.43) for i_m to get

$$i_m = \frac{i_{in}\,(FS) + I_{1M}\,(FM-HM) + I_{2S}\,(HS-FS)}{FS+FM+L} \qquad (D.44)$$

$$V_{out} = (i_m - I_{1M})(FM) + I_{1M}\,(HM) = i_m\,(FM) + I_{1M}\,(HM-FM)$$

$$V_{out} = (FM)\,\frac{i_{in}\,(FS) + I_{1M}\,(FM-HM) + I_{2S}\,(HS-FS)}{FS+FM+L} + I_{1M}\,(HM-FM)$$

$$V_{out} = \frac{i_{in}\,(FS)(FM) + I_{1M}\,(HM-FM)(FS+L) + I_{2S}(HS-FS)(FM)}{FS+FM+L} \qquad (D.45)$$

The condition that core A switch is satisfied if

$$i_{in} \geq \frac{I_{2S}\,(HS+FM+L) + I_{1M}\,(FM-HM)}{FM+L} \qquad (D.46)$$

The three states of Mode B are described completely in each region by the equations:

Mode B, State 1 - Equations (D.29) and (D.30);

Mode B, State 2 - Equations (D.37), (D.38) and (D.39); and

Mode B, State 3 - Equations (D.45) and (D.46).

The first step to be made in extracting some information from these equations is to put them together in one place. Thus, the important equations are listed below.

2. Summary of Valuable Equations in Modes A and B

Mode A

State 1 - Neither core switches

$$i_m < I_{1M};\ i_s \leqq I_{2S}$$

$$V_{out} = i_{in} \frac{(HS)(HM)}{HS+HM+L} \tag{D.7}$$

$$i_{in} \leqq I_{2S} \frac{HS+HM+L}{HM+L} \tag{D.8}$$

State 2 - Switch core switches; memory core does not switch

$$i_m \leqq I_{1M};\ i_s \geqq I_{2S}$$

$$V_{out} = (HM) \frac{i_{in}\,(FS) + I_{2S}\,(HS-FS)}{FS+HM+L} \tag{D.14}$$

$$I_{2S} \frac{HS+HM+L}{HM+L} \leqq i_{in} \leqq \frac{I_{1M}\,(HM+L+FS) + I_{2S}\,(FS-HS)}{FS} \tag{D.15, D.16}$$

State 3 - Both cores switch

$$i_m \geqq I_{1M};\ i_s > I_{2S}$$

$$V_{out} = \frac{i_{in}(FM)(FS)+I_{1M}\,(HM-FM)(FS+L)+I_{2S}(FM)(HS-FS)}{FS+FM+L} \tag{D.22}$$

$$i_{in} \geqq \frac{I_{1M}\,(HM+L+FS) + I_{2S}\,(FS-HS)}{FS} \tag{D.23}$$

Mode B

State 1 - Neither core switches

$$i_m \leqq I_{1M};\ i_s < I_{2S}$$

$$V_{out} = i_{in} \frac{(HS)(HM)}{HS+HM+L} \tag{D.29}$$

$$i_{in} \leq I_{1M} \frac{HM+HS+L}{HS} \qquad (D.30)$$

State 2 - Memory core switches; switch core does not switch

$$i_m \geq I_{1M};\ i_s \leq I_{2S}$$

$$V_{out} = \frac{i_{in}(HS)(FM) + I_{1M}(HM-FM)(L+HS)}{HS+FM+L} \qquad (D.37)$$

$$I_{1M} \frac{HM+L+HS}{HS} \leq i_{in} \leq \frac{I_{1M}(FM-HM) + I_{2S}(HS+FM+L)}{FM+L} \qquad (D.38, D.39)$$

State 3 - Both cores switch

$$i_m > I_{1M};\ i_s \geq I_{2S}$$

$$V_{out} = \frac{i_{in}(FS)(FM)+I_{1M}(HM-FM)(FS+L)+I_{2S}(HS-FS)(FM)}{FS+FM+L} \qquad (D.45)$$

$$i_{in} \geq \frac{I_{1M}(FM-HM) + I_{2S}(HS+FM+L)}{FM+L} \qquad (D.46)$$

3. Adjustment of Parameters so as to Obtain the Best Operation

It has been pointed out in Chapter III (Section C2) that there are two distinct manners in which the memory cycle may be run. One method consists of ending the read cycle at the same time that the write cycle begins. Operation in this case is required to be in Mode A, and the best results are achieved if the output of a half-selected switch supplies one-half the coercive force of the memory core. The half-selected switch should be driven just to the point at which it tends to switch.

The second method requires the write cycle to wait until the effects of the read cycle have completely decayed. Operation in this case may be either in Mode A or Mode B but the best results are obtained if both the

switch core and memory core are switched by the same excitation current. The half-selected switch core is driven to the point at which it is just about to switch (and so is the memory core). It is found that Modes A and B yield the same equations when both cores switch at the same time.

a. Operation When Read Cycle Ends Concurrently With Beginning of Write Cycle

Refer to Figs. D.1 and D.2. When the input current, i_{in}, is such that $i_s = I_{2S}$, then in order to obtain the best operation possible $i_m = (1/2)I_{1M}$. The voltage across the switch core,

$$V_s = i_s\,(HS) = i_m\,(L+HM) \tag{D.47}$$

Placing the known values of current into Equation (D.47) yields

$$I_{2S}\,(HS) = (1/2)\,I_{1M}\,(L+HM)$$

or

$$I_{2S} = I_{1M}\,\frac{L+HM}{2(HS)} \tag{D.48}$$

The application of Equation (D.48) to the equations of State 1 does not alter (D.7) but (D.8) is changed.

$$i_{in} \leqq I_{1M}\,\frac{L+HM+HS}{2\,(HS)} \tag{D.49}$$

State 2 is of no interest because a fully selected memory cell should operate in State 3 for the memory core must be switched when it is selected.

Equation (D.22) can be rewritten applying (D.48) as follows:

$$V_{out} = \frac{i_{in}\,(FM)(FS)+I_{1M}(HM-FM)(FS+L)+I_{1M}\,\frac{(L+HM)(FM)(HS-FS)}{2(HS)}}{FS+FM+L}$$

$$V_{out} = \frac{2i_{in}(FS)(FM)(HS)+I_{1M}\left[(HS)(HM)(2FS+2L+FM)-(FS)(FM)(2HS+L+HM)-L(HS)(FM)\right]}{2(HS)(FS+FM+L)} \tag{D.50}$$

Equation (D.23) becomes

$$i_{in} \geq \frac{I_{1M}(HM+L+FS) + \frac{I_{1M}(L+HM)(FS-HS)}{2(HS)}}{FS}$$

$$i_{in} \geq I_{1M} \frac{(HS)(HM)+L(HS)+2(HS)(FS)+L(FS)+(HM)(FS)}{2(HS)(FS)} \qquad (D.51)$$

$$i_{in} \geq I_{1M}/2 \left[2+(L+HM)\left(\frac{1}{HS}+\frac{1}{FS}\right)\right] \qquad (D.52)$$

It is now appropriate to consolidate the results obtained subject to the restrictions imposed by Equation (D.48).

State 1 - Neither core switches (Half Select)

$$V_{out} = i_{in} \frac{(HS)(HM)}{HS+HM+L} \qquad (D.7)$$

$$i_{in} \leq I_{1M} \frac{L+HM+HS}{2(HS)} \qquad (D.49)$$

State 3 - Both cores switch (Full Select)

$$V_{out} =$$

$$\frac{2i_{in}(FS)(FM)(HS)+I_{1M}\left[(HS)(HM)(2FS+2L+FM)-(FS)(FM)(2HS+L+HM)-L(HS)(FM)\right]}{2(HS)(FS+FM+L)} \qquad (D.50)$$

$$i_{in} \geq I_{1M}/2 \left[2+(L+HM)\left(\frac{1}{HS}+\frac{1}{FS}\right)\right] \qquad (D.52)$$

In order to obtain the best ONE-to-half select ratio and the fastest operating speed, the memory must be driven as hard as possible. This requires that Equation (D.52) be satisfied by the equal sign. The full select driving current is then twice this current. The results are

$$V_{\text{out Half Select ONE}} = I_{1M} \frac{HM}{2} \qquad (D.53)$$

$$V_{\text{out Full Select ONE}} = I_{1M} \frac{(HS)(HM)(2FS+2L+FM)+(FS)(FM)\left[L\left(1-\frac{HS}{FS}\right)+HM\right]}{2HS\ (FS+FM+L)} \qquad (D.54)$$

b. Operation When Write Cycle is Delayed Until Read Cycle is Completed

It is apparent that when the cycle is operated in this manner, the best results are obtained when State 2 is eliminated. This is accomplished by causing the memory and switch cores to switch simultaneously when selected.

Refer to Figs. D.1 and D.2. When the input current, i_{in}, is such that $i_s = I_{2S}$, then in order to obtain the best possible operation it is necessary that $i_m = I_{1M}$. The voltage across the switch core is

$$V_s = i_s\ (HS) = i_m\ (L+HM) \qquad (D.55)$$

Place the known values of current into Equation (D.55) to get

$$I_{2S}\ (HS) = I_{1M}\ (L+HM)$$

or

$$I_{2S} = I_{1M} \frac{(L+HM)}{HS} \qquad (D.56)$$

The application of Equation (D.56) to the equations of Mode B (the results are identical if (D.56) is applied to Mode A), does not alter the equations of State 1. State 2 is eliminated. The equations of State 3 must be rewritten.

Equation D.45 (State 3), must be rewritten

$$V_{out} = \frac{i_{in}(FS)(FM)+I_{1M}\left[(HM-FM)(FS+L)+\frac{(FM)(HS-FS)(L+HM)}{HS}\right]}{FS+FM+L}$$

$$V_{out} = \frac{i_{in}(FS)(FM)(HS)+I_{1M}\left[(HS)(HM)(FS+L+FM)-(FS)(FM)(HS+L+HM)\right]}{(HS)(FS+FM+L)} \qquad (D.57)$$

Equation D.46 becomes

$$i_{in} \geq \frac{I_{1M}\,(FM-HM) + I_{1M}\,\frac{(HS+FM+L)(L+HM)}{HS}}{FM+L}$$

$$i_{in} \geq I_{1M}\,\frac{HS+L+HM}{HS} \qquad (D.58)$$

It is now appropriate to consolidate the results obtained subject to the restriction imposed by Equation (D.47).

State 1 - Neither core switches (Half Select)

$$V_{out} = i_{in}\,\frac{(HS)(HM)}{HS+HM+L} \qquad (D.29)$$

$$i_{in} \leq I_{1M}\,\frac{HM+HS+L}{HS} \qquad (D.30)$$

State 3 - Both cores switch (Full Select)

$$V_{out} = \frac{i_{in}(FS)(FM)(HS) + I_{1M}\left[(HS)(HM)(FS+L+FM)-(FS)(FM)(HS+L+HM)\right]}{(HS)(FS+FM+L)} \qquad (D.57)$$

$$i_{in} \geq I_{1M}\,\frac{HM+HS+L}{HS} \qquad (D.58)$$

In order to obtain the best ONE-to-half select ratio and the fastest operating speed, the memory must be driven as hard as possible. This requires that Equation (D.50) be satisfied by the equal sign. The full select driving durrent is twice this current. The results are

$$V_{out\ Half\ Select\ ONE} = I_{1M}\ (HM) \tag{D.59}$$

$$V_{out\ Full\ Select\ ONE} = I_{1M}\ \frac{(HS)(HM)(FS+L+FM)+(FS)(FM)(HS+L+HM)}{(HS)(FS+L+FM)} \tag{D.60}$$

or

$$V_{out\ Full\ Select\ ONE} = \frac{I_{1M}}{HS}\left[(HS)(HM)+(FS)(FM)\ \frac{HS+L+HM}{FS+L+FM}\right] \tag{D.61}$$

4. Algebraic Expression for the ZERO

The two methods of driving the memory just described differ in the way the memory core is treated. Both methods drive the half-selected switch core so that it almost switches. In the reading of a ZERO, these two methods will be symbolically the same because the memory core does not switch.

The calculation of the size of the ZERO follows. A half-selected ZERO, is, by definition, the same size as a half-selected ONE. All of the driving currents and optimizing criteria have been arrived at from considerations of the ONE. The ZERO cannot be reworked. Whatever it is, it must stay.

For the fully selected ZERO,

$$V_s = i_m\ (L+HM) \tag{D.62}$$

$$\begin{aligned} V_s &= (i_s - I_{2S})(FS) + I_{2S}\ (HS) \\ &= i_s\ (FS) + I_{2S}\ (HS-FS) \qquad i_s > I_{2S} \end{aligned} \tag{D.63}$$

Set (D.62) equal to (D.63) and solve for i_s

$$i_m\ (L+HM) = i_s\ (FS) + I_{2S}\ (HS-FS)$$

$$i_s = \frac{i_m\,(L+HM) + I_{2S}\,(FS-HS)}{FS} \tag{D.64}$$

$$i_{in} = i_s + i_m = \frac{i_m\,(L+HM) + I_{2S}\,(FS-HS)}{FS} + i_m$$

$$= \frac{i_m\,(L+HM+FS) + I_{2S}\,(FS-HS)}{FS} \tag{D.65}$$

Solve (D.65) for i_m

$$i_m = \frac{i_{in}\,(FS) + I_{2S}\,(HS-FS)}{L+HM+FS} \tag{D.66}$$

It is desirable to express Equation (D.66) in terms of I_{1M} rather than I_{2S}. This conversion depends on how the memory is driven. In one case Equation (D.48) converts from I_{2S} to I_{1M}; in the other case, Equation (D.56) performs the conversion. Equation (D.56) shall be used here; it should be understood that if the other type operation is desired, I_{1M} must be replaced by $I_{1M}/2$.

$$i_m = \frac{i_{in}\,(FS) + I_{1M}\,\frac{(HS-FS)(L+HM)}{HS}}{L+HM+FS}$$

$$= \frac{i_{in}\,(FS)(HS) + I_{1M}\,(HS-FS)(L+HM)}{HS\,(L+HM+FS)} \tag{D.67}$$

$$V_{out} = i_m\,(HM)$$

$$= (HM)\,\frac{i_{in}\,(FS)(HS) + I_{1M}\,(HS-FS)(L+HM)}{HS\,(L+HM+FS)} \tag{D.68}$$

The input current, for the full select is

$$i_{in} = 2I_{1M}\,\frac{HM+HS+L}{HS} \tag{D.69}$$

Place this current into Equation (D.68) and the fully selected ZERO output is found.

$$V_{out\ Full\ Select\ ZERO} = \frac{I_{1M}\ (HM)}{(L+HM+FS)(HS)} \left[HS(FS+L+HM)+FS(HS+L+HM)\right] \qquad (D.70)$$

$$= I_{1M}\ \frac{HM}{HS} \left[HS+FS\ \frac{HS+L+HM}{FS+L+HM}\right] \qquad (D.71)$$

Equations (D.70) and (D.71) represent the fully selected ZERO outputs if the memory cycle has a delay between the read and write pulses. If there is no delay, (i.e. - write begins as read ends), then I_{1M} must be replaced by $I_{1M}/2$ in the two equations.

5. Ratios of ONE to ZERO and ONE to Half Select

The results obtained in sections 3 and 4 of this appendix may now be combined so that the ratios of desirable to undesirable signals may be determined.

a. Operation When Read Cycle Ends Concurrently With Beginning of Write Cycle

The equations governing the behavior of the memory read out are: (D.53), (D.54) and (D.70). However, (D.70) is valid only if I_{1M} is replaced by $I_{1M/2}$, as is pointed out in Appendix D. The equations are:

$$V_{out\ Half\text{-}Select} = (I_{1M/2})\ (HM) \qquad (D.53)$$

$$V_{out\ Full\text{-}Select\ ONE} =$$

$$\frac{I_{1M}}{2} \quad \frac{(HS)(HM)(2FS+2L+FM)+(FS)(FM)\left[L\left(1-\frac{HS}{FS}\right)+HM\right]}{HS\ (FS+FM+L)} \qquad (D.54)$$

V_{out} Full-Select ZERO =

$$\frac{I_{1M}\,(HM)}{2(HS)(L+HM+FS)}\left[\,HS(FS+L+HM)+FS(HS+L+HM)\right] \qquad (D.70)$$

It is now desired to find the ONE to ZERO, and ONE to half-select ratios, from the equations just written. In Chapter 2, the factor μ was introduced. It was defined as

$$\mu = FM/HM$$

The factor σ is now introduced by the definition

$$\sigma = FS/HS$$

If the memory and switch cores are made of the same material, a reasonable assumption would be that $\mu = \sigma$. This shall not be done, however.

A final definition is arrived at from equation (D.48) - the equation that fixes the relationship between the coercive forces of the memory and switch cores. Equation (D.48) states that

$$I_{2S} = I_{1M}\,\frac{L+HM}{2(HS)}$$

The factor K is introduced by the definition

$$\frac{K}{2} = \frac{I_{2S}}{I_{1M}} = \frac{L+HM}{2(HS)} \qquad (D.74)$$

It should be observed that the constants μ, σ and K are all larger than unity. It has been found that μ and σ are each almost 10. The size of K depends upon the cores and the loop, but it may be somewhat larger than 10.

That ratio of ONE to half select is

$$\frac{V_{out}\ ONE}{V_{out}\ Half\text{-}select} = \frac{(HS)(HM)(2FS+2L+FM)+(FS)(FM)\left[L\left(1-\frac{HS}{FS}\right)+HM\right]}{(HS)(HM)(FS+FM+L)}$$

$$\frac{V_{out}\ ONE}{V_{out}\ Half\text{-}select} = \frac{2FS+FM+2L}{FS+FM+L} + \frac{(FS)(FM)\left[\overline{L}(1-HS)+HM\right]}{(HS)(HM)(FS+FM+L)}$$

$$= \frac{2FS+FM+2L}{FS+FM+L} + \frac{L(1-\frac{1}{\sigma})+HM}{FS+FM+L} \qquad (D.75)^*$$

A reasonable approximation is that $(FS+L) \gg FM$, and that $\sigma \gg 1$. These assumptions lead to

$$\frac{V_{out}\ ONE}{V_{out}\ Half\text{-}select} \cong 2 + \sigma\mu\,\frac{L+HM}{FS+FM+L} \qquad (D.76)$$

If equation (D.74) is substituted into (D.76) - first in the numerator of the second term and then in the denominator (eliminating L) the results obtained are

$$\frac{V_{out}\ ONE}{V_{out}\ Half\text{-}select} \cong 2 + \sigma\mu\,\frac{K(HS)}{FS+FM+L}$$

$$= 2 + \sigma\mu\,\frac{K(HS)}{HS(\sigma+K)+HM(\mu-1)} \qquad (D.77)$$

Because the switch is usually considerably larger than the memory core, $HS > HM$, and further more $(\sigma+K) > (\mu-1)$. Utilizing these results leads to equation (D.78), as derived from (D.77).

$$\frac{V_{out}\ ONE}{V_{out}\ Half\text{-}select} \cong 2 + \mu\sigma\,\frac{K}{\sigma+K} \qquad (D.78)$$

*If, in equation (D.75), the switch core does not manage to switch, it behaves as if it were a linear inductor. This means (since operation is Mode A) that the memory core does not switch. If σ is set equal to 1, (D.75) becomes

$$\frac{V_{out}\ ONE}{V_{out}\ Half\text{-}select} = \frac{2FS+FM+2L}{FS+FM+L} + \frac{\mu(HM)}{FS+FM+L} = \frac{2FS+2FM+2L}{FS+FM+L} = 2$$

This, of course, is what should be expected if neither core switches.

As σ is made very large, the signal-to-noise ratio approaches $2+\mu K$. This may be a considerable improvement over the coincident current signal to noise ratio (which was found to be $1+\mu$).

If the factor K is made very large, the signal-to-noise ratio approaches $2+\mu\sigma$. This is essentially σ times better than the ratio obtained in the coincident current memory.

The ONE to ZERO ratio may be determined in the same manner.

$$\frac{V_{out}\ ONE}{V_{out}\ ZERO} =$$

$$\frac{\left\{(HS)(HM)(2FS+FM+2L)+(FS)(FM)\left[L\left(1-\frac{HS}{FS}\right)+HM\right]\right\}\left[HS(L+HM+FS)\right]}{(HS)(FS+FM+L)(HM)\left[HS(FS+L+HM)+FS(HS+L+HM)\right]}$$

$$= \frac{(2FS+FM+2L)+\sigma\mu\left[L\left(1-\frac{1}{\sigma}\right)+HM\right]}{(FS+FM+L)\left[1+\frac{\sigma(HS+L+HM)}{FS+L+HM}\right]} \qquad (D.79)$$

Equation (D.74) may be applied at this point for the purpose of simplifying (D.79)

$$\frac{V_{out}\ ONE}{V_{out}\ ZERO} = \frac{(2FS+FM+2L)+\sigma\mu\left[K(HS)-\frac{K(HS)-HM}{\sigma}\right]}{(FS+FM+L)\left[1+\sigma\frac{K+1}{K+\sigma}\right]} \qquad (D.80)*$$

Equation (D.80) may be greatly simplified by making a few approximations. Itmay be safely assumed that $FS+L >> FM$, that $HS > HM$, and that K and σ are each much greater than unity. The result obtained is that

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*In equation (D.80), set $\sigma=1$. This means that the switch core never really switches. The result is that

$$\frac{V_{out}\ ONE}{V_{out}\ ZERO} = \frac{(2FS+FM+2L)+\mu(HM)}{(FS+FM+L)(2)} = \frac{2FS+2FM+2L}{2(FS+FM+L)} = 1$$

This shows that the memory core never switches either, and that means that ONEs and ZEROs are the same.

$$\frac{V_{out\ ONE}}{V_{out\ ZERO}} \cong \frac{2}{1+\sigma\frac{K+1}{K+\sigma}} + \frac{K\sigma\mu\,(HS)}{(FS+FM+L)\,(1+\sigma\frac{K+1}{K+\sigma})}$$

Apply equation (D.74) to the second term in the above equation.

$$\frac{V_{out\ ONE}}{V_{out\ ZERO}} =$$

$$\frac{2}{1+\sigma\frac{K+1}{K+\sigma}} + \frac{K\sigma\mu\,(HS)}{\left[(HS)(\sigma+K)+(HM)(\mu-1)\right]\left[1+\sigma\frac{K+1}{K+\sigma}\right]}$$

Due to the fact that HS $\gg$ HM, $\sigma > 1$, and $K > 1$, the result is

$$\frac{V_{out\ ONE}}{V_{out\ ZERO}} \cong \frac{2}{1+\sigma\frac{K+1}{K+\sigma}} + \frac{K\sigma\mu}{(\sigma+K)(1+\sigma\frac{K+1}{K+\sigma})}$$

$$\frac{V_{out\ ONE}}{V_{out\ ZERO}} = \frac{2(\sigma+K)+K\mu\sigma}{K+\sigma+\sigma K+1}$$

$$= \frac{2(K+\sigma)+K\mu\sigma}{(K+1)(\sigma+1)} \qquad (D.81)$$

If either σ or K is much larger than unity, the ONE to ZERO ratio approaches μ. It was found that in the coincident current memory the ratio was essentially $\mu/2$. The ONE to ZERO has been improved by about a factor of 2.

b. Operation When Write Cycle is Delayed Until Read Cycle is Completed

The equations governing the behavior of the memory read out are (D.59), (D.61) and (D.71). The equations are:

$$V_{out\ Half\text{-}select} = I_{1M}\,(HM) \qquad (D.59)$$

$$V_{out\ full\text{-}select\ ONE} = \frac{I_{1M}}{HS}\left[(HS)(HM)+(FS)(FM)\,\frac{HS+L+HM}{FS+L+FM}\right] \qquad (D.61)$$

$$V_{out\ full\text{-}select\ ZERO} = I_{1M}\,\frac{HM}{HS}\left[HS+(FS)\,\frac{HS+L+HM}{FS+L+HM}\right] \qquad (D.71)$$

In the previous section the constants μ and σ were defined by equations (D.72) and (D.73) respectively. These results are repeated

$$\mu = \frac{FM}{HM} \tag{D.72}$$

$$\sigma = \frac{FS}{HS} \tag{D.73}$$

The factor K may be derived from equation (D.56) which is repeated below. It will be noted that K is the same figure that is expressed by equation (D.74). Equation (D.56) states that

$$I_{2S}\,(HS) = I_{1M}\,(L+HM)$$

The factor K is defined as

$$K = \frac{I_{2S}}{I_{1M}} = \frac{L+HM}{HS} \tag{D.82}$$

It should be recalled that the constants μ, σ, and K are all larger than unity. It has been found that μ and σ are each almost 10. D may be somewhat greater than 10.

The ratio of ONE to half-select is:

$$\frac{V_{out\ ONE}}{V_{out\ half\text{-}select}} = \frac{1}{(HS)(HM)}\left[(HS)(HM)+(FS)(FM)\,\frac{HS+L+HM}{FS+L+FM}\right]$$

$$= 1 + \frac{(FS)(FM)}{(HS)(HM)}\,\frac{(HS+L+HM)}{(FS+L+FM)}$$

$$= 1 + \sigma\mu\,\frac{(1+K)(L+HM)}{L(K+\sigma)+(HM)(\mu K+\sigma)} \tag{D.83}*$$

*If, in equation (D.83), K is set equal to zero, the switch core then becomes a linear inductance (it does not switch). The switch is just an extra load on the driver in this case. The ONE to half-select ratio becomes

$$\frac{V_{out\ ONE}}{V_{out\ half\text{-}select}} = 1 + \mu\,\frac{L+HM}{\sigma(L)+\sigma(HM)} = 1+\mu$$

A reasonable assumption seems to be one that has been used in the derivation os these equations in the first place. That is, that $L \gg FM = \mu(HM)$. The equations were arrived at by neglecting the loading of the loop on the memory core. Equations (D.83) then becomes

$$\frac{V_{out\ ONE}}{V_{out\ half\text{-}select}} \tilde{=} 1 + \sigma\mu \frac{1+K}{\sigma+K} \qquad (D.84)$$

$$= 1 + \mu \frac{1+K}{1+K} \qquad (D.85)$$

If $\sigma = 1$, the switch core never really switches, and so the memory unit should behave as if it were a coincident current memory. The signal-to-noise ratio is $1+\mu$, and this, indeed, is the coincident current ratio. However, as σ becomes very large, the signal-to-noise ratio approaches $1+\mu(1+K)$. This may be a considerable improvement over the coincident current signal-to-noise ratio.

If the factor K is made very large, the signal-to-noise ratio approaches $1+\mu\sigma$. This is essentially σ times better than the coincident current memory signal-to-noise ratio. Because the value of σ is about 10, this is a considerable improvement.

The ONE to ZERO ratio may be determined in the same manner.

$$\frac{V_{out\ ONE}}{V_{out\ ZERO}} = \frac{1 + \frac{(FM)(FS)}{(\overline{HM})(\overline{HS})} \frac{HS+L+HM}{FS+L+FM}}{1 + \frac{(FS)}{(\overline{HS})} \frac{HS+L+HM}{FS+L+HM}} \qquad (D.86)$$

This, of course, was the result obtained in the coincident current memory (equation 2.17). When the switch was transformed to a linear inductance, this system degenerated to the coincident current memory scheme.

$$\frac{V_{out\ ONE}}{V_{out\ ZERO}} = \frac{1 + \mu\sigma\ \frac{(L+HM)(1+K)}{L(\sigma+K)+(HM)(\mu K+\sigma)}}{1 + \sigma\ \frac{1+K}{\sigma+K}} \qquad (D.87)*$$

If the assumption is made that $L >> FM = \mu\ (HM)$, equation (D.87) becomes

$$\frac{V_{out\ ONE}}{V_{out\ ZERO}} \approx \frac{1 + \mu\sigma\frac{(1+K)}{(\sigma+K)}}{1 + \sigma\ \frac{(1+K)}{(\sigma+K)}} \qquad (D.88)$$

$$= \frac{1 + \mu\ \frac{1+K}{1+K/\sigma}}{1 + \frac{1+K}{1+K/\sigma}} = \frac{1+\mu A}{1+A} \qquad (D.89)$$

If $\sigma = 1$, the switch core never really switches, and so the memory unit should behave as if it were a coincident current memory. The signal-to-noise ratio is $\frac{1+\mu}{2}$ (became A=1), and this is the ratio in the coincident current memory. However, as σ becomes very large, the signal-to-noise ratio approaches $\frac{1+\mu(K+1)}{2+K}$, on approximately (because K is large) μ. This is an improvement, by about a factor of two, over the coincident current memory.

If the factor K is made very large, the ONE to ZERO ratio becomes $\frac{1+\mu\sigma}{1+\sigma}$ or again, approximately μ.

In summary of the algebraic results it may be stated, that operation by either method gives very approximately the same signal-to-

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*If, in equation (D.87), K is set equal to zero, the switch core then becomes a linear inductance (it does not switch). The switch is merely an extra load on thedriver in this case. The ONE to ZERO ratio becomes

$$\frac{V_{out\ ONE}}{V_{out\ ZERO}} = \frac{1 + \mu\sigma\ \frac{L+HM}{\sigma(L)+\sigma(HM)}}{1 + \frac{\sigma}{\sigma}} = \frac{1+\mu}{2}$$

noise ratios, and the same ONE to ZERO ratios. In each case there is an improvement noted when the results are compared to ratios obtained by coincident current methods.

The ratio of fully selected ONE to half select is improved by a factor of about 10, when the three core per bit memory is employed (assuming that both memory units use the same memory cores). The ONE to ZERO ratio is improved by about a factor of 2.

Over and above these improvements in the ratios of desirable to undesirable signals, is the improvement in speed. It is found that about 6 microseconds are required to complete the read and write excitations of a core in the coincident current memory. As is shown in Chapter 3, a complete cycle in the three-core-per-bit memory may be successfully finished in 0.5 microseconds.

It has been discovered that the ratios are virtually unaffected by the timing of the read and write excitations, at least on paper.

The ratios of the ONE obtained by equation (D.54) to the ONE obtained by equation (D.61) may be approximated. Call the first ONE "a"; this corresponds to the turning of the write cycle on and the read cycle off simultaneously. Call the second ONE "b"; this corresponds to delaying the write cycle.

$$\frac{a}{b} = \frac{(HS)(HM)(2FS+2L+FM) + (FS)(FM)\left[L\left(1-\frac{HS}{FS}\right) + HM\right]}{2\,(FS+FM+L)\left[(HS)(HM)+(FS)(FM)\,\frac{HS+L+HM}{FS+L+FM}\right]}$$

This, of course, was the result obtained in the coincident current memory (equation 2.16). When the switch core was transformed to a linear inductance, this system degenerated to the coincident current memory scheme.

Use the usual abbreviations in order to simplify this expression

$$\frac{a}{b} = \frac{(2FS+2L+FM) + \mu\left[L(1-\frac{1}{\sigma}) + HM\right]}{2(FS+FM+L)\left[1+\sigma\mu\,\frac{HS+L+HM}{FS+L+FM}\right]} \qquad (D.90)$$

Simplify equation (D.90) by the use of equation (D.82) and the fact that $K > 1$, $\mu > 1$, and $\sigma > 1$.

$$\frac{a}{b} \simeq \frac{(2FS+2L+FM) + \sigma\mu K(HS)}{2(FS+FM+L)\left[1+\sigma\mu\,\frac{1+K}{\sigma+K}\right]}$$

$$= \frac{2(HS)(\sigma+K)+(HM)(\mu-2)+\sigma\mu K(HS)}{2\left[(HS)(\sigma+K)+HM(\mu-1)\right]\left[1+\sigma\mu\,\frac{1+K}{\sigma+K}\right]} \qquad (D.91)$$

It is known that $HS > HM$, and that $\sigma+K > \mu$, so the terms including HM, in equation (D.91) may be dropped. The result is

$$\frac{a}{b} \simeq \frac{2(\sigma+K)+\sigma\mu K}{2(\sigma+K)\left(1+\sigma\mu\,\frac{1+K}{\sigma+K}\right)} \qquad (D.92)$$

An approximation which allows a rapid computation of the expected ratio of ONE "a" to ONE "b" is to assume that $\sigma = \mu = K > 1$. Call all of the constants K. The result is

$$\frac{a}{b} = \frac{4K + K^3}{4K\left(1+K^2\,\frac{K+1}{2K}\right)}$$

$$\frac{a}{b} \simeq \frac{K^3}{4K\left(\frac{K^2}{2}\right)} = 1/2 \qquad (D.93)$$

It should be expected then, that the ones obtained when a delay is permitted are twice the ONEs achieved when the read and write cycles overlap. The cores switch twice as rapidly in state b as they do in state a. However, the delay necessary in state b, removes any anticipated gain in speed. It is probably true that each method of operation will result in about the same cycle time. The 1 to 2 ratio of outputs should be expected because the memory core is hit twice as hard when the delay is allowed.

APPENDIX E

Derivation of the Graphical Solution of the Three Core Memory (Including Loading of Loop B)

The graphical solution of the problem concerning the expected outputs of the memory core for ONEs, ZEROs, and half-selects may be presented here. The loading of loop B is taken into account in this discussion.

The equivalent circuit of the unit is shown in Figure 3.10. The characteristics of the cores are shown in Figures 2.23 and 2.24. The volt-ampere characteristic of the loop is linear. The constructions described here are carried out in Figures 3.11 (when the memory core holds ONE), and in Figure 3.12 (when it holds a ZERO). The symbols used are defined here:

S_A = volt-ampere characteristic of switch core A;

S_B = volt-ampere characteristic of switch core B;

L = volt-ampere characteristic of loop;

M = volt-ampere characteristic of memory core.

S_B and L are in series, and their combined characteristic is obtained by adding the voltages across these elements when the current is fixed. The resulting curve is S_B+L. S_B+L is in parallel with M, and so the combined characteristic of these elements is obtained by adding the currents each draws for a given voltage. The result is $(S_B+L) \| M$, and this is in series with L. Thus to obtain their total characteristic, add voltages for given current values. Now the result is $L+(S_B+L) \| M$. The complete input characteristic is obtained by paralleling S_A with $L+(S_B+L) \| M$. The results are labelled Input.

By utilizing these curves, one may readily determine the current through any element, or the voltage at any node, when the driving current

and the information held by the memory are known. Use of this is made in determining the output voltage of the memory core as a function of the current driving the switch core. The operation is performed in the following manner. The input characteristic of the circuit has been determined, and so if a given current is pushed into switch core A, the voltage across the switch core is known. This is also the voltage across $L+(S_B+L) \| M$. From the volt-ampere curve of $L+(S_B+L) \| M$, the current through it may be found. But, this is also the current through $(S_B+L) \| M$. Because the volt-amper characteristic of $(S_B+L) \| M$ has been drawn, the voltage across it can be found when its current is known, and this is the required output voltage. The output characteristic has been determined following this method.

The case in which the loading of loop B is neglected is similar to the above, but it is simpler, because there are fewer elements cascaded. The results are shown in Figures 3.13 and 3.14.

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