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IMPROVING DIFFERENTIAL AMPLIFIER PERFORMANCE BY LOW CURRENT TRANSISTOR OPERATION

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INTRODUCTION

The advantages in noise reduction and power dissipation obtained by operating a differential amplifier at low collector currents have been recognized and described by several authors.[1, 2] The lack of commercially available transistors with high current gain in the microampere region in addition to the other required characteristics for low drift performance, i.e., low leakage and base-emitter voltage matching and temperature tracking has, however, in the past limited the input stage collector current to about 100 microamperes. Now with the recently announced low level NPN and PNP planar transistors, a further reduction in operating currents and the associated power dissipation is possible.

Such a differential amplifier with a total power dissipation of less than one milliwatt, a voltage gain of 60 db, and an equivalent input drift of less than $3uV/^{o}C$ over the operating temperature range of $-30^{o}C$ to $+75^{o}C$ was built. It's performance and the advantages of low level operation are discussed below.

AMPLIFIER DRIFT

The most serious criterion of a differential amplifier is its drift performance. Drift voltage in the amplifier input is indistinguishable from the signal and hence, the minimum detectable signal is determined by the drift.

Amplifier drift is attributed to the difference in the base-emitter voltages of the two transistors, their d.c. current gain, and their collector-base leakage currents. The terms containing these parameter differences appear in the amplifier output as an error signal. Okada has shown this output voltage of a single differential amplifier stage (Fig. 1) as[1]

$$E_{2o} - E_{1o} = \frac{\left[\alpha_1 R_{L1} + \alpha_2 R_{L2}\right]\left[\left(E_{1i} - E_{2i}\right) + \left(V_{BE2} - V_{BE1}\right)\right]}{\Delta} + \frac{\left[\alpha_1 R_{L1} + \alpha_2 R_{L2}\right]\left[\left(R_{b2} I_{CO1} - R_{b2} I_{CO2}\right) + \frac{V_e}{R_e}\left(\frac{R_{b1}}{\beta_1} - \frac{R_{b2}}{\beta_2} + R_{e1} - R_{e2}\right)\right]}{\Delta} + \left[I_{CO1} R_{L1} - I_{CO2} R_{L2}\right]$$

where $$\Delta = R_{e1} + R_{e2} + \frac{R_{b1}}{\beta_1} + \frac{R_{b2}}{\beta_2} + \frac{R_{b1} R_{b2}}{\beta_1 \beta_2 R_e}$$

with the extrinsic resistances included in R_b and R_e, the current gain assumed to be a constant and $R_L \ll r_c$. The desired zero output voltage for a zero input can always be obtained at any one operating temperature by making R_{e1} and R_{e2} adjustable at a sacrifice of equal emitter currents. In order to obtain a reasonably wide operating temperature range and a high long-term stability, the parameters of the two transistors must have similar temperature and aging effects.

The difference in the base-emitter voltages of the two input transistors is the predominant factor in the overall amplifier drift performance. In the amplifier of Fig. 2 this difference has been minimized both in the production of the dual unit 21K5 and in the circuit by keeping the collector current and the collector-emitter voltage low.

EFFECT OF LOW LEVEL OPERATION ON AMPLIFIER DRIFT:

Since the base-emitter voltage is extremely temperature sensitive with a thermal coefficient of about -2.3mV/°C, a temperature difference between the transistors of even a fraction of a degree would produce intolerable input drift. In the 21K5 unit, both transistors are mounted in close proximity on the same TO-5 header. Thus the temperature differential between the transistors is minimized. This mounting technique is common to all dual units intended for high or low level differential input stages, and in itself does not make the advantages of low level operation obvious until the power dissipation is considered. A transistor with a h_{FE} of 50 at I_C = 5uA and V_{CE} = 1.5v dissipates approximately 7.5 uW, raising the junction temperature (thermal resistance 300°C/ W) 0.0023°C compared with the common operating conditions of high level input stage operating conditions of I_C = 100uA and V_{CE} = 5v for a power dissipation of 502 uW and a junction temperature rise of 0.151°C. Since only a 1/1000°C temperature difference between the two junctions would produce an equivalent input drift of 2.3uV, the probability of error signals being generated by unequal junction temperatures is reduced by low level operation. This problem is more severe in high level input stages when the collector current is deliberately mismatched to obtain zero output.

Low level operation reduces the absolute value of the base-emitter voltage difference (V_{BE_1}-V_{BE_2}) in another way.

During the manufacturing process of all dual units, no accurate measurements of the base-emitter voltage is possible until the transistors have been mounted. The normal procedure is to select and match transistors for other characteristics and to rely on the process uniformity to produce units with low base-emitter voltage differences. A common specification is a maximum difference of 5mV at I_C = 100uA and V_{CE} = 5v for a high level dual unit. The fact that the base-emitter voltage is a function of the collector current reduces the absolute magnitude of the individual transistor V_{BE}'s and thus increases the probability of lower voltage differences. A typical value of individual V_{BE} in the 21K5 is 0.47V at I_C = 5uA as compared with .58v at 100uA for a high current unit. The temperature tracking of the difference voltage is also improved at low levels giving a typical change of 1uV/°C. Several unselected 21K5 units are plotted in Fig. 3.

Drift is also produced by the difference in d.c. current gains of the input transistors and its variation with temperature. The transistors in the 21K5 dual unit have a typical h_{FE} of 80 at I_C = 5uA, V_{CE} = 1.5v and their maximum mismatch is 10%. The variation in beta at this operating point is about 1.5%/°C; it is fairly linear with temperature as shown in Fig. 4. Since the collector current is kept constant at 5uA by the current generator, the change in h_{FE} results in a decrease of base current of about .5nA for each degree rise in temperature. This low base current change is another advantage of low level operation allowing higher source resistances to be used with less drift. A source resistance of 10k would produce, for example, $\pm$ 0.5uV/°C $[10^4 \times 0.5 \times 10^{-9} \times (\pm 10\%)]$ drift as a result of h_{FE} mismatch of 10%. For the same reason, a greater unbalance in the source resistances is permissible.

The third cause of drift is the collector-base leakage current I_{CBO}. This current is typically 0.1nA at room temperature, and it doubles with every 11°C rise in temperature. Thus the drift caused by the leakage currents can be neglected for operating temperatures up to 75°C if the source resistance is less than 1000 ohms.

AMPLIFIER DESCRIPTION

The differential amplifier of Fig. 2 was constructed using low level planar transistors in all stages. The input stage, using a 21K5 dual unit (2 matched 2N2524's) is biased at a collector current of 5uA and a collector-emitter voltage of 1.4v. Constant emitter current to this stage is supplied by a 2N2524 transistor in the common base configuration. The 500 ohm potentiometer in the emitter circuit of the first stage allows compensation for base-emitter voltage differences of up to 1.5 mV, which is more than the worst case voltage spread shown in Fig. 2. The choice of the 5uA collector current level allows high resistances to be used in the collector so that even at a supply voltage of 3 volts high enough voltage gain is realized to confine practically all the drift to this stage.

The second stage consists of two 2N2605 PNP transistors. This complementary stage arrangement allows the output level to be returned to ground potential in the emitter follower output stage. Thus the usual intermediate voltage divider networks which would be required if transistors of the same type were used throughout the circuit are eliminated. At the collector current of 10uA, high voltage gain is also obtained in this stage for an overall amplifier open loop gain of about 1400. Feedback resistors from the collectors of the second stage to emitters of the input stage provide means for gain control. An arrangement as shown in Fig. 5 provides gain control from 600 to 1100. Other resistor combinations could be substituted for lower amplifier gain, although for circuit gain of less than 200 additional resistor changes in the current generator may be necessary to enable the output adjustment to be set for zero output at elevated temperatures.

The output stage is an emitter follower. The output level potentiometer, shunted by a silicon diode for improved temperature tracking, provides about 400 millivolt adjustment range. This amplifier was built on a printed circuit

board using conventional construction techniques. Special attention was, however, given to the input stage by keeping the length of the conductors and the connections symmetrical because unequal thermally generated voltages in the base circuit can produce drifts at least as severe as those of the transistor.

AMPLIFIER PERFORMANCE

The performance of the amplifier just described was checked with four sets of unselected transistors. Very good drift performance was achieved in all cases. The equivalent input drift with balanced source resistances of 10 k was less than 2.5 uV/°C from -30°C to +75°C as shown in Fig. 6. The limiting factor at the high end is the difference in voltage drops across the input resistors produced by the collector-base leakage currents at the elevated temperature. The temperature range could be extended by reducing the source resistances. The low temperature range is limited by the h_{FE} falloff at low temperatures and the associated deviations from the current gain match.

The long term equivalent input drift of the amplifier with the same source resistances is less than 20uV over a 72 hour period.

The total power dissipation of the circuit is approximately 500uW with a current drain of 105uA from the negative three volt supply and 60uA from the +3v supply.

The input resistance is greater than 600k. The output resistance is about 7k. The maximum differential input signal of the amplifier is $\pm$ 1.4 mV peak with the maximum undistorted output of $\pm$ 1.4v peak into a 200 k load and $\pm$ 0.5v into 20 k.

The gain is flat from d.c. to 300 cps with a 3 db point and 4000 cps. as shown in Fig. 7. The gain is also flat with source resistances up to 20 k. (Fig. 8) With the voltage gain set for 300 the output voltage is within $\pm$ 1% from -20°C to +60°C. The variations are somewhat greater with higher gain.

The common mode rejection is greater than 80 db from 0 to 100 cps. and greater than 70 db to 1 kc.

The low noise characteristics of the 21K5 transistors and the I_C = 5uA operating point assures low output noise. The typical noise voltages referred to the input for noise bandwidths of 125 cps, 390 cps and 1570 cps versus balanced source resistances to 100 k are shown in Fig. 9.

CONCLUSIONS

Certain advantages in differential amplifier drift performance, output noise, and input resistance can be achieved by operating the input stage at low collector currents. These advantages, precluded by the lack of suitable transistors in the past, can now be realized with the use of matched low level planar transistors. An amplifier using the low level characteristics of these transistors has been constructed and its performance described.

REFERENCES

(1) Okada, R. H., "Stable Transistor Wide-Band D-C Amplifier", AIEE Electronics and Communications, March 1960, pp. 26-33.

(2) R. D. Middlebrook and A. D. Taylor, "Differential Amplifier With Regulator Achieves High Stability, Low Drift", Electronics, p. 58, July 28, 1961.

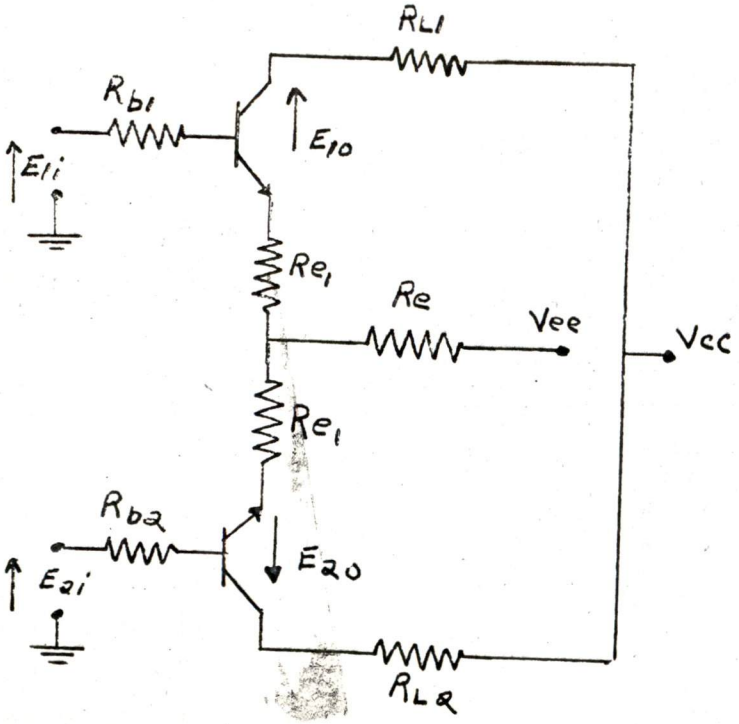


FIG. 1 DIFFERENTIAL AMPLIFIER INPUT STAGE

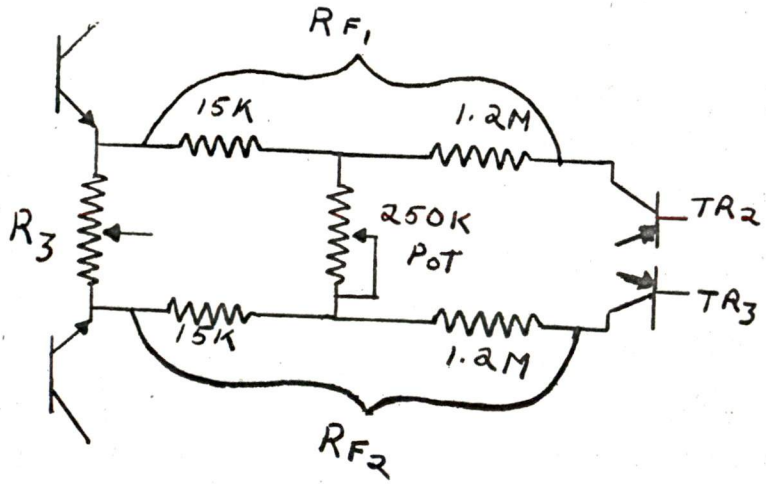
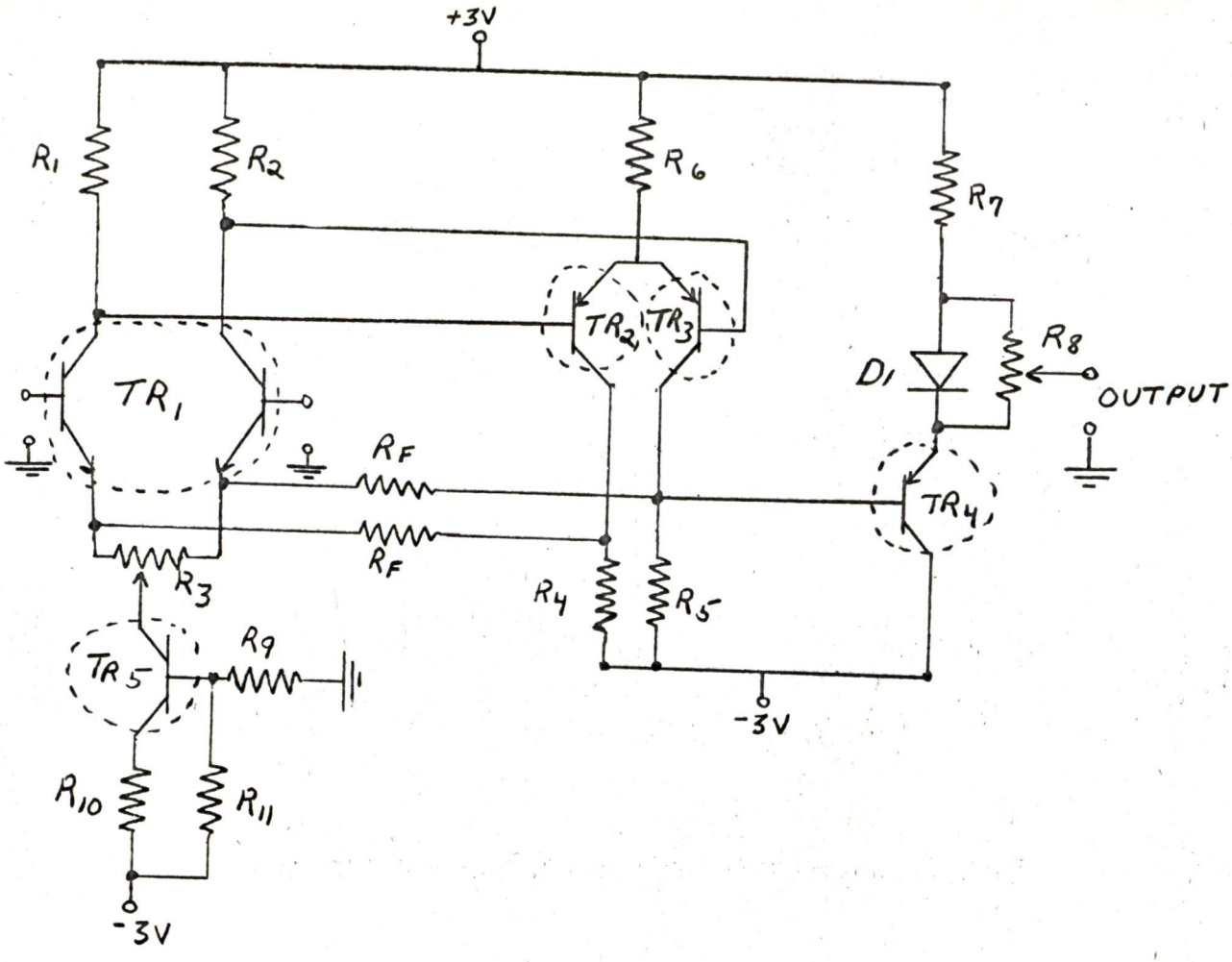


FIG. 5 GAIN CONTROL



TR_1 - 21K5

TR_2, TR_3, TR_4 - 2N2605

TR_5 - ~~2N2524~~ 2N2524

D_1 - 1N482

R_1, R_2 - 432K 1%, IRC Type RN 70B

R_4, R_5 - 249K 1%, IRC Type RN 70B

R_6, R_7 - 82K Ω ± 5% ¼ W

R_9 - 27K Ω ± 5% ¼ W

R_{10} - 120K Ω ± 5% ¼ W

R_{11} - 36K Ω ± 5% ¼ W

R_8 - 10K potentiometer, Spectro type 80-3-103

R_3 - 500 Ω potentiometer, Bourns type 200 P

FIG. 2 LOW LEVEL DIFFERENTIAL AMPLIFIER

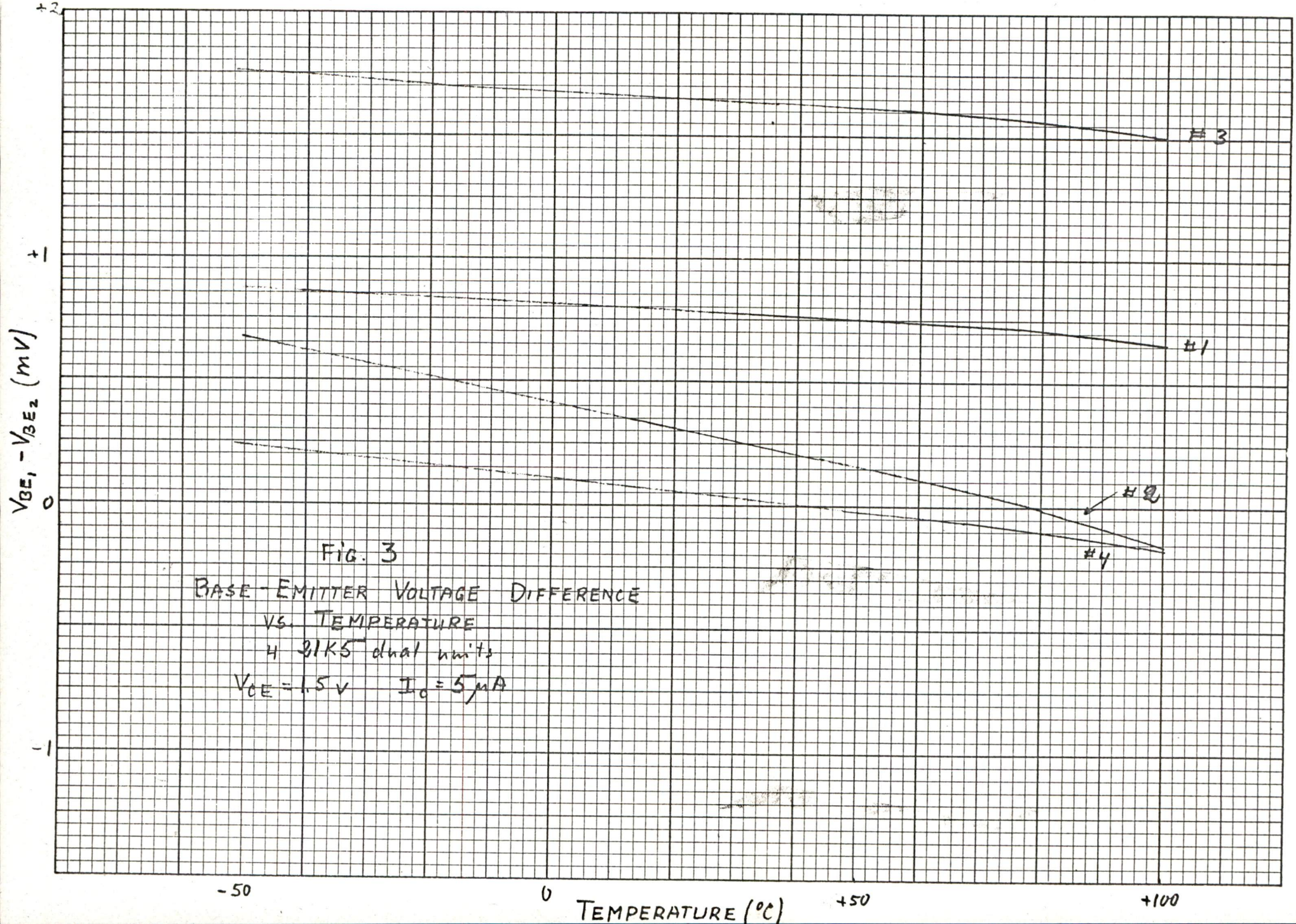


FIG. 3

BASE-EMITTER VOLTAGE DIFFERENCE VS. TEMPERATURE

4 2IK5 dual units

$V_{CE} = 1.5$ V $I_C = 5\mu$A

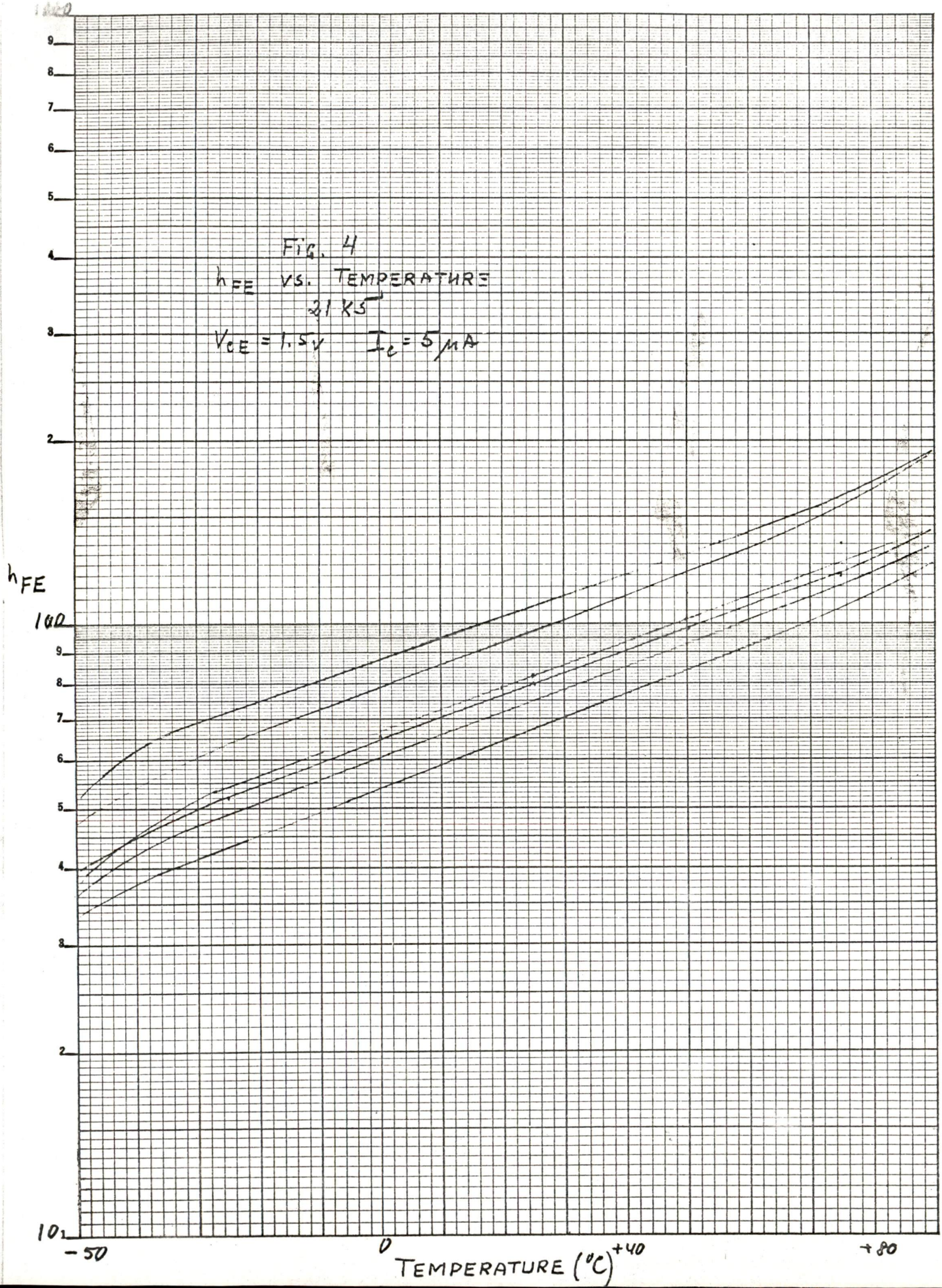


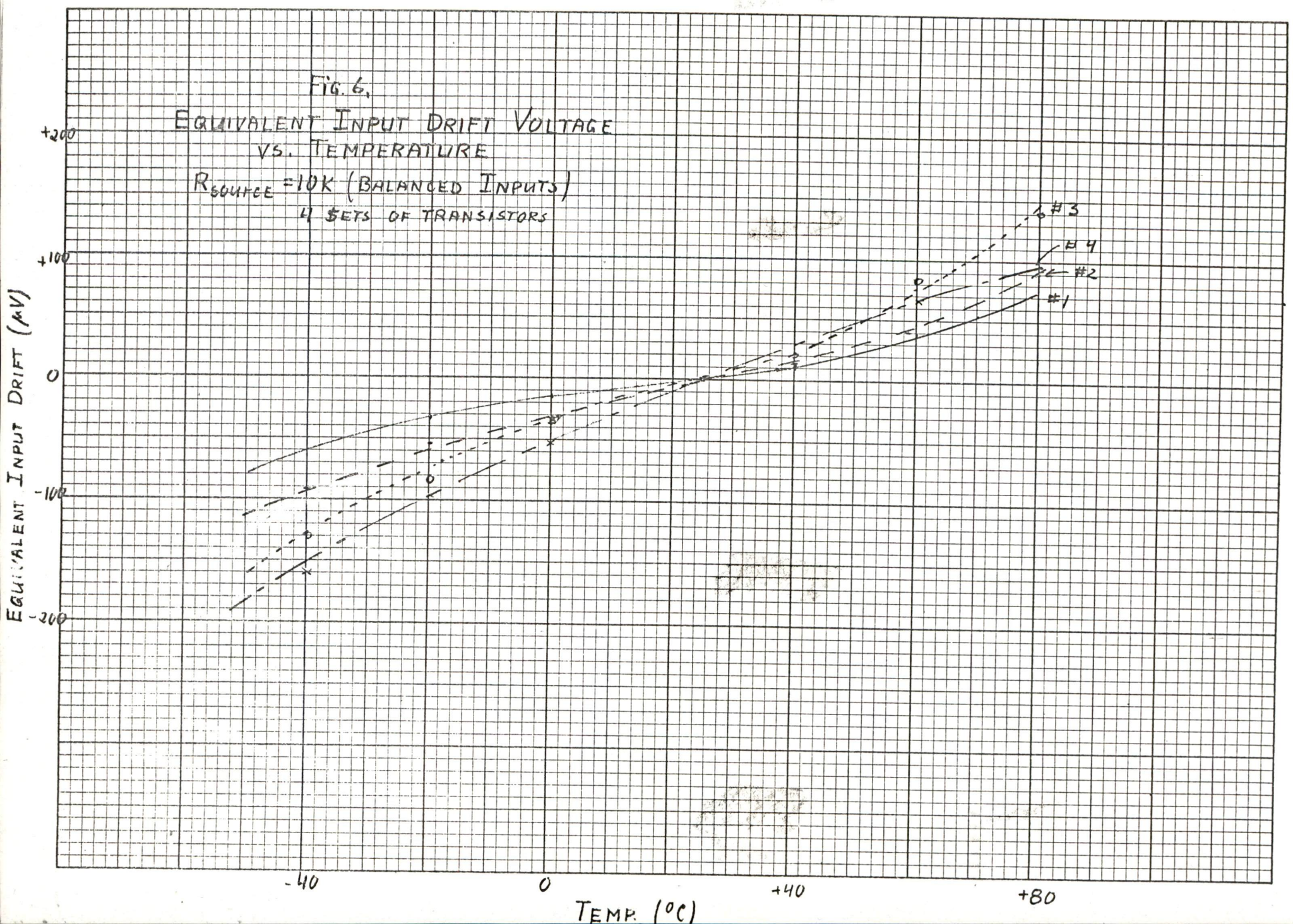
FIG. 4
h_{FE} VS. TEMPERATURE
2N5
$V_{CE} = 1.5V$ $I_C = 5\mu A$
h_{FE}
100
9
8
7
6
5
4
3
2
10
-50
0
+40
+80
TEMPERATURE (°C)

FIG. 6.

EQUIVALENT INPUT DRIFT VOLTAGE VS. TEMPERATURE

R_{SOURCE} = 10K (BALANCED INPUTS)

4 SETS OF TRANSISTORS



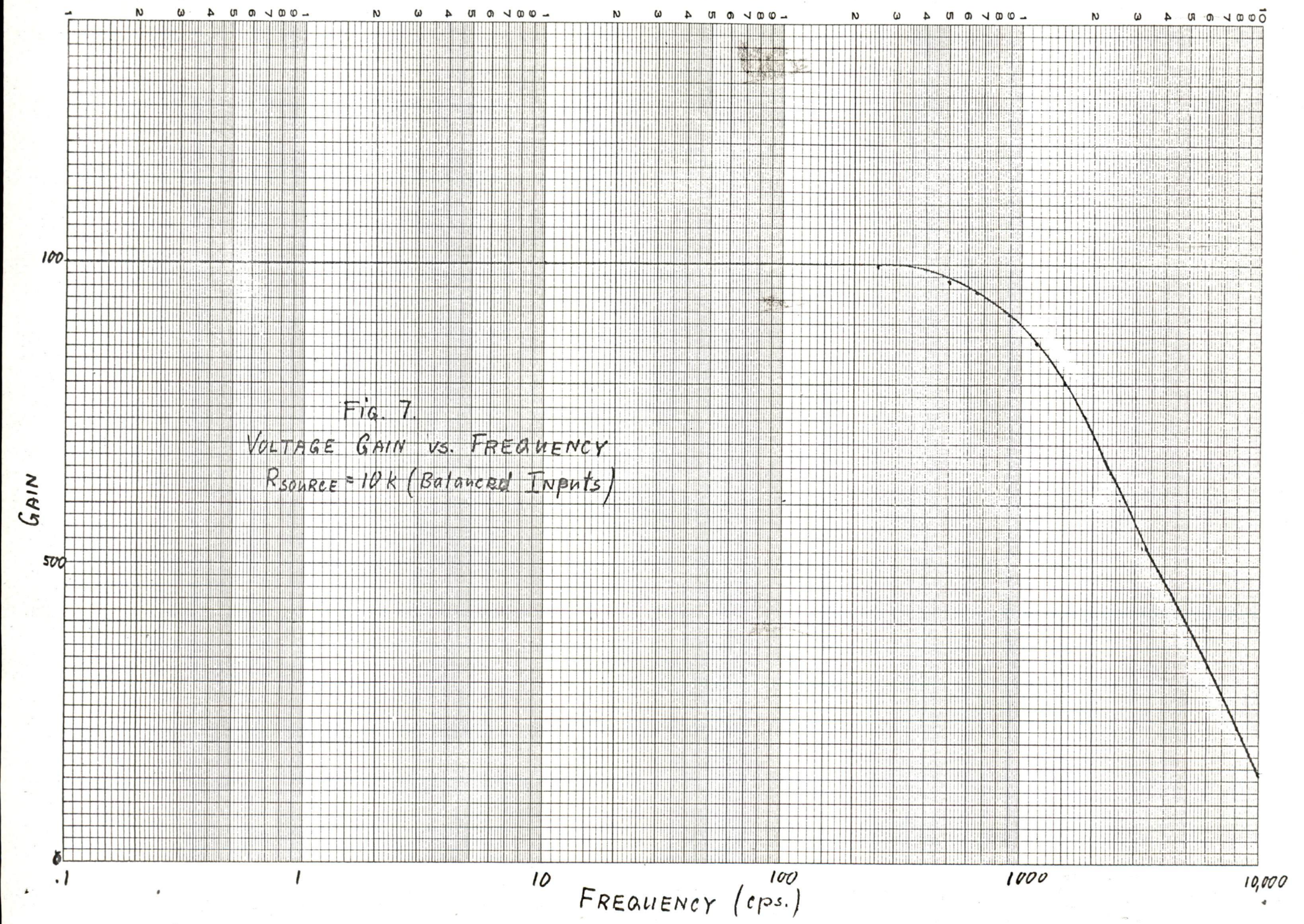


Fig. 7.
VOLTAGE GAIN VS. FREQUENCY
R_{SOURCE} = 10 k (Balanced Inputs)

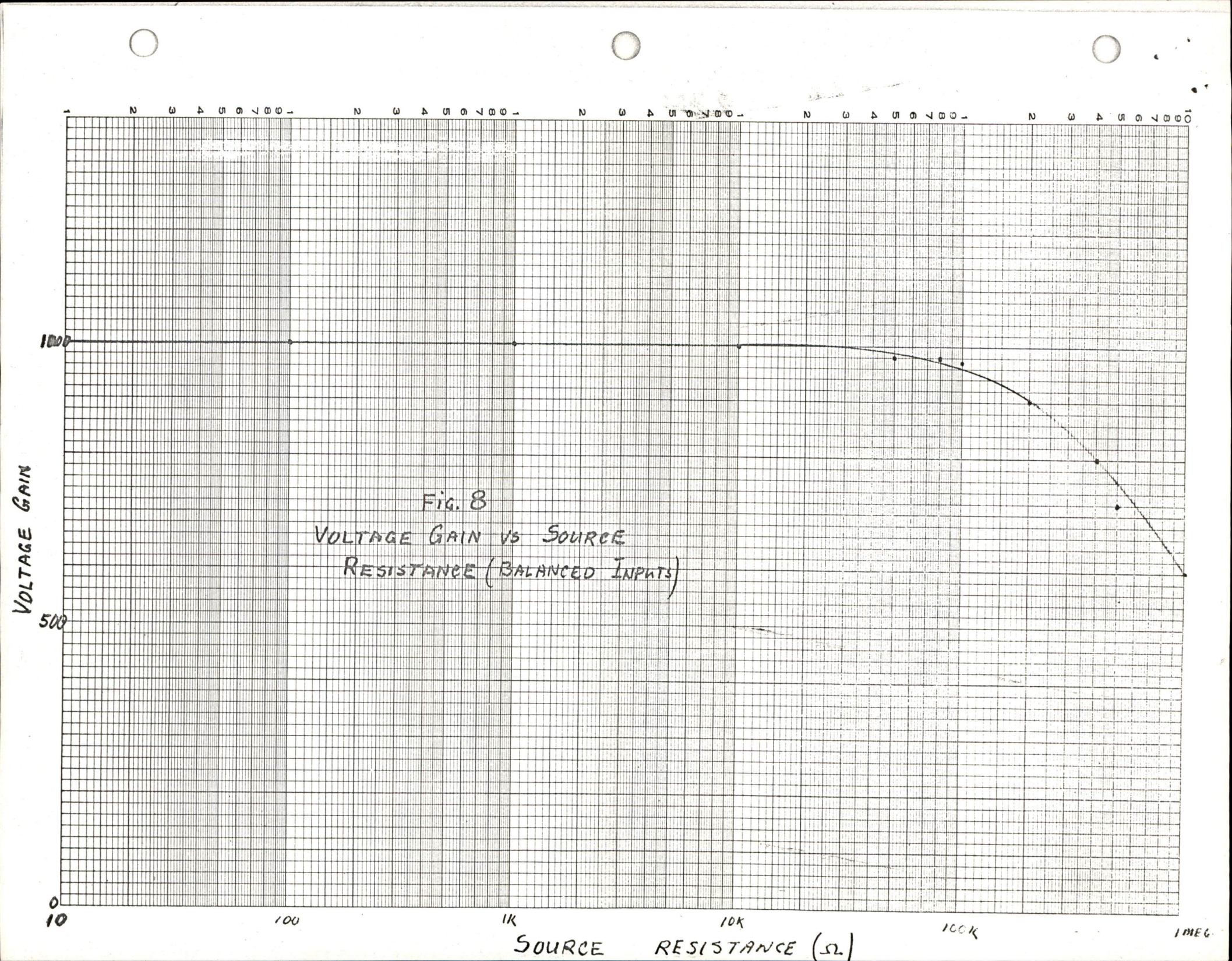


Fig. 8
VOLTAGE GAIN VS SOURCE RESISTANCE (BALANCED INPUTS)

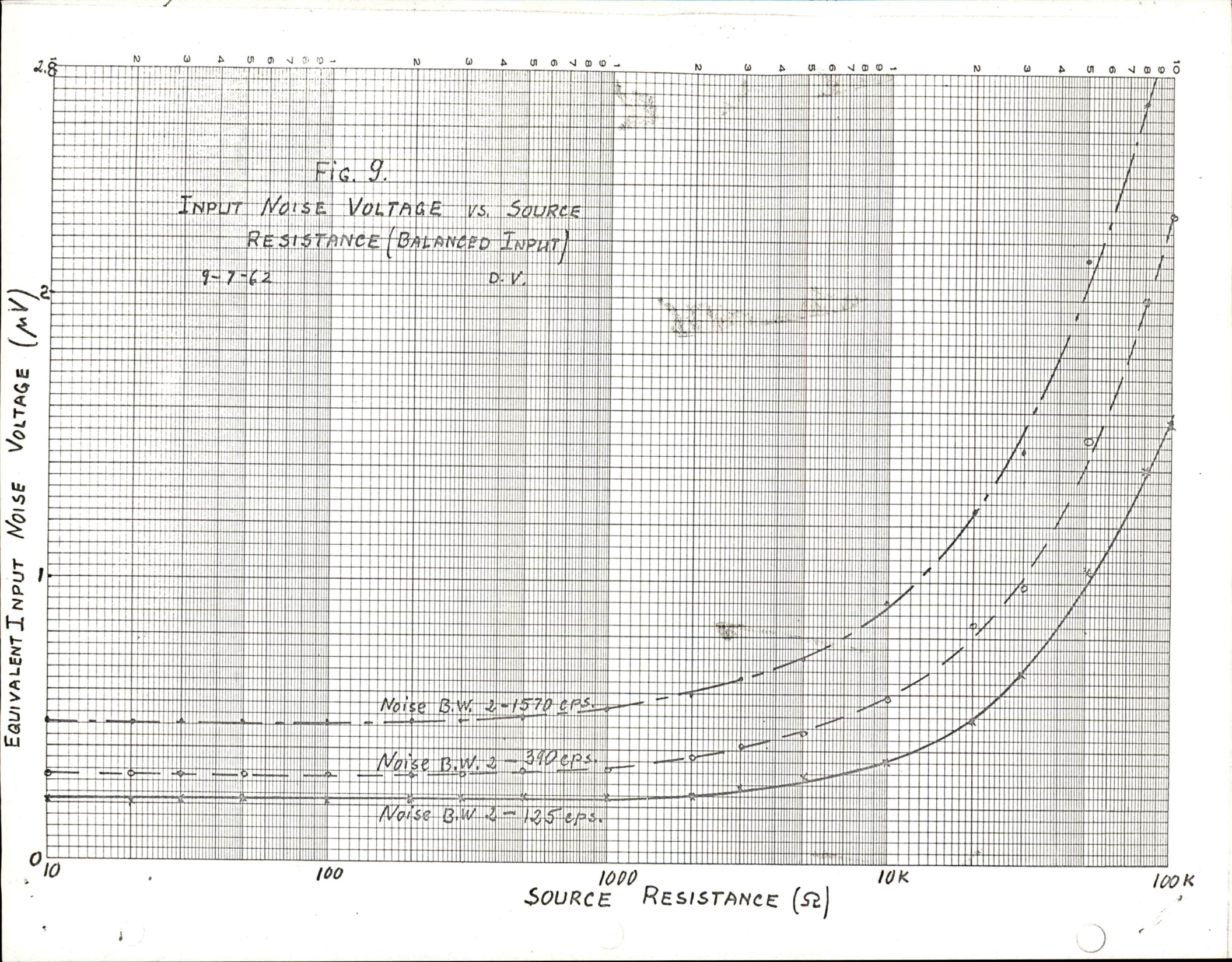


Fig. 9.
Input Noise Voltage vs. Source Resistance (Balanced Input)
9-7-62
D.V.
Equivalent Input Noise Voltage (mV)
2.8
2
1
0
Noise B.W. 2-1570 cps.
Noise B.W. 2-390 cps.
Noise B.W. 2-125 cps.
10
100
1000
10K
100K
Source Resistance (Ω)

A NEW D-C TRANSISTOR DIFFERENTIAL AMPLIFIER

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Palo Alto, California

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A NEW D-C TRANSISTOR DIFFERENTIAL AMPLIFIER

By David F. Hilbiber

The stable amplification of low-level signals of less than 1 millivolt magnitude has usually been done with a carrier-type feedback amplifier employing a complex modulation-demodulation system incorporating a short-lived and bulky mechanical chopper. The much simpler all-transistor d-c differential amplifier, however, has not been suitable due to drifts in gain and operating point during aging and temperature variations. The purpose of this paper is to relate improvements in both of these respects as a result of using planar silicon transistors described by Hoerni' and a compound transistor circuit. Equivalent input drifts of 3μV/°C to 5μV/°C have been attained over the temperature range of -70°C to +125°C, with negligible gain variations. This circuit also offers single-ended as well as differential output capabilities.

ESTABLISHMENT OF THE D-C OPERATING POINT

Okada[2] has shown for the conventional differential stage, Fig. 1, that the output function is given by:

$$E_{2o} - E_{1o} = \frac{\left[\alpha_1 R_{L1} + \alpha_2 R_{L2}\right]\left[\left(E_{1i} - E_{2i}\right) + \left(V_{BE2} - V_{BE1}\right)\right]}{\Delta} + \frac{\left[\alpha_1 R_{L1} + \alpha_2 R_{L2}\right]\left[\left(R_{b1} I_{CO1} - R_{b2} I_{CO2}\right) + \frac{V_{EE}}{R_{ee}}\left(\frac{R_{b1}}{\beta_1} - \frac{R_{b2}}{\beta_2} + R_{E1} - R_{E2}\right)\right]}{\Delta} + \left[I_{CO1} R_{L1} - I_{CO2} R_{L2}\right] \quad (1)$$

where $\Delta = R_{e1} + R_{e2} + \frac{R_{b1}}{\beta_1} + \frac{R_{b2}}{\beta_2} + \frac{R_{b1} R_{b2}}{\beta_1 \beta_2 R_{ee}}$

and where it is assumed that α is constant, $R_L \ll r_c$, and the device extrinsic resistances are included in R_{e1}, R_{e2}, R_{b1}, and R_{b2}.

To obtain the initial balance, that is when $E_{2o} - E_{1o}$ and $E_{1i} - E_{2i}$ are both zero, the remainder of Equation (1) must sum to zero. The term relating to V_{EE} may be made small if R_{ee} is sufficiently large which is readily accomplished by employing the impedance gain of a transistor operated as a current source. Then, for transistors ideally matched with respect to V_{BE} and I_{CO} the conditions of balance are fulfilled. Since such selection of units is not feasible on a production basis, the alternative is to vary the relative magnitudes of R_{e1} and R_{e2} at the expense of unequal emitter currents.

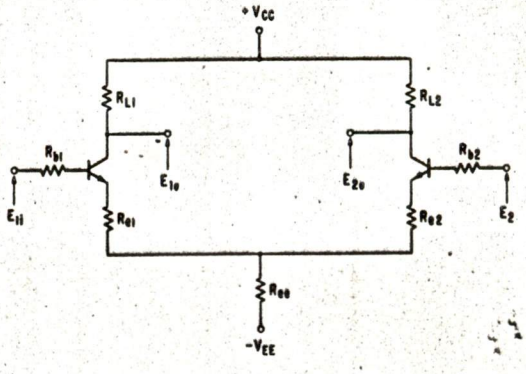

Fig. 1 The generalized transistor differential stage.

The primary factors responsible for drift of operating point are well known; specifically the thermal effects on the emitter-base voltage, current gain, and I_{CBO}. From Equation (1) it is seen that if $R_{bk} \rightarrow 0$, the effects of β_k variations are small. This, however, tends to restrict operation to very low source impedances and limits the usefulness of the stage. It is possible to alleviate this condition to a certain extent by operating at collector currents as low as possible commensurate with the output loading. A further reason to keep R_{bk} small is to minimize I_{CBO} effects. However, for the planar transistors mentioned previously[1], the magnitudes and distribution of I_{CBO} (as shown by Figure 2(a)) are such that their effects may be neglected to temperatures as high as 100°C to 125°C for source impedances of 10^3 ohms to 10^4 ohms. The most difficult obstacle to overcome is the matching of the magnitude and temperature coefficient of the emitter-base voltages, as both of these quantities are a function of current gain, emitter current, doping densities of the emitter and base at the junction and the relative magnitudes of diffusion and space-charge region recombination-generation currents.[3,4] It has been found, however, that the uniformity of characteristics inherent in the planar-diffused transistors lends to selection methods for optimum temperature matching. A typical group distribution is shown in Figure 2(b).

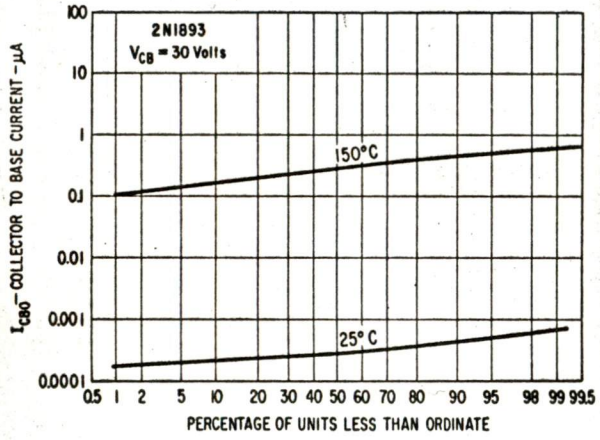

Fig. 2 (a) A typical distribution of I_{CBO} as a function of temperature, for the planar transistor.

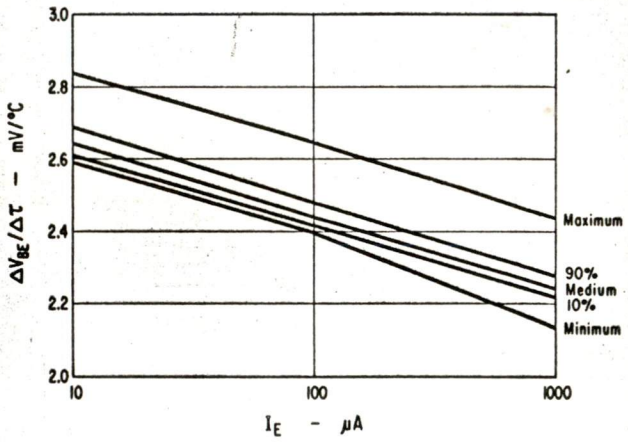

Fig. 2 (b) A typical distribution of Base-Emitter voltage temperature coefficient.

From experimental data it has been observed that the best tracking of emitter-base voltages (that is, $|V_{BE1} - V_{BE2}| \simeq 0$) is obtained when the collector currents are maintained constant with respect to temperature and loading. Since it is quite evident this requirement cannot conveniently be satisfied by the circuit of Figure 1, an alternate approach is used where the single transistors are replaced by equivalent three-terminal PNP/NPN compound transistor blocks. The basic circuit is shown in Figure 3. The collector current of Q_1, I_{C1}, is given by

$$I_{C1} = I_{B2} + \frac{V_1}{R_1} \qquad (2)$$

where I_{B2} is the base current of Q_2, V_1 is the voltage across R_1, and $I_{C1} < I_{C2}$ assumed. Further,

$$V_1 = V_{D1} + V_{BE2}$$

$$= V_{D1}(T) + V_{BE2}(T)$$

For a P-N junction in avalanche breakdown, the voltage is a function of temperature as given by

$$V_R = V_{Ro} + \gamma_R (T - T_o)$$

where γ_R is the temperature coefficient of the reverse breakdown voltage. Also, γ_R is a function of V_R and I_R,

$$\gamma_R = K_R (V - V') \qquad (K_R > 0)$$

where $K_R \simeq 1.1$ mv/°C/V and $V' = V'(I_R) \simeq 4.6$ to 5.0 volts. Since the temperature coefficient of voltage of a forward biased junction is given by

$$V_F = V_{Fo} + \gamma_F (T - T_o)$$

where $\gamma_F = \gamma_F \; I_F$ and $\gamma_F < 0$ at the operating levels of interest, then it is immediately apparent that V_1 can be made to increase, decrease, or remain constant with temperature by the proper selection of D_1. Equation (2) may be written

$$I_{C1} = I_{B2}(T) + \frac{\left(V_{BE2_0} + V_{D1_0}\right) + \left(\gamma_R + \gamma_F\right)(T - T_o)}{R_1}$$

For I_{C1} to remain constant with temperature,

$$\frac{\partial I_{C1}}{\partial T} = \frac{\partial I_{B2}}{\partial T} + \frac{\gamma_R + \gamma_F}{R_1} = 0 \qquad (3)$$

where $\frac{\partial I_{b2}}{\partial T}$ is usually a negative quantity as current gain normally increases with temperature. Thus, by the proper selection of D_1

$$\frac{\partial I_{B2}}{\partial T} + \frac{\gamma_R + \gamma_F}{R_1} \cong 0$$

The compound block also has a considerably higher current gain than the single transistor stage. Referring to Figure 3;

$$I'_C = I_1 + I_{E2} = I_1 + (1 + \beta_2) I_{B2}$$

and

$$I'_B = I_{C1}/\beta_1 = (I_1 + I_{B2})/\beta_1$$

therefore,

$$\beta' = I'_C/I'_B = \beta_1 \left[1 + \beta_2 \frac{I_{B2}}{I_1 + I_{B2}}\right] \qquad (4)$$

Then, if R_1 is chosen such that $I_{C1} < I_{C2}$ by an order of magnitude, I'_B is proportionately reduced compared to what it would be for the single transistor case. The reduction if I_{B1} compared to the circuit of Figure 1 permits operation from high source impedances if this is desired.

An extension of the PNP/NPN compound block having higher current gain is shown in Figure 4. The three-terminal current gain of this circuit is readily found to be

$$\beta^* = \beta_1 \left[1 + \frac{\beta_2 (1 + \beta_3) I_{B2}}{I_{B2} + I_1} \right] \qquad (5)$$

I_{C1} is maintained constant as before, but for a given I'_C, I_{B2} is smaller than for the two transistor block and hence I_{C1} may be reduced considerably. While the latter circuit results in very small input biasing currents the limitation on source impedance is again determined by I_{CBO} temperature considerations.

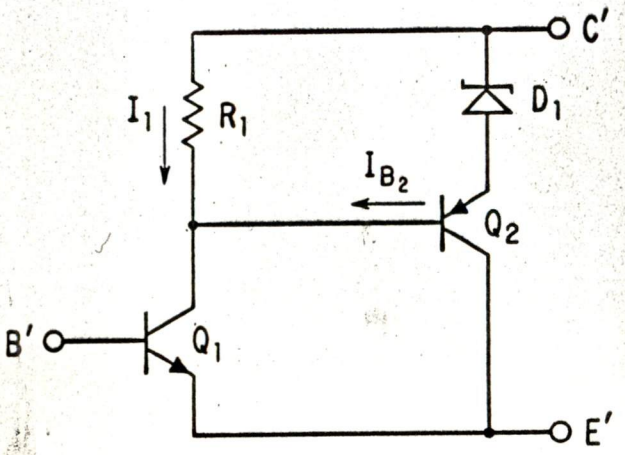

Fig. 3 The PNP/NPN compound block.

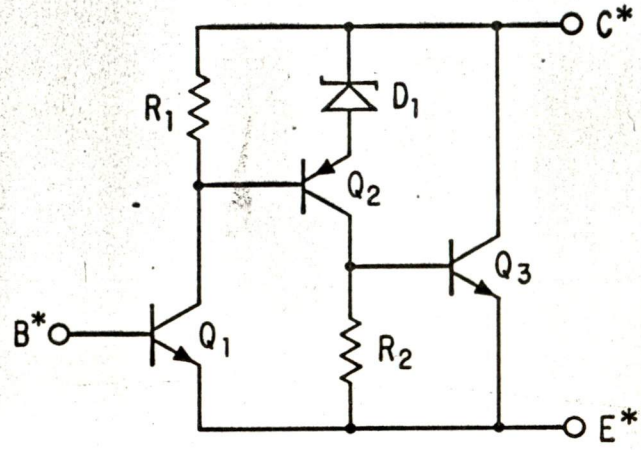

Fig. 4 An extension of the compound block, having higher gain.

Previously, only the electrical aspects of the amplifier have been considered. In packaging an assembly where the input transistor pairs are thermally separated such that temperature differentials could readily exist, the following effects will be present. Since the V_{BE} temperature coefficients are from 2 mV/°C to 3 mV/ °C in magnitude, than a ΔT of 0.01°C represents an apparent signal input of 20 μV to 30 μV. To overcome this very serious obstacle, units have been fabricated using two selected devices in a single TO-5 package, which under worse conditions gives small gradients having short duration. A further consideration concerns the device dissipation and thermal resistance.[5] For all practical junction devices where emitter and collector junctions are close together, the device collector dissipation and thermal resistance determine the temperature at the emitter. Hence low frequency signals create temperature variations at the emitter. These temperature changes associated with the emitter-base voltage temperature coefficient result in a thermally generated feedback voltage. This phenomenon is minimized by operating at low collector currents and voltages.

Specific examples of these amplifiers are the circuits shown in Figures 5 and 6 using the two-transistor and three-transistor blocks, respectively, which have been designed for optimum d-c performance. Matched input transistors provide equivalent input drifts in the range of 3 μV/°C to 5 μV/°C which have been attained over the range of -70°C to +125°C. Eight hour stability for the two-transistor block is approximately $\pm$12 μV with a 330 ohm source impedance and $\pm$ 16 μV for a 2500 ohm input and the three-transistor block drifts are halved. The circuit is insensitive to power supply variations. No selection is required with respect to V_{BE} of the PNP units. Operation is improved, however, if the current gains are somewhat matched.

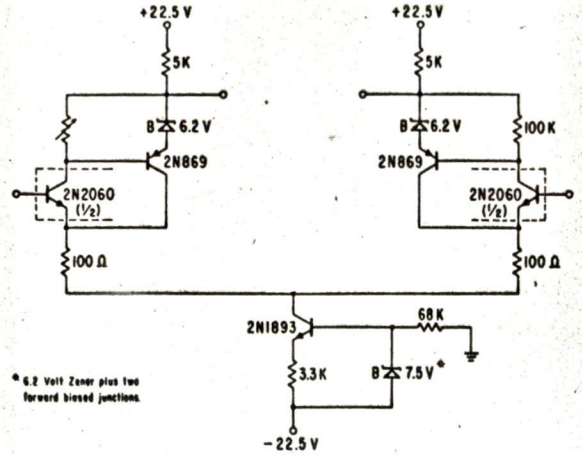

Fig. 5 The improved differential amplifier using the two-transistor block.

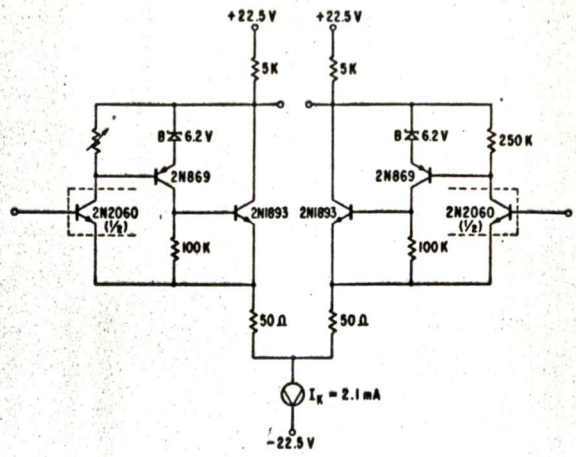

Fig. 6 The improved differential amplifier using the three-transistor block.

THE AMPLIFIER SMALL-SIGNAL CHARACTERISTICS

In addition to d-c stability criteria for the amplifier discussed, the designer must consider the incremental or small-signal behaviour. It is desired to make the circuit voltage gain insensitive to device parameter variations. The amplifier is analyzed here on the basis of the single-ended equivalent stage and a new method of determining optimum circuit resistance values is given.

Employing the conventional h-parameter notation, the voltage gain of common-emitter transistor stage with series emitter resistance is given by (see Appendix I):

$$A_v = \frac{-h_f R_L}{\left[h_i + (1 + h_f) R_e\right] + R_L (\Delta^h + h_o R_e)} \qquad (6)$$

where common emitter h-parameters are implied, and R_L and R_e are the collector and emitter resistances, respectively. For an ideal transistor ($r_e = r_b = 0$, $r_c = \infty$, $\alpha = 1.0$) the voltage gain is given by the ratio R_L/R_e. To determine how closely the actual gain approaches this number, Equation (6) is written

$$A_v = g\left(\frac{h_f}{1 + h_f}\right) \frac{1}{1 + \lambda}$$

where $g = \frac{R_L}{R_e}$, the ideal transistor gain, and

$$\lambda = \frac{1}{1 + h_f}\left(g R_e h_o + \frac{h_i}{R_e} + g\Delta^h\right)$$

The voltage gain will approach the ideal value as $h_f \longrightarrow \infty$ and $\lambda \longrightarrow 0$. It is obvious that λ may be minimized by an optimum R_e, which is readily obtained

$$\frac{d\lambda}{dR_e} = \frac{1}{1 + h_f}\left(g h_o - \frac{h_i}{R_e^2}\right) = 0$$

Solving for R_e,

$$R_e \text{ (opt.)} = \left(\frac{h_i}{g h_o}\right)^{1/2} \qquad (7)$$

A design criteria is thus established which permits the greatest independence of transistor parameters for a specified stage gain. Although $A_v < g$, the difference is normally quite small, and R_L may be increased slightly to achieve the desired gain. It is apparent that this optimization is also applicable to the three-terminal PNP/NPN compound blocks using the appropriate simplified h-parameters developed in Appendix II. Figure 7 is a family of curves (calculated) of g_o vs. g for the single transistor and the compound blocks assuming $R_e = R_e$ (opt.) and $R_e = 0.05\ R_e$ (opt.), using a typical 2N1893, where $g_o = A_v/g$.

The input resistance is also of interest since this determines the loading placed upon the source. This is related by (see Appendix I):

$$R_{IN} = \frac{h_i + \left(1 + h_f\right) R_e + R_L \left(\Delta^h + h_o R_e\right)}{1 + h_o R_L} \qquad (8)$$

The input resistance (calculated) corresponding to a given g is shown by the curves of Figure 8, for $R_e = R_e$ (opt.) and $R_e = 0.05\ R_e$ (opt.).

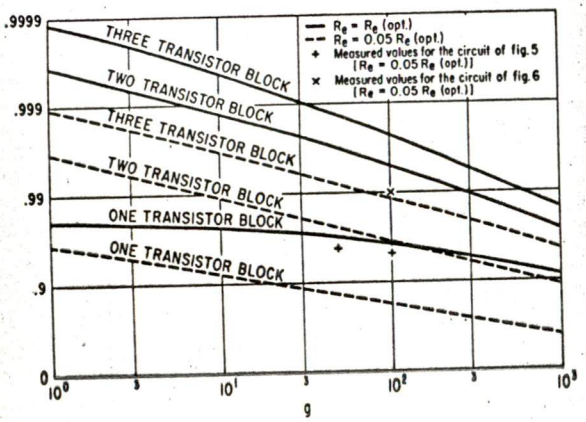

Fig. 7 Normalized gain, g_o, as a function of g ($g = R_L R_e$) for $R_e = R_e$ (opt.) and $R_e = .05\ R_e$ (opt.).

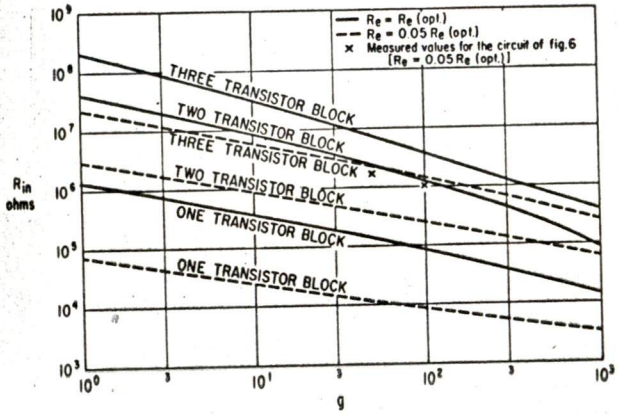

Fig. 8 Input resistance as a function of g for $R_e = R_e$ (opt.) and $R_e = .05\ R_e$ (opt.).

Experimental data obtained with the single-ended equivalent stage are in good agreement with the predicted behaviour. It should be noted that the optimum R_e for the circuit examples of Figures 5 and 6 was not selected for practical reasons. For the circuit of Figure 6 with a desired voltage gain of 100, R_e (opt.) = 1.03 KΩ and R_L = 103 K. Since $I'_c \simeq 1$ ma, the required collector supply would be 115 volts. The schematic values shown were selected to permit operation from reduced supply voltages. The curves of Figure 7 indicate the extent that the gain performance is degraded by using $R_e \ll R_e$ (opt.). The advantage of the multi-transistor block is quite evident in this respect, as g_o decreases much less than for the single transistor case.

TRANSISTOR CHARACTERISTICS FOR AN OPTIMIZED D-C AMPLIFIER

From Equation (1), it is immediately apparent that I_{CO} must be small, the base-emitter voltages must be well matched (essential to realize equal input-transistor collector currents), and the transistors must have similar current gains. One necessary condition in realizing these requirements is that surface effects be kept small. The oxide protected surface on planar units allows one to achieve this quite well. The planar diffused junction transistor has an excellent uniformity with respect to emitter and base sensitive characteristics making feasible a production type matching selection.

In addition, the Early effect in the transistor must be kept small to minimize h_o and h_r. This is best realized by having the collector doping much lighter than the base (ideally an abrupt junction), such that the depletion layer variations occur primarily in the collector. For this reason high β units are not desirable as high β implies narrow base width and an increased Early effect sensitivity.

CONCLUSION

The amplifier described compares favorably with many commercially available chopper types with respect to temperature drift and gain stability. The circuit is extremely simple and easily packages as shown by Figure 9.

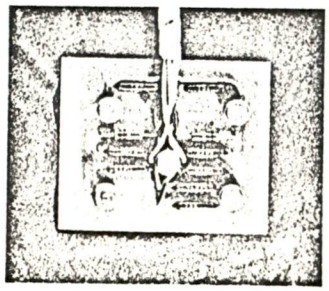

Fig. 9 Printed circuit board version of amplifier shown in Fig. 5.

While optimum gain behavior has been stressed, it is possible to effect compromises such as increased input impedance with an increased transistor dependence. The maximum bandwidth is of the order of 10^4 cps to 10^5 cps, but by rolling off at lower frequencies, equivalent input noise may be reduced considerably.

The writer gratefully acknowledges the many helpful discussion with Drs. V.H. Grinich and C.T. Sah and the patience and care of Messrs. R. Robson and E. Oliver in fabricating the devices and circuits used.

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APPENDIX I

The common-emitter stage with series emitter resistance may be characterized by an equivalent set of h"-parameters as given by:[6]

$$h_i'' = \frac{h_i + R_e\left(1 + h_f + \Delta^h - h_r\right)}{1 + h_o R_e}$$

$$h_f'' = \frac{h_f - h_o R_e}{1 + h_o R_e}$$

$$h_r'' = \frac{h_r + h_o R_e}{1 + h_o R_e}$$

$$h_o'' = \frac{h_o}{1 + h_o R_e}$$

where R_e is the series emitter resistance and common emitter parameters are implied. For the transistors used in the amplifier, it is noted

$$h_r \lll 1, \text{ and } h_o R_e \ll 1.$$

Then,

$$h_i'' = h_i + \left(1 + h_f\right) R_e \tag{A1}$$

$$h_f'' = h_f \tag{A2}$$

$$h_r'' = h_r + h_o R_e \tag{A3}$$

$$h_o'' = h_o \tag{A4}$$

Further, the voltage gain of a transistor stage is given by:[6]

$$A_v = \frac{-h_f R_L}{h_i + (\Delta^h) R_L}$$

where $\Delta^h = h_i h_o - h_f h_r$. Substituting in the h" parameters obtained above:

$$A_v = \frac{-h_f R_L}{h_i + \left(1 + h_f\right) R_e + R_L\left(\Delta^h + h_o R_e\right)} \tag{A5}$$

The input resistance of the common emitter resistance is given by:[6]

$$R_{IN} = \frac{h_i + (\Delta^h) R_L}{1 + h_o R_L}$$

With the h" parameters substituted, this becomes:

$$R_{IN} = \frac{h_i + \left(1 + h_f\right) R_e + R_L\left(\Delta^h + h_o R_e\right)}{1 + h_o R_L} \tag{A6}$$

APPENDIX II

The three-terminal n-transistor block may be characterized by an equivalent set of h'-parameters. Consider the circuit of Figure 3, having the block diagram shown in Figure 10 (a). To simplify the diagram, R_1 and the dynamic impedance of D_1 are included in the h parameters of Q_2 such that

$$h'_{i2} = \frac{R_1\left(h_{i2} + h_{f2}R_{D1}\right)}{R_1 + h_{i2} + h_{f2}R_{D1}} \tag{A7}$$

$$\text{and } h'_{f2} = h_{f2}\frac{R_1}{R_1 + h'_{i2}} \tag{A8}$$

The signal flow graph[7] corresponding to Figure 10 (a) is shown in Figure 10 (b). From the flow graph, the following relationships are obtained by inspection:

$$h'_i = \frac{h_{i1}\left(1 + h_{o1}h'_{i2}\right) - h_{f1}h_{r1}h'_{i2}}{1 + h_{o1}h'_{i2}}$$

$$h'_f = \frac{-h_{f1}h'_{f2}}{1 + h_{o1}h'_{i2}}$$

$$h'_r = \frac{h_{r1}h_{r2}}{1 + h_{o1}h'_{i2}}$$

$$h'_o = \frac{h_{o2}\left(1 + h_{o1}h'_{i2}\right) - h'_{f2}h_{r2}h_{o1}}{1 + h_{o1}h'_{i2}}$$

Since from the d-c operating bias conditions $I_{C1} \cong 0.1\ I_{C2}$, then it follows that $h_{o1} < h_{o2}$, and as a consequence $h_{o1}h'_{i2} << 1$. Further, since $h_{i1} > h_{i2}$, $h_{f1}h_{r1} << 1$, and $\left(1 - h_{r2}\right) <<< 1$, then the h' notations may be simplified to:

$$h'_i = h_{i1} \tag{A9}$$

$$h'_f = -h_{f1}h'_{f2} \tag{A10}$$

$$h'_r = h_{r1} \tag{A11}$$

$$h'_o = h_{o2} - h'_{f2}h_{o1} \tag{A12}$$

It must be noted that h_{k1} parameters used are for the common emitter configuration, and h_{k2} imply common collector.

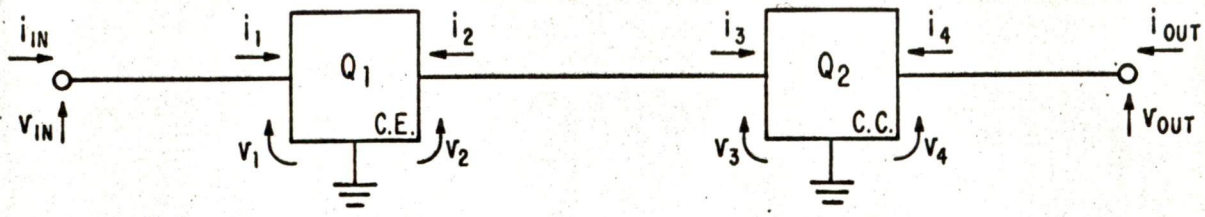

Fig. 10 (a) The block diagram of the two-transistor circuit of Fig. 3.

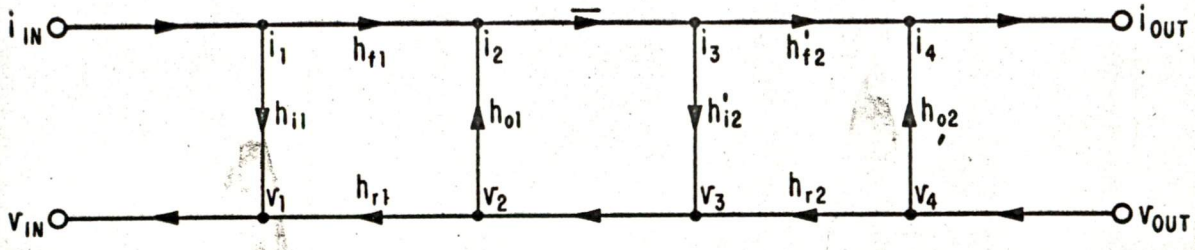

Fig. 10 (b) The associated signal-flow-graph.

The circuit of Figure 4 is analyzed in a similar manner, (See Figure 11). The complete expressions for the h*-parameters are found to be:

$$h^*_i = \frac{h_{i1}(D) - h^*_{i2}\left[h_{f1}h_{r1}\left(1 + h_{o2}h^*_{i3}\right)\right] - h^*_{i3}\left[h_{f1}h_{r1}\left(1 + h^*_{f2}\right)\left(1 - h_{r2}\right)\right]}{D}$$

$$h^*_f = \frac{-h_{f1}\left[h^*_{f2}\left(1 + h^*_{f3}\right) - h_{o2}h^*_{i3}\right]}{D}$$

$$h^*_r = \frac{h_{r1}\left[h_{r2}\left(1 - h_{r3}\right) + h_{r3} + h_{o2}h^*_{i3}\right]}{D}$$

$$h^*_o = \frac{h_{o3}(D) + h_{o2}\left[\left(1 + h^*_{f3}\right)\left(1 - h_{r3}\right)\right] - h_{o1}\left[h^*_{f2}h_{r2}\left(1 + h^*_{f3}\right)\left(1 - h_{r3}\right)\right]}{D} + \frac{h^*_{fe}h_{r3}\left(1 + h^*_{f2}\right)\left(1 - h_{r2}\right)}{D}$$

where $D = 1 + h_{o1}\left[h^*_{i2}\left(1 + h_{o2}h^*_{i3}\right) + h_{i3}\left(1 + h^*_{f2}\right)\left(1 - h_{r2}\right)\right] + h_{o2}h^*_{i3}$

and h^*_{i2} and h^*_{f2} are determined by the relationships given in Equations (A7) and (A8) respectively. Further, h^*_{i3} and h^*_{f3} are modified to include R_2. Using similar assumptions concerning relative magnitudes

as for the two-transistor case, the h*-parameters may then be reduced to:

$$h^*_i = h_{i1} \tag{A13}$$

$$h^*_f = -h_{f1}\left[h^*_{f2}\left(1 + h^*_{f3}\right)\right] \tag{A14}$$

$$h^*_r = h_{r1} \tag{A15}$$

$$h^*_o = h_{o3} + h_{o2}\left(1 + h^*_{f3}\right) - h_{o1}\left[h_{f2}\left(1 + h^*_{f3}\right)\right] \tag{A16}$$

where h_{k1} and h_{k3} parameters are for the common emitter configuration and h_{k2} are common collector.

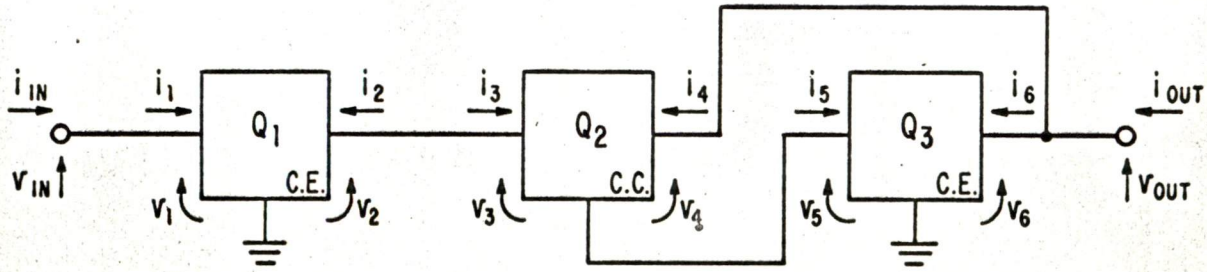

Fig. 11 (a) The block diagram of the three-transistor circuit.

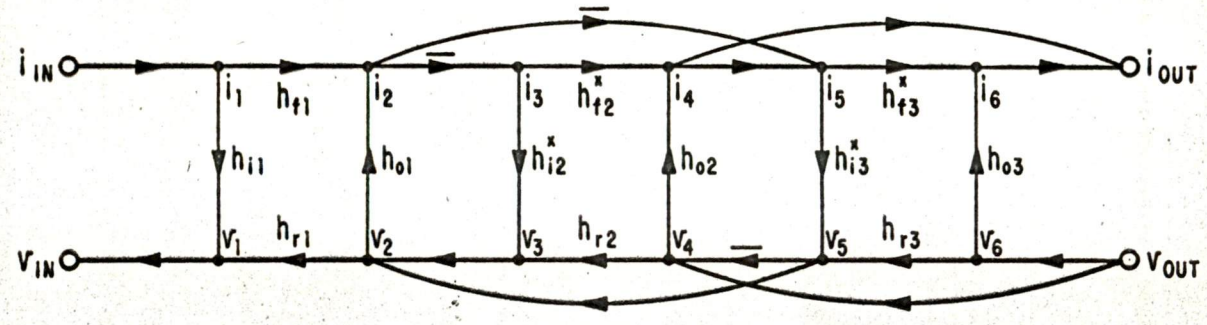

Fig. 11 (b) The signal-flow-graph