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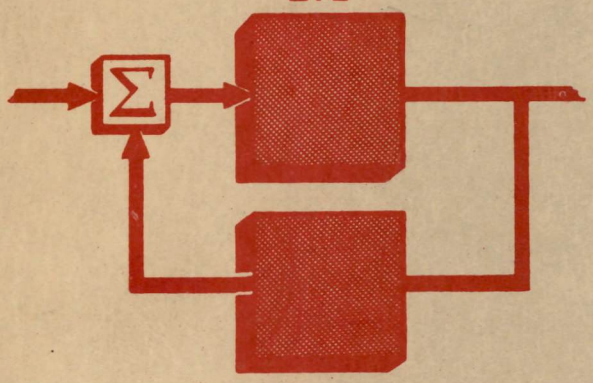
Design of an Eight-Pole Magnetic-Matrix Switch

By

John W. Brean



Report No. 6506-ER-45

Contract W33-038ac-13969

SERVOMECHANISMS LABORATORY

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

CAMBRIDGE 39, MASS.

ENGINEERING REPORT 6506-ER-45

SERVOMECHANISMS LABORATORY
ELECTRICAL ENGINEERING DEPARTMENT
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Project No. D.I.C. 6506

SUBJECT: Design of An Eight-Pole Magnetic-Matrix Switch

REFERENCE: Contract No. W33-038ac-13969

FILE INDEX: Switches, Magnetic Matrix
Timing References

ABSTRACT: This report describes the design of an eight-pole saturable-core magnetic-matrix switch and its use with an eleven-stage binary counter to generate consecutive eight-digit binary numbers for time coding of recorded data. The switch was designed to operate at 8 steps per second and has a maximum step delay of 0.1 millisecond. The model switch contains ten saturable-core transformers and is a plug-in unit embedded in plastic. The external dimensions are 5-1/2" by 1-7/8" by 2-5/8".

July 31, 1953

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I. INTRODUCTION

This report describes the design of a saturable-core magnetic matrix and its use as a fast-operating eight-position stepping switch to read binary numbers stored in an electronic binary counter. The matrix switch and the binary counter are components of an instrumentation system developed at M.I.T. for flight-test evaluation of airborne fire-control equipment.(1) The matrix switch, designed as a replacement for a mechanical stepping switch, is an adaptation of a magnetic matrix developed at the M.I.T. Digital Computer Laboratory for pulse distribution.(2)

The instrumentation equipment simultaneously records data by means of two synchronized movie cameras and a multi-channel recording oscillograph. Exact time synchronization is required between all data records, and this is provided by a time code generated by the binary counter and the magnetic-matrix switch.

The matrix is made up of eight magnetic-switch elements arranged so that the last eight stages of an eleven-stage counter are sensed singly and in a predetermined, repeated sequence. The existence or nonexistence of the matrix output signal during the observation period of a given stage is determined by the "1" or "0" condition of the stage being sensed. The idealized matrix output, which is a modulated 400-cps carrier as in Fig. 1, represents consecutive eight-digit binary numbers produced one digit at a time. One digit is produced for each rotation of the master camera shutter, and the code is transferred to the films by means of small neon lamps.

The model of the switch which has been constructed is a bank of ten matrix-connected toroidal transformers stacked horizontally on an aluminum plate 5-1/4 inches by 1-5/8 inches by 1/4 inch (see Fig. 2). Eight of the transformers have five windings each, and two have three windings

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(1) Instruction Manual for A-2 Fire-Control System Test Instrumentation, Engineering Report 6506-ER-29, J. M. Fiore, M.I.T. Servomechanisms Laboratory, May 31, 1951.

(2) A Magnetic-Matrix Switch and Its Incorporation into a Coincident-Current Memory, R-211, Kenneth H. Olsen, M.I.T. Digital Computer Laboratory, June 6, 1952.

each. The finished assembly is embedded in plastic with the connecting leads brought out through a 32-pin plug connector, and the overall dimensions are 5-1/2 inches by 1-7/8 inches by 2-5/8 inches (see Fig. 3). The physical size of a switch of this type could be greatly reduced by using smaller cores; however, for ease in handling, cores with one-inch inside diameters were chosen for the construction of the initial model.

The magnetic-matrix switch has been designed as a replacement for an eight-pole solenoid-operated stepping switch previously used for the same purpose. Although the mechanical stepping switch has been used successfully, it has given trouble because of variable time delays, excessive vibration, and overheating during continuous operation. In the model of the magnetic-matrix switch which has been constructed, the step-delay time is 0.1 millisecond. The stepping rate is limited by the reaction of the matrix transformers on the associated electronic flip flops in the binary counter. Reliable switch operation at eight steps per second was the design criterion, and the switch was found to operate satisfactorily up to 20 steps per second. The actual upper limit on the stepping rate was not determined.

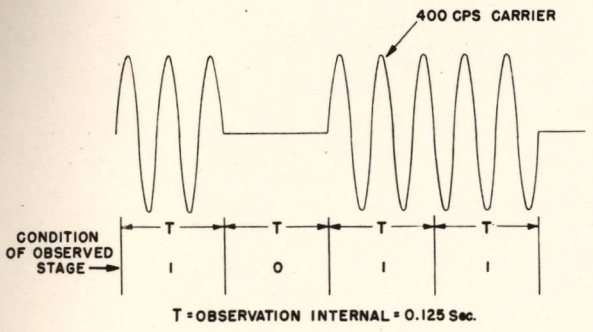

Fig. 1 - Ideal Matrix Output

It should be noted that, although the binary counter and matrix switch described in this report are capable of providing a binary code in response to any series of electrical pulses, their use in camera instrumentation systems is to provide a time code which is synchronous with the camera operation. It has been suggested by Arma Corporation that, since the code itself is predetermined, it can be generated from a tape which is run synchronously with the camera film. Arma Corporation has built and tested a coder which consists of a 16-millimeter magazine driven at half camera film speed by a direct mechanical drive from the camera. The time code, consisting of consecutive ten-digit binary numbers, is punched in a 50-foot film strip in the magazine and is read by a simple electrical

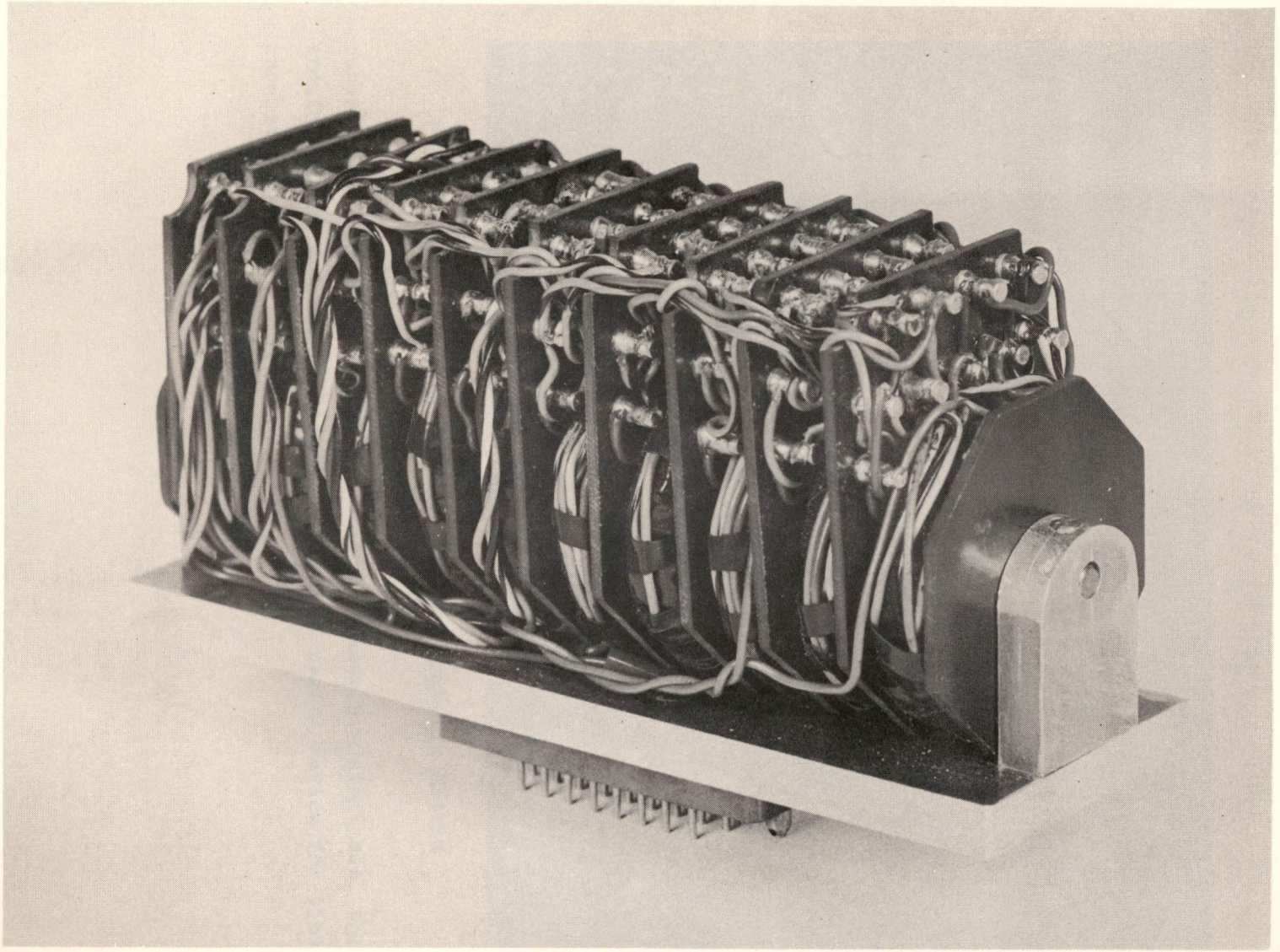

Fig. 2 - Assembled Magnetic Matrix Before Embedding

contact for operation of coding lamps. Where such a mechanically driven coder is feasible, it should be considered as a desirable replacement for the more complicated electronic counter and switch described in this

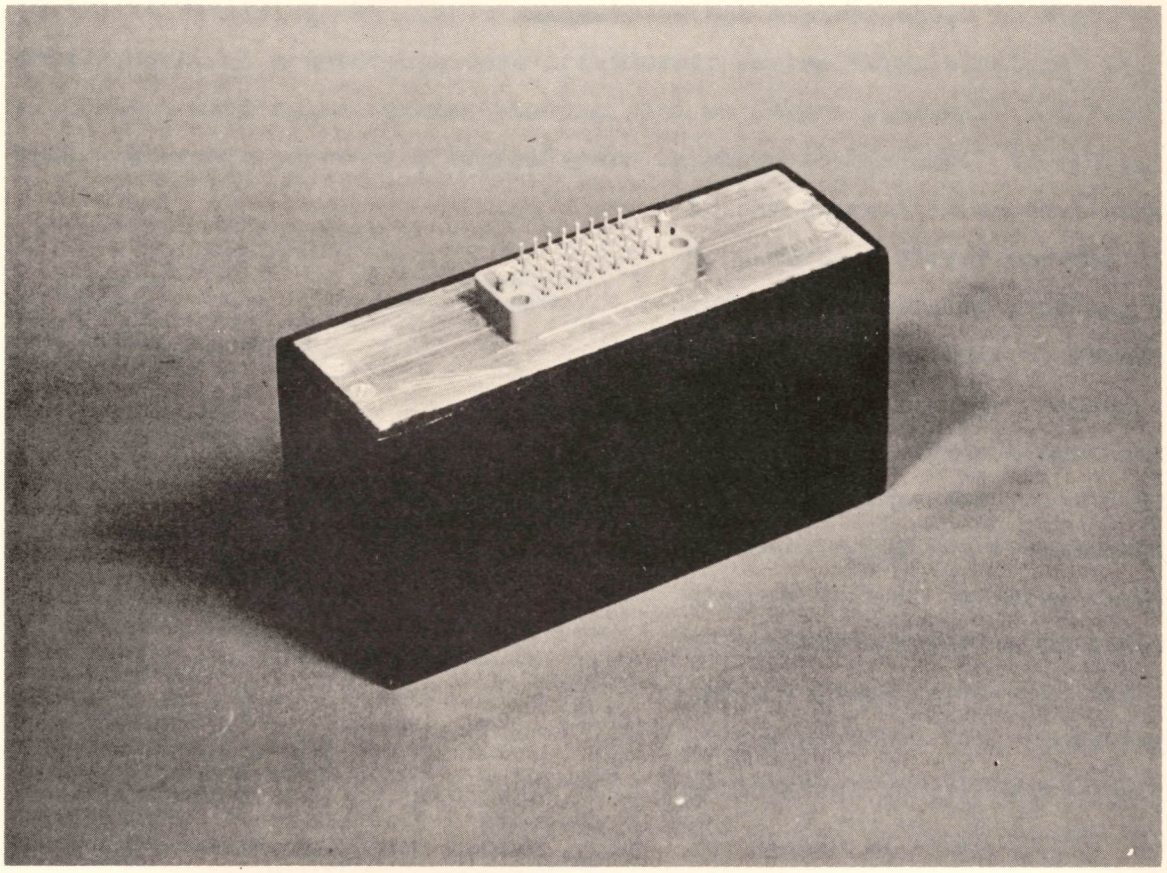

Fig. 3 - Assembled and Embedded Magnetic Matrix

report. If only electrical synchronizing pulses are available, the electronic counter and switch has proved to be a useful device for time code generation.

II. DESCRIPTION OF THE MATRIX OPERATION

A. The Magnetic Switch Principle

The principle of operation of the matrix switch can be illustrated by examining the simple magnetic-switch element shown in Fig. 4a. This element is a saturable-core transformer having three windings: an excitation winding, a sensing winding, and an output winding. The idealized hysteresis curve of a typical core is shown in Fig. 4b. Switching in the element is accomplished by passing a direct current through the sensing winding, of sufficient magnitude to saturate the core. The switch action is as follows: When a sinusoidal voltage is impressed on the excitation winding and the sensing winding current is zero, normal transformer action takes place and a voltage appears at the output winding. The operating point about which the sinusoidal mmf varies is shown in Fig. 4b as Operating Point 1. If now a direct current is caused to flow through the sensing winding, a constant magnetizing force is superposed on the sinusoidal one; and the operating point is forced into the region of saturation indicated as Operating Point 2. During operation about Point 2, the core permeability is reduced to unity, negligible coupling exists between the excitation and output windings, and essentially zero voltage appears at the output.

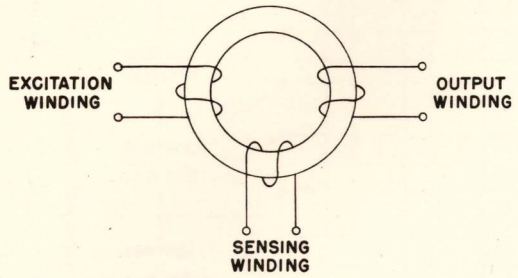

FIG. 4a

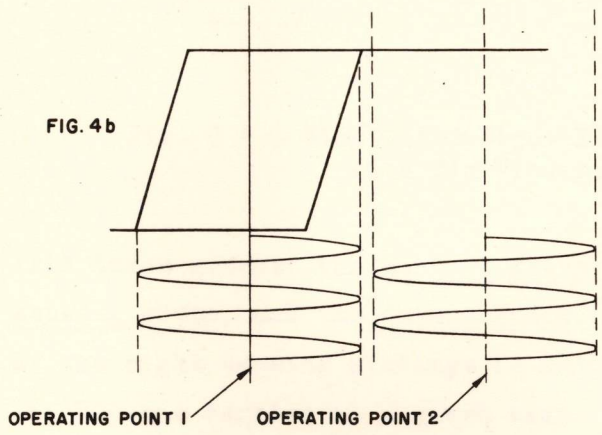

FIG. 4b

Fig. 4 - A Simplified Element and an Idealized Hysteresis Curve of a Typical Magnetic Core

B. The Matrix Configuration

The principle of core saturation for switching is used in the generalized matrix shown in Fig. 5. Each toroidal transformer core (shown as a straight core for simplicity), together with its windings, is called an element. The circuits into which the windings are connected are divided

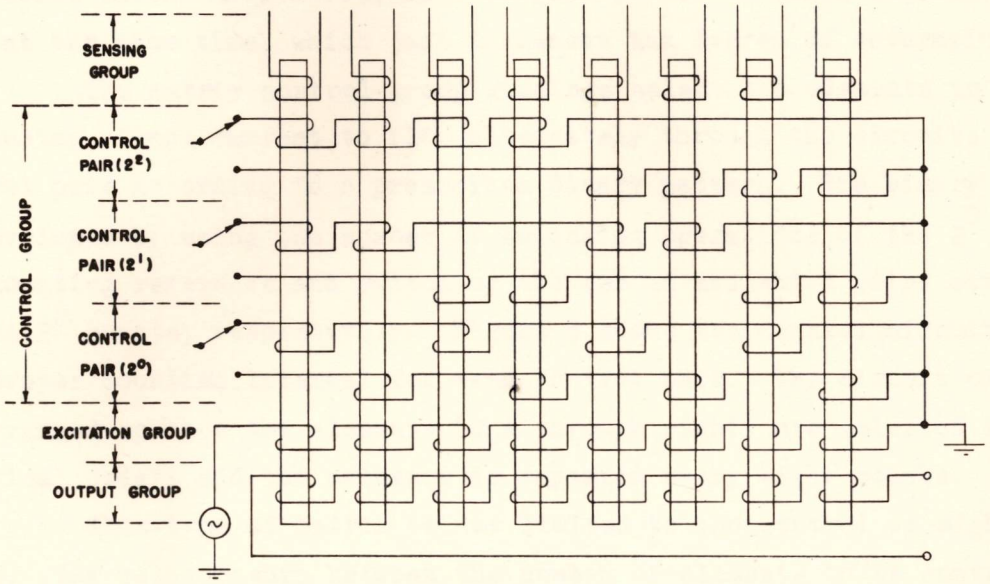

Fig. 5 - A Simplified Eight-Element Magnetic-Matrix Switch with Six Windings per Element

into three groups: the control group consisting of control pairs, the sensing group, and the output group. The control group determines which of the eight sensing windings is allowed to control the transmission of the 400-cps carrier at a given time. Each sensing winding, when chosen by the control group, is capable of blocking or allowing the transmission of the carrier, depending on the sensing winding current. A single output is obtained by connecting the eight windings of the output group in series.

Each element in the matrix of Fig. 5 has six windings. Three of the windings correspond to the sensing, excitation, and output windings described above for the simple element. The three additional windings which have been added to each element are interconnected in the control group (or matrix selector circuits). The six circuits of the control group are divided into three control pairs which are called the 2^0 pair,

2^1 pair, and 2^2 pair, as indicated. When direct current is caused to flow through one circuit in each control pair, control winding mmf appears in all but one of the element cores and forces them into the saturated condition represented by Operating Point 2 of Fig. 4b. The one element not subjected to control-winding saturation is free to operate as the simple element described above, and is called the selected element. Note that some cores in the matrix will have current in two or three control windings at the same time, which just increases the degree of saturation.

The matrix control-group windings select the elements in order by causing direct current to flow alternately through the circuits of each control pair according to a prescribed binary pattern. The binary pattern is developed by using the number of switching operations of the 2^0 pair as the counting reference and switching the second and third pairs after every 2^1 and 2^2 counts, respectively. Figure 5 shows the control circuits and the proper counting interval for each control pair. The circuit of Fig. 5 is arranged so that the elements (one through eight) are selected in their numerical order, and the sequence is repeated every eight counts.

This type of matrix is not limited to the control of eight elements. The relationship between the number of elements to be controlled and the required number of control pairs is: To control 2^n elements, n control pairs are required. For example, five control pairs must be provided to control 32 (2^5) elements.

C. Use of the Matrix and Counter to Generate Eight-Digit Binary Numbers

In order to obtain the desired series of consecutive eight-digit binary numbers, it is necessary to read (or sense) the last eight stages of the eleven-stage counter in order and in a repeated sequence. These are Stages 2^3 through 2^{10}. The binary number represented by the eight counting stages increases by "one" for every eight (2^3) camera pulses entering the counter, and it is therefore necessary to read one counting stage for each camera pulse. Figure 6 illustrates the binary number represented in the counting stages after 0, 8, 16, 24, 32 camera pulses.

A convenient method of reading a counting stage is to insert the sensing winding of a matrix element in series with one flip-flop cathode

of that stage.[1] In this manner, the cathode current and the consequent saturation condition of the matrix element indicates the binary digit represented. When an element is selected, the presence of an output voltage from the element shows that no current is flowing in the sensed half of the corresponding flip flops; and this condition is designated as binary digit "1." Conversely if no voltage appears at the element output, current flow is indicated in the sensed half of the flip flop; and this condition is designated as binary digit "0."

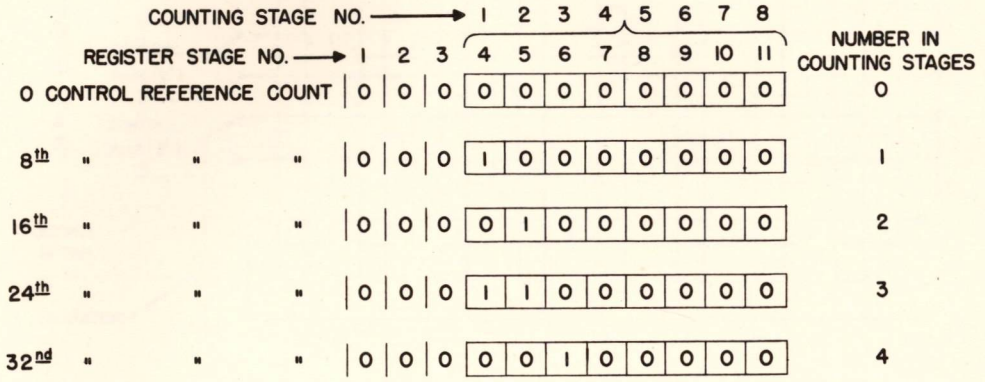

Fig. 6 - The Binary Number in the Counting Stages at the 0, 8, 16, 24, and 32 Control-Reference Counts

The matrix is made to select the elements corresponding to the eight counting stages in the desired order by connecting the 2^0, 2^1, and 2^2 circuits of the control group to the 2^0, 2^1, and 2^2 stages, respectively, of the counter. Thus, for every eight pulses entering the counter, the matrix selects and reads in sequence the eight digits of the binary number stored in the last eight stages. The order in which the counting stages are sensed is from the eighth (2^{10}) through the first (2^3) in a repeated sequence.

D. A Modification of the Basic Matrix

In the model switch which has been constructed, the number of windings required on each element was reduced from six to five by replacing

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[1] See Figure 9, Section IV, where the sensing windings are labeled s_1, s_2, s_3, etc.

the direct current in the 2^0 (counting reference) control pair by the sinusoidal excitation, eleminating the need for a separate winding on each element for excitation. The element-selecting ability of the matrix control circuits is not affected by this simplification. Figure 7 shows the simplified matrix.

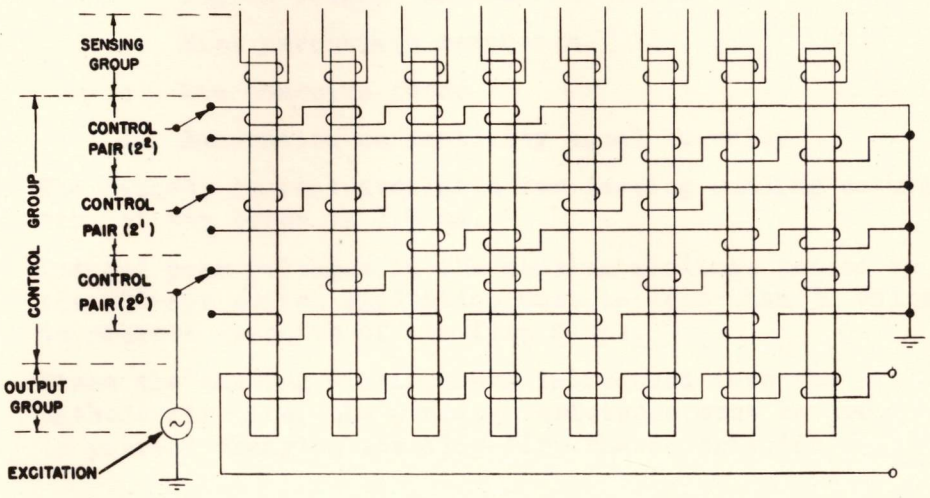

Fig. 7 - A Simplified Eight-Element Magnetic-Matrix Switch with Five Windings per Element

In the simplified matrix, the introduction of the a-c excitation through the 2^0 control pair requires a means for direct-current control of the excitation. This control is provided by adding two three-winding elements to the 2^0 control circuits as shown in Fig. 7. The principle of core saturation is applied in these elements as in the simple element previously described. The two control elements receive their excitation from a common a-c source.

III. DESIGN PARAMETERS AND PROCEDURES FOR THE MATRIX

From the theory of element operation and an analysis of the binary-counter stages, the following design parameters were assumed:

1. The core material must have the following characteristics:
   a. High effective permeability in the region between saturation limits
   b. High percentage remanence
   c. Low coercive force
   d. Saturation permeability equal to unity
2. The cathode current available for sensing winding saturation of the cores is 7.5 ma.
3. Induced peak voltages in the sensing windings caused by the 400-cps switch excitation must be less than 30 volts to prevent coercion of the flip flops.
4. Since the sensing windings are introduced into the cathode circuits, the winding resistance must be low to prevent changing the flip-flop characteristics.

After an investigation of core materials[1], the magnetic core material chosen was Delta-Max, a 50 per cent Ni - 50 per cent Fe, grain-oriented alloy which is produced in ribbon form and wound into toroids of various sizes. The core dimensions used in this matrix are 1-21/64" O.D. by 59/64" I.D. by 13/64" thick. The cores are encased in nylon covers, the dimensions of which are 1-1/4" O.D. by 1" I.D. by 1/4" thick. The ribbon used in the cores is 2 mils thick.

The manufacturer's hysteresis plot of a typical core is shown in Fig. 8.

It was found from an examination of 50 cores that the characteristics of Delta-Max are not sufficiently uniform to allow duplication of excitation and output windings on any two cores[1]; therefore, it was necessary to compute turns and turns ratios from the measured hysteresis curves of each core.

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[1] Investigation and Selection of Core Material for a Saturable-Core Magnetic-Matrix Switch, Engineering Memorandum 6506-EM-28, J. W. Brean, M.I.T. Servomechanisms Laboratory, Cambridge 39, Massachusetts.

In these computations the region between the two thresholds of saturation on each hysteresis curve was chosen as the unbiased operating range for the excitation mmf.

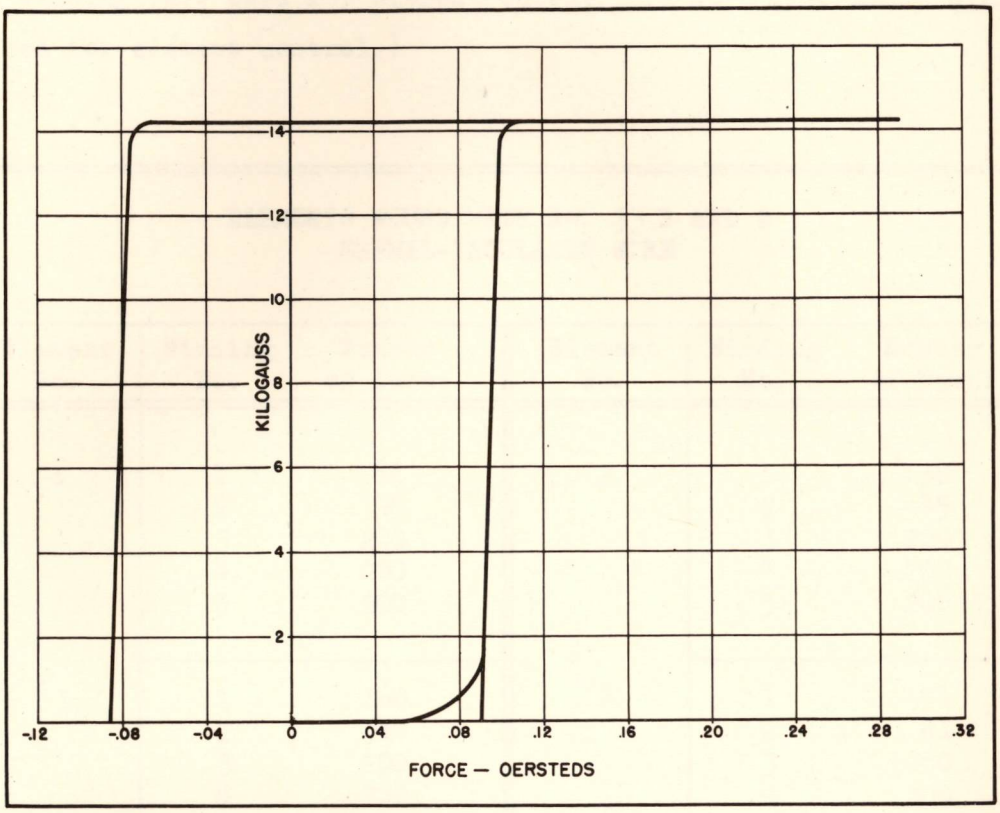


Fig. 8 - Manufacturer's Hysteresis Plot
of a Typical Delta-Max Core

The impedance across each of the 2^0 excitation-control circuits was expected to vary appreciably during the selecting sequence as a result of the nonuniformity in the element windings. To provide a constant current source for these excitation-control circuits, a series resistance was inserted in each of the circuits. An excitation current of 15 peak a-c ma. was chosen to excite the matrix.

The number of excitation and output turns for each core to produce 3.5 peak output volts was computed using the maximum permeability shown by the measured hysteresis curves and the sinusoidal excitation current. The sensing and d-c control windings were determined by using an experimentally obtained approximation: one d-c ampere-turn will saturate

a Delta-Max core sufficiently to prevent transmission of five 400-cycle a-c ampere turns. This approximation is crude, and cut-and-try changes were necessary in some cases. The following chart shows the final number of turns on the elements. (No. 1 windings are used for element excitation; No. 2 windings are used for element output; and No. 3, 4, and 5 windings are used for element control.)

ELEMENTS WOUND WITH NO. 33 B AND S ENAMEL-INSULATED WIRE

Element No.	Winding No.	Number of Turns	Element No.	Winding No.	Number of Turns
1	1	161	2	1	132
	2	45		2	45
	3	200		3	200
	4	200		4	200
	5	200		5	200
3	1	160	4	1	151
	2	40		2	41
	3	200		3	200
	4	200		4	200
	5	200		5	200
5	1	175	6	1	133
	2	48		2	69
	3	200		3	200
	4	200		4	200
	5	200		5	200
7	1	140	8	1	151
	2	71		2	50
	3	225		3	200
	4	225		4	200
	5	225		5	200
9	1	151	10	1	140
	2	235		2	215
	3	600		3	600

IV. THE COMBINED MAGNETIC MATRIX AND BINARY COUNTER

The model matrix was assembled with the elements stacked horizontally on an aluminum plate 5-1/4" by 1-5/8" by 1/4" as in Fig. 2. The assembly is embedded in plastic with the connecting leads brought out through a 32-pin plug connector. The dimensions of the embedded matrix are 5-1/2" by 1-7/8" by 2-5/8". The circuit of the model matrix is shown in Fig. 9, and its action will be described in three parts: the sensing circuits, the control circuits, and the output circuits.

A. The Sensing Circuits

The sensing windings of the matrix elements are connected in series with one cathode of each counting stage of the binary counter. When the state of the flip flop is such that no current flows in the sensing winding of a selected element, a voltage appears at the output winding of that element and a "1" is indicated. If current does flow in the sensing winding of the selected element, the element is saturated so that no voltage appears at the output and a "0" is indicated. By-pass condensers which act as transient filters are placed across each sensing winding. These condensers prevent switching transients from coercing the flip-flop stages. In Counting Stage 7, it was necessary to add a constant bias circuit to insure that the current of Stage 7 would saturate Element 5. The circuit consists of resistors R_1 and R_2 shown in Fig. 9.

B. The Control Circuits

The control pairs are operated by the flip-flop action of the first three stages of the counter. The 2^0 control pair is connected by the d-c control elements to the first stage of the counter, which provides the reference count and alternates the excitation between the circuits of the pair at every count. The 2^1 control pair operates directly from the cathode currents of the second stage of the counter. This stage alternates the control currents between the circuits of this pair after every two control reference counts. The 2^2 control pair operates from the cathode currents of the third stage of the counter. This stage alternates the control currents between the circuits of this pair after every fourth control reference count.

STAGES 7 TO 11 SAME AS STAGE 6 EXCEPT R_1 & R_2 IN STAGE "10 ONLY *

STAGE 1 | STAGE-2 | STAGE-3 | STAGE-4 | STAGE-5 | STAGE-6

NEON LAMP I-1 | NEON LAMP I-2 | NEON LAMP I-3 | NEON LAMP I-4 | NEON LAMP I-5 | NEON LAMP I-6

V-2 6AL5 | V-4 6AL5 | V-6 6AL5 | V-8 6AL5 | V-10 6AL5 | V-12

R-1 25K | R-2 50K | -75 V D.C. | GM RELAY | K-1 | +300V | V-1 6C4

R-4 5K 1/2W | R-5 30K 2W | R-6 500K 1W | R-7 10K 2W | .001 C-2 | R-8 20K 2W | R-9 200K | R-10 100K | R-11 10K 1W | C-3 .01 | C-4 .01 | C-5 .01 | R-12 100K | R-13 200K | R-14 15K 2W | R-15 5K 1/2W | 12AU7 V-3 2°b | 2°a | D.C. CONTROL WINDING FOR 2° CONTROL PAIR

R-16 20K 2W | R-17 200K | R-18 100K | R-19 10K 1W | C-6 .01 | C-7 .1 μfd | C-8 .1 μfd | R-20 100K | R-21 200K | R-22 15K | R-23 5K | 12AU7 V-5 2'b | 2'a | .05 | 2' CONTROL PAIR

R-24 20K 2W | R-25 200K | R-26 100K | R-27 10K 1W | C-9 .01 | C-10 50 μμf | C-11 50 μμf | R-28 100K | R-29 200K | R-30 15K | R-31 5K | 12AU7 V-7 2^2b | 2^2a | .1 | R-32 2M | 2^2 CONTROL PAIR

R-32 20K 2W | R-33 200K | R-34 100K | R-35 10K 1W | C-12 .01 | C-13 50 μμf | C-14 50 μμf | R-36 100K | R-37 200K | R-38 15K | R-39 5K | 12AU7 V-9 | S_8 | .05 | .01

R-40 20K 2W | R-41 200K | R-42 100K | R-43 10K 1W | C-15 .01 | C-16 50 μμf | C-17 50 μμf | R-44 100K | R-45 200K | R-46 15K | R-47 5K | 12AU7 V-11 | S_7 | .05 | 820Ω | .01

R-48 20K 2W | R-49 200K | R-50 100K | R-51 10K 1W | C-18 .01 | C-19 50 μμf | C-20 50 μμf | R-52 100K | R-53 200K | R-54 15K | R-55 5K | 12AU7 V-13 | S_6 | .05 | .01

TO ALL HEATERS

COUNTING STAGES

STAGE #1 | #2 | #3 | #11 | #10 | #9 | #8 | #7 | #6 | #5 | #4

PINS-8

S_1 S_2 S_3 S_4 S_5 S_6 S_7 S_8

2°b | 2°a CONTROL PAIR | 2'b | 2' CONTROL PAIR | 2'a | EXCIT. AND 2° CONTROL PAIR

1K 20W | ELEMENT #10 | 1K 20W | ELEMENT #9 | DC CONTROL WINDINGS FOR 2° CONTROL PAIR

ELEMENT No'S 1 2 3 4 5 6 7 8

+300 V.D.C. | TRACKING CAMERA CODING LAMP | TRIGGER INPUT FROM TRACKING CAMERA | COUNTER RESET | BINARY CODE TO OSCILLOGRAPH | PHOTO OBSERVER CAMERA CODING LAMP | 24 V.D.C. TO CONTROL BOX COUNTER

A B C D E F G H I

AN-3102-20-16S

24 V.D.C. SHIELD | +300V.D.C. INPUT | -75 V.D.C. | 6.3 V.A.C. | 60 V. FILTERED 400 CYCLES 6.3 V.A.C.

A B C D E F G

AN-3102-16S-1P

BLANKING RELAY IN JUNCTION BOX #1

NE-2 IN CAMERA | NE-1G IN CAMERA | +300V | +300V

EXCITATION TEST | 1K 25W | FILTERED 115 V 400~

EXCITATION CONTROL LOCATED IN BINARY COUNTER POWER SUPPLY

250K | .001 | 67 V.A.C. | 1.25 V.A.C. | 12AX7 | 500K 1/2 W | 100K 1/2 W | -75 V.D.C. | .1 μfd | 3K | 66 V.A.C. | 47 MEG. | 12AT7

+300 TEST | TEST #3 | 5.1K | 33K 1W | 33K 1W | 51K | TEST #2 | R_3 .51 MEG. | .51 MEG. | C_1 .004 | 10K 5W | CW | 10K 4W NULL CONTROL | 2 MFD

FIG. 9 COMBINED SATURABLE CORE MAGNETIC MATRIX AND BINARY COUNTER

The actions of Stages 1, 2, and 3 of the counter and their associated control circuits are to change the binary number in the counting stages at every eighth control-reference count, to select the elements in sequence, and to sense and represent as output voltages the conditions of the counting stages. A typical "1" signal, as observed at the matrix output, is shown in Fig. 10.

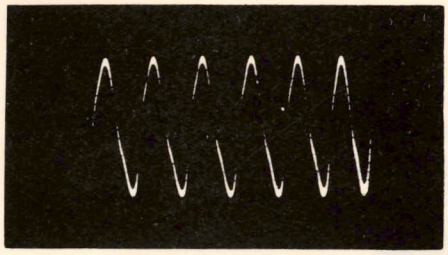
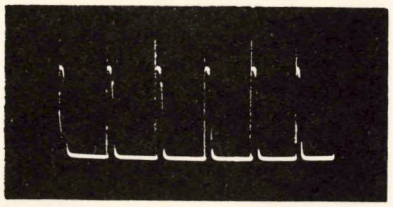


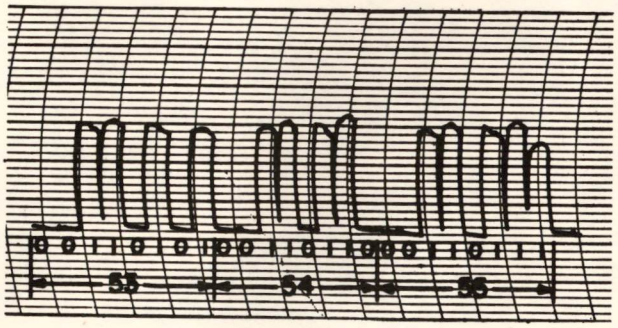
Fig. 10 - A Typical "1" Output Signal (400 cps) from the Magnetic Matrix

C. The Output Circuits

The purpose of the output circuits is to rectify and clip the matrix a-c output signals in order to form pulses of uniform amplitudes which are sent to two neon camera indicating lamps and to the recording oscillograph. Some leakage exists under the saturated conditions. The leakage voltages are not always the same magnitude and, together with nonuniform "1" or on-signals, cause nonuniform switching ratios. To obtain uniform effective "1" voltages and to improve the switching ratio, a high-gain triode amplifier and a clipper for rectification are used. The first stage of the output is a 12AX7 amplifier. The second stage, a 12AX7 cathode follower, is a low impedance source which drives the two 12AT7 output amplifier clippers. These amplifier clippers are biased below cut-off by an amount equal to the largest leakage-voltage peaks and operate only on positive grid-signal peaks corresponding to true "1" signals. The neon indicating lamps operate directly from the voltages developed across the plate-load resistors of the 12AT7 tubes. Before reaching the oscillograph, the 400-cycle carrier is removed from the signal by a low-pass R-C network (R_3 and C_1 of Fig. 9) to facilitate reading the oscillograph record. The neon lamp and the oscillograph signals are shown in Fig. 11. A "1" signal for the neon lamps is a train of pulses of 400-cycle frequency, and a "0" signal has zero magnitude. A "1" signal for the oscillograph is a filtered train of 400-cycle pulses, and a "0" signal has zero magnitude.



11a. A TYPICAL "1" SIGNAL (400 CPS) FROM OUTPUT STAGE WHILE FIRING NEON LAMP.



11b. AN OUTPUT SIGNAL CONSISTING OF THREE CONSECUTIVE EIGHT DIGIT BINARY NUMBERS APPLIED TO A RECORDING OSCILLOGRAPH

Fig 11 - The Final Output Signals
to the Neon Lamps and Recording Oscillograph

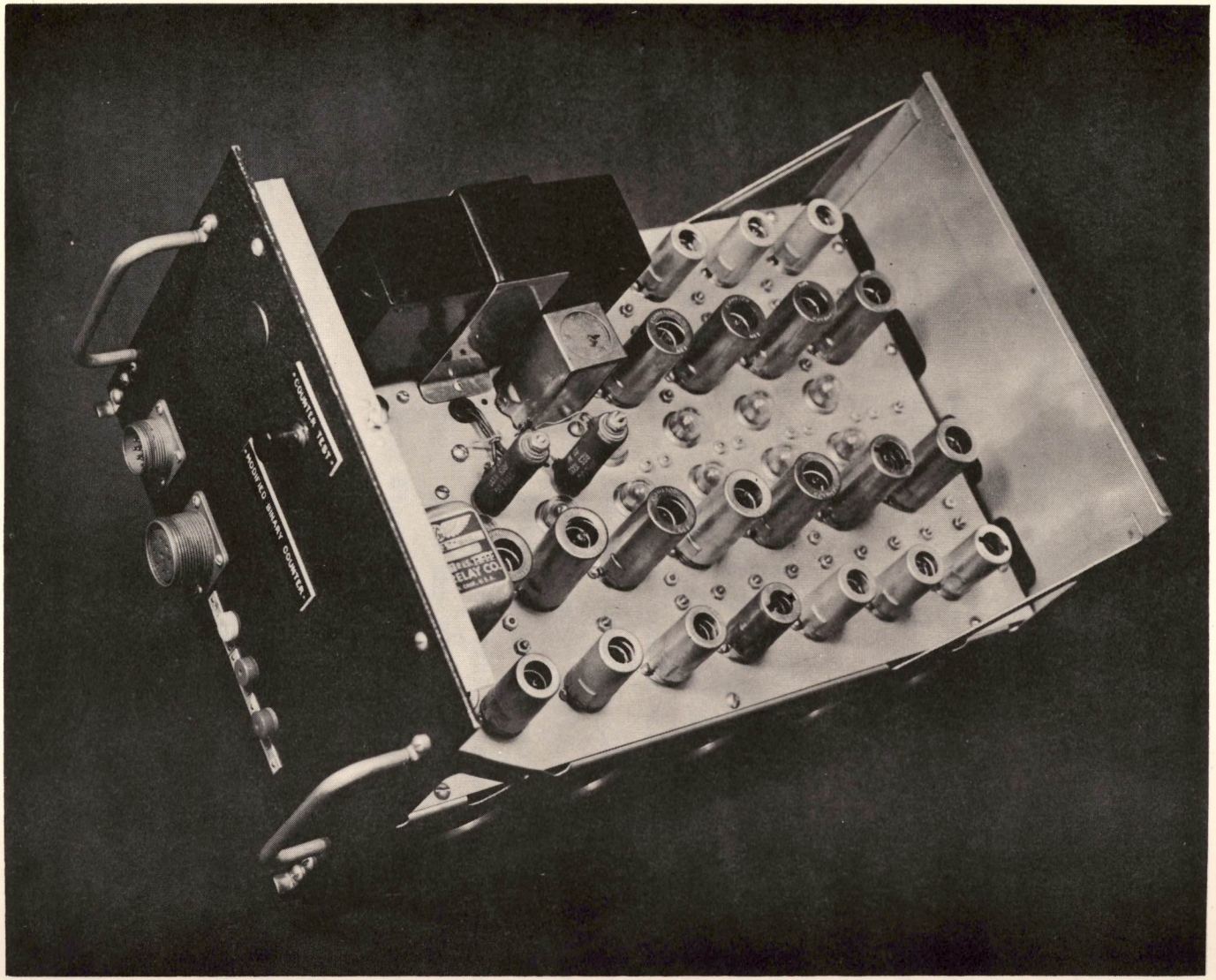


Fig. 12 - Binary-Counter Chassis with Magnetic-Matrix Switch Installed

V. APPENDIX

Adjustments for Operating Binary Counter and Magnetic-Matrix Switch

Excitation

1. Apply filtered 115 volts 400 cps to pin "C" of Cable No. 22. (Unit was tested with 400 cps supplied by a Varo Type 411 inverter.)

2. Measure the excitation voltage on the binary-counter power supply.

3. Adjust the Excitation Control potentiometer (on power-supply chassis) for 60 volts at Test Point 1. Do not allow voltage at Test Point 1 to exceed 75 volts.

Null Control

1. Observe with an oscilloscope the signal between Test Point 2 or Test Point 3 (both located on panel of binary counter) and ground.

2. Using the Counter Test button on the binary-counter panel, advance the counter through a series of counts and observe nulls. If nulls appear on oscilloscope, adjust the null control (located under binary-counter chassis) CCW until no nulls appear. [Note that: (1) the stage being sampled may be determined from the lamps associated with the 2^0, 2^1, and 2^2 stages of the counter; (2) as the count advances, the stages are sampled in a descending order. When the 2^0, 2^1, and 2^2 stages are all zero, the last stage, Counting Stage 8, of the counter is being sampled.]

Coding Lamps

The recommended neon-lamp types for coding are NE-16 and/or NE-2. As indicated in Fig. 9, one output circuit is wired for an NE-16 and the other circuit is wired for an NE-2. If different lamps are to be used in these circuits, the series limiting resistors (5.1 K for the NE-16 and 51 K for the NE-2) must be changed to obtain proper lamp operation.

Tests of counter and coding lamp operation may be made by connecting the proper lamps between the +300 Test Point and Test Points 2 and 3.

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MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LINCOLN LABORATORY

MAXIMUM EFFICIENCY TRANSISTOR SWITCHING CIRCUITS

R. H. BAKER

22 MARCH 1956

TECHNICAL REPORT NO. 110

UNCLASSIFIED

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

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MAXIMUM EFFICIENCY TRANSISTOR SWITCHING CIRCUITS

R.H. Baker

Group 24

Technical Report No. 110

22 March 1956

ABSTRACT

The important transistor properties relating to switching-circuit design are discussed. Circuit configurations are presented which utilize the advantage of circuit symmetry possible through the combined use of p-n-p and n-p-n transistors.

LEXINGTON MASSACHUSETTS

MAXIMUM EFFICIENCY TRANSISTOR SWITCHING CIRCUITS

I. INTRODUCTION

Failure to appreciate, understand and define the important transistor parameters has retarded the application of transistors to switching circuits and systems.

Human nature demands that one attack new problems in the light of past experience. This leads to the obvious approach of transistorizing vacuum-tube circuitry; this approach is helpful because by utilizing it one gains valuable data and experience in switching networks. On the other hand, the approach tends to hinder the exploration of some of the inherent advantages of transistors.

There is the tendency to consider every new device as a cure for all past difficulties. True, the transistor overcomes many of the deficiencies of the vacuum tube, but it also creates many new limitations. One must understand these and guard against them. In one respect the transistor is completely equivalent to the vacuum tube. That is, they both obey the good, logical, fundamental network-design principles that have held in the past.

This report attempts to point out in a general way some of the important electrical characteristics of transistors as they apply to switching networks.

II. TRANSISTOR SWITCHING-CIRCUIT PROPERTIES

A. GENERAL PROPERTIES OF TRANSISTORS AS ACTIVE ELEMENTS

The large signal equivalent circuit[1] of the n-p-n and p-n-p transistors and the grounded-base collector characteristics are shown in Fig. 1.

As may be seen from the grounded-base collector characteristics, the junction transistor may be operated in three different modes. They are: (1) cutoff (point A), (2) active (point B) and (3) saturated (point C).

In the cutoff mode the transistor current gain [Eq. (1) of Fig. 1] is equal to zero and the collector current is equal to the normal leakage current of a p-n diode [Eq. (10)].

$$I_{co} = I_s \left\{ \exp [qv/KT] - 1 \right\} \quad , \tag{10}$$

where I_s is the saturation current, q is the electronic charge, k is Boltzmann's constant and T is the temperature in degrees Kelvin. In the active region the currents are related as shown in Fig. 1.

In the saturated region the diode R_c may be thought of as effectively shorting the current generator $\alpha_N I_e$, and hence, for purposes of increasing the collector current beyond that necessary to saturate the transistor, the current gain is approximately equal to zero.

B. GENERAL SWITCHING-CIRCUIT PROPERTIES

One of the salient features of the digital approach to systems is that they may be analyzed or synthesized by repetitive use of relatively few, rather simple basic-circuit types.

It is imperative that one understands thoroughly the basic-circuit designs and its limitations. Fortunately, due to the fundamental nature of switching circuits, they are rather easily analyzed.

A typical switching network may be analyzed piecewise by dividing the output (timewise) into a discrete set of times utilizing appropriate equivalent circuits to describe circuit performance during each of the times. For example, consider the waveforms of a bistable Eccles-Jordan circuit as represented in Fig. 2. The voltage outputs (a and b), and hence the operation of the network, may be described for the rest times TR1 and TR2 in terms of appropriate equivalent circuits devoid of energy storage components. The transient conditions (TS1 and TS2) may be represented by equivalent circuits which usually involve energy storage components. However, the switching conditions may be analyzed in terms of initial conditions at the beginning of the switching time (obtained from the equivalent circuit at rest conditions) and final conditions at the end of the switching time (beginning of the succeeding rest time). This piecewise approach may be extended (by repetition) to analyze multistable circuits (or conditions) which may be impressed on the circuits by system considerations (variable loads, etc.).

III. BIAS LEVEL CONSIDERATIONS

The piecewise approach to switching-circuit analysis described in Sec. II is, of course, not new. Indeed, this approach has been used in vacuum-tube switching-circuit design for many years. However, at the present time it is felt that the approach is not fully appreciated nor utilized in transistor circuit design. There are two major reasons why transistors are particularly adaptable to the piecewise analysis approach. They are:

(1) The transistor is a very sharp cutoff device. An approximate 0.1-volt emitter-to-base reverse bias renders the unit completely cut off, and 0.1-volt forward bias renders the unit fully turned on.

(2) The transistor current gain is essentially constant over a large current range.

Property (1) allows the circuit designer to design large safety factors (margins) into circuitry conveniently; property (2) allows, with good approximation, the transistor voltage-current relationships to be expressed algebraically. The above-mentioned two points may be demonstrated by considering a general resistive loaded stage as shown in Figs. 3 and 4.

The quantities I_e and I_c may be expressed in terms of the junction leakage current, external resistors and bias supplies as shown in Eqs. (11) and (12).

$$I_e = f_1(I_{co}) + f_2(V_{ee}) + f_3(V_{bb}) \tag{11}$$

$$I_c = f'_1(I_{co}) + f'_2(V_{ee}) + f'_3(V_{bb}) \tag{12}$$

where:

$$f_1 = \frac{R_b}{R_e + R_b(1 - \alpha_N)} \qquad f'_1 = \frac{R_e + R_b}{R_e + R_b(1 - \alpha_N)}$$

$$f_2 = f_3 \frac{1}{R_e + R_b(1 - \alpha_N)} \qquad f'_2 = f'_3 \frac{\alpha}{R_e + R_b(1 - \alpha_N)} \quad .$$

Since in most currently available low power commercial transistors α_N is essentially constant over the emitter current range of 0.2 to 20 ma, and since the output of a transistor may be considered a current source, the output current I_c may be related algebraically to the bias voltages at the emitter, base and collector. However, it is important to note that the dependence of the magnitude of the various currents on transistor current gain is a function of the resistance ratio R_e/R_b as well as the magnitude of α_N.

Since the emitter, base and base collector barriers are p-n junction diodes, the transistor may be cut off with relatively low voltages [Eq.(10)], usually on the order of 0.1 volt by germanium units. The sharp, low voltage-cutoff characteristics ("knee") of a p-n junction not only allow conveniently large circuit margins, but also allow circuit design that is very efficient voltagewise; that is, collector signal swing very nearly equal to the supply voltage magnitude.

IV. TEMPERATURE STABILITY AND POWER DESIGNS

It is generally true that transistor limitations concerning power dissipation arise through the adverse effect on the p-n junctions of high temperature (neglecting conductivity modulation due to high current densities and voltage limitations due to avalanche and punch thru).* The major effect of temperature is to increase the conductivity of the p-n junctions [Eq.(10)]. Since the leakage current is changing so rapidly (exponentially) with junction temperature, the solution to the problem of designing high power circuitry (transistors due to the small size, etc., usually have a rather high thermal resistance) or low power circuitry to withstand evaluated ambient temperatures is usually that of designing circuitry to withstand large changes in leakage currents. This is easily accomplished by considering the effect of leakage currents on operating points for circuits when the transistor cutoff is cut off and when it is conducting. For the cutoff condition the base, emitter and collector potentials may be readily obtained from Eqs. (13) and (14) in Fig. 4, once the relationship for the variations of leakage currents with temperature are known. If the transistor is in the active region (conducting), the transistor terminal potentials depend upon the various currents which, in turn, are functions of temperature and the inherent current gain of the circuit configuration.

It has been shown[2] that the leakage current I_{co}, as a function of temperature, may be expressed as

$$I_{co}(t) = I_o \exp [a(T + HP_c - T_o)] \quad , \tag{15}$$

where I_o is the leakage current at T_o, T_o is the reference temperature, H equals $\Delta T_J/MW$ (junction temperature rise per milliwatt dissipation), T is the ambient temperature and a is a constant ($\approx 0.06 \sim 0.08$ for presently available low power germanium transistors).

In the active region the major contributor to self-dissipation is usually the dissipation of the collector junction except in saturation. In this mode of operation the base resistance

*Considering only the circuitry aspects of high temperature operation, through the effects of temperature on transistor parameter drift (stability), it is assumed that a transistor is chosen which will stand the power dissipation as such.

is the only significant resistance. The behavior of any given network as a function of temperature, therefore, may be predicted accurately by evaluating Eq. (15),* where

$$P_c = V_{cb} I_c \text{ (active region)} \tag{16}$$

and

$$I_c = f_1'(I_{co}) + f_2'(V_{ee}) + f_3'(V_{bb}) \quad . \tag{12 repeat}$$

Equations (12), (15) and (16) may be re-expressed to yield an expression for the rate of change of I_{co} with respect to temperature as

$$\frac{dI_{co}}{dT} = f(I_o, V, K_1 \text{ and } K_2) \quad , \tag{17}$$

where

$$V = \text{voltage biases } (V_{cc}, V_{bb} \text{ and } V_{ee}) \quad ,$$

$$K_1 = \frac{R_e}{R_b} \quad ,$$

$$K_2 = \frac{R_L}{R_e} \quad .$$

By the use of the above result along with Eq. (6) in Fig. 1, a given design may be accomplished so that the network is thermally stable** as well as operationally stable over temperature limits of the order of −80°C to +100°C for germanium transistors.

V. TRANSISTOR RESPONSE TIMES

A. FUNDAMENTAL EFFECTS

The normal† three-region junction transistor is, relative to the vacuum-tube triode, a slow device. The paramount reason for this is that, unlike the vacuum tube where the transient of electrons from cathode to plate is aided by strong electric fields, the transport of carriers (electrons or holes) is by diffusion. As a result, the circuit designer must consider two effects in the response of transistor circuits. They are: (1) normal integrative effects due to shunt capacitances and (2) delay or carrier transient time between emitter and collector. When the transistor is operated in the saturated mode, there exists an additional effect, that of "hole storage" or saturation delay.[3]

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*Care must be taken in evaluating I_o. Equation (15) applies only to the bulk leakage current; i.e., the leakage current due to thermal generation of carriers. The component of leakage current (due to poor surface clean up, etc.) does not change rapidly with temperature.

**The case where the change in I_{co} due to self-dissipation is self-sustaining.

†Excluding the "graded base" (drift) transistor.

As one would expect, the delay times, as well as the more familiar capacitive effects, impose serious circuit design limitations in high speed switching circuitry. Some of the limitations, and the circuit designs partially circumventing the problems, will be discussed subsequently.

B. TRANSISTOR RESPONSE TIMES

There may be as many as three separate response times, depending upon the mode of operation, associated with a single-stage transistor network. They are: (1) rise time, (2) storage or saturation delay and (3) fall time. The three effects are demonstrated in Fig. 5. If R_L, R_e, V_{cc}, and V_T are chosen so that the voltage polarity across the collector junction maintains the collector junction under reverse bias at the peak of the output pulse, the saturation delay vanishes.

The magnitude of the response times (T1, T2 and T3) is different for each of the three basic connections. Also, an accurate analytical expression relating the response times to transistor and circuit parameters is rather complex. However, a set of nine equations (three each for each of the basic connections) has been derived,[3,4] assuming current sources and neglecting the effect of collector capacitance which reveals the salient points that affect switching time for each connection. Some of the results of this work are shown in Fig. 6.

It is interesting to note that empirical results check closely ($\approx \pm 10$ per cent) with the results predicted by theoretical analysis for the switching times T1 and T3, provided the assumptions set down in the analysis are rigorously adhered to. These assumptions are:

(1) $r_c(1 - \alpha_N) \gg R_L$,

(2) $R_L C_c \ll \frac{1}{\omega_N}$,

(3) Current sources at the input.

Care must be taken to assign realistic values for the constants α_N, α_I, ω_N and ω_I, since each of these parameters is a function of voltage and current. It is difficult, in general, to obtain good agreement between theoretical and experimental results for the saturation delay T2, particularly at high current levels.* However, the equations can still be extremely useful to the circuit designer because they point out some of the salient circuit factors affecting the saturation delay time.

To the circuit designer the most stringent condition that limits the usefulness of the analysis is the assumption of current sources. In most practical system designs, this assumption is not valid and hence the circuit designer is forced to combine the results of transient analysis of the input (driving) network with the transient analysis of the transistor, in order to predict the over-all network response.

Perhaps the most significant result of the transient analysis[3,4] is the fact that in all cases (modes of operation) the transistor switching time is dependent upon the constants of the

*One reason for this is that α_N and α_I vary rapidly as functions of current in the saturated mode of operation; hence the assumption that these parameters are constants is inaccurate.

device and the amount of overdrive supplied at the input, or

$$T_s = K_d \ln \frac{\text{input current difference}}{\text{output current difference}} \quad . \tag{18}$$

The result of Eq. (18) indicates that the single, most important factor affecting the switching time is the frequency response of the device itself. Also, it has been shown[5] that minimum response time occurs when $\alpha_N = 1$. Since minimum time occurs when $\alpha_N = 1$ and the frequency response ω_N of the transistor is important, it is only natural for the circuit designer to call for high frequency devices. There is promise of obtaining the devices through graded base structures, etc. However, the interim solution of transistor manufacturers has been to build transistors with very narrow base widths and hence increase the value of ω_N. This approach is fruitful to a degree but it can be shown[6] that there exists an optimum base width that yields minimum switching time for practical switching circuits.

Further, the optimum base width is, in general, different for each of the three basic connections (i.e., grounded base, emitter and collector).

VI. ACTUAL CIRCUIT DESIGN CONFIGURATIONS AND THEIR LIMITATIONS

A. CIRCUIT AND SYSTEM CONSIDERATIONS

1. Reliability

Much has been said, but little actually proved, about the reliability of systems constructed from transistor switching circuits. From a fundamental point of view the transistor should be an extremely reliable device in that there is no theoretical reason why it should fail (i.e., nothing is used up by operation such as the cathode material of a vacuum tube). However, numerous circuits have been designed in which the transistor exhibits a half life on the order of 0.5 sec (usually associated with the thermal time constant of a transistor which is on the order of 1 sec). On the other hand, life test data on certain other circuitry utilizing the same transistor types from the same production run indicate that the transistor life is essentially infinite. On the basis of the above-described phenomena and other life test data, one can make the following general observations about transistor reliability:

(a) At the present state of the production art, the transistor exhibits a rather large spread in parameter values.

(b) The nonuniformity of a given type at the present time is inherent due to lack of adequate production control.

(c) Good production control may ultimately be attained through improved applied technology, but only after further knowledge and understanding of a fundamental nature are obtained concerning the intrinsic and extrinsic variables affecting the properties of semiconductor devices.

(d) At the present time most manufactures use selective segregation to meet uniformity requirements as is done in diode manufacturing.

(e) Transistors (all manufactures) may exhibit drift in parameters on the order of 2 to 1 in magnitude and the major portion of the drift takes place in the first few thousand hours (at room temperature).

(f) The rate and magnitude of parameter drift is, in general, proportional to temperature in an experimental manner (positive experimental).

(g) Aside from the long-term drift of transistor parameters with temperature and age, the junction cutoff current I_{eo} and I_{co} are directly affected by temperature (see Sec. IV).

(h) In order to achieve long-term stable operation of transistor circuits one must, in view of the long-term parameter drift with age and short-term drift with respect to ambient temperature changes, design circuitry with large safety margins.

(i) Reliable operation can be achieved at the time by designing switching circuits with the principles set forth in Secs. II through V of this report.

B. POWER AND SPEED

The transistor system affords great power savings over the equivalent systems built with vacuum tubes. There are two principal reasons for this:

(1) The lack of filament power,

(2) The natural voltage and current levels are lower.

These two effects account for a saving in power on the order of 20 or 30 to one over vacuum tube systems. In general, however, the same fundamental principles involving power and speed of systems are the same as for vacuum tube systems; i.e., rapid responses involve charging capacities in short periods of time, and hence the power consumptions of system naturally increase. This is particularly true due to the fact that presently available transistors are inherently slow (diffusion process), and hence considerable overdrive must be applied to speed up circuitry.

Unlike vacuum tube systems where the primary considerations involve response-time capacitive effects and not transient times of the electrons from cathode to plate, in transistor circuits the transit time of carrier across the base region plays an important role in circuit design.

The effect usually manifests itself by imposing an absolute minimum input pulsewidth which, in turn, sets rather large minimum capacitance values in a given circuit. The large capacitance values, in turn, impose recovery time problems that may be more serious than actual rise time considerations.

C. SIGNAL LEVELS

Because transistors are extremely efficient voltagewise (on the order of 0.1-volt "knees"; see Sec. III), the system voltage levels are usually set by a combination of system and transistor considerations. Among these are:

(1) Low voltage limit

The low voltage limit is automatically set if the transistors are allowed to saturate. Whether or not one allows the transistor to saturate is primarily determined by speed considerations (see Sec. V).

(2) High voltage limit

The primary considerations as to the upper voltage limit are the total power

consumption of the system and the upper voltage limit imposed on the transistor by the punch-thru[7] and avalanche phenomena.[8]

(3) System voltage swing (on-off voltage level difference)

The signal level of an all-transistor system is usually chosen as a compromise between two inherent opposing effects. They are:

(a) As the signal level increases (total swing), the amount of energy dissipated in charging and discharging capacities increases. This effect indicates that the signal level should be low.

(b) On the other hand, the signal level should be, for convenience of circuit design, large compared with the transistor (off-on) uncertainty region (corresponding roughly to the grid base in the vacuum tube systems), which is on the order of 0.2 volt for germanium transistors and 1 volt for silicon transistors.

For an all-transistor-diode system, the signal level should be large compared with the forward drop of several diodes or transistors in series* (for design convenience of diode or transistor gating circuitry).

D. ENERGY CONVERSION EFFICIENCY

Fundamentally the transistor, like the vacuum tube, has gain by virtue of dissipation changes. Unlike the vacuum tube, the input impedance is much lower than the output impedance. In the design of realistic transistor systems then, a serious problem arises in the available power to drive succeeding stages. This situation is aggravated still further in the design of high speed systems, since it is necessary in the transient state to overdrive the stages to obtain fast switching. This fact, more than any other, accounts for the large number of transistors required to build transistor systems compared with equivalent vacuum tube systems.

The above considerations indicate that circuitry should be designed to deliver maximum output power and that a high percentage of the available output power should be available to drive other transistors. Further, since currently available high frequency transistors are extremely low power devices (on the order of 0.5 Mc-watts as a figure of merit**), it is suggested that circuitry should be designed with energy conversion efficiency that is as high as possible. For example,

$$\frac{\text{useful signal output power}}{\text{transistor dissipation}} = n_1 \quad , \tag{19}$$

where

$$n_1 \to \infty \text{ for optimum design} \quad .$$

Also in the interest of designing a minimum-power drain system, a criterion (or figure of merit) for optimum circuit design is

$$\frac{\text{useful signal output power}}{\text{power supply drain}} = n_2 \quad , \tag{20}$$

*The high forward conductance of the punch-thru diode invented by R.H. Rediker (Group 35) should improve this situation.

**SBT-100, 50 Mcps, 10 mw.

where

$$n_2 \rightarrow 1 \text{ for optimum design} \quad .$$

The product of n_1 and n_2 should be made as large as possible. The ratio represented by n_1 can be made large by allowing the transistor to saturate or by controlling the voltage from collector to base through the use of clamping diodes. However, minimum power systems can be built only by making n_2 close to unity (this must be true if there exists a minimum power level to process intelligence). In most present transistor circuit designs, a high percentage of useful output power from the transistor is dissipated in the load resistors. This is especially true for direct-coupled logic. Therefore, the value of n_2 may be increased significantly by removing the standby power dissipated in this area.

The circuit design techniques in the following section show how the values of n_1 and n_2 may be increased yielding minimum power, maximum speed and minimum sensitivity to component and transistor drift circuits.

VII. MAXIMUM EFFICIENCY CIRCUITS

It turns out that, aside from eliminating the power dissipated in load resistors, an additional gain in system power efficiency may be obtained by utilizing circuitry designs that draw power from the supplies according to the power demand at the output. This process always involves feedback. An example of circuitry to accomplish this is exemplified by the cathode-follower or emitter-follower (grounded-collector) circuit. Unfortunately, however, these two circuits do not have voltage gain associated with them. A transistor circuit involving voltage gain, along with an ability to convert DC power into signal power as required by the load, is shown in Fig. 7.

The salient results of Eqs. 21 through 28 (in Fig. 7) are:

(a) The transistor dissipation is low and the output power is high for collector currents less than the maximum output current.

(b) The major portion of the power drawn from the supplies is available at the output for dissipation in the load resistor; i.e., $n_2 \approx 1$ and the circuit draws from the supplies only the power dissipated in R_L and R_b (neglecting transistor dissipation).

(c) The only transistor parameter of importance in the conducting state is the minimum base-to-collector current gain β_N.

To illustrate the above-mentioned points assume that the circuits, constants and the transistor parameters are:

$$\begin{aligned} \beta_N &= 20 (\alpha_N = 0.95) & V_{in} &= 5 \text{ volts} \\ r_{b\,sat} &= 50 \text{ ohms} & R_b &= 10 \text{ kilo-ohms} \\ V_{cc} &= 10 \text{ volts} & R_L &= 1 \text{ kilo-ohm} \end{aligned} \quad . \qquad (29)$$

Then

$$I_b \approx 0.5 \text{ ma}$$

$$I_{c\ max} = 10 \text{ ma} \quad , \tag{30}$$

$$I_e = I_b + I_c = 10.5 \text{ ma}$$

or

$$n_1 \approx \frac{50 \text{ mw}}{(0.2)\ (10.5)} = \frac{50 \text{ mw}}{2.1} \approx 24 \tag{31}$$

and

$$n_2 = \frac{50 \text{ mw}}{50 \text{ mw} + 2.5 \text{ mw}} \approx 0.95 \quad . \tag{32}$$

Two of the above circuits (Fig. 7) may be coupled together, with only slight modification, to form a bistable circuit as shown in Fig. 8. The difficulty with this configuration is that:

(a) The low voltage level is not fixed (depends upon I_{co}, etc.),

(b) The power dissipated in the internal load resistor R_L (in shunt with actual load) may be an appreciable percentage, particularly at low output power levels.

(c) For fast fall time (when the transistor is turned off), R_L must be made small.

A circuit configuration that circumvents these disadvantages is shown in Fig. 9. The salient features of the configuration are:

(a) Essentially all of the output current (collector current) is available to drive the load R_L.

(b) The standby power is low; i.e., when there is no load, the power taken from the supplies is approximately equal to the dissipation in the base resistors

$$PD_{SB} \approx 2 I_b^2 R_b \quad \text{(standby output power)} \quad . \tag{33}$$

(c) Both the high and low voltages are clamped (the p-n-p and n-p-n transistors saturate).

(d) The tolerance on all resistors may be large (on the order of ±50 per cent).

(e) Circuit operation is substantially independent of transistor parameters.

(f) The stability of the configuration is insensitive to supply voltages.

(g) The configuration leads to fast rise and fall time since large transistor overdrive is inherent.

Items (d), (e), and (f) are true since the configuration allows the transistors to set their own levels.

A complete circuit diagram based on the configuration of Fig. 9 is shown in Fig. 10. Data showing some of the operating characteristics of the circuit are shown in Figs. 11 and 12.

One difficulty with the circuit shown in Fig. 10 is that there is an appreciable delay "around the loop" because the conducting transistors are saturated. This difficulty may be

minimized by double triggering (triggering all four transistors simultaneously). A circuit employing this feature is shown in Fig. 13. Figures 14 and 15 give additional data about the operation of the circuit. Figures 16, 17 and 18 show the results of the current-demand flip-flop using 5-Mcps transistors.

The circuitry techniques described in Figs. 7 through 18 may be extended to nonsaturating circuitry. The primary gain in designing the circuits to operating in the nonsaturating mode is in the maximum operating speed.

The circuit configurations to accomplish this are shown in Fig. 19.

The action of the circuit may be explained in terms of the conducting p-n-p transistor shown in Fig. 20. It may be seen from Fig. 20 that the nonsaturating current-demand configuration of Fig. 19 meets all the conditions set down (a through f) for the saturated configuration of Fig. 9.

The major advantage of the nonsaturated over the saturated configuration is through decreased switching time. Figure 21 shows a typical design using the nonsaturated configuration employing single side triggering. Figure 22 shows a higher speed version using double triggering. Figure 23 shows the triggering conditions for the circuit.

The reason that the back-clamped configuration of Figs. 19 and 20 does not allow the transistors to be saturated may be seen by comparing the diode characteristics shown in Fig. 24.

If silicon transistors are used, the nonsaturated circuitry does not require the four silicon diodes. This may be seen from the silicon collector finally shown in Fig. 25. The required basic configuration using silicon transistors is shown in Fig. 26.

The salient electrical features afforded by back-clamping, current-demand technique (CD) are:

(a) Saturated (SCDFF)

(1) Low transistor dissipation,

(2) High conversion efficiency (output power/supply drain),

(3) Insensitivity to component and transistor parameters (standby load resistors not needed),

(4) Insensitivity to voltage supply drift,

(5) Maximum system efficiency (draws power from supplies according to needs of load),

(6) Fast rise and fall time (inherent overdrive),

(7) Loop delay (caused by saturation time).

(b) Nonsaturated (NCDFF)

(1) Low transistor dissipation,

(2) High conversion efficiency (output power/supply drain),

(3) Insensitivity to component and transistor parameters (standby load resistors not needed),

(4) Insensitivity to voltage supply drift,

(5) Maximum system efficiency (draws power from supplies according to needs of load),

(6) Fast rise and fall time (inherent overdrive),

(7) No saturation delay.

VIII. GATING CIRCUITRY

The design of maximum reliability switching systems depends very heavily upon the reliability of the voltage-pulse voltage-level gate. In order to assure maximum system reliability (assure positive action and suppress superfluous triggering), the gate circuits should fulfill the following general system qualifications. They are:

(a) Independent of pulsewidth,
(b) Independent of pulse amplitude,
(c) Independent of pulse repetition frequency,
(d) Independent of pulse level (within given limits),
(e) Fast response both to pulse and to level change.

The circuit design should also fulfill the following electrical qualifications:

(a) Insensitivity to component values,
(b) Insensitivity to transistor parameters,
(c) Minimum standby power,
(d) High available output power,
(e) Present constant load to pulse source (driver),
(f) Deliver a standardized output pulse that is insensitive to input pulse and level amplitudes.

A circuit configuration that fulfills to a high degree the above characteristics is shown in Fig. 27. The gating waveforms are shown in Fig. 28. A study of Figs. 27 and 28 shows that the circuit configuration fulfills to a high degree all of the qualifications imposed on system and circuit considerations for reliable gating circuitry.

IX. CONCLUSIONS

The reliability of transistor switching systems is closely related to the design of the circuits. The circuit designer must consider the drift of operating points caused by aging and ambient self-generated temperature changes. For high speed networks, due to the lack of high speed transistors, overdrive must be used to speed up the circuit response.

Due to the sharp cutoff characteristics of transistors, circuits with large margins may be conveniently designed.

Transistors are inherently efficient devices (both voltagewise and powerwise). This, along with the fact that two types of transistors are available (n-p-n's and p-n-p's), allows circuit design that is extremely efficient in terms of power supply drain to signal power output.

The transistor being an efficient, reliable, small device may be soldered into systems much as are ordinary resistors and capacitors. This, plus the fact that it is basically a three-terminal passive device which can produce power gain, makes its use in networks where feedback techniques are more widely employed appear very attractive.

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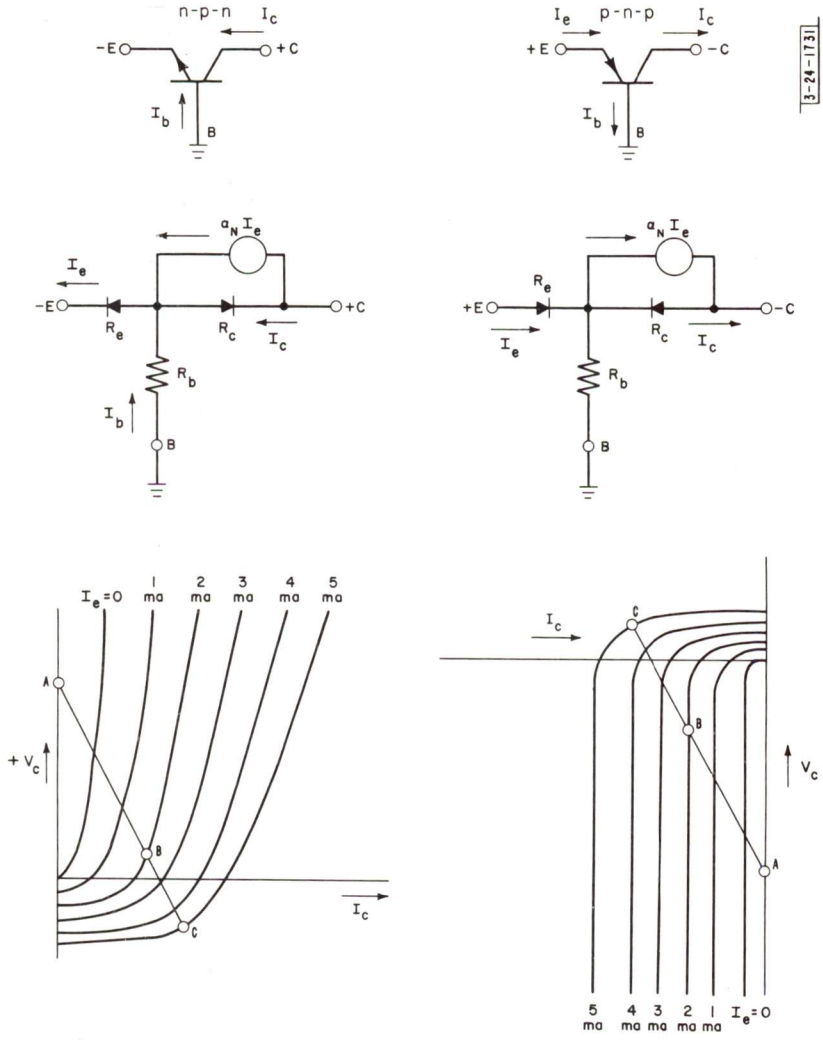


$$(1)\quad \alpha_N = \frac{\Delta I_c}{\Delta I_e}\,\Big|\, V_c = K$$

$$(2)\quad \beta_N = \frac{\Delta I_c}{\Delta I_b}\,\Big|\, V_c = K$$

$$(3)\quad I_c = \alpha_N I_e$$

$$(4)\quad I_b = I_e - I_c$$

$$(5)\quad I_b = I_e(1 - \alpha_N)$$

$$(6)\quad I_c = \left(\frac{\alpha_N}{1 - \alpha_N}\right) I_b$$

$$(7)\quad I_c = \beta_N I_b$$

$$(8)\quad R_{in} = R_e + R_b(1 - \alpha_N)$$

$$(9)\quad R_{out} = R_c$$

Where:

α_N = Normal emitter-to-collector current gain.

Fig. 1. Equivalent circuits and collector characteristics of p-n-p and n-p-n transistors.

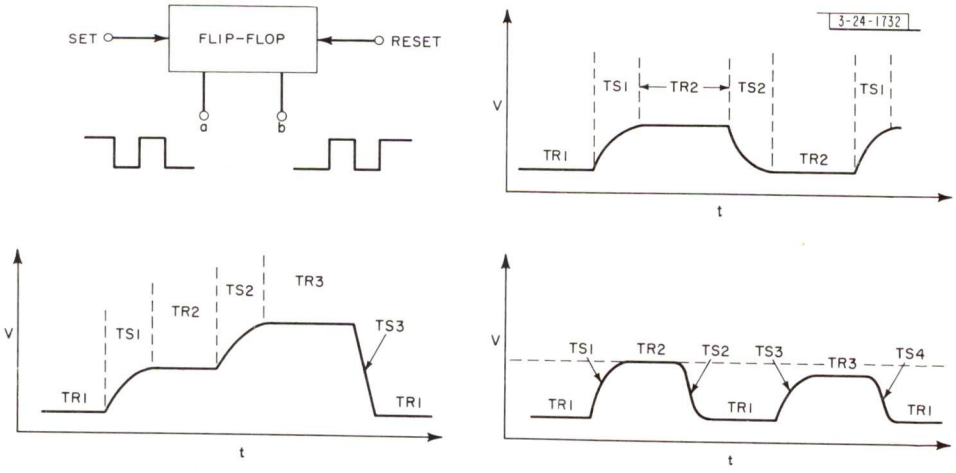


Fig. 2. Switching-circuit characteristics.

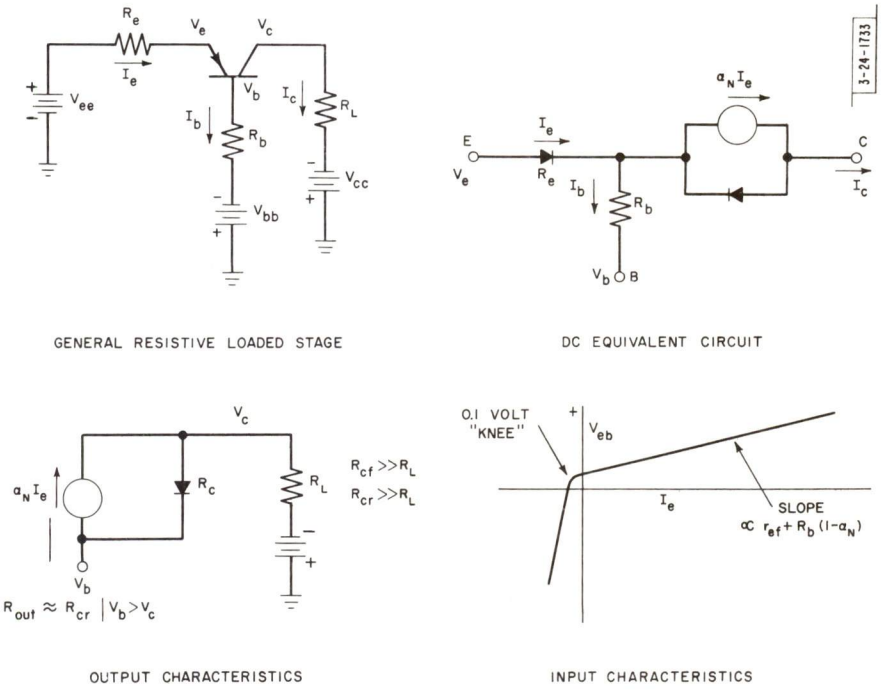
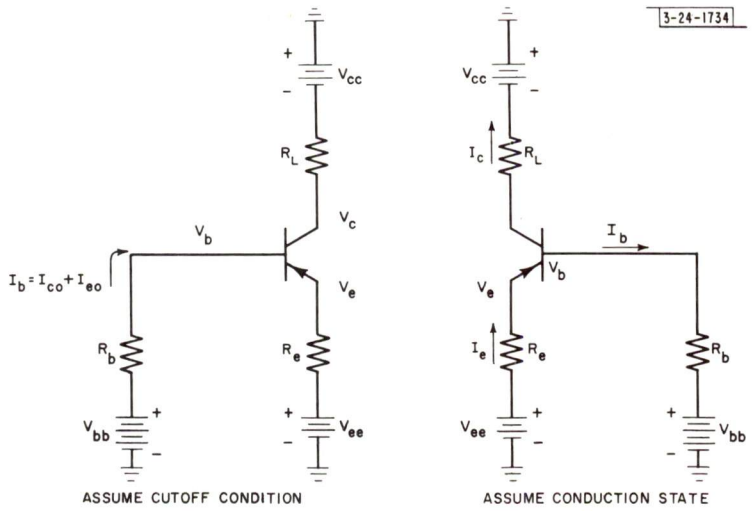


Fig. 3. Voltage and current characteristics of the p-n-p transistor.



(a) $R_e, R_L \ll R_{er}, R_{cr}$ $\quad V_{ee} > V_{bb}$ $\quad R_{cr} \gg R_L$

(b) $V_{ee} < V_{bb}$ (cutoff) $\quad R_{ef} \ll R_e$ $\quad I_b = I_e(1 - \alpha_N)$

$$I_e = f_1(I_{co}) + f_2(V_{ee}) + f_3(V_{bb})$$

Then:

(13) $V_b = V_{bb} - I_b R_b$

(14) $I_b = I_{co} + I_{eo}$

$$f_1 = \frac{R_b}{R_e + R_b(1 - \alpha_N)}$$

$$f_2 = f_3 \frac{1}{R_e + R_b(1 - \alpha_N)}$$

$$I_c = \alpha_N I_e$$

Fig. 4. General resistive loaded stage.

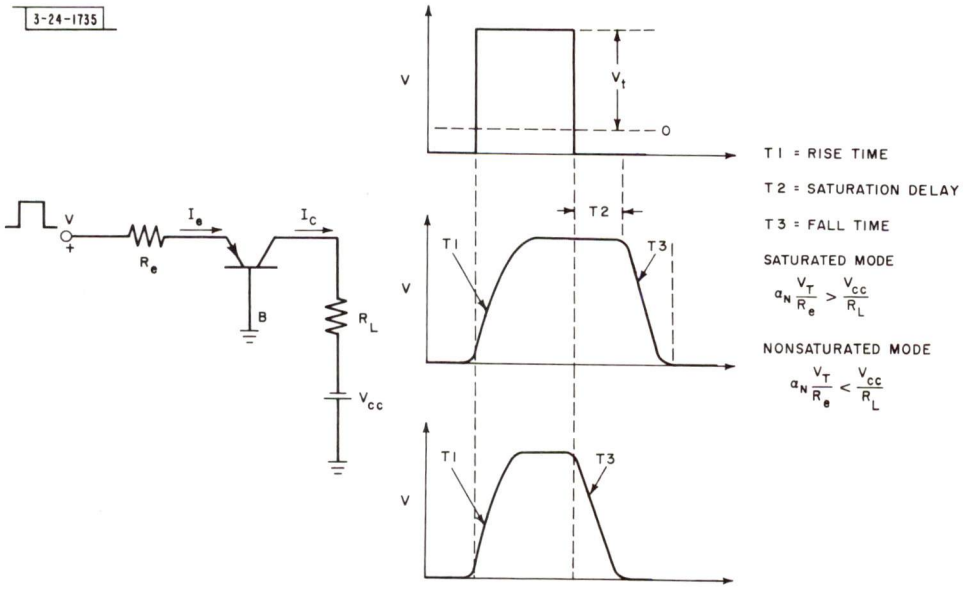
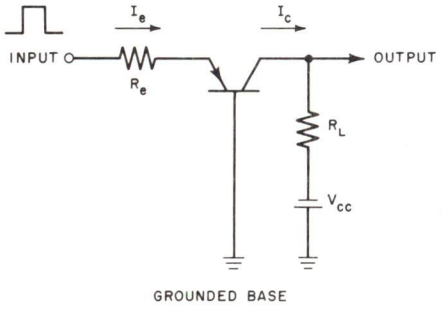
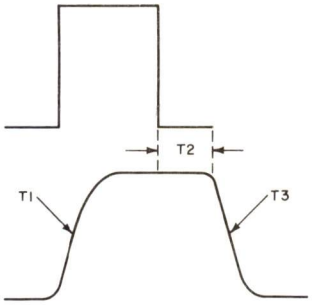


Fig. 5. Response time.



GROUNDED BASE



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$\omega_N = 2\pi f_\alpha$

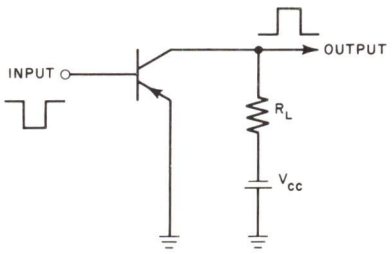
f_α = Frequency at which α is equal to 0.707 of low frequency value

$$T1 = \frac{1}{\omega_N} \ln \frac{I_e}{I_e - I_c/\alpha_N} \quad : \quad T2 = \frac{\omega_N + \omega_I}{\omega_N \omega_c (1 - \alpha_N \alpha_I)} \ln \frac{I_{e2} - I_{e1}}{I_{e2} - I_{c1}/\alpha_N} \quad : \quad T3 = \frac{1}{\omega_N} \ln \frac{I_{c1} + I_{e2}\alpha_N}{I_{c2} + \alpha_N I_{e2}} \quad .$$

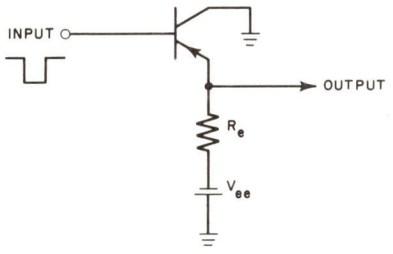
ω_N = Normal parameter
ω_c = Inverted parameter
α_N = Inverted parameter
α_c = Inverted parameter

Inverted parameter – emitter and collector transposed

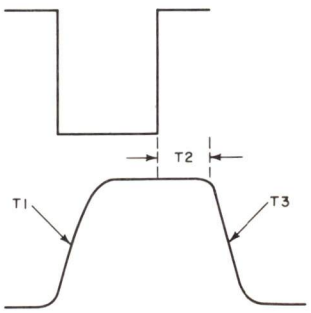
Subscript 1 refers to initial condition
Subscript 2 refers to final condition

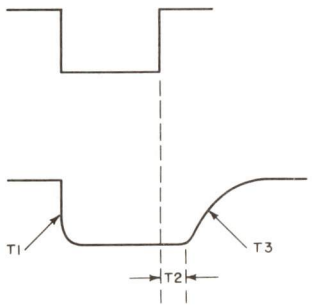


GROUNDED EMITTER



GROUNDED COLLECTOR





$$T1 = \frac{1}{\omega_N(1 - \alpha_N)} \ln \frac{I_b}{I_b - I_c/\beta_N}$$

$$T2 = \frac{\omega_N + \omega_I}{\omega_N \omega_I (1 - \alpha_N \alpha_I)} \ln \frac{I_{b1} - I_{b2}}{I_{c1}/\beta_N - I_{b2}}$$

$$T3 = \frac{1}{\omega_N(1 - \alpha_N)} \ln \frac{I_{c1} - I_{b2}\beta_N}{I_{c2} - I_{b2}\beta_N}$$

$$T1 = \frac{1}{\omega_N(1 - \alpha_N)} \ln \frac{\alpha_N I_b}{I_b - I_e(1 - \alpha_N)}$$

$$T2 = \frac{\omega_N + \omega_I}{\omega_N \omega_I (1 - \alpha_N \alpha_I)} \ln \frac{I_{b1} - I_{b2}}{I_{e1}(1 - \alpha_N) - I_{b2}}$$

$$T3 = \frac{1}{\omega_N(1 - \alpha_N)} \ln \frac{I_{e1} - I_{b2}/1 - \alpha_N}{I_{e2} - I_{b2}/1 - \alpha_N}$$

General equation: $T_s = K_d$ ln (input current difference/output current difference).

Fig. 6. Results of transient analysis.

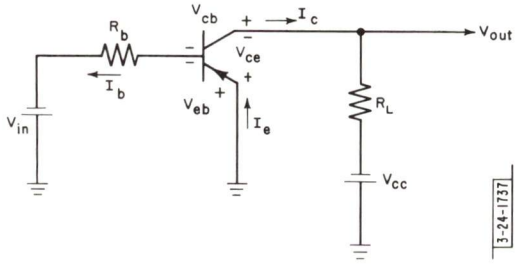


Fig. 7. Back-clamping technique.

(21) $I_b \approx \frac{V_{in}}{R_b}$ (22) $I_{c\,max} = \beta_N I_b$ (23) $I_c = \frac{V_{cc}}{R_L}$

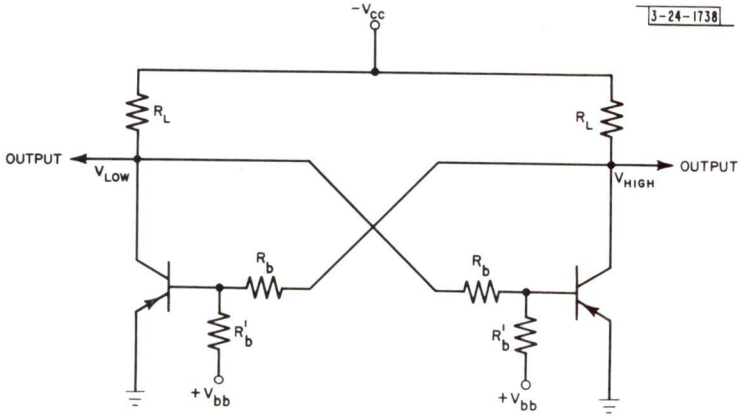
(24) signal output power = $I_c^2 R_L$

(25) input power = $I_b^2 R_b$

(26) $n_1 \approx \frac{I_c^2 R_L}{I_b^2 R_b + V_{eb} I_e}$

(27) $n_2 = \frac{\frac{V_{cc}^2}{R_L}}{\frac{V_{cc}^2}{R_L} + \frac{V_{in}^2}{R_b} + PD_{transistor}}$

(28) $G_v = \beta_N \left(\frac{R_L}{R_b}\right)$ (voltage gain before transistor limits)



typical values

$V_{cc} = -10\,V$

$V_{bb} = +\ 1\,V$

$R_b = 10\,K$

$R_L = 10\,K$

$R'_b = 5\,K$

Fig. 8. Bistable saturated circuit.

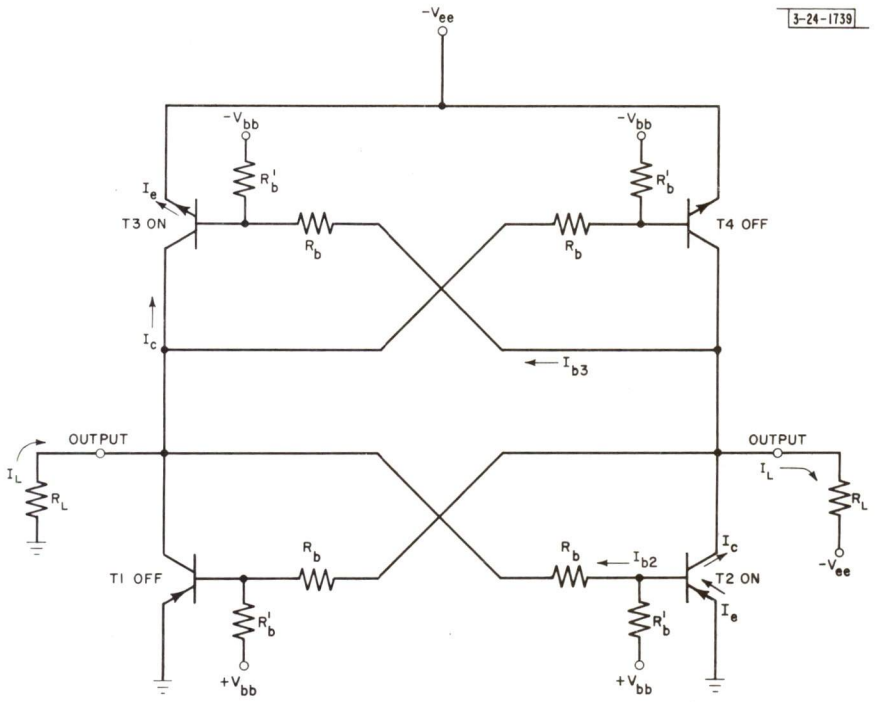


Fig. 9. Saturated current-demand configuration.

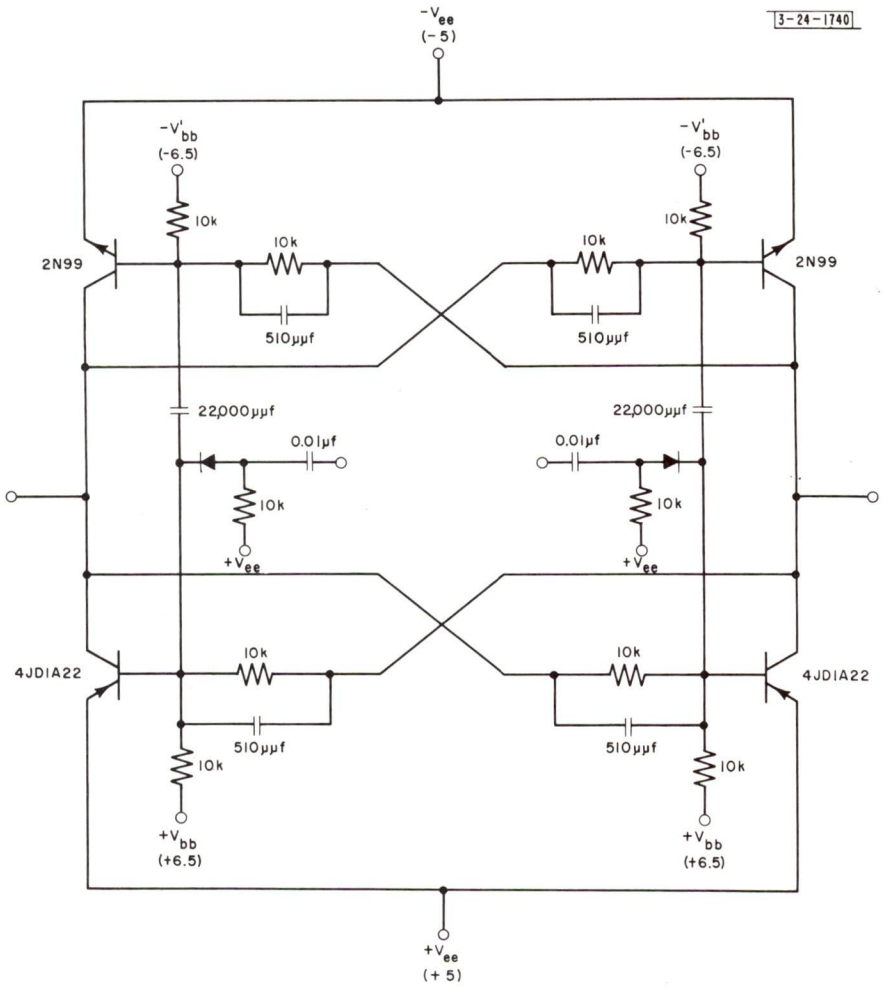


Fig. 10. Circuit diagram of saturated current-demand configuration single-triggering (SCDFFS) 1-Mcps transistors.

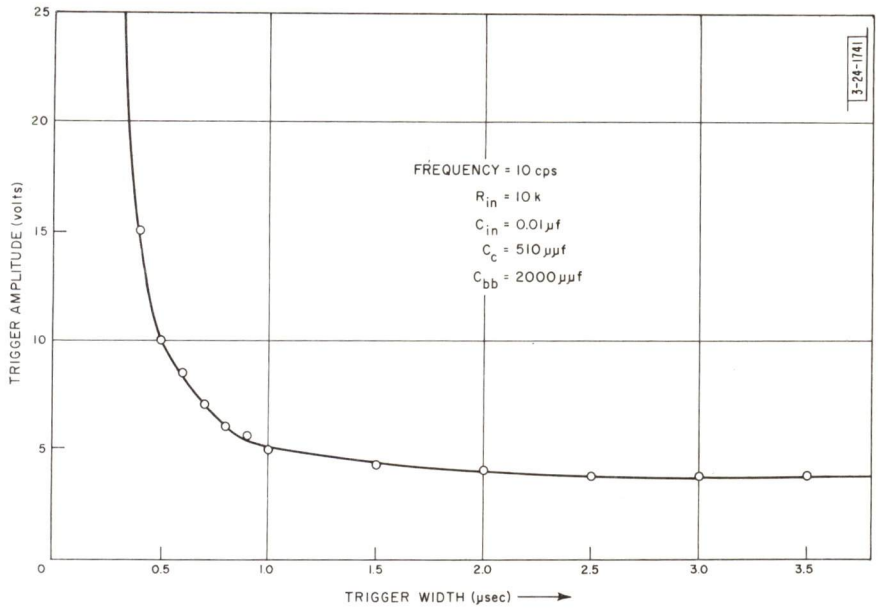


Fig. 11. Trigger voltage vs pulsewidth.

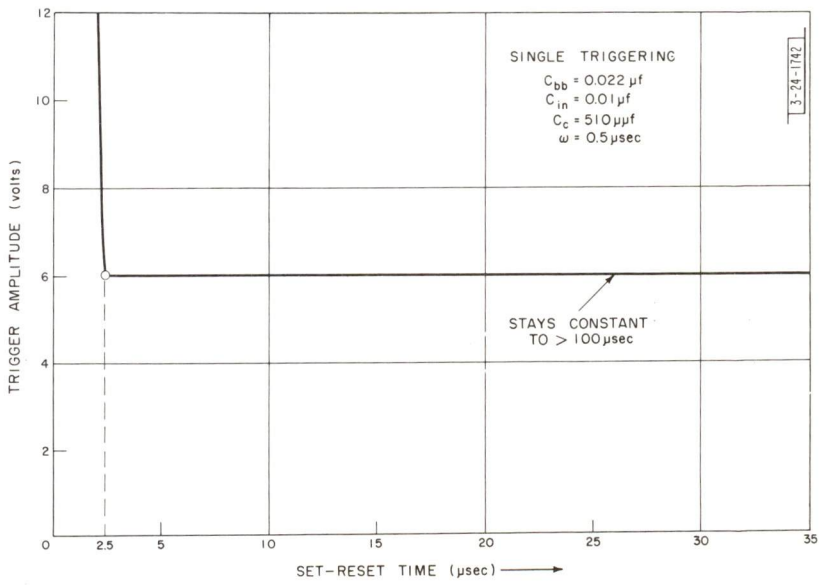


Fig. 12. Set-reset time vs pulse amplitude.

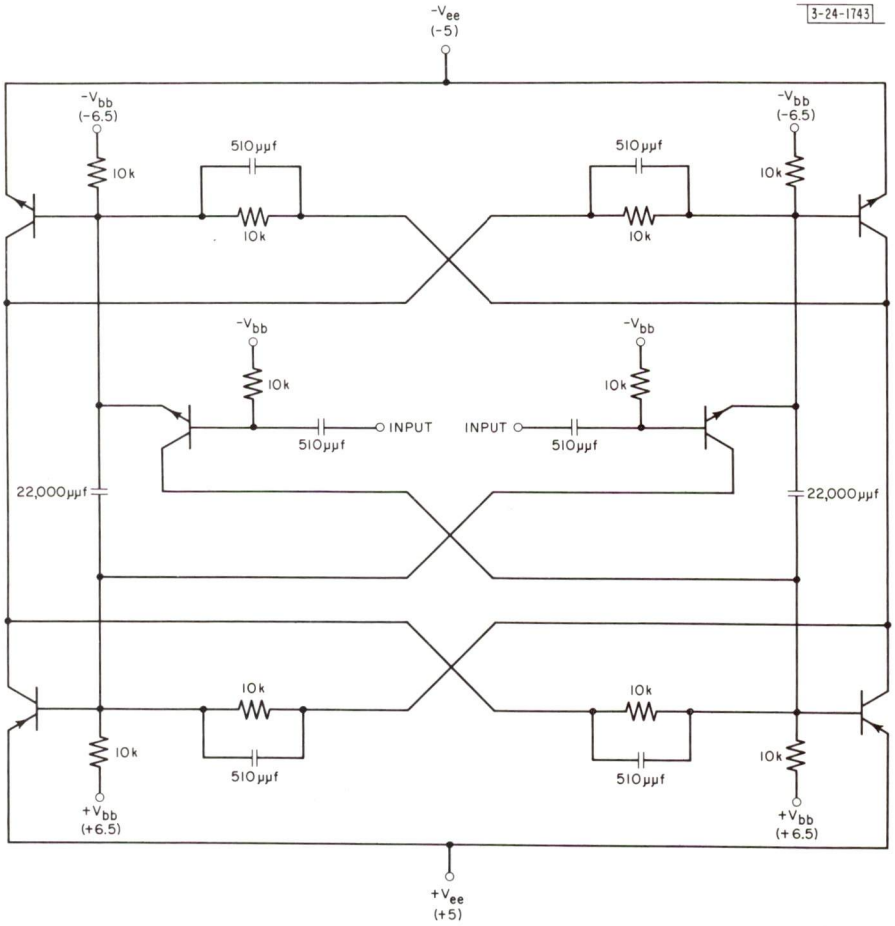


Fig. 13. Circuit diagram of saturated current-demand flip-flop double-triggering (SCDFFD) 1-Mcps transistors.

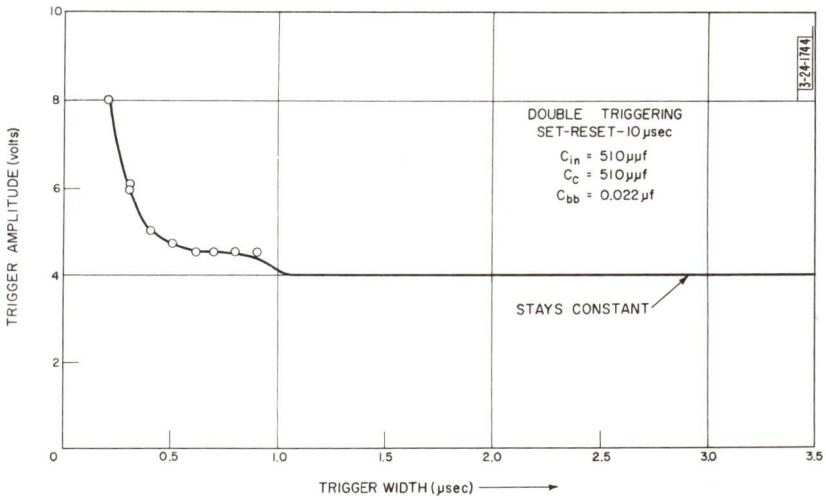


Fig. 14. SCDFFD trigger voltage vs width.

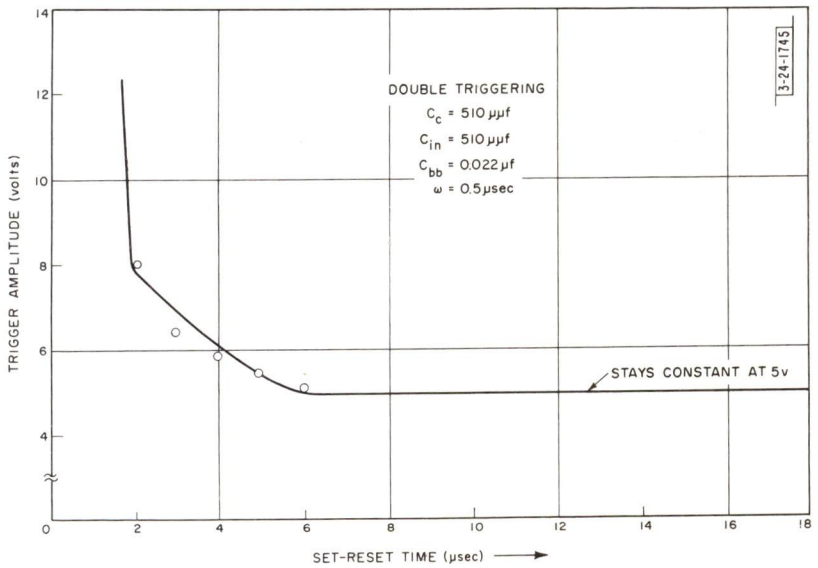


Fig. 15. SCDFFD trigger voltage vs set-reset time.

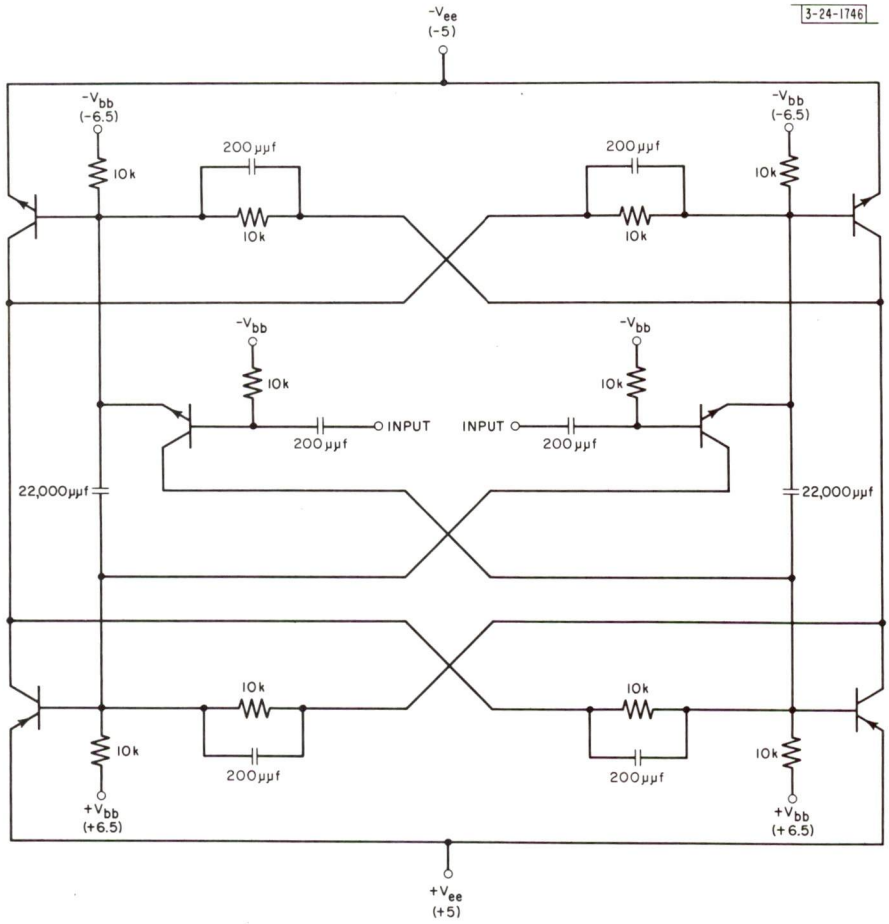


Fig. 16. Circuit diagram of SCDFFD 5-Mcps transistor.

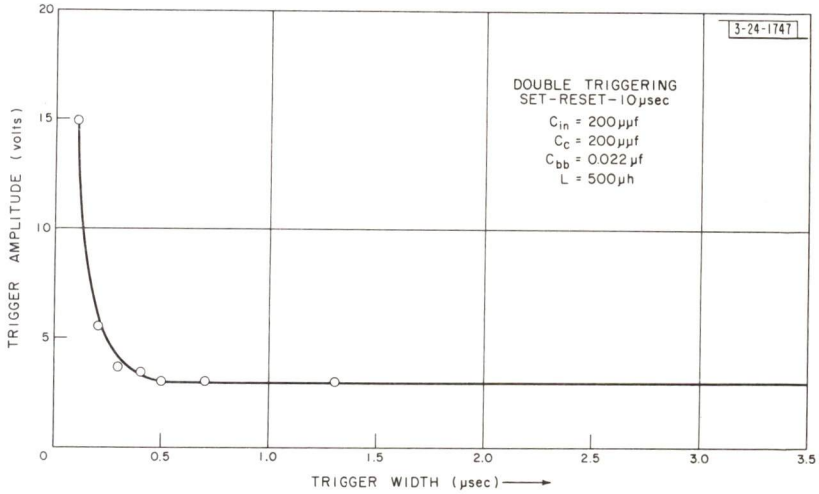


Fig. 17. SCDFFD (5 Mcps) trigger voltage vs width.

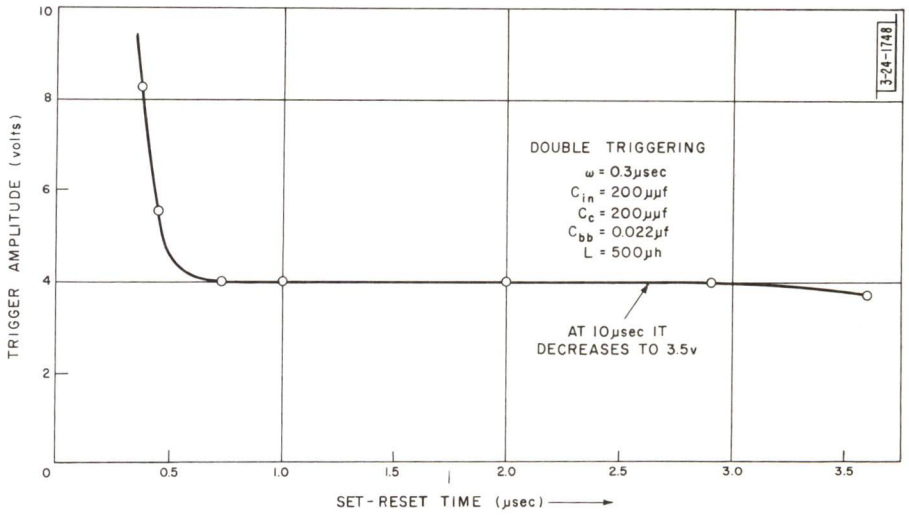


Fig. 18. SCDFFD (5 Mcps) trigger voltage vs set-reset time.

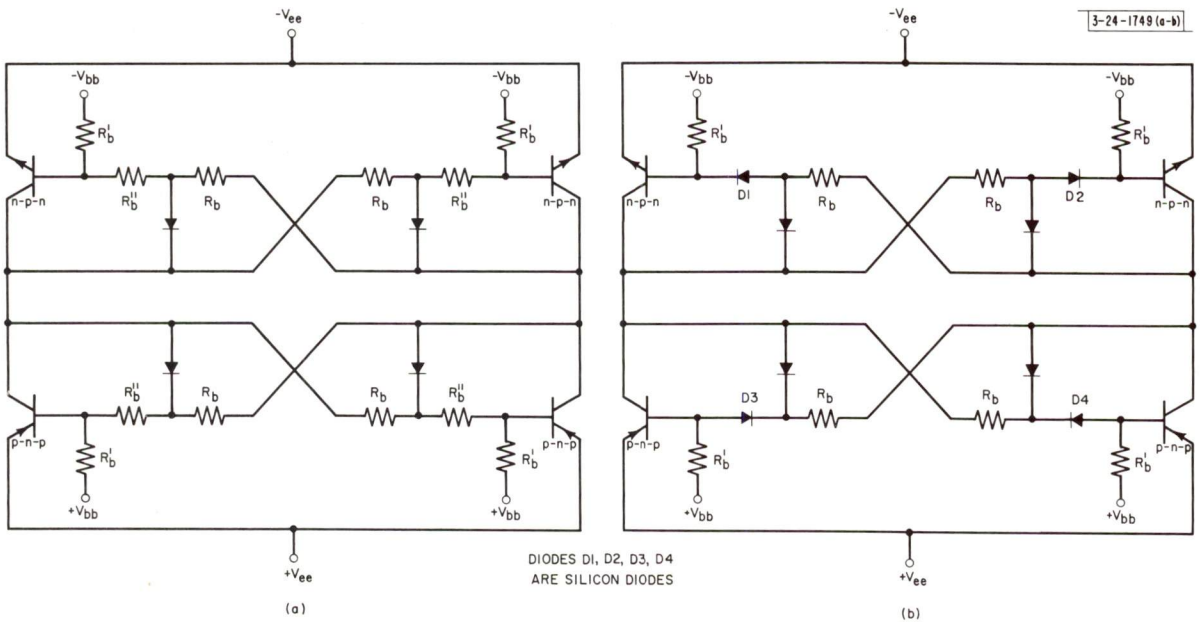


Fig. 19(a) and (b). Nonsaturated current-demand configurations.

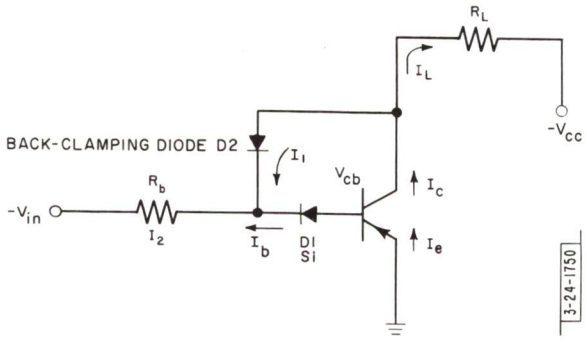


Fig. 20. Analysis of back clamping.

$$(34)\quad I_2 = \frac{V_{in} - V_{D1}}{R_b}$$

$$(35)\quad I_c = \beta_N I_b$$

$$(36)\quad I_1 = I_c - I_L$$

$$(37)\quad I_2 = I_b + I_1$$

$$(38)\quad V_{cb} = V_{D1} - V_{D2}$$

$$(39)\quad I_{c\,max} = I_2\,\beta_N \quad (I_1 = 0)$$

$$(40)\quad I_{c\,min} = I_2 \left(\frac{\beta_N}{1 + \beta_N}\right) \quad (I_L = 0)$$

V_{D1} = forward drop of silicon diode

V_{D2} = forward drop of germanium diode

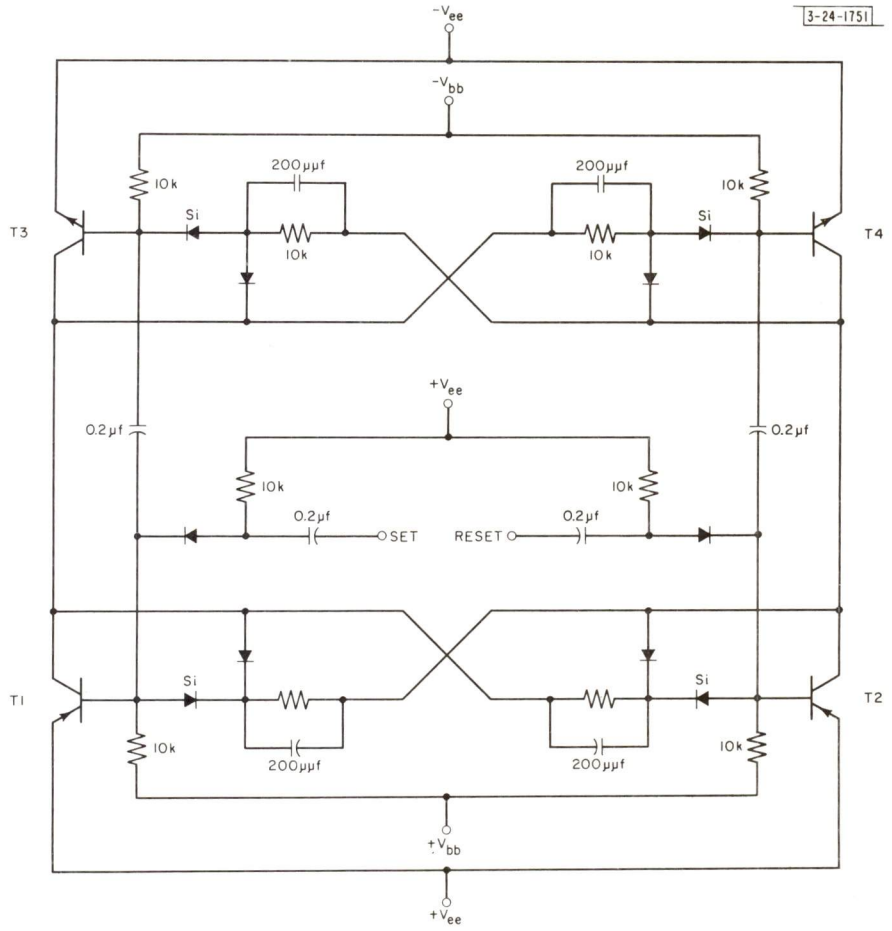


Fig. 21. Circuit diagram of nonsaturated current-demand flip-flop single-triggering (NCDFFS).

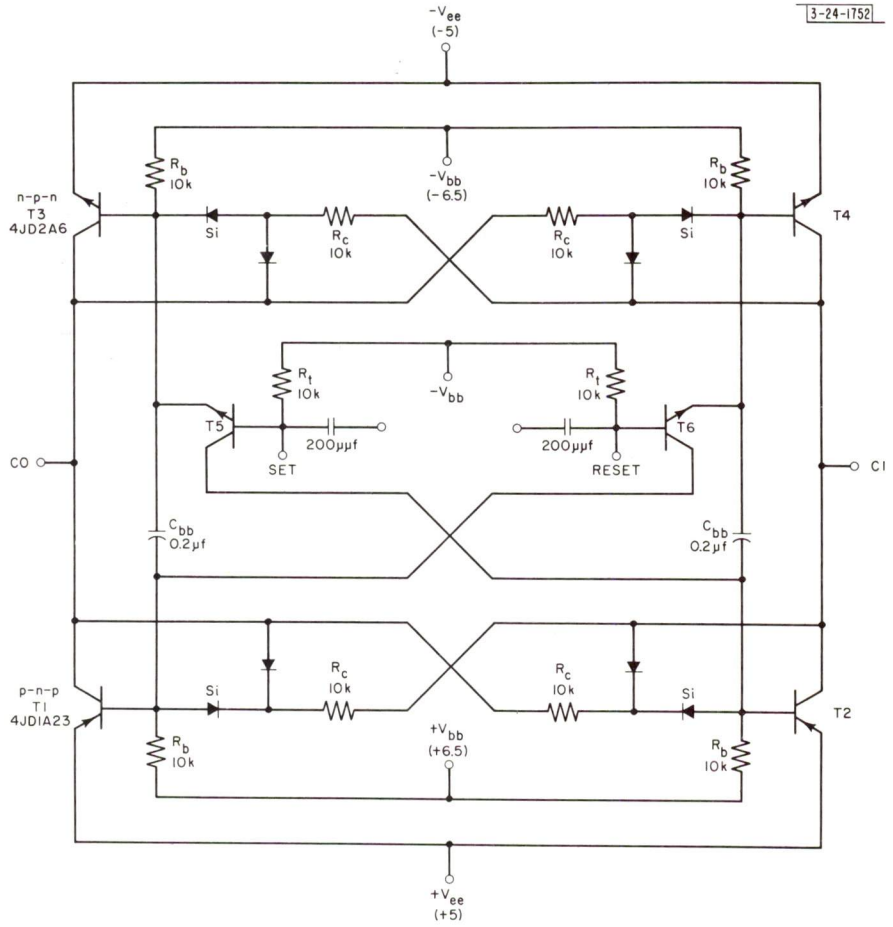


Fig. 22. Circuit diagram of nonsaturated current-demand flip-flop double-triggering (NCDFFD).

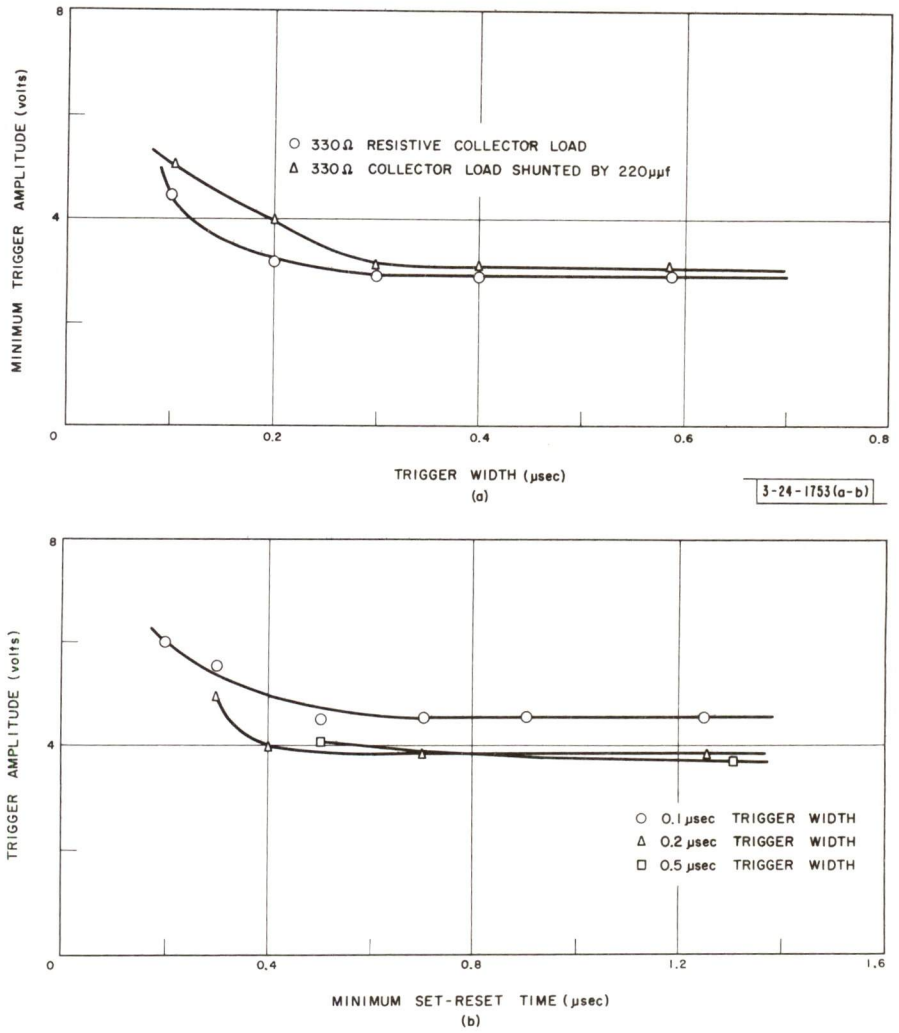


Fig. 23. (a) Trigger voltage vs width (NCDFFD) and (b) trigger voltage vs set-reset time (NCDFFD).

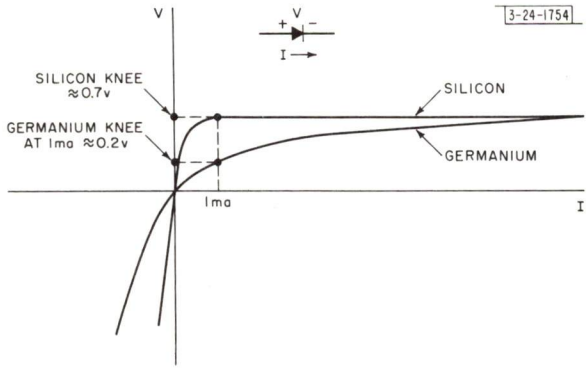


Fig. 24. Diode characteristics.

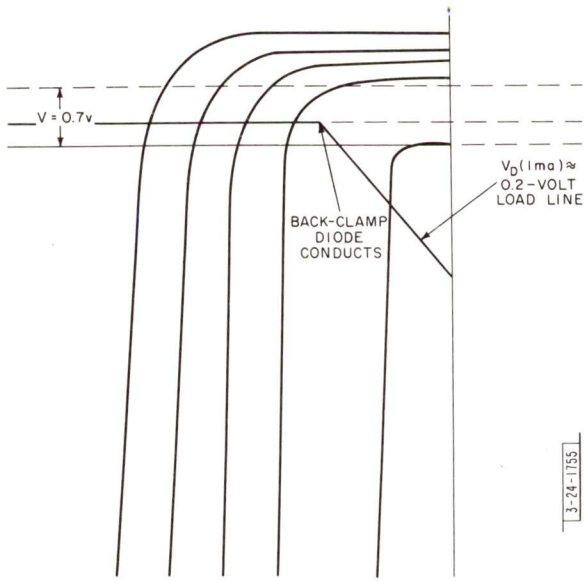


Fig. 25. Silicon transistor collector family.

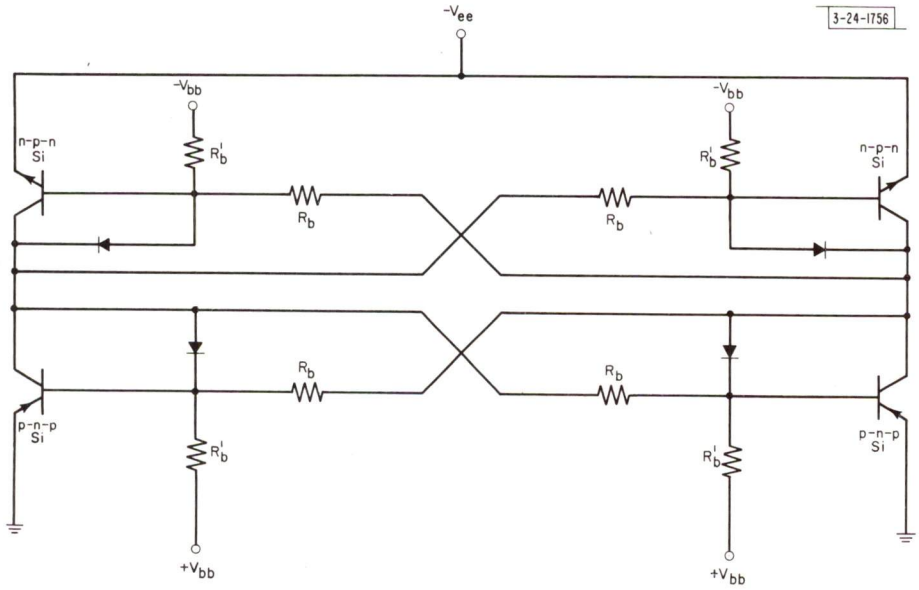


Fig. 26. Basic configuration of silicon nonsaturated current-demand flip-flop (NSiCDFF).

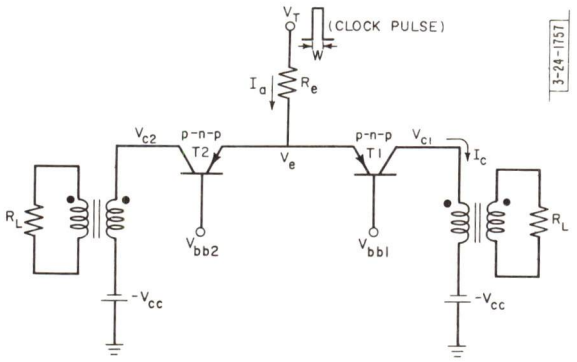


Fig. 27. Pulse-level gate configuration.

standby power:

(41) $PD_{SB} = 2\, V_{cc} I_{co}$

(42) $V_{T\,min} = \dfrac{\alpha_N R_L}{R_e}$

(43) $\omega_{min} > \dfrac{1}{\omega_N} \ln \dfrac{I_e}{I_e - \dfrac{I_{c\,max}}{\alpha_N}}$

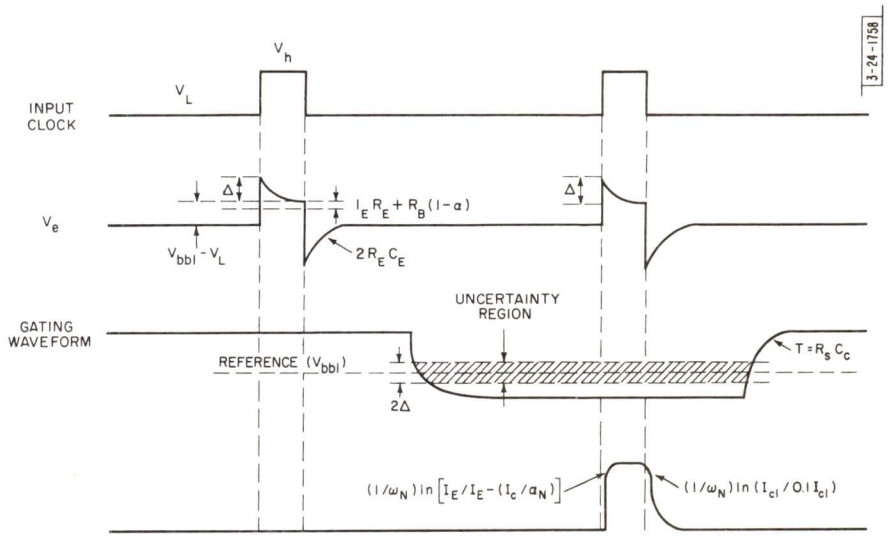
available output power:

(44) $p_{out} = P_{m\,(clock)} - PD_{transistor}$

(45) $V_{bb2} < V_{bb1} + \Delta$ pulse output (side 1)*

$V_{bb2} < V_{bb1} + \Delta$ pulse output (side 2)

*See Fig. 28.



$$I_e \approx \frac{(V_h - V_{bb1},\ V_{bb2})}{R_e}$$

$$\Delta = I_e (R_e + R_b)$$

R_e = emitter resistance of transistor

R_b = base resistance of transistor

R_s = level driving source resistance

Fig. 28. Waveforms of P-L gate.

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UNCLASSIFIED

MAGNETIC RELAXATION IN THIN FILMS

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MAGNETIC RELAXATION IN THIN FILMS†

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A static and dynamic theory are proposed to describe the behavior of thin magnetic films having a uniaxial anisotropy energy $E = K \sin^2\theta$. The theory predicts a reversible hysteresis loop transverse to the axis of lowest anisotropy energy with saturation occurring at a field of $2K/M$; the loop longitudinal to this axis is square with a coercive force of $2K/M$. The effect of a transverse dc field is investigated; such a field reduces the coercive force of the longitudinal loop and may also lead to asymmetrical loops if the magnetic axis is not kept perpendicular to the dc field. The dynamic theory is based on the Landau-Lifshitz equation and considers the application of impulse fields. An expression for the relaxation time is given which depends on the direction of the impulse field with respect to the anisotropy axis. With an impulse field of $2K/M$ the relaxation time varies from ∞ to 1 mμs as the direction of the impulse field varies from being aligned with the magnetic axis to being perpendicular to this axis. Both reversible and irreversible processes can occur in this time range. The theory is also extended to treat the problem of domain-wall motion. Equipment bandwidth limitation does not yet allow observation of processes faster than 20 mμs. Both reversible and irreversible processes have been observed which cannot be resolved in this time.

I. INTRODUCTION

The preparation and magnetic properties of thin films ($\sim$ 1000 Å thick) of vacuum-evaporated 80-20 permalloy have been reported by Blois[1]. When the film is deposited on a heated glass substrate (microscope slide) in the presence of an external magnetic field in the plane of the film, the film develops a preferred magnetic axis in the field direction, becoming a single domain oriented in this direction.

Due to the geometrical symmetry in the plane of the film it is anticipated that rotation of the magnetization in the plane will be unimpeded by energy barriers due to an angular dependence of demagnetizing field energy. Consequently, if a 180° reversing field great enough to overcome the uniaxial anisotropy energy is applied, the magnetization can be expected to reverse by simultaneous rotation of all the electron spins in the plane of the film.

In order to estimate the time for such a simultaneous reversal we refer to the theory developed by Menyuk and Goodenough[2] to describe the switching of toroids of polycrystalline magnetic material. In this case the reversal mechanism is wall motion and the time of reversal τ is given by $(H_m - H_o)\tau = S_w$, with H_m the reversing field, H_o a threshold field for irreversible flux change, and S_w the switching coefficient. S_w for thin-tape toroids of Mo-permalloy has an experimental value of 5×10^{-7} oe-sec. The theoretical expression for S_w gives $S_w \propto d/\delta$, with δ a wall thickness and d the distance this wall moves during reversal. For Mo-permalloy, the theory plus the experimental value of S_w give $d/\delta = 500$. If reversal takes place by rotation as a single domain, we set $d/\delta = 1$, leading to $S_w \approx 10^{-9}$ oe-sec.

The switching coefficient for 80-20 permalloy films as reported by Blois is 2×10^{-7} oe-sec, which is much greater than the extimated value of 10^{-9} oe-sec; however, Conger[3] measured the components of magnetization in the plane of these films during reversal and obtained results which proved that the reversal process was one of rotation. It is the purpose of the present paper to show how these contradictions can be resolved.

† The research in this document was supported jointly by the Army, Navy, and Air Force under contract with the Massachusetts Institute of Technology.

II. THEORETICAL MODEL

A. Static Theory

Let us assume that the uniaxial anisotropy observed in these films can be described by $E_k = K \sin^2\theta$, where E_k is the anisotropy energy, K is the anisotropy constant, and θ is the angle the magnetization M makes with the easy direction. With external fields H_s (switching field) longitudinal to the easy direction and $H_\perp$ transverse to this direction, the total energy becomes (cf Fig. 1)

$$E = K \sin^2\theta + H_s M \cos\theta - H_\perp M \sin\theta. \qquad \ldots (1)$$

For the hysteresis loop in the transverse direction we calculate $M \sin\theta$ vs. $H_\perp$ by setting $H_s = 0$ and $dE/d\theta = 0$. The result is shown in Fig. 2. Note the complete reversibility and the fact that saturation occurs at $H_\perp = 2K/M$.

For the hysteresis loop in the longitudinal direction ($M \cos\theta$ vs H_s) we set $H_\perp = 0$ and now require not only $dE/d\theta = 0$ but also $d^2E/d\theta^2 = 0$, since there is always an extrema at $\theta = 0$ when $H_\perp = 0$; when $d^2E/d\theta^2 = 0$ we pass from the case where this extrema is a minimum to where it is a maximum. This result is also shown in Fig. 2. In this case an irreversible flux change of 2M occurs when $H_s = 2K/M$.

The effect of a transverse dc biasing field on the longitudinal loops is shown in Fig. 3. As $H_\perp$ is increased to the value $2K/M$, the hysteresis loop gradually changes from the square loop to a reversible S-shaped loop. The rotational coercive force changes from the value of $2K/M$ to 0 as $H_\perp$ goes from 0 to $2K/M$. The functional dependence is found from the equations $dE/d\theta = d^2E/d\theta^2 = 0$. The result is

$$H_s\left(\frac{M}{2K}\right) = h_c^r = \cos^3\theta \qquad \ldots (2)$$

$$H_\perp \left(\frac{M}{2K}\right) = h_\perp = \sin^3\theta,$$

where H_s and $H_\perp$ are normalized with respect to the "anisotropy field" $H_k = \frac{2K}{M}$. h_c^r as a function of $h_\perp$ is shown in Fig. 4.

Next let us consider the more general case of the magnetic axis making an arbitrary angle α with the h_s direction and a pick-up coil which measures the flux in the h_s direction. The energy expression becomes (Fig. 5)

$$E = 2K\left[\frac{\sin^2\theta}{2} + h_s \cos(\alpha+\theta) - h_\perp \sin(\alpha+\theta)\right] \qquad \ldots (3)$$

If $h_\perp = 0$, the loops will be symmetrical and, as α goes from 0 to 90°, gradually change from the square form to the straight line form (Fig. 6-I). When $h_\perp \neq 0$ asymmetrical loops are to be expected, since it is clear that when $h_s = 0$ the equilibrium positions (θ_1 and θ_2) of M are not now symmetrical with respect to the axis of the pick-up coil. If these two equilibrium positions are in the first two quadrants M will move back and forth in these quadrants during a loop cycle; this is the case for $h_\perp = 0.5$, $\alpha = 45^\circ$ (Fig. 6-II). If the equilibrium positions are in the first and third quadrants, M will rotate a full 360° around the loop (Fig. 6-III, with $h_\perp = 0.5$, $\alpha = 60^\circ$). Finally, as α gets very near 90°

the loop becomes reversible (Fig. 6-IV, with $h_\perp = 0.5$, $\alpha = 75^\circ$).

B. Dynamic Theory

We now wish to calculate the time for the magnetization to change from one equilibrium position to another after the application of an external field having components h_s and $h_\perp$; the external field is considered to be turned on instantaneously. Consider first the two limiting cases $h_s = 0$, $h_\perp \neq 0$, and $h_s \neq 0$, $h_\perp = 0$. In the former case the impulse field $h_\perp$ is perpendicular to $\underline{M}$, producing a torque $h_\perp \times \underline{M}$ which is a maximum at $t = 0$; the rotational relaxation time $(\Delta t)_\theta$ should be as short as it ever will be. However, when $h_\perp = 0$ the impulse field is h_s and $h_s \times \underline{M} = 0$, so that no torque is ever applied and the relaxation time is infinite. With both fields applied simultaneously we expect the relaxation time to be in between these limiting cases.

In order to calculate $(\Delta t)_\theta$ we must consider the torque acting on the spins during the entire course of the relaxation process; for this purpose we take $T(\theta) = -dE/d\theta$. To relate this torque to the speed of motion we make a quasistatic approximation of the following sort: assume that the angular velocity $\dot{\theta}$ is at every instant proportional to the instantaneous torque, i.e.,

$$\dot{\theta} = a\,T(\theta) = -a\,\frac{dE}{d\theta}\,. \qquad \ldots (4)$$

Integrating Eq. 4 gives the relaxation time $(\Delta t)_\theta$ as

$$(\Delta t)_\theta = \frac{1}{a}\int_{\theta_1}^{\theta_2} \frac{d\theta}{T(\theta)}\,. \qquad \ldots (5\text{-a})$$

For the energy given by eq. 1

$$(\Delta t)_\theta = \frac{1}{2aK}\int_{\theta_1}^{\theta_2} \frac{d\theta}{h_s \sin\theta + h_\perp \cos\theta - \sin\theta\cos\theta}\,. \qquad \ldots (5\text{-b})$$

In evaluating the above integral the lower limit θ_1 will be the equilibrium angle before the impulse field is turned on. If h_s and $h_\perp$ are both turned on simultaneously θ_1 will be zero; however if $h_\perp$ is a dc biasing field, θ_1 is determined from the static theory by $\sin\theta_1 = h_\perp$. For the upper limit θ_2, the static equilibrium conditions may lead to an infinite relaxation time. This is simply due to the continually decreasing torque as M comes nearer and nearer to its final equilibrium value. To avoid this difficulty we determine θ_2 by the condition that the relaxation voltage pulse at θ_2 shall have dropped to 0.1 of its maximum value. For the switching voltage we have

$$e = M\dot{\theta}\sin\theta = Ma\,T(\theta)\sin\theta. \qquad \ldots (5)$$

In order to compare the experimental and theoretical voltage pulses, eq. 5 must be expressed as a function of time. This is not easily done and numerical methods must be used.

The integral in eq. 5-b can be easily evaluated for the case $h_s = 0$, $h_\perp = 1$; the limits are found to be $\theta_1 = 0$, $\theta_2 = 68.5^\circ$. We find

$$2K \int_0^{68.5^\circ} \frac{d\theta}{T(\theta)} = 7.48$$

from which $(\Delta t)_\theta = 3.74/aK$. A typical value of K, measured from the transverse loop at 1000 cps, is 10^3 ergs/cc (corresponding to $H_c^r = 2$ oe); the value of a must either be determined from an impulse relaxation experiment, or related to the ferromagnetic resonance measurement of relaxation. As will be shown in the next section, the value of a from resonance experiments is $\sim 3 \times 10^6$ $(oe^2\text{-sec})^{-1}$ so that $(\Delta t)_\theta \sim 1$ mμs. However, as will be shown in the next section, the simple theory given here is expected to break down for a process as fast as this, predicting a shorter relaxation time than would actually be the case. Experimentally, the transverse relaxation time is found to be ≤ 20 mμs, which is the lower limit on the timewise resolution of the experimental equipment.

For general values of h_s and $h_\perp$ the integral of eq. 5-b must be evaluated by numerical calculation. The results for various values of h_s and $h_\perp$ are shown in (Fig. 7-a and 7-b); the range of h_s is taken as $0 \leq h_s \leq 2$ and for $h_\perp$ we choose $0 \leq h_\perp \leq 1$. Since $(\Delta t)_\theta$ goes to ∞ for some of the fields in these ranges we plot $[2aK(\Delta t)_\theta]^{-1}$ vs $h_\perp$ (fixed value of h_s) (Fig. 7-a) and $[2aK(\Delta t)_\theta]^{-1}$ vs h_s (fixed values of $h_\perp$) (Fig. 7-b). In interpreting Fig. 7 the limitations of the quasistatic theory already mentioned must be kept in mind.

The above simple description of the motion of M takes no account of the acceleration required to keep the angular velocity proportional to the torque; equally serious is the fact that the torque $= -dE/d\theta$ is in the wrong direction to provide for motion of M in the θ direction. This is due to the angular momentum carried by the electron spins whose associated magnetic moments make up M. The torque $-dE/d\theta$ will initially tend to make M start to move upward out of the plane of the film, and it is the resultant demagnetization fields which provide the torque to move M in the θ-direction. For the details of these effects we now turn to a consideration of the Landau-Lifshitz equation of motion for the magnetization.

C. Landau-Lifshitz equation

The well-known Landau-Lifshitz equation[4] is

$$\dot{\underline{M}} = \gamma(\underline{M} \times H) - \lambda(\underline{M} \times \underline{H} \times \underline{H}), \qquad \ldots (6)$$

with γ the gyromagnetic ratio and λ an arbitrarily introduced damping constant. The coordinates for the description of the motion are shown in Fig. 8; the only new parameter is the angle ψ, by which M tilts upward out of the plane of the film. From Fig. 8 we see that $H_x = -H_s + H_k$, $H_y = H_\perp$, and $H_z = -4\pi M \sin\psi$. Substituting in eq. 6 and assuming $\sin\psi = \psi$, $\cos\psi = 1$, and $4\pi M \gg H_x$ or H_y, we find

$$\dot{\theta} = 4\pi\gamma M\psi + \frac{\lambda}{M^2} T(\theta) \qquad \ldots (7\text{-a})$$

$$\dot{\psi} = -4\pi\lambda\psi + \frac{\gamma}{M} T(\theta). \qquad \ldots (7\text{-b})$$

These are a pair of coupled equations in θ and ψ and provide for the translation of the torque T into a direction suitable to make M move in the θ-direction.

The previous assumption that we could write $\dot{\theta}=aT$ leads us to set T = constant in eq. 7-b and solve for ψ. With the initial conditions $t=0$, $\psi=0$, $\theta=0$ we find

$$\psi = \frac{\gamma T(0)}{4\pi M} (1-e^{-4\pi\lambda t}). \qquad \ldots (8\text{-a})$$

If the change in θ (and thus $T(\theta)$) is small in the time $1/4\lambda$ required for ψ to reach the quasistatic limiting value of eq. 8-a, we can regard ψ as only an implicit function of time through its θ dependence, and can disregard the explicit exponential dependence. Thus we write

$$\psi = \frac{\gamma T(\theta)}{4\pi M}. \qquad \ldots (8\text{-b})$$

Finally for $\dot{\theta}$ we have

$$\dot{\theta} = \left(\frac{\gamma^2}{\lambda} + \frac{\lambda}{M^2}\right) T(\theta), \qquad \ldots (9\text{-a})$$

which is of the form of eq. 4 with $a = \gamma^2/\lambda + \lambda/M^2$. From microwave resonance experiments $\lambda \sim 10^8$ cps*; for permalloy $M \sim 10^3$ oe; the gyromagnetic ratio $\gamma = 1.7 \times 10^7$ $(\text{oe-sec})^{-1}$. Thus $\gamma^2/\lambda \sim 3 \times 10^6$ $(\text{oe}^2 - \text{sec})^{-1} \gg \lambda/M^2 \sim 10^2$ $(\text{oe}^2 - \text{sec})^{-1}$ and eq. 8-a becomes

$$\dot{\theta} = \frac{\gamma^2}{\lambda} T(\theta). \qquad \ldots (9\text{-b})$$

Let us now examine the validity of the approximation of quasistatic motion which leads to eq. 9-b. From eq. 8-a ψ will reach an equilibrium value consistent with a given torque in a time approximately given by $(\Delta t)_\psi = 1/4\pi\lambda \sim 1$ mμs. Thus a good description of experiment might be expected for $(\Delta t)_\theta \sim 10$ mμs. For motion completed in a time < 10 mμs the relaxation time predicted by the quasistatic theory will be too short, since the torque $= dE/d\theta$ is only translated into the correct direction to provide motion in the θ direction with a time constant of 1 mμs. Thus all of the theoretical relaxation times of the previous section are too short by a factor which will become worse the shorter the relaxation time. However, it is to be expected that the general dependence of $(\Delta t)_\theta$ on h_s and $h_\perp$ will be preserved by a more exact theory.

D. Domain-Wall Motion

The previous theory of relaxation time can be readily used to obtain an expression for the velocity of a moving domain wall. We write

$$v = \frac{\delta}{(\Delta t)_\theta}, \qquad \ldots (10)$$

*P. Tannenwald, M.I.T. Lincoln Laboratory, (private communication)

where v is the wall velocity, δ the wall thickness, and $(\Delta t)_\theta$ the relaxation time of a spin as the wall moves by. From the well-known static wall theory we have[5]

$$\delta = 2\sqrt{\frac{K}{A}} \int_{0+\varepsilon}^{\pi/2-\varepsilon} \frac{d\theta}{g(\theta)^{1/2}}, \qquad \ldots(11)$$

where A is the exchange constant, K the anisotropy constant, $g(\theta)$ the angular dependence of the anisotropy energy, and ε a small number chosen to keep the integral from going infinite. For $(\Delta t)_\theta$ we write

$$(\Delta t)_\theta = \frac{\lambda}{\gamma^2} \int_{\theta_1}^{\theta_2} \frac{d\theta}{T(\theta)},$$

where $T(\theta) = -dE/d\theta$, and we must add the exchange energy into the expression for E. From static wall theory, we know that for each spin in the wall the exchange and anisotropy energies are equal, so that

$$E = 2K\, g(\theta) + \underline{H} \cdot \underline{M} \qquad (12)$$

The final form for v is

$$v = \frac{2\gamma^2}{\lambda} \sqrt{\frac{A}{K}} \left[\int_{0+\varepsilon}^{\pi/2-\varepsilon} \frac{d\theta}{g(\theta)^{1/2}} \right] \left[\int_{\theta_1}^{\theta_2} \frac{d\theta}{\left(\frac{\underline{H}\cdot\underline{M}}{MH_s}\right)' - \frac{1}{h_s} g'(\theta)} \right]^{-1} MH_s \qquad \ldots (13)$$

Equation 12 is to be compared with the expression given by Kittel[6]

$$v = \frac{2\gamma^2}{\lambda} \sqrt{\frac{A}{K}} \left[\int_0^{\pi} \left[g(\theta) \right]^{1/2} d\theta \right]^{-1} MH_s. \qquad \ldots (14)$$

The two expressions are the same except for the normalized integrals over the angle θ. Note that the new expression contains a nonlinear dependence of v on the driving field. A detailed comparison has not yet been made.

III. EXPERIMENTAL

A. Low-Frequency Hysteresis Loops

Low-frequency hysteresis loops are measured using the circuit of Fig. 9, which is patterned after that used by Crittenden[7]. The setup uses only standard commercial amplifiers plus the pick-up and drive coils and a simple balanced RC integrating network.

The transverse and longitudinal hysteresis loops ($\alpha = 90^\circ$ and 0°, $h_1 = 0$) of a typical film in a 1000 cps drive field are sketched in Fig. 10. It is seen that if we associate the saturation field in the transverse direction with $2K/M$, then in the longitudinal direction reversal is taking place in a field considerably less than the expected rotational coercive force of $2K/M$. This low value of coercive force must be due to domain walls and we designate it as the wall coercive force H_c^w. A very good

demonstration of wall reversal is obtained by lowering the frequency to 10 cps and examining the unintegrated voltage from the pick-up coil. The result is shown schematically in Fig. 11. It is seen that reversal takes place by discontinuous Barkhausen jumps, which have long been associated with wall motion. An idea of the speed of these walls can be obtained by varying the drive frequency. It is found that at 100 cps the resolution of the jumps illustrated in Fig. 11 is lost, and the reversal voltage is a single rounded pip. That walls can exist in thin films was first shown by direct observation using the Kerr effect by Fowler and Fryer.[9] Subsequently, observations using colloidal magnetite have been reported by Williams.[10]

If the longitudinal loop ($\alpha = 0$) is measured with a transverse dc biasing field $h_\perp$ present, the behavior predicted by Fig. 3 is obtained as soon as $h_\perp$ is large enough to make $h_c^r < h_c^w$. Variation of the angle α, with $h_\perp = 0$ leads to behavior of the type predicted by Fig. 6-I; when α is varied and $h_\perp \neq 0$, asymmetrical loops of the types shown in Fig. 6-II, III, and IV, are observed. The angle α can be varied by physically rotating the film, or by straining a film which has magnetostrictive properties. Asymmetrical loops obtained by straining magnetostrictive films were first reported by Mitchell and Rubens.[8] In all cases care must be taken to distinguish between rotational and domain-wall processes.

B. Impulse Behavior

The presence of a wall coercive force H_c^w which is considerably less than the rotational coercive force H_c^r means that in order to study the rotational relaxation time under impulse conditions we must apply a drive pulse which has a rise time short compared to the time required for walls to form and move. The apparatus used to accomplish this is shown schematically in Fig. 12. The drive pulse has a rise time of 2.5 mμsec and is generated by discharging a coaxial line through a mercury relay. In order to provide for an H-field with plane geometry, the pulse is sent down a strip transmission line, which is terminated to avoid reflections. A pulse to reset the film after reversal by the fast-rise-time drive pulse is provided by a capacitor discharging through a second mercury relay. The pick-up loop is balanced to eliminate air coupling as shown in Fig. 12; the balance may be made quite exact by inserting a tapered aluminium strip in one side or the other as required. A section of fine nichrome resistance wire makes up part of the loop in order to reduce circulating currents generated by the drive field. The film is placed in one arm of the loop and may be placed with its magnetic axis either parallel or perpendicular to the drive field. A photograph of this line is shown in Fig. 13-a, in which the nichrome-wire pick-up loop and supporting posts are easily seen. Fig. 13-b shows the line mounted in a pair of Helmoltz coils which provide a dc biasing field. In order to eliminate the magnetic field of the earth the whole assembly is placed in a large, double-walled, μ-metal box.

A convenient way to experimentally establish the time scale for rotational relaxation processes is to examine the transverse hysteresis loop in the pulse apparatus described above. In this case walls do not play a role, and there is a strong impulse torque applied the instant the drive field is turned on. The drive and output pulses are shown schematically in Fig. 14-a and b. The impulse H has a rise time of 2.5mμsec measured directly on the plates of the oscilloscope; a purposely unbalanced pick-up loop should have an output proportional to the derivative of the drive pulse, in this case a square topped pip of width 2.5 mμs. However, the actual output is rounded and of 20 mμs duration, because of the band width limitation of the scope pre-amplifier. As shown in Fig. 14-b, the transverse film-pips have the same form as the unbalanced air-coupling pips, so that the most that can be said is that the relaxation time is $<$ 20 mμs, with $h_\perp = 1$. Note that when the drive pulse is turned off a second film pip occurs as the magnetization swings back to its old equilibrium value. The theoretical relaxation time for this case has already been found to be 1 mμs ; thus theory and experiment are at least consistent.

For the case of the drive pulse in the longitudinal direction we expect irreversible switching, and consequently a restore pulse must follow each drive pulse and return the film to its initial state. This restore pulse is not shown in Fig. 12. With proper values of $h_\perp$ and h_s, the pick-up output should be much like the transverse case, except for the absence of the second pip, since the switching can now be irreversible. Again the same limitations on the viewing equipment arise; however, as shown in Fig. 10-c the film can be made to switch irreversibly in times $\leq$ 20 mμs with $h_s = 1$ and a suitably chosen $h_\perp$. As $h_\perp$ is varied a continuous range of rotational switching speeds can be observed, which vary over the range 1000 to 20 mμs. The effect of $h_\perp$ on lowering the rotational coercive force (cf Fig. 4) has been demonstrated by Olson, Pohm and Rubens."

An adequate experimental study of the relaxation behavior requires considerable improvement in experimental techniques. In this direction, a traveling wave oscilloscope with a band pass of 3000 mc will be employed to resolve the fastest relaxation behavior. A second difficulty involves spurious noise in the final oscilloscope display which should be eliminated by making the mercury relay completely coaxial. In addition, a coaxial relay can be expected to have a rise time another order of magnitude faster than 2.5 mμs, which will be needed in order to study the fastest relaxation phenomena.

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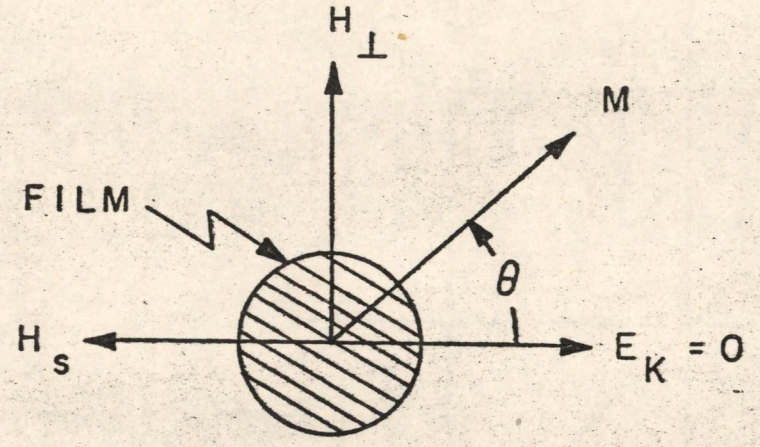

FIG. 1

$$E = K \sin^2\theta + H_s M \cos\theta - H_\perp M \sin\theta$$

STATIC MODEL OF AN ANISOTROPIC THIN FILM

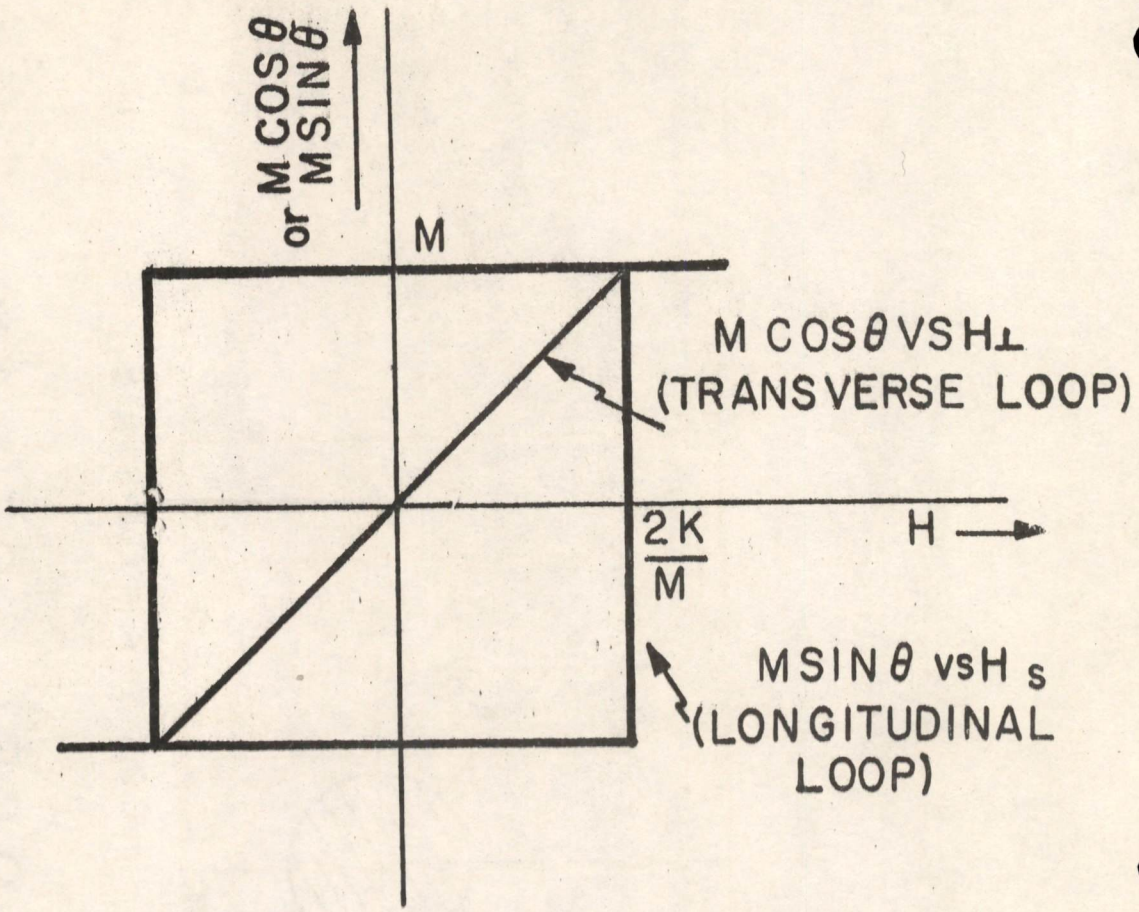

FIG. 2

THEORETICAL HYSTERESIS LOOPS
FROM THE MODEL OF FIG.1

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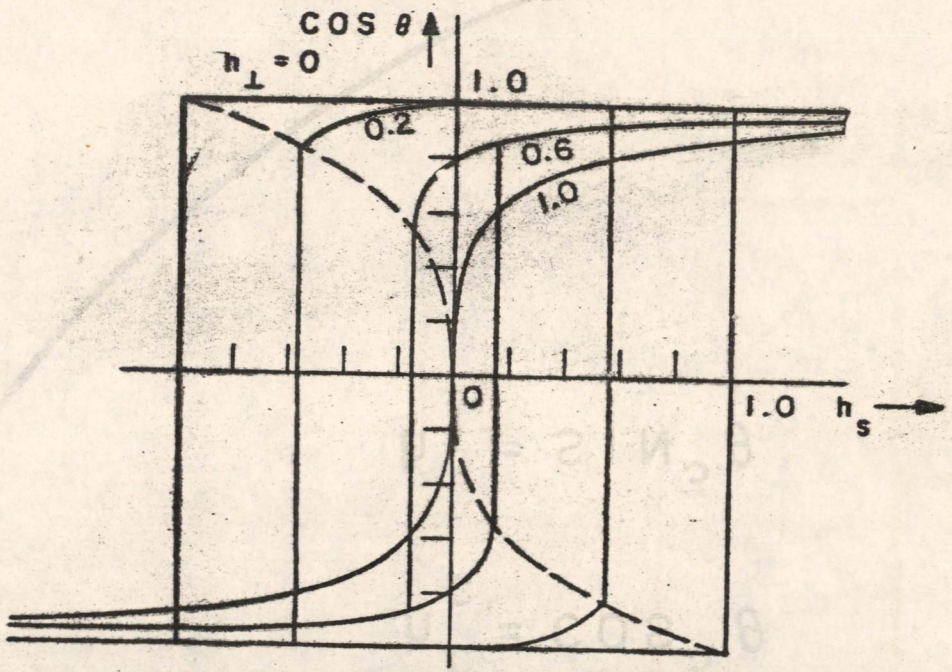


FIG. 3 THEORETICAL LONGITUDINAL HYSTERESIS FOR VARIOUS TRANSVERSE FIELDS $h_\perp$

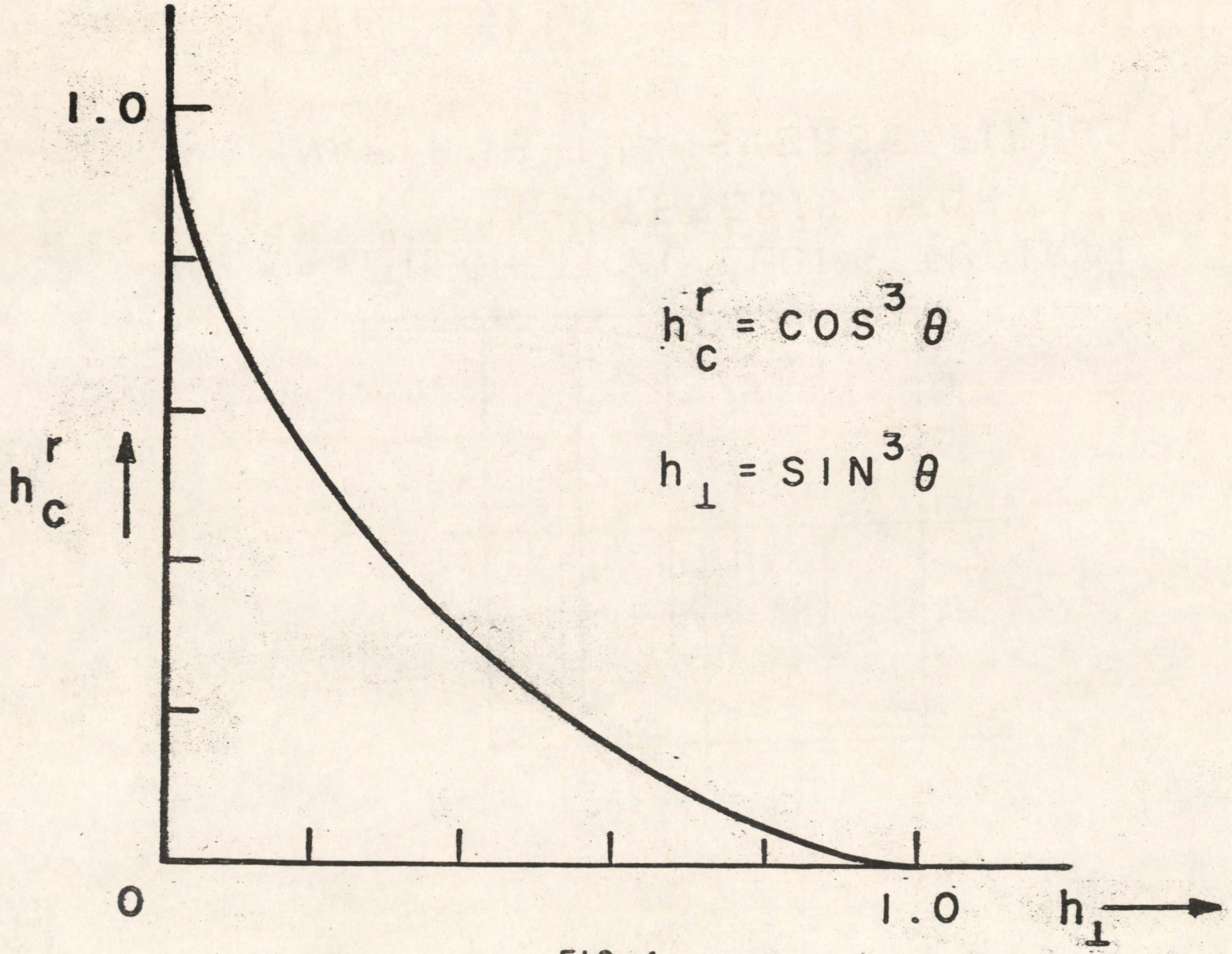
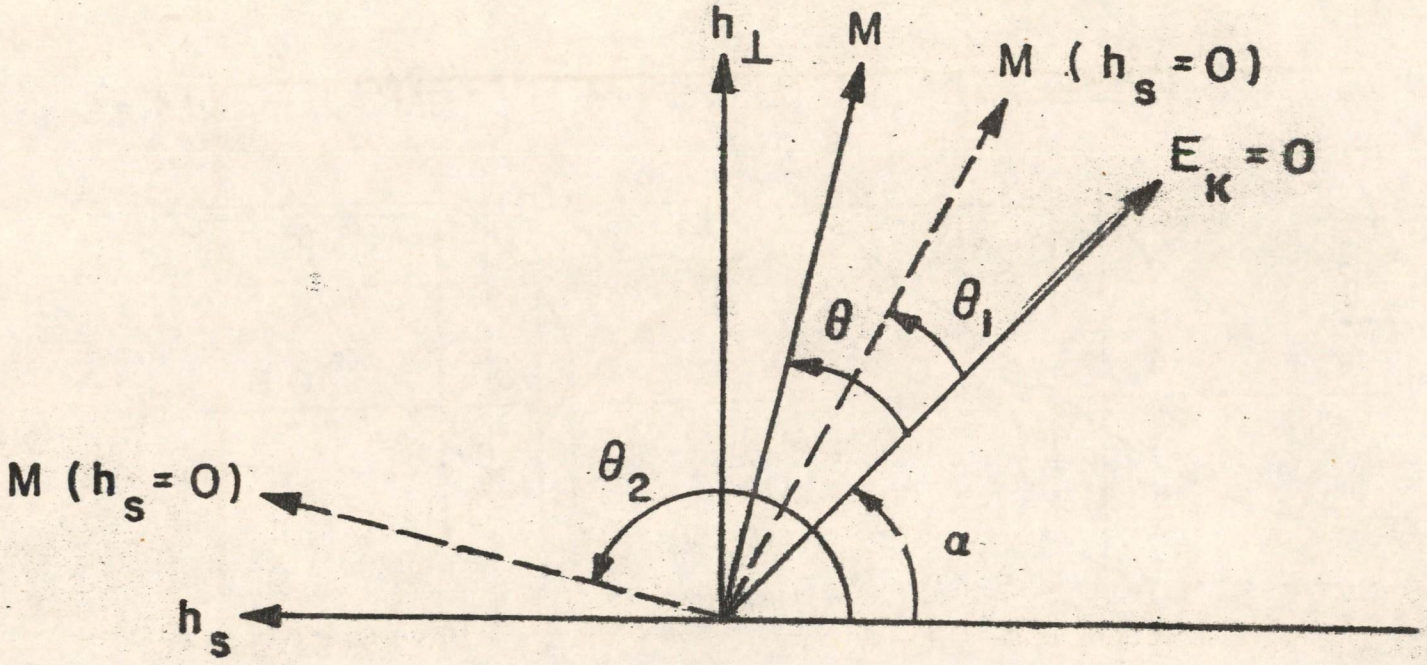


FIG. 4

ROTATIONAL COERCIVE FORCE h_c^r
vs TRANSVERSE FIELD $h_\perp$



$$E = \frac{2K}{M}\left[\sin^2\theta + h_s \cos(\alpha+\theta) - h_\perp \sin(\alpha+\theta)\right]$$

FIG. 5

ASYMMETRIC STATIC MODEL

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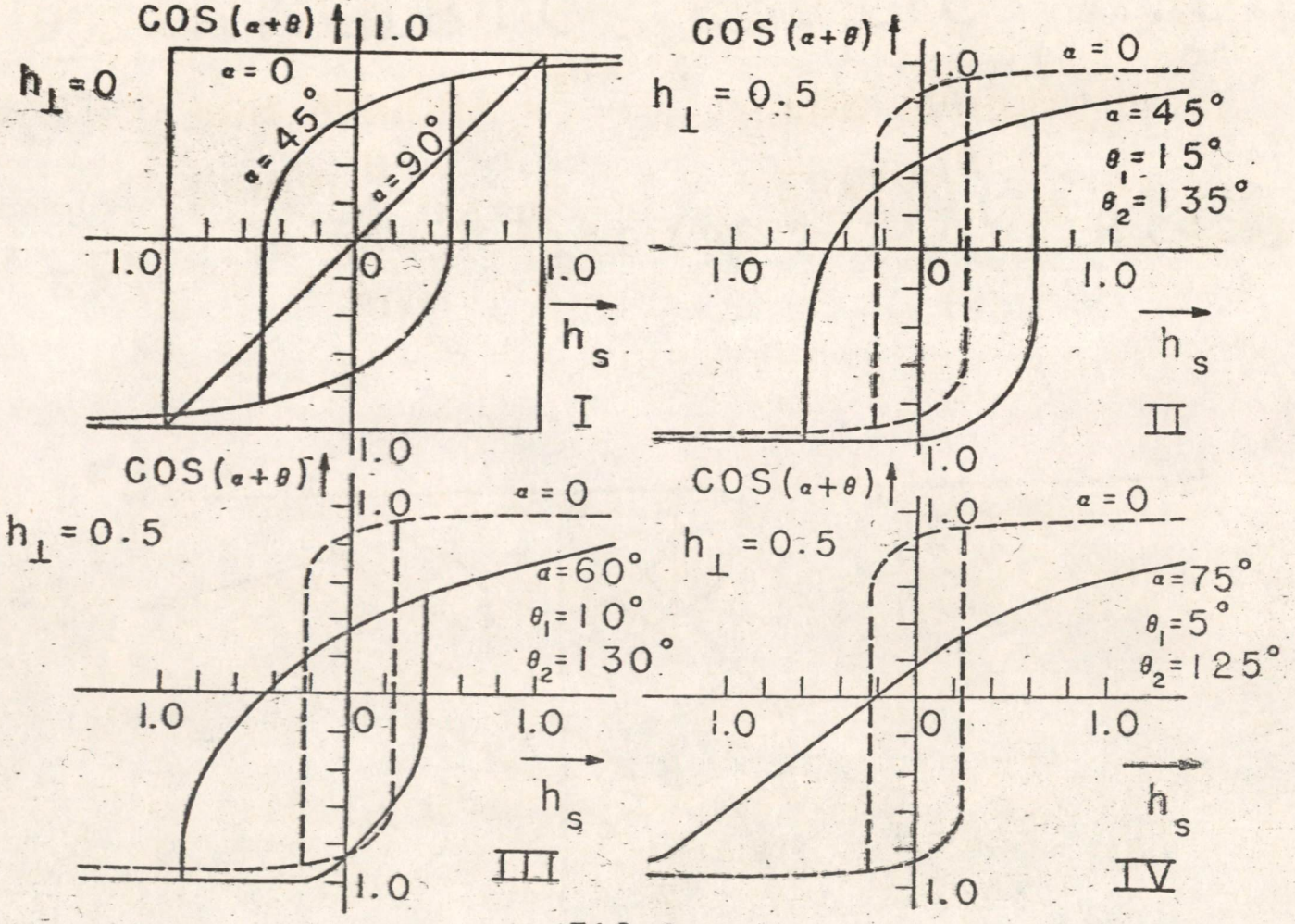


FIG. 6

THEORETICAL ASYMMETRICAL HYSTERESIS LOOPS

C-67921
[illegible]-1543
[illegible]-3399

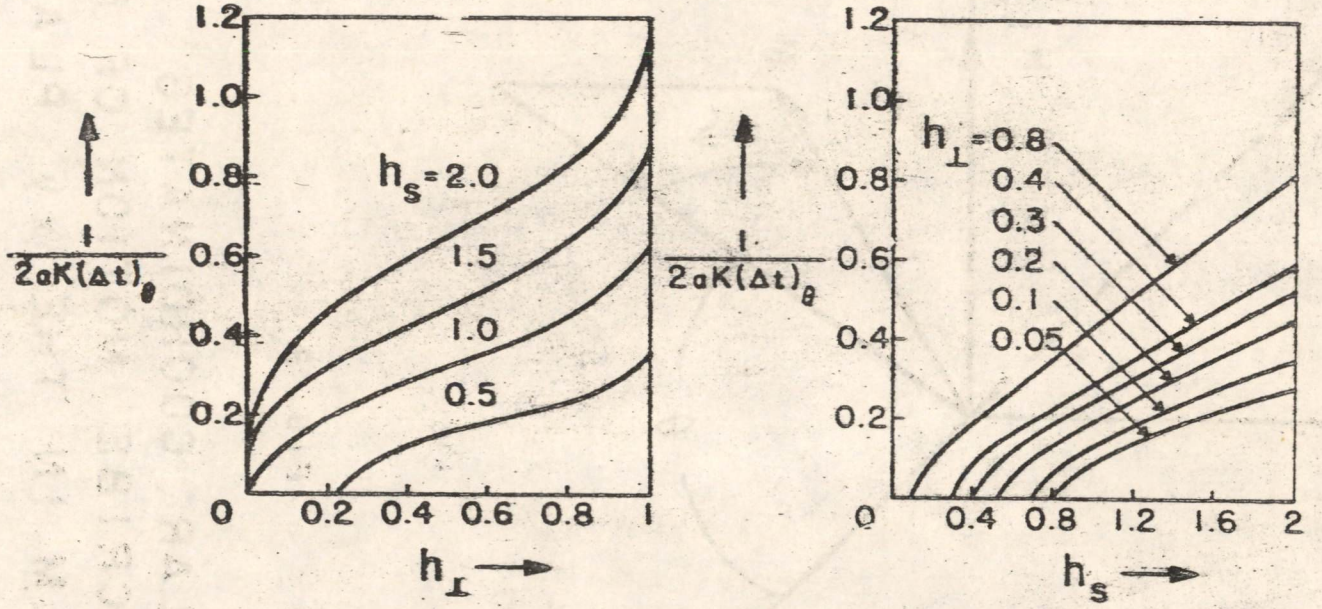


FIG. 7

(a)

$\frac{1}{2aK(\Delta t)_\theta}$ vs $h_\perp$

FOR VARIOUS h_s

(b)

$\frac{1}{2aK(\Delta t)_\theta}$ vs h_s

FOR VARIOUS $h_\perp$

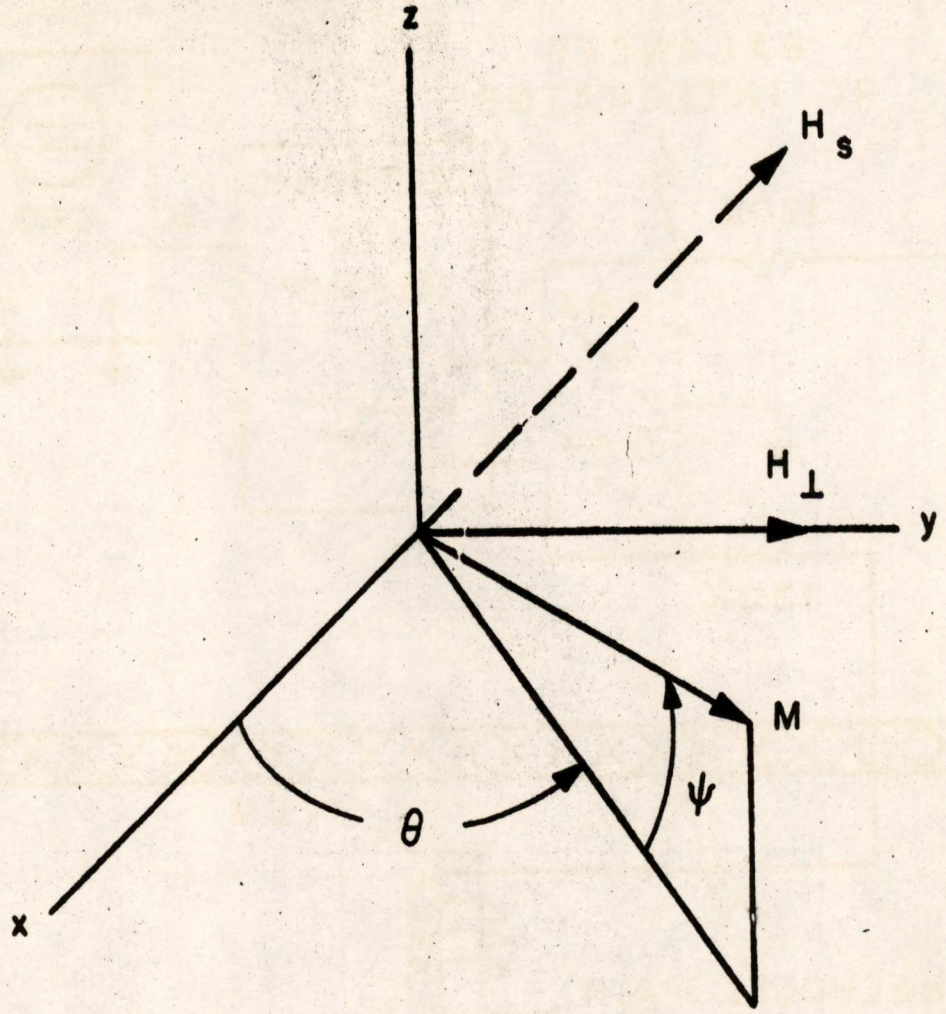


FIG. 8

ANGULAR COORDINATES
TO DESCRIBE MOTION OF M
WITH FILM IN THE xy PLANE

A-67672

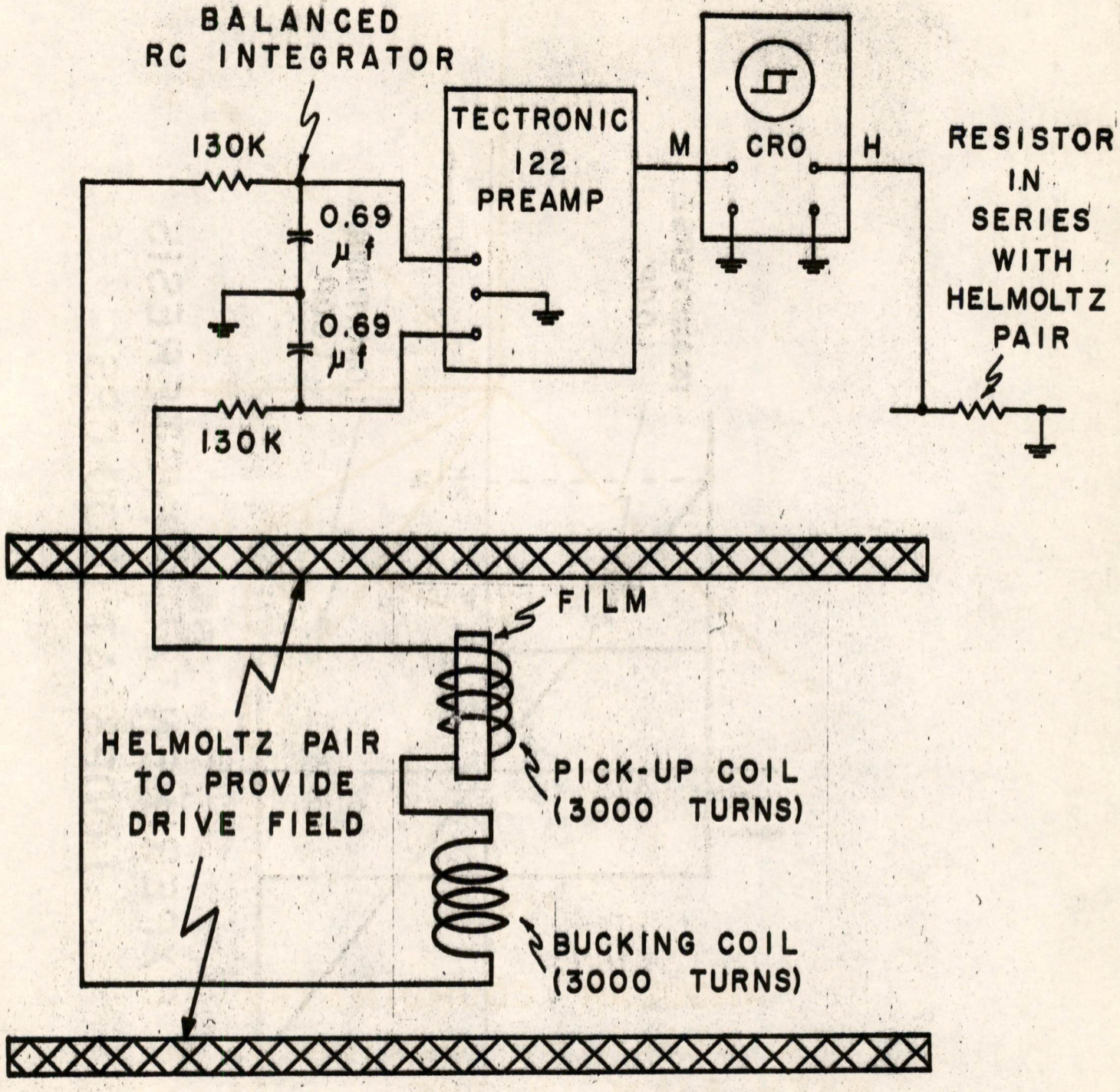


FIG. 9

CIRCUIT FOR MEASURING 1000 CPS HYSTERESIS LOOPS OF THIN FILMS

A-67673

A-67861
S -1525
F-3369

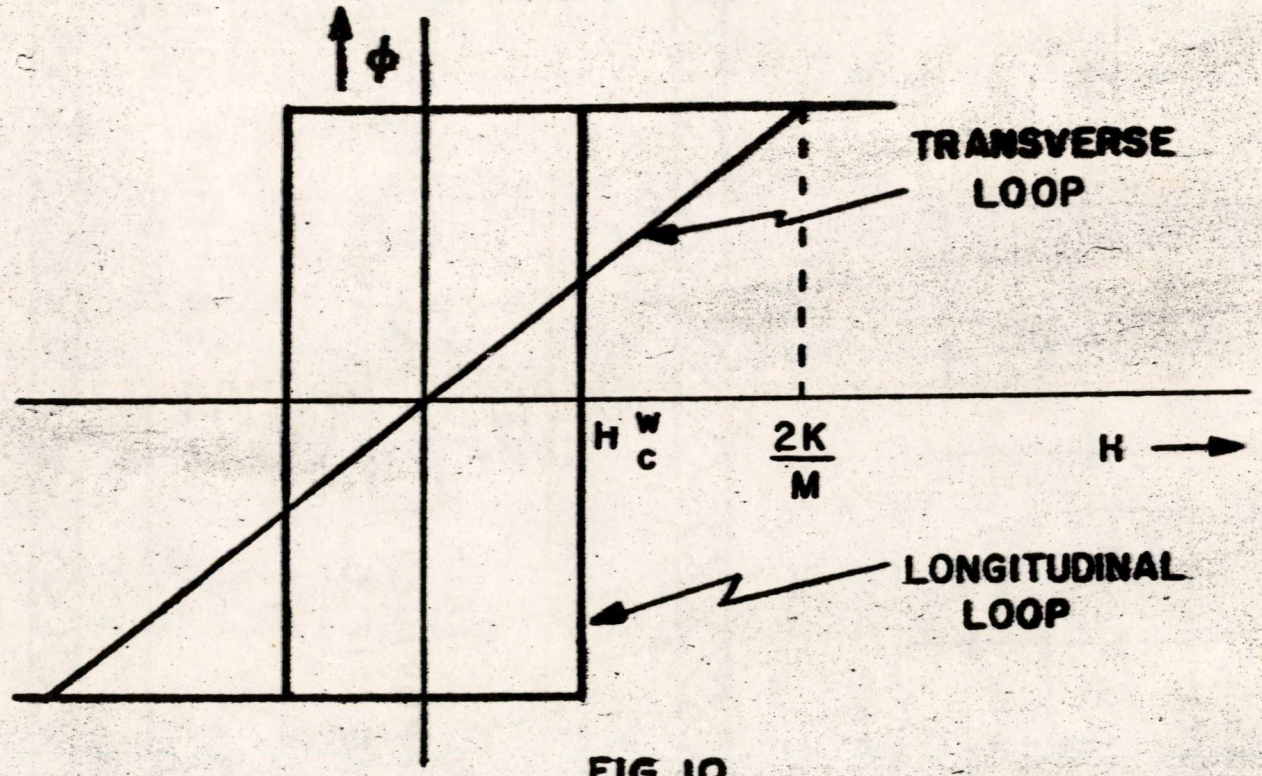


FIG. 10

EXPERIMENTAL HYSTERESIS
LOOPS AT 1000 CPS

A-67669
SN-1523
F-3367

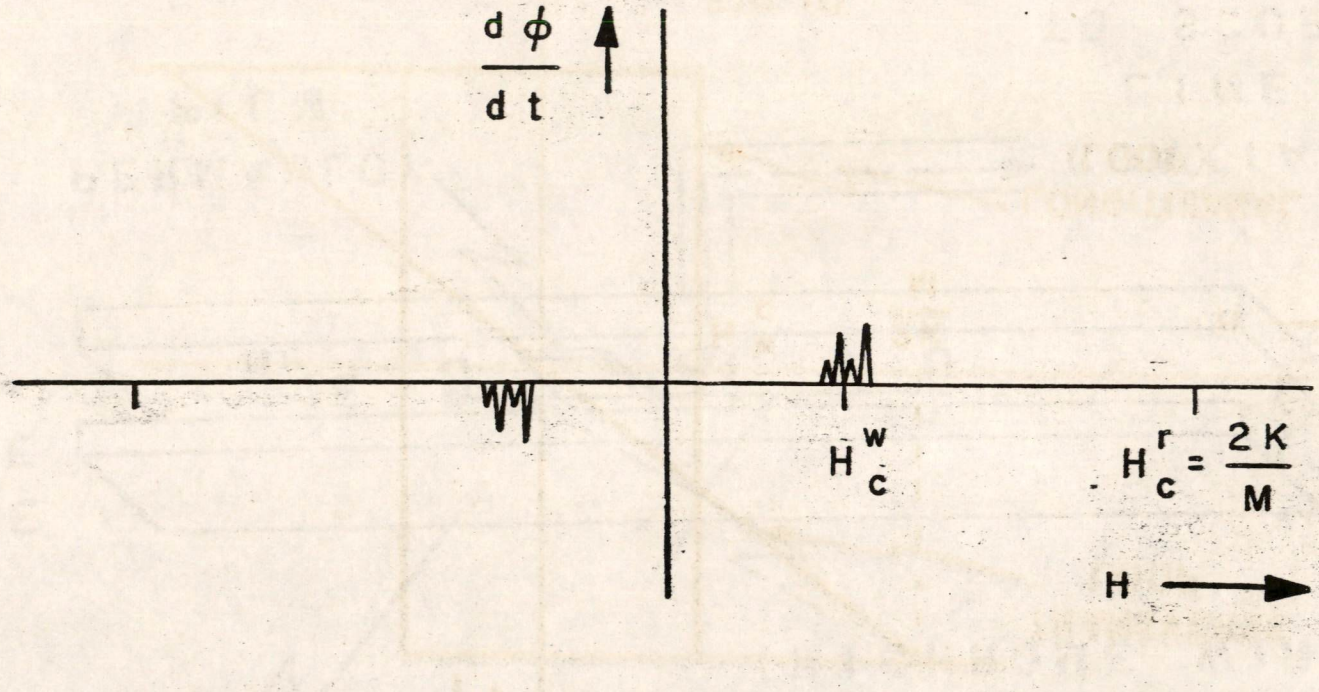


FIG 11

BARKHAUSEN JUMPS IN LONGITUDINAL DIRECTION (10 CPS)

A-67671
SN-1524
F-3368

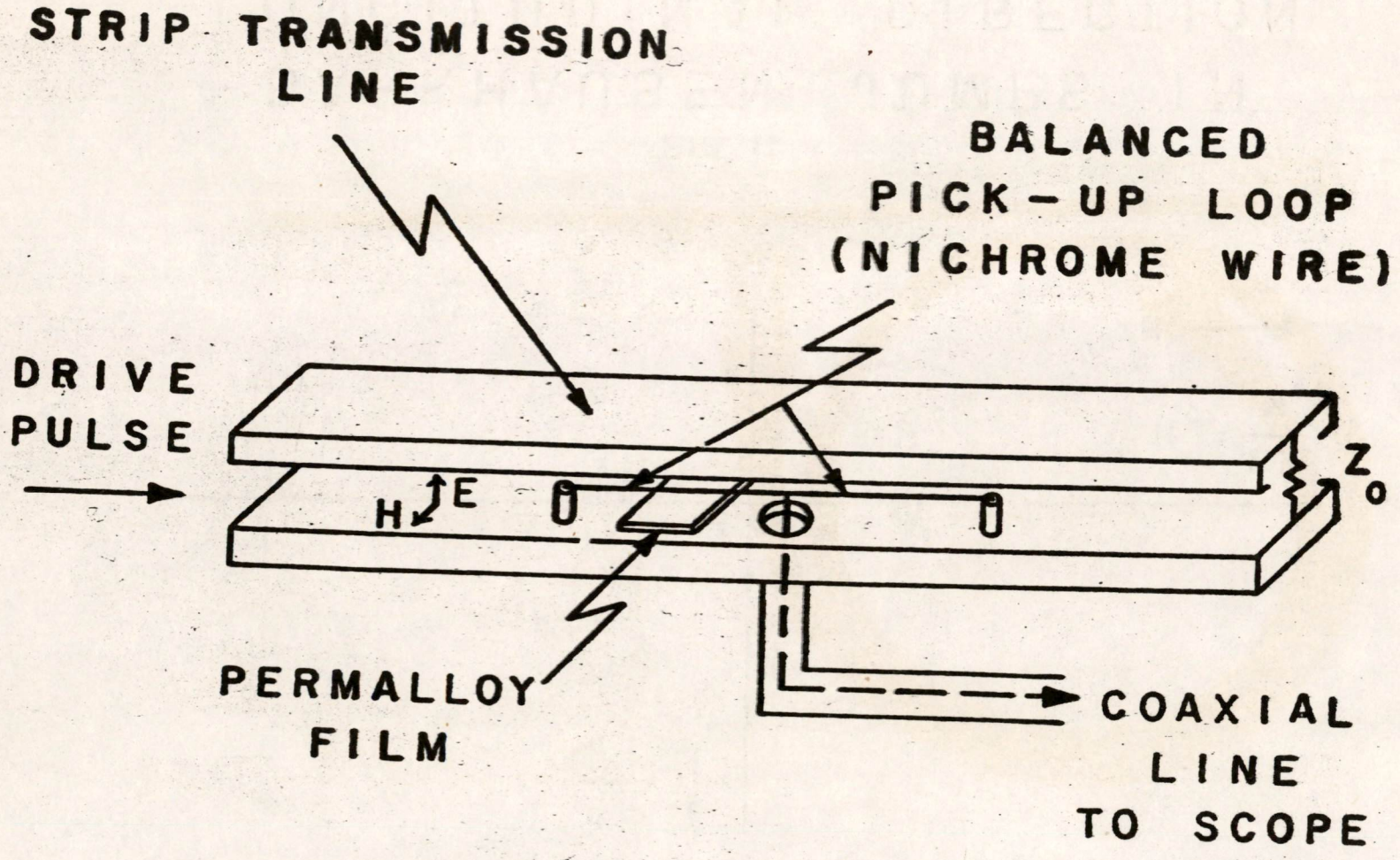


FIG. 12

IMPULSE APPARATUS

A-67913

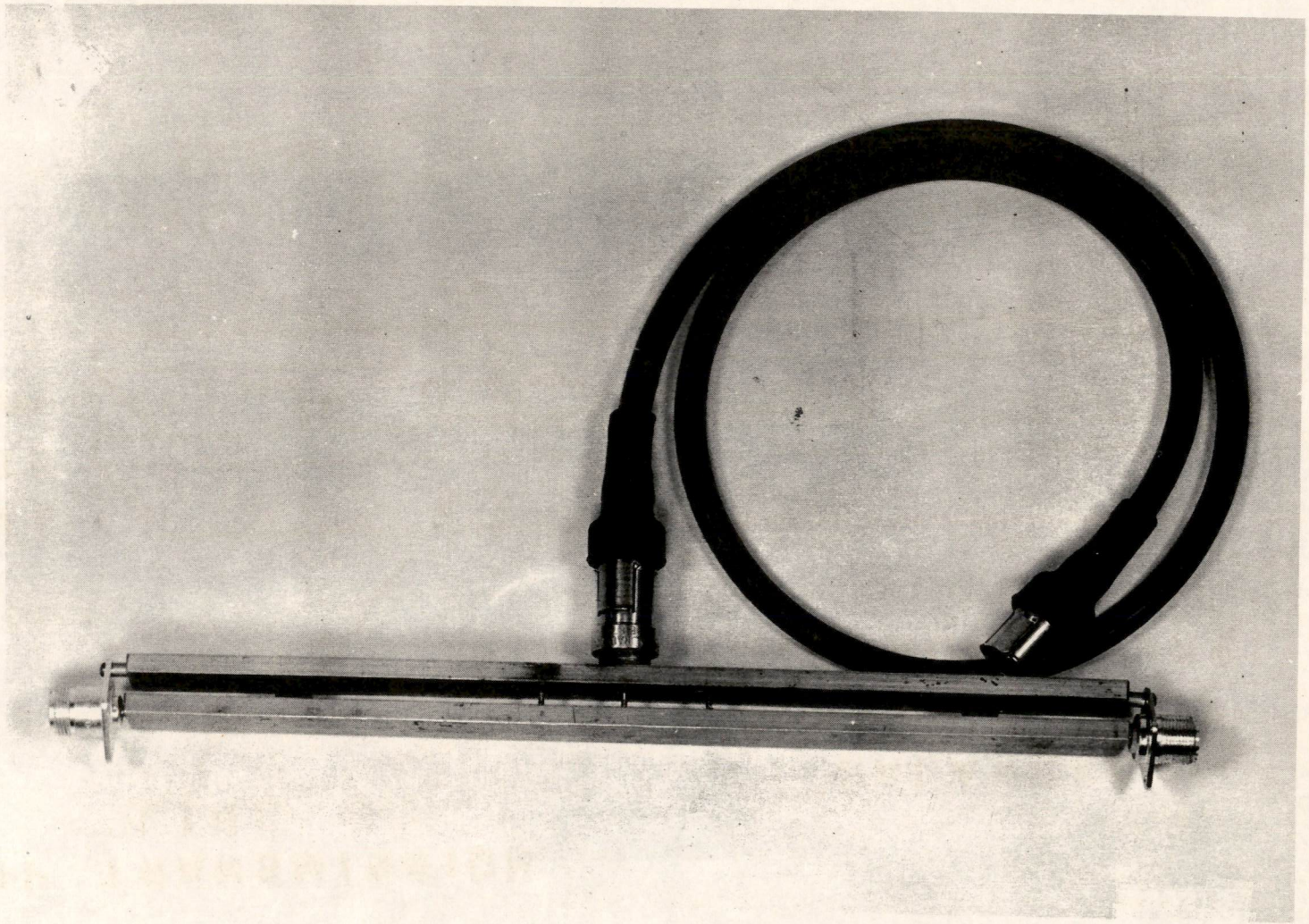


FIG. 13a

PHOTOGRAPH OF STRIP LINE AND PICK-UP LOOP

A-67914

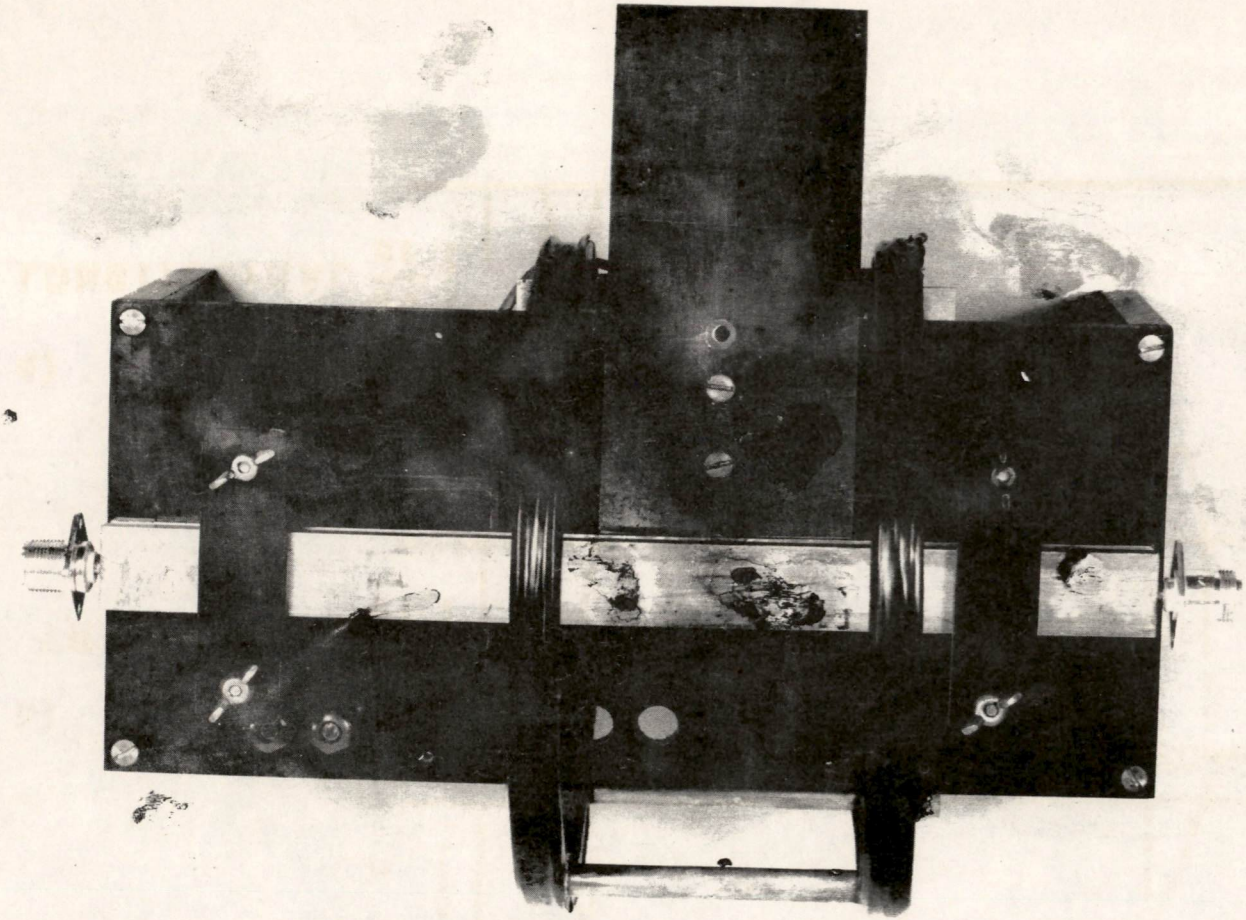


FIG. 13b

PHOTOGRAPH OF STRIP LINE AND $h_\perp$ BIASING COIL

B-67675
SN-1526
F-3370

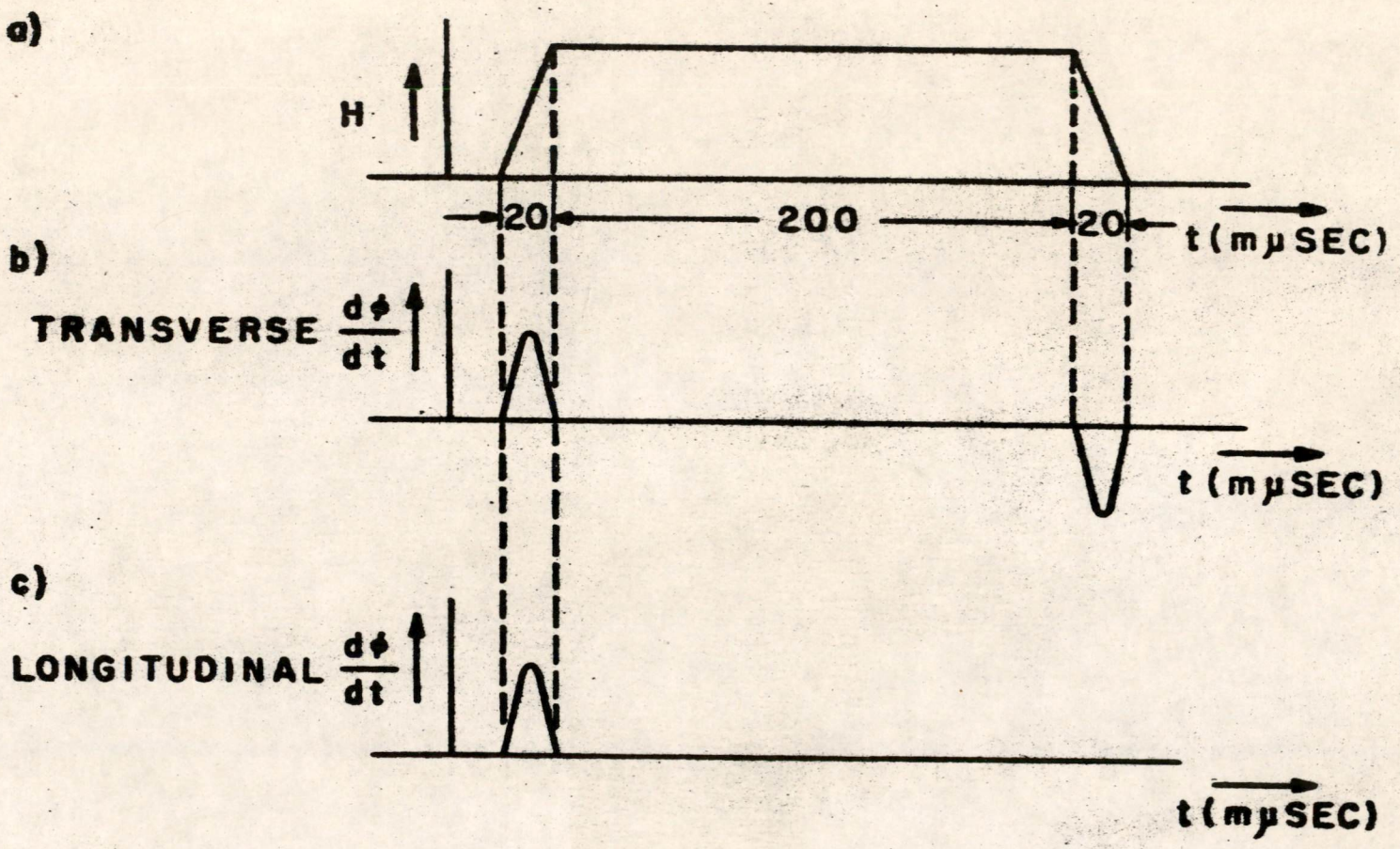


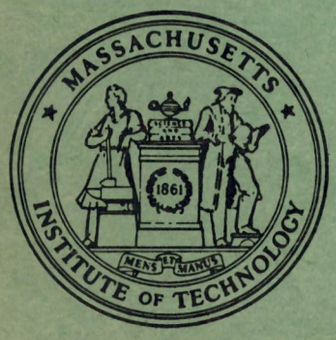
FIG. 14

IMPULSE RELAXATION BEHAVIOR

R-212

FERROELECTRICS FOR DIGITAL INFORMATION STORAGE AND SWITCHING

DUDLEY ALLEN BUCK



DIGITAL COMPUTER LABORATORY

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Report R-212

FERROELECTRICS FOR DIGITAL INFORMATION STORAGE AND SWITCHING

by
Dudley Allen Buck

DIGITAL COMPUTER LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Cambridge 39, Massachusetts

June 5, 1952
(Thesis Date: May 16, 1952)

FOREWORD

This report was originally issued as a thesis report and as such received but limited distribution. So as to extend the distribution to the many who have expressed interest in ferroelectric components for digital information storage and switching, this report is now issued as an M. I. T. Digital Computer Laboratory R-series report.

The author is indebted to Professor Arthur R. von Hippel, Director of the M. I. T. Laboratory for Insulation Research; to Mr. Jay W. Forrester, Director, and Mr. William N. Papian of the M. I. T. Digital Computer Laboratory; and to the staffs of their respective laboratories, whose combined efforts made this work possible.

ABSTRACT

FERROELECTRICS FOR DIGITAL INFORMATION STORAGE AND SWITCHING

by

Dudley Allen Buck

Submitted for the degree of Master of Science

in the

Department of Electrical Engineering

on May 16, 1952

Materials have recently been discovered within which exist domains of permanent electric dipoles. These materials, named ferroelectrics, can be used to advantage in many electronic applications where ferromagnetic materials are currently used, often in circuits which are the duals of those of their ferromagnetic counterparts. Ferroelectrics can be made in the form of single crystals or rugged ceramics.

Digital information can be stored in a matrix of ferroelectric condensers, and an efficient method of storage-element selection is available in the form of a two-coordinate, coincident-voltage scheme. The matrix can be made on a thin ferroelectric sheet by painting the coordinate rows on one side and the coordinate columns on the other. The information can be taken from the matrix via a simple mixing transformer.

Multi-position switching can be accomplished with a group of ferroelectric condensers. The logical circuitry of such a switch, capable of accomplishing many of the switching tasks in a high-speed information-handling system, can be painted directly onto the two sides of a thin ferroelectric ceramic sheet.

Ferroelectrics for pulsed applications are best studied by pulse

methods, which allow their properties to be studied without significant heating of the sample, and with rather low-powered test equipment. A barium titanate ceramic, which, when pulsed, switches in about one microsecond, is on the borderline of suitability for the memory application. The pulsed properties of this material are temperature dependent.

Thesis Supervisor: Arthur R. von Hippel

Title: Director of the M. I. T. Laboratory for Insulation Research

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CHAPTER I

INTRODUCTION TO FERROELECTRICS

Engineers have long utilized the residual induction of a ferromagnetic material for information storage. Such devices as the magnetic-wire and magnetic-tape recorders, the magnetic-drum computer memory, the magnetic stepping register, and more recently, the multi-dimensional magnetic-core memory all depend upon residual induction for their operation. The existence within a material of domains of permanent magnetic dipoles is a requisite for the phenomenon of residual induction.

Recently, materials have been discovered within which domains of permanent electric dipoles exist.[1,2,3] These materials, named ferroelectrics, exhibit residual displacement and have hysteresis loops in the D-E plane similar to those of the ferromagnetic materials in the B-H plane (Figs. 1,2). The residual displacement of ferromagnetic materials is a basis for digital information storage, making possible the use of ferroelectrics in applications similar to those in which ferromagnetic materials are currently used.

The phenomenon of ferroelectricity has been observed in three groups of materials whose representatives are Rochelle salt, dihydrogen potassium phosphate, and barium titanate. It was decided at the outset that the investigations of this thesis should be made on materials of the third group, represented by barium titanate. Barium titanate, unlike the others, can be

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1. A. von Hippel and co-workers, NDRC Reports 14-300 (August, 1944), 14-540 (1945).

2. A. von Hippel, "Ferroelectricity, Domain Structure, and Phase Transitions in Barium Titanate," Laboratory for Insulation Research Technical Report XXVII, Massachusetts Institute of Technology, March 1950; Reviews of Modern Physics, Vol. 22, No. 3, pp 221-237, (July, 1950).

3. W. J. Merz, "The Electric and Optic Behavior of $BaTiO_3$ Single-Crystal Domains," The Physical Review, Vol. 76, No. 8, pp 1221-1225 (October 15, 1949).

prepared in the form of a rugged ceramic which exhibits ferroelectricity over a wide temperature range, and which, when compounded with other titanates, can be tailored to a wide variety of electrical properties.

The remanent charge of a ferroelectric condenser (the residual displacement integrated over the area) is not to be confused with the charge of an ordinary condenser which has been subjected to a direct voltage. The charge of an ordinary condenser will "leak off" with time, whereas the remanent charge of a ferroelectric condenser will remain over a period of weeks even though the condenser terminals are short circuited. The remanent charge of a ferroelectric condenser represents a stable state for the dielectric; for an ordinary condenser, the only stable state is that with zero charge.

Ferroelectrics can be used in circuits which are, in general, the duals of those in which their ferromagnetic counterparts are used. Voltages sources must be substituted for current sources as drivers, and current detectors must be substituted for voltage detectors for observing changes in stored information (Fig. 3).

When a magnetic core, as it switches, moves from a saturated region of its hysteresis loop out onto a steep region and demands power to supply its switching losses, it does so by raising its impedance as seen by the driving winding. For this reason, it is best driven by a current source. A ferroelectric condenser, as it switches, lowers its impedance when it requires more power, and therefore should be driven by a voltage source. If driven by the incorrect source, both the magnetic core and ferroelectric condenser may switch quite slowly, the switching speed being limited by the source and not necessarily by the physical properties of the material.

Information is stored in a magnetic core in the form of remanent flux, either in a positive direction or a negative direction. Changes in the stored information (changes in the flux) manifest themselves as voltages across a winding on the magnetic core. Therefore, a voltage detector is needed to detect information changes in a magnetic-core circuit. A ferroelectric condenser, on the other hand, stores information in the form of a remanent electric charge. Changes in the stored information (changes in the charge) allow currents to flow in the condenser circuit. A current detector is therefore needed to detect information changes in ferroelectrics.

With this dualism in mind, we can explore the possible applications of ferroelectrics to digital information storage and switching circuits which at present involve magnetic cores. Two additional characteristics of ferroelectrics which distinguish them from magnetic cores must be kept in mind:

1. Because Div B = 0, one must provide a closed path for the lines of flux in a magnetic circuit, particularly if one desires a rectangular hysteresis loop. For this reason, magnetic cores in this application are usually made in the shape of rings or toroids. An electric field, however, can terminate on any charge-carrying material; this fact allows ferroelectric condensers to be made in the form of thin sheets with electrodes plated, or fired, on the sides.

Information is ordinarily transferred in a digital information-handling system in the form of electric pulses. With magnetic cores, a transformation between an electric field and a magnetic field must take place when information is being stored and again when it is being read. Ferroelectrics, however, store information in the form of an electric charge; this fact relieves ferroelectrics of the difficulties involved in obtaining flux linkages.

2. During switching from one remanent state to the other, or more simply, when the sign of the remanent flux or charge is being changed, energy is dissipated. On a per-unit-volume basis, ferroelectrics often have an energy loss due to switching more than one hundred times that of the ferromagnetic materials. This poses a heating problem due to switching losses. Fortunately, the thin-sheet fabrication of ferroelectrics facilitates cooling. This large difference in switching loss is illustrated in Table I. Losses for the various materials are computed as twice the product of the remanence times the coercive force, and as such are but approximations.

Table I Loss Comparison

T = 25 C	Material	Approximate Hysteresis Loss Joules /m^3
Ferro-electric	$BaTiO_3$ single crystals[1]	5,000
	$BaTiO_3$ ceramic[2]	15,000
Ferro-magnetic	Deltamax[3]	23
	Silectron[3]	302
	4-79 Molybdenum Permalloy 216[4]	11
	Ferramic[5] (Ferrite) A	36
	B	40
	C	90
	D	21
	E	20
	G	4
	H	4

Key

1. M. I. T. Laboratory for Insulation Research
2. The Glenco Corporation, Metuchen, New Jersey
3. Allegheny Ludlum Corporation, Brackenridge, Pa.
4. ARMCO Steel Corporation, Middletown, Ohio
5. General Ceramics and Steatite Corporation, Keasbey, New Jersey

Both ferromagnetic and ferroelectric materials operate as such only below a certain maximum temperature. This temperature, known as the Curie temperature, or Curie point, is the temperature at which the

dipole domains within the material are no longer able to spontaneously align themselves against the randomizing action of thermal vibrations. At the Curie temperature, the hysteresis loop disappears. For pure barium titanate, the Curie temperature is approximately 120 C, and impurities or additives have been observed to lower it. Most of this thesis investigation was carried out on a barium titanate ceramic body designated "X-18", made by the Glenco Corporation of Metuchen, New Jersey. This body, containing certain additives, was selected because its hysteresis loop is slightly more rectangular than that of ordinary barium titanate ceramics. Because of the additives, the Curie temperature is lower than 120 C (Fig. 2).

The lower Curie temperature of barium titanate is a disadvantage in applications in which the dielectric must exhibit a hysteresis loop during operation, especially in view of the high switching loss which leads to dielectric heating. Long before the Curie temperature is reached, however, many changes occur in the electrical characteristics of barium titanate. These changes with temperature are not very evident from the sequence of hysteresis loops shown in Figure 2, but the tests of Chapter II of this thesis show what a radical effect the temperature can have on the pulsed characteristics of the material. As already mentioned, it is fortunate that the thin sheets of ceramic, as the material is usually fabricated, are in a form which can be easily cooled.

An additional factor to be considered in engineering designs employing ferroelectric ceramics is long-term drift, or aging, of the electrical properties—a problem which is shared by ferromagnetic materials. Rzhanov[4,5] has reported temporary changes in the shape of hysteresis loops

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4. A. V. Rzhanov, Zhur Exsp. Teoret. Fiz. 19,335-45 (1949). Reported in English by reference 5.

5. D. R. Young, "Temporary Enhancement of Hysteresis Loops in Barium Titanate Samples," The Journal of Applied Physics, Vol. 22, No. 4, (April 1951).

due to high-field excitation above the Curie Temperature, followed by a slow drift back to normal with a time-constant of the order of 100 hours. In this thesis investigation, certain ferroelectric condensers were observed to acquire asymetric properties, as though a "built-in" bias were present, upon sitting idle for several days.

Figure 4 shows the samples put to test in the thesis investigation. The various samples are:

A. Glenco body "X-18" — .025" thick, silver paste electrodes.

B. General Ceramics and Steatite body #66431 various sizes and thicknesses, silver paste electrodes.

C. Glenco body "X-18" — .010" thick.

D. Glenco body "X-48" — .010" thick.

E. Body made from Ticon B (Titanium Alloy Manufacturing Company, New York, N. Y.) by the Electrical Ceramics Laboratory of the M. I. T. Laboratory for Insulation Research.

F. Glenco bodies "X-48" and "X-18", .010" thick with evaporated silver electrodes.

In spite of the present limitations of barium titanate ceramics, the use of the material for pulsed operation in digital information-handling systems poses exciting possibilities. As will be shown, circuit components made with barium titanate ceramic promise unique and compact packaging plus very rapid operation. In addition, the material can be easily fabricated and promises to be most inexpensive.

Chapter II of this thesis describes methods, equipment, and the results of pulse tests performed on barium titanate ceramics, while Chapter III describes a proposed ferroelectric two-dimensional matrix memory and Chapter IV describes a multi-position ferroelectric switch.

CHAPTER II

PULSE TESTING OF FERROELECTRICS

A. PULSE METHODS VS. STEADY-STATE METHODS

Dielectrics can be studied by pulse-test methods, by sinusoidal steady-state test methods, or by a combination of the two. In principle, the same information can be obtained from any of these test methods.[6,7,8] Because the comparison of information obtained from one method with that obtained from another is often mathematically difficult, it is usually desirable to test a dielectric by the method most closely approximating the conditions under which that dielectric will be called upon to operate. Ferroelectrics for digital information storage and switching will probably be pulse-operated. Pulse testing, therefore, naturally suggested itself as the proper method for evaluating ferroelectric materials for use in these applications. The application was the prime factor in the selection of the test method.

Pulse testing has at least three additional advantages over the other test methods:

1. Between pulses, an arbitrary length of time can be allowed for cooling of the dielectric. Although switching power is high during a pulse, a pulse-repetition frequency can be chosen which is low enough that heating of the dielectric is negligible. The minimization of heating during the experiment is especially important for the barium titanate ceramics which were studied because their electrical properties vary remarkably with

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6. B. Gross, "On the Theory of Dielectric Loss," The Physical Review, Vol. 59 p. 748, (May 1, 1941).

7. M. F. Manning and M. E. Bell, "Dielectric Theory and Insulation," Reviews of Modern Physics, Vol. 12, p. 215, (1940).

8. Unpublished papers of Professor A. R. von Hippel, Laboratory for Insulation Research, Massachusetts Institute of Technology, Cambridge, Massachusetts

temperature. During the course of the thesis it was suggested that the high-field-strength relaxation spectrum (plot of dielectric constant versus frequency) as obtained from steady-state measurements be compared with the relaxation spectrum as computed from pulse measurements. It was concluded that heating of the dielectric would prohibit high-field-strength steady-state measurements. In fact, the small condenser shown at A in Figure 4 (1-square-centimeter electrodes on the two sides of a 0.025-inch sheet) would dissipate over 1,000 watts in a field of 8.2 volts per mil at 10^6 cycles per second--providing that it remained at room temperature. It would be difficult, if not impossible, to control the temperature while making a measurement of the dielectric constant. In addition, there would be driving difficulties. This brings up the second point.

2. Pulse-test equipment also can rest between pulses. Although the equipment must be capable of supplying the peak power demanded by a ferroelectric sample as it switches, the average power can be quite low. Large pulse energies can therefore be supplied to a sample with rather modest equipment.

3. Breakdown of the dielectric caused by heating (such breakdown is believed to occur in many dielectrics) is prevented by the use of pulses so short that the dielectric does not overheat. Elimination of thermal breakdown as a cause for failure of the dielectric then allows pulse voltage amplitudes to be applied which exceed the steady-state breakdown voltage of the dielectric. Pulse measurements can thus be extended into a region not accessible to steady-state measurements.

B. PULSE TESTS OF THIS THESIS

In the pulse tests a ferroelectric condenser is subjected to voltage pulses of adjustable amplitude and of either polarity in a meaningful sequence. Two sequences were chosen for the tests (Figure 5). The first,

designated Mode A, was designed to study the switching speed and the switching losses of a ferroelectric. The second, designated Mode B, was designed to evaluate various ferroelectric materials for use in the two-dimensional ferroelectric memory described in Chapter III of this thesis.

Almost as important as the results of a test is a careful description of the techniques and equipment employed, with special attention to the limitations of the equipment. All too often important effects are masked or blurred by inadequate amplifier bandwidths, and anomalies are introduced which are peculiar to a particular testing sequence. Therefore, before a discussion of the results of these tests, a description of the tests and of the equipment will be given.

1. Mode A Tests

Mode A tests subject a ferroelectric condenser to a pulse sequence consisting of four positive pulses followed by four negative pulses. The first positive pulse and the first negative pulse reverse the polarity of the remanent charge, thereby switching the ferroelectric and producing a switching transient. The remaining three positive pulses and the remaining three negative pulses find the material already switched, and thus they produce non-switching transients. In computer terminology the switching transient is called a ONE, while the non-switching transient is called a ZERO. In addition, the positive pulses are arbitrarily called WRITE pulses and the negative pulses are called READ pulses. The significance of these terms will become clearer during the discussion of information storage in Chapter III. For the present, it will be sufficient to make the observation that a WRITE pulse will result in a ONE transient if preceded by a READ pulse and a ZERO transient if preceded by a WRITE pulse, while a READ pulse will result in a ONE transient if preceded by a WRITE pulse, and a

ZERO transient if preceded by a READ pulse. The pulse sequence and resulting transient sequence can then be written (Table II) for Mode A tests. (The ONE and ZERO are qualified by the word UNDISTURBED, the reason for which will be given in the next section.)

Table II Mode A Test Sequence	
Pulse	Transient
1. WRITE	UNDISTURBED ONE
2. WRITE	UNDISTURBED ZERO
3. WRITE	UNDISTURBED ZERO
4. WRITE	UNDISTURBED ZERO
5. READ	UNDISTURBED ONE
6. READ	UNDISTURBED ZERO
7. READ	UNDISTURBED ZERO
8. READ	UNDISTURBED ZERO
etc.	

2. Mode B Tests

Mode B tests subject a ferroelectric condenser to a sequence of positive and negative pulses of two amplitudes. The larger amplitude pulses are called WRITE pulses if positive and READ pulses if negative, just as in Mode A tests. The pulses of lesser amplitude are called + DISTURB if positive and —DISTURB if negative. These disturbing pulses are inserted between a WRITE and a READ pulse to test the ability of a ferroelectric condenser to retain a remanent charge under the operating conditions to which it would be subjected in the ferroelectric matrix memory described in Chapter III. Further discussion of Mode B tests along with the results of Mode B tests follow the memory discussion in Chapter III. For the present, it will be sufficient to define a DISTURBED ONE as the transient associated with a READ pulse which follows a WRITE pulse if one or more —DISTURB pulses have been inserted between the WRITE pulse and the READ pulse. The pulse sequence and resulting transient sequence can

then be written for Mode B tests (Table III).

Table III Mode B Test Sequence

Pulse	Transient
1. WRITE	UNDISTURBED ONE
2. WRITE	UNDISTURBED ZERO
3. WRITE	UNDISTURBED ZERO
4. + DISTURB	+ DISTURB TRANSIENT
5. −DISTURB	−DISTURB TRANSIENT
6. −DISTURB	−DISTURB TRANSIENT
7. −DISTURB	−DISTURB TRANSIENT
8. READ	DISTURBED ONE
etc.	

C. EQUIPMENT

1. The Ferroelectric Pulse Tester

The basic ferroelectric pulse-test circuit is shown in Figure 7A. A large condenser is used as the voltage source, and a thyratron is used as the switch. A small series resistance allows the transient current to be measured, and a large resistance in parallel with the ferroelectric condenser under test allows the circuit to stabilize after the thyratron is extinguished, with zero volts across that condenser.

The large condenser is chosen with sufficient capacity so that it loses but a small part of its charge, and therefore but a small part of its voltage, during the pulse (Figure 7B). The thyratron plate drops to V_t when the thyratron fires (Figure 7C). The voltage which is applied to the condenser under test is the difference between the voltage across the large condenser and the voltage across the thyratron and small resistance. (Figure 7D).

Figure 8 is a block diagram showing the way in which the sequences of pulses are generated. A low-frequency pulse generator operates an electronic counter which counts up to four. On every count, the oscilloscope

is triggered and, after a short delay, the thyratron switch is fired. On the count of zero the polarity of the condenser under test is reversed. If making Mode B tests, the voltage is changed from the read-write voltage to the disturb voltage, or vice-versa, on the count of three. The thyratron switch is extinguished a short time after it is fired.

Figure 9 is a circuit schematic of the ferroelectric pulse tester. The polarity-reversing switch and the voltage-selection switch consist of relays actuated by thyratron flip-flops. The thyratron switch is fired by a positive pulse on its grid, in the usual fashion, and it is extinguished by a second positive pulse on the same grid. It was noticed that when a capacitively leaded thyratron is operating in the low-current region (close to minimum current) it may be extinguished by a positive grid pulse. This phenomenon was not found in the literature. The following explanation is thought to describe what takes place: The plate is held at V_t, the thyratron voltage drop, during the grid pulse. The grid pulse, which drives the grid more positive than the plate, causes the space charge to drain off onto the grid, thereby deionizing the discharge region. The grid then starts negative and is able to reach its negative bias voltage before the tube can refire, because firing is very slow at such a low plate voltage. Once the thyratron is extinguished, the plate voltage rises exponentially to the read-write voltage or disturb voltage, whichever happens to be selected.

The rise time of the voltage step applied to the sample under test is approximately 0.1 microsecond, and a pulse length of 100 microseconds is commonly used in the tests. Although the pulse has a short rise time, it has a fall time-constant of about 100 microseconds. A pulse-repetition frequency of 70 per second was used.

The method described for extinguishing the thyratron switch has the rather fortunate advantage that the extinguishing pulse does not show up

to any extent across the sample under test. All other methods for extinguishing the thyratron which were considered consisted of driving the plate negative with respect to the cathode, resulting in an unwanted extra pulse across the sample in the same direction as the first pulse.

The large resistor in parallel with the sample under test (Figure 9) is made with three identical resistors in series. Coupled directly to the oscilloscope vertical deflection plates, these serve as a voltage divider of the proper size to permit observation of the applied voltage step.

2. The Oscilloscope

The oscilloscope used throughout the thesis investigation was a Browning Model OL-15A (Serial #41). Waveforms of voltages applied to the various ferroelectric samples were observed by directly coupling these voltages into the vertical deflection plates, whose measured deflection sensitivity is 67 volts per inch. Switching waveforms were observed using the vertical amplifier, whose maximum deflection sensitivity is 0.14 volts per inch and whose frequency response is flat within $\pm$ 10% from 20 cycles per second to 4 megacycles per second. Voltage measurements, when the amplifier was being used, were made by comparison with a built-in calibration voltage which is direct reading in peak-to-peak volts. Switching-time observations were made using a driven (triggered) sweep whose measured sweep speeds are 0.45, 0.96 and 4.8 microseconds per inch.

3. The Sample Holder; Temperature Measurement and Control Apparatus

Figure 10 is a photograph of a ferroelectric sample being tested. The sample is mounted in a holder and submerged in Dow 550 fluid (Lot BB-86), a Silicone oil. All measurements versus temperature were taken with falling temperature starting at 125 C. A mercury thermometer was used for temperatures about 0 C and a pentane thermometer below 0 C. Dry ice was added to the oil in chuncks whenever measurements were made below room temperature.

D. RESULTS OF MODE A TESTS

As already mentioned, the results of Mode B tests are deferred until Chapter III because Mode B tests are so intimately connected with the ferroelectric matrix memory. Here, the results of Mode A tests are discussed.

With a given condenser in the sample holder, two parameters were variable in the experiments:

1. Pulse amplitude
2. Temperature

Measurements were made as a function of one of these two variables with the other held constant. Figures 11, 12, and 13 are photographs of the switching transients at constant pulse amplitude (8.2 volts per mil). They are included as an example of the many runs made, so as to show the approximate shape of the switching transients and the remarkable temperature dependence of the transient shapes. The two lines in each photograph are actually the result of the eight traces of the Mode A. test superimposed. The current is measured at a point in the circuit at which it is always of the same polarity. Two UNDISTURBED ONE's merge in the larger of the two transients, and six UNDISTURBED ZERO's in the smaller for every major cycle of eight pulses.

Because the applied pulse is a constant-voltage pulse, the area under these transients has the dimension of energy. The area under the larger transient is a measure of the energy associated with the ferroelectric condenser switching, while the energy under the smaller transient is the non-switching energy.

The difference in area between the switching transient and the non-switching transient is what we shall here define as the dielectric switching loss. This area, as shown in Chapter III, is somewhat related to our ability to discriminate between the switching transient and the non-switching transient.

1. Dielectric Switching Loss as a Function of Temperature at Constant Pulse Amplitude

With the difference of these two areas taken as a measure of the dielectric switching loss, this loss is plotted as a function of temperature for Glenco body "X-18" (Figure 14) at three pulse amplitudes. The loss is divided by the volume of the sample used so as to yield joules per cubic meter. As can be seen, the switching loss varies with temperature. It is roughly constant in the region between -30 C and room temperature, at which point it drops off. At about 70 C it reaches a second, smaller peak and then goes to zero at the Curie temperature.

It is interesting to note that approximately the same dipping curve of loss versus temperature has been observed with stead-state loss-tangent measurements at moderately high field strengths. Such a curve has been included (Figure 15) for comparison.

The hysteresis loops at various temperatures of Figure 2, taken at 250 cycles per second for the same material, do not seem to show this dipping curve. This points up the fact that hysteresis loops can be used only as a rough indication as to the probable pulsed characteristics of a material. Vertical movements on the hysteresis loop are made up of a combination of reversible and irreversible changes. One does not know at any instant of time what portion of the integrated changes up to that time are reversible and what portion are irreversible; from an arbitrary point on the hysteresis loop, one does not know in advance what the exact path of the trace would be if the field were suddenly removed. Since it is the irreversible changes which contribute to the loss, the poor correlation between quasi-static hysteresis loops and the pulsed characteristics is understandable.

2. Approximate Switching Time as a Function of Pulse Amplitude at Constant Temperature

Of concern to the engineer who is to use ferroelectrics in pulse-operated circuits is the speed with which they can be switched. The switching

speed has been observed to be a function of the amplitude of the applied pulse. Figure 16 is a plot of switching speed versus pulse amplitude for a piece of Glenco body "X-18" barium titanate ceramic 0.025-inch thick with 0.006-square-inch silver-paste electrodes fired on opposite sides. The pulse amplitude has been converted to volts per mil (1 mil = 0.001 inch) rather than MKS units because thin barium titanate ceramic sheets are spoken of as being "so many mils" thick, not only by the manufacturers, but also by nearly all users. Included in Figure 16 is a plot of the approximate length of the non-switching transient.

It is difficult to define switching time; hence, the qualification "approximate". In the data presented in Figure 16, the switching time is defined as that time required for the transient to fall from its peak amplitude to 10% of its peak amplitude. The 10% level would correspond to 2.3 time-constants if the transient decayed exponentially, and we could then say that the transient is substantially over at about twice the switching time of Figure 16, five time-constants being the usual allowance. The transient is far from being exponential in shape, however. On tracing paper, exponentials of various time-constants were drawn whose initial amplitudes corresponded to the initial height of the transients in the photographs of Figures 11, 12, and 13. An attempt was then made to match up each transient with the exponential most closely resembling that transient, but with little success. It was concluded that all switching-time definitions were equally poor but that a consistent definition allowed a plot to be made which at least indicates the order of magnitude of switching times, and which in the case of this barium titanate ceramic shows that it indeed switches rapidly enough for our present applications.

For high pulse amplitudes, Figure 16 shows that switching time seems to asymptotically approach a lower limit in the region of 0.25 microseconds.

Low-field-strength bridge measurements indicate a drop-off of the dielectric constant of barium titanate between 10^8 and 10^{10} cycles per second. This would predict a much faster switching time than that observed. The measurements strongly suggest that switching of the dielectric involves a much slower mechanism than the one studied with low-field-strength bridge measurements.

3. Approximate Switching Time as a Function of Temperature at Constant Pulse Amplitude

A glance through the sequence of photographs of Figures 11, 12, and 13 will show that at a constant pulse amplitude the shapes of the transients vary with temperature. An attempt has been made, once again, to define a switching time so as to measure to some extent the change in the transient waveshape with temperature. Figure 17 is a plot of switching time versus temperature at two pulse amplitudes for a piece of Glenco body "X-18" 0.025-inch thick with 0.015-square-inch silver-paste electrodes fired on opposite sides. The data were taken from two of the runs of photographs. The two dotted regions are where the complete transient did not get in the picture. The plot gives a rough indication as to the temperature variance of switching time.

CHAPTER III

THE FERROELECTRIC MEMORY

Figure 19 is a photograph of a 64-cell ferroelectric memory. The part which actually stores information is the one-inch square of thin barium titanate ceramic on the top shelf. The compactness and simplicity of a ferroelectric memory along with the promise of high operating speed was the prime motivation behind this research. In the following paragraphs, it will be shown how information can be stored in ferroelectrics, why this particular design was chosen, how the matrix memory works, and how well it might work. It must be said parenthetically that the memory shown in Figure 19 does not actually work, but that a material has been uncovered which is on the borderline of suitability for the application. The batch of material from which the memory of Figure 19 was made later turned out to have electrical properties inferior to those of previous samples of the same material.

A. INFORMATION STORAGE IN FERROELECTRICS

Digital information, when presented in binary form, consists of a group of elementary yes or no answers, commonly called ONE's and ZERO's, which can be stored in a group of bi-remanent devices. A ferroelectric condenser is one such device, the remanent charge having always one of two polarities. We can arbitrarily define a positive remanent charge as a ONE and a negative remanent charge as a ZERO. We then can say that a ferroelectric condenser "remembers" a ONE or a ZERO which has been placed in it. To recover the stored information--that is, to read the bi-remanent storage device--we have merely to apply a reference pulse and then observe the nature of the resulting transient. Let us arbitrarily say that the reference pulse, or READ pulse, is negative. If the condenser contains a

ONE, we will observe a switching transient (undisturbed ONE) when the reference pulse is applied. If, on the other hand, the condenser contains a ZERO, we will observe a non-switching transient (undisturbed ZERO). The ability of a given ferroelectric condenser to store information, therefore, depends upon our ability to discriminate between these two kinds of transients. This we can do.

Application of a READ pulse to a ferroelectric condenser leaves that condenser in the same remanent state (containing a ZERO) regardless of whether it contained, just prior to application of the READ pulse, a ONE or a ZERO. The information is therefore destroyed during reading. A memory which is read in this way is said to have a destructive read. We must replace the information by re-writing. This is accomplished by following each ONE transient by a WRITE pulse.

B. SELECTION OF MATRIX LAYOUT FOR MEMORY

Having a method for storing and reading information, however, is but the first step in the design of a working memory. It has become increasingly clear as digital information handling systems have developed that the most difficult problem for which to find an economical solution is that of selecting among the storage cells of a memory. Certain of the completed memories have found their solution in making time one of the coordinates in the selection of memory cells. The mercury-delay-line and the magnetic-drum memories fall into this category. For the attainment of truly high-speed operation, however, a random-access memory in which time is not one of the selection coordinates is felt to be necessary. The electrostatic storage tube as used in the Whirlwind computer is one of the few working memories to fall into this latter category.

The possibility of locating the storage elements in a multi-dimensional matrix where selection is inherent in the storage elements

themselves is a recent and most promising scheme for solving the selection problem.[9,10] This basic idea is being investigated for ferromagnetic storage using a matrix of small toroids at the M. I. T. Digital Computer Laboratory. It will now be shown how the same basic idea can be used for ferroelectric materials, as first suggested by Jay W. Forrester. The three-to-one selection scheme to be described was the outgrowth of work done by R. R. Everett.[11]

C. DESCRIPTION OF THE MATRIX MEMORY

An economical method for selection among N objects is to arrange them in a square matrix so that by the selection of one row and one column the object at the intersection of that row and column is selected. The selection problem is at once reduced from selection among N objects to the problem of making 2 selections, each from among N objects -- one to find the proper row and one to find the proper column. How this method can be used to select among the storage elements of a memory, which in this case are ferroelectric condensers, will now be shown.

Consider the square n-by-n matrix of ferroelectric condensers shown in Fig. 21a. Having selected a single row and a single column, one may redraw the matrix as it is seen looking between this row and column. As can be seen (Fig. 21b), the selected condenser lies between the selected row and the selected column. In addition, condensers connect the selected row to each of the unused columns and the selected column to each of unused rows. Finally, there is a condenser between each unused row and each

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9. Jay W. Forrester, "Digital Information in Three Dimensions Using Magnetic Cores", Project Whirlwind Report R-187, (September 8, 1950), M.I.T. Servomechanisms Laboratory.

10. W. N. Papian, "A Coincident-Current Magnetic Memory Unit", Project Whirlwind Report R-192, (September 8, 1950), M.I.T. Servomechanisms Laboratory.

11. R. R. Everett, "Selection Systems for Magnetic Core Storage", Project Whirlwind Engineering Note E-413, (August 7, 1951), M.I.T. Servomechanisms Laboratory.

unused column.

Regardless of what voltages are applied to the selected row and the selected column, the unused rows will all be, by symmetry, at the same potential, and the unused columns will likewise be at the same potential. We can therefore, for this analysis, join the unused rows and sum the parallel condensers (Fig. 21c). Similarly, we can join the unused columns. We now see that a voltage applied between the selected row and the selected column will be directly across the selected condenser. In addition, this voltage will split among the three summed condensers, giving each of them a lesser voltage. The greatest of these lesser voltages is defined as the disturbing voltage, and the ratio of the voltage on the selected condenser to the disturbing voltage is defined as the selection ratio.

The summed condenser which joins the unused columns and the unused rows is n-1 times as large as the other two summed condensers. If the unused rows and unused columns are left floating (Fig. 22a), a voltage appears across this large condenser equal to $1/(2n-1)$ of the voltage across the selected condenser. Across the smaller summed condensers a voltage equal to $(n-1)/(2n-1)$ of the voltage across the selected condenser appears. Thus the selection ratio is $1 : (n-1)/(2n-1)$. For a 2 by 2 matrix, the ratio becomes 1 : 1/3 (three-to-one), and as n becomes large the ratio rapidly approaches 1 : 1/2 (two-to-one). This is illustrated by the Table IV.

Table IV Selection Ratio vs Matrix Size

MATRIX SIZE	SELECTION RATIO
2 x 2	3.00 : 1
3 x 3	2.50 : 1
4 x 4	2.33 : 1
5 x 5	2.25 : 1
6 x 6	2.20 : 1
7 x 7	2.17 : 1
8 x 8	2.14 : 1
16 x 16	2.07 : 1
∞ x ∞	2.00 : 1

Grounding the unused rows and unused columns (Fig. 22b) causes zero voltage to appear across the large condenser and a voltage of one-half to appear across the small condensers. The selection ratio is always 2 : 1 with this scheme regardless of the size of the matrix.

Presumable we would always be somewhere between these two cases, depending upon the internal resistance of the source used to apply voltage to the leads. For a matrix of size 16 by 16, the first scheme gives a selection ratio of $2\frac{1}{15}$: 1 and the second a ratio of 2 : 1, a difference of 3%. It therefore appears that the internal resistance of the voltage source has little effect upon the operation of the matrix for sizes which at present seem to be desirable.

A third scheme for driving the matrix appears to be promising. Instead of letting the unused rows and columns float or be grounded, the selection ratio can be improved by <u>driving</u> the unused rows and columns to voltages such that the voltage across the large summed condenser just equals the voltage across each of the smaller summed condensers (Fig. 22c). Although this scheme involves additional driving problems, it makes the selection ratio 3 : 1 regardless of the matrix size. This means that the hysteresis loop of the ferroelectric material need only be capable of discriminating between two voltages which bear a three-to-one relationship to each other.

Selection of a row and a column allows us to apply a READ or WRITE voltage to one condenser in the matrix while applying a lesser DISTURB voltage to other condensers in the matrix. Figure 20 illustrates the requirements placed on the hysteresis loop by this type of operation. The elementary ferroelectric condenser in the matrix must be able to switch when a READ pulse or a WRITE pulse is applied. At the same time it must be able to retain substantially all of its remanent charge during the application of

a large number of DISTURB pulses. The tests described, designated as Mode B, were specifically designed to test a material for this application.

D. MODE B TESTS

As already mentioned, our ability to read information out of a memory is the true measure of the memory's ability to retain information. If the memory, under a large number of disturbances, loses most of its remanent charge and yet we are able to reliably determine the algebraic sign of what little remains, we may have a working memory. It has been the observation thus far, however, that our ability to read out of the memory, that is, to discriminate between the two kinds of transients, is the weak link in the system. On a peak-amplitude basis, discrimination is completely out of the question (glance at photographs in Figs. 11, 12, 13). A more fundamental basis for discrimination is a comparison of the areas under the two transients, such as an integrator would see. Figure 24 is a plot of this area ratio versus temperature for Mode A operation (no disturbances) at 8.2 volts per mil for Glenco "X-18" barium titanate ceramic. The four-to-one area ratio is just barely usable for reliable discrimination. When disturbances are inserted between WRITE and READ, however, this ratio falls to a low value, defying discrimination.

As we look at the transients in search of a means to discriminate between them, we notice that the most striking difference is in their waveforms. There is a time, about a microsecond or so after the waveform starts, when the non-switching transient has dropped almost to zero and the switching transient, due to its slowness, still has considerable amplitude. If the waveform is sampled at a time when the amplitude ratio between the two transients is a maximum, good discrimination is possible.

The problem of detecting the current transient on the selected

row (or column) of a matrix is nicely handled by transformer coupling. Using single-turn coupling, wires to all of the rows can be threaded through a ring-shaped magnetic core (Fig. 25C lower). A secondary winding can then be coupled into a sensing circuit. If half of the wires are threaded through in one direction and half in the other direction, the small unwanted transients on the unused rows will tend to cancel. With this latter arrangement, however, the sensing amplifier must be prepared to look at either a positive-going waveform or a negative-going waveform due to the transient in the selected row.

The upper nine photographs (3 x 3 matrix) of Figure 25A is an introduction to the Mode B measurements. The left-hand column are Mode A waveforms for a 100-volt READ-WRITE pulse. The pulse itself is shown in the top row, the transient as seen across a resistor in the middle row, and the transient as seen when transformer-coupled in the bottom row. The middle column is an identical sequence for a 50-volt DISTURB pulse, once again Mode A. The right-hand column is the 100-volt READ-WRITE pulse and the 50-volt disturb pulse superimposed in a Mode B test. The details of the transformer coupling is shown in the upper part of Figure 25C. The sample used in these tests is a piece of Glenco body "X-18".

The lower photographs of Figure 25A illustrate the time-amplitude discrimination principle. Due to transformer coupling, the UNDISTURBED ONE and DISTURBED ONE are of opposite polarities.

Figure 25B is a sequence of photographs showing the drop in amplitude of a DISTURBED ONE as the amplitude of DISTURB pulses is increased. The READ-WRITE voltage is held constant. It can be seen that with this material a 3 : 1 selection ratio will allow discrimination whereas a 2 : 1 selection ratio will not.

It was found that most of the loss of amplitude is due to the

first DISTURB pulse. All changes in charge due to DISTURB pulses are either of a reversible or an irreversible nature. Those of an irreversible nature cause the remenant charge to diminish, while those of a reversible nature cause no loss of remanant charge. It appears as if the first DISTURB pulse "uses up" all, or nearly all, of the irreversible changes so that subsequent DISTURB pulses cause little or no further diminution. To test this hypothesis, the Mode B test was temporarily modified to give twice as many DISTURB pulses. The change in the DISTURB ONE waveshape when this change was made was less than the width of the scope trace.

CHAPTER IV

THE FERROELECTRIC SWITCH

A multi-position ferroelectric switch is proposed which can accomplish many of the switching tasks in an information handling system; in particular, it can select among the rows and columns of a ferroelectric memory. The logical circuitry of the ferroelectric switch can be painted directly onto the two sides of a thin ferroelectric sheet.

The non-linear electric displacement-versus-field characteristics of a ferroelectric can be utilized to construct a condenser whose capacitance is a function of the applied voltage. This phenomenon, which makes possible the operation of a dielectric amplifier,[12,13] is the basis for the ferroelectric switch. Figure 26 illustrates the operation of the basic switch element--a simple R-C filter which uses a non-linear condenser as its series branch. With no direct voltage across the condenser (Fig. 26A), the circuit behaves like any ordinary π-section R-C filter with the exception that distortion will result if the input voltage is large enough to drive the dielectric out of its linear region. Transfer characteristics are shown for simusoidal excitation. If a bias voltage V_c is inserted in the circuit as shown (Fig. 26B), the operating point for the transfer characteristics is shifted to a new point on the charge-versus-voltage characteristics of the non-linear condenser. At this new point, the condenser has a much lower capacity and, therefore, the filter characteristics are changed in such a way that the output

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12. Shepard Roberts, Barium Titanate and Barium-Strontium Titanate as Non-Linear Dielectrics, M.I.T. Sc.D. Thesis, Department of Electrical Engineering (1946).

13. Development and Application of Barium Titanate Ceramics as Non-Linear Circuit Elements, Final Report Contract No. W36-039 sc-44606 File No. 19028-PH-49-5(4060) Glenco Corporation (August 15, 1950).

diminishes in amplitude. With a fixed-amplitude input voltage, then, the output voltage can be changed by varying the bias voltage V_c. For ferroelectric switch operation, we need but two values for V_c: when $V_c = 0$ the switch is ON, and when V_c is equal to some fixed value high enough to bias the dielectric well into its saturation region, the switch is OFF.

Figure 27A illustrates a two-position ferroelectric switch. The two non-linear condensers are made as a single unit by firing a large electrode on one side of a ferroelectric sheet and two smaller electrodes on the opposite side. With S in position shown, output 2 is biased OFF, and output 1 is ON. In the opposite position, output 2 is ON.

Figure 27B illustrates an eight-position ferroelectric switch. Operation of the first stage, controlled by S_1, is the same as the two-position switch. Subsequent stages, however, have the lower ends of their resistors connected so that the even resistors are connected to ground when the odd resistors are connected to V_c, and the even resistors are connected to V_c when the odd resistors are connected to ground. There are eight possible paths through the switch (Fig. 28) only one of which will have all of its condensers ON. With S_1, S_2, and S_3 of the eight-position switch set as shown, output zero is ON. Outputs 1, 3, and 7 have one condenser OFF, outputs 2, 4, and 6 have two condensers OFF, and output 5 has all three condensers OFF. The number of OFF condensers among the outputs follows a binomial distribution (Table V).

Table V Ferroelectric Switch Analysis

	All ON	One OFF	Two OFF	Three OFF	Four OFF	Five OFF
4-position switch	1	2	1			
8-position switch	1	3	3	1		
16-position switch	1	4	6	4	1	
32-position switch	1	5	10	10	5	1

Successful operation of the switch postulates that a single OFF condenser leading to an output will cause that output to be OFF. To test this, an eight-position switch was constructed (Fig. 29) using a thin (0.025-inch) sheet of barium titanate ceramic (Glenco body "X-18"). All of the non-linear condensers were placed on the same sheet by firing electrodes on the two sides as shown. The signal enters the sheet via a large fired electrode (back view). Two electrodes match this input electrode on the opposite side (front view). Among the two condensers thus formed, one will always be OFF and one will always be ON. Each of these two electrodes is enlarged to match up with two electrodes on the opposite side which are alongside the input electrode. One of each pair of this third set of electrodes will be OFF. Finally the signal goes through the dielectric a third time coming out on one of the eight small electrodes (front view).

The operation of the switch is illustrated graphically by Fig. 30. With a constant-amplitude sine-wave input of variable frequency, the rms output at terminal 7 was measured as a function of frequency for each of the eight possible combinations of S_1, S_2, and S_3. At 800 cps, the best operating frequency for this particular design, the ratio of ON voltage to the highest OFF voltage is greater than three to one. This operating frequency can be shifted higher or lower by changing the size of the condensers and resistors. Both steady-state and pulse tests on this dielectric indicate that the operating frequency can be shifted up to several megacycles per second. If the resistors are replaced by inductors, the output-versus-frequency characteristics can be improved and losses are lowered.

For pulsed operation of this switch, a non-linear condenser is used in both the series and shunt arms of the filter. Fig. 31A illustrates such a switch which is so arranged that when the series condenser is ON, the

shunt condenser is OFF (Fig. 31B); and when the series condenser is OFF, the shunt condenser is ON (Fig. 31C). The filter looks like a condenser voltage-divider to the rising edge of a pulse. The divider has either a large condenser in its upper leg and a small condenser in its lower leg or vice-versa, depending on whether the switch in ON or OFF.

The ferroelectric switch is proposed as a means for driving the rows and columns of a ferroelectric memory and for switching within an information-handling system. Its unique packaging makes it promising in applications where size, weight, and cost are important considerations.

CHAPTER V

SUMMARY AND OUTLOOK

The investigations started in this thesis are being continued in the M.I.T. Digital Computer Laboratory. As the various parts of the thesis are briefly summarized below, an attempt is made to indicate the direction of present and future work in this field.

A. TESTING EQUIPMENT AND TECHNIQUES

This thesis has described equipment and techniques which can be used to evaluate ferroelectrics for digital information-storage and switching applications. The equipment permits observation of switching transients whose total duration is less than 1 microsecond. Provision is made for control of pulse amplitude and temperature.

Pulse-testing of ferroelectrics will continue on a routine basis in search of improved materials for these applications. Two basic pulse-tester improvements are planned for the near future. First, the thyratron will be eliminated in favor of hard tubes so that shorter pulses can be applied. Second, the relay switches will be replaced by electronic switches so that the pulse-repetition frequency can be increased. These changes will result in operating conditions more nearly like those found in a modern information-handling system. In addition, they will make photography easier (many of the photographs shown were two-minute exposures).

B. FERROELECTRIC MATERIALS

Virtually the only obstacle impeding progress in this field is the dearth of suitable materials. Of the samples tested, only Glenco body "X-18" (A in Figure 4) showed promise for storage applications. A subsequent batch of presumably the same material was inferior to the first batch. "Aging" effects were noted when this material sat idle for

two days, during which it acquired a small degree of asymmetry in its D-E characteristic.

In spite of the present limitations, there is cause for optimism. Much progress has been made in the science of making ferroelectric ceramics within the past few years. Mostly due to other applications of barium titanate (piezoelectric transducers), uniformity has steadily improved. Researchers have recently discovered many ferroelectric relatives of barium titanate, each of which must be investigated as a possible candidate for these applications. Many of these new ferroelectrics have a higher Curie temperature than barium titanate.

Single-domain barium titanate crystals have been grown which have properties superior to those of the ceramics for our applications. At the Bell Telephone Laboratories, Murray Hill, New Jersey, J. R. Anderson is studying many of the same problems using barium titanate single crystals grown at that laboratory.

C. FERROELECTRIC STORAGE AND SWITCHING DEVICES

This thesis has described a method for storing information in ferroelectric condensers and an efficient means for selecting among a group of such condensers by assembling them in a two-dimensional matrix where selection is accomplished by pulsing one row and one column of the matrix. A means for achieving a 3 : 1 voltage-selection ratio has been devised, and a system has been described for mixing the information-output current pulses of the matrix by transformer coupling. Information writing and reading have been demonstrated under repetitive conditions which simulate matrix operation. Switching time for some ferroelectric ceramics has been shown to be in the 1-microsecond region.

A ferroelectric switch has been described which can accomplish many of the switching tasks in an information-handling system. An

8-position model of such a switch was demonstrated.

Perhaps the most striking feature of the matrix memory and the switch is their packaging. The logical circuitry of both can be painted directly onto the two sides of a thin sheet of ferroelectric ceramic.

If we consider the ferroelectric switch as a box with inputs and outputs, with a unique output for every combination of inputs, we are free to define this unique relationship. We may, for example, define the output as the sum of the inputs, and thereby specify an adder, which can then be painted and packaged as neatly as the memory.

Many interesting fabrication techniques have been suggested to the author during the course of this thesis. One suggestion is to make a mask through which the circuitry can be evaporated or sprayed. Another is to paint the entire ferroelectric ceramic sheet with silver-paste or evaporated-silver electrodes, and then photoengrave the logical circuitry.

Thinner ceramic sheets will allow lower voltages to be used. Mechanical strength places the only practical limit on how thin the ceramic sheets can be made. Sheets as thin as 0.08-mil have been fired on platinum foil.

Fabrication and packaging improvements at first appear rather superficial as compared with the problem of getting a device that works. The engineer who has worked closely with large-scale digital computers, however, immediately sees in ferroelectric painted components a chance to eliminate thousands of the bad joints and soldered connections which have plagued him. The mathematician who has problems which must wait for computers having high-speed internal memories much larger than those of today sees in ferroelectrics the promise of realizing such memories, both physically and economically. The designer of aircraft electronic equipment sees in ferroelectric painted switches a light-weight and

compact component for airborne applications. The fabrication and packaging possibilities of ferroelectric components for digital information storage and switching are indeed promising and challenging.

Signed Dudley A. Buck
Dudley A. Buck

Approved
Jay W. Forrester

LIST OF DRAWINGS

Figure	Drawing
1	A-50545
2	A-51351
3	A-50546
4	A-51414
5	A-51158
7	A-51167
8	A-51170
9	C-51416
10	A-51226
11	A-51352
12	A-51353
13	A-51354
14	A-51342
15	A-51402
16	A-51399
17	A-51359
19	A-51413
20	A-50549
21	A-50547
22	A-50548
23	A-50550
24	A-51355
25A	A-51421
25B	A-51419
25C	A-51412
26	A-51155
27	A-51144
28	A-51151
29	A-50906
30	A-51148
31	A-51152

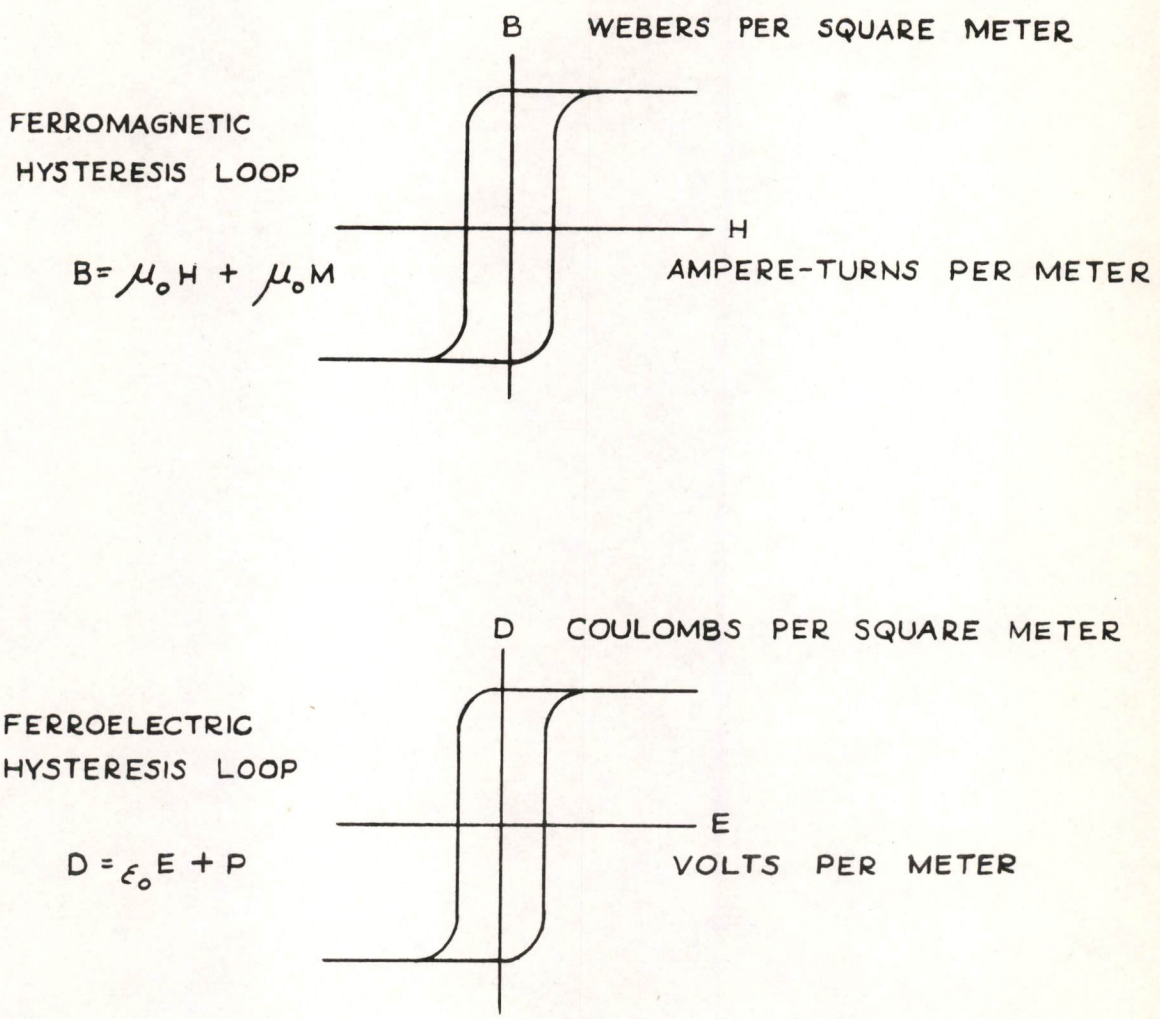


FIG. 1

COMPARISON OF FERROMAGNETIC AND FERROELECTRIC HYSTERESIS LOOPS

A-50545

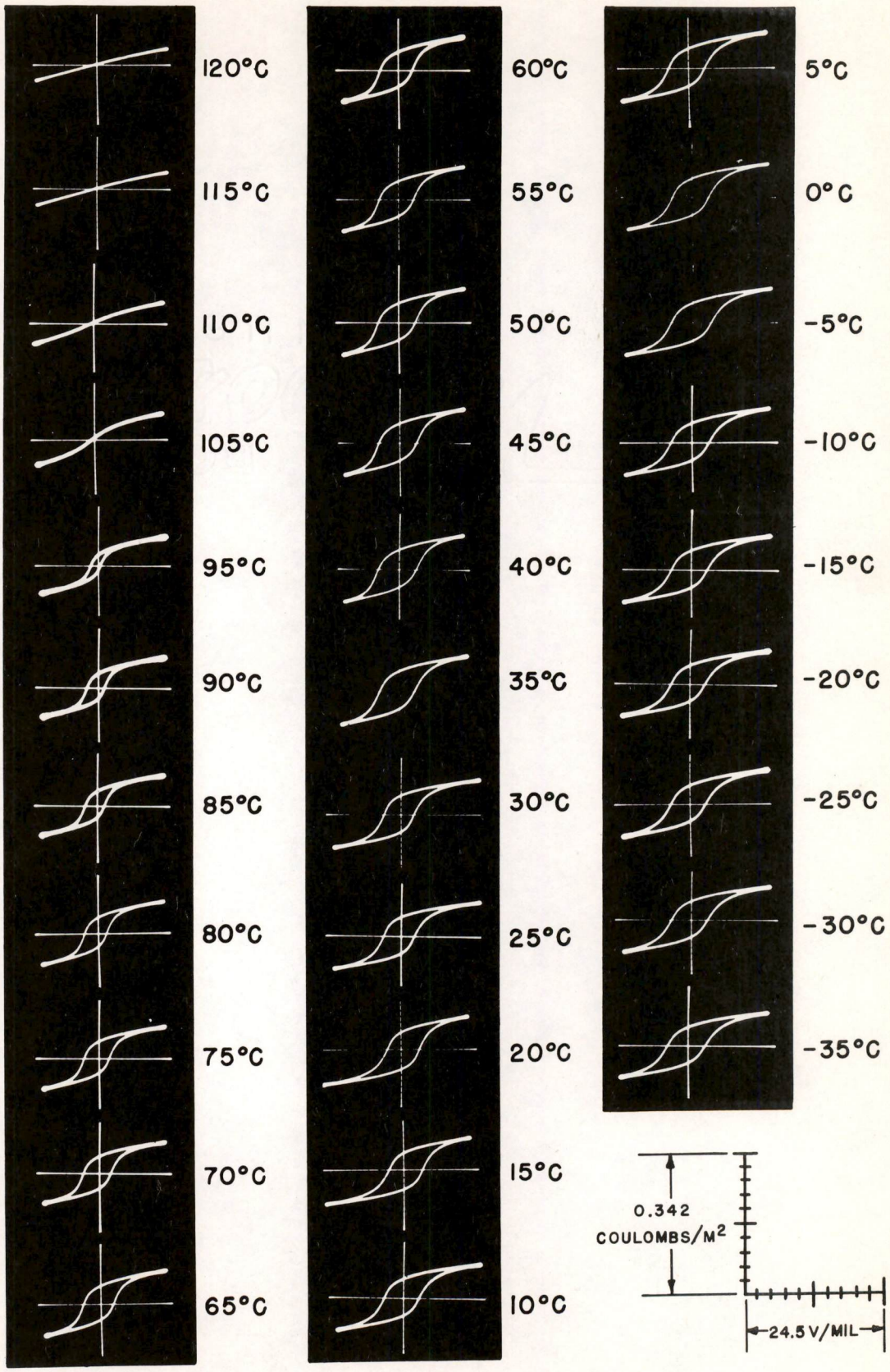
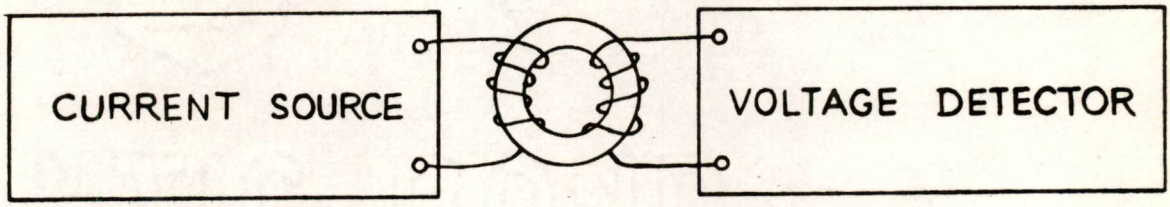


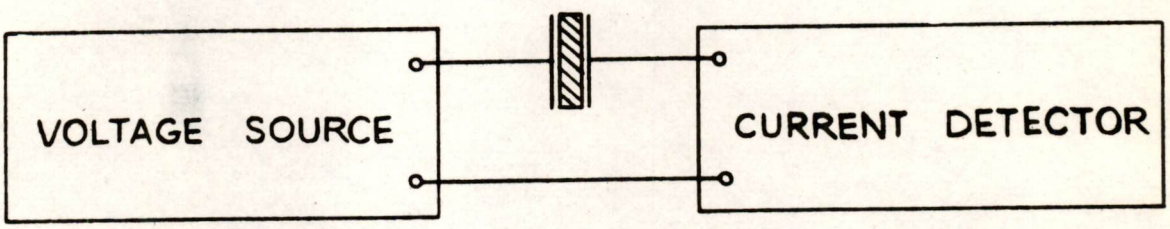
FIG. 2

HYSTERESIS LOOPS OF BARIUM TITANATE CERAMIC AS A FUNCTION OF TEMPERATURE

A-51351



FERROMAGNETIC STORAGE



FERROELECTRIC STORAGE

FIG. 3

A COMPARISON OF FERROMAGNETIC & FERROELECTRIC STORAGE

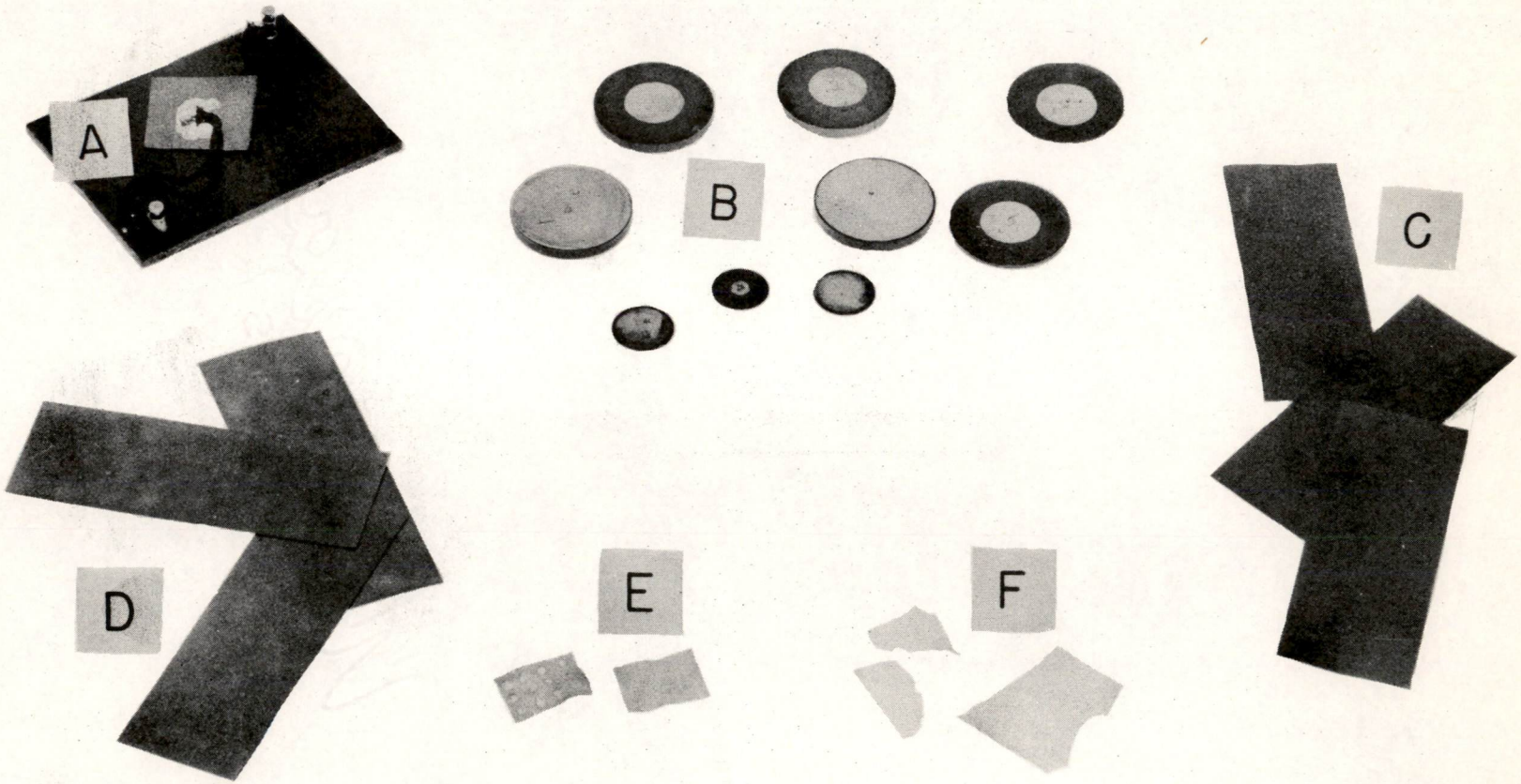
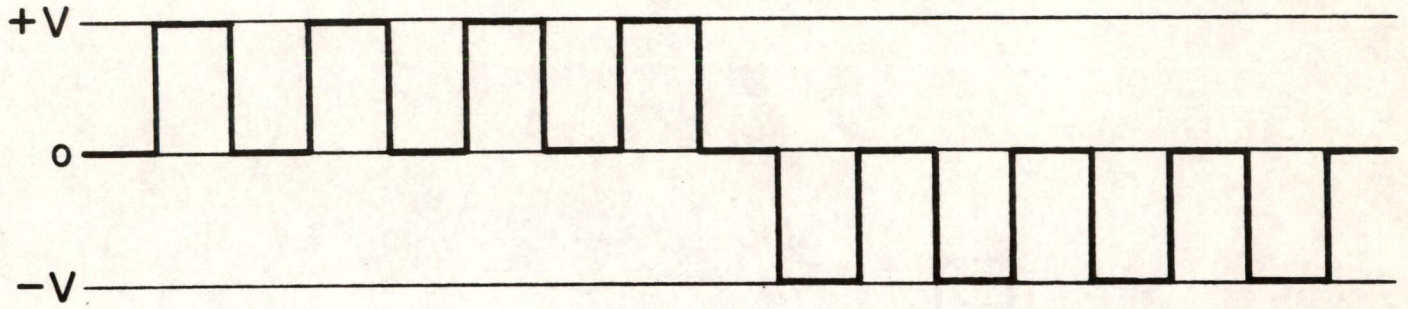
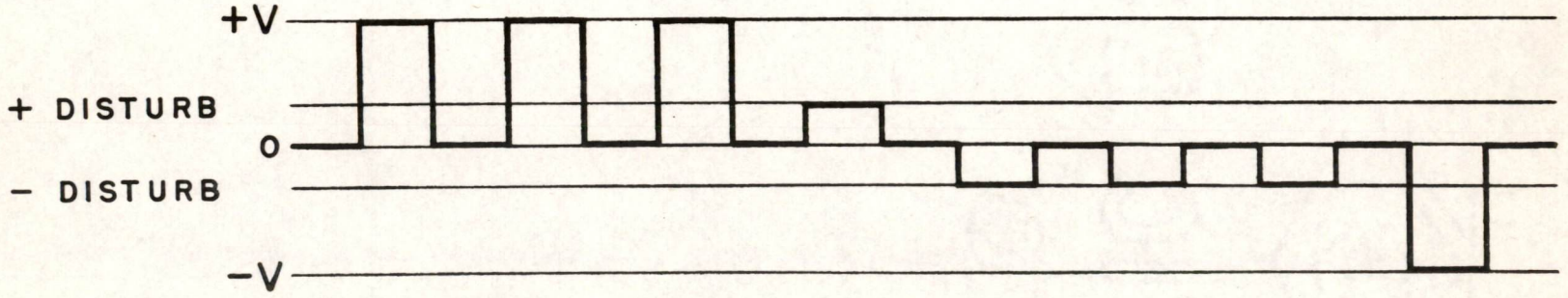


FIG. 4

FERROELECTRIC SAMPLES TESTED



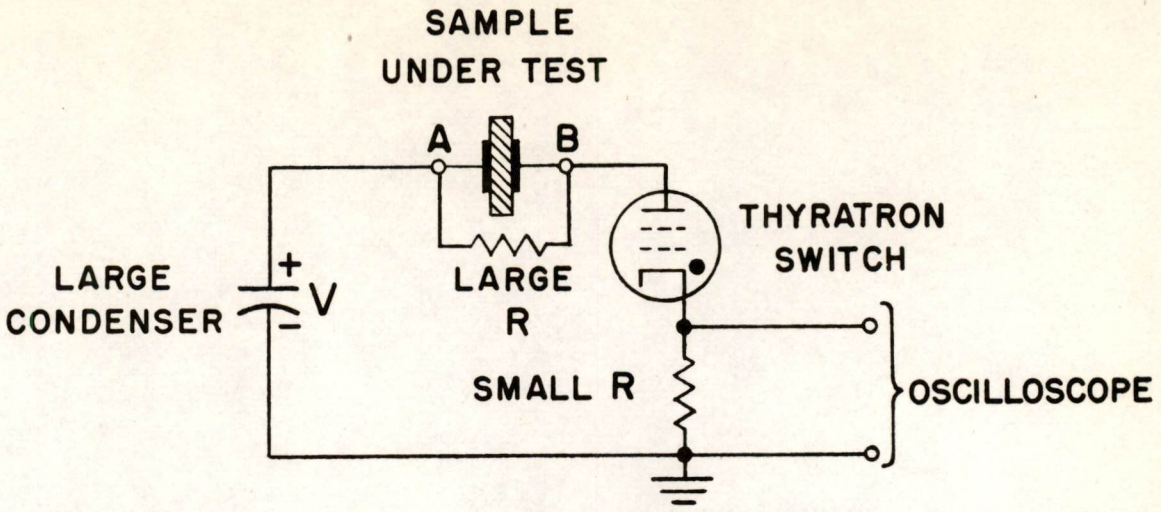
MODE A. WAVEFORM FOR SWITCHING-TIME STUDIES



MODE B. WAVEFORM FOR ANALYSIS OF EFFECT OF DISTURBANCES ON RESIDUAL DISPLACEMENT

FIG. 5

IDEALIZED FERROELECTRIC PULSE-TEST WAVEFORMS



A. BASIC FERROELECTRIC PULSE-TEST CIRCUIT

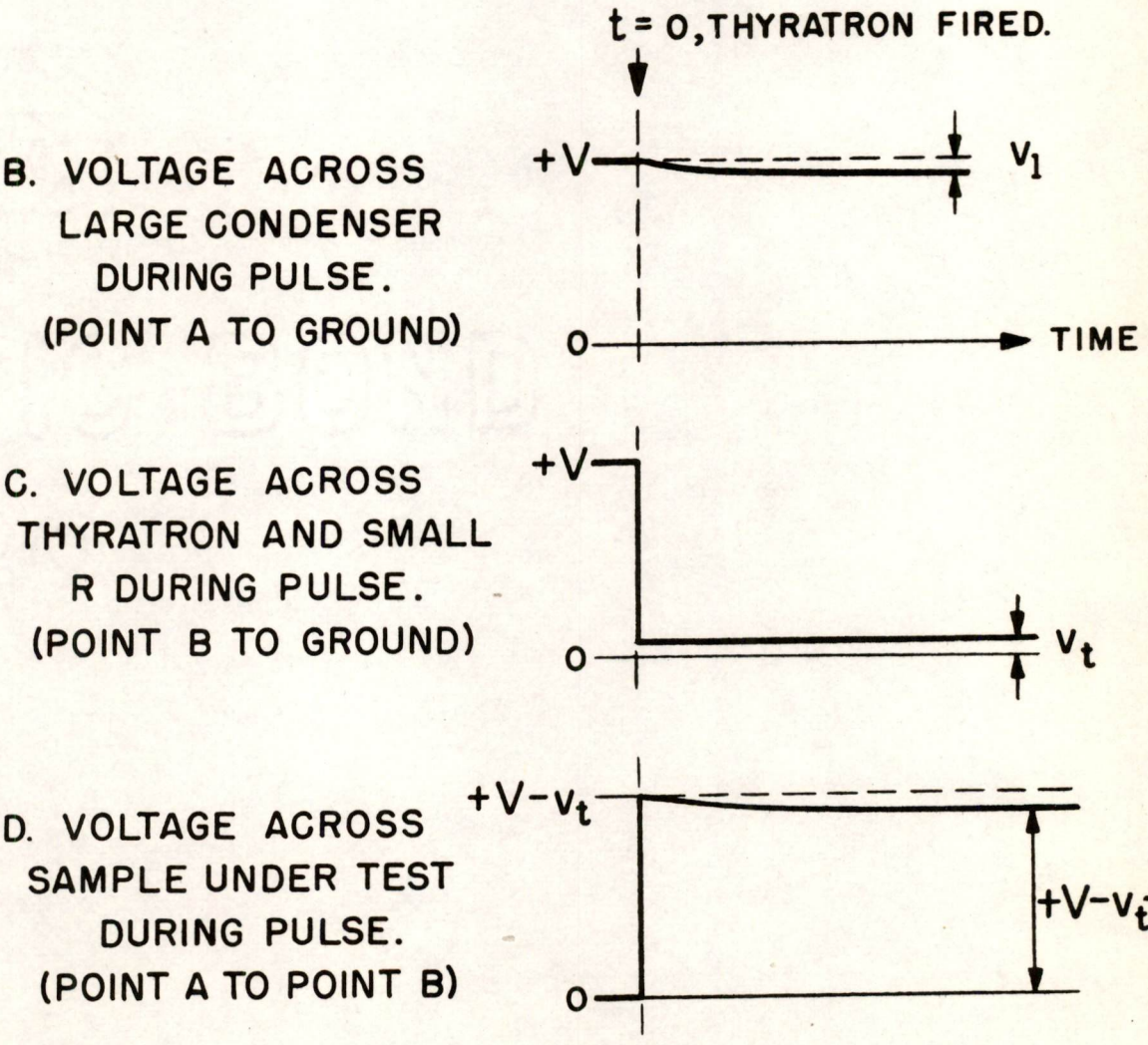


FIG. 7

METHOD OF PULSE TESTING FERROELECTRICS

A-51167

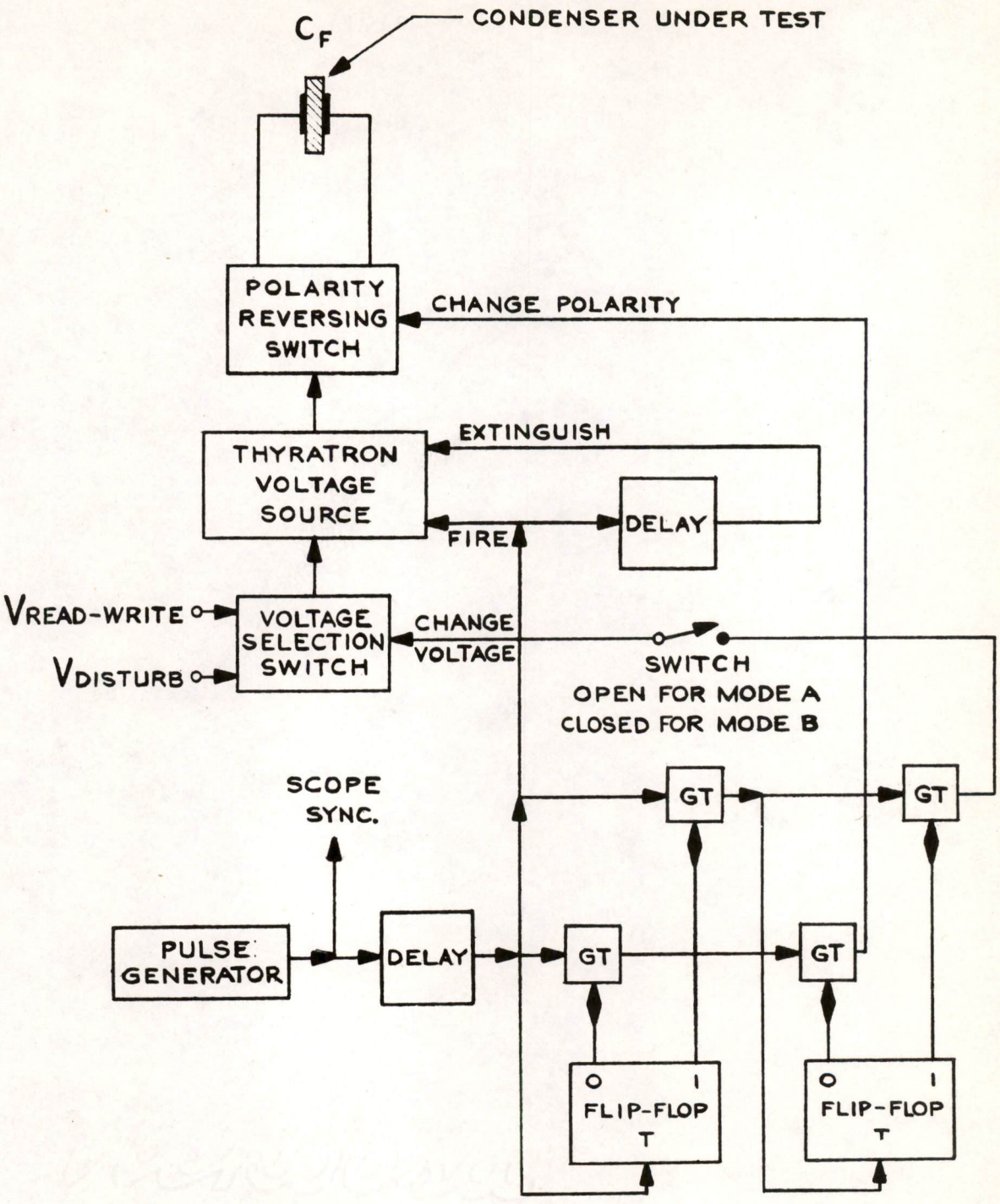


FIG. 8

BLOCK DIAGRAM OF FERROELECTRIC PULSE-TEST EQUIPMENT

A-51170

C-51416

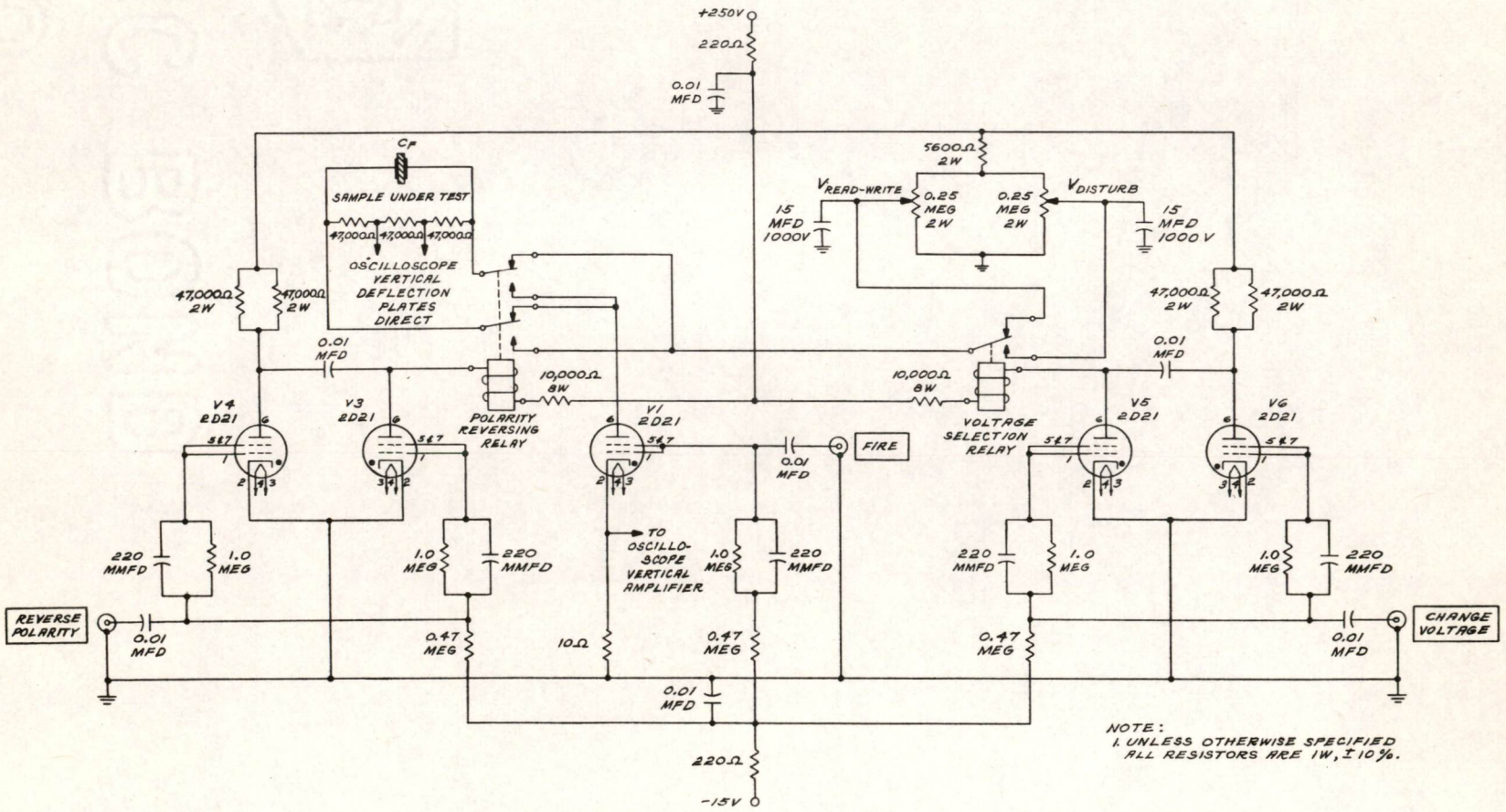
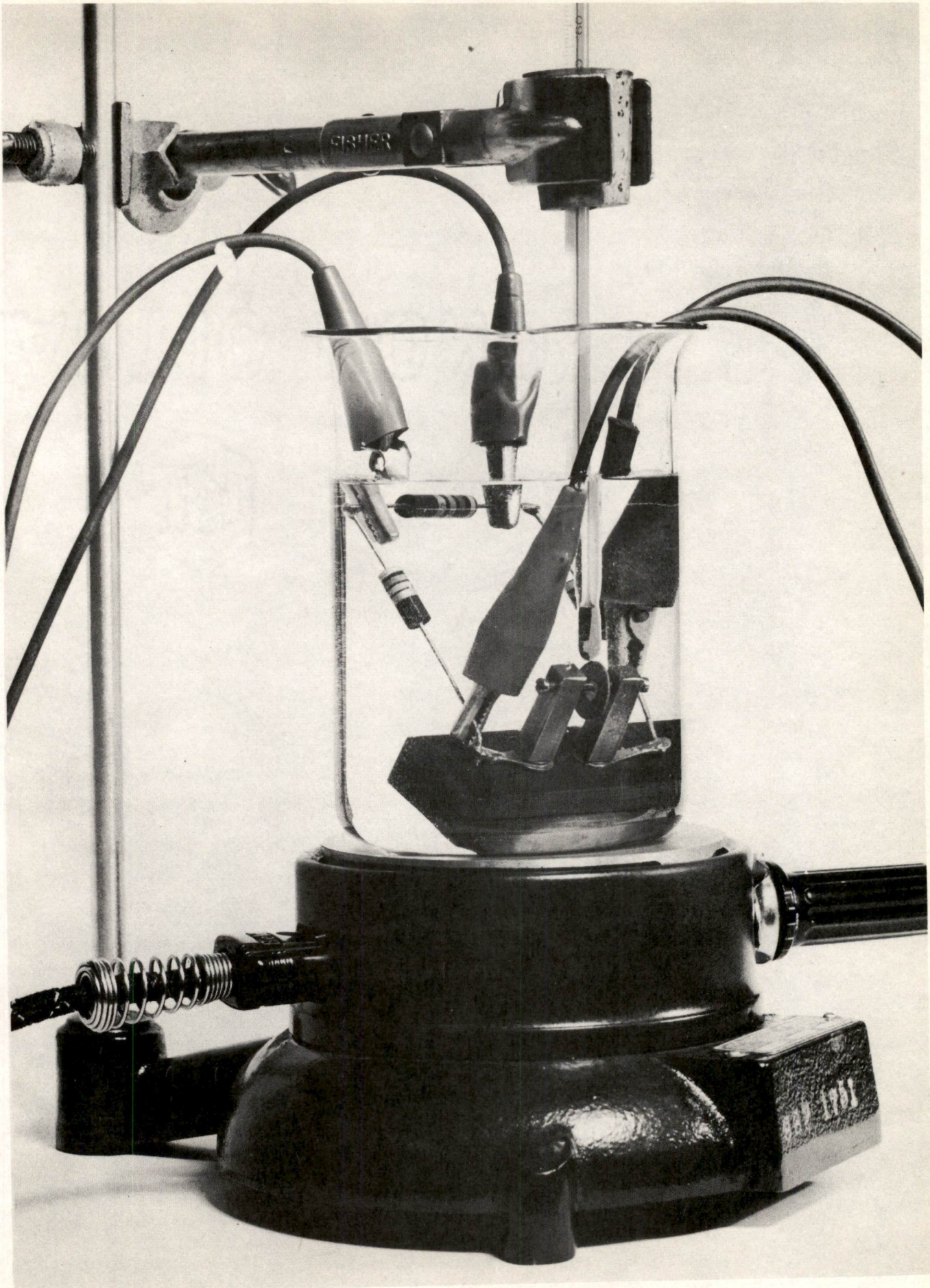


FIG. 9

CIRCUIT SCHEMATIC, FERROELECTRIC PULSE TESTER



FERROELECTRIC SAMPLE UNDER TEST

A-51226
F-1487

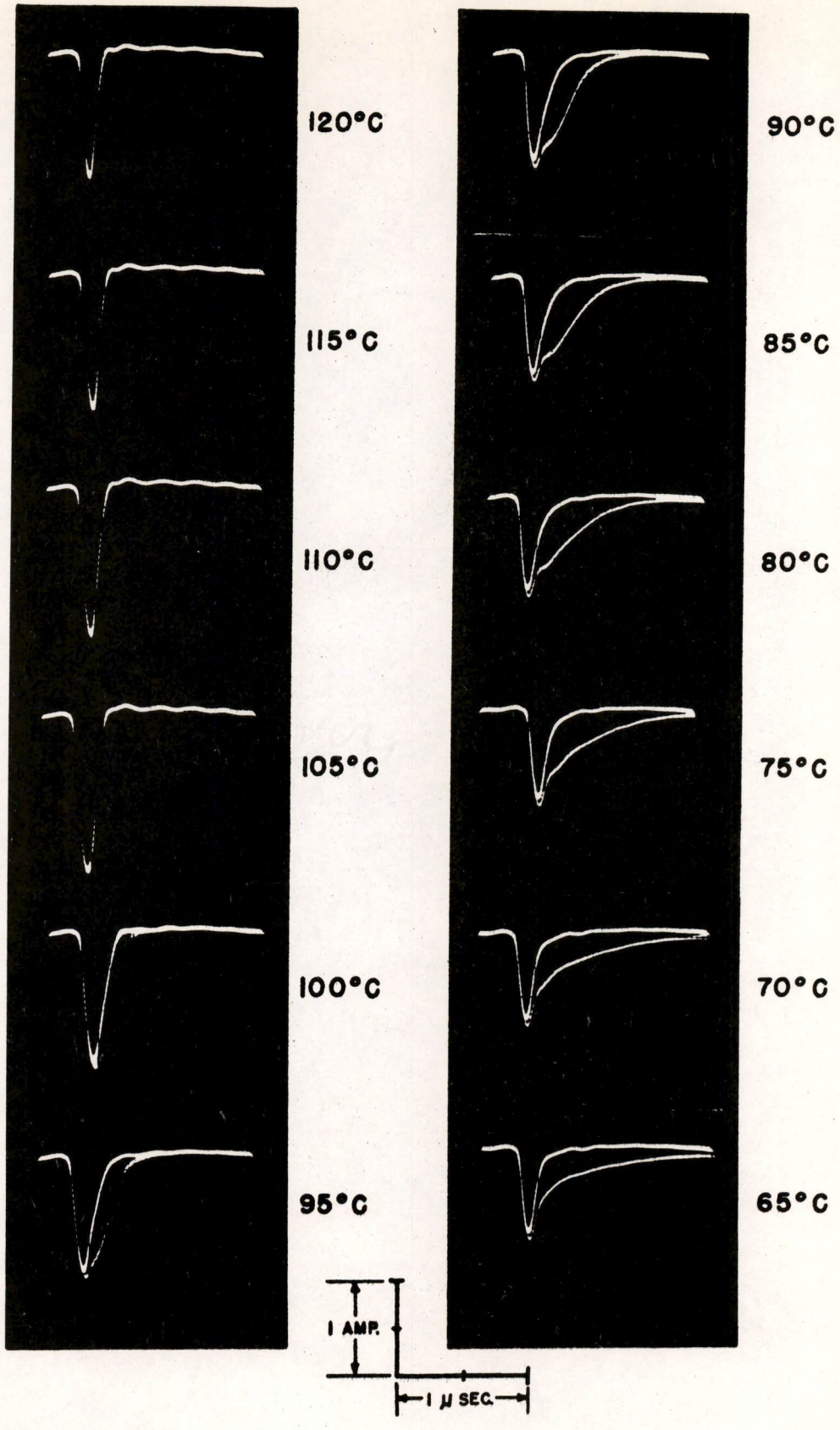


FIG. 11

MEASUREMENTS MODE A-I

CURRENT-VERSUS-TIME WAVEFORMS AS A FUNCTION OF TEMPERATURE AT CONSTANT PULSE VOLTAGE

A-51352

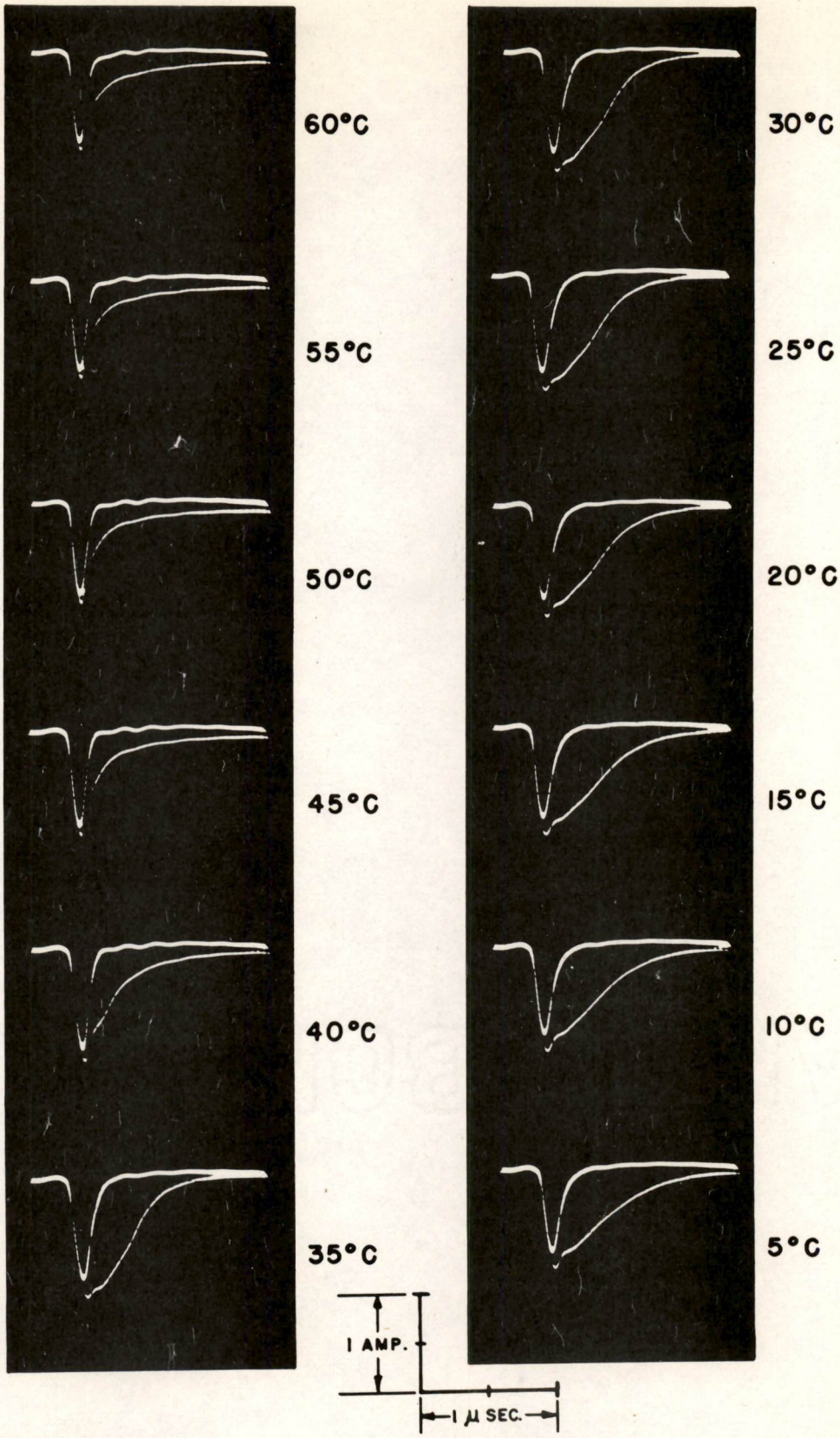


FIG. 12

MEASUREMENTS MODE A-II

CURRENT-VERSUS-TIME WAVEFORMS AS A FUNCTION OF TEMPERATURE AT CONSTANT PULSE VOLTAGE

A-51353

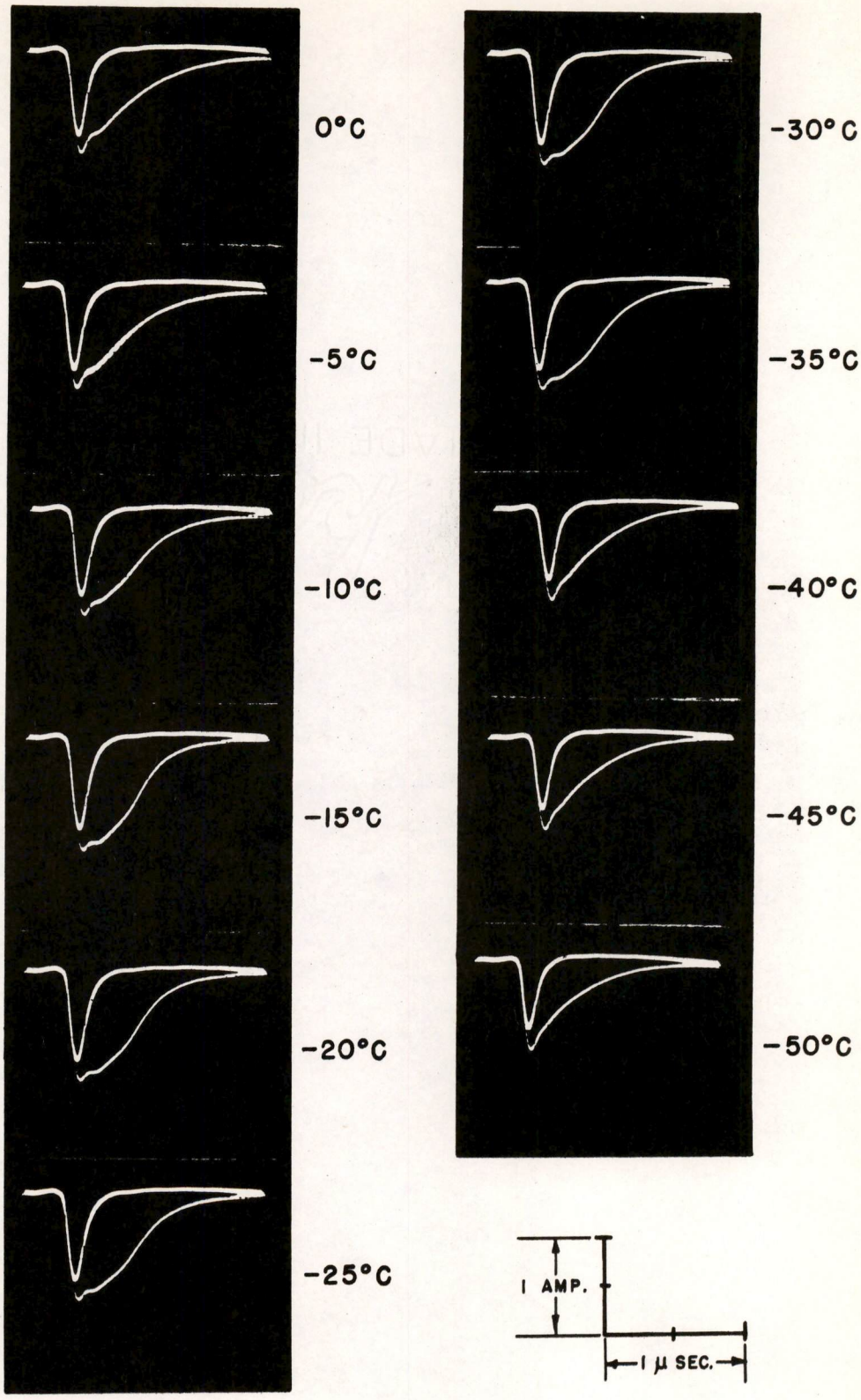


FIG. 13

MEASUREMENTS MODE A-III

CURRENT-VERSUS-TIME WAVEFORMS AS A FUNCTION OF TEMPERATURE AT CONSTANT PULSE VOLTAGE

A-51354

A-51342

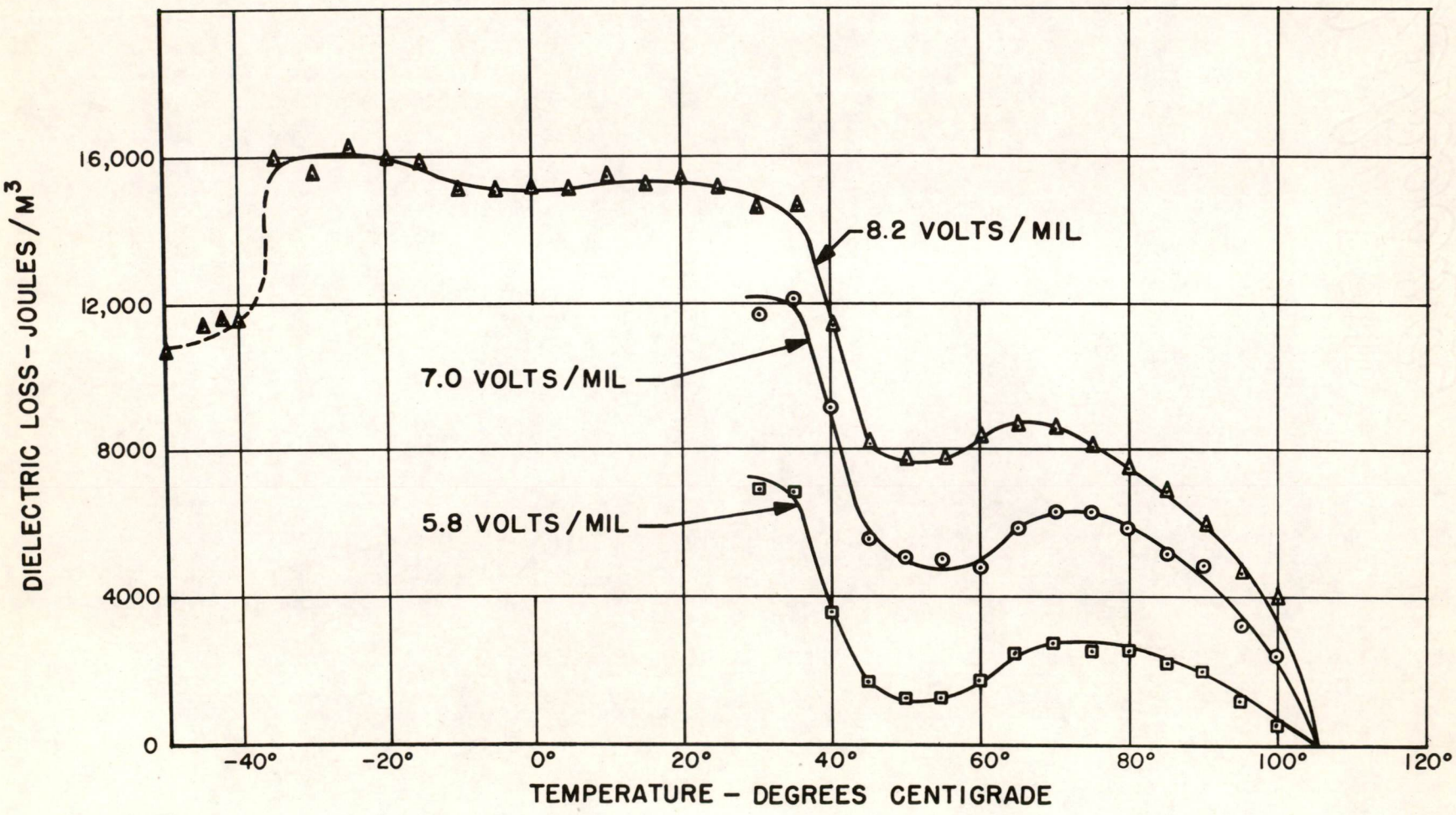


FIG. 14

DIELECTRIC LOSS FROM MEASUREMENTS MODE A

AS A FUNCTION OF TEMPERATURE FOR THREE PULSE AMPLITUDES

A-51402

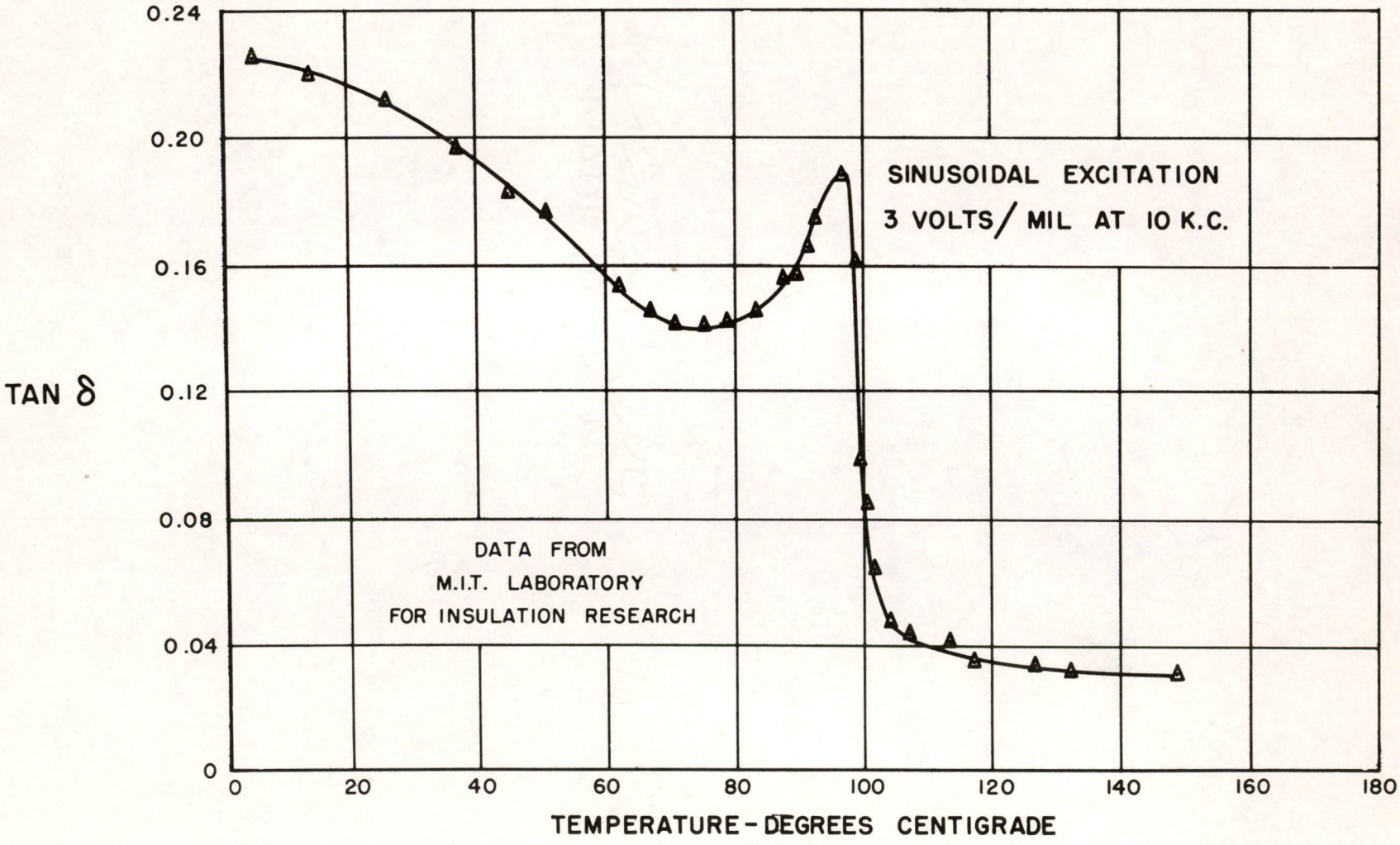


FIG 15

DIELECTRIC LOSS FROM STEADY - STATE MEASUREMENTS

AS A FUNCTION OF TEMPERATURE AT CONSTANT FIELD STRENGTH

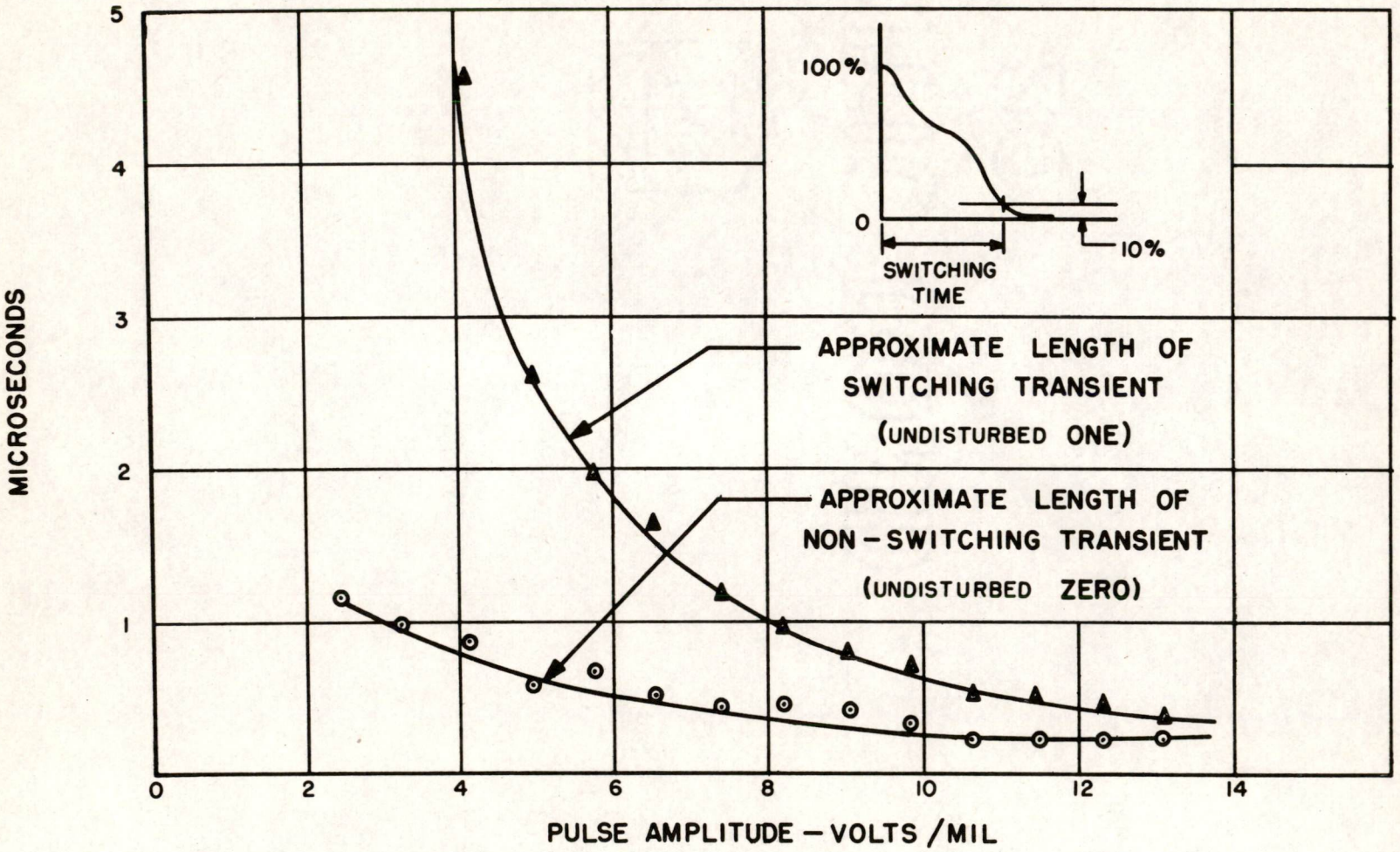


FIG. 16

APPROXIMATE SWITCHING TIME

AS A FUNCTION OF PULSE AMPLITUDE AT CONSTANT TEMPERATURE

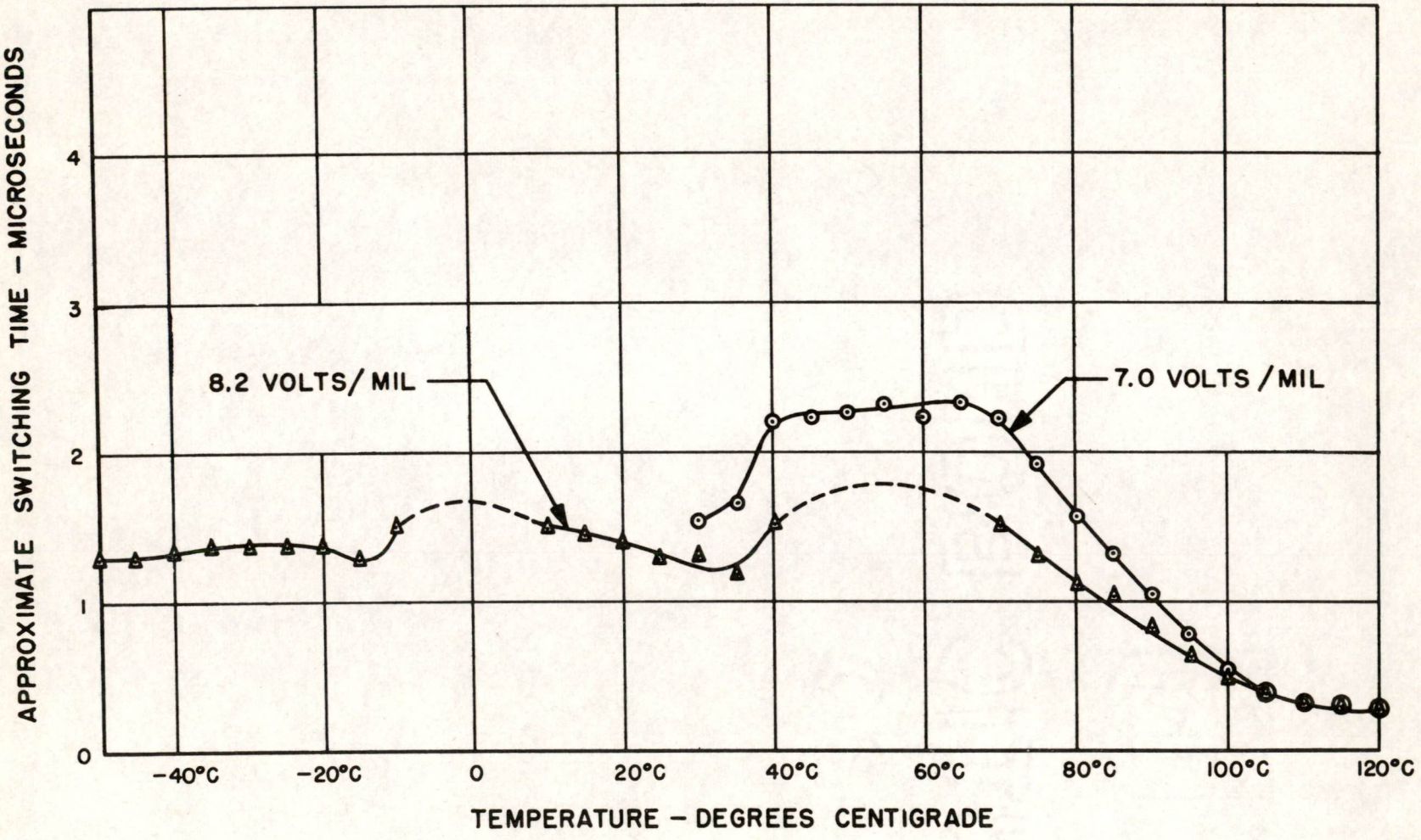


FIG. 17

APPROXIMATE SWITCHING TIME FROM MEASUREMENTS MODE A

AS A FUNCTION OF TEMPERATURE FOR TWO PULSE AMPLITUDES

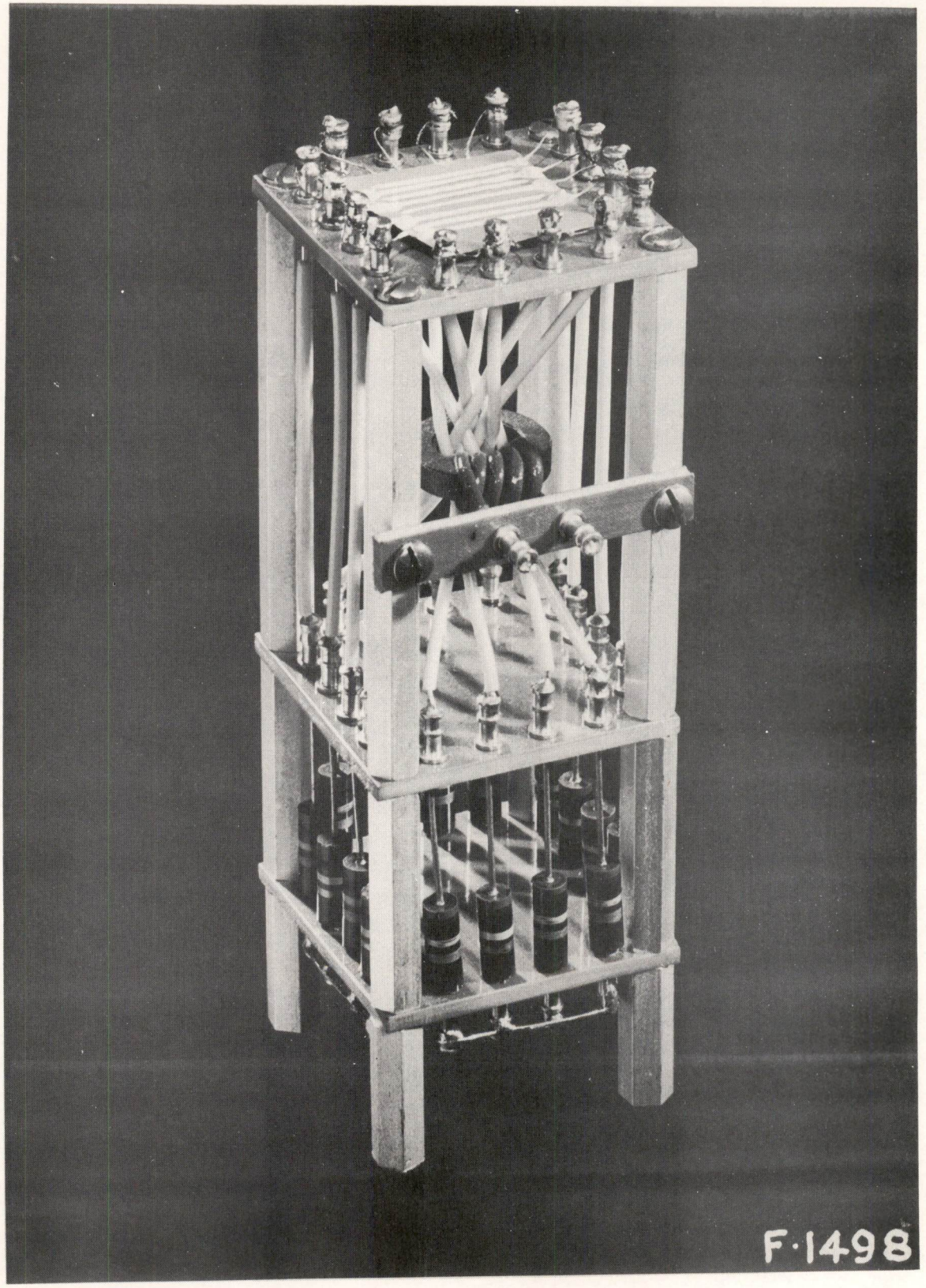


FIG. 19

EIGHT BY EIGHT FERROELECTRIC MEMORY

A-51413

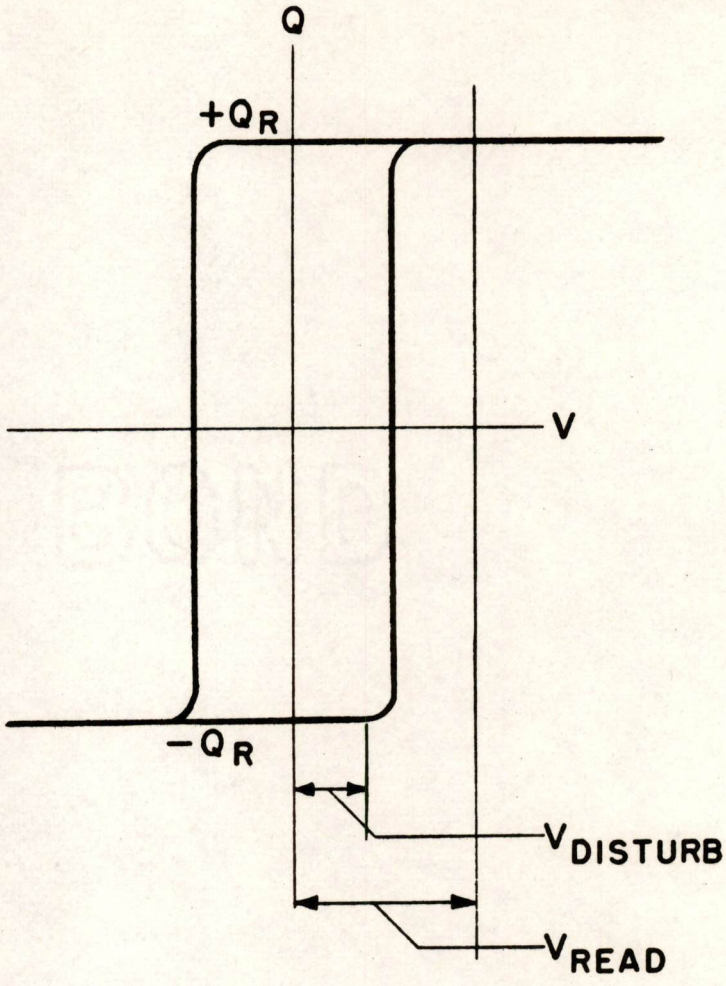


FIG. 20

DISCRIMINATION BETWEEN TWO VOLTAGES REQUIRED OF HYSTERESIS LOOP

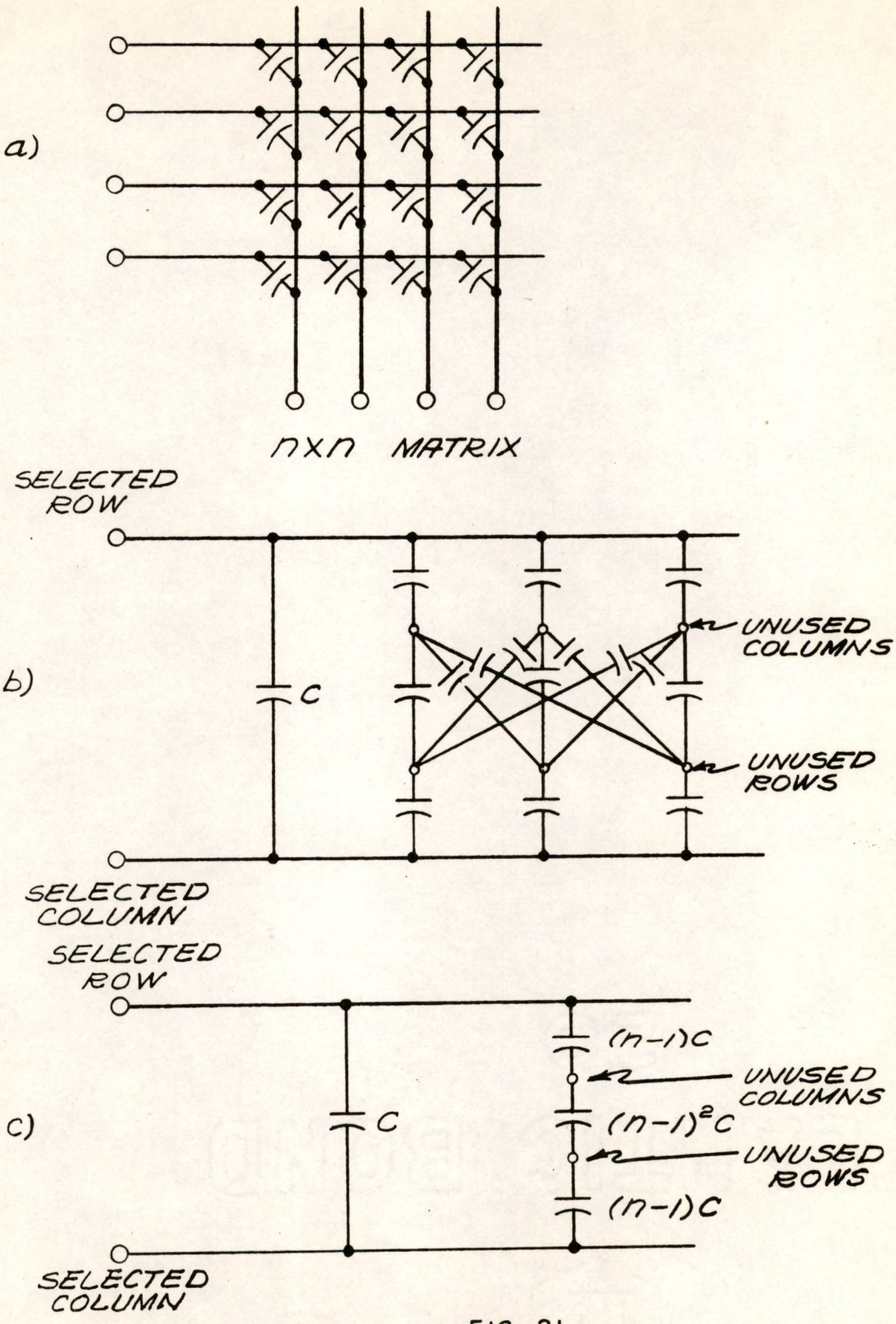


FIG. 21

MATRIX REDUCTION

A-50547

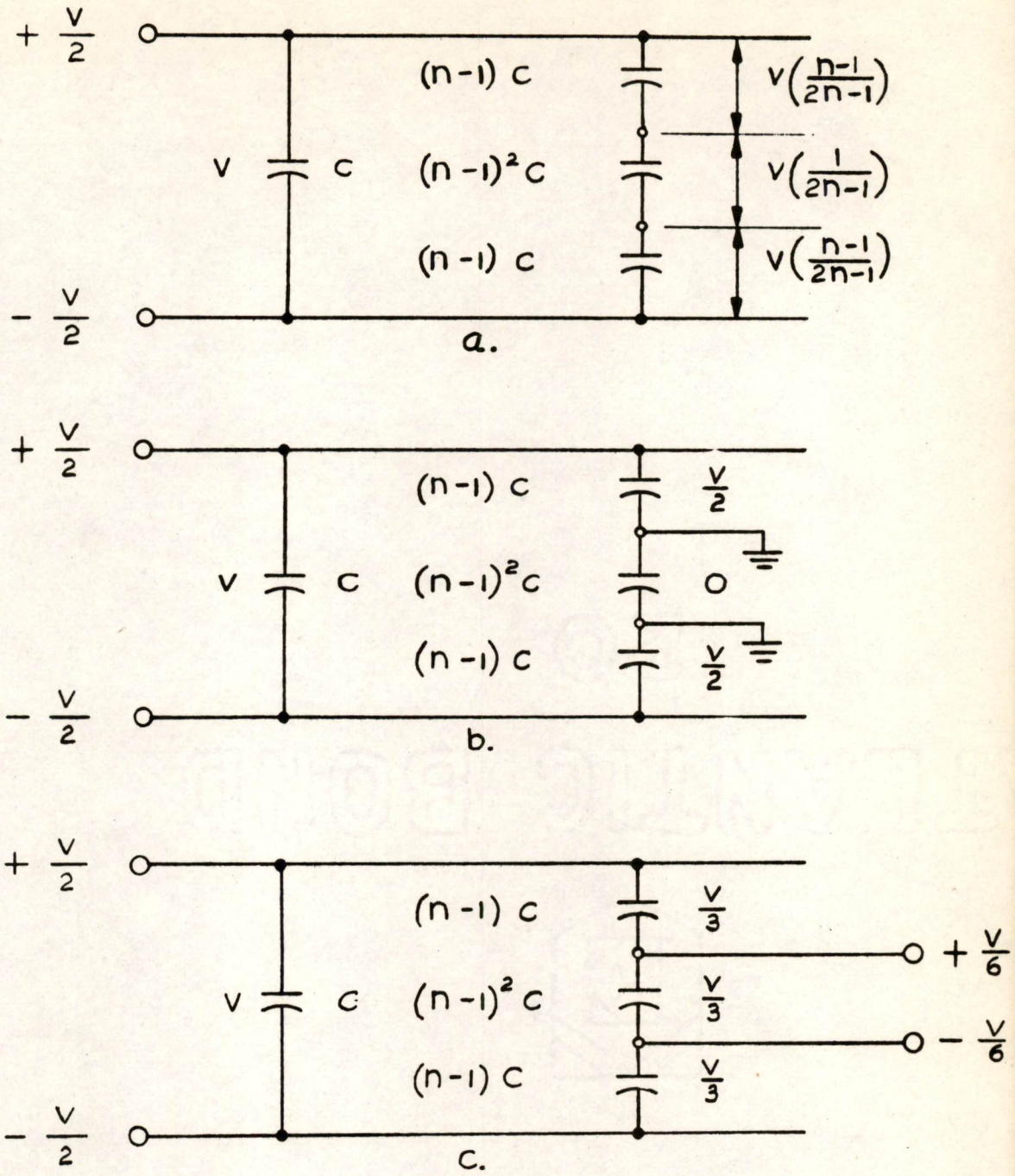
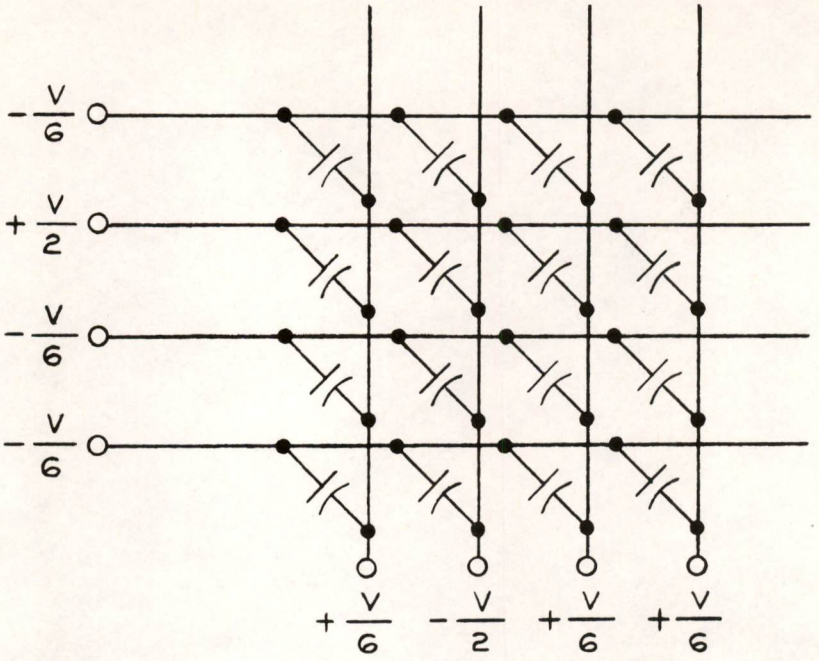


FIG. 22

THREE DRIVING SCHEMES AND RESULTING DISTURBING VOLTAGE



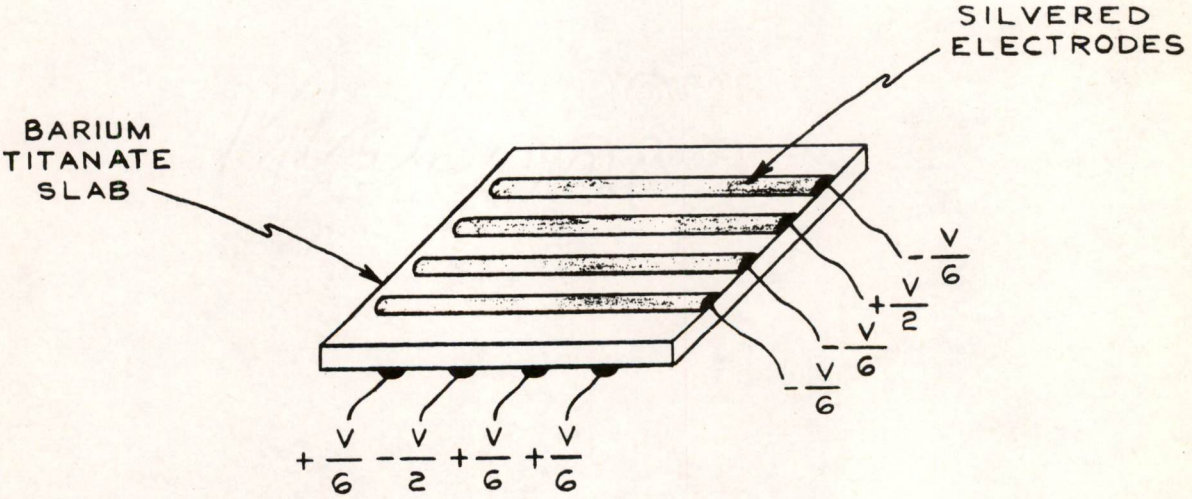


FIG. 23

FERROELECTRIC MEMORY

A-50550

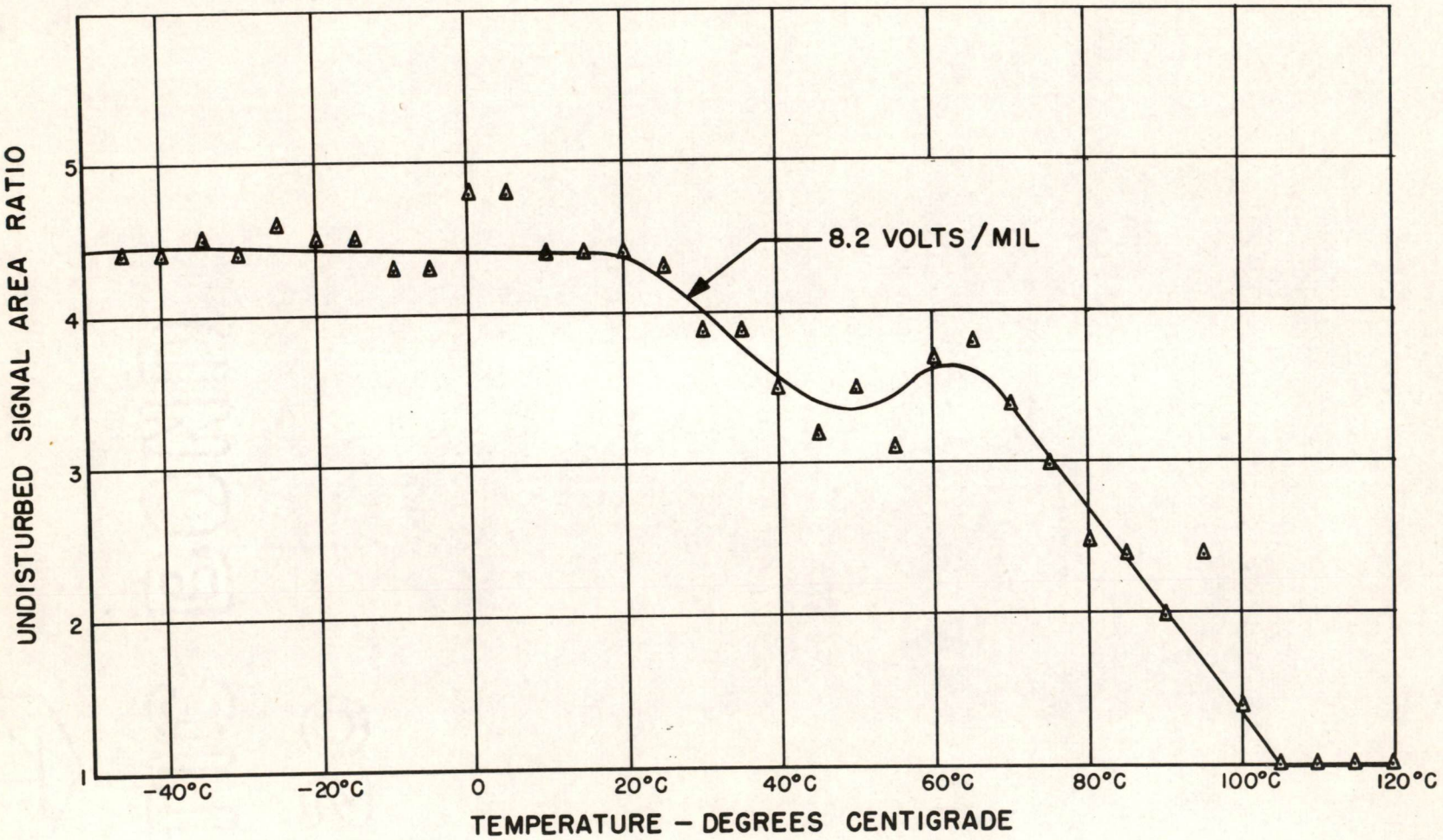
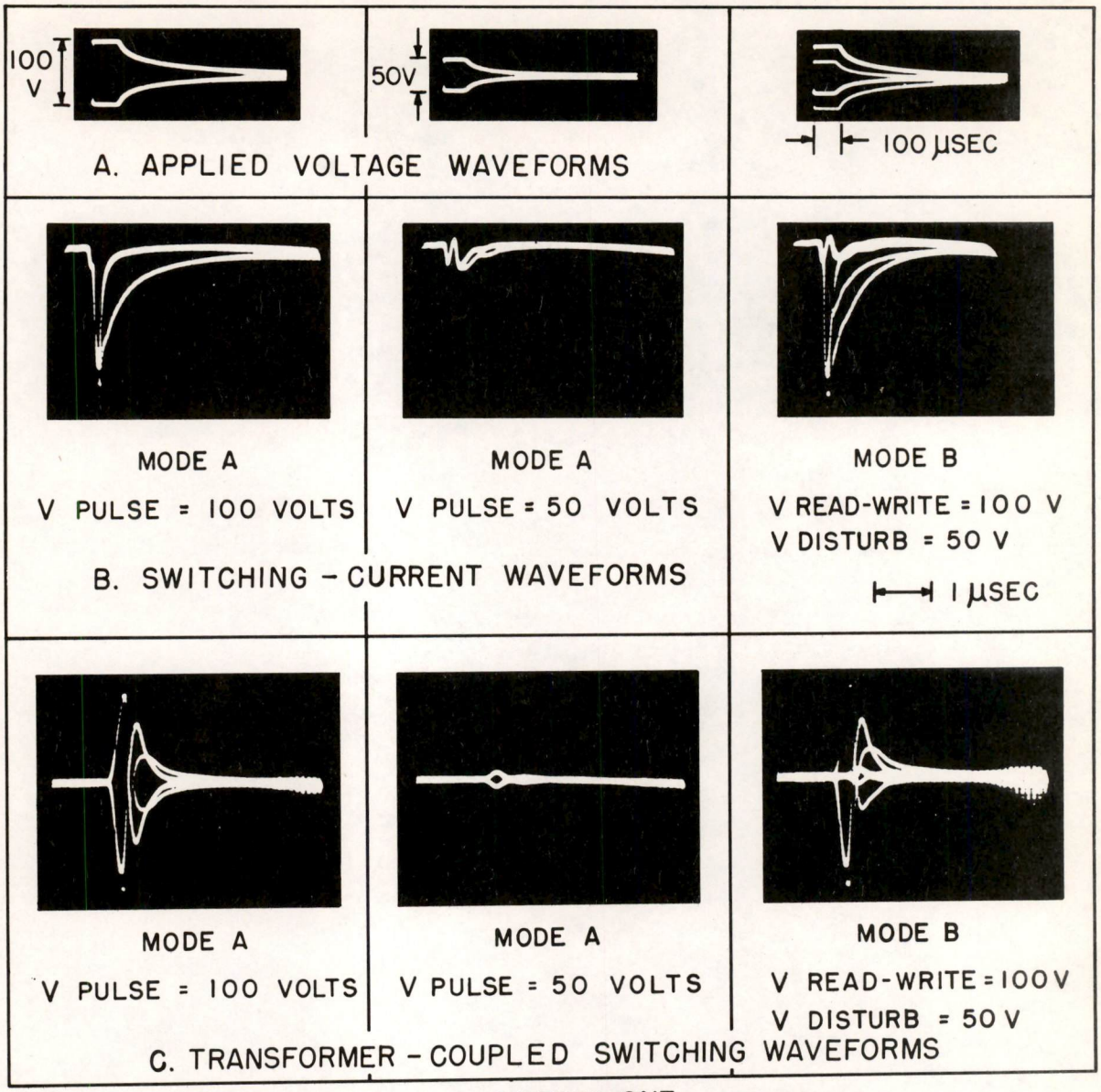


FIG. 24

UNDISTURBED SIGNAL AREA RATIO FROM MEASUREMENTS MODE A

AS A FUNCTION OF TEMPERATURE AT CONSTANT PULSE AMPLITUDE



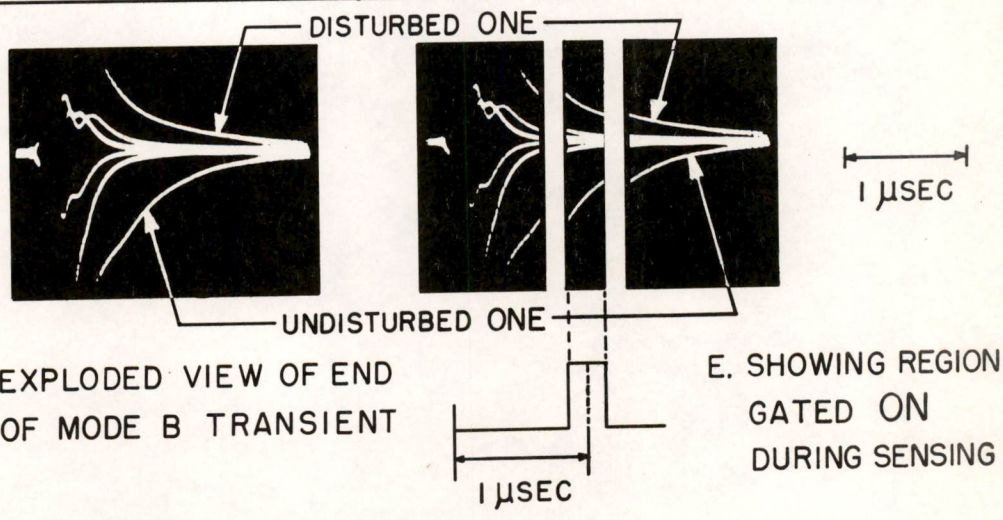
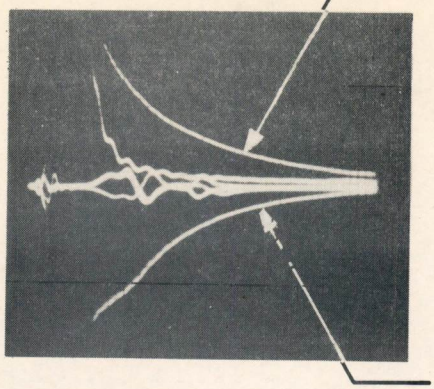


FIG. 25 A

INTRODUCTION TO MEASUREMENTS MODE B

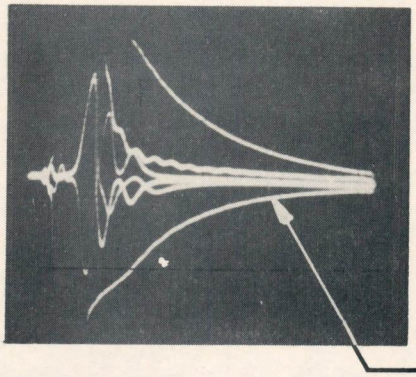
A-51421

A



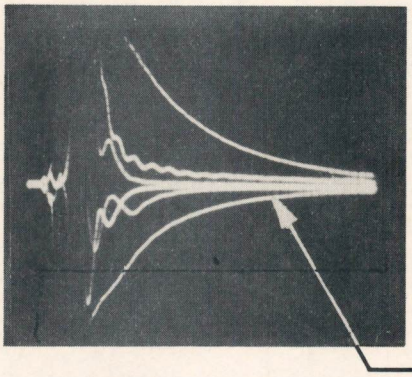
V READ-WRITE = 120V
V DISTURB = 30V
SELECTION RATIO = 4:1

B



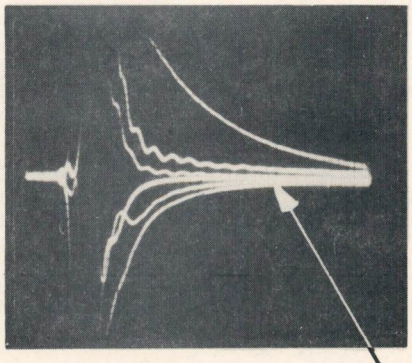
V READ-WRITE = 120V
V DISTURB = 40V
SELECTION RATIO = 3:1

C



V READ-WRITE = 120 V
V DISTURB = 50 V
SELECTION RATIO = 2.4:1

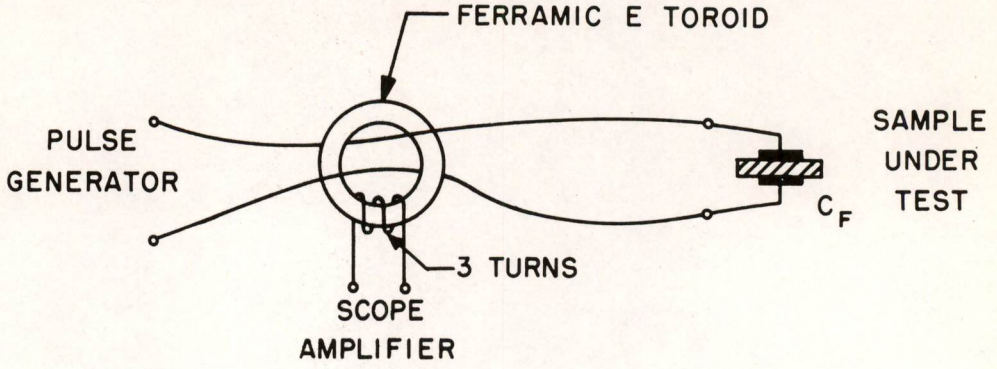
D



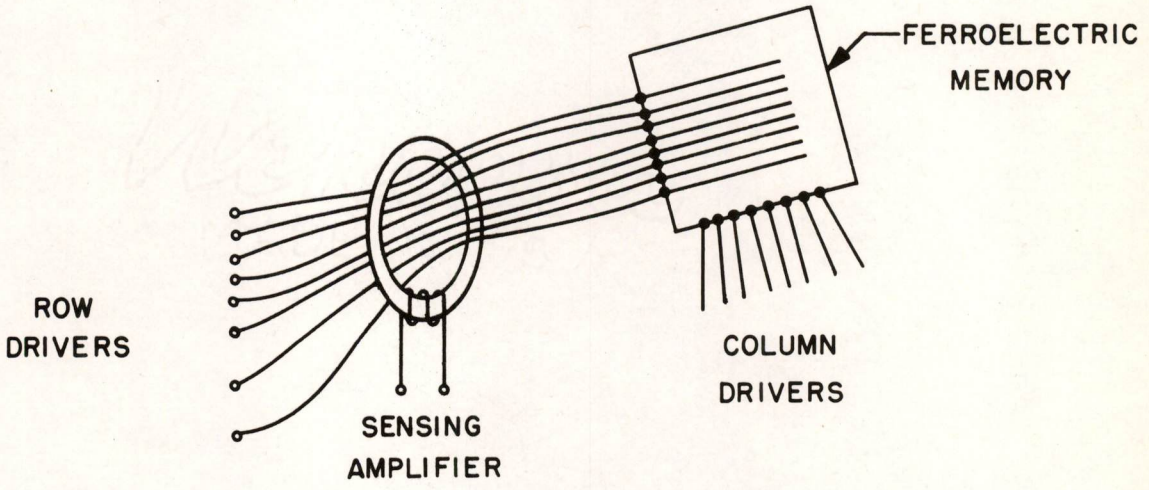
V READ-WRITE = 120 V
V DISTURB = 60 V
SELECTION RATIO = 2:1

MEASUREMENTS MODE B

AS A FUNCTION OF V DISTURB AT CONSTANT V READ-WRITE



A. TRANSFORMER COUPLING USED IN MEASUREMENTS MODE B

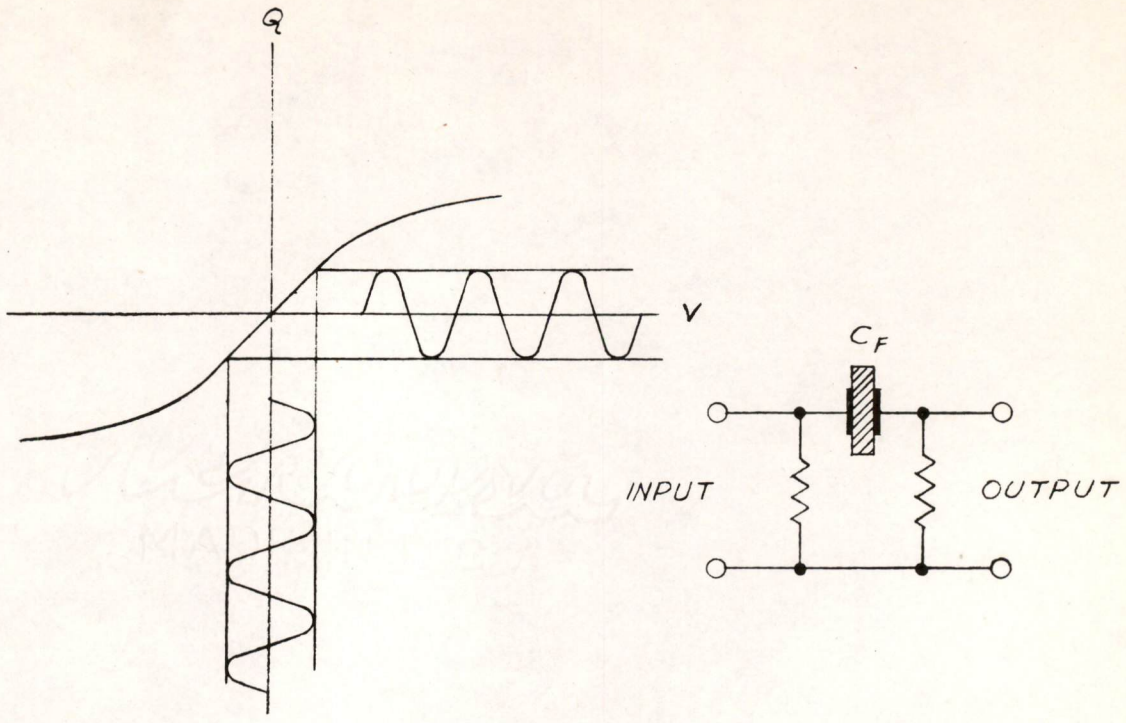


B. TRANSFORMER-COUPLING METHOD FOR SENSING FERROELECTRIC MEMORY

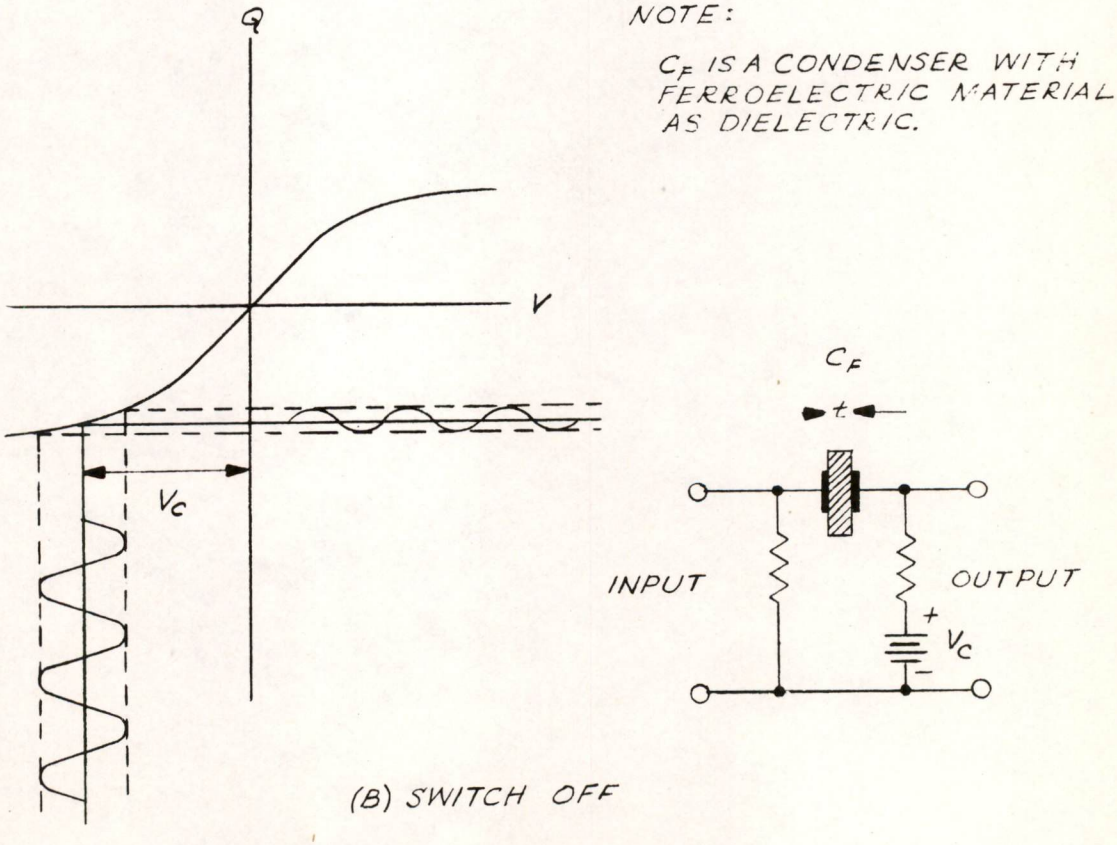
FIG. 25C

TRANSFORMER COUPLING FOR SENSING FERROELECTRIC MEMORY

A-51412



(A) SWITCH ON



NOTE:

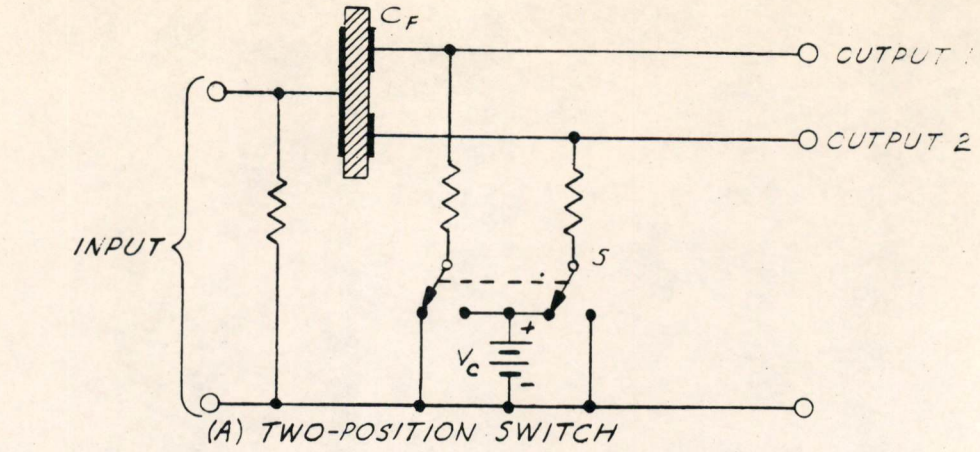
C_F IS A CONDENSER WITH FERROELECTRIC MATERIAL AS DIELECTRIC.

(B) SWITCH OFF

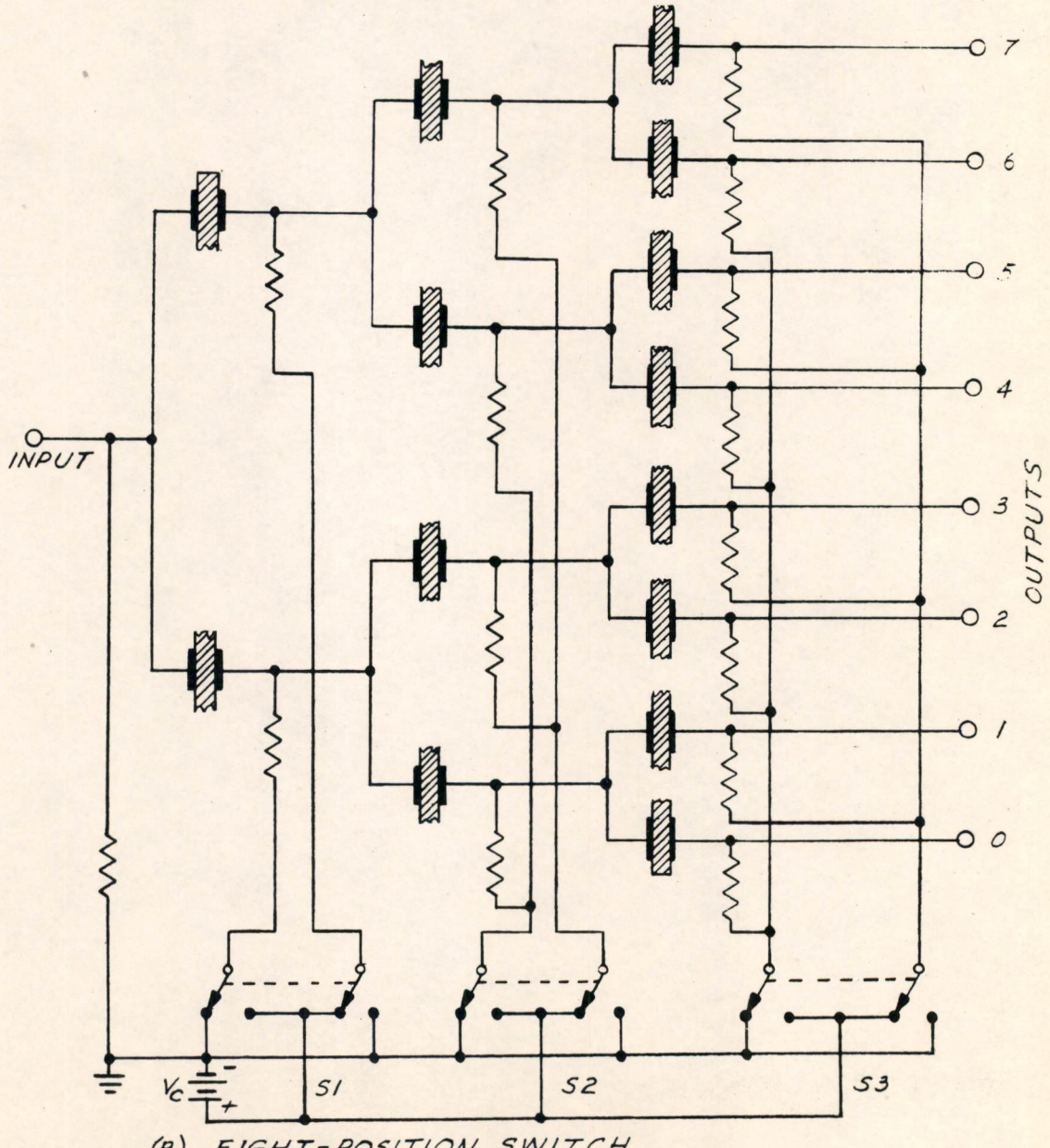
FIG. 26

FERROELECTRIC SWITCH OPERATION

A-51155



(A) TWO-POSITION SWITCH



(B) EIGHT-POSITION SWITCH

FIG. 27

FERROELECTRIC SWITCH SCHEMATIC DIAGRAM

A-51144

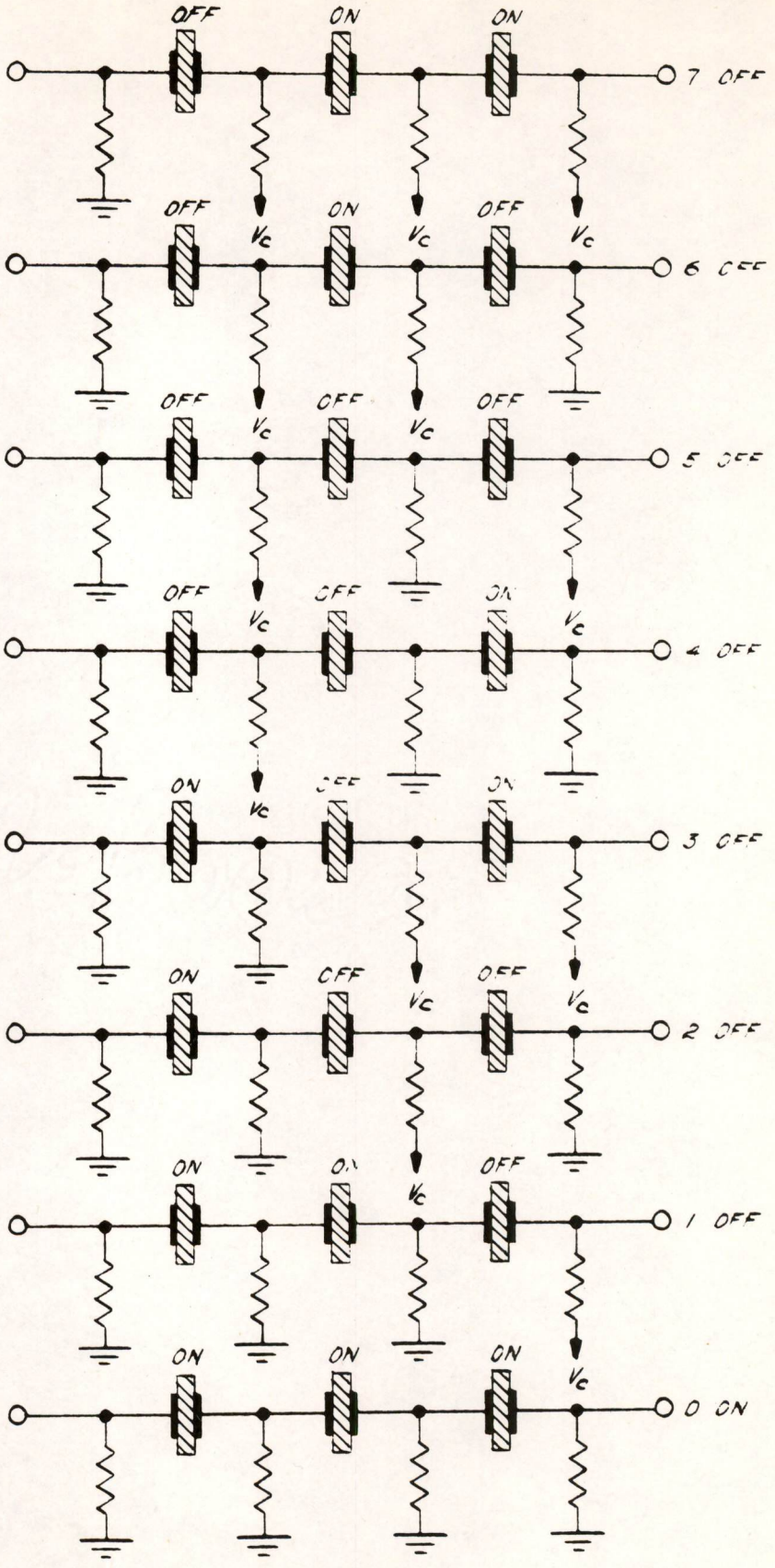
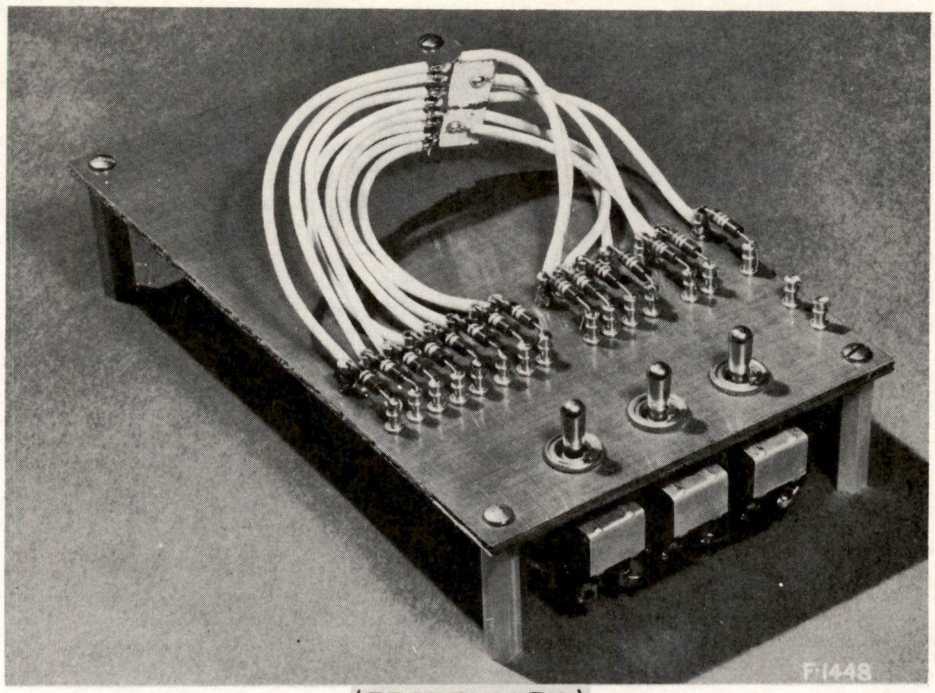


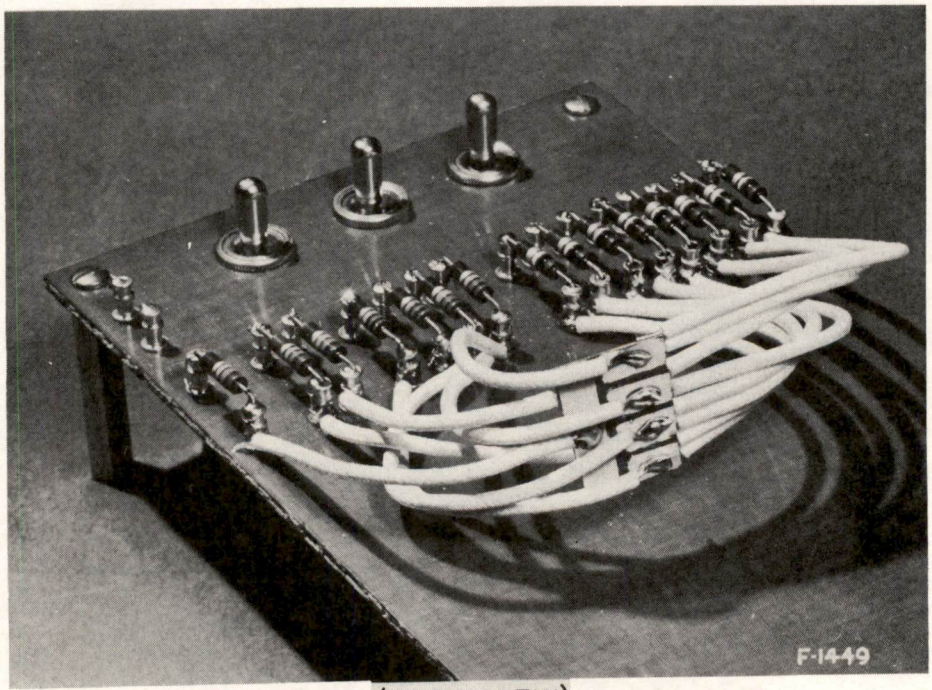
FIG. 28

EIGHT-POSITION SWITCH ANALYSIS

A-51151



(FRONT VIEW)



(BACK VIEW)

FERROELECTRIC MULTI–POSITION SWITCH

A-50906

A-51148

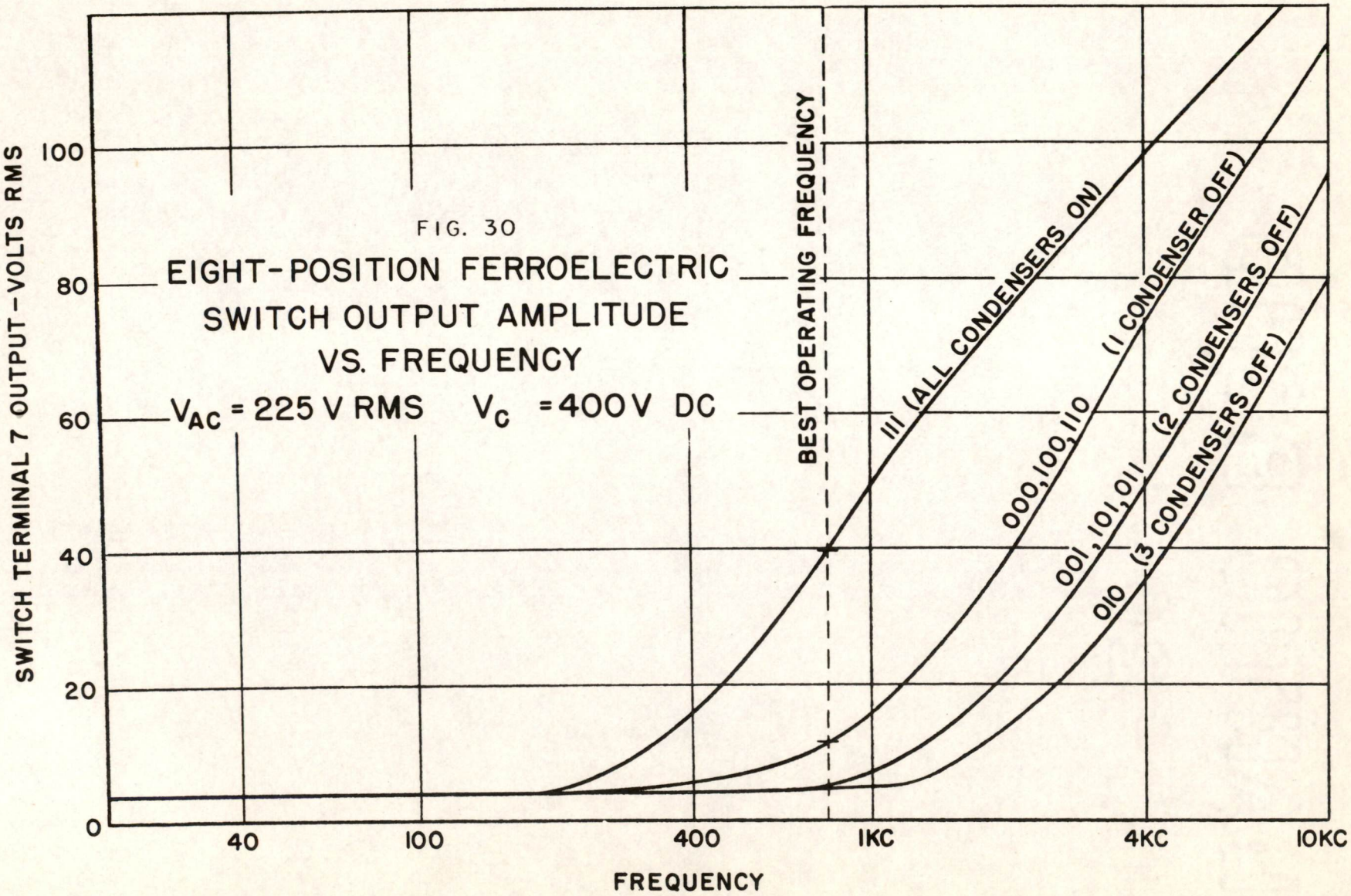
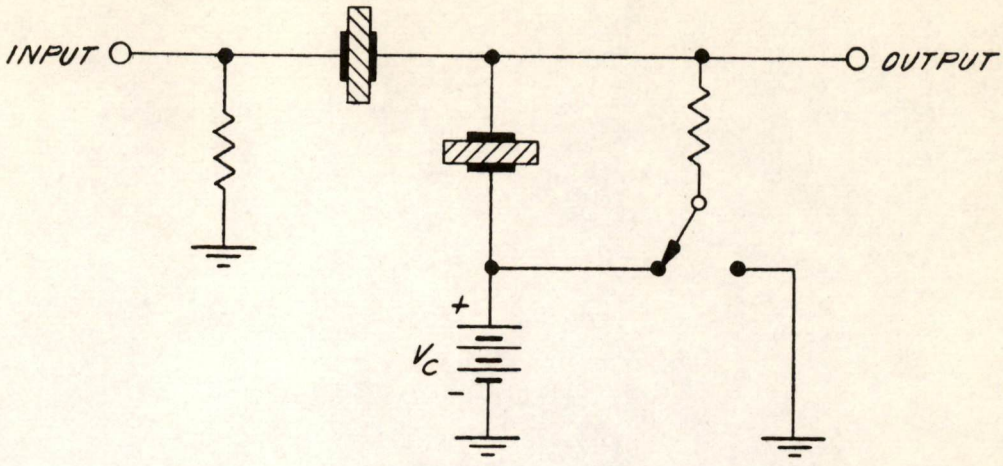


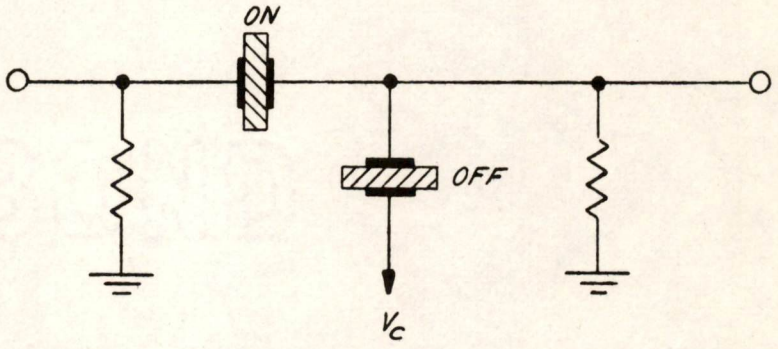
FIG. 30

EIGHT-POSITION FERROELECTRIC SWITCH OUTPUT AMPLITUDE VS. FREQUENCY

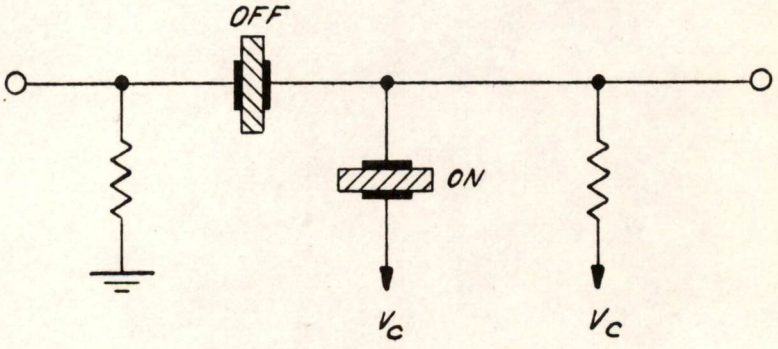
V_{AC} = 225 V RMS V_C = 400 V DC



A. CIRCUIT SCHEMATIC OF PULSE-OPERATED TWO-POSITION FERROELECTRIC SWITCH



B. SWITCH ON



C. SWITCH OFF

FIG. 31

FERROELECTRIC SWITCH FOR PULSES

A-51152