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MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LINCOLN LABORATORY

MAXIMUM EFFICIENCY TRANSISTOR SWITCHING CIRCUITS

R.H. Baker

Group 24

Technical Report No. 110

22 March 1956

ABSTRACT

The important transistor properties relating to switching-circuit design are discussed. Circuit configurations are presented which utilize the advantage of circuit symmetry possible through the combined use of p-n-p and n-p-n transistors.

LEXINGTON MASSACHUSETTS

A MAGNETIC-CORE MEMORY WITH EXTERNAL SELECTION

by

Sydney Bradspies

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(1953)

SUBMITTED IN PARTIAL FULFILLMENT OF THE

REQUIREMENTS FOR THE DEGREE OF

MASTER OF SCIENCE

at the

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January, 1955

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Department of Electrical Engineering, January 17, 1955

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ENGINEERING REPORT 6506-ER-45

SERVOMECHANISMS LABORATORY
ELECTRICAL ENGINEERING DEPARTMENT
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Project No. D.I.C. 6506

SUBJECT: Design of An Eight-Pole Magnetic-Matrix Switch

REFERENCE: Contract No. W33-038ac-13969

FILE INDEX: Switches, Magnetic Matrix
Timing References

ABSTRACT: This report describes the design of an eight-pole saturable-core magnetic-matrix switch and its use with an eleven-stage binary counter to generate consecutive eight-digit binary numbers for time coding of recorded data. The switch was designed to operate at 8 steps per second and has a maximum step delay of 0.1 millisecond. The model switch contains ten saturable-core transformers and is a plug-in unit embedded in plastic. The external dimensions are 5-1/2" by 1-7/8" by 2-5/8".

July 31, 1953

Prepared by: John W. Brean
John W. Brean

Approved by: John E. Ward
John E. Ward

PROJECT GRIND REPORT

ON

THE HIGH SPEED GATE CIRCUIT

Eugene Breiding
Robert Lindsay

6/30/53

THE LINCOLN TX-2 COMPUTER

LINCOLN LABORATORY

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

PRESENTED AT:

THE WESTERN JOINT COMPUTER CONFERENCE
LOS ANGELES FEBRUARY 1957

THE RESEARCH REPORTED IN THIS DOCUMENT WAS SUPPORTED JOINTLY BY THE ARMY, NAVY, AND AIR FORCE UNDER CONTRACT WITH THE MASSACHUSETTS INSTITUTE OF TECHNOLOGY

MONOSTROPHIC CODES

A Thesis

Presented to

the Faculty of the Department of Electrical Engineering

Northeastern University

In Partial Fulfillment

of the Requirements for the Degree of

Master of Science

---

by

Dale Sherwood Cockle

June, 1964

MONOSTROPHIC CODES

A Thesis

Presented to

the Faculty of the Department of Electrical Engineering

Northeastern University

In Partial Fulfillment

of the Requirements for the Degree of

Master of Science

---

by

Dale Sherwood Cockle

June, 1964

A TRANSISTOR SELECTION SYSTEM FOR A MAGNETIC-CORE MEMORY

by

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Department of Electrical Engineering, January 16, 1956

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Chairman, Departmental Committee on Graduate Students

DIGITAL EQUIPMENT CORPORATION

This report is submitted in partial fulfillment of course requirements at the Harvard Business School for the spring term of the academic year 1957-58.

ACKNOWLEDGEMENTS

We wish to express our gratitude to the two officers of the Digital Equipment Corporation, Mr. Kenneth Olsen and Mr. Harlan Anderson, for their ready permission and full cooperation during this study of the problems and operations of this new enterprise. The ready assistance of Mr. Anderson, during these early months of operations when company demands on his time and efforts were very pressing, was especially appreciated. We feel that we have been fortunate to observe the efforts of two such capable young entrepreneurs entering a relatively new and complex technical field. We extend our wishes for their success in their future business endeavors.

Donald N. Decof

Theodore G. Johnson

6D-2631

TX-2 CIRCUITRY HANDBOOK*

A discussion of the
circuitry used in the
Lincoln TX-2 Computer.

Jonathan R. Fadiman**

1 October, 1958

* The research reported in this document was supported jointly by the Army, Navy, and Air Force under contract with the Massachusetts Institute of Technology.

** Lincoln Laboratory, Massachusetts Institute of Technology.

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Research Laboratory of Electronics

Technical Report No. 65

March 17, 1949

THE TRANSMISSION OF INFORMATION

Robert M. Fano

Abstract

This report presents a theoretical study of the transmission of information in the case of discrete messages and noiseless systems. The study begins with the definition of a unit of information (a selection between two choices equally likely to be selected), and this is then used to determine the amount of information conveyed by the selection of one of an arbitrary number of choices equally likely to be selected. Next, the average amount of information per selection is computed in the case of messages consisting of sequences of independent selections from an arbitrary number of choices with arbitrary probabilities of their being selected. A recoding procedure is also presented for improving the efficiency of transmission by reducing, on the average, the number of selections (digits or pulses) required to transmit a message of given length and given statistical character. The results obtained in the case of sequences of independent selections are extended later to the general case of non-independent selections. Finally, the optimum condition is determined for the transmission of information by means of quantized pulses when the average power is fixed.

A STUDY OF THRESHOLD DETECTION

by

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S.B., Purdue University
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A SEMICONDUCTOR REGULATED POWER SUPPLY

by

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THE DESIGN OF HIGH SPEED ANALOG SAMPLE AND STORAGE GATES

by

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MASSACHUSETTS INSTITUTE OF TECHNOLOGY

LINCOLN LABORATORY

PLATED COMPONENT CONNECTIONS FOR MICRO-MINIATURE CIRCUITS

Elis A. Guditz

Approved

Group Report No. 51-4

March 19, 1959

The work reported in this document was performed by Lincoln Laboratory, a technical center operated by Massachusetts Institute of Technology with the joint support of the U.S. Army, Navy, and Air Force under Air Force Contract AF19(604)-5200

LEXINGTON MASSACHUSETTS

SEARCH PROCEDURES BASED ON MEASURES OF RELATEDNESS BETWEEN DOCUMENTS

by

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Copy 152

NEW TECHNIQUES AND EQUIPMENT FOR CORRELATION COMPUTATION

Technical Memorandum
7668-TM-2

James F. Kaiser and Roy K. Angell

December 1957

Contract AF 33(616)-3950
Task 50678

The research reported in this document was made possible through the support extended the Massachusetts Institute of Technology, Servomechanisms Laboratory, by the United States Air Force (Weapons Guidance Laboratory, Wright Air Development Center), under Contract No. AF 33(616)-3950, M.I.T., Project No. D.S.R. 7668. It is published for technical information only and does not represent recommendations or conclusions of the sponsoring agency.

Approved John E. Ward

Servomechanisms Laboratory
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Massachusetts Institute of Technology

A STUDY OF HIGH-SPEED MULTIPLIERS

by

W. A. Klein

DIGITAL COMPUTER LABORATORY

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

CAMBRIDGE 39, MASSACHUSETTS

JULY 1954

HOLE STORAGE IN A SATURATED GROUNDED-EMITTER TRANSISTOR CIRCUIT

by

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A DIFFERENTIAL THERMAL ANALYSIS STUDY OF SYNTHESIZED MAGNESIUM FERRITE, MANGANESE FERRITE, AND MAGNESIUM-MANGANESE FERRITE

by

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MASSACHUSETTS INSTITUTE OF TECHNOLOGY

39

LINCOLN LABORATORY

SURVEY OF MEMORY TECHNIQUES USING TRANSISTORS

R. E. McMahon

2G-24-82

1 October 1957

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

LEXINGTON MASSACHUSETTS

A MAGNETIC MATRIX SWITCH

AND

ITS INCORPORATION INTO A COINCIDENT-CURRENT MEMORY

by

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REQUIREMENTS FOR THE DEGREE OF
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A MAGNETIC MATRIX SWITCH

AND

ITS INCORPORATION INTO A COINCIDENT-CURRENT MEMORY

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Preliminary Draft

For Joint Eastern
Computer Conference,
December, 1953

William N. Papian
November 10, 1953

THE MIT MAGNETIC-CORE MEMORY

One recent development which is significantly raising the reliability of today's high-speed automatic digital computer is the multicoordinate magnetic-core memory. Two banks of 32 by 32 by 17 magnetic-core memory have been in full-time computer operation at the MIT Digital Computer Laboratory for some months. A description of the units and of the tests and operational data available on them will be preceded by a short review of the operating principles of this type of memory.

1. OPERATING PRINCIPLES[1]

Each binary digit is stored in the stationary magnetic field of a small, ring-shaped, ferromagnetic core. Two aspects of the core's rectangular flux-current characteristic are utilized:

a. The flux remanence of the core is utilized for the storage operation;[2]

b. The extreme nonlinearity of the flux-current characteristic is utilized to advantage in the selection operation.[3,4]

Fig. 1 shows the flux-current loop for a ferrite core. The remanent flux points are arbitrarily designated as ZERO and ONE. Note that the loop is sufficiently nonlinear so that the application of $I_m/2$ cannot switch the core, whereas the full I_m can. Fig. 2 illustrates how this nonlinearity may be used to select one core out of many by the coincidence of two half-currents in a 2-coordinate scheme. The extension to three coordinates may be accomplished by stacking planes like those of Fig. 2 behind each other and connecting respective x and y coordinate lines in common to obtain a "volume" of cores as sketched in Fig. 3.

The application of a half current to the coordinate x_0 results in the half excitation of a "selection plane" through the volume.

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LINCOLN LABORATORY

Memorandum No. 2G-24-76

To: E. W. Bivans

From: K. E. Perry and E. J. Aho

Subject: A Fourier Synthesis Character Generator

ABSTRACT

An analog device has been developed for displaying alphabetic or numeric characters on a cathode-ray tube face by deflecting the spot so that it traces out the character smoothly and continuously. The necessary "x" and "y" deflection voltages are obtained by a Fourier synthesis technique that involves combining various harmonic frequencies of a fundamental frequency. A single character is displayed in about thirty microseconds.

Date: 1 April 1957

Rec'd 2 May 1957

Signed K. E. Perry
E. J. Aho
Authors

Approved Paul B. Fellows

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LINCOLN LABORATORY

TRANSISTOR REGULATED POWER SUPPLIES

F.G. Popp

Group 24

Technical Report No. 106

19 January 1956

ABSTRACT

A method of designing power supplies utilizing power transistors as series-regulating elements and silicon diodes as voltage references is described. Information is given on efficiency, output impedance, regulation, ripple reduction and limits on output voltage and output power. Several variations of circuit design are given as well as circuit schematics for power supplies already in operation.

LEXINGTON MASSACHUSETTS

A HIGH-SPEED ANALOG-TO-DIGITAL ENCODER

by

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Chairman, Departmental Committee on Graduate Students

MAGNETIC RELAXATION IN THIN FILMS

Donald O. Smith

Lincoln Laboratory, Massachusetts Institute of Technology
Lexington, Massachusetts

THE LOGICAL DESIGN OF

A DIGITAL AVERAGE RESPONSE COMPUTER

by

Barbera Wertz Stephenson

SUBMITTED IN PARTIAL FULFILLMENT OF THE

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June, 1961

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SKETCHPAD, A MAN-MACHINE GRAPHICAL COMMUNICATION SYSTEM

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SUBMITTED IN PARTIAL FULFILLMENT OF THE

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MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LINCOLN LABORATORY

DESIGNING FOR RELIABILITY

N. H. Taylor

Division 6

Technical Report No. 102

9 December 1956

LEXINGTON MASSACHUSETTS

PEPR and Other Systems

A. H. Rosenfeld

University of California
Berkeley, California

and

H. D. Taft

Yale University
New Haven, Connecticut

This report represents an attempt to present a logical sequence of programs leading from bubble chamber film through the complete kinematical analysis of events. Since a number of systems already exist to handle the latter part of this problem, the emphasis here is placed upon the automatic scanning and measuring problem as well as upon the preparation of the data for the existing systems. In particular, Part I of this report is a detailed proposal for programming the Precision Encoder and Pattern Recognition device (PEPR) at present under development at MIT.[1] Part II contains a review of the leading automatic scanning and measuring systems as well as a proposal for unifying the output of these systems and processing this output. It is interesting to us that it now appears to be possible to outline a complete program which encompasses automatic scanning, measuring, and pattern recognition by relatively straight forward methods without recourse to any very sophisticated ideas or any theorems about the "discipline" of pattern recognition.

PART I - A Program of PEPR

Overall Program:

The proposed preliminary program for PEPR consists of three principal phases. Phase 1 consists of two orthogonal area scans designed to establish one

6R-235

MULTI-COORDINATE SELECTION SYSTEMS FOR MAGNETIC-CORE STORAGE

R. S. DiNolfo

The research reported in this document was supported jointly by the Dept. of the Army, the Dept. of the Navy, and the Dept. of the Air Force under Air Force Contract No. AF 19 (122)-458.

division 6 · lincoln laboratory · MIT · lexington 73, massachusetts

August 1954

Approved

R. R. Everett

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I am grateful to Mr. Dudley A. Buck and Prof. W. K. Linvill for undertaking the supervision of this thesis; to Mr. Jack Raffel for his careful criticism of the original manuscript; and to the staff of Division 6, Lincoln Laboratory, without whose aid this thesis work would have been impossible.

I wish to express special appreciation to the members of the Test Equipment Group and to Mrs. Hilda Carpenter through whose co-operation the experimental work was done with a minimum of delay; to Miss Rosemarie Balian, Mrs. Jean Devereaux, Miss Mary Matas, and Miss Anne Sullivan; and to all those in the Drafting Room and Publications Office who were unfailingly patient.

Report 6R-235

ABSTRACT AND FOREWORD

For many computational applications there is a need for a high-speed digital computer with a large internal memory capacity. The search for a reliable random-access memory with a fast information-access time brought about the development of the magnetic-core memory system. Systems of this type using a 2-coordinate "read" and 3-coordinate "write" have been operating very successfully for some time.

This thesis report reviews and extends the theory of magnetic-core memories for the generalized n-coordinate selection system. The criteria for obtaining the maximum selection ratio under a variety of conditions and arrangements are derived, and the resultant effects on the noise and sensing problem are discussed.

A particular system which uses a 4-coordinate read and 5-coordinate write in an attempt to reduce the number of required electronic circuits is analyzed. Experimental work with the breadboard of such a system (using a 3-to-2 selection-current ratio) was performed. The results, here indicated, show that a 4096-bit digit plane (8 driving lines in each of the 4 coordinates) is operable, albeit with very narrow margins, with a memory cycle time of approximately 9 microseconds, and with no more than one-fourth the number of driving cathodes required by a comparable system which uses a 2-coordinate read and a 3-coordinate write. The recent development of improved cores and diodes satisfactory for low-level mixing of memory signals could be used to improve the operating margins significantly.

Report 6R-235

Because it presents information of general interest, this thesis report, which has had only very limited distribution, is being issued as a Division 6 R-Series Report.

R. S. Di Nolfo

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LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS
(continued)

PART I

THE THEORY OF CORE MEMORY SYSTEMS

CHAPTER 1

SELECTION

1.01 The Basic Problems

To illustrate more clearly the basic concepts involved in random access magnetic-core memory systems, this section on the theory of selection will be developed for idealized memory elements. However, all that is derived for this case will apply directly or with slight modifications to the actual case.

The memory element to be considered is a ferromagnetic toroid which has nearly rectangular hysteresis loops. For binary storage* two remanent flux states of the core are used to represent the two digits, ZERO and ONE, as defined for the hysteresis loop of Fig. 1.01a.

In using an array of these elements as a storage medium, it is necessary that the system be able to perform two functions. The first is determining the information state of one or more cores, and the second is putting these cores in a desired information state; both of these being done without affecting the information state of the other cores in the array. An operation of the first type will be referred to as "reading" and that of the second type as "writing."

From a study of Fig. 1.01a, a suitable read operation may be defined as exciting the selected core with a pulse of current of maximum

---

*Only binary storage will be considered in this thesis.

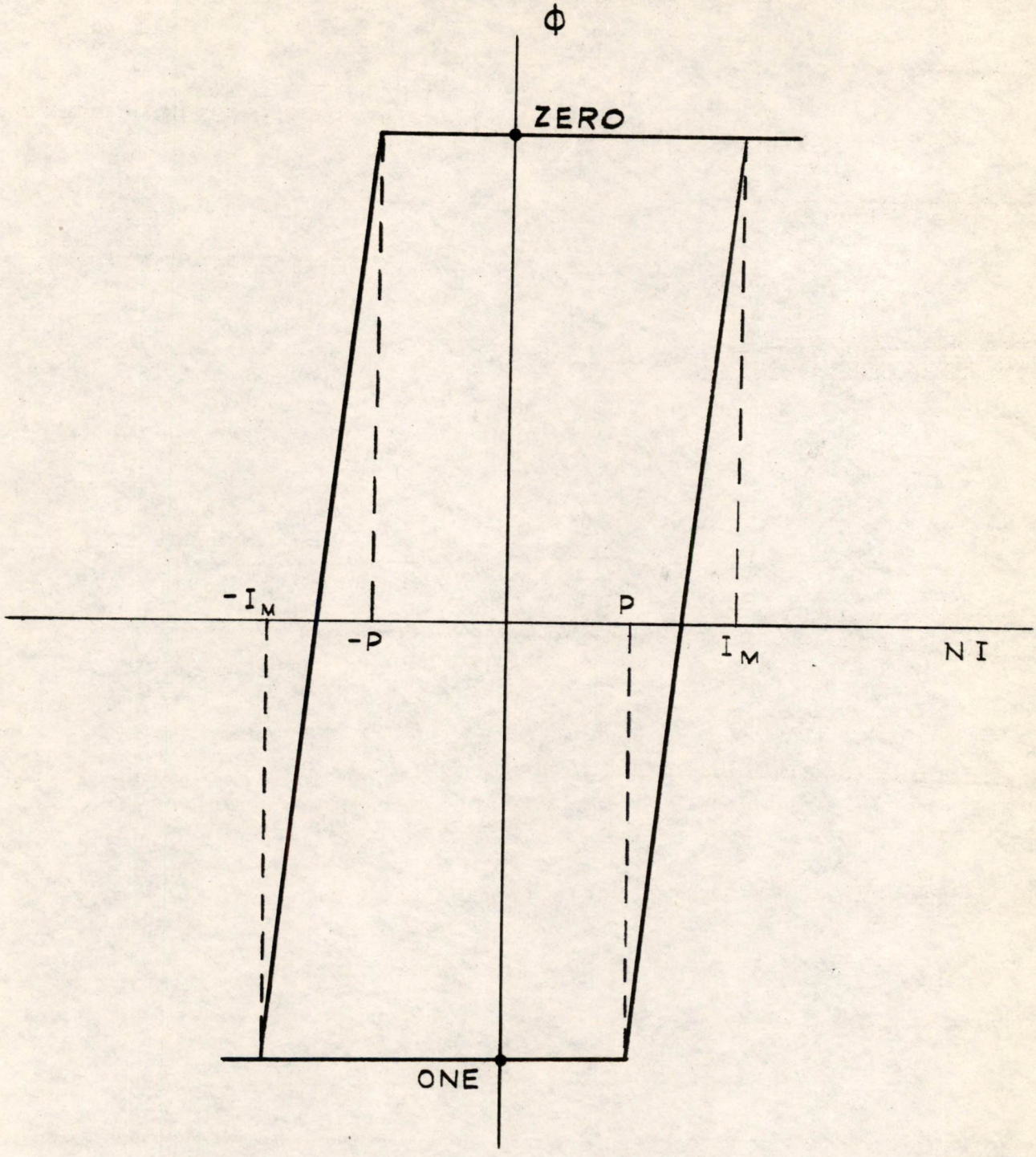


FIG. 1.01 a

HYSTERESIS LOOP OF AN IDEAL MEMORY CORE

A-59648

amplitude I_m, while restricting the excitations of the unselected cores to less than P and greater than -P. If a selected core is in the ONE state, it will "switch" to the ZERO state, resulting in a net change in flux, whereas if it is originally in the ZERO state, it will reassume its original state after the read operation with no change in flux. The flux state of all unselected cores will remain unchanged. If a "sense" winding is passed through a selected core, the reading of a ONE will induce a voltage in the winding, whereas the reading of a ZERO will induce no voltage in the winding. Voltage or flux amplitude discrimination can be used to distinguish a ONE from a ZERO, the first technique being a measure of the time derivative of flux. These two methods of detection will be discussed and compared more fully in the next chapter.*

Since after reading, a core in the ONE state will be left in the ZERO state, the read operation is destructive.** Consequently, if a core is to be left in the ONE state, the read must be followed by a write consisting of exciting the core with a pulse of current of maximum amplitude $-I_m$. Again the excitations of all unselected cores must be restricted to less than P and greater than -P.

1.02 Necessary and Redundant[3] Coordinates

As a basis for further discussion of selection systems, three definitions will be made at this point.

Definition 1: A coordinate of a selection system is a group of driving lines which do not intersect at any core within the array.

---

*See Section 2.03.

**Only the destructive read described will be discussed in this thesis. Non-destructive reads have been devised and the reader is referred to References 1 and 2.

Definition 2: A coordinate of a selection system is a necessary coordinate if upon removing it the same selection cannot be accomplished by an adjustment of the excitations in the remaining coordinates.

Definition 3: A coordinate of a selection system is a redundant coordinate if upon removing it the same selection can be accomplished by an adjustment of the excitations in the remaining coordinates.

To illustrate the definitions given above, first consider Fig. 1.02a. If an X, Y, and Z driving line are chosen, it is possible, with the proper choice of excitations, to select the one core lying at the intersection of the three selected lines without destroying the information states of the other cores. However, if any one of the three coordinates is removed (Fig. 1.02b), it is impossible to select only a single core for each choice of driving lines in the remaining coordinates since any line of one coordinate intersects those of another more than once. Therefore, the three coordinates of this system are nonredundant.

Fig. 1.02c shows a redundant system. Any one of the three coordinates is redundant since it may be removed (Fig. 1.02d) and the same selection accomplished, i.e., any core can be selected singly by an adjustment of excitations in the remaining coordinates.

The remainder of this thesis will be confined to the analysis of nonredundant systems, and the word coordinate without further qualification implies necessary coordinate.

1.03 p_{min} as a Function of the Number of Coordinates[3]

Consider an n-coordinate system which is capable of selecting a single core from an array of cores. Each core is at the intersection of n driving lines, one in each coordinate, and a core is selected by exciting one line in each coordinate such that the sum of the excitations

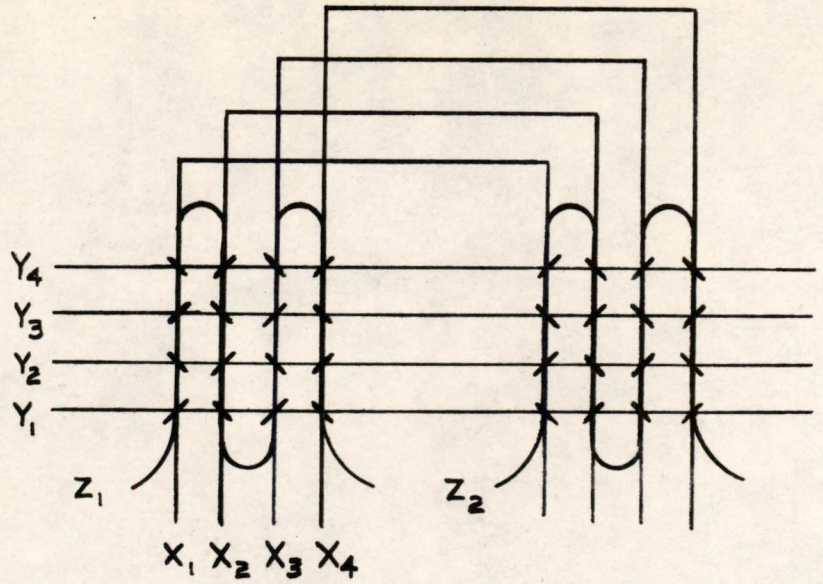


FIG. 1.02 a

A NONREDUNDANT SELECTION SYSTEM

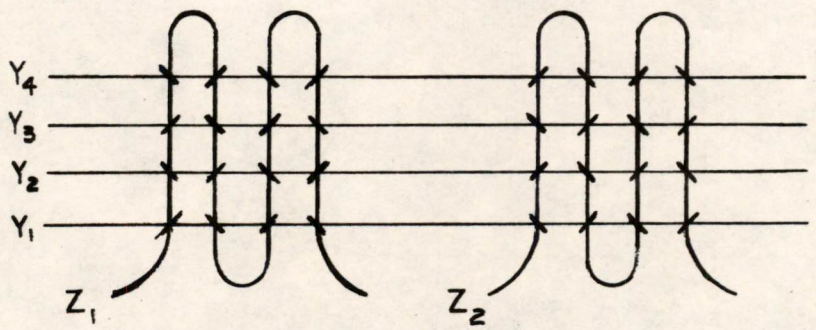


FIG. 1.02 b

THE SYSTEM OF FIG. 1.02 a

WITH THE X COORDINATE REMOVED

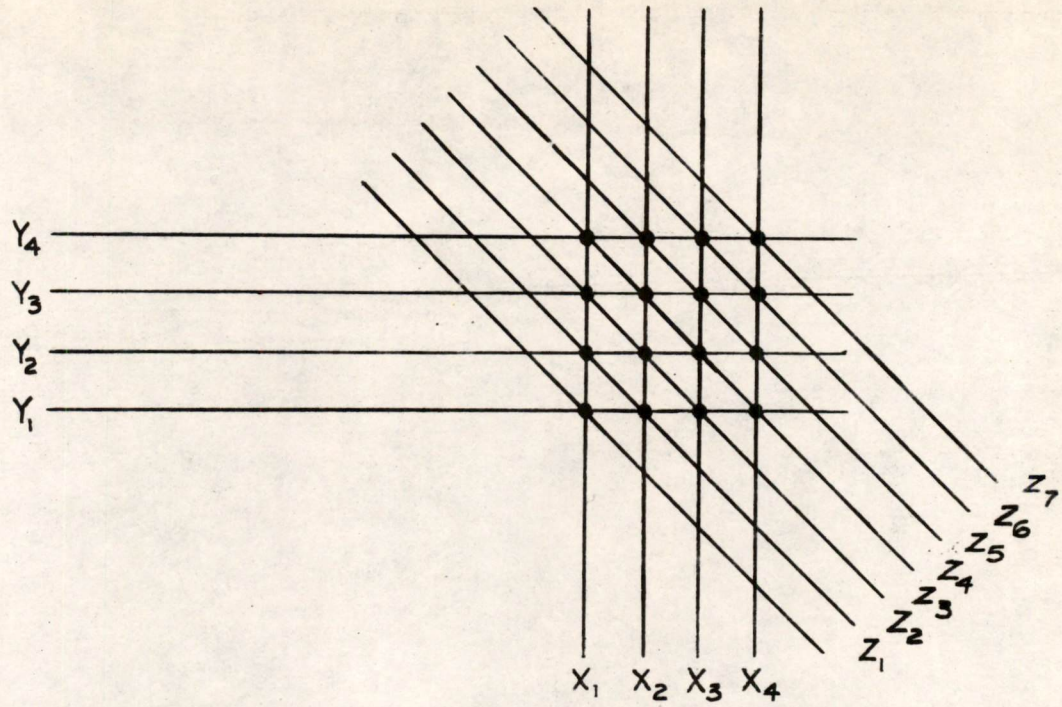


FIG. 1.02 c

A REDUNDANT SELECTION SYSTEM

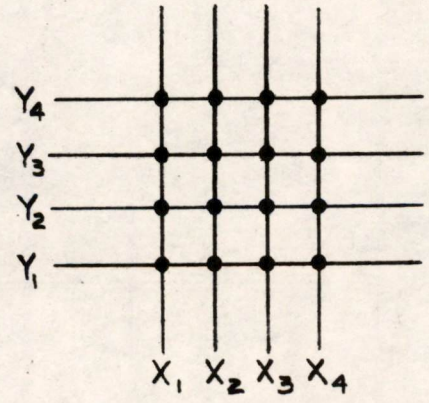


FIG. 1.02 d

THE SYSTEM OF FIG. 1.02 c
WITH THE Z COORDINATE REMOVED

is one unit. (See the hysteresis loop of Fig. 1.03a.) All other driving lines are excited so that at any other core the total excitation is less than p and greater than -p. The lines passing through the selected core will be termed selecting lines, and all other lines unselecting lines. For this system the minimum required value of p (p_{min}) is of interest since it places the least requirement on the rectangularity of the hysteresis loop, and this can be easily found in the following manner:

Since one and only one driving line from each coordinate passes through a core, if an equal amount is added to all the driving lines, selecting and unselecting, of any one coordinate, the excitation of all the cores will be changed by this amount. Let s_j be defined as the value of the excitation of the selecting line in the jth coordinate, and let u_j be defined as the value of the excitations of the unselecting lines in the same coordinate. By adding $-s_j$ to the excitations of all the driving lines in the jth coordinate, the excitation on all the cores will change by $-s_j$. If this process is repeated for all n coordinates, i.e., $-s_k$ is added to the driving lines of the kth coordinate, etc., the excitation on all the cores will diminish by one unit since as previously stated the sum of the selecting excitations is unity, $\sum_{j=1}^{n} s_j \triangleq 1$.

Passing through any unselected core there can be a minimum of one and a maximum of n unselecting lines, and if the above procedure were to be carried out, the maximum excitation on an unselected core would be $-U_j$ and the minimum excitation would be $-\sum_{j=1}^{n} U_j$, where

$$U_j \triangleq -(u_j - s_j) \cong s_j - u_j;\ j \cong 1, 2, \cdots, n \qquad (1)$$

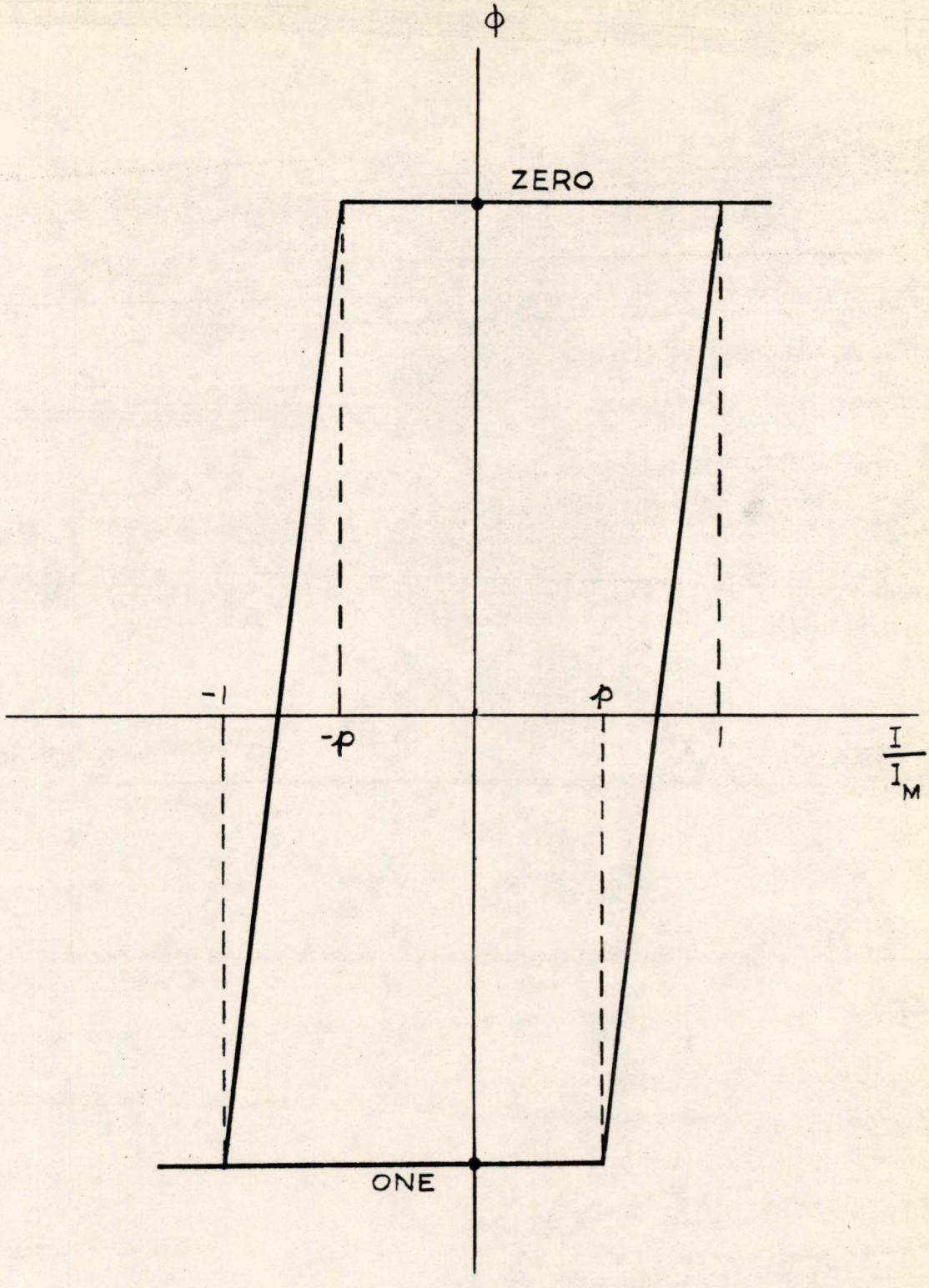


FIG. 1.03a

HYSTERESIS LOOP OF AN IDEAL MEMORY CORE

A-59645

Therefore, for the original system, the maximum excitation on an unselected core is $1-U_j$ and the minimum excitation is $1-\sum_{j=1}^{n} U_j$. From a consideration of the hysteresis loop (Fig. 1.03a), the restrictions on the system are

$$1-U_j \leq p \tag{2}$$

and

$$1-\sum_{j=1}^{n} U_j \geq -p \tag{3}$$

or subtracting one from both sides of inequality 1.03-(2) and summing from j=1 to j=n,

$$-\sum_{j=1}^{n} U_j \leq -n(1-p) \tag{4}$$

and subtracting one from both sides of inequality 1.03-(3),

$$-\sum_{j=1}^{n} U_j \geq -(1+p) \tag{5}$$

Combining inequalities 1.03-(4) and 1.03-(5)

$$-n(1-p) \geq -(1+p) \tag{6}$$

$$p \geq \frac{n-1}{n+1} \tag{7}$$

and therefore,

$$p_{min} = \frac{n-1}{n+1} \tag{8}$$

When the selection ratio (R) is defined as the excitation applied to the selected core divided by the maximum excitation applied to any unselected cores,

$$R_{max} = \frac{1}{p_{min}} = \frac{n+1}{n-1} \tag{9}$$

1.04 Necessary Condition for R_{max}

Continuing the discussion of the previous section, the next step is to obtain the necessary condition for R_{max}. This is easily obtained from the inequalities 1.03-(4) and 1.03-(5) by a substitution of equation 1.03-(8).

$$-(1+p) \leq -\sum_{j=1}^{n} U_j \leq -n(1-p) \tag{1}$$

and

$$p_{min} = \frac{n-1}{n+1} \tag{2}$$

therefore

$$\frac{-2n}{n+1} \leq -\sum_{j=1}^{n} U_j \leq \frac{-2n}{n+1} \tag{3}$$

$$\sum_{j=1}^{n} U_j = \frac{2n}{n+1} \tag{4}$$

But from inequality 1.03-(2)

$$U_j \geq (1-p) = \frac{2}{n+1} \tag{5}$$

and therefore

$$U_j = \frac{2}{n+1} \tag{6}$$

To determine what restriction this imposes on the original n-coordinate selection system, equation 1.03-(1) is recalled and the final result is that

$$s_j - u_j = \frac{2}{n+1} \; ; \quad j = 1,2,\cdots n \tag{7}$$

is a necessary condition for a maximum selection ratio, and this constraint with the original constraint that

$$\sum_{j=1}^{n} s_j = 1 \tag{8}$$

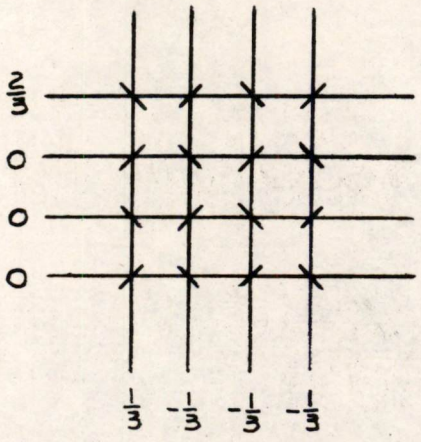
define the system. In a practical system the further restriction that

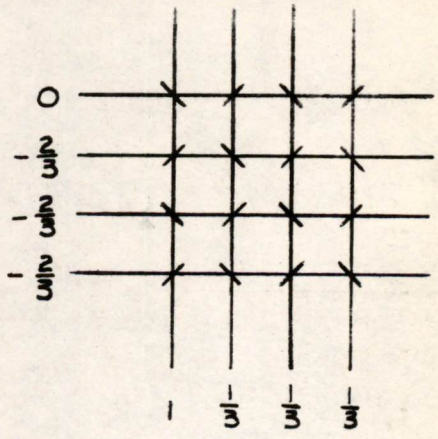
$$|u_j| \; ; \; |s_j| \leq \frac{2}{n+1} \tag{9}$$

is required to allow for variations in the times that the drivers take to reach maximum amplitude.

Fig. 1.04a shows two systems with a maximum selection ratio. Since in both cases n=2,

$$R_{max} = \frac{n+1}{n-1} = \frac{3}{1} \tag{10}$$





1	1/3	1/3	1/3
1/3	-1/3	-1/3	-1/3
1/3	-1/3	-1/3	-1/3
1/3	-1/3	-1/3	-1/3

1	1/3	1/3	1/3
1/3	-1/3	-1/3	-1/3
1/3	-1/3	-1/3	-1/3
1/3	-1/3	-1/3	-1/3

EACH NUMBER IN THE TABLES CORRESPONDS TO THE EXCITATIONS RECEIVED BY THE CORES IN THE SIMILAR POSITIONS IN THE ARRAY.

FIG. 1.04a

EXAMPLES OF 2-COORDINATE SYSTEMS

A-59643

and

$$s_j - u_j = \frac{2}{n+1} = \frac{2}{3} \tag{11}$$

By comparing the tables it should be noted that the distributions of excitations are identical. For any two nonredundant systems of the same n, this is always the case when the conditions for a maximum selection ratio are adhered to. This is implied in equation 1.04-(4), and is more readily seen in equation 1.04-(6).

1.05 The Choice of u_j and s_j

In the previous section it was shown that the only restrictions on s_j and u_j are:

$$-(1+p) \leq \sum_j^n u_j - s_j \leq -n(1-p) \tag{1}$$

and

$$\sum_{j=1}^{n} s_j = 1 \tag{2}$$

However, it is desirable to make either the unselecting or the selecting excitations zero in as many coordinates as possible since this system will require the smallest number of drivers. The following is a derivation of the best possible selection ratio that can be obtained when this is done, and it will be shown that this ratio cannot always be made equal to R_{max}.

Let N_u be the number of coordinates in which the excitations of the unselecting lines are zero, and let N_s be the number of coordinates

in which the excitation of the selecting line is zero. Then,

$$N_u + N_s = n \tag{3}$$

A study of Section 1.03 shows that for the best possible selection ratio

$$U_1 = U_2 = \cdots = U_n \triangleq U \tag{4}$$

since

$$R \cong \frac{1}{1-U_j} \tag{5}$$

Therefore,

$$s_j - u_j \cong U \; ; \; j = 1, 2, \cdots n \tag{6}$$

But in each coordinate either u or s is zero, and therefore, either

$$u \cong -U \tag{7}$$

or

$$s = U \tag{8}$$

with the least allowable value of p being correspondingly

$$p = 1+u \cong 1-s \tag{9}$$

Substituting the previous expressions into inequality 1.05-(1) and equation 1.05-(2), the conditions become

$$-(1+1-s) \leq n\,U \leq -n(1-1+s) \tag{10}$$

$$-(2-s) \leq n\,U \leq -ns \tag{11}$$

$$-(2-s) \leq -ns \leq -ns \tag{12}$$

$$-(2-s) + ns \leq o \tag{13}$$

$$-2 + (n+1)\, s \leq o \tag{14}$$

and

$$N_s\, s = 1 \text{ or } s = \frac{1}{N_s} \tag{15}$$

Substituting for s in 1.05-(14)

$$-2 + (n+1)\,\frac{1}{N_s} \leq o \tag{16}$$

$$N_s \geq \frac{n+1}{2} \tag{17}$$

and since

$$N_s = n - N_u \tag{18}$$

$$N_u \leq \frac{n-1}{2} \tag{19}$$

By combining equation 1.05-(5), (9) and (15), the best possible selection ratio can be expressed as

$$R = \frac{N_s}{N_s - 1} \tag{20}$$

where N_s is as small an integer as possible. When n is an even integer, the smallest integral value N_s can take on is

$$N_s = \frac{n+2}{2} \tag{21}$$

and correspondingly,

$$N_u = \frac{n-2}{2} \tag{22}$$

The best possible selection ratio is then

$$R(n) = \frac{n+2}{n} = R_{max}\,(n+1) \tag{23}$$

However, if n is an odd integer,

$$N_s = \frac{n+1}{2} \tag{24}$$

and

$$N_u = \frac{n-1}{2} \tag{25}$$

giving a best possible selection ratio of

$$R(n) = \frac{n+1}{n-1} = R_{max}(n) \tag{26}$$

Considering the case when n is an even integer, the value of U_j can be obtained from substituting equation 1.05-(23) into equation 1.05-(5).

$$U_j = 1 - \frac{n}{n+2} = \frac{2}{n+2} \tag{27}$$

For the case of n equal to an odd integer U_j is as given in equation 1.04-(6)

$$U_j = \frac{2}{n+1} \tag{28}$$

Therefore,

$$s_j - u_j = \begin{cases} \frac{2}{n+2} & \text{for even } n \\ \frac{2}{n+1} & \text{for odd } n \end{cases} \qquad (29)$$

1.06 Parallel-Digit Storage

Magnetic-core memories of the type described are ideal for parallel-type computers. In this case, a binary word of D digits is stored in the memory, all digits being stored simultaneously. The group of D cores in which the digits of a single word are stored is called a register, and the read operation consists of selecting all the cores of the selected register, whereas the write, which follows the read, consists of selecting only those cores of the register which are to be switched to the ONE state. The important point to note is that, in general, the write utilizes at least one more coordinate than the read, i.e., the read selects all the cores of the register whereas the write must discriminate between the different digits comprising a register.

Since only one register is selected at a time a single sense winding can pass through a given digit of all the registers. Generally, these cores on the same sense winding are placed in the same plane, and hence, the term "digit plane" is often used in reference to them.

All the derivations of the previous sections apply to systems of this type. The read selection and write selection are considered separately, the formulas being evaluated for the particular values of n, and in general, a system using an n-coordinate read will use an $(n+1)$-coordinate write.

1.07 An Economical Means of Doubling Memory Capacity for Even n*

Consider the special case discussed in Section 1.05 where either the selecting excitation or unselecting excitations in each coordinate are zero. For this case it will be shown that whenever n is even it is possible to double the selection capacity without doubling the number of drivers in a coordinate, but first the case for n=2 will be illustrated.

Referring to Fig. 1.07a, any core to the left of the dotted line can be selected by exciting the selected driving line in each coordinate with $I_j = \frac{1}{2}$, and any core to the right of the dotted line can be selected by exciting the selected line in one coordinate with $I_1 = \frac{1}{2}$ and the selected line in the other coordinate with $I_2 = -\frac{1}{2}$. Tabulated below the figure are the excitations for each case, and it is seen that the 2 to 1 selection ratio which would otherwise be obtained (equation 1.03-(9)) has not been affected.

At a first glance it would seem that nothing is gained since it is now necessary to have drivers of the opposite polarity, and the same effect could be obtained by just doubling the number of driving lines in a coordinate. However, when it is recalled that in a system, both read and write drivers are need, and that a write excitation can be made equal in magnitude but opposite in polarity to a read excitation, the benefits of the system are seen. To obtain the desired effect, it is only necessary to use the write drivers of one coordinate during the read cycle when the cores to the right of the dotted line are to be selected.

Consider again the case of Section 1.05, but now for any n.

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*This was first pointed out to the author for the case when n=2 by D. A. Buck.

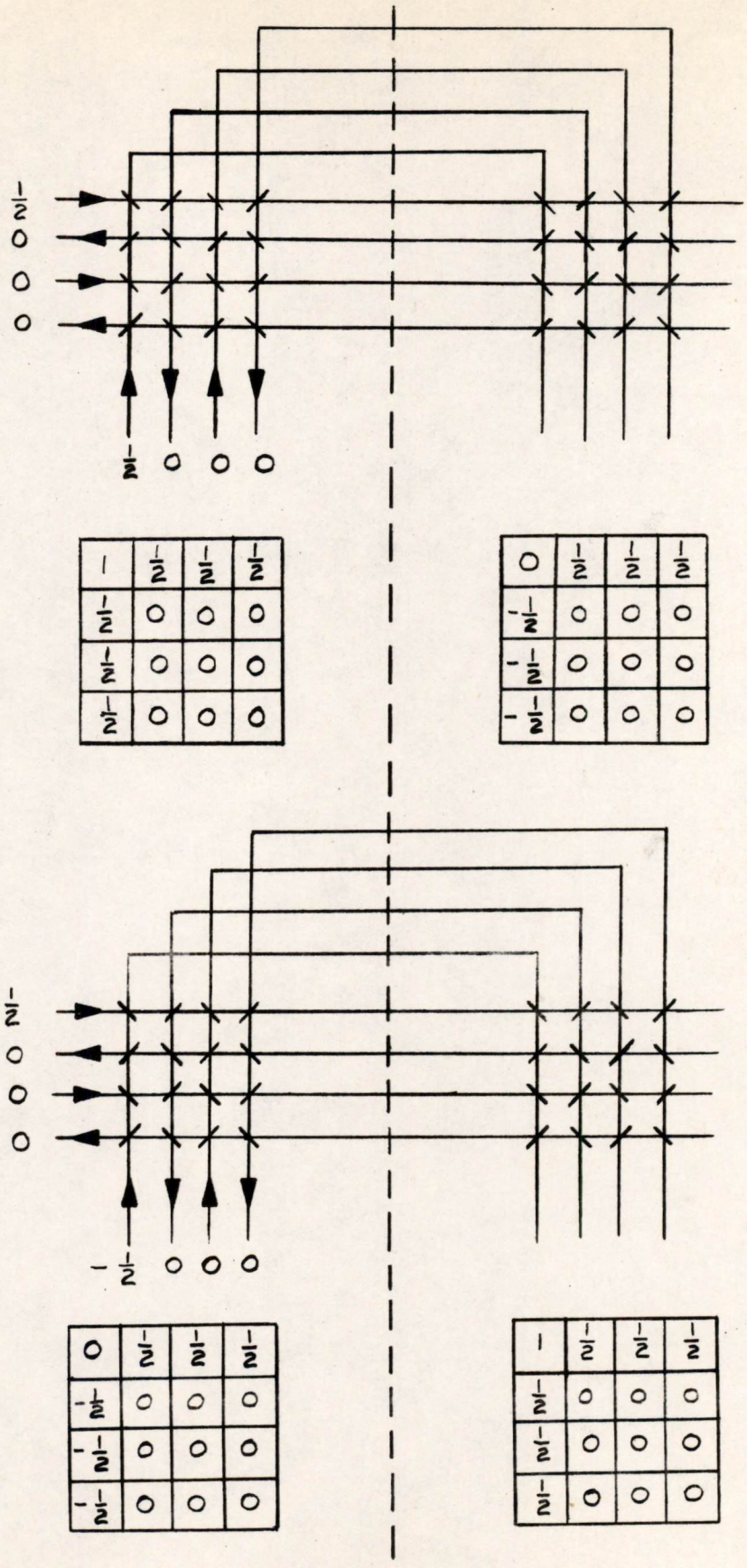

FIG. 1.07a

DOUBLING MEMORY CAPACITY FOR EVEN n

The maximum excitation is received by the selected core, and the value of this excitation is unity for both odd and even n. However, the minimum excitation any core receives is a function of n, and this function is not the same for odd and even n. The minimum excitation is

$$N_u\left[\frac{-2}{n+2}\right] \cong \frac{n-2}{2} \cdot \frac{-2}{n+2} \cong -\frac{n-2}{n+2} \text{ for even n} \qquad (1)$$

and

$$N_u\left[\frac{-2}{n+1}\right] \cong \frac{n-1}{2} \cdot \frac{-2}{n+1} \cong -\frac{n-1}{n+1} \text{ for odd n} \qquad (2)$$

Also, the best possible selection ratios are

$$R(n) \cong \frac{n+2}{n} \text{ for even n} \qquad (3)$$

and

$$R(n) \cong \frac{n+1}{n-1} \text{ for odd n} \qquad (4)$$

Now, consider reversing the polarity of just one of the selecting lines. Then the maximum excitation any core receives is now also a function of n and is

$$\left[N_s-1\right]\left[\frac{2}{n+2}\right] \cong \frac{n}{2} \cdot \frac{2}{n+2} = \frac{n}{n+2} \text{ for even n} \qquad (5)$$

and

$$\left[N_s-1\right]\left[\frac{2}{n+1}\right] \cong \frac{n-1}{2} \cdot \frac{2}{n+1} = \frac{n-1}{n+1} \text{ for odd n} \qquad (6)$$

and the minimum excitation is now

$$N_u \left[\frac{-2}{n+2}\right] + 1 \left[\frac{-2}{n+2}\right] = \left[\frac{n-2}{2}\right]\left[\frac{-2}{n+2}\right] - \frac{2}{n+2} = \frac{-n}{n+2} \text{ for even } n \quad (7)$$

and

$$N_u \left[\frac{-2}{n+1}\right] + 1 \left[\frac{-2}{n+1}\right] = \left[\frac{n-1}{2}\right]\left[\frac{-2}{n+1}\right] - \frac{2}{n+1} = -1 \text{ for odd } n \quad (8)$$

The best possible selection ratio for even n is still

$$R(n) = \frac{n+2}{n} \quad (9)$$

However, a system of odd n is no longer possible because of the possibility of the -1 excitation destroying the information stored in the array. Therefore, only when n is even is it possible to reverse the polarity of one selecting line without affecting the information state of the array. This fact plus the fact that two driving lines can be passed through a core such that the total excitation is either the sum or difference of the two separate excitations makes it possible, when n is even, to double the selection capacity without doubling the number of drivers in a coordinate.

The read selection is done by an even coordinate system and no additional drivers are necessary to read the information in the additional registers. However, since the write is one coordinate more than the read, the write selection will be done by an odd coordinate system, and, therefore, the number of drivers in one write coordinate must be doubled to write in the additional registers. Consequently, the total memory capacity can be doubled by doubling the number of drivers in just a write coordinate.

1.08 External Selection

No mention has been made yet of the means of selecting the driving lines within a memory coordinate. Generally, the initial selection in each coordinate is done by f_j bi-stable elements, where f_j is an integer related to d_j, the number of driving lines in the jth coordinate, by the equation

$$2^{f_j} = d_j \; ; \quad j = 1,2, \cdots n \tag{1}$$

Therefore, the external selection problem is that of going from an f_j coordinate system of two driving lines per coordinate to a one coordinate system of d_j driving lines. Except for the trivial case when d_j is equal to two, an intermediate system is necessary for performing this conversion. Usually it consists of a diode matrix switch [4,5], and its associated buffer amplifiers selecting gated drivers which excite either the memory coordinate line(s) or the coordinate line(s) of a magnetic core matrix switch[6,7,8,9] which excites a memory coordinate line*.

A. Diode Matrix Switch

Figure 1.08a shows a schematic of a diode matrix where for each setting of the bi-stable elements one output will be positive with respect to all other outputs which are at approximately the same potential, and Fig. 1.08b shows a matrix where the opposite is true. By properly biasing the gated drivers and using the correct type of diode matrix, either one or all but one of the drivers can be made to conduct when they are gated on.

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*The core switch cannot be used when several memory coordinate lines are to be excited simultaneously. Also, the diode matrix is unnecessary when the number of switch coordinates equals f_j.

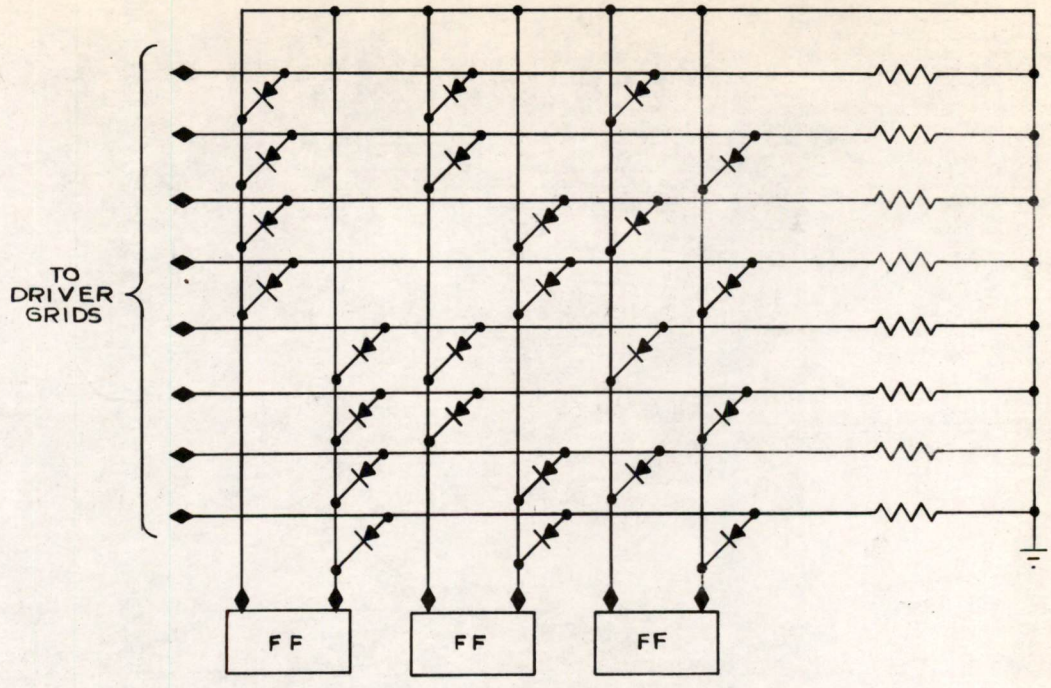


FIG. 1.08 a

CRYSTAL MATRIX FOR SELECTING A SINGLE DRIVER

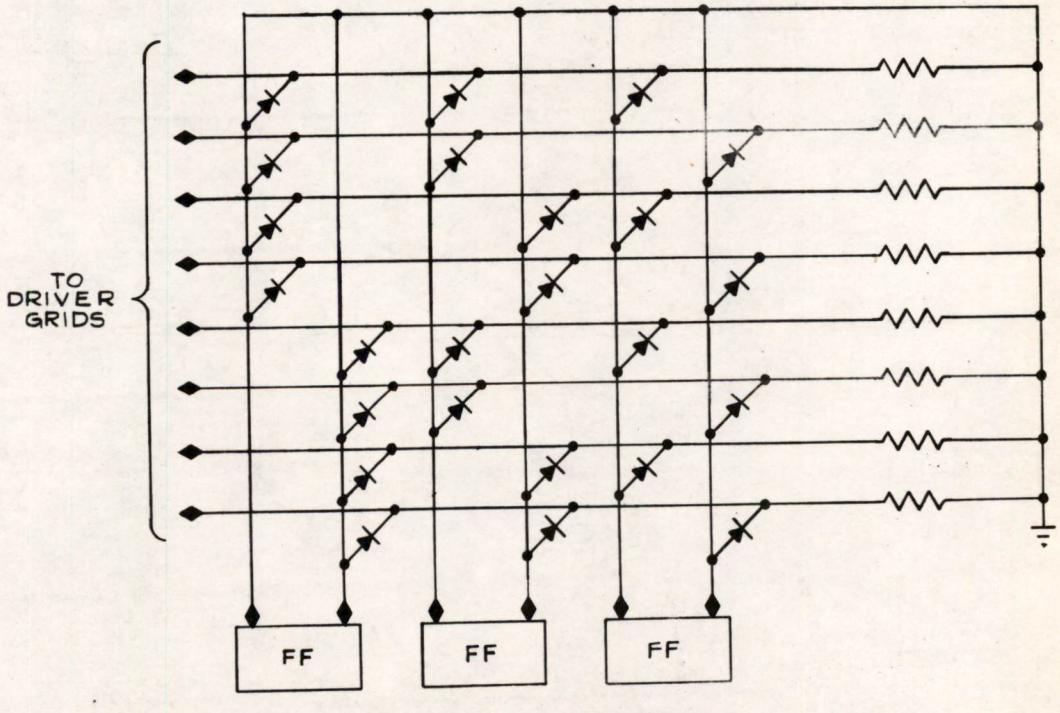


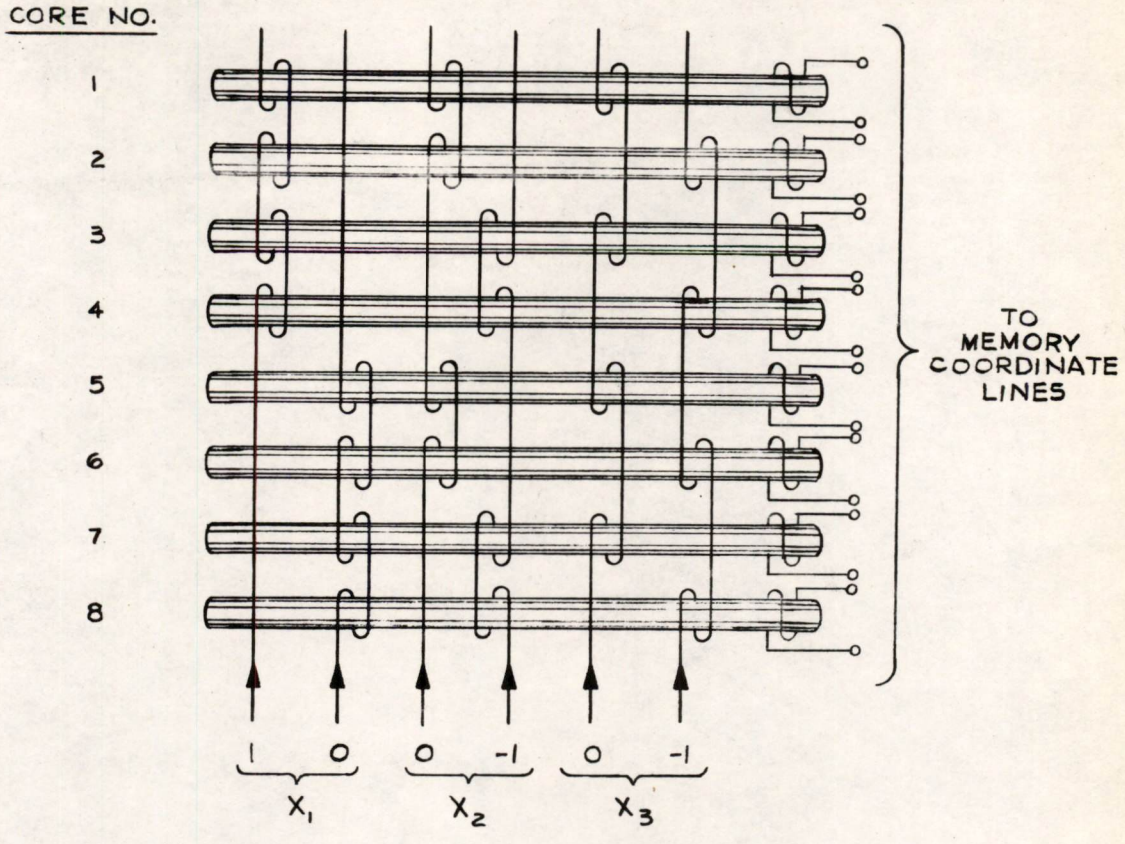
FIG. 1.08 b

CRYSTAL MATRIX FOR SELECTING ALL BUT ONE DRIVER

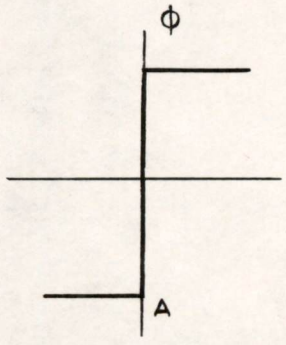
If the drivers are gated, this is another degree of selection in addition to that obtained from the diode matrix, and, therefore, each matrix output can be used to control the grid potential of more than one driver, each of these being selected by a different gate generator which is in turn selected by a bi-stable element.

B. Core Switch

Fig. 1.08c is a schematic of a magnetic core switch. The switch consists of an array of cores similar to the memory array, but unlike the memory, every core is in the same state at the beginning of each cycle (State A as shown in the figure). Therefore, the problem of selecting a single core from the switch core array is less severe than for the memory array. The only requirements are that the sum of the selecting excitations is equal to the switching current and that the unselecting excitations are of sufficient magnitude to bias all other cores so that they cannot switch. The outputs from the switch cores excite the memory lines directly, and the switch must be designed to give the proper outputs.



CORE NO.	EXCITATION
1	1
2	0
3	0
4	-1
5	0
6	-1
7	-1
8	-2



A HYSTERESIS LOOP
OF AN IDEAL SWITCH CORE

FIG. 1.08 c

A 3 — COORDINATE MAGNETIC CORE SWITCH

A-59647

CHAPTER 2

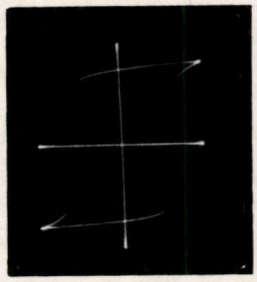
SENSING

2.01 The Sensing Problems

In the previous chapter a memory core was assumed to be in either one of two remanent-flux states referred to as the ONE and ZERO states, and it was assumed further that during the read operation only a fully excited core in the ONE state induced a voltage in the sense winding. These assumptions were made to simplify the discussion of the selection theory, but in doing so, the sensing problems involved in actual operation were hidden. If the hysteresis loop of Fig. 1.01a is assumed, the number of coordinates would seem to be limited only by the value of **P** and by the wire size and inside diameter of the cores, and there would seem to be no inherent limit to the memory capacity possible. However, if the actual hysteresis loops of the cores are considered, it is seen that deviations from the ideal loops impose limitations upon the memory.

Although the hysteresis loop traversed under pulse operation and the D.C. hysteresis loop differ, the remanent flux states are essentially the same,[10] and the shape of the D.C. loop does give a good indication of the suitability of a core material for memory application. Therefore, this more familiar and easily obtainable loop can be used in a qualitative discussion of sensing problems that arise in actual operation.

As can be seen in Fig. 2.01a, the hysteresis loop is not perfectly flat out to the knee, and therefore, $\frac{d\phi}{dt}$ is not zero in this region. Consequently, the partially excited cores will induce voltages in the sense winding during the read, and these voltages will add to that induced by the selected core. Also, as a result of the various disturb excitations, there exist not just a single ONE state and single ZERO state,



CORE MATERIAL : GENERAL CERAMICS TYPE BODY MF 1326-B,
F-394 DIE SIZE

MAXIMUM CURRENT: I_M = 840 ma.

FIG. 2.01a

A HYSTERESIS LOOP OF A TYPICAL MEMORY CORE MATERIAL

but several ONE states and several ZERO states.* If the voltage from the disturbed cores were a constant, the magnitude of a ONE output as seen across the sense winding (i.e., the voltage output from a selected core in a ONE state plus the disturb voltages) would always be larger than the ZERO output, and it would always be possible to discriminate between the two. However, the disturb outputs are not constant, but are a function of the information state of the core,and, therefore, one requirement must be that a fully selected ZERO output plus the maximum possible sum of disturb outputs never exceeds in magnitude a fully selected ONE output plus the minimum sum of disturb outputs.**

2.02 The ONE and ZERO States

To determine qualitatively the different possible information states of a core in a particular system, it is convenient to think of the magnetization process as consisting of both reversible and irreversible processes;[11,12] that is, either a very small fraction or a very large fraction of the potential energy is dissipated as heat, or in terms of the path traversed in the Ø-NI plane, the path closes for a reversible process whereas it does not close for an irreversible process (Figs. 2.02a and 2.02b).

For example, consider a core which is in the state represented by point A on the major hysteresis loop of Fig. 2.02a. If this core is excited with a current I_B, the path in the Ø-NI plane will be along the major loop to point B. Since the large change in flux was due mainly to an irreversible process, upon removal of the excitation, the core will not return to state A but will move along path ℓ to state C. However,

*See Section 2.02

**See Section 2.03

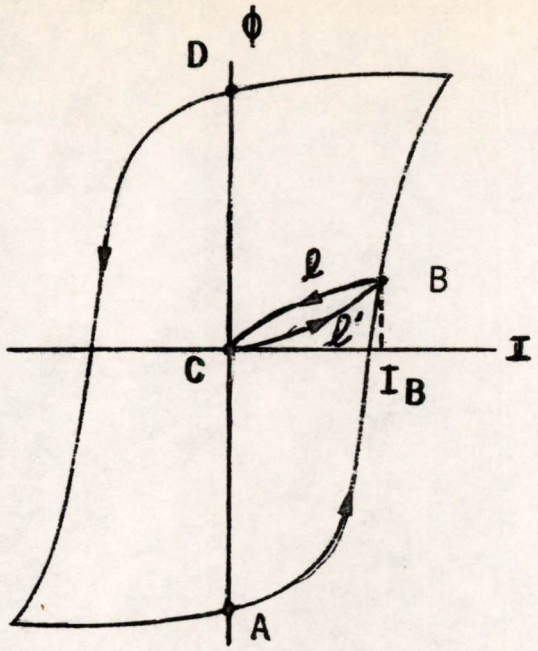


FIG. 2.02 a

CORE STATE AS A FUNCTION OF HISTORY

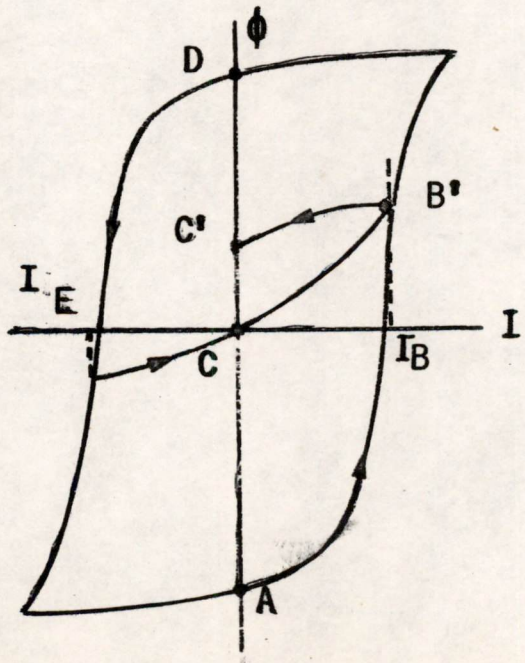


FIG. 2.02 b

CORE STATE AS A FUNCTION OF HISTORY

if the core is excited with I_B once more, it will move along ℓ' to approximately point B, and upon removal of the excitation it will follow approximately path ℓ back to state C. In this case the process was essentially reversible.

Figure 2.02b shows the path traversed in the Ø-NI plane when the core was placed in state C, starting originally in state D and exciting with I_E and then removing the excitation. If the core is now excited with I_B it will not assume state B, but a new state, B', and upon removal of the excitation, the final state will be C', the process being mainly irreversible. Although in both cases the core passed through state C, the final state was dependent upon previous history.

From the results of Chapter 1, the different possible disturbing modes for a particular system can be determined, and by reapplying the examples shown, the various information states can be determined.* It should be realized that the assumption is made that the loops close on the first traversal, while the actual process is an asymptotic one, and, therefore, the number of possible states is infinite. However, this assumption is a good first approximation, and the results are useful in the system analysis.

2.03 Sensing Schemes

Assuming temporarily that the polarity of all the cores on the sense winding is the same, the condition for reliable memory operation can be summarized symbolically as follows:

$$\left[\min V_1^{ONE} + \min \sum V_d\right] - \left[\max V_1^{ZERO} + \max \sum V_d\right] \geq \epsilon$$

or

$$\left[\min V_1^{ONE} - \max V_1^{ZERO}\right] - \left[\max \sum V_d - \min \sum V_d\right] \geq \epsilon \qquad (1)$$

*See Section 4.02

where

V_1^{ONE} = the voltage output from a fully selected core in a ONE state

V_1^{ZERO} = the voltage output from a fully selected core in a ZERO state

$\sum V_d$ = the sum of the outputs from the partially selected cores

and ϵ is the required working margin to allow for system variations. For simplicity the symbol V and not $V(t_1)$ was used; however, it should be remembered that the voltages are functions of time evaluated at a particular instant in time.

From the inequality above, it is easily seen that to maximize the left-hand side, it is desirable to maximize the difference in the first bracket and to minimize the difference in the second bracket. The first is accomplished mainly through the choice of core material and careful single core testing, whereas the second is accomplished both through the choice of core material and the use of various sensing techniques.

A. Direct Amplitude Discrimination

Of the various sensing schemes to be discussed, the simplest is amplitude discrimination in time. This scheme involves sensing at the same time in each cycle which gives the best over-all working margin for all addresses and patterns. Aside from its simplicity, this scheme gives a very fast information access time and a short memory cycle. With some ferrite cores, these times are of the order of 1 and 5 microseconds, respectively. However, since the effect of the

partially selected cores has not been appreciably minimized, the cores must be carefully selected and the memory size is seriously limited by the selection of cores. This assumes that there is a single sense winding per digit. Any number of sense windings could be used to reduce the effect of disturbed cores at the expense of additional sense amplifiers, and this is a factor to be considered in the choice of a sensing scheme for a particular system.

B. Post-Write Disturb

Several means have been used in trying to reduce the effect of the partially selected cores, one of the first methods being the "post-write disturb."[12,13] The assumption is that at the sensing time the outputs from partially excited cores will be more nearly equal if the cores are previously disturbed so as to make the outputs reversible. (When this method was first presented, it was not thought of in these terms, but this is what is actually being done.) In the general n-coordinate system a series of pre-read disturbs must be used to get the cores into these reversible states.*

C. Staggered Read

A more effective way of reducing the voltage outputs from partially selected cores at sensing time is to use staggering in the selection. The excitations can be chosen such that either the selecting or unselecting excitations in each coordinate are zero, and the selection done in the following manner. All but one of the coordinates are excited, the remaining coordinate being one in which the unselecting lines are zero, and after sufficient time has been allowed to let the voltages

*See Section 2.03D

induced in the sense winding decay to zero, the remaining coordinate is excited. If there are d_j driving lines in this remaining coordinate, when it is selected only $\frac{1}{d_j}$ of the total number of cores will induce voltages, one of these being the selected core, and thus the number of disturb outputs at sensing time has been greatly reduced.

When considering staggering, some thought should be given to the number of driving lines in each coordinate. Generally, the number of driving lines per coordinate is made equal to minimize the number of drivers required for a specified memory capacity. However, the staggering technique can be used to a greater advantage if the final coordinate excited is larger than the others since then a smaller fraction of the total number of memory cores will induce voltages at the sensing time.

By referring to the results of Chapter 1, it can be shown that the staggering technique does not destroy the information states of the unselected cores. When either the selecting or unselecting excitations in each coordinate are made zero, the values of the non-zero excitations will be $\pm \frac{2}{n+1}$ if n is odd and $\pm \frac{2}{n+2}$ if n is even. Also, the corresponding values of N_u and N_s are $N_s = \frac{n+1}{2}$ and $N_u = \frac{n-1}{2}$ for odd n, and $N_s = \frac{n+2}{2}$ and $N_u = \frac{n-2}{2}$ for even n. Therefore, when all but the last coordinate are excited, the minimum excitation any core receives is

$$\left(\frac{-2}{n+1}\right)\left(\frac{n-1}{2}\right) = -\frac{n-1}{n+1} \quad \text{for odd n} \tag{2}$$

and

$$\left(\frac{-2}{n+2}\right)\left(\frac{n-2}{2}\right) = -\frac{n-2}{n+2} \quad \text{for even n} \tag{3}$$

and the value of the maximum excitation any core receives is

$$\left(\frac{2}{n+1}\right)\left(\frac{n-1}{2}\right) = \frac{n-1}{n+1} \quad \text{for odd n} \tag{4}$$

and

$$\left(\frac{2}{n+2}\right)\left(\frac{n}{2}\right) = \frac{n}{n+2} \quad \text{for even } n \tag{5}$$

Recalling that the cores must be capable of withstanding excitations of $\pm\frac{n-1}{n+1}$ for odd n and $\pm\frac{n}{n+2}$ for even n, it is seen that the above procedure has not switched any of the cores in the array.

D. Amplitude Discrimination after Integration

Through the use of a pre-read disturb sequence it is possible to get all but the selected core into states that will give essentially reversible outputs when partially excited during the read, and since by definition there is no net flux change for a reversible output, the effect of the disturbed cores can be eliminated by integration. However, in actual operation the outputs are not completely reversible and these cores still have some effect although it has been reduced by a large factor.

The need for selective disturbing can be explained best by observing that if the partially excited cores receiving a positive read excitation are previously disturbed with the maximum partial excitation and those receiving a negative excitation are previously disturbed with the minimum partial excitation, they will be in states which give reversible outputs during the read. If none of the cores receive a negative excitation during the read, a disturb similar to the post-write disturb is sufficient. However, for most cases, the disturbing must be selective, being done by exciting the different coordinates in various sequences just before the read. (See Section 4.04.)

E. Sensing Schemes Using Difference Amplifiers

Several schemes which make use of a difference amplifier are outlined in Reference 13. One of these uses a double read pulse

after having disturbed the array so that there is only a single ONE state and a single ZERO state, all of the cores being in either one or the other. If the first read output is delayed and compared with the second read output in a difference amplifier, the outputs from the partially excited cores will be the same for each cycle and cancel.

A second proposal postulates a read current with the rise and fall times equal. If the outputs from the partially selected cores are the same in magnitude but the opposite in polarity at the beginning and end of the read pulse, by properly delaying and comparing in a difference amplifier, these outputs can be made to cancel. Actually cancellation here is only partial at best.

2.04 The Number of (1-kU) - Excited Cores

To quantitatively analyze the sensing problems involved with a particular memory system, it is always necessary to determine the number of cores receiving a specific excitation. A means of doing this is to use the same technique used in deriving the theory of selection where the excitation on all the core was diminished by one unit.* Then the problem becomes that of determining the number of cores having k unselecting lines through them where $k = 1,2,\cdots n$ and the value of the unselecting excitation is generally either $\frac{-2}{n+1}$ or $\frac{-2}{n+2}$ depending on whether n is either odd or even.

Consider the system with coordinates X_1, $X_2 \cdots X_n$ and let d_1, d_2, $\cdots d_n$ equal the number of drivers in the respective coordinates.

---

*See Section 1.03.

The total number of cores in the array will be $\prod_{j=1}^{n} d_j$, and any line in the mth coordinate will excite $\frac{1}{d_m}$ of the total number of cores. Therefore, when the mth coordinate is unselected $\frac{d_m-1}{d_m} \prod_{j=1}^{n} d_j$ cores will receive -U units of unselecting excitation. By using this fact a general formula can be deduced. Consider first unselecting only coordinate X_1; then

$\frac{d_1-1}{d_1} \prod_{j=1}^{n} d_j$ cores will receive 1 - U units

$\frac{1}{d_1} \prod_{j=1}^{n} d_j$ cores will receive 1 unit

If X_1 and X_2 are unselected, then

$\frac{d_1-1}{d_1} \prod_{j=1}^{n} d_j \frac{d_2-1}{d_2}$ cores will receive 1 - 2 U units

$\frac{1}{d_1} \prod_{j=1}^{n} d_j \frac{d_2-1}{d_2}$ cores will receive 1 - U units

$\frac{d_1-1}{d_1} \prod_{j=1}^{n} d_j \frac{1}{d_2}$ cores will receive 1 - U units

$\frac{1}{d_1} \prod_{j=1}^{n} d_j \frac{1}{d_2}$ cores will receive 1 unit

Summing the terms, the results become

$\frac{d_1-1}{d_1} \cdot \frac{d_2-1}{d_2} \prod_{j=1}^{n} d_j$ cores will receive 1 - 2 U units

$\frac{(d_1-1)-(d_2-1)}{d_1 d_2} \prod_{j=1}^{n} d_j$ cores will receive 1 - U units

$\frac{1}{d_1 d_2} \prod_{j=1}^{n} d_j$ cores will receive 1 unit

Carrying this procedure further the general form can be obtained for the case when all n coordinates are unselected. In doing so it is seen that each expression for the number of cores receiving 1-(k-1)U units of excitation can be obtained from that for 1-kU units, except for a constant factor, by adding the partial derivatives. Also $\prod_{j=1}^{n} d_j$ will be cancelled by the factors in the denominator when all n coordinates are selected.

Let C_k = the number of cores receiving 1-kU units of excitation.

Then $$C_n = \prod_{j=1}^{n} (d_j - 1) \tag{1}$$

$$C_k = \frac{1}{(n-k)!} \sum_{j=1}^{n} \frac{\partial C_{k+1}}{\partial d_j} \quad k = 1,2, \cdots (n-1) \tag{2}$$

$$C_o = 1 \tag{3}$$

Since the maximum number of cores can be selected with a given number of drivers when the number of drivers in each coordinate is the same, it is of interest to determine the form that these expressions take for this case.

Let $d_1 = d_2 = \cdots = d_n$

Then

$$C_n = (d-1)^n \tag{4}$$

$$C_{n-1} = \frac{1}{1!} n(d-1)^{n-1} \tag{5}$$

$$C_{n-2} = \frac{1}{2!} n(n-1)(d-1)^{n-2} \tag{6}$$

$$\vdots$$

$$C_k = \frac{1}{(n-k)!} n(n-1)\cdots(k+1)(d-1)^k \tag{7}$$

or

$$C_k = \frac{n(n-1)\cdots(n-k+1)}{k!}(d-1)^k, \; k = 1,2\cdots n \tag{8}$$

$$C_o = 1 \tag{9}$$

2.05 $ONE_{min} - ZERO_{max}$

The next step in this analysis is to determine the difference between ONE_{min} and $ZERO_{max}$ where

$$ONE_{min} = \min V_1^{ONE} + \min \sum V_d \quad (1)$$

and

$$ZERO_{max} = \max V_1^{ZERO} + \max \sum V_d \quad (2)$$

Since there are generally several ONE and several ZERO states possible and the disturb outputs from these states are different, it is difficult to derive a general expression for this difference. However, a general expression can be derived which can be used to obtain a lower limit, or modified to fit a particular case.

Assume that the sense winding goes through all the cores such that the voltage output induced by each core is positive when it is excited with a positive read current. The output voltage induced in the sense winding will be then the voltage from the selected core plus the sum of the voltages from all the partially excited cores. From the hysteresis loops, the indication is that the largest positive disturb voltages will come from cores in a particular ONE state and the minimum positive voltages will come from cores in a particular ZERO state.*

Let $V_{1\text{-}kU}^{ONE}$ = the voltage from a core in the ONE state giving the largest positive voltage output and receiving 1-kU units of excitation.

and

$V_{1\text{-}kU}^{ZERO}$ = the voltage from a core in the ZERO state giving the smallest positive voltage output and receiving 1-kU units of excitation.

*See Section 4.02

If it is assumed that these states also give the smallest and largest negative outputs respectively, then

$$ONE_{min} = V_1^{ONE} + \sum_{k=1}^{n} C_k V_{1-kU}^{ZERO} \quad (3)$$

and

$$ZERO_{max} = V_1^{ZERO} + \sum_{k=1}^{n} C_k V_{1-kU}^{ONE} \quad (4)$$

Let

$$\delta_{1-kU} = V_{1-kU}^{ONE} - V_{1-kU}^{ZERO} \quad (5)$$

Then

$$ONE_{min} - ZERO_{max} = V_1^{ONE} - V_1^{ZERO} - \sum_{k=1}^{n} C_k \delta_{1-kU} \quad (6)$$

This expression gives a lower limit which is usually not obtainable in actual operation. The actual worst difference is somewhat better than this since the mode of operation does not permit all of the cores to be in these worst states at the same time. A closer approach to this figure can be obtained by analysing the particular system to determine the different possible δ_{1-kU}'s and the worst possible combination of these obtainable; however, this becomes very involved because of the effect of previous history on the state of the cores.

2.06 Sense Winding Geometry

The effect of sense winding geometry on the difference between ONE_{min} and $ZERO_{max}$ is the next point to consider, and for all but a very small array, this difference can be shown to be independent of the winding geometry if air flux pickup is neglected.

Consider just two cores of an array, the selected core and a core receiving 1-kU units of excitation. Pass a sense winding through the two cores such that the voltage outputs add. Then,

$$ONE_{min} = V_1^{ONE} + V_{1-kU}^{ZERO} \quad (1)$$

$$ZERO_{max} = V_1^{ZERO} + V_{1-kU}^{ONE} \quad (2)$$

and

$$ONE_{min} - ZERO_{max} = V_1^{ONE} - V_1^{ZERO} - \delta_{1-kU} \quad (3)$$

Now pass the sense winding through the two cores such that the voltage output of the disturbed core is of opposite polarity.

Then,

$$ONE_{min} = V_1^{ONE} - V_{1-kU}^{ONE} \quad (4)$$

$$ZERO_{max} = V_1^{ZERO} - V_{1-kU}^{ZERO}$$

and

$$ONE_{min} - ZERO_{max} = V_1^{ONE} - V_1^{ZERO} - \delta_{1-kU} \quad (5)$$

Therefore, changing the polarity of the disturbed core did not affect the magnitude of ONE_{min} minus $ZERO_{max}$ for the selected core, and since the disturbed core was any one in the array, this will be true for the case when the winding goes through all the cores of the digit plane. Since, except for very small arrays, the magnitude of ONE_{min} and $ZERO_{max}$ will be the same for every address, ONE_{min} minus $ZERO_{max}$ is independent of the sense winding geometry.

Although ONE_{min} minus $ZERO_{max}$ is independent of geometry, it should be realized that the individual quantities are affected and, consequently, the ratio of ONE_{min} to $ZERO_{max}$ is a function of geometry. Air flux pickup varies with geometry too, and these factors must be considered in designing a system.

PART II

A 4-COORDINATE READ — 5-COORDINATE WRITE CORE MEMORY SYSTEM

CHAPTER 3

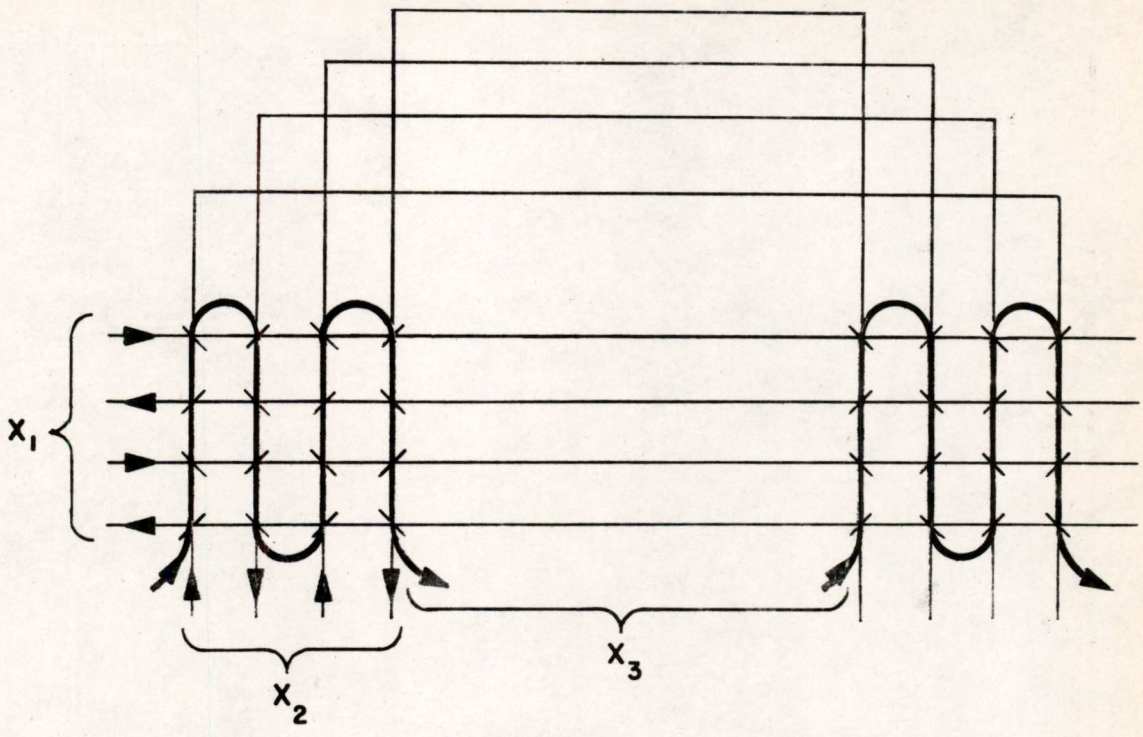
INTRODUCTION

3.01 History of the M.I.T. Core Memory

The most successful work in magnetic-core memories has evolved from a proposal made in 1949 by Jay W. Forrester.[14] It suggested the use of magnetic cores as memory elements and illustrated a 2-coordinate read, 3-coordinate write scheme of the general type discussed in Part I. (See Fig. 3.01a.) In 1950, W. N. Papian investigated this proposal, and found that metallic-ribbon cores with hysteresis loops of sufficient rectangularity for memory application were available.[15] From the results of this investigation, a one digit memory of 4 bits was built, and eventually this was expanded to 256 bits.[16] However, during this period, powdered ferrite cores were being developed which were faster switching and cheaper to manufacture than the metallic-ribbon cores, and, therefore, further experimentation was concentrated mainly on the use and development of ferrite cores. By 1953 the two banks of electrostatic storage of Whirlwind I (2048 17-digit registers) had been replaced by ferrite core storage, and by the spring of 1954 a memory of twice this capacity was operating reliably. At present, serious consideration is being given to the possibility of constructing memories of even larger capacity, and one of the problems to be dealt with is the increased number of vacuum tubes which would be required for the larger system.

3.02 Memory Systems with More than 3 Coordinates

By using magnetic-core switches and by increasing the number of memory coordinates, the number of vacuum tube drivers necessary



READ:

	X_1	X_2	X_3
S_j	$\frac{1}{2}$	$\frac{1}{2}$	0
u_j	0	0	0

WRITE:

	X_1	X_2	X_3
S_j	$-\frac{1}{2}$	$-\frac{1}{2}$	0
u_j	0	0	$\frac{1}{2}$

FIG. 3.01 a

A 2-COORDINATE READ-3-COORDINATE WRITE CORE MEMORY

A-59699

for a given memory capacity can be reduced by a large factor. A great deal of work has been done on the analysis and design of the core switch,[6,7,8,9] but no work has been done previously to investigate the possibility of memory systems with $n > 3$. It is only due to the improvement of core materials that such an investigation is now worthwhile.

As n increases the number of drivers is reduced and better core materials are required. This is true because:

1. For a given memory capacity the number of coordinate lines decrease as n increases and a larger fraction of the memory is excited by each coordinate line.

2. Since $p_{min} = \frac{n-1}{n+1}$, the cores must have more rectangular hysteresis loops as n increases.

3. With a given core material, $ONE_{min} - ZERO_{max}$ will decrease because of the fact that more cores are partially excited and the value of the maximum partial excitation increases with increasing n.

The third point mentioned is the most important disadvantage of increasing n since it affects the working margins of the system.

In many computer applications, a memory system is designed primarily with reliability in mind. If the term is defined as the ratio of the number of memory cycles to the number of errors, it is essentially the reciprocal of the probability of the operating point drifting from its optimum setting into a region of error.[17] This probability is dependent upon many things including the probability of tube failure and the size of the working margins. Therefore, any evaluation of a system design in terms of reliability must not only consider the tube count, but also the effect this design has on margins.

3.03 The Proposed Investigation

The remainder of this thesis will be concentrated on determining whether a large capacity memory using a 4-coordinate read — 5-coordinate write is practical from the standpoints of reliability, speed and cost. In Chapter 4 the general theory of Part I will be applied to this specific case, in Chapter 5 the data obtained from single cores will be analyzed, and in Chapter 6 the experimental analysis of a 8 x 8 x 8 x 8 memory plane will be given along with the final conclusions.

CHAPTER 4

SELECTION AND SENSING

4.01 The Selection System

The following specifications will be placed on the system to be analyzed.

1. The read will use a 4-coordinate selection system and the write will use a 5-coordinate selection system.

2. Either the selecting line or unselecting lines in each coordinate will use a zero excitation, and the excitations will be chosen to obtain the best possible selection ratio.

With these specifications in mind, the results of Part I can be evaluated to determine the necessary excitations. For the read,

$$u_j - s_j = \frac{-2}{n+2} = -\frac{1}{3} \tag{1}$$

with

$$N_s = \frac{n+2}{2} = 3 \tag{2}$$

and

$$N_u = \frac{n-2}{2} = 1 \tag{3}$$

and for the write,

$$u_j - s_j = \frac{2}{n+1} = \frac{1}{3} \tag{4}$$

with

$$N_s = \frac{n+1}{2} = 3 \tag{5}$$

and

$$N_u = \frac{n-1}{2} = 2 \qquad (6)$$

These results are tabulated below, and Fig. 4.01a shows the read wiring schematic for a 4x4x4x4 digit plane. The wiring for the write is the same except for an additional winding in each digit plane, this winding passing through all the cores of the plane.

TABLE 4.01a

READ EXCITATIONS

	X_1	X_2	X_3	X_4
s_j	1/3	1/3	1/3	0
u_j	0	0	0	-1/3

TABLE 4.01b

WRITE EXCITATIONS

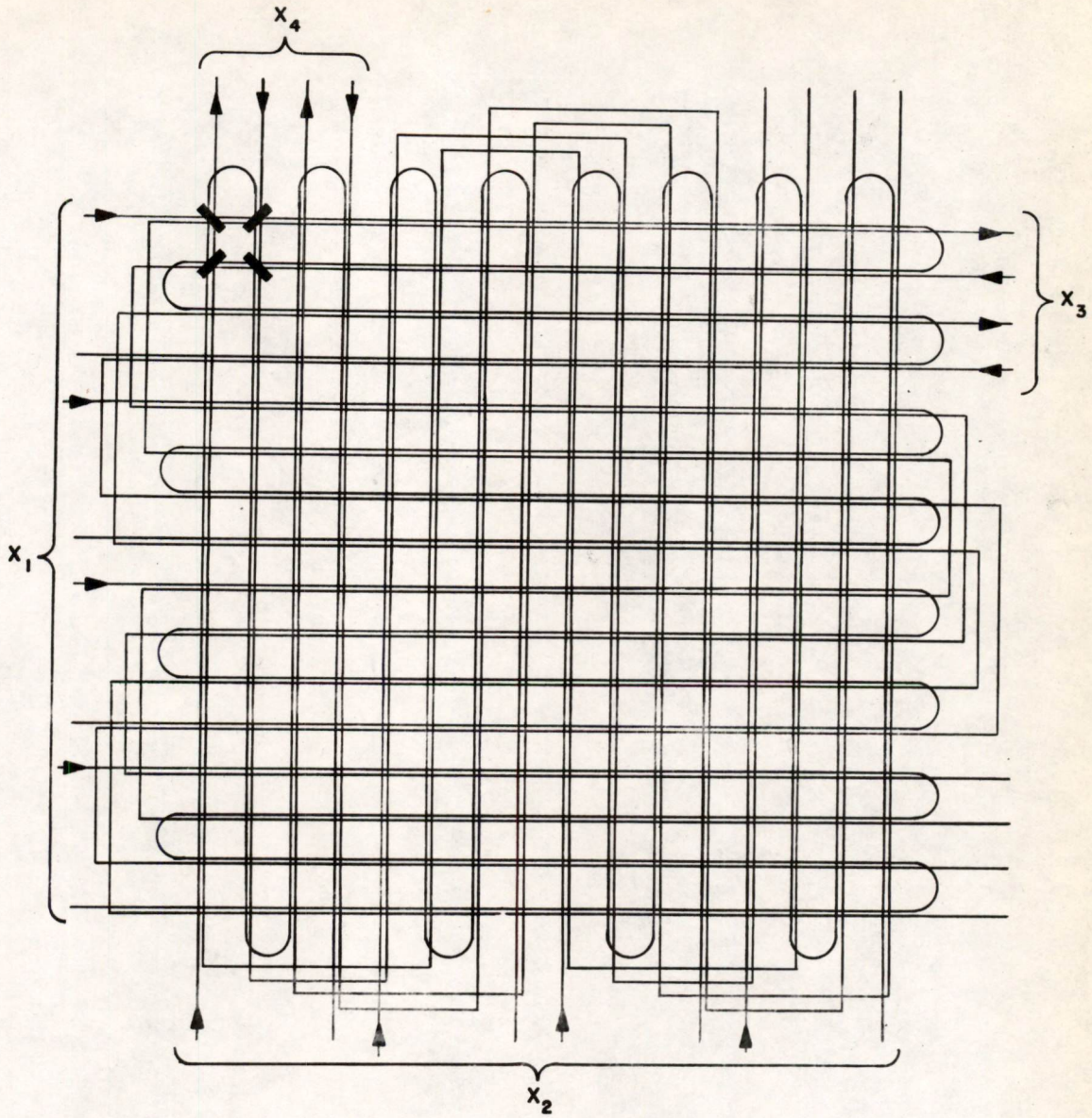
	X_1	X_2	X_3	X_4	X_5
s_j	-1/3	-1/3	-1/3	0	0
u_j	0	0	0	1/3	1/3

The selection ratios obtained with these excitations are:

$$R = \frac{n+2}{n} = \frac{3}{2} \qquad (7)$$

for the read selection, and

$$R = \frac{n+1}{n-1} = \frac{3}{2} \qquad (8)$$



	X_1	X_2	X_3	X_4
S_j	$\frac{1}{3}$	$\frac{1}{3}$	$\frac{1}{3}$	0
u_j	0	0	0	$-\frac{1}{3}$

NOTE: ONLY FOUR CORES ARE SHOWN

FIG. 4.01 a

A 4-COORDINATE READ SYSTEM

for the write selection.

4.02 The ONE and ZERO States

Assuming that the hysteresis loops close upon the first traversal, there will be a finite number of ONE and ZERO states, and these may be determined from the different possible read-write sequences tabulated below.*

TABLE 4.02a

POSSIBLE READ-WRITE SEQUENCES OF PULSES RECEIVED BY CORES IN THE PLANE

	If the information written in the selected core is ONE		If the information written in the selected core is ZERO	
	Read	Write	Read	Write
If core in question is selected	1	-1	1	-2/3
If core in question is unselected	2/3	-2/3	2/3	-1/3
	1/3	-1/3	1/3	0
	0	0	0	1/3
	-1/3	1/3	-1/3	2/3

*See Section 2.02.

These states and the associated hysteresis loops are depicted in the sketch of Fig. 4.02a, and combinations of read-write sequences that will place a core in each of these states are given in Table 4.02b.

To determine the accuracy of the qualitative picture given in Fig. 4.02a, D.C. hysteresis loops were obtained for a typical memory core material (Fig. 4.02b). From these loops it can be seen that for the smaller excitations the assumption that the loops close on the first traversal is quite good whereas for the larger excitations this assumption is less accurate. However, since the results of this section can be used in obtaining only a rough indication of the working margin, any more accurate assumptions would only add to the complexity of the problem without increasing the accuracy of the results.

4.03 The Memory Plane Output

As was stated in Section 2.05, because of the many information states that exist, it becomes nearly impossible to predict the memory plane output since it will be a function of both the pattern stored and the sequence of register selections. A very pessimistic estimate of the worst difference that will exist between a ONE and ZERO output can be obtained for this system by evaluating equation 2.05(6) for n=4*

$$ONE_{min} - ZERO_{max} = V_1^{ONE} - V_1^{ZERO} - \sum_{k=1}^{4} C_k(n)\,\delta_{1-k/3} \qquad (1)$$

and if $d_1 = d_2 = \cdots = d_n$

$$ONE_{min} - ZERO_{max} = V_1^{ONE} - V_1^{ZERO} - 4(d-1)\delta_{2/3} - 6(d-1)^2\delta_{1/3} - 4(d-1)^3\delta_0 - (d-1)^4\delta_{-1/3}$$

*One sense winding per digit plane is assumed.

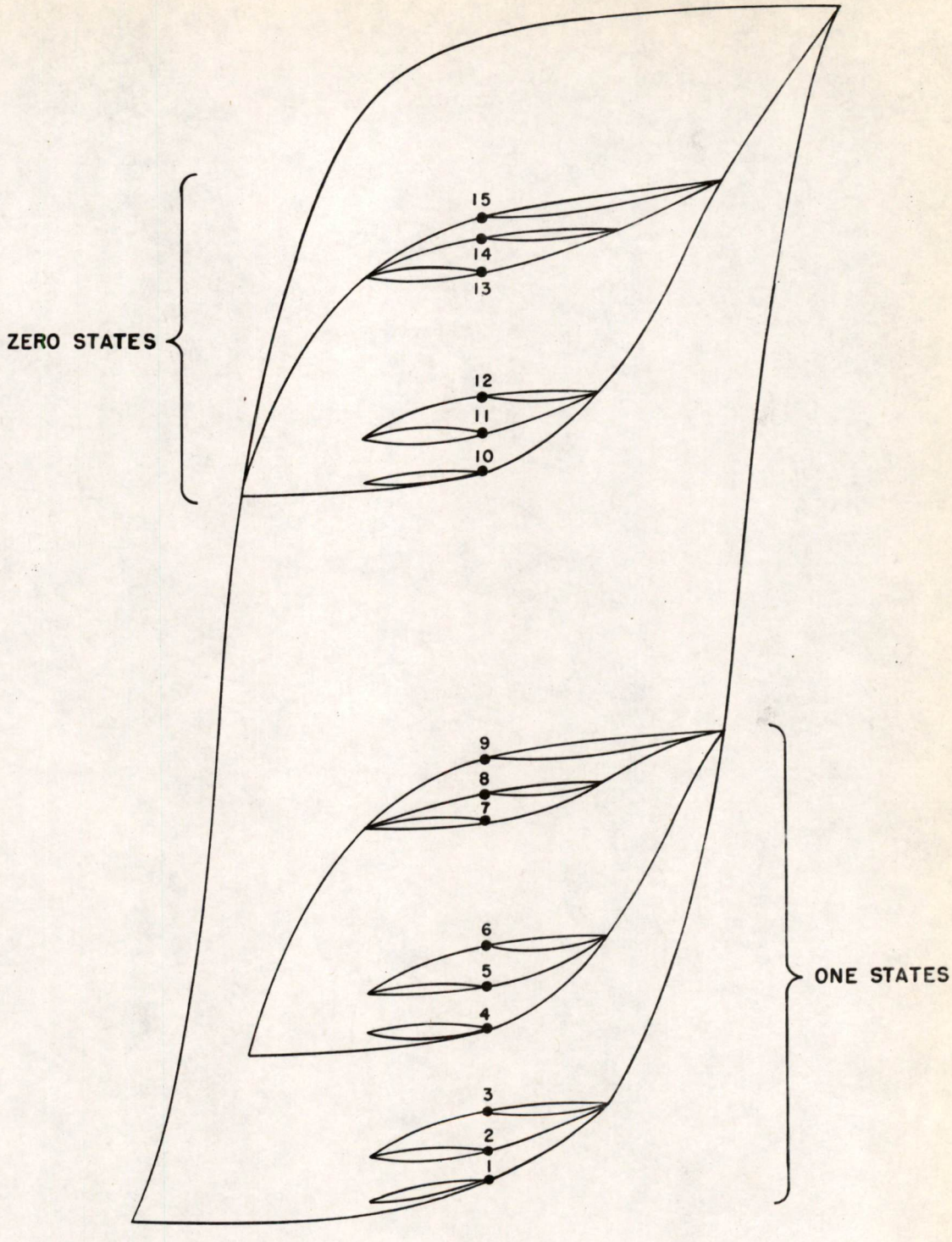


FIG. 4.02 a

THE ONE AND ZERO STATES

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TABLE 4.02b

SEQUENCES FOR OBTAINING A GIVEN STATE

State*	Cycle 1		Cycle 2		Cycle 3	
	Read	Write	Read	Write	Read	Write
1	1	-1				
2	1	-1	1/3	-1/3		
3	1	-1	1/3	0		
4	1	-1	2/3	-2/3		
5	1	-1	2/3	-2/3	1/3	-1/3
6	1	-1	2/3	-2/3	1/3	0
7	1	-1	2/3	-1/3		
8	1	-1	2/3	-1/3	1/3	0
9	1	-1	-1/3	2/3		
10	1	-2/3				
11	1	-2/3	1/3	-1/3		
12	1	-2/3	1/3	0		
13	1	-2/3	2/3	-1/3		
14	1	-2/3	2/3	-1/3	1/3	0
15	1	-2/3	-1/3	2/3		

*The numbers refer to Fig. 4.02a.

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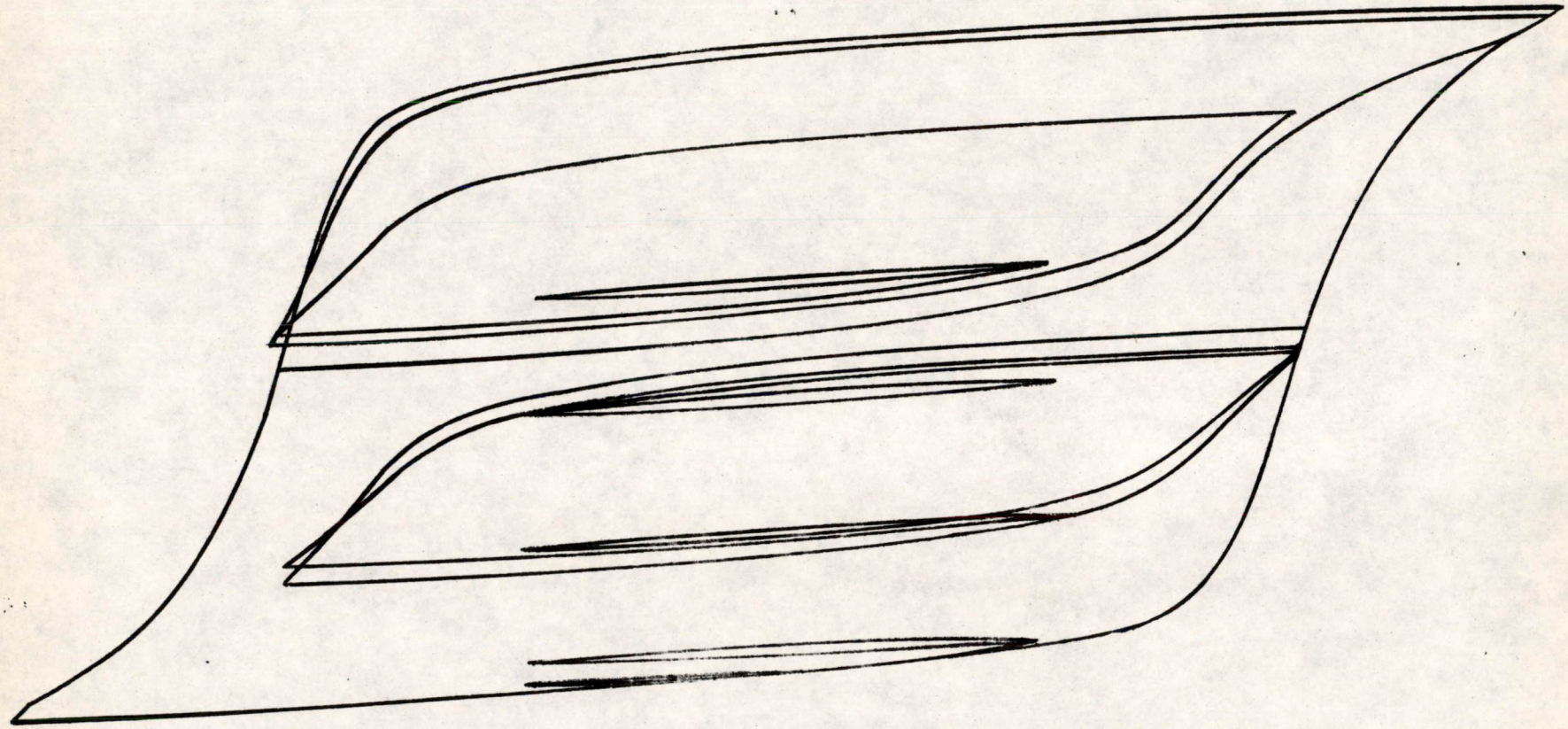

SAMPLE: MF 1326B
MOLD: F262

SCALE: ϕ - 25 MAXWELLS / INCH
NI-.625 AMP TURNS / INCH

FIG. 4.02 b

D.C. HYSTERESIS LOOPS FOR A TYPICAL MEMORY CORE MATERIAL

$$= V_1^{ONE} - V_1^{ZERO} - 4(d-1)\delta_{2/3} - 6(d-1)^2\delta_{1/3}$$

$$-(d-1)^4\delta_{-1/3} \qquad (2)$$

where the δ's are the worst possible. However, in actual operation it is impossible to get all the cores into the worst states simultaneously, and therefore, the results given by 4.03-(2) can be overly pessimistic by an order of magnitude.

If staggering is used in the selection, this margin (between ONE_{min} and $ZERO_{max}$) can be improved greatly since then only 1/d of the total array will give outputs at the sensing time. Also, a pre-read disturb sequence and integration can be used, and for this case equation 4.02-(2) still applies, being evaluated for the new values of δ_{1-kU}.

4.04 Selective Disturbing

It was pointed out in Section 2.03 that for some sensing schemes, it is necessary to have cores in states that will give reversible outputs when selected, and that this could be done by a selective pre-read disturb sequence. For the case under consideration this sequence can be determined by observing the following points.

1. Since during the read part of the array will receive positive disturbs and part will receive negative disturbs, the disturb sequence cannot consist of a single excitation on a winding common to all the cores of the digit plane, as was true of the post-write disturb of the system when n=2, for states which give reversible outputs for positive excitations will give irreversible outputs for negative excitations and vice versa. The pre-read disturb must be such that all cores receive an excitation equal in sign and at least equal in magnitude to the excitation received during the read (See Fig. 4.02a).

2. The only negative read disturb is a -1/3 disturb, and since driving lines in only one coordinate are negatively excited, and this excitation is -1/3, the previous selection of this coordinate alone will put the cores negatively excited during the read in states which will give reversible outputs. These cores will be unaffected by any pre-read selection of the remaining coordinates.

3. If the remaining coordinates are selected two at a time using the three possible combinations, all the cores receiving a 2/3 excitation during the read will be pre-disturbed by this amount, and all those receiving a 1/3 excitation will be pre-disturbed by at least 1/3 and at most 2/3.

Therefore, the disturb cycle consists of pulsing coordinate X_4 (Fig. 4.01a) and then pulsing the remaining coordinates two at a time, i.e., X_1 and X_2, followed by X_2 and X_3, followed by X_3 and X_1.

CHAPTER V

SINGLE CORE DATA

5.01 The Core Material

In order to make a preliminary selection from the large number of core materials available, use was made of the wealth of data taken at M.I.T. for 2 to 1 selection operation. The available data consisted of two types; that obtained from 60 cycle hysteresis loops* and that obtained from pulse tests. A quantitative index of hysteresis-loop squareness, the "squareness ratio" (see Figure 5.01a), had been defined and for each material data had been taken for the loop with the highest squareness ratio. This ratio then had been used as one means of comparing cores for memory application, the assumption being that the 60 cycle loop gives some indication of pulse operation, and that to a certain degree, the higher the squareness ratio the better the core. The cores with the higher squareness ratios and lower driving currents then had been pulse tested to determine the voltage outputs from the possible states and on the basis of these outputs, a final choice was made.

In selecting a material for the system under analysis, the same techniques could have been used. A new squareness ratio could have been defined (Figure 5.01b) and materials chosen on this basis with a final decision having been made from pulse tests. However, to economize on the time allowed for this study, the initial selection was done from

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* For this application the 60 cycle loop can be considered equivalent to the D.C. loop.

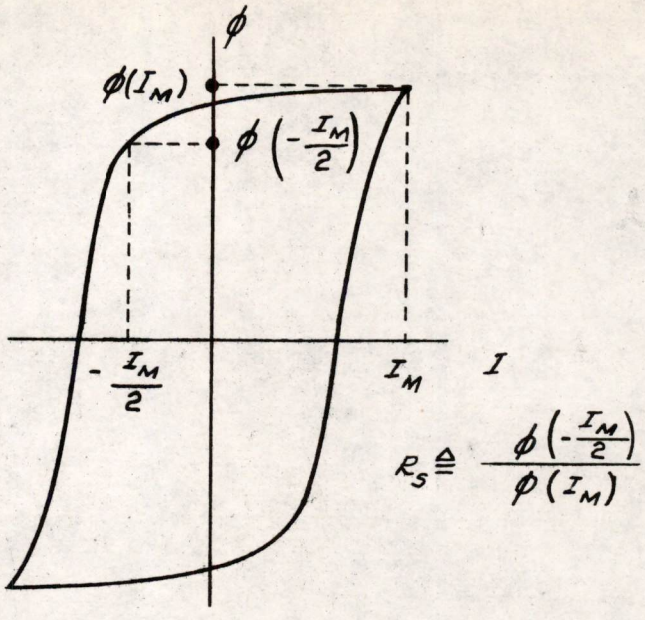


FIG. 5.01 a

SQUARENESS RATIO DEFINED FOR 2 TO 1 SELECTION

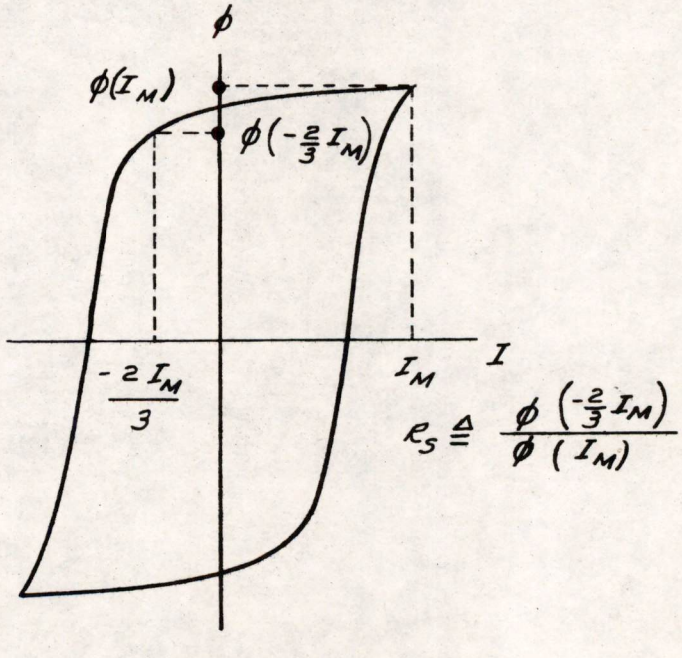


FIG. 5.01 b

SQUARENESS RATIO DEFINED FOR 3 TO 2 SELECTION

a study of the hysteresis loop data that had been obtained for the 2 to 1 selection system. The assumption made was that the squareness on the 2 to 1 basis gives an indication of the relative squareness on the 3 to 2 basis. Using this assumption and adding the restriction that the maximum driving force required be less than 1 ampere, several core materials were chosen for an initial pulse test and from these the core material chosen for extensive analysis was General Ceramics type body MF 1326-B, F-394 die size. There were several core materials that might have been used and the final choice was based mainly on the facts that it was a faster switching material and that a sufficient number of cores were readily available for building an 8 x 8 x 8 x 8 digit plane.

5.02 The Pulse Tester

The pulse tester was made up using Burroughs test equipment and Model V core drivers[20], and core outputs were observed with a Tektronix 514D, series A oscilloscope, a Tektronix 121 preamplifier being used when necessary. The tester was capable of placing cores in any one of the possible states of Figure 4.02a and then exciting them with any one of the six possible excitations. Binary counters were also included in the logic so that any read-write cycle could be repeated up to 4096 times. Figure 5.02a shows a block diagram of this set up.

5.03 Pulse Test Data for MF 1326B

Fifty MF 1326B cores were chosen at random from Lot G92 and used in obtaining the pulse characteristics for a 3 to 2 selection ratio. (The cores had been previously sorted for 2 to 1 operation and at the optimum selecting current of 820 m.a., the fully selected outputs ranged from

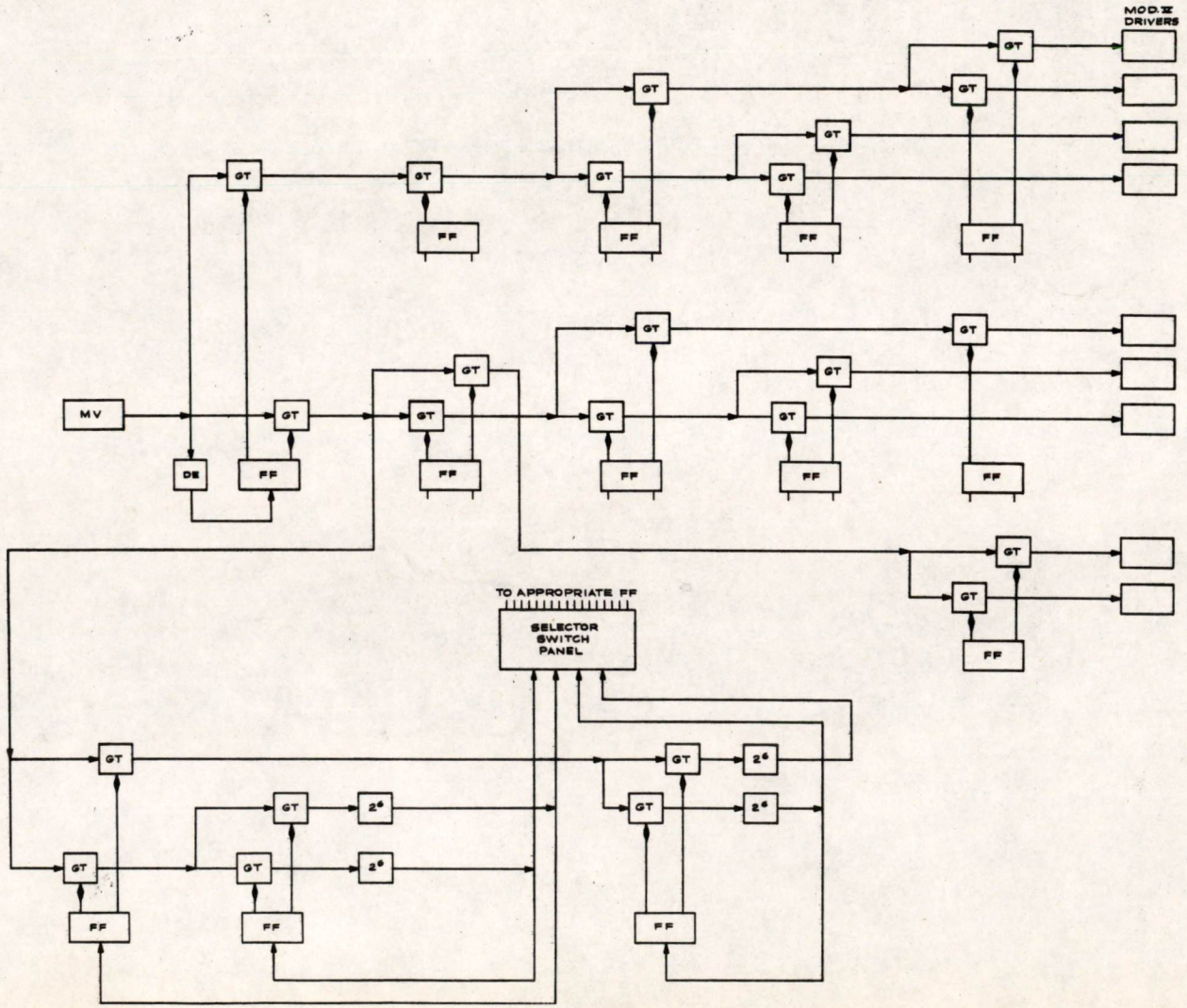


FIG 5.02a
BLOCK DIAGRAM OF CORE TESTER

105 to 120 mv.) These cores were driven simultaneously and the sum of the individual outputs was observed on a winding common to all the cores. Preliminary experimentation showed that for a 3 to 2 selection system the optimum current lay somewhere between 550 and 650 ma. and that even in this range, the various disturb voltage outputs were such that it would be impossible to operate an 8 x 8 x 8 x 8 digit plane with a single sense winding, using only amplitude discrimination. Pictures of these voltage outputs were taken for selecting currents of 600, 650 and 700 ma. with rise times of approximately .5 μsec and those for $I_m = 650$ are shown in Figures 5.03a through 5.03d. Taking measurements from the pictures an average value for each output was calculated on a single core basis for the time when the fully selected ONE output was maximum and these values are tabulated in Table 5.03a.

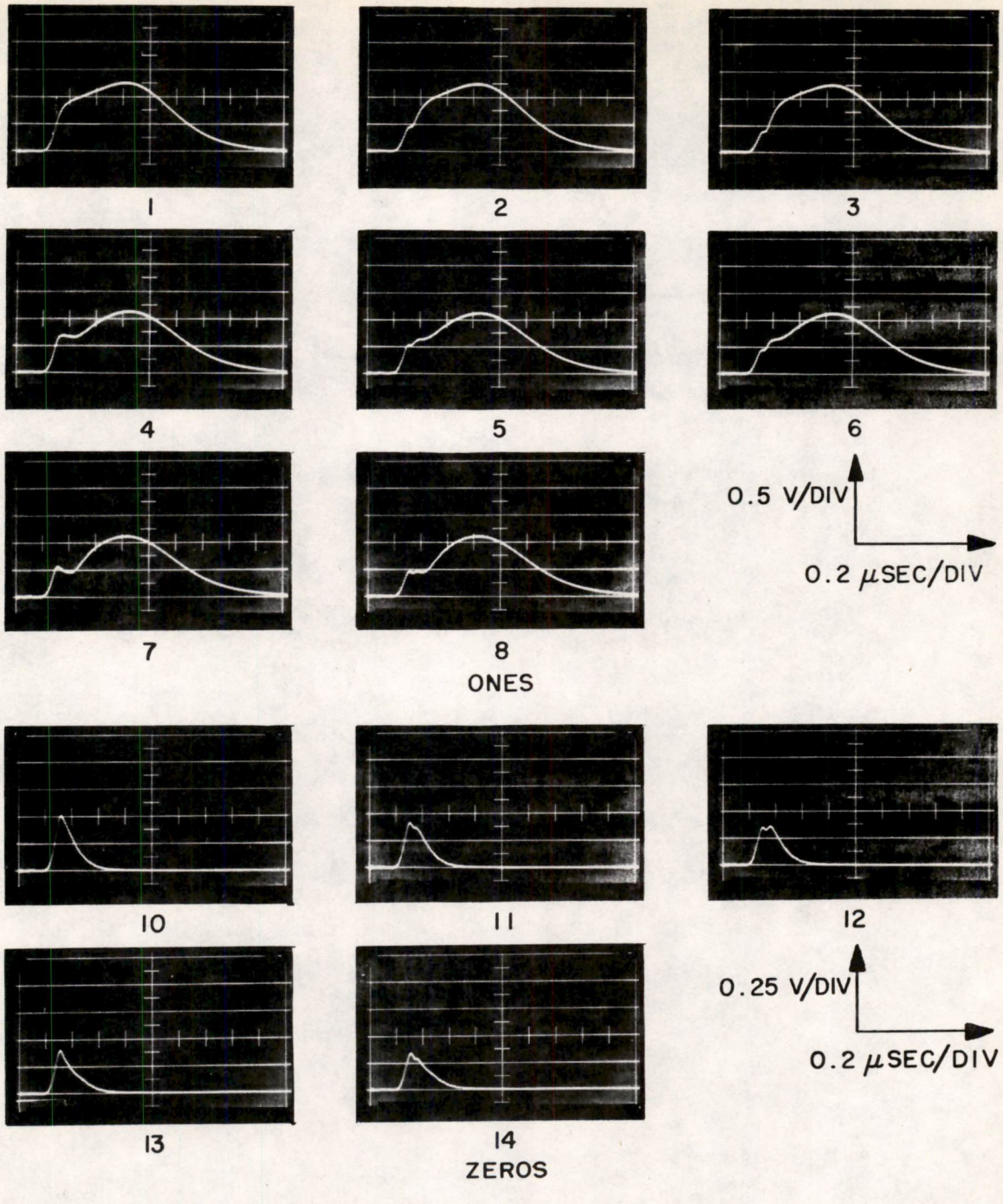
Equation 4.03-(2) can be evaluated using this data and for $I_m = 650$ ma. and $d_1 = d_2 = d_3 = d_4 = 8$.

$$|ONE|_{min} - |ZERO|_{max} = V_1^{ONE} - V_1^{ZERO} - 4(d-1)\,\delta_{\frac{2}{3}} - 6(d-1)^2\,\delta_{\frac{1}{3}} - (d-1)^4\,\delta_{-\frac{1}{3}}$$

$$= .044 - .001 - 28(.0053) - 294(.0008) - 2401(.0007)$$

$$= .044 - .001 - 2.16 < 0$$

Clearly, the magnitude of the disturb voltages is such that it would be impossible for the system to operate. The fact that the difference is negative indicates that the magnitude of the ZERO can exceed the magnitude of the ONE. Even if the results are in error by a factor of ten, this would still be true. The situation could be improved some if the sensing were done a little later in time since although the fully selected ONE



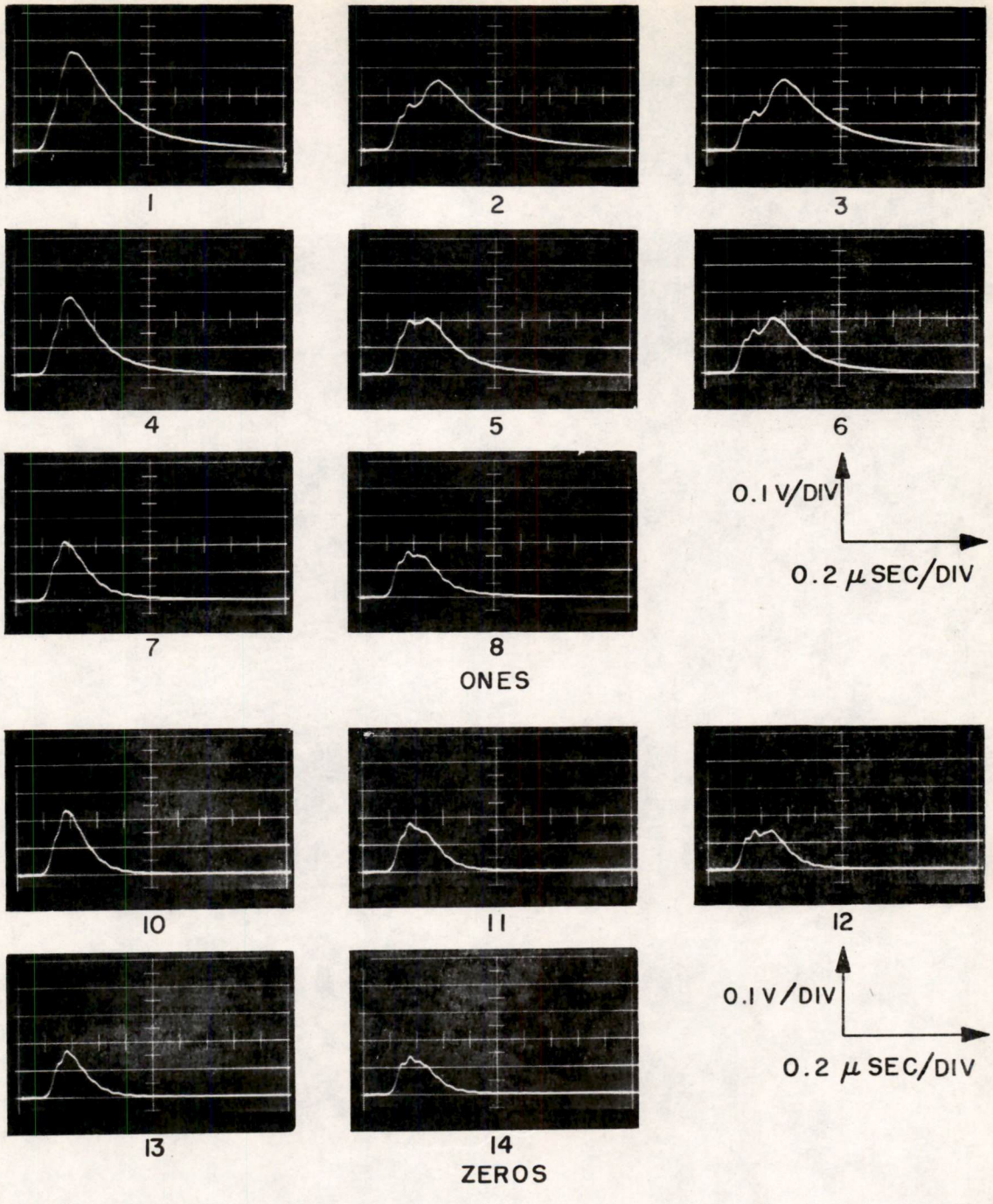
NOTES:

1. NUMBERS UNDER PICTURES REFER TO STATES OF FIG. 4.02 a
2. THESE OUTPUTS ARE FOR 50 CORES MF 1326-B, DIE SIZE 394, LOT G92

FIG. 5.03 a

V_1's AT I_M = 650 ma

A-59692



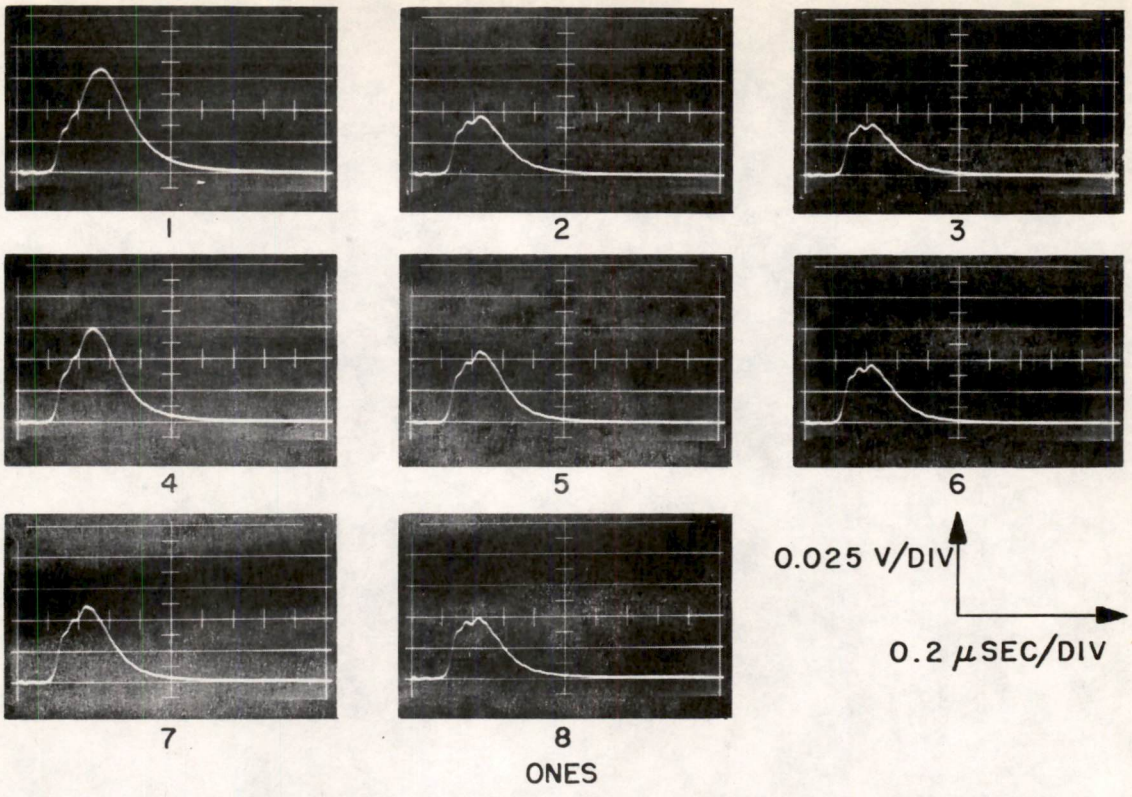
NOTES:

1. NUMBERS UNDER PICTURES REFERS TO STATES OF FIG. 4.02 a
2. THESE OUTPUTS ARE FOR 50 CORES MF 1326-B, DIE SIZE 394, LOT G92

FIG. 5.03 b

$V_{\frac{2}{3}}$'s AT I_M = 650 ma

A-59693

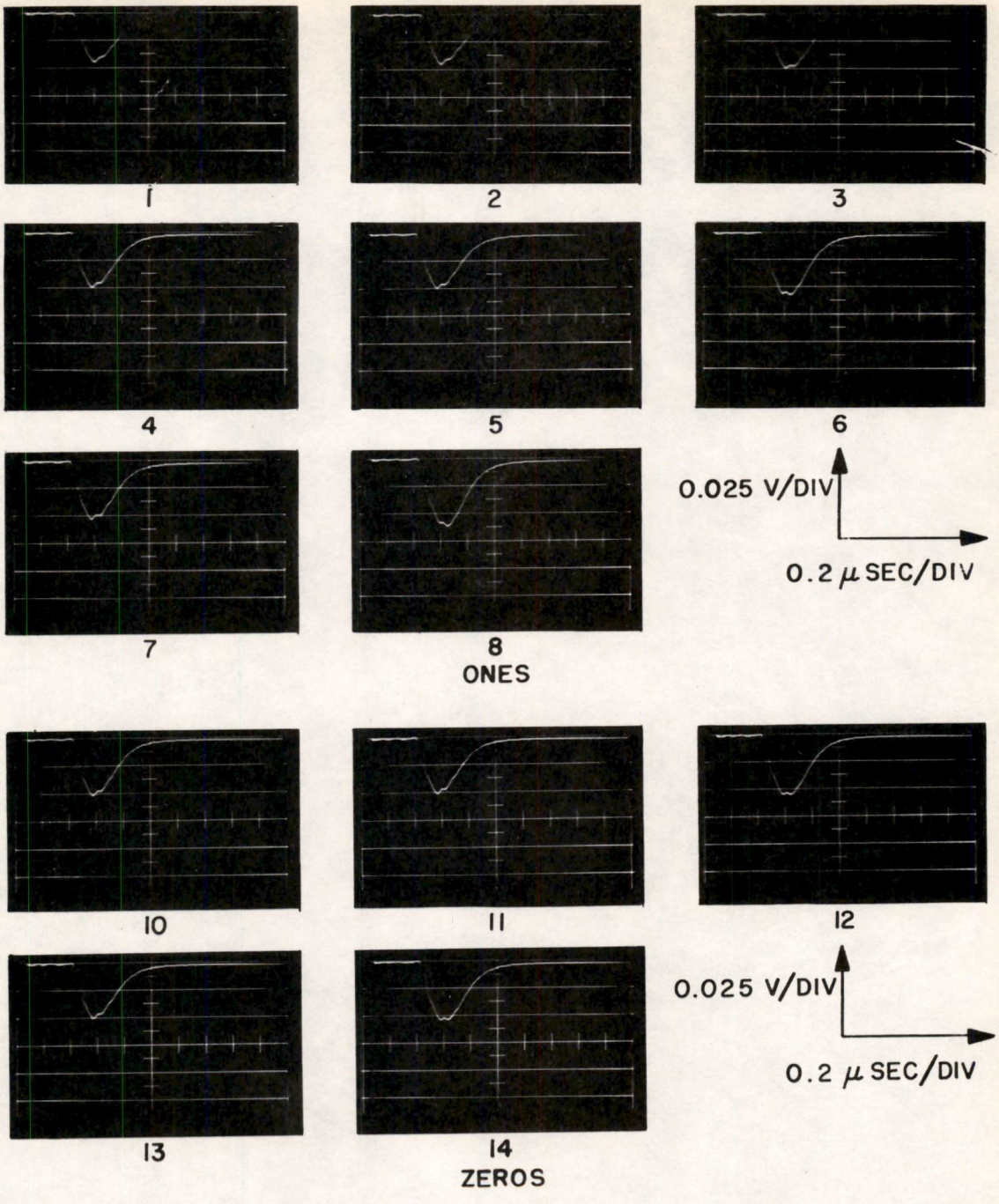


NOTES:

1. NUMBERS UNDER PICTURES REFER TO STATES OF FIG. 4.02a
2. THESE OUTPUTS ARE FOR 50 CORES MF 1326-B, DIE SIZE 394, LOT G92

FIG. 5.03c

$V_{\frac{1}{3}}$'s AT I_M = 650 ma



NOTES:

1. NUMBERS UNDER PICTURES REFER TO STATES OF FIG. 4.02a
2. THESE OUTPUTS ARE FOR 50 CORES MF 1326-B, DIE SIZE 394, LOT G92

FIG. 5.03d

$V_{-\frac{1}{3}}$'s AT I_M = 650 ma

TABLE 5.03a

VOLTAGE OUTPUTS AT A GIVEN SENSING TIME

STATE	EXCITATION I_m	VOLTAGE OUTPUT (Volts)		
		I_m=600 ma.	I_m=650 ma.	I_m=700 ma.
1	1	.036	.050	.070
2	1	.035	.049	.069
3	1	.035	.050	.068
4	1	.032	.045	.061
5	1	.032	.045	.060
6.	1	.032	.045	.060
7	1	.032	.045	.057
8	1	.032	.044	.057
9	1			
10	1	.001	.001	.001
11	1	.001	.001	.001
12	1	.001	.001	.001
13	1	.001	.001	.001
14	1	.001	.001	.001
15	1			
1	2/3	.0052	.0050	.0060
2	2/3	.0054	.0054	.0060
3	2/3	.0056	.0056	.0068
4	2/3	.0026	.0024	.0048
5	2/3	.0024	.0024	.0048
6	2/3	.0024	.0024	.0048
7	2/3	.0012	.0008	.0014
8	2/3	.0010	.0008	.0014
9	2/3			
10	2/3	.0008	.0003	.0006
11	2/3	.0006	.0004	.0004
12	2/3	.0007	.0004	.0003
13	2/3	.0006	.0004	.0002
14	2/3	.0004	.0004	.0002
15	2/3			

TABLE 5.03a (Continued)

STATE	EXCITATION I_m	VOLTAGE OUTPUT (Volts) I_m=600 ma.	I_m=650 ma.	I_m=700 ma.
1	1/3	.0015	.0010	.0009
2	1/3	.0003	.0003	.0002
3	1/3	.0003	.0002	.0002
4	1/3	.0009	.0005	.0005
5	1/3	.0005	.0003	.0003
6	1/3	.0004	.0002	.0002
7	1/3	.0005	.0003	.0004
8	1/3	.0003	.0003	.0003
9	1/3			
10	1/3	.0005	.0003	.0005
11	1/3	.0003	.0002	.0002
12	1/3	.0003	.0002	.0002
13	1/3	.0003	.0003	.0002
14	1/3	.0003	.0002	.0002
15	1/3			
1	-1/3	-.0005	-.0005	-.0003
2	-1/3	-.0005	-.0005	-.0003
3	-1/3	-.0008	-.0006	-.0005
4	-1/3	-.0007	-.0005	-.0009
5	-1/3	-.0007	-.0005	-.0005
6	-1/3	-.0009	-.0007	-.0006
7	-1/3	-.0005	-.0005	-.0004
8	-1/3	-.0008	-.0009	-.0006
9	-1/3			
10	-1/3	-.0005	-.0004	-.0003
11	-1/3	-.0005	-.0004	-.0003
12	-1/3	-.0006	-.0006	-.0004
13	-1/3	-.0003	-.0002	-.0003
14	-1/3	-.0005	-.0004	-.0004
15	-1/3			

NOTE: 1. The sensing time for I_m=600 ma. was .80 μsec. after the time marker shown in each of the photographs, and for I_m=650 ma. and I_m=700 ma., it was .85 μsec.

2. At the time the data was taken, the mistaken impression was held that states 9 and 15 were impossible in system operation and consequently no data was taken for these states; other results indicate that they do not differ greatly from states 8 and 14 respectively.

will be smaller in amplitude, the difference between the disturb voltages, which are much more numerous, would also be less. However, data from the 8 x 8 x 8 x 8 digit plane shows that there is not sufficient improvement, and therefore, other schemes, such as staggering in selection or disturbing and integrating, must be considered.*

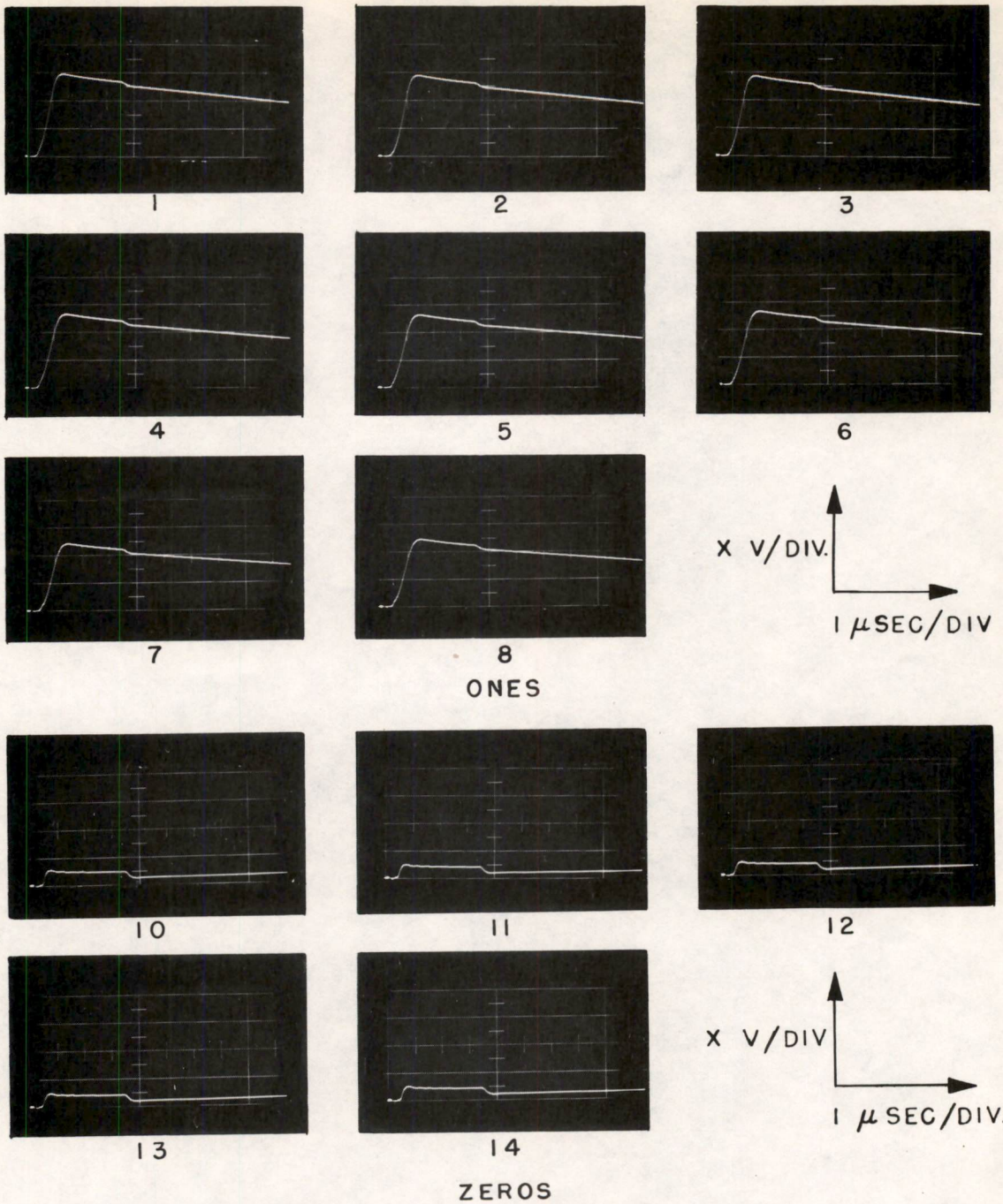
Since the data indicates that if the system is to operate at all, a more sophisticated technique of sensing must be used, possibly involving integration, a set of pictures were taken showing the integrated outputs for $I_m = 650$. A simple RC integrator with R = 100k and C = 220 μμf was used, and the integration was done from the start to the end of the read, the theory being that the integral of the reversible outputs is zero. These pictures are shown in Figures 5.03e through 5.03h and a comparison of this data and that already presented is given in Table 5.03b. The important point to note is that to a first approximation, those outputs that were predicted to be reversible are so.**

One final test was made to determine whether the cores were disturb sensitive, i.e., whether information was destroyed by repeatedly disturbing a core without rewriting. To determine this the cores were put in State 9 with $I_m = 700$ and then disturbed repeatedly from 1 to 4096 times with a 2/3 disturb pulse. The results of this test indicate that after an initial small change in the peak amplitude of the ONE output, no further change was noted. Figure 5.03i shows the outputs after 1, 64 and 4096 disturbs.

---

*See Section 2.03

**See Figure 4.02a



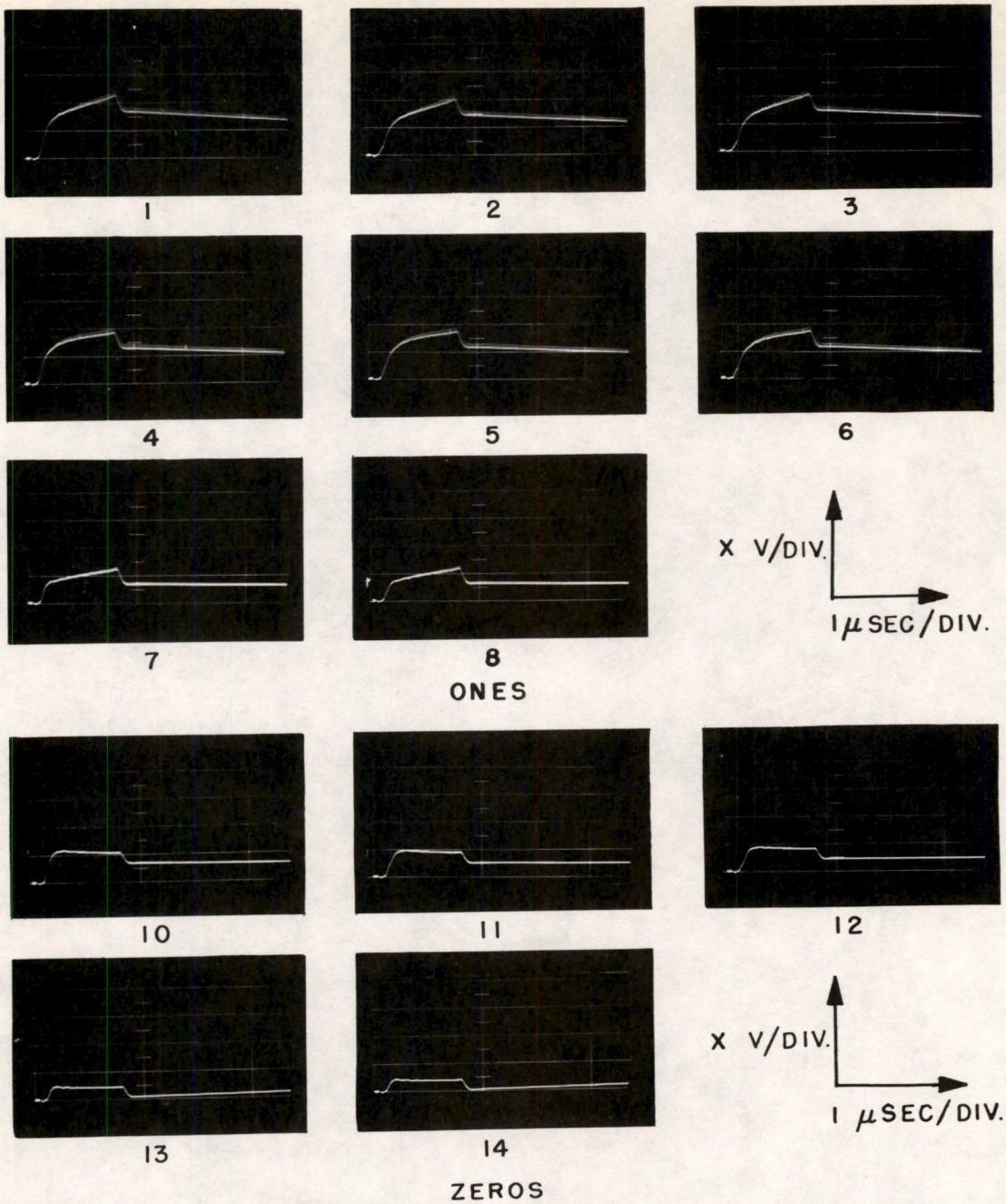
NOTES:

1. NUMBERS UNDER PICTURES REFER TO STATES OF FIG. 4.02a
2. THESE OUTPUTS ARE FOR 50 CORES MF 1326-B, DIE SIZE 394, LOT G92.

FIG. 5.03e

INTEGRATED V_1'S AT I_M = 650 ma.

A-59713

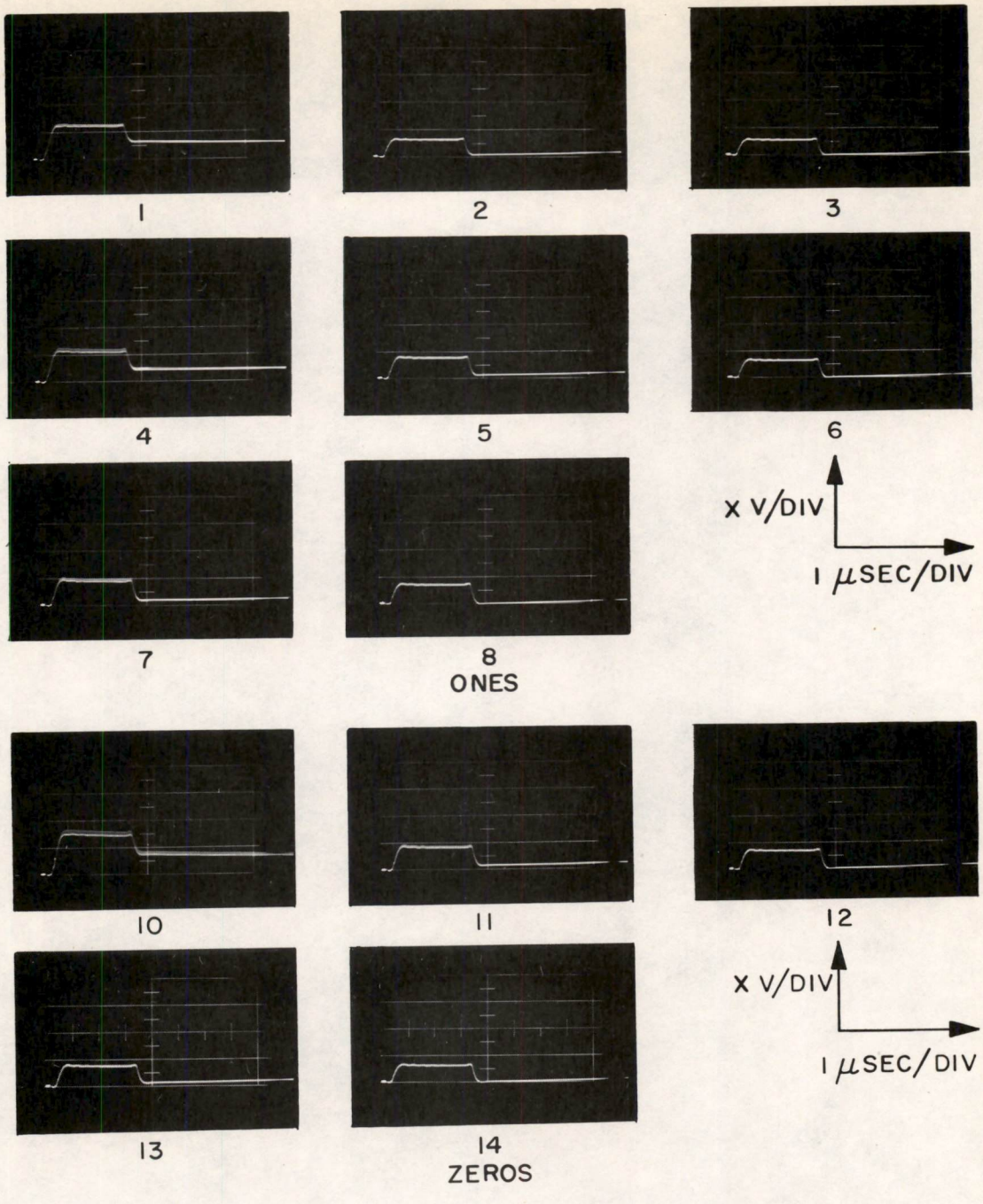


NOTES:

1. NUMBERS UNDER PICTURES REFER TO STATES OF FIG. 4.02a
2. THESE OUTPUTS ARE FOR 50 CORES MF 1326-B, DIE SIZE 394, LOT G 92.

FIG. 5.03f

INTEGRATED $V_{\frac{2}{3}}$'S AT I_M = 650 ma.



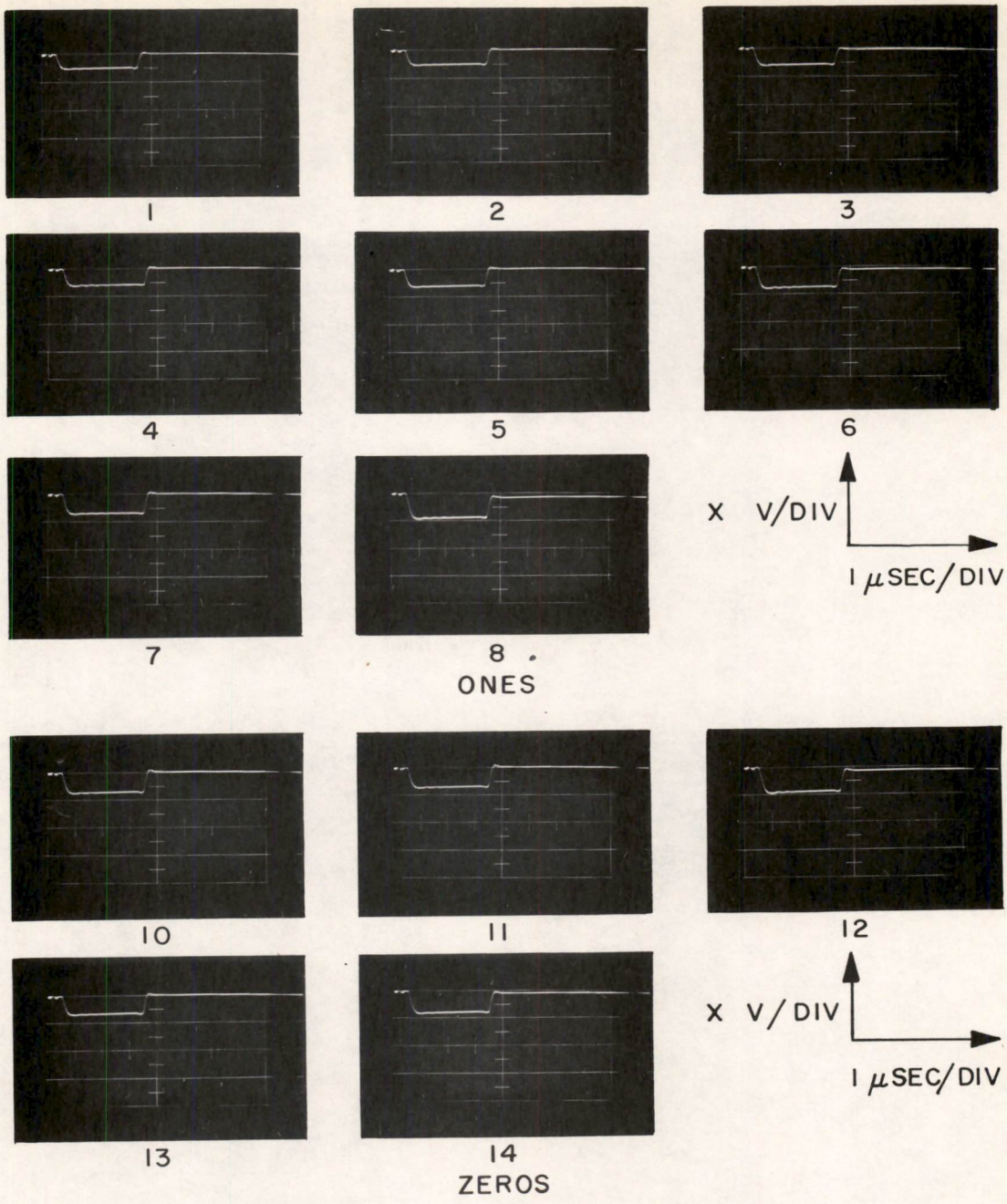
NOTES:

1. NUMBERS UNDER PICTURES REFER TO STATES OF FIG. 4.02 a
2. THESE OUTPUTS ARE FOR 50 CORES MF 1326-B, DIE SIZE 394, LOT G92

FIG. 5.03 g

INTEGRATED $V_{\frac{1}{3}}$'s AT $I_M = 650$ m.a.

A-59742



NOTES:

1. NUMBERS UNDER PICTURES REFER TO STATES OF FIG. 4.02a
2. THESE OUTPUTS ARE FOR 50 CORES MF 1326-B, DIE SIZE 394, LOT G92

FIG. 5.03h

INTEGRATED $V_{\frac{1}{3}}$'s AT I_M = 650 ma

TABLE 5.03b

A COMPARISON OF UNINTEGRATED AND INTEGRATED OUTPUTS

I_m=650 maa

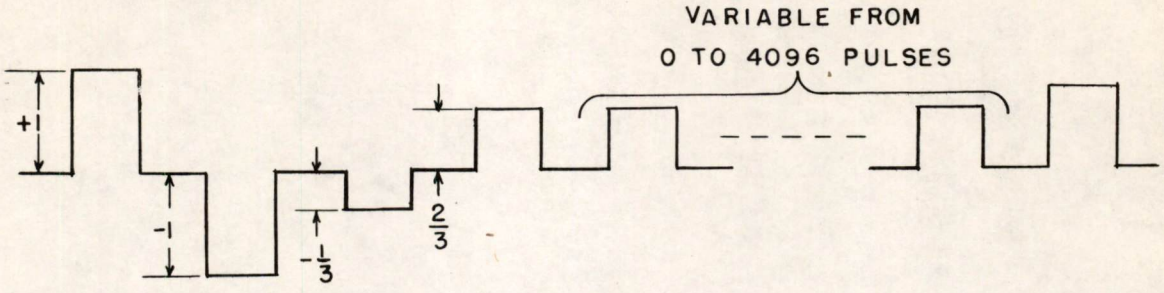
STATE	EXCITATION I_m	UNINTEGRATED OUTPUTS (Normalized)	INTEGRATED OUTPUTS (Normalized)
1	1	1.00	1.00
2	1	.98	.98
3	1	1.00	.97
4	1	.90	.89
5	1	.90	.89
6	1	.90	.89
7	1	.90	.82
8	1	.88	.80
9	1		
10	1	.02	.06
11	1	.02	.04
12	1	.02	.04
13	1	.02	.04
14	1	.02	.04
15	1		
1	2/3	.100	.136
2	2/3	.108	.116
3	2/3	.112	.121
4	2/3	.048	.109
5	2/3	.048	.092
6	2/3	.048	.096
7	2/3	.016	.052
8	2/3	.016	.052
9	2/3		
10	2/3	.006	.056
11	2/3	.008	.090
12	2/3	.008	.036
13	2/3	.008	.010
14	2/3	.008	.004
15	2/3		

TABLE 5.03b (Continued)

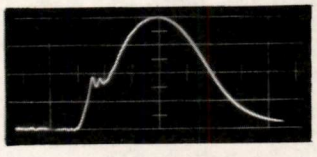
STATE	EXCITATION I_m	UNINTEGRATED OUTPUTS	INTEGRATED OUTPUTS
1	1/3	.020	.013
2	1/3	.005	.001
3	1/3	.004	.000
4	1/3	.010	.010
5	1/3	.005	.003
6	1/3	.004	.000
7	1/3	.006	.004
8	1/3	.005	.000
9	1/3		
10	1/3	.006	.014
11	1/3	.004	.009
12	1/3	.003	.000
13	1/3	.005	.003
14	1/3	.004	.000
15	1/3		
1	-1/3	-.010	-.000
2	-1/3	-.010	-.000
3	-1/3	-.012	-.001
4	-1/3	-.009	-.000
5	-1/3	-.010	-.000
6	-1/3	-.014	-.002
7	-1/3	-.010	-.000
8	-1/3	-.017	-.004
9	-1/3		
10	-1/3	-.007	-.000
11	-1/3	-.007	-.000
12	-1/3	-.011	-.003
13	-1/3	-.004	-.000
14	-1/3	-.007	-.001
15	-1/3		

NOTE: 1. The sensing time for the unintegrated data is .85 μsec. after the time marker, and for the integrated data 3.5 μsec.

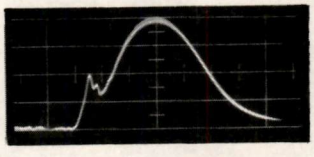
2. In both cases the data has been normalized with respect to the maximum output.



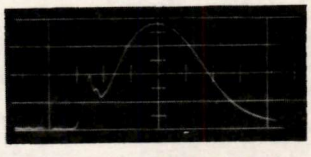
PULSE SEQUENCE



1 DISTURB



64 DISTURBS



4096 DISTURBS

FIG. 5.03 *i*

DISTURB SENSITIVITY AT I_M = 700 ma

CHAPTER 6

OPERATION OF AN 8x8x8x8 DIGIT PLANE

6.01 The Digit Plane

The data of Chapter 5 gave some insight into the sensing problem, but more experimentation was needed before any final decisions could be made as to the practicability of the system. Although the data indicated that with a single sense winding amplitude discrimination alone was not a satisfactory detection technique, the possibilities of either staggered selection or a pre-read disturb sequence followed by integration still remained to be investigated. Instead of predicting the results from single core data, more accurate information was obtained by testing the different schemes on an 8x8x8x8 digit plane, selecting different cores by manually switching the drivers from one coordinate line to the next.

The plane constructed for testing the different sensing schemes was made of MF1326B cores which had been tested for normal 2 to 1 operation, but had not been tested on the 3 to 2 basis. It was realized that the allowable variations in the fully selected ONE outputs were probably greater than could be allowed on the 3 to 2 basis, but it was felt that at sensing time, the different types of disturb voltages, which are of most concern in this study, would be uniform enough to give sufficiently accurate results. The plane was wired following a pattern similar to that shown in the schematic for a 4x4x4x4 plane (Fig. 4.01a). A cancelling sense winding was used i.e., if all the lines in any coordinate were similarly excited, half the cores would induce positive voltages in the winding and the remainder negative voltages. Fig. 6.01a is a photograph of the plane. In all there were ten #38 wires passing through each core, and the actual

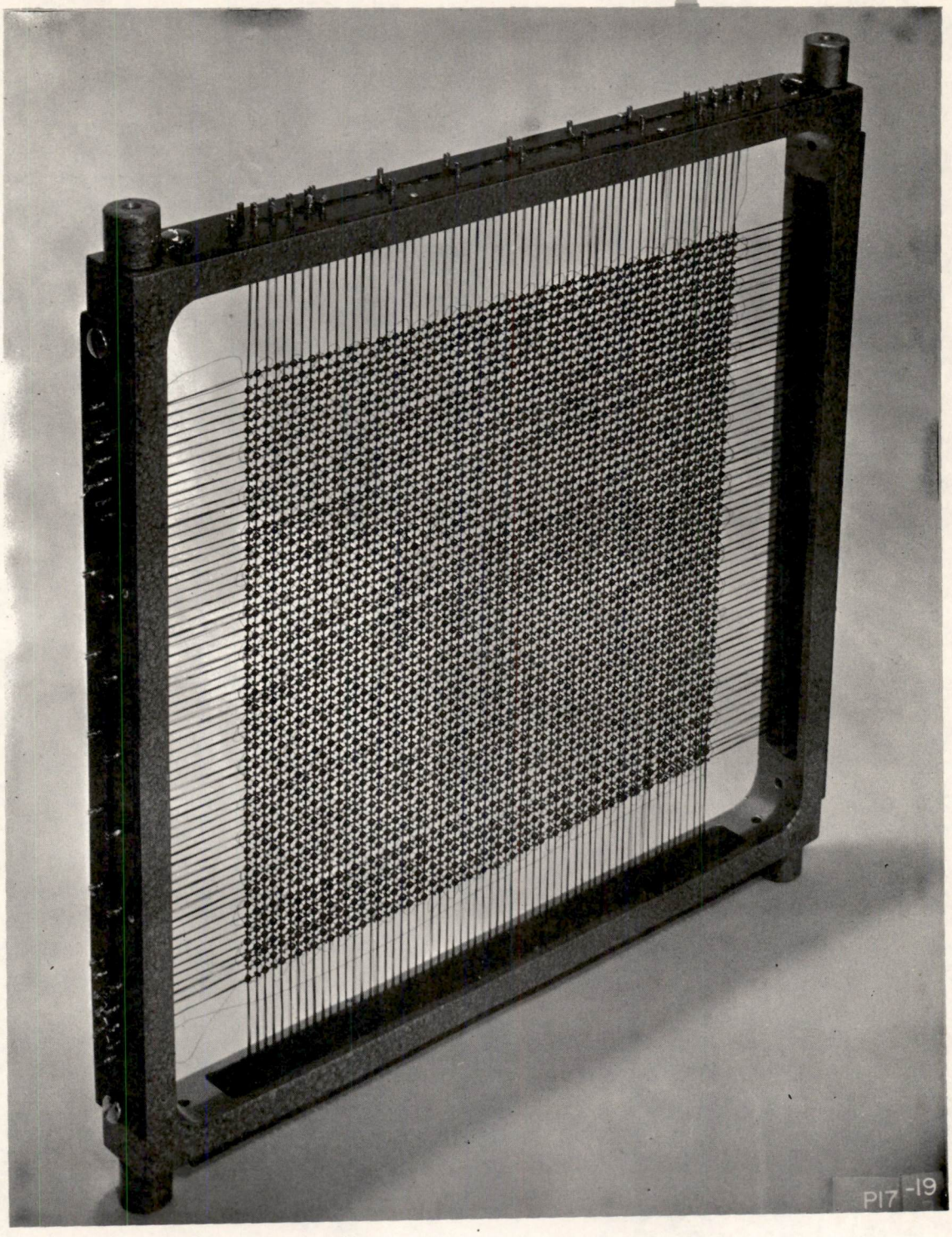


FIG. 6.01a

AN 8x8x8x8 MEMORY DIGIT PLANE

wiring time was approximately 50 hours, the wiring being done by a technician experienced in building 64x64 planes of the same physical dimensions.

6.02 The Memory-Plane Tester

Fig. 6.02a is a photograph of the memory-plane tester, and Fig. 6.02b is the block diagram. The equipment used was the same as that for the core tester with the addition of a balanced-input sense amplifier (Fig. 6.02c).

The tester was capable of doing the following:

1. Any one of four addresses could be selected manually through the use of toggle switches, and the four driving lines that comprised this group could be changed by resoldering.

2. At any of these addresses a simple read-write cycle, or a pre-read disturb sequence followed by a read-write cycle, or a staggered read-write cycle could be used.

3. All ONEs or all ZEROs (states 1 and 15, respectively) could be written by fully exciting the digit-plane winding.

4. Patterns that gave approximately the minimun ONE and maximum ZERO could be written by exciting the sense winding with $\pm I_m$. This would leave the cores of one polarity in a ONE state and those of the opposite polarity in a ZERO state, and would tend to maximize the magnitude of the net output from the disturbed cores.

6.03 Experimental Results

After making preliminary experiments at different current settings to determine the best operating range, the data were taken in the form of photographs, and those which seemed most significant are

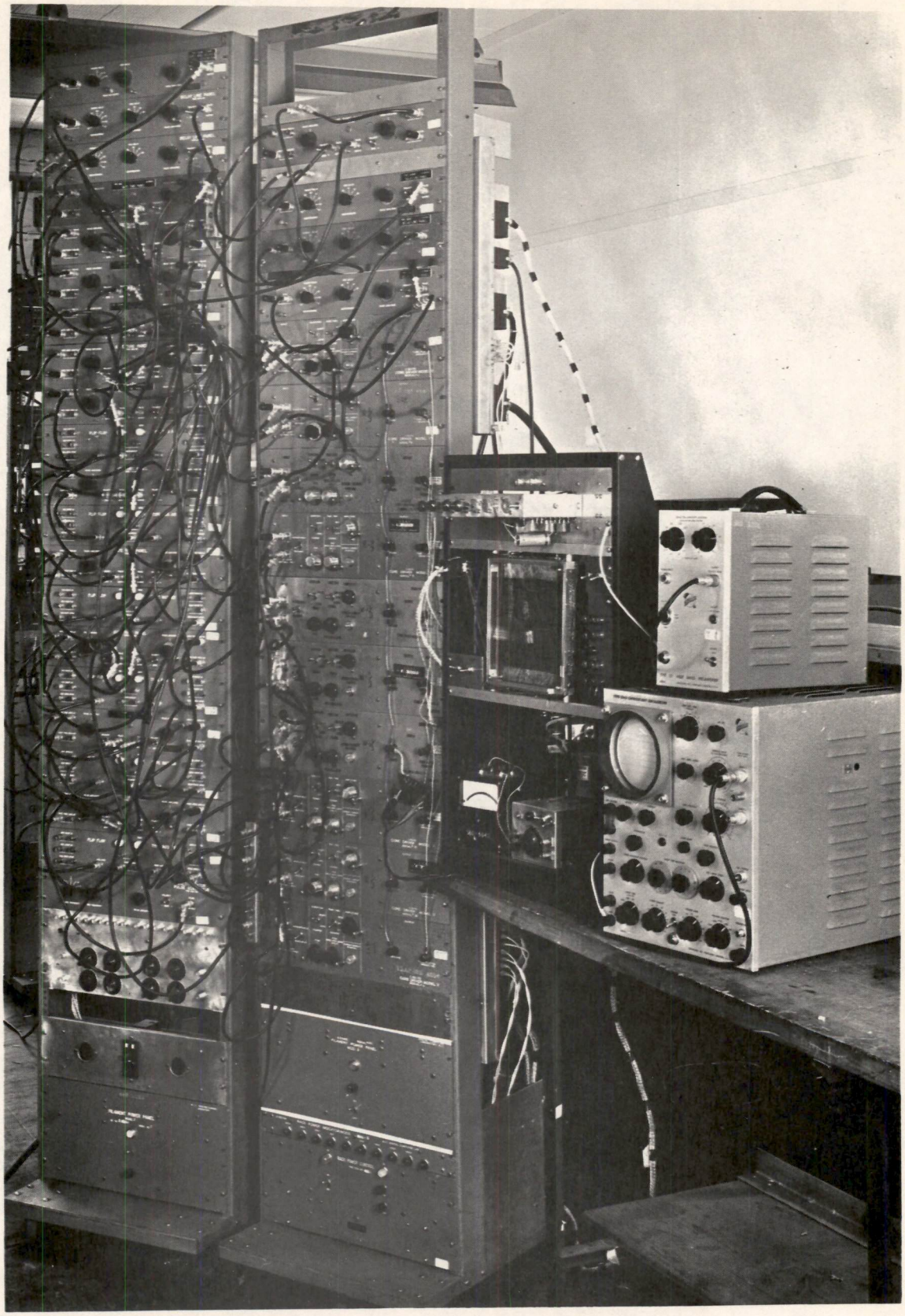


FIG. 6.02 a

MEMORY PLANE TESTER

A-59703

C-47145

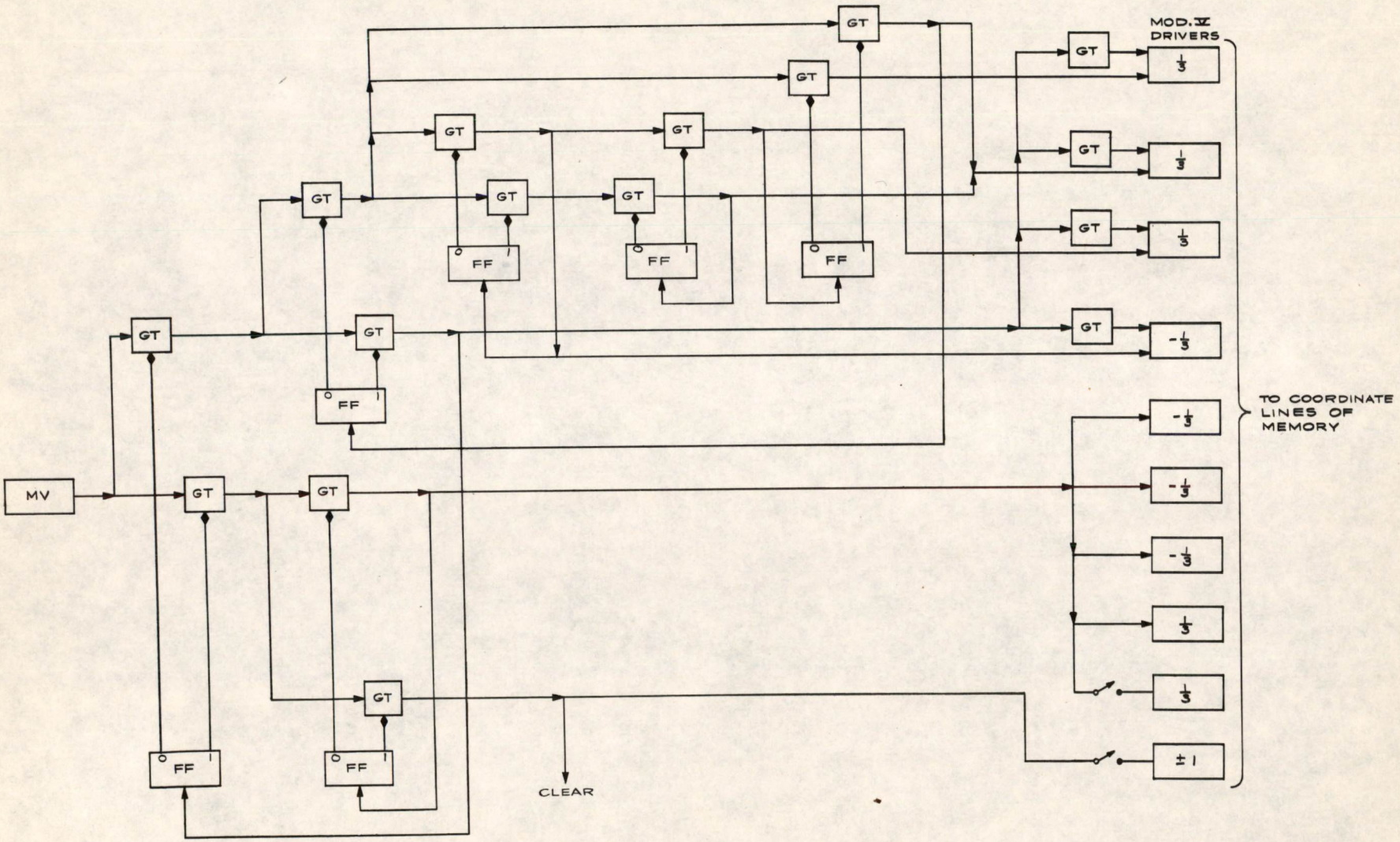
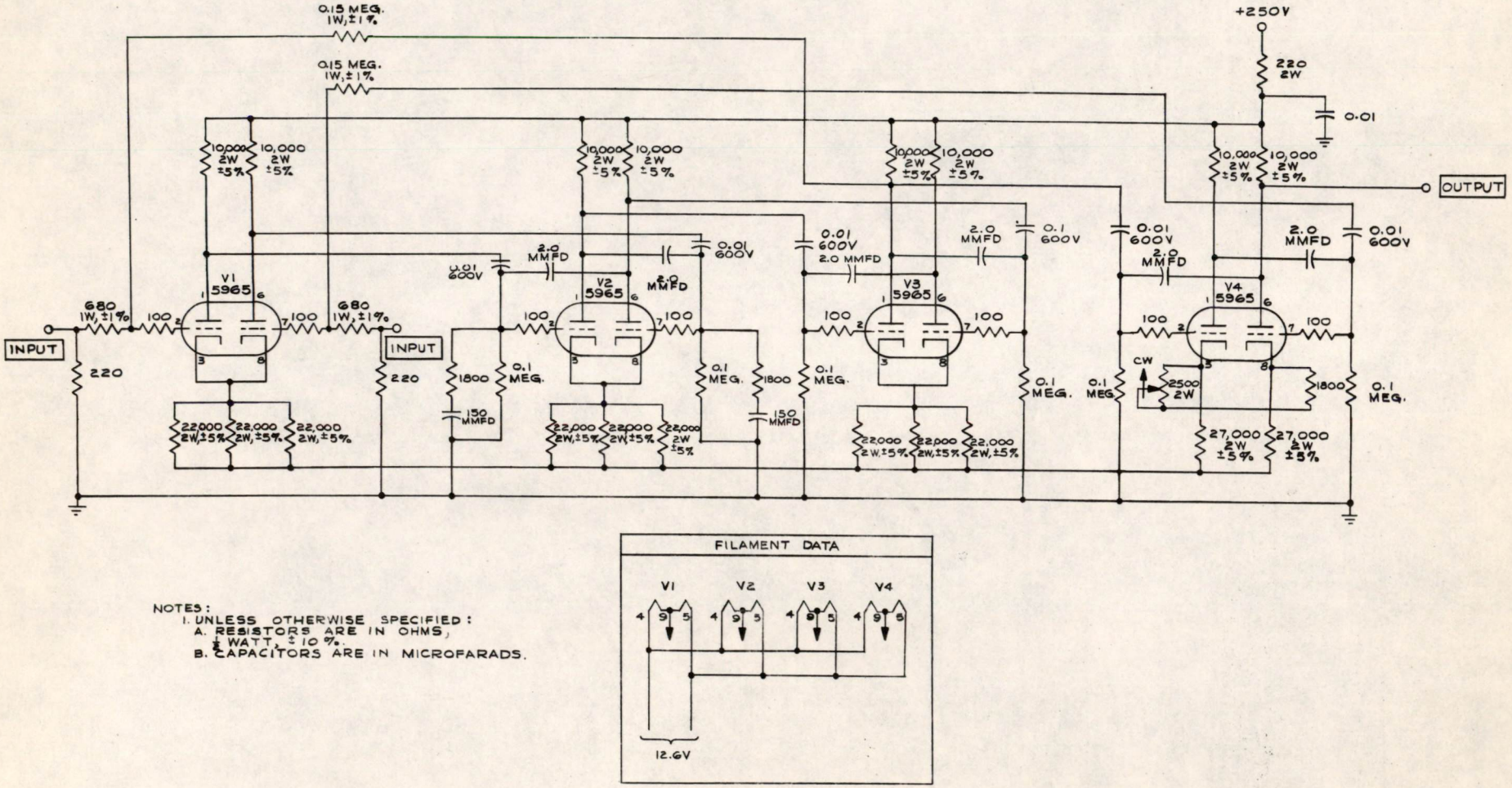


FIG. 6.02b
BLOCK DIAGRAM OF MEMORY PLANE TESTER

C-59747



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTORS ARE IN OHMS, ½ WATT, ± 10 %.
   B. CAPACITORS ARE IN MICROFARADS.

FIG. 6.02C

CIRCUIT SCHEMATIC, SENSING AMPLIFIER

shown in Figs. 6.03a through 6.03c.

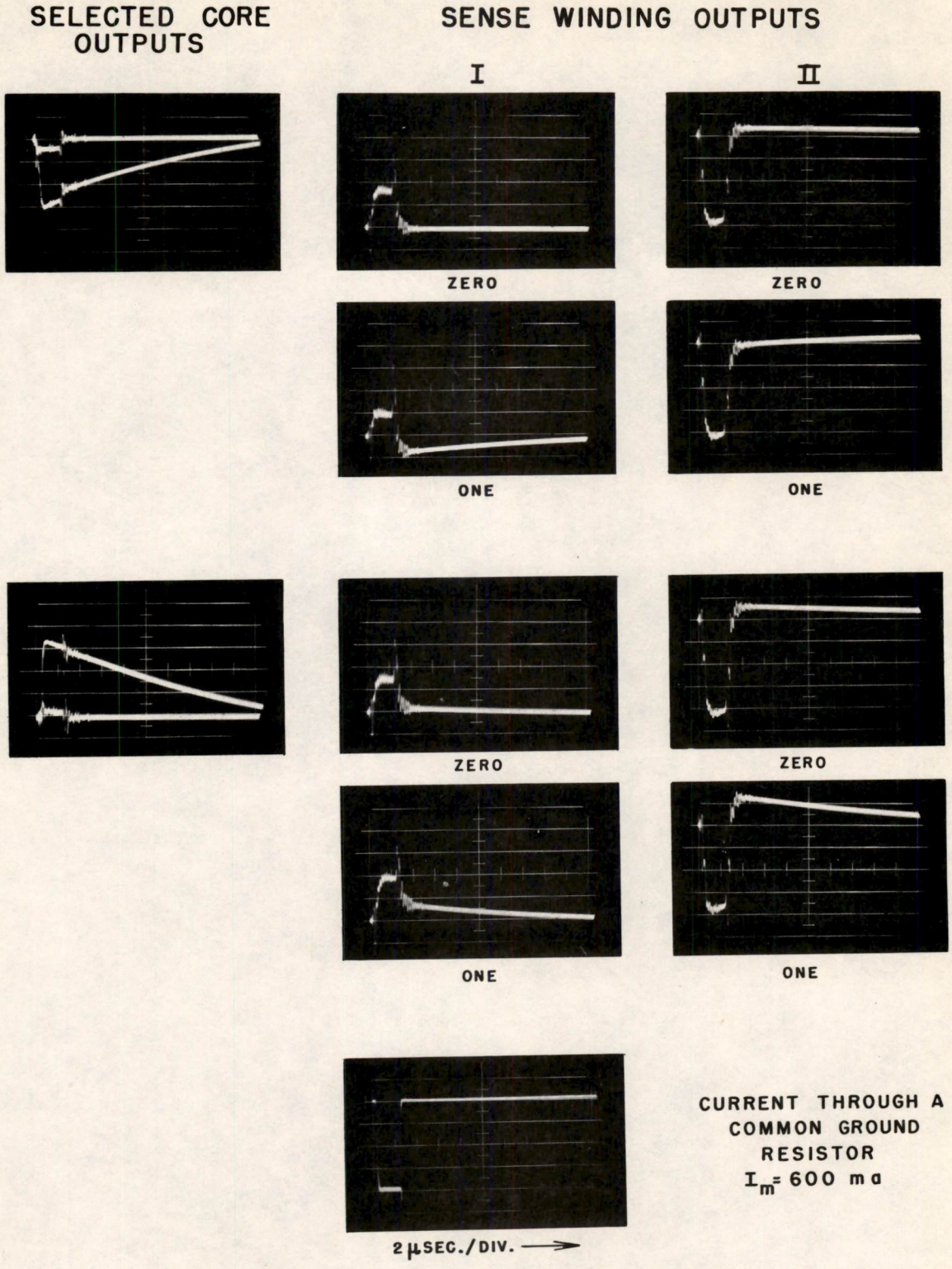
In the first tests that were made only amplitude discrimination was used, and as was predicted in Chapter 5, it was possible for the magnitude of a ZERO plus disturb voltages to exceed the magnitude of a ONE plus disturb voltages. Likewise, when the scheme involving a pre-read disturb and integration was used (Fig. 6.03a) although the results improved by an order of magnitude, there were cases where the magnitude of a ZERO plus disturb voltages was larger than the smallest magnitude of a ONE plus disturb voltages. The last scheme tried was the use of a staggered read, and this seemed to offer a promising solution.

The first data taken with the staggered read* were discarded when it was discovered that the results were in error because of air-flux pick-up. This pick-up was due to the fact that what was assumed to be a non-inductive sense winding was only partially so because of the position of the return lead.** The error was corrected, and Figs. 6.03b and 6.03c show outputs for various pattern sequences. An attempt was made to approximate the worst results that might arise in actual operation, but it should be observed from the photographs shown that, as would be expected, not only were the magnitudes of the outputs influenced by the pattern of information stored in the plane, but they were also influenced by the previous history.

The procedure used to obtain each sequence of photographs was first, the digit plane winding was excited with $\pm I_m$ to establish a pattern with all the cores in the same ONE state, and then a ONE and

* See Reference 20

** For a general discussion of sense winding geometry and its relation to the pick-up problem, see Reference 21.



NOTE: SEE TEXT FOR A DESCRIPTION OF THE DIFFERENT INFORMATION PATTERNS

FIG. 6.03 α

MEMORY PLANE OUTPUTS USING A PRE-READ DISTURB AND INTEGRATION

A-59768

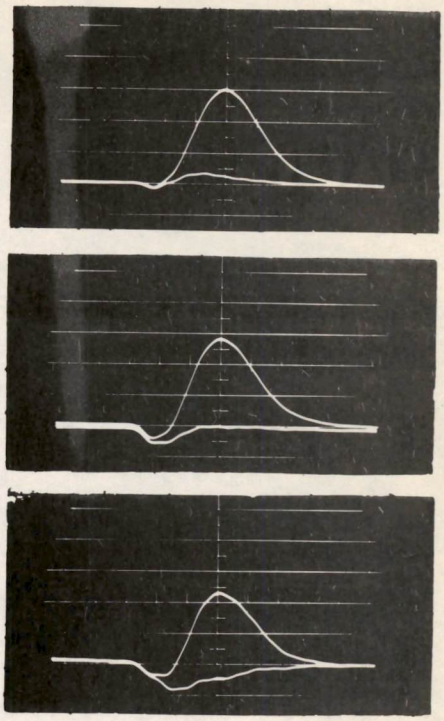
PATTERN SEQUENCE

ONE AND ZERO OUTPUTS

ALL ONES

CORES OF POSITIVE POLARITY ONES — CORES OF NEGATIVE POLARITY ZEROS

CORES OF POSITIVE POLARITY ZEROS — CORES OF NEGATIVE POLARITY ONES



ALL ONES

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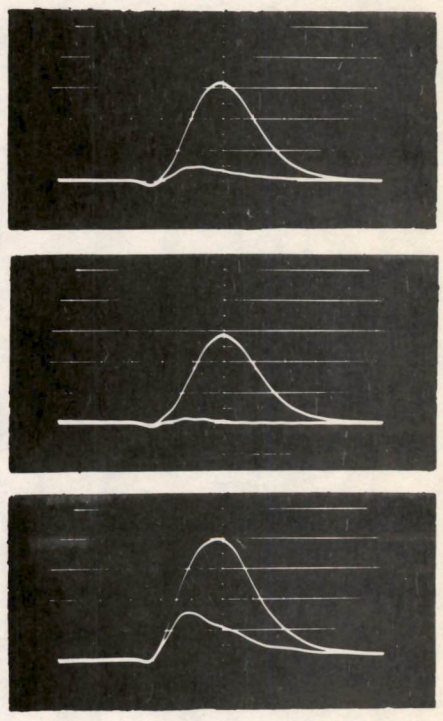
CORES OF POSITIVE POLARITY ONES — CORES OF NEGATIVE POLARITY ZEROS



0.5 μ SEC/DIV →

FIG. 6.03b

MEMORY PLANE OUTPUTS FOR A SELECTED CORE OF POSITIVE POLARITY, USING A STAGGERED READ WITH I_m = 630m.a.

A-61733
SHEET 1 OF 2

PATTERN SEQUENCE

ONE AND ZERO OUTPUTS

ALL ZEROS

↓

CORES OF POSITIVE POLARITY ZEROS — CORES OF NEGATIVE POLARITY ONES

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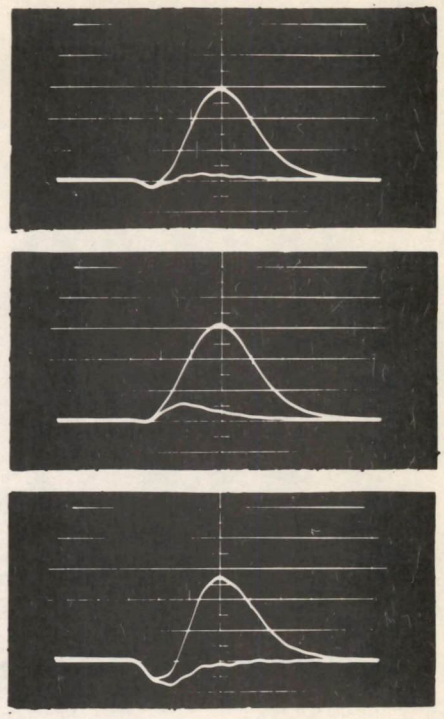
CORES OF POSITIVE POLARITY ONES — CORES OF NEGATIVE POLARITY ZEROS



ALL ZEROS

↓

CORES OF POSITIVE POLARITY ONES — CORES OF NEGATIVE POLARITY ZEROS

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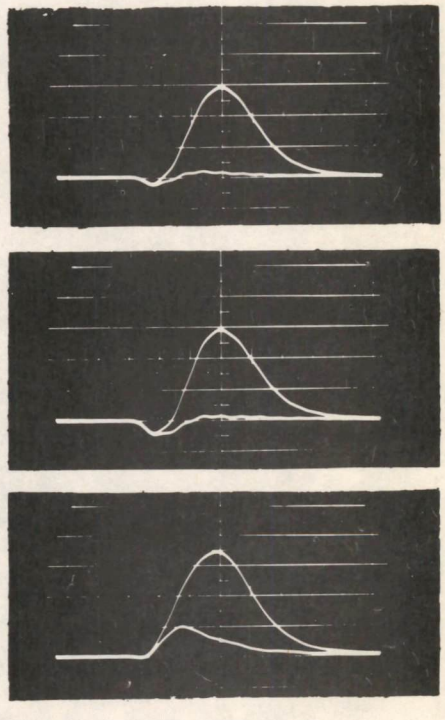
CORES OF POSITIVE POLARITY ZEROS — CORES OF NEGATIVE POLARITY ONES



0.5 μ SEC/DIV →

FIG. 6.03b

MEMORY PLANE OUTPUTS FOR A SELECTED CORE OF POSITIVE POLARITY, USING A STAGGERED READ WITH $I_m = 630$ m.a.

A-61733
SHEET 2 OF 2

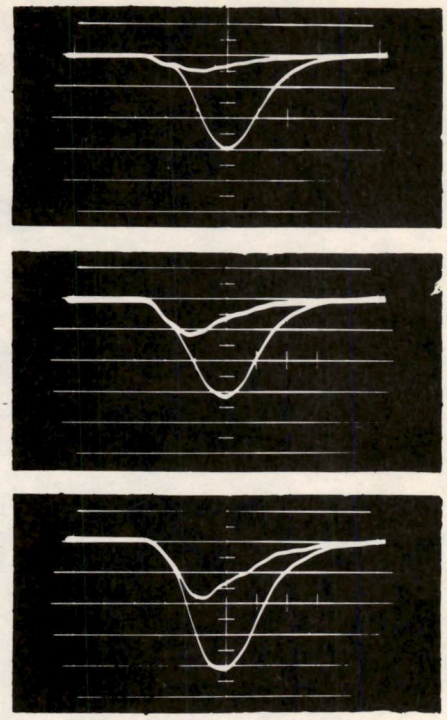
PATTERN SEQUENCE

ONE AND ZERO OUTPUTS

ALL ONES

CORES OF POSITIVE POLARITY ONES — CORES OF NEGATIVE POLARITY ZEROS

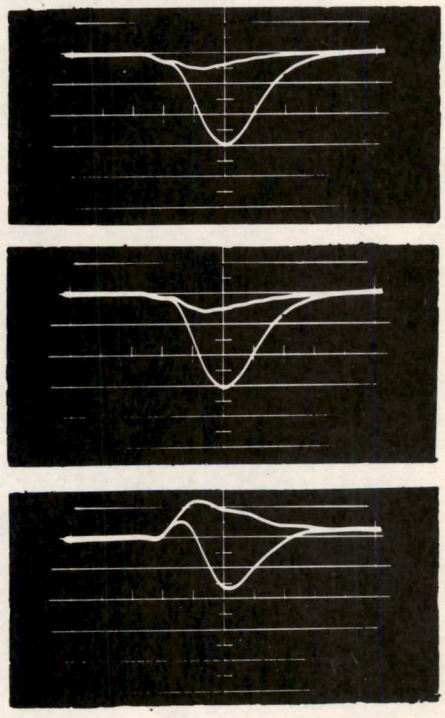
CORES OF POSITIVE POLARITY ZEROS — CORES OF NEGATIVE POLARITY ONES



ALL ONES

CORES OF POSITIVE POLARITY ZEROS — CORES OF NEGATIVE POLARITY ONES

CORES OF POSITIVE POLARITY ONES — CORES OF NEGATIVE POLARITY ZEROS



0.5 μ SEC/DIV ⟶

FIG. 6.03 c

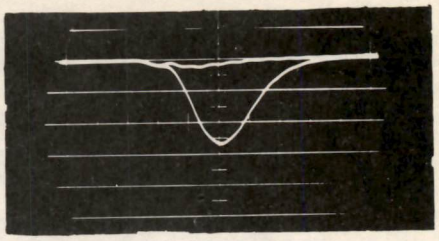
MEMORY PLANE OUTPUTS FOR A SELECTED CORE OF NEGATIVE POLARITY, USING A STAGGERED READ WITH I_m = 630 m.a.

A-61734
SHEET 1 OF 2

PATTERN SEQUENCE

ONE AND ZERO OUTPUTS

ALL ZEROS



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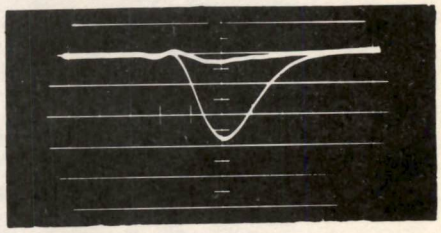
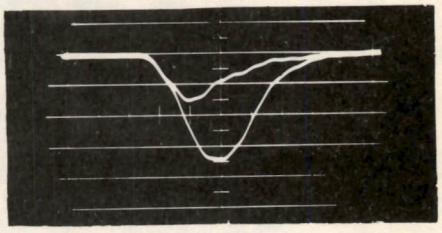
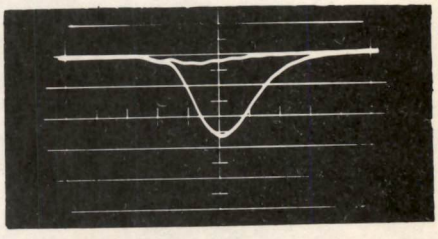


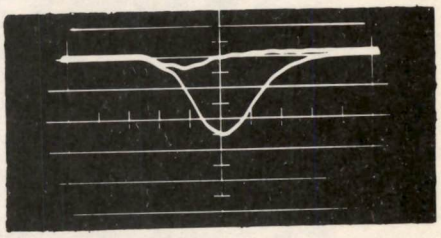
CORES OF POSITIVE POLARITY ONES — CORES OF NEGATIVE POLARITY ZEROS



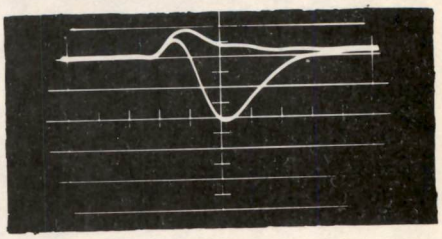
ALL ZEROS



CORES OF POSITIVE POLARITY ONES — CORES OF NEGATIVE POLARITY ZEROS



CORES OF POSITIVE POLARITY ZEROS — CORES OF NEGATIVE POLARITY ONES



0.5 μ SEC/DIV →

FIG. 6.03 c

MEMORY PLANE OUTPUTS FOR A SELECTED CORE OF NEGATIVE POLARITY, USING A STAGGERED READ WITH I_m = 630 m.a.

A-61734
SHEET 2 OF 2

ZERO output from a selected core were photographed. Next the sense winding was excited with $\pm I_m$ placing the cores of one polarity in a ZERO state and cores of the other polarity in the ONE state, and again the outputs were photographed. Finally, the sense winding was again excited to store the complement pattern in the plane and the outputs photographed.

A study of the data shows that although the margin is small, the smallest ONE does exceed the largest ZERO, and when it is recalled that the cores were not tested for a 3-to-2 selection scheme, the results are encouraging. It should also be noted that the magnitude of the difference between the smallest ONE and largest ZERO for the positive core chosen is a good deal larger than that for the negative core chosen, and this indicates that there is an appreciable variation in the core outputs, both fully selected and disturb outputs, and that careful core testing at the operating currents would greatly improve the results.

6.04 Conclusions

The data already taken indicate that a more extensive analysis of the proposed system is well worthwhile. It was shown that a core will hold its information even when repeatedly disturbed and that the major problem is due to disturb outputs masking the signal. For the 4096-bit digit plane, the effect of the disturb outputs is reduced by the use of a staggered read to the point where successful operation seems possible.

To further evaluate the proposed system, a comparison can be made with a comparable 4096-register memory using a 2-coordinate read–3-coordinate write. A 64x64 digit plane will require at least 2(64+64)=256 driving cathodes, whereas an 8x8x8x8 digit plane will require 2(8+8+8+8)=64 or 1/4 the former number. The excitation of each driving line in the

2-coordinate system is $I_m'/2$, and in the 4-coordinate system only $I_m''/3$ where the value of I_m is of necessity less for the 4-coordinate case, and experimental results indicate that the current per driving line for this system would be about 1/2 the current for the 2-coordinate system. Although the current is less for the 4-coordinate case, 1/8 of the total array of cores must be excited by each driving line as compared to 1/64 for the 2-coordinate case, and it may be necessary to use a more complicated driving circuit in the former system to obtain a comparable rise time.

In the 2-coordinate system, two 64-position crystal matrices are needed and because of the considerable load this presents, the flip-flops which control the matrices must be followed by cathode followers. With the 4-coordinate system, four 8-position matrices are needed, and the load is reduced to the point where the flip-flops could probably drive the matrices directly.

The magnitudes of the total disturb outputs can be compared roughly by determining the "core-amperes" for each case. That is, the number of excitations received by each core summed over all the cores in the plane. For the 2-coordinate case as operated with no staggering

$$\text{"core-amperes"} = 128 \times \frac{I_m'}{2}$$

and for the 4-coordinate case with staggering

$$\text{"core-amperes"} = \frac{4096}{8} \times \frac{I_m''}{3}$$

Since $\frac{I_m'}{2} \approx \frac{2I_m''}{3}$ the "core-amperes" increase roughly by a factor of 2 for the 4-coordinate case. If the hysteresis loop were linear in this region and if the loops for each case were the same, then twice the

disturb output could be expected for the 4-coordinate system. However, the hysteresis loop is not linear and therefore, the smaller excitation in the 4-coordinate system produces outputs which are less than would be encountered if the loop were linear. On the other hand, the loop traversed in the 2-coordinate system is larger and has smaller slopes, and this would tend to decrease the size of the outputs as compared to the 4-coordinate loop. These two factors then are seen to work in opposite directions and as a rough approximation might be considered to cancel one another.

Another factor which must be considered is that the ONE output for the 4-coordinate case, which is, after all, the signal to be detected, is about 1/2 as large as the ONE obtained for the 2-coordinate case. The net result, then, is that very roughly the ONE to ZERO ratio for the 4-coordinate system using staggering should be about 1/4 that obtained for a comparable 2-coordinate system not using staggering; the photographs show it is somewhat worse than this.

One final comparison to be made is between the memory cycle times. These times are approximately 6μsec for the 2-coordinate system and 9μsecs. for the 4-coordinate system.

In summarizing the results, it can be said that if a smaller working margin and longer memory cycle are allowable, a considerable reduction in driving cathodes can be made by using a 4-coordinate read–5-coordinate write system.*

* Since the time this work was begun, better cores have been developed and experimental work has also been done on diode mixing at low levels of signals from multiple sense windings. These further developments indicate that a reliable sensing system can be developed.

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R-216

THE 16 BY 16 METALLIC MEMORY ARRAY, MODEL 1

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DIGITAL COMPUTER LABORATORY

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Report R-216

THE 16 x 16 METALLIC-CORE MEMORY ARRAY, MODEL I

by
Bernard Widrowitz

DIGITAL COMPUTER LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Cambridge 39, Massachusetts

September 25, 1952

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FOREWORD

This report contains a history and some technical details of the development of our first two-dimensional, coincident-current, magnetic-core memory for binary digital computer use.

The work described herein received its impetus from the research of two men: Jay W. Forrester, who proposed the coincident-current selection scheme, and William N. Papian, who systematized the pulse-testing of magnetic cores and constructed an experimental 4-cell memory.

Signed Bernard Widrowitz
Bernard Widrowitz

Approved JWF
Jay W. Forrester

ABSTRACT

A 16 x 16 memory array of small molybdenum permalloy cores has been assembled and tested over a period of some months. Fairly reliable operation despite a rather wide dispersion of core characteristics is encouraging.

I - INTRODUCTION

A. PRINCIPLES OF OPERATION

The operation of a coincident-current, magnetic-core memory depends fundamentally upon the "bi-stable" properties of the cores and the mechanism of coincident-current selection.[2]

Ferromagnetic toroids having rectangular hysteresis loops can be magnetized in either of two directions, arbitrarily called "zero" and "one". A magnetized core is a "permanent" magnet whose rectangular hysteresis properties allow it to be switched to its alternate state of flux retention only when it is excited by a magnetomotive force greater than or equal to its "coercive" force.

1. Coincident-Current Selection

If a core is excited by two windings, X and Y, the currents in each may be made small enough so that they individually provide less excitation than the "coercive" force. They may be made large enough, however, so that when applied coincidentally in time, the sum of their magnitudes is greater than the "coercive" force and switching is possible.

Many similar cores containing two windings may be arranged in a two-dimensional matrix where groups of X windings are connected in series and groups of Y windings are also connected in series. A combination of a certain X line and a certain Y line

2. Superscripts refer to similarly numbered entries in the bibliography.

identifies a core of the matrix. Thus, a single selected core in the two-dimensional system may be switched when currents are applied coincidentally to corresponding X and Y lines in such directions that the two components of magneto-active force add algebraically to cause the desired operation. This method is not restricted to two-dimensional memories, and may be generalized for n-dimensions.[1]

2. Disturbances

In the two-dimensional system described above, cores on X and Y lines common to the selected core are "disturbed" by the half-amplitude excitations if these happen to be in directions to cause switching. Disturbances reduce the amplitude of residual flux in a core. This flux reaches a steady-state value (usually 20% or 30% less than that of a freshly switched core) after many disturbances. As long as the non-selected core has a disturbing excitation which is not greater than its "coercive" force, this condition appears, rather than a relaxation toward the zero flux level.

The cores used in this memory were not bi-stable in a strict sense. That they were able to retain most of their residual flux in the face of disturbance is all that is to be implied by the expression "bi-stable". It is believed that ideal cores with perfectly rectangular hysteresis loops would actually be bi-stable.

3. Current-Selection Ratio

The larger the magnitude of the excitation delivered to the selected core, the faster that core switches; however, the greater are the disturbances, and the narrower will be the current margins for reliable use. It is desirable to switch the selected core rapidly because switching time is the most significant part of total time required to "read" or "write" at a given address (core).

In designing a coincident-current memory, one always wishes to impart the most excitation with the least disturbances. The ratio of the excitation of the selected core to the greatest disturbing magnitude is called the selection ratio.

The selection ratio is a function of the configuration and connections of the driving lines of the memory. It has a value of 2 for the two-dimensional system described above. If the total (X+Y) excitation of the selected core is called I_m, the disturbing excitations are $\frac{1}{2}I_m$ in magnitude. Another two-dimensional system may be obtained by placing a Z winding on each core in addition to the X and Y. All of these Z windings must be in series. The selected X and Y lines then draw $2/3\ I_m$, while $-1/3\ I_m$ is applied to the Z line. The selected core receives I_m, and the disturbing excitations are either plus or minus $1/3\ I_m$ depending on whether or not the disturbed core is on a selected X or Y line. The selection ratio is therefore 3, the "best possible" two-dimensional current-selection ratio.[1]

4. Sensing (Read-out)

As we have seen, it is possible to set any core in the two-dimensional system in either direction (i. e., to write a "zero" or a "one"). To read out the information stored, we have only to write a "zero" into the selected core. If a "zero" is already stored, no switching occurs; if a "one" is stored, switching takes place. A sensing winding, threaded through every core in the system, is able to pick up an induced voltage if any core switches, so that it is possible to determine the state of the selected core prior to the reading operation.

Reading is destructive and clears the memory core. If it is necessary to retain the information in a core for further reading, provision must be made for re-writing after each read-out.

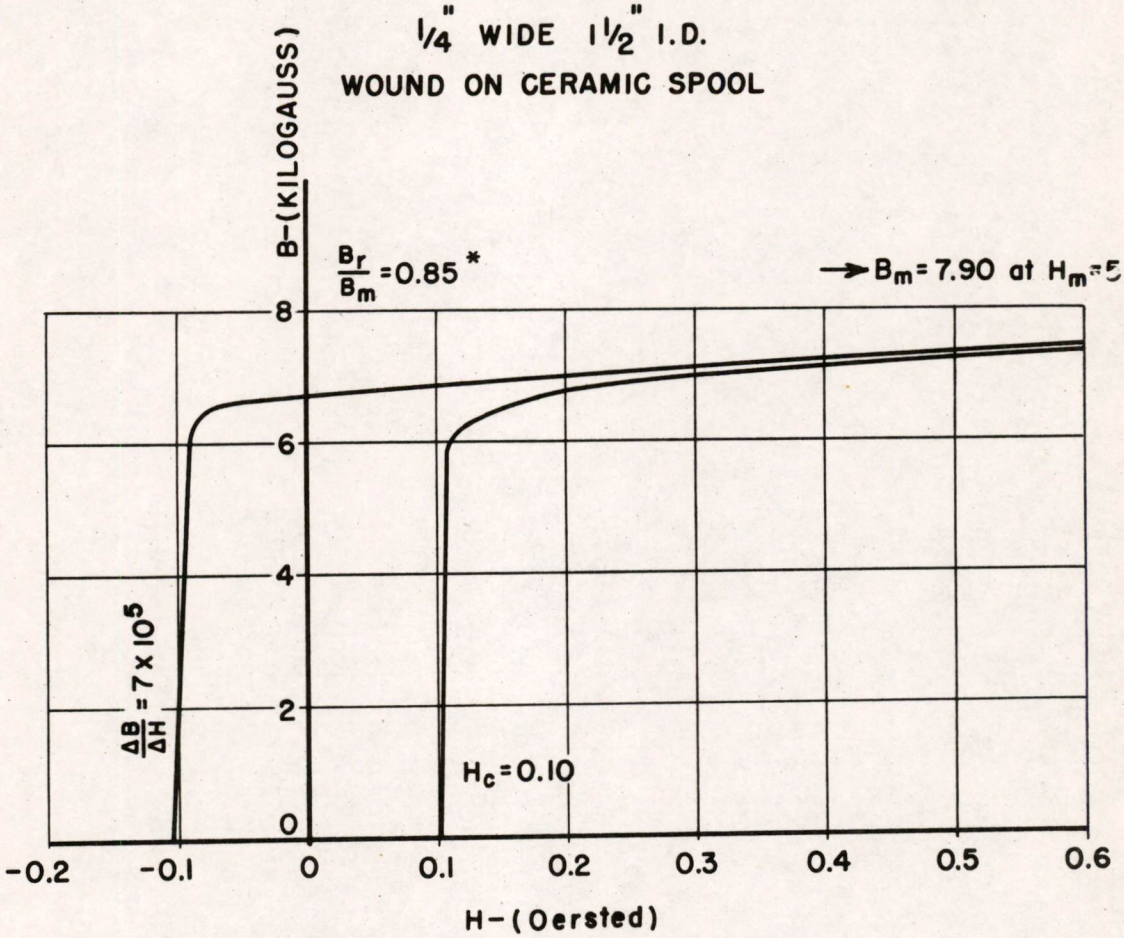
B. WINDINGS AND CORES

At the outset, it was decided that the cores were to have straight-line, single-turn windings, driven by vacuum tubes. The sensing winding was also to be single-turn.

The cores to be used were made of molybdenum permalloy, 1/4 mil thick tape, 1/8" wide, wound 5 wraps deep on a ceramic bobbin so that the diameter of the path of the metal is 3/16". These cores were fabricated by Magnetics, Inc. The d-c saturation hysteresis loop for a core of this type of material is shown in Figure 1.

D-C HYSTERESIS LOOP
CORE NO. 216

79-4 PERMALLOY
0.26 MILS
1/4" WIDE 1 1/2" I.D.
WOUND ON CERAMIC SPOOL



* $\frac{B_r}{B_m}$ = 0.915 for B_m = 7.45

CURVE NO. 5112
ARMCO RESEARCH LABORATORIES
4-13-51

Fig. 1

A-50265

II - CORE TESTING

Considerable variation in properties was found to exist among the cores. Since these cores would be excited by common driving lines in a coincident-current memory, and would have their flux paths linking a single sensing or pickup winding, it was quite important to select those cores whose characteristics clustered as closely as possible.

Standards of comparison were established to check each core for switching speed and voltage generated in a single turn, when switched under an excitation of I_m. The single-core pulse tester (described in reference 4) was used exclusively in the acceptance testing. The waveforms of the voltages induced by the cores when driven by identical currents on the pulse tester allow grading with respect to the above characteristics. From the 500 cores available, 256 cores were to be selected. It was desirable to maintain a history of each core. To facilitate this, the cores were color coded.

After testing 50 of the cores, W. Papian selected two cores, numbers 1 and 9, as standards whose properties would most likely bound those of the final 256.

The single-core pulse tester was set to simulate memory operation with a 2-to-1 selection ratio in current. Driving currents were optimized (when averaged over cores 1 and 9, best

combination of one-to-zero amplitude ratio, switching speed, and ability to withstand non-selecting disturbances). The waveforms of cores 1 and 9 were grease-penciled on the scope face, and the regions were labeled as shown in Figure 2.

The following production testing procedure was initiated: a jig was made that could accommodate a string of 10 cores in addition to the standards 1 and 9. This jig was plugged into the single-core pulse tester (Figure 3). A small pickup loop was threaded through a core and clipped onto the scope input. The scope and pulse tester were checked with each group of 10 cores by comparisons of the outputs of cores 1 and 9 against the grease-pencil curves on the scope. A single quantity could describe a core for acceptance consideration. As found by experiment, all cores having the same amplitude of voltage output per turn at some time after being excited (see vertical grease-pencil lines on Figure 2) were fairly similar with respect to their other critical properties.

The results of the pulse test are given in Figure 4. The distribution was not smooth because the widths of the grading regions were not identical. Also the positions of the grading boundaries were judged visually. The largest ratio of switching outputs of any two accepted cores was about 1.6 to 1.

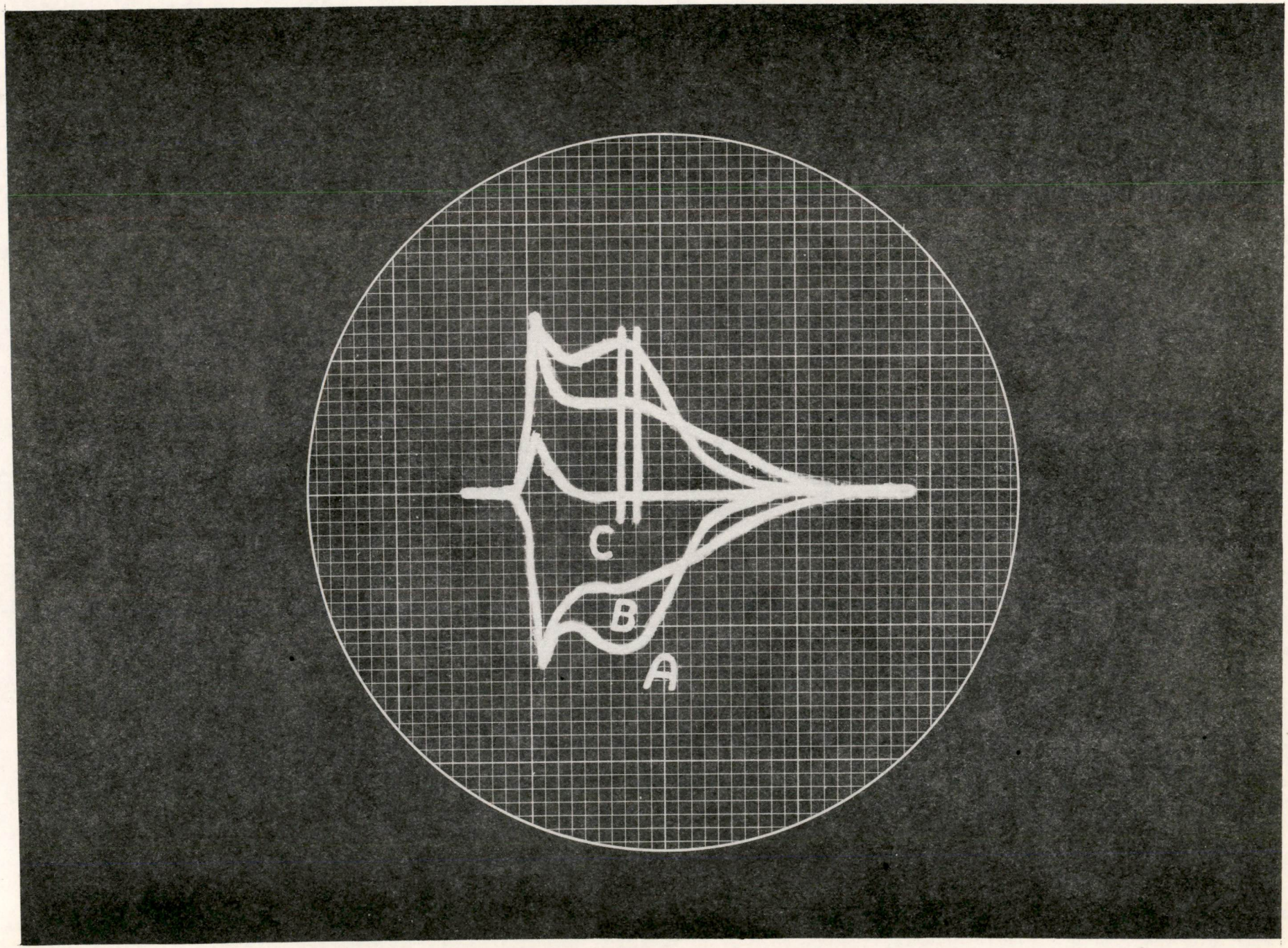


FIG. 2
PULSE TEST TEMPLATE

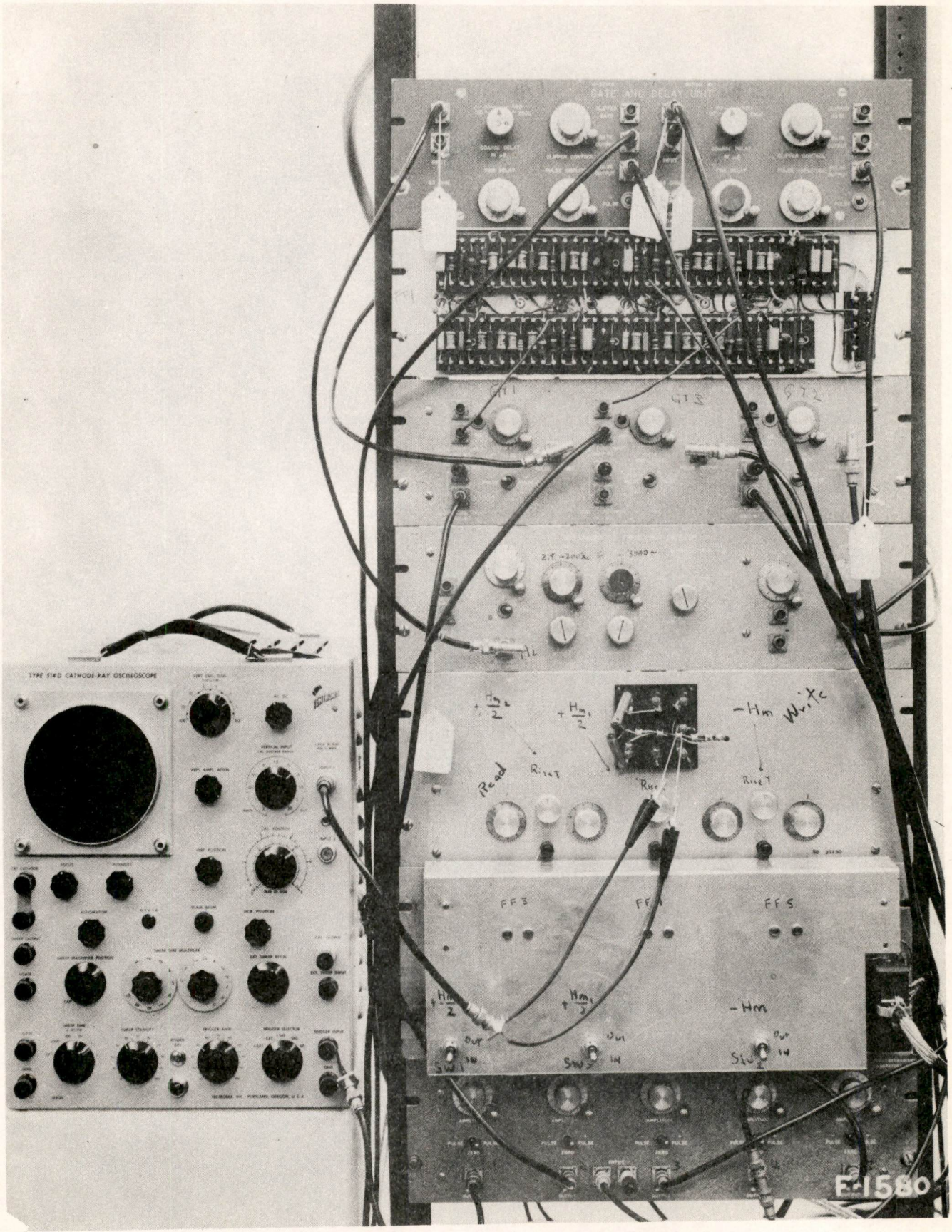
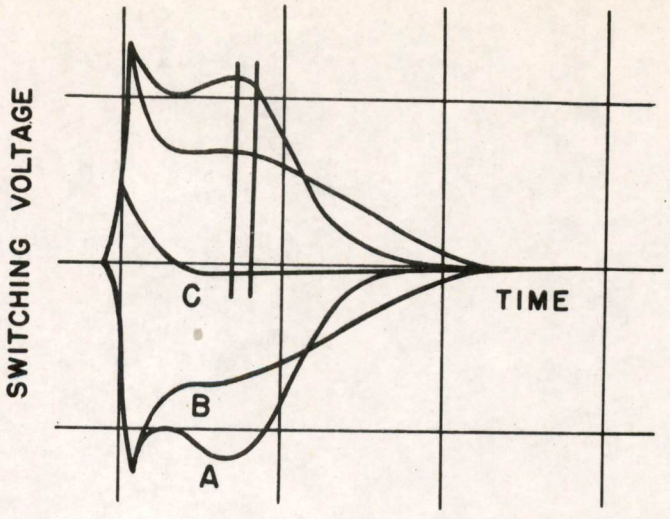
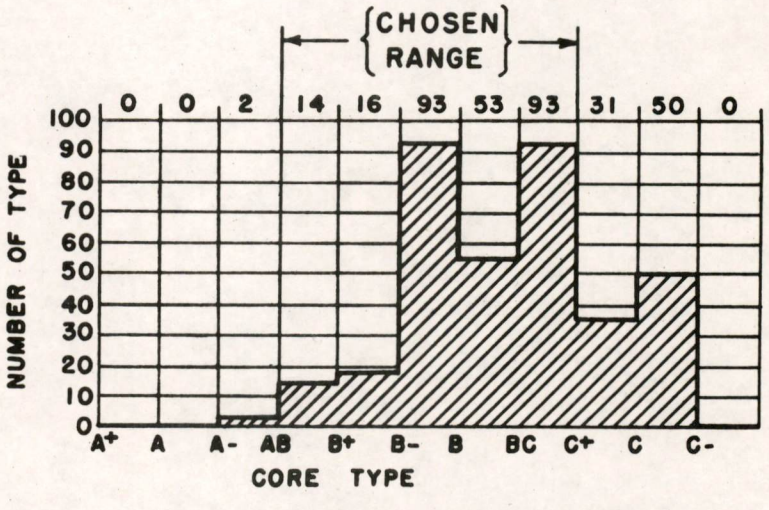


FIG. 3
SINGLE-CORE PULSE TESTER AND
JIG FOR PRODUCTION CORE TESTING

A-52347



A SKETCH OF TEST PATTERN



CORE TYPE DISTRIBUTION

LEGEND:

AB: IF ON BOUNDARY OF A AND B
B: IF IN REGION B
BC: IF ON BOUNDARY OF B AND C
C: IF IN REGION C
+ AND − INDICATE POSITION IN A REGION

FIG. 4

RESULTS OF SINGLE-CORE PULSE-TESTING

A-52359

III - DESIGN OF THE 16 x 16 ARRAY

After 256 cores were selected, the next step was to design and build the memory array. An array is a mesh of driving lines arranged so that it provides a supporting matrix for the memory cores.

The array was designed to have 16 X addresses, 16 Y addresses, and one Z address. The driving-current sources were able to draw current only in a single direction; and, because it was necessary to provide for core driving in both directions, two sets of X, Y, and Z lines were planned. A sensing winding was to be threaded through every core in the array in addition to the above; thus, a total of seven lines were concurrent at each core.

A 4 x 4 model of the wiring is shown in Figure 5. The X and Y coordinates were chosen arbitrarily. Current flowing from left to right was called "read", or "write 0", while current from right to left was called "write 1".

There were two reasons for a diamond rather than a square matrix. First, the ratio of inside diameter to length of bore of a core was such that it was impossible to pass two straight mutually perpendicular lines through it. Second, the diamond shape allowed short lead connections to the X drivers above and the Y drivers below the array.

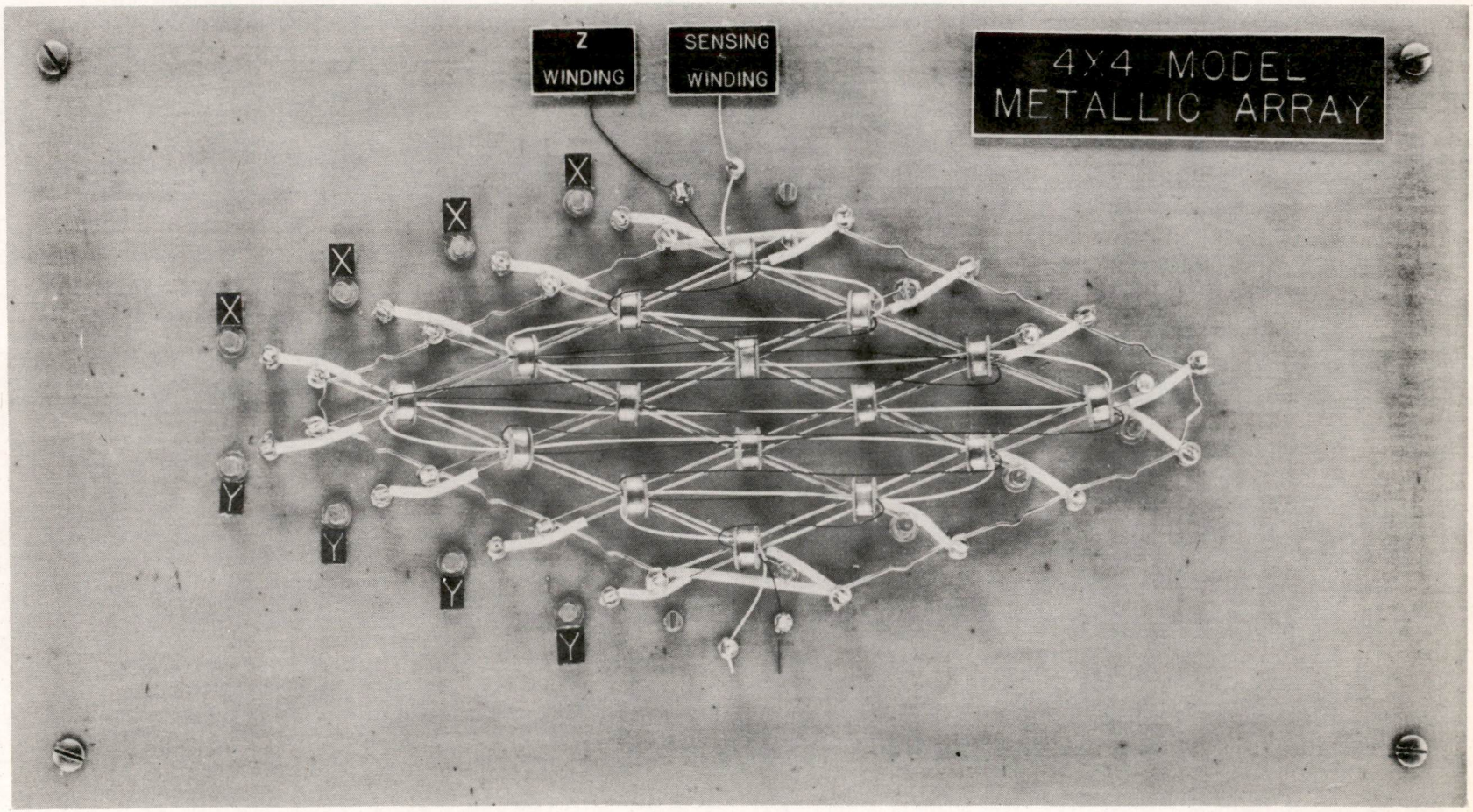


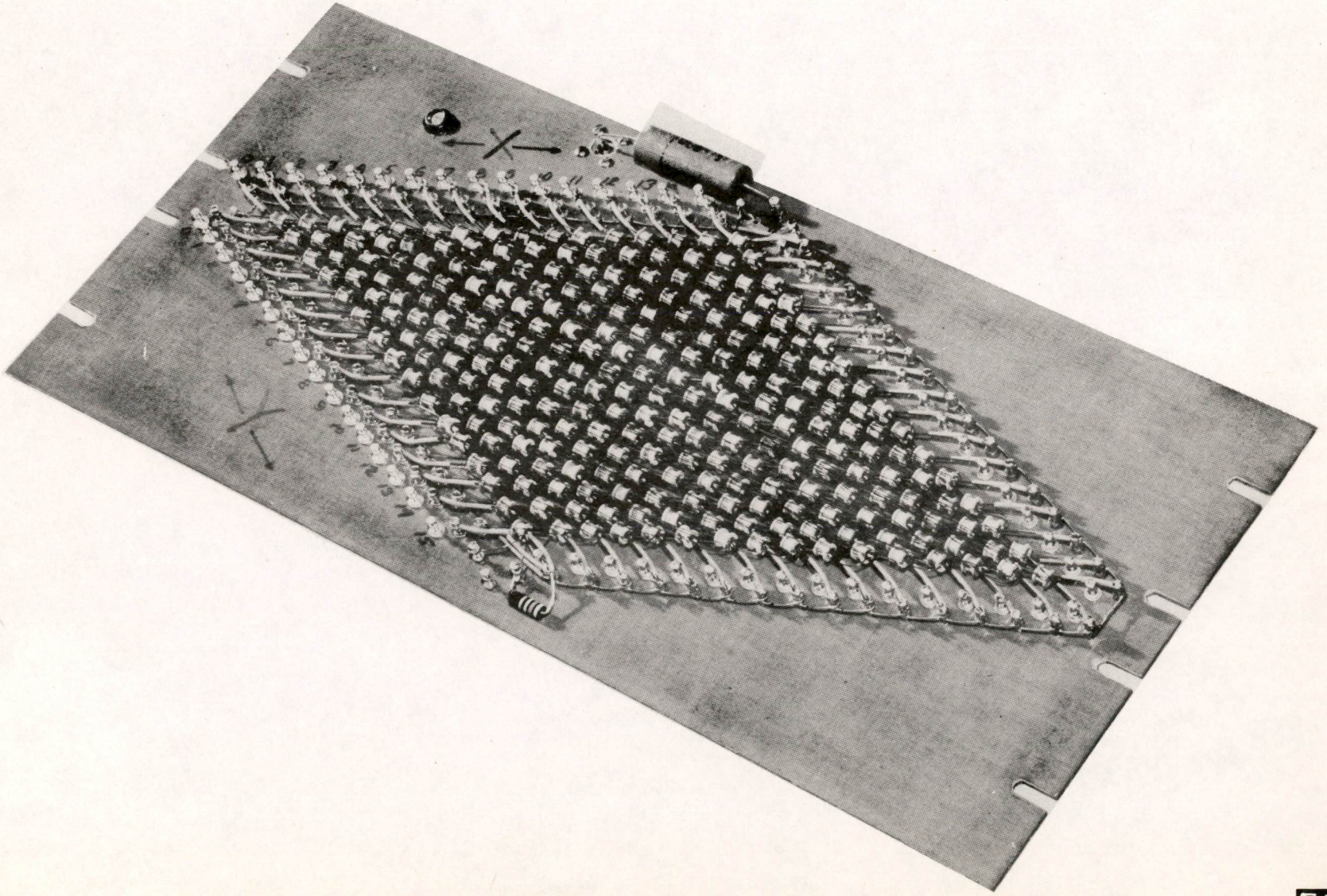
FIG. 5

4x4 MODEL OF THE METALLIC CORE ARRAY

F-1581

The sensing winding was drawn through every other core (along any X or Y line) in the same direction. This was quite different from the Z-dimension "write 1" line, which goes through every core from left to right in the positive sense. The sensing winding and only one Z-dimension winding are shown for clarity and contrast. The sensing winding was designed so that read-out pulses from non-selected cores (noise) would cancel. A discussion of this effect in a 4-core memory may be found in Engineering Note E-406.[5] A consequence of the weaving of the sensing winding is that the sensing amplifier had to be made to operate on positive-going and negative-going memory output pulses without discrimination.

The array was built on a piece of phenolic board to fit a standard 19" rack; a photograph is shown in Figure 6.



F-1443

FIG. 6

THE 16 x 16 METALLIC CORE ARRAY

IV - ADDRESS SELECTOR, DRIVERS, SENSING AMPLIFIER, AND ASSOCIATED ELECTRONICS

Two types of electronic units were used in the operation of the 16 x 16 memory: special "breadboard" panels, and standard M. I. T. and Burroughs pulse test equipment.

The pieces of standard test equipment may be thought of as logical "black boxes" that trigger the "breadboard" units by supplying pulses and gates in certain time sequences and are discussed in Chapter V, BLOCK DIAGRAMS.

The "breadboard" panels, which include the vacuum-tube line drivers, the flip-flop address selectors and associated crystal matrices, and the sensing amplifier, actually perform the work of running the memory. Because these units are peculiar to an electronically driven magnetic-core memory, they are of interest and will be discussed.

A. ADDRESS SELECTION AND DISPLAY SCOPE

The problem of address selection in a 16 x 16 memory is that of current-pulsing one X line of 16 and one Y line of 16. The problem was solved by energizing the driving tubes in tandum and biasing off the non-selected ones.

In computer use, a binary address would be pulsed into the memory before a "read" or "write" order. The address would be stored in the X and Y flip-flop address selectors at least

until the subsequently ordered operations were completed. These flip-flops supply the biasing information by operating the X and Y crystal matrices, whose output lines are connected to the control grids of the line-driving tubes.

The address flip-flops used were the 6Y6 type (Fig. 7). Each of the two banks of 4 (X and Y) was designed to work directly into a 16-position crystal matrix (Fig. 8) which was actually part of the plate loads of the flip-flops. A crystal matrix input line presented 630 ohms to ground to the corresponding flip-flop plate circuit. The selected output bias line of each coordinate was at ground potential; all other matrix outputs were 30 volts below ground.

A simple systematic way of indexing addresses was used in testing the memory. The X and Y address flip-flops were connected to count. The X set counted one for every pulse of a clock, while the X end carry was used to trigger the count input of the Y flip-flop bank. Thus the cores in the array could be repeatedly "scanned" in the manner of a conventional television system. Decoders were attached to each flip-flop set, so that X and Y analog voltages were available which were proportional to the binary numbers stored in the X address flip-flops and Y address flip-flops respectively. These voltages were applied to the horizontal and vertical inputs of a display oscilloscope. Because the address flip-flops remain in a steady-state during the "read

A-52066

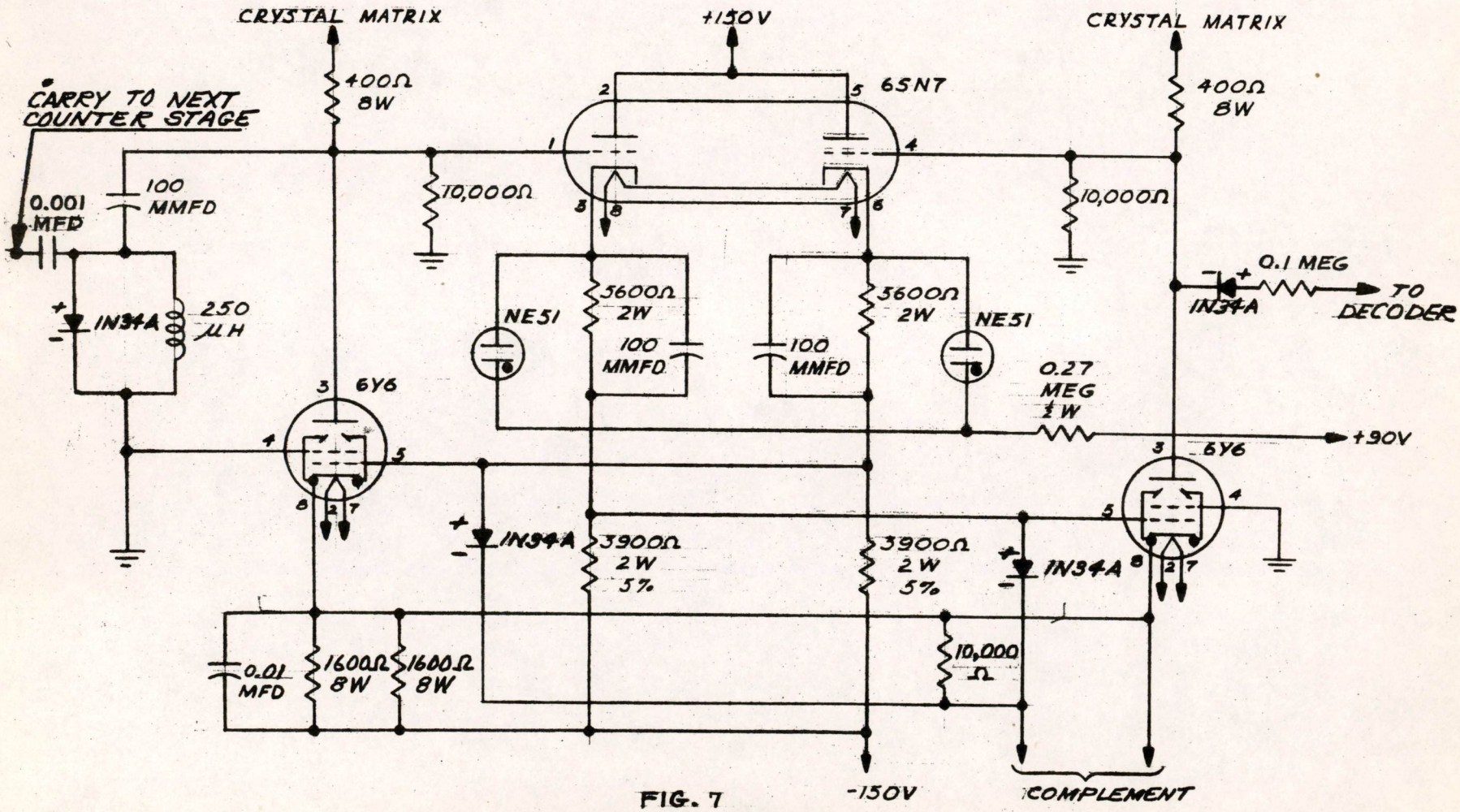
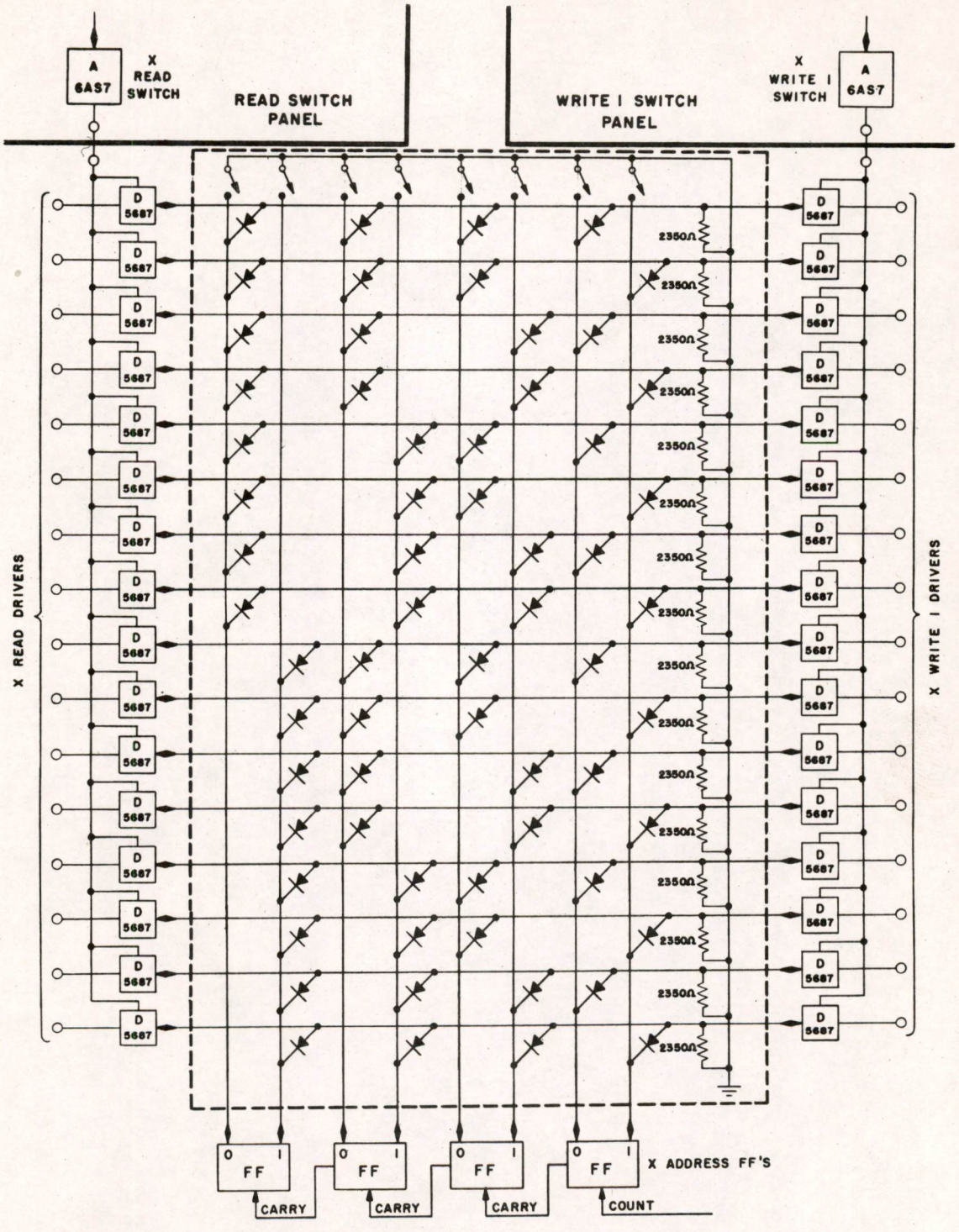


FIG. 7

CIRCUIT SCHEMATIC

ADDRESS SELECTION FLIP-FLOP



NOTES:
1. Y CRYSTAL MATRIX IDENTICAL
2. ALL DIODES ARE IN34'S

FIG. 8

FUNCTIONAL SCHEMATIC

METALLIC ARRAY X CRYSTAL MATRIX
AND X DRIVER PANEL

and "write 1" operations, time is available to itensify the display scope if a ONE is read out of a given core. Every address in the array has a corresponding position on the display scope so it is possible to display the information content of the memory as a set of blanks and bright spots as long as the array is scanned rapidly enough to prevent flicker.

B. DRIVERS

The drivers, or the current sources which energize the array, may be divided into two symmetric groups: those used to "write 0" or "read" and those used to "write 1". Each of these groups contains a set of 16 X drivers, 16 Y drivers, and one Z driver. The circuit used (Fig. 9) was designed by Kenneth Olsen.

Each set of drivers, the "X-read" drivers for example, consisted of a group of cathode followers (5687's) all having a common cathode resistor returned to -150 volts. The control grids were connected to the X-crystal matrix as mentioned above. Each plate was connected to its proper X-read driving line on the array, thence to +250 volts. The fact that all the cathodes were connected together allowed the cathode bias developed by the conducting tube to help the crystal matrix cut off the non-selected drivers. Normally, the cathodes' potential, held up by a 6AS7, allowed no current to flow in any of the driving lines, including the selected line. When it was desirable to apply a pulse of current, the proper 6AS7 was cut off and the selected driver then drew current. The 6AS7's associated electronics were mounted on separate

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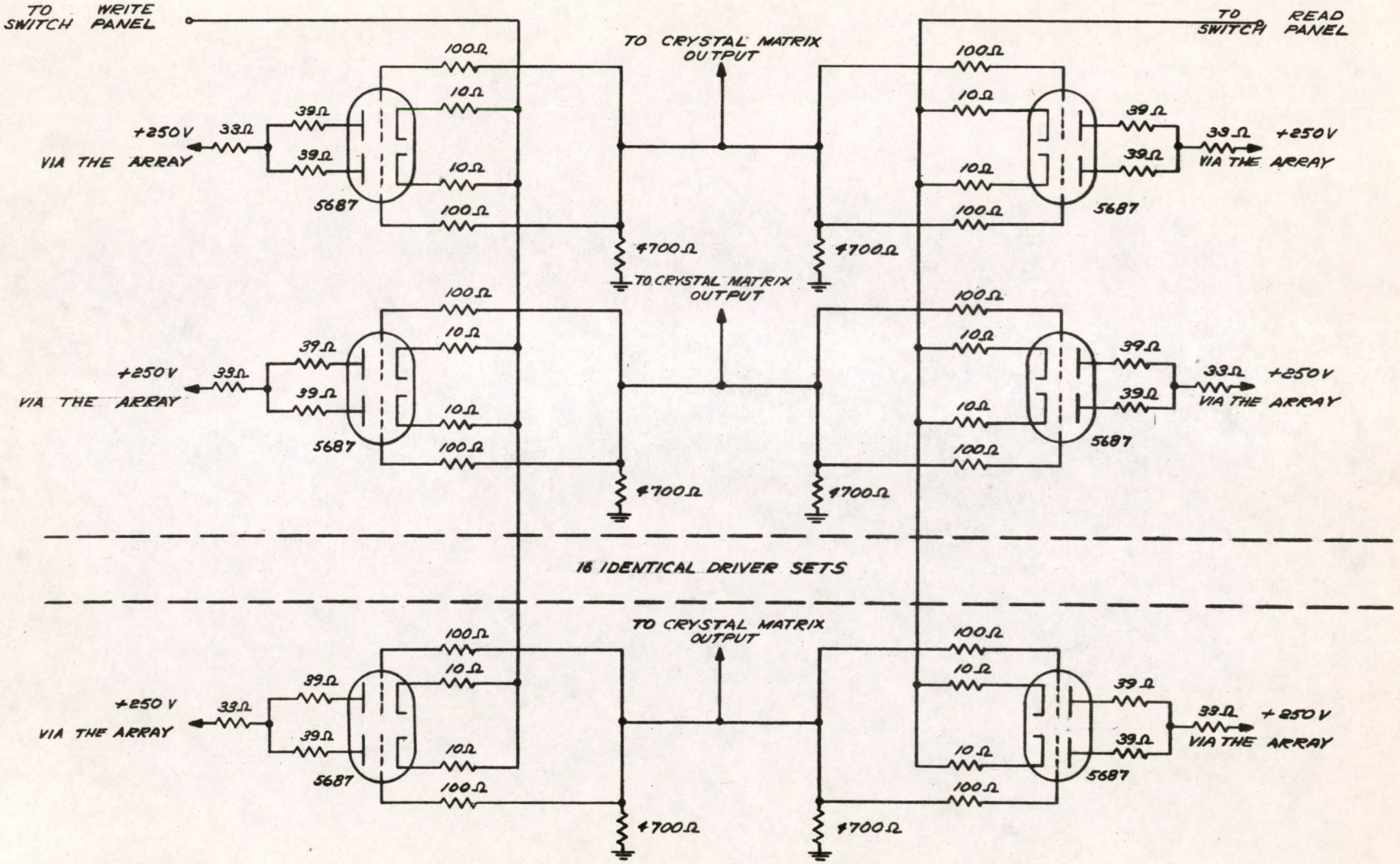

FIG. 9

X OR Y DRIVER PANEL FOR 16 x 16 METALLIC ARRAY

panels called "switch panels" (Fig. 10). These panels, "X, Y, Z read", and "X, Y, Z write 1" were responsible for switching on the selected drivers at the proper times. They, in turn, were controlled by the gate outputs of gate and delay units.

C. SENSING AMPLIFIER

The last "breadboard" panel to be considered is the sensing amplifier. This device was designed to produce 50-volt, positive-going gates from the positive and negative* input gates with amplitudes ranging from 5 to 35 millivolts induced in the sensing winding by the selected core. The output of this unit was to be used to control the suppressor grid of a gate tube. The input signals had rise and fall times that ranged from $\frac{1}{2}$ microsecond to 3 microseconds and lasted from 5 microseconds to 15 microseconds. The PRF could be random.

A schematic of the sensing amplifier is shown in Fig. 11. It consists of 3 stages of a-c-coupled linear amplification; a phase inverter, and two cathode followers providing output across a common cathode resistor.

The first 3 linear stages had a maximum gain well over 15,000. The remainder of the amplifier had a gain of about 0.8. The cathode followers in the output stage were biased almost to cutoff, and the grids were fed signals 180° apart from the preceding phase

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* Refer to Chapter II for a description of the sensing winding.

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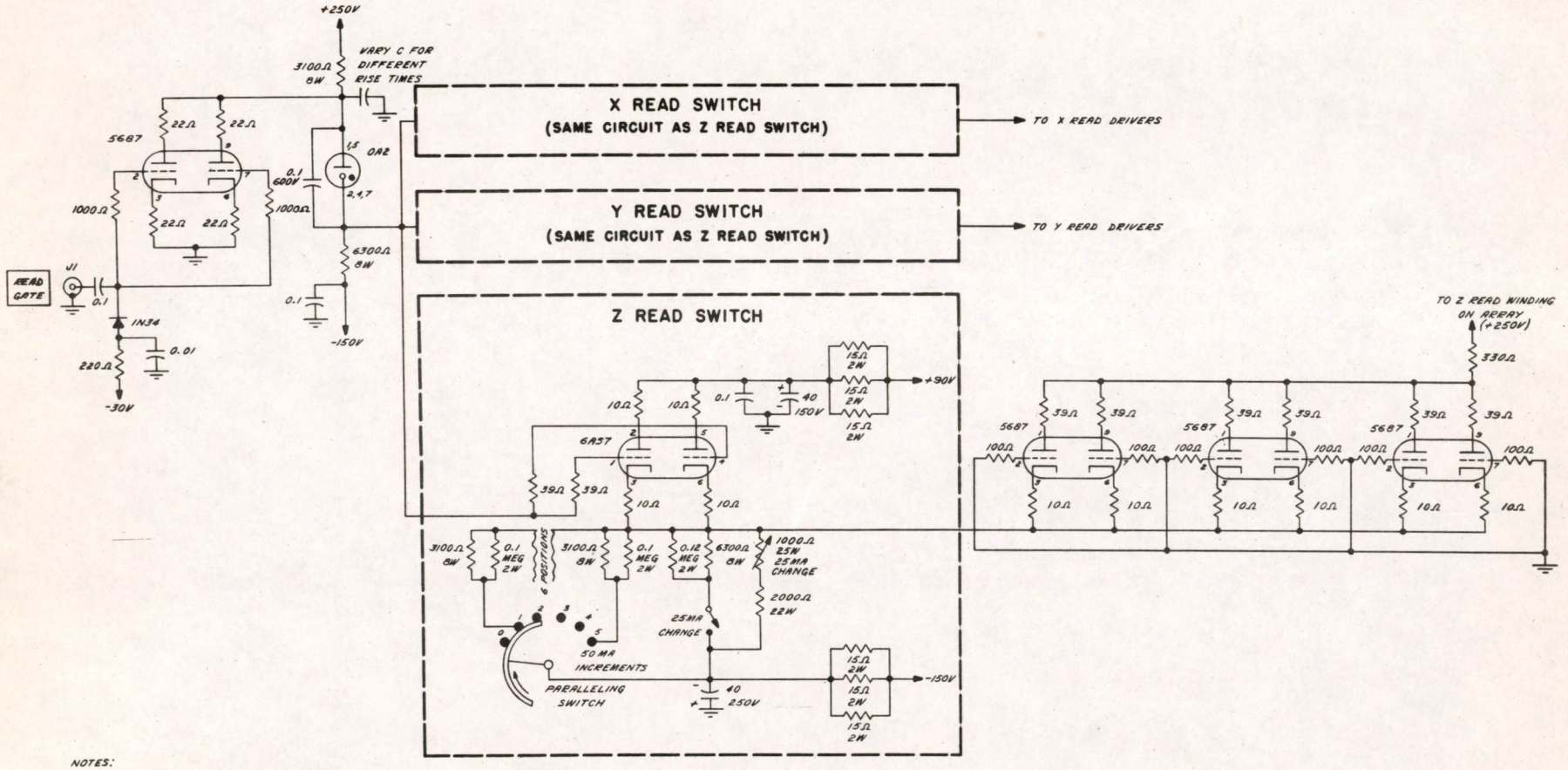


NOTES:
1. WRITE 1 SWITCH PANEL IS IDENTICAL.
2. ALL CAPACITORS ARE IN MICROFARADS.

FIG. 10

CIRCUIT SCHEMATIC,
METALLIC ARRAY READ SWITCH PANEL

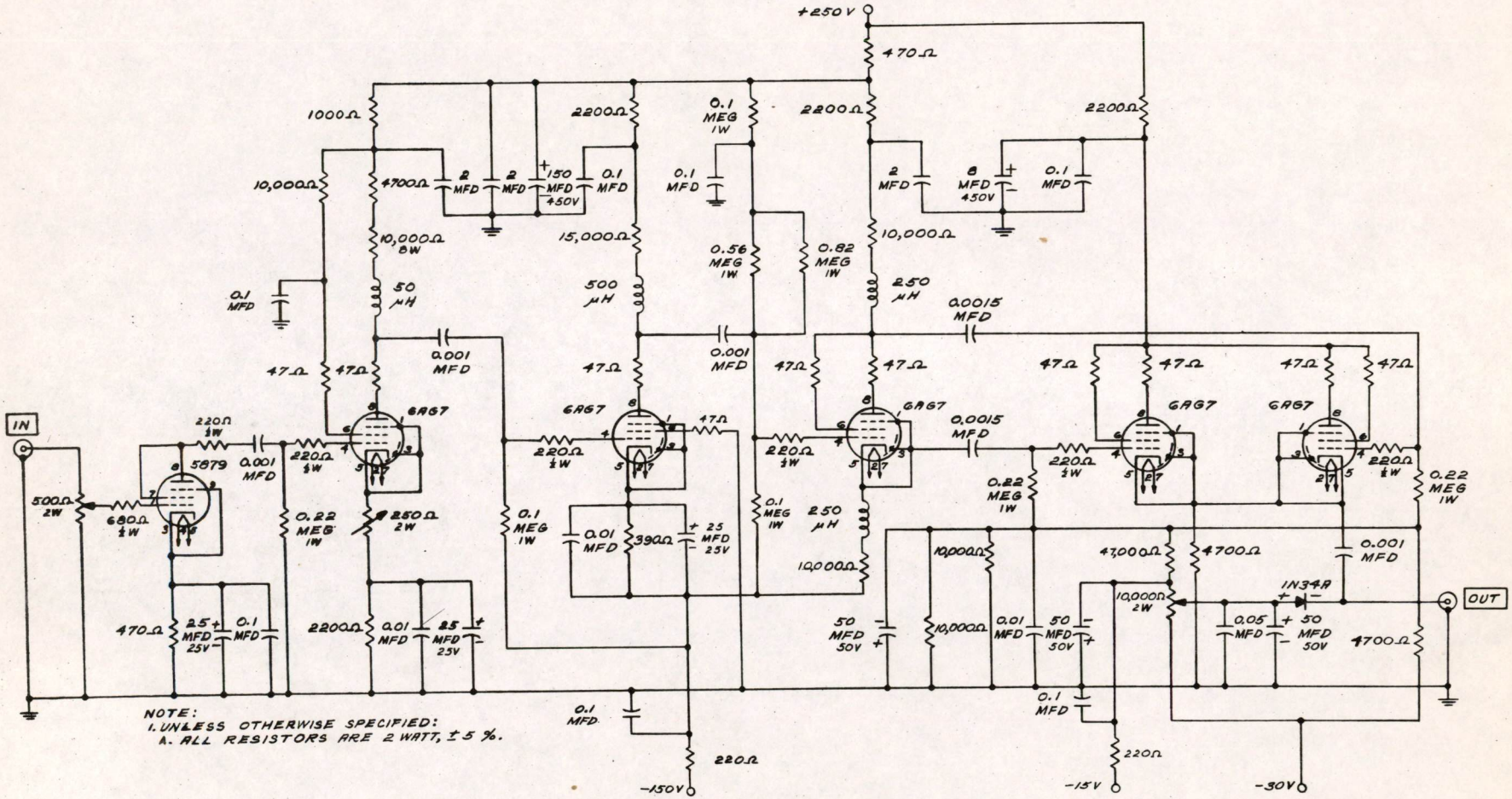


FIG. 11

CIRCUIT SCHEMATIC,

METALLIC ARRAY SENSING AMPLIFIER

inverter. When either grid went positive, the corresponding tube conducted as the other was cut off. Therefore, the output was always a low-impedance, positive-going signal proportional to the absolute value of the input.

The lower level of the output was clamped to a variable bias supply. Since discrimination between ZEROS and ONES was to be made on an amplitude basis in a gate tube, it was necessary to adjust this bias so that the ZEROS were below the threshold when the ONES were well above this threshold. The size of discrimination was determined by the incidence of the scanning pulse (0.1 microseconds) applied to the control grid of the gate tube. This function will be discussed further in Chapter V.

D. PHOTOGRAPHS OF BREADBOARDS

Fig. 12 shows the X-read and write 1 drivers and the array of cores. Fig. 13 shows the reverse side of the array and the X drivers. (Note coax cable leading from sensing winding to sensing amplifier.) Fig. 14 shows the entire system.

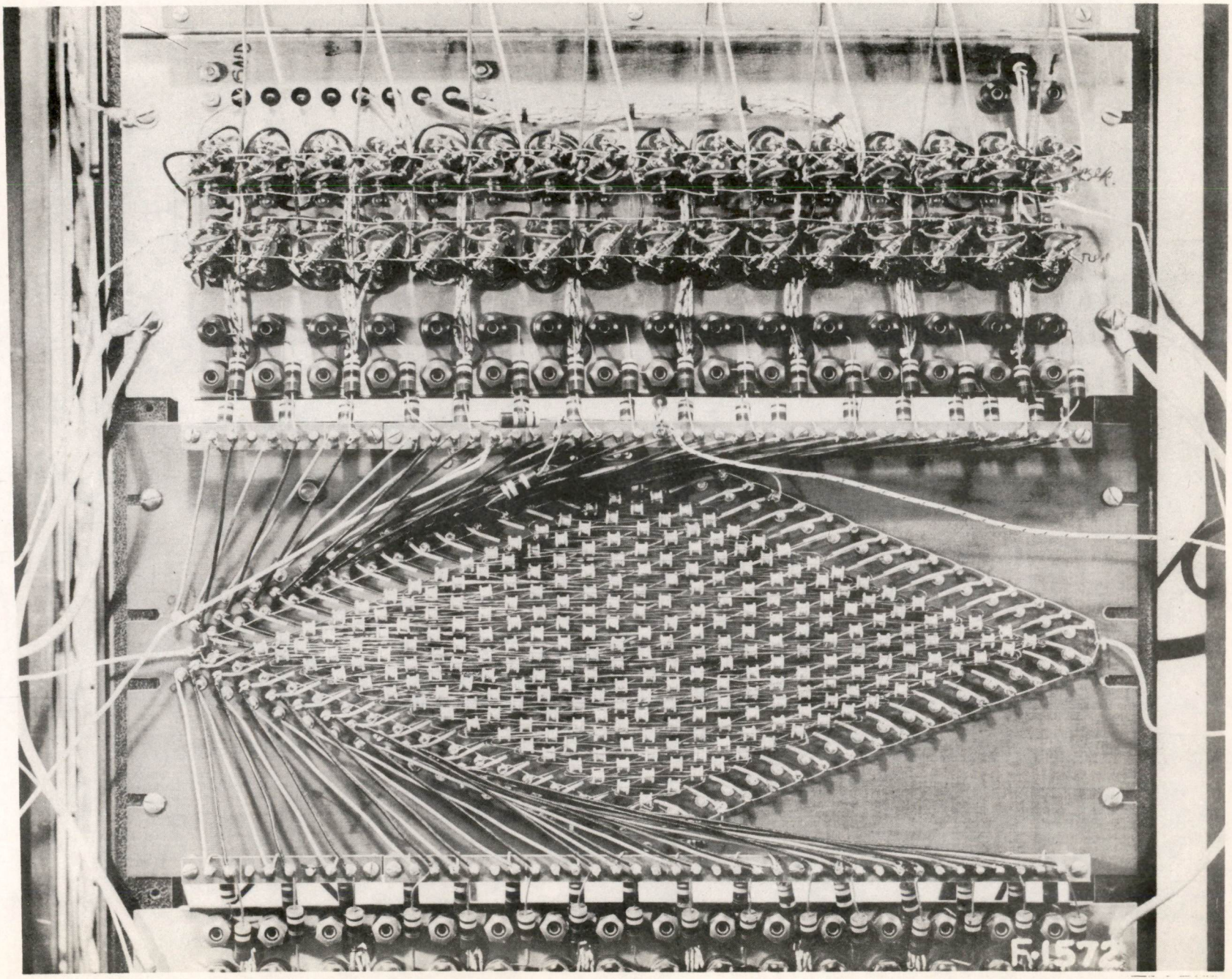


FIG. 12
16 x 16 METALLIC CORE ARRAY AND THE "X" READ AND WRITE 1 DRIVERS

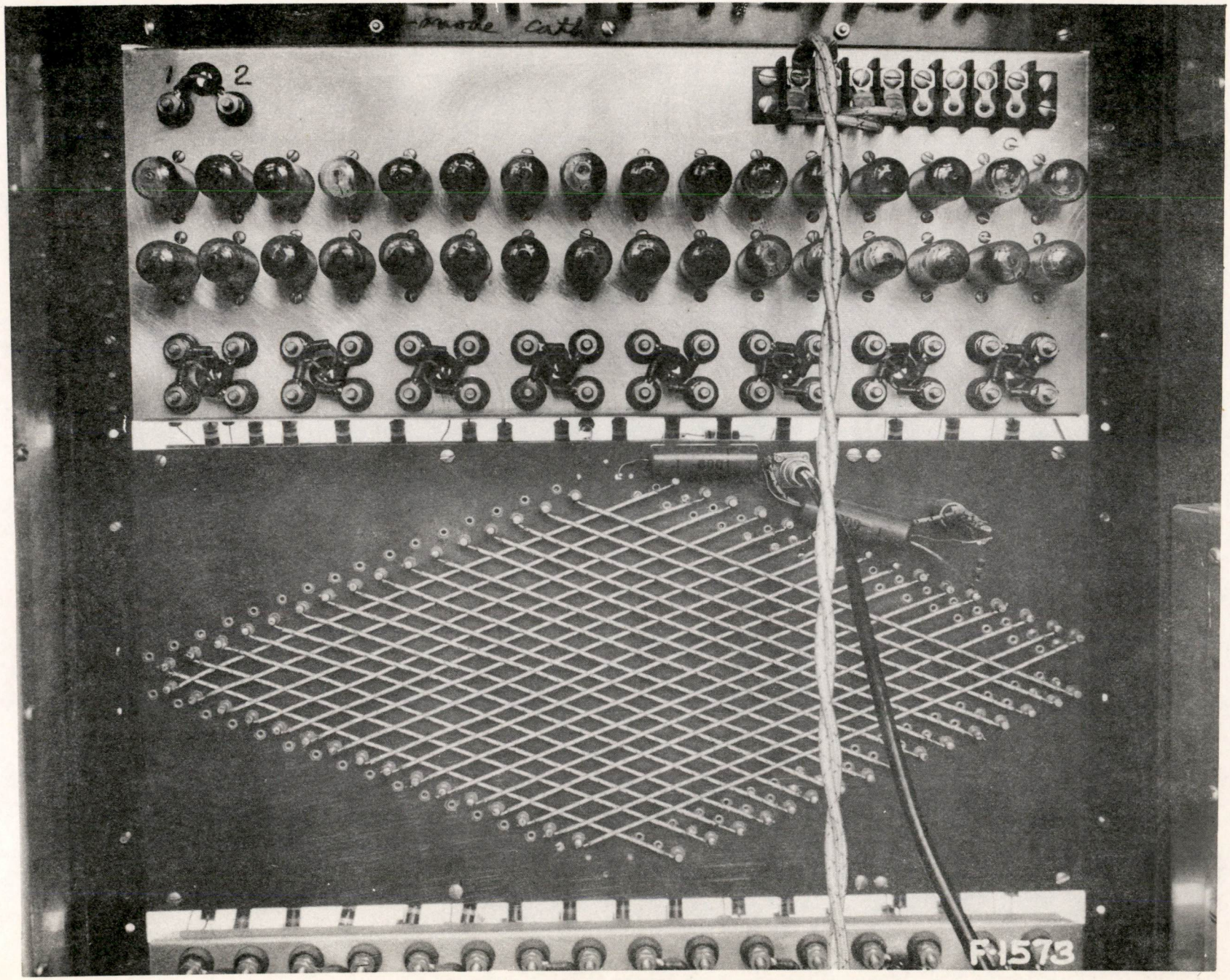


FIG. 13
REVERSE SIDE OF 16 x 16 METALLIC CORE ARRAY AND THE "X" DRIVERS

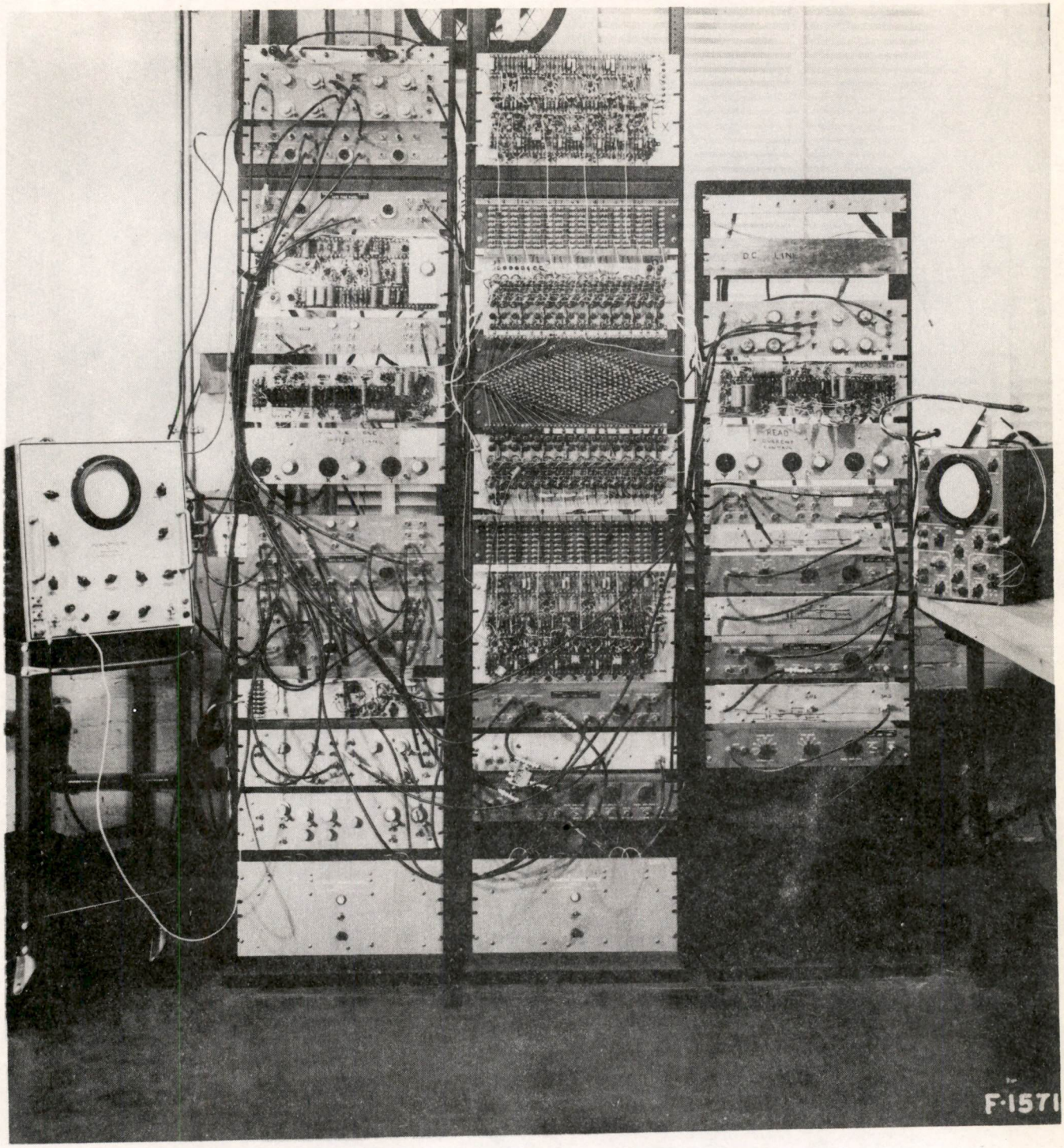
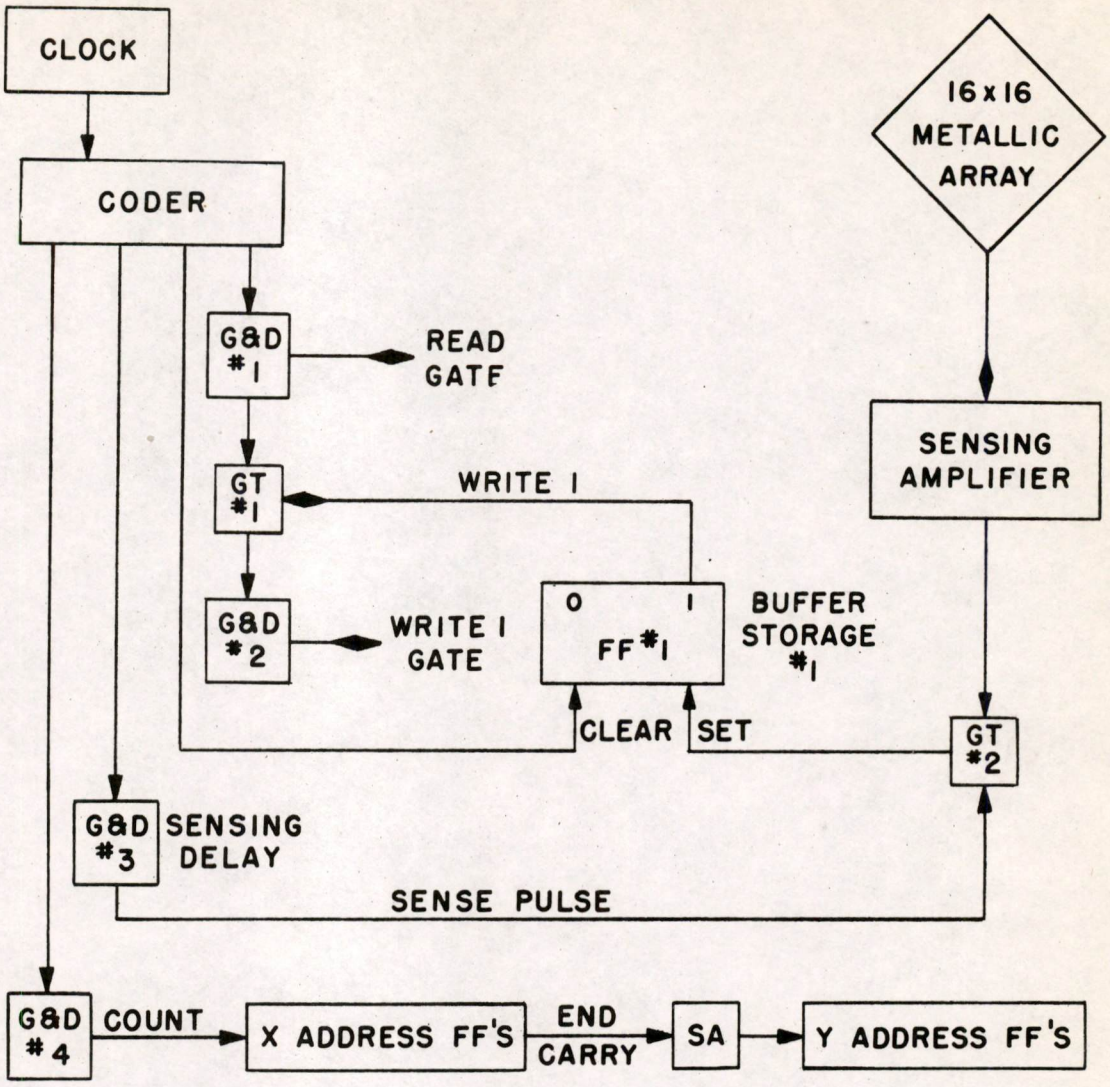


FIG. 14

16x16 METALLIC CORE MEMORY AND ASSOCIATED TEST EQUIPMENT

V - BLOCK DIAGRAMS

To simulate memory action, a logical system was set up to: approach a core and ask if it contains a "zero" or a "one". If it contains a "zero", leave it alone. If it contains a "one", re-write that "one" (it was destroyed by the asking). Go to the next core and repeat these operations. A block diagram of this system, utilizing standard test equipment units, may be seen in Fig. 15. The gate and delay units are adjusted to follow the timing diagram of Fig. 15. The clock pulse initiates the "read" gate by triggering gate and delay (G&D)#1 and clears a one-bit buffer storage flip-flop #1. During that gate, G&D #3 pulses the control grid of Gate Tube (GT) #2, the sensing gate tube. The buffer storage is either set or remains on "zero" after the sense pulse. This depends on whether the sensing amplifier has a large signal (ONE being read out of the selected core) or a small brief signal (ZERO being read out of the selected core, the selection being determined by the address that the X and Y flip-flops happen to be set on at the time). At the end of the read gate, G&D #1 pulses GT #1. A pulse is emitted by GT #1 to trigger G&D #2 (initiate the write 1 gate) only if buffer storage was on the "one" position (i.e., only if a ONE was read out of the selected core). Time is allowed for the complete read, re-write cycle before G&D #4 sends out a count pulse



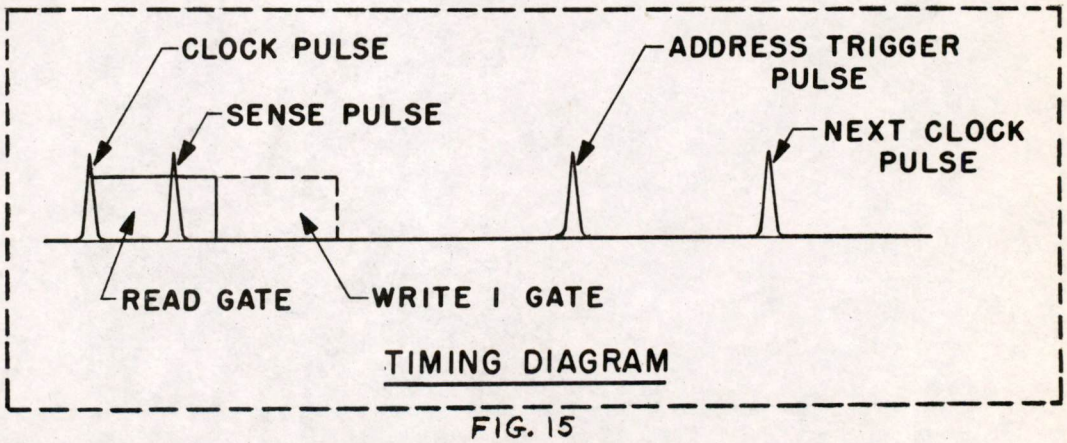


FIG. 15

BLOCK DIAGRAM

BASIC TEST SYSTEM OF MAGNETIC MEMORY

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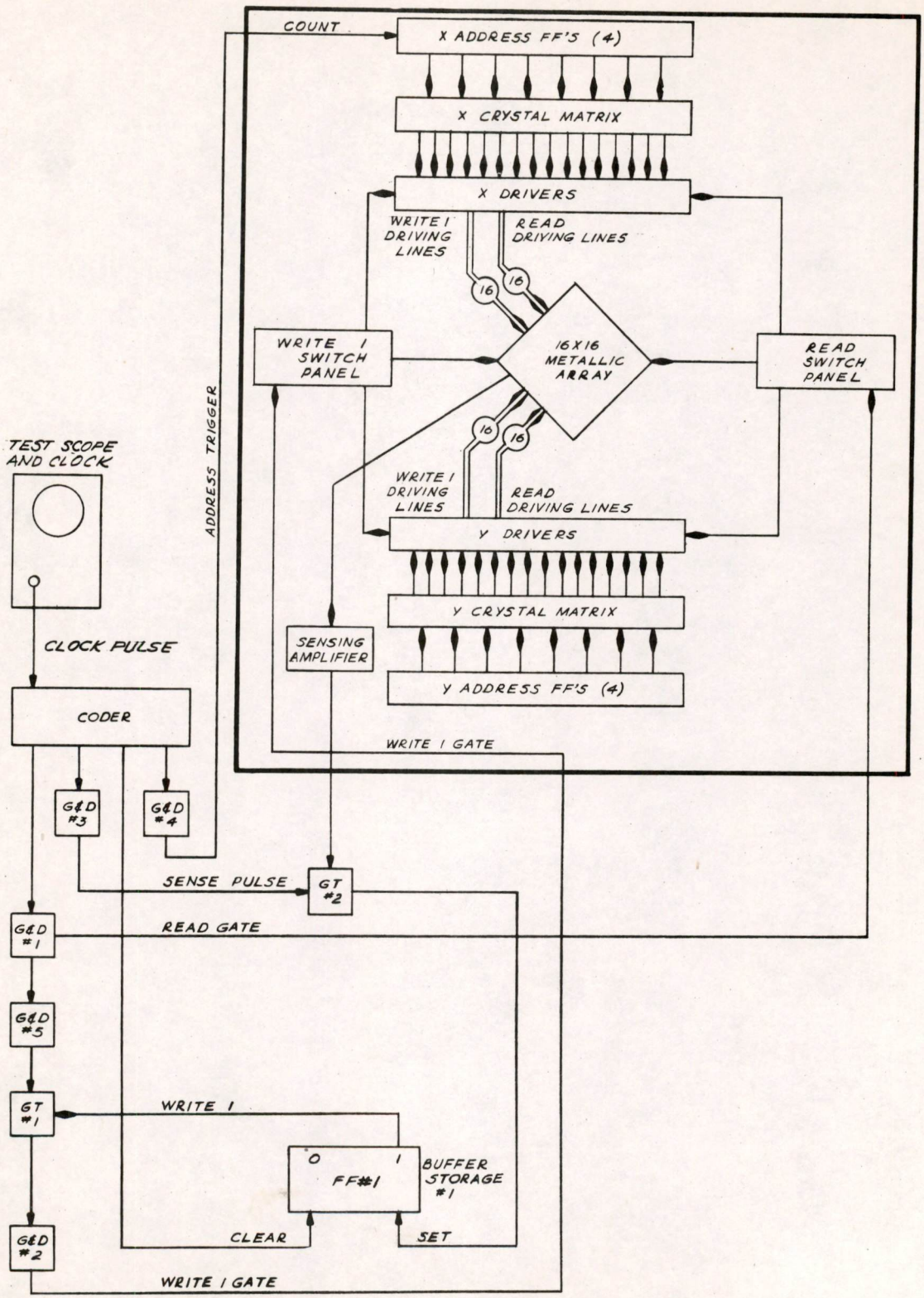

FIG. 16

BLOCK DIAGRAM, BASIC TEST SYSTEM OF MAGNETIC MEMORY SHOWING CONNECTIONS OF DRIVERS AND ADDRESS SELECTORS

(address trigger) to set the X and Y address flip-flops to the next address. This is done before the next clock pulse, so that the driver grid biasing potentials will be applied for the next reading, re-writing operation.

A. THE BASIC BLOCK DIAGRAM

The basic test system of the magnetic memory showing connections of drivers and address selectors may be seen in Fig. 16. Included is a gate and delay unit between G&D #1 and GT #1. This unit allows adjustment of the interval between the end of the read gate and the beginning of the write 1 gate. The master clock is a P5 synchroscope. Its pulse output must be standardized before it can be used to trigger the coder. This arrangement allows the array to be scanned at a 4-kilocycle PRF and avoids synchronization problems. When it was desired to run the array at a higher speed, a multivibrator pulse generator was used to trigger the coder.

The array was able to store random patterns of information (as presented on the display scope) that were stationary in time as scanning took place. The next section contains some special circuits that were added to the system in order to facilitate pattern writing and to allow more rigorous testing.

B. SPECIAL CIRCUITS

1. Light Gun

The light gun is a device for "shooting out" spots on the display scope. It simplifies the "writing" of arbitrary patterns by inserting "zeros" into a full array of "ones". Fig. 17 shows the light gun in operation.

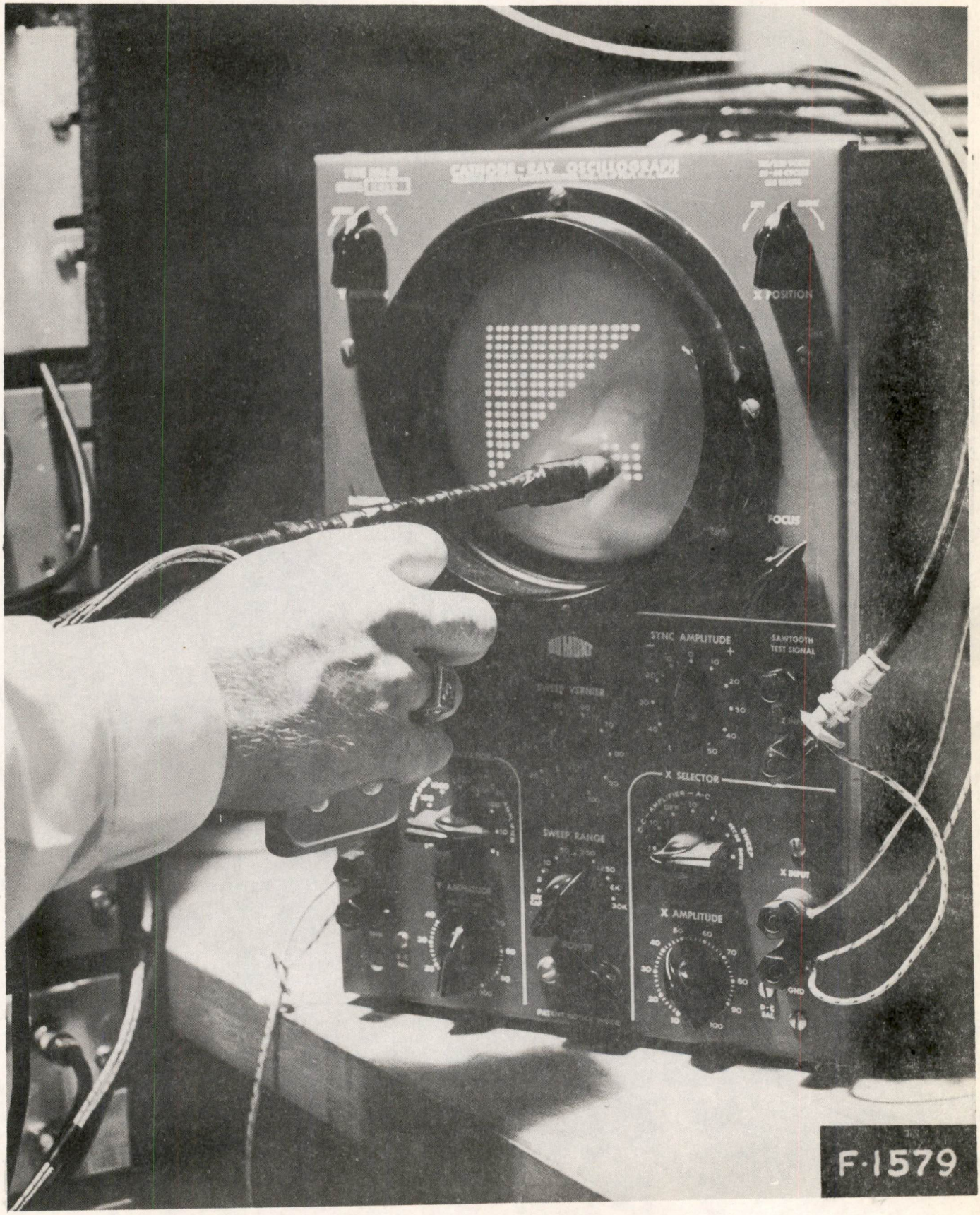

FIG. 17

WRITING PATTERNS WITH THE LIGHT GUN

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A-51163

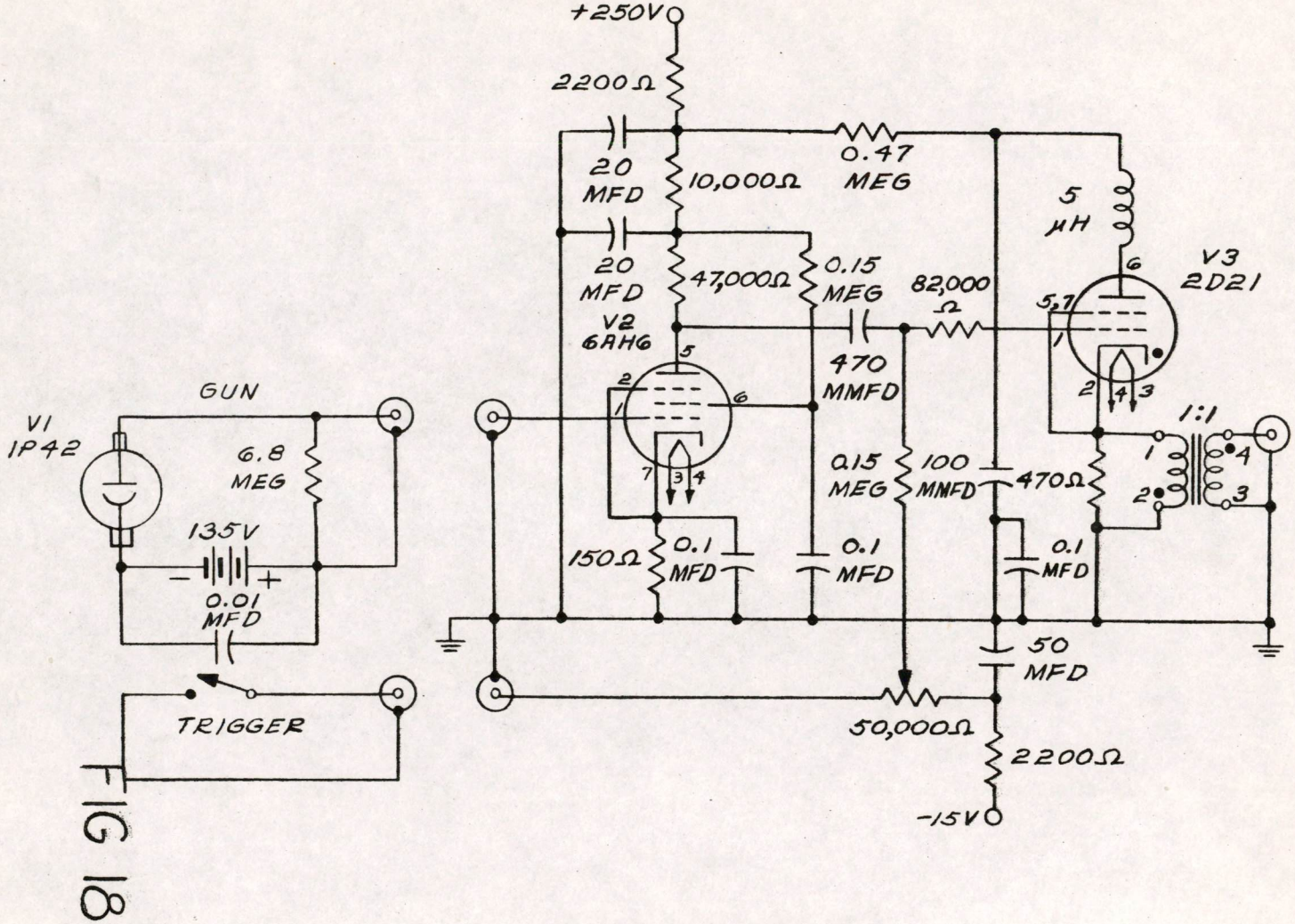
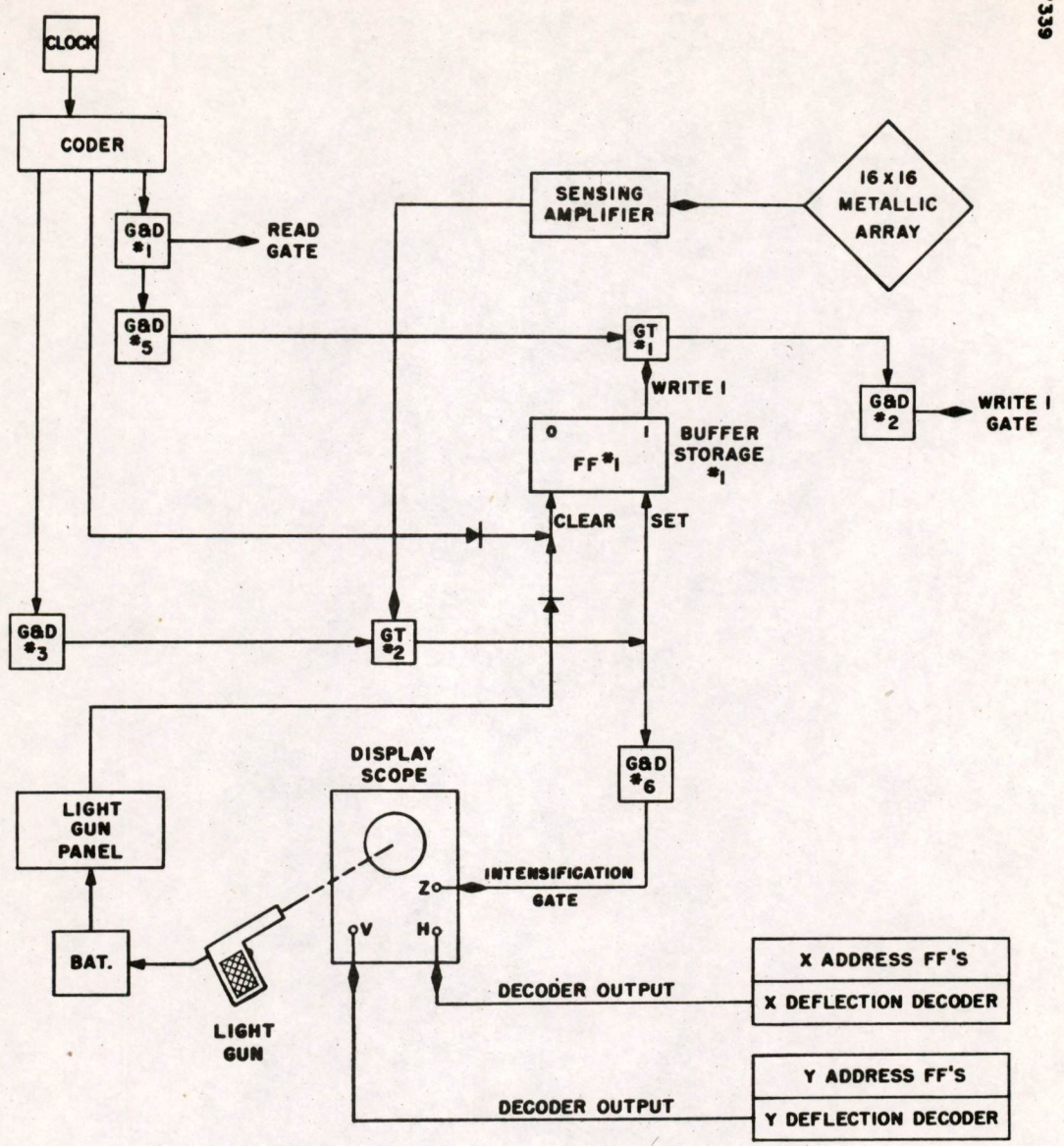


FIG 18

CIRCUIT SCHEMATIC,
LIGHT GUN PULSE GENERATOR



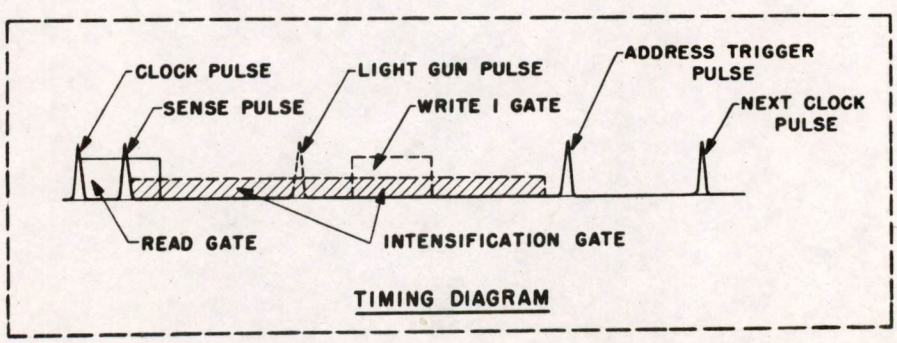


FIG. 19

BLOCK DIAGRAM

LIGHT GUN CONNECTIONS

The gun, a slender photocell built into a cable, is connected to a linear a-c amplifier which is able to actuate a gas tube pulse generator (Fig. 18). If the gun is placed over a bright spot on the display scope corresponding to a "one" stored in a core, it is able to give out a pulse about 15 microseconds after that spot is intensified. This pulse may clear buffer storage (FF #1, Figure 19) and prevent writing a "one" in the given core if the delay between the end of the read gate and beginning of write 1 gate (G&D #5, Fig. 19) is made greater than 15 microseconds. Once a "zero" is written in the core ("one" was not rewritten), the "zero" remains. That spot is no longer intensified.

Fig. 19 shows the block diagram of the light gun, the display scope, and associated equipment.

2. Moving Patterns

It is more difficult for a memory to hold a moving pattern than a fixed one. For the former, it is necessary that each core be able to remember both "zeros" and "ones". Addresses are scanned in the same manner, and the whole pattern is shifted one dot to the left for each raster scanned. This is done by writing into a core what was read out of the previously operated-upon core. Two buffer flip-flops are now necessary; one to hold the latest information read out, the other to hold the next-to-latest information (see Fig. 20).

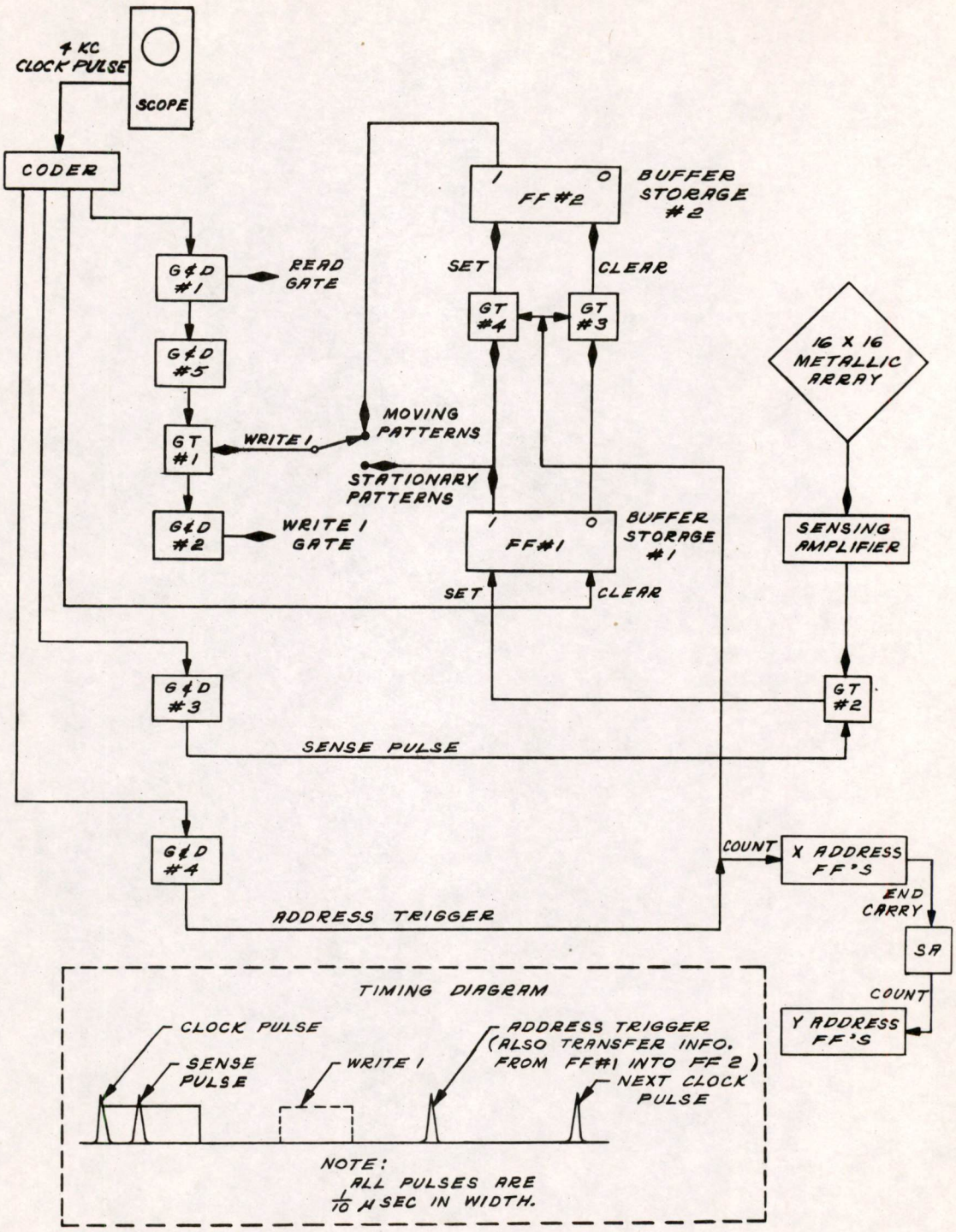


FIG. 20

BLOCK DIAGRAM,

MOVING PATTERNS SYSTEM

Flip-flop #1 is connected as before, and may be switched in to provide stationary patterns by connecting its "1" output to GT #1. FF #1 is cleared upon incidence of the clock pulse, remains cleared until the time of the sensing pulse, then is either in the "0" or "1" position (depending on whether the core contained a "0" or a "1") until cleared by the next clock pulse. During that time, the address FF's were set up on the next address. FF #2 is coupled to FF #1 through GT's #3 and #4. These gate tubes are pulsed at the time when the address FF's are triggered to the next address. This is done for convenience, to save a delay unit, and sets FF #2 to the number contained in FF #1. This number remains in FF #2 all the while the X and Y flip-flops are on the next address. Hence, if FF #2 is allowed to control GT #1, it becomes possible to write into a core the state of information of the core before. The display scope is connected as before, so that it always shows what was just read out. In the moving pattern mode, the pattern on the display scope "moves" because it is shifted one spot to the left each raster.

3. Skip Circuit

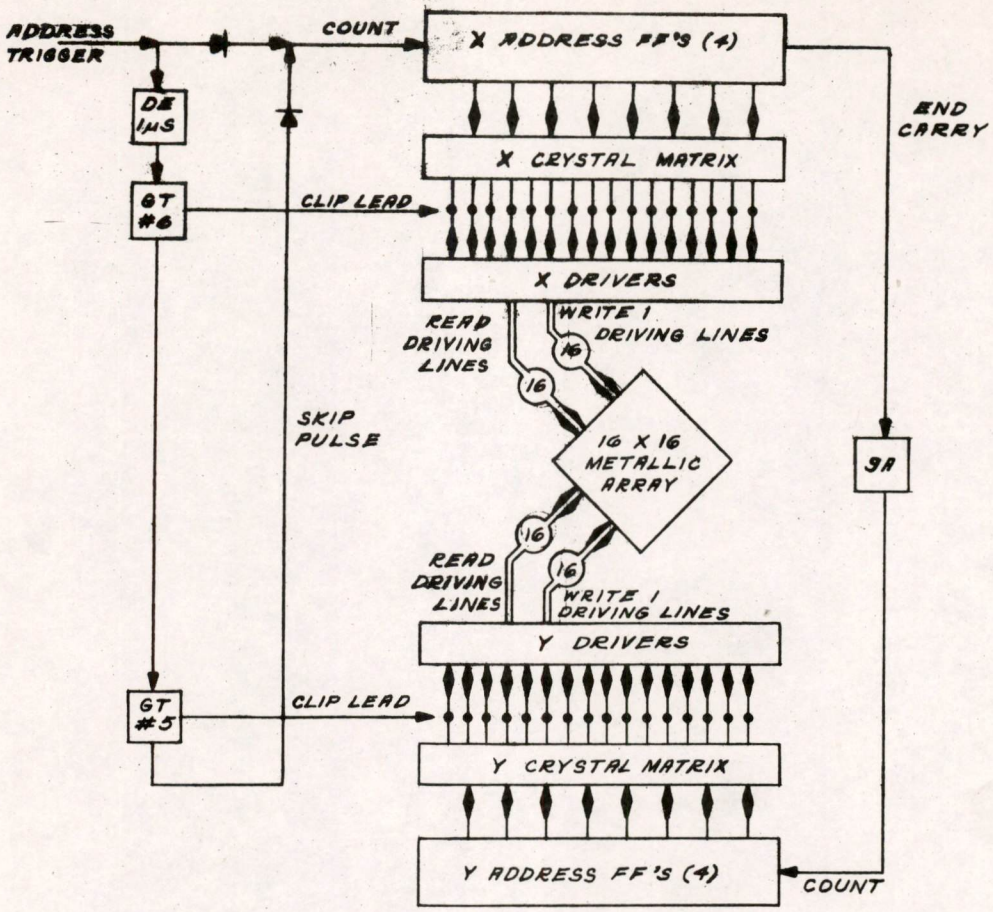
In a 16 x 16 array where the cores experience TV scanning, the maximum number of times that a given core may be disturbed before its information is refreshed is $2(n-1) = 30$, where n is the number of cores along a linear dimension. In order to allow an indefinite number of disturbances before a core is read, provision was made to skip this core during the normal scanning cycle. The array

could then be left running for hours, and the skipped core would be disturbed millions of times before its information was rewritten.

The circuit used is shown in Fig. 21. Clip leads connected to the suppressor grids of GT #5 and GT #6 are attached to outputs of the X and Y crystal matrices corresponding to the X and Y lines of the core to be skipped. A pulse delayed 1 microsecond relative to the regular address trigger will get through the gate tubes and trigger the address flip-flops to the next address only when the selected matrix outputs are those to which the clip leads are tied. The timing diagram (Fig. 21) shows how the double trigger is able to cause a skip and have the address flip-flops set up before the next read gate is begun.

4. Flip-Flop and Delay-Line Generators

Gate and delay units were used as the read and write-1 gate generators in the block diagrams shown thus far. They provided 40-volt gate inputs to the switch panels, allowed wide range adjustment of gate widths, and made operation simple. Their chief shortcoming, however, was their inability to maintain constancy of gate width during line transients. This was not serious until the array was run at high speed with a 3-to-1 selection ratio. Here, current gate widths were reduced to a minimum. Any jitter in the gate and delay units caused error. In order to allow high speed operation, it became necessary to use more reliable gate generators.



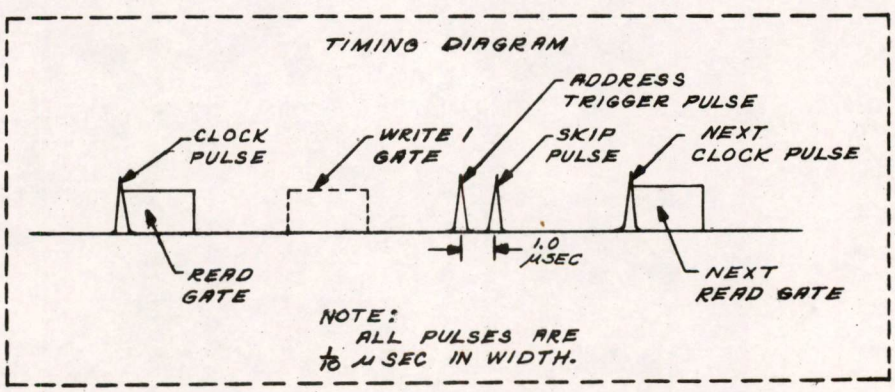


FIG 21

BLOCK DIAGRAM,
SKIP CIRCUIT CONNECTIONS

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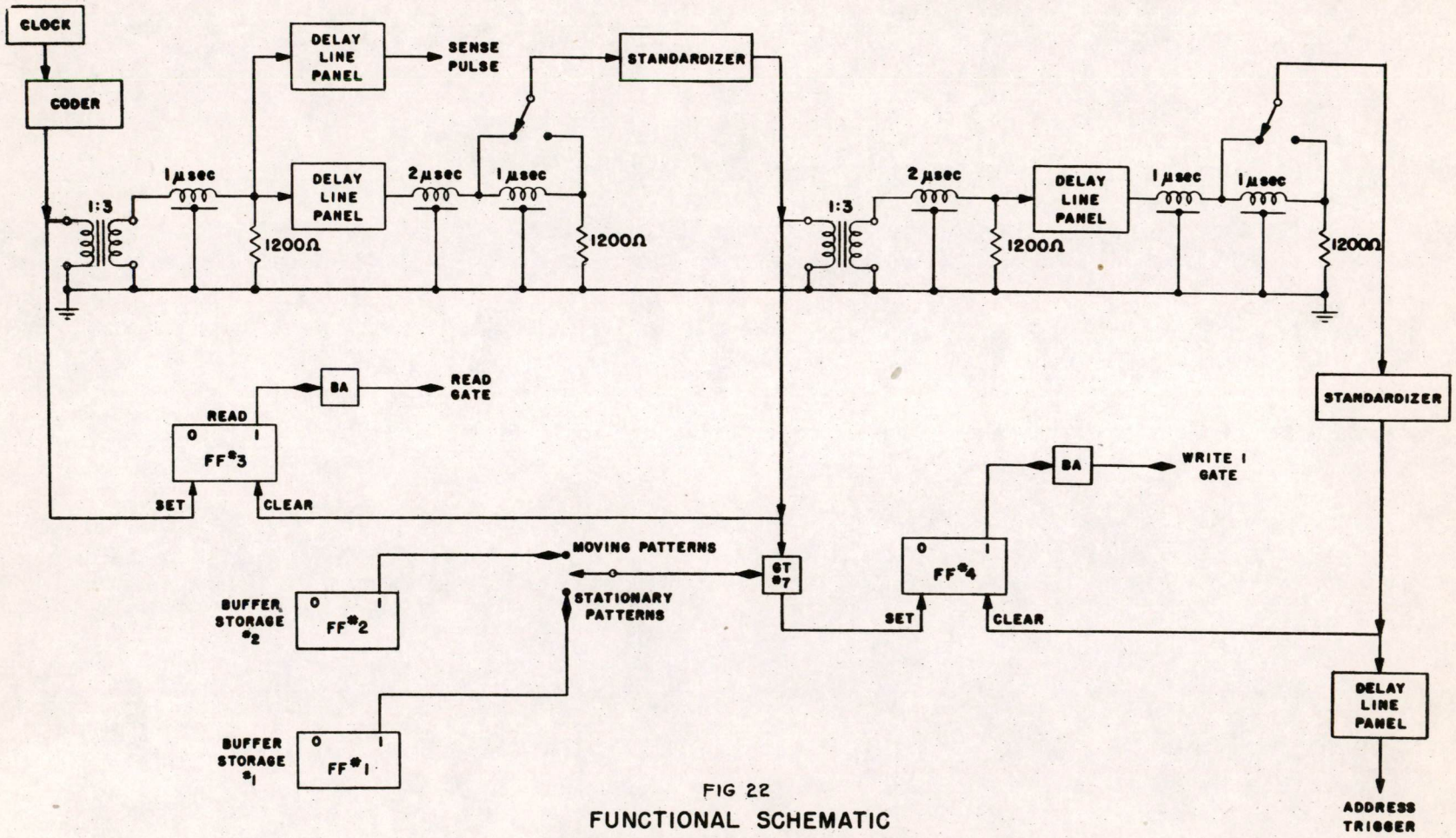


FIG 22

FUNCTIONAL SCHEMATIC

FLIP-FLOP AND DELAY LINE

TIME BASE AND GATE GENERATOR

A system was made of delay lines, flip-flops, buffer gate amplifiers, and pulse standardizers. A functional schematic of this system is shown in Fig. 22. When in use, it replaces the fundamental circuit of Fig. 15.

A time base is established by the delay lines and delay line panels. Each clock pulse yields a read gate, a sensing pulse, and an address trigger which is delayed long enough to allow for a write 1 if called for. GT #7 controls the initiation of the write 1 gate. The gate tube in turn is controlled by bugger storage FF #1 or FF #2 giving stationary or moving patterns.

3. Complete Block Diagram

Fig. 23 is a complete functional schematic of the metallic array as of July 1952. This diagram includes all of the information given in previously cited block diagrams.

D-37334

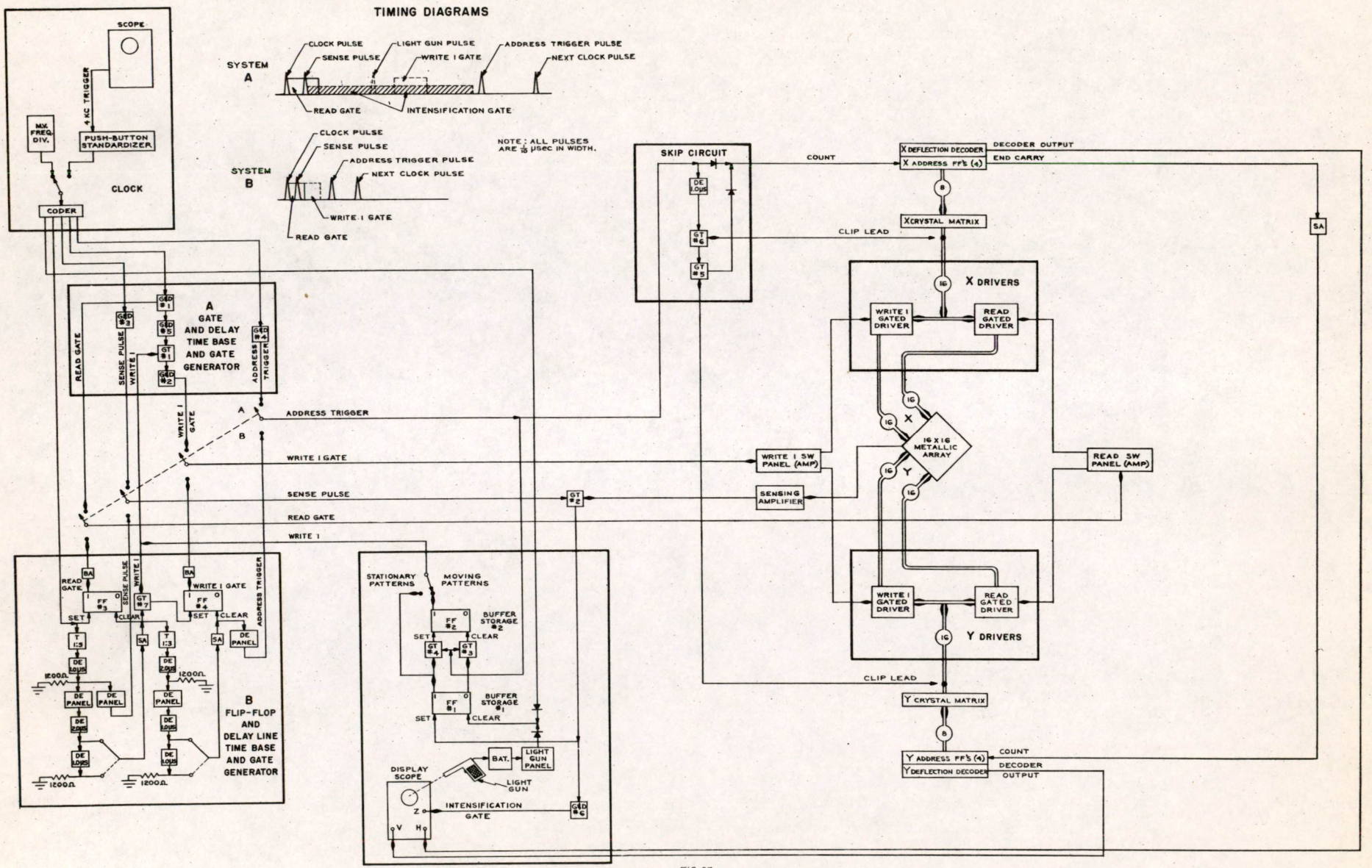


FIG 23

FUNCTIONAL SCHEMATIC, 16 X 16 METALLIC ARRAY

VI - OPERATING CHARACTERISTICS

The earliest testing was done by connecting one X and one Y driver to the array by clip leads. This allowed manual address selection, and was done before the flip-flop address selectors were set up.

When the X-address-selecting flip-flops and crystal matrix were de-bugged, a "16 x 1" array was run. Later, the X-address-selectors were able to be used, and full 16 x 16 operation took place.

The magnitude of driving currents used for the 1 x 1 operation was too large for coincident-current selection. 16 x 1 operation was possible only when these were reduced to the extent that non-selecting current disturbances were tolerable. When 16 x 16 operation was desired, it was necessary to increase the negative bias and the swing of the sensing panel output. Deviations in the outputs of the 256 cores were greater than was the case with only 16 cores being sensed, and this required a more careful adjustment of the sensing panel.

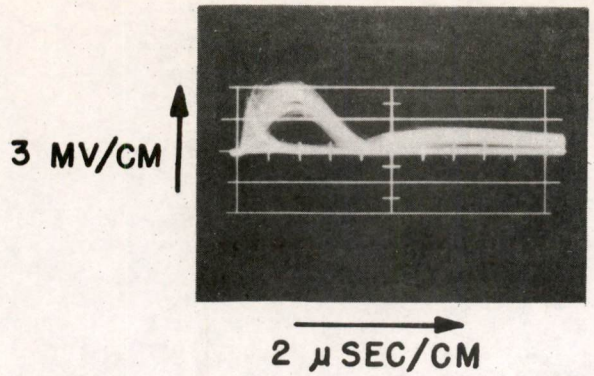
The preceding work was done with the block diagram of Fig. 16, using a 2-to-1 selection ratio. From there on, more logical equipment was added until the system represented in Fig. 23 was built up and operated. The next section contains some quantitative and qualitative operating characteristics that were derived during the first six months' run.

A. DRIVING-CURRENT WAVEFORMS

It is possible to look at waveforms of driving currents in the X and Y memory lines by observing the voltages developed across the 33Ω damping resistors in series with each line. The current drivers are nearly ideal current sources (Figs. 9 and 10), so that the back voltages of the memory lines (approximately ½volt peak on X and Y, 10 volts peak on Z) have negligible effects upon the current waveforms.

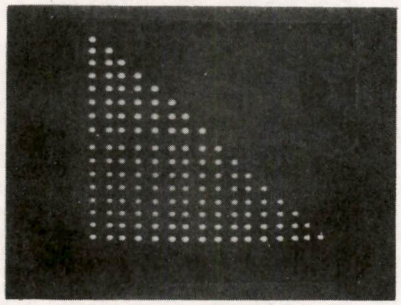
B. OUTPUT WAVEFORMS OF SENSING AMPLIFIER

Figure 24-1 is a composite of 256 traces showing the output of the sensing panel when the array is holding the pattern of Fig. 24-2 and is being cycled at a PRF of 4 kilocycles. The selection ratio is 2-to-1, with I_m = 280 milliamperes. Fig. 24-3 is the voltage at the input in the phase inverter of the sensing amplifier. This shows the positive and negative going signals induced in the sensing winding after going through linear amplification. Notice the variance in the amplitude of the ONES and ZEROS. Fig. 24-1 should be compared with Fig. 24-3, keeping in mind the sensing amplifier schematic, Fig. 11. Fig. 25 shows the output of a single type-B core containing a "zero" and a "one" (composite). The notch on the ONE output shows the incidence in time of the sensing pulse applied to the gate tube (GT #2) of Fig. 16 or Fig. 23. It is caused by suppressor current loading down the output of the sensing panel.



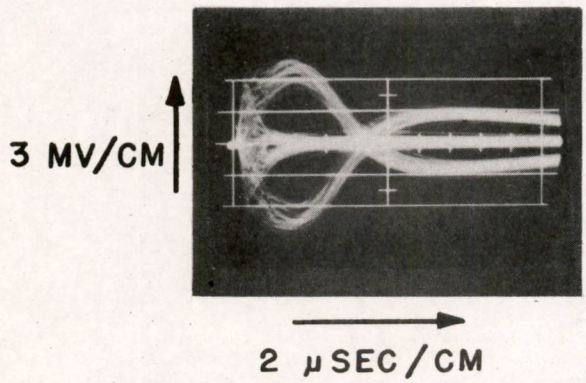
OUTPUT OF SENSING AMPLIFIER.
256 TRACES SHOW
ONES AND ZEROS

FIG. 24-1



DIAGONAL PATTERN
OF "ones" AND "zeros"
STORED IN MEMORY

FIG. 24-2



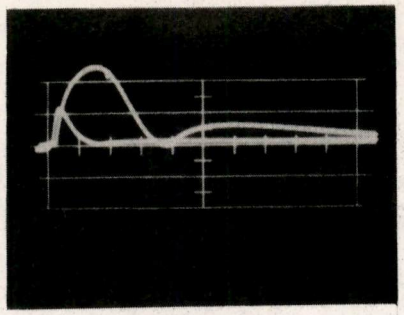
INPUT TO PHASE INVERTER
OF SENSING AMPLIFIER.
THE OVERSHOOT IS DUE
TO A-C COUPLING IN
THAT AMPLIFIER.

FIG. 24-3

ARRAY WAS RUN AT A PRF OF 4 KC
WITH 2:1 SELECTION.
$I_x = I_y = 140$ MA
OPTIMUM SENSING TIME = 4.33 μSEC

FIG. 24

SENSING AMPLIFIER WAVEFORMS
WHEN ARRAY STORES A DIAGONAL PATTERN



255 CORES HOLDING "ones"
ADDRESS FLIP-FLOPS STOPPED AT
THE ADDRESS X = 8, Y = 10 } CORE # 290 TYPE B
SHOWN IS A ONE AND A ZERO
OF THIS CORE.

ARRAY WAS RUN AT A PRF OF 4 KC
WITH 2:1 SELECTION.
$I_x = I_y = 140$ MA
OPTIMUM SENSING TIME = 4.33 μSEC

FIG. 25

ONE AND ZERO OUTPUTS
OF SENSING AMPLIFIER DURING READ-OUT
OF A TYPE B CORE

A-52353

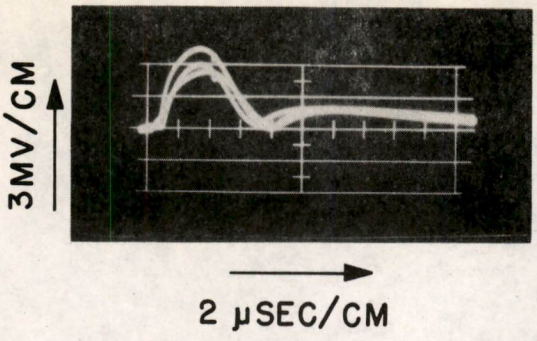
1. Variations in Sensed Outputs

The ONE outputs of the cores in the array were not identical in magnitude; neither were the ZERO outputs. The most significant reasons for these differences are:

a. Variations in magnetic properties of the individual cores are inherent in manufacture and are limited only by selection based on single core pulse test characteristics. Fig. 26-1 shows the ONE sensed output, while Fig. 26-2 shows the ZERO sensed output of typical types B, B-, and BC, since the rest of the array holds "ones".

b. Changes in I_m cause variation, because the output voltage varies almost linearly with I_m in the normal ranges of operation. This is not troublesome if driving current magnitudes are constant. These variations, which are applied to all the sensed cores, affect current margins. A sequence of photographs showing these variations for a 2-to-1 current-selection ratio for various values of I_m is shown in Fig. 27-1. Fig. 27-2 shows a similar set for 3-to-1 current selection.

c. Variations are sometimes caused by geometric irregularities of the array. The array was designed to minimize the mutual inductance between the sensing winding and all of the driving windings. If those windings were perfectly symmetric, the mutual inductance would be zero. Actually, this was not possible, so that voltages induced by the cores are superposed with those due to mutual coupling



ONES

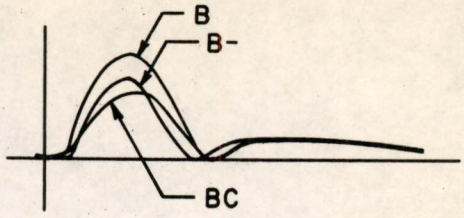
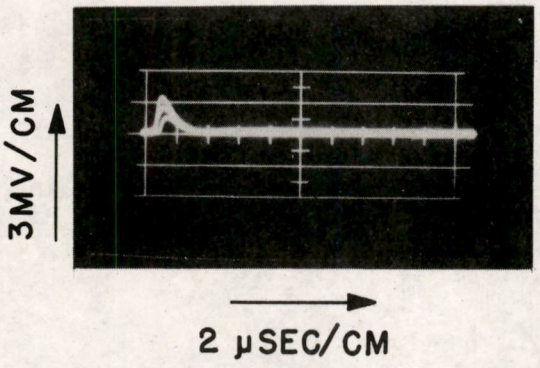


FIG. 26-1



ZEROS

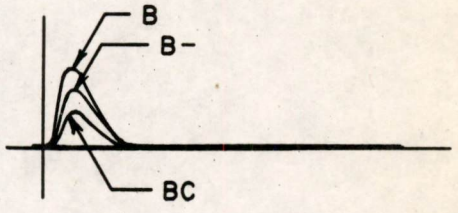


FIG. 26-2

ARRAY WAS RUN AT PRF OF 4KC WITH 2:1 SELECTION.
$I_x = I_y = 140$ MA.
OPTIMUM SENSING TIME = 4.33 μSEC.
TIME BASE = 2 μSEC/CM.
ARRAY HOLDING ALL "ones" EXCEPT CORE SPECIFIED.

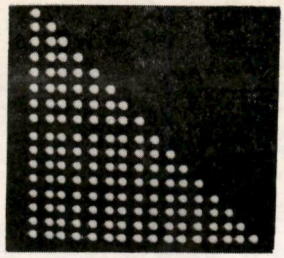
TYPE B: CORE #290, X=8; Y=10

TYPE B-: CORE #259, X=8; Y=11

TYPE BC: CORE #315, X=8; Y=9

FIG. 26

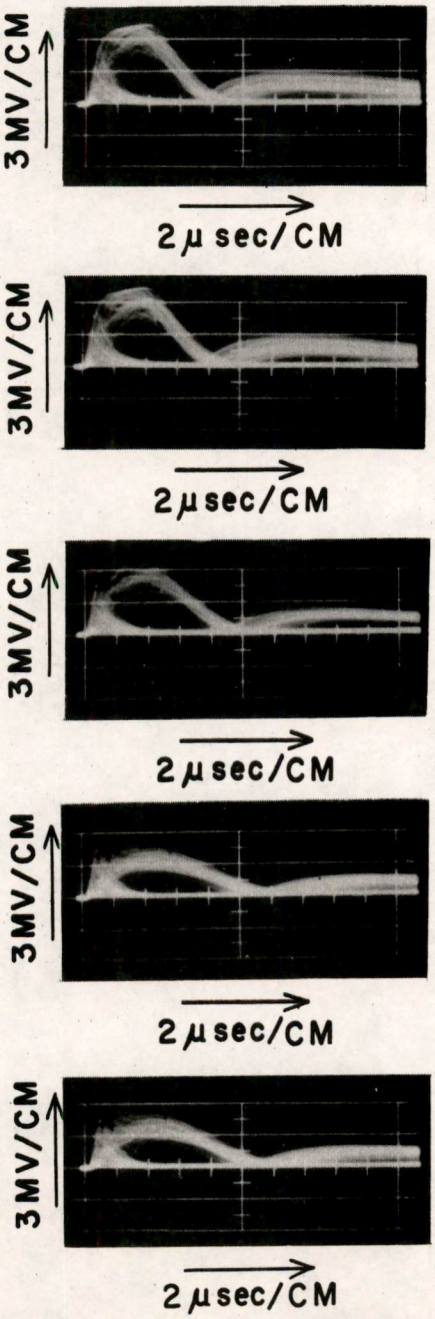
DIFFERENCES IN SENSED ONES AND ZEROS OF CORE TYPES B, B-, BC



MEMORY PATTERN WAS A DIAGONAL PATTERN OF "ones" AND "zeros"

DRIVER RISE TIME $\frac{1}{2}$ μsec

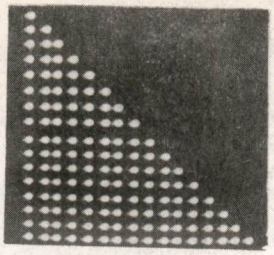
X AND Y CURRENT	OPTIMUM SENSING TIME
150 MA	4.33 μsec
140 MA	4.66 μsec
130 MA	5.00 μsec
125 MA	5.33 μsec
115 MA	5.50 μsec



OPERATING 2:1 CURRENT SELECTION

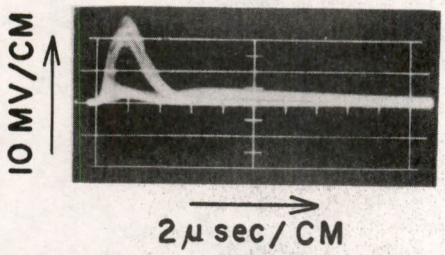
FIG. 27-1 SENSING AMPLIFIER OUTPUT WAVEFORMS FOR VARIOUS VALUES OF I_m

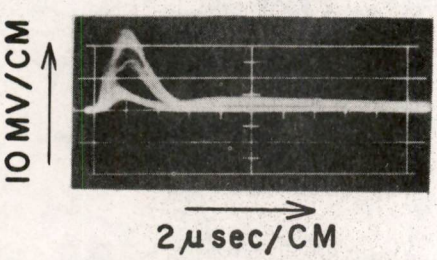
A-52367

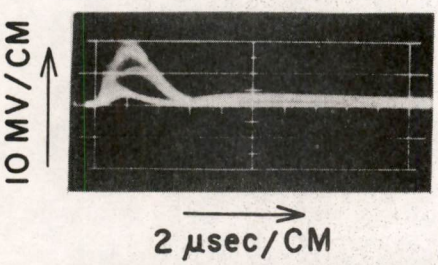


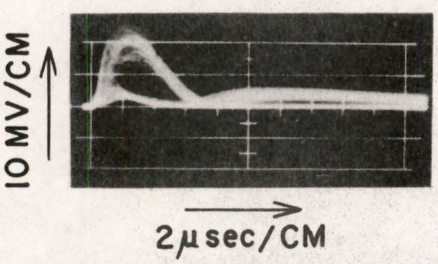
MEMORY PATTERN WAS A DIAGONAL PATTERN OF "ones" AND "zeros"

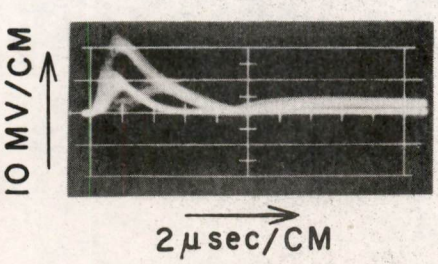
DRIVER RISE TIME $\frac{1}{2}$ μ sec











CURRENTS X=Y MA	CURRENTS Z MA	OPTIMUM SENSING TIME
275	137.5	3 μsec
250	125	3.2 μsec
225	112.5	3.5 μsec
200	100	4 μsec
175	87.5	4.33 μsec

OPERATING 3:1 CURRENT SELECTION

FIG.27-2 SENSING AMPLIFIER OUTPUT WAVEFORMS FOR VARIOUS VALUES OF I_m

across the sensing winding. Another factor is capacitive coupling between the driving lines and the sensing winding, which cannot be completely eliminated no matter how the windings are placed. With a current driver rise time of 0.2 microseconds, the voltage induced in the sensing winding by the Z-read winding is about half the size and shape of a typical ZERO when the Z current is 150 milliamperes. Under similar conditions, the Z-write 1 current would induce almost twice as much noise. Noise due to X and Y read and write 1 currents was found to be about 10% of the size of that due to the Z-write 1 current.

d. Variations may be due to the particular "zero" and "one" constellations stored in the memory. Not always does a given core (having fixed magnetic properties and geometrical position) produce the same size ZERO and ONE. The number and sequence of disturbances per raster depend upon the information pattern. The shape of a core's readout signals depends upon its history of disturbances from the time when the information was freshly written. More significant noise contributors are the non-selected readout-pulses of cores which may contain "zeros" (NS_0) or "ones" (NS_1). These cores have their X or Y line common with the selected core and are disturbed during reading or writing 1. The sensing winding is wound to cause all of these pulses to cancel, except for 2. This would be so if all cores yielded the same size non-selected pulses. They do not, however, and in addition, a given core will produce a larger non-selected pulse if it contains a "one" than if it contains a "zero".

The non-selected pulses have about the same shape and size as ZEROS. This is fortunate, because they decay away to 10% of peak before the sensing time occurs. Stored patterns were designed to emphasize the effects of differences in non-selected outputs upon sensed waveforms, and it was found that these differences seriously impair ONE-ZERO discrimination in a 256-bit memory with 3-to-1 selection (Z used for driving), and make operation almost marginal with 2-to-1 selection. The effect clearly places a limitation on the number of cores that may be sensed with the type of sensing winding used. Even when the induced noise is over before the sensing time, the transient has an effect upon an a-c-coupled sensing amplifier which may be troublesome in large arrays.

Fig. 29 shows ZEROS and ONES of a type-B core, the selected core where the three display scope patterns of Fig. 28 were stored to give either no noise or the maximum possible values of noise of both senses. The difference between the largest ONE and the ONE without noise (shown in Fig. 29-1) is approximately the same as that between the ONE without noise and the smallest ONE. This difference is equal to 14 times the difference between the non-selected output of a core containing a "one" (NS_1) and a "zero" (NS_0). Fig. 29-2 exhibits the same differences with the selected core containing a "zero" instead of a "one" as in Fig. 29-1. Fig. 30-1 shows the ONE output of the sensing amplifier while the patterns of Fig. 28 were stored with a 2-microsecond rise time instead of a $\frac{1}{2}$-microsecond rise time.

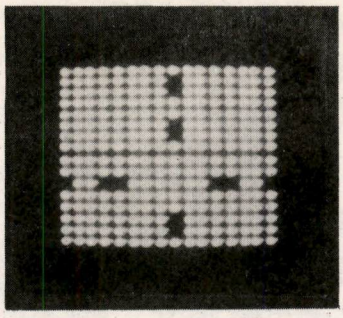


FIG. 28-1

PATTERN TYPE 1

ASSUMING LIKE CORES, THIS PATTERN DOES NOT INTRODUCE NON-SELECTED NOISE IN SENSING WINDING WHEN SELECTED "X" AND "Y" LINES ARE PULSED.

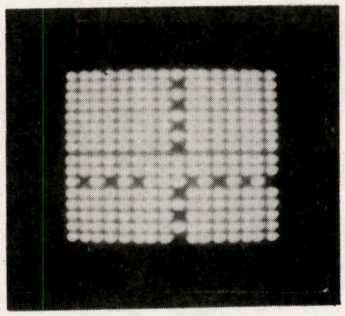


FIG. 28-2

PATTERN TYPE 2

INTRODUCES NOISE TO MAKE SELECTED CORE "one" OUTPUT LARGER.

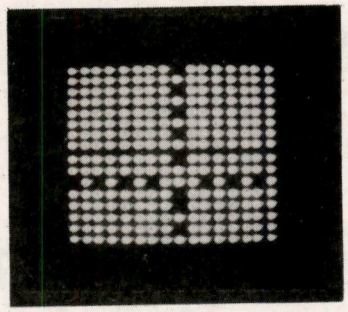


FIG. 28-3

PATTERN TYPE 3

INTRODUCES NOISE TO MAKE SELECTED CORE "one" OUTPUT SMALLER.

SELECTED CORE, #290, TYPE B, IS AT THE INTERSECTION OF LINES X=8, Y=10.

FIG. 28

DISPLAY OF STORED PATTERNS DESIGNED TO EMPHASIZE THE EFFECTS OF NON-SELECTED READ-OUT NOISE

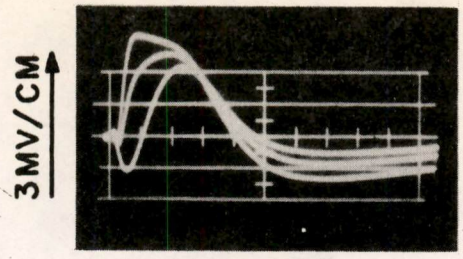
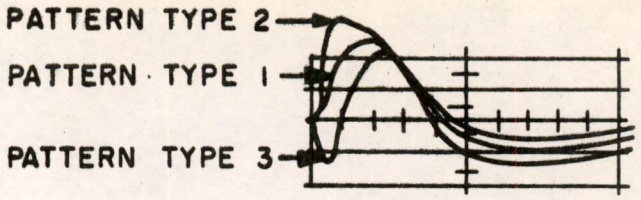


FIG. 29-1



SELECTED CORE HOLDING A "one"
FOR PATTERN TYPES 1, 2 AND 3
OF FIGURE 33.

SELECTED CORE TYPE B, #290, X=8, Y=10
OUTPUT TAKEN AT PHASE INVERTER INPUT OF SENSING AMPLIFIER.

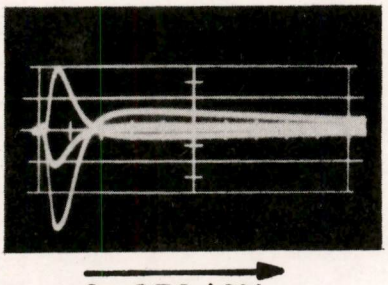
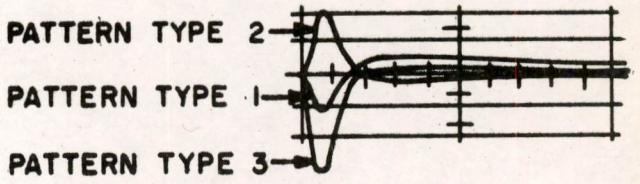


FIG. 29-2



SELECTED CORE HOLDING A "zero"
FOR PATTERN TYPES 1, 2 AND 3
OF FIGURE 33.

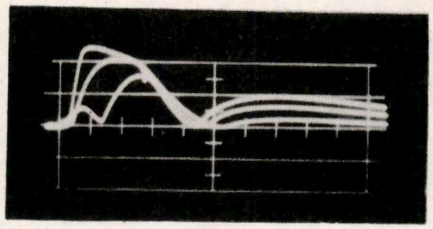
SELECTED CORE TYPE B, #290, X=8, Y=10
OUTPUT TAKEN AT PHASE INVERTER INPUT OF SENSING AMPLIFIER.

ARRAY WAS RUN AT A PRF OF 4KC WITH 2:1 SELECTION.
$I_x = I_y = 130$ MA
RISE TIME OF DRIVER $\frac{1}{2}\mu$SEC.
OPTIMUM SENSING TIME 4.33 μSEC.

FIG. 29

ONE AND ZERO INPUTS TO SENSING AMPLIFIER PHASE INVERTER
WITH ARRAY STORING PATTERNS OF FIGURE 33

3 MV/CM

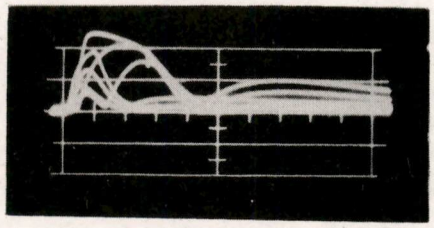


2 μ SEC/CM →

SENSING AMPLIFIER OUTPUTS, SELECTED CORE HOLDING A "one" FOR PATTERNS TYPES 1, 2, AND 3 OF FIG. 33.

FIG. 30-1

3 MV/CM



2 μ SEC/CM →

SENSING AMPLIFIER OUTPUTS, SELECTED CORE HOLDING "one" AND "zero" FOR PATTERNS TYPES 1, 2, AND 3 OF FIG. 33.

FIG. 30-2

2 TO 1 SELECTION.
$I_X = I_Y = 130$ MA.
OPTIMUM SENSING TIME 5 μ SEC.
SELECTED CORE TYPE B, NUMBER 290, X=8, Y=10.
RISE TIME OF DRIVERS INCREASED TO 2 μ SEC.

FIG. 30

SENSING AMPLIFIER OUTPUTS WHEN PATTERNS OF FIG. 33 ARE STORED

Fig. 30-2 is a composite of the ONES and ZEROS at the output of the sensing amplifier for the three patterns of Fig. 29. Increasing the rise time seems to have little effect upon the noise produced by the non-selected cores.

2. Standard Output

Since the shape of the output pulse of the sensing amplifier affects operating margins, it was necessary to establish standards so that the experimental data would be reproducible. It was decided that the gain of the sensing amplifier be set to give an output of 30 volts above bias for the smallest ONE (found by reading all "ones" into array) at the time of sensing. The output bias was set at -30 volts, and the 1/10-microsecond pulse applied to the control grid of GT2 of Fig. 23 was 30 volts high.

3. Optimum Sensing Time

A time always occurs when the ratio of the amplitude of the smallest ONE output of the sensing amplifier to the largest ZERO is maximum. This time is different for each of the 2^{256} possible patterns of stored information. Fortunately, it turns out that there exists a region of time about this point over which the ZERO-to-ONE ratio is almost constant. This region is usually one microsecond wide for a 20% deviation from maximum. For a given selection ratio (2-to-1 or 3-to-1), and for given current levels, it was possible to find by inspection of sensing panel waveforms some optimum sensing point that would be within this region for all the patterns stored. A plot of this optimum point in time for 2-to-1 current selection ratio is shown in Fig. 31.

A-52314

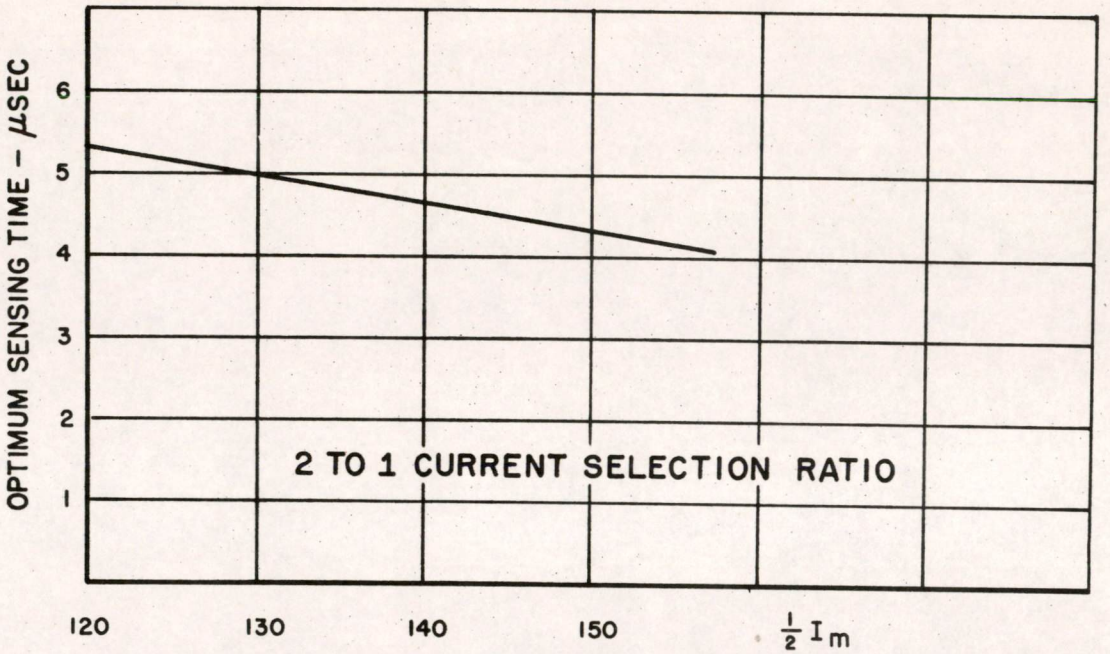


FIG 31

OPTIMUM SENSING TIME

(TIME WHEN INFORMATION IS AVAILABLE AFTER READING BEGINS)

vs $\frac{1}{2} I_m$

DATA TAKEN
ON AUGUST 12, 1952

C. SPEED OF OPERATION

The read-rewrite time, the smallest allowable time interval between the asking for a bit of information and the asking for a subsequent bit of information, is determined mainly by the time necessary to switch a core and, to a small extent, by the delays inherent in address flip-flop and crystal matrix set up time and by delays in the current drivers (including rise times). Readout time, or the time after the asking when the desired information is available, is the optimum sensing time, a function of the mode of operation, and the transient response of the sensing amplifier.

Switching time of a core may be measured by observing the sensed waveforms. The core may be considered switched when its output voltage is zero. In order to switch a core completely, the driving current gate must be equal to or greater in length than the time required for switching voltage to go to zero. If the current gate is shortened from this critical time, the sensed waveform changes; if lengthened, no change is experienced. The sensing panel, an a-c-coupled amplifier, does not permit a simple way of measuring switching time because of overshoot, but it does allow detection of change. The actual point of zero output of the sensing panel may not correspond to the end of switching. Switching times were measured by observing the durations of the read and write 1 current gates while monitoring the sensing amplifier waveforms.

When a core in the memory is to be set in either state, the information should always be read in by full-length write-0 or write-1 gates. The memory may be greatly speeded up, however, by squeezing in the current gate durations during a read-rewrite cycle.

The reading, or writing-0 operation, needs only to be carried on until the time of incidence of the sensing pulse. If the core was in the "zero" state, the reading, whether done by a long or short current, will still indicate the "zero" state. If the core was in the "one" state, it will soon be reset to that state, and the time required for this is less than if long gates were used in the reading operation. The procedure for adjusting the memory for the highest speed at given values of driving currents is the following: Set the sense pulse at the optimum sensing time. Reduce the read current gate width until the sensing amplifier output waveforms begin to be distorted at the optimum sensing time by the noise induced in the sensing winding when the read currents are shut off. The shortest allowable read current gate is usually 1 microsecond longer than the optimum sensing time. Now shorten the write-1 current gate until the amplitudes of the ONES at the sampling point are reduced to 90% of their peak values. Fig. 32 shows the minimum allowable read and write-1 times as functions of $\frac{1}{2} I_m$ for a 2-to-1 current-selection ratio. That the array was able to cycle random moving patterns is what is implied by "allowable". These times or current gate widths were measured as the intervals between those points at which the driving currents have risen and fallen to half their steady state values.

In order to estimate the minimum time required for a read-rewrite cycle with a given selection ratio, rise time of drivers, and I_m, the following calculations should be made:

min. read-rewrite time = min. read time + min. write 1 time + driver rise time + address flip-flop setup time.

There will be no delay between read and write 1. Since address setup requires $\frac{1}{2}$ microsecond, and if the driver rise and fall times are $\frac{1}{2}$ microsecond,

min. read-rewrite time = min. read time + min. write 1 time + 1 microsecond.

Using shortened gates, the array was run at a PRF of 50 kilocycles with a 2-to-1 current-selection ratio.

D. MARGINS AND RELIABILITY

1. Current Margins

It is important to have the driving currents regulated in order to have reliable operation. If the driving currents are made larger or smaller than when originally adjusted, the optimum sensing time of the first situation may not be the same as that after subsequent changes. If the driving currents are made too large, the information in the non-selected cores may be destroyed by disturbances. Also, noise due to non-selected cores may be great enough to cause ZEROS to be mistaken for ONES. On the other hand, if the driving current magnitudes are made too small, the driving current gates may not be wide enough to allow complete switching of cores, and this may entail loss of information. Also, some of the ONES may be too small to actuate the sensing gate tube. (GT #2, Fig. 23).

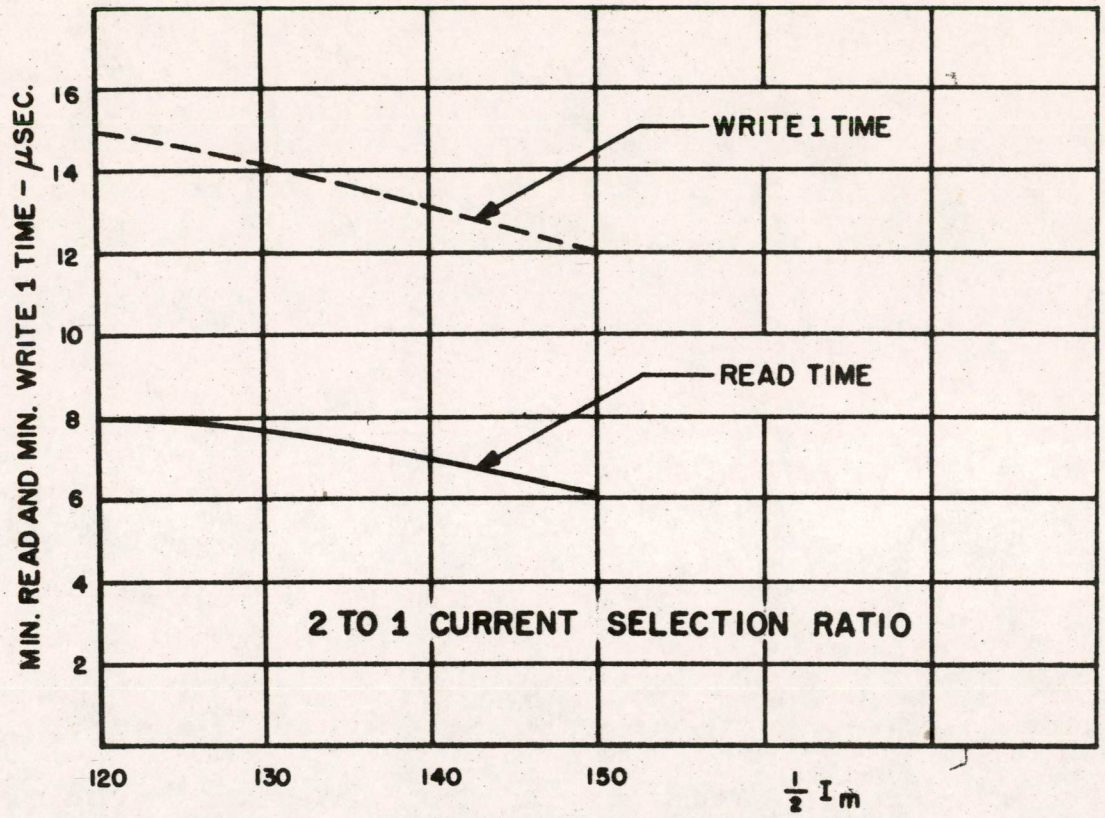


FIG 32

MINIMUM READ AND MINIMUM WRITE 1 TIMES

FOR READ RE-WRITE CYCLES vs $\frac{1}{2}$ I_m

DATA TAKEN
ON AUGUST 12, 1952

Some quantitative data were recorded concerning the amount that these currents may deviate about a set value when the memory's adjustments were optimized for that value. This was done with a driver rise time of $\frac{1}{2}$ microsecond for various values of I_m with 25-microsecond read and write 1 current gates, 2-to-1 selection, and the sensing pulse occuring at the optimum sensing time for the given value of I_m. These data, taken by cycling random moving patterns at a PRF of 4 kilocycles, are shown in Fig. 33.

2. Reliability

The system has worked successfully for six months, logging several hundred hours of memory operation with a 2-to-1 current selection ratio. During this time, errors were found to have occurred only when the power supplies were hit by heavy transients or when the system was out of adjustment. In no case was it clear that the array of cores was responsible for an error. Moveover, no deterioration of the magnetic properties has, as yet, been detected.

Use of the delay-line flip-flop gate generators (system B of Fig. 24) improves stability when the memory is run at high speed with 3-to-1 selection. Sensitivity to line transients is greatly reduced, in that operation of the array with an 8-microsecond read-rewrite time is possible whereas with gate and delay gate generators (system A of Fig. 23), this would not be so. It was found, however, that certain types of patterns, those resembling checkerboards, could not be reliably stored with 3-to-1 current selection using the system

of Fig. 23. The difficulty has been traced to non-selected noise produced by all cores linked by the "Z" axis winding except the selected core as discussed above. This noise may force a limitation upon the use of the "Z" winding during a reading operation.

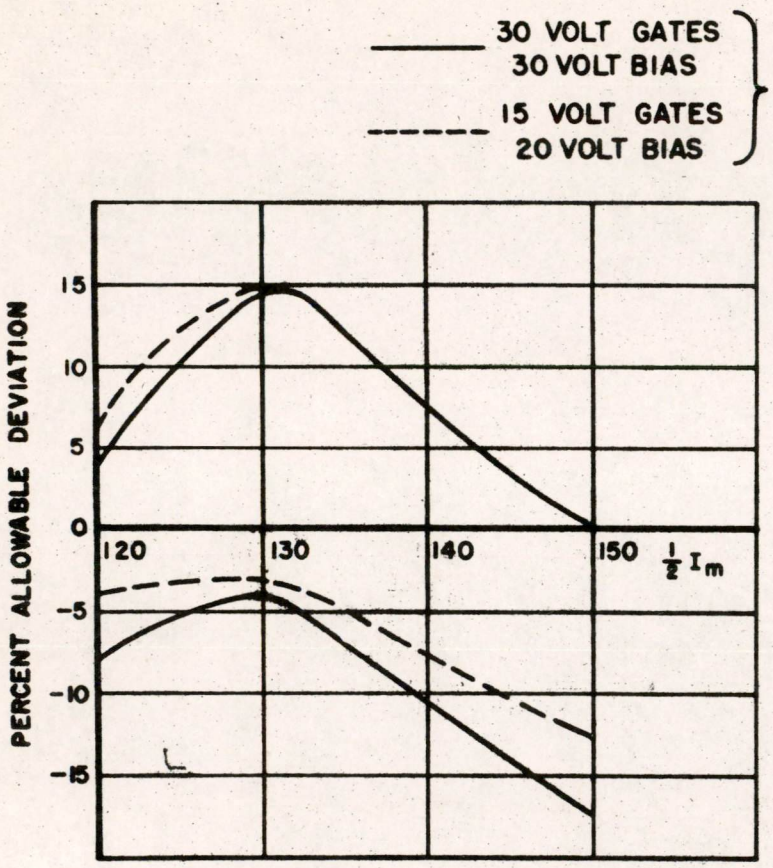
E. CONCLUSIONS

Evidence for the soundness of the concept and suggestions made in R-187 with respect to three-dimensional magnetic-core arrays has been gathered during months of testing on the 16 x 16 metallic memory. The results are encouraging for so early a stage of development of a new idea.

Two specific major problems which afflict the present array are the large variation in characteristics from core to core, and the uncancelled non-selecting output noise. Core variations can only be reduced by a high degree of quality control in manufacture and a rigorous preselection program. Uncancelled NS noise may be mitigated by improved core characteristics, by the use of multiple sensing windings and circuits, and by non-simultaneous application of the coordinate driving currents.

These problems will be studied on this array and others. Memory reliability is the first and main goal, and it is hoped that the information "put on the record" by this report will be of some small help.

A-52324



SENSING AMPLIFIER OUTPUT: 30 V GATE AT OPT. SENSING TIME, 30 V BIAS		
H_m ma	OPTIMUM SENSING TIME	SENSING AMPLIFIER GAIN
120	$5\frac{1}{3}$ μSEC	17,000
127	5 μSEC	13,000
130	5 μSEC	8,500
140	$4\frac{2}{3}$ μSEC	7,500
150	$4\frac{1}{3}$ μSEC	7,000

SENSING AMPLIFIER OUTPUT 20V GATE AT OPT. SENSING TIME, 15 V BIAS		
H_m ma	OPTIMUM SENSING TIME	SENSING AMPLIFIER GAIN
120	$5\frac{1}{3}$ μSEC	7,500
130	5 μSEC	5,000
140	$4\frac{2}{3}$ μSEC	4,000
150	$4\frac{1}{3}$ μSEC	3,000

FIG 33
CURRENT MARGINS

DATA TAKEN
ON AUGUST 12, 1952

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