digital INTEROFFICE MEMORANDUM

DATE: July 1, 1968

SUBJECT: Donations of Machines to Educational Institutions

TO: Mike Ford
cc: Ken Olsen ✓
Nick Mazzarese

FROM: Norm Doelling

1. I limit this hastily prepared list to secondary schools since the need for exposure and the potential growth in that area is greater than the need in the college environment by several orders of magnitude.

2. My criteria for selection are four-fold. First, the institution to which the donation is considered must have a program which has wide exposure to government funding agencies, particularly the National Science Foundation or the Office of Education.

Second, there must be wide exposure to other educational institutions, that is, it ought to be a regional project of some sort.

Third, it should be an innovative program in which the role of the small, stand-alone computer or small, time-shared system can be tested so that both the sponsoring institution and ourselves have some worthwhile marketing or technological information to gain.

Fourth, in any case where we donate equipment, the staff of the recipient institution must be adequately technically trained to utilize the equipment to its maximum capabilities.

On the basis of these criteria, I make the following recommendations ranked in order of importance and urgency. If any of these donations can be made in Fiscal '68, I would strongly recommend the first two be approved and implemented.

1. The Lexington School System should receive from us a high-speed paper tape reader, and a DECtape controller and two tape transports to go on our first TS-8.
Comment: In this situation the ongoing Project LOCAL has decided to accept a very minimal configuration of a TS-8 along with four other 8/I's of various configurations. The TS-8 is our prototype

test in this field. The high-speed tape reader is essential for the obvious needs for debugging and tests which will have to take place in the field. Second, the tape transports will give Walter Koelke ideas and inspirations on how to use the TS-8 in administrative applications for the Lexington School System. This project is a mature one; it is well funded by the Office of Education. The staff at the Lexington School System is technologically capable of finding innovative ways to use this system.

2. The Huntington Township High School System

DEC should donate a fully configured TS-8 with 8K of memory, an RF08 disk, an EAE, and paper tape punch and reader, 2 DECtape transports, and a DECtape controller.
Comment: Brooklyn Polytechnic Institute has been given a grant by the National Science Foundation entitled Cooperative College-School Science Program. This proposal was submitted over a year ago and was amended in January. The amendment was imposed at the specific request of NSF. The initial proposal stated that time sharing be used in 10 high schools to enrich the mathematics programs and many of the science and social science programs. NSF asked for a revised proposal which would include stand-alone computers in three of the high schools and two time-sharing terminals in seven or eight of the high schools. In at least one high school the stand alone computers would be evaluated for efficiency, utility, economy, etc., etc., with respect to time-sharing terminals. Brooklyn Polytech has ordered four PDP-8/I's with 32K word disk from us to implement this program. They are writing their own disk-oriented BASIC as part of this test. The staff at Brooklyn Polytech is extremely clever technically; they are already good DEC customers. This is a most crucial test for us. NSF already is extremely interested in this comparison; donation of a time-shared PDP-8 would be most helpful to us to assure a fair test and a favorable outcome of this experiment.

3. The Ernest A. Lawrence Hall of Science is a research center in science education located just below the Lawrence Radiation Laboratory in the hills behind Berkeley. I believe we should donate a time-shared 8 system although it probably cannot be utilized until six months from now, and thus is not of an urgent nature.
Comment: This center will be a showplace for educators throughout the nation. It will be a research institute for educators throughout the nation, and exposure here will be of great value to us.

A more complete, more considered memo will be submitted during mid-July.

cmp

digital INTEROFFICE MEMORANDUM

DATE: July 3, 1968

SUBJECT: SUCCESSOR TO PDP-9I

TO: Ken Olsen

FROM: John Holzer

The following are the only designs that have ever been seriously proposed as 9I successors:

1. 16 bit - PDP-X
2. 18 bit
   a. PDP-9 with expanded instruction set, general registers, 2's complement arithmetic
   b. 18 bit version of PDP-X
   c. New, presently unspecified architecture
3. 24 bit
4. Variable instruction word length

Larry Seligman is specifying/evaluating 2a, 2b, and 2c for John Jones. Apparently John has dropped 1, 3, and 4 from consideration.

Whatever design is adopted should at least conform to these two criteria:

1. Its instruction set should score well in a quantitative ranking against other proposed or implemented instruction sets. Otherwise, the architecture will not endure, and we will be developing new architectures ad infinitum.

2. It should employ the "family of machines" concept so that;

   a. Our customers will be more eager to learn the family's basic language, and

   b. We can spread the cost of architecture development over many machines.

Another factor: if our own sales people are unhappy with the PDP-9 design, they may pouh-pouh a PDP-9 rehashed design. The 9 group, more than any other computer group, must catch the imagination of the marketplace. It seems to me that to win big, the 9 group will have to accept big risks.

llp

digital INTEROFFICE MEMORANDUM

DATE: July 10, 1968

SUBJECT: Patent Investigation

TO: ~~Ken Olsen~~ FROM: Ed Schwartz

I was most surprised to find that no one in our organization checked with Bob Cesari as to the patentability of any aspects or workings of the 8/L or 9/L.

I think it highly desirable that before any new product is introduced to the public that Dick Best or myself be so informed so that our patent counsel can thoroughly investigate where it stands in the then status of the art.

EAS:o

yes. Let to. — We have 1 year, I think.

K. Olsen

INTEROFFICE MEMORANDUM

DATE July 12, 1968

SUBJECT Meeting with Bill Wrigley

TO K. Olsen
cc D. Sorensen
E. Schwartz

FROM J. Cohen

On Thursday, July 11, Bill Wrigley visited us to discuss his "remote data unit". Dick Sorensen, Dave Coll, Nick Wells and I were involved for DEC. Wrigley described in detail the marketing potential and technical characteristics of his invention and gave a demonstration of the prototype.

Our evaluation was fairly unanimous. On the positive side, his invention was a simple concept designed to fill what he thought was a marketing need. He had carried the work through to a complete working prototype. We all admired his determination to sell his idea. On the negative side, his FM scheme sounded somewhat expensive and was similar in effect to what we are already doing. Our conclusion was that DEC does not want to buy the rights to his patent.

I was, however, very much impressed with Wrigley personally. His invention was presented very well--he had carried his initial ideas through into design and construction. All panel lights and switches were carefully labeled, the internal construction looked very neat and it worked exactly as he said it would. My feeling is that he did a good job and carried it through to completion.

This brought up in my mind the thought that he might accept an offer of employment. He said that his prime goal is to sell his idea, but failing this he might indeed consider employment at DEC. He claims to have held a high level engineering management job with RCA (supervising 55 people). He says he left because he was disgruntled by the bureaucracy in such a large organization, and he implied that he liked what he saw of the DEC environment.

If DEC were to hire him, presumably it would be into a responsible position. Therefore I'd recommend that he be invited back to discuss employment and the he talk directly to you.

digital INTEROFFICE MEMORANDUM

DATE: July 15, 1968

SUBJECT: Proposed Machine Tool Control System

TO: Distribution List FROM: Charlie Kotsaftis

The enclosed specification concerns the application of the PDP-8/L to the machine tool control problem.

Please feel free to comment on this approach particularly as it might relate to in-house projects currently under consideration by our manufacturing department and marketing plans of the module product line.

Distribution: K. Olsen, N. Mazzarese, P. Kaufmann, S. Olsen, M. Ford, G. Rice, B. Landis, A. Devault, T. Stockebrand, J. Holzer, R. Lancaster

KEN OLSEN.

POINT-TO-POINT CONTROLLER SPECIFICATIONS

This proposal concerns the application of a PDP-8/L as a control system for a 2 or 3 axis point-to-point machine tool. It is based on the Quickpoint Tape Preparation System.

PHILOSOPHY

Quickpoint language is a simple, easy-to-use, efficient language. Because of its application in producing point-to-point tapes in minimal time with minimal input, it is only logical to use the Quickpoint language as the input for the machine tool itself. It requires that a post processor be written that directly controls the axis motion of the tool instead of punching a convential NC tape which is used as the input to existing machine tool controls.

ADVANTAGES

1. Can produce faster machining time since optimum acceleration and deceleration of the tool can be programmed.
2. Input tape, being in Quickpoint language, is easier to make, saving at least 50%, and in some cases as much as 100 to 1.
3. Input tape format error can be detected and compensated directly on the machine tool.
4. Customer buying first NC machine can learn to make tapes quicker since he has the Quickpoint language.
5. Customer does not have to buy Flexowriter at a cost of $4000-5000.

Advantages (continued)

6. Machine tool manufacturer supplying control system, also provides computer assist tape preparation, i.e., complete system.
7. Savings of Flexowriter gives additional cost justification for control system.
8. System has inherent capability through standard data communications hardware to communicate with centralized computers which are storing input information for tools, i.e., part data. NOTE: Many companies are extremely anxious to eliminate paper tape handling. They would like to start input data on mag tape and transmit to tool under centralized control - particularly larger companies.
9. Also, can be used as tape preparation system for older tools or for accounting program or inventory control, etc.

In general, all software available with Quickpoint.

HARDWARE

PDP-8/L with interface for tool, plus medium speed paper tape reader. Medium speed reader could be option, since Teletype might be sufficient initially with the computer's ability to buffer input data. This would also depend on machining speed of tool in question. The Teletype could be either on-line or separate. On-line could be used to modify machine tool data.

STRATEGY

Step 1

Design first system in house with an existing machine tool. A good possibility is a Bridgeport in the shop. The drive system would be a Slo-Syn stepping system where we could buy the retrofit drive bits and design our own interface. Software development would be minimal due to existance of Quickpoint. This system could be put together and running within 2-3 months of go-ahead.

Step 2

Demonstrate system to machine tool manufacturers. The goal would be to work in conjunction with them (they provide the machine tool and some engineering support), on implementing system to their tool. I have already received a verbal offer by the sales manager of Weidemann Division of Warner & Swasey. He might agree to provide the punch press at our facility.

Step 3

During Step 2, agressively promote this concept via demonstration, the NC Society meetings and various trade publications. Currently our contacts are excellent. I am confident we could get considerable publicity.

A part of the promotion plan would be to give a formal presentation to every machine tool manufacturer and use our existing NC mailing list to promote concept to end user.

Strategy, Step 3 (continued)

Due to Quickpoint, this mailing list exists and has approximately 2000 names. Within a year, we expect to expand this list to 4000-5000 names. This is a double-barrel approach to reach the end user and the tool manufacturer.

Step 4

Demonstrate a working system in our booth at the annual ASTME Show in Chicago next April. We may possibly be able to have an additional system or two in tool manufacturer's booths.

RESOURCE REQUIREMENTS

This program would require a full-time engineer and a full-time programmer. If someone were available with both skills he could be assisted by a technician. The PDP-8 Marketing Group would supply some programming support and all the marketing support.

GOALS

Establish DEC as THE supplier of NC computer controllers to the metal working industry.

POTENTIAL

During the current fiscal year we can expect to sell 100-200 computers for machine tool control. We are currently working with several manufacturers in this area. They are United Shoe Machinery, Sciaky Brothers and Monark Industries. Their total

Potential (continued)

potential is approximately 200-300 machines per year. Weidemann Division of Warner & Swasey could be sold 50-75 machines per year if we do the job. This estimate assumes existing hardware such as the PDP-8/L.

FUTURE

Within five years, assuming the current trend in offering lower cost computers continues, the potential could be 1000-2000 machines per year for machine tool control alone. In addition, related markets in the machine tool industry for DEC computers such as Digitizing Systems, Special Control Systems, Drafting Systems, Measuring Systems, Tape Preparation Systems, will provide additional outlets for DEC computers.

In 5-8 years the machine toool and associated markets could be 20-30 million dollars worth of business per year. This would include expanding our marketing efforts accross all product lines, particularly with the PDP-9 and PDP-10 class of computers used in conjunction with DEC's smaller computer systems for complete centralized computer control of all phases of manufacturing and factory information systems.

At this point in time, DEC has the range of products - financial and human resources to accomplish these goals. Obviously, other companies such as IBM and G.E. are working in this direction; however, I feel they do not have the range of products which DEC has.

Future (continued)

In addition, by starting at the bottom of the market, i.e., servicing the smaller shop and providing computerization for the less expensive machine tools, we can gradually build this market according to a long range plan to integrate all our existing and future products. By moving immediately in this area, I feel we can set and accomplish both short and long range goals of increased sales and profits.

dec INTEROFFICE MEMORANDUM

DATE 16th July 1968

SUBJECT Ministry of Technology

TO John Leng
cc K Olsen
H Mann
N Mazzarese
P Kaufmann
S Olsen
T Johnson
W Long
W Spittle
D Corsan (Cooper Bros)

FROM Geoff Shingles

Geoff

MEETING AT MINISTRY OF TECHNOLOGY, ABELL HOUSE, JOHN ISLIP STREET, LONDON

Present:-

Mr LLEWELYN) Mr CLOTHIER) Mr BENNETT)	Computer Advisory Service, Ministry of Technology
Mr CORSAN	Cooper Brothers
G Shingles) W Spittle)	Digital Equipment Co Limited

The meeting was convened at the request of Digital to report on the progress made by them in their schedule for production of computers in the U.K.

Of the people at the meeting, Mr Bennett was new. He was a person who paid great attention to detail and asked well thought out questions on minor as well as major points. He is apparently in a senior position with C.A.U., probably one step down from Mr Llewelyn. It appears that he is the person who will be attending to the detailed monitoring of the project.

Continued.....

The meeting opened with a statement by Digital that the meeting had not been held earlier because it was felt that real progress should be reported and that this progress was now being shown and the achievements to date had been:-

1) A letter of intention to purchase 10 million cores from Plessey to satisfy U.K. production requirements in the near future. These will be called off over approximately a one year period and is equal to approximately 200 PDP18/I stacks. Five have already been ordered for the pilot production run.

2) U.K. suppliers for power supplies, cabinet and control panels have been found and these items are available along with cables on reasonable delivery.

3) Semiconductors are being purchased from U.K. sources for the fabrication of the boards which will, pro tem, be performed in the U.S. but on these boards a significant U.K. content is achieved as the component content is approximately 70%.

The Ministry comments and queries on the above points were:-

1) Would the cores be for U.K. use only? The reply was "yes" but surplus machines produced would be used in Europe and there was a possibility of Plessey exporting the stacks to Maynard.

2) Would we be building the boards here? The reply was in the short term "no" as we wish to solve the other production problems first and maintain our expansion of effort within our "Learning" rate. In the longer term i e one - two years, the answer was "yes". We pointed out that our desire to produce here was based on a commercial premise that the quality control of the product must be maintained and that to attempt too ambitious an initial programme could jeopardise our later plans which were to expand our effort and range of items produced considerably.

Continued.....

The answers to these queries appeared to be taken in the positive way in which they were offered, especially query 2), which they pressed us on. I feel that this point should be raised by us at future meetings to emphasise it is under our surveillance and we should re-iterate our position that we certainly intend to do this production function as soon as it is reasonable to do so.

At this point it was felt appropriate to introduce the schedule we had for production (as agreed during J Leng's Maynard visit) and also to mention we had already increased our committment to include the 8/L and 9/L. It was stated that these had not caused delays in our original schedule although the 9 was one month in arrears due to the decision to build to the new mechanical configuration (this point was accepted as being a reasonable step).

In general terms, it was stated:-

a) Deliveries of parts = 3 months approximately.

b) Manufacture and checkout = 3 months approximately.

and the following timetable would be operated:-

	Initial Parts order	1st Production units	Quantity Production
8/I	June	November	January
8/L	September	March	May
9B	August	February	April
9/L	August	March	May

Continued.....

Mr Llewelyn stated that he felt these were eminently reasonable dates and that we were doing what we had stated and were also on schedule.

It was mentioned that we could foresee a point in time when our production plans could not be contained within Reading and we said we would welcome any advice Mr Llewelyn could give on this point. He said relocation to development areas was not handled by the Ministry of Technology but by the Board of Trade. However, he did state that plans were afoot to encourage certain industries to "co-locate" with Universities specialising in the particular topic of interest to the industry. This approach he stated would of course be favoured politically. This is a point worth pursuing with the Board of Trade.

The initiation and aims of the Special Systems Group were introduced as follows:-

Size

a) Now 4 engineers and 1 secretary

b) 1 year hence 12 - 14 people (including draughtsman, wireman and secretary)

Aims

a) To design and produce special products to enhance computer sales in Europe.

b) To form nucleus of engineers capable of doing initial product development with design and commercial responsibility.

The Special Systems Group really brought a very positive reaction and the points which impressed were:-

a) Design authority is being released from U.S. (This was emphasised as being the first such step to be made).

b) The fact that what are now standard DEC products (eg Displays and Data Communication systems) had come via Special Systems and it was the intention that this should happen here in Europe.

Continued.....

Mr Llewelyn said that support for the B.S. standard interface could be a worthwhile project for Special Systems to look at further. It was stated that one had already been designed.

Our new products such as VD8/I and our leading position with the large disk were discussed and were very well received, especially the large disk at a UK cost of approximately 0.25 pence per bit. Mr Bennett mentioned our plans did not initially include peripherals. It was stated that we would probably import the peripheral mechanisms in the foreseeable future (as indeed British manufacturers do, viz Data Products disks, Datamec transports etc) but peripheral controllers were in our plans, but we do feel that our main responsibility is to the market place not to "bite off more than we can chew" in the early stages and risk degrading quality. This point again appeared well taken in view of the positive intent to embark on this as soon as possible. Again, our progress in this area, especially via any UK or European "standard" peripherals eg Facit paper tape units, would help and our progress and intent should be re-iterated at the next meeting.

Mr Bennett requested a visit to see production in September when 8/I's start and this was agreed to be a good date and general product acceptance will be requested at this time.

CONCLUSIONS

1. Mr Corsan felt that this was a much better meeting with positive reactions from the Ministry of Technology and also constructive suggestions.

2. They appear to be beginning to trust us and stated that they appreciated our frankness and the detail given. The Ministry of Technology personnel certainly adopted a much more friendly posture.

Continued.....

3. The actual content required was not asked or hinted at or acceptance on "The List". The more one goes along one feels that acceptance on "The List" (which does not appear to exist in a fixed form) will be achieved not at a fixed point, but by a continuing show of progress and intent, and will manifest itself by favourable reaction to requests from the market place to the Government. Firm statement of our acceptance and progress will be solicited at each meeting however.

ACTIONS

1) Arrange September visit to Reading to include:-

   a) Inspection of product line.

   b) Latest status report on:
      (i) Production schedule
      (ii) Future plans
      (iii) Special Systems

   c) Demonstration of FOCAL.

2) Contact Board of Trade ref. The University Industrial Campus/Park scheme.

3) Arrange someone in Special Systems to contact Ministry of Technology regarding special projects eg BS Interface in which we could take an interest.

4) Via direct mail to let our market place know of our progress.

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digital INTEROFFICE MEMORANDUM

DATE: July 30, 1968

SUBJECT: Datron, Inc.

TO: Ken Olsen
Joe St. Amour

FROM: Menno Koning

I visited Datron, Inc. on July 26, and Seldon Lazarow told me of his forthcoming lunch with you on August 19.

Datron is a small company, now having six employees, started by principals from Anelex. Seldon Lazarow is president, and Robert Curtis is vice-president. They have funding from New York, and although it is not publicly known, they started a printer development program approximately two months ago. Their schedule calls for completion in one-half a year. Although they are competent people, I do not believe that they will meet such a short schedule.

Both Lazarow and Curtis come highly recommended.

bwf

digital INTEROFFICE MEMORANDUM

DATE: July 30, 1968

SUBJECT: Japanese Peripherals

TO: Ken Olsen FROM: H. Painter

Peripherals tend to be the weakest area of the Japanese computer business, from what I've learned so far. In fact, most computer manufacturers either import peripherals from the U. S. or manufacture here under license.

Tally paper tape equipment is common, as are IBM selectrics and flexowriters. CDC apparently has had some success in selling mag tape transports and disks.

A fellow from Honeywell in Japan told me that although some mechanical I/O devices are available here, the price, after shipping and duty, is higher than in the U. S.

I'll be visiting Fujitsu in the near future to see what they have and to see if they're interested in our PC02 and disks.

Mike Ford has some information I sent on T.D.K. plated wire memories. Although these memories are fast, the price is still higher than core.

Will keep you posted.

Best regards,

H. Painter

HOP/yk - No. 038

INTEROFFICE MEMORANDUM

DATE 5th August, 1968

SUBJECT Min Tech Meeting to present PDP-9 Computer - 25th July, 1968

TO K. Olsen
H. Mann
W. Hindle
S. Olsen
N. Mazzanese
J. C. Peterschmitt
W. Spittle
W. Long
D. Knoll

FROM G. Shingles

PRESENT:

G. Shingles)	
P. Burton)	D.E.C.
R. Willis)	
Mr. Loy)	
Mr. Thompson)	Min Tech.
Mr. Clothier)	C.A.U.

The meeting was held in three phases:-

I.	General Presentation - Production plans - Performance to date	G. Shingles
II.	Hardware Presentation	P. Burton
III.	Software Presentation	R. Willis

The hardware and software presentations were well received. Some interesting comments were made as a result of the initial presentation which included a resumé of our production plans.

Mr. Thompson was a new face and although we had been in contact about two years ago, he has recently become involved in our plans and is anxious to keep in close touch and monitor our work closely. He reports to Mr. Bennett who was mentioned in my previous memo as the man in charge of monitoring our progress. Thompson is a more open and forthright person than any so far, met and made some comments on our previous meeting with Min. Tech. They were as follows: -

continued/.....

1. I commented that our last meeting with Mr. Llewellyn on 15th July 1968 had been very useful and he stated that although they could have been mistaken they felt a bit intimidated by the "heavy artillery" we brought in to the earlier meeting in March.

2. The advantages of moving to a University campus type location for engineering and production were mentioned for the third time. (I have obtained from the Board of Trade a long list of Government Agencies and Nationalised Industries who are instructed - all things being equal - to purchase from firms operating their manufacturing units in development areas. This is, I am now sure, where Honeywell have gained much of their edge. (see attached sheet)

3. Mr. Thomas asked "what was the strange rumour he had heard about us buying semi conductors here and shipping them to the U.S.A. for board fabrication. People feel this is a bit fishy. This was one thing that could affect us getting onto the list of British Manufacturers". He said he presumed this was our intention. I reasoned as follows: -

> "Our intention is to progress as rapidly as possible in our production plans. We do feel that we have a strong responsibility to our customers to maintain quality of our products and we feel that this was the most logical step in view of the availability of plated thro hole capability in U.K. at present".

I also stated we have been building boards here for the special G.P.O. approval of the communications systems.

Personally I obtained the feeling that moves such as this cause them to doubt our committment a bit, but as long as we have a good technological argument it will be accepted.

- - - - -

At a recent meeting with Perkin-Elmer their Technical Adviser to the Managing Director gave some useful information.

From a previous meeting I knew he was going to Min Tech and I asked him to try to find independantly their position relative to us.

Mr. Nicolls of Min. Tech. with whom he spoke did not regard us as being British yet and stated that the process of becoming recognised as such was not clear cut and involved committments to production, development research and

continued/.....

also software generation. A broad based programme was indicated.

digital INTEROFFICE MEMORANDUM

DATE: August 14, 1968

SUBJECT: INEXPENSIVE TYPEWRITER RE-MEMO 8/1/68

TO: K. Olsen FROM: J. St. Amour

cc: R. Collings
P. Kaufmann

An inexpensive incremental and/or continuous typewriter can be built consisting of the following items:

1. Single type wheel approximately 2 3/4 inch diameter (64 characters) and .100 inches wide that has a 90° segment which is a feed cam (see figure 1).

2. Three combs, probably plastic, with teeth .100 inches wide spaced .200 inches apart. (For back spacing capability need four combs with teeth .300 inches apart.)

3. Non-traveling hammer which is a four bar linkage covering entire surface.

4. Motor -- 600 RPM = 10 characters per second and should have no wear problems -- 1800 RPM = 30 characters can be investigated.

5. Ball spline.

6. Paper feed mechanism operated by first rotation of type wheel.

7. Solenoids to actuate hammer and select combs.

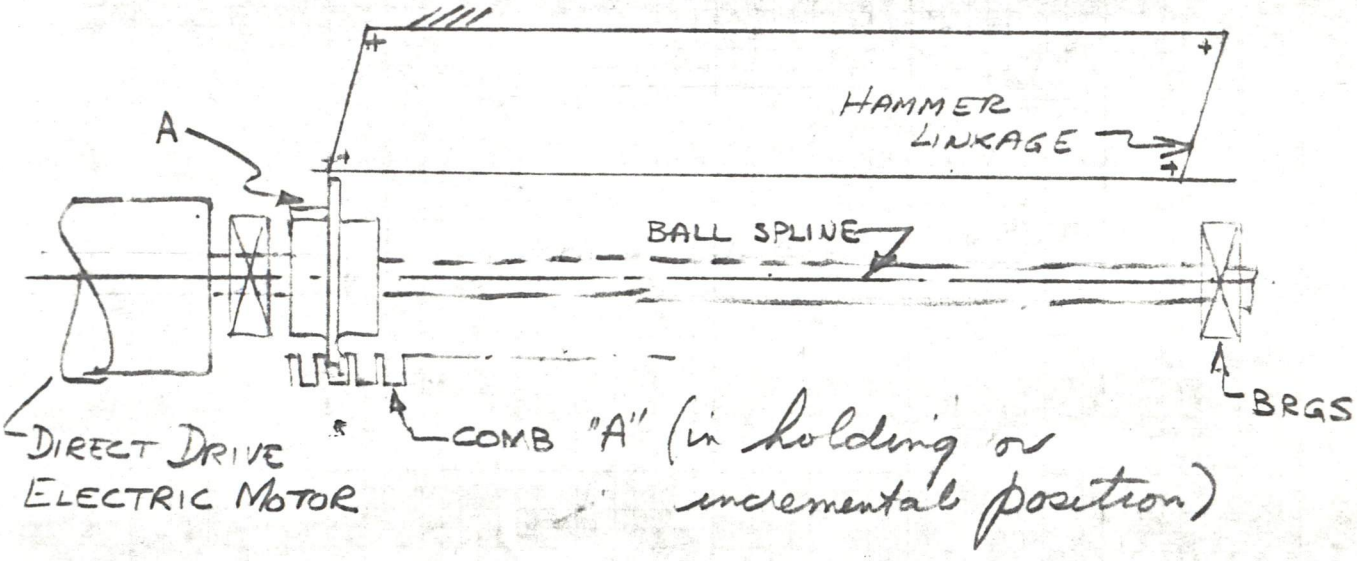
8. Hunter or similar type wheel return spring.

9. No ribbon, use carbonless paper.

The type wheel motor can rotate continuously or be shut down at any position. In continuous operation, the combs will be alternately fed into position to allow the type wheel to feed itself along the ball spline. If incremental mode is required, the comb feed can be held back, thus keeping the type wheel in a single position

until typing occurs. Withdrawal of all combs causes type wheel return to start. A single hammer will type any column location. Hammer solenoid recovery can occur during index to next position.

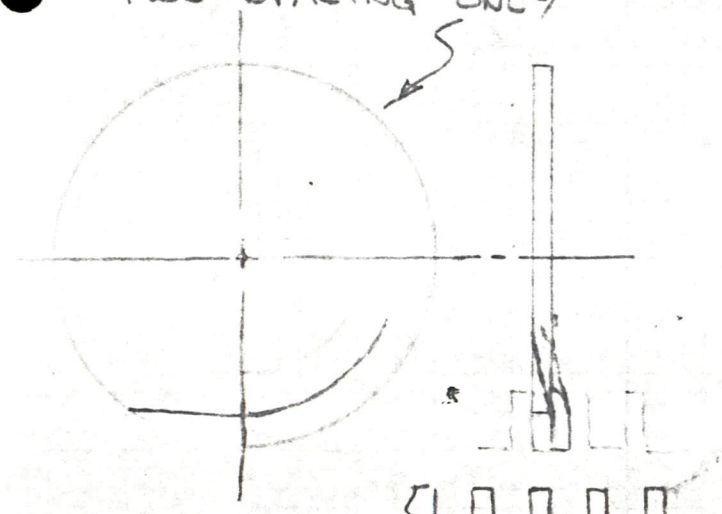
/kb
Attachment



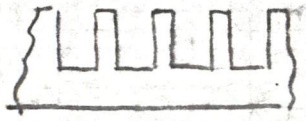
A - Cam on type wheel to index paper during print rotation.

8-14-68

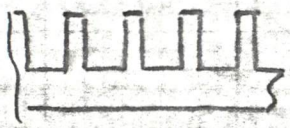
TYPE WHEEL
FWD SPACING ONLY



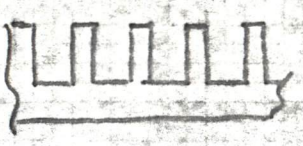
COMB "A"



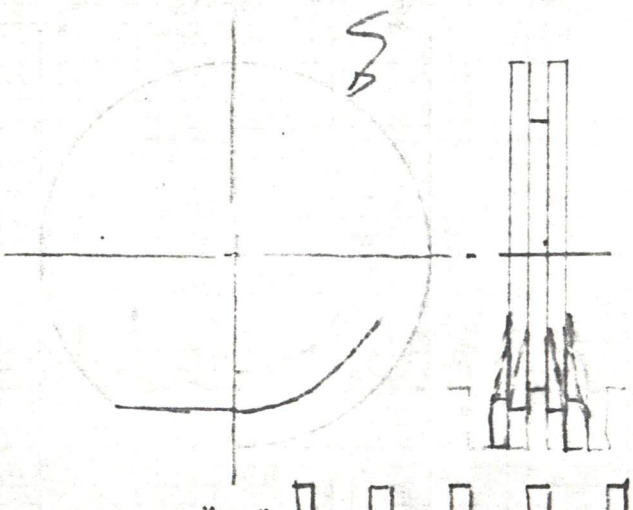
COMB "B"



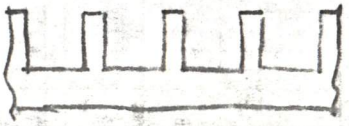
COMB "C"



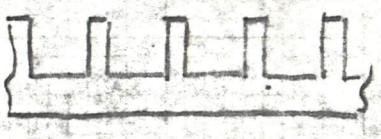
TYPE WHEEL
FWD + REAR SPACING



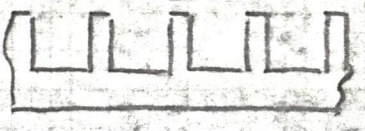
COMB "A_1"



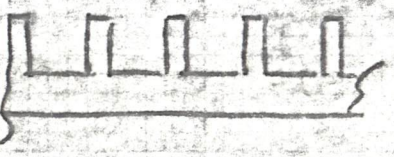
" B_1



" C_1



" D_1



8-14-68

9/20/68 Copies given to Nick and Win.

digital INTEROFFICE MEMORANDUM

DATE: August 14, 1968

SUBJECT: RELIABILITY PROBLEMS WITH PDP-8 & PDP-6, 10 AT APPLIED LOGIC CORP., PRINCETON, N. J.

TO: Ken Olsen FROM: John S. Jorgensen

We are experiencing some subtle intermittent failures with the equipment being used by our very good customer, Applied Logic Corp., in Princeton, N. J. Neither our field service engineers nor Applied Logic Corp. engineers can sufficiently isolate the troubles to pinpoint the source as being DEC hardware, interface problems, software problems, or externally generated noise. Unfortunately, the situation has degenerated to the point where the A.L.C. people do not have confidence in the PDP-8 computer and feel that perhaps its design is marginal, making it unusually susceptive to intermittent failures or external noise. Based on my recollection of your interest in "front line" problems and several documents you generated on noise problems in computer installations, I felt that you might wish to personally look into this situation. I feel there is a strong possibility that systems or environmental noise could be responsible for our difficulty and, in any event, I feel your attention would serve to accomplish the following:

1. Impress Applied Logic Corp. with the depth of our concern for their needs.

2. Perhaps solve A.L.C.'s problem and restore their confidence in our equipment.

3. At least insure A.L.C. that their problem is not due to marginal engineering or deficiencies in the design and manufacture of PDP-8's (and ensuing 8 family machines such as the PDP-8/I).

If you are inclined to assist us, please contact myself or Mel Mager, our District Service Supervisor, for further details.

Regards, John

JSJ:tdz

cc: Dave Cotten, Jack Shields, Dave Denniston, Mel Mager
Mike Ford

digital INTEROFFICE MEMORANDUM

DATE: August 19, 1968

SUBJECT: 8/L Power Supplies in the 8/I

TO: Ken Olsen

FROM: Roger Cady

cc: M. Ford
W. Long

The idea of putting an 8/L power supply in the 8/I has merit - and we actually tested an 8/I with the prototype 8/L supply.

There are several points that are presently inhibiting the incorporation of the 8/L power supply into the 8/I. The 8/L does not use any regulated -15 except for memory slice which we zener from -30. The 8/I with negative bus, and several of the options require a more closely regulated -15 then ±20%. A better approach would be the use of an 8/L type design, but tailored for the 8/I with -15 regulated.

The 8/I restrictions on line frequency and the resultant cost of a ferroresonant regulator have disturbed me for some time. Jim O'Loughlin is now developing a switching mode regulated supply which will be frequency insensitive. This may be the best approach to the 8/I's higher power requirements.

When I return from Wescon I will get together all the data on 8/L and 8/I and then make some detailed judgement on the route we should pursue. I do feel that we should improve all product rather then just European.

dec INTEROFFICE MEMORANDUM

DATE 20 August 1968

SUBJECT MAGNETIC DISKS

TO Ken Olsen

FROM John Leng

cc: Bill Long

Re your memo of May 3 (attached).

Did these people contact us in Maynard, as they told Bill, or has nothing happened on this?

Since I have now departed, I suggest that Bill Long be your contact man on matters such as this.

JL: cah

TOTTENHAM 4336

MR. CULLY

digital INTEROFFICE MEMORANDUM

DATE: May 3, 1968

10 MAY 1968

SUBJECT: MAGENTIC DISKS

TO: John Leng
cc: Joe St. Amour
Steve Lambert

FROM: Ken Olsen

We now have a good source of magnetic disks for our disk storage units, but it is our only source so we have to develop a backup in case this one disappears. Because they are so critical to us, I would like to consider making the disks ourselves.

We think we can develop the plating with the skills we have developed in that area, but would like to line up suppliers of machinery for machining the disks. Then if we need the equipment, we can get it very quickly. A large number of people are manufacturing IBM disk packs, so machinery and techniques for making aluminum blanks are getting to be quite well developed.

I understand that one of the ways of preparing blanks is to buy a lathe from Bryant-Simmons in London. With this lathe, people are able to make the disks flat and obtain a finish fine enough to plate without lapping.

Will you have someone contact this company to find out if this is really true. We would like to know the cost of the equipment and how large a disk can be handled. We would also like to know how they are able to make it flat, and if they supply the cutting tools to obtain this very fine finish. We should also find out the delivery of the machine. We may not get moving on this project until we are in trouble.

Ken

ecc

17 May 68

John -
Wally has contacted these people. They have qualified representation in the U.S. and will contact Ken Olsen there directly.

Wlong

digital INTEROFFICE MEMORANDUM

DATE: August 21, 1968

SUBJECT: A 16-bit PDP-8

TO: Ken Olsen
Nick Mazzarese
George Rice
Mike Ford

FROM: Richard Merrill

9/5

cc: Nick Mazzarese
Rick Merrill
John Jones
Stan Olsen
John Jones
Gordon Bell
from Ken Olsen

A 16-Bit PDP-8

I. Need

Customers need an inexpensive 16-bit computer for numerical control and laboratory data acquisition/ analysis. Statements made to justify a larger word length run the gamut from "everyone does it" to "multiple of eight" (no pun intended) and "increased accuracy". Also heard are the words "8-bit ASCII bytes" and "powerful instructions".

Salesmen have supplied more potent statements when fighting the 16-bit competition. The toughest cases arise when both accuracy and speed requirements give the edge to a single or double precision 16-bit word (0-15, 0-31) over a comparable double or triple 12-bit word (0-23, 0-35).

A number that is to contain information on the order of one part in a million needs 20-bits of data (1,048,576); but to retain that accuracy through several operations requires four or five bits more. This is borderline for two 12-bit words but just fine for two 16-bit words. Thus, the argument for increased accuracy bear the most force.

II. Requirements

A. Compatibility

Such a computer should be 99% program compatible with the PDP-8. This means that the machine could be fully usable with a minimum of programming effort. In fact, only the assembly, debugging, loading, and MAINDEC programs need to be rewritten since these are intimately concerned with the logic of machine. All other programs such as FOCAL would only need to be reassembled. Certain device oriented programs like the Disk Monitor would require minor corrections.

II. Requirements (Continued)

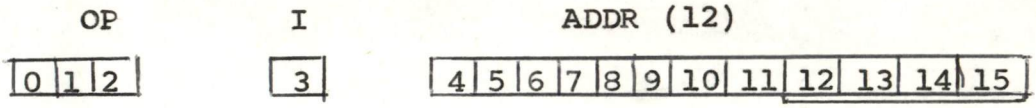
B. Simplicity

The machine should be as simple as possible to design and manufacture and easy to learn and to use. The instruction set should be streamlined yet relevant and should build upon that of the PDP-8.

III. Bit Allotment

The assignment of bits to supplement those of the PDP-8 order code is the crux of the problem. Three ways suggest themselves as reasonable.

A. The first would add four bits to the address portion of the PDP-8 giving a direct addressing capability of 4096:



0-4096

However, several studies and estimates show that full-field addressing capability, however convenient, is rarely used efficiently. Thus, 99% of the instructions in an average program could use only 80% of the available bits.

B. Therefore, a paging scheme seems to be a reasonable compromise between efficiency of utilization and convenience plus the bonus of expanding the instruction set.

0 - 2048

Adding only three bits to the address field gives an address range of 2K, but this prevents access to page zero (0-200) which violates the compatibility requirement.

III. B. Continued

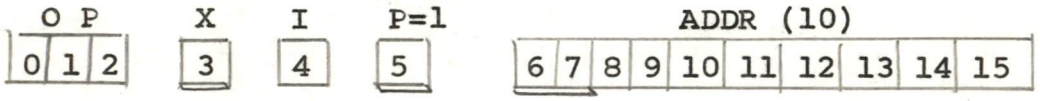
Adding a page bit gives us the ability to reference not only the current 1000 words but page zero as well:

0-1024

While program compatible, it is still not efficient to have one thousand words of commonly addressable page zero. Page zero is used predominantly for constants and subroutine pointers. Rarely could a thousand such be used!

C. A simple alternative scheme for page zero references can give us unique power and efficiency. For page zero references we shall take two bits from the direct address:

1) Current page operation

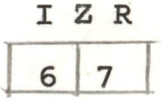


0 - 1024

2) Page zero references

0 - 256

This scheme still gives a larger (400 octal) page zero but lets us treat these references in a still more special way by specification of the IZR bits to control Indexing of page Zero References:



0 - no change

1 0 increment register content

1 1 decrement register content

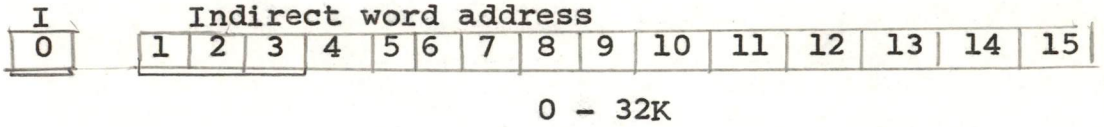
III. C No. 2 Continued

Thus each page zero location may be used as an index register! But the index function is fully programmable and operates in either direction. This simple feature is an extremely powerful programming tool.

On the PDP-8 incrementing can be done by ISZ or by using auto-index registers. Unfortunately, a program often needs to reference indirectly once without change in a series of index instructions which otherwise could use an auto-index register. As a result it is rare that any program makes either extensive or efficient use of the auto-index register.

Also, this indexing feature could be made usable with or without the indirect bit. This might necessitate an additional time state in the processor logic, but a special check would not have to be made for 10-17. The assembler would perform this function to achieve program compatibility.

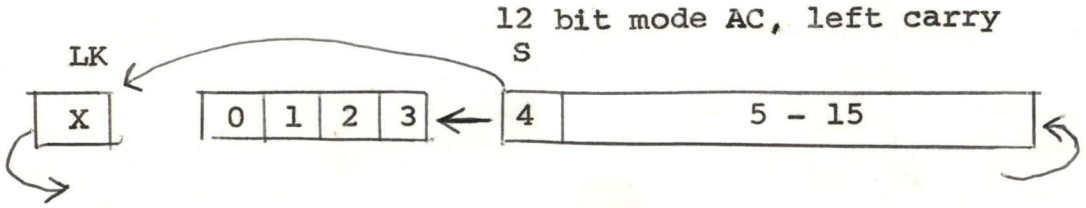
3. Indirect references can easily use bit zero to continue multi-level indirect chains. This would provide another powerful facility whose need is often felt in programming the PDP-8:



This eliminates the need for the awkward and space consuming manipulation of instruction and data fields.

4. The AC

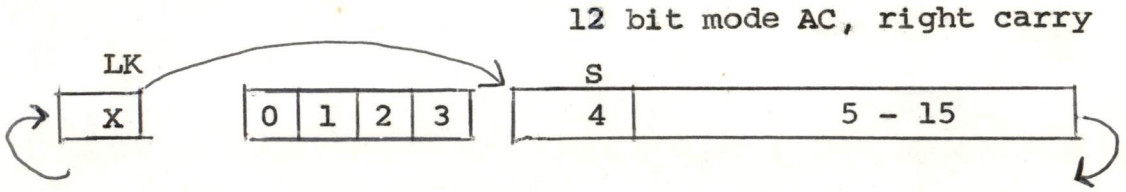
Finally, it is necessary to modify the AC to achieve program compatibility. This is done by using one of the new operate group (1110) instructions (there are at least $2 \uparrow 4$ new ones) to setup control modes for either 12-bit or 16-bit operation:



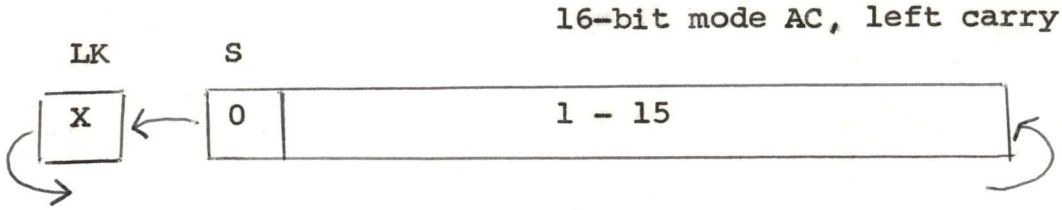
LK indicates the link bit, S the sign bit, and the arrows the left-hand carry in 12-bit mode. This scheme will work for

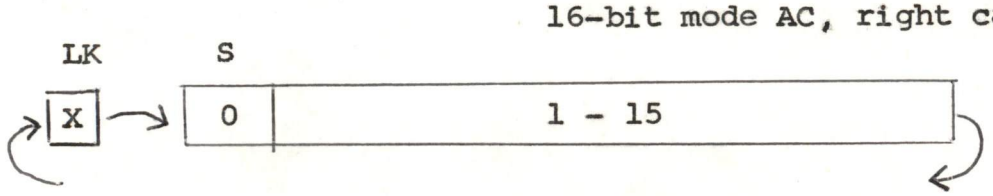
(a) normal addition (TAD) in two's complement,
(b) 12 bit testing,
(c) address computation regardless of negative numbers, octal constants, and masks,
(d) left rotates, and
(e) nearly all instruction formations.

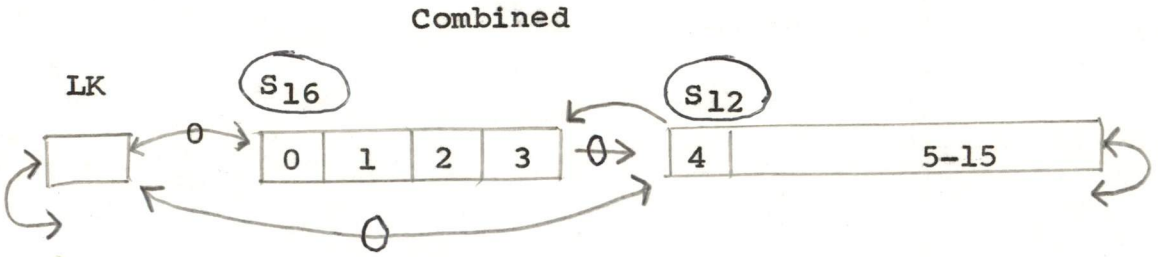
The latter are a rare and questionable practice ans since they are usually formed by adding a constant to an existing instruction there should be few problems of this kind.



For right rotates there should be no difficulty at all.







Only the circled paths and the sign bit definitions are controled by the 12/16 mode setting.

5. Summary

This arrangement of bits creates 1K page modules, 256 page zero index registers, a powerful and flexible indexing ability, extended indirect addressing range, total program compatibility, and the possibility to create eight new memory reference instructions (X = 1).

IV. New Instructions

In augmenting the PDP-8 instruction set we want to create codes that save a good deal of program space, programming effort, and execution speed with hardware readily available or not too far removed from that present in the PDP-8/I design. There are several memory reference instructions worth considering:

A. ADM - Add to Memory satisfies all of these requirements. Normally this takes three instructions

```
TAD   MEM
DCA   MEM
TAD   MEM
```

This can be implimented merely by setting both AC enable and MEM enable during time-state-two of the execute cycle.

B. Bit test instructions are becoming increasingly important for systems development on the PDP-8. Larger systems have a need for more status bits, and testing these (commonly called "bit crunching") is quite time consuming. For example:

```
TAD  BITS              TAD BITS
AND  MASK      or      RAL
SZA  CLA               SMA
```

IV. B. Continued

Such testing also destroys the contents of the AC which must then be reloaded.

SBN - Skip if bits not equal

SBO - skip if bits ones

SBZ - skip if bits zeros

There are also several bit setting instructions that might be considered.

C. Byte manipulation is important in symbolic data storage and retrieval for communications high order languages, et cetera.

0101 BYL - byte left half

1101 BYR - byte right half

If the leftmost bit is incremented and the overflow tested, then the instructions would self-convert to the opposite polarity. i.e. BYR when executed would become BYL automatically. The overflow bit would be added to the indirect memory address to automatically precess through a string of data. Perhaps this could be combined with decrement XR to reverse direction. Another option would be to have read byte and write byte.

D. Recursive Subroutine Call

CAL

E. Logical Instructions

XOR

F. Execute

XCT

G. Skip if unequal

SUN

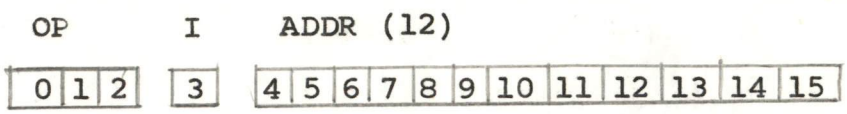
H. SAM - Search for A Match for the AC starting with the effective address and terminating when result found or bit zero is set to a one. This instruction would speed up FOCAL by a factor of five, assemblies by a factor of 10.

I. Others

Undoubtedly several others could be suggested. The selection can be made by a small jury of three representing hardware, programming and sales.

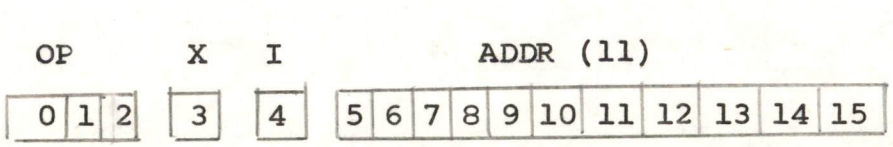
Appendix

I.



0-4096 7777

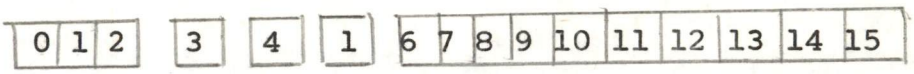
II.



0-2048 3777

III.

A.



0-1024 1777

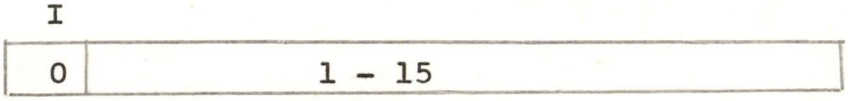
B.

0-256 377

0 - no action
1 0 INCR REGISTER
1 1 DECR REGISTER

C.

INDIRECT WORD

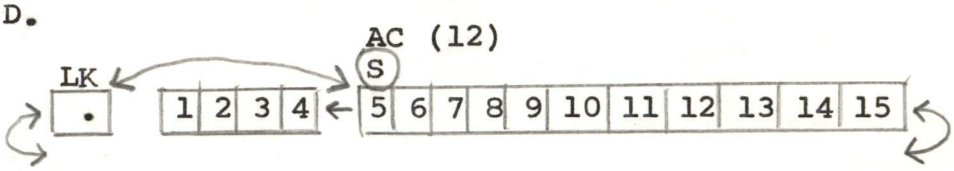


0-32K

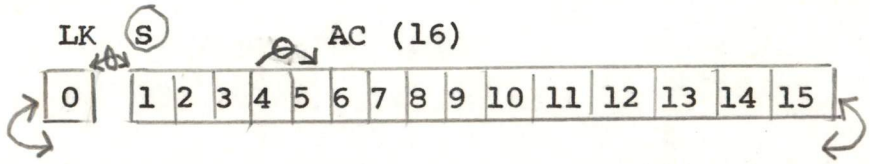
III. C. Continued

A. multi-level indirect
B. no field settings etc. required.

D.



E.



F. For X = Ø the PDP-8 instruction set

000	AND	16 bits data always
001	TAD	16 bits data always
010	ISZ	mode dependent (overflow test)
011	DCA	16 bits always
100	JMS	zero + 15 bits stored
101	JMP	--
110	IOT	10 bit device code = 1024 devices!
111	OPR	PDP-8/I microprogrammable operation set, plus 4 bits. For X = Ø the extra bits are used to augment the rotate class instructions. For X = 1 = mode control 12/16.

G. For X = 1 we can create seven (0-6) new memory reference instruction (MRI) codes:

(1) Bit tests

0011 SBN - skip if bits not equal

0111 SBO - skip if bits ones

1001 SBZ - skip if bits zeros

(2) Add to memory

1011 ADM

(3) Byte manipulation

0101 BYL

1101 BYR

III. G. Continued

4. Other

CAL, XOR, XCT, SUN, SAM

mc

digital INTEROFFICE MEMORANDUM

DATE: August 23, 1968

SUBJECT: PDP-8-190 AT SIEMENS

TO: Ken Olsen
Nick Mazzarese
Ted Johnson
Mike Ford

FROM: Jack Shields

I expect Ken to get a letter within the next few days from Director Gellinek referencing problems with his machine. The system is now up and was finally made operational by Bill Freeman from our Product Support group. However, it's important to understand a number of the details surrounding this installation.

The machine has been off warranty for a long period of time and maintenance has been performed by Siemens very infrequently or DEC when we were called. The PDP-8 was originally a table top machine which was converted to a rack mounted machine by the customer. The computer was allowed to get into a deplorable condition of operation and we discovered this when visiting to install a number of add-on options which had been ordered by Siemens in March.

The options installation started in March and it has taken us from March until now to put the system into proper operation and get all of the various options working. One of the options was a disk which was damaged in shipment and this prolonged the time for installation due to the fact that we had to ship a new disk, rewrite the timing track, realign, etc.

It's true approximately seven different people have been working on the system since March and it has taken until now to correct the problems. Field Service didn't do a very good job in this case. We do feel, however, there were extenuating circumstances and the situation has now been rectified. Bill Newell will visit Mr. Gellinek next week. Suggest any reply to Mr. Gellinek be made pointing out that we have asked Bill Newell to investigate and take the proper course of action. We are confident this will solve his problems for him.

ned

digital INTEROFFICE MEMORANDUM

DATE: August 26, 1968

SUBJECT: Invention Disclosures

TO: Ken Olsen

FROM: Ed Schwartz

I would greatly appreciate it if whenever you receive an inquiry from an outsider, as to whether or not DEC would be interested in any personal invention or idea, that this letter be channeled through me if you wish to pursue the matter.

All too frequently, I read of corporations involved in patent litigation because they had responded to an inquiry, such as I refer to above, without having the inquirer sign a non-confidential waiver. I have embarked upon a procedure of having such waivers signed prior to anyone in our company reviewing such disclosures.

I truly believe if the above procedure is followed we could well eliminate future problems.

EAS:o

digital INTEROFFICE MEMORANDUM

DATE: August 28, 1968

SUBJECT: More on 16 bit PDP-8

TO: Roger Cady

FROM: Richard M. Merrill

cc: Nick Mazzarese
Ken Olsen

More on 16 bit PDP-8

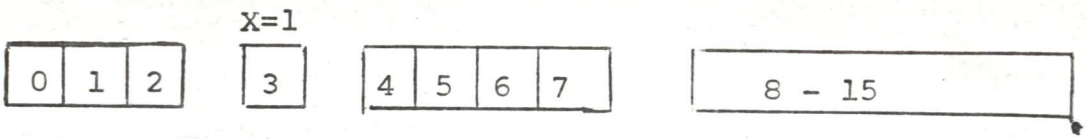
(C. F. proposal of ____?____)

Bits and Bytes are increasingly important! In fact, research shows that instructions to manipulate small data components are used more frequently than any others beyond the essentials.

Large systems programs have many status bits to test. On the PDP-8 and PDP-9 such testing takes as many as five instructions to test a single bit! For TS-8, the Disk Monitor, etc. mere bit crunching creates an intolerable system overhead and complexity. The following proposed extended instruction set would save execution time and many programmer headaches.

Bytes are essential for manipulating ASCII data. For conversational systems such as FOCAL and TS-8 byte manipulation is an enormous gain.

All PDP-8 programs run with bit 3 (called X) = Ø. For X = 1 we will have the following bit utilization:



8 bits

Test and Set to

bits 1 & 2

00 Ones
01 Zeros
10 Complement
11 No change

and skip if

bits 456	0	Equal
	1	Not Equal
	2	Ones
	3	Zeros
	4	Don't Skip
	5	Load byte into AC
	6	Parity of byte into link
	7	not used

Using

bit 0 & 7	00	Left half
	01	Right half

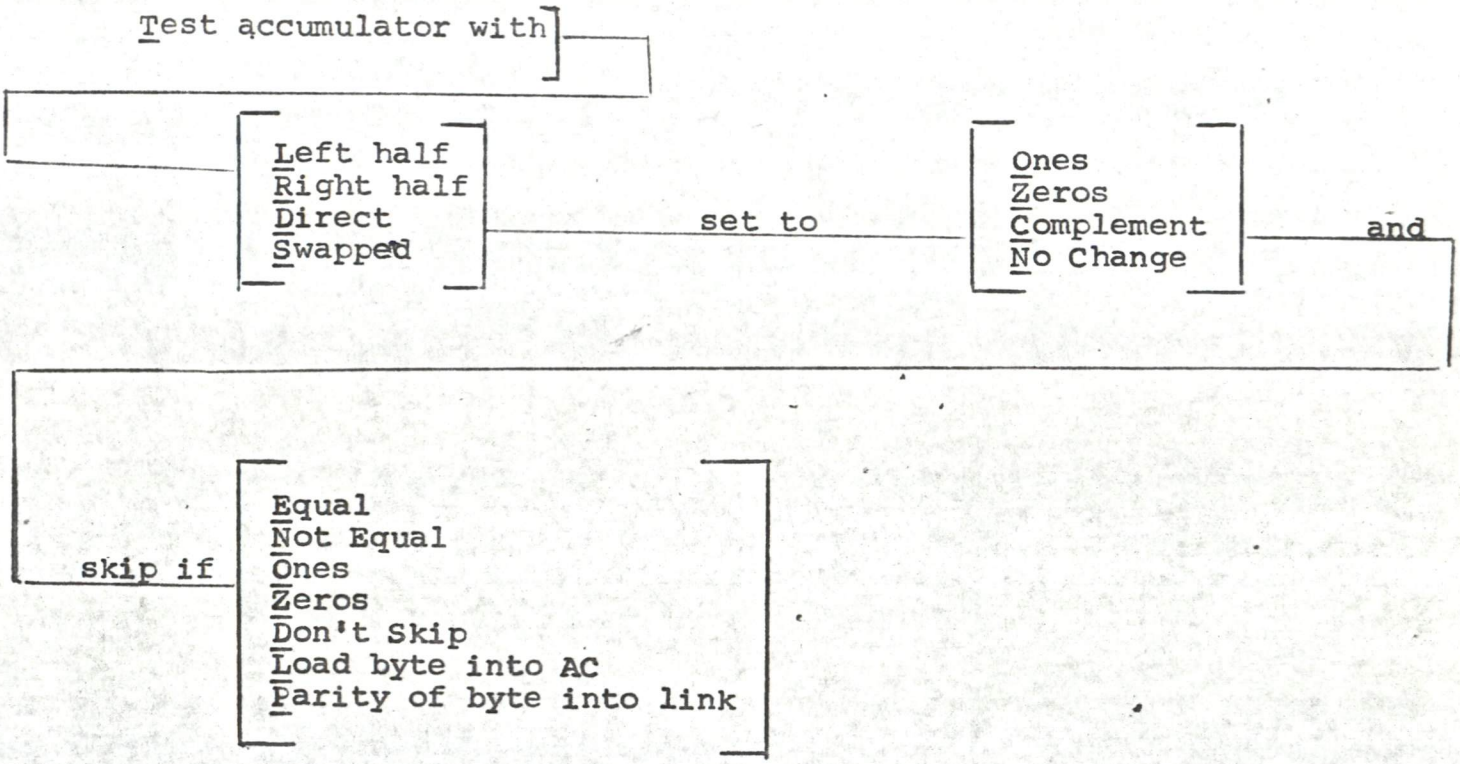
These two are executed in immediate mode using the rightmost 8 bits as the data.

	10	Direct
	11	Swapped

These use the full 16-bit contents of address on page zero.

Note: This bit assignment and instruction is independent of mode and is always considered to be in 16 bit mode.

SUMMARY OF MNEMONICS



Combinations Array

T	L	O	E
	R	Z	N
	D	C	O
	S	N	Z
			D
			L
			P

There are therefore 112 brand new instructions!

They are unambiguous, logically complete, easy to learn, and easy to assemble!

digital INTEROFFICE MEMORANDUM

DATE: 29 August 1968

SUBJECT: R. Merrill's Proposed 16-bit PDP-8

TO: Ken Olsen ✓ FROM: L. Seligman

9/5
cc: Nick Mazzarese
Rick Merrill
John Cohen
Stan Olsen
John Jones
Gordon Bell
Jim Nielsen

I have studied Rick Merrill's proposal for a modernized PDP-8 and find myself in almost complete agreement with him. His approach of assembly language compatibility with emulation aids* achieves simplicity and increased power, yet minimizes reprogramming and retraining for people experienced with the PDP-8.

There are a number of technical issues which ought to be discussed further as he suggests, but the basic instruction format and addressing facilities are excellent. A further improvement can be made by drawing on John Cohen's ISC as is shown in the figure below. The simplicity of the PDP-8 is retained and familiar programming techniques need not be discarded. Retraining of customers and salesmen will be easier with Rick's machine than with more complex or very different machines such as PDP-X or the "desk calculator".

The question of IO has not been discussed, nor has the question of how many 16-bit machines we ought to make**.

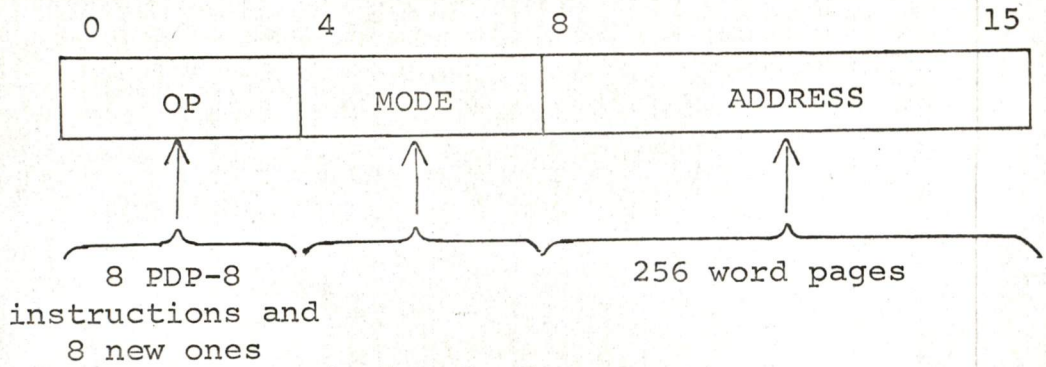
These are important issues that ought to be discussed before we proceed very far on any of these projects. I would hope that they all could share, at least, memories and IO devices.

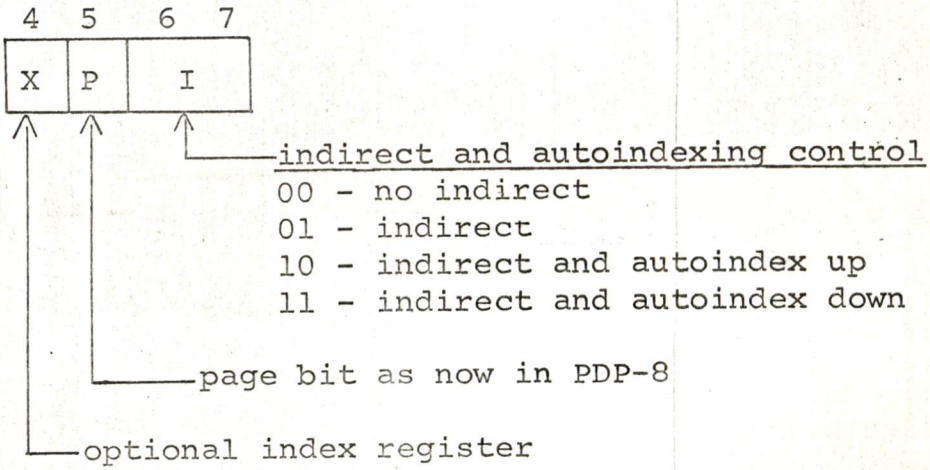
---

* Since the proposal before us implied rather than clearly stated these points concerning compatibility and emulation, let me amplify them. For any new computer with somewhat different capabilities than its predecessors, we must rewrite the diagnostics, the assembler, and certain other basic programs regardless of the nature of the new machine's compatibility with the old one. If, however, there is assembly language compatibility between the machines so that packages like TYPESETTING, FOCAL, FORTRAN can simply be reassembled, a purely mechanical process, ones saves the major burden of reprogramming at least to the extent that users will accept programs that do not fully utilize the capabilities of the machine.

In order to achieve this compatibility, it is important that emulation hardware be included in the new computer. The amount of hardware required is inversely related to the number of restrictions placed on the program to be emulated. My proposal along these lines was based on total compatibility; Rick's makes computed instructions illegal and in so doing achieves greater freedom in choosing an instruction format for the new machine. His seems the better compromise since, as he states, computed instructions "are a rare and questionable practice" at best.

**16-bit PDP-8, "desk calculator", PDP-9I replacement.


0
4
8
15
OP
MODE
ADDRESS
8 PDP-8 instructions and 8 new ones
256 word pages


4 5 6 7
X
P
I
indirect and autoindexing control
00 - no indirect
01 - indirect
10 - indirect and autoindex up
11 - indirect and autoindex down
page bit as now in PDP-8
optional index register

digital INTEROFFICE MEMORANDUM

DATE: August 30, 1968

SUBJECT: Pricing of Disk Pack Systems

TO: Bob Savell
cc: Win Hindle

FROM: Dave Cotton

We recommended the following prices for elements of the PDP-10 Disk Pack systems:

RP10 control	$23,000
RP01 drive (Memorex 630)	22,500
RP02 drive (Memorex 660)	26,000

in what we hoped would maximize profits by selling the maximum number of units at a good profit per unit.

In our pricing study, we found the following prices for competitive systems:

Competitor	Control Price	2311-Type Drive Price	2314-Type Drive Price
CDC	$25,000	$23,000	--
EAI	$23,000	$22,000	--
IBM	$27,200	$26,300	$252,000*

*for eight (8) drives

In addition, we took into account IBM's rental prices:

IBM 2311
purchase price = $26,300
rental/month = $ 575

IBM 2314 (8 drives)
purchase price = $252,000
rental/month = $ 5,250

These compare to:

DEC RP01

purchase price	=	$22,500	or	$23,000
rental at 1/30	=	$ 750		$ 766
at 1/40	=	$ 562.50		$ 575

DEC RP02

		Single	Eight	Single	Eight
purchase price	=	$26,000	$208,000	$27,000	$216,000
rental at 1/30	=	867	6,933	900	7,200
at 1/40	=	625	5,200	675	5,400

But our primary concern, in setting the pricing of the RP01 and RP02, was the unit prices that Memorex charges for the 630 ($20,900) and 660 ($24,000). It was our concern that if our prices were significantly above these unit prices, customers would purchase only controls, or controls plus one (1) drive, and buy additional drives from Memorex. Arguments about warranty and delivery from a single supplier (DEC) would be balanced by large savings for the customer buying 3-8 drives/system.

We have tried, unsuccessfully to date, to obtain the prices that SDS will charge for simular units, but Al Spahr (Memorex salesman) tells me that SDS is changing the units in such a way as to not be competitive (he would not say more).

As a result of the information shown above, I would recommend we stick with the drive prices of $22,500 and $26,000, although we probably can raise control prices to $24,000 (not higher) without seriously endangering sales.

Ken Olsen

digital INTEROFFICE MEMORANDUM

DATE: September 3, 1968

SUBJECT: Memorex Disk Pack Contract

TO: Bill Burns FROM: Bob Savell

cc: Lon Beaupre
Operations Committee

The Operations Committee would like to insure that the following terms are inserted into any contract we sign with Memorex.

1. Our financial liability will be limited only to the recomputed discount if we take delivery on less than the quantity contracted for during the delivery period.

2. If due to any other fault than Digital Equipment Corporation's reduction in quantity, Memorex fails to deliver the agreed-upon-quantity during the contract period, then the contract terms delivery period shall be extended until such time as Memorex can complete the quantity contracted for and if DEC so desires, and in any case, the price charged DEC will be the agreed-upon-price for the quantity we were originally scheduled to receive.

3. If for any reason Memorex reduces their prices during the contract period, all units delivered subsequent to the effective date of the reduced price will be paid for by DEC at the reduced price.

The Operations Committee further believes that since we have confidence that we can sell 300 units over a three-year period, then we should order the 300 units. Harry Mann will make sure that the proper reserves are set up to allow for payment of recomputed discounts in the event we either cancel early or, for other reasons, take less than the number of units for which we contracted.

bwf

digital INTEROFFICE MEMORANDUM

DATE: September 4, 1968

SUBJECT: Summary of Storage Tube Display System Configurations and Specifications

TO: Ken Olsen

FROM: Murray Ruben

I System Configurations

A. KV8/I STORAGE TUBE CONTROLLER

The KV8/I storage tube controller consits of a group of 4 modules designed to plug into the PDP8/I internal option interface to form a basic unit capable of point plot and linear or circular ~~strobe~~ stroke vector generation. Output is to the Tektronix Type 611 storage tube monitor oscilloscope or equivalent. The KV8/I contains means to activate the erase and write-thru functions of the scope. It also contains means to display analog inputs from a graphic input device and to select and read these analog signals into the computer by means of an analog to digital conversion program. There are two options which may be added to the basic KV8/I.

1) The KV8/I-A includes an option which permits the specification of live non-stored vectors or points in addition to stored vectors or points. This option also improves the line resolution of the display so that all vectors appear with equal resolution. This option would be used in appli-

cations requiring some degree of live interaction with a display containing mostly static (stored) information.

2) The KV8/I-B includes a multiplex interface option which permits up to 8 individual users to time share the KV8/I controller running independent programs. The interface accepts inputs from remote user keyboards and from remote graphic input devices.

3) The KV8/I-C is a combination of both of the above options.

Designations have been developed to describe the other components of the complete graphics terminal.

1) The VT01 refers simply to the Tektronix 611 Scope and to the graphic input device as a group of system components.

2) The VT02 refers to the complete remote station consisting of a VT01 and a keyboard with appropriate interface logic to control the remote station.

A complete single graphics terminal system then is composed of a PDP8/I, a KV8/I and a VT01. The PDP8/I ASR33 serves as the keyboard input device.

A multiple graphics terminal system is composed of a PDP8/I, a KV8/I-B or KV8/I-C and one or more VT02 terminals with appropriate interconnecting cables.

B. VS08 STORAGE TUBE CONTROLLER

The VS08 designation consists of the 4 KV8/I system modules in a half rack of logic with a power supply and appropriate interface converters to permit operation on a PDP8, PDP8/S, or PDP8/I external standard negative I/O bus. The VS08 may have either or both options, and the same letter option designations are used, i.e., VS08-A for refreshed vectors, VS08-B for multiple scopes, and VS08-C for both options. Remote stations still have the VT02 designation and are identical to those used for the KV8/I-B.

C. VS09 STORAGE TUBE CONTROLLER

The VS09 consists of a KV8/I and appropriate interface modules mounted in a half rack of logic with power supplies to permit interface to a PDP9 I/O bus. Provision is included for use on an API bus in the basic logic. Again the A, B, and C designations refer to the KV8/I options.

II Specifications of the KV8/I Controller and Its Options

A. HARDWARE MODULES AND INTERFACE

The KV8/I contains 4 modules:

1) M712 - I/O TIMING MODULE. This module decodes the IOT instructions and generates all system timing. It contains one adjustment for ~~strobes~~ stroke timing.

2) A612 - D/A AND GATE LOGIC. This module contains the data buffer and generates all gate signals for the

the A312 as well as the analog output from the D/A and all scope control signals. The modules also are containing a comparator to permit the selection and reading of one of two analog input signals by means of an appropriate computer program. The A612 contains 3 adjustments associated with the comparator.

Interface signals from/to the PDP8/I positive bus.

Signal Name (asserted +3V)	Number of Unit Gate Loads
BMB03(0)	1
BMB04(0)	1
BMB05(0)	1
BMB06(1)	1
BMB07(0)	1
BMB07(1)	2
BMB08(0)	1
BMB08(1)	2
BMB10(1)	4
BMB11(1)	4
AC02(1)	4
AC03(1)	2
AC04(1)	3
AC05(1)	2
AC06(1)	3
AC07(1)	2
AC08(1)	4
AC09(1)	6
AC10(1)	4
AC11(1)	4
IOP1	4
IOP2	2
IOP4	3
INITIALIZE	1
SKIP BUS RETURN	-
INTERRUPT BUS RETURN	-

Assigned locations in the PDP8/I

A312	HJ22
M712	HJ23
A612	HJ24
A712	J21
A313	H25
M713	J25

NOTE: H21 is spared for use by required buffer gates if necessary.

3. A312 ANALOG FUNCTION GENERATOR. This module accepts the 10 gate signals and the analog output generated by A612 and produces an appropriate X and Y axis output deflection signal to the Tektronix scope. Digital signals to the A312 include the following:

NAME	ACTION WHEN ACTIVE
PM	SELECTS THE POINT PLOT MODE
VM	SELECTS THE VECTOR MODE
CUR	SELECTS THE CURSOR MODE
RST	RESETS THE SAMPLE/HOLD AND INTERGRATED/ HOLD CIRCUITS
LV	EXECUTES A LONG VECTOR LINEAR STROBE
SV	EXECUTES A SHORT VECTOR LINEAR STROBE
CM	EXECUTES THE CIRCLE GENERATOR
ABS	CAUSES DATA TO BE LOADED IN ABSOLUTE REPRESENTATION
XFX	CAUSES THE X SAMPLE/HOLD TO SAMPLE THE D/A
XFY	CAUSES THE Y SAMPLE/HOLD TO SAMPLE THE D/A

The A312 contains 22 adjustments, all except 6 of which are adjusted only once, and all except 2 of which do not interact with each other. A block diagram of the KV8/I is shown in Figure 1 of the VD8/I brochure, which also shows the major paths in the AFG.

4. A712 VOLTAGE REGULATOR. This module accepts ± 15 to ±18 volts input and produces tightly regulated ±12 volts output to power the analog modules in the system.

The KV8/I options are contained in 2 modules:

1. A313 INTENSITY CONTROL MODULE. This module computes a Z axis pulse modulated signal proportional to the writing rate of the stroke being executed. Selection of 20µs or

.5μ pulses determines whether the vector is stored or not stored.

2. M713 MULTIPLEX INTERFACE OPTION. This module generates five interface signals for the VT02 remote terminals, and accepts the single return signal generated by the remote keyboards. These signals are as follows:

MXO	READ/WRITE SELECTION LINE
MX1, MX2, MX3	THREE STATION SELECTION CODE LINES
STROBE	SYNCHRONIZATION PULSE LINE
KBRET	A COMMON RETURN LINE FOR SAMPLING REMOTE KEYBOARDS

In addition, the M713 generates a real time 1 KHZ clock signal normally used to periodically interrupt the computer in order to effect a line scan of the incoming terminals.

The normal single scope system has the following interface signals:

XOUT YOUT	Analog deflection signals to scope X and Y axis inputs. Output from op amplifier, input to 100K at 80pf. Level ±1 volt.
XCUR YCUR	±1 volt return signals into 10K input impedance for graphic input device
Z	Digital intensify Z axis signal from normal 7410 gate. Scope input 100K at 80pf.
ERS/ERD	A bilateral digital bus driven by transistion driver. Negative going edge causes scope to erase and hold the line down until erase cycle is complete. Input

scope load is 10ma sink current.

WRT — A single digital line driven from 7400 gate which activates the scope write through curcuitry to produce small non-stored circular cursor. Scope load is 5ma sink current.

INTR — A single digital return line originating at the graphic input device interrupt request push button and terminating in a 2ma gate load.

In the multiple scope system, the same signals are present with the exception that WRT is generated locally by the VT02 interface and INTR is no longer part of the bus but instead derives from the clock on the M713. In addition, the six multiplex signals are added to the bus.

B. GENERAL PERFORMANCE SPECIFICATIONS

1. General

Scope	Tektronix 611 storage scope
Size	16 by 21 cm (6 by 8 inches)
Resolution	over 300 stored line pairs

2. Data Representation

Number Representation	10 bit 2's complement D/A
Addressing	±511 addressable co-ordinates. Normally adjusted to 512 co-ordinates in 6".

3. Vector Generator

Method	Analog ~~strobe~~ stroke
Functions	Linear or circular vector, or point

Execution Rates 250μs for short (up to 3/8") vector.
4ms for long (up to f/s) vector.
30μs for point.

Loading Rates 120μs to load X or Y

4. Vector Representation

Absolute or incremental linear vectors

Absolute point or circular vectors

5. Scope Control

Erase, write-thru and Z axis

6. Graphic Input

Accepts and displays ±1V analog signals in write-thru

Selects and compares ±1V X or Y signals against D/A

7. Keyboard Input

From TTY or (with B or C) option) micro switch Keyboard.

8. Intensity Modulator Option

Permits selection of stored or refreshed vectors

Max. 1500 vec/sec (approximately 8 characters or 50 vectors) line vectors.

9. Remote Terminal Options - (Max. of 8 terminals)

Keyboard 54 key ASR33 type keyboard

Graphic Input From ±1V source, local cursor display

Cabling Hardwired - 4 analog, 8 digital lines
4 KC min bandwidth
1000 feet maximum distance

10. Software

Edgrin editor with graphic interpreter interpretive graphics language

Basic subroutines for character generater, A/D conversion, basic output routine, and multiplex line scanners.

Patches to run Focal on the scope

Advanced Edgrin for disc swapping system with ability to call Focal

C. IOT INSTRUCTION (PDP8 FAMILY)

IOT		ACTION
6051	SNC	SKIP IF INTERRUPT FLAG IS LOW, ACTIVATE REAL TIME CLOCK INTERRUPT IF PRESENT
6052	CCF	CLEAR INTERRUPT FLAG
6053	SKB	SKIP IF KEYBOARD RETURN BUS IS HIGH
6054	LMX	LOAD AC BITS 8 THRU 11 AND EXECUTE INSTRUCTION:

AC8 HIGH - SELECTS STATION CODE AC9 to 11 AND ACTIVATE ITS WRITE SELECT CONTROL TO PERMIT IT TO ACCEPT SCOPE OUTPUT COMMANDS.

AC8 LOW - SELECT STATION CODE AC9 to 11 AND READ THE NEXT BIT OF ITS KEYBOARD REGISTER BACK ON THE KEYBOARD RETURN BUS

6062 LAC — LOAD AND SELECT ANALOG COMPARATOR:

AC BIT 2	9	6	FUNCTION
0	0	0	READ X INTEGRATOR
0	0	1	READ Y INTEGRATOR
1	0	0	READ X SAMPLE/HOLD
1	0	1	READ Y SAMPLE/HOLD
1	1	0	DISPLAY CURSOR AND READ X CURSOR SIGNAL
1	1	1	DISPLAY CURSOR AND READ Y CURSOR SIGNAL

6063 LDF — LOAD AND SELECT FORMAT, CLEAR VECTOR CONTINUE:

FORMAT

AC BIT 2	9	
0	0	VECTOR MODE, RELATIVE INPUT
0	1	VECTOR MODE, ABSOLUTE INPUT
1	1	POINT MODE
1	0	DISPLAY CURSOR

6064 LDX — LOAD X SAMPLE AND HOLD, CLEAR READY FLAG AND RAISE WHEN X IS LOADED (APPROX 120μs)

6065 LDY — SAME AS 6064 EXCEPT THE Y SAMPLE AND HOLD IS LOADED

6066 EXC — EXECUTE MICRO PROGRAMMED INSTRUCTIONS:

BIT	FUNCTION WHEN SET	NOT SET
2	See under 6063	
3	Erase the scope.	No action.
4	Set write thru option to refresh; execution to short vector speed.	Normal stored mode with speed set by bit 6.
5	Spare	
6	Execute long vector unless inhibited by bit 4.	Execute short vector.
7	Set vector continue when flag is raised.	Vector continue disabled.
8	Execute circle vector.	Execute linear vector.
9	See under 6063	
10	Reset integrators and sample/holds.	No effect.
11	Intensify vector.	Blank vector.

The ready flag is cleared and will go high at the end of 30μs for point plot, 250μs for short vector, and 4ms for long vector. The flag will also go high after 30μs in vector continue.

Any logical combination of bits may be grouped together to form an execute command.

6067 EXL — SAME AS 6066 EXCEPT THAT A LONG VECTOR WILL BE EXECUTED (UNLESS INHIBITED BY BIT 4) REGARDLESS OF THE STATE OF BIT 6.

6071 SRF — SKIP IF READY FLAG IS HIGH.

6072 CRF — CLEAR READY FLAG.

6073 SDA — SKIP IF D/A IS GREATER THAN (SELECTED) ANALOG COMPARISON SIGNAL.

6074 LDA — LOAD D/A

digital INTEROFFICE MEMORANDUM

DATE: September 9, 1968

SUBJECT: Some Random Thoughts on I/O Terminals

TO: Ken Olsen FROM: Ken Larsen

I/O terminals will probably evolve to some "standard form" (a la IBM compatible mag tape) or at least some standard conventions. In the meantime, many people will be pushing to make their device the industry preferred (or standard).

For applications with a high volume of information with a minimum of change, such as, telephone directory, airline schedules, etc., the device manufactured by Image Systems (Div. Houston Fearless), which has a carousal mechanism to position a 96 frame microfiche in a back lighted projector viewer, (I believe the DOARS system is a combination of this device and an IBM CRT) is the most practical. The photograph in this case is the low cost storage device.

For the Limited Character Terminal, I suggest you look at the Friden calculator. They use a CRT that is produced in high volume at a low cost and get a quite acceptable numerical display. For Alphanumeric Terminals, we probably should use C.C.I. or Conrac to give us a product without the engineering time and dollars invested. This would give us some experience in determining what would be the most desirable and economical method for building a terminal.

The application or systems analysis and implementation is going to be a key factor in the ability to sell terminal devices.

"Point-of-sale terminals" involve the exchange of money and must be tamper proof, particularly if there is to be a credit card reader involved. There will be attempts made to make fake credit cards or change credit cards to "beat the system." Cards that are magnetically coded are subject to tampering or at least "read" and duplicated by an unauthorized person. The information could also be inadvertently destroyed by exposure to a magnetic field, unless it does not depend on residual magnetism (a card with holes is easily duplicated or modified). LRL, for their security system, chose the copper strips

imbedded in the card to avoid the problems associated with magnetic materials. Their badge is easily produced using printed circuit etch techniques for half of the laminated badge. A badge/card reader with high reliability in all aspects would be valuable as a component in many areas outside the "point-of-sale" terminal. These would include: security, production control, reservation/ticketing, inventory control, etc. In this area, someone must set the standard - maybe we can, but most likely it would be in conjunction with someone like Addressograph/Multigraph. We should have them educate us on the current "credit card" system and try to determine their interest in working with us on a "new system."

I would like to discuss this with you if you are interested.

mdo

digital INTEROFFICE MEMORANDUM

DATE: SEPT. 9, 1968

SUBJECT: Market Analysis for the KV8/I-L Display and its options

TO: Ken Olsen

FROM: Murray Ruben

cc: P. Greene
N. Mazzarese
G. Rice

One and a half days of researching the past market for display products and estimating the future market have resulted in the ~~pxo~~ following figures:

Past market performance for display products

Product	Number Delivered*	Number on Back Order**
pdp 5	100	
pdp 8	1359	40
pdp 8S	726	30
pdp 8I	173	292
pdp 8L	-	100
linc 8	121	6
34B	10	-
34D	150	3
34E	5	
34H	55	
30N	10	
338	28	
339	6	
VC8I	8	6
VD8I	-	8

*source-field service 7/5 **source- computer admins. 8/24

From these figures, display products represented about 12% of overall PDP 8 sales, but a lower percentage of 8I sales. This may be due to incomplete data or to large OEM usage.

The 34D and VC8/I represented captive sales where, in most instances the display was not the primary reason for the customer buying the computer, but instead the display was bought for its value as a convenient option.

The KV8/I represents a complete display system, of greater power and considerably less expense, than any other existing system. It would be reasonable to assume that the display will be responsible for selling computers, rather than vice versa.

Therefore, it would seem reasonable that 5 to 8% of future PDP 8 family sales will have a KV8/I or one of its options. Additionally, maybe a similar number of past PDP 8 customers will buy the VS08 as a retro-sale, distributed over a two to three year period.

These numbers would imply a monthly average rate of from 5 to 8 systems based on 100 Family 8 sales per month. Additionally, 1 to 2 systems a month can be expected from the family 9. This makes between 72 and 120 systems as a base level. In addition, approximately 1 in 10 customers will probably order the multi-terminal system (this is about the percentage I have experienced in talking with some 25 or so potential customers, although several more - a total of maybe 25% - indicated an interest in adding additional scopes at a later date after the initial system was ordered). The multi-terminal customers will require an additional 40 to 60 scopes.

The net total therefore would lie between 102 and 180 scopes for the first year of production.

An independently conducted response from P. Greene resulted in very similar numbers being developed. It is my ~~xxxxxxx~~ belief that these numbers represent a conservative analysis of the potential market for the KV8/I. Talks with visitors at the exhibitions in England, and talks with other customers, have convinced me that this system will be very easy to sell.

digital INTEROFFICE MEMORANDUM

DATE: September 9, 1968

SUBJECT: Some Random Thoughts on I/O Terminals

TO: Ken Olsen FROM: Ken Larsen

I/O terminals will probably evolve to some "standard form" (a la IBM compatible mag tape) or at least some standard conventions. In the meantime, many people will be pushing to make their device the industry preferred (or standard).

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I would like to discuss this with you if you are interested.

mdo

digital INTEROFFICE MEMORANDUM

DATE: September 11, 1968

SUBJECT: Matsushita Electric

TO: K. Olsen
H. Mann
Ted Johnson
Nick Mazzarese
Howie Painter

FROM: Ron Wilson

Dr. Tsuguo Yoshida visited DEC Maynard approximately four months ago.

He had lunch and a tour of our facilities. No mention was made of a joint venture or license arrangement.

I have a complete brochure on Matsushita Electric (parent company) and Matsushita Communications for your peruse.

sjk

digital INTEROFFICE MEMORANDUM

DATE: September 16, 1968

SUBJECT: PDP/9 HEAT TESTS

TO: Don Vonada
cc: Ken Olsen
Stan Olsen
John Jones
Loren Prentice

FROM: Dave Nevala

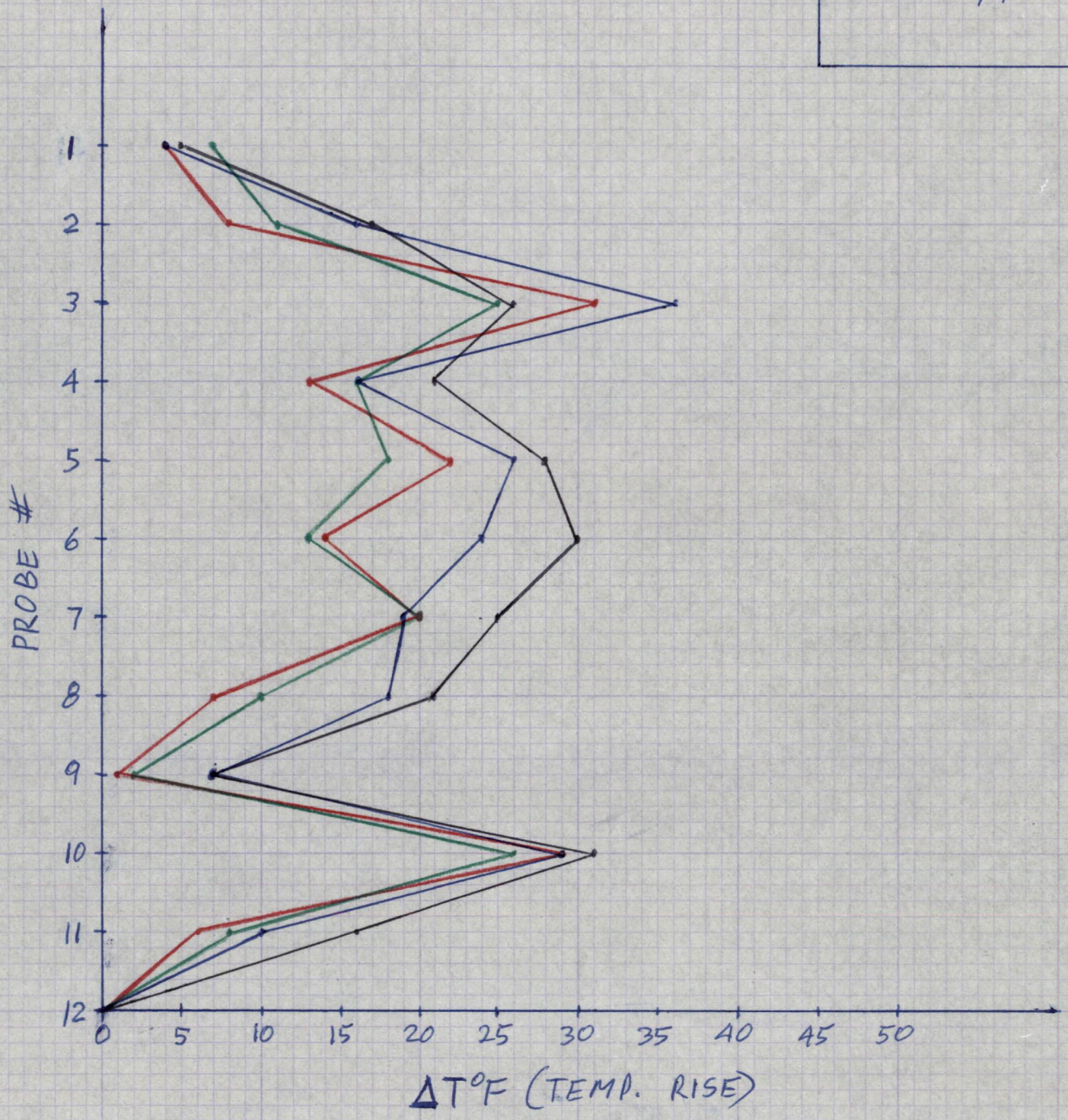
Included with this memo are the results of four heat tests run on the PDP/9. The variables in these tests were caravel fans below the table and foam strips in the modules.

It can be seen on the curves that probes #3 and #10 still run above a 20°F. temperature rise on test #4. Probes #5 and #6 in the extended memory control area show a significant improvement in test #4.

Dave

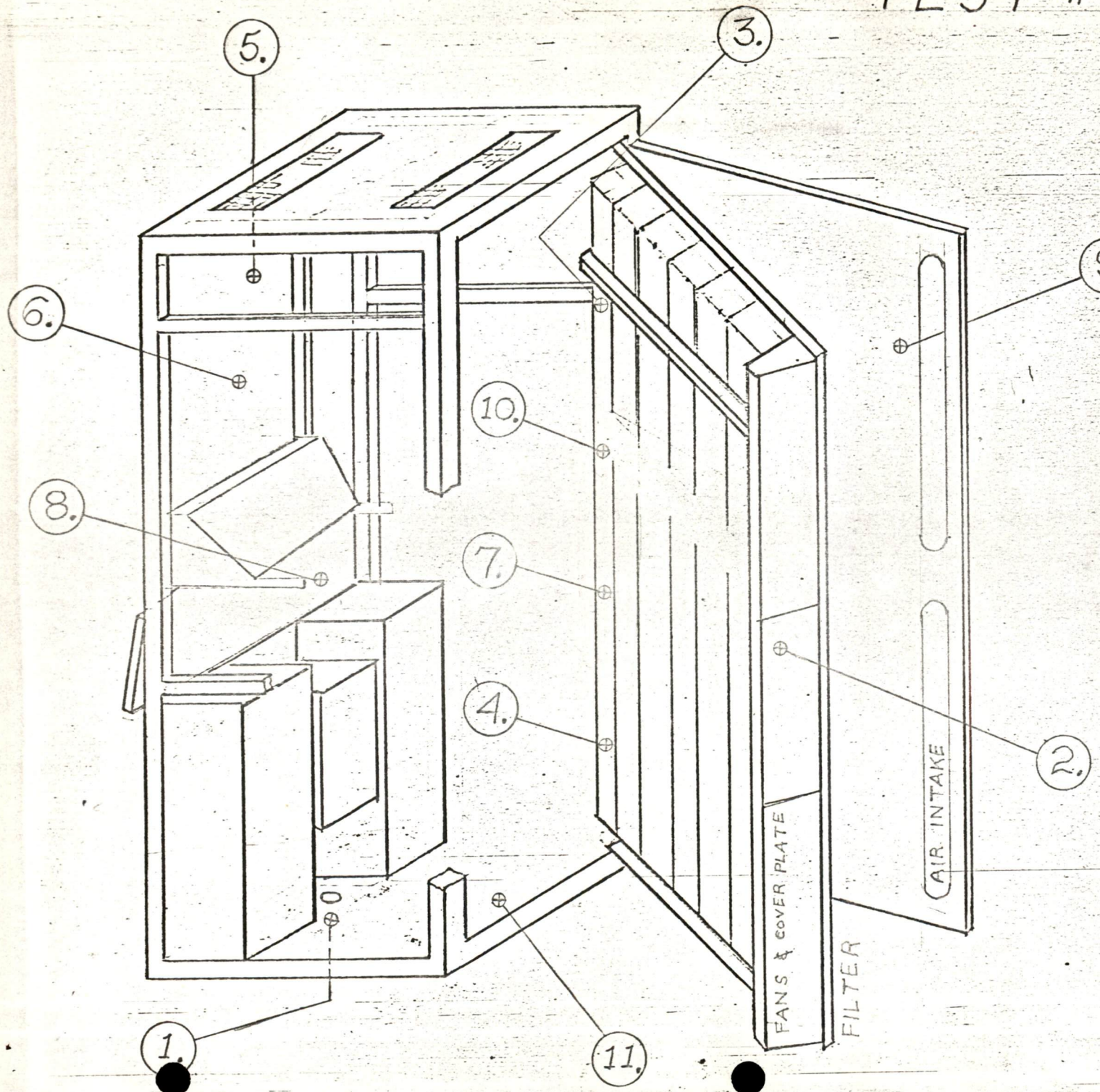
bn

PDP-9 HEAT TEST
DM 9/9/68

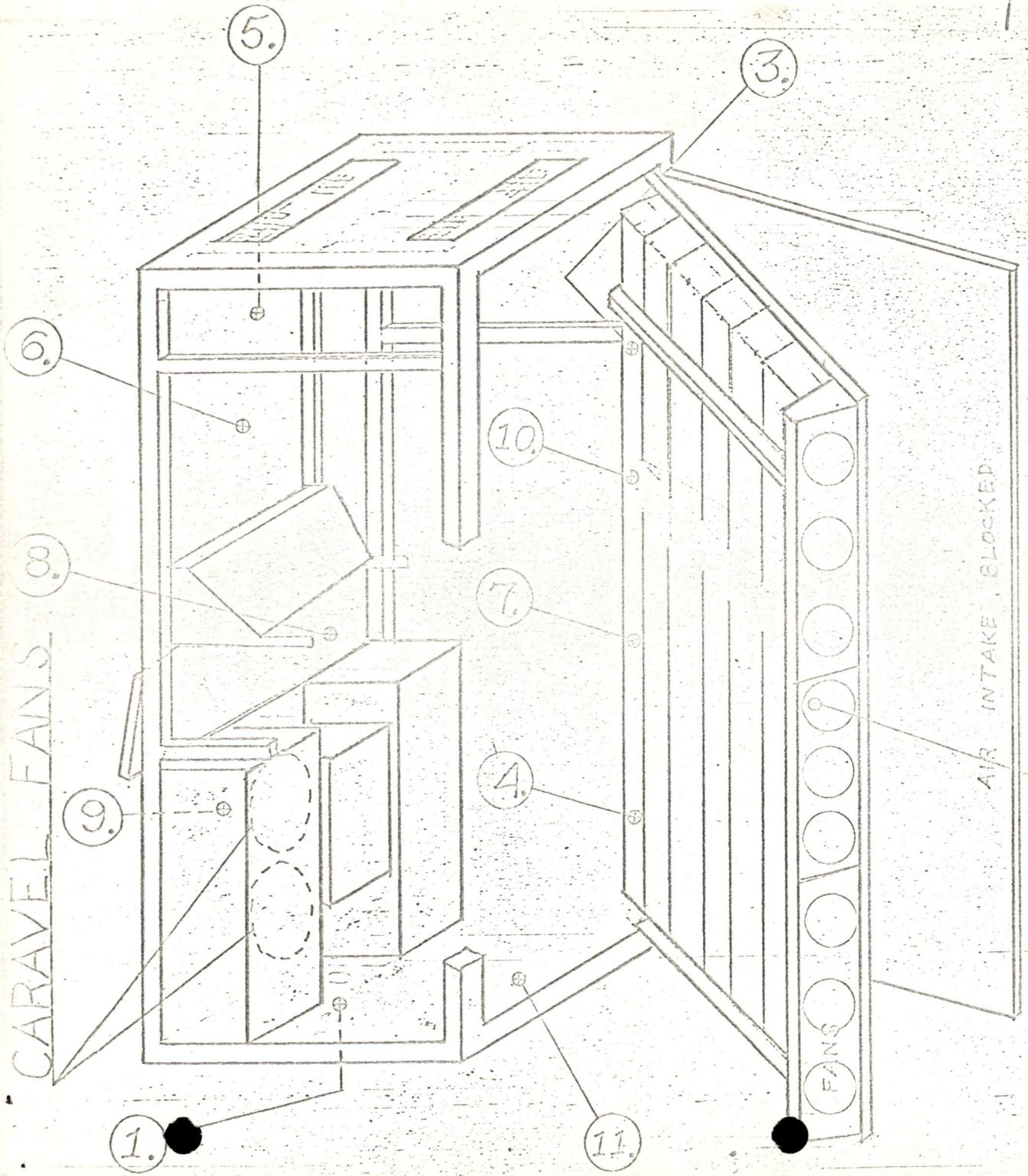


TEST #1 – STANDARD PDP-9
TEST #2 – PDP-9 WITH FOAM STRIPS
TEST #3 – CARAVELS – NO FOAM STRIPS
TEST #4 – CARAVELS + FOAM STRIPS

TEST #1 & 2



TEST #3,4



dec INTEROFFICE MEMORANDUM

DATE September 18, 1968.

SUBJECT

TO Ken Olsen

FROM Denny Doyle

c.c. Ted Johnson

Following our discussion regarding the customer complaint from the University of Sherbrooke the other day, you asked me to advise you in writing of my feelings with respect to sales administration.

I think Ted Graffe now sees the problems clearly and I feel he is going to make a major breakthrough in solving problems that have been with us for a long time. Therefore I am suggesting that you take no action on this memo, instead I would like to give Ted a few weeks and I will comment again at that time.

The fundamental problem is an unreliable communications link between sales administration and the people who provide the equipment to them, whether they be production, the product line, or field service. I have suggested that signatures be used more frequently in this chain of communications so errant individuals can be tied down.

As a second obsservation, the reprimands for overdue shipments do not appear severe enough. I've had shipments slip for over 6 months (relatively simple items like an AF01 A-D converter) and I am unaware of any being called up on the carpet about it.

I am making these comments only because you insisted that I do so. I will advise you again in one month's time if I don't feel the situation has improved markedly.

Denny

digital INTEROFFICE MEMORANDUM

DATE: 9/17/68

SUBJECT: Core Memory Manufacturing Proposal

TO: Pete Kaufmann
Dave Knoll
Joe St. Amour
Tom Stockebrand

FROM: Bill Owens

Ken Olsen
Dick Best
Henry Crouse

This is a first draft of the proposal. I need two more weeks to complete detailed cost evaluations outlined in the report. Those findings will be worked into the report at that time.

CORE MEMORY MANUFACTURING PROPOSAL

Abstract

Without major innovations and large capital expense on our part we cannot realize savings in the manufacture of core memories.

The thing we should do is look for the innovations. The major innovation would be the development of a line of memories for our small and medium size computers, all of which are made from a few standard "building blocks". By so standardizing we generate high volume parts for which we can afford to automate stringing and assembly techniques, and will give sufficient volume to warrant making our own cores.

I owe to two week study will predict in detail the savings possible through this standardization and automation. If savings look big enough then a major design effort can be initiated the purpose of which would be to:

a) evaluate and propose a automatable "building block" package.
b) design automatic equipment.

At the same time we should start a small facility to make desk calculator memories involving minimal capital investment. A detailed cost evaluation on this step needs to be completed; however, the goal here is to train the production team, not to realize a big dollar savings on DCM memories.

Finally, if the result of the "automation" design effort if favarable, then a major facility can be built on that engineering proposal, and the savings could be quite substantial.

Introduction

Core memories consist in large numbers of ferrite torroids arranged in arrays with tow, three or four fine wire passing through the center of each torroid, or core. The magnetic properties of each core are such that two stable states of magnetism are possible. The wires passing through a given core allow one to change the state of flux in the core and/or sense the state the core is in. By locating the cores in certain geometric arrays, by threading the wires in one of several definite patterns and by connecting these wires to the right electronics it is possible to : 1) select a given core in the array 2) sense its state of flux and 3) change its state of flux.

If our alphabet had only two letters then we could let each state of flux of a core represent one of the letters in the alphabet. We could store which ever letter we wanted in any core we wanted and we could go back at any time and find out which letter we had stored in that particular core. By getting a little fancier, we can find out what letters are stored in several cores at a time. That is, by working with groups of cores one can "read" or "write" words from or into the memory.

A given core memory can be fully described by specifying: 1) the number of words it can store 2) the number of letters, called bits, per word 3) the wiring pattern 4) the core material, shape and properties and 5) the associated electronics.

The following table lists the vital statistics about the core memory stacks DEC has purchased up to now.

DEC Memory History

Computer	Configuration	Core	Cycle Time	Stack Cost/bit	
PDP-1	4K×18	4w, 3D	50 mil	6 μs	8.2 ¢	
PDP-4	8K×18	4w, 3D	50 mil	5 μs	4.1 ¢	
PDP-5	4K×12	4w, 3D	50 mil	5 μs	5.1 ¢	
PDP-6	16K×37	4w, 3D	30 mil	1.6 μs	2.8 ¢	
PDP-7	8K×18	4w, 3D	30 mil	1.8 μs	1.2 ¢	
PDP-8	4K×12	4w, 3D	30 mil	1.5 μs	1.4 ¢	
PDP-8S	4K×13	4W, 3D	30 mil	6 μs	1.1 ¢	
PDP-8I	4K×12	4W, 3D	30 mil	1.5 μs	1.2 ¢	
PDP-9	8K×18	3w, 2½D	30 mil	1. μs	1.7 ¢	1966
					1.3 ¢	1968
PDP-10	16K×37	3w, 2½D	20 mil	.75 μs	1.7 ¢	

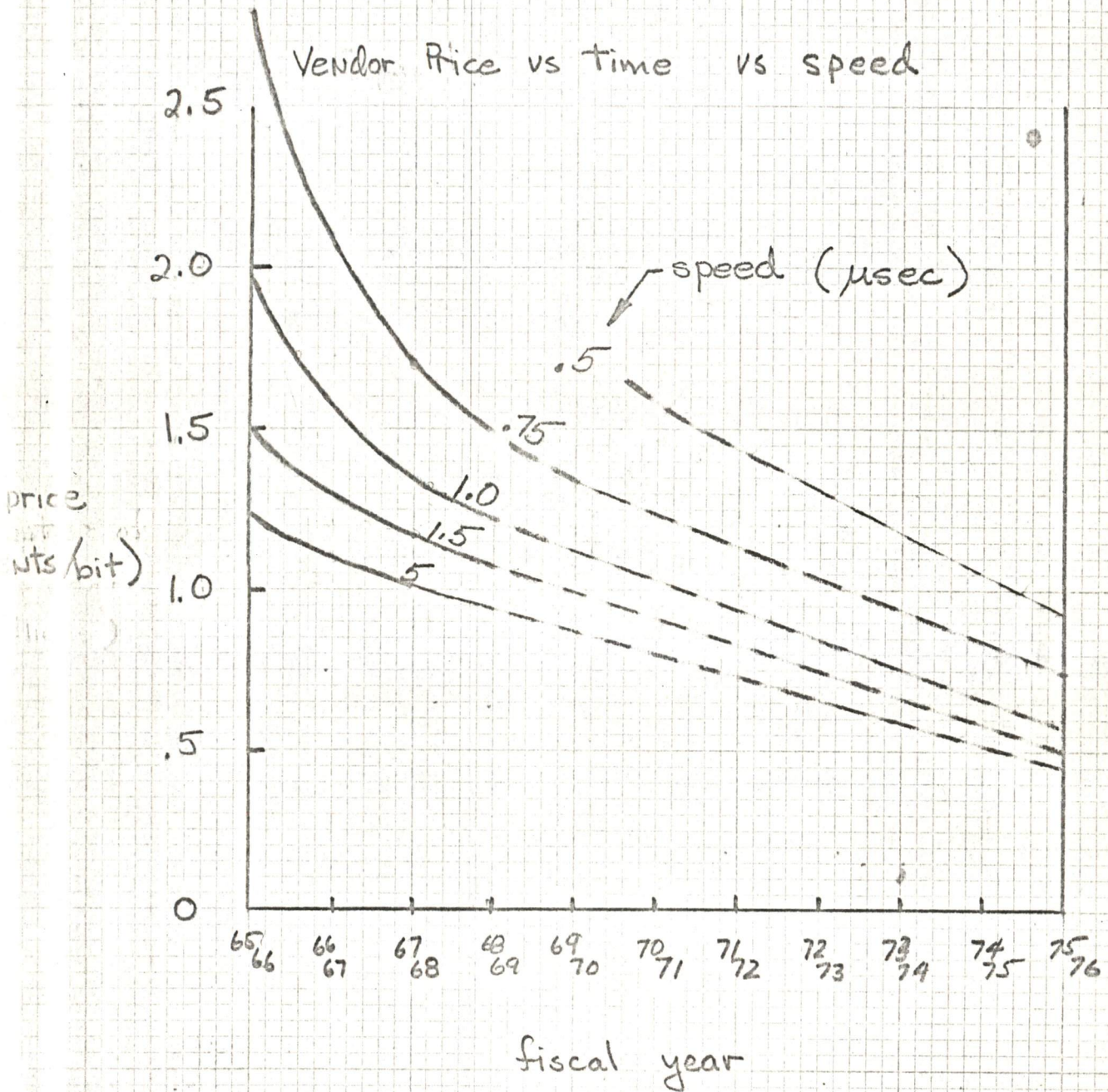

Vendor Price vs time vs speed
2.5
2.0
1.5
1.0
.5
0
price
nts/bit)
speed (μsec)
.5
.75
1.0
1.5
5
65/66
66/67
67/68
68/69
69/70
70/71
71/72
72/73
73/74
74/75
75/76
fiscal year

Figure 1

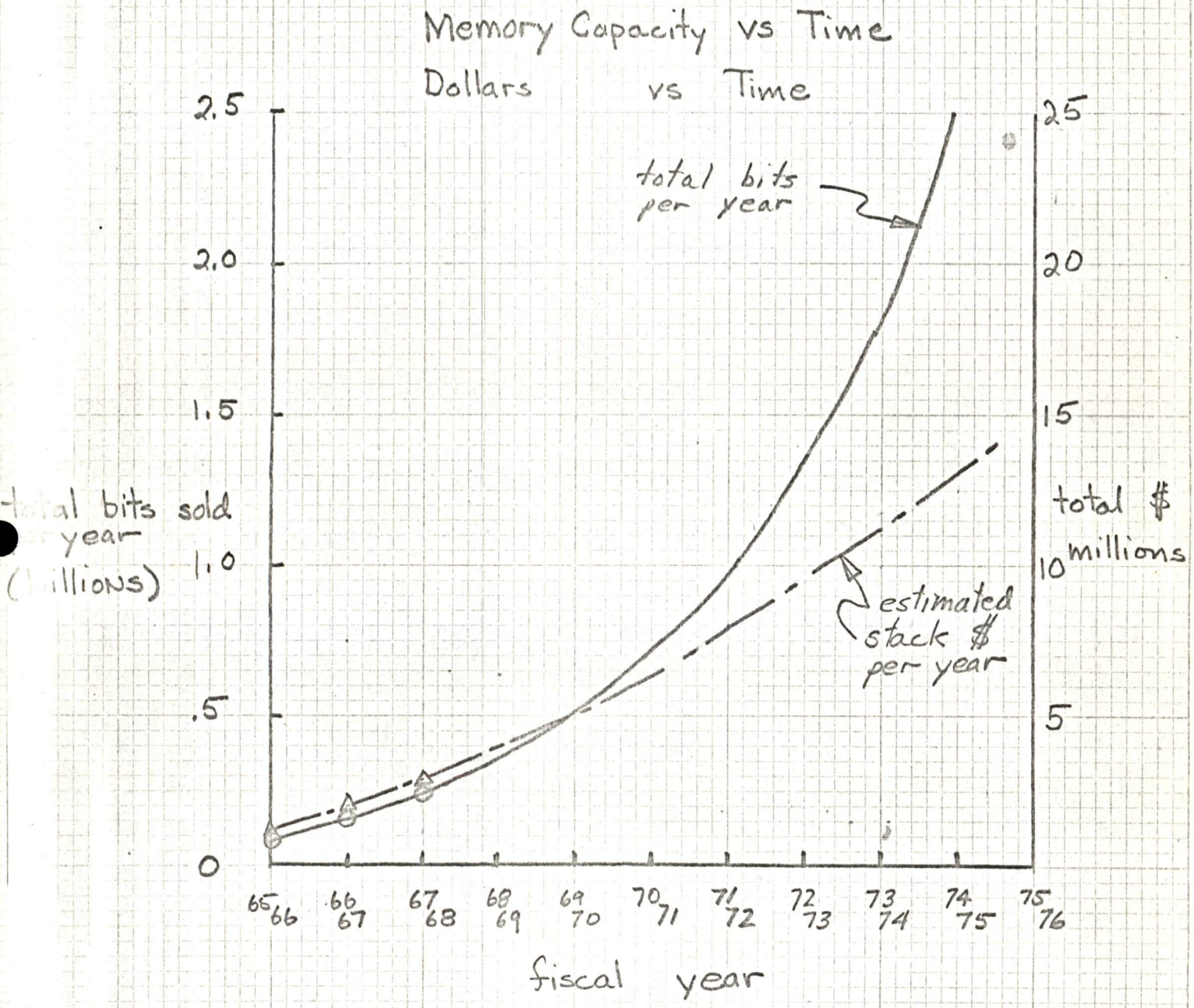

Memory Capacity vs Time
Dollars vs Time
total bits per year
estimated stack $ per year
2.5
2.0
1.5
1.0
.5
0
25
20
15
10
5
total bits sold per year (billions)
total $ millions
65 66
66 67
67 68
68 69
69 70
70 71
71 72
72 73
73 74
74 75
75 76
fiscal year

Figure 2

What do our future needs look like at DEC? In fiscal year 1965, we paid vendors $1.2 million for memory stacks totalling 60 million bits. Last year, fiscal 1967, we paid vendors $2.9 million for a total of 220 million bits. The following graph (figure 2) shows expected furture totals. This estimation shows us reaching the billion bit per year mark early in 1972, paying around 0.8 cents per bit to our vendors.

What about configuration, size, speed, etc. of future memories? The following table lists sure candidates between now and 1972. In addition, around 1972 we may start selling large mass memories (1 million - 20 million bits) of the 2D linear select type or 2½D type; although it is likely that thin film memories will be more economical in this area.

computer	configuration	core	cycletime	Volume
DCM	4K×8, 3w, 3D	30 mil (50 mil)	?	1000/yr
9I	8K×18, 3w, 3D	18 mil	800 ns	300/yr
?	1K×8, ?	?	?	?
8I	4K×12, 4w, 3D	30 mil	1.5 μs	1000/yr
8I Successor	4K×12, 3w, 3D	20 mil	1 μs	?
?	4K×16, 3w, 3D	20 mil	<1 μs	?
?	" "	30 mil	1.5 μs	?
10	16K×37, 3w, 2½D	20 mil	<1 μs	?
10 Successor	16K×37, 3w, 2½D	12 mil	500 ns	?
KI-10	4K×148, 2w, 2D	18 mil	600 ns	?
10 Successor	?	?	12 mil	<500 ns	?

Many of our future computers may have optional memories; one a fast memory using 20 mil or smaller cores and expensive electronics, the other using 30 or 50 mil cores being much slower and using cheaper electronics. As our peripheral effort grows, we will find needs for small core memories and possibly alterable read only memories. In the very small memory field (less than 1K bits) IC memories will probably be competitive in a very short while, but if not we may be making small 1K x 1 core memory chips for use in peripherals, lab apparatus, NC control, desk calculators and who know what else.

It is quite clear that our need for core storage is growing at a rapid rate and it will require considerable effort on our part to keep from paying 50 million dollars for memory stacks alone in fiscal 1975.

III. Market Outlook

In reviewing the graph (figure 2) dividing the total bits sold per year by the expected $ expenditure to vendors per year gives a yearly average cost per bit best shown in figure 3 below. The cost per bit is dropping quite rapidly at present, due to keen competition, but several important things must ~~be~~ happen to cause the price to continue to drop.

Cores: Cores are the essential part of the memory, and at present make up 30 to 40 per cent of the stack cost. Without good cores one cannot make good memories. In the past, cores were expensive. The great skill needed in ferrite powder mixing and firing, slow pressing machines requiring expensive maintainance, slow care handlers and testers, and poor yields resulting from "witchcraft-like" powers controls all contributed to the high cost. In addition core makers had very little competition and could get away with charging high prices allowing them to make huge profits. Research has brought new powder formulations which produce extremely desirable core properties and which can be fired in a consistent manner to give good yields.

Several economical high speed core presses are available now which increase by an order of magnitude the production possible from a single machine. Maintainance is greatly reduced and through improved die design yields are better. Pentronix has a very good machine on the market now which presses 60,000 cores/hour and costs $15K. Core handlers and testers have been developed and can handle up to 1000 cores per minute. Conveyor ovens are beginning to appear which make continious operation and hense better process control ~~p~~ possible. In addition core houses now have developed several reliable standard cores which they can bang out by the ~~l~~ millions. The search for new materials and techniques is continuing but ther pace can be less costly because adequate materials now exist.

Core reliability and yield may develop to the point where core vendor and buyer need not both 100% test cores. Either the seller or the buyer could test to source AQL thereby reducing costs significantly.

Cost savings due to these developments are just beginning to be felt and as new equipment gets amortized and processes become improved, core prices will drop further. New core making ~~l~~ techniques like the "cookie cutter" method being developed by Core Memories Ltd. could drastically reduce core proces in the near future. By June 1970 we will probably be able to buy 20 or 30 million cores, 100% tested, in quantities of 100 million for $1.00 per thousand. By 1975 $.50 per thousand. Figure 4 and 5 shows these expected cost trends.

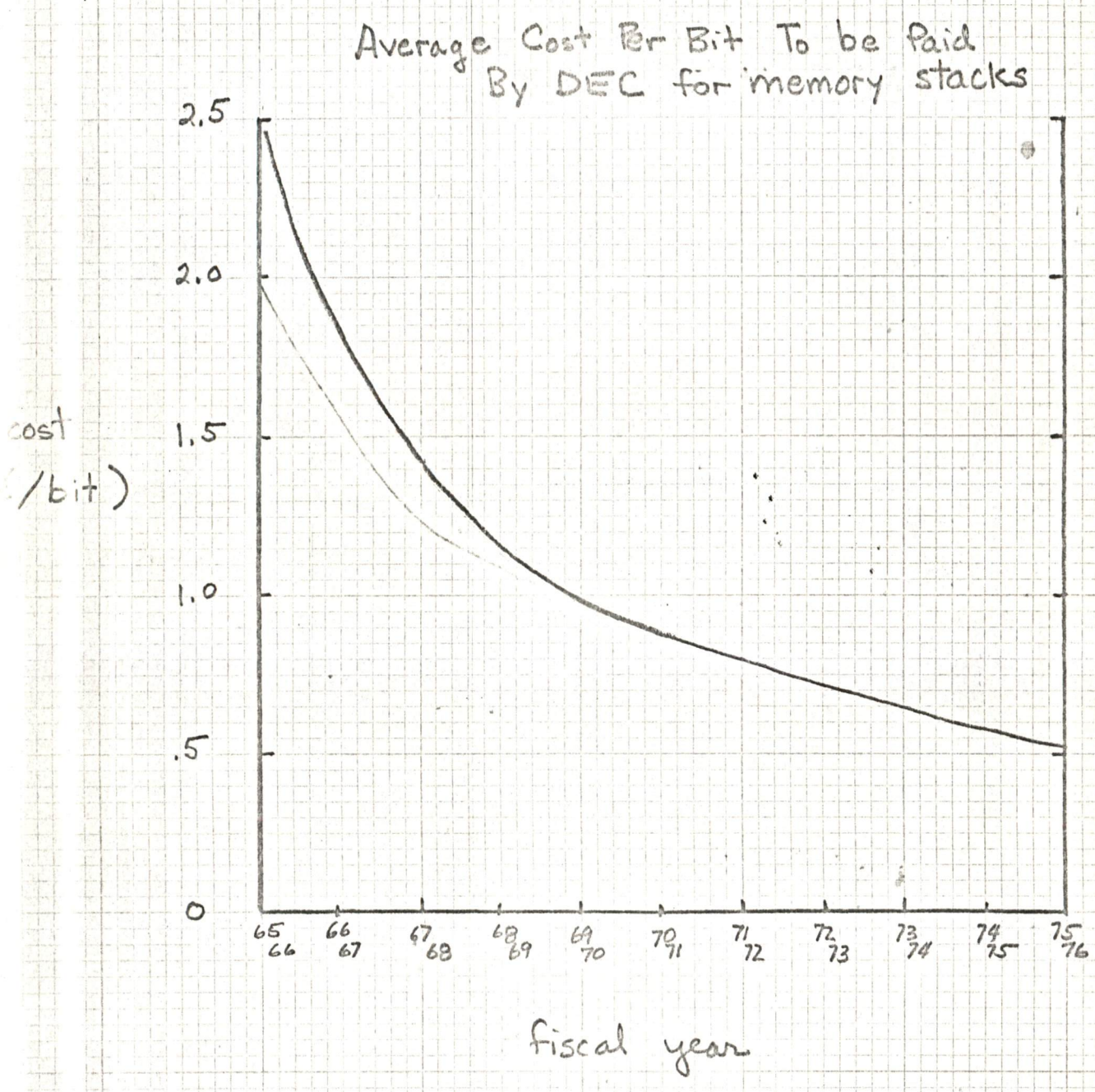

Average Cost Per Bit To be Paid
By DEC for memory stacks
2.5
2.0
1.5
1.0
.5
0
cost
(¢/bit)
65 66
66 67
67 68
68 69
69 70
70 71
71 72
72 73
73 74
74 75
75 76
fiscal year

Figure 3

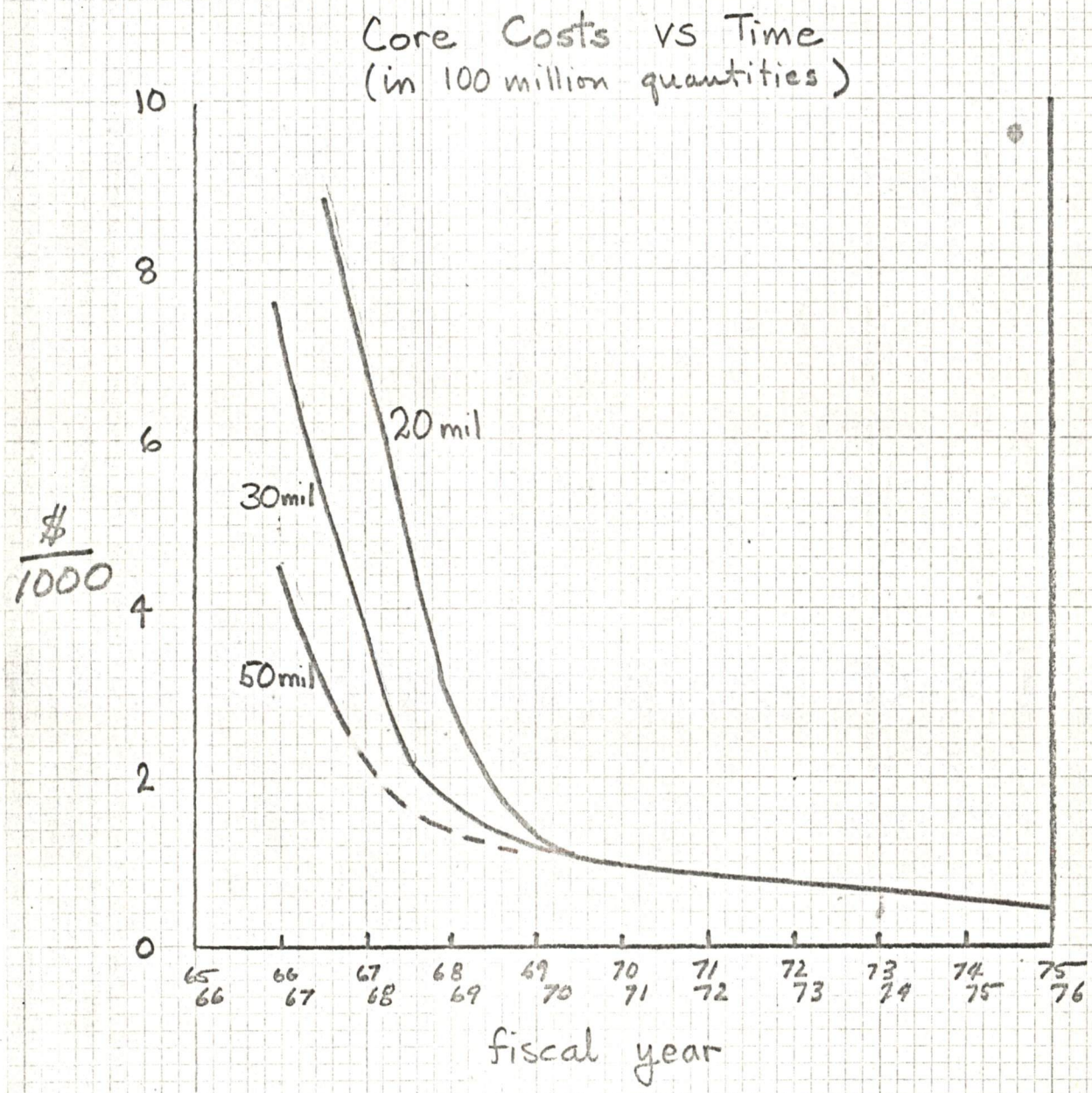

Core Costs vs Time
(in 100 million quantities)
10
8
6
4
2
0
$/1000
20 mil
30 mil
50 mil
65/66
66/67
67/68
68/69
69/70
70/71
71/72
72/73
73/74
74/75
75/76
fiscal year

Figure 4

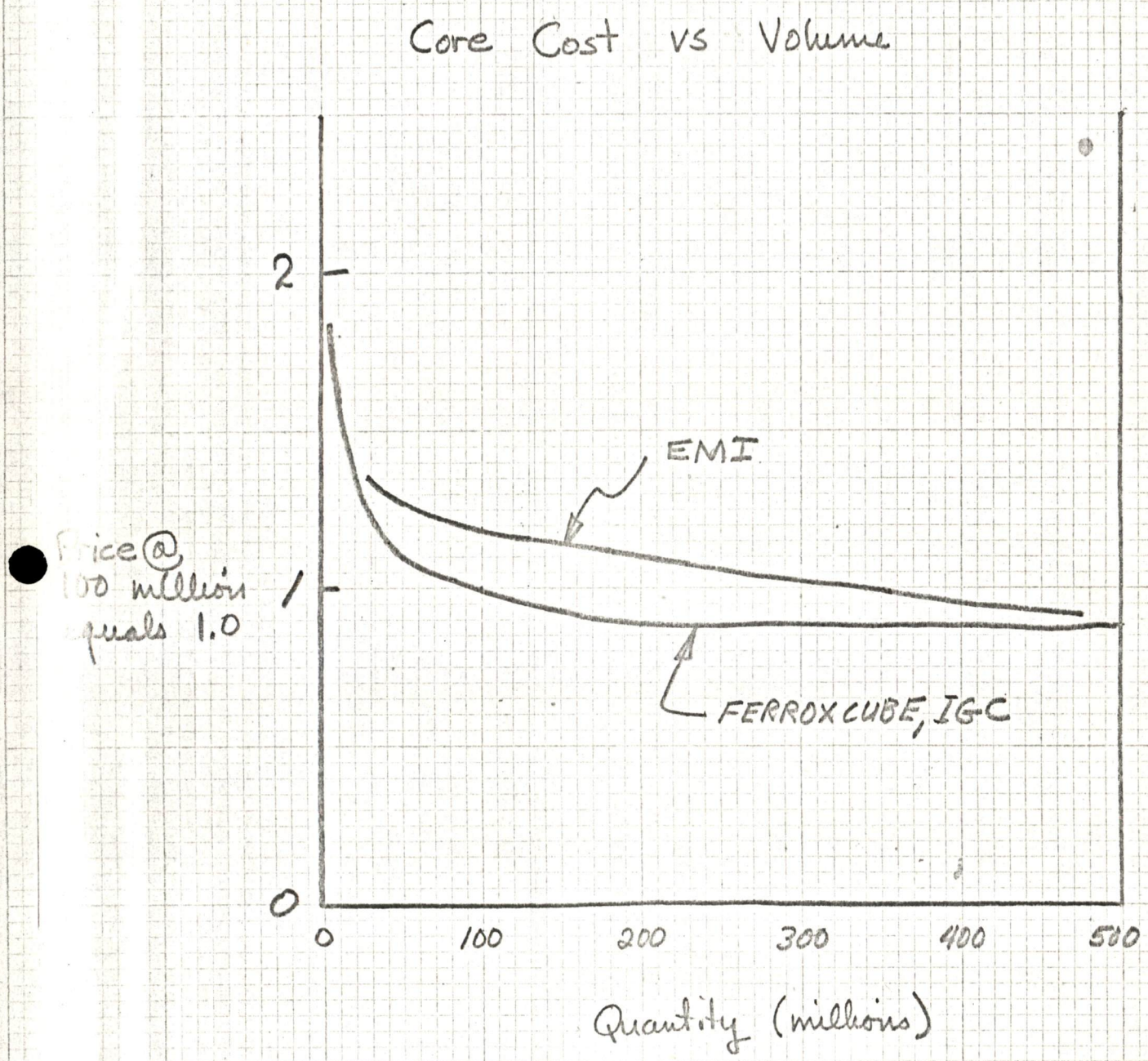

Core Cost vs Volume
2
1
0
Price @
100 millions
equals 1.0
EMI
FERROXCUBE, IG-C
0
100
200
300
400
500
Quantity (millions)

Figure 5

Demand in the market place is a very important factor in determining core prices. At present 30 mil cores are the most widely used core, and hence 30 mil cores are the cheapest. Probably even cheaper than 50 mil cores. Soon 20 mil cores will overtake 30 mil cores in popularity and the price of the two may become very nearly equal. Especially since the new core pressing and testing machines can handle 20 mil just as well as 30 mil cores.

It seems clear that in the quantities DEC needs, cores will continue to get cheaper.

2. Wire and Insullation: Several assembly and reliability problems with stacks can be associated with the wire and insullation used. Source of the problems are:

a) Cores are abraisive and can rub holes in the insulation if precautions are not taken. Usually this amounts to sticking cores to a mat or putting the cores so they con't shake around and secondly lubricating the wire to reduce abrasion during stringing. Still, magnetostrictive motion of the core can wear the insulation.

b) Insulation is thru and has some permeability to moisture. Result is on migration from wire to wire in humid climates, ie. corrosion of the wire.

c) Wire is so small in deameter that when solder joints are made, great care must be taken to see that the wire does not completely go into solution with resultnat deterioration in joint strength.

d) Wire lacks strength to the degree that a needle must be used to thread the cores and once threaded the wire does not lay flat making subsequent stringing more difficult.

Improvements and new techniques in these and other areas related to wire and insullation could reduce overall stack costs significantly.

3. Everyday some new technique for mounting cores, for fixturing during manual stringing, for making joints, and for stacking core planes comes into being. The objective of all these new approaches is to reduce the labor envolved, but often times reliability and repairability are improved sumultaneously. The trend seems to be to planes comes into being. The objective of all these new approaches is to reduce the lobor envolved, but often times reliability and repairability are improved simultaneously. The trend seems to be to planar designs, such as our DCM memory, which eliminates stacking. The effect being lower manufacturing cost and greatly reduced repair costs since all cores are exposed, and probably increased reliability through a reduction in number of soldered joints.

4. A big factor in memory stack cost is the training of oversea's labor forces and setting up and debugging of facilities there. Practically all major memory stringers (Ferroxcube being a notable exception) have large operations in low wage areas. These facicilities have been under development for the last three to five years and their real savings are probably just now beginning to be felt. For example, 3 years ago EMI started a plant in Hong Kong. One of their first steps was to try and make cores and they had a lot of trouble--this slowed them down. Now all of EMI's high volume work is done in Hong Kong. EMI has also found a very stable, skillful and maderatly inexpensive work force in Utah. Medium volume jobs are handled there. Only prototype and quick turnaround work is being produced at EMI's main plant in California. I think all their cores are made in California. The point is, these large labor forces are well along the learning curve and are becoming effective cost reducers.

5. & 6. The only way core memories will ever reach a projected average cost of 1.¢ per bit by 1970 and .5¢ per bit by 1975 will be through the combination of standardization and automation.

IBM presently makes core memories for 1/3 of a cent per bit. They are able to do this by standardizing on one core array and stringing pattern, and spending the money for tooling of automatic stringing and soldering equipment. Thus labor costs are cut by two orders of magnitude over present domestic stringing costs. Core costs are low because of standardization on one high volume core. Testing costs are reduced since only one core plane type needs to be tested.

Ferroxcube on the other hand has a room containing about ½/ ¼ of a million dollars worth of plane and stack testing fixtures, most of them obsolete.

In order for our vendors to reach the low predicted prices they will have to pick certain standards and we will either have to live with them or provide high enough volume to allow them to change their standards to suit us. This is already beginning to happen.

At the moment 30 mil cores are the industry standard because that's what everybody wants . A product like our DCM memory would possibly be quite happy using 80 mil cores, but we have to use 30 mil cores because they are cheapest. If we could buy 80 mil cores for the smae price as 30 mil cores we sould do it (for the DCM) because they're easier to string. The ultimate memory cost would be lower.

to string. The ultimate memory cost would be lower.

* Another example is the 8 I stack. The low cost obtained on this stack is due in part to the high volume and in part to the fact that our vendors make very similar planes (if not stacks) for their other customers.

In order for vendor prices to drop as predicted we must supply them with sufficiently high volume work, or we must comply with their high volume standards, so that automatic tooling can be used. If a high degree of automation cannot be accieved, memory price probably will not drop much under 1¢ per bit on the average; and we'll end up spending $50 million instead of $15 million for memories in 1975.

7. One last factor affecting prices is overhead due to research. Memory makers are looking for new core formula"s, they are exploring their films and in limited ways offer new technologies. All of these efforts cost money and must for the next few years be subsidized by the core memory business. Competition in core memorie will help keep this research overhead to a minimum. Bit it will be at least 3 to 5 years before these new techniques can stand on their own; the money has to come from somewhere.

B. When speaking about vendors there is more to consider than the price they quote. lAt the moment we are having quality problems with memory stacks for the 8 I, 9 and 10. Certain vendors seem to have greater problems than others; but all have some quality problems. These quality problems are costing both us and our vendor money. So even though stack costs will drop in the future, it is important to question whether sufficient vendors of quality stacks exist to satisfy our needs. If we think we have problems now with

1) qualifying vendors
2) meeting delivery dates
3) field failures
4) repair turnaround time

these problems will be an order of magnitude greater in 1972 when our business is 5 times as big.

C. There are several new memory technologies around these days and others are sure to develop. It is fascinating to learn about these new ideas (some aren't so new, being in development stages for years); hovever none appear to be able to threaten the economy of core memories for at least five years, except possibly in certain areas. For example, if plated wire technology can have a few small breakthroughs we could be seeing PDP-10 like memories appearing in plated wire form within a couple of years. If the breakthrough ever comes, plated wire memories will be tough competitors because they lend themselves very well to automated fabrication. Their film memories and permalloy memories are in the same boat.

Integrated circuit memories of small size (less than 1k bits) will probably be more than competitive by 1972; however, none of these new tecnologies will threaten the core memory in the main

conputer memory market for at least the next 5 years.

D. It is quite possible that these new technologies will take much longer to develop than expected. The presen5 and coming years see spending on graduate research dwindling, government spending for research in aerospace and electronics will be traded off to defense spending and social spending, pollution research, etc. In industry increasing competition will force cutbacks in research spending. The money necessary for doing the basic development work may not be available.

IV. How can DEC save meney?

A.&B. The manufacture of a core memory consists ofseveral steps:

core making
1) mix ferrit powders
2) press cores
3) fire cores
4) test cores
5) load cores into stringable array
6) make core mat

plane stringing
7) string X-Y wires
8) terminate X-Y wire mat
9) string 3rd and 4th wire & terminate
10) visually inspect & repair plane

plane testing
11) test plane
12) repair plane

stack assembly
13) make diode boards
14) assemble diodes into boards
15) test diode boards
16) assemble stack

final test
17) test stack
18) repair stack

Certain of these steps are expensive and/or difficult even for the vendor to do. Others are easier and in some instances require little capital equipment. Lets discuss the various steps starting with the easiest form DEC's point of view finishing with the hardest.

1) The eaisest thing for DEC to do would be to make the mats and diode boards in our etch board facility. We are tooled up for high volume runs of etch boards and could probably make these parts for helf of what it costs our vendores to make or buy these parts. Our vendors do have printed circuit facilities but they are about 1% the size of ours. Because of this we already supply diode boards, assembled, to our vendors.

2) The next easiest and cheapest things for DEC to do in the process would be to assemble wired planes and diode boards into stacks. This can require very little tooling if any, but could easily be developed into an assembly line operation likemodule assembly. However, our girls in Maynard could not mek this operation cost competive with our vendor operations over seas. Our only hope would be to design stacks that could be automatically assembled, and spend time and money developing the assembly operation that our vendors con't afford to spend. This requires high volume.

Core loading is also easy to do requiring small capital equipment (about$1K). But it is of course useless to do loading without stringing too.

3) Pland & Stack Testing is the next easiest thing for DEC to do but requires consideralbe capital equipment. However, we have many people here who are familiar with the design and use of such equipment, and a supply of good technicians to run the machines. Plane & Stack Testing is an area where our vendors are particulary weak. Not only must they keep on hand large varieties of test fixtures to handle all of their various customers different

TABLE

	$250K or $50K/year			$450K or $90K/year		
Capital Investment 5 year amortization						
Labor						
Staff	2 @ $38K/year			5 @ $ 90K/year		
Shift Labor (1 shift)	7 @ $70K/year			20 @ $200K/year		
	1 shift	2 shifts	3 shifts	1 shift	2 shifts	3 shifts
Cost/year	$158K	$228K	$298K	$380K	$580K	$780K
Production (60% yield) Core Volume Year	70 million	140 million	210 million	400 million	800 Million	1.2 billion
Cost $/1000 cores	$2.26	$1.63	$1.42	$.95	$.73	$.65

configurations, but it is difficult for them to perform tests which will garauntee a working stack in the customer's system. We now have to ship our vendors testing systems for some of our stacks. We thus save our vendors money by not vasing their time with meaningless tests and repairs. By doing the testing ourself we would gain by

a) not having to build many testers to ship to vendors
b) performign meaningful tests in minimum time
c) greatly shorten repair time by finding the right mistakes
d) shorten overall turn around time by finding out about basic stack faults sooner. Ideally this means we ship computer with fewer delays.

4) Plane stringing and wire termination require much less capital equipment than does pland and stack tesing, however a high degree of skill on the part of the stringer is necessary in order to do this jkob economically. It is doubtful that we at DEC could ever manually string planes cheaper than our vendors. We would definitely have to look to a low wage area. But our vendors are much farther along the learning curve than are we. The best we could probably ever do on manual stringing is break even.

5) Core making and testing are the hardest chores requiring the most capital equipment. The following table gives estimated costs of various volume core making facilities we might invest in. The $250,000 investment could make nost efficiently only one size core out of one material. The $450,000 investment could make as many as three or four core sizes out of one material without sacrificing efficiency. The low dollar investment facility is inefficient because the materials preparation equipment firing furnaces are not being used anywhere near their capacity, whereas other equipment like core presses and testors (only 1 each) are being used at their capacity. Adding more presses and testers up to the 450 K figure greatly improves the operation efficiency while also allowing a varieyt of cores to be made instead of just one.

C. Importance of Standardization

1) By standardizing on a few basic parts for memories (like one basic core plane and wiring configuration for all samll and medium size computer memories) we can achieve high enough per piece volume to afford development of highly automated fabrication and testing schemes (recall this is how IBM makes memorie for 1/3¢ per bit)

2) By pulling sufficient memory volume in house we can afford to invest in core making which can net substantial savings since a large and increaing fraction of memory costs is in the cores.

D. Summary of Introduction and Market Survey

Two essential points have been made up to now. (1) Our vendor's core memory prices are dropping and will continue to drop. We can make rough estimates of their prices, but much depends upon the ability to come up with high volume parts which can be automatically fabricated. (2) The second point is that we do inhouse manufacturing of memories using only conventional techniques we can't really expect to do much better than equal our vendors manufacturing costs. In fact if we don;t make our own cores we can't even expect to equal their costs.

Our average memory vendor's manufacturing costs are about 65% to 70% of selling price. (Direct labor amounts to ¼ of the manufacturing cost, material ¼ and overhead ½.) (The vendor's research and development expenses probably amount to 5% to 10% of selling price.) In contrast, DEC's manufacturing cost averages about 40-50% of selling price. This means that unless we can beteer our vendors cost by 20%, we shouldn't waste our labor force in this endeavor. There are more profitable places for our efforts. There are circumstances which might out weigh this loss in "productivity":

1) Vendor quality might be poor and I think we could improve on it because of our large brain pool.

2) Vendor volume simply might not be large enough.

So we don't belong in the state of the art memory manufacturing business unless we can find nothing more profitable for our people to do, or unless our vendors really do fail to perform.

TABLE

Company	Sales	CGS	SGA Expenses		Net Income after taxes
Cenelco (Ferrosubs)	100%	73½%	17%	2/3%	4%
Data Products (CM Ltd.)	100%	68½%	15%	7½%	4.2%
Fabritek	100%	81%	26.7%		Loss of 7.5%
EMI	100%	76%	14.2%	—	5½%
[illegible]	100%	75%	15%		4½%
DEC	100%	49%	19.2	10%	21%

V. What Should We Do?

We need to attack the engineering problems first spending two to three weeks evaluating in detail the "building block" idea whatever it is to see if large cost reductions really are possible; and spending a forth week evaluating in detail the DCM proposal below. Then, if the savings appear to be there, we should start two efforts:

1) A major design project responsible for coming up with the "basic building block" package. Electrical designs, packaging designs, and "automation" designs must be evaluated simultaneously, ending in a complete design and proposal to build.

2) Coincident with the above effort we should start buying cores and assembling from scratch DCM memories. The purpose of this is not to develop a state of the art memory production facility. Instead, the reasons for doing and manner in which this should be done are:

a) The main reason for starting state of the art process is that when automatic stringing does come, we will still possibly need experienced stringers to string 3rd wire and to do repairs.

b) Only small capital need be purchased. The most expensive item being the core tester which we can probably pick up second hand. A very inexpensive exercisor can be used as the memory tester. Total capital equipment needed $100,000. People to do the job can come from within Maynard plant.

c) The DCM memory is such that we might actually be able to make a savings on it. (ie. it is very simple and we're good at simple things)

d) It will allow us to become familiar with core vendors and their problems.

e) It will score our present memory vendors and might induce some extra needed effort on their part.

f) It might prove after all that we can use state of the art techniques to advantage and worthwhile savings.

g) Fastly, the operation gets a foothold in the company, training takes place, channels get developed, so that when the automated design is ready to go the working force will be all ready.

The options here are many. If automatic stringing evaluation says no go, we don't have a lot of money tied up, The operation still might be a success, and at that point in time it can either be shut down, continued or expanded depending upon the

situation. On the other hand if automation is "go" in a big way our start up time can be greatly shortened. Probably by 1970 we will be spending a half a million dollars a month on memories. The loss for every months delay getting the 7ØØ "big" facility on line could cost $100,000, well worth the initial $100K investment. If the "big" automated facility is go we will surely wnat to chedk core prices at the time, and seriously consider making our own cores.

So that's the plan.

1. Two week study.
2) Detailed design proposal (3-6 months)
3) Start small DCM memory production.
4) If word is go; build "big" facility.

So what's the plan. During the next two weeks I plan to predict the cost reductions possible through automation, and will give a detailed estimate of what it will cost us to set up for and make DCM memories. The time table looks ¢¥¿¥¢/¢¥/ like this:

TABLE

Sept 18 – Oct 2	1968	Preliminary cost evaluation (W. Owens)
Oct 2 – Oct 31	1968	Discussion period
Nov 1 – Apr 1	1969	Complete design project *
Nov 1 – – –		Get small production facility started
Apr 1 – September 1	1969	Fabricate automated machines and set up facility
Septo 1 – Dec 1	1969	Get automated facility on line
January	1970	Volume production using automated facility

digital INTEROFFICE MEMORANDUM

DATE: September 18, 1968

SUBJECT: Status of new and continuing developments.

TO: Ken Olsen ✓
Pete Kaufmann
cc: Ed Schwartz
Henry Crouse

FROM: George Wood

COMPANY CONFIDENTIAL

Relative to plating memory discs, the Sel-Rex salesman is sending me all the current literature on this subject. He tells me that people like Honeywell, IBM, and NCR are doing this now and are very secretive about their process. He did say however, (based on past experience) that if I were to come up with a process, Sel-Rex is in a position to design and build equipment that would plate the product the way it has to be plated in order to work. Note; I think what he's saying is, "I can't tell you what somebody else's process is by way of disclosure, but I can build you a piece of equipment that will work and you can go back from there to find out what the process is." Will keep in touch as things develop.

Relating to the plastic module, there have been some interesting developments. We are now in the process of cancelling our order with the molder. While we were in this phase of our contract, their salesman brought to Photocircuits (recently purchased by Buckbee Mears) a molded quad panel with our name and handle configuration. Yesterday Photocircuits area representative brought that part in, all plated with copper, stating;

1. They came across this by accident and didn't go looking for it.
2. Other people in the industry are also working on the same idea. (IBM strongly implied.)
3. They have been working independently with Union Carbide on an arrangement to preseed polysulfone.
4. They don't think polysulfone is the right plastic.
5. Preseeding will give better adhesion on almost any plastic.
6. They claim to have patent rights that cover the deposition of copper on any surface (Union Carbide may be violating their patents).

Based on the above, they would like to further their knowledge and development in this field. They are proposing we get together in this venture. We offer an existing mold and our experience to date, they offer their technology and I think the major portion of the development costs.

They will contact me again about October 15, 1968 to further investigate our interest. I suggest we have nothing to lose in talking, what happens beyond that will depend on the nature of the agreement.

Please give me your thoughts.

George

mm

dec INTEROFFICE MEMORANDUM

DATE September 20, 1968

SUBJECT UNIFORM RENTALS

TO Pete Waldron
cc: Henry Crouse
Lon Beaupre
Dan Sullivan
Al Hanson
Pete Kaufmann
Ken Olsen

FROM John Trebendis

Let us do something about our uniform rentals from Interstate Rental Company. There isn't a week that goes by that there aren't many, many complaints, such as, no pants, no shirts, or no clothes at all.

I have had men that do not receive their allottment of clean uniforms for weeks at a time. In every instance where the man does not receive his clothing, we are still charged for that rental. As many times as we complain about the deplorable situation, things will run smoothly for a week or two and the revert back to the same deplorable condition.

We have had many men that left our employ that had uniforms; and in almost every instance, we have asked that these names be dropped from the uniform list. If we are not careful and do not check the list every week, we find these names back on the list.

Even when our men go on vacation and no uniforms are used, we are still charged.

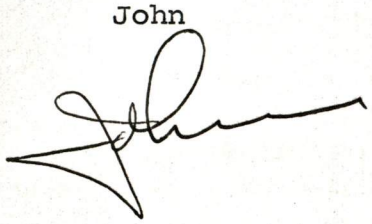
I suggest that we either drop these people completely or go to some other system; but if we look into this, I think we will find that every uniform rental company is the same.

As a suggestion -- Why don't we, Digital Equipment Corporation, purchase the prescribed sets of clothes required for our men? (In some cases five sets and in other nine sets per man). If we purchase these clothes outright and issue them to the men, we could have their wives or families launder them. I think that we would find the appearance of the men would improve, and it would be cheaper for us in the long run. As it stands now, we pay roughly $3.00 per man per week. At this rate, we are paying over $150.00 per year per man.

We could go into a no-iron dacron fabric that would easily be taken care of. I have looked into this a little bit and found that for less than $10.00 per set or $50.00 per man for five sets, we could outfit our people. If we look into this deeper, we could probably better this price even more so.

Any comments or suggestions you may have on this matter would be appreciated.

John



digital INTEROFFICE MEMORANDUM

DATE: September 23, 1968

SUBJECT: Talk at Maynard Community Chest Lunch on Thursday, September 26.

TO: Ken Olsen

FROM: Dimitri Dimancesco

Attending the luncheon will be members of the ten organizations which belong to the Maynard Community Chest, the Maynard Selectmen, leaders of the forthcoming drive, and the local press -- probably a total of about 30 people.

May I suggest the following outline for your talk.

A. A quick description of Digital's growth contrasting our early beginnings with our present size. (Total employment is now 2,879 of which 2,144 are located in Maynard.)

B. Some comments on the considerable use Digital employees get from the participating agencies. For example, over 100 cases involving Digital employees or their families handled by Emerson Hospital annually. See attached information on the agencies.

C. Praise for the Maynard Community Chest and for its organizers. Possibly a statement as follows, "Digital appreciates the services your agencies provide. In the past we have made corporate contributions to each of the agencies. We now feel that we can be of further help to you by encouraging our employees to participate in your campaign. I hope that other local organizations, the local business community and all the townspeople of Maynard will actively participate in your forthcoming campaign."

Dimitri

gm

MAYNARD COMMUNITY CHEST

Purpose: One appeal in place of ten assures low-cost fund-raising and an efficient administration. More dollars are put to work serving the people of Maynard and the best possible use of valuable time and energy of agency personnel is assured through the single annual Community Chest.

Member Agencies:
Girl Scouts
Red Cross
Emerson Hospital
Salvation Army
Walden Guidance Association
(treats mentally disturbed children)
Boy Scouts
Concord Family Service
(provides assistance for all kinds of family problems)
Mental Health Association
(assistance for adults)
Minutemen Association for Retarded Children
Assabet Valley Little League

Maynard residents were served 1,900 times in calendar 1967 by agencies and services of the Maynard Community Chest. The types of services most often used by Maynard residents were hospitals, youth agencies, and family services. Emerson Hospital provided the most units of service - 950. Other typical organizations and the number of persons they served included the Assabet Valley Little League - 400, Algonquin Council of Boy Scouts - 225, Girl Scout Council - 240.

The Maynard Community Chest was just organized. And its first fund drive will start September 30.

All of the member agencies received corporate contributions from Digital last year.

digital INTEROFFICE MEMORANDUM

DATE: September 24, 1968

SUBJECT: Reclassification to Engineer

TO: K. Olsen

FROM: G. Thayer

During the past month the Engineering Review Board has prepared the attached definition of those characteristics upon which all candidates being considered for reclassification to engineer will be assessed.

The Board would appreciate your reviewing this material and making any comments, corrections, or changes you feel are appropriate, so that we can begin to review candidates.

I have also attached, should you be interested, the procedure which was previously reviewed and approved by the Operations Committee. This will be given out to all engineering managers for their information and guidance.

GAT/lw

DEFINITION OF QUALIFICATIONS

for

RECLASSIFICATION TO ENGINEER

The following definitions outline those characteristics upon which the Engineering Review Board will evaluate all candidates being considered for reclassification to engineer:

1. Basic Knowledge/Technical Competence:

A candidate must have a knowledge of basic general engineering subjects, and have demonstrated that he can apply, and use meaningfully, these principles in areas related to his field of specialty.

He must have demonstrated his ability to be "a master of his trade", in addition to being a "jack-of-all-trades".

The application of general knowledge, outside of the confines of a limited field, is the trademark of a good professional.

For example, a logic design engineer must be thoroughly familiar with Boolean algebra, Karnaugh maps, synchronizers, registers, race conditions, logical delay, hazards, flow charts, synchronous and asynchronous logic. In addition, a logic designer must have a working knowledge of the related fields of circuit design, system design, transmission drive theory, and programming. (A programmable device designed by a non-programmer usually shows it.)

A crack logic designer who cannot evaluate a circuit as other than a "black box", cannot understand the subtle limits of the circuit as it applies to his logic when a specification may be incomplete. Likewise, this same individual must have a "feel" for the mechanics of modules, connectors, wiring difficulty, cabinet mounting, etc.

2. Creativity/Objectivity

Creativity is a "magic" characteristic, extremely valuable when correctly used, worthless when improperly used. In its more glamorous definition, it is the ability to bring into existance, through imagination and skill, the first representation of a particular form, be it hardware or software.

In a more practical engineering sense, it is the ability to understand when problems have more than a single solution; to be able to generate a number of alternate solutions; and to be able to objectively evaluate and combine these alternatives to select the one best solution for a set of circumstances. Implied is the ability to conceive and develop new and unique ideas and the discipline to reject these same ideas if they do not provide the optimum solution to a problem.

This ability to generate and accept new ideas, the ability to combine, to simplify, and to reject when necessary are critical for engineering success.

Many so-called creative people stifle themselves and their good ideas by becoming enamoured with the first unique solution that comes into mind. They are unable to reject, simplify, or accept critique that will help make for success. They tend to like complicated solutions for simple problems and must be taught that creativity, to be of value, must produce useful results.

3. Communication Ability

Perhaps one of the most important attributes of an engineer is his ability to communicate with others. Indeed, all facets of an engineer's job require some form of communication with people. In the conceptual design phases of a project, the engineer must research information prepared by other engineers, make notes, and prepare a project proposal. He must be able to clearly present his ideas for consideration by others. When he begins the actual design, he must prepare legible and reasonably organized sketches for the drafting department. He must help the draftsman organize the prints in an easily readable form so that the production department may order parts and construct his design. The engineer must prepare purchase specifications for special parts and converse with parts vendors.

When the design is complete, the engineer must prepare an overall equipment description which will be used by the publications department to prepare a manual. Often, this equipment description will be used directly in lieu of a manual. If the engineer's work is pure research not intended to produce

a finished product, he must be able to summarize his work in a paper clearly stating his experiment goals, procedures and results.

Every piece of work accomplished by an engineer is culminated in some major piece of communication in one or more disciplines. This communication ability must also be accompanied by sincere belief in its necessity and an inherent understanding that without a continuous, conscious effort to do adequate, accurate documentation at all project phases, his project will most likely fail to accomplish its objectives.

In summary, a candidate for change of classification to engineer must demonstrate in his actual performance the ability to execute clearly and willingly the following kinds of documentation:

engineering notebook
equipment log keeping
project proposals
drawings and sketches
schedules
cost estimates
purchase specifications
equipment checkout instructions
equipment descriptions and operating instructions
experiment descriptions and conclusions

In addition, the candidate must demonstrate an ability to pass on to company personnel verbal instructions and information in a cordial but effective manner.

4. Leadership

A minimum standard of leadership is that the applicant possess those qualities necessary to adequately direct the work of assistants. He should be able to reasonably assess their technical competence, assign their work accordingly, and evaluate formally their technical progress. He should be somewhat sensitive to their personal traits. He should also have demonstrated his ability and willingness to teach needed technical skills.

5. Personal Characteristics

A) Self Improvement Initiative:

Here we are concerned with what the individual has done, on his own initiative, to improve his ability to contribute in the engineering community. Included for review will be items like the following:

1. Formal educational programs or courses completed and/or now underway.
2. Participation in professional societies or related activities that would broaden his technical frame of reference and keep him current on new developments.
3. Familiarity with current literature in his field of specialization; journals; trade papers; etc.
4. Technical papers that he may have written and/or presented to engineering groups or societies.

B) Growth Potential:

Growth potential is the ability that the individual has to assume more responsibility and handle increasingly sophisticated technical problems. It is important to assess the candidate's ability to continue his professional growth. As a general rule, unless the candidate can grow at the rate expected to a recent graduate engineer for at least the next 2-3 years, it is unlikely that he will be capable of keeping up with today's fast moving technology.

C) Maturity:

Maturity is the demeanor and attitude which reflects the ability to interface effectively with people, thus permitting him to achieve his engineering objectives with a minimum of conflict. In assessing this trait in an individual, the Board will consider such factors as his ability to evaluate critically his own contributions; to accept constructive criticism from others; to approach his responsibilities in a serious-minded and professional manner; to conduct himself properly in his relationship with both professional and non-professional employees; etc.

digital INTEROFFICE MEMORANDUM

DATE: June 19, 1968

SUBJECT: Reclassification to Engineer

TO: Operations Committee

FROM: Personnel Committee
(G. A. Thayer)

The attached proposal covering reclassification to engineer has been reviewed and approved by the Personnel Committee and is forwarded to Operations Committee for final approval. The proposal represents the opinion of all Operations Committee members based on prior discussions with G. A. Thayer.

GAT/lw

RECLASSIFICATION TO ENGINEER

General:

It is the intent of this policy to provide a means for technical personnel in non-engineering classifications to qualify for an engineering rating, provided they have demonstrated the ability to discharge engineering responsibility in accordance with Digital's standards.

Eligibility:

Any full-time regular employee who has been continuously employed by the Company in a technical capacity for one full year is eligible for consideration, provided he has the prior approval of his manager.

Review Authority:

An Engineer Review Board, composed of a senior engineering representative from each of the product line operating groups and manufacturing, coordinated by the Manager, Professional Personnel, will review the qualifications of all employees being considered for an engineer rating under this policy.

Procedure:

1. A Manager considering reclassification of an employee to an Engineer rating, should contact the Manager, Professional Personnel in order to discuss his plans and clarify any questions that may exist on requirements/procedure.

2. The Manager, Professional Personnel will convene the Board, so that the requesting manager may review the employee's qualifications and work record with the Board.

3. The Board will determine the adequacy of the employee's overall qualifications and if sufficient proof of engineering capability does not exist, will require the employee to be placed on an engineering trial assignment of at least 90 days to further determine his qualifications. The trial assignment will be prepared by the requesting manager and approved by the Board, prior to employee's commencing the assignment. Upon completion of the trial assignment, Step 2 will be repeated.

4. The findings of the Board will be summarized and forwarded for requesting manager for his use in a) counseling with the employee (negative) or b) supporting a request for reclassification to Engineer with the Salary Review Committee (positive recommendation).

5. An employee rejected by the Board will be eligible for reconsideration provided

   a) Evidence is presented by the requesting manager that deficiencies noted earlier have been corrected.

   b) The employee has been in continuous employ with the Company in a technical capacity for one year since his prior Board review.

GAT/lw

dec INTEROFFICE MEMORANDUM

DATE 24 September 1968

SUBJECT POWER SUPPLIES FOR 8/I and 8/L

TO Wally Spittle

FROM Bill Long

cc: Ken Olsen
Roger Cady
Don White

During my visit to Maynard I was encouraged by both Ken Olsen and Roger Cady to press on with the adaptation of the 8/L power supply to drive the PDP-8/I . This seems like a reasonable project for us to pursue for the UK machines in particular, but if we are clever about it I think perhaps we could wind up building PDP-8/I supplies for the rest of the world as well.

Roger Cady has promised to send us the latest specifications on both supplies. We should not restrict our project to simply duplicating the capability of the 8/L supply, but rather analyse the actual need of the 8/I and develop a new supply to satisfy those needs.

You should keep in touch with Roger and Don White as to your progress. I am sure that they would be interested in our approach to the problem and also willing to provide advice if need be.

The UK Manufacturing budget can provide the necessary funds to purchase components required for a prototype supply.

Bill

WHL: cah

digital INTEROFFICE MEMORANDUM

DATE: September 26, 1968

SUBJECT: A 16-bit PDP-8/M (Macro)

(CONFIDENTIAL)

TO: Ken Olsen

FROM: Richard Merrill

cc: See attached list

A 16-bit PDP-8

I. Need

Customers need an inexpensive 16-bit computer for numerical control and laboratory data acquisition/analysis. Statements made to justify a larger word length run the gamut from "everyone does it" to "multiple of eight" (no pun intended) and "increased accuracy". Also heard are the words "8-bit ASCII bytes" and "powerful instructions".

Salesmen have supplied more potent statements when fighting the 16-bit competition. The toughest cases arise when both accuracy and speed requirements give the edge to a single or double precision 16-bit word (0-15, 0-31) over a comparable double or triple 12-bit word (0-23, 0-35).

A number that is to contain information on the order of one part in a million needs 20-bits of data (1,048,576); but to retain that accuracy through several operations requires four or five bits more. This is borderline for two 12-bit words but just fine for two 16-bit words. Thus, the argument for increased accuracy bear the most force.

II. Requirements

A. Compatibility

Such a computer should be 99% program compatible with the PDP-8. This means that the machine could be fully usable with a minimum of programming effort. In fact, only the assembly, debugging, loading, and MAINDEC programs need to be rewritten since these are intimately concerned with the logic of machine. All other programs such as FOCAL would only need to be reassembled. Certain device oriented programs like the Disk Monitor would require minor corrections.

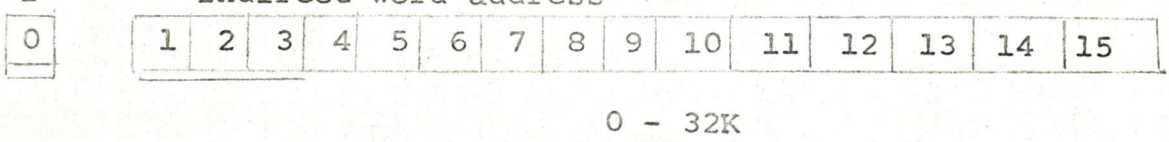
II. Requirements (Continued)

B. Simplicity

The machine should be as simple as possible to design and manufacture and easy to learn and to use. The instruction set should be streamlined yet relevant and should build upon that of the PDP-8.

III. Bit Allotment

A. Indirect references can easily use bit zero to continue multi-level indirect chains. This would provide another powerful facility whose need is often felt in programming the PDP-8:

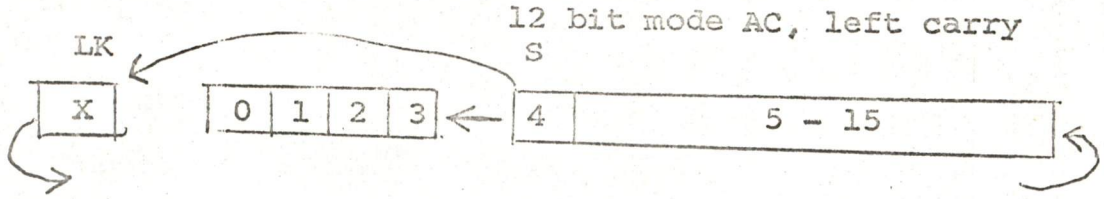


0 - 32K

This eliminates the need for the awkward and space consuming manipulation of instruction and data fields.

B. The AC

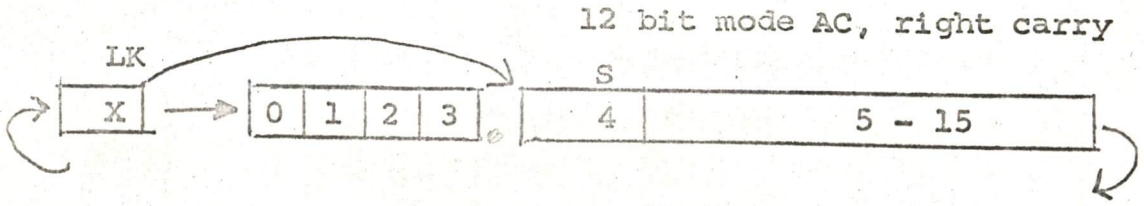
Finally, it is necessary to modify the AC to achieve program compatibility. This is done by using one of the new operate group (1110) instructions (there are at least 2 4 new ones) to setup control modes for either 12-bit or 16-bit operation:



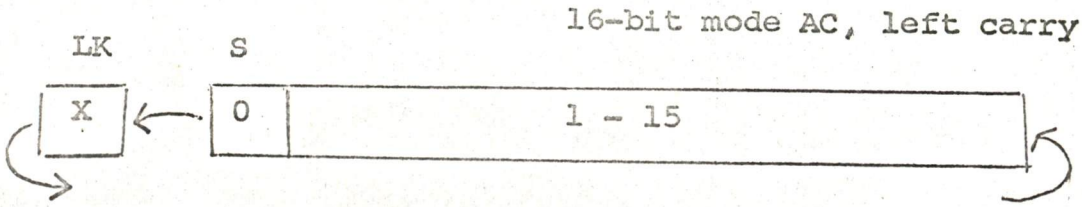
LK indicates the link bit, S the sign bit, and the arrows the left-hand carry in 12-bit mode. This scheme will work for

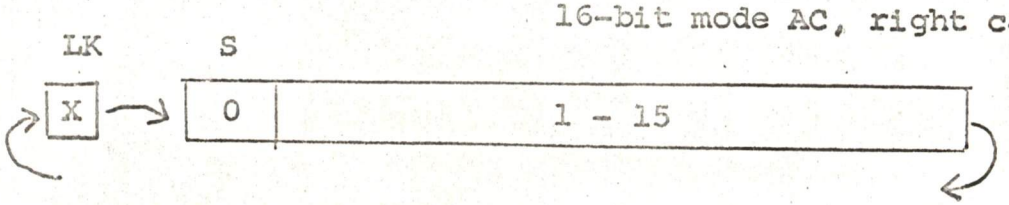
(a) normal addition (TAD) in two's complement,
(b) 12 bit testing,
(c) address computation regardless of negative numbers, octal constants, and masks,
(d) left rotates, and
(e) nearly all instruction formations.

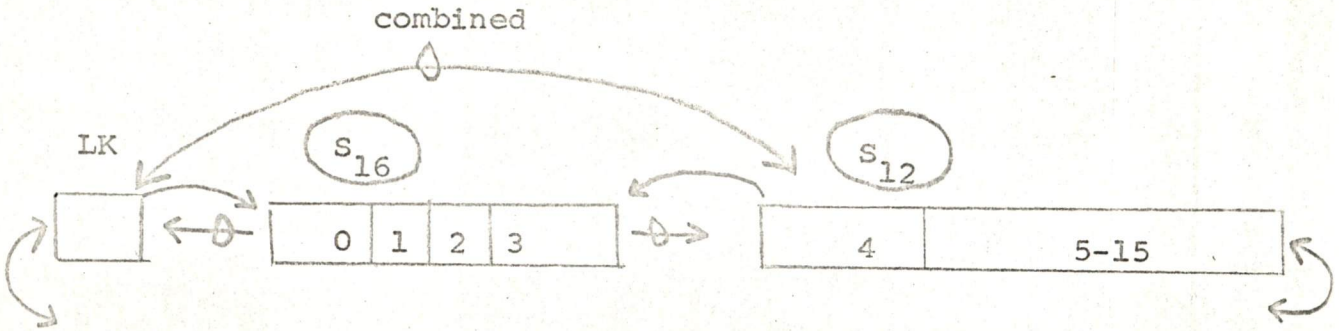
The latter are a rare and questionable practice ans since they are usually formed by adding a constant to an existing instruction there should be few problems of this kind.



For right rotates there should be no difficulty at all.



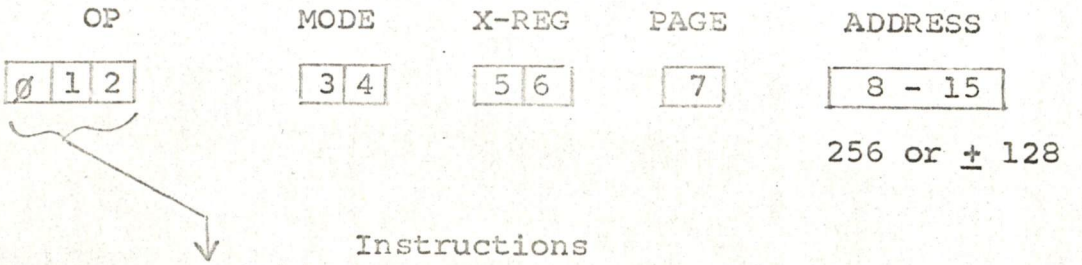




only the circled paths and the sign bit definitions are controlled by the 12/16 mode setting.

The following is a scheme for building a 16-bit PDP-8 that is program compatible with the PDP-8/I for 4K programs yet has many powerful new features. Mnemonics are underlined.

I. MEMORY REFERENCE INSTRUCTIONS



Instructions

oct	bin	
0	000	AND - logical AND
1	001	TAD - Two's ADD
2	010	ISZ - Increment and Skip if Zero
3	011	DCA - Deposit and Clear Accumulator
4	100	JMS - Jump and Save
5	101	JMP - Jump
6	110	BAC - Branch on ACcumulator

Modes

00	□	-
01	I	- Indirect
10	U	- Indirect, and index Up
11	D	- Indirect, and index Down

Incrementing or decrementing is done at the end of the indirect cycle.

X-REG

00	- no index register modification
01	- X1 = 21
10	- X2 = 22
11	- X3 = 23

The contents of x is added to the effective address after the indirect cycle.

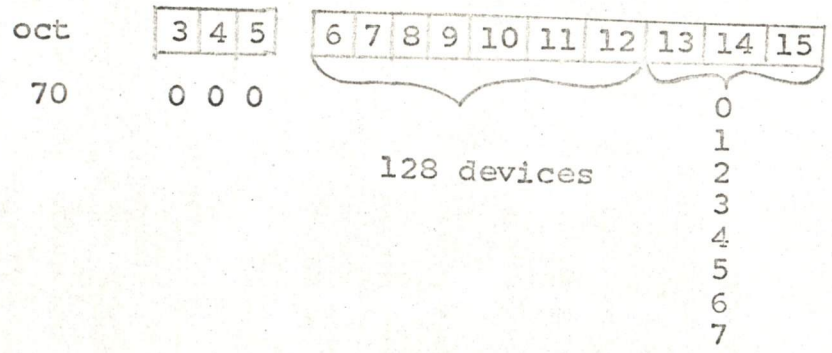
Page bit

1 -- Inpage, Relative (± 128) → MEM 8-15 + PC → MA

0 -- Page zero, Absolute (256) → MEM 8-15 → MA

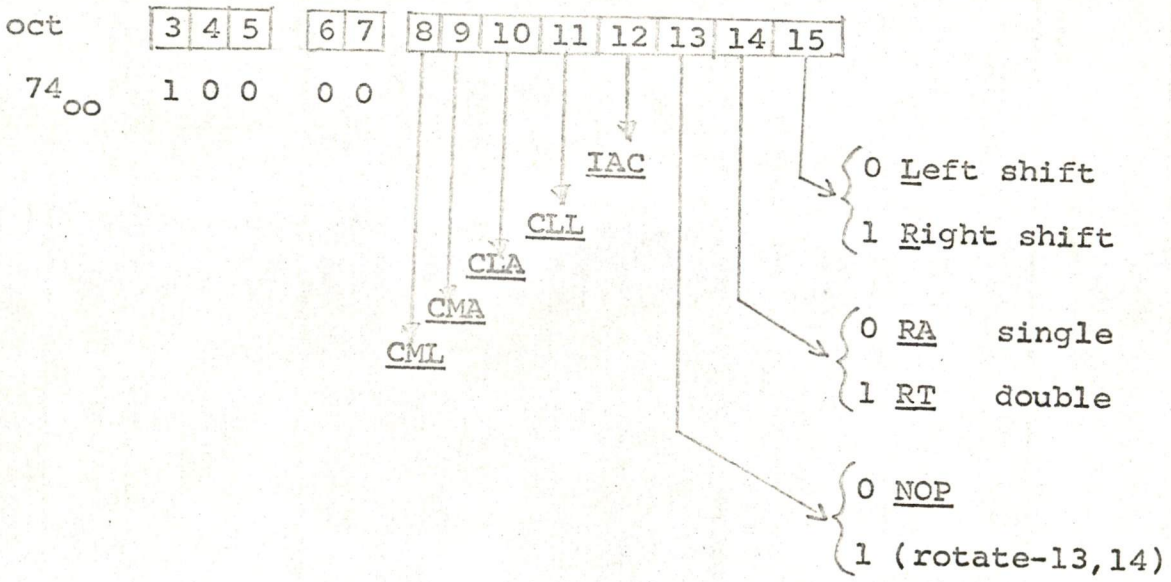
II. INPUT/OUTPUT and OPERATE

(A) IOT



There are twice as many device codes as before.

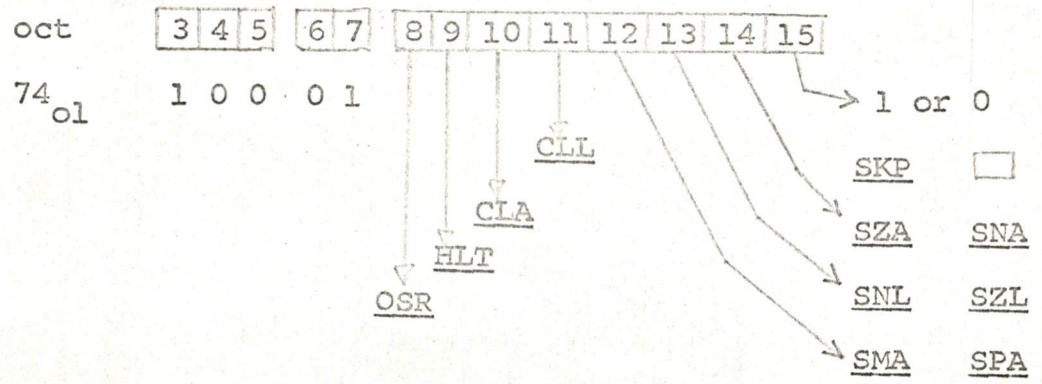
(B) OP1



Logical Sequences

1 - CLA, CLL
2 - CMA, CML
3 - IAC, NOP
4 - RAR, RTR, RAL, RTE

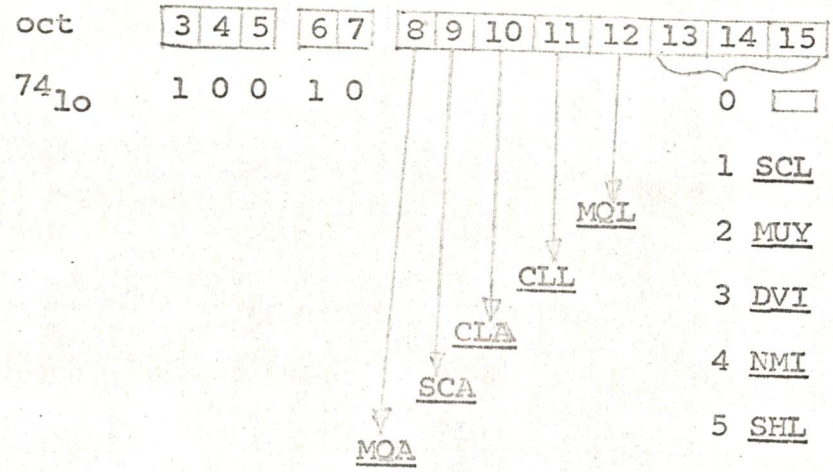
(C) OP2



Logical Sequences

1 - (bit 15 is zero) Either SMA or SZA or SNL
1 - (bit 15 is one) Both SPA and SNA and SZL or SKP
2 - CLA, CLL
3 - HLT, OSR

(D) EAE - Extended Arithemetic Element



1 SCL - scale
2 MUY - multiply
3 DVI - divide
4 NMI - normalize
5 SHL - shift left long
6 ASR - arithemetic shift right
7 LSR - logical shift right

Logical Sequences

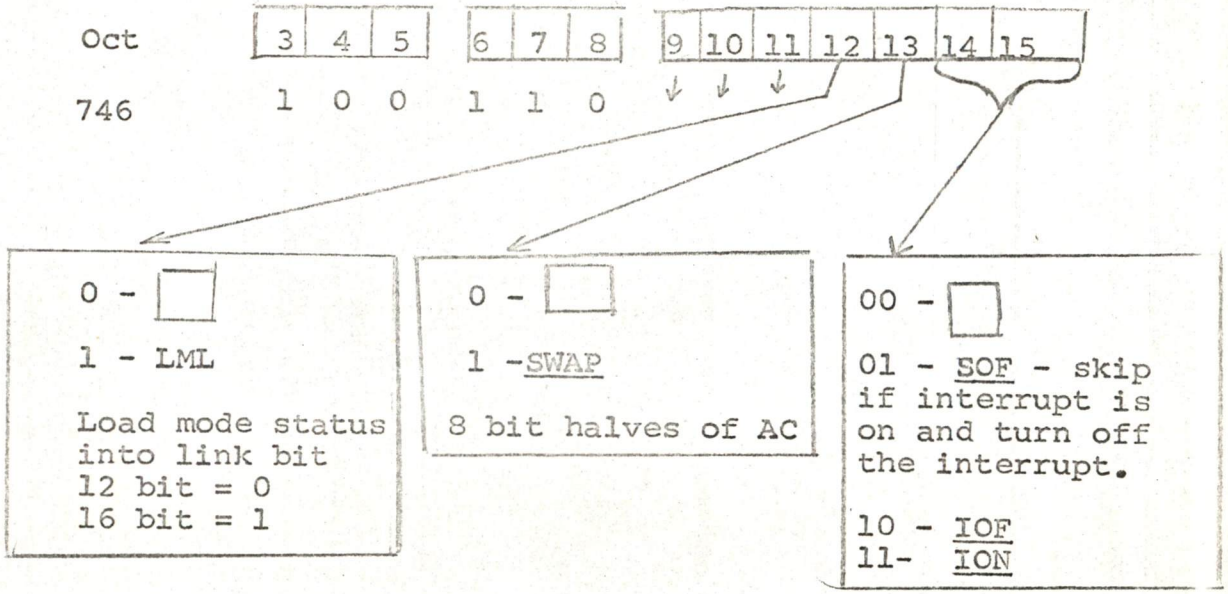
1 - CLA, CLL

2 - MQA, MQL, SCA

3 - others

III. MISCELLANEOUS INSTRUCTIONS!

A. Utility



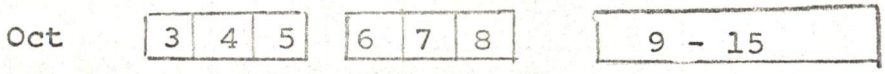
bits 9 + 10

0 □
1 clear half — 0 left = HCL, 1 right = HCR

bit 11

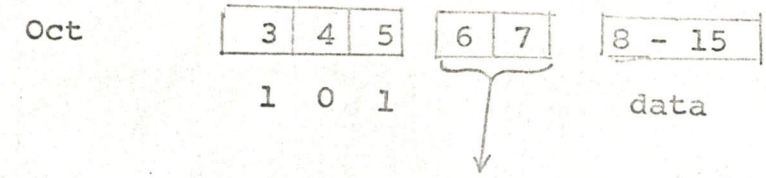
change mode to
0 - 12 bit mode
1 - 16 bit mode

B. Call Indirect location twenty: CAL



IV. HALF WORD IMMEDIATE INSTRUCTIONS

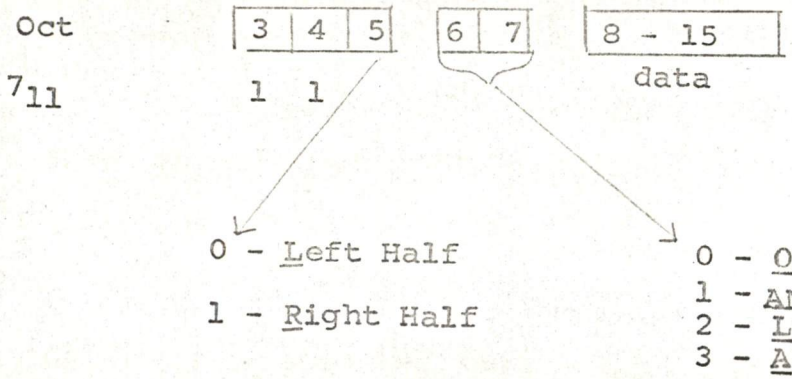
(A) Half word Immediate Tests



75_{00}
75_{01}
75_{10}
75_{11}

Skip if right half of AC is
00 - Less : HSL
01 - Equal : HSE
10 - Unequal : HSU
11 - Greater : HSG

(B) Half word Immediate Operations



Instruction matrix
H OR R
AN
LD
AD

Advantages of 16-bit PDP-8/M

A) The paging problem is gone totally, forever! Addressing is relatic (I 128) and dynamically relocatable!

B) Any register may be incremented or decremented when used indirectly!

C) There are three genuine index registers!

D) 32K addressable!

E) Multi-level indirect!

F) 256 common registers!

G) Half word load and test instructions!

H)

MRI	IO	OP1	OP2	EAE	MISC	HALF		TOTAL
112	+ 8	+ 160	+ 64	+ 256	+ 65	+ 12	=	677

Total combinations and permutations of Instructions! But the programmer only needs to learn mnemonics plus EAE operations.

I) Double precision accuracy better than one part in a million!

J) Fully program compatible with PDP-8/I.

Copies to:

Nick J. Mazzarese
Roger Cady
Dick Best
L. McGowan
J. Cohen
Gordon Bell
Jim O/Loughlin
Harold McFarland
J. Pitts
J. Jones

dec INTEROFFICE MEMORANDUM

DATE October 8th, 1968.

SUBJECT Displays

TO Bob Collings - Maynard

FROM Jack Richardson - Toronto

cc: K. Olsen

While I was visiting a classmate of mine (MIT '62) last week, I was very concerned over the attitude which he reflected regarding DEC's displays in the eyes of some people at Project MAC - specifically some people at ESL. I mentioned this conversation to Ken Olsen at the District Manager's meeting and he immediately suggested that this subject is of current interest to you.

Essentially he state that the speed, flexibility, and features available on DEC's displays are "hopelessly out of date". In one case he mentioned that when ESL went out to quote for a high speed display, DEC was mentioned but not considered as a source. This is in a room where a PDP-7 is currently sitting.

The characteristic that was mentioned quantitatively was that our displays are "100 times as slow as other top-of-the-line displays available today". In particular, he mentioned an Adage display that was considered although I do not recall that he mentioned who finally got the order.

I am sorry that I do not have better info but I was somewhat taken aback at such strong words in an area where I thought DEC was a strong contender. If you wish to know more, you might try contacting:

John Ward
or
Don Thornhill (my classmate)

at ESL. I would expect that they would both give more comprehensive details on this unsavoury attitude at ESL.

I am also enclosing a spec sheet on a display unit which may be of interest. This is a wired program display that works on

(con'd)

dec INTEROFFICE MEMORANDUM

DATE

SUBJECT

TO FROM

a Dataphone. I saw this display running (with "mouse") and was very impressed by its capability. How does this compare with our KV8/I or anything else which is currently in PDP-8 engineering? (e.g. VT09, VR-12 XY scope which we "saw" but received no information).

Jack.

Jack

JER/mp
Enclosure

DIGITAL

INTEROFFICE MEMORANDUM

DATE October 24th 1968

SUBJECT European Headquarters

TO Ted Johnson

FROM J.C. Peterschmitt

We had agreed in August to postpone the decision about European Headquarters until early 1969. At this point, I consider it urgent to make a decision much sooner, for following reasons :

1) The difficulty of getting together at frequent enough intervals with some headquarter people reduces their and my efficiency.

2) I keep insisting that until further notice, the Headquarters are in Reading. For most people in the UK, since all other Headquarters activities are there, there is little doubt about the current set up. For some of them however, and for the majority on the continent, since my office is in Cologne and I have no office in Reading, there are no such things as Headquarters at this point. This creates a very undesirable psychological feeling of lack of central unity.

3) Several people will have to move to headquarters soon. The cost estimated by Bob Dill is around $ 5.000.- per person. Even if it is less, as I hope it is, the longer we wait the more people must move, the higher the expense. Also, several headquarter people should know as soon as possible because of personal arrangements.

I . HEADQUARTER FUNCTIONS

1.1 District Headquarter Functions

Each main district, and probably each district, must have a strong organization of its own, capable of dealing with virtually all day-to-day operational matters. This organization includes :

- strong sales and F.S. management
- a specialized F.S. support team (for OEM support and high-power back up to the district F.S. organization)
- software support
- customer training

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Language and generally local image important factors for all these functions. Also, the possibility of drawing on the local supply of qualified personnel in each country is essential (we could not get all these people to move to a central location).

1.2 Regional Quarter Functions

European Headquarters for the next 3 years will perform following functions :

- provide on a continuous basis a unified set of rules and frame-work within which the District Manager will operate on a day-to-day basis.
- monitor the operations of the district offices.
- act as a central clearing place for all policies. These policies may be suggested by the districts in function of their needs (or at the European Headquarters), formulated at European Headquarters and submitted to Maynard for approval, or may be originated by Maynard.
- provide all services which can be effectively centralised such as :
  - Marketing
  - Central F.S. support
  - Training (both technical and management)
  - Accounting
  - Order Processing
  - Personnel
  - Advertising, Sales promotion, trade shows
  - Central warehousing

It has been formally stated by P. Kaufman that production is not necessarily tied to European Headquarters, so that no consideration is given to production in this analysis.

II. FACTORS FOR SELECTION OF THE LOCATION

2.1 Relation to any particular district headquarters

As appears from the above, European Headquarters are not involved in day-to-day operation of a district and should not be. The Reading experience however suggests that if European Headquarters are physically together with district

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Headquarters, it is difficult to avoid that people in European functions devote a substantial (and frequently excessive) part of their effort to the local district : typically, individuals whose work involves significant travel throughout Europe will only travel actually 20-30 % of their time outside of the UK. Plans and reports developped by them will devote at most 50 % and frequently only 1/3 of their voume to the non-UK aspects of the problem, even if these individuals make a conscious effort to the contrary. Therefore, I strongly believe that physical separation is necessary, even if European Headquarters were in the same city as a particular district headquarter.

2.2 Centralization in only one place ?

It is not certain at this point that all European headquarter activities should be centralized in one place. Activites which are extremely well defined and can operate practically autonomously, such as accounting, may not need to be located with others. The growing volume of our activity may justify within 2 years the establishment of communication lines between two or three European locations for the transmission of data and reports (I have requested cost information). However, it seems to me that at this point, efficiency requires that at least following functions be located together in the same place : Regional Manager, Field Service Manager, Central Marketing, Personnel, Promotion. I also believe th&t it would be desirable to have central training in the same place, because of its relationship to central support (marketing, central F.S. support).

2.3 Transportation

People working at the headquarters will have to travel fairly extensively within Europe. Therefore, the location should be :

- fairly central
- near an airport with adequate service. THE number of planes per day in any particular direction however is not critical, as travel to and from headquarters will typically be planned in advance rather than on an emergency basis.

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2.4 Communications

Telephone communications are essential, therefore good facilities should be available, allowing easy and reliable access to all European countries.

2.5. Cost

Costs for office space and facilities, as well as operating costs, legal fringe benefits, etc... should be low.

2.6 Availability of personnel

Three categories of personnel will work at headquarters :

1. Management
   These individuals will be drawn from individual district offices. Availability is not a problem, but working permits are necessary.

2. Other non support

   This includes marketing specialists, training personnel etc... To a large extent, they will be drawn from district personnel mostly as temporary positions (1-2 years) before returning into line functions at district levels,(working permits required). Another smaller part will be hired locally to the extent available.

3. Support Personnel

   Multilingual support personnel must be available.

2.7 Contact with outside organizations

Only promotion and advertising will have a need for contact with otuside organizations. According to Steve Bowers however [illegible], work with these organizations does not require that they are located in the proximity.

2.8 Factors relating to the individuals

2.8-1 International schools :
An important proportion of employees working at European Headquarters (temporarily or continuously) will be foreigners with children in school-age. A good international school is essential, with the 3 main languages (English, German, French).

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2.8-3 Personnel preferences

Headquarters will draw personnel from all countries. Europeans (even many DEC employees) have a propensity to stay in their country of origin. A tour of duty in a European function may not necessarily be a propotion (in the short term) but rather a stepping stone for advancement. It should be in a geographical location to which the individual (and his wife) will be attracted out of the comfortable home and job from which he comes.

III. Cities considered

Following cities are candidates :
Reading, Frankfurt, Amsterdam, Brussels, Geneva. Paris has been ruled out a priori, essentially because of the cost of operating in Paris. The following is a preliminary comparison of these cities :

	Reading	Frankfurt	Amsterdam	Brussels	Geneva
Geographically Central	Bad	very good	very good	very good	good
Airport	very good (but fog)	very good (but fog)	good	bad	medium to good
Spac e cost	Low	medium	medium	bad-medium	medium
Operating cost	Low-medium	$ 3/sqf medium	$ 3/sqf medium	$ 2.30/sqf medium	2.50/sqf low-medium
Close to major district office	yes	yes	no	no	no
Telecommunications	bad (no international direct dialing)	good	good	medium	good

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	Reading	Frankfurt	Amsterdam	Brussels	Geneva
Fringe benefits cost	medium	medium	high	medium	low
Availability of multilingual support personnel	bad	medium	good	medium	very good
Working permits	no problem	no problem	no problem	no problem	limited see note
Free Port	no	yes	yes	no	yes
Personnel income tax	high	medium to high	very high	medium	lowest in Europe
Housing cost	low	medium	high	medium	medium
International school	bad	good	good	good	good
Overall Geographical attraction	low to medium (high for British and Americans)	low (high for Americans)	medium to high	medium (high for French)	high

Note about working permit in Geneva

Permanent working permits are limited, but :

- temporary working permits for periods of up to 18 months are easily available.
- no working permits are required for people residing in a " Free Zone" on French territory surrounding Geneva (Distance to center of Geneva : 3-5 miles). There are no limitations imposed by French regulations for foreigners to reside in this zone.

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DATE: November 25, 1968

SUBJECT: LETTER FROM UNIVERSITY OF EDINBURGH

TO: Elsa Carlson FROM: Ron Wilson

I have forwarded the letter received from G. Idwal Williams to our Manchester Office for answering and follow-up.

I have also requested they provide you with an answer.

lm

11-15
Ron Wilson to ans.

UNIVERSITY OF EDINBURGH

SCHOOL OF ENGINEERING SCIENCE

(ELECTRICAL ENGINEERING)

TELEPHONE 031-667 1011
EXT. 3260

KING'S BUILDINGS
MAYFIELD ROAD
EDINBURGH, 9
Scotland.

Saturday, 9th November, 1968

Manager,
Research and Development,
Digital Equipment Corporation
Maynard
Massachusetts,
U.S.A.

Dear Sir,

I am involved on a project which is looking into the possibilities of using the Department's P.D.P.-8, along with one of the Department's Analogue Computers, as a hybrid computer.

We have been wondering whether D.E.C. had looked into this possible use of the P.D.P.-8 and if you had, whether you would be willing to pass some of the information gained, to us. What we would like is general information on the types of Digital-Analogue and Analogue-Digital converters and other peripheral equipment which you may have used or experimented with.

We would be very grateful for any information you passed to us.

Yours faithfully,

G. Edwal Williams.