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THE CALIFORNIA DIGITAL COMPUTER
WITH
A COMPACT MAGNETIC MEMORY

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Introduction

The California Digital Computer was expressly designed as an "intermediate" machine, to be capable of a considerable amount of general-purpose automatic computing but not to compete with the extremely high-speed electronic computers under construction in a number of laboratories. It is to be operated by and for the research and instructional staff of the University, and it is expected that its load will consist of an exceptionally wide variety of problems, corresponding to the breadth of interests of the University staff. It is also to be used in the instructional program of the graduate school, for training of students both in the design of computers and in their applications to engineering problems.

The design has been chiefly influenced by the following objectives:

1. Low Cost. The total cost of parts and direct labor of construction (not including research on components and overhead) will be less than $25,000.
2. Operation by the user. This has led to the use of the decimal rather than the binary number system and to other concessions to simplicity of programming rather than speed of operation or simplicity of construction.
3. Flexibility. The unusually large memory and other features make it readily adaptable to most problems without special techniques of coding.
4. Accessibility for demonstration as well as trouble-shooting and repair. All electronic components are accessible even when the machine is in operation.

These objectives have led to a machine which is exposed rather than packaged, but the total space requirement of about 100 square feet is not unreasonable and problems of heat dissipation and servicing have been greatly simplified.

Logical Design

In conformity with the design objectives listed above, the magnetic drum seemed to offer the only large low-cost memory system. To remove limitations on programming imposed by a small memory, and to simplify the input problem, the memory capacity was set at 10,000 10-decimal-digit numbers. Each number is stored as an absolute value preceded by its sign; in the memory the sign occupies the eleventh or left-hand digit position. Orders are stored interchangeably with numbers on the drum and any required portion of the memory can be devoted to orders. The magnetic memory is non-volatile and any stored information is retained until new information is written in its place. The computer can be shut down without losing the contents of the memory drum.

Figure 1 shows the word structure used for the computer. When the word is a number it is coded digit by digit into the binary system, with the four binary parts of each decimal digit transmitted in parallel but the decimal digits following each other serially. When the word is an order it appears as six digits just to the right of the empty sign column; the first two digits specify the operation and the other four usually indicate the memory position of the operand.

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* The development of the computer described was supported by the Office of Naval Research jointly with the University of California.

The "single-address" system of writing orders is used, so that if two numbers are to be added two orders are required to call them from the memory. If the sum is to be returned to the memory still a third order is needed to specify the location, if not, the sum remains in the A-register and other operations can be performed upon it.

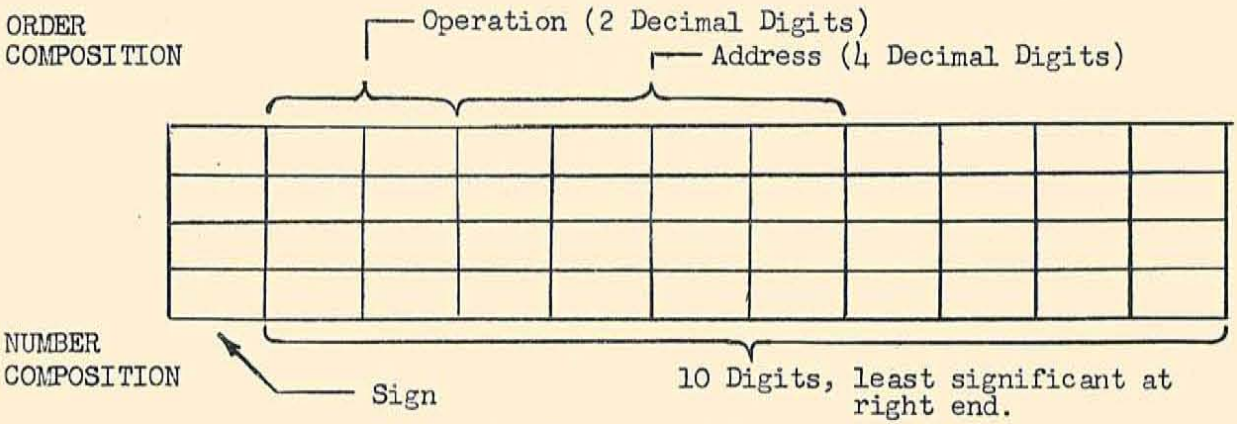

Figure 1. Word Structure in the CALDIC

Figure 2 shows the block diagram of the computer. The memory drum is provided with a timing track permanently recorded on the surface; this supplies timing pulses which initiate all operations of the electronic circuits. Since the timing pulses are supplied by the drum, changes in the drum speed do not cause difficulty and the drum is driven by a simple 3600-rpm induction motor.

The computer will contain three arithmetic registers, called the "A" or accumulator register, the "R" or multiplier register, and the "D" or multiplicand register. These all function as shifting registers, transmitting their contents from left to right under the control of shift pulses supplied by the central control. Various paths for circulation of the register contents are provided; for example the "shift left" operation is carried out by shifting to the right through a circulation path, but stopping before the original position is reached.

The operation of the computer follows a cyclic pattern, essentially as follows: 1. The address of the next order is taken from the order counter and used to locate the order which is read into the D-register. 2. The order is then shifted into the operation and address registers, while the contents of the address register are returned to the order counter and increased by one unit to provide for the next cycle. 3. Since the address register now contains the address of the operand, it is read into the D-register and immediately operated upon as instructed by the contents of the operation register. When the operation is complete the cycle repeats. Orders are therefore taken in sequence from the memory boxes; the sequence can be interrupted by special orders which change the contents of the order counter either unconditionally or in accordance with the results of the computation.

The orders to be provided are the following:

add	transfer to memory
subtract	print out
multiply	clear address and add
multiply and round off	change contents of the order counter
divide	change contents of the order counter but only
divide and round off	if the previous operation overflowed the register.
extract the square root	shift left
read the input tape	shift right

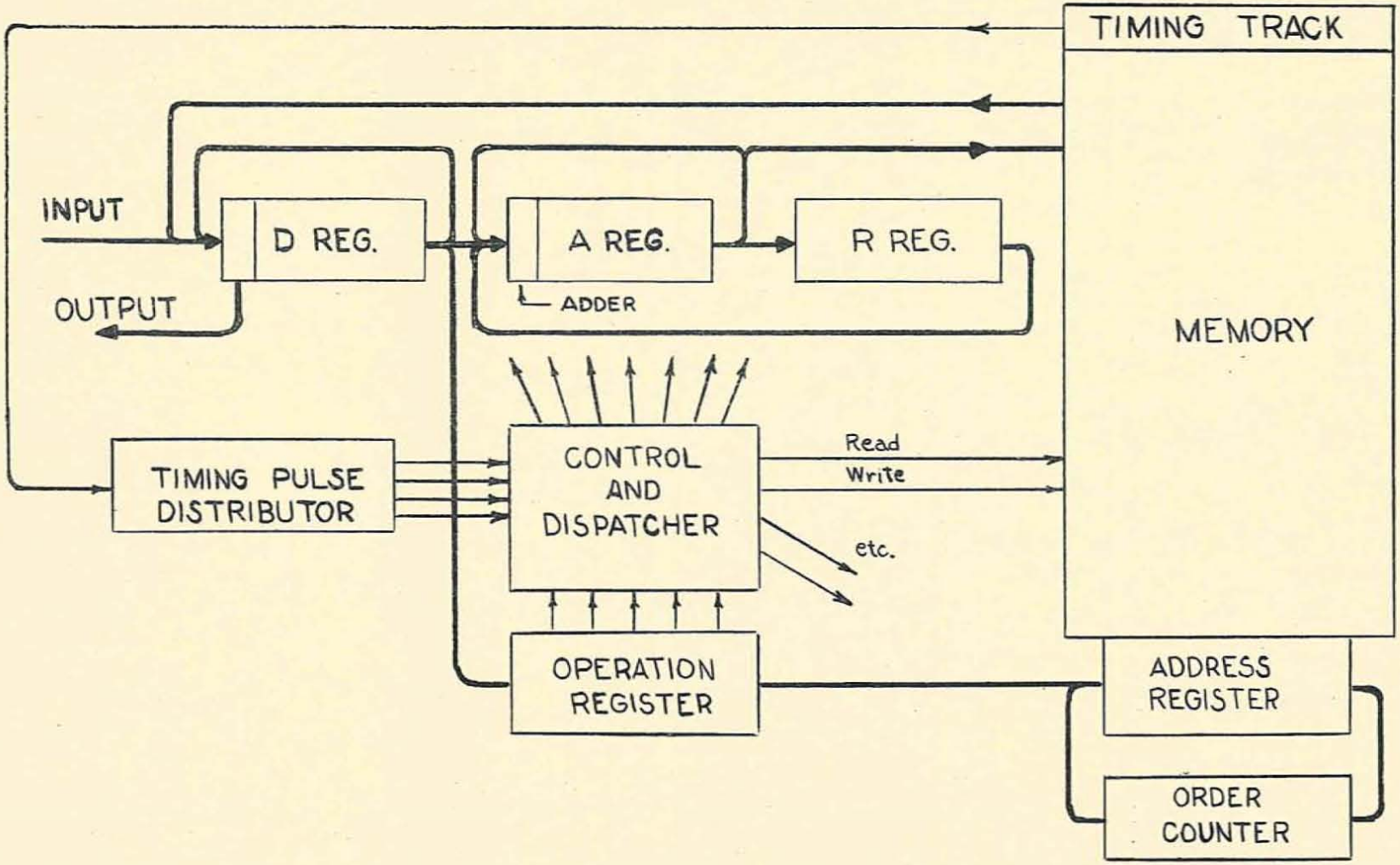

Figure 2. Block Diagram of the CALDIC

Addition and subtraction are performed as the operands are shifted from the D-register through the adder into the A-register, simultaneously with the circulation of the contents of the A-register through the second input of the adder. The result of the operation always stands in the A-register unless a second order transfers it to the memory. In multiplication the multiplicand circulates in the D-register while it is repeatedly added, with the necessary shifts, into the partial product which accumulates in the A-register. Meanwhile the multiplier, which was transferred from the A into the R register at the beginning of the multiplication, is used up digit by digit and the space vacated is used to hold the overflow from the addition process. At the end the A and R registers hold the double-length product, which may be rounded off to ten digits or retained in full at the wish of the programmer.

As just indicated, the only operations actually performed in the computer are addition, shifting, and complementing. The time required for an actual addition is very small compared to the time of rotation of the drum, so that the total time for an "add" operation is essentially the time required to get the order and the number, usually the time of one revolution of the drum. For a multiplication or division, either of which may require up to 99 additions or subtractions, an extra revolution may be necessary. In other words the basic arithmetic operations can be performed at a rate of about 25 to 50 per second.

The orders are all standard except two: the "clear address and add" order provides for the change of the address part of an order without affecting the operation part, while the conditional sub-program order takes effect only if an overflow occurs in the preceding operation rather than only if the result of the preceding operation is negative as is more customary. It is believed that this will reduce the number of necessary orders by providing for overflows other than those required for sub-programming; any possible overflow can be provided for simply by inserting an order which tells the computer what is to be done if the overflow occurs. If no overflow occurs, the conditional order is disregarded.

Magnetic Drum Memory

The magnetic drum used is of quite novel design. It is fabricated of a piece of aluminum tubing 8 1/2 inches in diameter and 26 inches long, fitted with end plates and shaft and accurately turned and balanced. The drum is mounted vertically in precision bearings and four columns of magnetic heads are arranged around it; because of the vertical position all of the heads are easily available for adjustment. The machining and the mounting must be sufficiently precise so that eccentricity or vibration are avoided, since the heads are normally operated about one one-thousandth of an inch away from the drum surface and even slight eccentricity would cause considerable modulation in the voltages recovered from the drum.

The drum is coated with a preparation of magnetite by spraying; a light coat of lacquer may be used over the magnetite but is not necessary. It is found that the coating usually has a grain structure after spraying, leading to a permanent pattern of magnetic flux which can be reversed but not eliminated. The level of the corresponding voltage, however, is below the voltage recovered from a recorded pattern enough so that no difficulty is expected from it.

The combination reading and recording heads are arranged in staggered columns in such a way that the heads write magnetic tracks 1/20 inch wide, spaced on 1/10-inch centers along the axis of the drum. The "non-return-to-zero" system of recording is used; the surface is always magnetized to saturation in one direction or the other, to correspond with the digit being written, and no erasing is used. A succession of similar digits leaves the surface uniformly magnetized in one direction, and a voltage is recovered only when a change occurs in the recorded pattern. The cell density along the circumference of each track is slightly over 90 per inch, so that some 900 binary digits are recorded per square inch of drum

surface and over 480,000 on the entire drum. Since the magnetic heads are operated in groups of 4, 48 cells are used for each 10-decimal-digit number--40 for the binary-coded digits, another in each track for the sign (actually the sign digit is written on one track only) and still another in each track for a zero digit used as a space between words. Since voltage is recovered only when the recorded digit changes, the reading circuits when switched on must be set correctly. All switching is therefore done while the zero space is passing the reading heads.

As suggested before, one reading head is used to read a timing track permanently recorded on one portion of the drum completely around it except for a small gap. The recovered signal is converted by the clock-pulse generator and timing-pulse distributor into three kinds of timing signals: an origin pulse, used to mark the initial sector of each recorded track and reset the sector counter; space pulses, occurring between recorded words and used to count sectors and thereby locate any desired word as well as to initiate switching; and digit pulses, of which trains of eleven occur between successive space pulses and are used to shift numbers or orders through the arithmetic organs of the computer.

Figures 3 and 4 show the magnetic head design used, with its internal parts and connection cap, and also the head mounting with adjusting and clamping screws. The heads themselves have been especially designed; the core consists of about 40 insulated laminations of 4-79 molybdenum permalloy 0.001" thick, and it is provided with a 200-turn reading coil and a center-tapped 200-turn writing coil. The current required for recording is about 150 milliamperes and the recovered voltage on reading is about 0.2 volt. Both of these figures correspond to head-to-drum spacings of about one mil; the gap between the poles of the magnetic heads is considerably larger, about six mils. Cell densities up to more than 300 per inch at frequencies up to 300 kilocycles have been recorded with these heads, but only about 90 per inch and 144 kilocycles are actually used.

Figure 5 shows a schematic arrangement of the memory and the associated circuits for selection of any required word within the time of one revolution of the drum. The address register is supplied with the four decimal digits of the address, each coded into binary form. Seven of the toggle circuits of the address register are used to control the band switch, thereby selecting one of the fifty groups of four heads each to write or read. The other nine toggle circuits contain the sector address which is continuously compared with the contents of the sector counter. (Two hundred sectors make up each band on the drum.) When the sector address and the contents of the sector counter coincide, the read-write switch is energized to perform the required operation, and simultaneously digit pulses are supplied to the information registers to shift their contents into or out of the amplifiers associated with the magnetic heads.

Figure 6 shows the arrangement of gating circuits used with the memory drum. One amplifier tube is used as a reading gate, one twin triode to provide the writing current, and another twin triode as a writing gate; these three tubes are duplicated for each of the 200 heads. In addition 50 tubes are used in the band switch to combine the band-switch output and the writing order and control the writing gate. All other portions of the reading and writing amplifiers are built in quadruplicate only, corresponding to the four-channel system of digit transmission.

Other Circuitry.

All circuitry for the computer will be arranged on phenolic panels forming three sides of a square about ten feet across. This arrangement makes all components accessible and provides for heat dissipation without air conditioning equipment. Figure 7 shows the layout of the completed portions of the computer, and Figure 8 shows one of the arithmetic registers which includes 44 toggle circuits

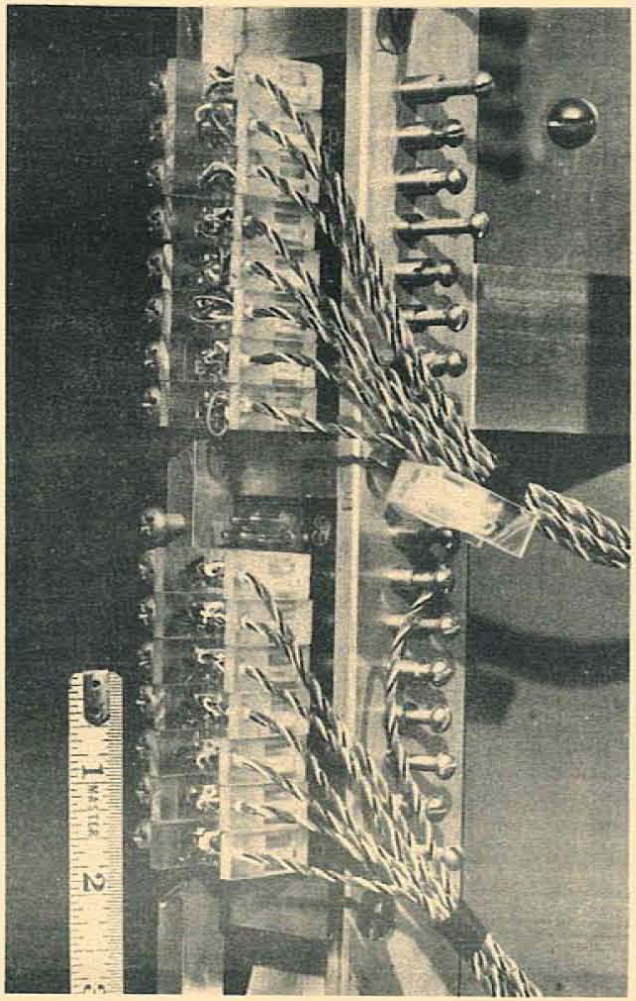

Fig. 3. Magnetic-Head Holder

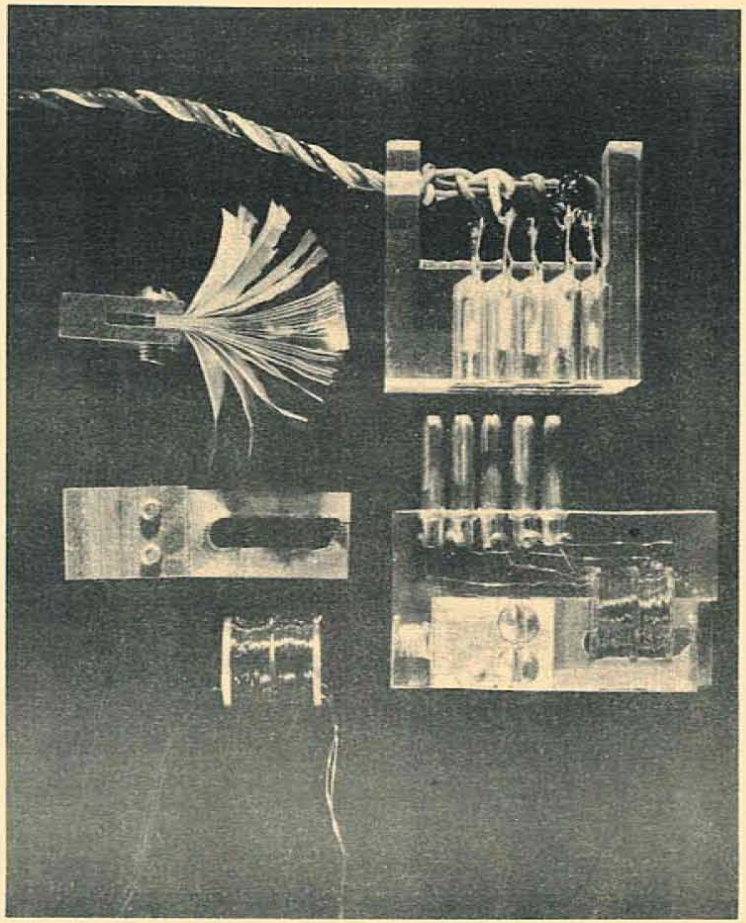

Fig. 4. Magnetic Head and Connection Cap

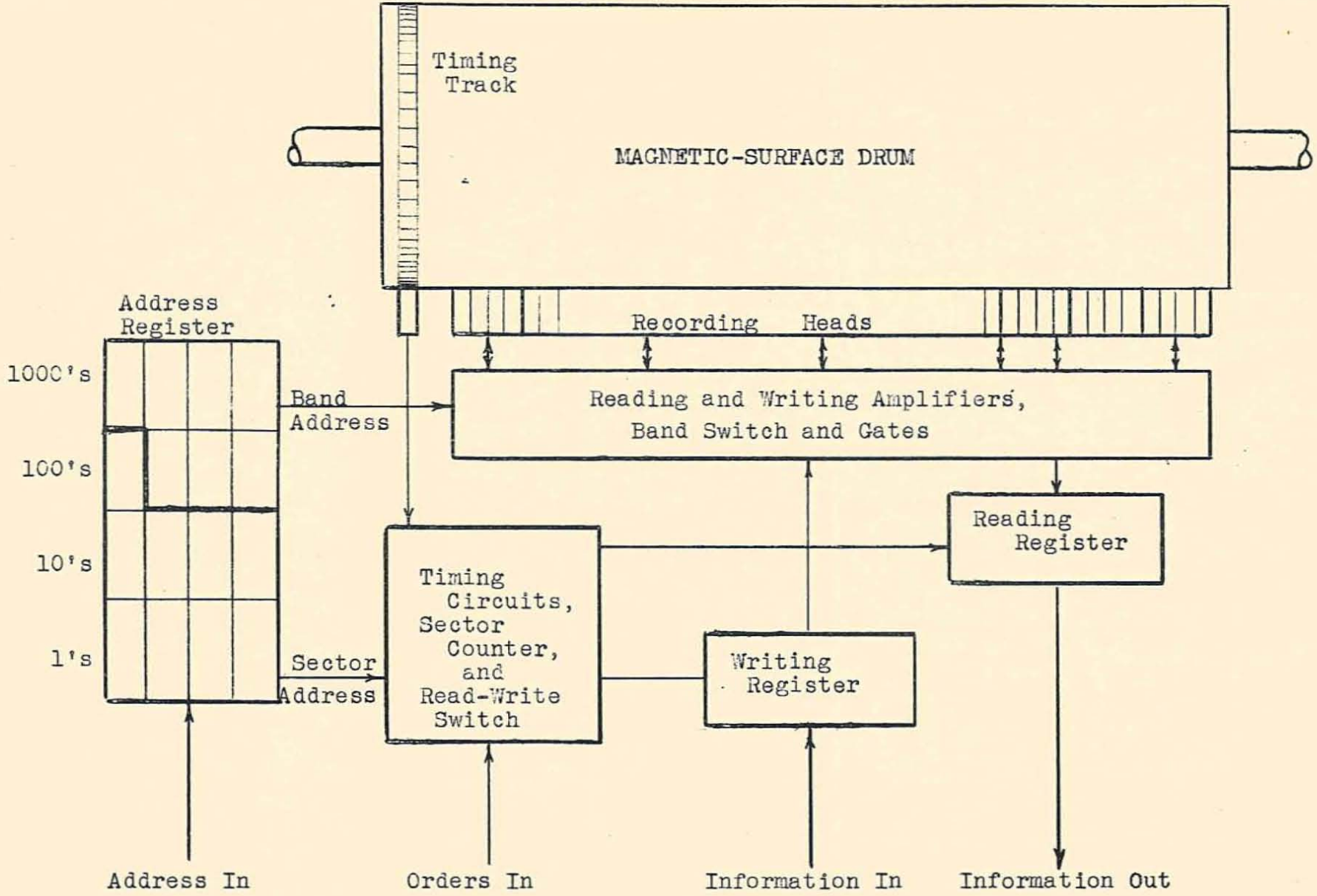

Figure 5. DIAGRAM OF MAGNETIC MEMORY

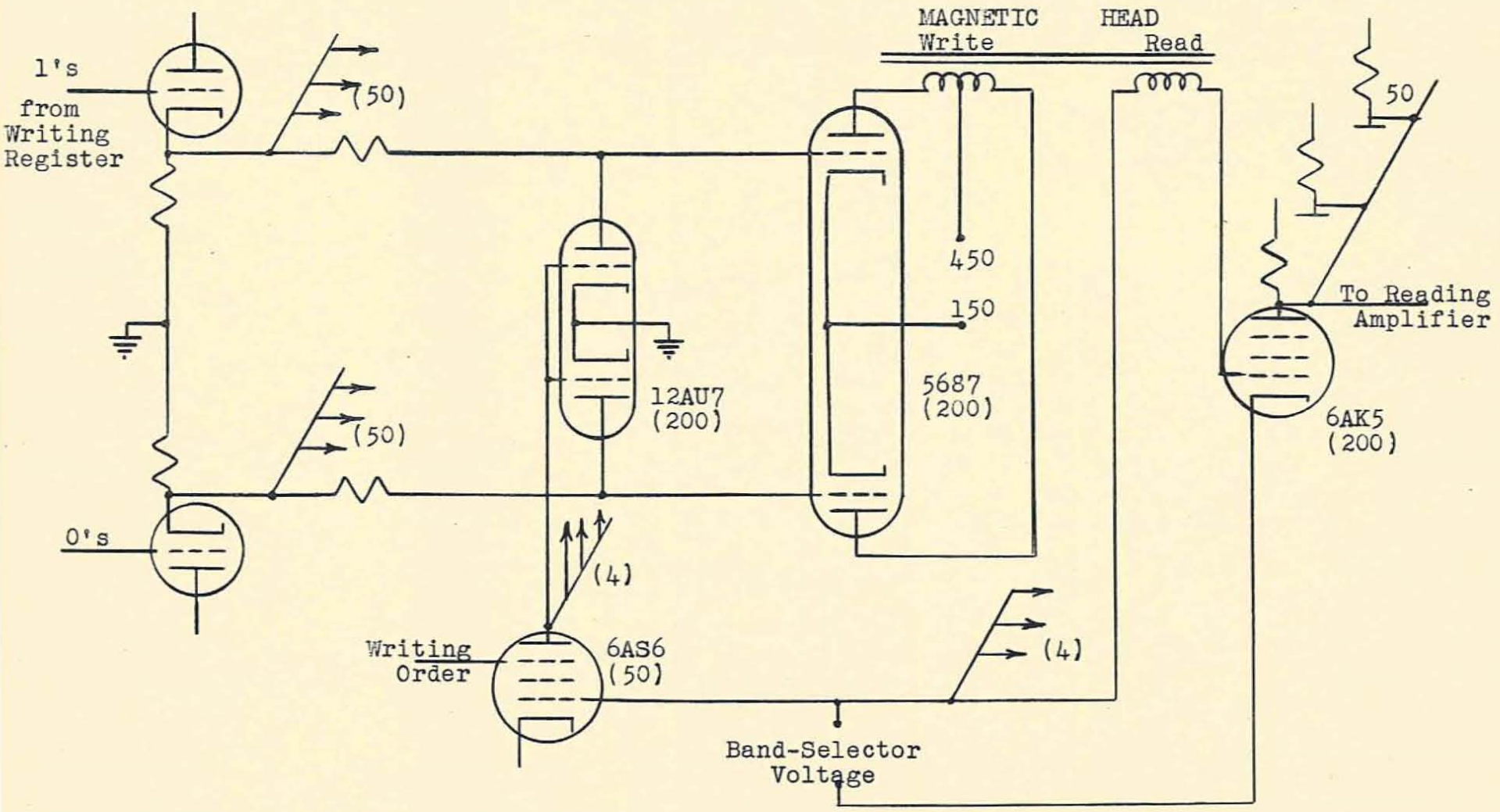

Figure 6. MEMORY GATING CIRCUITS
(For 50 Bands of 4 Tracks Each)

and the associated gates. Since the maximum pulse repetition rate is only 144 kilocycles very simple electronic circuitry can be used and little pulse-shaping or shielding is necessary. Both pentode and crystal-diode gates are used, rather more of the crystal type since these appear in the registers which use two crystals and one toggle per binary digit stored. So far the tube types used are 6AS6 gates, 12AU7 toggles, 5687 drivers, and 6AK5 reading amplifiers. The crystals used are 1N34A or Raytheon CK-706.

Figure 9 shows the block diagram and Figure 10 the circuit of the shifting registers, which have proved to be particularly reliable and convenient. Each toggle is supplied with shift pulses through one or the other of two gates which are controlled by the preceding toggle. Flipping of the toggle is required only if the digit to be received is different from the digit previously stored; no clearing is required. Each gate consists of a single crystal connected through appropriate resistors from the plate of one toggle to the grid of the next. The only requirement on pulse shapes is that the input pulse shall not be wide enough to make its trailing edge pass through a gate opened when the same pulse flips a toggle. (The shift pulses are about 1 microsecond wide, between 20 and 30 volts in amplitude.) As shown in Figure 8, the registers are built up of four channels of toggle circuits, each of which transmits only one of the binary parts of each coded decimal digit. There is no connection between channels except in the adder.

The order counter is similar to a shifting register except that it must also count and therefore connections between channels and provision for carry must be made. The order counter can be seen on the extreme right of Figure 7. The address registers are also similar, except that a buffer is attached to each toggle to allow the state of the toggle to be sensed by the band switch or sector counter.

Input and Output

Input to the computer will be from a perforated paper tape read through a photoelectric reader at a rate which will permit the memory to be completely filled in approximately three minutes. The computer can call for input, but does not refer to the input tape while computing and in general the contents of each input tape will be read completely into the memory at the beginning of each computation. Figure 11 shows the scheme of input used.

Numbers are typed on a tape-punching typewriter in the usual fashion, left to right with the sign first. The copy produced by the typewriter can be tabulated if desired; the corresponding tape is of course perforated in the order of typing. The tape is read into the D-register, where the order of the digits is reversed and the non-significant zeros, if any, added. Then the numbers pass into the A-register where they wait (a maximum of 17 milliseconds) for the drum sectors into which they are to be written. Ordinarily the memory boxes are filled in sequence under control of the order counter, but special coding on the tape specifies where the sequence is to begin and whether portions of the memory are to be skipped in the filling. This permits portions of the memory to be retained through several computations if desired, and the very large memory capacity makes it likely that subroutines may frequently be stored for long periods when all the memory capacity is not needed for orders and data.

The output cycle will be similar to the input, with the numbers reversed as they are read out of the memory and punched. Output will be much slower than input, since it is limited by the punch speed of about ten digits per second.

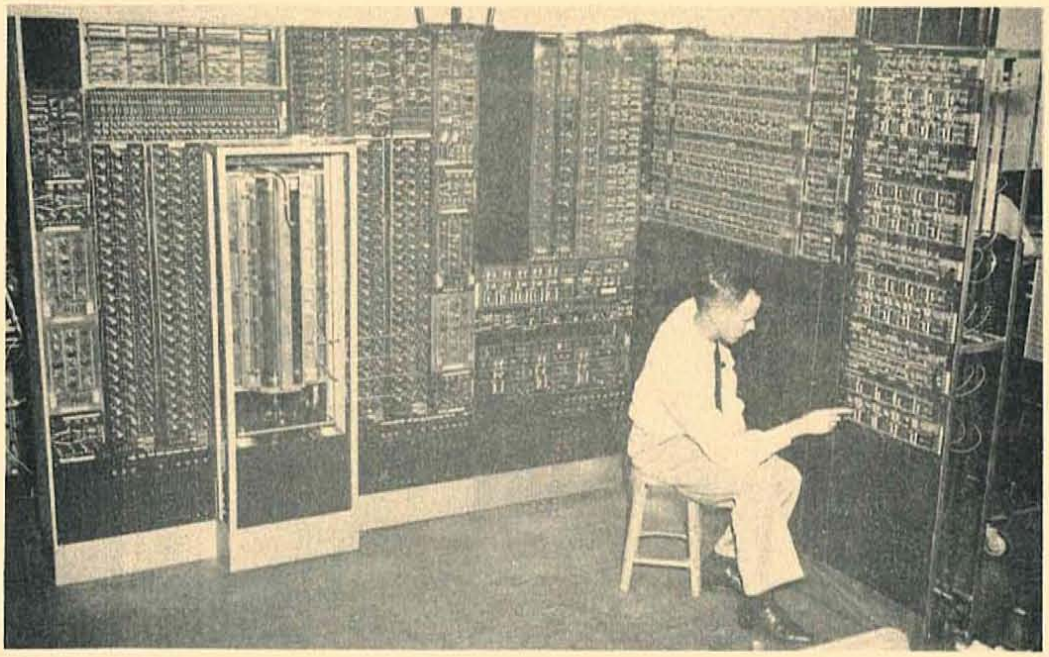

Fig. 7. Completed Parts of the California Digital Computer

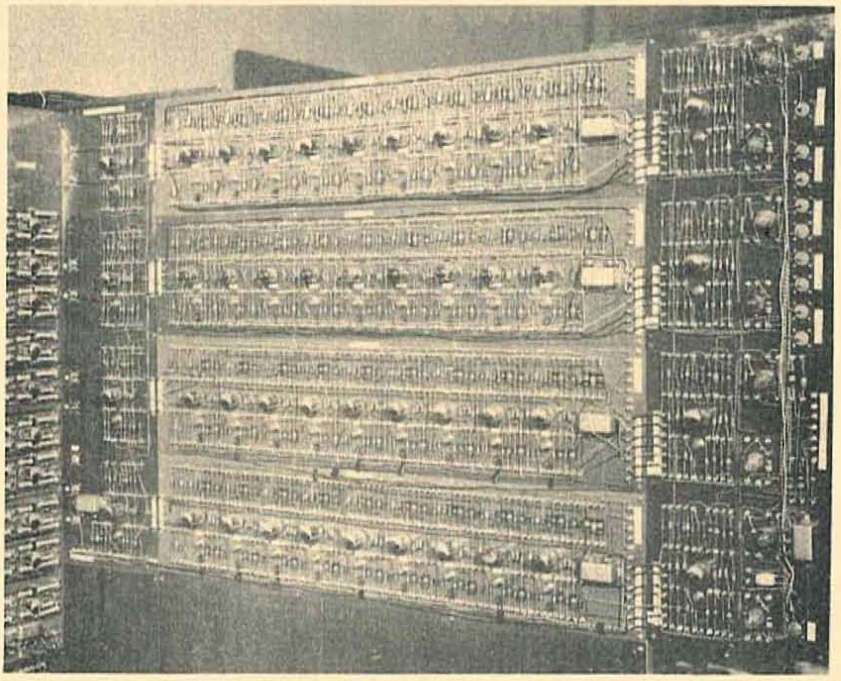

Fig. 8. Arithmetic Register with Temporary End Columns

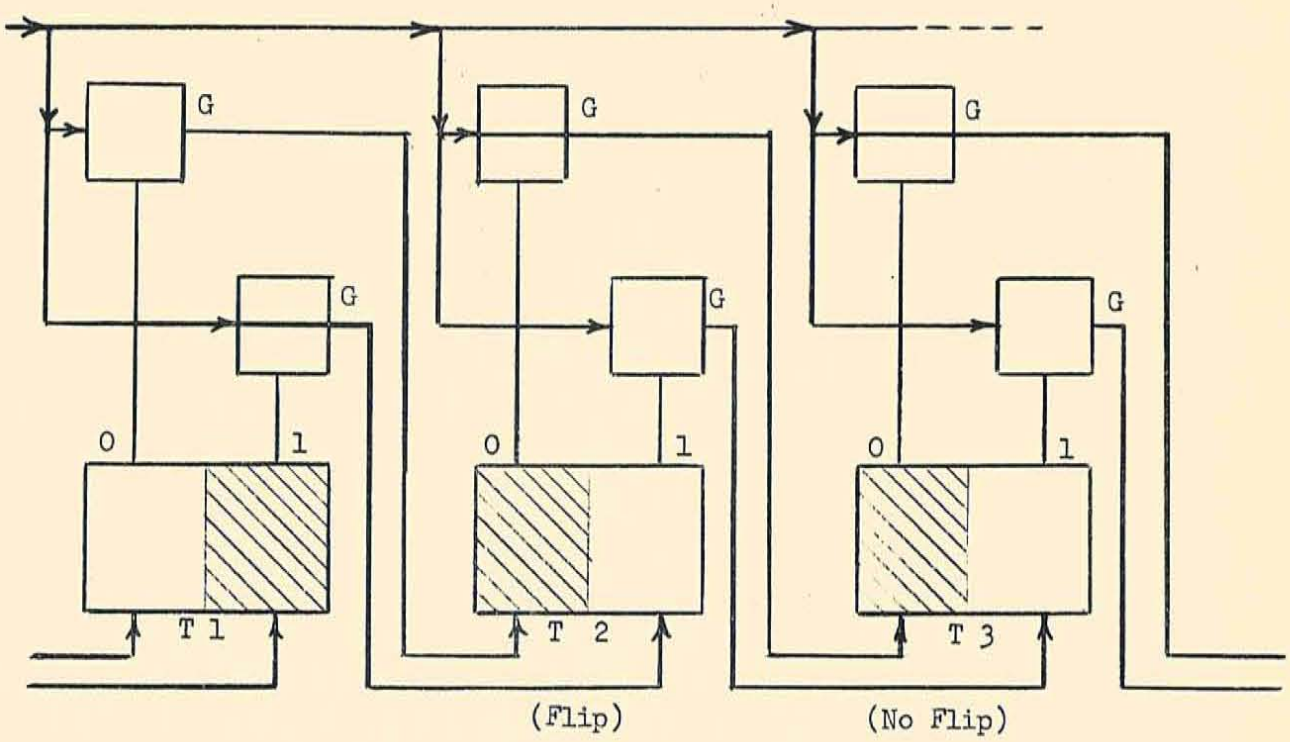

Figure 9. Gate-type Shifting Register
(3 stages of one channel)

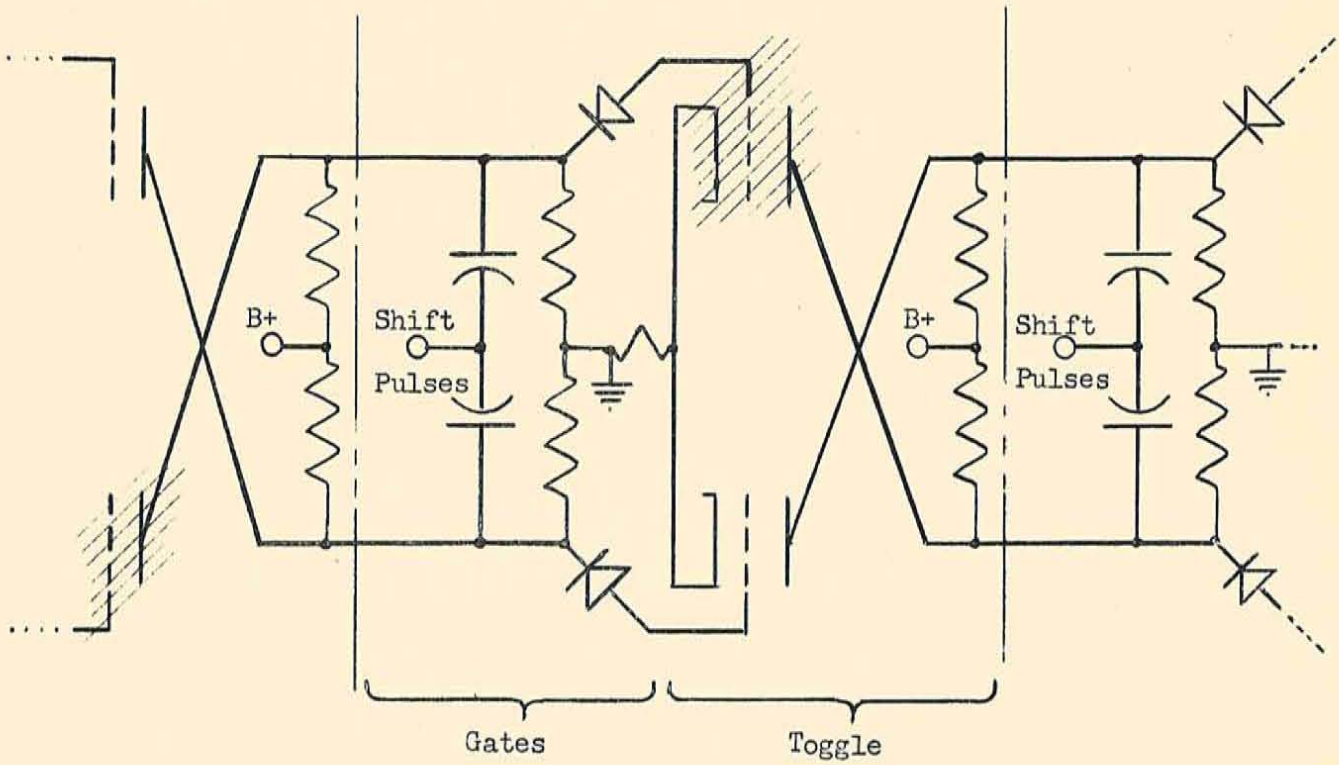

Figure 10. Register Circuit
(One stage of one channel)

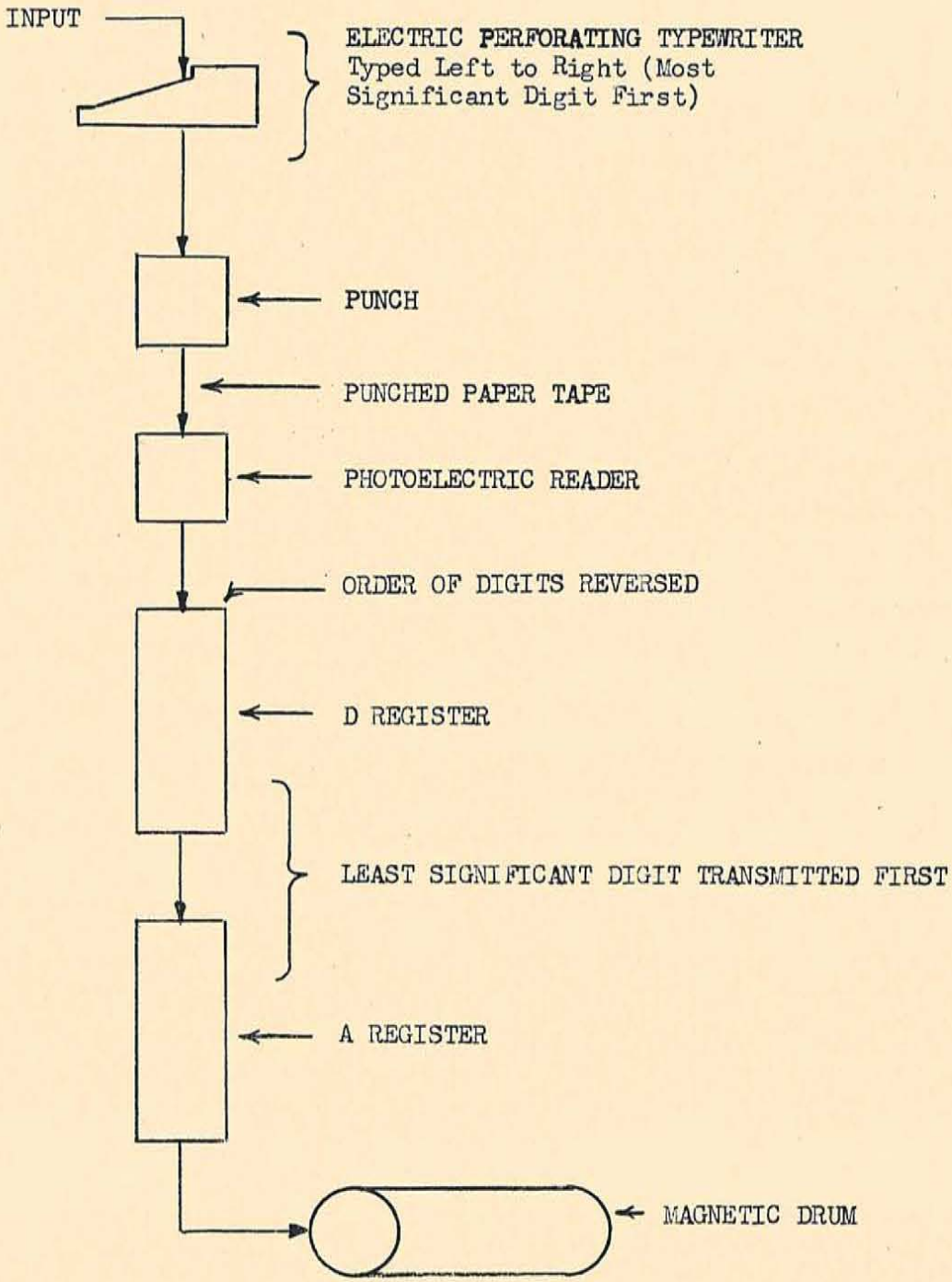

Figure 11. Diagram of Input Mechanism

Status

The completed computer will contain about 1300 tubes (half of them in the memory circuits) with about 2100 separate cathodes. In addition about 1300 crystal diodes will be used. About half of the panels of the computer have been completed and most of them are in operation at this writing (September 1, 1950); they are shown in Figure 7. These panels contain about 75% of the tubes and 50% of the crystal diodes. They comprise the memory, reading, writing, and address-selection circuits, one of the arithmetic registers and the order counter, in addition to parts of the control. Another register has been built and is ready to install except for the end columns which will incorporate the adder. The input mechanism is complete except for the photoelectric tape reader which is under construction.

No extended life or reliability tests have been made on the system as yet, but precession experiments have been carried out on the memory, one band at a time. These required reading and writing numbers from an arithmetic register into a sequence of specified locations at the rate of about 60 operations per second. These experiments have operated for periods of four hours or more before shutting down without failure.

Completion of the construction and beginning of overall testing and operation on practical problems is scheduled for January 1951.