XEROX **Internal Memo**

To
Ed Da Silva

From
Bo Sramek
CPT-77-6604

Subject
Janus Clock Distribution Rules

Date
September 29,1977.

This memo is an extension of memo CPT-77-6565, part of which is enclosed as an appendix.

There will be only three critical clocks distributed via low impedance transmission lines at the back panel: EDGE CLOCK (the most critical), RAM CLOCK and CYCLE 0 CLOCK.

These three clocks have special drivers located on a PC board in location J1, physically close to corresponding edge connector pins (location PK,NK or NL). The clocks for CPU Control (J1) are tapped from edge connector pins. The special clock drivers will be discrete for first version of layout with probable change into hybrid DIPs, phased in later. (Fig. 2)

The transmission lines terminating resistors (33 Ohms/0.5W) are located on the back plane close, or at, the connector location J16. The +5V end of each terminating resistor is bypassed to GND by 0.1uF (maintaining very short leads both of terminating resistors and bypassing capacitors is essential). (Fig. 3)

Other clocks (noncritical ones) are handled and distributed as regular TTL signals, following standard loading and distribution rules.

The critical clocks use the same S00 package (transmission line tap package), located nearest the edge connector pins assigned for critical clocks (location PL or PK on the PC board). (Fig. 1) The pin assignment of transmission line tap package is the same on all boards:

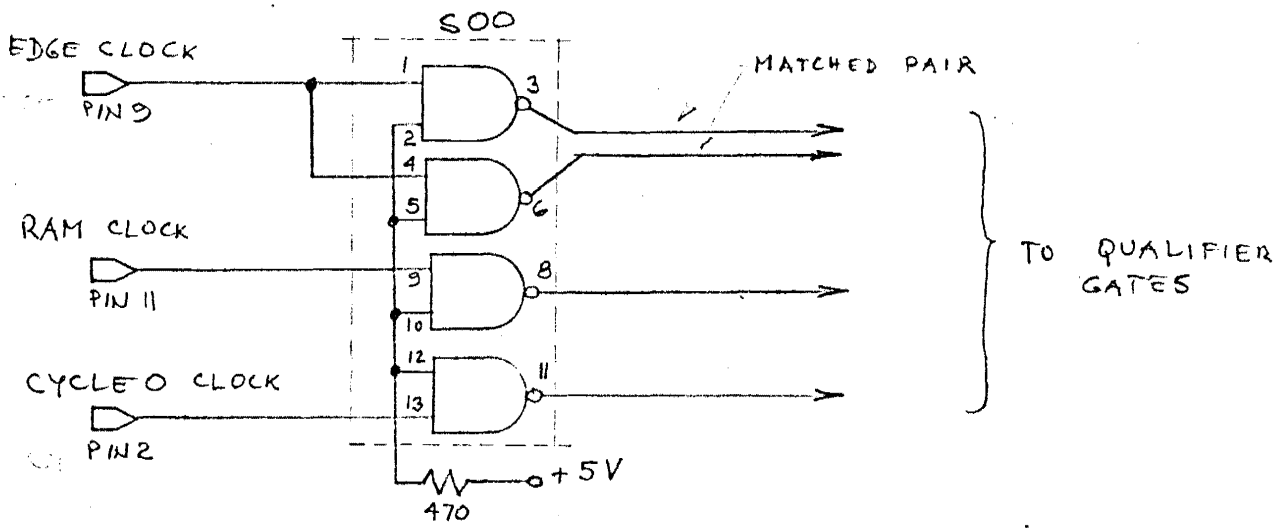


Fig. 1

Janus Clock Distribution - Continuation

The special clock drivers for low impedance transmission line are described in the enclosed appendix memo.

The qualifier gates for all clocks are located as close as possible to the physical center of each PC board. The most critical edge clock qualifier gates are arranged in a square pattern in the center and the remaining qualifier gates immediately surrounding them. (Refer to fig. 4). Clock signal from qualifier gates should be routed serially to various flip-flops and register in each board subdivision.

The edge clock tap package uses two gates (see fig.1) to feed sufficient number of qualifier gates (output pins 3 and 6). It is mandatory, that the connections from outputs 3 and 6 to two groups of edge clock qualifier gates are run as a matched pair.

If there would have been any questions concerning the clock layout or distribution, do not hesitate to call me. (Ext. 2624).

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Distribution:

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C. Tseng
P. Vysin
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XEROX **Internal Memo**

To
Brian Rosen

From
Bo Sramek, X2624
CPT-77-6565

Subject
Janus Clock Distribution

Date
9/16/77

Enclosed you will find some measured data on proposed low impedance transmission line clock distribution scheme.

Assumption was that there will be 16 boards maximum, plugged into the back plane at 0.7" intervals.

The distribution scheme addresses itself mostly to EDGE CLOCK distribution, but is, obviously applicable to remaining clocks, as well.

It was also assumed that maximum load of any board to any low impedance transmission line at one location is <u>two</u> $T^2L$ gates (one is even better).

Each load was simulated with 2k resistor to +5V and 7.5pF capacitor to ground (hence 16 times 1k/15pF for 16 boards).

The transmission line was simulated with a insulated wire run as close as possible to solid ground plane. The estimated impedance of the etched unloaded run is in the vicinity of 75 Ohms; together with 1k/15pF @ 3ns rise time pulses, the overall impedance of the transmission line is between 30 and 40 Ohms (hence 33 Ohm pullup for far end termination and two 68 Ohm pullups at both ends for the case of driving the transmission line from the middle.)

The clock generator itself consists of three discrete transistors (the transistor types used are the same as in X-WIRE Transceiver) and several resistors and bypassing capacitors.

If any questions, please do not hesitate to call me (note my new extension).

Bs

Distribution:

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# PROPOSED CLOCK GENERATOR
(TO BE LAID OUT ON BOARD J1)

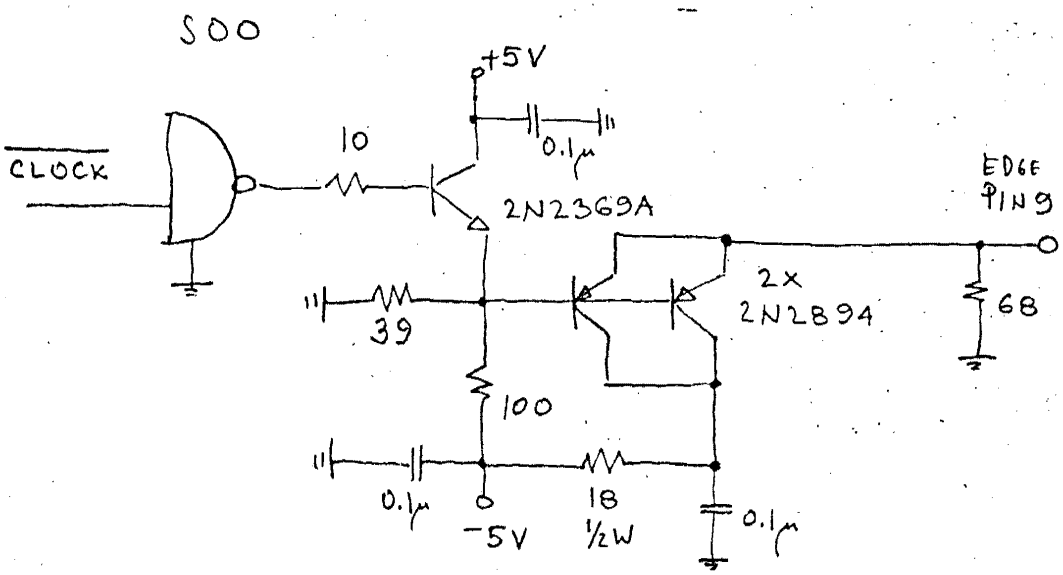


fig. 2

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Bo

# PROPOSED CLOCK DISTRIBUTION SCHEME

(CLOCK GENERATOR LOCATED AT ONE END OF THE BACK PLANE)

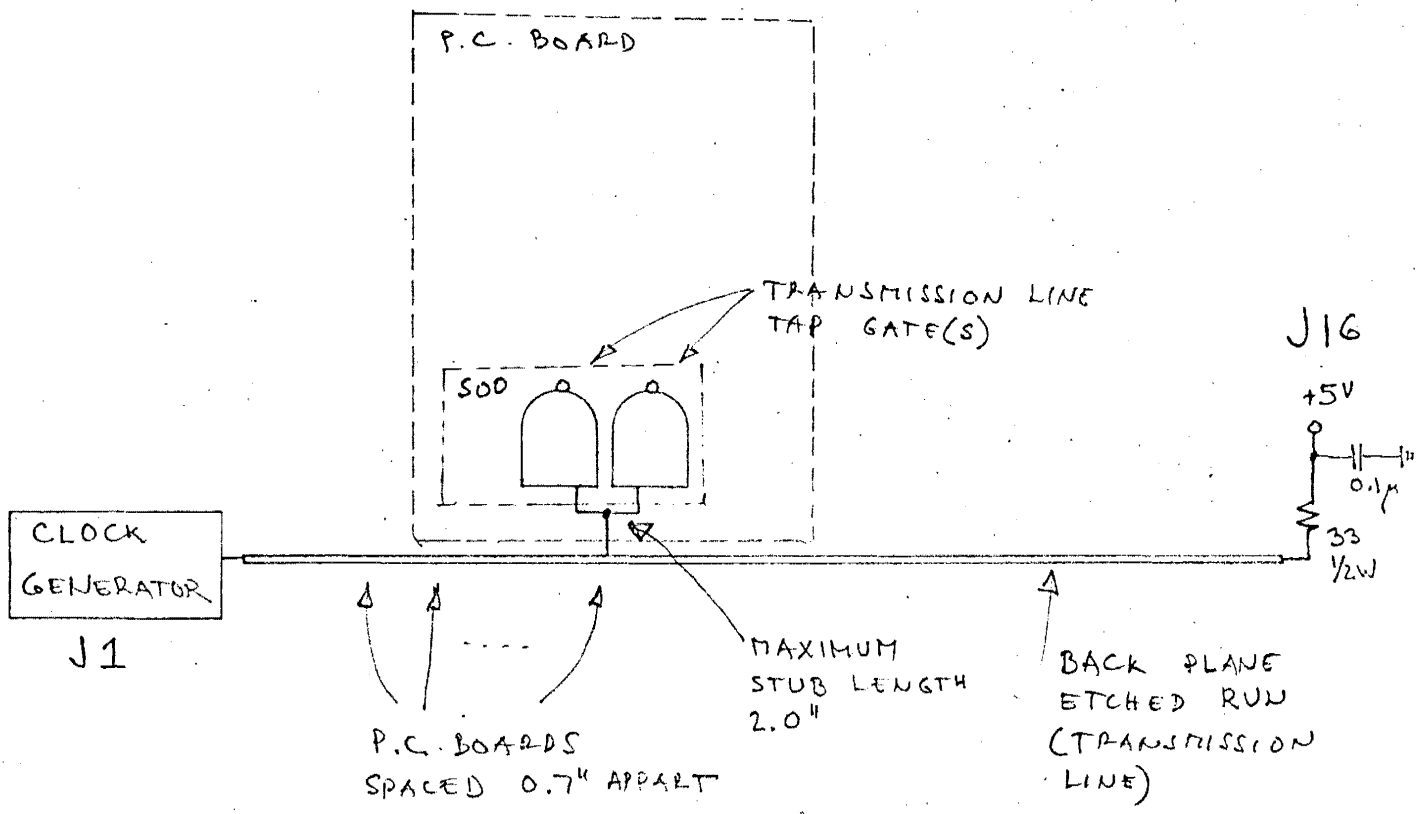


Fig. 3

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P.C. BOARD ASSIGNED LOCATIONS OF TAP AND QUALIFIER GATES

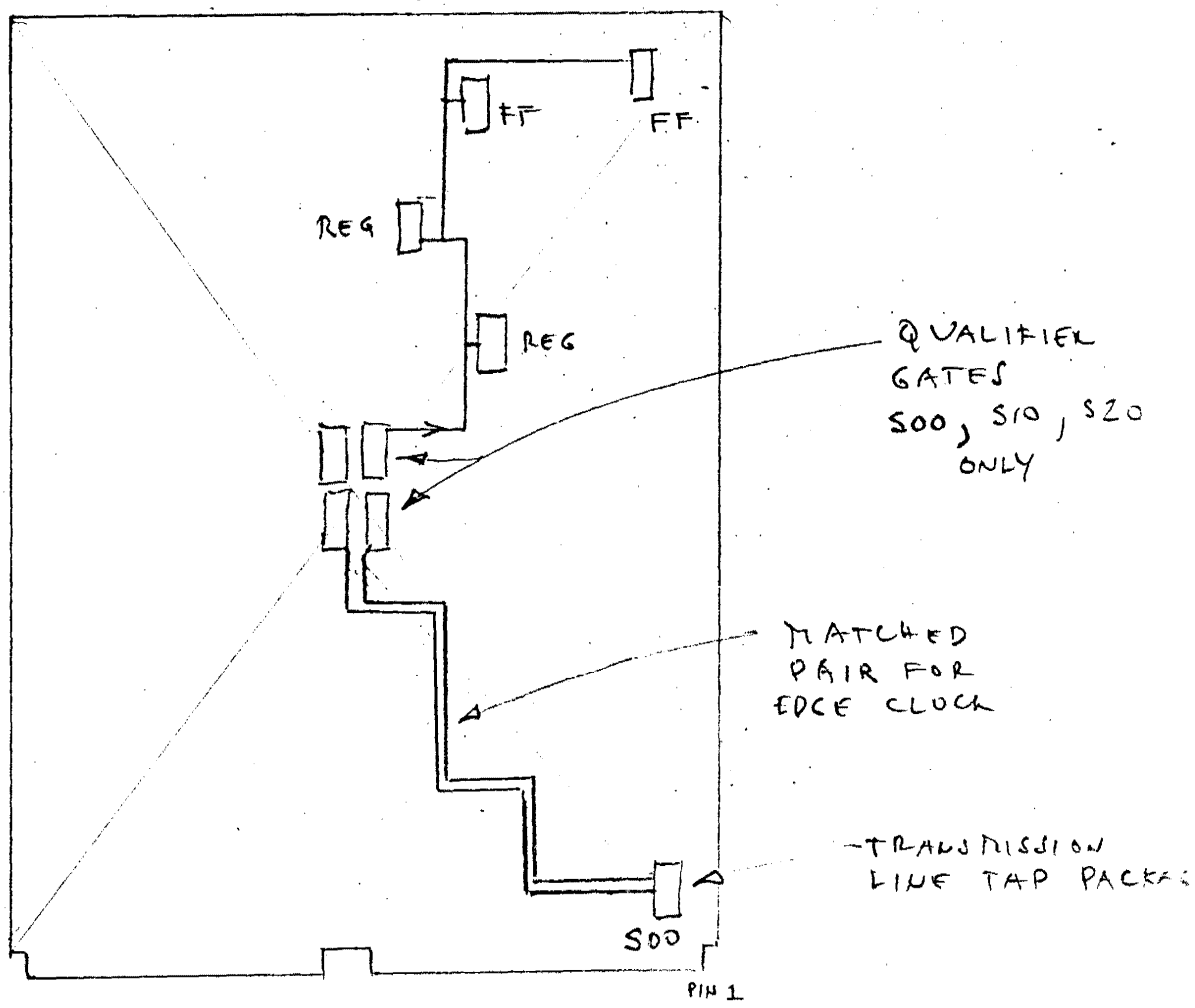


FIG. 4.