Individual Learning Program

In

DIGITAL TECHNIQUES

703-8

DIGITAL TECHNIQUES
EE-3201

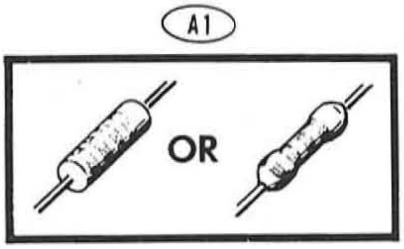
PARTS LIST

This parts list contains all of the parts used in experiments which you will perform with this course. The key number in the parts list corresponds to the numbers in the parts pictorial. Some parts are packaged in envelopes. Except for this initial parts check, keep these parts in their envelopes until they are called for in the experiment. A container is provided so that you can keep the small parts together in one place.

KEY No.	PART No.	QTY.	DESCRIPTION

RESISTORS (5%)

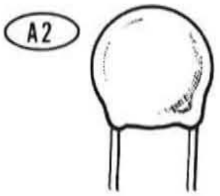
A1	6-102	2	1000 Ω 1/2 watt (brown-black-red)
A1	6-472	4	4700 Ω 1/2 watt (yellow-violet-red)
A1	6-103	2	10 kΩ 1/2 watt (brown-black-orange)
A1	6-473	2	47 kΩ 1/2 watt (yellow-violet-orange)
A1	6-224	1	220 kΩ 1/2 watt (red-red-yellow)
A1	6-151	1	150 Ω 1/2 watt (brown-green-brown)
A1	6-561	1	560 Ω 1/2 watt (green-blue-brown)



CAPACITORS

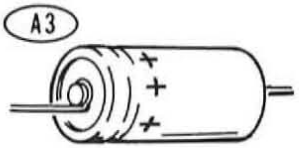
Disc

A2	21-47	2	.01 μF
A2	21-140	2	.001 μF



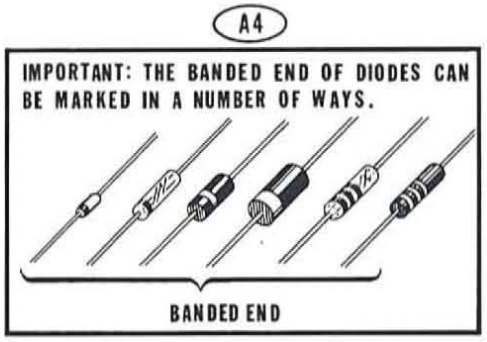
Electrolytic

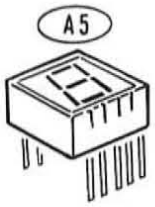
A3	25-111	2	1000 μF

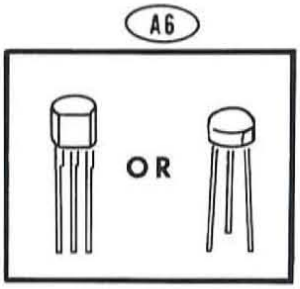


DIODES-TRANSISTORS-LIGHT EMITTING DIODE DISPLAY

	A4	56-56	4	1N4149 silicon diode
	A5	411-819	1	7 segment LED display
	A6	417-801	2	MPSA20 transistor





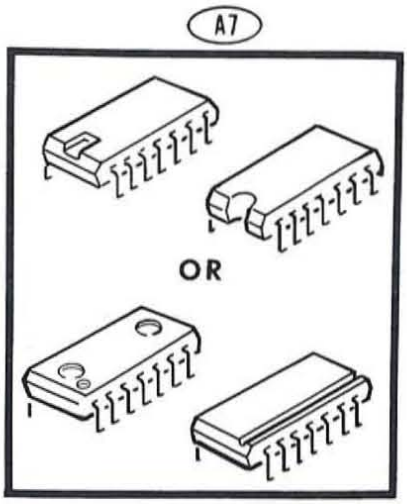


INTEGRATED CIRCUITS

NOTE: Transistors and integrated circuits are marked for identification in one of the following ways:

1. Part number.
2. Type number.
3. Part number and type number.
4. Part number with a type number other than the one listed.

	A7	443-1	2	SN7400N
	A7	443-2	1	SN420N (7420)
	A7	443-629	1	SN7490AN
	A7	443-13	1	SN7475N
	A7	443-16	2	SN7476N
	A7	443-18	1	SN7404N
	A7	443-25	1	SN74151N
	A7	443-46	1	SN7402N
	A7	443-53	1	SN7442N
	A7	443-54	1	SN7403N
	A7	443-90	1	SN74123N
	A7	443-612	1	SN74193N
	A7	443-680	1	SN7495AN
	A7	443-694	1	UA9368
	A7	443-695	1	CD4001
	A7	443-698	1	SN7486N



MISCELLANEOUS

	266-962	1	Small parts container

INDIVIDUAL LEARNING PROGRAM IN DIGITAL TECHNIQUES

EE-3201

COURSE OBJECTIVES AND OUTLINE

COURSE OBJECTIVES

When you complete this program, you will have the following skills and knowledge. You will be able to:

1. Discuss the advantages and benefits of using digital techniques in electronic equipment.

2. Name the major applications of digital techniques in electronics.

3. Convert between the binary and decimal number systems and recognize the most commonly used binary codes.

4. Name the major components used in implementing digital circuits and explain how they operate.

5. Explain the operation of digital logic gates.

6. Identify the more commonly used integrated circuit families used in digital equipment and discuss their operation, characteristics, and features.

7. Use Boolean Algebra to express logic operations and minimize logic circuits in design.

8. Explain the operation of flip-flops.

9. Discuss the operation and application of binary and BCD counters, shift registers and other sequential logic circuits.

10. Name the most frequently used combinational logic circuits and explain their operation.

11. Design both combinational and sequential logic circuits for a given application from definition and concept to the selection of the integrated circuits.

12. Discuss the operation and application of digital counters in time and frequency measurements.

13. Explain how a digital computer is organized and how it operates.

14. Discuss microprocessors, explain their operation and give examples of their applications.

COURSE OUTLINE

UNIT 1 Introduction to Digital Techniques

- Introduction
- Unit Objectives
- Unit Activity Guide
- Digital Techniques
  - Contrasting Analog and Digital Devices and Techniques
  - Where are Digital Techniques Used?
    - Communications
    - Telemetry Systems
    - Test Instruments
    - Industrial Controls
    - Consumer Electronic Equipment
  - Why Use Digital Techniques?
    - Greater Accuracy
    - Greater Dynamic Range
    - Greater Stability
    - Convenience
    - Automation
    - Design Simplicity
    - New Approaches
- The Binary Number System
  - Positional Number Systesm
  - Fractional Numbers
  - Converting Between the Binary and Decimal Number Systems
    - Binary to Decimal
    - Decimal to Binary
  - Binary Number Sizes
  - Number Identification
- Binary Codes
  - Binary Coded Decimal
  - Special Binary Codes
    - Excess 3 Code
    - Gray Code
    - ASCII Code
- Data Representation
  - Electromechanical Devices
  - Transistors
  - Magnetic Cores
  - Logic Levels
  - Positive and Negative Logic
  - Parallel vs Serial Data Representation
  - Logic Circuits
- Unit Summary
- Examination
- Answers

UNIT 7 Sequential Logic Circuits: Counters, Shift Registers, and Clocks

UNIT 10 Digital Applications (continued)

ILLUSTRATIONS FOR AUDIO RECORDS

UNIT 1, Record 3, Side 1

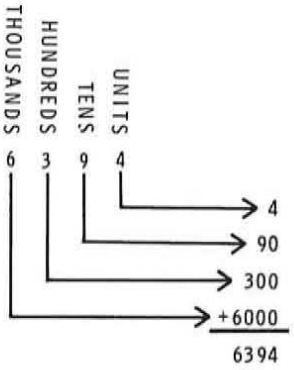


Figure A

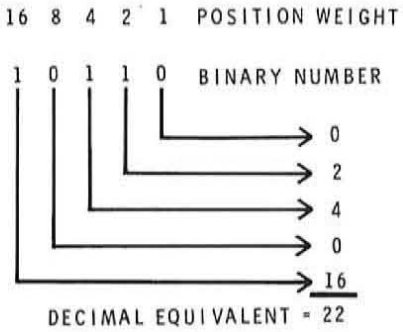


Figure B

DECIMAL	BINARY			
	8	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Figure C

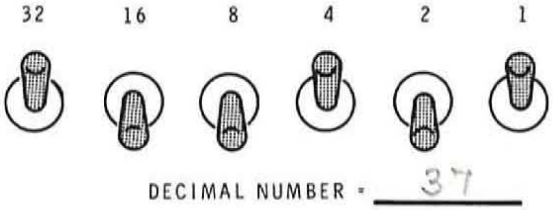


Figure D

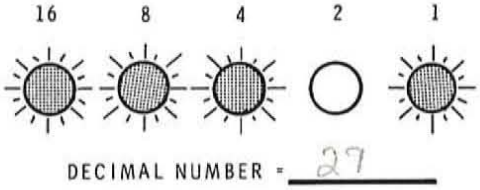


Figure E

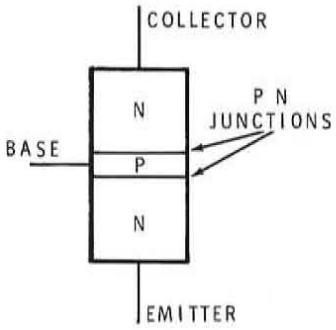


Figure A

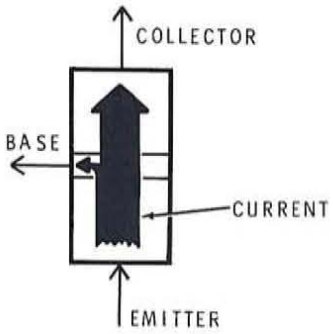


Figure B

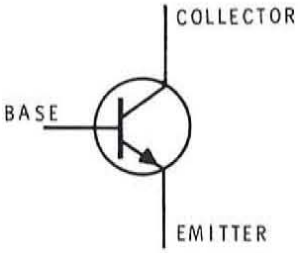


Figure C

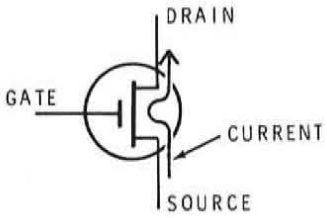


Figure D

UNIT 3, Record 4, Side 1

Figure A

Figure B

Figure C

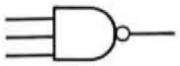


Figure D

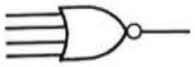


Figure E

UNIT 6, Record 5, Side 2

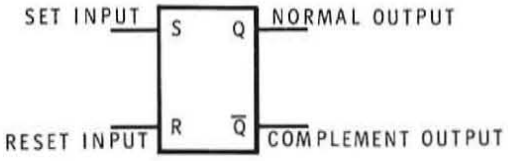


Figure A

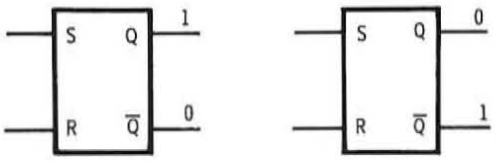


Figure B

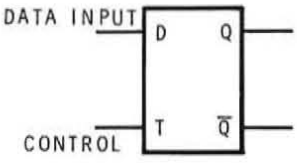


Figure C

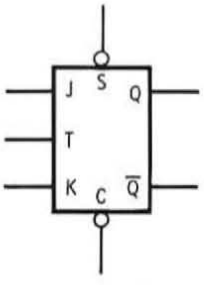


Figure D

Heathkit
ZENITH Educational Systems

UNIT 1

INTRODUCTION TO DIGITAL TECHNIQUES

EE-3201

HEATH COMPANY
BENTON HARBOR,
MICHIGAN 49022

CONTENTS

UNIT 1

INTRODUCTION TO DIGITAL TECHNIQUES

INTRODUCTION

The purpose of this first unit on digital techniques is to give you an overview of the subject and to introduce you to the basic concepts. You will learn what digital techniques are, how they are used and why they are used. You will learn about binary numbers and codes which are the basic language of all digital systems. And finally, you will see how digital techniques are implemented with hardware.

This unit provides you with the background and base upon which you will build your knowledge of digital techniques. This foundation will put the concept of digital techniques into perspective so that you can fully relate them to the field of electronics. With the information presented here you will clearly understand the need for and uses of digital techniques.

Digital techniques are so widely used today that it is almost impossible to think of electronic equipment without them. Digital techniques are used in virtually every area of electronics. They have greatly improved electronic methods and have given us practical electronic equipment with amazing capability. And, there is potential for further improvements and advances. As an electronic engineer, technician, or hobbyist you can benefit by knowing digital techniques. This program will provide you with a solid understanding of digital methods and a guide to their application.

Examine the Unit Objectives listed in the next section to see what you will learn in this unit. Then follow the instruction in the Unit Activity Guide to be sure you perform all of the steps necessary to complete this lesson successfully. Check off each step as you complete it, and in the spaces provided, keep track of the time you spend on each activity.

UNIT OBJECTIVES

When you complete this Unit you will have the following knowledge and capabilities:

1. Given a list of physical variables, components, devices, and other items, you will be able to classify them as being either analog or digital in nature.
2. You will be able to list at least five advantages of digital techniques over analog methods.
3. You will be able to list at least five examples of electronic equipment using digital techniques.
4. You will be able to state the factors that have most influenced the growth of digital techniques.
5. Given any decimal number, you will be able to convert it into its binary equivalent.
6. Given any binary number, you will be able to convert it into its decimal equivalent.
7. Given any decimal number, you will be able to convert it into its binary coded decimal (BCD) equivalent.
8. Given a BCD number you will be able to convert it into its decimal equivalent.
9. Given a list of popular digital codes, you will be able to read and identify them including pure binary, BCD, Gray, excess 3, and ASCII.
10. You will be able to list the two key ways binary data is represented with digital hardware.
11. You will be able to list the advantages and disadvantages of both serial and parallel methods of binary data transmission.

UNIT ACTIVITY GUIDE

	Completion Time
☐ Play audio record: Side 1, Introduction to Digital Techniques, Unit 1.	_____
☐ Read section Digital Techniques: Pages 1-6 to 1-16.	_____
☐ Answer Self Test Review Questions 1-6.	_____
☐ Read section The Binary Number System: Pages 1-19 to 1-26.	_____
☐ Answer Self Test Review Questions 7-13.	_____
☐ Read section Binary Codes: Pages 1-29 to 1-35.	_____
☐ Answer Self Test Review Questions 14-21.	_____
☐ Read section Data Representation: Pages 1-38 to 1-43.	_____
☐ Answer Self Test Review Questions 22-27.	_____
☐ Complete the Unit Summary.	_____
☐ Complete the Unit Examination.	_____
☐ Construct Heathkit ET-3200 Digital Design Experimenter.	_____

DIGITAL TECHNIQUES

There are two basic types of electronic signals and techniques, analog and digital. Analog signals are the most familiar type. An analog signal is an ac or dc voltage or current that varies smoothly or continuously. It is one that does not change abruptly or in steps. An analog signal can exist in a wide variety of forms. Several types of analog signals are shown in Figure 1-1.

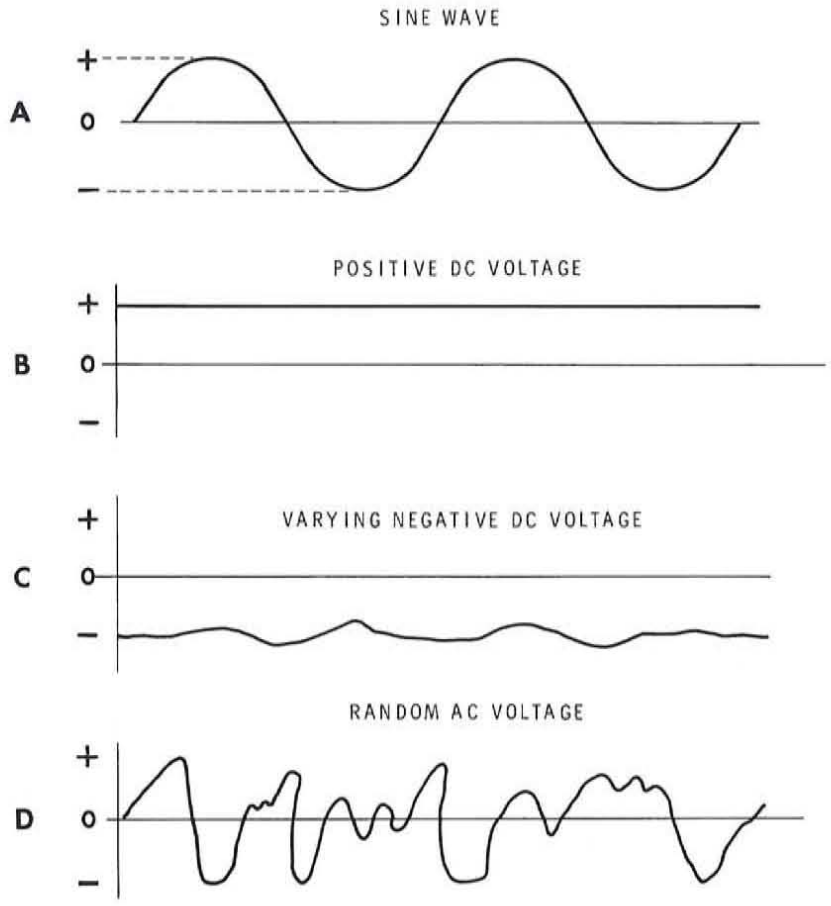


Figure 1-1
Types of Analog signals

Figure 1-1A shows the most common type of analog signal, a sine wave. A significant number of electronic signals are sinusoidal. Radio signals and audio tones are examples. A fixed dc voltage is also an analog signal. Figure 1-1B shows a constant positive dc voltage. Another type of analog signal is varying dc voltage or current. A changing negative dc voltage is illustrated in Figure 1-1C. Any random but continuously varying voltage waveform is considered to be analog. The signal shown in Figure 1-1D is only one of an infinite variety of such signals. Electronic circuits that process these analog signals are called linear circuits.

Digital signals are essentially a series of pulses or rapidly changing voltage levels that vary in discrete steps or increments. Digital signals are pulses of voltage that usually switch between two fixed levels. Figure 1-2 shows several types of digital signals. Notice how these signals switch between two distinct voltage levels. In Figure 1-2A, the two levels are 0 (ground) and +5 volts. In Figure 1-2B, the levels are 0 (ground) and −6 volts. In Figure 1-2C the signal alternates between the +3 and −3 volt levels. This two-level, off-on or up-down fast switching characteristic is fundamental of all digital signals. Electronic circuits that process these digital signals are called digital, logic, or pulse circuits.

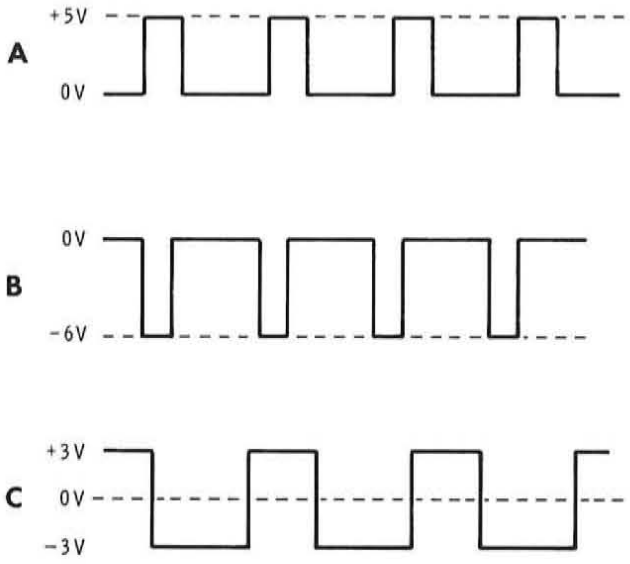


Figure 1-2
Types of Digital signals

Contrasting Analog and Digital Devices and Techniques

Now let's further define analog and digital methods in terms of devices and ideas that are already quite familiar to you. For example, a light bulb can be either an analog or digital device depending upon how it is used. The amount of current through a light bulb can be set to any level less than its maximum rated value. We can vary the current through it continuously and its brightness will vary. Used in this way the light bulb is an analog device. The brilliance of the lamp is proportional to the current through it. There are virtually an infinite number of brightness levels.

The lamp can also be used as a digital device where the current through it and its brightness varies in discrete steps. The most common way of using the light bulb as a digital device is to give it two brilliance levels, usually off and on. The important point is that the lamp has two states. Because of this off-on characteristic, we say that the lamp is binary in nature. The term binary designates any two-state device or signal.

Let's take some other examples to illustrate the concept of analog and digital techniques. The VHF channel selector switch on your television set is digital in nature because it can assume only discrete positions. It can be set to any one of thirteen unique states, channels 2 through 13 and UHF. Any type of switch is a digital device because it has two or more discrete positions.

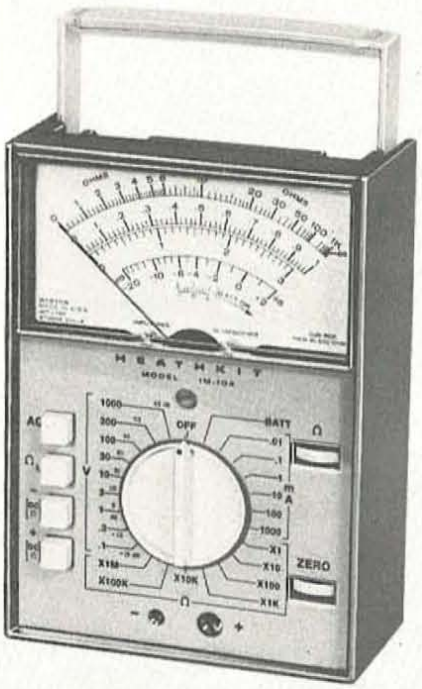
The volume control on your television set is an analog device. You can vary the volume of the sound continuously over a wide range from completely off to extremely loud.

The speedometer on your car is an analog device. It tells you the speed of your car in miles per hour on a smooth and continuously varying basis. You read the speed from a dial that is usually calibrated in no smaller increments than 5 miles per hour. To determine the speeds between the markings you must interpolate, or guess at, the exact speed.

The odometer portion of your speedometer, the part that indicates the number of miles traveled, is a digital device. Since the odometer records mileage in increments of one mile (or in some cases one-tenth mile), it is digital in nature.

Another example of an analog device is a typical clock or watch. It indicates the time continuously by the positions of the hands on a calibrated dial. The second hand sweeps smoothly and continuously around in an analog fashion as do both hour and minute hands. To determine the exact time, you must estimate the positions of the hands. Your ability to read the time accurately is limited by the precision of the dial calibration increments. Digital clocks overcome this problem. On a digital clock, you read the time directly from decimal number display readouts in discrete increments of hours, minutes and seconds. The accuracy is greatly improved and you gain the added convenience of a direct number display.

A standard voltmeter is also an analog device. It reads or measures voltage and indicates its value by the position of a pointer on a meter scale. The pointer moves smoothly or continuously as the amplitude of the analog voltage being measured varies. Of course, digital voltmeters are also available. These instruments measure the voltage and display it as discrete digits on a decimal readout.



An analog multimeter for measuring voltage, current and resistance

A typical digital multimeter

Here are a few other analog quantities and devices.

temperature — thermometer
direction — compass
light intensity — light meter

Keep in mind that all of these variables could be monitored and displayed as a digital readout.

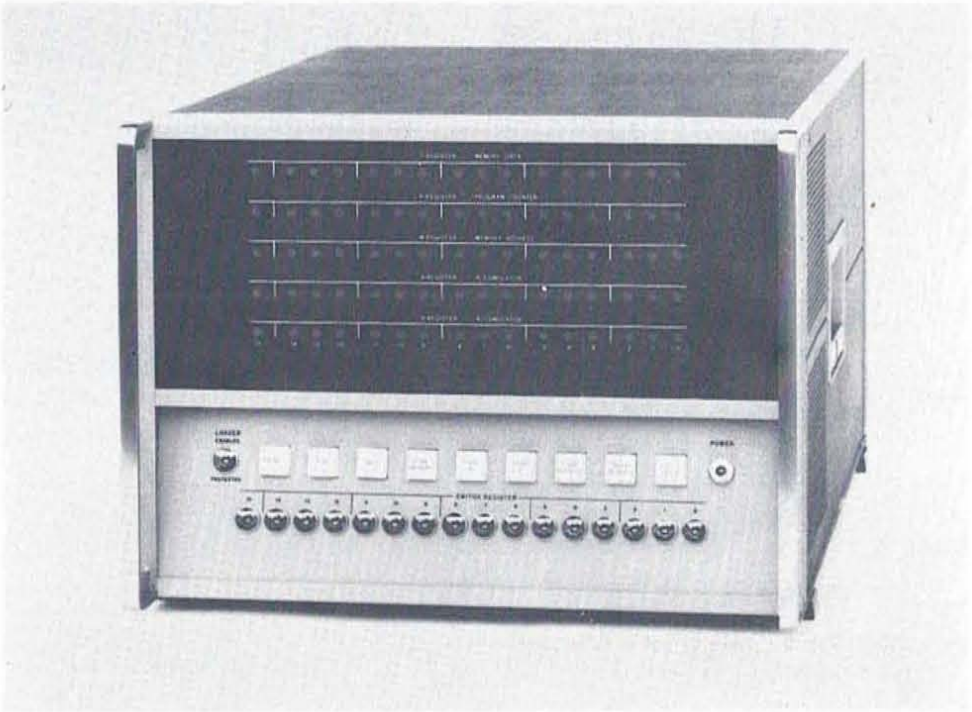
Further examples of digital variables are:

money
heart pulse rate

Where Are Digital Techniques Used?

Perhaps the greatest use of digital techniques today is in computers. Digital computers are used in virtually all areas of business and industry. They are extremely useful machines that can save man a tremendous amount of effort and greatly extend his capabilities.

Over the years digital computers have grown in capability, but have become smaller, cheaper and easier to use. As a result, their use has increased tremendously. The small, low-cost but very powerful minicomputer has put digital and computer techniques within the reach



A typical minicomputer. (Photo courtesy Hewlett-Packard)

of nearly everyone. A minicomputer can be quickly and easily designed into a system to replace more conventional equipment and circuitry for control, computation and automation.

Advanced semiconductor technology has recently given us a computer that is really a component. Known as microprocessors, these devices are complete digital computers in a single miniature integrated circuit package. Microprocessors can replace minicomputers in many applications and can often be used to replace conventional digital circuits. Like all digital computers, the microprocessor must be programmed to carry out its specified function.

But computers aren't the only application for digital techniques. Digital methods are being employed in almost every imaginable area of electronics. Here are just a few examples.

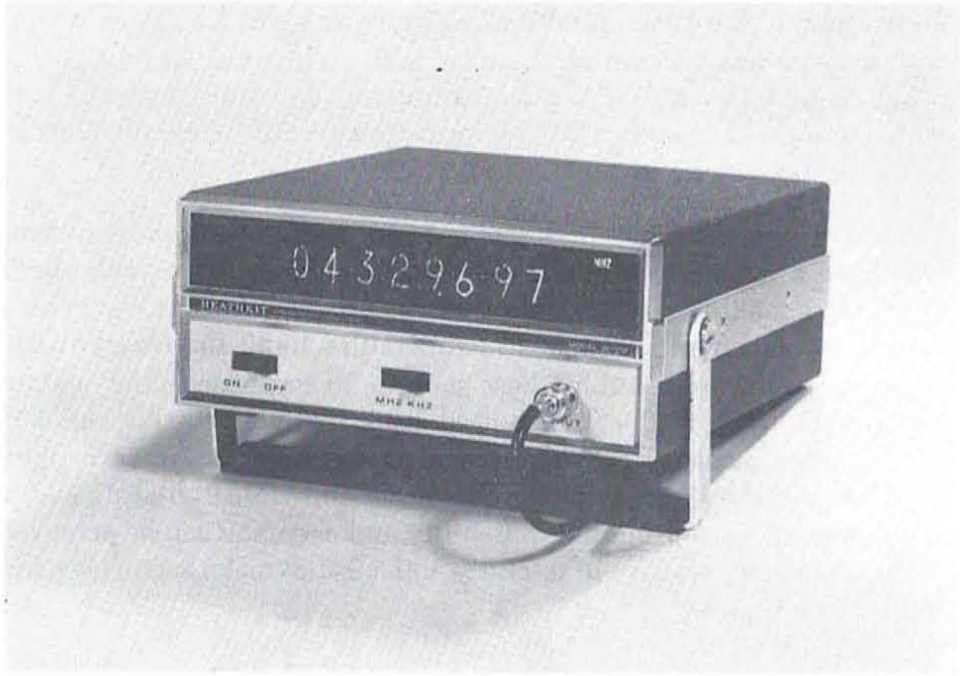
Communications. Instead of transmitting information over wire lines or by radio by analog methods, much data is now being transmitted in digital form. It has been found that pulse type signals are easier to work with and are less susceptible to noise and other problems common in communications systems. Digital computers can readily communicate with one another by transmitting information over the telephone lines by using digital techniques.

Telemetry systems. Those systems used for transmitting measurement data from a remote location, use digital techniques extensively. In an unmanned satellite, for example, sensors are used to monitor various environmental conditions such as temperature, light, and radiation.The analog voltages produced by these sensors, in response to the quantity being measured, can be transmitted back to the earth via radio by modulating a carrier using conventional analog methods. However, it has been found that by converting the analog variables into digital signals, an improvement in transmission reliability and accuracy can be achieved. Today, telemetry systems in satellites and missiles make extensive use of digital techniques.

Test Instruments. The trend in test and measurement equipment is clearly toward the use of digital techniques. Besides the convenience of a direct decimal display and the increased precision of measurement brought about by the use of digital techniques, it is possible to interface many digital instruments with a computer. This permits automatic monitoring, controlling, measuring and recording of data.

The most common electronic test instrument, the analog voltmeter, is gradually being replaced by the more sophisticated digital voltmeter (DVM). The DVM does the same job as its analog counterpart. The DVM measures voltage but instead of presenting the reading to the observer in the form of a pointer on a meter face, the voltage is a direct readout display of decimal numbers. Such an instrument, while generally higher in cost than an analog voltmeter, is extremely convenient to use and read. More important, it gives more accurate measurements of voltages. The digital multimeter (DMM), a DVM with refinements, is capable of measuring voltages as well as resistance and current like an analog VOM.

Another widely used digital test instrument is the electronic counter. This unit is widely used for measuring frequency and time intervals. Again the digital techniques provide a convenient decimal read-out of the exact quantity being measured, thereby eliminating man's need to interpolate continuous or analog meter scales to provide a reading. This result is greater accuracy and less error in measurement.



A digital counter used for measuring frequency. (Heath Co.)

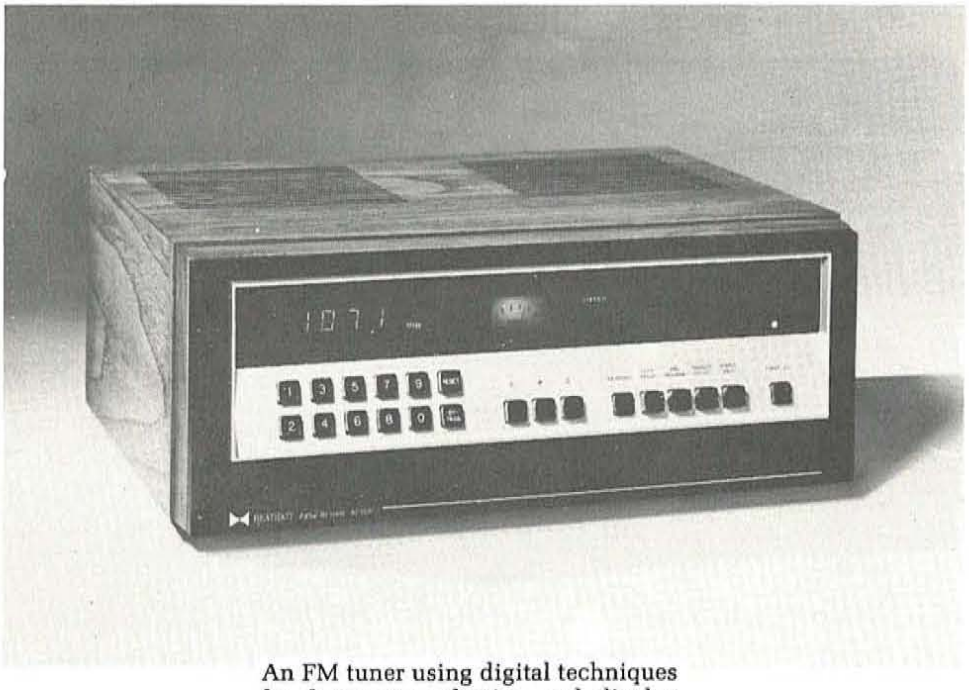
Industrial Controls. Digital techniques are becoming more widely used in manufacturing plants and refineries where complex operations must be accurately controlled. These systems use sensors to monitor various phases of the operation, and the outputs of these sensors are then used to produce signals that will control the various operations that affect the process.

Industrial feedback control systems have traditionally used analog techniques. Today, many of these control systems are digital in nature. Most involve both analog and digital methods. Analog quantities like temperature, pressure, liquid level and flow rate are monitored by sensors to produce an analog signal. These are converted into digital values by analog-to-digital converters. Other system inputs are already digital in nature such as limit switches or sensors of an off-on or go no-go nature.

All of this digital information is fed into a digital computer which monitors the input variables and according to a predetermined program generates output signals to control the process.

Another popular industrial application for digital techniques is machine tool control. Here a digital computer controls the drilling, cutting, punching and stamping of materials to produce specific metal parts accurately and automatically.

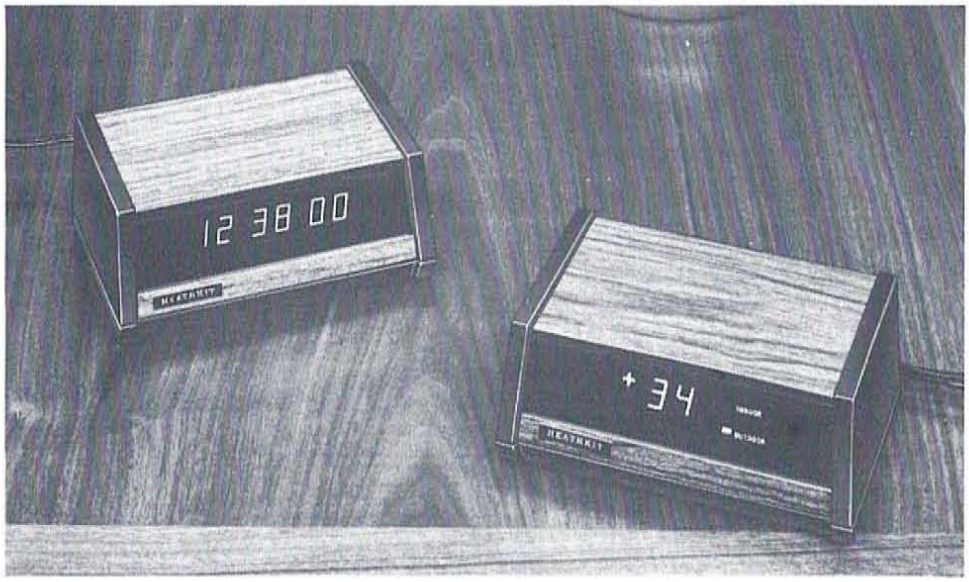
Consumer Electronic Equipment. Perhaps the biggest holdout against the use of digital techniques has been common consumer items such as radio, TV, hi-fidelity and other products. The higher cost of some digital methods has been the major reason for the delay in adopting these techniques. However, as prices of digital circuits have dropped, even these products have given way to the use of digital techniques. An example is the circuitry for digital channel selection used in some of the newer color television sets. Some hi-fi receivers use digital frequency synthesizers for tuning.



An FM tuner using digital techniques for frequency selection and display (Heath Co.)

Other popular consumer devices using digital methods are the popular digital clocks and electronic calculators. Even a home digital thermometer is available.

Handheld electronic calculator using digital circuits (Heath Co.)



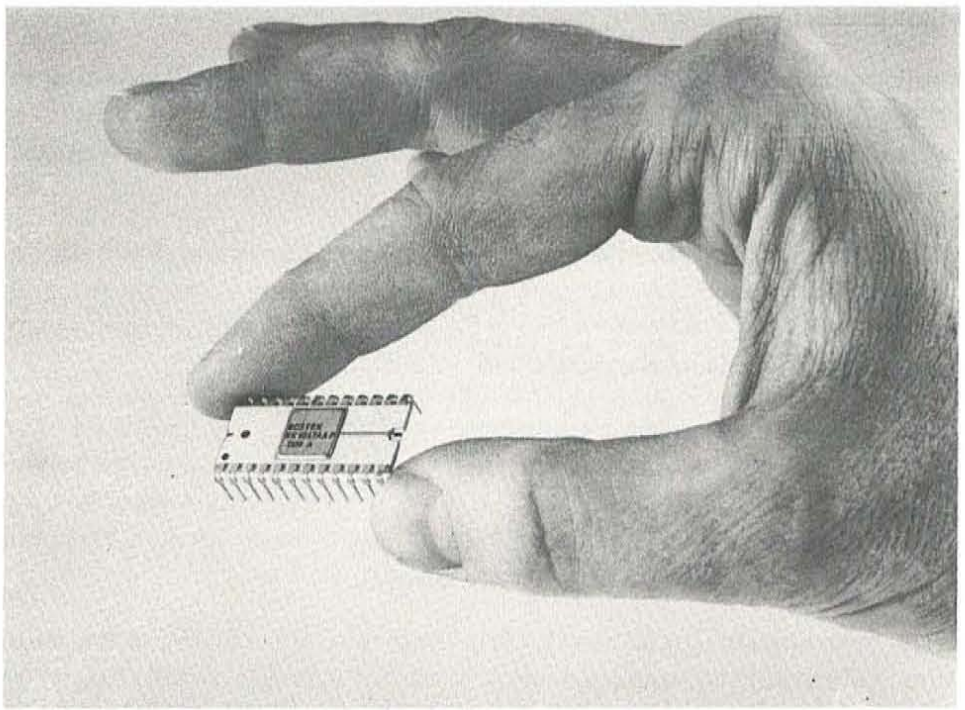
Digital clock and thermometer. (Heath Co.)

While consumer electronic devices will continue to use analog techniques, more digital controls and circuits will gradually be added to increase versatility and improve performance.

Where are digital techniques used? The answer is almost everywhere in electronics. And their use will increase. Why are digital techniques used? Digital methods are used basically to obtain greater resolution of measurement, control or calculation, and for convenience.

Why Use Digital Techniques?

The primary impetus for the widespread use of digital techniques has been the availability of low cost,digital integrated circuits (ICs). Advances in integrated circuit technology have produced many excellent low cost digital circuits. Such circuits are small, inexpensive and very reliable. The more recent medium scale and large scale (MSI and LSI) integrated devices can replace entire circuits and instruments. Electronic equipment designers recognize the availability of such devices and have begun to take advantage of them. While digital techniques have been known for years, it took integrated circuits to make them practical.



A large scale integrated circuit. (Photo courtesy MOSTEK).

By using digital IC's many equipment improvements have been made. Reductions in size, weight, cost and power consumption usually result when analog techniques are replaced by digital methods, thanks to digital IC's. Here are a few more reasons why digital techniques have become so popular.

Greater accuracy. Digital techniques permit greater precision and resolution in representing quantities or in making measurements than with analog methods.

Greater Dynamic Range. Dynamic range is the difference between the upper and lower data values that a system or instrument can handle. Analog systems are limited because of component capabilities and noise to a range of something less than 100,000 to 1. With digital techniques practically any desired dynamic range can be obtained.

Greater Stability. Analog or linear circuits are subject to the effects of drift and component tolerance problems. Temperature and other environmental factors affect resistor, capacitor and inductance values. Transistor biases vary causing non-linear operation and distortion to occur. Component imperfections and ageing cause drift and resultant problems. Digital methods greatly minimize or completely eliminate such problems.

Convenience. Digital techniques make instruments and equipment more convenient to use. The direct decimal display of data is not only more convenient, but the error of reading or interpolating analog meters or in setting analog dials is eliminated.

Automation. Many electronic processes can be fully automated if digital techniques are used. Special control circuits or a digital computer which are programmed can automatically, set up, control and monitor many operations. Data is readily recorded, stored and displayed.

Design Simplicity. Digital equipment is relatively easy to design. The available digital ICs make digital design a pleasure. Little or no breadboarding is required. In analog or linear circuits breadboarding is mandatory to ensure a workable circuit. Digital equipment can go from paper design to finished product in a very short time.

New Approaches. Digital methods permit new approaches to the solution of electronic equipment design. In addition, design solutions impossible with analog techniques are readily implemented with digital circuits. Digital circuits make it possible to do some things that have no analog equivalent.

Self Test Review

1. Analog Signals vary _____ while digital signals vary _____.
2. Identify the following items as being either analog or digital in nature.
   a. height of a human _____
   b. dice _____
   c. pages of a book _____
   d. typewriter _____
   e. barometric pressure _____
   f. slide rule _____
3. How many discrete voltage levels do most digital signals have? _____
4. The most widespread use of digital techniques is in _____.
5. List 3 advantages of digital methods over analog techniques.
   a. _____
   b. _____
   c. _____
6. The single factor most influential in the increased use of digital techniques was the
   a. recognition of the deficiencies in analog methods.
   b. development of integrated circuits.
   c. discovery of digital methods.
   d. developments resulting from the space program.

Answers

1. continuously (or smoothly), in steps (in discrete increments, etc.)
2. a. analog
   b. digital
   c. digital
   d. digital
   e. analog
   f. analog
3. Two (2)
4. computers
5. greater accuracy
   greater dynamic range
   convenience of direct decimal display
   and many others.
6. (b) development of integrated circuits

THE BINARY NUMBER SYSTEM

All digital circuits, instruments and systems work with numbers that represent specific quantities. For example, the analog voltage measured by a digital voltmeter is converted into digital form and displayed as a specific decimal number. The number that you enter into an electronic calculator is stored and used in the calculation you specify. The digital computer that prints your payroll check works with numbers, specifically your salary, the number of hours you work and the various deductions. As you can see, numbers or quantities are the basic source for an end product of most digital equipment. Figure 1-3 shows how most digital equipment accepts input numbers, processes them and generates number outputs. The actual form of the input and output numbers depends on the application. They may be in binary or decimal form. In some applications the input and/or output may be in analog form despite the digital processing.

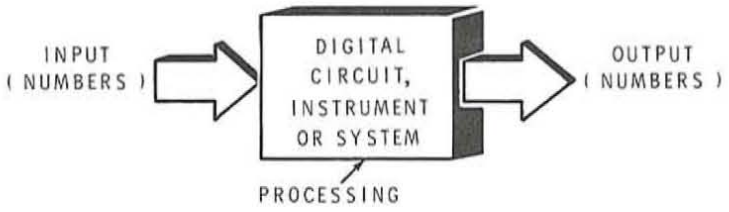


Figure 1-3 A general block diagram of any digital system

The type of numbers we are most familiar with are decimal numbers. In the decimal number system we combine the ten digits 0 through 9 in a certain way so that they indicate a specific quantity. In the binary number system, we use only two digits, 0 and 1. These binary digits, or bits, when appropriately arranged can also represent any decimal number. For example, the binary number 110101 represents the decimal quantity 53. All modern digital techniques are based on the binary number system.

The basic distinguishing feature of a number system is its base or radix. The base indicates the number of characters or digits used to represent quantities in that number system. The decimal number system has a base or radix of 10 because we use the ten digits 0 through 9 to represent quantities. The binary number system has a base of 2 since only the digits or bits 0 and 1 are used in forming numbers.

The decimal number system came about basically as a result of man having ten fingers. Man's earliest attempts to represent numbers, count and keep track of quantities involved the use of his fingers. Of course, the decimal number system is universally used and understood because it is our way of communicating information about quantities.

The binary number system, while simple, is inconvenient to use because we are not familiar with it. But once you learn it, you will find it easy to work with. It has special benefits when it comes to constructing the hardware used in digital equipment.

Digital systems can be implemented with either the decimal or binary number systems. However, the advantages of the binary number systems over the decimal number system in terms of hardware implementation are many. If we use the decimal number system, our hardware must have ten discrete steps or states each representing one of the digits 0 through 9. Various types of electrical, electromechanical, or electronic components and circuits are available to do this. A ten position rotary switch or a stepping relay are examples. However, when the binary number system is used, we only need to represent two states. An electronic component or circuit that has only two states is significantly simpler, less expensive, faster and more reliable than one with ten. Each bit can be implemented with components of a simple off/on nature such as switch or relay contacts or a transistor that conducts or does not conduct.

Positional Number Systems

The decimal and binary number systems are positional or weighted number systems. This means that each digit or bit position in a number carries a particular weight in determining the magnitude of that number. For example, you know that a decimal number has positional weights of units, tens, hundreds, thousands, etc. Each position has a weight that is some power of the number system base, in this case ten. The positional weights are $10^0 = 1$ (units)*, 10^1 (tens), 10^2 (hundreds), etc. We evaluate the total quantity represented by considering the specific digits and the weights of their positions. Consider the decimal number 7438 in which there are 8 ones, 3 tens, 4 hundreds, and 7 thousands. The number can be written as indicated below.

$$(7 \times 10^3) + (4 \times 10^2) + (3 \times 10^1) + (8 \times 10^0) =$$
$$7000 + 400 + 30 + 8 = 7438$$

To determine the value of the number, you multiply each digit by the weight of its position and add your results.

Binary numbers work the same way. Each bit position carries a specific weight. As in the decimal number system, the position weights are some power of the base of the number system. These weights from right to left are $2^0 = 1^*$, $2^1 = 2$, $2^2 = 4$, $2^3 = 8$, etc. The weight of each position is twice that of the weight of the number to the right. Consider the binary number 110101. This can be written as indicated below.

$$(1 \times 2^5) + (1 \times 2^4) + (0 \times 2^3) + (1 \times 2^2) + (0 \times 2^1) + (1 \times 2^0) =$$
$$32 + 16 + 0 + 4 + 0 + 1 = 53$$

The quantity represented by the number is determined by multiplying each bit by its position weight and obtaining the sum.

Fractional Numbers

So far we have only discussed whole numbers or integer quantities. But as you know it is often necessary to express quantities in terms of fractional parts of a whole.

Decimal fractions are numbers whose positions have weights that are negative powers of ten such as $10^{-1} = 1/10 = .1$, $10^{-2} = 1/100 = .01$, $10^{-3} = 1/1000 = .001$, etc. A decimal point separates the whole and fractional parts of a number. The integer or whole number portion is to the left of the decimal point and has weights of units, tens, hundreds, etc. The fractional part of the number is to the right of the decimal point and the positions have weights of tenths, hundredths, thousandths, etc. To illustrate this, the number 278.94 can be written as shown below.

$$(2 \times 10^2) + (7 \times 10^1) + (8 \times 10^0) + (9 \times 10^{-1}) + (4 \times 10^{-2}) =$$
$$200 + 70 + 8 + .9 + .04 = 278.94$$

In a fractional binary number, the weights of the fractional positions are negative powers of 2 or $2^{-1} = 1/2 = .5$, $2^{-2} = 1/4 = .25$, $2^{-3} = 1/8 = .125$, $2^{-4} = 1/16 = .0625$, etc. The position weight is one half of the weight of the position directly to the left. A binary point separates the whole and fractional parts of the number.

The binary number 1101.101 is evaluated as shown below.

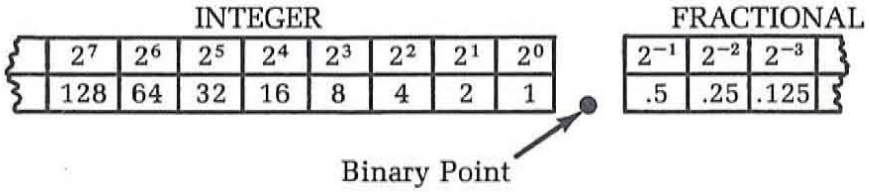
$$(1 \times 2^3) + (1 \times 2^2) + (0 \times 2^1) + (1 \times 2^0) + (1 \times 2^{-1}) + (0 \times 2^{-2}) + (1 \times 2^{-3}) =$$
$$8 + 4 + 0 + 1 + .5 + 0 + .125 = 13.625$$

*Any number with an exponent of zero is equal to one.

Converting Between The Binary and Decimal Number Systems

In working with digital equipment, you will often need to determine the decimal value of binary numbers. In addition, you will also find it necessary to convert a specific decimal number into its binary equivalent. Let's see how such conversions are accomplished.

Binary to Decimal. To convert a binary number into its decimal equivalent you simply add together the weights of the positions in the number where binary 1's occur. The weights of the integer and fractional positions are indicated below.



As an example, let's convert the binary number 1010 into its decimal equivalent. Since no binary point is shown, the number is assumed to be a whole number where the binary point is to the right of the number. The right-most bit, called the least significant bit or LSB, has the lowest integer weight of $2^0 = 1$. The left-most bit is the most significant bit (MSB) because it carries the greatest weight in determining the value of the number. In this example, it has a weight of $2^3 = 8$. To evaluate the number we add together the weights of the positions where binary 1's appear. In this example, 1's occur in the 2^3 and 2^1 positions. The decimal equivalent is ten.

Binary Number	1	0	1	0	
Position Weights	(8)	(4)	(2)	(1)	
Decimal Equivalent	8 +	0 +	2 +	0	= 10

As a further illustration of this process, let's convert the binary number 101101.11 into its decimal equivalent.

Binary Number	1	0	1	1	0	1	.1	1		
Position Weights	(32)	(16)	(8)	(4)	(2)	(1)	(.5)	(.25)		
Decimal Equivalent	32+	0+	8+	4+	0+	1+	.5+	.25	=	45.75

Note that you can disregard the position weights where binary 0s occur since they add nothing to the number value.

After you solve a few practice problems, you will quickly catch on to this procedure.

Decimal to Binary. Converting a known decimal number into its binary equivalent can be accomplished by a simple trial and error method once you are familiar with the weighting sequence of binary numbers. Suppose that you wish to convert the decimal number 175 into its binary equivalent. To do this you first determine the highest positional weight that is equal to or less than the number being converted. This is 128. Subtract 128 from 175 and note the remainder.

$$\begin{array}{r} 175 \\ -\ 128 \\ \hline 47 \end{array}$$

Again determine the highest positional weight that does not exceed the remainder. This is 32. Next determine their difference and continue to repeat the process until no further subtractions are possible.

$$\begin{array}{r} 47 \\ -\ 32 \\ \hline 15 \end{array}$$

The highest positional weight less than 15 is 8.

$$\begin{array}{r} 15 \\ -\ 8 \\ \hline 7 \end{array}$$

The highest positional weight less than 7 is 4.

$$\begin{array}{r} 7 \\ -\ 4 \\ \hline 3 \end{array}$$

The highest positional weight less than 3 is 2.

$$\begin{array}{r} 3 \\ -\ 2 \\ \hline 1 \end{array}$$

And finally, the highest positional weight less than or equal to 1 of course is 1.

Now using this information you construct the equivalent binary number. You write a binary 1 for the weight positions you subtracted from the original number and the remainders. In this exmple, these were 128, 32, 8, 4, 2 and 1. Note that you did not use the 64 and 16 weights, so these positions will be binary 0. The number then is 10101111 = 175. You can check it by converting the binary version back into decimal form using the procedure discussed earlier.

Another method for converting decimal numbers into binary is to repeatedly divide the number by 2 and note the remainder. When dividing by 2, the remainder will always be either 1 or 0. The remainder forms the equivalent binary number.

As an example, convert the number 175 into its binary equivalent.

	REMAINDER
175 ÷ 2 = 87	1 ← LSB
87 ÷ 2 = 43	1
43 ÷ 2 = 21	1
21 ÷ 2 = 10	1
10 ÷ 2 = 5	0
5 ÷ 2 = 2	1
2 ÷ 2 = 1	0
1 ÷ 2 = 0	1 ← MSB

Binary Number Sizes

Binary numbers are also referred to as binary words. An 8 bit binary number is also an 8 bit word. You will also see the term byte used to refer to binary words. Most digital circuits and equipment use a fixed word size. The size of this word determines the maximum magnitude and resolution with which numbers can be represented. The number of bits in a word determine the number of discrete states that can exist and the maximum decimal number value that can be represented.

The formula below indicates the number of states that can be represented with a given number of bits.

$N = 2^n$ N = total number of states.
n = number of bits in the word.

For example, with a 4-bit word, we can represent a maximum of

$$N = 2^n = 2^4 = 2 \times 2 \times 2 \times 2 = 16$$

This means that by using 4-bit positions, we can create a total of 16 different binary bit patterns or number combinations. These are shown in Table I along with their decimal equivalents.

TABLE I

DECIMAL	BINARY
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
10	1010
11	1011
12	1100
13	1101
14	1110
15	1111

Binary and decimal number equivalents for a 4-bit word.

As Table I indicates we represent the numbers 0 through 15 using the binary number weighting system. The maximum decimal number that can be represented is one less than the total number of states. The largest decimal number value (N) that can be represented for a given number of bits (n) is expressed with the formula below.

$$N = 2^n - 1$$

For example, with a 6-bit number we can represent a maximum value of

$$N = 2^6 - 1 = 64 - 1 = 63$$

If you know the maximum decimal quantity (N) that you wish to represent with a binary number, you can determine the required number of bits (B) with the expression given below.

$$B = 3.32 \log_{10} N$$

The common logarithm can be obtained from a set of tables, a slide rule or an electronic calculator with log capability. For example, if the maximum decimal number that you need to represent is 500, the number of bits required is:

$$B = 3.32 \log_{10} 500$$
$$B = 3.32 (2.69897)$$
$$B = 8.96$$

Of course you cannot implement fractional bits so the total number of bits required is the next highest whole number. Therefore, to represent the number 500, you would need a total of nine bits. Using the previously given expression, you can determine that, with a total of nine bits, the maximum number you can represent is

$$N = 2^n - 1 = 2^9 - 1 = 512 - 1 = 511$$

The Appendix at the end of this unit contains a table of numbers that are powers of 2. It will help you to quickly determine the relationship between decimal number size and binary word bit length.

Number Identification

When working with both binary and decimal numbers, it is often necessary to have some way of identifying whether a number is a decimal or a binary number. This is particularly true of numbers involving only ones and zeros. For example, the number 101 could represent a quantity of one hundred and one if it is a decimal number. However, if this number is in binary form it would represent a quantity of five.

To distinguish binary from decimal numbers a small subscript number is generally written after the number. The identifying subscript number is the base or radix of the number system being used. Several examples of this notation are indicated below.

$$101_2 = 5_{10}$$
$$101_{10} = 1100101_2$$

Self Test Review

7. The radix of the binary number system is _____.
8. Binary hardware is preferred over decimal hardware in digital equipment because binary components are
   a. _____
   b. _____
   c. _____
9. Convert the following binary numbers to decimal.
   a. 100101101
   b. 11100.1001
   c. 111111
   d. 100000.0111
10. Convert the following decimal numbers to binary.
    a. 127
    b. 38
    c. 22.5
    d. 764.375
11. What is the largest decimal number that can be represented with 8 bits?
12. How many discrete states can be represented with 6 bits?
13. How many bits does it take to represent the number 3875 in binary?

Answers

7. 2
8. a. faster
   b. simpler
   c. more reliable
9. a. $100101101_2 = 301_{10}$
   b. $11100.1001_2 = 28.5625_{10}$
   c. $111111_2 = 63_{10}$
   d. $100000.0111_2 = 32.4375_{10}$
10. a. $127_{10} = 1111111_2$
    b. $38_{10} = 100110_2$
    c. $22.5_{10} = 10110.1$
    d. $764.375_{10} = 1011111100.011$
11. $M = 2^8 - 1 = 256 - 1 = 255$
12. $N = 2^6 = 64$
13. $B = 3.32 \log_{10} 3875 = 3.32\ (3.58827) = 11.91$ 12 bits

BINARY CODES

The general term given to the process of converting a decimal number into its binary equivalent is coding. We express a decimal number as a binary code or binary number. The binary number system, as discussed, is known as the pure binary code. We give it this name to distinguish it from other types of binary codes. In this section you will see some of the other types of binary codes used in digital systems.

Binary Coded Decimal

Because the decimal number system is so familiar, it is easy to use. The binary number system is less convenient to use because we are not as intimately familiar with it. It is difficult to quickly glance at a binary number and recognize its decimal equivalent. For example, the binary number 1010011 represents the decimal number 83. You certainly cannot tell immediately by looking at the number what its decimal value is. However, you know that within a few minutes, using the procedures described earlier, that you could readily calculate its decimal value. The amount of time that it takes you to convert or recognize a binary number quantity is a distinct disadvantage in working with this code despite the numerous hardware advantages. Digital engineers recognized this problem early and developed a special form of binary code that was more compatable with the decimal system. Because so many digital devices, instruments and equipment use decimal input and output, this special code has become very widely used and accepted. This special compromise code is known as binary coded decimal (BCD). The BCD code combines some of the characteristics of both the binary and decimal number systems.

The BCD code is a system that represents the decimal digits 0 through 9 with a four-bit binary code. This BCD code uses the standard 8421 position weighting system of the pure binary code. The standard 8421 BCD code and the decimal equivalents are shown in Table II. As with the pure binary code, you can convert the BCD numbers into their decimal equivalents by simply adding together the weights of the bit positions whereby the binary 1's occur. Note, however, that there are only ten possible valid four bit code arrangements. The 4-bit binary numbers representing the decimal numbers 10 through 15 are invalid in the BCD system.

TABLE II

8421 BCD CODE

DECIMAL	BCD
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001

To represent a decimal number in BCD notation you simply substitute the appropriate four bit code for each decimal digit. For example, the number 834 in BCD would be 1000 0011 0100. Each decimal digit is represented by its equivalent 8421 four bit code. A space is left between each four bit group in order to avoid confusing the BCD format with the pure binary code

The beauty of the BCD code is that the ten BCD code combinations are very easily remembered. Once you begin to work with binary numbers on a regular basis you will find that the BCD numbers will come to you as quickly and automatically as decimal numbers. For that reason by simply glancing at the BCD representation of a decimal number you can make the conversion almost as quickly as if it were already in decimal form.

While the BCD code does help to simplify the man-machine interface it is less efficient than the pure binary code. It takes more bits to represent a given decimal number in BCD than it does with pure binary notation. For example, the decimal number 83 in pure binary form is 1010011. In BCD code the decimal number 83 is written as 1000 0011. In the pure binary code it takes only a 7 bit word to represent the number 83. In BCD form it takes 8 bits. The inefficiency arises out of the fact that for each bit in a data word there is usually a certain amount of digital circuitry associated with it. The extra circuitry associated with the BCD code costs more, increases equipment complexity, and consumes more power. Arithmetic operations with BCD numbers are also more time consuming and complex than those with pure binary numbers. As you recall, with four bits of binary information we can represent a total of $2^4 = 16$ different states or the decimal number equivalents 0 through 15. In the BCD system we waste six of these states (10-15), thus the inefficiency. When we use the BCD number system we trade off some efficiency for the improved communications between the digital equipment and the human operator.

Special Binary Codes

Besides the standard pure binary coded form, the BCD numbering system is by far the most widely used digital code. You will find one or the other in most of the applications that you encounter. However, there are several other codes that are used for special applications. Let's consider some of these.

Excess 3 Code. The excess 3 code (sometimes abbreviated XS3) is not a weighted code. Here each four bit number is three greater than the standard 8421 code number. To obtain the excess 3 code of a specific decimal number, you simply add 3 to it then use the corresponding 8421 binary code (Table I). For example, the excess 3 code for the number 7 is the binary equivalent of $7 + 3 = 10$. The four bit excess 3 code for the number 7 then is 1010. To convert from XS3 to decimal, you simply write the decimal equivalent of each four bit group then subtract three from each digit. The excess 3 code was developed primarily because of its ability to greatly simplify the arithmetic computations with BCD numbers.

Gray Code. The Gray Code is a widely used non-weighted code system. Also known as the cyclic, unit distance or reflective code, the Gray code can exist in either the pure binary or BCD formats. The Gray code is shown in Table III. As with the pure binary code, the first ten codes are used in BCD operations. Notice that there is a change in only one bit from one code number to the next in sequence. You can get a better idea about the Gray code sequence by comparing it to the standard four bit 8421 pure binary code also shown in Table III. For example, consider the change from 7 (0111) to 8 (1000) in the pure binary code. When this change takes place all bits change. Bits that were 1's are changed to 0's and 0's are changed to 1's. Now, notice the code change from 7 to 8 in the Gray code. Here 7 (0100) changes to 8 (1100). Only the first bit changes.

TABLE III

THE GRAY CODE

DECIMAL	GRAY	PURE BINARY
0	0000	0000
1	0001	0001
2	0011	0010
3	0010	0011
4	0110	0100
5	0111	0101
6	0101	0110
7	0100	0111
8	1100	1000
9	1101	1001
10	1111	1010
11	1110	1011
12	1010	1100
13	1011	1101
14	1001	1110
15	1000	1111

The Gray code is generally known as an error-minimizing code because it greatly reduces the possibility of ambiguity in the electronic circuitry when changing from one state to the next. When binary codes are implemented with electronic circuitry, it takes a finite period of time for bits to change from 0 to 1 or 1 to 0. These state changes can create timing and speed problems. This is particularly true in the standard 8421 codes where many bits change from one combination to the next. When the Gray code is used, however, the timing and speed errors are greatly minimized because only one bit changes at a time. This permits code circuitry to operate at higher speeds with fewer errors.

The biggest disadvantage of the Gray code is that it is difficult to use in arithmetic computations. Where numbers must be added, subtracted or used in other computations, the Gray code is not applicable. In order to perform arithmetic operations the Gray code number must generally be converted into pure binary form.

ASCII Code. The ASCII code is a special form of BCD code that is widely used in digital computers and data communications equipment. This code is known as the American Standard Code for Information Interchange (ASCII). It is a 7 bit binary code that is used in transferring data between computers and their external peripheral devices and in communicating data by radio and telephone lines. With 7 bits we can represent a total of $2^7 = 128$ different states or characters. The ASCII code is used to represent the decimal numbers 0 through 9, the letters of the alphabet (both upper and lower case) plus other special characters used for controlling various computer peripheral devices and communications circuits. The standard ASCII code is shown in Table IV.

TABLE IV
AMERICAN STANDARD CODE FOR INFORMATION INTERCHANGE

ROW	COLUMN → / BITS 4321 ↓ / 765 →	0 000	1 001	2 010	3 011	4 100	5 101	6 110	7 111
0	0000	NUL	DLE	SP	0	@	P	`	p
1	0001	SOH	DC1	!	1	A	Q	a	q
2	0010	STX	DC2	"	2	B	R	b	r
3	0011	ETX	DC3	#	3	C	S	c	s
4	0100	EOT	DC4	$	4	D	T	d	t
5	0101	ENQ	NAK	%	5	E	U	e	u
6	0110	ACK	SYN	&	6	F	V	f	v
7	0111	BEL	ETB	'	7	G	W	g	w
8	1000	BS	CAN	(	8	H	X	h	x
9	1001	HT	EM	)	9	I	Y	i	y
10	1010	LF	SUB	*	:	J	Z	j	z
11	1011	VT	ESC	+	;	K	[	k	{
12	1100	FF	FS	,	<	L	\	l	¦
13	1101	CR	GS	–	=	M	]	m	}
14	1110	SO	RS	.	>	N	^	n	~
15	1111	SI	US	/	?	O	—	o	DEL

Explanation of special control functions in columns 0, 1, 2 and 7.

NUL Null
SOH Start of Heading
STX Start of Text
ETX End of Text
EOT End of Transmission
ENQ Enquiry
ACK Acknowledge
BEL Bell (audible signal)

BS Backspace
HT Horizontal Tabulation (punched card skip)
LF Line Feed
VT Vertical Tabulation
FF Form Feed
CR Carriage Return
SO Shift Out
SI Shift In
SP Space (blank)

DLE Data Link Escape
DCI Device Control 1
DC2 Device Control 2
DC3 Device Control 3
DC4 Device Control 4
NAK Negative Acknowledge
SYN Synchronous Idle
ETB End of Transmission Block
CAN Cancel
EM End of Medium
SUB Substitute
ESC Escape
FS File Separator
GS Group Separator
RS Record Separator
US Unit Separator
DEL Delete

The 7-bit ASCII code for each number, letter or control function is made up of a 4 bit group and a 3 bit group. Figure 1-7 shows the arrangement of these two groups and the numbering sequence. The 4-bit group is on the right and bit 1 is the LSB. Note how these groups are arranged in rows and columns in Table IV.

To determine the ASCII code for a given number letter or control operation, you locate that item in the table. Then you use the three and four bit codes associated with the row and column in which the item is located. For example, the ASCII code for the letter L is 1001100. It is located in column 4, row 12. The most significant 3 bit group is 100 while the least significant four bit group is 1100.

There are both 6 and 8 bit special versions of the ASCII code. In addition, the International Business Machines Corporation (IBM) uses another 8 bit coding system called Extended Binary Coded Decimal Interchange Code (EBCDIC) instead of ASCII, for its peripheral and data communications operations.

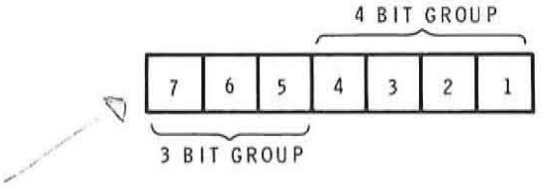


Figure 1-7
ASCII Code Word Format

Self Test Review

14. The BCD code is better than the binary code because
    a. it uses less bits.
    b. it is more compatible with the decimal number system.
    c. it is more adaptable to arithmetic computations.
    d. there are more different coding schemes available.
15. Convert the following decimal numbers to 8421 BCD code.
    a. 1049
    b. 267
    c. 835
16. Convert the following 8421 BCD code number to decimal.
    a. 1001 0110 0010
    b. 0111 0001 0100 0011
    c. 1010 1001 1000
    d. 1000 0000 0101
17. Which code is best for minimum hardware errors?
    a. Excess 3
    b. 8421 BCD
    c. pure binary
    d. Gray
18. Which BCD code is best for arithmetic operations?
    a. Gray
    b. 8421
    c. Excess 3
    d. ASCII
19. Convert the following Excess 3 BCD code to decimal.
    1100 0111 0100 0110
20. The ASCII code is used primarily in _____ and _____.
21. What is the ASCII code for the letter "f"? _____.

Answers

14. b. more compatible with the decimal system.
15. a. 0001 0000 0100 1001
    b. 0010 0110 0111
    c. 1000 0011 0101
16. a. 962
    b. 7143
    c. invalid (1010)
    d. 805
17. d. Gray
18. c. Excess 3
19. 9413_{10}
20. computers, data communications.
21. 1100110

DATA REPRESENTATION

Now that you understand the reason for using the binary number system and are familiar with some of the binary coding schemes used in digital equipment, you are ready to consider the actual hardware means of implementing these binary numbers. By hardware we mean the electronic components and circuits that are used to represent and manipulate the binary numbers used in the digital system. It is relatively easy to represent a binary number with electronic components. The component to represent a specific bit in a binary word must be capable of assuming two distinct states. One of the states will represent a binary 0 and the other a binary 1.

Electromechanical Devices

Switches and relays are ideal for representing binary data. A closed switch or relay contact can represent a binary 1 while the open switch or contact can represent a binary 0. Of course these logic representations can also be reversed. Switches and relays are still widely used to implement digital systems or parts of digital equipment. They are used in places where static binary conditions are required or very low speed operation can be tolerated.

Early digital equipment such as computers and test instruments used relays to represent binary numbers. But the relays were soon replaced by vacuum tubes in many applications. Each bit was represented by a vacuum tube that was either conducting or cut-off. When the tube was conducting it represented one binary state and when it was cut-off it represented the other binary state. Vacuum tubes worked well in digital applications. They achieved operating speeds significantly higher than that of relays. However, because of their large size, high power consumption and speed limitations they have been replaced by solid state devices.

Transistors

Today the most common way of representing binary data in digital equipment is with a transistor. A transistor can readily assume two distinct states, conducting and cut-off. When a transistor is cut-off it is essentially an open circuit. When a transistor is conducting heavily, it acts as a very low resistance and accurately simulates a closed switch. Most digital circuitry in use today uses saturated bipolar switching transistors for data representation. Non-saturated bipolar transistor switches are also used in many applications where high speed operation is desirable. Keep in mind that both discrete component and integrated circuit transistors are used in digital applications.

The enhancement mode MOS field effect transistor (MOS FET) is also widely used as a two state switch to represent binary data. This type of transistor is the key element in MOS and CMOS integrated circuits.

Magnetic Cores

Another common means of representing binary data is by the use of a magnetic core. This is a small donut shaped piece of magnetic material approximately one tenth inch in diameter or smaller. A wire passing through the center of the core carries a current that magnetizes the core in either of two directions depending upon the direction of current flow in the wire. One direction of magnetization represents a binary 0 and the other a binary 1. The permeability of the magnetic material is such that the core retains the magnetization once the current through the wire is removed. This means that the core can store one bit of binary data. It remembers in which direction it was magnetized so that the state of the core can be determined later. Such cores are the primary data storage medium for many digital computers.

Logic Levels

The basic element for representing a single bit of data is a switch: mechanical, electromechanical, electronic or magnetic. The on-off nature of a switch makes it perfect for binary data representation. The exact relationship between the state of the switch and the bit represented by this switch is arbitrary. In actual digital hardware we are not so much concerned with whether the transistor is off or on. Instead the bit assignments are generally represented by voltage levels. The switching element controls these voltage levels. For example, a binary 0 may be represented by 0 volts or ground. A binary 1 may be represented by +5 volts. Depending upon the equipment power supplies available, the exact circuitry used, and the application; almost any voltage level assignments can be used.

Figure 1-4 shows two ways in which a bipolar transistor can be used to produce two distinct voltage levels. In figure 1-4A, the transistor is connected as a shunt switch. This means that the transistor is in parallel with the output. When the transistor is not conducting, the output voltage is +5 volts as seen through collector resistor Rc. When the transistor is conducting it acts as a very low resistance or near short circuit. At this time the output is some low positive voltage level near ground or zero volts. The switching of the transistor of course is controlled by the application of the appropriate base signal. Switching times in the nanosecond (10^{-9} seconds) region are possible with modern transistors.

Positive logic 1 is greater than ∅ ie 1 = 5V, ∅ = 0V
Negative logic 1 is less than ∅ ie 1 = -5V, ∅ = 0V

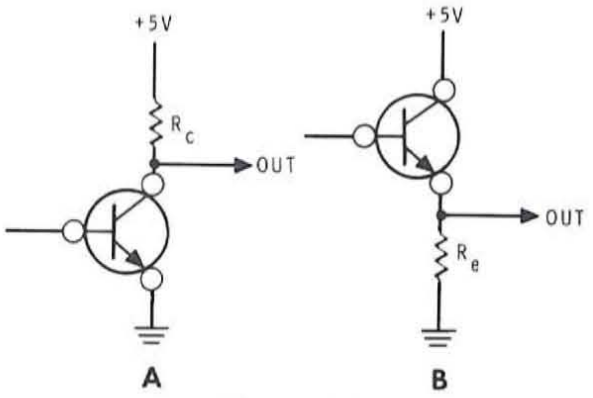


Figure 1-4
Bipolar transistor logic switches, (A) shunt switch (B) series switch.

In Figure 1-4B the transistor is connected as a series switch. When the transistor is cut off the output is zero volts or ground as seen through resistor R_E. When the transistor conducts, it acts as a very low impedance and connects the +5 volts supply line to the output. Again the operation of the transistor is controlled by applying the appropriate signal to the base. You will find both series and shunt transistor switches used in digital circuits.

Positive and Negative Logic

There are two basic types of logic level representation, positive logic and negative logic. When the most positive of two voltage levels is assigned the binary 1 state, we say that positive logic is being used. When the negative or least positive of two voltage levels is assigned to the binary 1 state, we say that negative logic is being used. Indicated below are several examples of both positive and negative logic level assignments. Keep in mind that the assignments are strictly arbitrary and are selected by the designer when the circuit or equipment is designed.

Positive Logic	Negative Logic
binary 0 = +.2V. binary 1 = +3.4V.	binary 0 = +3.4V. binary 1 = +.2V.
binary 0 = −6V. binary 1 = 0V.	binary 0 = 0 V. binary 1 = −6V.
binary 0 = +1V. binary 1 = +15V.	binary 0 = +15V. binary 1 = +1V.

Parallel vs. Serial Data Representation

There are two basic ways in which digital numbers are transmitted, processed or otherwise manipulated. These methods are designated as serial and parallel. In the serial methods of data handling, each bit of binary word or number is processed serially one at a time. In a parallel system all bits of a word or a number are processed simultaneously.

Serial Data. Figure 1-5 shows a binary number represented in a serial data format. The binary number exists as a series of voltage levels representing the binary 1s and 0s. These voltage level changes occur at a single point in a circuit or on a single line. Each bit of the word exists for a specific interval of time. The time interval allotted to each bit is in this example, one millisecond. The most significant bit (MSB) is the one at the far left. It occurs first since time is considered to be increasing from left to right. Because this is an 8 bit binary word, it takes 8 milliseconds for the entire word to occur or be transmitted. Positive logic level assignments are used. By observing the voltage levels at the specific point or on the transmission line, the number can be determined. The number is 10110010. This is the binary equivalent of the decimal number 178.

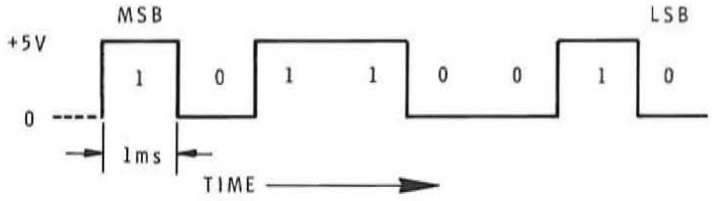


Figure 1-5
The serial binary word 10110010

The primary advantage of the serial binary data representation is that it requires only a single line or channel for transmitting it from one place to another. In addition, since each bit on the single line occurs separately from the others then only one set of digital circuitry is generally needed to process this data. For these reasons, serial data representation is the simplest and most economical of the two types. Its primary disadvantage is that the transmission and processing time required for a serial word is significant since the bits occur one after the other. Despite this time penalty, serial data representation is widely used because of its economy and simplicity.

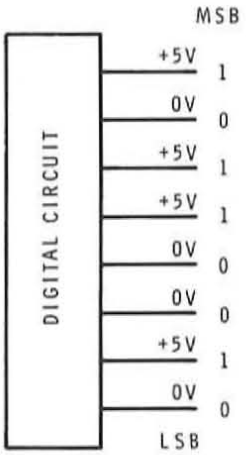


Figure 1-6
The parallel binary word 10110010

Parallel Data. The other method of representing, transmitting and processing binary data is designated as parallel. The reason for this is that all bits of a binary word or number are transmitted or processed simultaneously. For this reason a separate line or channel is required for each bit of the word in transmitting that word from one point to another. Refer to Figure 1-6. Here the 8-bit digital word 10110010 is available as voltage levels on eight separate output lines. Since all of the bits of the word are available at the same time, digital circuitry must be provided to process or otherwise manipulate each of the bits in the word simultaneously. The transmission and processing of parallel data, therefore, is more complex and expensive than that required for serial data. However, the clear advantage of parallel data transmission is its speed. All bits are processed at the same time and, therefore, the time required for handling of the data is very short. For high speed applications requiring rapid processing, parallel digital techniques are preferred.

Logic Circuits

The transistor is by far the most common way of representing binary data in modern digital equipment. These transistors are combined with other electronic components to form digital circuits. Digital, or logic, circuits are used to process or manipulate the binary information in some way. The primary emphasis in this program is on digital logic circuits and how they are designed and used.

There are two basic types of logic circuits, decision-making and memory. Our ability to think logically requires both a capability for making decisions based on given information and the ability to remember facts. This holds true for digital circuits and equipment as well. Logic circuits accept input binary data and based upon that information generate output binary signals that represent the results of a built in decision making capability or they store the input data for later use.

Decision making logic circuits are called gates. Such circuits have two or more inputs and a single output. Both the inputs and outputs are binary signals. These gates are combined in a variety of ways to form combinational logic circuits that can perform a wide range of sophisticated decision making functions.

The memory circuits store binary data. Commonly called flip flops, these circuits remember a single bit of data. Flip flops are combined to form a class of logic circuits called sequential circuits. Such circuits store, count, and shift binary data and otherwise manipulate it.

All digital equipment is made up of both gates and flip flops that form functional combinational and sequential circuits. Such functional circuits perform the specific operations called for by the application. The remaining lessons in this program are concerned with the detailed design and application of such circuits.

The key components used in digital circuits are semiconductors such as diodes and transistors. These are combined with resistors, capacitors and other electronic components to form the circuits that produce the various logic functions. Early digital circuits were made up of discrete components, individual components interconnected to form the circuit. Today, most digital logic is in integrated circuit form. These are microminiature semiconductor devices that are complete logic circuits constructed in a single package.

Since semiconductors are the basis for all modern digital circuits, you will find a knowledge of their operation helpful in designing, using or troubleshooting digital equipment. The next Unit in this program covers this important subject.

Self Test Review

22. The basic component used to represent a binary digit is a _____.
23. The two types of transistors used to implement digital circuits are _____ and _____.
24. Designate the following logic level assignments as being either positive or negative.
    a. binary 0 = +3
       binary 1 = −3
    b. binary 0 = +0.8
       binary 1 = +1.8
25. Serial data transmission is faster than parallel data transfers.
    a. True
    b. False
26. The following voltage levels appear on six parallel data lines designated A through F.
    A = +5 V, B = +5 V, C = 0 V, D = +5 V, E = 0 V, F = +5 V
    Using positive logic and assuming bit A is the LSB, what is the decimal number equivalent?
27. Gates and flip-flops are combined to form _____ and _____ logic circuits.

Answers

22. switch (mechanical, electro-mechanical or electronic)
23. bipolar, MOS FET
24. a. negative
    b. positive
25. b. False
26. A = +5 V = 1 (LSB), B = +5 V = 1, C = 0 V = 0, D = +5 V = 1, E = 0 V = 0, F = _ 5 V = 1 (MSB)
    Number = FEDCBA = 101011_2
    Decimal equivalent = 43_{10}
27. combinational, sequential

UNIT SUMMARY

1. The two basic types of electronic circuits and signals are analog and digital.

2. Analog signals are either ac or dc and vary smoothly or continuously.

3. Analog signals are processed by analog or linear circuits.

4. Digital signals are voltages or currents that vary in discrete steps or increments.

5. Most digital signals are binary in nature, that is having two states, steps or levels.

6. Digital signals are processed by digital logic circuits.

7. Digital techniques are used in virtually all areas of electronics.

8. The impetus for the increased use of digital circuits has been the recognition of their advantages and the development and availability of low cost digital integrated circuits.

9. Digital techniques were perfected by the computer industry.

10. Digital techniques offer several advantages over analog methods including greater accuracy, greater dynamic range, greater stability, convenience, automation and for many applications lower cost and less power consumption.

11. The decimal number system has a base or radix of ten because it uses the ten digits 0 through 9 to represent quantities.

12. The binary number system has a base of 2 since it uses only two bits, 0 and 1, to represent quantities.

13. The decimal and binary number systems are weighted positional systems in that the position of a digit in a number indicates the weight it has in determining the value of that number.

14. Binary numbers have a 1, 2, 4, 8, 16, 32, 64, etc. weighting system.

15. To determine the decimal value of a binary number you add together the weights of the positions containing a binary 1.

16. The number of bits (n) in a binary number or word determines the maximum quantity (N) that can be represented. $N = 2^n - 1$

17. The number of bits (B) needed to represent a quantity (N) is determined with the expression $B = 3.32 \log_{10} N$.

18. The binary number system is a system for coding quantities or other information.

19. The binary coded decimal (BCD) system of quantity representation is a compromise system that enhances the flexibility of communication between man and machine. It is based on both the binary and decimal systems.

20. With BCD coding each decimal digit is represented by a four bit binary code.

21. A variety of BCD codes are used, each having a specific advantage or function. These included the weighted 8421 code and the unweighted excess 3 code.

22. The Gray code is used where minimum error is required. Only one bit changes from one code group to the next in sequence.

23. The ASCII code is a special 7-bit BCD code used in data communications and computer peripherals. It is used to represent quantities as well as letters and special functions.

24. The transistor is the most common way of representing binary data. Both bipolar and MOS FET types are used.

25. Any switch, electronic, electromechanical or mechanical can be used to represent binary numbers.

26. Binary numbers appear as voltage levels in digital equipment. One voltage level is assigned to represent a binary 1 and another level is assigned to represent a binary 0.

27. Positive logic level assignment is where the binary 1 is the most positive of the two levels. Negative logic is where the most negative of the two levels is designated as a binary 1.

28. Serial data transmission requires only a single line and circuitry to handle one bit of data at a time. Each bit in a word is transmitted sequentially. Serial processing is the simplest, least expensive, and least complex of methods but is slow because of its sequential nature.

29. In parallel transmission or processing all bits of a word are handled at once. This makes for very high speed operation, but circuitry is required for each bit. This increases cost and complexity.

30. The two basic types of logic circuits are gates and flip flops which are used for decision making and memory functions respectively. These basic elements are combined to form combinational and sequential circuits that are the functional parts of any digital equipment.

EXAMINATION

UNIT 1

INTRODUCTION TO DIGITAL TECHNIQUES

This exam will test your knowledge of the important facts in this unit. It will tell you what you have learned and what you need to review. Answer all questions first then check your work against the correct answers given later.

1. A constant dc voltage is
   A. an analog signal
   B. a digital signal
   C. either a. or b. depending upon how it is defined.
2. The waveform in Figure 1-8 is
   A. analog
   B. digital

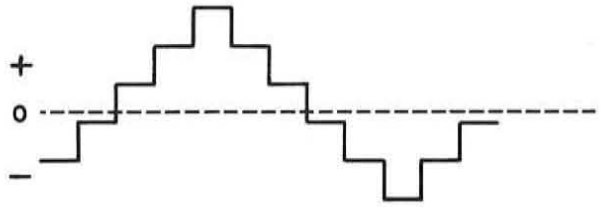


Figure 1-8
Waveform for Exam Question 2

3. For each item below designate whether it is analog or digital.
   A. auto headlights _____
   B. bathroom scale _____
   C. weather vane _____
   D. gasoline gauge _____
   E. camera shutter _____
4. What factor has influenced the growth and increased use of digital techniques more than any other?
   A. The need for greater accuracy.
   B. Computers
   C. Recognition of the benefits of digital methods.
   D. Availability and perfection of integrated circuits.

5. Which of the following is **not** an advantage of digital over analog techniques?
   A. greater accuracy
   B. simplicity
   C. greater dynamic range
   D. better stability
6. Convert the following binary numbers to decimal.
   A. 1001011
   B. 1110110010 . 0101
7. Convert the following decimal numbers to binary.
   A. 1000
   B. 95
8. Convert the following 8421 BCD numbers into their decimal equivalents.
   A. 1000 0110 0010 0101
   B. 0001 1001 0111 0100
9. Convert the following decimal numbers to 8421 BCD.
   A. 30.97
   B. 2486
10. A. The highest number you can represent with ten bits is _____.
    B. It takes _____ bits to represent the number 121.
11. Select the unweighted codes.
    A. Gray
    B. 8421
    C. ASCII
    D. Excess 3
12. The ASCII code is used primarily in
    A. digital test instruments
    B. computer arithmetic
    C. data communications
    D. electronic calculators
13. Digital signal levels of binary 0 = −.7 and binary 1 = −1.7 represent which type of logic?
    A. positive
    B. negative
14. Five wires A through E carry the voltage levels representing a binary number. These levels are A = 0V, B = 0V, C = +5V, D = 0V, E = +5V. Assuming E is the MSB and the use of positive logic, what decimal number is represented?

15. The primary advantage of serial data transmission is
    A. highest speed method for digital processing
    B. minimum hardware and complexity
    C. convenience
    D. ease of code recognition
16. Name six electronic devices that use digital techniques.
    A. _____
    B. _____
    C. _____
    D. _____
    E. _____
    F. _____
17. The most common way of electronically representing binary data is with a
    A. transformer
    B. magnetic core
    C. transistor
    D. toggle switch
18. The two basic types of logic circuits are _____ and _____.
19. Using only your knowledge of binary codes, identify the Gray code and the excess 3 code.

Decimal	a	b	c	d
0	0000	0000	0000	0011
1	0001	0001	0001	0100
2	0011	0010	0010	0101
3	0010	0011	0011	0110
4	0110	0100	0100	0111
5	0111	0101	1011	1000
6	0101	0110	1100	1001
7	0100	0111	1101	1010
8	1100	1000	1110	1011
9	1101	1001	1111	1100

20. Sketch the binary waveform of a serial data word for the number 18 where the LSB is transmitted first. Assume negative logic assignments of the binary levels 0V and +10V.

ANSWERS

UNIT 1 EXAMINATION

INTRODUCTION TO DIGITAL TECHNIQUES

1. C — A constant dc voltage could be an analog signal or one of two levels in a binary digital system depending upon the circuits and techniques used or the definitions given.
2. B — Since the waveform varies in discrete steps it is considered to be digital. However, since most digital signals are binary in nature the waveform in Figure 1-8 is not typical. We could call this signal a digital approximation to a varying analog signal.
3. A — auto headlights — digital
   B — bathroom scale — analog
   C — weather vane — analog
   D — gasoline gauge — analog
   E — camera shutter — digital
4. D — The availability of versatile, low cost integrated circuits has been the most significant factor in the increased use of digital techniques.
5. B — Simplicity. Digital techniques have many advantages (i.e. greater accuracy, etc.) but simplicity is not necessarily one of them. In fact, it is often necessary to increase the complexity of a device in order to gain the advantage of digital methods.
6. A — $1001011_2 = 75_{10}$
   B — $1110110010.0101_2 = 946.3125_{10}$
7. A— $1000_{10} = 1111101000_2$
   B — $95_{10} = 1011111_2$
8. A — 8625
   B — 1974
9. A — 0011 0000 . 1001 0111
   B — 0010 0100 1000 0110
10. A — $M = 2^n - 1 = 2^{10} - 1 = 1024 - 1 = 1023$
    B — $B = 3.32 \log_{10} 121 = 3.32\ (2.08279) = 6.915\ 7$ bits.
11. A,C,D— The Gray,ASCII and excess 3 codes are unweighted.
12. C — Data Communications and computer peripherals are the primary applications of the ASCII code.
13. B — Negative logic is where the most negative (least positive) of two levels is designated a binary 1.

14. The binary word is EDCBA = 10100_2 or 20_{10}.
15. B — The primary advantage of serial data transmission is minimum hardware and complexity, hence lowest cost. The sacrifice is lower data transmission rates. However, parallel transmission is faster at the expense of more hardware and complexity.
16. A — electronic calculators
    B — computers
    C — TV sets
    D — hi fi stereo receivers
    E — industrial controls
    F — data communication equipment
17. C — A transistor switch, bipolar or MOS FET, is the most common means of implementing binary data.
18. Gates and flip flops or decision-making and memory.
19. (a) Gray code, (d) excess 3.
20. See Figure 1-9.

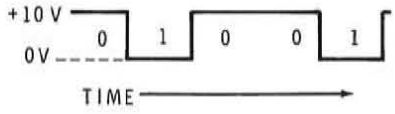


Figure 1-9
Solution to Exam Question 20.
Serial representation of
the number 18 using negative logic.

APPENDIX

TABLE OF POWERS OF 2

2^n	n	2^{-n}
1	0	1.0
2	1	0.5
4	2	0.25
8	3	0.125
16	4	0.062 5
32	5	0.031 25
64	6	0.015 625
128	7	0.007 812 5
256	8	0.003 906 25
512	9	0.001 953 125
1 024	10	0.000 976 562 5
2 048	11	0.000 488 281 25
4 096	12	0.000 244 140 625
8 192	13	0.000 122 070 312 5
16 384	14	0.000 061 035 156 25
32 768	15	0.000 030 517578 125
65 536	16	0.000 015 258 789 062 5

n = number of bits

2.5 HEXADECIMAL NUMBER SYSTEM

The hexadecimal number system has a base of 16. Sixteen different symbols are used to represent numbers which are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, and F. Table 2-4 shows the first few hexadecimal numbers and their decimal equivalents.

Table 2-4. Hexadecimal Counting

Hexadecimal	Decimal	Hexadecimal	Decimal
0	0	A	10
1	1	B	11
2	2	C	12
3	3	D	13
4	4	E	14
5	5	F	15
6	6	10	16
7	7	11	17
8	8	12	18
9	9	13	19

The use of the hexadecimal number system as another binary shorthand, became of use as digital computers began to use 8 binary bits to represent units of information.

2.5.1 Hexadecimal to Decimal Conversion

From Table 2-4 we see that hexadecimal 11 equals a decimal 17. The numbering system formula proves this is true:

$$N = a_2 r^1 + a_1 r^0$$

$$= 1 \times 16^1 + 1 \times 16^0$$

$$= 16 + 1$$

$$= 17$$

The powers of sixteen are shown in the following table.

etc	16^4	16^3	16^2	16^1	16^0	Powers of sixteen
etc	65536	4096	256	16	1	Decimal value

2.5.2 Decimal to Hexadecimal Conversion

The conversion from decimal to hexadecimal follows the same procedure as decimal to binary and decimal to octal except the base is now 16 instead of 2 or 8.

Example:

$27890_{10} = N_{16}$

Quotient	Remainder		Hexadecimal Remainder	
6	6	=	6	MSD
$16\overline{)108}$	12	=	C	↑
$16\overline{)1743}$	15	=	F	↑
$16\overline{)27890}$	2	=	2	LSD

Therefore; $27890_{10} = 6CF2_{16}$

2.5.3 Binary to Hexadecimal Conversion

The simplest way to convert a binary number to a hexadecimal number is to group the binary digits in groups of fours beginning at the radix point and read each set of four binary digits according to Table 2-5.

Table 2-5. Binary to Hexadecimal Equivalent

Four Binary Digits	Hexadecimal Digit	Four Binary Digits	Hexadecimal Digit
0000	0	1000	8
0001	1	1001	9
0010	2	1010	A
0011	3	1011	B
0100	4	1100	C
0101	5	1101	D
0110	6	1110	E
0111	7	1111	F

Example:

$1101011111101101_2 = N_{16}$

0110 1011 1110 1101

6 B E D

Therefore; $1101011111101101_2 = 6BED_{16}$

2.5.4 Hexadecimal to Binary Conversion

Hexadecimal numbers are converted to binary merely by taking the hexadecimal digit and representing it by its four binary equivalent digits shown in Table 2-5.

Example:

$6BED_{16} = N_2$

6 B E D

0110 1011 1110 1101

Therefore; $6BED_{16} = 1101011111101101_2$

2.5.5 Octal to Hexadecimal and Hexadecimal to Octal Conversion

Although it is possible to convert octal to hexadecimal and vice-versa by dividing one by the base of the other, as explained in the preceding number system conversions, it is much easier to convert the number to binary, then regroup the binary digits and convert to the system desired.

Examples:

4 digits each group

				$725_8 = N_{16}$
Converted to binary	111	010	101	$= N_{16}$
Regrouped	0001	1101	0101	$= N_{16}$
Converted to hexadecimal	1	D	5	$= N_{16}$

Therefore; $725_8 = 1D5_{16}$

3 digits on group

				$3DB_{16}$	$= N_8$
Converted to binary		0011	1101	1011	$= N_8$
Regrouped	001	111	011	011	$= N_8$
Converted to octal	1	7	3	3	$= N_8$

Therefore; $3DB_{16} = 1733_8$

2.4 OCTAL NUMBER SYSTEM

The octal number system has a base of 8. Eight different symbols are used to represent numbers. These are 0, 1, 2, 3, 4, 5, 6 and 7. Table 2-2, using positional rotation, shown the first few octal numbers and their decimal equivalents.

Table 2-2. Octal Counting

Octal	Decimal	Octal	Decimal
0	0	11	9
1	1	12	10
2	2	13	11
3	3	14	12
4	4	15	13
5	5	16	14
6	6	17	15
7	7	20	16
10	8	21	17

2.4.1 Octal to Decimal Conversion

From Table 2-2 we see that octal 21 equals a decimal 17. The numbering system formula proves this is true:

$$N = a_2r^1 + a_1r^0$$

$$N = 2x8^1 + 1x8^0$$

$$N = 2x8 + 1x1$$

$$N = 16 + 1$$

$$N = 17$$

The following power table lists the powers of eight.

etc	8^5	8^4	8^3	8^2	8^1	8^0	Power of eight
etc	32768	4096	512	64	8	1	Decimal Value

Example:

$$2174_8 = (2x512) + (1x64) + (7x8) + (4x1)$$
$$= 1024 + 64 + 56 + 4$$
$$= 1148_{10}$$

To convert an octal fraction to a decimal fraction we once again set up a negative power table for the octal system by dividing 1 by the base 8 some number of times.

Power of eight	2^{-1}	2^{-2}	2^{-3}	etc
Decimal value	.125	.015625	.001953125	etc

Example:

$$0.63_8 = (6x.125) + (3x.015625)$$
$$= .750 + .046875_{10}$$
$$= .796875_{10}$$

2.4.2 Decimal to Octal Conversion

The conversion from decimal to octal follows the same prodedure used in decimal to binary, except the base is now 8 instead of 2. The integer portion and the fractional portion are considered separately.

Examples:

$176_{10} = N_8$

Quotient	Remainder	
$8\overline{)176}$	0	
$8\overline{)22}$	6	
$8\overline{)2}$	2	MSD
0		LSD

Therefore, $176_{10} = 260_8$

$253.15_{10} = N_8$

		.15 x 8 = 1.2	1	MSD	.2
0	3	.2 x 8 = 1.6	1	↑	.6
		.6 x 8 = 4.8	4		.8
8/ 3	7	.8 x 8 = 6.4	6		.4
		.4 x 8 = 3.2	3		.2
8/ 31	5	.2 x 8 = 1.6	1	LSD	.6
8/253					

Therefore; $253.15_{10} = 375.114631_8$

2.4.3 Binary to Octal Conversion

The primary use of the octal number system is in conveniently recording the cumbersome numbers of ONEs and ZEROs in the binary system.

The most simple trick for converting a binary number to an octal number is to simply group the binary digits into groups of threes beginning at the octal point, and read each set of three binary digits according to Table 2-3.

Table 2-3. Binary to Octal Equivalent

Three Binary Digits	Octal Digits
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

Examples:

$1011110101_2 = N_8$

001 011 110 101

1 3 6 5_8

Therefore; $1011110101_2 = 1365_8$

$$101110100.11101_2 = N_8$$

101	110	100	.	111	010
5	6	4	.	7	2_8

Therefore; $101110100.11101_2 = 564.72_8$

2.4.4 Octal to Binary Conversion

As you have seen, binary numbers are directly convertible to octal. Octal numbers are also directly convertible to binary. Merely take each octal digit and represent it by its three binary equivalent digits shown in Table 2-3.

Example:

$$173.406_8 = N_2$$

1	7	3	.	4	0	6
001	111	011	.	100	000	110

Therefore; $173.406_8 = 1111011.10000011_2$

HEATHKIT
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2 SEMICONDUCTOR DEVICES FOR DIGITAL CIRCUITS

Individual Learning Program

In

DIGITAL TECHNIQUES

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UNIT 2

SEMICONDUCTOR DEVICES FOR DIGITAL CIRCUITS

CONTENTS

UNIT 2

SEMICONDUCTOR DEVICES AND CIRCUITS FOR DIGITAL TECHNIQUES

INTRODUCTION

At the heart of all modern digital circuits are semiconductor devices like diodes and transistors. Your ability to understand digital circuits and apply them to practical situations depends directly on a knowledge of semiconductors. The purpose of this Unit is to provide you with a solid background in semiconductor fundamentals as they apply to digital circuits, both discrete components as well as integrated circuits. For many of you, this Unit will be primarily a review. It will help you to remember the key points about semiconductor devices. For some of you the information may be mostly new. We have developed it to give you exactly what you need to understand digital circuits.

Since most engineers, technicians, and experimenters are users of semiconductor devices rather than designers, our discussion here will focus on practical operation and application rather than detailed coverage of internal device physics.

The Unit Objectives below will tell you exactly what you will learn in this Unit. Follow the Unit Activity Guide checking off each learning activity as you complete it. Keep track of your time and progress in the spaces provided.

UNIT OBJECTIVES

When you complete Unit 2 on semiconductor devices you will have the knowledge and skills indicated below. You will be able to:

1. Name the two types of semiconductor elements used in digital circuits and list two advantages and disadvantages of each.
2. Identify from a list of symbols used to represent PNP and NPN bipolar transistors and P- and N-channel enhancement mode MOSFETs.
3. Explain the operation of both bipolar transistors and MOSFETs.

4. Draw a diagram indicating the proper bias on a bipolar transistor for linear and saturated operations.
5. Name and explain the three operating modes of a bipolar transistor.
6. Explain the operation of a logic inverter circuit.
7. Design a saturated bipolar transistor switching circuit.

UNIT ACTIVITY GUIDE

	Completion Time
☐ Play Audio Record 3, Side 2 "Semiconductor Devices for Digital Circuits."	_____
☐ Read Section Programmed Review of Transistor Operation Pages 2-5 to 2-17.	_____
☐ Answer Self Test Review Questions 1-10.	_____
☐ Read section "The Bipolar Transistor Switch:" Pages 2-20 to 2-28.	_____
☐ Answer Self Test Review Questions 11-20.	_____
☐ Read Section "Designing a Saturated Switch Logic Inverter." Pages 2-29 to 2-35.	_____
☐ Work Self Test Review problem 21.	_____
☐ Perform Experiment 1.	_____
☐ Read Section "MOS Field Effect Transistors:" Pages 2-41 to 2-44.	_____
☐ Answer Self Test Review Questions 22-26.	_____
☐ Read the Unit Summary.	_____
☐ Complete the Unit Examination.	_____
☐ Review Examination Answers.	_____

A PROGRAMMED REVIEW OF TRANSISTOR OPERATION

Your understanding of logic circuits is dependent upon a knowledge of bipolar transistor operation. A knowledge of transistor action is a prerequisite to this program, but the following review is included to refresh your understanding of this important subject.

To use this program simply read the information in each numbered frame and answer the accompanying question by filling in the blank(s) or choosing the correct answer. Cover the frames below the one you are reading with a piece of paper so that you will not be tempted to look at the answers. As you complete each frame, slide the paper down to reveal the next frame in sequence. The correct answer to the question in the previous frame appears in parenthesis at the beginning. The lesson material then continues. For best results complete this entire section at one time rather than breaking it into several study periods.

1. A transistor is a three element semiconductor device used in electronic equipment for controlling a large current with a smaller current. Transistors are used primarily as amplifiers with gain but are also used as switches in digital logic circuits.

   Transistors are made of semiconductor materials such as silicon and germanium. These are materials whose resistance is somewhere between that of conductors and insulators.

   The resistance of silicon is
   a. greater than
   b. less than
   c. the same as

   the resistance of a good conductor such as copper.

2. (a. greater than) Since the conductivity is between that of good conductors and insulators, the resistance of a semiconductor like silicon is greater than that of copper but considerably less than the resistance of an insulator such as glass or ceramic.

There are two types of semiconductor material, P-type and N-type. A semiconductor such as silicon is combined with other materials to form these two different types. For example, certain impurities are added to pure silicon to form P-type and other impurities are added to form the N-type. The resulting N-type material is one which has an excess of free electrons. In other words, the majority current carriers are electrons. In P-type material, the majority current carriers are holes. A hole is the absence of an electron in the atomic structure of P-type silicon material, and it acts like a positive charge. P-type semiconductor material has an excess of holes to support current flow.

Current flow is by _____ in N-type material and by _____ in P-type material.

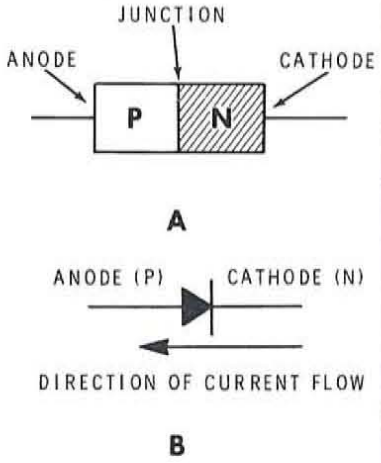


Figure 2-1
A PN junction diode
(A) and its schematic symbol (B)

3. (electrons, holes) Transistors and other semiconductor devices such as diodes and integrated circuits are made by combining P-type and N-type materials. For example, a diode is formed by joining P-type and N-type sections as shown in Figure 2-1A. The P-type section is designated as the anode, and the N-type section is designated as the cathode.

The PN junction thus formed has unilateral characteristics. That is, current will flow through it in only one direction. It blocks current (electron) flow in the opposite direction. Figure 2-1B shows the symbol used to represent a PN junction diode in schematic diagrams.

A junction diode is sensitive to the _____ of current flow.

4. (direction) If we apply a dc voltage to the junction diode, current may or may not flow through it depending upon the polarity of the voltage. This applied voltage is called bias. Figure 2-2 illustrates one way in which a junction diode can be biased. The series resistor R limits the current to a safe level.

In Figure 2-2, electrons flow out of the negative terminal of the battery into the N-type material. If the battery voltage is high enough to overcome an inherent potential barrier associated with the junction, the electrons will cross the junction and fill the holes. As the holes in the P-type material are filled, new holes are formed as electrons are pulled from the P-type material by the positive terminal of the battery. The result is a continuous current flow through the device. This arrangement is known as forward bias.

To bias a junction diode into conduction, the P-type element is connected to the _____ terminal of the battery and the N-type element is connected to the _____ terminal of the battery.

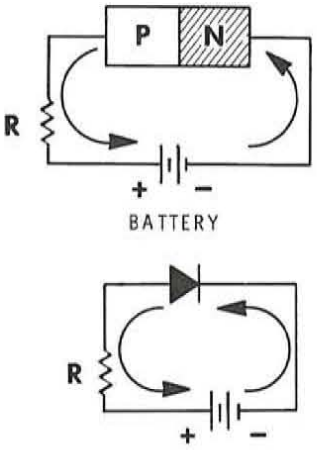


Figure 2-2
Forward biasing a PN junction diode so that it conducts

5. (positive, negative) To forward bias a PN junction diode, the positive (P) battery terminal is connected to the P-type element and the negative (N) terminal of the battery is attached to the N-type element. The result is a continuous flow of current through the device that is effectively limited by the external circuit resistance. A voltage drop of approximately .7 volts occurs across a silicon diode. This drop is essentially constant regardless of the current value. The drop across a conducting germanium diode is about .3 volt.

How much current flows in the circuit of Figure 2-3?

I= _____ ma

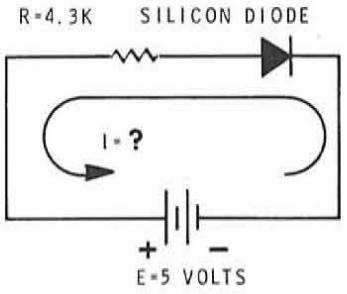


Figure 2-3
A forward biased diode.

6. (1 milliampere) In this circuit the diode is forward biased because the polarity of the applied voltage is correct. Therefore, current does flow. This current is limited by the resistance, but of course, is also a function of the battery voltage and the diode voltage drop. In this circuit, the diode drop is about .7 volts because the device is silicon. This means that the voltage drop across the resistor is (5 − .7) = 4.3 volts. The current (I) is then found by Ohm's law.

$$I = \frac{E}{R} = \frac{4.3}{4.3K} = \frac{4.3}{4300} = .001 \text{ amp} = 1 \text{ ma}$$

Current flows in a PN junction diode when it is _____ _____.

7. (forward biased) A forward biased diode conducts and acts as a very low resistance, permitting current to flow through it freely. If the polarity of the applied voltage is reversed as shown in Figure 2-4, the diode is said to be reverse biased.

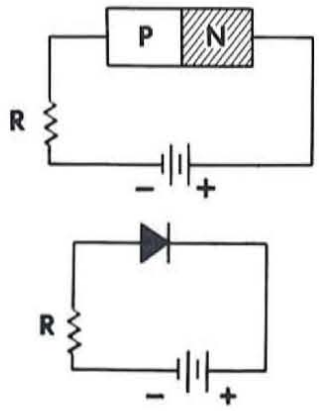


Figure 2-4 A reversed biased PN junction diode

With this arrangement, the electrons from the negative terminal of the battery fill the holes in the P-type material. The excess electrons in the N-type material are drawn away by the positive terminal of the battery. The effect is to draw the current carriers away from the junction so that no current flows. The diode acts as an effective open circuit. In a practical diode some leakage current does flow across the junction. But in a good silicon device this current is very low, in the microampere or nanoampere range, and for most applications can be considered to be negligible or zero.

To reverse bias a diode so that no current flows through it, the cathode (N) must be _____ with respect to the anode (P).

8. (positive) If the cathode is positive with respect to the anode, the diode is reverse biased and no current flows. To achieve this, the positive terminal of the battery is connected to the N-type cathode, and the negative terminal is connected to the P-type anode.

If the anode is made positive with respect to the cathode then current will flow. True or False? _____

9. (True) With the anode (P) positive with respect to the cathode (N), the diode is forward biased so current does flow. As you can see, the diode is polarity sensitive and that current does indeed flow through the device in only one direction, from cathode to anode.

Transistors are simply an extension of the junction diode concept. Transistors are formed by combining the P- and N-type material to form two junctions. This is done with three semiconductor elements. Figure 2-5 shows the two types of transistors.

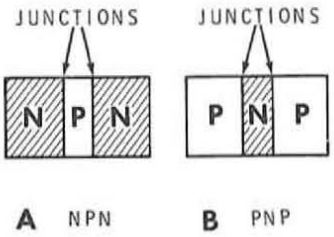


Figure 2-5
Types of junction transistors

The device in Figure 2-5A is an NPN transistor and the device in Figure 2-5B is a PNP transistor. Note the two arrangements of alternate P and N type materials.

The symbols used to represent these two types of transistors are shown in Figure 2-6 below.

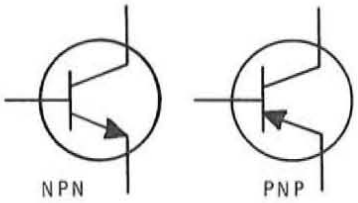


Figure 2-6
Transistor Symbols

The direction of the arrow is the distinguishing feature.

A transistor has (how many?) _____ PN junctions.

10. (two) Both types of transistors have two PN junctions. Each junction behaves exactly like the PN junction diode discussed earlier.

The three elements of each transistor are given specific names as indicated in Figure 2-7.

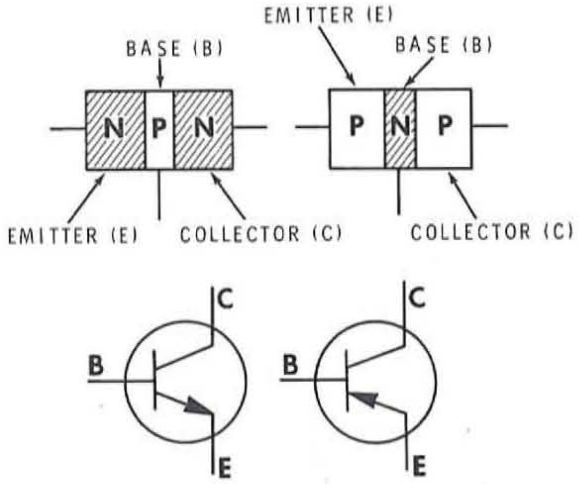
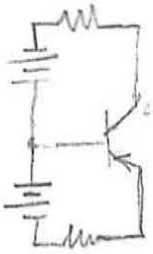


Figure 2-7
Identifying the three elements of a transistor

In a transistor, current flows through the device from the emitter through the base to the collector (holes in a PNP transistor and electrons in an NPN transistor). The presence or magnitude of this emitter-collector current is dependent upon the existence or magnitude of the base current.

The control element in a transistor is the _____.



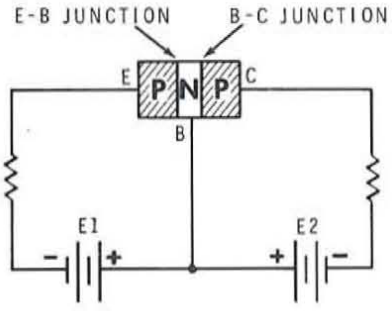


Figure 2-8

11. (base) Yes, the base is the control element. It effectively determines the magnitude (or presence) of any emitter-collector current.

In order for a transistor to function properly, the emitter-base (E-B) and base-collector (B-C) junctions must be properly biased. Proper bias to cause a transistor to conduct occurs when the E-B junction is forward biased and the B-C junction is reverse biased.

Is the PNP transistor shown in Figure 2-8 properly biased for conduction? Yes or No? ____

12. (No) The B-C junction is OK since it is reverse biased (+ to N and − to P), but the E-B junction is reverse, not forward, biased. The polarity of battery E_1 must be reversed.

Using the circuit configuration shown in the previous frame, draw the proper biasing for an NPN transistor.

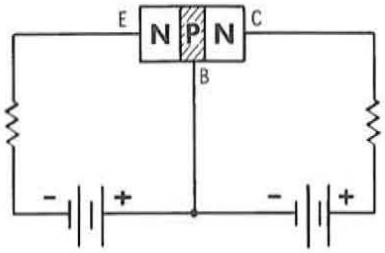


Figure 2-9
A properly biased NPN transistor

13. (Refer to Figure 2-9). The E-B junction is forward biased (+ to P and − to N) and the B-C junction is reverse biased (+ to N and − to P).

In a practical transistor circuit you can measure the voltages at each transistor element and noting the magnitudes and polarities, you can determine if the transistor is conducting or cut off.

Using the knowledge you've obtained to this point, determine the condition of the transistor in Figure 2-10.

This
a. PNP transistor
b. NPN
c. is conducting.
d. is not conducting.

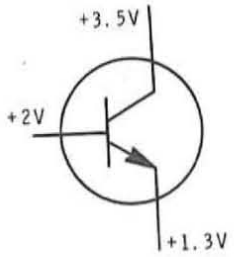


Figure 2-10

14. (b. NPN, c. is) The transistor is conducting. The base is more positive than the emitter so the E-B junction is forward biased. Note the difference of potential across the conducting E-B junction is .7 volts, the forward voltage drop of a silicon diode. Most modern transistors (diodes and integrated circuits) are silicon devices.

The base is less positive or more negative than the collector by (3.5 −2) = 1.5 volts so this junction is reverse biased. Therefore the transistor is conducting.

Is the PNP transistor in Figure 2-11 conducting or non-conducting? _____.

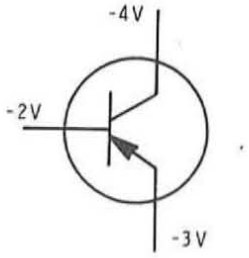


Figure 2-11

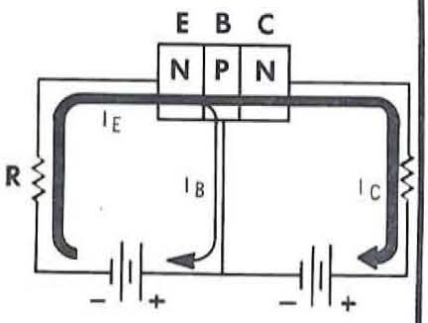
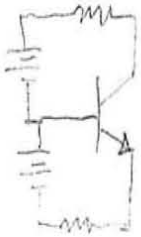


Figure 2-12 Current flow in a properly biased NPN transistor



15. (non-conducting) Both the E-B and B-C junctions are reverse biased so current does not flow from emitter to collector.

The actual path for current (electron) flow in a properly biased NPN transistor is shown in Figure 2-12.

A large current (I_E) flows into and through the emitter, through the base to the collector. Note that a small amount of emitter current divides off and flows out of the base. This is the E-B junction forward bias current or the base current I_B. Its magnitude is usually considerably less than that of the emitter current. The remaining current (I_C) flows out of the collector.

Considering the current relationship in Figure 2-12, how do you think the current flowing out of the collector compares to the current entering the emitter? The collector current is

a. equal to
b. less than
c. greater than

the emitter current.

16. (b. less than) The collector current (I_C) in reality is very nearly equal to the emitter current (I_E) but is less than the emitter current by an amount equal to the base current (I_B). The exact relationship is as expressed below.

$$I_C = I_E - I_B$$

You would expect current to flow in the E-B circuit because this junction is forward biased. But you would not normally expect current to flow in the collector because the B-C junction is reverse biased. The electrons flowing in the emitter enter the base. Here some of the electrons combine with holes in the P-type base and create the current flow out of the base. However, most of the electrons pass on through the base and into the collector. The reason for this is that the base is extremely thin and has only a minimum of available carriers to support current flow. The electrons passing through the base are then attracted by the positive charge on the collector. The collector current is

a. much higher than
b. much lower than
c. about the same as

the emitter current.

17. (c. about the same as) Most of the electrons in the emitter pass through the thin base into the collector and become collector current. A few electrons do combine with holes to produce a small base current.

The current flow in a properly biased PNP transistor is as shown in Figure 2-13. It is similar but not exactly like that in an NPN transistor.

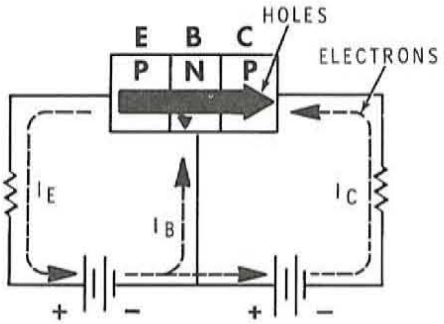


Figure 2-13
Electron and hole flow in
a properly biased PNP transistor

The current carriers in a PNP transistor are holes rather than electrons. Internally the holes flow from positive to negative. External to the transistor the current is electron flow as indicated by the dashed lines. The internal hole currents have the same relationship as electron flow in the NPN device.

$$I_C = I_E - I_B$$

The electron flow external to the transistor is perhaps more clearly expressed as

$$I_E = I_C + I_B$$

Of course these two expressions are mathematically identical since one can be derived from the other by simple algebraic manipulation.

If the emitter current is 4 ma and the collector current is 3.85 ma, what is the base current? I_B = _____

18. (.15 ma or 150μA) The base current is the difference between the emitter and collector currents or

$$I_B = I_E - I_C$$
$$I_B = 4 - 3.85 = .15 \text{ ma}$$

The collector current is less than the emitter current by the amount of the base current.

The ratio of the collector to emitter current is approximately one because in most cases the collector current is very nearly equal to the emitter current. This ratio is called the forward current gain (α or alpha).

$$\alpha = \frac{I_C}{I_E} \approx 1 \text{ since } I_C \approx I_E$$

($\approx$means approximately equal to)

Practical values of alpha run in the .95 to .99 range. The higher the gain the better the transistor.

Using the values in the previous example (I_E = 4 ma, I_C = 3.85 ma) what is the current gain alpha? _____

19. $$(\alpha = \frac{I_C}{I_E} = \frac{3.85}{4} = .9625)$$

While alpha is always less than one, we still refer to this current ratio as a gain.

Figure 2-14 below shows another way of connecting the bias to a transistor.

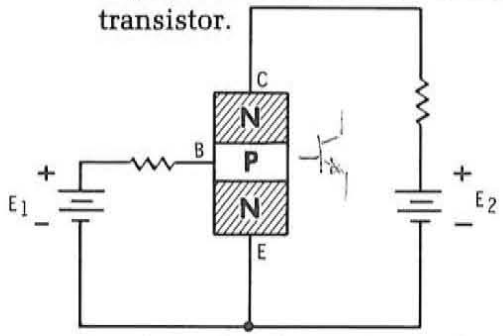


Figure 2-14
Biasing an NPN transistor with a common emitter connection

Note here that the emitter is the common element for the supply voltages rather than the base in the previous examples.

Will this transistor conduct? _____

20. (Yes) The transistor will conduct. Figure 2-15 shows the current paths.

The transistor conducts because the E-B junction is forward biased and the B-C junction is reverse biased. This reverse bias condition can be more readily seen if you consider the voltage on the base. With the E-B junction forward biased the base is .7 volts more positive than the emitter. The collector is more positive than the base with respect to the emitter because E_2 is usually much greater than .7 volts. For this reason the base is less positive or more negative than the collector, thus the reverse bias.

In Figure 2-15 what is the relationship between the various currents flowing?

a. $I_E = I_C + I_B$

b. $I_C = I_E + I_B$

c. $I_C = I_B + I_E$

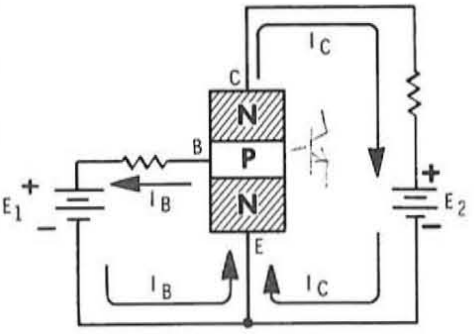


Figure 2-15
Current flow in
a common emitter biasing circuit

21. (a. $I_E = I_C + I_B$) The base and collector currents combine at the emitter to form the emitter current. The relationship expressed below

$$I_E = I_C + I_B$$

holds true for *any* transistor in *any* bias circuit configuration.

Since both bias voltages E_1 and E_2 are positive with respect to the emitter as shown in Figure 2-15 then they can be replaced by a single supply battery as shown in Figure 2-16. The result is proper bias for conduction at a considerable savings in the power supply.

The values of R_B and R_C are adjusted to provide the desired current levels. The bias voltage is labeled V_{CC} and is called the collector supply.

In Figure 2-16

a. $I_B > I_C$

b. $I_B = I_C$

c. $I_B < I_C$

Note: > means greater than
< means less than

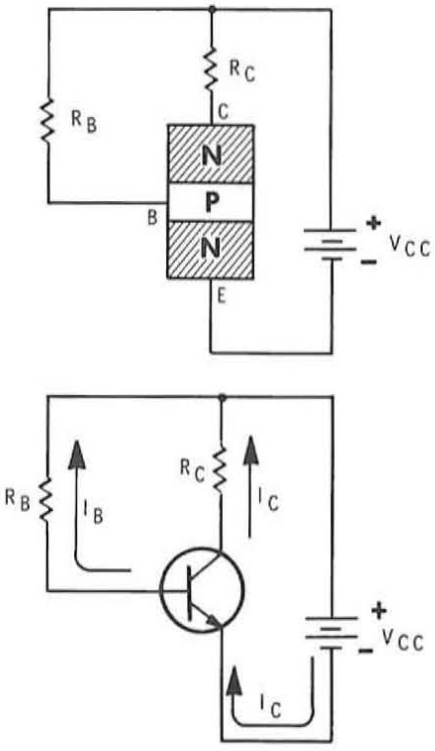


Figure 2-16 Simple voltage biasing of an NPN transistor

22. (c. $I_B < I_C$) The base current is always less than the collector current. But they are related as you learned earlier.

$$I_E = I_B + I_C$$

The ratio of the collector current to base current is another way of defining the gain of a transistor.

This is known as the dc forward current gain designated as β (beta) or h_{FE}.

$$h_{FE} = \beta = I_C/I_B$$

The higher this ratio, the higher the gain.

If I_C = 3.85 ma and I_B = .15 ma the gain is _____.

23.

$$(h_{FE} = \frac{I_C}{I_B} = \frac{3.85}{.15} = 25.67)$$

This current gain figure actually tells us how much control the base current has over the collector current. Remember that if no base current flows due to a lack of forward bias on the E-B junction, then no collector or emitter current flows. It is also true that the amount of collector current flowing depends upon the amount of base current. The collector current is directly proportional to the base current. The I_C/I_B ratio is essentially constant for a given transistor so increasing I_B increases I_C by a factor equal to h_{FE}.

If I_C is 4 ma, h_{FE} = 20 I_B =_____ ma.

24. (.2 ma or 200 μA) Since $h_{FE} = I_C/I_B$ then $I_B = I_C/h_{FE}$ so $I_B = 4/20 = .2$

If we decrease I_B by .05 ma the new I_C will be _____ ma.

25. (3 ma) $I_C = I_B\ h_{FE} = (.2 - .05)\ 20 = 3$ ma.

Note that we decreased I_B by .05 ma while I_C decreased by 1.0 ma, a 20 to 1 ratio (h_{FE}). Therefore you can see that the smaller base current can control the larger collector current.

As you change the base current to control the collector current the transistor acts essentially as a variable resistor. A high collector current means a low emitter to collector resistance and a low collector current represents a high emitter to collector resistance.

An increase in base current causes the emitter-collector resistance to _____. (increase/decrease)

26. (decrease) Increasing I_B increases I_C so that the transistor conducts more and appears as a lower resistance.

In amplifier applications a small signal such as a sine wave varies the base current to produce a larger collector current variation of the same shape.

The transistor can also be used as an on-off switch. If no base current is applied, no collector current flows so the transistor is cut off. It acts as an open switch. If a high base current is applied, the transistor conducts and acts like a very low resistance. The transistor appears as a closed switch. In this program on digital techniques, the transistor will be considered a switch.

Self Test Review

1. Current flow in N-type semiconductor material is by
   a. holes
   b. electrons
   c. positive ions
   d. negative ions

2. Current (electron) flow in a PN junction diode is from
   a. P to N
   b. N to P
   c. either a. or b.

3. To cause a current to flow in a PN junction it must be
   a. forward biased
   b. reverse biased
   c. connected to a source of ac
   d. subjected to an electric field

4. Current will flow in a PN junction diode if
   a. P is −, N is +
   b. the cathode is positive with respect to the anode.
   c. the cathode is negative with respect to the anode.
   d. P is +, N is −

5. Majority carrier flow through a transistor is from _____ through the _____ to the _____.

6. A conducting NPN transistor has which of the following bias conditions?
   a. base positive with respect to emitter and collector negative with respect to base.
   b. base negative with respect to emitter and collector negative with respect to collector.
   c. base negative with respect to emitter and collector positive with respect to collector.
   d. base positive with respect to emitter and collector positive with respect to base.

7. The gain of the common emitter transistor circuit is
   a. I_E/I_B
   b. I_C/I_E
   c. I_C/I_B
   d. I_E/I_C
8. Which expression below accurately describes the relationship between the various transistor currents?
   a. $I_C = I_E + I_B$
   b. $I_C = I_E - I_B$
   c. $I_E = I_C - I_B$
   d. $I_B = I_C + I_E$
9. The collector current is controlled by varying the _____ current.
10. The emitter-collector resistance
    a. increases
    b. decreases

    when the collector current decreases.

Answers

1. (b) electrons
2. (b) N to P or cathode to anode
3. (a) forward biased
4. (c) cathode is negative with respect to the anode and (d) P is + and N is −
5. emitter, base, collector
6. (d) base positive with respect to emitter and collector positive with respect to base
7. (c) $I_C/I_B = h_{FE}$
8. (b) $I_C = I_E - I_B$
9. base
10. (a) increases

THE BIPOLAR TRANSISTOR SWITCH

The basic component used in implementing any digital logic circuit is a switch. Modern digital integrated circuits use a high speed transistor switch as the primary component. There are two basic types of transistor switches used in implementing digital integrated circuits, the bipolar transistor and the metal oxide semiconductor field effect transistor (MOS FET). An understanding of these two devices is pertinent to the operation, capabilities and limitations of the various types of digital integrated circuits.

The primary function of a transistor switch in a digital logic circuit is to alternately connect and disconnect a load to and from the circuit power supply. In doing this the transistor switch produces two distinct voltage levels across the load which represent the binary 0 and binary 1 states. The transistor switch should make and break these connections as quickly and efficiently as possible.

The most commonly used digital switch is the bipolar transistor. In digital applications, the bipolar transistor operates as an off/on or two state device. In one state the transistor is non-conducting or cut-off and acts as essentially an open circuit. In the other state, the transistor is conducting heavily and acts as a very low resistance approaching a short circuit. A two state logic input signal is applied to the transistor to produce this on/off operation.

Modes of Operation

A bipolar transistor has three basic regions or modes of operation: cut-off, linear or active and saturation. All three of these modes are used in digital circuits, the cut-off and linear mode in non-saturated bipolar circuits and the cut-off and saturation modes in saturated bipolar circuits.

Cut-Off. In the cut-off mode the transistor is nonconducting. Both the emitter-base (E-B) and collector base (C-B) junctions are reverse biased or not biased at all to produce the cut-off state. In theory, no emitter or collector current flows, and the transistor acts as an open circuit between emitter and collector. In most practical transistors, however, the cut-off is not perfect. Because of imperfections in the semiconductor material out of which the device is made, some leakage current flows. In most modern transistors this leakage current is extremely low and for most practical applications can be neglected. However, where very high temperature operation is expected the leakage current becomes a more important consideration. In silicon transistors, the leakage current nearly doubles for each 10°C rise in temperature.

Linear. The linear or active mode of operation is characterized by a forward biased emitter-base junction and a reverse biased collector-base junction. In this mode, the transistor does conduct. Emitter and collector current flows. The emitter and collector currents are directly proportional to the base current variations. The emitter and collector currents are simply amplified versions of the base current variation. In this mode of operation, the transistor functions as a variable resistance and is used to amplify or otherwise process analog signals. This region is of concern in non-saturating digital integrated circuits.

Saturation. The third mode of bipolar transistor operation is saturation. In this mode, both the emitter-base and collector-base junctions are forward biased. The transistor conducts heavily and acts as a very low resistance. The resistance between the emitter and collector is very low, approaching that of a short circuit.

In digital applications, the bipolar transistor is usually switched between the cut-off and saturation states. As it switches, the transistor passes quickly through the linear region. The primary responsibility of the designer of a digital circuit is to see that the bipolar transistor switches as quickly as possible between cut-off and saturation and that these two states are as stable as possible. In non-saturating digital circuits, the transistors switch between cut-off and the linear region. Again, high speed is the primary requirement.

Saturated Switching Circuits

Figure 2-17 shows the most common form of saturated bipolar transistor logic switch. Here,the transistor is connected as a shunt switch since it is in parallel with the output load R_L. This circuit is also known as a transistor logic inverter.

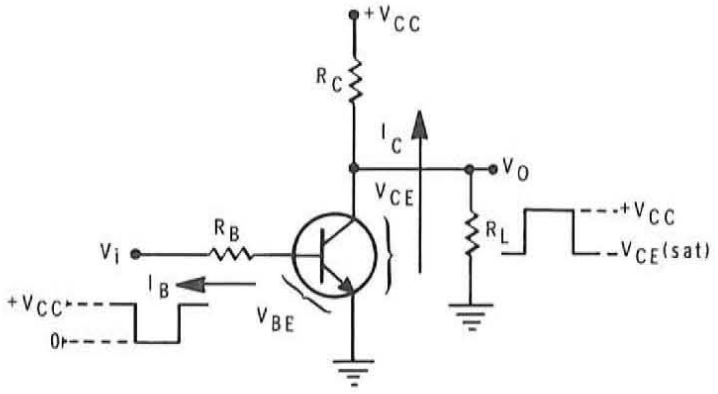


Figure 2-17 Basic transistor switching circuit

With an input voltage V_i of zero volts or ground, the transistor is cut-off. The emitter-base junction is not forward biased, therefore the transistor does not conduct. The only collector current flowing at this time is a minute leakage current. The output voltage V_o, with no load, is equal to the supply voltage V_{CC} as seen through collector resistor R_C. If a finite resistive load R_L is connected between the output and ground V_o will be some value less than V_{CC} and dependent upon the division ratio between R_C and R_L.

$$V_O = V_{CC}\left(\frac{R_L}{R_C + R_L}\right)$$

When an input voltage V_i of sufficient amplitude is applied to base resistor R_B, the emitter-base junction will become forward biased and the transistor will conduct. The transistor will be in the linear or saturation regions depending upon the size of V_i, the value of R_B and the gain (Beta or h_{FE}) of the transistor.

Figure 2-18 shows the typical input and output waveforms of a transistor switching circuit. The input switches between zero volts (LOW) and V_i (HIGH). When the input is LOW, the transistor is cut-off so you see an output voltage V_o that is equal to V_{CC} or some value slightly less (HIGH). When the input is HIGH, the transistor saturates and acts as a low resistance. The output voltage V_o is the collector-emitter saturation voltage V_{CE} (sat) which is only a few tenths of a volt (LOW). As you can see, the output is HIGH when the input is LOW, and the output is LOW when the input is HIGH. The input and output signals are always opposite one another. This is the reason for the name inverter.

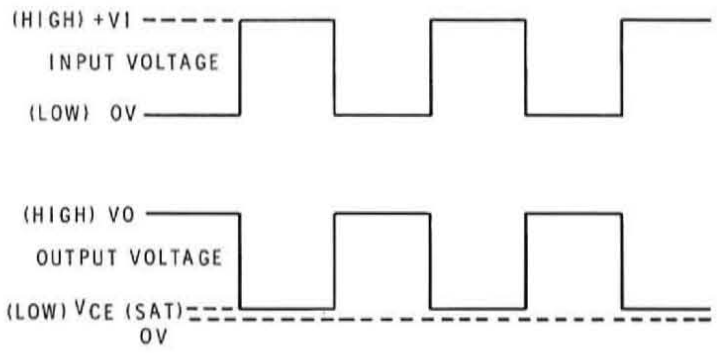


Figure 2-18 Input and output waveforms of a shunt transistor switching circuit

In a digital circuit the magnitude of V_i and R_B are such that sufficient base current flows in order to cause the transistor to saturate. This condition occurs when the actual base current I_B is greater than the ratio of the collector current I_C to the dc forward current transfer ratio h_{FE} (also known as the dc current gain or Beta).

$$I_B > \frac{I_C}{h_{FE}} \text{ (for saturation)}$$

The base current is a direct function of the applied input voltage V_i and the value of the base resistor R_B. This relationship is

$$I_B = \frac{V_i - V_{BE}}{R_B}$$

where V_{BE} is the voltage across the forward biased emitter-base junction.

As you can recall, the ratio of the collector current (I_C) to the base current (I_B) in a common emitter circuit is known as the dc forward current transfer ratio or h_{FE}. This ratio

$$h_{FE} = \frac{I_C}{I_B}$$

expresses the effective gain of the device or the ability of the base current to control the larger collector current. The greater this ratio, the higher the gain.

By algebraically rearranging this expression, we can calculate the base current for a given collector current and gain.

$$I_B = \frac{I_C}{h_{FE}}$$

If we design the circuit so that the base current is greater than this ratio, the transistor will saturate. That is, both emitter-base and collector-base junctions will become forward biased. In this state the transistor is conducting heavily and the resistance between the emitter and collector is very low. For typical switching transistors this value of resistance is in the 5 to 30 ohms range. The voltage drop between the collector and emitter during saturation V_{CE} (sat) is only several tenths of a volt. This is very low compared to the supply voltage V_{CC} and therefore for most practical purposes is considered to be nearly zero volts.

During saturation the amount of emitter and collector current flowing becomes basically a function of the value of the supply voltage V_{CC} and the collector resistance R_C. Because the voltage drop across the transistor is essentially zero, the collector current can be found from the expression

$$I_C = \frac{V_{CC} - V_{CE}\,(sat)}{R_C} \approx \frac{V_{CC}}{R_C}$$

This relationship holds true only if sufficient base current flows to saturate the transistor. If the value of the base current is less than the ratio of I_C/h_{FE}, the transistor will be operating in the linear region. The emitter-base junction will be forward biased but the collector base junction will be reverse biased. The collector-emitter voltage V_{CE} will be correspondingly higher.

There are two ways you can determine whether a transistor is saturated or operating in the linear region. The first method is to measure the junction potentials on the transistor. When measuring these voltages it is important to note the polarity of each transistor element with respect to the other. By knowing the magnitudes of the junction voltages and their relative polarities you can establish the state of the transistor.

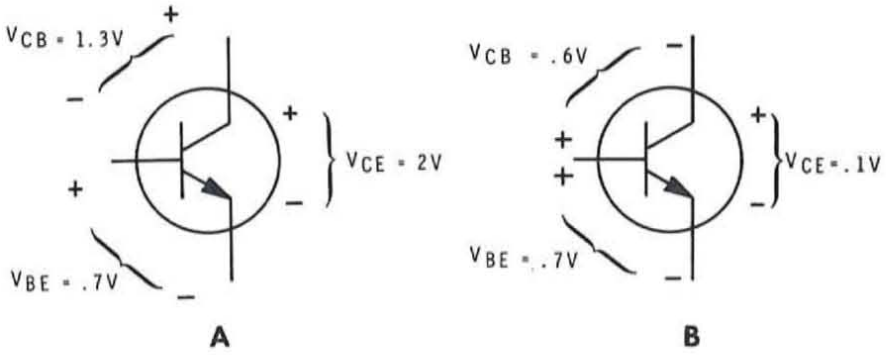


Figure 2-19 Polarity and voltage relationships in a conducting transistor (A) linear operation and (B) saturation

Figure 2-19 shows typical junction voltages for an NPN transistor both in the saturated and unsaturated states. The transistor in Figure 2-19A is operating in the linear or active region. The emitter-base junction is forward biased because junction voltage V_{BE} is of the proper polarity. A conducting junction in a silicon transistor typically has a voltage drop of approximately .7 volt. Observing the collector-base junction we see that the voltage across it (V_{CB}) is 1.3 volts with the collector being more positive than the base. This indicates a reverse biased condition on the collector-base junction. The voltage drop between the emitter and collector V_{CE} is two volts. Note the relationship between V_{CE}, V_{BE} and V_{CB}.

$$V_{CE} = V_{BE} + V_{CB}$$

In Figure 2-19B, the transistor is saturated. Again V_{BE} is approximately .7 volt with the polarity indicated. The big difference however is the polarity change in V_{CB}. Here the base is more positive than the collector indicating a forward biased condition on this junction. The junction voltage drop is approximately .6 volt. Again note that the collector-emitter voltage V_{CE} is the *algebraic* sum of (or difference between) V_{CB} and V_{BE} and in this case is only .7 − .6 = .1 volt. Because of this low voltage drop the effective resistance of the transistor is extremely low. Another beneficial characteristic of saturated operation is that the low collector-emitter voltage greatly minimizes the power dissipation in the conducting transistor. The power dissipation is

$$P = V_{CE} \cdot I_C$$

With V_{CE} so low during saturation, the power dissipation is also very low even though the collector current may be large.

The other method of determining whether or not a transistor is in saturation is to find both the base and collector current through actual circuit measurements and then determine if the base current is less than or greater than the ratio of the collector current and the dc current gain h_{FE}. As indicated before, if $I_B > I_C/h_{FE}$ then the transistor is saturated. If $I_B < I_C/h_{FE}$, the transistor is operating in its active region. The actual value of h_{FE} depends upon the type of transistor being used, the current level in the transistor, its temperature and other factors. The current gain value varies even among transistors of the same type. To ensure saturation in a switching transistor, designers generally make the base resistor small enough to produce a base current with a given minimum logic input voltage that is greater than the I_C/h_{FE} ratio. This safety factor is necessary in order to ensure saturation under all conditions. When the base current is greater than the I_C/h_{FE} ratio, we say that we are overdriving the base.

Self Test Review

11. The voltage drop across a conducting PN junction in a silicon transistor is approximately _____ volts.
12. The collector and base currents in a transistor inverter are measured and found to be $I_C = 10$ ma, $I_B = .5$ ma. The transistor h_{FE} is 15. Is the transistor saturated? _____
13. A PNP transistor has the following junction voltages $V_{BE} = .7$ volts, base negative with respect to emitter. $V_{CB} = .5$ volts, collector positive with respect to base. Is the transistor saturated? _____
14. When a transistor is saturated it acts as a (n)
    a. very low resistance
    b. very high resistance
    c. open circuit
    d. variable resistance
15. To act as an open circuit, a transistor must be operating in which mode?
    a. linear
    b. saturation
    c. cut-off
16. Another name for a saturated shunt transistor switch is _____.

Answers

11. .7
12. No. The transistor is not saturated since
    $I_B < I_C/h_{FE}$
    $I_B = I_C/h_{FE} = 10/15 = .666$ ma
    Actual $I_B = .5$ ma.
    I_B must be greater than I_C/h_{FE} for saturation.
13. Yes, the transistor is saturated. Both junctions are forward biased.
14. (a) Very low resistance
15. (c) Cut off
16. inverter

Switching Speed

One of the most important characteristics of a logic circuit is its ability to switch rapidly between the binary logic levels. This switching speed is affected by the transistor characteristics, the circuit component values, stray capacitance and inductance, the current and voltage levels in the circuit and the specific circuit configuration. When the input signal to a digital circuit changes from one logic level to the other, the output of the circuit does not change instantaneously in response. Instead there is a delay time existing between the change in the input signal and the corresponding change in the output. This time lag is generally referred to as propagation delay.

The turn on time of a transistor is primarily a function of the transistor characteristics and the amount of base drive applied to the circuit. A heavy base current helps to ensure a rapid turn on.

The turn off time delay is affected mainly by the transistor characteristics. The turn off of the transistor is delayed because of storage time. When a transistor is saturated, an excess of minority carriers (holes in an NPN and electrons in a PNP transistor) build up in the collector-base junction region. This charge storage keeps the transistor conducting even with the base drive removed. It takes a finite period of time for this charge to be removed so that the transistor begins to come out of saturation. This storage time is a function of the transistor characteristics and the amount of base drive.

By using the proper transistors, circuit configuration and component values, the switching delay times can be significantly reduced. Despite all of the factors that limit the switching speed, modern high speed switching transistors can change from one state to the next in only a matter of nanoseconds (10^{-9} seconds).

Non-Saturating Switching Circuits

The most serious limitation to the switching speed of a bipolar transistor is the storage time associated with the condition of saturation. The charge storage build up in the collector-base region during saturation takes a finite time to be cleared away in order to turn the transistor off. This storage time is the most significant part of the turn off time and therefore any means of minimizing it will greatly increase the switching speed of the transistor. Special bipolar switching transistors have been designed to help minimize this storage time effect and external circuitry can be adjusted to minimize it to some degree. The obvious way to increase switching speeds, therefore, is to avoid saturation. By keeping the transistor from going into saturation no charge storage occurs therefore very high switching speeds can be achieved. A number of logic circuits have been designed using non-saturating bipolar transistor switches. The transistors switch between the cut-off and linear regions. Such circuits are capable of switching at frequencies as high as 1 GHz.

Self Test Review

17. The finite time that it takes transistor logic switches to turn on and off is called _____ _____.
18. The turn on delay is a function of transistor characteristics and _____ _____.
19. The turn off delay is caused primarily by _____ _____.
20. Non-saturating logic circuits have a faster switching speed than saturated circuits.
    a. True
    b. False

Answers

17. propagation delay
18. base drive
19. charge storage
20. a. True

DESIGNING A SATURATED SWITCH LOGIC INVERTER

While most modern digital equipment is implemented with integrated circuits it is sometimes necessary or desirable to supplement the IC with a descrete component circuit to perform a special function. This includes things such as logic level conversion, driving an indicator light such as an incandescent lamp or light emitting diode (LED) or operating a relay. All of these circuits use a saturated bipolar transistor switch. Several examples are given in Figure 2-20.

The circuit in Figure 2-20A is simply an inverter where the input and output logic levels may or may not be equal. Such a circuit is useful in interfacing different types of logic circuits. In Figure 2-20B, the LED will light when an input voltage V_i is applied. The transistor acts as an on/off switch controlled by V_i. This is also true in the relay driver circuit of Figure 2-20C. Contacts A and B of relay K1 are normally open (N.O.) when V_i is zero. When V_i becomes sufficiently positive, the transistor saturates and K_1 is energized. The magnetic field produced by the relay coil closes contacts A and B. Diode D_1 is used to protect the transistor when the input voltage is removed. When the transistor cuts off the magnetic field the coil collapses thereby inducing a high negative voltage spike that can damage the transistor. The voltage spike causes D_1 to conduct and clamp the collector voltage to a safe level.

Such circuits are so common that it is desirable to know how to design them. The procedure is simple as you will see here.

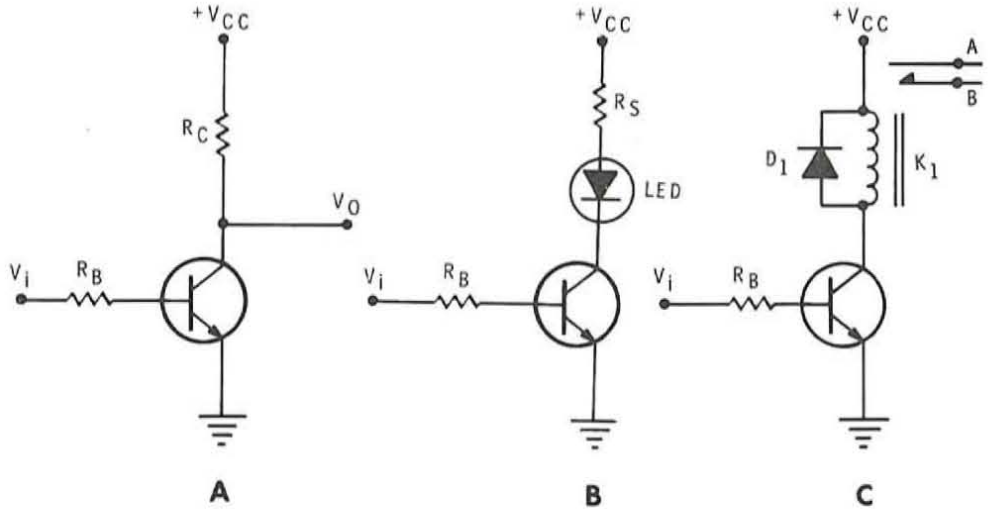


Figure 2-20
Bipolar transistor switch used as a logic inverter (A) an LED indicator driver (B), and a relay driver (C)

Procedure

1. Define the load.

   For a lamp or relay driver, the characteristics of the lamp or relay are given. These usually include a rated voltage (V_L), current and/or resistance. If the circuit is an inverter used to supply a signal to an external load, the load voltage and current or load resistance must be given.

2. Specify a supply voltage.

   The supply voltage (V_{CC}) will usually be equal to or higher than the desired load voltage. Normally, the circuit will operate from an existing supply of some standard value such as +5 volts, +12 volts, etc.

3. Select a suitable transistor.

   A wide variety of types are available. The exact application will guide you in its selection. A transistor designed for switching rather than linear applications is usually preferred. The voltage and current ratings will be determined by the load and supply characteristics. The collector current and voltage breakdown ratings should be at least twice the operating characteristics. Gain (h_{FE}) and operating speed requirements will be dictated by the application. The exact transistor characteristics can be determined from the manufacturer's data sheets.

4. Determine the value of any series dropping resistor.

   If the supply voltage is larger than the load (lamp, relay, etc.) voltage, then some series dropping resistor (R_S) will be needed. See Figure 2-20B. The voltage across this resistance will be the supply voltage (V_{CC}) less the load voltage (V_L) and the transistor saturation voltage V_{CE} (sat). The resistance can then be found with the expression

$$R_S = \frac{V_{CC} - V_L - V_{CE}\ (\text{sat})}{I_C}$$

   where I_C is the load current and the collector current V_{CE} (sat) is very low so can be considered zero. Use the closest standard resistor value. This step does not apply to an inverter with only a collector resistor.

5. Specify an output voltage.

If the circuit being designed is an inverter with a shunt load, the desired output voltage (V_o) should be specified. It will be some value less than V_{CC} depending upon the values of R_C and R_L. See Figure 2-21.

$$V_o = V_{CC} \frac{R_L}{R_C + R_L}$$

If there is no shunt load, $V_o = V_{CC}$.

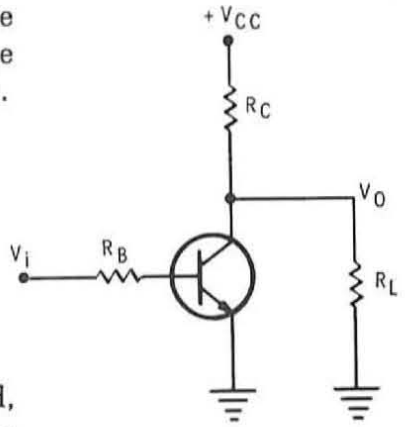


Figure 2-21
Logic inverter with shunt load

6. Determine the value of the collector resistor.

If the circuit being designed is an inverter with a shunt load to ground, the collector resistor R_C value can be calculated if the supply voltage (V_{CC}), load resistance (R_L) and desired output voltage (V_o) are known. Since

$$V_o = V_{CC} \left(\frac{R_L}{R_C + R_L}\right)$$

The collector resistance can be found by rearranging this expression.

$$R_C = \frac{R_L (V_{CC} - V_o)}{V_o}$$

Use the closest standard value of resistance.

7. Determine the collector current.

This is the load current specified earlier for lamp or relay drivers. For the inverter arrangement described in Step 6, the current is

$$I_C = \frac{V_{CC} - V_{CE}\,(\text{sat})}{R_C} \approx \frac{V_{CC}}{R_C}$$

Since V_{CE} (sat) is usually only several tenths of a volt it can be considered negligible or zero in the above expression.

8. Calculate the base current.

Knowing the gain (h_{FE}) from the manufacturer's data sheet and the collector current (I_c), the base current (I_B) can be found.

$$h_{FE} = \frac{I_C}{I_B} \quad \text{therefore } I_B = I_C/h_{FE}$$

Use the minimum value of h_{FE} quoted in the data sheet. To provide some overdrive and ensure saturation it is desirable to provide some safety factor by derating the h_{FE} by a factor of 2 (or more if desired). Therefore

$$I_B = \frac{I_C}{h_{FE}/2} \quad \text{or} \quad I_B = \frac{2\ I_C}{h_{FE}\ (\text{min})}$$

9. Calculate the base resistor.

The base resistor (R_B) is found with the expression below.

$$R_B = \frac{V_i - V_{BE}}{I_B}$$

Here V_i is the lowest expected value of base drive voltage. It is the binary 1 voltage level for positive logic. V_{BE} of course is the emitter-base voltage drop which is typically .7 volts for a silicon transistor.

If the circuit being designed is to be driven by another inverter as in Figure 2-22 its supply voltage and collector resistance should be considered.

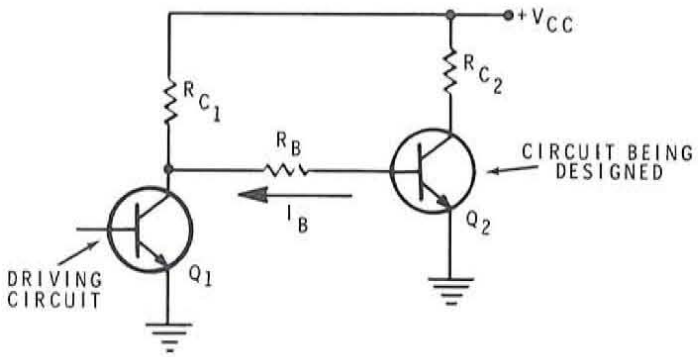


Figure 2-22

When Q_1 cuts off, the driver circuit will be activated by I_B flowing through R_B and the collector resistor R_{C1} of the driving circuit. In this case,

$$R_B = \frac{V_{CC} - I_B R_{C1} - V_{BE}}{I_B}$$

Use the closest lower standard resistance value.

The following examples will illustrate the procedure for two practical applications.

Example Application 1

Design a driver for an LED indicator. The steps below correspond to those in the procedure. See Figure 2-20B.

1. The load is a light emitting diode indicator whose normal brilliance is obtained with 20 ma of current. Its normal operating voltage, the load voltage drop (V_L), is 1.7 volts at this current value.
2. The supply voltage V_{CC} is +5 volts.
3. A type MPSA20 silicon transistor will be used. h_{FE} (min) = 100.
4. Since the LED voltage drop is less than the supply voltage a series dropping resistor is needed. The load (collector) current is 20 ma.

$$R_S = \frac{V_{CC} - V_L - V_{CE}\,(\text{sat})}{I_C}$$

If we consider V_{CE} (sat) negligible then

$$R_S = \frac{5 - 1.7}{.02} = \frac{3.3}{.02} = 165 \text{ ohms}$$

A standard 150 or 180 ohm 10 percent resistor or 160 ohm 5 percent resistor could be used.

5. Not applicable.
6. Not applicable.
7. I_C = 20 ma or .02 amp.
8. $I_B = \frac{2\,I_C}{h_{FE}} = \frac{2\,(.02)}{100} = \frac{.04}{100} = .4 \text{ ma} = 400\ \mu\text{A}$

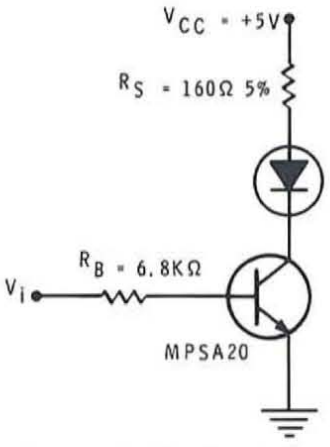


Figure 2-23 LED driver circuit: Example Application 1

9. Assume the input voltage V_i = +3.5 volts. V_{BE} = .7 volts for a silicon transistor.

$$R_B = \frac{V_I - V_{BE}}{I_B} = \frac{3.5 - .7}{.0004} = 7000 \text{ ohms}$$

A standard 6.8K 10 percent value can be used.

See Figure 2-23.

Example Application 2

Design an inverter circuit to apply +6 volts across a 600 ohm load. The supply voltage is +15 volts. The driving signal (V_i) is supplied by the +15 volt supply through a 1000 ohm collector resistor. See Figure 2-22.

1. R_L = 600 ohms V_L = 6 volts.
2. V_{CC} = +15 volts.
3. Use an MPSA20.
4. Not applicable.
5. V_O = 6 volts.
6. $$R_C = \frac{R_L(V_{CC} - V_O)}{V_O}$$

$$R_{C2} = \frac{600\ (15 - 6)}{6} = \frac{600\ (9)}{6} = 900 \text{ ohms}$$

A standard 910 ohm resistor could be used.

7. $$I_C = \frac{V_{CC}}{R_C} = \frac{15}{910} = .0165 \text{ or } 16.5 \text{ ma}$$

8. $$I_B = \frac{2\ I_C}{h_{FE}} = \frac{2\ (.0165)}{100} = .00033 \text{ amp} = .33 \text{ ma} = 330\ \mu\text{A}$$

9. $$R_B = \frac{V_{CC} - I_B\ R_{C1} - V_{BE}}{I_B}$$

$$R_B = \frac{15 - (.00033)\ (1000) - .7}{.00033} = \frac{13.97}{.00033} = 42{,}333 \text{ ohms}$$

A standard 39K ohm resistor could be used. See Figure 2-24.

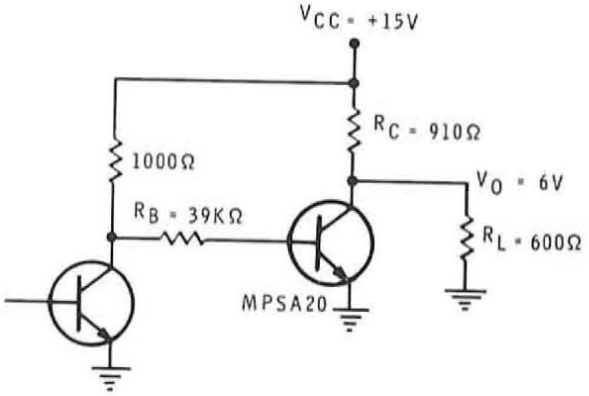


Figure 2-24 Inverter circuit: Example Application 2

Self Test Review

21. Design a transistor switch circuit that will energize a relay whose coil resistance is 400 ohms and current requirement is 30 ma. Use a supply voltage of +15 volts. The input voltage is +15 volts. Use an MPSA20 transistor. Draw the completed circuit and label all values.

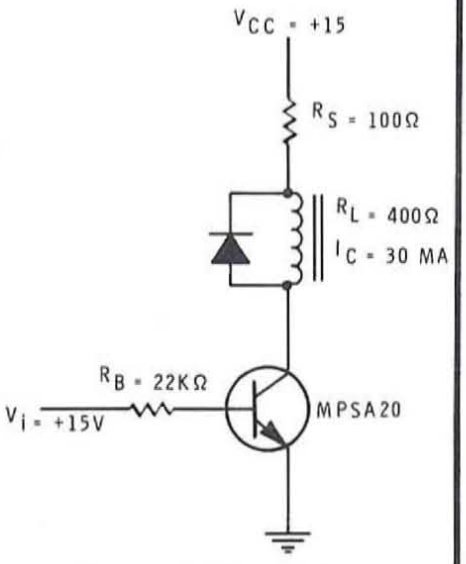


Figure 2-25 Solution to Self Test Review problem 21

Answers

21. The steps below correspond to those in the procedure.

1. $R_L = 400$ ohms, $I_L = I_C = 30$ ma, $V_L = R_L I_C = 400\ (.03) = 12$ volts
2. $V_{CC} = +15$ volts
3. MPSA20 transistor. h_{FE} (min) = 100
4. $$R_S = \frac{V_{CC} - V_L - V_{CE}}{I_C} = \frac{15 - 12}{.03} = \frac{3}{.03} = 100 \text{ ohms}$$
5. Not applicable.
6. Not applicable.
7. $I_C = I_L = 30$ ma
8. $$I_B = \frac{2I_C}{h_{FE}\ (\text{min})} = \frac{2\ (.03)}{100} = \frac{.06}{100} = .0006 \text{ ma} = 600 \text{ uA}$$
9. $$R_B = \frac{V_i - V_{BE}}{I_B} = \frac{15 - .7}{.0006} = \frac{14.3}{.0006} = 23{,}833$$

Use a standard 22 K ohm resistor.

See Figure 2-25.

EXPERIMENT 1

BIPOLAR TRANSISTOR SWITCH

OBJECTIVES: To demonstrate the operation, characteristics and design of a saturated bipolar transistor switch.

Materials Needed:

1 — NPN transistor MPSA20 (417-801)
1 — 560 Ω, 1/2-watt resistor
2 — 1 kΩ, 1/2-watt resistors
2 — 4.7 kΩ, 1/2-watt resistors
1 — 47 kΩ, 1/2-watt resistor
1 — 220 kΩ, 1/2-watt resistor

Voltmeter (vom, VTVM, etc.)
Heathkit Digital Design Experimenter (Refer to the ET-3200 manual for operational details and breadboarding procedures.)

Procedure:

1. Construct the circuit shown in Figure 2-26. The circuit receives its input from data switch SW1. You will monitor the output at the collector with a voltmeter. See Figure 2-27 for transistor base details.

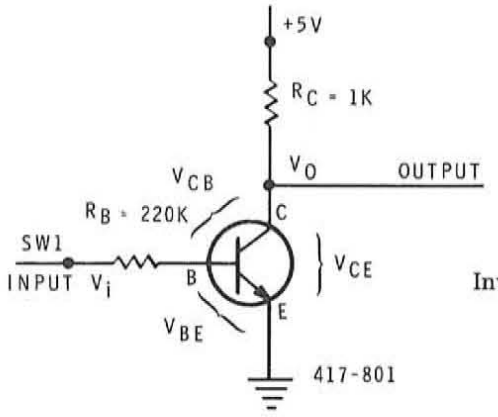


Figure 2-26
Inverter circuit for Step 1

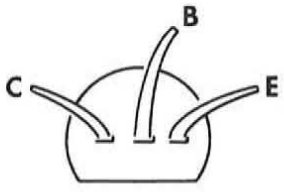


Figure 2-27
Lead connections
for 417-801 transistor

220 K

2. Set SW1 to the down (LO) position and measure the dc output voltage (V_o) with respect to ground. Record below.
   V_o = 5.0 volts
2. The input voltage (V_i) at this time is
   V_i = ϕ volts
3. Set SW1 to the up (HI) position and measure the circuit dc input voltage (V_i) with respect to ground. Record below.
   V_i = .135 volts.
   Next, measure the following transistor junction voltages: base-to-emitter (V_{BE}), base-to-collector (V_{CB}), and collector-to-emitter (V_{CE}). Record your values in Table I. Be sure to note the polarity of each voltage so that you can determine whether the junctions are foward or reverse biased. Study your results then answer the following question.
   Is the transistor saturated? No

V_{BE} 1.6V
V_{BC} -.9

TABLE I

R_B	V_{BE}	V_{CB}	$V_{CE} = V_o$
220 K	1.6V	-.9V	2.6
4.7 K	.75	-.7V	.056

4. Measure the voltage drop across the 220 K base resistor (V_{RB}) and the voltage across the collector resistor (V_{RC}) and record in Table II. Using these voltages and associated resistor values, calculate the base current (I_B) and collector current (I_C) using Ohm's law.

V_{RB}: 4V
V_{RC} 5V

$$I_B = \frac{V_{RB}}{R_B} \qquad I_C = \frac{V_{RC}}{R_C}$$

Record your values in Table II. Also calculate the ratio I_C/I_B and record in Table II.

TABLE II

	R_B = 220K	R_B = 4.7K
V_{RB}	4.0 V	3.8 V
V_{RC}	3.3V	4.8V
I_B	18.2 μA	80.9 μA
I_C	3.3 mA	4.8 mA
I_C/I_B	181.3	59.3

5. Using the criterion that states a transistor is saturated if the $I_C/I_B < h_{FE}$ and the data in Table II, determine the condition of the transistor assuming $h_{FE} = 100$.

   Is the transistor saturated?

   No

6. Replace the 220K ohm base resistor R_B with a 4.7K ohm resistor.
7. Repeat Step 3. Measure V_{BE}, V_{CB} and V_{CE} and record in Table I. Study your results.

   Is the transistor saturated? Yes
8. Repeat Step 4 recording your data in Table II.
9. Repeat Step 5. Is the transistor saturated? Yes

Discussion of Steps 1 Through 9.

In Step 1 you constructed a bipolar transistor switch. In Step 2 with the input from SW1 (LO or ground), the E-B junction is not forward biased, therefore the transistor is cut off and the output voltage you measured was $V_{CC} = +5$ volts as seen through the 1K collector resistor.

In Step 3 you applied forward bias to the emitter-base junction of the transistor from the +5 volt logic level output of SW1 through the 220K base resistor. The transistor conducts. This is indicated by the junction voltages. You should have measured a V_{BE} in the .6 to .8 volts range with the base positive with respect to the emitter. V_{CB} should have been one volt or so with the collector positive with respect to the base. The collector to emitter voltage V_{CE} should have been 1 to 4 volts with the collector the most positive element. The emitter-base junction is forward biased and the base-collector junction is reverse biased. See Figure 2-28 for a summary of the transistor junction voltage polarities for a properly biased transistor. With this arrangement, the transistor conducts but is not saturated. The transistor is operating somewhere in its linear region.

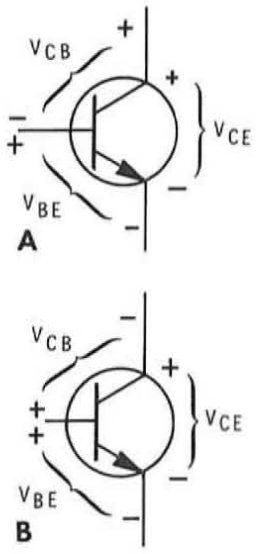


Figure 2-28 NPN Transistor Junction bias polarities

Because we do not know the exact value of h_{FE}, your voltages for V_{CB} and V_{CE} may not be exactly equal to those given above but they should be close.

In Steps 4 and 5 you determined the collector and base currents by measuring the voltage drops across the base and collector resistors then dividing by the respective resistor values. Then you determined if the ratio I_C/I_B was equal to, less then, or greater than the assumed h_{FE} value of 100. If $I_C/I_B < h_{FE}$ then the transistor is saturated. In this step you should have found I_C/I_B to be higher than h_{FE}. Obviously, the transistor is not saturated. What you calculated when you divided I_C by I_B was the true gain or h_{FE} of the transistor. It should have been greater than 100.

In Step 6, you replaced the 220 kΩ base resistor with a 4.7 kΩ resistor. This provides more base drive current. In Step 7 with +5 volts applied to the input, the transistor conducts, but this time much harder. The junction voltages should be approximately as follows: V_{BE} = .7 volt, V_{CB} = .6 volt, V_{CE} = .1 volt. The polarities of V_{BE} and V_{CE} are as before. But with the 4.7 kΩ base resistor, V_{CB} is such that the base is more positive than the collector. This indicates that the base-collector junction is forward biased whereas, with the 220 kΩ base resistor, it was reverse biased. With both the emitter-base and base-collector junctions forward biased, the transistor is saturated. The output voltage V_O or V_{CE} is the difference between V_{BE} and V_{CB}. See Figure 2-28B.

In Steps 8 and 9, you again determined I_C, I_B and I_C/I_B. In this case, you should have found I_C/I_B to be less than a nominal h_{FE} of 100. Therefore, the transistor is saturated.

10. Using the procedure outlined earlier, design a transistor switch to produce +4 volts across a 560 ohm shunt load. Use a +12-volt supply voltage and a MPSA20 (417-801) transistor (h_{FE} min = 100). The input logic signal will come from logic switch SW1 and is +5 volts as seen through a 470 Ω resistor. (See schematic of ET 3200 Digital Design Experimenter.) Calculate all values. Draw the completed circuit. Then breadboard the circuit using the closest available resistor values and check its operation. Use one of the procedures described earlier to establish that the transistor does saturate.

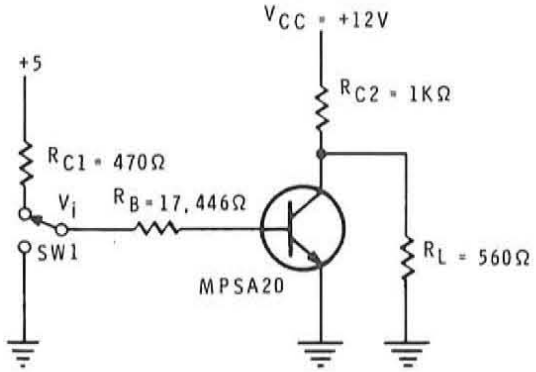


Figure 2-29 Solution to design problem in Step 10

Discussion of Step 10

Your calculations should appear like those shown below. See Figure 2-29.

$$R_{C2} = \frac{R_L (V_{cc} - V_O)}{V_O} = \frac{560\ (12 - 4)}{4} = \frac{560\ (8)}{4}$$

R_{C2} = 1120 ohms

Use a 1K ohm resistor

$$I_C = \frac{V_{CC}}{R_{C2}} = \frac{12}{1000} = .012 \text{ amp} = 12 \text{ ma}$$

$$I_B = \frac{2I_C}{h_{FE}} = \frac{2\ (.012)}{100} = \frac{.024}{100} = .00024 \text{ amp} = 240 \text{ uA}$$

$$R_B = \frac{V_{CC} - I_B R_{C1} - V_{BE}}{I_B} = \frac{5 - (.00024)\ (470) - .7}{.00024}$$

$$R_B = \frac{4.1872}{.00024} = 17{,}446 \text{ ohms}$$

A standard 15 K or 16 KΩ resistor could be used. A 10 KΩ resistor in series with a 4.7 KΩ resistor (14.7 KΩ total) could be used in breadboarding this circuit on your ET-3200.

In the calculation for R_B, V_{CC} is 5 volts since the 5 volt supply in your ET-3200 provides the basic source of base drive through the 470 ohm resistor associated with logic switch SW1. This resistor is designated R_{C1} in Figure 2-29.

MOS FIELD EFFECT TRANSISTORS

Another transistor widely used in digital integrated circuits is the enhancement mode metal oxide semiconductor field effect transistor (MOSFET). Also known as an insulated gate field effect transistor (IGFET), this device offers numerous advantages over the bipolar transistor particularly for digital work and integrated circuits. Because the MOSFET is basically a simple device, it is more easily constructed than a bipolar transistor. Since it can be made smaller than bipolar devices it permits more circuitry to be produced on a given area of semiconductor material. The cost of an integrated circuit is directly proportional to the area of the semiconductor material used to construct the circuit and the complexity of the devices used. Simple, low cost, high density circuits are readily constructed with MOSFET components.

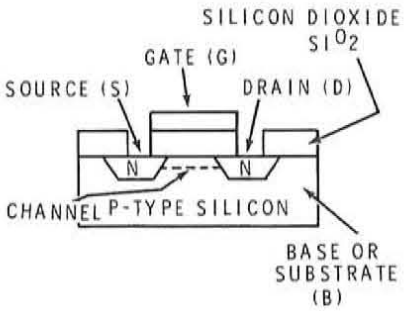


Figure 2-30 N-channel enhancement mode MOSFET

The N-channel MOSFET

Figure 2-30 shows the basic construction of an N-channel enhancement mode MOSFET. It is constructed of a P-type silicon base or substrate into which is diffused two N-type semiconductor material areas. These form the source and drain elements of the transistor. On top of this is diffused a thin layer of silicon dioxide, a glass insulator which isolates the source and drain regions from the remainder of the device. On top of the silicon dioxide insulator is formed a third element called the gate. The silicon dioxide insulates the gate terminal from the P-type silicon material. The gate is simply a metallized diffusion such as aluminum or a silicon conductive material that forms a capacitor with the P-type silicon base, the silicon dioxide layer acting as the dielectric. The area beneath the gate dielectric and between the source and drain is known as the channel. If the drain is made positive with respect to the source, current will flow between the source and the drain. It is the level and polarity of the voltage between the source and the gate that determines the conductivity of the channel.

With the gate source voltage equal to zero, no current flows between the source and the drain. The alternate N-type and P-type materials between source and drain effectively form two back-to-back diodes both of which are cut off. However, when the voltage applied between the gate and source exceeds a certain threshold level with the gate positive with respect to the source, an electric field will be established in the channel region. This causes the transistor to conduct and electrons will flow between the source and the drain.

The gate-source arrangement in the MOSFET acts as a capacitor. Applying a gate-source voltage charges this capacitor. The gate becomes positive and the area below the gate in the substrate becomes negative. The majority carriers in the P-type substrate (holes) will be depleted by the negative charge and the electron density will be enhanced. This negative

charge in the P-type base establishes a channel for current flow between the two N-type regions. Removing the gate-source voltage or decreasing it below the threshold level will cause the conduction to cease.

The enhancement mode MOSFET is an excellent switch. When the gate voltage is below the threshold value, the resistance between the source and the drain is extremely high and very closely approximates an open circuit. When the gate voltage is above the threshold level, the transistor conducts and the resistance between the source and the drain is very low, approximating a short circuit. Such characteristics make the enhancement mode MOSFET ideal for digital circuits.

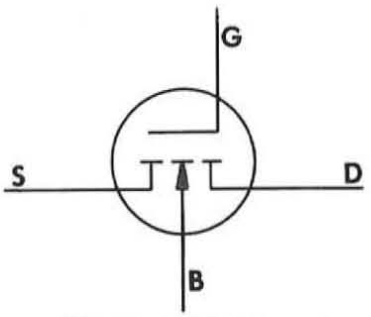


Figure 2-31 Schematic symbol for an N-channel enhancement mode MOSFET

One of the primary benefits of the MOSFET over the standard bipolar transistor is that the input impedance between source and gate is extremely high. The input impedance between the source and gate is many thousands of megohms and, in effect, is more capacitive than resistive. This high input impedance minimizes the loading of one logic circuit on the next. Figure 2-31 shows the schematic symbol normally used to represent an N-channel enhancement mode MOSFET.

The P-Channel MOSFET

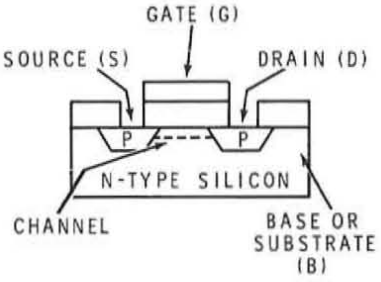


Figure 2-32 P-channel enhancement mode MOSFET

Figure 2-32 shows the construction of a P-channel enhancement mode MOSFET. It is similar in construction to the N-channel device. However, the substrate is N-type material, while the source and drain diffusions are P-type material. The symbol used to represent this device is shown in Figure 2-33. The operation of the P-channel MOSFET is similar to that for the N-channel device with the exception of the operating voltage polarities. Like the N-channel device, the P-channel MOSFET is normally off if the gate-to-source voltage is below a specific threshold value. When the gate is made negative with respect to the source and is of an amplitude beyond that of the threshold level, the transistor will conduct and current will flow between the source and the drain. In the P-channel device, the current carriers are holes instead of electrons.

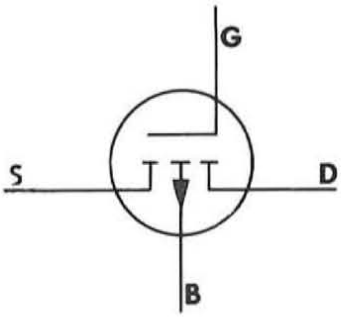


Figure 2-33 Schematic symbol of a P-channel enhancement mode MOSFET

One of the most important characteristics of the enhancement mode MOSFET is its threshold voltage, that value of gate-source voltage required to cause the transistor to conduct. There are two basic types of threshold in common use; low threshold and high threshold. The high threshold devices are easier to make and, therefore, are more common. This high threshold value is approximately three to four volts. There is circuitry available with a low threshold in the one to two volt region. Typically, P-channel devices have high thresholds, while N-channel devices have low thresholds.

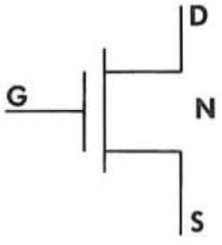


Figure 2-34 Simplified symbol of enhancement mode MOSFET

Figure 2-34 shows a simplified schematic symbol often used to represent an enhancement mode MOSFET. Because of the complexity of the standard symbols, they are rarely used. The letter P or N is written adjacent to the symbol to designate whether it is a P-channel or an N-channel device.

Bipolars vs. MOSFETs

The primary benefits of the MOSFET over the bipolar transistor are; small size, simplicity of construction, high input impedance and low power consumption. However, these advantages are somewhat offset by the major disadvantage; slow switching speeds. Because of the high impedance nature of the device and its capacitive characteristics, switching speeds are significantly lower than those for bipolar transistors. Recent advances have improved the switching speed of MOSFETs, and switching speeds in the region below 100 nanoseconds are now possible. Nevertheless, the advantages of the MOSFET over the bipolar for many applications offset this switching speed disadvantage. Bipolar transistors are still faster and offer the further advantage of being able to handle high power applications.

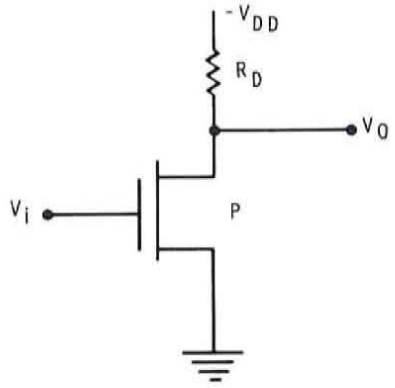


Figure 2-35
P-channel MOS inverter

MOSFET Circuits

Logic circuits are readily constructed with enhancement mode MOSFETs. Figure 2-35 shows an inverter circuit constructed with a P-channel MOSFET. With the gate input voltage (V_i) at zero, the transistor does not conduct and the output voltage (V_O) is the drain supply voltage (V_{DD}) as seen through the drain resistor (R_D). When the input voltage is made sufficiently negative beyond the threshold value, the transistor conducts and acts virtually as a short circuit. The output voltage at this time is near zero volts. An inverter using an N-channel device would be similar, but with positive logic levels and supply voltage.

In practical MOS circuits, the drain resistor (R_D) is not used. Because it occupies a substantial amount of space in an integrated circuit, it is generally eliminated and replaced by another MOSFET, biased on to act as a resistance. The transistor itself is smaller than a diffused resistor. A very popular type of MOS digital circuit combines both P-channel and N-channel devices to form what is known as a complementary MOS (CMOS) logic circuit.

Self Test Review

22. The MOSFET is also known as a IGFET.
23. To cause an N-channel enhancement mode MOSFET to conduct the gate-source voltage must be
    a. zero
    b. negative
    c. positive
    d. above the threshold level
24. The gate-source appears to external circuits primarily as a
    a. short circuit
    b. low impedance
    c. capacitor
    d. high impedance
25. The switching time of a MOSFET compared to that of a bipolar transistor is
    a. less
    b. more
    c. about the same
26. To cause a P-channel MOSFET to conduct, the gate-source voltage must be higher than the _____ and the drain must be _____ with respect to the source.

Answers

22. IGFET
23. (c) positive, gate positive with respect to the source and (d) above the threshold value
24. (c) capacitor (d) high impedance
25. (b) more
26. threshold, negative

UNIT SUMMARY

1. The basic element used to implement binary logic circuits is a switch.
2. The most commonly used switches in digital circuits are bipolar and MOS field effect transistors although conventional mechanical switches and relays are still used in some applications.
3. Bipolar transistors and MOSFETs are semiconductor devices.
4. The most common material used in making semiconductor devices is silicon. Another semiconductor, germanium, is also widely used.
5. A semiconductor is a material that has characteristics between those of conductors and insulators.
6. The basic semiconductor material, like silicon is modified to form two types of semiconductors, P-type and N-type.
7. N-type material contains an excess of electrons. Therefore, the majority current carrier is electrons.
8. P-type material contains an excess of holes. The majority current carrier is holes.
9. A hole is the absence of an electron in the crystal lattice structure of a semiconductor. Holes act like positively charged particles.
10. P-type and N-type semiconductor materials are combined to form PN junctions.
11. The simplest semiconductor device is a PN junction diode. This diode passes current freely in one direction but blocks current flow in the other direction.
12. To cause a junction diode to conduct or pass current, it must be forward biased. This is accomplished by connecting an external dc voltage to the diode with the positive terminal to the P-type material and the negative terminal to the N-type material.
13. If the negative terminal of the dc source is connected to the P-type material and the positive terminal to the N-type material, the diode will be reverse biased and no current will flow through it.
14. When a diode conducts it acts as a very low resistance or a short. When a diode does not conduct, it acts as a very high resistance or open circuit.

15. When a diode conducts it has a small-voltage drop across it, approximately .7 volts for a silicon diode and .3 volts for a germanium diode.
16. Transistors are formed by combining alternate layers of P-type and N-type materials. The result is a 3-layer, 2-junction device.
17. The two types of transistors are PNP and NPN.
18. The three transistor layers or parts are called the emitter, base and collector.
19. The basic function of a transistor is to control current flow either on a continuous or on/off basis.
20. The most common applications for transistors are amplification and switching.
21. Current flow in a transistor is from the emitter through the base to the collector.
22. To cause current to flow through a transistor the emitter-base (E-B) junction must be forward biased and the base collector (B-C) junction must be reverse biased.
23. Most of the current flowing into the emitter passes through the base into the collector. However, a very small current flows out of the base.
24. The following mathematical formulas express the current relationships in a transistor.

$$I_C \approx I_E$$

$$I_C = I_E - I_B$$

25. The collector current in a transistor is controlled by the much smaller base current.
26. A bipolar transistor has three basic modes of operation: cut-off, linear or active and saturation.
27. When the transistor is cut-off it does not conduct and therefore acts as an open circuit.
28. In linear or active operation the transistor operates as a variable resistance. The collector current is proportional to the base current.

29. When the transistor is saturated, it conducts and acts as a very low resistance or short circuit.
30. Both the E-B and B-C junctions must be forward biased to achieve saturation.
31. The most commonly used transistor switch is a shunt saturated bipolar transistor.
32. The shunt transistor switch is a logic inverter. When the input is LOW (binary 0) the output is HIGH (binary 1). When the input is HIGH, the output is LOW.
33. The two ways of determining if a transistor is saturated is to measure the junction voltages and polarities to see that both are forward biased or to measure I_C and I_B and determine if $I_B > I_C/h_{FE}$.
34. The turn-on time of a bipolar transistor switch is a function of the transistor characteristics and the amount of base drive applied.
35. The turn-off time of a saturated bipolar transistor switch is a function of the charge storage effect brought about by saturation as well as the output load capacitance and collector resistor value.
36. Non-saturated switching circuits can achieve switching speeds significantly faster than that of saturated switching circuits.
37. MOSFET means metal oxide semiconductor field effect transistor.
38. The enhancement mode MOSFET is an excellent switching component. It is smaller, easier to make and more economical than a bipolar transistor. It is widely used in large scale digital integrated circuits.
39. The switching speed of a MOSFET is significantly slower than that of a bipolar transistor.
40. Another name for the MOSFET is insulated gate field effect transistor (IGFET).
41. Both P and N-channel MOSFETs are used in digital integrated circuits.
42. P and N-channel MOSFETs are often combined to form complementary MOS logic circuits.

EXAMINATION

UNIT 2

SEMICONDUCTOR DEVICES FOR DIGITAL CIRCUITS

The following questions will test your retention and understanding of the key points in this Unit. Answer all questions first before checking your answers against the correct ones that follow the exam.

1. In Figure 2-36 identify each transistor type by filling in the blanks.

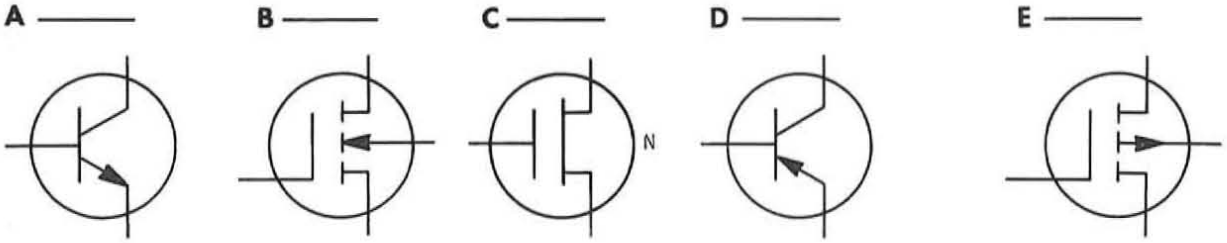


Figure 2-36 Exam question 1

2. The output of a shunt transistor logic inverter is equal to the supply voltage (binary 1) when the input is
   A. binary 1
   B. binary 0
   C. open
3. A bipolar transistor switch has an h_{FE} of 80. I_C = 18ma, I_B = .3ma. The transistor is
   A. cut-off
   B. conducting but not saturated
   C. saturated
4. Which of the following factors does *not* influence the base current in a saturated bipolar transistor switch?
   A. collector current
   B. logic input voltage
   C. base resistor
   D. V_{BE}
   E. h_{FE}

5. Which of the following logic switches is the fastest?
   A. MOSFET
   B. saturated bipolar
   C. non-saturated bipolar
   D. relay contacts.
6. If the gate-to-source voltage on a N-channel enhancement mode MOSFET is zero, the source-drain current is
   A. zero
   B. maximum
   C. not determinable with the given information
7. What factor does *not* affect the speed of the turn on of a bipolar switch?
   A. base current
   B. type of transistor
   C. shunt output capacitance
   D. base resistor value
8. What factor does *not* affect the turn off speed of a bipolar switch?
   A. transistor type
   B. base current
   C. storage time
   D. collector current
9. To cause a P-channel enhancement mode MOSFET to conduct
   A. the gate must be made positive with respect to the source.
   B. the gate-source voltage must be more negative than the threshold value.
   C. the gate-source voltage must be zero.
   D. the gate-source junction must be forward biased.
10. A silicon bipolar switching transistor with a minimum $h_{FE} = 50$ will be used as a saturated logic inverter. The supply voltage is + 5 volts. A collector resistor of 1500 ohms is specified to obtain the desired output impedance. The logic input signal is +10 volts. What value of base resistor is needed?

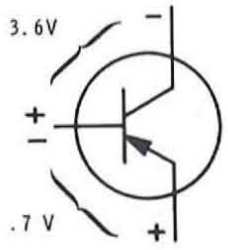


Figure 2-37 Exam question 11

11. The transistor in Figure 2-37 is
   A. cut-off
   B. conducting in the linear region
   C. saturated
12. Which of the following expressions most correctly describes the current relationships in a bipolar transistor?
   A. $I_C = I_E + I_B$
   B. $I_B = I_C + I_C$
   C. $I_E = I_C + I_B$
   D. $I_C = I_B - I_E$
   E. $I_E = I_C - I_B$

ANSWERS

UNIT 2

SEMICONDUCTOR DEVICES FOR DIGITAL CIRCUITS

1. A. NPN bipolar
   B. N-channel MOSFET
   C. N-channel MOSFET
   D. PNP bipolar
   E. P-channel MOSFET
2. B and C — binary 0 or open. If the input to a logic inverter is binary 0, usually ground or some very low voltage or if the input is open no base current flows. Therefore, the transistor does not conduct. Since it is cut off, the output is the supply voltage as seen through the collector resistor.
3. C — saturated. With $I_C = 18$ ma and $I_B = .3$ ma, $I_C/I_B = 18/.3 = 60$. If $h_{FE} > I_C/I_B$ then the transistor is saturated. $h_{FE} = 80 > I_C/I_B = 60$.
4. A — collector current. The collector current does not influence or control the base current in a saturated switch.
5. C — non-saturated bipolar. This is the fastest transistor logic switch.
6. A — zero. If the gate-source voltage in a MOSFET is zero, the transistor will be cut off so its source to drain current will be zero.
7. C — shunt output capacitance. The capacitance from the collector output to ground does not affect the turn on speed of a transistor.
8. D — collector current. The actual value of the collector current does not effect the turn off time of a transistor.

9. B — The gate-source voltage must be more negative than the threshold value. This is the main condition for conduction of a P-channel enhancement mode MOSFET.

10. $$I_C = \frac{V_{CC}}{R_C} = \frac{5}{1500} = .00333 \text{ amps} = 3.33 \text{ ma}$$

$$I_B = \frac{2I_C}{h_{FE\ (min)}} = \frac{2\ (3.33)}{50} = \frac{6.66}{50} = .1332 \text{ ma}$$

$$R_B = \frac{V_i - V_{BE}}{I_B} = \frac{10 - .7}{.1332} = 69.82 \text{ K ohms}$$

A standard 68K ohm resistor could be used.

11. B — Conducting in the linear region. The PNP transistor in Figure 2-37 is conducting since its emitter-base junction is forward biased and base-collector junction is reverse biased.

12. C — $I_E = I_C + I_B$

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UNIT 3

DIGITAL LOGIC CIRCUITS

CONTENTS

UNIT 3
DIGITAL LOGIC CIRCUITS

INTRODUCTION

All digital equipment, simple or complex, is constructed from just a few basic circuits. These circuits are called logic elements. A logic element performs some specific logic function on binary data.

There are two basic types of digital logic circuits: decision-making and memory. Decision making logic elements monitor binary inputs and produce outputs based on the input states and the operational characteristics of the logic element. Memory elements are used to store binary data.

Whether the digital equipment is a simple piece of test equipment or a large scale digital computer, this equipment is made up entirely of such logic circuits. Once you learn the basic logic elements and the most commonly used forms, you will be able to understand and determine the operation of any piece of digital equipment. By understanding how to apply these basic logic elements you will be capable of designing digital equipment.

In this unit you are going to study the basic types of digital logic circuits. You will learn the operation of decision making and memory circuits. You will also discover several special classes of logic circuits. We will also discuss the practical implementation of these logic circuits using switches and relays, discrete electronic components and integrated circuits. This unit provides the base upon which all of the remaining units in this program are built. The study of digital techniques is, in effect, a study of digital logic circuits and how they are applied. As a result, this is an extremely important background lesson.

UNIT OBJECTIVES

When you complete Unit 3 you will have the following knowledge and capabilities.

1. You will be able to list the three basic types of logic elements.
2. You will be able to write a definition for combinational logic circuits.
3. You will be able to write a definition for sequential logic circuits.
4. You will be able to draw the schematic and explain the operation of both diode and switch contact AND gates.
5. You will be able to draw the schematic and explain the operation of both diode and switch contact OR gates.
6. You will be able to draw the schematic and explain the operation of a transistor and switch contact inverter.
7. Given a list of symbols, you will be able to identify the industry standard symbols for inverters, AND, OR, NAND and NOR gates.
8. From a list of truth tables, you will be able to identify the logic functions being performed.
9. You will be able to write a truth table for any of the basic logic functions: AND, OR, NOT, NAND, NOR.
10. Given a list of logic equations you will be able to identify the logic function expressed by each.
11. You will be able to write the logic equation for any of the basic logic functions AND, OR, NAND, NOR, NOT.

UNIT ACTIVITY GUIDE

	Completion Time
☐ Play Audio Record 4, Side 1: Digital Logic Gates	_____
☐ Read Section: Types of Logic Circuits	_____
☐ Answer Self Test Review Questions 1-6.	_____
☐ Read Section: The Inverter	_____
☐ Answer Self Test Review Questions: 7-11.	_____
☐ Perform Experiment 2	_____
☐ Read section: Decision-Making Logic Elements	_____
☐ Answer Self Test Review Questions 12-23.	_____
☐ Perform Experiment 3.	_____
☐ Read Section: NAND/NOR Gates	_____
☐ Answer Self Test Review Questions 24-33.	_____
☐ Read Section: Practical Logic Circuits	_____
☐ Answer Self Test Review Questions 34-39	_____
☐ Perform Experiment 4	_____
☐ Complete Unit Examination	_____

TYPES OF LOGIC CIRCUITS

The two basic types of logic circuits are decision making and memory. Both types accept binary inputs and produce binary outputs. The nature of the output is a function of the state of the inputs and the characteristics of the particular logic circuit.

Decision-making logic circuits do exactly what their name implies; make decisions. The basic decision-making logic element is called a gate. A gate has two or more binary inputs and a single output. Figure 3-1 shows the generalized symbol used for representing a logic gate. More specific symbols are used to represent practical types of gates. There are several different types of logic gates, each performing a specific decision-making operation. The gate looks at its binary inputs, and based upon their states and its operation, it generates an appropriate output signal that reflects the decision it has made.

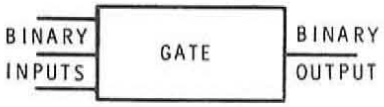


Figure 3-1
Basic symbol of a logic gate.

While many simple logic functions can be implemented with a gate, generally gates are combined to form more sophisticated and complex decision making logic networks called combinational circuits. A combinational circuit is made up of two or more gates and has two or more inputs and one or more outputs. Combinational circuits still perform a decision-making function but of a more sophisticated nature. Most combinational circuits perform some unique logic function such as decoding, encoding, multiplexing, comparison or an arithmetic operation with binary numbers. A generalized block diagram of a combinational logic circuit is shown in Figure 3-2.

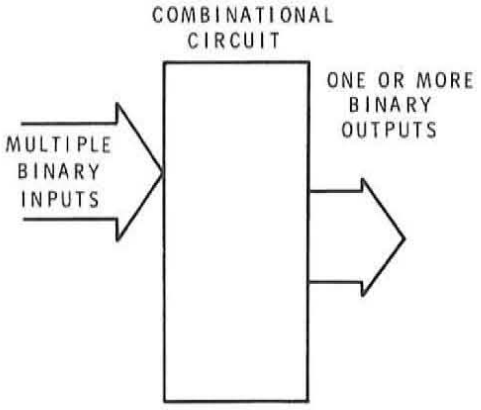


Figure 3-2
General block diagram of a combinational logic circuit.

The other type of logic element is a memory circuit. The basic memory element is a bistable storage device known as a flip-flop. This circuit has two stable states which can represent the two binary numbers 0 and 1. The circuit can be placed into either state so that it retains that state or remembers the bit stored there. Most memory circuits store a single binary bit. Many of these elements can be combined to store complete binary numbers or words.

Most memory elements are interconnected with combinational circuits to form another more sophisticated form of memory element known as a sequential circuit. A general block diagram of a sequential circuit is shown in Figure 3-3. The inputs to the sequential circuit consists of external binary data and feedback signals developed within the sequential circuit itself. The outputs of a sequential circuit are binary signals that are used to operate or control external circuits. The output of the sequential circuit is a function of the binary inputs, the binary data stored in the sequential circuit itself and the specific characteristics of this circuit.

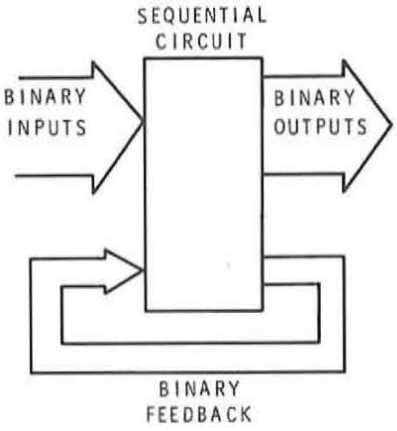


Figure 3-3
General block diagram of a sequential logic circuit.

Sequential circuits are used for a variety of operations in digital equipment. Typical sequential circuits consist of counters, shift registers, timers, sequencers and other circuits where binary data is stored and manipulated as a function of time. You will study these circuits in later units.

The three basic decision-making logic elements are the AND gate, the OR gate and the inverter. All other digital logic elements and circuits are variations or combinations of just these three basic elements. Each of these elements receive one or more binary inputs and generates a single binary output.

In order to distinguish one binary input signal from another and in order to identify both binary inputs and outputs, each signal is generally assigned a name or label. In its simplest form the label consists of a letter, a small word or mnemonic (pronounced ne-mon-ik). This label or designation indicates a specific logic signal which can assume either of the two binary states 0 or 1. In the discussions of the logic circuits presented here all inputs and outputs will be given such names and labels. In most cases a simple letter designation will be used. However, keep in mind that these designations may be words or letter and number combinations. Some typical examples are A, X, D3, CLR, JMPZ, etc.

Self Test Review

1. The two basic classifications of logic circuits are _____ and _____.
2. When multiple gates are interconnected to perform a specific function, the resulting circuit is called a _____ circuit.
3. The basic logic memory element is called a _____ and is capable of storing one _____ of data.
4. Combining memory elements with a combinational logic circuit produces a _____ logic circuit.
5. The three basic logic elements are the _____, _____, and _____.
6. A point in a logic circuit labelled STB3 can assume which of the following states:
   a. binary 0.
   b. binary 1.
   c. either binary 1 and 0.

Answers

1. decision-making, memory
2. combinational
3. flip-flop, bit
4. sequential
5. AND, OR, inverter
6. (c) either binary 0 and 1.

THE INVERTER

The simplest form of digital logic circuit is the inverter or NOT circuit. The inverter is a logic element whose output state is always opposite of its input state. If the input is a binary 0 the output is a binary 1. If the input is a binary 1, the output is a binary 0. We say that the inverter has an output that is the complement of the input. The binary states 1 and 0 are considered to be complementary.

The operation of the inverter is clearly summarized by a simple chart known as a truth table. The truth table shows all possible input states and the resulting outputs. Figure 3-4 is the truth table for an inverter. The input to the inverter is designated A while the output is labeled $\overline{A}$ (pronounced A NOT or NOT A). The bar over the letter A indicates the complement of A. Note that the truth table shows all possible input combinations and the corresponding output for each. Since the inverter has a single input, there are only two possible input combinations: 0 and 1. The output in each case is the complement or opposite of the input.

INPUT	OUTPUT
A	$\overline{A}$ B
0	1
1	0

Figure 3-4
Truth Table for logic inverter.

The symbols used to represent a logic inverter are shown in Figure 3-5. The triangle portion of the symbol represents the circuit itself while the circle designates the inversion or complementary nature of the circuit. Either of the two symbols may be used. Note the input and output labeling. Such simplified symbols are used instead of the actual electronic schematic in order to simplify the drawing and application of a logic circuit. It is the logic function and not the circuit that is the most important.

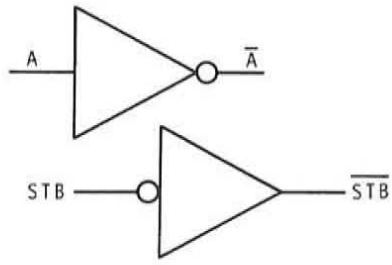


Figure 3-5
Symbols for a logic inverter.

The simplest and most widely used form of logic inverter is the transistor switching circuit shown in Figure 3-6. This inverter circuit operates with a binary input signal whose logic levels are 0 volts (or ground) and some positive voltage approximately equal to the supply voltage + Vcc. When the input B to the transistor is 0 volts or ground, the emitter-base junction of the transistor is not forward biased. Therefore, the transistor does not conduct. With the transistor cut-off, the output $\overline{B}$ with respect to ground is the supply voltage + Vcc as seen through collector resistor Rc. As you can see, with positive logic level assignments, the binary 0 input produces a binary 1 output.

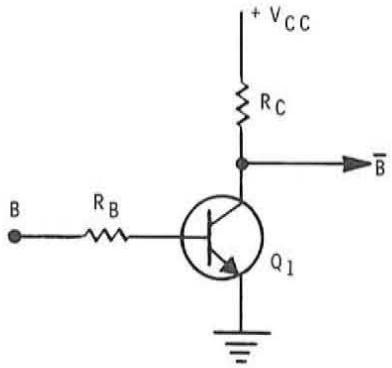


Figure 3-6
A transistor logic inverter.

Whenever a binary 1 or positive voltage level approximately equal to + Vcc is applied to the input, the emitter-base junction of the transistor becomes forward biased. Sufficient base current flows through the circuit to cause the transistor to saturate. When the transistor is saturated, both the emitter-base and base-collector junctions of the transistor are forward biased and it acts as a very low impedance. At this time, the complement output $\overline{B}$ is approximately equal to zero volts or ground as seen through the conducting transistor. The actual voltage will be equal to the saturation voltage of the transistor Vce (sat). For most good high speed switching transistors this voltage is several tenths of a volt or less and for most practical purposes can be considered to be zero. With a positive voltage binary 1 input the output is a binary 0. This circuit obviously performs logic inversion. The input and output voltage waveforms representing the operation of this circuit are shown in Figure 3-7. Most modern switching transistors are capable of turning off and on at nanosecond speeds, therefore very high frequency operation with this circuit is possible.

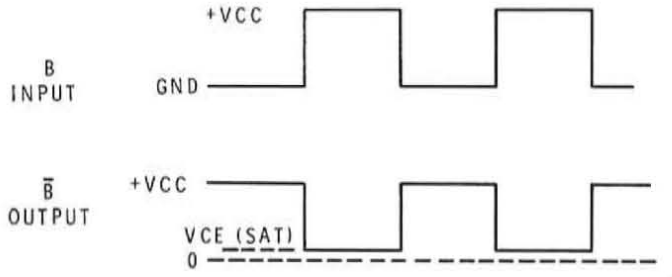


Figure 3-7
Input and output waveforms
of a transistor logic inverter.

Self Test Review

7. If the input to a logic inverter is labeled PLS, the output will be
   a. PLS
   b. SLP
   c. $\overline{PLS}$
   d. binary 0
8. The inverter input PLS is a voltage level that represents
   a. binary 0
   b. binary 1
   c. either binary 0 or binary 1
   d. Cannot be determined with information given.

9. If the input to the inverter in Figure 3-6 is simply left open and not connected to either a binary 0 or binary 1 level, what will the output be if negative logic level assignments are assumed?
   a. binary 0
   b. binary 1
   c. Cannot be determined with information given.
10. Saturation means
   a. both emitter-base and base-collector junctions reverse biased.
   b. both emitter-base and base-collector junctions forward biased.
   c. emitter-base junction forward biased, base-collector junction reverse biased.
   d. emitter-base junction reverse biased, base-collector junction forward biased.
11. The output of the inverter 2 in Figure 3-8 with a binary 1 input will be
   a. binary 0
   b. binary 1
   c. Cannot be determined with information given.

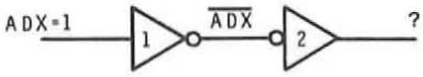


Figure 3-8

Answers

7. (c) $\overline{PLS}$ The output of an inverter is indicated by the input designation with a NOT bar over it to indicate the complement.
8. (c) either binary 0 or binary 1. The input designation PLS represents a logic variable that can assume either state.
9. (a) binary 0. If the input to the transistor logic inverter is left open, the transistor will not conduct. Therefore, the output will be $+V_{cc}$. With negative logic level assignments $+V_{cc}$ = binary 0 and zero volts or ground = binary 1.
10. (b) both emitter-base and base-collector junctions forward biased. Saturation means that the transistor conducts hard and represents a very low impedance. Both transistor junctions are forward biased.
11. (b) Binary 1. If the input ADX is binary 1 the output of inverter 1 $\overline{ADX}$ will be binary 0. With a binary 0 input to inverter 2, its output will be the complement or binary 1. The input ADX and output are the same. The output could also be called ADX. In this circuit, one inverter cancels the effect of the other. The output will be equal to the input for any even number of cascaded inverters.

EXPERIMENT 2

LOGIC INVERTER

OBJECTIVE: To demonstrate the operation and characteristics of typical discrete component and integrated circuit logic inverters.

Materials Needed

2 — MPSA20 transistor (417-801)
2 — 1 kΩ 1/2-watt resistor
2 — 4.7 kΩ 1/2-watt resistor
1 — SN7404N TTL hex inverter integrated circuit (443-18)
Heathkit ET-3200 Digital Design Experimenter
DC Voltmeter

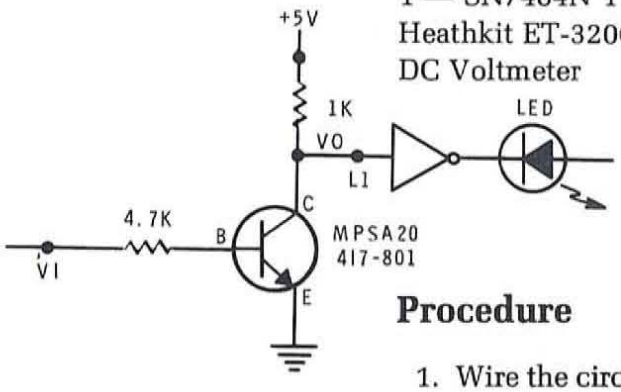
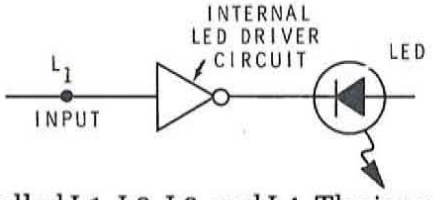


Figure 3-9

Procedure

1. Wire the circuit shown in Figure 3-9. The input is derived from logic switch SW1. You will measure the output state with your voltmeter and observe it on LED indicator L1.
2. Measure the inverter input and output voltages V_i and V_o with respect to ground for both positions of data switch SW1. Record your data in Table I.

NOTE:
The schematic diagram used to represent the logic indicators on the ET-3200 Digital Design Experimenter is shown below.



The inputs are labelled L1, L2, L3, and L4. The inverter symbol represents the internal LED driver circuit and **not** an external inverter. When the input is open or grounded, the LED is off. When the input is positive, the LED is on.

12. Set SW1 to binary 0 then binary 1 noting the output state for each input.
13. Modify your circuit to connect the L2 input of the LED indicator to pin 8 of the IC.

    How many inverters are cascaded? 4
14. Apply binary 0 and binary 1 to the circuit with SW1 again noting the corresponding output state.

    When an odd number of inverters are cascaded the output is

    a. the same as

    (b.) opposite

    the input. When an even number of inverters are cascaded, the output is

    (a.) the same as

    b. opposite

    the input.

Discussion of Steps 7 Through 14

In Steps 7, 8 and 9 you connected an integrated circuit inverter and evaluated its operation. With zero volts (binary 0) in you should have measured about +3.5 volts output (binary 1). With +5 volts input (binary 1) you should have measured about +.2 volts output (binary 0). Even with unequal input and output voltages, the circuit still performs logic inversion.

In Step 10 you determined the effect of an open input. With no input connection, the output is +.2 volts or binary 0. Since the input and output of a logic inverter are always complementary, the open input must be acting like a binary 1.

In Step 11 you cascaded 5 inverters. You should have found in Step 12 that the output was the complement of the input. Next in Step 13, you monitored the output of the fourth inverter in the chain. In Step 14 you demonstrated that the input and output were the same. From this data, you can conclude that in a chain of inverters an odd number produces a complementary input and output while with an even number of inverters the input and output will be the same.

DECISION-MAKING LOGIC ELEMENTS

The two basic types of decision-making logic elements are the AND gate and the OR gate. These are logic circuits with two or more inputs and a single output. The output state is a function of the input states and how the particular gate operates. The gate makes its decision based upon the input states and its particular function, then generates the appropriate binary output. Let's consider each of these basic gates in detail.

The AND Gate

The AND gate is a logic circuit that has two or more inputs and a single output. The operation of the gate is such that the output of the gate is a binary 1 if and only if all inputs are binary 1. If any one or more inputs are a binary 0 the output will be binary 0. The AND gate is a control circuit whose output is a binary 1 only when all inputs to the gate are in the binary 1 state at the same time.

The operation of a two input AND gate is indicated by the truth table in Figure 3-17. The inputs are designated A and B. The output is designated C. The output for all possible input combinations is indicated in the truth table. The total number of input combinations is determined by raising 2 to a power equal to the number of inputs. With two inputs, each capable of assuming either of the two binary states, the total possible number of combination inputs is $2^2 = 4$. Note that the output is binary 0 for any set of inputs where either, or both, of the inputs are binary 0. The output is binary 1 only when both inputs are binary 1.

INPUTS		OUTPUT
A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

Figure 3-17
Truth Table for an AND gate.

The basic symbol used to represent an AND gate is shown in Figure 3-18. Note that the inputs and outputs are labeled to correspond to the truth table in Figure 3-17. Keep in mind that the AND gate may have any number of logical inputs.

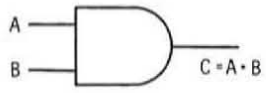


Figure 3-18
Logic symbol for AND gate.

An important point to note about the AND symbol in Figure 3-18 is the equation at the output, $C = A \cdot B$ or $C = AB$. This equation is a form of algebraic expression that is used to designate the logical function being performed. The equation expresses the output C in terms of the input variables A and B and is read "C equals A AND B". Here the AND function is designated by the dot between the two input variables A and B. The AND function is designated by an expression similar to the product of algebraic variables.

TABLE I

SW1 POSITION	V_i	V_o
DOWN	0 V	5V
UP	5V	.05V

3. From the data in Table I, answer the following questions.
   a. Does the circuit perform logic inversion? Yes
   b. What are the two output logic voltage levels assuming positive logic?
      binary 0 .05V
      binary 1 5 V
   c. Make a truth table from the data in Table I. Use positive logic and assume the circuit input is A.

in	out
0	1
1	0

4. Disconnect the 4.7 kΩ base resistor from input SW1 and let it hang free. Measure the output voltage V_o. V_o = 5V. With an open input, the output is binary 1. An open input has the same effect as a binary 0 input. (Use positive logic.)
5. Connect the free end of the 4.7 kΩ base resistor to the CLK output and set the clock frequency to 1 Hz. Connect LED indicators to the circuit inputs and outputs as shown in Figure 3-10. Observe the operation of the circuit by watching the LED indicator states and their relationship to one another. The circuit output is always the inversion of the input.

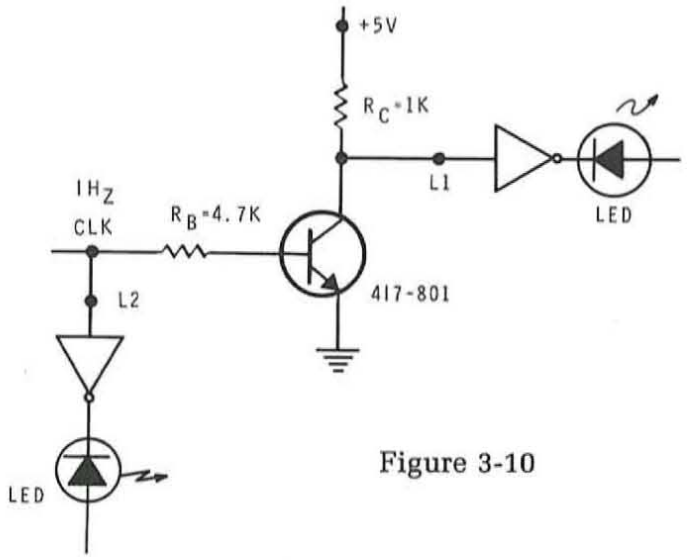


Figure 3-10

6. Modify your circuit as shown in Figure 3-11. Here you are cascading two inverter circuits. You will monitor the input on LED indicator L2 and the output of the second inverter on LED L1. Observe the input and output states as the 1 Hz clock operates the circuit.

   If the input to the circuit in Figure 3-11 is binary 1, the output will be binary ____0____. If the output is binary 0, the input must be binary ____1____.

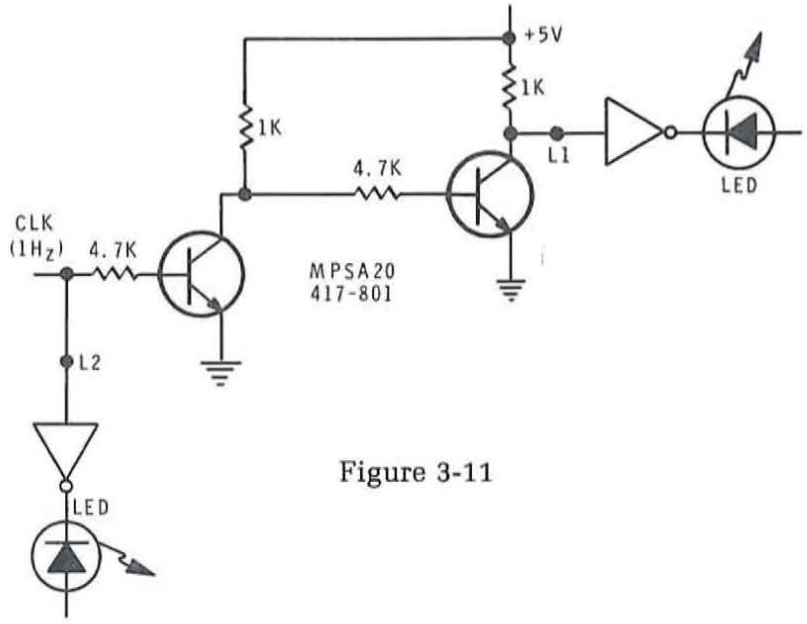


Figure 3-11

Discussion of Steps 1 Through 6

In Steps 2 and 3 you demonstrated inverter action. With input V_0 equal to zero volts, (SW1 down), the emitter-base function is not forward biased so the transistor does not conduct. The output voltage V_o is +5 volts as seen through the 1K collector resistor. With +5 volts input (SW1 up), the transistor is saturated and the output voltage is about .1 volts. Inversion is performed. The positive logic levels are binary 0 = .1V and binary 1 = +5 volts. The logic truth table you constructed for this circuit should appear as shown in Table II below.

TABLE II

INPUT	OUTPUT
A	$\overline{A}$
0	1
1	0

The input and output are complementary.

In Step 4 you disconnected the inverter input and left it open. With this condition, no forward bias is applied to the transistor so it does not conduct. The output voltage at the collector is +5 volts or binary 1. Therefore an open input produces the same effect as a binary 0 input.

In Step 5 you further demonstrated logic inverter action. The 1 Hz clock was used to drive the inverter. You observed the input and output states on the LED indicators. You should have found that the input and output states were always the opposite of one another or complementary as indicated by L1 and L2 which alternately switch on and off at a 1 Hz rate.

In Step 6 you cascaded two inverter circuits and observed their operation. You should have found that the output of the second inverter is the same as the input. One inverter cancels the effect of the other. The output state is the same as the input state when an even number of inverters is cascaded.

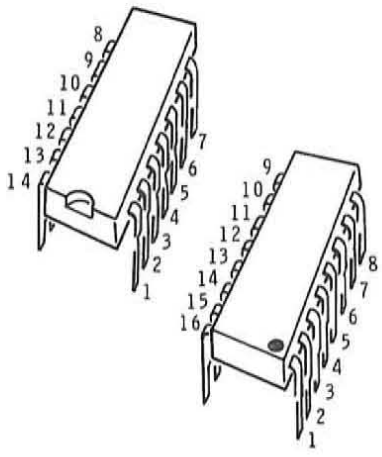


Figure 3-12
Typical 14 and 16 pin DIP ICs showing pin numbering schemes.

Integrated Circuit Hex Inverter

In the steps to follow, you will be using a typical TTL (transistor transistor logic) integrated circuit (IC) to demonstrate inverter action. This IC and all others supplied in this program are housed in a plastic dual in-line package (DIP) as shown in Figure 3-12. Both 14 and 16 pin versions are available. Note the way in which the pins are numbered. A notch or dot (indentations, etc.) is used to designate the location of pin 1.

Figure 3-13 shows the logic diagram and physical pin connections (pin out) on the SN7404N (or simply 7404) hex inverter IC. This IC contains six identical and independent logic inverters. The inputs and outputs are identified by pin number. In the diagrams used in these experiments the package outline will not be shown. Instead, only the inverter symbol with pin number labeling will be given. See the example in Figure 3-14. In an experiment, if no pin numbers are given you can use any inverter you want. Not all of the inverters in the IC will be used in every experiment. Simply ignore those not used.

Refer to the instruction manual of your ET-3200 Digital Design Experimenter for details on installing the IC on the breadboarding socket. The IC should straddle the center notch and all pins should be seated firmly. The pins are delicate so be careful when installing and removing the IC.

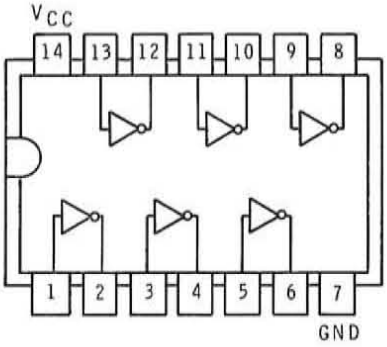


Figure 3-13
Top view of 7404 hex inverter IC showing pin assignments.

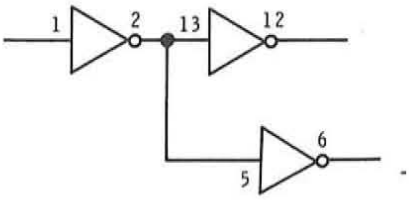


Figure 3-14

After the IC is installed, connect the power (V_{CC}) and ground leads. The supply voltage for the 7404 TTL IC is +5 volts and is applied at pin 14. Ground (GND) is connected to pin 7. Check the power and ground pin assignments for each IC you use as they vary from one type to another.

Procedure (continued)

7. Mount a 7404 hex inverter IC (part number 443-18) on the breadboarding socket and connect pin 14 to +5 volts and pin 7 to ground (GND).
8. Connect one of the inverters as shown in Figure 3-15. The input will come from logic switch SW1 and the output will be displayed on indicator L1.

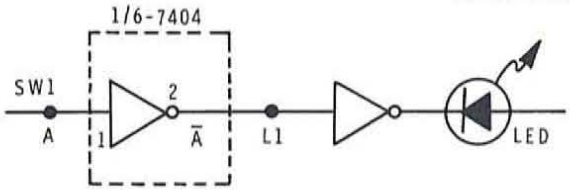


Figure 3-15

9. Apply the logic voltages to the input as shown in Table III and measure the corresponding output voltages. Record in Table III.

   Does the circuit invert? Yes

   What are the output logic levels for positive logic?

   binary 0 .1 volts
   binary 1 3.6 volts

TABLE III

A	$\overline{A}$
0V	3.6 V
+5V	.1 V

10. Remove the connection between pin 1 of the IC and SW1 so that the inverter input is open. Measure the output voltage. With the input open, the output voltage is .1 volts, or for positive logic, a binary 0. This means that an open input has the same effect as a binary 1 input.

11. Wire the circuit shown in Figure 3-16. How many inverters are cascaded? 5

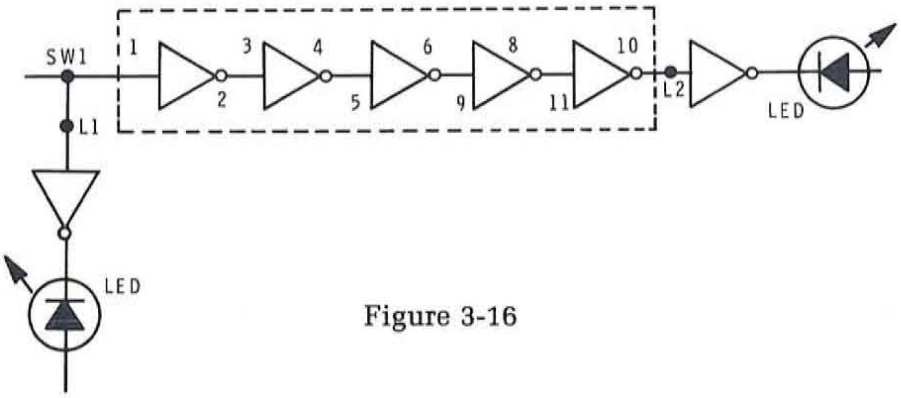


Figure 3-16

As you will see, the operation of all logic elements and gates can be expressed in the form of an algebraic equation. These expressions permit circuits to be analyzed, designed and optimized by using standard algebraic operations and special algebraic manipulations designated by rules of Boolean algebra. Boolean algebra is a special form of two state algebra that is useful in working with binary variables. You will learn more about this in a later unit.

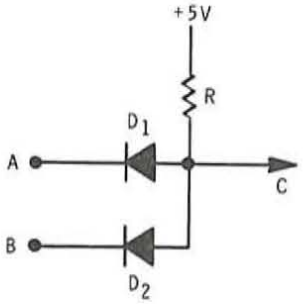


Figure 3-19
Two input diode AND gate.

The circuit in Figure 3-19 shows one electrical implementation of a logical AND gate. Here two diodes and a resistor form an electronic circuit that produces the AND function using binary signals. To analyze this circuit, assume the use of binary input signals using positive logic designations of zero volts (ground) and +5 volts. Let's also assume that perfect diodes are used. Keep in mind that in a practical circuit real diodes have a threshold voltage level before they conduct and a finite voltage drop across them during conduction.

Now let's analyze the operation of the AND circuit shown in Figure 3-19. If both inputs are a binary 0 (zero volts or ground) both diodes D1 and D2 will conduct. Assuming no forward voltage drop across the diode, the output will be zero volts. If either one of the inputs is a binary 0, while the other is at the binary 1 level (+5 volts), the diode associated with the input whose state is binary 0 will be forward biased and will conduct thereby clamping the output at the binary 0 level. (The diode associated with the input at the binary 1 level will be reverse biased, therefore it will be cut-off).

If both inputs are at the binary 1 level, neither diode D1 nor D2 will conduct and the output will be +5 volts. As you can see, the only time the output is at the binary 1 level is when both inputs are binary 1.

The operation of the AND gate shown in Figure 3-19 is fully illustrated by the voltage truth table in Figure 3-20 and the waveform timing diagram in Figure 3-21. Note that if positive logic is assumed, the voltage truth table corresponds to the logic truth table given in Figure 3-17. In the waveform diagram, both inputs A and B are shown switching at various times between the binary 0 and binary 1 levels of ground and +5 volts. The output C corresponding to this particular combination of inputs is also illustrated. Note that the only time that the output is binary 1 is when the inputs are both in the binary 1 state. The output is a binary 1 for a period of time during which the two inputs are coincidentally at the binary 1 level. The AND gate is sometimes referred to as a coincident gate.

INPUTS		OUTPUT
A	B	C
0V	0V	0V
0V	+5V	0V
+5V	0V	0V
+5V	+5V	+5V

Figure 3-20
Voltage truth table for diode AND gate.

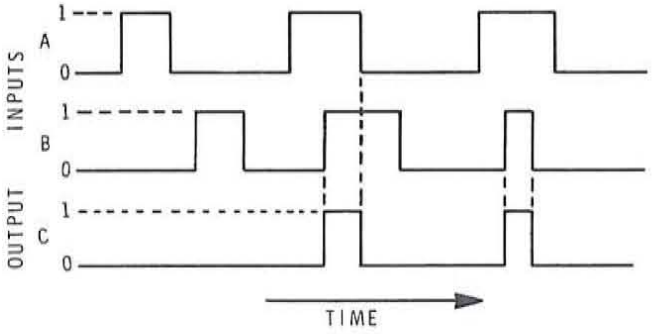


Figure 3-21
Input and output waveforms of the diode AND gate.

Figure 3-22 shows one of the most common applications of the AND gate in digital circuits. Here one input of the AND gate is used to control the passage of the other input signal to the output. The input control signal CTL enables or inhibits the passage of the other logic signal which is a train of square waves designated SQW. The output is identical to SQW during the time the CTL input is binary 1. Note the input and output waveforms as well as the logical expression for this function indicated in Figure 3-22.

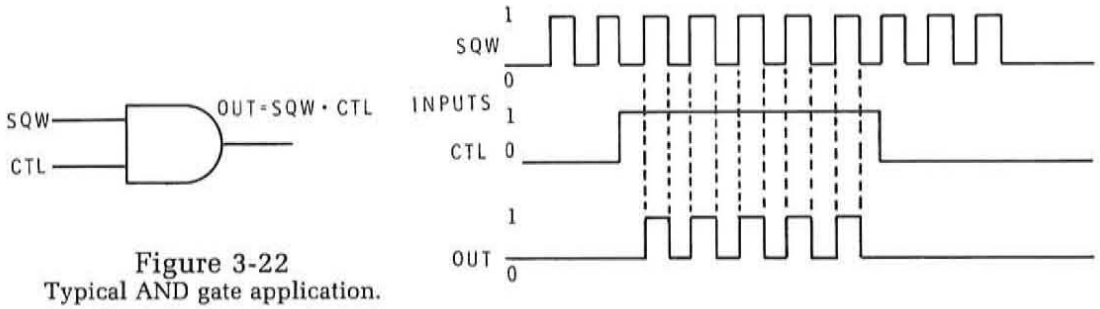


Figure 3-22
Typical AND gate application.

Remember that an AND gate may have more than two inputs, the exact number being dictated by the application. In addition, there are many other ways of implementing the logical AND function with hardware. Later in this unit and in the program you will learn about some of these circuits.

Self Test Review

12. Draw the logic symbol for an AND gate with inputs J7, K6, L4, and output F3.

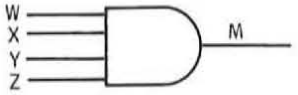


Figure 3-23
Circuit for
Self Test Review Question 14.

13. Write the logic equation for an AND gate with inputs XLT, ZMO, KMD, A3 and output TF. _____
14. The logic gate in Figure 3-23 will have how many different input combinations?
    a. 4
    b. 8
    c. 16
    d. 32
15. Write the truth table for a three-input AND gate with inputs A, B, and C and output D.
16. What is the algebraic output equation for the circuit in Figure 3-24?
    a. $P = \overline{MN}$
    b. $P = M\overline{N}$
    c. $P = \overline{M}N$
    d. $P = \overline{M}\,\overline{N}$

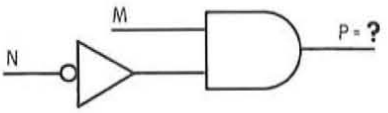


Figure 3-24
Circuit for
Self Test Review Question 16.

Answers

12. See Figure 3-25.
13. TF = XLT • ZMO • KMD • A3 The AND function is designated by the dot between each variable.
14. (c) 16 The four input gate in Figure 3-23 can have a total of $2^4 = 16$ different input combinations.

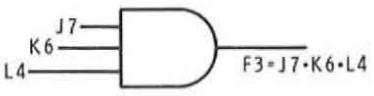


Figure 3-25
Answer to
Self Test Review Question 12.

15.

INPUTS			OUTPUT
A	B	C	D
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Figure 3-26
Truth Table for 3-input AND gate.

All possible input combinations are indicated. Note that the input states correspond to the 3-bit binary numbers representing the decimal numbers 0 through 7. This is a convenient way of listing all input state variations for a given number of input bits.

16. (b) $P = M\overline{N}$ The output of the inverter in Figure 3-24 is $\overline{N}$. This is one input to the AND gate along with input M. The output expression is constructed by writing the input variables adjacent to one another.

The OR Gate

The other basic logic element is called an OR gate. Like the AND gate it can have two or more inputs and a single output. It's operation is such that the output is a binary 1 if any one or all inputs are a binary 1. The output is binary 0 only when both inputs are binary 0.

The logical operation of a two input OR gate is expressed by the truth table in Figure 3-27. With two inputs there are $2^2 = 4$ possible input combinations as explained earlier. The truth table designates all four possible input combinations and the corresponding output. Note that the output is a binary 1 when either or both of the inputs are binary 1. The output is binary 1 if input D OR input E OR both are present.

INPUTS		OUTPUT
D	E	F
0	0	0
0	1	1
1	0	1
1	1	1

Figure 3-27
Truth Table for OR gate.

The logical symbol for an OR gate is shown in Figure 3-28. The inputs are labeled according to the truth table in Figure 3-27. Make note particularly of the output algebraic expression for the OR gate F = D + E. The plus sign is used to designate the logical OR function. The output F is expressed in terms of the input logic variables D and E.

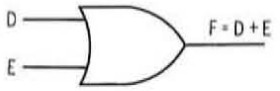


Figure 3-28
Logic symbol for OR gate.

The circuit in Figure 3-29 illustrates the implementation of the logical OR function using semiconductor diodes. This gate is similar to the AND circuit considered earlier except that the supply voltage and diode polarities are reversed. This circuit operates with logical input levels of zero and +5 volts as did the AND gate considered previously. Using positive logic designations, let's evaluate the operation of this circuit.

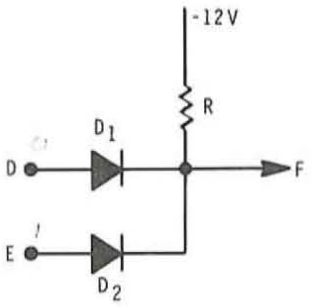


Figure 3-29
Diode OR gate.

When both inputs D and E are at binary 0 (zero inputs or ground) both diodes D1 and D2 conduct. Assuming perfect diodes, with no forward voltage drop, the output will be binary 0. If either one of the logical inputs is a binary 0, while the other is a binary 1 (+5 volts), the diode associated with the input at the binary 1 state will conduct causing the output to be +5 volts or a binary 1. The diode associated with the input at the binary 0 state will be reversed biased and will not affect the circuit. When both inputs are at the binary 1 or +5 volt level, both diodes D1 and D2 conduct and the output is a +5 volt or binary 1 level. The voltage truth table for this circuit is shown in Figure 3-30. Using positive logic, it corresponds to the table in Figure 3-27.

INPUTS		OUTPUT
D	E	F
0V	0V	0V
0V	+5V	+5V
+5V	0V	+5V
+5V	+5V	+5V

Figure 3-30
Voltage Truth
Table for the diode OR gate.

The operation of the OR gate is illustrated more fully by the waveforms shown in Figure 3-31. These diagrams show the output state for various combinations of the input voltage D and E as a function of time. Note that if one of the inputs switches to the binary 1 level the output switches to binary 1 correspondingly. The output is binary 1 when either or both inputs are binary 1. Study the waveforms in Figure 3-31 carefully at each point to be sure that you understand the circuit function.

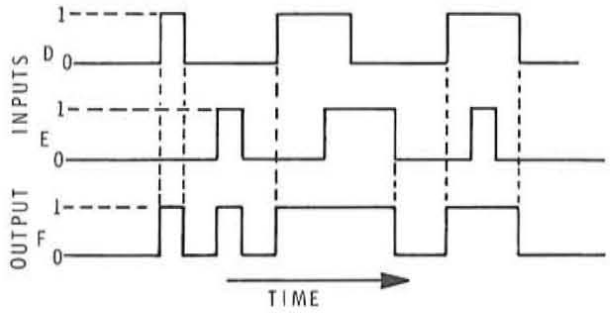


Figure 3-31
Input and output waveforms
of the diode OR gate.

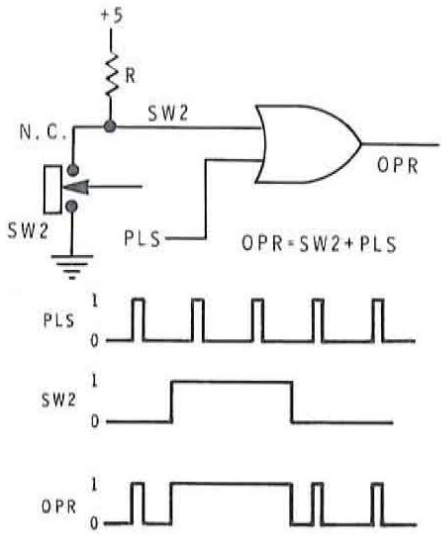


Figure 3-32
Typical OR gate application.

Figure 3-32 illustrates a typical application for the OR gate in a digital circuit. There are two inputs to the OR gate in this application: a push button switch SW2 and a train of pulses designated PLS. The output OPR will be a binary 1 when either SW2 or PLS is at the binary 1 (+5 volts) level. Switch SW2 is a normally closed pushbutton. The SW2 input to the OR gate is normally ground or binary 0. When the switch is depressed, the contacts open and the SW2 input becomes +5 volts or binary 1 level as seen through the resistor. The other input PLS is a series of pulse trains that switch momentarily between the binary 0 and binary 1 levels. Note the algebraic expression for the output, OPR = SW2 + PLS. The accompanying waveforms in Figure 3-32 illustrate the operation of the circuit. The OR gate permits either of the two inputs to control the output.

When considering the operation and application of an OR gate you should remember that this logic element can have two or more imputs as called for by the application. At the same time we have only illustrated one method of implementing the OR gate with electronic hardware. Many other circuit variations are used and these will be discussed later in the program.

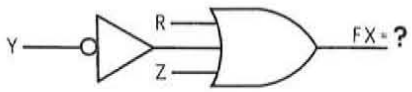


Figure 3-33
Circuit for
Self Test Review Question 18.

Self Test Review

17. Draw the logic symbol for an OR gate with inputs GB, PH, CD, SH, and output FF.
18. Write the output equation of the gate in Figure 3-33.
19. Write the truth table for a 4-input OR gate with inputs W, X, Y, Z, and output J.
20. The output of an OR gate is binary 0 when:
    a. all inputs are binary 0.
    b. any one or more inputs are binary 0.
    c. all inputs are binary 1.
    d. any one or all inputs are binary 1.
21. The logical OR function when expressed in algebraic terms is analogous to the:

    a. product
    b. sum
    c. difference
    d. quotient

Answers

17. See Figure 3-34. Note that the + signs between the two-letter input variables designate the OR operation.

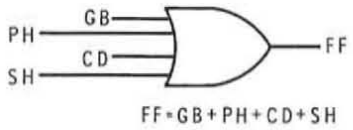


Figure 3-34
Answer to
Self Test Review Question 17.

18. $FX = R + \overline{Y} + Z$. The inverter complements the Y input before it is ORed with the other variables.

19.

INPUTS				OUTPUT
W	X	Y	Z	J
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Figure 3-35
Truth Table for 4-input OR gate.

For four input variables there are $2^4 = 16$ possible input combinations. These can be determined by simply writing the four bit numbers 0 through 15 as indicated. Note that the output is a binary 1, if any one or more inputs is binary 1.

20. (a) All outputs are binary 0. The only time the output of an OR gate is binary 0 is when all inputs are binary zero. At all other times at least one or more inputs is binary 1, thereby producing a binary 1 output.

21. (b) sum. The ORing of logic inputs is analogous to the summing algebraic variables. The AND function is analogous to the product of input variables.

The Dual Nature of Logic Gates

When we explained the operation of the diode gate circuit in Figure 3-19, we indicated that it performs the logical AND function. We proved this by considering the output voltage level for each of the four possible combinations of input voltage levels. The voltage truth table for this gate is repeated here in Figure 3-36A. In considering the operation of this circuit, we assumed the use of positive logic level assignments. By doing this we were able to translate the voltage levels given in the truth table into the table shown in Figure 3-36B. Naturally this table clearly indicates that the AND function is being performed. The output is a binary 1 only when both inputs are binary 1.

Figure 3-29 is also effect of

INPUTS		OUTPUT
A	B	C
0V	0V	0V
0V	+5V	0V
+5V	0V	0V
+5V	+5V	+5V

A

INPUTS		OUTPUT
A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

B

INPUTS		OUTPUT
A	B	C
1	1	1
1	0	1
0	1	1
0	0	0

C

Figure 3-36
Truth Table for
diode gate in Figure 3-11.

Neg logic

Now let's consider the function of this circuit when we assume negative logic level assignments. In this case the 0 volt level would represent a binary 1 and a +5 volt level would represent a binary 0. Using the original data as developed in Figure 3-36A and translating it into a truth table using binary 1's and 0's with negative logic level assignments, we obtain the truth table shown in Figure 3-36C. By studying this truth table, you will see that the circuit no longer appears to be performing the AND function. Close inspection of the truth table will reveal that the circuit is now performing the OR function since the output is a binary 1 when either one or both of the inputs is a binary 1. (The order or sequence of the inputs is not the same as that for the AND gate, but this is not important. It is the function that counts.) Our only conclusion can be that with positive logic the circuit in Figure 3-19 performs AND function but with negative logic the circuit performs the OR function. This clearly indicates that the diode gate circuit is capable of performing either of the two basic logical functions, and that function is strictly dependent upon the logic level assignments given to the input and output variables.

This dual nature of logic gates applies to any logic circuit. The diode gate that you considered in Figure 3-29 is also dual in nature. With positive logic level assignments it performs the OR function as indicated previously. However, if you analyze the circuit by using negative logic level assignments you will find that the circuit performs the AND function. Keep this important fact in mind as it will help you in analyzing, troubleshooting and designing digital circuits. You must not only know how the circuit operates electrically, but also what logic level assignments are being used.

Figure 3-37 shows the logic symbols normally used to represent gates that perform the logical AND and OR functions with negative logic level assignments. The circles at the inputs and outputs represent the effect of reversing the logic level assignments from positive to negative.

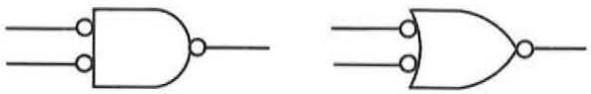


Figure 3-37
Negative logic gates

Self Test Review

22. Any logic gate can perform both AND and OR operations.
    a. True
    b. False
23. A given logic circuit performs the AND function when binary 0 = 0 volts and binary 1 = −6 volts. Reversing the logic level assignments makes the gate perform as a _____ _____ gate.

Answers

22. (a) True
23. positive OR

EXPERIMENT 3

DIODE LOGIC GATES

Objectives: To demonstrate the operation and characteristics of diode AND and OR gates.

Materials Needed

2 — 1N4149 silicon diodes (#56-56)
1 — 1 K ohm resistor — ½ watt
1 — 10 K ohm ½ watt resistor
1 — DC Voltmeter
1 — ET-3200 Heathkit Digital Design Experimenter

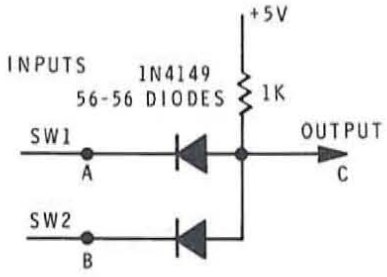


Figure 3-38

Procedure

1. Wire the circuit shown in Figure 3-38. The inputs A and B come from data switches SW1 and SW2. You will measure the output voltage C with respect to ground.
2. Using data switches SW1 and SW2, apply the input voltages indicated in Table I to the logic gate. For each set of inputs, monitor the output voltage and record in Table I.
3. Using positive logic assignments, convert the voltage levels in Table I into binary 1s and 0s and transfer to Table II.

TABLE I

A	B	C
0V	0V	.65
+5V	0V	.7
0V	+5V	.7
+5V	+5V	5V

TABLE II

A	B	C
0	0	0
1	0	0
0	1	0
1	1	1

TABLE III

A	B	C
1	1	1
0	1	1
1	0	1
0	0	0

4. Study Table II and determine the logic function being performed.
   Logic Function And
5. Convert the voltage levels in Table I into 1s and 0s using negative logic assignments and transfer to Table III.

6. Study Table III and determine the logic function being performed.
   Logic Function neg and also or
7. Modify your experiment circuit so that it appears as shown in Figure 3-39. One logic input will come from SW1. The other logic input will be a 1 Hz clock (CLK) signal. You will monitor the gate output with LED indicator L1 and the clock output on L2.

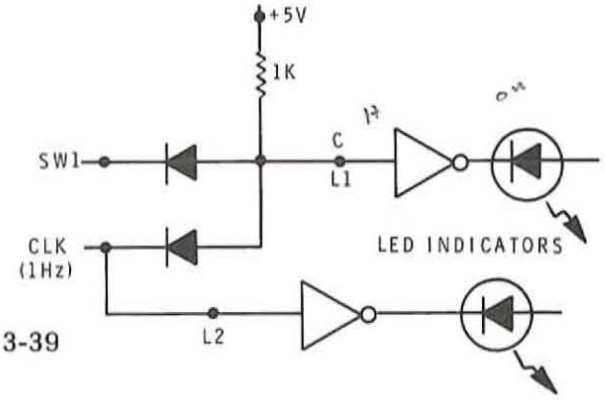


Figure 3-39

8. Set SW1 to binary 0 (down). Note the output on LED L1. Then set SW1 to binary 1 (up). Again note the output on LED L1. Explain your results.
   SW1 = 0 , Output C = off (Low)
   SW1 = 1 , Output C = Blinks
   What logic function is the gate performing? and
9. Construct the logic gate shown in Figure 3-40. Again, data switches SW1 and SW2 will supply the logic inputs D and E, and you will measure the output voltage at F with a DC voltmeter.
10. Apply the logic voltage levels indicated in Table IV to the circuit. Measure the output voltage for each set of inputs and record in Table IV.

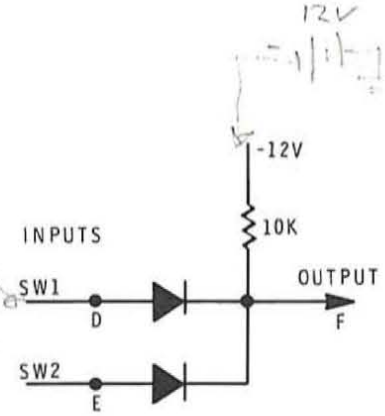


Figure 3-40

TABLE IV

D	E	F
0V	0V	-.6 V
0V	+5V	+3.6
+5V	0V	+3.6
+5V	+5V	+3.6

TABLE V

D	E	F
0	0	0
0	1	1
1	0	1
1	1	1

TABLE VI

D	E	F
1	1	1
1	0	0
0	1	0
0	0	0

11. Using positive logic assignments convert the voltage levels in Table IV into binary 1s and 0s and transfer to Table V.
12. Study Table V and determine the logic function being performed.
    Logic Function OR

13. Using negative logic assignments, convert the data in Table IV into binary 0s and 1s and transfer to Table VI.
14. Study Table VI and determine what logic function is being performed.

    Logic Function neg OR also and

15. Modify your experimental circuit so that it appears as shown in Figure 3-41. One input is from logic switch A. The other input is a 1 Hz clock signal you will monitor with LED indicator L1. You will observe the clock output on LED indicator L2.

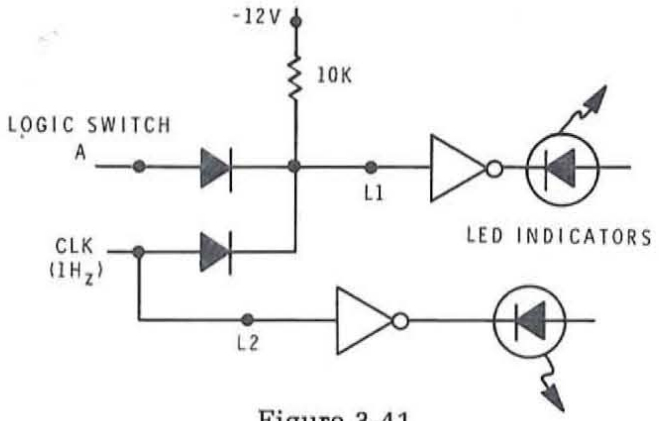


Figure 3-41

16. With logic switch A *not* depressed, the logic input to the gate is binary 0 (positive logic). Observe the gate output (L1) and clock (L2) signals. The gate output is Blinks.
17. Depress logic switch A while observing the gate output. With A depressed the output is on "1".
    What logic function is the gate performing? OR

Discussion

In this experiment you evaluated two basic types of diode logic gates. You determined their electrical performance by applying logic voltage inputs and measuring the corresponding outputs. Then using both positive and negative logic level assignments you determined the logic functions being performed. You also demonstrated several practical applications of these basic logic gates.

In Steps 1 through 6, you experimented with the gate in Figure 3-38. Your data in Tables I, II and III should appear as shown in Tables VII, VIII, and IX.

TABLE VII

A	B	C
0V	0V	+.7V
+5V	0V	+.7V
0V	+5V	+.7V
+5V	+5V	+5V

TABLE VIII

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

TABLE IX

A	B	C
1	1	1
1	0	1
0	1	1
0	0	0

From Table VII, you can see how the gate functions electrically. With either or both inputs at ground or zero volts, either one or both diodes conduct. The output, therefore, is the forward diode voltage drop of about .7 volts. When both inputs are +5 volts, neither diode conducts. The output is +5 volts as seen through the 1 kΩ resistor.

With positive logic assignments of the voltage levels in Table I (+5 volts =binary 1, 0V or +.7V = binary 0), the gate performs the AND function as you should have deduced from Table II. The output is a binary 1 only if all (both) inputs are binary 1. For all other input conditions, the output is binary 0. This is the AND function.

Next, you evaluated the gate using negative logic assignments (+5 V = binary 0, 0V or +.7 V = binary 1). From Table III, you should see that the OR function is being performed. The output is binary 1 (0V) if either one or both inputs are binary 1 (0V).

The logic gate in Figure 3-38 can perform both AND and OR operations, depending upon the logic level assignments. It is a positive AND/negative OR gate. The logic symbols representing these functions are indicated in Figure 3-42.

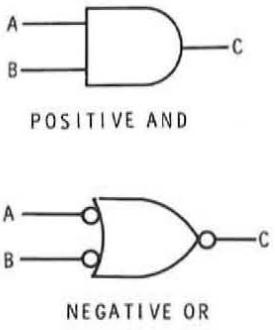


Figure 3-42

In Steps 7 and 8, you demonstrated a common application of a logic gate. Here, the gate acts as control elements to pass or inhibit the clock input. This control is handled by the SW1 input. With this input binary 0, the gate output is binary 0. The clock is inhibited and does not appear at the output. LED indicator L1 should have been off, indicating this condition. LED indicator L2 monitors the clock, so it should follow the 1 Hz pulsations.

With SW1 set to binary 1, the gate is enabled and the clock input is allowed to pass through to the output. LED indicators L1 and L2 should follow one another. Clearly, the AND logic function is being performed. This type of control gating is very widely used in digital circuits.

In Steps 9 through 14 you demonstrated the logic gate in Figure 3-40. You applied 0V and +5 V input levels and measured the output for each combination to determine its electrical characteristics. Your results in Tables IV, V and VI should be as shown in Tables X, XI, and XII below.

TABLE X

D	E	F
0V	0V	−.7V
0V	+5V	+4.3V
+5V	0V	+4.3V
+5V	+5V	+4.3V

TABLE XI

D	E	F
0	0	0
0	1	1
1	0	1
1	1	1

TABLE XII

D	E	F
1	1	1
1	0	0
0	1	0
0	0	0

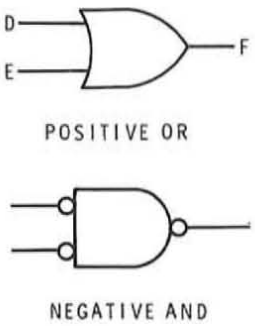


Figure 3-43

With both inputs at zero volts, both diodes conduct and the output is the forward diode voltage drop of −.7 volts. If either one or both diodes conduct the output is the input logic level (+5 volts) less the forward drop of the conducting diode or approximately +4.3 volts.

Transferring this electrical data into binary 1s and 0s, you completed Tables V and VI. Studying Tables XI and XII you can see that with positive logic assignments (+4.3 v or +5 V = binary 1, 0V or −.7 V = binary 0), the circuit performs the OR logic function since the output is binary 1 if either or both inputs is binary 1. With negative logic assignments (+4.3 V or +5 V = binary 0, 0V or −.7 V = binary 1), the gate performs the AND function. This gate is a positive OR/negative AND. The logic symbols representing these gate functions are shown in Figure 3-43.

Again you demonstrated the dual nature of a logic gate. Any logic gate can perform either the AND or OR function depending upon the logic level assignments.

Finally, you demonstrated a useful application of an OR logic gate. In Figure 3-41, two logic inputs, A and the 1 Hz clock, drive the gate. With logic switch A *not* depressed, its output is binary 0. The gate output follows the clock input. With A depressed, its output is binary 1. This turns on the output indicator and keeps it on as long as A is held down. When the clock input is binary 1 the output is binary 1. When A is binary 1, the output is binary 1. The gate is performing the OR function.

NAND/NOR GATES

While many digital circuits can be constructed with just the three basic digital logic elements — AND, OR, and NOT — most digital equipment is implemented with special versions of these circuits known as NAND and NOR gates. Such circuits are basically AND and OR gates combined with an inverter. NAND/NOR gates are the most widely used types of digital logic elements because they offer numerous advantages over the simple diode gates considered earlier. In large complex digital logic networks, it is difficult to cascade more than just a few of the simple diode logic gates. Because there is no buffering between the gates, loading problems occur and the speed of operation suffers. For that reason, it is generally desirable to combine a simple diode logic gate with some type of transistor buffer to permit more flexible interconnection of circuits. This transistor buffer is most often an inverter.

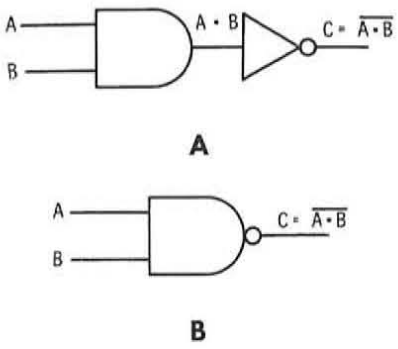


Figure 3-44
NAND gate.

NAND Gate

The term NAND is a contraction of the expression NOT-AND. A NAND gate, therefore, is an AND gate followed by an inverter. Figure 3-44A shows the basic diagram of a NAND gate. Note the algebraic output expression for the AND gate and the inverter. The entire AND output expression is inverted and indicated by the bar over it.

Figure 3-44B shows the standard symbol used for a NAND gate. It is similar to the AND symbol but a circle has been added at the output to represent the inversion that takes place.

The logical operation of the NAND gate is easy to infer from the circuit in Figure 3-44. This operation is indicated by the truth table in Figure 3-45. The NAND output is simply the complement of the AND output.

INPUTS		OUTPUT	
A	B	AND A • B	NAND $\overline{A \cdot B} = C$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

Figure 3-45
Truth Table of NAND gate.

NOR Gate

Like the NAND gate, the NOR gate is an improved logic element used for implementing decision-making logic functions. The term NOR is a contraction for the expression NOT-OR. Therefore, the NOR gate is essentially a circuit combining the logic functions of an OR gate and an inverter.

Figure 3-46A is a logical representation of a NOR gate. Figure 3-46B shows the standard symbol used to represent a NOR gate. Note that the output expression is the inverted OR function.

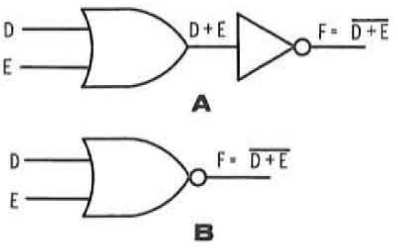


Figure 3-46
NOR gate.

INPUTS		OUTPUT	
D	E	OR D+E	NOR $\overline{D+E}=F$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

Figure 3-47
Truth Table of NOR gate.

The logical operation of a NOR gate is illustrated by the truth table in Figure 3-47. The NOR output is simply the complement of the OR function. Like any other logic gate, NAND and NOR gates may have two or more inputs as required by the application.

NAND and NOR gates can be used to implement any of three basic logical functions. For example, by tying all inputs together, either the NAND or NOR gate performs inversion. By combining the NAND or NOR gates with external inverters, the AND and OR operations can be performed.

Self Test Review

24. NAND/NOR gates are more widely used than simple AND/OR circuits because:
    a. NAND/NORs can also perform AND/OR operations.
    b. NAND/NORs are less expensive and smaller.
    c. NAND/NORs are self-buffering — this permits higher speeds and reasonable loading.
    d. AND/ORs can't perform the NOT function.

25. A 3-input NAND gate has inputs of 0, 1 and 1. The output is:
    a. binary 0
    b. binary 1

26. A 4-input NOR gate has inputs of 1, 0, 0 and 0. The output is:
    a. binary 0
    b. binary 1

27. The output equation of a NAND is:
    a. $C = A \cdot B$
    b. $C = A + B$
    c. $C = \overline{A \cdot B}$
    d. $C = \overline{A + B}$

28. The output equation for a NOR is:
    a. $F = D + E$
    b. $F = D \cdot E$
    c. $F = \overline{D \cdot E}$
    d. $F = \overline{D + E}$

Answers

24. (c) NAND/NORs are self-buffering — this permits higher speeds and reasonable loading. They are more versatile than the simple AND/OR circuits and therefore are more widely used.
25. (b) binary 1 The output of a NAND is binary 0 if and only if all inputs are binary 1. With a binary 0 on any or all inputs, the output is binary 1.
26. (a) binary 0 The output of a NOR is binary 0 if any one or more inputs is binary 1.
27. (c) $C = \overline{A \cdot B}$ is the output expression for a NAND.
28. (d) $F = \overline{D + E}$ is the output expression for a NOR.

How NAND/NOR Gates Are Used

The AND and OR logic functions can be performed by connecting inverters on the outputs of NAND and NOR gates respectively. Since the NAND and NOR functions are simply complementary logic functions of basic AND and OR operations, then it is logical to assume that the AND and OR operations can be obtained from NAND and NOR gates simply by adding an additional inversion. As stated in the previous section on inverters, the effect of one inversion is cancelled by adding a second. Cascading an even number of inverters removes the inversion function.

Figure 3-48 shows how the AND and OR operations are performed with NAND and NOR gates. But now, how is the OR function performed with a NAND gate and the AND function performed with a NOR gate?

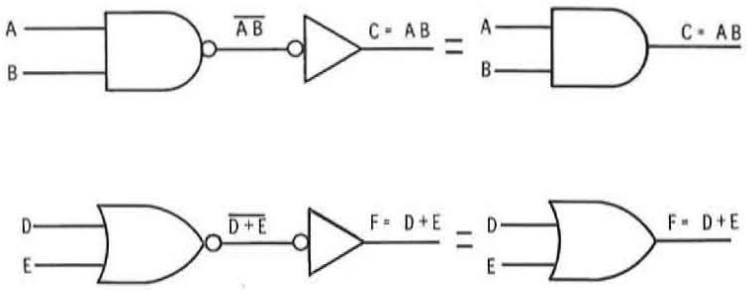


Figure 3-48
Performing AND and OR operations with NAND and NOR gates.

As mentioned earlier, any of the three basic logic functions — AND, OR, NOT — can be performed by either a NAND gate or a NOR gate. You have already seen how the AND and OR functions can be obtained with NAND and NOR gates by simply inverting the output. To obtain the other logic functions with each type of gate, inverters are used on the inputs.

INVERTED INPUTS		NAND INPUTS		OUTPUT
X	Y	A	B	C
1	1	0	0	1
1	0	0	1	1
0	1	1	0	1
0	0	1	1	0

Figure 3-49
Truth Table for NAND gate.

Figure 3-49 shows the truth table for a NAND gate. The inputs are A and B and the output is C. Now consider the effect of adding an inverter to each input as shown in Figure 3-50. These inverters simply complement the input signals. The effect is illustrated in the truth table of Figure 3-49. The input signals to the inverters are labeled X and Y. Note that they are the complements of the signals A and B respectively. Considering the two

inverters and the NAND gate as forming a single composite circuit, our inputs become X and Y instead of A and B. Output C remains the same. By observing the truth table in Figure 3-49 with this change in mind, you can now evaluate the logical function of the circuit. Disregarding the sequence of the X and Y input combinations and the A and B inputs, note the output state for each of the input states. You can see that the circuit produces a binary 1 output any time a binary 1 is applied to either one or both of the inputs. By definition this is the logical OR function. As you can see then the OR function can be performed with a NAND gate by simply placing inverters ahead of each input.

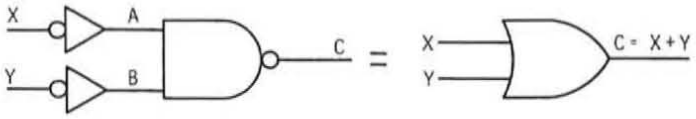


Figure 3-50
Performing the
OR function with a NAND gate.

By using inverters at the input of a NOR the AND function can be performed. Figure 3-51 shows the truth table for a NOR gate. The inputs are D and E and the output is F. Now assume that inverters are connected ahead of the NOR gate and the new inputs are labeled L and M as shown in Figure 3-52. The inverter or complementary input states would be as indicated in the truth table of Figure 3-51. If we interpret the logical function of the composite circuit where the inputs are L and M and the output is F then you can see by studying the truth table that the AND function is being performed. Note that the only time that the output F is a binary 1 is when both inputs L and M are at the binary 1 level. By definition this is the AND logical function. As Figure 3-52 indicates, a NOR gate with inverters at its input performs the AND function.

INVERTED INPUTS		NOR INPUTS		OUTPUT
L	M	D	E	F
1	1	0	0	1
1	0	0	1	0
0	1	1	0	0
0	0	1	1	0

Figure 3-51
Truth Table for NOR gate.

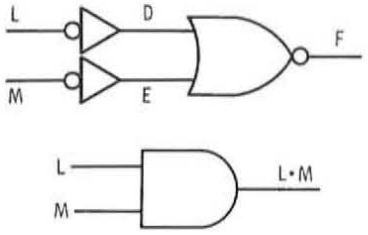


Figure 3-52 Using a NOR gate to perform the AND function.

As you can see any of the three basic logic functions can be performed with either a NAND gate or a NOR gate. For that reason entire digital circuits can be constructed with just one type of gate. The choice is arbitrary and strictly up to the designer. There are some cases where both NANDs and NORs are mixed within a circuit. As you will see later, some circuit economies result when NAND and NORs are combined. However, just remember that any logic function can be implemented with NAND gates or NOR gates alone.

Self Test Review

29. A NAND or NOR gate can perform any of the three basic logic functions AND, OR and NOT.
    a. True
    b. False
30. When inverters are used at the inputs to a NOR gate, the resulting circuit performs what logic function?
    a. AND
    b. OR
    c. NAND
    d. NOR
    e. NOT
31. When inverters are used at the input to a NAND gate, the circuit performs what logic function?
    a. AND
    b. OR
    c. NAND
    d. NOR
    e. NOT
32. A NOR or NAND can be used as a NOT circuit by
    a. inverting the output
    b. inverting the inputs
    c. connecting all inputs together
    d. cascading an even number of circuits.
33. Which circuit is preferred in implementing an entire circuit with one type of gate?
    a. NAND
    b. NOR
    c. Either

Answers

29. (a) True
30. (a) AND
31. (b) OR
32. (c) connecting all inputs together. By applying the same signal to all inputs of either a NAND or a NOR circuit it will perform the NOT or complement function.
33. (c) Either. NANDs or NORs can be used to implement a complete logic circuit. One type works as well as the other.

PRACTICAL LOGIC CIRCUITS

Now that you have completed this overview of the types of logic circuits in common use in digital equipment, let's take a look at several typical ways these logic elements are implemented. There are many different ways of electrically or mechanically obtaining the particular characteristics specified by the various types of logic elements. Here we will consider several popular ways of realizing digital logic elements with hardware.

Relays and Switches

The three basic logic functions — AND, OR and NOT — can be readily implemented with relay contacts and switches. For example, Figure 3-53 shows an AND gate made with relays. Here the normally open (N. O.) contacts of two relays labeled A and B are connected in series with a battery and a lamp. In this circuit, a closed relay contact and an ON lamp represent a binary 1. An open contact and an OFF lamp represent a binary 0. A zero voltage level represents binary 0 and a positive voltage level represents a binary 1 on the relay coil. You can see, for any of the four possible input combinations there is only one where the lamp will light. If either one or both of the relays are de-energized, their contacts will be open and current will not be supplied to the lamp. However, if voltage is applied to both relay coils, both contacts will be closed and a binary 1 (ON lamp) output will occur. Contacts A and B must be closed to light the lamp. Series connected switches usually perform the AND function.

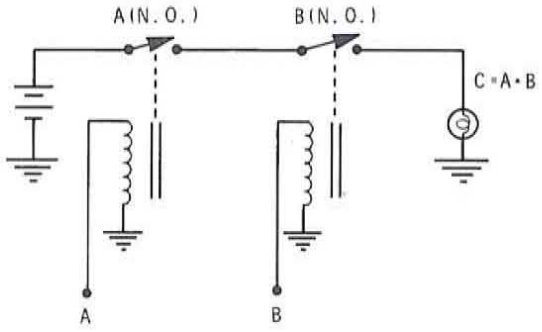


Figure 3-53 Relay AND gate.

Figure 3-54 shows an OR gate made with relays. The normally open relay contacts are connected in parallel. Here you can see that when a binary 1 voltage level is applied to either or both relay coils the D or E contacts will close, thereby supplying voltage to the lamp. An input to either relay D or E will close the circuit and turn on the lamp, representing a binary 1. Parallel connected contacts usually perform the OR operation.

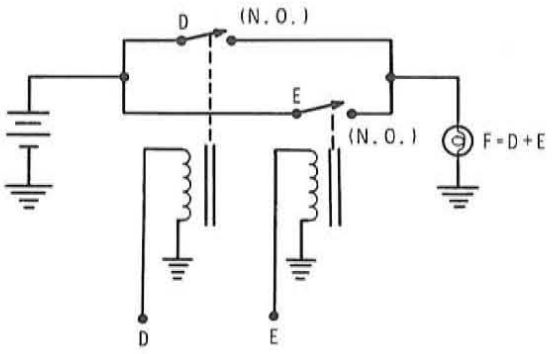


Figure 3-54 Relay OR gate.

A relay logic inverter circuit is shown in Figure 3-55. Here a relay with normally closed (N. C.) contacts is used. With a binary 0 (zero volts) applied to the relay coil, the relay is de-energized and the contact is closed representing a binary 1. This connects the battery to the lamp causing it to light. Therefore, with a binary 0 input the output is binary 1. Applying a binary 1 voltage level to the relay coil will energize the relay and open the contacts. This will cause the lamp to go off indicating a binary 0.

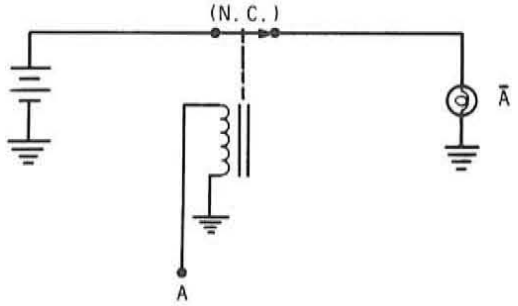


Figure 3-55 Relay inverter.

These relay switching circuits can be combined in many ways to form any logic function. In addition, manually operated switches can also be substituted for the relay contacts in some applications. Such relay or switch logic circuits are not often used today. Such circuits are large, slow in operation, and consume a significant amount of power. For most applications they are not practical. The very earliest of digital equipment including some computers were implemented with relays. However, many other different types of logic circuits are available now and these have many significant advantages over relays. There are still a few practical uses for relay and switch logic circuits. In some heavy industrial control systems where speed and power consumption is of little importance, relay logic circuits can handle high power applications and are very reliable. There are some applications where a mechanical means of operating the switches is available thereby making mechanical or manual switching logic necessary or desirable.

Discrete Component Logic Circuits

A discrete component logic circuit is a logic element made up of individual electronic components such as transistors, diodes, resistors, capacitors and other devices. These are assembled to form a complete circuit like the diode gates and inverter described earlier. For many years digital logic circuits were implemented with discrete components. They offered small sized, high performance and reasonable power consumption. However, today such discrete component circuits are rarely used. Like relay and mechanical switching logic circuits they have essentially been replaced by logic elements with greater performance, lower cost and improved features. You may still encounter discrete component logic circuits in some high power applications or in older digital equipment. Today however most digital logic functions are implemented with integrated circuits.

Integrated Circuits

An integrated circuit (IC) is a semiconductor device which combines transistors, diodes, resistors, and capacitors in ultra-miniature form on a single silicon chip. The advances in semiconductor technology have permitted the semiconductor manufacturers to design, develop and produce entire electronic circuits on a single silicon wafer that is generally less than one tenth of an inch square. These circuits are not only significantly smaller in size than discrete component logic circuits but also offer many other benefits as well. Because they can be mass produced, their cost is substantially less than discrete component circuits. Many offer significant savings in power consumption. Perhaps even more important is the elimination of the need for circuit wiring. When discrete components are used the components must be interconnected physically on a printed circuit board and then tested. With an integrated circuit the entire circuitry, all components included, are manufactured simultaneously. Manufacturing costs are reduced and reliability is improved.

Integrated circuits have been in existence for approximately 15 years. During this short time significant advances have been made. The complexity and sophistication of the circuits has increased significantly while the prices have continued to decline. Today with integrated circuit techniques it is not only possible to implement the basic logic elements, but also it is possible to fully integrate complete combinational and sequential circuits. Integrated circuits implementing the basic logic functions such as NAND, NOR, and flip-flops are known as small scale integrated circuits (SSI). Complete functional circuits of either the combinational or sequential type are generally designated as medium-scale

integrated circuits (MSI). However, today technology permits even greater flexibility. Complete circuits and systems can be constructed on a single chip. For example an entire digital computer is available as a single integrated circuit. Such circuits are known as large-scale integrated circuits (LSI). Today most digital equipment is implemented with integrated circuits. There are few applications where other forms of circuitry are necessary or desirable. This course emphasizes digital integrated circuits, their operation and application.

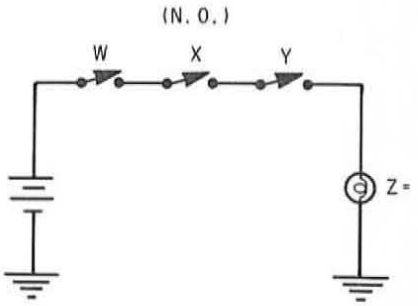


Figure 3-56 Circuit for Self Test Review Question 34.

Self Test Review

34. Write the logic equation of the relay logic circuit shown in Figure 3-56.
35. Write the logic equation of the relay logic circuit shown in Figure 3-57.
36. Draw a relay logic diagram for the function $J = L\bar{K}$.
37. Draw a relay logic circuit for the function $D = A \cdot B + \bar{C}$
38. Some relay and discrete component logic circuits are still used in some applications requiring
    a. high speed
    b. low cost
    c. small size
    d. high power
39. The basic logic functions NAND, NOR, etc.,in IC form are known as:
    a. SSI
    b. MSI
    c. LSI
    d. discrete

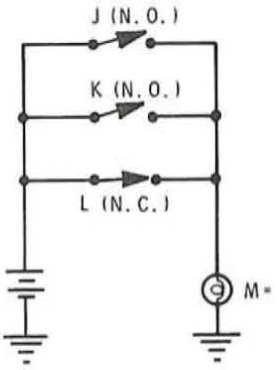


Figure 3-57 Circuit for Self Test Review Question 35.

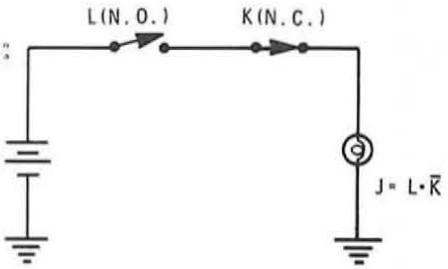


Figure 3-58 Answer to Question 36.

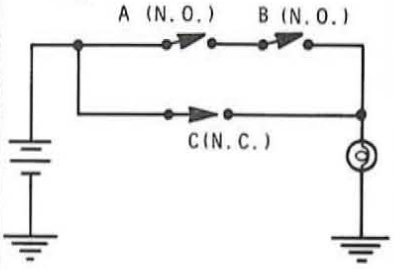


Figure 3-59 Answer to Self Test Review Question.

Answers

34. $Z = W \cdot X \cdot Y$
35. $M = J + K + \bar{L}$
36. See Figure 3-58.
37. See Figure 3-59.
38. (d) high power
39. (a) SSI small scale integration

EXPERIMENT 4

TRANSISTOR LOGIC GATE

OBJECTIVE: To demonstrate the operation and characteristics of a typical discrete component transistor logic gate.

Materials Needed

1 — MPSA20 transistor (417-801)
1 — 1K ohm ½-watt resistor
2 — 4.7K ohm ½-watt resistors
DC Voltmeter
Heathkit ET-3200 Digital Design Experimenter

Procedure

1. Construct the circuit shown in Figure 3-60. The inputs A and B will come from data switches SW1 and SW2. You will monitor the output on LED logic indicator L1.

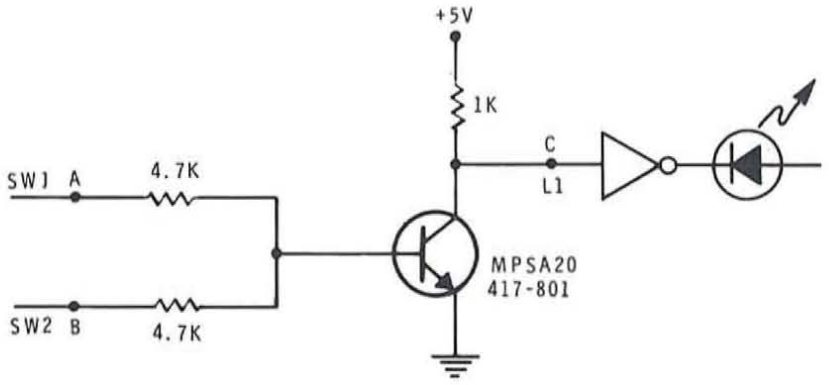


Figure 3-60

2. Apply the four input combinations given in Table 1 and measure the output voltage at C for each. Record your results in the C column in Table I.

TABLE I

A	B	C
0V	0V	on
0V	+5V	off
+5V	0V	off
+5V	+5V	off

3. Using positive logic level assignments convert the data in Table I into a truth table using binary 0s and 1s. Use Table II.

TABLE II

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

4. Study Table II and determine the logic function being performed.
   Logic function NOR

5. Using negative logic level assignments convert the voltages in Table I into binary 1s and 0s and complete Table III.

TABLE III

A	B	C
1	1	0
1	0	0
0	1	0
0	0	1

6. Study Table III and determine the logic function being performed.
   Logic function NAND

Discussion

The logic circuit in Figure 3-60 is called a resistor-transistor logic (RTL) gate. It is identical to a simple transistor inverter but with two input base resistors. A positive voltage level applied to either or both of the inputs will saturate the transistor and cause the output to go low. With both inputs near zero volts or ground, the transistor will be cut off and the output will be the supply voltage as seen through the collector resistor. This operation is completely defined by your truth table (Table I) and should appear as shown in Table IV below.

TABLE IV

A	B	C
0V	0V	+5V
0V	+5V	+.1V
+5V	0V	+.1V
+5V	+5V	+.1V

Using positive logic, your truth table (Table II) should be as indicated in Table V.

TABLE V

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

This defines the NOR function. The RTL gate acts as an OR gate followed by an inverter.

Using negative logic, your truth table (Table III) should appear as shown in Table VI.

TABLE VI

A	B	C
1	1	0
1	0	1
0	1	1
0	0	1

This is the NAND function. The gate performs the same function as an AND gate followed by an inverter for negative logic.

This circuit can be used to implement any of the basic logic functions by combining a number of gates. Additional base resistors can be added as more inputs are required. By paralleling inputs or using a single input, the circuit is nothing more than a simple inverter.

This type of logic gate was widely used in discrete component digital systems and a modified version of it is available in integrated circuit form.

EXAMINATION

UNIT 3

DIGITAL LOGIC CIRCUITS

The purpose of this exam is to help you review the key facts in this unit. The problems are designed to test your retention and understanding by making you apply what you have learned. This exam is not so much a test as it is another learning method. Be fair to yourself and work every problem first before checking the answers.

1. Logic gates are usually connected to form functional logic elements known as _____ circuits.
2. Draw the standard logic symbols for AND, OR, NAND, NOR gates and inverter.

3. Assuming logic levels of 0V and +5 V, analyze the operation of the logic circuit shown in Figure 3-61. Develop a voltage truth table for the circuit. Using both positive and negative logic level assignments, determine the logic function it performs. Use the tables in Figure 3-62.

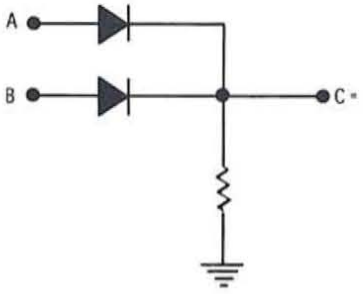


Figure 3-61
Circuit for Exam Question 3.

INPUTS		OUTPUT
A	B	C
0V	0V	
0V	+5V	
+5V	0V	
+5V	+5V	

VOLTAGE TABLE

INPUTS		OUTPUT
A	B	C

POSITIVE LOGIC

INPUTS		OUTPUT
A	B	C

NEGATIVE LOGIC

Figure 3-62 Truth Tables for analyzing the circuit in Figure 3-61.

Logic function:
Positive Logic _____
Negative Logic _____

4. Beside each logic equation below, write the logic function it describes.
   A. $G = N + \overline{\overline{M}}$ _____
   B. $H = J \cdot \overline{K} \cdot L$ _____
   C. $A = \overline{B}$ _____
   D. $Q = \overline{\overline{R} \cdot \overline{S}}$ _____
   E. $CLR = PB + RST$ _____

5. What logic function does the circuit in Figure 3-63 perform?

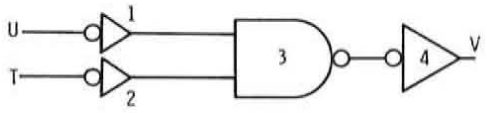


Figure 3-63
Logic circuit for Exam Question 5.

   A. AND
   B. OR
   C. NAND
   D. NOR

6. The ignition system of a car is set up so that the engine cannot be started unless the driver's front door is closed, the front seat belts are latched and the ignition key is on. What logic function is implied?
   A. AND
   B. OR
   C. NAND
   D. NOR
   E. NOT

7. Identify each truth table below with the logic function it represents. A and B are the inputs and C is the output in each case.

(A) A	B	C
0	1	1
1	0	1
1	1	1
0	0	0

_____

(B) A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

_____

(C) A	B	C
1	1	1
0	0	0
1	0	0
0	1	0

_____

(D) A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

_____

(E) A	C
0	1
1	0

_____

8. What logic function is being performed by the circuit in Figure 3-64?

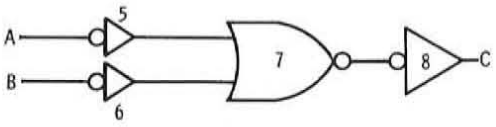


Figure 3-64
Logic circuit for Exam Question 8.

   A. AND
   B. OR
   C. NAND
   D. NOR

9. Analyze the operation of the diode gate circuit in Figure 3-65. Assume logic levels of 0V and −5V. Develop a voltage truth table and determine the logic function for both positive and negative logic level assignments. Use the tables in Figure 3-66.

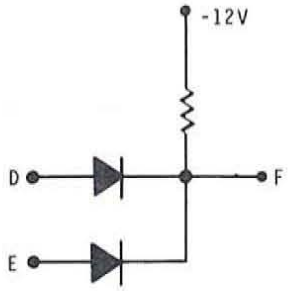


Figure 3-65
Logic circuit for Exam Problem 9.

INPUTS		OUTPUT
D	E	F
0V	0V	
0V	-5V	
-5V	0V	
-5V	-5V	

VOLTAGE TABLE

INPUTS		OUTPUT
D	E	F

POSITIVE LOGIC

INPUTS		OUTPUT
D	E	F

NEGATIVE LOGIC

Figure 3-66 Truth Tables
for the circuit in Figure 3-65.

Logic function:
Postive logic _____
Negative logic _____

10. A home intrusion alarm system is designed to sound a bell if any one of the following conditions occur: front or back doors open, any window opens, garage door opens. What logic function is implied?
    A. AND
    B. OR
    C. NAND
    D. NOR
    E. NOT
11. Write the logic equation of the relay logic circuit shown in Figure 3-67.

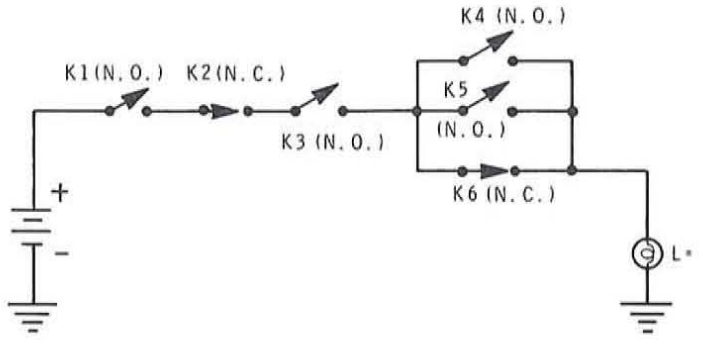


Figure 3-67
Circuit for Exam Question 11.

12. For the diode gate circuit in Figure 3-68, draw the logic diagram using standard symbols.

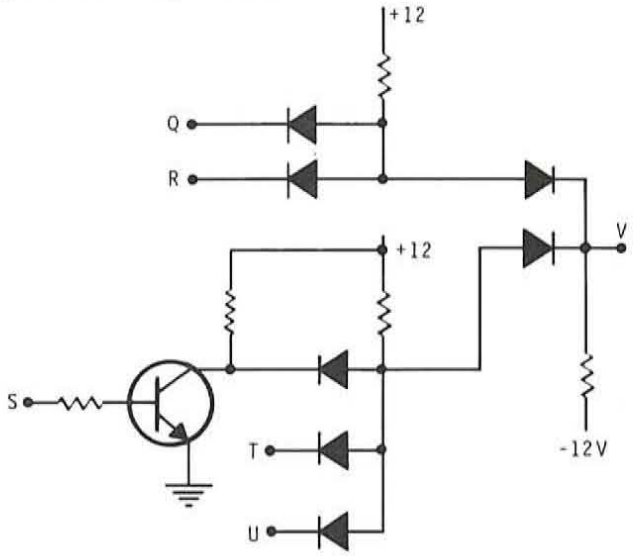


Figure 3-68
Circuit for Exam Question 12.

13. A logic circuit has 5 inputs. How many possible input combinations can it have?
    A. 2
    B. 4
    C. 5
    D. 16
    E. 32

14. Figure 3-69 shows the logic voltage levels applied to both an AND gate and an OR gate. Draw the output waveforms you would expect for each.

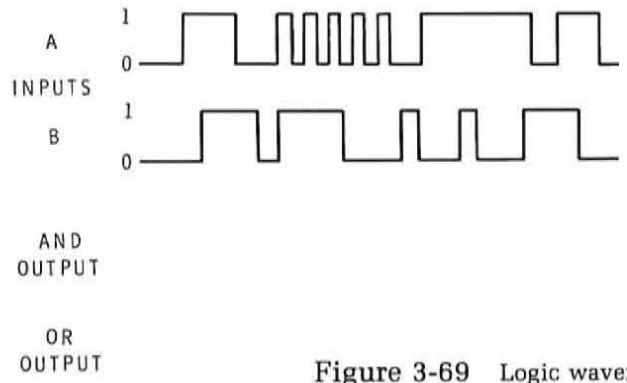


Figure 3-69 Logic waveform for AND and OR gates Exam Question 14.

ANSWERS

UNIT 3

DIGITAL LOGIC CIRCUITS

1. combinational
2. See Figure 3-70

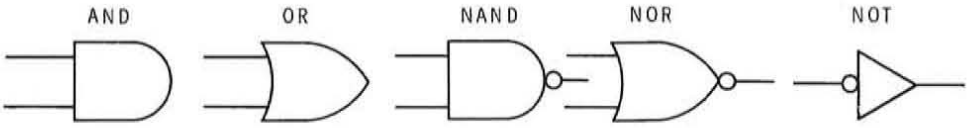


Figure 3-70
Answer to Exam Question 2.

3. In the logic gate of Figure 3-61, with both inputs at zero volts, both diodes will be cut off and the output will be zero. With one input at zero volts and the other at +5 volts, the diode associated with the +5 volt input will conduct. The other diode will be cut off. The output will be +5 volts less any diode drop. With both inputs at +5 volts, both diodes conduct and the output will be +5 volts. Your voltage truth table should be as shown in Figure 3-71A. The positive and negative logic truth tables are given in Figure 3-71 B and C. This circuit performs the positive OR negative AND function.

A	B	C
0V	0V	0V
0V	+5V	+5V
+5V	0V	+5V
+5V	+5V	+5V

VOLTAGE TABLE
A

A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

POSITIVE OR
B

A	B	C
1	1	1
1	0	0
0	1	0
0	0	0

NEGATIVE AND
C

Figure 3-71
Truth Tables for circuit
in Figure 3-61. Exam Question 3.

4. A. $G = \overline{N + \overline{M}}$ NOR
   B. $H = J \cdot \overline{K} \cdot L$ AND
   C. $A = \overline{B}$ NOT
   D. $Q = \overline{R \cdot S}$ NAND
   E. CLR = PB + RST OR
5. D. NOR NAND gate 3 and inverters 1 and 2 form an OR gate. Inverter 4 converts this to a NOR.
6. A. AND. The ignition cannot start the engine unless the driver's door is closed AND the seat belts are fastened AND the ignition key is on.
7. A. OR
   B. NOR
   C. AND
   D. NAND
   E. NOT

NOTE: The sequence of the inputs is irrelevant. The truth table should be analyzed in terms of the output it produces for the various input combinations.

8. C NAND NOR gate 7 and inverters 5 and 6 for an AND gate. Inverter 8 changes this to a NAND.
9. In the diode gate circuit of Figure 3-65, if both inputs are at zero volts, both diodes will conduct and the output will be 0 volts. If one input is 0 volts and the other −5 volts, the diode associated with the 0-volt input will conduct. The other diode will be reverse biased. The output will be 0 volts. If both inputs are −5 volts, both diodes will conduct and the output will be −5 volts. The voltage truth table is shown in Figure 3-72A. The positive and negative logic truth tables are shown in Figures 3-72B and C respectively. This circuit performs the positive OR/negative AND function.

D	E	F
0V	0V	0V
0V	-5V	0V
-5V	0V	0V
-5V	-5V	-5V

VOLTAGE TABLE
A

D	E	F
1	1	1
1	0	1
0	1	1
0	0	0

POSITIVE OR
B

D	E	F
0	0	0
0	1	0
1	0	0
1	1	1

NEGATIVE AND
C

Figure 3-72
Truth Tables for gate in Figure 3-65. Exam Question 9.

10. B OR The alarm horn will sound if the front door opens OR back door opens OR windows open OR garage door opens.
11. $L = K1 \cdot \overline{K2} \cdot K3 \cdot (K4 + K5 + \overline{K6})$
12. See Figure 3-73.

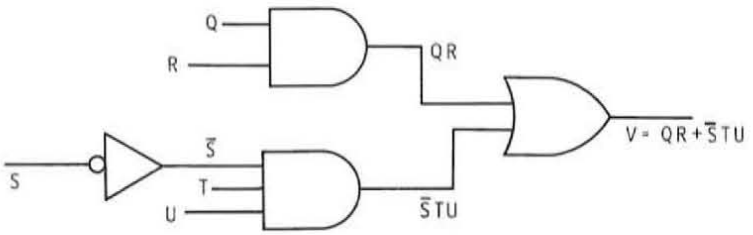


Figure 3-73
Solution to Exam Question 12.

13. E 32 With 5 inputs there can be $2^5 = 2 \times 2 \times 2 \times 2 \times 2 = 32$ possible input combinations.
14. See Figure 3-74.

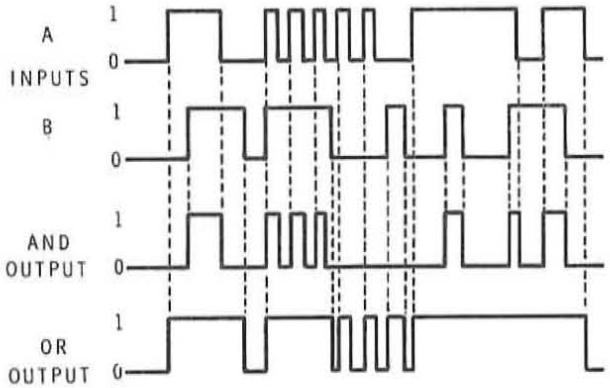


Figure 3-74
Solution to Exam Question 14.

The coordinates are referred to by the alpha coordinate first followed by the numeric coordinate, such as C7 which calls out the shaded coordinate of the illustration. When a drawing contains more than one sheet, the sheet number appears before the coordinates (2 C-7 indicates sheet 2).

6.2.2 Signal Levels

Throughout Data General Corporation documentation, a distinction is frequently made between electrical levels and logical values. To minimize confusion, electrical levels are always indicated by an "H" or "L", and logical values by a "1" or "0". As an electrical level, an "H" indicates that the signal is high (greater than +2.0 volts) and an "L" indicates that it is low (less than +0.7 volts). An asserted, or true, signal is indicated by a logical "1" and a false signal by a "0".

6.2.3 Signal Names

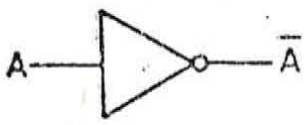
The voltage level at which a signal is said to be "asserted" ("true") is a matter of definition. To distinguish between signals that are asserted high (0=L, 1=H) and those that are asserted low (0=H, 1=L), a naming convention has been adopted in Data General's documentation which defines the relationship between the logical value and electrical level of a signal. If the signal name includes a horizontal bar over the name, as "$\overline{\text{WRITE}}$", then that signal is asserted true when it is at a low electrical level; conversely, a signal without the bar, "WRITE", is asserted true when high.

6.3 BASIC LOGIC GATES

Basic logic gates will be shown with its standard logic symbol and a truth table.

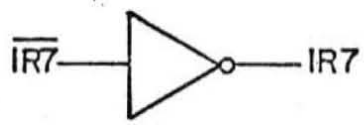
6.3.1 Inverters

Inverters are used to complement or negate an input signal.



Input A	Output $\overline{A}$
H(T) L(F)	L(T) H(F)

Now we will change the input and output to useful signal names to further explain logic conventions which you will be required to follow when using DGC logic drawings.



The above signal (IR7) identifies bit position 7 of the 16-bit Instruction Register.

Logic convention is as follows, when bit 7 of the IR contains a binary 1 bit, $\overline{IR7}$ is a "low" logic level and inverts to a "high" logic level identified as IR7. When bit 7 of the IR contains a binary 0 bit, $\overline{IR7}$ is a "high" logic level and IR7 is a "low" logic level.

Examples:

CPB10 contains a 1; then $\overline{CPB10}$ is low and CPB10 is high.

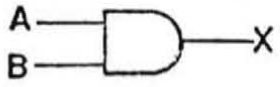
CPB10 contains a 0; then $\overline{CPB10}$ is high and CPB10 is low.

MEM10 = high when a 1 bit is contained on MEM10,
low with a 0 bit on MEM10.

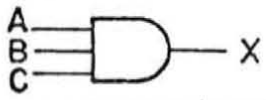
6.3.2 AND/NAND Gates

The "AND" gate is used when two or more signals must be present to produce an output signal. "NAND" gates are "AND" gates with an inverting output.

"AND" Gates



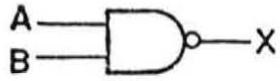
Inputs		Output
A	B	X
L	L	L
L	H	L
H	L	L
H	H	H



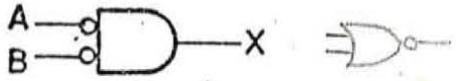
Inputs			Output
A	B	C	X
L	L	L	L
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	H

"NAND" Gates

neg logic



Inputs		Output
A	B	X
L	L	H
L	H	H
H	L	H
H	H	L

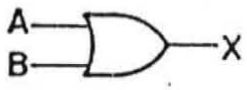


Inputs		Output
A	B	X
L	L	H
L	H	L
H	L	L
H	H	L

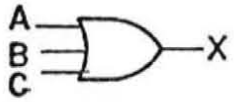
6.3.3 OR/NOR' Gates

The "OR" gate is used when any one signal being present produces an output signal. "NOR" gates are "OR" gates with an inverting output.

"OR" Gates



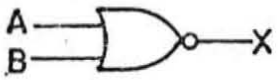
Inputs		Output
A	B	X
L	L	L
L	H	H
H	L	H
H	H	H



Inputs			Output
A	B	C	X
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	H

"NOR" Gates

neg logic.



Inputs		Output
A	B	X
L	L	H
L	H	L
H	L	L
H	H	L

Inputs		Output
A	B	X
L	L	H
L	H	H
H	L	H
H	H	L

6.3.4 "AND" "OR" Applications

Figure 6-1 illustrates how one type of gate can serve either as an "AND" or "OR" function by using two different applications.

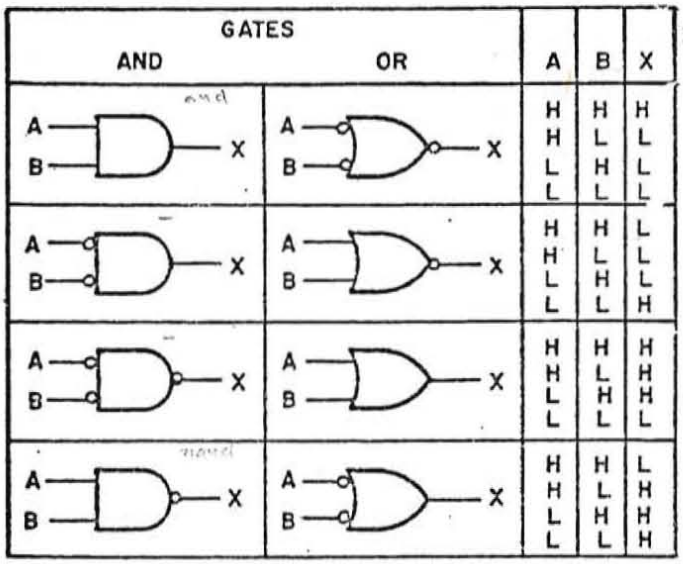


Figure 6-1. "AND" - "OR" Application Chart

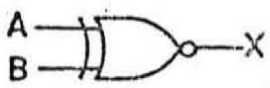
6.3.5 Exclusive-OR ("XOR")/Exclusive-NOR("XNOR") Gates

An "XOR" gate is used when only one of two inputs (one or the other but not both) must be present to produce an output. Exclusive-NOR gates are "XOR" gates with an inverting output.

"XOR" Gate

Inputs		Output
A	B	X
L	L	L
L	H	H
H	L	H
H	H	L

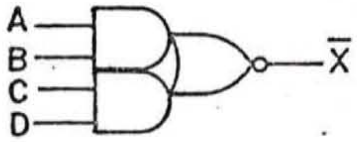
"XNOR" Gate



Inputs		Output
A	B	X
L	L	H
L	H	L
H	L	L
H	H	H

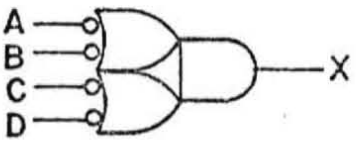
6.3.6 Multiple Input "AND-OR-INVERT" Gates

Integrated circuits are available which contain a multiple of input gates with an inverting output. The following two logic symbols illustrate the two different applications using one type of multiple input gate.



Output "$\overline{X}$" is low if both A and B are high, or if both C and D are high.
$\overline{X} = (A \cdot B) / (C \cdot D)$

• and
/ or



Output "X" is high if A or B and C or D is low.
$X = (A / B) \cdot (C / D)$

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UNIT 4

DIGITAL INTEGRATED CIRCUITS

CONTENTS

UNIT 4
DIGITAL INTEGRATED CIRCUITS

INTRODUCTION

All modern digital equipment is constructed with integrated circuits. A study of digital techniques, therefore, is a study of digital integrated circuits and their application. Because of integrated circuits, digital equipment can be analyzed and designed almost entirely at a conceptual logical or systems level as opposed to an electronics or circuits level. Digital integrated circuits are, in the true sense of the word, building blocks which are used to construct digital equipment. Previously, the designer of digital equipment had to design not only the logic involved but also the electronic circuits necessary to implement that logic. With integrated circuits, the designers job is primarily that of selecting commercially available devices and applying them to his specific application. No knowledge of electronic circuit design is necessary to the understanding and use of most digital techniques. However, by understanding the basic components and circuits used in modern digital integrated circuits your ability to work with and use them will be greater.

In this unit you will study the basic components and circuits used in the most common types of digital integrated circuits. The information in this unit will help you to analyze the operation of digital circuits and will help you to select a type of integrated circuit for a specific application. Look closely at the Unit Objectives that follow to determine the specific knowledge and skills you will have when you complete this unit. Then follow the steps in the Unit Activity Guide, recording the time you spent on each activity.

UNIT OBJECTIVES

When you complete Unit 4 on digital integrated circuits, you will have the knowledge and skills indicated below. You will be able to:

1. Name the two basic types of semiconductor switching elements used in digital circuits.
2. Define the four basic logic circuit characteristics of propagation delay, power dissipation, noise immunity and fan out.
3. Name and visually identify the three basic types of digital IC packages.
4. Name at least three distinct families of digital ICs and identify the three most popular and widely used types.
5. Explain the difference between current source and current sink types of logic circuits.
6. Describe the detailed operation and capabilities of TTL, ECL and CMOS integrated circuits given a schematic diagram of the circuit.
7. Select a type of digital IC to implement a given application for optimum performance and economy.

UNIT ACTIVITY GUIDE

	Completion Time
☐ Play Audio record 4, side 2: Digital Integrated Circuits	_____
☐ Read section "Logic Circuit Characteristics"	_____
☐ Answer Self Test Review Questions 1—6	_____
☐ Read Section "Integrated Circuits"	_____
☐ Answer Self Test Review Questions 7—12	_____
☐ Read section "Transistor Transistor Logic"	_____
☐ Answer Self Test Review Questions 13—20	_____
☐ Perform Experiment 5	_____
☐ Read section "Emitter Coupled Logic"	_____
☐ Answer Self Test Review Questions 21—25	_____
☐ Read section "Metal Oxide Semiconductor Integrated Circuits"	_____
☐ Answer Self Test Review Questions 26—31	_____
☐ Perform Experiment 6	_____
☐ Read section "Selecting a Digital Integrated Circuit for a Specific Application"	_____
☐ Answer Self Test Review Questions 32—34	_____
☐ Complete Unit Examination	_____

LOGIC CIRCUIT CHARACTERISTICS

There are many different types of digital integrated circuits available to implement digital equipment. Both saturated and unsaturated bipolar transistors as well as MOSFETs are used to implement a variety of logic circuits. Each type or family of digital integrated circuits has its own special capabilities and limitations. Their characteristics vary widely and the optimum circuit to use in a given application depends upon specific needs and requirements.

Some of the most important characteristics of digital integrated circuits are logic levels, propagation delay, power dissipation, noise immunity, and fan out. By understanding the meanings of these characteristics you can quickly compare, contrast and evaluate different IC logic families.

Logic Levels

Logic levels are the voltage values assigned to the binary 1 and binary 0 states for a given type of digital integrated circuit. Nominal values for the two levels are generally given, but in practice, the actual voltage levels may vary somewhat because of internal component tolerances, power supply variations, temperature and other factors. Generally, the manufacturer will list maximum and minimum acceptable voltage values for the binary 0 and binary 1 levels.

It is important to know the logic levels for a given type of integrated circuit so that when you are working with the equipment you can readily identify input and output logic states by measuring the logic levels with a voltmeter or an oscilloscope. A knowledge of the logic levels will permit you to analyze the operation of a circuit or determine whether it is functioning properly.

Propagation Delay

The propagation delay is a measure of the speed of operation of a logic circuit. Speed of operation is one of the most important characteristics of a digital circuit. For most digital applications high speed operation is beneficial.

Propagation delay is the amount of time that it takes the output of a digital circuit to respond to the input level change. It is the accumulation of all of the rise times, delay times and storage times associated with any logic circuit. When the input voltage changes from the binary 0 to binary 1 or from the binary 1 to binary 0 levels, the output of the logic circuit will respond at some finite time later.

Figure 4-1 illustrates propagation delay. Shown here is the input to a digital circuit and the corresponding output. The circuit could be an inverter, a NAND gate or a NOR gate. A binary 0 to binary 1 transition causes a binary 1 to binary 0 transition at the output. Note that the output transition occurs a specific time after the input transition. This is the propagation delay. The propagation delay (t_p) is generally measured between the 50 percent amplitude points on the corresponding leading and trailing edges of the input and output pulses. Note also that there are also two types of propagation delay, the propagation delay occurring when the output changes from high to low (t_{pHL}) and the propagation delay that occurs on the low to high output transition (t_{pLH}). Because of the characteristics of the logic circuit, the propagation delays for the two types of level changes are generally different. They are of the same order of magnitude and close in value but nevertheless unequal.

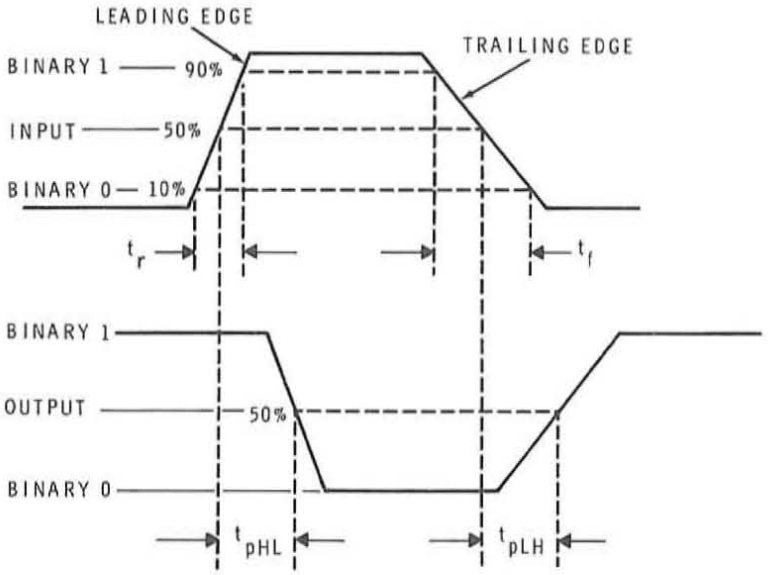

Figure 4-1
Propagation Delay.

The rise and fall times of the input and output pulses are another important consideration. The rise time (t_r) is the time it takes the pulse to rise from 10 percent to 90 percent of its maximum value. The fall time (t_f) is the time it takes for the pulse voltage to fall from 90 percent to 10 percent of its maximum value.

For most modern digital integrated circuits propagation delays are very short but finite. Propagation delays as low as one nanosecond are achievable. Some types of modern logic circuits have propagation delays as high as several hundred nanoseconds. Rise and fall times are usually less than the propagation delays. Because of manufacturing tolerances, circuit wiring and other factors, propagation delays can vary considerably from their nominal indicated value. In addition propagation delays are additive. When gates and other combinational logic circuits are cascaded, the propagation delays accumulate. If there is more than one level of logic, the total propagation delay from input to output is simply the sum of the individual gate propagation delays.

Power Dissipation

Another important characteristic of digital logic circuits is power dissipation. This is a measure of the amount of power consumed by the components in a typical logic gate or other circuit. Power dissipation, in milliwatts per logic gate, is an average value since the power consumption is usually different for the binary 1 and binary 0 output states.

The amount of power dissipated by a logic circuit is a very important consideration in the design of any digital equipment. A high power dissipation will mean high electrical energy consumption. Naturally, it is desirable to conserve as much electrical power as possible since the cost of operation of the equipment is an important consideration. This is particularly true of large scale digital systems such as computers.

The total power dissipation of the digital circuitry will also determine the size and cost of the power supply. In addition, high power dissipations mean high heat levels. In some instances special cooling requirements may be necessary to ensure proper operation of the equipment. Power dissipation is particularly important in portable or battery operated equipment. In order to reduce the cost of the battery and ensure long battery life, low power dissipation is desirable.

Gate power dissipation runs all the way from microwatts for certain types of MOS circuits to as high as 60 to 100 milliwatts per gate per certain types of high speed nonsaturated logic.

The Speed-Power Trade-Off

Two of the characteristics that we have considered so far, namely, speed and power dissipation are directly dependent upon one another in all types of digital logic circuits. The relationship between these two characteristics is such that speed is proportional to power dissipation. The faster a logic circuit switches the higher its power dissipation. In order to get high speed operation you must accept the penalty of high power dissipation. This trade-off or compromise between speed and power is one of the most important consideratons that a digital designer must make in a selection of a type of logic circuit for a given application. High speed digital logic circuits use nonsaturating bipolar transistors. Because the transistors do not saturate, their emitter-collector voltage drops are higher. Combine this with the very low circuit resistance values to minimize charge and discharge times of stray capacitances and the result is high power consumption.

MOS integrated circuits consume a very small amount of power. Their high impedance nature is partially responsible for this, however, this characteristic plus the built-in capacitances make for very slow switching speeds. The result is that the frequency of operation is severely limited. Nevertheless, the extremely low power consumption — on the order of nanowatts — makes MOS circuitry extremely desirable for portable and battery operation where high speed is not required. Other types of logic circuits fall between these two extremes. The speed-power trade off is an inherent compromise.

Noise Immunity

Noise immunity is a measure of the susceptibility of a logic circuit to noise pulses on the inputs and output of a logic circuit. Noise is considered to be any extraneous and undesired signal generated within the equipment itself or externally that is added to and appears superimposed upon the standard system logic levels. This noise can be a slowly varying dc level or very high frequency short duration voltage or current spikes. The noise may be either randomly occurring or repetitive. In any case the noise signals can cause the logic circuit to switch to an undesirable state at an improper time.

All digital logic circuits have built-in noise immunity. Because of the voltage thresholds associated with the components and the circuit, most logic circuits are capable of rejecting noise spikes of a relatively high amplitude. The noise immunity of most logic circuits is from approximately 10 to 50 percent of the supply voltage. This means that a noise spike occurring on a binary 0 or binary 1 level will be rejected if its amplitude is below a level that is 10 percent to 50 percent of the supply voltage. A circuit with a noise immunity of one volt, for example, would reject noise pulses that are one volt or less different from the nominal binary 0 or binary 1 logic levels. In some cases, noise is rejected by the logic circuit by virtue of its slow response. Some noise is high frequency in nature and noise pulses are of such short duration that the logic circuits cannot respond fast enough to cause a logic state change.

Noise immunity is an important consideration of digital logic circuits since most digital systems generate a substantial amount of noise during high speed switching. In addition, much digital equipment is used in noisy industrial environments where transients from the power line and other electrical equipment can cause false triggering of the logic circuitry. When selecting a particular digital integrated circuit for a logic application, noise immunity is an important consideration.

Fan Out

Fan out is a characteristic that indicates how much of a load can be connected to the output of a digital circuit. Fan out is generally expressed in terms of the number of standard size loads that a logic gate output can accommodate and still maintain proper operation at the nominal logic levels, speed, temperature range and other factors. Because of the component limitations and circuit configuration naturally there is a limit to the number of loads that can be connected to a logic circuit. A typical logic gate, for example, may have a fan out of ten, indicating that ten separate gate inputs can be attached to the output of this logic circuit and still maintain proper operation according to the manufacturer's specifications.

There are two basic ways that the output of a logic circuit is connected to the load. Some loads appear essentially between the output of the logic circuit and ground while others appear between the output of the logic circuit and the supply voltage.

Current Source Logic. When the loads appear between the output of the logic circuit and ground, the driving logic circuit functions as a current source. This type of logic is referred to as current sourcing logic. An illustration of this type of circuit configuration is shown in Figure 4-2A. Here the output of a logic circuit Q1 drives two similar logic circuits made up of Q2 and Q3. When transistor Q1 is on, the voltage at point X is near zero volts so no base drive is applied to Q2 and Q3, therefore they do not conduct. However, when Q1 cuts off, the supply voltage effectively furnishes current through collector resistor R_C to base resistors R_{B1} and R_{B2}. As you can see, each load consists of the emitter-base junction of a transistor and the appropriate base resistor connected between the output of the logic circuit (point X) and ground. As more of these loads are connected to the circuit, the total effective resistance of the load decreases and therefore causes increased current to be drawn from the supply through the collector resistor. The voltage divider formed by the collector resistance and the external loads causes the logic output voltage level to decrease as the number of loads increase. In order to maintain a specific minimum logic level at the collector of Q1, the number of loads must naturally be limited. In addition, the size of the supply voltage and collector resistor effectively limits the maximum amount of current that the driving logic circuit can supply to the transistor loads and still ensure that they all saturate. The maximum available current is $V_{CC} \div R_C$.

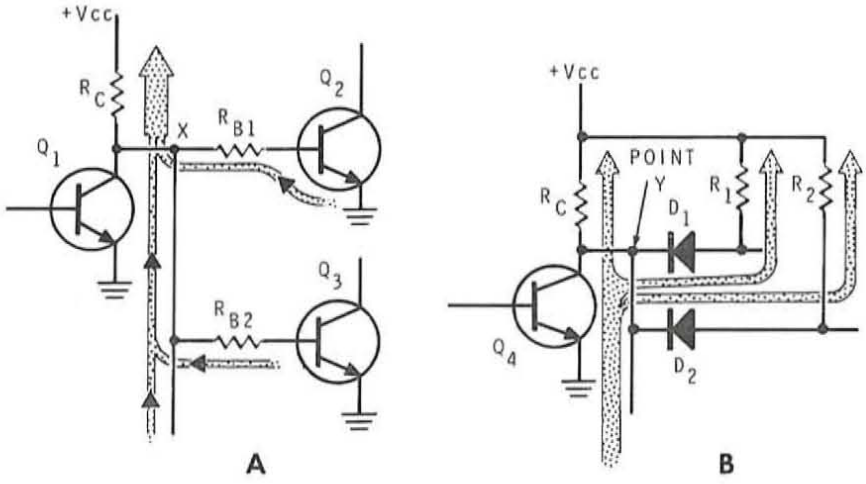

Figure 4-2 Examples of current sourcing (A) and current sinking (B) logic circuits.

Current Sink Logic. Another type of logic circuit, referred to as current sinking logic, is shown in Figure 4-2B. Here the loads appear effectively between the output of the logic gate (point Y) and the supply voltage. The logic circuit is shown driving two diode gates. When transistor Q4 is cut off its collector voltage is V_{CC}; therefore, diodes D1 and D2 are not forward biased so they draw no current. However, when transistor Q4 conducts, a current path is formed through Q4, the collector resistor R_C and through each diode gate load R_1-D_1 and R_2-D_2. The greater the number of loads connected, the higher the current that will pass through the driving or sink transistor Q_4. As more loads are added, the collector current of Q_4 increases, and the binary 0 output level increases. In order to maintain saturation and a reasonably low binary 0 level, the base drive to Q4 must be sufficiently high to handle the current of the external load as well as that determined by collector resistor R_C.

Self Test Review

1. The most important logic circuit characteristics are:
   a. _____
   b. _____
   c. _____
   d. _____
   e. _____
2. Typical propagation delay range for modern digital integrated circuits is
   a. 1 to 100 milliseconds
   b. 1 to 100 microseconds
   c. 1 to 100 nanoseconds
   d. 1 to 100 picoseconds
3. Decreasing the propagation delay of a logic circuit generally results in an increase in
   a. power dissipation
   b. fan out
   c. noise immunity
   d. package size
4. Increasing the number of loads on the output of a current source type logic circuit causes the binary 1 output level to
   a. increase
   b. decrease
   c. remain the same

5. Increasing the load on a current source type logic circuit causes more current to be drawn through the
   a. collector resistor
   b. output transistor
   and in current sinking logic increasing the number of loads causes more current to be drawn through the
   c. collector resistor
   d. output transistor
6. A logic circuit with a noise immunity of 40 percent is better in rejecting noise than one with 10 percent.
   a. True
   b. False

Answers

1. Logic levels, propagation delay, power dissipation, noise immunity and fan out.
2. (c) 1 to 100 nanosecond (1 nanosecond = 10^{-9} second)
3. (a) power dissipation
4. (b) decrease
5. (a) collector resistor
   (d) output transistor
6. (a) True

INTEGRATED CIRCUITS

Since all modern digital equipment is made up of integrated circuits you should be familiar with the various types. In this section you are going to learn how integrated circuits are classified and something about their physical characteristics. You will also learn of the most popular families of integrated circuits used in digital equipment today.

Integrated circuits are classified in three basic ways: by method of manufacturing, by application and by function. Let's briefly consider each of these types of classifications.

Manufacturing Methods

There are four basic ways of making integrated circuits. The most widely used method is called monolithic. Other types of manufacturing methods include thin film, thick film, and hybrid.

Monolithic. A monolithic integrated circuit is one that is constructed entirely on a single chip of silicon semiconductor material. Semiconductor materials are diffused into the basic substrate or base material to form the various junctions making up components such as diodes, transistors and resistors. The semi-conductor materials to be diffused into the substrate are in gaseous form and are deposited on the substrate through a series of masking operations under very high temperature. The result is that the entire circuit, all components and interconnections, are on a single base, thus the term monolithic. Most integrated circuits are constructed using this monolithic technique.

There are two basic forms of monolithic integrated circuits: bipolar and MOS. Here the difference is primarily that of the type of transistors used in constructing the circuits. Bipolar circuits which can be either saturating or non-saturating are by far the most widely used. But MOSFET circuitry is becoming more popular. The MOS circuitry is easier to make and takes up less space; therefore, much more circuitry can be placed on a silicon chip of a given size. The simplicity of the components also make the manufacturing yield much higher. The result is that MOS circuits can be constructed with higher density and at lower costs.

Thin and Thick Film Techniques. Thin and thick film integrated circuits are manufactured by depositing certain materials on a non-conducting base such as ceramic. Through a series of masking procedures, various resistive and conducting materials are deposited on the base or substrate to form resistors, capacitors, and inductors. Semiconductors are not usually manufactured in this way. Thin and thick film techniques are primarily used for manufacturing passive networks such as attenuators, filters, phase shift networks and the like. Because such networks can be made extremely small they offer the same advantages over discrete component circuits as do monolithic integrated circuits. Another advantage is that component tolerances can be closer than equivalent components made by monolithic techniques. For high quality precision circuits, thin and thick film techniques are preferred.

Hybrid Circuits. A hybrid integrated circuit is one made up of a combination of monolithic, thin film or thick film circuits. Any number of combinations are considered to be hybrid. A hybrid integrated circuit may consist of multiple monolithic chips interconnected in a single package. Another example of a hybrid is a monolithic circuit combined with a thin film or thick film passive network. Sometimes monolithic circuits and thin film or thick film circuits are also combined with individual semiconductor component chips to form a special high grade circuit for an unusual application.

Hybrids offer the advantage that a variety of different integrated circuits and components can be combined to offer special advantages not available in individual types of integrated circuits alone. For example, because of the ultra small size of a monolithic circuit, power dissipation is limited. In order to handle high power requirements it may be necessary to combine a low power monolithic circuit with a power transistor mounted on a separate chip but physically interconnected within the same package. High precision circuit requirements might be met by a combination of a monolithic circuit and a highly accurate thin film network. Because more than one type of technique is involved, and the complication of the interconnections that are necessary, hybrid circuits are more complex and expensive than other types. However they do offer the designer a wide range of capabilities while still maintaining the ultra small size and other benefits generally associated with integrated circuits.

Application

Another method of classifying integrated circuits is by their application. Primarily, this is a means of distinguishing between linear and digital circuits. Digital integrated circuits of course work with logic levels, pulses and binary data. Such switching circuits use either bipolar transistors of MOSFETs. Linear integrated circuits usually involve amplifiers of some kind and work with analog signals. They are constructed with bipolar transistors.

The chart in Figure 4-4 shows the basic integrated circuit hierarchy.

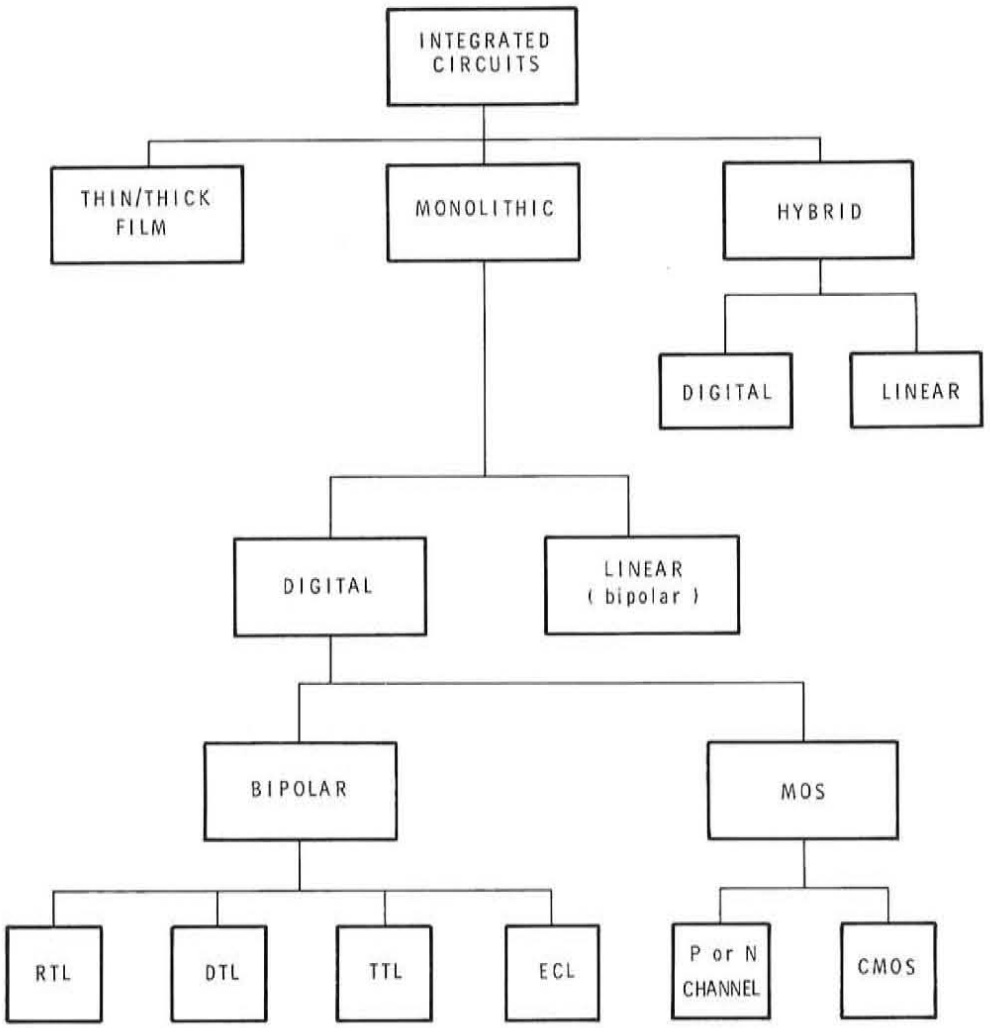

Figure 4-4 Hierarchy of integrated circuits.

Function

There are three basic classifications that identify the function of a digital integrated circuit. These are small scale integration (SSI), medium scale integration (MSI), and large scale integration (LSI).

SSI circuits are the simplest and most basic form of integrated circuits. These are amplifier or gate circuits that perform a single basic function. They must be interconnected externally in order to form complete functional or operational circuits. A typical SSI digital integrated circuit might consist of several multiple input gates or a flip-flop.

Medium scale integrated circuits are more complex. MSI circuits involve multiple gates which are interconnected to form a complete functional circuit. Most MSI circuits contain twelve or more equivalent gates or circuitry of similar complexity. An MSI circuit is usually a complete functional operating network such as a decoder, a counter or multiplexer. Such circuitry eliminates the need of having to interconnect individual gates in SSI packages to form the same function. MSI circuits greatly reduce the number of integrated circuits in a system and thereby reduce cost, assembly time, and in some cases, power consumption.

LSI circuits contain 100 or more equivalent gate circuits or networks of a similar complexity. LSI circuits are larger functional circuits or are the equivalent of multiple MSI circuits. An LSI circuit often forms a complete system or instrument. The major application of LSI circuits is in semiconductor memories which store binary data. However, there are many different types of complex LSI circuits including electronic calculators, computers and certain types of test instruments.

Integrated Circuit Packaging

A primary consideration to the integrated circuit user is the packaging and physical characteristics of integrated circuits. There are three basic methods of packaging the silicon chip. These are the TO5 can, the flat pack, and the dual in-line package. These three basic types of packages are illustrated in Figure 4-3.

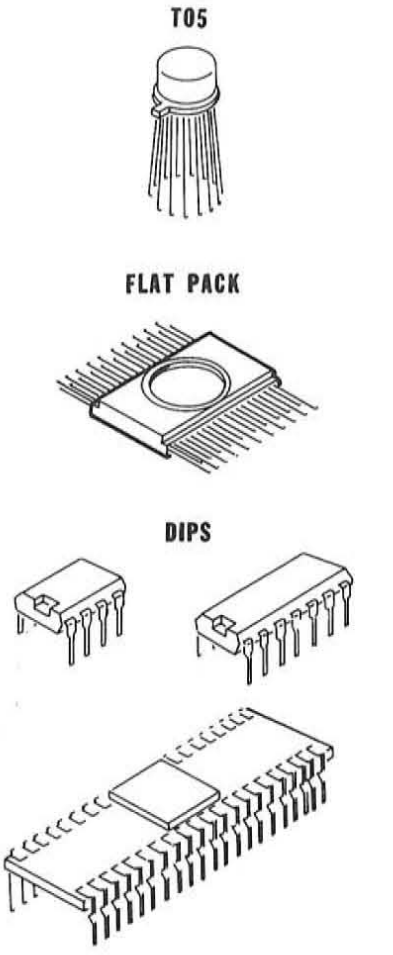

Figure 4-3 Illustrations of typical T05, flat pack and DIP ICs.

TO5. The earliest form of package used for integrated circuits was the TO5 can. This is a standard configuration for packaging transistors. This same package was modified by including additional leads. This type of package is still used with integrated circuits today but it is not the most popular form. Its advantage is that it can dissipate a substantial amount of heat. For that reason, this package is used mostly with linear integrated circuits.

Flat Pack. The flat pack was another type of housing used in the early development stages of integrated circuits. It is the smallest of all available integrated circuit packages and is designed for high density packaging. The packages are flat and are designed to be soldered or spot welded to a circuit board. Circuits can be placed close together and, therefore, a considerable amount of circuitry can be packaged in an extremely small area. Because of their ability to be packed so densely, these integrated circuits are generally made of a ceramic material that can withstand high temperatures. Closely packaged circuits cause heating and cooling problems. Therefore, the circuitry must be able to withstand such an environment. Flat pack circuits are used primarily in critical-size applications such as avionics, high reliability military systems and special industrial equipment.

DIP. The newest and most widely used form of integrated circuit packaging is the dual in-line package (DIP). It is slightly larger than the other types available but it offers many advantages. Such circuits are easy to mount and use. They are designed to be adaptable to machine insertion on printed circuit boards. They are available in various sizes, all the way from an 8-pin package (mini DIP) to a 40-pin package. Most SSI circuits are housed in 8, 14 or 16-pin dual in-line packages. MSI circuits are found in 14, 16 and 24-pin dual in-line packages. LSI circuits, because of their greater size complexity, require a greater number of input and output leads and, therefore, are usually housed in 24, 28 and 40-pin packages.

Several different types of dual in-line package materials are used. The most commonly used and least expensive is a plastic package. In this type of package, the integrated circuit chip is spot welded to a metal lead frame. The entire circuit is then encapsulated by an injection molded plastic technique.

For some critical integrated circuits, several types of ceramic packages are used. These are capable of withstanding higher temperatures and are generally hermetically sealed to provide an extra clean and safe environment for the circuit.

Temperature Ranges

Most integrated circuits are rated according to the range of temperatures over which they can operate satisfactorily. Most manufacturers generally specify both a military grade and a commercial or industrial grade circuit. The military grade circuits can be packaged in TO5 cans, ceramic flat packs, or ceramic dual in-line packages. These devices are capable of operating over a wide temperature range, usually from −55°C to +125°C. Circuits that perform properly over this wide temperature range are generally much more expensive. Such circuits are used only in high quality military equipment or in industrial equipment that is to be operated in severe environments.

For most general applications the commercial or industrial grade integrated circuits can be used. These are generally housed in plastic packages and are capable of operating over the 0°C to 70°C temperature range. Other temperature ranges are sometimes specified for different types of integrated circuits. Check the manufacturers data sheet for specific information on temperature ranges.

Self Test Review

7. Most digital ICs are
   a. Thin film.
   b. Thick film.
   c. Hybrid.
   d. Monolithic.
8. Transistors are not usually made by thin or thick film techniques.
   a. True
   b. False
9. A functional digital IC containing 50 gates is classified as
   a. SSI
   b. MSI
   c. LSI
10. The most popular IC package is the
    a. TO5 can
    b. flat pack
    c. DIP
11. The two types of DIP packaging materials are _____ and _____.
12. List the two temperature ranges of most digital ICs.
    Military _____
    Commercial/Industrial _____

Answers

7. (d) Monolithic
8. (a) True
9. (b) MSI
10. (c) DIP
11. Plastic, ceramic
12. Military: −55°C to +125°C
    Commercial/Industrial: 0°C to +70°C

TRANSISTOR TRANSISTOR LOGIC

There are many different types of integrated circuit logic elements used in implementing digital equipment. All of them perform the basic logic functions but have different characteristics, capabilities and limitations. Different types of digital logic circuits have been developed to meet special needs. Over the years a variety of circuits have emerged.

One of the biggest and most important design decisions made by an engineer designing digital equipment is in the selection of a type of digital logic circuit. In this section we are going to discuss the most popular form of bipolar integrated circuit logic elements, transistor transistor logic. Non-saturating bipolar circuits and MOS digital integrated circuits will be considered in following sections.

The most popular and most widely used type of digital IC is transistor-transistor logic (TTL or T^2L pronounced T square L). Its popularity is primarily the result of its extremely low cost and the availability of a wide variety of SSI logic elements and MSI functional circuits. Its ease of use, high performance characteristics and interfacing capability are other features that make it desirable. A number of special types of TTL circuits are available to match special needs. Even though TTL integrated circuits have been available for approximately ten years, this type of logic circuit continues to remain popular for use in new equipment designs. Its versatility has made it the standard logic circuitry used in modern digital equipment. Most of the experiments you will perform in this program use TTL integrated circuits.

Circuit Operation

Figure 4-5 shows the circuit of a typical TTL logic gate. It operates from a single +5-volt power supply and has typical logic levels of .4 volts for binary 0 (low) and 2.4 volts for a binary 1 (high). The circuit consists of three basic sections: a multiple emitter input transistor (Q1), a phase splitter transistor (Q2), and a totem-pole output circuit consisting of transistors Q3 and Q4. The multiple emitter-base junctions of transistor Q1, along with R1, form a diode gate. The primary advantage of this arrangement over individual diodes is that higher speed operation can be obtained.

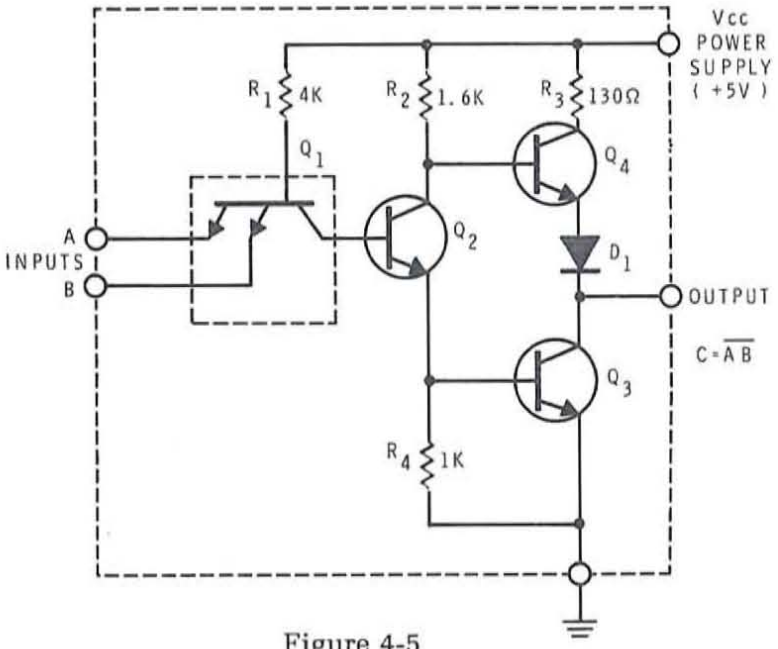

Figure 4-5
A typical transistor-transistor logic gate.

The phase splitter transistor (Q2) is a circuit that provides complementary drive signals for the two output transistors. The output circuit consists of transistors Q3 and Q4. These transistors are stacked one upon the other. Thus, this arrangement is given the name totem-pole. Transistor Q3 is simply a shunt transistor switch. Q4 in this circuit essentially serves as an active load resistor for Q3. In some logic circuits, the collector of the output transistor is returned through a collector resistor to the supply voltage. This collector resistor is known as a pull-up resistor because it causes the output to be pulled up to the supply voltage when the output transistor cuts off. In the TTL gate, Q4 serves as an active *pull-up* resistor. Current to any shunt load on the output is supplied by this transistor. This arrangement provides a much lower output impedance in the high

output state and therefore higher speed operation can be obtained. In logic circuits using a pull-up resistor, any shunt output capacitance must be charged through the collector pull-up resistor. This charging time can be long depending on the amount of shunt capacitance and the value of the collector resistor. With the active pull-up arrangement in the TTL gate, any output capacitance can be charged more quickly through the very low impedance represented by Q4.

To simplify the discussion of the TTL logic circuit it is convenient to show a diode equivalent of the key parts to this circuit. This diode equivalent arrangement is shown in Figure 4-6. Diodes D1 and D2 in this circuit represent the emitter-base input junctions of transistor Q1. Diode D3 represents the base-collector junction of transistor Q1. Diode D4 represents the emitter-base junction of Q2, and D5 is the emitter-base junction of Q3. Study the diode equivalent in Figure 4-6 and relate it to Figure 4-5. Keep in mind that a PN junction silicon diode requires approximately 0.7 volts across it before it conducts. The forward voltage drop across this diode is also approximately 0.7 volts. Since diodes D3, D4 and D5 are connected in series, the voltage at point X will be the sum of the individual voltage drops or in this case approximately $3 \times 0.7 = 2.1$ volts. A voltage less than 2.1 volts at point X will mean that all three diodes will be cut off.

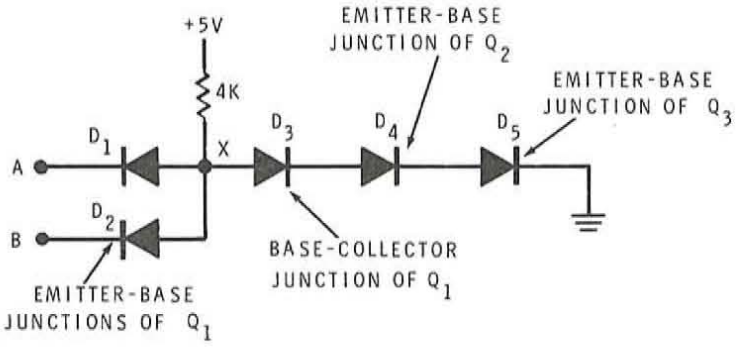

Figure 4-6 Diode equivalent circuit of TTL gate.

Now consider the operation of the circuit. If either one or both of the logic inputs are at their binary 0 level, 0.4 volts or less, the associated input emitter junction will conduct. The voltage at the base of Q1, (point X in Figure 4-6) will be the input logic level voltage plus the drop across the input emitter-base diode, in this case approximately $0.4 + 0.7 = 1.1$ volts. Current will flow through the input diode whose input is low and through the 4K pull-up resistor. Since the voltage at the base of Q1 (point X in Figure 4-6) is less than that required to cause the three diode string to conduct, the base-collector junction of Q1 will not conduct. The emitter-

INPUTS		OUTPUT
A	B	C
+.4V	+.4V	+3.6V
+.4V	+3.6V	+3.6V
+3.6V	+.4V	+3.6V
+3.6V	+3.6V	+.4V

A

INPUTS		OUTPUT
A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

B

INPUTS		OUTPUT
A	B	C
1	1	0
1	0	0
0	1	0
0	0	1

C

Figure 4-7 Truth tables for typical TTL logic gate (A) electrical, (B) positive logic NAND, (C) negative logic NOR.

base junctions of Q2 and Q3 will not conduct therefore these transistors will be cut off. With Q2 off, base current will be supplied to transistor Q4 through resistor R2. Q4 will conduct if an output load is connected to ground. The output voltage at this time will be the supply voltage $+V_{CC}$ less the drop across diode D1, Q4 and the 130 ohm collector resistor. A typical TTL binary 1 output voltage level is approximately +2.4 to +3.6 volts. A binary 0 voltage level at either or both of the inputs will produce a binary 1 output.

If a binary 1 logic level is applied to both inputs, the input diode junctions will be reverse-biased. A typical binary 1 logic level input will be +2.4 volts or higher. Most of the inputs will be driven from other TTL output circuits and therefore, the output voltage will in most practical situations approach +3.6 volts. With the emitter-base input diodes reverse-biased, the diode equivalent string D3, D4, and D5 in Figure 4-6 will conduct through the 4K resistor. This means that the emitter-base junctions of Q2 and Q3 will be forward-biased as well as the base-collector junction of Q1. With Q2 conducting, its collector voltage is lower than that required to turn Q4 on. Base current normally supplied to Q4 through R2 is shunted away by the conduction of Q2. With Q2 conducting Q3 will saturate. At this time the output voltage is the emitter-collector saturation voltage of Q3 which will be +0.4 volts or less. As you can see, with binary 1's on both inputs, the output will be binary 0. From this circuit description you can see that the circuit performs the NAND function for positive logic and the NOR function for negative logic. The truth tables in Figure 4-7 sum up the operation of the basic TTL gate while the basic characteristics are summarized in Table I.

Table I

TTL Characteristics

Type of logic: Current sinking
Propagation delay: 10 nanoseconds
Power dissipation: 10 milliwatts
Fan out: 10
Noise immunity: high
Logic levels: binary 0 = + .4 volts
binary 1 = +3.6 volts
Basic gate form: positive NAND/negative NOR
Supply Voltage V_{CC} +5 volts ±10 percent

TTL integrated circuits continue to be one of the most popular and widely used forms of logic elements. Many new equipment designs continue to use this type of circuit. Many manufacturers supply TTL circuits and new circuits are developed regularly. The wide range of SSI and MSI types make TTL circuitry perhaps the most versatile line of digital integrated circuits available. The most common type of TTL circuits are the 7400 series originally developed by Texas Instruments. Almost all other integrated circuit manufacturers second source this series of TTL circuits. Other TTL circuits are also available. These include the 9300 series made by Fairchild and the 8000 series manufactured by Signetics. All of these types of TTL circuits are compatible with one another. In this program you will use and demonstrate many different types of the 7400 series of TTL ICs.

Special TTL Variations

All TTL integrated circuits whether SSI or MSI, combinational or sequential use the basic TTL gate circuit shown in Figure 4-5. In addition there are several other versions of this TTL circuit made for special applications. These include gates for low power operation, higher speed operation or special logic functions.

Low Power TTL. Low power TTL circuits are similar to the basic TTL circuit described earlier. The only difference is that the resistor values in the circuit are approximately ten times higher meaning that the power consumption of the circuit is one tenth of that of the standard circuit. Low power TTL circuits are excellent for applications requiring a versatile high speed logic line with minimum power consumption. Increasing the values of the internal resistances, causes the propagation delay of the circuit to be increased. The propagation delay in a typical low power gate is approximately 30 to 40 nanoseconds. High speed is sacrificed for low power consumption.

High power TTL. The high power TTL circuit is basically the same as the standard circuit considered earlier. In this circuit resistor values are decreased significantly in order to improve operating speed. Typically, the gate propagation delay is reduced to approximately 6 nanoseconds. This increase in speed is accompanied by a power dissipation approximately twice that of a standard gate. This is approximately 22 milliwatts average power dissipation per gate. High power TTL circuits have for the most part been replaced by the newer Schottky TTL circuits which are not only faster but also consume less power.

Schottky TTL. The transistors in a TTL logic circuit operate in the saturation mode. To achieve higher speed operation than that obtainable with a standard or high power TTL gate, non-saturating transistors must be used. This is what is done to improve the speed of operation of Schottky TTL circuits.

The circuit of a Schottky TTL gate is basically the same as the standard TTL gate circuit we discussed earlier. The primary difference is that a diode is connected between the base and collector of each transistor in order to prevent those transistors from saturating. See Figure 4-8A.

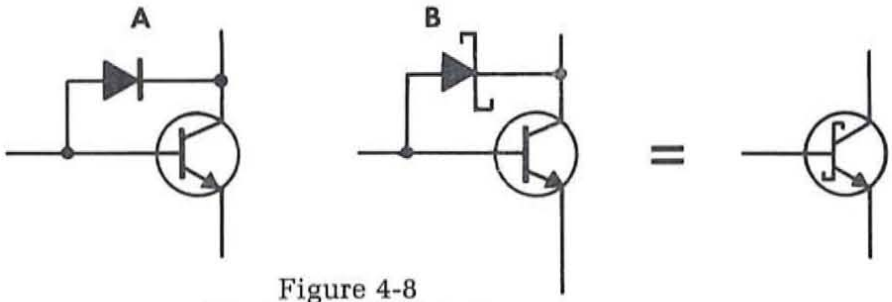

Figure 4-8
Hot carrier diode clamped transistors used in Schottky TTL circuits to prevent saturation and increase switching speed.

When the transistor begins to turn on, its collector voltage will drop quickly to some low value. When it drops beyond a certain point, the diode will conduct and shunt current away from the collector-base junction that would normally conduct during saturation. The diode effectively clamps the collector to a voltage sufficiently high to keep the base-collector junction reverse biased. This circuit permits the condition of saturation to be closely approached but still avoided.

The diode used to provide the clamping that prevents saturation is a hot carrier or Schottky diode. This type of diode, unlike other semiconductor diodes, is not a PN junction type. Instead a Schottky diode is the junction of a metal such as gold or aluminum and N-type semiconductor material. These diodes are not separate units. Instead they are part of the complex integrated circuit diffusion on the silicon chip. These diodes are high speed in operation because they do not have the normal charged storage normally associated with PN junction diodes. The forward voltage drop or voltage required for the diode to conduct is also much less than a standard PN junction.

The Schottky clamp diode as it is used on the transistors in a TTL gate is illustrated in Figure 4-8B. Note the special symbol used to represent the Schottky diode. The special symbol on the right in this figure is a Schottky diode clamped transistor. You will see this symbol used in schematic diagrams of Schottky TTL logic circuits.

The primary advantage of the Schottky TTL gate is its higher speed of operation. Since the transistors do not saturate, no charge storage problems occur. Gate propagation times as low as 3 nanoseconds are possible with this type of circuit. At the same time Schottky TTL gates achieve this rate of switching at a power dissipation of approximately 19 milliwatts, something less than the high power TTL circuit. A special low power Schottky TTL circuit with a propagation delay of 10 nanoseconds and a power dissipation of 2 milliwatts is also available. This form of TTL has one of the most favorable speed-power trade-offs of any digital integrated circuit.

Three State TTL. Three state TTL integrated circuits are a special version of TTL circuits whose output can assume three states instead of the normal two. Besides the binary 0 and binary 1 logic levels normally associated with a TTL gate output, the three state circuit has a third *open* state. This open state represents a very high impedance and is essentially equivalent to disconnecting the TTL totem pole output circuit from the output pin on the integrated circuit. This particular type of circuit is useful in digital systems using multiplexed or bussed data transmission.

A data bus is a group of wires, transmission lines or cables over which digital information or binary numbers are transferred in parallel from one point to another. There are basically two types of data busses, unidirectional and bi-directional. On a unidirectional bus, data is transferred in only one direction. On a bi-directional bus, data can move in either direction. Most digital busses are bi-directional in nature.

Instead of having multiple parallel paths for the transmission of digital data in two directions, a common bus is used and the information is transferred from one place to another on a time shared basis. While data from one particular source is being transferred, other data waits until the current transfer is complete. The concept of having one bus serve as a carrier for multiple signals is known as multiplexing. Circuits not currently in use are disabled while those sending and receiving data on the bus are activated.

Figure 4-9 shows a simplified diagram of a typical bi-directional digital data bus. Only one of several identical bus lines is shown. This bus line is generally responsible for transmitting one bit of data of a multiple bit binary word. The bus itself may be simply a cable several feet long or a transmission line several hundred feet long. Gates 1, 2, or 3 can transmit one bit of information down the bus line to be received by gate 8. Only one of the three gates will be enabled at a time to transmit the desired data. Note that the same bus can be used to transmit binary information from either gate 6 or gate 7 down the transmission line to be received by gates 4 or 5. Just keep in mind that only a single data transmission may take place at any given time but that it may be in either direction from any one of several sources or to several destinations.

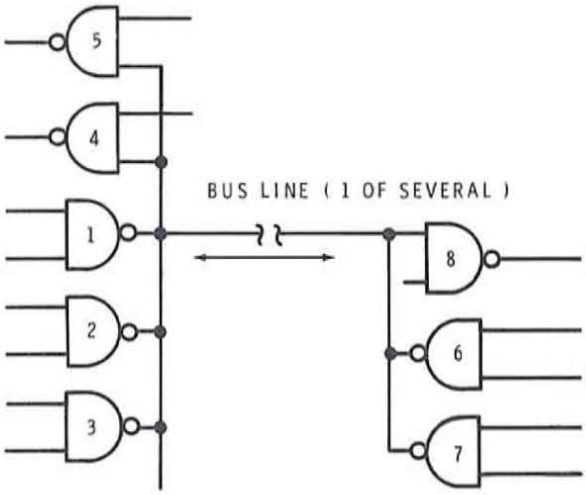

Figure 4-9
Bi-directional digital data bus.

The digital bus is relatively easy to implement with logic circuits using collector pull up resistors. The outputs of the gates from which the digital data comes are simply connected in parallel as illustrated in Figure 4-10. By connecting their outputs directly together, we effectively parallel the collector resistors, thereby reducing the total resistance to one half the value of an individual resistor. The two output transistors then share a common collector resistance. With this arrangement either transistor Q_1 or Q_2 can bring the output to the binary 0 condition. If Q_1 conducts and Q_2

is cut-off or if Q_2 conducts and Q_1 is cut-off, the output will be binary 0. The only time that the output will rise to $+V_{CC}$ is when both Q_1 and Q_2 are cut-off. The way digital data is transmitted by one gate then is to disable the gates not responsible for transmitting data. This is done by applying the appropriate input to the gate so that its output transistor is cut-off. This permits the other transistor to control the state of the output.

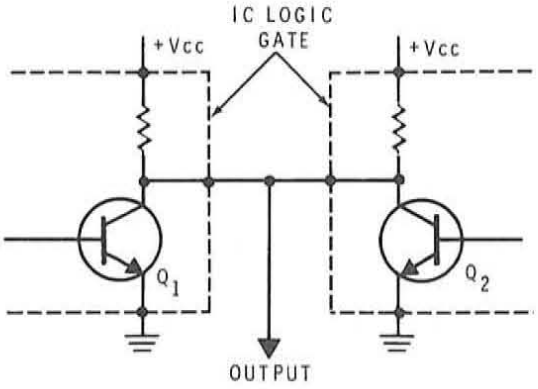

Figure 4-10
Paralleling gate outputs to share a common output line.

Parallel gate outputs form what is known as the wired OR connection. It is given this name simply because either transistor Q_1 OR Q_2 can bring the output to the binary 0 level. This connection is frequently used to implement the logical OR function without the need of an additional gate.

Because of the active pull-up circuit in the totem pole output of a TTL gate, TTL circuits cannot be wire ORed. Improper operation or damage can occur. For this reason TTL ICs cannot be used in bussing operations. To overcome this problem, open collector TTL circuits can be used. In these circuits, the active pull-up stage is eliminated and the collector of the shunt output transistor is made available at an output pin. To this is connected an external collector pull-up resistor. The wired-OR arrangement can then be used. However, because the active pull-up transistor is removed, one of the primary advantages of a TTL gate is eliminated. The active pull-up produces higher speed operation and lower output impedance, both of which are desirable not only from a speed stand point but from one of improving noise immunity.

The disadvantage of not being able to use TTL circuits in bus applications was overcome by the development of three state logic. This type of logic was originally introduced by National Semiconductor Corporation as Tri-State Logic. Three state logic is a special form of TTL that retains the basic TTL circuit configuration including the totem pole active pull-up output circuit. However, additional circuitry has been added to produce an optional high impedance third state that can effectively remove from any common bus line those circuits not transmitting data.

A typical three state TTL circuit is shown in Figure 4-11A. The circuit arrangement is basically identical to the TTL gate circuit we discussed earlier. Q_1 is the multiple emitter input transistor, Q_2 is the phase splitter while Q_4 and Q_5 form the totem pole output circuit. Transistor Q_3 has been added in order to provide better control of output transistor Q_4. Together, Q_3 and Q_4 form a compound or Darlington transistor with high gain. Components D_1, Q_6, Q_7 and Q_8 have been added to control the third state.

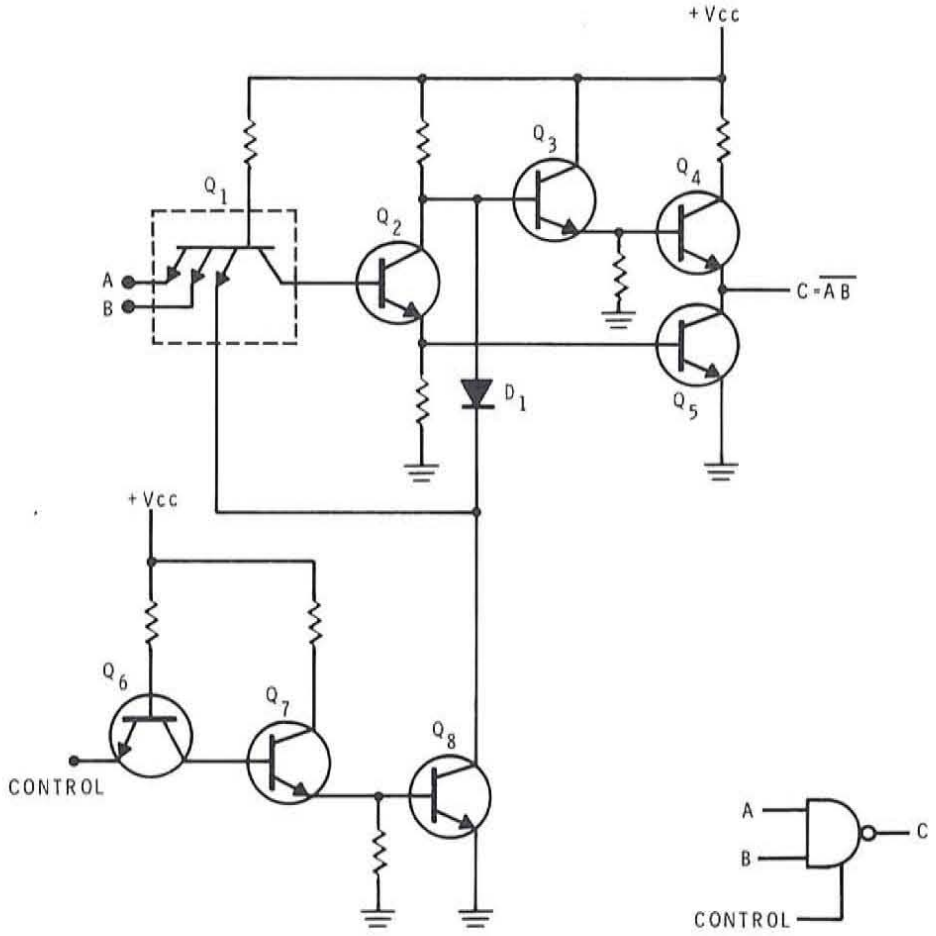

Figure 4-11
Three state TTL gate schematic (A) and the logic symbol (B).

A B

Whenever the control input is low, transistor Q_6 saturates. When it saturates it causes the collector of Q_6 and hence the base of Q_7 to be nearly the same low input value. This means that Q_7 and Q_8 are cut-off. The TTL gate then functions normally. Here the standard TTL output logic levels for binary 0 and binary 1 are achieved according to the input states.

When the control input is made a binary 1, Q_6 cuts off. The emitter-base junctions of Q_7 and Q_8 become forward biased through the base-collector junction of Q_6 and the associated base resistor. With Q_8 saturated, the third input to Q_1 is brought to ground along with the cathode of diode D_1. As you recall, when anyone or more of the inputs of a TTL gate are brought to a binary 0 level, the output is forced high. This is done by turning on the active pull-up transistor Q_4 and turning off the shunt output transistor Q_5. But in this case, both output transistors Q_4 and Q_5 are cut-off. When Q_8 saturates, the cathode end of D_1 is grounded. All the base current for Q_3 is shunted away. This causes Q_3 and Q_4 to cut off. With both output transistors Q_4 and Q_5 cut-off, the output is effectively an open circuit. Looking from the output of the gate back into the circuit, any load sees an extremely high impedance. Because of the high quality of the circuit and the low leakage, any load sees essentially an open circuit. With this arrangement, any number of three-state TTL outputs may be paralleled to form a common bus line. When data is to be transmitted, all of those gates not transmitting data will have their control lines at binary 1 so that their outputs represent an open circuit. Only the gate designated to transmit data will be enabled.

Figure 4-11B shows the logic symbol normally used to represent a three state TTL gate.

Self Test Review

13. A standard TTL gate performs what logic function for positive logic?
    a. AND
    b. OR
    c. NAND
    d. NOR
14. If all inputs of a TTL gate are binary 1, the output will be
    a. binary 0
    b. binary 1
    c. indeterminate
15. The typical TTL logic levels are
    binary 0 . _____ volts
    binary 1 . _____ volts
16. Two features that make the TTL gate faster than other types of gates are _____ and _____.
17. Schottky TTL is faster than standard TTL because
    a. smaller resistor values are used.
    b. it consumes more power.
    c. hot carrier diodes are faster than regular diodes.
    d. non-saturating transistors are used.
18. Three state TTL has three possible output states. These are _____, _____ and _____.
19. The two types of TTL that can be wire ORed are _____ and _____.
20. For TTL loads, a TTL circuit acts as a
    a. current source
    b. current sink.

Answers

13. (c) NAND
14. (a) binary 0.
15. binary 0 =+0.4 volts
    binary 1 = +3.6 volts
16. multiple emitter input transistor, totem pole or active output circuit.
17. (d) non-saturating transistors are used.
18. binary 0, binary 1, open
19. open collector, three state
20. (b) current sink for TTL loads.

EXPERIMENT 5

TTL LOGIC GATES

OBJECTIVE: To demonstrate the operation and characteristics of a TTL logic gate and to show how it can be used to perform any of the three basic logic functions.

Materials Required

1 — SN7400N (7400) quad-two input TTL integrated circuits (443-1)

1 — 1N4149 silicon diode (56 - 56)

1 — 560 ohm ½ watt resistor

Heathkit ET-3200 Digital Design Experimenter

DC Voltmeter

Procedure

1. Mount the 7400 TTL integrated circuit on the breadboarding socket. Be sure that it is seated firmly straddling the notch in the socket and that none of the pins are bent. Connect pin 14 to +5 volts and pin 7 to GND to supply power. Figure 4-12 shows the pin connections.

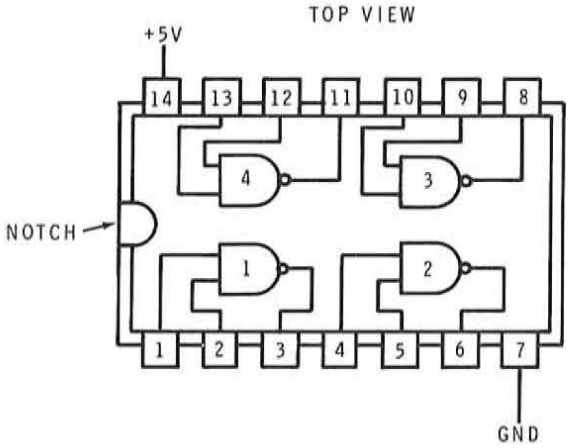

Figure 4-12
Pin connections for 7400 TTL IC.

2. Connect one of the four gates in the IC as shown in Figure 4-13. The input will come from data switch SW1. You will monitor the input and output states with the L1 and L2 LED indicators and your DC voltmeter.

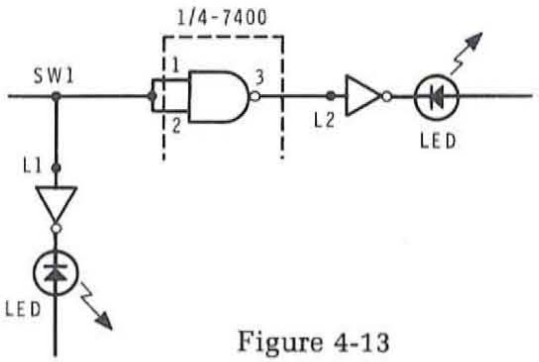

Figure 4-13

3. Set SW1 to the down position then the up position. Measure the DC input (pins 1 and 2) and output (pin 3) voltage for each position. Record your data in Table I. Also note the LED indicator input/output states.

Table I

INPUT	OUTPUT
0	3.8V
1	.1V

4. Assuming positive logic, the output logic levels are:
   binary 0 = .1V volts.
   binary 1 = 3.8V volts.
5. Study Table I. What logic function is being performed?
   Invert.
6. Connect the diode-resistor circuit shown in Figure 4-14 to the output of the TTL gate. This circuit simulates a load of about 5 TTL gate inputs. Again measure the input and output voltages of the circuit for both positions of SW1. Record your data in Table II.

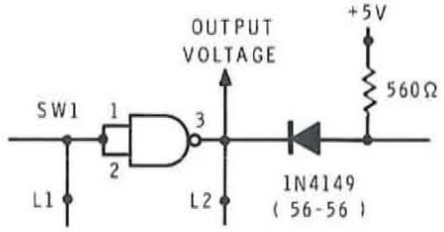

Figure 4-14

Table II

INPUT	OUTPUT
0	4.4V
1	0.15 V

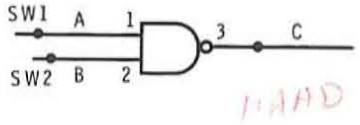

Figure 4-15

7. Compare the output data in Tables I and II and account for any differences. Does the loading affect the binary 0 or binary 1 output state most? 1.

8. Wire the circuit shown in Figure 4-15. Remove the 1N4149 and 560Ω resistor load used in the previous steps. The inputs come from SW1 and SW2. You will measure the output voltage C at pin 3 of the 7400 IC.

9. With SW1 and SW2, apply the input voltages given in Table III. Measure and record the output voltage for each set of inputs.

Table III

INPUTS		OUTPUT
A(SW1)	B(SW2)	C
OV	OV	3.8 V
OV	+5V	3.8
+5V	OV	3.8 V
+5V	+5V	.06

10. Using positive logic convert your electrical truth table in Table III into 1's and 0's in Table IV.

Table IV

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

11. Study Table IV. What logic function is being performed? Nand.

12. Using negative logic, convert the data in Table III into 1s and 0s and record in Table V.

Table V

A	B	C
1	1	0
1	0	1
0	1	1
0	0	1

13. Study Table V. What logic function is being performed? NOR.

14. Remove the wires connecting pins 1 and 2 of the IC to SW1 and SW2. Let the gate inputs hang free. Note the output state.

    With open inputs, the TTL gate output is _____ volts or binary _____ for positive logic. This means that an open input acts like a binary _____.

15. Wire the circuit shown in Figure 4-16. With SW1 (A) and SW2 (B), apply the states shown in Table VI. Record the state for each set of inputs. Observe LED indicators L1, L2, and L3 to obtain your input and output data. Use positive logic (binary 1 = on, binary 0 = off).

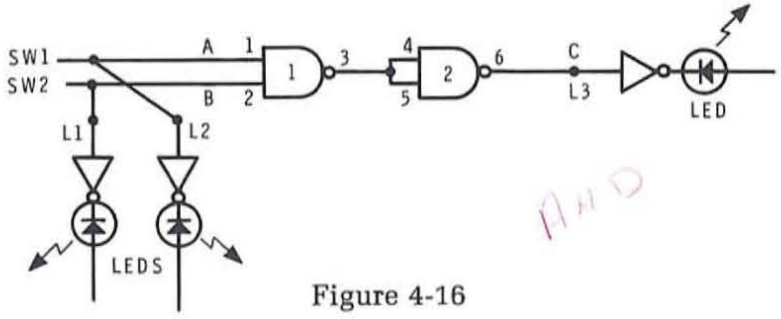

Figure 4-16

Table VI

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

16. Study the circuit in Figure 4-16 and the data in Table VI. What logic function is being performed? And.
17. Connect the circuit shown in Figure 4-17. Monitor the inputs and output on LED indicators L1, L2, and L3. With SW1 (A) and SW2 (B), apply the input shown in Table VII. Record the output state corresponding to each set of inputs. Use positive logic.

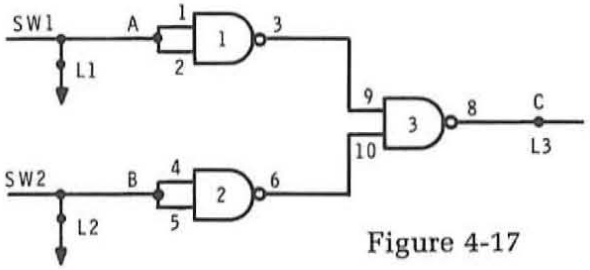

Figure 4-17

OR

Table VII

A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

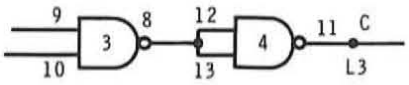

Figure 4-18

18. Study Figure 4-17 and Table VII. What logic function is being performed? OR.
19. Modify your circuit in Figure 4-17 by adding the fourth gate in the 7400 to the output as shown in Figure 4-18. Only the output change is shown. The rest of the circuit stays as in Figure 4-17.

NOR

20. Using SW1 (A) and SW2 (B) data switches and monitoring LED indicators L1, L2 and L3, apply the states shown in Table VIII. Record the output state for each set of inputs.

Table VIII

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

21. Study Table VIII. What logic function is being performed? NOR.

Discussion

In Steps 3 through 7 you demonstrated how one of the four gate circuits in the 7400 IC could be used as an inverter. The two inputs are tied together to form a single input line. With this arrangement, the gate performs as a TTL logic inverter where the input and output are complementary.

In Step 4 you measured the input and output voltages. The input from SW1 is 0 and +5 volts. The approximate output levels should have been binary 0 = +0.1 volts and binary 1 = +3.8 volts.

In Step 6 you loaded the TTL circuit with a current sinking type load then observed the output under load conditions. You should have found that with the load, the binary 0 output state was higher by about .1 volt than it was for no load. In the binary 0 output state, the shunt output transistor must sink the load current. The greater the sink current the higher the output voltage (V_{CE} sat). If the sink or load current is too high, the transistor will come out of saturation and the gate output voltage will be even higher. For this type of TTL gate, the maximum fan out is 10. Each gate input represents a sink current of 1.6 ma. Therefore each TTL gate output can sink 16 ma. If the load is greater, the output voltage in the binary 0 state may rise to more than .8 volts which is the maximum allowable level for a binary 0.

In Steps 9, 10 and 11 you demonstrated the basic logic function of the TTL gate. Using positive logic it performs the NAND function. In Steps 12 and 13 you should have found that the basic TTL gate performs the NOR function with negative logic.

In Step 14 you investigated the effect of open inputs. With both inputs open the output should have been binary 0, this indicates that open inputs act like binary 1 levels.

You demonstrated how TTL gates could be connected to perform the basic AND function in Steps 15 and 16. In Figure 4-16, gate 1 is a NAND while gate 2 is connected as an inverter to complement the NAND output to produce the AND output.

You connected TTL gates as an OR circuit and demonstrated its function in Steps 17 and 18. In Step 19 you added an inverter to the output of the OR to produce the positive NOR function. The AND and OR circuits are commonly used with the TTL gate. However, the NOR version is rarely used. A separate positive NOR TTL logic element is available (SN7402N) to eliminate the need to interconnect a 7400 as we did here.

EMITTER COUPLED LOGIC

The major switching speed limitation of bipolar logic circuits is the charge storage that occurs in the base region when both the emitter-base and base-collector junctions of a bipolar transistor are forward-biased to achieve saturation. The time required for this charge to be eliminated delays the turn-off of the transistor. Switching speeds can be greatly increased if this delay time is minimized or eliminated. In Schottky TTL circuits this storage problem is eliminated by preventing the transistors from saturating. This significantly increases the switching speed. Non-saturating transistor circuits offer the best potential for fast logic.

Another major form of logic circuits using non-saturating bipolar transistors is called emitter coupled logic (ECL). Also known as current mode logic, this circuitry is essentially a differential amplifier configuration which effectively prevents transistor saturation. ECL ICs are the highest speed logic circuits available today.

Circuit Operation

Figure 4-19 shows the schematic diagram of a typical ECL logic gate.

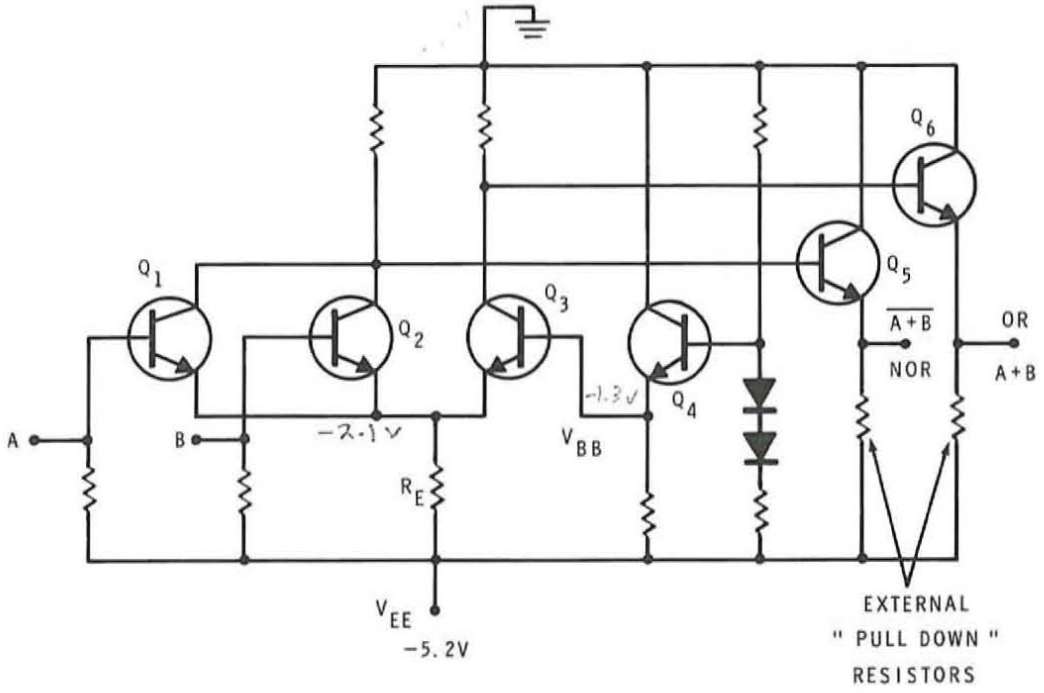

Figure 4-19 Typical emitter coupled logic gate.

Transistors Q_1 and Q_2 along with Q_3 form a differential amplifier. The inputs (A and B) are applied to transistors Q_1 and Q_2 whose emitter and collector connections are in parallel to form one side of the differential amplifier circuit. If additional inputs are required, more transistors are paralleled. Q_3 is the other side of the differential amplifier. Input logic levels are typically −1.75 volts (binary 0) and −.9 volts (binary 1). The output and input voltage swing is typically the difference between these two voltage levels or (1.75 − .9) = .85 volts. The supply voltage V_{EE} is −5.2 volts. The supply voltage V_{EE} and R_E form a current source that supplies a fixed current whose level is below the point that permits saturation.

In Figure 4-19, transistor Q_4 and the associated components form a temperature stabilized voltage source that biases the base of Q_3 to approximately −1.3 volts. The emitter of Q_3 will be approximately .8 volts more negative than its base because of its emitter base voltage drop. Therefore, the voltage at the emitters of Q_1, Q_2, and Q_3 will be approximately (−1.3 − .8) = −2.1 volts.

Assume that both logic inputs A and B are at the binary 0 logic level of −1.75 volts. With this condition transistors, Q_1 and Q_2 will not conduct because the emitter-base bias is insufficient. At this time the collectors of Q_1 and Q_2 are high while the collector of Q_3 is low. These two output levels are buffered by output emitter followers Q_5 and Q_6 and produce the proper binary 0 and binary 1 logic levels. Note that both the normal and complement outputs are available simultaneously.

If any one or both of these logic inputs rise to the binary 1 state (−.9 volts), the associated input transistor will conduct. The emitter of Q_1, Q_2, and Q_3 will then be one emitter-base junction drop more negative than the input voltage or approximately −1.7 volts. This means that when one or more of the inputs rises to the binary 1 level, the common emitter point will rise from −2.1 volts to −1.7 volts. This voltage will cause transistor Q_3 to cut-off. As you can see the current supplied by the emitter supply voltage and the common emitter resistor R_E switches from Q_3 to the conducting input transistor or transistors. With this arrangement the collectors of Q_1 and Q_2 will be low while the collector of Q_3 will be high. These logic output levels are buffered by the emitter followers Q_5 and Q_6. The circuit performs the OR and NOR functions for positive logic level assignments.

One of the major advantages of most commercial ECL IC logic circuits is the availability of both the normal and complement outputs simultaneously. This permits both OR and NOR functions to be obtained at the same time. No external inverters are required. Note that the emitter follower "pulldown" resistors are usually external to the integrated circuit itself. This permits the resistors to be located remotely at the end of a transmission line or in another desirable location depending upon the exact circuit configuration and application. It is also possible to tie together the OR or NOR outputs of ECL logic circuits to permit the wired OR function.

Circuit Characteristics

ECL logic circuits are extremely versatile, easy to use and produce high quality results. However, these circuits are normally higher in cost and of course consume significantly more power than other types of logic circuits. Their only real advantage is their high speed. Naturally, this high speed capability should be used only where absolutely necessary. Other types of logic are preferred for slower speed applications. The most widely used form of ECL is Motorola's MECL series.

Table II

ECL Characteristics
Type of logic: unsaturated, current sourcing
Propagation delay: 1—3 nanoseconds
Power Dissipation: 40—60 milliwatts
Fan Out: 10—25
Noise Immunity: High
Logic levels: binary 0 = −1.75 volts.
binary 1 = −.9 volts.
Basic gate form: OR/NOR
Supply voltage V_{EE}: −5.2 volts

Self Test Review

21. The basic ECL circuit is a(n)
    a. inverter
    b. differential amplifier
    c. saturated switch
    d. emitter follower
22. ECL gate outputs can be wire ORed.
    a. True
    b. False
23. For positive logic in an ECL gate
    binary 0 = _____ volts
    binary 1 = _____ volts
24. An ECL gate performs what functions in negative logic.
    a. AND
    b. OR
    c. NAND
    d. NOR
25. With ECL loads, ECL gates are
    a. current sources.
    b. current sinks.

Answers

21. (b) differential amplifier
22. (a) True
23. binary 0 = −1.75 volts
    binary 1 = −.9 volts
24. (a) AND
    (c) NAND
25. (a) current sources

METAL OXIDE SEMICONDUCTOR INTEGRATED CIRCUITS

Metal oxide semiconductor field effect transistors (MOSFETs) or insulated gate field effect transistors offer numerous advantages over bipolar transistors in digital circuits. First, these devices are simpler in construction and therefore can be made much smaller. Because they occupy less space, higher density logic networks can be placed on a given silicon chip. This permits large scale digital integrated circuits to be readily constructed. Another advantage of the MOSFET is its high impedance and therefore, low power consumption. MOS digital integrated circuits consume only a fraction of the power of equivalent bipolar circuits.

The big disadvantage of MOS digital integrated circuits is their lower speed. The high impedance and capacitive nature of these circuits produce switching speeds that are several orders of magnitude slower than bipolar digital integrated circuits. Despite their low speed nature, these circuits have nevertheless found wide application in those areas not requiring high speed operation. Recent technological advances in the manufacturing of MOSFET circuitry have also helped their switching speed approach that of some bipolar circuits.

There are two basic types of MOSFETs used in MOS digital ICs: the P-channel and the N-channel. As indicated earlier, the MOSFETs used in digital ICs operate in the enhancement mode. In this mode of operation, the transistor is normally cut-off. When the appropriate voltage level is applied between the source and the gate, the transistor suddenly switches on. These devices are near perfect switches in that they have an extremely high impedance when not conducting and an extremely low impedance when conducting.

The earliest MOS devices in use in digital circuits were PMOS circuits. P-type MOSFETs are the simplest and easiest to manufacture. N-channel MOS devices are more difficult to make, however, recent technological advances have simplified their construction. N-channel MOSFETs are smaller in size and switch at higher speeds. Their switching threshold is also much lower making them more compatable with bipolar digital integrated circuits. Another class of MOS logic circuits combines both P- and N-channel devices in a single circuit. These digital circuits are known as complementary MOS or CMOS.

MOS digital integrated circuits are clearly the digital ICs of the future. Their small size, low power consumption and simplicity make them attractive for many medium and large scale applications. Entire test instruments and computers can be made on a single silicon chip with MOS techniques. Improvements in manufacturing techniques will gradually reduce the switching speeds to levels acceptable to all but the most demanding high speed applications. It is expected that MOS ICs will eventually replace many of the various types of bipolar circuits.

PMOS and NMOS Circuits

When a digital IC circuit is constructed only with P-channel MOSFETs, it is known as PMOS. If the circuitry uses only N-channel enhancement mode MOSFETs, the circuits are referred to as NMOS. The basic circuit configurations are the same for either type of transistor.

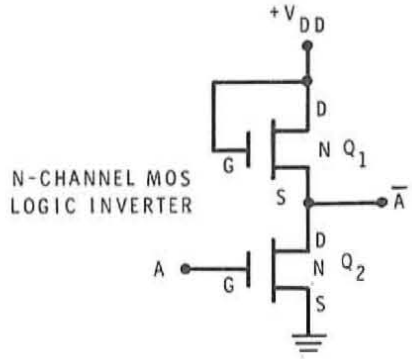

Figure 4-20
N-channel MOS logic inverter.

Figure 4-20 shows the circuit for an N-channel MOS logic inverter. Q_2 is the standard shunt inverter switch. Transistor Q_1 is connected to form a drain or load resistance. Another MOSFET (Q_1), biased into conduction, is substituted for a finite load resistor. A standard integrated resistance occupies substantially more space than the MOSFET and therefore, if used in any quantity, greatly reduces the amount of digital circuitry that can be placed on a given size silicon chip. The gate and drain of Q_1 are connected together which biases the transistor into conduction. It acts as a low resistance.

In operation, this circuit performs like any other inverter. When the logic input voltage is less than the gate-source threshold voltage, Q_2 is cut off. Since the gate and drain of Q_1 are connected together, Q_1 conducts and the output voltage is the supply voltage V_{DD} less the gate-source threshold voltage. When the input voltage exceeds the gate-source threshold of Q_2, Q_2 conducts. Its output voltage drops to a very low level. The on resistance of transistor Q_2 is made significantly less than the resistance of Q_1 by a ratio of at least 20 to 1.

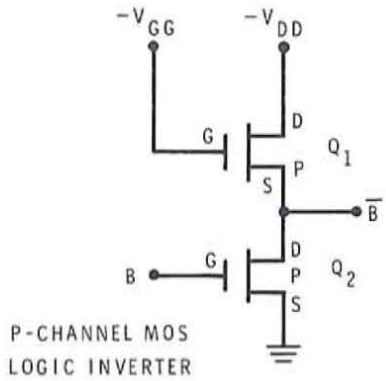

Figure 4-21
P-channel MOS logic inverter.

A logic inverter circuit using P-channel MOSFETs is shown in Figure 4-21. This circuit is similar to the N-channel inverter discussed earlier, however, a different means is used to bias the load transistor into conduction. In this circuit, the gate voltage is made more negative than the source voltage by the use of another power supply designated $-V_{GG}$. This voltage causes Q1 to conduct and act as a low value resistance. Q_2 in this circuit is the shunt inverter switch. Note the power supply polarity difference in this circuit due to the use of P-channel rather than N-channel transistors. The circuit operation is as described before. When

the gate-source threshold voltage is exceeded, transistor Q_2 will conduct and the output voltage will drop to a value near ground. When the gate-source voltage is less than the threshold value, Q_2 will cut off and act as an open circuit. At this time the output voltage is some negative voltage less than $-V_{DD}$. This particular circuit arrangement produces somewhat faster switching speeds than the circuit in Figure 4-20 but the disadvantage is that it requires the additional power supply.

Figure 4-22 shows how the various logic functions are implemented using the MOSFETs. In Figure 4-22A, two N-channel devices are connected in parallel and share a common load (Q_3). If either one or both of the input devices is biased on, the output voltage will drop to a low value. When the input voltages are both less than the threshold voltage, Q_1 and Q_2 will be cut off, allowing the output to rise toward $+V_{DD}$. With this arrangement, the circuit performs a NOR function for positive logic.

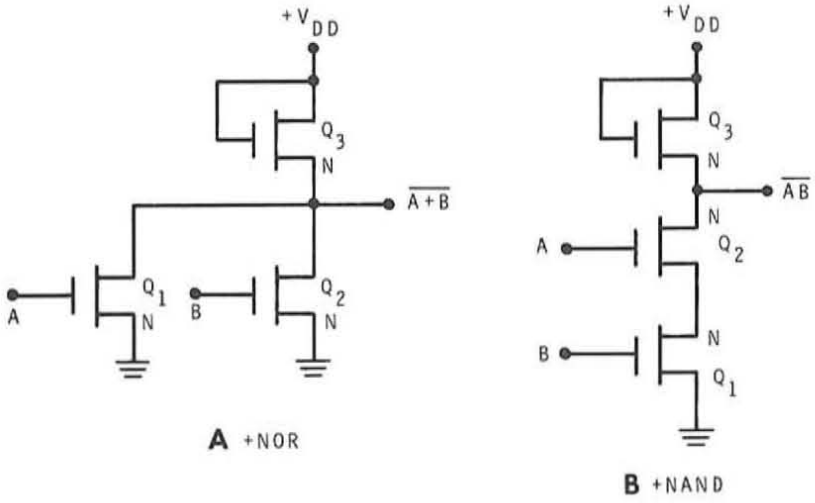

Figure 4-22
NMOS logic circuits.

The circuit in Figure 4-22B performs the NAND function for positive logic. Here transistors Q_1 and Q_2 are connected in series. In order for the output line to be brought low, input signals must appear high at both the A and B inputs simultaneously. If either one or both of the inputs are low, the output will be high. This is the NAND function.

The type of MOS logic circuits that we have discussed here are known as static logic circuits in that they perform logic functions with voltage levels. Another type of MOS logic is also widely used. Known as dynamic logic this circuitry has the same basic configuration as we have discussed here. However, the difference lies in that the circuits take advantage of the capacitive nature of the input to the MOS devices. Here the input capacitors are used to store charges or logic levels temporarily. During operation, high speed clock signals are used to transfer stored charges from one circuit to the next. The advantage of this type of MOS circuitry is still lower power consumption than the static circuits just discussed and higher operating speeds.

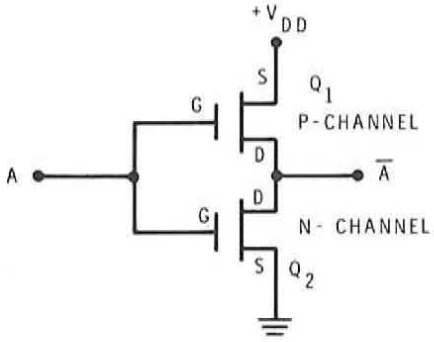

Figure 4-23
A complementary MOS logic inverter.

Complementary MOS

Complementary MOS or CMOS logic circuits use both P-channel and N-channel enhancement mode MOSFETs. A logic inverter constructed using both types of devices is shown in Figure 4-23. Here the input signal drives the gates of both devices simultaneously. When the input voltage is low or near ground, the gate-source threshold level for Q_2 is less than that required for conduction. Therefore Q_2 is cut off. However with the input low, the gate-source voltage threshold of Q_1 is exceeded. Since the gate is more negative than the source, this P-channel device conducts and connects the supply voltage V_{DD} to the output.

If the input voltage is brought to a high logic level, normally the same as the supply voltage $+V_{DD}$, the gate-source threshold voltage of Q_2 will be exceeded. Q_2 will conduct and act as a very low resistance bringing the output to a low level. At this time with the gate and source of Q_1 approximately at the same levels, the threshold is not exceeded, therefore, Q_1 is cut off. The logic inversion function is performed. It is interesting to note that in this circuit both the current sink and current source modes are used. When Q_2 conducts it sinks current from external loads connected between the outputs and the supply voltage. When Q_1 conducts it supplies current to any load connected between the output and ground. Because of the very low on resistance of a conducting device and the extremely high input impedance of other MOS devices, the logic levels are very nearly equal to ground and the supply voltage $+V_{DD}$.

Figure 4-24 shows a diagram of a typical CMOS logic gate. It consists of two P-channel devices Q_1 and Q_2 connected in series and two N-channel devices Q_3 and Q_4 connected in parellel. When either one or both of the inputs go high to the positive binary 1 voltage level, the associated N-channel transistor Q_3 or Q_4 will conduct. This will cause the output to drop to a voltage level near zero volts indicating a binary 0 output. With either input high, either Q_1 or Q_2 will be cut-off. Since Q_1 and Q_2 are in series, the path between the supply voltage $+V_{DD}$ and the output is not completed unless both Q_1 and Q_2 conduct.

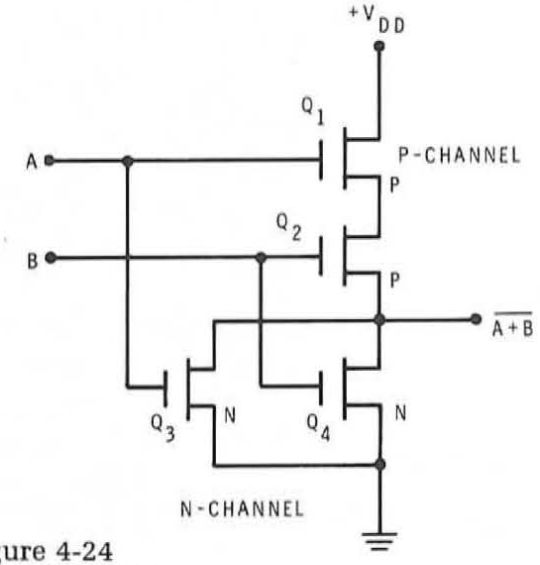

Figure 4-24
CMOS NOR logic gate.

When both inputs go low, Q_3 and Q_4 will become cut-off because their gate-source voltage is below the threshold level necessary to cause conduction. At this time the gate-source voltages of Q_1 and Q_2 will be approximately equal to $+V_{DD}$. Both devices conduct and form a low resistance path between the output and the supply voltage.

Summarizing the operation of this CMOS logic gate, you can see that the NOR logic function is being performed with positive logic. Any logic function including NAND, AND and OR can be performed by suitably arranging the P- and N-channel devices in the circuit.

If a digital designer were to specify the perfect logic circuit for all applications, this logic circuit would have characteristics very similar to those of CMOS. CMOS logic circuits offer a balanced combination of characteristics making it highly versatile and desirable. This type of logic circuit features very low power dissipation, excellent noise immunity, wide power supply voltage variations, high fan out and moderately high speed of operation.

Low power dissipation in CMOS circuits is achieved because there is never a continuous path through any of the devices in the circuit from the supply voltage to ground. A look at the inverter circuit in Figure 4-23 or the NOR gate in Figure 4-24 will indicate this. When the N-channel devices connected between the output and ground are conducting, the P-channel devices between the output and $+V_{DD}$ are cut off. Similarly, when the P-channel device between the supply voltage and the output is on, the N-channel devices from the output to ground are cut off. The current flow that does take place between the supply voltage and ground is that which flows when the output state switches. It is during this time that the P- and N-channel devices may be on together momentarily thereby causing a small current to flow. If the switching rate is high, the rate of occurrance of this current flow increases. The power consumption of a CMOS device increases with its operating frequency because of this effect.

Table III

CMOS Characteristics

Type of logic:	Current sinking and current sourcing.
Propagation delay:	30—100 nanoseconds.
Power Dissipation:	.01 milliwatt (static) 1 milliwatt at 1 MHz
Fan out:	50 +
Noise immunity:	very high (45 percent V_{DD})
Logic levels:	binary 0 = 0 volts binary 1 = $+V_{DD}$
Basic gate form:	positive NOR/negative NAND
Supply voltage V_{DD}:	+3 to +15 volts

The most popular forms of CMOS logic are the 4000 series circuits made by RCA and the 74C series made by National Semiconductor. Both offer a variety of SSI, MSI and LSI circuits.

Self Test Review

26. P-channel MOS is faster than N-channel MOS.
    a. True
    b. False
27. MOS combining both P- and N-channel in series is called _____.
28. The primary disadvantage of MOS ICs is _____.
29. The CMOS logic levels are
    binary 0 = _____ volts
    binary 1 = _____ volts
30. Most MOS ICs are usually
    a. SSI
    b. MSI
    c. LSI
31. The input to a CMOS gate appears primarily as a
    a. low resistance
    b. high resistance
    c. capacitor
    d. inductor

Answers

26. (b) False
27. CMOS
28. low speed
29. binary 0 = zero volts
    binary 1 = $+V_{DD}$
30. (c) LSI
31. (c) capacitor

EXPERIMENT 6

CMOS LOGIC GATES

OBJECTIVE: To demonstrate the operation and characteristics of a CMOS logic gate and to show how it can be used to perform any of the three basic logic functions.

Materials Required

1 — CD4001AE (4001) quad two input CMOS integrated circuit (443-695)

Heathkit ET-3200 Digital Design Experimenter

DC Voltmeter

Procedure

1. Mount the 4001 CMOS integrated circuit on the breadboarding socket. Be sure that it is seated firmly straddling the notch in the socket and that none of the pins are bent. Connect pin 14 to +5 volts and pin 7 to GND to supply power. Figure 4-25 shows the pin connections.

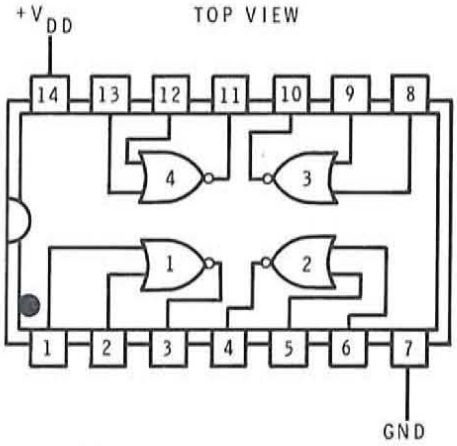

Figure 4-25 Pin connections for 4001 CMOS IC.

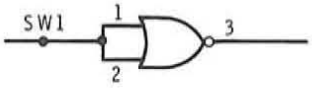

Figure 4-26

2. Connect one of the four gates in the IC as shown in Figure 4-26. The input will come from data switch SW1. You will measure the input and the output states with your DC voltmeter.

3. Set SW1 first to the down position then the up position. Measure the DC input (pins 1 and 2) and output voltage (pin 3) for each position. Record your data in Table I.

Table I

INPUT	OUTPUT
Ø V	5 V
5 V	Ø V

4. Assuming positive logic, the output logic levels are:
   binary 0 = Ø volts.
   binary 1 = 5 volts.
5. Study Table I. What logic function is being performed? INV. (Not)
6. Wire the circuit shown in Figure 4-27. The inputs come from SW1 and SW2. You will measure the output voltage C at pin 3 of the 4001 IC.

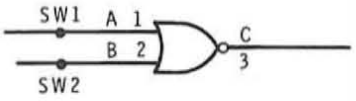

Figure 4-27

7. With SW1 and SW2, apply the input voltages given in Table II. Measure and record the output voltage for each set of inputs.

Table II

INPUTS		OUTPUT
A (SW1)	B (SW2)	C
OV	OV	5
OV	+5V	0
+5V	OV	0
+5V	+5V	0

8. Using positive logic, convert your electrical truth table in Table II into 1s and 0s in Table III.

Table III

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

9. Study Table III. What logic function is being performed? Nor.

10. Using Negative logic, convert the data in Table II into 1's and 0's and record in Table IV.

Table IV

A	B	C
1	1	0
1	0	1
0	1	1
0	0	1

11. Study Table IV. What logic function is being performed? _____.

12. Remove the wire connecting pins 1 and 2 of the IC to SW1 and SW2. Let the gate inputs hang free. Measure the output voltage.

With open inputs, the CMOS gate output is ∅ volts or binary 0 for positive logic. This means that an open input acts like a binary 1.

13. Wire the circuit shown in Figure 4-28. With SW1 (A) and SW2 (B), apply the input states shown in Table V. Record the output state for each set of inputs. Observe LED indicators L1, L2, and L3 to obtain your input and output data. Use positive logic (binary 1 = on, binary 0 = off).

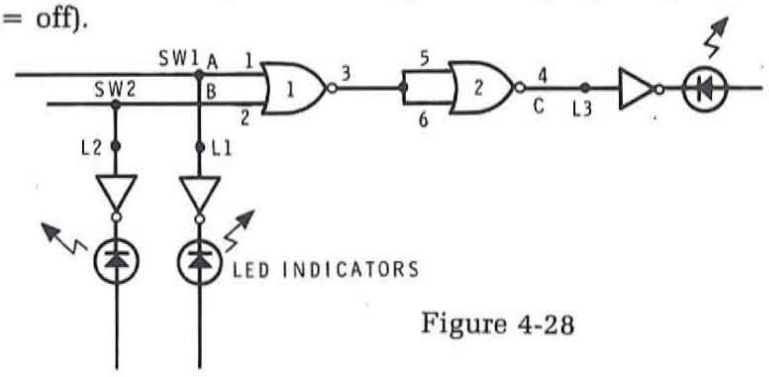

Figure 4-28

Table V

A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

14. Study the circuit in Figure 4-28 and the data in Table V. What logic function is being performed? OR.
15. Connect the circuit shown in Figure 4-29. Monitor the inputs and output on LED indicators L1, L2, and L3. With SW1 (A) and SW2 (B), apply the inputs shown in Table VI. Record the output state (C) corresponding to each set of inputs. Use positive logic.

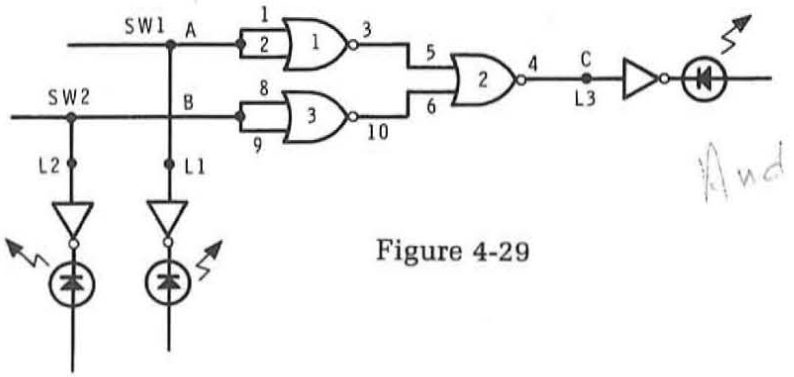

Figure 4-29

Table VI

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

16. Study Figure 4-29 and Table VI. What logic function is being performed? And.
17. Modify your circuit in Figure 4-29 by adding the fourth gate in the 4001 to the output as shown in Figure 4-30. Only the output change is shown. The rest of the circuit stays as in Figure 4-29.

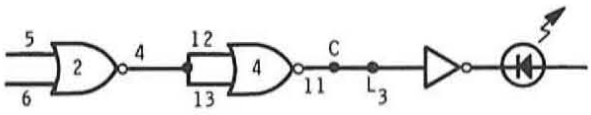

Figure 4-30

18. Using SW1 (A) and SW2 (B) data switches and monitoring LED indicators L1, L2 and L3, apply the states shown in Table VII. Record the output state (C) for each set of inputs.

Table VII

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

19. Study Table VII. What logic function is being performed? Nand.

Discussion

In Steps 3 through 5 you demonstrated how one of the four gate circuits in the 4001 IC could be used as an inverter. The two inputs are tied together to form a single input line. With this arrangement, the gate performs as a logic inverter where the input and output are complementary.

The input from SW1 is 0 and +5 volts. The approximate output levels should have been binary 0 = +.1 volts and binary 1 = +5 volts.

In Steps 7, 8 and 9 you demonstrated the basic logic function of the CMOS gate. Using positive logic it performs the NOR function. In Steps 10 and 11 you should have found that the basic CMOS gate performs the NAND function with negative logic.

In Step 12 you investigated the effect of open inputs. With both inputs open, the output could have been any voltage between 0 and +5 volts. Open inputs can result in operation in the linear region due to biasing by noise at the high impedance inputs. CMOS inputs should never be left open.

You demonstrated the CMOS gate can be connected to perform the basic OR function in Steps 13 and 14. In Figure 4-28, gate 1 is a NOR while gate 2 is connected as an inverter to complement the NOR and produce an OR output.

You next connected CMOS gates as an AND circuit and demonstrated its function in Steps 15 and 16. In Steps 17, 18 and 19 you added an inverter to the output of the AND to produce the positive NAND function. The AND and OR circuits are commonly implemented with CMOS NOR gates. However, the NAND version shown here is rarely used. A separate positive CMOS NAND logic element is available (CD4011AE) to eliminate the need to interconnect a 4001 as we did here.

SELECTING A DIGITAL INTEGRATED CIRCUIT FOR A SPECIFIC APPLICATION

The most important decision that you will make in designing a piece of digital equipment is in selecting the type of integrated circuit. The success or failure of your design from a performance and economic standpoint will depend directly upon this choice. For this reason, you must carefully consider the requirements of your application.

The first step in selecting a digital integrated circuit is to completely define the system characteristics. Performance, economy, and reliability are the prime requirements. These are specifically stated in the terms of needed system speed, noise immunity, power dissipation and other factors. Once all of the specifications have been detailed, these can be matched against the capabilities and characteristics of the various types of integrated circuits available.

The three key factors in defining a digital system and selecting a type of integrated circuit are speed (propagation delay), power consumption and noise immunity. While these are the most important characteristics in terms of performance and economy, there are other considerations. These include cost, availability, trends and the need for complex functions. The cost and availability factors are obvious. Lowest cost circuits are best if they meet all of the requirements of your application. And the circuits you choose must be readily available. It is desirable to select a circuit with several sources of supply.

Trends

The semiconductor industry is one of the most volatile in the field of electronics. New technological developments occur frequently and therefore some devices are quickly obsoleted while others with improved characteristics are added. These changes take place so quickly that it is difficult for any designer to select an integrated circuit with long life and a stable price. It is important for you to follow the trends by reading the manufacturer's literature and the technical publications. By staying abreast of the latest technology you will be better prepared to select a circuit that not only meets your design requirements but also will have favorable life, cost and availability trends.

Complex Functions

A highly desirable characteristic of any integrated circuit type is the availability of medium scale integrated circuits (MSI). These are functional circuits either of the combinational or sequential type. Since most digital equipment is made up of only a few basic types of circuits (decod-

ers, counters, etc.), a large portion of the equipment can be designed by simply interconnecting the functional circuits. It is much more economical to use MSI functions than to implement these same functions with SSI gate circuits. By using MSI functions the design time is reduced substantially. In addition the total package count and size is proportionally reduced. Savings in power consumption and in assembly labor can be significant. The more MSI functions available in a digital integrated circuit logic line, the more advantageous it is.

Trade Offs

Keep in mind that all of these factors are somewhat inter-related. Your choice of a type of digital IC will be a compromise based on your application and the circuits available. The speed-power trade off is one of the most critical trade-offs in selecting a circuit. Noise immunity is also a factor that may have to be traded off with some other characteristic depending upon the types of circuits available. You may have to juggle circuit specifications with cost and availability.

Figure 4-31 shows the primary characteristics of all of the types of digital logic circuits discussed in this section. It will permit you to compare the different types for your application. Only these types should be considered for new product design.

Comparison Of IC Logic Family Characteristics

Characteristic	TTL	ECL	MOS	CMOS
Fan-out	10	25	20	50+
Cost	low	medium to high	medium to high	low to medium
Power dissipation per gate (mW)	12 to 22	40 to 60	0.2 to 10	0.01 static 1 at 1 MHz
Noise generation	high	low to medium	medium	low medium
Immunity to external noise	good	good	good	very good
Temperature range (°C)	−55 to +125 0 to 75	−55 to +125	−55 to +125 0 to 75	−55 to 125 −40 to 85
Typical supply voltage (V)	+5	−5.2	−27, −13 (PMOS) +5 (NMOS)	+1.5 to 18
Avg. propagation delay per gate (ns)	3 to 12	1 to 2	300 (PMOS) 50 (NMOS)	70
Avg. clock rate (MHz)	15 to 120	200 to 1000	2 (PMOS) 5 to 10 (NMOS)	5 to 10

Figure 4-31

Figure 4-32 shows a chart of speed vs. power consumption for the various types of integrated circuits. Here propagation delay is plotted as a function of power dissipation for all of the most popular types of digital logic circuits. Naturally, the best circuit is the one with the shortest propagation delay and the least amount of power dissipation. You can see from this chart the type of circuit with the most favorable speed-power rating is low power Schottky TTL.

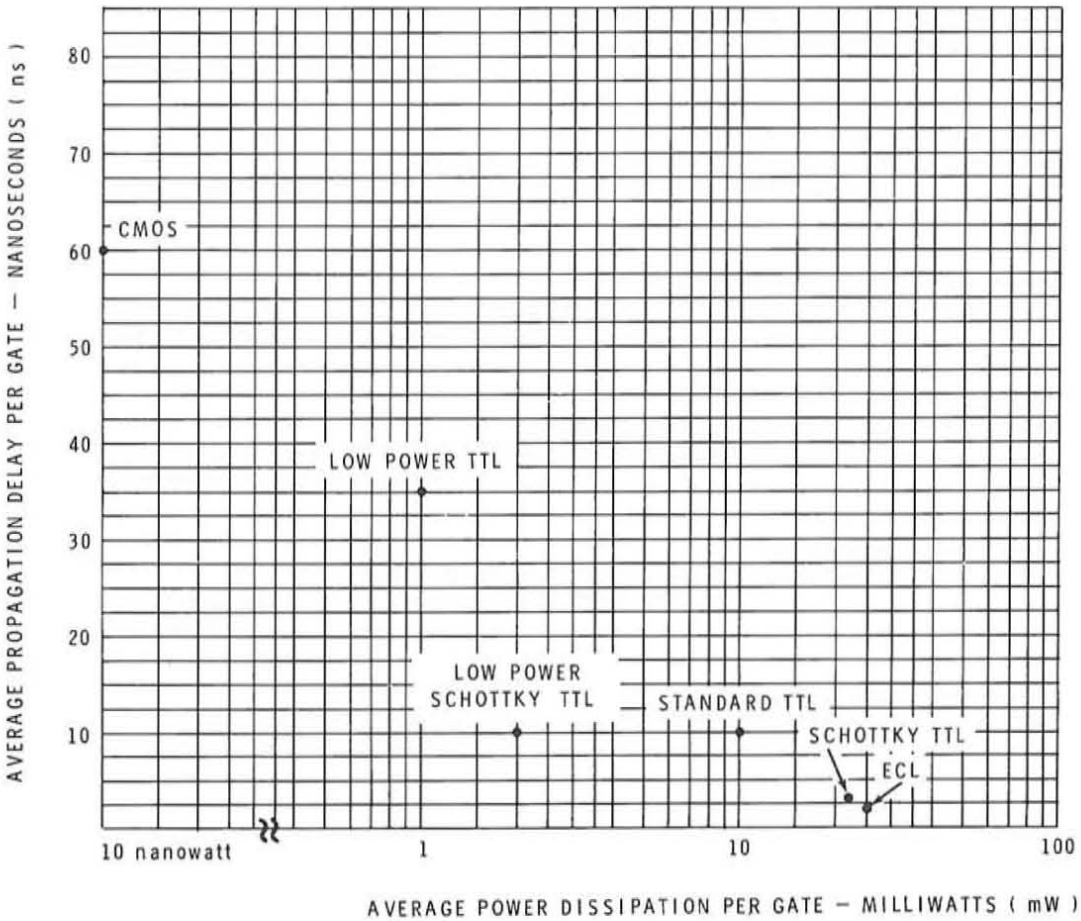

Figure 4-32
Speed (propagation delay) vs. Power dissipation for popular digital integrated circuits.

Self Test Review

32. The digital ICs primarily recommended for new equipment design are _____, _____, _____, and _____.
33. Name three *non-technical* characteristics that affect a designer's choice of a digital IC.
    a. _____
    b. _____
    c. _____
34. The most important trade-off in selecting a digital IC is the one involving _____ and _____.

Answers

32. TTL, CMOS, ECL, MOS
33. Cost, availability, trends, complex functions (MSI)
34. speed, power

EXAMINATION

UNIT 4

DIGITAL INTEGRATED CIRCUITS

The purpose of this exam is to help you review the key facts in this unit. The problems are designed to test your retention and understanding by making you apply what you have learned. This exam is not so much a test as it is another learning method. Be fair to yourself and work every problem first before checking the answers.

1. The most popular and widely used logic type is
   A. TTL
   B. CMOS
   C. MOS
   D. ECL
2. The fastest logic type is
   A. TTL
   B. CMOS
   C. MOS
   D. ECL
3. The logic type with the lowest power consumption is
   A. TTL
   B. CMOS
   C. ECL
   D. MOS
4. The logic type most used for LSI is
   A. TTL
   B. CMOS
   C. MOS
   D. ECL
5. The logic type with the best noise immunity is
   A. TTL
   B. CMOS
   C. MOS
   D. ECL

6. The type of transistor used in MOS and CMOS circuits is the
   A. depletion mode junction FET
   B. enhancement mode junction FET
   C. enhancement mode MOSFET
   D. NPN bipolar
7. Three CMOS logic gates with an average propagation delay of 70 nanoseconds are cascaded. The output state will change how many nanoseconds after a change in input state?
   A. 23.3
   B. 70
   C. 140
   D. 210
8. The power dissipated by a logic gate is proportional to its
   A. complexity
   B. noise immunity
   C. speed
   D. fan out
9. Refer to Figure 4-32. Which type of logic gate has the best speed-power trade off?
   A. Standard TTL
   B. Schottky TTL (low power)
   C. CMOS
   D. ECL
10. What type of logic circuit would you select for a battery operated unit in a noisy environment?
    A. TTL
    B. ECL
    C. CMOS
    D. MOS
11. The most popular IC package is the
    A. Plastic DIP
    B. ceramic DIP
    C. TO5
    D. flat pack
12. LSI circuits are most likely to be
    A. TTL
    B. MOS
    C. CMOS
    D. ECL

13. A combinational logic circuit made up of 35 gates inter-connected to perform a specific function is referred to as
    A. SSI
    B. MSI
    C. LSI
    D. MOS
14. The propagation delay of a typical logic gate is usually measured in
    A. nanoseconds
    B. microseconds
    C. milliseconds
    D. seconds
15. Draw the logic symbols used to represent a standard TTL gate and a standard ECL gate.

ANSWERS

UNIT 4

DIGITAL INTEGRATED CIRCUITS

1. A — TTL
2. D — ECL
3. B — CMOS
4. C — MOS
5. B — CMOS
6. C — enhancement mode MOSFET
7. D — 210 nanoseconds. The propagation delays are additive. 70 + 70 + 70 = 210 ns.
8. C — speed
9. B — Schottky TTL (low power) Those circuits in the lower middle portion of this graph have the shortest propagation delay and the lowest power. They are the best compromise of speed and power dissipation.
10. C — CMOS
11. A — plastic DIP
12. B — MOS Many LSI circuits also use CMOS.
13. B — MSI
14. A — nanoseconds
15. See Figure 4-33.

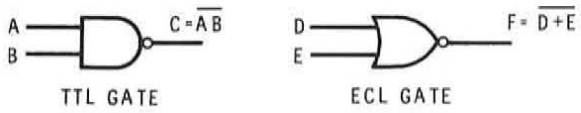

Figure 4-33
Basic RTL gate.

Individual Learning Program

In

DIGITAL TECHNIQUES

5-3 → 5-23

Heathkit
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UNIT 5

BOOLEAN ALGEBRA

Contents

UNIT 5
BOOLEAN ALGEBRA

INTRODUCTION

Boolean algebra is the special language of digital logic circuits. It is a mathematical method of expressing, analyzing, and designing logic circuits. It is similar in many ways to conventional algebra, but it is simpler and has several pertinent differences. It is easy to learn and extremely useful. It is almost essential to the proper understanding and application of digital circuits. In this unit, you will learn how to use Boolean Algebra. You will see how truth tables help you to design and understand logic circuits. And you will learn how to implement practical digital circuits using integrated circuit logic elements.

The specific things you will learn in this unit are outlined in the Unit Objectives which follow. Follow the individual steps listed in the Unit Activity Guide. Check off each item as you perform it and keep track of your time and progress in the spaces provided.

UNIT OBJECTIVES

When you complete this Unit on Boolean algebra, you will be able to:

1. Define Boolean Algebra.
2. Write the Boolean expression corresponding to a given logic circuit.
3. Draw the symbolic logic circuit implementing or corresponding to a given Boolean expression.
4. Write the Boolean expression corresponding to a given truth table.
5. Develop a truth table corresponding to a given Boolean expression.
6. Give an example of each of the two basic types of Boolean expressions.
7. Minimize a given logic expression using the various rules of Boolean algebra.
8. Implement a given Boolean expression with either NAND or NOR gates.

9. Write the two versions of DeMorgan's theorem.
10. Write the Boolean expression of logic circuits using the wired OR connection.
11. Properly connect the inputs and outputs of TTL and CMOS logic gates in typical applications.

UNIT ACTIVITY GUIDE

	Completion Time
☐ Play audio record 5, side 1 "Boolean Algebra"	_____
☐ Read section "Relating Digital Logic Circuits and Boolean Algebra"	_____
☐ Answer Self Test Review questions 1—5	_____
☐ Read section "Truth Tables"	_____
☐ Answer Self Test Review questions 6—7	_____
☐ Read section "Boolean Rules"	_____
☐ Answer Self Test Review questions 8—9	_____
☐ Read section on "Minimizing Logic Expressions"	_____
☐ Answer Self Test Review questions 10—14.	_____
☐ Read section on "Using NAND/NOR Gates"	_____
☐ Answer Self Test Review questions 15—16	_____
☐ Perform Experiment 7.	_____
☐ Perform Experiment 8	_____
☐ Complete Unit Examination	_____

RELATING DIGITAL LOGIC CIRCUITS AND BOOLEAN EQUATIONS

1. Boolean algebra is a simplified mathematical system used to deal with binary or two value functions. It permits us to express all of the various logic functions, both simple and complex, in a convenient mathematical format. This system gives us a method of understanding and designing digital logic circuits.

   In Boolean algebra, logic functions are expressed _____.

2. (mathematically) The mathematical expression of logic functions permits a convenient means of analyzing and expressing operations in digital circuits. It also aids greatly in design. The proper application of Boolean algebra usually results in the simplest, least expensive and most efficient logic circuit design.

   One of the most beneficial applications of Boolean algebra is in _____.

3. (design) Most digital equipment in use today is made with integrated circuits. Boolean algebra is used in designing these devices. The applications of integrated circuits in the design of modern electronic equipment, also involves Boolean algebra, but only to a lesser extent. At one time, the engineer or technician designing a digital system had to design not only the logic functions but also the circuits to implement them. Boolean algebra was his primary design tool.

   The modern digital designer does not need Boolean algebra today as much as he did in previous years because of the availability of _____ _____.

4. (integrated circuits) The engineer and technician using and designing digital circuits, finds Boolean algebra most valuable in expressing and analyzing logic circuits. His design job is basically that of choosing and using existing integrated circuits to implement the functions required by the application. Occasionally, Boolean algebra will be used to minimize a function and achieve an efficient design.

   However the greatest benefit of Boolean Algebra to the modern designer is in _____ and _____ digital logic operations.

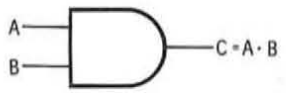


Figure 5-1

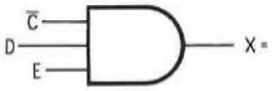


Figure 5-2

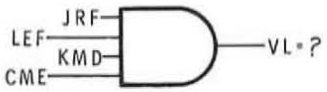


Figure 5-3

5. (analyzing or expressing) A Boolean expression is an equation that expresses the output of a logic circuit in terms of its inputs. You were introduced to Boolean expressions when you studied basic logic gates. The binary inputs and outputs were expressed as letters of the alphabet, alpha-numeric combinations, abbreviations or short words called mnemonics. For example, in the AND gate in Figure 5-1, the inputs are A and B and the output is C.

Note that the output C is expressed in terms of the inputs. The dot between the A and B indicates the AND function. The output expression C = A • B is read C equals A AND B. Remember that the inputs and outputs are binary signals which may assume either the binary 0 or binary 1 state.

What is the output expression of the AND gate in Figure 5-2? X $\overline{C}$ • D • E.

6. (X = $\overline{C}$ • D • E) In most Boolean expressions for the AND function the dot between each input variable can be eliminated and the expression written as a standard algebraic product like X = $\overline{C}$ D E. The AND function is sometimes referred to as the logical product.

Write the output expression for the AND gate in Figure 5-3. JRF LEF KMD CME = VL

7. (VL = JRF • LEF • KMD • CME) In this expression each input is identified by a three letter combination called a mnemonic. The output is a two letter mnemonic. The dot between each input not only designates the AND function but also helps to separate or distinguish the inputs from one another. Occasionally you will see parenthesis used to separate the inputs and indicate the logical product or AND function.
VL = (JRF) (LEF) (KMD) (CME).

If all of the inputs in the above expression are binary 1, the output will be binary 1.

8. (binary 1) The AND function states that the output will be binary 1 only if all inputs are binary 1. If any one or all inputs are binary 0, the output will be binary 0.

Sketch the AND gate implementing the function W = (F) (MX) ($\overline{G}$.) Label inputs and outputs.

9. (See Figure 5-4)

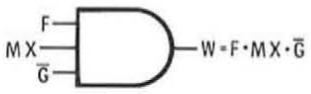


Figure 5-4

Other logic functions like inversion are also expressed with Boolean expressions.

If the input to an inverter is B and the output is designated Z, write the output expression. $Z = \overline{B}$.

10. ($Z = \overline{B}$) The output of an inverter is the complement of the input. This is expressed by putting a bar over the input variable. The term $\overline{B}$ is expressed as NOT B or B NOT. The term NOT refers to logic inversion. See Figure 5-5.

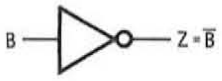


Figure 5-5

Draw the logic circuit corresponding to the expression CTL = $\overline{INV}$.

11. (See Figure 5-6) The output CTL is the complement of the input INV. CTL = $\overline{INV}$

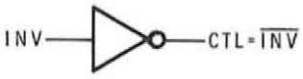


Figure 5-6

If the input is a binary 1, the output will be binary _____.

12. (binary 0) And if the input is binary 0 the output will be binary 1.

Another common logic function is the OR. In an OR gate the output will be binary 1 if

a. only all inputs are binary 1
b. any one or more inputs are binary 1
c. all inputs are binary 0.

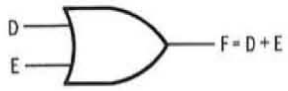


Figure 5-7

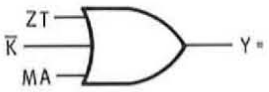


Figure 5-8

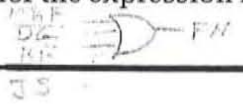
13. (b) The output of an OR gate is binary 1 if any one or more of the inputs is a binary 1. A typical OR logic gate and its related output expression is shown in Figure 5-7. The plus sign between the input variables designates the OR function. It is sometimes referred to as the logical sum.

$Y = ZT + \overline{K} + MA$

Write the output expression of the logic gate in Figure 5-8.

14. (Y = ZT + $\overline{K}$ + MA) The plus sign or OR function separates the input variables.

Draw the logic symbol for the expression FN = MAF + $\overline{DG}$ + BF + JS



15. (See Figure 5-9)

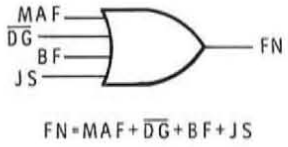


Figure 5-9

It is important that you be able to draw the logic diagram corresponding to a given Boolean expression or write the Boolean equation from a given logic diagram.

The output of a logic circuit is a function of its inputs.

16. (inputs) The output of a logic circuit is a function of the states of the inputs and, of course, the special logical characteristics of the circuit itself.

While there are some simple digital control operations that can be implemented with a single logic gate, more often it is necessary to use a number of logic gates to implement the desired decision-making function. When two or more logic elements are combined, the result is known as a combinational logic circuit. The circuit usually has multiple inputs and either a single output or multiple outputs depending upon its exact function.

Using AND and OR gates together to implement a special logic function creates a type of digital circuit called a combinational circuit.

17. (combinational) Any combination of multiple ANDs, ORs, and NOTs is called a combinational logic circuit. Such circuits are used for sophisticated decision-making functions.

There are many common combinational logic circuits used in digital equipment. They perform specific functions that tend to regularly reoccur in digital equipment. However, regardless of the type of combinational logic circuits there are two basic circuit forms. These are referred to as the sum-of-products and product-of-sums circuits. Here the term product refers to the AND function while the sum refers to the OR function.

The AND function is written in the same form as the algebraic product or the multiplication of two variables. (A and B = AB) The OR function is written as the sum of two input variables. (D OR E = D + E). The sum-of-products or product-of-sums expressions combine the AND and OR functions in a variety of ways.

Combinational logic circuits are used for _____ _____.

18. (decision making) Any combination of AND and OR gates is used for logical decision making purposes.

The most commonly used Boolean expression of complex decision making functions is the sum-of-products. The expression X = A • B + C • D • E is an example.

Figure 5-10 shows the logic circuit implementing this sum of products logical function. Here AND gate 1 forms the logical product AB while gate 2 forms the product CDE. These products are summed or logically ORed in gate 3 to form the output expression. This is what is meant by the sum-of-products.

Is the expression $QT = PJ \cdot \overline{W} + HV \cdot LM + GND \cdot \overline{C} \cdot F$ in sum-of-products form? _____.

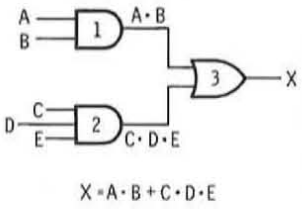


Figure 5-10

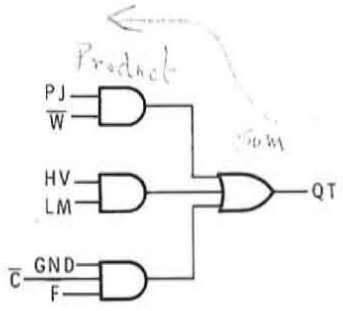


Figure 5-11

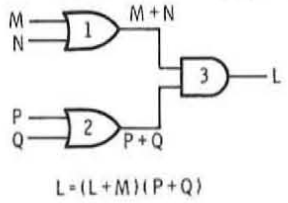


Figure 5-12

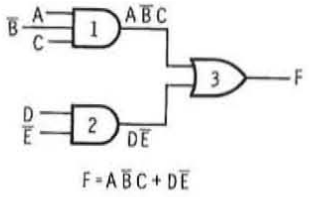


Figure 5-13

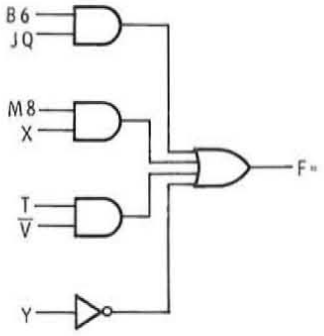


Figure 5-14

19. (yes) This expression is in the sum-of-products form. The various inputs are ANDed together in several combinations which are then ORed together. The circuit for this function is shown in Figure 5-11.

The distinguishing feature of this circuit is that the inputs feed AND gates and the output is derived from an OR gate.

The other type of Boolean expression is the product-of-sums. An example is the expression L = (M + N) (P + Q). The equivalent circuit is shown in Figure 5-12. Inputs M and N are ORed together in gate 1 while inputs P and Q are ORed in gate 2. The two logical sums are ANDed in gate 3 to produce the logical product. In this arrangement the distinguishing feature is the OR gate inputs and AND gate output.

The AND function produces a logical _____ while the OR function produces a logical _____.

20. (product, sum) Your familiarity with this system should permit you to write the Boolean expression from any logic circuit and draw the logic circuit corresponding to a given Boolean equation.

To write the equation of a given logic circuit, you start at the inputs and write the output expression for each gate in the circuit from left to right until the output equation is developed. The unique gate symbols of course will tell you the logic function being performed. The example in Figure 5-13 illustrates this procedure.

You first write the output expressions for the two input AND gates. These expressions become the inputs to the OR gate whose output equation is then written. The result is the Boolean expression for the circuit.

$$F = A\overline{B}C + D\overline{E}$$

Write the equation of the circuit given in Figure 5-14. _____.

21. $(F = B6 \cdot JQ + M8 \cdot X + T \cdot \overline{V} + \overline{Y})$

You simply write the correct output for each of the input AND gates and use these as the inputs to the OR gate. Working this way from left to right quickly produces the complete output expression.

What form is this equation in? _____.

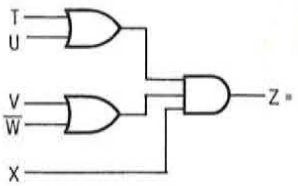


Figure 5-15

22. (sum-of-products)

The input AND gates form products which are logically summed in the output OR gate.

This procedure of writing the equation for a given circuit also works on a product-of-sums circuit like the one in Figure 5-15.

$Z = T+U \cdot V+\overline{W} \cdot X$

What is the output expression of this circuit? _____.

23. $(Z = (T + U) \cdot (V + \overline{W}) \cdot X)$

The logical sums are formed by gates 1 and 2 and their outputs are combined to form the logical product in the output AND gate. See Figure 5-16.

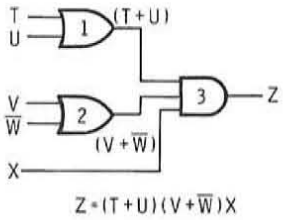
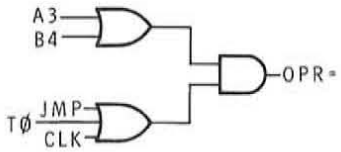


Figure 5-16

Again you work from left to right developing the output of each gate until the complete expression is formed.

What is the output of the circuit Figure 5-17? _____.



OPR = A3B4 + TØ(JMP + CLK)

Figure 5-17

24. $(OPR = (A3 + B4)(JMP + T\phi + CLK))$

To draw the diagram corresponding to a given expression you first study the equation to determine whether it is a sum-of-products or product-of-sums. This will give you the type of output gate.

A sum-of-products circuit uses an _____ gate output.

25. (OR) A product-of-sums uses an _____ gate output.

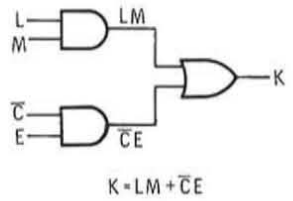


Figure 5-18

26. (AND) Then you work backward from the output developing the inputs and outputs from right to left.

For example, consider the expression K = LM + $\overline{C}$E. This is in sum-of-products form so the output gate is an OR. The inputs to this OR gate are LM and $\overline{C}$E. Each of these is a product that is developed by an AND gate with the appropriate inputs. See Figure 5-18.

Draw the circuit for the expression SH = (CLK + T5) ENB.

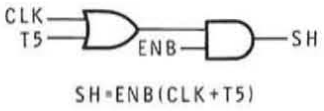


Figure 5-19

27. (See Figure 5-19) This expression is in product-of-sums form but here there is only one logical sum (CLK + T5). The output is a product, however, and is produced by an AND gate. The input sum is produced by the OR gate.

Draw the circuit for the expression Y = ADD • CY + SUB • $\overline{\text{INV}}$ + MPY • ADD • SUB

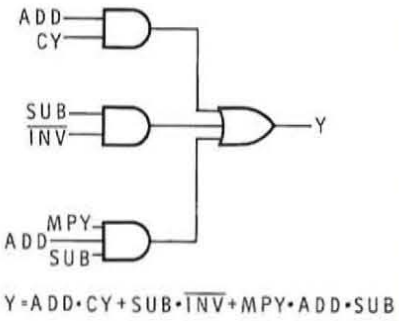


Figure 5-20

28. (See Figure 5-20)

This is sum-of-products form. Note that some of the input signals (ADD, SUB) are applied to more than just one of the input gates.

So far we have only worked with two levels of logic, that is the inputs are conditioned by two sets or levels of logic gates in cascade: ANDs into OR or ORs into AND. Other more complex logic networks use three, four or even more levels of logic. The expression and circuit in Figure 5-21 is one example.

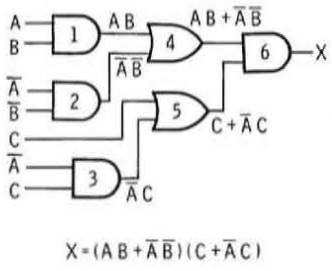


Figure 5-21

Here both the sum-of-products and product-of-sums formats are combined.

How many levels of logic are there in the circuit of Figure 5-21?

_____.

29. (3) The input signals must propagate through a series of three gates before a level change occurs at the outputs. Input C on gate 5 only propagates through two levels.

Draw the circuit corresponding to the expression

$$F = (A + \overline{B})\,(\overline{A} + B) + (B + \overline{C})\,\overline{A}$$

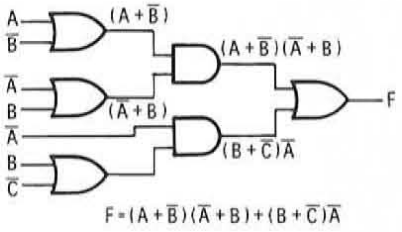


Figure 5-22

30. (See Figure 5-22) Again you can see that the sum-of-products and product-of-sums are combined to form a three level logic circuit.

The same principles of converting from circuit to equation and equation to circuit you learned for two level logic apply to more complex multi level circuits.

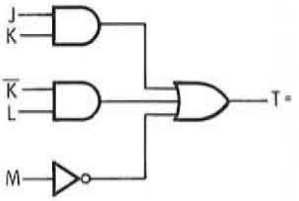


Figure 5-23

Self Test Review

1. The most commonly used logic format is
   a. sum-of-products
   b. product-of-sums
   c. combination of a. and b.
   d. neither a. or b.
2. Draw the circuit for the expression $M = \overline{V}W + XY + \overline{W}\overline{X}Y$.
3. Draw the circuit for the expression $F = T\,(U + \overline{V})\,(\overline{T} + W)$.
4. Write the Boolean expression for the circuit in Figure 5-23.
5. Write the Boolean equation for the circuit in Figure 5-24.

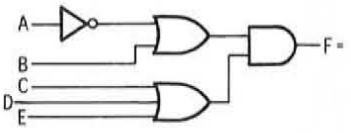


Figure 5-24

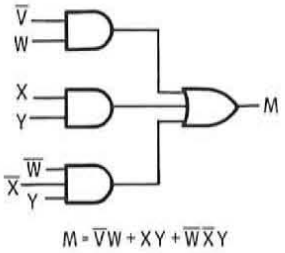


Figure 5-25

Answers

1. a. sum-of-products
2. See Figure 5-25
3. See Figure 5-26
4. $T = JK + \overline{K}L + \overline{M}$
5. $F = (\overline{A} + B)\,(C + D + E)$

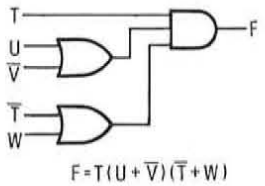


Figure 5-26

TRUTH TABLES

31. One of the most useful tools for analyzing, designing or otherwise working with digital circuits is the truth table. A truth table is a chart that lists all possible input and output signal combinations for a given logic circuit. The truth table is a tabular listing of all input and output states in binary 0 and binary 1 form. The truth table completely defines the operation of the circuit.

    A truth table can be used to determine what input conditions cause a given logic circuit to produce a binary 1 output. True or False.

32. (True) You can look at a truth table and quickly identify which specific combination of input states that will produce a binary 1 (or binary 0) output.

    Truth tables are used in defining the operation of simple logic circuits like inverters and gates as well as more complex combinational logic circuits. You have already seen how truth tables are used in defining the basic logic operations such as AND, OR and NOT.

    In the way of a review, the truth table below defines what type of logic circuit? _____.

INPUT A	OUTPUT $\overline{A}$
0	1
1	0

33. (inverter or NOT circuit) The truth table shows both the input and output. The output $\overline{A}$ is always the opposite or complement of the input A. Therefore, the circuit is an inverter.

The truth table for a two input AND gate is illustrated below. The inputs A and B define all possible input combinations.

INPUTS		OUTPUT
A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

Column C shows the output state corresponding to each input combination. By studying the inputs and outputs you can determine the exact nature of an AND gate.

The only time the output is binary 1 is when input A is _____ and input B is _____.

34. (1, 1) The output is binary 1 only when both inputs are binary 1. This is true of any AND gate.

Complete the truth table below to define the operation of an OR gate where the output will be binary 1 if any or all inputs are binary 1.

INPUTS		OUTPUT
D	E	F
0	0	0
0	1	1
1	0	1
1	1	1

35. (Binary 1 outputs occur for input states of 01, 10 and 11) The total number of possible input conditons is 2^n where n is the number of inputs. In two input circuits there are $2^2 = 4$ possible input conditions. If we treat the inputs as bits in a multibit binary word, we can quickly define and record all input states by using the binary number equivalents. For example, with four possible input states we use the four numbers 0 through 3 or 00, 01, 10 and 11 in binary. These are all possible combinations for a two bit word.

A logic circuit has three inputs. How many possible logic input conditions are there? _____.

36. ($2^3 = 8$) We represent the eight possible input conditions with the binary equivalent of the numbers 0 through 7. If the inputs are designated X, Y and Z, the input states are as shown below.

INPUTS			OUTPUT
X	Y	Z	W
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

This particular method of listing all possible input combinations by counting from zero through the upper limit is orderly and convenient.

The logic function defined by the table above is the _____ function.

37. (OR) The output is binary 1 any time one or more of the inputs is a binary 1 so the OR function is defined.

There are two basic ways of using truth tables in logic work. First we can develop a truth table from a given logic circuit, and second we can develop an equation or logic circuit from a given truth table. The circuit-to-table method is useful in circuit analysis. The table-to-equation or circuit is a useful design method.

A useful circuit analysis approach is to develop a _____ _____ from the _____ _____.

38. (truth table, logic circuit) Developing the truth table for a given circuit starts with defining all of the inputs. Then the output for each gate in the circuit is developed until the final output is obtained. Consider the circuit shown in Figure 5-27.

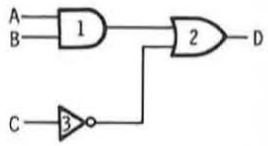


Figure 5-27

The Boolean output expression for this circuit is _____.

39. ($D = AB + \overline{C}$) The output of gate 1 is AB and the output of inverter 3 is $\overline{C}$. These signals are ORed in gate 2 to produce $D = AB + \overline{C}$.

To develop the truth table for this circuit, we start with the inputs. Since there are three inputs there are $2^3 = 8$ possible input conditions that we define with the three bit numbers 000 through 111 as indicated in the table below. In the table we also create a column for the output of each gate or element in the circuit.

INPUTS			OUTPUTS		
A	B	C	Gate 1 AB	Inverter 3 $\overline{C}$	Gate 2 D
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

Observing the inputs, we can fill in the AB and $\overline{C}$ columns. The $\overline{C}$ column is simply the complement of the C input column. To complete the AB column, you consider the A and B inputs and their effect on the AND gate output.

Complete the AB and $\overline{C}$ columns above, and check your results in the next frame.

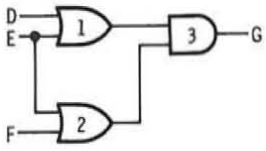


Figure 5-28

40. (See Table below)

INPUTS			OUTPUTS		
A	B	C	AB	$\overline{C}$	D
0	0	0	0	1	1
0	0	1	0	0	0
0	1	0	0	1	1
0	1	1	0	0	0
1	0	0	0	1	1
1	0	1	0	0	0
1	1	0	1	1	1
1	1	1	1	0	1

Next, to find the D output, you note that the AB and $\overline{C}$ outputs are ORed in gate 3. You complete the D column by recording a binary 1 each time either one or both of the AB or $\overline{C}$ columns are binary 1. Check this in the table above.

Now, do the entire job yourself. Create a complete truth table for the circuit in Figure 5-28. Check your results in the next frame.

41. (See table below)

INPUTS			OUTPUTS		
D	E	F	(D + E)	(E + F)	G
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	1	1
0	1	1	1	1	1
1	0	0	1	0	0
1	0	1	1	1	1
1	1	0	1	1	1
1	1	1	1	1	1

To produce this table you first note the number of inputs. There are three different variables D, E, and F so there are $2^3 = 8$ possible input combinations.

Next you create a column for each gate output. In this case, gate 1 output is (D + E), gate 2 output is (E + F), and the final output at gate 3 is G = (D + E) (E + F).

To fill in the (D + E) column you OR together the D and E input columns. You record a binary 1 when either one or both column D or E are binary 1. You complete the (E + F) column in a similar manner considering all eight E and F input combinations.

Finally, you AND together the (D + E) and (E + F) columns, recording a binary 1 in the G column only when both (D + E) AND (E + F) columns are binary 1.

The truth table like the one you developed above completely defines the circuit operation for all possible conditions. And your analysis is thorough because to obtain the final output you had to derive the outputs of all other gates in the circuit.

The primary value of the circuit-to-truth table approach is in circuit _____.

42. (analysis) In designing digital circuits we use the opposite approach. We develop a truth table as the result of our design. In designing a logic circuit we designate the number of inputs and what the output state should be for each set of input conditions. Then we write the Boolean equation from the truth table. From there the equation is readily translated into a logic diagram.

Assume that the circuit we want to design has two inputs A and B and we want a binary 1 output C to occur when A is 0 and B is 1 or when A is 1 and B is 0. Otherwise the output is binary 0.

Which truth table below defines these conditions?

a.

INPUTS		OUTPUT
A	B	C
0	1	1
1	0	1

b.

INPUTS		OUTPUT
A	B	C
0	0	1
0	1	0
1	0	0
1	1	1

c.

INPUTS		OUTPUT
A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

43. (c.) The correct table is shown below.

INPUTS		OUTPUT
A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

To write the output equation from this table we observe the output column C, noting those input states where binary 1s occur. Then we write a sum-of-products type Boolean expression based on these inputs. For each binary 1 state in the output we write one product term for the equation then we logically sum (OR) these terms.

The product terms are written from the input states. If the input is binary 1 we write the input letter. If the input is binary 0 we write the complement of the input letter. For example, when A is 0 and B is 1, the product term is $\overline{A}B$.

What is the product term where A is 1 and B is 0? $A\overline{B}$.

44. ($A\overline{B}$) The input conditions for each binary 1 output state is now defined. The product terms are then ORed. The result is C = _____.

45. ($C = \overline{A}B + A\overline{B}$) Write the output equation from the truth table below.

INPUTS		OUTPUT
J	K	L
0	0	1
0	1	0
1	0	0
1	1	1

L = _____.

46. ($L = \overline{J}\overline{K} + JK$) A binary 1 output occurs for two of the four possible input combinations. Therefore you know that the sum-of-product output equation will mention two product terms. The inputs are ANDed to form these products. The first output occurs when J = 0 and K = 0. Therefore the corresponding product is $\overline{J}\,\overline{K}$. The second output is binary 1 when J = 1 and K = 1. The product defining this condition is JK. To obtain the complete output expression we logically sum (OR) these products. $L = \overline{J}\,\overline{K} + JK$.

From here the logic diagram can be drawn.

Sketch the logic diagram of the equation just derived.

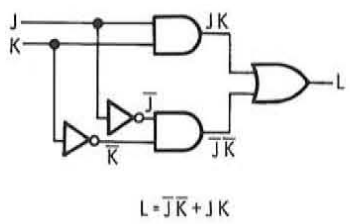


Figure 5-29

47. (See Figure 5-29)

Now try your hand at a more complex problem. Write the equation and draw the circuit corresponding to the truth table below.

INPUTS			OUTPUT
A	B	C	D
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

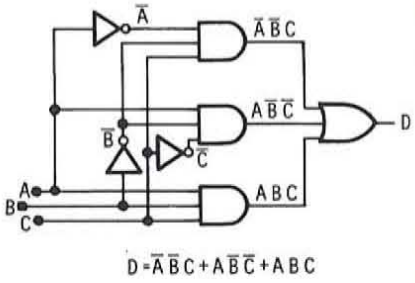


Figure 5-30

48. ($D = \overline{A}\,\overline{B}\,C + A\,\overline{B}\,\overline{C} + A\,B\,C$, See Figure 5-30)

In this problem there are three inputs, so each product term will have three factors and the number of product terms is set by the number of times a binary 1 output appears in the D output column. You develop each product by looking at the input states and writing the variable when a binary 1 input occurs and the complemented variable when a binary 0 input occurs. The product term when A = 0, B = 0 and C = 1 is $\overline{A}\,\overline{B}\,C$. Once all the product terms are developed they are ORed together to obtain the output. The logic diagram is then drawn from the equation. Note in the logic diagram that inputs A, B and C are considered to be available and signals $\overline{A}$, $\overline{B}$, and $\overline{C}$ are generated with inverters. In some circuits the complement signals may already be available from other sources in which case the inverters can be omitted.

Self Test Review

6. Develop a truth table for the circuit shown in Figure 5-31.
7. What is the Boolean equation corresponding to the truth table below?

INPUTS			OUTPUT
R	S	T	V
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

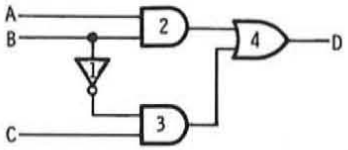


Figure 5-31

Answers

6.

INPUTS			OUTPUTS			
A	B	C	Inverter 1 $\overline{B}$	gate 2 AB	gate 3 $\overline{B}C$	gate 4 D
0	0	0	1	0	0	0
0	0	1	1	0	1	1
0	1	0	0	0	0	0
0	1	1	0	0	0	0
1	0	0	1	0	0	0
1	0	1	1	0	1	1
1	1	0	0	1	0	1
1	1	1	0	1	0	1

7. $V = \overline{R}\overline{S}\overline{T} + \overline{R}\,S\,T + R\,\overline{S}\,\overline{T} + R\,S\,\overline{T}$

BOOLEAN RULES

49. As we mentioned earlier, the primary benefit of Boolean Algebra to a technician or engineer today is in analyzing, understanding and concisely expressing digital logic functions. The availability of a wide variety of integrated circuits has greatly minimized the use of Boolean Algebra as a design tool. However, even with modern ICs, the designer can often benefit from the use of Boolean algebra in minimizing or implementing a function.

Boolean Algebra is the algebra of two-valued functions. Many of the ordinary rules of algebra such as factoring or expanding a function, apply to Boolean expressions. However, the binary nature of the functions greatly simplifies most of the operations. There are also numerous special rules that apply to handling binary logic functions. We will explain these rules in this section and show how they are used.

Most standard algebra rules work with Boolean expressions. True or False? _____.

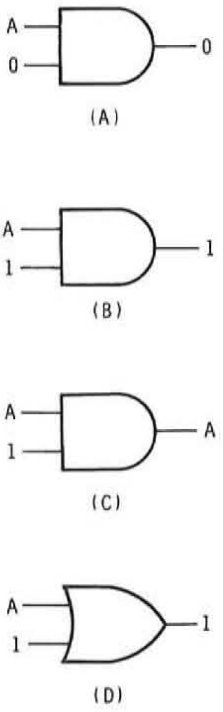


Figure 5-32

50. (True) Yes, most conventional algebra manipulations will work on binary expressions. But it is the special rules that are of the most value to the digital designer.

The Laws of Intersection, for example, apply to AND gates. The two forms of this law are stated below.

$$A \cdot (1) = A$$
$$A \cdot (0) = 0$$

Remembering that A is a binary signal that can be either binary 0 or binary 1, we can prove the validity of these expressions if we remember how an AND gate works. The first expression simply says that if we apply a binary 1 to one input of an AND gate and the signal A to the other input, the output will be A. The binary 1 input simply enables the gate so that the A input state controls the output. If A = 1, the output will be 1. If A = 0, the output will be 0.

Which circuit in Figure 5-32 expresses this relationship?

51. (c) The other form of the Laws of Intersection is just as easy to understand.

$$A\ (0) = 0$$

It says that if one input to an AND gate is 0 and the other is A, the output will always be 0. Remember that the only time the output of an AND gate can be 1 is when all inputs are binary 1. If one input is fixed at 0, the output will always be 0. The circuit in Figure 5-33 expresses this.

Figure 5-33

Complete the expression: D • E • (0) = _____.

52. $(D \cdot E \cdot (0) = 0)$ If one input to an AND gate is 0, the output will be zero regardless of the states of the other inputs. This proves that the Law of Intersection works for AND gates with more than two inputs. For example, D • E • (1) = D • E. You can also equate this expression to the algebraic version that says that a function (DE) multiplied by 1 is the function.

$$DE \times 1 = DE$$

Another similar set of rules exist for OR gates. These are called the Laws of Union. Expressed algebraically they are

$$B + 1 = 1$$
$$B + 0 = B$$

Sketch the logic diagrams for each of these and label the inputs and outputs.

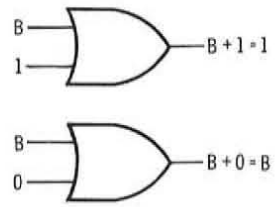


Figure 5-34

53. (See Figure 5-34) These expressions like those for the AND gate almost perfectly define the operation of an OR gate. In the first version, if we apply a binary 1 to one input of an OR gate and a signal B to the other, the output will always be binary 1 by definition of an OR gate. If one input to an OR gate is binary 0, the other input B will control the output.

A quick way to prove the Laws of Union is to look at the truth table for an OR gate.

INPUTS		OUTPUT
B	C	D
0	0	0
0	1	1
1	0	1
1	1	1

To prove that B + 1 = 1 simply assume input C to be fixed at 1 and observe the output D for those cases. Do the same to prove B + 0 = B. Assume input C is 0 and observe the output D for the two corresponding B input states.

By using the truth table for an AND gate you can prove the Laws of _____.

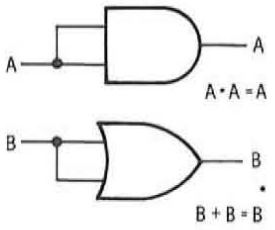


Figure 5-35

54. (Intersection) The procedure is the same for proving the Laws of Intersection with the truth table of an AND gate.

The Laws of Tautology apply to both AND gates and OR gates. The basic rules are given below.

$$A \cdot A = A$$
$$B + B = B$$

The related logic symbols are shown in Figure 5-35.

What these expressions say is that if you apply the same signal to all inputs of a logic gate, the output will be the same as the input. Again, you can prove this to yourself by looking at the truth tables for AND and OR gates.

Use the Laws of Tautology to simplify the expression QT = JMX + JMX + F9. _____.

55. (QT = JMX + F9) The JMX term is redundant. In terms of circuitry you can see the simplification. The circuit in Figure 5-36A implements the original expression. Figure 5-36B shows the simplified but fully equivalent circuit.

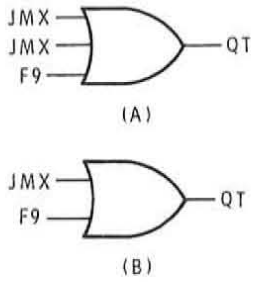


Figure 5-36

This same simplification procedure applies to AND gates.

Use the Laws of Tautology to simplify the expression $X = Q \cdot Q \cdot J$. Draw the original and simplified logic diagrams.

56. (See Figure 5-37)

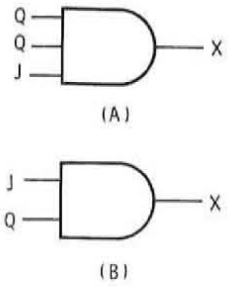


Figure 5-37

The original circuit can be implemented as shown in Figure 5-37A. The simplified but equivalent circuit is shown in Figure 5-37B. The logical function is identical. Now you are beginning to see that the value of Boolean algebra is simplifying the design of a circuit.

Another Boolean law is the Law of Complements. These are

$$A \cdot \overline{A} = 0$$
$$B + \overline{B} = 1$$

If we apply a logic signal and its complement to a logic gate, the output becomes either a binary 0 or a binary 1 depending on type of logic gate. This is illustrated in Figure 5-38.

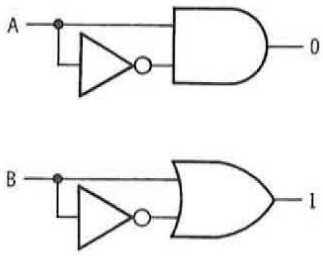


Figure 5-38

In these circuits, the output is a function of the state of the input. True or False? _____.

57. (False) If you look closely at these circuits and analyze what happens, you will see that in either case the output is not affected by the state of the input. It can be either a 1 or a 0 and the output will be binary 0 for the AND gate and binary 1 for the OR gate. In this case the output is a function of the _____.

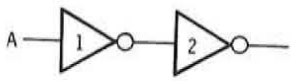


Figure 5-39

58. (type of logic circuit) You can further verify these laws by referring to the AND and OR truth tables. A binary 0 on either input of an AND gate will always produce a binary 0 output. A binary 1 on either input of an OR gate will always produce a binary 1 output.

Now consider the Law of the Double Negative.

$$\overline{\overline{A}} = A$$

It says that the complement of the complement of A is equal to A. Or a signal that is complemented twice is the same as the original signal. You can see this from the circuit in Figure 5-39.

If input A is 1, the output of inverter 1 is _____ and the output of inverter 2 is _____.

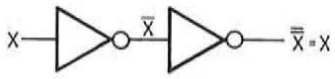


Figure 5-40

59. (0, 1) Inverter 1 complements the 1 input to a 0. Inverter 2 complements the 0 back into a 1 so that the output of the circuit is equal to the input. Complementing a signal twice or any even number of times gives us the original signal. Figure 5-40 shows this.

To simplify this two inverter circuit you could replace it with which of the circuits in Figure 5-41? _____

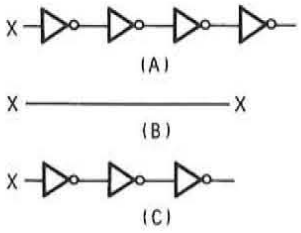


Figure 5-41

60. (B) In terms of simplification, if you encounter two inverters in cascade, you can simply remove them and substitute a piece of wire since the effect is the same. Three cascade inverters or any odd number produces the same effect as a single inverter so this is not equivalent. Four cascade inverters does produce an output that is the same state as the input, but this is certainly not simplification.

All along we have been saying that when an even number of inverters are cascaded, the output is the same as the input. This is true of course for a static (non changing) input. But when the input is switching rapidly, the output is almost, but not quite the same as the input.

Which characteristic of a logic gate do you think causes this difference when the input signal is changing rapidly?

A. Logic level
B. Power dissipation
C. Noise immunity
D. Propagation Delay.

61. (D., Propagation delay) Of course. When the input signal changes it takes a finite time for it to propagate through each circuit in a chain. The output then is delayed from the input by an amount of time of the total circuit propagation delay.

In a two inverter string where the propagation delay for each inverter is 12 nanoseconds, the output is delayed from the input by _____ nanoseconds.

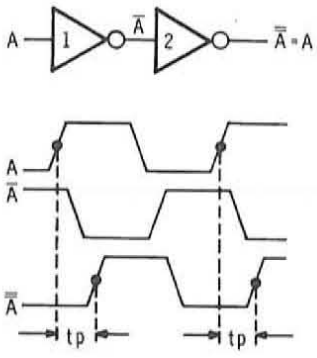


Figure 5-42

62. (24) The total propagation delay is the sum of the individual propagation delays. Figure 5-42 shows the input and output waveforms of a two inverter string. The total propagation delay is t_p.

Another Boolean rule is the Law of Commutation. This is the same rule from basic algebra. The two forms of it are:

$$A \cdot B = B \cdot A$$
$$A + B = B + A$$

All it really says is that you can arrange the inputs to AND or OR gates in any order and the effect is the same. You can write the input variables in any order and they will mean the same thing.

$$W + X + Y = X + W + Y$$

True or False? _____.

63. (True) Also JML = LJM = MLJ = JLM = LMJ = MJL. The order of the inputs is different, but the logical results is the same for each. Incidentally, don't forget that all of these Boolean rules work for 3 or more inputs although we are illustrating them with only two inputs for simplicity.

Now let's give you some practice in using these rules. What are the simplifications of the expressions below?

a. $A + \overline{B} + A =$ _____
b. $B\,C\,\overline{B} =$ _____
c. $C + 1 + \overline{B} =$ _____
d. $\overline{X} + Y + X =$ _____

Work these problems using the previously discussed rules. Check your answers in the next frame.

64. a. $A + \overline{B}$
b. 0
c. 1
d. 1

In problem (A) you first rearranged it by using the Law of Commutation $A + \overline{B} + A = A + A + \overline{B}$. By the Law of Tautalogy, you know that $A + A = A$, so the resulting simplified equation is $A + \overline{B}$.

In problem (B) you again rearrange the term using the Law of Commutation. $BC\overline{B} = B\overline{B}C$. From the Law of Complements you know that $B\overline{B} = 0$. Substituting this in the expression gives $0 \cdot C$. You know from the Law of Intersection that $0 \cdot C$ or $C \cdot 0 = 0$.

In problem (C) you should recognize the Laws of Union. $C + 1 + \overline{B} = 1$.

In problem (D), you first rearrange the equation by way of the Law of Commutation to $\overline{X} + Y + X = X + \overline{X} + Y$. The Law of Complements says that $X + \overline{X} = 1$. Therefore, the equation becomes $1 + Y$. Of course this reduces to 1 by way of the Law of Union.

Go to the next frame.

65. Now try a few more examples using the previous solutions as a guide. But this time draw the logic diagram of the original expression as well as the simplified version to get a feel for the result of Boolean simplification in terms of circuitry.

a. $L + M + \overline{M}$
b. $J K \overline{K} L$
c. $F + T + F$
d. $\overline{B} + A C \overline{A} + D$

The answers are given in the next frame.

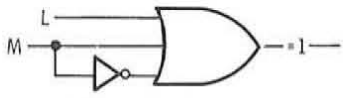


Figure 5-43

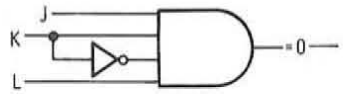


Figure 5-44

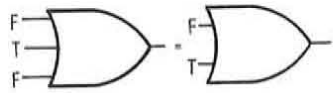


Figure 5-45

66. a. $L + M + \overline{M} = L + 1 = 1$

The three input OR and inverter called for by the original expression reduces to a single wire with a binary 1 on it.

b. $J\,K\,\overline{K}\,L = J \cdot 0 \cdot L = 0$

The reduced expression is simply a binary 0 level.

c. $F + T + F = F + F + T = F + T$

d. $\overline{B} + A\,C\,\overline{A} + D = \overline{B} + A\,\overline{A}\,C + D = \overline{B} + 0 \cdot C + D = \overline{B} + 0 + D = \overline{B} + D$

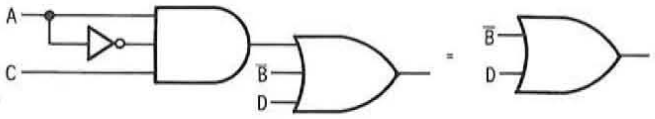


Figure 5-46

By now you should be able to see the value of Boolean algebra in simplifying a logic expression and minimizing the amount of circuitry required to implement it. Fewer parts means lower cost, smaller size and less power consumption.

Go to the next frame.

67. Another Boolean law identical to the basic algebra rule is the Law of Association. These are

$$(A \cdot B)\,C = A\,(B \cdot C) = A \cdot B \cdot C$$
$$A + (B + C) = (A + B) + C = A + B + C$$

You can see the circuitry simplification that results by applying these rules. See Figure 5-47.

Figure 5-47

Note that we trade two 2-input AND gates for a single 3-input gate.

Draw the OR gate circuit equivalents for the Law of Association.

68. (See Figure 5-48)

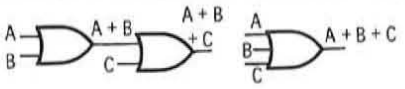


Figure 5-48

Note that the logical effect is the same for either version of the circuit. The three input gate is usually more economical than two 2 input gates.

Now let's consider the Laws of Distribution. We will use some of the rules described earlier to prove this law. The Laws of Distribution are:

$$A\,B + A\,C = A\,(B + C)$$

You should be able to infer this because all you are doing is factoring out one term as you would in basic algebra.

Sketch the logic diagrams for each side of the above equation.

69. (See Figure 5-49)

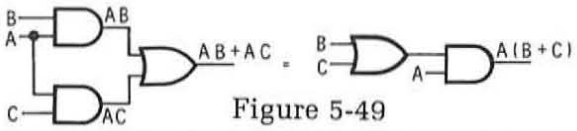


Figure 5-49

Study these two frames carefully. Not only was there a reduction in the number of circuits used, but also note that the expression changed from a sum-of-products to a product-of-sums form.

Using a truth table show that the logical effect of both circuits is identical.

70. (See tables below) Your tables should appear as shown below.

INPUTS			GATE OUTPUTS					
A	B	C	AB	AC	AB + AC	A	B + C	A (B + C)
0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	1	0
0	1	0	0	0	0	0	1	0
0	1	1	0	0	0	0	1	0
1	0	0	0	0	0	1	0	0
1	0	1	0	1	1	1	1	1
1	1	0	1	0	1	1	1	1
1	1	1	1	1	1	1	1	1

equal

The table shows the eight possible input combinations of the three variables. It also shows the outputs of the intermediate and output gates for both the sum-of-products and product-of-sums forms. And they are equal. This shows you another use of truth tables in analyzing and understanding logic circuits.

Another version of the Laws of Distribution is

$$(A + B)(A + C) = A + BC$$

Note the format of the original and simplified versions.

The original expression is in the _____ of _____ form but is changed to the _____ of _____ form when it is simplified.

71. (product-of-sums, sum-of-products) The logic diagrams of the two versions illustrated in Figure 5-50 show this difference.

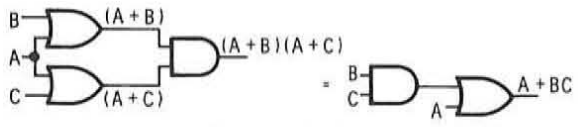
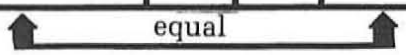


Figure 5-50

You can use truth tables to prove the equality of the two expressions or circuits. Do this now and check your results in the next frame.

72. (See table below)

INPUTS			GATE OUTPUTS					
A	B	C	(A + B)	(A + C)	(A + B) (A + C)	A	BC	A + BC
0	0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0
0	1	0	1	0	0	0	0	0
0	1	1	1	1	1	0	1	1
1	0	0	1	1	1	1	0	1
1	0	1	1	1	1	1	0	1
1	1	0	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1



Another way to prove the equality of these expressions is to use some of the Boolean rules learned earlier.

$$(A + B)(A + C) = A + BC$$

First expand the expression on the left side of the equation as you would any algebraic expression. Multiply each term by the others and sum the products as shown.

$$(A + B)(A + C) = AA + AC + AB + BC$$

Next, this can be reduced by substituting A for AA and factoring an A out of the first three terms.

$$A + AC + AB + BC = A(1 + C + B) + BC$$

Then, the Laws of Union will reduce (1 + C + B) to 1 and the expression becomes

$$A(1) + BC$$

Finally, the Laws of Intersection makes this

$$A + BC$$

Go to the next frame.

73. Next there are the Laws of Absorption. There are four versions.

$$A\,(A + B) = A$$
$$A\,(\overline{A} + B) = AB$$
$$AB + \overline{B} = A + \overline{B}$$
$$A\overline{B} + B = A + B$$

Now use the previously explained Boolean rules to prove the first expression

$$A\,(A + B) = A$$

74. (See procedure below) The related Boolean rule is indicated in parenthesis.

$A\,(A + B)$
Expand by multiplying (Distribution)

$AA + AB$
Replace AA by A (Tautology)

$A + AB$
Factor out A

$A\,(1 + B)$
Replace (1 + B) by 1 (Union)

$A\,(1)$
Replace A (1) by A (Intersection)

A
Next prove $A\,(\overline{A} + B) = AB$

75. (See procedure below)

$A(\overline{A} + B)$
Expand by multiplying (Distribution)

$A\overline{A} + AB$
Replace $A\overline{A}$ by 0 (Complements)

$0 + AB$
Replace $AB + 0$ with AB (Union)

AB

The other Laws of Absorption are more difficult to prove. You can use truth tables as we did before. But it can be done with Boolean Algebra by using a trick. Let's prove that

$$AB + \overline{B} = A + \overline{B}$$

There isn't anything we can do with the expression on the right side of the equation. So let's multiply the $\overline{B}$ term by $(A + 1)$. Since $A + 1 = 1$ and $\overline{B}(1) = \overline{B}$ we will not change the original meaning of the expression. It is equivalent to multiplying a term by 1. Therefore

$$AB + \overline{B} = AB + \overline{B}(A + 1)$$

Now, complete the proof yourself using the previously explained Boolean rules.

76. (See proof below) The related Boolean rules are indicated.

$AB + \overline{B}(A + 1)$
Expand by multiplying (Distribution)

$AB + A\overline{B} + \overline{B}$
Factor out from first two terms (Distribution)

$A(B + \overline{B}) + \overline{B}$
Replace $(B + \overline{B})$ with 1 (Complements)

$A(1) + \overline{B}$
Replace $A(1)$ by A (Intersection)
$A + \overline{B}$

You can use the same trick to prove the expression.

$$A\overline{B} + B = A + B$$

Do it for practice then check your solution in the next frame.

77. (See proof below)

$A\overline{B} + B$
Multiply B by (A + 1) (Distribution)

$A\overline{B} + B\,(A + 1)$
Expand by multiplying (Distribution)

$A\overline{B} + AB + B$
Factor A out of first two terms (Distribution)

$A\,(\overline{B} + B) + B$
Replace $(\overline{B} + B)$ by 1 (Complements)

$A\,(1) + B$
Replace A (1) by A (Intersection)

$A + B$

The equality of the expression $A\overline{B} + B = A + B$ can also be proven by using a _____ _____.

78. (truth table) Don't overlook truth tables as a means of verifying the operation of a logic circuit or in proving the equivalence of two equations or circuits.

Another important Boolean rule is DeMorgan's theorem. There are two forms of it as indicated below.

$$\overline{AB} = \overline{A} + \overline{B}$$
$$\overline{A + B} = \overline{A}\,\overline{B}$$

The best way to prove the equality of these expressions is by a truth table. The first expression above is proven this way as indicated below.

INPUTS		OUTPUTS				
A	B	$\overline{A}$	$\overline{B}$	AB	$\overline{A\,B}$	$\overline{A} + \overline{B}$
0	0	1	1	0	1	1
0	1	1	0	0	1	1
1	0	0	1	0	1	1
1	1	0	0	1	0	0

equal

There are two variables A and B so there are four possible input combinations. These are indicated in columns A and B. Columns are also provided for the other terms called for by the expressions

$$\overline{A}, \overline{B}, \overline{AB} \text{ and } \overline{A} + \overline{B}$$

Using the inputs as a guide these other columns are completed. Go through each column yourself to be sure you understand how each state is obtained. Note the equality of the $\overline{AB}$ and $\overline{A} + \overline{B}$ columns.

Now, prove the expression $\overline{A + B} = \overline{A}\,\overline{B}$ yourself using the same procedure. Check your results in the next frame.

79. (See Table below)

INPUTS		OUTPUTS				
A	B	$\overline{A}$	$\overline{B}$	A + B	$\overline{A + B}$	$\overline{A}\,\overline{B}$
0	0	1	1	0	1	1
0	1	1	0	1	0	0
1	0	0	1	1	0	0
1	1	0	0	1	0	0

equal

The correct proof of the expression $\overline{A + B} = \overline{A}\,\overline{B}$ is shown above.

Like other Boolean rules, DeMorgan's theorem is useful in minimizing logic equations, particularly those that have whole terms or expressions negated with a complement bar over them. For example, the expression

$$X = \overline{A\,\overline{B}\,C} + \overline{A + \overline{C}}$$

cannot be simplified by using the previously given Boolean rules. It can only be reduced by using DeMorgan's theorem.

If you look closely at the two forms of DeMorgan's theorems you will see that they essentially show how an AND expression can be changed to an OR expression and vice versa.

$$\overline{AB} = \overline{A} + \overline{B}$$
$$\overline{A + B} = \overline{A}\,\overline{B}$$

Logic expressions of either form can be readily converted to another form more desirable in simplifying the expression.

Like other Boolean rules, DeMorgan's theorem is used to _____ logic expressions.

80. (Simplify, minimize, or reduce) DeMorgan's theorem provides one more tool for you to use in minimizing certain types of logic expressions. In addition, it can be used to change the form of an expression for AND to OR or OR to AND.

The following procedure can be used in making the conversions.

To change a Boolean expression from one form to another, use the following procedure:

1. Change all AND (•) expressions to OR (+) expressions.
2. Complement the individual terms that were ANDed or ORed.
3. Complement the entire expression.

Let's try it out on the expression $\overline{AB}$.

1. Change AND to OR or vise versa.

$$\overline{AB} \text{ becomes } \overline{A + B}$$

2. Complement each term.

$$\overline{A + B} \text{ becomes } \overline{\overline{A} + \overline{B}}$$

3. Complement entire expression

$$\overline{\overline{A} + \overline{B}} \text{ becomes } \overline{\overline{\overline{A} + \overline{B}}} = \overline{A} + \overline{B}$$

The result $\overline{AB} = \overline{A} + \overline{B}$ is one of our DeMorgan's relationships. Now try converting the expression $\overline{A}\,\overline{B}$ using this procedure.

81. $(\overline{A}\,\overline{B} = \overline{A + B})$ (See procedure below)

1. $\overline{A}\,\overline{B}$ Change AND to OR $\overline{A} + \overline{B}$
2. $\overline{A} + \overline{B}$ Complement each term $\overline{\overline{A}} + \overline{\overline{B}} = A + B$
3. $A + B$ Complement entire expression $\overline{A + B}$

The procedure is easily remembered and can be applied to other more complex expressions. The examples below illustrate some typical applications.

$\overline{A\overline{B}}$ becomes

$\overline{A + \overline{B}}$ then

$\overline{\overline{A} + B}$ and finally

$\overline{\overline{A} + B} = \overline{A} + B = \overline{A\,\overline{B}}.$

Note that while only two terms are shown in the basic DeMorgan's theorems, the same rules apply to logic expressions with three or more terms.

$X + Y + Z$ becomes

$X \cdot Y \cdot Z$ then

$\overline{X}\,\overline{Y}\,\overline{Z}$ and finally

$\overline{\overline{X}\,\overline{Y}\,\overline{Z}} = X + Y + Z$

Use DeMorgan's rules to change the form of the expression:

$$\overline{\overline{J} + K + \overline{L}}$$

82. (J $\overline{K}$ L) You use the same procedure for converting any Boolean expression with DeMorgan's theorem.

The following example will show you how DeMorgan's theorems can significantly reduce a Boolean expression.

$\overline{(A\ \overline{B})\ (\overline{B}\ C)\ (C\ \overline{D})\ (A\ C)}$ Original expression

$\overline{(A\ \overline{B})} + \overline{(\overline{B}\ C)} + \overline{(C\ \overline{D})} + \overline{(A\ C)}$ Expanded by DeMorgan's

$(\overline{A} + B) + (B + \overline{C}) + (\overline{C} + D) + (\overline{A} + \overline{C})$ Each term in expression expanded by DeMorgan's

$\overline{A} + B + B + \overline{C} + \overline{C} + D + \overline{A} + \overline{C}$ Expression expanded by Law of Association

$\overline{A} + \overline{A} + B + B + \overline{C} + \overline{C} + \overline{C} + D$ Expression rearranged by Laws of Commutation.

$\overline{A} + B + \overline{C} + D$ Expression simplified by Laws of Union.

A significant simplification takes place. Note that DeMorgan's theorems were applied twice, once to the original expression and again to each term in the expanded form resulting from the first application. In simplifying an expression like this you use DeMorgan's theorem as many times as necessary for any terms to achieve the greatest minimization.

You do not need to use DeMorgan's theorem on all Boolean expressions. As a rule, the only place you will use it is when a NOT bar appears over all or part of the logic equation.

Now, take a close look at the first expression for DeMorgan's theorem.

$$\overline{A\ B} = \overline{A} + \overline{B}$$

What logic function is indicated by the term on the left? _____.

83. (NAND) This expression relates the positive NAND function ($\overline{AB}$) to the negated NOR or negative NOR function ($\overline{A} + \overline{B}$).

What about the other form of DeMorgan's $\overline{A + B} = \overline{A}\,\overline{B}$? Which logic function is indicated by $\overline{A + B}$? _____.

84. (NOR) Yes. The positive NOR function ($\overline{A + B}$) is indicated. It is equivalent to the negated NAND or negative NAND function $\overline{A}\,\overline{B}$. You saw earlier how NAND and NOR gates can perform NAND or NOR functions in positive or negative logic. These operations are clearly expressed by the two forms of DeMorgan's theorem. You will find DeMorgan's theorems useful in dealing with NAND and NOR gates.

Self Test Review

Reduce the following logic expressions:

8. $\overline{(ABC)} + \overline{(\overline{A}\,\overline{B}\,C)}$
9. $\overline{(A + \overline{B} + \overline{C})}\;\overline{(A + \overline{C})}$

Answers

8. $\overline{(A\,B\,\overline{C})} + \overline{(\overline{A}\,\overline{B}\,C)}$

   $\overline{A} + \overline{B} + C + A + B + \overline{C}$

   $A + \overline{A} + \overline{B} + B + C + \overline{C}$

   $1 \quad + \quad 1 \quad + \quad 1 \quad = \quad 1$

9. $\overline{(A + \overline{B} + \overline{C})}\;\overline{(A + \overline{C})}$

   $(\overline{A}\,B\,C)\;(\overline{A}\,C)$

   $\overline{A}\,\overline{A}\,B\,C\,C = \overline{A}\,B\,C$

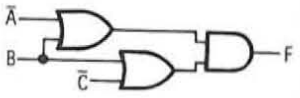
MINIMIZING LOGIC EXPRESSIONS

85. You have already seen how the Boolean rules are used to simplify logic expression and you have had a little practice in minimizing some simple logic equations yourself. But now we want you to polish your skill with Boolean so that you can deal with any practical logic function that you might encounter. The problems presented here will give you the necessary practice.

Let's start with the expression $F = (\overline{A} + B)(B + \overline{C})$

Draw the logic diagram for this expression.

86. (See Figure 5-51)



$F = (\overline{A} + B)(B + \overline{C})$

Figure 5-51

Now, using Boolean algebra, minimize the equation. The first step is to expand the expression by multiplying as you would in algebra.

$F = (\overline{A} + B)(B + \overline{C}) = \overline{A}\,B + \overline{A}\,\overline{C} + B\,B + B\,\overline{C}$

Basic Boolean rules can then be used as indicated below to reduce the equation.

$\overline{A}\,B + \overline{A}\,\overline{C} + B\,B + B\,\overline{C}$
Laws of Tautology

$\overline{A}\,B + \overline{A}\,\overline{C} + B + B\,\overline{C}$
Laws of Commutation

$\overline{A}B + B + B\overline{C} + \overline{A}\,\overline{C}$
Factor a B out of the first three terms

$B\,(\overline{A} + 1 + \overline{C}) + \overline{A}\,\overline{C}$
Laws of Union

$(\overline{A} + 1 + \overline{C}) = 1$

$B\,(1) + \overline{A}\,\overline{C}$
Laws of Intersection

$B + \overline{A}\,\overline{C}$

Now draw the logic diagram of the minimized version of the original expression.

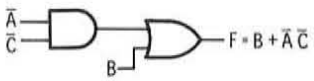


Figure 5-52

87. (See Figure 5-52)

As you can see, there is a significant simplification in that the minimized circuit uses one less gate.

Just to be sure that the two circuits and expressions do indeed produce the same logical function, prove their equality with a truth table.

Check your results in the next frame.

88. (See table below) The truth table proves conclusively that

$$F = (\overline{A} + B)(B + \overline{C}) = B + \overline{A}\,\overline{C}$$

the two expressions are equivalent.

INPUTS			GATE OUTPUTS						
A	B	C	$\overline{A}$	$\overline{C}$	$(\overline{A}+B)$	$(B+\overline{C})$	$(\overline{A}+B)(B+\overline{C})$	$\overline{A}\,\overline{C}$	$B+\overline{A}\,\overline{C}$
0	0	0	1	1	1	1	1	1	1
0	0	1	1	0	1	0	0	0	0
0	1	0	1	1	1	1	1	1	1
0	1	1	1	0	1	1	1	0	1
1	0	0	0	1	0	1	0	0	0
1	0	1	0	0	0	0	0	0	0
1	1	0	0	1	1	1	1	0	1
1	1	1	0	0	1	1	1	0	1

equal

Now let's try the expression below.

$$X = A\,\overline{B}\,\overline{C} + A\,B\,\overline{C} + A\,\overline{B}\,C + \overline{A}\,B\,\overline{C}$$

First draw the logic diagram.

89. (See Figure 5-53)

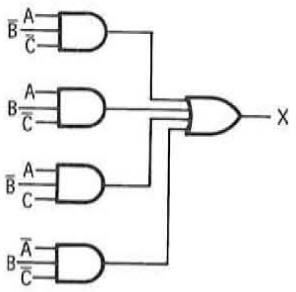


Figure 5-53

Observing the equation, try to spot common factors in each of the terms, then regroup the terms and rearrange the factors using the Laws of Commutation.

$X = A\,\overline{B}\,\overline{C} + A\,B\,\overline{C} + A\,\overline{B}\,C + \overline{A}\,B\,\overline{C}$
$X = A\,\overline{B}\,\overline{C} + A\,\overline{B}\,C + B\,\overline{C}\,A + B\,\overline{C}\,\overline{A}$

Next we factor out the common expressions, $A\overline{B}$ in the first two terms and $B\overline{C}$ in the last two terms.

$X = A\,\overline{B}\,(\overline{C} + C) + B\,\overline{C}\,(A + \overline{A})$

By the Laws of Complements this becomes:

$X = A\,\overline{B} + B\,\overline{C}.$

Draw the corresponding logic diagram.

90. (See Figure 5-54)

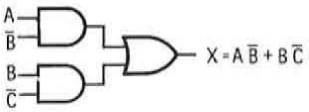


Figure 5-54

Comparing this circuit with the one in Figure 5-53 (Frame 89), you can see the result of minimization. The three gate circuit performs exactly the same logic function as the original five gate circuit at a considerable savings.

Next, let's minimize a logic equation with DeMorgan's theorem.

Reduce the equation

$$G = \overline{\overline{(A\,\overline{B}\,\overline{C} + B\,C)\,(A\,\overline{B})}}$$

Work the problem yourself keeping in mind that DeMorgan's theorem must be used several times to expand the equation into a form that will permit it to be minimized with the other Boolean rules.

Check the solution in the next frame.

91. The correct solution is shown below.

$G = \overline{(A\,\overline{B}\,\overline{C} + B\,C)\,(A\,\overline{B})}$
DeMorgan's

$G = \overline{(A\,\overline{B}\,\overline{C} + BC)} + \overline{(A\,\overline{B})}$
DeMorgan's

$G = \overline{A} + B + C + B\,C + \overline{A} + B$
Law of Commutation

$G = \overline{A} + \overline{A} + B + B + C + B\,C$
Law of Tautology

$G = \overline{A} + B + C + B\,C$
Law of Distribution

$G = \overline{A} + B + C\,(1 + B)$
Law of Union

$G = \overline{A} + B + C\,(1)$
Law of Intersection

$G = \overline{A} + B + C$

Self Test Review

Simplify the following logic equations using Boolean Algebra.

10. $X = A\,B\,\overline{C}\,D + A\,B\,C\,\overline{D} + B\,\overline{C}\,D + \overline{A}\,B\,C\,\overline{D}$
11. $F = (A + B + \overline{C})\,(\overline{A} + B + \overline{C})$
12. $X = \overline{A\,\overline{B}\,C} + \overline{A + \overline{C}}$
13. $M = \overline{(A + \overline{B})\,(\overline{A} + C)\,(B + C)}$
14. $D = \overline{A}\,B\,\overline{C} + \overline{A}\,B\,C + A\,B\,\overline{C} + A\,B\,C$

Answers

10. $X = A\,B\,\overline{C}\,D + A\,B\,C\,\overline{D} + B\,\overline{C}\,D + \overline{A}\,B\,C\,\overline{D}$

Rearrange order of terms (Law of Commutation)

$X = A\,B\,\overline{C}\,D + B\,\overline{C}\,D + A\,B\,C\,\overline{D} + \overline{A}\,B\,C\,\overline{D}$

Factor out $B\overline{C}D$ in first two terms and BCD in second two terms (Law of Distribution)

$X = B\,\overline{C}\,D\,(A + 1) + B\,C\,\overline{D}\,(A + \overline{A})$

Reduce first term by Law of Union and the second by Law of Complements

$X = B\,\overline{C}\,D\,(1) + B\,C\,\overline{D}\,(1)$

Reduce by Law of Intersection

$X = B\,\overline{C}\,D + B\,C\,\overline{D}$

Factor out B (Law of Distribution)

$X = B\,(\overline{C}\,D + C\,\overline{D})$

11. $F = (A + B + \overline{C})\,(\overline{A} + B + \overline{C})$

Expand by multiplying (Law of Distribution)

$A\,\overline{A} + A\,B + A\,\overline{C} + B\,\overline{A} + B\,B + B\,\overline{C} + \overline{C}\,\overline{A} + \overline{C}\,B + \overline{C}\,\overline{C}$

Minimize with Laws of Tautology and Complements.

$F = A\,B + A\,\overline{C} + B\,\overline{A} + B + B\,\overline{C} + \overline{C}\,\overline{A} + \overline{C}\,B + \overline{C}$

Rearrange terms (Law of Commutation)

$F = A\,\overline{C} + B\,\overline{C} + \overline{A}\,\overline{C} + \overline{C} + A\,B + \overline{A}\,B + B$

Factor out terms (Law of Distribution)

$F = \overline{C}\,(A + B + \overline{A} + 1) + B\,(A + \overline{A} + 1)$

Reduce by Law of Union

$F = \overline{C}\,(1) + B\,(1)$

Reduce by Law of Intersection and rearrange terms (Law of Commutation)

$F = B + \overline{C}$

Answers (Cont'd)

12. $X = \overline{A\,\overline{B}\,C} + \overline{A + \overline{C}}$

Expand with DeMorgan's theorem

$X = \overline{A} + B + \overline{C} + \overline{A}\,C$

Rearrange terms (Law of Commutation)

$X = \overline{A} + \overline{A}\,C + B + \overline{C}$

Factor out $\overline{A}$ (Law of Distribution)

$X = \overline{A}\,(1 + C) + B + \overline{C}$

Reduce by Law of Union

$X = \overline{A}\,(1) + B + \overline{C}$

Reduce by Law of Intersection

$X = \overline{A} + B + \overline{C}$

13. $M = \overline{(A + \overline{B})\,(\overline{A} + C)\,(B + C)}$

Expand with DeMorgan's

$M = \overline{(A + \overline{B})} + \overline{(\overline{A} + C)} + \overline{(B + C)}$

Again expand with DeMorgan's

$M = \overline{A}\,B + A\,\overline{C} + \overline{B}\,\overline{C}$

Note that all you have done here is to convert a product of sums expression to a sum of products expression. This is one valuable use of DeMorgan's theorem. You can change any expression from sum-of-products to product-of-sums or vice versa by applying DeMorgan's theorem.

Answers (Cont'd)

14. $D = \overline{A}\,B\,\overline{C} + \overline{A}\,B\,C + A\,B\,\overline{C} + A\,B\,C$

Law of Commutation

$D = \overline{A}\,B\,\overline{C} + A\,B\,\overline{C} + \overline{A}\,B\,C + A\,B\,C$

Factor out $B\overline{C}$ and BC

$D = B\,\overline{C}\,(\overline{A} + A) + B\,C\,(\overline{A} + A)$

Law of Complements

$D = B\,\overline{C}\,(1) + B\,C\,(1)$

Law of Intersection

$D = B\,\overline{C} + B\,C$

Factor out B

$D = B\,(\overline{C} + C)$

Law of Complements

$D = B(1)$

Law of Intersection

$D = B$

A and C have no effect on the output and no gates are needed to implement this relationship. D is connected directly to B.

USING NAND/NOR GATES

92. Throughout this unit we have shown logic equations implemented with AND and OR gates. However, most modern digital system's and circuits are made with NAND or NOR gates. As you saw in an earlier unit, any of the three basic logic operations can be realized with either NAND or NOR circuits.

The three basic logic functions are _____, _____, and _____.

93. (AND, OR, and NOT) A NAND gate or a NOR gate can be used as an inverter by tying all of the inputs together as shown in Figure 5-55.

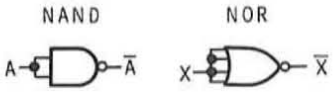


Figure 5-55

Both circuits produce an output that is the complement of the input.

When used as inverters NAND and NOR gates are represented by the proper symbol. Sketch this symbol.

94. (See Figure 5-56) These are the commonly used symbols for an inverter.

Figure 5-56

On schematic and logic diagrams, it is desirable to use a symbol that represents the logic function being performed despite the nature of the circuit used to implement it.

A NAND gate can be used for AND operations by inverting its output as shown in Figure 5-57.

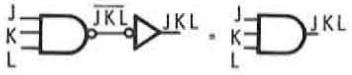


Figure 5-57

The inversion of the NAND is removed by the added inverter producing the pure AND function.

The inversion is indicated by the _____ in the inverter logic symbol.

95. (circle) The small circle associated with a logic symbol indicates the complement function.

A NAND can also perform the OR function as you saw in a previous unit. This is accomplished by inverting the inputs as shown in Figure 5-58.

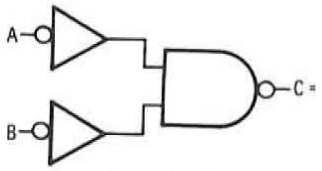


Figure 5-58

Write the output equation for this circuit. _____.

96. ($C = \overline{\overline{A}\,\overline{B}}$) Now using DeMorgan's theorems, reduce this expression.

$$C = \overline{\overline{A}\,\overline{B}} = \_\_\_\_\_$$

97. ($C = A + B$) Correct. When you invert the inputs on a NAND the OR function is performed.

DeMorgan's theorem tells us that a NAND can also perform the negated OR function.

$$\overline{A\,B} = \overline{A} + \overline{B}$$

When the NAND is used for the negated OR function the symbol in Figure 5-59 is used.

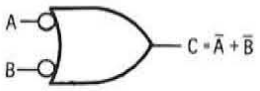


Figure 5-59

When this symbol is used, it is clear what function is being performed.

DeMorgan's theorem tells us that a positive NAND is also a _____ _____.

98. (negative or negated OR) Putting inverters ahead of the inputs creates the pure OR function as indicated in Figure 5-60.

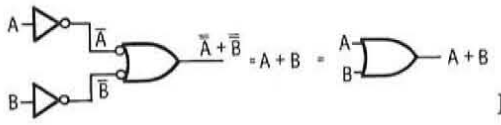


Figure 5-60

You should realize that the symbol used for the negated NOR shows circles or inverters at the inputs. In a true physical sense there are no inverters there, but the logic effect produced is as if there were.

In writing the Boolean equation from a logic diagram simply treat the symbol literally and interpret each circle as an inversion and each gate as the designated logic function.

Write the equation of the circuit in Figure 5-61.

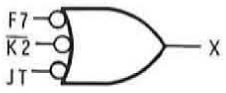


Figure 5-61

X = _____.

99. (X = $\overline{F7}$ + K2 + $\overline{JT}$) If you had drawn this circuit with the equivalent NAND symbol as indicated in Figure 5-62, you might expect a different logic operation to be performed.

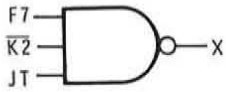


Figure 5-62

Write the equation for this circuit. X = _____.

100. (X = $\overline{F7 \cdot \overline{K2} \cdot JT}$) Use DeMorgan's theorem on this expression and you will get X = _____.

101. ($X = \overline{F7} + K2 + \overline{JT}$) This little exercise proves that a positive NAND is also a negated NOR.

The NOR gate can also be used to perform any logic function. By inverting its output the OR operation is performed as shown in Figure 5-63.

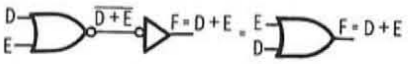


Figure 5-63

In an earlier unit you saw how the NOR could also be used to express the AND function. Sketch the logic symbols illustrating this.

102. (See Figure 5-64)

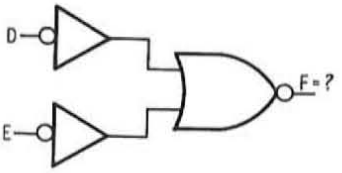


Figure 5-64

Write the output equation of this circuit. F = _____.

103. ($F = \overline{\overline{D} + \overline{E}}$) Now reduce it with DeMorgan's theorem. F = _____.

104. ($F = \overline{\overline{D} + \overline{E}} = D \cdot E$) This is of course the AND function.

DeMorgan's theorem tells us that the positive NOR can also perform as a _____ _____.

105. (negative or negated NAND) The DeMorgan's expression for this relationship is

$$\overline{D + E} = \overline{D} \cdot \overline{E}$$

When the negated NAND function is used the symbol in Figure 5-65 indicates the function.

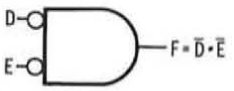


Figure 5-65

When a negated NAND is to be used for the AND equation, a (n) _____ must be connected ahead of each input.

106. (inverter) The positive NOR or negated NAND connected as an AND is shown in Figure 5-66 below.

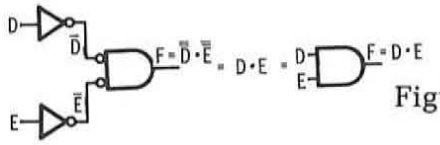
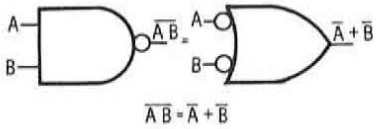


Figure 5-66

Interpret the negated NAND logic symbol literally for the purpose of writing equations, even though in reality no inverters are physically present at the inputs where circles are indicated.

Figure 5-67 summarizes the functions and symbols of NAND and NOR gates.



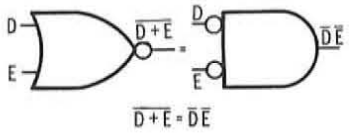


Figure 5-67

The AND and OR equivalent circuits with NANDs and NORs are summarized in Figure 5-68.

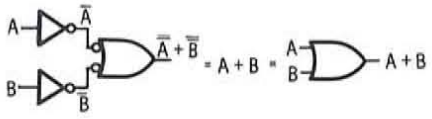
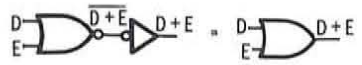


Figure 5-68



Now let's show how any Boolean equation can be implemented with NAND or NOR gates. Such logic circuits are generally known as _____ circuits.

107. (combinational) A combination circuit is any logic function implemented with gates.

Here is a straight forward procedure for implementing any Boolean expression with NAND or NOR gates.

1. Minimize the equation using Boolean algebra and DeMorgan's theorem.
2. Draw the logic circuit of the reduced equation using standard AND and OR symbols.
3. Select a type of logic gate either NAND or NOR.
4. Replace each AND or OR symbol with the circuit for the NAND or NOR equivalent of the specified logic function (see Figure 5-68).
5. Eliminate any redundancy in the NAND/NOR circuit.

Let's take several examples to illustrate this procedure. Go to the next frame.

108. Consider the equation $F = X + \overline{Y}\,Z$. Following the procedure given above we will arrive at an implementation for NAND or NOR gates.

1. The equation is already in its minimum form.
2. The circuit is shown in Figure 5-69.

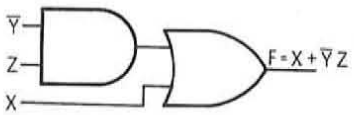


Figure 5-69

3. Let's use NAND gates.
4. The NAND circuit is given in Figure 5-70.

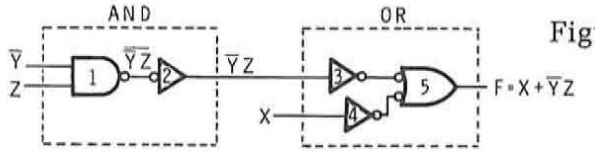


Figure 5-70

5. The redundancy in Figure 5-70 is the combination of inverters 2 and 3. Two cascaded inverters produces no logic inversion so they can be replaced by a direct connection as indicated in Figure 5-71.

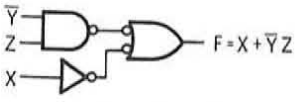
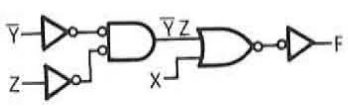


Figure 5-71

Using the same equation and procedure, develop the circuit implementation with NOR gates.



$F = X + \overline{Y}Z$

Figure 5-72

109. (See Figure 5-72) By comparing the circuits in Figure 5-71 and 5-72 you can conclude that the circuit using _____ gates is the most economical.

110. (NAND) When NAND gates are used to implement this function fewer logic elements are used so the circuit is more economical. It will be less expensive and will consume less power. There are fewer levels of logic (2) in the NAND circuit (4 in the NOR circuit) so its propagation delay will be less. Nevertheless, either circuit performs the same logic operation.

Once you become familiar with DeMorgan's theorem and its relationship with NAND/NOR gates, the procedure described here will come naturally to you. A little practice and experience will make you competent in dealing with modern NAND and NOR integrated circuits to implement logic functions. Keep in mind that your goal is to arrive at the minimum circuit for your application.

Self Test Review

15. Write the equation of circuit in Figure 5-73 and simplify with DeMorgan's theorem.

16. Implement the logic expression $F = C\,(A + \overline{B})$ with both NAND and NOR gates. Use the procedure described earlier.

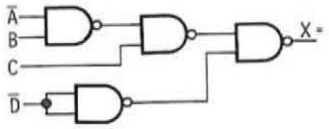


Figure 5-73

Answers

15. $X = \overline{\overline{(\overline{A}\ B)\ C\ D}}$

$X = \overline{\overline{(\overline{A}\ B)}\ C} + \overline{D}$

$X = (A + \overline{B})\ C + \overline{D}$

$X = A\ C + \overline{B}\ C + \overline{D}$

Note that the circuit of Figure 5-73 is drawn using all NAND symbols. By replacing these where appropriate with the symbols representing the actual function of each gate you can more quickly get a picture of the actual logic function. In addition, you could more quickly determine the output equation without DeMorgan's theorem. See Figure 5-74.

16. $F = C\,(A + \overline{B})$ See Figure 5-75.

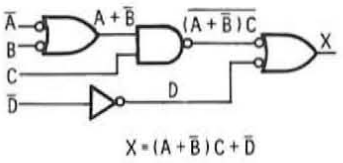


Figure 5-74

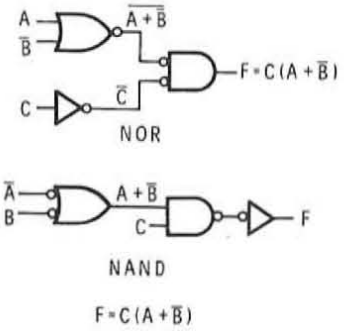


Figure 5-75

EXPERIMENT 7

APPLYING NAND AND NOR GATES

OBJECTIVES: To show how TTL and CMOS, NAND and NOR gates are used to implement any logic functions and to demonstrate the value of Boolean algebra in reducing logic circuits to their minimum configuration.

Materials Required

Heathkit Digital Design Experimenter (ET-3200)
1 — 7400 TTL IC (443-1)
1 — 7420 TTL IC (443-2)
1 — 7402 TTL IC (443-46)
1 — 4001 CMOS IC (443-695)

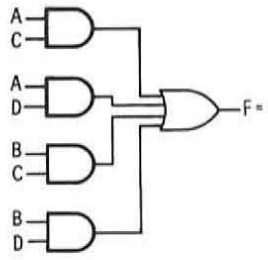


Figure 5-76

Procedure

1. Write the output expression of the circuit shown in Figure 5-76.
   F = AC + AD + BC + BD

2. Figure 5-77 shows the NAND gate implementation of the circuit in Figure 5-76. Wire the circuit shown in Figure 5-77. The pin connections for the 7400 and 7420 IC are given in Figure 5-78. Be sure to connect pin 14 to +5 volts and pin 7 to GND on each IC.

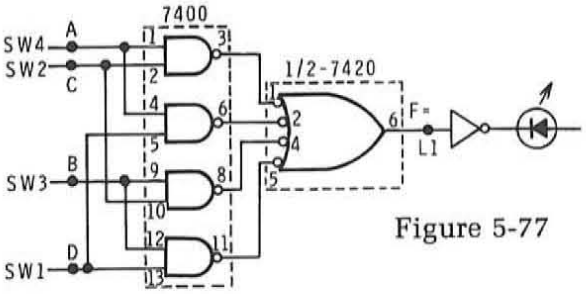


Figure 5-77

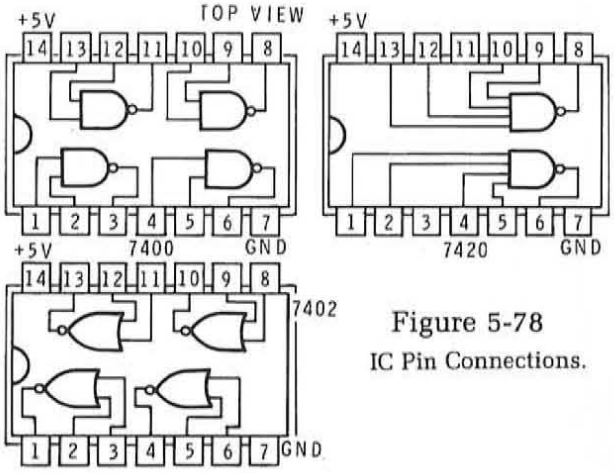


Figure 5-78
IC Pin Connections.

Note:

In Figure 5-77 and 5-79 we show a dashed line around the IC gate symbols. This represents the IC package. The number (7400, 7420, 7402, etc.) identifies the type of IC. Accompanying the IC designation number you will see 1/2, 3/4 or other fractions. This is a method of indicating how many of the gates in the IC are used. For example, in a 7400 IC there are 4 - 2 input NANDs. In Figure 5-77 we use all four of them. The 7420 IC contains two - 4 input gates. But in Figure 5-77 we use only one of them and we indicate this by the designation 1/2-7420. In Figure 5-79 we use three of the four NORs in the 7402 so the designation is 3/4-7402. This terminology will be used throughout the program.

3. Apply the inputs A, B, C and D in Table 1 to the circuit with data switches SW1 through SW4. Monitor the output on L1 and record the state for each set of inputs in the left-hand F column in Table I.

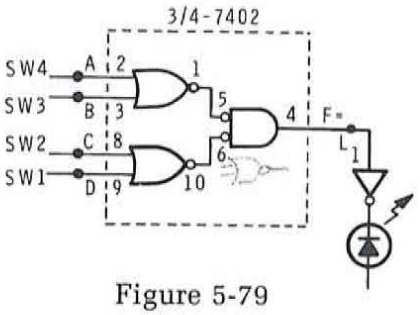


Figure 5-79

TABLE I

INPUTS				OUTPUTS	
A (SW4)	B (SW3)	C (SW2)	D (SW1)	F (LI) Fig. 5-77	F (LI) Fig. 5-79
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	0	0
0	1	0	1	1	1
0	1	1	0	1	1
0	1	1	1	1	1
1	0	0	0	0	0
1	0	0	1	1	1
1	0	1	0	1	1
1	0	1	1	1	1
1	1	0	0	0	0
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1

4. Using Boolean algebra, reduce the output equation obtained in Step 1. The minimized expression is:

   F = $(C+D)(A+B)$

5. Construct the circuit shown in Figure 5-79.
6. Write the output equation of the circuit in Figure 5-79. Compare it to the expression you derived in Step 4.

   F = $A+B(C+D)$

7. Apply the inputs shown in Table I and record the output state in the right-hand column.
8. Compare the two F output columns in Table I. What conclusion can you reach regarding the circuits in Figure 5-77 and 5-79?

Discussion

In this part of the experiment you demonstrated how TTL NAND and NOR gates are used to implement logic functions and how Boolean algebra is useful in minimizing the equation and the hardware.

Table III

INPUTS			OUTPUT
K	L	M	X
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

You next minimized the original expression by using Boolean algebra. Your reduction should appear like this.

$$X = \overline{L}\,[\overline{K}\,(K + L) + M]$$
$$X = \overline{L}\,(\overline{K}\,K + \overline{K}\,L + M)$$
$$X = \overline{L}\,\overline{K}\,K + \overline{L}\,\overline{K}\,L + \overline{L}\,M$$
$$X = \overline{L}\,M$$

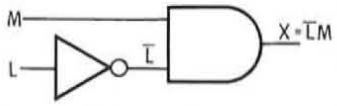


Figure 5-83

The logic circuit for this is shown in Figure 5-83. This reduced expression is readily implemented with a positive NOR gate as shown in Figure 5-84. The K input has absolutely no effect on the circuit as this reduced expression indicates. The reduced circuit will produce the same logic function as the original more complex circuit as your truth table should indicate.

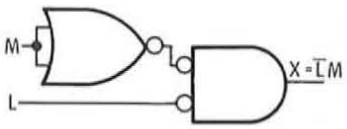


Figure 5-84

The important point to get from this exercise is that while the use of Boolean algebra accomplished a circuit minimization from 4 gates (Figure 5-82) to 2 gates (Figure 5-84), there is no real reduction in circuit size or power consumption. The type 4001 CMOS IC contains 4-2 input NOR gates. It can be used to implement the original circuit (Figure 5-82). It is also used to implement the reduced circuit (Figure 5-84). But only two gates are used. The unused gates could possibly be used elsewhere. If not they are wasted. Either circuit takes one IC package (the 4001) and there is no power reduction since even though two gates are unused they still consume power. This illustrates that with today's IC's, a Boolean reduction is not always helpful in reducing the expense or size of the equipment, with older discrete component circuits some clear cut reductions would normally take place.

Procedure (continued)

18. Write the truth table for a 3 input AND gate and sketch the appropriate logic symbol.
19. Show how to implement a three input AND gate with a quad 2 input NAND (7400). Draw the circuit, implement it on your Experimenter and verify its operation with a truth table.

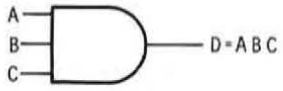


Figure 5-85

Discussion

The truth table for a three input AND gate is given in Table IV. The logic diagram is shown in Figure 5-85.

Table IV

INPUTS			OUTPUT
A	B	C	D
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

A three input AND gate implemented with a 7400 IC is shown in Figure 5-86. Inputs B and C are NANDed in gate 1. Gate 2 is connected as an inverter to produce BC. BC is then NANDed with A in gate 3 to produce A (BC). Gate 4, connected as an inverter, gives D = A (BC) which by the Law of Association is the same as D = A B C.

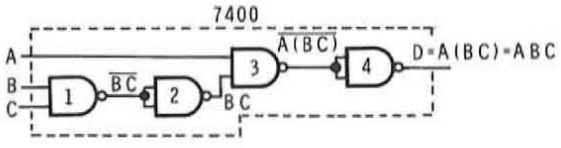


Figure 5-86

First we illustrated the desired logic circuit (Figure 5-76), and you wrote the output equation.

$$F = AC + AD + BC + BD$$

Then we illustrated how this circuit could be implemented with TTL NAND gates (Figure 5-77). It took four 2 input gates from the 7400 IC and one 4 input gate from the 7420, or two IC packages. Next you developed a truth table for this circuit.

In Step 4 you minimized the original equation with Boolean algebra. Your solution should look like this.

$$F = AC + AD + BC + BD$$

Factor out A, factor out B

$$F = A\,(C + D) + B\,(C + D)$$

Factor out (C + D)

$$F = (C + D)\,(A + B)$$

Then in Step 5 you constructed a circuit (Figure 5-79) made with a 7402 TTL NOR gate that implements the above reduced equation. Its output expression is $F = (A + B)(C + D)$. To verify its operation, you developed a truth table. By comparing the output results of the circuits in Figure 5-77 and 5-79 in Table I, you should find them identical. Obviously, the simpler circuit in Figure 5-79 is preferred because it will take up less space and will consume less power.

Procedure (continued)

In the following steps you will be given a Boolean equation to implement with CMOS NOR gates. You will implement the original expression and test it. Then you will minimize the expression and implement the reduced version. Finally, you will compare the logical operation of the two circuits.

9. Draw the AND and OR gate logic diagram of the expression

$$X = \overline{L}\,[\overline{K}\,(K+L) + M]$$

10. Redraw the circuit using positive NOR gates.
11. Implement your circuit in Step 10 with a 4001 CMOS quad two input NOR gate IC. The pin connections for the 4001 IC are given in Figure 5-80. Connect +5 volts to pin 14 and ground to pin 7.

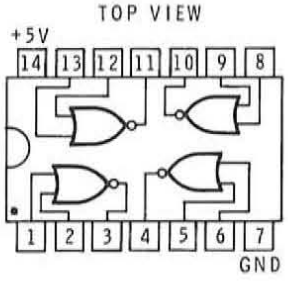


Figure 5-80
Pin Connections for 4001 CMOS IC.

12. Develop a truth table for the circuit. Use SW2, SW3 and SW4 to apply the K, L and M inputs. Monitor your output on L1. Record your output in the left hand X column of Table II.

TABLE II

INPUTS			OUTPUTS	
K (SW2)	L (SW3)	M (SW4)	X (Step 12)	X (Step 16)
0	0	0	1	
0	0	1	1	
0	1	0	0	
0	1	1	0	
1	0	0	1	
1	0	1	1	
1	1	0	0	
1	1	1	0	

13. Reduce the expression in Step 9 using Boolean algebra. The minimized equation is.

X = $\bar{L}M$

14. Draw the logic diagram of this circuit using AND and OR gates.
15. Implement the circuit developed in Step 14 with CMOS NOR gates.
16. Wire the minimized circuit and develop a truth table. Apply inputs K, L, and M with data switches SW2, SW3 and SW4. Monitor the output on L1. Use the right-hand X column in Table II to record your data.
17. Compare the two X output columns in Table II. What conclusions can you draw? What circuit minimization was really accomplished?

Discussion

Your logic diagram for the original expression in Step 9 should appear as in Figure 5-81. Redrawing the circuit using positive NOR gates should have given you the circuit in Figure 5-82. Your truth table should appear as in Table III.

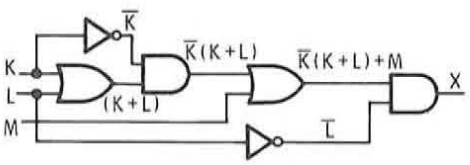


Figure 5-81

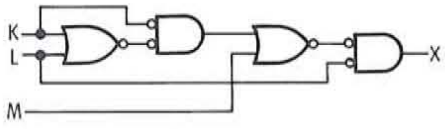


Figure 5-82

EXPERIMENT 8

THE WIRED OR CONNECTION

OBJECTIVE: To investigate the wired-OR connection of logic gates, to determine their logical function and to demonstrate their application.

Introduction

With some types of logic gates it is possible to connect their outputs directly together to perform certain logic operations. Figure 5-87 shows two NAND gates connected this way. This connection causes the gate outputs to be effectively ORed together. The OR and NOR functions can be achieved in some applications by simply tying gate outputs together like this. No additional circuitry is needed.

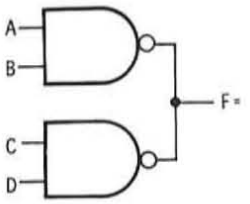


Figure 5-87

Logic gates with shunt output transistors and either internal collector pull resistors or open collector outputs can be wired ORed. Typical gates that can be connected this way are RTL, DTL, open collector TTL and ECL. Logic circuits using active pull up devices such as in standard TTL and CMOS gates cannot be wired ORed.

When gate outputs are connected together, the output transistors in the gates are connected in parallel as shown in Figure 5-88A. Any internal pull-up resistors are also paralleled. With open collector circuits, a single external pull-up resistor is used as shown in Figure 5-88B. When either one or both of the shunt output transistors is conducting, the output will be low.

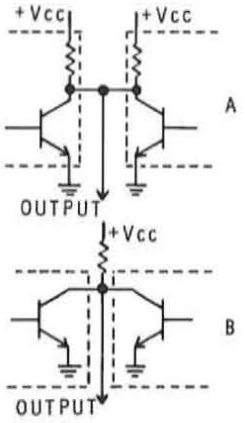


Figure 5-88

In this experiment, you are going to investigate the effect of wired OR connection with open collector TTL gates.

Materials Needed

Heathkit Digital Design Experimenter (ET-3200)

1 — 7403 TTL IC (443-54)

1 — 1 K ohm ½ watt resistor

Procedure

1. Connect the circuit shown in Figure 5-89. Mount the 7403 IC on the breadboarding socket and make the indicated connections. The pin connections for the 7403 are shown in Figure 5-90. Connect +5 volts to pin 14 and the 1 K resistor. Connect pin 7 to GND. The inputs A and B will come from data switches SW1 and SW2 while the output will be displayed on LED indicator L1.
2. Apply the inputs indicated in Table I and record the corresponding output in column C. Use positive logic.

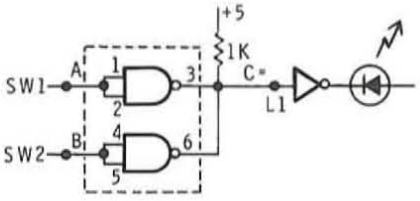


Figure 5-89

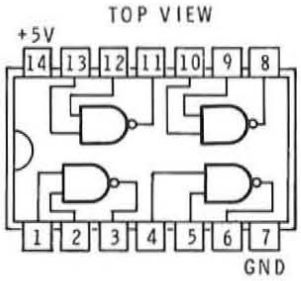


Figure 5-90 Pin connections for 7403 integrated circuit.

Table I

INPUTS		OUTPUT
A (SW1)	B (SW2)	C (L1)
0	0	1
0	1	0
1	0	0
1	1	0

3. Study your results in Table I. What logic function is being performed? Logic function _____.
4. Write the output expression of this circuit from the truth table using the procedure described in this Unit and use DeMorgan's theorem to change its form. C = _____ = _____.
5. Wire the circuit shown in Figure 5-91.
6. Apply the inputs A, B and C from data switches SW1, SW2 and SW3 as indicated in Table II. Record the output state registered by L1 in column F.

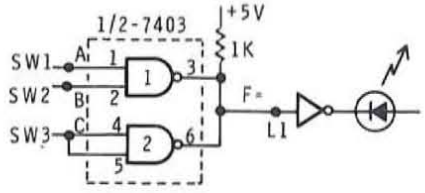


Figure 5-91

Table II

INPUTS			OUTPUT
A (SW1)	B (SW2)	C (SW3)	F (L1)
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

7. From the data in Table II, write the Boolean expression for the output F. F = _____.
8. Using Boolean algebra including DeMorgan's, reduce the equation to its simplest form. F = _____.
9. Draw the equivalent logic diagram of the expression F you derived in Step 8 using AND gates, OR gates and inverters.
10. Based on your knowledge of the wired OR circuit now, write the output expression for the circuit in Figure 5-92. X = _____.

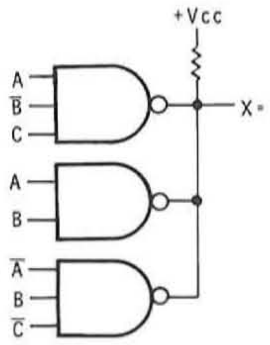


Figure 5-92

Discussion

In Step 1 you connected two of the gates in the 7403 as inverters with their outputs connected in parallel. In Step 2 you plotted a truth table for the circuit to see how it works. Then by studying the truth table you should have concluded that the circuit performs the NOR function since the output is 0 if either one or both of the inputs is 1. The output equation then is $C = \overline{A + B}$.

In Step 4 you wrote the output equation from the truth table. Here you create a product (AND) of the two input variables for each occurance of a binary 1 output. The input terms will be the complement if they are 0s. The only binary 1 output occurs when A is 0 and B is 0. Therefore the output expression is $C = \overline{A}\,\overline{B}$. Knowing DeMorgan's theorem you should see that $C = \overline{A}\,\overline{B} = \overline{A + B}$. This checks with your results in Step 3.

To get further verification of the wired OR connection, you investigated the circuit in Figure 5-91. You developed a truth table in Step 6. Next you wrote the output expression F from the truth table.

$$F = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,B\,\overline{C} + A\,\overline{B}\,\overline{C}$$

Next in Step 8, you reduced this expression with Boolean algebra. Your reduction should be like this:

$F = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,B\,\overline{C} + A\,\overline{B}\,\overline{C}$

Factor out $\overline{A}\,\overline{C}$

$F = \overline{A}\,\overline{C}\,(\overline{B} + B) + A\,\overline{B}\,\overline{C}$

Law of Complements

$F = \overline{A}\,\overline{C}\,(1) + A\,\overline{B}\,\overline{C}$

Law of Intersection

$F = \overline{A}\,\overline{C} + A\,\overline{B}\,\overline{C}$

Factor out $\overline{C}$

$F = \overline{C}\,(\overline{A} + A\,\overline{B})$

Law of Absorption

$F = \overline{C}\,(\overline{A} + \overline{B})$

DeMorgan's

$F = \overline{C}\,(\overline{A\,B})$

DeMorgan's

$F = \overline{C + A\,B}$ or $\overline{A\,B + C}$

NOTE:
$\overline{A} + A\,\overline{B} = \overline{A} + \overline{B}$
by the Laws of Absorption

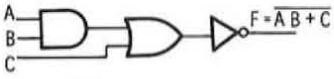


Figure 5-93

In Step 9 you drew the equivalent circuit. It should appear as shown in Figure 5-93. Equating this equivalent circuit to the original in Figure 5-91 you can see that gate 1 performs the AND operation while the common collector connection performs the OR or NOR function.

Based on your knowledge of the wired OR circuit, you should have found the expression of the circuit in Figure 5-92 to be

$$X = \overline{A\,\overline{B}\,C + A\,B + \overline{A}\,B\,\overline{C}}$$

EXAMINATION

UNIT 5

BOOLEAN ALGEBRA

The purpose of this exam is to help you review the key facts in this unit. The problems are designed to test your retention and understanding by making you apply what you have learned. This exam is not so much a test as it is another learning method. Be fair to yourself and work every problem first before checking the answers.

1. Which of the following is **not** a use for Boolean algebra?
   A. Analyze logic circuits.
   B. Solve binary number problems in logic circuits.
   C. Design logic circuits.
   D. Minimize logic circuits.
2. The Boolean equation for the circuit in Figure 5-94 is
   A. $X = (A + B)(\overline{C})(A + D)$
   B. $X = \overline{A\,B} + C + A\,D$
   C. $X = \overline{A\,B + \overline{C} + A\,D}$
   D. $X = A\,B + \overline{C} + A\,D$

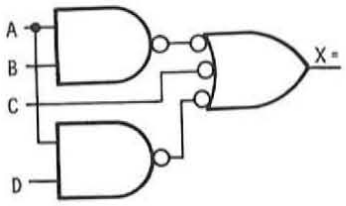


Figure 5-94

3. Using AND gates, OR gates and inverters, draw the circuit for the Boolean expression $F = (J + K)\,L + \overline{N}$.
4. The Boolean equation represented by the truth table below is:
   A. $X = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,B\,\overline{C} + \overline{A}\,B\,C + A\,B\,\overline{C} + A\,B\,C$
   B. $X = C + A + A\,C$
   C. $X = \overline{A}\,\overline{B}\,C + A\,\overline{B}\,\overline{C} + A\,\overline{B}\,C$
   D. $X = (\overline{A} + \overline{B} + C)(A + \overline{B} + \overline{C})(A + \overline{B} + C)$

INPUTS			OUTPUT
A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

5. The output of a combinational logic circuit is an OR gate. The Boolean equation then is in the form of a
   A. sum-of-products.
   B. product-of-sums.
   C. logical product or sum.
   D. product-of-products.
6. When minimized by Boolean algebra the expression $F = A\,\overline{B}\,C + \overline{A}\,B + \overline{B}\,C + \overline{B}\,\overline{C}$ becomes
   A. $F = \overline{B}\,C + \overline{A}\,B + \overline{B}\,\overline{C}$
   B. $F = B + A\,\overline{B}$
   C. $F = \overline{A} + \overline{B}$
   D. $F = \overline{B} + \overline{A}\,B$
7. Which of the following is **not** a form of DeMorgan's theorem?
   A. $A + B = \overline{A}\,\overline{B}$
   B. $\overline{A + B} = \overline{A}\,\overline{B}$
   C. $\overline{A\,B} = \overline{A} + \overline{B}$
   D. $\overline{A}\,\overline{B}\,\overline{C} = \overline{A\,B\,C}$
8. Which of the following IC logic circuits cannot be wire ORed?
   A. ECL
   B. CMOS
   C. open collector TTL
   D. DTL
9. Using Boolean algebra and DeMorgan's theorem, the expression $X = \overline{\overline{A}\,B + A\,\overline{B}}$ can be changed to
   A. $X = (\overline{A}\,B)\,(A\,\overline{B})$
   B. $X = (A + B)\,(\overline{A} + \overline{B})$
   C. $X = A\,B + \overline{A}\,\overline{B}$
   D. $X = \overline{A\,B} + \overline{\overline{A}\,\overline{B}}$
10. Design a logic circuit to implement the truth table below. Write the equation from the truth table, minimize it with Boolean Algebra, and sketch how the circuit would be implemented with both positive NOR gates and positive NAND gates.

INPUTS			OUTPUT
A	B	C	D
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

11. Using a truth table, show that $\overline{A}\,\overline{B} + A\,\overline{B} + AB = \overline{\overline{A}\,B}$.
12. The expression $M = \overline{A\,\overline{B}\,C} + \overline{A} + B\,\overline{C}$ when reduced by Boolean Algebra and DeMorgan's theorem to its minimum form becomes:
    A. $M = \overline{A} + B + \overline{C}$
    B. $M = \overline{A} + B + \overline{C} + B\overline{C}$
    C. $M = A\,(\overline{B}C + B\overline{C})$
    D. $M = A\,\overline{B}\,C$

ANSWERS

UNIT 5

BOOLEAN ALGEBRA

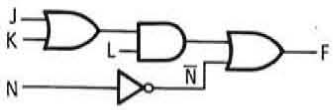


Figure 5-95

1. B — Boolean algebra is **not** used to solve binary number problems.
2. D — $X = AB + \overline{C} + AD$
3. See Figure 5-95
4. C — $X = \overline{A}\,\overline{B}\,C + A\,\overline{B}\,\overline{C} + A\,\overline{B}\,C$
5. A — Sum-of-products
6. C — $F = \overline{A} + \overline{B}$

   $F = A\,\overline{B}\,C + \overline{A}\,B + \overline{B}\,C + \overline{B}\,\overline{C}$

   Law of Commutation

   $F = A\,\overline{B}\,C + \overline{B}\,C + \overline{A}\,B + \overline{B}\,\overline{C}$

   Factor out $\overline{B}\,C$

   $F = \overline{B}\,C\,(A + 1) + \overline{A}\,B + \overline{B}\,\overline{C}$

   Law of Union

   $F = \overline{B}C\,(1) + \overline{A}\,B + \overline{B}\,\overline{C}$

   Laws of Intersection and Commutation

   $F = \overline{B}\,C + \overline{B}\,\overline{C} + \overline{A}\,B$

   Factor out $\overline{B}$

   $F = \overline{B}\,(C + \overline{C}) + \overline{A}\,B$

   Law of Complements

   $F = \overline{B}\,(1) + \overline{A}\,B$

   Law of Intersection

   $F = \overline{B} + \overline{A}\,B$

   Laws of absorption and commutation

   $F = \overline{A} + \overline{B}$
7. D — $\overline{A\,B\,C}$ does not equal $\overline{A\,B\,C}$.
8. B — CMOS logic gates cannot be wire ORed.
9. C — $X = A\,B + \overline{A}\,\overline{B}$

$X = \overline{\overline{A}\,B + A\,\overline{B}}$

DeMorgan's

$X = (\overline{\overline{A}B})\ (\overline{A\,\overline{B}})$

DeMorgan's

$X = (A + \overline{B})\ (\overline{A} + B)$

Expand by multiplying

$X = A\,\overline{A} + A\,B + \overline{A}\,\overline{B} + B\,\overline{B}$

Law of Complements

$X = 0 + A\,B + \overline{A}\,\overline{B} + 0$

Law of Union

$X = A\,B + \overline{A}\,\overline{B}$

10. The equation from the truth table is:

$$D = \overline{A}\,\overline{B}\,C + A\,\overline{B}\,C + A\,B\,\overline{C} + A\,B\,C$$

Reduced by Boolean algebra it becomes:

$D = \overline{A}\,\overline{B}\,C + A\,\overline{B}\,C + A\,B\,\overline{C} + A\,B\,C$

Factor out $\overline{B}\,C$ and $A\,B$

$D = \overline{B}\,C\,(\overline{A} + A) + A\,B\,(\overline{C} + C)$

Law of Complements

$D = \overline{B}\,C\,(1) + A\,B\,(1)$

Laws of Intersection and Commutation

$D = A\,B + \overline{B}\,C$

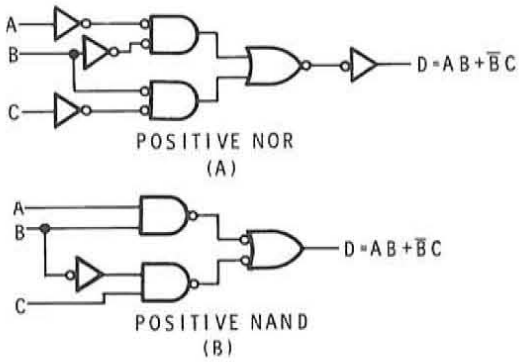


Figure 5-96

The circuit implemented with positive NOR gates is shown in Figure 5-96A. The same logic function implemented with positive NAND gates is shown in Figure 5-96B.

11.

A	B	$\overline{A}$	$\overline{B}$	$\overline{A}\,\overline{B}$	$A\overline{B}$	AB	$\overline{A}\,\overline{B} + A\overline{B} + AB$	$\overline{A}B$	$\overline{\overline{A}B}$
0	0	1	1	1	0	0	1	0	1
0	1	1	0	0	0	0	0	1	0
1	0	0	1	0	1	0	1	0	1
1	1	0	0	0	0	1	1	0	1

equal

12. A — $M = \overline{A} + B + \overline{C}$

$M = \overline{A\,\overline{B}\,C} + \overline{A} + B\,\overline{C}$

DeMorgan's

$M = \overline{A} + B + \overline{C} + \overline{A} + B\,\overline{C}$

Laws of Commutation and Tautology

$M = \overline{A} + B + \overline{C} + B\,\overline{C}$

Factor out $\overline{C}$

$M = \overline{A} + B + \overline{C}\,(1 + B)$

Law of Union

$M = \overline{A} + B + \overline{C}\,(1)$

Law of Intersection

$M = \overline{A} + B + \overline{C}$

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UNIT 6

FLIP-FLOPS AND REGISTERS

CONTENTS

UNIT 6
FLIP-FLOPS AND REGISTERS

INTRODUCTION

In this unit you are going to learn about flip-flops. A flip-flop is a digital logic element used for storing one bit of binary data. It has two stable states, one representing a binary 1 and the other a binary 0.

The flip-flop is the basic logic element used in sequential logic circuits. The primary characteristic of a sequential circuit is memory. Such circuits are used for a variety of storage, counting, sequencing and timing operations.

A major use of the flip-flop is in storage registers where a multibit binary word is stored. A register is made up of a number of flip-flops, each storing one bit of the number.

Read the Unit Objectives to see what you will learn, then follow the directions in the Unit Activity Guide. Be sure to record your time for each step.

UNIT OBJECTIVES

When you complete this unit you will have the following skills, knowledge and capabilities:

1. You will be able to write a definition for a flip-flop.
2. You will be able to name the three basic types of flip-flops.
3. Given a logic diagram, you will be able to identify each of the three types of flip-flops from their symbols or logic gate connections.
4. You will be able to draw the symbols and detailed logic diagrams of the RS, D and JK flip-flops.
5. Given a truth table of the RS, D or JK flip-flops, showing all possible input conditions, you will be able to fill in the appropriate output states for each.

6. Given a set of input waveforms for the RS, D or JK flip-flop, you will be able to draw the corresponding output waveforms.
7. You will be able to give a practical application for each of the three types of flip-flops.
8. You will be able to write a definition for a register.
9. Given a register made with any type of flip-flop, you will be able to measure the output states and determine the binary number stored there.

UNIT ACTIVITY GUIDE

	Completion Time
☐ Play audio record 5, side 2 "Flip-Flops and Registers"	_____
☐ Read section "Flip-Flops"	_____
☐ Answer Self Test Review questions 1—11	_____
☐ Perform Experiment 9 on "Set-Reset Flip-Flops"	_____
☐ Read section "D Type Flip-Flops and Registers"	_____
☐ Answer Self Test Review questions 12—16	_____
☐ Perform Experiment 10 "D Type Flip-Flops and Registers"	_____
☐ Read section "JK Flip-Flops"	_____
☐ Answer Self Test Review questions 17—27.	_____
☐ Perform Experiment 11 "JK Flip-Flops"	_____
☐ Take Unit Examination	_____

UNIT 6

FLIP-FLOPS

1. A flip-flop is a digital logic circuit whose basic function is memory or storage. A flip-flop is capable of storing a single bit of binary data. It can assume either of two stable states, one representing a binary 1 and the other a binary 0. If the flip-flop is put into one of its two stable states, it will remain there as long as power is applied or until it is changed.

   A flip-flop is used to store binary data.

2. (remember, memorize, or store) A flip-flop remembers to which state it was previously set. It effectively memorizes the data we give it. We give it this data by applying appropriate logic inputs to it. To determine the value of the bit stored in the flip-flop, we look at its outputs.

   How many bits of binary data can a single flip-flop store? _____.

3. (one) The flip-flop has two states, one used to represent a binary 1, the other a binary 0.

   There are three basic types of flip-flops: the latch, the D type, and the JK. Let's start with the simplest, the latch. The latch or set-reset flip-flop is the simplest form of binary storage element. The symbol shown in Figure 6-1 is used to represent this type of flip-flop.

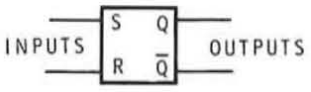


Figure 6-1

   The flip-flop has two inputs, S and R, and two outputs Q and $\overline{Q}$. Applying the appropriate logic signal to either the S or R input will put the latch into one state or the other. The S input is used to *set* the flip-flop. When a flip-flop is set, it is said to be storing a binary 1. The R input is used to reset the flip-flop. A reset flip-flop is said to be storing a binary 0.

   A latch is storing a binary 1. Therefore it is in the set state.

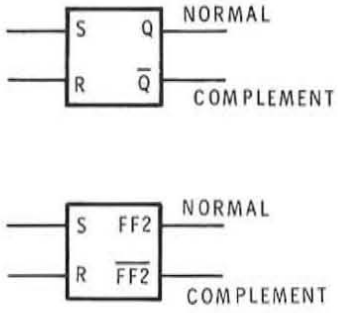


Figure 6-2

4. (set) If a latch is set it is storing a binary 1. If it is reset it is storing a binary 0. The latch, also called a set-reset or RS flip-flop, is put into one state or the other by applying a logic signal to either the S or R input.

As for knowing which state the flip-flop is in, we look at the outputs. The latch has two outputs labeled Q and $\overline{Q}$. These are called the *normal* and *complement* outputs respectively. As in other logic circuits, any letter or alphanumeric mnemonic can be used to designate logic signals. See Figure 6-2.

For example, the designation FF2 (meaning flip-flop number 2) could be used as shown.

To tell what state the flip-flop is in, you look at the *normal* output. The logic level present there tells you which bit, 0 or 1, is being stored.

For example, suppose that you measure the voltage at the normal output of a flip-flop with a voltmeter and find it to be the level normally associated with a binary 0. You know immediately then that the flip-flop is storing a binary ____0____.

5. (binary 0) Yes. If the normal output is a binary 0 level then the flip-flop is reset or storing a binary 0. The normal output always tells the state of the flip-flop. At the same time, the complement output has the state opposite that of the normal output.

If a flip-flop is reset, its complement output is binary ____1____.

6. (binary 1) Correct. If a flip-flop is reset, its normal output is a binary 0. The complement is a binary 1. The complement output is just as useful in determining the output state of the flip-flop as long as you remember the above relationship. The simple table below sums up the whole thing.

	OUTPUTS	
FLIP-FLOP STATE	Q	$\overline{Q}$
SET	1	0
RESET	0	1

This relationship is true for the latch and all other types of flip-flops.

A latch is readily constructed with logic gates as shown in Figure 6-3. Here two NAND gates are wired back-to-back so that the output of one feeds the input to the other.

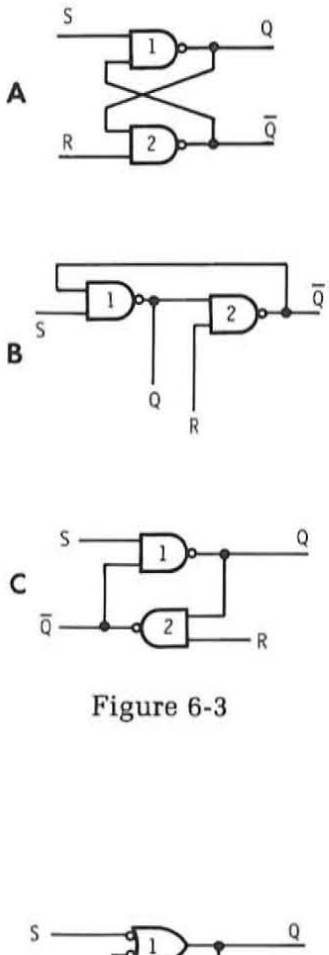


Figure 6-3

Three methods of drawing the latch are illustrated in Figure 6-3. They are all electrically the same, but the version in Figure 6-3A is the most widely used. The other versions are used occasionally so it is a good idea to be familiar with the various configurations so that you will recognize them on a logic diagram when you see them.

The latch is also sometimes drawn using the negative logic NOR symbols. Sketch the latch in its most popular configuration using this symbol.

7. (See Figure 6-4)

Either the NAND or NOR logic symbols can be used to illustrate a latch, but the operation of the circuit is a function of how a positive NAND/negative NOR gate works.

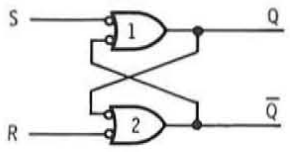


Figure 6-4

Let's see how much you remember about this circuit.

If both inputs to a 2 input TTL NAND gate are binary 1, the output will be 0.

8. (binary 0 or low) In order for the output to go low, both (all) inputs must be binary 1 or high. Otherwise, any other combination of inputs will produce a binary 1 (high) output. If both inputs are open, the output will also go low. For that reason, an open input has the same effect on the gate as a _____ input.

9. (binary 1 or high) The operation of the NAND gate is summarized by the truth table below.

INPUTS		OUTPUT
A	B	C
low	low	high
low	high	high
high	low	high
high	high	low

High usually refers to the most positive logic voltage level while low refers to the least positive logic level.

Observing the truth table above, what input state (high or low) seems to have the most predominant affect on the state of the output? Specifically, which input state produces the greatest number of common output states? _____.

10. (low) Good thinking! A look at the NAND gate truth table shows that of the four output states, three of them are high. The high output state is created by one or more low inputs. For that reason, we say that the predominant input state is a low or binary 0 for this type of gate. Now, let's consider the operation of the latch. Refer to Figure 6-5.

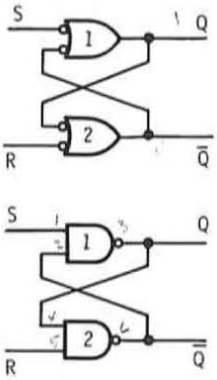


Figure 6-5

If the S and R inputs are both binary 1 (or open), which is the normal condition for this type of latch, the circuit is simply storing a bit put there by an earlier manipulation of the inputs. For example, if the flip-flop is set, the normal (Q) output from gate 1 (the set gate) will be high (binary 1). This output is fed back around to the upper input on gate 2 (the reset gate). The lower input to gate 2 is a binary 1 (or open) so its output $\overline{Q}$ is low. The output from gate 2 is fed to the lower input of gate 1. This input holds the Q output high. You can see now why they call this circuit a latch. Because of this feedback arrangement, the flip-flop is latched into this state. It will stay this way until you change it. And the way you change it is by applying a low level to either the set or reset inputs.

If the latch is set and a low level is applied to the R input (S remains high), the $\overline{Q}$ output will become _____.

11. (high or binary 1) Right. If we apply a low to the R input of the latch, it will reset. The low level on the R input will force the output of gate 2 high. This will cause both inputs to gate 1 to be high so its output will be low or binary 0 thereby indicating the reset state.

Assume that the latch is set. A low input is applied to the S input. What will happen?

A. The flip-flop will change states.
B. Nothing will happen.
C. The flip-flop will reset.

12. (B. Nothing will happen) If the flip-flop is set, applying a low to the S input will not do anything. The low level from the $\overline{Q}$ output fed back to the set gate keeps the Q output high. In the same way, applying a low level to the R input while the latch is reset will not produce a state change.

So, summing it all up we can say that to set the latch you must apply a binary 0 to the S input. To reset it you must apply a binary 0 to the R input. The waveform timing diagrams in Figure 6-6 shows the effect of various inputs on the outputs.

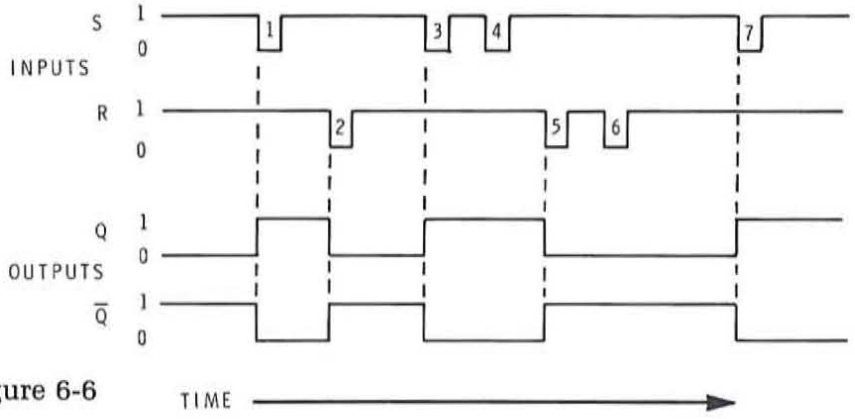


Figure 6-6

Go through these waveforms from left to right observing the effect of each input pulse on the outputs.

Looking at the waveforms above, what state is the flip-flop in *prior* to the application of pulse 1? _____.

13. (reset) Yes. Since the Q output is low and the $\overline{Q}$ output is high, before the occurrence of (to the left of) pulse 1, the latch is in the reset state storing a binary 0. Now look at these waveforms again.

When pulse 1 occurs on the S input, the latch sets with the outputs going to their proper levels. Pulse 2 comes along next on the R input so the latch resets. Pulse 3 again sets the flip-flop. Note that pulse 4 also occurs on the S input. Since the flip-flop is already set naturally nothing will happen. Pulse 5 then resets the latch. Pulse 6, also occuring on the R input, has no affect on the state of the latch. Finally, pulse 7 again sets the latch.

When the state of the latch is not being changed, the normal state of the inputs is binary _____.

14. (binary 1) Both inputs should normally be high on a NAND gate latch unless you are changing its state. The high inputs do not disturb the state of the latch so either a binary 1 or binary 0 may be stored there. Short duration input pulses that switch from high to low should be used when the latch is to be set or reset.

Now look at the latch circuit in Figure 6-7.

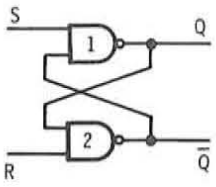


Figure 6-7

What happens if both inputs go low at the same time?

A. The latch becomes set.
B. The latch becomes reset.
C. The state of the latch cannot be determined.

15. (C. The state of the latch cannot be determined.) With both S and R inputs low, the Q and $\overline{Q}$ outputs will *both* be high. No longer are the outputs complementary, therefore, we really don't know what state the flip-flop is in. It is in some ambiguous state and is neither set or reset. This condition is one of the peculiarities of a latch. When you are using it you have to be careful to avoid simultaneous low inputs on the S and R terminals. This ambiguous state is generally undesirable because it can produce undesirable operation of a logic circuit if it is not avoided or accounted for. The ambiguous condition actually represents a third state in which the latch can exist. This state is sometimes referred to as the "limbo" state.

One way to avoid this condition is to modify the latch as shown in Figure 6-8.

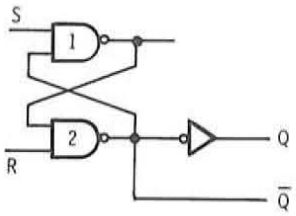


Figure 6-8

The normal and complement outputs are both derived from gate 2. The inverter ensures that the outputs are always complementary even if both inputs do go low simultaneously.

What happens if both inputs are high?

A. The flip-flop will be in the ambiguous state.
B. Nothing, this is the normal state of the inputs.
C. The state of the flip-flop will reverse.

16. (B. Nothing, this is the normal state of the inputs). Unless the latch is being set or reset, both inputs should be high (or open).

The operation of a NAND gate latch can be summarized by the truth table below.

INPUTS		OUTPUTS		STATE
S	R	Q	$\overline{Q}$	
0	0	1	1	Limbo
0	1	1	0	Set
1	0	0	1	Reset
1	1	X	$\overline{X}$	Either set or reset

The truth table accounts for all possible input and output states. Note that when both S and R inputs are binary 1, the output state of the flip-flop is designated X, where X can be either a 0 or a 1 as determined by previous input conditions.

If the flip-flop is set, you know that the last low input level was applied to the _____ input.

17. (S) The only way the flip-flop can become set is by the application of a binary 0 or low input to the S input.

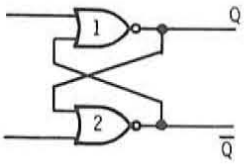


Figure 6-9

The latches we've discussed so far use positive logic NAND gates. We can also make latches out of positive logic NOR gates. Such a latch is shown in Figure 6-9.

It is identical to the other latches just discussed in that the two gates are wired back-to-back. Even the logic symbol is the same. But does this latch function the same way?

Recalling your knowledge of positive logic NOR gates, determine how the latch works and select the correct answer below.

A. The NOR latch is set or reset by binary 1's at the inputs instead of binary 0's.
B. The NOR latch requires an inverter on each input to make it function like an NAND latch.
C. The NOR latch functions exactly like the NAND latch.

18. (A. The NOR latch is set or reset by a binary 1 at the inputs instead of a binary 0.)

First, refresh your memory on NOR gate operation by referring to the truth table below.

INPUTS		OUTPUT
A	B	C
low	low	high
low	high	low
high	low	low
high	high	low

A high or binary 1 on either or both inputs produces a low or binary 0 output. This is considerably different from the NAND gate so the effect is to make the operation of a NOR latch completely different from the NAND latch.

While NOR and NAND latches have exactly the same function, they achieve it in a slightly different way. To set the NOR latch you apply a binary 1 to the S input. To reset it you apply a binary 1 to the R input. Normally, both inputs should rest at binary 0. And, if both inputs are made binary 1 simultaneously, the "limbo" or ambiguous state occurs. This is the exact opposite set of input conditions that exist in the NAND latch. Take a look at the circuit in Figure 6-10.

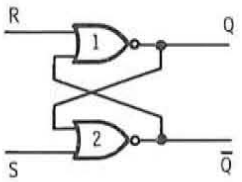


Figure 6-10

Note a subtle difference. The R and S inputs are reversed from those on the NAND latch. The reason for this has to do with the characteristics of the NOR gate. Applying a binary 1 to the R input forces the output of gate 1 low. This makes the upper and lower inputs to gate 2 low or binary 0 so its output is a binary 1. With this arrangement ($Q = 0, \overline{Q} = 1$) the flip-flop is clearly reset. As you can see, the interpretation of the outputs is the same. In fact, it is the same for *any* flip-flop.

When the NOR latch is in the "limbo" condition, both outputs will be 0.

19. (low) Yes, both outputs will go to the binary 0 state if a binary 1 level is applied to the R and S inputs simultaneously. This is exactly the opposite of what happens in the NAND latch. Nevertheless, this ambiguous condition is generally avoided unless there is some specific application for it.

To sum up the operation of a NOR latch, complete the truth table below. Then check your answer in the next frame.

INPUTS		OUTPUTS		
S	R	Q	$\overline{Q}$	STATE
0	0	X	$\overline{X}$	
0	1	0	1	Set
1	0	1	0	Reset
1	1	0	0	Ambiguous

20. (See correct truth table below).

INPUTS		OUTPUTS		
S	R	Q	$\overline{Q}$	STATE
0	0	X	$\overline{X}$	Either set or reset
0	1	0	1	Reset
1	0	1	0	Set
1	1	0	0	Ambiguous

As before in the NAND latch, the X output indicates either set or reset.

One of the most common and useful applications for a latch flip-flop is in switch buffering. Pushbutton switches are used in digital equipment to control various aspects of its operation. However, most pushbutton switches produce contact bounce. When the button is depressed or released, the switch contacts do not make an immediate solid electrical or mechanical connection. The contacts "bounce" open and closed for a brief period of time

The waveform in Figure 6-11 indicates this effect.

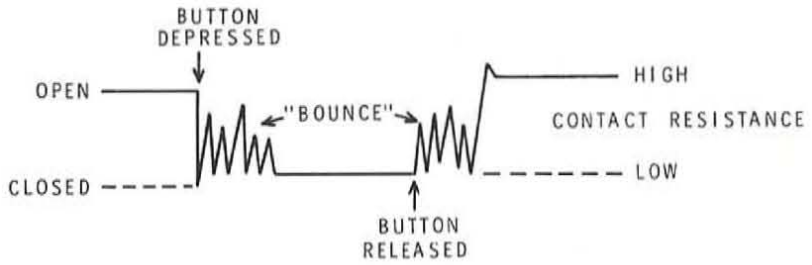


Figure 6-11

This waveform could represent contact resistance. Naturally, if current is being switched, this waveform would represent the voltage across the switch. Instead of getting solid off-on switching, you get pulses. Such pulses can repeatedly trigger digital circuits. In pressing the button once you would expect to get a single pulse or level change. Instead, the contact bounce gives you several. This effect is usually detrimental to the performance of digital circuits.

The circuits in Figure 6-12 show two ways of using a pushbutton switch to supply a logic pulse or level change. Such circuits are usually producing a considerable amount of contact bounce.

Instead of the switch supplying a single logic level change when depressed or released, _____ are produced because of the contact bounce.

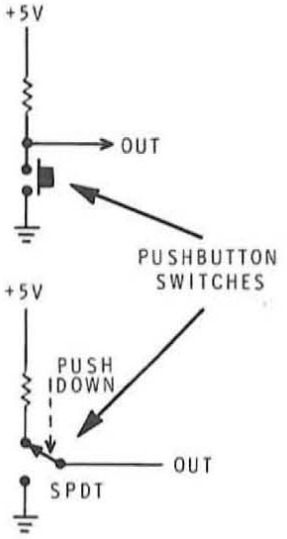


Figure 6-12

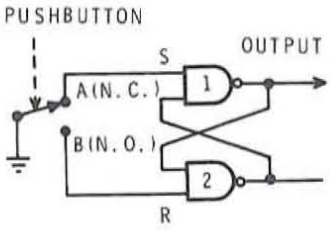


Figure 6-13

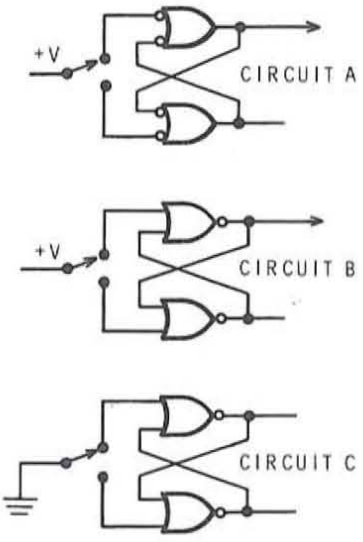


Figure 6-14

21. (pulses) Pushing a pushbutton will usually generate a series of pulses instead of a single, clean logic level change because of contact bounce. To overcome this problem, the switch can be combined with a latch as shown in Figure 6-13.

An SPDT break-before-make (non-shorting) momentary contact pushbutton switch is normally used. With the switch in position A (not depressed or normally closed, N.C.), the output of gate 1 is held high. Depressing the switch, so that the grounded arm contacts position B, forces the output of gate 2 high and the output of gate 1 low. So how is the "bounce" removed? Well, as the button is depressed the arm of the switch breaks contact with point A. Even though it may bounce several times between open and ground, it has no effect on the state of the latch. The effect is the same as trying to repeatedly set a latch that is already set. Nothing happens. As the contact arm is in transit between points A and B, both inputs to the latch are open so the latch simply remains set. As point B is contacted, the latch resets. The slightest disturbance will trigger the state change of the latch. The feedback in the latch carries the state change through quickly. Even if switch bounce occurs, the latch is insensitive to it. The result is a single clean logic level change at the output. Releasing the pushbutton causes the latch to change back to its original state.

A NOR latch can also be used to buffer contact bounce. Which circuit in Figure 6-14 accomplishes this?

A. Circuit A
B. Circuit B
C. Circuit C

22. (Circuit B) The NOR latch removes contact bounce just as well as the NAND latch, but the arm of the switch must have a plus voltage (the supply voltage or binary 1 logic level) on it. The NAND latch requires a ground or binary 0 level on the switch arm for proper operation.

Another switch buffer latch circuit is shown in Figure 6-15.

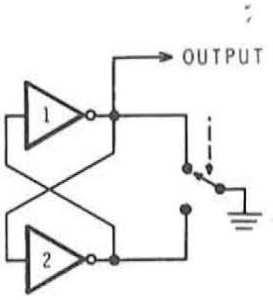


Figure 6-15

The latch is made of inverters so the outputs and inputs are common. The switch normally holds the output of inverter 1 low so that inverter 2 output is high. Pressing the switch reverses this state. The output is a "bounceless" level change.

The most important requirement for a switch used with a latch buffer is that it must be —

A. An SPST type.
B. Momentary contact only.
C. An SPDT type.

23. (C. A SPDT type.) The switch must have two terminals so a SPDT unit is required. And it is important that it be a break-before-make type so that the A and B contact points are not shorted momentarily in switching from one position to the other. This would put the latch into its "limbo" state briefly and false triggering will occur.

Another point is that the switch doesn't necessarily have to be a momentary contact type pushbutton. Any SPDT switch, slide or toggle, can be used. If it supplies logic level changes to a digital circuit, it will probably need buffering.

This completes the material on latch flip-flops. Answer the Self Test Review questions, then perform Experiment 9.

Self Test Review

1. What will the normal output level of a latch be if it is set?
   a. high
   b. low
2. The complement output of a latch is low. What is the bit value stored?
   a. binary 0
   b. binary 1
3. Normally the duration of the pulses applied to the set or reset inputs should only be long enough to put the latch in the proper state.
   a. True
   b. False
4. Which of the following is *not* a typical name for the circuit discussed in this section?
   a. latch
   b. RS flip-flop
   c. set-reset flip-flop
   d. multivibrator
5. The ambiguous state in a latch is indicated by which of the following conditions?
   a. both outputs low
   b. both outputs high
   c. either a or b
   d. one output low, the other high
6. Unless the state of a NAND gate latch is being changed, its inputs should both be
   a. high
   b. low
   c. open
7. Both inputs of a NAND latch are low. The state of the latch is:
   a. set
   b. reset
   c. ambiguous
8. Both inputs to a NAND latch are low. The S input goes high. Shortly thereafter, the R input goes high. The state of the latch is
   a. set
   b. reset
   c. ambiguous

9. Both inputs to a NOR latch are high. The R input goes low, then the S input goes low. What is the value of the bit stored in the latch?
   a. binary 0
   b. binary 1
10. Besides the storage of binary data, latches are also commonly used for _____ _____.
11. The fan out (maximum allowable number of loads) of a TTL gate is 10. What is the fan out of a latch?
    a. 1
    b. 2
    c. 9
    d. 10

Answers

1. a. high
2. b. binary 1
3. a. True
4. d. multivibrator
5. c. Either a. or b. The ambiguous state is indicated by two high outputs in a NAND latch and two low outputs in a NOR latch.
6. a. high
7. c. ambiguous
8. b. reset. The *last* or most recent input level determines the state of the latch.
9. b. binary 1. See explanation in 8 above.
10. switch buffering (to eliminate contact bounce).
11. c. 9 The output of a TTL gate in a latch is connected to the input of the accompanying gate, therefore its fan out is reduced by one. If the total fan out of a gate is 10, the fan out or load capability of the gates in a latch is one less or 9.

EXPERIMENT 9

SET-RESET FLIP-FLOPS

OBJECTIVES: To demonstrate the operation and characteristics of a set-reset (latch) flip-flop.

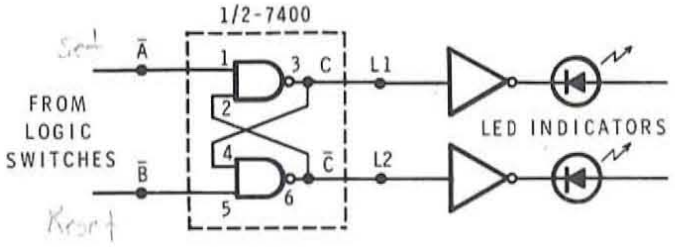
Materials Needed:

Heathkit Digital Design Experimenter
1 — 7400 IC (443-1)
1 — 7402 IC (443-46)

Procedure

1. Wire the latch circuit shown in Figure 6-16. The set (S) and reset (R) inputs to the latch will come from the $\overline{A}$ and $\overline{B}$ outputs of the two logic switches. The A logic switch is the set input, the B logic switch is the reset input. The latch outputs, C and $\overline{C}$, will be displayed on LED indicators L1 and L2 respectively. Be sure to apply power to the IC by connecting pin 14 to +5 volts and pin 7 to GND.

Figure 6-16



When the logic switches are not depressed, what is the normal state of the S and R inputs? High.

2. Apply power to the Experimenter and note the state of the latch by observing LED indicator L1. L1 = binary 1.

Using the logic switches, apply the logic levels designated in Table I to the S and R inputs of the latch. Observe the output conditions on the LED indicators for each set of input states. Record your output states in Table I.

Table I

INPUTS		OUTPUTS		
S (A)	R (B)	C(L1)	$\overline{C}$(L2)	STATE
0	0	1	1	—
0	1	1	0	Set
1	0	0	1	Reset
1	1	0	1	stable

In the column marked STATE in Table I, write a single word designating the state represented by each set of outputs. To get a feel for how the circuit operates, play with the inputs while observing the outputs. By repeatedly putting the latch into the set, reset and ambiguous states you will understand it better.

3. Construct the circuit shown in Figure 6-17. Use a type 7402 IC. As before, the set and reset input signals will come from the logic pushbuttons A (set) and B (reset).

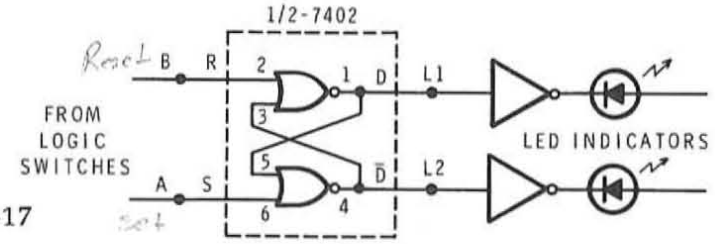


Figure 6-17

4. Apply power to the circuit. Note the state of the latch by observing L1. L1 = binary ____1____. Then apply the inputs given in Table II. Observe the outputs for each set of inputs and complete the D and $\overline{D}$ columns.

Table II

INPUTS		OUTPUTS		
S (A)	R (B)	D	$\overline{D}$	STATE
1	1	0	0	LATCH
0	1	0	1	Reset
1	0	1	0	Set
0	0	0	0	

In the column labelled STATE in Table II, write a word that designates the state of the latch as indicated by each of the output indications.

5. Compare the data in Tables I and II and note the similarities and differences in operation between the NAND and NOR latches.

Discussion

In Steps 1 and 2 you constructed a NAND gate latch using a type 7400 IC. The inputs were obtained from the momentary contact logic switches A and B. Specifically, the $\overline{A}$ and $\overline{B}$ outputs of these logic switches were used to supply the set and reset inputs respectively. The $\overline{A}$ and $\overline{B}$ outputs are normally high. When the switch is depressed, the $\overline{A}$ or $\overline{B}$ output goes low. With both switches in their normal or non-depressed state, the S and R inputs to the latch are binary 1. Therefore, they have no effect on the state of the latch.

When power is applied the latch can go into either state. The C output could be either 0 or 1 as indicated by LED indicator L1. Regardless of the initial state, C and $\overline{C}$ should be complementary.

When the B logic switch is actuated, a low level is applied to the reset input. The C output (L1) should go low and the $\overline{C}$ (L2) output high. When the B switch is released, the flip-flop will remain reset thereby storing a binary 0. Actuating the A logic switch supplies a low to the set input. The C output (L1) goes high and the $\overline{C}$ output (L2) low. When the A switch is released, the flip-flop remains set storing a binary 1.

When both logic switches are actuated to apply a low to both set and reset inputs, both C and $\overline{C}$ outputs go high. This is the ambiguous state.

In Steps 3 and 4 you constructed and tested a NOR gate latch. The set and reset inputs are supplied by the normal outputs (A and B) of the two logic switches on your Experimenter. The A and B outputs are normally low when the switches are not actuated. A low input to a NOR latch does not affect its state as it does in the NAND latch. Therefore, with both inputs low, the latch can be either set or reset depending upon the arbitrary state it comes up in when power is applied.

When the B logic switch is actuated, the B output goes high applying a high or binary 1 level to the reset input. This forces the D output low and the $\overline{D}$ output high thereby indicating that a binary 0 has been stored. Upon releasing the B switch, the latch retains the reset state.

When you depress the A logic switch, you apply a high level to the set input. The D output goes high and the $\overline{D}$ output goes low. The flip-flop remains in the set state when the switch is released.

If you apply binary 1's to both set and reset inputs at the same time by simultaneously actuating the A and B logic switches, the latch goes into the ambiguous state. Both outputs go low.

In comparing the NAND and NOR gate latches, we can say in summary:

1. Either type flip-flop will store one bit of data, with the state of the outputs indicating the value of the bit stored. The two outputs are complementary.
2. The NAND latch requires a low level on either input to set or reset it. The NOR latch requires a high level at the appropriate input to change its state.
3. For a NAND latch, the inputs normally rest in the high state. The NOR latch inputs are normally both low.
4. Both types of latches have an ambiguous state. In the NAND both outputs are high. In the NOR gate latch, both outputs are low.

D TYPE FLIP-FLOPS AND REGISTERS

24. Now let's consider the D type flip-flop. Its symbol is shown in Figure 6-18.

Like any other flip-flop the D flip-flop has two outputs that are used to determine its contents. That is, the outputs indicate what bit is stored there.

If we are using positive logic and the $\overline{Q}$ output is high, then the contents of the flip-flop is —

A. Binary 0
B. Binary 1
C. Can't tell, insufficient information given.

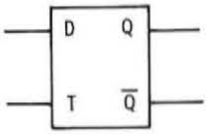


Figure 6-18

25. (A. binary 0) The $\overline{Q}$ output is high indicating a binary 1. The Q or normal output therefore is the complement or a binary 0. The Q output tells you the state of the flip-flop directly. Since it is a binary 0, the flip-flop is reset. The point here is that you read the outputs of a D flip-flop as you would a latch or any other flip-flop for that matter.

Now look at the inputs. Like on the latch there are two. But they work differently. The D input is where you apply the data or bit to be stored. Of course, it can be either a binary 1 or a binary 0. The T input line controls the flip-flop. It is used to determine whether the input data is recognized or ignored. If the T input line is high or binary 1, the data on the D line is stored in the flip-flop. If the T line is low or binary 0, the D input line is not recognized. The bit stored in the flip-flop previously is retained. The D line can essentially do anything and it will just be ignored if T is low.

If both the D and T inputs are binary 1, the normal output will be _____.

26. (binary 1) Right. The T line is high so the flip-flop stores whatever is on the D input line. Since a binary 1 is present, it is stored, and the normal output indicates this condition. As long as the T line is high, the normal output will simply follow or track the D input.

You can get a better idea about how the D flip-flop works by taking a look at its insides. The logic diagram of one type of D flip-flop is shown in Figure 6-19.

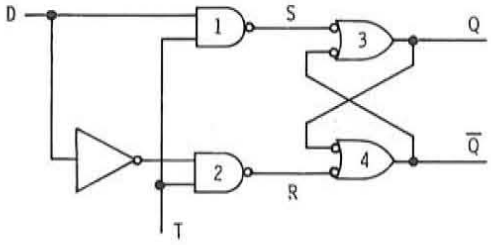


Figure 6-19

Gates 3 and 4 form a latch where the bit is stored. Gates 1 and 2 are enabling gates that pass or inhibit the input. The inverter makes sure that the S and R inputs to the latch are always complementary to avoid any possibility of the ambiguous state occurring.

With the T input low, the S and R latch inputs are _____.

27. (high or binary 1) Yes. The low input on the T line holds the outputs of gates 1 and 2 high. This is the normal state for the inputs of a NAND latch to assume. In this state the latch is undisturbed.

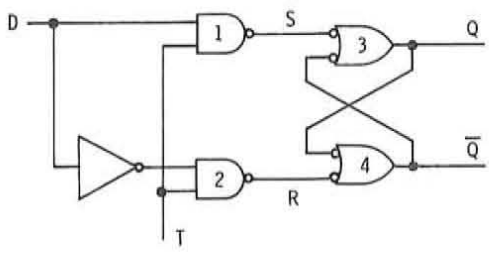


Figure 6-19

Refer to Figure 6-19. Suppose a binary 1 is applied to the D input. Of course, nothing happens if the T input is still low. Now, make the T input go high. This enables both gates 1 and 2. The binary 1 on the D input makes gate 1 output go low. The inverter puts a low on the input to gate 2 so its output stays high. The low output of gate 1 sets the latch causing it to store the binary 1. Returning the T input low disables the input, but the binary 1 is retained.

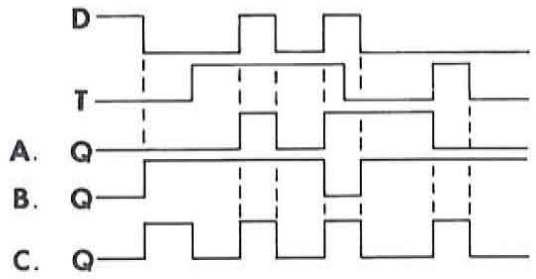


Figure 6-20

Now, look at the waveforms in Figure 6-20. These represent the D and T inputs to a flip-flop. Which of the three waveforms given represents the Q output produced by these inputs.

28. (A) With the indicated input waveforms, you will get the Q output illustrated in Figure 6-21. It takes a bit of concentration to arrive at this, but it's not difficult. All you have to remember is that the Q output is identical to the D input as long as the T input is high. And, when the T line goes low, the flip-flop stores the *last* state it sees on the D input.

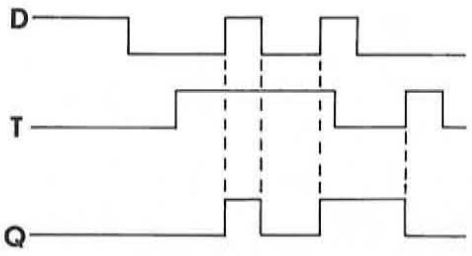


Figure 6-21

A D flip-flop is reset. The state of the D input prior to T going low was binary _____.

29. (binary 0) The circuit in Figure 6-22 shows another method of implementing the D flip-flop. As in the other circuit, gates 3 and 4 form the storage latch while gates 1 and 2 handle the input control.

Note that no separate inverter is needed. This arrangement functions exactly like the other circuit but is more economical of logic circuits. This circuit is quickly and easily made from a common quad 2 input NAND IC.

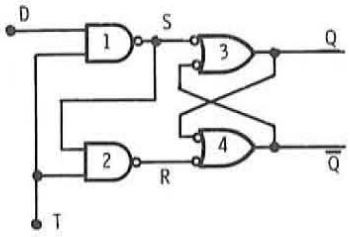


Figure 6-22

The operation of a D type flip-flop can be completely described by a truth table. From your present knowledge of D flip-flop operation, complete the truth table below.

INPUTS		OUTPUTS	
D	T	Q	$\overline{Q}$
0	0		
0	1		
1	0		
1	1		

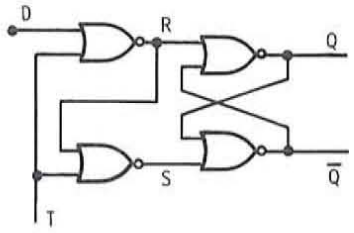
30. (See truth table below)

INPUTS		OUTPUTS	
D	T	Q	$\overline{Q}$
0	0	X	$\overline{X}$
0	1	0	1
1	0	X	$\overline{X}$
1	1	1	0

Note that when T is binary 1, the Q output is the same as the D input. When T is binary 0, the Q output can be either binary 0 or 1 depending upon a previous input. This is indicated by the X state in the table. Note that a D flip-flop does not have an ambiguous state.

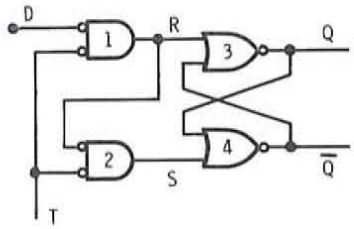
A D flip-flop can also be constructed with positive NOR gates as indicated in Figure 6-23.

Figure 6-23



To explain the NOR latch better, however, it is desirable to redraw it so that the gates are shown as they are used. See Figure 6-24.

Figure 6-24



Gates 3 and 4 make up the latch that can be set or reset by the inputs from gates 1 and 2. Gates 1 and 2 control the input in that they determine whether the D input will be transferred to the latch. Functionally they perform the *AND* operation.

Now, analyze the circuit shown above and determine how it operates.

The NOR latch operates exactly like the NAND latch.

A. True

B. False

31. (False) The NOR flip-flop does not perform exactly like the NAND flip-flop, but it is similar. Both circuits store one bit of information. The recognition of the D input is determined by the state of the T input. And, here lies the difference. In the NAND flip-flop, the T line has to be high in order for the flip-flop to store the D input state. In the NOR flip-flop, the T line must go *low* in order to recognize the D input. Bringing the T line high disables the D input. The last D input state prior to the T input going high is stored.

The most common application of the D flip-flop is as an element in a storage register. A register is a group of flip-flops used to store a binary word. Each flip-flop stores one bit of the data word.

How many flip-flops would be needed to store one BCD digit of data? _____.

32. (4) Correct. A single BCD digit consists of four bits. To store this word, we need one D flip-flop for each bit. The result is a 4 bit storage register.

Figure 6-25 below illustrates a 4 bit register.

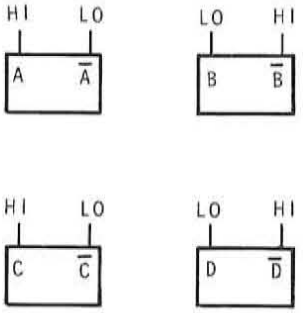


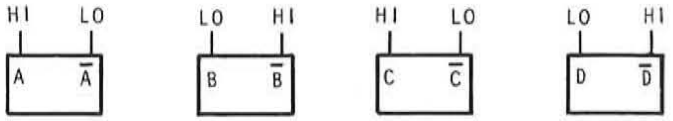
Figure 6-25

Each flip-flop is labeled with its own designation, A through D, so that it can be identified. Also shown here are the states of the flip-flop.

Given this information, what number is stored in this register? (assume positive logic)

A. 1010
B. 0101
C. Can't tell, not enough information

33. (C. Can't tell, not enough information) With the information given you really can't tell what the number is. True, you can look at normal outputs of the flip-flop and write down the corresponding bit values. This will give you two possible bit patterns depending upon whether you read from right to left or left to right. These bit patterns are 1010 (left to right) and 0101 (right to left).



Repeat Figure 6-25

There is one missing ingredient. Which bit is the most significant (MSB)? The answer is, it could be A or it could be D. Usually the LSB is designated as the earliest letter of the alphabet or the lowest number if the number designations are used. If A is the LSB above then the number stored there is 0101 or a decimal 5. If D is the LSB the number is 1010 or a decimal 10. It's always necessary to identify the LSB and/or MSB positions on a register in a logic diagram.

A five bit register with flip-flops A, B, C, D and E is storing a number. The flip-flop states are: A-reset, B-set, C-set, D-reset and E-set. If A is the LSB, what is the decimal value of the binary number stored in the register? _____.

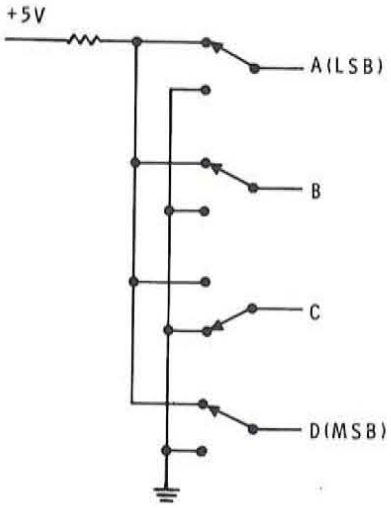


Figure 6-26

34. (22) Good work. The binary number is written from the flip-flop states, 0 = reset and 1 = set. The A flip-flop is the LSB so the binary number is EDCBA or 10110. This converts to a decimal 22.

Another type of register you should be familiar with is the switch register. This is exactly what its name implies, a register made of switches. The group of switches form a register for storing a single word or bit pattern using one switch per bit. The position of the switch (up/down, on/off, open/closed, etc.) determines the bit value.

A four bit switch register is shown in Figure 6-26. Four single pole double throw (SPDT) switches store the bit value as a physical position. The A, B, C, and D outputs are ground (0) or +5 (1) depending upon their position.

What *decimal* number is stored in this register? _____.

35. (11) Right. The binary number stored in the switch register is 1011 or decimal 11. You can determine the switch register contents by monitoring its electrical outputs. Or in most switch registers, the switches are mounted adjacent to one another horizontally with the LSB on the right and their position (usually up or down) is readily observable. Up usually means 1, down means 0. Therefore, a visual identification of the switch register contents is possible.

A frequent operation in digital equipment is the transfer of data from one register to another. Figure 6-27 illustrates how the data in a switch register can be transferred to a register made of D flip-flops. The switch outputs are fed to the D inputs. The control of the transfer is by the common T lines on the flip-flops.

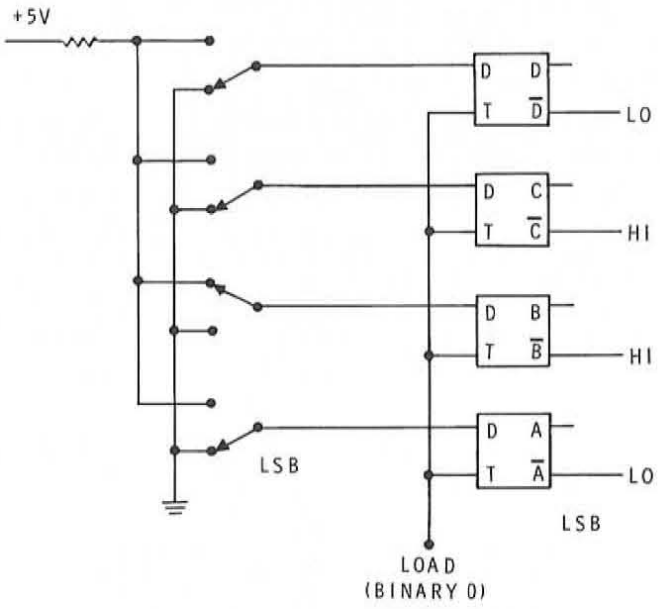


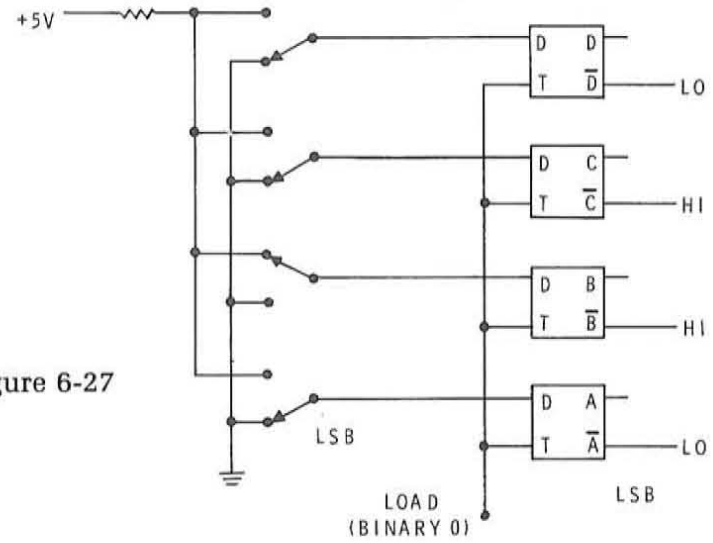
Figure 6-27

Assuming the use of positive logic and NAND flip-flops, what is the content of the flip-flop register above?

A. 1001
B. 0010
C. 0110

36. (A. 1001) The data provided to you was the flip-flop complement outputs. From this you could determine the normal outputs and hence the contents of the register. You could also determine the output of the switch register, 0010, by inspection. With the T inputs to the flip-flop at binary 0, the data input from the switch register is not recognized by the flip-flops. But, if the LOAD control line goes high momentarily, the flip-flop register contents will become the same as the switch register, 0010.

Repeat Figure 6-27



There are two important points to note here. First, the LOAD input controls the transfer of the data from the switch register to the flip-flop register. This LOAD input is the parallel or simultaneous control of all the flip-flop T inputs. This line is also sometimes called the STROBE input since it is usually only enabled or "strobed" momentarily with a binary 1 pulse to transfer the data.

Second, the data transfer is a parallel one. That is all bits from the switch register are loaded into the flip-flop register simultaneously.

Instead of drawing the individual flip-flops, most registers are shown as only a single box with the inputs and outputs identified as shown in Figure 6-28.

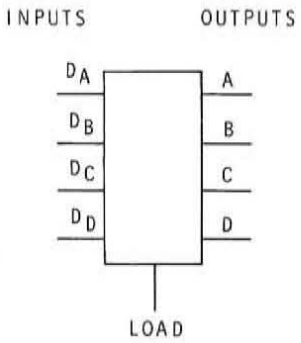


Figure 6-28

This is particularly true of MSI integrated circuit registers. Many IC registers also do not have the complement outputs available.

How is a D flip-flop register like the one in Figure 6-28 reset?

A. Apply a binary 0 to the LOAD line.
B. Load the input 0000

37. (B. Load the input 0000) Correct. To reset the register you simply load 0000. You apply 0000 to the inputs and momentarily bring the load line high. The register will then be cleared or reset since each flip-flop will be storing a binary 0.

Some commercially available D flip-flop IC registers have a single reset line which will clear all flip-flops in the register at once without having to load 0000.

Now answer the Self Test Review questions and perform Experiment 10.

Self Test Review

12. The T input of a D type flip-flop determines its state.
    A. True
    B. False
13. D type flip-flops are widely used to form _____ _____.
14. Complete the truth table of a NOR gate D flip-flop.

INPUTS		OUTPUTS	
D	T	Q	$\overline{Q}$
0	0		
0	1		
1	0		
1	1		

15. What is the decimal equivalent output of the register shown in Figure 6-29? Assume positive logic. _____

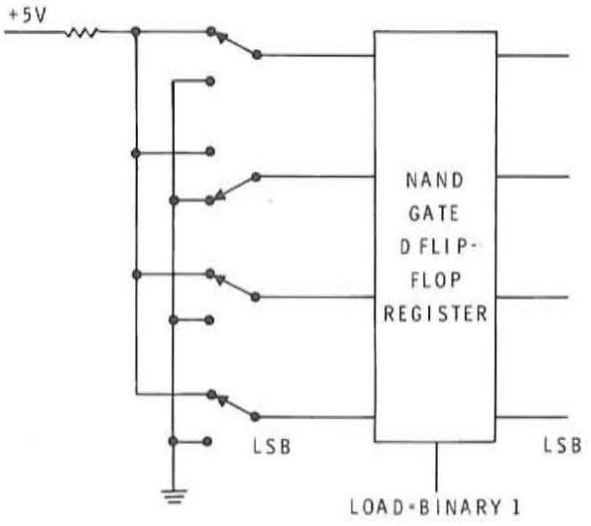


Figure 6-29

16. Given the input waveforms shown in Figure 6-30, sketch the normal output waveform of a NAND gate D type flip-flop.

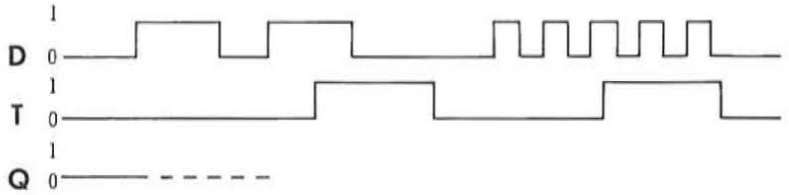


Figure 6-30

Answers

12. False
13. storage registers
14.

INPUTS		OUTPUTS	
D	T	Q	$\overline{Q}$
0	0	0	1
0	1	X	$\overline{X}$
1	0	1	0
1	1	X	$\overline{X}$

X = 0 or 1

The normal (Q) output will be the same as the D input when T is low. When T is high, the D input is ignored, and the flip-flop simply retains the bit X stored there previously.

15. 11_{10} The output of the switch register is 1011. This is stored in the flip-flop register since the LOAD line is high. Therefore, the register output is $1011_2 = 11_{10}$.
16. See Figure 6-31.

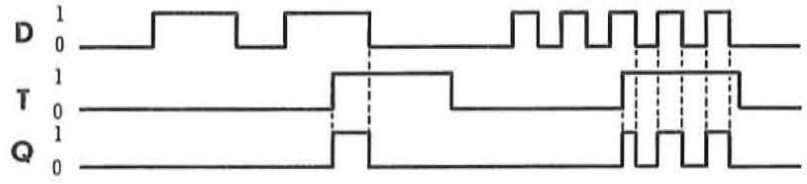


Figure 6-31

EXPERIMENT 10

D TYPE FLIP-FLOPS AND REGISTERS

OBJECTIVES: To demonstrate the operation of a D type flip-flop and a storage register.

Materials Needed:

Heathkit Digital Design Experimenter ET-3200

1 — 7400 TTL IC (443-1)

1 — 4001 CMOS IC (443-695)

1 — 7475 TTL IC (443-13)

Procedure

1. Wire the circuit shown in Figure 6-32. Use a type 7400 IC. Because of the large number of connections required, take your time to avoid making a wiring mistake. Double check your connections before you perform the experiment. Don't forget to connect pin 14 to +5 volts and pin 7 to GND. The D and T inputs will be supplied by data switches SW1 and SW2. The flip-flop outputs will be monitored on LED indicators L1 and L2.

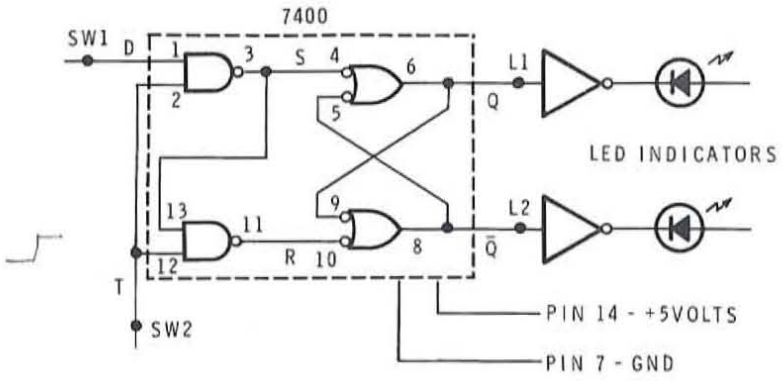


Figure 6-32

2. Set input data switches to binary 0 and record the state of the flip-flop.

   Apply the logic levels indicated in Table I to the D and T inputs. Note the output states for each set of inputs and record your results in Table I.

TABLE I

INPUTS		OUTPUTS	
D	T	Q	$\bar{Q}$
0	0	1	0
0	1	0	1
1	0	1	0
1	1	1	0

3. For a more graphic indication of exactly what takes place, replace the data switch on the D input with a logic clock signal. Set the clock frequency to 1 Hz and connect one of the free LED logic indicators to monitor it. Set the T input first to binary 1 and observe the flip-flop outputs for a brief period. Note the relationship between the clock state and the Q output. Set the T input to binary 0 and again observe the outputs. Repeat.

T = 1
transfer data

4. Construct the circuit shown in Figure 6-33. Use a 4001 CMOS NOR IC. Use data switches for the D and T inputs and LED indicators for the outputs.

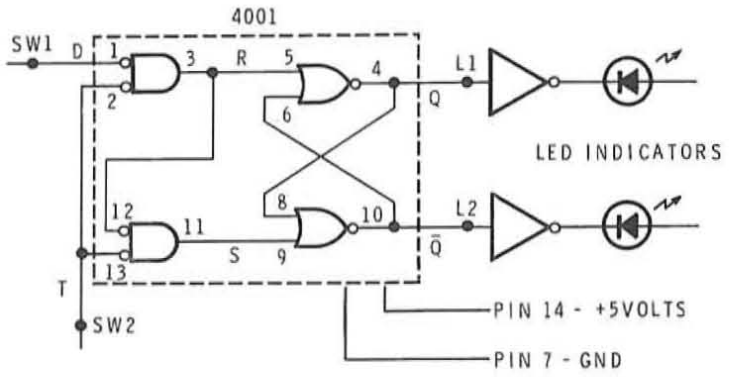


Figure 6-33

T = 0
transfer data

5. Apply the logic levels given in Table II to the D and T inputs. Note the output states for each set of inputs and record your data in Table II.

TABLE II

INPUTS		OUTPUTS	
D	T	Q	$\bar{Q}$
0	0	0	1
0	1	0	1
1	0	1	0
1	1	1	0

6. Repeat Step 3 for the NOR D-type flip-flop.
7. Compare your results in Tables I and II and in Steps 3 and 6.
8. Wire the circuit shown in Figure 6-34. The 7475 IC contains four TTL D type flip-flops similar in operation to the NAND D type flip-flops

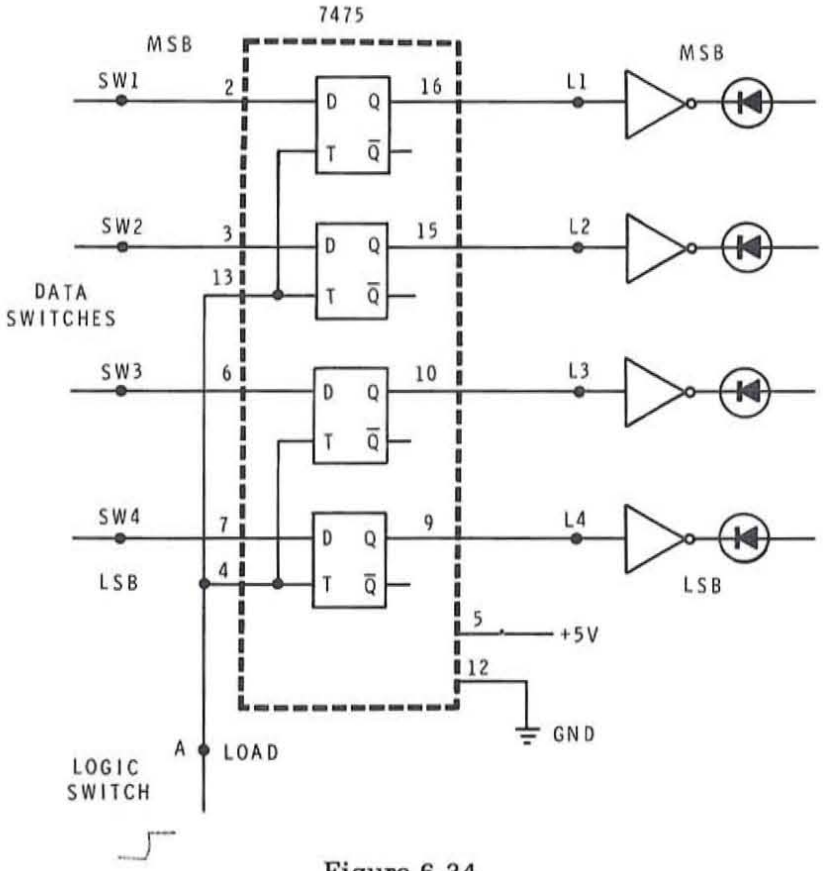


Figure 6-34

discussed earlier. Figure 6-35 shows the internal structure and pin connections for this device. Note that +5 volts is connected to pin 5 and GND is connected to pin 12. The data switches on the Experimenter will be used as a switch register. The switch outputs will be used as a source of data for a four bit register made from the flip-flops in the 7475. You will monitor the register output on the LED logic indicator.

Logic switch A will be used as the LOAD or strobe signal which transfers input data into the register.

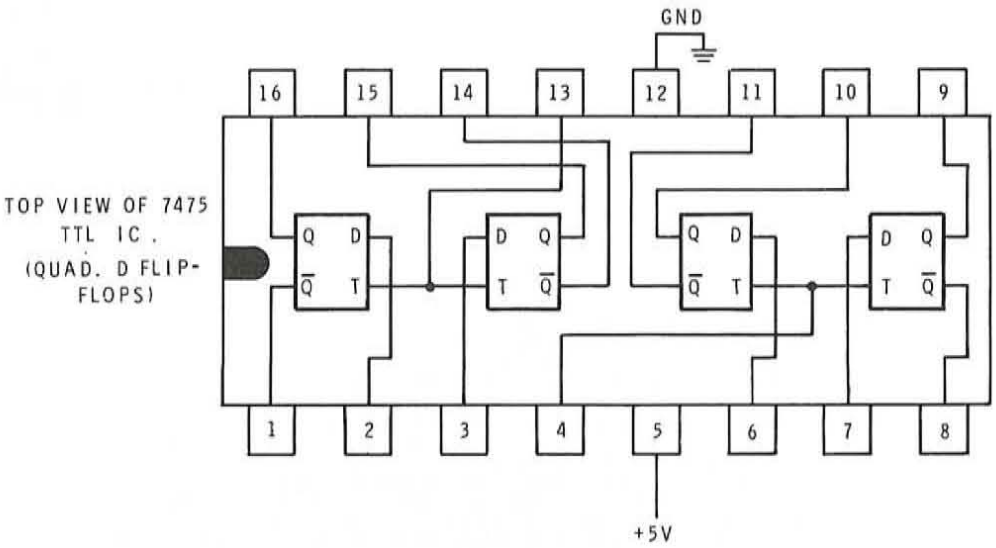


Figure 6-35 Top view of 7475 TTL IC. (quad D flip-flops).

9. Apply power to the circuit and record the number in the register. Indicator L4 monitors the LSB. 0
10. Set all of the data switches to binary 0. Then momentarily depress the A logic switch. Record the binary number in the register. 0 0 0 0
11. Set all the data switches to binary 1. Depress the A logic switch and note the register contents. Record. 1 1 1 1
12. Load the sixteen binary numbers 0000 through 1111 into the register one at a time by setting the data switches then actuating the A logic switch. Verify that the input does load by comparing the LED indicator states with the data switch setting *after* the A button is depressed.

Discussion

In Step 1 you constructed a D type flip-flop with TTL NAND gates. When you applied power in Step 2, the flip-flop could have assumed either the set or reset state. When you set the T input to binary 1 and the D input to binary 0, the flip-flop will be reset as indicated by L1 being off. With both the D and T inputs binary 1, flip-flop will become set. L1 will be on. With the T input set to binary 1, you can switch the D input between binary 0 and 1 and watch the normal output follow it. If the T input is binary 0, the flip-flop state will be that determined by previous inputs. Switching the D input between 0 and 1 while T is binary 0 will not affect the state of the flip-flop.

In Step 3 you applied the 1 Hz clock signal to the D input and observed the operation of the flip-flop. With T set to binary 0, the clock signal at the D input is ignored. But with T set to binary 1, the flip-flop output follows the D input. The LED indicators on the CLK and Q lines should switch off and on in synchronism.

In Step 4 you assembled a D flip-flop from CMOS NOR gates. In Steps 5 and 6 you evaluated its operation. Basically you should have found that its operation was identical to that of the NAND D flip-flop with the exception of the state of the T input. On the NOR flip-flop, the T input must be low in order for the D input to be recognized. With the T input low, the normal output follows or tracks the D input. When the T input is high, the D input will have no effect on the state of the flip-flop.

In Step 8 you assembled a 4 bit storage register using the four D type flip-flops in a type 7475 TTL MSI IC. The operation of the flip-flops in this device is similar to the NAND D flip-flop you studied earlier. The data switches on the Experimenter were used as a switch register. The A logic switch is used as a manual LOAD control. The A output is normally low thereby keeping the T inputs to all four register flip-flops low. The inputs from the switch register are ignored. When the A switch is actuated, the A output goes high causing the data from the switch register to be loaded into the register.

When you first applied power, the contents of the register could have been anything. When power is applied to a flip-flop it can come up in either the set or reset condition. Next you reset the register by loading all binary 0's. Then you loaded 1111. These two operations check to see that all four flip-flops work in both states.

Finally, you sequentially loaded the numbers 0000 through 1111. This gives you an opportunity to become familiar with setting binary numbers on the switch registers and practice in reading binary numbers from the LED indicators. An important point you should have grasped is that the input word can be different from the register contents. With the LOAD input low, the D inputs to the flip-flop are ignored. When LOAD is made binary 1, however, the register output becomes equal to the inputs.

JK FLIP-FLOPS

38. The JK flip-flop is the most versatile type of binary storage element in common use. It can perform all of the functions of the RS and D type flip-flops described earlier plus it can do several other things that these simple flip-flops cannot. Naturally, it is more complex and expensive than the other types so for that reason it isn't always used where simpler and less expensive circuits will do.

An integrated circuit JK flip-flop is really two flip-flops in one. It usually consists of two latches, one feeding the other, with appropriate input gating on each. See Figure 6-36.

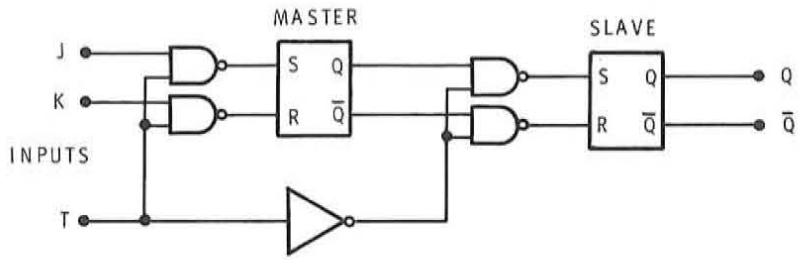


Figure 6-36

The arrangement is called a master-slave JK flip-flop. The master flip-flop is the input circuit. Logic signals applied to the JK flip-flop set or reset this master latch. The slave flip-flop is the latch from which the outputs are taken. The slave latch gets its input from the master latch. Both latches are controlled by a clock pulse. Since there are two *places* to store bits in a JK flip-flop, there can be times when both master and slave latches are identical or times they are complementary. But only one of these latches is responsible for indicating the state of the JK flip-flop.

Which latch, master or slave, determines the state of a JK flip-flop?

_____

39. (slave) Yes, the slave latch designates the state being stored. If it is set, the JK flip-flop is storing a binary 1. The slave latch is the output. And to determine the state of a flip-flop, look at its outputs. Even though it's called the slave, it tells the value of the bit stored. The master flip-flop controls the state that the slave latch assumes. You can see this better by studying the logic diagram of a typical JK flip-flop in Figure 6-37.

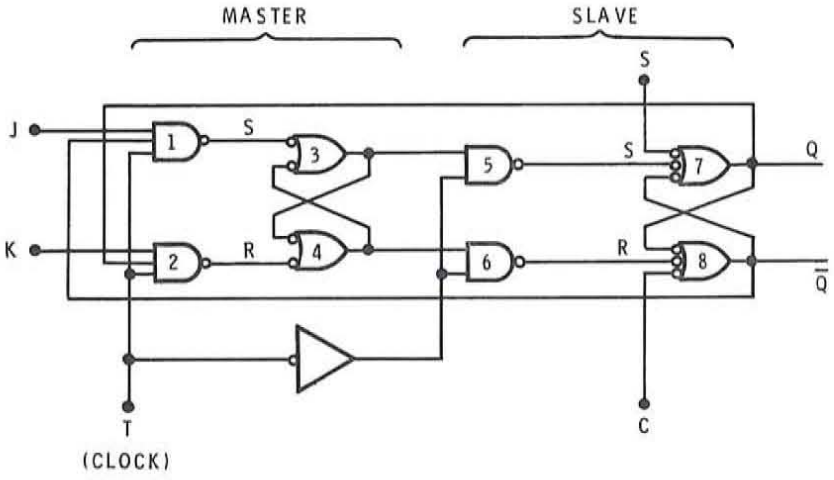


Figure 6-37

The logic gates are the positive NAND type. Gates 3 and 4 make up the master latch while its input is controlled by gates 1 and 2. The slave latch is made up of gates 7 and 8. Gates 5 and 6 control the transfer of the master latch state to the slave latch. Note that clock signal T controls the input gating circuits. The inverter keeps the clock to the master and slave input gates complementary. The clock pulse controls the JK flip-flop while the J and K inputs determine exactly how it will be controlled. (Note: You will also see the T input referred to as CP or CK, designating clock pulse or clock.)

Refer to the logic diagram of the JK flip-flop in Figure 6-37. What other inputs control the JK flip-flop? _____

40. (S and C inputs) The set (S) and clear (C) inputs also control the JK flip-flop. These are inputs to the slave latch that can be used to set or reset (clear) the flip-flop. These inputs override all other circuitry in the JK flip-flop. These inputs are used to preset the state of the flip-flop prior to any other operation involving the JK inputs and the clock. They work just like the inputs on any latch.

To set the JK flip-flop, which of the following conditions must exist?

A. S input high, C input low
B. S input low, C input high
C. S and C inputs low
D. S and C input high

41. (B. S input low, C input high) To set the slave latch *and* the JK flip-flop, the S input should be low, the C input high. This forces the normal Q output high indicating that a binary 1 is being stored. To reset the JK flip-flop, the C input is made low while S is high. Normally, the S and C inputs will be high when they are not being used to preset the flip-flop. This arrangement is identical to that for the NAND latch.

Now let's consider how the J, K and T (clock) inputs affect the flip-flop. Refer to Figure 6-37.

Consider the time when the clock input is low. Gates 1 and 2 will be inhibited so the J and K inputs cannot control the state of the master latch. The master latch can be in either state.

What is the state of the slave latch when the clock line is low and assuming the S and C inputs are open?

A. Binary 1
B. Binary 0
C. The same as the master latch

42. (C. Same as the master latch) Yes, the slave latch will have the same state as the master latch when the clock input is low. The output of the inverter in the clock line is binary 1, causing the gates 5 and 6 to be enabled during this time. Therefore, the state of the master latch is simply transferred to the slave latch. For example, if binary 1 is stored in the master latch, the output of gate 3 will be high and the output of gate 4 will be low. This will make the output of gate 5 low and the output of gate 6 high. This low on the input to gate 7 will force its output high, thereby setting the slave latch and storing a binary 1.

Now if the clock T goes high, gates 1 and 2 will be enabled. The output of the inverter will inhibit gates 5 and 6. The master latch cannot further change the slave latch. But now with gates 1 and 2 enabled, the J and K inputs can affect the state of the master latch.

What other signals affect the master latch at this time? _____.

43. (Q and $\overline{Q}$) The JK flip-flop outputs Q and $\overline{Q}$ are fed back around to gates 1 and 2 where, along with the J and K inputs, they will determine the state of the master latch.

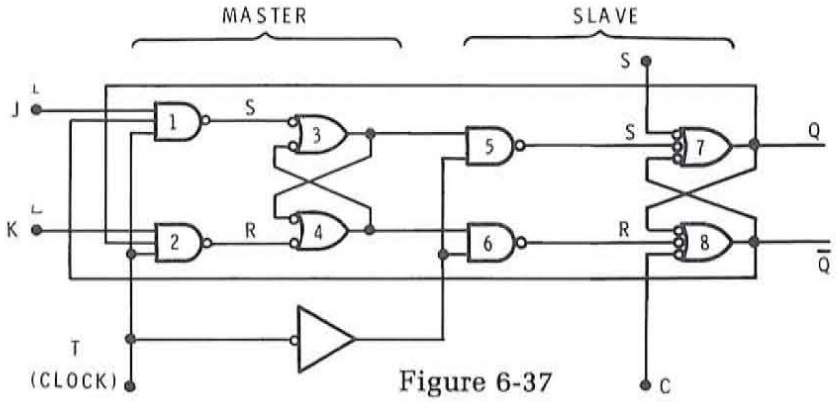


Figure 6-37

If both J and K inputs are low, the outputs of gates 1 and 2 will be held high, so no change takes place in the master latch.

If the J and K inputs are both high (or open), then the state of the master latch will be determined by the Q and $\overline{Q}$ outputs. For example, if the slave latch is set, the master latch will be reset. If the slave is reset, the master will be set. The reason for this is the way the outputs are crisscrossed back to gates 1 and 2. Remember that with the J, K and T inputs high, the state of the master latch will be determined by the Q and $\overline{Q}$ outputs.

If T, J, and K are high, and the slave latch is storing a binary 0, the master latch will be storing a binary _____.

44. (binary 1) Now let's consider the effect of the J and K inputs. These inputs are analogous to the set and reset inputs on a latch. If J is 1 and K is 0, we will set the master latch. If J is 0 and K is 1, the master latch will be reset. Remember, the T input line must be high for this to happen.

Does the JK flip-flop get set or reset as soon as the desired states are applied to the J and K inputs when T is high? _____.

45. (No) The state of the JK flip-flop is the state of the slave latch. The state of the slave latch is determined by that of the master latch. The state of the master is, in turn, determined by the J and K inputs. And to top it off, the clock input determines *when* each of these latches will be affected. With the clock input high, only the master latch will be affected. The inverter on the clock line blocks gates 5 and 6 so the slave latch is not disturbed. The states of the JK inputs will ultimately determine the output state but only at a specific time. When the clock line switches from high to low (trailing edge), the state of the master latch is transferred to the slave latch.

Which of the following conditions occurs when the clock input is high?

A. The state of the master latch is determined by the JK inputs.
B. The state of the slave latch assumes the state of the master latch.
C. Neither the master or slave latches are affected.

46. (A. The state of the master latch is determined by the JK inputs). When the clock (T) is high gates 1 and 2 will be enabled therefore the master latch will be changed by either the Q and $\overline{Q}$ outputs or by the J and K inputs. When the clock goes low, the state of the master latch is transferred to the slave latch through gates 5 and 6 which are enabled at this time. Gates 1 and 2 are inhibited so the J and K inputs have no effect.

If the J and K inputs are both left open or high, the flip-flop will change state each time the clock input switches from high to low. Consider the following: Clock high, JK inputs high and slave latch set. The master latch then is _____.

47. (reset) Right. The Q and $\overline{Q}$ lines fed back to gates 1 and 2 cause the master latch to be reset. Then when the trailing edge of the clock pulse occurs, (clock switches from 1 to 0), the reset state in the master is transferred to the slave. The JK flip-flop is now reset. When the clock again goes high, the slave latch then sets the master latch. As the clock goes low, the set state in the master is transferred to the slave. As you can see then, with the JK inputs high, the flip-flop complements itself each time the clock switches from high to low (trailing edge). We call this operation toggling.

Assume the J and K inputs are open or high. Which waveform in Figure 6-38 represents the normal flip-flop output?

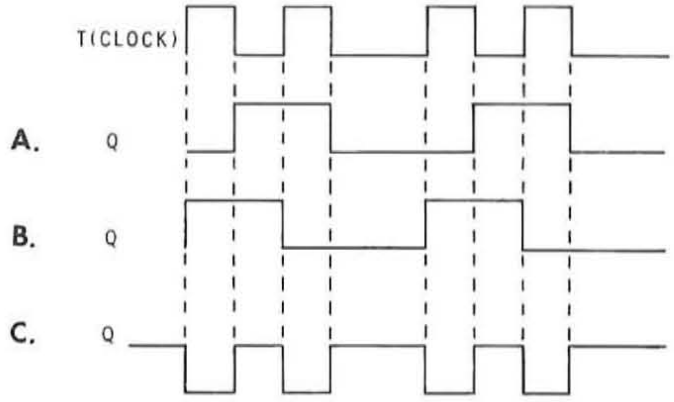


Figure 6-38

48. (A.) When the clock switches from 1 to 0, the state of the flip-flop will change. The output is not affected during the 0 to 1 transition (leading edge).

If you will look at the clock and output waveforms in Figure 6-39, you will see a definite relationship. What is it?

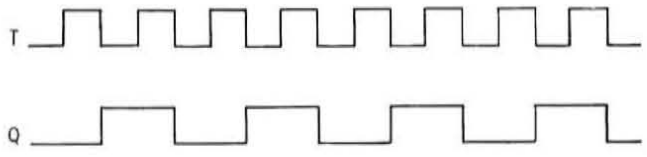


Figure 6-39

A. The output is the complement of the clock input.
B. The output has a frequency twice the input.
C. The output has a frequency one half the input.

49. (C. The output has a frequency that is one half the input.) The reason for this is simply that the flip-flop changes state on only the trailing edge or every other transition of the clock. Therefore, the JK flip-flop in its toggling mode is a two to one frequency divider. It halves any input frequency applied to the clock input. If an input of 50 KHz is applied, the output will be one half or 25 KHz. Cascading JK flip-flops permits frequency division by any factor of 2 (2, 4, 8, 16, 32, 64, etc.). The frequency division ratio is 2^n where n is the number of flip-flops cascaded.

We have now considered all of the modes of operation of the JK flip-flop, but let's review them each briefly.

First, there are the S and C inputs. The effect of these can be summed up by the truth table below.

INPUTS		OUTPUTS	
S	C	Q	$\overline{Q}$
1	1	X	$\overline{X}$
0	1	1	0
1	0	0	1
0	0	1	1

This is exactly the same truth table we established for the NAND latch.

The JK flip-flop has an ambiguous state. True or False?

50. (True) Yes, the JK flip-flop does have an ambiguous state. If both S and C inputs are low, both the Q and $\overline{Q}$ outputs will be high. Therefore, care should be taken to see that this condition cannot occur.

The set (S) and clear (C) inputs are used to preset the flip-flop to some desirable condition prior to another operation. The most common operation is to reset it. For that reason many IC JK flip-flops have only a C input line. Use of the S and C inputs is referred to as asynchronous operation. The state of the flip-flop changes immediately upon the application of the appropriate input level. No other conditions are necessary. This is not true of the J and K inputs. Their effect is dependent upon the state of the clock signal. Therefore, we call the J and K input effects synchronous because they cause state changes only on the occurrence of a specific clock transition, that is in synchronism with the clock.

In the JK flip-flop discussed here, state changes take place on the _____ to _____ transition.

51. (high to low, 1 to 0) When the clock input switches from 1 to 0, state changes occur. It is on this transition that the contents of the master latch is transferred to the slave latch. For some types of JK flip-flops just the opposite is true. Be sure to check the manufacturer's data sheet for details on any device you are using.

The synchronous operation of the JK flip-flop is summed up in the truth table below. Note that only the normal (Q) output condition is shown, but it is given twice, once prior to a clock pulse (t) and then after one clock pulse (t + 1). The output state X can represent either set (1) or reset (0).

INPUTS		OUTPUTS	
J	K	Q (t)	Q (t + 1)
0	0	X	X
0	1	X	0
1	0	X	1
1	1	X	$\overline{X}$

Refer to the truth table.

What happens when the J and K inputs are both low and a repetitive clock signal is applied?

A. The flip-flop complements.
B. The flip-flop state doesn't change.
C. The flip-flop is reset.

52. (B. The flip-flop state doesn't change) The clock can change all it wants to but it will not affect the state of the flip-flop when both J and K inputs are low. The flip-flop simply retains its previous condition which can be either set or reset. This is an inhibit mode.

INPUTS		OUTPUTS	
J	K	Q (t)	Q (t + 1)
0	0	X	X
0	1	X	0
1	0	X	1
1	1	X	$\overline{X}$

According to the truth table above, how does the flip-flop get reset?

A. J input = 0, K input = 1.
B. Apply binary 0 to the C input.
C. Let the clock toggle it.

53. (A. J input = 0, K input = 1) To reset the JK flip-flop, apply a 0 to the J input and a 1 to the K input then apply a clock pulse. The flip-flop will reset. To set the JK flip-flop you apply a 1 to J and 0 to K and again apply a clock pulse. The flip-flop will set on the trailing edge of the clock.

What happens when both J and K inputs are high and a clock pulse is applied?

A. The flip-flop is set.
B. The flip-flop complements.
C. The flip-flop is inhibited.

54. (B. The flip-flop complements) With the J and K inputs at binary 1, the flip-flop toggles or complements each time the clock switches from 1 to 0. The flip-flop acts as a 2 to 1 frequency divider. Modern integrated circuit flip-flops are available in a variety of configurations. Some ECL flip-flops can toggle at rates as high as 1 GHz.

That completes the basic operation of a JK flip-flop. The symbol used to represent it is shown in Figure 6-40.

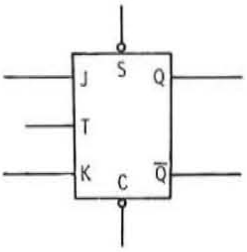


Figure 6-40

As a final check of your understanding of this important device, consider the input waveforms shown in Figure 6-41.

Which output waveform is produced by this set of inputs?

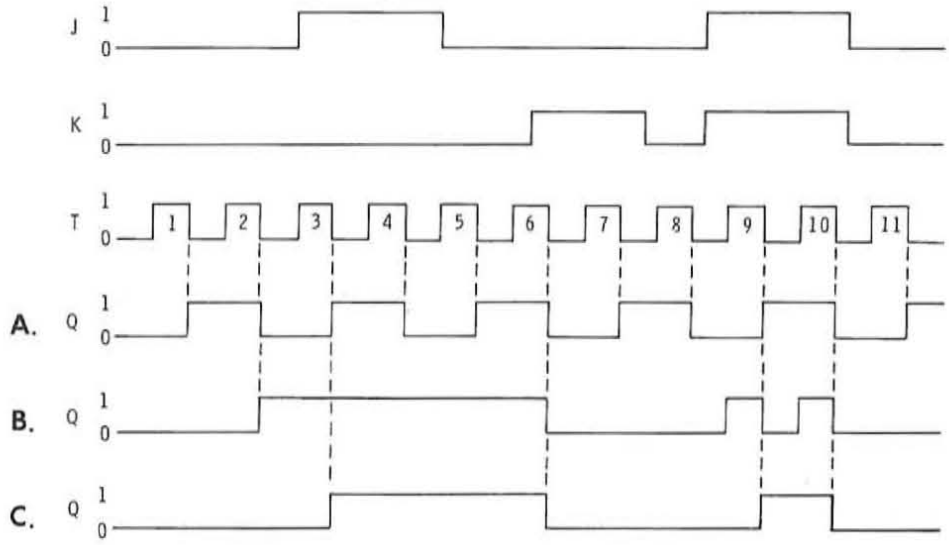


Figure 6-41

55. (C) Good work. You seem to have the idea. The J and K inputs affect the flip-flop state, but state changes occur only on the 1 to 0 transition of the clock pulse. This is synchronous operation.

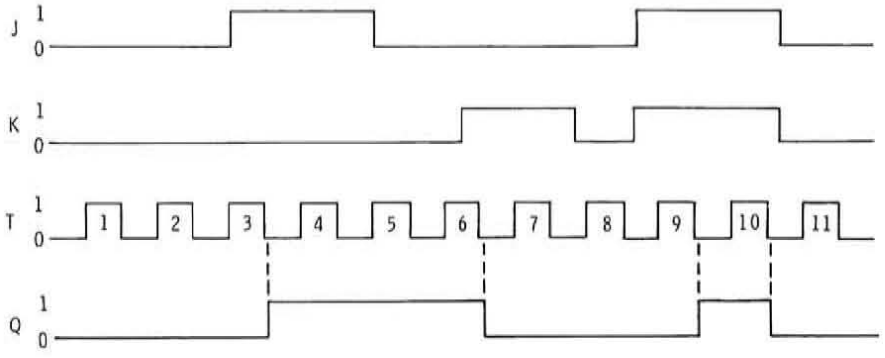


Figure 6-42

In Figure 6-42, the normal output of the flip-flop is low prior to the occurrence of the first clock (T) pulse. Pulses 1 and 2 occur but since both the J and K inputs are low, the flip-flop is inhibited and no state change takes place. Then, the J input goes high. On the trailing edge of the next clock pulse (3), the flip-flop sets. When pulse 4 occurs, J is still high so the flip-flop would be set again. However, it is already set. The J input goes low, then clock pulse 5 occurs. With both J and K low, the trailing edge of pulse 5 has no effect. The flip-flop remains set. Next, the K input goes high and J remains low. On the occurrence of the 1 to 0 transition of pulse 6, the flip-flop resets. Pulse 7 tries to reset it again. The K input goes low. Pulse 8 occurs and since J and K are low, the flip-flop remains reset. The J and K inputs go high simultaneously. Pulses 9 and 10 then toggle or complement the flip-flop, 9 setting it and 10 resetting it. After this J and K go low inhibiting the flip-flop. Pulse 11 has no effect.

The JK flip-flop is highly versatile. They are widely used in storage registers, shift registers, frequency dividers and counters. You will learn more about each of these circuits in a later unit.

Answer the Self Test Review questions and perform Experiment 11.

Self Test Review

17. The asynchronous inputs to a JK flip-flop are designated:
    a. J and K
    b. S and C
    c. Q and $\overline{Q}$
    d. T
18. The JK flip-flop operates as a NAND latch when which inputs are used?
    a. S and C
    b. J and K
    c. T
    d. none of the above
19. On a JK flip-flop the S and C inputs are high, the J input is high, the K input is low. What is the state of the flip-flop when one clock pulse occurs on the T input?
    a. reset
    b. set
    c. ambiguous
    d. insufficient information given to determine the state.
20. The state of the JK flip-flop changes when the clock signal on T switches from:
    a. high to low
    b. low to high
    c. either a. or b.
21. The following conditions exist in a JK flip-flop: J = K = 1, S = C = 1, Q = 1, $\overline{Q}$ = 0. What is the binary contents of the flip-flop after three clock pulses occur?
    a. binary 0
    b. binary 1
    c. insufficient data given to determine state.
22. Both J and K inputs are held low. The S and C inputs are high. The Q output is 0. What is the state of the flip-flop after three clock pulses?
    a. binary 0
    b. binary 1
    c. insufficient information given.

23. Which of the following conditions will reset a JK flip-flop? (indicate all choices that apply)
    a. J = 1, K = 0, S = 1, C = 1, T changes
    b. J = 1, K = 1, S = 1, C = 1, T changes
    c. J = 0, K = 1, S = 1, C = 1, T changes
    d. J = 0, K = 0, S = 1, C = 0, T changes
    e. J = 1, K = 1, S = 0, C = 1, T changes
    f. J = 1, K = 0, S = 0, C = 0, T changes
24. Disregarding the S and C inputs, a JK flip-flop changes state when
    a. J changes
    b. K changes
    c. J and K change
    d. when T switches from 1 to 0.
25. In a JK flip-flop, J = K = 1, S = C = 1. The T input is a 330 KHz square wave. The Q output is a
    a. binary 0
    b. binary 1
    c. 165 KHz square wave
    d. 330 KHz square wave.
26. In a JK flip-flop, J = K = 1, S = C = 1. The T input is at 2 MHz with a duty cycle of 30 percent. What is the frequency and duty cycle of the Q output?
    a. 2 MHz, 30 percent
    b. 2 MHz, 15 percent
    c. 1 MHz, 15 percent
    d. 1 MHz, 30 percent
    e. 1 MHz, 50 percent.

NOTE: The duty cycle is the ratio of the pulse on (binary 1) time to the period of the signal times 100 percent

$$\text{percent duty cycle} = \frac{\text{pulse on time}}{\text{period}} \times 100 \quad (\text{period} = 1/f)$$

27. A JK flip-flop could be used for switch contact bounce buffering
    a. True
    b. False

Answers

17. b. S and C
18. a. S and C
19. b. set
20. a. high to low (1 to 0)
21. a. binary 0. With J = K = 1 the flip-flop will toggle or complement. The flip-flop is initially set. The first clock pulse toggles the flip-flop to a binary 0, the second to binary 1 and the third back to binary 0.
22. a. binary 0. With J = K = low (binary 0) the flip-flop will not toggle.
23. c. J = 0, K = 1, S = 1, C = 1, T changes (synchronous)
    d. J = 0, K = 0, S = 1, C = 0, T changes (asynchronous)
24. d. when T switches from 1 to 0
25. c. 165 KHz square wave. A JK flip-flop divides by 2.
26. e. 1 MHz, 50 percent. The JK flip-flop divides by 2. The output always has a 50 percent duty cycle (equal binary 0 and binary 1 times) if the T input is a fixed frequency. Regardless of the duty cycle of the input signal, the flip-flop toggles on the 1 to 0 transition making the duration of the set and reset states equal to the period of the input.
27. a. True. Use the S and C inputs.

EXPERIMENT 11

JK FLIP-FLOPS

OBJECTIVES: To demonstrate the operation and characteristics of a JK flip-flop.

Materials Needed:

Heathkit Digital Design Experimenter ET-3200

1 — 7476 TTL IC (443-16)

Procedure

1. Connect the circuit shown in Figure 6-43. Use data switches for the J, K, S, and C inputs. Use logic switch A for the clock T input. Connect

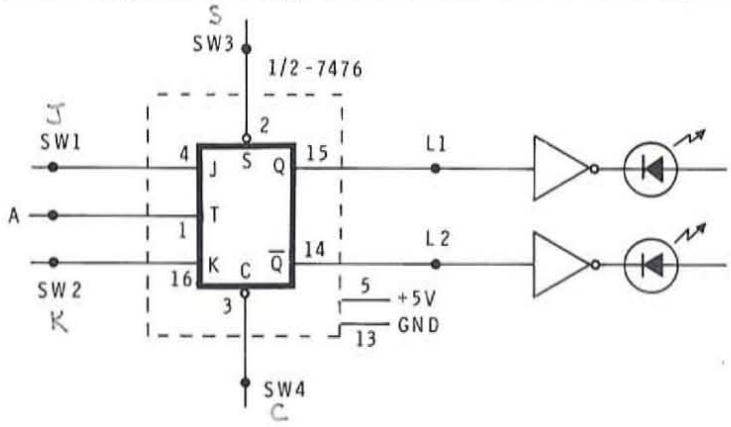


Figure 6-43

LED indicators to each output. The pin connections for 7476 dual JK flip-flop are shown in Figure 6-44. There are two complete JK flip-flops in the 7476 IC, but we will use only one as they are identical. Connect +5 volts to pin 5 and GND to pin 13.

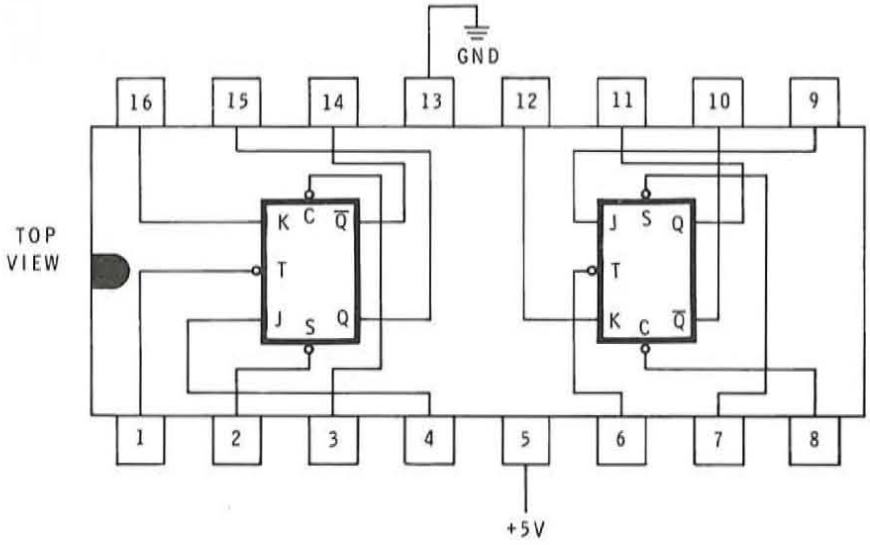


Figure 6-44
Pin connections for dual TTL JK flip-flop 7476.

2. First you will check the asynchronous operation of the JK flip-flop. Set J = K = 1 with SW1 and SW2. Apply the levels indicated in Table I to the S and C inputs. Note the output states and record them in Table I. Repeat this step with J = K = 0. Note the result.

TABLE I

INPUTS		OUTPUTS	
S	C	Q	$\overline{Q}$
1	1	1	0
0	1	1	0
1	0	0	1
0	0	1	1

Do the JK inputs affect the asynchronous operation? No.

3. Next, verify the synchronous operation of the JK flip-flop. Set the S and C inputs to binary 1. Then apply the logic levels indicated in Table II. Note the normal output state before (Q) and after [Q (t + 1)] the application of a single clock pulse from the A logic switch. After you have completed Table II, repeat the inputs given and toggle the clock (T) input several times with the A logic switch for each set of inputs. Note the results on the LED logic indicators.

TABLE II

INPUTS		OUTPUTS	
J	K	Q	Q (t + 1)
0	0	0	0
0	1	0	1
1	0	1	0
1	1	0	1

NOTE:Q (t +1) means the state of the Q output after the application of one clock pulse with the given inputs.

4. Set the J and K inputs to binary 1 with the logic switches. Remove the A logic switch from the T input and connect a 1 Hz clock (CLK) signal to it. Also connect a LED logic indicator to the CLK signal. Observe the CLK input and Q and $\overline{Q}$ outputs on the LED indicators. Note the relationship between input and output frequencies.
5. Construct the circuit shown in Figure 6-45. The circuit will be driven from the 1 Hz CLK signal. The A and B logic switches will control the circuit. You will observe the output states on LED indicators L1, L3 and L4.

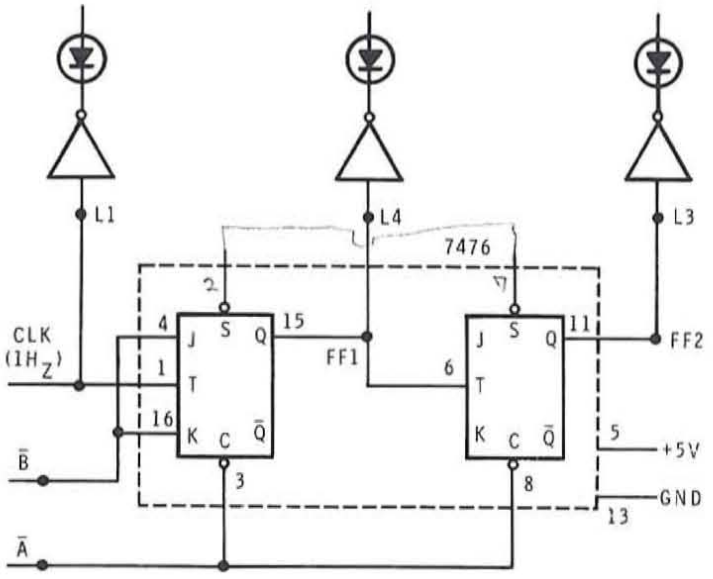


Figure 6-45

6. Observe the relationship between the input (L1) and output (L3 and L4) waveforms. You can do this by counting the number of input and output pulses. Sketch a timing diagram illustrating this relationship.
7. While the circuit is operating, depress the B logic switch. What effect does this have on the circuit? (Note the output states). Release the B switch. Repeat this step several times.
8. Depress the A logic switch while the circuit is operating. Note the effect on the outputs. Repeat several times.

NOTE: If you have an oscilloscope, set the CLK frequency to 1 KHz or 100 KHz and observe CLK, FF1 and FF2 noting their frequency relationship.

DISCUSSION

In Steps 1 and 2 you verified the operation of the JK flip-flop in the asynchronous mode. This refers to the use of the set (S) and clear (C) or reset inputs to control the state of the flip-flop. From the data you recorded in Table I, you should have found that the JK flip-flop functions just like a NAND latch when the S and C inputs are used. With both inputs binary 1, the flip-flop can be in either state. When C is low and S is high, the flip-flop is reset. With C high and S low, the flip-flop is set. If both S and C are low, the ambiguous state ($Q = \overline{Q} = 1$) occurs.

In Steps 3 and 4 you verified the synchronous operation of the JK flip-flop. Your data in Table II should be identical to that given earlier in Frame 51. The most important points to note are:

1. It is not the JK inputs that cause the state of the flip-flop to change. It is the T input 1 to 0 transition that causes the state change. The J and K inputs do determine the state to which the flip-flop goes but not *when* it changes.
2. The flip-flop toggles or complements each time a 1 to 0 change occurs on the T input with J and K = 1.
3. The flip-flop does not toggle when a clock pulse occurs if J = K = 0. This makes the JK inputs useful as a toggle inhibit control.
4. For every two binary 1 input pulses on T, one binary 1 pulse occurs at the Q output. This indicates a two to one frequency division.

In Step 5 you cascaded to JK flip-flops and in Step 6 you determined the input-output relationships. By observing the LED indicators you should have found that for every four binary 1 clock input pulses there were two pulses from FF1 and one pulse from FF2. This indicates that each flip-flop divides the input frequencies by 2. The overall circuit, both flip-flops together, divides by 4. The input is 1 Hz. The output of FF1 is .5 Hz and the output of FF2 is .25 Hz. Your input-output waveforms should appear as shown in Figure 6-46.

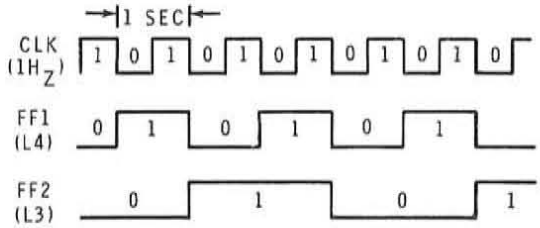


Figure 6-46

In Step 7 you used the B logic switch to control the JK inputs to FF1. With the switch in its normal up position, the $\overline{B}$ output is binary 1. Therefore, the JK inputs are binary 1 and the flip-flop toggles with each clock pulse. When you depress the B logic switch, $\overline{B}$ goes low. This inhibits FF1. The clock pulses will not affect it with J = K = 0. It will simply retain the state to which it was set by the last clock pulse prior to the JK inputs becoming low. Since FF1 does not toggle, FF2 will not toggle. The input to FF2 comes from FF1. As a result, when the JK inputs on FF1 go low, the clock pulse has no effect and the flip-flop states can be anything.

When you depress the A logic switch you reset both flip-flops. With the A logic switch in its normal up position, the $\overline{A}$ output is high. This puts a binary 1 on both C inputs. This will not affect the flip-flop states. When you depress the A logic switch, the $\overline{A}$ output goes low. This resets both flip-flops immediately. Regardless of the states of the flip-flops, when you depress A, both will be put into the binary 0 condition. You will note that this reset state overrides the clock signal. With the C inputs low, the clock input has no effect. In a JK flip-flop, the asynchronous inputs always take precedence over the synchronous inputs.

EXAMINATION

UNIT 6

FLIP-FLOPS AND REGISTERS

The purpose of this exam is to help you review the key facts in this unit. The problems are designed to test your retention and understanding by making you apply what you have learned. This exam is not so much a test as it is another learning method. Be fair to yourself and work every problem first before checking the answers.

1. The normal output of a flip-flop is high. What state is the flip-flop in?
   A. Set
   B. Reset
2. The complement output of a flip-flop is low. What binary state is stored in the flip-flop?
   A. binary 0
   B. binary 1
3. A storage register made up of six D-type flip-flops is storing a binary number. The flip-flop states are:
   A — reset, B — set, C — reset, D — reset, E — set, F — set
   The A flip-flop is the LSB.
   The decimal equivalent of the register content is
   A. 16
   B. 19
   C. 36
   D. 50
4. How many JK flip-flops are needed to generate a 125 KHz square wave from a 1 MHz square wave?
   A. 1
   B. 2
   C. 3
   D. 4

5. Draw the normal output of the flip-flop in Figure 6-47 given the input waveforms shown.

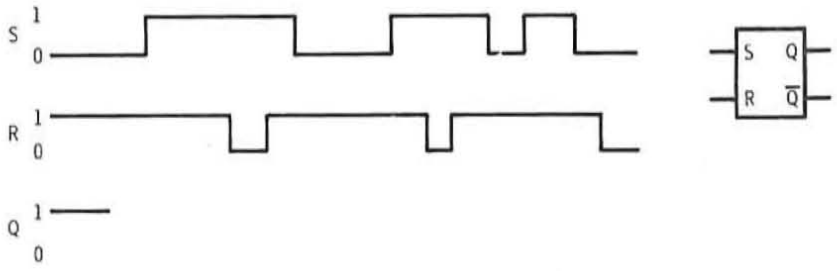


Figure 6-47

6. Draw the normal output of the flip-flop in Figure 6-48 given the input waveforms shown.

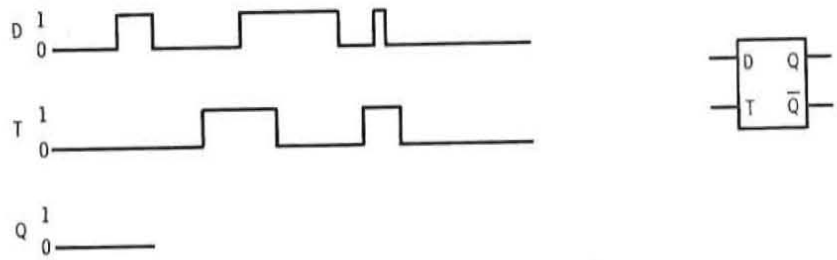
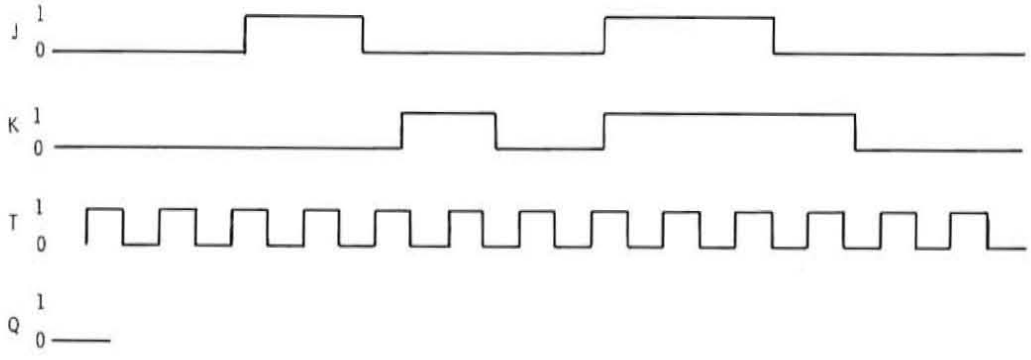


Figure 6-48

7. Draw the normal output of the flip-flop in Figure 6-49 given the input waveforms shown.



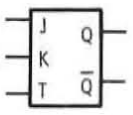


Figure 6-49

8. Which of the following ways can a JK flip-flop be set? Check all that apply.
   A. Ground the C input
   B. Ground the S input
   C. Set J to 0 and K to 1 and apply a clock pulse
   D. Set J to 1 and K to 0 and apply a clock pulse
   E. Toggle the T input with J = K = 1.
9. How many flip-flops will be needed to store the binary equivalent of the decimal number 114?
   A. 3
   B. 7
   C. 12
   D. 57
10. A flip-flop is the basic logic element in what type of logic circuit?
   A. sequential
   B. combinational
11. The trailing edge of a logic signal generally refers to its transition from
   A. 0 to 1
   B. 1 to 0
   C. either a. or b.
12. For a JK flip-flop to work properly in its synchronous mode, the S and C input states must be
   A. S = 0, C = 0
   B. S = 0, C = 1
   C. S = 1, C = 0
   D. S = 1, C = 1
13. When the T input to a D flip-flop is high and the D input is a logic signal X, the complement output is
   A. binary 0
   B. binary 1
   C. $\overline{X}$
   D. X
14. The basic application of the D flip-flop is
   A. Switch contact debouncing
   B. Registers
   C. Frequency division
   D. Counting.
15. Which type of flip-flop does *not* have an ambiguous state
   A. RS
   B. D
   C. JK

ANSWERS

UNIT 6

FLIP-FLOPS AND REGISTERS

1. A — set
2. B — binary 1
3. D — 50 The number in the register is 110010.
4. C — 3 A 1 MHz (1000 kHz) signal must be divided by 2 three times to generate a 125 KHz signal. (1000 ÷ 2 = 500 ÷ 2 = 250 ÷ 2 = 125)
5. See Figure 6-50 RS or latch flip-flop.

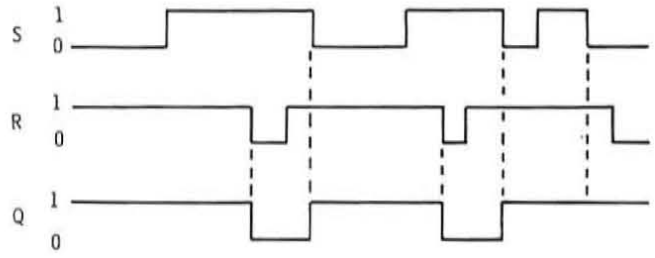


Figure 6-50

6. See Figure 6-51 D flip-flop.

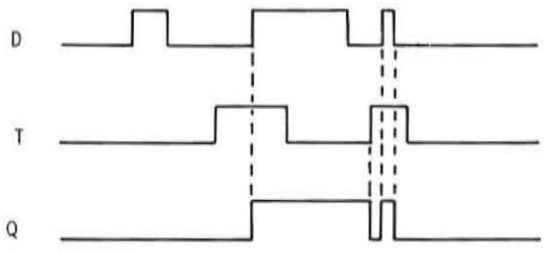


Figure 6-51

7. See Figure 6-52 JK flip-flop.

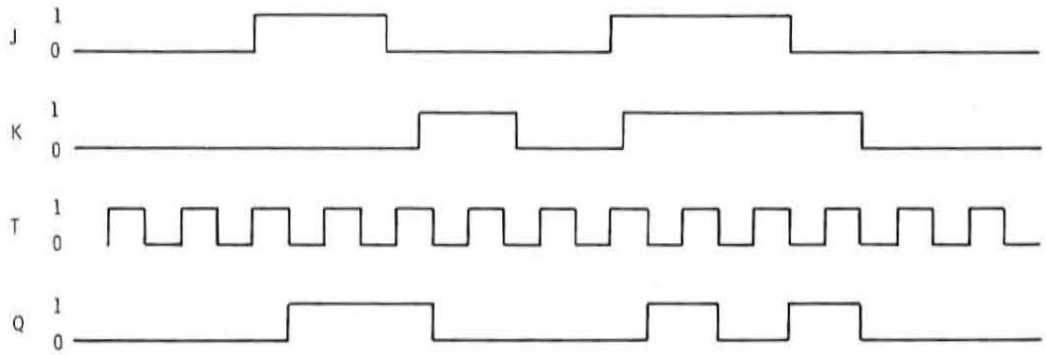


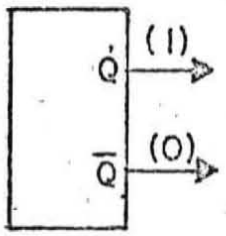
Figure 6-52

8. B,D,E — Either of these methods can be used to set a JK flip-flop.
   B — Ground the S input.
   D — Set J to 1 and K to 0 and apply a clock pulse.
   E — Toggle the T input with J = K = 1.
9. B — 7 It takes 7 bits to represent the decimal number 114 in binary. $114_{10} = 1110010_2$.
10. A — sequential. The basic characteristic of a sequential circuit is storage or memory of binary data which is the basic function of a flip-flop.
11. B — 1 to 0 The 1 to 0 transition is the trailing edge of a logic signal.
12. D — S = 1, C = 1
13. C — $\overline{X}$. The normal output follows the D input, therefore the complement output is the complement of the D input when T is high.
14. B — Registers
15. B — D type flip-flop does not have an ambiguous state.

6.4 FLIP-FLOPS

A flip-flop is an electronic circuit capable of storing a binary bit (ONE or ZERO). It is also known as a bi-stable multivibrator or latch. Flip-flops have two stable states. One state is called the "SET" state, and the other state is the "RESET" or "CLEARED" state. A flip-flop can be in only one of its stable states at a time. Therefore, a flip-flop is either set or reset (cleared).

Flip-flops have two outputs called Q and $\overline{Q}$ which are sometimes referred to as "1" and "0" output respectively.



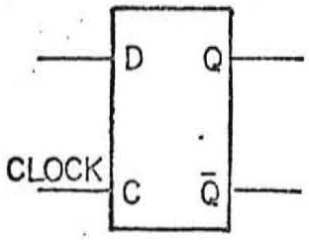
The levels on the output lines depends upon the state of the flip-flop as illustrated in the following chart.

STATE	Q(1)	$\overline{Q}$(0)
Set	H	L
Reset	L	H

You're probably wondering why nothing has been mentioned about the flip-flop inputs. The inputs vary with the different type flip-flops as described in the following paragraphs.

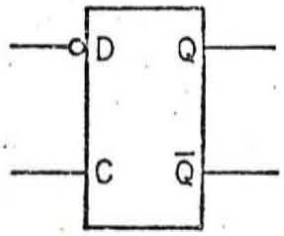
6.4.1 "D" Type Flip-Flop

A "D" type flip-flop will set or reset depending upon the state of the "D" input when a clock pulse occurs.

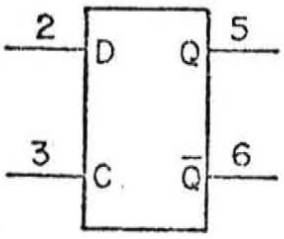


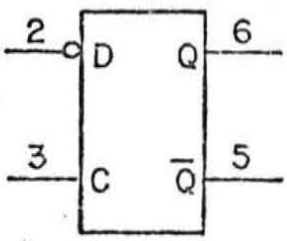
In the above illustration, the "D" input is examined on the positive going edge (⌐) of the C (clock) input. When D is high, the flip-flop sets and "D" input low resets the flip-flop.

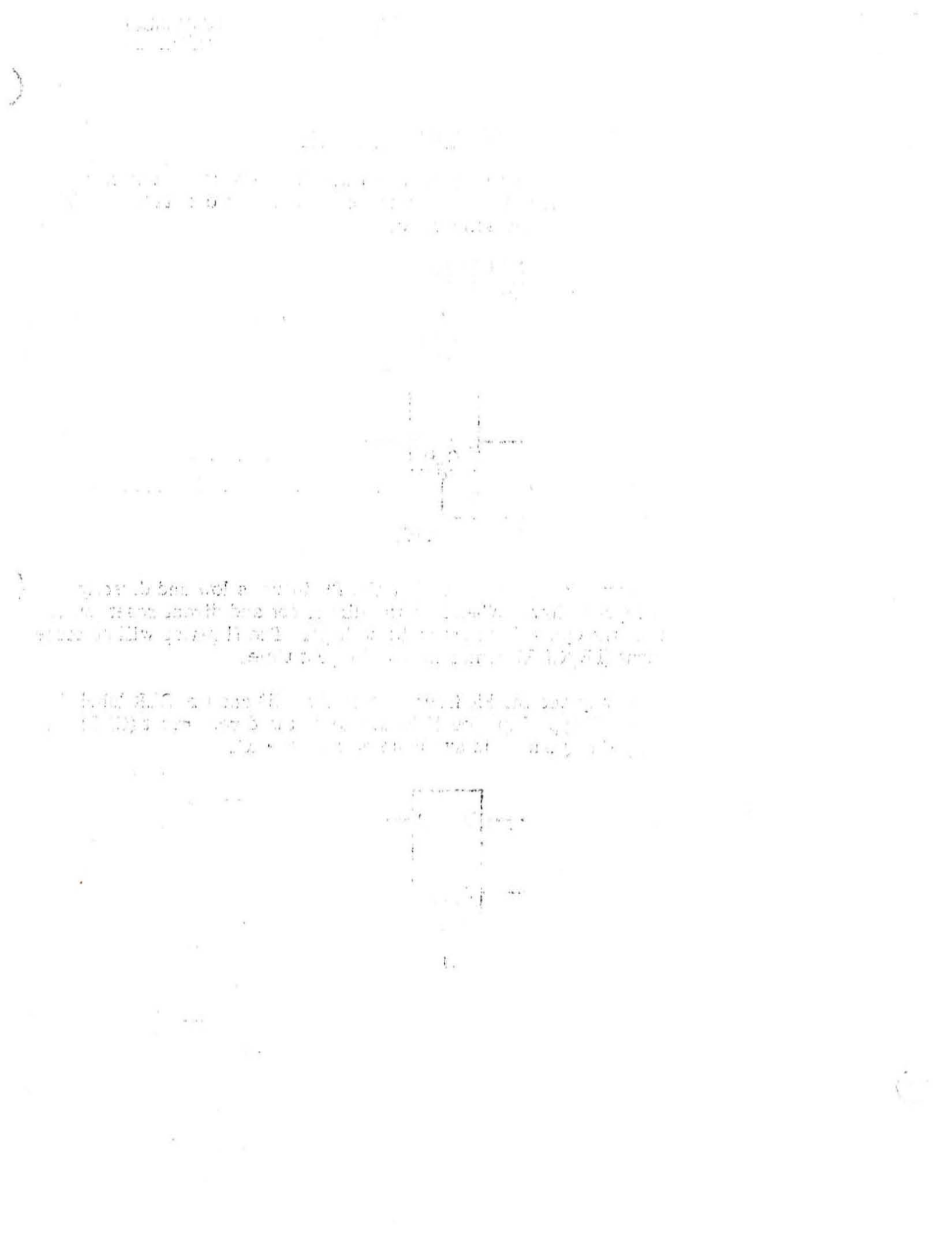
At times the "D" flip-flop may be illustrated as follows:



This indicates the flip-flop sets if the "D" input is low on the positive going edge of clock. In actual application the Q and $\overline{Q}$ output leads have been reversed, as shown below. Therefore the flip-flop in reality is reset, but for application purposes, it is set when "D" input is low on a positive going clock.

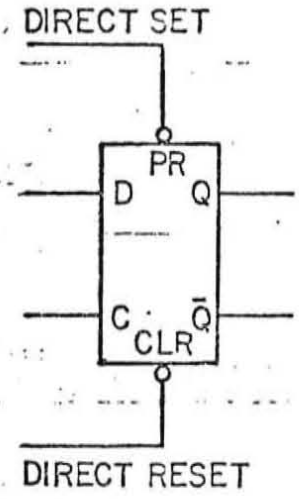






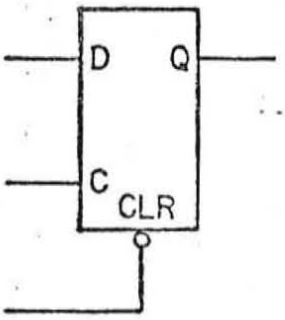
6.4.1.1 "D" Type Flip-Flop with Preset and Clear

A "D" type flip-flop is available with inputs which will directly set or directly reset the flip-flop without a clock input. The direct inputs also override the "D" input and clock when present at the same time.



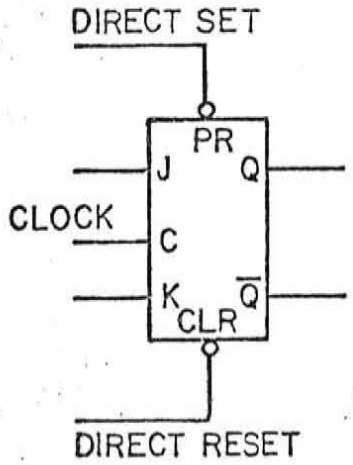
The flip-flop, shown above is directly set when the PR input is low and directly reset when the CLR input is low. When both the direct set and direct reset inputs are low together, both the Q and $\overline{Q}$ outputs will be high. The flip-flop will stabilize in the state of the input (PR/CLR) remaining the longest time.

At times, in logic, you may see the PR input labeled S or SD and the CLR labeled R or CD. Also some "D" type flip-flop IC's have only the direct reset (CLR) input and at times only the Q output is available outside the IC.



6.4.2 J-K Type Flip-Flop

A J-K type flip-flop has an input configuration which allows it to be used in many different ways.

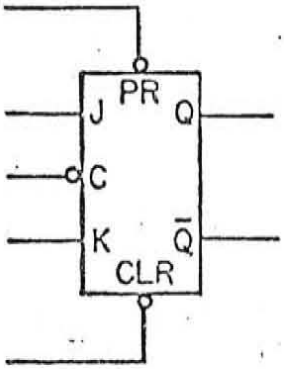


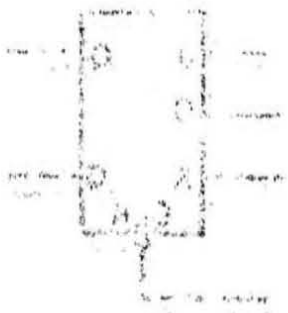
The J-K flip-flop can be directly set or reset by applying a low on the PR or CLR input.

The J-K inputs are examined on the positive going edge of clock with the J-K flip-flop assuming the state as illustrated in the following chart:

J	K	Clk	State
L	L	⌐	Remains in Preset state
L	H	⌐	Resets
H	L	⌐	Sets
H	H	⌐	Toggles to opposite state

J-K flip-flops are also available which examine the J-K inputs on the negative (¬L) going edge of clock.





J-K flip-flops are also available in IC's which have only a preset or a clear input.