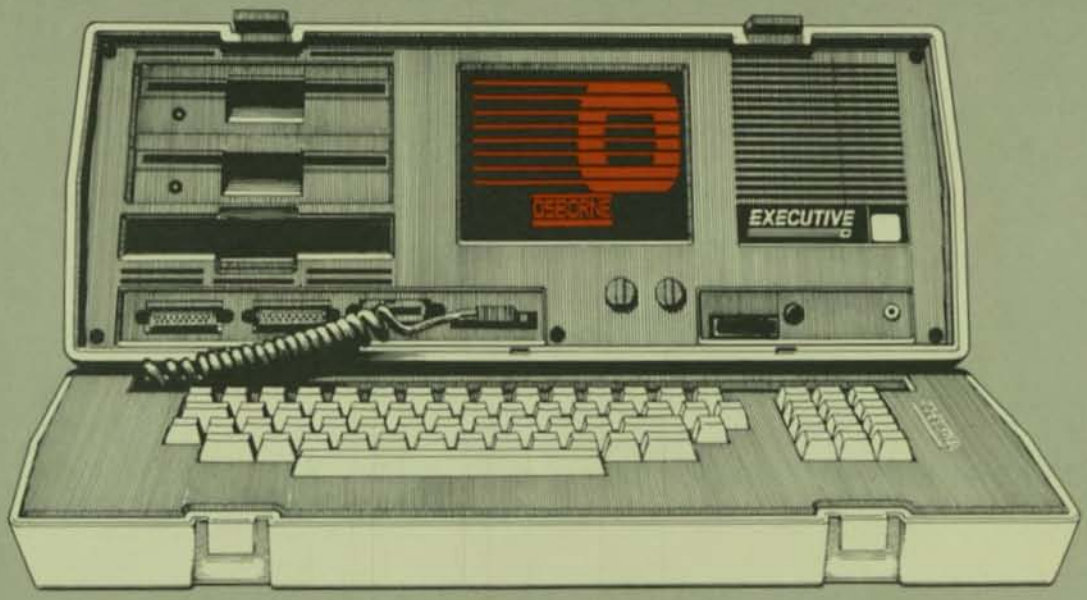
EXECUTIVE™

OSBORNE

Technical Manual



Volume D: Integrated Circuit Specifications

OSBORNE
COMPUTER CORPORATION

OSBORNE EXECUTIVE TECHNICAL MANUAL
VOLUME D: INTEGRATED CIRCUIT SPECIFICATIONS

ABSTRACT

This manual provides the specifications for the six most important integrated circuits contained within the Osborne Executive. Each description includes a functional block explanation, pin definitions, a summary of registers, electrical characteristics, and timing diagrams for critical operations.

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VOLUME D: INTEGRATED CIRCUIT SPECIFICATIONS

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SERIAL INPUT/OUTPUT

General Information

The material within this section covers the Serial/Input Output unit equivalent to the Z80A SIO/2 manufactured by Zilog. The information also applies to those integrated circuits produced by other manufacturers that may have somewhat different nomenclatures, but very similar physical and electrical characteristics.

Feature List

The following list summarizes the most important and salient features of the Z80 Serial Input/Output chip.

Two Full Duplex Communications Channels
Quadruple Buffering of Receive Data Bytes
Double Buffering of Transmit Data Bytes
Data Rates to 550 Kbps @ 2.5 MHz System Clock
Data Rates to 880 Kbps @ 4.0 MHz System Clock
Modem Control I/O-Separated by Channel
Provision for Automatic Interrupt Vectoring
Synchronous, Isosynchronous, Asynchronous Operation
HDLC, IBM SDLC Compatibility
All I/O Pins are TTL-Compatible
Single +5-Volt Supply
40 Pin Dual In-Line Package
Single Phase 5-Volt Clock

Block Diagram and Pin Assignment

Figure D-1 is a block diagram representation of the functions contained within the SIO. Figure D-2 is a drawing of the actual DIP pin assignments.

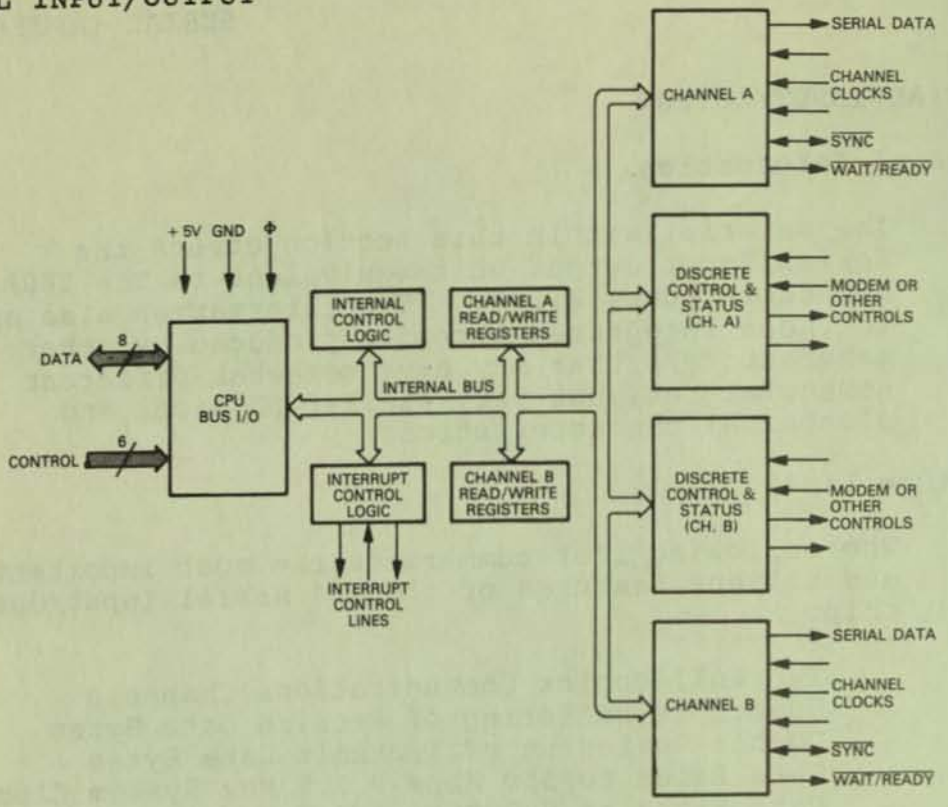


FIGURE D-1. SIO BLOCK DIAGRAM

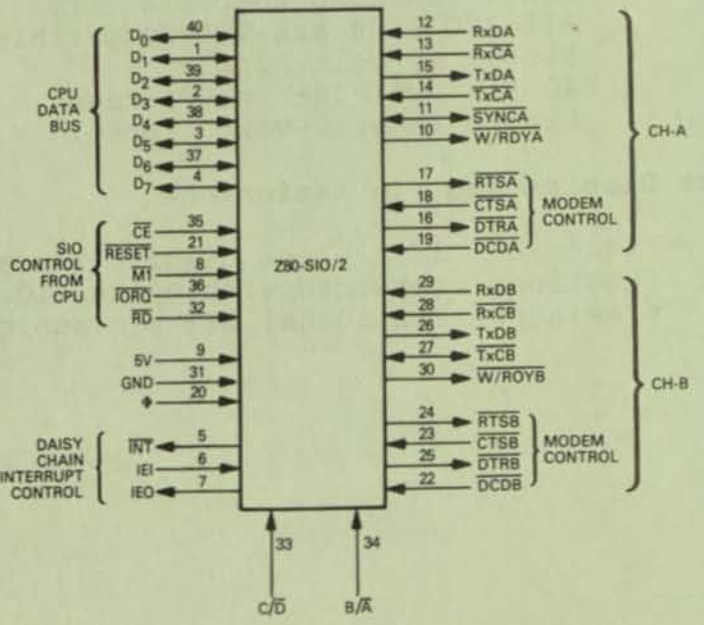


FIGURE D-2. SIO PIN ASSIGNMENTS

Overall Description

The SIO is a programmable serial communications device that allows microcomputer systems to meet widely varying data communications requirements. The SIO contains two complete, independent communications channels in one package and can handle both synchronous data (data accompanied by clock) and asynchronous data (data with no clock). The SIO converts incoming serial data to parallel bytes for the host processor and converts parallel bytes from the host to outgoing serial data.

The SIO is able to meet a variety of serial communications protocols, such as IBM Bisync, IBM SDLC, and HDLC. The SIO will also support many other protocols to allow communication with such devices as cassette and floppy disk interfaces.

Data error checking is important in data communications environments and the SIO can generate and check error codes in the synchronous mode for this purpose. It also provides error status bits that may be read and acted upon by the host processor.

There is also provision for interfacing to a modem through the modem control lines. If a modem is not used, these lines may be used for general-purpose I/O.

The SIO consists of the following functional blocks:

Bus I/O
Internal Control Logic
Interrupt Control Logic
Channel A,B Read/Write Registers
Channel A,B Serial I/O
Channel A,B Control and Status

Pin Description

Table D-1 summarizes the function of each pin of the SIO.

Table D-1. SIO Pin Functions

Pin	Mnemonic	Function
1-4 37-40	D0 - D7	**Data Bus.** This eight bit bidirectional data bus allows data and commands to be transferred between the host processor and the SIO.
5	INT*	**Interrupt Request.** When the SIO is interrupting the host, this line goes low.
6	IEI	**Interrupt Enable In.** When there are two or more interrupting devices, this line is used in conjunction with IEO to provide a daisy-chained interrupt priority structure. A high level indicates that higher-priority interrupting device is being serviced.
7	IEO	**Interrupt Enable Out.** This signal is used in conjunction with IEI to provide a daisy-chained priority interrupt structure. This signal is high only if IEI into the SIO is high and the SIO is not in the process of being serviced for an interrupt it gave to the host CPU. It is low if there is any higher priority device being serviced or if the SIO itself is being serviced. In this way, a higher-priority device locks out all lower-priority devices.
8	M1*	**Machine Cycle One.** When the Z80 is fetching an instruction, M1* and RD* are active low. However, if M1* and IOREQ* are both active low, the SIO interprets this as an interrupt acknowledge from the Z80 if the SIO is the highest-priority interrupting device at the moment (IEI is high).
10,30	W*/RDYA,B*	**Wait/Ready A,B.** These lines serve either one of two purposes: They can serve as Wait outputs to synchronize the host CPU to the SIO data rate, or they may be programmed to act as Ready lines for a DMA controller.

Note: An asterisk (*) denotes an active-low signal.

Table D-1. SIO PIN FUNCTIONS (Cont.)

11	SYNCA	**Synchronization A.** This signal is bidirectional. It serves as an input while the SIO is operated in the asynchronous or external sync modes. In the asynchronous mode, it acts as a modem control input similar to CTS* and DCD*. In the external sync mode, it acts as an input that is driven low by external logic on the second rising edge of RXCA* after the edge of RXCA* on which the last bit of a sync character was detected. This signal, when used in the external sync mode, should be kept low until the sync status changes. In the internal sync mode (Monosync and Bisync), this pin acts as an output that goes low each time a sync character is recognized.
12,29	RXDA,B	**Receive Data A, B.** These are the serial data input signals for the two channels.
13,28	RXCA,B*	**Receive Clock A, B.** These clock inputs determine the receive data rate. In synchronous mode the clocks must run at the baud rate desired. In the asynchronous mode, they may be run at 1, 16, or 64 times the desired baud rate. Receive data is sampled on the rising edge of Receive Clock.
14,27	TXCA,B*	**Transmit Clock A, B** These clock inputs determine the transmit data rate. In synchronous mode the clocks must run at the baud rate desired. In the asynchronous mode, they may be run at 1, 16, or 64 the baud rate, but the clock rate multiplier must be the same for both the transmitter and the receiver. Transmit data changes on the falling edge of transmit clock.
15,26	TXDA,B	**Transmit Data A,B.** These are the serial transmit data output signals for the two channels.
16,25	DTRA,B*	**Data Terminal Ready A,B.** These are outputs which are programmed to a high or low state by system software. They can either be used as modem control or general-purpose outputs.

Note: An asterisk (*) signifies that the signal is active low.

Table D-1. SIO PIN FUNCTIONS (Cont.)

17,24	RTSA,B*	**Request to Send A,B.** This bit is used as a modem control signal and is controlled by software. It may also be used as a general-purpose output. When operating in the asynchronous mode, the RTS* output is set low according to the software bit with no delay. However, when the software sets the bit high, the RTS output does not go high until the transmitter is empty. In the synchronous mode, the RTS output follows the software bit exactly.
18,23	CTSA,B*	**Clear to Send A,B.** These inputs may be programmed as either Auto Enable or general-purpose inputs. When used in the Auto Enable mode a low on the respective input enables the appropriate transmitter. The SIO generates an interrupt to the host processor when the CTS* input makes a transition in either direction.
19,22	DCDA,B*	**Data Carrier Detect A,B.** These inputs are similar to the CTS* inputs, except they may be used to enable the receiver channels.
20	CLK	**System Clock.** This is a single phase clock that the SIO uses to generate and synchronize all its internal timing signals.
21	RESET*	**Reset.** This signal resets the SIO internal registers and disables both the receivers and transmitters. It also disables interrupts, forces the transmit outputs to the high state, and forces all the modem control outputs high.
32	RD*	**Read.** This is an input which is used to cause the SIO to read data and commands issued to it by the host processor. When active, it means that either a memory or I/O cycle is in process.
33	C/D*	**Control/Data Select.** This line, when high, allows control information to be written to the SIO from the host. When C/D* is low, data may be transferred to and from the SIO.

Note: An asterisk (*) denotes an active-low signal.

TABLE 1. SIO Pin Functions (Cont.)

34	B/A*	**Channel B/A* Select.** This line, when high, selects Channel B as the channel over which data is to be transferred to or from the CPU. When B/A* is low, Channel B is selected.
35	CE*	**Chip Enable.** When low, this input allows the SIO to transfer data and commands between itself and the host.
36	IORQ*	**Input/Output Request.** This signal is used to transfer data and commands between the SIO and the host. When IORQ*, CE*, and RD* are all low, a read operation occurs in which data is transferred from the SIO to the CPU. When the CE* and IORQ* lines are low and the RD* line is high, a write operation takes place in which data or command information, as determined by C/D*, is transferred from the CPU to the SIO.

Note: An asterisk (*) denotes an active low signal.

Hardware Functional Description

Bus I/O

The Bus I/O section of the SIO provides the basic interface between the host CPU and the SIO for the transfer of data and command information. This transfer of information can be controlled in one of three ways:

1. Polling
2. Block Direct Memory Access (DMA) Transfer
3. Interrupts

Polling

The SIO has two internal read registers, Read Register Zero (RR0) and Read Register One (RR1), in which are contained status bits that indicate that a receive byte or transmit byte needs to be transferred. There are also error status bits contained in these registers for use by the program. The interrupt capability of the SIO must be disabled in order for it to be used in the polled mode.

Block DMA Transfer

The SIO has an internal write register, Write Register One (RR1), that has Wait/Ready bits that are used along with the W*/RDY* line of the device to allow interfacing to a DMA Controller or CPU in a block transfer mode. This output line of the SIO can be defined by software to be a READY* signal for use by a DMA Controller or it can be defined to be a WAIT* line for use by a CPU. When interfacing to a CPU, the WAIT* line indicates to the CPU to extend its I/O cycle. The READY* line is used when interfacing with a DMA Controller to indicate readiness of the SIO to transfer data to or from memory.

Interrupt Transfer

Interrupt transfers are typically used when there is a need to conserve real time. The SIO is capable of interrupting the host upon any of the following conditions:

The SIO is Ready to Transmit a Character
The SIO Has Received a Character
Sync or Status Changes

When an interrupt occurs, the CPU needs an interrupt vector so it knows where to go to get the interrupt service routine. Write Register Two (WR2) and Read Register Two (RR2), located only in Channel B register space, contain this interrupt vector value. Under program control, this vector can be changed to point to any one of eight interrupt-service routines.

When the SYNC*, CTS*, or DCD* pins undergo any transition, an interrupt is generated. An interrupt is also generated if it is detected that there has been a break in the data stream in the asynchronous mode or an abort condition in the SDLC synchronous mode.

The SIO is programmable to allow several conditions at the receiver to cause an interrupt. Interrupts may be generated on the first character received, all characters received, or on special receive conditions.

Internal Control Logic

The Internal Control Logic is responsible for generating all internal address, control, and timing signals. When a read or write cycle is to be performed on the SIO, this logic orchestrates and supervises the overall signal generation.

Interrupt Control Logic

This part of the SIO is responsible for monitoring all the conditions that can cause an interrupt, and starting into motion the appropriate signals that result in a correct, prioritized interrupt to the CPU when enabled to do so.

Channel A, B Read/Write Registers

The SIO contains eight write registers, WR0 - WR7, and three read registers, RR0 - RR2. These registers are configured by appropriate system software to put the SIO into the mode of operation desired for the particular application.

A summary of the function of each register is given below:

WR0-- Register Pointers, CRC, Initialization Commands
WR1-- Tx/Rx Interrupt and Data Transfer Mode
WR2-- Interrupt Vector (Channel B Only)
WR3-- Receive Controls
WR4-- Tx/Rx Controls
WR5-- Transmit Controls and Parameters
WR6-- Sync Character or SDLC Address Field
WR7-- Sync Character or SDLC Flag
RR0-- Tx/Rx Buffer, External, and Interrupt Status
RR1-- Special Receive Condition Status
RR2-- Channel B Modified-Interrupt Vector

These registers will be discussed more in-depth in the Software Information section.

Channel A, B Serial I/O

The Serial I/O portion of the SIO provides the serial-to-parallel and parallel-to-serial interface between the CPU and the data communications channel.

Receiver Logic

Serial data flows into the receiver logic in several different ways, depending on how the SIO has been programmed. If the SIO is being operated in the synchronous mode, the SIO must establish that synchronization has taken place before accepting data and transferring that data to the host. If the SIO has been programmed for Monosync, a match must be made between incoming data and a single sync character stored in W7. If Bisync has been programmed, a match must be made with two separate sync characters, stored in WR6 and WR7. Once synchronization is established, incoming data is no longer matched against the sync register(s).

If the SDLC mode has been programmed, the SIO performs zero deletion; that is, if the sixth bit is a zero following five ones in a row, the zero is deleted from the data stream. If the sixth bit is a one instead of a zero, the seventh bit is examined and is determined to indicate an abort sequence if a one, and a flag sequence if a zero. In order to sync on SDLC data, the SIO looks for a match between incoming data and the flag character, which is stored in WR7.

In the asynchronous mode, data is routed through an eight-bit shift register if its bit length has been programmed to be five or six bits. If the bit length is seven or eight bits, the data is routed through an additional three-bit shift register first.

The SIO performs a Cyclic Redundancy Check (CRC) on received data. This may be done for both synchronous and SDLC data. The SIO provides an eight-bit delay in the synchronous mode and no delay in the SDLC mode. The eight-bit delay is to allow the CPU to decide which bytes to include in the CRC check. For SDLC, no delay is needed since the SIO has internal logic which determines which bytes to include in the CRC calculation for SDLC.

Transmitter Logic

The transmit logic of the SIO allows both synchronous and asynchronous data to be transmitted. When transmitting asynchronous data, the SIO appends the proper parity, start, and stop bits to the data stream. The data is shifted out from the parallel, eight-bit transmit register at the appropriate rate.

In order to transmit synchronous data, the SIO must first send one sync character (Monosync) or two characters (Bisync) at the beginning of the data.

This is done by placing the sync characters from WR6 or WR7 into the transmit shift register. These characters are then shifted out first before the actual data. In the SDLC mode, the flags are loaded into the shift register at the beginning and end of messages. A CRC generator allows real-time CRC generation.

SDLC and HDLC data is shifted out through zero insertion logic, which appends a zero to a field of five consecutive ones.

Channel A, B Control and Status

The SIO maintains internal status registers which are available to the CPU. Parity, overrun, and framing errors are detected and reported to the CPU.

The SIO also allows manipulation of several modem control signals so that interfacing to a modem is a simple task.

Timing Information

Four types of timing cycles important to the operation of the SIO will be explained below.

Read Cycle

Figure D-3 illustrates the timing relationships involved in reading a status or data byte from the SIO.

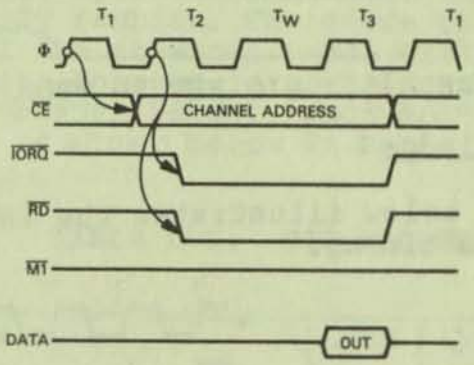


FIGURE D-3. SIO READ CYCLE

Write Cycle

Figure D-4 illustrates the timing for a write cycle to the SIO. A write cycle is necessary in order for data or control information to be loaded into the SIO from the host CPU.

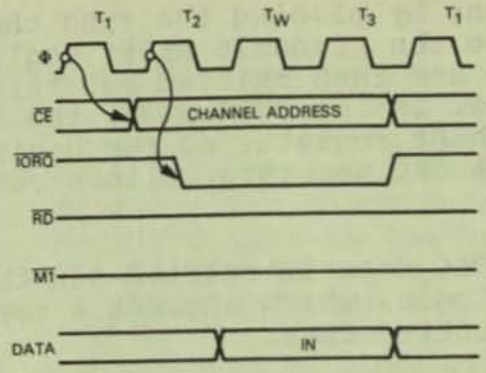


FIGURE D-4. SIO WRITE CYCLE

Return From Interrupt Cycle

Figure D-5 illustrates the return from interrupt timing. The Z80 CPU issues a Return From Interrupt instruction at the end of an interrupt service cycle. This is a two-byte instruction consisting of the bytes hex ED and 4D.

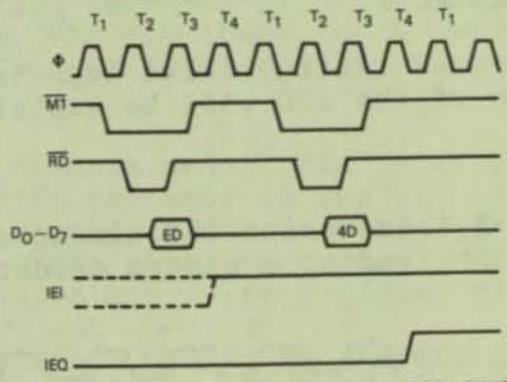


FIGURE D-5. SIO RETURN FROM INTERRUPT

Interrupt Acknowledge

Figure D-6 below illustrates the interrupt acknowledge timing.

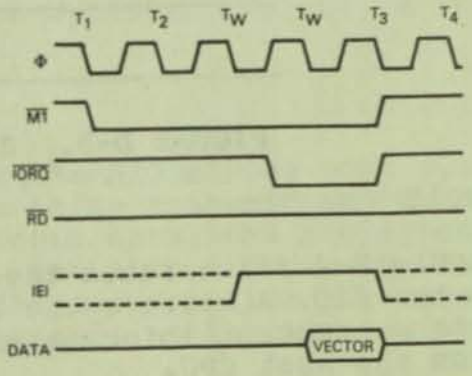


FIGURE D-6. SIO INTERRUPT ACKNOWLEDGE

Electrical Characteristics

Listed below are the DC electrical characteristics of the SIO. These characteristics apply, unless otherwise noted, at an ambient temperature of 0 to 70 degrees Centigrade and Vcc = +5 V, plus or minus 5%.

TABLE D-2. SIO ELECTRICAL CHARACTERISTICS

Parameter	Min	Max	Unit
Clock Input Low (Vilc)	-0.3	+0.45	V
Clock Input High (Vihc)	-0.6	+5.5	V
Input Low (Vil)	-0.3	+0.8	V
Input High (Vih)	+2.0	+5.5	V
Output Low (Vol) (Note: Iol = 2.0 mA)		+0.4	V
Output High (Voh) (Note: Ioh = -250 uA)	+2.4		V
Power Supply Current (Icc)		100.0	mA
Input Leakage Current (Ili)	-10.0	+10.0	uA
Tri-State Output Leakage (Iz)	-10.0	+10.0	uA
Sync Pin Leakage Current	-40.0	+10.0	uA

Software Addressing

The SIO must be programmed by writing to several internal registers. Also, the status information and data transfer operations must be able to take place in an orderly fashion. Therefore the SIO is arranged so that all the internal Read, Write, and Data registers are located in specific address locations using the Channel Select input B/A* and Command Data input C/D* as shown below in Table D-3:

TABLE D-3. SIO ADDRESSING

Operation	B/A*	C/D*
Channel A Data	0	0
Channel A Read/Write Reg.	0	1
Channel B Data	1	0
Channel B Read/Write Reg.	1	1

Read/Write Registers

The SIO contains three Read Registers, RR0 - RR2, and eight Write Registers, WR0 - WR7. SIO status details are available through RR0 - RR2. RR0 and RR1 apply to both Channel A and B, while RR2 applies only to Channel B. Note that WR4 must be set up first when initializing the SIO.

SIO Read Registers

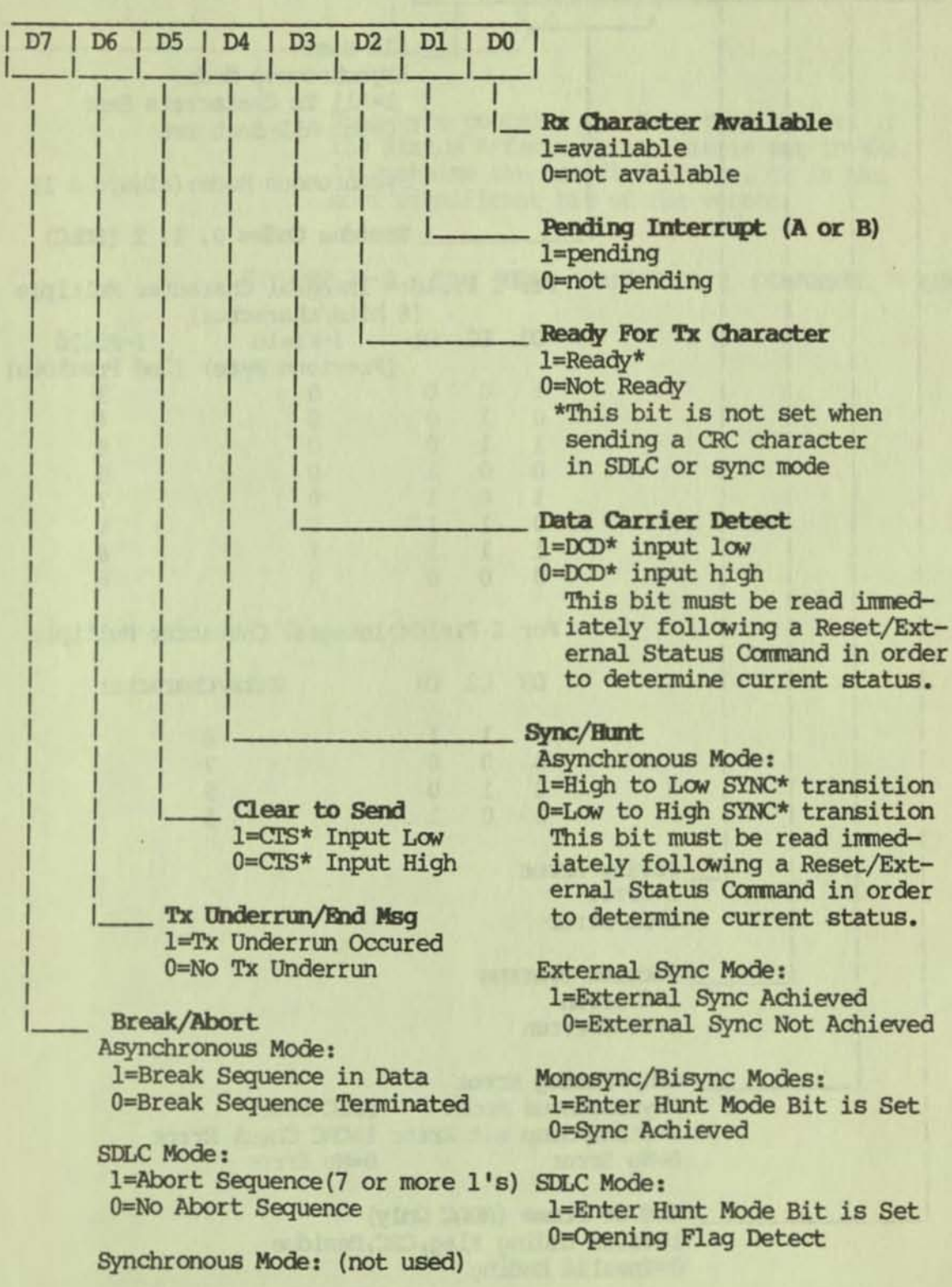


FIGURE D-7. READ REGISTER 0

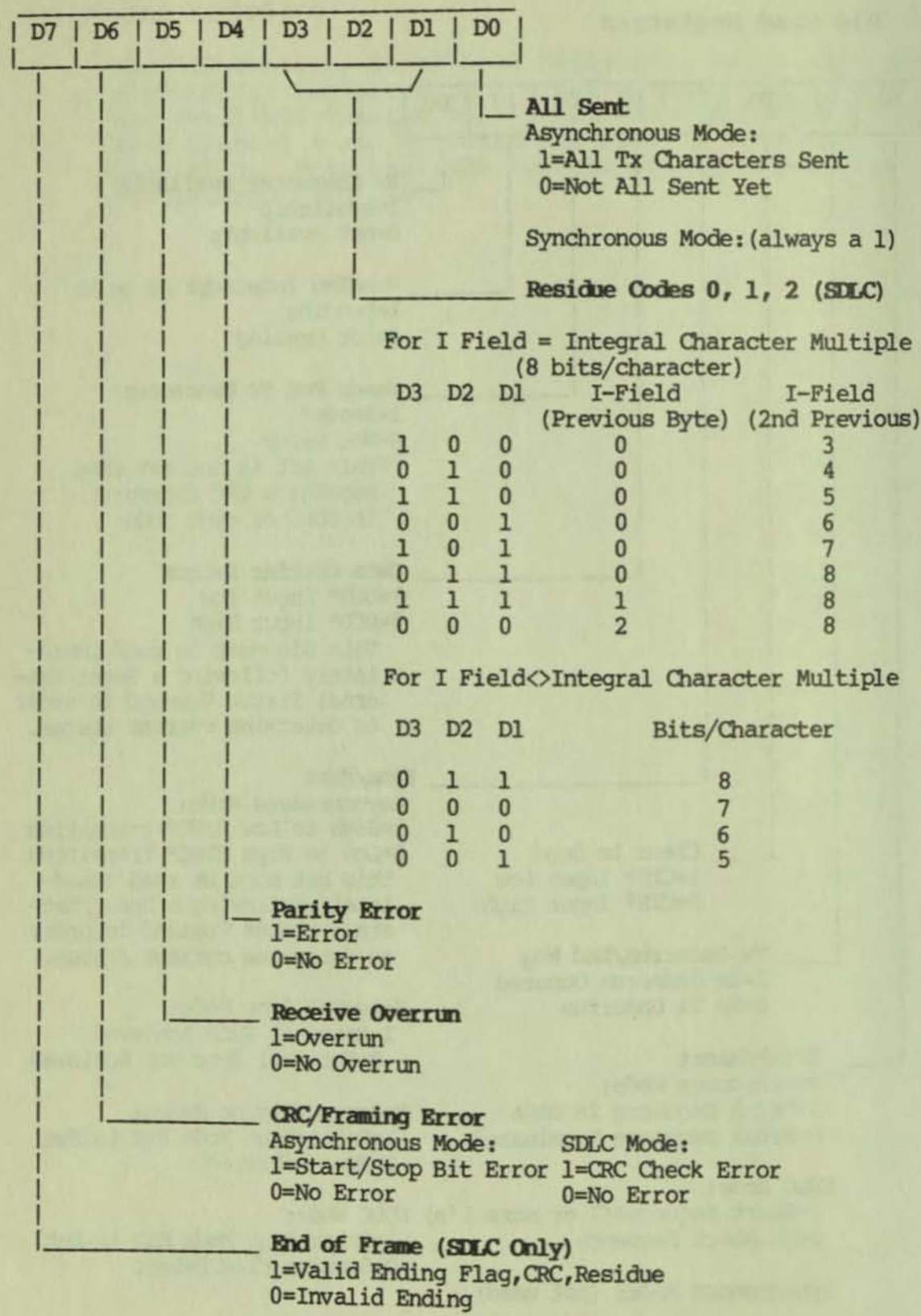


FIGURE D-8. SIO READ REGISTER 1

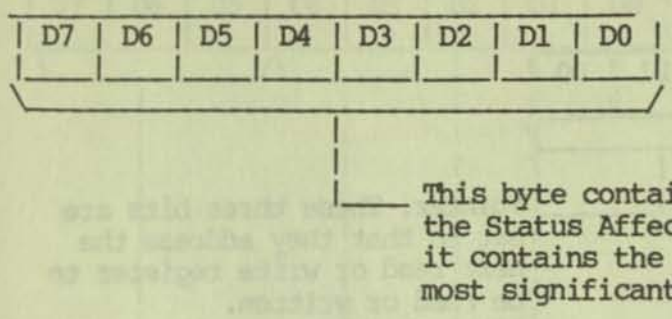
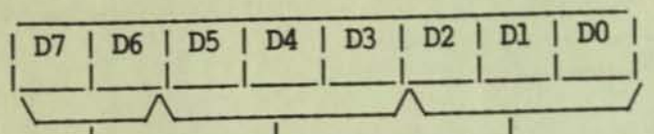


FIGURE D-9. SIO READ REGISTER 2 (CHANNEL B ONLY)

SIO Write Registers



Pointer. These three bits are set so that they address the next read or write register to be read or written. After the read or write is completed, the bits are reset to zero.

Register	D2	D1	D0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

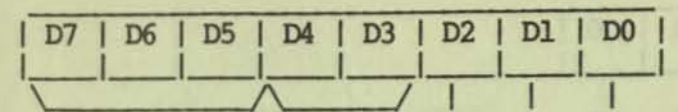
Command Bits.

Command	D5	D4	D3
No Command	0	0	0
Send Abort (SDLC)	0	0	1
Reset Ext/Status Interrupts	0	1	0
Channel Reset	0	1	1
Enable Int. On Next Rx Char	1	0	0
Reset Tx Int. Pending	1	0	1
Error Reset (latches)	1	1	0
Return From Int. (Channel A)	1	1	1

CRC Reset Codes.

Reset Code	D7	D6
No Code	0	0
Reset Rx CRC Character	0	1
Reset Tx CRC Character	1	0
Reset Tx Underrun/End Msg.	1	1

FIGURE D-10. SIO WRITE REGISTER 0



External/Status Int. Enable
1=DCD*,CTS*,SYNC*,Break/ Abort transitions cause interrupt.
0=No interrupt from transitions of above signals

Transmitter Int. Enable
1=Interrupt on Tx buffer empty
0=No interrupt

W*/RDY* Control

01X=RDY* High
00X=W* Floating

Status Affects Vector (Channel B Only)
1=Vector returned from int. acknowledge is according to below table

1X0=RDY* High when Tx Buffer full.
W* Low when Tx buffer full and an SIO data port is selected.
RDY* Low when Tx Buffer empty.
W* Floating when Tx buffer empty

1X1=RDY* High when Rx buffer empty.
W* Low when Rx buffer empty and an SIO data port is selected.
RDY* Low when Rx buffer is full.
W* Floating when Rx buffer is full.

Interrupt Condition	V3	V2	V1
B Tx Buffer Empty	0	0	0
B Ext/Status Change	0	0	1
B Rx Character Available	0	1	0
B Special Rx Condition*	0	1	1
A Tx Buffer Empty	1	0	0
A Ext/Status Change	1	0	1
A Rx Character Available	1	1	0
A Special Rx Condition*	1	1	1

* Parity Error, Rx Overrun Error, Framing Error, End of Frame (SDLC).

0=Fixed Interrupt Vector from WR2 is used.

Receive Interrupt Mode

Mode	D4	D3
Rx Interrupts Disabled	0	0
Rx Interrupt on 1st Character	0	1
Int. on All Rx Characters*	1	0
Int. on All Rx Characters**	1	1

*Parity Error=Special Condition; **Parity Error=Special Condition

FIGURE D-11. SIO WRITE REGISTER 1

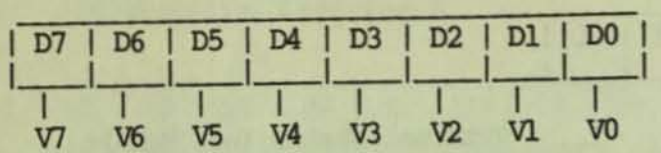


FIGURE D-12. SIO WRITE REGISTER 2

WR2 is the Interrupt Vector byte. This is written in Channel B only. If the Status Affects Vector bit in WR1 is set, V3, V2, and V1 are modified according to the information presented in the WR1 information. If the bit is not set, the Interrupt Vector bits in this byte are returned to the CPU with Interrupt Acknowledge exactly as written in WR2.

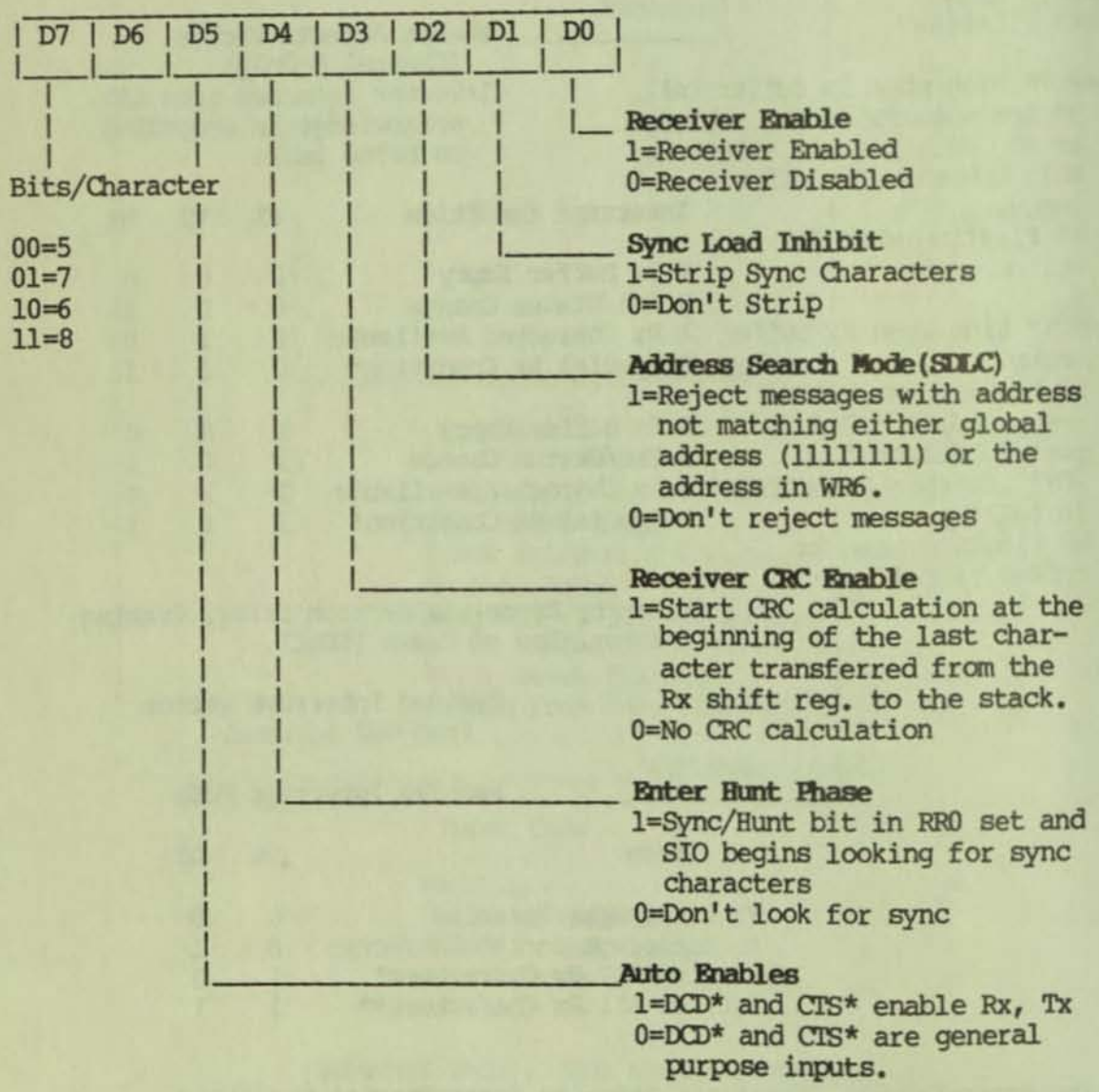
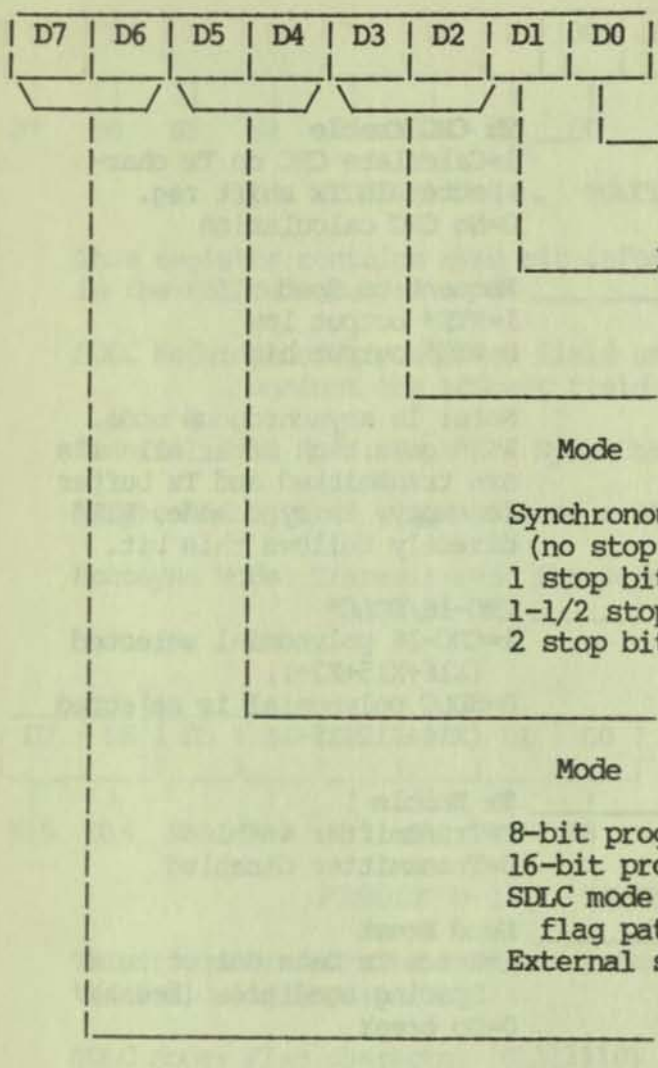


FIGURE D-13. WRITE REGISTER 3

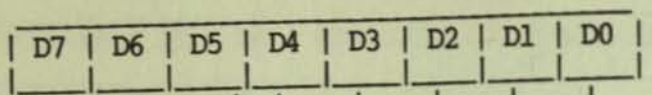


Mode	D3	D2
Synchronous Mode (no stop bits)	0	0
1 stop bit/character	0	1
1-1/2 stop bits/character	1	0
2 stop bits/character	1	1

Mode	D5	D4
8-bit programmed sync	0	0
16-bit programmed sync	0	1
SDLC mode (01111110) flag pattern	1	0
External sync mode	1	1

Mode	D7	D6
Data rate X 1 = Clock Rate	0	0
Data rate X 16= Clock Rate	0	1
Data Rate X 32= Clock Rate	1	0
Data Rate X 64= Clock Rate	1	1

FIGURE D-14. WRITE REGISTER 4



Tx CRC Enable
1=Calculate CRC on Tx character in Tx shift reg.
0=No CRC calculation

Request to Send
1=RTS* output low
0=RTS* output high

Note: In asynchronous mode, RTS* goes high after all bits are transmitted and Tx buffer is empty. In sync mode, RTS* directly follows this bit.

CRC-16/SDLC*
1=CRC-16 polynomial selected (X16+X15+X2+1)
0=SDLC polynomial is selected (X16+X12+X5+1)

Tx Enable
1=Transmitter enabled
0=Transmitter disabled

Send Break
1=Force Tx Data Output to a Spacing condition (break)
0=No break

Transmit Bits/Character

Bits/Character	D6	D5
Five or less	0	0
7	0	1
6	1	0
8	1	1

Data Terminal Ready
1=DTR* output low
0=DTR* output high

Note: If five or less bits are sent the CPU should format them as shown below:

D7	D6	D5	D4	D3	D2	D1	D0	#Bits
1	1	1	1	0	0	0	D	1
1	1	1	0	0	0	D	D	2
1	1	0	0	0	D	D	D	3
1	0	0	0	D	D	D	D	4
0	0	0	D	D	D	D	D	5

FIGURE D-15. WRITE REGISTER 5

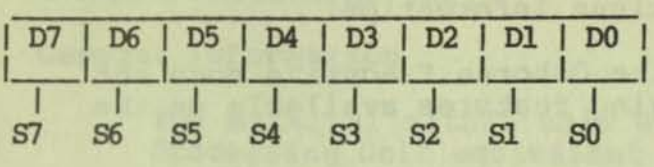


FIGURE D-16. WRITE REGISTER 6

This register contains sync bit information which is used in the following ways:

SDLC Mode: Secondary address field used to compare against the address field of the SDLC frame.

External Sync Mode: Transmit Sync Character

Bisync Mode: First eight bits of a 16-bit sync word

Monosync Mode: Transmit Sync Character

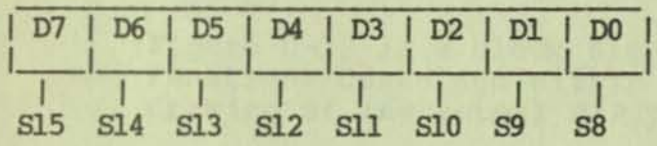


FIGURE D-17. WRITE REGISTER 7

This register contains sync bit information which is used in the following ways:

SDLC Mode: Flag character (01111110)

External Sync Mode: Not used

Bisync Mode: Second eight bits of a 16-bit sync word

Monosync Mode: Receive sync character

Osborne Executive Applications Information

The SIO as used in the Osborne Executive does not implement the following features available on the chip:

External Sync
Wait/Ready
Interrupt Enable Daisy-Chaining Option (IEI is strapped high, always enabling interrupts)

CENTRAL PROCESSING UNIT

General Information

The material within this section covers the Central Processing Unit equivalent to the Z80A manufactured by Zilog. The information also applies to those integrated circuits produced by other manufacturers that may have somewhat different nomenclatures, but very similar physical and electrical characteristics.

Feature List

The following list summarizes the most important and salient features of the Central Processor Unit (CPU).

REFRESH Output for Dynamic RAM Control
Non-Maskable Interrupt Capability
64K-Byte Addressing Range
Memory-Mapped and I/O Operation
8-Bit Data Bus

Block Diagram and Pin Assignments

Figure D-18 is a block diagram representation of the functions contained within the CPU. Figure D-19 is a drawing of the actual DIP pin assignments.

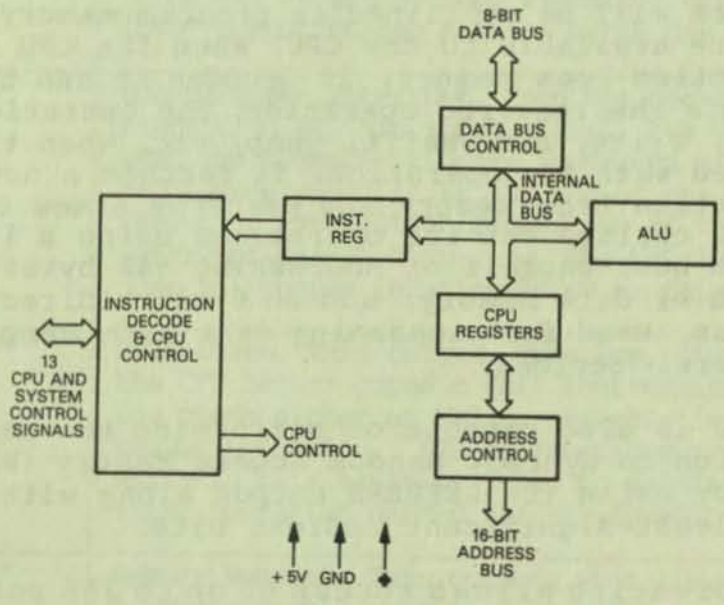


FIGURE D-18. Z80A CPU BLOCK DIAGRAM

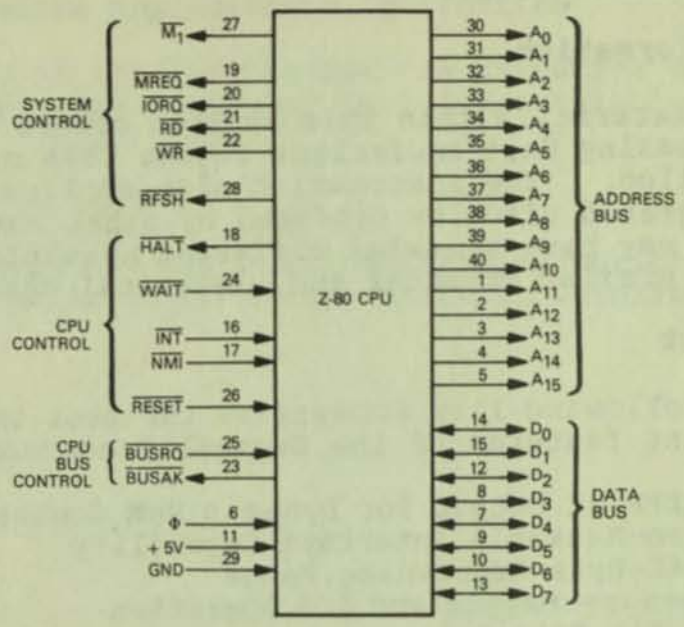


FIGURE D-19. Z80A CPU PIN ASSIGNMENTS

Overall Description

The CPU's function is to obtain instructions from program memory and execute them. Both instructions and data will be contained in program memory where they are available to the CPU. When the CPU reads an instruction from memory, it decodes it and then performs the required operation. The operation may be a read, write, add, shift, jump, etc. When the CPU is finished with the operation, it fetches a new instruction from memory and performs a new operation. The CPU carries out its operations using a 16-bit address bus, capable of addressing 64K bytes of program or data memory, and an 8-bit bidirectional data bus, used for exchanging data with memory and peripheral devices.

The CPU is also capable of performing the refresh operation on dynamic Random Access Memory (RAM) chips by using its REFRESH output along with the seven least-significant address bits.

I/O Addressing allows access of up to 256 ports using the IORQ* control signal.

The CPU consists of the following major functional blocks:

Registers
Arithmetic and Logic Unit (ALU)
Control

Pin Description

Table D-4 summarizes the function of each pin of the CPU.

Table D-4. Z80A CPU PIN FUNCTIONS

PIN	MNEMONIC	FUNCTION
1-5 30-40	A0-A15	**Address Bus.** These signals allow the CPU to address up to 64K bytes of memory. I/O addresses use the lower 8 bits, while memory-mapped addresses use the entire 16 bits. During refresh time, the lower 7 bits contain a refresh address.
6	CLOCK	**Clock.** This is a single-phase TTL clock.
7-15	D0-D7	**Data Bus.** This is the eight-bit bidirectional data bus over which the CPU exchanges data with memory and peripherals.
16	INT*	**Interrupt Request.** This is an input to the CPU and is generated by an external device needing CPU service. If the interrupt-enable flip-flop has been enabled, the request will be honored at the end of the currently executing instruction, if any. When the CPU accepts and responds to the interrupt, it generates an acknowledge signal by driving low the IORQ* output during Machine Cycle One time (M1).
17	NMI*	**Non-Maskable Interrupt.** Upon the negative-going transition of this input signal, the CPU recognizes that the highest-priority interrupt has occurred, and acknowledges it at the end of the currently executing instruction regardless of the state of interrupt-enable flip-flop. The CPU is forced to jump to program location 0066H at this point.
18	HALT*	**Halt State.** This output, when low, signifies that the CPU has executed a Halt instruction. The CPU now needs either an NMI or maskable interrupt to resume operation. NOP instructions are executed while in this state in order to maintain the refresh operation needed for the dynamic RAM memory.
19	MREQ*	**Memory Request.** This output, when low, means that a memory-mapped operation is taking place and that the address bus is valid for either a write or read operation.

TABLE D-4. Z80A CPU PIN FUNCTIONS (Cont.)

20	IORQ*	**I/O Request.** This output is low when the CPU is doing an I/O mapped operation, such as a read or write. The lower eight bits of the address bus are used for the address in this case. When an interrupt is being acknowledged, IORQ* is taken low during M1 time.
21	RD*	**Read.** This output goes low when the CPU is requesting that a read cycle be executed from memory or from an I/O device. The memory or I/O device may drive the data bus once this signal goes active.
22	WR*	**Write.** This output signals the external memory or I/O device that the CPU is driving the data bus with valid data.
23	BUSAK*	**Bus Acknowledge.** This output allows other bus master devices to gain control of the CPU data, address, and control lines. When the signal is low, the CPU has relinquished control.
24	WAIT*	**Wait.** This input signals the CPU that the external memory or I/O is not yet ready for the read or write transfer. The CPU will enter wait states, thus prolonging the execution of the cycle until WAIT* line goes back to a high state.
25	BUSRQ*	**Bus Request.** This input requests the CPU to turn over control of its data, address, and control signals to an external device that shares these lines. Upon completion of the currently executing instruction, the lines enter high impedance state.
26	RESET*	**Reset.** This input, when low, resets the CPU and forces the program counter to zero.
27	M1*	**Machine Cycle One.** This output, when low, means the CPU is doing an Opcode fetch. M1* also occurs in conjunction with IORQ* to signal an Interrupt Acknowledge cycle.
28	RFSH*	**Refresh.** When this output is low, the lower 7 address lines contain the refresh address to be used to refresh dynamic RAM, if used.

Hardware Functional Description

Registers

Program Counter

The program counter is a 16-bit register that contains the address of the currently executing instruction. This counter increments each time an instruction's address is placed on the CPU's address lines. It is set by a jump instruction to the value of the address being jumped to.

Stack Pointer

This is a 16-bit register that contains the address of the last data byte placed on the stack. Data is placed onto the stack with a PUSH instruction and taken off the stack with a POP instruction. The data which is removed from the stack is the last byte that was pushed onto the stack.

Refresh Register

This 8-bit register contains the 7-bit address counter used when refreshing dynamic RAM from the CPU. During memory refresh cycles, the CPU RFSH* pin goes low and the refresh address appears on the lower seven bits of the address bus.

Interrupt-Page Address Register

This register is used to store the upper 8 bits of an interrupt vector so that the CPU may use the lower 8 bits provided by an external interrupting device. This allows interrupt routines to be located anywhere in memory space.

Index Registers

The CPU has two independent 16-bit registers for use in indexed addressing modes.

Accumulator and Flag Registers

There are two accumulator and two flag registers, all of which are eight bits. The accumulators hold the results of arithmetic and logical operations, while the flag registers contain bits that get set for certain conditions, such as not equal to zero, etc.

General Purpose Registers

There are twelve 8-bit registers that may be used alone or in 16-bit pairs for general reading and writing.

Instruction Register

The instruction register is where the instruction read from memory is placed when the CPU does an Opcode fetch operation.

ALU

The ALU performs logiocal and arithmetic operations, such as:

Test Bit	OR
Increment	Reset Bit
AND	Subtract
Rotate	Exclusive-OR
Set Bit	Compare
Decrement	Add
Shift	

Control

Once the CPU has fetched an instruction, it then decodes it and activates the proper set of control signals (such as RD*, WR*, IORQ*, MREQ*, etc.) according to the requirements of the specific instruction.

Maximum Ratings

Listed below are the maximum ratings of the CPU. If these ratings are exceeded, permanent damage may result. Also, exposure to the maximum ratings for extended periods may affect the reliability of the device.

Storage Temperature	-65 to +150 Degrees C
Voltage on Any Pin	-0.3 to +7 Volts
Power Dissipation	1.5 Watts

Electrical Characteristics

The following table describes the DC electrical characteristics of the CPU. These characteristics apply, unless otherwise noted, at an ambient temperature of 0 to 70 degrees Centrigrade and Vcc = 5 V$\pm$5%.

TABLE D-5. CPU ELECTRICAL CHARACTERISTICS

Parameter	Min.	Max.	Units	Notes
Clock Input Low (Vilc)	-0.3	0.8	V	
Clock Input High (Vihc)	Vcc -0.6	Vcc 0.3	V	
Input Low (Vil)	-0.3	0.8	V	
Input High (Vih)	2.0	Vcc	V	
Output Low (Vol)		0.4	V	Iol=1.8 ma
Output High (Voh)	2.4		V	Ioh=-250 ua
Power Supply Current (Icc)		150	ua	
Input Leakage Current (Ili)		10	ua	Vin=0 to Vcc
Tri-State Output Leakage (Iloh)		10	ua	Vout=2.4 to Vcc
Tri-State Output Leakage (Ilol)		-10	ua	Vout=0.4 V
Data Bus Leakage Current (Ild)		±10	ua	0<=Vin<=Vcc

CPU Timing

The following paragraphs are intended to convey information about the timing relationships that exist when the CPU is executing its basic operations, such as:

Memory Write and Read Cycles
I/O Write and Read Cycles
Interrupt Acknowledge Cycles
Bus Request/Grant Cycles
Opcode Fetch Cycles

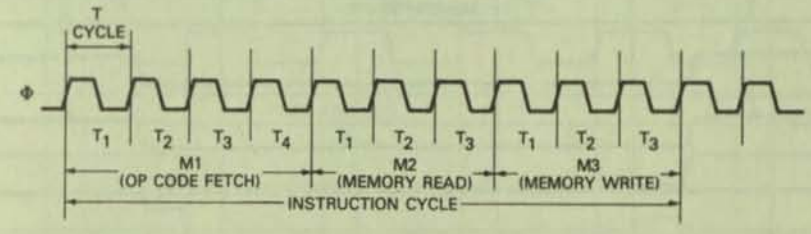


FIGURE D-20. BASIC CPU TIMING EXAMPLE

Memory Write and Read Timing

The following figures, D-21 and D-22, illustrate the CPU memory read and write cycles, both with and without wait states.

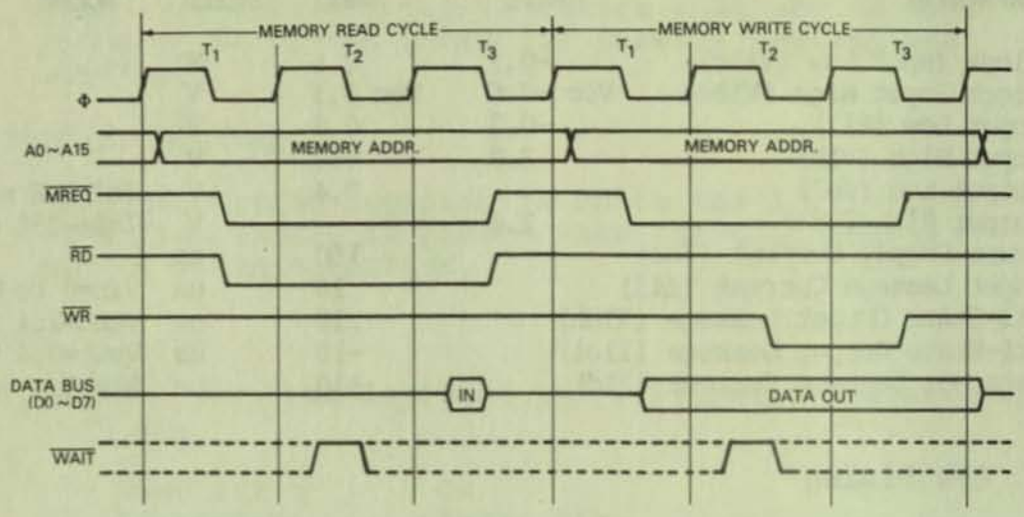


FIGURE D-21. Z80A MEMORY WRITE AND READ TIMING (No Wait States)

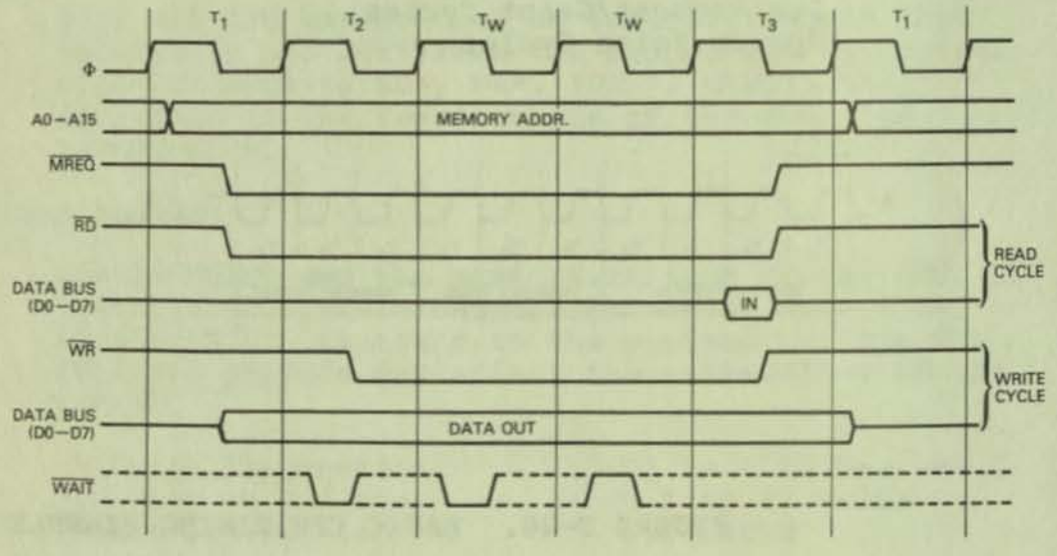


FIGURE D-22. Z80A MEMORY WRITE AND READING TIMING (with Wait States)

I/O Write and Read Timing

Figures D-23 and D-24 below illustrate I/O Write and Read cycles, both without and with wait states.

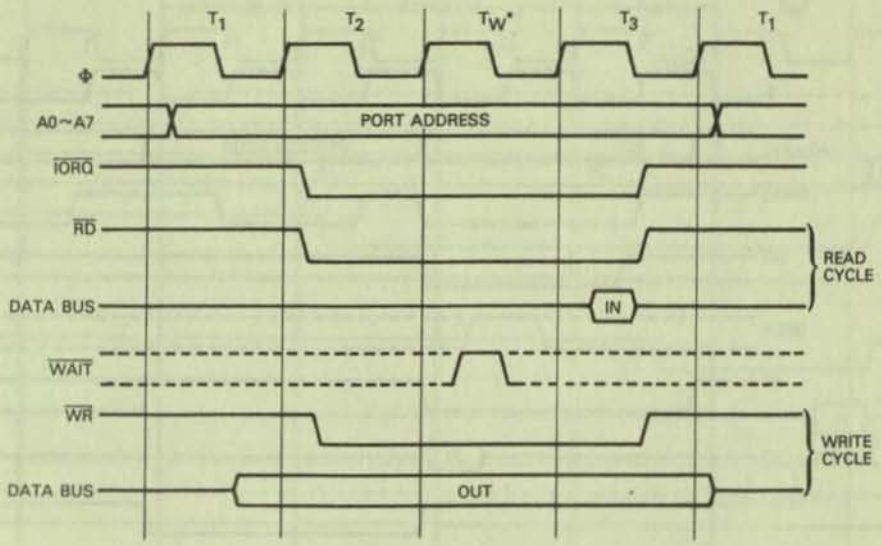


FIGURE D-23. Z80A WRITE AND READ TIMING (No Wait States)

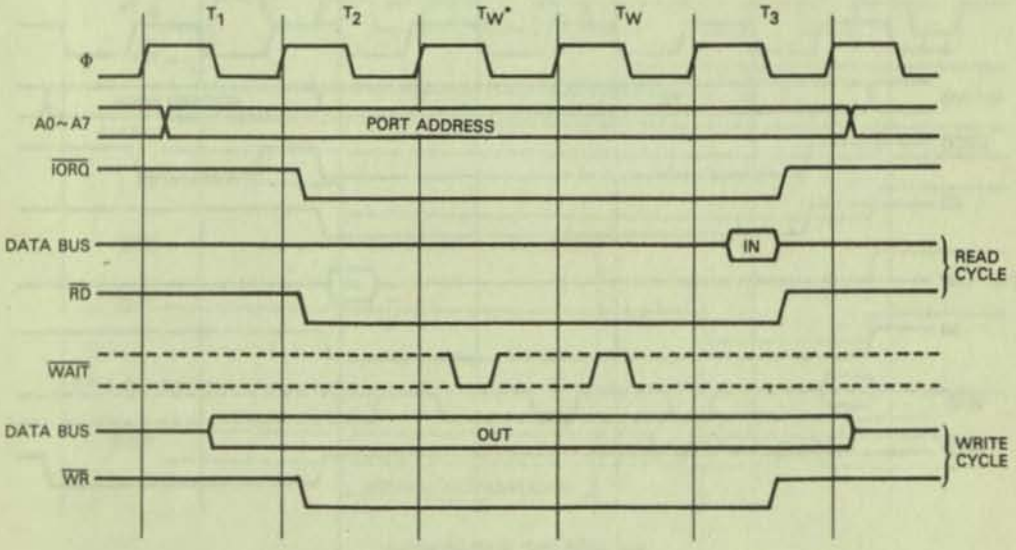


FIGURE D-24. Z80A WRITE AND READ TIMING (with Wait States)

Opcode Fetch Timing

Figures D-25 and D-26 below illustrate the CPU Opcode fetch timimg, both without and with wait states.

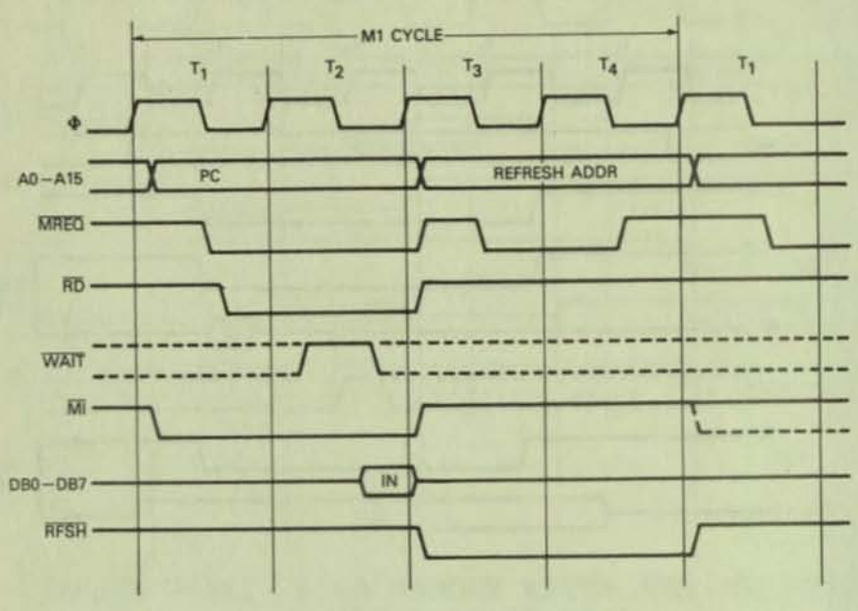


FIGURE D-25. Z80A OPCODE FETCH TIMING (No Wait States)

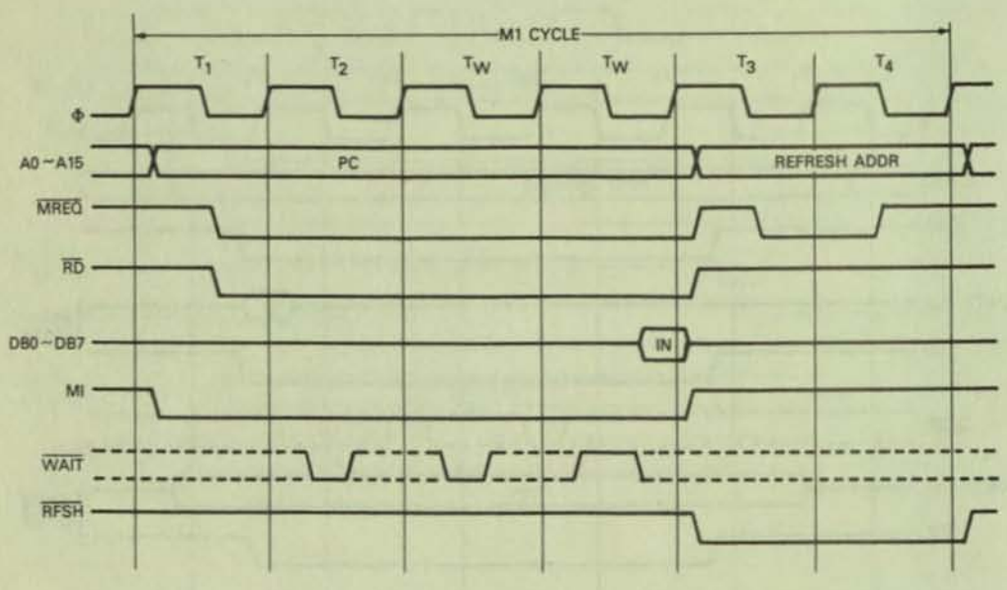


FIGURE D-26. Z80A OPCODE FETCH TIMING (with Wait States)

Interrupt Acknowledge Timing

Figures D-27 and D-28 below illustrate the CPU Interrupt Acknowledge Cycle timing relationships.

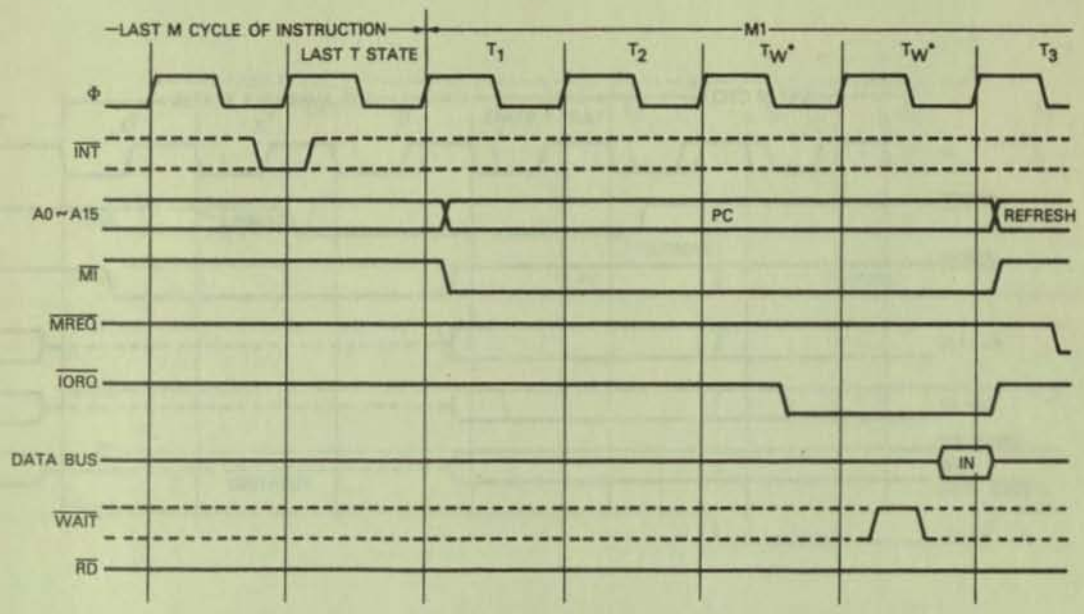


FIGURE D-27. Z80A INTERRUPT ACKNOWLEDGE TIMING (No Wait States)

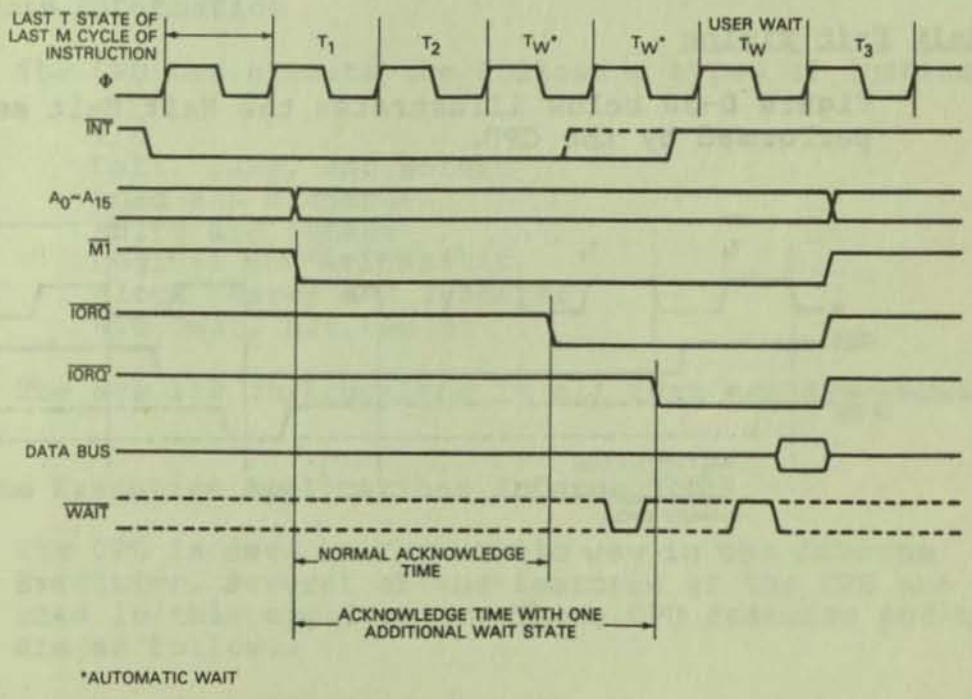


FIGURE D-28. Z80A INTERRUPT ACKNOWLEDGE CYCLE (with Wait States)

Bus Request/Acknowledge Timing

Figure D-29 below illustrates the Bus Request/Acknowledge timing relationships for the CPU.

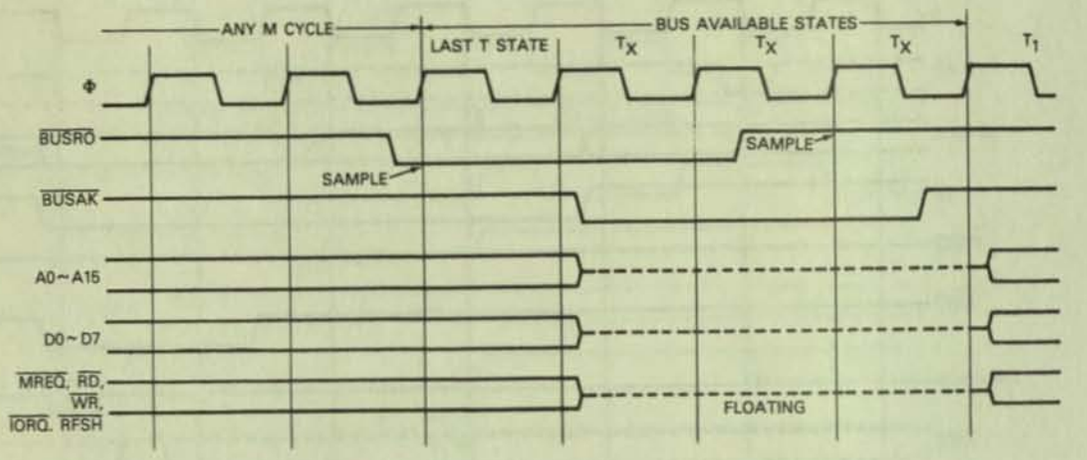


FIGURE D-29. Z80A BUS REQUEST/ACKNOWLEDGE TIMING

Halt Exit Timing

Figure D-30 below illustrates the Halt Exit sequence performed by the CPU.

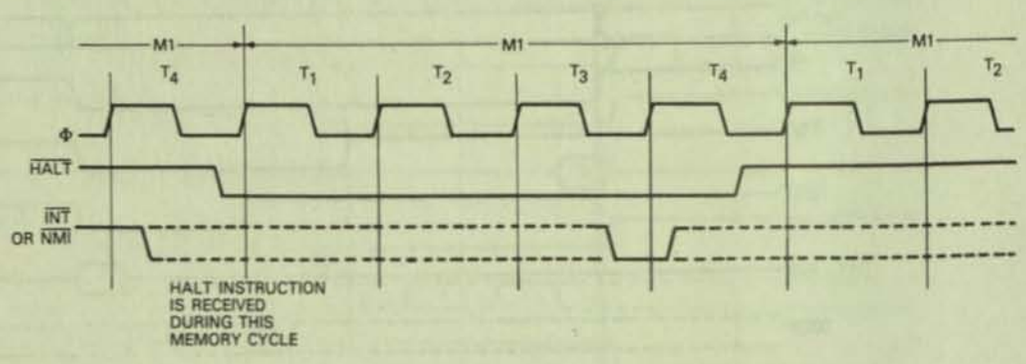


FIGURE D-30. Z80A HALT EXIT TIMING

Non-Maskable Interrupt Timing

Figure D-31 below illustrates the CPU Non Maskable Interrupt timing relationships.

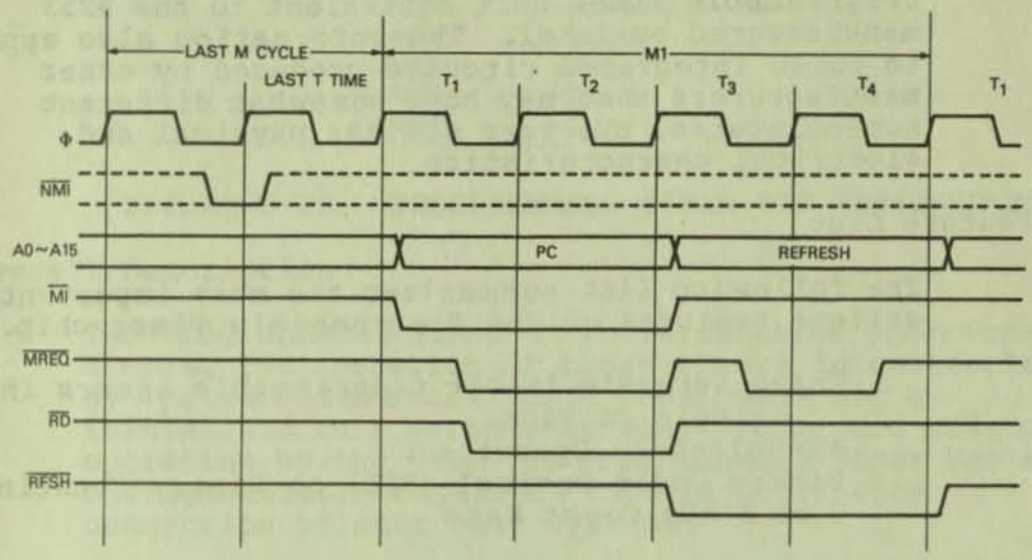


FIGURE D-31. Z80A NON-MASKABLE INTERRUPT TIMING

Software Information

The CPU can execute the following types of instructions:

I/O
Call, Jump, and Return
Load and Exchange
Shift and Rotate
Logical and Arithmetic
Block Search and Transfer
Bit Test, Set, Reset

The are 158 instructions in all that may be executed.

Osborne Executive Applications Information

The CPU is used in a specific way in the Osborne Executive. Several of the features of the CPU are not used in this application. Those CPU features not used are as follows:

Non Maskable Interrupt
Bus Request/Acknowledge
Halt

PROGRAMMABLE TIMER

General Information

The material within this section covers the Programmable Timer unit equivalent to the 8253 manufactured by Intel. The information also applies to those integrated circuits produced by other manufacturers that may have somewhat different nomenclatures, but very similar physical and electrical characteristics.

Feature List

The following list summarizes the most important and salient features of the Programmable Timer chip.

- Three separate 16-Bit programmable timers in a single package.
- +5-Volt-Only Operation.
- Binary Coded Decimal (BCD) or Binary Counting.
- 0 to 2 MHz Count Rate

Block Diagram and Pin Assignments

Figure D-32 below is a block diagram representation of the functions contained within the Programmable Timer. Figure D-33 is a drawing of the actual DIP pin assignments.

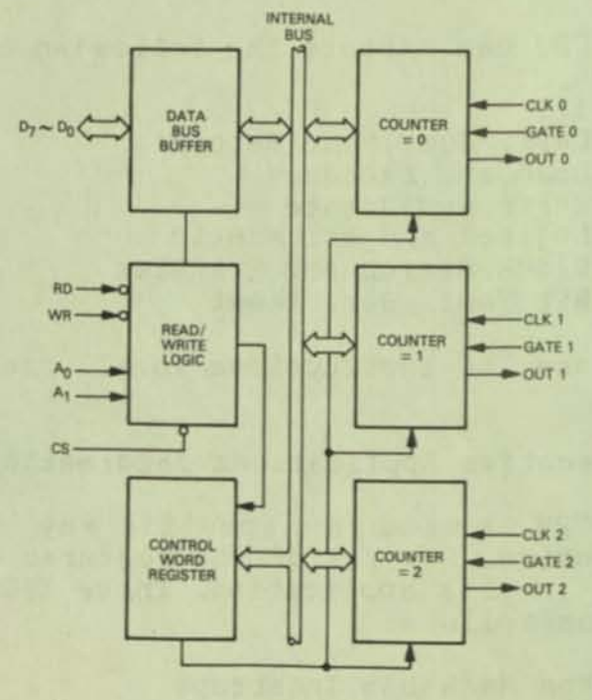


FIGURE D-32. PROGRAMMABLE TIMER BLOCK DIAGRAM

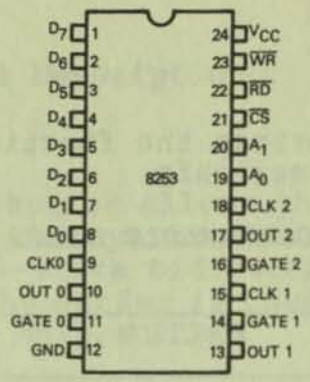


FIGURE D-33. PROGRAMMABLE TIMER PIN ASSIGNMENTS

Overall Description

The Programmable Timer IC contains three programmable timers. The operation of these timers is controlled by system software. Each of the timers may be initialized to a particular count value and mode of operation by the CPU. The Programmable Timer has a microprocessor-compatible interface for easy connection to most host systems.

The Programmable Timer consists of the six following functional blocks:

Data Bus Buffer
Read/Write Logic
Control Word Register
Counter 0
Counter 1
Counter 2

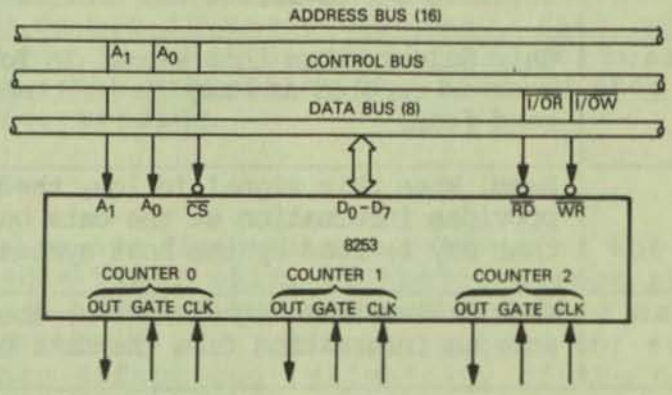


FIGURE D-34. 8253 SYSTEM INTERFACE

Pin Description

Table D-6 summarizes the function of each pin of the Programmable Timer chip.

Table D-6. PROGRAMMABLE TIMER PIN FUNCTIONS

PIN	MNEMONIC	FUNCTION
1 - 8	D7 - D0	**Data Bus.** These eight lines provide a bi-directional data interface to the host microprocessor. The microprocessor uses the data bus to write into the timer's registers and read status and timing count information from the timer.
9,15, 18	CK0,1,2	**Clock 0,1,2.** These are the timing inputs that are used to run timers 0, 1, and 2, respectively.
10,13 17	OUT0,1,2	**Output 0,1,2.** These are the final outputs of timers 0, 1, and 2, respectively.
11,14 16	GATE0,1,2	**Gate 0,1,2.** These signals control the operation of timers 0, 1, and 2. They are used to start, stop, and resynchronize the counting of the timers.
19,20	A0, A1	**Address 0,1.** These two signals are used to select which of the three timers is to be accessed and to select the control register.
21	CS*	**Chip Select.** When this signal is low, the timer is enabled and may be written into or read from.
22	RD*	**Read.** When this signal is low, the timer provides information at the data bus D0-D7 that may be read by the host system.
23	WR*	**Write.** When this signal is low, the timer accepts information from the data bus D0-D7.

Note: An asterisk (*) denotes that the referenced signal is active low.

Hardware Functional Description

Data Bus Buffer

The Data Bus Buffer allows the Programmable Timer to interface to the system data bus. This consists of an eight-bit tri-state bidirectional buffer arrangement. Basically, the buffer is used to read from and write to the timer chip.

Read/Write Logic

The Read/Write logic is responsible for the overall control of the timer. This section of the timer chip receives read, write, address, and chip select signals from the system bus and causes the proper registers within the timer to be loaded or read.

Control Word Register

The Control Register is write-only and is accessed when both address inputs (A0 and A1) are high. The data stored in this register is used to control the operational characteristics of each of the three counters.

Counters 0, 1, and 2

As mentioned previously, the Programmable Timer contains three identical counter circuits. Each counter is controlled by the information loaded into the control register by the system CPU. Each counter counts **down** in either binary or BCD fashion, depending on how it was programmed. Each counter is 16 bits long, and may be read by the software while operating, thus preventing the need to stop the counter for reading.

Maximum Ratings

Listed below are the maximum ratings of the Programmable Timer chip. If these ratings are exceeded, permanent damage to the device may result. Also, exposure to the maximum ratings for extended periods may affect the reliability of the device.

Operating Temperature	0 to 70 Degrees C
Storage Temperature	-65 to 150 Degrees C
Positive Voltage on Any Pin	-0.5V to 7V
Power Dissipation	1 Watt

Electrical Characteristics

Listed below are the D.C. and A.C. electrical characteristics of the Programmable Timer. These characteristics apply, unless otherwise noted, at an ambient temperature of 70 Degrees Centigrade and at a power supply voltage of +5 V ±10%.

Refer to figures D-35, D-36, and D-37 for more information regarding the timing parameters mentioned below.

TABLE D-7. PROGRAMMABLE TIMER D.C. AND A.C. ELECTRICAL CHARACTERISTICS

Parameter	Min.	Max.	Unit	Comment
Input Voltage				
Low Level	-0.5	0.8	V	
High Level	2.2	Vcc+.5	V	
Output Voltage				
Low Level		0.45	V	Iol=2.2 ma
High Level	2.4		V	Ioh=400 ua
Input Current				
Load Current		±10	ua	Vin=Vcc to 0V
Leakage				
Output Float		±10	ua	Vout=Vcc to 0V
Current				
Vcc Supply		140	ma	
Capacitance				
Input		10	pf	
I/O		20	pf	
Add. Stable Before Read (Tar)	50		ns	
Add. Hold Time for Read (Tra)	5		ns	
Read Pulse Width (Trr)	400		ns	
Data Delay From Read (Trd)		300	ns	
Read to Data Floating (Tdt)	25	125	ns	
Recovery Time Between Read and Any Other Control (Trv)	1000		ns	

TABLE D-7 (cont.)

Parameter		Min.	Max.	Unit
Add. Stable Before Write	(Taw)	50		ns
Add. Hold Time for Write	(Twa)	30		ns
Write Pulse Width	(Tww)	400		ns
Setup Time for Write	(Tdw)	300		ns
Hold Time for Write	(Twd)	40		ns
Recovery Time Between Write and Any Other Control	(Trv)	1000		ns
Clock Period	(Tclk)	380	dc	ns
High Pulse Width	(Tpwh)	230		ns
Low Pulse Width	(Tpwl)	150		ns
Gate Width High	(Tgw)	150		ns
Gate Width Low	(Tgl)	100		ns
Gate Setup to Clk High	(Tgs)	100		ns
Gate Hold After Clk	(Tgh)	50		ns
Output Dly From Clk Low	(Tod)		400	ns
Output Dly From Gate Low	(Todg)		300	ns

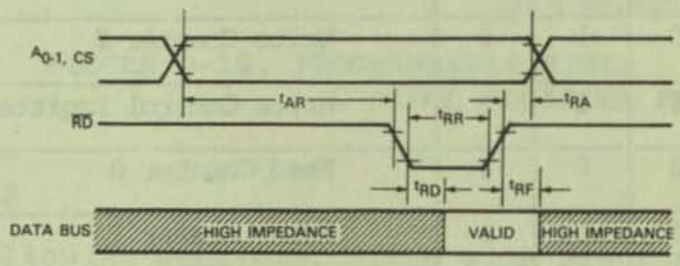


FIGURE D-35. PROGRAMMABLE TIMER READ TIMING

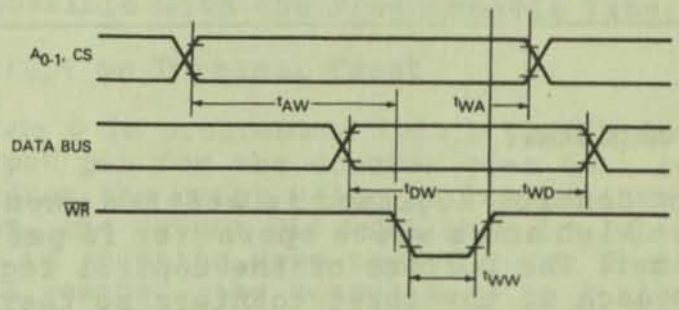


FIGURE D-36. PROGRAMMABLE TIMER WRITE TIMING

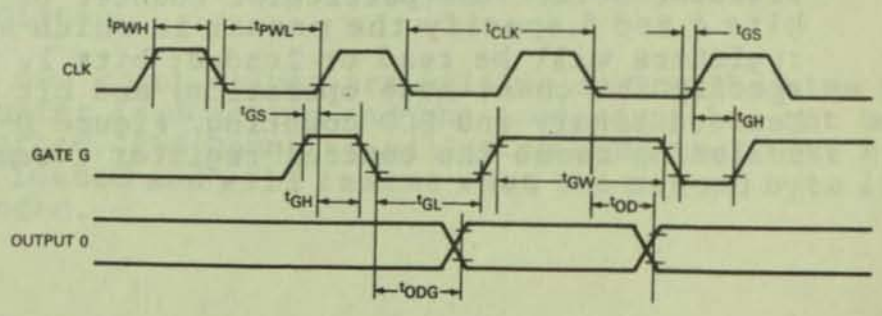


FIGURE D-37. PROGRAMMABLE TIMER GATE AND CLOCK TIMING

Software Addressing

Since the Programmable Timer is controlled with two address inputs, A0 and A1, it is apparent that there are four distinct address locations within the device that can be accessed. Three of these locations allow writing or reading values into or from the count registers for each of the three counters. The fourth location is write-only and allows setting up the control register. The addressing map is shown in Table D-8.

Table D-8. PROGRAMMABLE TIMER ADDRESS MAP

A1	A0	CS*	RD*	WR*	Operation
X	X	1	X	X	Timer Not Selected
0	0	0	1	0	Write Counter 0
0	1	0	1	0	Write Counter 1
1	0	0	1	0	Write Counter 2
1	1	0	1	0	Write Control Register
0	0	0	0	1	Read Counter 0
0	1	0	0	1	Read Counter 1
1	0	0	0	1	Read Counter 2

Control Register

The Control Register is written when both A0 and A1 are high and a write operation is performed to the timer. The purpose of the control register is to set up each of the three counters so they are in the desired counting mode. Bits 6 and 7 of the control register select the particular counter of interest, bits 4 and 5 specify the manner in which the count registers will be read or loaded; bits 1, 2, and 3 specify the count mode operation; and bit 0 selects between binary and BCD counting. Figure D-38 following shows the control register format.

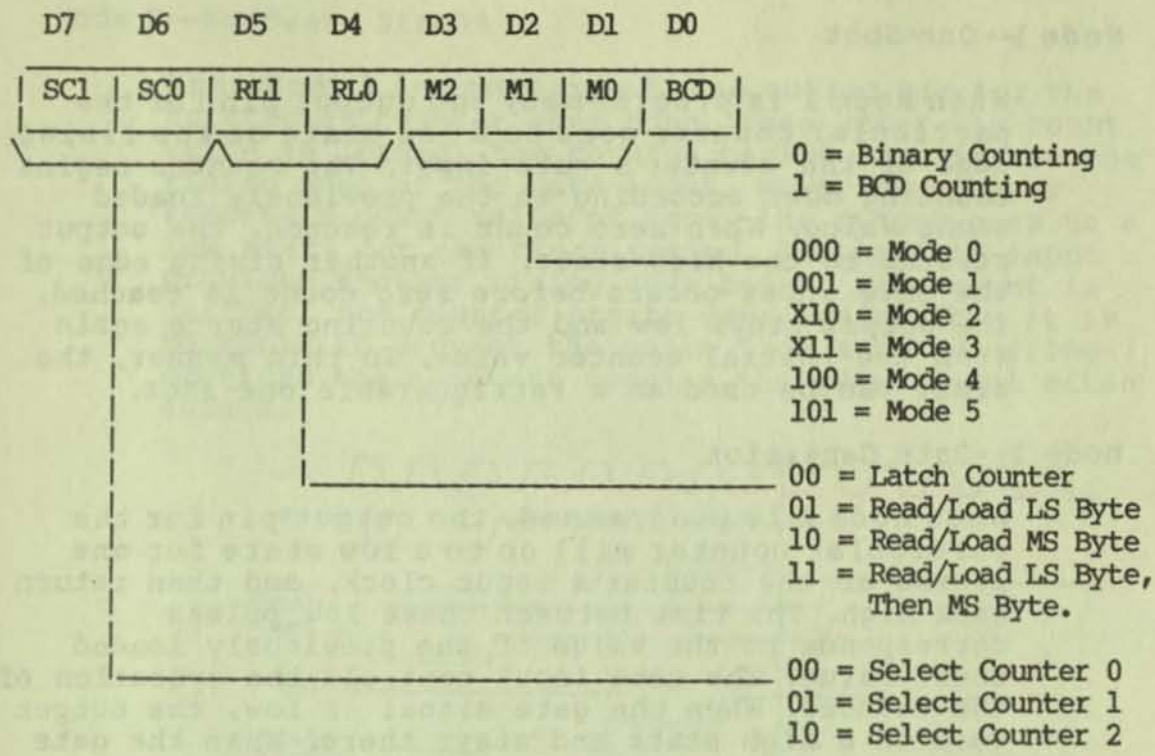


FIGURE D-38. PROGRAMMABLE TIMER CONTROL REGISTER FORMAT

Counter Modes

The following sections, along with Figures D-39 though D-44 provide information about the counter modes possible with the Programmable Timer.

Mode 0--Interrupt on Terminal Count

When Mode 0 is programmed into a particular counter, the output pin for the counter goes to a low state. Then, after the count value is loaded into the count register, the output pin will stay low while the counter is counting down toward zero. When the zero count is reached, the output goes to a high state and stays there until a new count value is loaded, or until a new mode is written into the control register.

If new count values are written during the time the counter is counting and the zero count has not been reached, the counting will stop when the first byte is loaded and will resume when the second byte is laoded.

Mode 1--One-Shot

When Mode 1 is programmed, the output pin for the particular counter goes to a low state on the rising edge of the counter's gate input. The counter begins counting down according to the previously loaded count value. When zero count is reached, the output returns to the high state. If another rising edge of the gate input occurs before zero count is reached, the output stays low and the counting starts again from the initial counter value. In this manner, the timer can be used as a retriggerable one-shot.

Mode 2--Rate Generator

When Mode 2 is programmed, the output pin for the particular counter will go to a low state for one period of the counter's input clock, and then return back high. The time between these low pulses corresponds to the value of the previously loaded count value. The gate input controls the operation of the counter. When the gate signal is low, the output goes to a high state and stays there. When the gate input goes high, the counter is allowed to run.

If the counter is reloaded between pulses, the current period is not affected, but the following period will conform to the new value.

Mode 3--Square Wave Generator

When Mode 3 is programmed, the operation is similar to that of Mode 2, except that the output will remain high for half of the count value, and go low for the other half.

Mode 4--Software Strobe

When Mode 4 is programmed, the output pin for the particular counter goes high until after the count value is loaded, at which time the counter begins counting. The counter is inhibited, however, if the gate input is low. When the counter reaches zero count, the output pin goes low for one clock period and then returns high. If the counter is reloaded between low pulses, the counter starts counting from the new value (even if the same value is continuously reloaded). Thus it is possible to prevent the pulse from ever occurring provided the software services the counter regularly.

Mode 5--Hardware Strobe

When Mode 5 is programmed, the output pin for the particular counter goes high. Then after the count value is loaded, the counter begins counting on the rising edge of the gate input. When the counter reaches a count value of zero, the output goes to a low state for one clock period. If the gate input provides another rising edge before zero count is reached, the counter starts over again. Thus it is possible to prevent the pulse from ever occurring provided the hardware toggles the gate signal often enough.

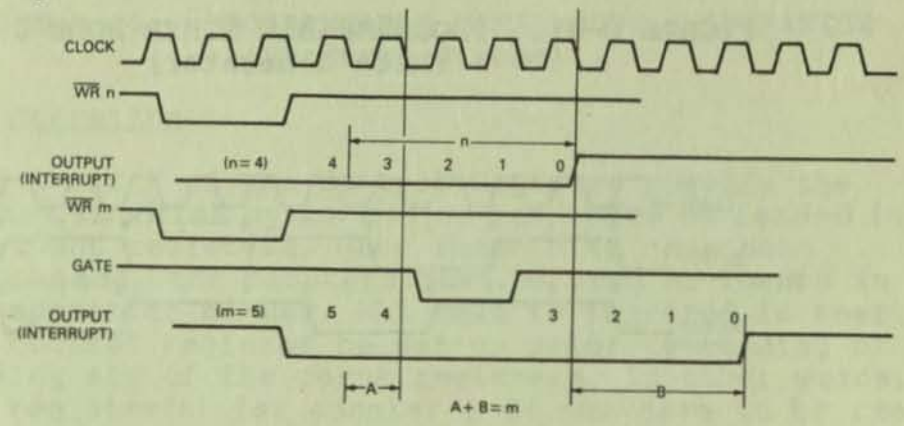


FIGURE D-39. PROGRAMMABLE TIMER MODE 0 OPERATION (Interrupt on Terminal Count)

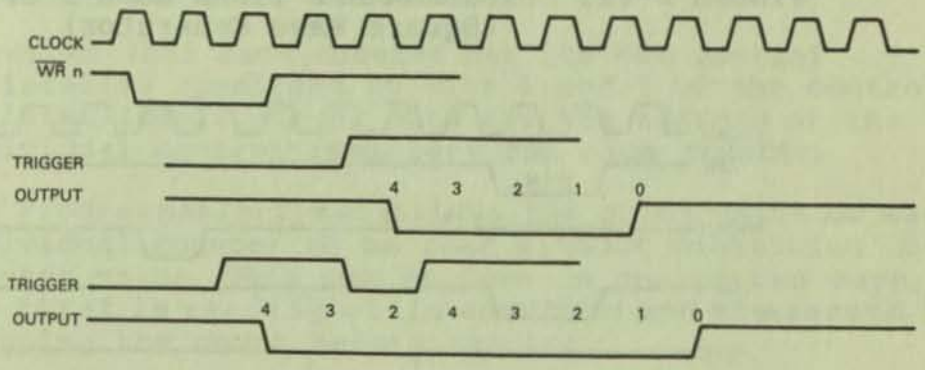


FIGURE D-40. PROGRAMMABLE TIMER MODE 1 OPERATION (One Shot)

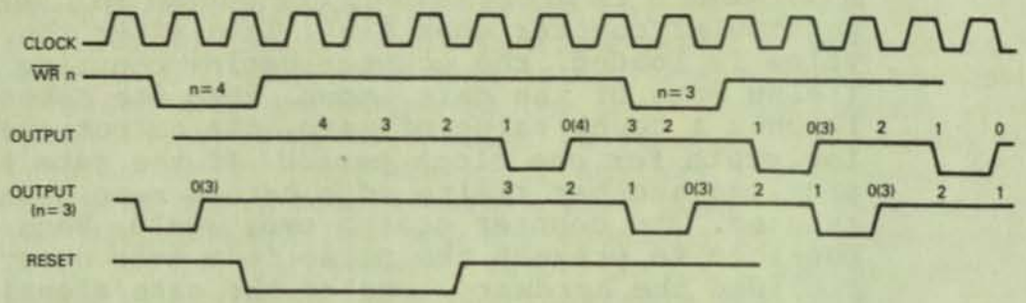


FIGURE D-41. PROGRAMMABLE TIMER MODE 2 OPERATION (Rate Generator)

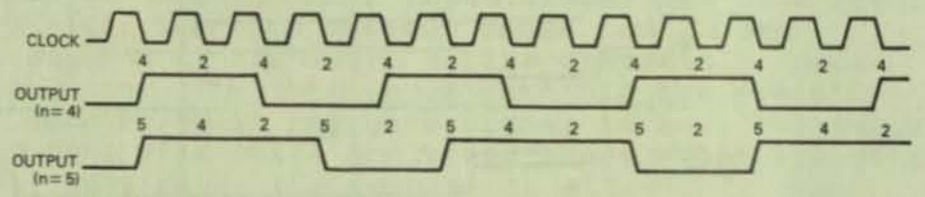


FIGURE D-42. PROGRAMMABLE TIMER MODE 3 OPERATION (Square Wave Generator)

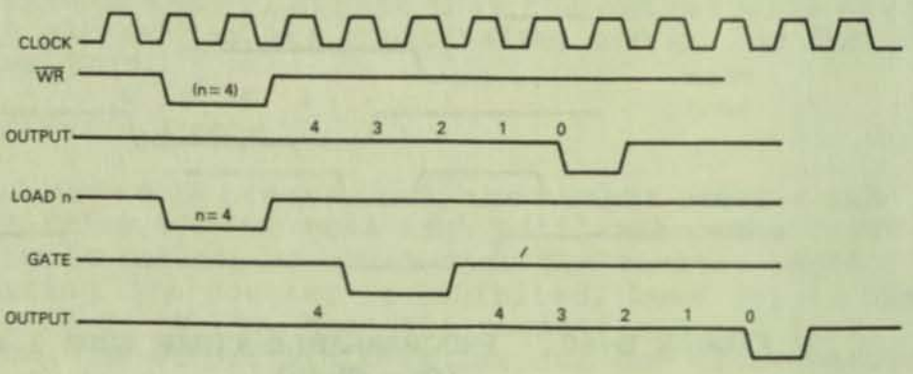


FIGURE D-43. PROGRAMMABLE TIMER MODE 4 OPERATION (Software Strobe)

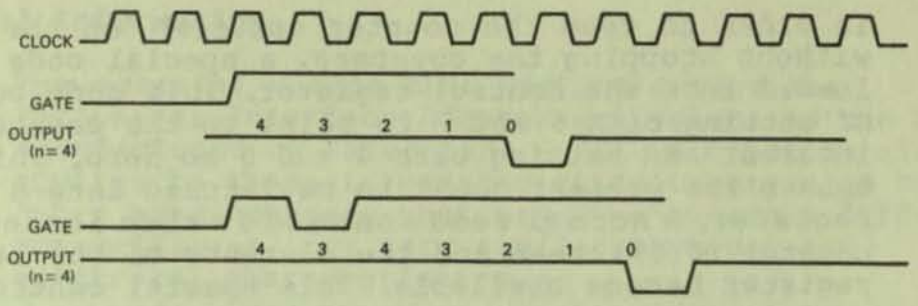


FIGURE D-44. PROGRAMMABLE TIMER MODE 5 OPERATION (Hardware Strobe)

Read/Load Operation

Bits 4 and 5 of the Control Register specify the manner in which bytes may be read from or loaded into the count registers. Once these bits have been programmed, the counters must be read or loaded in the specified manner. All that is required is that the control register be set up prior to reading or loading any of the count registers. In other words, the register(s) for counter 1 do not have to be read or loaded prior to those of register 2. The count registers may be loaded or read in any order once the proper control register values have been set up for each.

Remember that each counter has its own control register as specified by bits 6 and 7 of the control register itself. These bits are the address of the individual control registers for each counter.

The Programmable Timer allows the count value of each individual counter to be read without disturbing the counter value. This may be done in one of two ways. The first is reading while counting and the second is stopping the count before reading.

Reading While Counting

In order to read the counter value(s) "on the fly" without stopping the counters, a special code is loaded into the control register. This code consists of setting bits 6 and 7 to point to the counter of interest and setting bits 4 and 5 to zero. This causes the present count to be latched into a storage register. A normal read command is then issued to the counter of interest and the contents of the latched register become available. This special control register operation has no effect on the control register values previously set up for the counter, and the sequence and number of bytes must be read exactly as previously programmed.

Stopping Before Reading

If the above method of latching before reading is not used, the counter of interest must be stopped by either controlling the gate input or by stopping the clock input. Only in this manner can a stable count be guaranteed to be read. Again, the reading of the counter bytes must be performed in the manner previously specified in the control register bits.

Osborne Executive Applications Information

The Programmable Timer is used in the Osborne Executive portable computer for the following functions:

Timer 0 = Serial Communications Clock A
Timer 1 = Serial Communications Clock B
Timer 2 = Floppy Disk Drive Spindle Clock

The clock inputs for Timers 0 and 1 are generated by a divider circuit that divides a 24 MHz signal by 13. This yields a clock of 1.846 MHz, a common communications clock frequency which the Programmable Timer can divide further to yield the common baud rate values for serial communications.

The clock input for Timer 2 is 2 MHz. The Programmable Timer is equipped to supply the proper spindle clock for the floppy disk drive, although this feature is not currently utilized.

All the gate inputs are pulled up to +5 Volts and are thus not controllable by the Executive logic circuits.

PERIPHERAL INTERFACE ADAPTER

General Information

The material within this section covers the Peripheral Interface Adapter equivalent to the F6821 manufactured by Fairchild. The information also applies to those integrated circuits produced by other manufacturers that may have somewhat different nomenclatures, but very similar physical and electrical characteristics.

Feature List

The following list summarizes the most important and salient features of the PIA chip.

- Two Separate 8-Bit Bidirectional Ports
- Interrupt Capability Under Program Control
- Microprocessor-Compatible Bus Interface
- Programmable Data Direction and Control Registers
- +5-Volt-Only Operation
- TTL-Compatible Inputs and Outputs

Block Diagram

The following figure, D-45, is a block diagram representation of the functions contained within the Peripheral Interface Adapter. Figure D-46 is a drawing of the actual DIP pin assignments.

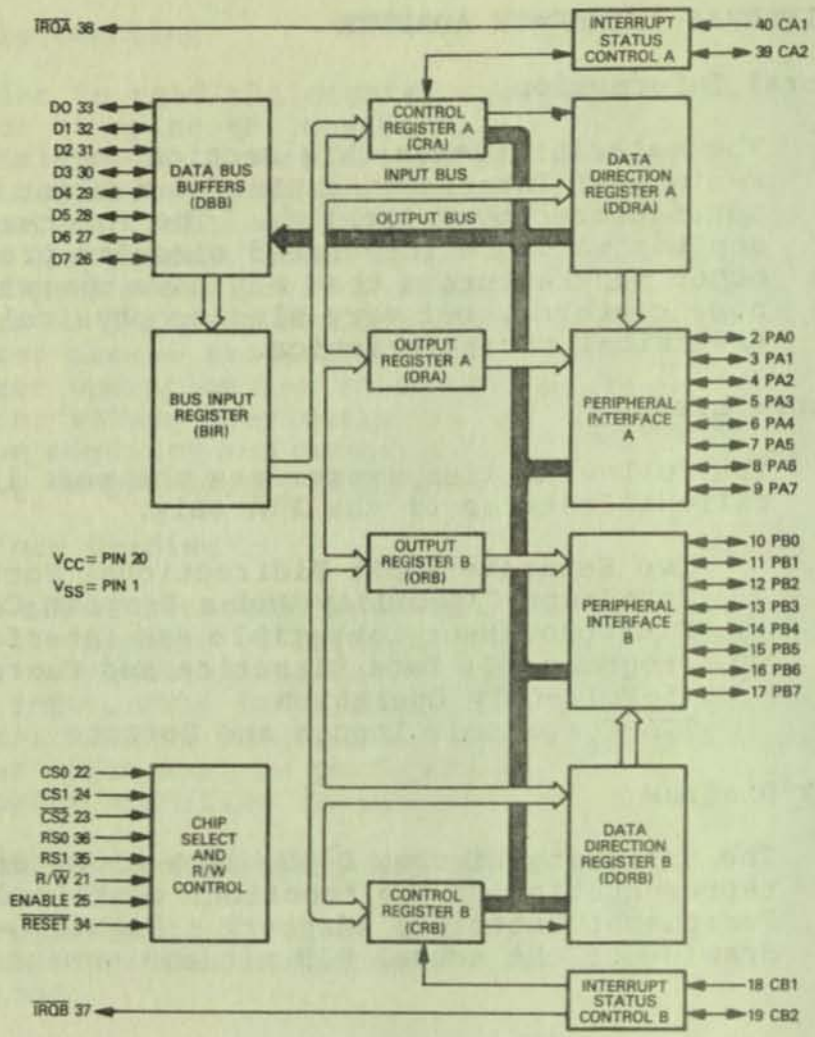


FIGURE D-45. PIA BLOCK DIAGRAM

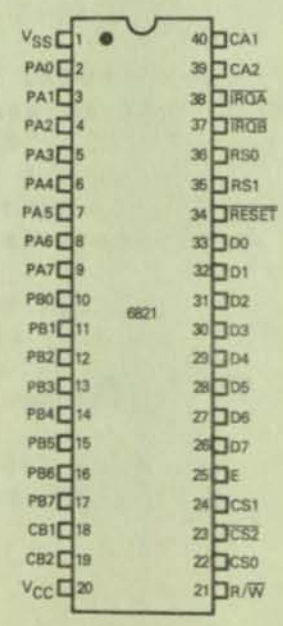


FIGURE D-46. PIA PIN ASSIGNMENTS

Overall Description

The Peripheral Interface Adapter contains two eight-bit parallel ports that can be manipulated by system software to act as either inputs or outputs and provides four control lines that allow interrupts to be received or generated under software control. The data direction and use of control lines for the parallel ports is set up by the software which configures the control register for the applicable port.

The Peripheral Interface Adapter consists of the following functional blocks:

Data Bus Buffer
Bus Input Registers
Chip Select and Read/Write Control
Control Registers A and B
Output Registers A and B
Data Direction Registers A and B
Peripheral Interface A and B
Interrupt Status Control A and B

Pin Description

Table D-9 summarizes the function of each pin of the Peripheral Interface Adapter chip.

Table D-9. Peripheral Interface Adapter Pin Functions

Pin	Mnemonic	Function
2 - 9	PA0 - PA7	**Parallel Port A Data.** These eight lines provide the parallel data interface for port A of the Peripheral Interface Adapter. It is over these pins that data may be transferred to and from a peripheral device connected to Port A.
10-17	PB0 - PB7	**Parallel Port B Data.** These eight lines provide a similar function to the PA0-PA7 lines, except for Data Port B.
18	CB1	**Port B Interrupt.** This signal is an input only and is used to set the interrupt flag of Control Register B.
19	CB2	**Port B Control.** This signal may be used as as either an input or output. When used as an input, it is used to set the interrupt flag of Control Register B. When used as an output its function is controlled by Control Register B.
21	R/W*	**READ/WRITE.** The host processor uses this line to control the direction of data flow. When this signal is high, data is being transferred from the Peripheral Interface Adapter to the host processor. When the signal is low data is being transferred from the host processor to the chip.
22-24	CS0,1,2*	**Chip Selects.** These three input signals are used to select the Peripheral Interface Adapter. The chip is enabled only when CS0 and CS1 are high and CS0* is low. Any other states on these lines will disable the device
25	E	**Enable.** This signal is a timing or clock signal into the chip to which all of the internal device timing is referenced.

Note: An asterisk (*) denotes an active-low signal.

TABLE D-9. PERIPHERAL INTERFACE ADAPTER PIN FUNCTIONS (Cont.)

PIN	MNEMONIC	FUNCTION
26-33	D7 - D0	**Data Bus.** These eight lines provide the bi-directional data path to the host processor
34	RESET*	**Reset.** This signal is an input and is used to initialize the chip to a known state. This line is active low and may be generated during power-on reset or master clear.
35-36	RS1,0	**Register Select 1,0.** These signals are used in conjunction with bit 2 of the control registers to address the various registers within the chip.
37-38	IRQA*,B*	**Interrupt Request.** These lines are used as interrupt request inputs to the host processor based on activity of the interrupt and control lines for the particular port. These lines may be tied together in a "wired-or" configuration.
39	CA2	**Port A Control.** This signal is similar to the Port B Control signal described above, except it applies to port A.
40	CA1	**Port A Interrupt.** This signal is similar to the Port B Interrupt signal described above, except it applies to port A.

Note: An asterisk (*) denotes an active-low signal.

Hardware Functional Description

Data Bus Buffer

The data bus buffer allows the PIA to interface to the system data bus. This consists of an eight-bit, tri-state bidirectional buffer arrangement used to place data onto the data bus during read cycles and to accept data from the data bus during write cycles.

Bus Input Register

When data is written to the PIA from the host, it is placed in the Bus Input Register. Then, depending on the state of the Register Select inputs RS0 and RS1, and the state of bit two of the control register, the data in the Bus Input Register is transferred into one of the following internal PIA registers:

Control Register A
Control Register B
Data Direction Register A
Data Direction Register B
Output Register A
Output Register B

Chip Select and Read/Write Control

The Chip Select and Read/Write Control section of the PIA is used to create all of the PIA internal control signals for reading, writing, and controlling data flow to and from the chip. CS0, CS1, and CS2 are used to enable the chip; RS0 and RS1 are used to address the internal registers; R/W* is the read/write control; ENABLE is a clock signal that is used to generate internal chip timing; RESET* serves to initialize all internal storage elements.

Control Registers A, B

These two control registers allow the host processor to enable and monitor interrupts, to control peripheral input and output lines, and control the direction of data flow to and from external peripheral devices.

Output Registers A, B

These registers may be loaded with the data bits being output to the peripheral device. If the corresponding Data Direction Register bit is set high, the data will appear at the output of the PIA. A high level in the Output Register will appear as a high level at the PIA output, and a low will appear as a low. A bit set low in the Data Direction

Register will cause the peripheral device bit to be input to the host. The data in the Output Registers may be written and read by the host processor.

Data Direction Registers A, B

These registers are used to individually control the input/output direction of each bit stored in the Output Registers. A high bit causes the corresponding bit of the Output Register to appear at the PIA input/output pin. A low bit causes the corresponding bit at the PIA input/output pin to appear as an input to the host processor during a read cycle.

Peripheral Interface A, B

Both Peripheral Interface A and B sections act as eight bit bidirectional ports to peripheral devices, but with differing characteristics. The A side is designed to drive CMOS logic to normal 30% to 70% levels, and has an internal pull-up. The A side, then, requires more drive current in the input mode than the B side. The B side uses normal three-state NMOS buffers which cannot pull-up to CMOS levels without external pull-up resistors. The B side can drive heavier loads than the A side.

Interrupt Status Control A, B

Bits 3, 4, and 5 of Control Registers A and B are used to control the Peripheral Device lines CA2 and CB2. Bits 0 and 1 of the Control Registers are used to control the Peripheral Device Lines CA1 and CB1. CA2 and CB2 can be used as either interrupt inputs or output control signals. CA1 and CB1 are used as interrupts only. When used as outputs, CA2 and CB2 have slightly different loading characteristics.

Maximum Ratings

Listed below are the maximum ratings of the Peripheral Interface Adapter. If these ratings are exceeded, permanent damage to the device may result. Also, exposure to the maximum ratings for extended periods may affect the reliability of the device.

Supply Voltage	-0.3 V to 7.0 V
Input Voltage	-0.3 V to 7.0 V
Operating Temperature	0 to 70 Degrees Centigrade
Storage Temperature	-55 to 150 Degrees Centigrade

Electrical Characteristics

Listed below are the D.C. and A.C. electrical characteristics of the Peripheral Interface Adapter. These characteristics apply at a power supply voltage of 5.0 VDC±5%, and a ground voltage (Vss) of 0 VDC unless otherwise noted.

Refer to figures D-47 through D-55 for more information regarding the timing parameters mentioned below.

TABLE D-10. PERIPHERAL INTERFACE ADAPTER D.C. AND A.C. ELECTRICAL CHARACTERISTICS

Characteristic	Min	Typ	Max	Unit
Bus Control Inputs (CS0,CS1,CS2,RS0,RS1,R/W*,Enable,Reset*)				
Input High Voltage (Vih)	Vss+2.0	-	Vcc	V
Input Low Voltage (Vil)	Vss-0.3	-	Vss+0.8	V
Input Leakage Current (Iin)	-	1.0	2.5	uA
Capacitance (Cin)	-	-	7.5	pF
Interrupt Outputs (IRQA*, IRQB*)				
Output Low Voltage (Vol)(Iload=3.2 ma)			Vss+0.4	V
Three State Output Leakage (Ioz)	-	1.0	10	uA
Capacitance (Cout)	-	-	5	pF
Data Bus (D0 - D7)				
Input High Voltage (Vih)	Vss+2.0	-	Vcc	V
Input Low Voltage	Vss-0.3	-	Vss+0.8	V
Three State Input Leakage (Iiz)	-	2.0	10	uA
Output High Voltage (Voh)(Iload=-205uA)	Vss+2.4	-	-	V
Output Low Voltage (Vol)(Iload=1.6 ma)	-	-	Vss+0.4	V
Capacitance (Cin)	-	-	12.5	pF

TABLE D-10 (Cont.)

Characteristic	Min.	Typ.	Max.	Unit
Peripheral Bus (CA1,CA2,CB1,CB2,PA0-7,PB0-7)				
Input Leakage Current (Iin)	-	1.0	2.5	uA
Three State Leakage (Iiz)(PB0-7,CB2)	-	2.0	10	uA
Input High Current (Iih)(PA0-7,CA2)	-200	-400	-	uA
Darlington Drive (Ioh)(PB0-7,CB2)	-1.0	-	-10	mA
Input Low Current (Iil)(PA0-7,CA2)	-	-1.3	-2.4	mA
Output High Voltage (Voh)				
Iload = -200 uA)(PA0-7,PB0-7,CA2,CB2)	Vss+2.4	-	-	V
Iload = -10 uA)(PA0-7,CA2)	Vcc-1.0	-	-	V
Output Low Voltage (Vol)(Iload=3.2 mA)	-	-	Vss+0.4	V
Capacitance (Cin)	-	-	10	pF
Power Requirements				
Internal Power Dissipation (Pint)			550	mW

Bus Timing Characteristics	Min	Max	Units
Cycle Time (Tcyc), #1	1.0	10	us
Pulse Width, E Low (PWel), #2	430	—	ns
Pulse Width, E High (PWeh), #3	450	—	ns
Clock Rise and Fall Time (Tr,Tf), #4	—	25	ns
Address Hold Time (Tah), #9	10	—	ns
Address Setup Time Before E (Tas), #13	80	—	ns
Chip Select Setup Time Before E (Tcs), #14	80	—	ns
Chip Select Hold Time (Tch), #15	10	—	ns
Read Data Hold Time (Tdhr), #18	20	50*	ns
Write Data Hold Time (Tdhw), #21	10	—	ms
Output Data Delay Time (Tddr), #30	—	290	ns
Input Data Setup Time (Tdsw), #31	165	—	ns

TABLE D-10 (Cont.)

Peripheral Timing Characteristics

Characteristics	Min.	Max.	Units
Data Setup Time (Tpds)	200	—	ns
Data Hold Time (Tpdh)	0	—	ns
E Low to CA2 Low (Tca2)	—	1.0	us
E Low to CA2 High (Trs1)	—	1.0	us
CA1, CA2 Rise, Fall Time (Tr, Tf)	—	1.0	us
CA1 Active to CA2 High (Trs2)	—	2.0	us
E Low to Data Valid (Tpdw)	—	1.0	us
E Low to PA0-7, CA2 Data Valid (Tcmos)	—	2.0	us
E High to CB2 Low (Tcb2)	—	1.0	us
Data Valid to CB2 Low (Tdc)	20	—	ns
Enable High to CB2 Highm (Trs1)	—	1.0	us
CA2/CB2 Pulse Width (PWct)	500	—	ns
CB1, CB2 Rise, Fall Time (Tr, Tf)	—	1.0	us
CB1 Active to CB2 High (Trs2)	—	2.0	us
Interrupt Release Time, IRQA*/IRQB* (Tir)	—	1.6	us
Interrupt Response Time (Trs3)	—	1.0	us
Interrupt Input Pulse Time (PW1)	500	—	ns
RESET* Low Time** (Trl)	1.0	—	us

* The Data Bus Output Buffers are no longer sourcing or sinking current by Tdhr max (High Impedance).

** The RESET* Line must be held high a minimum of 1.0 us before addressing the chip.

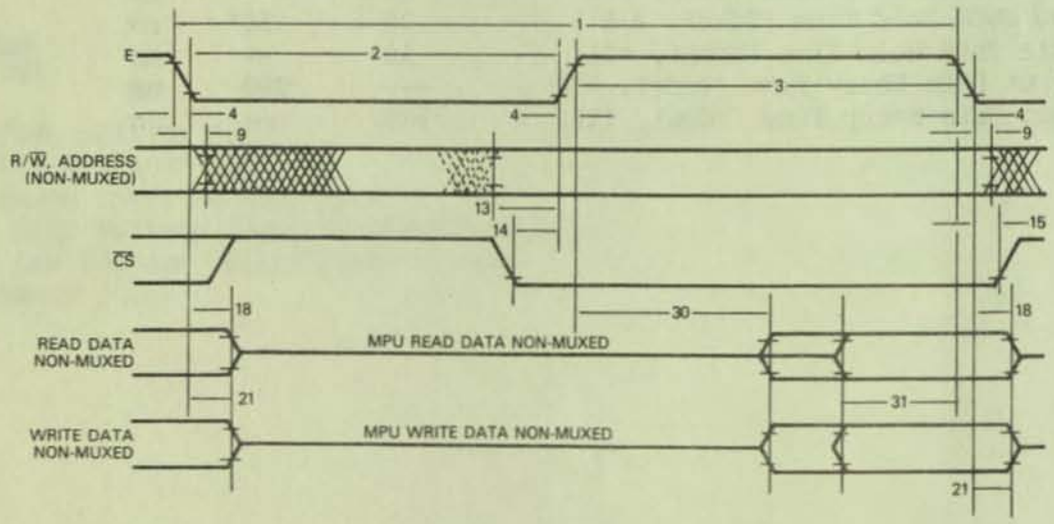


FIGURE D-47. PIA BUS TIMING

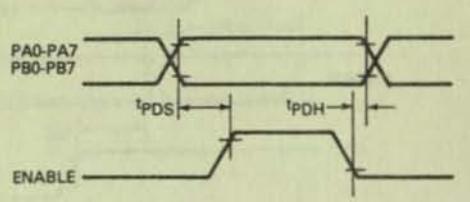


FIGURE D-48. PIA DATA SETUP AND HOLD TIMES (Read Mode)

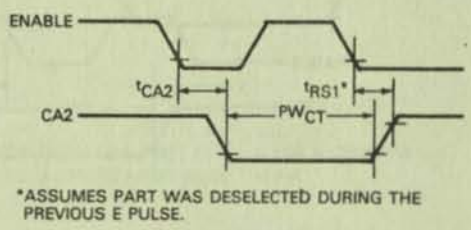


FIGURE D-49. PIA CA2 DELAY TIME (Read Mode: CRA-5=CRA-3=1, CRA-4=0)

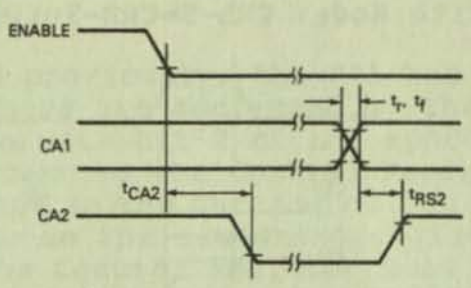


FIGURE D-50. PIA CA2 DELAY TIME (Read Mode: CRA-5=1, CRA-3=CRA-4=0)

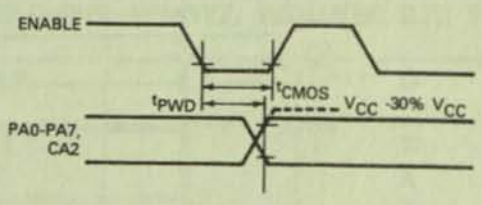
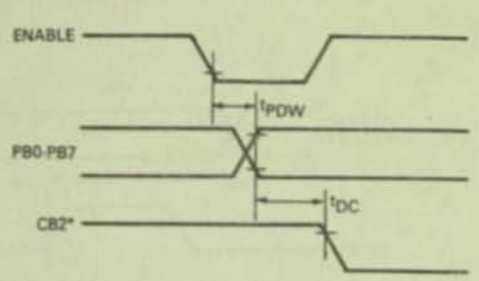
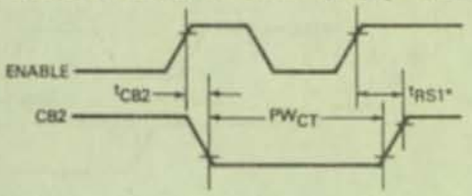


FIGURE D-51. PIA DATA DELAY TIMES (Write Mode: CRA-5=CRA-3=1, CRA-4=0)



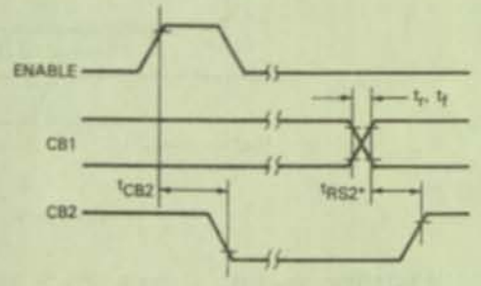
*CB2 GOES LOW AS A RESULT OF THE POSITIVE TRANSITION OF ENABLE.

FIGURE D-52. PIA DATA AND CB2 DELAY TIMES (Write Mode: CRB-5=CRB-3=1, CRB-4=0)



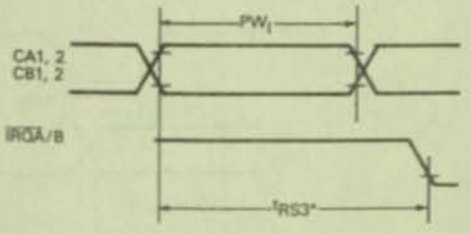
*ASSUMES PART WAS DESELECTED DURING THE PREVIOUS E PULSE.

FIGURE D-53. PIA CB2 DELAY TIME (Write Mode: CRB-5=CRB-3=1, CRB-4=0)



*ASSUMES PART WAS DESELECTED DURING ANY PREVIOUS E PULSE.

FIGURE D-54. PIA CB2 DELAY TIME (Write Mode: CRB-5=1, CRB-3=CRB-4=0)



*ASSUMES INTERRUPT ENABLE BITS ARE SET.

FIGURE D-55. PIA INTERRUPT PULSE WIDTH AND IRQ* RESPONSE

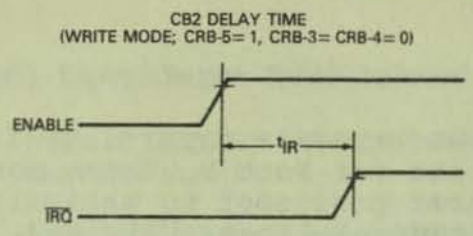
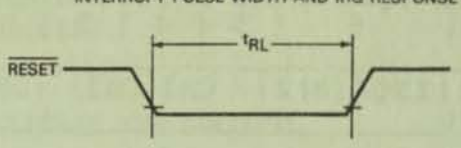


FIGURE D-56. PIA IRQ* RELEASE TIME



*THE RESET LINE MUST BE A V_{IH} FOR A MINIMUM OF 1.0 μs BEFORE ADDRESSING THE PIA.

FIGURE D-57. RESET* LOW TIME

Software Addressing

As mentioned previously, the PIA has several internal registers. These are addressed by the RS0 and RS1 inputs, along with bit 2 of the appropriate control register. Access to the Control Register does not, of course, depend on the setting of its own bit number 2, but access to the remaining registers does. Therefore, the Control Register must be set up before attempting to access any other register of the PIA. Table D-11 below summarizes the PIA register addresses:

TABLE D-11. PIA Register Address Map

REGISTER	REGISTER SELECT BIT		CONTROL REGISTER BIT #2	
	RS1	RS0	A	B
CONTROL A	0	1	X	X
CONTROL B	1	1	X	X
DDR A	0	0	0	X
DDR B	1	0	X	0
PER A	0	0	1	X
PER B	1	0	X	1

Control Register

There are two separate control registers, one for Port A and one for Port B. These control registers allow the host processor to manipulate the four peripheral control lines, CA1, CA2, CB1, and CB2. Via the control registers, the host also may enable interrupt lines and monitor interrupt status flags. The format of the control registers is given in Figure D-58.

7	6	5	4	3	2	1	0
IRQA(B)1	IRQA(B)2	CA2(CB2)			DDR	CA1(CB1)	

FIGURE D-58. PIA CONTROL REGISTERS A AND B FORMAT

Bit 0—Interrupt Request Enable/Disable

Zero: Disables IRQA(B) interrupt by CA1(CB1) active transition. IRQA(B) will occur on the next positive transition of this bit caused by the host processor if CA1(CB1) active transition occurred while the interrupt was disabled.

One: Enables IRQA(B) interrupt by CA1(CB1) active transition.

Bit 1—Determine CA1(CB1) Active Transition for Setting Interrupt Flag IRQA(B)1

Zero: IRQA(B)1 set by high-to-low transition on CA1(CB1)

One: IRQA(B)1 set by low-to-high transition on CA1(CB1)

Bit 2—Data Direction Register/Output Register Select

Zero: Data Direction Register Selected

One: Output Register Selected

Bits 3, 4, 5—CA2(CB2) Input/Output Establishment

Bits 5	4	3	
0	X	X	CA2(CB2) are inputs
0	X	0	Disables IRQA(B) interrupt by CA2(CB2) transition. IRQA(B) will occur on the next host processor positive transition of bit 3 if CA2(CB2) active transition occurred while the interrupt was disabled.

Bits 3, 4, 5—CA2(CB2) Input/Output Establishment (Cont.)

0	X	1	Enables IRQA(B) interrupt by CA2(CB2) active transition.
0	0	X	IRQA(B)2 set by high-to-low transition of CA2(CB2).
0	1	X	IRQA(B)2 set by low-to-high transition of CA2(CB2).
1	X	X	CA2(CB2) are outputs.
1	0	0	Read Strobe with CA1 Restore. CA2 goes low on the first low going Enable transition following a read by the host of the A Output Register. It is returned as a high by the next active CA1 transition.
1	0	1	Read Strobe with E Restore. CA2 goes low on the first low transition following a read by the host of output register A. It is returned high by the next low-going E transition during a deselect.
1	0	0	Write Strobe with CB1 Restore. CB2 goes low with the first high transition of E following a host write into Output Register B. It is returned high by the next active CB1 transition. Bit 7 of Control Register B must first be cleared by a read of data.
1	0	1	Write Strobe with E Restore. CB2 goes low on the first low transition of E following a host write into Output Register B. It is returned high by the next high E transition following an E pulse occuring during the time that the chip was not selected.
1	1	0	CA2(CB2) goes low when the host writes a zero into bit 3 position of the Control Register.
1	1	1	CA2(CB2) goes high when the host writes a one into bit 3 of the Control Register.

Bit 6—IRQA(B)2 Interrupt Flag

When CA2 or CB2 are being used as inputs, IRQA(B) goes high on the active transition of CA2(CB2). This bit is cleared by a host read of Output Register A(B) or by a hardware reset condition. If CA2 or CB2 is being used as output, IRQA(B)2 is always set to zero and is not affected by CA2 (CB2) transition(s).

Bit 7—IRQA(B)1 Interrupt Flag

This signal goes high on the active transition of CA1(CB1), and is cleared by a host read of Output Register A(B) or by hardware reset.

Osborne Executive Applications Information

The two Peripheral Interface Adapter chips are used in the Osborne Executive to handle the following functions:

IEEE 488 Interface
Modem Control
Real Time Clock Interrupt (Vertical Blank Signal)
50/60 Hz Video Timing Selection
Serial Communication Port Clock Selection
Floppy Disk Drive Select
Floppy Disk Density Selector
Audio Beeper Control
Keyboard Control
Z80A Interrupt Requests
RAM Bank Enable

FLOPPY DISK CONTROLLER

General Information

The material within this section covers the Floppy Disk Controller equivalent to the MB8877M manufactured by Fujitsu or the SYP1793 manufactured by Synertek. The information also applies to those integrated circuits produced by other manufacturers that may have somewhat different nomenclatures, but very similar physical and electrical characteristics.

Feature List

The following list summarizes the most important and salient features of the Floppy Disk Controller (FDC).

- Flexible Formats
- IBM 3740 Single-Density FM
- IBM System 34 Double-Density MFM
- Operates With Both 8" and 5-1/4" Floppy Disk Drives
- Microprocessor-Bus Compatible
- Handles Write Precompensation
- DMA Data Transfer Capability
- Automatic Track Seek
- Programmable:
  - Head Step Rate
  - Head Engage/Settle Time
  - Sector Length
  - Side Compare
  - Write Operation (Single/Multiple Sector, Entire Track)
  - Read Operation (Single/Multiple Sector, Entire Track)
- +5 Volts Only
- Single 40-Pin DIP Package

Block Diagram and Pin Assignment

Figure D-59 is a block diagram representation of the functions contained within the FDC. Figure D-60 is a drawing of the actual DIP pin assignments.

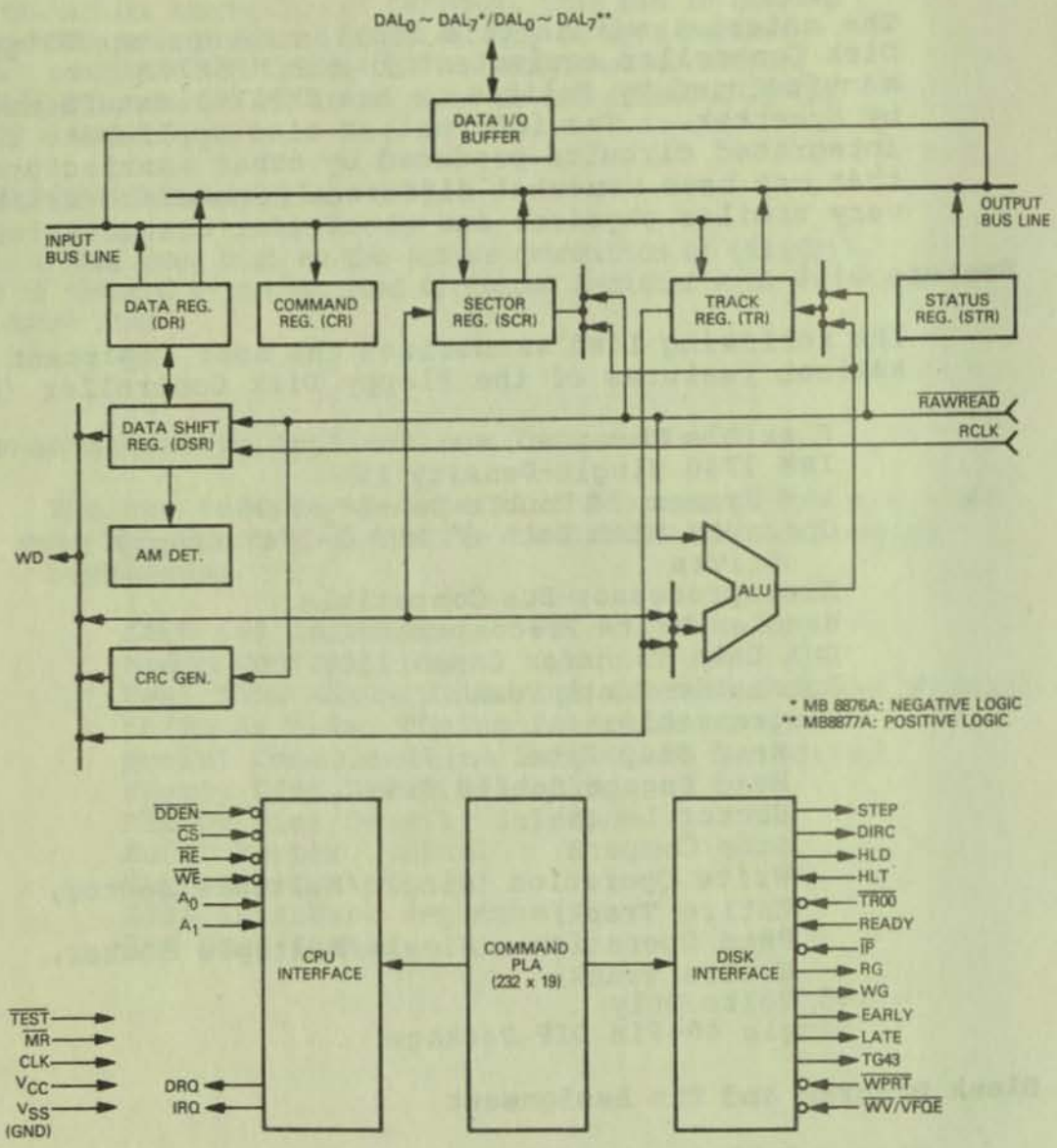


FIGURE D-59. FDC BLOCK DIAGRAM

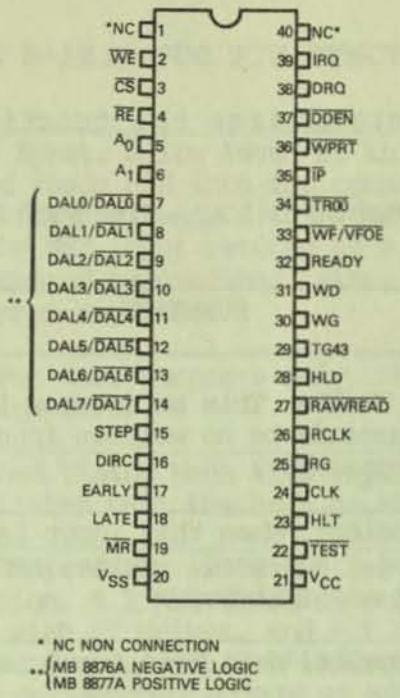


FIGURE D-60. FDC PIN ASSIGNMENTS

Overall Description

The FDC is a single-package floppy disk controller. The FDC performs all those functions that a host microprocessor needs in order for it to read data from or write data to a floppy disk. Both 5-1/4" and 8" single- and double-density storage configurations are supported with this device.

The FDC contains a microprocessor interface which allows it to communicate over a standard address, data, and control bus to all bus-oriented microprocessors.

The floppy disk interface consists of all the signals normally required by industry-standard floppy disk drives. The FDC will not only read and write, but will also format the diskette in IBM standard single- and double-density formats. This is done under processor command. Once the command has been received by the FDC, the rest is automatic.

The FDC consists of the following functional blocks:

Command Register	ALU
Status Register	Data Modulator
Data Register	Programmable Logic Array
Data Shift Register	Sector Register
Track Register	
CRC Circuit	
Address Mark Detection Circuit	

Pin Description

Table D-12 summarizes the function of each pin of the FDC.

TABLE D-12. FDC PIN FUNCTIONS

PIN	MNEMONIC	FUNCTION
2	WE*	**Write Enable.** This active-low input allows data and commands to be written into the FDC from the host processor.
3	CS*	**Chip Select.** When this input is low, the FDC is enabled, and read, write, and command sequences can be accomplished.
4	RE*	**Read Enable.** When this input is low, the FDC places its data or status information onto the data bus so that the processor may read it.
5,6	A0,A1	**Address.** These two lines allow the processor to select a particular FDC internal register for a read or write operation.
7-14	D0-D7	**Data Bus.** These eight bits provide for the transfer of bidirectional data between the FDC and the processor. The direction of transfer is determined by the state of the RE* and WE* lines.
15	STEP	**Step.** This output provides a pulse to the floppy disk drive for each track the drive is to increment either in the inward or outward direction.
16	DIR	**Direction.** This output is provided to the floppy disk drive and is high when the drive is to step toward the inward tracks and low when it is to step in the outward direction.
17	EARLY	**Early.** When this signal is active high, it indicates that the data being written to the drive should be shifted early for purposes of write precompensation.
18	LATE	**Late.** When this signal is active high, it indicates that the data being written to the drive should be shifted late for purposes of write precompensation.

Note: An asterisk (*) denotes an active-low signal.

TABLE D-12. FDC PIN FUNCTIONS (Cont.)

19	MR*	**Master Reset.** A low level at this input resets the FDC and loads 03H into the command register. Status bit 7, the Not Ready bit, is set at this time also. When the MR* input returns to a high level, a Restore command is executed. Also, 01H is loaded into the sector register.
22	TEST*	**Test.** For test purposes only. This is normally tied to a high level.
23	HLT	**Head Load Timing** When this input is at a high level it indicates that the head on the drive is engaged
24	CLK	**Clock.** This input is used for internal timing generation. A 2 MHz clock is required for interfacing with 8" drives, and a 1 MHz clock, for interfacing with 5-1/4" drives.
25	RG/SSO	**Side Select Output.** This output, when high, indicates to the drive that side number 0 of the drive is selected. A low level indicates that side number 1 is selected.
26	RDCLK	**Read Clock.** This input is clock that has been separated from the incoming data stream. The relationship of RDCLK transitions relative to incoming read data is critical.
27	RAWRD*	**Raw Read Data.** This input is the data from the disk drive after it has been separated from the clock.
28	HLD	**Head Load.** This output may be used to load the drive head against the diskette.
29	TG43	**Track > 43.** When this output is high, it indicates that the head is positioned on any of the tracks from 44 through 76. When low, it indicates that the head is located on any of the tracks from 0 to 43.
30	WG	**Write Gate.** This output indicates to the drive that data is being written to the diskette.
31	WD	**Write Data.** This is the write data output. It consists of 250 ns pulses for MFM data(Double Density) or 500 ns pulses for FM data (Single Density). WD also contains the address marks and embedded clock.

Note: An asterisk (*) denotes an active-low signal.

TABLE D-12. FDC PIN FUNCTIONS (Cont.)

32	RDY	**Ready.** This input informs the FDC that the disk drive is ready for a read or write operation.
33	WF*/VFOE*	**Write Fault/VFO Enable.** This is a bidirectional signal. When WG is high, it serves as an input to monitor write faults as reported by the drive during a write sequence. If WF goes low, indicating write fault, any write command will terminate. When WG is high, pin 33 serves as a VFOE output to an external PLO data separator.
34	TR00*	**Track 0.** This input is from the drive and indicates that the head is positioned over track 0.
35	INDEX*	**Index.** This input from the drive pulses each time the index hole in the diskette passes by the sensor built into the drive.
36	WPRT*	**Write Protect.** This signal comes from the drive and informs the FDC that no write operation is to be performed on the disk.
37	DDEN*	**Double-Density Enable.** This input selects the density with which data is to be read and written. A low level selects the double-density option.
38	DRQ	**Data Request.** This output indicates when the Data register contains data during read operations, or is empty during write operations. When the processor reads or writes the data register, this output is reset.
39	INTRQ	**Interrupt Request.** This output is set high at the end of any operation and is reset when a new command is loaded into it from the processor, or when the status register is read.

Note: An asterisk (*) denotes an active low signal.

Hardware Functional Description

Data Register

This register is accessible by the processor and may be both written and read. During a read operation, this eight-bit register gets loaded in parallel from the Data Shift Register which contains the serial data coming from the drive. During write operations, the processor loads up the Data Register with an eight-bit parallel word. The data is then loaded in parallel to the Data Shift Register and then shifted out serially to the disk drive. Therefore the Data Register serves as a temporary data buffer between the processor and drive.

Data Shift Register

This is an eight-bit shift register which is the direct interface to the disk drive from the FDC. Serial data coming from the drive is shifted serially into this register and then loaded into the Data Register as a single eight-bit parallel word. The data is then accessible by the CPU. Data coming from the processor is transferred in parallel from the Data Register into the Data Shift Register and then transferred serially out to the drive.

Command Register

This register is written into from the CPU to cause the FDC to execute a particular command. The CPU must wait until the BUSY bit of the Status Register is low before attempting to load in a command. After the command that was loaded is finished executing, the FDC sets the FDC Interrupt-Request output pin high.

Status Register

This register contains eight bits of data which may be read by the CPU to gain knowledge of the operating status of the FDC. After the status has been read, the FDC automatically resets the Interrupt Request pin.

Sector Register

This byte is used by the processor to designate the required sector number for both read and write operations to the disk drive.

Track Register

For Read Data and Write Data commands issued by the CPU, this register contains the track number to be used during the execution of the command. For Step-in, Step-out, Step, and Restore commands, this register contains the present track number.

Data Modulator

This circuit prepares the data being written to the disk so that it is in the proper single- or double-density format. For single-density recording, the data gets modulated in Frequency Modulated (FM) format, and for double-density, it gets modulated in Modified Frequency Modulation (MFM).

Address Mark Detection Circuit

This circuit is capable of detecting the following unique data patterns encoded into the serial data:

Index Mark
ID Address Mark
Data Address Mark

CRC Check Circuit

During write operations the FDC automatically calculates a 16-bit CRC and this data is transferred to the disk along with the normal data. When the data is read back from the disk, a new CRC is calculated based on the incoming data and then compared against the CRC coming off the disk. This is how error checking is performed. The polynomial used is $G(x) = x16+x12+x5+1$.

Arithmetic Logic Unit

The Arithmetic Unit is a serial comparator, incrementer, and decrementer and is used for modifications to the registers and for comparisons with the disk-recorded ID field.

Programmable Logic Array

This circuit allows the FDC to execute a micro-program which generates the control signals for the FDC. The size of the program is around 232 X 19 bits.

Maximum Ratings

Listed below are the maximum ratings of the Floppy Disk Interface. If these ratings are exceeded, permanent damage to the device may result. Also, exposure to the maximum ratings for extended periods may affect the reliability of the device.

Voltage On Any Pin	-0.3 to +7.0 Volts
Operating Temperature	0 to 70 Degrees C
Storage Temperature	-55 to 150 Degrees C

Electrical Characteristics

Listed below are the D.C and A.C. characteristics of the FDC. These characteristics apply, unless otherwise noted, at an ambient temperature of 0 to 70 degrees Centigrade, Vcc=+5V±5%, and Vdd=+12V±5%.

Figures D-61 through D-65 give more information regarding the timing parameters listed:

TABLE D-13. FDC D.C. AND A.C. ELECTRICAL CHARACTERISTICS

Parameter	Min.	Max.	Units
Output High Voltage (Voh) (Ioh=-200ua)	2.4		V
Output Low Voltage (Vol) (Iol=1.8 ma)		0.4	V
Power Consumption (Pc)		350	Mw
Input Leakage Current (Iinl) (Except for HLT,TEST*,WE*,WPRT*,DDEN*)		2.5	ua
Input Leakage Current (Iin2) (For HLT,TEST*,WE*,WPRT*,DDEN*)		100	ua
Three State Input Current (Itsi)		10	ua
Three State Output Leakage (Iloh)		10	ua
READ TIMING (PROCESSOR/FDC)			
Address Setup Time (Tset)	50		ns
Address Hold Time (Thld)	10		ns
RE* Pulse Width (Tre)	280		ns
DRQ Reset Time (Tdrr)		250	ns
IRQ Reset Time (Tirr)		500	ns
Data Delay Time (Tdacc)		250	ns
Data Hold Time (Tdoh)	50	150	ns
DRQ Service Time (Tsevr) (for RDCLK cycle=2 us)		13.5**	us

Note: ** These values are doubled for CLK=1 MHz

TABLE D-13 (Cont.)

Parameter	Min.	Max.	Units
WRITE TIMING (PROCESSOR/FDC)			
Address Setup Time (Tset)	50		ns
Address Hold Time (Thld)	10		ns
WE* Pulse Width (Twe)	200		ns
DRQ Reset Time (Tdrr)		250	ns
IRQ Reset Time (Tirr)		500	ns
Data Setup Time (Tds)	250		ns
Data Hold Time (Tdh)	0		ns
DRQ Service Time (Tsevw) (DDEN*=low)		11.5**	us

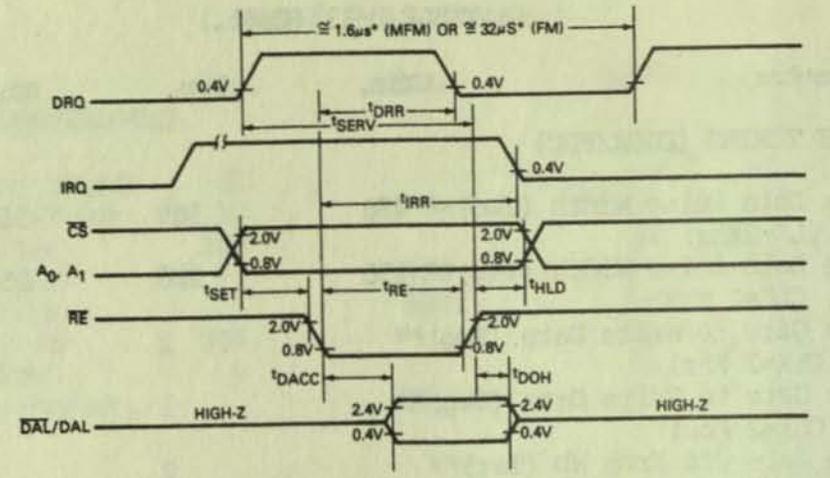
Parameter	Min.	Typ.	Max.	Units
READ TIMING (DISK/FDC)				
RAWRD* Pulse Width (Tpw)	100		250**	ns
Clock Setup Time (Td)	40			ns
Clock Hold Time for MFM (Tcd)	40			ns
Clock Hold Time for FM (Tcs)	40			ns
RAWRD* FM Cycle Time (Tbc)		2**,3**, or 4**		us
RAWRD* MFM Cycle Time (Tbc)		2** or 4**		us
RDCLK MFM High Pulse Width (Ta)	0.8	1**	20	us
RDCLK FM High Oulse Width (Ta)	0.8	2**	20	us
RDCLK MFM Low Pulse Width (Tb)	0.8	1**	20	us
RDCLK FM Low Pulse Width (Tb)	0.8	2**	20	us
RDCLK MFM Cycle Time (Tc)		2**		us
RDCLK FM Cycle Time (Tc)		4**		us

TABLE D-13 (Cont.)

Parameter	Min.	Typ.	Max.	Units
WRITE TIMING (DISK/FDC)				
Write Data Pulse Width (Twd)** (FM, CLK=2Mhz)	450	500	550	ns
Write Data Oulse Width (Twd)** (MFM, CLK=2 Mhz)	150	200	250	ns
Write Gate to Write Data (Twg)** (FM, CLK=2 Mhz)		2		us
Write Gate to Write Data (Twg)** (FM, CLK=2 Mhz)		1		us
Write Gate Off From WD (Twr)** (FM, CLK=2 Mhz)		2		us
Write Gate Off From WD (Twr)** (MFM, CLK=2 Mhz)	1		2	us
Early (Late) to Write Data (Ts) (MFM, CLK=2 Mhz)	125			ns
Early (Late) From Write Data (Th) (MFM, CLK=2 Mhz)	-50			ns
WD Valid After CLK (Tdl) (MFM, CLK=1 Mhz)	200			ns
WD Valid After CLK (Tdl) (MFM, CLK=2 Mhz)	30			ns
WD Valid to CLK (Td2) (MFM, CLK=1 Mhz)	50			ns
WD Valid to CLK (Td2) (MFM, CLK=2 Mhz)	50			ns

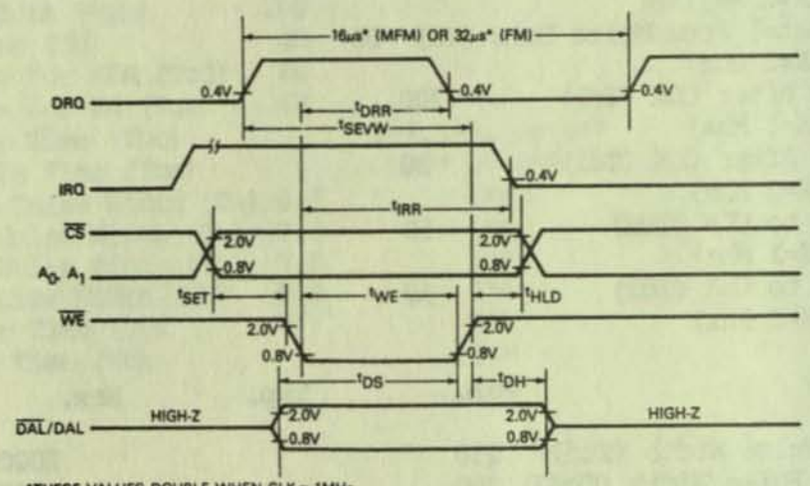
Parameter	Min.	Typ.	Max.	Units
CLK Low Pulse Width (Tcdl)	230		20000	ns
CLK High Pulse Width (Tcd2)	200		20000	ns
STEP Pulse Width, MFM (Tstp)	2**			us
STEP Pulse Width, FM (Tstp)	4**			us
DIR Setup Time (Tdir)	12**			us
MR* Pulse Width (Tmr)	50**			us
INDEX* Pulse Width (Tip)	10**			us
WF* Pulse Width (Twf)	10**			us
CLK Cycle Time (Tcyc)		0.5**		us

Note: ** These times are doubled when CLK=1 MHz.



*THESE VALUES ARE DOUBLED WHEN CLK = 1MHz

FIGURE D-61. PROCESSOR/FDC READ TIMING



*THESE VALUES DOUBLE WHEN CLK = 1MHz

FIGURE D-62. PROCESSOR/FDC WRITE TIMING

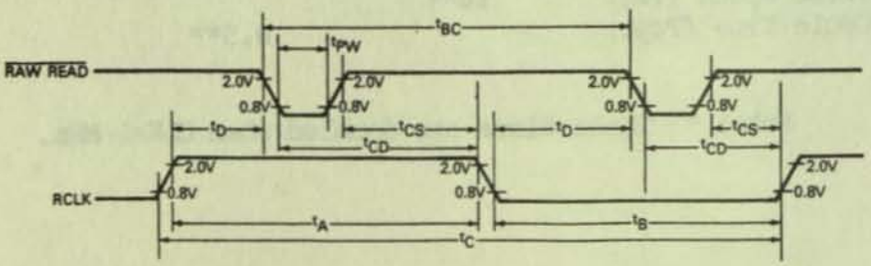


FIGURE D-63. DISK/FDC READ DATA TIMING

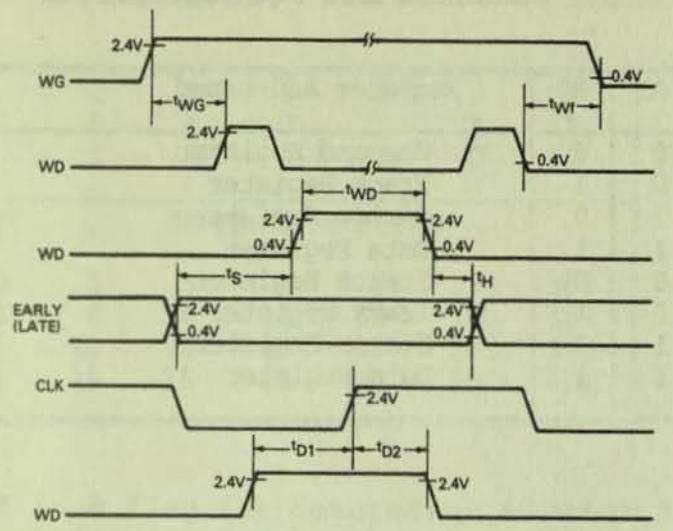


FIGURE D-64. DISK/FDC WRITE DATA TIMING

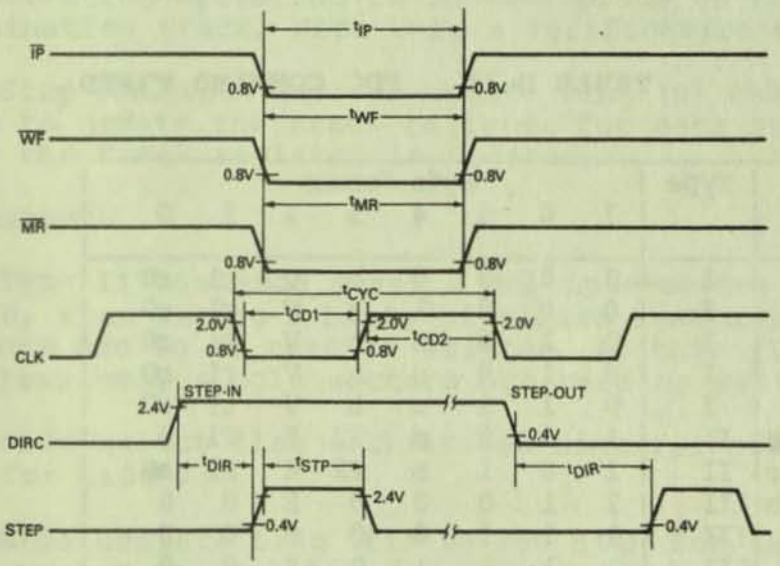


FIGURE D-65. FDC MISCELLANEOUS TIMING

Software Addressing

The FDC is programmed by writing to its internal registers. FDC status is read by accessing the internal status register. The register addressing information is given in Table D-14.

TABLE D-14. FDC ADDRESSING

WE*	RE*	A1	A0	Register Addressed
0	1	0	0	Command Register
0	1	0	1	Track Register
0	1	1	0	Sector Register
0	1	1	1	Data Register
1	0	0	0	Status Register
1	0	0	1	Track Register
1	0	1	0	Sector Register
1	0	1	1	Data Register

Commands

Commands must be loaded into the command register only when the busy status bit of the status register is off. The commands executed by the FDC fall into four basic categories, labeled Type I, II, III, and IV. There are 11 commands in all, summarized in Table D-15.

TABLE D-15. FDC COMMAND TYPES

Command	Type	Byte Format							
		7	6	5	4	3	2	1	0
Restore	I	0	0	0	0	h	V	r1	r0
Seek	I	0	0	0	1	h	V	r1	r0
Step	I	0	1	0	u	h	V	r1	r0
Step In	I	0	1	0	u	h	V	r1	r0
Step Out	I	0	1	1	u	h	V	r1	r0
Read Sector	II	1	0	0	m	F2	E	F1	0
Write Sector	II	1	0	1	m	F2	E	F1	a0
Read Address	III	1	1	0	0	0	E	0	0
Read Track	III	1	1	1	0	0	E	0	0
Write Track	III	1	1	1	1	0	E	0	0
Force Int.	IV	1	1	0	1	I3	I2	I1	I0

Type I Commands

Each of the Type I commands contains a rate field (Bits 0 and 1, r0 and r1) which determines the stepping rate as defined in Table D-16.

TABLE D-16. FDC STEPPING RATES

CLK(Mhz):		2	2	1	1	2	1
DDEN*:		0	1	0	1	X	X
TEST*:		1	1	1	1	0	0
rl	r0	Stepping Rate (ms)					
0	0	3	3	6	6	184	368
0	1	6	6	12	12	190	380
1	0	10	10	20	20	198	396
1	1	15	15	30	30	208	416

The head load flag (h) determines whether the head is to be loaded at the beginning of the command. When h=1, the HLD output goes high, and if h=0, HLD goes low.

The verification flag (V) determines if a verification operation is to take place on the destination track. When V=1, a verification is done.

The Step commands have an update flag (u) which is used to update the track register for each step. When u=1, the track register is updated.

Type II Commands

The Type II commands have a multiple-sector flag (m) which, when set to a high, signifies that multiple sectors are to be read or written. If this flag is set low, only single sectors are read or written.

The side select flag (F2) is set high for side 1 and low for side 0.

The side compare flag (F1) is set high for testing side number and set low for not testing.

The delay flag (E) is set high for a 15 ms delay between activation of HLD and HLT. It is set low for no delay.
The data address mark flag (a0) is set high when a pattern of F8H (deleted data) is to be written into the Data AM field, and low when a pattern of FBH (data) is to be written into the Data AM field.

Type III Commands

The Read Address command reads the next ID field (6 bytes) into the FDC. The Read Track command reads all bytes of the entire track, including gaps. The Write Track command writes all bytes to the track, including gaps.

Type IV Commands

The only Type IV command is the Force Interrupt command. This allows the processor to abort any command in process.

The I0, I1, I2, and I3 bits allow several conditions to be attached to this command, as given below:

I3: Immediate.	0=No Effect 1=Force INTRQ Immediately
I2: Index Pulse.	0=No Effect 1=Force INTRQ on next Index Pulse
I1: Not-Ready Transition.	0=No Effect 1=Force INTRQ when READY input goes from high to low
I0: Ready Transition.	0=No Effect 1=Force INTRQ when READY input goes from low to high

Status Register

The status register allows the processor to monitor the activity of the FDC. The status bits are summarized below.

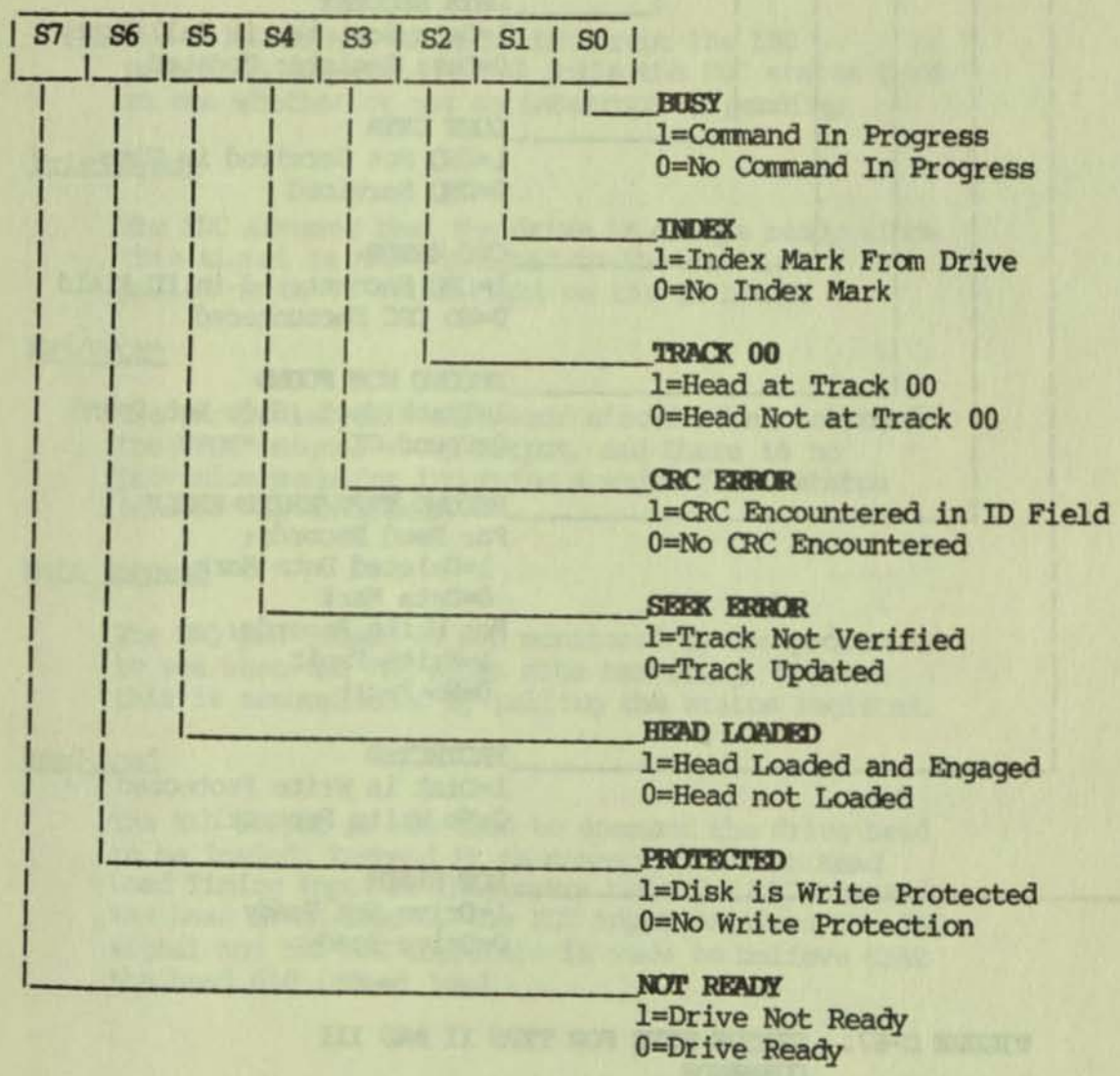


FIGURE D-66. STATUS BYTE FOR TYPE I COMMANDS

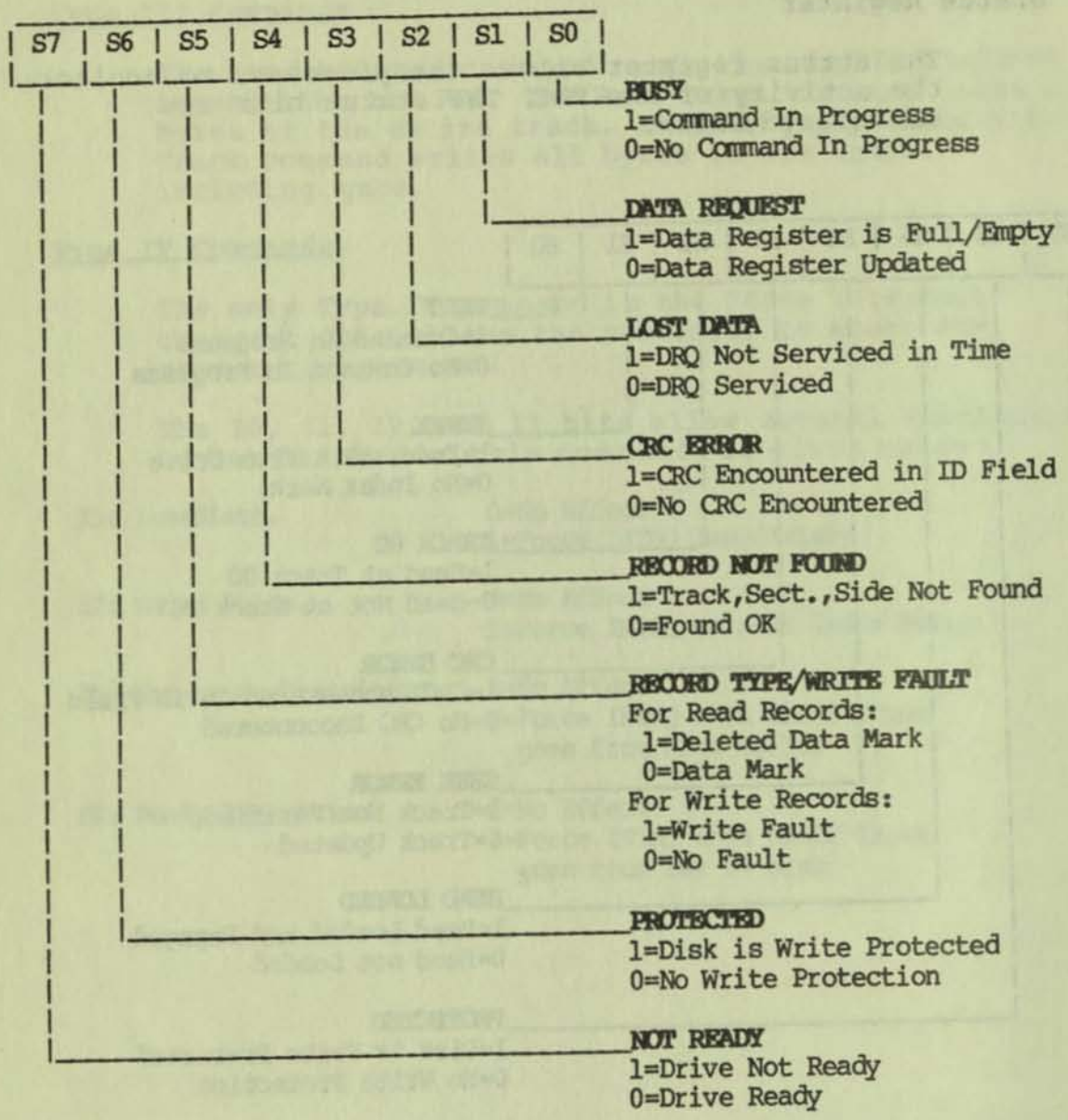


FIGURE D-67. STATUS BYTE FOR TYPE II AND III COMMANDS

Osborne Executive Applications Information

The FDC is a very flexible and powerful chip, and is used in the Executive in some unique ways that bear explaining.

Interrupts

The FDC does not directly interrupt the Z80 processor. Instead the Z80 polls the FDC status byte to see whether or not an interrupt is pending.

Drive Ready

The FDC assumes that the drive is always ready since this signal is not connected to the drive, but is pulled up to +5 volts right on the PC board.

WF*/VFOE*

The particular data-separator circuit does not need the VFOE* signal as an output, and there is no provision made for inputting a write fault status into WF* as an input.

Data Request

The DRQ pin output is not monitored by the processor to see when the FDC needs data servicing. Instead this is accomplished by polling the status register.

Head Load

The HLD output is not used to command the drive head to be loaded. Instead it is connected to the Head Load Timing input so that every time the FDC commands the head to be loaded, the HLT input receives the HLD signal and the FDC therefore is made to believe that the head did indeed load.

FLOPPY DISK DATA SEPARATOR

General Information

The material within this section covers the Floppy Disk Data Separator equivalent to the FDC 9216 manufactured by Standard Microsystems Corporation. The information also applies to those integrated circuits produced by other manufacturers that may have somewhat different nomenclatures, but very similar physical and electrical characteristics.

Feature List

The following list summarizes the most important and salient features of the Floppy Disk Data Separator chip.

- Eight Pin Dual In-Line Package (DIP)
- +5-Volt-Only Operation
- Inputs and Outputs Completely TTL Compatible
- Provides Data Separation on Frequency Modulated (FM) or Modified Frequency Modulated (MFM) Data
- No Adjustments Needed
- Compatible with Industry-Standard Floppy Disk Controller Chips

Block Diagram and Pin Assignments

Figure D-68 below is a block diagram representation of the functions contained within the Floppy Disk Data Separator. Figure D-69 is a drawing of the actual DIP pin assignments.

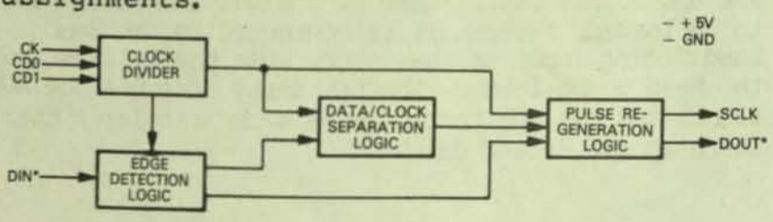


FIGURE D-68. DATA SEPARATOR BLOCK DIAGRAM

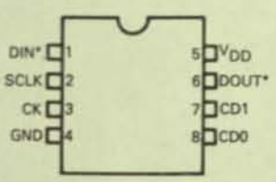


FIGURE D-69. FLOPPY DISK DATA SEPARATOR PIN ASSIGNMENTS

Overall Description

When data is recorded on a floppy disk, it is recorded as a single, serial bit stream. Within the bit stream the data is encoded in a manner that allows both clock and data information to be present. When the data is read from the disk drive, it is read as a single, serial bit stream; it is the job of the data separator chip to extract and separate the data and clock signals so that they may be presented to the floppy disk controller chip.

The data separator consists of the four following functional blocks:

Clock Divider
Edge Detector
Data/Clock Separation
Pulse Regeneration

Pin Description

Table D-17 summarizes the function of each pin of the data separator chip.

TABLE D-17. DATA SEPARATOR PIN FUNCTIONS

Pin	Mnemonic	Function
1	DIN*	**Disk Data In.** This is the data directly from the disk drive. It contains the combined clock and data information.
2	SCLK	**Separated Clock.** This is the clock which has been derived and separated from the disk-drive data stream.
3	CK	**Reference Clock.** This is the clock provided by the host system. Its frequency is either 4 or 8 MHz, depending on the density of the recorded data.
4	GND	**Ground.** This is the package ground connection.
5 6	CD0 CD1	**Clock Divisor.** These inputs determine the divisor that is applied to the Reference Clock on pin 3. The resulting clock is used internally and runs at a rate according to the following table: **CD0 CD1 Divisor** 0 0 1 0 1 2 1 0 4 1 1 8
7	DOUT*	**Disk Data Out.** This is the data from the data separator once the clock information has been removed.
8	VCC	**Power Supply** This is the +5-Volt power pin for the package.

Note: An asterisk (*) denotes that the referenced signal is active low.

Hardware Functional Description

Clock Divider

The Data Separator uses the Reference Clock provided on pin 3 to derive an internal operating clock. The Reference Clock can run at a frequency of either 4 or 8 MHz, depending on the disk drive size and data recording density. The two clock-divider inputs on pins 5 and 6 determine the final internal clock frequency. The various clock divider options are summarized in Table D-18.

TABLE D-18. DATA SEPARATOR CLOCK DIVIDER OPTIONS

CD1	CD0	DRIVE SIZE		DRIVE DENSITY		CK (MHz)	COMMENT
		8"	5 1/4"	Single	Double		
1	0		X	X		8	Any Combination
0	1		X	X		4	
0	0		X	X		2	
0	1		X		X	8	Any Combination
0	0		X		X	4	
0	1	X		X		8	Any Combination
0	0	X		X		4	
0	0	X			X	8	

The operating frequency of the Data Separator internal clock is normally 16 times the Separated Clock output frequency. As internal timing corrections take place to properly position the data with respect to the clock, the internal clock may vary from a minimum of 12 to a maximum of 22 times the Separated Clock frequency.

Edge Detector

The edge detector's function is to detect the leading edges of the combined data and clock data-stream pulses. The phase of the internal operating clock is then adjusted so that data and clock may be properly located with respect to each other. Short-term and long-term timing correctors provide proper timing relationships.

Data Separation

The data separator's main function is to provide an output that is the recreation of the original data that was sent to the disk drive.

Pulse Regeneration

Once data has been separated from the combined data and clock stream, the pulse regeneration circuitry provides the final separated clock and data outputs in the proper synchronized time relationship. The trailing edge of DOUT* is always two internal clock cycles ahead of the SCLK trailing edge. See Figure D-70.

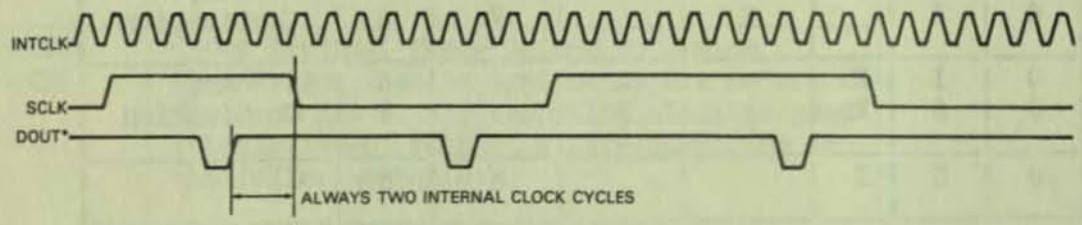


FIGURE D-70. DATA SEPARATOR CHIP TIMING OUTPUTS

Maximum Ratings

Listed below are the maximum ratings of the Data Separator chip. If these ratings are exceeded, permanent damage to the device may result. Also, exposure to the maximum ratings for extended periods may affect the reliability of the device.

Operating Temperature	0 to 70 Degrees C
Storage Temperature	-55 to 150 Degrees C
Lead Temperature (soldering, 10 sec)	325 Degrees C
Positive Voltage on Any Pin	8.0 V
Negative Voltage on Any Pin	-0.3 V

Electrical Characteristics

Listed below are the D.C. and A.C. electrical characteristics of the Data Separator. These characteristics apply, unless otherwise noted, at an ambient temperature of 70 Degrees C and at a power supply voltage of +5V ±5%.

Refer to Figure 4 for more information regarding the timing parameters mentioned below.

TABLE D-19. DATA SEPARATOR D.C. AND A.C. ELECTRICAL CHARACTERISTICS

Parameter	Minimum	Typical	Maximum	Units	Comments
Input Voltage					
Low Level Vil			0.8	V	
High Level Vih	2.0			V	
Output Voltage					
Low Level Vol			0.4	V	Iol=1.6 ma
High Level Voh	2.4			V	Ioh=-100 uA
Input Current					
Leakage Iil			10	uA	0≤Vin≤Vdd
Input Capacitance					
All Inputs			10	pF	
Power Supply Current					
Idd			50	mA	
CK Frequency (Fcy)	0.2		4.3	Mhz	
CK High Time (Tckh)	50		2500	ns	
CK Low Time (Tckl)	50		2500	ns	
CK to DOUT* "On" Dly (Tsdon)		100		ns	
CK to DOUT* "Off" Dly (Tsdoff)		100		ns	
CK to SCLK Dly (Tspck)	100			ns	
DIN* Active Low Time (Tdll)	0.1		100	ns	
DIN* Active High Time (Tdlh)	0.2		100	ns	

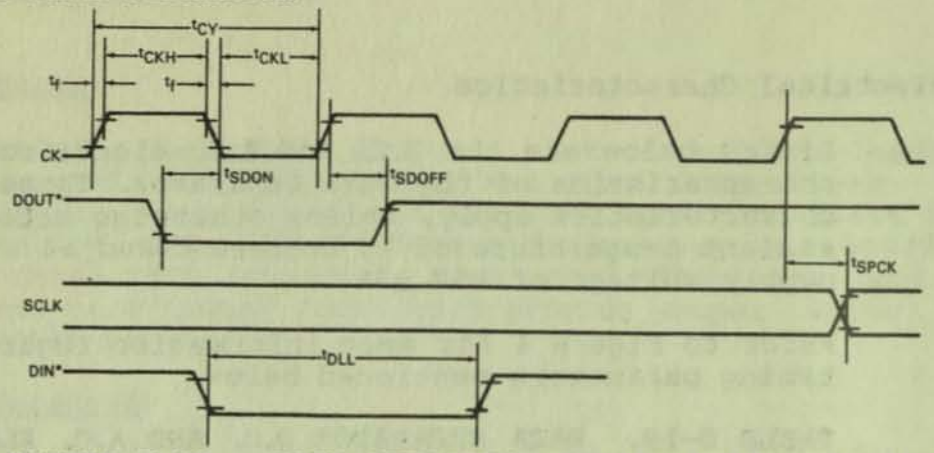


FIGURE D-71. DATA SEPARATOR TIMING RELATIONSHIPS

Software Information

The Data Separator contains no programmable registers.

Osborne Executive Applications Information

The Data Separator's use in the Osborne Executive is specifically oriented toward operation with a 5-1/4" single- or double-density disk drive. You will notice that the CD1 input is tied to ground and the CD0 input is a bit controlled by software.
Also, the CK input runs at a fixed frequency of 4 MHz. Given these conditions, it becomes apparent after referring to Table D-18 that the Data Separator is configured for operation in the above mentioned modes.

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