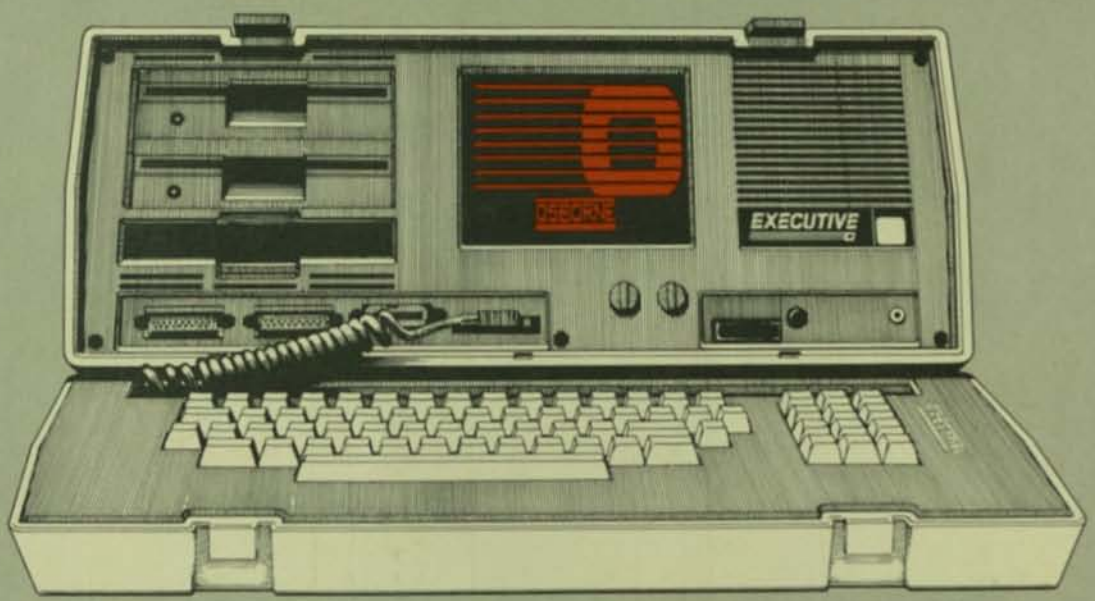
EXECUTIVE™

OSBORNE

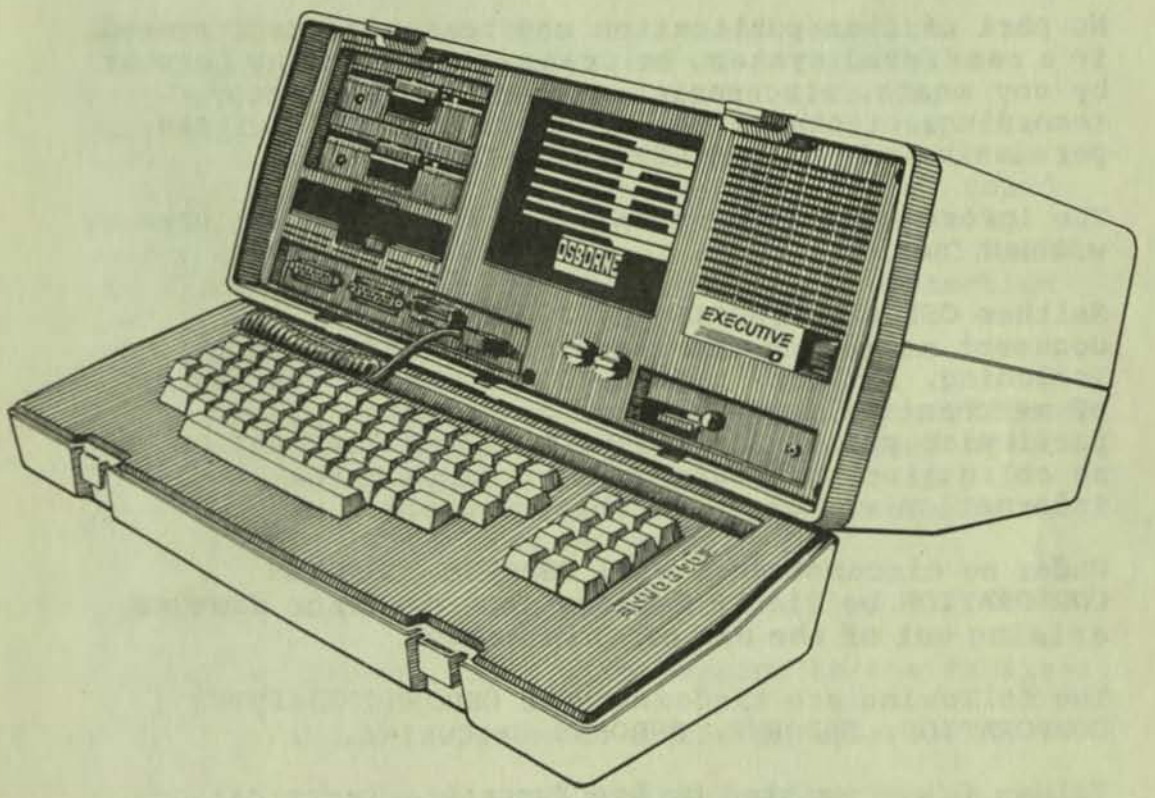
Technical Manual



Volume C: Hardware Design and Theory of Operation

OSBORNE
COMPUTER CORPORATION

OSBORNE EXECUTIVE TECHNICAL MANUAL
VOLUME C: HARDWARE DESIGN AND THEORY OF OPERATION



ABSTRACT

This manual describes the hardware architecture and circuit operation for each of the five assemblies contained within the Osborne Executive. Discussions proceed from a general functional block level to detailed chip-level explanations. Timing diagrams for important circuit operations are included. Schematics for the assemblies are also included at the back of the manual.

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SUPPLEMENTARY SECTION

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Main Logic Board Schematics (Sheets 1 through 15)
Dynamic RAM Board Schematics
Disk Drive Electronics Board Schematics
Power Supply Board Schematics
Video Monitor Board Schematics

DESIGN CONSIDERATIONS

While creating the Executive, Osborne's design engineers kept one objective in mind: to hold the hardware costs low while still producing a reliable, highly-adaptable microcomputer. This section summarizes the principles behind the design of the Executive, and compares the features of the Executive with those of the Osborne 1.

Exterior Changes

Most of the design changes are visible externally. The two half-height 5-1/4 inch diskette drives are set to the left side of the computer's face to provide more room for the video monitor. The Executive's monitor measures seven inches diagonally as compared to five inches for the Osborne 1. An amber display replaces the earlier black-and-white or black-and-green display.

The power switch has been moved to the front of the computer, and the battery connector utilized by the Osborne 1 has been eliminated in favor of providing battery-generated power directly through the power cord socket. An EIA RS-170 composite video-output connector (RCA type) has been added to simplify interfacing with monitors.

The earlier IEEE 488 edge connector has been replaced by a more universal IEEE 488 connector. The keyboard connector has been modified to provide power and a bidirectional strobe allowing other model keyboards to be adapted to the Executive.

A recessed fan installed at the back of the computer prevents internal heat build-up and thus ensures longer component lifespans.

Interior Changes

Internally, the Executive differs significantly from the Osborne 1; the schematics illustrate the differences. Dynamic RAM forms the Executive's main memory banks, two blocks of 64K bytes accessed by bank enable circuitry and 16 address lines. The Z80A microprocessor automatically refreshes the dynamic RAM; no additional hardware is required for refresh operations. Additionally, the Executive is capable of memory expansion; five bank-enable lines from the 6821 PIA remain unused. If further decoding was employed, as many as 64 additional banks of memory could be accessed

Two ROM sockets are resident on the main logic board as opposed to one ROM socket on the Osborne 1. A series of jumpers directs the addressing at the ROM sockets allowing higher-capacity ROM IC's to be substituted. These jumpers also permit a 6116 RAM chip to be inserted in the ROM socket with the higher address.

The system of memory mapping used by the Osborne 1 to communicate with internal devices and external I/O ports has been replaced by a system of I/O mapping in the Executive. This allows access to all devices external to the CPU chip without the necessity of bank switching.

A separate Video RAM within the Executive frees the entire main memory bank for program use. The Osborne 1 was limited by having to reserve the highest 4K bytes of memory space to act as the Video RAM.

The Video display extends to a full 80-column width over the previous 52-column width for the Osborne 1.

An 8 x 10 dot matrix is the display format for the 256 characters stored in the FONT RAM. Unlike the Osborne 1 which used a fixed character ROM, the Executive's FONT RAM can be downloaded with any combination of graphic symbols or character sets desired. To further increase the flexibility inherent in this video system, direct memory access (DMA) to the video memory permits an external device to load the Video RAM with any conceivable pattern (depending on the nature of the characters within the FONT RAM). An external device using DMA can utilize the surplus memory locations in the video memory as scratchpad or utility space. This DMA port also gives the Executive the capability of interfacing with a hard disk drive or other external device.

Additional storage space is provided in the Video RAM for attribute bits designating an alternate character set (from the FONT RAM), underline, blinking, or reverse video. These bits are transferred during block move operations within video memory in correspondence with the character bits that they modify.

The frequency of the alarm signal provided to alert the user can be altered by software to produce different tones.

In order to keep costs reasonable, small-scale logic was used to implement the video display circuits instead of using one of the specialized IC's currently available.

The Executive includes increased capabilities for interfacing with peripheral devices. With the addition of the Z80A SIO/2, two serial RS-232-C channels can now be serviced. The modem port can handle synchronous RS-232-C communication; however, the printer port still operates only in asynchronous mode. The potential baud rate on these channels has been expanded: the asynchronous limit now stands at 38.4 Kilobaud. A programmable counter-timer circuit clocks the serial channels providing a greater range of baud rates than had previously been possible. The transmit and receive clocks for the synchronous channel can now be either internal or external.

The OCC1 allowed optional use of double-density diskettes; double-density formatting is standard on the Executive. The Executive's disk-interface connector corresponds with the ANSI standard. Unlike the OCC1, the Executive routes the disk-drive power lines separately from the data and control signals. By adopting this standard, the Executive is capable of interfacing any disk drive meeting the ANSI conventions.

A spindle clock is provided on the disk drive connector which, if utilized, could control the rotation speed of the disk drive spindle under software control. This simplifies the necessary disk-drive electronics and allows nonstandard drive speeds to be used.

The interface with the keyboard differs slightly from the OCC1. The high-order address lines from the Z80A are now utilized to interrogate the keyboard matrix rather than the low-order lines. The nature of the Z80A instruction set allows certain useful software manipulations by handling keyboard scanning this way.

MAIN LOGIC BOARD: FUNCTIONAL DESCRIPTION
Functional Block Diagram

The functional block diagram illustrates the interrelationships of the major components of the Executive. Although each of these areas is covered in greater detail further into the manual, the brief description given here should be a useful orientation to the architecture of the computer.

Z80A Microprocessor

The Z80A CPU, illustrated on Sheet 2 of the schematics, maintains control over most logic board functions through the timed manipulation of the address, data, and control lines. Since all operations on the board originate through the Z80 execution of instructions stored in the Program ROM or downloaded into the system RAM, the Z80A can be thought of as the key component in the system.

Basic Architecture

The Z80A contains four 16-bit registers and eighteen 8-bit registers which are utilized to carry out the 158 different instructions that the Z80A can recognize and execute. Two sets of six registers can either be used individually or can be combined to form 16-bit registers.

An instruction register receives each instruction as it is fetched from memory. These instructions are decoded and the Z80A generates all necessary control signals to:

- Write to the registers or read from them
- Execute control over the components on the main logic board
- Perform necessary calculations in the internal Arithmetic Logic Unit.

The Z80A communicates with the rest of the components on the main logic board through 8 bidirectional data lines, 16 unidirectional address lines, and a number of control inputs and outputs. Not all of these control signals are utilized in the Executive's design. Note on the schematic that HALT*, BUSAK*, BUSRQ*, and NMI* are not functional in this application.

To obtain more information about the Architecture, Pin Descriptions, and CPU Timing for the Z80A, consult Volume D of this Technical Manual.

CPU Clock

The Z80A CPU is driven by a 3.9936 MHz clock signal derived from the output of a crystal oscillator. This value results in a Z80A T-state period of 250 nanoseconds. Since the typical Z80A instruction execution requires between 4 and 20 T-states, execution times will range from 1.0 microsecond to 5.0 microseconds.

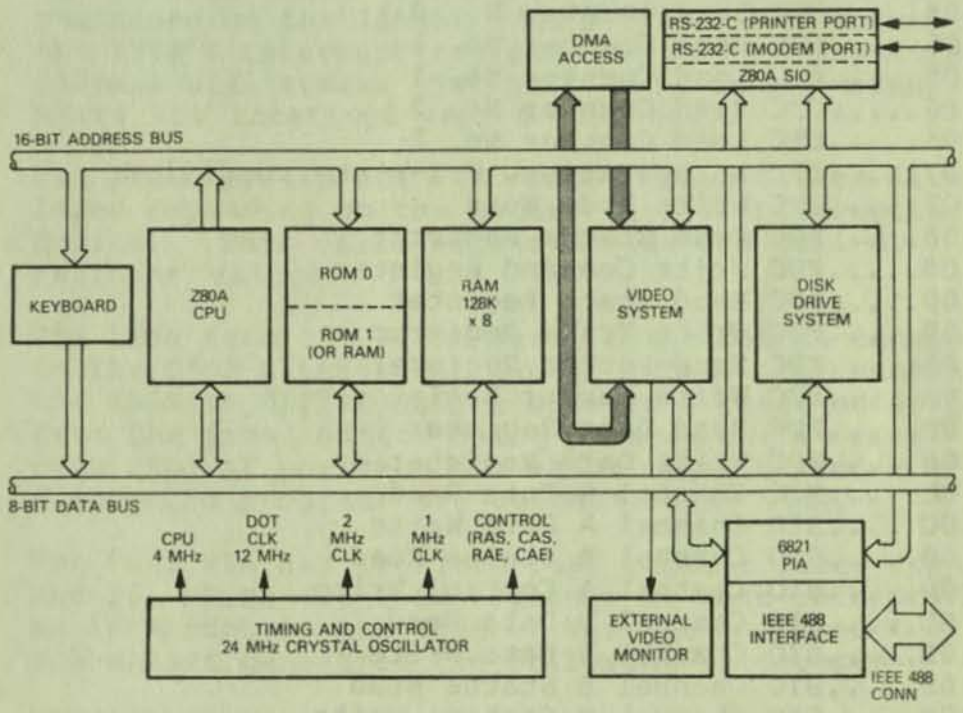


FIGURE C-1. EXECUTIVE 1 FUNCTIONAL BLOCK DIAGRAM

I/O Mapping

The technique of partial I/O mapping is employed to allow the Z80A to direct data to and from other components and external interfaces. Z80A IN and OUT instructions result in a Port Address being generated on the lower eight Z80 Address lines. These addresses are decoded by the 74LS138 chip (Sheet 4, zone A7) to produce chip select signals for the Real-Time Clock (RTC), the Keyboard, the IEEE 488 channels, the Z80A Serial Input Output (SIO/2), the Floppy Disk Controller (FDC), and the Counter-Timer Circuit (CTC). The I/O Port Addresses are:

I/O Port Addresses
(All port addresses are in hexadecimal notation.)

```
 IN 00.....System PIA Select; Channel A Data/Direction Read
OUT 00.....System PIA Select; Channel A Data/Direction Write
 IN 01.....System PIA Select; Channel A Control Read
OUT 01.....System PIA Select; Channel A Control Write
 IN 02.....System PIA Select; Channel B Data/Direction Read
OUT 02.....System PIA Select; Channel B Data/Direction Write
 IN 03.....System PIA Select; Channel B Control Read
OUT 03.....System PIA Select; Channel B Control Write
 IN 04.....CTC Read Counter No. 0
OUT 04.....CTC Load Counter No. 0
 IN 05.....CTC Read Counter No. 1
OUT 05.....CTC Load Counter No. 1
 IN 06.....CTC Read Counter No. 2
OUT 06.....CTC Load Counter No. 2
 IN 07.....CTC No operation, Tri-state condition
OUT 07.....CTC Write Mode Word
 IN 08.....FDC Read Status Register
OUT 08.....FDC Write Command Register
 IN 09.....FDC Read Track Register
OUT 09.....FDC Write Track Register
 IN 0A.....FDC Read Sector Register
OUT 0A.....FDC Write Sector Register
 IN 0B.....FDC Read Data Register
OUT 0B.....FDC Write Data Register
 IN 0C.....SIO Channel A Data Read
OUT 0C.....SIO Channel A Data Write
 IN 0D.....SIO Channel A Status Read
OUT 0D.....SIO Channel A Control Write
 IN 0E.....SIO Channel B Data Read
OUT 0E.....SIO Channel B Data Write
 IN 0F.....SIO Channel B Status Read
OUT 0F.....SIO Channel B Control Write
 IN 10.....IEEE 488 Channel A Data/Direction Read
OUT 10.....IEEE 488 Channel A Data/Direction Write
 IN 11.....IEEE 488 Channel A Control Read
OUT 11.....IEEE 488 Channel A Control Write
 IN 12.....IEEE 488 Channel B Data/Direction Read
OUT 12.....IEEE 488 Channel B Data/Direction Write
 IN 13.....IEEE 488 Channel B Control Read
OUT 13.....IEEE 488 Channel B Control Write
 IN 14 through
 IN 17.....Keyboard Read
 IN 18 through
 IN 1B.....Real-Time Clock Read
OUT 1C through
OUT 1F.....Video Display Enable
```

Interrupts

The Z80A is initialized to use Mode 2 Interrupt servicing. The Z80A handles a Mode 2 Interrupt by creating an interrupt vector based on 8 bits from the data bus (either hard-wired or supplied by the interrupting device) and 8 bits stored in the Z80's Interrupt Register.

If the interrupt is generated by one of the PIA's or the RESET push button, the Z80A will read a hex FE on the data lines (from the values of 7 pull-up resistors on the lines). This value is combined with the Z80A's interrupt register value. The resulting address will access that portion of Bank 0 memory where the interrupt vector is stored.

The SIO supplies its own vector value to the data lines depending on the nature of the interrupting device. This value will override the pull-up resistor values.

The line from the Front Panel reset button connects to the Z80A's interrupt input. This line enables the Z80A to differentiate between a reset occurring from the panel button being pressed and a reset occurring at power-up (in which case, a number of diagnostic programs are automatically run).

The 6821 PIA has two interrupt request lines (pins 37 and 38) which are tied together so that both provide an interrupt to the Z80A. The PIA on Sheet 4 of the schematics generates the following interrupts:

VERTICAL BLANK: Allows the Z80A to keep track of real time and to detect the start of the vertical blanking interval.

KEYBOARD STROBE: Not currently utilized.

DMA INTERRUPT REQUEST: This signal is routed from the DMA connector and lets an external device interrupt the Z80A. The line is bidirectional and may also be used to route an interrupt to an external device.

The 6821 PIA on Sheet 14 uses the Service Request line from the IEEE 488 connector (pin 10) to interrupt the Z80A. The Floppy Disk Controller has a line physically connected to this PIA for interrupting the Z80A, but the BIOS and ROM firmware uses a polling approach to read the FDC's status rather than responding to direct interrupts.

The Serial Input Output seen on Sheet 12 is fully programmable for handling interrupt generation. The vector supplied to the Z80A by the SIO at the time of Interrupt Acknowledge will reflect the condition of the SIO.

Reset Sequencer

The Reset Sequencer is activated at Power-On or whenever the reset button on the computer's front panel is depressed. The three 74LS74 flip-flops serve to control the pulse width so that the reset signal is long enough to meet the minimum requirements for all components utilizing this signal, yet short enough to ensure that the refresh sequence of the Dynamic RAM is not impaired in any way.

Refresh

The Refresh of Dynamic RAM is carried out automatically by the Z80A during the T3 and T4 states of every instruction fetch cycle. The Refresh Address is calculated and incremented sequentially by the Z80A to refresh dynamic RAM a full row of the address matrix at a time. Column addresses are not used as part of the refresh cycle. Without periodic refreshing, the contents of the dynamic RAM would gradually be lost.

Timing and Control Signals

Sheet 2 of the schematics illustrates the generation of the clock and control signals; these signals regulate the interaction of all logic board operations.

The System Clocks originate from the crystal oscillator X1 at zone D7. Three 74S175 flip-flops divide the 23.9616 MHz output by six. The output is then buffered and becomes the clock signal to the Z80A microprocessor. The same signal also clocks the Z80A SIO/2.

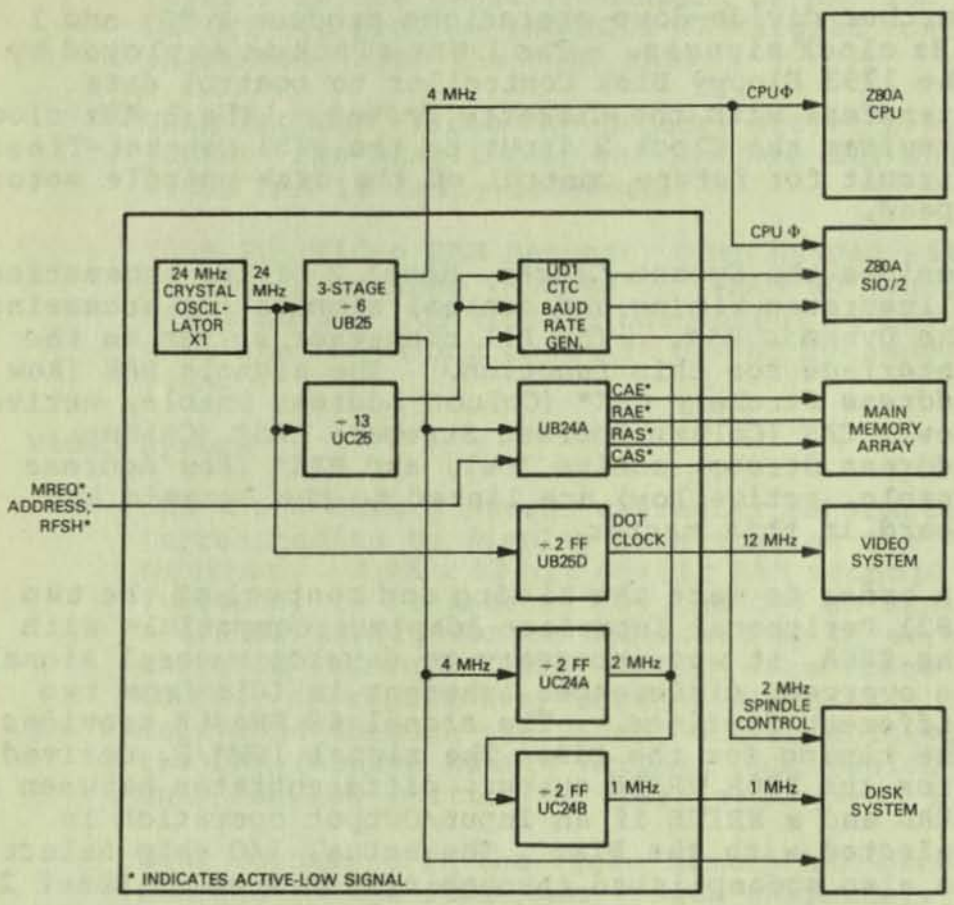


FIGURE C-2. BASIC TIMING SIGNALS

The timing diagram for the System Clocks shows the additional derivative signals output by this timing network. The active-low signal Phi* is negative-NANDed to generate the WRITE strobe to the FONT RAM. Phi* also provides clocking to the Read Data Separator and the Write Precompensator of the Disk Drive System.

The signal 24 MHz (actual value: 23.9616 MHz) clocks a synchronous four-bit counter set up to divide by 13; the resulting 1.8432 MHz signal drives the clock inputs to the 8253 Counter-Timer Circuit which in turn provides Transmit and Receive clocks for the SIO. A divide-by-two of the 24 MHz signal generates the Dot Clock, a 12 MHz signal that controls the rate

of the bit stream sent to the video monitor. Additionally, the dot clock is used to synchronize Video Memory access by a DMA device.

Further divide-down operations produce 2 MHz and 1 MHz clock signals. The 1 MHz clock is employed by the 1793 Floppy Disk Controller to control data transfers with the diskette drives. The 2 MHz clock provides the Clock 2 input to the 8253 Counter-Timer Circuit for future control of the disk-spindle motor speed.

Besides the System Clocks, Sheet 2 of the schematics illustrates timing and control signals for accessing the Dynamic RAM. The P11 connector serves as the interface for this function. The signals RAS (Row Address Strobe); CAE* (Column Address Enable, active low); CAS (Column Address Strobe); CAS* (Column Address Strobe, active low), and RAE* (Row Address Enable, active low) are linked to the Dynamic RAM board in this manner.

In order to make the timing and control of the two 6821 Peripheral Interface Adapters compatible with the Z80A, it was necessary to develop several signals to overcome differences inherent in IC's from two different families. The signal 68 ENABLE provides the timing for the PIA. The signal IOW*/R, derived from the Z80A WRITE output, differentiates between a READ and a WRITE if an Input/Output operation is selected with the PIA. The actual I/O chip select is also accomplished through timing seen on Sheet 2; the Z80A's IORQ* (Input/Output Request) is negative-ANDed with the WR (Write) or RD (Read) lines. The clock Phi and a 74LS74 flip-flop control the pulse width of IOCS*; this chip select is then decoded with selection of the appropriate PIA (Ports 00 through 03 for the System PIA; Ports 10 through 13 for the IEEE 488 Interface PIA).

The IOWAIT* to the Z80A inserts additional WAIT states to accommodate the Z80A to slower I/O devices.

DISK WE* (Disk Write Enable) and DISK RE* (Disk Read Enable) provide Read and Write strobes to the 8253 CTC and to the 1793 FDC to initiate Read and Write operations.

Bank Enable lines 7 and 8 and Z80A lines MREQ*, RFSH*, ADR13, ADR14, and ADR15 are decoded through a series of random logic gates to produce ROM DECODE*, VRAM RQ, and VRAM DECODE* signals.

ROM DECODE* provides the chip enables for the ROM 0 and ROM 1 IC's on any READ operation of the ROM addresses. A Z80A WRITE to the same memory address results in the negative-NANDing of WR* and ROM DECODE* to produce the FONT WR* signal (used to write characters into the FONT RAM).

VRAM DECODE* (Video RAM Decode, active low) acts to inhibit the enabling of the Dynamic RAM whenever the Video RAM is being accessed.

VRAM RQ (Video RAM Request) when NANDed with the Z80A RD signal creates VRAM RD*. VRAM RD* enables Tri-State Buffer UC9 to gate the output of the Video RAM onto the TDATA bus where it can be accessed by the Z80A.

Video System

The Video Memory stores character information corresponding to display locations on the video monitor. A 4K x 12 bit static RAM accomplishes this function; it is accessed by the CPU as Bank 7. This block of memory can be addressed by three sources: the Z80A (through ADR0 - ADR11), the Video Address Counter (a repetitive, sequential address count delivered through the Video Address Multiplexer), or the DMA (Direct Memory Access) port (which can access only the low portion of video memory--4K x 8 bits).

Data contained in the Video Memory RAM becomes the address to the FONT RAM. Each character, whether in ASCII format or a graphic representation, is encoded with a unique address which accesses an 8 x 10 bit pattern in the FONT RAM. The Video Address Counter and the Video Timing Network work together, accessing one scan line at a time, character-by-character, to shift the bit patterns through a shift register to the video monitor.

The actual address to the FONT RAM comes from the low Video Memory RAM and is 8 bits wide. The high Video Memory RAM has a capacity of 4K x 8 bits, but only 4K x 4 bits of the actual space is useable. The 4 attribute bits in the high Video Memory RAM serve to modify the character information in the low Video Memory RAM, interacting with the bit patterns as they are moved through the shift register for output to produce dim intensity, blinking, and underline. One attribute bit provides access to the alternate character set in the FONT RAM. An additional attribute bit, reverse video, is stored as the most significant bit of the low Video Memory RAM.

Low Video Memory RAM comprises addresses hex C000 through CFFF. High Video Memory RAM starts at hex D000 through DFFF. Data is loaded into the high RAM by the 4 high-order bits on the CPU data bus.

The areas of the Video RAM that are not part of the actual display (several locations at the end of each text row and a 1K area at the end of the Video RAM) are available as a scratchpad RAM for the Z80A and are accessible through the DMA port.

FONT RAM is also a static RAM and may be downloaded with any set of 256 eight-by-ten bit patterns. The alternate character-set bit switches between one of two 128 character blocks; in typical usage one block contains the full ASCII character set. The other block may be graphic symbols, characters necessary for other languages, or whatever the software requires. The actual memory size of the FONT RAM is 4K x 8 bits.

The timing for the Video Memory RAM consists of:

- o A 12MHz dot clock to control the rate of the shift register to the video monitor,
- o A character clock to periodically access the correct character locations in Video RAM,
- o Horizontal and vertical sync and blanking signals to direct the video trace on the monitor,
- o A scan counter to supply to the FONT RAM a value corresponding to the scan line (or "slice") of the character being accessed,
- o The addresses automatically supplied by the video address counter.

Read-Only Memory

The Read-Only Memory for the main logic board in the most common configuration for the Executive comprises a 2764 ROM (8K x 8 bits) in the ROM 0 socket, and a 6116 static RAM (2K x 8 bits) in the ROM 1 socket. A number of jumpers allow the substitution of other memory IC's in these sockets.

In the ROM 0 position (socket UD18) a 2732, 2764, or a 27128 ROM can be used if the jumpers are positioned correctly. The ROM 1 position (socket (UD15) can hold a 2732, 2764, 27128, or a 6116 RAM memory chip.

The following jumper placement reflects the normal configuration (2764 in ROM 0 position; 6116 in ROM 1) for the main logic board:

J1: Pins 1 and 2 jumpered
J2: Pins 3 and 4 jumpered
J3: Pins 1 and 2 jumpered
J4: Pins 2 and 3 jumpered
J5: Pins 1 and 2 jumpered
J8: Unjumpered

Bank 8 covers the address range between hex 0000 and 3FFF, effectively 16K bytes of memory with the top 6K bytes unused in the present configuration. During a Z80A READ operation of this memory space, the incoming ROM DECODE* line provides the chip enable for both the 2764 and the 6116 memory chips. The Z80A is able to write to the 6116 through the decoding of the WR* line routed through the jumper J4 to the Write Enable input.

The FONT RAM shares the same address space as the ROM but is limited to responding to WRITE operations from the Z80A only. The signals FONT WR* and FONT EN* are produced through decoding to allow the Z80A to load any conceivable character set into the FONT RAM.

The ROM contains the initialization routine to start the computer system at power-up. Various driver routines, diagnostic code, and utility programs are also contained within the ROM.

Dynamic RAM

The 128K-byte dynamic RAM resides on a separate PC board and consists of sixteen 64K x 1-bit memory chips grouped to form two 64K x 8-bit arrays. These chips form two memory banks, BANK 0 and BANK 1, which are simultaneously refreshed by the Z80A's automatic refresh cycle.

Each 64K by 8-bit array has eight address inputs. Since sixteen values are necessary to differentiate 64 K unique address locations, the Z80A outputs 16 address bits which are latched. Refresh circuitry then strobes first an 8-bit row address followed by an 8-bit column address. The signals RAE* and CAE* (Row Address Enable and Column Address Enable) serve to enable the buffers driving the Dynamic RAM address inputs selecting between the low and the high Z80A address lines. The timing network seen on Sheet 2 of the schematics generates the strobe signals for the BANK 0 RAM (RAS0* and CAS0*) and the BANK 1 RAM (RAS1* and CAS1*).

BANK 0 represents the default bank, accessed if no other bank is specified by the System PIA. It contains system routines including BIOS, some of BDOS, buffers for the diskette drives, interrupt routines, and CP/M Plus. This bank is not available for user programs during normal CP/M operation.

Bank 1 during CP/M Plus usage contains CP/M code in some addresses, but approximately 58K bytes are available for user programs.

The Executive has five additional bank-enable lines available through the 6821 PIA (seen on Sheet 4 of the schematics) to accommodate future memory expansion.

Disk Drive System

The main logic board contains part of the electronics necessary to operate the diskette drives. A 1793 Floppy Disk Controller (FDC) resides on the board acting as the primary interface between the Z80A and the disk-drive electronics board, a separate board which handles the physical interface and signal translation for the drive mechanisms.

Parallel data is supplied to the FDC along with a clock and appropriate enables; a serial bit stream is outputted to the disk-drive electronics board to be written upon the diskette with respect to the INDEX pulse and track positions. Incoming serial data from the drive head is routed through a 9216 Data Separator IC. The clock signal is extracted from the data by this circuit, and the FDC uses the clock to convert the serial data to a parallel format.

Although the FDC has an Interrupt Request output, this feature is not utilized to notify the Z80A of disk drive data transfers. Polling of the FDC accomplishes this function in the present revision of the Executive. A status register within the FDC can be read by the Z80A by performing an IN 08 instruction.

Based on Z80A instructions, the FDC issues signals to control the direction and distance of head travel (thereby accessing specific tracks on the diskette). A system of write precompensation is employed by the 74LS166 IC to ensure that data written to the diskette occurs in the correct position (depending on their track locations and other factors, bits written to the diskettes tend to shift positions; timing alterations are made to adjust the write data).

The values on ADR0 and ADR1 determine the nature of Z80A communication with the FDC. The status register, track and sector registers, and read and write data registers can be examined or loaded by this means.

The P8 connector interfaces the disk-drive electronics board. Besides the inputs and outputs mentioned, P8 routes the signal SPINDLE* to the drive electronics, permitting software control of the diskette drives' spindle speed (this feature is not currently implemented). The signals DRV SEL1* and DRV SEL2* engage either the A or B disk drives. MOTOR ON* supplies a signal to start the selected drive spinning (although this signal is not currently used).

Keyboard

The Executive's detachable keyboard contains no active electronics. A switch matrix is interrogated through the Z80A's eight high-order address lines; any key closures are detected on the incoming Z80A data lines. A software routine implements three-key rollover to process rapid, sequential key closures.

A tri-state buffer is incorporated to isolate the keyboard from the data lines. This buffer is accessed whenever the Z80A performs an IN 14 through IN 17 instruction.

The keyboard connector has a power output line and bidirectional strobe making it possible to attach keyboards containing electronics.

CONVENTIONS AND ORIENTATION

Introduction

For those desiring a gate-by-gate circuit analysis of the PC boards within the Osborne Executive, the following sections cover the theory of operation using the schematics as a focus for the discussion. Each of the five boards included in the Executive is covered: the main logic board, the memory board, the disk-drive electronics board, the power supply board, and the monitor board.

Rapid advancements in electronic design practices necessitate frequent product improvements. To guarantee that the documentation matches the product design changes, supplements will periodically be made available offering updated schematics. A description of the design changes, circuit analysis of the new areas of the schematics, and a summarized product history will be provided in these updates.

Because the schematics originate from more than one vendor source, there are a number of different conventions utilized for expressing the logic organization and circuit architecture. These conventions are summarized below.

Active-Low Symbols

The acronyms used to signify signal names within the circuits generally include a symbol to specify those signals that are considered active (or "true") when in a low-voltage state (close to 0 volts in TTL terms).

An asterisk (*) following a signal name (such as IOWAIT* or CAS*) indicates an active-low signal. The virgule, sometimes referred to as a diagonal or slash mark, appears at the end of signal names in some instances. The signals DSELB/ and WRDP/ are two examples.

Other possibilities that may be encountered are a bar appearing over the signal name or a '-N' appearing after the signal name. The bar denotes an active-low signal as does the '-N'. A '-P' represents an active-high signal.

Integrated Circuit Locations

On schematics originating from Osborne, each IC number is prefaced with the letter designation "U". REV A or earlier initial-production Main Logic Boards use a zone coordinate system linking each socket on the PC board to a zone having both an alphabetic and a numerical coordinate. Thus the IC UC24 would be found at the intersection of the "C" row and the "24" column on the PC board. Note that the edges of the board have these zone designations expressed in solder.

In the Theory of Operation discussion, whenever IC's are mentioned by board location, the "U" number will be referenced. For example, the IC UB25 pin 6 output is fed back to the Data input.

However, if an IC is referenced to its location on the schematics, the text will refer to the system of zone coordinates used on the schematics. Therefore, IC UB25 at location A1 would indicate that the reader should look at the coordinate location A1 on the schematics to see the diagram of the IC UB25.

Signal Extensions

An expression precedes or follows each signal name as it enters the schematic drawing on the left-hand side of the page, or exits the schematic on the right-hand side of the page. This expression, or expressions if there are more than one, refers to the page number(s) and zone coordinates where the signal either originated or is being directed to. Some signals occur on several different sheets of the schematics and these signal extensions can also be followed by referencing these numerical values.

Multiple IC References

Because a number of logic circuits may be packaged in the same IC, it is not unusual to find on the schematics a gate or a flip-flop having a "U" number the same as another. Where this occurs you will notice that although the "U" number is the same, the pin numbers for these IC's will differ. The "U" number simply refers to an IC in a particular socket location; this IC may have several different gates or flip-flops within it which may be differentiated by their unique pin numbers.

MAIN LOGIC BOARD: SHEET 1 OF THE SCHEMATICS

The material contained on the first sheet of the schematics covers several areas of the PC board design, expressing standards that are followed on subsequent sheets.

The upper left-hand portion of the page enumerates the logic gates remaining on the PC board that are not used by the current design. These gates are available for design modifications without incurring the need for inserting additional IC's upon the board.

The power supply board interfaces with the Executive main logic board through the P7 connector shown at the left side of the sheet. Through the filtering network of capacitors shown, the main logic board receives the DC power necessary to operate all on-board components: +12 V, -12 V, and +5 V.

The connection at P6 links the chassis ground traces of the PC board to the common chassis-ground tie point to ensure that no differential voltages exist.

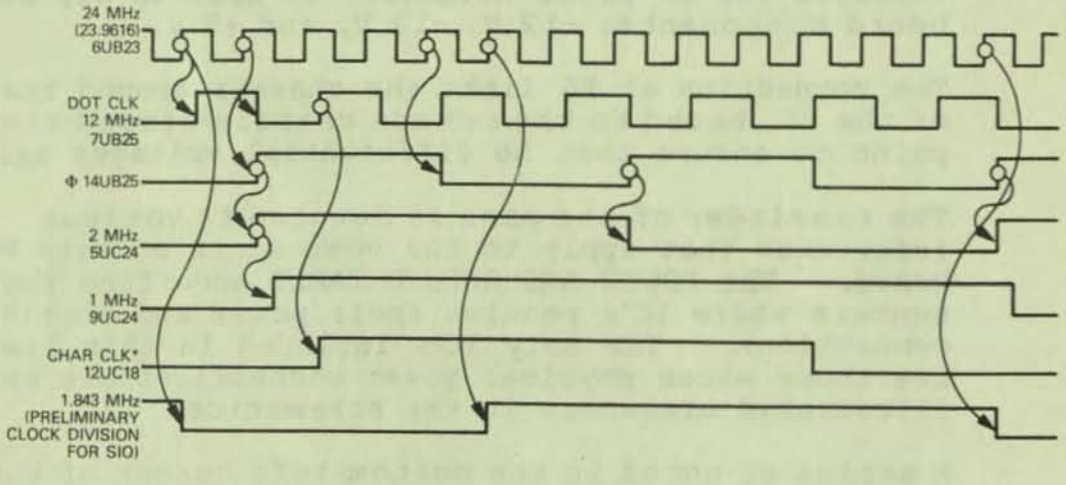
The remainder of the page is devoted to various references that apply to the components on this PC board. The POWER AND GROUND TABLE specifies the pin numbers where IC's receive their power and ground connections. The only IC's included in this list are those whose physical power connections are not illustrated elsewhere in the schematics.

A series of notes in the bottom left corner of the sheet specifies a number of universal conditions that apply to hardware components upon the board.

MAIN LOGIC BOARD: SHEET 2 OF THE SCHEMATICS

Sheet 2 illustrates generation of the clock signals for the Executive system, and the creation of the memory and I/O timing signals that control access during READ and WRITE operations to the I/O Ports, the Video RAM, the Dynamic RAM, and the Monitor ROM.

All system clock signals originate from one source, the 23.9616 MHz crystal oscillator X1 located at D7 on the schematic. The timing diagram illustrates the relationships between the clock signals that are generated by the various divide-down networks. The block diagram (on page C-9) shows the destinations for these clock signals, as well as the arrangement of the divide-down networks used to arrive at the final values.



* DOT CLK COULD BE INVERTED FROM THIS WITH RESPECT TO SLOWER CLOCKS DEPENDING ON THE CONDITIONS AT POWER UP.

FIGURE C-3. SYSTEM CLOCKS

The three 74S175 edge-triggered, D-type flip-flops form a three-stage divide-by-six network. The output of the crystal oscillator, labeled 24 MHz for convenience, clocks each of the flip-flops simultaneously.

The Master Reset to Pin 1 of each of the flip-flops only functions if at power-up the three flip-flops happen to initialize with the pin 10 output high, the pin 3 output high, and the pin 15 output high. In such a case, these signals ANDed at UB22 would cause the Master Reset. If not for this feature, the time network could be locked into a mode dividing by two instead of by six.

The output of the timing network, a clock signal of approximately 4 MHz, forms Phi*, a timing input for the FONT WRITE function and for the READ DATA SEPARATOR.

The timing network output is also inverted, shaped and clamped by the resistor/diode circuit at D4, and then used to provide the basic clock input for the Z80A microprocessor.

The Dot Clock is generated by a simple divide-by-two of the 24 MHz signal by the flip-flop at location D2.

Note also that the portion of the 24 MHz signal that bypasses the divide-down network is used, undivided, to clock the Synchronous Counter seen on Sheet 12.

The bottom half of Sheet 2 illustrates the development of various memory and input/output timing signals used on the main logic board.

ROM DECODE*, used to enable both IC's installed in the ROM0 and ROM1 sockets, requires that PRI8 (a bank enable signal) be active and ADR15 (the most-significant address line) be inactive; these signals are negative-NANDed at UE6, pins 11 and 12, with the output providing the signal to satisfy one input, pin 12, of UE5. To produce ROM DECODE*, RFSH* and ADR14 should also be inactive and the jumper J3 should be in place (necessary if the standard 2764 ROM is in the ROM0 position). ROM DECODE* is used to access the Scratchpad RAM as well as the 2764 ROM.

Note that if a 2732 ROM is to be used, the jumper J8, shown at location C6, must be installed.

ROM DECODE* also serves another function; it provides the write enable input to the FONT RAM. Since the FONT RAM and the Monitor ROM occupy the same address space, the Z80A differentiates between the two using the RD* and WR* signals to prevent simultaneous access. The FONT RAM is "write-only" and, of course, the ROM is "read-only" which prevents any conflicts during access.

The connector P11 provides signals from the main logic board to the separate PC board containing the main memory (a 128K-byte RAM) to control chip enables and regulate the address timing to the RAM with RAS (Row Address Strobe) and CAS (Column Address Strobe).

Although the relationships are rather difficult to explain verbally, the two following timing diagrams depict the origins of the RAS and CAS signals during an M1/REFRESH cycle (used to fetch an instruction

from memory and to re-energize the individual addresses of the Dynamic RAM on a periodic basis) and during a normal READ or WRITE operation.

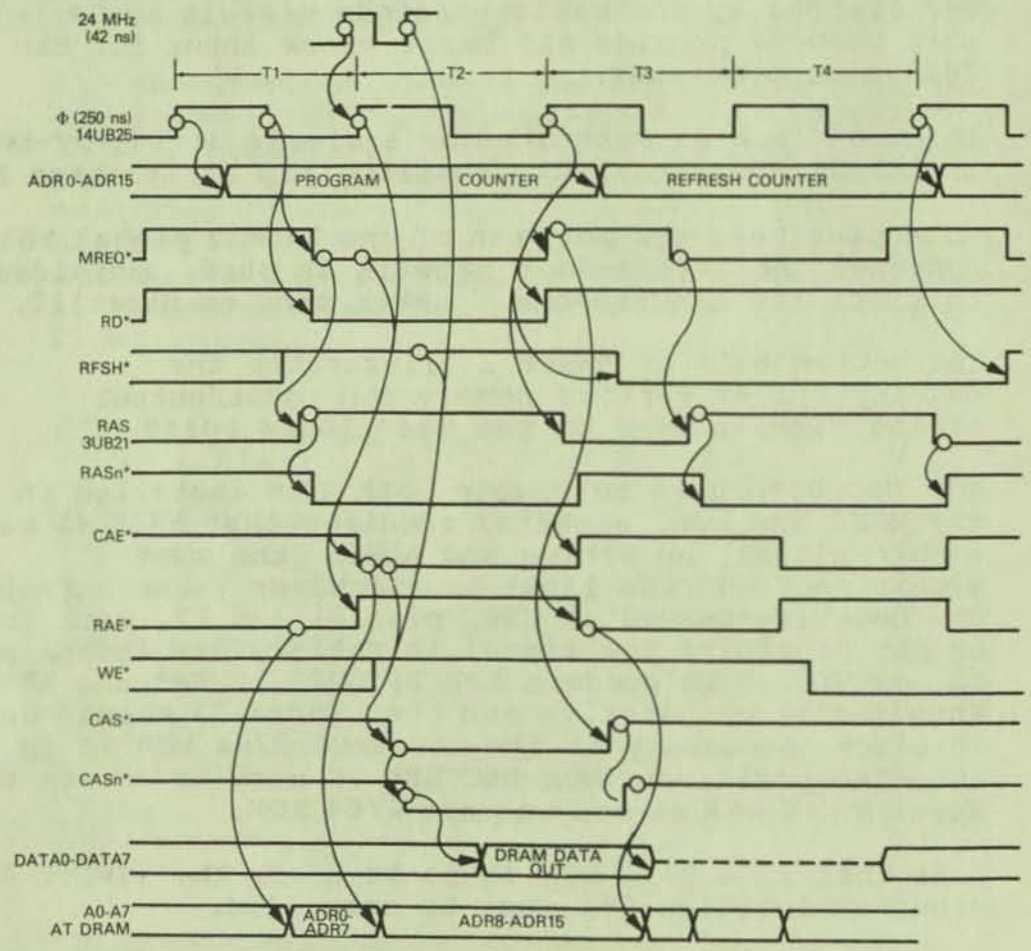


FIGURE C-4. DYNAMIC RAM (M1/RFSH) TIMING

The signal VRAM RQ (Video RAM Request) is an important constituent of the enable signals for reading and writing to the Video RAM. VRAM RQ is produced by the conjunction of the MREQ* (Memory Request) signal from the Z80A and the NANDed combination of the PRI7 Bank Enable signal, the Address lines ADR14 and ADR15, and the absence of ADR13 or RFSH*.

These same signals, minus the MREQ*, serve to activate the VRAM DECODE* line which is used on the main memory board to disable it during access to the video RAM.

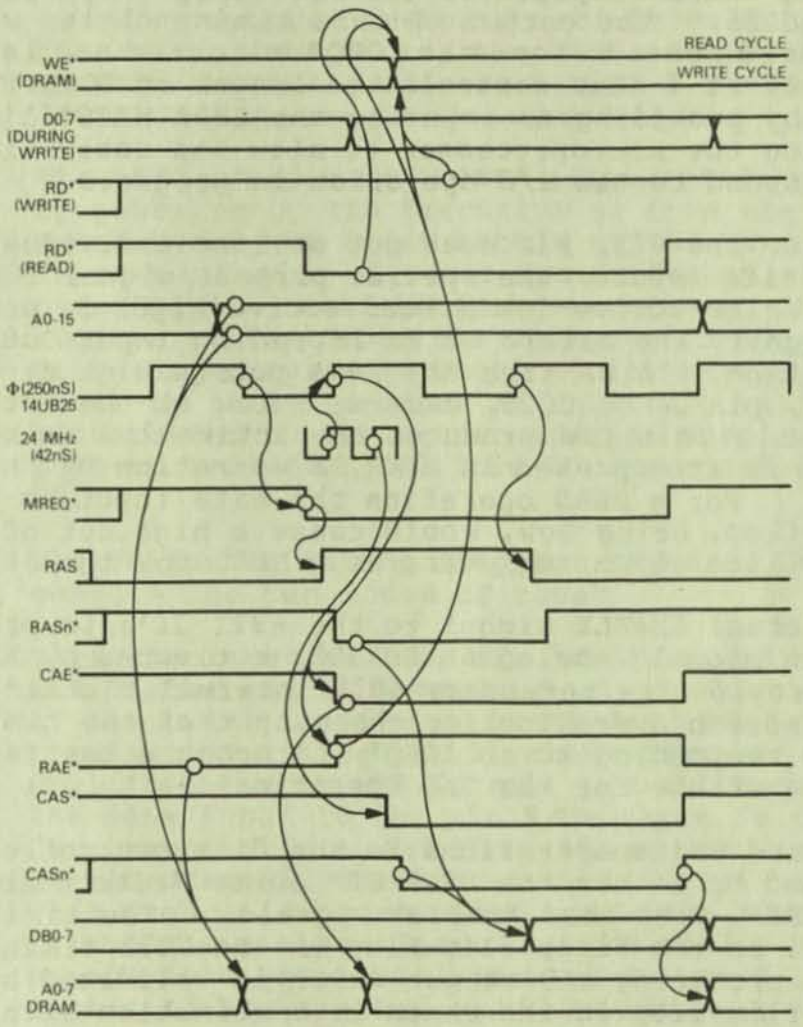


FIGURE C-5. DYNAMIC RAM (RD/WR) TIMING

The IOCS* (Input/Output Chip Select) enables the I/O Decoder (shown on Sheet 4) to determine by the contents of the Z80A Address bus which I/O device is to be accessed. The output of negative AND-gate UC21 pin 1 starts the IOCS* whenever IORQ* and a Z80A Write or Read are activated. The duration of the IOCS* is stretched by the output of UC23 pin 9 which clocks in the high on the data line when IOCS* first comes active and holds the chip select line active.

To adjust the timing requirements of the 6800 family IC's to the operation of the Z80A, a number of special-purpose timing signals were created. IOWAIT (I/O Wait) is one of these signals, produced by the

combination of IORQ* negative-ANDed with a Read or Write operation and validated by the output of the timing chain composed of the four flip-flops seen at B5 and B6. The output of this timing chain, which was held reset before the IORQ* occurred and is clocked at 4 MHz, controls the length of IOWAIT* thereby providing an input to the Z80A WAIT* line, forcing the microprocessor to slow its activities to correspond to the I/O operation in progress.

Because the 6821 PIA does not utilize individual Read and Write inputs, the special-purpose signal IOW*/R (I/O Write active-low / Read active-high) is produced to signify the nature of an impending Input/Output operation. A WR from the Z80A puts a high at the D-input, pin 2, of UC23, causing a low at the not-Q output. This low produces the active-low value which is interpreted as a WRITE operation by the 6821. For a READ operation the data input to the flip-flop, being low, would cause a high out of the not-Q line which registers as a READ for the 6821.

The actual ENABLE signal to the 6821 IC's is provided by the signal labeled 68 ENABLE, activated by RFSH* (to provide the necessary 6821 internal clocking for the Refresh operation) or the output of the timing chain responding to an IORQ* (to produce the required timing strobe for the I/O operation).

Read and Write operations to the disk controller are strobed by either the DISK WE* (Disk Write Enable) or DISK RE* (Disk Read Enable) signals. The timing relies on the first flip-flop in the UC22 timing chain producing a Q-output which is validated by the last flip-flop in the chain in combination with a WR signal from the Z80A to produce the Disk Write Enable.

DISK RE* is produced from the Q-output of the first flip-flop in the timing chain negative-ANDed with a Z80A RD signal. DISK RE* and DISK WE* also provide the I/O read and write strobes required by the 8253 counter-timer.

Consult the timing diagrams for more detailed analysis of the signals discussed on this sheet.

MAIN LOGIC BOARD: SHEET 3 OF THE SCHEMATICS

The Z80A microprocessor, operating at a 4 MHz rate, coordinates most on-board activities for the Osborne Executive, interfacing the other components through 16 unidirectional address lines, 8 bidirectional data lines, and a number of control lines.

The Z80A receives a RESET* signal either from the act of powering up the Executive or from the deliberate pressing of the Reset button on the front panel. These two modes of reset are differentiated in that pressing the Reset button generates an Interrupt request to the Z80A; the Z80A avoids the time-consuming diagnostic routines it normally runs at power-up if it receives an interrupt with Reset accompanied by the vector address supplied by the pull-up resistors RN7 (the D0 line pulled low), hex FE.

The following timing diagrams, Figures C-6 and C-7, compare the two modes of reset.

When the reset switch, S1, is depressed, capacitor C58 discharges to ground, placing a low at the input of the 1489A causing a low-to-high edge to be transmitted to the pin 11 clock input of flip-flop UF21 (labeled the PB latch). The "1" clocked from the data input to the pin 9 Q-output is tied to the data input of the next flip-flop and clocked when the 64-microsecond, horizontal sync signal arrives. This high will be passed along to the third flip-flop in the chain when clocked by the Z80A's RFSH* line, causing a high to be outputted on the Q line. The high will be inverted by UF19 to become the start of the active-low Reset pulse.

Reset is sent to the 6821 PIA which controls memory bank selection; to the Z80A; to the video output latch; to the Z80A SIO/2; to the 1793 Floppy Disk Controller; and to the 6821 PIA which controls the parallel interface. It serves to initialize all the internal registers for these IC's and must be held long enough to meet the requirements for each chip.

The second flip-flop in the reset sequence, at the same time as it is clocked with a "1", transmits a "0" from its not-Q output to the first flip-flop's Reset input. The Reset creates a low out of the Q-output which will be clocked into pin 2 of UF20 by the following HSYNC signal. Since the resulting low pulls the Reset line of the third flip-flop in the sequencer producing a low out of the Q-output, the RESET* pulse is effectively turned off. By maintaining the RESET* pulse within these parameters,

it ensures that the information in the Dynamic RAM will not be lost--the information can still be retrieved for diagnostic purposes.

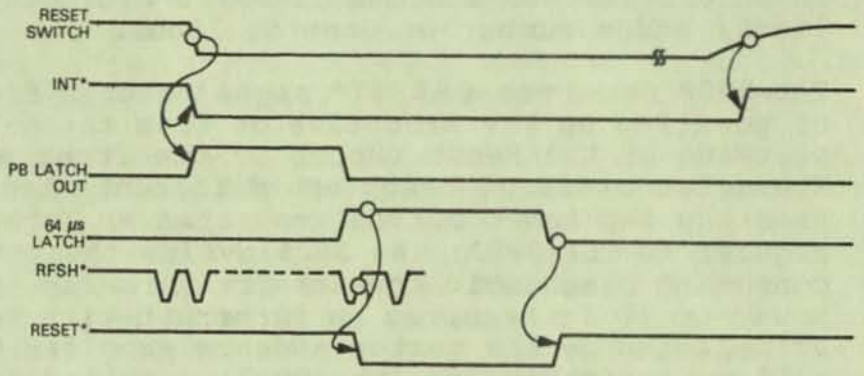


FIGURE C-6. RESET TIMING

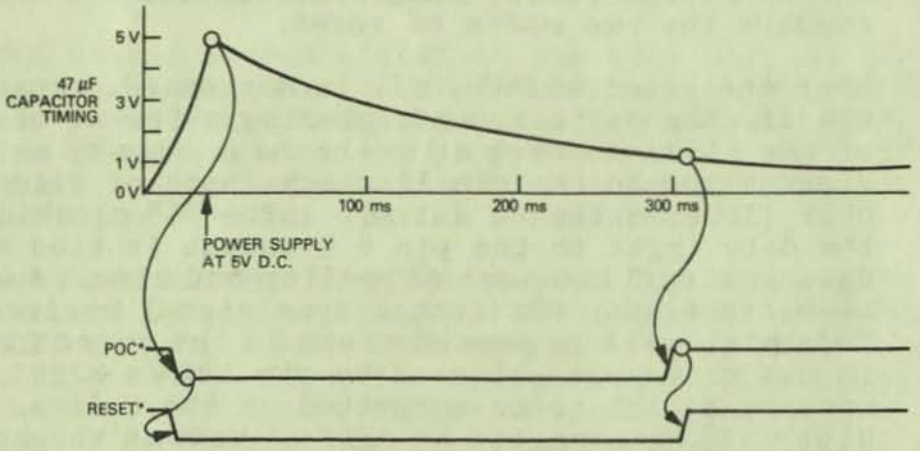


FIGURE C-7. POWER-ON CLEAR

The power-on Reset occurs in a different manner. At power-up, the capacitor C57 is charged through a resistor in the 1489A IC. As the voltage across this resistor passes the threshold level for the 1489A, the IC outputs an active-low signal to the S-input, pin 10, of UF20. This forms the start of the Reset* pulse. The Reset* pulse ends when the capacitor charges to the point where the voltage across the 1489A's internal resistor drops below the threshold level, releasing the input at pin 10. The input to the pin 13 Reset pulls the Q-output low and produces a high signal out of the UF19 invertor to drop the R signal.

When power is turned off, the capacitor C57 discharges rapidly through diode CR7.

Four signal lines are not utilized for this application of the Z80A. Inputs BUSRQ* and NMI* are each pulled high to remain inactive; and outputs HALT* and BUSAK* are not connected.

The Interrupt Request line (IRQ*) notifies the Z80A of devices on the board wishing to be serviced. The Z80A SIO/2 uses this line when there is activity on either of the serial communication lines. Likewise, the 6821 PIA uses IRQ* to alert the Z80A to communication events on the parallel (IEEE 488) lines.

The Z80 SIO/2 is capable of generating an interrupt vector onto the data lines to cue the Z80A to the starting address of the proper service routine, but the present application uses only a 3-bit vector from the SIO to denote one of eight interrupting conditions. The Z80A, when utilizing Mode 2 Interrupt handling, automatically inputs the contents of the data lines to obtain the vector address whenever it acknowledges an external interrupt. For all devices other than the SIO, the vector becomes hex FE, fixed by resistor values on the data lines. The Z80A then determines the nature of the interrupt by polling each device in order of priority.

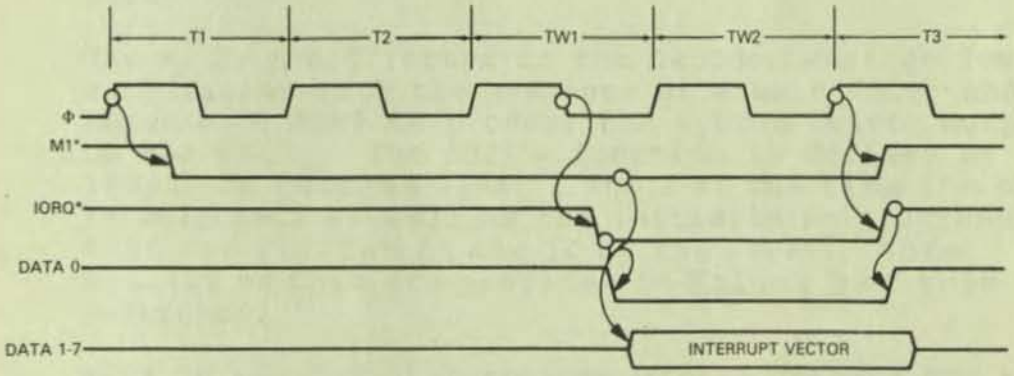


FIGURE C-8. INTERRUPT ACKNOWLEDGE

Note that the signals IORQ* and M1* (which normally do not occur simultaneously) are negative-ANDed to produce the INT ACK (Interrupt Acknowledge) signal which pulls the D0 line low forcing the low-order bit of the interrupt vector to be 0.

Two signals are capable of holding the Z80A in a WAIT state (the Z80A will suspend operations in order to synchronize itself with a slower device). The line IO WAIT* originates from the timing network on Sheet 2 and is used to permit the Z80A to function with the IC's in the 6800 family. The signal VRAM WAIT* prevents the Z80A from attempting to access the Video RAM if a Direct Memory Access operation or video

access operation is being performed.

The RFSH* line serves to validate the periodic refreshing of Dynamic RAM. Full refreshing of the Dynamic RAM must occur at least every 2 milliseconds to prevent loss of data. The refresh address automatically generated by the Z80A handles the refresh one row of memory at a time.

MAIN LOGIC BOARD: SHEET 4 OF THE SCHEMATICS

By means of a system of Input/Output and Memory Mapping, the Executive selectively enables the correct device or area of memory before performing a READ or a WRITE operation. Two components interacting, the 6821 Parallel Interface Adapter and the 74LS138 1-of-8 Decoder, maintain control over the necessary signal lines to accomplish this.

The decoding of the I/O device addresses is performed by the 74LS138 using three address inputs and three enable signals to activate one of eight chip select signals. One of these chip select signals, labeled SYS SEL* (System Select) on the schematics, chooses the 6821 PIA which is utilized for bank enable functions (to activate a desired segment of memory) and monitoring and controlling other on-board operations.

Of the three enable inputs to the 74LS138, pin 6 is tied permanently high. One is the actual I/O chip select signal, IOCS*, produced in response to the Z80A's IO REQUEST through the timing network on Sheet 1. The final signal, ADR7, requires that this address line be low if any I/O decoding is to take place.

The A, B, and C inputs to the Decoder must be low in combination with the presence of enable IOCS* and the absence of ADR7 to produce the System Select output to the 6821. The 6821's function is defined by the levels on Address lines 1 and 2 at the time the chip is selected, as well as the initializing programming that was written to the IC by the Z80A. More details on this are provided in Volume D of this reference.

Z80A IN and OUT instructions with addresses 00h to 03h are decoded as chip selects for the 6821 PIA. Channel A and Channel B may each be selected for a Data/Direction Read or Write, or a Control Read or Write.

Interrupt response of the 6821 is also programmable through the setting of two internal control registers (CRA and CRB). By the values stored in these registers, the functions of the two Interrupt Inputs (CA1 and CB1) and the two Peripheral Control lines (CA2 and CB2) are defined. The 6821 notifies the Z80A of an Interrupt condition by activating the IRQA* (Interrupt Request Channel A) or IRQB* (Interrupt Request Channel B); in this application the two lines are tied together (as an "open drain" functioning in a wire-OR configuration). The Z80A

must perform a READ operation of the control registers of the 6821 to determine which interrupt flag bits are set.

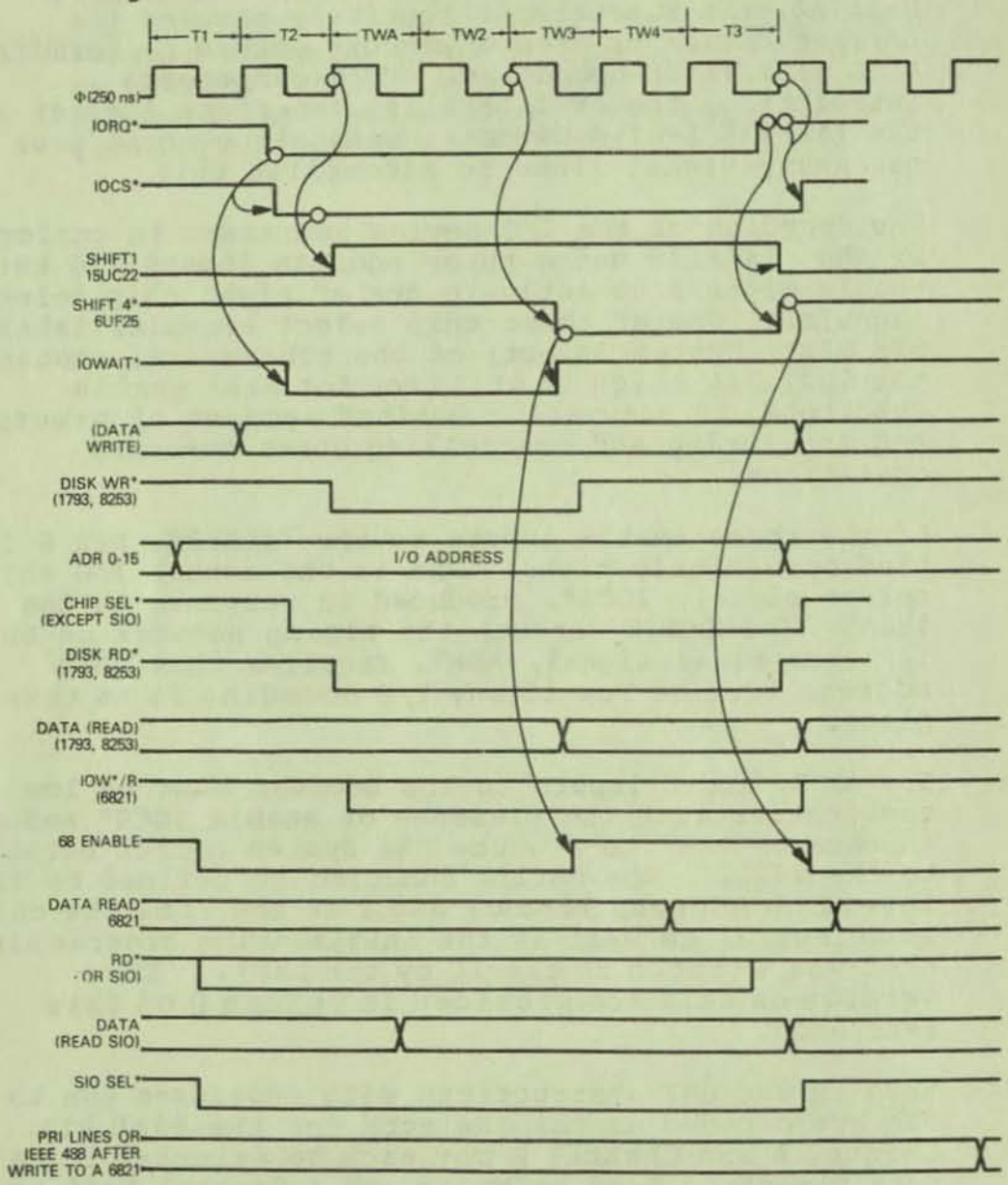


FIGURE C-9. I/O CYCLE TIMING

Notice that the CA1 Interrupt Input is fed by DMA IRQ* (Direct Memory Access Interrupt Request) which is routed through the connector P12, the DMA connector. This interrupt condition permits a device external to the main logic board which normally accesses only the address and data lines of the video memory to notify the Z80A CPU directly of some condition.

For the Executive the CA2 line may be programmed to function as an input or output, in this case, a Keyboard Strobe signal which allows interfacing the computer with an intelligent keyboard.

The remainder of the Channel A signals are programmed as outputs: the eight Bank Enable lines, labeled PRI1 (Priority 1) through PRI8. The P11 connector interfaces with the separate Dynamic RAM PC board where the PRI1 line is used to switch from the default bank, BANK0, to BANK1. PRI8 enables the ROM memory bank. PRI7 enables the Video memory bank. The other five bank-enable lines are available to handle bank switching should memory expansion be employed.

The Channel B Interrupt Input, CB1, receives the VBLANK (Vertical Blanking) signal from the video timing circuitry on Sheet 7. This signal orients the Z80A to the occurrence of the vertical retrace interval which precedes the display screen scan.

The CB2 line is used to supply a signal to the video timing circuitry defining whether the frame rate of the display is to be 50 or 60 Hz (depending on the power source selected).

The PB7 line inputs the MODEM RI* (Modem Ring Indicator) signal, alerting the Z80A to incoming information on the RS-232-C Modem port.

TXC SEL (Transmit Clock Select) and RXC (Receive Clock Select) serve to gate the appropriate clock signal from the modem to the Z80A SIO/2 inputs.

Similarly, the drive select signals, DSEL2* and DSEL1*, activate the appropriate disk drive prior to data exchange activity.

The DDEN* (Double-Density) line is supplied as an indication to the Floppy Disk Controller that double-density encoding and decoding should be employed.

The signal out of PB3 drives the Audio Transducer, X2. By varying the frequency of the pulses sent to the 7406, UF7, the pitch of the audio signal can be varied.

MAIN LOGIC BOARD: SHEET 4 OF THE SCHEMATICS

The signals out of the I/O Decoder are defined as follows:

VID ENA*: Video Enable--Serves to re-enable the video output after a reset. It is activated after all initialization is complete so as to keep any stray images from appearing on the video display immediately after power-up or reset.

RTC SEL*: Real Time Clock Select--Enables reading the Real Time Clock by gating the outputs onto the Data Bus through the 74LS244 tri-state buffer, UF13.

KBD SEL*: Keyboard Select--Serves to gate the Row and Column information from the Keyboard matrix, through the 74LS244, and onto the Data Bus for the Z80A to read.

488 SEL*: IEEE 488 Port Select--Enables the 6821 PIA that controls the IEEE 488 port.

FDC SEL*: Floppy Disk Controller Select--Supplies a chip select input to the 1793 Floppy Disk Controller to activate it for operations involving the disk drives.

CTC SEL*: Counter-Timer Circuit--Provides a chip select signal to the 8253 CTC permitting it to generate clock signals to the printer, modem or spindle clock lines.

SIO SEL*: Serial Input/Output Select--Supplies the chip enable input to the Z80A SIO/2 to activate it for communication over either of the serial ports.

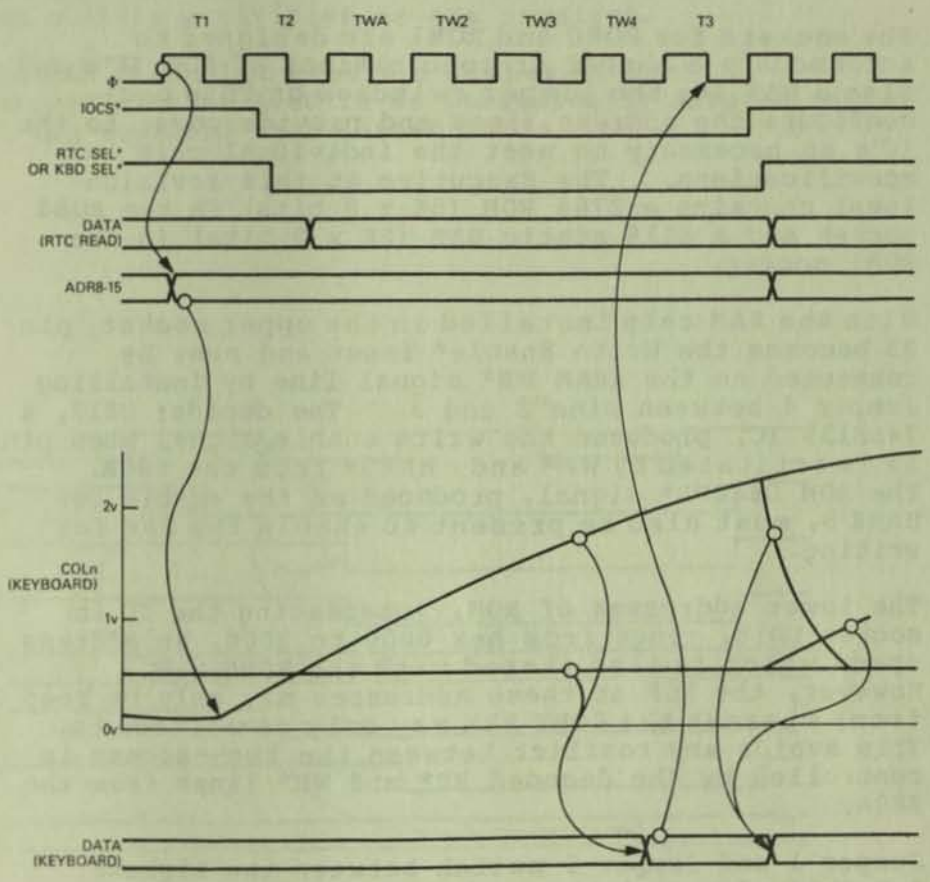


FIGURE C-10. KEYBOARD I/O TIMING

MAIN LOGIC BOARD: SHEET 5 OF THE SCHEMATICS

The sockets for ROM0 and ROM1 are designed to accommodate a number of combinations of ROM IC's and also a RAM IC; the jumper switches on this page configure the address lines and provide power to the IC's as necessary to meet the individual chip specifications. The Executive at this revision level contains a 2764 ROM (8K x 8 bits) in the ROM0 socket and a 6116 static RAM (2K x 8 bits) in the ROM1 socket.

With the RAM chip installed in the upper socket, pin 23 becomes the Write Enable* input and must be connected to the XRAM WR* signal line by installing Jumper 4 between pins 2 and 3. The decoder UE17, a 74LS139 IC, produces the write enable signal when pin 15 is activated by WR* and MREQ* from the Z80A. The ROM DECODE* signal, produced as the enable for BANK 8, must also be present to enable the RAM for writing.

The lower addresses of ROM, interfacing the IC in socket UD18, range from hex 0000 to 2000, an address space which is also shared with the FONT RAM. However, the ROM at these addresses may only be read from; whereas the FONT RAM may only be written to. This avoids any conflict between the two--access is controlled by the decoded RD* and WR* lines from the Z80A.

Jumper 1 and Jumper 5 switch between the highest accessed address line at the ROM0 and ROM1 sockets, respectively, and the +5 V supply line which is required to be switched to pin 26 to provide Vcc if a 2732 or 2764 IC is utilized in the socket.

The FONT RAM is enabled by the signal FONT EN*, produced by the negative-NANDing of ROM DECODE* and pin 12, active-low, out of UE17. Pin 12 will output a low at the conjunction of WR* (enabling the decoder) and the absence of any high address value at input A combined with the active-low MREQ* signal from the Z80A.

FONT WR* then occurs half a clock cycle later as the Phi* high-to-low transition causes a pulse to be outputted from UC19, pin 6. This pulse acts as the strobe to write data into the FONT RAM.

Within the ROM, as utilized for this particular Revision Level of the Executive, are the routines necessary to boot strap the computer upon power-on; to initialize the hardware; to write the introductory message to the screen; to perform I/O operations at

the hardware level; and to handle various diagnostic and utility activities as are required.

The RAM is used to handle a number of machine parameters that need to be periodically altered such as the keyboard translation table.

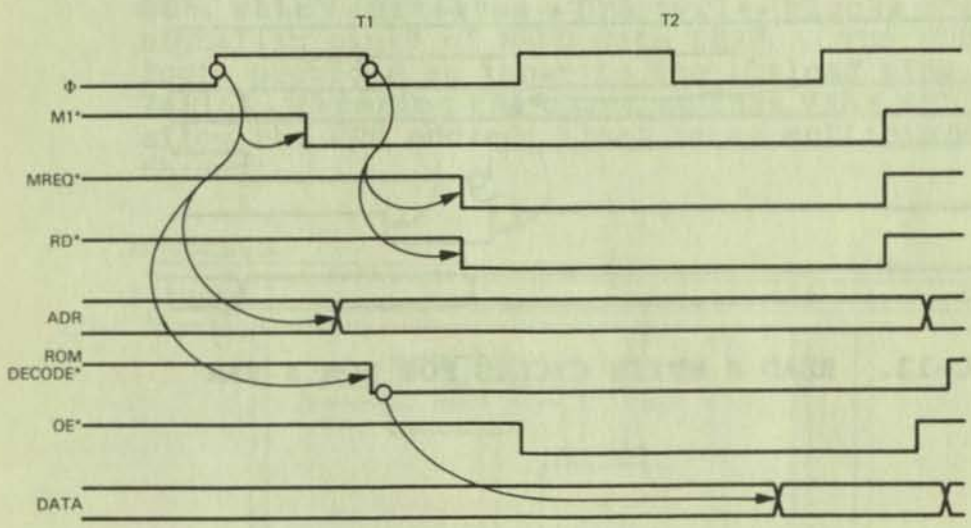


FIGURE C-11. ROM M1 CYCLE

MAIN LOGIC BOARD: SHEET 5 OF THE SCHEMATICS

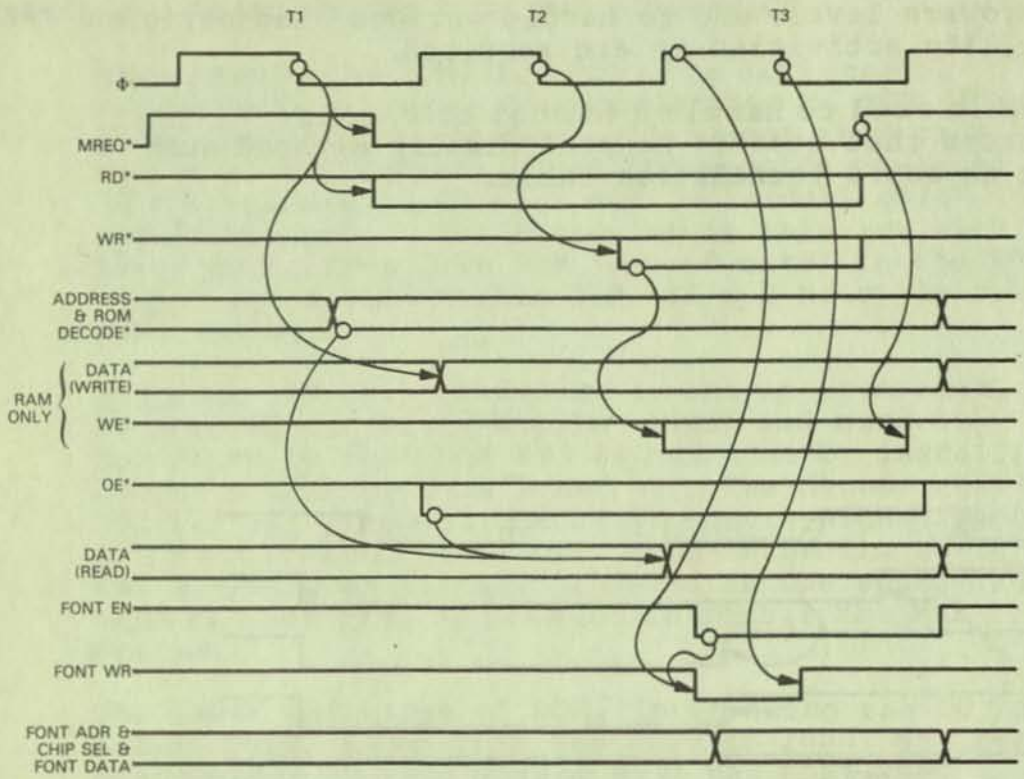


FIGURE C-12. READ & WRITE CYCLES FOR ROM & RAM

MAIN LOGIC BOARD: SHEET 6 OF THE SCHEMATICS

The signals generated by the video timing network on this sheet serve to limit access to the Video RAM for specific periods, allowing the Z80A to access the RAM during a specific window period, and the automatic sequential reading of the RAM to occur during another period. VRAM SEL (Video RAM Select), outputted as the most-significant line from the 74S161 counter, instructs the Video RAM Multiplexer (seen on Sheet 8) which address lines to gate to the Video RAM: the Z80A address lines or the video timing lines. Z80A access to the RAM may be overridden by the Direct Memory Access provisions; the incoming signal DMA GO*, which initiates a DMA cycle, blocks the VRAM RQ signal at pin 9 of NAND-gate UE20. The subsequent logic provides an input to the preload pins of the 74S161, altering the count so that VRAM SEL will not allow the CPU address lines to be multiplexed through.

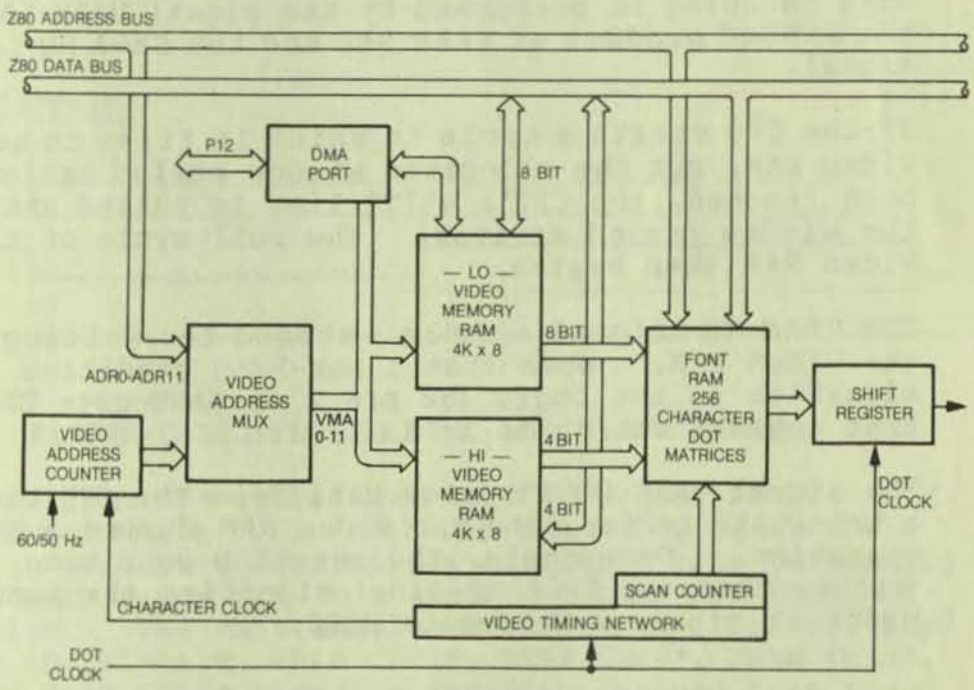


FIGURE C-13. VIDEO SYSTEM BLOCK DIAGRAM

The timing chain is driven by DOT CLK, a 12 MHz signal derived from the divided-down output of the crystal oscillator, X1. DOT CLK provides the clock input for the 74S161 4-Bit Synchronous Counter at location C4. The count is arranged so that for every 8 cycles of the dot clock, a full cycle of the character clock (CHAR CLK*) is generated.

MAIN LOGIC BOARD: SHEET 6 OF THE SCHEMATICS

The character clock controls the timing regulating the vertical blanking interval, increments the Text Address count (giving row position indications), latches the attribute bits through the video path synchronously with the video data output, and clocks the two flip-flops that can suppress the video output during either horizontal or vertical blanking periods.

The latter half of the character clock is used to produce the signal DMA INH, useful for a DMA device to coordinate data transfer with the video memory.

Each 8 transitions of the dot clock also produces the signal SR LOAD* (Shift Register Load) which takes parallel video data off the video RAM data bus for conversion into a serial bit stream.

During a CPU read of the Video Memory, the character out of the VRAM is temporarily latched into a flip-flop and then read shortly thereafter by the CPU. This latching is performed by the signal VRAM LATCH*, the NANDed product of VRAM SEL and the Z80A RD signal.

If the CPU starts a cycle in which it tries to access Video RAM, but the allocated window period has not been reached, the CPU's WAIT* line is pulled until the window period arrives. The full cycle of the Video RAM then begins.

The VRAM WR* signal acts as a strobe for writing into the Video RAM. Note that a not-READ condition signifies to the logic (at pin 2 of NAND-gate UE18) that a WRITE operation is indicated.

The signal VRAM DOUT* gates data from the CPU through a tri-state buffer into the Video RAM during a WRITE operation. Once again, the not-READ condition (rather than the Z80A WR line) signifies the pending WRITE at pin 2 of NAND-gate UE20.

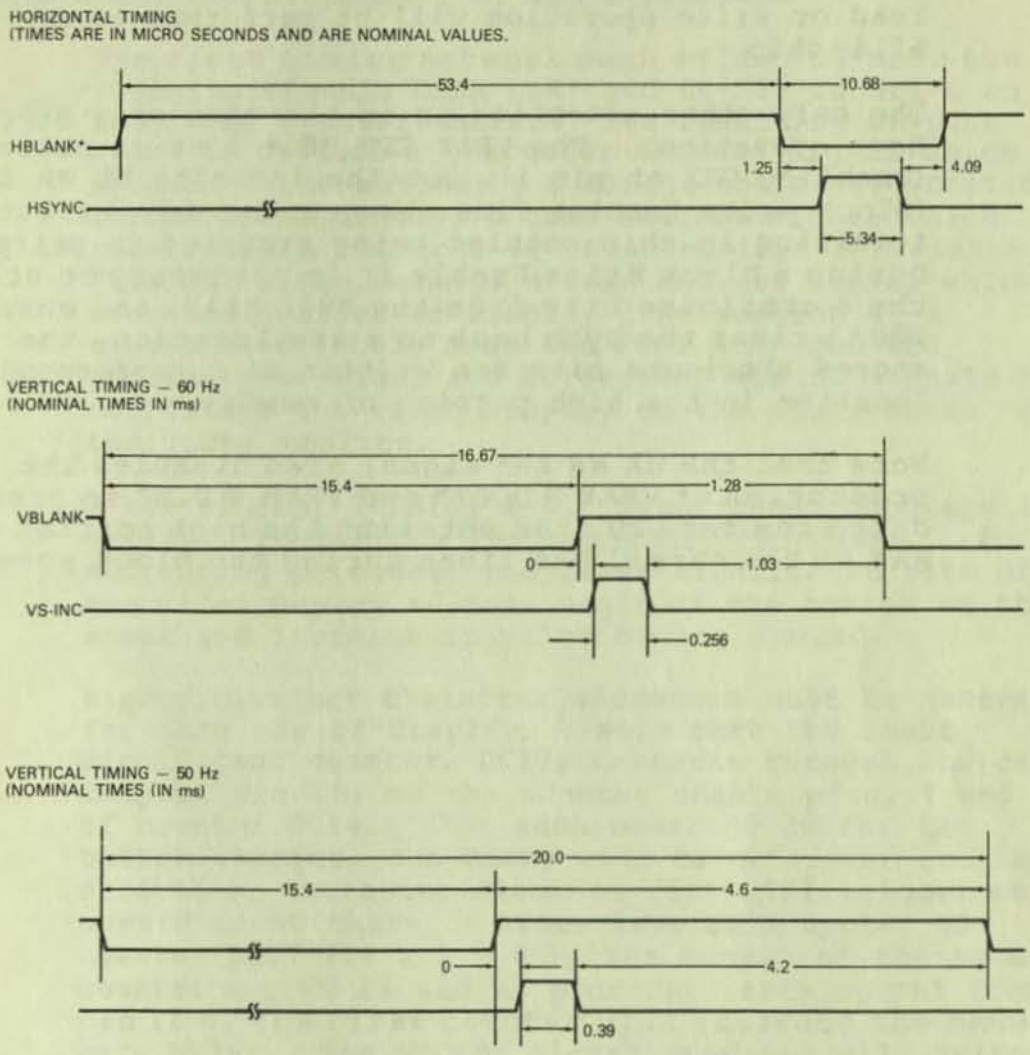


FIGURE C-14. VIDEO SYNC AND BLANK TIMING

The Video RAM is divided into a low portion (containing a full 8 bits of character data) and a high portion (containing 4 attribute bits pertaining to each character) each consisting of two 6116 RAM chips. The chip enables to these IC's are provided by the signals VRAM CEH1*, VRAM CEH0*, VRAM CEL1*, and VRAM CEL0* based on decoding derived from the four 74LS139 1-of-4 Decoders.

Normally a pair of video memory chips (encompassing either hex addresses C800 - CFFF and D800 - DFFF or C000 - C7FF and D000 - D7FF) is enabled simultaneously, allowing the full 12-bit data word to be accessed from the Video RAM for display. If the CPU is reading or writing to the Video RAM, the signal VRAM CPU SEL* is produced, enabling the decoder UB2 at pin 1. The incoming ADR 12 line from the Z80A, when decoded, differentiates between the

low portion of memory and the high, ensuring that the read or write operation will be performed to a single 6116 chip.

The only other exception is in the case of a Block Move operation. The VRAM CPU SEL* line is active (enabling UB2 at pin 1), but the incoming BK WR EN* (Block Write Enable) line changes the decoder output, resulting in chip enables being produced in pairs. During a Block Write Enable it is necessary to store the 4 attribute bits from the Z80A READ, and when the Z80A writes the byte back to a new location, the stored attribute bits are written to a corresponding location in the high portion of memory.

Note that the BK WR EN* signal also disables the production of VRAM H DOUT* and VRAM H DIN* to prevent data from the CPU from entering the high portion of RAM on the normal bus lines during the block move.

MAIN LOGIC BOARD: SHEET 7 OF THE SCHEMATICS

The video timing network seen on Sheet 7 uses the incoming signals CHAR CLK* and 60*/50 to drive an intricate counter chain. The resulting outputs serve to produce a character address signal which addresses automatically a single character location in the video memory; a text address signal which references a row (one of 26 accessible for display) from the video memory; a scan address signal which accesses a slice or display line portion of a character directly from the FONT RAM; and the necessary vertical and horizontal timing signals to coordinate the video display to the electronics of the video monitor.

A set of four 74LS161 4-Bit Synchronous Counters is employed to perform the necessary functions. For addressing purposes, the least-significant bits of the video memory address begin at the bottom of the sheet and increase in value moving upward.

Eighty distinct character addresses must be generated for each row of display. Note that the least significant counter, UC17, connects through its carry output, pin 15, to the counter enable pins, 7 and 10, of counter UC14. For each count of 16 for the bottom counter, one carry will be generated and the arrival of character clock at UC14 will trigger an upward count there. After five full cycles of counter UC17 (16 x 5 = 80), the output of the second counter's pins 11 and 12 plus the carry output from pin 15 of the first counter will activate the NAND-gate UF18. The HLOAD* signal produced will initiate a synchronous loading of both counters to the hex value F0, equivalent to a -16.

Simultaneously, the HBLANK* interval will be started; the high-level condition from pin 11 of UC14 will be held until the bottom counter goes through a count of 16, outputs the carry signal allowing UC14 to count at the character clock. The Fh value in counter UC14 will recycle to 0, dropping the pin 11 output low, and concluding the HBLANK* interval.

During this horizontal blanking interval, the output of flip-flops UE19 and UA6 will produce the count enable signals for the third counter in the network, UC12. Thus, for each blanking interval, UC12 will increment once, advancing the scan line count.

When the scan line count reaches a decimal "10", the outputs from pins 11 and 13 satisfy NAND-gate UE4, and one portion of the resultant signal is routed back around to the LOAD input of the counter to

preset it for the next count of ten scan lines. Another portion of the signal out of the NAND-gate activates the J and K* inputs of UE3 (pins 2 and 3), causing it to toggle at the next arriving character clock signal, thus creating the least-significant address value for the text address. The final portion of the NANDed value enables the counting of UC2, causing the row address to increment.

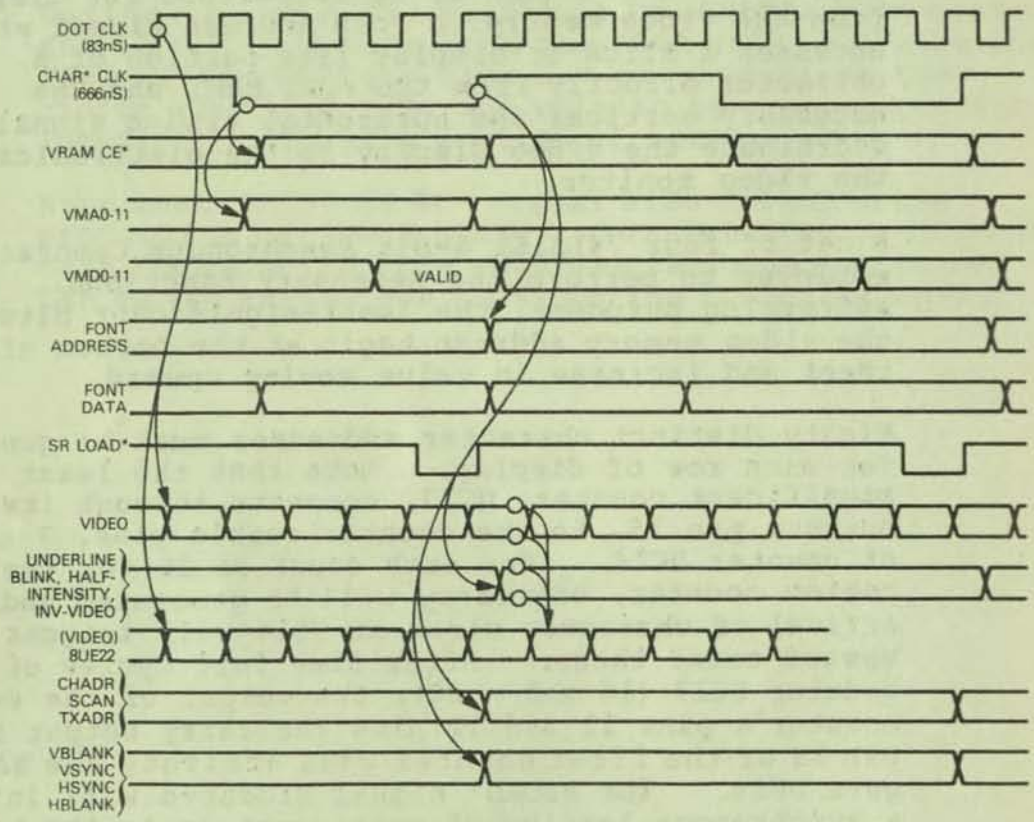


FIGURE C-15. VIDEO TIMING

By this method, all the characters stored in a row are accessed ten times for the display of one character line, but each time a different scan line address to the FONT RAM results in a different slice of the character's dot matrix to be displayed. After all 10 slices of all 80 characters on the line have been displayed, the timing network increments the text address accessing the next row of characters from the video memory.

Twenty-six rows of video memory are counted by the combination of 4-Bit Counter UC2 and the JK flip-flop UE3 shown at C4. The JK flip-flop is used to simulate the first stage of a synchronous counter. Two lines occur during the vertical blanking interval; the other 24 occur during the visible portion of the display.

The pin 6 output of JK flip-flop UE3 is used as TXADR0 and also as one enable to the 74LS161 counter. Each time the JK clocks to output a "1" from this line, the incoming CHAR CLK* signal will increment the counter if the scan counter (UC12) has reached line 10 thereby supplying the other necessary enable.

At the end of the 24th line, the decoded output of the counter UC2 places a low at the K* input of JK flip-flop UE3 to initiate the vertical blanking period--VBLANK*. A delay of two character clocks occurs at JK flip-flop UE3 as the high Q-output is brought back around to satisfy NAND-gate UF18 with the decoded output of the counter. When the JK flip-flop begins to toggle, Q drops low triggering the start of the vertical blanking interval.

The low output of UF18 also produces the signal VLOAD* which causes a synchronous loading of a -2 value at the counter when the next character clock arrives at pin 2 of UC2. VLOAD* also serves to set the scan address counter back to 0. The text address counter counts from -2 to -1 and back to 0 covering rows 25 and 26 and restarting the display screen at row 0 when the vertical blanking interval is turned off.

During the vertical blanking interval, the vertical sync pulse is produced by flip-flop UF21, set by the active-low output of UE3 and reset by the clock pulse supplied by scan line 2. The vertical sync pulse is used by the monitor electronics to initiate the retrace period.

The signal 60*/50 affects the presetting of the counters UC2, and UC12 at the start of the vertical blanking interval. If the computer is being operated from a 50 Hz supply, low values will be fed into pins 3 and 4 of UC2 forcing the counter to take longer to leave the vertical blanking period. This delay results in a number of extra scans being added at the end of the display screen, but does not affect the timing in any other way.

MAIN LOGIC BOARD: SHEET 8 OF THE SCHEMATICS

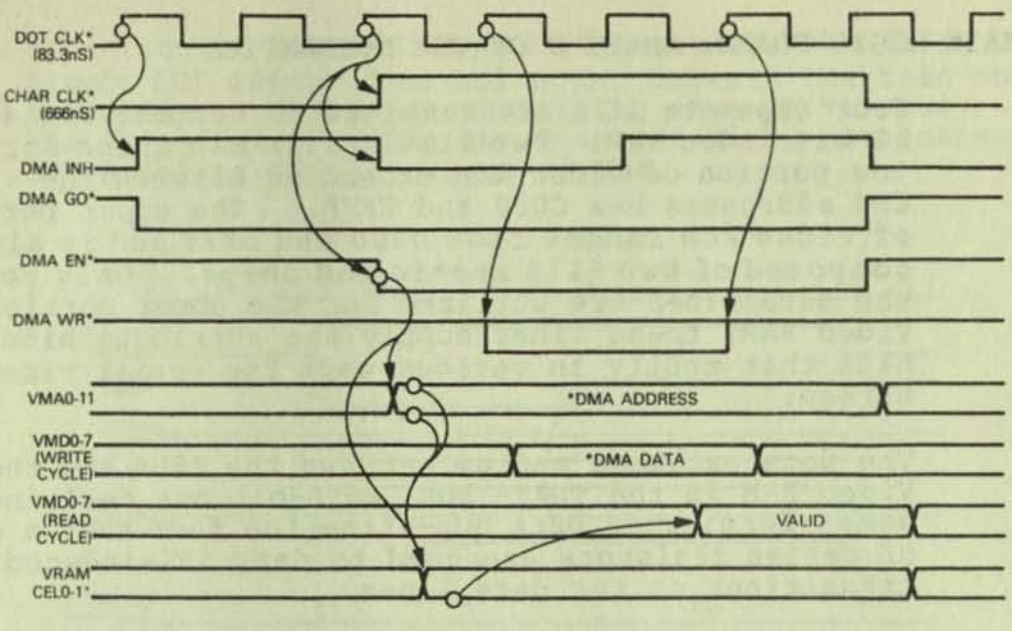
Three possible means of addressing the video display memory exist; these means are illustrated on Sheet 8 of the schematics.

Twelve address lines, VMA0 through VMA11, interface the 4K x 12 RAM that makes up the video memory. Through the three 74LS257 multiplexers, the memory may be addressed by the Z80A microprocessor; automatically (without intelligent control) by the video timing network as part of the display sequence; or through intervention by an external device on the DMA port, connector P12.

Any DMA access of video memory takes priority over CPU access. The signal DMA EN* (DMA Enable) serves to force the multiplexers into a tri-state condition allowing the DMA device use of the address bus and the data bus of the video memory. The DMA device, however, must keep track of the video-memory timing cycle through the supplied timing signals to avoid preempting the normal video display sequence. Otherwise display errors will result.

The Video Ram timing circuit shown on Sheet 6 produces the data select input (VRAM SEL0) which, if low, selects the addressing from the video display network; if high, from the Z80A microprocessor. VRAM SEL avoids any possible bus conflicts in attempting to access the video memory.

The timing for DMA access is illustrated in the following timing diagram:



* DMA ADDRESS AND DATA ARE ASSUMED TO BE SUPPLIED BY THE DMA BOARD DURING THE TIME THE EXECUTIVE BOARD COMPONENTS ARE IN TRI-STATE.

FIGURE C-16. DMA CYCLE

MAIN LOGIC BOARD: SHEET 9 OF THE SCHEMATICS

Four separate IC's are combined to compose the 4K x 12 bit Video RAM. Two 6116 static RAM chips form the low portion of Video RAM extending between the CPU addresses hex C000 and CFFF. The upper portion of Video RAM ranges from D000 and DFFF and is also composed of two 6116 static RAM chips. Only four of the data lines are utilized for the upper portion of Video RAM; these lines supply the attribute bits, 4 bits that modify in various ways the serial video bit stream.

The data exchange medium between the Z80A and the Video RAM is the TDATA bus, an 8-bit bus deriving its name--Terminated Data bus--from the fact that a group of series resistors are used to damp TTL-induced transitions on the data lines.

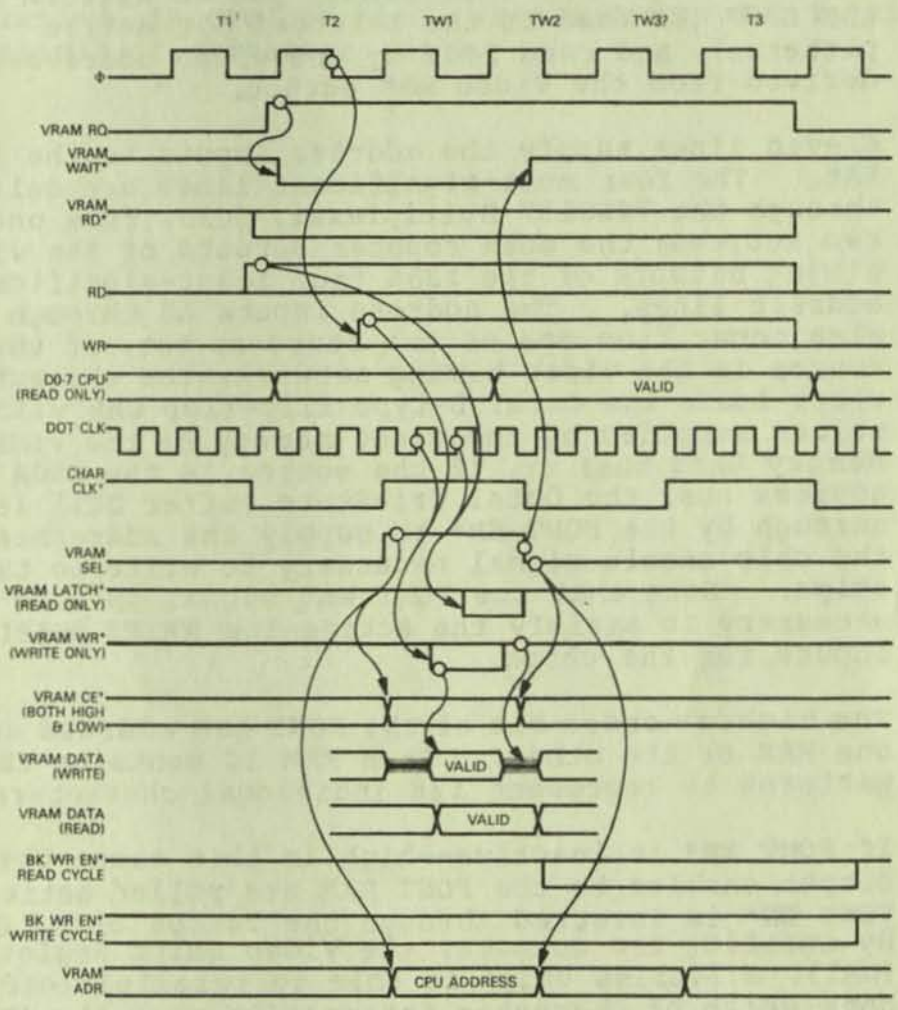
When the Z80A is performing a normal WRITE operation to the Video RAM, the high and low RAMs must be written to individually: the 8-bit data bus cannot accommodate the 12-bit word that the Video RAM stores. Both high and low RAMs are accessed together automatically as part of the display process, supplying a 12-bit word to the VMD bus (Video Memory Data). The VMD lines 0 through 7 go directly to the FONT RAM to produce the necessary characters. The VMD lines C, D, E, and F go to other circuitry, in parallel motion with the rest of the video word, to alter the displayed characters by adding an underline, blinking effect, half intensity, or inverse video.

If the Z80A is performing a READ operation of the Video RAM, the addressed data is latched into the Octal D-Type Flip-Flop UC9 by the signal VRAM LATCH*. By performing a quick read cycle, the Z80A can read the contents of the latch at a later time without interfering with the video display cycle.

Circuitry is provided through the register UA8, flip-flop UE11, and buffer UA7 to handle both the high and low video RAMs simultaneously during a block move operation. A block move consists of a READ followed by a WRITE (without an intervening Z80A M1 cycle); conditions require that the operation be within the address confines of Video RAM.

During the block move, the attribute bits stored in high Video RAM are moved in conjunction with the appropriate byte in the low video RAM. The attribute bits are latched into the 74LS173 during the READ cycle, and then gated out by the VRAM WR* signal. The 74LS74 flip-flop only allows this

operation if the M1* signal (attached to the flip-flop's SET input) does not occur between the read and the write. Otherwise the rising edge of M1 sets the flip-flop, forcing the Q-output high, preventing the enabling of the output of UA8.



VRAM CE* LINES HAVE SEPARATE DELAYS FOR LOW (ACTIVE) AND HIGH (INACTIVE).

NOTES: ═══ INDICATES BUS CONFLICT.

ALL SIGNALS FROM DOT CLOCK DOWN CAN BE MOVED BY ANY INTEGER MULTIPLE OF 24 MHz PERIOD (≈41.7nS) EARLIER OR LATER.

A BLOCK MOVE CONSISTS OF A READ CYCLE FOLLOWED DIRECTLY BY A WRITE CYCLE. BK WR EN* GOES LOW DURING THE READ (AS SHOWN) AND STAYS LOW DURING THE WRITE AND RETURNS HIGH WHEN THE CPU EXECUTES AN OP CODE FETCH (M1 CYCLE).

FIGURE C-17. TYPICAL VIDEO RAM READ & WRITE CYCLE

This block move operation is carried out in one instance as part of the initialization of the video memory. A space character is written into the first byte of the low section of video memory with appropriate attribute bits in the high. Then a block move is performed, reading from the first location and writing into the second location and so on until the entire video memory has been cleared of any random characters.

MAIN LOGIC BOARD: SHEET 10 OF THE SCHEMATICS

The FONT RAM stores within two 2K x 8 6116 static RAM chips the representational dot patterns for the characters that will be displayed on the video screen. This two-port memory can be written to by the Z80A (to load in the selected dot matrix patterns), and read from by the video addresses derived from the Video RAM output.

Eleven lines supply the address inputs to the FONT RAM. The four most-significant lines are delivered through the 74LS157 Multiplexer, UC13, from one of two sources: the scan counter outputs of the video timing network or the Z80A four least-significant address lines. The address inputs A0 through A7 also occur from one of two sources, but, if the source is the video timing network, the character clock loads the Octal D-type flip-flop UA9 with the values supplied by the video memory on the Video Memory Data bus; or, if the source is the Z80A address bus, the Octal Tri-State buffer UC11 is gated through by the FONT EN* to supply the addresses and the chip enable signal necessary to write to the RAM chips. Note that the FONT WR* signal is also necessary to satisfy the active-low WRITE ENABLE inputs for the chips.

The highest-order bit of the FONT RAM address selects one RAM or the other. Each RAM IC contains the bit patterns to represent 128 individual characters.

If FONT EN* is inactive--high in this case--the output enables to the FONT RAM are pulled active when FONT EN* is inverted through the 74LS04 chip, UE17. By enabling the outputs, the Video Shift Register (UA13, a 74LS166 chip) is able to parallel-load eight dots worth of character information when the SR LOAD* signal goes true. The DOT CLK then will drive the shift register to output the actual video information, a portion of a character's dot pattern, to the circuitry that supplies the video monitor.

The Video Shift Register is held reset whenever the Z80A is performing a WRITE operation into the FONT RAM. This prevents any extraneous dot patterns from reaching the screen.

The two D-Type flip-flops seen at the top of the sheet (each labeled UA6) serve to transfer the attribute bits through the system synchronously with the video data. The signal CHAR CLK* drives the flip-flops. The delay introduced at this point for the attribute bits corresponds with the delay required to access the video data from the FONT RAM.

MAIN LOGIC BOARD: SHEET 10 OF THE SCHEMATICS

One additional attribute bit, inverse video, is stored in the lower portion of the video memory and thus is part of the 8-bit video data word. Inverse Video is handled by the flip-flop UE19 shown at D2. The data line, connected with VMD7 of the video display, is clocked high, when appropriate, by the arrival of character clock.

MAIN LOGIC BOARD: SHEET 11 OF THE SCHEMATICS

Sheet 11 illustrates the circuitry that translates the signal representing the video data to the levels necessary for the internal monitor, the external monitor output, and the composite video output. The components that produce the Real Time Clock, used to record elapsed time while interrupts are disabled, are also shown at the bottom of the sheet.

A delay of two character clocks is induced in the signals HBLANK* and VBLANK* by the two 74LS175 flip-flops, UE19, producing the signal, CBLANK*. CBLANK* turns off the video that goes to the monitor during the horizontal and vertical retrace times.

The video signal enters OR-gate UC19 at pin 13 and is modified according to how the various attribute bits affect the random logic that interacts with the video.

If the UNDERLINE attribute is active, each time the scan count reaches 10 (the bottom line of the dot matrix) the AND-gate UE23 at location D7 will be satisfied and the underline displayed after passing through the remainder of the logic.

The INV VID (Inverse Video) signal, if active, will change the logical state of the video (dark to light and light to dark) at the Exclusive OR-gate UF16.

The blink rate is a function of the output of the ripple counter, UE13, a 74LS393 IC. If the blink attribute bit is on, the rate of blinking is regulated at AND-gate UE4 by the ripple counter's output, between 1 and 2 blinks per second.

The pin 8 output of NAND-gate UE4 is ORed and then X-ORed at UF16 to turn the video on and off at the prescribed rate (either letting dark and light go through, or holding the video to dark).

The DIM attribute bit feeds the data input of flip-flop UE22, pin 2, so that when clocked in by the dot clock the resulting low not-Q output will be sent to the 7406 inverters, lowering the output voltage of the video signal sent to the monitor.

Note that the CBLANK* signal, when active, prevents any video from passing through AND-gate UF15 at D4.

Table C-1 illustrates the effect that various combinations of attribute bits have on the video:

TABLE C-1. VIDEO ATTRIBUTE BITS

ATTRIBUTE					
UNDERLINE	ALT CHAR SET	REV VIDEO	BLINK	DIM	EFFECT
X	0	X	X	X	Selects 1st or 2nd 128-Character Video Font
X	1	X	X	X	
0	X	0	0	0	Dim Character on Dark Background
0	X	0	0	1	Bright Character on Dark Background
0	X	0	1	0	Alternating Dim and Dark on Dark Background
0	X	0	1	1	Alternating Bright and Dark on Dark Background
0	X	1	0	0	Dark Character on Dim Background
0	X	1	0	1	Dark Character on Bright Background
0	X	1	1	0	Dark Character on Dim Background Alternating with Dim Character on Dark Background
0	X	1	1	1	Dark Character on Bright Background Alternating with Bright Character on Dark Background
1	X	X	X	X	Underline Overrides Font Data and is Always Same Intensity as Character

The Real Time Clock is made up of an eight-bit ripple counter, UE13, and a 74LS244 tri-state buffer, UF13. It has two basic functions:

1. To generate the blink rate that turns the video on and off whenever the blink attribute is set. (The frame rate--either 50 or 60 Hz--is divided down to produce the necessary output.)

2. To provide a reference clock for the Z80A.

During the time the floppy disk controller is reading or writing a sector, the Z80A needs to respond rapidly to incoming characters or to supply the characters to be written. Interrupts are disabled during this time. The clock signal allows the Z80A to calculate and adjust for real-time interrupts that occur periodically (the interrupt generated through the PIA at every vertical blank signal).

Immediately before the Z80A disables the interrupts to handle the disk drive it reads the value from the ripple counter. After taking care of the disk drive, interrupts are turned back on and another counter reading is taken. By calculating the difference between the two values, the Z80A can adjust its operations for the time interval missed.

Since a ripple counter has a tendency to produce slightly skewed outputs, the Z80A reads the counter twice and makes a comparison between the two values. Only when it receives two identical values (indicating that the output of the ripple counter has stabilized at a correct value) will the Z80A interpret the count as being correct.

The signal RTC SEL*, a decoded I/O strobe, is used to gate buffer UF13 onto the data bus, allowing the Z80A to read the counter's outputs.

The composite video output combines the video with the sync signals for a composite signal that varies between 0 and 2 volts. This output, designated as P10, meets RS-170 standards, and monitors not designed to function within the prescribed signal parameters should not be attached to this connector.

Varying signal levels differentiate the black, half-intensity, white, and sync signals from each other as seen by the monitor.

The output to the internal monitor, P9, is illustrated at the right of the sheet in the middle. The signals required by the monitor PC board are shown being outputted: the vertical and horizontal synchronization signals, the video bit stream, the three lines directed to the brightness potentiometer, the +12 V power to the monitor, and the chassis and power grounds. All signal lines are buffered and shifted to levels appropriate to the monitor electronics.

An edge connector, P5, is also provided to connect the early-version Osborne monitors that some users may have. Due to a variation in the width of the Executive's horizontal sync pulse as compared to the pulse required by the early monitor board, an adapter is necessary to use this interface.

The incoming VID ENA* signal occurs as the result of a decoded I/O instruction generated by the software at such time as the video memory is cleared and normal display is ready to begin. The pin 13 reset of UE22 is held, suppressing the video display, until the system is properly initialized.

MAIN LOGIC BOARD: SHEET 12 OF THE SCHEMATICS

The Z80A SIO/2 manages the two serial communication channels provided by the Osborne Executive, offering asynchronous communication with a DTE (Data Terminal Equipment) device such as a printer and either synchronous or asynchronous communication with a DCE (Data Communication Equipment) device such as a modem. The Z80A SIO/2 may be programmed by the Z80A for a wide variety of communication applications and protocols; specific details as to the capabilities of the SIO/2 are provided in Volume D of this manual.

By writing to the SIO/2's control registers, the Z80A conditions it for the communication activities planned. Upon initialization the following conditions are set according to the current revision level of the monitor ROM:

The X16 Clock Mode is selected.
One stop bit will be utilized.
No parity is utilized.
Each received character will be represented by 8 data bits.
Auto enables are turned on.
Receive enable is turned on.
Each transmitted character will be represented by 8 data bits.
Transmit enable is turned on.
Request to Send is activated.
Data Terminal Ready is activated.
Channel B is set to operate in a mode where changes in status will affect the interrupt vector.
External interrupt is enabled.
Receive interrupt is set to trigger on all received characters.
The parity of received characters will affect the interrupt vector.

Channel A is capable of either utilizing the transmit and receive clocks generated by the modem or operating from the internal clock produced by the timing network of the Executive. The two control signals, TXCSEL and RXCSEL (seen at location D7), perform the selection of clocks from the modem, rather than internally, by routing the buffered inputs from the RS-232-C connector P1 to the SIO/2 clock inputs.

The 8253 Programmable Counter-Timer Circuit, seen directly below the SIO/2, provides the necessary communication clocks when so selected at a rate prescribed by its initialization settings and the clock input from the 74S161 Synchronous Counter.

The counter divides the 24 MHz clock signal by 13 to produce an exact value of 1.8432 MHz.

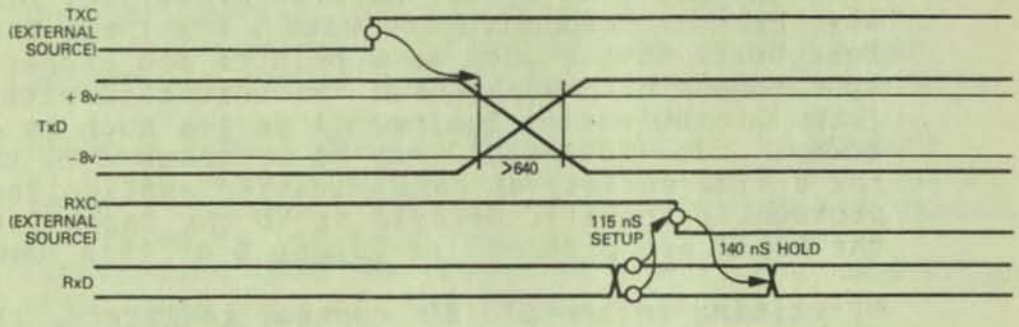


FIGURE C-18. SIO PERIPHERAL TIMING

The CTC responds to data words written into it from the Z80A data bus to generate a variety of baud rates for communications purposes. The clock times delivered to the SIO/2 should be 16 times greater than the desired baud rate for asynchronous mode. The following table equates the data word values with the desired baud rate. To determine the actual clock signal value outputted by the CTC, multiply the baud rate by 16.

TABLE C-2. DATA WORDS FOR BAUD RATES

Data word (in decimal)	Baud rate
2304	50 baud
1536	75 baud
1047	110 baud
847	134.5 baud
768	150 baud
384	300 baud
194	600 baud
96	1200 baud
64	1800 baud
48	2400 baud
32	3600 baud
24	4800 baud
16	7200 baud
12	9600 baud
06	19200 baud
03	38400 baud

One line out of the 8253 CTC (OUT2, pin 17) is intended to be utilized for regulating the speed of the spindle motor on the disk drives for special-purpose data handling and increased precision of operation. This function is not utilized for this revision level of the main logic board.

The two DB25S connectors, P1 and P2, interface to the main logic board through typical RS-232-C drivers and receivers. The signal levels present on the communication line are converted to TTL levels for compatability with the logic board circuitry.

Jumpers J12 and J13 provide the capability of manipulating the choice of ground connections for the RS-232-C connector. The jumper can be left open, connected to earth ground, or connected to signal common to correspond with any given application of the RS-232-C port.

Jumper J11 is provided to supply +12 volts to power the Osborne modem.

Two modem status lines, MODEM RI* (Modem Ring Indicator) and MODEM DSR* (Modem Data Set Ready), are converted to TTL levels before being routed to the 6821 PIA where they can be detected by the Z80A.

MAIN LOGIC BOARD: SHEET 13 OF THE SCHEMATICS

Three primary components are involved in converting data that is transferred to and from the disk-drive electronics boards into the appropriate formats.

The 1793 Floppy Disk Controller (FDC) acts as the intermediary between the Z80A CPU and the drive electronics. Besides parallel-to-serial and serial-to-parallel data conversion, the FDC converts diskette address information into directional signals for the disk drive, maintains a status register for the CPU, provides signals to control the Write Precompensation circuitry, detects ID, data, and index address marks during read and write operations, generates a 16-bit Cyclic Redundancy Check character for error detection, and functions utilizing both FM and MFM data-encoding techniques.

The Write Precompensation IC, UA17, reacts to control signals from the FDC to induce changes in the positioning of data on the diskette. These positioning changes are designed to compensate for data shifts that normally occur because of electromagnetic factors inherent in the rotating diskette.

Three possible means are available for handling the process of data separation, removing the embedding clock signals from the incoming data stream for use by the FDC. The 9216 Floppy Disk Data Separator (FDDS) provides data separation for both FM and MFM data formats. It must be removed from the circuit board if the Analog Data Separator (the Double-Density Hybrid circuit, UA20) is installed at the connector shown at B5.

Additionally, the connector P13 allows the double-density adapter board, originally designed for use on the Osborne 1, to be attached. Future revisions of the main logic board will eliminate this connector.

The Z80A interfaces with the FDC through 8 bidirectional data lines, and 6 control lines. Timing is provided by a 1 MHz clock signal.

Two register select lines, A0 (pin 5) and A1 (pin 6) are used to choose the register where the data will be written to or read from. The direction of the data transfer is determined by the Read Enable (RE*) and Write Enable (WE*) lines.

The register select lines define the operations as shown below:

CS*	A1	A0	RE*	WE*
0	0	0	Status Reg	Command Reg
0	0	1	Track Reg	Track Reg
0	1	0	Sector Reg	Sector Reg
0	1	1	Data Reg	Data Reg

The Interrupt Request line, outputted from pin 39, is delivered to the Z80A through the 488/Parallel Interface, the 6821 PIA shown on Sheet 14. When the Z80A detects the Interrupt Request, it will poll all devices in the order that is established by priority, reading the status register of the FDC in turn. Status will vary according to the type of command that was previously issued to the FDC by the CPU.

Several capabilities of the FDC remain unused. The DRQ (Data Request) output is ignored; this signal functions as a handshaking signal during data exchange. The Interrupt Request line serves to provide the same basic function for this operation.

The TEST* has special-purpose diagnostic functions and is designed to normally be tied high.

The HLD (Head Load) line is tied back to the HLT (Head Load Timing) input; the FDC will assume that the recording head is perpetually loaded. Since there is no head loading occurring for the present application, this function is handled as such.

The RDY (Ready) line at pin 32 is also tied permanently high signifying to the FDC that the diskette drive is in a constant state of readiness for any read or write operations.

WF*/VFOE* (Write Fault*, VFO Enable*) signifies writing faults when connected, but is not utilized for this application.

The Floppy Disk Interface consists of a number of signals to control movement of the recording heads over the diskette, to detect various conditions present at the drive, to format the outgoing data stream as necessary, and to input returning serial clock and data signals for conversion to parallel data bytes.

MAIN LOGIC BOARD: SHEET 13 OF THE SCHEMATICS

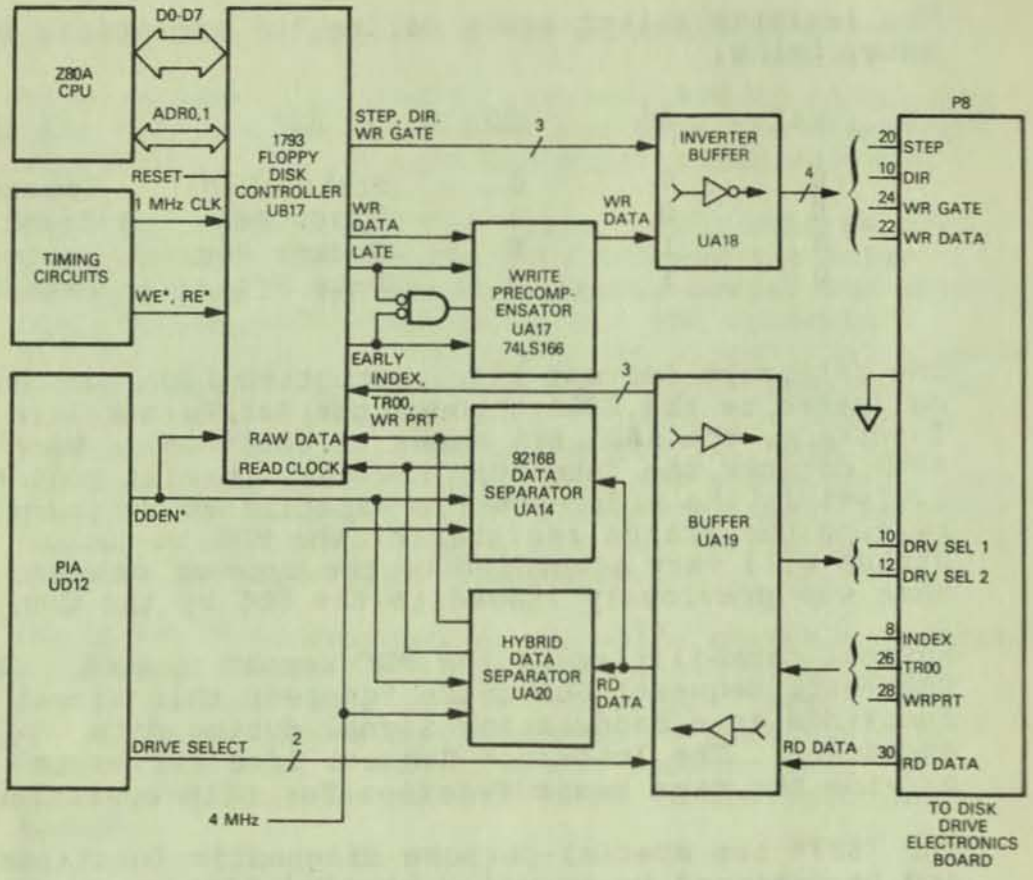


FIGURE C-19. DISK CONTROLLER FUNCTIONAL BLOCK DIAGRAM

The STEP and DIR (Direction) lines provide incremental movement of the recording head to position it at the correct track. The STEP line produces a pulse to move from one track to another; the DIR line indicates whether that movement should be towards the center of the diskette or away from it. The 7406 drivers adjust the signal levels for use by the disk drive electronics.

Notice at the top of the P8 connector that the signal SPINDLE* provides the capability of controlling the rotational speed of the disk drive's spindle motor. This feature is not utilized with current disk drive configurations.

INDEX* pulses returning from the disk drive orient the FDC to a fixed position on the diskette--one index pulse is returned for each revolution of the diskette.

The WPRT* (Write Protect*) line indicates the disk drive has detected the presence of a write-protect sticker on the diskette, a warning that no WRITE operations may be directed to the diskette.

The TR00* (Track 00*) indicates that the Read/Write head is located directly over the Track 00 position on the diskette.

The Read Gate at pin 25 is provided to synchronize external data separators. The SSO (Side Select Output) is a signal indication that will be available whenever a 1797 FDC is substituted for the 1793. The 1797 FDC is capable of handling double-sided diskette drives, and the SSO line relates to this ability.

The Write Gate at pin 30 comes valid immediately prior to a Write operation to the diskette.

The Write Data signal is the actual serial data stream from the FDC to the diskette. For MFM recording, a 250 nanosecond pulse is outputted for each flux transition. For FM recording, the pulse width is 500 nanoseconds. Before being sent to the diskette, the Write Data signal is sent to the 74LS166 shift register for timing alterations.

Write Precompensation is based on the control signals LATE and EARLY from the FDC. Any Write Data pulse occurring while the EARLY line is active will be shifted out early to be written to the diskette. The late signal indicates that the Write Data pulse will be shifted out late to be written to the diskette. The absence of the EARLY and LATE signal causes the Write Data pulse to be shifted out serially without any timing alteration.

Write Precompensation adjusts for bit shifts that occur as different patterns of bits are written to the diskette. The calculated timing alterations produced by the shift register overcome this tendency of the bits to shift by writing the bits in the opposite direction of their known shift, causing them to read back in their nominal position.

Incoming data from the diskette drive is routed through pin 30 of the P8 connector to the Read Data Separator where the clock signals and the data signals are isolated from each other and channeled separately to the FDC.

The 9216 FDDS receives the 4 MHz Phi* signal and divides it according to the signals present at Pin 5, CD0, and pin 6, CD1. Since the CD1 line is tied to ground, only the CD0 line is available to select one of two divisors. If the DDEN* (Double-Density) signal is present, cueing the FDDS to MFM formatting of the data stream, the divisor of the clock signal will be "1" (leaving it at the initial 4 MHz).

The separated clock is timed to run at one sixteenth of this rate, so the RDCLK signal to the FDC will have a frequency of 250 KHz. A divisor of 2 is used on the clock for FM formatting, resulting in a 2 MHz reference clock signal and a 125 KHz RDCLK signal to the FDC.

The DSEL2* and DSEL1* lines shown at the bottom of the sheet serve to activate the desired disk drive. The jumper J6 provides the capability to offer a MOTOR ON* signal to those drives that require a signal to start their motors spinning. This jumper should not be connected for the normal drives supplied with the Executive.

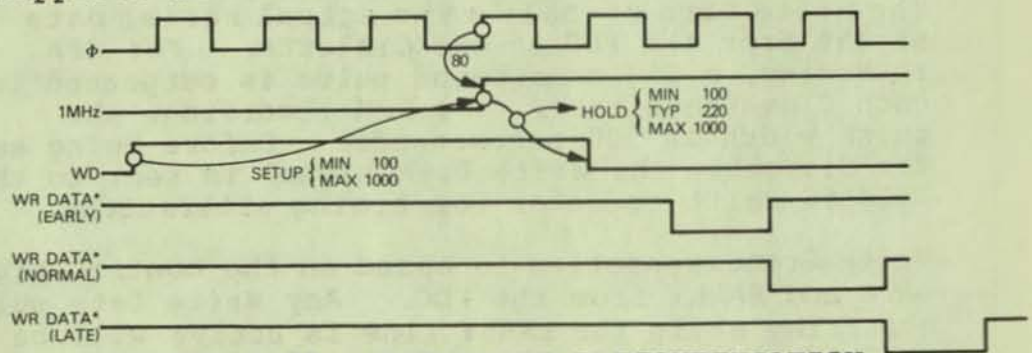


FIGURE C-20. FDC WRITE PRECOMPENSATION

MAIN LOGIC BOARD: SHEET 14 OF THE SCHEMATICS

The 6821 Peripheral Interface Adapter (PIA) shown on Sheet 14 is used quite differently from the System PIA illustrated on Sheet 4. The IEEE 488 port is serviced by this PIA, the inputs and outputs having been programmed by the Z80A at initialization. A collection of drivers and receivers translates the signal levels as necessary to maintain the standard between the IEEE 488 levels at the P3 connector and the TTL requirements of the PIA.

The signal definitions applicable to this port may vary (within the range of acceptable subsets defined by the IEEE 488 standard) to meet specialized applications. However, for purposes of discussion, the signal definitions may be examined as defined through the Monitor ROM at initialization.

Eight data lines provide the parallel exchange medium. At the Z80A side of the exchange, the lines are labeled DATA0 through DATA7, interfacing the PIA bidirectional lines D0 through D7. At the PIA side of the exchange, the data lines at the P3 connector are labeled DI01 through DI08; these lines interface, after passing through the appropriate drivers or receivers, with PIA bidirectional lines PA0 through PA7. Depending on whether a READ or a WRITE operation is to be performed, the PA0 through PA7 lines are programmed to function as inputs or outputs. A "1" is written to the Data Direction Register of the PIA by the Z80A for each line intended to function as an output. A "0" written to the same register causes the corresponding data line to become an input.

Two of the three required chip-select inputs for the PIA (CS0 and CS1) are tied high so that the third chip select, 488 SEL* from the I/O decoder, serves to activate the PIA for a required function. The 68 ENABLE line is the sole timing signal utilized for PIA functions; this enable adapts the timing criteria maintained by Z80 family IC's to the necessary timing for 6800 family products.

The register select lines, RS0 and RS1, direct data to or from the desired PIA internal registers. The Z80A uses its two least-significant address lines to perform this function.

MAIN LOGIC BOARD: SHEET 14 OF THE SCHEMATICS

The RESET* input responds to a power-on reset or a master system reset by clearing all the PIA's internal registers.

The IOW*/R (Input/Output Write/Read) line, produced by the timing network seen on Sheet 2, controls the direction of data transfer with the PIA.

The two interrupt-request outputs of the PIA (IRQA* and IRQB*) are tied together. An interrupt request is generated either from the floppy disk controller requesting an interrupt (FDCIRQ*) or the service request line being activated by a device connected to the IEEE 488 port. The Z80A deduces the identity of the interrupting device by polling.

The B section of the PIA is devoted to the handshaking signals that coordinate the IEEE 488 data exchange process. Once again, the PB0 through PB7 lines are programmed to act as either inputs or outputs by the Z80A.

Note that the CA1 and CB1 inputs function as interrupt requests for this particular application. CA2 and CB2 function as peripheral control signals with the following definitions:

IFC (Interface Clear) at CA2 acts to reset the connected device to a known state.

REN (Remote Enable) at CB2 acts to transfer control from the front panel to the IEEE 488 bus.

The other signals related to the IEEE 488 port are:

NDAC (No Data Accepted) signals acceptance or non-acceptance of data by the receiving device.

EOI (End or Identify) signifies the end of a message block if ATN is inactive. If ATN is active, EOI signals a request for a parallel poll.

DAV (Data Valid) provides a strobe function when the information on the data bus is valid.

NRFD (Not Ready for Data) provides either a "busy" indication, or indicates a readiness to accept data, depending on its state.

ATN (Attention) alerts the connected device to the presence of a command byte on the data bus, as opposed to actual data.

MAIN LOGIC BOARD: SHEET 15 OF THE SCHEMATICS

The keyboard interface is exceptionally simple from a hardware point of view. Eight of the Z80A address lines are buffered through to the row inputs of the keyboard. This provides the Z80A with the necessary interface to produce a pattern upon the address lines which may then be read back from the column outputs on the keyboard through the 74LS244 Tri-State Buffer. Only those lines for which a key depression has linked the row and column matrix will appear on the data lines when the Z80A performs the KBDSEL* (Keyboard Select IN instruction) to gate the contents of the tri-state buffer.

The jumpers J9 and J10 are provided to adapt the keyboard interface for the attachment of an intelligent keyboard. Jumper J9 supplies +12 V power to the keyboard, and Jumper J10 acts to route a Strobe signal for transferring data with the keyboard.

DYNAMIC RAM BOARD

The Dynamic RAM Board is situated directly above the Main Logic Board, separated by four standoffs keeping the two boards approximately 3/4 of an inch apart. The P1 receptacle of the Dynamic RAM board fits flush with the P11 plug on the Main Logic Board. All signals necessary for accessing the main memory are channeled through this connector.

The 128K-byte capacity of the Dynamic RAM is achieved by grouping sixteen 64K x 1 RAM chips into an 8 x 2 array. Each 64K x 8 bit memory segment represents one bank, addressable by 16 lines. Because only 8 address inputs are available to each group of 8 IC's, the total 16-bit address is accessed from the Z80A address lines in two 8-bit groups; one group is latched into the selected RAM IC as a row address, the next group as a column address.

To multiplex the correct set of address lines to the RAM IC's, two 74LS244 octal tri-state buffers are utilized. The gating action is triggered by the signals RAE* and CAE* which are produced on the main logic board as part of the system timing network. The row address enable is always received first and the address information latched into the appropriate register in each Dynamic RAM chip by the Row Address Strobe* signal. Then the column address enable gates the remainder of the memory address to the RAM chips. The occurrence of the Column Address Strobe* signal validates the address and makes either the memory data inputs or data outputs available to the bus depending on whether a READ or a WRITE operation is being accomplished.

The incoming RD* signal, shown at the top of the P1 connector, signifies by its inactive state that the pending operation is a WRITE. The high signal to the pin 2 data input of flip-flop U1 is clocked by RAS*, dropping the not-Q output at pin 6, thereby activating the WE* (Write Enable) lines for the selected bank of RAM.

The circuitry shown at the bottom left quadrant on the sheet illustrates the logic required to direct the row address strobe and column address strobe to the appropriate banks. Bank 0, normally enabled by the system unless otherwise specified, is logically related to the following conditions:

The ROM DECODE* line is not active, and

The VRAM DECODE* line is not active, and

The PRI 1 (Priority 1) bank enable is not present (which would indicate that BANK 1 had been enabled) or a hex F appearing on the 4 high order address lines (ADR 12 through ADR 15).

If these conditions are present, the NAND-gate U5 and the negative NAND-gate U4 will direct the RAS signal from the P1 connector to the Bank 0 RAM chips, and CAS* likewise to the same bank.

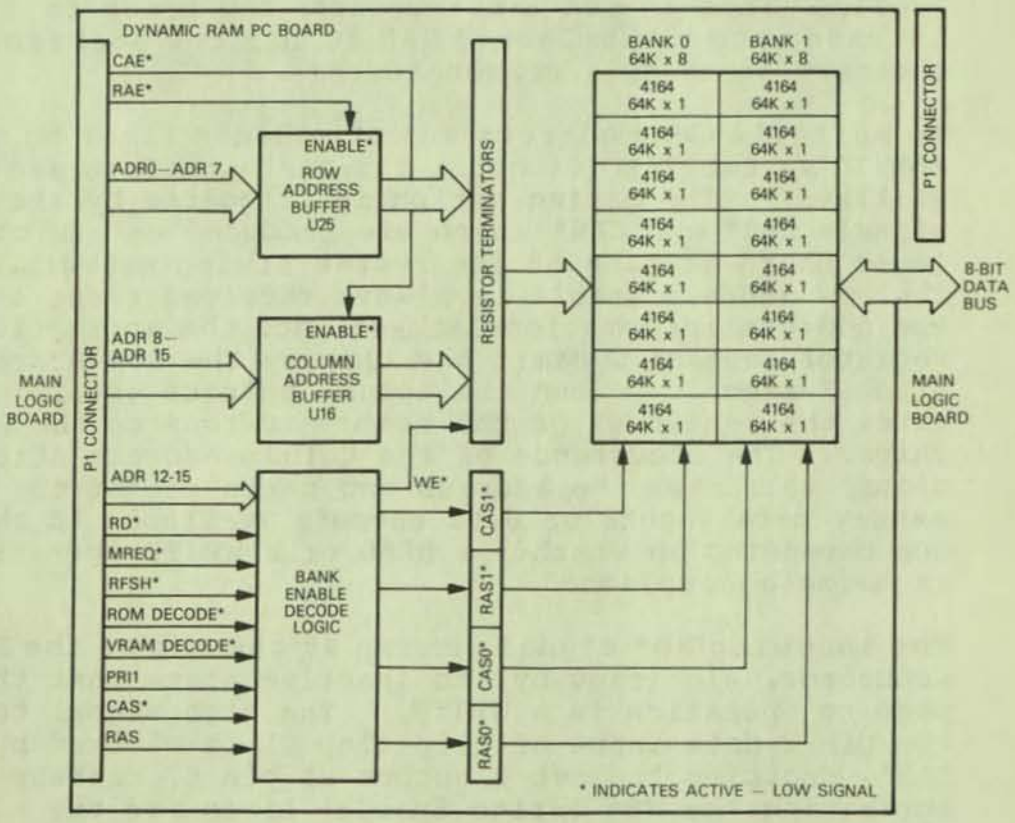


FIGURE C-21. DYNAMIC RAM FUNCTIONAL BLOCK DIAGRAM

The Bank 1 enable is generated through the following logic combinations:

The ROM DECODE* line is not active, and

The VRAM DECODE* line is not active, and

A hex F is not present on the 4 high-order address lines.

These conditions precipitate passage of RAS and CAS* through the logic network by satisfying pins 9 and 10 of NAND-gate U5 to produce RAS1* and pins 12 and 13 of negative NAND-gate U4 to produce CAS1*.

To accomplish the refresh cycle, the Z80A automatically supplies a refresh address, but the presence of the RFSH* signal suppresses generation of the column address strobe. Consequently, neither the data inputs nor the outputs of the RAM chips are activated, but one of the 128 rows within memory will be refreshed. To ensure data survival within the Dynamic RAM, a full refresh of all memory locations must be accomplished within a 2 millisecond period.

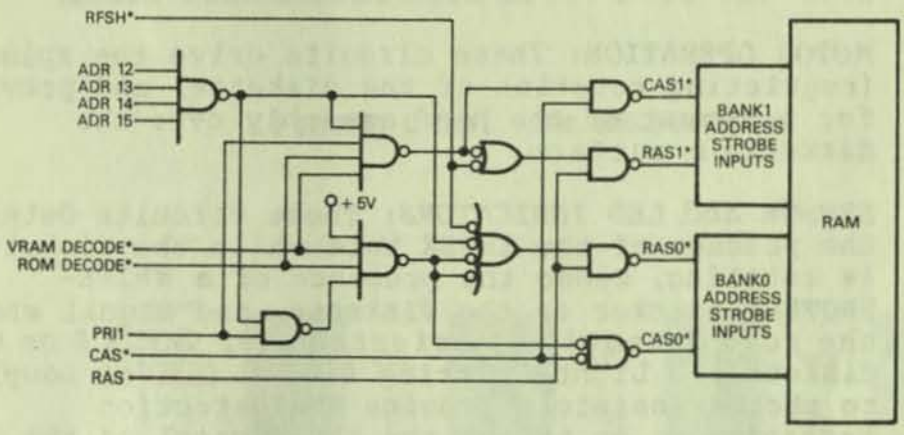


FIGURE C-22. RAS/CAS LOGIC

Note that the incoming ADR 7 line is disabled at NAND-gate U3 at the occurrence of RFSH*. The refresh logic only requires address lines ADR 0 through ADR 6 to be successfully accomplished. When RFSH* is not present, the ADR 7 line is gated normally through tri-state buffer U25. A portion of the circuitry shown on this sheet designated by the NOTE 3 symbol is not presently used, a remnant of an earlier design. Since one half of the flip-flop U1 is still utilized, the parts remain on the board.

The 4164 RAM chips have an access time of 200 nanoseconds and a cycle time of 335 nanoseconds.

DISK DRIVE ELECTRONICS

The disk drive electronics associated with the ALPS disk drives are contained upon three separate circuit boards. Data and control signals are routed from the Floppy Disk Controller and translated from the TTL levels utilized by the main logic board to the necessary levels for driving motors, accomplishing data conversion, and powering indicators. The circuitry performing these functions can be examined according to three primary groupings:

READ and WRITE OPERATIONS: These circuits control the routing of the data stream to and from the read/write head of the disk drive.

MOTOR OPERATION: These circuits drive the spindle (regulating rotation of the diskette) and provide for movement of the head assembly over the diskette's surface.

SENSOR and LED INDICATORS: These circuits detect the passage of the INDEX hole while the diskette is rotating, sense the presence of a WRITE-PROTECT sticker on the diskette, and signal when the head assembly is oriented over TRACK 0 on the diskette. Light-Emitting Diodes (LED's) coupled to phototransistors provide the detection mechanism. An LED on the front panel of the disk drive indicates disk-drive activity.

Stored data occurs in the form of flux transistions upon the magnetic oxide surface of the diskette. Depending on whether the information on the diskette is recorded in single-density or double-density format, the encoding technique will either be FM (Frequency Modulation) or MFM (Modified Frequency Modulation). The Executive 1 is equipped to handle both formats.

Clock pulses are embedded in the data stream at regularly spaced intervals for FM data and at intervals determined by the binary values represented for MFM data. The following diagrams show the manner in which the data is encoded.

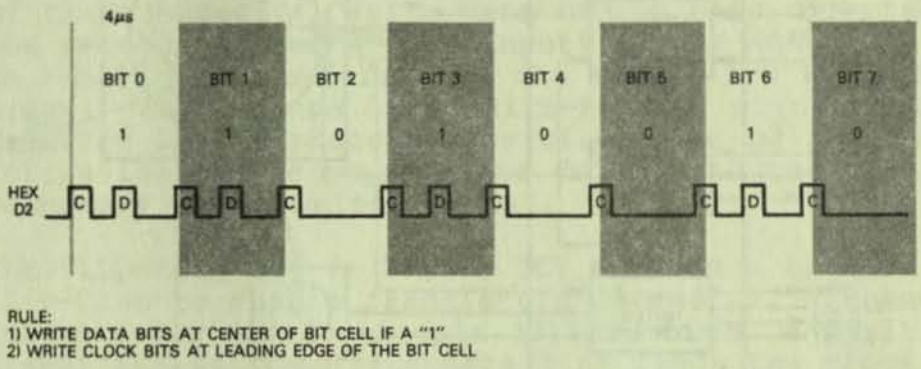


FIGURE C-23. FM RECORDING

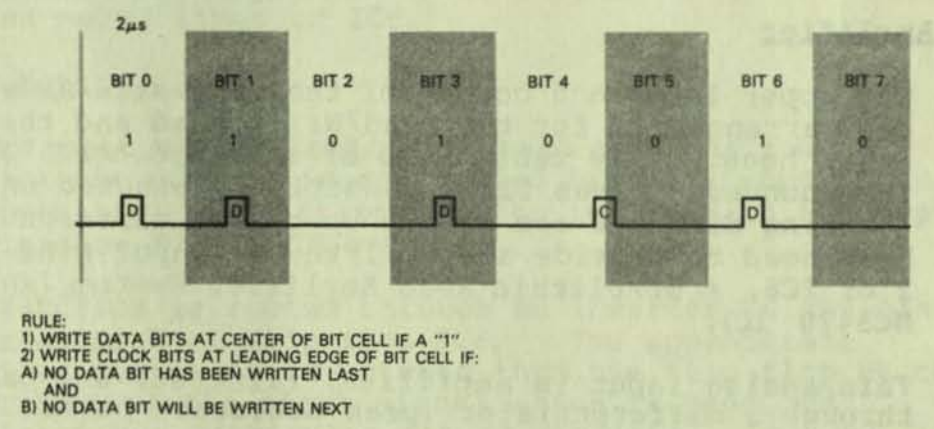
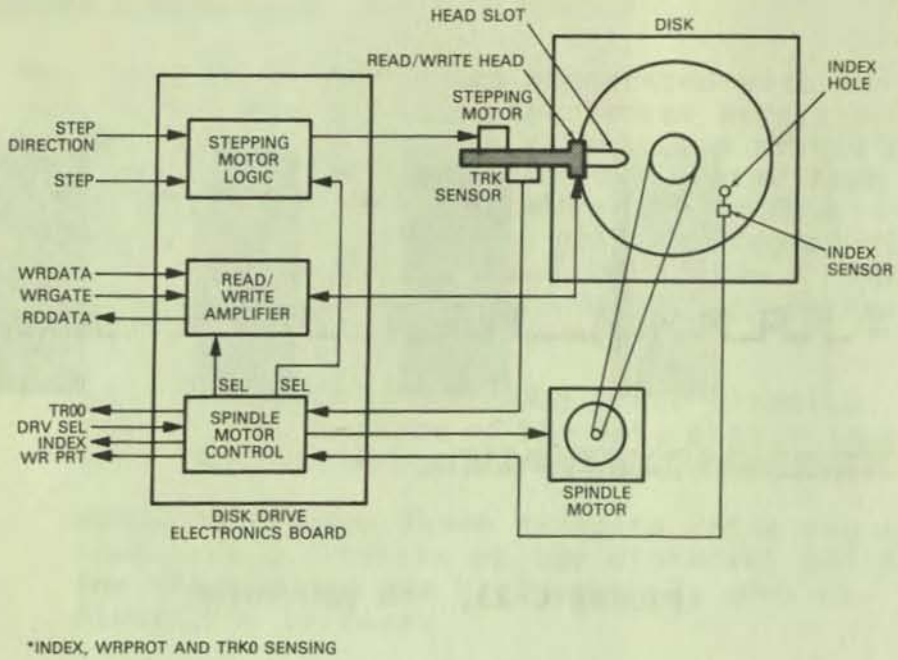


FIGURE C-24. MFM RECORDING

Theory of Operation

Two circuit boards arranged at right angles to each other are contained within the disk drive enclosure providing the majority of the drive's electronics. An additional smaller circuit board is located near the spindle offering spindle motor control functions.

The functional block diagram (Figure C-25) illustrates the overall architecture of the disk drive electronics boards.



*INDEX, WRPROT AND TRK0 SENSING

FIGURE C-25. DISK DRIVE ELECTRONICS FUNCTIONAL BLOCK DIAGRAM

Read Amplifier

The upper left-hand corner of the schematic shows the coil arrangement for the Read/Write head and the Erase head. The center tap of the Read head, J3-A4, is grounded. Thus flux transitions detected on the rotating diskette are picked up by the differential Read head to provide a signal to the input pins 1 and 2 of IC8, a monolithic Read Amplifier System (an MC3470 IC).

This analog input is amplified, filtered, and passed through a differentiator (peak detector) before being converted to digital data which is outputted from pin 10 of the IC. Pins 17, 16, 15, and 14 provide coarse filtering of the signal (through the attached filter network) to ensure that the bandwidth of the Read amplifier will reject that area of the frequency spectrum that is not significant.

Pins 12 and 13 are connected to active differentiator components. The differentiated Read signal is routed to a comparator circuit that supplies two One-Shot Multivibrators. The One-Shot Multivibrators provide discrimination of the digital signal as controlled by the RC time constants connected at pins 6, 7, 8, and 9. The signal out of pin 10 is in the form of the actual Read data to be decoded by the Floppy Disk Controller.

Write Operations

The incoming WRITE GATE signal controls the operation of the two output transistors, Q3 and Q4, seen at A1 of the schematic. Write data can be only directed to the recording head if the inputs to the NAND-gate IC5 (a 74LS10) are satisfied by the active-low WRITE GATE signal, the absence of a WRITE-PROTECT sticker (as detected by the photo-sensor circuit at D3), and the activation of the appropriate drive with the necessary drive-select signal.

The flip-flop IC6 (a 74LS74 IC) acts as a toggle flip-flop to enable transistors Q3 and Q4. Whenever Set (pin 10) and Reset (pin 13) are high, a positive transition of the Write data line feeds the clock input (pin 11) and causes the flip-flop to toggle. Each time the toggle occurs, a flux transition will be produced on the recording medium from the change in current directions to the coils as controlled by the activation of either Q3 or Q4.

Each complete pulse of Write data produces one flux transistion signified by an output change of the Q and not-Q lines of IC6.

Stepper Motor

Movement of the Read/Write head assembly over the diskette surface is controlled by the stepper motor circuitry. The stepper motor responds to two input signals: DIRECTION and STEP.

DIRECTION is routed through an inverter to the pin 2 Data input of flip-flop IC6. The appropriate direction state is latched into the flip-flop at the arrival of the clock signal which is produced whenever a particular set of conditions is met: (1) A WRITE operation is not occurring; (2) the correct drive has been selected; and (3) a STEP pulse has been supplied. The not-Q output then controls the output of the exclusive OR-gate, IC14. The high or low supplied by IC14 provides an input to the 1-of-4 counter composed of 4 negative AND-gates within IC12 and IC15. The 1-of-4 counter essentially provides upcounting or downcounting depending on the selected direction for the head assembly movement. The direction of counting controls the routing of current to the A, B, C, and D coils of the stepper motor and thereby determines the head assembly motion.

The IC11 pin 13 Q-output provides a fixed amount of time that the stepper motor will remain on based on trigger signals provided by the STEP pulse. The stepper motor is disabled to save power whenever IC11 is not retriggered with steps.

Sensor Indications

The photosensors and LED's shown at A3 of the schematic provide for the detection of specific conditions of the drive operation. These conditions are provided to the Floppy Disk Controller through the J1 connector.

WRITE PROTECT is generated if a protection sticker has been placed over the write notch on the edge of the diskette. This physically blocks the passage of light to the photosensor, and results in a low signal being sent to exclusive OR-gate IC14. A high is outputted from the exclusive OR-gate which is then NANDed at IC1 to provide the active-low WRITE PROTECT to the Floppy Disk Controller.

The INDEX pulse is generated whenever the hole in the diskette rotates over the photosensor/LED combination. Besides the indication that is provided to the Floppy Disk Controller through the J1 connector, this signal is routed to IC9 and IC10 where it is converted to a READY indication for use by the Floppy Disk Controller.

The final indication to orient the Floppy Disk Controller to the disk drive activity is the TK00 signal which occurs when the head assembly is directly over the Track 0 position of the diskette.

Drive Selection

DRIVE SELECT signals are generated by the Floppy Disk Controller to activate the appropriate disk-drive unit according to jumper placement on each drives PC board.

For the drive configuration supplied within the Osborne Executive 1, the following illustration shows the correct placement of jumpers to relate the DRIVE SELECT 1 signal to Drive A and the DRIVE SELECT 2 signal to Drive B.

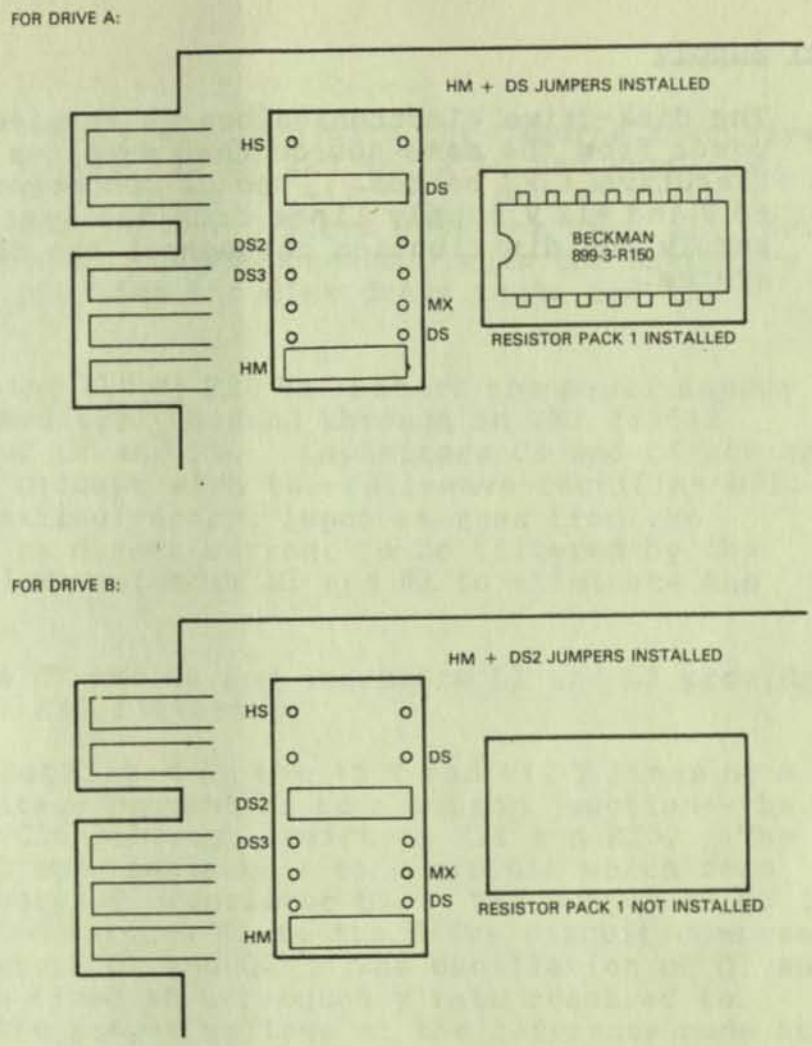


FIGURE C-26. JUMPER AND RESISTOR PACK CONFIGURATIONS

A resistor pack must also be supplied to terminate the interconnections for Drive A as illustrated in the diagram. Note also that the 'HM' jumper is in place on both drive boards.

Power Supply

The disk-drive electronics boards receive external power from the same source that supplies all of the Executive 1 PC boards. The J2 connector routes the +5 V and +12 V supply lines from the system power supply for distribution throughout the disk drive system.

POWER SUPPLY

The power supply provided with the Osborne Executive 1 accepts either 110 or 220 Volts AC and supplies regulated DC voltages of +12, -12, and +5 through frequency modulation. These voltages meet all the requirements of the components within the Executive including powering the disk drive units and the monitor.

The incoming 110 or 220 VAC enters the power supply and is immediately passed through an EMI filter composed of C1 and T1. Capacitors C5 and C6 act as a doubler circuit with the full-wave rectifier DB1. The alternating current input emerges from the rectifier as direct current to be filtered by the small series resistors R1 and R2 to eliminate the EMI.

Capacitors C7 and C8 and inductors L1 and L2 provide additional EMI filtering.

Power is regulated on the +5 V and +12 V lines by a sample voltage brought in to a common junction--the bottom of C16--through resistors R24 and R25. The sample voltage regulates a tank circuit which sets the frequency of transistor Q3. The output of Q3 is then coupled through T3 to the drive circuit composed of transistors Q1 and Q2. The oscillation of Q1 and Q2 is thus fixed at a frequency rate required to maintain the proper voltage at the reference node at the bottom of capacitor C16.

Overvoltage protection is provided by the silicon-controlled rectifier, SCR1, which turns on whenever the 5 V line exceeds the breakdown voltage of zener diode Z1 causing a base-emitter turn-on voltage at the cathode gate of SCR1. Thus, when the overvoltage limit is exceeded, SCR1 will clamp the +12 V supply to common. The excessive current draw at the primary of T2 will then blow the fuse F1.

By pulling down the entire secondary of T2 in this manner, the SCR protects the +5 V line. The shutdown current is routed through diode D6 and back around through D8 when the secondary is pulled down.

The drive circuit operates in basically a flyback mode. Diode D3 and capacitor C12 clamp any transients at the collector of the main drive transistor Q2. The complex clamping circuit composed of C11, R13, and D2 further prevents any transients from occurring on the collector of Q2.

POWER SUPPLY

The -12 V line is regulated by the negative 12 V regulator chip, IC1. The diode D12 ensures that if there is very light loading on the -12 V line, when the power supply turns off, reverse voltages will not damage the IC.

Similarly, D13 protects the IC against positive voltage appearing on the -12 V line. In such a case the positive voltage is clamped to ground.

VIDEO MONITOR

Video information supplied to the monitor electronics consists of three basic elements:

1. A serial bit pattern representing the video data for display on the monitor.

2. A vertical sync signal that, when converted to a ramp voltage, controls the deflection of the electron beam from the top of the video display to the bottom.

3. A horizontal sync signal that, when converted to a ramp voltage, controls the deflection of the electron beam from the left to the right side of the video display.

Video data enters at pin 8 and connects to the base of the video driver transistor, Q402. The input of the next stage, video output transistor Q401, has a very low impedance which results in very high frequency characteristics for Q402.

The output from the collector of Q401 connects to the grid of the CRT (VX201) where, depending on the state of the video data, the electron beam will either be allowed to pass through to the phosphor coating of the display screen (to excite and consequently illuminate the display), or the beam will be suppressed by the voltage present at the grid.

Vertical sweep is initiated by the vertical sync pulse entering the circuit at pin 9. The transistors Q301 and Q302 form the vertical oscillator circuit; they function as independent oscillators but are synchronized with the vertical sync signal.

The vertical sync signal is then directed to a vertical output driver. A number of transistors are used to provide high voltage to the vertical yoke--voltage increased from the +5 V level to a +12 V level. This ensures sufficient program current to drive the vertical yoke.

The vertical yoke current increases in a linear, ramp pattern to gradually deflect the electron beam from the top of the screen to the bottom of the screen. At the peak of the ramp, the beam must quickly flyback to its original position (this represents the vertical retrace interval) to begin the next sweep down the display screen.

The horizontal sync signal enters at pin 6 to be amplified by the Sync Amplifier, Q104. The sync signal then feeds the Horizontal Oscillator, IC 101, to provide a distinct synchronizing signal to the Horizontal Oscillator Transistor, Q101. Q101 drives Q102 to a Horizontal Drive transformer and finally connects to the Horizontal Output transistor, Q103. Ultimately the sync signal drives the sweep transformer, TX102, to produce current through the Horizontal Yoke.

The Horizontal Yoke moves the beam from left to right and then quickly sweeps back across the screen. Additionally, the Horizontal Driver output circuit provides voltage to the sweep transformer sufficient that the 10 to 12 kilovolts necessary to accelerate the electrons in the CRT tube can be developed from the transformer output.

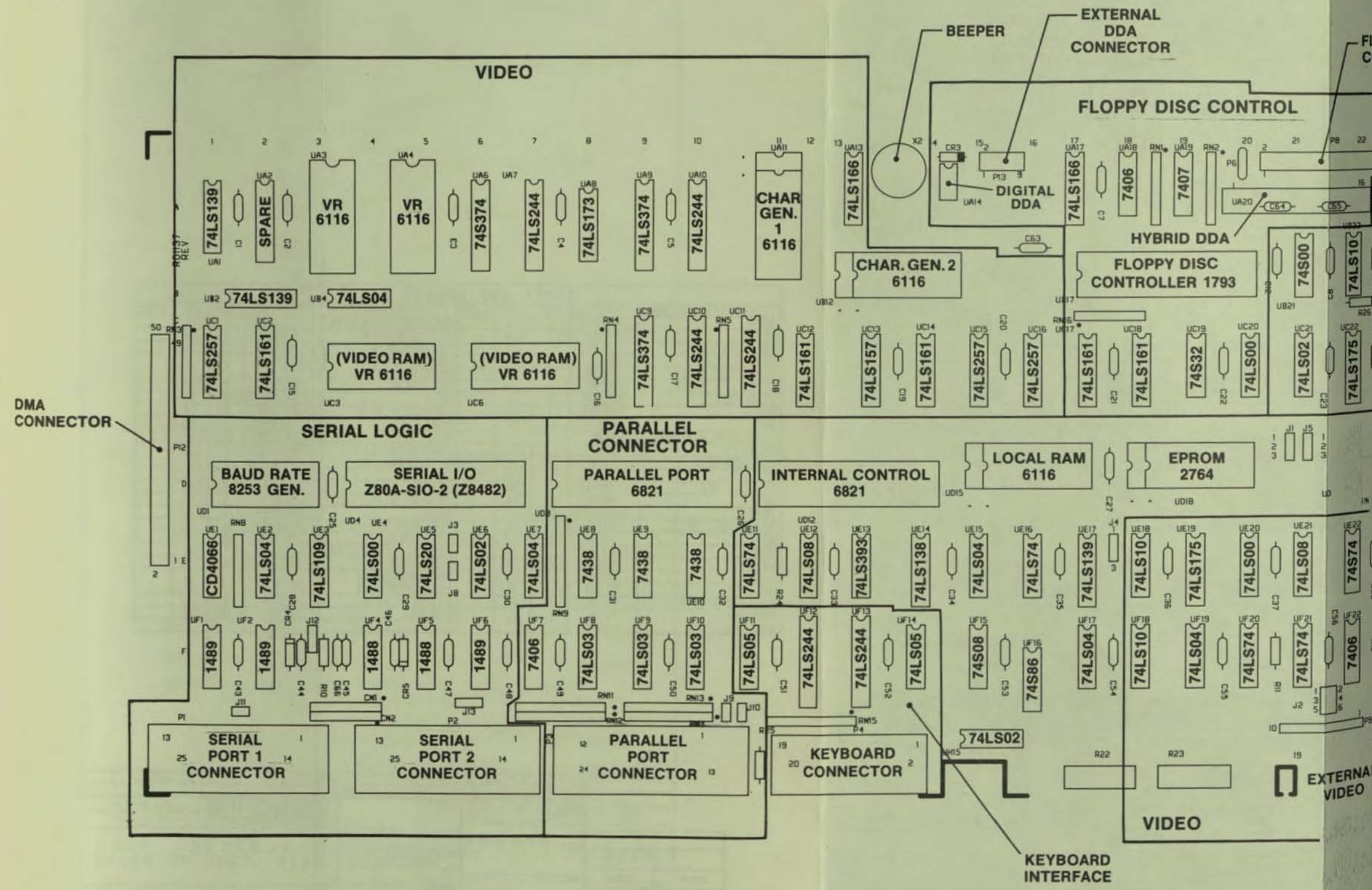
The sweep transformer has three essential functions:

1. It provides the +50 V signal used in the internal video driver circuitry.

2. It develops the +12.5 kilovolt signal to the face of the CRT for accelerating the electrons.

3. It provides the linear yoke current to sweep the beam in a linear pattern across the screen.

EXECUTIVE 1 MAIN PCB



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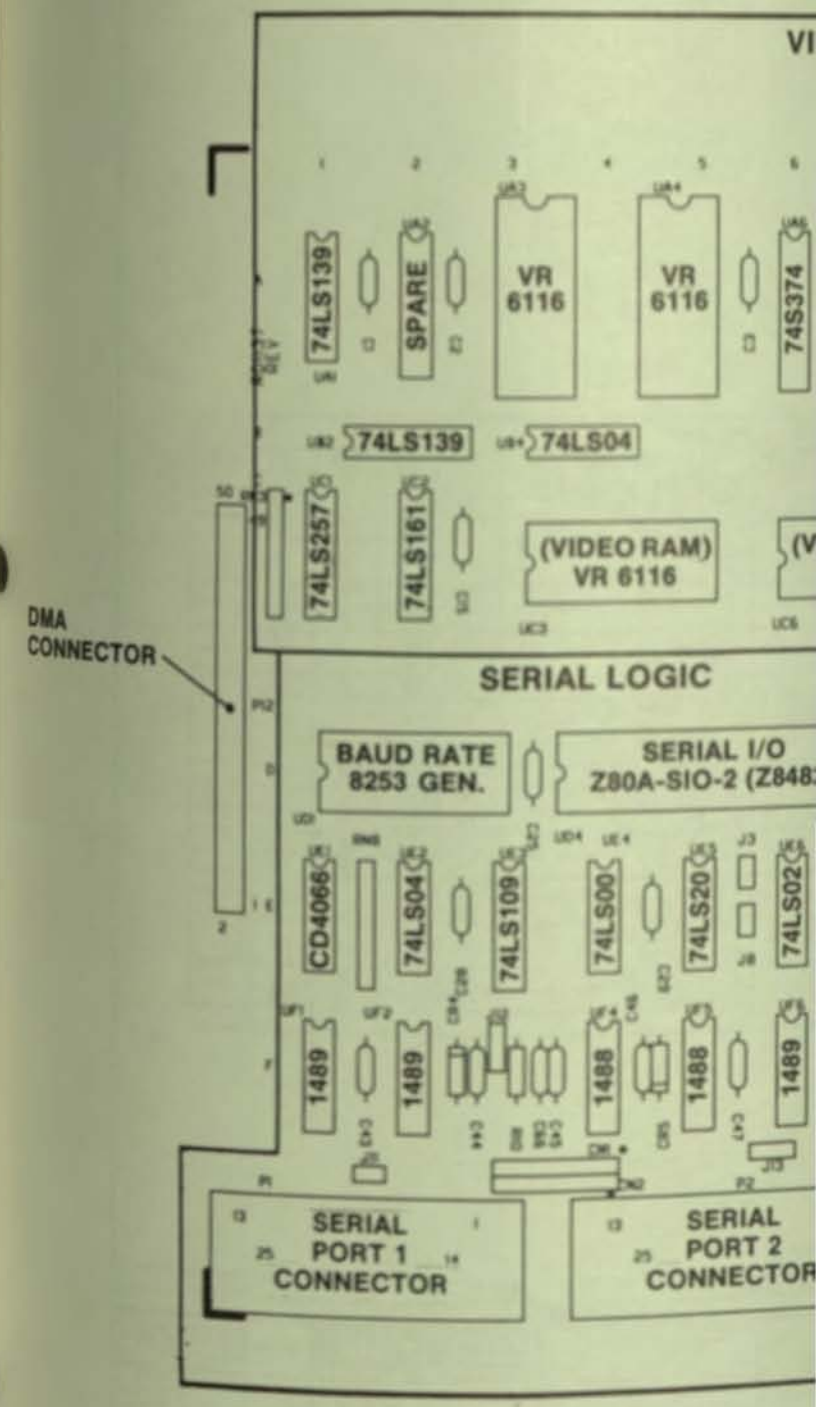
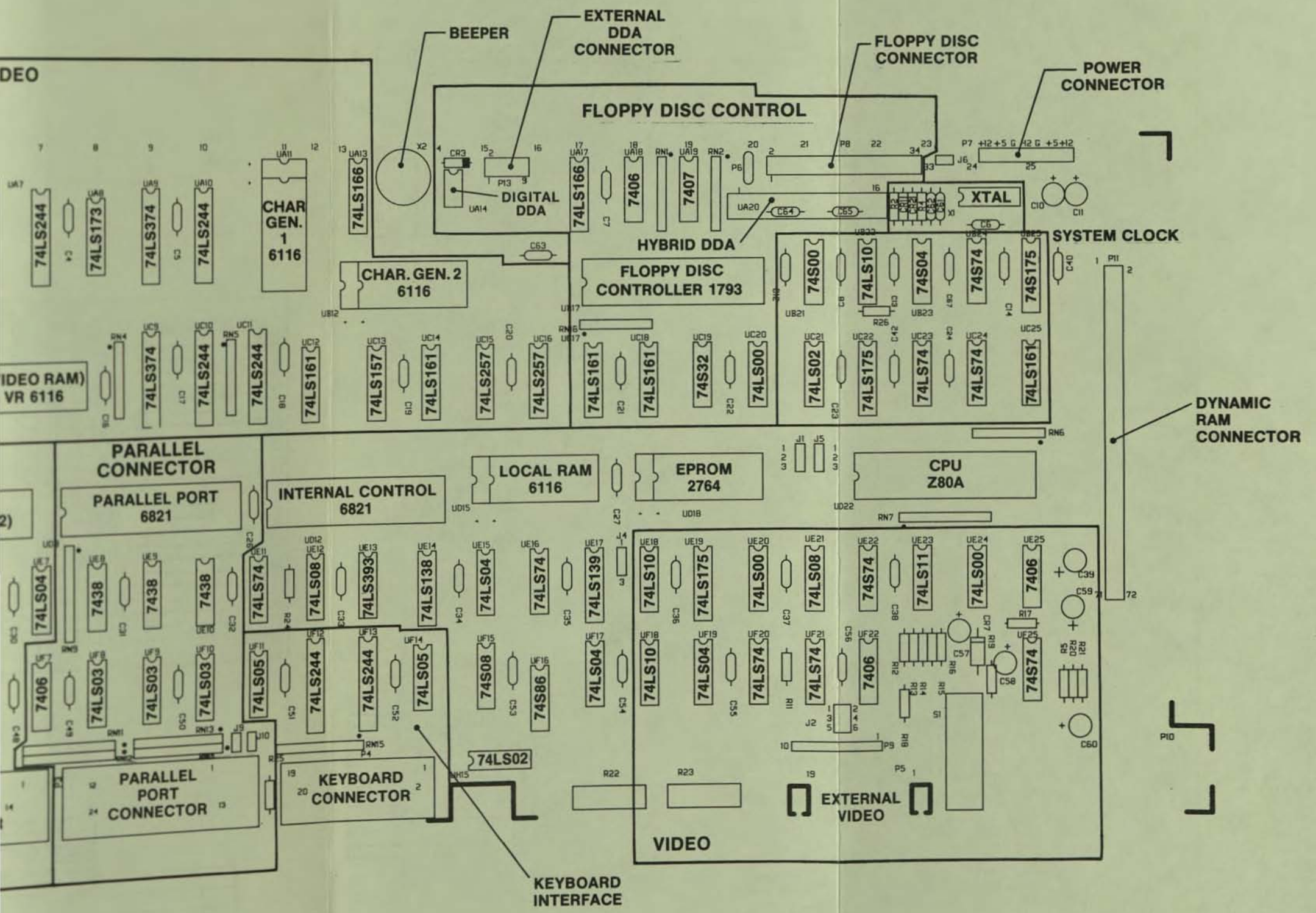


EXECUTIVE 1 MAIN PCB



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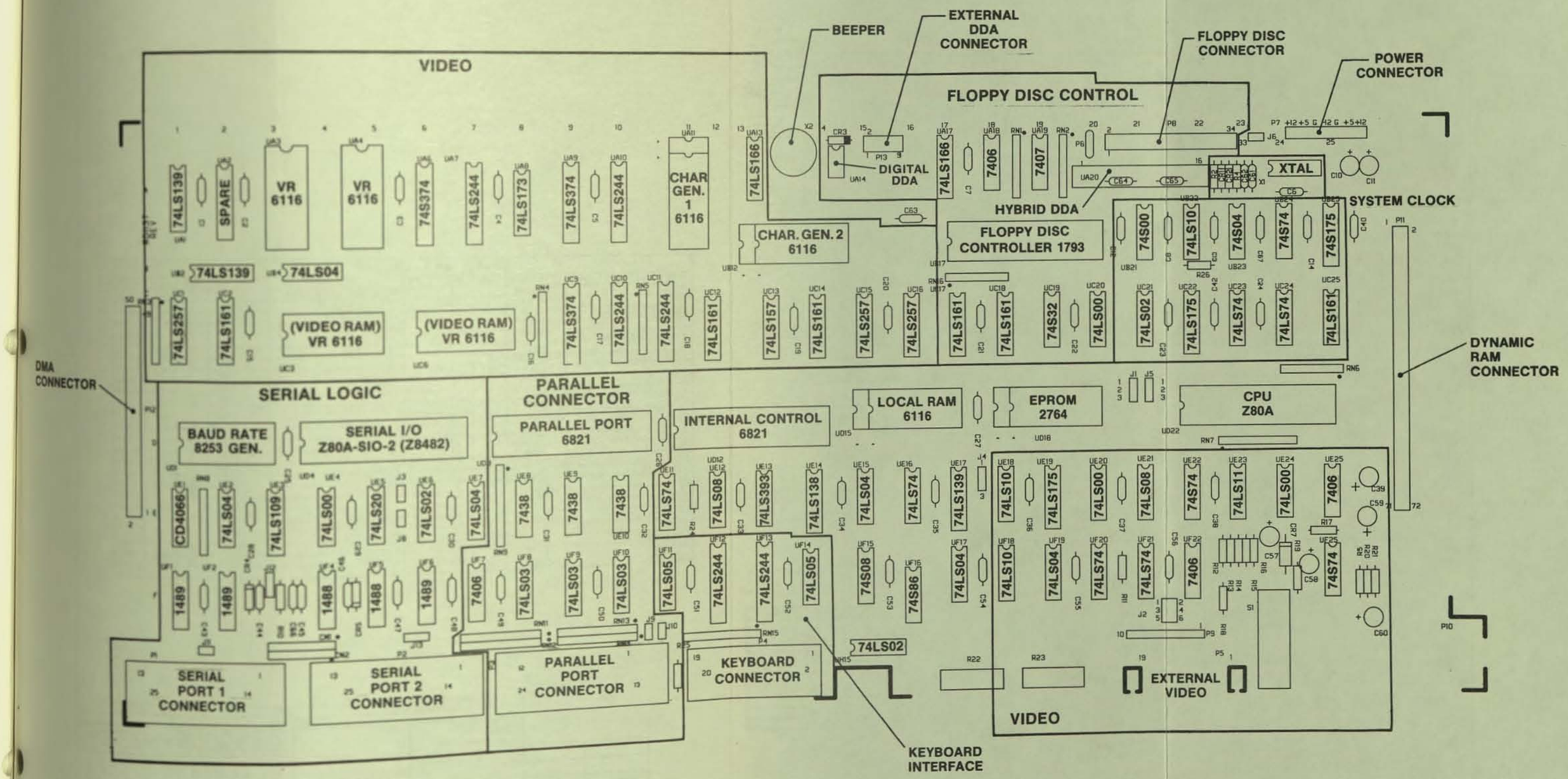
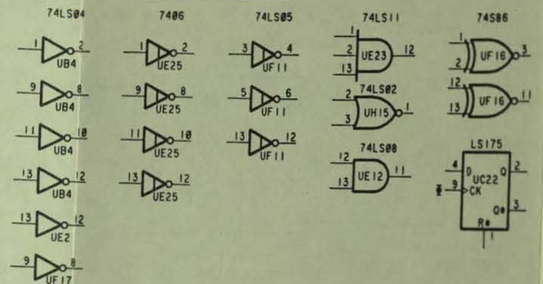
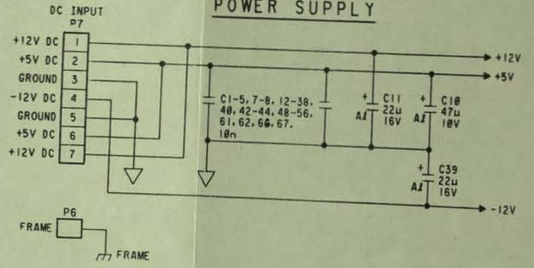


SPARE GATES



POWER SUPPLY



NOTES: UNLESS OTHERWISE SPECIFIED.

1. ALL RESISTANCE VALUES ARE IN OHMS. 1/4W. 5%.
2. ALL RESISTORS 4.7K.
3. ALL CAPACITANCE VALUES IN FARADS.
4. RAMS MUST OPERATE WITH WRITE PULSE WIDTH OF 125 NS.
5. IF UA20 IS USED, OMIT UA14.
6. LOCATIONAL CODING FOR SHEET TO SHEET CONNECTIONS:
   - INDICATES SHEET NO.
   - 8C6
   - INDICATES ZONE ON THE SHEET.

7. THIS TRACE DOES NOT APPREAR ON BOARD. CONNECTION MUST BE COMPLETED USING JUMPER WIRE.
8. THIS TRACE MAY NOT BE ON SOME BOARDS. IF IT IS, CUT IT. OTHERWISE IGNORE THIS NOTE.

REFERENCE DESIGNATION	
LAST	NOT USED
C68	C9, C41
CN2	—
CR7	CR6
J13	J7
P13	P6
R26	R1, R3, R6-9, R17
RN16	RN10
S1	—
X2	—

REV	DESCRIPTION	DATE	APPROVED
6	REVISED AND REDRAWN		
7	ADDED REWORK		
7	PRE PROD REL ECO #552		
8	CHANGE REF DESIG ECO #581		
9	ADD CIRCUIT BETWEEN UB25 AND UF25 ECO #587		
10	CHANGE R18 VALUE ECO #603		

POWER AND GROUND TABLE

REF. DESIGNATION	TYPE NO.	GND	+5V	+12V	REF. DESIGNATION	TYPE NO.	GND	+5V	+12V
UE13	74LS393	7	14		UC20, UC4, UC20, UC24	74LS00	7	14	
UB23	74S04	7	14		UC21, UC6, UH15	74LS02	7	14	
UB21, UE21, UF15	74S08	7	14		UF8, UF9, UF10	74LS03	7	14	
UC19	74S32	7	14		UB4, UE2, UE7,				
UB24, UE22, UF25	74S74	7	14		UE15, UF17, UF19	74LS04	7	14	
UF16	74S86	7	14		UF11, UF14	74LS05	7	14	
UC18, UC25	74S161	8	16		UE12	74LS08	7	14	
UB25	74S175	8	16		UB22, UC19, UF18	74LS10	7	14	
UA6	74S374	10	20		UE23	74LS11	7	14	
UA18, UE25, UF7, UF22	7406	7	14		UE5	74LS20	7	14	
UA19	7407	7	14		UC23, UC24, UE11,				
UE8, UE9, UE18	7438	7	14		UE16, UF20, UF21	74LS74	7	14	
UF4, UF5	1489	7			UE3	74LS109	8	16	
UF1, UF2, UF6	1489A	7			UE14	74LS138	8	16	
UE1	4066	7	14		UA1, UB2, UE17	74LS139	8	16	
UD22	Z80A-CPU	29	11		UC13	74LS157	8	16	
UD8, UD12	6821	1	20		UC2, UC12, UC14, UC17	74LS161	8	16	
UB17	1793	20	21	40	UA13, UA17	74LS166	8	16	
UD4	Z80A-SIO	51	9		UA8	74LS175	8	16	
UD18	2764	14	28		UC22, UC19	74LS175	8	16	
UD1	8253	12	24		UA7, UA18, UC18,				
UA14	92168	4	8		UC11, UF12, UF13	74LS244	10	20	
UA11, UB12, UD15	6116	14	28		UC15, UC16	74LS257	8	16	
UA3, UA4, UC3, UC6	6116 LP2	12	24		UA9, UC9	74LS374	10	20	

1K00073	OCC-2		
NEXT ASSY	USED ON		
APPLICATION			

DO NOT SCALE DRAWING

3/83

OSBORNE COMPUTER CORPORATION

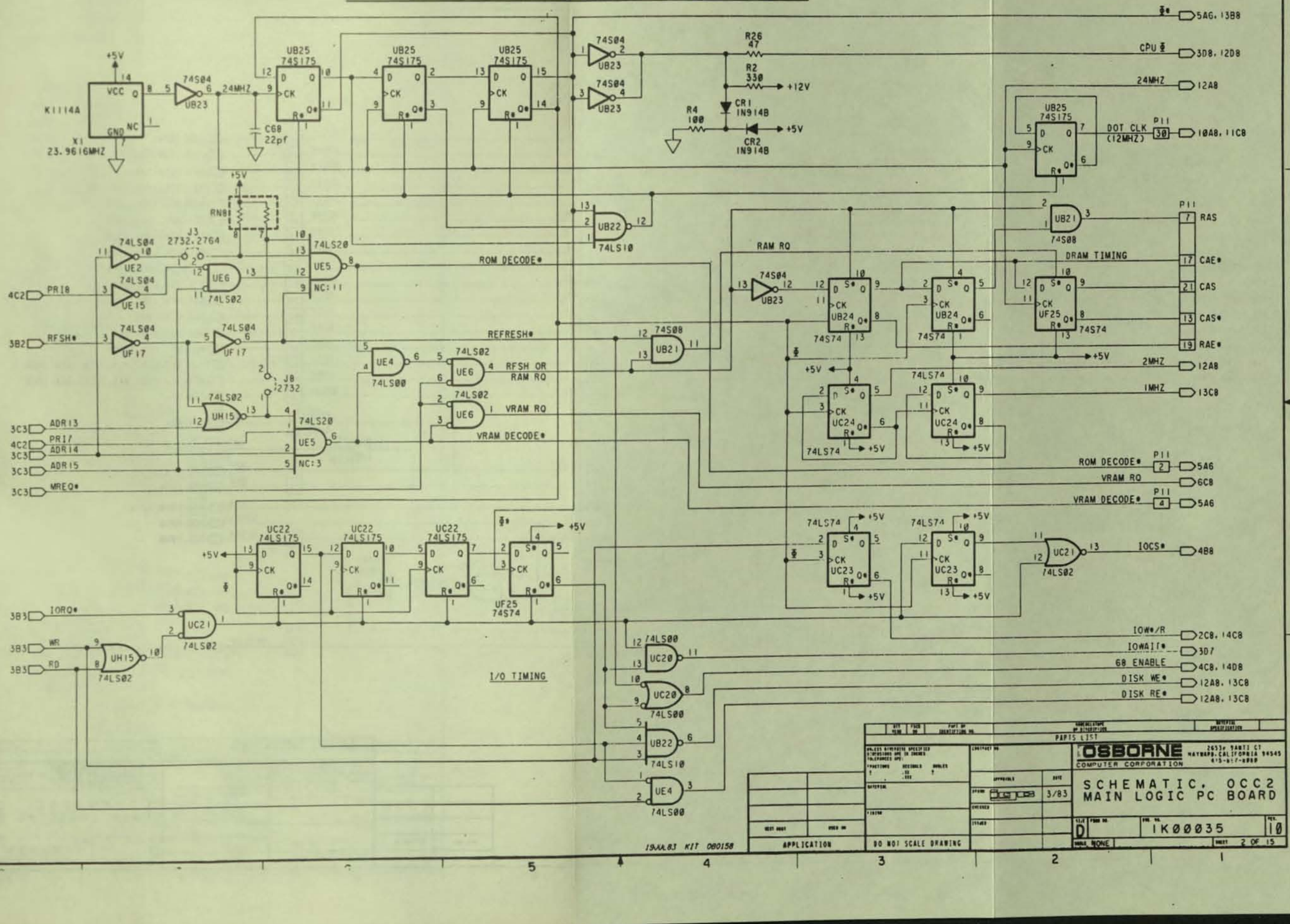
SCHEMATIC, OCC2
MAIN LOGIC PC BOARD

D | IK00035 | 10

SCALE: NONE | SHEET 1 OF 15

BOARD KIT 000157

OSCILLATOR, CPU, MEMORY AND I/O TIMING



IK00035	SH 2	REV 10
REVISIONS		
ZONE	REV.	DESCRIPTION — SEE SHEET ONE

PARTS LIST

OSBORNE COMPUTER CORPORATION
2653-A BANTI CT
HAYWARD, CALIFORNIA 94545
415-657-0990

SCHEMATIC, OCC2
MAIN LOGIC PC BOARD

SIZE	DWG NO	REV
D	IK00035	10

SCALE NONE — SHEET 2 OF 15

APPLICATION	DO NOT SCALE DRAWING

3/83

19MAR83 KIT 080158

CPU. RESET

1K0035	3	10	
		SEE SHEET ONE	

RN6 33 +5V

RN7 33 +5V

3C2, 12A1, 14C8 IRQ*
1C2 CPU Φ
2B2 IO WAIT*
6D1 VRAM WAIT*

74S08 UB21

4C8, 12D8, 13C8, 14C8 DATA7
DATA6
DATA5
DATA4
DATA3
DATA2
DATA1
DATA0

UD22 Z80A CPU

BUSRQ* HALT* NC
NMI* BUSAK* NC
INT*
Φ
WAIT*
RST*
MREQ*
WR*
RD*
M1*
IORQ*
RFSH*
A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
D7 D6 D5 D4 D3 D2 D1 D0

P11

ADR15 ADR14 ADR13 ADR12 ADR11 ADR10 ADR9 ADR8 ADR7 ADR6 ADR5 ADR4 ADR3 ADR2 ADR1 ADR0

2B8, 15D8
2B8, 15D8, 5A6
5D7, 15D8, 5A6
5D7, 9C8, 15D8, 5A6, 6B8
5D7, 8D8, 10B8, 15C8
5D7, 8D8, 10B8, 15C8
5D7, 8D8, 10B8, 15C8
5D7, 8D8, 10B8, 15C8
4C8, 5D7, 8C8, 10B8
5D7, 8C8, 10B8
5D7, 8C8, 10B8
4C8, 5D7, 8C8, 10C8
4C8, 5D7, 8C8, 10C8
4C8, 5D7, 8C8, 10C8, 12C8, 13C8, 14C8
4C8, 5D7, 8C8, 10C8, 12C8, 13C8, 14C8
2B8, 5A6

UF15 74LS04
2B8, 6C8
2B8, 6C8

5A6
5A5, 12C8
9C8, 13C8, 12C8
2B8, 12C8
2C8, 10A8

9D1 TDATA7 TDATA6 TDATA5 TDATA4 TDATA3 TDATA2 TDATA1 TDATA0

RN5 33
RN4 33

UF11 74LS05
PR IRQ

+5V C57 47µ 10V A1
CR7 IN4001

UF6 1489A

RESET

S1 RESET
R19 2.2K
C58 4.7µ A1

UF1 1489A

PB LATCH

UF21 UF20 UF20 74LS74 74LS74 74LS74

+5V 64US

DRAM SYNC

74LS02 UC21
UA18 7406
10 INT 4CK 5

UF19 74LS04

P12 36 RESET* 4C8, 11B8, 12B8, 13C8, 14C8

6B2 HSYNC (64US)

PARTS LIST

OSBORNE COMPUTER CORPORATION

SCHEMATIC, OCC2
MAIN LOGIC PC BOARD

D | 1K0035 | 10

SHEET 5 OF 15

APPLICATION

DO NOT SCALE DRAWING

3/83

1K0035 KIT 080159

MEMORY BANK CONTROL

DWG NO	IK00035	SH 4	REV. 10

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET ONE		

12B1 MODEM DSR*
12B1 MODEM RI*
7D1 VBLANK (RTC IRQ)

3C8 DATA7 26
3C8 DATA6 27
3C8 DATA5 28
3C8 DATA4 29
3C8 DATA3 30
3C8 DATA2 31
3C8 DATA1 32
3C8 DATA0 33

3C2 ADR1 35
3C2 ADR0 36

2B2 65 ENABLE 25
2B2 IOW*/R 21
3A2 RESET* 34

UD12 6821 PIA
PORTS 02.03

D7 D6 D5 D4 D3 D2 D1 D0 RS1 RS0 E R/W* RESET*
CB1 18
CB2 19
PB7 17
PB6 16
PB5 15
PB4 14
PB3 13
PB2 12
PB1 11
PB0 10
CA1 40
CA2 39
IRQA* 38
IRQB* 37

60*/50 7C8
TXC SEL 12D8
RXC SEL 12D8
OSEL2* 13A8
OSEL1* 13A8
DDEN* 13C8

+5V
RN3
UF7 7406
CR3 IN914B
X2 AUDIO TRANSDUCER

DMA IRQ* P12 44
KBD STB 15A8
IRQ* 3D6

(ROM BANK ENA) PRI8 2C8
(VRAM BANK ENA) PRI7 2C8
(BANK6ENA) 66 PRI6
(BANK5ENA) 65 PRI5
(BANK4ENA) 64 PRI4
(BANK3ENA) 63 PRI3
(BANK2ENA) 62 PRI2
(BANK1ENA) 61 PRI1
P11

PORTS 00.01 (40.41)
PA7 PA6 PA5 PA4 PA3 PA2 PA1 PA0 CS0 CS1 CS2*
9 8 7 6 5 4 3 2 22 24 23

+5V

I/O DECODER

UE14 74LS138
E E* E* C B A Y7* Y6* Y5* Y4* Y3* Y2* Y1* Y0*

2B1 IOCS*
3C3 ADR7
3C3 ADR4
3C3 ADR3
3C3 ADR2

7 9 10 11 12 13 14 15
SYS SEL

(18-1B)
(14-17)
(10-13)
(08-0B)
(04-07)

VID ENA* 11B8
RTC SEL* 11A7
KBD SEL* 15B7
488 SEL* 14D8
FDC SEL* 13C8
CTC SEL* 12B8
SIO SEL* 12C8

74LS02 UH15
74LS11 UE23
UF19 74LS04

(0C-0F)

19JAN83 KIT 080160

APPLICATION

DO NOT SCALE DRAWING

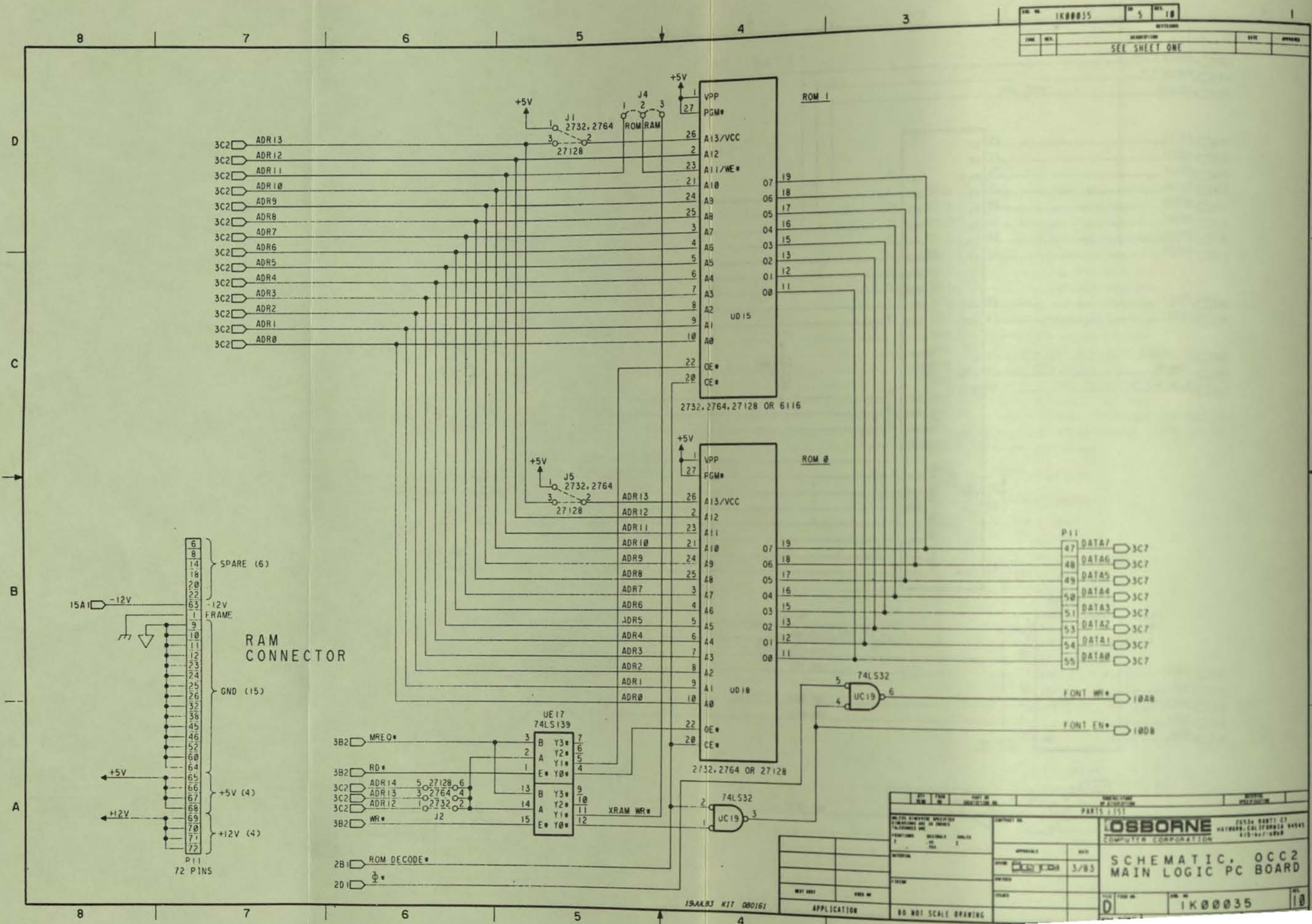
PARTS LIST

OSBORNE COMPUTER CORPORATION
2953e BAYTI CT. HAYWARD, CALIFORNIA 94545 415-8x7-x8x8

APPROVALS	DATE
DRAWN	3/83
CHECKED	
ISSUED	

SCHEMATIC, OCC2
MAIN LOGIC PC BOARD

SIZE D | FSCM NO | DWG NO IK00035 | REV 10
SCALE NONE | SHEET 4 OF 15


SEE SHEET ONE
ROM 1
ROM 0
+5V
J1
2732,2764
27128
J4
ROM RAM
J5
J2
VPP
PGM*
A13/VCC
A12
A11/WE*
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
OE*
CE*
O7
O6
O5
O4
O3
O2
O1
O0
UD15
UD18
2732,2764,27128 OR 6116
2732,2764 OR 27128
ADR13
ADR12
ADR11
ADR10
ADR9
ADR8
ADR7
ADR6
ADR5
ADR4
ADR3
ADR2
ADR1
ADR0
3C2
UE17
74LS139
MREQ*
RD*
WR*
ADR14
XRAM WR*
74LS32
UC19
FONT WR*
FONT EN*
P11
DATA7
DATA6
DATA5
DATA4
DATA3
DATA2
DATA1
DATA0
3C7
SPARE (6)
-12V
FRAME
GND (15)
+5V (4)
+12V (4)
15A1
RAM
CONNECTOR
72 PINS
ROM DECODE*
Φ*
2B1
2D1
PARTS LIST
OSBORNE
COMPUTER CORPORATION
SCHEMATIC, OCC2
MAIN LOGIC PC BOARD
IK00035
APPLICATION
DO NOT SCALE DRAWING
19AUG83 KIT 080161

VIDEO RAM TIMING

DWG. NO.	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET ONE		

VRAM SEL → 8D8
CHAR CLK* [32] P12 → 7D8, 10D8, 11C8

+5V, RN3

74S161 (UC18): PD, PC, PB, PA, LD*, R*, CK, ET, EP, TC, QD, QC, QB, QA

74LS04 UF17 → UB22 (74LS10) → SR LOAD* → 10A8

DMA INH P12 [28]

UB21 (74LS08) → 74LS04 UE15 → UE20 (74LS00) → 74LS04 UF19

UF18 (74LS10) → UE20 (74LS00) → UC20 (74LS00)

+5V, 74LS74 UE16 (S*, D, CK, Q*, R*)

8A1 P12 [40] DMA GO*

2B1 VRAM RQ

3B3 RD
3B3 DOT CLK*
3B3 WR

UC20 (74LS10) → VRAM LATCH* → 9C8

UE18 (74LS10) → VRAM WR* → 9B8

VRAM WAIT* P12 [34]
VRAM RD* → 9D8

UE11 (74LS74): S*, D, CK, Q*, R*, +5V

UE20 (74LS00) → VRAM DOUT* → 9D8

VRAM CPU SEL*

UB4 74LS04 → UE18 (74LS10) → 74LS139

74LS139: B, A, E*, UA1, UB2, Y3*, Y2*, Y1*, Y0*

VRAM CEH1* → 9A8
VRAM CEH0* → 9A8

VRAM CEL1* → 9A8
VRAM CEL0* → 9A8

VRAM H DOUT* → 9C8
VRAM H DIN* → 9D8

3C7 ADR 12

RN3 8 1 +5V

8A1 DMA EN*
8D1 VMA 11

9A1 BK WR EN*

19AA.83 KIT 080162

PARTS LIST

APPLICATION | DO NOT SCALE DRAWING

OSBORNE COMPUTER CORPORATION
26538 BARTI CT
HAYWARD, CALIFORNIA 94545
415-887-8080

SCHEMATIC, OCC2
MAIN LOGIC PC BOARD

SIZE	FSCM NO.	DWG. NO.	REV.
D		IK00035	10

SCALE NONE | SHEET 6 OF 15

DWG. NO.	IK00035	SH. 7	REV. 10
ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET ONE		

VIDEO TIMING

CHAR CLK* 6D1
VLOAD*
4D2 60*/50
74LS04 UE21
74LS161 UC2 (TC, PD, PC, PB, PA, LD*, R*, CK, ET, EP; QD, QC, QB, QA)
TXADR4 TXADR3 TXADR2 TXADR1
UE12 74LS08
UF18 74LS10
+5V
UE3 74LS109 (J, S*, CK, K*, R*, Q*)
VBLANK* 11C8
VBLANK 4D8
UE21 74LS08
VSYNC 11B1
UF21 74LS74 (D, S*, CK, R*, Q*)
74LS04 UE7
UE4 74LS00
TXADR0
TXADR4 8D8
TXADR3 8D8
TXADR2 8D8
TXADR1 8D8
TXADR0 8D8
74LS04 UE15
74LS08 UF15
74LS161 UC12
SCAN3 10C8, 11D8
SCAN2 10C8
SCAN1 10C8
SCAN0 10C8, 11D8
HLOAD*
UF18 74LS10
UE19 74LS175 (D, CK, R*, Q)
UA6 74LS374 (D, CK, OE*, Q)
UE16 74LS74 (D, S*, CK, R*, Q*)
HSYNC* 11B8
HSYNC 11C8
74LS161 UC14
74LS04 UE15
HBLANK* 11C8
HBLANK
CHADR6 8C8
CHADR5 8C8
CHADR4 8C8
CHAR CLK*
74LS161 UC17
CHADR3 8C8
CHADR2 8C8
CHADR1 8C8
CHADR0 8C8

19JUL83 KIT 080163

APPLICATION

DO NOT SCALE DRAWING

PARTS LIST

OSBORNE COMPUTER CORPORATION 2453 - 26TH ST. HAYWARD, CALIFORNIA 94545 415/786-8080

SCHEMATIC, OCC2
MAIN LOGIC PC BOARD

3/83

D | IK00035 | 10

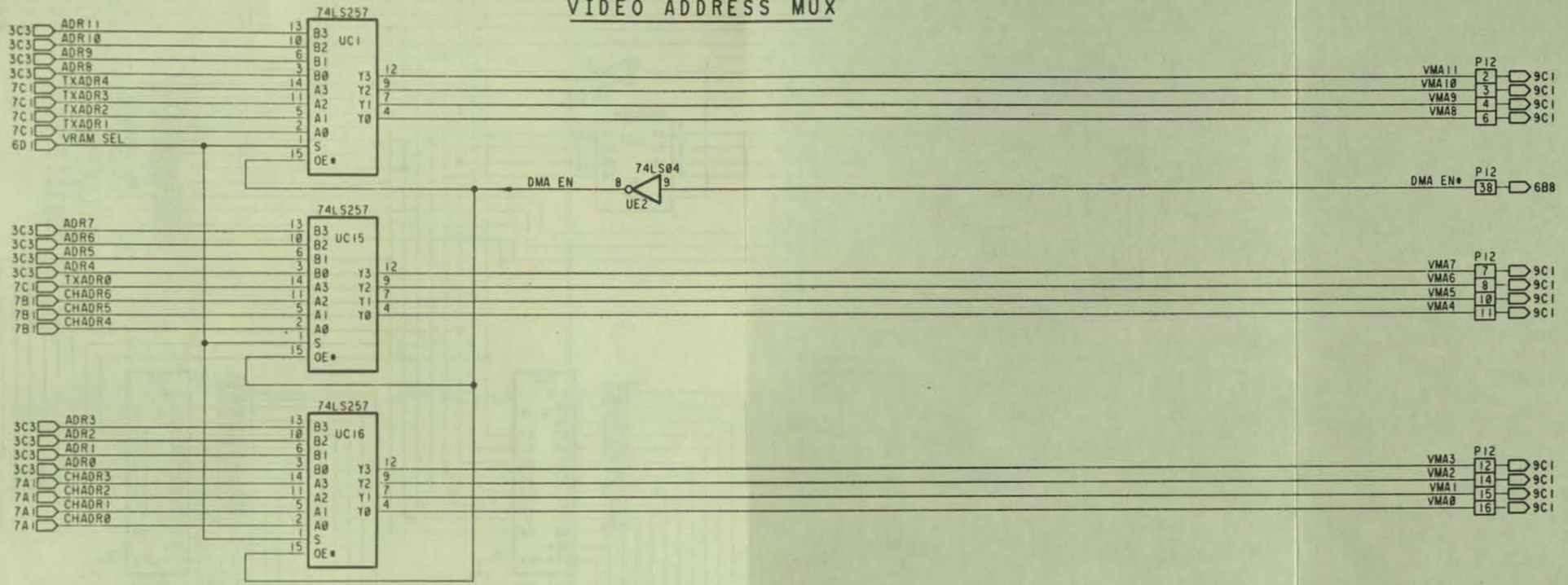
NONE | SHEET 7 OF 15

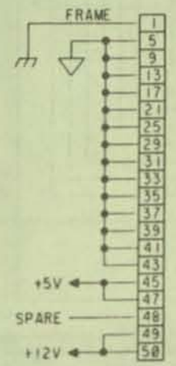
DWG. NO.	SIZE	REV.
1K00035	D	10

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET ONE		

VIDEO ADDRESS MUX





DMA

NEXT ASSY	USED ON
APPLICATION	

DO NOT SCALE DRAWING

PARTS LIST

OSBORNE COMPUTER CORPORATION
2653a BANTI CT
HAYWARD, CALIFORNIA 94545
415-xxx-xxxx

APPROVALS	DATE	
DRAWN	3/83	
CHECKED		
ISSUED		

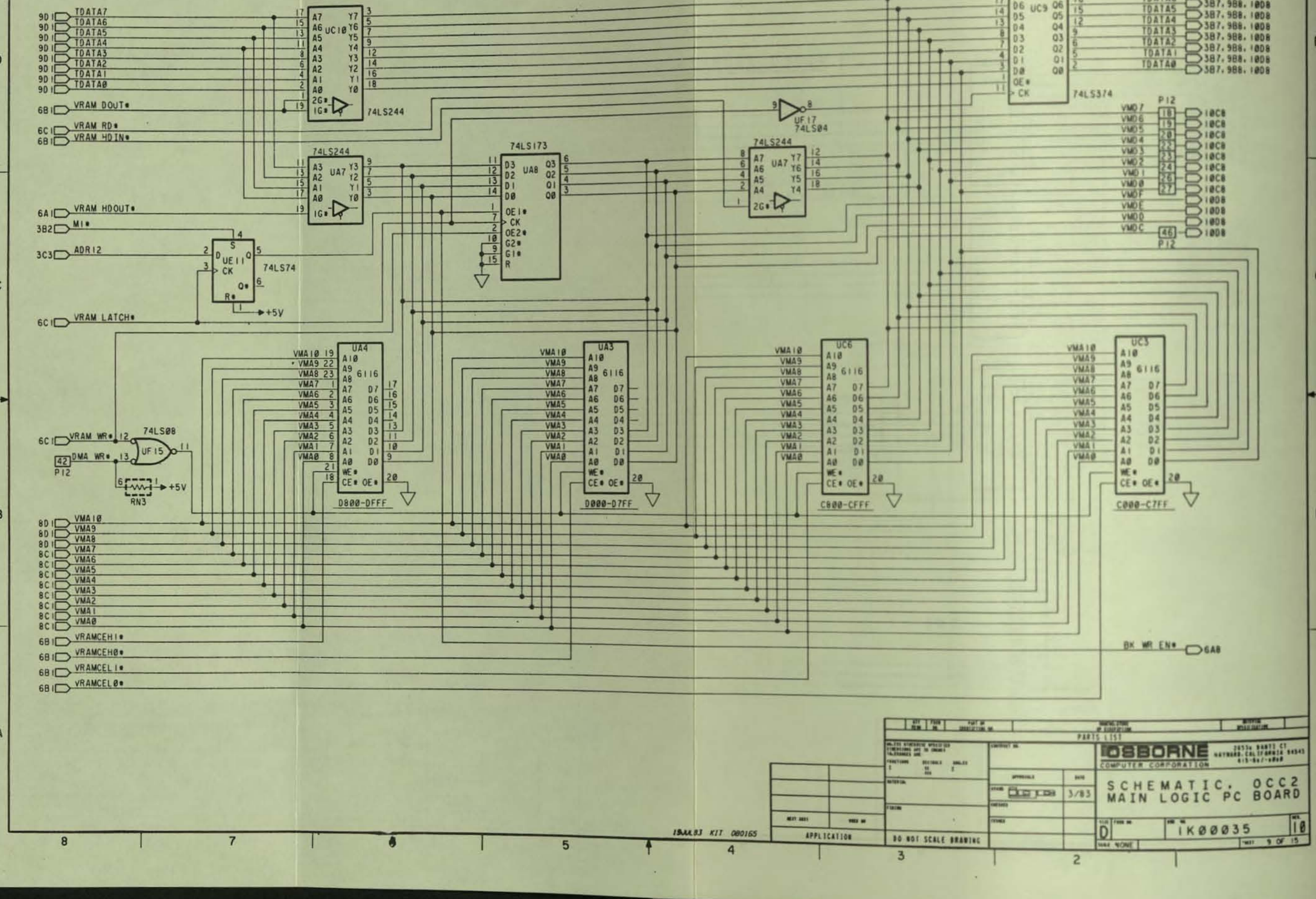
SCHEMATIC, OCC2
MAIN LOGIC PC BOARD

SIZE	FSCM NO.	DWG. NO.	REV.
D		1K00035	10

SCALE NONE — SHEET 8 OF 15

19AUG83 KIT 080164

VIDEO RAM



APPLICATION

DO NOT SCALE DRAWING

PARTS LIST

OSBORNE COMPUTER CORPORATION

SCHEMATIC, OCC2
MAIN LOGIC PC BOARD

SIZE D	FSCM NO.	DWG NO. 1K00035	REV. 10
SCALE NONE		SHEET 9 OF 15	

1983 KIT 000165

FONT RAM

IK00035	10	10	
SEE SHEET ONE			

VMDF VMDE VMDD VMDC CHAR CLK* → 74LS374 UA6
HALF INTENSITY* → 11C8
UNDERLINE → 11D8
BLINK → 11D8
INV VID → 11D8
74LS175 UE19
R24 10K → +5V
74LS08 UE12
UE7 7406
74LS244 UA10
FONT EN*
TDATA0 TDATA1 TDATA2 TDATA3 TDATA4 TDATA5 TDATA6 TDATA7
74LS157 UC13
SCAN3 SCAN2 SCAN1 SCAN0 ADR3 ADR2 ADR1 ADR0
VMD7 VMD6 VMD5 VMD4 VMD3 VMD2 VMD1 VMD0
74LS374 UA9
(SEE NOTE 4)
6116 UB12
6116 UA11
2K X 8 RAM
+5V
PGM
OE* CE* WE* WE*/A11
74LS166 UA13
VIDEO → 11D8
QH A B C D E F G H R* LD*/SH CK CKB* SI
UE17 74LS04
UE15 74LS04
ADR11 ADR10 ADR9 ADR8 ADR7 ADR6 ADR5 ADR4
74LS244 UC11
2G* 1G*
SR RESET*
FONT WR*
SR LOAD*
DOT CLK
RFSH*
74LS08 UE12
74S04 UB23
UE24 74LS00

19AA83 KIT 080166

APPLICATION	DO NOT SCALE DRAWING	PARTS LIST	

OSBORNE COMPUTER CORPORATION
2453A BANTI CT. HAYWARD, CALIFORNIA 94545 415-887-8080

SCHEMATIC, OCC2
MAIN LOGIC PC BOARD

SIZE	FSCM NO.	DWG NO.	REV.
D		IK00035	10

SCALE NONE SHEET 10 OF 15

VIDEO AND SYNC OUTPUT

UNDERLINE
SCAN0
SCAN3
VIDEO
INV VID
BLINK
HBLANK*
VBLANK*
CHAR CLK*
DOT CLK
HALF INTENSITY*
HSYNC
VSYNC
HSYNC*
VID ENA*
RESET*
RTC SEL*
BLINK RATE
CBLANK*
(SYNC)
(VIDEO)
(DIM)
+5V
+12V VIDEO
CONTRAST
BRIGHTNESS
FRAME
COMPOSITE VIDEO OUT
EXTERNAL MONITOR
INTERNAL MONITOR
VERT SYNC
HORIZ SYNC
VIDEO (↑WHT)
BRIGHTNESS
+12V
GND
GND
FRAME
DATA7
DATA6
DATA5
DATA4
DATA3
DATA2
DATA1
DATA0

74LS11 UE23
74LS32 UC19
74LS32 UC19
74LS08 UE21
74S86 UF16
74LS08 UE21
74LS00 UE4
74LS08 UE21
74LS08 UF15
74LS08 UE21
74LS175 UE19
74LS175 UE19
74LS74 UE22
74LS74 UE22
74S86 UF16
UF22 7406
7406
7406
UF22
UF7 7406
7406
7406
7406
UF22
74LS00 UE24
74LS00 UE24
74LS393 UE13
74LS244 UF13

C59 47µ 10V
R5 47
R20 100
R21 100
R16 100
R15 100
C60 47µ 10V
P10
R11 1K
R13.220
R14.47
R12.470
R18 910
R23 500
R22 100K
CW

REAL TIME CLOCK OVERFLOW

19.NOV.83 KIT 000167

PARTS LIST

OSBORNE COMPUTER CORPORATION
2453A BANTI CT HAYWARD, CALIFORNIA 94545 415-667-xxxx

SCHEMATIC, OCC2
MAIN LOGIC PC BOARD

3/83

APPLICATION

DO NOT SCALE DRAWING

D
IK00035
10

SHEET 13 OF 15

SERIAL I/O

REV	DESCRIPTION	DATE	APPROVED
	SEE SHEET ONE		

IK00035 — SH 12 — REV 10

TXC SEL
RXC SEL

DATA7
DATA6
DATA5
DATA4
DATA3
DATA2
DATA1
DATA0
CPUΦ
RESET*
MI*
IORQ*
RD*
ADR1
ADR0
SIO SEL*

UD4 — PORTS 0C-0F Z80A SIO/2

TXDA
RXDA
RTSA*
CTSA*
DCDA*
TXCA*
SYNCA*
RXCA*
DTRA*
RXCB*
TXCB*
RXDB*
TXDB*
DCDB*
RTSB*
DTRB*
CTSB*
INT*
IEO
W*/RDYA*
W*/RDYB*
IEI

UD1 — PORTS 04-07 8253 — COUNTER/TIMER

OUT0
OUT1
OUT2
A1
A0
CS*
GATE0
GATE1
GATE2
CK0
CK1
CK2
RD*
WR*

COMM CLK B
COMM CLK A
CTC SEL*
2MHZ
DISK RE*
DISK WE*
24MHZ

UB23 — 74S04 — UC25 ÷13 — 74S161

+12V SIO
+5V
-12V SIO
C63 10n
C45 10n
C47 10n
C46 10n
RN8
4066
UE1
UE2 74LS04
UF1 1489A
UF2 1489A
UF4 1488
UF5 1488
UF6 1489A
CN1 390p
CN2 390p
R10 22
J11
J12
J13

TO MODEM OR DCE
P1 DB25S
TXD
RXD
RTS
CTS
DSR
DCD
+V
TXCLK
RXCLK
DTR
TXCLK
RI
MODEM RI*
MODEM DSR*
CR5 IN4001 -12V
CR4 IN4001 +12V
P2 DB25S
TO PRINTER OR DTE
IRQ*
SPINDLE CLK

19AA.83 KIT 080168

PARTS LIST

OSBORNE COMPUTER CORPORATION
2453a DANTI CT. HAYWARD, CALIFORNIA 94545 415-ba7-a8a8

SCHEMATIC. OCC2
MAIN LOGIC PC BOARD

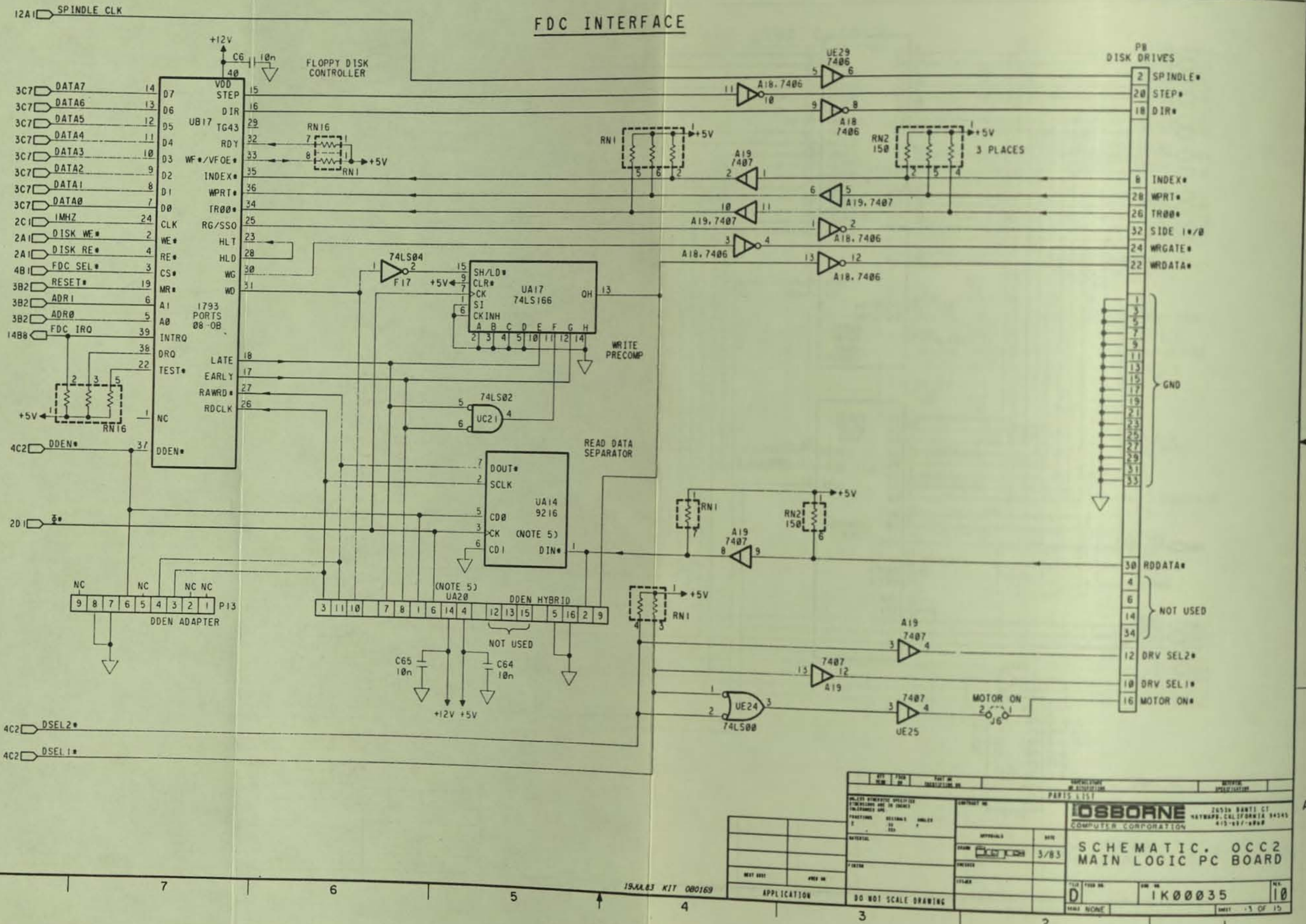
SIZE	FSCM NO	DWG NO	REV
D		IK00035	10

SCALE NONE — SHEET 12 OF 15

APPROVALS — DATE — 3/83

APPLICATION — DO NOT SCALE DRAWING

FDC INTERFACE



		IK00035	10
	SIZ SHEET ONE		

	PARTS LIST		
APPLICATION	DO NOT SCALE DRAWING	3/83	OSBORNE COMPUTER CORPORATION 2453A BANTI CT HAYWARD, CALIFORNIA 94545 415-887-8080
			SCHEMATIC, OCC2 MAIN LOGIC PC BOARD
			SIZE D FSCM NO. IK00035 REV. 10
			SCALE NONE SHEET 3 OF 15

19.XX.83 KIT 080169

488 / PARALLEL INTERFACE

ENG. NO.	IK00035	SH 14	REV. 10
ZONE	REV.	DESCRIPTION	DATE - APPROVED
		SEE SHEET ONE	

3C7 DATA7 26
3C7 DATA6 27
3C7 DATA5 28
3C7 DATA4 29
3C7 DATA3 30
3C7 DATA2 31
3C7 DATA1 32
3C7 DATA0 33
+5V 22, 24
4B2 488 SEL* 23
2A1 68 ENABLE 25
3C3 ADR0 36
3C3 ADR1 35
3B3 RESET* 34
2B1 IOW*/R 21

6821 PIA
UD8
D7 D6 D5 D4 D3 D2 D1 D0 CS0 CS1 CS2* E RS0 RS1 RESET* R/W*
PA7 PA6 PA5 PA4 PA3 PA2 PA1 PA0
PB0 PB1 PB2 PB3 PB4 PB5 PB6 PB7
CA1 CA2 CB1 CB2
IRQA* IRQB*

3D8 IRQ* 38, 37
13C8 FDCIRQ 18
PB6 16 (NDAC)
PB3 13 (EOI)
PB5 15 (DAV)
PB7 17 (NRFD)
PB2 12
PB1 11
CA1 40 (SRQ)
CA2 14 (ATN)
39 (IFC)
CB2 19 (REN)

UE7 74LS04 ×6
UE8 7438 ×2
UF8 74LS03
RN9 3.3K
UF10 UF9 74LS08
UE10 7438
UE9 7438
UE6 74LS02
UF7 7406 ×3
RN13 3.3K
RN14 6.8K
RN11 3.3K
RN12 6.8K
+5V

P3 IEEE 488
16 DIO8
15 DIO7
14 DIO6
13 DIO5
4 DIO4
3 DIO3
2 DIO2
1 DIO1
18 DAV GND
19 NRFD GND
20 NDAC GND
21 IFC GND
22 SRQ GND
23 ATN GND
24 LOGIC GND
12 SHIELD
8 NDAC
5 EOI
6 DAV
7 NRFD
10 SRQ
11 ATN
9 IFC
17 REN

19JUL83 KIT 080170

PARTS LIST

OSBORNE COMPUTER CORPORATION
2453A BANET CT. HAYWARD, CALIFORNIA 94545 415-xx/-xxxx

APPLICATION | DO NOT SCALE DRAWING | 3/83

SCHEMATIC, OCC2
MAIN LOGIC PC BOARD

SIZE D | IK00035 | REV. 10 | SHEET 14 OF 15

IK00035	15	10	
		SEE SHEET ONE	

KEYBOARD INTERFACE

3C7 ADR15 — UF11 74LS05 pin 11 / 10
3C7 ADR14 — UF14 74LS05 pin 1 / 2
3C7 ADR13 — UF14 74LS05 pin 5 / 6
3C7 ADR12 — UF14 74LS05 pin 9 / 8
3C7 ADR11 — UF14 74LS05 pin 13 / 12
3C7 ADR10 — UF14 74LS05 pin 3 / 4
3C7 ADR9 — UF11 74LS05 pin 9 / 8
3C7 ADR8 — UF14 74LS05 pin 11 / 10

P4 KEYBOARD

9	ROW7
5	ROW6
7	ROW5
2	ROW4
4	ROW3
6	ROW2
8	ROW1
3	ROW0

+5V

RN15 3.3K

10 9 7 8 5 6 3 4 2

P4 KEYBOARD

COL7	17
COL6	16
COL5	15
COL4	14
COL3	13
COL2	12
COL1	11
COL0	10
KBDSTB	18
+12V KBD	19
FRAME	1
GND	20

J10 2 1
J9 2 1
FRAME
+12V
R25 22

4C2 KBDSTB
4B2 KBDSEL* (PORT 14H)

74LS244 UF12

17	2A4	2Y4	3
15	2A3	2Y3	5
13	2A2	2Y2	7
11	2A1	2Y1	9
8	1A4	1Y4	12
6	1A3	1Y3	14
4	1A2	1Y2	16
2	1A1	1Y1	18
	A	Y	
	G*		
1	1G*	2G*	19

KEYBOARD INTERFACE

DATA7 3B7
DATA6 3B7
DATA5 3B7
DATA4 3B7
DATA3 3B7
DATA2 3B7
DATA1 3B7
DATA0 3B7

ISSUED KIT 000171

		APPLICATION	

PARTS LIST

DO NOT SCALE DRAWING

3/83

OSBORNE COMPUTER CORPORATION
2453A HARTE CT
HAYWARD, CALIFORNIA 94545
415-XXX-XXXX

SCHEMATIC. OCC2
MAIN LOGIC PC BOARD

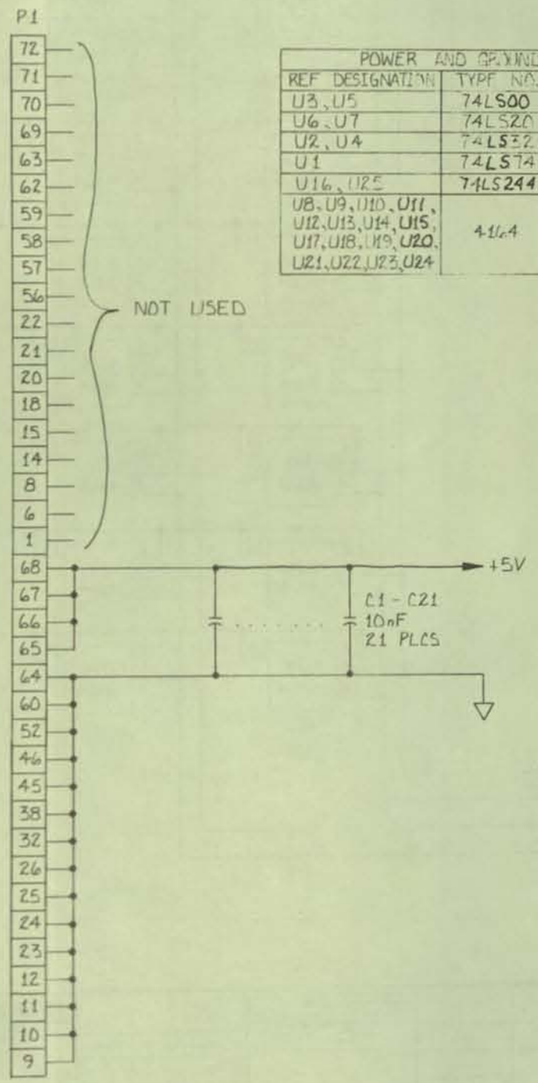
SIZE	DWG. NO.	REV.
D	IK00035	10

SCALE NONE SHEET 15 OF 15

DWG. NO. 1K000036	SH. 1	REV. B

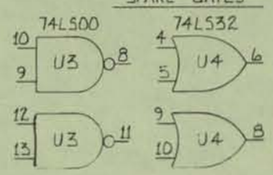
REVISIONS

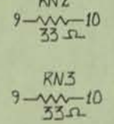
ZONE	REV.	DESCRIPTION	DATE	APPROVED
RELEASED	B	REDRAWN	8/Nov.	7/12/83



POWER AND GROUND TABLE			
REF DESIGNATION	TYPE NO.	GND	+5V
U3, U5	74LS00	7	14
U6, U7	74LS20	7	14
U2, U4	74LS32	7	14
U1	74LS74	7	14
U16, U25	74LS244	10	20
U8, U9, U10, U11, U12, U13, U14, U15, U17, U18, U19, U20, U21, U22, U23, U24	4164	16	8

SPARE GATES





REFERENCE DESIGNATION	
LAST	NOT USED
C21	—
RN3	—
U25	—

4 CIRCUITRY INSIDE DOTTED LINE NOT INCLUDED IN PC BOARD LAYOUT.

3 CIRCUITRY INSIDE DOTTED LINE NOT USED.

2. CAPACITOR VALUES ARE +80 -20%, 25VDC.

1. RESISTOR VALUES ARE ±10%, ⅛ W.

NOTES: UNLESS OTHERWISE SPECIFIED

		UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ARE: FRACTIONS DECIMALS ANGLES . XX . XXX .		OSBORNE COMPUTER CORPORATION 26500 Corporate Avenue Hayward, California 94545 415-887-8080
		MATERIAL	APPROVALS / DATE	SCHEMATIC, MEMORY PCB, OCC 2
2K00073	OCC 2	FINISH	DRAWN J. Spurr 7-22-83	
NEXT ASSY	USED ON		CHECKED C. Engelman 8-25-83	SIZE D / DWG. NO. 1K000036 / REV. B
APPLICATION		DO NOT SCALE DRAWING	ISSUED	SCALE NONE / SHEET 1 OF 2

DWG. NO.	REV.	SHT.
1K000036	B	2 OF 2

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

P1
RD* 16
ADR15 27
ADR14 28
ADR13 29
ADR12 30
ADR11 31
ADR10 33
ADR 9 34
ADR 8 35
CAE* 17
ADR 7 36
ADR 6 37
ADR 5 39
ADR 4 40
ADR 3 41
ADR 2 42
ADR 1 43
ADR 0 44
RAE* 19
MREQ* 3
RFSH* 5
PRI 1 61
ROM DECODE* 2
VRAM DECODE* 4
CAS* 13
RAS 7
P1

+5V
U1 74LS74
U116 74LS244
U115 74LS244
U2 74LS32
U3 74LS00
U4 74LS32
U5 74LS00
U6 74LS20
U7 74LS20
F DECODE*
BANK 1 ENA*
BANK 0 ENA*
CAS 1*
RAS 1*
CAS 0*
RAS 0*
RN1 33Ω
RN2 33Ω
WE* TO PIN 3,U8-U15,U17-U24
TO PIN 1,U8-U15,U17-U24
RA7 TO PIN 9,
RA6 TO PIN 13,
RA5 TO PIN 12,
RA4 TO PIN 11,
RA3 TO PIN 10,
RA2 TO PIN 7,
RA1 TO PIN 6,
RA0 TO PIN 5,

BANK 1
BANK 0
U24 U15 U23 U14 U22 U13 U21 U12 U20 U11 U19 U10 U18 U9 U17 U8
4164
DI DO CAS* RAS*

P1
47 DATA 7
48 DATA 6
49 DATA 5
50 DATA 4
51 DATA 3
53 DATA 2
54 DATA 1
55 DATA 0
P1

		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .X ± .XX ± .XXX ±		OSBORNE COMPUTER CORPORATION	26500 Corporate Avenue Hayward, California 94545 415-887-8080
		MATERIAL	APPROVALS DATE	SCHEMATIC, MEMORY PCB, OCC 2	
		FINISH	DRAWN		
NEXT ASSY	USED ON		CHECKED L. Bagnaden 8-25-83		
APPLICATION		DO NOT SCALE DRAWING	ISSUED	SIZE D DWG. NO 1K000036 REV B	
				SCALE NONE SHEET 2 OF 2	

ADJUSTING PARTS LIST

* MAKER ICR RESISTER	HITACHI	FUJITSU	MITSUBISHI
R39	160KΩ	160KΩ	180KΩ
R40	56.2KΩ	57.6KΩ	62.0KΩ

NOTES: UNLESS OTHERWISE SPECIFIED—
1. ALL CAPACITORS ARE IN MICROFARADS 50V, +80, -20%
2. ALL INDUCTORS ARE IN MICROHENRIES, 10%
3. ALL RESISTORS ARE IN OHMS, 1/4W, 5%

IC PARTS

SYMBOL	TYPE
IC12	74LS27
IC9,11	74LS123
IC8	MC3470AP
IC7	7407
IC6,10	74LS74
IC5	74LS10
IC4,15	74LS02
IC2,13	74LS14
IC1,3	7438
RP5	47KΩ
RP4	150Ω
RP3	2.2KΩ
RP2	22KΩ
RP1	150Ω
IC17	—
IC16	2003
IC14	74LS

APPLICATION	NEXT ASSY		
	USED ON		
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±			
MATERIAL			
FINISH			
DO NOT SCALE DRAWING			
DRAWN	W.L.H.+ROTH	APPROVALS	DATE
ISSUED			
CHECKED			8/8/83

ALPS

OSBORNE COMPUTER CORPORATION
26500 Corporate Avenue
Hayward, California 94545
415-887-8080

SIZE	DWG. NO	REV
D	FDD2124AE1	

SCALE

DISK DRIVE ELECTRONICS BOARD

SHEET

ZONE	REV.	DESCRIPTION	DATE	APPROVED
		REVISIONS		

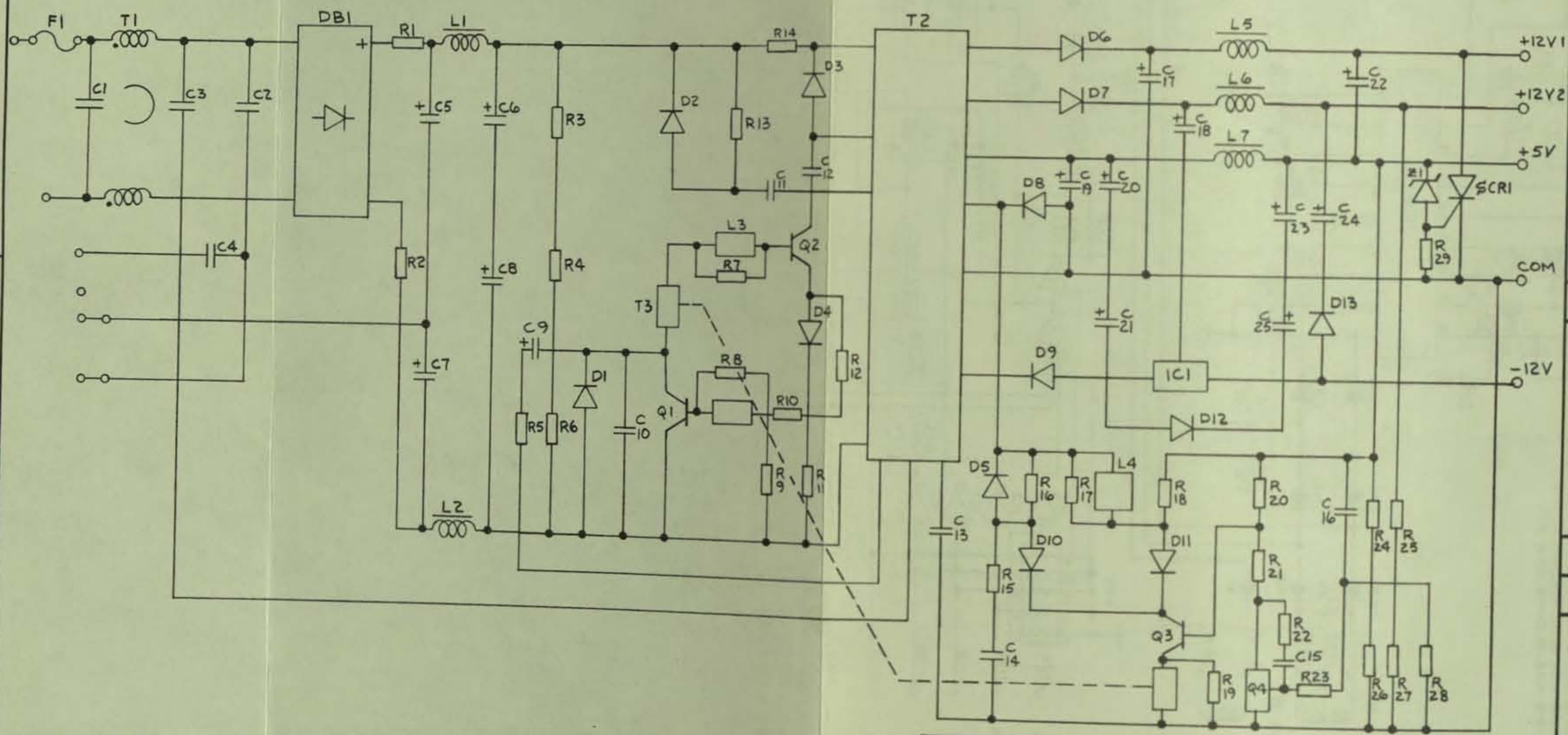
4 3 2 1

D

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

R			R1, R2	R5, R3, R4, R6	R7, 8, 9, 10, 13, 14	R11, 12	R15, 16, 17	R18, 19, 20, 21, 22, 23	R24, 25, 26, 27, 28, 29	
C	C1	C3 C4, C2	C5, C7	C6, C8, C9	C10	C11, C12	C13 C14	C19, 20, 21 C17, C18	C23, 24, 25, 22, 16	
L/T	T1		L1, L2		T3	L3	T2	L4	L5, 6, 7	
D/Q				D1	D2, Q1	D3, Q2, D4	D5, 6, 7, 8, 9, 10		D11, Q3, D12, Q4	D13
MISC F1		DB1						L4		Z1, SCR1

C



B

A

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS .XX .XXX ANGLES

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN W. LILLROTH	8/10/83
CHECKED	
ISSUED	

OSBORNE COMPUTER CORPORATION — Hayward, California 94545 415-887-8080

POWER SUPPLY

SIZE	FSCM NO.	DWG. NO.	REV.
C			
SCALE	ASTEC	SHEET	

DWG. NO. SH REV

SUMNER & TAYLOR REORDER NO. 40-107

4 3 2 1

Circuit Codes	Description
TB1	Wafer 3CCT
TB2	Wafer 2630-13
C3, C12	Tube-HS ID-13MM THK=.3MM
Q2	TRS-NPN 2SC1325A
Q1	TRS-NPN 2SD467
Q3	TRS-PNP 2SB561
Q4	IC TL431CLP
D5, D10, D11	Diode-SI 1N4606
Z1	Diode-Z 5.6V +-5% .040mA
D4	Rect RGP15B
D2	Rect RGP10J
D1, D9	Rect RGP10B
D12, D13	Rect IN4001GP
D3	Rect RGP10M
DB1	Bridge Rect KBP10
R9, R10	Res-CF 10R +-5% 1/4W
R28	Res-CF 100K +-5% 1/4W
R29	Res-CF 12K +-5% 1/4W
R22	Res-CF 12K +-5% 1/4W
R15	Res-CF 27K +-5% 1/4W
R16, R17	Res-CF 270K +-5% 1/2W
R19	Res-CF 330K +-5% 1/4W
R8	Res-CF 47K +-5% 1/4W
R23	Res-CF 470K +-5% 1/4W
R20, R21	Res-CF 56K +-5% 1/4W
R7, R12	Res-CF 5.6K +-5% 1/4W
R27, R28	Res-CF 68K +-5% 1/4W
R6	Res-CF 820K +-5% 1/4W
R18	Res-CF 8.2K +-5% 1/4W
R11	Res-MF .47K +-5% 1W
R14	Res-MF 1K +-5W
R25	Res-MF 22K +-2% 1/4W
R26	Res-MF 2.7K +-1% 1/4W
R24	Res-MF 4.7K +-2% 1/4W
R3, R4	Res-MOF 100K +-5% 1W
R13	Res-MOF 120K +-5% 1W
R5	Res-MOF 33K +-5% 2W
R1, R2	Res-Thmtr 4K +-20%
L4	Choke 1.5mH
L3	Base Choke 2.2uH
L7	Filter Choke Coil Assy
T2	Power Trf Assy
T3	Control Trf Assy (J/V)
L5, L6	Choke Coil Assy
T1	Com Mode Trf Assy
C12	Cap-C .01u +-20% 1KV Z5U
C10	Cap-C .01u +-20% 100V Z5U
C11	Cap-C 470p +-20% 3KV Z5P
C3, C4	Cap-C 4700p +-20% 400 VAC
C5, C7	Cap-E 100u +-20% 250V
C21, C25	Cap-E 100u +-20% 25V
C17, C18	Cap-E 1000u +-20% 16V

COMPONENT VALUES ON POWER SUPPLY BOARD

C9	Cap-E 220u +-20% 10V
C22, C23, C24	Cap-E 2200u +-20% 16V SM
C19, C20	Cap-E 2200u +-25% 10V
C6, C8	Cap-E 47u +100-10% 250V
C15	Cap-P .022u +-20% 100V
C14, C16	Cap-P .22u +-10% 100V
C1, C13	Cap-MPR .01u +-20% 250VAC
C2	Cap-MPR .1u +-20% 250VAC
F1	Fuse 2.5A 250V 3AG
L1, L2	Toroid
IC1	-12V Regu MC7912C
D8	Diode-SCK S10SC3M
D6, D7	Rect-SCK CTB-24
SCR1	SCR C122U

SAMPLES OF NEW OR REVISED PART MUST BE APPROVED BY ZENITH RADIO CORPORATION BEFORE PROCEEDING WITH PRODUCTION. UNLESS OTHERWISE SPECIFIED IN CHANGE COLUMN, AFTER APPROVAL MANUFACTURER SHALL NOT CHANGE THE DESIGN, PERFORMANCE, MATERIALS, OR MANUFACTURING SITE WITHOUT PRIOR NOTIFICATION AND APPROVAL BY ZENITH RADIO CORPORATION.

A	123-5657
MUST PASS THE FOLLOWING SPECIFICATIONS	
OTHER	ZENITH

CHANGES

A — REVISED SCHEMATIC

VERTICAL

HORIZONTAL

VIDEO

VX201

Q301 VERT OSC
Q302 VERT OSC II
Q303 DIFF AMP
Q304 VERT DRIVER
Q306 VERT OUT II
Q307 VERT OUT I
Q308 VERT RETRACE
Q401 VIDEO OUTPUT
Q402 VIDEO DRIVER
Q101 HORIZ OSC
IC 101 HORIZ OSC
Q102 HORIZ DRIVE
Q103 HORIZ OUTPUT
Q104 SYNC AMP

P.C. BOARD EDGE CONNECTOR (FOIL SIDE)

KEY

VERT. VID GND	VERT. DRIVE	VIDEO INPUT	B+ 12V	HORIZ. DRIVE	BRIGHT. TAP	BRIGHT. LOW	BRIGHT. HIGH	HORIZ. GND	
0	9	8	7	6	5	4	3	2	1

= DC VOLTAGE SOURCE

= DC VOLTAGE APPLIED

NOTE 1. CUSTOMER SUPPLIED EXTERNAL PIN 7 EDGE CONNECTOR.

123-5657
SHEET 2

SCHEMATIC FOR DS7 VIDEO DISPLAY
15.6 KHZ HORIZ SCAN FREQ

ZENITH RADIO CORP. CHICAGO, ILL. | A | 123-5657

OSBORNE
COMPUTER CORPORATION

2F00213-01