The Engineering Staff of
TEXAS INSTRUMENTS INCORPORATED
Semiconductor Group

TIB0203 Magnetic-Bubble Memory and Associated Circuits

NOVEMBER 1978

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Information contained herein supersedes previously published data on these devices.

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INTRODUCTION

magnetic-bubble memory description

Magnetic-bubble-memory technology has advanced considerably since the concept was introduced by Bell Telephone Laboratories in 1967. Research indicated that small cylindrical magnetic domains, which are called magnetic bubbles, can be formed in single-crystal thin films of synthetic ferrites or garnets when an external magnetic field is applied perpendicularly to the surface of the film. These bubbles can be moved laterally through the film by using a varying magnetic field. These characteristics of magnetic bubbles make them ideally suited for serial storage of data bits; the presence or absence of a bubble in a bit pisition is used to define the logic state. Since the diameter of a bubble is so small (as little as a tenth of a micrometer), many thousands of data bits can be stored in a single bubble-memory chip. In the spring of 1977 Texas Instruments was the first to market a 92,304-bit bubble memory. This bubble memory is much like magnetic tape or magnetic disc memory storage in that it is nonvolatile meaning that the data is retained even when power is no longer applied to the chip. Since bubble memories are a product of solid-state technology (there are no moving parts), they have higher reliability than tape or disc storage and do not require any preventive maintenance. In addition, the bubble memory is small and lightweight and is, therefore, an excellent choice for compact designs and portable applications.

functional operation of bubble memories

The basic bubble-memory package contains the bubble-memory chip, magnetic field coils, and permanent magnets as shown in Figure 1. A rotating magnetic field created by two mutually perpendicular coils causes the data in the form of magnetic bubbles to move serially through the magnetic film in a manner similar to data in a semiconductor shift register. Two permanent magnets provide nonvolatility and allow for the stable existence of magnetic-bubble domains. Interfacing circuits that are compatible with standard TTL devices complete the memory module to allow a convenient building-block concept for the nonvolatile memory system.

The chip is composed of a nonmagnetic crystaline substrate upon which a thin crystalline magnetic epitaxial film is grown. Only certain materials exhibit the properties necessary to form magnetic bubbles and these include orthoferrites, hexagonal ferrites, synthetic garnets, and amorphous metal films. Among these, the synthetic garnets have the best combination of the desired properties. Synthetic garnets support the formation of small magnetic bubbles that allow high-density data storage. The bubbles are highly mobile and are stable over a fairly wide range of temperatures.

The material chosen for the substrate depends on several factors. The crystalline structure should be compatible with that of the magnetic film, it should have nearly the same coefficient of expansion, and it should be nonmagnetic. The most-used garnet substrate with these properties is gadolinium gallium garnet (GGG). The magnetic film grown on this substrate has a crystalline structure that will allow the formation of magnetic domains (bubbles) in a plane perpendicular to the substrate.

Without the influence of an external magnetic field, these magnetic domains form random serpentine patterns of equal area, minimizing the total magnetic energy of the magnetic film (see Figure 2). The magnetic field of the serpentine domains tends to line up primarily along a single axis (the "easy" axis) that is perpendicular to the plane of the film. If an external magnetic field is applied, its energy tends to expand domains polarized in the direction of the field and to shrink those polarized opposite to the field until they become small cylinders embedded in a background of opposite magnetization. Viewed on end, these cylinders have the appearance of small circles or bubbles with diameters from 2 to 30 micrometers. Increasing the field further causes the bubble to collapse or to be "annihilated". The external field provides a bias that makes the bubbles stable. This bias, being a static field, can be readily provided by permanent magnets with no expenditure of power.

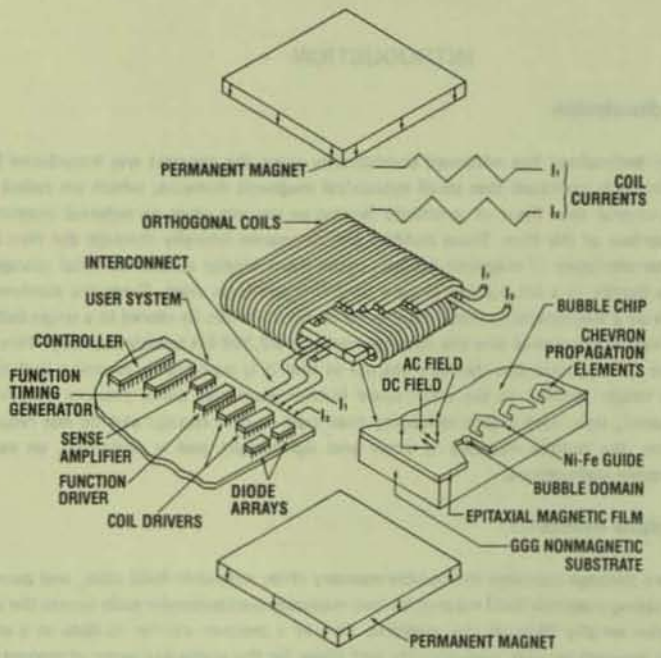
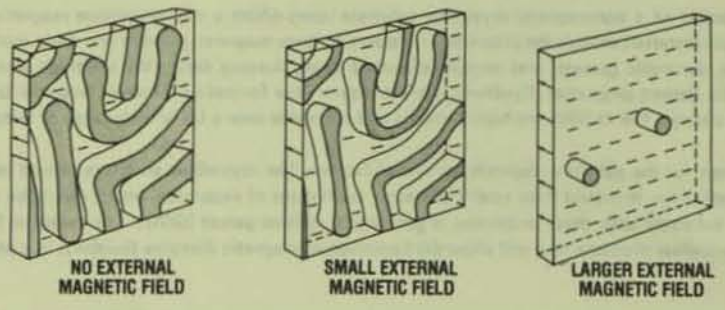


FIGURE 1–MAGNETIC-BUBBLE MEMORY (EXPLODED VIEW)



External magnetic field shrinks random serpentine domains of magnetically neutral crystal to cylindrical form.

FIGURE 2–MAGNETIC-BUBBLE DOMAINS

Before bubbles can be shifted through the magnetic film, they must be generated in accordance with input data. Bubbles are generated by locally altering the bias field with a magnetic field produced by a pulse of current through a microscopic one-turn metallized loop. This loop is located on a secondary layer immediately above the magnetic film on the surface of the chip. Given a current of the correct amplitude and polarity through the one-turn loop, a localized vertical magnetic field opposite to that of the permanent magnets is produced. This localized field establishes a domain wall inversion in the magnetic film resulting in bubble creation.

Once a bubble has been created, a method is then required to move the bubble domain along a predetermined path. This is accomplished by the deposition of chevron-shaped patterns of a soft magnetic material on the chip surface above the magnetic epitaxial film. When magnetized sequentially by a magnetic field rotating in the same plane, these chevron propagation patterns set up magnetic polarities that attract the bubble domain and establish motion. Figure 3 shows the various polarities at different positions of the rotating magnetic field. In actual practice the rotating in-plane magnetic field is implemented by applying a two-phase alternating current to the two coils shown in Figure 1.

One possible implementation for the magnetic bubble memory is a long shift register. As shown in Figure 4 the bubbles would shift under the influence of the rotating magnetic field following the path determined by the placement of chevron patterns. Even though this approach offers the simplest design and interface control, it suffers a major disadvantage of having the slowest access time. The reason for this is that after a data bit is entered or written it must circulate through the entire shift register before it can be retrieved or read. Another problem with this single loop design is that a single fault in the shift register structure produces a defective bubble memory chip. This results in a low processing yield and a high cost to the consumer.

For these reasons TI has chosen the major-minor loop architecture, which offers a dramatic improvement in access time. As shown in Figure 5, during a write operation (data entry), data is generated one bit at a time in the major loop. The data is then transferred in parallel to the minor loops where it circulates until the next time data is to be read out of the memory.

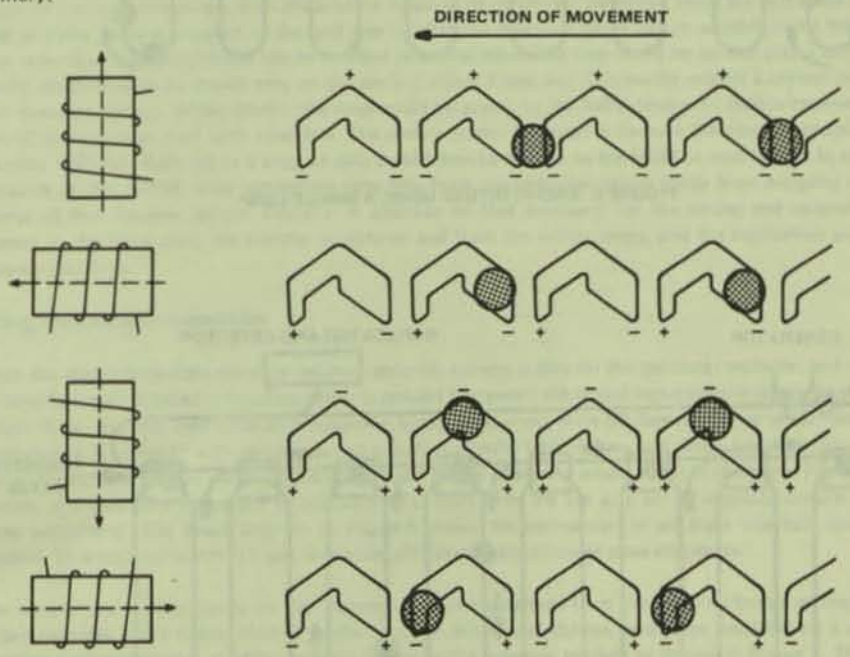


FIGURE 3

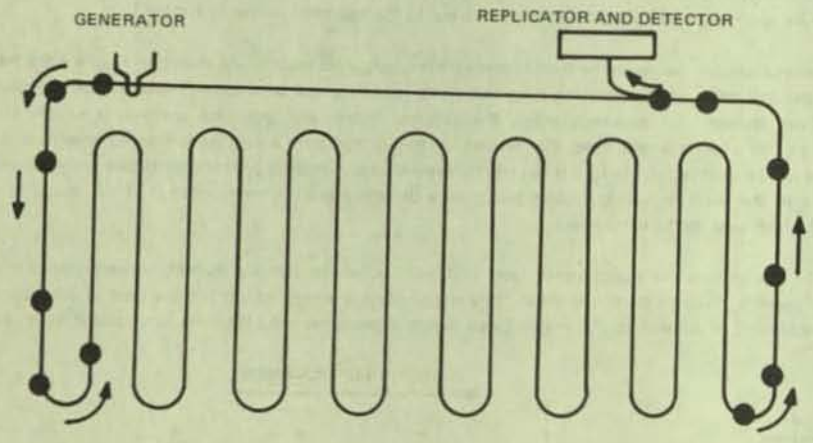


FIGURE 4. ARCHITECTURE USING A SINGLE LOOP

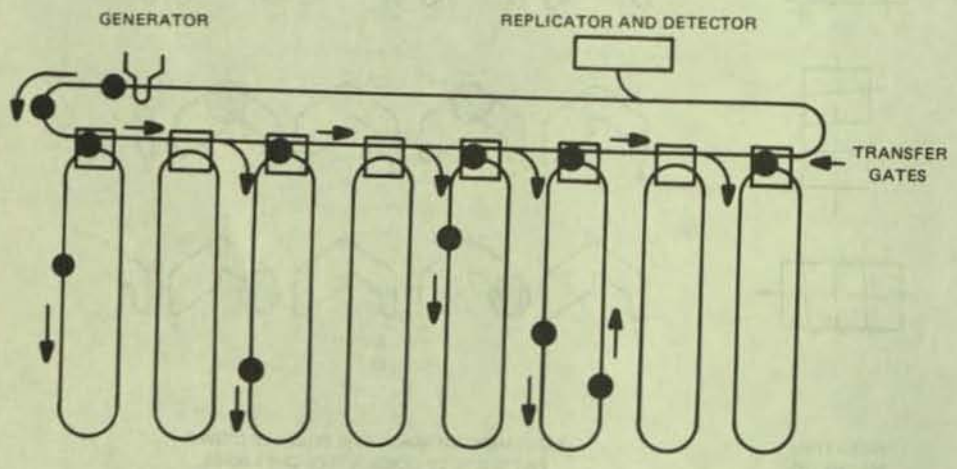


FIGURE 5. ARCHITECTURE USING MAJOR AND MINOR LOOPS

During a write operation data are introduced into the major loop by pulses of current through the hairpin loop of the generator. The major loop is essentially a unidirectional circular shift register from which data can be transferred in parallel to the minor loops. Thus a block of data is entered in the major loop and shifted until the first data bit is aligned with the most remote minor loop. At that time, each parallel transfer element receives a current pulse that produces a localized magnetic field causing the transfer of all the bubbles in the major loop to the top bit position of the corresponding minor loop. Once data is written into the magnetic bubble memory, new data may be written only by first removing the old data by doing a destructive read. In this operation bubbles are transferred from the minor loops and annihilated by running them into the Permalloy guard rail that usually surrounds bubble devices.

During a read operation the data block to be accessed in the minor loops is rotated until it is adjacent to the major loop. At this time the data block is transferred in parallel to the major loop. The block of data is then serially shifted to the replicator where the data stream is duplicated. The duplicated data takes the path to the magneto-resistive detector element. The presence of a bubble in the detector lowers the resistance resulting in a corresponding increase in detector current, which can be detected via a sense amplifier. The original data stream remaining in the major loop is rotated and transferred back into the minor loops thus saving the data for further operations.

The magnetic-bubble-memory devices are fabricated using fine geometries that make the manufacture of perfect devices a difficult task. In order to increase production yields and achieve correspondingly lower costs, redundant minor loops on the bubble-memory chip allow some loops to be defective. Defective loops are determined at final test and a map of these loops is supplied to the end user so that the defective loops can be avoided in the final memory system. This redundancy of minor loops can be handled in several ways. The map could be written into a software program that would direct data to be stored only to the perfect minor loops, but this would require a unique software package for each memory system. Alternatively, the map could be stored in the MBM (magnetic-bubble memory) itself with some risk of being written over with new data. The recommended approach is to store the map in a programmable read-only memory (PROM). Each bit in a page of data would then be written to the MBM or read from it in accordance with the contents of the PROM, thus preventing data bits from the defective minor loops from mingling with valid data. Of course all this requires control circuitry in addition to that necessary for the timing and control of the alternating current in the field coils, the transfer of data to and from the minor loops, and the replication and detection of the magnetic bubbles.

interfacing with bubble memories

Since the magnetic-bubble memory requires accurate current pulses for the generate, replicate, and transfer operations, an interface circuit called a function driver is needed to convert the digital input control signals to the required current pulses. Also, the two field coils each require a triangular current drive 90 degrees out of phase with each other. This requirement is satisfied with another set of interface circuits (coil drivers and diode array) that is driven with digital input signals. The output signal amplitude of the MBM is relatively small, about 3 millivolts. For this to be useful in a system, the output is converted to standard TTL levels with the use of a set of interface circuits (RC networks and sense amplifiers). The block diagram in Figure 6 shows the connection of all these interface circuits as a memory module. This modular building block promotes efficient construction of mass memories.

The control and timing signals for the memory module are derived from the function-timing generator. This integrated circuit provides input timing control to the function driver, coil drivers, and sense amplifier on a per-cycle basis. The function-timing generator provides control signals to the memory module as shown in Figure 7. These signals provide control for five basic operations: generate, replicate, annihilate, transfer-in, and transfer-out. The function-timing generator also initiates the rotating magnetic field and precisely synchronizes the timing of other control signals with this field.

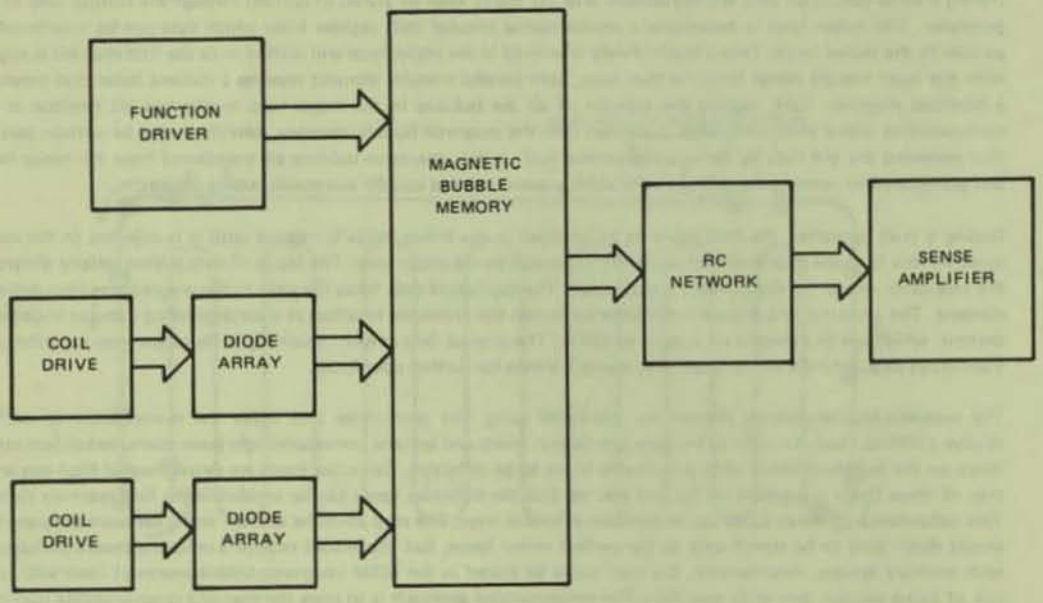


FIGURE 6. BUBBLE MEMORY MODULE

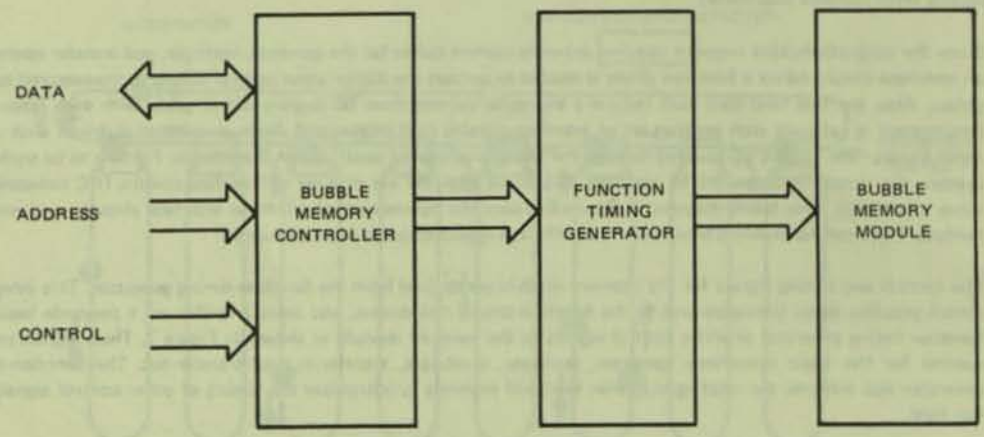


FIGURE 7. TIMING AND CONTROL FUNCTIONS

The time at which a particular data bit is detected in the MBM may not exactly match the time at which it is needed in the system. The sense amplifier not only increases the voltage level of the detected data, but also provides temporary storage of the data bits in a circuit called a D-type flip-flop. The sense amplifier receives a control input from the function timing generator to transfer the detected data into the internal flip-flop. In addition, the function-timing generator provides the control signals necessary to put the existing data in a known position during a power shut down. When the system is turned on again, the stored data can then be accurately located and retrieved.

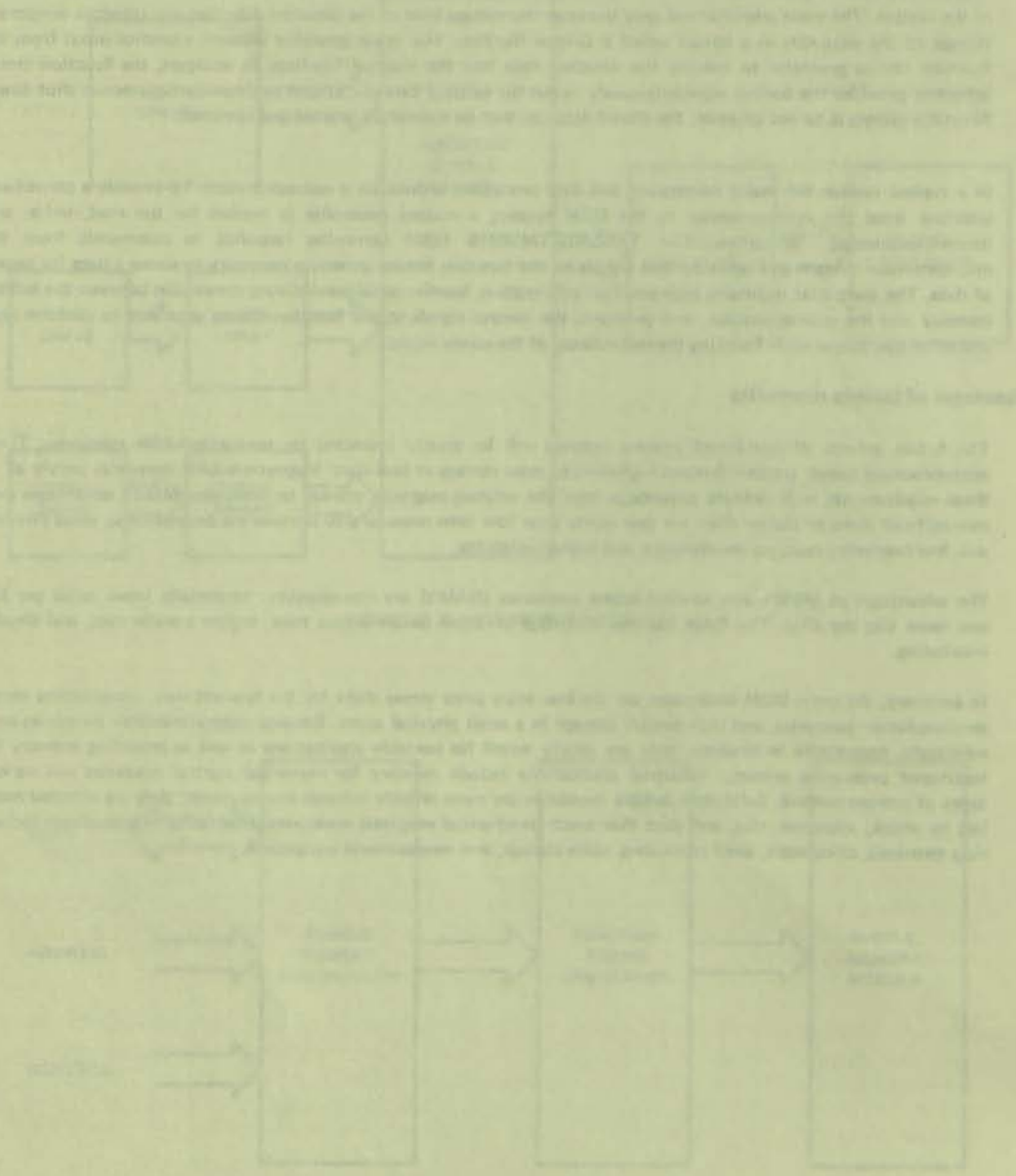
In a typical system the major computing and data processing is done by a microprocessor. To provide a convenient interface from the microprocessor to the MBM system, a custom controller is needed for the read, write, and memory-addressing operations. The TMS5502/TMS9916 MBM controller responds to commands from the microprocessor system and sends control signals to the function timing generator necessary to access a page (or pages) of data. The controller maintains page-position information, handles serial-parallel data conversion between the bubble memory and the microprocessor, and generates the control signals to the function-timing generator to perform read and write operations while handling the redundancy of the minor loops.

advantages of bubble memories

The future growth of distributed process systems will be greatly impacted by magnetic-bubble memories. These microprocessor-based systems demand high-density mass storage at low cost. Magnetic-bubble memories satisfy all of these requirements with definite advantages over the existing magnetic storage technologies. MBM's advantages over moving-head disks or floppy disks are low access time (the time necessary to retrieve the desired data), small physical size, low user entry cost, no maintenance, and higher reliability.

The advantages of MBM's over random-access memories (RAM's) are nonvolatility, potentially lower price per bit, and more bits per chip. The RAM has the advantage of much better access time, higher transfer rate, and simpler interfacing.

In summary, the main MBM advantages are the low entry price versus disks for the low-end user, nonvolatility versus semiconductor memories, and high-density storage in a small physical space. Because magnetic-bubble memories are a solid-state, nonvolatile technology, they are ideally suited for portable applications as well as providing memory for traditional processing systems. Industrial applications include memory for numerical control machines and various types of process control. Solid-state bubble memories are more reliable in harsh environments; they are affected much less by shock, vibration, dirt, and dust than electromechanical magnetic memories. Innovative new products include data terminals, calculators, word processing, voice storage, and measurement equipment.



TYPE TIB0203 MAGNETIC-BUBBLE MEMORY

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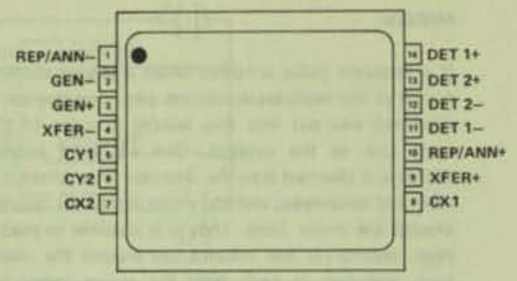
- 92,304-bit Nonvolatile Memory
- Major/Minor Loop Architecture
- 100-kHz Field-Rate Operation
- 50-kb/s Input/Output Data Rate
- Average Access Time (First Bit) . . . 4 ms
- Consumes Less Than 0.7 W for Continuous Operation
- Weighs Approximately 25 grams
- Rugged Package with Self-Contained Magnetics
- Occupies Less Than 1.25 in^2 (8 cm^2) of Board Area

TOP VIEW



description

The TIB0203 magnetic-bubble-memory device is a 14-pin dual-in-line module containing a 92,304-bit bubble-memory chip, coils for providing a rotating magnetic field, a permanent-magnet structure for providing the required static magnetic field, and a magnetic-shield assembly. The major/minor-loop architecture consists of 144 circular shift registers (minor loops) of 641 bits each that can transfer data in and out of a control loop (major loop). The major loop contains the generate, replicate, and annihilate control functions as well as the detector.

Control functions (i.e., generate, transfer-in, transfer-out, replicate and annihilate) are accomplished by providing current pulses through the appropriate control elements on the chip. A current pulse through a control element causes a local alteration in the magnetic field. This field alteration, in conjunction with the local permalloy pattern, accomplishes the control function. Pulses must be timed to coincide with the arrival of the bubble domain at the proper location on the chip.

To detect the presence or absence of bubbles, two magneto-resistive elements are provided. These elements may be used as part of a bridge circuit configuration that provides a high degree of noise cancellation when used with an external differential amplifier.

operation

generation

Bubble domains may be created by applying the specified current pulse through the generate loop. These domains step through the major loop in the predetermined direction. The presence or absence of a bubble in a bit position is used to define the logic state.

transfer-in

When a data string equal in length to the number of minor loops (a page) has been generated and shifted such that the first bit is positioned over the first minor loop, the transfer gate may be energized. This operation transfers the page from the major loop into minor loops. The data now circulates in the minor loops. New data may be generated, shifted, and transferred into each of 641 different minor loop page positions.

transfer-out

Data is retrieved by doing a transfer-out operation when the desired page rotates to the top of the minor loops. This moves the page out of the minor-loop structure and puts it back into the major loop. The page now moves around the major loop in bit-serial form until the first bit arrives at the replicate/annihilate element. One of two control operations may now be performed: replicate or annihilate.

operation (continued)

replicate

If a replicate pulse is issued when a bubble domain arrives at the replicate/annihilate gate, that domain is stretched and cut into two bubble domains of the same size as the original. One of these bubble domains is diverted into the detector area where it is read and destroyed, and the other continues moving around the major loop. Thus it is possible to read a page, recirculate the information around the major loop and put it back into the minor loops for nonvolatile storage. This operation provides a nondestructive read capability.

annihilate

Annihilation is accomplished by applying to the replicate/annihilate gate a current pulse that transfers the bubble out of the major loop, and into the detector track where it propagates off the chip.

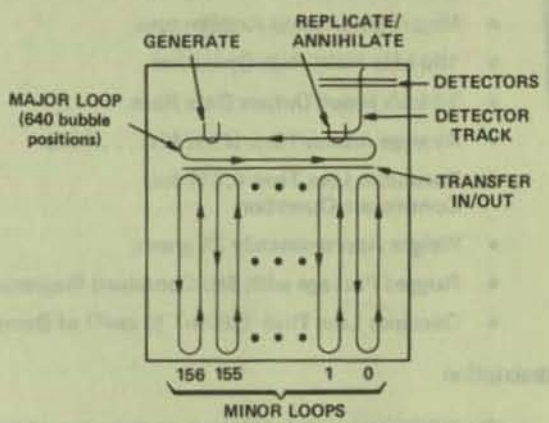


FIGURE 1–BASIC CHIP ARCHITECTURE

redundancy

To enhance production yields and thereby reduce device cost, redundancy has been designed in so that as many as 13 of the total 157 minor loops on the chip may be defective. Defective minor loops result from manufacturing processes related to the small geometry of the permalloy patterns. Defective minor loops are identified during factory testing and in no way relate to a field-failure mode. A map of the defective minor-loop locations will be printed on the device at the factory before shipment. This map consists of the hexadecimal address of each defective loop starting from address 00. See Drawing under Ordering Instructions and Mechanical Data.

Writing into defective loops is *not* an option. Some of these loops will have defects that may reproduce bubbles from normal coil-field drives. The reproduced bubbles may eventually contaminate the entire chip with unwanted bubbles.

coil drive

The bubble-memory chip is surrounded by two orthogonal coils that, when driven 90° out of phase, produce a rotating magnetic field in the plane of the chip. It is this rotating field that causes bubble domains to move under the permalloy patterns.

Triangular current waveforms are recommended for driving the two coils. This approach lends itself to precise digital control of the drive field. See Figure 2. It is essential that the starting and stopping sequences shown in Figure 2 be followed exactly to prevent loss of stored data. Starting begins with the buildup of positive current through CX2 and the final event in stopping is the decay of positive current through CX2.

If the two coils are turned on and off in the prescribed manner, bubble-domain motion in the minor loops can be started and stopped without error. Thus, if continuous duty is not required, a power savings can be realized by operating in the start/stop mode. Data in the major loop must be transferred to the minor loops before the field is stopped because data in the major loop is susceptible to loss when the field is stopped.

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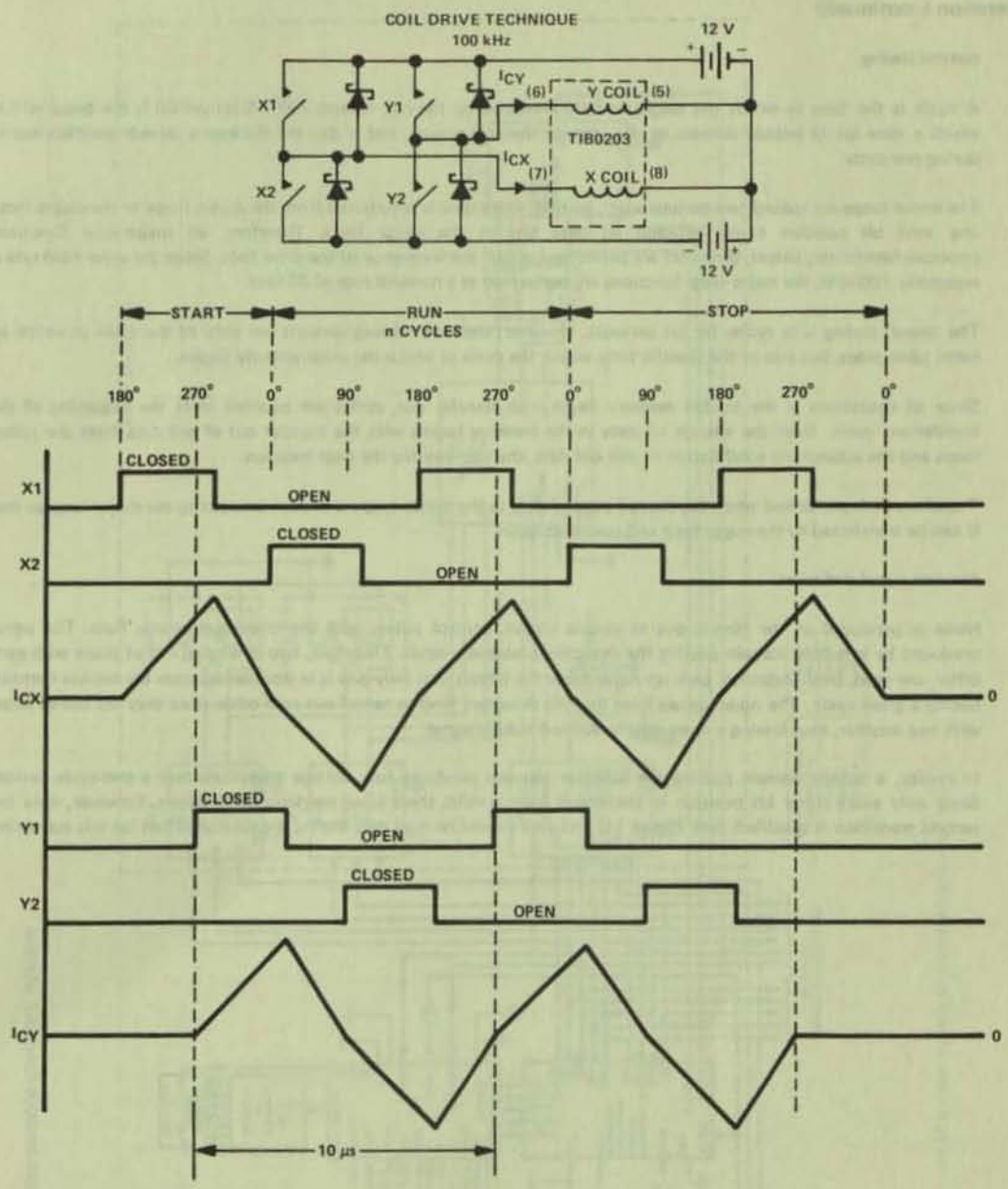
COIL DRIVE TECHNIQUE
100 kHz
12 V
X1
Y1
X2
Y2
ICY
(6)
Y COIL
(5)
TIB0203
ICX
(7)
X COIL
(8)
12 V
START
RUN
n CYCLES
STOP
180°
270°
0°
90°
180°
270°
0°
90°
180°
270°
0°
CLOSED
OPEN
X1
CLOSED
OPEN
X2
ICX
0
CLOSED
OPEN
Y1
CLOSED
OPEN
Y2
ICY
0
10 µs

FIGURE 2

operation (continued)

control timing

A cycle is the time in which the magnetic field produced by the coil rotates 360°. A bit period is the space within which a data bit (a bubble domain or the absence thereof) occurs, and is also the distance a bubble position moves during one cycle.

The minor loops are spaced two periods apart, so that, when data is transferred from the minor loops to the major loop, one void bit position exists between all data bits in the major loop. Therefore, all major-loop functions (replicate/annihilate, detect, generate) are performed at half the frequency of the drive field. Since the drive-field rate is nominally 100 kHz, the major-loop functions are performed at a nominal rate of 50 kHz.

The overall timing is in cycles (or bit periods). However, the exact timing consists not only of the cycle in which an event takes place, but also of the specific time within the cycle at which the pulse actually begins.

Since all operations in the bubble memory begin with transfer out, cycles are counted from the beginning of the transfer-out cycle. Even the storage of data in the memory begins with the transfer out of old data from the minor loops and the subsequent annihilation of this old data, thereby clearing the page location.

Transfer out is performed when the desired page of data in the minor loops is in position next to the major loop so that it can be transferred to the major loop and operated upon.

detector signal and noise

Noise is produced in the circuit due to circuit layout, control pulses, and the rotating magnetic field. The signal produced by a bubble domain passing the detector is relatively small. Therefore, two detectors, out of phase with each other, are used. Both detectors pick up noise from the circuit, but only one is in position to sense the bubble domains during a given cycle. The noise signals from the two detectors tend to cancel out each other since they are out of phase with one another, thus leaving a more clearly defined bubble signal.

In reality, a bubble domain passing the detector element produces four voltage transitions over a two-cycle period. Since only every other bit position in the major loop is valid, there is no overlapping of signals. However, only the second transition is specified, (see Figure 11) and data should be read only during the time specified for this transition.

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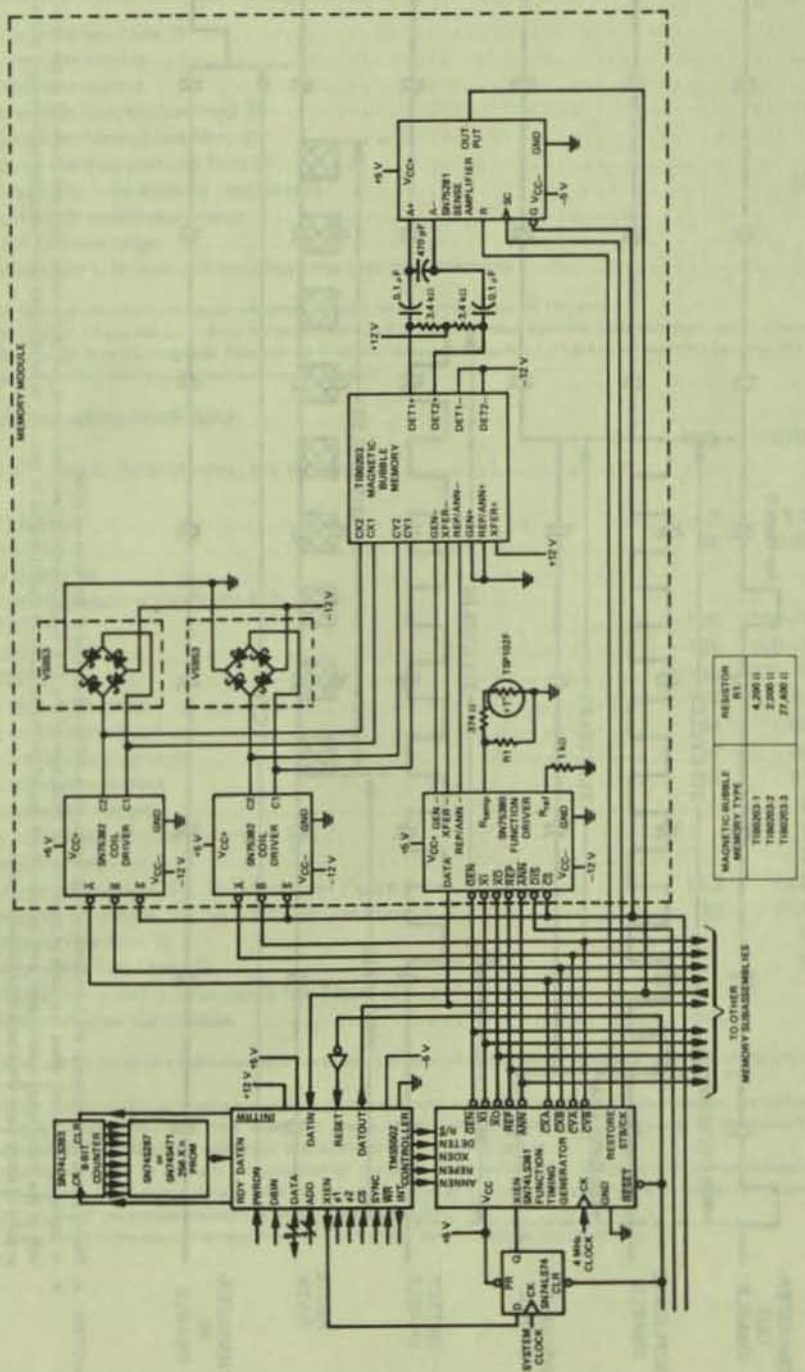
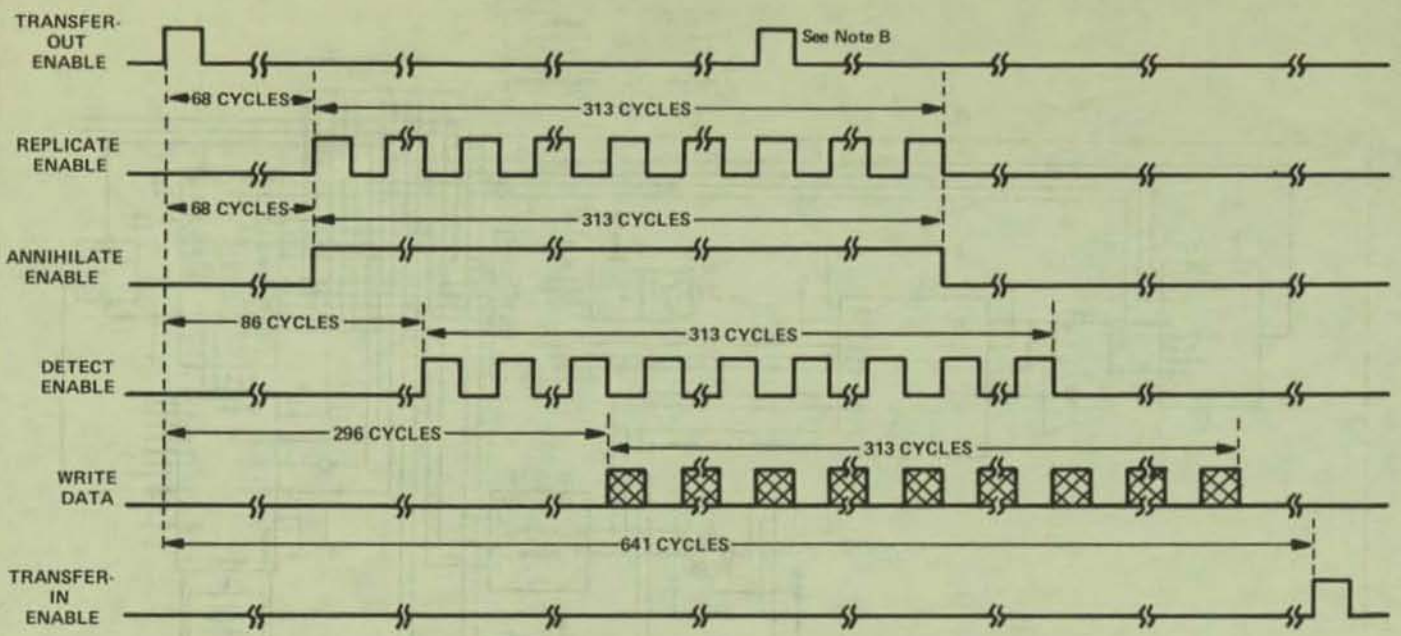


typical magnetic-bubble-memory system

VSB53 is a part number of Varo Semiconductor, Inc.

control timing



NOTES: A. Enable pulses are applied at the function timing generator, data pulses are applied at the function driver
B. In multipage operation, when one page of data (one bit from each of the 157 minor loops) has been transferred out of the minor loops and advanced to the other side of the major loop, another page may be transferred out of the minor loops so that it will be in position to be operated upon when the earlier page is in the process of being trans efred back into the minor loops.
C. Each enable pulse (or string of pulses) is 313 cycles long to allow the bits from all 157 minor loops plus the 156 void bit positions between the data bits in the major loop to pass the operating element. Transfer-out and transfer-in are parallel operations and therefore essentially one-cycle operations for all 157 bits.
D. See Figure 7 for the timing of pulses within the cycle.

FIGURE 3

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Peak coil current (see Note 1)	600 mA
Detector element current	7 mA
Transfer element current	50 mA
Replicate element current (see Note 2)	180 mA
Generate element current (see Note 2)	400 mA
Annihilate element current (see Note 2)	100 mA
External magnetic field intensity (see Note 3)	150 Oe (11.9 kA/m)
Operating free-air temperature range	0°C to 50°C
Storage temperature range	−40°C to 100°C
Lead temperature 1/16 inch (1.6 mm) from the case for 10 seconds	260°C

NOTES: 1. This value applies for a triangular waveform in each coil at a frequency of 100 kHz.
2. These values of current apply only for pulse operation at recommended nominal pulse duration and at a frequency of 100 kHz.
3. Exposure to external magnetic fields of an intensity between 20 oersteds (1.6 kA/m) and 150 oersteds (11.9 kA/m) may require manual clearing with a calibrated permanent magnet.

recommended operating conditions

	MIN	NOM	MAX	UNIT
External dc magnetic field intensity, any direction			20 (1.6 kA/m)	Oe
Detector current	4.8	5.2	5.7	mA
Field frequency	98	100	102	kHz
Generate frequency			51	kHz
On-state generate current (see Notes 4, 5, and 6)				
TIB0203-1	−10%	290−T	10%	mA
TIB0203-2	−10%	360−T	10%	mA
TIB0203-3	−10%	235−T	10%	mA
On-state replicate current	72	80	88	mA
On-state annihilate current	54	60	66	mA
On-state transfer-out current	34	38	42	mA
On-state transfer-in current	34	38	42	mA
Off-state generate current		0	±50	μA
Off-state replicate/annihilate current		0	±50	μA
Off-state transfer current		0	±50	μA
Coil-drive pulse amplitude, V_1, I_O = 5 mA, see Figure 4	11.3	11.9	12.5	V
Coil-drive pulse amplitude, V_2, I_O = 450 mA, see Figure 4	10	11.1	11.7	V
Dc coil current (see Note 7)		0	±3	mA
Coil-current offset (see Figure 5)		0	±10	mA
Current overshoot in coil X on stopping (see Figure 6)			−15	mA
Data-retention storage temperature	−40		85	°C

NOTES: 4. Care should be taken to ensure that no undershoot is present on the generate pulse as this can adversely affect the performance of the memory.
5. Generate pulse amplitude must be temperature compensated from the specified nominal value at the rate of −1 mA/°C over the operating temperature range. The quantities shown under NOM give the nominal values at temperature T and the percentages shown for MIN and MAX are tolerances that apply to these nominal values.
6. TI reserves the right to ship any combination of the three dash numbers for this part. All devices packed within the same box shall be of the same dash number. Each dash number requires a different resistor value in the resistor/thermistor network at the R_{temp} input of the bubble-memory function driver, SN75380.
7. Dc coil current is the current through the coils in the off condition (coils not driven).

timing requirements (see figures 7 and 8)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{d(gen)}$	Generate-pulse delay time†	5.1	5.2	5.3	µs
$t_{d(rep)}$	Replicate-pulse delay time†	5.1	5.2	5.3	µs
$t_{d(ann)}$	Annihilate-pulse delay time†	3.4	3.5	3.6	µs
$t_{d(XO)}$	Transfer-out-pulse delay time†	3.4	3.5	3.6	µs
$t_{d(XI)}$	Transfer-in-pulse delay time†	0.7	0.8	0.9	µs
$t_{d(CY2)}$	CY2-pulse delay time†	2.47	2.50	2.53	µs
$t_{d(CX1)}$	CX1-pulse delay time†	4.97	5.00	5.03	µs
$t_{d(CY1)}$	CY1-pulse delay time†	7.47	7.50	7.53	µs
$t_{w(gen)}$	Width of generate pulse	0.4	0.5	0.6	µs
$t_{w(rep)}$	Width of replicate pulse	2.65	2.75	2.85	µs
$t_{w(ann)}$	Width of annihilate pulse	4.65	4.75	4.85	µs
$t_{w(XO)}$	Width of transfer-out pulse	5.9	6.0	6.1	µs
$t_{w(XI)}$	Width of transfer-in pulse	5.9	6.0	6.1	µs
$t_{w(CX1)}$	Width of coil-drive pulse through CX1	2.95	3.0	3.05	µs
$t_{w(CX2)}$	Width of coil-drive pulse through CX2	2.95	3.0	3.05	µs
$t_{w(CY1)}$	Width of coil-drive pulse through CY1	2.95	3.0	3.05	µs
$t_{w(CY2)}$	Width of coil-drive pulse through CY2	2.95	3.0	3.05	µs
$t_{r(gen)}$	Generate-pulse rise time		0.1	0.2	µs
$t_{f(gen)}$	Generate-pulse fall time (see Note 4)		0.1	0.2	µs
$t_{r(rep)}$	Replicate-pulse rise time		0.1	0.2	µs
$t_{f(rep)}$	Replicate-pulse fall time		0.1	0.2	µs
$t_{r(ann)}$	Annihilate-pulse rise time		0.1	0.2	µs
$t_{f(ann)}$	Annihilate-pulse fall time		0.1	0.2	µs
$t_{r(XO)}$	Transfer-out-pulse rise time		0.1	0.2	µs
$t_{f(XO)}$	Transfer-out-pulse fall time		0.1	0.2	µs
$t_{r(XI)}$	Transfer-in-pulse rise time		0.1	0.2	µs
$t_{f(XI)}$	Transfer-in-pulse rise time		0.1	0.2	µs

NOTE 4: Care should be taken to ensure that no undershoot is present on the generate pulse as this can adversely affect the performance of the memory.

†All delay times are measured from the beginning of the cycle (leading edge of the CX2 pulse) in which they occur.

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP‡	MAX	UNIT
r_G	Resistance of generate element		4	7	Ω
r_R	Resistance of replicate element		8	12	Ω
r_T	Resistance of transfer element		300	350	Ω
r_{D1}	Resistance of detector element 1	850	1100	1450	Ω
r_{D2}	Resistance of detector element 2	850	1100	1450	Ω
$r_{D1} - r_{D2}$	Differential resistance between detector elements			±20	Ω
L_x	Inductance of coil X (f = 100 kHz)	62	64	66	µH
L_y	Inductance of coil Y (f = 100 kHz)	57	59	61	µH
$z_{x(real)}$	Real part of impedance of coil X (f = 100 kHz)		4.8		Ω
$z_{y(real)}$	Real part of impedance of coil Y (f = 100 kHz)		4.3		Ω

‡All typical values are at T_A = 25°C.

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operating characteristics over operating free-air temperature range (unless otherwise noted)

		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
$V_{B(p-p)}$	Peak-to-peak bubble voltage	See Figures 9 and 11	2	3.5		mV
		See Figures 10 and 11		22		
$V_{N(p-p)}$	Peak-to-peak noise voltage§	See Figures 9 and 11		0.5		mV
		See Figures 10 and 11		5		
t_v	Time to valley before second transition†	See Figures 9 and 11	5.9	6.1	6.3	μs
t_{pk}	Time to peak of second transition†	See Figures 9 and 11	6.7	7.0	7.3	μs

†All delay times are measured from the beginning of the cycle (leading edge of the CX2 pulse) in which they occur.
‡All typical values are at T_A = 25°C.
§This noise voltage is largely a function of circuit layout. The value specified is typical for a well-designed circuit.

PARAMETER MEASUREMENT INFORMATION

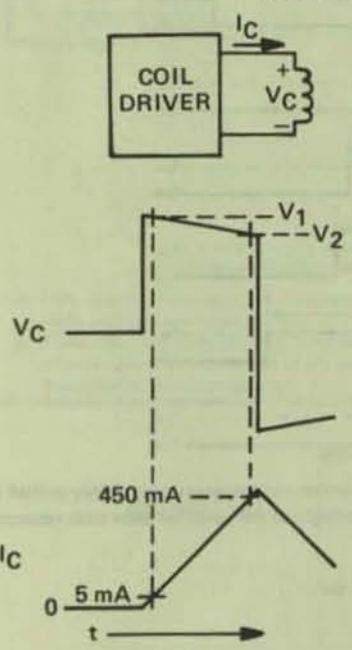

FIGURE 4

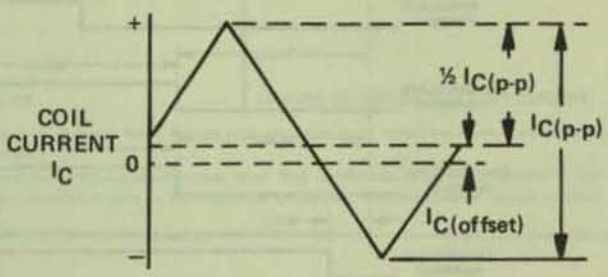

FIGURE 5

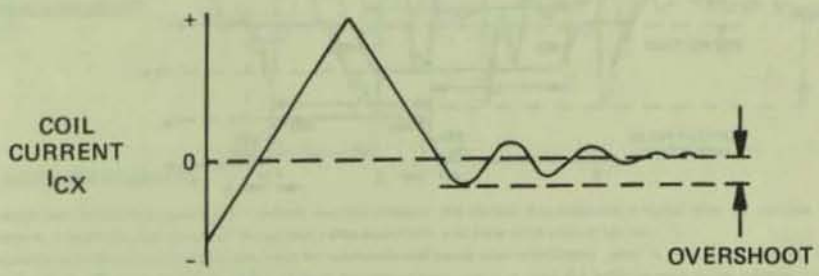

FIGURE 6

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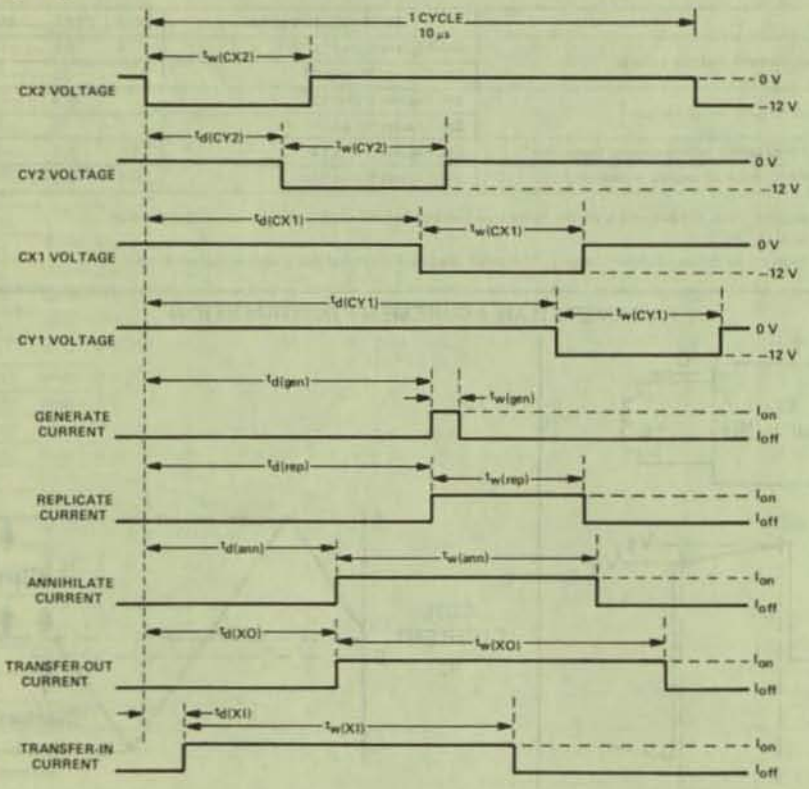
PARAMETER MEASUREMENT INFORMATION

pulse timing diagram



This diagram shows the timing of pulses within a cycle. The control pulse under consideration occurs only within the cycle in which it is enabled (see Figure 3). When it does occur the pulse must begin at the specified time with respect to the beginning of the cycle in which it occurs.

FIGURE 7

measurement points for pulse timing

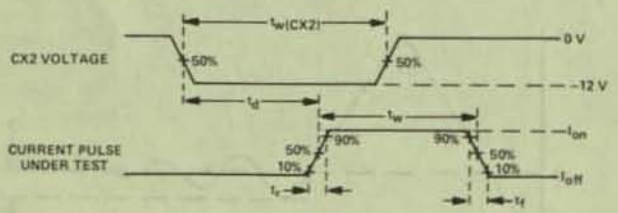


FIGURE 8

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PARAMETER MEASUREMENT INFORMATION

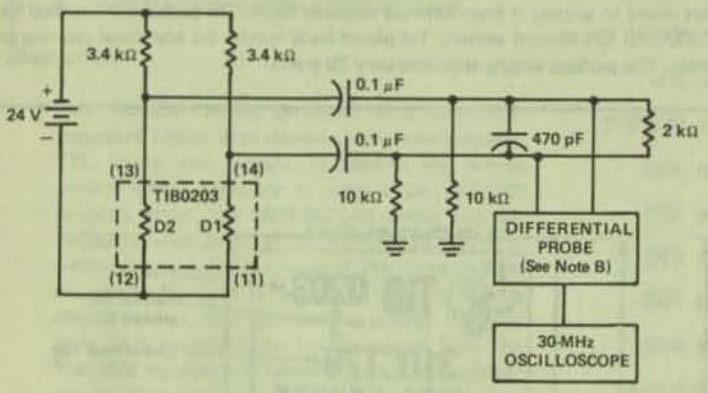


FIGURE 9–LOADED TEST CIRCUIT

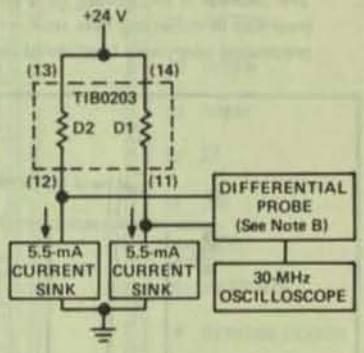
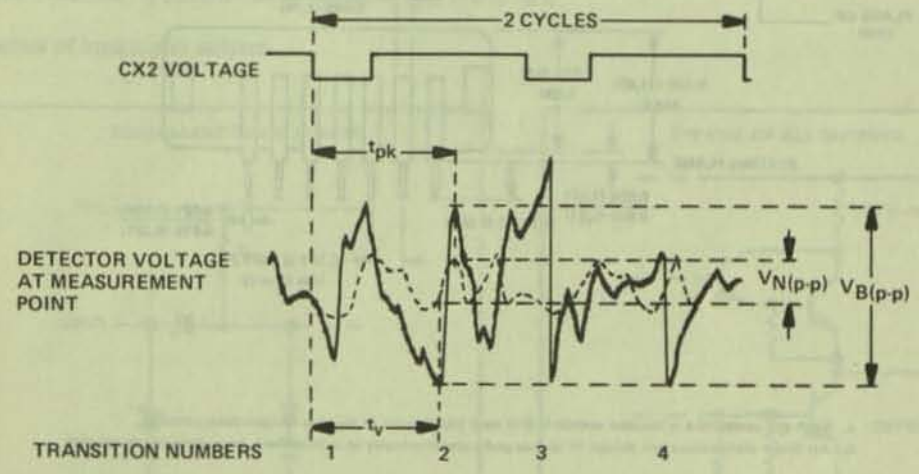


FIGURE 10–UNLOADED TEST CIRCUIT

NOTES: A. Care must be exercised in circuit layout to ensure that detector leads do not pick up noise from coil-drive leads, power-supply leads, and function current pulses.

B. Probe impedance must be greater than two megohms and probe capacitance less than five picofarads to avoid attenuating the observed signal. The bandwidth of the oscilloscope and probe should be 20 megahertz or greater. Common-mode rejection ratio should be 60 decibels minimum.



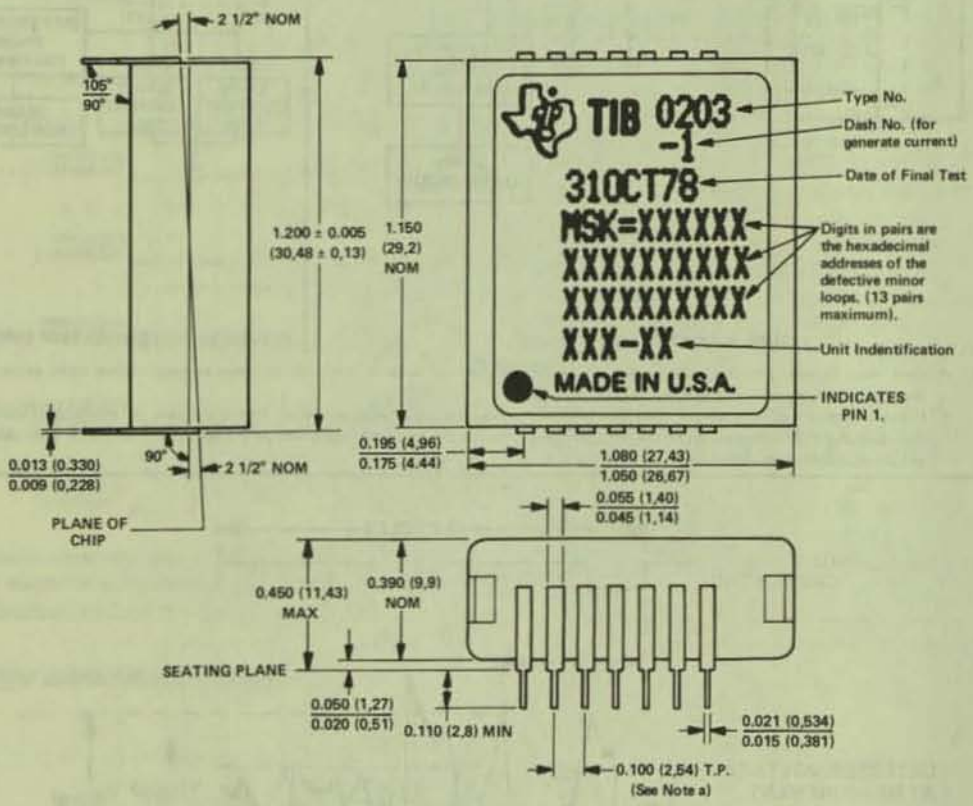
NOTES: A. The solid line indicates a signal with a bubble domain present; the dashed line indicates a signal with no bubble domain present. The shape, amplitude, and phase of the actual noise waveform will vary with circuit layout.

B. A magnetic-bubble domain passing the detector elements will cause four transitions over a two-cycle period. Only the second transition is specified, and both the peak-to-peak bubble voltage, $V_{B(p-p)}$, and the peak-to-peak noise voltage, $V_{N(p-p)}$ should be measured only during the time specified for this transition, i.e., minimum t_v to maximum t_{pk}.

FIGURE 11–VOLTAGE WAVEFORMS

ORDERING INFORMATION AND MECHANICAL DATA

The TIB0203 is mounted on a 14-pin dual-in-line lead frame and encapsulated in an electrically nonconductive plastic compound. Included in the package are the two coils that provide the rotating magnetic field and a permanent magnet. The package is surrounded by a magnet shield to protect it from external magnetic fields. The package is intended for insertion in mounting hole rows on 1.200-inch (30.48-mm) centers. Tin-plated leads require no additional cleaning or processing when used in soldered assembly. The package weighs approximately 25 grams.



NOTES: a. Each pin centerline is located within 0.010 inch (0,26 mm) of its true longitudinal position.
b. All linear dimensions are shown in inches and parenthetically in millimeters. Inch dimensions govern.

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TEXAS INSTRUMENTS
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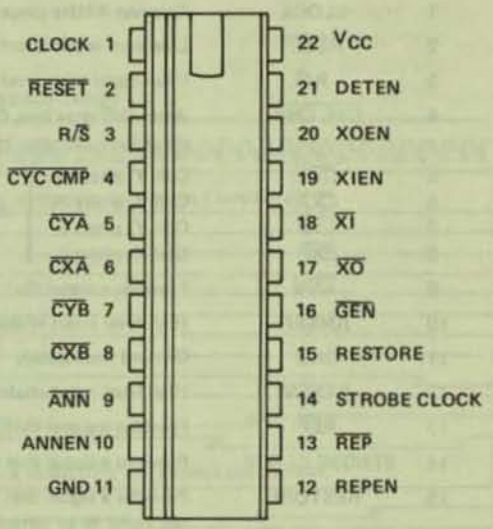
TYPE SN74LS361
BUBBLE-MEMORY FUNCTION TIMING GENERATOR

NOVEMBER 1978

- Provides Cycle Timing for TIB0203 92,304-Bit Magnetic-Bubble-Memory System
- Single 5-V Power Supply
- 400-Mil-Row-Center 22-Pin Package

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

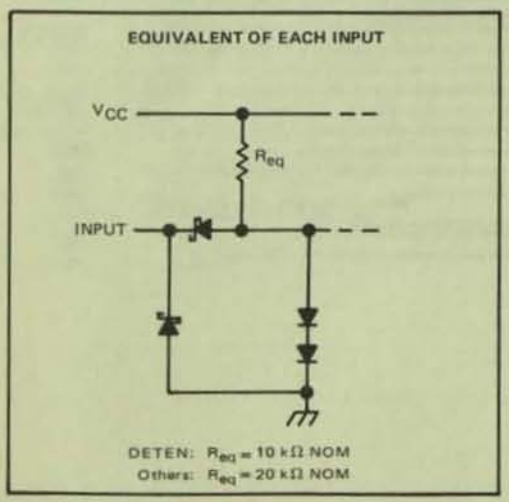
This function timing generator is a monolithic integrated circuit with standard low-power Schottky TTL inputs and outputs. It provides the precise control timing necessary to operate the SN75380 function driver, the SN75382 coil driver, and the SN75281 sense amplifier for the TIB0203 chevron-pattern magnetic-bubble-memory. The device consists of control flip-flops, a counter, a decoder matrix, output latches, and gating. The control flip-flops serve to synchronize the run/stop signal from the TMS5502 controller to control the starting, shifting, and stopping sequences of the bubble-field rotation. Each bubble-field rotation is divided into 40 intervals by the counter. The decoder matrix is accessed on the rising edge of the clock pulse during each interval and its outputs are latched. These outputs are then gated with the control signals from the TMS5502 to provide timing pulses to the coil drivers, sense amplifiers, and function drivers.

The SN74LS361 contains a V_{CC} monitor network that provides data protection during five-volt power up/down transient conditions. This network forces the coil-drive outputs of the function timing generator to the high logic level when the V_{CC} supply drops below approximately 3.5 volts.

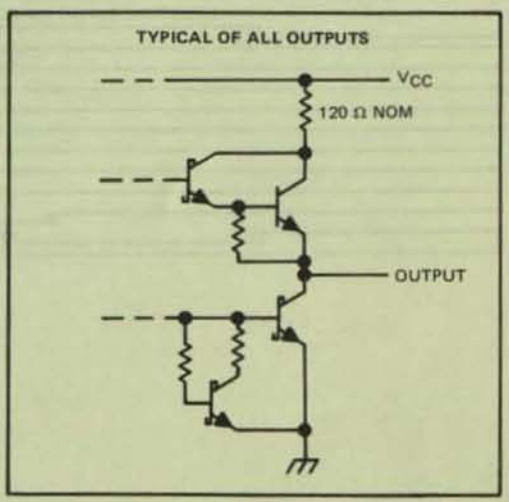
The SN74LS361 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



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TYPE SN74LS361
BUBBLE-MEMORY FUNCTION TIMING GENERATOR

PIN	SIGNATURE	FUNCTION
1	CLOCK	Receives 4-MHz clock signal, active on low-to-high transition.
2	$\overline{\text{RESET}}$	Low level input clears flip-flop and initializes the circuit.
3	R/$\overline{\text{S}}$	(Run/stop) High level initiates bubble shift, low level stops it.
4	$\overline{\text{CYC CMP}}$	After R/$\overline{\text{S}}$ goes low, $\overline{\text{CYC COMP}}$ goes low when the system is back to page 0 and the drive field will stop 1/4 cycle later.
5	$\overline{\text{CYA}}$	Coil Y, phase A } to coil driver inputs
6	$\overline{\text{CXA}}$	Coil X, phase A } to coil driver inputs
7	$\overline{\text{CYB}}$	Coil Y, phase B } to coil driver inputs
8	$\overline{\text{CXB}}$	Coil X, phase B } to coil driver inputs
9	$\overline{\text{ANN}}$	Provides a signal that, when low, causes the function driver to emit an annihilate pluse.
10	ANNEN	High level input enables the $\overline{\text{ANN}}$ output.
11	GND	Ground (substrate).
12	REPEN	High level input enables the $\overline{\text{REP}}$ output.
13	$\overline{\text{REP}}$	Provides a signal that, when low, causes the function driver to emit a replicate pulse.
14	STROBE CLOCK	Provides a signal that clocks the sense amplifier on the low-to-high transistion.
15	RESTORE	Provides a signal that, when high, initializes the sense amplifier, and when low, allows the signal to be sensed.
16	$\overline{\text{GEN}}$	Provides a signal that, when low, causes the function driver to emit a generate current pulse.
17	$\overline{\text{XO}}$	Provides a signal that, when low, causes the function driver to emit a transfer-out current pulse.
18	$\overline{\text{XI}}$	Provides a signal that, when low, causes the function driver to emit a transfer-in current pulse.
19	XIEN	High level input enables the $\overline{\text{XI}}$ output.
20	XOEN	High level input enables the $\overline{\text{XO}}$ output.
21	DETEN	High level input enables the STROBE CLOCK and RESTORE outputs.
22	V_{CC}	+5-V supply.

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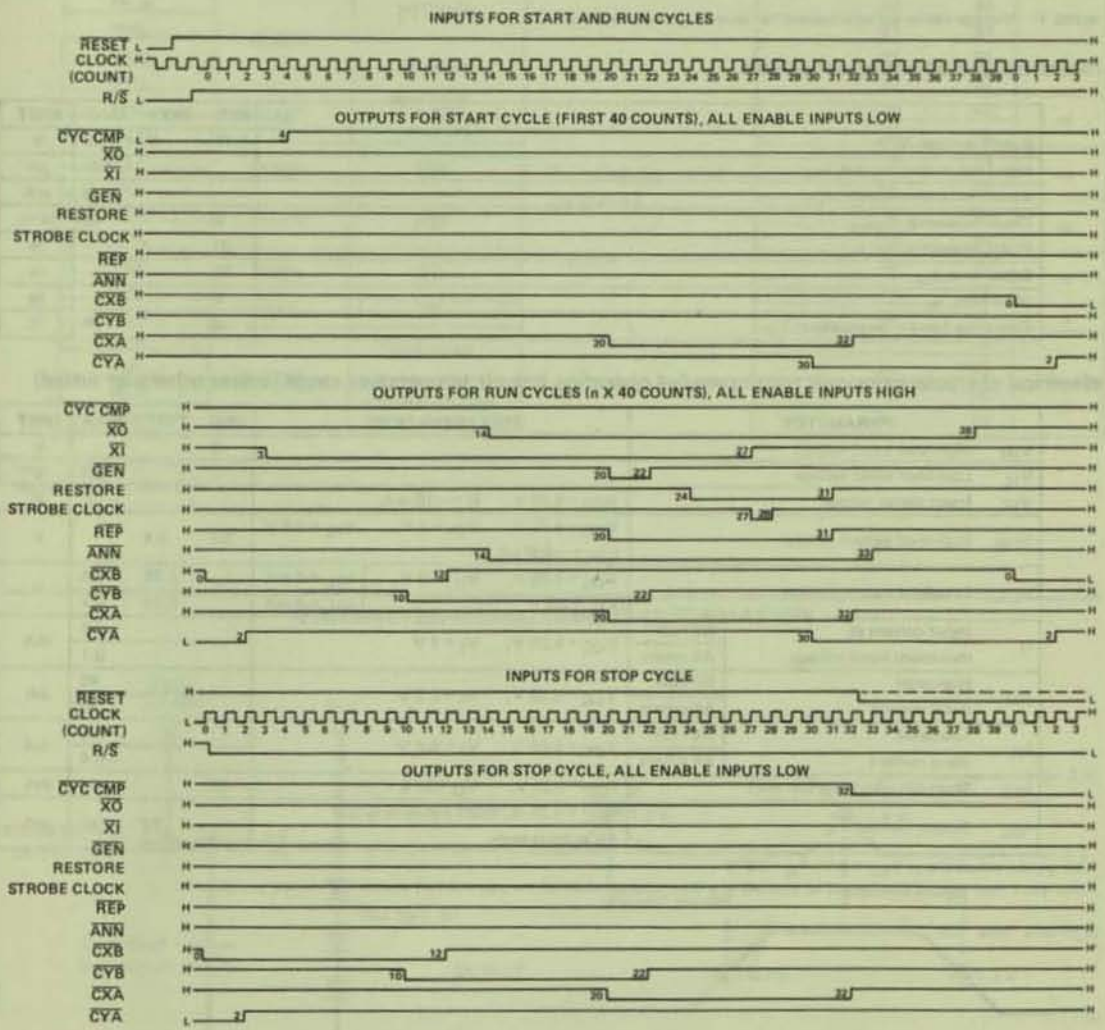
typical timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level output current, I_{OH}			−400	μA
Low-level output current, I_{OL}			8	mA
Clock frequency, f_{clock}	0		12	MHz
Width of clock pulse, t_w	20			ns
Setup time, t_{su}	20			ns
Hold time, t_h	0			ns
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = 4.75 V, I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA		2.7	3.1		V
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OL} = 8 mA		0.35	0.5	V
				I_{OL} = 4 mA		0.25	0.4	
I_I	Input current at maximum input voltage	DETEN	V_{CC} = 5.25 V, V_I = 7 V				0.2	mA
		All others					0.1	
I_{IH}	High-level input current	DETEN	V_{CC} = 5.25 V, V_I = 2.7 V				40	μA
		All others					20	
I_{IL}	Low-level input current	DETEN	V_{CC} = 5.25 V, V_I = 0.4 V				−0.8	mA
		All others					−0.4	
I_{OS}	Short-circuit output current‡		V_{CC} = 5.25 V, V_O = 0		−20		−100	mA
I_{CC}	Supply current		V_{CC} = 5.25 V, All inputs at GND, All outputs open			70	115	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C
‡ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

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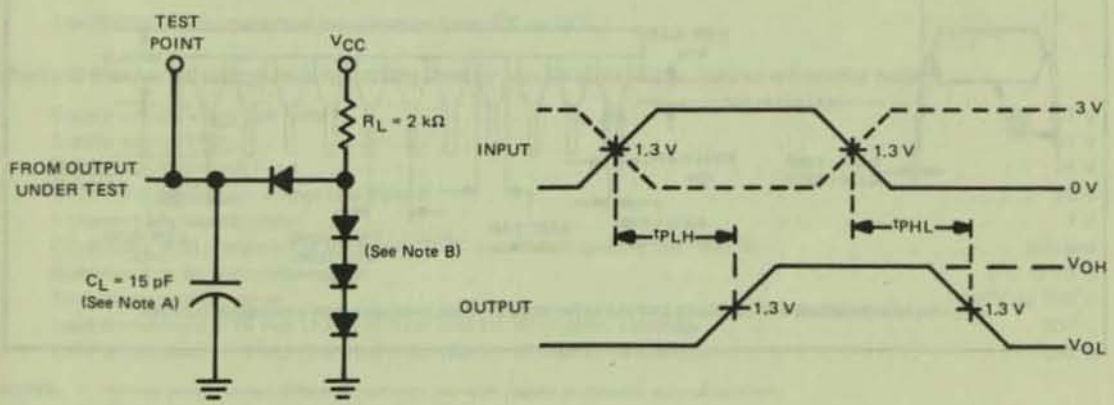
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			R_L = 2 kΩ, C_L = 15 pF, See Figure 1	12	16		MHz
t_{PLH}	CLOCK	$\overline{CYC\ CMP}$			43	60	ns
t_{PHL}					41	60	
t_{PLH}		All others			35	55	ns
t_{PHL}					33	50	
t_{PHL}	RESET	$\overline{CYC\ CMP}$			26	40	ns
t_{PLH}		All others			39	55	
t_{PLH}	ANNEN	$\overline{ANN}$			9	15	ns
t_{PHL}					13	20	
t_{PLH}	REPEN	$\overline{REP}$			9	15	ns
t_{PHL}					13	20	
t_{PLH}	XOEN	$\overline{XO}$			10	15	ns
t_{PHL}					13	20	
t_{PLH}	XIEN	$\overline{XI}$			30	45	ns
t_{PLH}	DETEN	RESTORE			11	15	ns
t_{PHL}					13	20	
t_{PLH}		STROBE CLOCK			9	15	ns
t_{PHL}					14	20	

†f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high level output
t_{PHL} = propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. Input pulses are supplied by a generator having the following characteristics: $t_r \leq 15$ ns, $t_f \leq 6$ ns, PRR ≤ 1 MH_z, $Z_{out} \approx 50\ \Omega$.

FIGURE 1

1178

TYPE SN74LS361
BUBBLE-MEMORY FUNCTION TIMING GENERATOR

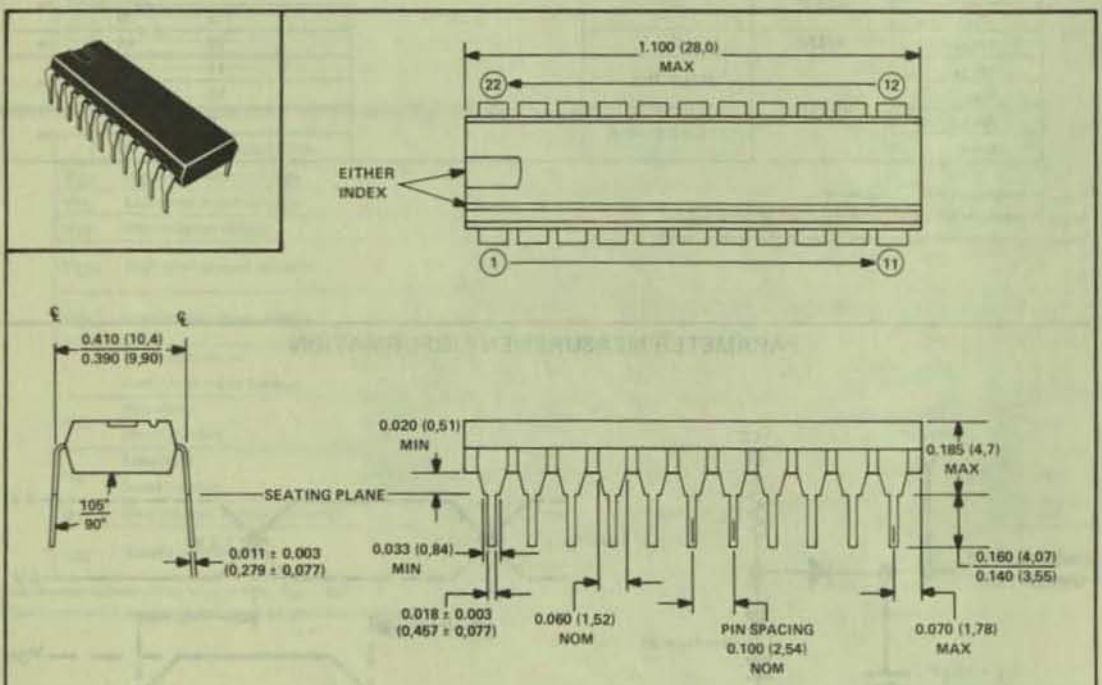
ORDERING INSTRUCTIONS AND MECHANICAL DATA

general

This circuit is available in the 22-pin plastic dual-in-line package (outline N). Orders for this circuit should include the package outline letter (N) at the end of the circuit type number, i.e., SN74LS361N.

N plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a 22-lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 0.400-inch (10,16-mm) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



ALL LINEAR DIMENSIONS ARE IN INCHES AND PARENTHETICALLY IN MILLIMETERS. INCH DIMENSIONS GOVERN.

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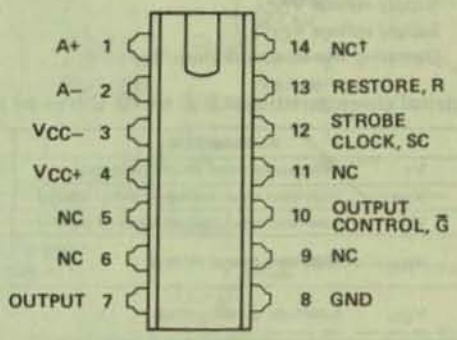
TYPE SN75281
BUBBLE-MEMORY SENSE AMPLIFIER

NOVEMBER 1978

- Precision Sensing Threshold Level between 0.8 mV and 1.2 mV
- TTL-Compatible Control Inputs
- Three-State TTL Output
- Operates from ±5-Volt Supplies

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC–No internal connection
†Grounding pin 14 improves isolation between restore and A+ input.

description

The SN75281 is a monolithic integrated circuit available in either a plastic or ceramic package. It senses the voltage change when a bubble passes the magneto-resistive detector elements in a magnetic-bubble memory. The output of this detector is connected between the differential sense inputs, A+ and A–, through an RC network. The signal produced by the presence of a bubble passing the detector elements is converted to a TTL-compatible output by the sense amplifier.

The SN75281 consists of an internally ac-coupled amplifier, a threshold sense circuit, a D-type flip-flop, and a three-state output.

Three TTL-compatible control inputs allow the precise timing necessary to detect the presence or absence of a bubble. The restore input sets the dc reference voltage on the internal coupling capacitors so that data may be sampled a short time later. The strobe clock determines the time at which the input signal is sampled by clocking the output of the differential amplifier into the D-type flip-flop. The output control, when high, sets the output to the high-impedance state.

The SN75281 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	7 V
Supply voltage V_{CC-}	–7 V
Voltage at either sense input	±5 V
Differential sense input voltage (see Note 2)	±5 V
Voltage at any control input	7 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3)	800 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	–65°C to 150°C
Lead temperature 1/16 inch (1.6 mm) from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch (1.6 mm) from case for 10 seconds: N package	260°C

NOTES: 1. Voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential input voltages are at A+ with respect to A–.
3. Above 52°C free-air temperature, derate the J package at the rate of 8.2 mW/°C.
Above 63°C free-air temperature, derate the N package at the rate of 9.2 mW/°C.

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TYPE SN75281
BUBBLE-MEMORY SENSE AMPLIFIER

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage V_{CC+}	4.75	5	5.25	V
Supply voltage V_{CC-}	−4.75	−5	−5.25	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at 0°C to 70°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_T	Differential input threshold voltage	$V_{CC\pm}$ = ±5 V, T_A = 25°C	0.8	1.0	1.2	mV
V_{IH}	High-level input voltage (control inputs)		2			V
V_{IL}	Low-level input voltage (control inputs)				0.8	V
V_{OH}	High-level output voltage	$V_{CC\pm}$ = ±4.75 V, I_{OH} = −400 μA, Output control at 0.8 V	2.4			V
V_{OL}	Low-level output voltage	$V_{CC\pm}$ = ±4.75 V, I_{OL} = 10 mA, Output control at 0.8 V		0.5	0.8	V
I_{IH}	High-level input current (control inputs)	$V_{CC\pm}$ = ±5.25 V, V_I = 4 V			20	μA
I_{IL}	Low-level input current (control inputs)	$V_{CC\pm}$ = ±5.25 V, V_{IL} = 0			−0.4	mA
z_i	Input impedance	f = 2 MHz		2		kΩ

†All typical values are at $V_{CC\pm}$ = ±5 V, T_A = 25°C.

timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER			MIN	MAX	UNIT
t_{su}	Data setup time (see Figure 2)	sense input high to strobe clock high	15		ns
		sense input high to restore high	25		
t_h	Data hold time, restore high to sense input low (see Figure 2)		15		ns
t_{RLAH}	Delay time, restore low to sense input high (see Figure 2)		30		ns
t_r	Rise time, restore and strobe clock inputs (see Figure 2)			100	ns
t_f	Fall time, restore and strobe clock inputs (see Figure 2)			100	ns

switching characteristics at $V_{CC\pm}$ = ±5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 4 kΩ, C_L = 25 pF, See Figures 1, 3, and 4	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output		20	ns
t_{PZH}	Output enable time to high level		30	ns
t_{PZL}	Output enable time to low level		30	ns
t_{PHZ}	Output disable time from high level		10	ns
t_{PLZ}	Output disable time from low level		10	ns

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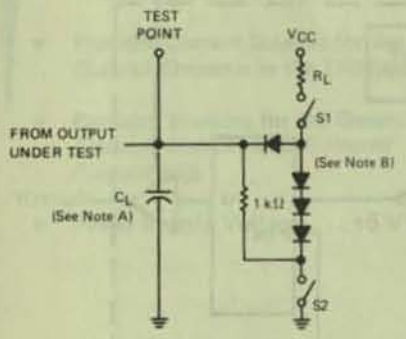
PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.

FIGURE 1–LOAD CIRCUIT

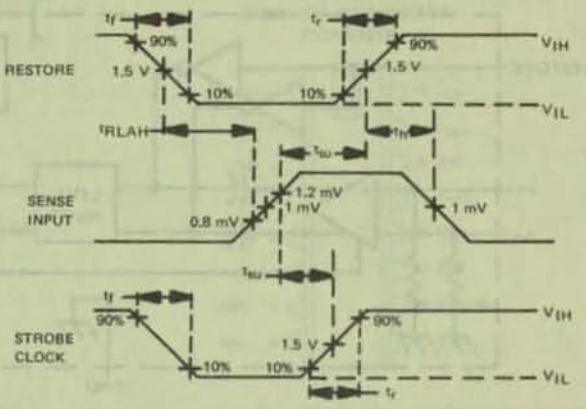


FIGURE 2–VOLTAGE WAVEFORMS, SETUP, HOLD, AND RESTORE TIMES

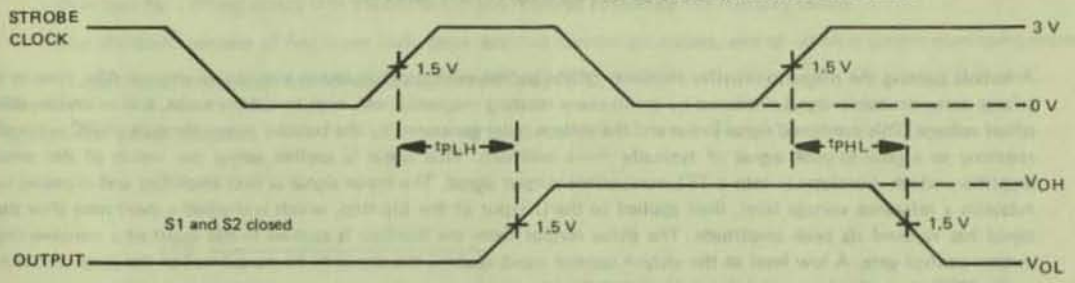
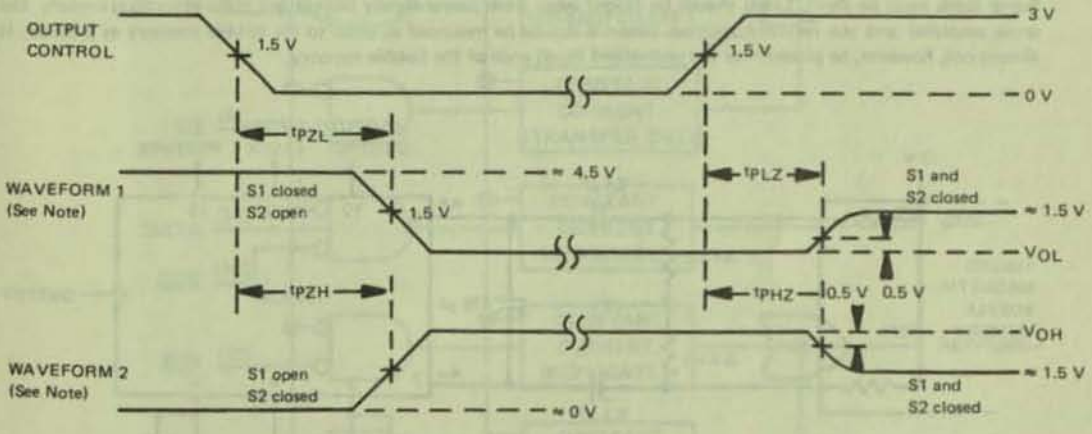


FIGURE 3–VOLTAGE WAVEFORMS, PROPAGATION DELAY TIMES



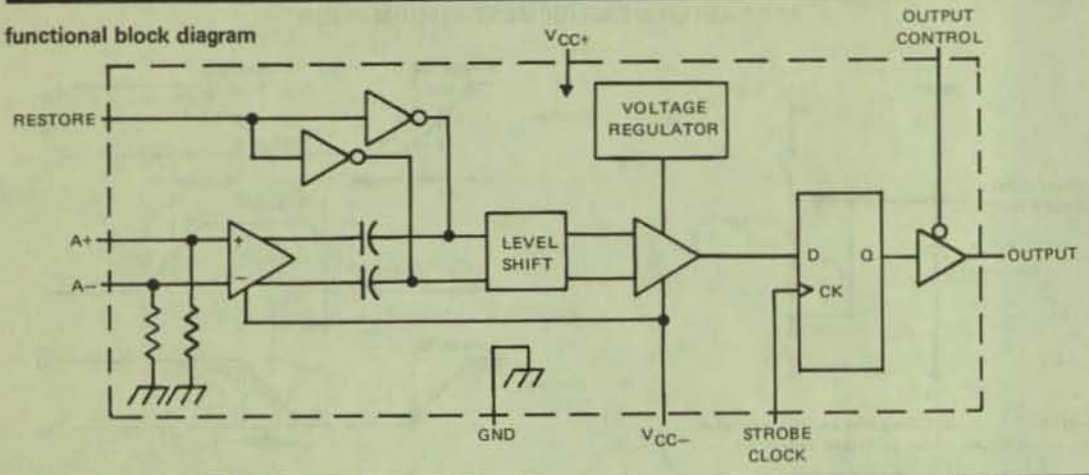
NOTE: Waveform 1 shows the output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 shows the output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 4–VOLTAGE WAVEFORMS, ENABLE AND DISABLE TIMES

All input pulses are supplied by generators having the following characteristics: $t_r \leq 7$ ns, $t_f \leq 7$ ns, PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$.

TYPE SN75281
BUBBLE-MEMORY SENSE AMPLIFIER

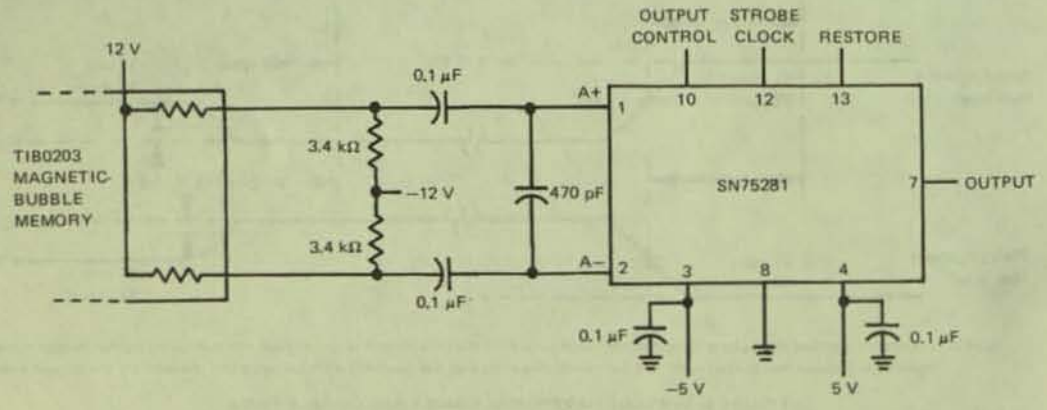
functional block diagram



TYPICAL APPLICATION DATA

A bubble passing the magneto-resistive elements on the bubble-memory chip causes a resistance change. Also present is a large common-mode signal produced by the in-plane rotating magnetic field, high-frequency noise, and an undesirable offset voltage. This combined signal (noise and the voltage pulse generated by the bubble) passes through an RC network resulting in a peak-to-peak signal of typically three millivolts. This signal is applied across the inputs of the sense amplifier, which translates it into a TTL-compatible output signal. The input signal is first amplified and clamped to establish a reference voltage level, then applied to the D input of the flip-flop, which is clocked a short time after the signal has reached its peak amplitude. The pulse output from the flip-flop is applied to the input of a noninverting output-control gate. A low level at the output-control input enables the signal to be passed out of the sense amplifier to the MOS controller integrated circuit.

Signal leads must be short. Leads should be placed away from power-supply lines or any noise-generating circuits. The sense amplifier and the resistor/capacitor network should be mounted as close to the bubble memory as possible. It should not, however, be placed near the unshielded (lead) ends of the bubble memory.



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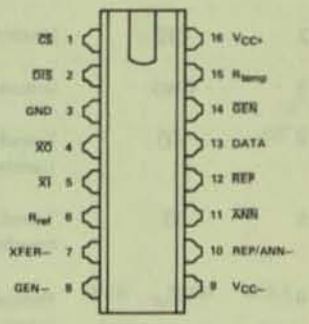
TYPE SN75380
BUBBLE-MEMORY FUNCTION DRIVER

NOVEMBER 1978

- TTL-Compatible Inputs
- Provides Current Sources for the Control Elements in the TIB0203
- Provides Tracking for the Generate Element with Minimal External Components
- Power Supply Voltages . . . +5 V and −12 V

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



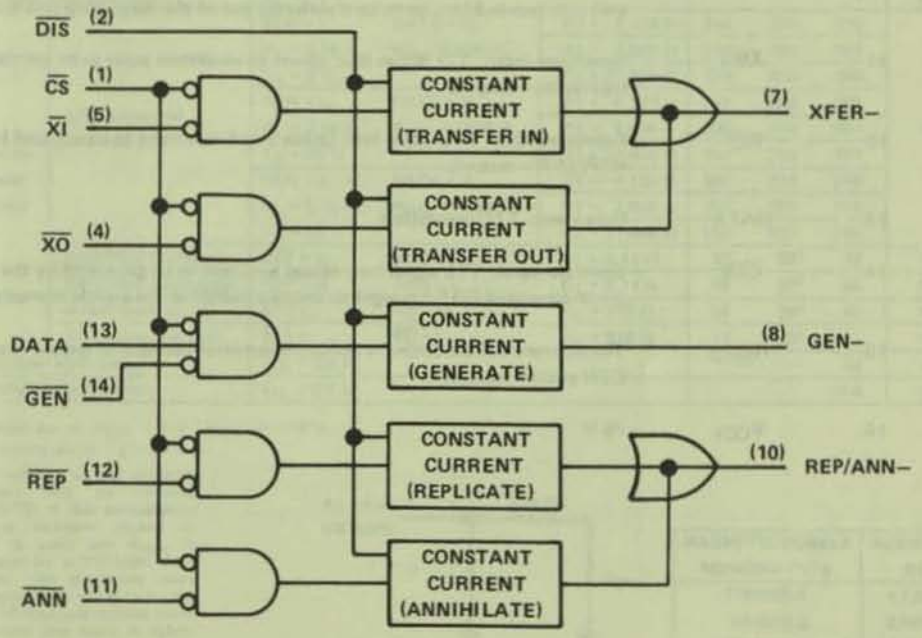
description

The SN75380 is a 16-pin dual-in-line device with constant-current outputs for driving the transfer gate, generator element, and replicate element of a magnetic-bubble memory. The function driver converts the digital control pulses generated by a timing circuit into the current pulses required to operate the memory device.

The SN75380 consists of five input logic gates and five current generators, one of which is temperature compensated.

The SN75380 is characterized for operation from 0°C to 70°C.

functional block diagram



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TEXAS INSTRUMENTS
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TYPE SN75380
BUBBLE-MEMORY FUNCTION DRIVER

PIN NO.	SIGNATURE	DESCRIPTION
1	$\overline{CS}$	Chip-select input: TTL active low.
2	$\overline{DIS}$	Disable input: TTL active low; disables all current sink outputs.
3	GND	Ground
4	$\overline{XO}$	Transfer-out enable input: TTL active low; enables bubbles in the minor loop to be transferred into the major loop.
5	$\overline{XI}$	Transfer-in enable input: TTL active low; enables bubbles in the major loop to be transferred into the minor loop.
6	R_{ref}	Reference resistor; 1% resistor to-ground sets the XFER– and REP/ANN– output currents.
7	XFER–	Transfer output; provides a current pulse that generates a transfer (in or out) operation in the bubble memory.
8	GEN–	Generate output; provides a current pulse that generates a magnetic domain inversion in the bubble memory.
9	V_{CC-}	–12 V
10	REP/ANN–	Replicate/annihilate output: provides two different types of current pulses that, depending on amplitude or timing, cause the bubble at the replicator either to be split into two bubbles, or to be transferred out of the major loop and eliminated.
11	$\overline{ANN}$	Annihilate input: TTL active low; causes an annihilate pulse to be emitted from the REP/ANN– output.
12	$\overline{REP}$	Replicate input: TTL active low; causes a replicate pulse to be emitted from the REP/ANN– output.
13	DATA	Data input: TTL compatible
14	$\overline{GEN}$	Generate input: TTL active low; causes a current to be generated by the function driver (provided DATA is high) to create a bubble in the bubble memory.
15	R_{temp}	Temperature compensation; a resistor/thermistor network to ground that sets the GEN output current.
16	V_{CC+}	+5 V

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	7 V
Supply voltage V_{CC-}	−13 V
Input voltage	5.5 V
High-level output voltage	15 V
Continuous total dissipation	600 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch (1.6 mm) from case for 10 seconds	260°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage V_{CC+}	4.75	5	5.25	V
Supply voltage V_{CC-}	−11.4	−12	−12.6	V
Operating free-air temperature	0		70	°C

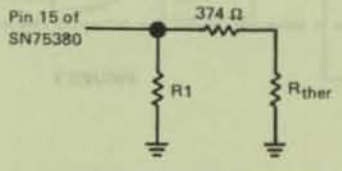
Caution: Permanent damage may be done to the bubble memory if specified pulse widths for the function timing generator are exceeded.

electrical characteristics over recommended ranges of V_{CC+}, V_{CC-}, and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage					2			V
V_{IL}	Low-level input voltage							0.8	V
$I_{O(off)}$	Off-state output current		V_O = 12 V					1	mA
$I_{O(on)}$	On-state output current	GEN (generate) See Note 2	GEN = L, R_L = 3.16 Ω, T_A = 0°C	DATA = H, R_{ther} = 826 Ω,	R1 = 4,120 Ω	264	290	316	mA
					R1 = 2,000 Ω	328	360	392	
					R1 = 27,400 Ω	214	235	256	
			GEN = L, R_L = 3.16 Ω, T_A = 25°C	DATA = H, R_{ther} = 1000 Ω,	R1 = 4,120 Ω	241	265	289	
					R1 = 2,000 Ω	305	335	365	
					R1 = 27,400 Ω	191	210	229	
			GEN = L, R_L = 3.16 Ω, T_A = 70°C	DATA = H, R_{ther} = 1366 Ω,	R1 = 4,120 Ω	200	220	240	
					R1 = 2,000 Ω	264	290	316	
					R1 = 27,400 Ω	150	165	180	
		REP/ANN (replicate)	$\overline{REP}$ = L,	$\overline{ANN}$ = H,	R_L = 5.11 Ω	72	80‡	88	mA
		REP/ANN (annihilate)	$\overline{REP}$ = H,	$\overline{ANN}$ = L,	R_L = 5.11 Ω	54	60‡	66	mA
		XFER (transfer in)	$\overline{XI}$ = L,	$\overline{XO}$ = H,	R_L = 316 Ω	34	38‡	42	mA
		XFER (transfer out)	$\overline{XI}$ = H,	$\overline{XO}$ = L,	R_L = 316 Ω	34	38‡	42	mA
I_{IH}	High-level input current		V_{IH} = 2.4 V					20	μA
I_{IL}	Low-level input current		V_{IL} = 0.4 V					−0.4	mA

†All typical values are at V_{CC+} = 5 V, V_{CC-} = −12 V.
‡These typical values are at T_A = 25°C.

NOTE 2: The current to the generate element will be reduced 1 mA/°C if the temperature sensing network shown at right is used and R_{ther} is replaced by a TSP102F thermistor. The particular value of resistor R1 depends on the type of magnetic-bubble memory used (see table at right).



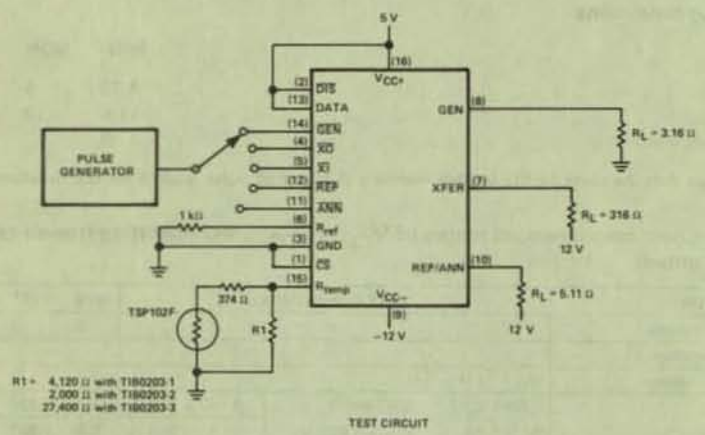
Resistors must be 1% tolerance.

MAGNETIC-BUBBLE MEMORY TYPE	RESISTOR R1
TIB0203-1	4,120 Ω
TIB0203-2	2,000 Ω
TIB0203-3	27,400 Ω

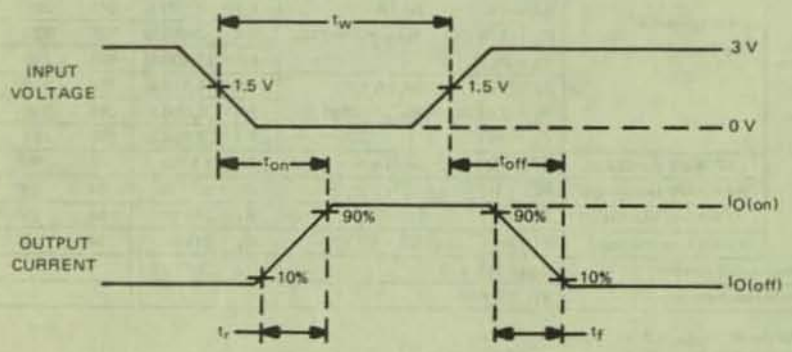
switching characteristics at V_{CC+} = 5 V, V_{CC-} = −12 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{on}	Turn-on time	See Figure 1		125		ns
t_{off}	Turn-off time			125		ns
t_r	Rise time			50		ns
t_f	Fall time			50		ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



WAVEFORMS

NOTE: The input pulse is supplied by a generator having the following characteristics: $t_r \leq 7$ ns, $t_f \leq 7$ ns, $t_w \geq 400$ ns, duty cycle ≤ 2%, Z_{out} = 50 Ω.

FIGURE 1

TEXAS INSTRUMENTS
INCORPORATED
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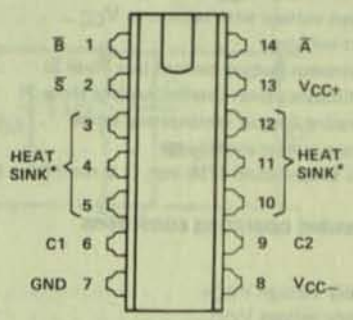
TYPE SN75382
BUBBLE-MEMORY COIL DRIVER

NOVEMBER 1978

- Two High-Current Totem-Pole Outputs
- TTL-Compatible Inputs
- NE Package with Power Dissipation Capability of up to 2 W
- Two Power Supplies . . . +5 V and −12 V

NE
DUAL-IN-LINE PACKAGE
(TOP VIEW)



*Internally connected to V_{CC-}

description

The SN75382 is a monolithic integrated circuit with two totem-pole outputs capable of supplying the high peak current required in bubble memory coils.

Inputs $\overline{A}$ and $\overline{B}$ are TTL compatible and are driven with pulses from a function timing generator. The TTL input pulses pass through gates to drive level-shift circuits that in turn control the current source/sink outputs.

Enabling of the gates is controlled by the $\overline{S}$ input.

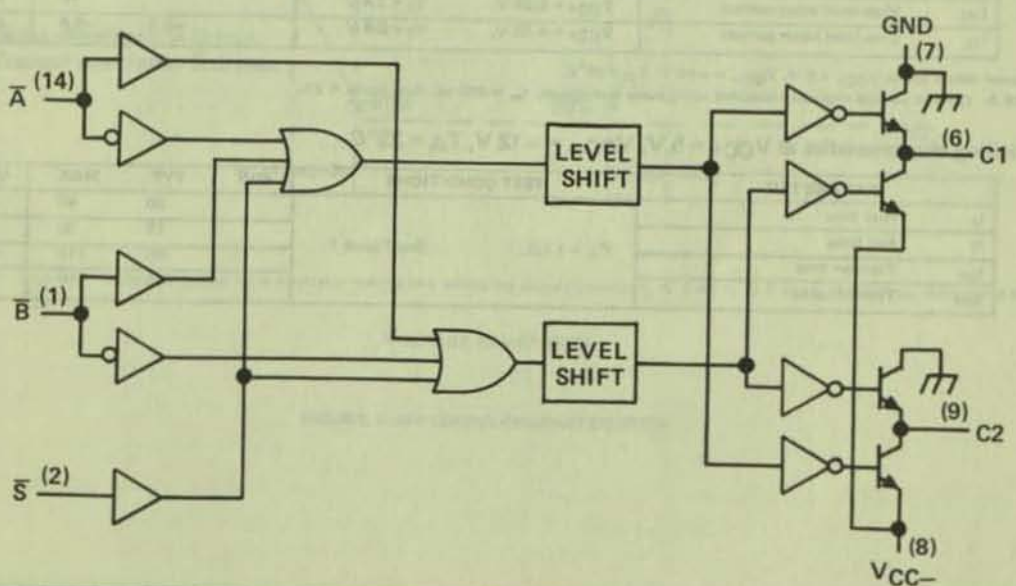
The SN75382 is characterized for operation from 0°C to 70°C. It is supplied in the NE package with a copper lead frame that allows it to operate with a power dissipation of up to two watts.

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{A}$	$\overline{B}$	$\overline{S}$	C1	C2
X	X	H	Z	Z
L	L	L	Z	Z
L	H	L	≈ V_{CC-}	≈ Gnd
H	L	L	≈ Gnd	≈ V_{CC-}
H	H	L	Z	Z

H = high level, L = low level, X = irrelevant,
Z = high impedance (off)

functional block diagram



TEXAS INSTRUMENTS
INCORPORATED
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TYPE SN75382
BUBBLE-MEMORY COIL DRIVER

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1) . . . . . 6 V
Supply voltage V_{CC-} . . . . . −14 V
Output voltage with respect to V_{CC-} . . . . . 15 V
Input voltage . . . . . 5.5 V
Continuous output current (see Note 2) . . . . . −400 mA
Continuous power dissipation (see Note 3) . . . . . 2 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1.6 mm) from case for 10 seconds . . . . . 260°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage V_{CC+}	4.75	5	5.25	V
Supply voltage V_{CC-}	−11.4	−12	−12.6	V
Peak output current, I_{OM} (see Note 4)		±490	±550	mA

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise noted.
2. Derate linearly to 150 mA at 70°C at the rate of 5.56 mA/°C.
3. Above 29°C, derate linearly to 1325 mW at 70°C at the rate of 16.6 mW/°C.
4. Output current values are for ramp waveforms as shown in Figure 2.

electrical characteristics at 0°C to 70°C free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{OD}	Differential output voltage	V_{CC-} = −11.4 V, I_O = 450 mA, $\overline{A}$ (or $\overline{B}$) and $\overline{S}$ at 0 V, See Note 5	±10	±10.4		V
I_I	Maximum current at maximum input voltage	V_{CC+} = 5.25 V, V_I = 5.5 V			0.1	mA
I_{IH}	High-level input current	V_{CC+} = 5.25 V, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC+} = 4.75 V, V_I = 0.4 V		−0.5	−0.8	mA

†Typical values are at V_{CC+} = 5 V, V_{CC-} = −12 V, T_A = 25°C.
NOTE 5: Output voltage must be measured using pulse techniques. t_w ≈ 300 ns, duty cycle < 2%.

switching characteristics at V_{CC+} = 5 V, V_{CC-} = −12 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	R_L = 1 kΩ, See Figure 1		20	40	ns
t_f	Fall time			15	30	ns
t_{on}	Turn-on time			65	110	ns
t_{off}	Turn-off time			60	100	ns

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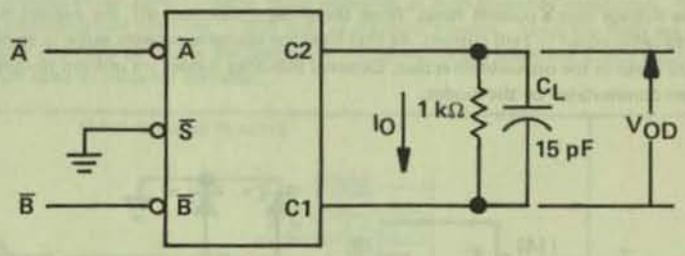
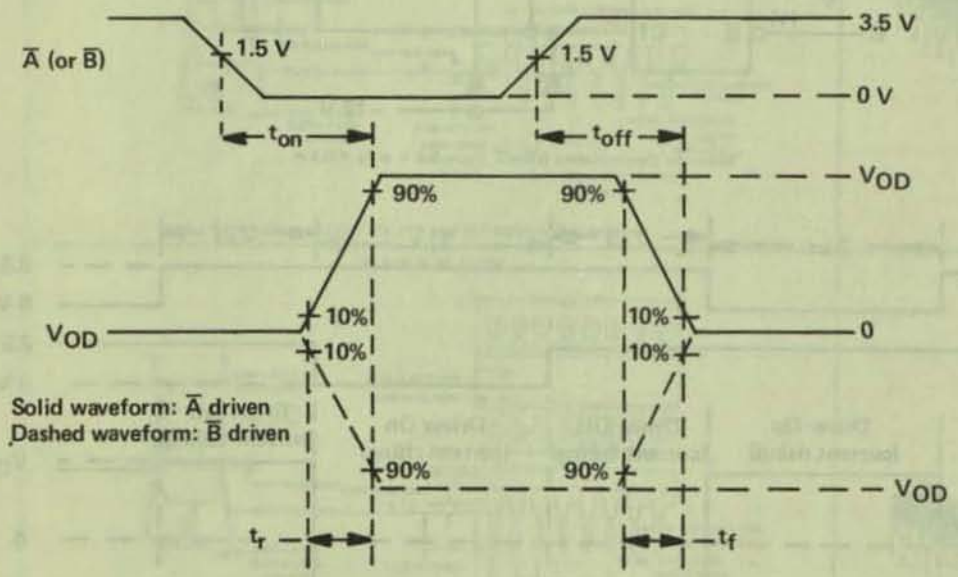
PARAMETER MEASUREMENT INFORMATION



NOTE: C_L includes probe and jig capacitance.

TEST CIRCUIT



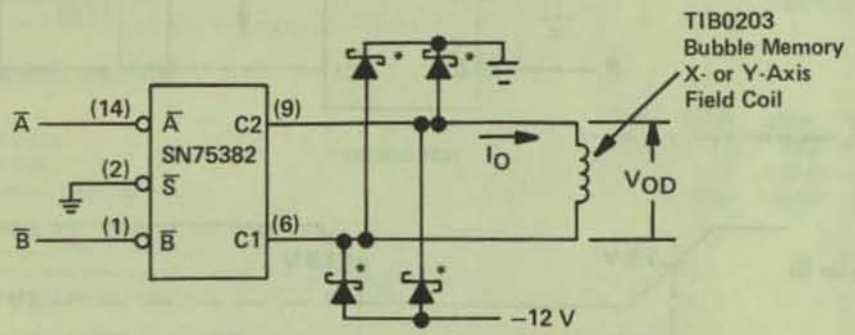
NOTE: The input pulse is supplied by a generator having the following characteristics: $t_r \leq 7$ ns, $t_f \leq 7$ ns, $t_w = 300$ ns, duty cycle ≤2%, $Z_{out} = 50\ \Omega$.

VOLTAGE WAVEFORMS

FIGURE 1–SWITCHING CHARACTERISTICS

TYPICAL APPLICATION DATA

The coil-driver circuit is used to generate triangular current waveforms for the bubble-memory coils. The currents are generated by switching the coil driver in such a way that a voltage pulse is applied to the coil. The coil inductance integrates the voltage into a current ramp. When the pulse is switched off, the current is commutated by two diodes and allowed to ramp down to zero current. At that time the opposite-polarity pulse is applied to the coil, which causes the current to ramp in the opposite direction. External Schottky diodes are utilized to minimize the voltage drop across the coils when commutated by the diodes.



*Schottky Commutating Diodes: $V_F \leq 0.5$ V at $I_F = 0.5$ A

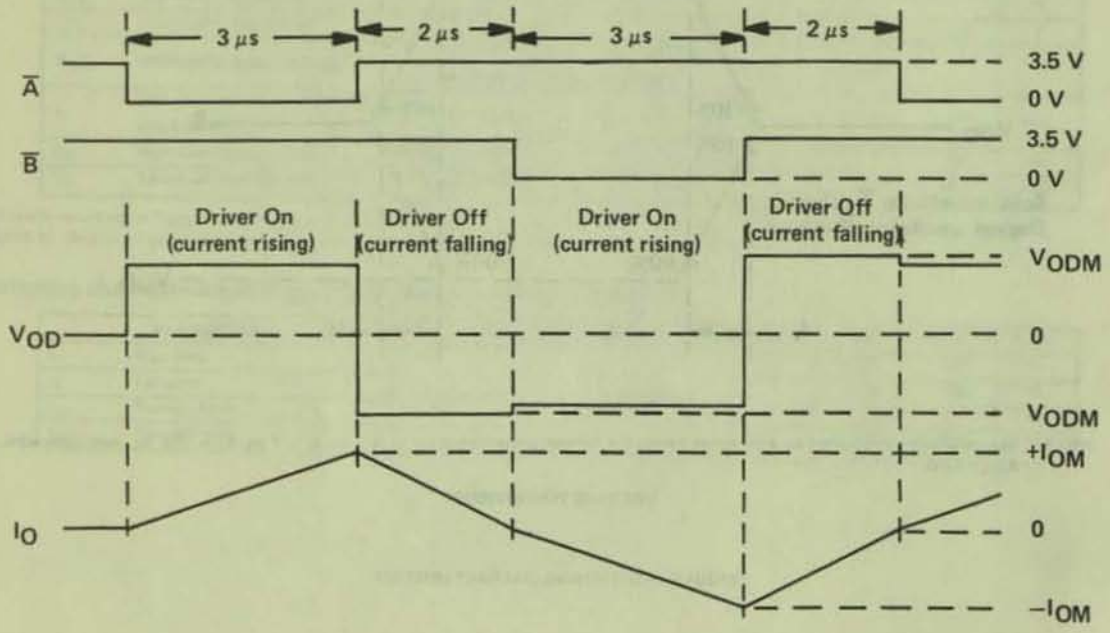


FIGURE 2

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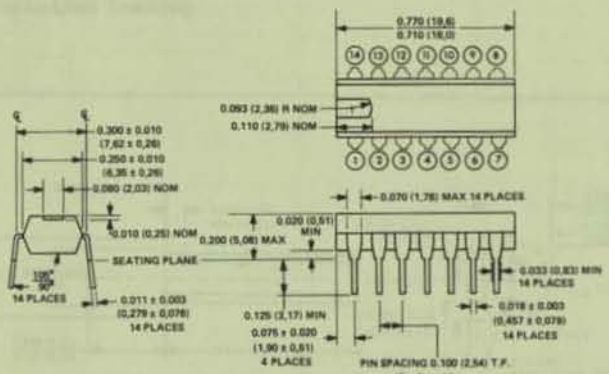
N and NE plastic dual-in-line packages

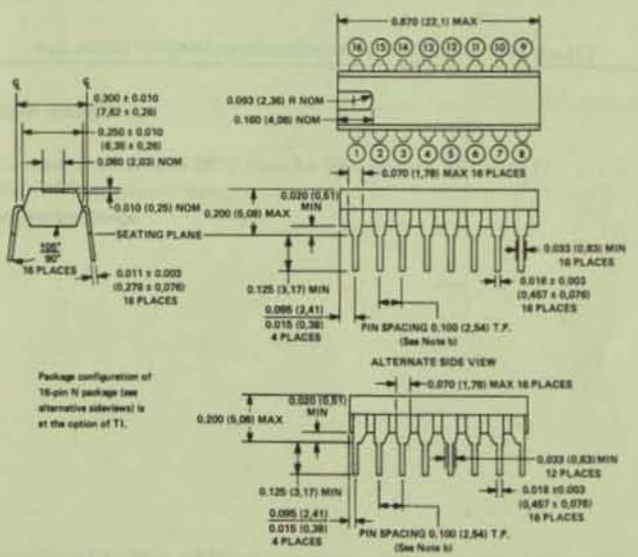
These dual-in-line packages consist of a circuit mounted on a 14- or 16-lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 0.300-inch (7,62-mm) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

14-PIN N and NE PLASTIC



Falls within JEDEC TO-116 and MO-001AA Dimensions

16-PIN N PLASTIC



NOTES: a. All dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.

b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

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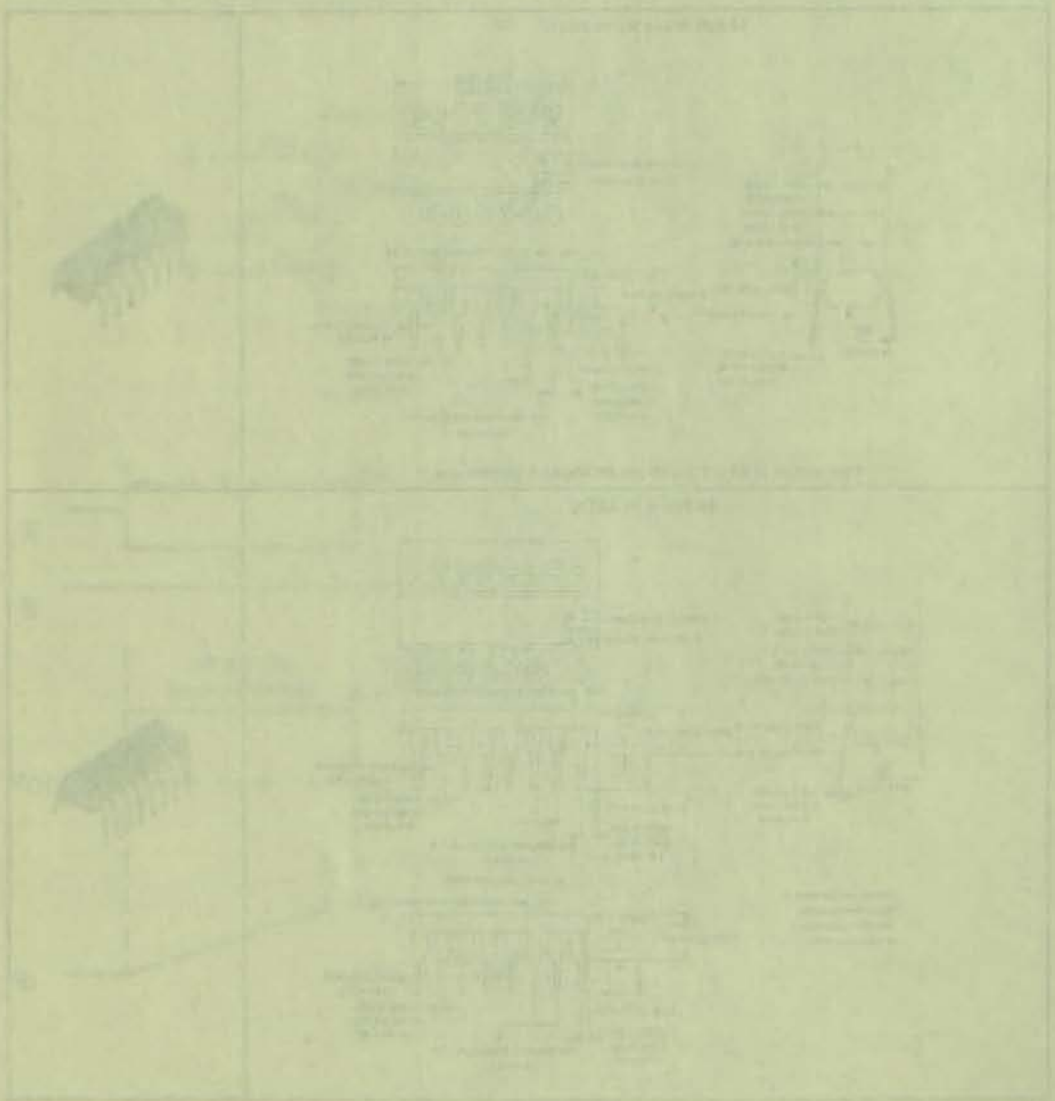


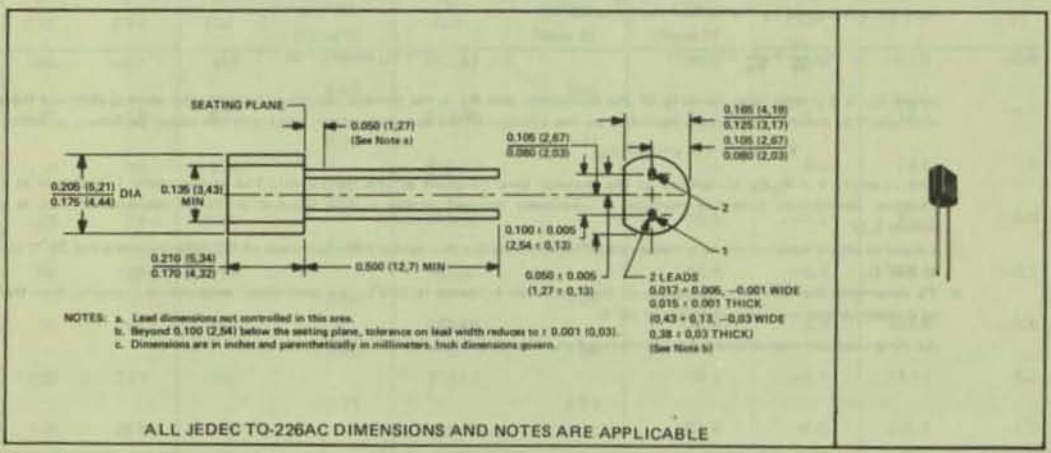
TYPE TSP102
POSITIVE-TEMPERATURE-COEFFICIENT SILICON THERMISTOR

BULLETIN NO. DL-S 12507, JUNE 1977—REVISED JUNE 1978

PTC TEMPERATURE SENSOR

- Planar Technology Employing Spreading-Resistance Principle*
- Large Positive Temperature Coefficient of Resistance . . . Approx 0.7 %/°C
- 1000-Ω Nominal Resistance Value at 25°C
- Available in ±1%, ±2%, ±5%, and ±10% Tolerances†
- Close Unit-to-Unit Tracking

Mechanical data



ALL JEDEC TO-226AC DIMENSIONS AND NOTES ARE APPLICABLE

absolute maximum ratings

Continuous Current at (or below) 25°C Free-Air Temperature (See Note 1)	10 mA
Operating Free-Air Temperature Range	−55°C to 125°C
Storage Temperature Range	−65°C to 150°C

NOTE 1: Derate linearly to 2 mA at 125°C, see Figure 3. In general, sensing current should be maintained at or below 2 mA at all temperatures to reduce self-heating and nonlinearity of response.

*Patent pending

†Tolerance is ±1% for TSP102F, ±2% for TSP102G, ±5% for TSP 102J, and ±10% for TSP102K. If no suffix is added, the ±10% tolerance is assumed. The tolerance applies to the resistance at 25°C and not to the temperature coefficient of resistance. Zero-power resistance ratios are independent of tolerance.

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TYPE TSP102
POSITIVE-TEMPERATURE-COEFFICIENT SILICON THERMISTOR

electrical and thermal characteristics

		MIN	TYP	MAX	UNIT
$R_{25°C}$	Resistance at $T_A = 25°C$		1000 Nom†		Ω
$R_{125°C}/R_{25°C}$	Zero-Power Resistance Ratio	1.89	1.92	1.95	
$R_{-55°C}/R_{25°C}$	Zero-Power Resistance Ratio	0.496	0.501	0.506	
τ_L	Thermal Time Constant, Liquid-to-Liquid (See Notes 2 and 3)		4.3	5	s
τ_A	Thermal Time Constant, Free-Air (See Notes 2 and 4)		30	35	s

†Tolerance is ±1% for TSP102F, ±2% for TSP102G, ±5% for TSP102J, and ±10% for TSP102K. If no suffix is added, the ±10% tolerance is assumed.

NOTES: 2. The thermal time constant of a thermistor, analogous to the R·C time constant of a circuit containing resistance and capacitance, is defined as that time interval in which the thermistor temperature undergoes a change equal to 63.2% of an externally applied step change in temperature. The time constants cited here were obtained by transferring the thermistor, with negligible time delay, from a medium at temperature T_0 to a medium of the same composition at temperature T_1. The instantaneous thermistor temperature is given by the differential equation:

$$C_\theta \frac{dT}{dt} = \frac{1}{R_\theta}(T_1 - T) \qquad (T = T_0 \text{ when } t = 0)$$

where C_θ is the total heat capacity of the thermistor and R_θ is the thermal resistance between the sensing chip and the external medium. The thermal response is described by the solution of the above equation, subject to the stated boundary condition:

$$T = (T_0 - T_1)\, e^{-t/\tau} + T_0$$

The quantity $\tau = R_\theta C_\theta$ is defined as the thermal time constant of the thermistor. The temperature T is shown in Figure 1. Thermal equilibrium with the medium is essentially reached within a time interval of 5τ. A response of 90% is achieved within 2.3τ.

3. Liquid-to-liquid time constant is measured by transferring the thermistor from one bath of DC-200 silicone oil at 25°C to another at 100°C.
4. To determine the free-air time constant, the thermistor is heated to 100°C in a controlled-temperature chamber, then transferred to a room-temperature environment at 25°C.

All time-constant measurements are performed at a constant current of 1 mA through the thermistor.

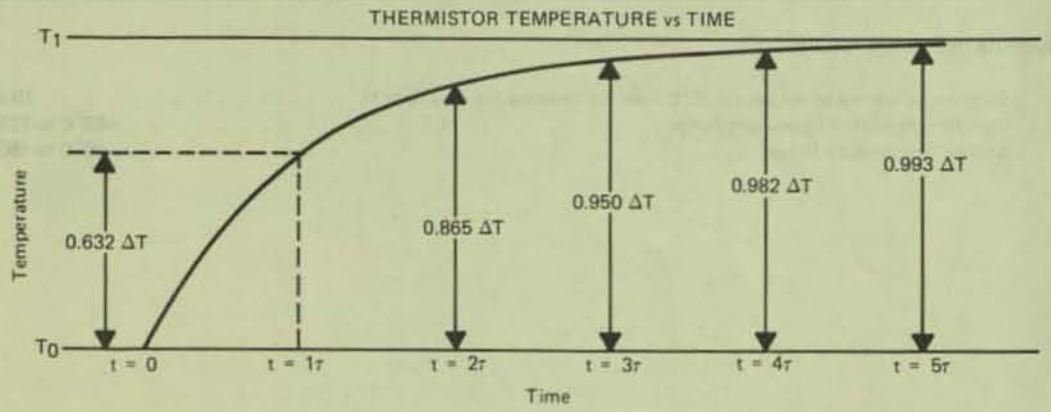

FIGURE 1

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LINEARIZATION OF RESISTANCE VS TEMPERATURE CHARACTERISTICS

The change of resistance with temperature can be made very nearly linear by connecting a 2370-ohm resistor in parallel with the thermistor.

In the tables it is assumed that the shunt resistor is exactly 2370 ohms at all temperatures. R_p is the equivalent parallel resistance calculated from $R_p = 2370\ R/(2370 + R)$ and T' is the temperature calculated from $T'\ (°C) = (R_p - 612.6)/3.601$. Table 1 shows the error in both Celsius and Fahrenheit degrees introduced by assuming perfect linearity for a thermistor having nominal resistance at 25°C and a typical slope of resistance versus temperature. Table 2 takes into account the minimum and maximum values of zero-power resistance ratio.

TABLE 1

T (°C)	T (°F)	R (Ω)	α_R (Ω/°C) (Note 1)	R_p (Ω)	α_{RP} (Ω/°C) (Note 5)	T' (°C) (Note 6)	T − T' (°C)	T' (°F)	T − T' (°F)
−55	−67	501		413.57		−55.3	+0.3	−67.5	+0.5
			5.63		3.63				
−25	−13	670		522.34		−25.1	+0.1	−13.1	+0.1
			6.24		3.61				
0	32	826		612.52		0.0	0.0	32.0	0
			6.96		3.63				
25	77	1000		703.26		25.2	−0.2	77.3	−0.3
			7.76		3.63				
50	122	1194		793.99		50.4	−0.4	122.7	−0.7
			8.60		3.59				
75	167	1409		883.65		75.3	−0.3	167.5	−0.5
			9.68		3.58				
100	212	1651		973.11		100.1	−0.1	212.2	−0.2
			10.76		3.50				
125	257	1920		1060.70		124.4	+0.6	256.0	+1.0

NOTES: 5. The temperature coefficients are the average slopes for the indicated temperature intervals and are calculated from:

$$\alpha_R = \frac{(R @ T_2) - (R @ T_1)}{T_2 - T_1}$$

6. A linear regression on R_p yields 612.6 Ω at 0°C with a slope of 3.601 Ω/°C. Therefore:

$$T'(°C) = (R_p - 612.6)/3.601$$

TABLE 2

TRUE TEMPERATURE (°C)	TRUE TEMPERATURE (°F)	THERMISTOR RESISTANCE (Ω)	INDICATED TEMPERATURE (°C)	ERROR (°C)	INDICATED TEMPERATURE (°F)	ERROR (°F)
		*496	−56.0	+1.0	−68.8	+1.8
−55	−67	501	−55.0		−67.0	
		*506	−54.0	−1.0	−65.2	−1.8
		*1890	122.2	+2.8	252.0	+5.0
125	257	1920	125.0		257.0	
		*1950	127.7	−2.7	261.9	−4.9

*These lines of data represent a thermistor having nominal resistance (1000 Ω) at 25°C, but different slopes of resistance versus temperature corresponding to the minimum and maximum values of zero-power resistance ratio. A system calibrated to read −55.0°C and 125.0°C when the resistance values are 501 ohms and 1920 ohms, respectively, will yield the "Indicated Temperature" readings when the resistance is actually the value shown under "Thermistor Resistance."

TYPICAL CHARACTERISTICS

RESISTANCE
vs
THERMISTOR TEMPERATURE

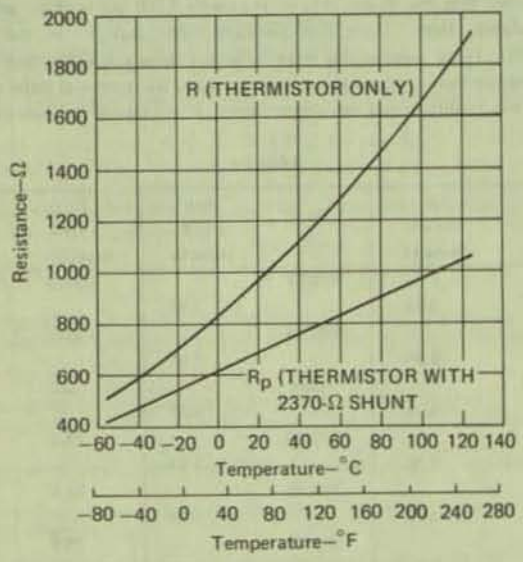

FIGURE 2

THERMAL INFORMATION

CURRENT DERATING CURVE

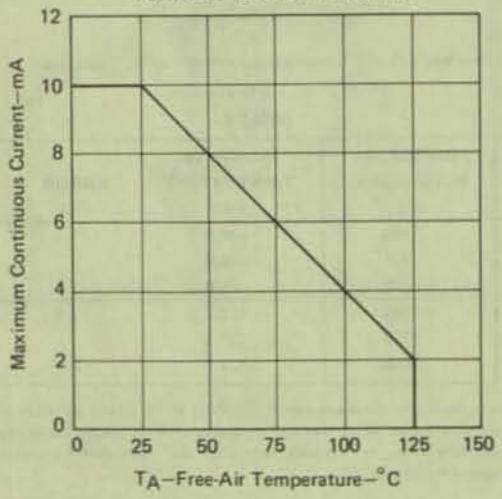

FIGURE 3

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DLS-079/JUNE 1978

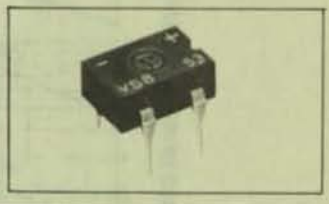
SCHOTTKY DIB 750 mA DUAL IN-LINE BRIDGE

10v, 20v, 30v AND 40 v V_{RRM}

.65VOLT v_f PER DIODE AT 750 mA

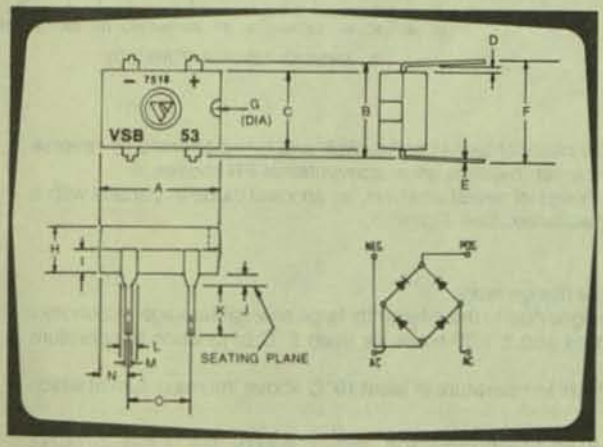
STANDARD .10" — 2,54MM DIP LEAD SPACING
2 DIBS WILL FIT INTO STANDARD 14 PIN DIP SOCKET

MOISTURE RESISTANT EPOXY CASE



MAXIMUM RATINGS AT $T_A = 25°C$ (unless otherwise specified)	SYMBOL	VSB51	VSB52	VSB53	VSB54	UNITS
DC Blocking Voltage Working Peak Reverse Voltage Peak Repetitive Reverse Voltage	V_{RM} V_{RWM} V_{RRM}	10	20	30	40	Volts
RMS Reverse Voltage	$V_{R(RMS)}$	7	14	21	28	Volts
Peak Surge Current, 100 μ Sec. Pulse Width (non-rep) and $T_A = 40°C$	I_{FSM}	75				Amps
Peak Surge Current, ½ cycle at 60 Hz and $T_A = 40°C$	I_{FRM}	30				Amps
DC Forward Current at $T_A = 40°C$	I_O	750				mA
Junction Operating and Storage Temperature Range	T_J, T_{STG}	−50 to +150				°C
Max Soldering Temperature and Time		5 sec. at 265°C				

ELECTRICAL CHARACTERISTICS (At $T_A = 25°C$ unless otherwise noted)	SYMBOL	VSB51	VSB52	VSB53	VSB54	UNITS
Maximum Instantaneous Forward Voltage Drop (per Diode @ 750 mA) $I_F = 0.1$ Amp $I_F = 0.5$ Amp $I_F = 0.75$ Amp	V_f	.41 .56 .65				Volts
Maximum Reverse Current (per diode) at Rated V_{RRM} and $T_A = 100°C$	I_{RM}	3				mA



LTR	INCHES	MILLIMETERS
A	.370-.390	9,40-9,91
B	.280-.320	7,11-8,13
C	.240-.260	6,10-6,60
D	.010-.020	0,25-0,51
E	.008-.015	0,20-0,38
F	.380 MAX	9,65 MAX
G	.057-.067	1,45-1,70
H	.140-.160	3,56-4,06
I	.070-.080	1,78-2,03
J	.055 MAX	1,40 MAX
K	.120-.130	3,05-3,30
L	.040-.060	1,02-1,52
M	.016-.020	0,41-0,51
N	.080-.100	2,03-2,54
O	.190-.210	4,83-5,33

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FIG. 1

TYPICAL REVERSE CURRENT

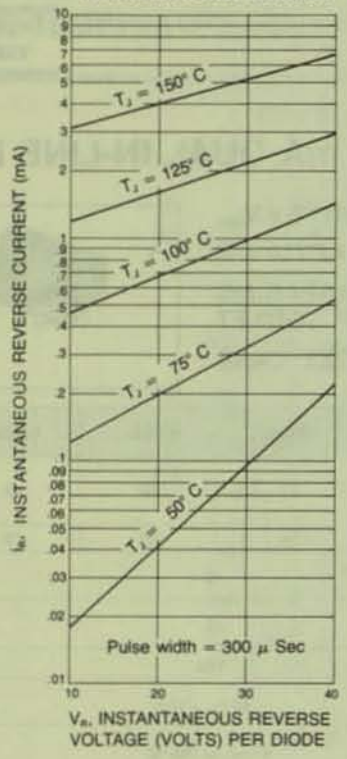


FIG. 2

TYPICAL FORWARD VOLTAGE

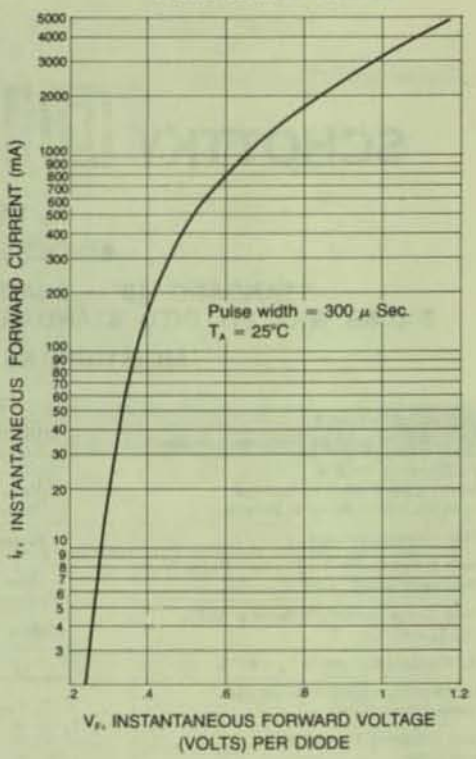


FIG. 3

CAPACITANCE VS. REVERSE VOLTAGE

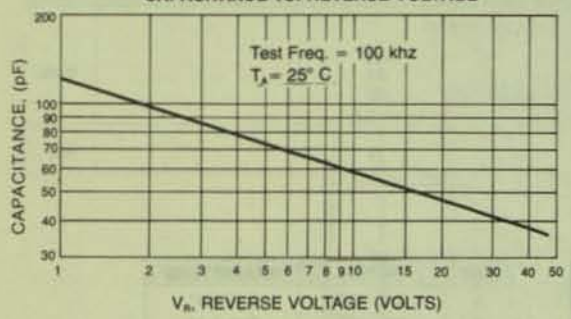
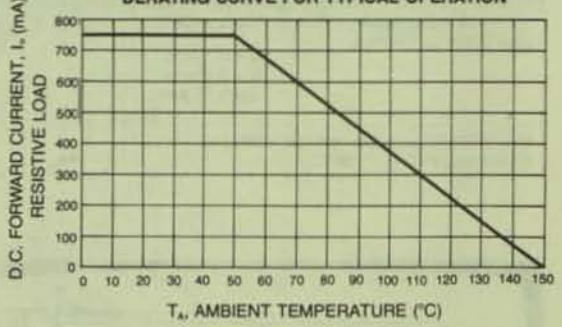


FIG. 4

DERATING CURVE FOR TYPICAL OPERATION



I. The current flow in a Schottky barrier rectifier is due to majority carrier conduction and is not affected by reverse recovery transients due to stored charge and minority carrier injection as in conventional PN diodes.
The Schottky barrier rectifier may be considered for purposes of circuit analysis, as an ideal diode in parallel with a variable capacitance equal in value to the junction capacitance. See Figure 3.

II. THERMAL CONSIDERATIONS

A. The derating curve of figure 4 may be used for initial design work.

B. Thermal runaway is entirely possible on marginal designs due to the inherently large reverse leakage of Schottky barrier rectifiers and the fact that reverse power multiplies about 1.32 times for each 5° C of junction temperature increase.

C. We recommend that all designs be verified at an ambient temperature at least 10° C above the maximum at which the equipment will ever have to operate.

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