SILICIDE RESISTORS FOR INTEGRATED CIRCUITS

BY

R. K. WAITS

Reprinted from the PROCEEDINGS OF THE IEEE
VOL. 59, NO. 10, OCTOBER, 1971
pp. 1425-1429

Silicide Resistors for Integrated Circuits

ROBERT K. WAITS

Abstract—Thin-film resistors are useful in monolithic integrated circuits whenever high sheet resistance (ρ_s>1 kΩ/sq) or radiation hardness are required. Silicide resistive films ($MoSi_2$, $CrSi_2$, and Si–Cr) deposited by dc sputtering have been shown to be compatible with monolithic circuit production and require no protective overlayer. Si–Cr films 200–300 Å thick have ρ_s and temperature coefficients of resistance (TCR) ranging from about 1 kΩ/sq and +150 ppm/°C ($CrSi_2$) to 20 kΩ/sq and −1400 ppm/°C (17 at % Cr). $MoSi_2$ is best suited for resistor applications requiring 100–200 Ω/sq. $MoSi_2$ films are about 700 Å thick at 200 Ω/sq, compared to <100 Å for 200-Ω/sq Ni–Cr, and their TCR is −125 ppm/°C. Typical stability for unprotected silicide resistors in TO-5 packages at 200°C, no load, is <±3 percent during the first 200 h and <±0.5 percent during the next 2000 h. The films are stable during short term exposure to high temperatures as encountered during monolithic or hybrid circuit ceramic package sealing.

Introduction

THIS PAPER describes a silicide thin-film resistor technology that has been developed to fill the need for 200-Ω/sq to 20-kΩ/sq thin-film resistors compatible with monolithic and hybrid integrated circuit production. The resistor process, film characteristics, reproducibility, life-test results, and examples of monolithic circuit applications will be described.

Why thin-film resistors? In most monolithic circuits thin-film resistors can be avoided by using semiconductor resistors or by clever circuit design. Table I summarizes the available technologies. One case where there is no reasonable alternative to thin-film resistors is in radiation-hardened circuits, since all semiconductor resistors become conductors in a radiation environment. A second application of thin-film resistors (at least for the time being) is in low-power circuits that require high-value resistors. Thin films can provide a high sheet resistance (ρ_s) while still having a reasonably low temperature coefficient of resistance (TCR). Using 150–200-Ω/sq diffused resistors in such applications takes an uneconomical amount of space. In the near future high-value resistors will be produced economically and reproducibly by ion implanting a thin n or p layer in a silicon substrate [1]. These semiconductor resistors, being about one-tenth as thick as a diffused resistor of comparable ρ_s, will have a higher doping concentration, and therefore a relatively low TCR. Implanted resistors will not, of course, be radiation-resistant. Semiconductor resistors, whether diffused, implanted, or bulk, are nonlinear at higher voltages and contribute parasitic capacitance.

Silicide resistor processes have been developed for three ρ_s ranges: 200 Ω/sq, 2 kΩ/sq, and 20 kΩ/sq. The 200-Ω/sq resistor is a molybdenum disilicide ($MoSi_2$) film which has a resistivity of 1300–2000 μΩ·cm (depending on substrate and deposition conditions). Thus a 200-Ω/sq film has a thickness of 650–1000 Å. The 2-kΩ/sq and 20-kΩ/sq resistors are silicon–chromium (Si–Cr) films containing approximately 43 wt % chromium and 27 wt % chromium, respectively. Chromium disilicide ($CrSi_2$) films have also been studied extensively. All films are deposited by dc diode sputtering. Table II lists some of the characteristics of silicide resistors. Silicide resistors should *not* be confused with Cr–SiO or other cermet-type films containing oxides.

TABLE I
RESISTOR TECHNOLOGIES

Sheet Resistivity Range	Thin Film	Semiconductor
200 Ω/sq	$MoSi_2$ Cr–SiO Ta Ni–Cr	diffused
2 kΩ/sq	Si–Cr Cr–SiO	implanted bulk diffused pinched
20 kΩ/sq	Si–Cr	implanted active loads buried layers

All the thin-film resistor technologies listed in Table I have limitations. Nickel–chromium (Ni–Cr), although well-established as a stable low TCR (usually ±50-ppm/°C) resistor is difficult (and expensive) to mass produce. The film thickness for 200 Ω/sq is 80–150 Å, and depends on film resistivity, which is determined by deposition technique and alloy composition [2]–[4]. (Ni–Cr or Nichrome* films described in the literature contain from 30 to 80 wt % nickel.) Such a thin film is readily consumed by residual chemicals (etchants, resist strippers), and process control must be stringent. Ni–Cr films also require some type of protective layer, such as SiO or SiO_2, to prevent oxidation and electrochemical reactions in moist environments.

Tantalum film resistors (β–Ta or TaN_2), as developed by Bell Laboratories, were originally designed for ρ_s values around 10 Ω/sq and thicknesses greater than 1000 Å [5]. Higher value resistors of β–Ta or TaN_2 require films nearly as thin as Ni–Cr. Low-density tantalum, deposited by low-voltage sputtering, has a higher film resistivity and can be used to achieve ρ_s values as high as 1000 Ω/sq, but the porosity of the film makes it susceptible to oxidation and a passivating film is required.

Chromium–silicon monoxide cermet (Cr–SiO) films have been used on monolithic circuits, and are suitable for the range 300 to 2000 Ω/sq [6], [7]. Because of their higher SiO content, reproducibility is poorer and delineation by etching is more difficult for Cr–SiO films having ρ_s>2 kΩ/sq [8], [9]. In one process that has been described [7], the Cr – SiO resistors are annealed at 450°C. Subsequent exposure to temperatures in excess of this value results in further annealing. This is a disadvantage if a one-step metallization (for monolithic circuits) or ceramic packaging is required. If aluminum is used to contact Cr–SiO films, as is desirable for monolithic circuits, an increase incontact resistance may occur under dc load for temperatures as low as 100°C [10].

In comparison with present Ni–Cr, Ta, and Cr–SiO resistors, the silicide resistors offer a potentially simpler process that will produce

Manuscript received February 11, 1971; revised April 26, 1971.
The author is with the Research and Development Laboratory, Fairchild Camera and Instrument Corporation, Palo Alto, Calif. 94304.

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TABLE II
SILICIDE RESISTOR CHARACTERISTICS

	$MoSi_2$	$CrSi_2$	Si–Cr	Si–Cr
Sheet resistivity (Ω/sq)	200	1300	2000	20 000
Thickness (Å)	650	300	200	225
Film resistivity ($\mu\Omega \cdot$ cm)	1300	2600	4000	45 000
Film composition wt % Si	37	52	57	73
at % Si	67	67	71	83
Avg TCR, 50–150°C (ppm/°C)	-125 ± 25	$+200 \pm 50$	-150 ± 50	-1400 ± 200
Stability[a]—200°C storage				
first 200 h	<1.5			3.2
next 1800 h	<0.2	0.46		0.21
Stability—125°C, 5×10^5 A/cm^2				
first 200 h		0.75[a]		
next 1800 h	0.77[b]	0.51[a]		
Reproducibility (absolute value)	±10%	±10%	±15%	±30%

[a] Average percent change.
[b] Maximum percent change after 10 000 h, 1.3×10^5 A/cm^2 (37 units).

resistors of comparable long-term stability and improved short-term high-temperature stability. A disadvantage of silicide resistors is that extensive reliability data are not yet available. Among thin-film resistors having $\rho_s > 10$ kΩ/sq there is no present alternative to Cr–Si [11].

SILICIDE RESISTOR PROCESS

The following summarizes the silicide resistor process sequence:

1) film deposition by dc diode sputtering;
2) contact metal deposition;
3) contact pattern delineation: photoresist, metal etch;
4) resistor pattern delineation: photoresist, resistor etch;
5) resistor anneal: nitrogen, 500–565°C, 5–15 min.

A. Film Deposition

Silicide films are deposited by dc diode sputtering in argon. Initially, silicide films were deposited by electron-beam evaporation, but reproducibility was poor. An automatic magazine-fed sputtering machine has been developed to allow high-volume production of sputtered films.[1] The substrates are placed on 10-cm diam carriers within a 7.5-cm diam area. The magazine capacity is 60 carriers. An automatic feed mechanism transfers the carrier from a vertical loading magazine to a platform which then rotates 120° to position the carrier under the cathode. The cathode or sputtering target consists of a 10-cm diam disc of $MoSi_2$ or Si–Cr fabricated by hot pressing. After a 2-min resistor deposition period (nominal), the substrate platform is rotated 120° once more, a new carrier is positioned under the cathode, and the carrier with the sputtered substrate is picked up by a receiving magazine.

Including loading and unloading time, the system is capable of about two cycles (60 carriers each) per eight-hour shift. For integrated circuit wafers (whole or broken) the carrier capacity is one wafer or equivalent per carrier. The wafer diameter can be 5 or 7.5 cm (2 or 3 in). Carriers for 2.5 by 2.5-cm or 2.5 by 5-cm ceramic substrates would be limited to four 2.5- by 2.5-cm substrates or two 2.5- by 5-cm substrates per carrier. A three-minute sputter time per carrier would reduce the capacity to three cycles for each two consecutive eight-hour shifts.

[1] P. Fehlhaber, aided by J. Vietor, developed the silicide resistor production process.

The thickness uniformity of the deposited film across a substrate depends on the ratio of the target diameter to the substrate diameter, cathode-substrate spacing, and the cathode shield geometry. Thickness uniformity of ±2–3 percent across a 5-cm diam substrate is not difficult to achieve using a 10-cm diam target [4].

Reproducibility of ρ_s from run to run depends on a reproducible deposition rate which in turn depends on sputtering voltage, current, time, and residual gas background [12]. Techniques for achieving such reproducibility have been described by Bickley and Campbell [13] and by Stern and Caswell [12].

Sputtering voltages between 2 and 3 kV have been used with cathode current densities of about 0.5 mA/cm^2. Details of the process have been described elsewhere [14].

B. Contact Metal

Evaporated aluminum 1 to 1.5 μm thick has been used most often as a contact metal. Sputtered molybdenum–gold has been used for contacts on alumina and sapphire substrates. Gold does not adhere well to silicides or ceramics, so 500 Å of molybdenum has been used as an intermediate layer. The gold thickness can be 1 to 5 μm or more.

We are concerned with reactions that may occur between the resistor and the contact films at elevated temperatures. Silicon diffuses rapidly into aluminum at 500°C or higher. During annealing, free silicon in the silicide film may diffuse into the aluminum contact, causing thinning of the resistor next to the aluminum contact boundary or lateral movement of this boundary. This effect has been seen in silicon–molybdenum and silicon–chromium films containing over ~75 at % silicon. It has *not* been seen in $CrSi_2$ or $MoSi_2$ films. Free molybdenum in the film could also cause problems by dissolving in the aluminum and forming intermetallic compounds. There is no evidence that uncombined molybdenum is present in the molybdenum disilicide films. Molybdenum–gold films have reportedly been used for high-reliability metallization on integrated circuits. Molybdenum can dissolve slightly in gold, but no intermetallic compounds are formed.

The contact is masked and etched first; then the resistor is masked and etched. It is often difficult to align a contact mask with an already defined resistor, especially on ceramic substrates or where the contact metal is ten times thicker than the resistor film. On monolithic circuits, the vertical resistance of the resistor film beneath the aluminum metallization and over the contact cuts in the oxide/nitride is usually negligible after alloying. Similar results

TABLE III
PHOTOMASKING TOLERANCES

Resistor Width (μm)	Tolerance for 95-percent Yield (percent)	Tolerance for 99-percent Yield (percent)
25	± 5	± 10
50	± 3	± 8

have been reported for Cr–SiO films as intermediate layers in monolithic circuit contacts [15]. Molybdenum can be etched in acid etchants and gold can be etched in iodine–KI etch [4]. None of these contact etching solutions attack silicide resistors.

C. Resistor Delineation

The silicide resistor film can be delineated by etching or by lifting; that is, dissolving away a prepatterned underlying film. Silicon etchants containing HF, HNO_3, and H_2O, or H_3PO_4 can be used to etch silicides [4]. Silicon nitride on monolithic circuits or alumina or sapphire for hybrid circuits are unaffected by these etchants.

Resistor films can be lifted using metals such as aluminum [16] or copper [17], or by dielectrics such as bismuth oxide [18], in cases where silicon etches would attack the substrate (for example, phospho-silicate glass on monolithic circuits). Photoresists cannot be used for lifting since the sputtering plasma can degrade the photopolymer (by heat, electron bombardment, and UV radiation) so that it is difficult to remove. In addition, the gases evolved by decomposition or outgassing of the resist can adversely affect reproducibility.

In some cases, sputter etching [16] of the film may be economically feasible.

D. Etching Tolerance

Resistor matching tolerance depends on linewidth. Our results on resistor matching agree with data reported by Glang and Shaible [16]. They found that the limit on etching precision was ± 0.5 μm (0.2 mil) regardless of size. Etching precision usually ranged from ± 0.5 μm to ± 2 μm. Assuming an ultimate standard deviation of ± 1 percent for sheet resistance variation over a substrate, Table III summarizes the experimental and theoretical results. It is an often overlooked fact that resistor reproducibility and matching are strongly dependent on the inherent reproducibility of the method used to define the resistor. Precision resistors require widths of 50 μm (2 mils) or more. Optimum pair matching requires identical resistor geometries; optimum ratio reproducibility requires identical line widths.

E. Annealing

After contacts and resistors have been patterned, the resistors are annealed at 500 to 565°C in nitrogen for 5–15 min. For monolithic circuits, this is the "alloy" step used to ensure ohmic contact between the aluminum metallization and the silicon devices. The step also eliminates resistor contact resistance and stabilizes the resistor against further changes (due to annealing) during die attach, packaging, and life.

SILICIDE RESISTOR CHARACTERISTICS

A. Resistivity and Temperature Coefficient

The film resistivity (ρ) in ohm-centimeters is defined as the product of the measured sheet resistance (Ω/sq) and the film thickness (cm). All resistivities quoted are those of films annealed at 530–565°C in nitrogen for 5–10 min. A useful range of film resistivities is 10^{-3} to 0.1 $\Omega \cdot$ cm (10^{3}–10^{5} $\mu\Omega \cdot$ cm) since with film thicknesses between 200 Å and 1000 Å, the sheet resistance range from 100 Ω/sq to 50 kΩ/sq can be produced. The average temperature coefficient of resistance (α) is here defined as $\alpha(\text{ppm}/^\circ\text{C}) = 10^4 [(R_2/R_1) - 1]$, where R_1 is the resistor value at 50°C and R_2 is the value at 150°C.

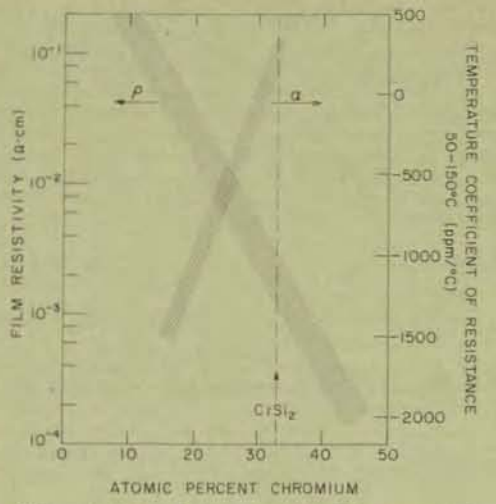

Fig. 1. Film resistivity and temperature coefficient versus chromium content for Si–Cr films.

For silicon–chromium resistors, the relation between chromium content, ρ and α is shown in Fig. 1. The data represent films deposited on thermally oxidized silicon substrates by electron-beam evaporation or by sputtering at 2–3 kV [14]. Both ρ and α are dependent on deposition conditions and substrate type, as well as chromium content [19]. Films deposited by sputtering from a hot-pressed chromium disilicide target ($CrSi_2$, 33 at % chromium) have a ρ of $2.6 \pm 1 \times 10^{-3} \Omega \cdot$ cm and an α of ± 50 ppm/°C. Increasing the silicon content of the film increases ρ and makes α more negative. Films containing about 30 at % chromium have a near zero α. The resistance-temperature curve for a near zero α film is shown in Fig. 2. The resistance of this sample has a maximum at about 75°C so that α calculated between 25° and 125°C would be essentially zero. In actuality the TCR is positive below 75° and negative above 75°C. The temperature for maximum resistance can vary slightly across one substrate so that α (the average TCR between 50° and 150°C) may vary by 50 ppm/°C on one substrate.

Molybdenum disilicide ($MoSi_2$) films, all deposited by dc sputtering, were found to have a negative TCR, and $\rho(\sim 1.3 \times 10^{-3}\ \Omega \cdot \text{cm})$ was about half that of $CrSi_2$ films. Increasing the silicon content of the films increased ρ, but resulted in even more negative TCRs, so silicon–chromium films appeared to be more suitable for higher values of ρ_s. Disilicide films of Ti, Zr, Hf, V, Nb, Ta, and W were found to be similar to $MoSi_2$ in resistivity and TCR.

Fig. 3 shows the relation between ρ_s and film thickness for $CrSi_2$ and $MoSi_2$. Thicknesses between 200 Å and 1000 Å represent a practical range for silicide resistors. Thinner films are more variable in ρ and TCR (more sensitive to sputtering conditions), and thicker films take too long to deposit and are more difficult to delineate. Thus $MoSi_2$ films are suitable for ρ_s values between 150 and 600 Ω/sq, and $CrSi_2$ films are useful for 300 to 1300 Ω/sq. The film resistivities indicated apply to films on smooth substrates: oxidized silicon wafers with or without silicon nitride passivation. Table IV shows the typical apparent[2] film resistivity variation for 1000-Å thick $MoSi_2$ film on various substractes. For good repro-

[2] "Apparent" because the roughness factor (ratio of actual surface area to geometric surface area) is unknown.

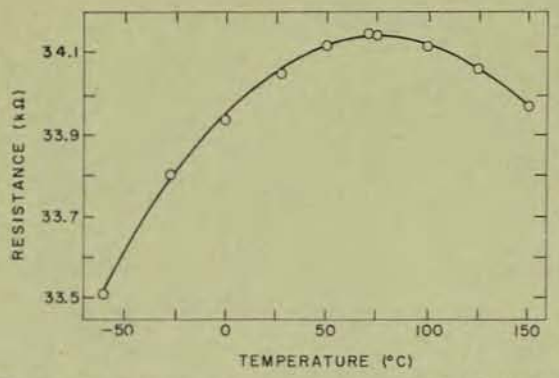

Fig. 2. Resistance versus temperature for a low TCR Si–Cr film.

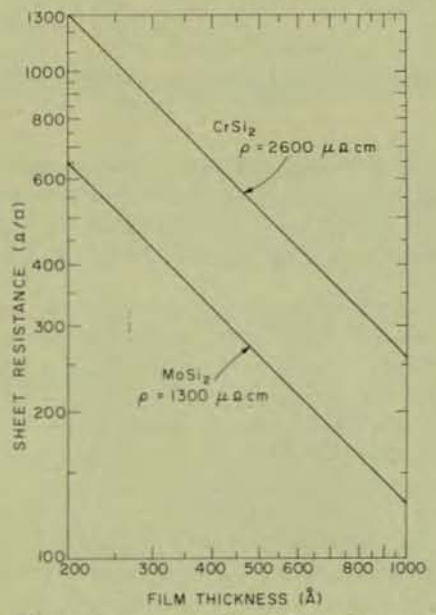

Fig. 3. Sheet resistance versus film thickness for typical $MoSi_2$ and $CrSi_2$ films.

ducibility on ceramic substrate, films thicker than 200 Å are required so that the practical thickness range is narrowed to 400–1000 Å. For $MoSi_2$ on 10-μin (CLA) alumina, ρ_s at 400 Å is about 600 Ω/sq. The resistivity of $CrSi_2$ and Si–Cr films on alumina substrates has not been extensively investigated, but Si–Cr films containing more than 75 at % silicon appear to be more sensitive to substrate surface conditions than $CrSi_2$ or $MoSi_2$ films.

Two "standard" Si–Cr resistor compositions have been developed for 2-kΩ/sq and 20-kΩ/sq resistors. The nominal compositions and characteristics of these resistors are listed in Table II. Increasing the silicon content to increase ρ_s requires tradeoffs in TCR and reproducibility.

B. Reproducibility

As indicated in Table III, resistor tolerances for resistors less than 50 μm (2 mil) wide are limited to no better than ± 3 percent (95 percent yield) by the photomasking/etching process. Variation of ρ_s across a substrate and from substrate-to-substrate or run-to-run will further increase the spread in resistor values. Estimated spreads for 95–99 percent yield for four silicide resistor processes are given in Table II. These represent run-to-run deviations of 2- to 4-mil wide resistors from their target values after all processing, including sealing in TO-5 cans. Deviations within a run are approximately half of these spreads.

TABLE IV

$MoSi_2$ Resistivity on Various Substrates

Substrate	Apparent Film Resistivity (thickness ~1000 Å) ($\mu\Omega \cdot$ cm)
99.5-percent alumina (Coors, 10-μin CLA)	2200
99.5-percent alumina (American Lava, 8-μin CLA)	2000
99.5-percent alumina, polished[a] (American Lava, 2-μin CLA)	1600
Sapphire, polished (Meller, 1-μin CLA)	1300
99.5-percent alumina, glazed	1300–1800
Silicon, thermally oxidized with or without Si_3N_4	1300

[a] Polished by Techwave, Princeton, N. J.

C. Stability

Typical stability data are summarized in Table II. All data refer to resistors annealed at 550°C to 565°C for 5 to 10 min in nitrogen, having *no* protective overlayer, and sealed in TO-5 cans. In general, $MoSi_2$, $CrSi_2$, and Si–Cr resistors are about equal in stability.

Silicide resistors, even when unprotected, show excellent stability during short term exposure to temperatures up to 550°C, such as during chemical vapor deposition (for scratch protection of aluminum metallization[3]), die attach, and ceramic package sealing.

Unprotected $MoSi_2$ resistors (200 Ω/sq on oxidized silicon) sealed in ceramic glass-sealed packages (Cerpak) changed <1.2 percent during packaging. During sealing the resistors are at a temperature >450°C for 16 to 18 min, and at 515° to 520°C for 4 min in oxidizing atmosphere.

For metallization scratch protection, vapor deposited silicon dioxide can be used. $MoSi_2$ resistors coated with 1 μm of vapor-deposited silicon dioxide changed by 0.25 percent or less during deposition. Coated resistors having aluminum bump contacts have been ultrasonic flip-bonded to ceramic substrates with no measurable change in resistor value during bump fabrication or bonding.

Extensive load-test data are not available for Si–Cr resistors, since the original development was for use in low-power circuits where the resistors carry less than 10 μA. More silicide resistor life-test data are needed particularly for high current densities, both steady state (dc and ac) and transient.

D. Radiation Resistance

Limited (unclassified) data indicate that silicide resistors are as radiation resistant as thin-film metal resistors, such as Ni–Cr or Ta. The resistors do not exhibit radiation-induced photocurrents and change less than 0.3 percent after radiation doses of 10^{15} N/cm^2 or 10^6 rad (Si)(Co^{60} gamma source).

E. Monolithic Circuit Application

$MoSi_2$ resistors (200 Ω/sq) are being evaluated in newly developed radiation-hardened monolithic circuits requiring resistor values between 100 Ω and 20 kΩ; that is, for resistors in the 100–200-Ω/sq range. Low-power radiation-hardened circuits requiring higher value resistors will use $CrSi_2$ or Cr–Si resistors (1.3 kΩ/sq or 2 kΩ/sq). For example, Si–Cr (2 kΩ/sq) resistors have been used in a radiation-hardened operational amplifier. This device has been described by Stafford and Oberlin [20], [21]. Si–Cr (20 kΩ/sq) resistors have been used in a low-power operational amplifier [22], [23], and in low-power bipolar digital arrays developed under an Air

[3] Silicide resistors themselves are extremely hard and scratch resistant.

Force contract [24]. In the digital circuits resistors still required 50 percent of the chip area, even with a 20-kΩ/sq ρ_s and a 10-μm (0.4-mil) resistor width.

Conclusion

Silicide resistors ($MoSi_2$, $CrSi_2$, and Cr–Si) have decided advantages in terms of short-term high-temperature stability and ease of fabrication over competitive thin-film resistors in the range 100–1000 Ω/sq. Between 2 kΩ/sq and 20 kΩ/sq, no (thin-film) competition exists. Silicide resistors are compatible with monolithic circuit wafer fabrication and assembly, and also offer an alternative technology for hybrid circuits destined for ceramic packages.

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Sputtered Silicon–Chromium Resistive Films*†

Robert K. Waits

Fairchild Camera and Instrument Corporation, Research and Development Laboratory, Palo Alto, California 94304

(Received 9 August 1968)

The resistivity, temperature coefficient of resistance (TCR), and structure of annealed films deposited by dc diode sputtering have been studied as a function of chromium content over the range 17–33 at.% Cr. The resistivity decreases from 0.1 to 0.001 Ω cm and the TCR changes from −1500 to +500 ppm/°C with increasing Cr content. Films containing about 27 at.% Cr had the lowest TCR. Films deposited at a cathode potential of 1.0 kV have a more positive TCR for the same resistivity than films sputtered at 2.5 kV. Electron micrographs showed the latter films to have a coarser structure—due either to a larger grain size (150 Å compared to 50 Å) or to a clumping of grains. Electron diffraction patterns indicated a nearly amorphous film; $CrSi_2$ was the only identifiable phase. The average drift of 50 μm-wide resistors (1 to 25 kΩ/square) during 1800 h at 200°C (no load) or 125°C (50 V dc) was ±0.5% after an initial 200 h aging under the same conditions.

Introduction

Many low-power monolithic integrated circuit applications require high-resistivity thin-film resistors.[1] Such resistors are fabricated on the same chip as the integrated circuit so the circuit and resistor processing and packaging must be compatible. A previous study[2] of silicon–chromium films deposited by electron-beam heating showed that films containing about 30 at.% Cr had low temperature coefficients and resistivities near 4×10^{-3} Ω cm. Stable resistors compatible with integrated circuit manufacture were produced that had sheet resistivities up to 10 kΩ/square. Film composition could not be precisely controlled, however, and adequate reproducibility was not achieved.

This paper describes the properties of silicon–chromium films deposited by dc diode sputtering. Diode sputtering was selected as the deposition technique most likely to achieve a uniform and reproducible film. Film resistivity, temperature coefficient, and structure were studied as a function of chromium content. The chromium content of the films was varied by varying the silicon–chromium ratio of the sputtering source. Resistive films containing from 17 to 33 at.% Cr were investigated since films having low temperature coefficients lie within this composition range.

Terry[3] has reported rf and triode dc-sputtering of resistive films from a cathode containing 33 at.% Cr (hot-pressed $CrSi_2$). The films had resistivities of 1100 to 3000 μΩ cm and temperature coefficients from −125 to −275 ppm/°C. Annealing in air at 450°C for 1 h did not change the resistor values. Several studies of vacuum-evaporated silicon–chromium have been made; see references listed in Refs. 2 and 4. Youmans[1] has reported that silicon–chromium films evaporated by electron-beam and containing 60.1–68.6 wt.% silicon (20–26.5 at.% Cr) have temperature coefficients of ±50 ppm/°C. Investigations of vacuum-sublimed silicon–chromium resistive films have recently been described in the Soviet literature.[5, 6] With regard to the application of such film resistors in integrated circuits, Wolf and Greenough[1] have described the use of one kΩ/square vacuum-deposited silicon–chromium resistors in a monolithic differential amplifier, and Hall[7] has reported the use of 200–500 Ω/square triode-sputtered "silicon-based alloy" thin-film resistors in several types of monolithic circuits. Both investigations reported temperature coefficients "less than 200 ppm/°C," but no resistivity data or process details were given.

* This work was sponsored in part by the Electronic Technology Division, Air Force Avionics Laboratory, Air Force Systems Command, United States Air Force.

† This paper was presented at the 15th National Vacuum Symposium of the AVS, Pittsburgh, 28 October 1968. The paper was not included in the Proceedings of the Symposium due to length limitations on papers published.

[1] H. Wolf and K. Greenough, Micoelectronics Reliability 6, 285 (1967). See also, A. P. Youmans, United States Patent 3,381,255 (30 April, 1968, filed April 1965).

[2] R. K. Waits, Trans. Met. Soc. AIME 242, 490 (1968).

[3] L. E. Terry, Final Report, AD 827 212 (Feb. 1968).

[4] R. B. Belser and M. D. Carithers, NASA Final Report, CR 88468, N67-36927, (Dec. 1966).

[5] A. I. Sokolenko and I. B. Staryi, Soviet Powder Met. Metal Ceram. (English Transl.) 50, No. 2, 142 (1967).

[6] I. B. Staryi and O. L. Chepok, Soviet Powder Met. Metal Ceram. (English Transl.) 50, No. 2, 145 (1967).

[7] J. H. Hall, Vacuum 17, 261 (1967); Semicond. Products 10, 50 (1967).

aluminum contact during annealing to produce a low-resistivity (10^{-3} to 10^{-4} Ω cm) phase that migrated from the contact area for distances of up to 100 μm along the resistor. (Similar results were reported for vacuum-deposited SiCr and Si films.[2]) This distance increased with increasing aluminum area adjacent to the resistor contact and with the annealing time and temperature. For annealing temperatures below 450°C, the effect was not noticeable.

This effect occurred only with films containing less than 25 at.% Cr (including silicon films), and which were sputtered at ~1.5 kV to 2.5 kV. (No films were deposited at voltages >2.5 kV.) Films sputtered at 1.0–1.25 kV did not react with the contacts nor did any films containing more than 25 at.% Cr. It is probable that the reaction is due to the high diffusivity of silicon into aluminum at the annealing temperature used. The characteristic diffusion length $2(Dt)^{\frac{1}{2}}$, where D is the diffusion constant and t is time, of silicon in aluminum after 10 min at 550°C is approximately 40 μm.[8] The granular structure of the thin aluminum and silicon films might be expected to enhance this diffusion rate. Similar silicon–aluminum diffusion reactions have been reported for evaporated polycrystalline silicon resistors contacted with aluminum[9] and for silicon films vacuum-deposited on single-crystal aluminum surfaces.[10]

All resistivity data that follow refer to annealed films.

B. Resistivity vs Composition

Sputtered films weighing 200–800 μg were analyzed colorimetrically for chromium. The films were deposited on oxidized silicon; the film weight was determined by weighing the wafers before and after deposition. The film was lifted from the wafer with conc. HF and then dissolved with HF/HNO_3. The chromium was determined by a modified S-diphenylcarbazide technique. Table I lists the results of film analysis along with the nominal and analyzed chromium content of the sputtering source. The analysis results for the sources may be low due to incomplete recovery of chromium. For films sputtered at 2.5 kV, the film analyses and cathode composition agree within the analytical uncertainty.

TABLE I. Weight percent chromium in sputtering source and sputtered films.

Source		Film analysis	
Nominal	Analysis	1.0 kV	2.5 kV
	(all ±2%)		
38.5	36.6	···	37.7 ± 1.0
31.5	28.6	···	28.6 ± 0.7
28.5	26.9	···	···
26.5	25.3	24.4 ± 1.5	28.2 ± 1.0

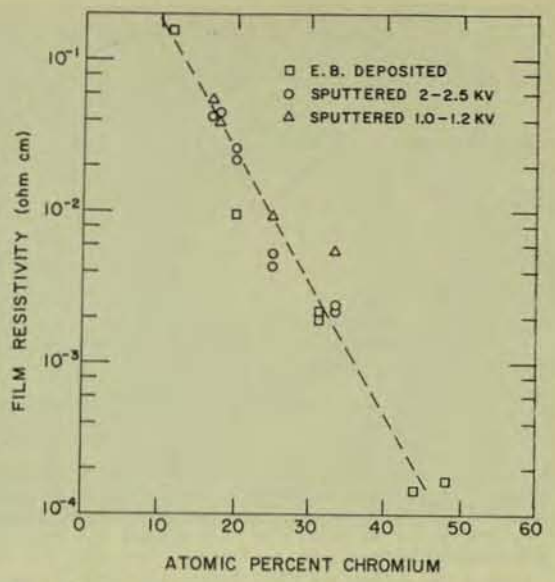


FIGURE 1. Film resistivity vs at.% Cr for SiCr films. For sputtered films, film composition assumed equal to cathode composition; for evaporated films, Cr content found by chemical analysis.

Film resistivity vs at.% Cr for both sputtered and electron-beam deposited films[2] is shown in Fig. 1. For sputtered films, the chromium content of the film was assumed to be the same as the nominal source composition. The electron-beam points are based on film analyses. The results are fairly consistent with the exception of films sputtered at 1.0 kV from cathodes containing 25 and 33 at.% Cr, which had a higher resistivity than those sputtered at 2.5 kV. A higher resistivity could be explained by a lower chromium content for lower voltage sputtering. Analyses of films sputtered at 1.0 and 2.5 kV from the same cathode (Table I) also indicate this might be the case. As discussed below, all films sputtered at lower voltages had a more positive temperature coefficient for the same resistivity than higher voltage films. The effect of less chromium should be an increase in resistivity while maintaining the same relation between resistivity and temperature coefficient; however, the experimental results show that this is not the case.

C. Resistivity vs Temperature Coefficient of Resistance

The temperature coefficient of resistance between 50° and 150°C as a function of film resistivity is plotted in Fig. 2. The dashed line is the least-squares fit for 22 runs, >500 Å thick, vacuum-deposited by

[8] C. J. Smithells, Ed., *Metals Reference Book* (Plenum Press, New York, 1967), 4th ed., Vol. II, p. 662.
[9] R. Gong, NASA Final Technical Status Report, CR 84144, N67-26520 (Oct. 1966).
[10] F. Jona, Bull. Am. Phys. Soc. 12, 549 (1967).

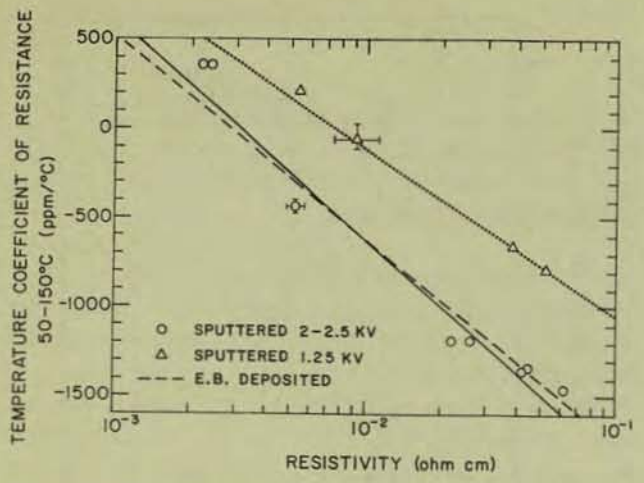


FIGURE 2. Temperature coefficient of resistance vs resistivity for SiCr films. Each point is the average of 4–7 runs; lines are least-squares fit for all runs. The data spreads for two points are indicated by bars.

electron-beam heating.[2] The solid line is the least-squares fit for 36 runs sputtered at 2.0–2.5 kV, 140 to 750 Å thick. The dotted line is the best fit for 18 runs sputtered at 1.25 kV, 350 to 750 Å thick. Each point represents the average of four to seven consecutive runs from the same sputtering source. The temperature coefficient is the average for ten units from the run. The data spreads for two of the points are indicated by bars.

The films sputtered at 2.0–2.5 kV and the electron-beam deposited films are similar, but the films sputtered at 1.0 or 1.25 kV have a more positive temperature coefficient of resistance for a given resistivity. This effect was voltage-dependent, not rate-dependent. Films sputtered at 1.0 kV at deposition rates up to 4 Å/sec (obtained by increasing the argon pressure) still had more positive temperature coefficients than films sputtered at 2.0–2.5 kV at the same rate. Conversely, sputtering at low rates and high voltages did not result in more positive temperature coefficients. The film resistivities for near-zero temperature coefficients are tabulated below:

Film	Resistivity for $\alpha = 0$ (Ω cm)
Sputtered 1.0–1.25 kV	0.0074
2.0–2.5 kV	0.0031
Electron-beam deposited	0.0029

Thus the films sputtered at lower voltages have the advantage of a 2.5 times higher resistivity at "zero" temperature coefficient. A further advantage is their previously discussed nonreaction with the aluminum contact metal during annealing.

Based on Figs. 1 and 2, hypothetical 200-Å-thick SiCr resistors sputtered at 1.0–1.25 kV would have the following characteristics:

at.% Cr	ρ (Ω cm)	α (ppm/°C)	Sheet resistance at 200 Å (kΩ/square)
30	0.0058	+100	2.9
27	0.0074	~0	3.7
25	0.0095	−100	4.8
19	0.026	−500	13

D. Resistivity-Temperature Curves

The results of resistivity-temperature measurements as log resistivity vs reciprocal temperature are plotted in Figs. 3 and 4. The circles and triangles represent films sputtered at 2.5 kV and 1.25 kV, respectively. The log ρ vs $1/T$ curves for the 2.5-kV films are similar to those for electron-beam deposited films.[2] The curves for films deposited at 1.25 kV have less curvature than corresponding 2.5-kV films. Films having resistivities near 3×10^{-3} Ω cm sputtered at 2.5 kV, and films between 5×10^{-3} and 10^{-2} Ω cm deposited at ~1.0 kV had a maximum in resistance at some temperature between − 60° and +300°C.

All resistors decreased slightly in value during resistance measurements above 200°C. (The lower temperature measurements were made first.) The maximum decrease observed was 2.7%, but the typical change was less than 1%.

E. Film Structure

The structure of the sputtered SiCr films was studied by electron diffraction and electron-transmission

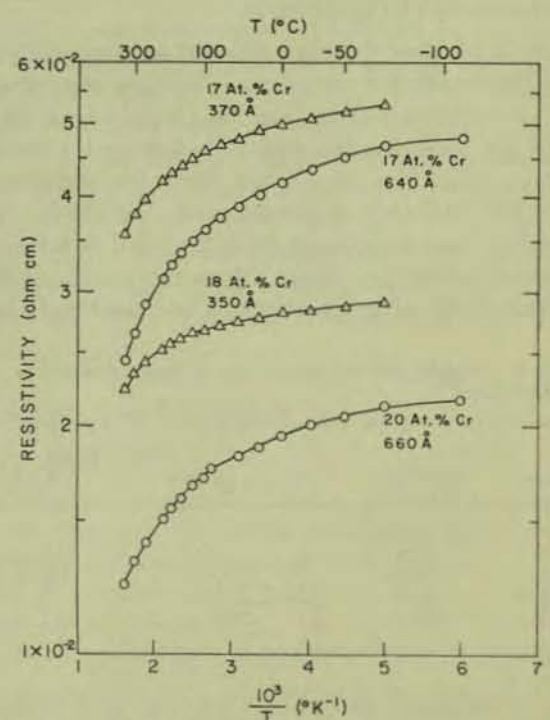


FIGURE 3. Log resistivity vs $1/T$ for sputtered SiCr films containing 17–20 at.% Cr. Film thicknesses are noted. ○ cathode potential 2.5 kV; △ cathode potential 1.25 kV.

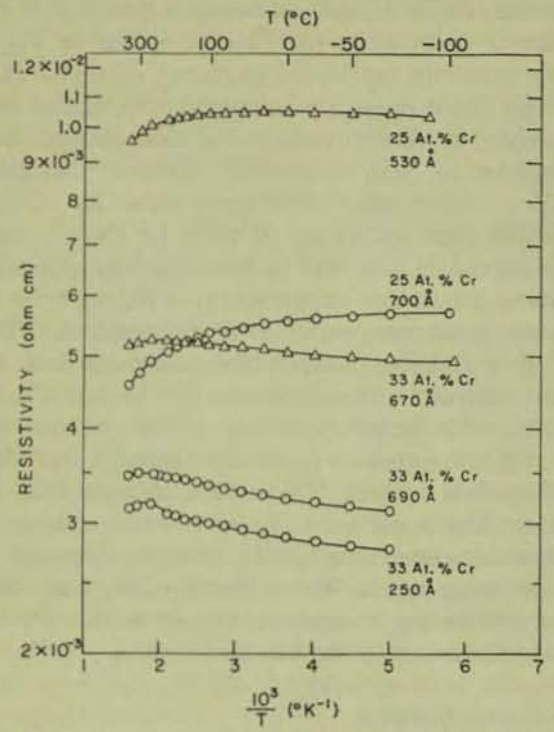


FIGURE 4. Log resistivity vs $1/T$ for sputtered SiCr films containing 25–33 at.% Cr. Film thicknesses are noted. ○ cathode potential 2.5 kV; △ cathode potential 1.25 kV.

microscopy. The films were deposited on oxidized silicon wafers whose backs were protected by a gold film having etched holes. After film deposition, the silicon exposed in the holes of the gold film was etched away leaving either a thin (<1000 Å) oxide skin or no oxide supporting the sputtered film.

Films sputtered from cathodes containing 17, 20, 25, and 33 at.% Cr were examined. Each composition was represented by films deposited at 1.0 and 2.5 kV and by annealed (5 min, 550° to 565°C) and unannealed films. Longer annealing times had little additional effect on film resistivity.

All the diffraction patterns had diffuse rings indicating nearly amorphous films. The only crystalline phase that could be identified was chromium disilicide. The sharpness of the diffraction rings increases with increasing chromium content. Annealing the films also sharpens the diffraction patterns (Fig. 5), and films sputtered at 2.5 kV have a less diffuse pattern both before and after annealing than those sputtered at 1.0 kV.

The greatest difference between 1.0- and 2.5-kV films shows up in the electron-transmission micrographs. Typical micrographs are shown in Fig. 6. The films were sputtered at 1.0 kV (left) and 2.5-kV cathode potential. Both films have a very fine structure. The average grain size is 40–50 Å for the 1.0-kV film. The 2.5-kV film appears to be composed either of clumps of two or three small (40–50 Å)

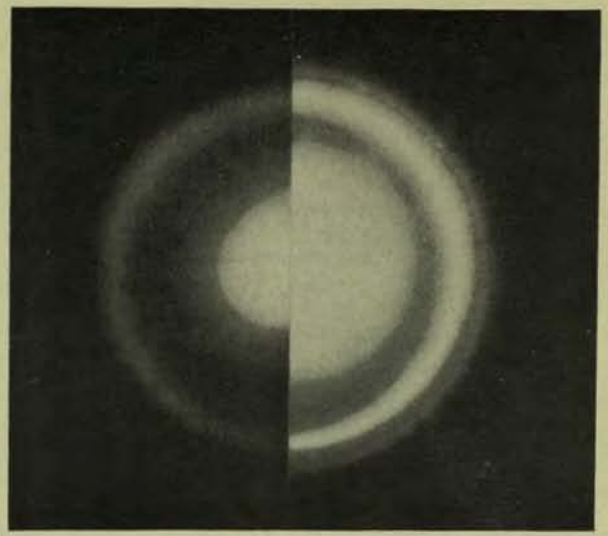


FIGURE 5. Electron diffraction patterns, sputtered silicon-33 at.% Cr. Cathode potential 2.5 kV, 690 Å thick. *Left:* not annealed. *Right:* annealed 5 min, 550°C in nitrogen.

grains, or of irregular grains about 80–150 Å long. Micrographs of the same films after annealing for 5 min at 565°C in nitrogen showed no difference in grain size.

There was little discernible difference between electron micrographs of films over the composition range 17–33 at.% Cr except for a tendency toward a chain-like orientation of grains in some of the films containing 17 at.% Cr. The chains were approximately 1000 Å long and sometimes oriented parallel to each other.

Our observations are similar to those of Sokolenko and Staryi[5] who have reported x-ray diffraction studies of SiCr films deposited on fused quartz by vacuum sublimation of an alloy containing 24 wt.% Cr (14.5 at.% Cr.). (From the reported film resistivity, 0.01–0.025 Ω cm, it is probable that the films contained 20–25 at.% Cr.) Diffuse lines were found that corresponded to $CrSi_2$ for films annealed at 350° to 400°C.

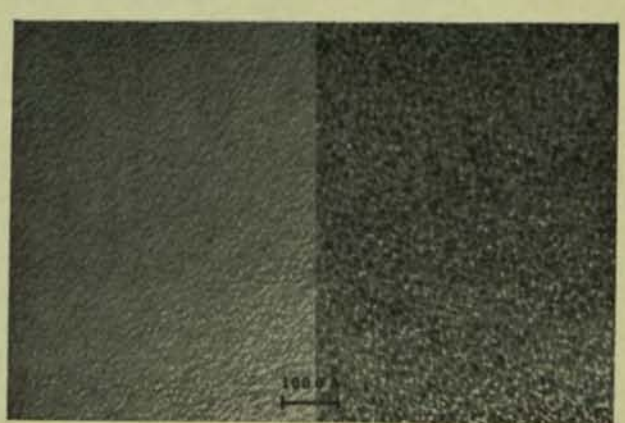


FIGURE 6. Electron-transmission micrographs, sputtered silicon-20 at.% Cr. *Left:* cathode potential 1.0 kV, 680 Å thick. *Right:* 2.5 kV, 920 Å.

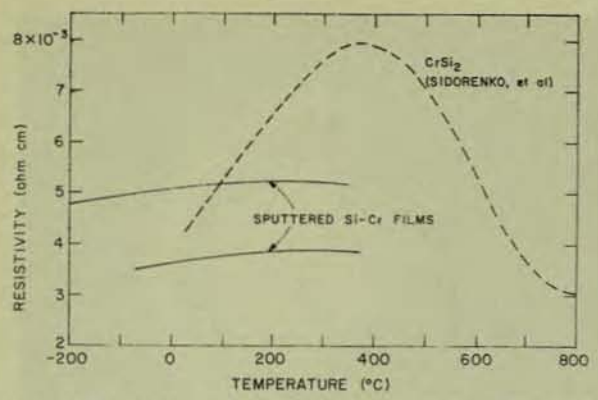


FIGURE 7. Resistance-temperature curves for chromium disilicide (dashed line) and sputtered SiCr films (solid lines). The SiCr films were 670–690 Å thick and were deposited from a source containing 33 at.% Cr at 1.25 kV (top) and 2.5 kV (bottom).

At 500°C sharper lines corresponding to Cr were also noted. At 600°C the Cr lines disappeared and Si lines appeared. The crystal size, calculated from the x-ray linewidths, was 40–50 Å after annealing at 400° to 500°C.

Previous electron-diffraction studies of electron-beam deposited films[2] showed Cr_3Si to be present in films containing from 10–33 at.% Cr; no $CrSi_2$ or Cr was detected. In contrast, Cr_3Si was not detected in sputtered SiCr films.

Chromium disilicide may be the major conductive component in sputtered SiCr films. The room temperature resistivity of $CrSi_2$ has been reported as 1.4×10^{-3} Ω cm,[11, 12] 4.3×10^{-3} Ω cm,[13] and $1.7–20 \times 10^{-3}$ Ω cm.[14] The temperature coefficient is positive (2500–2900 ppm/°C) below 350° to 370°C and is negative from 400° to 700°C.[11, 13] The band gap calculated from high temperature resistivity-temperature measurements is 0.5 eV[13] to 0.74 eV.[14] The resistivity and band gap energy are sensitive to composition in the range $CrSi_{1.95}$ to $CrSi_{2.05}$.[12, 14]

Although annealed SiCr films containing 25–33 at.% Cr have resistivities in the range reported for chromium disilicide, the resistance vs temperature behavior is quite different. This is shown in Fig. 7 where resistivity curves for sputtered silicon-33 at.% Cr films (solid lines) are compared with similar data for polycrystalline chromium disilicide (dashed line) as reported by Sidorenko *et al.*[13] (Nikitin[12] has given similar conductivity–temperature data for $CrSi_2$.) Annealed films containing 33 at.% Cr show a resistance maximum near 300°C, but films containing less Cr have a negative temperature coefficient or a resistance maximum at a lower temperature. Films having a negative temperature coefficient had apparent activation energies from 10^{-4} to 0.05 eV, increasing with temperature and silicon content. The film resistivity appears to be exponentially dependent on chromium content. These data indicate that the resistive film is not behaving as a simple mixture of a chromium-based conducting medium dispersed in an insulating matrix. Even though $CrSi_2$ may be a major conducting component, the conduction mechanism is dominated by the film structure.

F. Resistor Stability

Canned resistors having resistivities of 1–25 kΩ/square were stored at 200°C, no load, and their room temperature resistance measured at intervals up to 2000 h. The measurement uncertainty was ±0.05%. Films having resistivities of 1–1.5 kΩ/square were also load tested at 50 V dc at 125°C. A silicon overlayer was electron-beam deposited on some resistor films prior to resistor etching in order to determine whether such an overlayer would improve resistor stability.

Representative 200°C storage results for 15–25 kΩ/square films are summarized in Table II. The films were sputtered at a cathode potential of 1.0 kV and contain approximately 20 at.% Cr. These data represent five runs with and five runs without a silicon overlayer. Resistors having a silicon overlayer were more stable during the initial 200 h than unprotected films, but there was no difference in stability during the subsequent 1800 h.

Table III summarizes storage and load test data for 1 and 1.5 kΩ/square resistors. A total of 248 resistors were tested representing four runs with and four runs without a silicon overlayer. The sputtering potentials

[11] D. A. Robins, Phil. Mag. 3, 313 (1958).
[12] E. N. Nikitin, Soviet Phys.-Solid State 2, 1966 (1961).
[13] F. A. Sidorenko, I. Z. Radovskii, L. P. Zelenin, and P. V. Gel'd, Soviet Powder Met. Metal Ceram. (English Transl.) 48, No. 9, 730 (1966).
[14] B. K. Voromov, L. D. Dudkin, N. I. Kiryuchina, and N. N. Trusova, Soviet Powder Met. Metal Ceram. (English Transl.) 49, No. 1, 56 (1967).

TABLE II. Resistor stability, 15–25 kΩ/sq, 20 at.% Cr.

No. units	kΩ/square	Overlayer thickness Å	SiCr thickness Å	Resistor change—200°C, $\Delta R/R$ (%) 0–200 h Av.	Max	200–2000 h Av.	Max
73	15–25	None	210–230	3.2	7.0	−0.21	−0.79
71	18–25	1300–1500	140–240	0.65	2.0	−0.17	0.81

TABLE III. Resistor stability, 1–1.5 kΩ/sq, 33 at.% Cr.

kΩ/square	Overlayer thickness Å	SiCr thickness Å	Resistor change, $\Delta R/R$ (%) 200°C (60 units/group) 0–1000 h[a] Av.	Max.	125°C, 50V (64 units/group) 0–200 h Av.	Max.	200–2000 h Av.	Max.
1.0	None	190–250	0.46	1.2	0.75	4.4	0.51	3.2
1.5	1100–1400	140–190	0.34	0.94	0.31	0.50	0.1	0.33

[a] No measurements made at 200 h.

were 2 kV (1.5 kΩ/square) and 2.5 kV (1.0 kΩ/square), and the films contained about 33 at.% Cr. Half of the units were stored at 200°C, no load, and half were load tested at 50 V dc at 125°C. The 50-V bias during load testing resulted in a higher current density for the 1.0 kΩ/square films (no overlayer) than for the 1.5 kΩ/square films (silicon overlayer). The units having no overlayer were subjected to a current density of 20 A/cm² and 1.0 kW/cm². The current and power densities for the resistors having a silicon overlayer were 13 A/cm² and 0.67 kW/cm². The resistor leads were identified and the dc polarity kept the same throughout the test.

During storage at 200°C, there was no significant difference in stability between films with and without a silicon overlayer; the maximum changes after 1000 h were 0.94% and 1.2%, respectively. During load test, the overcoated resistors were significantly more stable during both the initial 200-h period and the subsequent 1800 h. The 50% higher power level for the unprotected resistors may be responsible for most of the stability difference. Figure 8 shows the average resistor change vs time for representative runs (15–16 resistors each) from Tables II and III.

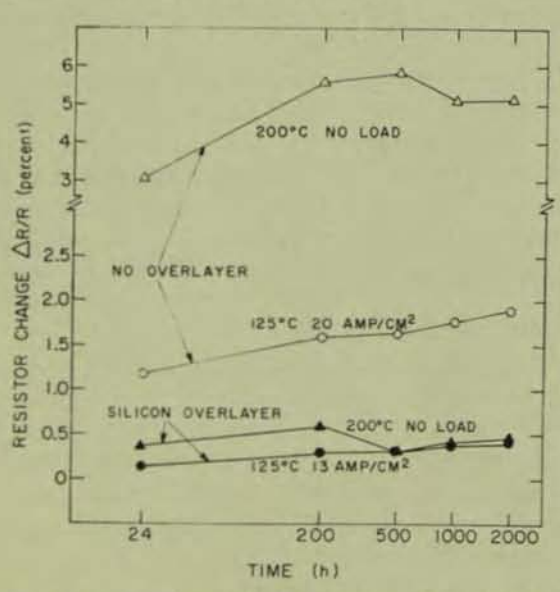


FIGURE 8. SiCr resistor stability vs time. Triangles: 200°C, no load (Table II). Circles: 125°C, 50 V (Table III). Each point is the average change for one run of 15–16 units.

During the tests described above, three resistor failures occurred. All were opens caused by a defective ultrasonic bond between the lead wire and the aluminum contact pad.

G. Reproducibility

The distributions in resistance values and temperature coefficients for 50 μm-wide resistors were measured for 1.5 kΩ/square and 11 kΩ/square resistors. The results are summarized in Table IV. The spreads were calculated from the standard deviations assuming a normal distribution.

The 1.5 kΩ/square resistors were deposited at 2 kV from a cathode containing 33 at.% Cr. The average film thickness was 150 Å and the films had a 1500 Å silicon overlayer. For the six runs, 255 units were measured on wafers; 99% were within ±7% of the mean. The wafers were then separated into dice, mechanically damaged dice were discarded, and about 15 randomly selected units from each run were sealed in cans and measured. The mean resistor value increased 0.55% and the spread remained the same. The temperature coefficient was +357 ppm/°C ±11% for 99% yield.

Similar measurements were made for five runs of 11 kΩ/square resistors sputtered at 1.0 kV from a cathode containing 20 at.% Cr. The average film thickness was 210 Å; the resistors had no overlayer. The spread for 99% yield was ±20% on wafers and ±21% in cans. The mean increased 3% during canning. The average temperature coefficient was −205 ppm/°C ±28% for 99% yield.

Glang and Schaible[15] have reported that standard deviations of ±0.5 to 2 μm can be expected in the dimensions of film resistors formed by the photoresist/etching technique. For a 50 μm-wide resistor stripe, they found the standard deviation in resistor value due to dimensional variations to be ±2.3%. To estimate the tolerances within which 99% of all resistors will fall, the estimated standard deviation must be multiplied by 2.6. This gives an expected tolerance of ±6% for 99% yield for 50 μm-wide resistors longer than 5 squares. The data for 1.5 kΩ/square are just outside

[15] R. Glang and P. M. Schaible, Thin Solid Films 1, 309 (1968).

TABLE IV. Reproducibility of 50 μm-wide resistors.

	No. units measured	Av.	Standard deviation (%)	Spread for 99% yield (%)
	1.5 kΩ/sq (6 runs, 2 wafers/run)			
R, on wafers	255	1.47 kΩ/sq	2.57	±6.6
R, in cans	86	1.48 kΩ/sq	2.58	±6.6
TCR, in cans	86	+357 ppm/°C	4.42	±11
	11 kΩ/sq (5 runs, 1 wafer/run)			
R, on wafers	140	11.0 kΩ/sq	7.55	±20
R, in cans	148	11.3 kΩ/sq	8.18	±21
TCR, in cans	123	−205 ppm/°C	11.3	±28

this tolerance, indicating that run-to-run variations due to the deposition and annealing steps were small. The resistance spread for 11 kΩ/square resistors exceeded the tolerances to be expected from the masking and etching steps. It is believed that this is due to sheet resistivity variations that occur during both deposition and annealing. The large temperature coefficient spread also indicates that there is a variation in film properties.

The variation in sheet resistance across a typical 1–2 mm square silicon die is negligible. Therefore, the accuracy of resistor matching or ratio control for resistors on the same integrated circuit chip is limited only by the precision of the resistor delineation method used.

H. Application to Integrated Circuits

Thin-film resistors having nominal sheet resistivities of 2 kΩ/square and 20 kΩ/square have been used in pilot production runs of two linear circuits: a radiation-hardened amplifier and a low-power, low-noise amplifier. Working circuits have been fabricated and the compatibility of the thin-film resistor and the integrated circuit processes has been demonstrated.[16]

III. Conclusions

Silicon–chromium thin-film resistors having sheet resistivities up to 11 kΩ/square can be reproducibly (±15% or better for 90% yield) deposited by dc diode sputtering in argon. The chromium content of the sputtered films was equal to the cathode composition within the analytical uncertainty. Film resistivities and temperature coefficients are dependent on composition. As the chromium content is increased from 17 to 33 at.%, the resistivity increases from 0.1 to 0.001 Ω cm and the temperature coefficient (50° to 150°C) changes from −1500 to +500 ppm/°C. Near-zero temperature coefficients occur at about 27 at.% Cr; the film resistivity is 3100 μΩ cm for films sputtered at 2.5 kV and 7400 μΩ cm for films deposited at 1.0 kV. Films deposited at a cathode potential of 1.0–1.25 kV have a more positive temperature coefficient for the same resistivity than films sputtered at 2.0–2.5 kV. Electron-transmission micrographs showed the latter films to have a coarse structure—due either to a larger grain size (150 Å compared to 50 Å) or to a clumping of grains.

All films were nearly amorphous. The only crystalline structure indentifiable by electron diffraction was chromium disilicide. The $CrSi_2$ rings increase in intensity and sharpness with increasing chromium content. Annealing of films at 550°C for 5 min in nitrogen also increased the sharpness of the $CrSi_2$ diffraction rings, and in general resulted in a decrease in resistivity.

The average stability of 1 to 25 kΩ/square SiCr resistors during 1800-h life tests was ±0.5% after an initial 200-h aging period, during which the values increased 0.5% to 7%. The initial increase was less for films having an evaporated silicon overlayer deposited prior to resistor etching. The life tests were made at 200°C, no load, and 125°C at 50 V dc.

Acknowledgments

I am grateful to the following persons for their contributions of knowledge and skill. The film depositions and thickness measurements were made by Satoshi Sekigahama. Douglas Mattern, Carl Fender, and Robert Warnacke performed the electron microscope examinations, and Eugene Meieran interpreted the results. Robert Ceynowa developed the chromium analysis technique and analyzed the films. Dorothy Unruh made many of the tedious calculations and plotted the data.

[16] J. S. MacDougall, D. W. Oberlin, and K. R. Stafford, (U.S.) Govt. Microcircuits Appl. Conf., Digest of Papers 1, 326 (Office of Naval Research, 1968); C. A. Bittman, *et al.*, IEEE Internat. Solid-State Circuits Conf., Digest of Techn. Papers, 152 (Lewis Winner, New York, 1969).

Silicon-Chromium Electron-Beam-Deposited Resistive Films

Robert K. Waits

The resistivity, temperature coefficient of resistance, stability at 200°C, and structure of annealed Si-Cr films have been studied as a function of film composition. Colorimetric analyses of the films indicated 20 to 60 wt pct Cr over the resistivity range of 1 to 10^{-4} ohm-cm. Resistors were delineated by photolithographic etching, contacted with aluminum, and mounted in TO-5 packages. The average temperature coefficient of resistance, α, between 50° and 150°C is related empirically to the film resistivity, ρ, by α (ppm per °C) = −2900 − 1140 log ρ (ohm-cm). Near a resistivity of 3.5×10^{-3} ohm-cm (30 at. pct Cr), the temperature coefficient changes from positive to negative. The temperature at which the resistance maximum occurs increases with decreasing resistivity. The conduction mechanism between −196° and +360°C appears to have two components—an activated conduction dominating at low chromium content and higher temperatures and a linearly temperature-dependent conduction dominating at high chromium content and low temperatures. Electron diffraction patterns showed the films to consist of Cr_3Si and amorphous silicon. Resistors thicker than 150Å typically drifted less than 0.6 pct after 5000 hr storage at 200°C. Resistors as thin as approximately 80Å that had a silicon overlayer showed similar stability. Such films had sheet resistivities of 10 kilohm per square and temperature coefficients near −600 ppm per °C.

THIN-FILM resistors having sheet resistivities greater than 1 kilohm per square are required in many integrated circuit applications. A process for producing such resistors should be compatible with present circuit fabrication and packaging, including exposure to maximum temperatures of 300° to 570°C during contact alloying, die-attach, and ceramic package sealing. In addition, the resistors should have a low temperature coefficient of resistance and change less than 1 pct during storage at temperatures up to 200°C for 1000 hr or longer.

Reports of work beginning in 1949 at Battelle Memorial Institute indicated that, among other materials, the silicides of chromium, Cr-Co, molybdenum, tantalum, and tungsten were worthy of further study as high-stability resistive films. Later work on Si-Cr films vacuum-deposited by flash evaporation from a tungsten boat[1] led to the conclusion that Si-Cr had "excellent properties for development into high-stability ... resistive elements". More recently, Si-Cr films have been vacuum-deposited from a tantalum boat,[2] from a BeO-coated tantalum boat,[3] by flash evaporation from an electron-beam-heated tungsten source,[4] and by triode sputtering.[5]

This paper describes a study of Si-Cr films vacuum-deposited by electron-beam heating of Si-Cr alloys. Resistivity, temperature coefficient of resistance, stability at 200°C, and structure were studied as a function of film composition.

EXPERIMENTAL PROCEDURE

Film Deposition. Si-Cr sources were prepared by vacuum-melting pressed pellets of mixtures of powdered chromium (99.9 pct, −100 mesh, Lunex Co., Pleasant Valley, Iowa) and silicon (99.99 pct, −325 mesh, United Mineral and Chemical Co., New York). A permanent-magnet focused electron-beam gun having a water-cooled copper crucible was used to heat the pellet until complete melting occurred. The mixture was then kept molten for an additional 5 min. The alloy thus formed was used as the source material for Si-Cr film depositions using the same electron-beam gun. Pieces of semiconductor-grade silicon ingots were used as sources for silicon depositions. The films were deposited within a standard vacuum evaporator having an 18-in.-diam Pyrex bell jar, a liquid-nitrogen-cooled trap, and a Consolidated Vacuum Corp. 6-in. diffusion pump containing Dow Corning DC-705 pump fluid. The substrates were thermally oxidized* silicon wafers 2 to 2.5 cm in diam. The wafers were cleaned prior to deposition by a 1-min dip in a chromium trioxide-sulfuric acid solution followed by a deionized water rinse. The substrate holder was radiantly heated by tantalum filaments. The temperature during deposition was 300°C as indicated by a chromel-alumel thermocouple on the surface of the substrate holder. The wafers were held in contact with the substrate holder by Inconel-X alloy clips. Two source-to-substrate distances were used, 28 and 43 cm. The pressure during the depositions was typically 4 to 6×10^{-6} Torr; the background pressure was a decade lower.

*Steam, 1200°C, 2 hr; about 1.5 μm oxide.

The deposition rate and thickness were monitored by a quartz-crystal oscillator. Deposition rates ranged from 0.3 to 22Å per sec for Si-Cr and from 2 to 8Å per sec for silicon. During a run the deposition rate was kept relatively constant by manual control of the electron-beam current. A frequency counter was used to monitor rates less than 1Å per sec.

A 2.5-cm-sq glass microscope slide was included in each run and the film thickness determined by multiple-beam interferometry.[6] Film thicknesses measured on an oxidized, mechanically polished silicon wafer and on a glass slide agreed within the accuracy

ROBERT K. WAITS is Senior Engineer, Fairchild Semiconductor Research and Development Laboratory, Palo Alto, Calif.
This work was sponsored in part by the Air Force Avionics Laboratory, Research and Technology Division, Air Force Systems Command, United States Air Force.

This manuscript, submitted on September 1, 1967, was based on a talk presented at the IMD Electronic Materials Conference on August 28-30, 1967, in New York City.

of measurement for a 1000Å film. Silicon wafers were not used as thickness monitor slides, however, since their roughness prevented accurate measurement of fringe displacement for thinner films.

Resistor Fabrication. After deposition, the wafers were masked with Kodak Thin Film Resist. The Si-Cr film, including silicon overlayer when present, was etched with a mixture of concentrated phosphoric, nitric, and hydrofluoric acids (60-5-1 by volume). Etch rates were 10 to 15Å per sec. The photoresist was then removed and 0.5 to 0.6 μm of aluminum was vacuum-deposited over the etched resistor pattern. The aluminum was then masked and etched to delineate the resistor contact pattern. The resistor and contact pattern are shown in Fig. 1. The pattern consists of eight resistors, each 50 μm wide (0.002 in.) and from 3 to 24 squares in area. The aluminum contacts overlap the resistor by 50 μm at each end of the resistor providing a contact area of 2500 sq μm (4 sq mil). For a single array, if the measured resistor value is plotted against resistor length (no. of squares), a straight line results that crosses the resistance axis at the contact resistance value. An erratic contact resistance causes scatter in the points. Thus, it is possible to determine easily the presence or absence of nonnegligible contact resistance. In any case, the slope of the line gives the sheet resistance directly in ohms per square. Negligible contact resistance was achieved by heating at 550° to 565°C in nitrogen for 2 to 10 min. This treatment also annealed the resistive film and stabilized the resistor value against further change during storage at 200°C. The film resistivity in ohm-cm was taken as the product of the sheet resistance after annealing and the film thickness. In all cases, "film resistivity" refers to the resistivity after annealing. After annealing, the wafers were diced, the dice were optically sorted to remove damaged resistors, and ten to fifteen randomly chosen dice were mounted on TO-5 headers. The aluminum contact pads were connected to the header posts with ultrasonically bonded 25-μm-(0.001-in.) diam aluminum wire. The units were then vacuum-baked for 2 to 3 hr at 300°C and sealed under nitrogen. Only the 10 square resistor in each array was connected.

Resistance-Temperature Measurements. The average temperature coefficient of resistance, α, between 50° and 150°C was calculated using the relation:

$$\alpha \text{ (ppm per °C)}^* = 10^4\left(\frac{R_2}{R_1} - 1\right)$$

*Parts per million per °C = 10^{-6} ohm per ohm°C.

where R_1 is the resistor value at 50°C and R_2 is the value at 150°C. Resistance-temperature measurements were also made for some films at −196°C (liquid nitrogen), at −115°C (liquid nitrogen-ethyl alcohol), at 25°C intervals from −73° to +200°C in a liquid carbon dioxide cooled temperature chamber, and at 300° and 360°C in an oil bath. Resistances were measured using a Cubic Corp. Model 041 digital ohmmeter.

RESULTS AND DISCUSSION

Composition and Resistivity. The resistivity of films evaporated from Si-Cr sources prepared as described above depended on source composition as shown in Fig. 2. Even where the deposition rates from a given source were identical, the resistivity could vary from run to run by as much as a factor of two. The silicon/chromium ratio in the evaporant depends on the source temperature (unless the mixture vaporizes congruently) and reproducing the rate does not guarantee reproducing the temperature unless the evaporating area and geometry remain the same. These factors depend on the source size and placement, area of focused electron beam, and so forth.

A series of films from 1500 to 2000Å thick, weighing 400 to 1400 μg, was analyzed colorimetrically for chromium. Up to about 30 wt pct Cr the films had nearly the same composition as the source. The deposition rates were between 1.1 and 1.6Å per sec. Above 30 wt pct Cr the films contained more chromium than the source. The deposition rates were lower (0.70 to 1.0Å per sec) but the power input and the estimated source brightness temperature were greater. These results are shown in Fig. 3.

The resistivity of 1500 to 2000Å-thick films vs atomic percent chromium is shown in Fig. 4. Film resistivity increases rapidly for films containing less than 10 at. pct Cr. These data, expressed as conductivities, are shown in Fig. 5, compared with the electrical conductivity curve as determined by Nikitin[7] for the ordered Si-Cr system.

Films containing between 5 and 25 at. pct Cr were found to react with the evaporated aluminum contacts during the 550° to 565°C annealing process to produce a low-resistivity phase that migrated from the aluminum contact pad into the resistor area for a distance of 10 to 50 μm. (A similar reaction occurred between aluminum contacts and pure silicon films deposited at temperatures below 300°C.) This contact reaction could be prevented by overcoating the Si-Cr film with

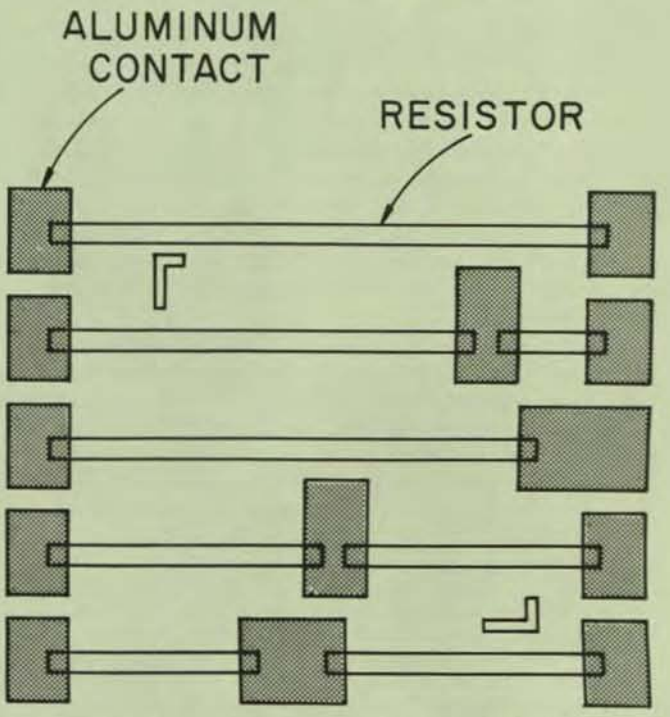


Fig. 1—Resistor array; resistors are 50 μm wide and 3 to 24 squares long.

about 1200Å of silicon deposited at 300°C during the same pumpdown or in a subsequent deposition. This two-layer film was masked and etched in the same manner as a single-layer film. During the annealing process at 550° to 565°C, the aluminum rapidly diffused through, or reacted with, the overlying silicon to make ohmic contact to the underlying resistive film. No contact spreading occurred and any remaining contact resistance was negligible. A cross section of the contact area of a Si-Cr resistor having a silicon overlayer is diagramed in Fig. 6.

Resistance vs Temperature. Resistance-temperature measurements were made between −196° and +360°C for two groups of resistors: 1) 10^{-1} to 10^{-5} ohm-cm films greater than 600Å thick, and 2) 0.0028 to 0.0051 ohm-cm films less than 300Å thick. Films 100Å thick or less had a silicon overlayer. The thick films exhibited a permanent change of less than ±0.15 pct during the temperature cycle except for the 0.2 ohm-cm film which changed +0.35 pct. Three of the thin films decreased 0.5 to 0.7 pct and two (Nos. 88 and 38) changed less than 0.05 pct. Data for the two groups of films are listed in Tables I and II.* Plots of log resistivity vs reciprocal temperature for the thick films and one film from group 2 are shown in Figs. 7 and 8. The film thicknesses (Å) and α between 50° and 150°C (ppm per °C) are indicated on the curves. For films greater than 0.05 ohm-cm (15

*For runs 35 and 38, the source-substrate distance was 28 cm; for the other runs listed, the source-substrate distance was 43 cm.

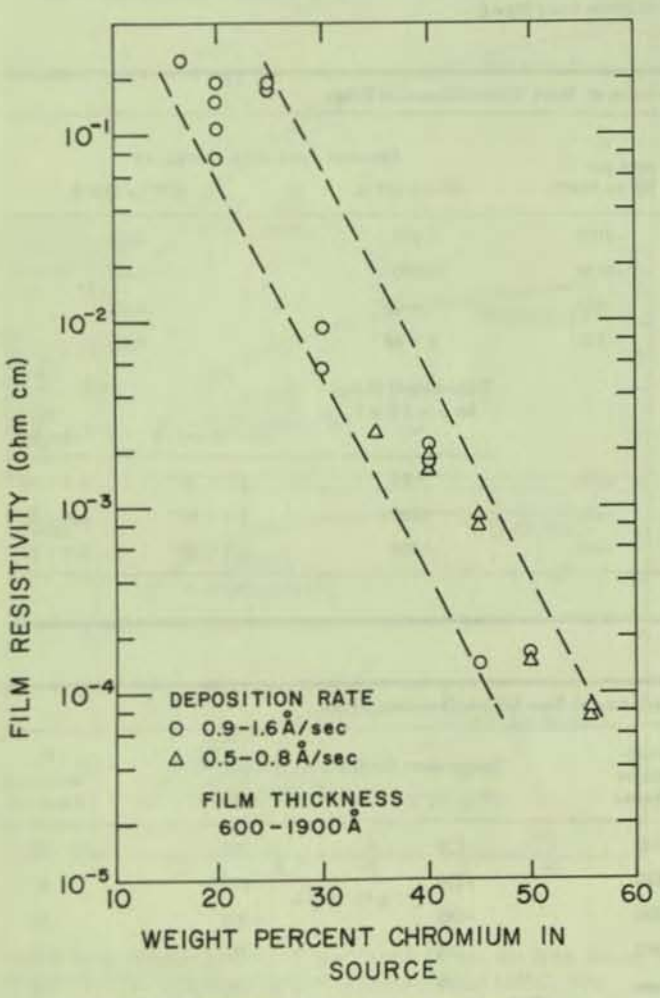


Fig. 2—Film resistivity vs source composition.

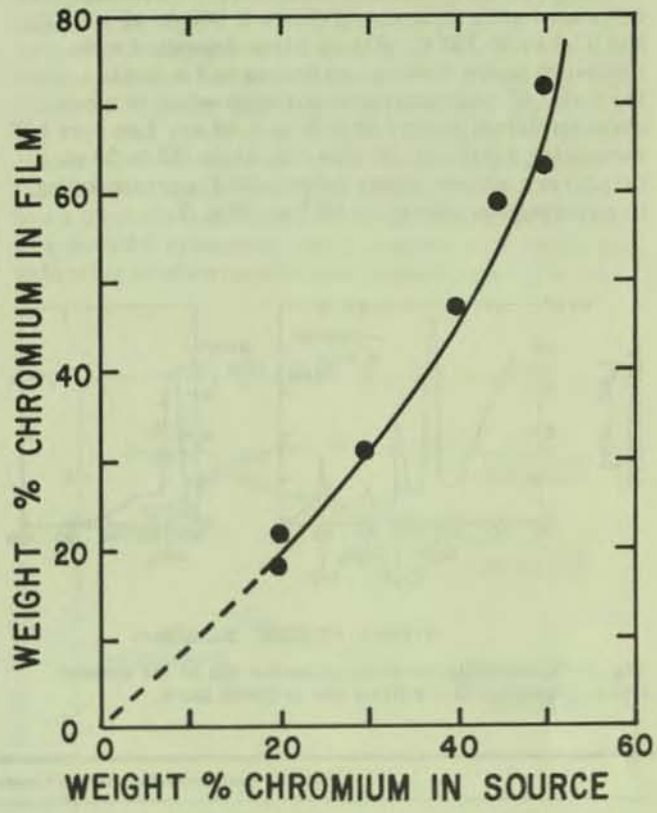


Fig. 3—Film composition vs source composition.

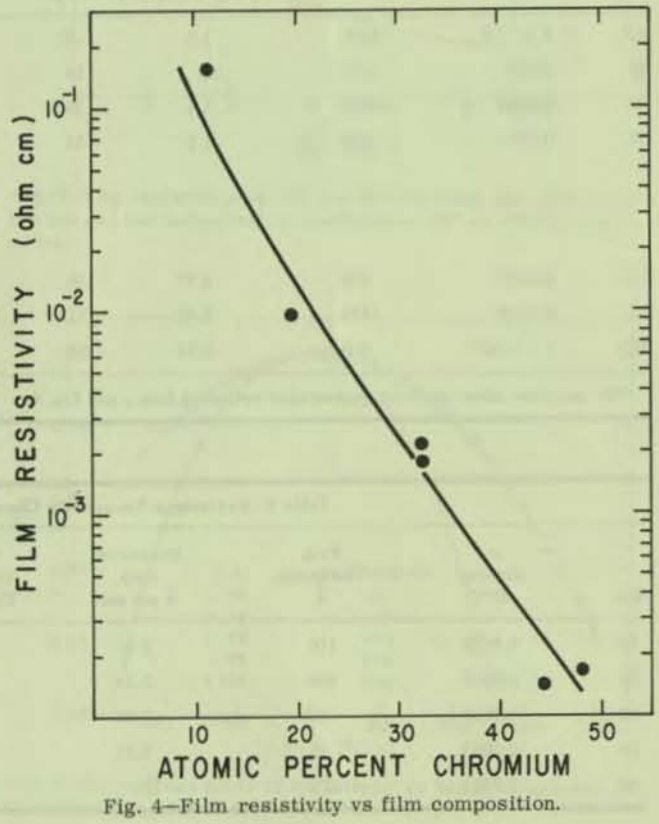


Fig. 4—Film resistivity vs film composition.

at. pct Cr) the log ρ vs $1/T$ curves, Fig. 8, have a positive curvature (*i.e.*, the slope decreases as $1/T$ increases) as though some type of activated conduction mechanism were dominating such that the activation energy increases with temperature. Typical calculated activation energies are 0.003 ev at −150°C and 0.06 ev at 330°C. Silicon films deposited and measured under similar conditions had a linear log ρ vs $1/T$ characteristic corresponding to a constant activation energy of 0.62 to 0.63 ev. Log ρ vs $1/T$ curves for 0.005 to 0.01 ohm-cm films (22 to 25 at. pct Cr) are almost linear below −25°C corresponding to an activation energy of 10^{-4} ev, Fig. 7.

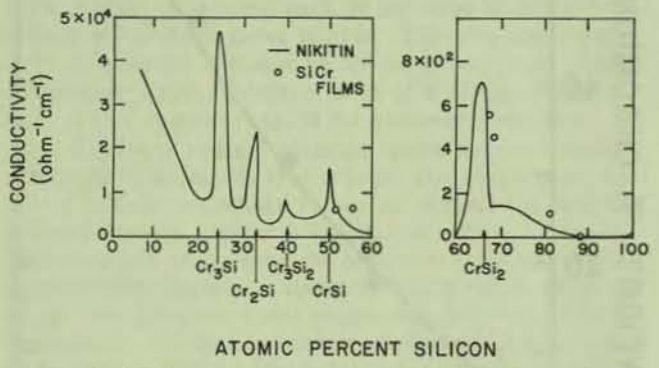


Fig. 5—Conductivity vs composition for the Si-Cr system[7] and for annealed Si-Cr films 700 to 2000Å thick.

In the intermediate resistivity range, 0.001 to 0.004 ohm-cm (27 to 34 at. pct Cr), where α changes sign, a resistivity maximum occurs at the inversion temperature. For the thin films listed in Table II, a plot of ρ vs T near the maximum is symmetrical, Fig. 9, and corresponds to the empirical parabolic relation:

$$\rho/\rho_i = 1 - A(T - T_i)^2$$

where $A = 1.1 \times 10^{-6}$, T_i is the inversion temperature, ρ_i is the resistivity maximum, and ρ is the resistivity at any temperature T where $|T - T_i|$ is less than 150°C. Run 105 (0.0027 ohm-cm) had a resistance maximum at about 250°C and was the only thick film that had an observed inversion. The ρ vs T curve is also symmetrical about T_i and the above relation true for $|T - T_i|$ less than 100°C and $A = 2.7 \times 10^{-6}$.

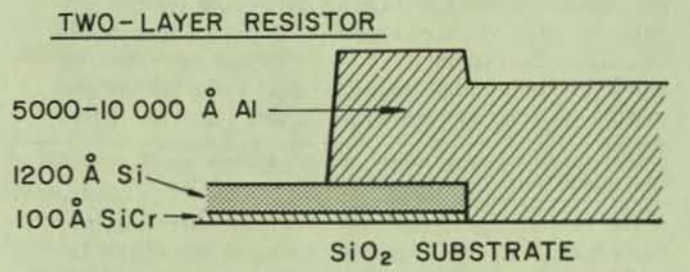


Fig. 6—Cross section of contact area of Si-Cr resistor with silicon overlayer.

Table I. Resistance-Temperature Characteristics of Thick Silicon-Chromium Films

Run	ρ, ohm-cm, 25°C	Film Thickness, Å	Deposition Rate, Å per sec	At. pct Cr	α, ppm per °C, 50° to 150°C	Apparent Activation Energy, ev 77° to 158°K	573° to 633°K
AD	0.2	1600	1.3	9	−2150	0.007	0.07
35	0.067	1975	22.	14	−1530	0.003	0.06
BB	0.0095	1850	1.4	19.5*	−430	7×10^{-5}	0.02
AC	0.0057	660	1.1	25	−510	2×10^{-4}	0.02

Run	ρ, ohm-cm, 25°C	Film Thickness, Å	Deposition Rate, Å per sec	At. pct Cr	α, ppm per °C, 50° to 150°C	Temperature Range for $\rho = AT + B$, °C	A, ohm-cm per °K	B, ohm-cm
105	0.0027	970	0.77	30	+580	<75	2.1×10^{-6}	2.1×10^{-3}
BC	0.0018	1835	0.88	32.5*	+630	<125	1.3×10^{-6}	1.4×10^{-3}
102	7.4×10^{-4}	660	0.51	53	+740	<200	5.9×10^{-6}	5.9×10^{-3}

*By analysis; other chromium percentages estimated from ρ and Fig. 4.

Table II. Resistance-Temperature Characteristics of Thin Silicon-Chromium Films

Run	ρ, ohm-cm, 25°C	Film Thickness, Å	Deposition Rate, Å per sec	Silicon Overlayer Thickness	Temperature Coefficient, ppm per °C 77° to 162°K	50° to 150°C	T_i Inversion Temp, °C
78	0.0028	100	0.31	1300	+226	−100	49
52	0.0033	100	2.3	2170	+190	−122	37
88	0.0034	~60	0.41	1200	+185	−200	10
79	0.0035	95	0.33	1240	+41	−280	−100
38	0.0051	275	11.	None	+178	−187	0

For thick films having resistivities less than 10^{-4} ohm-cm, the high-temperature portion of the resistivity-temperature curve becomes linear with temperature. As indicated in Table I, the lower the resistivity, the lower the temperature at which ρ vs T becomes linear. For films containing over 50 at. pct Cr, the resistance is linear from –196° to +200°C. At temperatures above the linear range, the ρ vs T curves have a decreasing slope.

A plot of the temperature coefficient of resistance between 50° and 150°C, α, vs film resistivity, ρ, is shown in Fig. 10. For films thicker than 500Å, α and ρ are related empirically by: α(ppm/°C) = –2900 – 1140 log ρ (ohm-cm), (indicated by the solid line in Fig. 10). For films thinner than 200Å, the intercept in the above relation is –2960, with the slope remaining the same. Near a resistivity of 3.5×10^{-3} ohm-cm (~27 at. pct Cr), α changes from positive to negative.

Film Structure and Conduction Behavior. Replica electron micrographs of Si-Cr films before and after annealing show a very fine-grained structure with little discernible change occurring during the heat treatment.

Electron diffraction patterns of films deposited at 300°C were obtained before and after annealing at 550°C for 5 min. Before annealing, diffuse silicon diffraction rings indicate that almost amorphous silicon is present up to about 33 at. pct Cr, at which composition Cr_3Si rings appear. The Cr_3Si lines increase in sharpness with increasing chromium content. Annealed samples show Cr_3Si rings at 10 at. pct Cr, increasing in sharpness to about 33 at. pct Cr. No lines corresponding to other silicides or to chromium were detected. Typical diffraction patterns are shown in Fig. 11. The Cr_3Si rings begin to disappear in the annealed films at about the same composition at which the film resistivity starts increasing rapidly. Cr_3Si has a positive temperature coefficient characteristic of a metallic conductor, and a positive Hall coefficient, indicating predominantly hole conductivity.[8] The re-

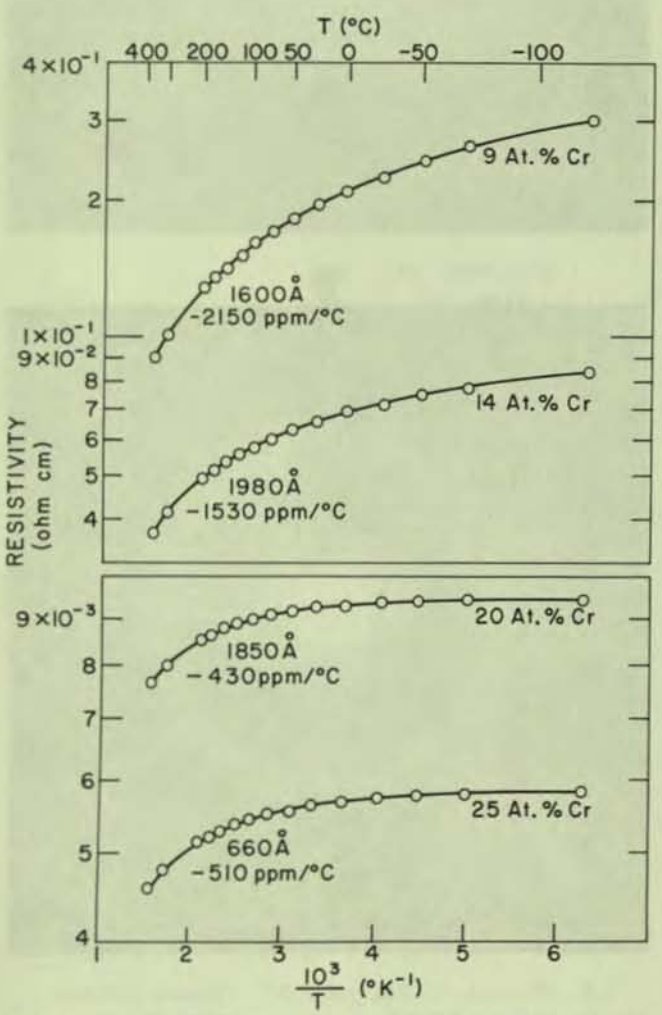


Fig. 7—Log resistivity vs $1/T$ for Si-Cr films; the film thicknesses and the temperature coefficients (50° to 150°C) are noted.

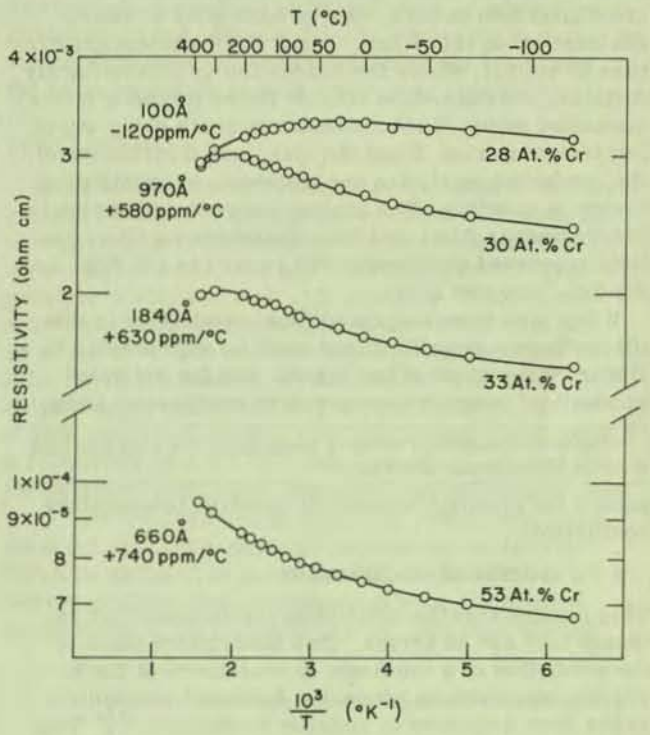


Fig. 8—Log resistivity vs $1/T$ for Si-Cr films; the film thicknesses and the temperature coefficients (50° to 150°C) are noted.

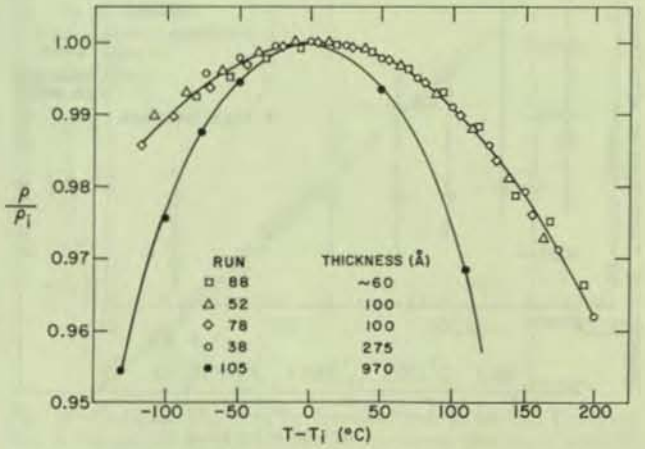


Fig. 9—Normalized plots of resistivity vs temperature for films having a resistance maximum.

ported resistivity of Cr_3Si ranges from 22[7] to 35 ± 5 microhm-cm.[6,9] The lower value is probably more reliable since conductivity maxima occur at stoichiometric compositions in the Si-Cr system, Fig. 5, and impurities also tend to decrease the conductivity. It seems probable that Cr_3Si is the dominant conducting component in annealed Si-Cr films containing between 10 and 50 at. pct Cr. Cr_3Si also has been reported to be a major conductive component in annealed Cr-SiO films.[10]

Below 25 at. pct Cr (25 vol pct Cr_3Si) activated conduction occurs, suggesting that the Cr_3Si is dispersed within an amorphous silicon medium and that the conduction mechanism may be similar to that for discontinuous thin metal films. The intermediate range of 29 to 38 vol pct Cr_3Si, where the temperature coefficient inversion occurs, may be analogous to island coalescence in thin films. For a Cr_3Si content greater than 60 vol pct, where the conduction is predominantly metallic, the chromium silicide phase probably forms connected paths. These effects are more clear-cut at low temperatures. Since the sizes and distribution of the conducting particles are unknown, no quantitative theory is possible. The analogy between conduction in heterogeneous films and thin discontinuous films has been suggested previously with regard to Cr-SiO[10] and Au-SiO_2[11] cermet films.

It has also been suggested[12] that conduction in thin discontinuous metallic films could be represented by a linear combination of two terms: one for activated conduction* (negative temperature coefficient) and a second for metallic conduction (positive temperature coefficient):

$$\rho = \rho \text{ (activated)} + \rho \text{ (metallic)}$$

This implies that the conduction mechanisms act as though they are in series. This assumption leads to the prediction of a minimum in resistance at the inversion temperature where the dominant mechanism shifts from activated to metallic conduction.[12,14] This minimum has been observed for thin gold and platinum films.[12]

*Proposed mechanisms of activated conduction in thin films have been reviewed by Neugebauer and Wilson.[13]

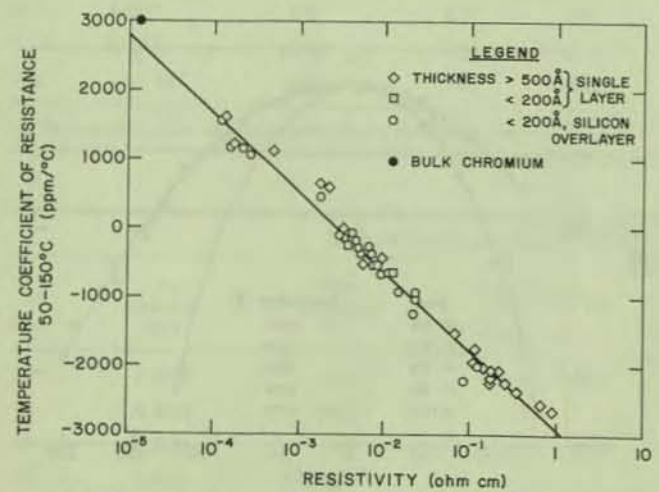
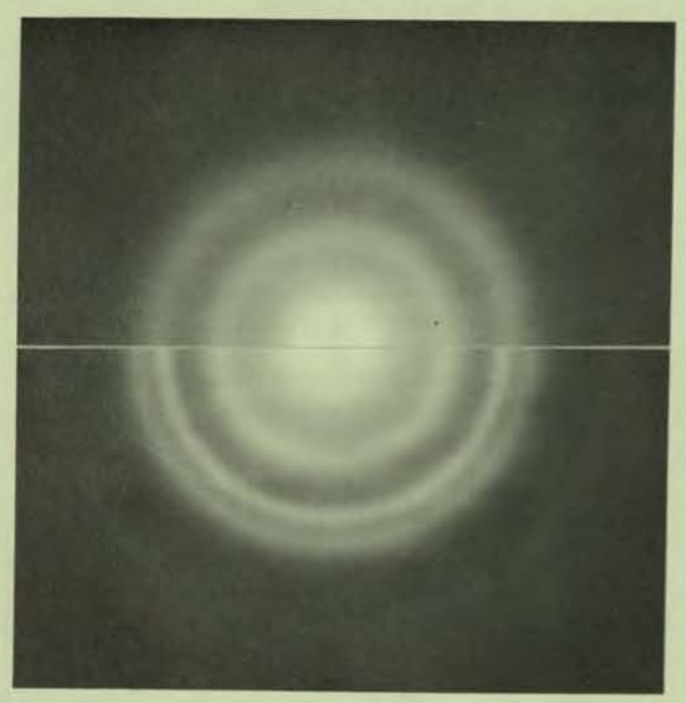


Fig. 10—Temperature coefficient of resistance vs resistivity for Si-Cr films.

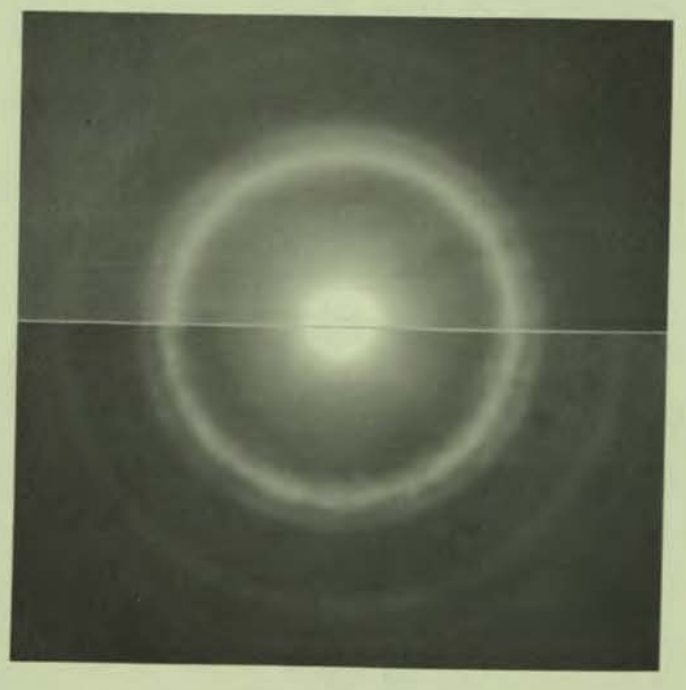
If one assumes that activated and metallic conduction mechanisms act in parallel, *i.e.*:

$$\frac{1}{\rho} = \frac{1}{\rho \text{ (activated)}} + \frac{1}{\rho \text{ (metallic)}}$$

then a maximum in resistance is predicted at the inversion temperature.[14] Resistance maxima have been observed in thin chromium films[15] where the resistivity is dominated by impurities, probably oxides, in-



(*a*)



(*b*)

Fig. 11—Electron diffraction patterns of Si-Cr films before (top) and after (bottom) annealing at 550°C for 5 min: (*a*) silicon, 12 at. pct Cr, 850Å thick; (*b*) silicon, 44 at. pct Cr, 1100Å thick.

troduced during the deposition process. For such films the mean free path of the conduction electrons was found to be less than 30Å and was not affected by film thickness. This is also probably the case for the Si-Cr films described here. This is consistent with the fact that the relation between α and ρ is not sensitive to film thickness for films thinner than 200Å.

An equation having two terms, one for activated conduction with a single activation energy and a second for metallic conduction linear with temperature, did not fit the Si-Cr data for either series or parallel combinations of the two terms.

Resistor Stability. Canned resistors were stored at 200°C and their room-temperature resistance measured at intervals up to 5000 hr. All resistors had been annealed at 550° to 565°C for 2 to 10 min prior to dicing and canning. Resistor stability was independent of thickness for 0.1 to 0.2 ohm-cm films between 400 and 2000Å.

A silicon overlayer improved the stability of thin resistive films as shown in Fig. 12. Three split runs were represented, having a resistive film thickness of 130 to 280Å, with a silicon overlayer of 1200 to 1700Å on half the units from each run. The film resistivities were 0.005 to 0.01 ohm-cm and the sheet resistances were 2 to 10 kohm per sq. The change after 5000 hr was 0.2 to 0.3 pct for the resistors with a silicon overlayer and about 0.5 pct for those without the overlayer. The measurement uncertainty was about 0.1 pct. The resistive film deposition rates were 2 to 11Å per sec.

The pct change vs time at intervals up to 5000 hr is shown in Fig. 13 for three runs (forty-three units), 80 to 130Å thick, having a 1000 to 1300Å silicon overlayer, and a sheet resistance of 6 to 7 kohm per sq. The deposition rate for the resistive films was about 0.4Å per sec. The resistor values decreased during the first 24 hr; thereafter they increased but changed little between 200 and 2000 hr.

No load-life tests were made since these resistors were studied for possible application in low-power digital and linear integrated circuits, where each resistor would dissipate less than 20 μw of power.

Application to Integrated Circuits. As indicated by the scatter of points in Fig. 2, reproducibility of sheet resistance by electron-beam deposition was not demonstrated. Reproducibility could probably be achieved by adequate control of the source temperature, or by an alternate deposition technique such as sputtering. Resistors in the range of 7 to 10 kohm per sq having a silicon overlayer have been successfully fabricated on the same chip with high-β, low-power transistors.

CONCLUSIONS

Si-Cr films show promise as stable (200°C storage) resistive elements having sheet resistances from 100 ohm per sq up to 10 kohm per sq and temperature coefficients between +600 and −600 ppm per °C. Temperature coefficients of ±100 ppm per °C can be obtained in the sheet resistance range of 250 ohm per sq to 3.5 kohm per sq. The average temperature coefficient of resistance, α, between 50° and 150°C is related empirically to the film resistivity, ρ, by α (ppm per °C) = $-2900 - 1140 \log \rho$ (ohm-cm). Near a resistivity of 3.5×10^{-3} ohm-cm (30 at. pct Cr), the temperature coefficient changes from positive to negative. The temperature at which the resistance maximum occurs increases with decreasing resistivity. Electron diffraction patterns showed the films to consist of Cr_3Si and amorphous silicon. Resistors thicker than 150Å typically drifted less than 0.6 pct

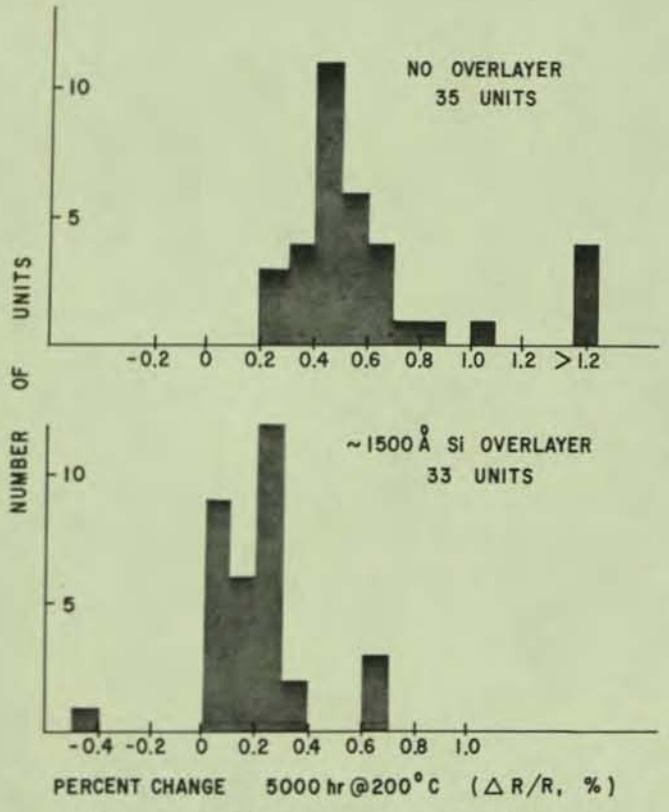


Fig. 12—Comparison of Si-Cr resistor stability for three split runs with and without a silicon overlayer; resistor film thickness 130 to 280Å.

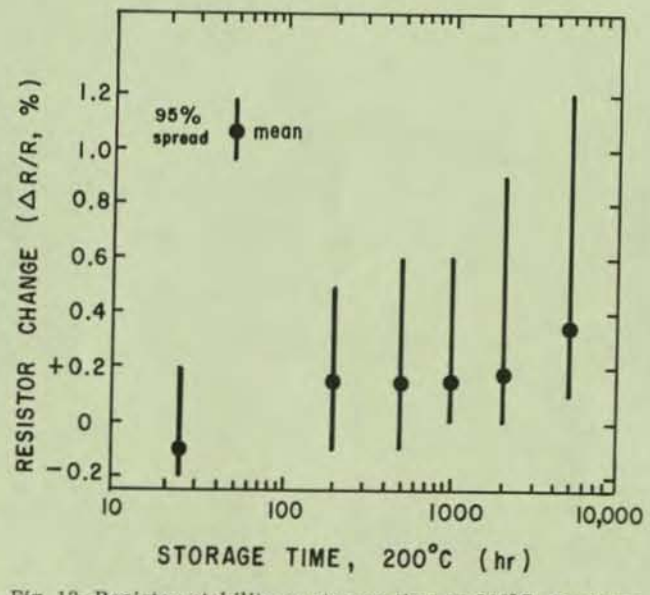


Fig. 13—Resistor stability vs storage time at 200°C. Resistor film thickness 80 to 130Å, silicon overlayer thickness 1000 to 1300Å, film resistivity 5 to 8×10^{-3} ohm-cm (5 to 7 kohm per square). Three runs, forty-three units.

after 5000 hr storage at 200°C. Resistors as thin as approximately 80Å that had a silicon overlayer showed similar stability. Such films had sheet resistivities of 10 kohm per sq and temperature coefficients near −600 ppm per °C.

ACKNOWLEDGMENTS

The assistance of O. Uyeda, who performed the film depositions and thickness measurements, is greatly appreciated. I am also indebted to E. Meieran and D. Mattern for the electron diffraction and electron microscopy studies, to R. Ceynowa and B. Yurash for the film analyses, and to J. F. Campbell, Jr. for the initial analysis of the Si-Cr resistance-temperature data and for his aid in preparing this paper.

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Reprinted from THE REVIEW OF SCIENTIFIC INSTRUMENTS, Vol. 38, No. 2, 277–278, February, 1967
Printed in U. S. A.

Interferometer Jig for Film Thickness Measurement

OSAMU UYEDA

Fairchild Semiconductor, A Division of Fairchild Camera and Instrument Corporation, Palo Alto, California 94304

(Received 13 September 1966; and in final form, 19 October 1966)

THE thickness of thin films is often measured by Tolansky multiple beam interferometry.[1] Tolansky described a simple jig that can be used to bring the Fizeau plate into the proper relationship with the object being measured. This type of jig, having three adjustment screws, requires experience and a certain degree of skill in order to achieve the desired fringe spacing and alignment with respect to the thin-film step.

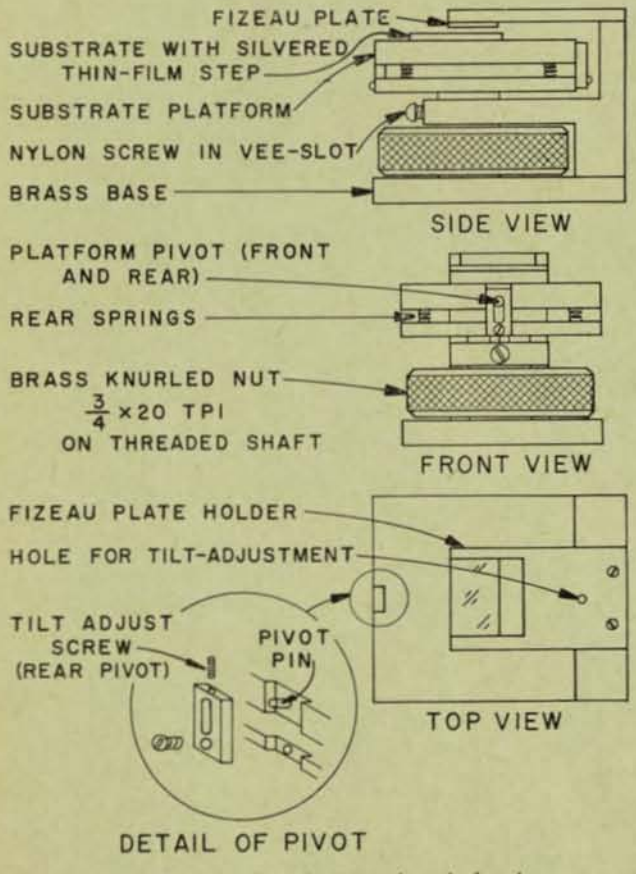

FIG. 1. Interferometer jig, approximately ½ scale.

Modifications of the Tolansky design employing three differential screws have been described by Gould and Pick[2] and by Klute and Fajardo.[3] Both jigs allow alignment of the fringes in any direction, and are better suited to micro-topographic studies than to routine thin-film thickness measurements.

An interferometer jig for thickness measurements has been designed, having a single adjustment nut, that automatically achieves the proper wedge angle between the Fizeau plate and the thin-film substrate (Fig. 1). The jig is used with a Bausch and Lomb microscope fitted with a Leitz sodium-vapor microscope illuminator and an American Optical Polaroid camera adapter.

The main parts of the jig are machined from aluminum alloy, except for the brass base and knurled brass adjusting nut. The knurled nut turns on a partially threaded post that supports a fixed top plate. Turning the nut raises and lowers the post and top plate; the bottom of the post slides within a hole in the brass base. The substrate platform is supported on the top plate by three weak helical springs (one centered near the front and two in the rear) and two pivots (front and rear edge) that allow the platform to tilt slightly in any direction. The rear pivot point can be raised or lowered by a 2-56 set screw. Adjusting this screw determines the initial (maximum) wedge angle formed between the Fizeau plate and the substrate. This tilt adjustment is required only after initial assembly of the jig. Rotation of the platform during raising or lowering is prevented by a pointed nylon screw running in a V-shaped key slot in the threaded post.

A 2.5×1.3 cm Fizeau plate is attached to the removable, U-shaped holder with two narrow strips of double-sided masking tape. The silvered thin-film substrate is placed on the platform with the step to be measured at right angles to the front edge of the Fizeau plate. The knurled nut is then rotated to raise the substrate toward the Fizeau plate. Because of the slight tilt of the platform with respect

to the Fizeau plate, initial contact is made at the front edge of the plate. The single pivots at the front and rear of the platform allow automatic alignment of the front edge of the Fizeau plate with the substrate. At this point, after initial assembly, the tilt adjusting set screw is positioned to give the minimum desired fringe spacing. Further rotation of the knurled nut reduces the wedge angle and increases the fringe spacing. Still further rotation brings the Fizeau plate into complete contact with the substrate and the platform moves downward against the support springs, minimizing damage to the Fizeau plate and substrate. In many instances, a small Fizeau plate would be advantageous, and could be accommodated by modifying the Fizeau plate holder.

Note that the tilt adjusting set screw determines the minimum fringe spacing achieved when the Fizeau plate first makes contact with the substrate. During thickness measurement, the optimum fringe separation is adjusted by means of the knurled nut. A 5 cm diam nut having a $\frac{3}{4}$-20 thread gives adequate control over the wedge angle; a differential screw adjustment was found to be unnecessary.

An inexperienced person can learn to use the jig with one lesson, and subsequent sample alignments take only a minute or two.

I am grateful to J. F. Campbell, Jr., and R. K. Waits for their encouragement and advice.

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