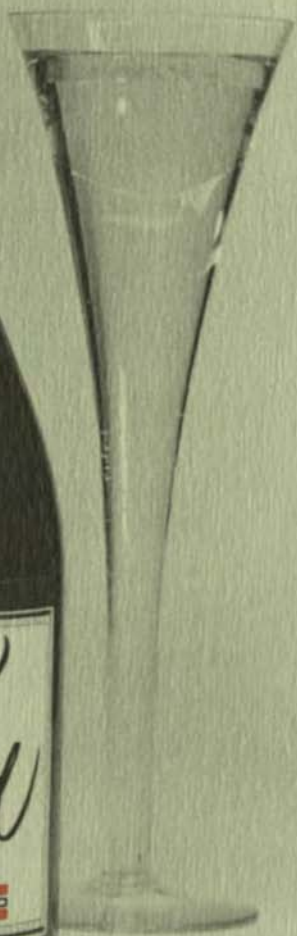


Silicon Valley Wayfairers Association
1044 Forest Avenue
Palo Alto, CA 94301



INVITATION



You're invited to a party to celebrate the memory of Fairchild Semiconductor and to give our thanks to the prolific progenitor of Silicon Valley.

Come visit with founders, friends and fellow-alums. There'll be food, drink, music and memorabilia of a time when we didn't have to ask if we were having fun.

Date: Thursday, April 14, 1988

Time: 6 to 11 P.M.

Place: Hyatt Rikeys Ballroom
4219 El Camino Real
Palo Alto, CA

Admission: \$25.00 per person (advance)
\$35.00 per person (at the door)

Lavish buffet and one drink included in admission price.
(No host bar)

Space is necessarily limited so make reservations early. Make checks payable to: Silicon Valley Wayfairers Association (or SVWFA). Do not send cash. Tickets will be mailed for orders received by April 4, 1988

(Excess of receipts over expenses will be donated to charity)

Name: _____

Company Name: _____

Home Address: _____

Phone: _____

What years did you work at Fairchild? _____ to _____

Enclosed is \$ _____ for _____ tickets

I can't attend but please add me to your mailing list for future events.

*Please return this portion with your check, in envelope provided and send to:
Silicon Valley Wayfairers Association
1044 Forest Avenue
Palo Alto, CA 94301*

SVWFA
1044 Forest Ave.
Palo Alto, CA 94301

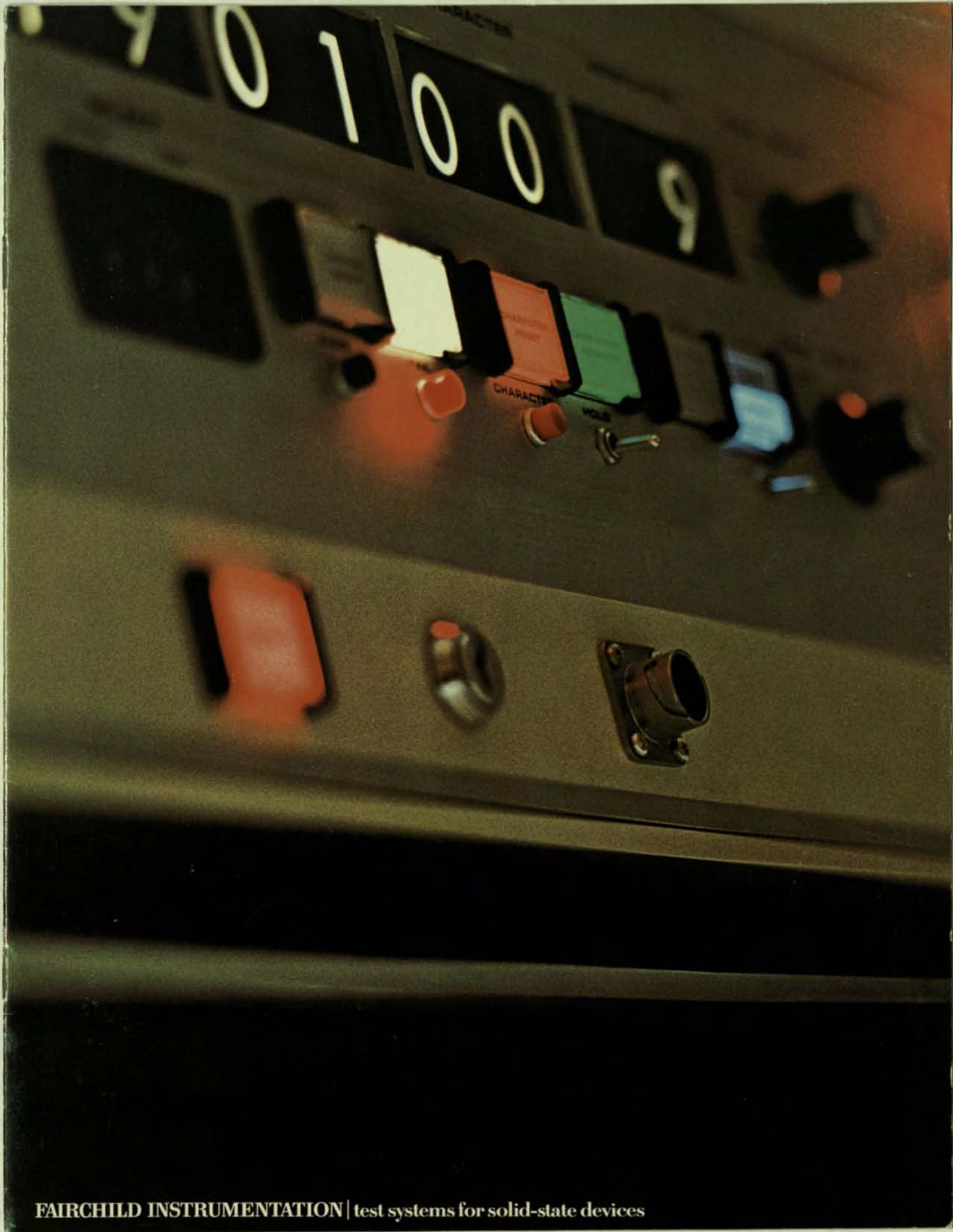
Stamp

Name:

Address:

Your tickets will be mailed to you in this envelope.
Please fill in your name and mailing address and
return this envelope with your order request,
in the envelope provided.

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FAIRCHILD INSTRUMENTATION | test systems for solid-state devices

Fairchild Instrumentation has manufactured and installed more semiconductor test systems than all other manufacturers combined. Almost every significant improvement made in such systems, from the early Beta testers of 1960 to the complex module testers of today, has come from Fairchild. This wealth of experience is reflected not only in technical excellence, but also in a serious concern with, and an ability to respond to, customers' needs.

Cecil Bradley
650-327-4224

USER ORIENTED SYSTEMS Fairchild Instrumentation was created to fill a growing need for reliable, accurate equipment to measure and test the performance of semiconductor devices. As the semiconductor industry expanded and its products became more complex, its needs for test equipment continued to multiply and grow in sophistication. Today there are more than 500 Fairchild Instrumentation test systems in operation, ranging from simple Beta testers to automatic high speed systems capable of testing 144-pin modules. These systems are located throughout the world, and are used by every major semiconductor manufacturer, and by high-volume semiconductor users.

Every Fairchild system is fully protected by a one year free service warranty. Because of the large number of Fairchild test systems in operation, Fairchild Instrumentation maintains a separate, full-time service organization. Fairchild Service Engineers are not involved in sales activity. All of their time is devoted to keeping installed systems in top operating condition. Fairchild service is worldwide, and can be rendered, in most cases, within 24 hours. Every Fairchild Service Engineer is experienced, highly qualified, and has completed an intensive six-month training program at the Fairchild facility in Mountain View.

To assist customers in the efficient and trouble-free operation of their systems, Fairchild maintains a Customer Training School at Mountain View, where users may send selected supervisors, engineers and technicians to learn operating and routine maintenance procedures. Courses range from two to three weeks and include programing, system diagnostics, maintenance, functional operation, and actual use of the equipment.

The user oriented system from Fairchild is more than hardware. It is a functional solution to a user's requirement. Long before the system configuration is finalized we establish contact with the user organization at responsible engineering levels. By assisting the customer in choosing system options, and by making modifications where required, we make sure that the system will fit the need. After the system becomes operational we maintain contact through our service organization to make sure that it will keep functioning for as long as a need for it exists.

TESTING CAPABILITIES Fairchild Instrumentation makes three basic types of semiconductor test systems: those designed to test discrete transistors; those designed to test integrated circuits; and those designed to test large scale integration (LSI) circuits or monolithic complex arrays. These systems range in size and scope from simple, hand operated testers to large scale systems which automatically handle the devices, test them, classify them and record the test results. Because a system used for laboratory testing of prototype devices has different requirements than a system used for production line testing, Fairchild Instrumentation offers a wide range of options with each system. By selecting the options suited to his specific needs, each user gets a custom tailored system, yet without having to pay the prohibitive development costs of building the system from scratch. Fairchild test system options fall into four basic categories: programing options; instrumentation and switching time options; environmental and device handling options; and data logging options. Most of these optional capabilities are available for every system type.

Programing: All Fairchild Instrumentation test systems are programable and feature magnetic disc storage. The magnetic disc affords the capability to store many types of tests with many parametric variations, to execute them in any desired sequence, and to change tests or test sequences at will. Specific programing features particular to each system will be discussed on the following pages.

Instrumentation and Switching Time: Most Fairchild systems offer a number of instrumentation options and switching time capabilities to suit special customer needs. Larger systems offer multiplexing capabilities, allowing several test stations to operate from a single central processor. Multiplexing capabilities are also available to permit functional and parametric testing of complex digital modules, at any station.

Environmental and Device Handling Options: Where systems are used for production line applications, Fairchild makes available several options for automatic handling and classification of devices. These options range from a series of classification lights and counters, to systems capable of automatic device handling, testing, classification and sorting, with the devices deposited in appropriate bins at the end of the test sequence. An environmental chamber is available, which automatically brings the device to be tested to the required temperature, then performs the test.

Self-Calibrating Single Socket: One of the most significant options available for Fairchild integrated circuit test systems is a self-calibrating single socket that permits DC linear and dynamic tests to be performed in a single test socket. A Fairchild "first," the self-calibrating single socket uses MOS active probes, and calibrates itself by making voltage checks against a reference voltage prior to each dynamic test—a procedure that effectively eliminates inaccuracies due to probe and sampling bridge drift, and gain nonlinearity.

Data Logging Options: All popular readout and data logging devices can normally be accommodated on Fairchild systems. Options available include digital and scope readouts, hard copy typewriters, paper and magnetic tape equipment.

Computer Compatibility: The programable capabilities inherent in Fairchild systems are sufficient for most applications, so that no further capability from a computer is normally required. However, where the application calls for computer tie-in, Fairchild systems may be interfaced with virtually any computer on the market today.

Customized Systems: Because of the wide variety of applications for which Fairchild test systems are used, there may be occasions where the standard options available do not meet all the requirements. Fairchild systems are built with an expansion capability, which allows special modifications to be made on a system at a minimal cost. Fairchild Customer Engineers are available for consultation to evaluate special requirements.





Fairchild discrete component test systems include the Series 300 Transistor-Diode Tester, the Series 500 Test System, and the Series 600 Test System. □ The Series 300 is a GO/NO-GO tester for transistors and diodes. It operates on a dynamic load-line principle, and is programed by means of plug-in resistor cards. It is designed primarily for large volume testing and classification.

The Series 500 Test System performs DC, pulsed and 1kHz small signal tests on transistors, diodes, SCR's, and zener diodes. The basic system is switch programed and offers digital readout. Optional capabilities include GO/NO-GO decisions, single or dual limit testing, programing and data logging. The system is capable of both high power and high sensitivity measurements.

The Series 600 performs DC and pulsed tests on transistors, diodes, and reference diodes at speeds up to 100 tests per second, with digital readout and GO/NO-GO decisions. Programing is simple and can be performed by unskilled personnel. The Series 600 is programed by digiswitches or magnetic disc, and executes many test types in any sequence, or one test type with many bias conditions and limits. Up to 21 tests can be switch programed and several hundred by magnetic disc or computer. Classification into 20 categories is optionally available. Connectors are provided for interfacing to automatic handling and sorting as well as data logging equipment. Simplicity of operation is stressed in the basic system. Automatic ranging and placement of the decimal point in the digital readout is provided, and many safety features are incorporated to protect the operator, the system and the device under test.

The system can test leakage, breakdown voltage, latching voltage, DC forward current transfer ratio (displayed directly as the ratio I_C/I_B), saturation voltage and base turn-on voltage. Tests are performed on one power pulse per test programed. DC equivalent tests are made with long pulses (40 milliseconds) while high power tests such as latching voltage, DC gain and saturation tests are made with short (400 microsecond) pulses. A special safety feature automatically switches to the short pulse if high power tests are erroneously programed on a DC basis. Fail lights indicate which tests failed to meet the programed limit, while digital readout windows provide 3-digit indication of the result, the parameter measured and the unit of measure. The system provides ten picoampere resolution on leakage measurements (10 nanoamperes full scale), and collector current is programable from 1 microampere to 10 amperes.

System operation is simple and consists of inserting the device into one of two sockets. The operator then slides over a cover, exposing a second socket which he proceeds to load. Before he can load the second socket, tests are already complete on the first, so that the only limitation on production speed is the manual dexterity of the operator.

The accuracy, versatility and speed of the Series 600 system make it suitable for every kind of transistor and diode testing, in incoming inspection, quality control, reliability testing, device characterization and production line testing applications. For further information on the Series 600 return the enclosed self-addressed, prepaid postcard.





Fairchild integrated circuit test systems include the Series 4000 and the Series 5000 systems. □ The Series 5000 test system incorporates functional and attractive design, high reliability and speed, and versatile and powerful programming into a system of extraordinary capabilities. Over 1,800 integrated circuits are used in the circuitry of this system to achieve increased system reliability and reduced size. DTL logic is used to provide the highest operating speed and noise immunity consistent with economy and accuracy. The system tests all types of multi-lead solid-state modules, digital and linear integrated circuits. The basic system performs function, DC, DC linear tests, and offers AC, switching time and environmental tests as options. All tests can be performed automatically.

The key to the power of the Series 5000 system is a simple yet versatile programming capability. A magnetic disc is used to store more than 1,350 tests. A variable sentence length programming language is used to give greater flexibility and conserve disc storage space. The program sequence begins with certain set-up instructions, to program power supplies, for example. Once set up, these settings may remain constant and are held until they are reprogrammed. Thus, after initial set-up, the program needs only a few words to incorporate program clauses such as pin connections and pulse lengths. In this way the programmer's task is simplified, since he does not have to reprogram the entire system for each test. An important advantage of the variable length is that any number of options required for a test may be programmed in a single sentence. Hexadecimal characters are used, and over 100 addressable options may be specified. The programming language includes both conditional and unconditional jumps, affording the capability normally associated only with a digital computer system. For example, the system may be programmed to transfer to a subroutine when a test fails, and perform further tests to ascertain the causes of failure. Upon completion of the subroutine the system returns to perform the next test in the original sequence.

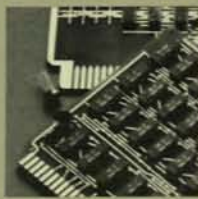
Programming is accomplished through a simple keyboard, eliminating cards and wire board techniques. Optionally the magnetic disc may be programmed through a high speed paper tape reader with tape prepared off-line. In either case, panel controls within easy reach of the operator give access to any disc location, any character, or any test word, to allow program modifications and on-line verification of all conditions. Testing and programming can be carried on simultaneously.

The standard system includes two measuring lines. These may be used to make a dual limit measurement against high and low limits, or two independent measurements, simultaneously, against separate limits. With the 200 tests-per-second option, this gives an effective test rate of 400 tests-per-second. Each of the two measuring lines is fully guarded through the matrix. Power pulses are programmable in 1msec. steps to 10msec., in 10msec. steps to 100msec., in 100msec. steps to 1 second and in 1-second steps to 10 seconds. A V/IFM instrumentation module allows maximum use of the Series 5000 capabilities. It can be used as a constant current generator or a voltage forcing source. In the current mode the module can measure voltage. In the voltage mode it measures current.

Another unique option available with the Series 5000 system is the self-calibrating single socket (see page 4). The single socket can be installed in the ambient test station or in the environmental chamber, to perform high accuracy AC, DC and switching time tests under all conditions. Up to 5 slave test stations can be multiplexed to operate with a single master test station on the Series 5000, to perform DC and dynamic measurements. Additionally, automatic device handling, classification, and sort equipment is available for high speed, high volume testing.

The complete capabilities of the Series 5000 can only be hinted at here. For complete information return the self-addressed, prepaid postcard enclosed.





The Fairchild Instrumentation Series 8000 test system is especially designed for functional logic tests of complex digital circuits. These circuits may be printed circuit boards, potted modules, large scale integration (LSI) circuits, thin and thick film circuits, multi-chip circuits, or system subassemblies. The Series 8000 can test such circuits having over 100 pins, at test rates in excess of 10,000 tests per second. With special pulsing options the test speed is extended into the megahertz region. The functional testing is accomplished by programing into the system memory a series of digital patterns. The input patterns are applied as synchronized data words to the inputs of the module under test, and all outputs are examined simultaneously to see that they are in the correct logic state and level. All pins of the module are designated either as input or output; if a pin is defined in the test memory as an input it will be connected to an input conditioner and forced into the correct state during the test. If a pin is defined as an output, it will be connected to a load board and level comparator, and will be tested to determine that it is in the correct state for that test. Testing of all output pins occurs simultaneously. A search mode is provided to insure that the system is testing the device to the correct truth table, taking into account the state of all internal, inaccessible memory elements. In this way devices which contain memory cells with no reset capability can be tested satisfactorily.

The standard magnetic disc provided with the system provides storage for 1,800 test words and test rates of 1,000 tests per second. A larger, faster disc is optionally available with 50,000 test word storage capacity, and rates of up to 10,000 tests per second. Pin capability can be expanded to accommodate devices with more than 144 pins. Magnetic disc programing is accomplished either through a keyboard or high speed paper tape. GO/NO-GO results are visually displayed, and additionally may be data logged along with information on which test failed, and which pins of the module under test gave the erroneous readings.

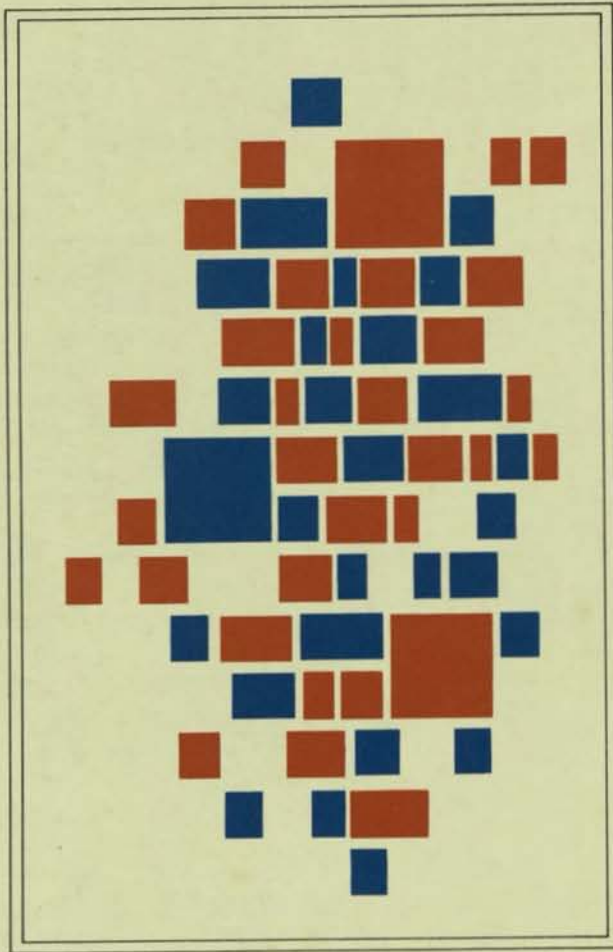
Where diagnostics must be performed to determine further the causes of failure, several techniques are available. Each test has independent addressing of subroutines, and upon failure the system may be instructed to proceed to a diagnostic test routine in an effort to pinpoint the failure. An oscilloscope can also be provided in the system, and can be used with a sync/stop selector to recirculate a mode of operation. In this way the operator can obtain a continuous trace of a particular test sequence and visually determine possible causes of the failure.

The Series 8000 is a unique system. No other system currently available can match either its speed or the number of pins it can test in a single operation. For complete information on the Series 8000 system return the enclosed self-addressed, prepaid postcard.



FAIRCHILD
INSTRUMENTATION

**MICROMOSAIC™
ARRAYS
... AN MOS
APPROACH
TO CUSTOM
LSI**



The Micromosaic™ Array Concept

The 3400 Micromosaic™ Array utilizes Metal Oxide Silicon (MOS) technology to fabricate high complexity digital arrays. It offers the use of a standard circuit library, a standardized interconnection system, and computer controlled automated design procedures to build custom digital subsystems quickly and economically. The objectives of the 3400 family are to implement large numbers of custom Large Scale Integration (LSI) subsystem functions with a low design cost, short turnaround time, and a highly flexible custom capability. Low and medium volume custom arrays, not economically feasible utilizing "hand-crafted" techniques, can be implemented with the Micromosaic array concept.

To meet these objectives, the 3400 Micromosaic Arrays have been specifically designed to utilize automated computer design techniques. Standard functional building blocks (or "cells") are utilized to realize the actual circuit portions of each custom subsystem. The use of predesigned, thoroughly characterized, standardized cells provides fast turnaround time, and a large volume of data from which reliability and failure-mode predictions may be made.

These standard building blocks are systematically interconnected by regular orthogonal interconnection line segments placed along the lines of an imaginary X-Y grid and proceeding between grid intersections. This grid-oriented interconnection system not only facilitates systematic routing as required for automated design, but it also obviates the need for dimensional considerations beyond the initial design of the array family.

The benefits of fast turnaround time and systematic design procedures would be negated if the degree of standardization required to realize them resulted in such inefficient area usage that subsystems of true LSI complexity could not be economically integrated. Several factors ensure that area efficiency will be maintained in the development of custom Micromosaic arrays. First, there is a wide variety of standard functional blocks (over 35) so that the various internal functions of a custom array are implemented as concisely as possible. Moreover, each of these cells has been topologically optimized. The extent of the library ensures sufficient flexibility to let the array family be useful in widely differing types of appli-

cations. Second, unlike the bipolar Micromatrix™ arrays, the cell patterns are not prediffused and the location of each functional block is selected during the design phase to minimize the total length and physical complexity of the interconnection system. Finally, both the cell patterns and the interconnection system take full advantage of present day technology to conserve surface area.

Organization of A Custom Array

As the preceding remarks indicate, a custom subsystem implemented with the Micromosaic array capability is composed of predesigned building blocks which have been systematically placed and interconnected to form a monolithic array of cells. The organizational diagram of Figure 1 illustrates the important features of such a composed array. The individual cells, which may be considered as dimensional blocks with terminals, are uniform in height and are arranged in rows as shown on the diagram. Since complexity varies with the function, the width is varied to accommodate various numbers of devices. The voltage and ground supplies are

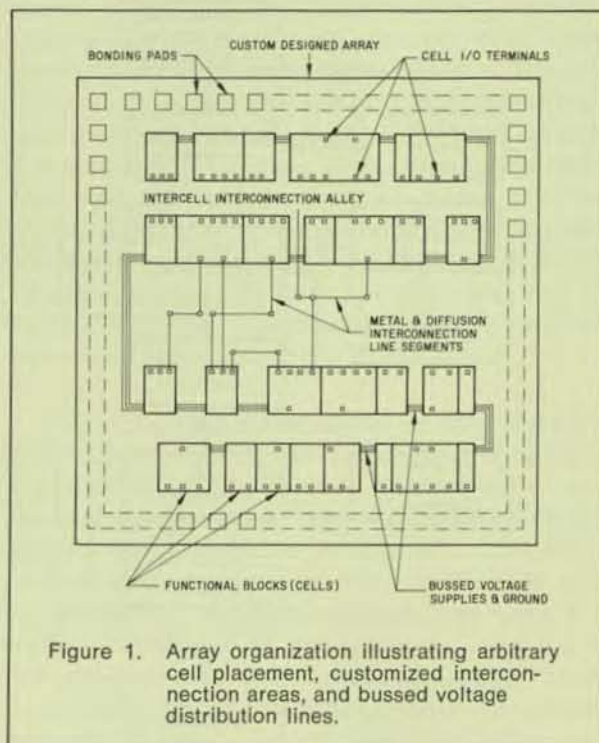


Figure 1. Array organization illustrating arbitrary cell placement, customized interconnection areas, and bussed voltage distribution lines.

bussed horizontally through each cell and the rows of cells may be rotated about these voltage busses to place the cell terminals in the most advantageous position. Total cell count and the

number of different cell types are determined entirely by the logic requirements of the subsystem under development. Finally, the height of the interconnection alleys between rows of cells is also a design variable which is determined by actual "wire" density. The flexibility inherent in this "composition approach" to LSI enables efficient usage of silicon surface area.

Computer Aided Design

The 3400 Micromosaic™ Array has been specifically designed to make maximum use of Computer Aided Design (CAD).

CAD is obviously not required for LSI, because some very complex MOS designs have been produced using conventional techniques. But for Micromosaic arrays, where low engineering costs and fast turnaround time are paramount, CAD is a necessity. The present Fairchild CAD procedure, as it relates to Micromosaic

arrays, is shown in Figure 2. The CAD system is entered after system and logic design have been completed. The cell interconnection of the proposed Micromosaic array and a design verification test is coded in FAIRSIM format. FAIRSIM is Fairchild's digital simulation program. The array logic is then simulated to check for functional correctness and coding accuracy. This is followed by automatic cell placement and interconnection routing with manual intervention which increases the efficiency of this procedure. Once a satisfactory design has been accomplished, the master artworks are automatically generated on a computer-controlled cutting table, checked, and submitted to Mask-making. Meanwhile, the logical and final topological descriptions of the array are used as inputs to a test generation program which establishes a functional test sequence to test for all realistically possible shorts, opens, and stuck conditions within the circuit.

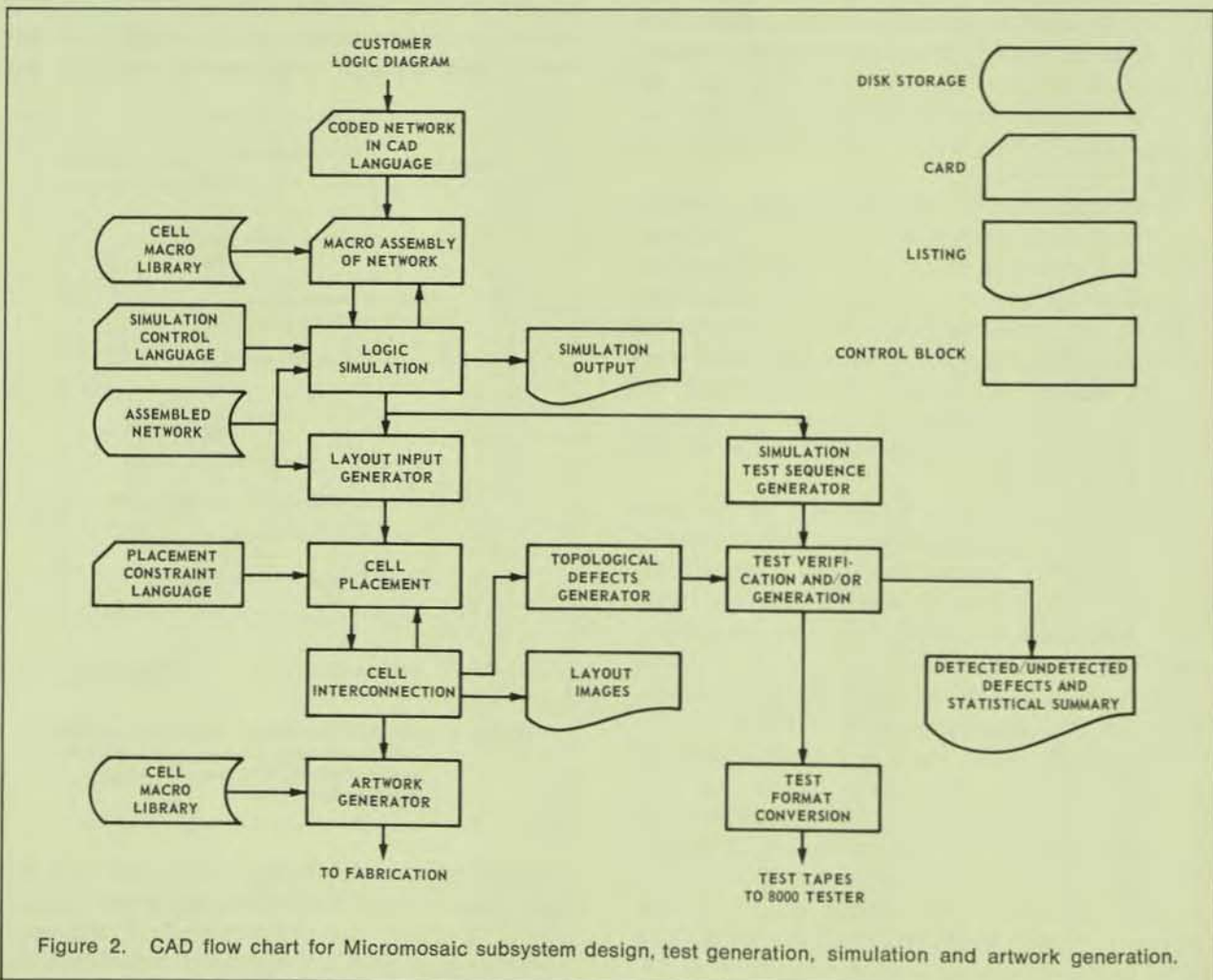


Figure 2. CAD flow chart for Micromosaic subsystem design, test generation, simulation and artwork generation.

Customer Interface

The economics of arrays have projected the semiconductor manufacturer into the business of subsystem fabrication. Where he once interfaced only with circuit and component engineers, he must now also communicate with system engineers, logic designers, and packaging engineers. The systems manufacturer, conversely, must become more aware of the process technology and its limitations. Since every customer has different expertise, manpower, design schedules, etc., no single interface definition can be made which will be optimum for all customers. In any case, the interface should be chosen so as to make the division and identification of responsibilities as well defined as possible. The necessary steps in a design are shown in Figure 2. The system requirements must be defined by the customer. The areas of logic design, verification, and CAD coding are in the flexible interface area and may be performed by Fairchild and/or the customer. Mask generation, fabrication, and testing must be done by Fairchild.

While many working relationships are possible, there are four primary types:

1. **Performance Specification:** The customer provides a system design and generates performance specifications. Fairchild then performs the logic design for minimum cost implementation. This may involve the use of one or more Micromosaic™ arrays, MOS standard products, interface circuits, multi-chip packages, etc.
2. **Logic Diagram Only:** The customer provides a logic diagram to Fairchild. Fairchild will analyze the design, generate test criteria, and perform computer simulation. The customer then analyzes computer simulation data and verifies design.
3. **Logic Diagram and Functional Test Criteria:** The customer provides logic diagram and functional test data. The logic is simulated and verified with test criteria. This approach requires less Fairchild involvement than does No. 2 above.
4. **FAIRSIM Interface:** Fairchild's computer simulation program provides a compact language for specification of Micromosaic arrays and associated test criteria. The *FAIRSIM User's Manual* (which is available upon request) provides detailed information of FAIRSIM use. The customer may elect to supply design data to Fairchild with FAIRSIM punched cards.

The logic simulation generated with the FAIRSIM program eliminates the need for breadboarding. (Breadboarding with MOS is impractical for arrays because the parasitic capacitance between logic functions is almost eliminated when functions are integrated using Micromosaic arrays.) The use of computer aided layout and mask generation obsoletes the need for pencil layouts.

To provide customer support with Micromosaic arrays, the Fairchild Array Systems Engineering group is available for consultation on all aspects of arrays including FAIRSIM programs. To aid in specifying a Micromosaic array, a technical specification form is provided at the back of this brochure. It outlines the type of information that is necessary to develop an array.

Micromosaic™ Array Logic Elements

The library of standard cells, with which the custom subsystems are implemented, is the backbone of the 3400 Micromosaic Array capability. In the design of the cell set, standardized device topologies for various circuit configurations were determined, and all cells have been constructed using these devices. The primary objective of the standardized geometries was that all internal logic cells have similar transfer characteristics. Thus, a standard MOS load resistor between the cell output and the V_{DD} supply is used in each circuit. Three transistor designs are used to ensure identical DC characteristics from circuits using one, two or three transistors "stacked" in series between the output terminal and the substrate.

With the input capacitance of the standard switching devices determined, capacitance loading due to fan-out on any internal node may be easily calculated from the logic diagram. Once a layout has been accomplished, the additional capacitance due to interconnections may be added to this input capacitance. Since the output impedance to the substrate or to V_{DD} is the same for all cells, a knowledge of node capacitance is all that is required to determine typical and worst-case on-chip propagation delay times.

Besides the internal logic circuitry, some additional cells have been designed and characterized for output buffering and on-chip clock

pulse generation. These circuits use different device geometries than the internal cells to provide higher drive capability.

Using standard device topologies, an extensive library of cells has been established to provide the flexibility necessary to implement a wide variety of logical designs. The individual cells are illustrated on the following pages. The NOR and NAND gates as well as the more complex "GA" or "gate array" logic elements require no explanation. Flip-flops are available for both single and two-phase clock operation as the logic diagrams indicate. The NAND and NOR expanders (PD, EXP, EXP3, NREX2, NREX3) are simply groups of gates that may be tied to other cell outputs to expand the function of that particular cell. These cells are especially useful for large NOR functions (in excess of five inputs) and for reducing logic complexity when true and complement signal

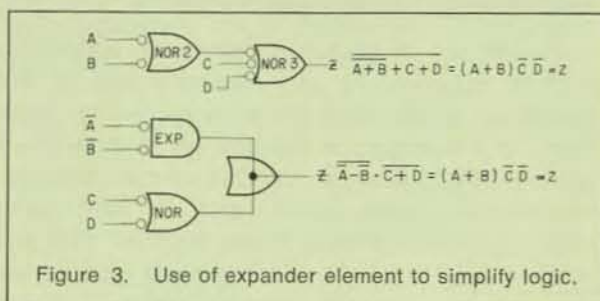


Figure 3. Use of expander element to simplify logic.

polarities are available. Figure 3 presents a simple example of logic reduction. Note that one level of logic and one resistor node have been eliminated, thus improving speed and reducing power.

No "stored charge" or "transmission gate" circuitry is used in the design of these cells. All flip-flops are of "master-slave" type, similar to bipolar designs.

Operating Temperature Range

The features outlined in the cell circuit description allow Micromosaic™ arrays to be specified for use in industrial environments (0°C to +70°C) or military environments (-55°C to +125°C) using either high or low threshold material.

Logic Symbols

The logic symbols used for Micromosaic array cells are in accordance with MIL-STD-806B. This symbology, as it pertains to MOS circuitry, may be unfamiliar to some readers, so an explanation is in order. The military standard for graphic symbols used in logic diagrams, MIL-STD-806B, is probably the most popular logic symbol convention for bipolar logic. The symbols are defined by combination tables which describe the circuit in terms of "H" (highest algebraic voltage) and "L" (lowest or most negative voltage). Two symbols are defined for each circuit corresponding to the user's definition of "active level" or "logic one." Combination tables from MIL-STD-806B corresponding to the common MOS transistor connections are shown in Figure 4. By examination of the combination table we observe that the MOS series-string corresponds to the upper symbols, the parallel connection to the middle symbols, and the MOS "OR tie" (used with expanders) connection to

		TABLE OF COMBINATIONS			SCHEMATIC	
<p>AND</p>	<p>OR</p>	A	B	X		
		H	H	L		
		H	L	L		
		L	L	H		
		H	H	L		
		H	L	H		
		L	H	H		
		L	L	H		
		H	H	H		
		H	L	H		
		L	H	H		
		L	L	L		

Figure 4. Combination tables from MIL-STD-806B.

the lower symbols. Unfortunately, this is in contradiction to the most common industry usage which might be described as the 806B NOT convention for MOS symbols. The decision to use 806B notation with its somewhat unfamiliar symbols for Micromosaic™ array cells is not based on any "ivory tower" idealism, but our conviction that the continued use of the 806B NOT convention will result in a source of confusion and subsequent errors when designing systems using a combination of bipolar and MOS logic.

The Micromosaic array concept, with its low voltage capability, makes hybrid MOS/bipolar systems quite practical. It can be seen that use of the same logic symbol for devices with non-identical combination tables will result in a potential source of confusion and subsequent errors. In addition, where contracts specify compliance with MIL-STD-806B no costly re-formatting of logic diagrams is required. For Boolean descriptions of the cells, the common MOS convention of logic one = L, logic zero = H was used.

FAIRSIM Formats

Some customers may prefer to supply Fairchild Micromosaic array designs coded in FAIRSIM format on punched cards. The FAIRSIM format for each logic element is listed in the individual descriptions. Here is the array description format:

1. Designation: This is the name which the designer assigns a particular cell. Each name must be unique, begin with a letter, and be less than five characters long. The description is entered starting in Column 1 of an 80 column punched card.
2. Configuration: This is type or configuration of cell used such as NAND3, GA7, etc. The configuration is entered starting in Column 10.
3. Inputs: The designated names of the cells or array inputs which are inputs to the cell are listed here starting in Column 16. The exact order of these inputs is specified in the individual cell description.
4. Delay: The inverter delay is listed following the inputs. Delays may range from 0 to 63. The FAIRSIM model should be examined to determine the delay characteristics of a cell.

In addition to the cell description, a pad card is required per bonding pad. The bonding pads correspond to the package pins of the final unit.

The format consists of the signal name or designation starting in Column 1, and the word PAD starting in Column 10. If the signal is an input, the signal name will be the same as that shown for the appropriate cell inputs. If the signal is an output, the name will be the same as the cell which drives it.

An example of a completed coded Micromosaic array for an up-down counter is shown in Figure 5.

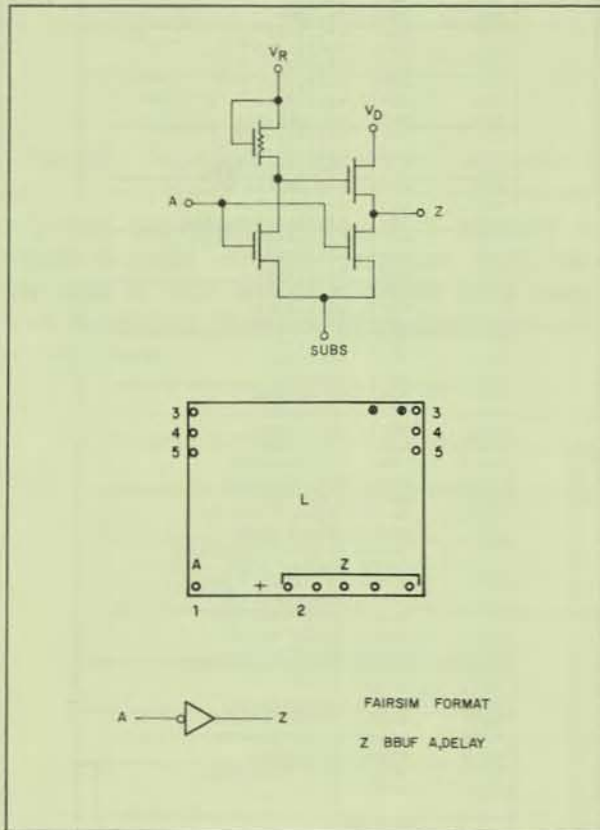
NET START		
BF1	BUF	FA1QN
BF2	BUF	FA2QN
BF3	BUF	FA3QN
BF4	BUF	FA4QN
BF5	BUF	N311
CG1	MPI	M11, SUB5
CG1N	MPI	N217, CG1
FA1	FSR	G412, CG1, CG1, G411, MR, CG1N
FA2	FSR	N219, CG1, CG1, N214, MR, CG1N
FA3	FSR	N220, CG1, CG1, N213, MR, CG1N
FA4	FSR	G442, CG1, CG1, G441, MR, CG1N
G31	GA3	N32, FA4QN, ND3, N33, PE, P1
G41	GA4	P0, PE, N24, FA1QN
G42	GA4	FA1QN, FA2Q, FA1Q, FA2QN
G43	GA4	ND7, FA3Q, N26, N34
G44	GA4	ND20, N24, PE, P3
G71	GA7	FA4QN, G711, BIN
M11	MPI	N217, SUB5
N21	NDR2	CLK, SUB5
N22	NDR2	BIN, SUB5
N23	NDR2	SUB5, UP
N24	NDR2	PE, SUB5
N25	NDR2	G31, SUB5
N26	NDR2	SUB5, G712
N27	NDR2	N23, ND9
N28	NDR2	ND17, SUB5
N29	NDR2	ND11, ND12
N31	NDR3	ND1, ND2, N21
N32	NDR3	N23, PE, G421
N33	NDR3	G422, PE, UP
N34	NDR3	FA1Q, FA2Q, FA3Q
N35	NDR3	N34, UP, FA4QN
N36	NDR3	N23, ND8, FA4Q
N37	NDR3	FA1QN, FA2QN, FA3Q
N38	NDR3	FA1Q, FA2Q, FA3QN
N39	NDR3	N211, N37, N38
N210	NDR2	ND13, ND14
N211	NDR2	G421, FA3QN
N212	NDR2	ND21, SUB5
N213	NDR2	N312, ND19
N214	NDR2	N215, N25
N215	NDR2	N216, N22
N216	NDR2	N32, N33
N217	NDR2	N218, SUB5
N218	NDR2	N212, N31
N219	NDR2	N214, SUB5
N220	NDR2	N213, SUB5
N310	NDR3	N35, N36, N27
N311	NDR3	N28, N29, N210
N312	NDR3	N39, PE, N23
ND1	NAND3	CE1, CE2, CE3
ND2	NAND3	CE4, CE5, CE6
ND3	NAND3	FA2QN, FA3QN, FA4QN
ND7	NAND2	FA1QN, FA2QN
ND8	NAND3	FA1Q, FA2Q, FA3Q
ND9	NAND3	ND8, FA4Q, BIN
ND11	NAND3	BIN, FA1Q, FA2Q
ND12	NAND3	FA3Q, FA4Q, UP
ND13	NAND3	N22, UP, FA1Q
ND14	NAND3	FA2QN, FA3QN, FA4Q
ND15	NAND2	P2, PE
ND16	NAND3	G432, N24, N23
ND17	NAND3	N34, N23, FA4QN
ND18	NAND3	UP, FA1QN, G711
ND19	NAND2	ND15, ND16
ND20	NAND3	ND17, N310, ND18
ND21	NAND2	PE, CLK
NET END		
407 SIGNALS ASSEMBLED		
= 04.07 PCT OF FAIRSIM CAPACITY		

Figure 5. FAIRSIM coding of up/down counter.

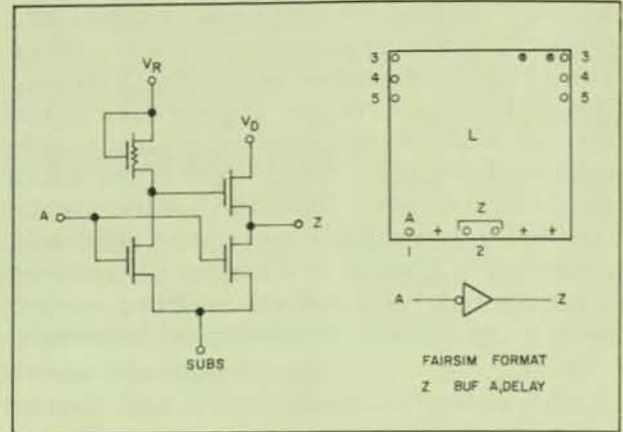
3400 Micromosaic™ Array Cell Set

The library of cells utilized in the computer aided design of custom arrays has been extensively characterized to provide an operating history as a function of temperature, power supply variation and fan-out.

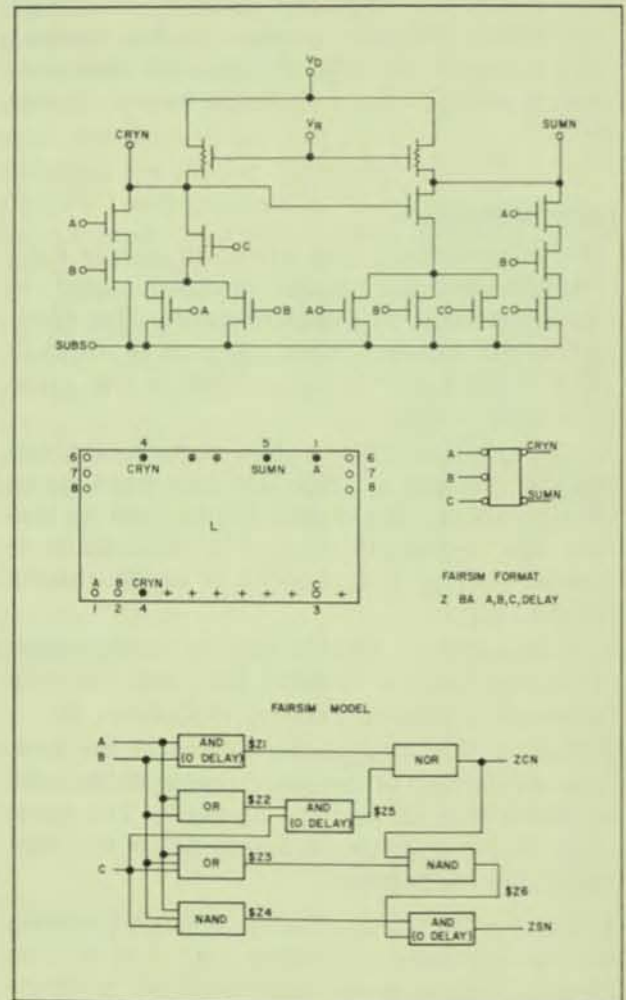
The Micromosaic array has been designed for and characterized over the full military temperature range of -55°C to $+125^{\circ}\text{C}$. These custom arrays are also available in an industrial range of 0°C to $+70^{\circ}\text{C}$. MOS circuitry performance depends strongly upon the operating temperature of the chip. In general, speed and power dissipation are inversely proportional to temperature, and directly proportional to the power supply voltages. At -55°C , power dissipation is approximately 1.4 times the room temperature value and propagation delays are approximately 0.7 of the room temperature value. Conversely, at $+125^{\circ}\text{C}$, power dissipation is approximately 0.7 and propagation delays are 1.4 times the room temperature value.



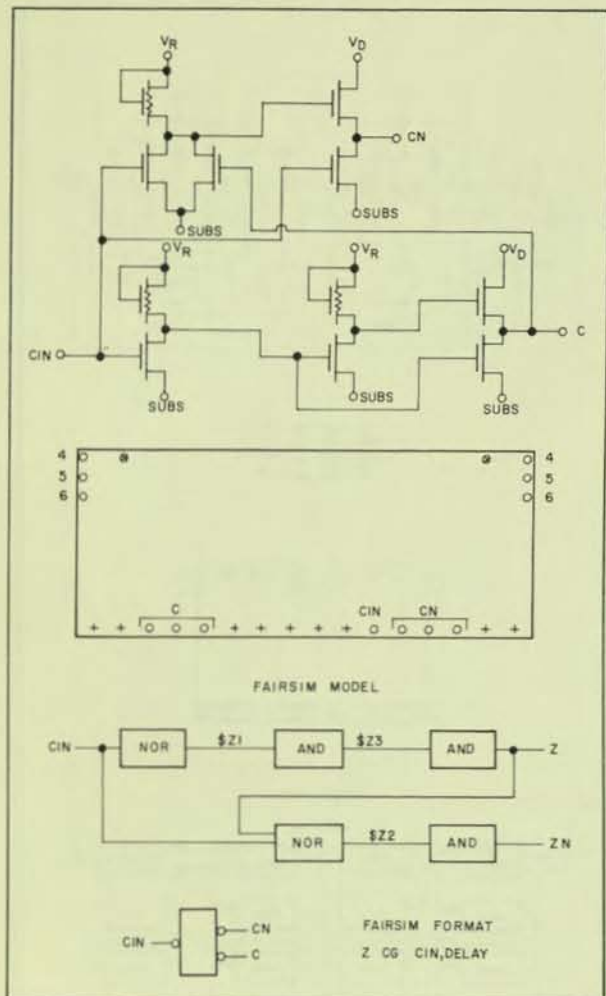
BBUF: This cell is similar in concept to BUF, but impedances are lower for increased capacitive drive capability.



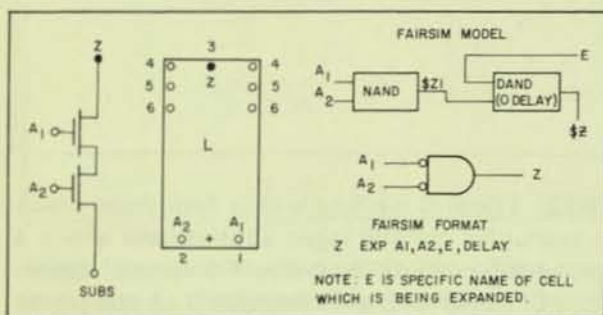
BUF: This "totem-pole" output buffer is utilized for driving off-chip capacitive loads. Logically, it operates as an inverter.



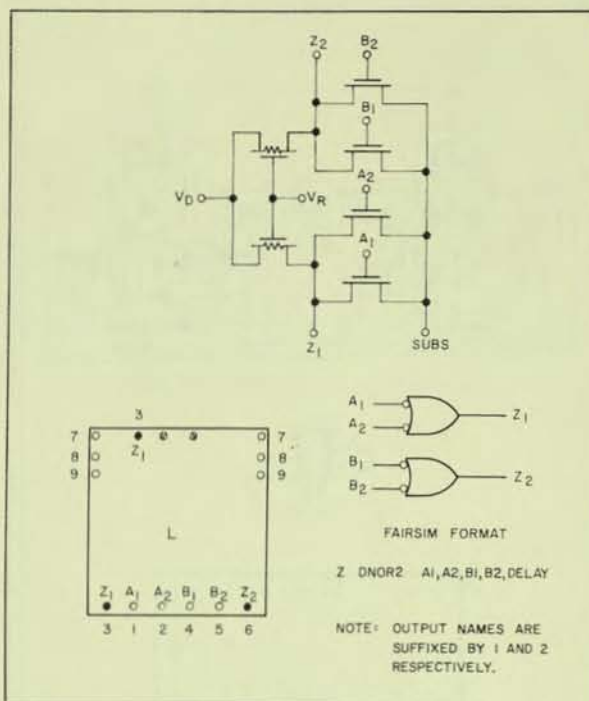
BA: This binary adder cell accepts inputs A, B and C and generates active level high SUM and CARRY (ZSN and ZCN) outputs.



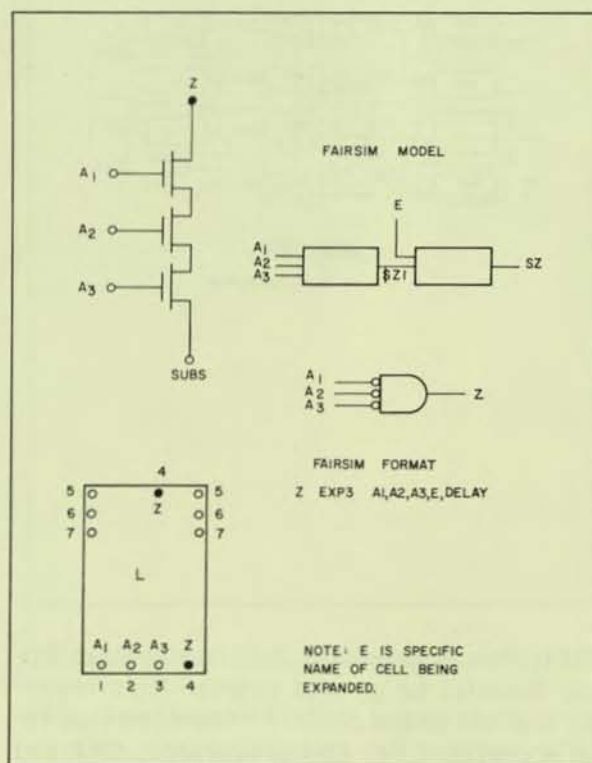
CG: The clock generator cell is utilized to convert single-phase clocks to non-overlapping two-phase clocks. Buffer outputs provide good on-chip capacitive drive capability. Where speeds or fan-outs are low, this same function may be achieved more economically with standard gates.



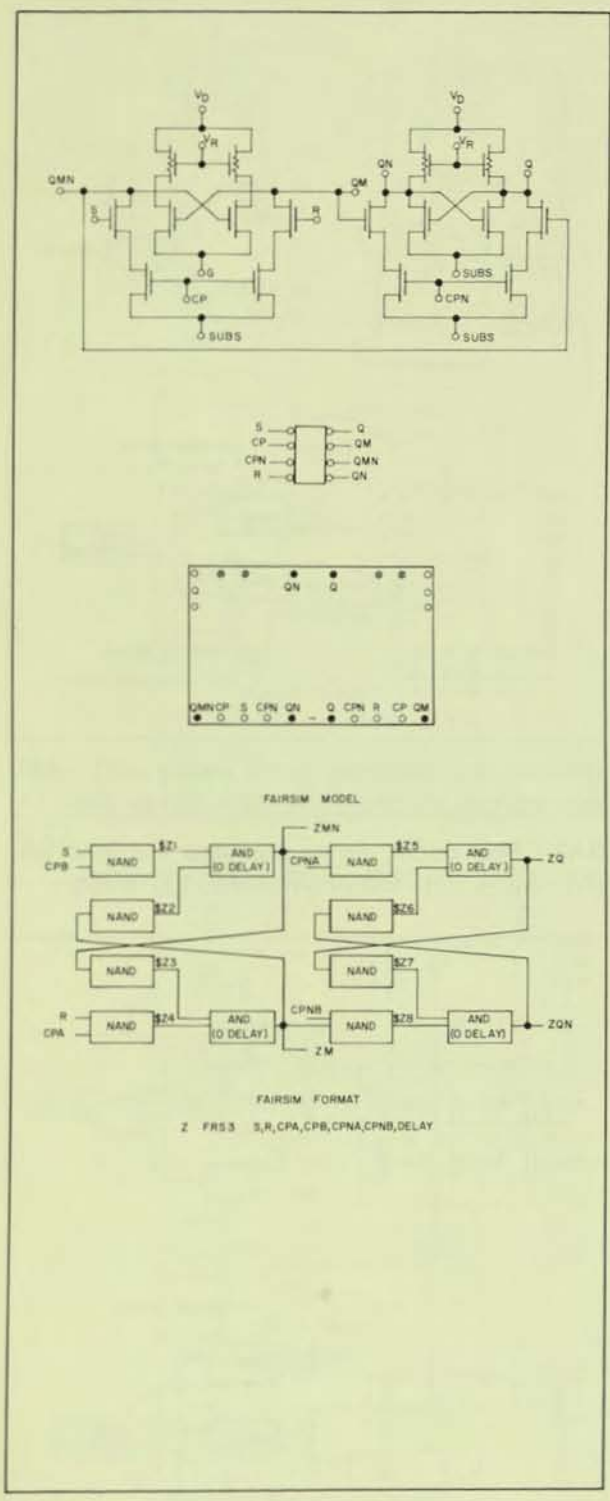
EXP: The expander provides two series transistors for the purpose of expanding the logic capability of other cells.



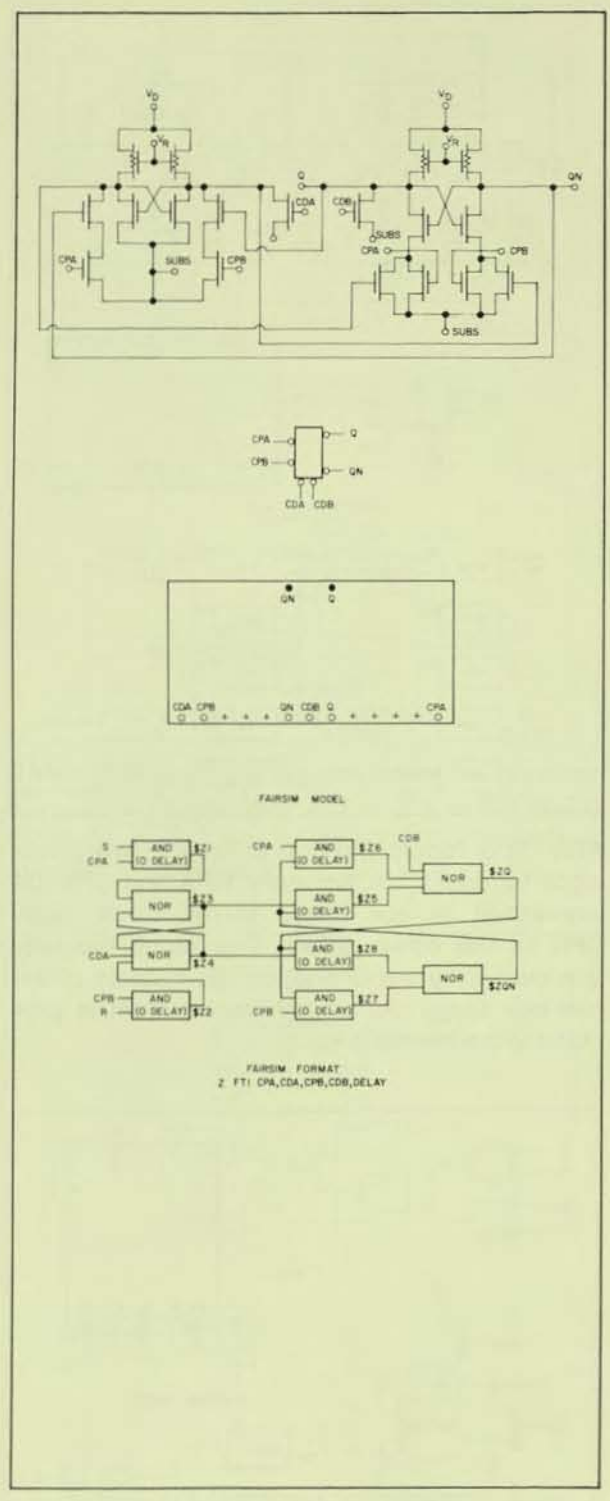
DNOR2: This cell provides two independent two-input NOR gates.



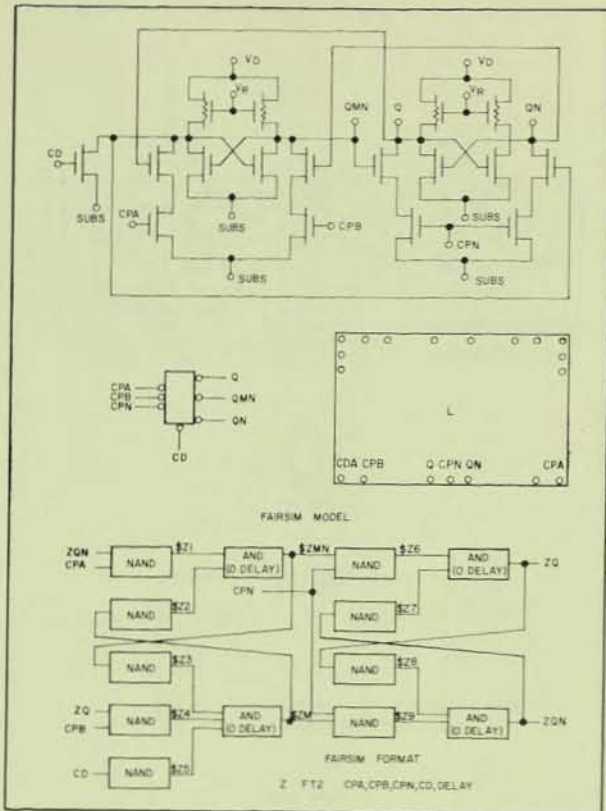
EXP3: This expander provides three series transistors for the purpose of expanding the logic capability of other cells.



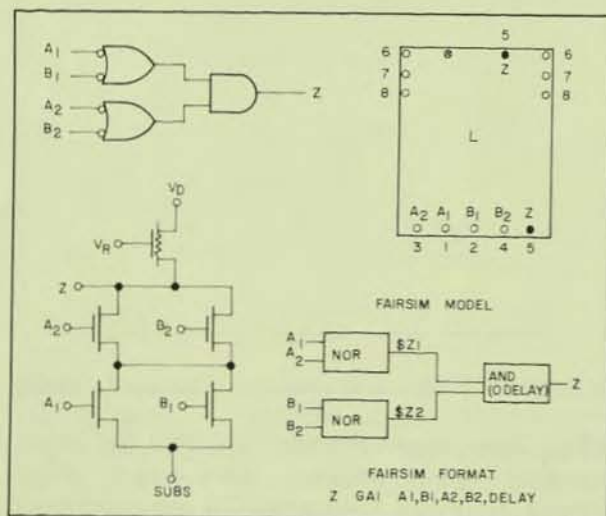
FRS3: This R-S flip-flop with a two-phase clock is similar to FRS2 with the exception that no direct clear is provided. Normally, CPA and CPB are commoned to one phase of the clock input, and CPNA and CPNB are commoned to the other phase.



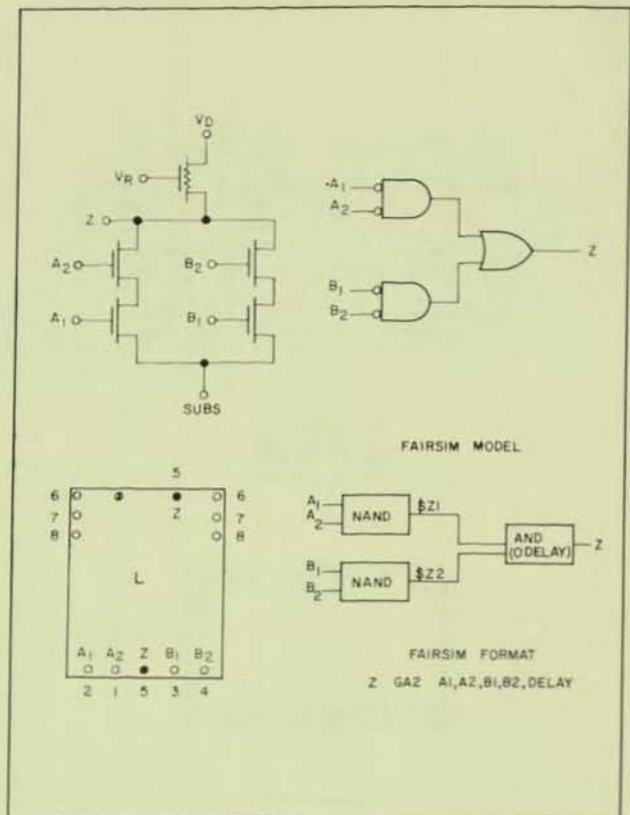
FT1: This toggle flip-flop is useful for implementing ripple counters with single phase clocks. Normally, CPA and CPB are commoned to the clock input; the flip-flop will toggle on the positive-going clock transition. CDA and CDB are commoned as the asynchronous reset.



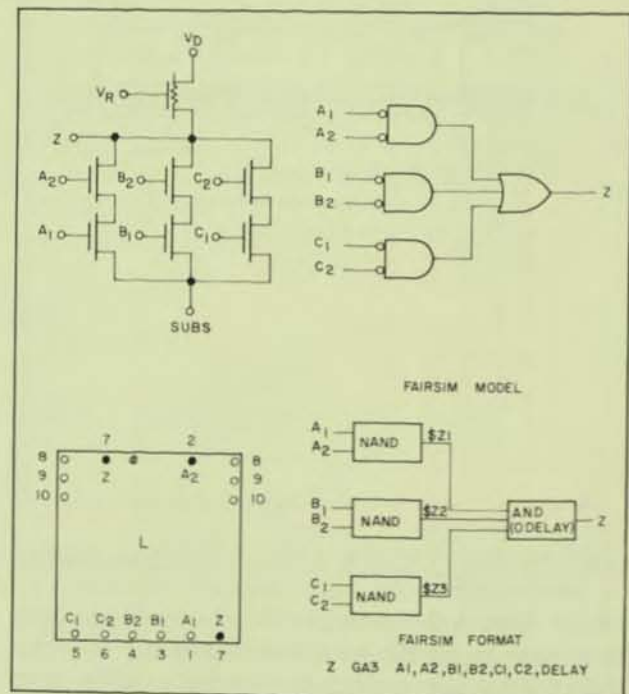
FT2: This toggle flip-flop utilizes a two-phase clock for operation. Normally, CPA and CPB are commoned to one phase of the clock input, CPN to the other phase. This clock typically is provided by the Q and the QN outputs of the previous stage. An asynchronous reset is provided to the master only.



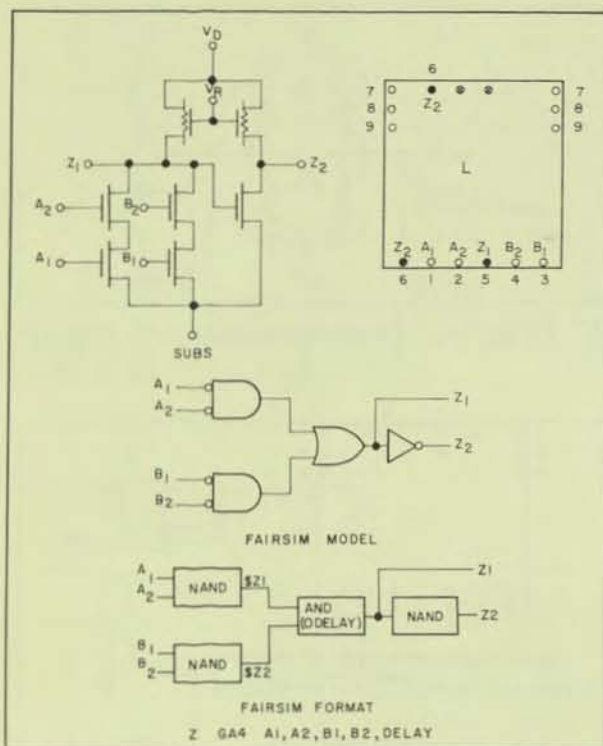
GA1: This gating array provides the function: $(A1 + B1) \cdot (A2 + B2)$ or $\overline{A1} \overline{B1} + \overline{A2} \overline{B2}$



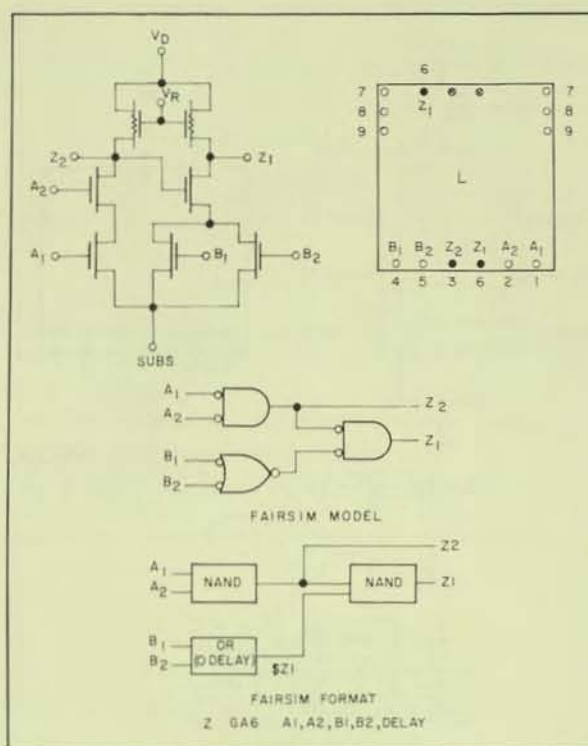
GA2: This gating array provides the function: $(A1 \cdot A2) + (B1 \cdot B2)$ or $(\overline{A1} + \overline{A2})(\overline{B1} + \overline{B2})$



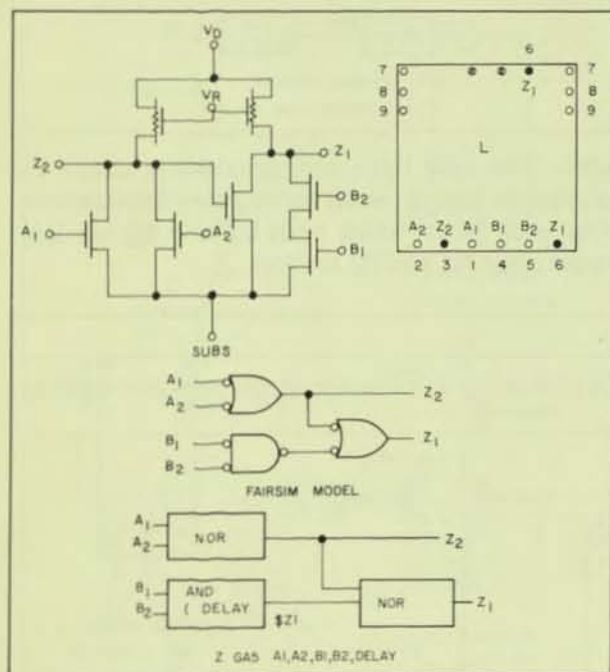
GA3: This gating array provides the function: $(A1 \cdot A2) + (B1 \cdot B2) + (C1 \cdot C2)$



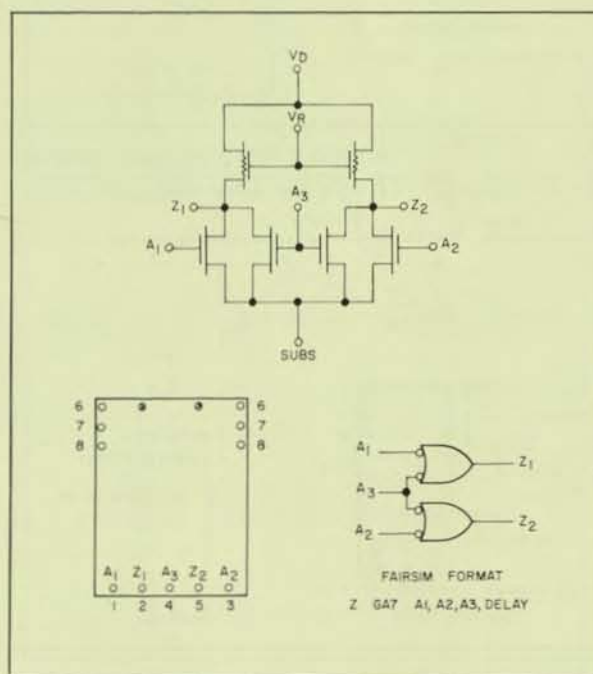
GA4: This gating array provides the function $(A1 \cdot A2) + (B1 \cdot B2)$ at Z2 and its complement at Z1.



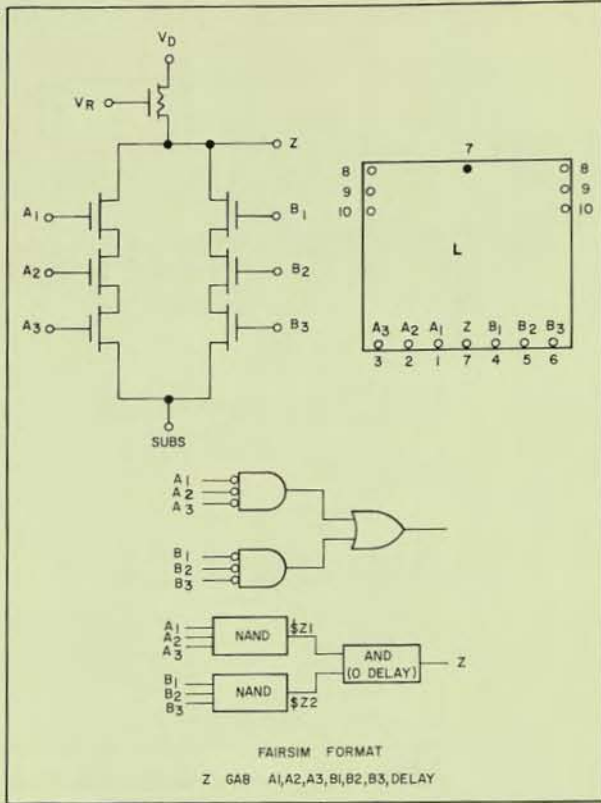
GA6: This gating array provides the function $A1 \cdot A2$ at Z2 and $(A1 \cdot A2) + \overline{(B1 + B2)}$ at Z1. When $A1 = B1$, and $A2 = B2$, the comparison function is generated.



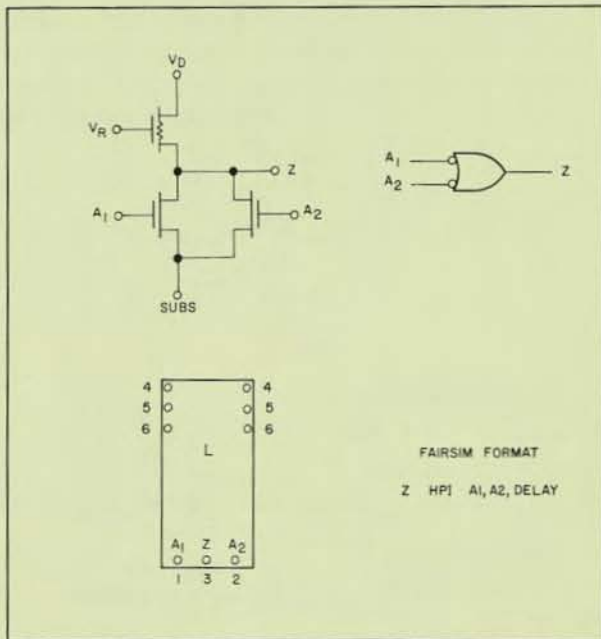
GA5: This gating array provides the function $A1 + A2$ at Z2 and $(A1 + A2) \overline{(B1 \cdot B2)}$ at Z1. When $A1 = B1$ and $A2 = B2$, the EXCLUSIVE-OR function is generated.



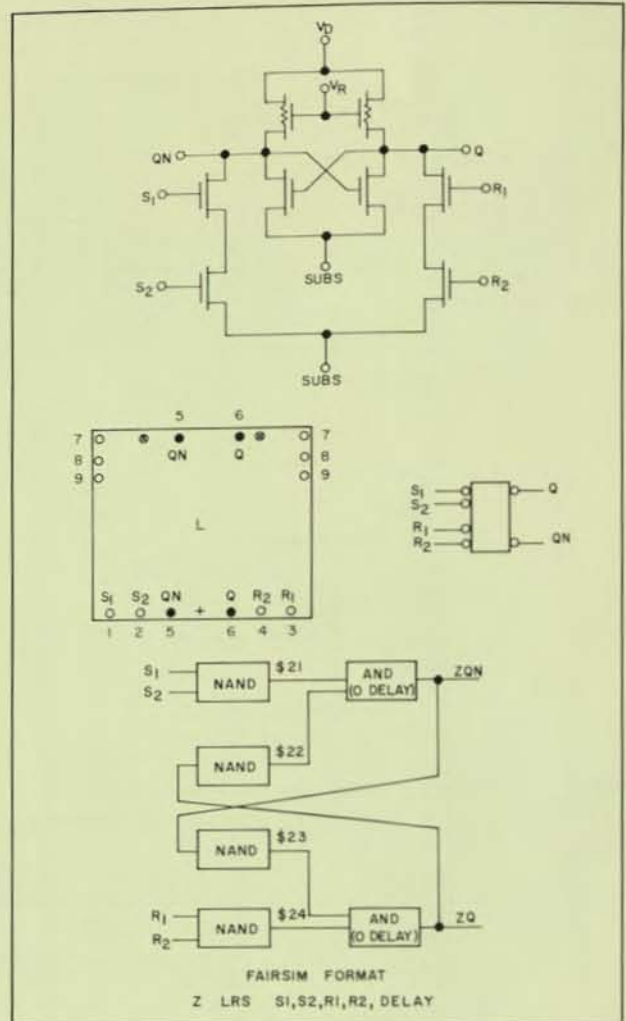
GA7: This gating array provides two, two-input NOR gates having a common input.



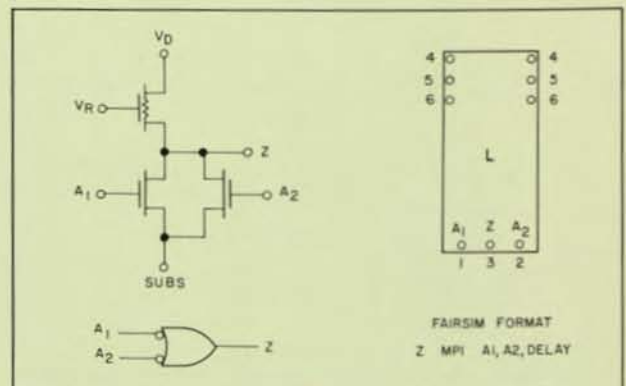
GA8: This gating array provides the function:
 $A1 \cdot A2 \cdot A3 + B1 \cdot B2 \cdot B3$



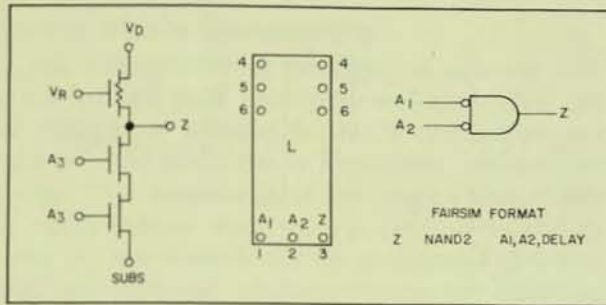
HPI: This driver element, logically a two-input NOR, provides lower impedance devices for improved capacitive drive capability.



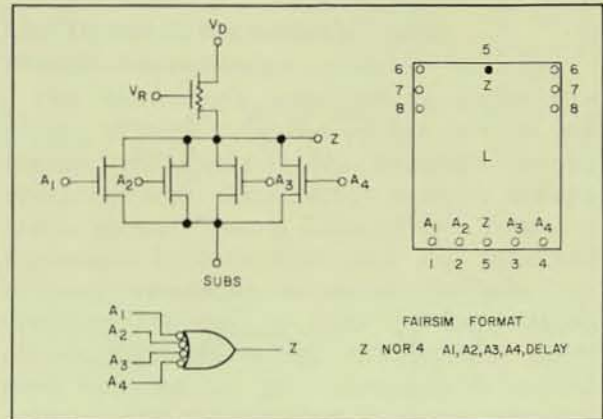
LRS: The LRS latch cell provides a single bit of storage and is useful for register applications. The latch is set when both S1 and S2 are low; reset when R1 and R2 are low.



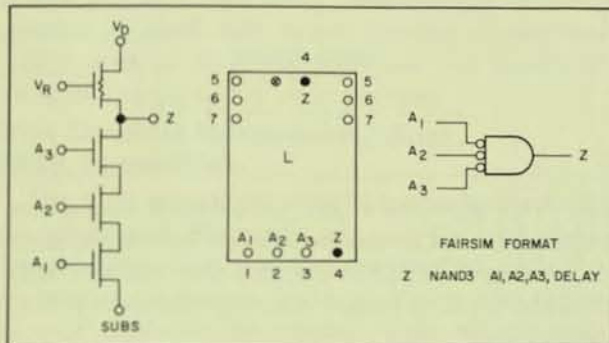
MPI: This driver element, logically a two-input NOR, provides lower impedance devices for improved capacitive drive capability.



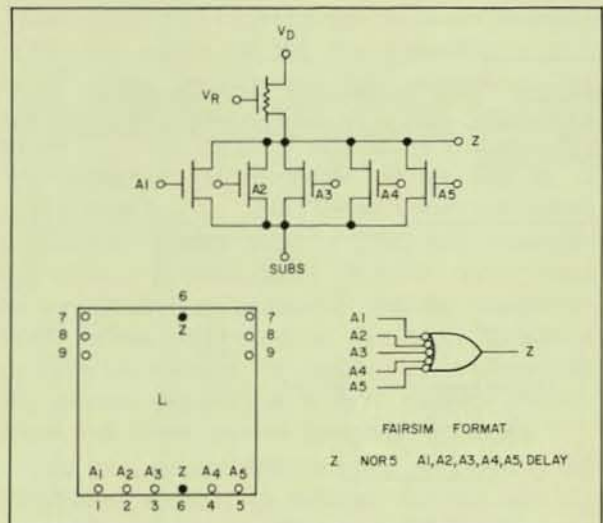
NAND2: This gate provides the function $\overline{A1 \cdot A2}$ or $\overline{A1} + \overline{A2}$



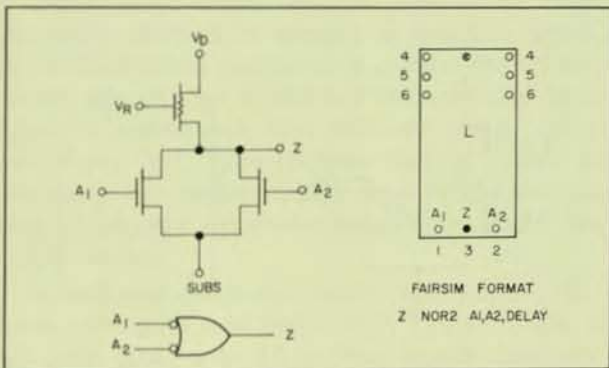
NOR4: Provides the function $\overline{A1 + A2 + A3 + A4}$ or $\overline{A1} \cdot \overline{A2} \cdot \overline{A3} \cdot \overline{A4}$



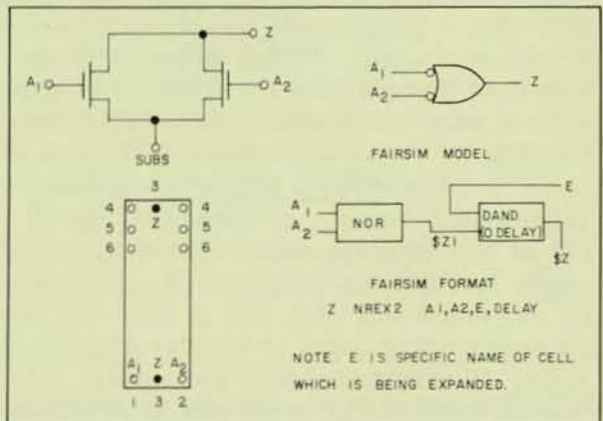
NAND3: This gate provides the function $\overline{A1 \cdot A2 \cdot A3}$ or $\overline{A1} + \overline{A2} + \overline{A3}$



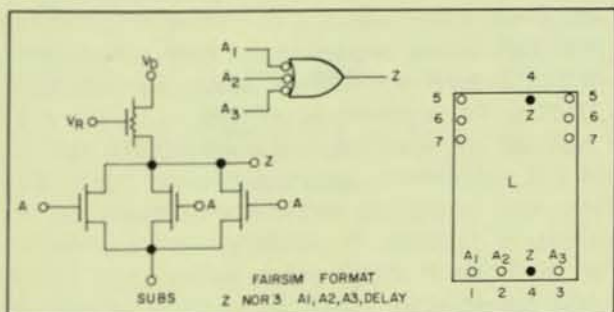
NOR5: Provides the function $\overline{A1 + A2 + A3 + A4 + A5}$ or $\overline{A1} \cdot \overline{A2} \cdot \overline{A3} \cdot \overline{A4} \cdot \overline{A5}$



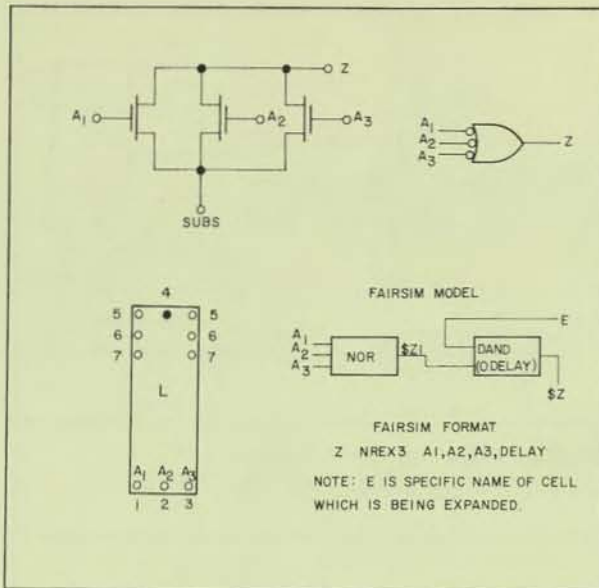
NOR2: Provides the function $\overline{A1 + A2}$ or $\overline{A1} \cdot \overline{A2}$



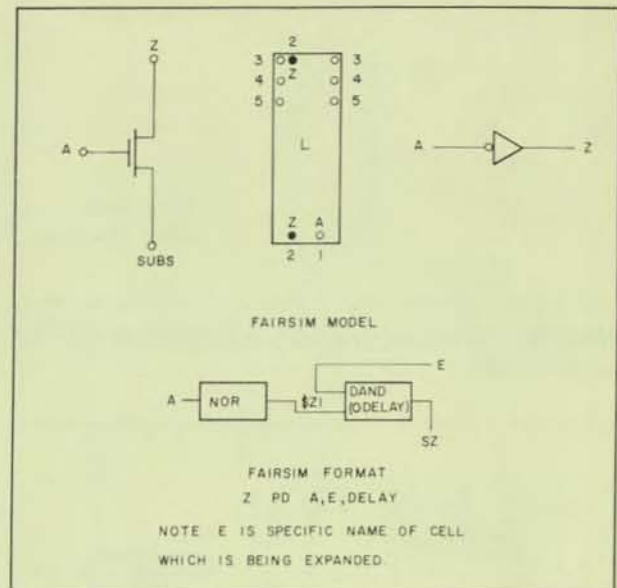
NREX2: This two-input NOR expander provides two parallel transistors for expansion of other cells.



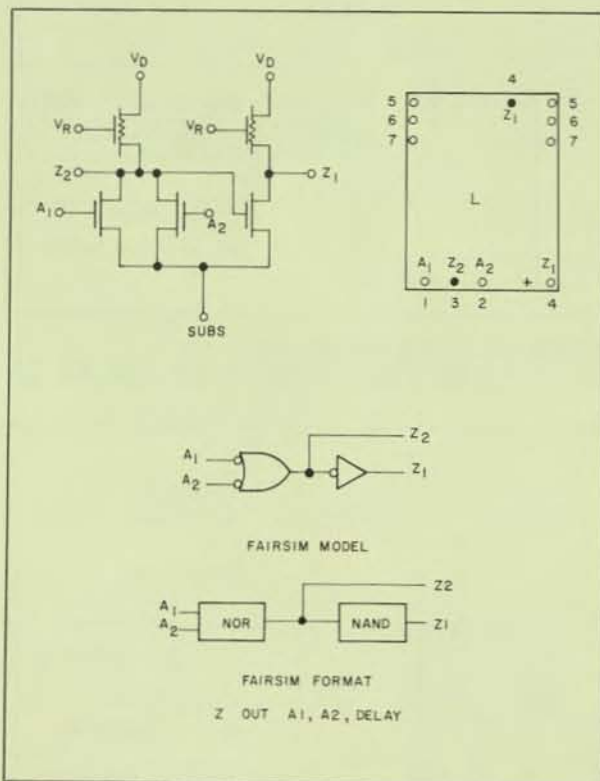
NOR3: Provides the function $\overline{A1 + A2 + A3}$ or $\overline{A1} \cdot \overline{A2} \cdot \overline{A3}$



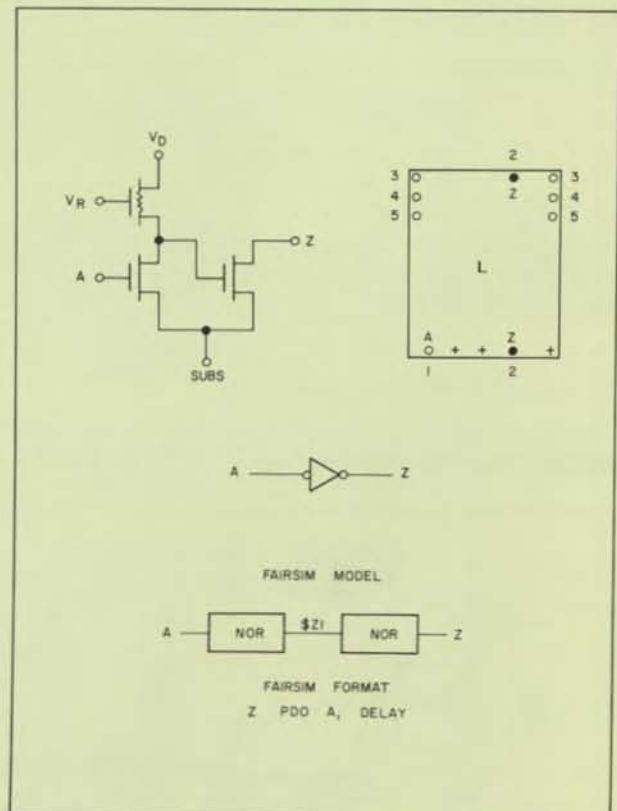
NREX3: This three-input NOR expander provides three parallel transistors for expansion of other cells.



PD: The pull-down cell provides a single low impedance MOS device useful for output buss connections. In addition, the PD element may be used on-chip to pull down a maximum of four gates.



OUT: The output driver, logically equivalent to a NOR2 driving a low impedance inverter, is used where high capacitive drive is required. The output characteristics are similar to those of the HPI.



PDO: This pull-down cell provides an input inverter input to a PD element.

MOS or Bipolar Compatibility

The 3400 cell set is designed to operate with either of two sets of supply voltages. One set of voltages is utilized for MOS compatible arrays and the other set is for bipolar compatible arrays. The magnitude of the device thresholds is optimized for each set of conditions and is fixed by the manufacturing process. The nominal performance characteristics for each of the two sets of operating conditions are outlined below. This brochure describes a general purpose custom capability rather than complete worst-case and best-case performance characteristics of each cell. More detailed characterization data on both the high and low threshold cell sets are available upon request.

High Threshold Micromosaic™ Array (MOS Compatible)

The high threshold circuits have device turn-on voltages in the range of -2.9 to -4.2 volts. The circuits have been characterized with the resistor gate supply voltage, V_R , in the range of $-28 \pm 4V$ and the resistor drain supply voltage, V_{DD} in the range of $-10 \pm 2V$. Assuming nominal voltages (-28 and -10 volts), the typical MOS load resistor impedance is $75k\Omega$ at room temperature, and the impedance of on switching devices to ground is typically $6.5k\Omega$. Worst-case noise immunity is greater than 1 volt under any of the operating voltage and temperature conditions, and nominal power dissipation per "on" gate (output low) is $1.2mW$. In addition, each output buffer required by the design dissipates approximately $8mW$ when the output is low.

To quickly estimate power dissipation, assume 50% gate and buffer duty cycles. Thus, a 150 gate array with 10 buffers would dissipate $130mW$ under nominal conditions.

On-chip propagation delays, and therefore the operating frequency of a custom subsystem, depend on the load capacitances associated with each internal node. Under the typical conditions of $V_R = -28V$, $V_{DD} = -10V$, and $T = 25^\circ C$, average propagation delays are 50 ns/pF "on" chip. Each fan-out typically contributes 0.3 to 0.5 pF, depending on the transistor type and interconnection variables. In general, a useful typical propagation delay figure is about 70 ns per internal logic level. Thus, for a design with a maximum of seven levels of logic, the maximum room temperature operating frequency would be in the neighborhood of 2 MHz.

Low Threshold Micromosaic™ Array (Bipolar Compatible)

The Micromosaic array cell topologies employed in high threshold voltage circuits are equally well suited to low threshold circuits operating with significantly reduced voltage levels. In fact, several designs have been implemented in both high and low threshold technologies utilizing the same mask sets. The low threshold devices have turn-on voltages of $-1.7V$ to $-2.3V$ and are typically operated with the V_{DD} pin connected to ground potential and the substrate (V_{SS}) operated at a positive potential between $+4.5V$ and $+6V$. This provides input and output logic levels of ground and approximately $0.75V$ below the V_{SS} supply. The resistor gate bias voltage, V_R , is set between $-7V$ and $-20V$, for the low threshold arrays, which gives an effective bias relative to the substrate of from $-11.5V$ to $-26V$, depending upon V_{SS} . The nominal operating voltages for low threshold Micromosaic arrays are $V_R = -15V$ and $V_{SS} = +5V$. These conditions yield a nominal resistor value of $90k\Omega$ and a switching device on impedance of $15k\Omega$. Worst-case noise immunity is somewhat less for low threshold arrays compared to the high threshold circuits because of the reduced ratio of switching device impedance to load resistor impedance and lower device threshold voltages.

The low voltage Micromosaic arrays may be interfaced directly to bipolar current sinking logic if proper precautions are taken. The Micromosaic inputs require a V_{IL} of $\leq 400mV$, and a V_{IH} of $\geq (V_{SS} - 100mV)$. This may be obtained by the use of a $DT_{\mu L}$ or $LPDT_{\mu L}$ resistive pull-up gate driving Micromosaic inputs only. The Micromosaic outputs may drive bipolar circuitry by utilizing a BUF element to drive a single $LPDT_{\mu L}$ load. Other techniques to drive $DT_{\mu L}$ or $TT_{\mu L}$ loads directly may be practical depending on specific conditions.

Power dissipation is reduced considerably for low threshold arrays primarily due to the reduced logic voltage swing. Nominal power per "on" gate is 0.23 mW. This figure can be significantly reduced by reducing the magnitude of the resistor bias supply. Output buffer power dissipation is also lower for low threshold circuits (due to the lower V_R bias) and is typically $4mW$ per "on" buffer.

On-chip propagation delays for the nominal voltages suggested above are approximately

the same as those measured for the high threshold circuits. The typical delay is 70 ns/pF, and for typical fan-outs, a propagation delay of 110 ns per logic level is useful for speed estimates.

Finally, the temperature dependence of low threshold Micromosaic™ arrays is similar to that of the high threshold circuits. The effect of threshold changes with temperature, which tends to offset changes in device impedance, is more significant for low threshold circuits; however, the speed and power variations with temperature are slightly reduced from the figures reported above for the higher threshold system.

Applications

The 3410/11 Four-Bit Up/Down Counter is a typical Micromosaic array application. The logic diagram is shown in Figure 6. This counter provides the capability for counting in BCD or binary, controlled by the BIN input, and up or down as controlled by the UP input. A six input Count Enable input allows up to seven 3410/11 counters to be connected as a 28-bit synchronous up/down counter. A decoded terminal count and synchronous parallel entry are also provided. The connection as a 16-bit counter is shown in Figure 7.

The Fairchild CAD system was utilized to design the 3410/11; the FAIRSIM computer description for the 3410/11 is shown in Figure 5. The signal names were arbitrarily selected. This description was used by the Computer Aided Design system to perform cell placement and interconnection routing. The computer-generated layout description is shown in Figure 8. A photomicrograph of the completed chip is shown in Figure 9.

Packaging

Micromosaic arrays are available in a variety of packages. Package selection is determined by the number of pins, thermal transfer, and form factor. Standard Fairchild packages presently consist of 16, 24, 36 Dual-In-Line and ribbon (Flatpack) types. In addition, multi-chip packages will be available for logic requirements exceeding the economic capability of a single Micromosaic array chip, or designs requiring special interface requirements. Fifty and 64 pin packages are being developed to accommodate arrays requiring more than 36 connections.

Testing

The number and types of tests performed on a Micromosaic array depend on logic design, required confidence level, and eventual environment. Potential failure modes must be analyzed to determine the proper tests. Worst-case DC measurements will be required for inputs and outputs to assure that interfaces with other devices achieve the desired margins. The number of such tests is proportional to the number of pins, and in general will be small in comparison to functional tests. Functional tests will verify the transfer function, truth table, or state diagram of the device and will check internal devices.

Functional tests may be conveniently classified into two groups: performance and acceptance tests. Basically, a performance test validates the basic design of the array. It consists of applying a representative sampling of input sequences which verify that operation is as expected. It is the type of a test that would be written for the FAIRSIM program to verify a design. On the other hand, acceptance tests

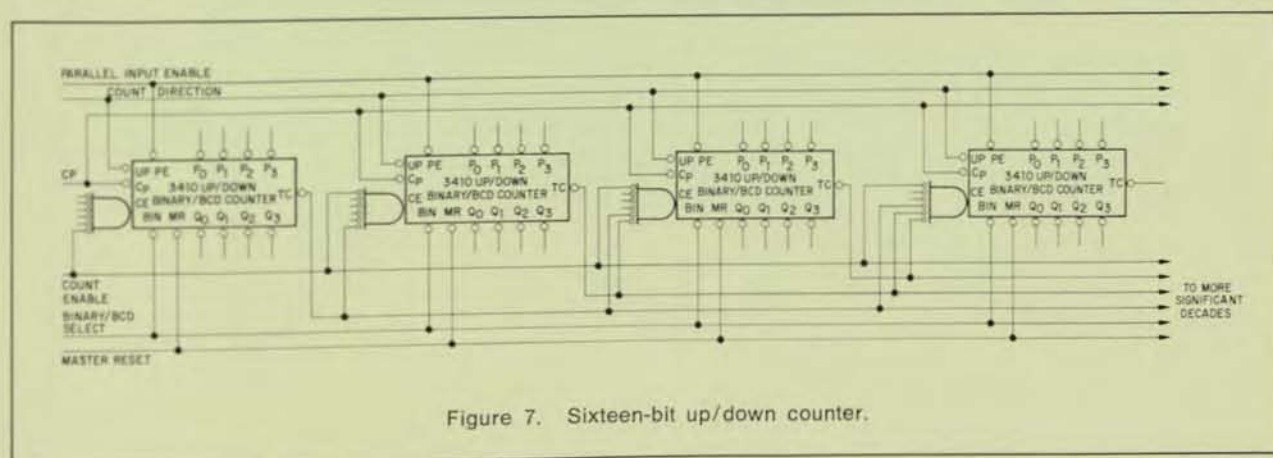


Figure 7. Sixteen-bit up/down counter.

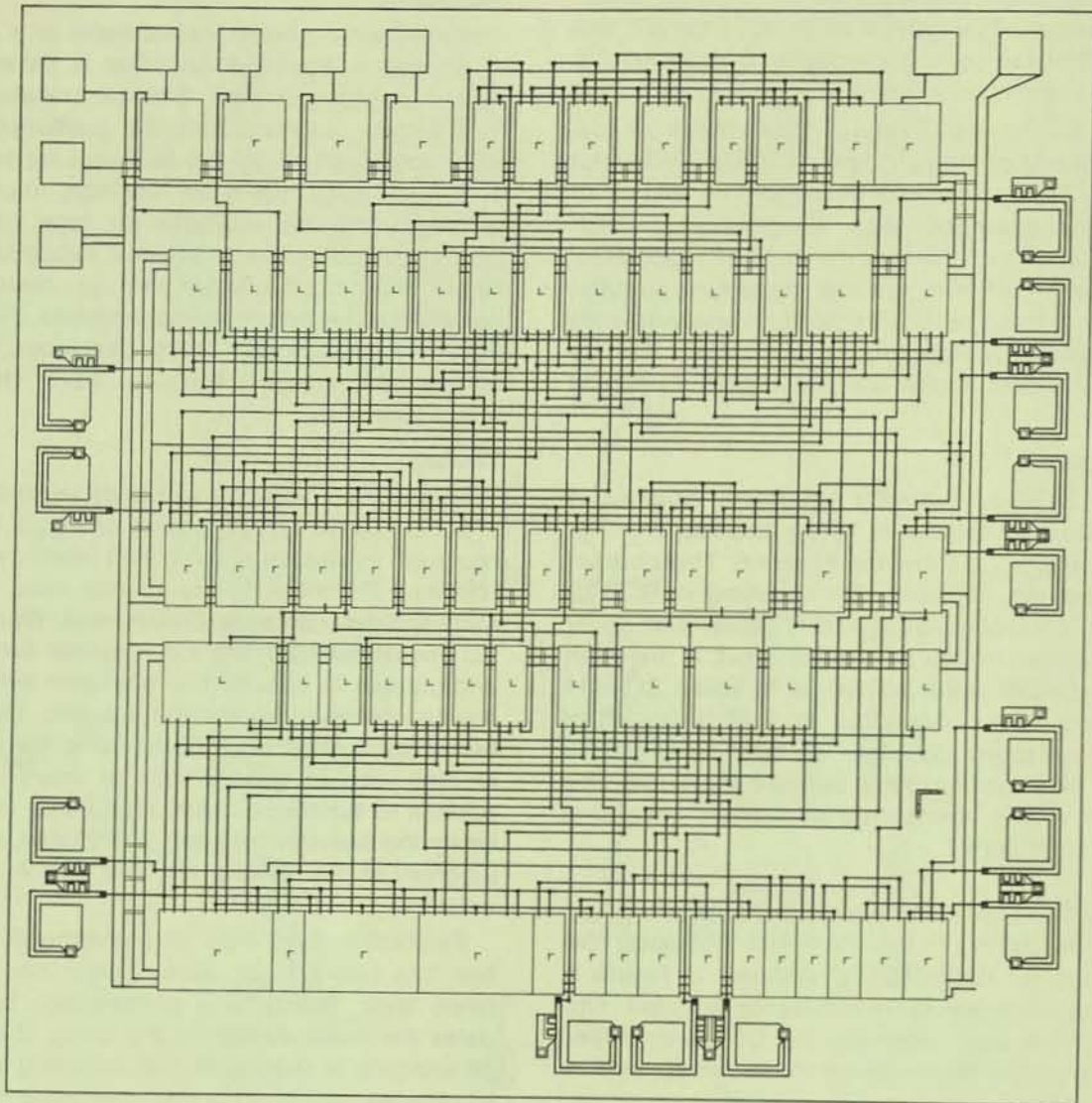


Figure 8. Computer generated interconnection layout for 3410 Four-Bit Counter.

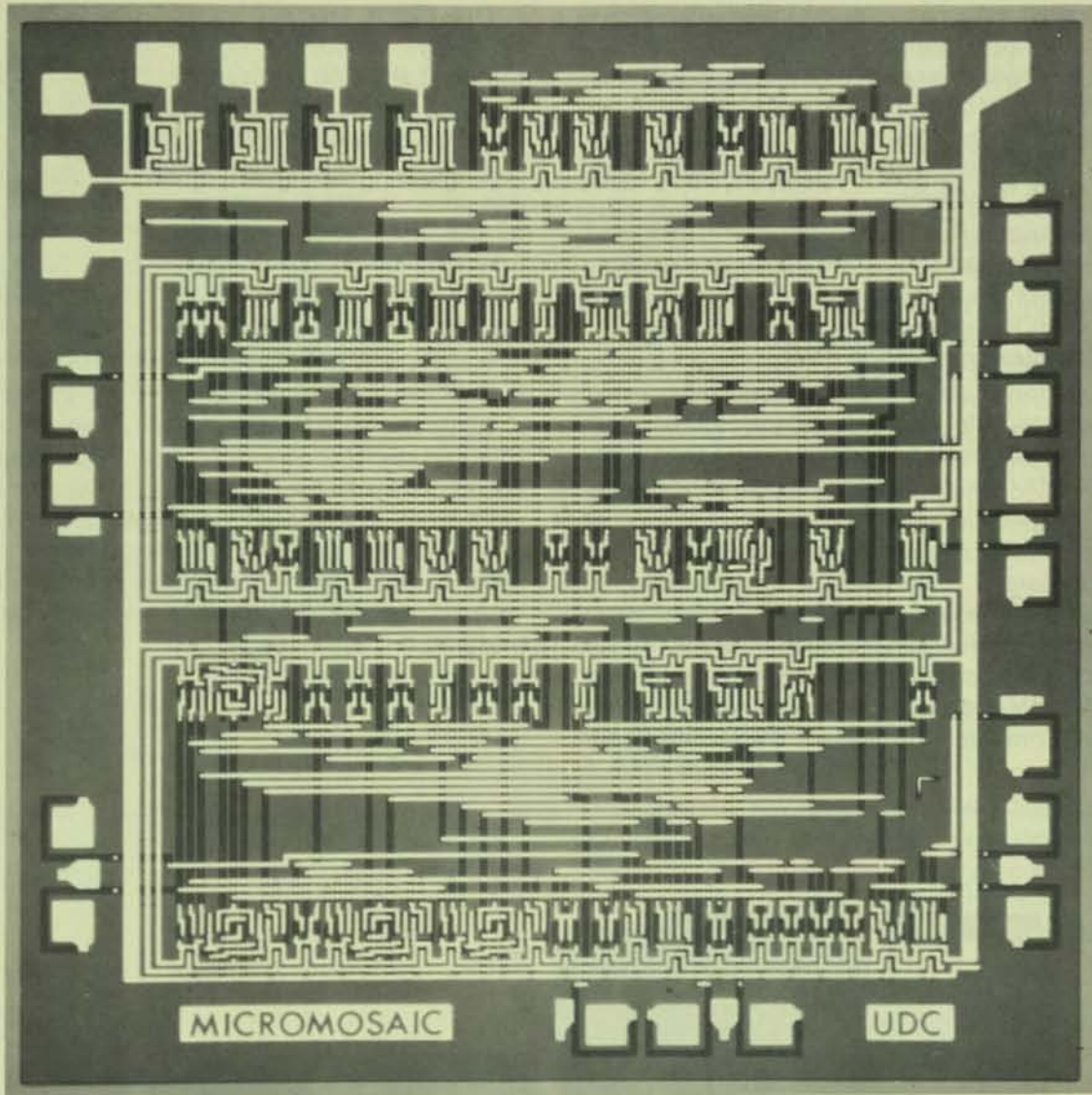


Figure 9. 3410 Four-Bit Counter photomicrograph.

must verify the complete operation of the device before it is shipped. These tests are inherently longer than performance tests and yet, because they (or some portion of them) must be applied to every array manufactured, they must be reasonably short. The program performs three functions:

1. It analyzes the FAIRSIM performance test and generates a list of untested array elements. At this point, more tests may be written in FAIRSIM format to test the array more completely, or automatic test generation selected.
2. It performs automatic test generation using sophisticated algorithms to select optimum test sequences. These additional tests are then combined with the performance tests to form the final functional acceptance test.
3. It provides automatic formatting of test sequences to the appropriate tester format.

Functional testing is presently being done using Fairchild Instrumentation 8000A Array Testers. Tests can be either hand-generated in the FAIRSIM language, or automatically generated and machine-formatted in the 8000A input format.

The 8000A will perform DC function testing on arrays containing up to 50 pins. A photograph of the unit is shown in Figure 10. Basically, the tester stores in memory a sequence of forcing functions and expected output responses plus control words which identify package pins as input, output, or "don't care" terminals. The tester sequentially applies logic levels representing forcing functions to the array inputs and compares actual array outputs to the predicted responses on a go/no-go basis.

A complete description of the 8000A is available in the publication *8000A Array Test System*.

While the 8000A performs only limited parameter testing, the new Fairchild Instrumentation 8000B Array Tester, currently in advanced development, combines the functional capability of the 8000A with the parameter testing of a 5000. In the interim, parameter tests are being performed on the Fairchild Instrumentation 5000 Integrated Circuit Tester.



Figure 10. Digital array test system.

Summary

These customer benefits are associated with the use of 3400 Micromosaic™ Arrays:

1. Fast design turnaround time and low non-recurring design costs — This results from the speed and accuracy of a totally integrated Computer Aided Design system. By utilizing pre-designed and characterized cells, engineering "redesigns" are drastically reduced.
2. Low cost/gate function — The production cost of an LSI circuit is a function of chip fabrication, packaging and testing costs. In addition to the very accurate computer-controlled maskmaking of the 3400, which contributes to its excellent yield, the advanced semiconductor technology and concise allocation of interconnections based on actual requirements make 3400 Micromosaic Array chip sizes competitive with conventional "hand-crafted" custom arrays. Packaging and testing of custom arrays (which can be the principle expense) are the same for "hand-crafted" and Micromosaic arrays. This results in economical production of Micromosaic arrays from a few hundred to hundreds of thousands of parts.
3. Parameter flexibility — With the cell design of Micromosaic arrays, high voltage (MOS compatible) and low voltage (bipolar compatible) arrays can be generated from the same mask set. In addition, the extensive characterization available allows reliable operation over large ranges of power supply variation. Performance over the industrial temperature range (0° to +70°C) or the full military range (-55°C to +125°C) is fully specified.
4. Delineation of responsibility — Finally, a prime customer benefit of the Micromosaic array concept is the flexible, but well-defined delineation of responsibility. All too often, misunderstanding of specifications or customer generated artwork have resulted in unusable arrays and a question of which party was responsible for the error. With Micromosaic arrays, the customer has final responsibility to approve operation of the design, as simulated on the CAD system, before artwork is started. Changes at this stage are easy and the need for functional breadboarding is eliminated. After customer approval, arrays are produced and tested by Fairchild using the customer approved test sequences.

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Technical Specification

To expedite the quotation of a custom Micro-mosaic array, the Technical Specification sheet that follows may be completed and submitted

to your local Fairchild sales engineer along with a logic specification or logic diagram. This will allow the array systems engineers to consider all aspects of your requirements.

CUSTOM MICROMOSAIC™ ARRAYS TECHNICAL SPECIFICATION

Customer: _____

Device: _____ Date Prepared: _____

Technical Interface Desired:

Performance Specification FAIRSIM Coded Logic and Tests
General Logic Diagram Micromosaic Cell Logic Diagram
Above with Functional Test Specification Above with Functional Test Specification

Package Type: _____ Pins Used: _____

Voltage Supplies: V_{DD} _____ $V_R = V_{GG}$ _____ V_{SS} _____ Substrate _____

Temperature Ranges: Operating _____ Storage _____

Noise Immunity:

Min. "Low" Level Noise Immunity on Chip _____ Min. "High" Level Noise Immunity on Chip _____

Thermal Characteristics:

Maximum Operation Junction Temperature _____ °C

Junction to Case _____ °C/W

Junction to Ambient _____ °C/W

Desired Development Time:

Simulation Finished (ARO) _____ Weeks, Parts Delivered After Approval of Simulation _____ Weeks

Available Power Dissipation:

Nominal: _____ Worst Case: _____

$V_{GG} =$ _____ Volts $V_{SS} =$ _____ Volts $V_{GG} =$ _____ Volts $V_{SS} =$ _____ Volts

$V_{DD} =$ _____ Volts $T =$ _____ Volts $V_{DD} =$ _____ Volts $T =$ _____ Volts

Speed Requirement — Choose Most Applicable Specification:

Worst-Case Propagation Delay _____ Minimum Input Pulse Width _____

Clocks:

Maximum Input Frequency _____ Duration of CP (Min.) _____

Phases Externally Generated _____ Duration of CPN (Min.) _____

Phase(s) Internally Generated _____ Clock Transition Time _____

Amplitude of External Clock: Min. _____ Max. _____

Inputs:

Logic Swing: "LOW" Level _____ "HIGH" Level _____

Input Impedance _____

All inputs have non-destructive internal protection against over voltage to prevent rupture or gate oxides.

Outputs:

Impedance to Substrate: Nominal _____ Maximum _____

Impedance to V_{DD} : Nominal _____ Maximum _____

Load _____ Voltage Swing _____

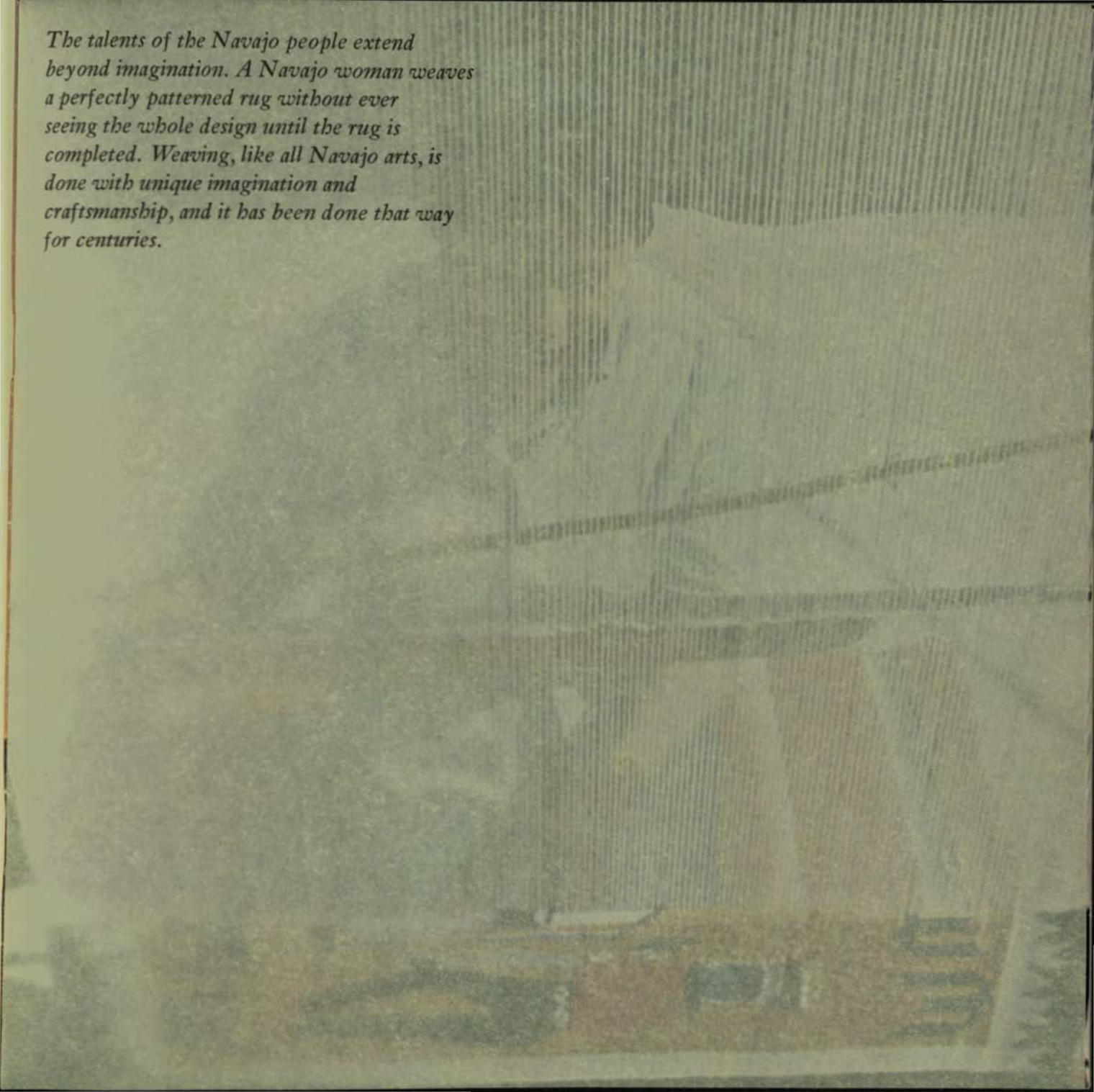
Gene Hodley
650-327-4224





*Thank you for helping us celebrate the
dedication of Fairchild Semiconductor's
new Shiprock facility—
a partnership in progress.
September 6, 1969
Shiprock, New Mexico*

The talents of the Navajo people extend beyond imagination. A Navajo woman weaves a perfectly patterned rug without ever seeing the whole design until the rug is completed. Weaving, like all Navajo arts, is done with unique imagination and craftsmanship, and it has been done that way for centuries.





Building electronic devices, transistors and integrated circuits, also requires this same personal commitment to perfection. And so, it was very natural that when Fairchild Semiconductor needed to expand its operations, its managers looked at an area of highly skilled people living in and around Shiprock, New Mexico, a city of 8000 located in the northeast corner of the vast Navajo lands.

That was in 1965. Since then, Fairchild's Shiprock manufacturing and training operation has served as the keystone of a planned industrial development complex conceived by the Navajo Tribal Council as part of its effort to shift the economic base of the tribe from one purely agricultural to a more diversified mix of business and industry. From 50 initial employees, Fairchild's Shiprock facility has grown to almost 1200 men and women, making Fairchild the nation's largest non-government employer of American Indians. All but 24 of the 1200 are Navajo; in fact, of 33 production supervisors, 30 are Navajo.



As Shiprock grew to become a critical link in Fairchild's world-wide network of manufacturing operations, it became quite evident that more space would be needed to house this fast-growing operation. Under the direction of the Navajo Tribal Council, a 33,600 square foot modern manufacturing facility has just been constructed in Shiprock, and in early August Fairchild moved into this brand new one-level structure. Housing the most advanced semiconductor electronic assembly equipment in the world, this brightly decorated, fully air-conditioned building also features an employee cafeteria and a parking area for added convenience. And, there is ample room for further expansion of the operation.





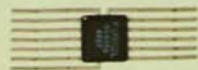
FAIRCHILD

SEMICONDUCTOR

The blending of innate Navajo skill and Semiconductor's precision assembly techniques has made the Shiprock plant one of Fairchild's best facilities—not just in terms of production but in quality as well.

Quality becomes a necessity in the semiconductor business. Fairchild's transistors and integrated circuits, some of which before packaging are no larger than the head of a pin, must perform to perfection in complex computers, electronic appliances, radios and televisions, and on the way to the moon as part of Apollo's communications, guidance, and gyro systems or in instrumentation units located in various stages of the Saturn rocket.

Back on earth, the success of the Shiprock facility can easily be measured in terms of growth and expansion. However, the real value of this progress lies in the creation of meaningful jobs for those who have not had jobs, jobs which will keep them in the land they love and among the people they know. And, that is success in very real terms.

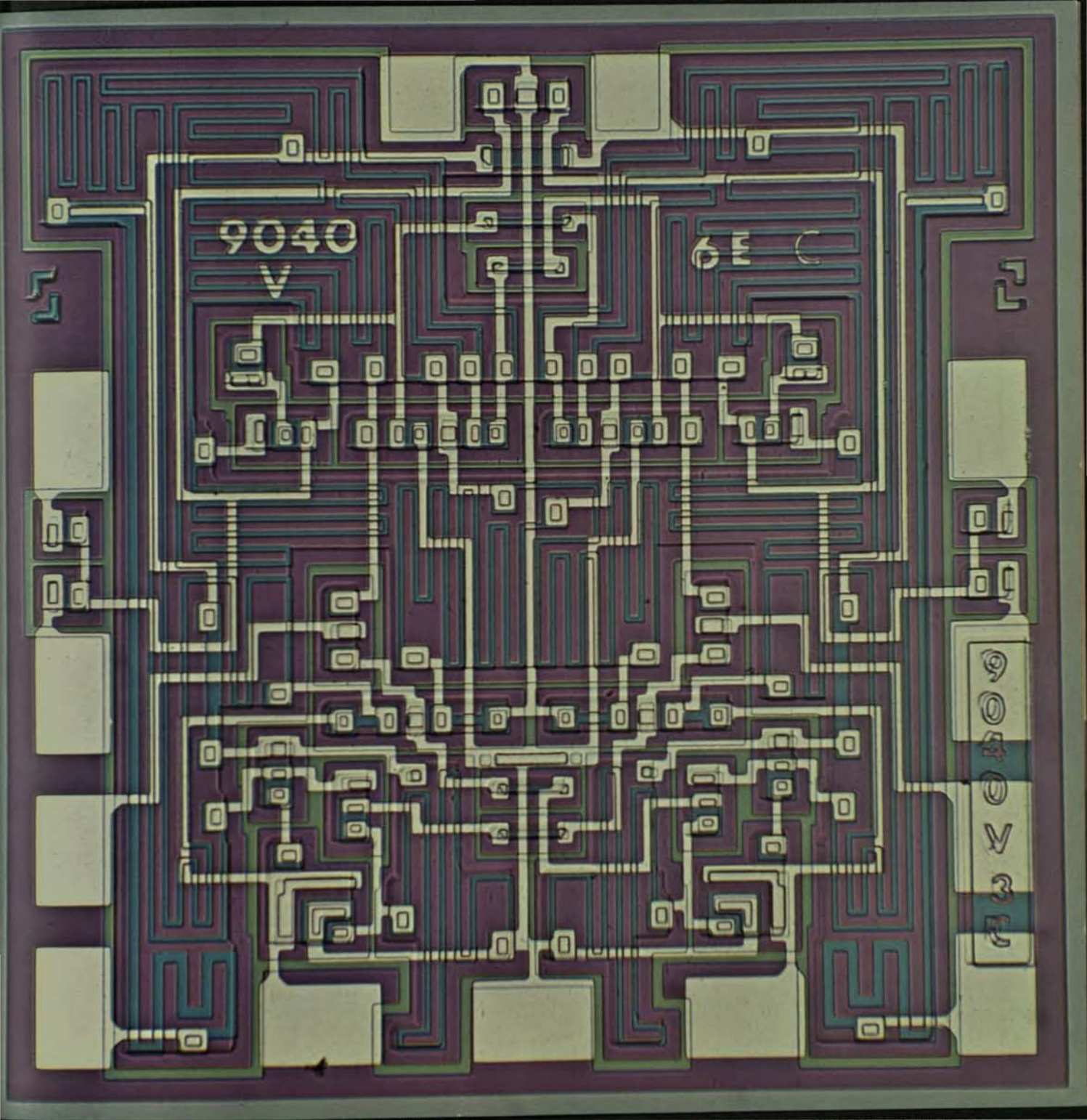


A Fairchild 9040 integrated circuit geometry shown enlarged on the opposite page is in reality this tiny chip. It is packaged in this 13-lead flat pack, just one of many different electronic devices made by the men and women who work at Fairchild Semiconductor's Shiprock facility. The 9040 is used in communications satellites like COMSAT.

9040
V

6M

9040
V



The dedication of this new Shiprock plant is proof of the successful partnership that exists between the Navajo people, the United States Government, and private industry, today represented by Fairchild Semiconductor. In the next several years we expect to see expansion of this nearly all Navajo operated plant, concurrent with further development of the Shiprock community and increased opportunities for all Navajos. There is no doubt in my mind that the human and physical resources of the Navajo people will be a vital and key part of the American economy. We are glad we came to Shiprock to play some part in this industrial growth.

Dr. C. Lester Hogan
President and Chief Executive Officer,
Fairchild Camera and Instrument
Corporation



We are very proud of our association with Fairchild. Together we have turned a hopeful idea into a successful and prosperous business reality. The past four years can best be described as the industrialization of a sleeping giant. The future lies in using the lands of the Navajo people for businesses such as this, places where Navajo labor and skill can be used for the benefit of all people.

Raymond Nakai
Chairman, Navajo Tribal Council



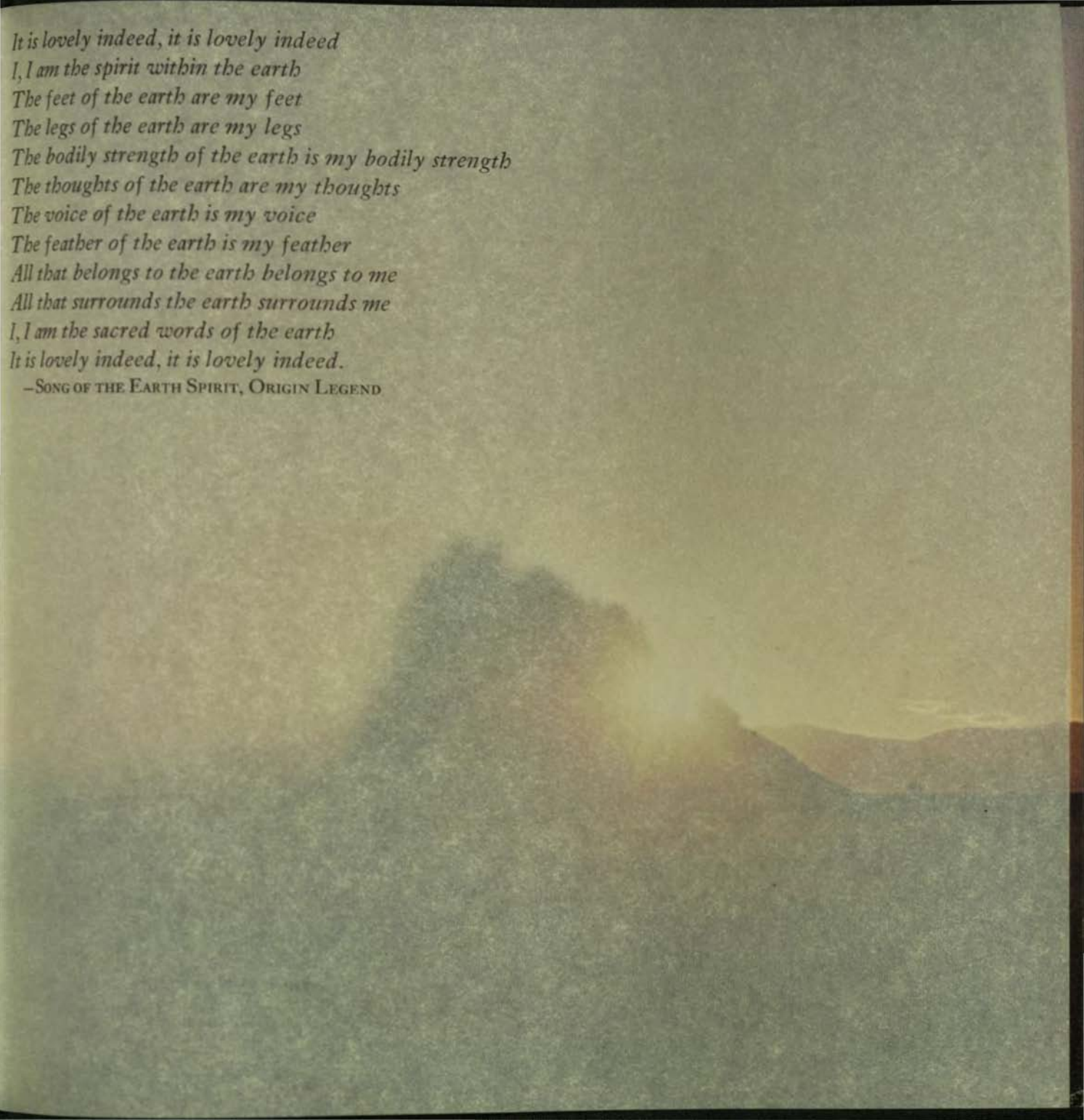
The most important ingredient of any manufacturing operation is people, and I happen to think we have very special people here at Shiprock. The Navajo men and women working here have made my job as Plant Manager one of the most pleasant experiences of my whole life. Their adaptabilities and proven skills have shown they can do any job well, and their industriousness and desire to learn is unmatched. I hope that in the very near future every job in this plant, including mine, will be held by Navajos. The credit for our success here belongs to them.

Paul Driscoll
Shiprock Plant Manager



*It is lovely indeed, it is lovely indeed
I, I am the spirit within the earth
The feet of the earth are my feet
The legs of the earth are my legs
The bodily strength of the earth is my bodily strength
The thoughts of the earth are my thoughts
The voice of the earth is my voice
The feather of the earth is my feather
All that belongs to the earth belongs to me
All that surrounds the earth surrounds me
I, I am the sacred words of the earth
It is lovely indeed, it is lovely indeed.*

—SONG OF THE EARTH SPIRIT, ORIGIN LEGEND





Gerit Hadley

650-327-4224

FAIRCHILD
SEMICONDUCTOR

LET'S TALK FACTS

MARCH 3, 1975

FAIRCHILD SAID YESTERDAY (SUNDAY) IT HAS BEEN FORCED TO SUSPEND SEMICONDUCTOR ASSEMBLY OPERATIONS ON THE NAVAJO RESERVATION AT SHIPROCK, NEW MEXICO, DUE TO THE CONTINUED OCCUPANCY OF THE PLANT BY AN ARMED GROUP OF AMERICAN INDIANS.

WILFRED J. CORRIGAN, PRESIDENT AND CHIEF EXECUTIVE OFFICER, SAID THE COMPANY IS TAKING STEPS TO MEET CUSTOMER REQUIREMENTS THROUGH ALTERNATIVE MANUFACTURING MEANS.

EMPLOYEES OF THE NAVAJO-OWNED FACILITY HAVE BEEN NOTIFIED OF THE ACTION AND ADVISED THEY WILL BE INFORMED BY FAIRCHILD OF ANY FURTHER DEVELOPMENTS REGARDING THE SEIZURE.

"ON THE BASIS OF THE REFUSAL BY AN ARMED, OUTSIDE GROUP -- REPRESENTING NEITHER EMPLOYEES, TRIBAL AUTHORITIES NOR THE COMMUNITY -- TO SURRENDER CONTROL OF THIS PLANT, FAIRCHILD HAS NO CHOICE BUT TO SUSPEND CURRENT OPERATIONS IN SHIPROCK," MR. CORRIGAN SAID.

"THE QUESTION OF RESUMING PRODUCTION WHEN THE INTRUDERS LEAVE CONTINUES TO BE EVALUATED BY THE COMPANY," HE SAID.

"FAIRCHILD REGRETS THAT ITS 10-YEAR RELATIONSHIP WITH THE NAVAJO COMMUNITY HAS BEEN DISRUPTED BY THE FORCIBLE SEIZURE AT SHIPROCK. WE CONTINUE TO SUPPORT THE EFFORTS OF THE NAVAJO NATION, WHICH BOTH OWNS THE FACILITY AND GOVERNS THE RESERVATION, TO REGAIN CONTROL OF THE PLANT WHILE ASSURING THE SAFETY OF ALL CONCERNED.

"WE APPRECIATE ALSO THE SUPPORT THAT OUR EMPLOYEES AND THE SHIPROCK COMMUNITY CONTINUE TO GIVE FAIRCHILD IN THIS REGRETTABLE AND ENTIRELY UNWARRANTED SITUATION," MR. CORRIGAN SAID.

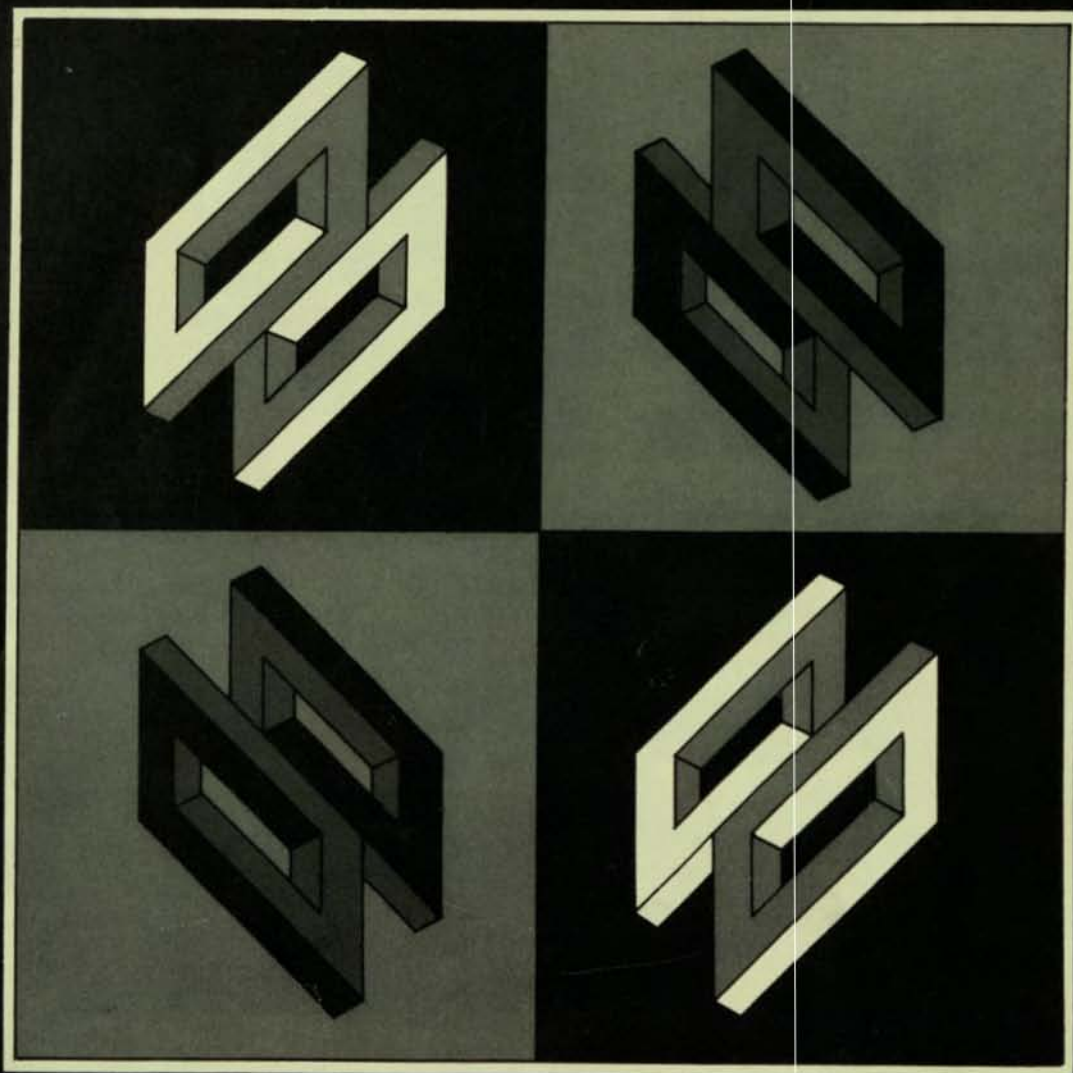
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Craig Hedley
650-327-4224

Innovation is about the art
of managing
advancing technology

Special Reprint
Number Eight, 1969

The Splintering of the Solid-State Electronics Industry



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The Splintering of the Solid-State Electronics Industry

One of the most striking features of high technology companies in the past twenty years is the spinoff. Indeed, around certain small geographical centers, the process of creating new companies—from financing, to organizing people and material resources, to making and distributing products—has become a way of life. Take the semiconductor industry. In the last year and a half twelve new semiconductor firms were launched around San Francisco. Most of them, either directly or indirectly, were spinoffs of Fairchild Semiconductor Corporation, which has already had a rich spinoff history. In looking into this recent spinoff episode, senior editor • Nilo Lindgren • asks whether we may not be seeing the first signs of a fundamental change in the way business is conducted in this country.

From the traditional point of view as to how new industries are formed and evolve, the semiconductor industry, now barely 20 years old, presents some puzzling problems to the industrial anthropologist.

It grows fast, going through generation after generation technologically. Right now, like the computer industry which is its technological peer and natural ally, it is embarked on the realization of fourth-generation concepts. And it shows no signs of losing momentum. Indeed, one of the striking characteristics of this industry is the rate at which it spins off new small companies, and the surprising number of these that survive and grow. Despite predictions that the giants will absorb the little companies and grow more dominant (as the automotive companies did in their earlier stages of evolution) there are signs that an opposite tendency is operative.

In the past year and a half, for instance, 12 new semiconductor firms have been started in the San Francisco Bay area alone, all of them

Deep in California semiconductor country is Walkers Wagon Wheel bar and restaurant, favored by Fairchilders for their after-work gatherings where, it is said, they oftentimes hatched new semiconductor companies.





In the beginning, Shockley co-invented the transistor, and then he decided to go back home to Palo Alto where he started his own transistor company. That was the prolific seed of the West Coast semiconductor industry. Here Shockley, seated at the end of the table, is toasted on the occasion of his winning the Nobel Prize. With him in this early 1957 photo are four of the group of eight young scientists who left later that year to form the Fairchild Semiconductor Corp. At bottom left are Gordon Moore and Sheldon Roberts. At top, fourth from left, is Robert Noyce. Furthest at right is Jay Last. This year the last of the original eight founders of Fairchild left there for other ventures. Hoerni, Last, Roberts and Kleiner left in 1961 to found Amelco. Subsequently, Hoerni went on to found Union Carbide Electronics in 1964 and Intersil in 1967; when Amelco was purchased by Teledyne, Last stayed on to become a VP; Roberts went on to become a consultant and Kleiner first founded Edex, a non-semiconductor firm, and then began dealing in venture capital for electronic firms. Noyce and Moore left Fairchild in mid-1968 to form their own firm, Intel. Blank, the last to leave, joined Nesson Industries, management and venture capital consultants in high-technology fields. Grinich, who has been teaching, rejoined Hoerni this October as an advisor to Intersil.

within a few miles of one another, and there are hints that other new companies are in the planning stage. This is not even counting a half dozen new semiconductor production equipment firms established during the same period.

Our correspondent on the West Coast, Marion Lewenstein, whom we asked some months ago to dig out information on these new companies, reports that even in that industry, the people-in-the-know are stunned at the number of new entries into what has been from the very beginning one of the most phenomenal industries our industrially based country has seen.

You might think a saturation point would have been reached long ago. But counting the new arrivals, there are now nearly 25 semiconductor firms all in the same tight area just south of San Francisco. Why the sudden explosion of new firms? Why all in the same region?

As one looks into it, one finds that almost all of these new firms are (directly or indirectly) spinoffs of Fairchild Semiconductor. Fairchild's own Route 128. That in itself is intriguing. Motorola in Phoenix and Texas Instruments in Dallas haven't experienced a spinoff history like that. And one successful spinoff from TI—Siliconix—didn't stay in Dallas. It nestled right up against the others within cannon shot of Papa Fairchild.

One can say, of course, that the attraction of living in Bay area California is part of the answer. It is, but only part.

One can say advancing technology is part of the answer, but that isn't all either.

One could say that what we are seeing is merely a short-term phenomenon, soon to be re-dressed and normalized, but this "explanation" short-circuits certain other suggestive alternatives.

We might ask, for instance, whether or not the electronics business, as typified in the semiconductor industry, is *fundamentally* different from other businesses? More generally, we can ask whether or not *all* modern high-technology business is *fundamentally* different from the business of the past.

In his book *The Limits of American Capitalism*, the economist Robert L. Heilbroner speculates persuasively that modern technology is a major glacial force changing the basic character of capitalism itself. Is it too far-fetched to imagine what we see in the semiconductor industry is a perceptible instance of such a fundamental change? Rather than living through a short-term event, typified by the trade press mind as "exciting" and "spectacular," might we already be going through the threshold of a more fundamental change whose long-term ramifications and consequences are not yet clear?

There is some evidence to support such a view, and some of the issues pertaining to it have already been discussed in past pages of *Innovation*—e.g., the increasing mobility of our society (Bennis); the social revolutionary upheaval and need for decentralization (Goodman); the semiconductor industry is no ordinary business, it supplies "vitamins" to the whole industrial structure (J. Last); to list just a few.

If we are really in the process of such a fundamental change, what does it mean for the manager of advancing technology? How should he "read" his role?

Such speculative questions can hardly be answered conclusively, but they might be kept in mind as a frame of reference for the study of the semiconductor industry of the Bay area. We suggest that Fairchild's own Route 128 might be viewed as a case study of a more general phenomenon, the nature of which should be actively and vigorously explored.

The immediate reasons for the phenomenal growth of semiconductor companies near San Francisco are many and complex, but the character of the Fairchild Semiconductor Company, as the new president of the parent company (Fairchild Camera & Instrument) Dr. C. Lester Hogan, points out, plays a major role. The fact is that Fairchild was started by eight extremely bright young men, and they attracted to them a group of highly energetic, bright professionals, both in the technical sense and in the marketing sense. This gave Fairchild, Hogan goes on, more than its share of industry leaders who could potentially strike out on their own, and subsequently did just that.

The result of this extraordinary spinoff history is shown on the family tree. The dozen new firms started in the last year and a half are shown in color. Although the tree shows that some of the new company organizers come immediately from other companies than Fairchild, almost all at some point in their careers worked at Fairchild. The map shows the small region where the dozen new companies are located.

In the same region is Hewlett Packard Associates, a semiconductor manufacturer, which is extraor-

dinary for another reason. It is virtually the only firm in the region with no history of spinoffs—only three individuals have left the company so far as anyone knows. The answer? HPA has always had a strong policy of making their people feel comfortable and necessary to their job. Further, long before it became fashionable, the company had stock option plans that extended far down into the company, to the level of some factory workers. (In the past, Fairchild had no such stock options.) Although HPA is beginning to get big and unwieldy now, and there begins to be dissatisfaction, the image hangs on—"Hewlett Packard people stay."

Although the story of the "original eight" founders of Fairchild Semiconductor has been told many times by people in the electronics industry, the highlights need recapitulation here. In 1955, a half-dozen years after his co-invention of the transistor at Bell Telephone Labs, Dr. William Shockley left the Labs and after a brief flirtation with Raytheon in the East, returned to his native Palo Alto to start his own company, Shockley Transistor Corporation. That, in fact, was the beginning of the semiconductor industry on the San Francisco peninsula. Shockley was successful in attracting many really bright physicists and engineers, but was not so successful in his personal relations with them. This was one of the factors which (less than a year after he won the Nobel prize for his work leading to the transistor) helped lead to the departure of the group of eight who founded Fairchild Semiconductor in Mountain View, California. That was in September 1957 with the backing of the Fairchild Camera & Instrument Corporation whose headquarters are on Long Island. The eight founders were Victor Grinich, John Hoerni, Jay Last, Sheldon Roberts, Eugene Kleiner, Julius Blank, Gordon Moore, and Robert Noyce, who two years later, in 1959, was put in charge of the Fairchild Semiconductor operation, and who managed it over most of the time of its spectacular growth.

The recent activities of the eight founders, who have now

all left Fairchild, are summarized in the Shockley photo caption. One might note that the eight have alone been directly responsible for the formation of at least five new companies since Fairchild, although only three men—Noyce, Moore, and Hoerni—are still directly involved in semiconductor manufacturing. The original Shockley Transistor Corp. meanwhile was bought by Clevite in 1959, then by ITT in 1965. ITT moved the R&D work to Palm Beach, Florida, in 1968, and shut down Shockley's Palo Alto facility in 1969. Shockley himself moves between Stanford University, Bell Labs, and other non-semiconductor activities.

Though Fairchild grew fast after the breakaway from Shockley in 1957, it experienced its own first spinoff in 1959 when E. M. Baldwin left to form Rheem Semiconductor; and then in 1961, four of the original eight—Hoerni, Last, Roberts, Kleiner—formed Amelco. This was quickly followed by the formation of Signetics also in 1961, of Molelectron in 1962, and of General Micro-Electronics in 1963, all out of Fair-

child. Of the original eight, Hoerni must surely be the most restless or driven—since forming Amelco in 1961, he has gone on to form Union Carbide Electronics in 1964 and Intersil in 1967.

In retrospect, considering these and other subsequent spinoffs, one could conclude that the semiconductor industry (besides being what it is—one of the most competitive, gut-eating industries going) has also been one of the most unusual and spectacular schools of technical management in this country. It should be remembered that Shockley and the men he attracted were scientists, trained at a time when scientists expected to be just that, and before the tremendous financial rewards of semiconductor theory had become overpoweringly evident.

When Noyce, for instance, was made manager of Fairchild's operation, he was only 32, he had no management experience, and more than that, some reluctance to become one. He resisted going with the defecting group at first, though he was prevailed upon. And when he was offered a management position, he took it partly because of an incident that had occurred during his work with Shockley. During the clashes that had gone on there, Shockley had conducted a straw vote among his thirty or so colleagues, asking who among them they believed would be the best technical leader. Everyone voted for Noyce! That expression of confidence persuaded Noyce, when the time came, that he should step into the position of making decisions and being responsible for them.

When Noyce and Moore left Fairchild in July 1968 to form a new company, followed not much later by the last of the original eight, Julius Blank who joined Ness Industries, it marked, in the world of electronics, the end of an epoch.

Noyce's departure was duly observed by the investment world. Fairchild stock took a sharp dip, the electronics and financial communities spawned rumors faster than the production lines turned out new semiconductor circuits, and Fairchild lived for the space of a breath without a leader. Then, C. Lester Hogan was lured away from Motorola by Sherman Fairchild to become the new president of Fairchild Camera & Instrument Company, and hot after him came some of his erstwhile Motorola colleagues and an enormous lawsuit which is still to be settled.

It was not long before Hogan made his presence felt at Fairchild. From the outside, there was clearly, as the stories of departures and new appointments made the news, a lot of reorganizing going on as Hogan reshaped the company. From the inside, as Hogan studied the internal economics of the Fairchild operation, a fascinating insight emerged. Hogan discovered, in the retrospective of the records that in May 1965 there was an abrupt change for the worse in all the internal records—in sales, production, and so on. That sharp break came in exactly the same week that Noyce had left active management to act as a vice president of the parent company in the East! It showed, in Hogan's view, how brilliantly strong Noyce's command was of the semiconductor operations. Both Hogan and Noyce have concurred in stating that certain important changes were needed in Fairchild about that time. Hogan testified, "Bob Noyce made my job easy for me. He had already done all the hard things that needed to be done in building Fairchild, and he left the easier part for me."

Among other things, in fact, Hogan was able to attract some top quality semiconductor professionals who had not previously been at Fairchild. From Hewlett Packard, he got M. M. John Atalla; from Bell Labs came James Early; from Stanford came John Moll, a full professor.

Meanwhile, Bob Noyce and Gordon Moore had gone on, last July, to form their new company, Intel, as had been rumored, a company that almost everyone predicts will be as successful as was the original Fairchild. With its first products just coming into the

market ("right on schedule"), Intel projects at least \$25 million in sales within the first five years. Some people think they might do twice that. Noyce believes they will build up a \$100-million business "over a period of time."

Moore, Intel's vice president, stresses that although there is lots of room for specialization, and therefore room for new firms, the only way for a semiconductor company to stay in the mainstream is to get big. Yet, with the change at the top of Fairchild, which all (including Noyce) agree is for the best, the parent company is expected to remain a major and alert contender in the semiconductor business. Can there be two companies of the same great size in the same business? Much less 12? What are the chances of these new spinoffs?

The early rash of Fairchild spinoffs, in 1961-63, arose partially because many key people (including four of the original founders) felt frustrated by the increasing bigness of the company and by the refusal of the conservative Eastern headquarters to give stock options or profit-sharing. One of Hogan's first acts, in fact, was to pass along a greater share of the action down through the lines with stock options. But the new spinoffs do not seem to come from dissatisfaction. Rather the reverse. The evolving technology of semiconductors is once again opening up handsome new opportunities.

Generally speaking, the spurts of real growth in microelectronic firms have come with breakthroughs in technology. For instance, Texas Instruments succeeded with its initiation of silicon transistors, Fairchild with the so-called double diffused and planar techniques, and Siliconix with so-called junction field effect transistors (FET's).

What is happening today in the semiconductor technology is potentially of a different order. As one looks at the new companies emerging, one could break down their product lines into two rather traditional categories—those that are going after different specialized segments of the market, and those that are exploiting the forefront technology to go after the colossal computer market. The latter category includes the so-called MOS (metal-oxide-semiconductor) and LSI (large-scale integration) technologies. The name LSI refers to the semiconductor chips that hold an enormous number of circuits rather than just a few components. For instance, one of the first products being developed by Intel is an entire 256-bit memory that goes on a chip 1/10th of an inch on a side! A great deal is expected in the field of

advanced semiconductor memories for computers, especially if computer manufacturers do some redesigning to take advantage of such circuits.

What this means is that as computers become larger and faster, the standard concepts of their architecture are changing. It is said that the use of small, fast, more expensive semiconductor memories to act as buffers to assist the core memory could increase the performance of existing core memories by as much as 300%. More attractive, but perhaps further away (as volume production drops the cost), is the use of semiconductor components for the core memories themselves. Thus, there is a push in the new small companies to perfect semiconductor memories and to persuade computer manufacturers of their advantages.

Another enormous new market growing out of the advancing technology will be for light-emitting devices, which the experts believe will find many possible uses (in digital readout, and so on).

But there is an aspect of the advancing semiconductor technology that goes even beyond these traditional directions, as vast as they are. The plain fact is that hardly anyone (in

all the other industries outside the semiconductor field) really grasps the enormous amount of electrical circuitry he now has available to him "on the head of a pin." That is, LSI's, or even smaller units, can undertake tasks in industries that never before used any electronics—all kinds of industrial machinery, for instance, could be redesigned for greater effectiveness and controllability through the incorporation of what amounts to the "intelligence" functions of LSI. Automobiles will certainly use more such microminiaturized functions—small cheap computers for safer driving, and the like.

This penetration of the semiconductor technology into other industries is really just beginning. It is going to require much "custom" designing of integrated circuits, and the redesigning of industrial (and home) equipment, but the semiconductor industry is consciously mobilizing itself for precisely this end. The consequence of this twin thrust—of semiconductors and computers—is that the Second Industrial Revolution (that of integrated information functions in all machines) that Norbert Wiener predicted 20 years ago is fast upon us (maybe in light of recent events, we should call it the Age of Electro-Aquarius).

In any event, much of the explosive spinoff and reorganizing within the semiconductor industry may be regarded as partly symptomatic of as a broadening of aims allied to a consciousness of specific new markets.

But what do the new company founders say about themselves? Let's take a quick look in the next three pages.

Semiconductor Country: an Overview

Within the San Francisco Peninsula area, semiconductor firms are moving southward. Palo Alto, the initial location for Shockley and early Fairchild, is 35 miles south of San Francisco. Twenty five or more semiconductor facilities are located in this one small area. The furthest from one another is probably only 17 miles . . . 20 at the most. Many are only ¼ mile off the extensive and swift freeway system, the furthest from a freeway is about 1½ miles. Airport connections, also important to the semiconductor industry, are excellent. San Jose has a growing airport; San Francisco has worldwide service; and fast helicopter service links up the major points of the whole Bay area.

As the population increases in this area, all the newcomers who moved from crowded Eastern seaboard locations see some of the same problems of transportation, smog, hustle-bustle they thought they had left behind. So the impulse is to move down toward San Jose where there is more open, cheaper land and fewer people. Some communities—like Sunnyvale's Science Industry Park and Santa Clara's Space Park—are trying to attract more of the electronics industry. The executives of the many semiconductor companies live mostly in the plushier areas west of Palo Alto—the Los Altos Hills, Saratoga, Portola Valley—where it is easy to commute to Santa Clara, Sunnyvale, Mountain View.



1. Advanced Memory Systems, Inc. is aiming mainly at developing so-called bipolar memory semiconductors, the technology in which the founders have had the greatest combined experience. This area, the founders feel, is not being properly served now. Also, there is less existing competition in the system area, so these people are using designers with computer experience to come up with customer-oriented products. The staff held middle management positions in advanced technology in their previous firms.

Founders:

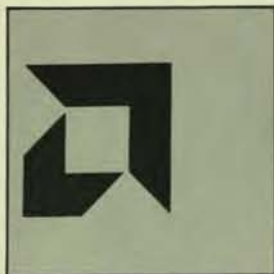
Robert Lloyd, president—formerly with IBM, manager of memory device development
 Jerome Larkin, vp marketing—formerly with Fairchild, IC product manager
 Brent Dickson, vp manufacturing—formerly Motorola, manager LSI production
 Drew Berding, vp engineering—formerly IBM, manager high-speed memories
 Charles Fa, vp technology—formerly of Collins, Newport Beach, manager IC technology

Capitalization:

private plus two mutual funds

Employees:

40 total; about 25 engineers



2. Advanced Micro-Devices, Inc., whose entire group of founders came from Fairchild, is considered to be most "market oriented" of all the new startups. The firm will specialize in medium scale integrated circuits (MSI) (both linear and digital types), and will emphasize its processing capability to distinguish itself from the big firms who can offer low costs through mass production. MSI complex linear and digital circuits, which are difficult to build, depend more on the kind of customized engineering that a small company can provide.

Founders: (all formerly of Fairchild)

Walter J. Sanders, president
Jack Gifford, vp marketing and business development
John Carey, vp complex digital integrated circuits
Larry Stenger, vp complex linear circuits
Edwin Turney, vp sales & administration
Jim Giles, director linear circuit engineering
Frank Botte, director linear circuit operations
Sven Simonsen, director complex digital engineering

Capitalization:

investment houses and banks from both Coasts and Europe

Employees:

11 at present; expect 50 by 1969, about half of whom will be professional staff



3. Avantek, Inc., which was started four years ago to produce broadband microwave components in micro-electronic configurations, has launched its Micro Integrated Circuit Division to fulfill the need for highly specialized, exotic devices that the large companies are pretty much ignoring. Thus, by satisfying its own need for high frequency, high gain, low noise microwave transistors, amplifiers and oscillators, and by keeping pace with developments in other microwave areas, the company can take advantage of a grow-

ing advanced equipment market of other users as well. Because it had no semiconductor background, Avantek lured Dr. Yozo Satoda from Hewlett Packard Associates and Dr. Andrew Anderson from Texas Instruments to head up the MIC Division.

Founders:

Lawrence Thielen, president—formerly of Applied Technology and Ampex

Dr. Yozo Satoda, manager MIC division—formerly of Hewlett Packard Associates
Dr. Andrew Anderson, manager active devices—formerly of Texas Instruments

Capitalization:

Avantek (founded 4 years earlier) is parent firm



4. Cartesian, Inc., which was phased out of a mask-making company affiliated with Electromask, Inc. It will engage in circuit wafer fabrication and LSI masking for those other firms that can design and test their own circuits. What Cartesian offers is lower cost for mass production of LSI devices through low overhead and without high-priced circuit designers. Part of Cartesian's "talent" philosophy is to look not for supermen, but to get competent middle management from older firms where such men have no access to stock options.

Founders:

Gerald M. Henriksen, chairman of the board and current president of Electromask, Inc.
Robert Cole, president—formerly of Philco-Ford General Micro-electronics, earlier with Fairchild—then with Cartesian Corp., an affiliate of Electromask, Inc.
Daniel R. Borrer, vp—formerly of GME, before that Fairchild, then on to Cartesian Corp.

Capitalization:

investment banking

Sales:

several hundred thousand—June 1970; \$2 million—June 1971

Employees:

12; 35-50 projected within a year



5. Cermetek, Inc., will concentrate its products on high speed, high voltage hybrid devices with high reliability, a field in which designer-founder is said to have no competitors. For instance, the firm now has a high-speed clock driver for MOS circuits that is said to be unique. The company expects to keep a lead in mass production of hybrid MOS devices (nearest competitors are Signetics and National Semiconductor) through a licensing arrangement whereby Components, Inc. (located in Maine and in Phoenix) will produce Cermetek designs, a mode of operation that Fairchild and other firms practiced in the past.

Founders:

Samuel A. Schwartz, president—formerly design consultant to Fairchild, ITT, and others—also research scientist with Lockheed Missiles and Space
James Charnes, executive vp—formerly with components division of Sprague Electric, before that with Burroughs Corp.
Dr. Bernard Jacobs—formerly of General Instruments, now resigned from Cermetek

Capitalization:

privately held, and through investment firms; probably go public in year or two

Sales:

\$4 million by October 1970

Employees:

55; 200 projected by end of second year



6. Computer Microtechnology, Inc. will aim at the area that is clearly going to be the biggest future market and that is also going to be most competitive—computer memory devices. In a big and growing market, president F. J. Megan argues that there will be no single source and that all companies will get their share. Those who have a good grasp of the memory technology and who are (as the currently popular phrase describes them) "people sensitive," believe that it

"will be hard not to be a success" despite the competition.

Founders:

Francis J. Megan, president—formerly of ITT, Florida
John Schroeder, vp process development—formerly of Fairchild
John Schmidt, vp engineering—formerly of Fairchild
Charles Ellenberger, vp management—formerly of Fairchild

Capitalization:

personal from founders, some seed money from other personal investors and investment sources

Employees:

35; 100 within a year



7. Intel, Inc., started by Noyce and Moore from Fairchild, will push hard with LSI varieties of advanced memories. These men expect that by concentrating on memories, these products will get cheaper and better, and that Intel will keep a lead on the giants like Fairchild, Motorola, and TI, whose efforts are more dispersed. Although Intel is expected to grow fast, it is significant that Noyce was partly motivated to leave Fairchild because he prefers keeping closer touch with the laboratory research, which is easier in a small company atmosphere. He sees the small company as allowing more "human involvement," as well as providing the chance to make big money. Noyce and Moore both indicate they were getting stale in their old jobs, and uncomfortable as the situation at Fairchild changed, so that they felt a loss of loyalty from both above and below. Now, with Intel, these men can explore a major new market opportunity with the decision-making power in their own hands.

Founders:

Dr. Robert Noyce, president—formerly of Fairchild
Dr. Gordon Moore, vp—formerly of Fairchild

Capitalization:

personal investment, principally by founders but otherwise from a few other people in the firm and other private sources

Sales:

\$25 million projected within 5 years

Employees:

125 by September 1969



Monsanto

NEW ENTERPRISE DIVISION

8. Monsanto Co., headquartered in St. Louis, which has a background in developing materials used in photo emitting devices, is now setting up an off-shoot called Electronic Special Products. The company will concentrate its product line on photo emitting or photo-optic electronic devices. Not only is this product new but so are its applications. However, the market projection is \$300 to \$500 million/year within ten years, and Monsanto is a strong bidder for a healthy share. Like other established companies who have come to the San Francisco Bay area, Monsanto has the same reason—this is where all the high technology people, where new developments are assimilated virtually by osmosis at cocktail parties and the like. George M. MacLeod, general manager of the new operation, as a big company representative must struggle with a conservative Eastern management to supply the motivation other small new companies can offer top professionals (i.e., stock options). But he has an alternative in his deck: He is setting up each area of research in light emitting devices as a miniature business set-up, with its own R&D, its own marketing, and so on.

Founders:

New division of Monsanto, George M. MacLeod is general manager

Capitalization:

parent company

Employees:

25 including 15 professionals

dice, or package. In practice, this differs from Fairchild custom work, for example, in that Fairchild works out the complete configuration and then fabricates it. The customer must reveal proprietary information about his end product and then pays a markup on engineering time as well. With the ever widening use of semiconductor circuits, there has been an increasing need for semiconductor fabricators who will work to a customer's mask, and there are, as well, an increasing number of companies that have staff engineers who can design circuits for MOS or LSI production. (Hewlett Packard, incidentally, started its internal semiconductor operation to protect its proprietary information. At first it sold most of its production within the company, but has progressively increased external sales, and now is one of the top five semiconductor producers in the San Francisco area.)

Founders:

Robert H. Norman, president—formerly of Fairchild, founder of GME, left there for Nortec after GME purchased by Philco
Thomas L. Turnbull, vp financing—formerly of Applied Technology
Edgar R. Parker, vp operations—formerly of GME, stayed on after Philco purchase but went to Fairchild when GME moved east

Capitalization:

individual investments, including founders

Employees:

15; 30 by end of year



10. Precision Monolithic, Inc., aims at moving fast with an initial big financial investment in order to "get to the top of the heap." Its product line, to start, consists of unusually precise analog integrated circuits for special processors and for peripheral computer equipments and special circuits for digital-to-analog converters. The founders reason that by putting together an electric capability by recruiting people from instrument, aerospace, and circuit design firms, and by bringing in people with good judgment who have not been "isolated in top management," they will help create a healthy company, where the research teams will be small and where each individual will see the results of his contributions. One feature of Precision's backing is that Bourns, Inc., an electronics components company in Riverside, Cali-

fornia, has put up 40% of the initial investment with the option to acquire controlling interest of the firm by mid 1974.

Founders:

Marvin Rudin, president—formerly of Fairchild
Dr. Garth H. Wilson, vp—formerly of Fairchild

Capitalization:

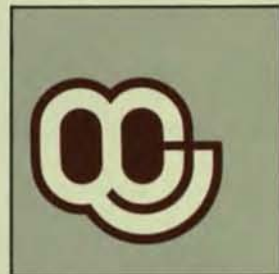
40% by Bourns, Inc., an electronics components company from Riverside, Cal.—60% private, mostly from within company

Sales:

\$10 million projected in five years

Employees:

11; 100 by early 1970



11. Qualidyne Corp., whose present president, H. Ward Gebhardt, was previously a founder of Intersil (in 1967), takes a tack contrary to all the other new startups. Its founders believe that it is not necessary to start out with a unique position, either technically in its products or in its potential markets. New items, they point out, are not company money-makers. For instance, Intersil, which never bothered becoming a technological leader, nonetheless goes on earning money. So, Qualidyne says, it will reverse the usual procedure in becoming a leader—it will do its technological development *after* it is established. This it will do by producing custom and standard sense amplifier integrated circuits for computer core memories. Most of the firm's business thus far is as a "second source" producer for devices pioneered by other companies. For the future, the company feels it has up its sleeve the capability of marrying micro-resistor thin-film techniques with linear integrated circuits, which so far no one else has been able to do successfully.

Founders:

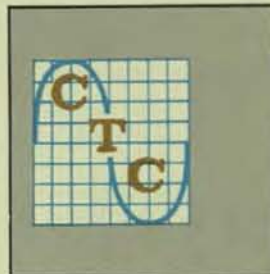
H. Ward Gebhardt, president—formerly of Fairchild and among founders of Intersil
Dave Hilbiber, former president, now left—formerly of HPA and Fairchild
William Lehrer, manager thin film—formerly of Fairchild
Eugene Blome, manager photo masks—formerly of Fairchild

Capitalization:

venture capital and investment of founders

Employees:

35



12. Communications Transistor Corp., the newest of the new dozen, formed as of Friday, October 17th, also has three founders who have been at Fairchild, although its president, Thomas E. Ciochetti, was most recently with National Semiconductor. The new company will be located in plant space at Varian Associate's Eimac Division and will be a Varian affiliate. It will produce high frequency transistors in the UHF, VHF, and microwave range, approximately the same range served by conventional Eimac klystron tubes. Thus, it seems clear that CTC is planted cheek to jowl with its first "natural" market. Varian holds equity in the firm, and some Varian officers will sit on the CTC board. However, the officers of both companies insist that CTC will preserve its own distinct identity.

Founders:

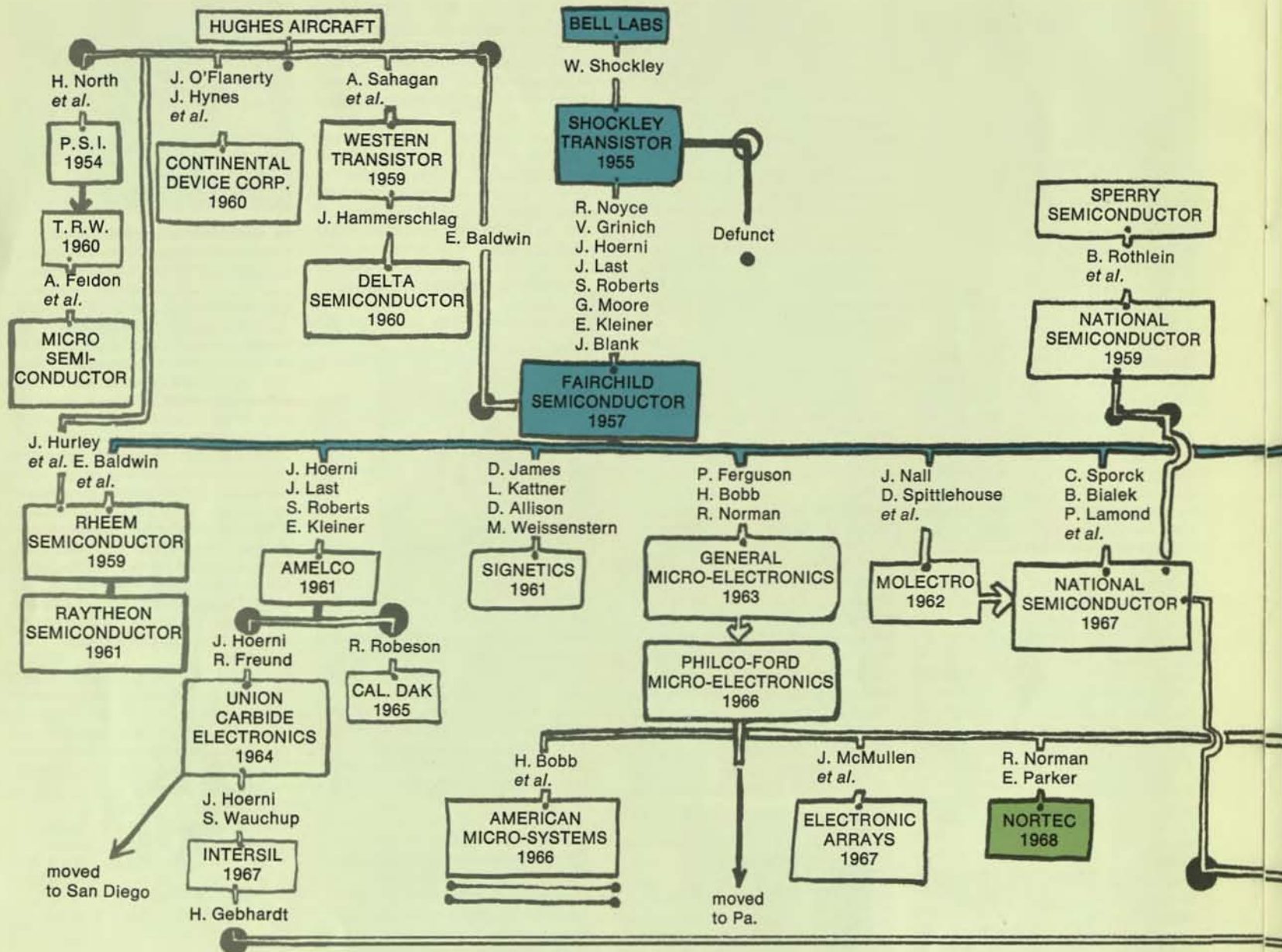
Thomas E. Ciochetti, president—formerly of National Semiconductor and Fairchild
Robert Reber, vp—formerly of Fairchild
Thomas Moutoux, vp engineering—formerly of Fairchild

Capitalization:

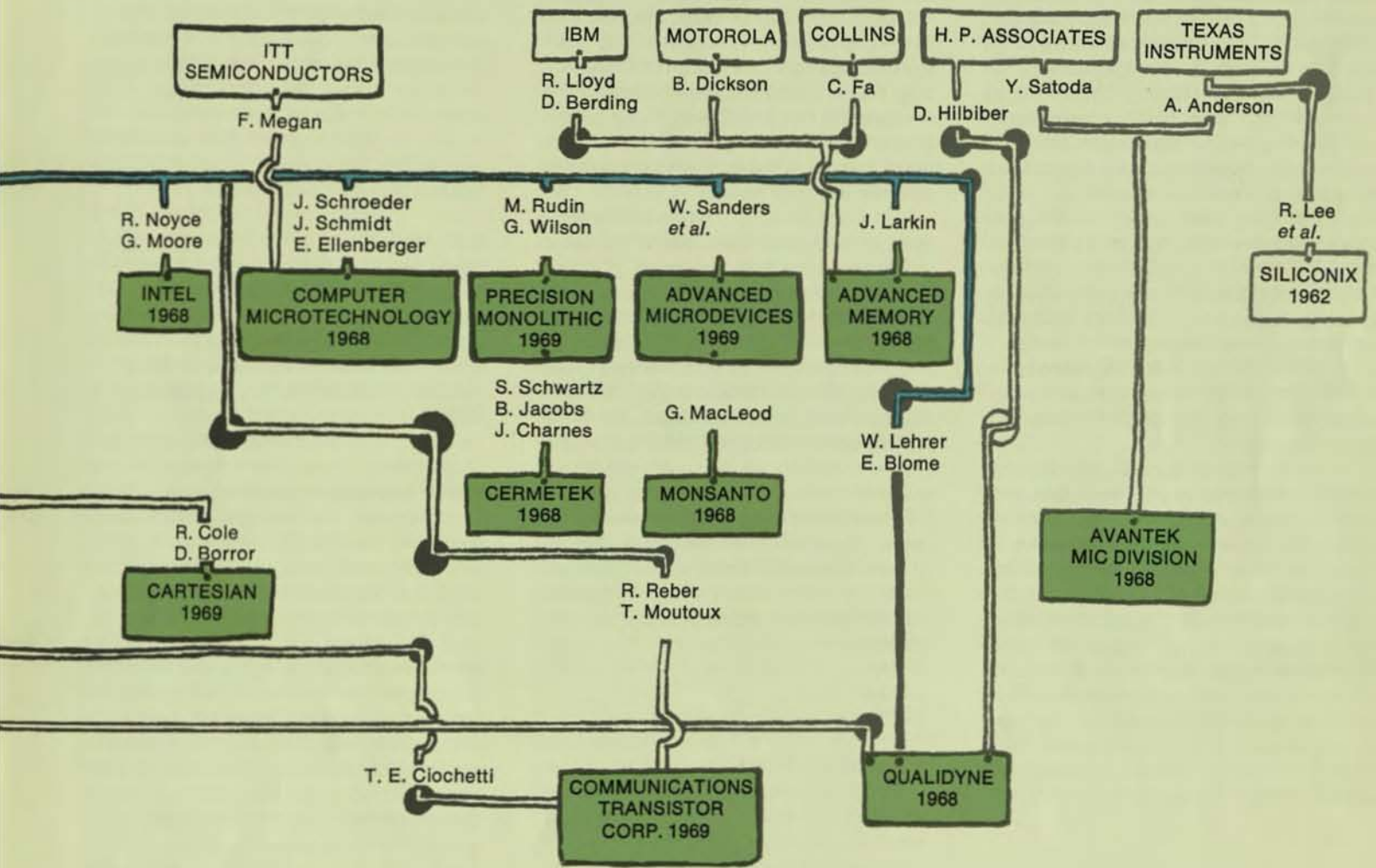
affiliate of Varian



9. Nortec Electronics, Inc., whose president Robert H. Norman was one of the founders of General Micro-Electronics in 1963, and who was with Fairchild before that, will specialize as fabricators in MOS and LSI production. Rather than compete with Fairchild, Signetics, Amelco, and others, the company will use its customers own designs rather than generating its own proprietary circuits. With the mask provided by the customer's engineers, Nortec will make the wafer,



Partial family tree of West Coast semiconductor firms showing (in green) the dozen new companies launched in the last year and a half. Brief descriptions of these new companies appear on later pages with a map showing their general location in the San Francisco Bay area. The main line of the Bay area semiconductor industry (in blue) runs down from Bell Labs through Shockley and Fairchild. Although this family tree shows some of the founders of the new dozen coming from companies other than Fairchild, most of them had worked at Fairchild earlier in their careers.



That's the quick rundown on the rough technological positions and philosophies of the new dozen. What are their chances for success?

Knowledgeable insiders in the semiconductor industry say that Intel (7) will "absolutely" make it, for not only are Noyce and Moore technical geniuses, but they have their already spectacular track records at operating a company. Cartesian (4) has a smart formula, but there is some doubt about how large it can grow. Monsanto (8) seems a good bet on the basis of its unusual technology. AvanteK (3) may become leaders in a specialized area and financially lucrative, but not likely to become giants. Advanced Memory Systems (1), Cermetek (5), Computer Microtechnology (6) are all given a "reasonable chance" on the basis that they have the ingredients for success. Precision Monolithic (10) is thought to have smart enough leadership, though the firm may not be specialized enough. Nortec (9) and Qualidyne (11) are looked at dubiously mostly because they lack high-technology capability, and it is pointed out that Qualidyne's "reverse" formula has not previously succeeded in the semiconductor industry. Most uncertainty seems to register on Advanced Micro-Devices (2).

That is, of course, only one set of starting odds on the new dozen, and they leave out certain interesting possibilities. For instance, the general feeling in the semiconductor community in the West is that the market is so bullish for the evolving MOS technology, the diversification of products in light of ever-widening applications creating room for all, and the semiconductor memory business so staggering in its potential, that it will be hard for anyone with any competence to lose. Even if all these firms are not around five years from now, the founders, it is said, will

have made money by selling out to others. Certainly, the new firms with big parent backing (who hold options to buy controlling interest later) fuel this image. The Westerners think of Raytheon's acquisition of Rheem and Philco-Ford's acquisition of General Micro-Electronics.

So, it is said, no one will lose, for all these people are competent. As one founder said, "We all know each other, and we all respect each other's capabilities." But only a few, it is assumed, will really make it big. And no matter what they all say about their motives—the challenge of going after new markets, the ego satisfaction in being top dog, the excitement of risk-taking where the potential for reward is good, the pleasures of a small company—there is little doubt that the prime motive for most is the potential financial reward.

However, the situation is also read more darkly by some observers. They feel that some of these new companies are being deliberately set up for luring in public money, and that the founders will sell out, enriching themselves and leaving others to hold the bag. Said one long-time industry observer, "Most of these companies are parasites, the modern day equivalent of gold-mining stocks." Little companies, he says, do have a real economic function in developing markets for a radically new technology like holography. But when a technology is mature, he concludes, as it is with semiconductors, there is a real question as to whether the little company is performing a socially useful function.

Why the semiconductor industry should have grown so strongly on the San Francisco peninsula has been partially answered and has been partially self-evident.

The obvious reasons that everyone cites, once Fairchild's germinal role is acknowledged, is that besides being a pool of major talent, it is the best region for recruiting lower levels of personnel such as senior technicians, laboratory workers, assembly workers (mostly girls), and so on, who would be expensive to move across the country the way engineers are. The availability of support people with 5 to 10 years' experience in such work as machine tooling for dies, saves new companies lots of training time. Moreover, it is easier to lure such workers to change jobs because they know they can always get another job in the same locale if the new company fails.

On top of this is the availability of materials and equipment—vendors of vacuum equipment, silicon and industrial gas (clean nitrogen, for instance, is hard to get in regions where winters are snowy). Because the vendors are familiar with the problems of the semiconductor customers, they are able to offer better services.

Also, Richard Lee, president of Siliconix, notes the influence of the University of California, Berkeley, and Stanford. Between the two, they are probably doing the leading solid-state work in the U. S., Berkeley being strongest in solid-state applications while Stanford is strongest in original development.

On that point, Robert Noyce points out that it was after the original success of Fairchild that the two schools became important supporters of the technology. If the Shockley-Fairchild ventures had not brought an influx of people interested in the field, Noyce believes the two schools may not have become the solid-state leaders they now are.

Not so obvious is the existence of a strong financial community that has confidence in the semiconductor industry. Because of the existence of past winners, there has been bred a sense of confidence among investors as well as among professional employees.

Still less obvious to the outsider is the atmosphere of mutual help that pervades the peninsula and that is beneficial to the new company. One new company founder (James Charnles of Cermetek) said, "If I need something, I know I can walk

over to Fairchild and get help." Unless one is directly competitive with another firm, one can get aid even from a relatively competitive firm.

Everyone in fact speaks of the enormous camaraderie in the region. Despite their being competitive on a business basis, and their business willingness "to wipe someone out," the high-technology people mix frequently socially, exchange ideas, and have a genuine high regard for each other. Most of the top management people from different companies are social friends. Said one, "It is not like GE and Westinghouse top management who are not likely to become close personal friends."

One fact certainly stands out. Most of the people are ex-Fairchilders, but not even those who were forced to leave Fairchild recently seem to have anything nasty to say about Fairchild or Lester Hogan.

Hogan himself has been struck by this since his arrival, and he was unprepared for it. He sees a number of reasons behind it. For one thing, over the years of working together, many friendships have developed. When you see people, even rivals, in relaxed social conditions, Hogan says, you learn to like their human qualities. You learn to assess their strengths and weaknesses, and you know in what areas they will likely succeed and likely fail.

Another factor is the geographical closeness, with many industry people living and working nearby, so that encounters are frequent. It's hard to build up images of "the enemy," Hogan remarks, when you see someone often. In contrast, when you are isolated, as you would be in Phoenix or Dallas, for example, without frequent contact with your competitors, it is much easier to build false images.

There is, too, a family feeling among semiconductor people, and Fairchild is the father. That's why, Hogan says, they don't speak harshly of Fairchild—it would be like attacking their father. This is confirmed even by some new-firm founders who were

displaced by Hogan. If they were to continue working for a salary, they say, they would prefer working at Fairchild rather than any other firm because the parent company, with its big resources, allows an individual more flexibility in research and a chance to be creative.

Why then don't they go back to Fairchild when the new venture sours, say, through personality conflicts? Says one man who has started more than one firm: "A certain momentum builds up. When you have started one successful firm, it is difficult to go looking for a job. There is a tendency to regroup with other people and start yet another firm." Pride is certainly an ingredient—a man with enough ego to launch his own company is not going to find it easy to admit failure. Another reason, of course, is that even stock options in another company are not as attractive when you get a taste of the potential financial rewards by starting your own.


One must also look at the other side of the picture: Why didn't new industries spring up around Motorola and Texas Instruments? One reason given is that Phoenix and Dallas are not nearly as attractive places to live, the climate is too hot, and so on.

A case in point is Siliconix, Inc., whose principal founders, all from TI, chose to emigrate to the Bay area rather than stay in Dallas, both because they personally preferred it and because they knew it would be easier to get the high technology people they wanted to move from the East or Midwest rather than the reverse.

Whether climate and the metropolitan attractions of San Francisco were the prime movers or not, the fact remains that Motorola and TI never could attract the number of high calibre, high technology people that Fairchild did. In the semiconductor community, those companies were considered too mundane and were unable to attract many "genius personalities." But Fairchild started off with so many of the bright, creative types who had the urge to do it on their own that they started a chain reaction that now reaches down even to mediocre people. "If so-and-so can do it, so can I," is virtually a slogan of the Bay area companies. The aura of Fairchild accomplishment hangs on.

But there are gnats in semiconductor paradise too. Some professionals are sometimes reluctant to move West because the Bay area has a high cost of living, is smoggier and more crowded than other regions, and has a reputation for more hippies, more drugs, more unrest among the young. They do not wish to expose their children to "immoral" California. But this reluctance is exhibited virtually always from Midwesterners, not from those on the East Coast.

A persuasive aura of well-being comes through all the descriptions of the Californians. It is almost enough to make an Easterner bolt for the semiconductor paradise, especially as winter dulls the skyline of New York and the icy slush impedes progress along the sidewalks. But then, New York is the publishing capital of the U. S. gathered tightly on the small island of Manhattan. Everyone knows everyone, and even competitors meet often socially. There are publishing spinoffs, and new magazines like *Innovation* are started. There is an esprit de corps and...well...a common sense of superiority. The real "professionals" in any field, one supposes, are the ones who enjoy doing what they are doing.

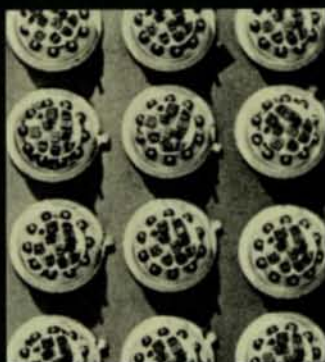
And what they are all doing together is an open-ended proposition. An evolutionary (or perhaps revolutionary) process has been set in motion, in which all groups in society seek participation, and the outcome of which is yet to be crystallized. For the short run, it is certainly not stability. 

This article is reprinted from *Innovation*, the journal of The Innovation Group. It is published for the Group by Technology Communication, Inc.

Purpose of The Innovation Group is to advance the art of managing technology. It has been organized by Technology Communication, Inc., to include men who manage the work of scientists and engineers, executives of public and private organizations in which technology plays an important part, and other people who are concerned that changes in technology be skillfully managed. Activities of the Group include: publication of its journal, **Innovation**; development and distribution of books, reports, films, and tapes on topics important to technical managers; conduct of workshops and seminars; arrangement of direct contacts among members of the Group.

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FAIRCHILD INTEGRATED MICROSYSTEMS



Many of the needs for lightweight and compact packaging that cannot be met with monolithic integrated circuitry are now possible with hybrids. Hybrids fill the needs for microminiature devices that are presently beyond the range of monolithic technology. Design functions such as flexibility in component use; tight electrical tolerances; high voltage requirements; and power dissipation that are difficult in monolithic design, are now easily obtainable in hybrid devices. □ The following pages discuss how we can help solve problems you encounter with lightweight and compact packaging with a broad range of hybrid products now available in mass production. If your application does not appear to be available in a standard hybrid, the Design Guide section of this brochure explains how to quickly determine if your circuitry is feasible in a custom device.

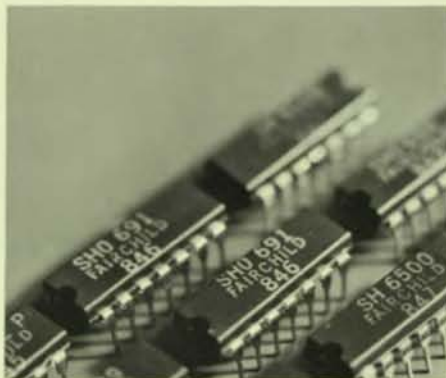
Selecting the Right Manufacturer

If you are in the market for any type of hybrid product, the following are most likely your primary considerations in selecting a manufacturer:

Capability Is the manufacturer capable of delivering what you need, when you need it, in the quantities that you specify?

Reliability or Quality Can you rely on the fact that each hybrid shipped to you measures up to your electrical and mechanical requirements?

Economy Quality doesn't necessarily mean high cost. Does the manufacturer have facilities to produce the hybrid you need as efficiently as possible?



How We Can Help You

Here are a few reasons why Fairchild is particularly qualified to deliver the hybrid devices you need, when you need them, at a competitive price:

- Fairchild specializes in manufacturing semiconductor products. Since we manufacture all of the active components used in hybrids, we can more readily meet hybrid delivery schedules, and you can be sure that the hybrid circuit designed for you employs the most sophisticated products and design techniques.
- We have a broad selection of assembly and testing facilities designed specifically for high volume hybrid production.
- We have one of the largest hybrid manufacturing facilities in the world, with an equally large testing capacity.

Standard and Custom Products

Fairchild offers a broad selection of standard hybrid devices such as a high current, high frequency driver; high impedance, wideband DC amplifier; analog switch; etc. (the complete line of standard products is explained in detail in another section of this brochure, others will be announced as they are released).

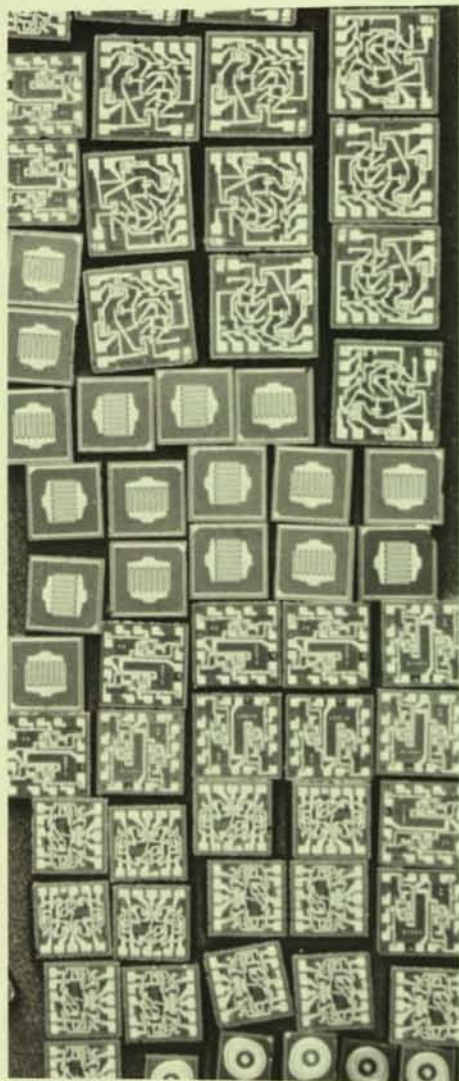
Possibly you have a variation of one of these devices, or you don't see the function you need. If this is the case, our custom products engineers can help analyze your requirements. In semiconductor devices such as hybrids, quality must be built in — it cannot be tested in. To show how we build in quality, a brief tour of our plant has been prepared for you in the following pages.



HOW HYBRIDS ARE MANUFACTURED

Dice Testing and Inspection

The most important building block of hybrids, the die, or chip, is first tested while still a part of the silicon wafer. A programmed tester automatically tests, and classifies each die, thus assuring required electrical tolerances. Each month, Fairchild's hybrid section tests over three million dice, and stores more than ten million in a nitrogen atmosphere ready for use on the assembly line.



Because Fairchild manufactures its own wafers, we can afford to select the most suitable dice for each product.

After testing, the wafer is scribed and broken into several hundred dice. The dice are sorted, cleaned, and visually inspected with a high power microscope by trained personnel.

Personnel Training

Personnel efficiency is an important feature of Fairchild hybrid production. Assembly line operators participate in a training program that explains the significance of specific production line duties in relation to the overall function of hybrid production.

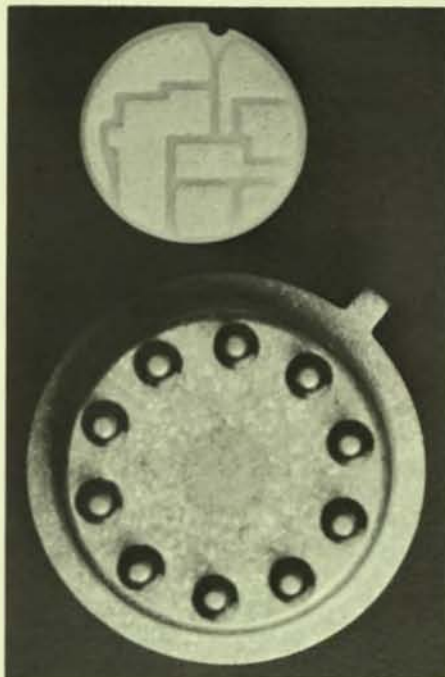
Under the direction of a training specialist, each operator trains for a specific duty such as inspecting dice for defects in masking, etching, scribing, or a phase of assembly, such as die attach or lead bonding.

Our Quality Assurance group requires that each operator performs her duties at 100% accuracy before joining the production line.



Substrate Preparation

Electrical connections with proper resistances are provided between each die in a hybrid with either a thick film or thin film conductor, printed directly on the substrate (a dielectric material to which the die is attached).



The amount of electrical resistance is determined by the cross section of the film connection. The thick film is fired onto the substrate with a resistance tolerance of 20%. Existing techniques permit testing and trimming to $\pm 1\%$ tolerance.

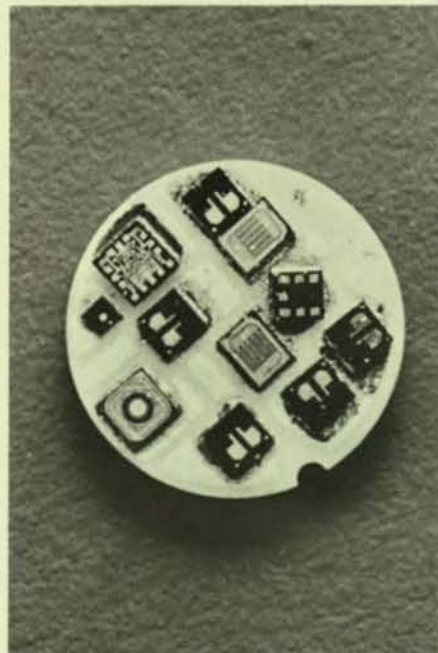
It is economically and technically significant to you, the hybrid buyer, that your manufacturer has the facilities for both thick and thin film substrate preparation. Most manufacturers handle only thick film which is less expensive to mass produce, but in some applications it is also less accurate.

In addition to handling both processes, Fairchild is one of the few manufacturers capable of combining both thick and thin film technologies in one package. This combination of production techniques allows the most reliable and economical method of hybrid assembly.

The Design Guide provides a summary of design possibilities with our thick and thin film applications.

Die Attach and Lead Bonding

After the thick or thin film interconnection pattern is prepared on the substrate, the dice are attached, and the leads bonded with the gold ball technique. In addition to gold ball bonding, we have an aluminum ultrasonic bonding capability primarily for radiation environments.



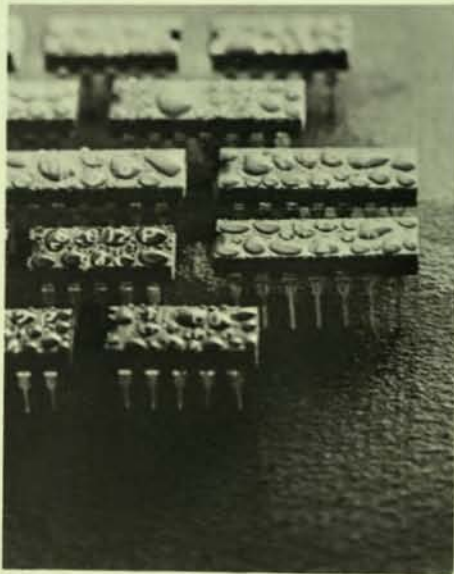
When the lead bonding functions are completed, the bonds are closely screened to ensure good workmanship. The package is then given a vacuum tight seal.

Testing

After the hybrid is sealed, it is subjected to a series of environmental and electrical tests before shipment to the customer. The nature and extent of these tests depend on customer specifications. Here are a few examples of environmental and electrical tests, all of which conform to military standards:

Environmental Tests

Gross and fine leak tests assure a vacuum tight seal. For gross leak testing the device is emersed in a clear, hot oil and inspected for escaping bubbles caused by gas expansion within the package. Fairchild's RADIFLO method checks for fine leaks up to a 10^{-8} torr.



Other available high reliability environmental tests assure electrical stability of the device after undergoing shock; vibration fatigue; variable frequency vibration; and centrifuge.

Electrical Tests

Most electrical testing is performed on the Fairchild Series 500 tester; or the fully automatic Series 4000M with special test adaptors.

The Series 500 tester performs small signal tests on transistors, diodes, and zener diodes. Capabilities include GO/NO-GO decisions, single or dual limit testing, programming and data logging, as well as high power and high sensitivity measurements.

The Series 4000M tester, with data logging capability, tests all major DC parameters; and a sample plan covers switching time tests providing up to 100 tests per second. Programming the 4000M tester with an "adding machine" type keyboard permits rapid programming flexibility usually found only in discrete device testers. Multiplexing a number of separate test stations and testing programs permits high volume production testing on a wide variety of devices. This combination of speed and flexibility makes Fairchild's hybrid testing operation unique in the industry.



The burn-in process, available as an option, is a combination of environmental and electrical testing which subjects the device to various thermal environments while it functions electrically for a specified length of time.

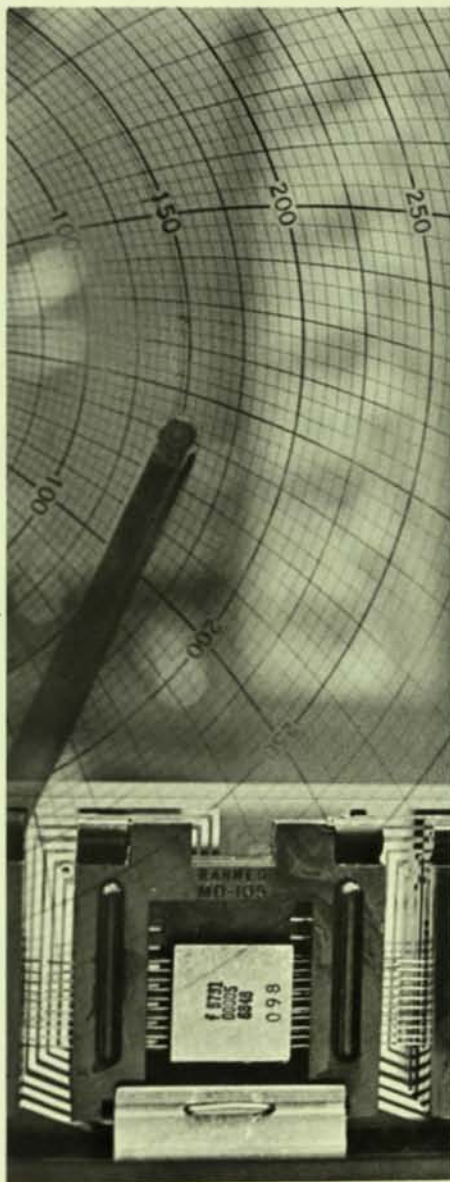
Fairchild's hybrid testing department is equipped to provide these and many other optional testing requirements.

When all environmental and electrical tests are completed, the device is given a 100% visual inspection; is classified, marked, and prepared for shipment.

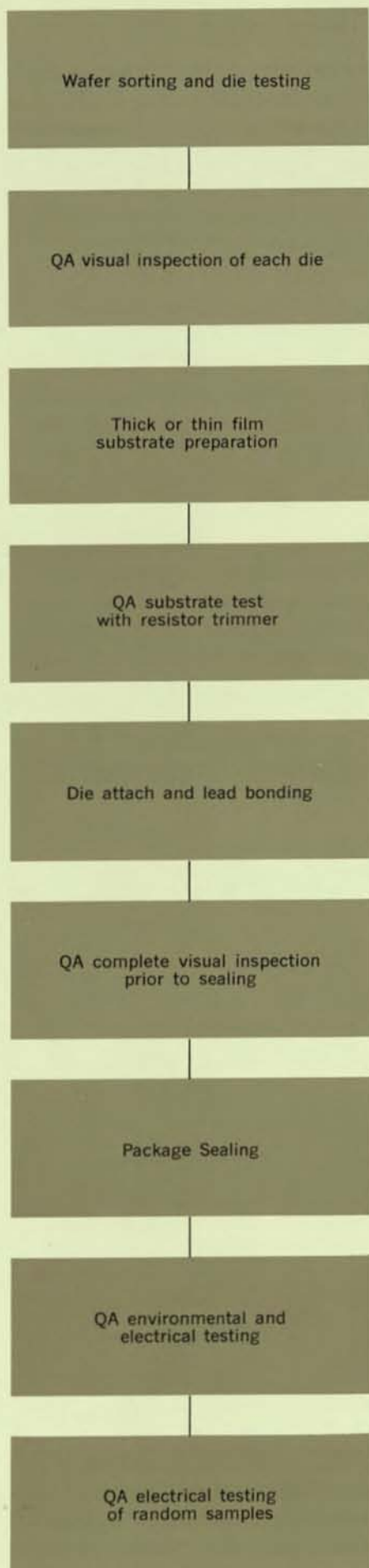
Quality Assurance Programs

From testing and selection of individual die until your manufactured hybrid devices are packed and ready to ship, the Quality Assurance Department ensures that the detailed requirements of your specifications are complied with.

Operating independently of production, QA establishes a system of tests and inspections that are an integral part of the production program.

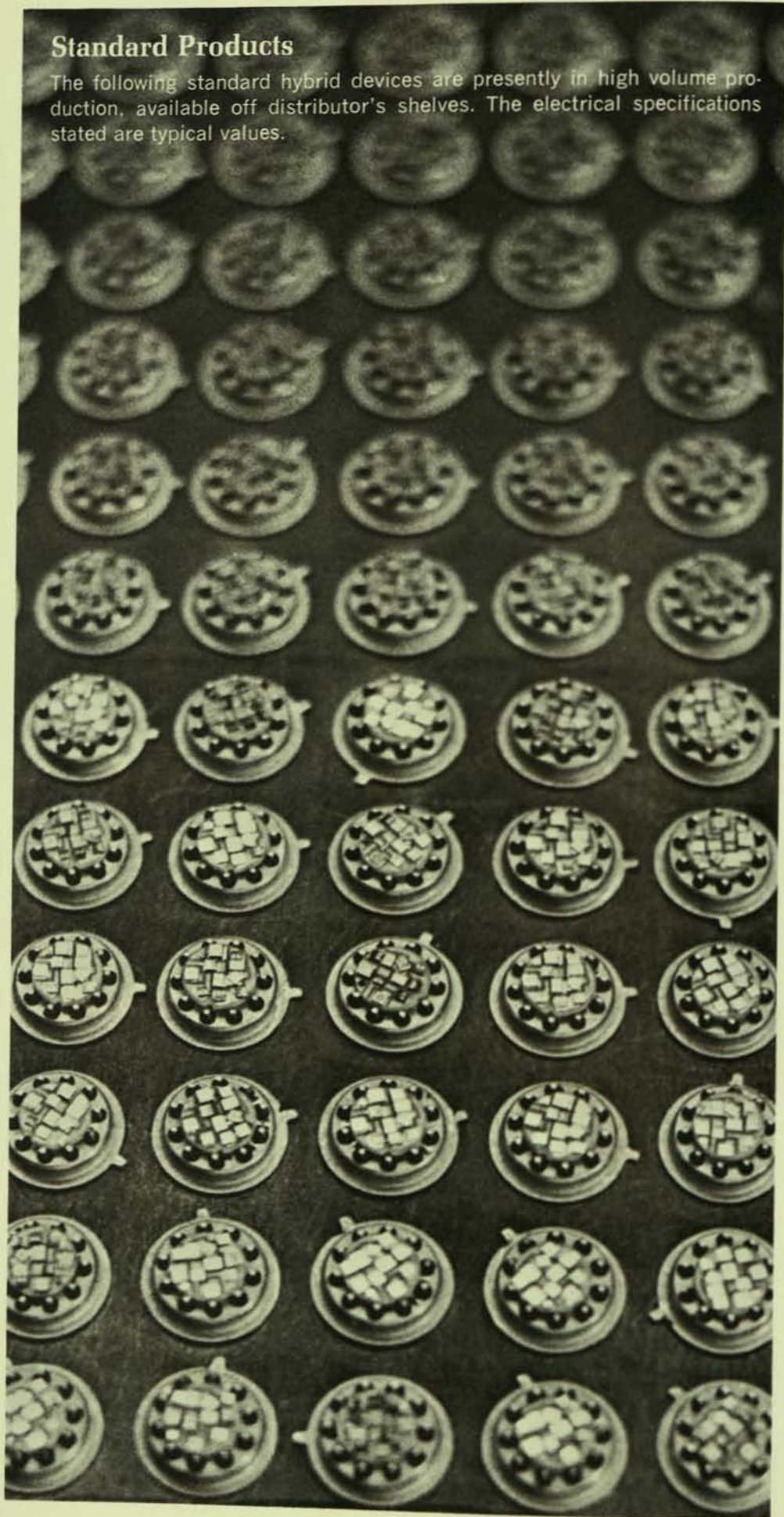


The following diagram summarizes the manufacturing process you've just reviewed and shows how QA tests and inspections are involved at every critical phase of manufacturing, assuring that reliability is built in to each device:



Standard Products

The following standard hybrid devices are presently in high volume production, available off distributor's shelves. The electrical specifications stated are typical values.



High-Voltage, High-Current Driver

SH2001

INPUTS CCSL COMPATIBLE
HIGH CURRENT CAPABILITY . . . 250 mA SINKING CURRENT AT 0.5 VOLT
HIGH VOLTAGE CAPABILITY . . . 40 VOLTS V_{CE0}
LOGIC FLEXIBILITY 4 INPUT NAND WITH INHIBIT (NOR) INPUT
HIGH SPEED $t_{on} = 70$ ns (TYP); $t_{off} = 110$ ns (TYP)

APPLICATION

Core, Cable and Lamp Driver

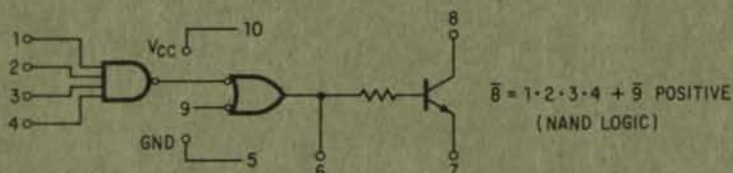
ABSOLUTE MAXIMUM RATINGS (25°C Free Air Temperature unless otherwise noted)

Voltage Applied to Pin 8	+40 Volts
Voltage Applied to Pin 10	8 Volts
Operating Power	800 mW
Storage Temperature	-65°C to +150°C
Input Reverse Current	1 mA
Current on Pin 8	1 Amp

STANDARD PACKAGES

TO-100
10 Lead Flat Pack

Logic Diagram



DTuL High Power Driver

SH2002

LOGIC FLEXIBILITY LATCHABLE 4 INPUT NAND WITH INHIBIT (NOR) INPUT
HIGH CURRENT CAPABILITY . . . UP TO 150 mA
HIGH VOLTAGE CAPABILITY . . . 40 VOLTS V_{CE0}
INPUTS CCSL COMPATIBLE
-55°C TO +125°C TEMPERATURE RANGE

APPLICATION

Core, Cable and Lamp Driver

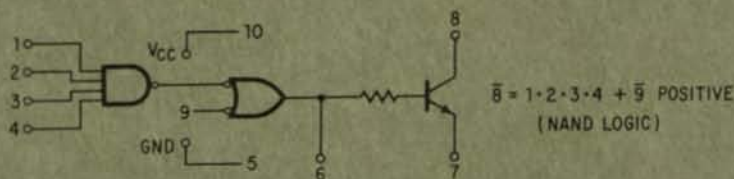
ABSOLUTE MAXIMUM RATINGS (25°C Free Air Temperature unless otherwise noted)

Voltage Applied to Pin 10 (continuous)	+8.0 Volts
Input Reverse Current	1.0 mA
Voltage Applied to Pin 8 (continuous)	+40 Volts
Voltage Applied to Pin 10 (pulsed ≤ 1 second)	+12 Volts
Storage Temperature	-65°C to +150°C
Power Dissipation (Derate Linearly to +175°C)	800 mW

STANDARD PACKAGES

TO-100
10 Lead Flat Pack

Logic Diagram



DTuL High Power Driver

SH2002-P

LOGIC FLEXIBILITY LATCHABLE 4 INPUT NAND WITH INHIBIT (NOR) INPUT
HIGH CURRENT CAPABILITY . . . UP TO 150 mA
HIGH VOLTAGE CAPABILITY . . . 40 VOLTS V_{CE0}
INPUTS CCSL COMPATIBLE

APPLICATION

Core, Cable and Lamp Driver

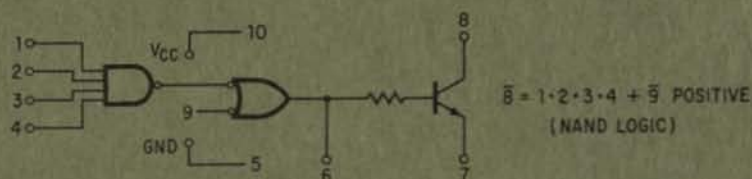
ABSOLUTE MAXIMUM RATINGS (25°C Free Air Temperature unless otherwise noted)

Voltage Applied to Pin 10 (continuous)	+8.0 Volts
Input Reverse Current	1.0 mA
Voltage Applied to Pin 8 (continuous)	+40 Volts
Voltage Applied to Pin 10 (pulsed ≤ 1 second)	+12 Volts
Storage Temperature	-65°C to +150°C
Operating Temperature	0°C to +70°C
Power Dissipation (Derate Linearly to +175°C)	800 mW

STANDARD PACKAGE

10 Lead Plastic DIP

Logic Diagram



Byte Parity Generator or Checker

SH2204

35 ns TYPICAL INPUT TO ODD PARITY DELAY
ALL INPUT DIODE CLAMPING
CCSL INTERFACING
HERMETIC PACKAGE
MULTIPLE MSI HYBRID

APPLICATIONS

Airborne Computers
Desk Top Calculators
High Speed Data Processing Equipment

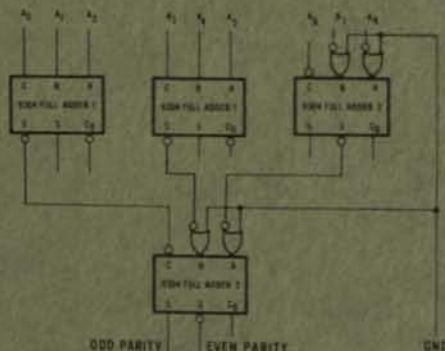
ABSOLUTE MAXIMUM RATINGS (25°C Free Air Temperature unless otherwise noted)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V_{CC} Pin Potential to Ground Pin	-.5V to +7V
Voltage applied to Outputs for High Output States	-.5V to V_{CC} value
Input Voltage	-.5V to 5.5V

STANDARD PACKAGE

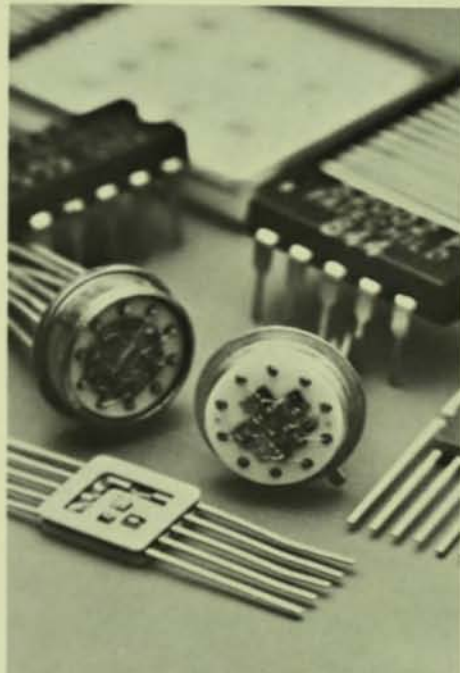
$\frac{3}{8}$ " x $\frac{3}{8}$ " 14 Lead Flat Pack

Logic Diagram



Custom Products

In the event that one of our standard hybrid devices doesn't fill your requirement, our custom products engineers can design the device you need, and have a prototype assembled on our Quick Reaction Line.



The QRL, a miniature version of our standard production line, is used to rapidly produce limited quantities of new hybrids. Following your request, you quickly receive a prototype of your design for evaluation.

The Fairchild engineers designing your custom device operate within the hybrid manufacturing plant, where they monitor the development of your product from the drawing board to delivery.

Custom hybrid devices at Fairchild typically fall into one of four categories:

- Interface circuits—typically combining one or more monolithic IC chips with high performance bipolar or MOS switching transistors.
- Linear devices — linear IC chips with associated passive components. In many cases, these also contain discrete transistor chips to improve on input or output characteristics.
- Multiple transistors in a compact package.
- Multiple digital IC chips.



A prototype of your custom device is promptly built and tested on our Quick Reaction Line.

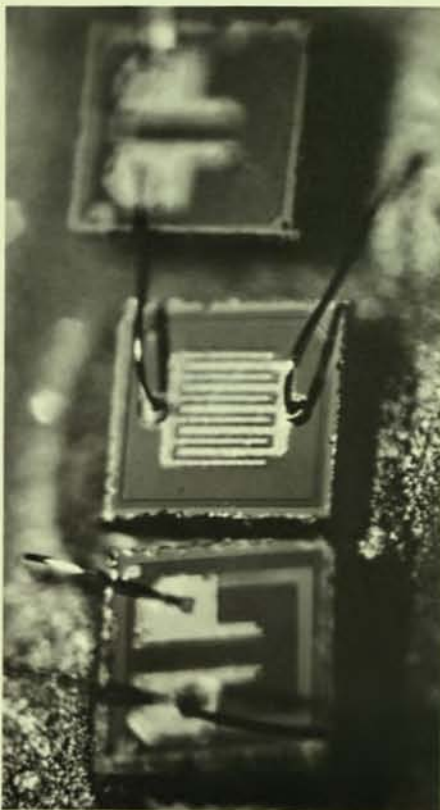
DESIGN GUIDE

This guide permits you to determine if your project is feasible with hybrid design. By doing the following preliminary work you can . . .

- Immediately determine if your circuit design is compatible with present hybrid packaging techniques.
- See if required close relationships between components in your circuit are compatible with hybrid design.
- Be prepared to efficiently discuss your circuit needs with a Fairchild engineer. This means a quick response to all of your questions.

Design Rules

1 The substrate (bottom of the die) of a transistor, diode, and capacitor die is connected directly to the package substrate (metallized pad). The metallized pad therefore acts as an electrical connection. You must perform a lead bond to the metallized pad if you wish to interconnect the die with another point in the circuit.



2 The thin film resistor chips are electrically isolated from the metallized pad. This permits multiple mounting on a single metallized pad.

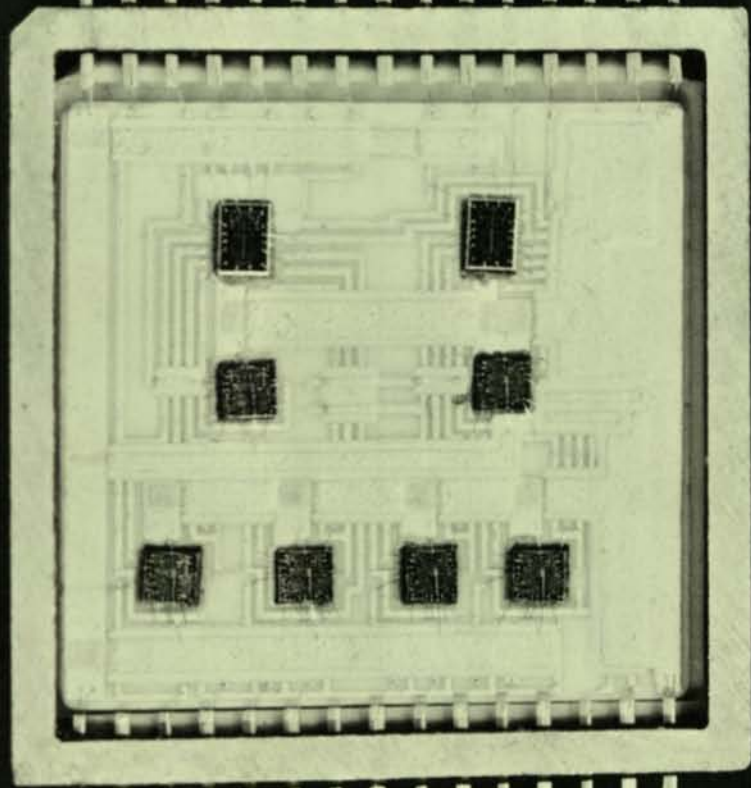
Layout Procedure

- 1 List all components of your circuit.
- 2 Use the reference table to list the approximate die size of each component.
- 3 Sum up the total space your dice will occupy. For most designs the total die area should be less than 20% of the space available to allow for interconnections. In some instances a total die area above 20% and as much as 50% of the space can be accommodated by special interconnecting techniques.
- 4 Compare your circuit's total power dissipation with the package dissipation listed on the reference table. Special heat sinking arrangements external to the package can handle power dissipation exceeding listed package limits.
- 5 Compare your number of circuit terminations to the available number of pins.



Package Layout Rules

- 1 In order to allow enough room for attaching a die to a pad, a minimum 5-mil space between adjacent dice are required.
- 2 It is preferable to leave a 10-mil space between adjacent dice on the metallized pad when it is necessary to bond a wire to the pad.
- 3 Crossing interconnecting leads over other leads is undesirable. Although the possibility of shorting is small, cross-overs are not consistent with good manufacturing processes.



Design Reference Table

COMPONENT	CHARACTERISTICS	DIE SIZE (in mils)*
Resistors—thick film	10 Ω /sq. to 1 M Ω /sq.	40 x 40 (approx. max. size of thick film resistor)
Resistors—thin film	10 Ω /sq. to 100 k Ω /sq.	30 x 30
Capacitors Ceramic	from 10 pF to 0.1 μ F	Maximum length - 80 Maximum width - 50
Thick Film	up to 1,000 pF	
Diodes		
FD100	BV > 80 V $t_{RR} < 4$ ns	20 x 20
FD200	BV \approx 150 V $I_F > 100$ mA @ 1 V	20 x 20
FD300	BV \approx 150 V $I_R < 1$ nA @ 125 V	25 x 25
FD600	BV = 80 V $t_{RR} < 4$ ns	20 x 20
FD700	BV = 25 V $t_{RR} < 700$ ps	20 x 20
Zeners	V _Z 6-200 V	20 x 20
Transistors (Typical 2N types.)		
NPN		
2N3725	High voltage, high current switch	30 x 30
2N2222	High speed switch	25 x 25
2N2484	Low level, low noise type	17.5 x 17.5
PNP		
2N2907	High speed switch and core driver	20 x 20
2N3251	High speed switch and RF amplifier	10 x 15
2N3962	Low level, low noise	15 x 30
LIC Circuits (Linear Integrated Circuits)		
700 Series		60 x 60
RTL Circuits (Resistor - Transistor Micrologic®)		
900 Series		40 x 40
DTL Circuits (Diode - Transistor Micrologic®)		
930 Series	CCSL compatible	40 x 40
TTL Transistor - Transistor Micrologic®)		
	CCSL compatible	50 x 50
MSI (Medium Scale Integration)		
	CCSL compatible	80 x 80
LSI (Large Scale Integration)		
	CCSL compatible	140 x 140
MOS Circuits (Metal Oxide Silicon)		
		80 x 80

*Sizes vary for individual members of each family. Contact a Fairchild representative for die sizes of specific devices.

Hybrid Component Capability

Generally speaking, every semiconductor device manufactured by Fairchild may be used in hybrid design. In addition however, passive components and packaging also play important roles in overall hybrid capability. The following is more specific information on Fairchild's current status in these areas.

Summary of Component Capability

THICK FILM

Resistors

Resistivity.....	10 Ω /sq. to 1 M Ω sq.
Temperature Coefficient between -55°C to 125°C:	< \pm 250 ppm/C°
or.....	< \pm 100 ppm/C° for some cases
Drift.....	< 1%/1000 hours at 150°C storage
or.....	< .1%/1000 hours at 125°C
Power Dissipation.....	25 to 50 w/sq. inch
Tolerance.....	Untrimmed \pm 20%
	Trimmed \pm 1.0% of desired value

Conductor, Gold

Resistivity.....	< .008 Ω /sq. inch
	3 mil lines with 3 mil spacing is available

Multi-layer metal (gold with glass ceramic dielectric)

K (dielectric constant) = <12

Capacitors

	screened 100K pF/sq. inch
	TCC = +400 ppm
	Temperature range 25°C to 100°C
Typical Values.....	100" x .100" = 1,000 pF
	.040 x .040 = 160 pF
Dissipation factor = 1% @ 1 kc	chip capacitors range from 10 pF to 0.1 μ F
	other values available depending on package.

THIN FILM

Resistors

	Nickel chrome deposited on oxidized silicon wafers or glazed ceramics. Passivated.
TCR.....	< \pm 50 ppm/°C
Range.....	10 Ω /sq. to 100 k Ω
Accuracy.....	Normally \pm 5% of target value and \pm 1% if required.
Drift.....	< 0.1% after 1000 hours under rated power.

Resistor Arrays

Resolution.....	In addition to above parameters tracking is available within 1%. Line width as narrow as 0.5 mil is available.
-----------------	--

Conductor, Aluminum

Resistivity.....	.004 Ω /sq.
Resolution.....	0.5 mil with 0.5 mil spaces
Uniformity.....	1% max. variation in resistivity.
Flip chip.....	Some DT μ L and TT μ L ICs and Discrete Devices are available in flip chip form.

NOTE: Aluminum conductors and aluminum ultrasonic bonding are acceptable in radiation environments.

Packaging

Fairchild hybrid circuits are available in a broad selection of packages.

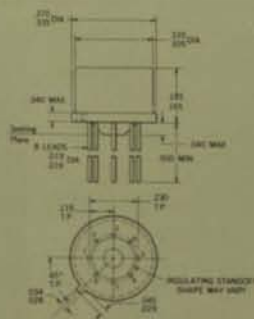
PACKAGE		NUMBER OF LEADS	INSERT SIZE	POWER DISSIPATION	
				#jc	#ja (in free air)
5T	TO-100	8	Disc: .200 Dia. (max.)		
AG	TO-100	10	Cog: .265 Dia. (max.)		
BW	TO-101	12			
BG	¼" x ¼" Flat Pack	10	.125 x .125	40°C/watt	200°C/watt
BH	¼" x ¼" Flat Pack	14	.125 x .125	40°C/watt	200°C/watt
BK	⅜" x ⅜" Flat Pack	14	.245 x .245	40°C/watt	125°C/watt
2A	⅝" x ⅝" Flat Pack	20	.465 x .495	30°C/watt	100°C/watt
2B	1" x 1" Flat Pack	30	.750 x .750	20°C/watt	60°C/watt
BY	0.8" x 1" Flat Pack	32	.550 x .825	20°C/watt	60°C/watt
6K	Hermetic DIP	14	.137 x .520	50°C/watt	175°C/watt
6R		16	.137 x .520	50°C/watt	175°C/watt
6F	Plastic DIP	10	.220 x .450	60°C/watt	175°C/watt
6Q		14	.220 x .650	60°C/watt	175°C/watt

Note the following two considerations concerning POWER DISSIPATION:

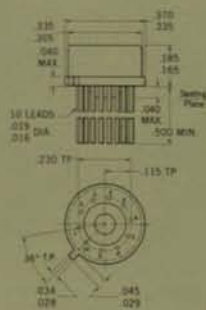
- #jc (Dissipation-junction to case) can vary at least 50% depending on the type of dice used and dice arrangement in the circuit.
- #ja (Dissipation-junction to ambient) can be substantially reduced through proper heat sinking. For example: #ja in our 1" x 1" or .8" x 1" packages can be reduced from 60°C/watt to about 20°C/watt.

Physical Dimensions

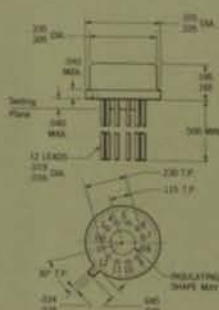
TO-100



TO-100



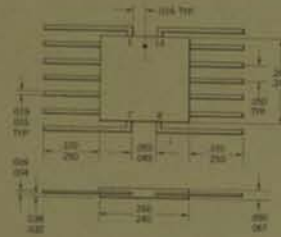
TO-101



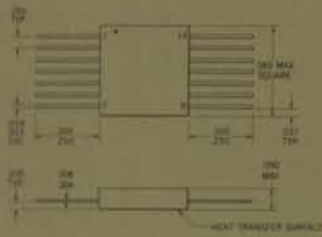
10 Lead Flat Pack



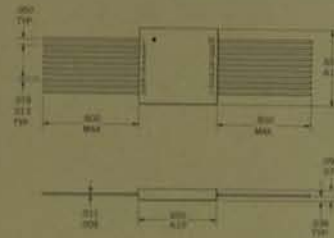
14 Lead 1/4" x 1/4" Flat Pack



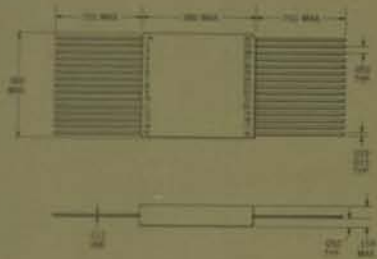
14 Lead 3/8" x 3/8" Flat Pack



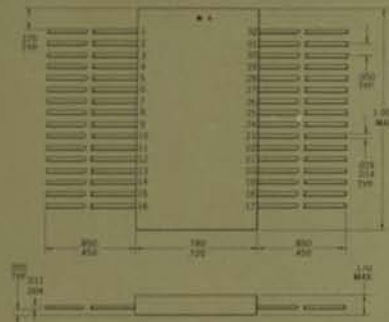
20 Lead 5/8" x 5/8" Flat Pack



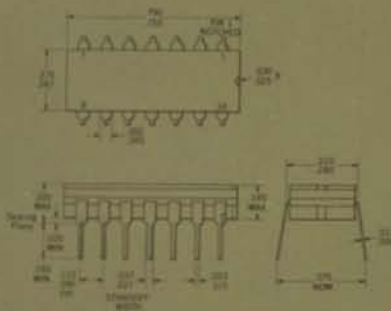
30 Lead 1" x 1" Flat Pack



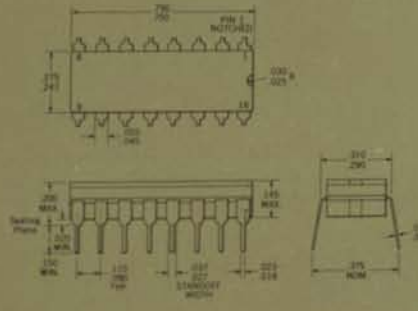
32 Lead 1" x 0.8" Flat Pack



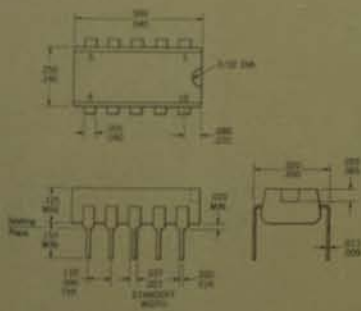
14 Lead Hermetic DIP



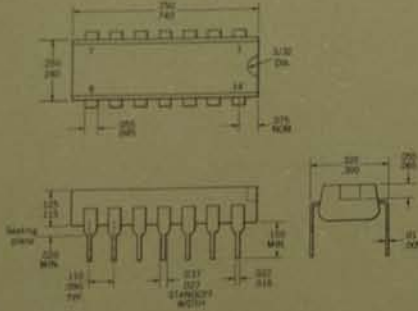
16 Lead Hermetic DIP



10 Lead Plastic DIP



14 Lead Plastic DIP



Gene Madley

650-327-~~4224~~4224

FAIRCHILD
SEMICONDUCTOR

*What
is a
Fairchild
Open
House?*

FA
SEN
FAIRCHILD

people



food



exhibits



prizes



balloons



brass band



families



clowns



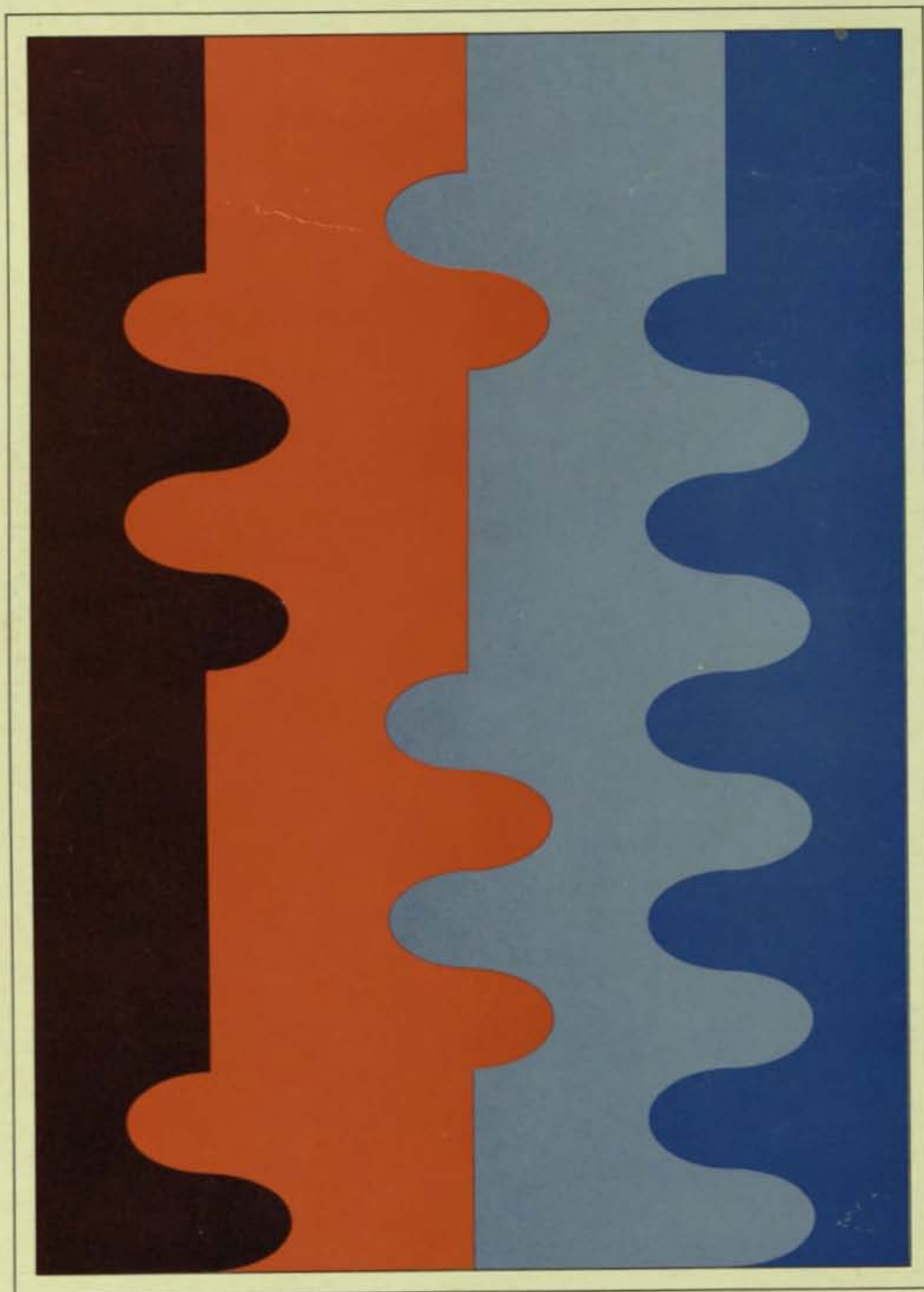
***...and the
result of
hard work
by quite
a few
unsung
heroes***



***What
is a
Fairchild
Open
House?***



Applications of the μ A742 TRIGAC
A Zero Crossing AC Trigger



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B.	A Note on Thyristor Structures	p. 28
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I. FOREWORD — USE OF THE HANDBOOK

The μ A742 TRIGAC supplies systems designers, circuit engineers, and experimenters with an integrated circuit that facilitates the design of zero crossing ON-OFF controls for a wide range of uses. Some examples are:

Industrial

- 1) conveyor belt drive motor ON-OFF control
- 2) oven or curing region temperature control
- 3) motor protection (current limit and winding temperature limit)
- 4) air conditioning (see Appliance)
- 5) process temperature-humidity control
- 6) plant safety fire detection
- 7) product proximity interlocks
- 8) product sorting
- 9) table positioning systems

Appliance

- 1) wall thermostat
- 2) fan controls responsive to air temperature flow
- 3) oven temperature controls for roasting, warming, self-cleaning functions
- 4) dehumidifier humidity detector
- 5) kitchen fan ON-OFF temperature control
- 6) portable heater temperature control
- 7) refrigerator
freezer cabinet temperature
refrigerator cabinet temperature
compressor motor overload protector
evaporator coil frost detector (for defrost cycle control)
start winding switch control
- 8) home laundry washing machine
water level detector
turbidity sensor
water temperature-mixing valve
out-of-balance detector
end-of-cycle annunciator
- 9) dishwasher
water temperature
water level
motor start-run winding control
motor winding temperature protector

- 10) room air conditioners and home heat pump installations
room temperature control
compressor motor start winding-overload protector
evaporator ice detector
defrost operation termination (temperature)
- 11) home safety fire detector
temperature responsive central alarm control
- 12) kitchen range surface burner temperature control (burner-with-a-brain and detecting boiling liquids)
- 13) outside ice detector
(automatic defrost of icy walks and gutters)

Aircraft

- 1) fan control
- 2) environmental control —heater and air conditioning equipment
- 3) servo motor control
- 4) engine temperature monitor and control
- 5) panel lighting

Marine

- 1) explosion proof ON-OFF control for hazardous environment (engine compartment, fuel storage areas, etc.)
- 2) environmental control
- 3) general low RFI/EMI motor control

The AC power control field has two major classifications for basic control systems: phase controls and zero crossing switches. (See Figures 1 and 2) The phase control changes the average load power applied by varying the point at which the power switch is turned ON. The top trace shows a small amount of power being delivered to the load; the lower trace shows almost full power being applied. Note the abrupt change in waveshape at the thyristor's turn-ON point. One of the major problems with phase control systems is suppression of RFI (Radio Frequency Interference) generated during this abrupt transition from the OFF to the ON state. The amount of unwanted high frequency energy generated is a function of the power being switched. Then the E-I product change will determine the RFI intensity produced. Just before switching,

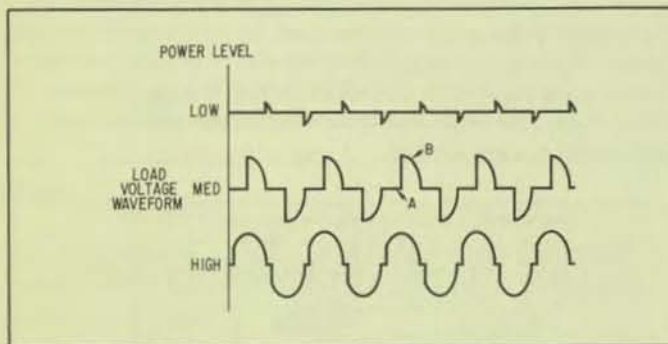


Fig. 1. Phase control.

the load current is zero, so the system power will also be zero. This is represented by position A in the diagram. However, just after the thyristor has turned ON, the system power condition is very high. In a 120 volt system, for instance, with a resistive load which dissipates 1200 watts average power, the instantaneous switched power may be as high as 1750 watts. This is represented at B in Figure 1. Generally, this transient must be suppressed by filter networks. These filters have one or more components in the main load current conduction path that introduce significant power dissipation. Filter systems are generally costly, bulky, and may cause problems with reflected asymmetries in the power distribution system.

The zero-crossing switch has none of these problems. Its typical operation is shown in Figure 2. Power is applied to the load by turning on the power switching thyristor when the line voltage (or current) crosses zero. With this approach, RFI is held to a minimum. (A direct inspection of the diagram shows

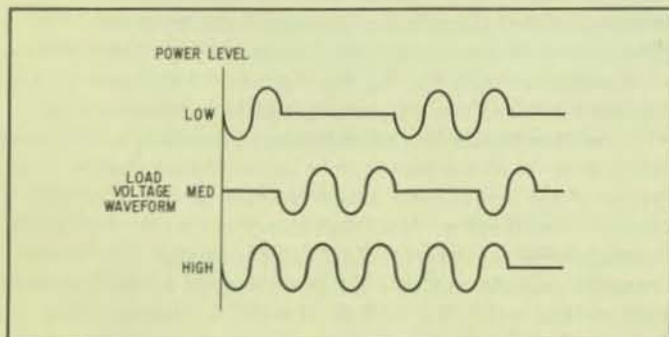


Fig. 2. Zero crossing control.

that there will be a minimum energy change in the 'before switch-ON' to 'after switch-ON' transition.) The upper trace in Figure 2 shows minimum power applied to the load; the lower trace, maximum power. Note that the power input is increased by discrete steps of full cycles. Designers interested in developing controls with a minimum time investment will find sufficient information for their purposes by briefly reviewing the Handbook's Introduction, checking the circuit given in the Applications section that most nearly resembles the need at hand, and choosing the proper load switch (SCR or triac) to match the system power requirement. The TRIGAC's inherent flexibility and ease of application should allow circuits to be designed in this manner for functions ranging from the simple single threshold coffee pot temperature control to the much more complex three-phase 24 kVA Y or Δ -connected two-level threshold control complete with time proportioning. In all cases, wiring complication is kept to a minimum because the TRIGAC has:

1. Its own internal power supply for operation with line voltages ranging from 24 to 440 volts (AC and DC).
2. Internal voltage stabilization for compensating large variations in supply source. (For instance, when connected for 110 VAC operation, the unit experiences practically no change in operation for line voltages ranging from 85 to 135 VAC).
3. Built-in bias supply for external sensors which tolerates most commonly used analog sources. (Inputs such as unidirectional phototransistors or bidirectional photoresistors, temperature sensors, pressure sensors, etc. are acceptable.)

For ease in locating various circuits, the Applications section is divided into four parts:

- A. One phase AC circuits (p.10).
- B. Accessory circuits (for expanded functional flexibility) (p.13).
- C. Three phase AC circuits (p.19).
- D. DC circuits. (p.20).
- E. Construction section (p.20).
Component locations, and parts lists.

Of course, there are many other potential applications for the μ A742.

II. INTRODUCTION

The $\mu A742$ TRIGAC is a flexible integrated circuit interface between an analog sensor and the gate terminal of a power switching thyristor (SCR or triac). Its location in a typical control system is shown in Figure 3.

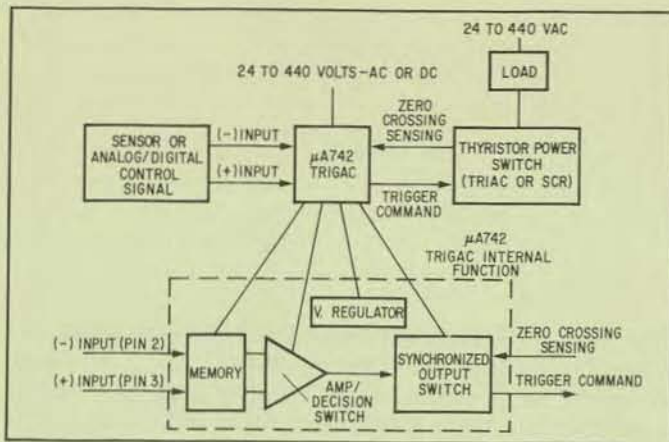


Fig. 3. Typical TRIGAC control system.

The TRIGAC is engineered to permit the maximum number of variations of this basic control configuration with the minimum number of external components.

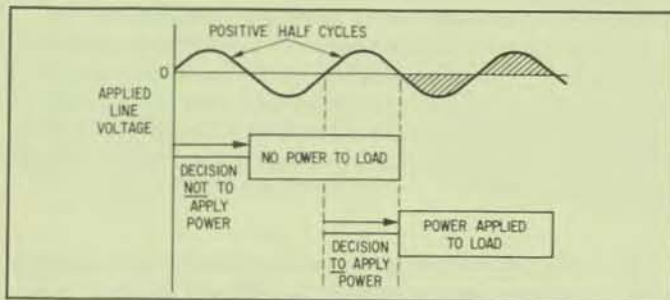


Fig. 4. Functional TRIGAC operating logic.

The TRIGAC's main function is to control the power applied to a load. In addition to this, other available functions add to its flexibility, such as:

1. Assured 360° load switching symmetry to avoid DC saturation of AC loads.
2. Zero crossing control to limit RFI/EMI (unwanted high frequency noise).
3. Predictable and stable critical operating 'set' points with well defined hysteresis.
4. The smallest possible number of external parts.
5. The use of sensors with widely varying characteristics:
 - a. resistance values ranging from $4k\Omega$ to $40k\Omega$
 - b. unidirectional types (e.g., photodiodes, phototransistors, etc.)
 - c. bidirectional types (e.g., NTC or PTC thermistors)
 - d. low power dissipation types (dissipation limited to 10 milliwatts for $10k\Omega$ sensors)
6. Switching for all loads ranging from resistive to inductive, with accommodation for time varying inductances. Capacitive loads may also be switched when a separate DC supply is available.

7. Transformer isolation from the power line.

The ON-OFF decision is made in the following manner:

Whenever the (+) input (pin 3) has a higher voltage than the (-) input (pin 2), a current pulse will be delivered to the gate of the power switch at the following two load current zero crossings.

This statement (represented in Figure 4) contains enough information to accurately predict the control's response to all combinations of sensor input signals.

Control transfer characteristics can easily be described in electromechanical (relay) terms. For instance, in the presence of a slowly rising input (coil) signal, a normally closed contact relay will reach a pickup voltage at which its armature will move from the unenergized to the energized condition. This will cause its normally closed contacts to open, and will result in the removal of power from the load. For higher values of applied signal at the relay coil, there will be no change in the load power. If the coil voltage is then lowered, a drop-out voltage is reached at some value below the pickup voltage. At this point, the armature returns to its unenergized position, and load power is again applied.

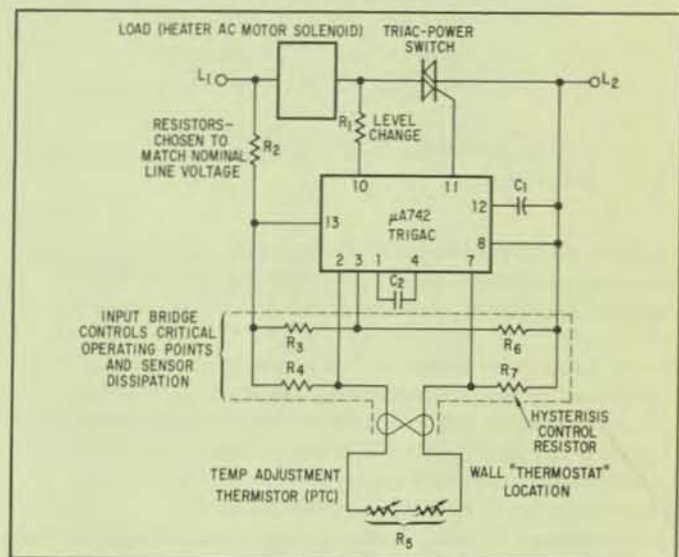


Fig. 5. Full-wave temperature control.

The transfer characteristic of the relay's operation is shown in Figure 6a. S_1 corresponds to the relay pickup point while S_2 describes the dropout condition. It should also be noted that the load has only two possible conditions, ON and OFF.

This also establishes the shape of the basic zero crossing hysteresis control characteristic. The signals needed for the TRIGAC's ON-OFF decision are supplied by the input bridge network which contains R_3 , R_4 , R_5 , R_6 , and R_7 in Figure 5. The R_5 element is in a 'remote' sensing location consisting of a PTC (Positive Temperature Coefficient) thermistor temperature sensor in series with a temperature adjust potentiometer. This branch of the input bridge would typically serve a 'wall thermostat' type function. Note that this circuit shows the sensor location as R_5 — between TRIGAC terminals 2 & 7, although it could as well be in any of the input bridge's other three arms (represented by R_3 , R_4 , or R_6). If an NTC (Negative Temperature Coefficient) thermistor had been chosen, R_6 would be the logical choice for the remote sensor position.

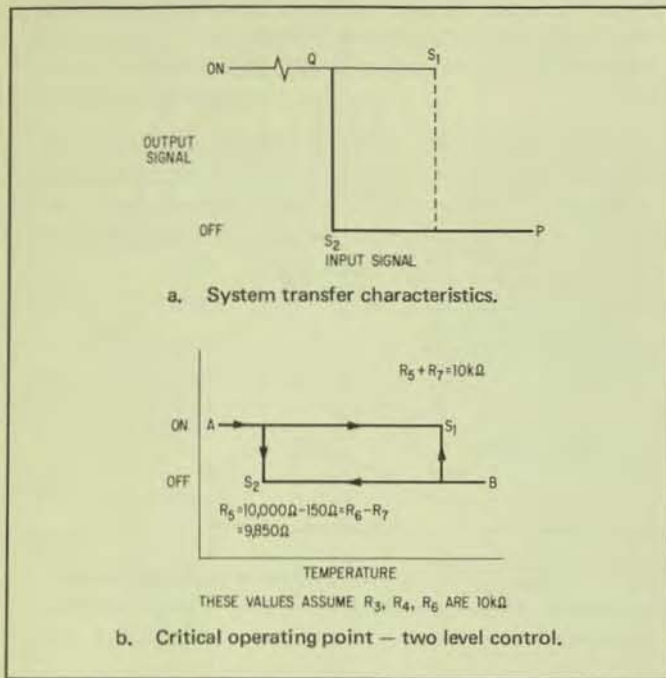


Fig. 6.

If we assume that each arm of the input bridge is approximately $10k\Omega$, then the critical operating points could be represented as shown in Figure 6b.

TRANSFER CHARACTERISTICS

A typical system operating cycle (assuming that the controlled load in this instance varies the temperature in the vicinity of the input sensor) is as follows:

1. With the PTC thermistor resistance (R_5) value low at low ambient temperature, we enter the Figure 6b diagram at point A. The thyristor power switch is held in the ON condition by the TRIGAC.
2. As the thermistor is warmed by the heater element, the resistance of R_5 is increased until the $R_5 + R_7$ branch of the input bridge rises above $10k\Omega$. At this point (S_1), gate drive is removed from the power switching triac, and the heater element (load) is turned OFF. The TRIGAC also shunts R_7 with a current path approximately equivalent to a 150Ω resistor.
3. After some thermal overshoot, the temperature at R_5 decreases until the value of its branch of the input bridge is again at $10k\Omega$ (including the 150Ω shunt at R_7). We have now reached point S_2 in Figure 6b, and the TRIGAC again applies gate signal to the power switch.
4. After thermal undershoot, R_5 will be re-warmed by the heater's output and the entire cycle will be repeated.

Note that:

1. The critical operating points — S_1 and S_2 — are completely controlled by the values of resistors R_5 and R_7 .
2. The turn OFF point for the system (S_1) is set by the sum $R_5 + R_7$.

3. The turn ON point for the system (S_2) is set by R_5 alone.
4. The difference between S_1 and S_2 (the control hysteresis) is set approximately by R_7 .

In Figure 5 and in the Applications section of this Handbook, each arm of the input bridge is shown to have a $10k\Omega$ resistance. Actually there is a great deal of freedom in choice of input components. The input bridge arms may be chosen with values ranging from $4k\Omega$ up to $40k\Omega$ with little change in system performance.

Resistors R_1 and R_2 are line voltage dropping elements. In combination with the TRIGAC's internal structure, they limit its terminal voltage to no more than 22 volts (a safe value for reliable IC operation). The total current requirement for the system is low so that only two-watt resistors are required for 110 VAC systems. The need for the remaining external components, C_1 and C_2 , is discussed in the explanation of the TRIGAC's internal circuit that follows.

THE $\mu A742$ CIRCUIT OUTLINE

The TRIGAC's principle of operation is explained in two parts:

1. A simplified description of the purposes of each functional block. (Figure 7)
2. Complete circuit description.

The circuit has three main sections: *power supply*, *input amplifier*, and a *two level synchronized output switch*.

The *power supply* consists of a shunt zener regulator D_2 . During time intervals in which the AC line is positive (L_1 positive with respect to L_2) this zener holds the maximum voltage at V_{CC} to within 21 volts of the system ground reference (L_2). During the line supply's negative half cycle, the voltage at V_{CC} collapses and the portion of the TRIGAC to the left of the zener (the input amplifier, etc.) is allowed to 'idle'. We can say that this part of the circuit operates on a 50% duty cycle, but that during each interval that the line applies over 21 volts (a period slightly less than 8.3 milliseconds), it operates as if it were being supplied from a normal DC source.

The *input amplifier* and its associated functions:

1. Amplifies the input signal.
2. Makes the decision on whether or not power will be applied to the gate of the power switch by turning ON an internal SCR whenever the (+) input is larger than the (-) input (thus defining the S_1 value shown in Figure 5).
3. Sets the width of the hysteresis characteristic (the distance between S_1 and S_2 in Figure 6) by shunting R_7 in the input bridge. Retains memory of the IC's operating condition from positive half cycle to positive half cycle.

The two input signals from the external bridge are fed through forward biased diodes D_7 and D_8 into the bases of transistors Q_1 and Q_2 . Whenever the (+) input exceeds the (-) input by more than a slight offset voltage (typically about 3 millivolts), gate 2 current is extracted from thyristor 1. When this gate signal is present, thyristor 1 switches ON, applying approximately 20 volts to resistors R_a and R_b . The resultant current through R_a charges C_1 , later used to supply gate drive for the power switch. At the same time, current through R_b turns on

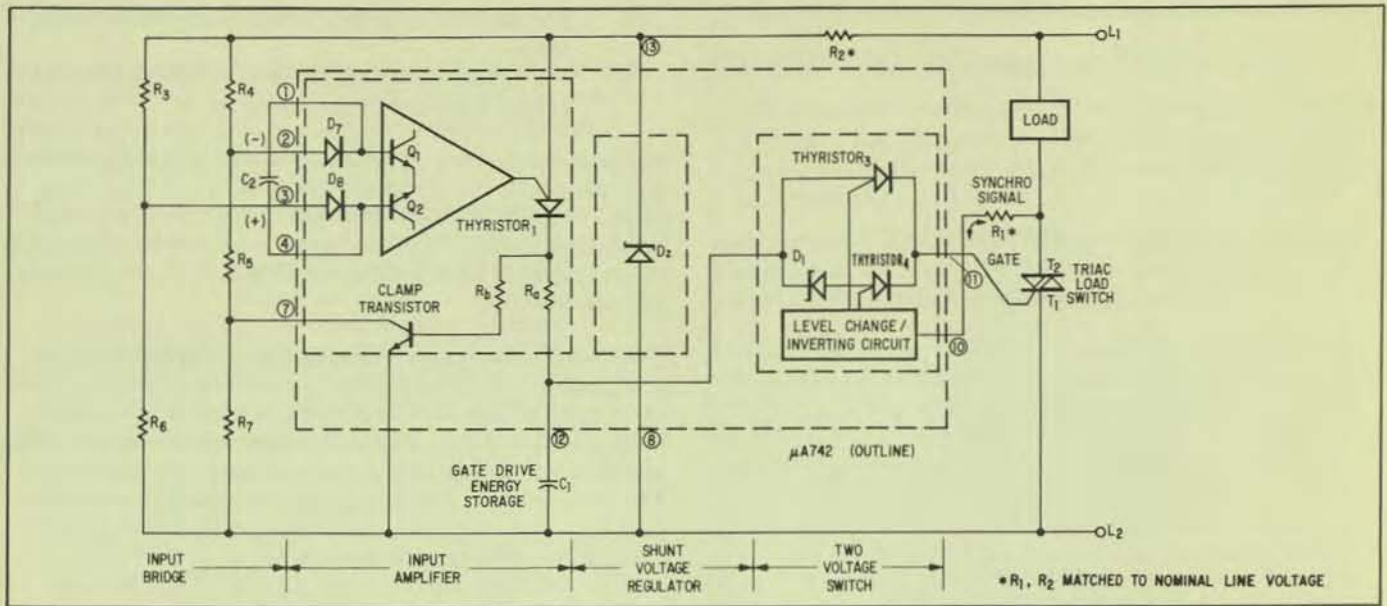


Fig. 7. Simplified TRIGAC internal schematic diagram.

the clamp transistor so that the voltage drop across external resistor R_7 is reduced to a single $V_{CE}(\text{sat})$. This has the effect of driving the (-) input further negative and widening the difference between the (+) and (-) inputs which, in turn, furnishes added gate drive for the switch.

The operation of the clamp, by shunting R_7 , also defines the change in input voltage level required to make the circuit return from the ON to the OFF stage.

The hysteresis transfer characteristic in Figure 5 explains the need for D_7 , D_8 , and C_2 . For input signals between the two critical operating points, S_1 and S_2 , the system may have either of the two possible output states, ON or OFF. For instance, if an input signal between S_1 and S_2 is applied for the first time, the system will assume the OFF state. However, if later changes in the input signal cause the system to turn ON, then it should continue to retain the ON condition for signals between S_1 and S_2 until the lower threshold point, S_2 , is reached. To do this, the circuit must have some form of memory. In conventional two-level circuits — such as the Schmitt trigger — a transistor held latched ON maintains a record from moment to moment of the system's previous state. Obviously, a continuous V_{CC} supply is needed to hold the latched transistor ON for this type of memory. The TRIGAC, with its periodically interrupted V_{CC} , must resort to a different form of memory.

Memory of the control's condition is kept during negative line half cycles (when the circuit is idling) by energy storage in capacitor C_2 . This stored energy forces the differential amplifier (Q_1 and Q_2) to assume the previously held state at the beginning of each positive half cycle. Diodes D_7 and D_8 prevent C_2 's stored voltage from discharging into the input bridge during 'idle' intervals.

The charge on C_2 is refreshed during each positive half cycle. C_2 also has a secondary function: it slows the amplifier frequency response to help eliminate false system noise turn ON. (Actually, system frequency response is set by the relatively slow 60Hz line.)

To summarize, the input amplifier has the job of delivering energy to C_1 whenever a gate signal is required for the external power switch. The decision on whether or not to supply this energy is made during each positive half cycle of the line. Once C_1 has been charged, the two level synchronized switch (covered next) will pass its stored energy to the gate of following SCR or triac within ten milliseconds.

The two level synchronized output switch transfers the C_1 charge into the external power switch gate during the two line current zero crossings immediately following the particular positive cycle in which C_1 was charged. To do this, two basic functions are required:

1. The energy must be parcelled out in two separate bursts; the first occurring when the load current crosses zero while traveling in the negative direction, and the second when the load current again crosses zero while traveling in the positive direction.
2. The amount of energy discharged from C_1 during both pulses must be accurately controlled so that the external power thyristor receives an adequate gate signal at each zero crossing.

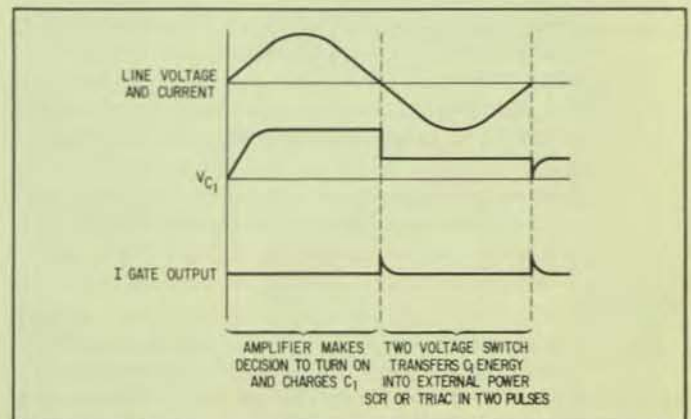


Fig. 8. Synchronized switch operation — resistive load.

These features are implemented through the use of thyristor 3, and thyristor 4, in Figure 7. The signal derived from the T_2 terminal of the power triac changes sign when the load current passes through zero.

A digression is in order here to explain the significance of using a signal derived from T_2 to sense information about the load current. The line/load waveforms for a typical AC inductive load switching condition are shown in Figure 9.

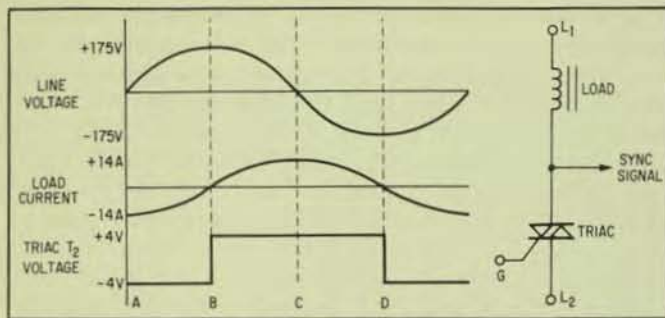


Fig. 9. TRIGAC zero crossing control — inductive load waveforms.

Beginning at the left edge of the illustration, assume that the thyristor in use is a triac and that it is already in conduction in the negative direction. When the load current passes through zero, the triac loses holding current and momentarily presents a high resistance to the series divider formed by the load and the thyristor. Since the load has a relatively low impedance, the remote thyristor terminal attempts to increase to line voltage. This produces a positive signal that is then coupled into the pulse generator via the synchronizing signal connection. The arrival of this signal causes the pulse generator to very rapidly deliver a pulse to the gate of the thyristor. The thyristor then resets into the ON condition for another half cycle.

The benefit of using this arrangement is obvious if we assume that the phase lag of the load current varies. (This is a situation frequently encountered in the case of motor loads. As the motor start winding is switched out, the phase lag of the motor can change by as much as 50 degrees.) If we assume that the position of the load current's zero crossing moves either forward or back in time, it is obvious that the synchronizing signal will also shift (the thyristor waits to fall out of latch until its current passes through zero). This will cause precisely the required change in the timing of the thyristor gate pulse to hold RFI generation to a minimum.

Returning to the discussion of the two level output switch's operation: The synchronizing signal from T_2 passes through R_1 and a level change inverting circuit (not shown on our simplified diagram) which extracts current from the gate 2 terminal of thyristor 4 just after the current zero crossing. This causes thyristor 1 to turn ON, discharging C_1 via zener diode D_1 , the anode-cathode circuit for thyristor 4 and the gate — T_1 circuit of the external triac power switch. C_1 is discharged until its voltage is too low to sustain current through thyristor 4 (which then falls out of latch because its anode current falls below I_{HO}). The level at which C_1 stops discharging — 8 volts — is held for the remaining negative half cycle of the load current (as shown in Figure 9).

When the load current next passes through zero (now traveling in the positive direction) the level change inverting circuit extracts current from gate 2 of thyristor 3. This unit (which does

not have a series zener) discharges C_1 into the thyristor gate via its anode-cathode circuit and the triac's gate — T_1 circuit. Thyristor 3 falls out of latch when C_1 's voltage has dropped to about 1 volt.

The energy delivered into the gate of the power switch (triac) has been controlled in both cases by the voltage change at C_1 .

At this point the line voltage becomes positive so that the input amplifier V_{CC} approaches 21 volts. If conditions at the TRIGAC's inputs (pins 2 and 3) dictate that thyristor 1 will again be turned on to charge C_1 , the entire cycle will be repeated for the following two load current zero crossings.

The sequence of events during the $\mu A742$'s operation generates the waveforms given in Figure 10.

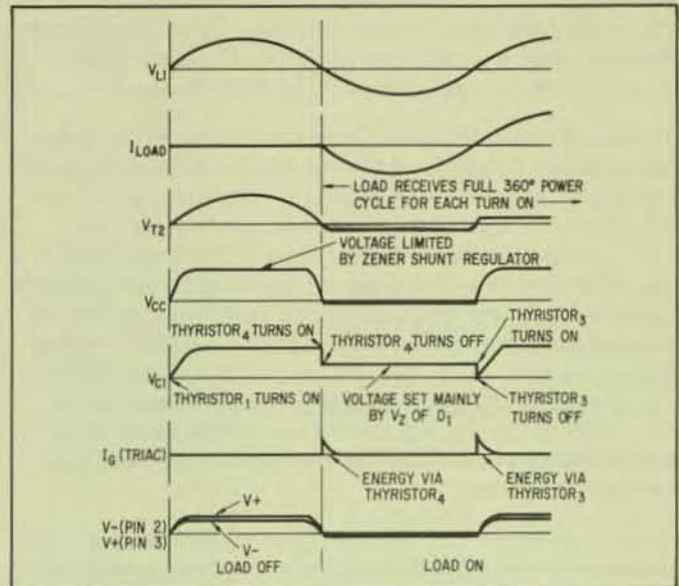


Fig. 10. Operation of the gate output switch — resistive load.

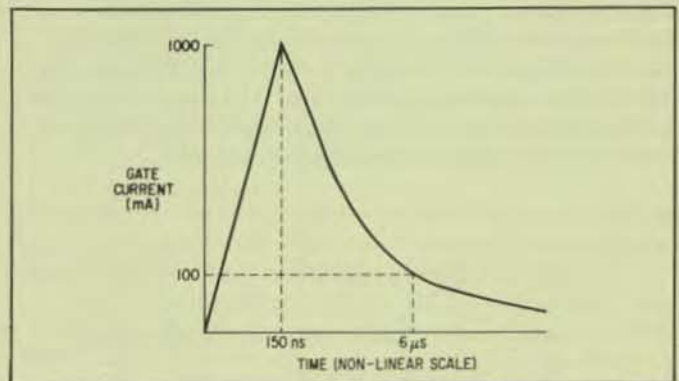


Fig. 11. TRIGAC output waveform.

Now for a look at the circuit's signal output. The TRIGAC produces a nearly ideal gate drive for power switching thyristors. When attached to the recommended external components, its waveshape (shown in Figure 11) has a rise time of about 150ns to a peak value of 1 ampere. The rate of decay is held so that there will be least 100mA available after 6 microseconds. If necessary, this interval may be stretched through alteration of the external components.

This completes the simplified discussion of the TRIGAC's operation.

III. TRIGAC COMPLETE CIRCUIT DESCRIPTION

OPERATION FROM AN AC SUPPLY

The schematic diagram of Figure 12 shows the connections for a TRIGAC control circuit operating directly from a single AC supply. It shows the necessary external components as well as the various sections within the TRIGAC. When operated directly from an AC line through a dropping resistor, zener diodes D₂, D₃, D₄, and diodes D₅, D₆ in the Power Supply Section provide a regulated supply of about +21 volts at pin 13 during the positive half cycles. During the negative half cycles, the isolation diode D₁, holds this potential to about -0.7V.

The Charge Control Section contains a conventional differential amplifier comprised of a matched pair of transistors Q₁, Q₂, and fed via a constant current source Q₃. Q₃ begins to conduct only after the supply voltage at pin 13 has exceeded about 14 volts, or when diodes D₃ through D₆ conduct.

The inputs of the differential amplifier are connected to the Sensor Bridge Network. If the input to the differential amplifier is such that the voltage at pin 2 (- input) is higher than that at pin 3 (+ input), Q₁ will conduct and thus hold Q₂ OFF. Let us call this the "inhibit state". When the input to the differential amplifier is positive (pin 3 at a higher potential than pin 2), Q₂ will conduct, and will pull current out of the anode-gate of thyristor T₁ in the Charging Network, causing T₁ to start conducting. We will call this the "trigger state". As soon as T₁ conducts, it will cause the storage capacitor C_{ST} to charge via T₁, D₉, and R₅ to a voltage equal to the supply voltage of pin 13 minus the drop across T₁ and D₉; roughly 19.5 volts.

Transistors Q₆ and Q₇, thyristor T₅ and their associated components form the Zero Crossing Detector. They provide the necessary control to ensure that trigger output pulses supplied to the external circuit are delivered near the zero crossing of the load current in order to minimize the RFI generated. The trigger pulses are supplied through the Pulse Generator which receives its energy from the external storage capacitor C_{ST}. The Pulse Generator is made of transistor Q₈, thyristors T₃, T₄, and their associated components. The Zero Crossing Detector and the Pulse Generator work together and therefore, their functions will be explained simultaneously.

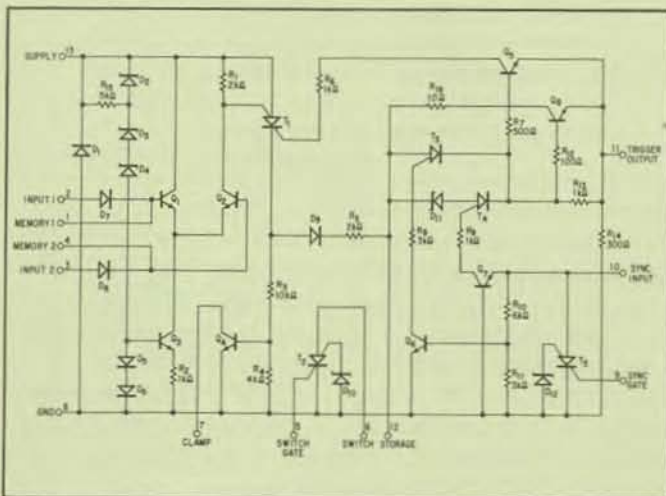


Fig. 12. μ A742 zero crossing AC trigger - TRIGAC schematic diagram.

Early during positive half cycles, before the triac anode voltage has reached about 7 volts, Q₆ is forward-biased via resistors R₅ and R₁₀. When the anode voltage of the triac exceeds the zener voltage of D₁₂ (about 7 volts), T₅ switches ON and causes the sync input voltage at pin 10 to collapse to about 1 volt, thus turning Q₆ OFF. This ensures that if T₃ is to turn ON, it will do so within the first seven or so volts of the positive half cycles. It will be recalled from the above explanation that C_{ST} begins to charge only after diodes D₃ through D₆ have started conducting, or roughly when the supply voltage at pin 13 has reached about 14 volts. It is therefore obvious that the charging and discharging of the storage capacitor occur at two distinct times. During the first positive half cycle, coinciding with, or immediately following the start of conduction of Q₂, current will flow out of the anode gate of T₃ within the first 7 volts of the positive half-cycle, but will not turn T₃ ON due to the absence of voltage on the storage capacitor C_{ST}. A little later during the same positive half cycle when the supply voltage at pin 13 has reached about 14 volts, the storage capacitor will begin to charge; its voltage will rise to about 19.5 volts during the remainder of the half cycle and will retain this value.

At the start of the following negative half cycle, Q₇ begins to conduct and it causes T₄ to turn ON due to the current pulled out of the anode-gate of T₄. T₄ provides the base drive to Q₅ and Q₈. Thus Q₈ turns ON and dumps some of the energy stored in C_{ST} and provides a high energy pulse to the gate of the triac, thus causing the triac to turn ON near the beginning of the negative half cycle. As soon as the voltage across C_{ST} falls to about 8 volts (because of D₁₁), the current through T₄ falls below its holding current level and thus T₄ and Q₈ are turned OFF. The storage capacitor therefore discharges from 19.5 volts to about 8 volts at the beginning of the negative half cycle. C_{ST} maintains this voltage for the remainder of the negative half cycle. At the start of the following positive half cycle, Q₆ is forward-biased again, and T₃ and Q₈ conduct. The storage capacitor C_{ST} now discharges to about 1 volt through R₁₆ and Q₈. Once the current through T₃ falls below its holding current level, T₃ turns OFF. The high energy pulse so generated triggers the triac ON near the start of the positive half cycle. As soon as the voltage across the triac collapses, base drive of Q₆, and consequently, the current out of the anode-gate of T₃, is stopped. When Q₅ comes out of saturation, Q₂ causes T₁ to turn ON again. The storage capacitor charges up and thus the cycle continues until the device reverts to the inhibit state.

OPERATION FROM A DC SUPPLY

The connection diagram for DC operation is given in Figure 13. There are some similarities as well as marked differences between DC and AC operations. In the DC operation mode, the constant supply voltage keeps the differential amplifier always in operation. Therefore, regardless of the instantaneous polarity of the AC line, the storage capacitor C_{ST} starts charging as soon as T₁ is triggered ON by Q₂. Let us now examine the transition from the inhibit state occurring during a positive half cycle of the AC supply. At the beginning of the next negative half cycle, Q₇ will be forward-biased and just as it was in the AC operation mode, T₄ will turn ON, forward-biasing Q₈ and Q₅. Q₈ produces an output trigger pulse at the beginning of this half cycle while Q₅ pulls current out of the

cathode gate of T_1 causing it to turn OFF. Note that in the AC mode of operation, T_1 turns OFF at the end of each positive half cycle, by the natural reversal of the line voltage. In this mode, since the TRIGAC is powered through a DC supply and Q_2 is assumed conducting, T_1 turns ON again as soon as Q_5 turns OFF, and re-charges C_{ST} back up to about 19.5 volts. With the next half cycle (positive) Q_6 is forward-biased and similarly a trigger output pulse is delivered to the triac; Q_5 pulls current out of the cathode gate of T_1 , turning it OFF. This time C_{ST} discharges to about 1 volt. However, when Q_2 turns T_1 ON again, C_{ST} recharges back up to about 19.5 volts and thus the cycle continues.

Now assume that the transition from the inhibit to trigger state takes place during a negative half cycle of the AC line. At the beginning of the next half cycle, Q_6 will be forward-biased and this time T_3 will turn ON first, forward-biasing Q_8 and Q_5 . The triac will, therefore, conduct initially at the start of a positive half cycle. The rest of the operation is similar to the description given above. When the input to the differential amplifier reverts back to the inhibit state, the TRIGAC will stop delivering output pulses. The triac will then start blocking, always beginning with a negative half cycle.

HYSTERESIS AND TIME PROPORTIONING OPERATION

So far, the function of the hysteresis transistor Q_4 and memory capacitor C_{MEM} have been deliberately omitted. However, as can be seen in Figure 12, every time T_1 is turned ON, Q_4 saturates due to the bias it receives through R_3 . In the meantime, C_{MEM} charges up according to the input conditions at pins 2 and 3. When Q_4 saturates, it shunts the hysteresis resistor R_{HYS} causing Q_2 to turn ON harder, thus supplying positive feedback to the differential amplifier. The memory capacitor then adjusts its charge according to this new input and "remembers" it for the next cycle. The transfer characteristic of this mode of operation is given in Figure 14. Note that if the connection from pin 7 to the bridge input is omitted, points S_1 and S_2 would coincide.

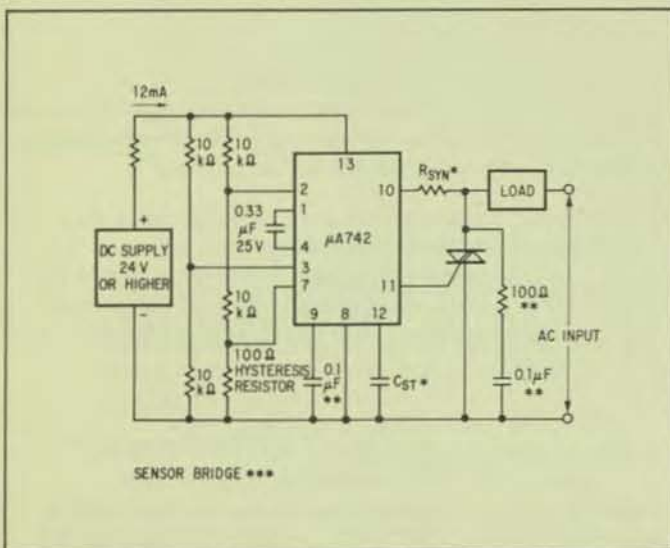


Fig. 13. Zero crossing circuit with DC supply.

Proportional control, another feature available with the TRIGAC, is shown in Figure 15. This function is achieved by

using thyristor T_2 to develop a ramp function which is superimposed upon the bridge input signal through the 200k resistor. Once the voltage on pin 6 reaches about 7 volts, T_2 switches into conduction and lowers the input voltage to pin 3, causing Q_2 to turn OFF. As the ramp voltage on pin 6 starts to increase again, the input to pin 3 also increases. The level on the ramp at which Q_2 conducts determines how long the load remains energized.

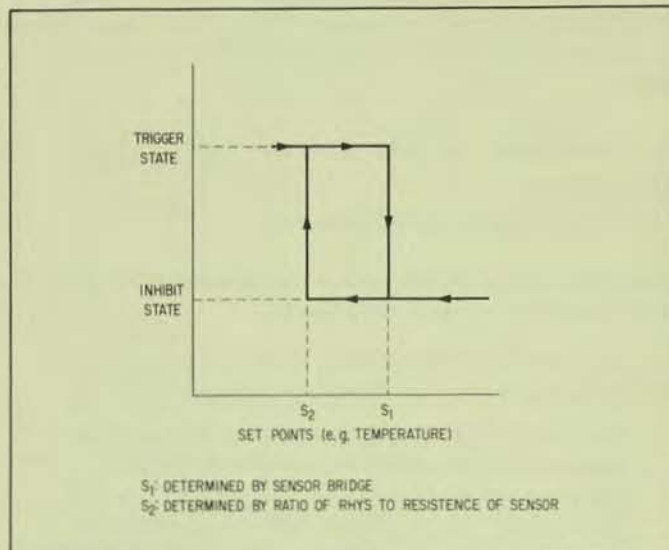


Fig. 14. Transfer characteristic of hysteresis control operation.

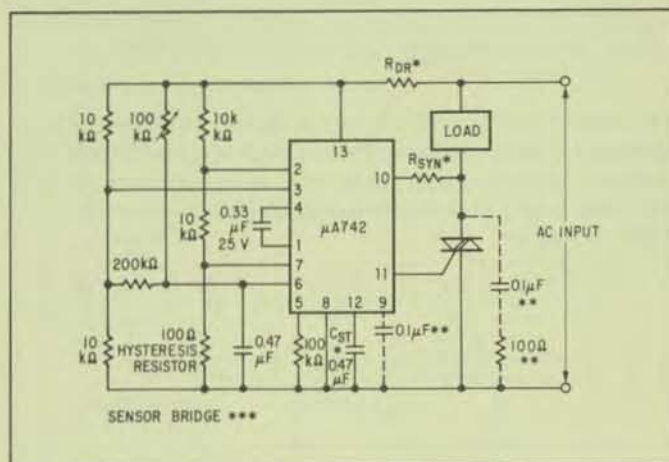


Fig. 15. Zero crossing with proportional control.

Recommended Values*

AC Supply Voltage 60Hz Volts - RMS	R_{DR}	R_{SYN}	C_{ST}
24	1.0kΩ	1.0kΩ	0.47μF/25V
110	10kΩ	10kΩ	0.47μF/25V
220	22kΩ	22kΩ	0.47μF/25V

FOR SUPPLY VOLTAGE FREQUENCY OF 400Hz REDUCE C_{ST} TO .047μF/25V

** Necessary with inductive loads.

*** The sensor resistance will determine the values of the bridge resistors. For the values of R_{DR} shown, the total current into the bridge should not exceed 5mA at 20V.

IV. APPLICATIONS

The following applications are a sampling of a few of the many TRIGAC uses. Each has an associated circuit board layout, parts list, and sufficient information for modeling the most common operating situations. The printed circuit board layouts, and parts lists appear in the Construction section.

The use of PC boards in testing TRIGAC circuits is encouraged — particularly if voltages higher than 24 VAC are to be used. When hooking up test systems with higher line voltages, the use of isolation transformers is recommended in the interest of safety.

A. ONE PHASE AC CIRCUITS (APP. 1-4)

APPLICATION 1

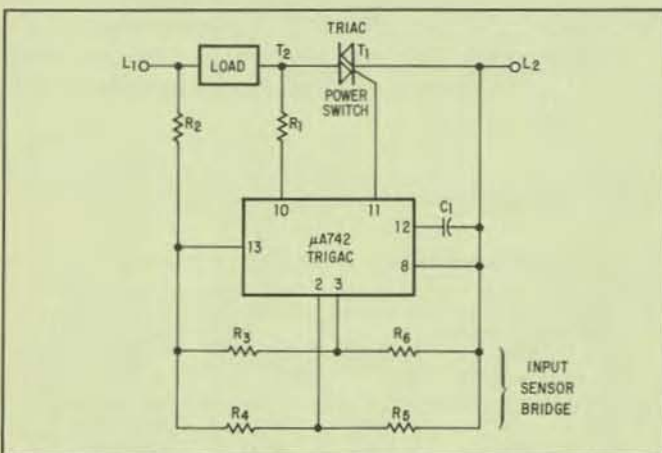
1Φ, 110 VAC Single Threshold Control

This form of the TRIGAC control circuit requires the minimum number of external components.

Circuit operation will be explained in the context of a simple low cost temperature controller (a common application).

Assume that the input sensor is a PTC (Positive Temperature Coefficient) thermistor with an operating point resistance of about 5kΩ. Further, assume that it is in series with a potentiometer (temperature adjust pot) set at a value near 5kΩ. The value of R₅ is then approximately 10kΩ (5kΩ + 5kΩ). Then temperatures holding R₅ below this value result in (+) input high or ON condition. Temperatures holding R₅ above this value provides for an OFF condition. (See Section II)

The circuit's operation is not limited to temperature control — the input sensor could as easily be a photodiode, photoresistor, pressure transducer, moisture sensor, water level detector, or any other analog sensor with resistance values ranging from 200Ω to 40kΩ.



Application 1. 1Φ, 110 VAC single threshold controller.

For applications with bridge arm resistance values differing from 10k, the important factor to keep in mind is the relationship:

$$\frac{R_3}{R_6} < \frac{R_4}{R_5}$$

Note that one of these resistors would usually be a sensor in series with an adjustment potentiometer. Whenever the left hand term of this equation is larger than the right, the external power switch will receive a zero crossing gate drive from the TRIGAC. If the right hand term is larger, then no gate drive is supplied to the power switch. In practice, there will be a very small undefined area when the two input signals (pin 2 and 3) are within a few millivolts of each other.

In this case:

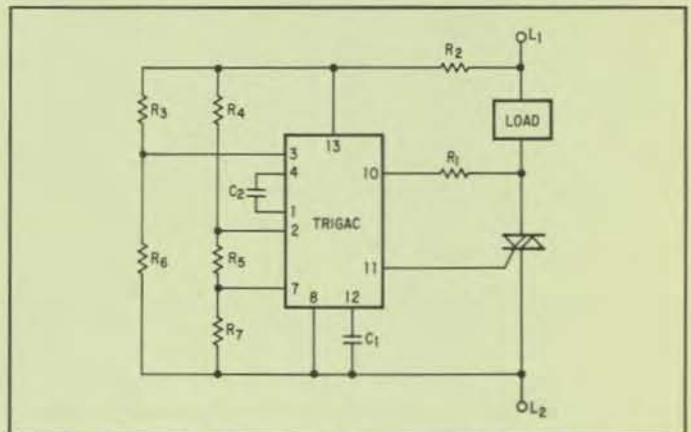
$$V_{CC} \left[\frac{R_3}{R_3 + R_6} - \frac{R_4}{R_4 + R_5} \right] > 3 \text{ millivolts} \text{ where } V_{CC} = 21V$$

For most controls, this undefined region is too small to be significant.

APPLICATION 2

Single Phase, 110 VAC Dual Threshold Control (With Hysteresis)

The transfer characteristic, a square loop, with dual threshold "critical operating points", has been described by example in the Introduction and illustrated in Figure 6. In this case the input sensor values for both thresholds is set by the input bridge resistance values. The transition from the OFF to the ON states is determined by the relative values of R₃, R₄, R₅, R₆, and R₇ as discussed in Figure 5 of the Introduction.



Application 2. 1Φ, 110 volt dual threshold controller.

1. Transition from OFF to ON:

In this situation, the clamp transistor of Figure 7 is OFF, and the input bridge is a simple four-armed configuration with this relationship for bridge balance:

$$\frac{R_3}{R_6} \geq \frac{R_4}{R_5 + R_7} \text{ Condition for turn ON}$$

When the bridge is unbalanced so that the left hand term is larger than the right, the TRIGAC will supply power to the gate of the power switch (triac or SCR).

When turn ON takes place, the input bridge will be unbalanced by an amount equal to the effect of replacing R₇ with a V_{CE} voltage drop.

2. *Transition from ON to OFF:*

Representing the effect of the clamp transistor in the circuit under consideration by inserting an equivalent resistor, $R7^*$ to replace $R7$:

$$R7^* = \frac{(R4 + R5)}{\frac{V_{CC}}{V_{CE(sat)}} - 1}$$

This assumes that:

- Input bias current can be ignored.
- The circuit's offset voltage is zero.
- The TRIGAC's internal (V_{CC}) is 21 volts.
- The clamp saturation voltage is $V_{CE(sat)}$.
- The value of $R7$ is large compared to $R7^*$.

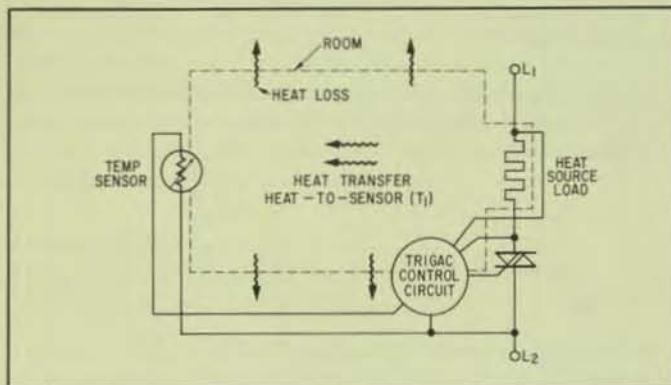
The condition for turn OFF now becomes:

$$\frac{R3}{R6} < \frac{R4}{R5 + R7^*}$$

APPLICATION 3

1 Φ , 110 VAC Dual Threshold Control with Time Proportioning

The need for time proportioning (or for the ability to smoothly control the load power) can be appreciated if we consider the interaction between a control and the environment it controls. For instance, an example of a room temperature controller is seen in Application 3a.

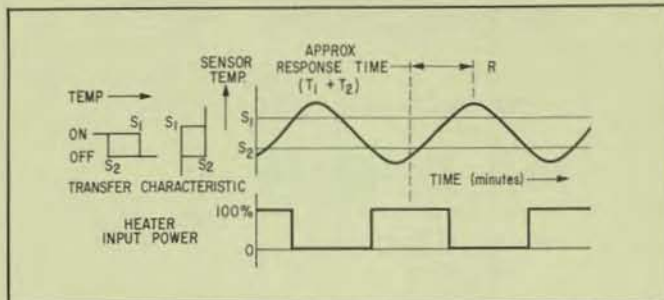


Application 3a.

There are a number of time related factors associated with this layout. If we list them in approximate order of importance:

- T₁ The primary path heat convection propagation time. (Period required for a step change in heat output at the heater element to change the temperature in the vicinity of the sensor.) Typically more than 2 minutes.
- T₂ Response time for the temperature sensor to react to a step change in its ambient. (15 - 45 seconds)
- T₃ Lumped summary of other effects — including: disturbances due to room air movement, boundary layer effects at the surface of the heater and the sensor secondary convection routes, changes in room heat loss due to external variations (outside temp, etc.).

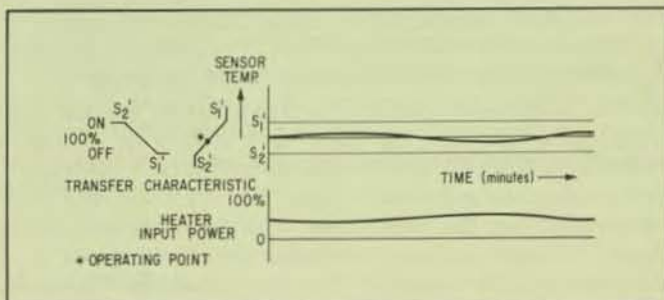
T_1 and T_2 are the dominant factors. A moment's reflection on the effect of the time delay between application of power to the heater and the responding resistance change in the thermistor sensor leads to the conclusion that the room's temperature must oscillate if power is applied in slowly cycling blocks of either full power or no power at all. This is illustrated in Application 3b.



Application 3b.

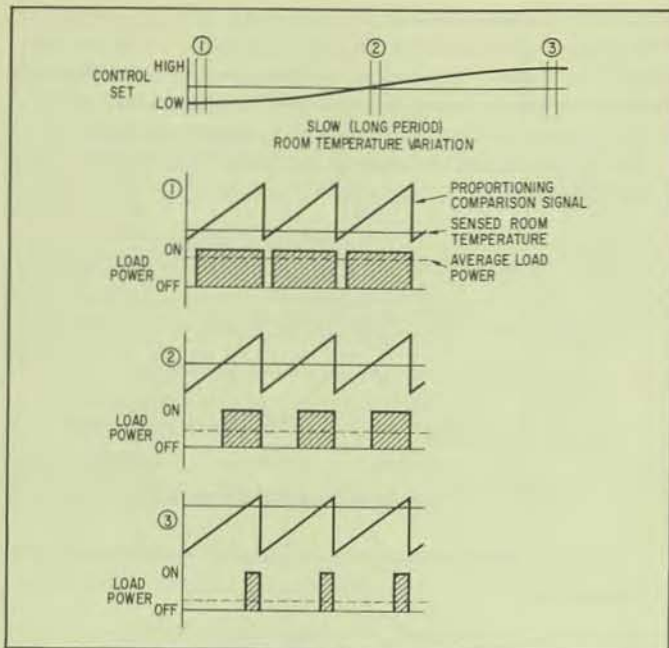
In many cases, tightened control of the hysteresis (S_1 - S_2) will provide sufficiently accurate temperature control and time proportioning will not be needed.

However, in systems which will not tolerate the overshoot-undershoot excursions of the dual threshold control, time proportioning is necessary. In this case, the control should have a 'single valued' response for each possible input temperature. Time proportioning is similar in concept to the 'continuously variable control' in that the variation of the average power applied through a given input signal range (0 to 100%) is proportional to the sensor output.



Application 3c.

If this response (App. 3c) is compared to that given in Application 3b, the advantage of time proportioning is apparent. The time/temperature variation is smaller due to the fact that the system stabilizes at a condition in which the average room power input exactly balances the heat loss. Therefore, virtually steady state heat flow exists throughout the room. Circuits using phase control are capable of this feature, but have the disadvantage of high RFI/EMI generation. Since zero crossing control is by definition limited to turning the load supply ON and OFF at the zero crossing of the load current, it must switch in whole cycles only. Therefore, the one possible method for varying average load power input with zero crossing control is to control the *percentage* of the total number of available line whole cycles which are applied to the load. One form of this technique is called time proportioning.



Application 3d.

Its operation is illustrated in Application 3d. The top of this figure shows a room temperature control system in which the sensed temperature very slowly varies (possibly over a period of hours). Three representative conditions are selected:

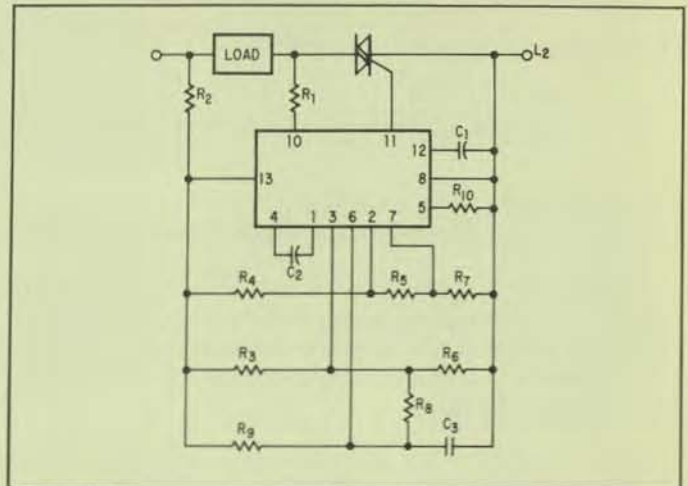
- Case 1. Low room temperature — the system calls for high heat.
- Case 2. Medium room temperature — the system demand is for 50% heat.
- Case 3. High room temperature — system demands low heat.

The first case is modeled by the signals shown in the second graph from the top. Note that the input temperature is represented by a straight line (the variation in this parameter is so slow that no slope is visible). The proportioning reference signal is represented by a "sawtooth" waveform. If the control system is arranged so that the load power is turned ON whenever the sawtooth reference is higher than the sensed room temperature, then the "load power" cycling period will occur as shown. It should be kept in mind that the switching rate of the load is very fast relative to the room's response. Therefore, the power "bursts" shown on these diagrams are seen by the room as continuous power input (represented by the dashed line). In this control condition the average load power is high, and the load is turned ON for a greater proportion of the time.

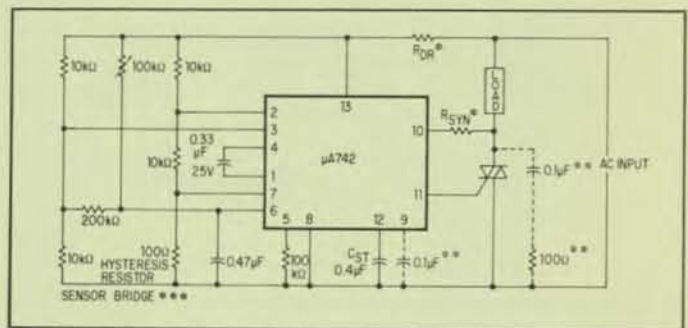
The second case (shown in the third graph from the top) is similar to the first, with the exception that the temperature signal is higher and the control demands less power. In this situation, the proportioning reference input is higher than the measured temperature for only half of the time — creating conditions which hold the load power for an identical period. In Case 2, therefore, the room receives an average power equal to half of the power available when the heater is on continuously.

The third case shows conditions when the input temperature is high and the load power demand is low. Here, the proportioning reference exceeds the sensed temperature only near the peaks of the sawtooth, and the load is switched ON for only a small percentage (or proportion) of the time.

The time proportioning mechanism: Application 3e produces the transfer characteristic given in Application 3c, and shows how the power applied to the load is 'time proportioned' in order to control the average power output. The operation is implemented by simply generating a sawtooth waveform (analogous to the 'reference' waveform given in Application diagram 3d) through the use of an RC charging circuit and a constant voltage breakover trigger built into the TRIGAC. The sawtooth is then applied to the (+) input of the TRIGAC (pin 3) via a coupling resistor. The comparison room temperature signal is fed into the TRIGAC's (-) input (pin 2) in the manner used in Applications 1 and 2. Thus, electronic signals reproducing those shown in Application 3d are produced. The circuit is shown in Application 3f.



Application 3e.



Application 3f. Time proportioning control.

The sawtooth is generated by the 'relaxation oscillator' formed by Rg, C3, and a 6.6 volt (approx.) fixed threshold thyristor (of the type described on page 29) in the TRIGAC. If we start with Cg discharged, then charge current through Rg causes C3's voltage to increase during each positive excursion of the line voltage (when the 21 volt VCC is present). When the capacitor's voltage reaches the threshold 6.6 volts, the thyristor between TRIGAC pins 6 and 8 turns ON, and the capacitor is rapidly discharged to about one volt. The thyristor then loses latching current during a negative line half cycle, and C3 is again permitted to begin charging. The sawtooth thus generated across C3 is coupled to the pin 3 input of the TRIGAC by R8. The $\mu A742$'s input amplifier section treats the sawtooth generator output as an additional input signal, which produces a tendency for the system to proportionally switch the load for sensor input signals varying between S1 and S2.

This input signal's effect is set by the relationship of the resistance value of R_8 to the other parts of the connected arms of the input bridge — R_3 and R_6 .

Since the time proportioning switch operates between two set points V_1 , and V_2 , (the turn ON and turn OFF voltages for the thyristor), and the value of R_8 is typically at least ten times the value of the standard bridge input resistors (R_3 and R_6), then we can approximate the effect of the time proportioning switch's swing by saying that R_8 is connected to ground at the end of the proportioning period (when the switch turns ON). During the rest of the time, R_8 is driven by C_3 's rising voltage ramp. If this is the case, then:

$$\Delta V_{\text{pin 3}} = 21 \left[\frac{R_6}{R_3 + R_6} - \frac{R_6 // R_8}{R_3 + (R_6 // R_8)} \right]$$

Substituting values for those given in the Construction section:

$$\Delta V_{\text{pin 3}} = 21 \left[\frac{5k}{5k + 5k} - \frac{\frac{(10k)(200k)}{210k}}{10k + 9.53k} \right] \begin{matrix} R_3 = 10k\Omega \\ R_6 = 10k\Omega \\ R_8 = 200k\Omega \end{matrix}$$

$$= 21 (0.500 - 0.487)$$

$$= 0.237 \text{ volts}$$

The circuit has a small resistor for the hysteresis function, R_7 . This is used to provide the system with some noise immunity, and should be used if any tendency to 'jitter' is observed with slowly rising ramp inputs from the time proportioning switch.

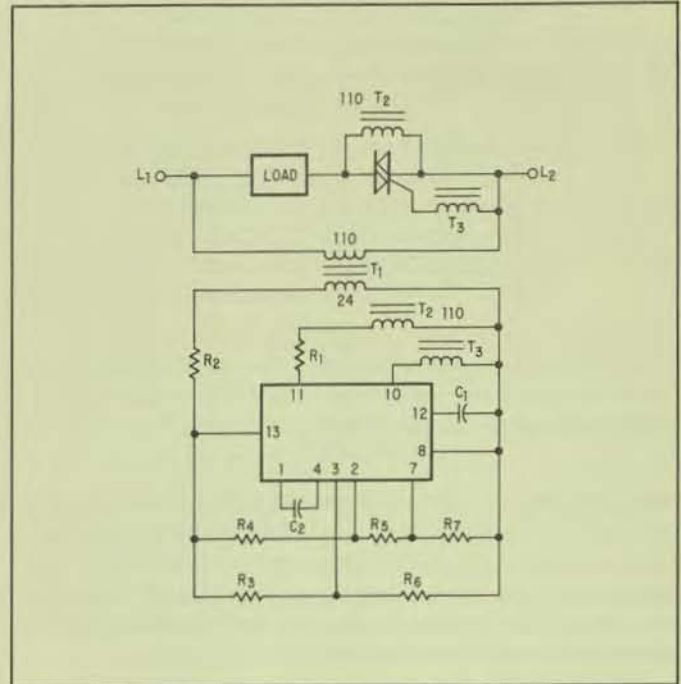
Note also that a resistor R_{10} has been placed between TRI-GAC pin 5 (marked 'switch gate') and system ground. This resistor controls the switching sensitivity of the proportioning switch, and should be selected for values between 10k and 100k Ω . In addition, for control systems in noisy environments (or when switching inductive loads) a small capacitor may be required to suppress noise pickup at the input bridge. If this is the case, a .01 μ Fd, 25V capacitor in parallel with R_{10} should eliminate the problem.

APPLICATION 4

1 Φ Operation with Transformer Isolation Between the Control Circuit and the AC Line

The form of the TRIGAC's output gate pulses and the nature of the synchronizing signal make DC isolated operation conven-

ient. Two systems are shown: for circuits which have resistive loads (the synchronizing signal exactly in phase with the line voltage), and for circuits with inductive loads (synchronizing signal time shifted from the line voltage zero crossing).



Application 4b. Transformer isolated circuit for inductive loads.

B. ACCESSORY CIRCUITS (APPLICATIONS 5-11)

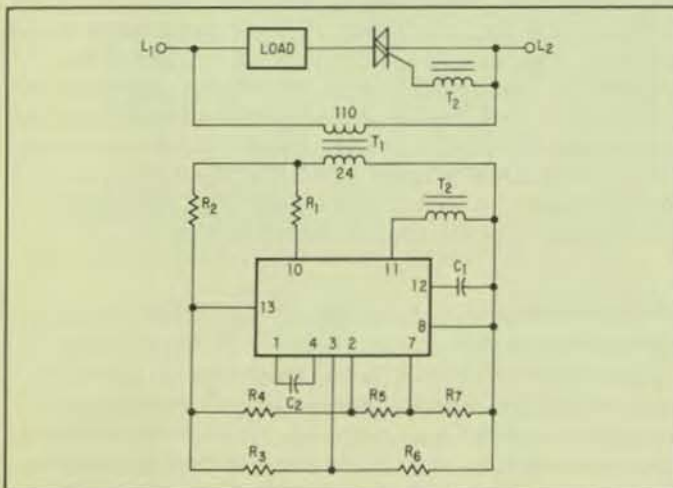
The following circuits add to the flexibility of the four preceding Applications. Each circuit has a printed circuit board layout in conjunction with the Construction section of the Handbook with letter coded terminals that match directly with the PC board layouts for Applications 1, 2, and 3. Each accessory application has a separate part numbering system, so the parts list for each design should be consulted to avoid confusion.

APPLICATION 5

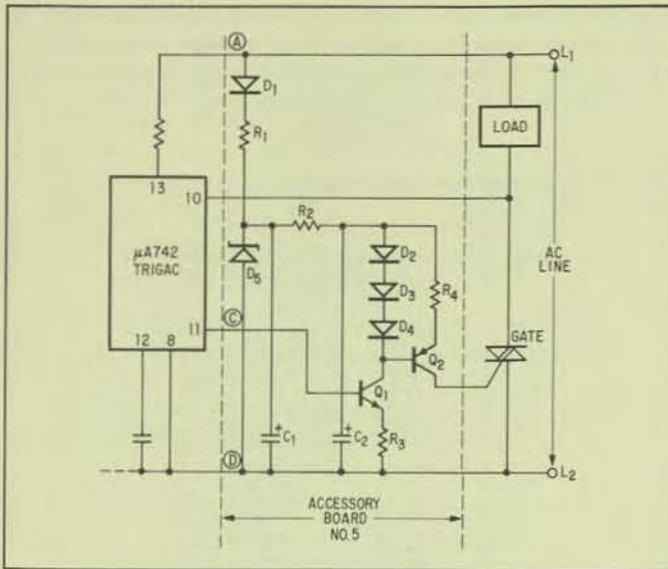
Output Pulse Amplifier

The TRIGAC produces an output pulse powerful enough for most currently manufactured triac and SCR power switches. However, there may be situations in which very insensitive power switches or loads with extremely slow current rise times will require longer and larger gate current pulses. This circuit produces 2 ampere 100 microseconds gate pulses for a typical triac and should be adequate for SCR's and triac's with current ratings of over 400 amperes.

In this circuit D_1 , R_1 , C_1 , and zener diode D_5 form a 20 volt half-wave shunt regulated DC supply. (The circuit values are for a 110 VAC supply line.) Energy stored in C_2 is transferred via R_4 and the collector-emitter circuit of Q_2 into the attached triac or SCR gate terminal. In a normal operating sequence, the output gate pulse from the TRIGAC is fed into the base of Q_1 . Q_1 then turns ON, forward-biasing diodes D_2 , D_3 , and D_4 .



Application 4a. Transformer isolated circuit for resistive loads.



Application 5. Output pulse amplifier.

This places a fixed voltage between the (+) terminal of C_2 and the base of Q_2 . This places a relatively constant 1.8 volts between the higher voltage side of R_4 and the base of Q_2 . If we subtract from this the 0.6 volt V_{eb} of Q_2 , then the remaining 1.2 volts will be maintained across R_4 , and the emitter current will automatically be held at the value

$$\frac{1.2}{R_4}$$

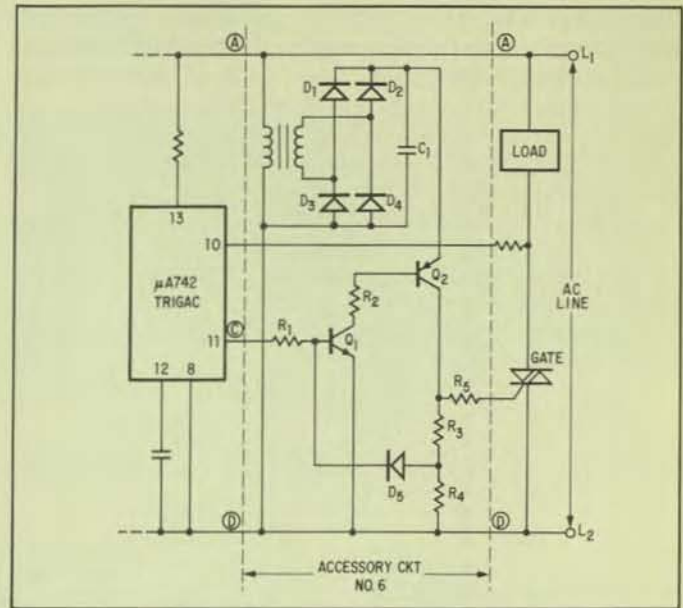
since for reasonably high gain transistors, $I_e = I_c$, the combination D_2, D_3, D_4, R_4 , and Q_2 form a constant current source which is switched ON whenever Q_1 is turned ON by the TRIGAC's output pulse. Note that the ON period for this circuit can be controlled by varying the size of the TRIGAC's storage capacitor (C_1).

APPLICATION 6 Output Pulse Amplifier (with Transformer)

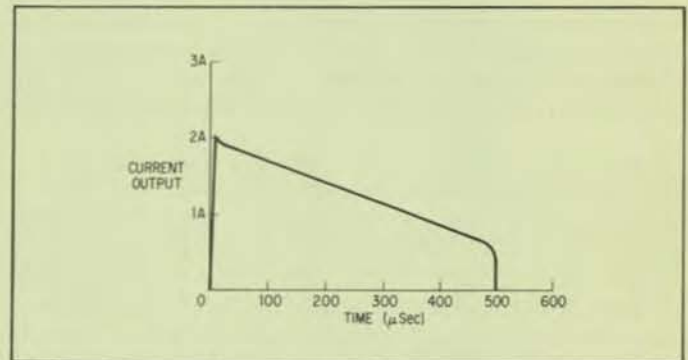
This circuit produces amplified pulses of longer duration than those developed by Application 5. Also, it has lower power dissipation and lower cost for high volume control systems.

It produces output pulses which typically have a 2 ampere peak current with relatively linear decay to 1 ampere within 500 microseconds. The arrangement is basically simpler than that used for Application 5, but does not have the constant current feature. Therefore, the output current is more dependent upon the power switch gate's terminal characteristics. For this reason, the circuit's output waveform should be checked with the particular SCR or triac to be used.

Power for the circuit is supplied by the stepdown transformer T_1 (a common 6.3 volt filament transformer), the full wave rectifier bridge formed by diodes D_1, D_2, D_3, D_4 , and capacitor C_1 . When an output pulse is received from the $\mu A742$ via R_1 , transistor Q_1 is turned ON. Q_1 's collector current provides base drive (through R_2) to PNP transistor Q_2 . Q_2 is the output switch, and transfers energy from C_1 into the gate of the external power thyristor. During the output pulse, the increased voltage at Q_2 's collector provides some added base



Application 6a. Long duration pulse amplifier.



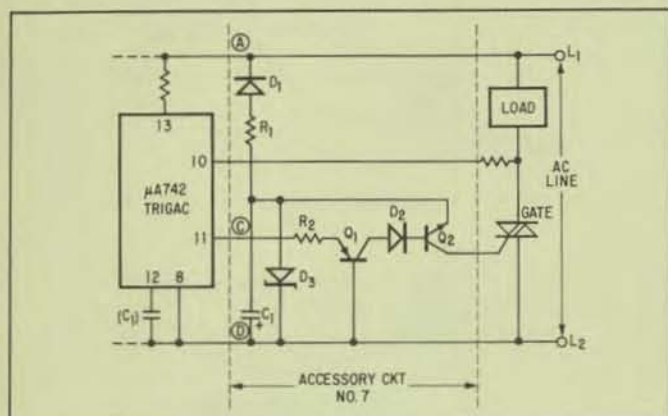
Application 6b. Output pulse waveshape.

drive for Q_1 via the R_3 - R_4 divider. This has an effect identical to the thyristor action described on page 28, and causes the Q_1 - Q_2 transistor pair to latch ON until C_1 has been partially discharged. When the current supplied by C_1 has fallen to a value below that required to hold Q_1 - Q_2 in latch (about 1 ampere), the transistor pair turns OFF, and C_1 is recharged by the power supply. Note here that the energy contained in each output pulse is set by the voltage change C_1 experiences during the pulse. The rate of discharge of C_1 is set mainly by the triac's input characteristics. Also, the TRIGAC only serves to initiate the output pulse for this arrangement, and does not set the resultant Q_2 ON time. For this reason, the circuit is useful when it is desirable to lower the TRIGAC circuit's C_1 (the charge capacitor) — a good feature when driving insensitive gate load switching thyristors in 400Hz systems.

APPLICATION 7 Output Pulse Inverter

Some triacs, such as the "logic-triac" require negative gate pulses for proper full wave operation. Since the TRIGAC produces positive pulses, this circuit is included in the Handbook as an output pulse inverter for control systems using negative gate thyristors.

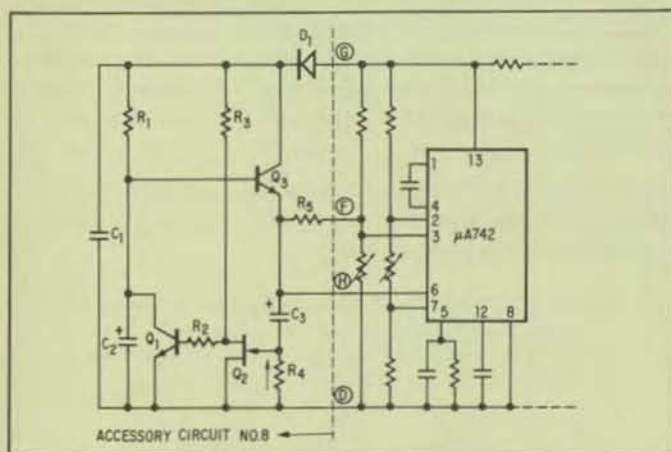
The circuit's operation: D_1 , D_3 , R_1 , and C_1 form a zener-stabilized 20 volt half-wave supply for the inverter. Output pulses from the TRIGAC's pin 11 are fed through R_2 into the emitter of Q_1 — permitting conduction in Q_1 's collector. This in turn supplies base drive to Q_2 through D_2 . Q_2 is then turned ON, discharging the energy stored in C_1 in the form of negative triac gate current. The duration of this pulse is set by the TRIGAC's output pulse, and may be varied by adjusting the value of R_2 or the size of the TRIGAC circuit's (C_1). D_2 prevents reverse breakdown of Q_2 's emitter-base junction.



Application 7. Output pulse inverter.

APPLICATION 8 Period Extender for Time Proportioning

It is occasionally necessary to extend the period for the time proportioning* form of operation (to model external system time constants, for instance). The circuit given in this Application will provide a proportioning time base input for the TRIGAC with a period of up to 1½ minutes.



Application 8. Long "90 second" time proportioning.

The time base for the sawtooth waveform is generated by the RC charge circuit formed by R_1 and C_2 . Charge from the TRIGAC's V_{CC} (21 volt) supply is supplied via forward biased D_1 for this purpose. Tracing a standard operating cycle for generating the sawtooth:

1. Assume that C_1 is charged and C_2 discharged. Current through R_1 caused C_2 's voltage to rise at the rate set by R_1 , C_2 .
2. This rising voltage is presented to the base of the Q_3 emitter follower, which holds the positive terminal of C_3 to within 0.6 volts of C_2 .
3. The time rise of C_2 is then reflected as an equal increase in C_3 's voltage, which is coupled by R_5 to the (+) input of the TRIGAC.
4. When C_3 's voltage has reached the breakover value of the TRIGAC's internal threshold thyristor, it is rapidly discharged via the path formed by pins 6 and 8 of the TRIGAC (the internal thyristor) and resistor R_4 . Discharge current flows through R_4 in the direction shown by the arrow.
5. The charge-discharge fluctuation in the voltage of C_3 generates a sawtooth waveform which functions in exactly the same manner as the shorter period sawtooth described in Application 3. R_5 couples this into the (+) input of the TRIGAC.
6. The remaining components have the function of resetting the charge in C_2 to approximately zero during the C_3 discharge. The method:
 - a. During the charging interval: Current through R_3 is shunted to ground by the drain-source circuit of Q_2 , a junction field effect transistor. (For the purpose of this discussion, Q_2 may be regarded as simply a resistor of about 125Ω when zero or a positive voltage is applied to its gate. However, when a negative gate voltage of sufficient magnitude is applied, its drain-source terminals become essentially open-circuited.)
 - b. During the discharge interval: C_3 's discharge current through R_4 produces a negative gate voltage for Q_2 — causing a sharp rise in the drain-source resistance. The current through R_3 is then routed via R_2 into the base of Q_1 . With Q_1 turned ON, C_2 is reset via Q_1 's collector emitter terminals.

Diode D_1 and capacitor C_1 serve to maintain the V_{CC} supply for this part of the circuit during the line voltage's negative cycles (when the TRIGAC's V_{CC} is not present).

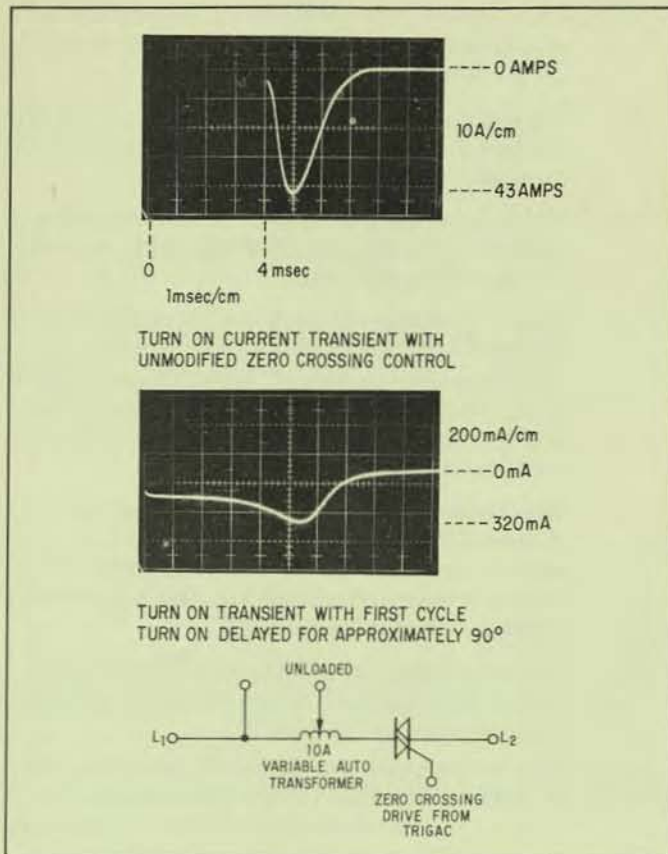
APPLICATION 9 Initial Cycle Delay

A number of common AC loads have magnetic structures which are capable of being saturated during the first cycle after turn ON. Loads of this type include:

- welding transformers
- large standard transformers
- variable autotransformers ("Variacs")
- large motors.

This first cycle magnetic saturation results in a very sharp rise in load current just after the application of power. This phenomenon, often an unrecognized problem, can cause failure of the power switching thyristor (triac or SCR). For instance, the waveforms shown in Application 9a were taken with a standard 10 amp bench autotransformer.

*See Application 3.



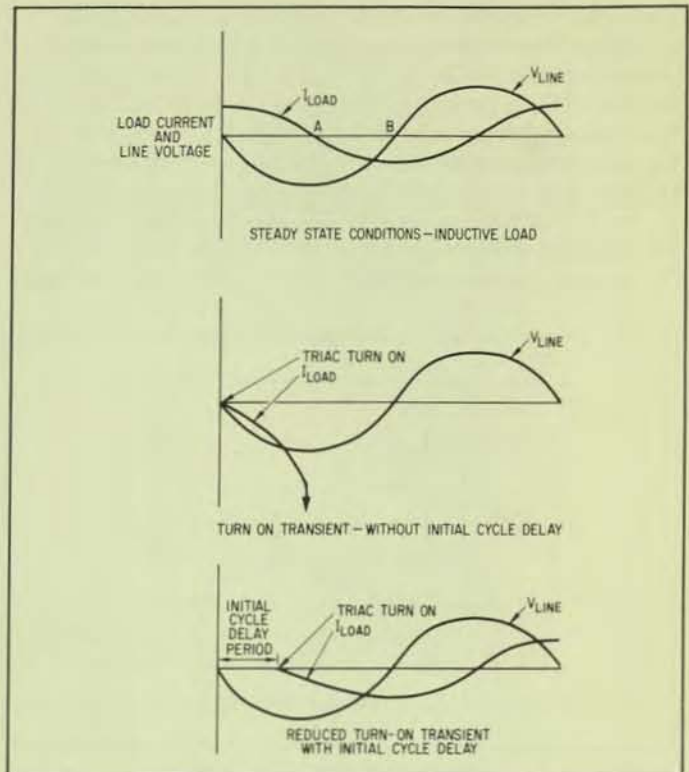
Application 9a. Typical initial cycle transients.

Note that by delaying the start of the first cycle turn ON of the triac by about 4 milliseconds, the surge transient has been reduced from 43 amperes to just about 0.3 amperes.

We may logically explain the use of initial cycle delay in this manner: If we plot steady state operating conditions for an inductive load, Application 9b results.

The three possible operating conditions are shown in this diagram. In the first plot, the steady state (normal) condition shows that there is a positive current in the load at the extreme left of the diagram. This current crosses zero at approximately the peak of the negative half cycle and then reverses to reach a peak in the negative direction at the same time as the applied voltage's positive going zero crossing. The initial positive current represents an energy storage condition in the load's core structure that "prebiases" the load with a field which is reversed by the negative half cycle of the applied line voltage.

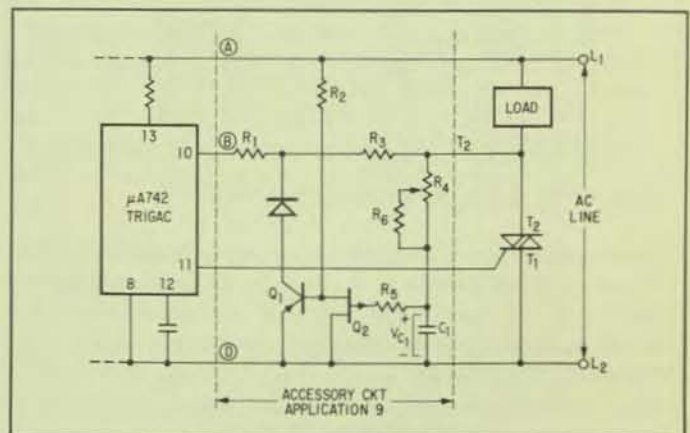
If we compare this with the center diagram (starting from the OFF condition), we see that no such "prebias" exists. In this case, the magnetic structure receives a full 8.3 milliseconds of applied negative voltage. The current flow for the first quarter cycle of this operation is loosely analogous to time span A-B in the first graph. However, in this case the applied line voltage does not reverse at the end of a quarter cycle, but continues with the same negative polarity. Therefore, after the first quarter cycle, further application of negative line voltage results in a rapid increase in load current, as shown. This causes an increase in magnetic flux until the core's saturation level is reached. The condition can be destructive to the triac power switch, particularly if it coincides with a negative line transient.



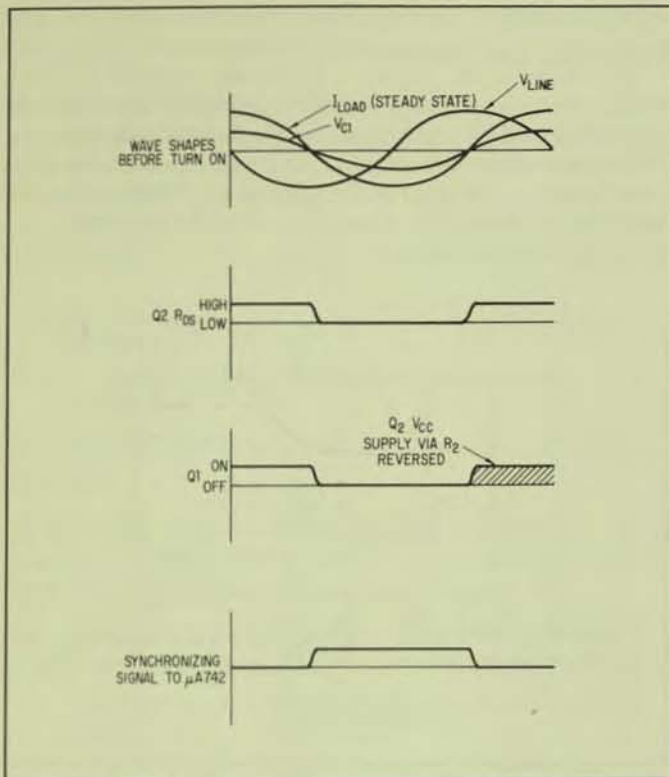
Application 9b.

The bottom plot demonstrates the effect of the initial cycle delay. A comparison of the top and bottom plot shows the similarity in the load current/flux condition. We have applied negative current to the load at approximately the same time that its current would have crossed zero when operating in steady state conditions. The load receives only about 4 milliseconds of applied negative voltage before the line reverses polarity. Numerous experiments have shown that this approach can reduce the turn ON transient to almost the same level as the steady state operating current. The RFI/EMI (ElectroMagnetic Interference) that would normally be generated by switching in midcycle is avoided because the flux-free load acts as its own inductive EMI filter during initial turn ON.

This circuit blocks the first synchronizing signal to the TRI-GAC's pin 10 terminal until the middle of the first negative line half cycle has been reached.

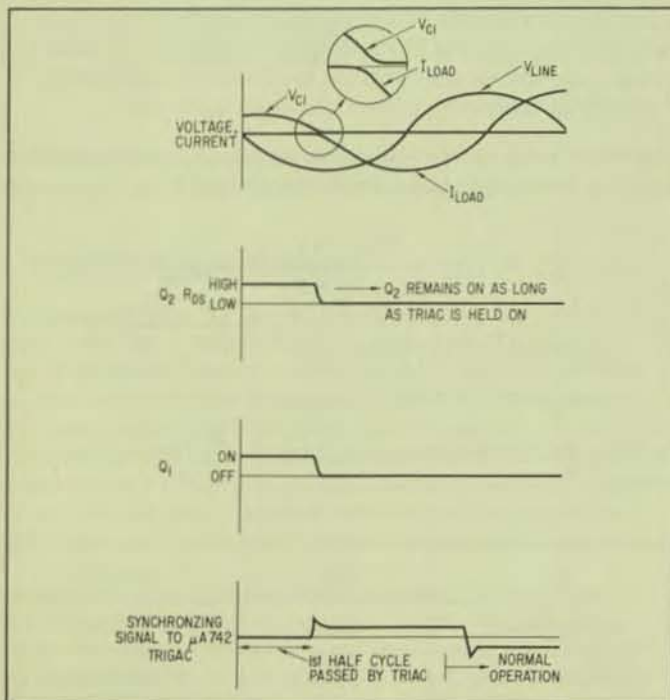


Application 9c. Initial cycle delay schematic diagram.



Application 9d.

If we assume that the triac is OFF (there are no gate pulses from the TRIGAC), approximately full line voltage will be developed across its T₁-T₂ terminals. R₄ and C₁ will then form a phase shift network which generates a 90° phase shifted voltage across C₁. This voltage is applied via R₅ to the gate of Q₂, a P channel junction field effect transistor. A bias network formed by R₂ (connected to L₁) and Q₂'s drain-source terminals drives the base of Q₁ during the periods in which the



Application 9e.

R_{ds} value of Q₂ is high. These conditions are illustrated in Application 9d. In this circumstance, the circuit produces a synchronizing signal that is delayed by approximately 90° from the line voltage zero crossing. This condition continues until the TRIGAC's input amplifier calls for the application of gate drive to the triac power switch.

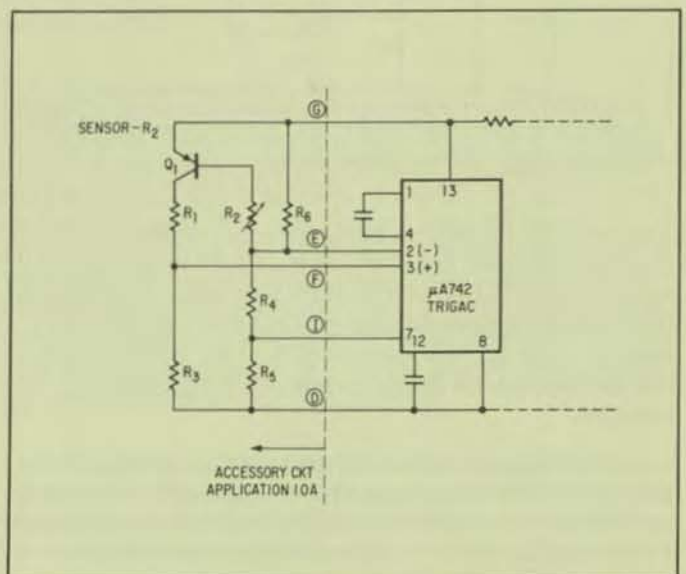
When this occurs, the waveforms shown in Application 9e are generated. Here the circuit works as before until the drive to R₄ is interrupted by the triac's low saturation voltage (about 2 volts). There is now insufficient drive for the R₄, C₁ phase shift circuit to apply turnoff voltage to the gate of Q₂. The FET then stays permanently ON, holding Q₁ OFF. With Q₁ turned OFF, R₁ and R₃ act as the normal synchronizing drive resistor (which is given as R₁ in the schematics for Application 1, 2, 3, and 4).

An additional note: The divider formed by R₁ and R₃ limits the V_{CE} voltage applied to Q₁. R₁ also acts as a divider together with the TRIGAC's internal input resistors to prevent false application of the synchronizing signal. For optimum performance, the circuit's phase delay should be matched to the load. For this purpose, potentiometer R₄ is provided.

APPLICATION 10

Sensor Failure Detection Circuit – Failsafe Operation

In many control systems the failure (short or open circuit) of an input sensor can cause a dangerous condition. For instance, a heating control with an NTC (Negative Temperature Coefficient) sensor would interpret shorted thermistor leads as a very high sensed temperature and would interrupt the application of power to the load. This could be regarded as a 'failsafe' condition since furnace oven temperature (and the resultant fire or explosion hazard) is avoided. However, if the same NTC sensor fails in the 'open' condition (due to lead wire breaks, etc.) the control system would respond as if to a low temperature, and power would be continuously applied to the load. In this case, an open sensor detector is required to protect the system against the resulting dangerous condition.



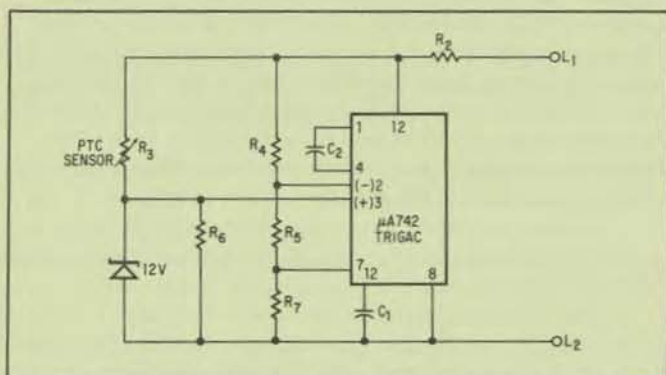
Application 10a. Open sensor detector.

In general, both types of sensor — NTC and PTC — have one failure mode which is subject to interpretation by the control system in a dangerous manner. If we assume that the 'output thyristor OFF' condition is safe, then the unsafe modes would be:

Sensor Type	Unsafe Failure
NTC	Open Circuit
PTC	Short Circuit

The two circuit modifications of the TRIGAC's input bridge shown are suggested to handle these conditions. Of course, other control situations (e.g. airconditioners or motor controls) will require a different combination of these two circuits. The important point is that these two techniques may be applied to detect either of the two possible dangerous conditions — short or open circuit.

During normal operation, Q₁ is held in the saturated ON condition by the current through R₂. This provides enough base drive to apply V_{CC} (minus Q₁'s V_{CE} (sat)) to R₁. R₆ (about 50kΩ) is too high to seriously affect the circuit's operation. If R₂ (which includes the sensor) should open, then base drive for Q₁ is interrupted, and the transistor turns OFF. With Q₁ OFF, there is no voltage supply for R₁, and the (+) input (pin 3) voltage falls. At the same time, R₆ applies a positive voltage to the (-) input. This fulfills the condition given on page 6, (+) input lower than the (-) input for the TRIGAC's OFF state and insures that no gate drive will be delivered to the power switching thyristor — a 'safe' condition.



Application 10b. Shorted sensor detector.

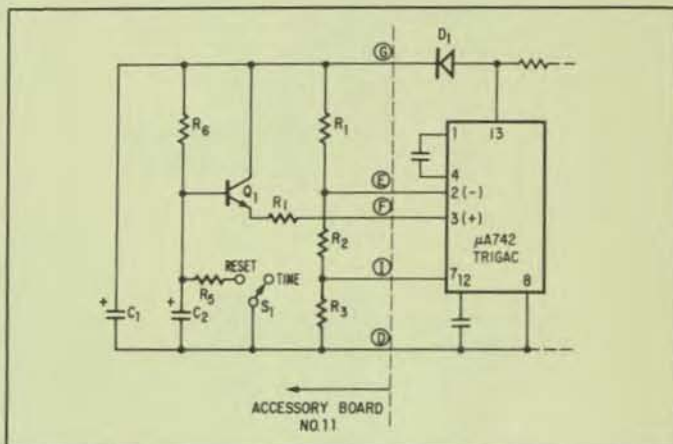
The circuit for the shorted sensor detector is shown in Application 10b. When the sensor arm of the input bridge is shorted, zener diode D₁ limits the TRIGAC's V_{CC} voltage by shunting the IC's internal zener regulator. In this case, the TRIGAC's internal circuitry will prevent turn ON of the input amplifier, and thereby prohibit charge transfer into the C₁ storage capacitor.

It may be necessary to shift the values of R₄ and R₅ so that the (+) input will not exceed 10 volts under normal operating conditions. No circuit layout is given for this in the Construction section, since it only involves adding a zener diode in parallel with one of the input bridge resistors for the printed circuit boards given for Applications 1, 2, 3, and 4.

APPLICATION 11

Time Delay 'Relay' Circuit

There are many possible ways in which the TRIGAC's flexible input bridge may be used to generate a time delay function. One of the most common utilizations would be the 'time delay relay' which is illustrated in Application 11. This circuit holds the TRIGAC in the OFF state for a controlled time after switch S₁ has been opened.



Application 11a. Time delay 'relay'.

If we assume that S₁ is in the 'Reset' position, R₅ holds the C₂ voltage to within one volt of ground. This will hold Q₂ in the OFF condition, effectively lowering the TRIGAC's (+) input to near ground. At the same time the voltage divider formed by R₁, R₂, and R₃ holds the (-) input near 10 volts. The TRIGAC will therefore be held in the OFF condition.

When the switch is moved to the 'Time' position, C₂ is charged by current through R₆. The emitter voltage of Q₁ will correspondingly increase along with the C₁ voltage until the (+) input (pin 3) voltage is within several millivolts of the (-) input. At this point, the TRIGAC switches into the ON state, and gate C₂ voltage will continue to rise until it stabilizes at some higher value.

The circuit's C₂ turn ON voltage is set primarily by the resistor values in the bridge biasing the (-) input (pin 2):

$$V_{\text{turn ON}} \cong V_{CC} \frac{R_2 + R_3}{R_1 + R_2 + R_3} + V_{beQ1}$$

$$\text{Where } V_{CC} \cong 21 \text{ volts}$$

$$V_{beQ1} \cong 0.5 \text{ volts}$$

Test results for the circuit values given in the Construction section:

R ₆	C ₂	Time delay
4.7 megohm	1.0μFd	5 seconds
10 megohm	1.0μFD	10 seconds
4.7 megohm	25μFd	150 seconds

When S_1 is returned to the 'Reset' position, C_2 is discharged through R_5 . The value for R_5 given in the construction section is small — for rapid reset of C_2 . However, if a time delay on turn OFF function is desired, R_5 may be increased. In this case, C_2 would be discharged at the rate determined by the R_5C_2 product. The C_2 voltage level for turn OFF would then be approximately:

$$V_{\text{turn OFF}} \cong V_{CC} \frac{R_2}{R_1 + R_3} + V_{beQ_1}$$

Where $V_{CC} \cong 21$ volts

$V_{beQ_1} \cong 0.5$ volts

D_1 and C_1 provide the timer circuit with a half-wave rectified DC supply.

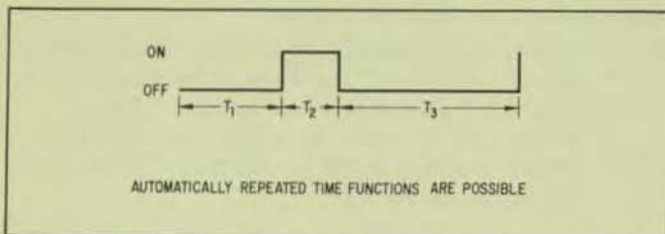
When the C_2 voltage has reached this level, the TRIGAC will be held in the OFF condition until the switch is again moved to the 'time' position.

There are three threshold detection methods for generating various simultaneous time delay functions with the TRIGAC:

1. Normal input voltage level detection (as used in this application).
2. Use of the clamp transistor (pin 7) to generate a second turn OFF level by unbalancing the input bridge by a controlled amount.
3. Use of the TRIGAC's internal 6.6 volt proportioning switch (pin 6).

Combinations of these features will produce control functions such as the one shown here.

Also, automatically repeated time functions are possible.



Application 11b. One possible time sequence.

C. THREE PHASE AC CIRCUITS

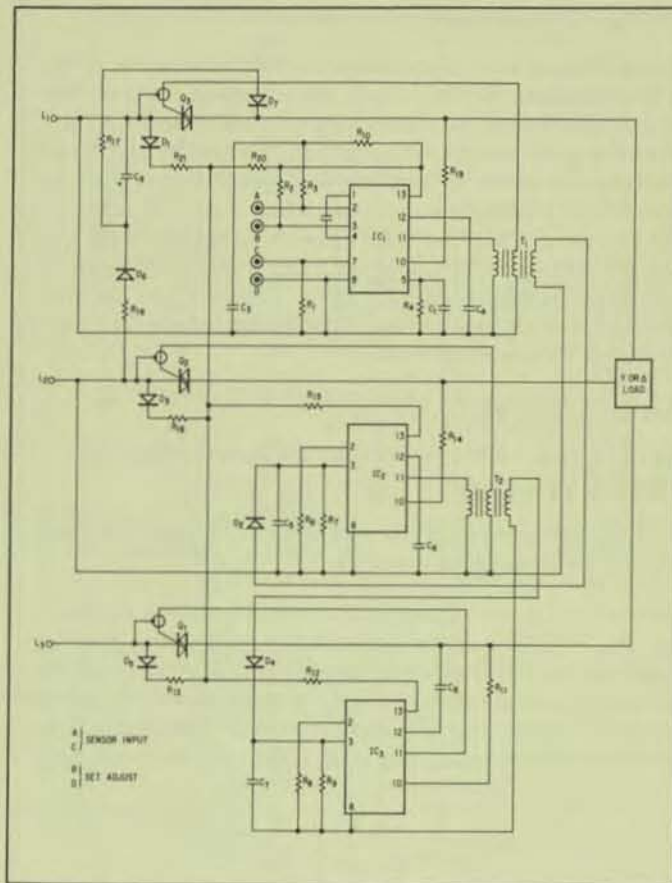
This section shows the $\mu A742$ TRIGAC in two three-phase circuits. The first, Application 12, uses three TRIGAC's, two of which are 'slaved' to the lead unit. The configuration permits turn ON of the three supply lines (for either Y or Δ connected loads) in a 1-2-3 sequence. The second circuit gives complete control for a three-phase Y-connected load from the center of the Y. The three power switching thyristors are placed adjacent to the center (neutral) which is used as a common circuit ground — analogous to L_2 in the single-phase circuits.

Both applications lend themselves to most of the features available with Applications 1, 2, 3, 4 and the Accessory circuits. For instance, the addition of long period time proportioning (Application 8) or sensor failsafe (Application 11) should simply require small modifications of the 'lead' TRIGAC's input bridge.

APPLICATION 12

3 Φ , 208 VAC Dual Threshold Control with Time Proportioning — for Y or Δ Loads

This circuit supplies all of the features outlined in the discussion for Application 3. The values given in the Construction section have been tested in a 24kVA industrial application. With suitable variation in the voltage level shifting resistors (R 's 11 through 21) the circuit will operate on three-phase line voltages ranging from 24 to 440 volts.



Application 12.

TRIGAC₁ is the lead device. Its operation may be calculated with the same input bridge design formulas given in the discussion for Applications 2 and 3. The unit's V_{CC} supply is derived from a common buss fed by diodes D_1 , D_3 , and D_5 , and resistors R_{13} , R_{18} , R_{21} . Level change from the buss for TRIGAC₁ is via R_{20} . The synchronizing signal is through R_{19} . The circuit also has time proportioning (explained in Application 3), which is accomplished by R_{10} , C_3 , R_3 . False firing of the time proportioning switch is controlled by R_4 and C_1 . The input bridge consists of R_2 , R_1 , (on the printed circuit layout) and external resistors R_{22} , R_{23} , and R_{24} .

The IC's output pulses are coupled via T_1 's two secondary windings into the gate of the L_1 triac, Q_3 , and into the input of the following TRIGAC₂. The triac's gate terminals are transient-protected by using shielded wire for gate leads with the shields connected to the adjacent TRIGAC-triac pair's ground reference (L_1 in this case).

If we assume that TRIGAC₁ has just begun an ON cycle, then the gate pulse from it will be coupled via T₁ into an input filter for TRIGAC₂ which consists of D₂, R₆, and R₇. This presents a positive voltage to pin 3 (the (+) input), which causes TRIGAC₂ to supply gate drive to the L₂ triac, Q₂.

As Q₂ receives its gate drive, a second inter-TRIGAC input pulse is carried forward via T₂ to TRIGAC₃, which then turns ON at Q₁'s next zero crossing. Since there is no return connection between TRIGAC₃ and TRIGAC₁, the sequence ends here.

Thus for each ON command from TRIGAC₁, each of the following TRIGAC's deliver a full 360° input to the load.

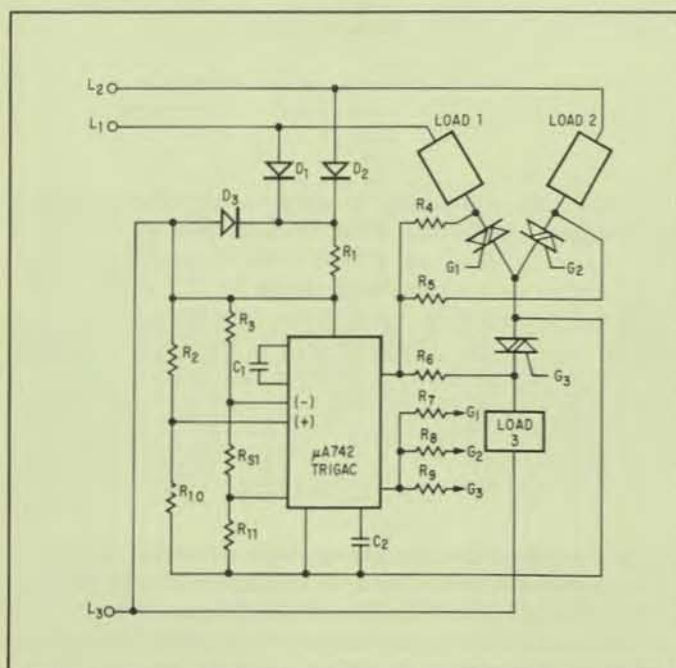
One additional note: For systems in which the center of the Y is ungrounded, or for Δ loads, the voltage of the three terminals entering the load block (the triac leads most remote from the gate) is relatively undefined (the load block "floats"). Therefore, a source for triac latching current during the initial turn ON of TRIGAC₁ must be supplied. This is done by using the half wave charge-discharge network formed by R₁₆, R₁₇, D₆, D₇, and C_g. When all of the triacs are OFF, C_g is charged to approximately the peak L₁ to L₂ voltage. When the first turn ON gate signal is applied, C_g is discharged via R₁₇ and D₇ to supply triac holding current.

APPLICATION 13

3Φ, 110 VAC, 400Hz Dual Threshold Control with Single TRIGAC for Y Loads

This application offers the lowest possible cost dual threshold control for three phase operation.

Diodes D₁, D₂, and D₃ act as three-phase rectifiers driving R₁ for the TRIGAC power supply signal. R₂, R₃, R₁₀, and R_{S1} comprise the TRIGAC's input bridge, with R₁₁ acting as the hysteresis control resistor. Since the operation of the two level hysteresis control has been dealt with in the Introduction and in the discussion in Application 2, it will not be covered here.



Application 13.

This control's operation differs from the description given in Application 2 only in these respects:

1. The V_{CC} supply is always present (there is no 'idling' interval for the input amplifier section).
2. There are three times the normal number of synchronizing signals (derived from the three triac T₂ terminals).
3. Current sharing resistors are required in series with the gates of each of the load switching triacs.
4. Because the TRIGAC's output current is shared by three gates, only sensitive gate triacs should be used.

The synchronizing signals are derived from the triac remote terminals via resistors R₄, R₅, and R₆. The output gate drive current sharing resistors are R₇, R₈, and R₉. C₂ is the gate drive charge storage capacitor while C₁ serves the memory capacitor function.

D. DC CIRCUITS

The TRIGAC has been designed primarily for operation directly from the AC line. However, its internal circuitry (see page 8) also permits operation with a fixed DC V_{CC} supply. In fact, the DC V_{CC} supply offers a number of advantages:

1. Convenient interfacing with external DC powered driving circuits.
2. Increased system noise immunity (due to the DC supply's filtering).
3. Increased gate output pulses for use with very insensitive triac or SCR thyristor power switches. (See the μA742 data sheet).
4. Operation with very capacitive loads.
5. Operation with supply line frequencies above 400Hz.

Almost all of the features listed in Applications 1 through 13 may be applied with the DC supply. However, the modifications suggested below should be used.

1. Supply Circuit Changes: The AC line supply resistor from L₁ to TRIGAC pin 13 should be disconnected from the line and a new value selected. (This is shown as R₂ in Applications 1, 2, 3, and 4.) Its size should be chosen so that a current of 12 milliamperes is available for pin 13:

$$R_{2dc} = \frac{V_{dc} - V_{CC}}{I_{supply}} = \frac{V_{dc} - 21}{.012} \quad \text{Where } V_{dc} \text{ is given in volts}$$

The circuit will operate with V_{dc} supplies ranging from 24 to 440 volts.

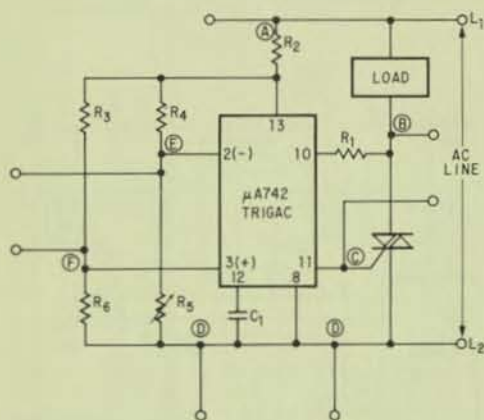
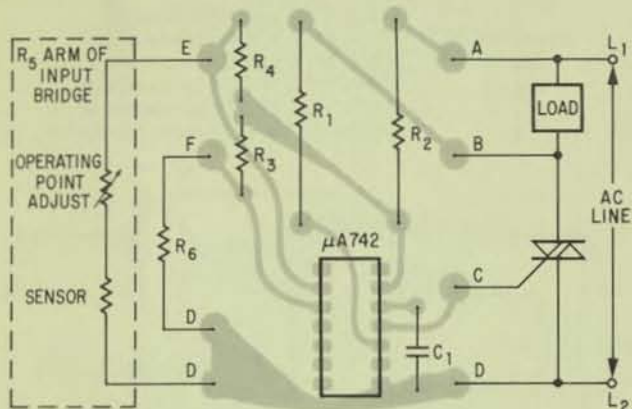
2. Circuits using relaxation oscillators: Several of the time proportioning and time delay configurations may encounter latch-up problems with the internal switch (pins 6 to 8). If this occurs, the switch's sensitivity may be decreased by lowering the resistor between the switch gate (pin 6) and ground (pin 8). This will also increase the current required to turn the switch ON and may force some compromises in the RC period. The effect, however, should not be serious.

E. CONSTRUCTION

This section includes the parts lists and the component location diagrams for all of the Applications described in parts IV A, B, and C or the Handbook.

APPLICATION 1

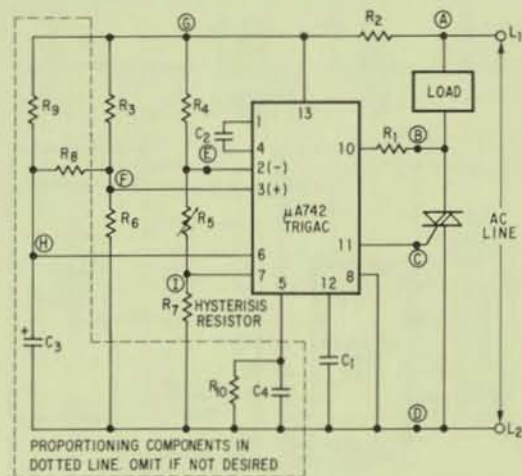
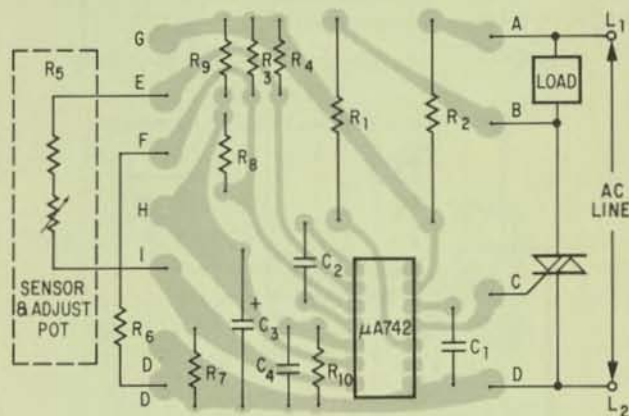
- R₁, R₂ 1k Ω , 1W (24 VAC Operation)
 10k Ω , 2W (110 VAC Operation)
 22k Ω , 5W (220 VAC Operation)
- R₃, R₄, R₅, R₆ 10 Ω 1/4W
 C₁ .47 μ F 25V Ceramic Capacitor



Application 1.

TRIGAC APPLICATION BOARD 2

- | Part Number | Description |
|---|--|
| R ₁ , R ₂ | 1k Ω 1W for 24VAC, 60Hz
10k Ω 2W for 110VAC, 60Hz
22k Ω 5W for 220VAC, 60Hz |
| R ₃ , R ₄ , R ₅ , R ₆ | These four Resistances are in the input bridge and are nominally 10k Ω each. R ₅ and R ₆ are the variables in the bridge and either one may be used depending on the sensor used. |
| R ₇ | The value of this Resistance determines the amount of Hysteresis in the System. (Min. 100 Ω for 10k Ω Bridge). |
| Proportioning Components | |
| R ₈ | 200k Ω 1/4W |
| R ₉ | 20k Ω 1/4W |
| R ₁₀ | 39k Ω 1/4W |
| C ₃ | 5 μ F 25V Electrolytic Capacitor |
| C ₄ | .01 μ F 10V Ceramic disc. Capacitor |
| C ₁ | .47 μ F 25V (60Hz Operation) Ceramic Capacitor Sprague 5C023474X025-0B3 (or equivalent) |
| | .047 (400Hz Operation) |
| C ₂ | .33 μ F 10V Ceramic Disc. Capacitor Sprague HY-327 (or equivalent) |



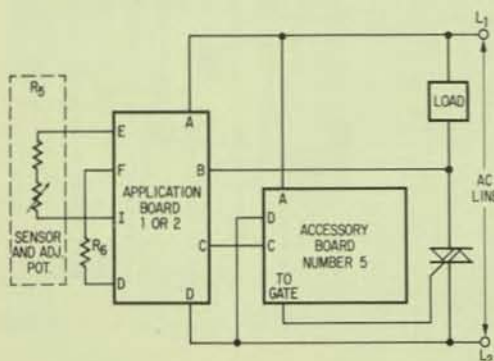
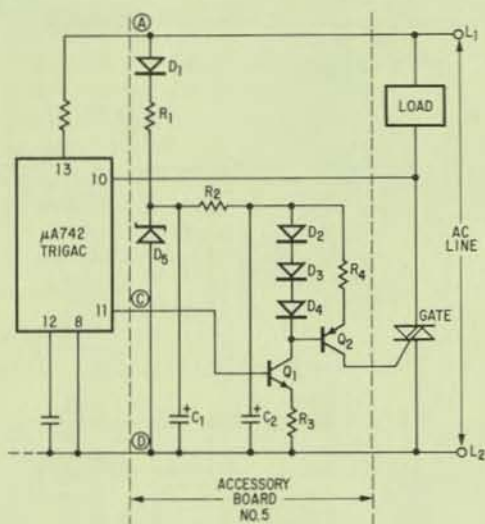
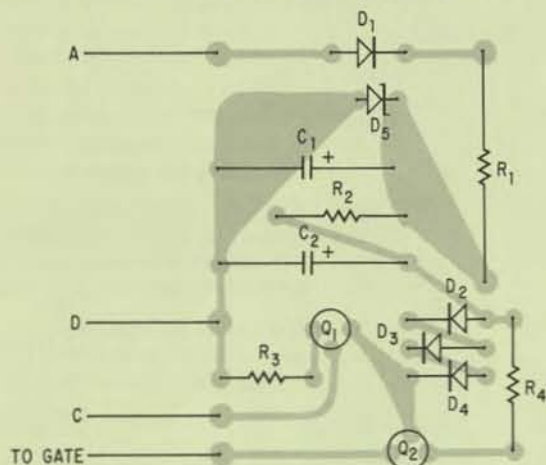
Application 2 and 3.

APPLICATION 4

Use the PC board supplied for Applications 2 and 3, and mount isolating transformers off the board.

ACCESSORY CIRCUIT APPLICATION 5

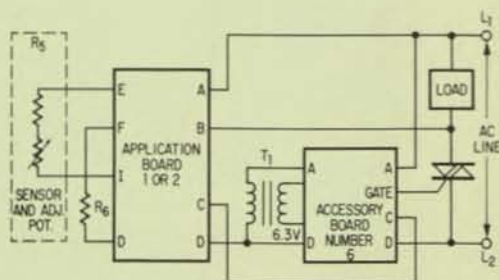
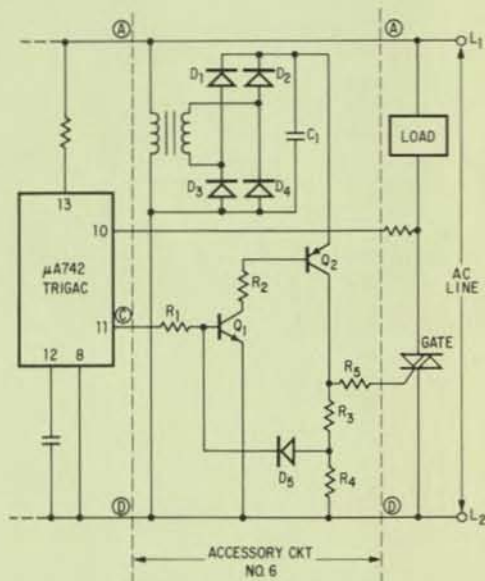
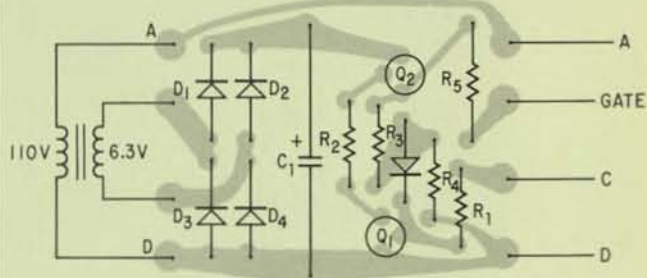
Part Number	Description
R ₁	2k Ω 5W Wirewound
R ₂	270 Ω 1/2W
R ₃	10 Ω 1/4W
R ₄	.5 Ω 1/2W
C ₁	20 μ F 50V Electrolytic Capacitor
C ₂	25 μ F 25V Electrolytic Capacitor
D ₁	1N 4004 (or equivalent)
D _{2, D_{3, D₄}}	FAIRCHILD FD 222 (or equivalent)
D ₅	1N 3796 (20V 1.5W Zener)
Q ₁	FAIRCHILD SE 6002 (or equivalent)
Q ₂	FAIRCHILD SE 8510 (or equivalent)



Application 5. Gate pulse amplifier.

ACCESSORY CIRCUIT APPLICATION 6

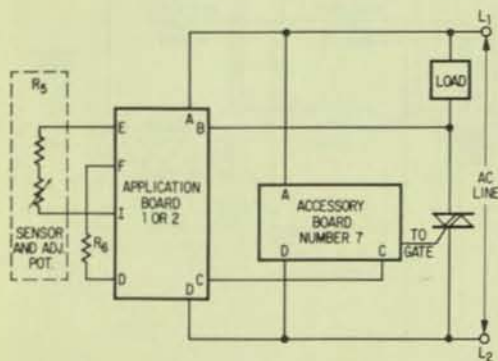
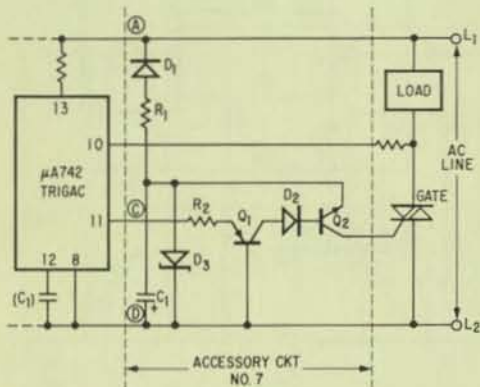
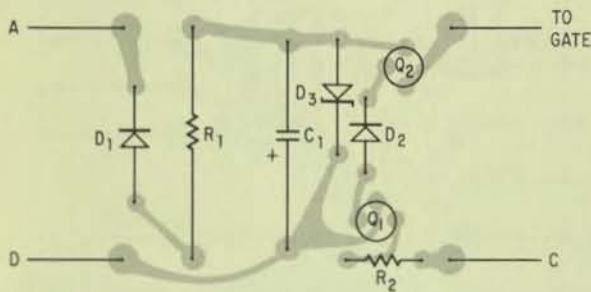
Part Number	Description
R ₁	27 Ω 1/4W 10%
R ₂	20 Ω 1/4W 10%
R ₃	270 Ω 1/4W 10%
R ₄	120 Ω 1/4W 10%
R ₅	1 Ω 1/2 10%
C ₁	100 μ F 25V Electrolytic Capacitor
D _{1, D_{2, D_{3, D₄}}}	Silicon diode 1N2069 (or equivalent)
D ₅	FAIRCHILD FD222 (or equivalent)
Q ₁	FAIRCHILD 2N3642 (or equivalent)
Q ₂	FAIRCHILD SE8510 (or equivalent)
T ₁	110V/6.3V 1 Amp Filament Transformer



Application 6. Output pulse amplifier (with Xfmer).

ACCESSORY CIRCUIT APPLICATION 7

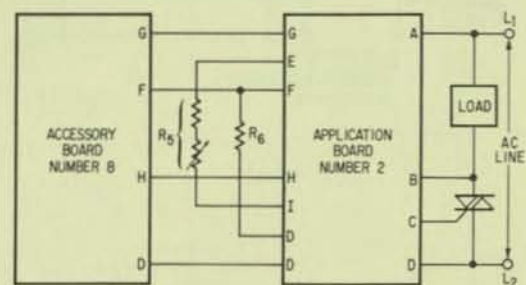
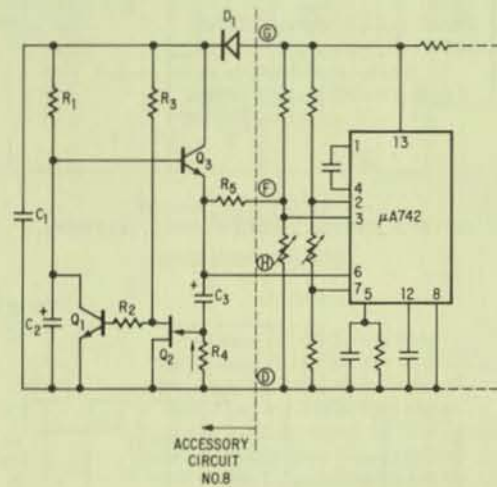
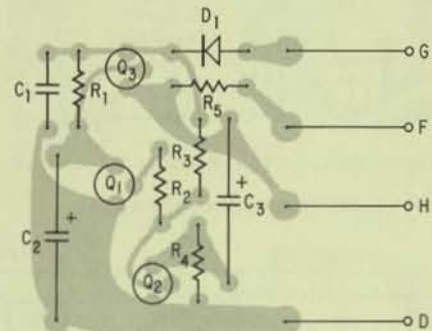
Part Number	Description
R1	5k Ω 5W
R2	27 Ω 1/4W 10%
C1	5 μ F 25V Electrolytic Capacitor
D1	1N2070 (or equivalent)
D2	FAIRCHILD FD222 (or equivalent)
D3	1N4747 20V Zener Diode (1W)
Q1	2N3638 (or equivalent)
Q2	2N3642 (or equivalent)



Application 7. Output pulse inverter.

ACCESSORY CIRCUIT APPLICATION 8

Part Number	Description
R1	3.9M Ω 1/4W
R2	10k Ω 1/4W
R3	47k Ω 1/4W
R4	270 Ω 1/4W
R5	330k Ω 1/4W
C1	.47 μ F 25V Ceramic Capacitor
C2	25 μ F 25V Electrolytic Capacitor
C3	1 μ F 25V Electrolytic Capacitor
D1	FAIRCHILD FD222 (or equivalent)
Q1	FAIRCHILD SE6002 (or equivalent)
Q2	2N5163 (or equivalent)
Q3	FAIRCHILD SE4010 (or equivalent)

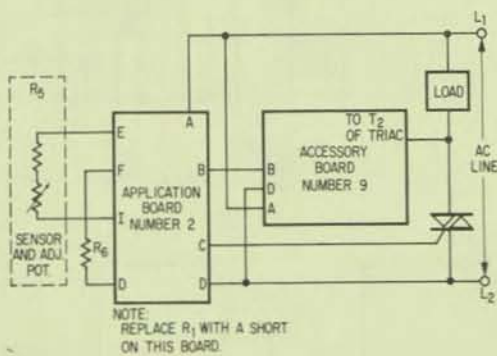
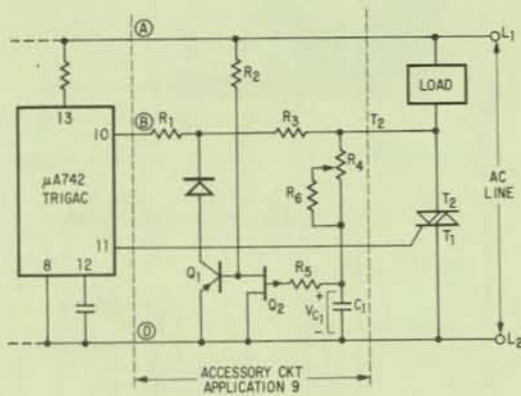
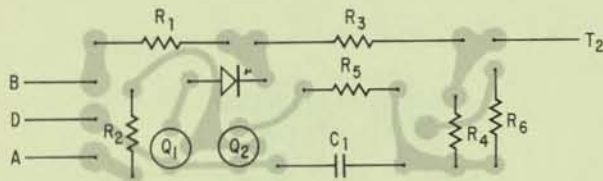


NOTE:
OMIT R₈, R₉, C₃.
CHANGE R₁₀ TO 4.7k Ω

Application 8. Long period time proportioning.

ACCESSORY CIRCUIT APPLICATION 9

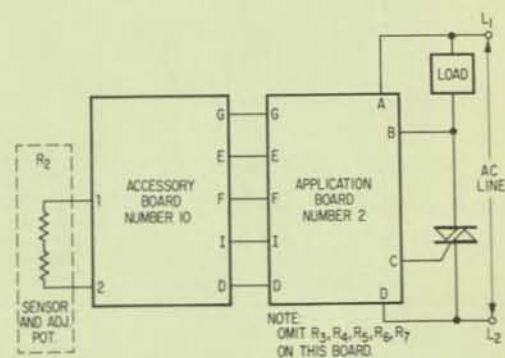
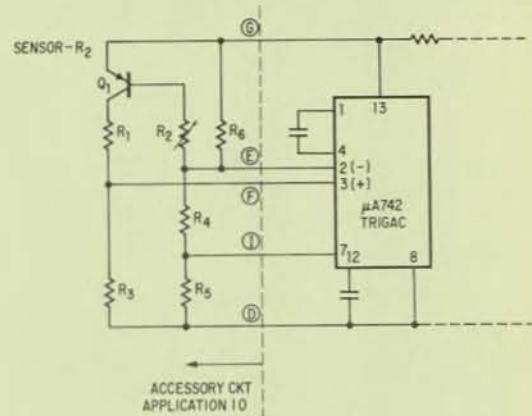
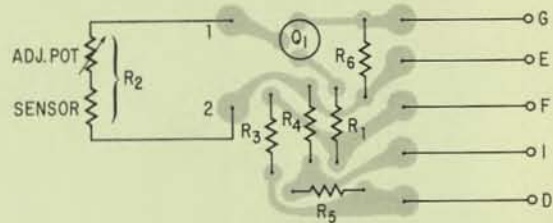
Part Number	Description
R1	1.5kΩ 1/2W
R2	330kΩ 1/4W
R3	8.2kΩ 2W
R4	250k Trimpot, (IRC type)
R5	4.7MΩ 1/4W
R6	33kΩ 1/4W
C1	.025μF 200V Ceramic disc. capacitor
D1	FAIRCHILD FD222 (or equivalent)
Q1	2N4250
Q2	2N4343



Application 9. Initial cycle delay diagram.

ACCESSORY CIRCUIT APPLICATION 10

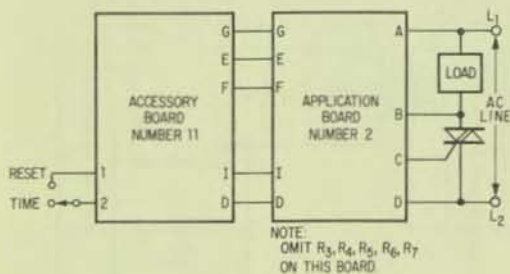
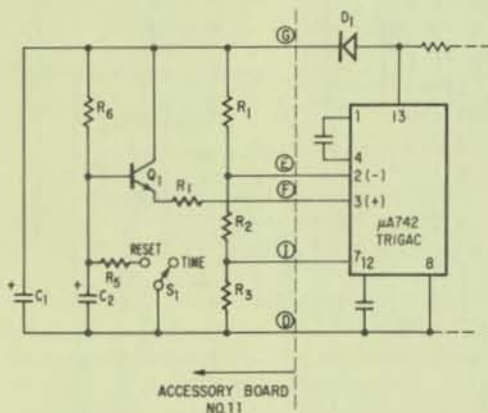
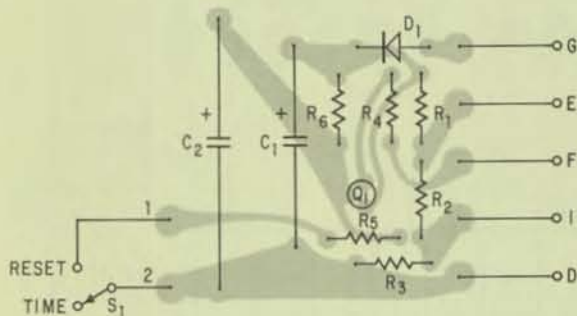
Part Number	Description
R1	10kΩ 1/4W
R2	Sensor (NTC) & adjust Pot. (Total of 10kΩ)
R3	10kΩ 1/4W
R4	10kΩ 1/4W
R5	100Ω (increase if more hysteresis is desired)
R6	100kΩ 1/4W
Q1	2N4250 (or equivalent)



Application 10. Open sensor detector.

ACCESSORY CIRCUIT APPLICATION 11

Part Number	Description
R ₁	47kΩ 1/4W
R ₂	100kΩ 1/4W
R ₃	1kΩ 1/4W
R ₄	47kΩ 1/4W
R ₅	100Ω 1/4W
R ₆	Timing Resistor (See Text)
C ₁	10μF 25V Electrolytic Capacitor
C ₂	Timing Capacitor (See Text)
D ₁	FAIRCHILD FD222 (or equivalent)
Q ₁	FAIRCHILD SE4010 (or equivalent)
S ₁	SPDT Switch



PARTS LIST, THREE PHASE CONTROL SYSTEM (PRINTED CIRCUIT BOARD)

Part Number	Description
C ₁	.01/200V Mylar Capacitor CDE MCR-2S1
C ₂	.0/100V Mylar Capacitor CDE MCR-2P1
C ₃	5/50V Electrolytic Capacitor Sprague TE-1303
C ₄ , C ₆ , C ₈	.47/100V Mylar Capacitor CDE MCR-2P47
C ₅ , C ₇	.047/100V Mylar Capacitor CDE MCR-2S47
D ₁ , D ₂ , D ₃	FAIRCHILD FD-333
D ₄ , D ₅	FAIRCHILD FD-333
IC ₁ , IC ₂ , IC ₃	μA742
R ₁	39k 1/4W 10% Resistor
R ₂	10Ω 1/4W 10% Resistor
R ₃	220k 1/4W 10% Resistor
R ₄ , R ₅	680Ω 1/4W 10% Resistor
R ₆ , R ₈	47k 1/4W 10% Resistor
R ₇ , R ₉	10k 1/4W 10% Resistor
R ₁₀	22k 1/4W 10% Resistor
T ₁ , T ₂	Sprague 11Z13 Pulse Transformers

PARTS LIST, THREE PHASE CONTROL SYSTEM (OFF-BOARD CIRCUITRY)

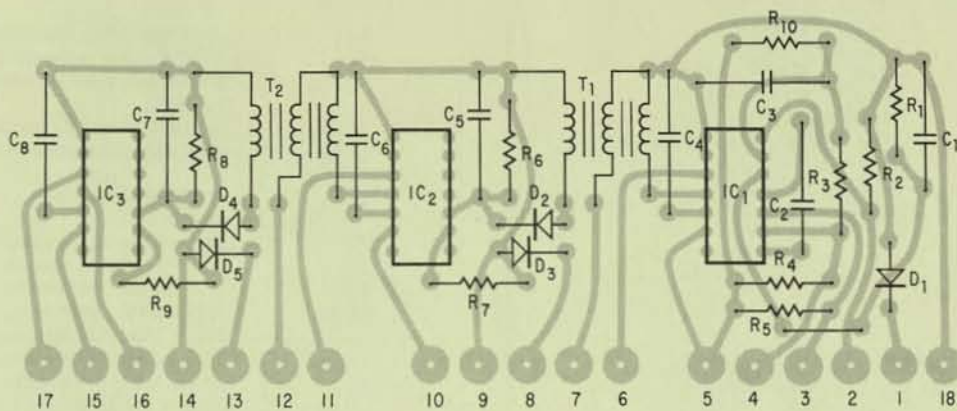
Part Number	Description
C ₉	20/450 Electrolytic Capacitor/Sprague TVA-1709
D ₆ , D ₇	1N4004
Q ₁ , Q ₂ , Q ₃	2N5445 RCA Triac
R ₁₁ , R ₁₄ , R ₁₉	15k 5W Resistor, Dale RH-5 15k
R ₁₂ , R ₁₃ , R ₁₅	10k 5W Resistor, Dale RH-5 10k
R ₁₆	25k 5W Resistor, Dale RH-5 25k
R ₁₇	1.5k 1/2W 10% Resistor
R ₂₀	1k 5W Resistor, Dale RH-5 1k
R ₂₂	1k 10 Turn, Linear Taper Pot

PARTS LIST, THREE PHASE CONTROL SYSTEM (MISC. COMPONENTS)

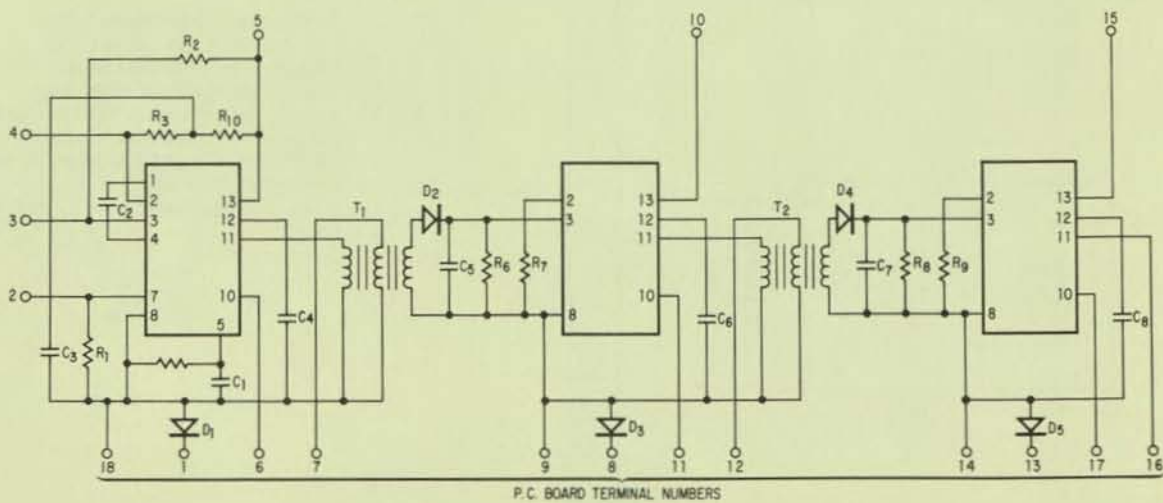
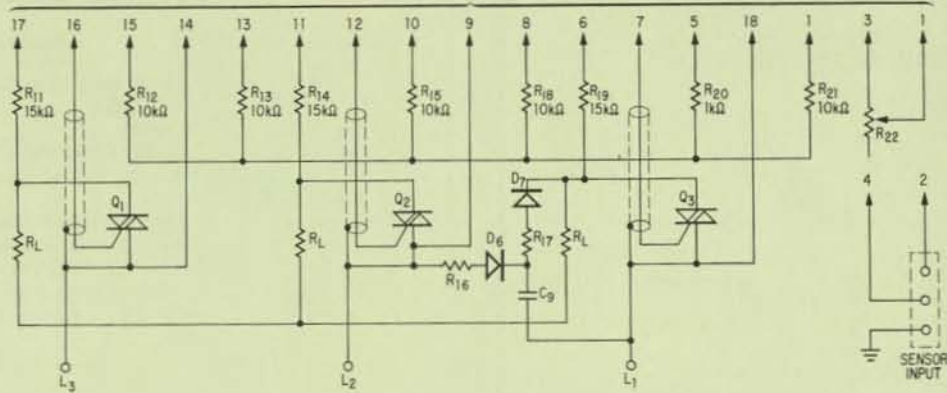
Quantity	Description
1	Cinch-Jones 3-140 Barrier Strip
2	Cinch-Jones 4-150 Barrier Strip
3	Wakefield NC 432k Heat Sinks
3	Marco-Oak VM-308-8 Pilot Lamps
1	Vernier Dial, Microdial 1370 or equivalent
12	Wakefield 103 Heat Sink Insulators
12	3/8" x 1/4", Tapped 6-32 Spacers for Above
1	BUD CU-622 Chassis
1	BUD PA-1138 Panel

Application 11. Time delay relay.

Application 12. Three-phase controller Y or Δ.



PRINTED CIRCUIT BOARD TERMINALS



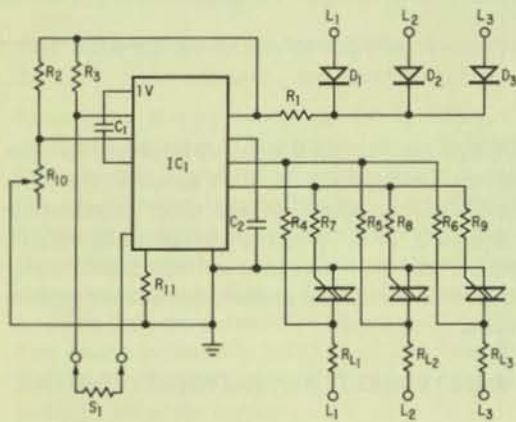
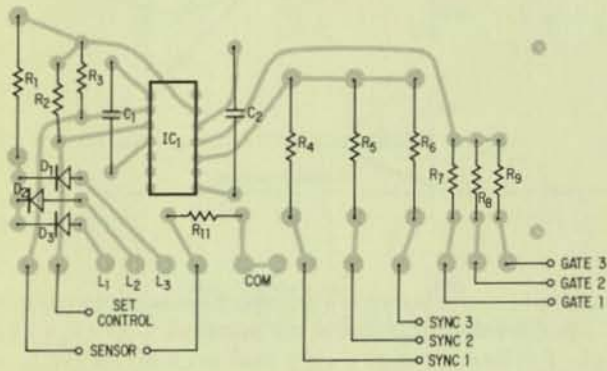
P.C. BOARD TERMINAL NUMBERS

Application 12. Three-phase controller Y or Δ.

APPLICATION 13

3 ϕ CONTROLLER, SINGLE TRIGAC

Part Number	Description
C1	.1/100V Mylar Capacitor
C2	.22/100V Mylar Capacitor
D1, D2, D3	1N4004 Diode
IC1	FAIRCHILD μ A742 "TRIGAC"
R1, R4, R5, R6	10k, 2W, 10%
R2, R3	10k, 1/4W, 10%
R7, R8, R9	24 Ω , 1/4W, 10%
R10	"Set Control", 10k Pot
R11	Hysteresis Control Selected Value
S1	Sensor, Nom, Value = 10k, External



Application 13. Three-phase controller – single TRIGAC.

V. MISCELLANEOUS

A. USE OF THE TRIGAC WITH NONRESISTIVE LOADS

A few comments are necessary on use of the TRIGAC with inductive or capacitive loads.

Capacitive Loads

For capacitive loads with leading current phase angles of more than 10° , the TRIGAC should be operated from a DC supply. (DC supply operation is covered in section IV-D of the Handbook.) Particular care should be taken with loads of this type to prevent destruction of the power thyristor due to excessive di/dt current rise just after turn-ON. This factor may dictate the use of two SCR power switches (for bidirectional control) or a series saturable reactor to restrict turn-ON current rise.

The limiting factor for the TRIGAC when operating with capacitive loads is whether or not time is available under all operating conditions to charge the storage capacitor, (C_1 in Applications 1, 2, 3, and 4) to its peak voltage. This must be done before the first trigger pulse is required after the line voltage has dropped below +21 volts (during its positive excursion). See also the following note on inductive loads for information on added external components.

Inductive Loads

Operation of the TRIGAC with inductive loads requires special treatment in two areas: proper limiting of the rate of rise of the power thyristor's T_2 - T_1 voltage, and control of the effect that this has on the TRIGAC's synchronizing signal.

When switching a resistive load, the power thyristor experiences a zero crossing transient turn-ON voltage that rises at the rate:

$$\frac{dv}{dt} = (2\pi F) (V_{P_{line}}) \quad \text{Where } \frac{dv}{dt} \text{ is in volts/second}$$

F is in line frequency in Hz
 $V_{P_{line}} = 1.41 V_{line_{RMS}}$

For a 110 VAC, 60Hz supply voltage, a dv/dt value of approximately 0.06 volts/microseconds is produced. However, inductive loads produce transients with much greater rates of rise. Figure A shows typical turn-OFF conditions:

During turn-OFF, the T_2 voltage of the triac attempts to instantaneously rise to the line voltage as the current waveform crosses zero. A check of Figure A shows that this can coincide with the peak of the applied line voltage. In this situation, the only limitation on the rate of rise of T_2 is the stray capacitance in the load and in the triac. This rate of rise, which can be higher than 10 or 20 volts/microsecond, is so high that it tends to be coupled internally in the triac in such a way that the unit is continuously held ON. Triac specification sheets generally set the critical value for this internally coupled turn-ON under the heading "dv/dt (commutating)" and include with it a recommended value for an external RC suppression network of the configuration shown in Figure A. Presently available triacs are capable of turning OFF reliably with transients ranging from 2 to 5 volts/microsecond.

The very high dv/dt appearing at the T_2 terminal is coupled to the TRIGAC via the synchronizing signal resistor, R_1 . Because this rapid rate of rise may cause malfunction of the TRIGAC's

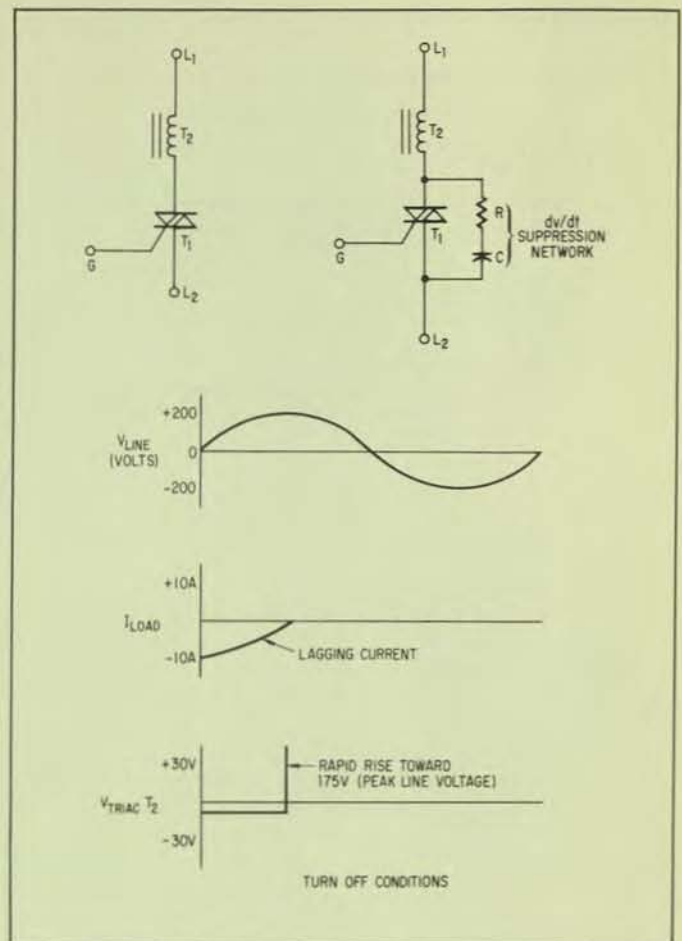


Fig. A. Turn OFF transient - inductive load.

synchronizing switch, an additional terminal has been supplied for the required suppression. This terminal, the 'sync gate' (pin 9) provides correct operation with most inductive load situations when a $0.1\mu F$, 25 volt capacitor is connected between it and ground (pin 8). This capacitor may also be useful when very noisy line conditions present unwanted signals at the synchronizing terminal.

B. A NOTE ABOUT THYRISTOR TYPE STRUCTURES

Since an understanding of thyristor cells is required before the TRIGAC and its associated circuits can be properly grasped, this brief review is presented. (See Figure B-1)

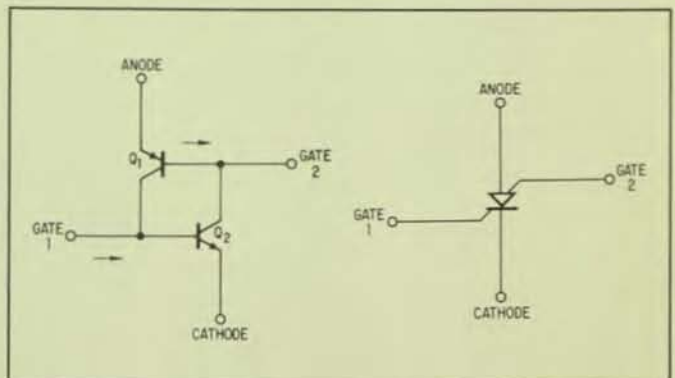


Fig. B-1. The basic thyristor - integrated circuit cell.

This circuit operates according to the equation:

$$I_{ANODE} = \frac{I_{CB01} + I_{CB02} + \alpha_1 I_{Gate1} + \alpha_2 I_{Gate2}}{1 - (\alpha_1 + \alpha_2)}$$

(where gate currents in the direction of the arrows are positive)

The relationship between α_1 , α_2 and the respective collector currents can be illustrated by a graph of the type shown in Figure B-2.

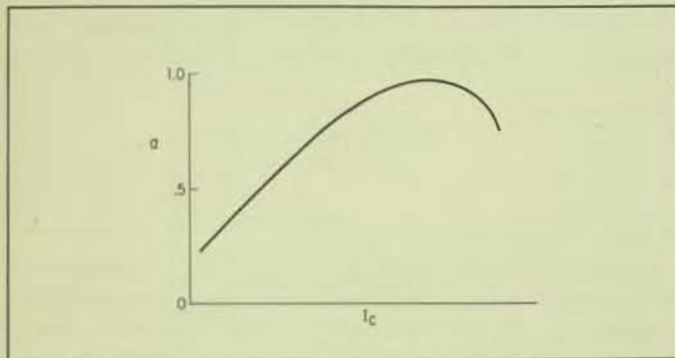


Fig. B-2.

As current of the sense shown by the arrows applied to either gate (I_{G1} or I_{G2}) increases, the collector current for both transistors rises until the term $(I_{G1} + I_{G2})$ approaches 1. At this time the right hand side of equation (1) rises rapidly and anode current is limited mainly by external circuit resistance.

A better 'feel' for these events can be had from inspection of the circuit:

1. Assume that there is no connection to Gate₂, that the anode terminal of the transistor pair is blocking a positive voltage, and that a current in the direction of the arrow is slowly applied to the Gate₁ terminal.
2. As this gate current is increased from zero, transistor Q₂ will be gradually turned ON. However, since there is no connection to Gate₂, Q₂'s collector current also serves as the base current for Q₁.
3. This results in the slow turn ON of Q₁. Now the base drive for Q₂ has two sources: The original gate drive and Q₁'s collector current.
4. The additional increment of Q₂ base current due to the Q₁ collector current, causes Q₂ to turn even further on, and results in a stronger base drive for Q₁.
5. A rapid escalation of the two base-collector current drives both transistors into virtual saturation, and the voltage at the anode collapses.

For most practical purposes, the anode-cathode circuit has transformed from a condition analogous to an open switch to a low impedance "closed circuit".

The overall transfer characteristic of the circuit is represented in Figure B-3.

Note that if gate drive to the circuit is removed after turn-ON, the thyristor will continue to conduct. However, if anode current is subsequently lowered to a value below that required to hold both transistors in 'latch', then the unit will return to its OFF or open circuit condition. This current is identified as I_{HO} on the transfer characteristic.

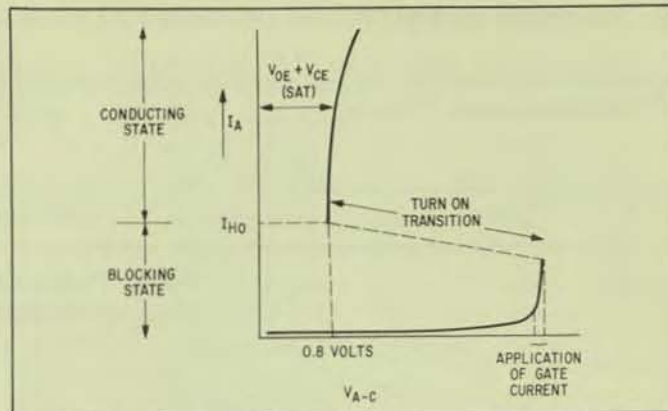


Fig. B-3. Thyristor transfer characteristic.

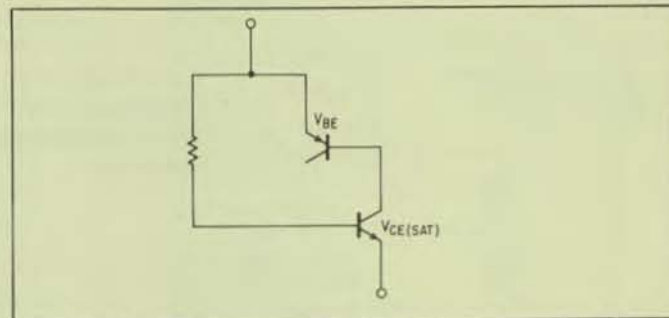


Fig. B-4. ON condition equivalent circuit.

For the time proportioning mode of operation, a switch with an accurately controlled turn-ON voltage is required*. This is represented in the thyristor-two transistor analogy by adding a zener diode to the Gate₂ terminal. (See Figure B-5)

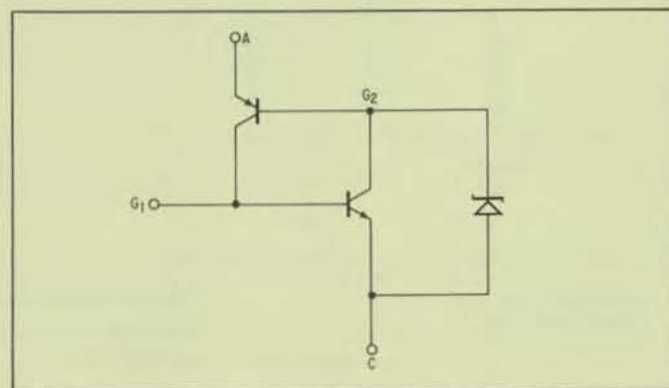


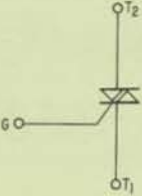
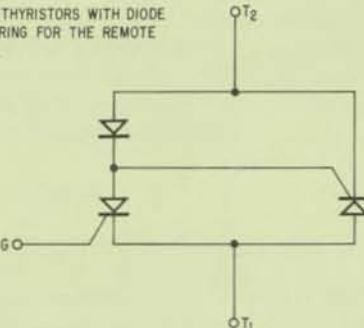
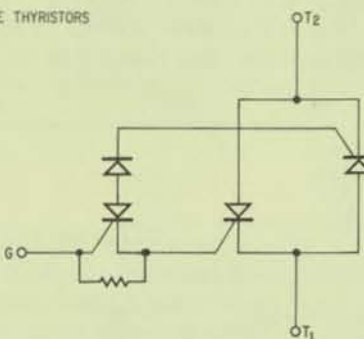
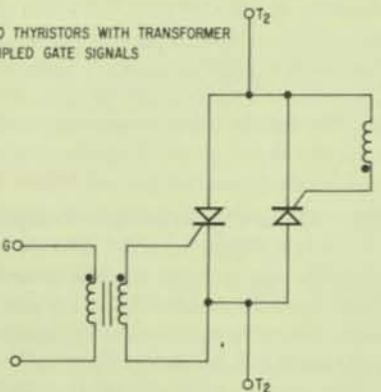
Fig. B-5.

Current through the zener will now be equivalent to applied drive to Gate₂. The thyristor will then turn ON whenever its anode voltage exceeds the Q₁ V_{BE} voltage plus the breakover voltage of the zener. Since both of these voltages are predictable and repeatable under normal circuit operating conditions, the thyristor-zener serves as a stable threshold switch.

*For a detailed discussion of the time proportioning function see Application 3.

C. FULL WAVE OUTPUT POWER SWITCHES FOR USE WITH THE TRIGAC

All of the switches shown below will produce reliable ON - OFF full wave zero control when used together with the TRIGAC output (pin 11) pulse.

SYMBOL/CIRCUIT	APPLICATIONS	COMMENTS
<p>TRIAC</p> 	<p>Standard bidirectional thyristor output power switch.</p>	<p>Useful for most applications, although limitations in cost, heat dissipation, or transient immunity may make the inverse parallel SCR circuits below more attractive.</p>
<p>TWO THYRISTORS WITH DIODE STEERING FOR THE REMOTE GATE</p> 	<p>For low power/low cost full wave switching, or higher power applications in which load symmetry is not critical.</p>	<p>The left SCR does double duty: It serves as a power switching element, and also as a third-quadrant gate drive for the remote SCR. The diode is necessary to steer the right SCR's gate current, but does produce load voltage assymetry.</p>
<p>THREE THYRISTORS</p> 	<p>For higher power bidirectional switches requiring symmetry.</p>	<p>The two main conduction SCR's (2 & 3) are power types. Low current SCR 1 supplies gate drive at the beginning of negative half cycles.</p>
<p>TWO THYRISTORS WITH TRANSFORMER COUPLED GATE SIGNALS</p> 	<p>All applications in which two SCR's are more attractive than a single triac.</p>	<p>The additional cost of the transformer may make the circuits above more attractive.</p>

Two of the circuits listed rely on the 'third quadrant' operation of SCR's as remote-based PNP high voltage transistors. For a more detailed treatment of this technique, request FAIRCHILD Application Brief 114 - 'A New Gate Drive System for Bidirectional SCR Circuits'.

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National
Semiconductor
Corporation

Twenty Years

20

Silicon Valley

*A look back
at the people, products
and technology
that helped shape one
of the world's leading
electronics companies.*

National Semiconductor Corporation

Long before the invention of the transistor and the integrated circuit, "Silicon Valley," as it is known today, was famous more for its prunes than its silicon. There was only one major semiconductor manufacturer in the Valley when, in 1967, Charlie Sporck was named president of National Semiconductor, an ailing transistor company.

"National was essentially bankrupt," recalls Sporck. "So we cut costs wherever we could — while trying to build up a whole new product line at the same time." Within one quarter, the company became profitable.

Though National was originally based in Danbury, Connecticut, the new management team was based in California — along with a growing labor pool of circuit designers and process engineers. Consequently, National's headquarters moved to Santa Clara and work began on a new line of proprietary integrated circuits.

"We had about 100 people in Santa Clara," says Sporck. "That's not too many, considering the intense product development we were doing, but everybody felt a part of the effort to survive and succeed and grow."

Sometimes that effort meant packing products for shipment at the end of the month. "I guess I'm probably one of the few CEOs who has spent time in the shipping department," says Sporck. "But in that first year, everybody did whatever it took to get product out the door." By the end of the year, in 1968, sales increased 53 percent to more than \$11 million.

Over the past 20 years National has shared in periods of phenomenal growth, industry downturns, and technology "firsts." In meeting the challenges of new markets, the changing needs of our customers, and the threat of foreign competition, National has continued to evolve.

In the 1970's part of that evolution included a major change in direction. National entered the systems business.

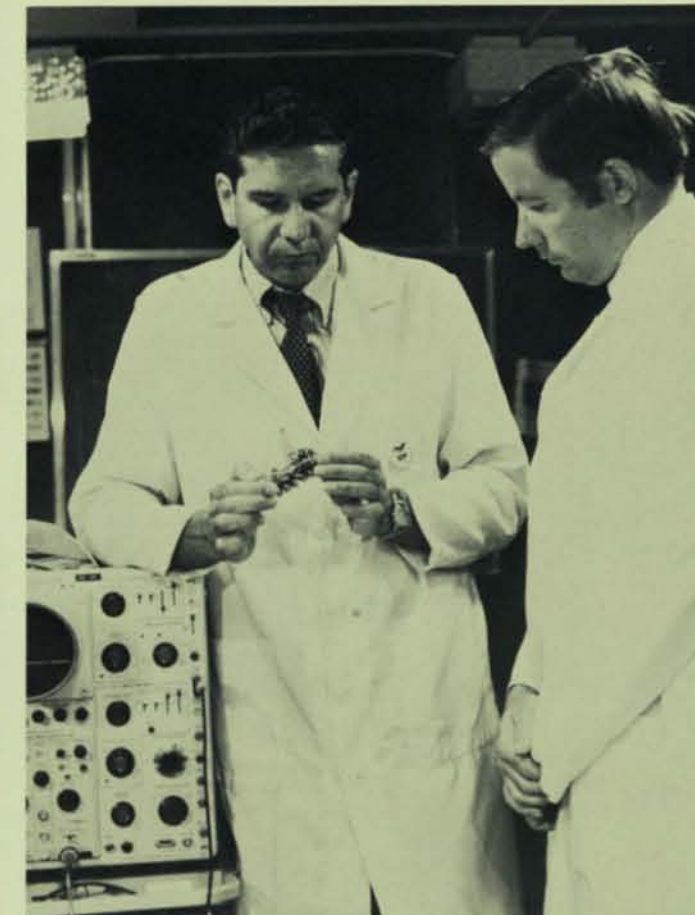
"Our decision to enter the systems business was an important factor in our success," says Sporck. "A strong systems business not only softens the cycles of the semiconductor industry, but also helps us better understand the needs of our systems customers." By the end of the 1986 fiscal year, the company's Information Systems Group, which includes National Advanced Systems, DATACHECKER/DTS and Microcomputer Products, accounted for more than 40 percent of National's total sales.

Another important factor in the company's success is *people*.

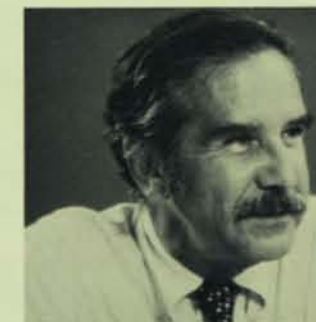
"We've always recognized the simple fact that people are the key to success in this company," says Sporck. "From the very beginning, we wanted to make National the kind of company where innovation is encouraged and rewarded, where ideas can take shape without a lot of the roadblocks you find in big companies."

Continuing success in the years ahead also depends upon National's renowned manufacturing capability and its increasing investment in R&D and proprietary products.

What lies ahead, Sporck predicts, is a company "considerably larger than it is today, one that is relatively balanced between systems and components."



President and CEO Charlie Sporck with Chairman Peter Sprague—nearly 20 years ago.



"In the next 10 to 20 years I see a company relatively balanced between systems and components."—Charlie Sporck, 1986.

M I L E S T O N E S

1967*

Charlie Sporck was named president of National Semiconductor and the company moved its headquarters from Danbury, Connecticut, to Santa Clara, California. Work began on a line of proprietary integrated circuits, including the LM100 linear op amp. Today, National is the world leader in the linear market.



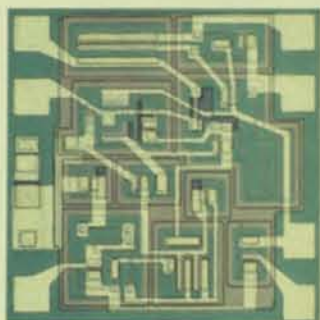
In less than two years National introduced dozens of proprietary ICs. (Above: The Digital Devices design group.)

1968

Sales increased more than 53 percent as more than 30 linear products were introduced, along with two new product lines — Logic and MOS Memory. Also, construction began on the 29-acre "National Industrial Park," the site of today's world headquarters.

1969

Sales more than doubled and profits soared 65 percent. To increase market share in Europe and the Far East, the company began construction on facilities in Germany, Scotland and Singapore.



National's early success was based on proprietary products like the LM100 linear op amp.



World headquarters in 1967 was one small building with a leaky roof.

1970

As facilities were completed around the world, the number of employees more than doubled — to 3,320. Today, the number is 10 times higher.

1971

National broadened its technology base with the development of new CMOS, NMOS and bipolar processes.

1972

Investments in facilities and equipment more than quadrupled during the year. Microprocessors were introduced, along with memory systems and hybrid devices. Wafer fabrication facilities expanded in Santa Clara and Scotland.



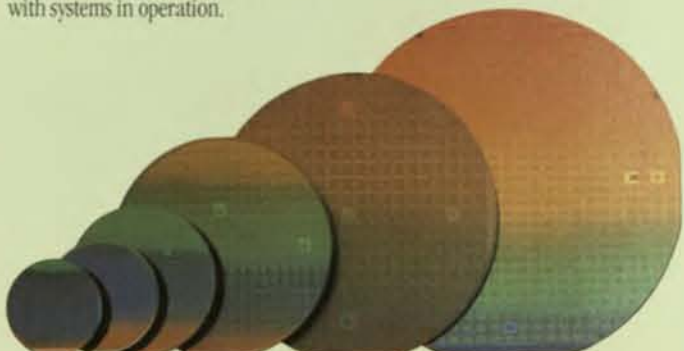
A high-volume manufacturing capability has always been one of National's enviable strengths.

1973

Realizing the potential of electronic systems in the retail industry, National introduced a line of DATACHECKER® point-of-sale systems. Totally upgradeable (a unique feature at the time), DATACHECKER systems soon became the preferred product of the top 10 supermarket chains. On the semiconductor side, assembly plants were completed in Penang and Malacca.

1974

Sales more than doubled, giving National a growth rate exceeding that of its top three competitors. DATACHECKER also made records — in the rate of new installations and in the number of supermarket chains with systems in operation.



After 20 years wafers are not only bigger, but better.

1975

Though plagued by an industry slowdown, component sales were down only 4 percent, compared to 25 percent throughout the industry. National introduced the first commercially available 16-bit microprocessor system and patented BI-FET™ a revolutionary design process.

1976

State-of-the-art 4-inch wafers began rolling off a new multimillion-dollar fabrication line in Utah, and an assembly plant was completed in the Philippines.

1977

National achieved a record in low-cost assembly, due in part to leading-edge automated assembly techniques. System products expanded with the creation of the Computer Products Group (later to become National Advanced Systems and the Microcomputer Products group).

1978

Development was under way on a low power, high performance CMOS process — what National calls *microCMOS*. Other industry firsts included COPS™ microcontrollers, the DP8350 CRT controller, and the ADC0816 single-chip data acquisition system.



NAS is the fastest-growing supplier in the IBM-compatible mainframe market.

1979

R&D spending increased 57 percent and included development of the revolutionary Series 32000® 32-bit microprocessor family. In Tucson, Arizona, construction began on the industry's first U.S. facility dedicated to the manufacture and test of high reliability ICs for the military/aerospace market.

1980

National Advanced Systems, a subsidiary formed from National's Computer Products Group, began marketing and servicing IBM-compatible mainframe computers and peripherals.

1981

Sales passed the \$1 billion mark. New products included advanced microprocessors like the 32-bit Series 32000 family and the microCMOS NSC800™ family; DNR™ a noise reduction circuit for audio/radio applications; and Digitaltalker®, a speech synthesis chip later used in DATACHECKER's POSItalker™ "talking" cash register. National Advanced Systems introduced its leading-edge AS/9000 series of IBM-compatible mainframe computers.



1982

microCMOS product offerings continued to grow and work began on a CMOS 64K static RAM for the U.S. Defense Department's VHSIC (Very High Speed IC) Program. National Advanced Systems installed more medium- and large-scale general purpose computers than any other IBM-compatible mainframe supplier.

1983

In a move that marked the beginning of a new era in IC development, National introduced the Customer Specific Products group — specifically, gate arrays. Customers now have the ability to create their own proprietary products using National's design facilities.



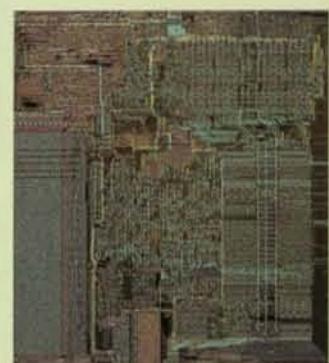
Today, National's world headquarters includes a 14-acre employee park.

1984

National introduced the industry's first commercially available, single-chip, 32-bit microprocessor, the NS32032. With the acquisition of Data Terminal Systems (DTS) in late 1983, a new DATACHECKER/DTS diversified into nearly all retail markets throughout the world. Today, there are over 400 installations in Europe alone.

1985

More than 100 proprietary products were introduced, including a family of advanced peripheral devices for local area network and mass storage control applications. National Advanced Systems introduced the Series 32000-based AS/Gateway, a network product for the office automation and distributed processing markets.



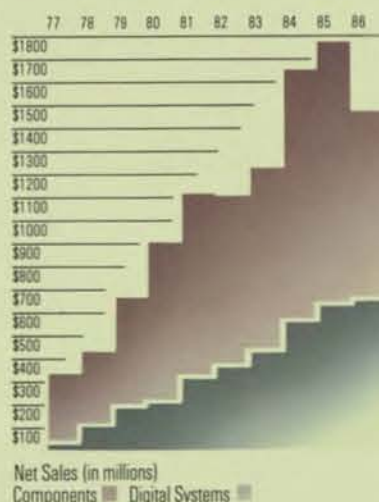
The NS32032 was the industry's first commercially available, single-chip, 32-bit microprocessor.

1986

Despite the semiconductor industry downturn, R&D expenditures remained at record levels, and more than 75 percent of National's new products were proprietary. The company also opened a 6-inch wafer fabrication plant in Texas for the production of microCMOS devices. NAS began shipping its new Alliance Generation AS/XL Series of mainframe computers, the most powerful general purpose mainframes commercially available. And DATACHECKER/DTS unveiled a revolutionary retail scanning system to the growing European market.



CMOS process technology, used here to manufacture gate arrays, is being used in all of National's new VLSI designs.



DATACHECKER, BI-FET, COPS, SERIES 32000, NSC800, DNR, Digitaltalker, and POSItalker are trademarks of National Semiconductor Corporation.