Once upon a time, in a place known as Testingland, there was a big company. Fairchild, as the company was called, was a veritable giant in the field of semiconductor testing. But a kind and benevolent giant. And so, when Fairchild stumbled upon an old and dusty tome hidden deep within the walls of a wise old engineer's office, it decided to share it with the world. And so our story begins...

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Logic in Testingland—a tale of measurement techniques

Repair costs grow larger, timing margins small, but without IC testing there may be no profits at all.

Martin Marshall, Associate Editor

The road to Testingland is a strange one indeed. One path leads in directly, while another is quite long, twisted and agonizing to follow. Both paths proceed to the same point—the entrance to Testingland—but since the second is so strewn with broken epoxy and the bones of Chapter XI companies it is naturally the path that most companies choose to follow. The journey begins with a designer—George, and a concept—the Gaussian curve.

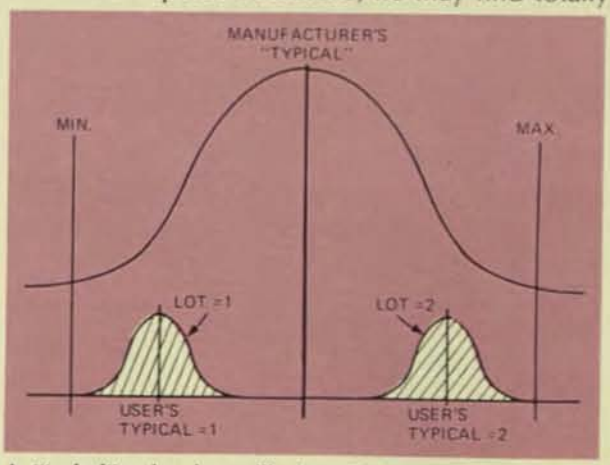
George orders IC's from both distributors and manufacturers. He gets his parts and the spec sheets to go along with them, as well as the good will of the vendors. Now only one question remains: Will the IC's work in his applications, and will they keep working when his product is in the field?

Once upon a spec...

Spec sheet numbers represent the manufacturer's best efforts to characterize the IC. However, those efforts are often made on prototype devices and on samples taken from the first few lots. Subsequent process changes and field reports of performance limitations may modify the specs on an IC, but several runs of devices may be shipped before the new paperwork is generated.

Volume testing, to the IC manufacturer, means performing GO/NO-GO tests that try to select "good" devices, 99% of which fall somewhere between the minimum and maximum published limits for a given spec. The "typical" spec quoted by the manufacturer and widely taken as gospel by designers means typical for the manufacturer's engineering characterization samples, not necessarily for the user.

In his shipment George may very well receive IC's from one lot clustered at the minimum spec, as well as another lot clustered at the maximum. George, like most designers, would like to believe the "typical" spec published by the manufacturer. He often cannot afford the performance loss of designing against top-and-bottom worst case specs. Therefore, he may find totally



A "typical" value is an illusion. The manufacturer usually generates his "typical" specifications by averaging data over sample lots. On the other hand, a user's shipment may contain units from two different production lots with greatly differing specs.

unacceptable deviant lots that the manufacturer correctly labels totally acceptable.

A stacked deck?

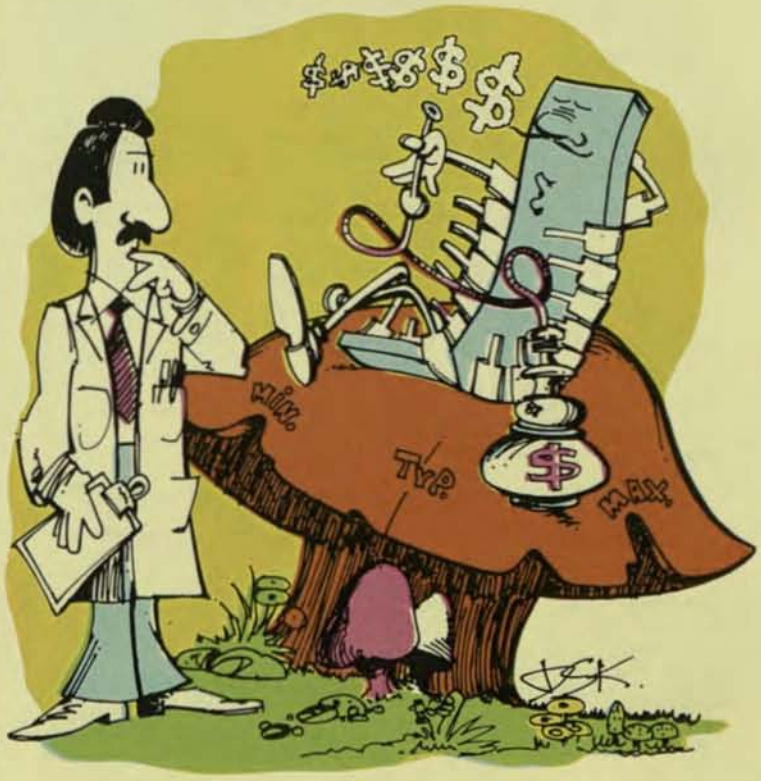
When George lost the probabilistic game of designing against the manufacturers' bell curves, he felt that the deck was stacked against him. He suspected the manufacturers of carving out the middle of the bell curve for their best and highest volume customers. He ushered in a team from the manufacturer's test lab and showed them the IC's socketed in malfunctioning boards. The manufacturer's test team then proceeded to show him their test data on the IC's and suggested that George had found a "misapplication" of the IC's limits. His test method, they politely suggested, was just a pack of pc cards.

They pointed to extra screening programs of their own and of independent test labs, each of which multiplied the cost of the IC's to George severalfold. They then exited in a train, with words of encouragement to George and congratulations to each other, leaving George with the choice of scrapping the pc design, modifying it, or paying a premium for "selected" IC's.

"There must be a better way," thought George, and he began contemplating how he could take up a collection for an incoming inspection IC tester. He could collect up to $100 for each bad IC caught by the tester that would otherwise wind up in the finished product, and he could collect up to $1000 for each IC caught by the tester that would have otherwise failed in the field. He could also collect from the design department for redesign time saved, as well as from the purchasing department for saving the extra cost of selected IC's. He might even collect from the marketing department for providing them with a fundamentally more reliable product to sell. With these visions dancing in his head George could just begin to see the entrance to Testingland.

"Use your head."

At the entrance to Testingland was a crossroad. Next to it was a post with signs reading LOGIC, MEMORIES, MICROPROCESSORS, LINEARS, PCB's and HYBRIDS, running off in all directions. Under the signpost was a bell-curve shaped mushroom and on top of it, at a spot marked "typical," sat an IC. The IC was smoking a pile of money while its pins kept bending and seemingly talking among themselves.



"How can I test you?" asked George, who looked around to make sure that none of his colleagues overheard him talking to an IC. The IC thought for a few nanoseconds, blew out a smoke ring in the shape of a dollar sign, and answered, "That depends on which forms of me you want to test."

"I'm trying to test a UART, a calculator chip, a watch chip, some ROM's, shift registers, gates, CCD's, adders, parity generators, decoders, flip-flops and small scratch pads," said George.

"UART?" said the IC.

"Yes, I am," said George.

"Well, then, you had best follow the path marked LOGIC. You'll find a Cheshire cat there who has slept near every IC baking oven from Texas to New Jersey to California, and he knows all my faults as well as I know his," said the IC. "One branch of each path leads to the general purpose tester area, but you can decide that when you get to the Hall of Testers. On the underside of this bell curve are your testing budget constraints. One side makes the budget larger, the other makes it smaller. Take what you need, but don't use it all. You'll need the rest for software."

"How will I know how much testing is enough for me?" asked George.

"Use your head," said the IC, and it crawled off into the stock room.

"The very thing I would have said."

Not far along the path George saw a Dormouse sleeping by the side of the road. "Are you here to test logic too?" asked George.

"Hmm?" said the Dormouse, "Oh yes, the very thing I would have said." And it went back to sleep.

"Good!" said George, loudly enough to wake the Dormouse, "then perhaps you can tell me which is the best method."

"Method?" said the Dormouse, who thought for a moment, "Well, that depends on what you want to do."

"I want to test logic," answered George.

"Oh, no one is allowed to test logic around here except mathematicians and philosophers—and occasionally politicians," said the Dormouse.

"No, I mean logic *IC's*," said George.

"Oh yes, just what I would have said," said the Dormouse, "logic IC's. I've been testing logic IC's for almost ten years. I started with a couple of generators, an attenuator and a scope. Now I have an automated system."

"What is your system comprised of?" asked George, who was hoping it wouldn't be too elaborate.

"It's simple," said the Dormouse, "I built it myself. It has a power supply, some amplifiers and attenuators, and some switching circuitry that feeds everything into a simple, commercially bought socket. It's quite versatile. If I want to change from a 14-pin socket to a 16-pin socket—or even to a 24-pin socket, if I ever need one—all I have to do is unsolder the wires from all the pins and solder them back onto the new socket. I have some more switching on the output pins that channels a chosen output signal to a DMM."

"What is automatic about it?" asked George.

"Ah, that's the part I'm proudest of," said the Dormouse. "I have a little hexadecimal keyboard that tells the power supply what voltage I want on the input pin and on the device power pin. Then all I have to do is switch a lever to indicate which pin is my input pin and another lever to indicate which pin is my output pin. I push a button that says 'test', the measurement appears on the LED's of the DMM, and my logic is tested."

"I see," said George.

"Yes, they are," said the Dormouse.

"Can you measure propagation delays?" asked George.

"No, but I can force voltage or current and measure current, voltage and resistance," said the Dormouse.

"How do you know the parameters will be the same when your logic is operating at rated speed?" asked George, who was still thinking about his malfunctioning pc boards.

"I was told that tests were run in the late 1960's which showed a correlation between dc and ac parameters," said the Dormouse.

"Twinkle, twinkle, twinkle, twinkle..."

"How do you verify the truth table?" asked George.

"Oh that's easy," said the Dormouse. "I just multiplex the input voltage to the appropriate pins and switch the DMM to successive output pins. Eventually I get the output word, and then I switch the input pins and measure another output word, and so on. It **is** rather slow, but it does the job."

"Can you load the output pins?" asked George.

"Oh sure," beamed the Dormouse, "all I do is get under the socket and solder resistors between the appropriate output pins and ground."

"What about capacitance?" asked George.

"Life is so short," mused the Dormouse, "why worry about everything?"

"You are happy with your system, then?" asked George.

"Oh no, not at all," said the Dormouse. "It's very noisy, and since it is a one-of-a-kind system, it's much more expensive than it should be. I have other things to do with my time than design test systems, so I figure a test-system vendor can design a similar system both better and cheaper. That's why I'm here, to find one."

"Well, then, you had best come with me," said George. "I'm going to see the Cheshire cat, who knows all about IC's and testers. It can tell you which system to choose."

"I'm not sure that would be wise," said the Dormouse, whose whiskers were standing on end. "My parents taught me that it is dangerous to take advice from cats—Cheshire or otherwise."

"You can hide behind my pocket calculator and listen in," suggested George. The Dormouse reluctantly agreed, and to calm itself on the journey it sang George a song. It went:

"Twinkle, twinkle, microcircuit
How I wonder if you work it
Pulses running in my system
Do you catch or do you miss 'em?
Twinkle, twinkle, microcircuit
How I wonder if you work it."

And before long the Dormouse was asleep again, interrupting itself only occasionally with a "Twinkle, twinkle, twinkle, twinkle..."

"Do cats eat bats?"

Not very far along, George came upon an enormous and obviously complex piece of branching logic, and sitting on one of the branches was a Cheshire cat. It grinned from ear to ear and kept swishing its tail, which had the color markings of a precision 50Ω resistor.

"Do dc parameters correlate with ac parameters?" asked George, hoping to obtain a more recent report than those alluded to by the Dormouse.

"Yes," smiled the Cheshire cat, "for SSI and for some bipolar MSI. Beyond that, no one knows for certain, but suspicion is that they don't.

"Why is that?" asked George, who noticed that the Dormouse's ears were sticking up over the ENTER key in his pocket calculator.

"Because of the rabbits," said the Cheshire cat, "they control the clock rate and signal flow. The faster they go, the more power they draw. The more power they draw, the more current they carry. The more current they carry, the greater the crosstalk induced on neighboring pins. Also, the more current they carry, the hotter they get, and the greater the chance of such effects as aluminum migration. Be especially wary of the latter. The more the aluminum migrates, the greater the chance that your device will start talking backwards—and that may not always be what you want it to do."

The Dormouse, who never believed anything that wasn't second-sourced, whispered "Tell me about the rabbits again, George."

"Later," whispered George, who asked the Cheshire cat, "What will a dc tester buy me, then?"

"It will catch about 1-2% bad devices," said the Cheshire cat. "The IC manufacturer expects that on stabilized products. One percent is his AQL (Acceptable Quality Level) and another 1% is mislabeled or mishandled during shipment. You must remember that all IC manufacturers claim to test all of their devices dc before shipment." The Cheshire cat winked and swished its tail.

Searching for the truth

"What are my alternatives?" asked George.

"To find out if a device is telling you the truth you should examine its truth table," said the Cheshire cat. "That requires pulsed input patterns and some form of output pattern recognition. If you have N input pins then you have 2^N possible input patterns, or 2^{MN} if M is the level of sequential logic on the IC. If 2^{MN} becomes too big a number—which is bound to happen on 24-pin devices and larger—then you must make compromises on the length of the test pattern.

"To detect the output patterns you can use AND gates and a counter, or voltage comparator systems. The generic term for these systems is that of 'ac functional tester'. The subgenus classes are 'real-time' and 'computer-rate', which means MHz and kHz data rates, respectively. Beyond that, everyone invents his own terminology."

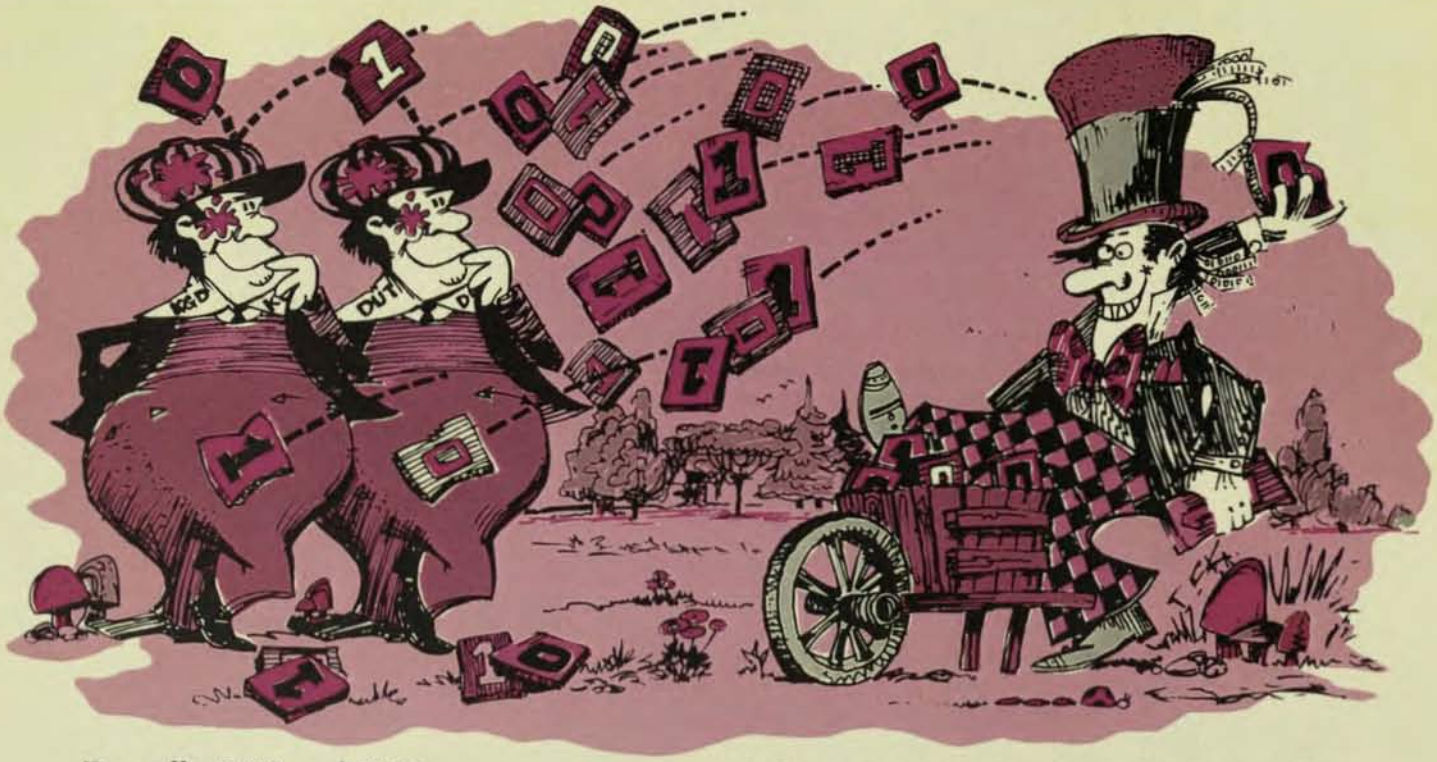
George noticed that the Dormouse was standing on the calculator staring up into the rather large glowing eyes of the Cheshire cat. For irises the Cheshire cat had red, yellow and green LED

arrays that flashed whenever it spoke like an Aurora Borealis. The Dormouse was transfixed and swayed slowly at the clock rate of the Cheshire cat's eyes.

"Perhaps you could direct me to some ac functional testers," said George, who was dropping the Dormouse into his pocket and hoping to appear nonchalant. The Dormouse fell asleep immediately upon impact, interrupting itself only occasionally to purse up its whiskers as if to say "twinkle."

"They are on the other side of the door," said the Cheshire cat, who disappeared with a swish of its tail.

George looked around for a door, but could not see one until he looked down at the trunk of the logic tree. There was a small door marked "ac testing." The Dormouse could fit inside it easily, but George—no way. So George ate a piece of the IC's mushroom marked "Budget under $20,000," and suddenly became so small that he could actually ride on the shoulders of the Dormouse, that is, if the Dormouse was not continually falling asleep.



Tweedle DUT and KGD

On the other side of the door George heard a good deal of splattering and munching, followed by shouts of "One-one! Zero-zero! One again!" The source of the shouting seemed to be a creature with two heads arguing with itself, but upon closer examination George could see that it was actually two creatures with one head, each of whom was somehow linked by an arm. One had KGD (Known Good Device) embroidered on its collar, while the other had DUT (Device Under Test), but aside from that they seemed identical.

"I know a ONE when I taste one," said the one marked KGD, "and since I taste the outputs of the Known Good Device that means that **you** must be wrong."

"And I know a ZERO when I taste one," said the one marked DUT.

"You see there, you admit tasting a ONE and thinking that it is a ZERO. Ergot, your logic is fault!" said the KGD.

"That's 'ergo', without the 't'," said the DUT, "which proves that **your** logic is faulty."

"If I prefer tea with my ergo that is my own affair," said the KGD.

"No way," said the DUT.

"No how," said the KGD, and they both did a little dance.

"Perhaps if you told me what you were arguing about," said George, "I could help you resolve the question."

"The question has yet to be solved, let alone resolved," said the DUT. "We each sample the output signals of different IC's and then compare our results with each other. If the units are indeed functionally identical then our results should match. If not, then they assume that my Device Under Test is wrong and that his supposedly Known Good Device is right. My IC is rejected. My question is, how do they know that the KGD isn't itself only marginally acceptable in its specs? If it is, then it can be used to reject IC's that are good, but simply not on the same side of the bell curve as the KGD."

"What is the testing mechanism?" asked George, who was trying to decide whether it was polite to mention the cherry sauce that was smeared on the faces of both KGD and DUT.

A tray of tarts

"It's quite simple," said KGD. "The Mad Pattern Generator throws clusters of cherry tarts at the input pins of the IC's being tested. If the tarts have cherry sauce in them, then they are ONE's. If they don't, then they are ZERO's. The cherry sauce is electrically charged and it enters the IC with the waveshape of its pastry shell. It comes out the output pins according to the truth table of the IC. That's what we taste to test."

"Where does Pattern Generator get the cherry sauce for his tarts?" asked George.

"Why, from Cherry Hill, of course," said both DUT and KGD simultaneously. DUT added that once a year everyone in the IC tasting business goes to Cherry Hill to hold a symposium, and that everyone returns with wheelbarrows full of new cherry patterns to throw at their IC's.

"How do you capture the output information?" asked George, who noticed that the Mad Pattern Generator was off having tea with his tarts.

"That depends upon our configuration," said the DUT. "In our simplest form we are AND gates that lead to a single-input counter. The Mad Pattern Generator first throws a particular pattern

of tarts at a socket occupied by the KGD, then the counter records the total number of output transitions. Next the DUT replaces the KGD and the Mad Pattern Generator throws the same pattern of tarts at it. If the counter shows the same total, then we label the DUT 'accepted'."

"We can also take other forms," said KGD. For example, we can be voltage comparators—one for each output pin—that are strobed by a signal from the Mad Pattern Generator. He throws an extra tart directly at us, and this tells us exactly when to compare the output cherry sauce with our reference cherry sauce. On the less expensive system our outputs are compared directly by a parity tree. If our outputs differ, the parity tree pumps cherry sauce up to the red LED marked NO-GO."

"On more expensive systems," added DUT, "KGD is replaced by a stored pattern in a computer. I compare the patterns I taste to those of the theoretical performance of the IC as simulated by the computer. If my taste differs from that of the computer's stored pattern, then I take a stack vector out of my pocket, write on it, and throw it back into the computer. That lets the computer know which pattern I was on when the device failed. I then turn on the red NO-GO light and go to sleep until the next test."

At this point George noticed that KGD was gone—or rather, half-gone, since only his legs remained. They stuck out from under a large fur carpet, which was really no carpet at all but rather the Dormouse, who had fallen asleep again and rolled over on KGD.

George and DUT pulled out KGD, who announced that it was tea time. They all danced in a ring around the Dormouse and KGD and DUT skipped off, singing:

"We once had a tester of dc
And found the programming quite easy
But with dynamic chips
It's so easy to slip
That now we test functional ac."

The hatful of patterns

By now the Mad Pattern Generator had finished his tea and was busily arranging his tarts. George stood nearby, waiting for an appropriate time to speak. The Mad Pattern Generator spoke first. "Your hair wants cutting," he said, although he hadn't looked at George.

"It's too late for that now," said George, "too many of us have graduated from college and assumed important positions in the industry." "Besides," he added, remembering, "my hair **is** short."

"Well, then it needs to be grown longer," said the Mad Pattern Generator, conclusively.

George thought the conversation had gotten off on the wrong footing, so he tried again. "Why do they call you Mad?" he asked.

"I'm not, really, though I sometimes seem to be when I'm throwing out random patterns," said the Mad Pattern Generator. He pointed to his hat and whispered confidentially, "Actually, very few of the patterns are truly random. Most of them are generated according to a Grey code that I keep in the lining of my hat. The Grey code is a pseudorandom formula that allows only one input pin in a pattern to change at a time. If it were truly random then any number of input pins could change state."

"Why do you use random patterns—pseudo or otherwise?" asked George.

"If the test system is inexpensive or if the logic I'm testing is too complex, then I must compromise somewhere," said the Mad Pattern Generator. "Psuedorandom patterns are generated from a formula—which means they can be as long or as short as you want. If you want to throw all possible patterns at a given IC, not only do you get long test times, but also a long and complex software program."

"Is there any advantage to that?" asked George.

"There are advantages to an entirely systematic approach," said the Mad Pattern Generator. "For example, those interested in low-budget, GO/NO-GO testing generally put together pseudorandom pattern generation with comparison output detection using a KGD. This saves them an enormous amount of software preparation. Those interested in fault diagnosis and very accurate tests buy a more expensive, computer-controlled system with large pattern storage capability, word generators and stored theoretical truth tables rather than KGD comparisons.

"To compare the efficacy of the two approaches, by the way, Continental Testing Laboratories tested 634 marginal IC's of the 7483-type on both an Alma 480B and a Fairchild Sentry 610. The Alma system, which is a GO/NO-GO type, caught 192 IC's that failed the truth table, while the Sentry

ALMA 480B		SENTRY 610	
PASS	FAIL	PASS	FAIL
354	192 Functional	338	223 Functional
	50 VOH		42 VOH
	30 VOL		24 VOL
	3 IIH		3 IIH
	5 IIL		4 IIL
354	280	338	296
TOTAL = 634		TOTAL = 634	

Test results can vary somewhat, depending on what kind of equipment you use. In this case, Continental Testing Laboratories compared results from an Alma 480B lower cost GO/NO-GO tester to those from a general-purpose, sophisticated Fairchild Sentry 610. Under test were 634 marginal 7483-type TTL 4-bit binary full adders.

610, which is in the bit tester class, caught 223."

"You seem quite sane to me," said George, who was busily taking notes.

"Actually, there is one thing that makes me mad," said the Mad Pattern Generator, whose eyes turned yellow as his breath began to steam. "It's these tarts. Just look at them. There's hardly any waveshape at all on a good many of them. I've seen 25% overshoot and more on some of them. It's one thing to make sure that your IC's can withstand sloppy input signals, but it's quite another to obscure test results with the inaccuracies of the test system. You'd be surprised at how many people buy test systems without even observing the waveforms in the different parts of the system. In the larger, more expensive test systems they have state-of-the-tart pulse generators with complete control over the shape of the tart shell. In some of the less expensive ones you get things that are supposed to be square tarts, but which really look more like flapjacks."

The Mad Pattern Generator then went back to breaking off undesirable pieces of tart shell and throwing them at passing IC's.

Bake, burn, spin and dunk

When George went back to look for the Dormouse, all he found was the fading grin of the Cheshire cat. Suddenly he heard cries of distress coming from the other side of a thicket comprised of Kelvin twisted-pair connections. Carefully he worked his way through the thicket, until he beheld one of the most awesome sights in all of Testingland: There before him was a large lake, and floating in it was an armada of LSI comprised of SOS/CMOS, high-powered Schottky TTL, I^2L, CML, and even ECL. These devices were being bombed and strafed by a test engineer whose epaulets read "JAN." Jan then scooped the IC's up and dropped them from great heights onto a minefield, where they were run over by a tank. George caught up with him just as he was pulling pin 14 of a 1/10 CMOS decoder chip back into a half-nelson.

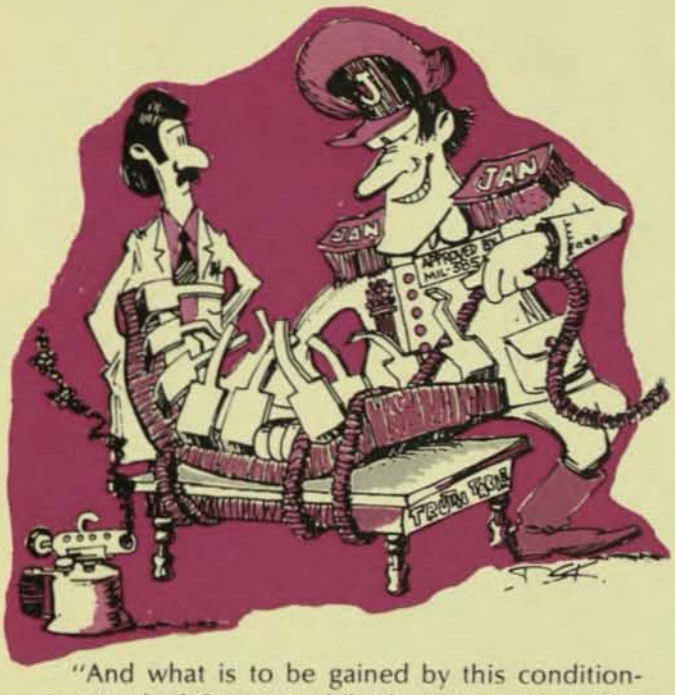
"What kind of testing is this?" asked George.

"I have not yet begun to test!" shouted JAN. "This is only the conditioning." Next he took out a torch and began chasing an LSI around a table, whose only inscription was "TRUTH."

MANUFACTURER	TOTAL TESTED	PERCENT FAILED	REASON FAILED
7400 SERIES			
Signetics	1M	5%	ac parameter (T_{pd})
Fairchild	500k	5%	ac parameter (T_{pd})
		7%	mechanical (bent leads, marking)
National	550k	3%	ac parameter (T_{pd})
		10%	mechanical (bent leads, marking)
TI	750k	2%	ac parameter (T_{pd})
		4%	mechanical (solderability, bent leads)
SHUL			
TI	1.5M	2%	ac parametric
	2.1M	0.9%	ac parametric
		4%	mechanical (plating)

Of the devices that passed this screening, only 0.05% failed after assembly.

Test results from a major IC user reveal quality variations between similar products from several major semiconductor manufacturers. These IC's are intended for computer-related applications, or approximately reliability class C (commercial) of MIL-STD-883. The company uses a combined dc, real-time functional and ac parametric test system. The results shown are for illustration only, because quality levels can shift over periods of time.



"And what is to be gained by this conditioning?" asked George, while the JAN was tying the pins of the LSI down to the table.

"About 1-2% extra bad IC's on the average, but there is no average. Every IC is an individual case," said JAN, and he held a box marked "DANGER, RADIATION" over the IC, which by now was squirming on the truth table.

"When Uncle Sam pays as much as he does for a Rel A or Rel B grade IC he has a right to get one that works. That's why the military standard 883-38510 program was put into effect. We find conditioning a good way to drop out IC's that work in the test socket, but that have short lifetimes in the field."

"What kind of conditioning do you do?" asked George.

"We use stabilization bake, thermal shock, and mechanical shock," said JAN, who began jumping up and down on the IC, "as well as temperature cycling, centrifuge, hermeticity, and burn-in. These achieve an accelerated life in the IC's before any electrical tests are performed. Sometimes we use irradiation as a substitute for thermal heat."

"What kind of electrical tests do you recommend?" asked George, who had begun to brace himself by nibbling on a piece of the IC's mushroom marked, "Budget over $100,000."

"That depends on the reliability level we want to test for," said JAN. "Grade C is for the more complex commercial circuits, such as those inside a standard minicomputer. Simpler, noncritical circuits, such as those with only ten IC's on a pc board, can get by with class D testing. Class D, incidentally, is the one recommended by the IC manufacturers. Going up, class B IC's often cost five times their commercial counterparts and are used in important groundsupport equipment. Class A IC's, which often cost ten or more times their commercial counterparts, are used in aircraft, satellites and other critical applications. If an IC doesn't pass any of these tests we label it 'class E' and sell it to the Red Army."

"Off with its head!"

At that point the pin that JAN had been pulling on broke. "Aha! Off with its head!" he exclaimed, and began pulling out the LSI's other pins. "Now, on electrical tests," he continued, "we always perform the standard dc parametric tests on every IC. Whenever possible we run all of the 2^{MN} input patterns to verify its truth table. For class A and B devices we will often run extended pseudorandom patterns as well.

"We also have direct single-shot ac parametric measurement capability. We bought it because of our need to test class A and B devices; however, we use it for class C devices as well. If we didn't have the single-shot equipment, we could still measure propagation delays on a repetitive basis to within ±2 nsec by varying the strobe delay on the ac functional comparators.

"We measure critical ac parameters partly for the same reason that we perform accelerated life tests. Tests run by my colleague George Nelson of the Naval Research Laboratory, among others, have indicated a direct correlation between those IC's with marginal ac parametric values and those that have early life failures in the field. With ac functional testing, even if we know the given pattern that failed an IC, it's often hard to guess the physical cause of the failure. With direct ac parametric measurement it is much easier.

"One place where ac parametric measurement has helped greatly has been with CMOS. The quiescent power consumption test—basically a dc test, but performed under ac conditions—has been shown to be a definite indicator of early life

TYPE PART	TOTAL TESTED	FAILED DC	FAILED RT FUNCTIONAL	FAILED AC PARAMETRIC	TOTAL FAILED
TTL/SSI	8328	5.9%	0.7%	4.5%	10.9%
TTL/MSI	905	8.0%	0.8%	21.6%	27.4%

The total failed is less than the sum of the parts (tweedle-dee?) in this data from George Nelson of the Naval Research Laboratory, Washington, DC, because some IC's failed more than one kind of test. George produced this data after running dc parametric, real-time functional and ac parametric tests on each of 9233 TTL devices. The IC's were screened to reliability class B of MIL-STD-883.

failures. On faster logic, such as ECL, I^2L and Schottky TTL, measurement of propagation delays—and sometimes even switching times—can be an important binning factor for IC's that have passed both the dc and truth table tests."

"How much does ac parametric equipment add to the cost of a test system?" asked George, who had been holding an ECL/MSI while JAN delivered a series of body punches to it.

"For us it costs an extra $80,000 to $100,000," said JAN, "but that was because we needed clean subnanosecond risetime tarts to test ECL. Cherry sauce channeling in the one nanosecond region is a very sticky business."

A question of insight

"Can you give me any hints on improving my IC reliability using a lower cost tester?" asked George, who was beginning to wonder if such a thing was possible.

"Yes," said JAN, who took George aside and looked around to make sure none of the IC's were listening. "Call up the IC manufacturer—or better yet, visit his plant—and ask him which production lines have been certified by the government for 38510-type parts. Since reliability is a built-in characteristic, the chances are that commercial IC's built on the same production line as military JAN parts will receive more attention than the same parts built on a different production line by the same manufacturer. Often the only difference between a commercial IC and

a JAN part is the paperwork involved—that, and the differences that my tester can detect."

George thanked JAN, who was ceremoniously awarding purple medals marked "JAN part—reliability level A, B, etc." to the assembled survivors among his IC's. As George turned away, he caught a glimpse of the face of the Cheshire cat materializing on the horizon. He pursued it through a dense fog, which became lighter as he reached the crest of a hill. There he could begin to see not only the Cheshire cat's face, but the moon as well. When the images coincided, George said to the cat, "You have led me through the measurement techniques, but what I need now is a test system. Where is this Hall of Testers that you mentioned?"

"Before introducing you to the Hall of Testers it was first necessary to give you the insight to understand them," said the Cheshire cat. "The Hall of Testers is before you." And with that the Cheshire cat dissolved into the face of the moon.

The fog lifted and George looked down to find a pile of test system brochures sitting on his desk. Under the brochures he found a chart with notes appended to it and signed by the Cheshire cat. George sipped some black coffee and started to read. □

HALL OF TESTERS: LOGIC DIVISION

Company	Model No.	Price	Circle No.	NOTES
FIXED-PATTERN FUNCTIONAL TESTERS				
Alpha Data, Inc. 20750 Marilla St. Chatsworth, CA 91311 Phone (213) 882-6500	1416	$855 to $985	150	Low cost is achieved using DUT and KGD comparison. Limited-length Grey code patterns serve as input stimulus.
Electro Scientific Industries, Inc. (ESI) 13900 N.W. Science Park Dr. Portland, OR 97229 Phone (503) 646-4141	1248	$630	151	Counters are used to create 65-kHz word rates that are limited in length. Grey code stimulus feeds an output transition counter for extremely low-cost testing. Uses KGD vs. DUT, 14-pin, 16-pin.
Fut-heuristic Devices Box 1117 Reseda, CA 91335 Phone (213) 342-1800	"Evaluator"	$300	152	Low-cost ac functional tester. Uses KGD comparison and 12-stage ripple counter stimulus. Clock rate is 250 kHz, but since it is divided by 12 input pins, pattern rate is 20 kHz. Corresponding output pins of KGD and DUT are wired to exclusive-OR gates. Comparison errors lasting longer than 600 to 800 nsec will be detected. Input patterns are hardwired on KGD board; five are supplied. Socket has 16 pins.
Fluke/Trendar Corp. 500 Clyde Ave. Mt. View, CA 94040 Phone (415) 965-0350	3010 2000A 1010A	Under $10K	153 154 155	Basically PCB test systems, but are also available with IC socket interface. The systems feature Grey code input stimulus at 4-MHz data rates and output total transition count for comparison of DUT and KGD.
BENCHTOP TESTERS				
Alma, Div. of Develco, Inc. 530 Logue Ave. Mt. View, CA 94043 Phone (415) 968-3903	380C 480B	Under $10K	160	Both dc parametric and 10-kHz functional tests are performed using manual programming. 20V p-p swings allows CMOS testing. Failed parameter and failed pin are identified.
Fairchild Systems Technology 1725 Technology Dr. San Jose, CA 95110 Phone (408) 998-0123	901	$8K	161	Plastic cards program Grey code tests as well as dc parametric tests. A counter is used for KGD and DUT transition comparisons, but unlike the other units the 901 also counts the number of periods that the output was in a logic ONE state. 10-MHz rate.

Macrodata 6203 Variel Ave. Woodland Hills, CA 91364 Phone (213) 887-5550	104	$8K	162	Functional comparisons to an algorithmically-generated truth table at rates to 5 MHz are made using comparators, not counters. Input patterns may be Grey code or other formula-generated sequences.
Siemens/Computest 186 Wood Ave. S. Iselin, NJ 08830 Phone (201) 494-1000	716A 720	$3K to $14K	163 164	The 716A is a dc parametric tester. Voltages and currents are forced at the inputs and read on a DPM. The 720 series tests both dc parameters and Grey code functional patterns at 50-kHz and 100-kHz rates. Comparators are used rather than transition counters.
Biomation/Sitek 10411 Bubb Rd. Cupertino, CA 95014 Phone (408)255-9500	3200A	$7K+	165	Both dc parametric and Grey code functional tests are performed at up to 400-kHz data rates. Pattern depth is 44,000 patterns. KGD and DUT comparisons are used.
Teradyne, Inc. 183 Essex St. Boston, MA 02111 Phone (617) 482-2700	J133C	$5.7K	166	DC functional and dc parametric tests use comparison of KGD and DUT. Both a device card and a family card are required to establish logic levels and loads for each device.
Technology Marketing, Inc. (TMI) 3170 Red Hill Ave. Costa Mesa, CA 92626 Phone (714) 979-1100	5000	$17.5K to $27.5K	167	Premiered here before your very eyes, this microprocessor-controlled system tests ac functional patterns up to 10-MHz rates. Datalogging includes overriding addresses and data without disturbing the test patterns or test speed.
SPECIAL-PURPOSE TESTERS				
Teradyne, Inc. 183 Essex St. Boston, MA 02111 Phone (617) 482-2700	J197 J193 J325	$32.5K $35K $98.5K	168 169 170	The J-197 is designed to test calculator chips. It tests dc parameters for both voltage and current. The J-193 does the same for watch chips, and the J-325 tests dc parameters and dc functions for ECL and CMOS.
COMPUTER-CONTROLLED TESTERS				
Datatron, Inc. 1562 Reynolds Ave. Santa Ana, CA 92705 Phone (714) 540-9330	44 45 50	$100K to $250K	171 172 173	The Hustler series systems are all computer controlled. Model 44 is a dc parametric and functional system. Model 45 tests ac functional patterns at 10 MHz. Word generators and comparators compare the output response to a stored truth table. Model 50 combines Models 44 and 45.
E-H Research Laboratories, Inc. 575 11th St. Oakland, CA 94604 Phone (415) 834-3030	4500 4800	$300K+ range $80K to $150K	174 175	This is the Rolls-Royce of test systems. As such it is for the select few who both need its performance and can afford its price tag. It boasts dc parametric, 10-MHz ac functional, and subnanosecond-risetime ac parametric measurement capabilities. Reliable sources in the field claim 99.95% IC yields after full screening with this tester.
Fairchild Systems Technology 1725 Technology Dr. San Jose, CA 95110 Phone (408) 998-0123	Sentry	$150K to $350K	177	The Sentry is a family of test systems. The Sentry 610, formerly at the top of the line and now replaced by the Sentry II, has the largest sales dollar volume on the test system market. It performs dc parametric and real-time functional tests. Pattern rates on functional tests go to 10 MHz. It is usually described as the Cadillac of the test system market.
Macrodata 6203 Variel Ave. Woodland Hills, CA 91364 Phone (213) 887-5550	154 501	$100K+ range $250K range	178 179	The MD 154 is an engineering evaluation test system built to test up to 48-pin devices at ac functional pattern rates up to 10 MHz. Like the Datatron, Fairchild, and other more sophisticated real-time functional testers, it can also glean propagation delays on a repetitive basis down to TTL speeds. DC parametric tests are also performed. The same is true of the larger MD 501, which ranks with the Fairchild Sentry 610 as one of the most actively marketed test systems.
Mirco Systems, Inc. 2106 W. Peoria Ave. Phoenix, AZ 85029 Phone (602) 997-5931	500	$6K to $18K	176	Intended primarily for PCB testing, but can also be used with IC sockets. Pseudorandom patterns keep cost and complexity down. Unit is intended for GO/NO-GO applications, and is priced to compete with the lower cost benchtop systems, rather than the more sophisticated computer-controlled IC test systems.
TRW/Colorado Electronics, Inc. 3450 N. Nevada Ave. Colorado Springs, CO 80907 Phone (303) 475-0660	System IV	$250K+ range	180	Primarily intended for PCB testing, the System IV can also handle ac functional testing of LSI at speeds up to 50 MHz. Tests hybrids. Pin count runs to 264, each with an individual I/O driver.
Tektronix, Inc. Box 500 Beaverton, OR 97077 Phone (503) 644-0161	3260	$200K+ range	181	This is the Bentley of test systems. It performs dc parametric, subnanosecond-risetime ac parametric and 20 MHz real-time functional tests. Since it uses a DEC PDP-11, it can interface to Tektronix graphic terminals for sophisticated datalogging and engineering characterization.
Teradyne, Inc. 183 Essex St. Boston, MA 02111 Phone (617) 482-2700	J-283	$89.5K	182	The J-283 is a dc parametric and dc functional test system. Its computer also acts as host to options such as the 10-MHz ac functional module (J-277) and the nanosecond-risetime region S-157 ac parametric module. (These options are not included in the price shown.)
Testline Instruments, Inc. 1625 White St. Titusville, FL 32780 Phone (305) 267-7212	2100	$9.8K	183	Performs dc voltage measurements and ac functional comparisons at 37-msec cycle times (giving approx. 30-Hz data rate). Cannot detect hardwired shorts.

Through the memory cells—further explorations of IC's in Testingland

Part 2 of our semiconductor testing series reveals in detail the intricate mechanisms of memory testing.

Martin Marshall, Associate Editor

George was happy with the logic tester he bought after his first visit to Testingland (EDN 1/20/76), but when his company introduced a product line that used a large number of memory devices he knew it was time for another visit. So he picked out a 4k RAM from the stockroom, brought it into his office cubicle and closed the door.

He began contemplating how a colleague at another company had experienced a 43% failure rate on an early shipment of 4k RAM's. Since his friend had not tested the IC's, all the failures were at the pc-board level, costing him over $30,000 to repair the products. Through visions of scattered and malfunctioning pc boards, George could begin to see the entrance to Testingland forming quickly before his eyes.

"Memory is often my business."

Once again the crossroads met near a post with signs reading LOGIC, MEMORIES, MICROPROCESSORS, PCB's, LINEARS and HYBRIDS. Once again a bell-curve shaped mushroom stood in the shade of the signpost, and once again the IC, this time wrapped in an epoxy cocoon marked "Memory," sat atop the bell curve and smoked a

pile of money. Memory sat watching George for a long time, pausing only occasionally to puff out a dollar-sign shaped smoke ring. Finally, George spoke.

"Do you remember me?" he asked.

Memory thought for a few hundred nanoseconds, puffed on its hookah and replied, "Memory is often my business."

"Do you know how to test memories?" asked George.

"I am the memory," said Memory, "and testing is a function more associated with Intelligence. The Cheshire cat is the symbol of intelligence, so he has become the expert on testing."

"I'm more interested in results than intelligence," said George (who had never once mentioned to his colleagues that he had played Hamlet at Yale University), "but I enjoy using intelligence to achieve those results. Where might I find this Cheshire cat?"

Memory blew a stream of smoke into the air that engulfed them both in dreams of the wealth of money to be saved by producing products that work, as opposed to products that don't. George remembered that quality control is an old Yankee tradition that dates back to the cotton gin, not to mention the invention of electricity by the Nordic god, Thor.

"Remember what you are here for."

As George was beginning to doze off into memories of great moments in the history of electronics he saw the face of the Cheshire cat materializing before him. Memory gathered up its bag of money and floated off back into the stockroom, casually remarking, "Remember what you are here for."

The Cheshire cat just sat, grinning from ear to ear, so it seemed to George that starting a conversation was up to him. He asked, "How can I test my memories?"

"The best way to test memories," replied the Cheshire cat, "is by remembering things. If you remember them well enough, then you can compare them to what you expected to remember. If there is a difference, then your memory is faulty."

"So real-time functional testing is the way to go, then?" queried George.

"Every system that describes itself as a memory tester has either 5-, 10- or 20-MHz functional testing," explained the Cheshire cat. "A dc-only test system is usually not equipped to handle a dynamic chip, but several ac functional systems do add a dc measurement capability and thus can make dc measurements."

"What about timing measurements?" asked George.

"Some people," said the Cheshire cat, "think that direct measurement of access times can be used in conjunction with minimal functional patterns to solve the problems of long test times on large memories. The trouble is, no one is sure yet just which access times are the most critical. And unless you know that you can wind up having as many access time measurements as you do functional patterns, and that is too many."

"What's the big deal about test times?" demanded George, who liked doing things in a straightforward fashion. "It seems that all I need do is to write a ONE into each of the memory cells and then read the whole memory. Then I do the same for ZERO's and I'm finished."

"Failure is where you find it."

"You would be finished," said the Cheshire

cat," but not finished testing. You will only have proved that at least one of the cells in your memory works, and that each cell is not shorted to itself. If all the cells in your memory were wired together they would also pass that test."

"I had a feeling it was a little too easy," said George, "but then, what is the proper pattern?"

The Cheshire cat just grinned and said, "Failure is where you find it. Often a different pattern or set of patterns exists for each failure mode. If you want to find out what has been tried, you should ask the GO/NO-GO player. He supplies the Mad Pattern Generator with ideas for patterns."

With that, the image of the Cheshire cat disappeared, as did the smoke surrounding George. He found himself on a grassy ridge overlooking a large field on which there stood what looked like a giant maze of hedgerows and brooks. Upon closer examination he noticed that the maze was actually quite structured. The main portion of it was square and divided into 64 sections by the rows of hedges. These sections were in turn divided by 64 brooks running perpendicular to the hedgerows, and out of these mazes there stretched 22 hedgerows that led to the periphery of the maze.

"Come in and get me, Chopper!"

George thought how much the maze resembled a diagram of a 4k RAM, with the hedgerows resembling the X-addresses and the brooks resembling the Y-addresses. Suddenly he heard an electronically amplified voice shouting, "All right, Bugs, I know you're in there! Come on out with your address lines up or I'll come in and get you."

George immediately recognized the voice as belonging to the Mad Pattern Generator. He spotted him crouched behind a loudspeaker in a formation of squad cars near the peripheral hedgerows. Another voice shouted from the maze, "Come in and get me, Chopper! You'll never find me in all this mess."

George hurried down the hill to join the Mad Pattern Generator, who now was reading from a paper tape marked with ONE's and ZERO's. George got there just in time to see him pick through a wheelbarrow full of cherry tarts.

"It is the cause."

"He thinks he can hide from me, does he?" roared the Mad Pattern Generator. "Sixteen million patterns I've used up already, but this time I'm going to mash this electrified cherry sauce right in his face!" And before George could stop him the Mad Pattern Generator scopped up an armful of tarts and stomped off into the input hedgerows, shouting "It is the cause. It is the cause, my soul. Oh, let me not name it to you, you chaste formulae. It is the cause."

In the quiet left behind by the Mad Pattern Generator, George heard a soft clicking noise coming from behind one of the squad cars. He followed it to find a test engineer wearing a silk lab coat embroidered with the words GO/NO-GO, as well as Maxwell's equations and silk screens of successive mask changes of the 1103-type RAM. The clicking noise resulted from the engineer placing several little white stones marked ONE and little black stones marked ZERO on a wooden gridwork before him. He set a pattern of stones on the gridwork and copied it onto a paper tape similar to that used by the Mad Pattern Generator.

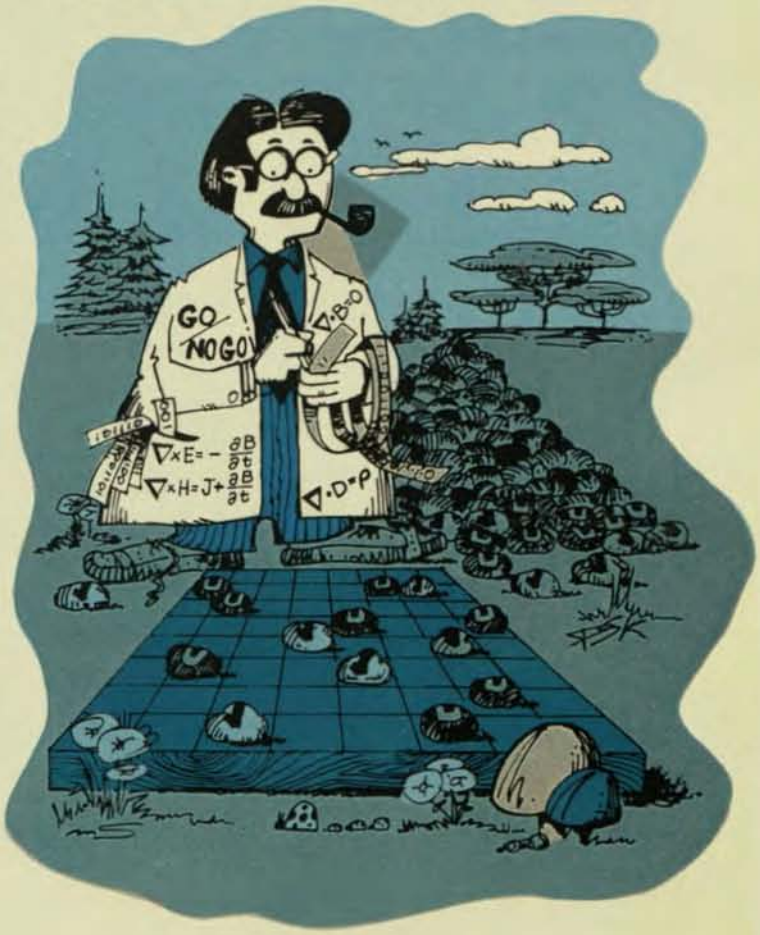
The GO/NO-GO player

George sat watching the GO/NO-GO player's process for a while. Finally, he asked, "How is it that you know the failure modes of a memory?"

"I guess," said the GO/NO-GO player, "but my guesses usually are based on experience." He continued placing ZERO's and ONE's.

"And what is your experience?" asked George.

The GO/NO-GO player, examining the pattern he had just created, answered, "My experience is that most memory bugs cluster into groups, like villagers at a few, easily named hamlets. A few



others roam through the memory like outlaws, and are thus very hard to find. The majority of bugs, I have found, hide in these places:

- Memory cell opens or shorts
- Address decoder opens or shorts
- Access times
- Surrounding cell disturbances"

"How do you determine the patterns that will reveal these failure modes?" asked George.

"On a one-by-one basis," replied the GO/NO-GO player. "No one functional pattern can find all of Bugs' hideouts. The geometry of the memory cell also introduces an unknown factor."

"I would think that the IC manufacturers would supply a detailed description of their memory's internal geometry, so that you could determine the physical effect of your patterns."

"That would be most accommodating," said the GO/NO-GO player, "but, unfortunately, the arrangement of, for example, cell #4095 adjacent to cell #0000 may give one manufacturer an edge over his competitors. He then declares the entire cell geometry proprietary and his users are left puzzling over the true effects of their patterns."

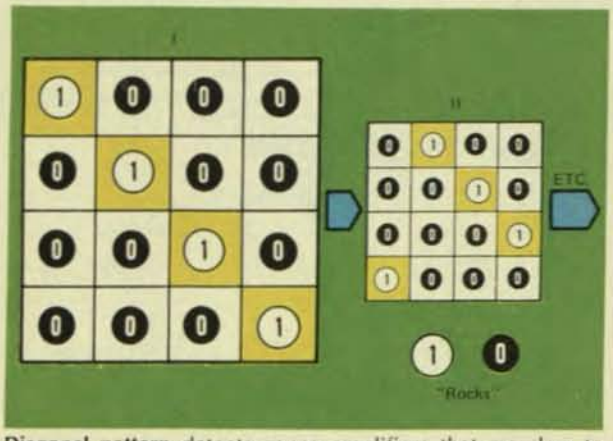
Stone buttons danced upon the grid

The GO/NO-GO player motioned to the gridwork before him, saying "These patterns assume a 64-cell by 64-cell array, with the first cell in one corner and the last cell in the opposite corner. The cell addresses increase in linear fashion. Other memories may have a 32- by 128-cell arangement, or even a dual-16 by 128-cell geometry, and within each the rows and columns may be designated in different orders. Many patterns are immune to variations in cell geometry. Some, however, are quite susceptible and their purpose is thwarted."

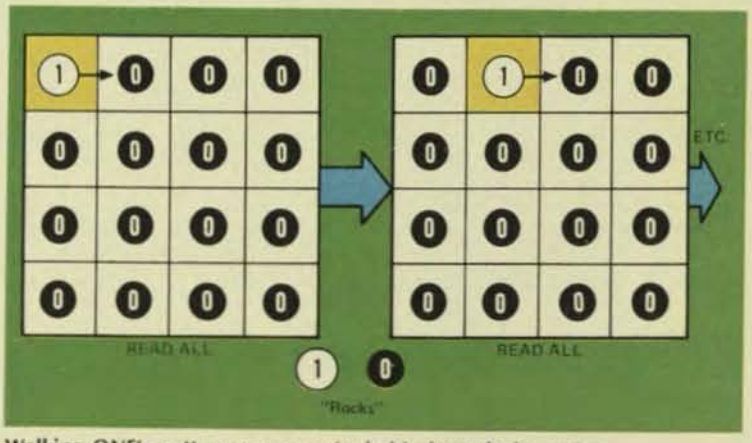
"Can you give me some specific patterns based upon this model?" asked George.

"Certainly," said the GO/NO-GO player. He placed the ZERO's and ONE's on his gridwork so that a diagonal of ONE's stood out against a background of ZERO's. "This is a **diagonal pattern**," he explained. "It verifies that the address decoders are functional. If the address decoding lines malfunction by selecting multiple cells, then a ONE will appear in a cell off the diagonal. If a cell is inaccessible it will eventually appear as a ZERO in a diagonal of ONE's.

He waved his hand over the gridwork and the columns of stones permuted themselves cyclically, so that the diagonal pattern traveled left-to-right across the grid and reappeared again on the left. After each wave of his hand, the GO/NO-GO player noted the contents of all cells on the grid on his paper tape.



Diagonal pattern detects sense amplifiers that are slow to recover.



Walking ONE's pattern moves a single bit through the entire grid, providing a good test of the memory's cell addressing. It also detects slow sense-amplifier recovery.

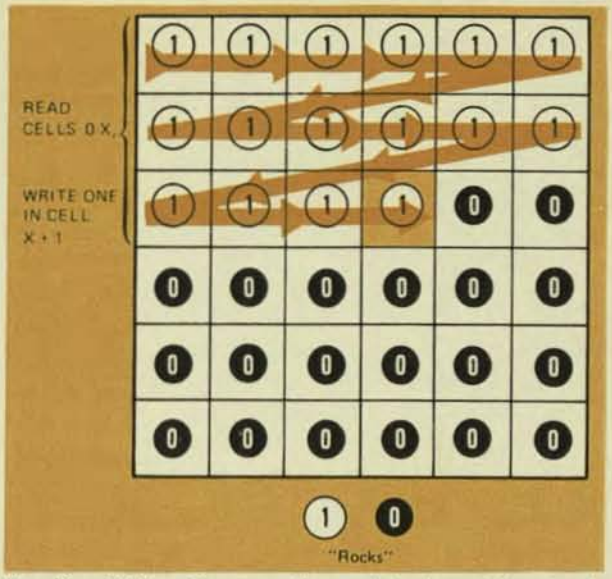
"The diagonal pattern is a special case of the **walking ONE's** pattern," he continued. "In the latter pattern a single ONE is placed into one cell in the array and the other cells remain with their original ZERO's. All the bits are noted (read) and the ONE is changed to a ZERO. A ONE is then placed in the next cell and the process repeats."

George sat opposite the GO/NO-GO player and watched a single ONE progress through the gridwork with each wave of the GO/NO-GO player's hand. "The diagonal pattern is considerably shorter," noted George. "So why use a walking ONE pattern?"

"Bugs is also a very resourceful player," replied the GO/NO-GO player. "If he hides in the sense-amplifier recovery portion, then the diagonal pattern will find him. He will cause a long string of ONE's followed by a ZERO to be noted as all ONE's. If he hides somewhere else in the memory's functionality, then the walking patterns have a better chance to find him. If you wish to compromise on test pattern length then you may try a **marching ONE's** pattern."

Marching to Bugs' hideout

The GO/NO-GO player started with a white



Marching ONE's pattern provides a minimal test of functionality and addressing problems, but is poor at pinpointing difficulties in access times, write recoveries and multiple cell selections. After any test, such as the marching ONE's pattern, is performed, it's often followed by its complement—in this case, a marching ZERO's pattern.

stone in the first position and the rest black. He then waved his hand several times and each time the stone in the next address turned from black to white. After each hand wave he noted only the stones that turned white. "This is a marching ONE's pattern," he said, and he continued the process until all the stones were white. He then reversed the process, turning white stones black. "And this is a **marching ZERO's** pattern. A given pattern is often used with its complement, the same pattern with colors reversed."

"It sounds like you have Bugs' hideouts pretty well covered," said George.

"Simplest wishes," said the GO/NO-GO player, "are sometimes hardest to fulfill. Walking and marching patterns are rich in discoveries of functionality and address hideouts, but poor in locating Bugs when he hides among the access times, write recoveries and multiple cell selections. Observe."

The GO/NO-GO player placed a pattern on the grid. He noted the contents of the first cell and changed the status of the bit. He then observed the contents of a second cell and returned to note the contents of the first cell again. He continued noting the contents of other cells, each time returning to verify that the bit in the first cell had not changed. When he had checked all cells in this fashion he moved to the second cell and changed its bit status. He then repeated the noting process, returning each time to the second cell. He continued until each cell had been used as a reference cell for this "galloping" process.

"This **galloping pattern**," said the GO/NO-GO player, "tests all possible read/read transitions, as well as examining the disturbance caused in other cells by writing in a given cell. It also gives a rough check of access times between any two cell locations."

"Even the best trees bear some poor fruit."

"It's very long," sighed George, "but if it covers all the bases I suppose I can use it."

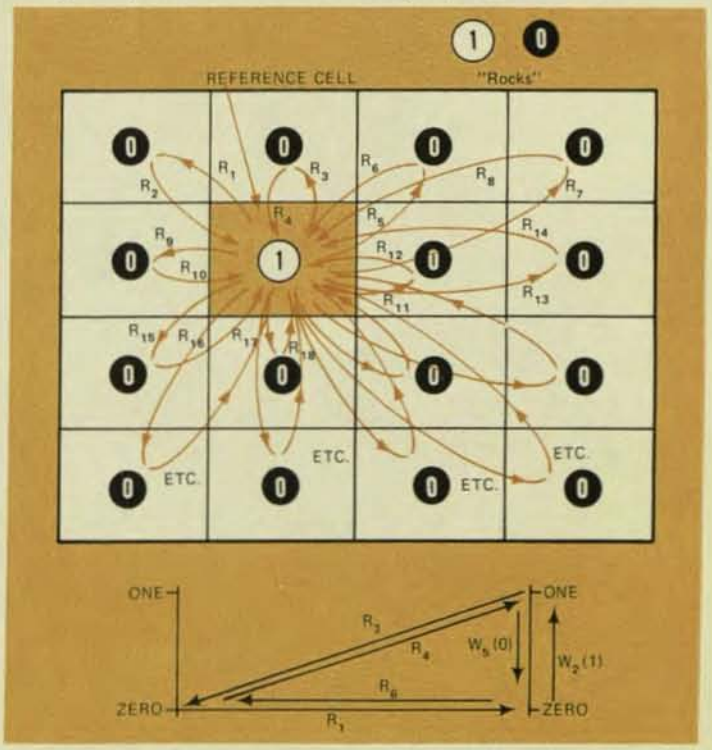
"Even the best trees bear some poor fruit," said the GO/NO-GO player. "This pattern will seek Bugs in access time, functionality, addressing and multiple cell selection. But if Bugs is hiding in a write recovery, then the chances of finding him are poor."

The GO/NO-GO player paused for a moment and considered. "If the cell geometry is known, then I can show you a much shorter galloping pattern." He repeated the galloping pattern process, but this time instead of noting all of the other cells alternately with a given cell he noted only the eight surrounding cells alternately with the subject cell.

"This is a **surround-disturb pattern**," he said. "It has basically the same strengths and weaknesses of the first galloping pattern, except that it checks far fewer access times."

"Is there any way of checking write recovery times?" queried George.

"Yes, but it requires a galloping pattern twice as long," replied the GO/NO-GO player. He noted



Galloping ONE's pattern tests all possible read/read transitions. It also examines the disturbance caused in other cells by writing in a given cell and provides a rough check of access times between any two cell locations.

the second cell, then placed a ONE in it and observed the first cell. Rechecked the ONE in the second cell, he noted the first cell again and changed the ONE in the second cell back to a ZERO. The test engineer repeated the process, each time noting both the first cell and a successive cell into which he had placed a ONE. When that process was completed, he snapped his fingers and the test pattern repeated itself many times, until each cell had a turn to be the reference cell in a series of comparisons, just as the first cell had been.

Tea and porcelain

"This is a **galloping write-recovery pattern**," said the GO/NO-GO player. "It examines every write/read transition in the memory. While it is only a fair test of access times on some memories, it nevertheless is an excellent test of functionality, addressing and multiple cell selection, as well as write recovery."

The GO/NO-GO player then set aside his bowls of stones to offer George some tea. They exchanged pleasantries about the weather and George expressed his admiration for the craftsmanship of the painted porcelain teaware. The GO/NO-GO player informed him that it was from the Chiang dynasty.

After both had enjoyed their tea in silence, George spoke. "I noticed that the galloping write-recovery pattern required $12N^2$ operations to complete, where N is the number of memory cells. On my 4k RAM's that would require at least 90.6 seconds per chip. If I add a galloping ONE/ZERO pattern then each chip ties up my test system for over two minutes."

MEMORY TEST PATTERNS

Pattern	Tests	Comments	No. Operations	Equations*
1. Diagonal (Barber pole)	slow sense amplifier recovery	Minimal Fn test	2N	$\sum_{k=0,N^{1/2}-1} [\sum W(1)\,C_{ij}, R(all), W(0)\,all]$ (all i and all i = j + k)
2. Parity	some address decoder problems	Minimal Fn test	4N	$\sum W(1)\,C_{ij}$ (all ij where ij in binary contains an odd number of ONE's), $\sum W(0)\,C_{ij}$ (all ij where ij in binary contains an even number of ONE's), R(all)
3. Marching I/O	functionality of cells	Cannot check all interactions. Min. Fn. test.	8N	$\sum_{all\ ij} [RC_{ij}, W(1)\,C_{ij}, R(\sum C_{k\ell})]$ (k = 0, i; ℓ = 0, j)
4. Masest	address decoder logic	Min. Fn. test	8N	[illegible]
5. Walking I/O	slow sense amplifier recovery; verifies cell addressing, some dc pattern sensitivity	Poor access time test; poor noise test, write recovery test, and multiple cell selection test	$2N^2$	$\sum_{all\ i,j} \{W(1)C_{ij}, R(all), W(0)C_{ij}\}$
6. Galloping I/O	verifies functionality, multiple cell selection, access times, all read/read transitions	Poor write recovery test (loses effectiveness if IC returns to cell 4095 after each operation)	$4N^2$	[illegible]
7. Ping Pong	address latches	Special case of galloping I/O; only gallops to cells with address one bit off from reference cell	$2N \log_2 N$	$\sum_{i,j} [RC_{ij}, W(1)C_{ij}, \sum (RC_{k\ell}, RC_{ij}), W(0)C_{ij}]$ (all k, ℓ where k, ℓ expressed in binary is one bit off from i, j)
8. Galloping write-recovery	all write/read transitions; Fn. of cells, addressing	Only fair test of access time for some RAM's	$12N^2$	[illegible]
9. Walking columns	sense amplifier X-decoder	Specialized test. Medium Fn. test	$2N^{3/2}$	$\sum_{i} \{ [\sum_{j} W(1)C_{ij}], R(all), [\sum_{j} W(0)C_{ij}] \}$
10. Multiple walking columns	sense amplifier X-decoder	Same as #9, but walks two columns simultaneously	[illegible]	[illegible]
11. Walking complementary columns	sense amplifier imbalance, X-decoder	Same as #9, but column is half ONE's, half ZERO's	$2N^{3/2}$	$\sum_{i} [\sum_{j=0,\frac{N^{1/2}}{2}-1} W(1)C_{ij}, \sum_{j=\frac{N^{1/2}}{2},N^{1/2}} W(0)C_{ij}, R(all), W(0)all]$
12. Galloping columns	"worst case" refresh and cell interaction coupling	Guarantees refresh to last 8, 6, or 2 msec depending on version	[illegible]	[illegible]
13. Galloping diagonal	XY decoder switching "worst case" access time	Shorter galloping, medium Fn. test	$3N^{3/2}$	$\sum_{i,j} [RC_{ij}, W(1)C_{ij}, \sum_{k=1,\frac{N^{1/2}}{2}-1} (RC_{i+k,j+k}, RC_{ij}), W(0)C_{ij}]$

*NOTES
1. All patterns start with all ZERO's.
2. W = write, R = read, C = cell
3. W(0) = write a ZERO, W(1) = write a ONE
4. RC_{ij} = read the contents of cell at location i, j
5. R(all) = read all cells
6. As in math, operations are performed within brackets or parentheses first. Commas separate prior events (left of comma) from subsequent events (right of comma).
7. $C_{k\ell}$ is a cell other than C_{ij}

The last rays of sunset

"You are very observant," replied the GO/NO-GO player. "I anticipate that, like the last rays of sunset, you would hold the beauty of a minute enclosed within a single second. I, too, seek this beauty. In pursuit of it I have developed patterns that vary according to $N^{3/2}$ rather than N^2. These patterns are shorter by a factor of $N^{1/2}$, which is about 60 for a 4k memory."

The GO/NO-GO player then quickly showed George several $N^{3/2}$ patterns. One was a **walking column** pattern, which was similar to a walking ONE pattern, except that it walked an entire column instead of a single cell. A variation of this pattern walked two columns simultaneously and was twice as fast. A second variation walked a complementary column, which is a column with one color stone in the top half and the opposite color stone on the bottom. All three tested quite well for Bugs' hideouts in the sense amplifiers and X-decoders, but they were also less thorough than the N^2 patterns in testing functionality.

One more pattern, called the **galloping column pattern**, used a process similar to the galloping ONE/ZERO pattern, except that the galloping process was used only between the reference cell and cells in its own row. A variant of this pattern, the **galloping diagonal pattern**, substituted the diagonal for the row in the galloping process. The galloping column, said the GO/NO-GO player, was designed as a worst case test of the refresh cycles of the memory, just in case Bugs decided to hide there. The galloping diagonal explored the switching of the XY decoders and attempted to create worst case access time transitions, but the GO/NO-GO player explained that he was not yet convinced of the latter.

MANUFACTURER	DEVICES TESTED	PERCENT FAILED
1103 MOS		
AMI	550k	4%
MIL	700k	11%
Intel	455k	15%
1103A MOS		
Intel	1.9M	3%
BIPOLAR RAM's		
Intel	120k	15%
Signetics	60k	8% (mostly high temperature failures)
4k MOS		
TI	120k	18%
Intel	10k	15% (pattern sensitivity at temperature)

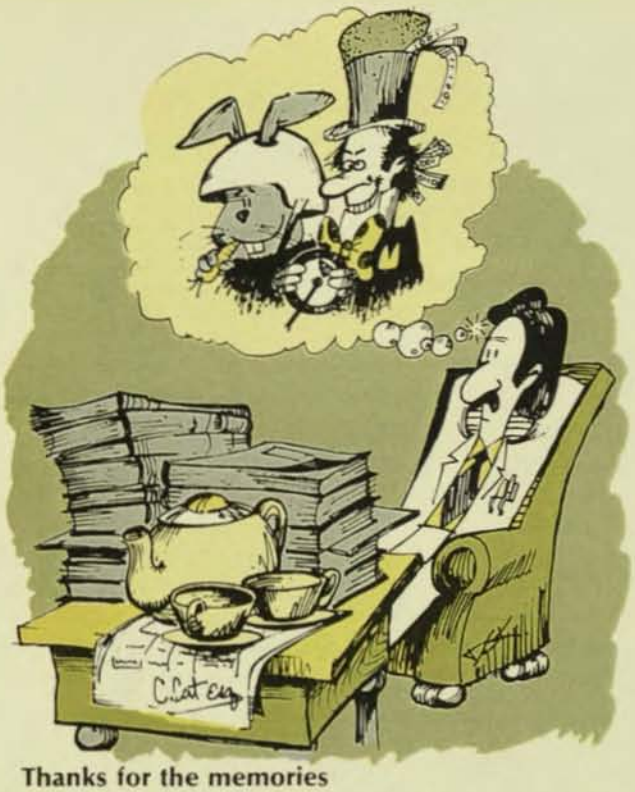
A major user of semiconductor memories tested his devices both dc parametrically and functionally at operating speeds. He screened his devices roughly to military reliability level C, or "good commercial" grade. In addition to the manufacturer's suggested tests he applied a few pseudorandom and special-application patterns of his own. His own patterns were related to computer usage and they did not outlast the suggested patterns in test length. The results he obtained should not be interpreted literally. Rather, they are a good indication of the magnitude of the overall problem of memory IC quality.

"If a single star burns out..."

As the late afternoon sun began to wane, the GO/NO-GO player wrote all the patterns he had shown George into a chart, along with his comments, and presented it to George for future use. George thanked him and added: "By the way, if I were to use all of these patterns in turn on a single memory chip, would I then be 100% sure of finding all the failure modes?"

The GO/NO-GO player smiled with the wisdom of the ages and replied, "If a single star burns out in the heavens we may not notice until it comes crashing down upon us. Just recently, my colleague George Nelson at the Naval Research Laboratory in Washington, DC, was testing high reliability CMOS/SOS memories. He tried most of the popular patterns and collected the devices that passed. He then tested them with a modified galloping ONE's pattern in which each cell in the memory was read twice in a row instead of once on each galloping iteration. Thirty percent of them failed the test."

At this point the GO/NO-GO player's eyes grew almost fond. "Bugs," he said, "can be a subtle and complex player. He can hide so well that only just the right combination of voltage levels, timing, temperature and stored pattern can bring him out. He can even hide in chains of formulae. Consider the changing of the number of ONE's in a given pattern. This corresponds to a change in the total charge on the memory chip, which causes a change in total capacitance, which in its turn causes a change in access times. Bugs can hide in any link in a chain of events. That is what makes him a worthy opponent.



Thanks for the memories

George and the GO/NO-GO player nodded in acknowledgement, and George rose to find his way back between the squad cars. He turned and asked, "Where might I find the Hall of Testers?"

"A test system is the vehicle for the exploration of the circuit," said the GO/NO-GO player. "Step into the squad car."

George saw the Mad Pattern Generator sitting at the wheel of one of the squad cars and waving for George to join. George entered the back seat of the black-and-white and the Mad Pattern Generator began driving through the hedgerows maze at a dizzying speed, lights flashing and siren howling. The hedgerows and brooks began to whirl by as in a dream, and the last thing that George remembered seeing was that the Mad Pattern Generator had been joined in the front seat by a little grey rabbit who sat munching a carrot.

When he awoke, George found himself at his desk before a large pile of test system brochures. At the bottom of the pile was another anotated chart signed by the Cheshire cat. Behind the brochures George found a set of porcelain teaware from the Chiang dynasty. George poured himself a cup of tea and read on. □

HALL OF TESTERS: MEMORY DIVISION

Manufacturer	Model No.	Price	Circle No.	NOTES
Adar Associates, Inc. 118 North Ave. Burlington MA 01803 Phone (617) 273-1850	DR 12 Series	$65K to $150K	150	At 8 MHz the DR series is not the fastest computer-controlled memory test system, but it is fast enough for the vast majority of memories. Its advantage is that it combines a modest price with big-system sophistication. DC parametric measurement is also performed. Double-speed testing, available as an option, puts limitations on the number of address lines (12 instead of 24). Input swings 0-20V, comparators swing ±5V.
Alma, Div. of Develco, Inc. 530 Logue Ave. Mt. View, CA 94043 Phone (415) 968-3903	760	$25K to $40K	151	This benchtop unit uses hard-wired control. Featuring 16 address lines and 4 input data lines, it performs dc parametric measurements as well as functional tests at 5-MHz rates. Comparator range is ±3V, and the drivers can swing from +20 to −5V. Test sequences are switch-selectable from a PROM board containing the most popular patterns. Different memories require different PROM boards. Driver voltage levels are set manually.
Datatron, Inc. 1562 Reynolds Ave. Santa Ana, CA 92705 Phone (714) 540-9330	45 50	$100K to $200K	152 153	The Hustler series units are general-purpose LSI test systems. Model 45 is a 10-MHz functional test system and the Model 50 adds dc parametric measurement capability to the capabilities of the Model 45. CMOS leakage currents are measured with 1-nA resolution on the Model 50. Like the other computer-controlled 10-MHz systems, the Hustler can measure propagation delays on a repetitive basis to within 2 nsec. The leading edge of the comparator strobe is incremented until a false output pattern is forced. This transition is considered the leading edge of the output pulse. Also, like the other $100,000-plus test systems, one driver/comparator is used per pin. Driver voltage swings are ±15V, as are comparator swings.
E-H Research Laboratories, Inc. 515 11th St. Oakland, CA 94604 Phone (415) 834-3030	4500	$250K to $400K	154	This general-purpose system's outstanding features are its expensive price tag and its super-high quality single-shot ac parametric measurements. Capabilities include dc parametric and 10-MHz functional tests. AC pulse channeling is performed through a subnanosecond-risetime fixture. Any IC with voltage swings to ±20V can be tested, with the appropriate speed tradeoffs (down to 5 MHz) occurring at the high voltage swings. Up to 96 pins are available, with a driver/comparator per pin. The word generator is 48 channels by 256 bits deep.
Fairchild Systems Technology 1725 Technology Dr. San Jose, CA 95110 Phone (408) 998-0123	Sentry series	$150K to $350K	155	The Sentry series boasts the largest sales dollar volume on the test system market. Controlled by Fairchild's own special-purpose computer, it performs dc parametric as well as 10-MHz real-time functional tests. At the top of the line, the new Sentry II is distinguished from the well-known Sentry 600 by its sequence processor and pattern processor. Like other sophisticated, general-purpose test systems, Sentry II can "telescope" its system delays to compact the testing process. Fairchild claims repetitive propagation delay measurements well within ±1 nsec. Sixty pins are available, with a separate driver/comparator for each.

Manufacturer	Model No.	Price	Circle No.	NOTES
Macrodata Corp. 6203 Variel Ave. Woodland Hills, CA 91364 Phone (213) 887-5550	MD 100 MD 104 MD 104M MD 154 MD 501	$8K $30K $100K $200K $300K	156 157 158 159 160	**Model MD 100** is a 5-MHz functional-only tester. Like other dedicated memory testers it generates patterns algorithmically for both the input patterns and the comparator reference patterns. It is hard-wire controlled by the pattern generator and intended for production GO/NO-GO testing. **Model MD 104**, a 10-MHz functional tester, offers a dc parametric add-on for $15,000. It features assembly language control of the pattern generator. Driver and comparator swings are ±15V, 64 pins. **Model 104M** also is a 10-MHz functional tester that can be interfaced to either an automatic handler or a wafer prober. Driver and comparator swings are ±15V and 64 pins can be accommodated. Like the MD 104 it is controlled by the pattern generator. Each pin may have either a driver or comparator, but not both. **Model MD 154**, a dc parametric and 10-MHz functional tester, uses a Nova 1200 computer for control. It features a driver/comparator per pin on 48 pins. **Model MD 501** extends the capabilities of the MD 154 to 64 pins. Its computer is multiplexed in such a way that four simultaneous foreground/background activities can be performed. With the MS option, up to 18 test stations can operate, 17 of them simultaneously. Like the other Macrodata systems, the MD 501 uses squarewaves (1V/nsec risetimes into 200 pF) for stimulus.
Micro Control Co. 1364 Buchanan Pl. Minneapolis, MN 55421 Phone (612) 788-3351	M-10	$35K	161	This unit is a benchtop tester dedicated to testing memories at 10-MHz rates. It is ac functional only and similar to Macrodata's MD-104. It features magnetic-tape storage and low-cost test jigs.
Pacific Western Systems, Inc. 855 Maude Ave. Mt. View, CA 94043 Phone (415) 961-8855	"Mustang"	$50K to $70K	162	Primarily oriented toward wafer probing, the Mustang can also handle packaged IC's. Besides dc parametric measurements, it tests ac functionally at 10-MHz rates. Drivers swing −1V to +21V, 32 pins, with 12 drivers and four multiplexed comparators.
Siemens/Computest Corp. 186 Wood Ave. S. Iselin, NJ 08830 Phone (201) 494-1000	901 203	$9.7K $150K	163 164	**Model 901** is an ac functional-only tester with pattern rates to 10-MHz. It's geared for the benchtop production line market. Part of the tradeoff for the low cost is that the TTL level drivers and comparators require a performance board to set the requisite voltage levels. 16 to 48 pins. **Model 203** is a computer-controlled dc parametric and functional test system. Its functional patterns are run at up to 20-MHz rates, and the unit can accommodate 24-pin devices. Driver voltage swing is ±30V; comparator swing, ±10V.
TRW/Colorado Electronics, Inc. 3450 N. Nevada Ave. Colorado Springs, CO 80907 Phone (303) 475-0660	System IV	$200K to $600K	165	System IV features pin counts to 264 and the ability to test PCB's, linear IC's and hybrids as well as digital IC's so it can be configured to just about anything you want. A choice of more dedicated modules costs less, naturally. For memory testing, TRW offers dc parametric measurement as well as ac functional tests at rates up to 50-MHz. Driver and comparator swings, depending on option, can go to ±40V.
Technitrol, Inc. 1952 E. Allegheny Ave. Philadelphia, PA 19134 Phone (215) 426-9105	4604	$40K to $50K	166	Exercising memories at either the IC, pc card or system level is the purpose of the Model 4604. It performs ac functional tests at 10-MHz rates, uses English language programming, and can also accommodate access times to 15 nsec. You build the performance boards to interface with this system's TTL driver/comparator levels.
Technology Marketing, Inc. 3170 Red Hill Ave. Santa Ana, CA 92705 Phone (714) 540-9330	5000	$17K to $28K	167	By using an 8-bit microprocessor to control what is basically a benchtop system, Model 5000 achieves a sophistication of control and datalogging resembling that of larger and much more expensive systems. It is a 10-MHz ac functional-only tester that is also used for logic testing. Up to 65k words of RAM memory are available to the controller. 24 pins.
Tektronix, Inc. Box 500 Beaverton, OR 97077 Phone (503) 644-0161	3455 3260	$100K to $150K $250K to $350K	168 169	Capable of testing 24-pin packages at 10-MHz speeds, **Model 3455** also boasts dual-limit comparators. Dual-limits on high/low comparisons allow greater sensitivity to noisy pulses on both the high and low ends of the output pulses. This feature is found elsewhere only on more costly systems such as the Fairchild Sentry, Siemens 203 or Tektronix 3260. Like the E-H system, **Model 3260** tests dc parametrics, real-time functional and single-shot ac parameters. Its functional tests are run at a 20-MHz rate and its fixture allows subnanosecond risetime system response on ac parametric measurements. It is a sophisticated computer-controlled test system with the ability to interface to Tektronix graphics terminals for powerful datalogging. 64 pins. Driver/comparator per pin.
Teradyne, Inc. 183 Essex St. Boston, MA 02111 Phone (617) 482-2700	J834	$90K	170	This system is dedicated to memory testing, but it has several features of the larger systems. It is computer-controlled and tests dc parameters as well as 20-MHz ac functional patterns. You can vary the strobe for propagation delay measurements, in addition to being able to vary the input voltage and timing. Voltage swing on the drivers is ±20V; on the comparators, ±2V.
Xincom Corp. (Div. of Fairchild Systems Technology) 8944 Mason Ave. Chatsworth, CA 91311 Phone (213) 341-5040	5500 series	$50K to 100K	171	Built around concept of placing programmable modules on a common data bus, the 5500 series uses ASCII as a program language. Capabilities include both dc testing and 12-MHz functional testing. Dual-limit comparators are featured. 24 pins. Random data option allows 16 bits by 2048 words.

Microprocessors in Testingland—the jury receives its instructions

Part III of our semiconductor testing series adjudicates the most embroiled issue of all—the microprocessor.

Martin Marshall, Associate editor

Logic and memory testing had become a familiar process to George after his first visits to Testingland (EDN, 1/20/76 and 2/20/76), but when his company decided to put "intelligence" in its products he was faced with testing the most complex chip in the industry, the microprocessor. The scene is George's cubicle in the engineering department. Enter George, holding a microprocessor and closing the door behind him.

George: "O that this too, too complex chip would partition into recognizable blocks—or that all its gates and wires would combine themselves into an introspective voltage upon a single pin. What a single pin that line would feed, that all the chip's logic and memory—and, yes, even the function of intelligence itself—would diagnose and reduce its decision to a simple ONE or ZERO on an output line. But no, a chip tests not itself but by incoming inspection. These dreams of self-testing IC's are for some better time, for some future generation who do not fight so intensely for chip area."

To test, or not to test

(George holds the μP up to fluorescent lights in contemplation.)

"To test, or not to test, that is the question. Whether it is cheaper in the end to pay the QC department outrageous fortunes, or to seek out functional patterns within a sea of complexity, and by so stimulating, test them. To stimulate, to compare—to compare, perchance to overlook. Ah, there's the bug! For, in those instruction sequences, who is to say which voltage and timing conditions, which interrupted pattern sequences, will bear the name "worst case"? Indeed, how can I say any pattern is worst case so long as untested possibilities outnumber tested ones like the stars outnumber the trees?

"In thought, this is a machine of ONE's and ZERO's, but in reality those HIGH and LOW voltages depend upon such subtle physical interactions as would turn the mind of Einstein awry, giving pause to his labors. A whisker of metal, the influence of a neighboring subcircuit, or a particular set of timing delays, these—and what far more subtle factors I know not—can turn a good circuit into a malfunctioning monster."

With that George once again begins to see the entrance to Testingland. Once again he finds himself before a crossroads next to a signpost reading LOGIC, MEMORIES, MICROPROCESSORS, PCB's, LINEARS and HYBRIDS, and once again a bell-curve shaped mushroom stands in the shade of the signpost. But this time the IC is not to be found sitting on top of the mushroom smoking a pile of money. Instead, the Dormouse

"A jury of its peers" was contributed by Fairchild Systems Technology to complement the cover theme.

slumbers in the shade of the mushroom.

George: (Loudly enough to wake the Dormouse) "Can you tell me what has become of the IC?"

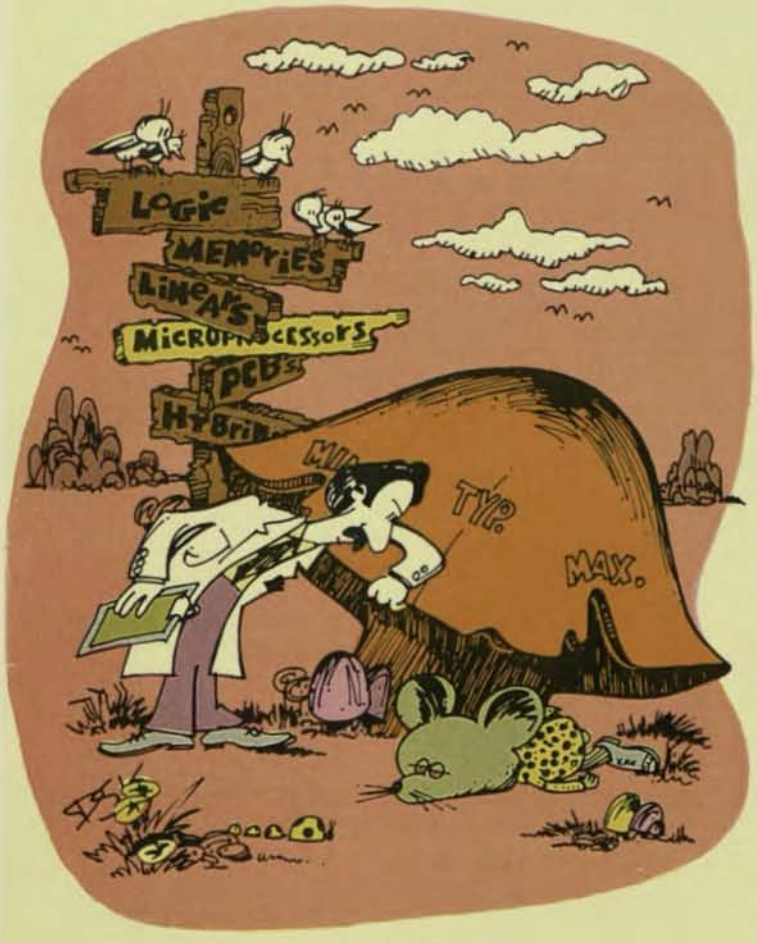
Dormouse: (Waking) "Oh yes, yes, the very question I would have asked. We should have a management seminar about that sometime." (The Dormouse goes back to sleep.)

George: (Pinching the Dormouse awake) "No, I mean the IC that sits on this mushroom."

Dormouse: "There is no IC sitting on this mushroom, unless I'm mistaken. There used to be one, but it's off at the trial."

George: "What trial?"

Dormouse: "Why, its own trial, of course. It has become a member of the μP's and therefore must undergo incoming inspection. The Cheshire cat is the judge, the Mad Pattern Generator is the prosecutor and I am the defense attorney. Oh dear, I'm very late!" (Dormouse falls asleep again.)



The Dormouse's defense

George puts the Dormouse in his pocket behind his calculator and walks down the path marked MICROPROCESSORS into a densely forested area. Suddenly he comes upon a large clearing in which a trial is obviously underway. Twelve assorted IC's buzz about in the jury box. The Cheshire cat, wearing a black robe, sits at the bench. The Mad Pattern Generator and the GO/NO-GO player sit at the prosecution table sipping tea, while the μP sits at the defense table reading EDN. George deposits the Dormouse at the defense table and sits in a neighboring chair just as the Cheshire cat finishes calling the court to order. The court falls to a hush and the Mad Pattern Generator rises.

Mad: "Your Honor, SSI, MSI and LSI of the jury. I intend to prove that yon microprocessor is guilty of deviation from its manufacturer's published specifications, and furthermore that said deviations are not only academic in nature, but can, if this device is left in the society of good IC's, cause catastrophic failures that will bring down a whole system."

Cheshire cat: "Does the defense have an opening statement?"

Dormouse: "The defense—rests." (Dormouse falls asleep again. The μP pinches its ear.) "Uh, which is to say, we intend to show that all this fuss about quality control is really much ado about nothing." (Turns to jury) "Could my client possibly be guilty? As fellow IC's you need only look at it to appraise it. It is such a piece of work of man! How limitless in faculty, with up to 65k of memory! A hundred different instructions, each of which it will follow the best it can! In form and design how admirable! In calculation, how like a god! The paragon of LSI! The state space of a minicomputer! The universal logic element and the true Prince of the industry!"

(Applause from courtroom audience. The Dormouse falls asleep on its feet. Cheshire cat bangs the gavel, waking the Dormouse.)

Dormouse: "Oh yes, the defense rests." (He sleeps. Gavel bangs.)

The μP speaks

μP: (Rising) "As long as it is *my* incoming inspection I would like to put *my* four, eight or 16 bits into this conversation."

Mad: (Rising angrily) "Sit down, I'm prosecuting you and we're controlling this test!"

Cheshire cat: (Bangs gavel toward Mad Pattern Generator) "One more pattern burst like that and I'll have your floppy disc removed from the Court." (To the μP) "Continue."

μP: "I call Tweedle DUT and KGD (Device Under Test and Known Good Device) to the stand."

Mad: (To Cheshire cat) "As prosecution I claim the right to call the first witnesses. I call them as my witnesses."

μP: "Suit yourself, I'll cross-examine."

(Tweedle DUT and KGD appear on the stand. After the appropriate protocol the Mad Pattern Generator approaches the stand.)

Mad: "You both sampled and compared the outputs of the DUT with those of the KGD did you not?"

DUT and KGD: (Look at each other and wink) "We did."

Mad: "Are they in the courtroom?"

DUT and KGD: "Yes."

Mad: "Could you point them out for the court?"

DUT: (Points to the μP) "That's the DUT."

KGD: (Points to a μP in the courtroom audience) "And that's the KGD." (The reference μP is escorted to the prosecutor's table. As it approaches, George notices that it has "Military Reliability Level 'A'—tentative" stamped under its JAN label. Flash bulbs pop and the Cheshire cat bangs its gavel.)

Mad: "And what was your finding?"

DUT and KGD: "It passed."

Mad: (Taken aback, but recovering) "Perhaps you could tell the court the method you used to test the IC's?"

DUT and KGD: "Certainly. We simultaneously sampled the outputs of both the KGD and DUT at intervals strobed by the system clock. We compared the sampled outputs of corresponding pins and found no differences."

Mad: "And what did you use to stimulate these devices?"

The Tweedle tests

DUT: "We used patterns that you generated by throwing identical sets of electrified cherry tarts at the IC's. At first you loaded the patterns 2k at a time into your local memory, the tart tray, but then after every burst of 2k patterns we had to wait 40 msec while you reloaded your tart tray from the test system memory. This made for a 5% duty cycle, which took us over 20 sec to sample the outputs of a multi-million byte pattern."

KGD: "Then we went to algorithmically generated patterns that allowed us a 100% duty cycle, but required that your patterns be generated according to some relatively simple formula. Finding a relatively simple formula that would also test everything we wanted was not a relatively simple task."

Mad: "Aha! And I suppose that you have records to document all this activity?"

DUT and KGD: "Heavens, no! Comparison testing is not intended for engineering characterization or any kind of sophisticated datalogging operation. We provide a low-cost solution for

production testing based upon the validity of the input patterns and the reliability of the reference μP."

Mad: "Your Honor, I request that the evidence of the Tweedle twins be stricken from the record because it was never, in fact, entered into the record."

Cheshire cat: "It is very difficult to take something from nothing—unless, of course, you are an official of the government or a large corporation. The jury is instructed, however, that the evidence presented was indicative, not conclusive."

Mad: (To the μP) "Your witnesses."

μP: (To Mad Pattern Generator) "You are doing an excellent job of presenting my case for me. No questions."

The reference μP's version

Cheshire cat: "It seems to me that the credibility of the Tweedle testimony depends upon the credibility of the reference μP."

Mad: "My point exactly, your Honor. I call the reference μP to the stand." (Reference μP takes the stand.) "You are the reference μP?" (Reference μP whispers into Cheshire cat's ear.)

Cheshire cat: "It requests that you address it either in the legal operation codes (op codes) detailed in its instruction manual or in its own symbolic mnemonic language."

Mad: "I can't go looking up op codes for everything I need to say. It would take all day!"

μP: (Holding up a mortar board hat) "Here, wear this assembler. It contains an embedded look-up table that allows you to speak or program the test system directly in the language of the μP."

Mad: (To μP) "For this relief, much thanks—but I'm still watching you." (He dons mortar board and turns to reference μP.) "Would you tell the court your occupation?

Ref. μP: "During the day I control a point-of-sale terminal at MacDonald's and at night I work part-time holding off the firing mechanism of an ICBM."

Mad: "I see."

Ref. μP: "Yes, I am."

Mad: "Well, perhaps you can tell us what happened the afternoon of the comparison test?"

Ref. μP: "The defendant was placed in a test socket that was interfaced to an environmental test chamber. I was placed in a test socket at ambient temperature and was given nominal voltage and timing conditions with which to perform. The defendant was subjected to temperature variations of 0 to +55°C and was fed incomplete pulses of variable height. We were given the same tasks to perform and we did so."

A military IC

Mad: "And how sure were you that the tasks that you performed were done correctly?"

Ref. μP: (To the music of Gilbert & Sullivan's "Monarch of the Sea") "I am a military IC, a reliability 'A' IC. I've been tested through and through, been through tough conditions too. I've been visually inspected. I've been rattled and injected. And though my supervisor, JAN, has done the best he can to make me exercise my functions while he microscopes my junctions, still my answers came out right."

Cheshire cat: "Still his answers came out right!"

Ref. μP: "Yes, that's right. They came out right." (Music subsides.)

Mad: (Leaning over stand) "I notice that 'tentative' is written under your reliability label. Could you explain that to the court?"

Ref. μP: "Yes, definite MIL STD 883-38510 certification procedures have not yet been established for μP's. Hence, the 'tentative' label."

Mad: "So even the military is not sure of your performance!"

Ref. μP: "No sir, but they are working on it."

Mad: (To μP) "Your witness."

μP: (Rises, goes to witness stand.) "No questions, but I would like to acknowledge that the reference μP and myself were born on the same assembly line, though not in the same lot." (The μP and reference μP go through an elaborate handshaking procedure and both return to the defense table.)

Enter the GO/NO-GO player

Mad: "I call the GO/NO-GO player to the stand." (GO/NO-GO player takes stand.) "Have you ever tested the defendant?"

GO/NO-GO: "Yes, I have."

Mad: "Would you describe those tests?"

GO/NO-GO: "Yes, at the time my concern was with the stability of the reference device. Using an approach outlined by my colleague, Bob Huston of Fairchild, I stored the response patterns of the reference μP in the memory of the test system. These stored responses, rather than the reference μP, were used in subsequent comparisons with the defendant. This freed the tests from any subsequent failures of the reference μP."

Mad: "Is this data logged?"

GO/NO-GO: A printout has been supplied to the court, and to the defense and prosecution."

Mad: (Thumbing through printout) "I see that there are only some 5k bytes in this test pattern (turns page) and less than 2k in this one. I have seen 4k RAM test patterns in excess of 16 million in length. Since the μP is more complex than a 4k RAM, why is its test pattern length so short?"

GO/NO-GO: "In these tests it was my objective to find a minimal-length test pattern that would also exercise the basic functionality of the μP. The second test you see there is that recommended by the μP manufacturer."

Mad: "So, if I understand you correctly, your object was not to find out if the μP *always* works, but to find out if it works *at all.*"

GO/NO-GO: "It could be stated that way. It is only fair to note, however, that once all the failure modes of a μP are known, then the test program can be shortened to test only for those failure modes. Such is the case with mature memories. Initially, N^2 patterns must be used, where N is the number of cells in the memory. But when the failure modes are all known, the patterns can be shortened to the order of N or $N^{3/2}$. When all the failures in the current generation of μP's are known, then a like shortening of test pattern length should be applicable."

What is "enough"?

Mad: "And have μP's—including the defendant—come to that stage yet?"

GO/NO-GO: "No, although the shorter patterns suggested by the vendors are based upon some failure analysis as well as some *a priori* reckoning. One must also consider that the nature of a μP is different from that of a memory. A typical 8-bit μP has 72 bits of internal memory, whereas a memory chip might have thousands. A μP also has large blocks of logic, such as the ALU, which are not as simply structured as a memory array."

Mad: "Is it not also true that these short test patterns were concocted to overcome the limited pattern length that nonalgorithmic pattern generators could provide without going to a pattern-burst process, and thus entailing a 5% duty cycle?"

GO/NO-GO: "True. Patterns this short are manageable even by some very inexpensive test systems. It is also true that these tests examine the μP's basic ability to perform conditional jumps, add numbers, carry bits, increment and decrement various registers, detect positive and negative values, rotate data left and right, transfer blocks of data between registers and execute programmed interrupts. In short, the ability of a μP to perform each of its individual functions with at least one set of data is verified. These test patterns are to the μP what a checkerboard pattern is to memory testing. They are compact and very useful, but by no means complete."

Mad: "What do you feel is lacking in these 5k length and less test patterns?"

GO/NO-GO: Coverage. These patterns will reveal a static fault such as a stuck-at-ONE and they will also reveal a section's inability to perform its basic function. Many field failures of LSI devices, however, are due to more subtle failures such as propagation delay variation with data load, sense

amplifier recovery after certain data patterns, and a collection of other failure modes that cannot as yet be identified in an *a priori* fashion. These failures, called 'instruction sensitivities' for lack of a better name, are at present only revealed by a massive but coherent infusion of input patterns to exercise the μP."

Mad: "Do you believe, then, that algorithmic pattern generation, which generates a continuous string of patterns in real-time and can be relatively inexpensive, is the proper method for μP testing?"

GO/NO-GO: It is certainly very useful, and the economics of testing can require it. But like a strong tree in a monsoon storm, its flexibility is sometimes limited."

Learn, execute and diagnose

Mad: "How so?"

GO/NO-GO: "The evolutionary process of finding a new device's failure modes, isolating the causes, and—if Fortune smiles upon you—creating a compact functional pattern for production testing requires many tools. One such tool is the random-logic pattern generator."

Mad: "You mean a pseudorandom Grey-code pattern generator, which changes only one bit from one input word to the next?"

GO/NO-GO: "No, Grey-code generators also depend upon a fixed formula. I refer to those word generators whose local memories are loaded with pattern bits arbitrarily specified by the programmer. Such word generators are useful in so-called 'back-door characterization' schemes. In these schemes someone finds a new failure mode in the field, and needs to develop a short program to test for that mode. If he has an arbitrary word generator, he can change his test program fairly easily. If he has an algorithmic generator, he may have to find a whole new formula. If he has both algorithmic and arbitrary pattern generation, then his flexibility increases. Such combined capability systems, however, cost upward of a quarter million dollars."

Mad: "Do you find any other flaws in the algorithmic-pattern generation technique?"

GO/NO-GO: "Only that, in some algorithmic test system configurations, one can only sample the μP address lines and not the data bus lines."

Mad: "Thank you." (To μP) "Your witness."

The μP's ordeal

μP: (Walks over to the witness box.) "It's good to see you again, GO/NO-GO player. As I recall, the last time we met was at my engineering characterization." (GO/NO-GO player smiles and nods.) "And, as I recall we performed some tests together."

GO/NO-GO: "Yes, that is true."

μP: "Would you mind telling the Court the specific approaches you chose to take in programming these functional tests?"

GO/NO-GO: "I would be pleased. I began with an algorithmic pattern approach. It stimulated your reset input, a task which took very few words to accomplish. I then incremented your program counter (PC) through its full range. Your PC is 16 bits long, and can assume 65k different values. Each instruction required four test systems cycles, so that the entire PC test required about 260k clock cycles."

μP: "So you tested my PC completely?"

Mad: (Rising) "Objection, your Honor! The only instruction that was executed by the defendant in that test sequence was a 'no operation' (No-op) instruction. The operation of the PC was not tested under a program load, as would be encountered in an actual application."

Cheshire cat: "Objection noted. The witness will answer the question."

GO/NO-GO: "As an independent module, the PC was tested for functionality. It is true that varying loads of operations would vary the total charge on the chip, thus changing the total capacitance and, thereby, affecting the various propagation delays within the chip. To explore the functioning of an entire program in each of the PC's 65k states would mean running 65k programs. That would multiply the test times for the PC to a number beyond the scope of my abacus."

μP: "Did you test any other functional blocks?"

GO/NO-GO: "Yes, I used 50k clock cycles to test your index register and associated memory. I loaded your H and L memories with alternating ONE's and ZERO's, and then transferred the patterns among the various registers."

μP: "—Until the entire memory section was tested. Correct?"

Mad: "Objection! Loading the memory registers with a long series of transfer instructions is an unlikely end use for the μP."

Cheshire cat: "Objection noted. The witness will answer."

The algorithmic procedure

GO/NO-GO: "Yes, within the limits of test time."

μP: "I further recall that you went on to test my stack pointer by incrementing and decrementing it through its full range, and that you used up some 260k clock cycles doing so. You then brought out the H and L memories by transferring them to the stack pointer."

GO/NO-GO: "This is true."

μP: "Then you spent 50k clock cycles on testing my ALU. You exercised its various functions many times, using 2^{16} different bit patterns. You then spent on the order of 1k patterns testing my accumulator. Using all 2^8 of its possible states you loaded, readback, rotated and transferred the contents of my accumulator. Did I pass these tests?"

GO/NO-GO: "Your responses were like sweet orange blossoms caressing the setting sun."

μP: "In the 2k clock cycles that followed, you tested my timing and control logic. Since there were some 20 untested instructions left, you used another 1k clock cycles to exercise each of these."

Mad: "Objection!" (Dormouse startles, then settles back to sleep.) "If so many patterns were required for each of the other instructions, how can we believe that a mere 1k patterns will adequately test the remaining instructions?"

Cheshire cat: "Noted. The witness will state the test results."

GO/NO-GO: "The defendant passed."

μP: "And did I not also pass several shorter tests—including one recommended by my manufacturer—that were applied by arbitrary-pattern word generators?"

GO/NO-GO: "Yes."

μP: "So, in essence, I have already passed the most rigorous electrical tests in the IC testing industry?"

GO/NO-GO: "Yes, you have."

μP: (To the jury) "The conclusion is obvious. Since I have not been found guilty of any malfunction I must, therefore, be found innocent and pass inspection."

A surprise witness

Mad: "Not so fast. I have one more witness to call before anyone starts drawing conclusions."

Cheshire cat: "I see no new characters on the agenda."

Mad: "This is a surprise witness, your Honor." (Wheeling and pointing) "I call the defendant to the stand!"

μP: "Gladly." (Takes stand) "What can I do for you?"

Mad: (Goes to prosecution table and picks up a tray full of cherry tarts. He brings it to the witness stand.) "This array of electrified cherry tarts represents a binary number that is 2k bits long. If cherry sauce is present in the tart shell then it is a ONE; if not, it is a ZERO. Factor this number."

μP: "Gladly." (The μP sets about rapidly tasting and rearranging the tarts. It continues while the Mad Pattern Generator turns to the jury.)

Mad: "The question of competence of a computer, be it on a chip or in an IBM 380, depends not only upon its ability to handle events that occur in the synchronized world of the CPU, but also in the highly asynchronous world outside—μP!" (The μP quickly gathers up the tarts it is working on and stuffs them, in order, into its stack.)

μP: "Yes?"

Mad: "Do you mind being interrupted in your work?"

μP: "Not at all."

Mad: "Very well, then. Here, wear this mask while you are working, so that no one can interrupt you. Continue." (The μP removes the stored tarts from its stack and resumes its search pattern. The Mad Pattern Generator turns back to the jury.) "You have just witnessed an interrupt. The μP is now masked and should not respond to an interrupt request—μP!" (The μP continues sorting.) "Good, now we will see how the μP handles distraction."

The moment of truth

Mad Pattern Generator goes to the stand and removes μP mask. He replaces it and takes it away again, then turns to the jury.

"As I was saying, the highly asynchronous nature of an interrupt makes it difficult to determine exactly when one will come upon a worst case timing condition." He suddenly wheels toward the witness stand and shouts, "Microprocessor!" The startled μP flings the entire tart tray into the air, spewing tarts in every direction over the courtroom. Realizing what it has done the μP sits in disgrace at the witness stand, performing No-ops.

Mad: (Triumphantly) "This, members of the jury, is the paragon of LSI, the universal logic element and the Prince of the industry!" (To the Cheshire cat) "I submit, your Honor, that a *prima facie* case has been demonstrated against the defendant. I ask that it be thrown on the junkpile and salvaged for its precious metals." (He returns to the prosecution table and sits with feet up.) "The prosecution rests." (The μP returns to the defense table.)

Cheshire cat: "Does the defense have any closing statements?"

μP: "Yes, I would like to change my plea to guilty, with explanation."

Cheshire cat: "Continue."

The μP pleads

μP: (Addressing court) "Imperfection itself need not be cause for total oblivion among intelligent creations. Consider the design engineer. He performs his duties in an intelligent fashion, and yet how seldom it is that his first design works flawlessly. Indeed, how many engineers have examined a design long after their product is on the market and concluded that the product needed revision? Are these engineers thrown onto the scrap heap? Not often, because the systems in which they work tolerate a certain number of errors, as long as the engineers perform the bulk of their work correctly.

"Is there not, then, among all the systems in electronics, a socket where my one tragic flaw can be tolerated? I have useful functions that are proven by experience—and with the discovery of my flaw my selling price has dropped to a pitiable fraction of my former cost. Therefore, put money in your purse! If I were a simple adder with a malfunctioning gate then the dictates of economics would be painfully clear, but as it is there are thousands of services that I can perform without a hint of imperfection. Therefore, put money in your purse!

"Let not the wheel of industry grind down its own profit margin into a meaningless pile of ceramic dust and so many base and precious metals. Rather, put money in your purse!

"Employ me in such capacity as befits my abilities and within such limits as to make my flaws irrelevant. The very universality of my design, which has caused me to be extensively tried, should also be that which saves me. If you are advocates of intelligence—and, of necessity, you are—then I know that you will be loathe to destroy the work of a whole generation of IC design that I embody. Therefore, once again I ask of you, put money in your purse!" (μP goes back to the defense table, pauses and says:)

"Use me in whatever way you will
So long as I draw current still"

(Courtroom applause, Cheshire cat bangs gavel.)

Tomorrow and tomorrow

George: (Rising) "If it please the Court, I have an application in which the μP need not be concerned with interrupts. If the appropriate discount can be arranged, I would be happy to purchase the μP."

Cheshire cat: (Writing up a bill of sale and handing it to the court Marshall) "It is so ordered." (Cheshire cat bangs its gavel, begins to rise, stops, and turns toward George.)

"Life is but a Jacob's ladder
Radiating new forms to the start
I close this case
Let us move apace
Before they close the bars"

(Exuent all, except George. Courtroom dissolves leaving George in the spotlight created by a lamp overhanging his desk. Before him, once again, is a pile of test system brochures and a chart annotated by the Cheshire cat. George picks up the μP left beside the brochures and examines it in his hand.)

George: "Tomorrow, and tomorrow, and tomorrow, your price will fall and Mishap's cost will rise. Now is the time for imagination and application to assume an equal size." (George opens a copy of EDN and reads on.) □

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HALL OF TESTERS: μP DIVISION

Manufacturer	Model No.	Price	Circle No.	NOTES
TEST SYSTEMS				
E-H Research Laboratories, Inc. 511 11th St. Oakland, CA 94604 Phone (415)834-3030	4500	$250K to $400K	418	Like other test systems with nonalgorithmic pattern generators, this one suffers from the low duty cycle involved in bursting patterns from the word generator in long test sequences. The word generator is 48 channels by 256 bits deep, reconfigurable to 24 by 512. The company states that it will shortly add an algorithmic generator to supplement the system. Advantages of the system include excellent single shot ac parametric measurements and realtime bidirectional I/O per pin.
Fairchild Systems Technology 1725 Technology Dr. San Jose, CA 95110 Phone (408)998-0123	Sentry 610 Sentry II	$250K to $400K	419 420	In terms of dollar volume, the Sentry 610 is the most popular test system on the market. Its word generator is 60 channels by 2k bits deep, which means that a minimal checkout of the μP can be performed without bursting the patterns. Longer test sequences require a 37-msec wait per pattern burst. The processors in the Sentry II compact the local memory required for pattern generation somewhat by using algorithmic generation to perform looped patterns within the local memory of the word generator.
Macrodata Corp. 6203 Varnel Ave. Woodland Hills, CA 91364 Phone (213)887-5550	104M 154 501	$100K $200K $300K	421 422 423	These systems use an algorithmic pattern generator to obtain both input- and output-compare patterns. These patterns are generated by two independently controlled sections within the pattern generator. Model 104M has its own assembly language (MTSA) and its own set of mnemonics. Model 501 uses a combination of FORTRAN IV and a test-oriented assembly language. All input pulses are square waves. Programming in MPU symbolic language on the MD104 is just becoming available for the Intel 8080. This feature will be offered for the Motorola 6800 in April, and for other μP's later at the rate of one MPU language per month.
Micro Control Co. 1601 37th Ave. NE Minneapolis, MN 55421 Phone (612)781-2612	M-10A MPU-1	$39K $ 8.5K	424 425	Model M-10A, unlike the above test systems, uses a reference μP as the KGD and simply stimulates the KGD and DUT in an identical fashion, comparing the outputs of both devices at strobed intervals. Input patterns are algorithmically generated. An Intel 8080 controls the system, which is oriented toward GO/NO-GO testing, rather than diagnostics. Model MPU-1, on the other hand, is a benchtop tester that uses a program stored in a 4k RAM to generate patterns algorithmically to test the μP. Unlike the M-10A, its timing is fixed rather than programmable.
Mirco Systems, Inc. 2106 W. Peoria Ave. Phoenix, AZ 85029 Phone (602)997-5931	500 Series	$25K	426	Basically a pc-board tester, this benchtop system has recently been modified to include testing of the Motorola 6800 μP and its associated PIA (peripheral interface adaptor). The system uses a short home-what larger than 1k) pattern supplied by Motorola that runs on bursts of 256 bits. Programming language is proprietary (MIRCODE).
Tektronix, Inc. Box 500 Beaverton, OR 97077 Phone (503)644-0161	S3260	$250K to $350K	427	Like the E-H and Fairchild systems, this system must use a pattern-bursting process whenever the test pattern length exceeds pattern generator bit depth. Its word generator is 64 channels wide by 1032 bits deep. Programming is done entirely in the instruction mnemonics of the μP under test. This is made possible by a flexible assembler. A Tektronix graphics terminal allows simple and highly interactive operator control. If a device engineer can program a μP, he can write a device characterization program for this tester. The system also is capable of single-shot ac parametric measurements.
TRW/Colorado Electronics, Inc. 3450 N. Nevada Ave. Colorado Springs, CO 80907 Phone (303)475-0660	System IV	$200K to $600K	428	This test system uses a you-dick-it/we-will-interface-it approach, offering pc-board test, analog and hybrid testing as well as that for digital IC's. BASIC programming language is featured.

LOGIC ANALYZERS

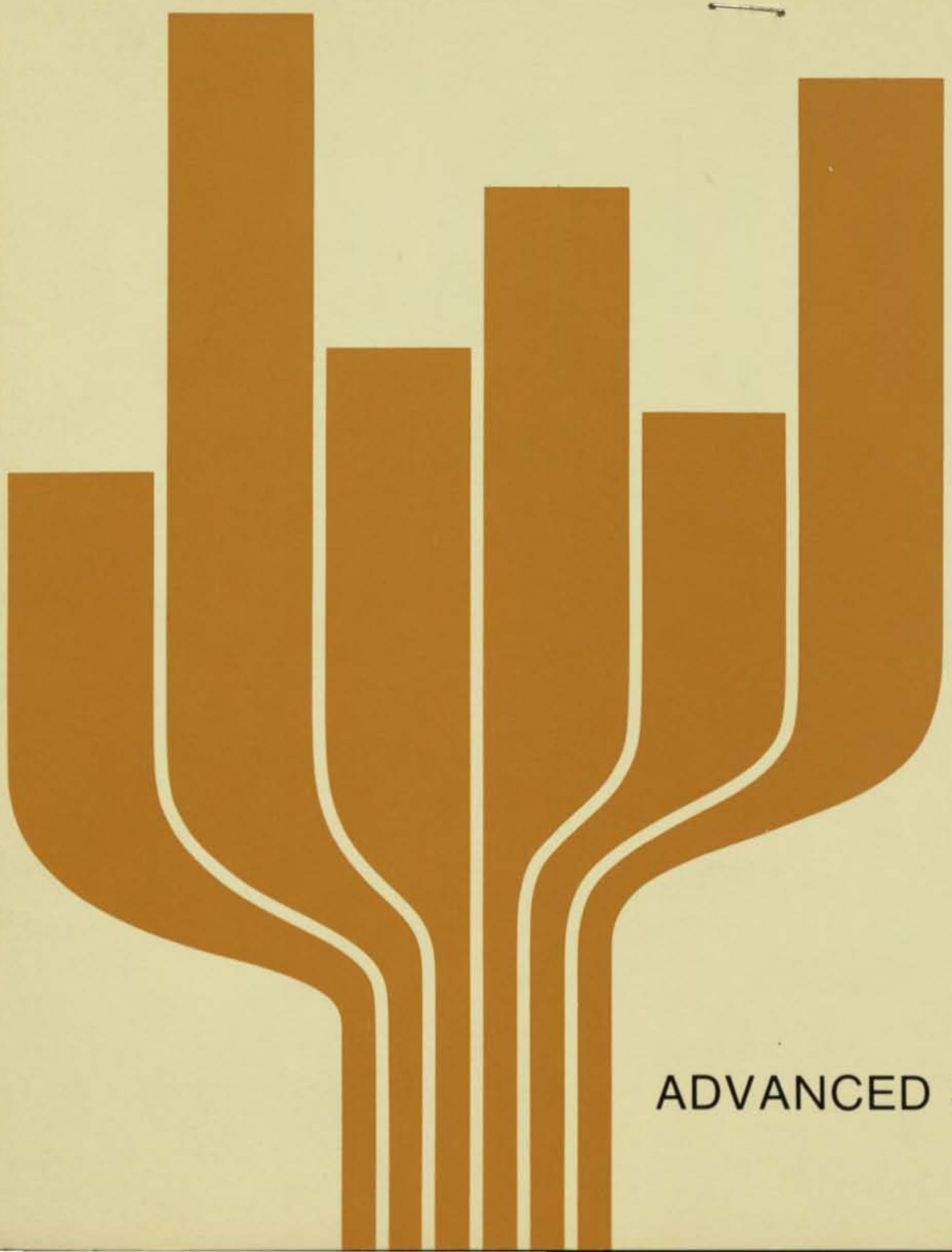
Biomation 10411 Bubb Rd. Cupertino, CA 95014	8100 851 8100D	$1955 $3575 $8850	429 430 431	Model 8100 is a 10-MHz, 8-channel logic state analyzer with pseudo timing-diagram display. Its word recognizer is external. Model 851, which was just released in February, is a 50-MHz, 8-channel logic timing analyzer with 256 bits of memory per channel and combinatorial triggering. It can also trigger when a repeated word ceases to occur. Models 8100D and 8200 are both ECL timing analyzers. The former operates at speeds to 100 MHz; the latter, to 200 MHz.
BP Instruments, Inc. 10601 S. Saratoga/Sunnyvale Rd. Cupertino, CA 95014 Phone (415)446-4322	20D	$2375	432	This 8-channel, 20-MHz analyzer features a 256 bits/channel. You can select different single-threshold voltages for channels 1-4 and 5-8.
E-H Research Laboratories, Inc. 515 11th St. Oakland, CA 94804 Phone (415)834-3030	1320	$9800	433	With up to 16 channels of 50-MHz logic, this analyzer is geared toward advanced labs. It has active probes (15 pF, 10 MΩ), dual-voltage thresholds per channel, leading/trailing edge triggering and glitch latching features.
Hewlett-Packard 1501 Page Mill Rd. Palo Alto, CA 94304 Phone (415)493-1501	1601L 5000A 1600A 1607A	$3375 $2275 $4000 $2750	434 435 436 437	Models 1601L and 5000A are 10-MHz, first-generation logic state analyzers. They are triggered externally, have external (optional) combinatorial triggering, and single-threshold comparators. Models 1600 and 1607A are 20-MHz, 16-channel, second-generation instruments. Like the 1601L, display format is in ONE/ZERO characters, arranged in either octal or hexidecimal. Bit depth per channel is not large (16 bits), but a separate memory can be exclusive-OR'd with the data streams. Microprocessor debug is enhanced by this capability and also by its address flow mapping mode.
Motorola Display Products 455 E. North Ave. Carol Stream, IL 60187 Phone (312)690-1400	MPA-1	$2985	438	Displaying 24 channels directly as six hexidecimal characters (four for address and two for data), this analyzer was designed specifically for debugging of μP systems. Its speed, 2.2 MHz, is not fast, but is adequate for software debug. Up to 65k cycles of delay can be selected and memory depth is 32 bits/channel. It features active probes (10 MΩ, 10 pF).
Moxon, Inc. 2222 Michelson Dr. Irvine, CA 92664 Phone (714)833-2000	777	$11,950	439	This instrument can generate 16 channels of TTL-level signals at up to 20-MHz, while at the same time receiving 16 channels of data. Display is selectable for either generated pattern or received pattern. Memory is 1024 bits total, divided by the number of channels displayed.
Tektronix, Inc. Box 500 Beaverton, OR 97077 Phone (503) 644-0661	LA501	$3250	440	This plug-in 16-channel analyzer was developed for the TM500 line mainframes, which supply power. Operating speed is configurable for 16 channels at 20 MHz, eight channels at 50 MHz or four channels at 100 MHz. Memory depth is 4096 bits/channel. The instrument requires external display and external combinatorial triggering.
Vector Associates, Inc. 685 Station Rd. Bellport, NY 11713 Phone (516)286-9000	V-16	$4200	441	This 20-MHz instrument has a combinatorial triggering capability and can accept up to 16 channels of data, which is displayed in pseudowaveform format. Memory depth is 256 bits/channel. A glitch-capture latching is also included.

MICROPROCESSOR DEVELOPMENT SYSTEMS

AMI 3800 Homestead Rd. Santa Clara, CA 95051 Phone (408)246-0330	AMI 6800 Kit MDC	$225 to $500 $12.8K	442 443	Minimum kit includes μP development board, operating program, 512 bytes of RAM and ACIA interface for TTY. The $500 kit includes 1k bytes of RAM, 2k ROM, 2k EAROM, three PIA ports and PROM programming capability. MDC, a full blown development tool with intelligent terminal and dual floppy-disc storage, also includes resident assembler and ability to program EAROM's. User can develop PC cards and run them on the 6800 μP that is internal to the terminal.
Digital Electronics Corp. 2126 Sixth St. Berkeley, CA 94710 Phone (415)548-2994	DICE/68	$795	444	This unit is an add-on to the Motorola Exorcisor®, which extends the debugging power of the Exorcisor's Exbug® software routines.
Intel Corp. 3065 Bowers Ave. Santa Clara, CA 95051 Phone (408)246-7501	Intellec® ICE MDS	$1200 $3950	445 446	Developed for the Intel 8080 μP and for Series 3000 bit slice elements, the MDS is a complete μC development system. The Intellec® ICE modules allow display of single- and multiple-step routines as well as status at breakpoint halts.
Micro Kit, Inc. 2180 Colorado Ave. Santa Monica, CA 90404 Phone (213)828-8539	8/16 mod 80	$4950 (with ICE)	447	Configured for use with the 8080, this system uses a CRT to display a symbolic snapshot (such as "JMP300" for a jump to address 300) of μP system operation. The snapshot can be taken without halting system operation.
MOS Technology 950 Rittenhouse Rd. Norristown, PA 19401 Phone (215)666-7950	KIM-1	$245	448	This μC card can check out other μC cards. At present no software has been developed to determine the best pattern for the various μP chips. A 6-digit LED display and TTY interface are offered. The μC card contains 1024 8-bit bytes of RAM.
Motorola SPD, Inc. 5005 E. McDowell Rd. Phoenix, AZ 85036 Phone (602)244-6737	Exorcisor® MEX-68CT	$2600 $2495	449 450	As the Intellec® is a complete development system for the Intel 8080, so is the Exorcisor® an emulation and development system for the Motorola 6800 and its associated chips. The MEX-68CT is a component tester for the 6800 family chips. An add-on to the Exorcisor, it runs a 750-byte test program in 256-byte bursts.
National Semiconductor Corp. 2900 Semiconductor Dr. Santa Clara, CA 95051 Phone (408)732-5000	IMP-16P PACE P	$3900 $3900	451 452	These development systems are complete with a conversational assembler that is programmed in the symbolic language of the μP. Source code and object code are simultaneously resident in its 8k to 32k memory.
Pro-Log Corp. 2411A Garden Rd. Monterey, CA 93940 Phone (408)372-4593	4004 starter set 4040 starter set 8008 starter set 8080 starter set 6800 starter set	$3700 to $4000	453 454 455 456 457	This is the broadest line of μC development tools. Sets specifying development of 4004-, 8008- or 6800-type systems are available, with a different system for each type of chip.
Rockwell International Corp. 3370 Miraloma Ave. Anaheim, CA 92803 Phone (714)632-3860	PPS-4MP PPS-8MP Basic PPS-4	$2895 $3450 $8000	458 459 460	As the Exorcisor® and Intellec® are to the 6800 and 8080 families, respectively, so are the Models PPS-4MP and PPS-8MP to the Rockwell family of μP chips. The systems contain an editor similar to that used on a PDP-10. Storage includes 4k for programs and 2k for data. The Basic PPS-4 is a device test system for the PPS-4 family. It runs vendor-supplied functional test patterns at a 200-kHz rate. The test patterns are less than 2k in length. Software is included.

Fairchild Systems, A Division of Fairchild Camera and Instrument Corporation,
1725 Technology Drive, San Jose, CA 95110.
(408) 998-0123 TWX: 910-338-0558

(408) 998-0123. TWX: 910-338-0558.



FAIRCHILD SYSTEM'S ADVANCED SOFTWARE CAPABILITY

FAIRCHILD SYSTEM'S ADVANCED SOFTWARE CAPABILITY

THE AGE OF TECHNOLOGY
A SOFTWARE REVOLUTION.....

This brochure discusses the advance software capability developed at Fairchild Systems; not only with respect to the current product offerings, but with regards to some of the history of software and how it has evolved into a modern device testing oriented software in the tester environment.

The discussion will include the basic concepts in prior art and then, reflecting on the requirements of advanced devices, the development of new programming techniques to meet the testing needs of the MSI, LSI arena. Although technical requirements dictate the basic thrust of software organization, significant implications with regard to user/management control will be covered and finally, some conclusions.

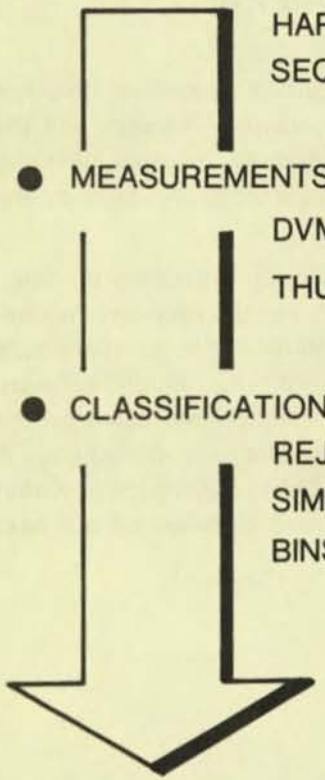
Basically, early testers were hardware controlled. Stimuli connections were hardwired and sequences if any, were controlled by panel switches or push-buttons which connected a power supply to the device-under-test.

Measurements were fundamentally digital volt meter oriented. Essentially, one single instrument was switched from function to function manually; the limits were thumb-wheel set and measurements were performed on a single measurement by measurement basis.

Classification in most cases was quite primitive, in some cases – plug board type programs simply identified a good part or bad part based on the output from the DVM. This developed into a simple classification of devices on a "good" or "bad" basis and binning was almost a semi manual procedure. The number of bins available were selected by either a plug board or by switches. These techniques were basic to the fundamental notion of automatic testing of devices and are still used in many cases for simple transistor testers.

EARLY TESTERS WERE BASED ON HARDWARE CONTROL FOR ALL FUNCTIONS

- STIMULI CONNECTIONS
  - HARDWIRED
  - SEQUENCE CONTROL BY SWITCHES
- MEASUREMENTS
  - DVM ORIENTED SINGLE INSTRUMENT
  - THUMBWHEEL LIMITS
- CLASSIFICATION
  - REJECT IDENTIFICATION
  - SIMPLE CLASS PLANS
  - BINS SEMI-MANUAL



BASIC TECHNIQUES DEVELOPED
(AND STILL USED)
FOR TRANSISTOR TESTING

It wasn't too long before the introduction of more complex devices (initially small scale integration IC's) increased the amount of control and data requirements necessary to manage the test functions.

This increase in complexity triggered the general thrust of our first large step forward in automatic tester development. First and obviously, the issue of more pins had to be addressed. Since there were more pins associated with the larger function capability within the device; more stimuli, and multiple drivers were required to address the device with multiple signals simultaneously.

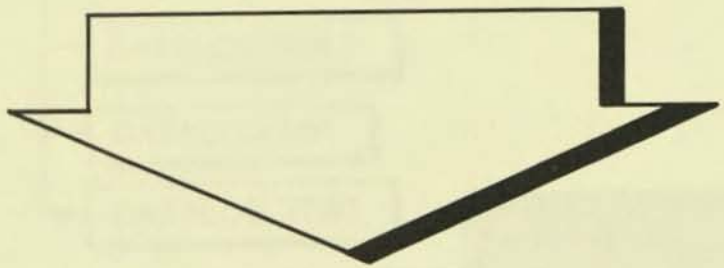
This, of course, implied more measurements, preferably measurements performed in parallel, although this was not possible on early testers. Class plans were now oriented towards, not only the device category with regards to fan-out and functional performance, but were also based on classing devices by grades, i.e., industrial, commercial, military, etc.

Binning strategies were quite advanced as compared to the original transistor oriented strategies and the user demanded a much broader interface, insisting upon the print-out of data obtained through the testing medium.

These basic requirements really led to the introduction of computer control, and the necessary requirement to manage the computer and tester with simple software. One example of that simple software approach to the testing function was based on the natural evolution of transistor test philosophy. A sample in representative block diagram of how that software might be organized is shown on our next chart.

THE INTRODUCTION OF MORE COMPLEX DEVICES SUCH AS I.C'S INCREASED CONTROL AND REQUIREMENTS

- MORE PINS
- FUNCTIONAL DRIVERS/STIMULI
- MORE MEASUREMENTS
- COMPLEX CLASS PLANS
- BINNING ADVANCED
- USER INTERFACE EXPANDED

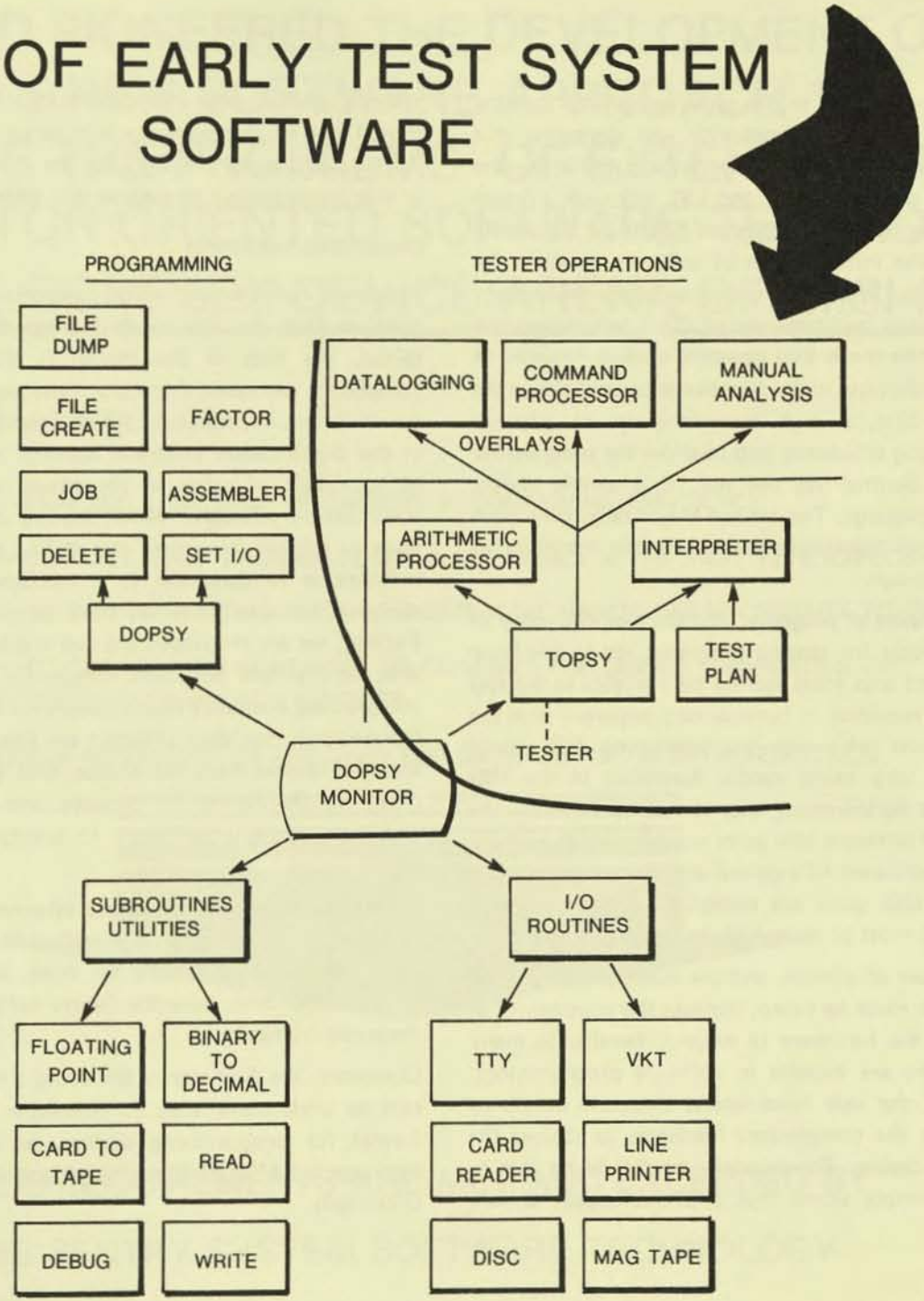


REQUIRED THE INTRODUCTION OF
COMPUTER CONTROL AND SIMPLE SOFTWARE

The next chart is a simplified block diagram of the basic software system used by Fairchild Systems to manage the popular Sentry product series. The segmented portion of the diagram, in the upper right corner, represents the essential functions from early transistor and simple I.C. systems preserved and integrated into a more complete organization. As can be seen by the chart, this functional requirement is an essential sub-set of the total software body required to treat the technology and part-type explosion created by device manufacturers.

Additional discussions will be centered on the response to these requirements, but in general, observe that control is now based in a total operating system rather than simply managing the multiplexing function. Strengths have been added in the user interface; utilities and extensive I/O; and in support to the programmer, files and storage management.

FOCUS OF EARLY TEST SYSTEM SOFTWARE



Fairchild, very early in the game recognized that the evolution of device complexity was increasing at a rate far beyond what had been anticipated in the late fifties. At that time, MSI and LSI, although a dream in the eyes of device designers had to be accommodated in the initial design of software to allow for that growth. Therefore, a new software technology was started in that time period. This technology was based on the thesis that complex devices required at least the following major functional capabilities in the software; first, a high level language to improve programming efficiency and to allow the programmer to retain control via the use of a simple syntax oriented language. The second major departure from conventional transistor systems was the introduction of mass storage.

Large numbers of programs, and the low efficiency of current media for storing programs, led to the basic requirement that mass storage be available to the test system as required. It became very apparent that the manufacturer who was manufacturing SSI would evolve to very many special functions in the MSI arena, and furthermore, that it was quite likely, the number of different MSI gates would explode as these more complicated IC's gained acceptance on the part of users. MSI gates are complicated; the degree of parallelism must be quite high to retain efficiency.

The number of stimuli, and the number of measurements that must be taken, increase the complexity of managing the hardware (a subject, familiar to many people who are experts in software programming). Therefore, the user must receive extensive assistance to manage the complicated hardware to achieve the results he desires. For example, he should be able to state in simple terms that a power supply should attain a specific value in a specific amount of time. It should not be necessary for him to go in and detail the bit positions of the DAC, for the analog converter in that power supply to achieve that value.

Classification strategies

Although early devices were categorized simply as good or bad, or how much leakage the part contained, the fact of the matter is that as device complexity increases, there are many parameters and combinations of parameters which must be considered in the classification program. Specific examples will be provided, of some of the newer techniques in classification strategies which require complex software to achieve. However, the ability to create this software is fundamental to a modern test system designed for evolution to more advanced devices. Further, we are convinced the user is seldom satisfied with very simple printouts; frequently, he has very complicated customer requirements for data. Military requirements for data printout are extensive, therefore, he should have the choice, and the ability to create in the format he chooses; and the kind of printout which is necessary to satisfy his requirements.

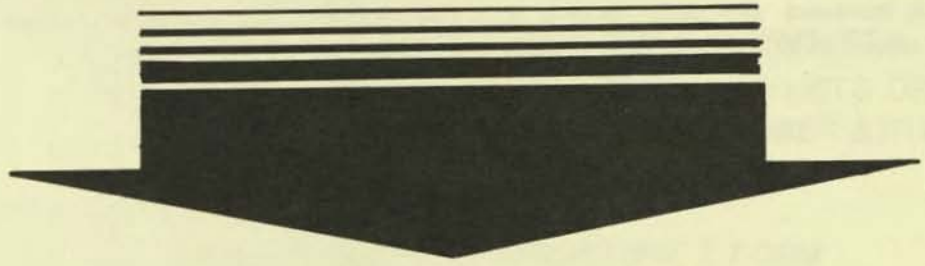
We feel that these are basic and inherent to software required to manage a modern MSI, LSI or integrated circuit device environment. We think, and we would like to show then, how the Sentry software exceeds these requirements.

Obviously, the first step is achieving a very common, easy to understand, easy to remember language and format for programming devices. At Fairchild the language is FACTOR (Fairchild Algorithmetic Tester ORiented).

FAIRCHILD PIONEERED THE DEVELOPMENT OF A COMPLETE NEW SOFTWARE APPROACH TO ELIMINATE THE PROBLEMS OF EXTENDING A TRANSISTOR ORIENTED SOFTWARE TECHNOLOGY INTO THE COMPLEX DEVICE ARENA OF MSI & LSI

COMPLEX DEVICES REQUIRE:

- HIGH LEVEL (ENGLISH) LANGUAGE TO IMPROVE PROGRAMMING EFFICIENCY
- MASS STORAGE FOR LARGE PROGRAMS, MEDIA EFFICIENCY & THE PART TYPE EXPLOSION
- ASSISTANCE TO THE USER TO CONTROL THE EXTENSIVE HARDWARE NECESSARY TO TEST
- THE ABILITY TO CREATE NEW SOFTWARE TO CLASSIFY THE UNIQUE PROPERTIES OF ADVANCED SEMICONDUCTOR CIRCUITS
- HIGHLY FLEXIBLE INTERFACE TO THE USER FOR DATA OUTPUT & DATA REDUCTION



THESE REQUIREMENTS ARE MET AND EXCEEDED BY

THE SENTRY SYSTEM SOFTWARE TECHNOLOGY

As always, knowledge is enhanced by learning the structure of a language. If we have an action verb, the recipient of the action, and can define the degree of action, we can achieve then a simple degree of sequence which is consistent.

For example;

Force voltage to 5 volts – range 1.
Defines an action, on what, and how much.

This simple language becomes then a vehicle not only for the production of software but for communication. Source parameters are in test terminology, not the terminology of the software expert, this reduces a need, in fact, eliminates the need, for the memorization of complicated rules, long lists or conversion tables to obtain an understanding of the program. The software programmer will make real sense to the product engineer who is responsible for getting the product produced, tested and delivered on time. Error detection is increased. Obviously there is a visual impact that retains its structural value in a form which becomes very easy to use once one is involved in the program.

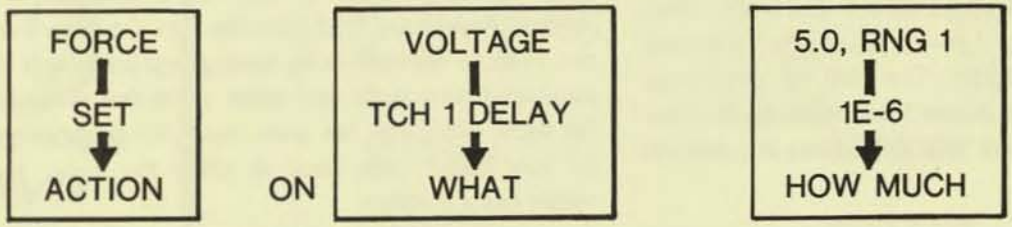
We have a language which is converted to machine statements, which does follow rules internal to the machine. Thus, when the statement is performed improperly or where elements within a statement are missing, errors can be flagged by the compiler to the user, before that error is propagated onto the production floor or into the data for that device.

One parameter which is frequently overlooked with a high level language is the power of a statement. Previously many low level assembly language programming techniques required laborious generation of internal sequences to accomplish what are essentially very simple functions. Here, at Fairchild, with one or two FACTOR language statements, as much as 1500 words of equivalent assembly language code is saved. This represents a phenomenal increase in efficiency and power of the programmer.

A LANGUAGE PERMITS THE RAPID AND EFFECTIVE GENERATION OF MASSIVE PROGRAMS WITH LITTLE TOTAL PROGRAMMING EFFORT

- LEARNING IS ENHANCED DUE TO STRUCTURE:
  - AN ACTION VERB
  - THE RECIPIENT OF THE ACTION
  - THE DEGREE OF ACTION (IF REQUIRED)

I.E. :



- VEHICLE FOR COMMUNICATION

  TEST TERMINOLOGY USED - VOLTAGE, CURRENT, ETC.

  NO MEMORIZATION OF LISTS OR TABLES
  NO DECODING OF NUMBER STRINGS

- ERROR DETECTION IS INCREASED
  - VISUAL - DUE TO INHERENT STRUCTURE & FORM
  - COMPILER - INFORMS USER WHEN STATEMENT IS IMPROPERLY WRITTEN OR WHEN ELEMENTS WITHIN A STATEMENT ARE INVALID OR MISSING

- PROGRAMMER HAS THE POWER TO GENERATE AS MUCH AS 1500 WORDS OF EQUIVALENT ASSEMBLY LANGUAGE CODE WITH ONE OR TWO FACTOR STATEMENTS

Although mass storage is a requirement for the manipulation of complicated test plans in programs, there are many other reasons for the use of a mass storage oriented data base.

Let's compare some of the basic media oriented towards data storage. The disk Fairchild uses, for example, is very fast and contains 18 million bits of storage space. Paper tape, of course, has infinite storage space but its density is relatively low in the order of ten characters per inch. Cartridges or cassettes achieve what are significant orders in improvement which is about 10,000 characters. However, – and this is the rub – it takes time to achieve access to a given program. The disk has an average seventeen milliseconds access time, whereas, in paper tape or cartridges, we're talking minutes and seconds respectively.

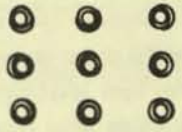
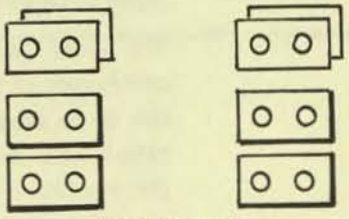
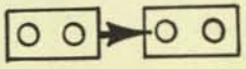
There is effectively no media storage for disk, it comes in one piece. However, to those of us who have been exposed to a programming environment in a production facility, there are literally cabinets and drawers full of various paper tapes, cartridges and cassettes which must be managed and controlled in order to achieve a reproducible test program on the machine.

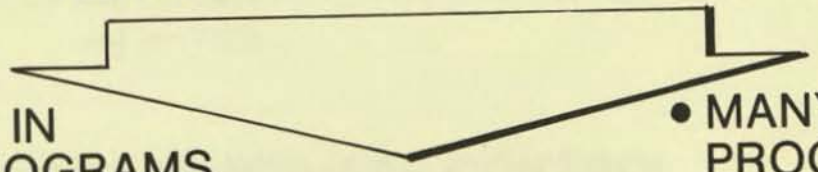
Editing on the disk is essentially on line, whereas, with paper tapes and cartridges, a new copy has to be created to replace the old copy. This sounds very simple; it's difficult to discard the old until the new has been tested and once tested, we now have two copies which can easily be interchanged.

Back-up for the disk is a system oriented function. Mag tape, and cards can back up a disk effectively in case of problems or in case of difficulties with storage. Paper tape, and cartridges on the other hand can only be backed up by having duplicates and the duplicates have little real value when the peripheral for those duplicates has gone down. It's questionable to have paper tape back-up when the paper tape reader has a problem.

For these major considerations, plus the fact that there is a very high error rate in loading especially with many programs, we recommend disk storage with mag tape backup. Also, programs get lost, are not replaced or are replaced with the wrong ones and they are relatively inflexible with regards to editing when using older media storage techniques.

MASS STORAGE PROVIDES THE DATA BASE NECESSARY TO DEVELOP A TEST PLAN, SET UP A STATION AND MANAGE THE COMPLETE TESTER ENVIRONMENT

	PAPER TAPE	CARTRIDGES OR CASSETTES
• CAPACITY DISK  18,000,000 B	 10 CH/IN	 10,000 CH
• LOAD TIMES 17 MS AVG.	MINUTES	SECONDS
• MEDIA STORAGE NONE	CABINETS	CABINETS
• EDIT ON-LINE	OLD NEW  DUPLICATES	OLD NEW  DUPLICATES
BACK-UP MAG TAPE CARDS		



- HIGH ERROR RATE IN LOADING MANY PROGRAMS
- HIGH ERROR RATE DUE TO LABEL/CONTROL
- MANY LOST PROGRAMS
- INFLEXIBILITY

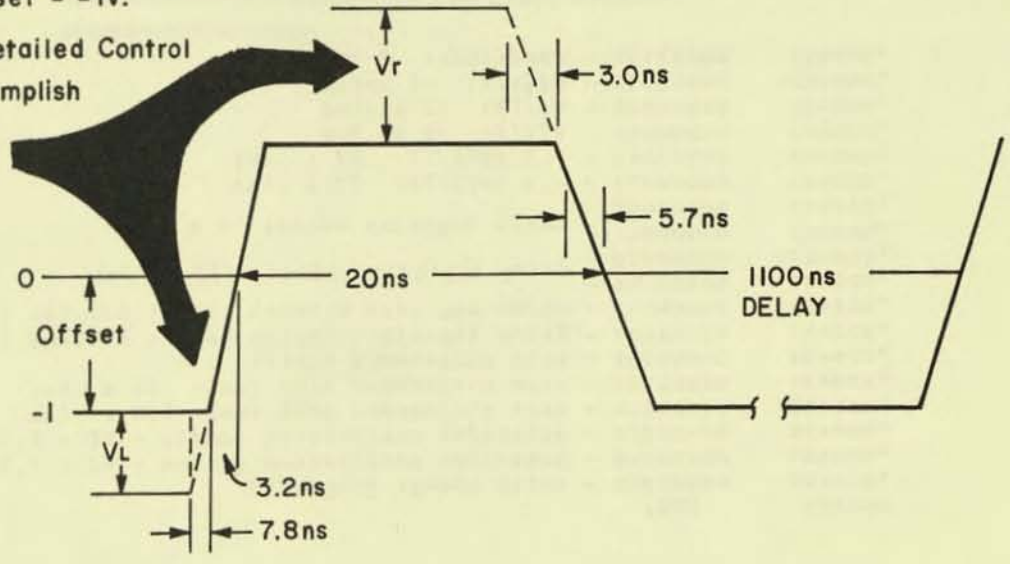
One of the major requirements listed earlier in this discussion was the use of the software to manage the hardware and produce the desired results. Programming of power supplies are rather trivial examples. Let's take a look at a pulse generator on Fairchild Systems Technology's Time Machine. The desired parameters are listed as pulse width of 20 ns, rise time of 8 ns, fall time of 13 ns and a delay of 1.1 μs or 1100 ns, amplitude of 2 volts and we'd like the pulse to be offset by 1 volt.

The pulse generator does not respond directly to commands of that nature. Generally pulse generators like to be programmed from some low level to some offset value and from some maximum level down to the amplitude of interest. The correction for rise time on pulse width must be computed so that the pulse width and the rise time is achieved on the device to match the requirements. The delay to the rising waveform of the next pulse must be compensated for. Also, fall time and the delay of the pulse by the pulse generator must be allowed for. This is not easy to keep track of, especially if its not done frequently, therefore, Fairchild provides extensive software to do these computations to achieve the result desired.

THE USE OF FACTOR ALLOWS THE USER TO PROGRAM COMPLEX WAVEFORMS WITH SIMPLE CONTROL STATEMENTS-- THE COMPILATION SOFTWARE MANAGES THE DETAILED CONTROL OF THE HARDWARE TO PRODUCE THE SPECIFIC RESULT

- PW = 20 nsec, tr = 8ns, tf = 13ns, Delay = 1100 ns
  Amplitude = 2v, Offset = -1v.

Software Provides Detailed Control of Hardware to Accomplish Desired Values



SOFTWARE MANAGES HARDWARE CONTROL REQUIREMENTS & AUTOMATICALLY COMPUTES OFFSETS

```
000057          SET TCH1 DELAY 1E-6, FDELAY 100E-9, FWIDTH 20E-9, TR 8E-9,
000060          TF 13E-9, AMPL 2, OFFSET -1, BURST 1;
*000372     17370001 - long register addr extend to address time option
*000373     04400001 - registers.
*000374     04467067 - write delay register:  1103.7ns
*000375     04500000 - write width register:  16.3ns
*000376     04540543 - write edge transition register - rise: .800 V/NS
*000377     04605440 - write edge transition register - fall: .492 V/NS
*000400     04606754 - write amplitude register:  2 volts
*000401     04667130 - write offset register:  -1 volt
*000402     04710310 - initiate a time delay of 3ms for previous register
*000403     17601030 - writes
*000404     24740001 - write burst counter:  1
*000405     17370000 - reset extend register to address sentry system
*000406     66500001 - registers.
*000407     00000000 - interpretive code to cause transfer of following
*000410     00000000 - 26 words to global for any subsequent interpretive
*000411     00000000 - timing generator changes.
*000412     00000310 - user programmed period:  0
*000413     00000000 - user programmed width:   200 x .1ns
*000414     00025370 - user programmed delay:   11000 x .1ns
*000415     00005440 - leading edge transition scope:   .800 V/NS
*000416     00004754 - trailing edge transition scope:  .492 V/NS


*000417     00027130 - amplitude:  2 volts
*000420     00010310 - offset:  -1 volts
*000421     00000022 - VL/TR:  18 x .1ns
*000422     00000036 - VT/TF:  30 x .1ns
*000423     00000040 - -.5 AMPL/TR:  32 x .1ns
*000424     00000071 - -.5 AMPL/TF:  57 x .1ns
*000425     00000000 -
*000426     00000001 - width register value:  1 x 10ns
*000427     00000000 -
*000430     00000156 - delay register value:  110 x 10ns
*000431     00000143 - width register vernier value: 63x.1ns (2-4-2-1 BCD)
*000432     00000067 - delay register vernier value: 37x.1ns (2-4-2-1 BCD)
*000433     00000001 - user programmed burst:  1
*000434     00000120 - user programmed rise time:  80 x .1ns
*000435     00000202 - user programmed fall time: 130 x .1ns
*000436     00000226 - generator calibration factor - VL : 1.5 volts
*000437     00000226 - generator calibration factor - Vt : 1.5 volts
*000440     40000000 - entry change flag word
000060        END;
```

A representative list is shown here of a software program showing what actually went on with regards to producing the details of managing a pulse generator. As can be seen, the compensation for a rise and fall time at various low rates are accomplished, amplitude registers are addressed, time delays are put in for previous register manipulations, and code generated to take care of the management of the storage of the various variables, etc. The point of the matter is, the programmer had in mind a specific arrangement of the pulse sequence and values, this translation is performed automatically in software. This frequently is not the case on many older test systems which still adapt and utilize a basic transistor programming strategy.

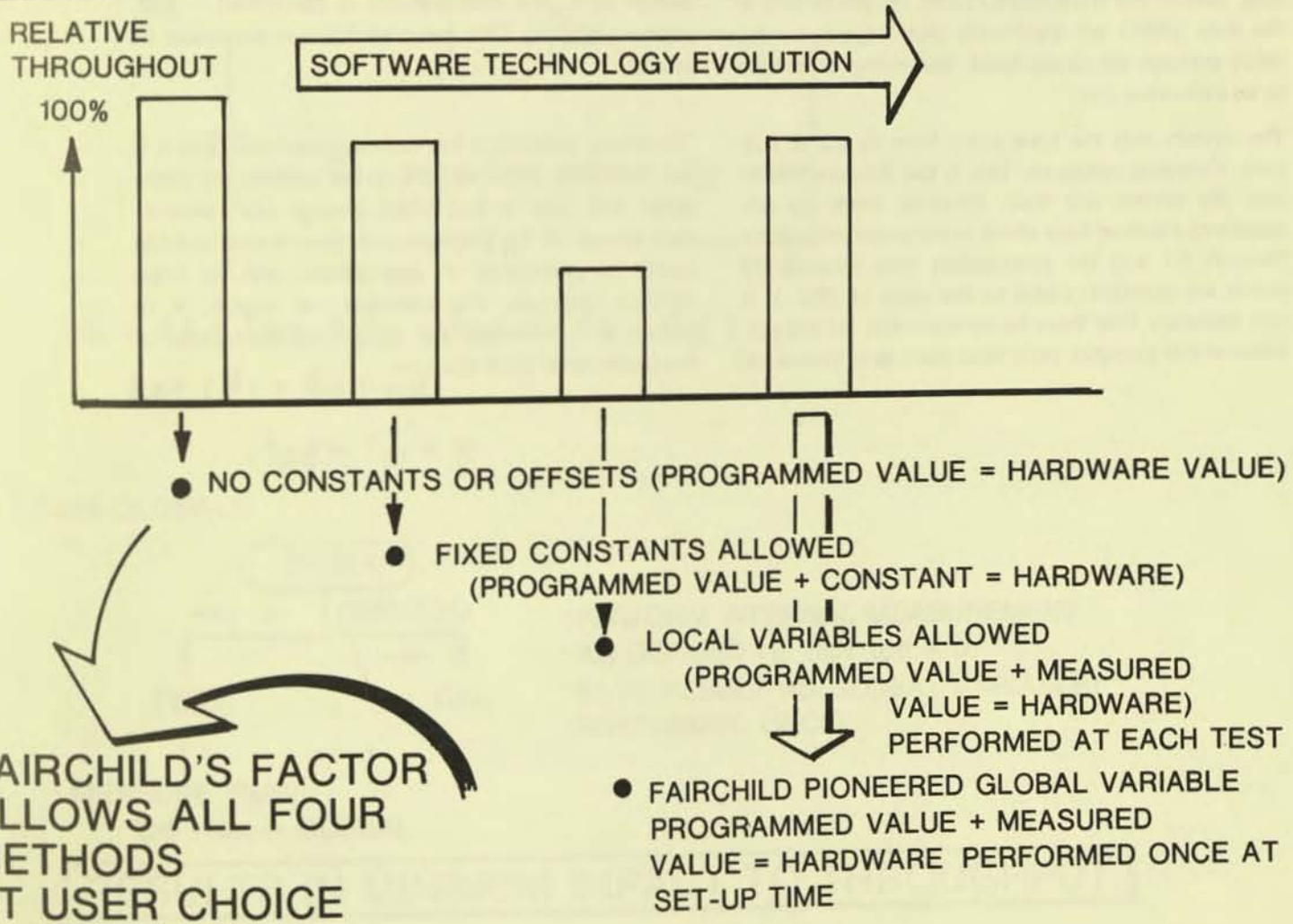
The next figure illustrates the multiple techniques for the calibration function provided by our advanced software technology. Now, in many transistor oriented test system software bodies, this calibration function is constrained to the user for utilization in just one dimension. A system will operate at its' maximum throughput with no constant, no constraints and no offsets to be managed or handled in the hardware. Whatever is programmed is supplied to the controlling registers and the system runs essentially wide open.

However, it is possible to add constants in many systems so that a program value is constantly offset or corrected by a constant which is then applied to the software. This manipulation does take time and there is a drop in throughput as a result of the manipulations.

Further flexibility can be gained by having the value itself offset the new value to the hardware so that a program level plus or minus a measured level is a resulting level, to be translated and to be delivered to the hardware.

Now obviously, there are at least two tests involved in this type of operation, so the impact of throughput is the greatest with this kind of calibration. Essentially since we are taking a value, treating it as a variable as a result of a prior measurement, it must be performed at each test. However, Fairchild provides a new technique called, "Global Variables" which essentially performs the same function, only once at setup time, or as frequently as desired so that the user regains control of the system's throughput throttle. Furthermore, we do not constrain the user in any way to the use of any particular technique. Fairchild's Factor allows the use of all four methods at user's choice to optimize the amount of time the user is willing to spend on the calibration function with regards to the management of throughput on the system.

AN ADVANCED SOFTWARE TECHNOLOGY MUST PROVIDE MULTIPLE TECHNIQUES FOR THE CALIBRATION FUNCTION--- TO OPTIMIZE THROUGHPUT AND TO MATCH REQUIREMENTS OF NEW PARTS



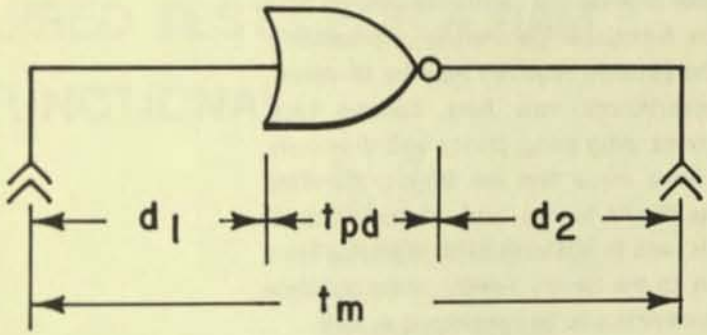
A typical application of this technique might be for example, the calibration of fixed delays; delays which are common to all devices placed in sockets due to the location of loads or the location of stimuli or measurement probes. Also the device itself if it's a large device, has transmission paths on the surface of the chip which are significant with regards to the delay through the device itself. Sometimes these have to be calibrated out.

The system sees the total delay from inputs to outputs, including constants. This is the measured delay that the system will treat, however, there are two constants involved here which is the propagation time through D1 and the propagation time through D2 which are constants added to the value of TPD. It is not necessary that these be constant but for the purposes of this example, we'll treat them as if they were.

Therefore, D1 and D2 represent K and the propagation delay TPD is equal then to TM-K. Using global variables in Fairchild's approach, you can start the system, set switch equal to 0, do the test, measure the time and set up that time as a variable. Then setting switch to 1, the measurement is performed – just once – (setting TPD equal to 0,) and the result is stored.

Therefore, calibration has been accomplished and it is not necessary to repeat the entire process for every single test. One in fact might arrange one's production or use of the machine such that the calibration could be performed at appropriate, and we hope sensible intervals. The objective, of course, is to reduce to a minimum the impact on throughput of extensive calibration routines.

A TYPICAL APPLICATION OF THIS APPROACH MIGHT BE FOR THE CALIBRATION OF FIXED DELAYS --- A tpd MEASUREMENT

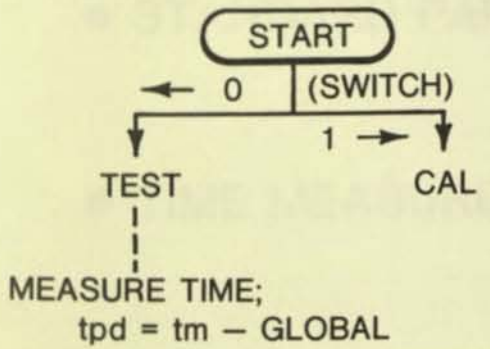


$$t_m = d_1 + t_{pd} + d_2 = t_{pd} + (d_1 + d_2)$$

$$\text{Let } (d_1 + d_2) = K$$

$$t_{pd} = t_m - K$$

- USING GLOBALS



(PERFORM INTERNAL MEASUREMENT
AS DEFINED i.e. SET tpd = 0.
SAVE RESULT AS GLOBAL VARIABLE)
PERFORMED ONCE!

RESULTS IN MINIMUM IMPACT TO THROUGHPUT

Software complexity can be a problem to user understanding. Many devices such as RAMS require many thousands of tests and it must be possible to program these devices easily. Fairchild's Sentry Software System does provide this capability. Shown here are some of the functional parametric requirements for a RAM. The patterns required may be all zeros', all ones', checkerboards, row bars, column bars, walking ones, zeros, ping pong, parity and diagonals, and I'm sure there are a few we forgot. Standard parametric tests should be run, and are run on most device programs, and in the case of at least the Time Machine option to the Sentry family, there are time measurement parameters to be considered as well.

EVEN THE MOST COMPLEX DEVICES, SUCH AS RAM'S, REQUIRING THOUSANDS OF TEST MAY BE EASILY PROGRAMMED WITH THE SENTRY'S SOFTWARE SYSTEM

REQUIRED TESTS FOR A RAM -

- FUNCTIONAL
  - ALL 0's
  - ALL 1's
  - CHECKERBOARD
  - ROW BARS
  - COLUMN BARS
  - WALKING 1's, 0's
  - PING PONG
  - PARITY
  - DIAGONALS
- STANDARD PARAMETRICS
- TIME MEASUREMENT PARAMETERS

The key to programming these many different variable patterns efficiently is in the software. Fairchild's Factor allows a very large user oriented software program such as "Rampat" to be invoked with very few command statements. This popular Rampat is Factor callable (it means that once you own the ability to program in Factor, you can call on Rampat with a simple command). It not only generates these functional patterns but it also assists the user in setting up the device by requiring a few very simple things to be done. First, you must know the RAM size, the addresses, inputs and outputs, which is common knowledge if you are going to test this part. You must provide a command to write any of the available patterns and a command to read the written patterns and set up the time measurements.

THE KEY TO THIS STEP FUNCTION IMPROVEMENT IN PROGRAMMING EFFICIENCY IS FST'S FACTOR APPROACH WHICH ALLOWS LARGE PROGRAMS SUCH AS RAMPAT TO BE INVOKED WITH FEW WORDS

- THE POPULAR 'RAMPAT' IS A FACTOR CALLABLE PROGRAM WHICH GENERATES FUNCTIONAL PATTERNS AS WELL AS ASSISTING THE USER TO SET UP THE DEVICE-----VIA

  -A DESCRIPTION OF THE RAM SIZE, ADDRESSES, INPUT, OUTPUTS

  -A COMMAND TO WRITE ANY OF THE AVAILABLE PATTERNS

  -A COMMAND TO READ THE WRITTEN PATTERN

  -AND SETS UP THE TIME MEASUREMENTS

Let's take a look at how that might be done on a common 95415/1024 bit RAM. You may read the commentary for the listing shown. Essentially as shown here, we have described that RAM with six statements. In the first statement, we have defined the size of the cell structure as one output. The second statement defines the X addresses followed by the Y addresses, we identify the data input pin, the data output pin and the write input pin. The RAM is now completely described.

DESCRIBING A RAM SUCH AS THE 95415 1024 BIT REQUIRES ONLY 6 STATEMENTS

1. EXEC RAMPAT (0, 32, 32, 1)
   - THE RAM IS 32 BY 32 IN CELL STRUCTURE AND HAS ONE OUTPUT

2. EXEC RAMPAT (1, 2, 3, 4, 5, 6) ;
   - PINS 2, 3, 4, 5, 6 ARE THE X ADDRESSES

3. EXEC RAMPAT (2, 12, 11, 10, 9, 7) ;
   - PINS 12, 11, 10, 9, 7 ARE THE Y ADDRESSES

4. EXEC RAMPAT (3, 15) ;
   - PIN 15 IS THE DATA INPUT PIN

5. EXEC RAMPAT (5, 1) ;
   - PIN 1 IS THE OUTPUT PIN

6. EXEC RAMPAT (7, 13) ;
   - PIN 13 IS THE WRITE INPUT PIN

THE RAM IS NOW COMPLETELY DESCRIBED

Writing and reading the RAM is accomplished with very little user effort. Only two statements are required to write and they are shown as follows; the patterns, of course, are given a code to represent the various patterns that are currently available and the code space is large enough to include room for future growth. Reading the RAM requires three statements and we will give a complete test and display of the fail matrix. Now these statements are simple, convenient and easy to invoke. However, to program a device such as a RAM in older software systems requires literally thousands of words to accomplish what is essentially a relatively simple function.

WRITING AND READING THE RAM IS ACCOMPLISHED WITH LITTLE USER EFFORT

- WRITING PATTERNS REQUIRES ONLY TWO STATEMENTS:

  1. SET M O
  2. EXEC RAMPAT (N)

  WHERE:

N	PATTERN
100	O's
101	CHECKERBOARD
102	COLUMN BARS

ETC.

- READING THE RAM REQUIRES ONLY THREE STATEMENTS FOR COMPLETE TEST AND DISPLAY OF FAIL MATRIX

  1. SET M 1
  2. EXEC RAMPAT (42)
     (ENABLE FAIL MATRIX PRINT-OUT)
  3. EXEC RAMPAT (N)
     (N DEFINED AS ABOVE)

OPERATIONS REQUIRING THOUSANDS OF WORDS IN OLDER SYSTEMS

Special measurements such as "time" can be accommodated by the Rampat approach. This very simple sequence of events is illustrated here. Write the desired pattern, enable the Time Machine, read the pattern but instead of using the functional pattern results available to a user without the Time Machine, in this case we would use the Time Machine results. (See example). Essentially what we have here is the description of the Ram there at the bottom portion of the program. The calling of the Time measurement capability carried on the top of the next page, also, identifying the X addresses, Y addresses and the various terminals associated with the device and then finally using the time results. So the basic technological thrust, of course, has been to ease the hardware, ease the software, to describe and test complicated devices.

TIME MEASUREMENTS ON RAMS USING THE FACTOR & RAMPAT COMBINATION ARE EQUALLY SIMPLE & EFFECTIVE

- WRITE DESIRED PATTERN
- ENABLE TIME MACHINE
- READ PATTERN, BUT USE THE TIME MACHINE RESULTS INSTEAD OF FUNCTIONAL PATTERN RESULTS

SEE EXAMPLE:

```
000067      REM ENDD SUBR HOOKAL;
000067
000067      SUBR PGWRIT;
000067      SET TCH2
000070                  DELAY 3E-6,
000070                  WIDTH 1E-6,
000070                  TR 10E-9,
000070                  TF 10E-9,
000070      OFFSET -.7,
000070      AMP -1.0,
000070                  BURST 1;
000070      END;
000070      REM ENDD SUBR PGWRIT;
000070
000070      SUBR WRITAL (PATRN);
000070      REM WRITE PATTERN TO RAM VIA CAALLING PARAMETER;
000070      SET M * [61] 110;
000071      EXEC RAMPAT (PATRN,0,0);
000072      END;
000072      REM ENDO SUBR WRITAL;
000072
000072      SUBR PG1RD;
000072      SET TCH1
000073      DELAY 3E-6,
000073                  FWIDTH 150E-9,
000073                  TR 4E-9,
000073                  TF 4E-9,
000073      OFFSET -.7,
000073      AMPL -1,0,
000073                  BURST 1;
000073      END;
000073      REM ENDD SUBR PG1RD;
000073
000073      SUBR HOOK1;
000073      EXEC RAMPAT (20,32,16,1); REM X0 NOT USED BY RAMPAT;
000074      EXEC RAMPAT (21,3,4,5,6); REM ROW ADDRESS;
000075      EXEC RAMPAT (22,12,11,10,9,7); REM Y ADDRESSES;
000076      EXEC RAMPAT (23,15); REM DATA INPUT;
000077      EXEC RAMPAT (25,1); REM DATA OUTPUT;
000100      EXEC RAMPAT (27,13); REM CLOCK PIN;
000101      END;
000101      REM ENDD SUBR HOOK1;
000101
000101      END; REM ENDD PROGRAM;
```

```
00012       CALL TTIME; REM ALL TESTS DONE IN SUBR TTIME SO VEE CAN BE ITERATED;
00013
00013       SUBR TTIME;
00013       ASSIGN A1/2,B1/3,C1/4,D1/5,E1/6,B2/14; REM A2/13 ASSIGNED;
00013       ASSIGN A2/13; REM REMOVE;
00013       STDLY=10E-6;
00014       SET DELAY STDLY;
00015       XCONF TCH1 2;
00016       XCONF TCH1 3;
00017       XCONF TCH1 4;
00020       XCONF TCH1 5;
00021       XCONF TCH1 6;
00022       XCONF TCH2 14;
00023       CONF TCH2 13;                          REM WE CLOCK;
00024       SET D * 01111 11011 11111;
00025       SET TRB * [16] 11111 11011 11011; REM TRB1 LOAD, REST CAPS;
00026       SET M [61] 11111 11;
00027       SET F [61] 11111 11; REM DISABLE ALL PGS AND TCH0;
00030       CALL PGWRIT;                           REM SETUP PG2 FOR RAMPAT;
00031       CALL HOOKAL;  REM CONFIGURE RAMPAT FOR WRITING 1024 BITS;
00032       SET LOGIC POS;
00033       SELECT GENERATOR;  REM NOTIME TESTING BUT PG CYCLES;
00034       CALL WRITAL (103); REM WRITE ROW BARS;
00035       SET M [61] 101;    REM TURN OFF PG2 TURN ON PG1;
00036       CALL HOOK1;   REM PG1 ON X0, RAMPAT ON REST OF ADDRESS PINS;
00037       CALL PG1RD;  REM CONF PG1 TO READ PULSE SPECS;
00040       CONF TCH1 2;  REM CONNECT PG1 TO PIN 2 X0;
00041       SET TRB [16] 1 (15:0);
00042       SELECT TIME;
00043       SELEGT TMEAS 20;  REM PG1 PULSE FOR EVERY SET F FROM RAMPAT;
00044       REM 00 TAA POS-POS FOR 0-1 TRANSITIONS;
00044       SELECT TPD NEG,POS,2,1;
00045       SET TMRC 1;
00046       SET TMBC 1;
00047       SET TMEC 1;
00050       SET BTHV -1.30;
00051       SET ETHV -1.15;
00052       ENABLE TCT1 GT 55E-9;
00053       ENABLE TCT0 LT .1E-9;
00054       LOOP69;
00054       EXEC RAMPAT (42); REM ENABLE FAIL MATRIX;
00055       EXEC RAMPAT (103,0,0); REM READ;
00056       IF SWITCH EQ 69 THEN GOTO LOOP69;
00060       END; REM ENDD SUBR TTIME;
```

Here we would like to describe new functions which were not required and were not available on older software technologies. This is the use of the test system and the use of the test system's results, so that the user orients his skill on obtaining test feedback into the manufacture of the device and the use of the device, rather than being constantly preoccupied with simply getting the tester to run.

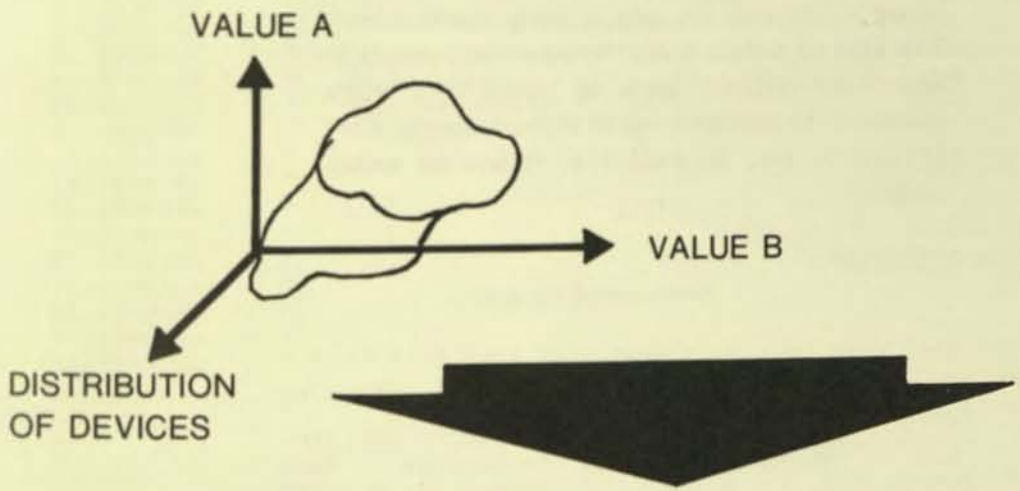
Many test systems provide bar graph or semi-curve plots or parametric distributions and literally require the user to connect the points as when we were children in school in order to obtain the desired curve. These are of course very useful data plots because they describe the relative distribution of goodness versus parametric value for the device.

Newer devices not only require this kind of information but also need to have information related to the safe area of operation or the accepted area of performance, and at the same time obtain the distribution of the devices. So literally we are asking for what sounds at face value to be an impossibility, a "SCHMOO" plot, and further a schmoo plot in three dimensions so that we have value A versus value B and height of the plane above value A and value B plane is the distribution of the devices in the population. There's no way to obtain this kind of information with assembly base programming techniques.

FAIRCHILD SYSTEMS' ADVANCED SOFTWARE SYSTEM ALLOWS THE USER TO CONCENTRATE HIS SKILL ON THE USE OF THE TEST SYSTEM---INSTEAD OF DETAILED CODE TO RUN THE SYSTEM

FOR EXAMPLE---EARLY SYSTEMS DEVELOPED PRIMATIVE "BAR-GRAPH" PLOTS OF PARAMETRIC DISTRIBUTIONS & REQUIRED THE USER TO DRAW THE CURVE

ADVANCED MSI & LSI DEVICES REQUIRE MUCH MORE INFORMATION--- PREFERABLY IN "SHMOO" PLOT FORM - AND IN 3 DIMENSIONS!!



EFFECTIVELY IMPOSSIBLE FOR ASSEMBLY BASED PROGRAMMING APPROACHES

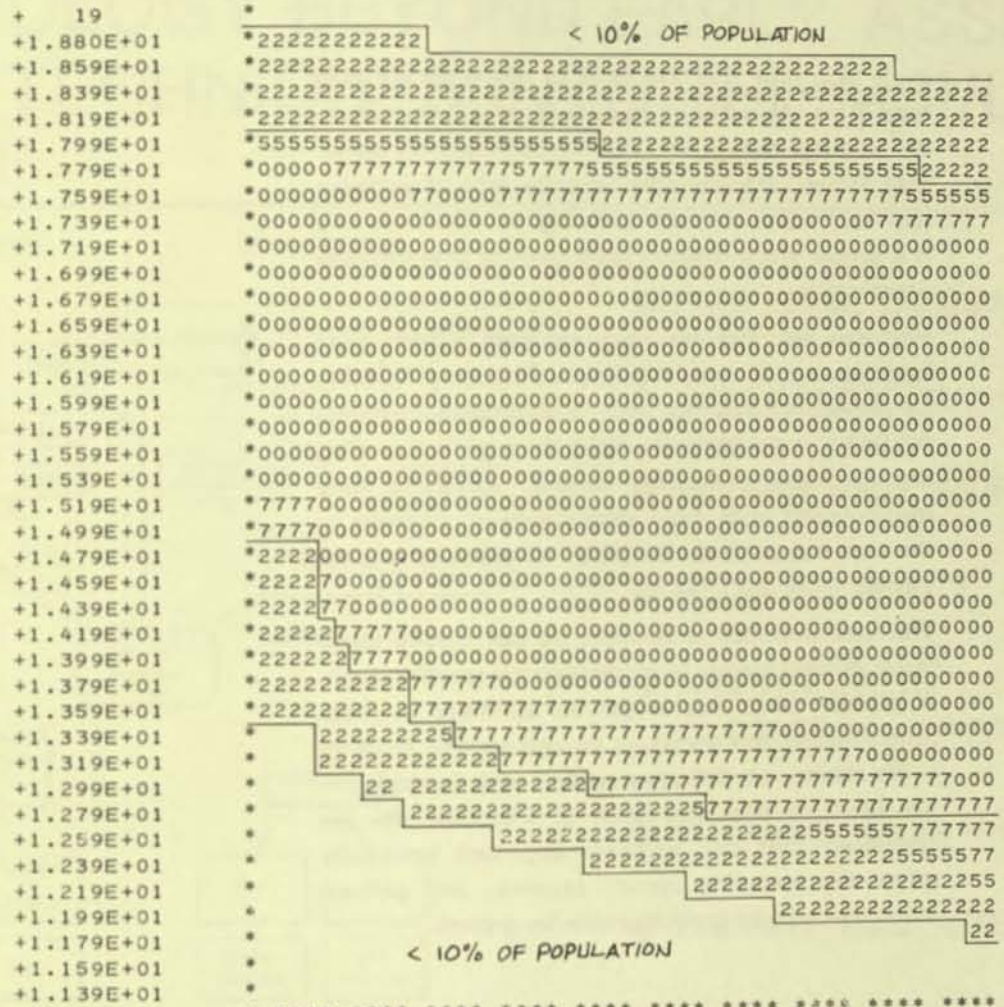
Illustrated here is one of these complex device schmoo plots. We won't go into the values and parameters shown, but basically we do have a schmoo, we do have 100% of the population shown as the central portion of the schmoo. In this particular plot we've taken the next 70 percentile followed by 50 percentile, 20 percent, on down to less than 10 percent of the population.

The value of a plot like this is enormous to the user who is looking for balanced distribution in his process as well as the detection of anomalies. Although this particular example contains no anomalies in the 100 percent profile, we have seen some plots with a hole in the center of the distribution which is not accountable with regards to the process, but leads to the conclusion that there is something fundamentally wrong in the way the part is being manufactured. This kind of a chart is read by very many people in very many different ways to obtain data that's impossible to appreciate when it is constantly constrained to two dimensions as it was on earlier systems.

STATID

SHMOO FLOT OF VDD VERSUS CHIP SELECT INTERVAL

ORDINATE VALUES
VDDMAX = 19 VDDMIN = 11 DELTA = +2.000E-01
COMPOSITE SHMOO PLOT -- DEVICE NUMBER 11



ABSCISSA VALUES:
XMAX = +1.300E-07 XMIN = +5.000E-08
DELTA = ±1.600E-09

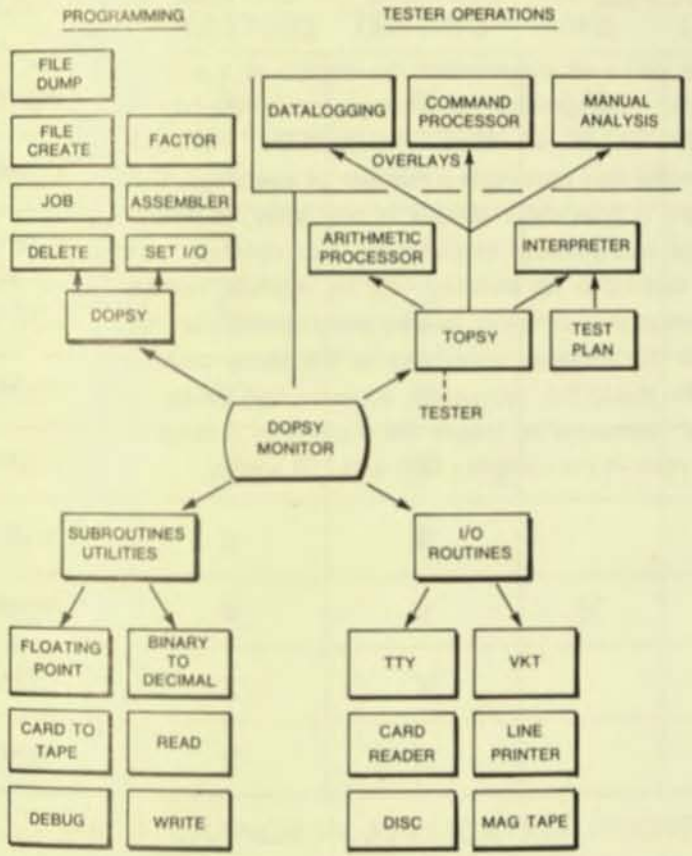
5 = +5.800E-08 20 = +8.200E-08 35 = +1.060E-07
10 = +6.600E-08 25 = +9.000E-08 40 = +1.140E-07
15 = +7.400E-08 30 = +9.800E-08 45 = +1.220E-07

Let's stop now and take store of where we are with regards to the software requirements and the assembly language techniques. You'll recall the chart earlier that showed the assembly language type of software and the kind of software provided by Fairchild. This is a simple block diagram once again of that software organization.

You can see that we have achieved a high level language, we do have maximum program efficiency, we provide mass storage with its accompanying media flexibility, we extensively assist the user in managing the hardware under his control. Advanced data manipulation aside from simple passing of results to the user has been shown to be an absolute requirements.

The user interface is flexible, he can invoke many many different ways to accomplish his specific result. A problem that was major on assembly language programs was this particular canned routine problem – no choice, no definition and no way to change – the problem does not exist at Fairchild. We are convinced that our software approach essentially solves the complete system problem, and perhaps more importantly provides room for growth.

FAIRCHILD SYSTEM'S ADVANCED SOFTWARE SYSTEM CLEARLY EVOLVES TECHNOLOGY BEYOND EARLY ASSEMBLY LEVEL TECHNIQUES INTO THE MSI/LSI FUTURE



- HIGH LEVEL LANGUAGE
- MAXIMUM PROGRAMMER EFFICIENCY
- MODERN MASS STORAGE
- MEDIA FLEXIBILITY
- ASSISTANCE TO THE USER FOR COMPLEX HARDWARE CONTROL
- ADVANCED DATA MANIPULATION
- FLEXIBLE USER INTERFACE
- SOLVES THE "CANNED" ROUTINE PROBLEM

SOLVES THE COMPLETE SYSTEM PROBLEM

No discussion on software can be complete without at least a brief mention of the management of software. For example, many early systems had a specific software module to perform either a specific function or to relate to a specific configuration of the system. What we've done here is tabulate an earlier software approach. Across the top of the page you can see listed either a digital technique or a linear testing problem; various kinds of peripherals, and then we have the software modules that are designed to perform a specific system function. We've simply drawn there with X's, the intersection of each module in each of the packages required to do a job. For example, on P507, it's used in both linear and digital, magnetic tape cartridge is used as the engineering monitor and provides a capability for a second TTY. If you were to change the magnetic tape cartridge management software, you not only impact P507 but also 508, 510 and 511. In fact, a change in application scope could impact as many as 10 to 15 modules. A change in hardware could, therefore, be in conflict with various software modules provided across the line.

So! As we're all accustomed to change as a way of life, the management of change now requires a management of all these intersections. Fairchild abandoned that technique a number of years ago. Our software is essentially always in one body, is always updated and checked at the factory completely, and is rev leveled in its entirety, not by module, not by application and certainly not by constraining the user to find the software anomalies in his tester and his site. We think this represents a useful and powerful control technique to insure the success of a modern test system in the complex MSI and LSI arena.

EARLY SOFTWARE APPROACHES REQUIRED SPECIAL MODULES OR 'PACKAGES' FOR SPECIFIC OPTIONS OR APPLICATIONS

MODULE	DIGITAL TESTING	LINEAR TESTING	PAPER TAPE	MAG-TAPE CARTRIDGE	ENG. MONITOR	END-OF-LIFE	SECOND TTY
P501	X	X	X				
P503	X	X	X		X		
P502	X	X	X			X	
P504	X	X	X				
P506	X	X	X			X	
P507	X	X		X	X		X
P508	X	X		X		X	
P509	X	X	X		X		
P510	X	X		X	X		X
P511	X	X		X			

- A CHANGE IN APPLICATION SCOPE COULD IMPACT 10-15 MODULES
- A CHANGE IN HARDWARE COULD BE IN CONFLICT FROM APPLICATION TO APPLICATION

THE SENTRY SOFTWARE CONTAINS ALL FUNCTIONS IN ONE REV LEVEL CONTROLLED BODY

Sales Offices

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Sunnyvale, California 94086
(415) 962-2231 / 962-2481
TWX: 910-373-1204

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(516) 487-5300

Texas

P.O. Box 874
Richardson, Texas 75080
(214) 231-9351
TWX: 910-867-4720

FOREIGN LOCATIONS

Germany

Fairchild Automation Systems, GMBH
Truderingerstrasse 13
8 Munich 80
West Germany
Telephone: 47 60 25/26
Telex: 523184

England

Fairchild Systems Technology
Grove House
551 London Road
Isleworth, Middlesex, England
Telephone: 560-0838/9
Telex: 0051-24693

France

Fairchild Systems Technology
10 Rue Du-Seminaire
94150 Rungis
Paris, France
Telephone: 686-51-50
Telex: FAIRP AR 26937 F

Japan

Fairchild Systems Technology, Ltd. or
Tokyo Electron Labs (Sales Rep)
Meiho Building
1-21, Nishishinjuku
Tokyo 160, Japan
Telephone: (03) 343-4411
Telex: (232)-2240 LABTEL

For information on other worldwide locations: Contact
Fairchild Systems Technology headquarters in Palo Alto, California

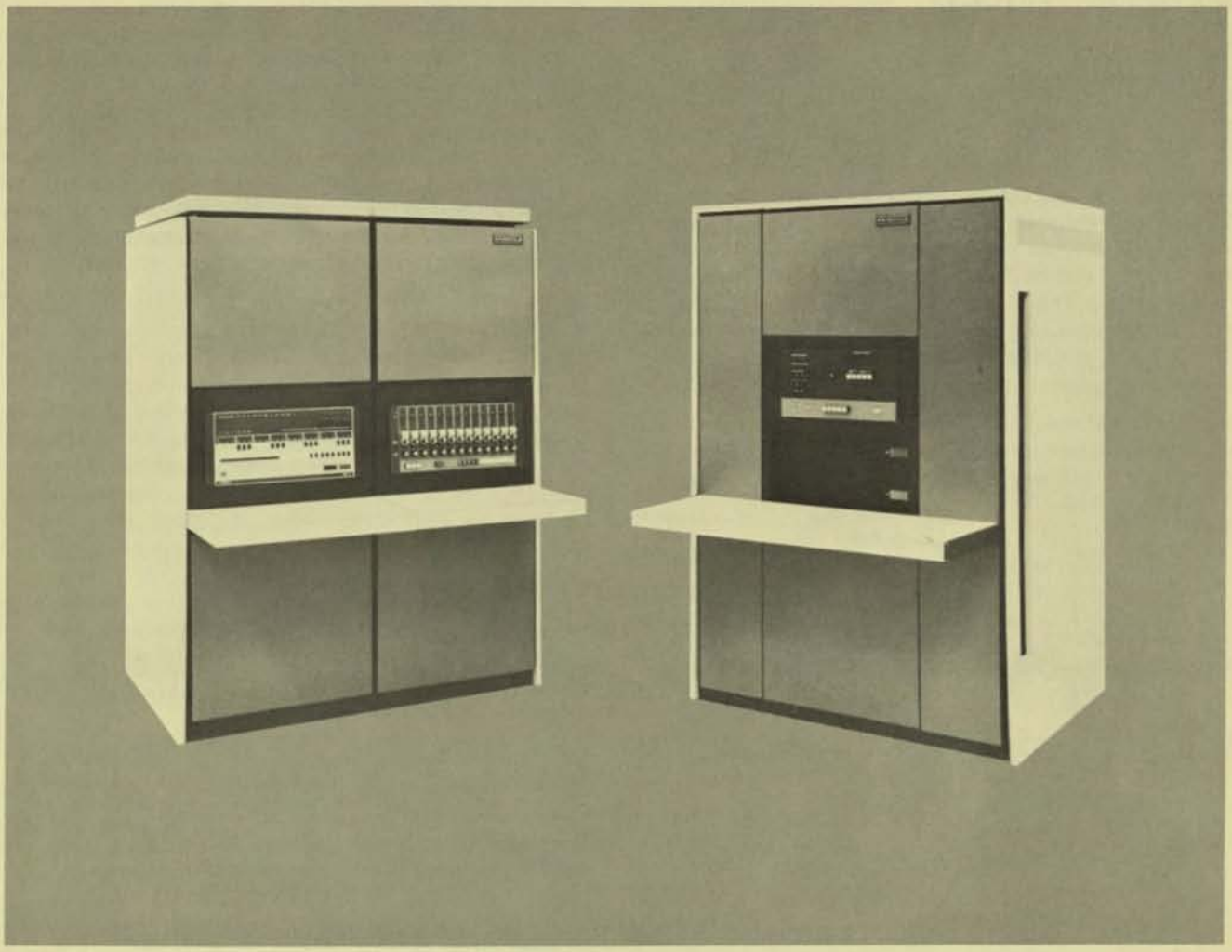
FAIRCHILD
SYSTEMS TECHNOLOGY

3500 Deer Creek Road
Palo Alto, California 94304
(415) 493-5011 • TWX 910-373-1204

FAIRCHILD
SYSTEMS TECHNOLOGY

Fairchild Systems Technology, a division of Fairchild Camera and Instrument Corporation
3500 Deer Creek Road Palo Alto, California 94304 (415) 493-5011

System Description **Computer Controlled Test System Series** **Sentry 400**



INTRODUCTION

It is generally recognized that computer-controlled test systems are needed to test large-scale integrated arrays, printed-circuit modules and other digital subsystems, because the test sequences are extremely long and variable. The capital cost is necessarily high, obligating the designer to protect the investment against obsolescence as well as to reduce direct costs of testing and data processing.

These interrelated requirements are satisfied in the Sentry 400 Series of LSI/MSI test systems by a powerful new computer, a software package developed specifically to make the programming and execution of binary network testing more efficient, and modularly expandable test stations. The Sentry 400 represents at least an order of magnitude improvement in test capability with nothing like a corresponding increase in capital cost. It can test as many as four networks with up to 120 terminals each at rates some 30 times as fast as previous systems (see test capabilities summary in Table 1).

TABLE 1. SYSTEM CAPABILITIES SUMMARY

Operating modes	Automatic, Manual, Monitor
Automatic test rate	Functional, to 286,000/sec DC parameters, 250 pins/sec
Applications	Binary network test (LSI, MSI, MOS, bipolar, PC modules, etc.)
Network complexity	To 240 terminals, combinatorial or sequential
Test stations	Maximum of 4 independent stations (multiplexed)
Control computer	FST-1, 24-bit word length
Software systems	Interpretive operating systems, Algorithmic compiler

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FAIRCHILD
SYSTEMS TECHNOLOGY

SENTRY 400 FEATURES

A minimum Sentry 400 system will perform static and dynamic tests on one 30-terminal combinatorial or sequential network at a time. Instrumentation expansion modules can be added in 30-pin increments to a total of 480 pins at four independently operating, 120-terminal test stations.

Logic and memory functional test rates can range up to 286,000 tests per second. Absolute DC parameter measurements, such as input pin leakages and saturation voltages, are made at a rate of 250 tests per second at each station, on a pin-by-pin basis. Forcing and sensing ranges (Table 2) encompass bipolar and MOS semiconductor requirements. Utility inputs are supplied for addition of special external sources.

Word length of the new FST-1 control computer is 24 bits. Its software is configured to permit programming of up to 240-pin tests without modification. Also, the operating software enables production and engineering personnel to modify test procedures and run desired programs with a set of commands written in simple, readily understood language. The interpretive software and the selected test routines are stored in the computer's core memory for high-speed processing.

The computer is a general-purpose machine that may be used for other data-processing and control functions. It also controls auxiliary test equipment, such as wafer probes and packaged device or module handlers at the test stations.

To facilitate both production and engineering test applications, all Sentry 400 systems operate in three modes: automatic, for high-speed testing without operator intervention; manual, for program debugging and other single-step functions; and monitor, which allows authorized users to modify test conditions, display test responses, and insert special test-data requests and analysis subroutines in the

TABLE 2. ELECTRICAL SPECIFICATION SUMMARY

Programmable unit	Maximum Number	Maximum Range	Resolution	Special Features
Functional test driver	120*	±30.72 Volts at ±40mA	10mV/40mV in 2 ranges	Current limits at 50mA, short circuit protected, maximum slew rate 30 volts/μsec.
Functional test comparator	120*	±30.72 Volts; 5MΩ	10mV/40mV in 2 ranges	Detects open circuit lines, monitors inputs and outputs, 0.4μsec response time for 10mV overdrive at −30 to +30 volts.
Precision measurement unit	1*	±40.92 Volts; ±102.3mA	1mV/40mV in 3 ranges 1nA/100μA in 4 ranges	Voltage or current force and sense, programmable current and voltage limit, 60μs A/D converter (11 Bits).
Programmable power supply	3	±40.92 Volts; ±1.023 Amp	10mV/40mV in 2 ranges 0.1mA/1mA in 2 ranges	Voltage or current force and sense, go/no-go trip output for over or under current or voltage, current/voltage magnitude measurement 3 msec settling time to 0.1% of full scale.
Programmable reference	10	±30.72 Volts at ±40mA	10mV/40mV in 2 ranges	Four references for functional test drivers, two for functional test comparators, four for low current bias supplies, 3 msec settling time to 0.1% of full scale.
Time delay	1	5.73405 sec	0.35μsec/0.35msec in 2 ranges	
Clock-burst generator	1	255 sync pulses	1 sync pulse	
Sync output	4	T^2L Driver 0 to 5 Volts		
Socket identification		32,767 codes		Large number ensures proper load boards to test program correspondence.

*In one standard test station enclosure. Software is configured for up to 240 pins. Two 120 pin test station enclosures are used for a 240 pin tester configuration.

test program. Combinations of these modes may be employed in a multi-station system without interference among the test stations.

Programs may be interleaved, by assigning test functions to specific input/output pins at the test stations, so that several unique networks may be tested simultaneously. When several stations are multiplexed to the central control system, the computer will process the network responses from the previously selected station and prepare the control data for the next station during the interval required for execution of a test sequence at the selected test station. This interval includes response time of the instrumentation in the test station and propagation delay through the network being tested.

The 240-terminal limit on tested network size is based upon the anticipated practical restrictions in LSI packaging technology. It does not restrict test capabilities with respect to internal network complexity, which may include numerous feedback loops and buried states. Nor are the test applications restricted to semiconductor memory and logic. PC modules and, in fact, any components resembling binary networks may be tested economically. For example, the user may employ test adapters to check out wiring-path continuities in multilayer circuit boards and computer backplanes.

GENERAL DESCRIPTION

Overall, a Sentry 400 system resembles a general-purpose computer in its operation. The computer views the instrumentation much like a peripheral subsystem, busing out control data and receiving subsystem status reports, interrupt requests and test data through its input-output interfaces. The basic system organization and main data flows are outlined in Figure 1.

Test programs are transferred from the bulk storage, a disc file, to the computer's core memory and processed to generate tester commands such as assignment of logic levels to designated test pins, comparison of device output functions with programmed references, and switching of DC forcing voltages and currents to selected pins. This data is multiplexed to the test stations, where the forcing and measuring circuits are located. After performing the measurements and comparing device outputs against reference values, the test stations return digital response data to the central system for analysis and automatic data logging.

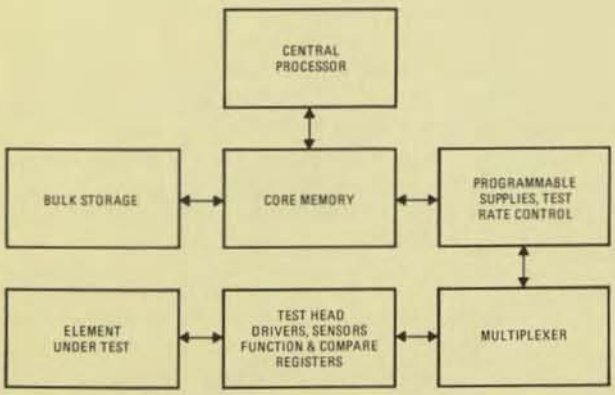


Figure 1

System Configurations

Two typical expanded Sentry 400 systems, one representative of system production-testing subsystems or LSI arrays of various complexities and the other a production and engineering test center, are illustrated in Figures 2 and 3.

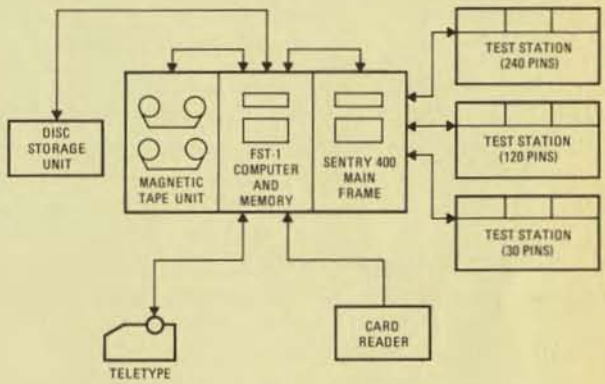


Figure 2

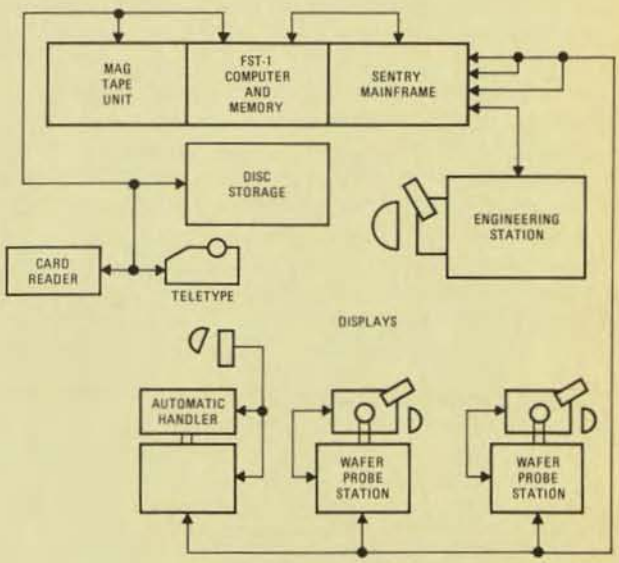
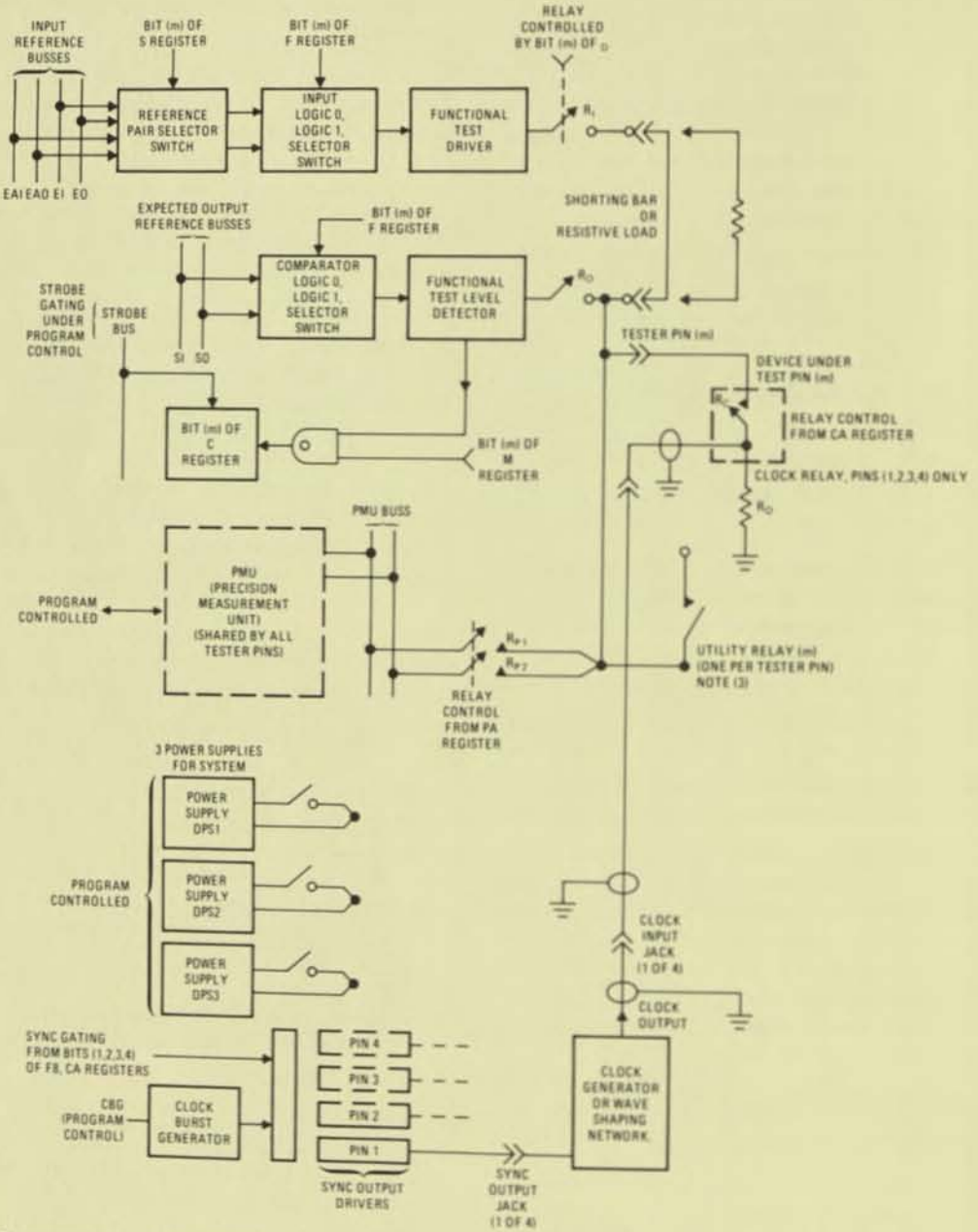


Figure 3

A disc file facilitates program assembly and storage. The file also refreshes the computer memory when long programs are run. About 350 test programs averaging 1,500 instructions each can be stored on disc along with the computer operating systems software.

A card reader to enter new programs will free the teletypewriter for data logging and communications between users and computer. Magnetic tape decks increase on-line program capacity, retain data in the format needed for more detailed analysis, and facilitate exchanges of programs and test data among test and engineering groups.

Each "pin" at the test stations involves associated sense, force, and utility connections, drivers, sensors, forcing and compare register positions, and so forth. Figure 4 illustrates a few of the pin control-reponse and test conditioning loops at a test station (the details will be discussed later). A mix



NOTES:

(1) RELAYS R_I, R_D, R_C DISABLED WHEN RELAYS R_{P1} & R_{P2} ARE ENABLED.

(2) SYNC OUT OCCURS WHEN BIT (m) OF F REGISTER AND BIT (m) OF CA REGISTER ARE TRUE. NUMBER OF SYNCS CONTROLLED BY CLOCK BURST COUNT.

(3) UTILITY RELAY (m) CONTROLLED BY BIT (m) OF R REGISTER.

(4) RELAYS R_I, R_D, R_{P1}, R_{P2} DISABLED WHEN RELAY R_C IS ENABLED BY CA REGISTER (5).

Figure 4

of pin complements may be employed at the various stations of an expanded system. Combinations like the one in Figure 2—which can test networks having 30, 120 and 240 terminals (or less)—may be used to cover the full range of a component or system manufacturer's production and R & D requirements.

Logic Function Tests

Functional tests are executed by forcing programmed logic levels on the input terminals of the assembly, wiring matrix or semiconductor logic or memory array under test. After an interval including the correct propagation delay through the network, output comparators are strobed to determine whether the network produces the expected responses in the proper time relationship. During this delay, the central processor will generally be processing responses from a previous test and formatting the control data needed to execute the next test in a sequence.

Pin output loadings can be simulated and go/no-go responses isolated to a single pin on displays or readouts. In essence, the computer compares the device to a software model.

The functions tested may be combinatorial or sequential, defined as:

- Combinatorial logic networks contain no internal storage elements (buried states) and/or have no feedback loops.
- Sequential networks may contain both logic and storage elements (internal states) and may also have feedback loops generating buried states. An example is a read-only memory simulating a binary counter.

To test the sequential networks, the system can be programmed to generate complex sequences of input pulses so that the comparators can explore the output configurations based on a history of known events.

The outputs of a large network may have many redundant and "don't care" states. Therefore, the Sentry 400 software has been configured such that the user can mask these states out of the logical compare operations, to increase the throughput of meaningful test data. Another means of improving system efficiency that is provided in the Sentry 400 is assignment of logic levels "broadside" to groups of pins in the test heads. Once the initial pattern of logical "1" and "0" conditions for a group of pins is set up, only the changes in states desired for a specific pin, or pins, need be programmed for the remainder of the tests on that network.

Pairs of logical "1" and "0" reference levels are set up on dual reference supplies in the central instrumentation subsystem. The levels are bused to the selected pins as part of the multiplexed operation. A Sentry 400 may contain up to five dual reference supplies so that a variety of steady-state references are continuously available within the system.

Precision DC Measurements

The main constraint on absolute DC parameter measurement rate is the desirability of using only one precision measuring unit per test station, to reduce system cost. The pins are connected to this unit selectively through a matrix of high-frequency switches that will not degrade test-signal accuracy. The rate of 250 measurements per second per station (4 msec per individual test) provides ample time for signal switching and settling, as well as for measurement functions such as output comparison and analog-to-digital conversion.

As a rule, this rate will not significantly lower system throughput, because the number of absolute DC tests per program is typically very small compared with the number of logic function tests. If a pin is assigned solely to the precision measurement unit for a test, it will automatically be returned to its previous logic condition when released from the unit. At other times the pin is maintained in its assigned logic condition.

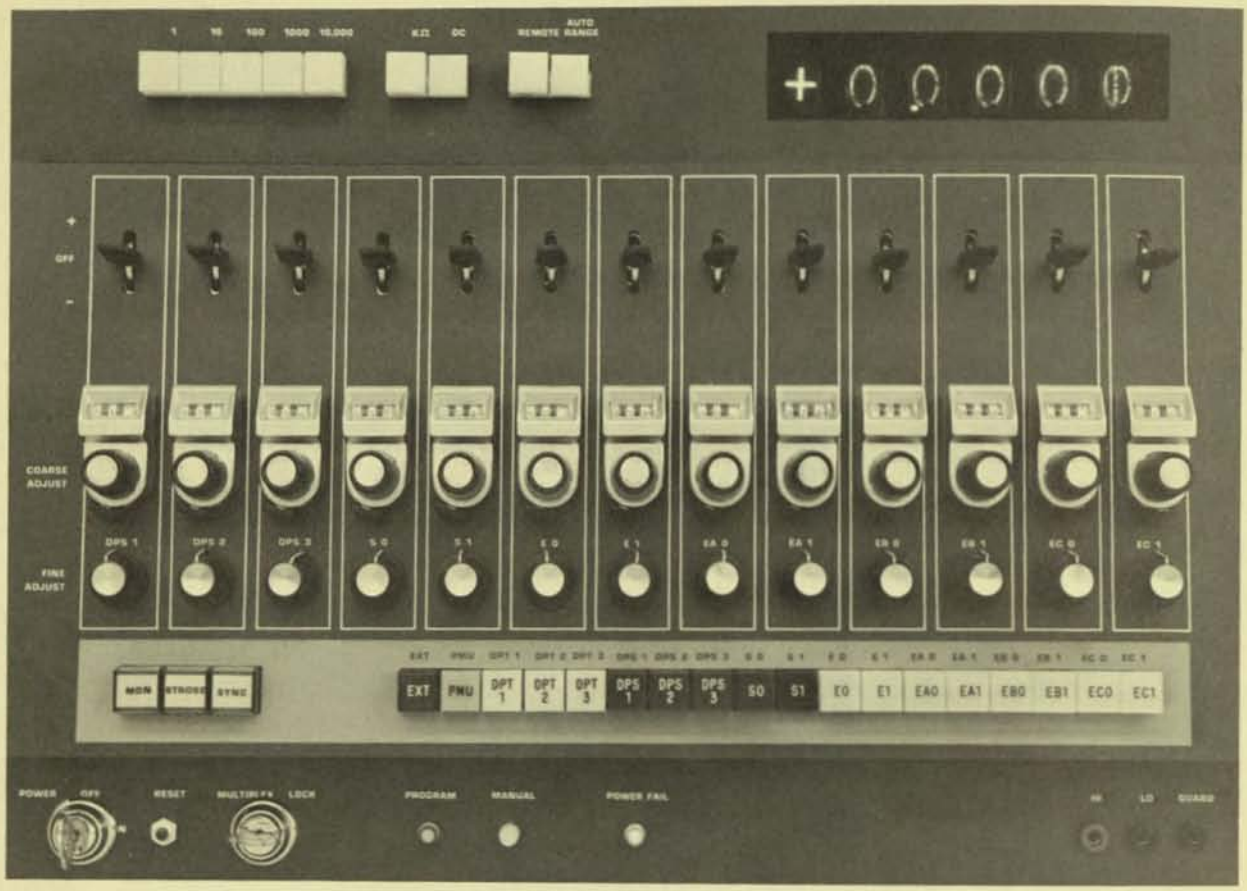
The precision measuring unit also checks the test supply levels during system self-test operations. Any variation from the programmed levels will generate a priority interrupt to the computer.

Operating Modes

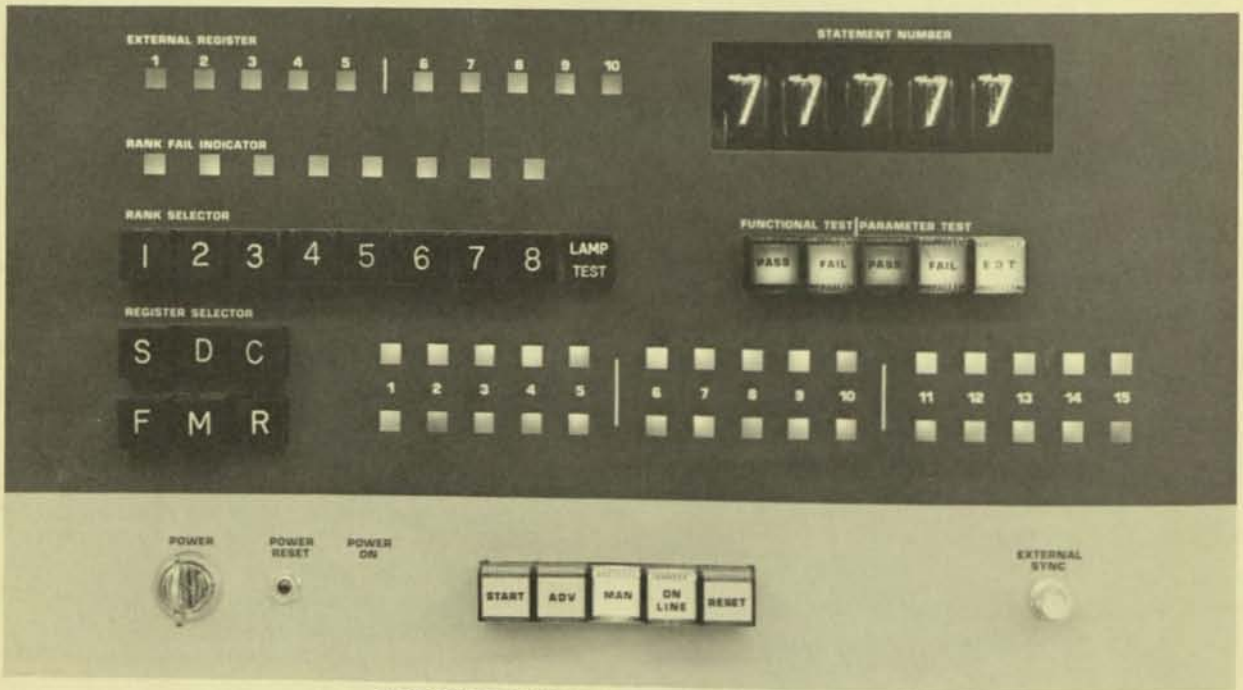
The normal operating mode of the Sentry 400 is the high-speed automatic mode under full computer control. Automatic programs can be written to accommodate operator and handling equipment functions such as reloading test stations. However, programmers, engineers conducting development tests, and other personnel with special requirements or authority may intervene in the automatic operation of any station and use the manual or monitor modes.

As a rule, programmers use the manual mode to debug or verify programs. The programs are written as a sequence of commands which are translated by the system compiler into specific settings of the tester instrumentation, reference supplies, switches and so forth. The manual mode allows the user to select displays, such as the contents of a specific function-forcing or compare register, so he can verify that the programming statements were written correctly and in the desired sequence. The user presses the start button at a test station to execute each step in a program for that station. Program steps may be edited via the teletypewriter, or by placing correct instructions in the card reader.

The monitor mode can only be enabled by authorized personnel (the mode switch is locked). It allows the user to modify and experiment with test conditions at a given station. It is intended primarily for R & D, engineering and system calibration operations. The special monitor control panel and displays are used to observe system voltage and current levels, modify them while observing the element being tested, check out power supply levels, run the strobe signals through an oscilloscope, etc. All programmable



MONITOR CONTROL PANEL



TEST STATION CONTROL PANEL AND DISPLAY

power supply settings can be overridden by the monitor controls. Digital readouts allow pre-selection of manual settings before activation, to ensure protection for the device under test.

In the monitor mode, the user can also request special services of the central processor, with the simplified interface programming language. As an example, he might instruct the computer through the teletypewriter to insert the following steps into the test program being run:

- Stop on first failure
- Stop on instruction N
- Modify test rate (e.g., use a software counter to slow the test rate to 1 test per second)
- Recycle subroutine X so response waveforms may be observed on an oscilloscope
- Datalog all logic and/or DC no-go results, along with specified go results
- Change test program at station A.

Since the user can command a combination of automatic, manual and monitor modes of operation, test rates in manual or monitor can approach the full automatic rate of up to 286,000 tests per second. For instance, should a programmer need only to reverify certain sequences in a test program after an initial debugging run, he can command the system to stop for manual operation at the start of those sequences. Likewise, as shown by the monitor example list above, operation is automatic except during interventions requested by the user.

The monitor control panel is centrally located on the Sentry 400 main frame and can be used to monitor any station. Manual operation is controlled and observed with the panel at each station. After executing a program step at any station, the central system will execute the steps programmed for the other stations before returning to the controlled station. Therefore, operation of a station in manual or monitor modes does not normally inhibit automatic operation at other stations.

CENTRAL CONTROL SYSTEM

The control system is memory oriented. That is, the central processing unit (CPU) in the computer, the tester and all peripherals interface with the core memory through buses (Figures 5, 6, and 7).

The accumulator bus is the input/output channel for control data transfers. It is under direct control of the software. In addition, two other interfaces are provided:

- Access directly into the core memory through the memory buses, so that data transfer operations such as loading core memory from the disc file can be performed at high speed.
- Priority interrupt system that implements the necessary decision controls. Interrupt priorities are assigned to certain operating conditions and various types of failures.

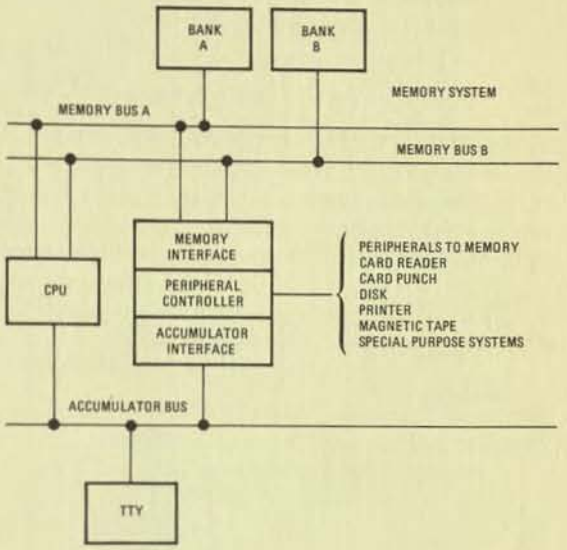


Figure 5

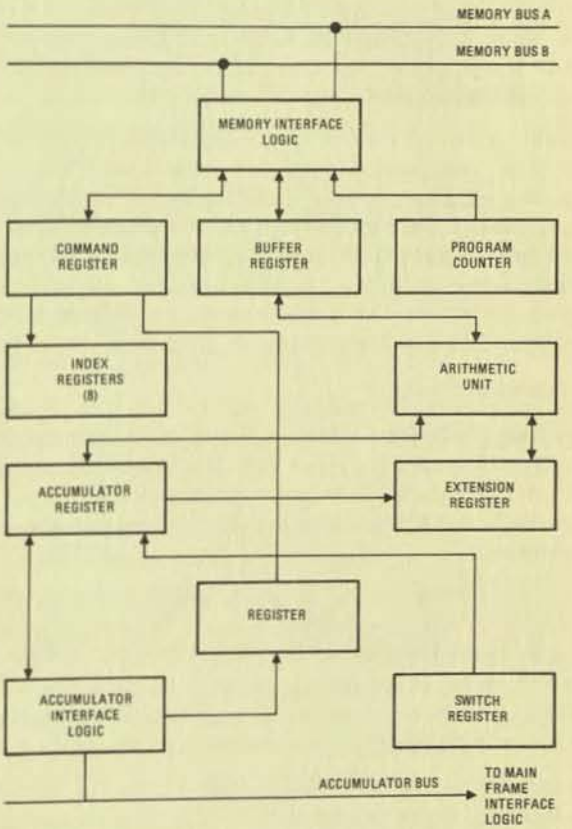


Figure 6

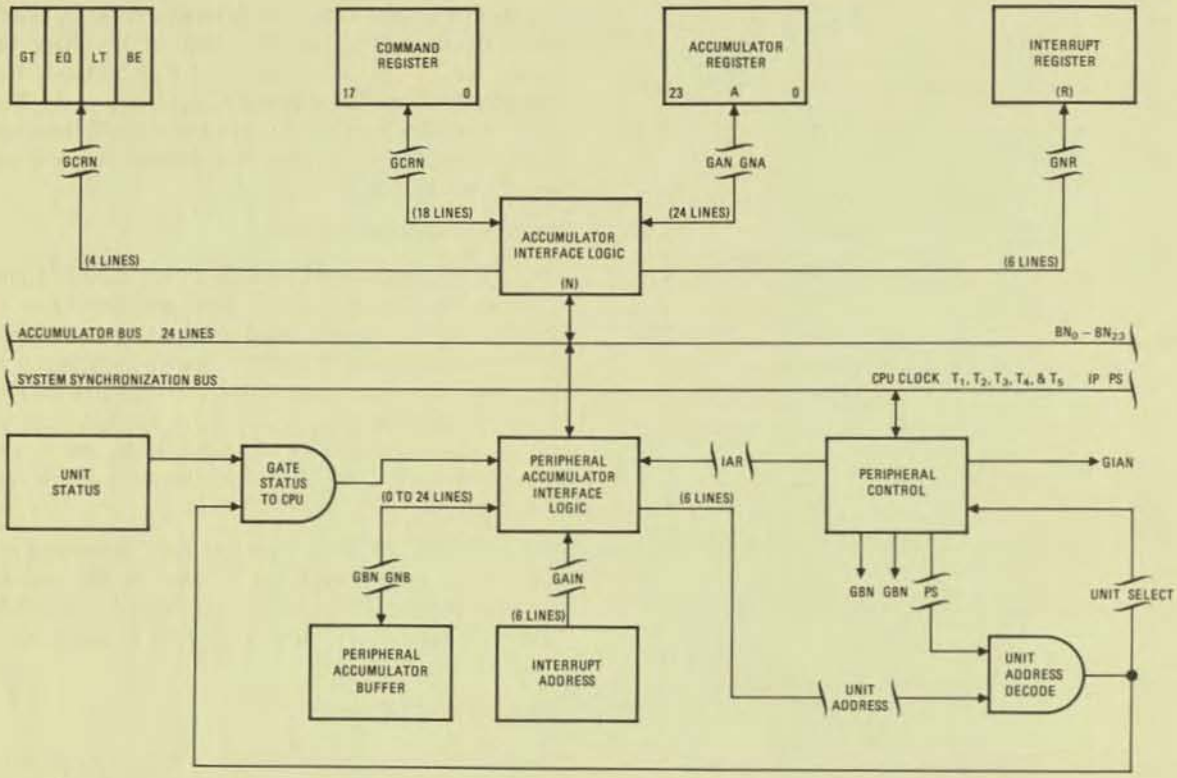


Figure 7

Test-Control Registers

Several registers in the test system operate peripherally with the CPU. Three with considerable authority are: the function (F) register, which is loaded with the desired input functions and the anticipated output functions of the network being tested; the C register, which receives the digital response patterns from the sensing circuits and makes a logical comparison; and the M register, which masks the responses to prevent processing of "don't care" conditions.

Comparison Timing

The comparison instructions include a strobe operator that sets the delay between input force and output comparison. The strobe gates the data from the compare sensors in the test head, and also actuates the logical mask and compare operations.

A strobe may be delayed by a programmable counter (TD) or gated by the simultaneous presence of suitably located bits in a strobe-enable register (SE) and the F register. A counter delay is normally programmed for combinatorial testing. The more complex input histories of a sequential test are supplied by four programmed sync generators.

A timing sequence for a typical combinational test is shown in Figure 8. A nominal delay of 0.7 μsec is incremented to allow for input rise and fall times, network delay, and test system response times.

All four sync lines may be gated by the first four bits of the F register before being delivered to a sequential network's clock inputs. A clock-address register (CA) defines the lines used and TD the pulse period. A generalized sequential timing pattern is illustrated in Figure 9A; Figures 9B and 9C are an example of a four-phase clock and the program statements that generate it. If the network requires more complex input patterns, the sync signals can be used to trigger external signal generators or waveshaping circuits, which then clock the network.

The instrumentation main frame also includes up to three digitally programmed power supplies that are shared by the test stations and can be operated independently. Each consists of a power supply and current or voltage trip-level detector. The program specifies voltage, sign, magnitude

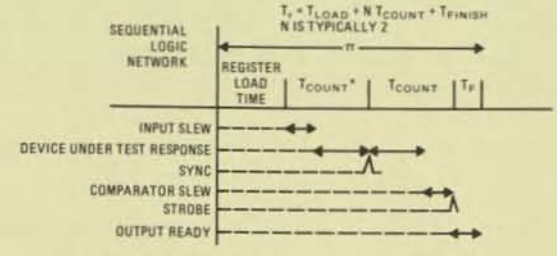


Figure 8

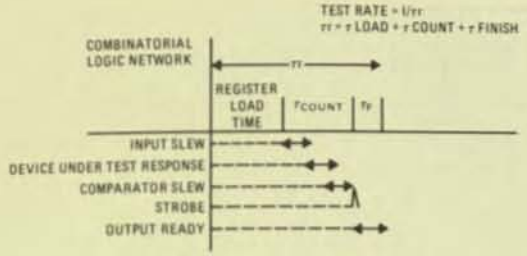


Figure 9A

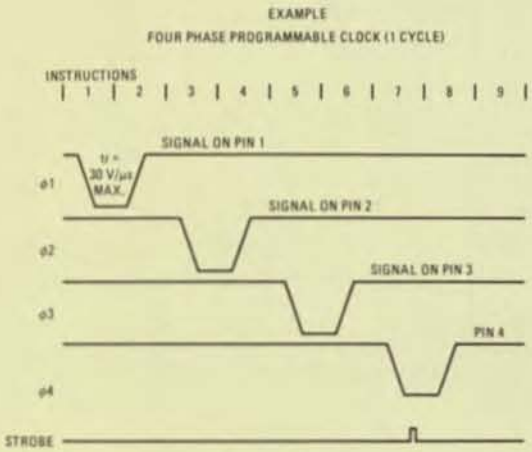


Figure 9B

```
0001          FORCE VF0 -25.0;
0002          FORCE E1 -20.0;
0003          FORCE E0 0.0;
0004          SET DELAY 2.5E-6;
0005          SET D 111100000010;
0006          ENABLE STROBE 0001;
0007 000001 SET F 10000101010,
0007 000002       01001010101,
0007 000003       00101110000,
0007 000004       00010011001;
0008          END;
*
```

Figure 9C

and current. With as many as five dual reference supplies also available, the system can satisfy a variety of functional test ranges—for example, MOS stress testing along with MOS and bipolar functional testing when the device being tested is a hybrid subsystem.

In addition, one register is available for control of wafer probes and other auxiliary equipments, and various utility components and displays. The multiplexer matrix, whose functions were shown in Figure 4, is also in the main frame.

TEST STATIONS

Each station is provided with up to 120 function drivers and sensors. These are located next to the test terminals to minimize capacitance. The drivers change signals monotonically at the test rate. Logic and reference levels are bused to the stations (see Table 2 and Figure 4).

Depending on the excitation bit transmitted by the F register, a driver input is gated to produce a voltage equal to either the "1" or "0" levels on a pair of buses from the digitally programmed supplies in the main frame. The comparator sensors are similarly gated to the reference supplies. Each responds with a logic level output that is gated with the M register bits.

Precision Measurement Unit

The precision measurement unit (PMU) contains a digitally programmed power supply with programmable current limit, a digitally programmed current supply with programmable voltage clamp, and an analog-to-digital converter programmable as a precision current or voltage detector. Either voltage-force/current-sense or current-force/voltage-sense measurements may be made. A software dual limit comparator may be programmed for go/no-go decisions on the A/D response.

Pin addresses, which operate the relay switching array of the PMU, are derived from an input/output register (D), address register (PA), and clock-address register (CA). The relays are placed as closely as possible to the pins to minimize stray capacitance.

Pin Control Applications

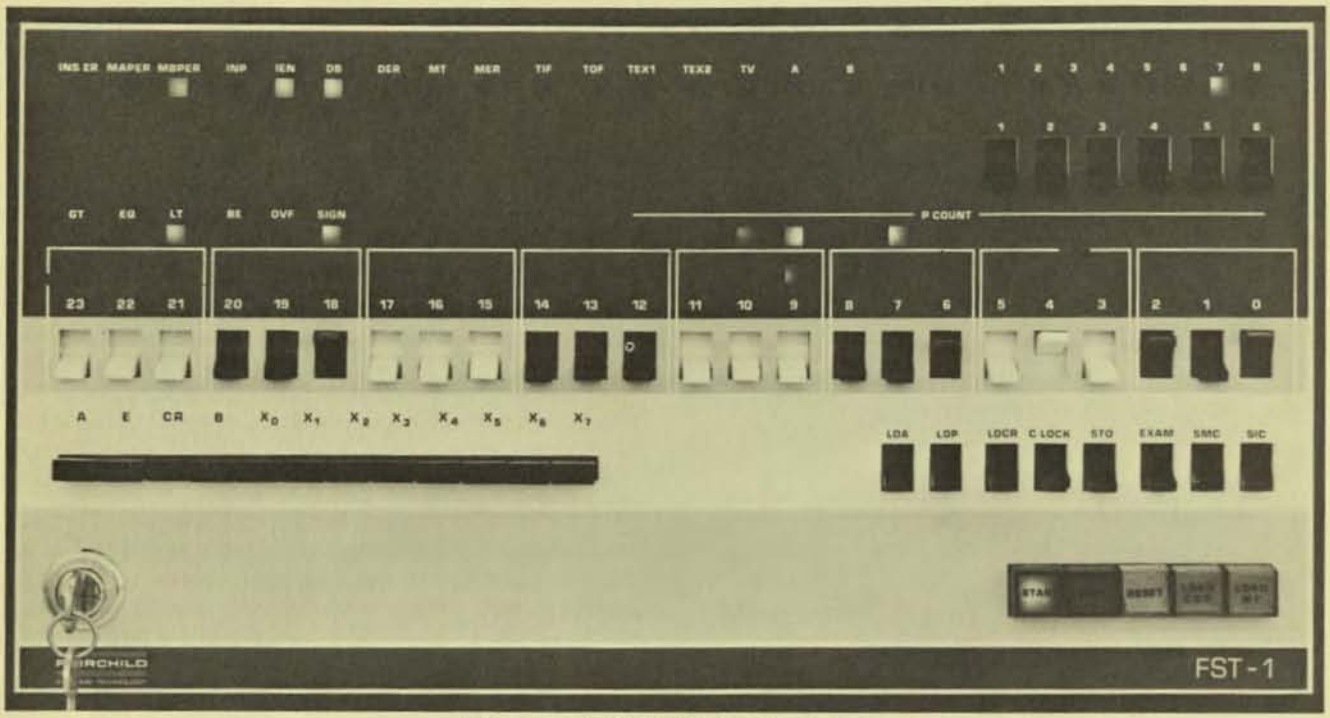
Output pins can be loaded in series with the driver. Then, when the driver is switched and the output is detected, concurrent go/no-go results are obtained. Alternatively, the pin is connected to a programmable supply via a utility relay so that load current is applied when the supply is switched to the appropriate level. Load boards are provided for these tests.

Device power supply pins can be decoupled with a capacitor in series with the utility relay. Output pins may be biased through load resistors to programmable supplies. When making a DC measurement, the load resistor may be disconnected by the utility relay.

CONTROL PANELS AND DISPLAYS

Controls and displays are provided for modifying and observing all of the principal test operations. The control groups are:

- Monitor control panel, used to perform the operations mentioned in the discussion of the monitor operating mode. The panel includes a digital voltmeter that can be connected to any internal programmable supply or to an external probe.
- Test station control panel, which includes lamp displays that indicate input-output logic states, register contents, go/no-go indications, etc. Conditions displayed are switch-selectable.
- FST-1 computer displays and controls, and the controls provided on the computer peripheral equipments.



FST-1 CONTROL PANEL AND DISPLAY

In addition to all of the controls and displays needed for housekeeping and testing, each of the test stations has ten binary lamp displays that the system user can define to suit his requirements.

SOFTWARE SYSTEMS

Three levels of software, which become more interpretive as they rise in authority, are employed. These are:

- FACTOR, The Fairchild Algorithmic Compiler, Tester-Oriented. The programmer uses the FACTOR program guide to write and compile statements such as those in Figures 9C and 10. The actual instruction words, as translated and compiled by FACTOR, follow 24-bit binary formats.
- Assembler and various other utility programs.
- DOPSY, the Disc Operating System, DOPSY components include the file-operating subsystems, the subroutine library, and a short bootstrap program to enter DOPSY into core. Once DOPSY is in core, it can be used to assemble complete test programs from the various instructions and subroutines.
- TOPSY, the Tester Operating System. This is the executive and the main operator/system interface. The example monitor-mode operations previously cited would be obtained by the user with TOPSY calls.

```
0001          WRITE (LP) 'THIS PROGRAM USES ALL TESTER STATEMENTS';
0002          SET DELAY 2.5E-6;
0003          SET DELAY 31.7E-3, DC;
0004          SET SI 3.5, RNG2;
0005          SET S0 0.7;
0006          SET CLOCK 255;
0007          SET PMU SENSE, AUTO;
0008          SET PMU FORCEI, RNG2;
0009          SET D 110 (32:0) (41) (31:1) 01;
0010          SET M (40:1) (8:0);
0011          SET S 11001010111100000001;
0012 000001 SET F 10001111000010110000011111000011111000001010100001,
0012 000002         1 (3:0) (4:1) (4:0) 1011 (5:0) (4:1) (4:0)
0012 000002            (5:1) (5:0) 10100001,
0012 000003         (47) 11,
0012 000004         0010 (18) (14:1) 01 (48) 0;
0013          SET R (34) 111;
0014          SET LOGIC NEG;
0015          ENABLE ILO LT 0.04;
0016          ENABLE IHI GT 0.09;
0017          ENABLE LATCHES;
0018          ENABLE COMPARATORS;
0019          ENABLE RELAY;
0020          DISABLE COMPARATORS;
0021          ENABLE DCT0 LT 21E-2;
0022          ENABLE DCT1 GT 0.7;
0023          FORCE E0 -2.5;
0024          DCL A/10/,B/20/;
0025          FORCE E1 (A+B)/3, RNG2;
0026          FORCE VF2 (B/A), RNG2;
0027          FORCE PMU (A*B)*10E-5, HOLD;
0028          FORCE STROBE;
0029          FORCE CLOCK;
0030          FORCE RESET;
0031          FORCE WAIT;
0032          FORCE DELAY;
0033          CPMU PIN 47;
0034          XPMU PIN;
0035          XCON VF2;
0036          MEASURE VALUE;
0037          MEASURE VALUE, LOG;
0038          MEASURE NODE 143;
0039          ON DCT, EXIT;
0040          EXIT: END;
*
```

Figure 10

TOPSY and Its Monitor

TOPSY executes the test programs in a highly interpretive mode. It requires little more than a word or two from the

authorized user to carry out a command. For example, an engineer might type in:

/.PAUSE ON STATEMENT 15.

The /. is a TOPSY identifier, and STATEMENT is a "noise" word that is ignored by the system. The user is permitted to add noise words so that the commands are easily understood by all personnel concerned.

TOPSY's monitor, as the name implies, keeps watch over the programs being run. If a subroutine is missing from a program, for instance, the monitor orders a search for it in the file and advises the user if TOPSY does not find it. The monitor may also be used to initialize programs, modify tester operating conditions, and so forth.

Users of the Sentry 400 will rarely be concerned with the internal machine language, which is FACTOR's responsibility. The use of English-language commands allows the system to be used more efficiently by engineers because they do not have to depend upon programmers to carry out changes in test procedures. TOPSY will automatically wait for the proper instrumentation delays in any sequence of events in a test program but will execute non-time dependent instructions in a sequence to minimize total test time.

Disc Operating System

DOPSY is also easy to use. After it is loaded into core, a user can select routines and assemble programs from stored instructions and the subroutine library. Then he can file away the programs for future use. DOPSY, too, tolerates a lot of "noise" words, like the lower-case words in the following request:

//CREATE a DATA file named 'SAMPL 1." record size is 15.

The subroutines, which the operator simply references in his calls, include binary-to-decimal and machine language-to-communications code conversions, and the various input-output routines for the peripherals.

FACTOR

FACTOR, of course, demands precise statements. But the programmer is given little chance to go wrong. Actually, the language can be learned quickly by most technical personnel. FACTOR will inform the programmer of errors in syntax, entry of overlong statements, etc.

The compiler is one of the DOPSY overlay programs. On recoverable errors, FACTOR will continue to compile. If the number is not recoverable, the programmer will be put back on DOPSY and notified of that. DOPSY's monitor operates here, and also notifies the test system user when a compiled program enters the working store so that he can execute the program with TOPSY.

FACTOR accommodates: numbers as integers, decimal fractions and exponentials; handles Boolean, scalar (non-Boolean) and mixed variables; arrays (ordered series of variables); parametered calls; and a wide variety of other functions.

To avoid endless rewriting of long, but somewhat repetitive, programs, and to conserve space in the core memory, "blocks" and "global variables" may be used. Blocks are simply subroutines that can be nested like so:

```
BLOCK (a)
   BLOCK (b)
   END (b)
   BLOCK (c)
      BLOCK (d)
      END (d)
   END (c)
END (a)
```

Any number of subroutines can be placed in up to eight nesting levels, and subroutines can be repeated as often as desired. The global variables are quantities accessible to all blocks.

Various statements such as IF, THEN, GOTO, and so on, may be used to mix and match sequences of instructions and branches, in response to test results. For instance, IF an element fails a critical test, GOTO an analysis routine to find out why, and THEN put the element into the reject bin.

Fairchild Systems Technology
Division Headquarters
974 East Arques Avenue
Sunnyvale, California 94086
(408) 735-5011
TWX: 910-339-9217

Fairchild Systems Technology
Regional Sales Office
621 Hawaii Street
El Segundo, California 90245
(213) 678-3166
TWX: 910-325-6607

Fairchild Systems Technology
3935 Glenhaven
Garland, Texas 75040
(214) 272-6687

Fairchild Systems Technology
Regional Sales Office
1020C North King's Highway
Cherry Hill, New Jersey 08034
(609) 667-0241
TWX: 710-892-2566

Fairchild Systems Technology
London Sales Office
Grove House, 551 London Road
Isleworth, Middlesex, England
TEL: 560-0838
TELEX: 24693

Fairchild Systems Technology
Munich Sales Office
Truderingerstrasse 13
8 Munich 80
West Germany
TEL: 45-84-16

Fairchild Systems Technology
National Sales Office
974 East Arques Avenue
Sunnyvale, California 94086
(408) 735-5486
TWX: 910-339-9217

Fairchild Systems Technology
Regional Sales Office
2434 Dempster Street
Des Plaines, Illinois
(302) 299-1048
TWX: 312-299-8137

Fairchild Systems Technology
Regional Sales Office
3440 N.E. 12th Avenue, Room 2
Ft. Lauderdale, Florida 33308
(305) 564-0546
TWX: 510-944-9808

Fairchild Systems Technology
Regional Sales Office
87 Terrace Hall Avenue
Burlington, Massachusetts 01803
(617) 272-7060

Tokyo Electron Labs
1-Higashikata-Machi
Kohoku-ku, Yokohama
Kanagawa, Japan 226
TEL: 045-471-8321
TELEX: YH7753

FAIRCHILD
SYSTEMS TECHNOLOGY

TECH TALK

FAIRCHILD SYSTEMS TECHNOLOGY EMPLOYEES NEWSPAPER

Rec Council Plans Spring Dance

SPRING is in the air and plans are being made for the Annual FST Spring Dance to be held at the Sunnyview Club on April 18. Details include a spaghetti dinner, Bingo, and dancing to George Barry's 5 piece band. Dress will be casual. Watch for posters with full details!

Rec Council Schedule for the coming year includes:

Spring Dance	– April 18
Picnic	– June 6
Fall Dance	– October 24
Children's Christmas Party	– December 5
Christmas Dance	– December 12

Be sure to mark your calendars so you don't miss out on these fun-filled events!

George W. Leisz Named as a Vice President

George W. Leisz, former Executive Vice President of North American Rockwell's Autonetics division, was recently elected a vice president of Fairchild Camera and Instrument by the Board of Directors of the corporation.

Alan J. Grant, group vice president, said that Mr. Leisz will be in charge of a newly formed group which will include the Systems Technology and Controls divisions of the company. Mr. Grant, to whom Mr. Leisz will report, announced that the formation of the Systems and Controls group is being made at this time to accelerate Fairchild's corporate objective of expanding its position in the industrial and commercial equipment markets. He further emphasized that Fairchild's technological leadership in semiconductor devices will serve as a basis for introducing advanced industrial control and data systems into a world-wide expanding market.

At North American Rockwell, Mr. Leisz's responsibilities included the direction of its three divisions, Computer and Data Systems, Navigation Systems and Electro Sensor Systems. During his 18 years at Autonetics, Mr. Leisz served in various capacities which included the direction of the design and production of advanced computers, automatic test systems and precision sensing equipment. He previously was affiliated with Sylvania Electric Products, Inc. and Hoffman Radio Corporation.

People in New Places

Chuck Lavarnway of purchasing turned Friday the 13th into a lucky day by receiving his promotion to the position of Buyer. Chuck has been with Fairchild since September, 1969.

The Personnel Department welcomes their new Employment Manager, **Jay Waste**. Jay will be handling all professional and technical recruiting for the division. He comes to Fairchild Systems Technology with many years of experience in the recruiting field, most recently working with Watkins-Johnson as Senior Personnel Administrator.

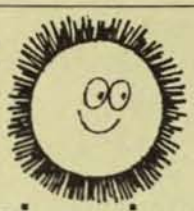
Dick Bodenschatz was promoted in January to head the inspection area of PC Board Manufacturing. He joined Fairchild in September, 1969.

Mechanical Systems welcomes **Lou Thayer** to head the Automation Products Department. Lou comes to FST from Hughes Aircraft in Oceanside, California, where he was Product Line Manager of Displays. He will be in charge of the Product Design effort for the development of peripheral handlers for Semiconductor as well as environmental and ambient automatic test handlers to support the FST line of electronic test equipment.

Walter Allen has moved from the PC Board area to Production Engineering to assume his new position as Assistant Manufacturing Engineer. Walter joined Fairchild in April, 1968.

Carl Steffens has recently been appointed Group Director of Marketing. Carl was Director of General Sales and Acting Marketing Group Director prior to his new appointment. He will oversee the Marketing activities which ininclude Customer Engineering, Product Marketing and General Sales Directorates.

Department Spotlight



Systems Engineering

Our imaginary product in idea form is ready to be developed and engineered into a product. At this point the product can take one of three paths, depending on whether it is a computer controlled test system, a mechanical system or a data system. Let's look first at the Systems Engineering directorate and test systems. The other areas, Data Systems and Mechanical Systems, will be covered in future issues.

Systems Engineering is headed by **Vito DiMucci**, Director, and consists of five operating departments and one support department: including, Advanced Development, Functional Test Systems Engineering, Component Test Systems, Measurement and Control, Electronic Sub Systems and Engineering Administration and Services. Systems Engineering plays a major role in developing and specifying all of the assemblies and sub-assemblies in the complete system. It is interesting to note that some of the major assemblies specified are products of the other engineering directorates such as computers from Data Systems Engineering and mechanical handlers from Mechanical Systems Engineering.

One of the largest of the product development operating departments is Functional Test Systems Engineering where, among other products the "Sentry 400" Test System is under development. The "Sentry 400" will make its debut to the public at the forthcoming IEEE Show to be held this March 23-27 at the New York Coliseum. **Bob Huston**, Program Manager for the "Sentry 400" and Section Manager of the Array Test Systems Section within FTS Engineering, along with many other project personnel, have literally been working night and day to complete the "Sentry 400" design and debug phase. Also within FTS Engineering, **Brian Marchant**, Section Manager of FTS Software and his crew have been working at breakneck speed developing the new 5000C Executive Program so that it will be operational in time for the show.

Another of the large product development operating departments is Component Test Systems Engineering where another new product line, the 700 Series Testers, developed and engineered by CTS, will be making its debut to the public at the IEEE Show. A great deal of the responsibility for the development of the 700 series rests with **Ken Rinaldo**, Program Manager for the 700T Transistor Test System and Systems Engineering Section Manager. The 700T is the particular tester that will be shown at the IEEE Show this year. Other models of the 700 Series will follow. Other new products to be at the show will be the 6300A Op Amp analyzer, which will grace the hospitality suite, and the 600C Tester which will be shown in the main display area. Both of these new products were developed by CTS Engineering.

The Advanced Development Department within Systems Engineering, managed by **Harold Vitale**, has the prime responsibility for proving the theoretical and practical feasibility of various product ideas. To do so, Advance Development often must push the state-of-the-art forward to bring the product idea to the stage where it can be engineered.

The Measurement and Control Engineering Department is managed by **Dick Rice**. Dick and his crew in M&C are involved in the design of "front end" boxes for system applications and will have their first instrument, a 15 Bit Converter, ready for production in the second quarter, 1970. This is the first of many M&C products which will increase the percent of "in-house build" modules for our present systems. In addition, other products are in the preliminary stages of development.

Included in the project personnel who have been giving their all to get these products ready, are members of another Systems Engineering department, Engineering Administration and Services, managed by **Burton Hirsch**. EAS consists of four engineering support sections: P.C. Board Design and Drafting, the Engineering Information center where all changes are recorded and controlled; the Custom Product Shop which has done a fantastic job in building the IEEE show machines; and Administration Services, which monitors and controls the project and departmental budgets and schedules.

In all, Systems Engineering is the focal point for total test system design, large and small, computer controlled or otherwise, to develop, engineer and document the product for release to Manufacturing where it will be built and subsequently shipped to the customer. As indicated above, the job cannot be done by any one department, but is the result of a team of departments all working toward the common objective of offering our customers a highly reliable product of which all of us at Systems Technology can be proud.

Vito DiMucci, Director, Systems Engineering.

Bob Huston, (second from right) Program Manager for the "Sentry 400" and Section Manager of the Array Test Systems Section, and his crew (left to right) George Niu, Tony Beccia, and Carlo Silva.

Primarily responsible for the 700 series is the Component Test Systems Engineering group – (left ro right) Dave Crosby, Ken Rinaldo, Program Manager for the 700T Transistor Test System, Bill Calkins, Jerry Pillsbury, George Baxley, Vince Schommer and Bill Ragin.

Brian Marchant, (right) Section Manager of FST Software and the crew who developed the 5000C Executive Program for the IEEE Show – (left to right) Frank Evenson, Ron Parker, Roger Derin.

Bits and Pieces

There was something fishy going on around **Dick Ribas'** office on February 24 when the people in his area helped celebrate his Pisces birthday with an office full of decorations. 21st Dick?

There's something going on around **Mickie McNally's** desk lately too. Every time you pass her, it seems she has another beautiful bouquet of flowers on her desk. We inquired and it seems her secret admirer is none other than her thoughtful husband, Richard.

Celebrating their 43rd anniversary on January 14 were **Doc** and **Bertha Douglas.** Doc is a Senior Design Engineer in the Automation Production group of Mechanical Systems. He describes his 43 years of marriage as "eventful" and rightfully so with a proud total of five children ranging from vice president at Libby, McNeill & Libby to a youngest son in Viet Nam. They have six grandchildren.

Wedding bells for three FST employees – **Louise Hendrix**, Distaffer in the Metal Shop, changed her name to McBrayer on February 14. The couple is residing in San Jose.

Bert Graeve, Technical Staff Member in Systems Engineering Advanced Development, took the hand of the former Gudrun Weber on February 7 at the Los Altos Lutheran Church. They took their honeymoon trip to Napa Valley.

Mimi Hill became the bride of Robert K. Bowers on January 31. The ceremony was held at the Calvin Presbyterian Church with a champagne reception at the Cabana in Palo Alto. The newlyweds took a short trip down the coast for their honeymoon. Mrs. Bowers works in Cabling.

The Metal shop wishes a speedy recovery to fellow worker **Leo Chapman** (Metals Q.A.) who is in the Stanford Medical Center.

Sports

For you bowling fans, the Fairchild Tuesday Night Mixed Fives League officially closed out the first half of play on the 16th of December. The #1 team was "Two Pair and a Spare" with a 37.5/22.5 win/loss record. The members of this fine group are **Kandy & Velvet Sanchez, Clay & Earline (Sam) Bisson** and **Garry Rae.**

In the individual trophy standings:
J. Bernhardt (Mens Hi Series – 638)
R. Chapman (Mens Hi Game – 226)
B. Sazian (Mens Hdcp Series – 680)
B. Ahrendt (Mens Hdcp Game – 256)

For the Distaffers:
J. Hart (Women Hi Series – 553)
K. Berendsen (W/Hi Game – 224)
S. Fredrickson (W/Hdcp Series – 280)
N. Takemura (W/Hdcp Game – 258)

The Fairchild Summer League is now forming and will be mixed pairs. For more information on a full summer of bowling fun, contact **Fran Humphrey** in the Metal Shop. He'll be happy to help you enter your team, or place you on one.

For the more daring sports fan, a new Fairchild sky diving club has been formed. For more information, contact **Bob Gray** on extension 5215.

FST Welcome Mat

MANUFACTURING
Reza Alaneih
Garry Batterman
Jill Correa
Phillip Green
Pamela Klier
Georgiann Pidcock
Bob Richter

SYSTEMS ENGINEERING
Harold Brown
May Moore
Daniel Oakes

MARKETING
John Boundy
Richard Brouillard
George LaRose
Cliff Travis

DATA SYSTEMS
Marv Ackerman
John Burnett

ACCOUNTING
Rod Trainer

PERSONNEL
Jay Waste

On The Line

February certainly seems to have been a productive month for the line people, off the line. **Chatta Morrison**, Chassis Wirer on **Don Dunkles** line has just returned to work after adding a bouncing 6 lb. boy, Todd, to her family. Todd is Chatta's third child.

Lou Guevara's wife presented him with their first child, Louis, on February 19. Lou is a Production Planner on the Sandia Project.

Another proud father, **Frank Ambrosini**, welcomed a baby girl to his family. Frank's wife gave birth to 7 lb., 7 oz. Antionette Theresa, on February 21. Frank is a Material Handler for the Stockroom.

A few more celebrations were in order for three Cabling girls with February birthdays – **Helen Foreman, Mary Jo Humphrey, Barbara Fey.**

Poor "long-suffering" **John Javelet**, Production Planner, seems to be smiling more since another male has been added to the Pilot Line. The new Tech on the line, **Floyd Kling**, drives all the way from Richmond every day to make the odds more even with three men now against twenty girls.

Sally O'Brien of Pilot isn't really out of shape nor is her color normally purple, but due to a fractured rib, she is having a hard time moving around lately. To laugh is sheer torture, and of course we all try not to make her laugh.

Having survived four months on his new job as Foreman of twenty women on the Pilot Line, **Martin Johnson's** favorite comment seems to be, "Why me?". Of course the girls can't understand it because they are most cooperative, never dispute his word or try to change his ideas – well, hardly ever.

An Easter Message

"One Solitary Life"

He was born in an obscure village, the child of a peasant woman. He grew up in still another village, where he worked in a carpenter shop until he was 30. Then for 3 years he was an itinerate preacher. He never wrote a book. He never held an office. He never had a family or owned a house. He didn't go to college. He never visited a big city. He never traveled 200 miles from the place where he was born. He did none of the things one usually associates with greatness. He had no credentials but himself. He was only 33 when the tide of public opinion turned against him. His friends ran off. He was turned over to his enemies and sent through the mockery of a trial. He was nailed to a cross between two thieves. While he was dying the executioners gambled for his clothing, the only property he had on earth. When he was dead, he was laid in a borrowed grave through the pity of a friend.

Nineteen centuries have come and gone, and today he is the central figure of the human race and leader of mankind's progress. All the armies that ever marched, all the navies that ever sailed, all the parliments that ever sat, all the kings that ever reigned, put together, have not affected the life of men on this earth as much as that One Solitary Life.

Author unknown

Medical Services News

ATTENTION MEDICAL PATIENTS: CLAIMS FOR 1969

Those of you who have insurance claims pending from 1969, and have neither heard nor inquired about your claim, please do so immediately. United States Life, the former insurance carrier, is exercising its right to deny claims if all forms and bills have not yet been submitted. Contact Medical Services on 5122 to learn the status of your claim.

SPRING IS HERE

Baseball, picnics, volleyball, swimming and just good old outdoor exercise are all in the fun of Spring. But don't let the sunshine and warm days make you forget to be careful. Spring is the time for outdoor injuries, sprained ankles and pulled muscles. Be certain you won't have to sit out Spring on the sidelines this year.

"Moving Up"

Yes, even our Stores Operations are moving up into space – the unused overhead space in their warehouse. **Jim Cooper**, Stores Manager, has had his crew busy for two weeks installing a new pallet rack system designed to utilize the available height in the building. The improvements will increase storage space to three times the present capacity. In addition, a parts location and identification system will facilitate the flow of material to and from the Stores area.

The Stores warehouse is located to the right rear of our main building.

Before rearranging, Jim Cooper surveys the boxes of material stored on the floor of the main Stores area.

After rearranging, the materials rise to their designated heights in the warehouse.

Responsible for the stores transformation are: (Left to right) Frank Ambrosini, Tony Guarascio, Don Wheatley, Gene Alquist and Jim Cooper.

Service Awards

Celebrating 5-year awards this month:

Glen Harbeck receives congratulations and his service award from Supervisor, Stu McClelland. The celebration was held on February 2 with cake and coffee enjoyed by fellow workers. Glen works in Metal Fabrication.

Slicing into her tempting celebration cake is Wanda Ross, Chassis Wirer on Pilot Line. Foreman Martin Johnson presented Wanda with her service award. Wanda joined us in the assembly operation in January, 1965.

Nat Watchman, Electronic Technician in Product Test celebrated his 5 years on February 11. Nat is being congratulated by Supervisor Bill Herman.

TECH TALK

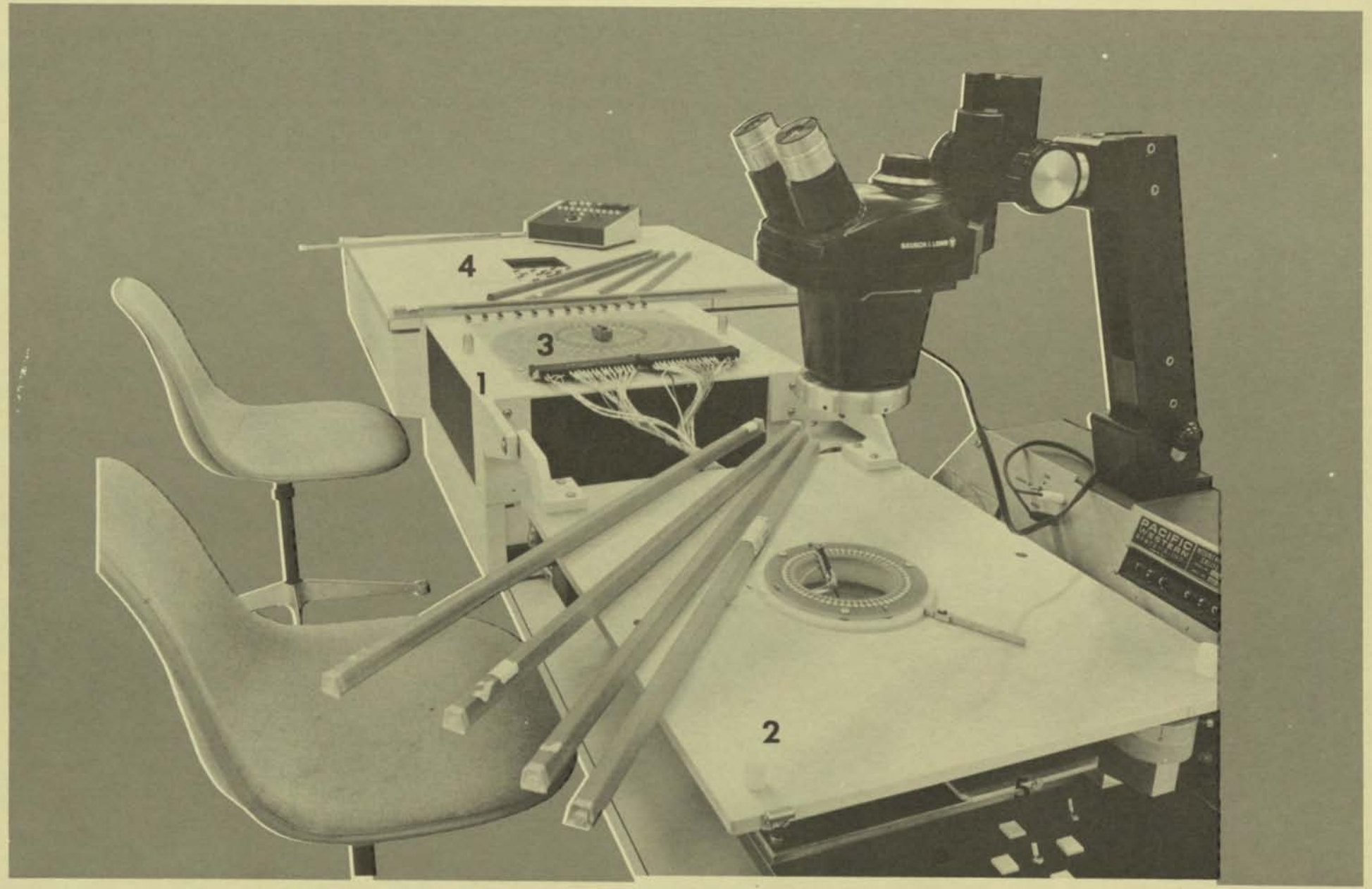
March 1970

Published by and for the employees of Fairchild Systems Technology Division in Sunnyvale, California

Editor: Carol Leighton

Photographers:
Pete Guckenheimer and Tim Russ

Reporters: Wes Bell, Gerri Bentley, John Botek, Darlene Harbeck, Mimi Hill, Ken Karraker, Larry Lawrence, Tim Russ, John Schuler and Ruth Zabel.

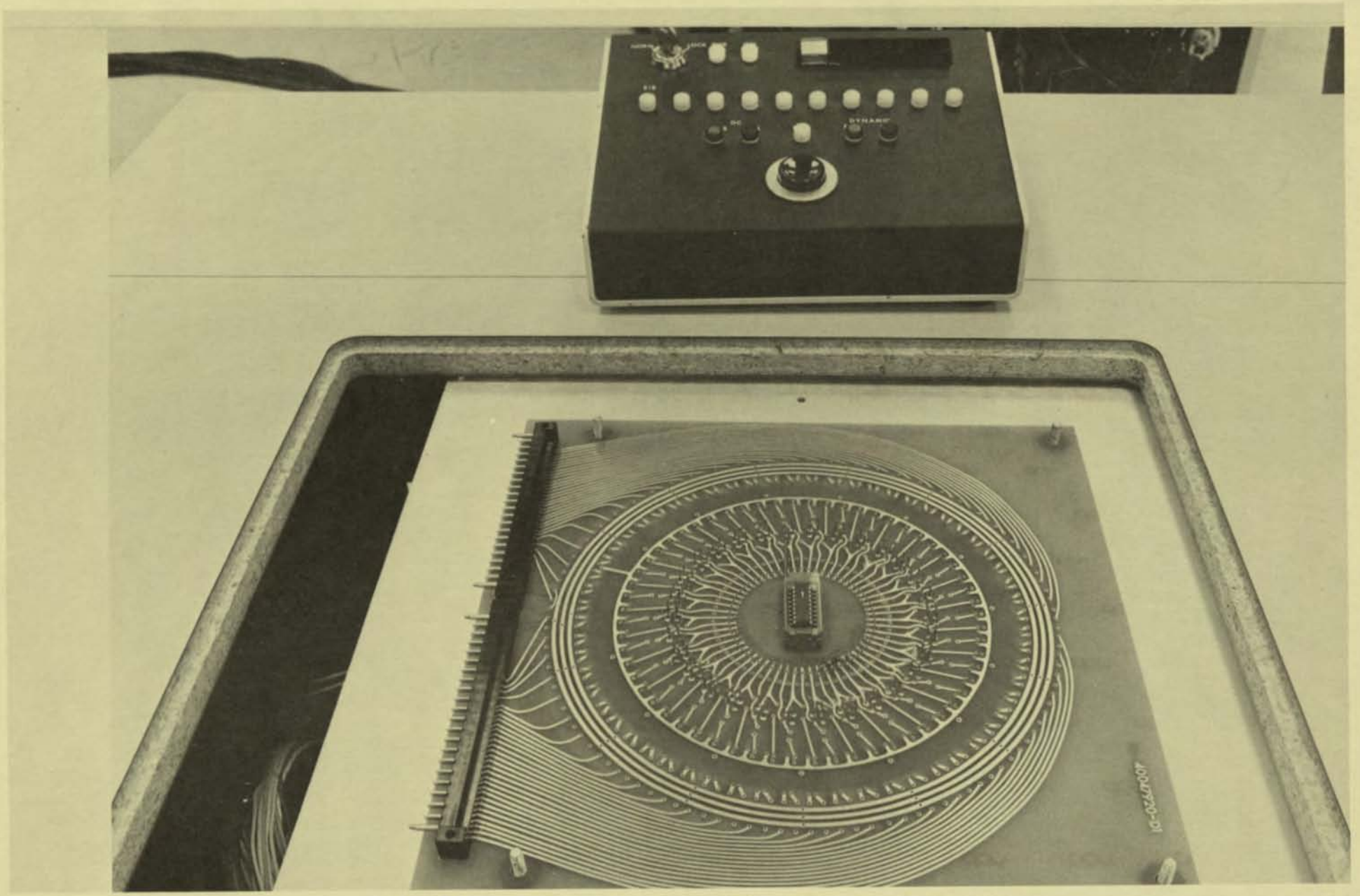


TEST HEAD ON WAFER PROBER PROVIDES PRODUCTION VERSATILITY AND OPERATING CONVENIENCE

FAIRCHILD
SYSTEMS TECHNOLOGY

Production versatility and line balance is achieved when standard test head (1) mounted on wafer prober (2) is hinged open to allow "final" testing of packaged devices (3). Thus, wafer probe station doubles as a "manual" test station (4). During wafer probe operations device socket (3) is replaced with probe interface ring, test head is secured over prober, and extended chuck (5) allows fast wafer change.

P-006-11/71

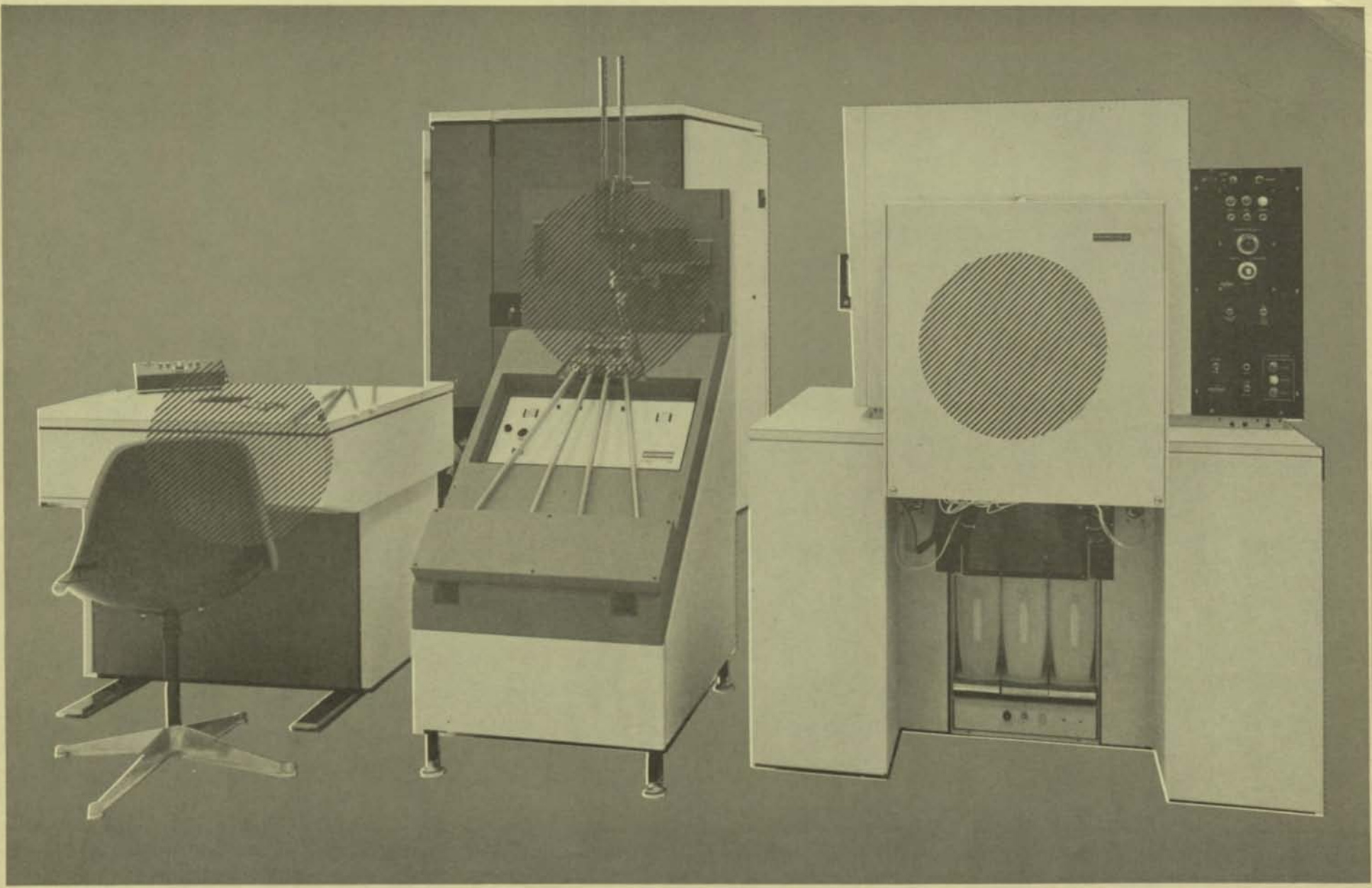


HIGH SPEED TEST HEAD DESIGN ELIMINATES SPECIAL HARDWARE REQUIREMENTS

FAIRCHILD
SYSTEMS TECHNOLOGY

Here's the 1103-1 under test! Test head pin electronics are positional radially beneath the socket/load board shown here. Just one viewing resistor on load board is required to test this 1024 x 1 Random Access Memory. Unique system design eliminates error prone, time consuming hardware twiddling, decision making, and cumbersome personality or pin swap boards. Connector on left controls other loads, if required.

P-004-11/71

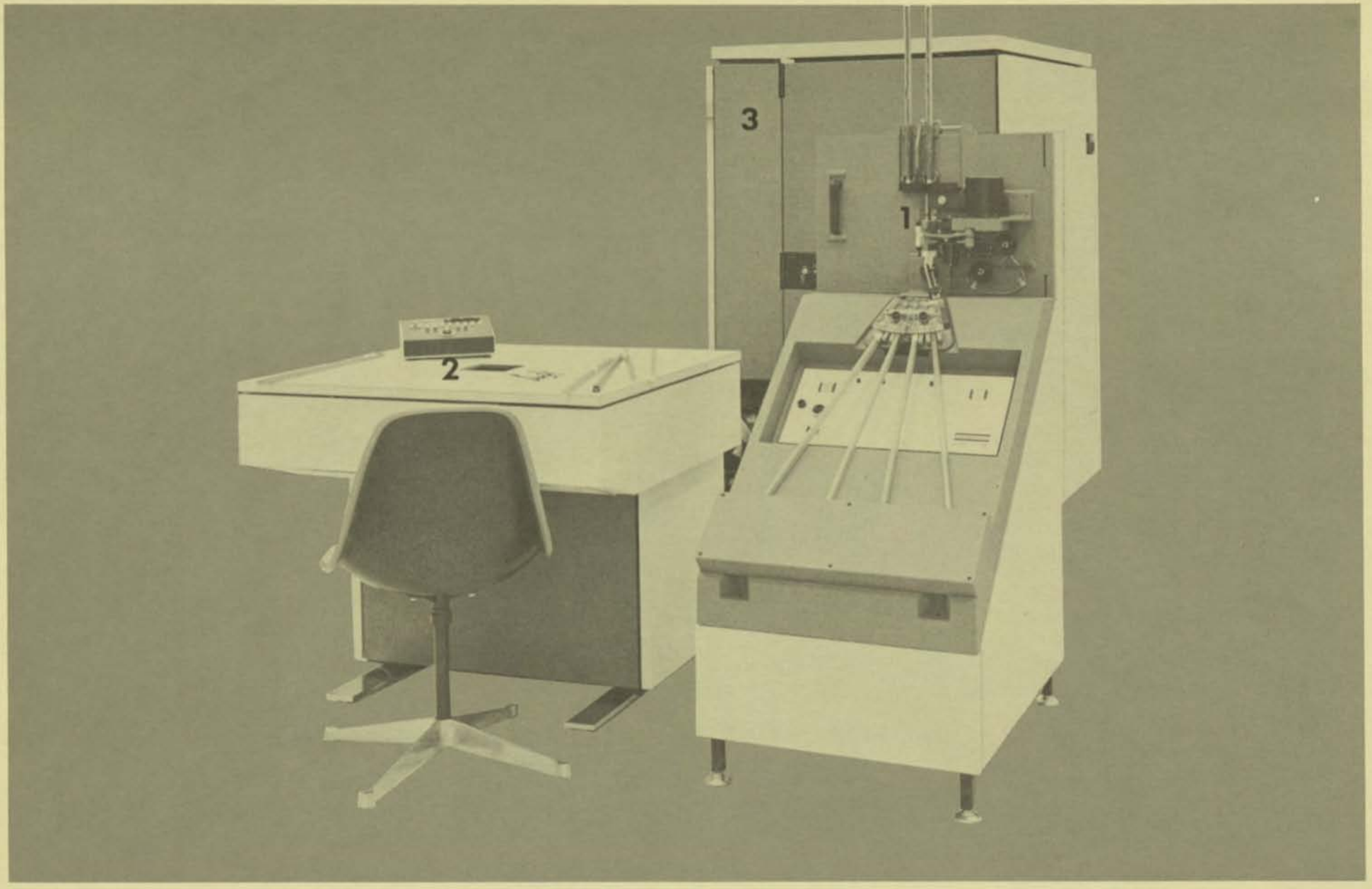


UNIQUE TEST HEAD PROVIDES CORRELATION AT ALL TEST STATIONS

FAIRCHILD
SYSTEMS TECHNOLOGY

Testing correlation is assured when identical test heads (see dots) provide the same high quality electrical environment for complete DC and 5MHz function testing of multiphase MOS and bipolar devices at all test stations - manual insertion, auto handler, and temperature chamber. For complete versatility, test head on any equipment hinges open for direct access to device adapter/load board and to accommodate hand testing.

P-008-11/71

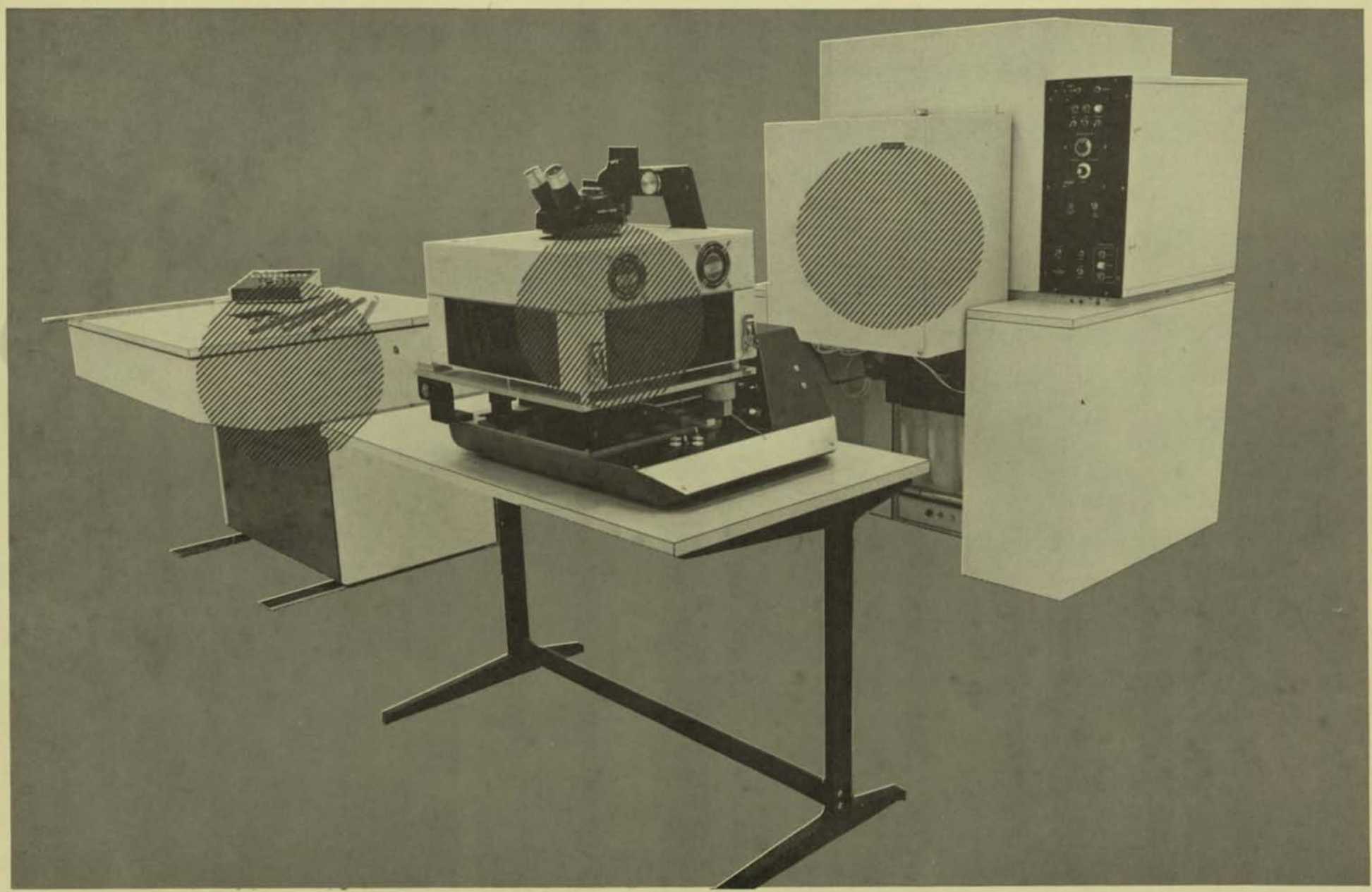


TEST HEAD ON AUTO HANDLER INCREASES THROUGHPUT WITHOUT DEGRADING TESTING

FAIRCHILD
SYSTEMS TECHNOLOGY

Compact test head mounted behind auto handler contactor (1) provides same high quality electrical environment as test head mounted in manual test station (2). Both are supported from the High Speed Test Station Controller (3) on a time shared multiplex basis. SENTRY Mainframe (not shown) provides efficient system architecture to support high throughput testing of different devices at up to four test stations.

P-007-11/71

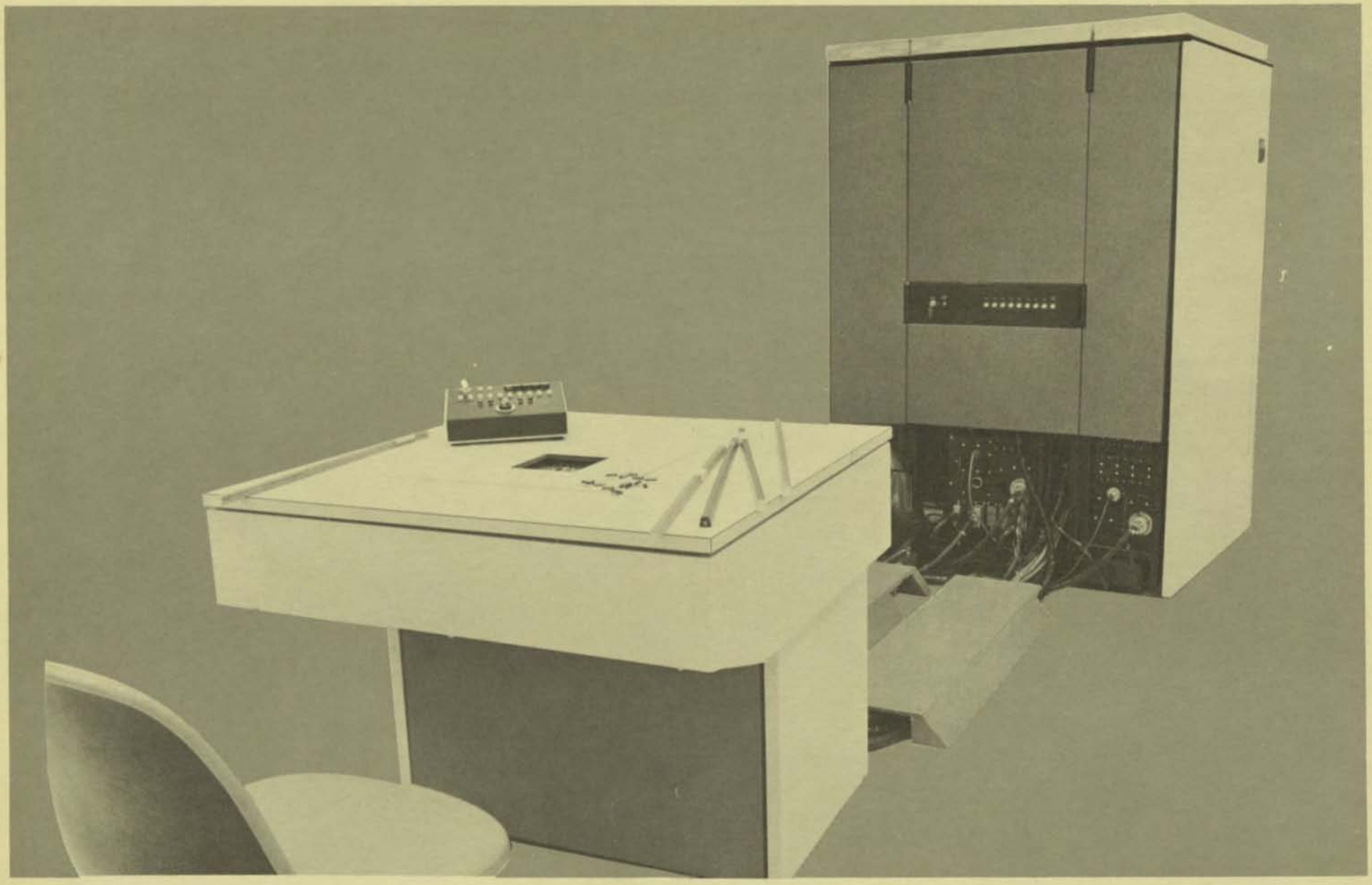


UNIFORM 5 MHz TESTING AT ALL STATIONS ASSURES CORRELATION AND LOWER COSTS

FAIRCHILD
SYSTEMS TECHNOLOGY

Testing correlation is assured when identical test heads (at each (dot)) provide the same electrical environment for complete DC and 5 MHz function testing of LSI at both wafer probe and final test. Identical test head at environmental chamber assures correlation for both production and Q.A. Costs are reduced when complete testing at wafer level screens out bad chips before packaging materials and labor are committed.

P-005-11/71

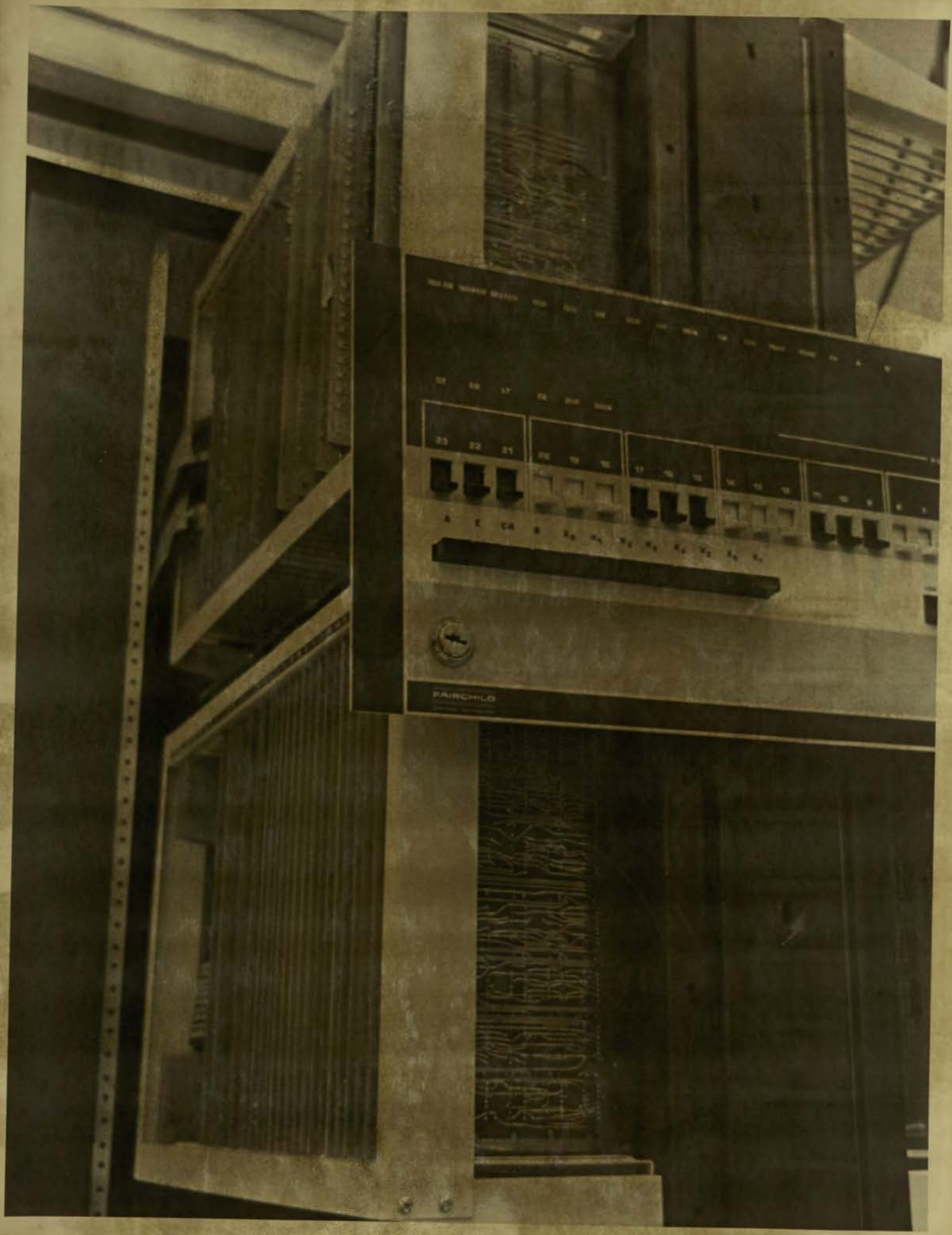


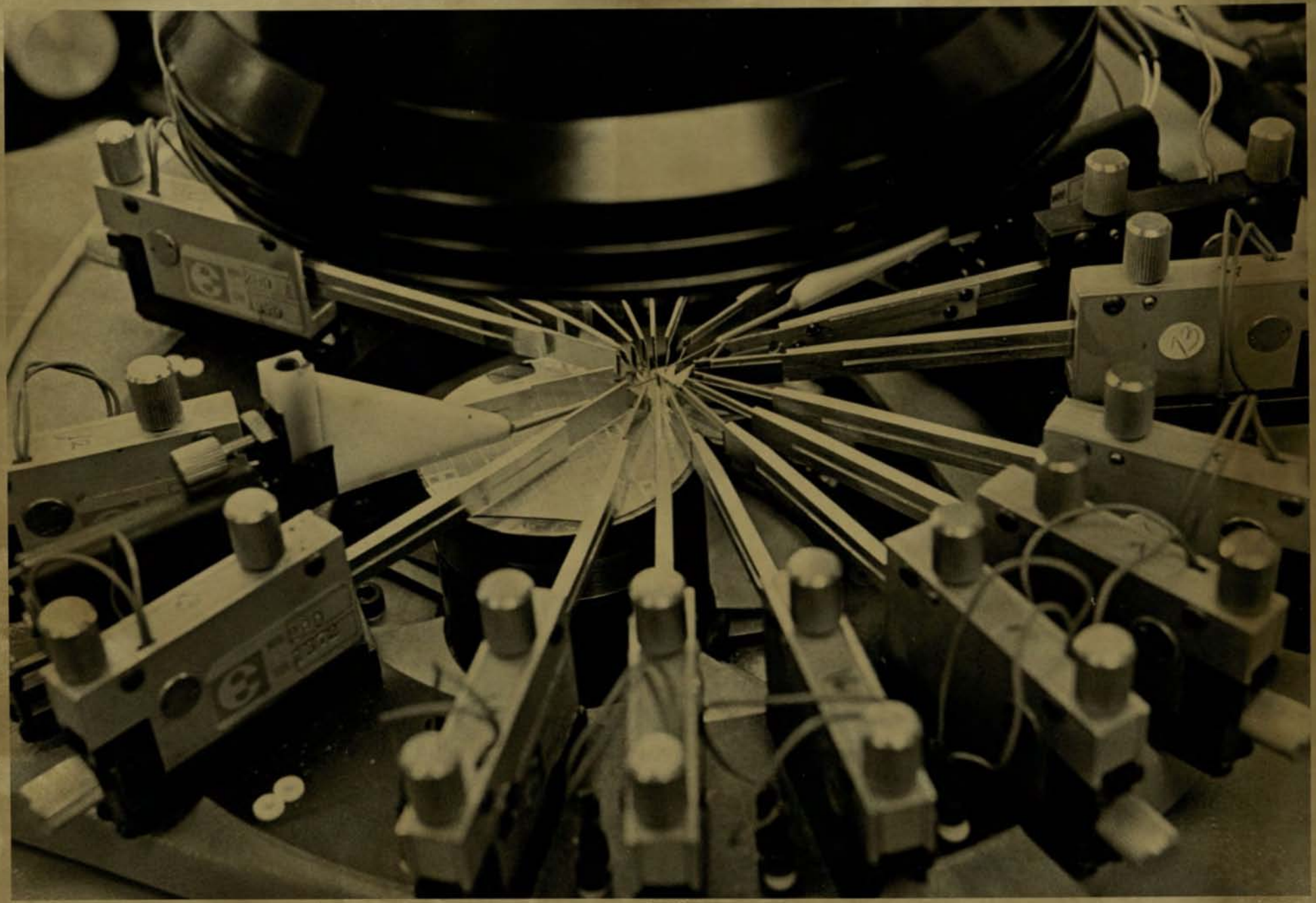
5 MHz TEST STATION CONTINUES SENTRY'S MODULAR DESIGN

FAIRCHILD
SYSTEMS TECHNOLOGY

Basic high speed test group (shown above) added to SENTRY mainframe group provides up to 5 MHz function testing plus complete DC testing of all LSI devices. High speed test station controller (on right) supports test station (on left). Modular system design allows each controller to support up to four test stations - each testing different device types and technologies with up to 60 pins - all under software control.

P-002-11/71


FAIRCHILD



Robe ring

Mrs. Nancy L. Huston
5819 Vargas Ct.
San Jose CA 95120-1736

tech talk

Published for the Employees of the Systems Technology Division of Fairchild

June 1975

A lesson in monster management

How do you begin when your assignment is to tackle a monster?

The first order of business is to get organized. Set priorities and break the apparently impossible task into manageable segments. Then get to work.

Organization is the overriding impression in the office of Jerry Crosby as he confronts his organizational monster. Jerry recently returned to the Systems Technology Division as marketing manager for small testers, a newly-created post that as closely resembles monster wrestling as any other task in industry.

To begin with, it's a job without end. The demands for Qual-card* programs to respond to user's specific applications arrive via phone and mail in ever-growing waves. Jerry leafs through the newest listing of Qual-card offerings published in a multi-page catalog that is updated monthly, satisfied that the Division is making progress in developing its Qual-card library. Yet, that satisfaction is short-lived. He refers to the five-foot list of Qual-cards in progress that covers a major section of the wall in his office and contains reports on the status of each. New additions to that list are made weekly.

"The library of Qual-cards will largely control the sales of our Qualifier* 901," Jerry says. "We have to be able to offer customers all of the standard programs they will use in their applications, plus continually add programs to our offerings in order to enhance the value of the Qualifier.

The Qual-card library and the calls it generates from sales representatives and customers is only one of the tasks that demand Jerry's attention as he structures an organization tailored to the special needs of the market for under-$30,000 semiconductor test systems. He, along with the entire Division, is working in an area that is relatively new to the Division. Reaching the vast market for these relatively low-cost testers requires a sales organization that can economically devote the time necessary in getting to know and calling upon the numerous users of semiconductor devices who would have application for the attributes of the Qualifier 901 and the PATT line of testers.

Today, Systems Technology has contracts with some 15 manufacturers' representatives across the United States to

(continued page 5)

Jerry Crosby

*TM-FCIC

Jim Bowen elected vice president

Jim Bowen

The election of Jim Bowen and George Wells as vice presidents of Fairchild was announced on June 4 by Wilf Corrigan, Fairchild president.

Mr. Bowen is general manager of the System Technology Division. Mr. Wells is general manager of the Discrete Products Group, which includes the Diode and Transistor Divisions.

Systems inventors receive awards

Y.B. Chau and Brooks Cowart recently received patent awards for inventions they developed as part of their work with Systems Technology. Y.B. received his award as co-inventor of an improved testing circuit. Brooks' award was for a parametric tester for input levels of semiconductor devices.

To be eligible for a cash patent award of up to $200, the inventor must file a description of the idea or device with the corporate patent office in Mountain View. An evaluation of the disclosure will be made, and if it is eligible as an original idea or device for patent under U.S. Patent Office rules, the inventor will receive an award at the time the application is made for patent.

Notes from Jim Bowen

This should be the year that Systems Technology makes significant inroads into test systems markets in Europe. Our efforts have been intensified to encourage customers in this part of the world to include Fairchild products on their shopping list when they are looking for a semiconductor test system. Marketing activity in Europe has been greatly accelerated with the result that we are receiving an increasing number of inquiries from potential customers on the Continent.

- - - -

Even though Japan has suffered an economic downturn that has been more severe and prolonged than that which we have realized in the United States, we have not allowed the slowing of orders to relax our attitude toward this potentially exciting market for our products. We recently hosted a large group of Japanese IEEE members, most of whom represent companies which are prospective customers for our systems. Al Perry escorted the Japanese visitors on a tour of manufacturing and engineering areas and provided the engineers with a detailed description of the capabilities of our products.

- - - -

I am encouraged to learn from Gordon Daggy that the number of articles and papers being prepared for publication and presentation is on the increase. I believe that this is one of the most beneficial methods for bringing Systems Technology's capability to the attention of our customers. Articles on systems design and test programming which appear in major trade publications, carry more credibility than we could ever hope to gain through an advertisement in the same publications. We know that we are the best in the business, but making the rest of the world aware of this fact takes special effort. We recently doubled the author's incentive award to a maximum of $400. If that alone doesn't give you encourgement to put your ideas down on paper to share with others, by-lined articles in respected journals bring professional prestige. Just ask those engineers and scientists who have become recognized as experts in their field because they have made the effort to document their developments and ideas for publication. Gordon's office is eager to lend support in preparing material for publication or presentation.

- - - -

The signs of our gradual recovery to former activity levels is most evident in manufacturing where we are seeing an increase in our work force for the first time in many months. We are proceeding with cautious optimism, believing that we have seen the bottom of the recession.

- - - -

My family and I plan to spend most of the day at the FST picnic at Blackberry Farms on June 14. Hope to see everyone there.

--Jim Bowen

Turning trash into treasures--The Recreation Council found a fortune on the way to the trash bin. Starting a paper recyling program little over a month ago, the Rec Council treasury has been growing gradually as a result of the income from the sale of recyclable data processing print-outs and punched cards. Regular contributors to the program, such as Nancy Ramirez (above), have been responsible for contributing almost a ton of the paper and cards each week. Income from the recycling program will be used to underwrite a major employee social activity. Others who are hoarding computer paper and cards that they would like to contribute to the recycling program, can bring them to the collection area near the receiving dock in the rear of the building.

Prizes for photos

Awaken your imagination, get out the camera and capture a winner in the annual HORIZONS photo contest. Nine prizes will be awarded to photographers who submit the winning entries in each of three categories: People, Animals and Scenic.

Mark your entries, either slides or prints, clearly with your name and Fairchild location and send them to the Employee Communications Office, mail stop 20-2260, Mountain View. Deadline for entries is August 15. Winning photographs will be published in the fall issue of HORIZONS.

Bob Huston:

SYSTEMS' SHOWMAN

Bob Huston, manager of software development, appears to spend almost as much time behind a podium as he does in his office and lab.

Bob is in great demand as a technical speaker, particularly when the program centers around the latest concepts in testing semiconductor devices. Talks on microprocessor testing have recently taken Bob to Wiesbaden, Germany; Paris; and Anaheim, California, where he participated in the NEPCON International Microelectronic Conference....and his talks have drawn record crowds.

The subject that is fascinating technical audiences around the world is the programming of testing for new microprocessors devices, in cluding Fairchild's own F8.

Bob is very careful, because of the nature of the conferences in which he participates and the expectations of his audience, to resist turning his address into a sales pitch for the System Technology testers. "I carefully explain in the beginning of my talk that all programs I describe have been developed for and checked out on a Fairchild tester, but, aside from one or two references to the capability of our testers, I concentrate on the test programming developments we have made, with the hope of giving the members of the audience new information that will aid them in their jobs."

However, even with the careful avoidance of overt selling techniques, many inquiries about Systems Technology products come from the members of Bob's audiences. His role as performer was arrived at naturally. "I've been performing since I was in junior high school," he says. "I played trumpet and regularly entered state-wide music competitions." But even with his lengthy history in handling audiences, describing microprocessor testing draws upon all of Bob's communication abilities. "A manufacturer or user of microprocessors faces the test problems inherent in RAMs, ROMs, shift registers, decoders, sequential states, counters, oscillators, and arithmatic logic units rolled into a single device.

"The audiences are eager," Bob states, "for any information that will make testing of the microprocessors more manageable, so that accounts for the numerous invitations I've received lately."

However, Bob's participation in technical conferences has gone beyond that of principal speaker. He has become so well-known in the tight, little community of technical experts in the testing business that he was recently asked to act as coordinator for a conference to be held in Vail, Colorado this summer. His experience on the conference circuit enabled him to assemble quickly a panel of top notch speakers, most of whom he has shared a podium with in previous conferences.

Though Bob is unchallenged as chief technical speaker for Systems Technology, he views his presentation at technical conferences and seminars as extra-curricular activity and does not allow it to infringe on his prime assignment. A marathon worker, Bob will enter the laboratory late Sunday evening and remain engrossed in projects for 48 hours running before leaving for home. This style of non-stop effort was developed while he was a student at Purdue and has been sustained throughout his career. "I relish the peace and solitude in the laboratory throughout the night and find that this is my most productive period. Meanwhile, the developments that are taking place in that laboratory in the small hours of the morning are providing the ideas for future papers which will be presented to technical audiences throughout the world.

Service has a dual meaning for field personnel

"Service" is an important part of the title that Systems Field Service personnel share. And they obviously take that title seriously in more ways than one. The Field Service Department has one of the longest service records among its employees, who claim between five and twelve years with the company.

New marketing approach for Europe

The Systems Technology Division is having its presence in Europe felt more acutely as the result of a new marketing approach. The Division is developing a network of national representatives to serve major European markets.

Managing the Systems Technology marketing efforts in Europe is Jim Healy, who is located at the International Division Europe headquarters office in Wiesbaden, Germany. Jim was formerly Asian Sales Manager for the International Division. He brings to his new assignment lengthy experience in marketing through representatives, a sales approach that has been used successfully by Systems Technology in Asia.

Recent additions to the European representative system are firms in Germany, France, South Africa and Israel which join Systems' established representatives in Scandinavia and Italy. Jim is currently negotiating for the establishment of a Systems Tech representative to serve Great Britain.

The movement toward national representatives in Europe has been beneficial in broadening the Division's exposure in these countries, Al Perry, International marketing manager for Systems Technology, said. "This new method of marketing has been underway only since August, but already we've begun to see a great deal of additional activity from Europe." In the Systems Technology order cycle, test equipment usually represents a sizeable capital expenditure for the customer and, therefore, an order takes up to a year for conclusion depending on the purchaser's budgeting calendar.

"We're obviously benefitting from the broader coverage we receive through national representatives," Perry adds. "It should prove to be the most economical and beneficial approach to reaching potential customers in European countries. All of our representative firms have established reputations in the nations in which they do business and are known to most of the companies which would have use for our products."

Jim Healy, European marketing manager of Systems Technology reports to Don Brettner, general manager of Fairchild's European operations. Jim was replaced in Tokyo as East Asian sales manager by Dave Wiesen, who reports to Andy Procassini, general manager, marketing, Asia/Pacific area.

Systems bounds away with basketball title

The point spread in the Fairchild basketball league only once became so tight that Systems Technology basketball players really had to pour on the heat to maintain their lead. The DIC marketing team, on May 7, shook Systems Tech's complacency with a game that ended 52-48. But no matter how you measure, Systems Tech ended league play unbeaten in the fast-paced, intra-company competition.

In the nine league games, score spreads ranged from an impressive 34 points to the narrow four in the DIC contest.

The Systems Tech team entered the play-off on May 21 to face winners of the first elimination, one of the deciding challenges. The result: a 64-56 win. They met the second place team on the courts at Awalt High School on June 4. A win in that game secured the Fairchild basketball title for Systems Technology. Team members are: Mike Holley, Keith Erickson, Mike Soutas, Randy Howard (captain) Bob Merrill, Roy Van den Akker, Bob Warner, Ron Nelson and Zeke Valladolid.

TAKING HOME THE TROPHIES: Systems Tech's top bowlers and teams claimed trophies at the annual awards banquet held May 21 at Michael's in Sunnyvale. Above, members of the first place team (left to right) Army Armstrong, Ruth Zabel and Fran LaValley accept their awards with smiles. Ruth juggles trophies for Joe Cotey and Nu Weaver who were unable to attend the banquet. Center, Bob Crabb clutches the trophy for the high handicap performance (277); and (right) Marian Oswald and Fran La Valley claimed a tie for the women's high scratch game (214). Other significant accomplishments over the season were: Judy Lang, women's high handicap game (263); Carol Graham, women's high handicap series (679); Bernie De Los Angeles, men's high handicap series (733); Ralph Colbacchini, men's high scratch game (254) high scratch series honors went to Michele Jorgensen (558) and Dennis Shutter (632). Second place team members are Carol Graham, Michele Jorgensen, Linda Holthouse, Len Holthouse and Tony Barela.

FST in a word

To some it is a seemingly endless stream of paperwork; to others it is a moving experience sprinting around the plant eight hours a day; to yet others it is components and parts and wires; to still others it is a mind-bending experience attempting to match test problems to hardware solutions; and to some it is an exercise in communications--the voice at the other end of the phone line and the recipient of the letter.

Everyone has their own point of view on the Systems Technology experience, and that view is largely determined by the job in which the individual is involved. Beyond that, every Systems Technology employee also has an overview of the division--a succinct impression that is the combination of all the activity within the walls of 1725 Technology Drive.

This is what Tech Talk sought in a brief trip around the plant recently--a one-word description of life at the division. From Ruth Zabel came the word "interesting," from Steve Small, "provocative," and Jerry Carson added "well-seasoned." (If you read these three adjectives in order, you arrive at a well-known product commercial. We can only assume that Jerry believes working at Systems Tech is somehow like eating potato chips. Absurd. It's more like nibbling pretzels.) And the final word or words came from Roxie Reddick, "I take the fifth amendment." What does the combination of this quartet's comments on the Systems Technology experience tell? Our experts in communication, after lengthy analysis, decided it sounds like fun.

Ruth Zabel

Steve Small

Jerry Carson

Roxie Reddick

Women bowlers take honors

A Fairchild woman's team entered in the city tournament on March 1-2 and 8-9 represented the company admirably by taking cash awards in all events. The Positive Thinkers--Barbara Butler, Marian Oswald, Vickie Risso and Peg Wood--took tenth place in the overall tourney. Marian and Peg claimed 15th in the B doubles event; and Peg took a ninth in the B singles and first place in B Division, All Events. The tournament, held over two weekends, took place at the Cherry and Camino Bowls.

Marian reports that a woman's bowling team will enter the State Tournament in San Diego in July. A women's team of 10 members is also entered in the Fairchild East-West intra-company tourney. In this competition, the top players of the West Coast pit their skills against Fairchilders working in East Coast plants. Weekly individual and team standings are reported in the mail and top teams and individual players are judged on the basis of performance during April.

The West Coast women's team claimed the trophy in the 1975 competition, and the semiconductor-west men's team took top honors for its performance in the long-distance contest.

Monster management (continued)

handle the sales of the smaller test systems throughout the country. Though Jerry and newly appointed sales manager for small systems, Earl Jones, are anxious to expand the organization of representatives to cover still open territory, the current sales force has developed to the point of continuing a training program for the manufacturers' representatives. Beginning this month and throughout the summer, detailed training in the applications and attributes of Systems Technology's small testers will be conducted for the 110 salespersons working for the 15 manufacturers' representatives who will be responsible for getting the Systems Technology name to customers who have a need for these products.

Jerry has a well-developed knowledge of the capabilities and market potential of the Qualifier 901 and its related products because he was a member of the team that initially developed the concepts for the Qualifier. "With the smaller test systems," he explains, "we are dealing with a customer who expects demonstration of the product at his site, 30-day delivery, and rapid spare parts and repair responses. It is a vastly different relationship than that which occurs with our large systems purchasers. No one expects an in-house demonstration of a room-sized system. If it takes two years to decide on the purchase of a test system with a $100,000 price tag, it is highly unlikely that the customer will demand that it be manufactured and delivered in a month. A buyer of a high cost system has the right to expect, even demand, the immediate and undivided attention of a member of the Division's field service force when something goes amiss."

Maintaining this high level of product performance and service that customers have grown to expect in large test systems while delivering a low-cost product is the monster that Jerry wrestles each work day. Determination and organization will be the weapons that will conquer this marketing challenge.

Rec council plans active calendar

The Rec Council party planners recently unveiled a dazzling calendar of events for the next several months. Leading the schedule was the Moonlight Cruise on the Bay, which drew more than 170 employees and their guests on May 16. Nature performed beautifully for the Systems Tech party. Clear skies, calm waters and a refreshing, rather than chilling, breeze added pleasure to the round trip from Fisherman's Wharf to Jack London Square.

Employees and their guests arrived in Oakland at approximately 8 p.m., visited the restaurant of their choice for dinner and regrouped aboard the cruise ship at 10:30 for the return trip. "San Francisco was magnificent--a jewel gleaming in the dark, making the return trip particularly memorable, "Kay Fields, Rec Council president, reports.

Saturday, June 14 is the date the Rec Council has set for the annual picnic. The site will be Blackberry Farms where Systems Tech employees and members of their families will have exclusive use of Sycamore Grove from 9:30 a.m. until the park closes. Division directors are being recruited to man the barbeques and will prepare steak and hamburgers to order from 11:30 a.m. to 2 p.m. on that day. Tickets are priced at $1.50 per person for a steak luncheon, 50 cents for hamburgers, and are available from Recreation Council representatives.

Entertainment will include bingo and a softball game in the morning and volleyball and horseshoe competitions throughout the day. The Rec Council will equip a games and crafts area for small children. Tickets will be on sale through June 9.

--August Buses loaded with Systems Technology employees and their guests will head for a weekend in Lake Tahoe or Reno.

--October Plans are taking shape for a Halloween Party.

--November will bring a spaghetti and bingo party for employees, their spouses and guests.

And in December the Rec Council will reach the peak of their party planning with a holiday dinner-dance for employees, their spouses and guests.

This party-a-month program is designed to offer events and excursions to entertain everyone.

Grunts, groans and giggles emanate from the prep area of manufacturing every afternoon around 2 p.m. Those are the sounds of women in search of improved physical fitness. Led by Alice White, physical fitness hobbyist, several members of the manufacturing department meet each day during the afternoon break to bend, twist and stretch their way toward smaller waistlines and improved muscle tone. Alice, who has been pursuing a strenuous exercise regimen for more than three years, has lost almost 50 pounds and now heads for the trim size 10s when she goes clothes shopping.

Though the coffee break exercise group has been meeting for less than a month, Roxie Reddick claims she can see visable results in her waistline; Annie Eaker can, for the first time in years, bend over to tie her shoes without bending her knees; and Yoyo McCullan proudly shows how loosely her waistband fits. Deborah Washington, when asked the changes the exercise program has made in her physical well-being, said "I hurt all of the time." Annie Mitchell, Chris Calloway and Eloise Reyes have each given up two inches of waistline in the coffee break exercises.

Heir raising

Marilyn (former Fairchild employee) and Larry Bell (He works in the Phoenix Field Service Office) became the proud parents of a daughter, Candice Lee, on April 16. Betty and Ed McLaughlin welcomed a daughter on January 24. Her name is Andrea. Kirsten and Ray Badger became parents of a son, Eric Torvald, on May 5.

the sports scene

The patio area adjacent to the cafeteria will be the scene of sports life beginning in mid June. Once the work day is over, employees will turn their thoughts to volleyball, shuffleboard, ping pong and putting contests organized by fellow employees.

Tom Cox is the brains behind the volleyball tournament which will be conducted over the summer months. Ten six-person teams are expected to play Tuesdays and Thursdays after work in a double elimination tournament.

Plans are also taking shape for ping pong, shuffleboard and putting contests for employees whose sports prowess lies in these areas. Watch the bulletin boards for registration instructions for these tournaments.

U. S. Sales Offices

Fairchild Systems Technology
3080 Olcott Street
Suite 100C
Santa Clara, CA 95050
Telephone: (408) 998-0123
TWX: 910-338-0558

Fairchild Systems Technology
931 South Douglas Street
Suite 115
El Segundo, CA 90245
Telephone: (213) 678-3166
Tie Line: 223

Xincom Systems
8944 Mason Avenue
Chatsworth, CA 91311
Telephone: (213) 341-5040
TWX: 910-494-2769

Fairchild Systems Technology
9950 West Lawrence Avenue
Suite 318
Schiller Park, Illinois 60176
Telephone: (312) 671-4480
TWX: 910-227-0056

Fairchild Systems Technology
500 West Broadway
Suite 103
Tempe, Arizona 85282
Telephone: (602) 966-7297
TWX: 910-950-4699

Fairchild Systems Technology
7600 Parklawn, Room 251
Minneapolis, Minn. 55435
Telephone: (612) 835-3322
TWX: 910-576-2944

Fairchild Systems Technology
505 Northern Blvd.
Great Neck, N.Y. 11021
Telephone: (516) 466-6393
TWX: 510-223-0838

Fairchild Systems Technology
1790 E. Marlton Pike
Cherry Hill, N.Y. 08003
Telephone: (609) 424-3100
TWX: 710-896-1381

Fairchild Systems Technology
303 Whooping Loop
Altamonte Springs, Florida 32701
Telephone: (305) 834-7070

Fairchild Systems Technology
888 Worcester Road
Wellesley, Massachusetts 02181
Telephone: (617) 237-4787

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B. HUSTON
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Mrs. Nancy Huston
5819 Vargas Ct
San Jose, CA 95120

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A FAIRCHILD INSTRUMENTATION & SYSTEMS NEWSLETTER

FAIRCHILD

vol.2 no.8

september-october, 1976

INTEGRATOR AND SENTRY VII INTRODUCED AT WESCON '76 SHOW

Wescon '76, which was held in Los Angeles during September, was another successful trade show effort for Fairchild. We introduced two innovative products — INTEGRATOR and Sentry VII — which created a great deal of excitement. Also displayed at the show were Xincom III, the F-8 Formulator, and a new digital panel meter featuring .8" LED display. With show attendance exceeding 38,000, Fairchild's products were exposed to one of the largest show audiences in recent times.

The INTEGRATOR takes test data from multiple and remote test systems and performs data reduction and analysis on the data generated by the individual test systems without slowing the throughput of any tester. The INTEGRATOR thus provides management test data for important decision-making applications.

Sentry VII is our newest test system with up to 196K of memory storage. This eliminates the need for pulling individual programs or routines from disc storage. The entire software program can now be stored in memory and used as needed, significantly increasing throughput.

For details on any of the products displayed at Wescon, please contact your local Fairchild sales office, or Marketing Services, FST, 1725 Technology Dr., San Jose, CA 95110 at (408) 998-0123.

Brian Sear, Divisional Vice President of Fairchild Systems Technology, presents Sentry VII and INTEGRATOR at Wescon '76. Invited customers and prospects also viewed a film on the new products along with a slide presentation given by Bill Howe. A question and answer session was followed by cocktails.

Bob Huston (l) observes as Bob Hickling (r) types in commands on the CKT connected to Sentry VII during Wescon.

LOOKING FORWARD TO ELECTRONICA '76

Electronica '76, Munich, Germany (Nov. 25-Dec. 1) will be a significant show for Fairchild Systems Technogy. We'll exhibit our new semiconductor test systems — Sentry VII, INTEGRATOR, and Xincom III. All three systems will be demonstrated "live" to underscore the importance of the distributed test system concept and its impact on cost-effective management decision making.

Invitations to the demonstrations and briefings have been sent to prospects who plan to attend. The Sentry VII brochure will be translated into German for distribution at the show.

MORE WESCON

Ken Rinaldo, Mgr. of Advanced Engineering (l) and Art Winter, Consultant (r) at work in the Instrumentation Division section of the Fairchild Wescon booth. A popular attraction in this portion of the display was the digital scale where attendees could see their weight in digital readout.

XINCOM DOCUMENTATION AND MAINTENANCE TIPS

Updates to Xincom 5551 DMT documentation will soon be available from the FST Training Center. Included are: table of contents for the schematic notebook, deletions from this notebook of items no longer in use, and up-to-date schematics for refresh, pins down, and F8 when a Nova 3 computer system is added to the 5551. This documentation is available to all former Xincom students on a request basis to the FST Training Center, Diane Lynch, 1725 Technology Dr., San Jose, CA 95110; (408) 998-0123.

If you are having trouble with the brass stand-offs in the test head, contact your local Fairchild field service office and arrange to have new steel stand-offs installed.

Power-up reset is available on request and can be installed by your local Fairchild field service office.

Probe ring adapters to aid in easy alignment of the Xincom scrambler cards to the test head are also available as a field service-installed retrofit.

NEW FROM SOFTWARE SYSTEMS

Sentry Revision 10.4E is now released and available from SOCD. Major features include memory management to handle both the FST-1 and FST-2, improvement of ALLINK handling, removal of the // and /. requirements in DOPSY and TOPSY, and much more. Some specific examples are:

- With DOPSY, a user can choose to run only part of a DIF file using an added NOTE capability.
- TOPSY now has capability for NOTE, as well as SET, for I/O devices.
- A new command, VAR, in TOPSY allows for displaying and/or writing variables at run time. This includes an array display option.
- Up to six ALLINK programs can be co-resident.
- DATALOG device can be changed without altering the options. Datalog of every n'th device has been added.

ALSO AT WESCON. . . AN ANIFORM CHARACTER NAMED "TINY"

"Tiny," an Aniform cartoon character, provided comic relief in the Fairchild booth during Wescon. Tiny entertained attendees and expressed salient opinions on the technical presentations given in the booth. Aniform characters are created by a technique employing closed-circuit TV, audio equipment, and a live performer situated in a booth. Good-natured Fairchild personnel acted as straight-men during Tiny's entertaining performances.

FAIRCHILD SYSTEMS TECHNOLOGY FIELD OFFICES

Fairchild Systems Technology
931 South Douglas Street/Suite 115
El Segundo, California 90245
Telephone: (213) 678-3166
Tom Engels, Service Mgr.

Fairchild Systems Technology
3080 Olcott Street/Suite 100C
Santa Clara, California 95050
Telephone (408) 998-0123
TWX: 910-338-0558
Jim Leonard, Service Mgr.

Fairchild Systems Technology
303 Whooping Loop
Altamonte Springs, Florida 32701
Telephone: (305) 834-7070
Ben Oatley, Service Mgr.

Fairchild Systems Technology
537 Foundry Road
Norristown, Pennsylvania 19401
Telephone: (215) 631-1500
Ron Morse, Service Mgr.

Fairchild Camera & Instrument Corp.
6202 Wiesbaden-Biebrich
Postfach 4559, Hagenauer Str. 38
Telephone: 06121 2051
Telex: 841-4186588
Dieter Kramer, Service Mgr.

Fairchild Systems Technology
John Scott House, Market Street
Bracknell, Berks., England RG 12 IDQ
Telephone: (0344) 21101
Telex: 849467
Jack Seed, Service Mgr.

Fairchild Camera & Instrument Corp.
121, av. d'Italie, 75013, Paris 13e
Telephone: 00331 5805566
Telex: 0042 20614
Ray Valensi, Service Engr.

NEW LITERATURE

Panel Instruments

Instrumentation Application Note 2, Rev. 1, "External Decimal Point Selection." Provides instructions on how to incorporate the External Decimal Point Selection option on meters. Decimal point positions and board assignments are given.

"Model 80 3-½ Digit Panel Meter, 115 VAC Line Power Input, 0.8" LED Display." This four-page brochure provides descriptions of features, detailed specifications and dimensional drawings, along with prices and ordering information. Delivery is December 1; accepting orders now.

"Model 55 Variable Time Base Counter" data sheet. Delivery is November 1; accepting orders now. Contact your local rep or the factory for further information.

Sentry Test Systems

Technical Bulletin 9, "Test Strategy Trends for LSI/GSI Technology." This paper discusses the evolution of a high speed general-purpose LSI/GSI test system. The system approach provides advanced capabilities to test the new generation of semiconductor parts that include microprocessors, large memories and telecommunication devices. Various approaches to the strategy of test are discussed in the context of obtaining a "worst case" test environment.

Application Note 57, "Testing a TV Character Generator with the Sentry II Sequence Processor." A test program for a MOS-integrated circuit intended for displaying a TV channel number on the screen of a TV receiver was recently completed. This program uses a number of sequence processor features and this note should easily relate to Sentry II capabilities.

Testing: 1, 2, 3 folder with brochures on Sentry VII, Integrator, and Xincom III; Management testing information; IC Testing; and Dedicated Memory Testing information.

Application Notes/Technical Bulletins — Sentry and Xincom Test Systems. An updated listing of application notes and technical bulletins on Sentry and Xincom test systems is now available.

To request any of the above documents, contact the local Fairchild System sales office or Patti Greig, Marketing Services, Fairchild Instrumentation and Systems Group, 1725 Technology Drive, San Jose, CA 95110; (408) 998-0123.

Small Systems Make a Good Showing at NEPCON/Central

PATT AND QUALIFIER FEATURED AT NEPCON/CENTRAL

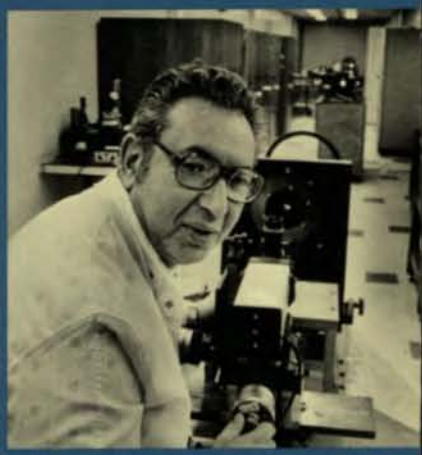
Small systems from Fairchild were highlighted in our booth at NEPCON/Central which took place Sept. 28-30 in Chicago. Featured were PATT (Programmable Automatic Transistor Tester) and the Qualifier™ 901 IC Tester.

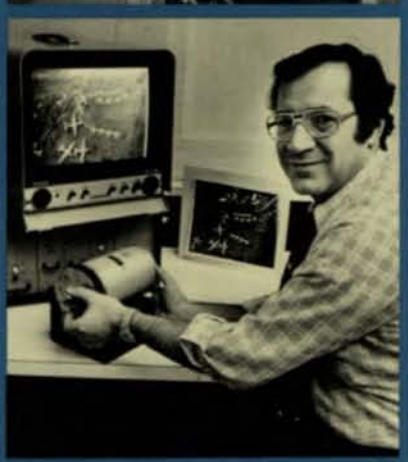
Earl Jones, Marketing Manager for Small Systems, has asked us to print this message from him: "I would like to thank all of those persons who returned their Semiconductor Test Equipment Questionnaire. As stated in the letter you received with the questionnaire, a drawing was to be held at the NEPCON/Central show on the 28th of September. However, because of the late mailing, you could not return them in time for the drawing. Therefore, be assured that the drawing for the watches will be held and the winners will be published in the next *interface* publication."

Fairchild Camera and Instrument Corporation

Annual Report 1976









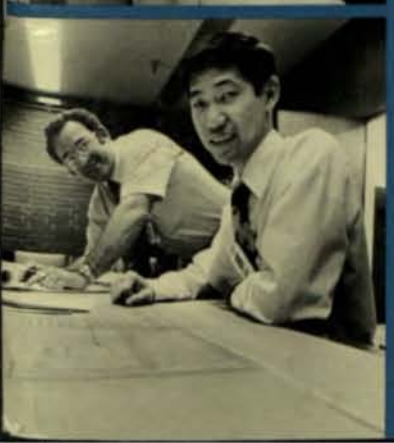




TABLE OF CONTENTS

On the cover:
Fairchild people at work on varied products...from microprocessors to miniature television cameras.

Annual Meeting of Shareholders
The annual meeting of shareholders of Fairchild Camera and Instrument Corporation will be held at Rickey's Hyatt House, Palo Alto, California, on Friday, May 6, 1977.

FINANCIAL HIGHLIGHTS

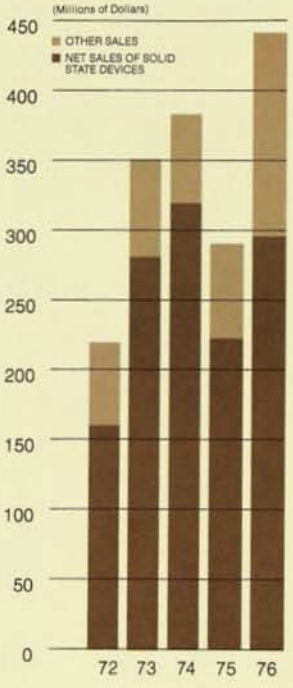
	1976	1975	% Change
For the year:			
Net sales	$443,221,000	$291,542,000	+52.0
Income before cumulative effect of change in accounting method	$ 12,456,000	$ 10,424,000	+19.5
Cumulative effect on prior years (to December 29, 1974) of change in accounting method	–	$ 2,649,000	–
Net income	$ 12,456,000	$ 13,073,000	−4.7
Average number of common and common equivalent shares outstanding	5,476,865	5,372,901	+1.9
End of year:			
Working capital	$113,865,000	$100,506,000*	+13.3
Shareholders' equity	$177,609,000	$166,329,000*	+6.8
Number of employees	21,293	17,405	+22.3
Number of shareholders	10,429	11,179	−6.7
Shares issued	5,359,552	5,278,563	+1.5
Per share statistics:			
Income before cumulative effect of change in accounting method	$ 2.27	$ 1.94	+17.0
Cumulative effect of change in accounting method	–	.51	–
Net income	2.27	2.45	−7.3
Shareholders' equity at year end	33.14	31.51*	+5.2
Cash dividends	.80	.80	–

**Restated – see Note 3 of the Notes to Consolidated Financial Statements.*

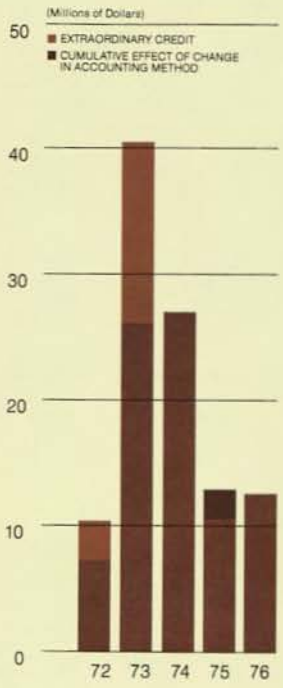
Annual Report on Form 10-K

Fairchild's Annual Report on Form 10-K for the year ended January 2, 1977, as filed with the Securities and Exchange Commission, contains additional information about the company and is available to Fairchild shareholders on request, without charge. Please write: Corporate Communications Department, Fairchild Camera and Instrument Corporation, 464 Ellis Street, Mountain View, California 94042.

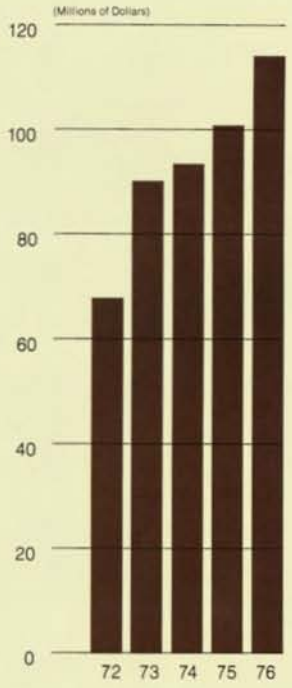
NET SALES



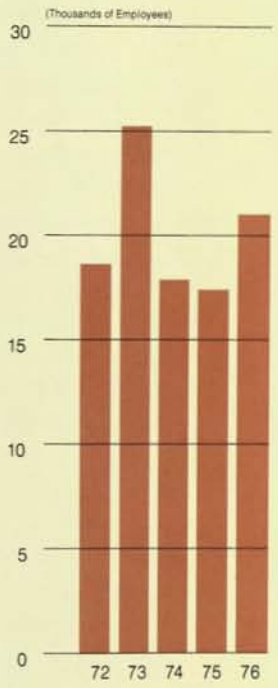
NET INCOME



WORKING CAPITAL



EMPLOYEES AT YEAR END



TO OUR SHAREHOLDERS:

While on many counts 1976 was a difficult business year, it was a milestone for Fairchild Camera, particularly as we begin our fiftieth anniversary as a company.

Worldwide sales grew 52 percent, to the all time high of $443,221,000, from $291,542,000 the year before. All portions of the company contributed to this record, which constitutes an important benchmark in our long-term corporate growth.

Earnings rose 20 percent to $12,456,000, or $2.27 per share. This compares with $10,424,000, or $1.94 per share in 1975. The company reported an additional $2,649,000, or 51 cents per share, in 1975 as the result of an accounting change.

Although sales gained momentum early in the year, profit margins came under pressure from excessively low pricing on commodity components, related to the 1975 recession. Earnings were further depressed by the financial impact of a semiconductor production problem which surfaced in late 1975. Both of these situations improved in subsequent quarters.

The overall business climate changed at mid-year from one of vigorous recovery to a general slackening of demand. Despite this economic pause, our earnings rose in the second half, enabling us to report $2.27 per share for the full year.

We are still feeling the effects of the slowdown in components and consumer products. The components market, sensitive to economic trends, has been flat for some months. The consumer products business currently reflects the seasonal, post-holiday lull in buying activity. We expect 1977 as a whole to be a good year, however, as we believe demand will resume its uptrend in the spring.

The company introduced a broad spectrum of advanced, electronic products last year. These included new logic and memory devices, semiconductor test systems, audio/visual equipment and solid-state television cameras. Our position in the LSI (large scale integration) and microprocessor markets continued to grow stronger and represents by far the highest potential portion of our semiconductor business.

Consumer electronics—a field in which the company was not engaged two years ago—has become a new growth area for Fairchild. In addition to digital watches and clocks, we developed and brought to market the Fairchild Video Entertainment System, a programmable home TV game based on our F8™ microcomputer. The system won approval of the Federal Communications Commission in the fourth quarter and limited shipments took place during the holiday season, with excellent customer response.

TM Trademark of Fairchild Camera and Instrument Corporation

The company is in a strong financial position. Working capital at the end of the year was $114 million and shareholders' equity $178 million. Cash and short-term securities approximated $27 million. Inventories during 1976 rose by only 4 percent, despite our 52 percent increase in sales.

Fairchild has moved aggressively to obtain the necessary funds for anticipated future growth. In December, our wholly-owned subsidiary, F.C.I. International Finance N.V., generated additional capital through the sale of $20 million of 5¾ percent convertible subordinated debentures in the Eurobond market. Last month, Fairchild was listed for trading on the London Stock Exchange.

These activities reflect both the strong interest in our company in Europe and the rapid growth of our international business during the past five years. Foreign sales in 1976 exceeded 30 percent of the total.

Despite the lag in the economic growth rate, we have continued to invest significantly in new product development and expanded production facilities around the world. Spending for research, development and engineering in 1976 was approximately $47 million. Capital expenditures amounted to $36 million.

The result of these investments is to give Fairchild a technical and manufacturing capability matching the opportunities we see ahead in our various markets. As a company, our strategic thrust will be in those technologies which have the greatest growth potential. Our target is to penetrate new markets—including those for semiconductor-based end products—and to grow profitably on the frontiers of the LSI revolution.

Since 1927, our people have been designing, building and selling products that have made contributions to progress...from the first aerial camera to the Planar transistor and the modern integrated circuit. The skill and commitment of Fairchild employees have made us a strong, expanding company and an industry leader.

As we move into our second half-century, we will continue to build on that tradition.

Roswell L. Gilpatric
Chairman of the Board

Wilfred J. Corrigan
President and Chief Executive Officer

March 14, 1977

BOARD OF DIRECTORS

Wilfred J. Corrigan,
Louis F. Polk, Jr.,
Directors

William A. Stenson,
Director
Roswell L. Gilpatric,
Chairman

William C. Franklin,
Albert Bowers,
Directors

C. Lester Hogan,
Vice Chairman
James B. Lampert,
Director

Not pictured:
J. Bradford Wharton, Jr.,
Director

Inset:
Roswell L. Gilpatric,
Chairman of the Board;
Wilfred J. Corrigan,
President and
Chief Executive Officer

MANAGEMENT OVERVIEW

Fairchild Camera and Instrument Corporation is organized into six manufacturing/marketing operations in addition to a corporate staff. Collectively the groups produce semiconductor components, systems and end products for the consumer, commercial, industrial and government markets. The company has some 30 manufacturing plants in four states and eight foreign countries.

Semiconductors, a basic product line of the company, are manufactured and marketed by the LSI Group, headed by David J. Marriott, and the Components Group, headed by George D. Wells. Both groups are headquartered in Mountain View, California. John A. Duffy, Jr. is in charge of the International Division, with responsibility for all foreign marketing.

The Instrumentation and Systems Group, based in San Jose, California, manufactures and markets semiconductor test systems, microprocessors and related products, digital panel meters, data acquisition and analysis instruments, and memory systems. James D. Bowen is general manager.

In addition to digital electronic watches, the Consumer Products Group is responsible for digital clocks, video entertainment systems, and a line of optoelectronic products and watch components. Managed by Greg Reyes, this group is presently based in Palo Alto, California, but will be relocating to a new facility in Santa Clara, California, before the end of 1977.

Louis H. Pighi manages the Federal Systems Group based in Syosset, New York. Primary product lines include electronic data systems, radio-frequency monitoring systems, aerial reconnaissance and surveillance systems, and a range of imaging systems based on the CCD (charge-coupled-device) miniature television camera.

The Industrial Products Division is located in Commack, New York, and produces a line of audio-visual equipment for the commercial and industrial markets in addition to a variety of systems and products for aircraft use. Raymond G. Hennessey is division manager.

At corporate level, Warren J. Bowles heads industrial relations, including personnel management and employee training and development programs. Frederick M. Hoar is responsible for internal and external communications, including financial relations, public affairs and advertising.

Fairchild's corporate finance operation is headed by R. Douglas Norby. A. J. Hazle is controller and James A. Unruh is in charge of treasury and corporate planning. Dr. Thomas A. Longo, chief technical officer, has responsibility for overall research and development. Nelson Stone is corporate secretary and general counsel, managing the company's legal and patent affairs.

CORPORATE VICE PRESIDENTS

Left to right, standing: Nelson Stone, General Counsel and Secretary; Frederick M. Hoar, Communications. Seated: Dr. Thomas A. Longo, Chief Technical Officer.

Left to right, standing: George D. Wells, Components Group; John A. Duffy, Jr., International Division; Greg Reyes, Consumer Products Group; David J. Marriott, LSI Group. Seated: James D. Bowen, Instrumentation and Systems Group.

Left to right: Raymond G. Hennessey, Industrial Products Division; Louis H. Pighi, Federal Systems Group.

Left to right: A.J. Hazle, Controller; R. Douglas Norby, Finance; James A. Unruh, Treasury and Corporate Planning.

Inset: Fairchild president and corporate vice presidents hold regular, off-site planning and strategy meeting.

Not pictured: Warren J. Bowles, Industrial Relations

LSI GROUP

Formation of the Large-Scale Integration Group in 1976 spotlights the growing importance of LSI products to our total business. LSI is the term applied to integrated circuits of high complexity and density, frequently in the thousands of components per silicon chip. Our new 265,000-square-foot wafer fabrication plant in San Jose, California, is one of the industry's largest and most modern production facilities dedicated to LSI.

Bipolar Memory and ECL Products This division maintained its dominance of the bipolar memory and high-performance ECL (emitter-coupled logic) markets. New, programmable read-only memories (PROMs) were added to the product line, finding widespread use in microprocessor systems.

The introduction of products combining our proprietary Isoplanar process with injection logic technology (I^3L), made possible the first 4,096-bit bipolar dynamic random access memory (RAM). The 4K dynamic RAM offers the speed of bipolar circuitry at costs comparable with high performance MOS memories, and is the forerunner of a 16,384-bit bipolar memory, scheduled for later this year. A 4K bipolar static RAM utilizing conventional circuit technology also is scheduled for 1977.

Development of a 16-bit bipolar microprocessor, utilizing I^3L technology, was also announced. This product will find many high-end applications during the next five years. Fairchild's sub-nanosecond (trillionths-of-a-second) ECL logic family found significant use in the mainframe computer industry, and total ECL sales quadrupled during the year.

MOS/CCD Products Shipments of components for the Fairchild F8™ microprocessor increased during the year. The F8 is aimed at volume applications in the consumer and industrial areas, including TV tuning, video recorders and games, appliance controllers and "smart" terminals.This division also filled volume orders for MOS (metal-oxide semiconductor) memory devices, including the 4K N-channel RAM produced in our Wappinger Falls, N.Y., plant, and introduced a 16K N-channel RAM in the first quarter of 1977.

In CCD (charge-coupled device) technology, additional imaging arrays were introduced and an improved CCD analog delay line, available in component form or module assembly, designed for European television systems.

Fairchild increased its share of the CCD memory market with its 9,000-element serial memory and its 16,000-bit line-addressable RAM. These products are forerunners to the 65,000-bit CCD memory scheduled for pilot production later this year. Primary applications for the 65K part will be in bulk serial back-up memories for computers.

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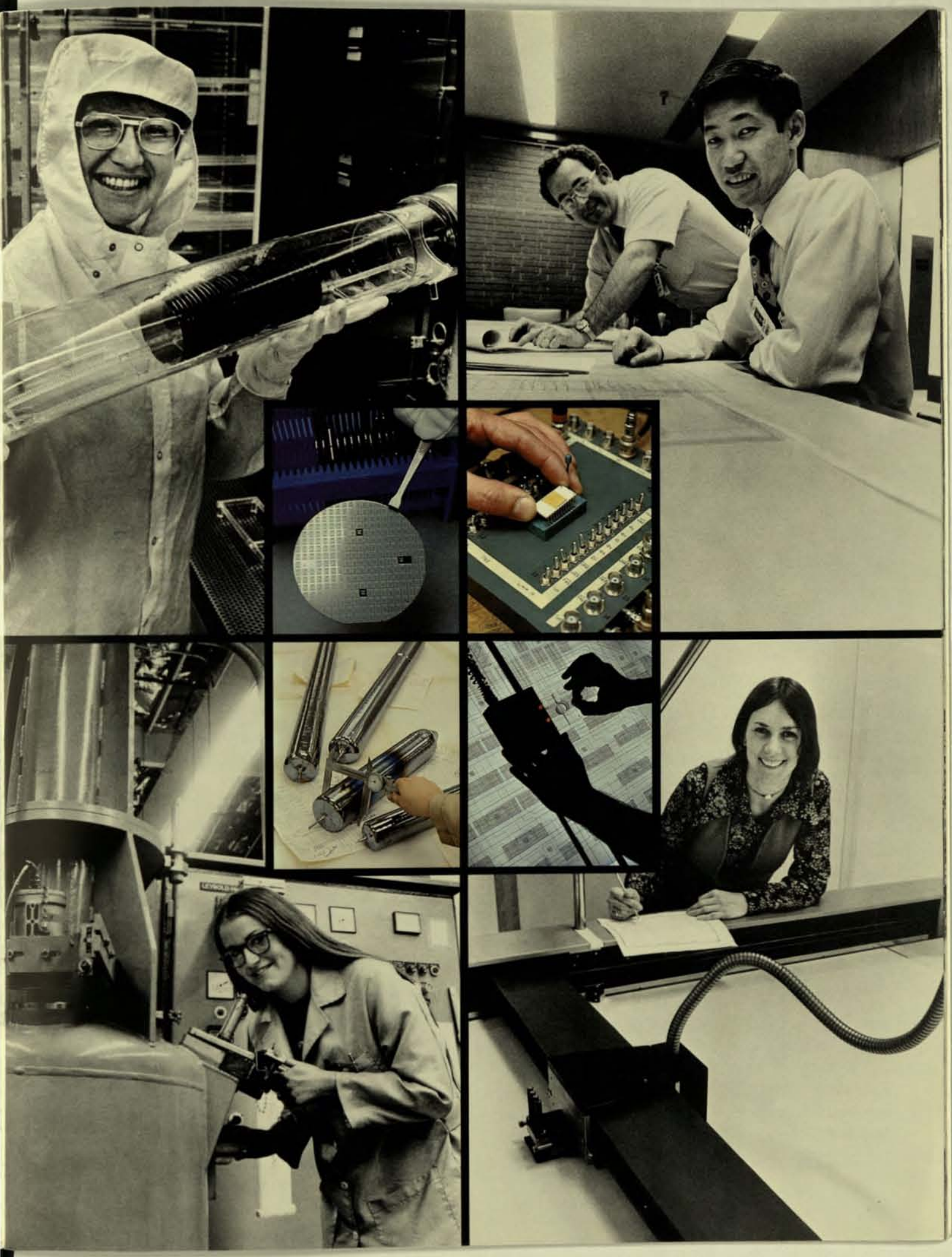
Diffusion operator Ena Aulicino handles MOS circuit wafers at Wappingers Falls plant. Inset: Typical LSI wafer.

Bipolar circuit designers Larry DeClue and Daniel Wang study advanced microprocessor engineering drawing. Inset: Prototype circuit under test.

Operator Dorothy Dudley checks silicon crystal growth in Healdsburg plant. Inset: Completed silicon ingots.

MOS circuit designer Solange Keefe uses computer-driven drawing machine. Inset: Digitizer converts artwork to computer tape information.



COMPONENTS GROUP

New capital investments, coupled with the application of cost reduction measures, helped increase efficiency in our various components divisions. Materials costs, as an example, were reduced through smaller die sizes and new metallization techniques. High-speed, automated handling and test systems were installed in the Far East. The global logistics program, initiated in late 1975, enabled the group to reduce inventories while at the same time improving customer service in the United States, the Far East and Europe.

Digital Products Heavy pricing pressures on commodity-type semiconductors continued to depress the digital products market in 1976. Fairchild expanded its digital product line, including new CMOS (complementary MOS) integrated circuits and low-power Schottky TTL (transistor-transistor logic) devices. Because of their inherent low power drain and high noise rejection characteristics, CMOS circuits are finding widespread use in both consumer and industrial products, particularly in battery-powered instruments. Low-power Schottky is rapidly becoming the standard logic family in most bipolar systems.

Linear Integrated Circuits Fairchild expanded its long-established market position in consumer electronic components with new circuits for television sets and audio equipment. The company saw major growth in Europe where Fairchild is the largest U. S. supplier of PAL (phase-alternating line) TV circuits, the primary broadcast circuits used outside the United States. The division also brought to market a range of new industrial circuits, including high-speed dual operational amplifiers and fixed or adjustable voltage regulators.

The Automotive/Hybrid Unit increased production of solid-state ignition systems for the automotive market, and late in the year introduced a family of high-current regulators that have gained rapid acceptance in power supply design.

Discrete Products The Diode Division's production of silicon diodes, zener diodes and diode arrays increased substantially during 1976. In particular, gains were made in the market for zener diodes, used to provide a stable voltage source in many types of consumer and industrial end products.

The Transistor Division continued to serve the discrete market with a broad line of high-performance transistors, both small-signal and power. More than 50 devices were added to the power transistor line, including a new package type called Dynawatt™ which provides a high degree of power handling capability at very low cost.

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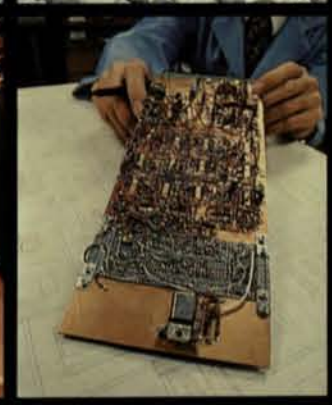
John Reimer helped design machine that doubles diode test rate at San Rafael. Inset: Diodes being packed for shipment.

Test operator Insoon Carman inspects handler during power transistor testing. Inset: Power transistors packed for shipment.

Noella Chadbourne operates automated film-bonding machine that completes integrated circuit connections in one step. Inset: Conventional wire-bonding procedure.

Linear Division engineer Don Smith checks performance of new color tv circuit design. Inset: "Breadboard" of integrated circuit prototype.



INSTRUMENTATION AND SYSTEMS GROUP

The company's position and scope in the instrumentation field gained steadily throughout 1976. The group now encompasses a diversified product line, including distributed test systems, microprocessors, memory systems, digital panel meters and data acquisition systems. This portion of our business will continue to grow in strategic importance to the company.

Systems Technology The Sentry™ IV and Sentry™ VII computer-controlled semiconductor test systems and the Integrator™ data communications systems were the key introductions of the group's largest division. The Sentry systems provide fast, flexible testing capabilities for LSI devices. Sentry VII is designed to interface directly with the Integrator in a test network that integrates raw data from on-line testers to provide status reports at various stages of semiconductor processing.

The Xincom III, introduced in May, is the first commercial tester to make use of distributed system architecture—a concept that permits numerous remote test heads to communicate with a central host computer. The Xincom III is designed primarily for memory testing.

Microsystems This division was formed in 1975 to handle company efforts in the area of microprocessor systems and microcomputers. The two-chip F8™ microprocessor has been the catalyst of this division's growth, gaining a dominant position in the low-cost, high-volume segment of the controller field. Early in 1977 the division announced a one-chip F8 that is expected to further penetrate this market.

During the first quarter of 1977, production began in a 50,000-square-foot addition to the Instrumentation and Systems plant in San Jose, California, housing a fully-automated printed circuit assembly line for microprocessor systems. As part of a technology exchange agreement with Motorola, Inc., Fairchild announced in October that it will also manufacture the Motorola 6800, a leading microprocessor for the data processing industry.

Instruments In December, Fairchild acquired Data Works Instrumentation of Chatsworth, California, a manufacturer of microprocessor-based data acquisition and analysis instruments used primarily in the solar, environmental and process industries. Data Works became part of the Instrumentation Unit, formed in 1975 to produce and sell digital panel meters to electronic instrument manufacturers.

Memory Systems Several large, high-speed bipolar memory systems were shipped during the first quarter of 1977, and design activity is being carried out on other products ranging from complete systems to board-level subsystems. This effort utilizes all of Fairchild's advanced LSI technology, including 4K and 16K MOS and bipolar memories, CCD memories, and Isoplanar integrated injection logic devices.

Emma McConaghy assembles microprocessor components for a microwave oven controller. Inset: Formulator™ microprocessor development system.

Digital panel meter is assembled by Sandra Mendenhall in San Jose plant. Inset: Completed panel meters being tested.

Lydia Coronel assembles printed circuit boards for Sentry test system. Inset: Completed circuit board.

Applications engineer John Hopp checks Sentry VII test system during assembly. Inset: Close-up view of integrated circuit test head.

TM Trademark of Fairchild Camera and Instrument Corporation

CONSUMER PRODUCTS GROUP

Fairchild's successful entry into the digital watch market in 1975 proved to be a base from which the company was able to launch new consumer electronic products last year. In addition to expanding its watch and clock lines the group announced the first computer-based home television game, which drew nationwide attention. Ground was broken late in the year for a new 150,000-square-foot headquarters building.

Time Products During 1976, Fairchild offered the broadest range of digital watches available in the market, both domestic and international. The Timeband™ line of men's and ladies LED (light emitting diode) watches—priced from $19.95 to $54.95—contributed to digital watch demand early in the year, through mass merchandising outlets. The Fairchild™ series, now retailing from $50 to $195, provided the company with additional timepieces in the more expensive jewelry category. Fairchild also marketed a full line of LED solid-state digital clocks, ranging from table models to a clock/high-intensity lamp.

At mid-year, the company introduced a family of LCD (liquid crystal display) watches, with shipments starting in September. By the end of 1977 it is expected that the LCD, or continuous display, technology may account for as much as half of our watch sales. Throughout the year, the Time Products Service Center steadily improved its performance and turnaround time, and the company embarked on a training program to aid dealers in handling simple service requirements.

Exetron This division continued to be a major producer of CMOS circuits and modules for both LED and LCD watches, and started the industry's first four-inch wafer fabrication facility. Exetron also manufactures the Fairchild Video Entertainment System, a programmable TV game with color and sound. The system incorporates Fairchild's F8 microprocessor and MOS RAMs, and can accept an expanding library of unique Videocart™ plug-in memory cartridges. Games ranging from Hockey to Blackjack to Math Quiz are now on the market, and the company will add new program cartridges during the year.

Optoelectronics Demand for optoelectronics products grew in 1976, despite a slowing of orders for watch displays. Applications for light-emitting diodes expanded into such areas as appliances, TV channel indicators, hi-fi equipment and taxi meters. Fairchild was the only supplier of displays to the two major citizens band radio manufacturers, and the company was selected to produce clock/radio frequency displays for Ford's 1978 car models. The division produced 132 new optical coupler products and announced the stackable digit concept—digits mounted on a printed circuit board. The first Fairchild Solid-State Technology Kits™ for educators and hobbyists were marketed toward the end of 1976.

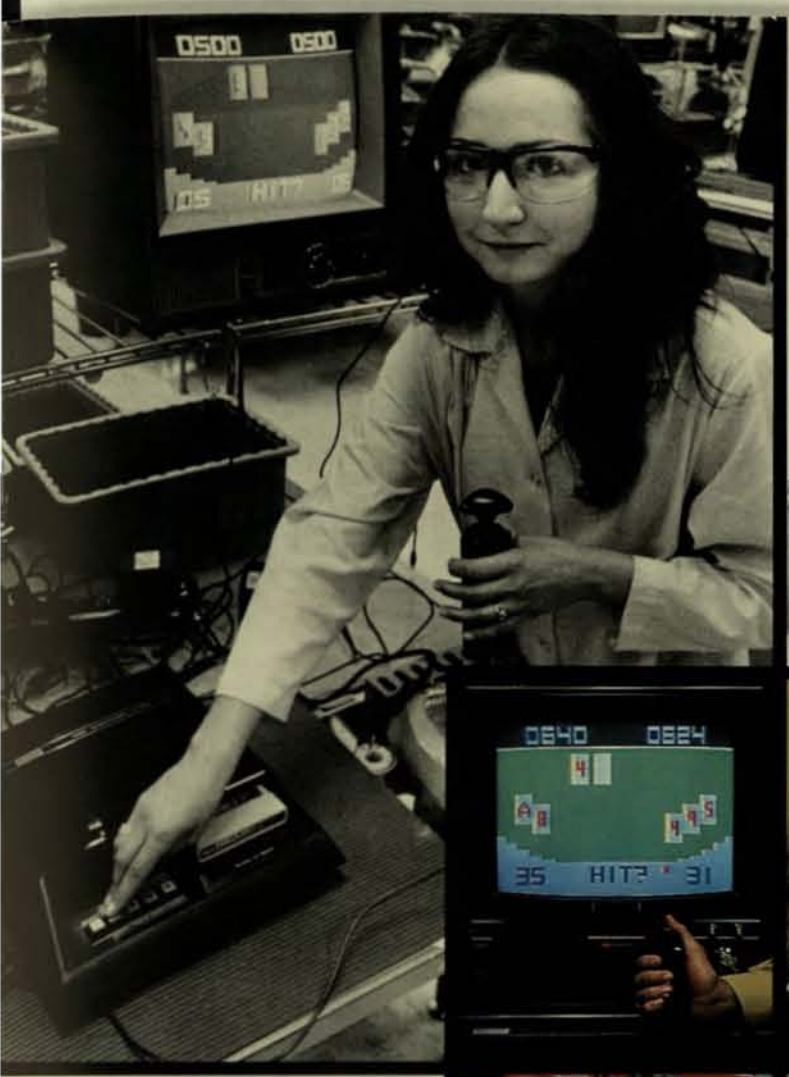
TM Trademark of Fairchild Camera and Instrument Corporation

Angelina Trujillo tests Fairchild Video Entertainment System at Exetron Division. Inset: Blackjack is one of the more popular video games.

Becky Stanton of the Optoelectronics Division prepares machine for packaging of Fairchild Technology Kits. Inset: Various clocks assembled from Technology Kits.

Digital clocks are packaged by Laura Perkinson prior to shipment. Inset: Two new digital clocks announced early in 1977 are the Fairchild Model C-8211 (foreground) and Timeband Model C-6110.

In the watch casing operation in Palo Alto, Linda Carter inspects assembled timepieces. Inset: Model FC 1155 LCD digital watches are new in the Fairchild™ line.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TECHNOLOGY KIT
FAIRCHILD

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FEDERAL SYSTEMS GROUP

During the past year, the Federal Systems Group continued to perform most of its work under government contracts from the military services. A highlight of 1976 was Industrial Research magazine's award for Fairchild's development of the solid-state MV-201 miniature television camera.

Space and Defense Systems In 1976, this division received a sizable contract to continue work on analog/digital converter synchronizer equipment for U.S. Navy electronic countermeasures aircraft. The division also received a major contract to develop self-contained surveillance and tactical communications equipment for the U.S. Army.

Imaging Systems Three new cameras embodying charge-coupled device (CCD) technology were developed in 1976. The first, an electronic gunsight camera, was produced for the Air Force and replaces existing 16 mm film cameras. It will be tested by the Tactical Air Command in 1977. The second, developed for NASA, is compatible with standard 525-line television screen displays and offers the potential for use in commercial broadcasting. A special-purpose TV camera was developed for the U.S. Army to interface with a helicopter-carried tracking sight, permitting an instructor to monitor a gunner's aimpoint during live or simulated missile firings.

A project still in the developmental stage involved mounting a CCD TV camera in an artillery shell which can be fired over a selected area and deployed on a parachute, transmitting terrain and target information to a remote command post.

The KA-99 panoramic aerial camera was developed in 1976 under a U.S. Navy contract. Designed to operate at altitudes ranging from 500 to 12,000 feet, it has been chosen as the prime sensor in a new Navy reconnaissance system. Two contracts for electronic timer systems were received: one, from the U.S. Air Force, for a safety device to be used in a guided weapon program; the second, from the U.S. Army, for an electro-mechanical safety and arming device for the improved Hawk missile.

Art Roberts, a senior staff engineer with the Imaging Systems Division demonstrates the CCD artillery shell television camera. Inset: Soldering operation being performed on the CCD camera.

The Industrial Products Division's Pat Tomasi assembles a Synchromatic 110 filmstrip projector. Inset: Final adjustments on a filmstrip projector are made just prior to shipment.

Leads on a circuit board for an A/D converter are checked by Mavis Catherwood. Inset: A/D converter produced by the Space and Defense Systems Division.

Carl Solomon, optical specialist with the Imaging Systems Division, helps insure that aerial camera lenses meet specifications. Inset: Lens is carefully installed in camera body.

Industrial Products Division

Fairchild audio-visual products introduced in early 1977 include a new generation of Super 8 mm film projection equipment and new 35 mm rear and front screen slide projectors. Sales of the Synchromatic 110 filmstrip projectors advanced during 1976, finding growing customer acceptance both here and abroad. Airline use of our STAN™ integral weight and balance systems increased, particularly in overseas markets. Fairchild voice and flight data recorders maintained their leadership in the field of aircraft recording equipment.

TM Trademark of Fairchild Camera and Instrument Corporation

FIVE YEAR SUMMARY OF OPERATIONS AND FINANCIAL REVIEW

	1976	1975	1974	1973*	1972*
Progress in Operations (in thousands, except per share data)					
Net sales	$443,221	$291,542	$384,933	$351,171	$223,896
Royalties and other income	7,157	8,188	10,619	10,397	6,329
	450,378	299,730	395,552	361,568	230,225
Cost of sales	327,381	208,712	264,194	245,450	165,794
Administrative and selling expenses	94,427	69,732	75,882	61,975	47,888
Interest expense	5,504	4,154	3,868	4,176	4,252
	427,312	282,598	343,944	311,601	217,934
Income before income taxes, extraordinary credit and cumulative effect of change in accounting method	23,066	17,132	51,608	49,967	12,291
Provision for income taxes	10,610	6,708	24,576	23,649	4,956
Income before extraordinary credit and cumulative effect of change in accounting method	12,456	10,424	27,032	26,318	7,335
Extraordinary credit (2)	—	—	—	14,506	3,176
Cumulative effect on prior years (to December 29, 1974) of change in accounting method (1)	—	2,649	—	—	—
Net income	$ 12,456	$ 13,073	$ 27,032	$ 40,824	$ 10,511
Per share of common stock:					
Income before extraordinary credit and change in accounting method	$ 2.27	$ 1.94	$ 5.17	$ 5.04	$ 1.51
Extraordinary credit (2)	—	—	—	2.77	.65
Cumulative effect of change in accounting method (1)	—	.51	—	—	—
Net income	$ 2.27	$ 2.45	$ 5.17	$ 7.81	$ 2.16
Per share of common stock assuming full dilution:					
Income before extraordinary credit and change in accounting method	$ 2.27	$ 1.94	$ 5.00	$ 4.86	—
Extraordinary credit (2)	—	—	—	2.59	—
Cumulative effect of change in accounting method (1)	—	.47	—	—	—
Net income	$ 2.27	$ 2.41	$ 5.00	$ 7.45	—
Shares of common stock used to compute primary income per share	5,476,865	5,372,901	5,228,523	5,224,826	4,877,184
Cash dividends per share	$ .80	$ .80	$ .75	$ .30	—

**Restated—see Note 3 of the Notes to Consolidated Financial Statements.*

(1) In 1974 and 1975, the Company adopted improvements in its inventory costing method. The effect of these changes in inventory costing was not material to income before extraordinary credit and cumulative effect of accounting change for any period presented.

(2) Represents income tax reductions resulting from carryforward of prior years' operating losses.

NOTE—See "Management's Discussion and Analysis of the Summary of Operations," on pages 20 to 22.

	1976	1975	1974	1973	1972
Selected Operating Data (in thousands)					
Net sales by line of business:					
Electronic components and systems	$400,765	$256,378	$344,790	$301,091	$178,890
Other products—principally government	42,456	35,164	40,143	50,080	45,006
Income before income taxes, extraordinary credit and change in accounting method by lines of business:					
Electronic components and systems	17,306	13,041	46,909	45,406*	10,738*
Other products—principally government	5,760	4,091	4,699	4,561*	1,553*
Net sales of solid state devices	298,187	226,036	321,548	281,370	161,714
International sales	138,466	82,732	113,574	87,730	42,919
Royalty income	6,373	4,766	7,312	7,467	6,037
Research, development and engineering (1)	46,939	37,550	40,288	38,251	29,287
Depreciation and amortization	16,663	15,890	14,092	12,039	10,368
Capital expenditures	36,076	20,693	41,342	34,558	11,218
Financial Position at Year End (in thousands)					
Cash and temporary cash investments	$ 26,898	$ 25,194	$ 33,392	$ 34,272	$ 25,535
Short-term borrowings	13,618	9,455	6,819	7,265	9,525
Working capital	113,865	100,506*	93,892*	90,809*	68,692*
Property, plant and equipment, net	130,404	112,256	108,847	88,040	66,044
Long-term debt, including current portion	68,088	46,825	49,592	51,674	57,199
Shareholders' equity	177,609	166,329*	153,875*	128,692*	81,511*
Statistics and Key Ratios					
Shares issued at year end	5,359,552	5,278,563	5,161,592	5,106,187	4,979,476
Number of shareholders at year end	10,429	11,179	12,325	10,464	11,836
Shareholders' equity per common share at year end	$ 33.14	$ 31.51*	$ 29.81*	$ 25.20*	$ 16.37*
Employees at year end	21,293	17,405	18,092	25,525	18,866
Net sales per employee (based on average number of employees)	$ 22,100	$ 17,660	$ 17,650	$ 15,800	$ 13,200
Backlog of orders at year end (000's)	$147,000	$128,000	$161,000	$265,000	$129,000
Income before extraordinary credit and change in accounting method as a percent of:					
Net sales	2.8%	3.6%	7.0%	7.5%*	3.3%*
Shareholders' equity at year end	7.0%	6.3%*	17.6%*	20.5%*	9.0%*
Current ratio at year end	2.1	2.2*	2.0*	2.1*	2.2*
Long-term debt to total capitalization at year end (2)	28%	22%*	24%*	29%*	41%*

**Restated—see Note 3 of the Notes to Consolidated Financial Statements.*

(1) Stated in accordance with the definition expressed in Summary of Accounting Policies in the consolidated financial statements. Amounts shown include customer reimbursements.

(2) Total capitalization defined as the sum of long-term debt (including current portion) and shareholders' equity.

MANAGEMENT'S DISCUSSION AND ANALYSIS OF THE SUMMARY OF OPERATIONS

Comparison of 1976 with 1975

Net Sales Net sales increased $151,679,000 (52%) to $443,221,000 as compared to 1975 net sales of $291,542,000. Of this increase, approximately half resulted from continued expansion of the digital watch and watch module product lines which were introduced in 1975. The balance of the increase resulted primarily from increased semiconductor product shipments. Demand for semiconductors increased sharply in the first part of the year, slackened at mid-year and expanded slightly during the last quarter.

Royalties and Other Income Royalties and other income combined decreased $1,031,000 (12.6%) to $7,157,000 as compared to 1975 income of $8,188,000. Royalty income from patents related to the process of manufacturing semiconductor devices generally fluctuates in proportion to semiconductor sales. In 1976, royalty income increased $1,607,000 (34%) to $6,373,000. However, this increase was offset by a $2,638,000 reduction in interest and other income.

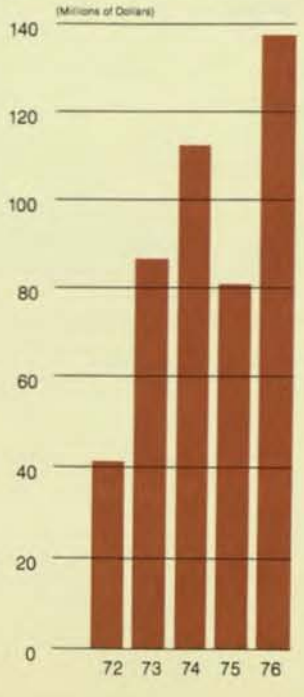
Cost of Sales Cost of sales increased $118,669,000 (56.9%) to $327,381,000 as compared to 1975 cost of sales of $208,712,000. Most of this increase is attributable to the higher sales discussed above. As a percent of net sales, cost of sales increased slightly (2.3%). This slight increase reflects the residual effects of the 1975 recession which continued to depress prices for commodity-type semiconductor components during the first half of 1976.

Administrative and Selling Expenses Administrative and selling expenses increased $24,695,000 (35.4%) to $94,427,000 compared to 1975 expenses of $69,732,000. The increase is primarily attributable to the higher volume of activity in the sale of semiconductor components, digital watches and watch modules. Selling expenses rose in proportion to the increased sales volume, where administrative expenses, as a percent of net sales, declined reflecting the fixed nature of certain of these expenses. Administrative and selling expenses in total, as a percent of net sales, dropped from 23.9% to 21.3% in 1976.

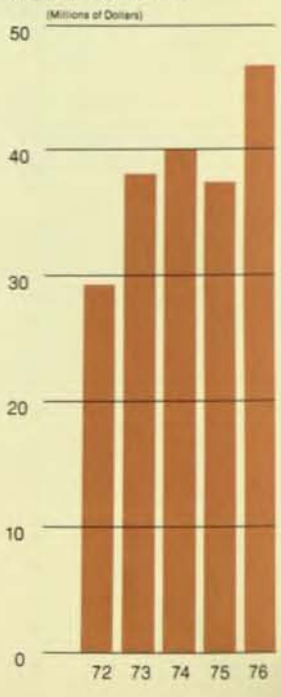
Interest Expense Interest expense increased $1,350,000 (32.5%) to $5,504,000 as compared to 1975 interest expense of $4,154,000, due to a substantial increase in average borrowings partially offset by a reduction in the average interest rate.

Provision for Income Taxes The provision for income taxes increased $3,902,000 (58.2%) to $10,610,000

INTERNATIONAL SALES



RESEARCH, DEVELOPMENT AND ENGINEERING



from the 1975 provision of $6,708,000. This increase is attributable to: (1) the increase in pretax income in 1976; (2) the favorable impact of 1975 net gains of approximately $400,000 from the sale of land and buildings occupied by a foreign subsidiary which were taxed at nominal rates; and (3) the forgiveness in 1975 of taxes of approximately $890,000 on income earned by a foreign subsidiary in a prior year.

Net Income Income before the cumulative effect of a change in accounting increased $2,032,000 ($.33 per share) to $12,456,000 ($2.27 per share) from comparable 1975 income of $10,424,000 ($1.94 per share). Income was depressed during the first half of the year as a result of losses relative to digital medium-scale and small-scale integrated circuits, which came under adverse pricing pressure in mid-1975 and continued into 1976. This unfavorable situation improved during the latter part of the year. Net income for 1975 benefited from the cumulative effect of a change in accounting method amounting to $2,649,000 ($.51 per share).

Comparison of 1975 with 1974

Net sales Net sales declined $93,391,000 (24.3%) to $291,542,000 as compared to 1974 net sales of $384,933,000. This decline in sales reflected a continuation of the worldwide recession in the semiconductor industry which began in the second quarter of 1974 and was aggravated by customer liquidation of inventories. For 1975, the largest sales decline related to digital medium-scale and small-scale integrated circuits, the Company's largest single line of semiconductor devices, for which unit demand fell and prices declined sharply. For 1975, net sales included approximately $12.5 million attributable to digital watches and watch modules, which were first sold in the third quarter of 1975.

Cost of Sales Cost of sales declined $55,482,000 (21.0%) to $208,712,000 as compared to 1974 cost of sales of $264,194,000. During 1975 cost of sales declined along with the sales decline. Even though the Company reacted promptly to the sales decline, production capacity could not be fully utilized, resulting in a smaller percentage decline in cost of sales as compared to sales. Despite the improved sales level in the latter part of 1975, the cost of sales remained proportionately higher because of continued pricing pressure on commodity type components and yield problems in the manufacture of certain semiconductor devices. As a result of the foregoing factors, cost of sales, as a percent of net sales, increased 3.0% in 1975.

Administrative and Selling Expenses
Administrative and selling expenses declined $6,150,000 (8.1%) to $69,732,000 as compared to

1974 expenses of $75,882,000. As a percent of net sales, however, administrative and selling expenses increased from 19.7% to 23.9%. This percentage increase was substantially attributable to the non-variable elements of such expenses. In addition, 1975 marked the Company's entry into the consumer market with the Fairchild line of digital watches, which required introductory promotional expenditures. The Company also temporarily increased marketing costs by adding independent sales representatives to its field organization in an effort to increase market penetration.

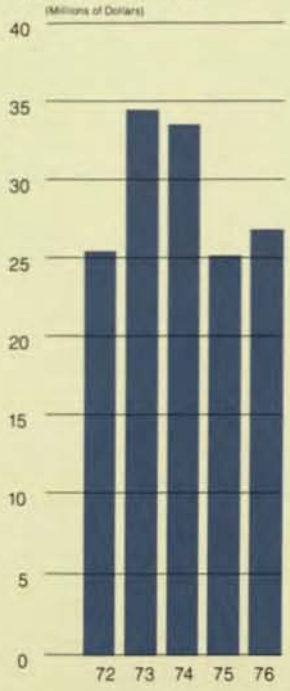
Provision for Income Taxes The provision for income taxes decreased $17,868,000 (72.7%) to $6,708,000 as compared to the 1974 provision for taxes of $24,576,000. This decrease resulted from the decline in sales and net income as well as a reduction in the effective tax rate to 39.2% from the 1974 effective tax rate of 47.6%. The decrease in the effective tax rate reflected the inclusion of credits in the 1975 tax provision related to the tax benefit of a foreign subsidiary's operating loss and forgiveness of taxes on income earned by a foreign subsidiary in a prior year.

Net Income During 1975, the decline in net income was attributable almost entirely to a sharp industry-wide drop in sales, coupled with price reductions, in the Electronic Components and Systems line of business. In particular, sales of digital medium-scale and small-scale integrated circuits (the most profitable products in 1974) resulted in a loss in 1975. In addition, problems encountered in the manufacture of certain memory components in the fourth quarter of 1975 resulted in increased units costs (as a consequence of reduced yields) which almost eliminated any profit contribution for the year for such components. The decline in semiconductor components' profitability did not affect all types of devices and was partially offset by the profitable results of digital watch operations. Income before the cumulative effect of a change in accounting method decreased $16,608,000 ($3.23 per share) to $10,424,000 ($1.94 per share) as compared with comparable income in 1974 of $27,032,000 ($5.17 per share) as a result of factors set forth above. In addition, 1975 net income was increased by the cumulative effect of a change in accounting method amounting to $2,649,000 ($.51 per share).

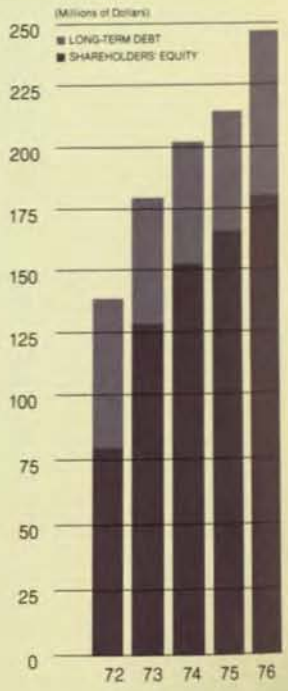
FINANCIAL POSITION

Throughout 1976 and 1975, the Company maintained a strong financial position. Cash and temporary investments at year end 1976 were $26.9 million compared

CASH AND TEMPORARY CASH INVESTMENTS



TOTAL CAPITALIZATION



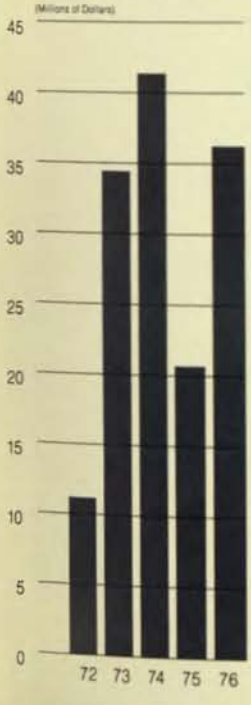
with $25.2 million in 1975. Short-term bank borrowings, the Company's only short-term debt, increased $4.2 million to $13.6 million. At year end 1976, working capital remained strong at $114 million and the current ratio was 2.1:1 compared to $101 million and 2.2:1 in 1975.

Inventories at year end 1976 of $96.5 million increased $3.5 million (4%) over year end 1975, despite a 52 percent increase in sales. Accounts and notes receivable increased $25.6 million at year end 1976 to $82.2 million as a result of the increase in sales.

Net investment in property, plant and equipment increased $18.1 million to $130.4 million in 1976. Capital expenditures were $36.1 million in 1976 as the Company expanded production facilities in anticipation of future sales increases.

Long-term debt increased $21.3 million as a foreign finance subsidiary of the Company issued debentures of $20 million to generate additional capital for future growth. Long-term debt, including the current portion, was 28 percent of total capitalization at year end 1976, an increase of 6 percent over the prior year. Shareholders' equity increased to $178 million, or $33.14 per share, from $166 million, or $31.51 per share, in 1975. Dividends of $.80 per share were paid in both 1976 and 1975.

CAPITAL EXPENDITURES



Despite the lag in the economic recovery, the Company continues to invest significantly in advanced technology and product development programs. Total spending for research, development and engineering was $47 million in 1976 compared to $38 million in 1975. Reimbursements from customers totaled $4.0 million in 1976 compared to $3.3 million in 1975.

COMMON STOCK PRICE AND DIVIDENDS

The Company's common stock is traded on the New York, Pacific and Mid-West Stock Exchanges; Symbol-FCI. The price range of its common stock and dividends per share during 1975 and 1976 were as follows:

	Price Range of Common Stock		Dividends Per Share
	High	Low	
1975			
First quarter	$38¼	$17	$.20
Second quarter	62¼	36	.20
Third quarter	61¾	42¼	.20
Fourth quarter	53¼	31⅛	.20
1976			
First quarter	53¾	36⅝	.20
Second quarter	51⅝	36⅛	.20
Third quarter	55¼	44	.20
Fourth quarter	51¾	36	.20

Fairchild Camera and Instrument Corporation and Subsidiaries

CONSOLIDATED BALANCE SHEET

Assets	January 2, 1977	December 28, 1975*
Current assets:		
Cash	$ 14,606,000	$ 12,526,000
Temporary cash investments (interest-bearing) at cost, which approximates market	12,292,000	12,668,000
Accounts and notes receivable, less allowance for doubtful accounts of $2,766,000 and $2,657,000	82,230,000	56,645,000
Inventories (Note 2):		
Raw materials and parts	21,857,000	17,022,000
Work-in-process, less progress payments of $5,130,000 and $3,069,000	46,773,000	45,736,000
Finished goods	27,901,000	30,268,000
Accumulated income tax prepayments (Notes 3 and 4)	6,906,000	10,893,000
Prepaid expenses and other current assets	3,669,000	1,806,000
Total current assets	216,234,000	187,564,000
Investment in joint ventures (Note 9)	2,881,000	2,534,000
Property, plant and equipment, at cost (Note 5):		
Land	4,159,000	4,199,000
Buildings and improvements	78,764,000	66,597,000
Machinery and equipment	104,864,000	94,505,000
	187,787,000	165,301,000
Less accumulated depreciation and amortization	57,383,000	53,045,000
Net property, plant and equipment	130,404,000	112,256,000
Other assets	2,567,000	1,366,000
	$352,086,000	$303,720,000

**Restated – see Note 3.*

The accompanying summary of accounting policies and notes to consolidated financial statements are an integral part of these statements.

Liabilities and Shareholders' Equity	January 2, 1977	December 28, 1975*
Current liabilities:		
Notes payable to banks (Note 5)	$ 13,618,000	$ 9,455,000
Current installments of long-term debt (Note 5)	3,030,000	2,318,000
Accounts payable	23,905,000	18,742,000
Accrued compensation and employee benefits (Note 6)	13,559,000	11,017,000
Other accrued liabilities	27,215,000	26,721,000
Estimated income taxes payable (Notes 3 and 4)	21,042,000	18,805,000
Total current liabilities	102,369,000	87,058,000
Long-term employee benefits	2,914,000	2,607,000
Deferred income taxes (Notes 3 and 4)	4,136,000	3,219,000
Long-term debt, less current installments (Note 5):		
Other secured loans	8,233,000	5,932,000
Note payable to insurance company	11,250,000	13,000,000
Convertible subordinated debentures	45,575,000	25,575,000
Total long-term debt	65,058,000	44,507,000
Shareholders' equity (Notes 3, 4, 5, and 7):		
Common stock, $1 par value, authorized 10,000,000 shares; issued 5,359,552 and 5,278,563 shares	5,360,000	5,279,000
Additional paid-in capital	81,316,000	78,308,000
Retained earnings	90,933,000	82,742,000
Total shareholders' equity	177,609,000	166,329,000
Contingencies and commitments (Notes 3, 9, 10, and 11)		
	$352,086,000	$303,720,000

Fairchild Camera and Instrument Corporation and Subsidiaries

CONSOLIDATED STATEMENT OF INCOME

	Year Ended	
	January 2, 1977	December 28, 1975
Revenues:		
Net sales	$443,221,000	$291,542,000
Royalties and other income	7,157,000	8,188,000
	450,378,000	299,730,000
Costs and expenses:		
Cost of sales	327,381,000	208,712,000
Administrative and selling	94,427,000	69,732,000
Interest	5,504,000	4,154,000
	427,312,000	282,598,000
Income before income taxes and cumulative effect of change in accounting method	23,066,000	17,132,000
Provision for income taxes (Note 4)	10,610,000	6,708,000
Income before cumulative effect of change in accounting method	12,456,000	10,424,000
Cumulative effect on prior years (to December 29, 1974) of change in accounting method (Note 2)	–	2,649,000
Net income	$ 12,456,000	$ 13,073,000
Per share of common stock (Notes 2 and 8):		
Income before cumulative effect of change in accounting method	$2.27	$1.94
Cumulative effect of change in accounting method	–	.51
Net income	$2.27	$2.45
Per share of common stock assuming full dilution (Notes 2 and 8):		
Income before cumulative effect of change in accounting method	$2.27	$1.94
Cumulative effect of change in accounting method	–	.47
Net income	$2.27	$2.41

The accompanying summary of accounting policies and notes to consolidated financial statements are an integral part of these statements.

Fairchild Camera and Instrument Corporation and Subsidiaries

CONSOLIDATED STATEMENT OF SHAREHOLDERS' EQUITY

	Common Stock		Additional Paid-In Capital	Retained Earnings
	Shares	Amount		
Balance, December 29, 1974 as previously reported	5,161,592	$5,162,000	$74,868,000	$79,360,000
Restatement (Note 3)	–	–	–	(5,515,000)
Balance, December 29, 1974 as restated	5,161,592	5,162,000	74,868,000	73,845,000
Net income – 1975	–	–	–	13,073,000
Sales of common stock under employee stock option plan	110,302	110,000	2,531,000	–
Conversion of convertible subordinated debentures (Note 5)	6,669	7,000	519,000	–
Tax benefit related to employees' premature disposition of option shares and exercise of nonqualified stock options (Note 4)	–	–	390,000	–
Cash dividends – $.80 per share	–	–	–	(4,176,000)
Balance, December 28, 1975	5,278,563	5,279,000	78,308,000	82,742,000
Net income – 1976	–	–	–	12,456,000
Sales of common stock under employee stock option plan	80,989	81,000	2,013,000	–
Tax benefit related to employees' premature disposition of option shares and exercise of nonqualified stock options (Note 4)	–	–	995,000	–
Cash dividends – $.80 per share	–	–	–	(4,265,000)
Balance, January 2, 1977	5,359,552	$5,360,000	$81,316,000	$90,933,000

At January 2, 1977, 1,446,283 shares of unissued common stock are reserved for conversion of convertible subordinated debentures and exercise of employee stock options. See Notes 5 and 7.

The accompanying summary of accounting policies and notes to consolidated financial statements are an integral part of these statements.

Fairchild Camera and Instrument Corporation and Subsidiaries

CONSOLIDATED STATEMENT OF CHANGES IN FINANCIAL POSITION

	Year Ended	
	January 2, 1977	December 28, 1975
Financial resources were provided by:		
Operations:		
Income before cumulative effect of change in accounting method	$12,456,000	$10,424,000
Charges (credits) to income not affecting working capital:		
Depreciation and amortization	16,663,000	15,890,000
Deferred income taxes	917,000	2,211,000
Provision for employee benefits	307,000	(1,034,000)
Gain on disposition of property, plant and equipment, net of income tax	(134,000)	(441,000)
	30,209,000	27,050,000
Cumulative effect on prior years (to December 29, 1974) of change in accounting method	–	2,649,000
Financial resources provided by operations	30,209,000	29,699,000
Increase in common stock and additional paid-in capital:		
Exercise of stock options	2,094,000	2,641,000
Tax benefits relating to stock options	995,000	390,000
Conversion of subordinated debentures	–	526,000
Proceeds from disposition of property, plant and equipment, net of income tax	1,399,000	1,835,000
Proceeds from long-term borrowings	22,699,000	553,000
Total financial resources provided	57,396,000	35,644,000
Financial resources were applied to:		
Expenditures for property, plant, and equipment	36,076,000	20,693,000
Cash dividends	4,265,000	4,176,000
Reduction of long-term debt, including $526,000 on conversion of subordinated debentures into common stock in 1975	3,193,000	3,106,000
Investment in joint ventures	347,000	641,000
Other	156,000	414,000
Total financial resources applied	44,037,000	29,030,000
Increase in working capital	$13,359,000	$ 6,614,000

The accompanying summary of accounting policies and notes to consolidated financial statements are an integral part of these statements.

Fairchild Camera and Instrument Corporation and Subsidiaries

CHANGES IN ELEMENTS OF WORKING CAPITAL

	Year Ended	
	January 2, 1977	December 28, 1975
Changes in elements of working capital:		
Current assets—increase (decrease):		
Cash and temporary cash investments	$ 1,704,000	$ (8,198,000)
Accounts and notes receivable	25,585,000	(12,312,000)
Inventories	3,505,000	19,642,000
Accumulated income tax prepayments	(3,987,000)	151,000
Prepaid expenses and other current assets	1,863,000	(62,000)
	28,670,000	(779,000)
Current liabilities—(increase) decrease:		
Notes payable to banks	(4,163,000)	(2,636,000)
Current installments of long-term debt	(712,000)	214,000
Accounts payable	(5,163,000)	(2,083,000)
Accruals—compensation, employee benefits and other	(3,036,000)	1,587,000
Estimated income taxes payable	(2,237,000)	10,311,000
	(15,311,000)	7,393,000
Increase in working capital	$13,359,000	$ 6,614,000

Accounting policies of the Company and its subsidiaries conform with generally accepted accounting principles and reflect practices appropriate to the industries in which they operate. The significant policies are summarized below.

Fiscal Year The Company's fiscal year ends on the Sunday nearest to December 31. Fiscal year 1976 ended January 2, 1977 and comprised 53 weeks; fiscal year 1975 ended December 28, 1975 and comprised 52 weeks.

Principles of Consolidation The consolidated financial statements include the accounts of the Company and all of its domestic and foreign subsidiaries. The investment in joint ventures is carried in the consolidated financial statements at the Company's equity in the ventures' net assets.

Translation of Foreign Currencies The asset and liability accounts of foreign subsidiaries are translated into United States dollar equivalents at year-end rates of exchange, except for inventories and property, plant and equipment which are translated at historical rates. The income statement accounts of foreign subsidiaries are translated into United States dollar equivalents using average rates of exchange in effect during the year, except that cost of sales and depreciation are translated at historical rates. Exchange adjustments, including those resulting from performed and unperformed forward exchange contracts, are included in the results of operations.

Inventories Inventories are stated at the lower of cost or market. The major portion of the Company's inventories is based on standard costs, adjusted as required to reflect approximate actual costs; other inventories are based on average costs. Quantities in excess of estimated requirements are not valued. Progress payments received on contracts as to which title to the related inventories vests in the United States government are deducted from the applicable inventories. During 1975, the Company changed its method of accumulating manufacturing overhead in inventory. See Note 2.

Property, Plant and Equipment Expenditures for property, plant and equipment and for renewals and betterments which extend the originally estimated economic life of assets or convert the assets to a new use are capitalized. Expenditures for maintenance, repairs and other renewals of assets are charged to operations. When assets become fully depreciated or are disposed of, the cost and accumulated depreciation are removed from the accounts and any gain or loss is included in the results of operations.

Provisions for depreciation and amortization are made using the straight-line method for the major portion of assets acquired after 1968 and for all assets acquired prior to 1954; the sum-of-the-years'-digits method is used for the remaining assets. Depreciation is computed using various estimated economic lives ranging from 20 to 60 years (principally 40 years) for buildings and from 3 to 15 years (principally 6 and 7 years) for machinery and equipment. Leasehold improvements are amortized over the remaining terms of the leases or the estimated economic lives of the improvements, whichever is shorter.

Contracts Revenue on fixed price contracts is recorded at the time deliveries or acceptances are made and the Company has the contractual right to bill. Revenue under cost reimbursement contracts is recorded as cost is incurred in accordance with contractual terms. Provisions are made on a current basis to fully recognize any estimated losses on contracts.

Royalty Income The Company owns certain patents relating to the process of manufacturing semiconductor devices. Licenses to use these patented processes and other technical knowledge of the Company have been granted to a number of companies. Royalty income is based upon either a percentage of sales of licensed products or a fixed schedule of payments. Royalties are included in income in the period that payments are scheduled to be received.

Research and Development The Company is actively engaged in basic technology and applied research and development programs which are designed to develop new or improved products, processes and applications. In 1976 and 1975, the costs of the research and development programs were approximately $22,000,000 and $21,000,000, respectively. In addition, substantial ongoing support programs relating to existing products and processes are conducted within production engineering departments. The combined costs of research, development and engineering programs were approximately $47,000,000 and $38,000,000 (before re-

imbursements of approximately $4,000,000 and $3,000,000) in 1976 and 1975, respectively. Research, development and engineering expenditures are charged to operations as incurred and are included in cost of sales in the consolidated statement of income.

Pension Plans The Company maintains pension plans for domestic employees. Costs and funding requirements of such plans are determined in accordance with actuarial methods and the costs applicable to past service at the time of adoption or modification of the plans are amortized generally over twenty-five years. The plans are funded and deposits are maintained by trustees.

Income Taxes Investment tax credits are applied to reduce Federal income tax expense by the amount allowable each year.

No provision is made for income taxes relating to potential future distributions of accumulated earnings from foreign subsidiaries, the joint ventures or the Domestic International Sales Corporations, since it is the Company's present intention to utilize substantially all of the undistributed earnings in its foreign operations and qualified export activities.

NOTES TO CONSOLIDATED FINANCIAL STATEMENTS

1. Foreign Operations: The following is a summary of certain combined financial information for the Company's foreign operations:

	January 2, 1977	December 28, 1975
Working capital	$51,495,000	$47,617,000
Net assets	55,700,000	68,816,000
Undistributed earnings	49,790,000	45,118,000

Operations of the foreign joint venture were not material in relation to the consolidated financial statements. Net exchange adjustments, included in the determination of net income for 1976 and 1975, were not material to the consolidated statement of income.

2. Accounting Change: During 1975, the Company made improvements in its method of inventory costing. As a result, the overhead content of inventory was increased to include certain elements of manufacturing overhead (primarily depreciation) which had been excluded from inventory. In the opinion of Management, this accounting change represents adoption of a preferable accounting method and also complies with the Internal Revenue Service inventory costing regulations.

The cumulative effect of the accounting change, as of the beginning of 1975, in the amount of $2,649,000 ($.51 per share) after related income taxes of $2,117,000, is included in income for the year. The effect of the accounting change on 1975 income before cumulative effect of change in accounting method was not material.

3. Federal Income Tax Assessment: In July 1976, the Company reached agreement with an Appellate Conferee of the Internal Revenue Service regarding adjustments which resulted from their examination of the Company's Federal income tax returns for the years 1964 through 1971. Accordingly, retained earnings as of December 29, 1974 have been reduced by $5,515,000. The restatement of retained earnings includes nonrecoverable Federal taxes and interest (net of tax effect) for the years 1964 through 1971, related provisions for additional state taxes (net of Federal tax effect) and additional Federal taxes arising from repatriation of funds from a foreign subsidiary as a result of the agreement. Also, accumulated income tax prepayments, other accrued liabilities, estimated income taxes payable and deferred income taxes have been restated as of December 28, 1975 in the consolidated balance sheet.

The Company's Federal income tax returns for years after 1971 were prepared on bases substantially consistent with those of prior years, and the returns for 1972 and 1973 are currently being examined. In the opinion of Management, any additional provisions that might be required as a result of the examination of tax returns for years subsequent to 1971 will not be material to the Company's consolidated statement of income.

On February 18, 1977, the Company was notified that the agreement with the Appellate Conferee, referred to above, received approval by the Joint Committee on Internal Revenue Taxation. The settlement negotiated with the Conferee has therefore become final.

4. Provision For Income Taxes: The provision for income taxes is comprised of the following:

		1976	1975
Current	– Federal	$ 1,985,000	$ 3,930,000
	– State	1,103,000	472,000
	– Foreign	4,434,000	1,318,000
Deferred	– Federal	2,604,000	2,311,000
	– State	512,000	549,000
	– Foreign	(28,000)	(1,872,000)
		$10,610,000	$ 6,708,000

The 1975 deferred provision for income taxes includes the tax benefit of a foreign subsidiary's operating loss of approximately $2,100,000 which was included in accumulated income tax prepayments in the consolidated balance sheet. In 1976, the foreign subsidiary's operating loss was utilized and the related tax benefit was credited to accumulated income tax prepayments. The 1975 current provision for income taxes includes a credit of approximately $890,000 related to forgiveness of taxes on income earned by a foreign subsidiary in a prior year. In addition, the provision for income taxes for 1976 and 1975 reflects utilization of investment tax credits of approximately $1,300,000 and $950,000, respectively.

Differences between financial and taxable income result primarily from exercise of nonqualified stock options, use of accelerated depreciation and financial statement provisions which are not currently tax deductible. In addition, portions of the taxes related to the inventory accounting change, referred to in Note 2 above, are payable in future periods. The tax effect of deductions applicable to employee exercises of nonqualified stock options and premature dispositions by employees of option shares resulted in tax benefits of approximately $995,000 in 1976 and $390,000 in 1975, which was credited to additional paid-in capital.

5. Long-Term Debt and Notes Payable to Banks: In September 1976, the Company replaced the $50 million international and domestic revolving credit agreement in effect at December 28, 1975 with the following bank credit agreements:

(a) a two-year, $50 million domestic revolving credit agreement which provides for advances at the agent bank's prime rate. The Company is required to pay an annual commitment fee of ½ of 1% of the unused commitment. The Company may, at its option, convert to five-year term debt any advances outstanding at the termination of the revolving credit agreement in September 1978.

(b) Fairchild Consumer Products, Inc., a wholly-owned finance subsidiary of the Company, entered into an agreement with several banks for a one-year credit line in an amount up to the lesser of $20 million or 80% of the accounts receivable generated by the Company's consumer products group and sold to the finance subsidiary. This Agreement provides for short-term advances at the agent bank's prime rate, secured by such accounts receivable.

(c) The Company also has arrangements with several banks under which short-term, multi-currency borrowings may be available to the Company and its foreign subsidiaries. These borrowings are limited to an aggregate of $30 million by the agreement described in (a) above.

At January 2, 1977, no borrowings were outstanding under the agreements described in (a) and (b) above.

At January 2, 1977, notes payable to banks of $13,618,000 were outstanding at a weighted average interest rate of 19.5%, principally related to foreign borrowings. The maximum amount of short-term borrowings outstanding at any month end during 1976 was $27,116,000. The approximate monthly average short-term borrowings during 1976 were $20,469,000 at a weighted average interest rate of 12.1%.

Other secured loans bear interest at a weighted average rate of 7¼% and are repayable in varying installments of principal and interest. These loans are secured by liens and mortgages on property, plant and equipment with an approximate net book value of $8,016,000.

The note payable to an insurance company bears interest at 5½% per annum and requires annual principal payments of $1,750,000 from 1977 to 1979 and a final payment of $7,750,000 in 1980.

The Company's 5¾% convertible subordinated debentures of $25,575,000 are convertible into common stock at the rate of $76.11 per share at any time until their maturity in 1989. No conversions were executed in 1976. During 1975, the Company issued 6,669 shares of previously unissued common stock in connection with conversion of debentures having

$526,000 principal amount. The Company has reserved 336,027 shares for future conversion of these debentures. Commencing in 1979, the Company will be required to redeem 6% of the outstanding principal balance annually. At its option, the Company may redeem all or any part of the debentures at premiums decreasing from 2¾% in 1977 to zero in 1986.

In December 1976, Fairchild Camera and Instrument International Finance N.V. (Fairchild N.V.), a newly formed, wholly-owned foreign finance subsidiary of the Company, sold to foreign investors $20,000,000 of 5¾% convertible subordinated guaranteed debentures due 1991. The debentures are guaranteed by the Company on a subordinated basis and are convertible on or after August 1, 1977 into common stock of the Company at a conversion price of $45.50 per share. The Company has reserved 439,560 shares for future conversion of these debentures. At its option subject to certain conditions, Fairchild N.V. may redeem all or any part of the debentures at premiums decreasing from 4½% in 1978 to zero in 1987.

Under the most restrictive provisions of the loan and bank credit agreements, the Company is required to maintain specified working capital and net worth levels, is restricted as to borrowing under any new debt agreements and purchasing its stock, and is limited as to the maximum amounts of cash dividends which may be paid. At January 2, 1977, the Company was in compliance with all restrictive covenants of the loan and bank credit agreements and approximately $22,500,000 of retained earnings was unrestricted for payment of cash dividends.

Aggregate principal payments on long-term debt in each of the next five years are approximately as follows: 1977–$3,030,000; 1978–$3,017,000; 1979–$4,353,000; 1980–$10,364,000; 1981–$2,511,000.

6. Pension and Profit Sharing Plans: Pension expense charged against operations was $1,768,000 in 1976 and $1,321,000 in 1975. As a result of the Pension Reform Act of 1974, the Company amended the benefit formula, vesting and eligibility provisions of its pension plans as of the beginning of 1976. The effect of these amendments was to increase pension expense by approximately $400,000 in 1976. The pension fund assets and balance sheet accruals exceed the actuarially computed value of vested benefits under the plans.

The Company has a qualified, noncontributory profit sharing plan for eligible employees of the Company and participating subsidiaries. The Company's contribution to the plan, as determined by the Board of Directors, is discretionary but may not exceed 15% of the annual aggregate compensation (as defined) paid to all participating employees. In addition, the maximum contribution may not exceed 15% of the amount by which Income Before Income Taxes for the year (as defined) exceeds 10% of Shareholders' Equity (as defined).

The Company also has an incentive compensation plan for awarding bonuses to certain officers and other key employees. The aggregate awards, which may be in cash or common stock, shall not exceed 6% of the amount by which Income Before Income Taxes for the year (as defined) exceeds 10% of Shareholders' Equity (as defined).

Contributions to these plans during 1976 and 1975 were not material to the consolidated statement of income.

7. Stock Options: At January 2, 1977 and December 28, 1975, there were 670,696 and 776,839 shares, respectively, of common stock reserved for issuance under stock option plans (1965 Plan, which terminated as of March 17, 1975, and 1974 Plan) for officers and key employees. Issuance of the following types of options is permitted:

(a) A "qualified" option (as defined in the Internal Revenue Code) exercisable until the fifth anniversary of the grant date;

(b) A "nonqualified" option exercisable until the tenth anniversary of the grant date.

Options may not be granted at prices lower than the market price at the date of issuance and exercisable options expire 90 days after termination of employment. Under the 1974 Plan, options become exercisable in four annual installments commencing one year after the dates of grant. Under the 1965 Plan, through May 1974, options become exercisable in three annual installments commencing two years after the dates of grant; options granted subsequent to May 1974 become exercisable in four annual installments commencing one year after the dates of grant.

During 1975, the shareholders approved a reduction of the option price for all options outstanding under the 1965 Plan. Such approval covered 448,390 shares of common stock purchasable at an average per share price of $34.09. The new option price was $25.38 per share (equal to 100% of fair market price on February 26, 1975) and each option has a new five or ten year term depending upon the type of new option granted. During 1975, 86,070 options were issued in exchange for 114,836 options previously outstanding.

A summary of transactions relating to outstanding options during 1976 and 1975 is shown below:

	1976	1975
Balance, beginning of year	568,089	559,632
Add (Deduct) – Granted	92,805	296,261
– Exercised ($18.38 to $46.13 per share)	(80,989)	(110,302)
– Cancelled	(56,461)	(177,502)
Balance, end of year	523,444	568,089

At January 2, 1977, options were outstanding at prices of $18.31 to $60.88 (an average of $34.24) per share, of which options as to 164,634 shares were exercisable.

8. Income Per Share of Common Stock: Income per share of common stock for 1976 and 1975 has been calculated using the weighted average number of shares of common stock (5,331,127 and 5,222,255, respectively) and common stock equivalents (stock options – 145,738 and 150,646, respectively) outstanding during the year.

Fully diluted income per share of common stock for 1976 and 1975 has been computed based upon the weighted average number of common and common equivalent shares outstanding, and the assumed conversion of the 5¾% convertible subordinated debentures into shares of common stock, after elimination of related interest expense net of taxes.

9. Investment in Joint Ventures: The Company participates with TDK Electronics, Co., Ltd. in a 50-50 corporate joint venture. The venture, TDK-Fairchild Corporation, sells semiconductor products and electronic equipment, parts and components thereof in Japan.

In 1975, the Company invested in a newly-formed corporate joint venture, Great Western Silicon Corporation (Great Western). The venture is 45% owned by the Company and 55% owned by Applied Materials, Inc. (Applied). The venture, whose plant is scheduled for completion in 1978, will manufacture and sell polycrystalline silicon. The Company and Applied have entered into a noncancellable materials purchase agreement with Great Western providing generally that the Company and Applied will purchase 75% and 25%, respectively, of a specified level of production for a period of seven years after production commences. Such purchases are to be at the best price available to such parties from an independent United States source, but in no event at a price less than that which is necessary to provide Great Western with the funds required to pay its manufacturing costs and the cost of debt service and retirement.

In the event Great Western is unable to commence operations or fails to maintain for ninety days delivery of acceptable quantities or quality of silicon, the Company and Applied are obligated to lend to Great Western, in the ratio of their respective equity ownership, amounts sufficient to cover its operating costs and the cost of debt service and retirement. In the event Great Western ceases to deliver specified minimum quantities after commencing operations and maintaining acceptable delivery levels for ninety days, the Company and Applied may be required to provide the funds to cover Great Western's operating costs and the cost of debt service and retirement. Any such payment constitutes an advance payment in the nature of a deposit against future delivery of silicon.

At January 2, 1977, Great Western has a line of credit with a bank for $2,500,000. There are no borrowings outstanding under this line of credit. In addition, arrangements have been made with an insurance company for a long-term construction loan of $7,500,000. Borrowings under this loan agreement amounted to $2,500,000 at January 2, 1977.

10. Customs Matters: As previously reported, the Company is reviewing its practices with respect to compliance with the United States customs laws applicable to products imported into the United States.

The Company has undertaken a review to assure compliance with the highly complex customs laws concerning classification and valuation of imported articles, as well as to determine the propriety and

adequacy of its past practices. Such review includes the classification and valuation, for duty purposes, of a wide variety of items, including semiconductor components partially fabricated in the Company's United States plants and shipped to its Far Eastern plants for labor intensive manufacturing or assembly operations, and then imported into the United States for completion or sale.

In 1973, representatives of the Company initiated contact with the Customs Service and advised it of the Company's voluntary program, and the Company is in the process of submitting to the Service proposals regarding future handling of customs activities and information concerning any past inadequacies discovered in the review. It has also notified the Customs Service that it intends to report to and deposit with the Customs Service amounts found to be owing, if any. In response to requests made, the Company has received several rulings from the Customs Service and is currently engaged in concluding its internal review and preparing the submission of its proposals to the Service.

The Customs Service has statutory authority to collect underpayments of duty and, in some instances, to assess civil penalties based upon the value of the imports involved. Currently, no determination can be made as to whether any penalty assessment will be proposed. Petitions for remission or mitigation are permitted under Customs statutes and regulations, and have been granted to varying degrees in other situations involving electronics companies. After the Company had initiated contact with the Customs Service, in 1974 the Customs Service published its position with respect to voluntary disclosure which provides, in effect, that if the Customs Service determines that a disclosure is made voluntarily any penalty will be mitigated to the amount of any applicable duty underpayment plus a maximum of one times that amount.

It is the Company's position that it voluntarily initiated its pending proceedings with the Customs Service and that, to the extent it may be relevant, it should be considered as having made a voluntary disclosure. There is, however, no assurance that the Company's position will be sustained. The Company intends to pursue this matter diligently so as to minimize the ultimate consequences to the Company. The Company has made provisions in its financial statements for estimated underpayments and penalties, if any, which may result, as well as provisions for other costs being incurred in resolving this matter. In the opinion of Management, any ultimate liability which may result will not have a material effect on the consolidated balance sheet or statement of income of the Company.

11. Contingencies and Commitments: A portion of the Company's sales is subject to renegotiation. Clearances have been received through the year 1974 and no refunds for 1975 and 1976 are anticipated.

The Company leases data processing equipment and various facilities under long-term, noncancellable leases which expire at various dates prior to 1992. Facility leases generally require the Company to maintain the facilities, pay incremental property taxes and provide insurance and utilities. Rent expense under all rental agreements, including the above leases, was $9,520,000 and $7,938,000 in 1976 and 1975, respectively. Minimum annual rentals under long-term, noncancellable leases will be approximately as follows:

Year	Facilities	Equipment
1977	$2,842,000	$1,869,000
1978	2,606,000	1,646,000
1979	2,019,000	1,415,000
1980	1,668,000	1,220,000
1981	1,575,000	905,000
1982-1986	5,759,000	1,297,000
1987-1991	2,805,000	—

Noncapitalized financing leases, as defined by the Securities and Exchange Commission, are not material.

An action against the Company seeking an injunction and damages in an unspecified amount was commenced in December 1975. The plaintiff in its complaint alleges, among other things, that its trade secrets relating to the design of a semiconductor device were improperly obtained and used by the Company. The Company's request for an order dismissing the complaint or alternatively granting summary judgment has been denied. The Company intends to defend this action diligently and, in the opinion of Management, if the Company is ultimately adjudicated to be liable, it will not have a material effect on the consolidated balance sheet of the Company.

12. Selected Quarterly Data (Unaudited): The 1975 interim financial information was not subjected to a

limited review by the Company's independent accountants.

	Net Sales	Gross Profits*	Net Income	Net Income Per Share of Common Stock
1975	(amounts in thousands except per share data)			
First quarter	$ 69,757	$21,070	$3,255**	$.62**
Second quarter	68,964	20,866	3,287	.61
Third quarter	71,453	20,836	2,717	.50
Fourth quarter	81,368	20,058	1,165	.21
1976				
First quarter	94,624	20,762	197	.04
Second quarter	111,753	29,356	2,858	.52
Third quarter	118,157	33,152	4,243	.77
Fourth quarter	118,687	32,570	5,158	.94

Net sales less cost of sales.

***Before cumulative effect of change in accounting method of $2,649,000 ($.51 per share)—see Note 2.*

13. General Description of the Impact of Inflation (Unaudited): Although the cumulative impact of inflation over a number of years has resulted in higher costs for replacement of existing plant and equipment, such inflationary increases have partially been offset by technological improvements and design changes which often result in substantial increases in productivity of the newer asset additions. Generally, the Company's rapid rate of technological advance and the resulting production efficiencies have mitigated unfavorable inflationary pressures.

The Company's annual report on Form 10-K contains specific information with respect to year end 1976 replacement cost of inventories and productive capacity, and the approximate effect which replacement cost would have had on the computation of cost of sales and depreciation expense for the year. To obtain a copy of the Company's Form 10-K, please write to the Corporate Communications Department, Fairchild Camera and Instrument Corporation, 464 Ellis Street, Mountain View, California 94042.

REPORT OF INDEPENDENT ACCOUNTANTS

Price Waterhouse & Co.

To the Shareholders and Board of Directors of Fairchild Camera and Instrument Corporation

We have examined the consolidated balance sheets of Fairchild Camera and Instrument Corporation and its subsidiaries as of January 2, 1977 and December 28, 1975, and the related consolidated statements of income, shareholders' equity and of changes in financial position for the years then ended. Our examinations were made in accordance with generally accepted auditing standards and accordingly included such tests of the accounting records and such other auditing procedures as we considered necessary in the circumstances.

The method of inventory costing was changed in 1975 as described in Note 2 to the consolidated financial statements.

In our opinion, the consolidated financial statements examined by us present fairly the financial position of Fairchild Camera and Instrument Corporation and its subsidiaries at January 2, 1977 and December 28, 1975, and the results of their operations and the changes in their financial position for the years then ended in conformity with generally accepted accounting principles consistently applied during the period subsequent to the change, with which we concur, made as of December 30, 1974, referred to in the preceding paragaraph.

Price Waterhouse & Co.

121 Park Center Plaza
San Jose, California

January 26, 1977 (except as to the last paragraph of Note 3 which is as of February 18, 1977)

DIRECTORS

Roswell L. Gilpatric	Chairman of the Board of the Corporation; Presiding Partner, law firm of Cravath, Swaine & Moore
C. Lester Hogan	Vice Chairman of the Board of the Corporation
Wilfred J. Corrigan	President and Chief Executive Officer
Albert Bowers	President, Syntex Corporation; Vice Chairman of the Board, Syntex Corporation (pharmaceuticals and chemicals)
William C. Franklin	Consultant
Lt. General James B. Lampert (U.S. Army—Retired)	Vice President, Massachusetts Institute of Technology
Louis F. Polk, Jr.	Chairman, President and Chief Executive Officer, Leisure Dynamics, Inc. (hobby and game products)
William A. Stenson	President, Alliance Capital Management Corporation
J. Bradford Wharton, Jr.	Management Consultant; President of the Wealdon Company (a family corporation—investments and farming)

OFFICERS

Wilfred J. Corrigan	President and Chief Executive Officer
Corporate Staff	
Warren J. Bowles	Vice President—Industrial Relations
A. J. Hazle	Vice President—Controller
Frederick M. Hoar	Vice President—Communications
Thomas A. Longo	Vice President—Chief Technical Officer
R. Douglas Norby	Vice President—Finance
Nelson Stone	Vice President—General Counsel and Secretary
James A. Unruh	Vice President—Treasury and Corporate Planning
Operations	
James D. Bowen	Vice President and General Manager—Instrumentation and Systems Group
John A. Duffy, Jr.	Vice President and General Manager—International Division
Raymond G. Hennessey	Vice President and General Manager—Industrial Products Division
David J. Marriott	Vice President and General Manager—Large-Scale Integration Group
Louis H. Pighi	Vice President and General Manager—Federal Systems Group
Gregorio Reyes	Vice President and General Manager—Consumer Products Group
George D. Wells	Vice President and General Manager—Components Group
Joseph H. Akerman, Jr.	Assistant Treasurer
Richard Franklin	Assistant Secretary
John J. Giblin	Assistant Controller
Philip Haas	Assistant Treasurer
Stanley Winston	Assistant Secretary (Attesting)

Independent Accountants	Price Waterhouse & Co.
Transfer Agent	The Bank of New York
Registrar	Citibank, N.A.

Roswell L. Gilpatric has announced that he will retire as Chairman of the Board after the Shareholder's Meeting to be held on May 6, 1977. Mr. Gilpatric is a nominee for re-election as director and will continue as a director of the corporation. The nominees for election to the Board of Directors listed in the Proxy Statement for such Annual Meeting have announced their intention to elect Wilfred J. Corrigan as Chairman of the Board of the Corporation after the meeting.

FAIRCHILD

Fairchild Camera and Instrument Corporation
464 Ellis Street, Mountain View, California 94042
Telephone (415) 962-5011