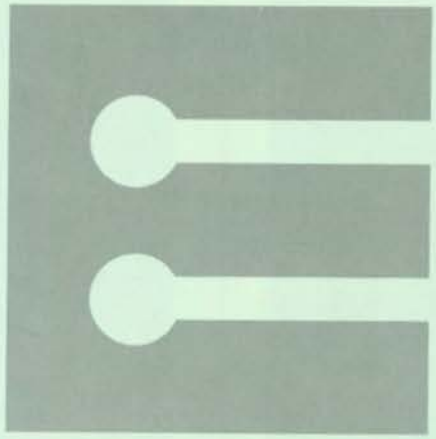
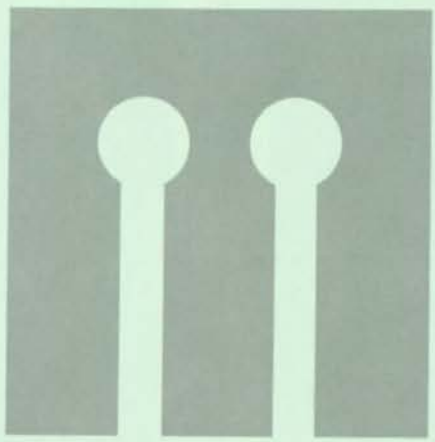


HOW TO SPECIFY A SPECIAL PURPOSE CORE MEMORY SYSTEM



INTRODUCTION

Core memory systems have many applications in digital data handling equipment. The core memory is a highly reliable and versatile instrument, using as its basic storage element a ferrite ring, or core. The cores are threaded by fine wires in such a way as to afford individual selection of any core. Reading or writing at any selected address out of many thousands is thereby achieved in times down to a microsecond or less.

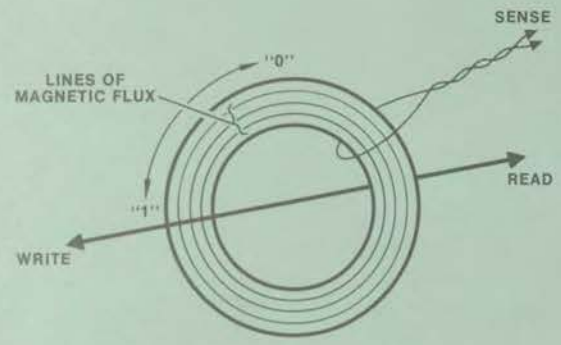


Figure 1a.

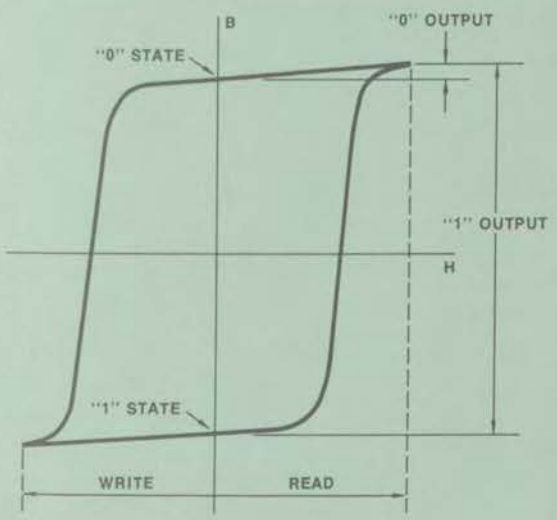


Figure 1b.

The storage element in a core memory is a ferrite ring. It is magnetized in one direction to store a "one," and in the other direction to store a "zero." To read the information out of the core, a current is passed through it to put it into the zero state. If it was already in that state, no magnetic flux would be switched, and no e.m.f. would be observed on another wire (the "sense" line) passing through the core. If it had stored a "one," however, the switched flux would produce an e.m.f. in the sense line which may be amplified to present a logical "one" level at the memory output, (Fig. 1-c). This process, which is necessary in all stores using regular cores, is called destructive read-out. The memory user usually requires the data to be retained in the memory after reading it out, so most core memory systems automatically access the same core a second time with current in the opposite direction, to write in a "one" if a "one" had been read out. The same amplified data that is presented at the output is used to control whether to write back a "one" or a "zero."

The foregoing explanation really says that a "read mode" operation consists of two memory accesses (or half-cycles), "read" and "restore." The analogous "write mode" accesses are called "clear" and "write," because although the same two current pulses are passed in sequence through the core, the first one is used simply to clear the core into the zero state, and the second is used to write in the information presented at the data inputs.

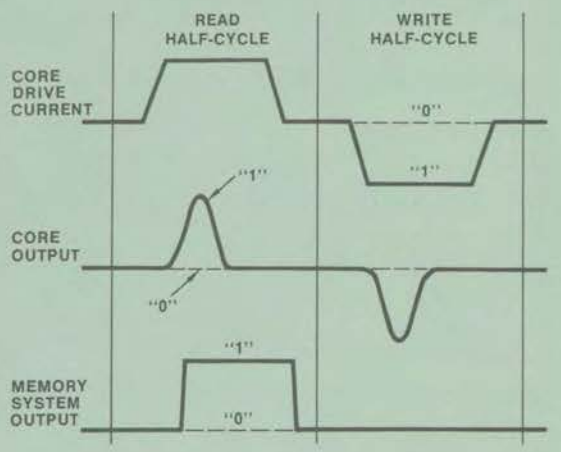


Figure 1c.

A memory system is distinguished from a core array, or stack, by the addition of drive, sense and interface circuits which together make up a memory "black box." The full storage capacity of the core store is accessible on presentation of the appropriate binary levels on a relatively small number of interface lines. Input and output circuits are normally completely compatible with standard integrated logic elements.

This application note gives general information on core memory systems that should be known to anyone contemplating using one, with particular emphasis being given to the practical question of adequately specifying a special purpose system to a prospective vendor. For the assistance of those who do not wish to write a core memory specification from scratch, a form is appended at the end of this note which summarizes the major specifications.

WHAT TO LOOK FOR

Naturally, the most economical way to buy a core memory system is to select an "off-the-shelf" unit, in production, with proven design standards and field reliability data. Thus, the first step in selection of any product is to discuss your requirement with all suitable vendors. Most applications or sales engineers are not only well versed about their own company's products, but they are usually quite familiar with competitive types, and they will quickly be able to analyze your needs and determine whether *any* existing system can meet it.

If a standard memory system is not available to meet your needs, discuss your requirement with the sales engineer in detail and give him a few days to think it over. (Use the form at the end of this paper.) He will come back with suggestions and advice for implementing your particular system and will probably save you money and trouble by applying the experience gained by his association with other customers.

TABLE 1

1. Addressing Mode
2. Capacity
3. Signal Functions
4. Speed
5. Signal Characteristics
6. Power
7. Environmental Requirements
8. RFI Provisions
9. Testing
10. Size and Weight
11. NDRO or DRO
12. Workmanship and Design Standards
13. Quality Control
14. Maintainability
15. Documentation
16. Warranty and Service
17. Price and Delivery

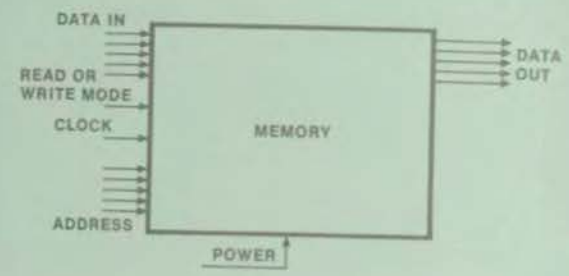
Table 1 lists the principal requirements which should be specified when considering a core memory system. You should have some idea of your requirements for each of these particulars when you shop for a memory.

The following paragraphs discuss each item of Table 1 describing the various possibilities and trade-offs.

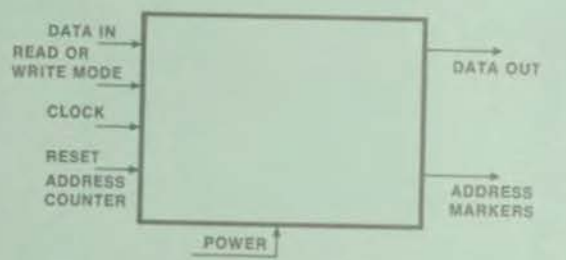
1. ADDRESSING MODE

The usual internal organization of a core memory is such that a number of cores, comprising one memory "word," are accessed in parallel at every memory cycle. This gives an optimum relationship between magnetics cost and electronics cost.

Any one of the total capacity of memory words is equally capable of being accessed and is defined by the address presented to the memory. This organization is known as "random by word, parallel by bit."



(a) Block diagram of a random access parallel-organized memory.



(b) Block diagram of a serial access memory.

Figure 2

All normal applications of memory systems use the random-access parallel memory shown in: (a). In special cases the serial memory (b) may offer advantages.

Other addressing modes are possible. For instance, by giving the memory address circuits a counting capability, a "serial by word, parallel by bit" memory may be obtained. This has the advantage that, once started, it will access successive addresses without requiring them to be explicitly defined at the memory address inputs.

A fully serial memory is often required for data storage and retrieval, where only one information channel is to be processed. This is often the case in spacecraft applications. Such a system may be obtained by applying serial/parallel conversion processes to a parallel-organized memory, but an attractive alternate for low-power, high reliability systems is the use of magnetic switching techniques for accessing the core store. In such memories, ferrite core ring switches or current-steering switches perform the triple functions of address decoding, sequencing, and storing.

Consideration of accessing mode leads into the next parameter to be specified, the capacity of the system.

2. CAPACITY

Specify the required word length in bits (for a bit serial memory, just state the total number of bits) and quantity of words required. Economical word lengths for the average system lie between 16 and 72 bits, with the longer word lengths used where quantity of data handled in a given time is at a premium. Quantity of words is usually an exact 2^n, with "n" ranging roughly between 10 and 16.

If your requirements are not within these limits, don't worry—there are many economical ways of implementing special capacity requirements and your sales engineer contact will undoubtedly suggest some of them.

3. SIGNAL FUNCTIONS

The function of signals to the memory will depend on your particular requirements. Your first discussion with a sales engineer may change your ideas, but the following signals are typical:

A. Data Out. The one function that is common to all memory systems is output of stored data. A serial memory will provide a stream of data on one channel; a parallel memory will put out data on many channels simultaneously.

B. Data In. All memories except those used purely for "fixed" storage require channels for input data, either serial or parallel.

C. Clocks. It is conceivable for a memory to be free running, i.e. to read out stored data continuously without external control. Such a memory would be very difficult to interface with, and all practical core memories in fact operate in response to input "clock" signals. These may be supplied at regular or irregular rates up to the maximum inherent speed of the memory.

D. Modes. If the clock signal is regarded as telling the memory when to perform an operation, the "mode" signal tells the memory what to perform. The two basic modes of memory operation are "read" and "write." Many memory systems have just one mode channel, which is held, say, true for read, and false for write. Another useful mode is "split cycle," which is a combination of the two half-cycles whereby useful information is read out by the first pulse, and new information is stored in the same core by the second pulse. This mode is considerably faster than using a normal two-pulse read operation followed by a normal two-pulse write operation, but extra hardware may be required to implement it. Other "modes" may be devised whereby some specified bits of a parallel word are read-restored while others write new data; or certain address sequences may be accessed in an automatic indirect addressing mode. Such features may be built into a custom memory system and are often offered as options on standard equipment.

E. Addresses. In all random-access memories, the user must define the address he wishes to read out of or write into. These are always defined in binary code on "n" channels for a 2^n word memory.

F. Resets. In serially accessed memories, the user usually requires to start at a known address. Rather than specifying an address on "n" lines as in (e) above, it is often found satisfactory to reset to a predetermined starting point by means of a single signal on one line. This is easy to mechanize in any serial memory. Further reset lines may select other starting points as required.

G. Markers. These are outputs from the memory analogous to resets and may be used instead of or in conjunction with resets. They are again relevant only to serially addressed systems, and indicate on special output channels when particular addresses have been reached.

H. Miscellaneous. At the whim of the specifying activity such signals may be generated by the memory as monitor outputs showing physical or electrical conditions within the memory, or alarm signals showing power failure, illegal input conditions, or overheating. Extra inputs may be conceived to put the memory into self-test modes, or to define various degrees of protection against accidental erasure.

4. SPEED

Speed is expressed in terms of "cycle time," which is the time taken for a read or write mode operation to be completed. Cycle times of 2 μsec are commonplace, and cycle times of less than 1 μsec are available. A parallel memory with long word length naturally allows a large number of bits of data to be processed in one cycle time.

Another speed parameter which may be important is access time, which is the time taken between asking the memory to read out information, and the time the information appears on the output lines. The access time is usually about ¼ to ⅓ of the cycle time.

5. INTERFACE SIGNAL CHARACTERISTICS

Most off-the-shelf memories are designed with regular integrated circuits at the inputs and outputs, typically DTL or TTL. These will interface directly with the user's own logic circuits, provided the noise immunity and loading rules are not violated.

As with interfacing any two digital systems, it is desirable to keep cable capacitance low in order to preserve rise-times (when high speed is required) and to minimize crosstalk and ringing.

Specify that all parameters are to be measured at the memory inputs.

The user must be certain that his system will not introduce noise such as to invalidate his inputs to the memory. If there is any doubt about this, a more elaborate interface must be specified, for instance, a differential receiver at the memory with specified common mode and noise spike rejection characteristics. To reduce cable cross-talk, input and output signals may be filtered. Specify to the memory manufacturer the required maximum frequency content of any such filtered output pulses, and the roll-off above that frequency. This will cost in operating speed, and also price and delivery, but it may make the difference between a smoothly running system and one plagued by trouble.

If you are still worried about interface signal characteristics, you are very wise, and you should read Section (8) on RFI.

6. POWER

Memories work off three (3) or four (4) d-c levels. Usually +5V is required for the integrated circuits and about +15V and −15V to generate drive currents. Required regulation is about ±5%, including ripple. If you have these voltages available, it is as well to supply them to the memory. The memory will be cheaper, and will not have to contain an internal power supply that the memory manufacturer will have to buy outside anyway. If you supply the memory voltages, however, be sure and specify the maximum surge current at turn-on, and the maximum rate of change of current under operating conditions, which the memory may draw. Core memories use short duration current pulses in the order of amperes, which can throw a power supply out of regulation if not sufficiently decoupled. The decoupling itself can cause difficulty, since very large capacitance across the power lines can trouble a power supply at turn-on.

Commercial memory manufacturers usually offer a 110v 60 cps power supply as an option. Special power supplies can of course be made to enable a memory to work off any power source, a.c. or d.c.

Power consumption is generally low, and by special design may be made extremely low. Spacecraft memories, powered by solar cells, run at fractions of a watt, while even the largest ground-based commercial memory is unlikely to take more than a few kilowatts. Consumption is generally proportional to speed and word length.

If you require any data to be retained in the memory while the power is turned off, it is essential to so specify. The core store itself is not dependent on any source of power for data retention. However, it is very difficult to assure that the circuits do not spuriously access the store during turn-off and turn-on, thereby garbling some of the data. It is not sufficient to rely on the results of one test, or to accept a statement that "the circuits are all inhibited." Different sequences of power shut-down may change all that. The memory manufacturer will require an assurance from you that no "clock" signals will be sent to the memory during power turn-off and turn-on, and you may make life easier for him by supplying him with a signal which you guarantee will be true during turn-off and turn-on.

7. ENVIRONMENTAL REQUIREMENTS

For use in a laboratory or an office you should specify correct operation at 5°C to +45°C, and 0 to 95% relative humidity. This is not a difficult specification for any memory to meet.

A mobile system would require a specification on mechanical environment as well. You should investigate your own situation thoroughly before making a final specification.

8. RFI

If an RFI specification is required for system integration, you should specify that the unit should be immune to the applied disturbances shown below at (a), (b), and (c), and that it should not generate any disturbances in excess of those specified below at (d) and (e).

A. Conducted spikes. Specify: amplitude, duration, repetition rate, and power and signal lines on which the interference is to be applied. The repetition rate should be independent of the rate of the clock or other genuine inputs. This interference is to be superimposed on the genuine inputs and monitored at the memory inputs.

B. Conducted r.f. Specify amplitude, frequency limits, and points of application.

C. Radiated spikes and r.f. This is best specified in terms of the test conditions, which may simply be a wire at a certain distance from the memory, which is arranged to carry current spikes and oscillations of the specified characteristics.

D. Conducted output noise. Limits should be placed on high-frequency spikes and oscillations backing up on input signals and power lines, and also on similar noise being superimposed on genuine outputs on the output signal lines.

E. Radiated output noise. Core memories contain high-current loops switching at high speed. They can, therefore, radiate a substantial amount of energy. This may be minimized by good design, both electrical and mechanical, but if RFI could be a problem, specify that the memory be completely enclosed in a conducting box, with RFI gasketing at all joints.

9. TESTING

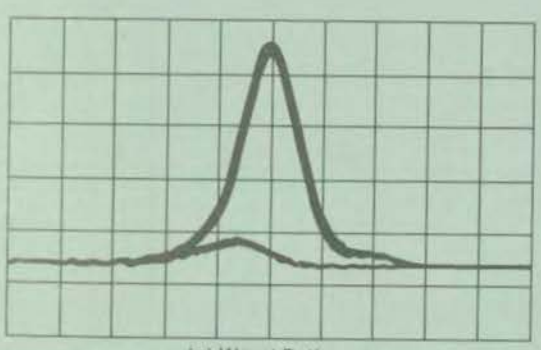
It is impossible to test a memory system under all conditions. Whatever testing you decide you can afford should be carried out at the worst conditions specified.

Some severe conditions are listed below. You may not need to operate under all these conditions, but the so-called "worst pattern" check should always be performed.

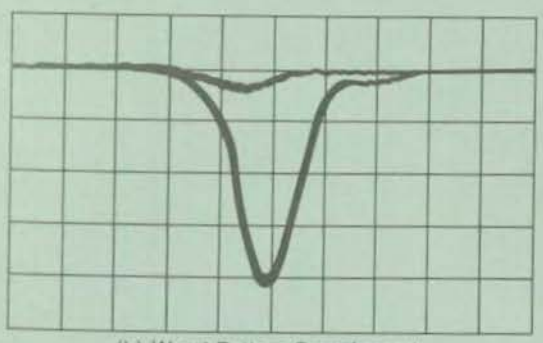
For testing elaborate non-standard memories it will usually be necessary to commission the building of a special purpose test set.

Any test set used should be equipped with means for automatically checking the data read from the memory, and indicating an out-of-spec condition. The test set should also have provision for monitoring input and output waveforms on an oscilloscope, and margining critical input parameters, such as power supply voltages, clock widths, amplitudes, and rise times.

Worst Pattern—This is a condition where the stored 1's and 0's are distributed in such a way that all the 1's give rise to a pulse of the same polarity (Fig. 3a). In this case, the zeros look more like 1's than in any other case, and the sense amplifiers have their hardest task distinguishing them. Worst pattern is fairly easy to generate in the test set. The complement (Fig. 3b) must also be checked.



(a) Worst Pattern



(b) Worst Pattern Complement

Figure 3

Bit Complement—This is a condition where worst pattern is stored in the memory and then each bit in turn is complemented, checked, and complemented again. In this case, the 1's are at their lowest condition.

Dwelling on One Word—In fast stores, there is a considerable heating effect in the cores. Have the test set continuously access one word (storing all 1's) for several seconds at its maximum operating speed. Then write a zero and error-check.

Always ensure that your specification states just what testing the vendor is required to perform, or at least references a document where this vital information may be found.

10. SIZE AND WEIGHT

You will get more favorable price and delivery if you specify a standard package which is usually a free-standing rack or a rack-mountable structure. If you have special requirements, a new design can be made. Size and weight considerations, if they are very stringent, as in the case of many aerospace programs, can have a considerable effect on the electrical and magnetic design. It is quite feasible to produce a memory weighing under a pound, and occupying less than 30 cubic inches.

You should specify that the vendor supply you, at an early date, with an outline drawing showing mounting dimensions, overall dimensions, and pin allocation on the connectors. This drawing should then become a contractual document.

11. NDRO or DRO

Non-destructive readout is an expensive luxury that may not be all that it seems.

Firstly, NDRO using multiaperature cores is as vulnerable to erasure due to equipment malfunction as any other core store, unless the writing circuits are physically disconnected.

Secondly, although the DRO two-beat cycle explained in Section (1) may seem an elaborate and risky way of handling data, it depends on magnetic and electronic parameters that are inherently very stable. DRO memory users very soon come to regard their memory as an NDRO black-box.

There are applications for wired-in program using core storage but they are generally expensive and inflexible once a design has been committed to manufacture, so the advice is to specify a straightforward DRO store, and concentrate your attention on more critical factors.

12. WORKMANSHIP AND DESIGN STANDARDS

For a commercial operation, the specification "good commercial practice" and the warranty provisions will take care of most requirements if you buy from an established manufacturer. The military are more fussy, and government contractors are usually bound by the terms of their contract to impose strict standards on their vendors. It is normally required that the vendor submit workmanship standards for approval and have his facilities inspected. If special designing is to be done, it is always advisable to specify ground rules for

worst-case design and derating of components. Approval of parts and components is often required for military products, but parts used in memories are so commonplace and so inherently reliable that an approval mill is little more than an academic exercise and should be avoided where possible. Spend the effort on detailed design reviewing and liaison on integration of the memory into your overall system.

Military customers should specify the appropriate MIL-specs but should be prepared to allow deviations in some areas which are not applicable to core memories. For instance, magnet wire soldering and some frame interconnect techniques are not covered by existing government specifications.

13. QUALITY CONTROL REQUIREMENTS

It is desirable to let the vendor think that all aspects of the specification will be monitored. The cheapest way of doing this is to let the vendor do it himself. So specify that a quality control plan is to be submitted and that facilities for your own inspection to carry out on-site audits of the vendors quality control system are to be provided. You will also save a lot of time and trouble by allowing the vendor materials review authority. This can be done under sufficient control to prevent abuse of the authority.

14. MAINTAINABILITY

A full pluggable system is obviously desirable, especially if a supply of spare modules is available. The memory stack is not normally divisible into modules, and even separating it from the drive decoding system involves breaking a large number of connections. You may have to specify this as one large replaceable unit in the interests of simplicity. Manufacturers will always be glad to sell you a stock of spare parts.

15. DOCUMENTATION

The very minimum is a certification that the memory meets the requirements of your P.O., and installation and operating instructions. These must be specified.

Further desirable documentation is a technical description (which may come free if you request a proposal), monthly progress reports, and an operating manual. You should specify in some detail just what is to appear in these documents.

More elaborate documentation which is often required for government contracts comprises some or all of the following:

1. Quality control procedures
2. Part and material specifications
3. Failure reports on returned material
4. Test data on the completed memory
5. Test data on components
6. Configuration logs
7. Assembly drawing
8. Materials review board actions
9. Design review minutes

The imaginative procuring officer will doubtless think of more, but an excess of paperwork will prejudice price and delivery.

16. WARRANTY AND SERVICE

These are usually specified in the contract rather than in the procurement specification, but it is essential to ensure that prompt attention will be given to malfunctioning equipment, and that the manufacturer accept appropriate financial responsibility.

17. PRICE AND DELIVERY

These factors will naturally be roughly proportional to the work required to meet the specification. Therefore, be prepared to relax on aspects of the specifications during negotiations. Sales Engineers will know best where the biggest savings are to be made. The most economical approach of all is to buy an existing design exactly as is.

The form shown on the following pages contains most of the specification requirements referred to in this article, and is provided as a convenient check-list for your future memory requirements.

CORE MEMORY VENDOR SPECIFICATION FORM: 4 units

GENTLEMEN:

We need a core memory system with the following specifications:

MEMORY CAPACITY:

How many words? 4096	☐ Minimum Requirement	☒ Exact Requirement
How many bits/word? 36	☐ Minimum Requirement	☒ Exact Requirement
Total storage capacity _____	☐ Minimum	☐ Exact

DATA:

☒ Parallel In ☒ Parallel Out

☐ Serial In ☐ Serial Out

SPEED: 2 μ sec / 4 μs microseconds per cycle (500K cycles per second)

_____ microseconds access time

MODES:

☒ Read/Restore	(full cycle)
☒ Clear/Write	(full cycle)
☒ Read/Write	(split cycle)
? ☐ Read	(half cycle-destructive unload)
? ☐ Write	(half cycle-load)
☐ Bash Clear	
☐ Block Load/Block Unload	
☐ Other (describe)	

ADDRESSING:

☒ Random Access

☐ Sequential Access ☐ Single Address ☐ Double Address

☐ From Internal Register

☒ From External Register ☒ Single Sided ☐ Double Sided

☐ Magnetic Counting Register

☒ Semiconductor Flip-Flop Register

☐ Other (describe) common on data bus

ADDRESS MARKERS:

☐ None

☐ Last Address

☐ First Address

☐ Other (describe)

TEMPERATURE RANGE:

Operating: − +15 ° Centigrade to − +45 ° Centigrade

Storage: − _____ ° Centigrade to − _____ ° Centigrade

Type of Cooling Available:

☒ Convection

☐ Cold Plate

☐ Radiation

PHYSICAL SIZE: _____" x _____" x _____" = _____ cu. in.

☐ Firm

☒ Negotiable

WEIGHT: Desired: _____; Maximum: _____

SHOCK REQUIREMENTS: _____

VIBRATION: _____

OTHER ENVIRONMENTAL REQUIREMENTS: Data save on power shutdown

APPLICABLE MIL SPECS none

APPLICABLE NASA SPECS none

OTHER APPLICABLE SPECS best commercial practice

CONNECTORS: How many? _____

Pins _____

INTERFACE SIGNALS:

# of Lines	
	Clock - start
2	Mode
	Address
	Reset
36	Data In
	Data Out
	Other Memory busy, Data ready

LOGIC ZERO = _____V ±_____ at _____ma. t_r = _____ μ sec.

LOGIC ONE = _____V ±_____ at _____ma. t_w = _____ μ sec.

t_f = _____ μ sec.

Type of Interface Ckt. (T²L), DTL, NPN Collector, NPN Emitter-etc. _____

Are mode, address, and data input lines settled at time of clock pulse? _____

How long do the input lines remain settled after leading edge of clock pulse? _____

POWER AVAILABLE:

_____watts maximum, operating at _____ (rate)

_____watts maximum, standby.

1.	115 volts	d.c. (a.c.)	at _____ amperes	±_____% tolerance
2.	_____		_____	_____
3.	_____		_____	_____
4.	_____		_____	_____

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