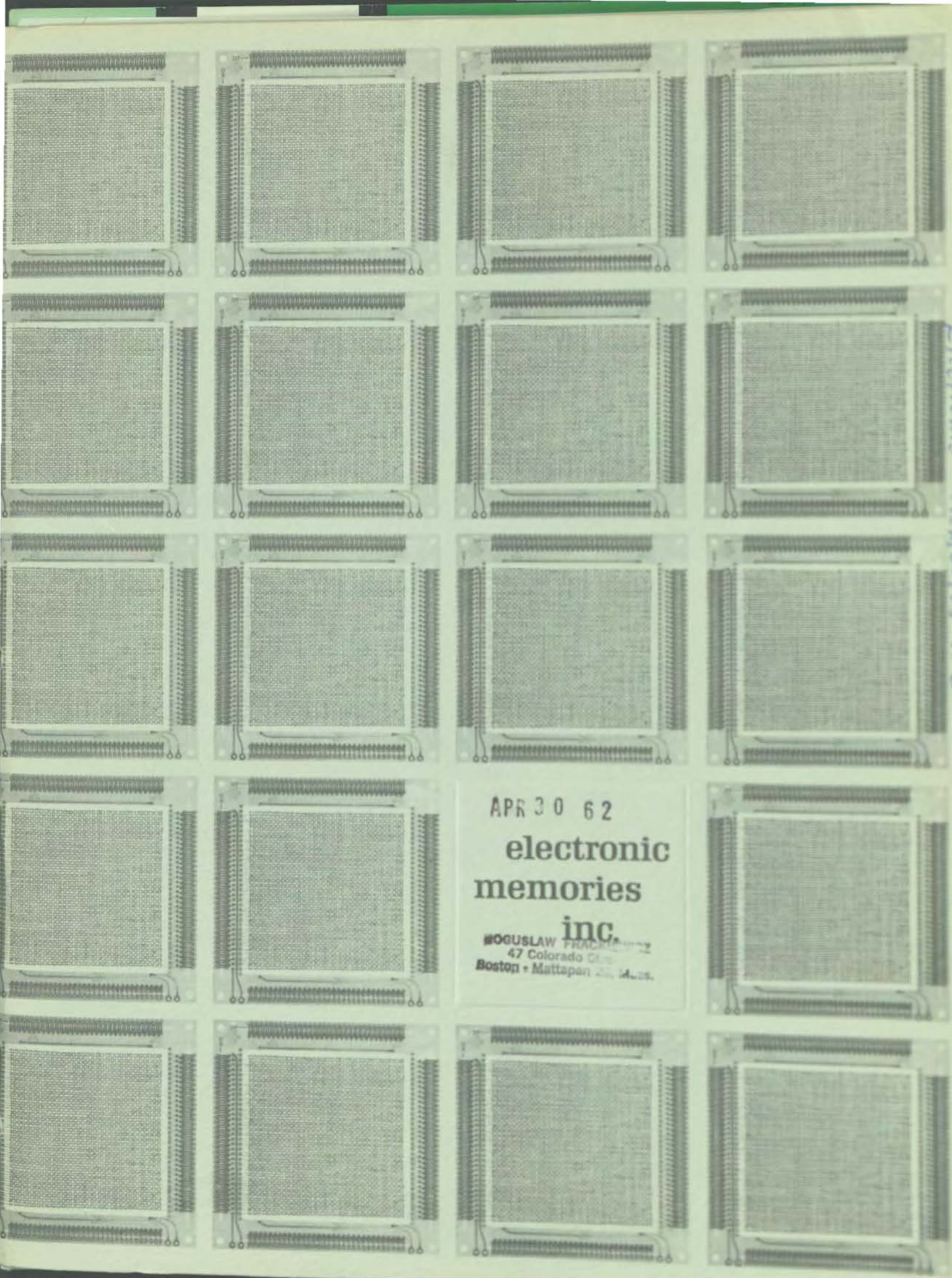

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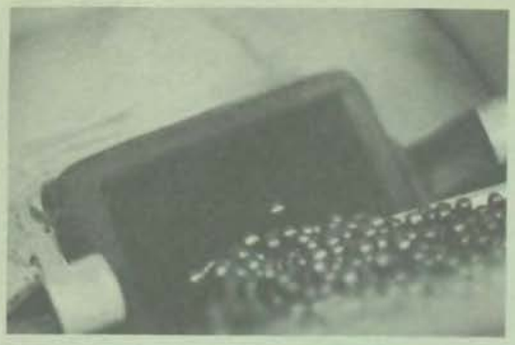
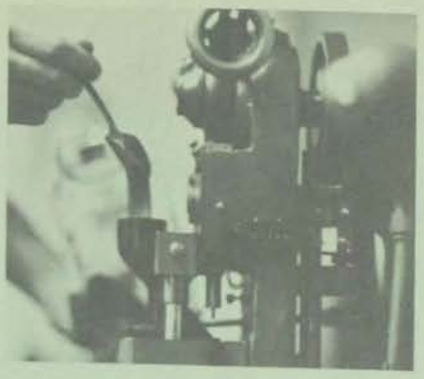
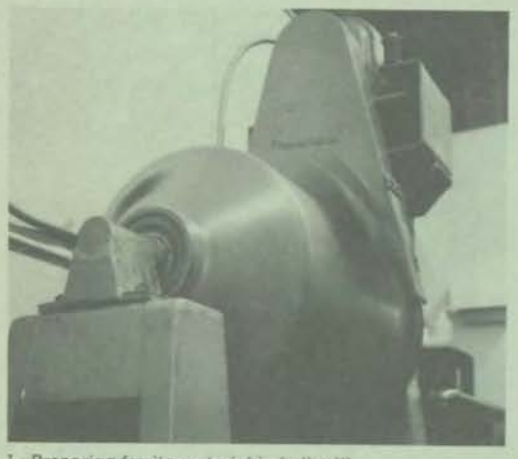
electronic memories inc.

BOGUSLAW FRACKIEWICZ
47 Colorado St.
Boston • Mattapan 25, Mass.

Electronic Memories Inc







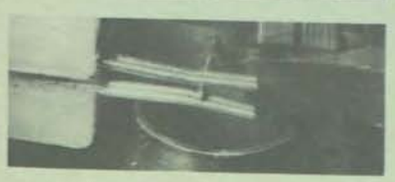
1. Preparing ferrite material in ball mill

2. Pressing toroidal shapes

3. Weight and dimensional quality control of unfired cores using an electro balance accurate to 10 micrograms

4. Cores are fired in kilns at temperatures ranging from 800°F. to 2300°F.

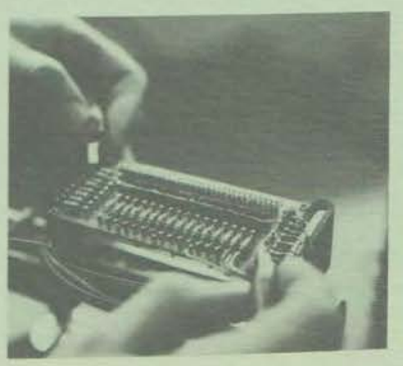
5. Cores are cleaned, sized and tested . . . a continuous quality control program is in effect.



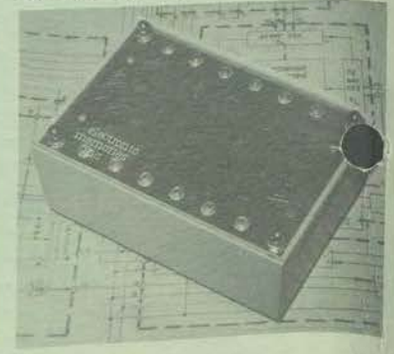
precise, controlled manufacturing techniques

6. Finished, tested ferrite cores are assembled into matrices

7. A continuous program of design and development work utilizes ferrite cores in memory systems



8. A finished product . . . ISODRIVE® Memory Model RE144OZ1



electronic memories inc.

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THE COMPANY AND ITS PURPOSE

Electronic Memories, Inc. was formed in June 1961 to develop, manufacture and market electronic and magnetic memory products. The company objective is to fill the increasing need for memory devices in the data processing industry, the communications field, guidance and control systems for the missile industry, communications and control systems for space vehicles and in the broad field of automation.

Electronic Memories, Inc. has designed and produced satellite core memory systems for Applied Physics Laboratories, General Electric Company, Goodyear Aircraft Corporation, Jet Propulsion Laboratory, Space Technology Laboratories, Burroughs Corporation, Aeronutronic, Librascope, and other leading scientific organizations.

Management at Electronic Memories is committed to a program of continuing state-of-the-art developments in cores, arrays, stacks and memory systems. A continuous effort, consistent with the company growth and funds available for research and development purposes, is being carried on in the area of more advanced memory elements and techniques.

PRODUCTS

Cores: The standard ferrite core product line is composed of 30, 50, 80, 140 and 180 mil sizes which have characteristics and specifications in general use throughout the data processing industry.

Electronic Memories has developed and is manufacturing two special types of ferrite cores which represent advances in the state-of-the-art:

(1) The ISODRIVE core, available in 30, 40 and 50 mil sizes, eliminates the need for either current compensation or oven enclosures when designing memories which must operate over a large temperature excursion; spe-

cifically, −55°Centigrade to +100°Centigrade. In addition, the ISODRIVE core yields a high output in millivolts on turnover and has a better disturb ratio, (knee current/full drive current) over the entire temperature range than standard cores have at room temperature. Development of 30 mil ISODRIVE cores for use in memories having cycle times of 1 microsecond and less is being carried on.

(2) EMI has developed a two-hole "shmoo" shaped transfluxor, which allows the first practical application of a transfluxor in a coincident current non-destructive memory. The "shmoo" shape gives excellent electrical characteristics, such that in the saturated state for Read or Write the unsaturated area of the transfluxor is very small. The physical and electrical characteristics of the Read hole of the transfluxor can be matched with those of a standard 50 mil toroid, allowing a design of a non-destructive coincident current memory and a destructive read "scratch pad" memory using the same drive circuitry design. The transfluxor has been successfully tested in coincident current operation over a temperature range of 0°C to +70°C with compensated drive currents.

Arrays and Stacks: Electronic Memories provides cores on standard matrices for standard stack configurations, or designed and manufactured for special customer requirements. Standard stacks are completely wired to connectors for the interface and come complete with mounting brackets. Stacks are available in both 50 mil and 30 mil core sizes. With the fast-switching EMI 30 mil cores, cycle times to less than 2 microseconds are achievable in a coincident current system. Among the special designs available are heated stacks for both commercial and adverse environment applications and non-destructive readout stacks incorporating the EMI "shmoo" in a coincident current configuration. For the memory design engineer, EMI has a supply of arrays in stock incorporating our standard cores. The arrays are available on loan so that driving and sensing circuits can be checked out before production quantities are ordered.

Memories: The forward steps in ferrite core development described above have given Electronic Memories, Inc. the ability to design and develop unique memory products offering substantially improved operating characteristics to the customer. Two important memory systems have already been developed for the customer who faces severe environmental conditions in his applications:

(1) The ISODRIVE MEMORY Model No. SE1440Z1 is a MIL-SPEC bit serial core memory which can perform in space vehicles as a communication buffer, time interval programmer, function control programmer, computer program memory, computer working memory, or as a set of core logic nets. This ISODRIVE MEMORY operates over a temperature range of −30°C to +90°C, weighs less than 16 ounces, occupies a volume of less than 30 cubic inches, has a storage capacity of 1440 bits, and an

operating speed of 100 Kilocycles. The unit is designed to use the minimum number of semiconductors and maximum core logic and core switching. The SE1440Z1 ISODRIVE MEMORY has been designed using MIL-approved components, finishes, fabrication standards and quality controls. Memories having capacities of 8000 and 30,000 bits are also available.

(2) The modular ISODRIVE MEMORY RE4096Z40 designed to meet MIL-SPECS is a medium sized, high speed random access memory. The memory uses coincident current techniques with the ISODRIVE core and has a cycle time of 2.5 microseconds. The memory construction is modular to allow word sizes of 4096, 8192 and 16,384 words with a bit length from 8 bits to 80 bits. The signal levels for both input and output allow for a reasonable range of signal amplitudes. The RE4096Z40 will operate over a temperature range of −30°C to +80°C. The memory has been designed for minimum power consistent with the 2.5 microsecond cycle time. The physical package is designed to give maximum space utilization. Normal use of this ISODRIVE MEMORY will be in ship or ground-based equipment.

Electronic Memories has developed additional memory systems for the requirements of the adverse environment market as well as commercial systems for the data processing and computer field.

Programmed Magnetics Testers: A series of precise test instruments has been specifically designed for the testing and evaluation of magnetic cores and circuits. The testers are completely modular, allowing cost and test program flexibility.

PLANT FACILITIES

Electronic Memories, Inc. is housed in a modern building located about ¾ of a mile from the Los Angeles International Airport and 4 blocks from the Manchester Avenue exit of the San Diego freeway. The building has 10,000 square feet of floor space. The plant is well lighted and has an asphalt tile floor; it is efficiently laid out, allowing 2000 square feet for office space, 1000 square feet for Research, and 7000 square feet for Engineering and Production. The entire building is air cooled and the office space and production test equipment areas are air conditioned. An additional 40,000 square feet is being acquired for expansion of the production facilities.

ENGINEERING

The engineering laboratories at Electronic Memories are well equipped consistent with over-all company size. In addition to the normal complement of oscilloscopes, meters, power supplies and signal generators, the Engineering laboratories contain approximately $250,000 worth of equipment of special design required in testing and designing magnetic core memories. This equipment includes five magnetics testers used for studying and plotting curves of various core characteristics, three environmental chambers for testing and

evaluating core parameters over the various necessary temperature ranges, and a core array tester designed and built by EMI personnel used for studying and evaluating magnetic core properties in arrays, core stacks, and special winding configurations.

MANUFACTURING

Facilities presently exist in the Manufacturing Department for the production and test of:

ferrite square loop memory cores
ferrite square loop switch cores
ferrite linear cores
core memory systems for space programs
core memory systems for military programs
core memory systems for commercial computers
magnetics testers

Manufacturing facilities include a temperature-controlled and dust-free area for core and array test, three Ramsey high speed core handlers, two DEC core testers, one EMI core stack tester, one random-access memory exercisor and the conventional complement of oscilloscopes, magnetics pulse generators and equipment for the manufacture of cores, arrays and memory systems.

PERSONNEL

Electronic Memories was founded and is managed by personnel with a unique depth and breadth of experience in the ferrite core, memory and computer industry. Each of these men has held key design, engineering, research, production and marketing management positions in these fields prior to associating with Electronic Memories. *This wealth of talent is our most valuable asset.*

President: **Trude C. Taylor**

Mr. Taylor has worked in the computing and data processing industries since 1951, performing engineering, manufacturing, and marketing functions with Northrop, Telecomputing, Telemeter Magnetics, and Ampex Computer Products. Mr. Taylor is a graduate of University of California at Los Angeles (BSME) and the Harvard Graduate School of Business Administration (MBA).

Prior to forming Electronic Memories, Inc., Mr. Taylor was a Vice President and Director of Telemeter Magnetics, Inc. until that company was merged with Ampex Corporation in January 1961. Mr. Taylor joined Telemeter Magnetics as Vice President and Director of Marketing. He was later appointed Vice President and General Manager of the Data Equipment Division, which achieved an annual sales volume in excess of five million dollars.

After TMI's merger with Ampex Corporation, Mr. Taylor held the position

of Director of Marketing for the Ampex Computer Products Company, where he was responsible for the promotion, sales, service and product planning of the previous Telemeter Magnetics business plus other Ampex products being sold to the computer industry.

Vice President, Engineering: **Milton Rosenberg**

Mr. Rosenberg, sole or co-inventor of more than twenty-five U.S. patents and author of numerous papers on core memory engineering techniques, brings to Electronic Memories, Inc. a significant reputation in the ferrite core and memory technology. Through effective use of electronics, magnetic and ceramic disciplines, he has made major contributions to the memory art.

As Manager of the Advanced Development Division of Ampex Computer Products Company (and the predecessor, Telemeter Magnetics, Inc.) from June 1959 to June 1961, he was responsible for the development, design and pilot production of new commercial cores, adverse environment cores and satellite memory systems.

As General Manager of the Ferromagnetics Division of Telemeter Magnetics, Inc. from 1955 to 1959, he was responsible for the development, design and production of memory cores. He established a new core facility and developed production to a rate of 2,000,000 cores per week.

During the period 1953 to 1955, he was responsible for the magnetics design of several large core memory systems produced for the Rand Corporation, Argonne Laboratories, Aberdeen Proving Ground, Patrick Air Force Base, and others. At RCA Laboratories in Princeton, Mr. Rosenberg was a Research Engineer from 1946 to 1953. In this capacity he was responsible for development of storage devices utilizing both cathode tube and ferrite core techniques.

Director of Research: **Dr. Robert S. Weisz**

The contributions of Dr. Weisz to the metal ceramics field have been numerous and significant. During the past twelve years his efforts have been devoted exclusively to this field: six years at the RCA Laboratories in Princeton, New Jersey, where he worked continuously in research and development of square loop ferrite core materials and processes. Dr. Weisz's work continued while employed by Telemeter Magnetics, Inc. (now the Ampex Computer Products Company) during the past six years, where he was responsible for the development, design and process formulation of all magnetic cores produced by TMI.

Dr. Weisz has also conducted original research in magnetic thin film techniques, and his work in this field will continue at Electronic Memories, Inc. From 1942 through 1947 Dr. Weisz was employed by the Westinghouse

Research Laboratories in Pittsburgh to do advanced research in physical chemistry with emphasis on ceramics techniques including some early research in linear ferrite materials. From early 1947 and until mid-1949 Dr. Weisz continued advanced development and research at the Thomas A. Edison Company as a Research Chemist. His efforts were primarily devoted to development of new and improved thermistors and batteries.

Dr. Weisz has published many professional papers in the fields of inorganic chemistry and electro-chemistry. He was honored in 1951 with an award by the Foote Research Foundation for reporting on his work in lithium ferrite materials. He is sole or co-inventor of over ten U.S. patents in ferrites and electro-chemistry.

Dr. Weisz received his AB from Cornell University in 1939 and his Ph.D. in 1942. The Doctorate was awarded in Physical Chemistry. While earning his advanced degree, Dr. Weisz served as an instructor in analytical chemistry at Cornell University.

Senior Chemist: **Daniel L. Brown**

As a Senior Chemist from 1957 to 1961 at Telemeter Magnetics, Inc., Mr. Brown was responsible for new ferrite core development, production engineering, and process formulation of a full product line of memory and switching cores. During the period 1955 to 1957, he was employed by Lincoln Laboratories as Ceramic Laboratory Supervisor responsible for the development of high-speed memory cores for the TXI Computer. He was employed by the U.S. Bureau of Mines from 1952 to 1955 in the synthetic materials group at Norris, Tennessee, responsible for research and development of synthetic asbestos. Mr. Brown received a BS degree from Knoxville College, Knoxville, Tennessee in 1951. He has also completed advanced courses at Northeastern University, Boston, Mass. Mr. Brown is the sole or co-inventor of 3 U.S. patents in ferrite materials and synthetic minerals.

Senior Staff Engineer: **William S. Knowles**

Before joining Electronic Memories, Mr. Knowles had been Project Engineer responsible for satellite core memories used as communication buffers, flight programmers and control computers for the VEGA, MARINER, and TRANSIT programs. This work was conducted at Ampex Computer Products Company (formerly Telemeter Magnetics, Inc.) where Mr. Knowles' responsibility included the magnetics, electronics, system and environmental packaging design, and schedule and budget performance.

From 1957 to 1959 at TMI Mr. Knowles was responsible, as Project Engineer, for the design and construction of data translators to convert analog information to computer format magnetic tape; translate magnetic tape to paper tape; and to drive a high-speed Videograph printer from a com-

puter tape input. From 1954 to 1957, Mr. Knowles was a member of an engineering group responsible for the design of a wide line of computer core memories ranging in storage capacity from a few hundred bits to 500,000 bits and operating speeds ranging from 1.5 microsecond to 20 microseconds cycle time. His major concentration was on core driving and sense amplifier circuits.

From 1952 to 1954 he was with ASCOP (Applied Science Corporation of Princeton) where he worked on a digital system for automatic analysis and processing of missile telemetry data. At Johns Hopkins University Applied Physics Laboratory from 1942 to 1952, he participated as an Electronic Design Engineer, later becoming Project Engineer, in the development of proximity fuzes, f.m. receivers, and the basic development of the f.m./f.m. system of missile telemetry instrumentation.

Mr. Knowles is the sole or co-inventor of 12 U.S. patents in the field of electronics.

Senior Magnetics Engineer: **W. Robert Johnston**

Mr. Johnston has specialized in core memory development and production design during the past seven years. During the past two years, he has been responsible for the magnetics design of satellite core memories for the VEGA, MARINER, and TRANSIT Programs. In addition, he was the Design Engineer for a satellite decade counter and magnetic logic circuits using ferrite cores.

From 1956 to 1959, Mr. Johnston was responsible for the magnetics and driver circuits for core memories which have been produced in substantial quantities during the past several years. The memories were both serial and random access systems with the former employing magnetic switch cores for access decoding and driving. During the period 1953 to 1956, Johnston was responsible for the design and fabrication of automatic core testing equipment, calibration techniques, quality control procedures, and manufacturing process standards. Mr. Johnston is the sole or co-inventor of 3 U.S. patents.

Senior Staff Engineer: **Ben T. Goda**

Twelve years of Mr. Goda's professional career have been concentrated in the design of computer circuits and magnetic core memories. His aggressive design efforts have provided memories of high performance at low manufacturing cost levels. During the period of 1952 to the present, he has concentrated on the design of magnetic core memories for commercial digital computers. As Engineering Section Head at Telemeter Magnetics, from 1956 to 1961, he was responsible for the development and production design of sequential buffer memories, high-speed printer line buffer memories, small random access eight-microsecond memories, and

large five-microsecond memories with a storage capacity of 16,384 words of up to 60 bits. These designs provided modular memory packages to meet a wide range of capacity requirements.

From 1952 to 1956, Mr. Goda was a Senior Engineer for Bendix Computer, responsible for the design of a magnetic drum memory and associated circuits (tube) for the G-15 Computer. He also undertook development design of transistor circuits for advanced computers and designed a small random access solid state core memory. Employed by Northrop Aircraft from 1950 to 1952, Mr. Goda was a Circuit Engineer and Peripheral Equipment Designer for the MADDIDA Computer System. Mr. Goda is a graduate of the Engineering School at the University of Southern California (BSEE) and is sole or co-inventor of 6 U.S. patents in the computer field.

Senior Staff Engineer: **Harry L. Knapp**

Mr. Knapp is a graduate of Iowa State University with a BSEE degree. At EMI Mr. Knapp is the Project Engineer on a spacecraft memory system. Prior to joining EMI Mr. Knapp was employed at Telemeter Magnetics, Inc. (later Ampex Computer Products Company) as Project Engineer and later Manager of Military Systems. In these capacities he worked on memory design and development for the Bank of America ERMA system, the Air Traffic Control System, and the high speed 1-microsecond Aberdeen Proving Ground memory. In military systems Mr. Knapp was responsible for the design and development of a high speed buffer system for use in radar applications, a buffer system for the BIRDIE missile program, and a spacecraft memory program.

From 1955 to 1958 Mr. Knapp held the position of Design Engineer at Remington Rand UNIVAC and designed the core memories used in their Scientific Computer program. He also worked on the design of the computer proper for the UNIVAC Scientific Computer program.

Chief Mechanical Engineer: **V. E. Hovnanian**

Mr. Hovnanian received his BME from New York University. Before joining EMI he held the position of Supervisor, Mechanical Design at Gilfillan Bros. Inc. In this position he was responsible for the transmitter design of a Navy radar system. Prior to this Mr. Hovnanian was a member of the technical staff at Thompson Ramo-Wooldridge responsible for mechanical design of airborne electronic equipment.

From 1957 to 1959 he was the engineer in charge of large engine test stands at Rocketdyne. He was responsible for the design of systems required to test Atlas rocket engines, including electrical, mechanical, pneumatic and propellant systems. From 1950 to 1957 he was Thermodynamicist at Lockheed Aircraft Corporation where he performed design

weight analysis of aircraft structures and systems and heat transfer analysis.

Senior Electronics Engineer: **Robert W. Chambers**

Prior to joining EMI Mr. Chambers was Project Engineer on the Electrada Corporation's Datacom unit. While at Electrada Corporation he worked on design and development of digital data transmitters and mechanical drum test units.

From 1956 to 1960 he held the position of Project Engineer at Advanced Electronics Manufacturing Corporation and worked on control and storage systems for automatic embossing machine equipment, computer input/output equipment and drum memory storage. Prior to this Mr. Chambers worked on remote metering systems for the oil industry at the Smith Meter Corporation subsidiary of A. O. Smith.

While at the Rand Corporation he worked on the design and development of the prototype Johnniac Computer and the final design.

Mr. Chambers is the co-inventor of one U.S. patent and attended Santa Monica City College and the University of Southern California, where he majored in physics.

Staff Engineer: **Helmet Graf**

Mr. Graf engaged in the design of U.H.F. television transmitters from 1951 until 1954. In 1954 Mr. Graf became associated with Motorola as a Design Engineer in a pulse circuitry development group. From 1958 until 1961 he was responsible for design and development of coincident current core memories at Telemeter Magnetics, Inc.

Mr. Graf received a BEE from the Oskar V. Maller College, Munich, Germany. Since his affiliation with EMI he has completed the circuit design for a MIL-SPEC high speed memory.

Staff Engineer: **Loy Spears**

Mr. Spears joined EMI in June, 1962. His experience in the design of ferrite memory devices includes a position as Staff Engineer, designing memory systems with Rese Engineering in Philadelphia, Pa. from August, 1961 until June, 1962. Before that, Ampex Computer Products Company (formerly Telemeter Magnetics, Inc.) employed him as a Staff Engineer designing memory systems, from June, 1959 to August, 1961. While with Ampex, Mr. Spears was also the Project Engineer on a 1.5 microsecond memory project. During 1959, he was a Field Engineer with IBM in Kingston, New York.

Mr. Spears attended Santa Monica City College and Reed College (Portland, Oregon) where he majored in mathematics. His present responsibility with EMI is the design of satellite data storage units.

Manager of Ferrite Production: **Donald A. Zumwalt**

Mr. Zumwalt received a BS degree from the University of Illinois in Electronic Engineering and has taken advanced courses in metallurgy and electronics at the University of California at Los Angeles.

Before joining EMI Mr. Zumwalt held the position of Production Manager and Chief Engineer for Statnetics Corporation. His work involved producing new types of miniaturized ceramic capacitors. From 1958 to 1961 Mr. Zumwalt was Manager of Ferrite Production at Telemeter Magnetics, Inc. and was responsible for the manufacture of all ferrite memory cores and magnetic head pieces. This included electronic testing, formulation and processing of the ferrite memory cores. From 1956 to 1958 he held the position of Ceramics Engineer with Collins Radio Company where he developed processes for special radio frequency ferrites. Projects included particle size studies and their relation to crystal growth, methods of producing special shapes, formulations, process specification and process methods for extrusion.

Previous to 1956 Mr. Zumwalt worked in research and development for Glascote Products Division of A. O. Smith. The experience gained here covered a wide range of electronic applications, such as special ceramic coatings for high temperature applications used in rockets, aircraft exhaust and automatic reactors. Laboratory work was also done in formulation and testing of electrically resistant glass for chemical pressure tanks.

Director of Manufacturing: **Bernard Hathaway**

Mr. Hathaway brings more than ten years of electronic manufacturing production experience to EMI. From 1957 through 1961 he held a series of managerial positions in Engineering and Production at Ampex Computer Products (formerly Telemeter Magnetics, Inc.) Prior to joining TMI, Mr. Hathaway was associated with Lear, Inc. and Canadian Marconi as a Project Engineer.

Mr. Hathaway is responsible for all facets of production at EMI. He supervises the work of more than 100 engineers, technicians and production line workers engaged in the manufacture of ferrite cores, arrays, stacks and complete memory systems.

Mr. Hathaway was educated at Rotherham College of Technology, where he graduated in 1949 with a Bachelors Degree in Electrical Engineering. His professional affiliations include membership in both the Institute of Electrical Engineers and the Institute of Radio Engineers.

Production Manager: **Jack Hill**

Mr. Hill brings to Electronic Memories 20 years of experience in electron-

ics manufacturing, maintenance and ferrite core assembly techniques. From 1941 to 1945 Mr. Hill worked with radar and moving target indicator equipment at MIT Radiation Laboratories. During the period 1945 to 1950 he maintained and installed custom-made television projection systems. From 1951 to 1954 he was employed by International Telemeter Corporation in the production and installation of the early pay-as-you-go television systems. During 1954 and 1955 at ITC Mr. Hill was engaged in the development and production of several large scale memory systems for the Rand Corporation, Aberdeen Proving Grounds, and others.

At Telemeter Magnetics (now Ampex Computer Products Company) from 1956 to 1961 Mr. Hill was responsible for the supervision of the Engineering model shop. In this capacity he developed pre-production and production techniques for a complete line of magnetic core buffers and commercial random access memories. He was also responsible for the prototype production and initial production models of a large 1.5 microsecond cycle time memory.

Mr. Hill presently manages a skilled production crew who are producing a number of satellite memories and other memories for MIL-SPEC applications.

Product Manager: **Dean Knutson**

During the period 1958 to 1961, Mr. Knutson was employed by Telemeter Magnetics as a Product Application Engineer and later as Sales Manager for the Advanced Development Division. He was responsible for design analysis and application studies of ferrite cores and memories to a wide range of computer, data handling, automatic control systems, and memories for satellite and missile programs.

Mr. Knutson was employed by Waugh Engineering from 1956 to 1958 as Project Engineer for engine fuel flow test facilities. From 1949 to 1956, he was employed by Telecomputing Corporation successively as Customer Service Engineer, Field Service Engineering Manager, Applications Engineer, and Sales Manager for data reduction equipments. During this period, he was actively involved in system and equipment design and application for telemetry, high speed camera and wind tunnel instrumentation, data collection and data processing. Mr. Knutson received a BSEE from the University of California at Berkeley.

Product Manager: **Ronald G. Heath**

Mr. Heath received his degree in Electrical Engineering from the Royal Aircraft Establishment College in England in 1952. He has 8 years of experience in sales of core memory and core memory products.

Prior to joining EMI, Mr. Heath was employed by the Military Electronics

Division of Daystrom, Inc. as Sales Manager for high speed memory products and development contracts in the Western USA. From 1958 through 1961, Mr. Heath was associated with Telemeter Magnetics, Inc. as a Project Engineer on high speed memories and buffers, and as a Sales Engineer for their Core Memory Division. Mr. Heath was also associated with Canadair Ltd. in Montreal as a Senior Engineer in the Missile Instrumentation Group. His professional affiliations include membership in the Association for Computing Machinery.

Eastern Regional Sales Manager: **Richard J. Dadamo**

Mr. Dadamo is responsible for the sales of EMI products in the Eastern seaboard states.

Mr. Dadamo's educational background includes a BSEE at Pennsylvania State University, 1951; MSEE at Drexel Institute of Technology, 1954; Graduate Work, Digital Computers at Moore School, University of Pennsylvania; Graduate Work, Business Administration, Drexel Institute of Technology.

Mr. Dadamo joins EMI from Burroughs Corporation where he was Engineering Manager of the Electronic Instruments Division, responsible for all phases of engineering. He joined Burroughs in 1956 as a Design Engineer responsible for magnetic circuits, memory stacks, memory systems and memory test systems. He participated in the Atlas Guidance system program at Burroughs; and in 1958 he was promoted to Supervisor of the Electronic Design Group, responsible for the development of magnetic devices.

Prior to Burroughs, Mr. Dadamo worked as a Design Engineer at Sperry Rand Univac and for the U. S. Naval Department. In addition, Mr. Dadamo has taught digital computer courses at Temple University, Philadelphia, Pa.

Western Regional Sales Manager: **Jack Ogg**

Mr. Ogg is responsible for all EMI sales activities in the Western states. He has a wealth of experience in marketing computer related products, having held the position of Marketing Division Manager for Ampex Computer Products Company (formerly Telemeter Magnetics, Inc.) before joining Electronic Memories.

Prior to joining Ampex, Mr. Ogg was employed by Telecomputing Corporation, where he began in 1950 as Data Reduction Supervisor in the Computing Center and rose to Sales Manager, Data Equipment Division in 1957.

Mr. Ogg attended both the University of Southern California and the University of California, Los Angeles, where he majored in Business Administration.

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sales offices

electronic memories

Thank you for your recent inquiry. The information you requested is enclosed. We look forward to supplying you with ferrite memory cores, arrays and stacks, or complete memory systems.

For your convenience, your nearest EMI representative is listed below.

RECEIVED
APR 11 1967
P. FRACKIEWICZ

CALIFORNIA

Electronic Memories Inc.
12621 Chadron Avenue
Hawthorne, California 90250
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TWX 910-325-6213

Electronic Memories, Inc.
Western Regional Sales Office
13415 Ventura Blvd. Suite 2
Sherman Oaks, California 91403
(213) 872-1062

Tech Marketing Associates
355 West Olive Avenue
Sunnyvale, California 94086
(408) 736-3687
TWX 910-339-9227

ILLINOIS

Electronic Memories, Inc.
Central Regional Sales Office
259 E. Rand Road
Mt. Prospect, Illinois 60056
(312) 253-7540

Ropek-Cahill, Inc.
5439 West Division Street
Chicago, Illinois 60651
(312) 287-7292
TWX 910-221-5219

MASSACHUSETTS

Electronic Memories, Inc.
Eastern Regional Sales Office
11 Chestnut Street
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TWX 710-347-0334

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W. R. Hummon & Associates
P.O. Box 501
Farmington, Michigan 48024
(313) 474-0661

MINNESOTA

Lloyd Murphy Associates
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Minneapolis, Minnesota 55415
(612) 333-4511
TWX 910-576-3417

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TWX 513-944-0256

Jay Engineering Company
4712 West 130th Street
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coincident current NDRO memory

The Electronic Memories "Shmoo" transfluxors are designed to combine nondestructive readout (NDRO) capability with the low cost of coincident current selection.

Electronic Memories is presently producing NDRO stacks to be operated over a wide temperature range in an aircraft type environment.

The "Shmoo" core may be operated in a number of different ways. After a discussion of the basic principles of operation of the core, we shall briefly describe two methods of operation in a stack.

principles of operation

The core in Figure 1 is shown in the "cleared" or "0" state. The core has been fully saturated by a clear current pulse as shown. The orientation of the lines of flux are indicated by the arrows.

If a current pulse is passed through the read hole of a core in the "0" or cleared state, essentially no output voltage will appear across the sense winding. Since the core is in hard saturation as shown in Figure 1, any current in the read hole (as shown in Figure 2) will not cause any significant change in flux.

Naturally, there are limitations of current amplitudes for which the above statement is true. These limitations will be discussed later in detail.

If a current is passed through the write hole in the opposite direction to that of clear current, the flux in leg 2 and part of that in leg 3 will be reversed. The core is now said to be in the "1" state as shown in Figure 3. Write current amplitude must be limited in order not to reverse more than half of the flux in leg 3.

A current pulse in the read direction in the read hole will now reverse the flux in legs 1 and 2, and will result in an output voltage across the sense winding. A current pulse in the set direction following the read pulse will reset the flux in legs 1 and 2 to the original "1" state condition, and while so doing, will produce an output voltage of opposite polarity across the sense winding (see Figure 4).

figure 1.

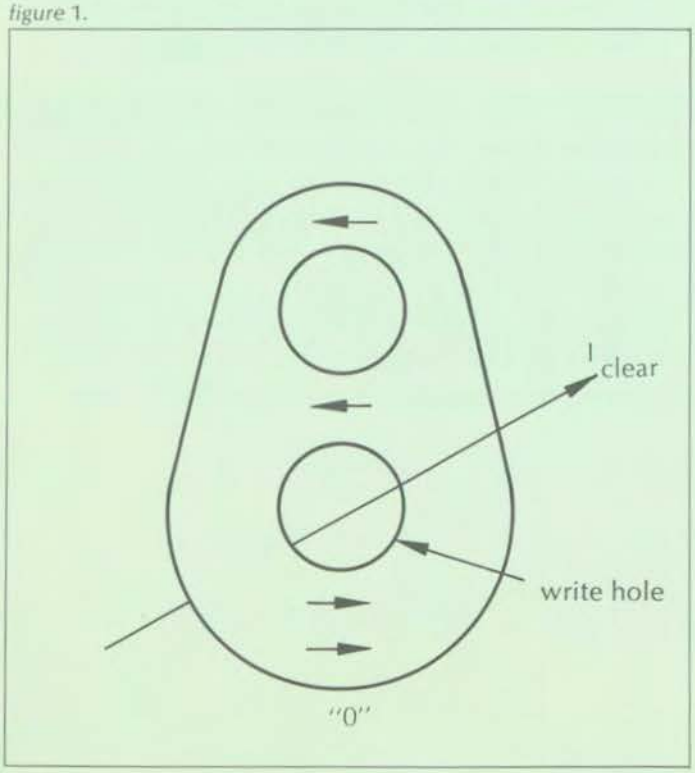
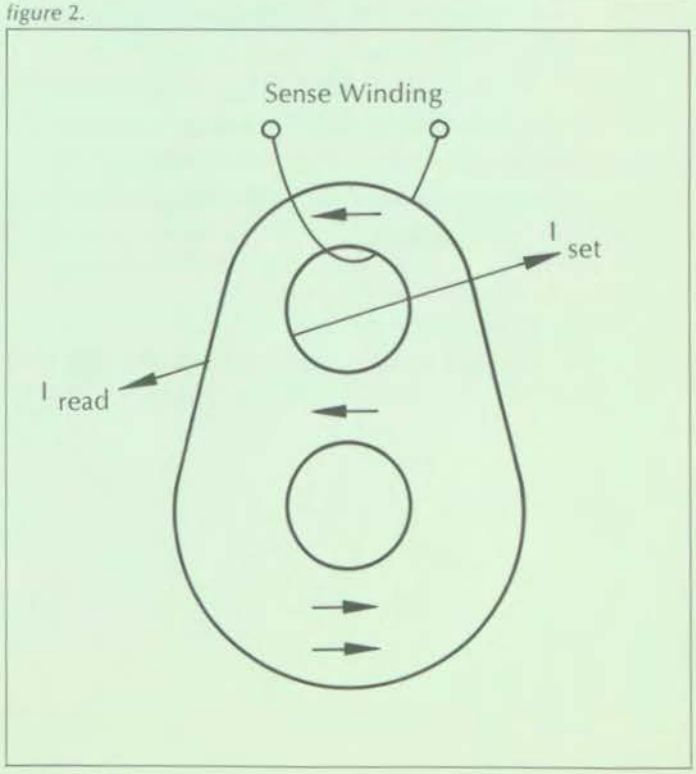


figure 2.



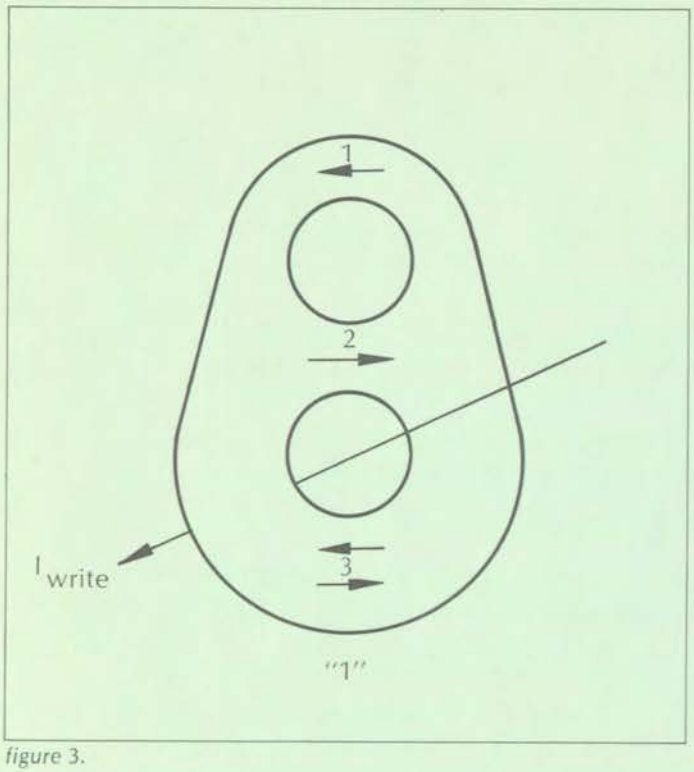


figure 3.

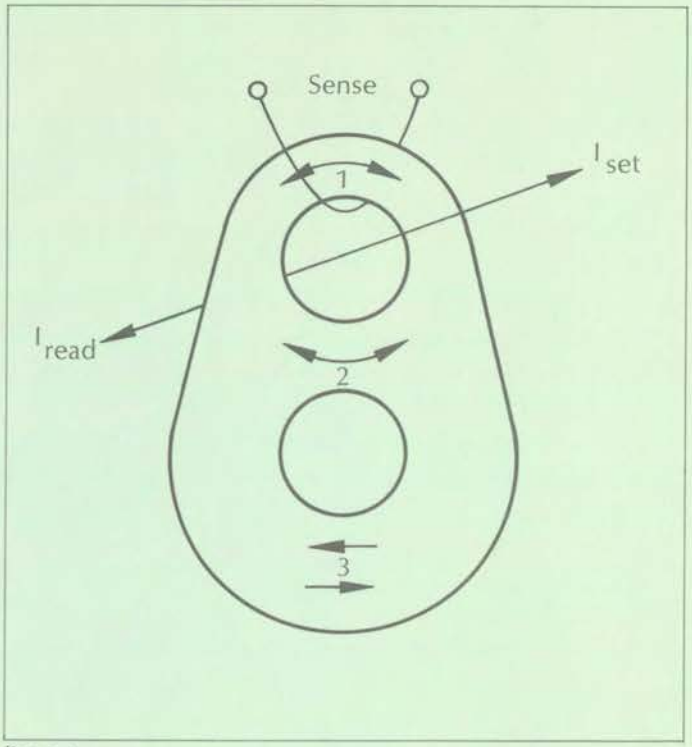


figure 4.

The NDRO principle of operation results from the fact that the core can be read and set an infinite number of times without ever having to re-write the information as in a standard toroid memory core.

The information stored is determined by the state of flux in leg 3.

practical limitations:

In order to discuss basic limitations of this geometry, some definitions are first in order.

I_{KR} = Knee of the read hole.
I_{KW} = Knee of the write hole.
$I_{KR\text{-}W}$ = Unblock knee, amplitude of current in the read hole, in the read direction, that will cause a core in the "0" state to begin to change to the "1" state. Current pulses at this level or higher will cause the information written into the memory to be destroyed.

Hence, the absolute limits for read current are:

$$I_{KR} < I_{R\ min.} < I_R < I_{KR\text{-}W}$$

where $I_{R\ min.}$ is the minimum value of read current necessary to produce a desired output signal level.

Figure 5 depicts the results of $I_R > I_{KR\text{-}W}$. Since the flux in leg 2 is already saturated in that same direction, the only possible flux couple is between legs 1 and 3. The current begins to switch the innermost flux in leg 1, along with the innermost flux of leg 3 (shortest path length). When all of the flux of leg 1 has been reversed, half of the flux of leg 3 is also reversed, and the core is now in the "1" state.

operation: *Write Mode*

The write operation is a coincident current operation which may be performed only after the desired word/words to be written into have been cleared by applying clear current in the appropriate clear section.

A "ONE" is written by applying a Y set pulse in coincidence with an X read pulse with polarities as shown in Figure 6.

When writing it is imperative that the least significant bit of the X address register be complemented in order to select the proper address. For example, to write a "ONE" in X_{00} Y_{00}, a Y_{00} set pulse is applied in coincidence with an X_{01} read pulse due to the fact that the X drive line through a read hole of a core re-enters the write hole of a core on an adjacent line.

During this operation, the Y read and X set pulses are gated off by a timing generator.

In order to write or maintain a "ZERO," the write operation is performed in coincidence with an inhibit pulse of the proper polarity as is normal for coincident current operation.

operation: *Read Mode*

The read mode of operation is identical to the standard coincident current operation of a toroidal core. The core output is sensed during the full read pulse and the core is subsequently set to the original state by a full set pulse of equal but opposite polarity.

five-wire system

In the five-wire system, each core is threaded in the following manner:

Write Hole	*Read Hole*
1. Clear winding	1. X drive line
2. Inhibit winding	2. Y drive line
	3. Sense winding

The clear winding again divides the stack into sections for convenience. The X, Y drive, inhibit and sense windings are conventional.

operation: *Write Mode*

In order to write information into the memory, the appropriate clear section/sections must first be cleared by applying a clear current pulse of proper polarity, amplitude and duration to the clear line.

The write operation is performed following a clear operation by selecting in a coincident current manner, the appropriate X and Y lines and driving with current pulses equal to $\frac{I}{2}(R+W)$ amplitude.

Hence, writing is accomplished by overdriving the read hole to produce the "ONE" and by adding an inhibit pulse in the clear direction in the write hole to maintain a "ZERO."

operation: *Read Mode*

The read operation of the NDRO is performed by coincidence of I_{read} followed by I_{set} on the appropriate X, Y lines. In addition, in coincidence with the I_{read} pulses, a pulse bias in the clear direction may be provided in the write hole on the clear sections common with the selected address to increase the current tolerances.

After writing, the memory must be cycled through completely one time before valid data is available. The reason for this is that while writing with $\frac{I}{2}(R+W)$ half pulses, cores on the selected lines are left in the readout state and therefore must be reset before being read in the next cycle.

A new "Shmoo" core is currently being developed at Electronic Memories which will not require the pulse bias current in the write hole in the five-wire system. Shmoo's are being made in both the conventional MgMn ferrite and in the low temperature coefficient lithium materials. Cycle times as low as 2 microseconds are obtainable in NDRO memories. Drive currents are as low as 190 ma for half pulses. Signal-to-noise ratios of 5:1 with drive current tolerances of ± 10 percent over a temperature range of 100°C are obtainable.

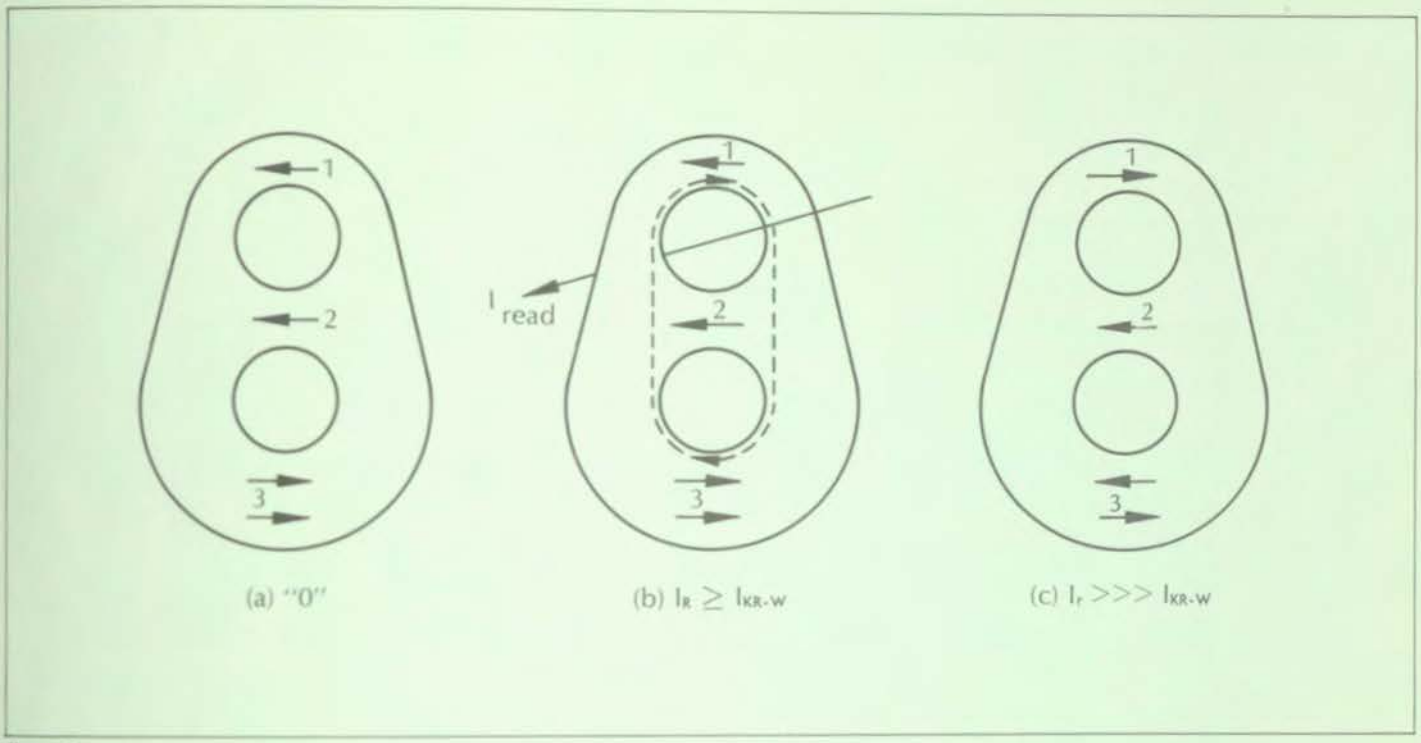


figure 5.

The ratio of $\frac{I_{KR\text{-}W}}{I_{KR}}$ is on the order of 1.7. This ratio results in a loss of tolerance in coincident current operation in comparison with a standard toroid.

Shmoo $I_{r\,min} < I_r < 1.7\ I_{KR}$

Toroid $I_{r\,min} < I_r < 2\ I_{KR}$

Obviously, steps must be taken to prevent this from occurring in a memory system.

The effective path length between the read hole and the write hole may be altered by passing a current through the write hole in the clear direction during the presence of the read pulse. The magnitude of this current must always be less than I_{KW} in order not to affect the flux surrounding the write hole.

This current may either be in the form of a pulse or a DC bias. The pulse is more desirable as DC current presents another problem during the set pulse if the magnitude of the bias is too large.

The pulsed current may be mechanized by either pulsing the clear line in the presence of the read current pulse, or by re-entering the read hole drive line through the write hole.

seven-wire system

In the seven-wire system, each core is threaded in the following manner:

Write Hole	*Read Hole*
1. Clear winding	1. X drive line
2. Inhibit winding	2. Y drive line
3. X drive line	3. Sense winding
4. Y drive line	

The X and Y drive line configuration is shown in Figure 6. Notice that the Y drive line through the read hole re-enters the write hole of the same core. The purpose of this is to increase tolerances while guarding against the unblock condition previously discussed.

The X drive line through the read hole re-enters the write hole on an adjacent line.

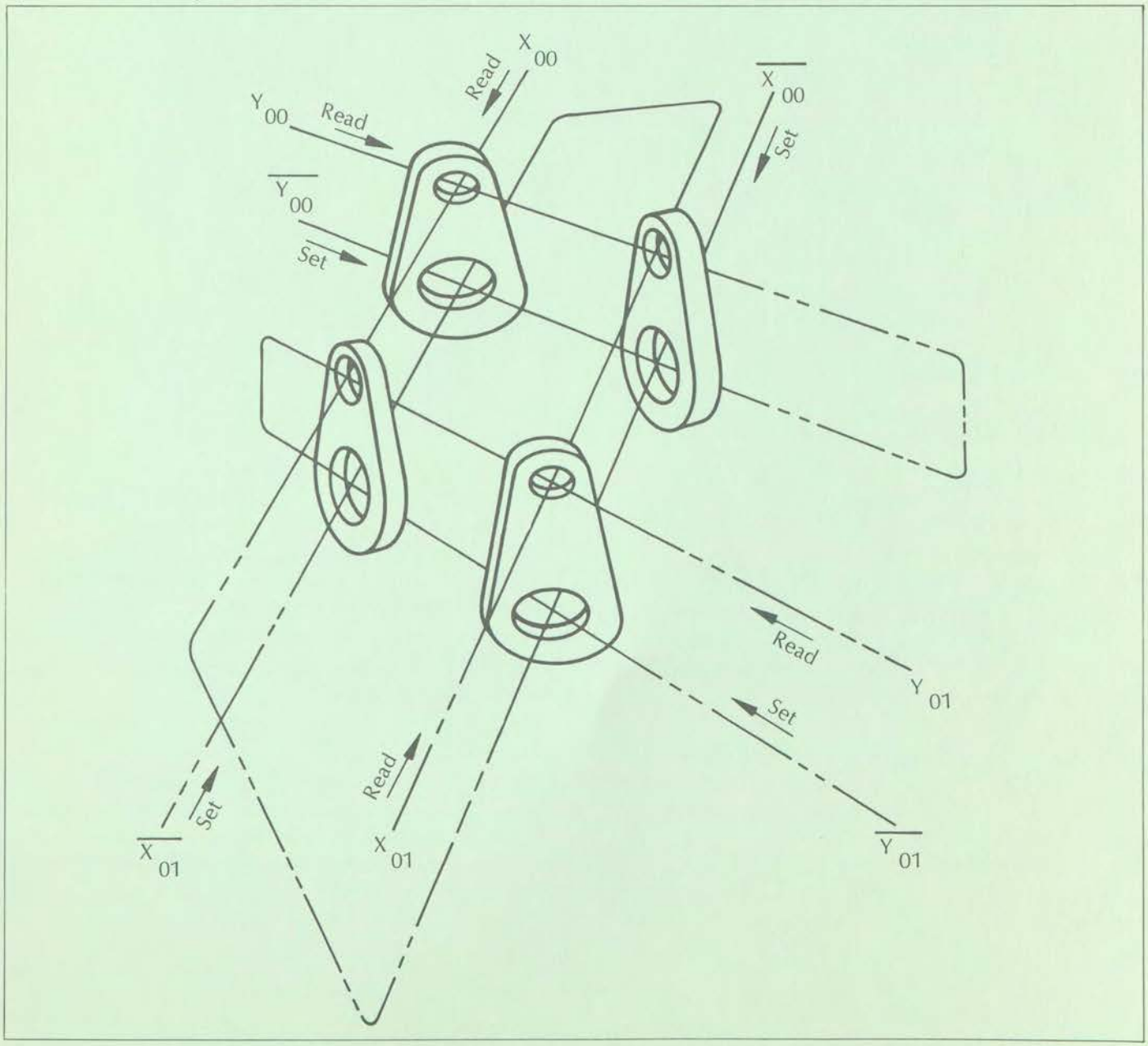
The clear winding is made common to certain sections of the memory stack. For example, for a 4096 x 12 memory stack, there could be four 1024 x 12 clear sections. This is done in order to compromise between clearing one word at a time (word organized), and having to clear all locations at one time.

The design of EMI's "Shmoo" transfluxor was based upon certain considerations given to an electrically alterable NDRO memory system. Among these considerations was that for an airborne type computer, the information contents would be changed infrequently relative to the number of read cycles performed. From a system standpoint, the writing of information into the memory would generally be accomplished on the ground and would be done in blocks of words. Hence, the advantage of an NDRO system would best be utilized when writing information was performed only on the ground, and the clear operation was more practical when divided into discrete sections of the memory rather than one word at a time.

The inhibit and sense windings, although in separate holes, are threaded in the same manner as in a conventional toroid core memory stack.

The advantage of the seven-wire system is that the same drive lines and drive circuitry may be used for both the read and write modes of operation.

figure 6. drive line configuration



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CORE MEMORY STACK
APPLICATION NOTE NO. 638

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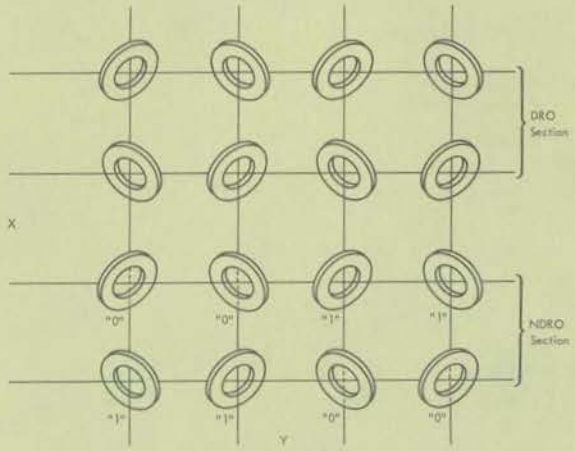


TYPICAL X AND Y DRIVE LINE WIRING FOR DRO AND NDRO SECTIONS

"0" cores in NDRO section are not threaded by a Y drive line.

COMBINATION FIXED PROGRAM NDRO AND DRO SCRATCHPAD CORE MEMORY STACK

FEATURES

For applications where fixed program NDRO and DRO scratchpad memories are desired, this type of stack has the following advantages:

Coincident Current Selection

No additional circuitry is required for operation of the NDRO section.

Presently, computers having both fixed program NDRO and DRO scratchpad memories typically use two systems, such as a rope memory and a core memory. Each system requires entirely different selection and drive circuitry. When NDRO and DRO storage are combined into a single stack utilizing coincident current selection, overall circuit complexity is drastically reduced.

High Reliability

The NDRO program is permanently wired; therefore, loss of information resulting from external circuit and/or power failure is not possible.

Fast Cycle Times

Cycle times are compatible with conventional 4 wire DRO coincident current core memory stacks utilizing the same core type.

Low Volume

The volume is identical to that of a conventional 4 wire, coincident current core memory stack of the same storage capacity.

Low Power

Power requirements are less than those of a conventional 4 wire stack of the same storage capacity and the same core type.

Ruggedized Construction

The stack operates over a wide temperature range of -55°C to +100°C. It is suitable for military and space environments.

Low Cost

The cost is lower than other solutions to this type of application.

CONSTRUCTION

The ratio of NDRO to DRO storage capacity is virtually unlimited. For the purpose of simplicity, a stack of 4,096 words of N bits, equally divided into 2,048 words of NDRO and 2,048 words of DRO, is used to illustrate the wiring.

DRO Section

1. 32 X lines
2. 64 Y lines
3. Standard diagonal type sense winding for each of the N bits.
4. Standard inhibit winding passing through 2,048 cores parallel to the X drive lines. One inhibit winding is required for each of the N bits.

NDRO Section

1. 32 X lines, each of which threads all cores on a given drive line.
2. 64 Y lines, each of which threads only those cores containing a "1". The Y drive lines are common to both the DRO and NDRO sections of the memory.
3. Standard diagonal type sense winding. The sense winding is also common to both the NDRO and DRO sections of the memory.
4. No inhibit line is required, as the NDRO section contains permanent information.

OPERATION

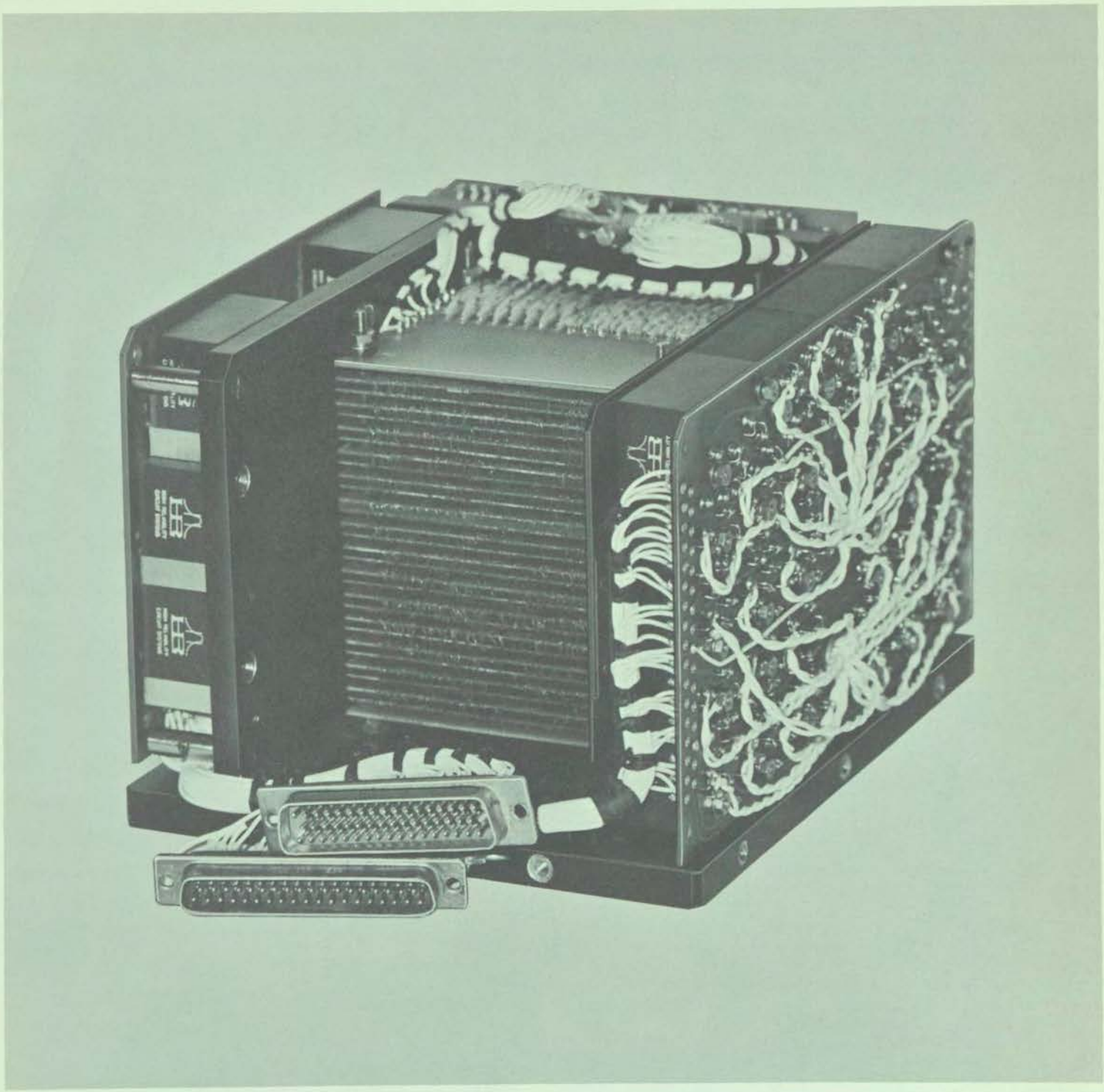
The operation of the stack is essentially identical to any coincident current core memory stack. The same type and number of drive and sense circuits, as well as address and data registers, are used.

The NDRO section operates on the principle that only cores containing a "1" receive a full current pulse when selected, whereas the "0" cores are limited to a half current pulse because of the nature of the Y drive line wiring.

PERFORMANCE

The performance of the stack over a wide temperature range of -55°C to +100°C is excellent. High signal-to-noise ratios in conjunction with wide drive current tolerances are obtained even under worst case pattern conditions.

Further details may be obtained upon request.



SEMS-3R AEROSPACE CORE MEMORY SYSTEM

Capacity:	256 to 4096 words / 4 to 28 bits per word
Speed:	4.5 μsec cycle time
Temperature Range:	−55°C to +100°C or −25°C to +75°C
Size:	4½" x 5¾" x 6¾"
Volume:	175 cubic inches

Meets MIL shock, vibration and humidity specifications

electronic memories inc.

12621 Chadron Avenue, Hawthorne, California

THE SEMS-3R

Volume: 175 cubic inches.

Capacity: 4096 words of 28 bits.

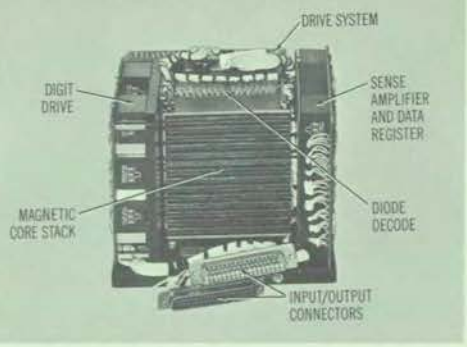
Speed: Access time less than 1.0 microseconds; 220,000 Random Memory cycles per second. Cycle time less than 4.5 microseconds.

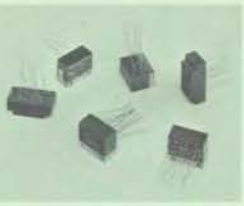
Environments: MIL-E-5400, MIL 16400E, MIL 4158B.

The SEMS-3R allows severe environment control and guidance systems designers to put a fast, rugged, large capacity core memory system into tightly restricted space. The memory system is available in a range of word capacities and bit sizes. The SEMS-3R is available in two operating temperature range versions for maximum applications economy.

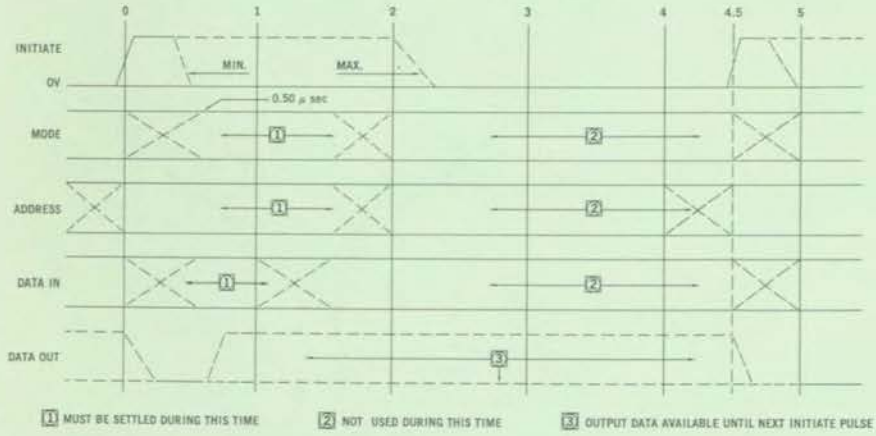
The SEMS-3R is designed specifically for airborne, satellite, shipboard and ground based applications where high reliability, low weight and volume, minimum power and high speed are required design criteria.

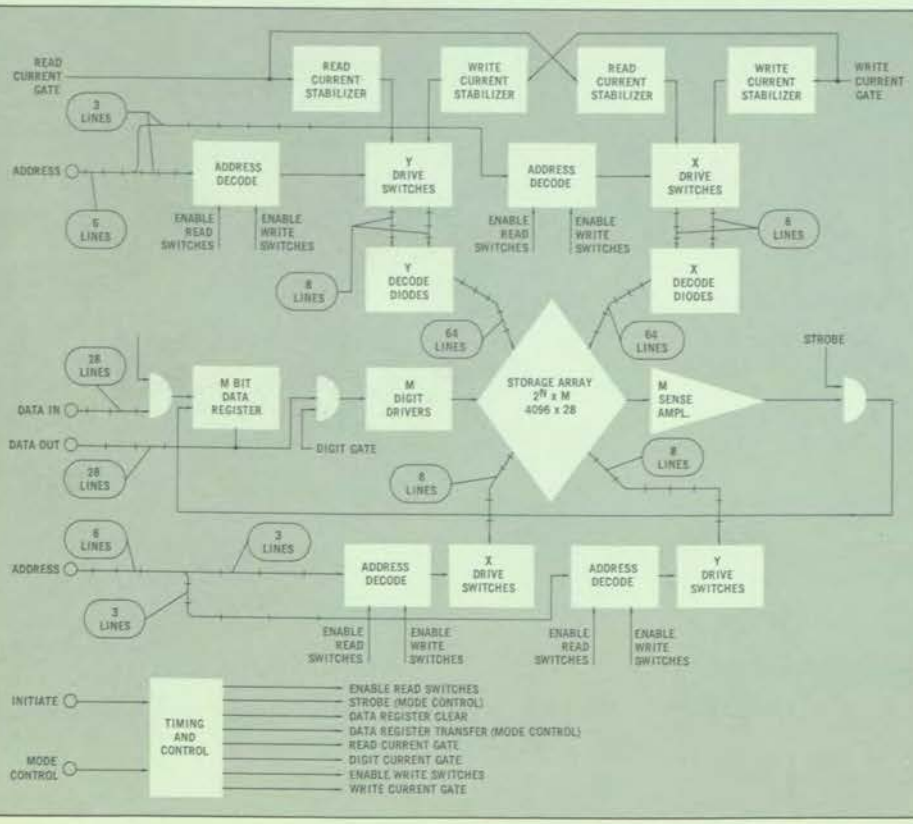
TYPICAL SEMS-3R SYSTEM





TIME IN MICROSECONDS





SPECIFICATIONS

Storage Capacity	256, 512, 1024, 2048, or 4096 words by 4 to 28 bits (in 2 bit increments)
Operating Temperature	−55°C to +100°C or −25°C to +75°C
Storage Temperature	−65°C to +125°C
Altitude	70,000 ft., or higher at slightly reduced upper temperature limits
Read/Restore Cycle Time	4.5 μsec.
Clear/Write Cycle Time	4.5 μsec.
Access Time	Less than 1.0 μsec.
Operating Rate	0 to 220 Kc
Input Signal Levels	Binary 0 = 0 to 0.5 V Binary 1 = +4 V to +7 V
Output Signal Levels	Binary 0 = 0 to 0.25 V Binary 1 = +5 V to +6.5 V
Input Currents	
A. Address	3 ma. max. for 1.5 μsec. if line is in + state; 0 ma. if line in 0 state
B. Mode Control	0.4 ma. in 0 state (CLEAR/WRITE), 0 ma. when in + state (READ/RESTORE)
C. Information	0 level — no current required ± level — less than 1.0 ma.
D. Initiate	0 level — no current required + level — less than 1.0 ma.
E. Edge Current	In addition to the logic current required, approximately 9.0 ma. of edge current must be supplied to charge a capacity of approximately 200 μμf to effect a change from one logic level to another level within 100 nanoseconds
Output Current	
Information Lines	0 level — 0 current + level — 5.0 ma.

Input Signal Characteristics	Rise Time (μsec.)	Width (μsec.)
A. Address	.1	1.5 min.
B. Initiate	.1	0.2 to 2.0
C. Information Lines	.1	1.0 min.
D. Mode Control	level	level
Output Signal Characteristics		
Information	.1	2.0 min.

Power Req'mt (4096 x 28)	35 watts for 4.5 μsec. cycle time
Voltages Required	+15, +6, −3
Volume (4096 x 28)	175 cubic inches
Weight (4096 x 28)	8 lbs.
Form Factor (4096 x 28)	Length = 6.75; Width = 5.79; Height = 4.45
Applicable Mil Specs	MIL-E-5400, MIL 16400E, MIL 4158B, MIL-Q-9858
Vibration and Shock	Per applicable mil spec
Type of Packaging	Welded circuit modules and encapsulated magnetics

Word capacities to 8192 and bit length to 56 are available for special requirements.

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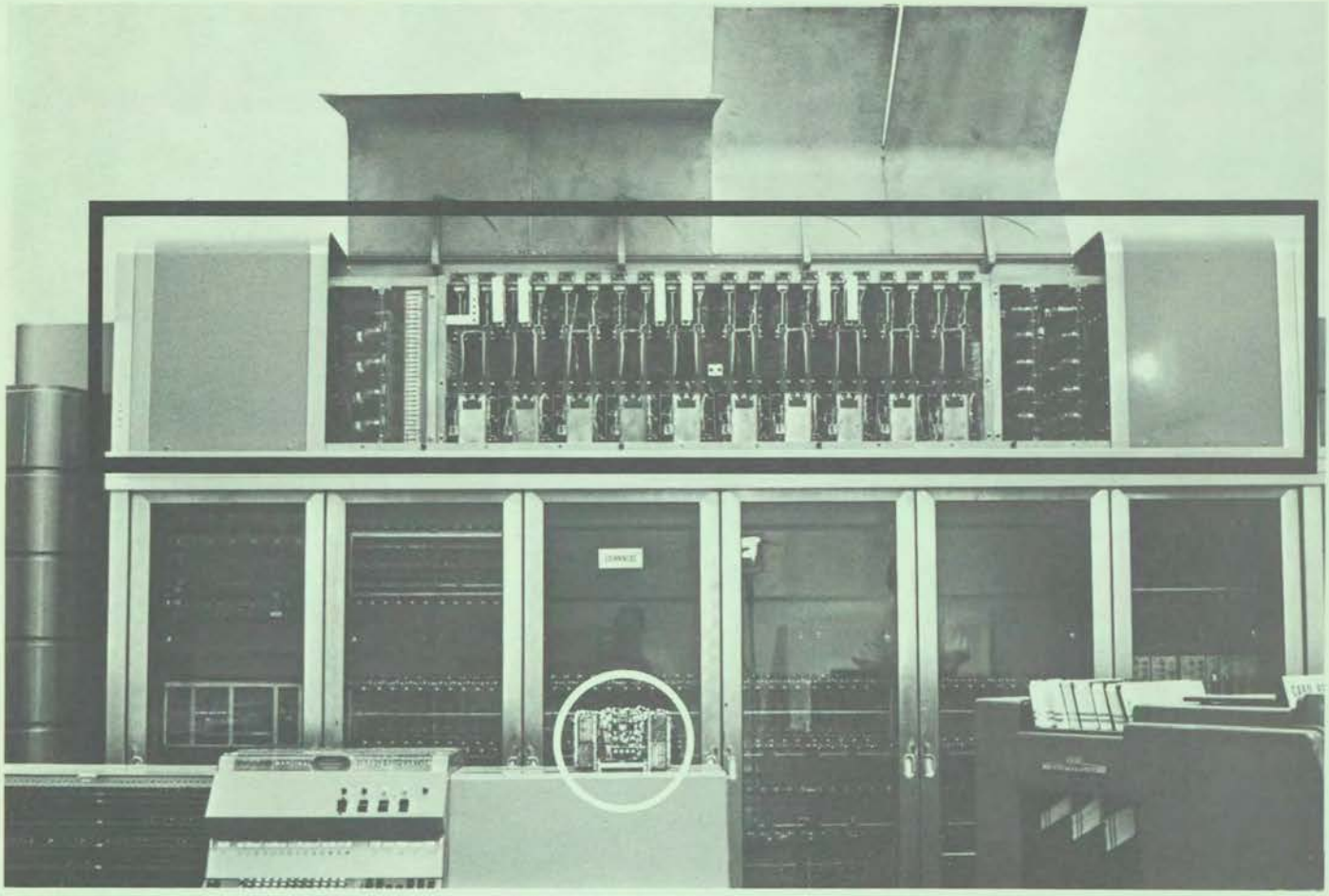
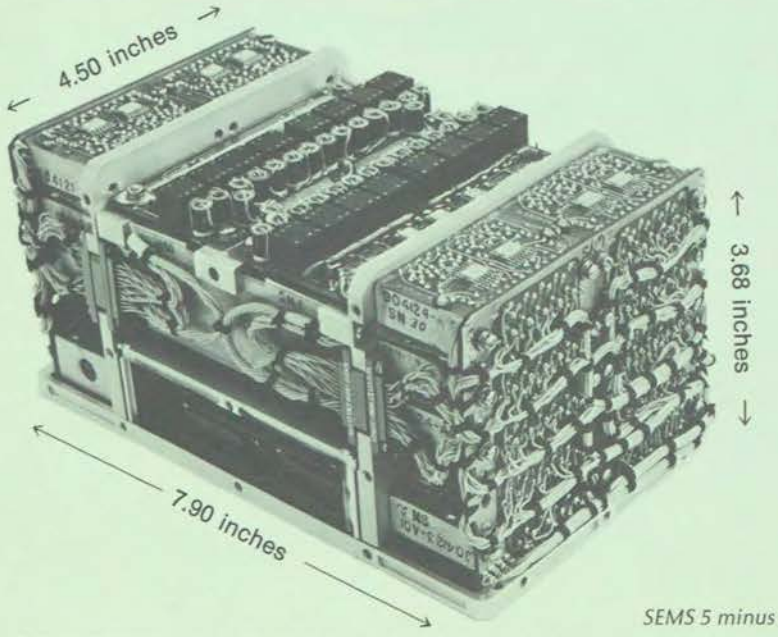
core memory development 1955-1967

The small white box is SEMS 5 (Severe Environment Memory System), 7 pounds of militarized core memory which stores as much data as the historic 800-pound, 1955 unit behind it, which is the first commercial core memory ever built. Each contains 4,096 words of comparable lengths. Electronic Memories personnel instrumental in the design of both offer you a somewhat nostalgic comparison of their characteristics, to underline the strides core memories have made in 12 years.



The tiny SEMS 5 core memory (circle) sits in front of the JOHNNIAC computer. Only the height and width of JOHNNIAC'S core memory are shown (outlined portion). The historic memory has a depth of nearly six feet and occupies the entire top portion of the computer.



SEMS 5 minus its cover, to show integrated circuit construction.

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A slightly nostalgic comparison of the first commercial core memory ever built—and some of its eccentricities—with a 1967 version, the SEMS 5.

Name	JOHNNIAC MEMORY – 1955	SEMS 5 MEMORY – 1967
distinction	First commercial core memory ever built. 1955-1967.	Smallest commercial core memory ever built with a storage capacity comparable to Johnniac's.
	Preceded only by experimental core memories built at Massachusetts Institute of Technology.	Only standard core memory for severe environment applications in production.
age	12 years old.	Just over one year old.
history	Installed 1955 in the JOHNNIAC computer at RAND Corp., Santa Monica, Calif. Retired February 1966 with full honors to the Los Angeles County Museum after 53,000 hours of operation.	Introduced for military and aerospace applications by Electronic Memories, November 1965.
amount of information stored	4,096 computer words, each 40 bits long.	4,096 computer words, each 32 bits long.
weight	800 pounds.	6.9 pounds. 1/115th Johnniac's weight.
size	105 cubic feet.	1/13th of a cubic foot. 1/1000th Johnniac's size.
power requirement	15,000 watts.	60 watts. 1/250th Johnniac's power. No more than used by an ordinary light bulb. 6 watts standby.
speed		
access time	15 microseconds.	700 nanoseconds. 21 times faster.
cycle time	15 microseconds.	2 microseconds. Nearly 8 times faster.
split cycle	None.	2.4 microseconds (optional).
required temperature environment	Earned the nickname "Pneumoniac" because it worked only when the temperature was a cool 44°F (13.5°C). 8 tons capacity of air conditioning was installed to maintain this temperature.	Operates unaided in temperatures as brisk as 65°F below zero to a hot 185°F (−55°C to +85°C).
eccentricities about working conditions	The computer was afraid of the dark. Fluorescent nightlights were installed when it refused to operate properly after room lights were turned off. In spite of this temperature failing, Johnniac introduced a new order of reliability and performance.	None. Operates under severe shock, vibration and humidity conditions as defined by applicable portions of military specifications MIL-E-5400, MIL-E-4158, and MIL-E-16400.
voltages required	8 types: −550V, −300V, −200V, −150V +110V, +150V, +300V, +450V	3 types: +15V, +5V, −5V
type	Coincident current; parallel; random access.	Coincident current; parallel; random access.

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sems 5
severe environment
military aerospace memory

electronic memories

- fast: 2 μsec cycle time
- small: 132 cubic inches
- mil-spec reliability: MIL-E-5400, MIL-E-4158, MIL-E-16400
- minimum weight and power: 6.9 lbs., 60 watts
- large storage capacity: 4092 x 32

sems 5 military and aerospace memory

SEMS 5 (Severe Environment Memory System) is a very small, very fast militarized core memory. It is specifically designed for severe environment applications. Reliability, high speed, wide operating margins and minimum power, weight and size are optimally combined in a tightly packaged unit small enough to hold in one hand.

The system is a standard, production-line memory. It is now being delivered for tough airborne, missile, space, ship and ground applications. These include:

- satellites
- avionics
- military land vehicles
- military aircraft
- antisubmarine warfare
- fire control systems
- electronic countermeasures
- display systems
- guidance systems
- navigation systems
- airborne computers

severe environment reliability

The ability of SEMS 5 to withstand severe vibration, shock, humidity and temperature extremes makes it the most rugged memory system available.

SEMS 5 is capable of taking 10 g's as defined by MIL-E-5400 of vibration, and has passed tests up to 30 g's.

It operates over temperatures ranging from 65 degrees below zero to 185 degrees above (−55 to +85°C).

The unit meets applicable portions of military specifications MIL-E-5400, MIL-E-16400, and MIL-E-4158, for vibration, shock and humidity in aircraft, ship and ground applications.

speed, storage, size and power

SEMS 5 has a cycle time of 2 microseconds and an access time of 600 nanoseconds. The standard SEMS 5 stores 4,096 words of 32 bits each. Optional storage capacities are available from 256 to 16,384 words of 8 to 32 bits long.

The standard SEMS 5 weighs 6.9 pounds. It measures 4.50 wide by 3.68 high by 8.0 inches long, and has a total volume of 132 cubic inches.

Power consumption is less than 60 watts at maximum worst case dissipation, and only 6 watts on standby.

Voltage requirements are minimal: +15V, +5V, and −5V. Internal tantalum by-pass capacitors store sufficient energy to complete a full memory cycle without fault in the event that supply current is interrupted at initiate time.

Except in the final drive switch stage and current stabilizers, integrated circuitry is used throughout the system, in logic, sense amplifiers, address decoders, and data and address registers.

operating modes

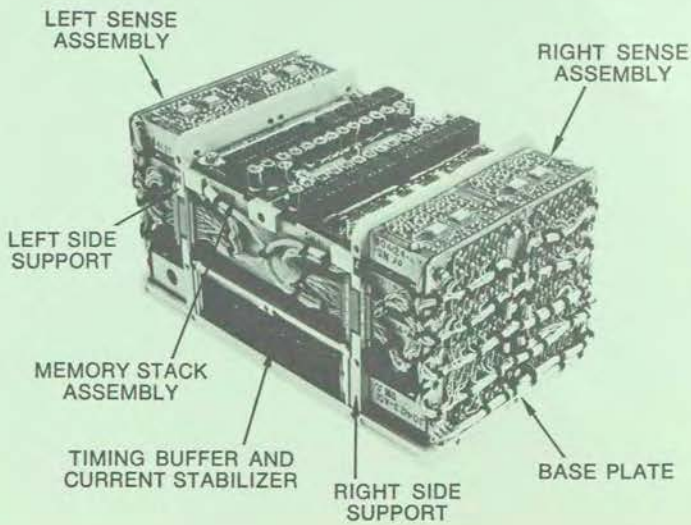
Both clear/write and read/restore are standard modes. A read/modify/write split cycle and a buffer cycle are optionally available.

Logic interface is TTL positive true. The input signals are measured from the leading edge of initiate.

memory stack reliability

To increase reliability, SEMS 5 employs an unusual magnetic organization. Each coincident current plane contains eight bits instead of the usual one. Only three wires instead of the normal four are used, with a common line performing both sense and inhibit functions. This organization eliminates a significantly large number of electrical interconnections, which are a common source of memory stack failure.

A proprietary stack technique provides exceptional thermal characteristics. It minimizes accessory cooling equipment by dissipating heat through built-in conduction cooling. Because conduction cooling allows components to operate at comparatively cool temperatures, stack reliability and operating life are enhanced.



options

Power supplies and a memory exerciser are optionally available. Split (read/modify/write) and buffer cycles, and extended or reduced storage capacities are also available.

SEMS 5 can be modified to meet specialized operating environments, unusual storage specifications, or other requirements. In the past systems have been built to operate during 2,000 g's of shock for one millisecond and 27 g's of random vibration. Capacities have been extended to a 40-bit word length, and telemetry link interface circuitry can be provided.

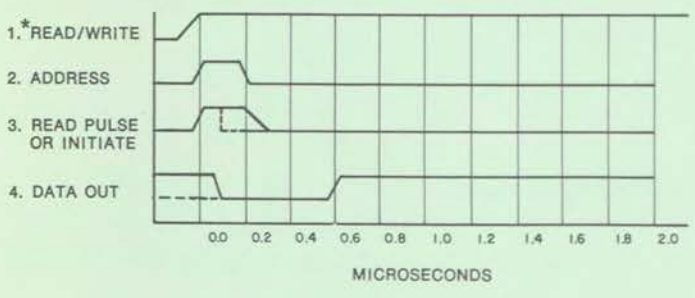
SPECIFICATIONS

Speed	600 nanosecond access time 2 microsecond cycle time (2.1 split cycle)
Storage Capacity	4,096 words of 32 bits each, standard. 256 to 16,384 words from 8 to 32 bits each, optional.
Shock, Vibration & Humidity Resistance	Meets applicable portions of MIL-E-5400, MIL-E-4158, and MIL-E-16400. Also MIL-Q-9858.
Operating Temperature Range	−55°C to +85°C (Base Plate)
Volume & Dimensions	132 cubic inches, 4.50 x 3.68 x 8.00 inches.
Weight	6.9 pounds. (4,096 words x 32 bit capacity)
Power Consumption	60 watts maximum all zero pattern at 2 microseconds cycle time, 6 watts standby.
Voltage Requirement	+15V ± 5%, +5V ±5%, −5V dc ±2%. Voltages may be applied in any sequence.
Operating Modes	Clear/write and read/restore, standard. Split cycle (read/modify/write) and buffer cycle, optional.
Input/Output Signal Levels	TTL logic positive true (Sylvania SUHL)
Input Signal Access	Memory access is by initiate and read/write mode lines, or by separate read and write pulse inputs.
Optional Equipment	Power supplies Memory exerciser

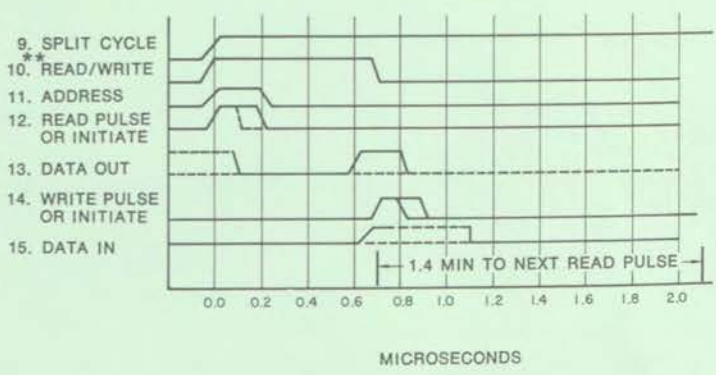
mode timing

Read/write control	Must be stable at time 0.0 and remain so until initiate returns to 0 volt level.
Address	Must be stable from time 0.0 to 0.2 microsecond.
Initiate (read and write)	0.1 minimum microsecond, 0.2 maximum microsecond duration.
Data Out	Access time 0.6 microsecond.
Data In	Must be stable from 0.3 to 0.85 microsecond.
Split Cycle-Write	Pulse duration time can occur any time after time 0.0 to 0.7 microsecond. Next read pulse cannot occur sooner than 1.4 microseconds after leading edge of write pulse. Minimum full split cycle time is 2.1 microseconds.

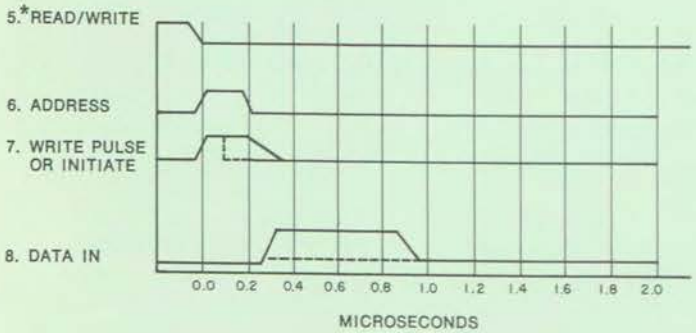
READ/RESTORE MODE



SPLIT CYCLE MODE
(read/modify/write)



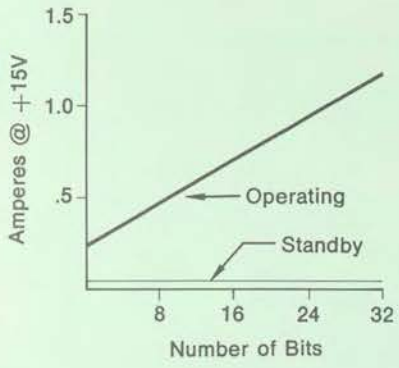
CLEAR/WRITE MODE

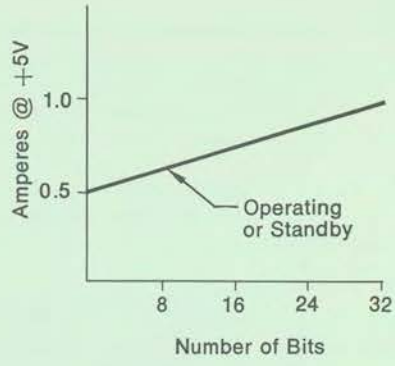


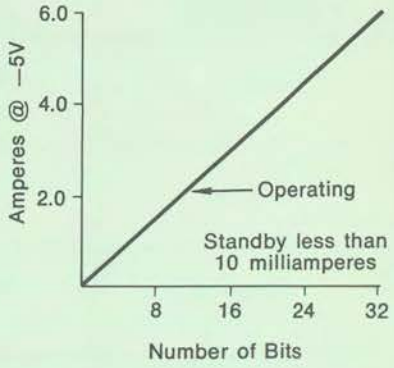
*Option can be high or low.

**Split cycle operations may be activated by Read pulse. Write pulse without a R/W mode line, or by an Initiate pulse and a R/W line. When the R/W line and Initiate signals are used, the mode signal must be settled before the leading edge of Initiate pulse for each half-cycle operation.

typical currents



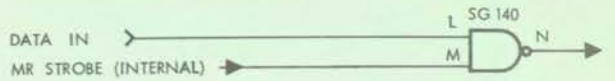
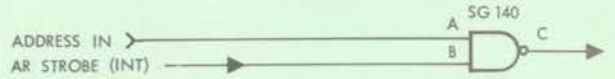
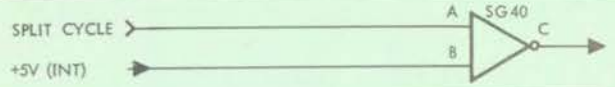
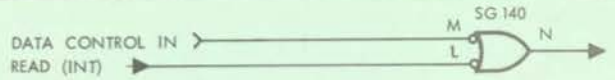
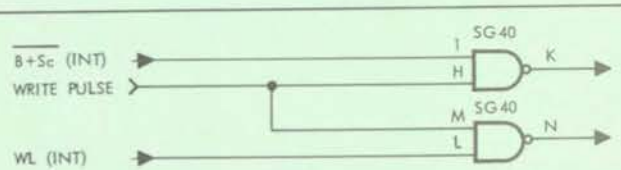
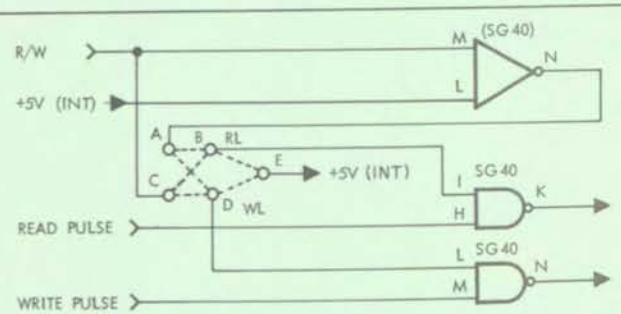
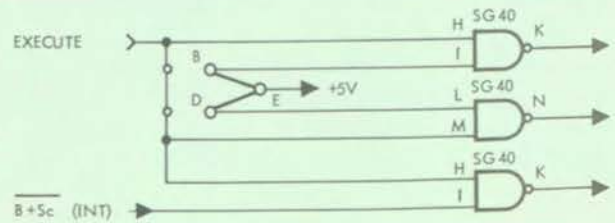
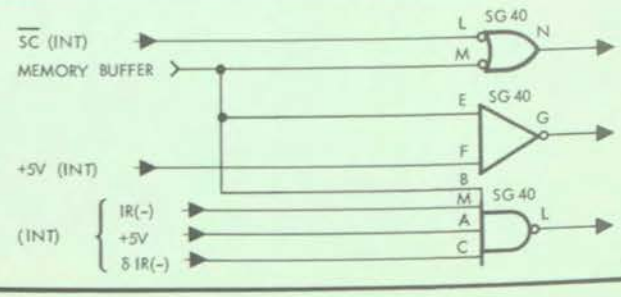




Currents shown are for operation @ +25°C; 2 microseconds cycle time; read restore mode; reading all zeros from memory.

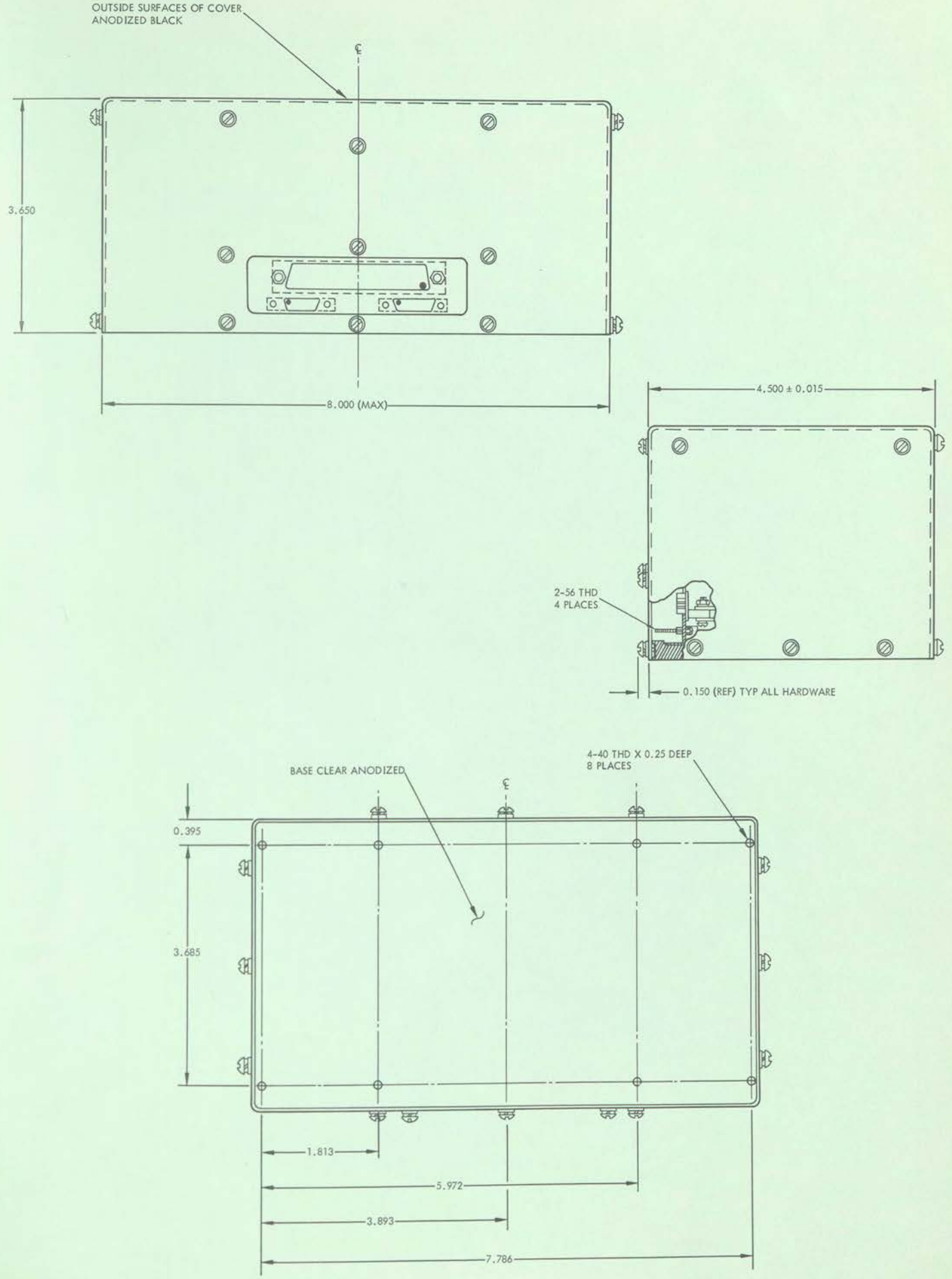
interface connection data

Pin Number	Connector		
	J1	J2	J3
1	Address 2^6	Data In 2^0	Data In 2^2
2	Address 2^8	Data In 2^1	Data In 2^3
3	Address 2^{10}	Data In 2^4	Data In 2^6
4	Read Pulse	Data In 2^5	Data In 2^7
5	Spare	Data In 2^8	Data In 2^{10}
6	Data Control	Data In 2^9	Data In 2^{11}
7	—5V	Data In 2^{12}	Data In 2^{14}
8	+5V	Data In 2^{13}	Data In 2^{15}
9	OV	Data In 2^{16}	Data In 2^{18}
10	OV	Data In 2^{17}	Data In 2^{19}
11	OV	Data In 2^{20}	Data In 2^{22}
12	+15V	Data In 2^{21}	Data In 2^{23}
13	—5V	Data In 2^{24}	Data In 2^{26}
14	Start Read	Data In 2^{25}	Data In 2^{27}
15	Read/Write	Data In 2^{28}	Data In 2^{30}
16	Split Cycle	Data In 2^{29}	Data In 2^{31}
17	Address 2^4	Data Out 2^0	Data Out 2^2
18	Address 2^2	Data Out 2^1	Data Out 2^3
19	Address 2^0	Data Out 2^4	Data Out 2^6
20	Address 2^7	Data Out 2^5	Data Out 2^7
21	Address 2^9	Data Out 2^8	Data Out 2^{10}
22	Address 2^{11}	Data Out 2^9	Data Out 2^{11}
23	Write Pulse	Data Out 2^{12}	Data Out 2^{14}
24	Spare	Data Out 2^{13}	Data Out 2^{15}
25	—5V	Data Out 2^{16}	Data Out 2^{18}
26	—5V	Data Out 2^{17}	Data Out 2^{19}
27	+5V	Data Out 2^{20}	Data Out 2^{22}
28	OV	Data Out 2^{21}	Data Out 2^{23}
29	OV	Data Out 2^{24}	Data Out 2^{26}
30	+15V	Data Out 2^{25}	Data Out 2^{27}
31	—5V	Data Out 2^{28}	Data Out 2^{30}
32	Spare	Data Out 2^{29}	Data Out 2^{31}
33	Spare		
34	Memory Buffer		
35	Address 2^5		
36	Address 2^3		
37	Address 2^1		

INPUT-OUTPUT DESCRIPTION	INTERFACE CIRCUIT TYPE	CIRCUIT
DATA IN	SYLVANIA TTL (SG 140)	
DATA OUT	SYLVANIA TTL (SG 140)	
ADDRESS IN	SYLVANIA TTL (SG 140)	
SPLIT CYCLE	SYLVANIA TTL (SG 40)	
DATA CONTROL	SYLVANIA TTL (SG 140)	
READ PULSE	SYLVANIA TTL (SG 40)	
WRITE PULSE	SYLVANIA TTL (SG 40)	
READ/WRITE (R/W)	SYLVANIA TTL (SG 40)	
EXECUTE	SYLVANIA TTL (SG 40)	
MEMORY BUFFER	SYLVANIA TTL (SG 40)	

NOTE

1. ALL INTEGRATED CIRCUITS ARE SYLVANIA TTL
2. INTEGRATED CIRCUIT TYPE SHOWN IN SYMBOL


OUTSIDE SURFACES OF COVER
ANODIZED BLACK
℄
3.650
8.000 (MAX)
4.500 ± 0.015
2-56 THD
4 PLACES
0.150 (REF) TYP ALL HARDWARE
BASE CLEAR ANODIZED
4-40 THD X 0.25 DEEP
8 PLACES
0.395
3.685
1.813
5.972
3.893
7.786

how sems 5 dissipates heat

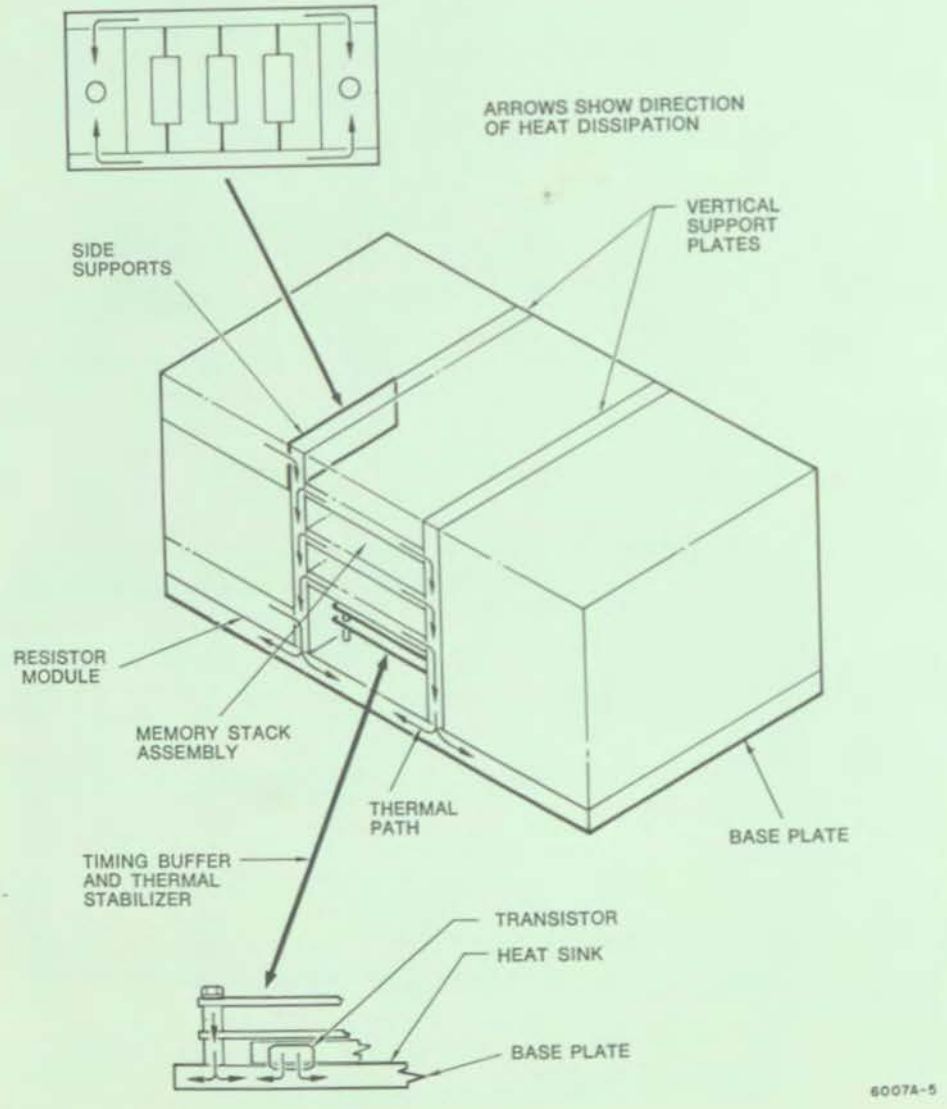
Little or no accessory cooling equipment is required by SEMS 5 because the heat it generates is dissipated by conduction. System reliability is improved because conduction cooling results in lower component temperatures and thus promotes longer operating life. Thermal flow through the memory system is shown in this isometric diagram.

Heat generated by the module components flows to aluminum blocks directly contacting the two side supports at (a). Heat flows from each thin film resistor module pack (b) to the side support it directly contacts. From the side supports, heat flows to the base plate (c).

Each array in the core stack assembly (d), both the top and bottom vertical support frames (e), and the side supports located at the four corners and both ends of the memory system, are thermally connected to form a heat dissipation path (f) to the base plate.

The timing buffer and current stabilizer assembly (g) dissipates heat through a number of direct connections to the base plate. Certain assembly transistors are mounted in a heat sink directly contacting the base plate, for additional transfer.

Several simple methods can be used to transfer heat from the system. A larger plate providing adequate thermal transfer can be mounted directly to the SEMS 5 base plate, or an air stream of sufficient flow can be directed at the base plate.



electronic memories
12621 chadron avenue, hawthorne, california 90250
telephone (213) 772-5201

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summary of typical core characteristics

electronic memories

				Typical Operating Conditions at 25°C						
				Pulse Drive Characteristics			Output Signals			
Description	Mils	Type	Size OD/ID/ht (mils)	Amplitude (ma)	Duration (μs)	Rise & Fall Time (μs)	Amplitude ONE (mv)	Amplitude ZERO (mv)	Peak Time (μs)	Switch Time (μs)
Coincident Current	20	22-100	22/14/05	700/350	0.5	0.05	55	5	0.13	0.22
	30	31-103	31/20/07	580/290	0.6	0.1	61	8	0.23	0.37
		31-108	31/20/07	720/360	0.5	0.1	62	5	0.21	0.39
	50	51-106	50/30/15	500/250	1.2	0.2	90	9	0.43	0.75
		51-110	50/30/15	500/250	2.0	0.2	68	8	0.52	1.02
		51-119	50/30/15	400/200	2.0	0.5	90	5	0.75	1.25
	80	81-104	80/50/25	410/205	6.0	0.5	60	6	1.4	2.6
Coincident Current Lithium for Wide Temperature Range Applications	20	24-100	21/14/05	780/390	0.4	0.05	40	4	0.145	0.270
	30	34-102	31/19/10	760/380	0.6	0.1	63	4	0.26	0.49
Coincident Current for 2-1/2D Applications	20	21-104	22/14/04	850/425	0.5	0.05	32	3	0.12	0.20
	30	31-115	29/21/07	750/375	0.5	0.1	52	4	0.21	0.37

				Typical Characteristics at 25°C				
				Saturation flux density (gauss)	Coercive force (oersted)	Curie Temperature		
Switch	100	101-101	100/70/35	2500	0.58	220°C		
	140	141-101	140/90/90	2500	0.35	220°C		
				Saturation flux density (gauss)	Remanent/ saturation flux ratio	Coercive force (oersted)	Initial Permeability	Curie Temperature
Linear	180	183-101	175/88/95	—	0.5	0.3	1800	170°C
	180	183-102	175/88/95	—	0.33	0.3	1400	220°C

definitions

$I_f(I_m)$ = Full current. The magnitude of the full drive currents I_r and I_w used at any time.

I = Drive current pulse amplitude.

I_{os} = Overshoot. The extent to which the maximum instantaneous current exceeds the current pulse amplitude, I, expressed as a percentage of I.

I_w = Write current pulse. Value of I to switch core from the ZERO to ONE state.

I_r = Read current pulse. Value of I to switch core from the ONE to ZERO state.

I_{pw} = Partial write current. A current pulse of the proper polarity to attempt to drive the core to the remanent "one" state, but with insufficient magnitude to cause significant irreversible flux switching.

I_{pr} = Partial read current. A current pulse of the proper polarity to attempt to drive the core to the remanent "zero" state, but with insufficient magnitude to cause significant irreversible flux switching.

$I_k(I_b)$ = Knee current. Value of I_{pw} required to reach the switching threshold of the non-recoverable flux.

$\frac{I_k}{I}$ = Disturb ratio.

t_o = Reference time. Time I reaches 10%.

T_r = Rise time of I from t_o to 90%.

T_d = Pulse duration. Time I remains above 90%.

T_f = Fall time of I from 90% to 10%.

t_p = Peaking time. Time between t_o and when output reaches peak of uV_1 or dV_1 response.

C_f = Temperature coefficient of full current. The change in I_f required to maintain a constant amplitude of uV_1 as the temperature varies.

$$C_f, \text{ ma/°C} = \frac{(I_f @ T_1) - (I_f @ T_2)}{(T_2 - T_1)}$$

where:
T_1 = lower temperature, and
T_2 = upper temperature

t_s = Switching time. Time between t_o and the decrease of output voltage to 10% of uV_1 or dV_1 response.

uV_1 = Peak output voltage when I_r is applied to a core in the undisturbed ONE state.

dV_1 = Peak output voltage when I_r is applied to a core in the disturbed ONE state.

dV_z = Peak output voltage when I_r is applied to a core in the disturbed ZERO state.

I_{reset} = I of sufficient amplitude and duration to switch a core to its saturated state.

I_{set} = I required to drive a core from a remanent state toward the opposite saturation state.

I_{read} = I of sufficient amplitude and duration, and opposite I_{reset} direction, to switch the core to the alternate saturated state.

H_c = Coercive force. Equivalent to I and of defined duration necessary to bring the flux density of the core to zero.

H_{mv} = Switch core output, measured in millivolts, at the ouput of an integrator with a time constant of 10 μs ± 1% (I/e value) when I_{read} is applied. A stable point in the high permeability region of switching, close to H_c.

ψ/t = Switch core flux output, measured in millivolts, at the output of an integrator with a time constant of 10 μs ± 1% (I/e value) when I_{read} is applied.

B_s = Saturation flux density.

B_r = Remanent flux.

t_c = Curie temperature.

C_b = Temperature coefficient of break current. The change in I_b for a change in temperature with I_f maintained constant, C_b, ma/°C $= \frac{(I_b @ T_1) - (I_b @ T_2)}{(T_2 - T_1)}$

where:
T_1 = lower temperature, and
T_2 = upper temperature.

quality control

Cores are delivered 100% tested to mechanical and electrical specifications or to statistical quality level of AQL 0.015 or 6.5 as defined by MIL-STD-105D, Inspection Level II. Cores are electrically tested as defined by the test specification.

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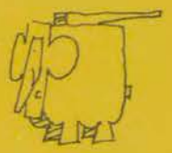
How to build a flying, bouncing, submerging memory system

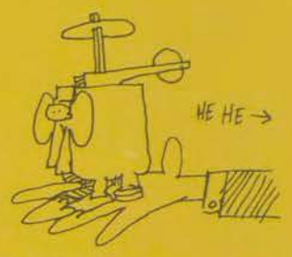
Start with one large-capacity memory (A & B). Make it rugged enough to meet mil-specs. Versatile enough to survive severe environments. A beast.



2. Prepare for take-off. Attach powerful engine (C), barber-type pole (D), lifter-upper blades (E). (To lift-her-upper, of course.) Insert stabilizing blades (F). (They won't stabilize anything, but they'll keep the flies away.)

3. Secure to dive. Fasten swim fins (G), face mask (H). (If Lloyd Bridges can have them, so can your mammoth memory system.)

4. Get ready to roll. Attach shock and bounce-resistant springs (I) to rear feet. (Handle with care after Munson road test. Some mammoth memory systems just go to pieces at this point.)



5. All finished. Sit back. Chuckle. Call Electronic Memories Inc. Ask about flying, bouncing, submerging SEMS memory systems.

If there's no room for a mammoth memory on your desk, take it home for your children to enjoy.

SEMS—1R Memory

Capacity:	256 to 4096 words of up to 32 bits
Speed:	4.5 μsec cycle time 1.0 μsec access time
Temperature Range:	−55°C to +100°C or −25°C to +75°C
Size:	12.25" x 6.37" x 4.87"
Volume:	380 cubic inches

SEMS—2S Memory

Capacity:	5005 bits to 150150 bits (serial)
Speed:	10 μsec cycle time
Temperature Range:	−55°C to +100°C or −25°C to +75°C
Size:	variable depending on number of bits
Volume:	45 to 120 cubic inches

SEMS—3R Memory

Capacity:	256 to 4096 words of 4 to 28 bits
Speed:	4.5 μsec cycle time 1.0 μsec access time
Temperature Range:	−55°C to +100°C or −25°C to +75°C
Size:	4.50" x 5.75" x 6.75"
Volume:	175 cubic inches

SEMS—4R Core Memory

Capacity:	256 to 8192 words of 6 to 40 bits
Speed:	4 μsec cycle time, 1 μsec access time
Temperature Ranges:	−40°C to +85°C −20°C to +65°C 0°C to +50°C
Size:	17" x 17" x 7" (19" rack mounting)
Volume:	2023 cubic inches

SEMS memory systems come in a wide range of word capacities and bit sizes. And they're lightweight, compact, fast and highly reliable. Standard models are available off-the-shelf. Custom systems take a little longer. Find out about SEMS. They're real beasts.

One other thing. When you dial (213) 772-5201, ask for the man in charge of mammoth memory systems. That's Dean Knutson.

electronic memories inc.
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computer design

design and application of digital circuits, equipment and systems in computing, data processing and control

DATA STORAGE IN SPACECRAFTS

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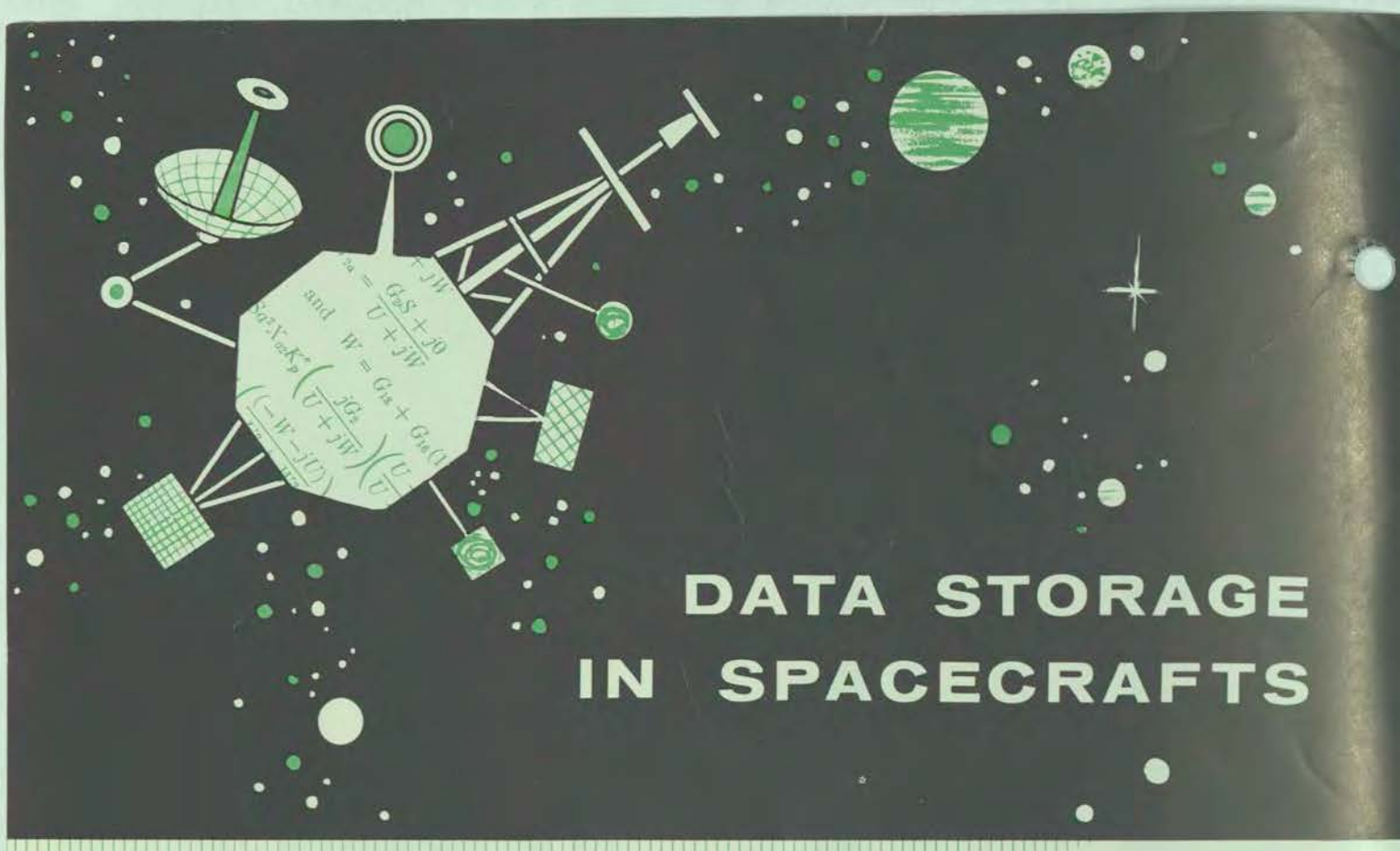


DATA STORAGE IN SPACECRAFTS

ALEX EGGER,
Space Technology Labs, Inc.

WILLIAM S. KNOWLES,
Electronic Memories, Inc.

Designers of spacecraft data storage units have been confronted with the problem of supplying, on the one hand, a rapidly increasing amount of data storage capacity, while on the other, a system which is very small in size, consumes litt' power, and is highly reliable. Less than three years ago the first storage memory was launched into space. This formed a part of the STL digital telemetry unit (Telebit) which was flown on Explorer VI and later on Pioneer V. The capacity of the memory, which used transistors as memory elements was 120 bits. Weight of the memory was five pounds, the volume 150 cubic inches, and the power consumption approximately 1.2 watts. Based on a paper presented at the 1962 National Telemetering Conference, this article describes a data storage unit that has a storage capacity of 10,000 bits and yet weighs far less than the memory of Telebit, is much smaller, and consumes less power.

In addition to high data capacity, small size, and low weight, this data storage unit appears to offer advantages over the other types of storage units available for space applications. As a static type of data storage unit, it appears to be more desirable in terms of low power consumption, reliability, and long life than systems requiring mechanical motion, such as tape recorders. And, unlike certain static storage devices, such as transistor memories, no loss of stored data occurs in the event of temporary power failure. This system consists of a highly reliable magnetic core storage unit utilizing a unique organization of core access circuits.

DESIGN CONSIDERATIONS

Typically the problem of achieving a magnetic core memory has revolved around the inefficiency in the peripheral or access equipment. The size of the memory plane has not been a central problem area. Organization techniques in the past have leaned toward the use of decoding and addressing requiring many active elements. The result has been large weight and volume, high power consumption, and low reliability. A careful examination of the properties of cores, plus organization techniques, allows the circuit designer to also exploit magnetic cores for the access circuits and overcome these shortcomings. In addition, the use of magnetic cores in the access circuits minimizes the number of transistors required and thus increases system reliability.

If a large number of cores must be utilized, a square matrix arrangement provides the most efficient access technique. For n cores in a square matri the two selection coordinates each number $(n)^{1/2}$. For example, in a 10,-

Until recently, the use of ferrite core memories has been confined to the high speed computing field. Here are the system design concepts behind the development of a satellite memory that fully exploits the advantages of magnetic cores.

000-bit memory, the two sets of selection coordinates number 100 lines each.

Prior to discussing the access logic and organization, it is desirable to consider the specific organization of the memory. There are various approaches to devising a magnetic core memory. One of the simplest approaches is to use single aperture square loop ferrite cores in a matrix as previously stated and use coincident current selection; that is, each coordinate supplies a current half the magnitude of the total current required to switch the core. The selection process is based upon the coincidence of two coordinate lines and the nonlinear characteristics of the square loop ferrite core. Another approach is to use a word organized memory which requires external decoding to select the group of bits – defined as a word. This approach does not make use of the nonlinear characteristics of the core in the decoding or selection process and, therefore, requires a much greater quantity of external decoding equipment.

Multiaperture cores could be used but suffer from several drawbacks. First, the magnetic core must be larger and therefore requires more power for switching. Next, the wiring of the planes becomes more complex than that of the simpler single aperture core because of the number of wires and the non-orthogonal threading which must be used.

Spacecraft data storage systems are generally concerned with communications to and from the ground and therefore the bit serial method of data storage and retrieval is compatible with the bit serial transmission link. In addition, the memory is likely to operate at moderate speeds in the order of hundreds or thousands of bits per second. Thus, the active operating duty factor of the memory is exceedingly small; this coupled with the use of pulsing techniques results in low average power consumption.

MAGNETIC SELECTION

As previously mentioned, the basic component of a coincident core memory is the ferrite core, which has a square hysteresis loop and which is switched by the application of two additive currents from one state to the other. Refer to standard text on magnetics for a typical BH loop of a ferrite core. Normally, the current applied in either of the two drive axes is stabilized to a value somewhat less than the knee of the hysteresis loop, thereby causing no irreversible flux change. Only the core in an array at the intersection of the X drive and the Y drive receives a full select current, thereby experiencing a full flux excursion.

Until recently, the use of this type memory for space applications was not practical because of the temperature sensitivity of the core, which in turn required too critical compensation of the coordinate selection currents. A recent advance in the art has been the introduction of a core material (Ref. 1 and 2) which is far less sensitive to temperature changes than the magnesium-manganese family of cores used during the past decade. This core operates over a temperature range from −55° to +100° centigrade with negligible change in drive current required. Consequently, it is now very feasible to employ the simplicity of the classic coincident current concept for applications requiring wide tolerance to severe environment.

The selection concept for supplying the X and Y coordinate drive currents is based on magnetic current steering switches (Ref. 3) which act to sequentially program the coordinates and steer a precise half select current. In this way only one current stabilizing source is required.

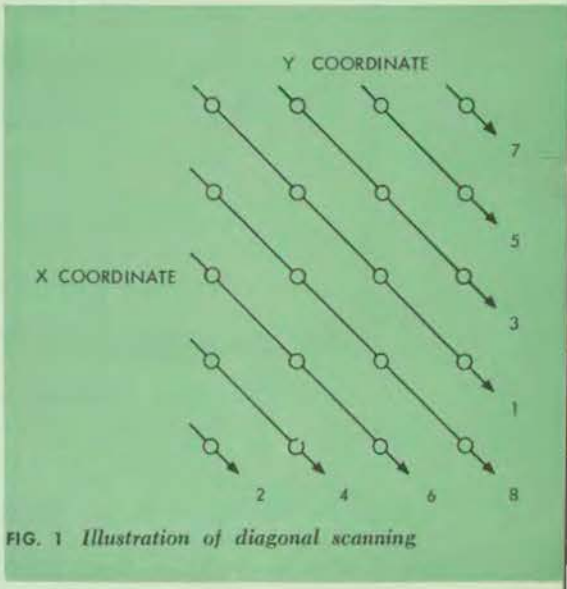


FIG. 1 *Illustration of diagonal scanning*

We will now discuss the access logic for a nominal 10,000 bit storage array using magnetic addressing and selecting. The choice of the exact number of bits in a memory plane is influenced by the method of driving by magnetic switches. In order to eliminate the need for static address registers which would add many components and waste power, as well as lower reliability, the address will be stored by ferrite switch cores. By operating these switches, both coordinates simultaneously, a diagonal scanning pattern of the storage matrix occurs. If the dimensions of the storage unit, as to the rows of cores and columns of cores, are mutually prime, all cores will be scanned before any given diagonal is repeated. Fig 1 illustrates this case for a sample (4 x 5) matrix (two mutually prime numbers). The numbers illustrated are the core scans which are interrogated by simultaneously stepping X and Y selection coordinate rings. Fig 2 shows an example of how to derive a four-coordinate magnetic selection cir-

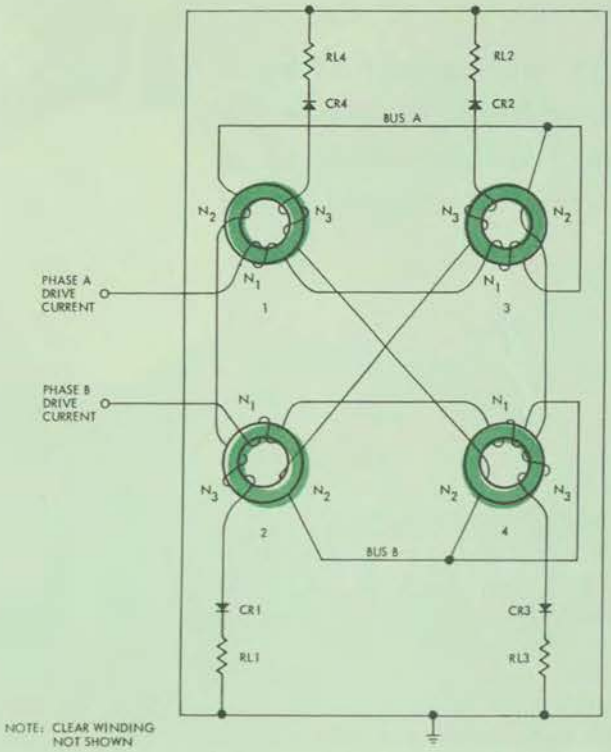
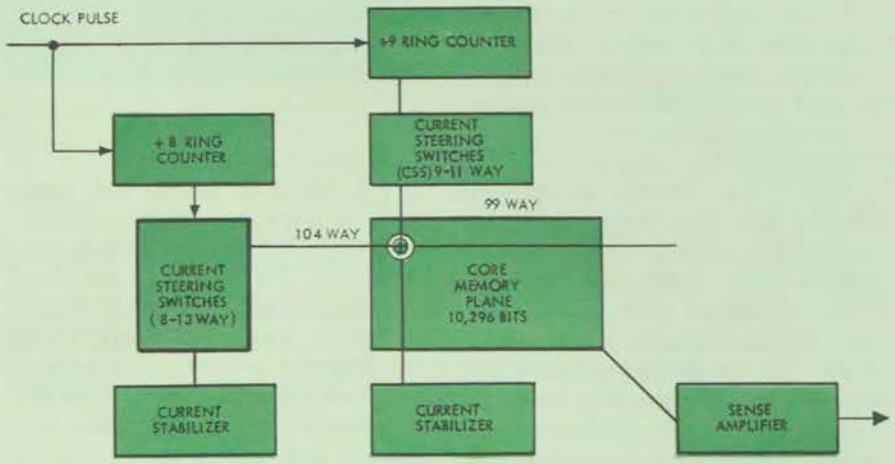


FIG. 2 *Two phase, four-position steering switch*



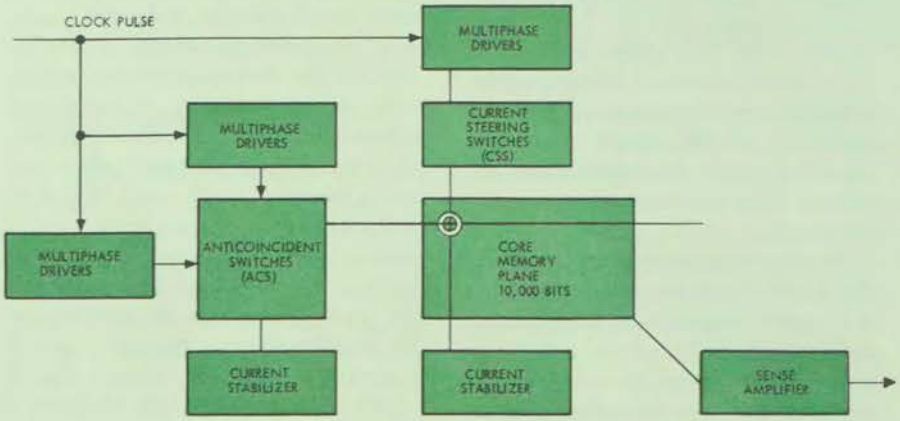


FIG. 4 *Memory unit using ACS and CSS*

cuit. It provides sequential pulse power to loads RL_1, RL_2, RL_3, and RL_4 in that order. This pulse power is conductively steered to these loads from a single current source. At time t_0, core 1 is in a state that current flowing from driver A will cause a flux change to take place; core 3 is in the oppositely saturated state which does not permit any flux change. A current pulse flowing from driver phase A will flow through winding N_1 on both cores 1 and 3 in series, and around to bus A. A voltage then appears across winding N_2 of core 1 in a direction which back biases diode CR3 associated with core 4, resulting in current being steered through winding N_2 on core 1 and then through the winding N_3 on core 2. Current flowing through this winding is in a direction to cause core 2 to experience a flux change, therefore setting this core in an opposite flux state so as to be the next selected core during the successive pulse period associated with driver phase B. The current is steered to load RL_1 (one line of the storage matrix).

During the next driver pulse a current is obtained from driver phase B which is steered through winding N_2 associated with core 2 and then through winding N_3 associated with core 3, and so on. This circuit is a passive register as well as as a current steering circuit. The gating voltage derived from the N_2 winding is a low impedance source. Therefore, if some of the diodes have a degraded back resistance, several milliamperes may be drained off without a failure in the switch operation. The normal current flow is several hundred milliamperes.

The current steering switch may be fabricated as several identical subassemblies, each containing a set of cores and diodes to provide the required Y selection lines to the storage core arrays. These submodules can be assembled and individually electrically-tested prior to assembly in the memory. The modules require approximately 12 cubic inches including diodes and related wiring terminals.

Although this technique requires one diode per coordinate, the requirements on this diode are so minimal that its actual failure rate is approximately one order magnitude lower than values normally considered. The reliability of diodes in this

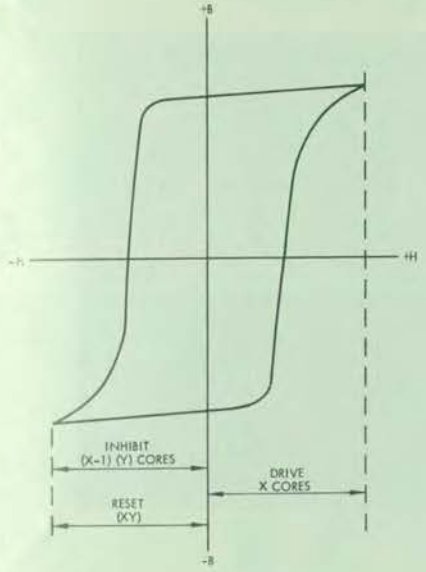


FIG. 5 *Relative magneto-motive forces applied to anti-coincident switch*

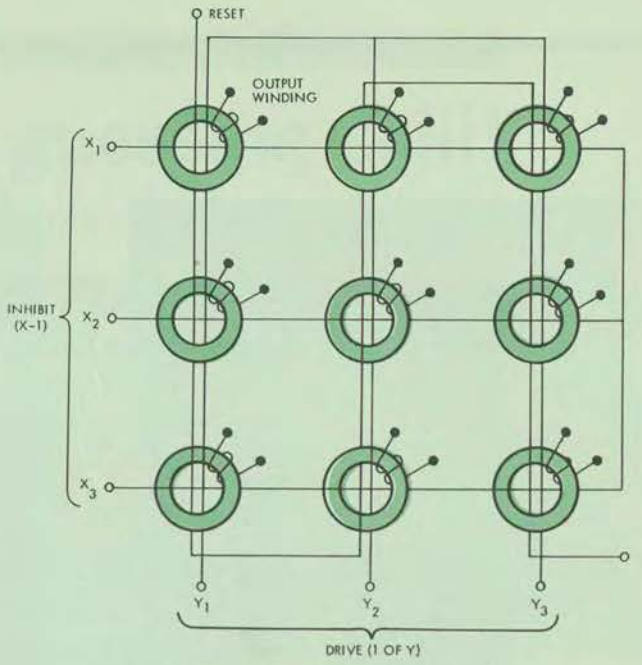


FIG. 6 *Anti-coincident current switch*

application is also unusually high because of the low duty cycle imposed on the diode and the low back voltage presented to the diode. Reliable operation with diode back resistance degradation to as low as 1000 ohms is possible.

Fig 3 illustrates the use of magnetic stepping switches for the nominal 10,000 bit memory. As shown, the two mutually prime numbers are 99 by 104, which result in completely scanning out 10,296 bits. In the example shown in Fig 4 two drive phases were used. To achieve reasonable length of the current steering register, an 8-phase ring counter is used to establish eight phases (for the Y coordinate system) and a 9-phase ring counter for the X coordinate system. Rather than use eight current stabilizers for the current steering register it is more efficient to use an 8-way commutator (ring counter) and one stabilizer. This over-all approach provides that normally cut-off blocking oscillators are used in the ring counters. This scheme provides no standby power.

As a result of this approach the drive and selection system is comprised of one regulated current source per coordinate, multiphase X and Y driver circuits, and current steering switches. A volume of several cubic inches accommodates approximately nominal selection magnetic circuits.

It is feasible to use a type of selection, in one of the coordinates, based on the principle of current transformation. This scheme minimizes the number of diodes. The practicality of its application is based on the condition that both select currents need not approach the ideal current source. The above device is known as the anti-coincident switch (ACS); its use in a memory system is shown in Fig 4. The Y drive is provided by a multiphase driver linked through current steering switch cores. Separate steered current outputs are required for read and write operations. The X drive is provided by an anti-coincident switch, which in turn is driven by a multi-phase inhibit drive circuit and a multi-phase drive circuit.

A read operation is performed by the coincidence of a half select current pulse from the current steering switch and a half select current pulse from the anti-coincident switch. A write (or restore) "1" operation is performed by a half select current from the current steering switch, in opposite direction from the read current, in time coincidence with a half select current in the same direction from the anti-coincident switch. To write an "0," these two current pulses are not time coincident. Therefore, digit driver windings, conventionally used in core matrices, are not required.

The drive current in the X direction is delivered to the array through magnetic anti-coincident switches. Fig 5 shows the relative magnetomotive forces applied by the inhibit, drive, and reset windings of the switch.

Fig 6 illustrates the ACS operation of a nine-way anti-coincident switch. Inhibit currents are set up in all but the selected inhibit line applying magnetomotive force to all switch cores, except those on the selected line, driving the unselected cores far into remnant saturation.

As soon as inhibit current is established in the ACS, one of the multiphase drivers is activated. This current causes the selected core in the ACS to traverse a flux excursion. The output winding of the selected switch core links the storage array to provide the X half select read current.

The write cycle is accomplished by applying mmf to all (ACS) switch cores in the opposite polarity to the mmf applied for the read operation. This resets the one selected switch

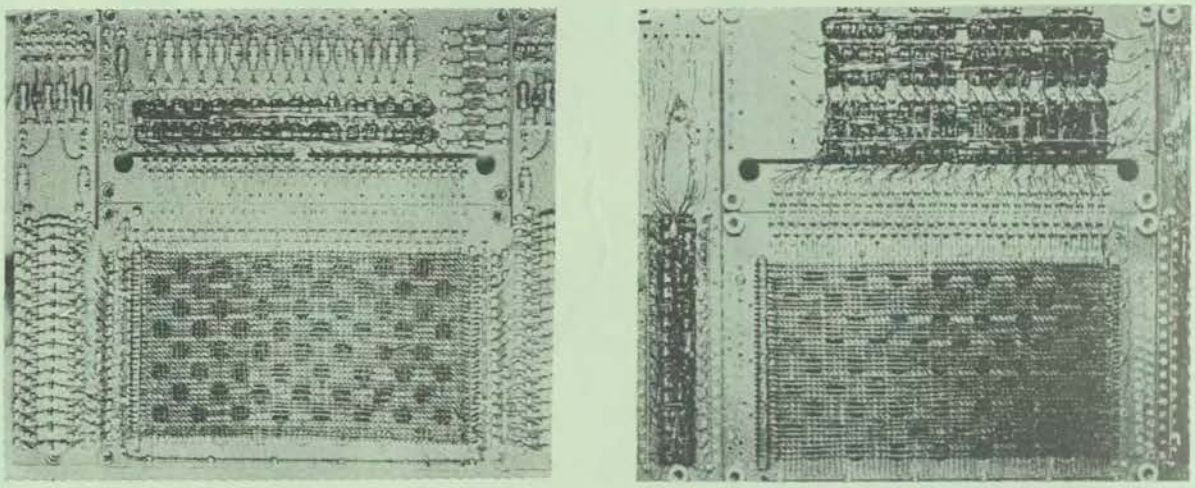


FIG. 7 *4000-bit memory unit (top and bottom view)*

core to the negative remnant condition providing an output half select write current to the storage array. If this write pulse occurs in time coincidence with the Y drive pulse from the current steering switch, a "1" will be written or restored in the array. If not coincident a "0" will be written or restored.

The scanning sequence of cores in the anti-coincident switch (for simplest access circuitry) is in a diagonal fashion, which is obtained by utilizing ring driver circuits in both the inhibit and drive directions. Since the number of lines driving this anti-coincident switch is not composed of mutually prime numbers, an additional pulse is applied in the inhibit direction (to cause an additional step of that driver circuit) each time the last line of the drive circuit to the switch has completed its operation. In this way, a diagonal scan of all cores in the anti-coincident switch is obtained.

In Fig 7, photographs of a 4000 bit memory plane with the current steering switches and anti-coincident switches are shown. A 10,000 bit memory has been selected for discussion, however, the system can be expanded in capacity without linearly increasing the weight and size. For example, increasing the memory capacity from 10,000 to 100,000 bits would result in an increase in weight and transistor count by only approximately the square root of the increase in memory capacity. Moreover, above 100,000 bits the transistor count does not necessarily increase as fast as the square root function. The drive circuitry for this type of sequential magnetic core storage system required a space only slightly larger than that of the storage core arrays themselves. While the present design utilizes a space of under 100 cubic inches, further reduction could be obtained by reducing the core size. END

REFERENCES

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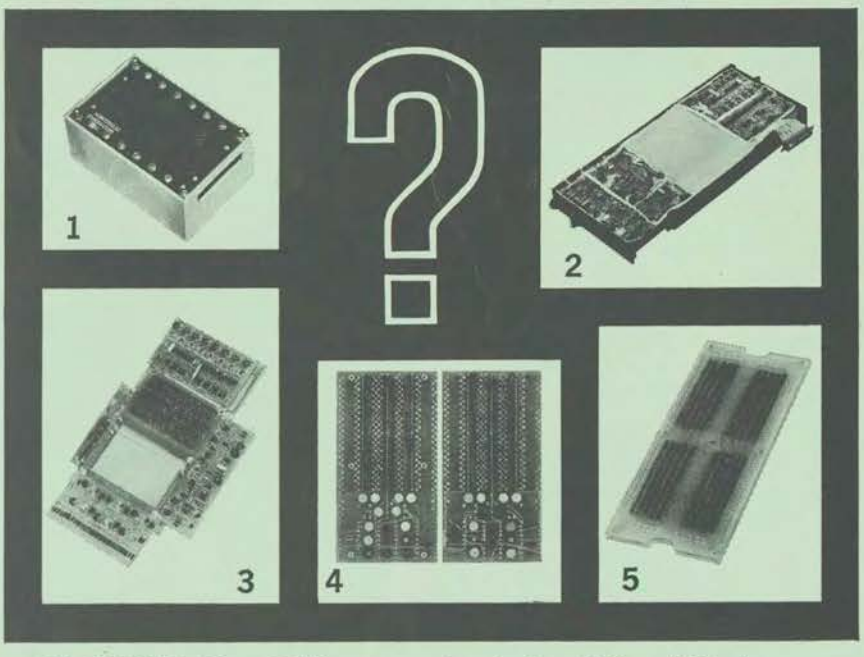
2. WEISZ, *"Ferrites With Temperature Independence and Improved Disturb Ratio,"* Journal of Applied Physics; June 1961

3. KARNAUGH, *"Pulse-Switching Circuits Using Magnetic Core,"* Proceedings of the IRE; May 1955

Dr. R. S. Weisz is Director of Research and Milton Rosenberg is Vice President of Engineering at Electronic Memories, Inc.

test your guessing skill!

(space vehicle core memory)



1 Model RE128Z34 – 128 word, 34-bit memory
Power Requirement: 300 mw at 1Kc
Temperature Range: –20°C to +80°C

2 Model RSM70 – Relay Status Monitor dynamically checks 80 relays at 10Kc
Power Requirement: 1 W at 10Kc, less than 2 mw standby.
Temperature Range: –20°C to +80°C

3 Model SE30KZ1 – 30,000 serial bits (with confidence level of .8 for 1 yr.) Wt. 3.6 lbs.
Power Requirement: 200 mw at 256 cycles
Temperature Range: –20°C to +65°C

4 Model SE1440Z1 – 1440 serial bit Isodrive® memory tolerates 3000 Gs shock
Power Requirement: 300 mw at 1Kc
Temperature Range: –30°C to +90°C

5 All Welded Memory Stack (unpotted) – 6,000 bit Isodrive® core memory stack, uses all welded construction – takes 54Gs vibration

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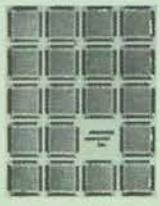

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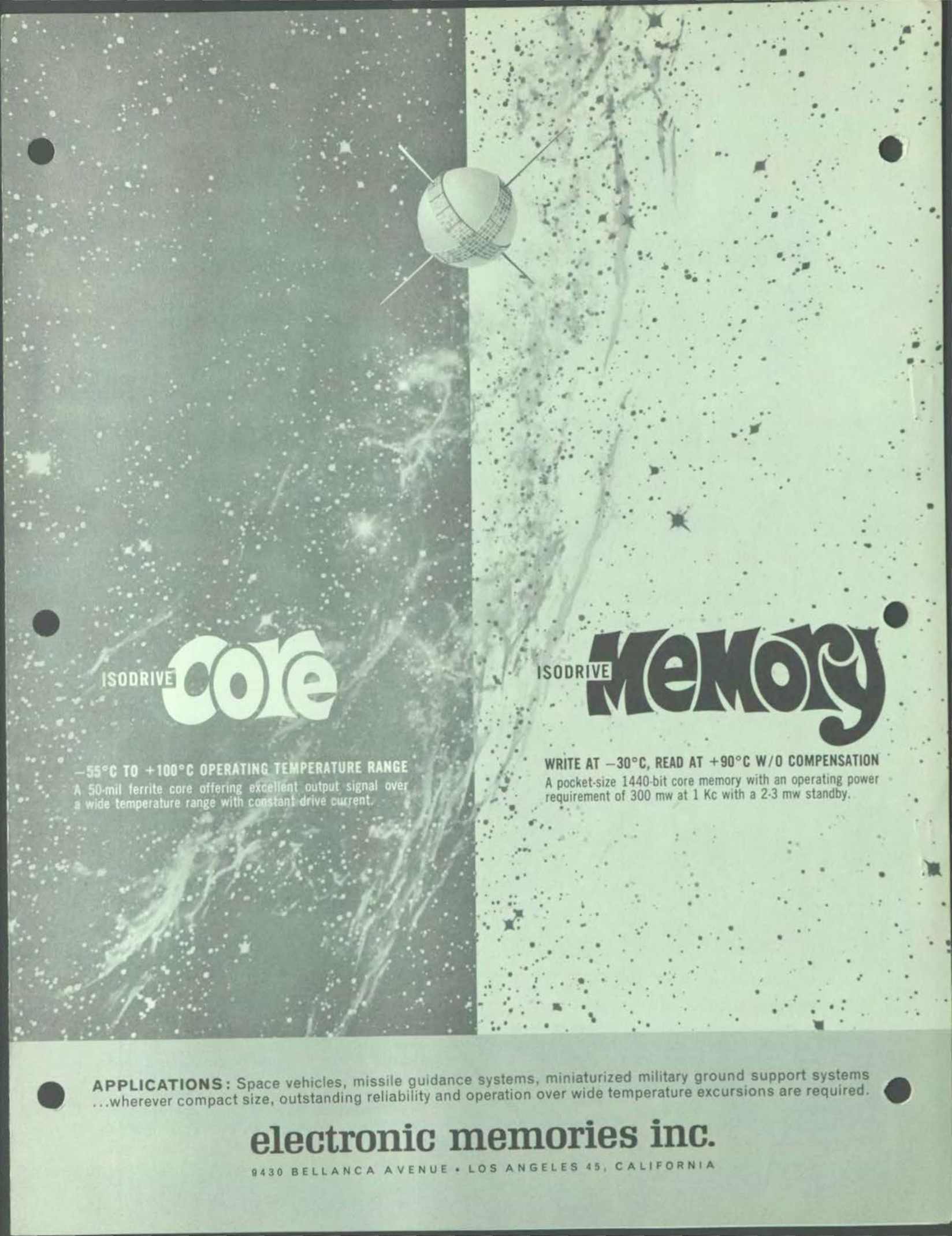

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−55°C TO +100°C OPERATING TEMPERATURE RANGE

A 50-mil ferrite core offering excellent output signal over a wide temperature range with constant drive current.

ISODRIVE MEMORY

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A pocket-size 1440-bit core memory with an operating power requirement of 300 mw at 1 Kc with a 2-3 mw standby.

APPLICATIONS: Space vehicles, missile guidance systems, miniaturized military ground support systems ...wherever compact size, outstanding reliability and operation over wide temperature excursions are required.

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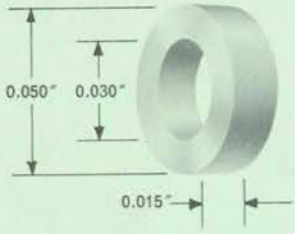
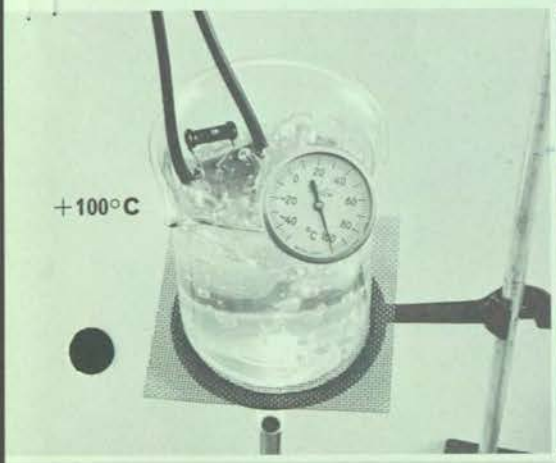
ISODRIVE core

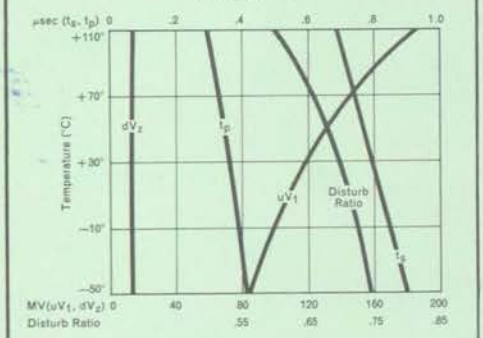


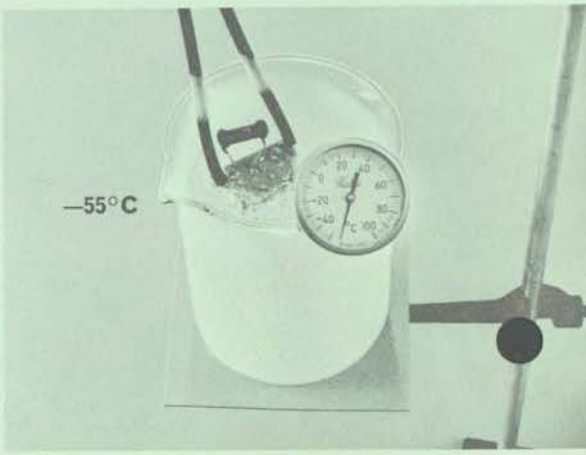
All dimensions are ± 0.002"

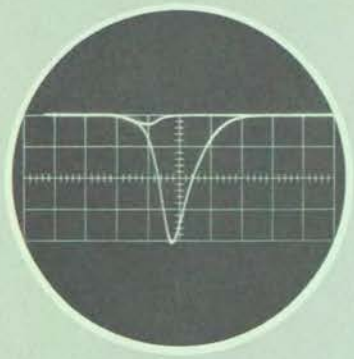
A 50-mil ferrite core offering excellent output signal over a wide temperature range with constant drive current.



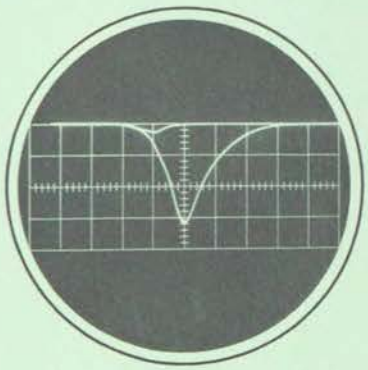
CORE PERAMETERS VS. TEMPERATURE
(Constant Drive)



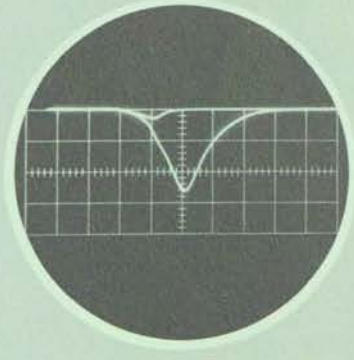




+100°C
Actual test oscillogram with core immersed in boiling water



+25°C ROOM TEMP.
Scale for oscillograms 50mv/cm, .25 μsec/cm, rise time: .2 μsec



–55°C
Actual test oscillogram, core in dry ice and alcohol.

FEATURES

Fast switching, high drive, high output. Improved disturb ratio allowing increased tolerance to drive current drift. Increased signal-to-noise ratio at sampling time. Excellent characteristics over –55°C to +100°C operating range without current compensating circuits.

RECOMMENDED OPERATING CONDITIONS

Temperature	–55°C to +100°C
Drive Pulse (I_r=I_w)	1000/500 ma turns
Pulse Width (t_w)	2μs
Pulse Rise Time (t_r)	.2μs ± .02μs linear
Pulse Fall Time (t_f)	.3μs min.

TYPICAL OUTPUT SIGNALS

Temperature:	–50°C	+25°C	+100°C
Switching time (t_s)	0.90 μs	0.80 μs	0.70
Peaking time (t_p)	0.42 μs	0.36 μs	0.30 μs
Amplitude ONE (uV_1)	85 mv	117 mv	175 mv
Amplitude ZERO (dV_z)	14 mv	14 mv	16 mv

WRITE AT −30°C, READ AT +90°C W/O COMPENSATION

ISODRIVE Memory

A pocket-size 1440-bit core memory with an operating power requirement of 300 mw at 1 Kc with a 2-3 mw standby.

SPECIFICATIONS

Model #SE1440Z1

1440 serial bits

Operating Modes:

Buffer—Memory
Shift Register or Memory Split Cycle

Speed:

Intermixed load and unload buffer operations up to 100 Kc. Complete memory cycle up to 50 Kc. Shift rate up to 50 Kc.

Input Signals:

Buffer Operation

Pulses	Levels
0 to +6V	0 to +6V
Load	Info Input
Unload	
Clear	

Memory Operation

Pulses	Levels
0 to +6V	0 to +6V
Unload	Read/Return
Clear	Clear/Write
	Info Input

Shift Register or Memory Split Cycle

Pulses	Levels
0 to +6V	0 to +6V
Unload	Read/Restore
Clear	Clear/Write
	Info Input

Output Signals:

Buffer—Memory—Shift Register or Memory Split Cycle
Pulse 0 to +6V—5 μs duration

Power Supply:

Supplied by customer, one voltage +28 volts. Stand-by requirement is 10-15 milliwatts. Operating power at 1 Kc rate is 300 milliwatts.

Dimensions:

1440 bit capacity requires 2" x 3" x 5"

Weight:

1440 bit capacity weighs 15 oz.

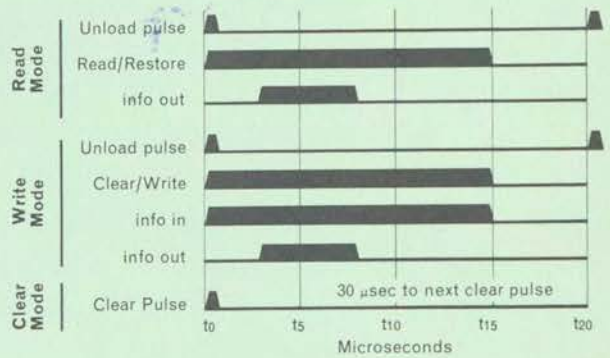
Environment:

Operates without temperature stabilization of the magnetics or current compensation of the drive currents over a range of −30°C to +90°C. Withstands normal ICBM shock and vibration.

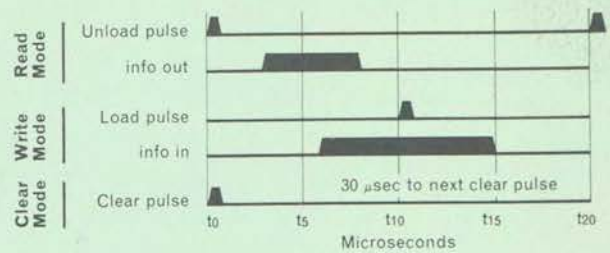
Other Memories:

Additional storage capacities and wider temperature ranges available on special order.

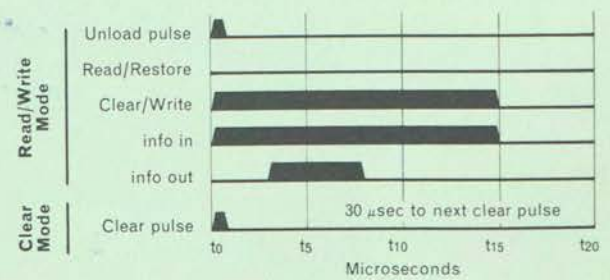
MEMORY OPERATION



BUFFER OPERATION

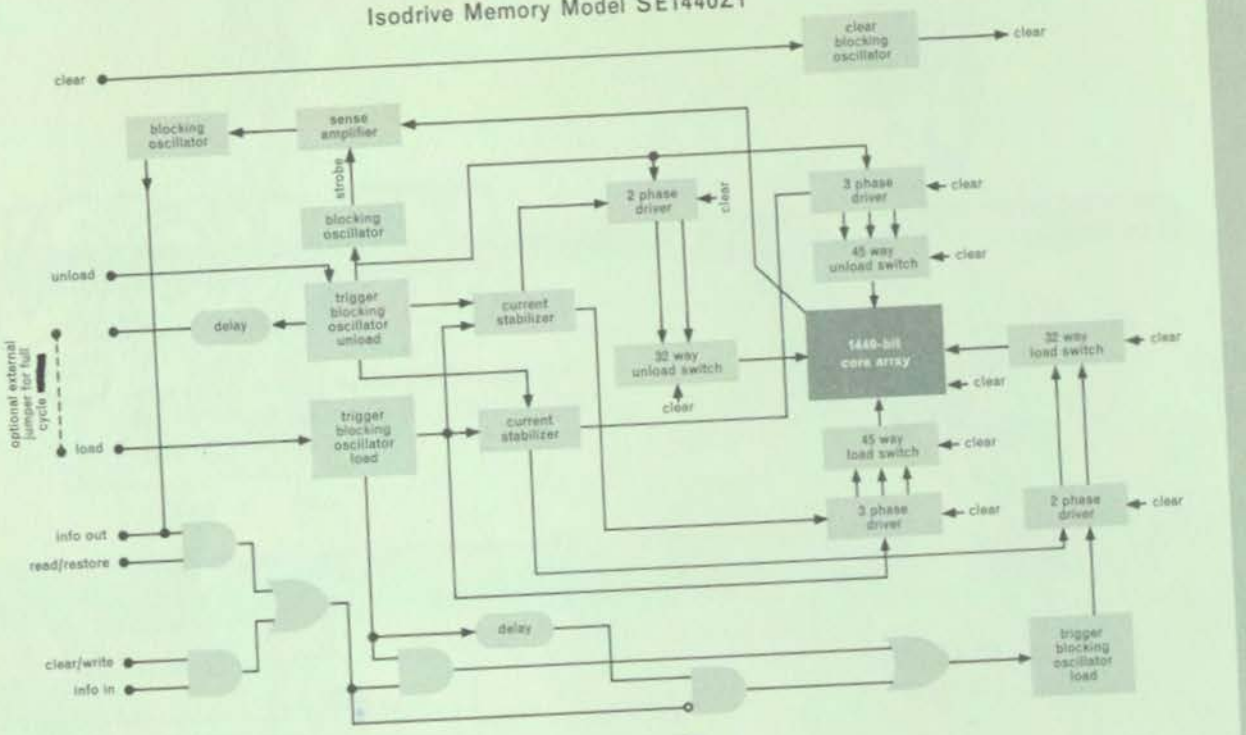


SHIFT REGISTER OR MEMORY SPLIT CYCLE



BLOCK DIAGRAM

Isodrive Memory Model SE1440Z1



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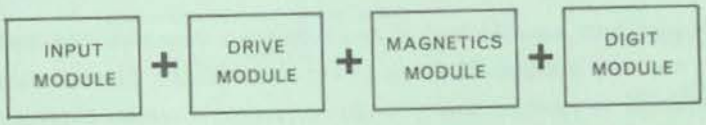

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MIMS Modular Core Memories utilize the latest in silicon semiconductor technology, Electronic Memories' ISODRIVE® Core, and advanced packaging techniques, to deliver unusually reliable coincident current memories of varying sizes, operable over a temperature range of —30°C to +80°C.

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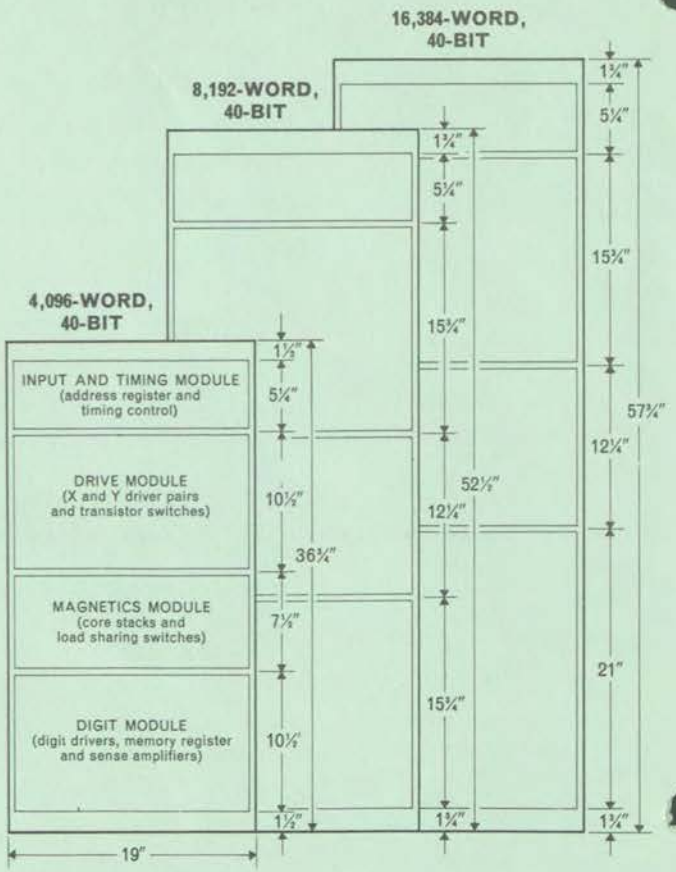
"MIMS" is the convenient way to designate Electronic Memories' Modular ISODRIVE® Memory Series. MIMS memories are notable for their wide operating temperature range, high reliability, and adaptability to a broad range of applications. Standard MIMS memories are available in compact, relay rack configurations, and will withstand normal shock and vibration. For applications where severe "G" environments will be encountered, custom MIMS are available in special 3-dimensional packages to meet customer-supplied size, configuration and environmental requirements.

MIMS RELIABILITY

Throughout the MIMS design and manufacturing cycle, careful attention has been given to the operational reliability of the complete memory system. The use of the ISODRIVE® Core ensures operation of the memory over a wide temperature range or permits use of wider circuit tolerances over narrower temperature ranges. Load sharing switches are used to drive the MIMS core stack. These switches, driven by transistors operated far below rated capacities, provide high current pulses with fast rise times. The use of silicon semiconductors, taper pin connectors, and advanced design concepts developed by Electronic Memories, ensures the operating reliability of each MIMS.

STANDARD PACKAGING

MIMS memories are normally supplied in standard card cages mounted in relay rack cabinets. A standard MIMS, including power supply, consists of four basic modules, with the height of the modules and the memory configuration dependent on the capacity requirement.



TYPICAL COMPONENT COMPLEMENTS W/O POWER SUPPLY

MEMORY COMPONENTS	4096-word 40-bit MIMS	8192-word 40-bit MIMS	16,384-word 40-bit MIMS
Total diodes and transistors	3510	4099	4,864
Total resistors, capacitors, etc.	4684	5431	6,906
Total Components	8194	9530	11,770

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SPECIFICATIONS:

Operating Mode: Coincident Current

Speed: Cycle Time—2.5 μs Access Time—1.0 μs

Capacities: 4,096, 8,192, or 16,384 words—8 to 80 bits

Temperature Range: −30°C to +80°C without current compensation or temperature stabilization.

Power Requirements: 4,096-word, 40-bit memory: 750 watts D.C.
16,384-word, 40-bit memory: 1500 watts D.C.

Input Signals: (0 to +3 volts minimum to 0 to +10 volts maximum with typical voltage of 0 to +5 volts)

SIGNAL REQUIRED	SIGNAL TYPE	SIGNAL CHARACTERISTICS
Start Cycle	Pulse	10 mils of current, pulse rise time of 0.1 μs into a pulse transformer. Pulse width at 90% point is 0.1 μs min., 0.5 μs max.
Read/Write Signal	Single-ended level	3 mils of current settled at start cycle.
Address	Single-ended level	3 mils of current settled at start cycle.
Information Input	Single-ended level	3 mils of current settled at .8 μs from start cycle.

Output Signals:

SIGNAL REQUIRED	SIGNAL TYPE	SIGNAL CHARACTERISTICS
Information Out	Double-ended level	10 mils of current, available 1 μs after start cycle.

MIL-SPECS: Designed to meet MIL-E-16400D, MIL-E-4158B, MIL-E-5400E specifications.

Special Features:

ISODRIVE® Core allows memory operation over a wide temperature range or allows use of wide circuit tolerances within narrower temperature ranges.

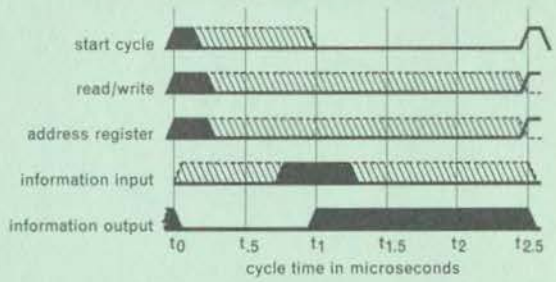
Silicon Semiconductors are used throughout to ensure high reliability over a wide temperature range.

Load Sharing Switches which drive the core stack, provide high current pulses with fast rise times, yet do not require large currents from the transistor drivers.

Optional Features:

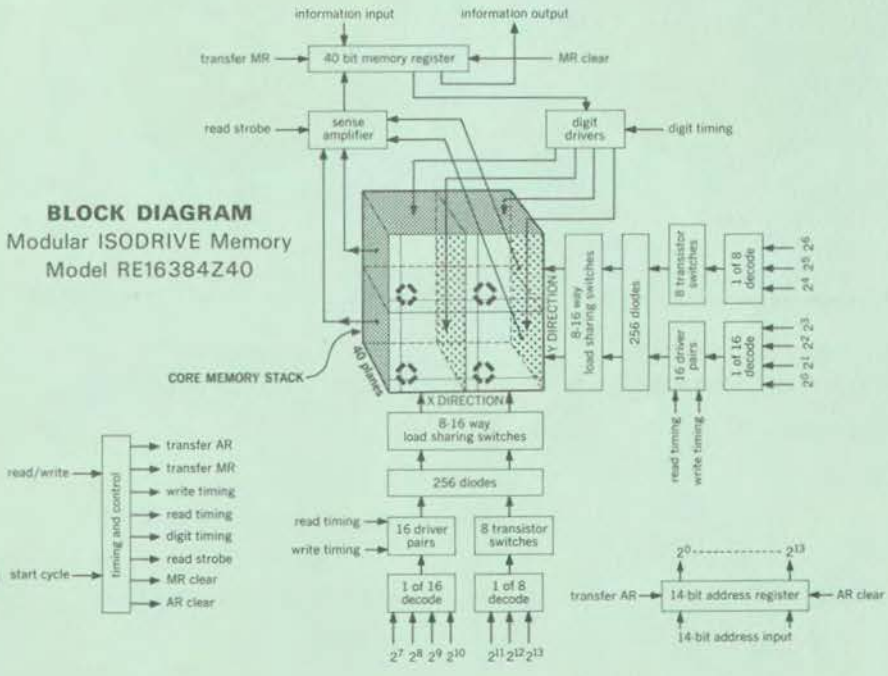
Complete MIL-Spec documentation...special packaging configurations...packaging for shock and vibration... register indicators...split cycle...partial substitution... information available signal...end-of-cycle signal.

TIMING DIAGRAM



Top of pulse indicates when information must be settled in register.
Solid lines indicate minimum times pulse or level can exist.
Dotted lines indicate maximum times pulse or level can exist.

BLOCK DIAGRAM
Modular ISODRIVE Memory
Model RE16384Z40



SPECIAL PACKAGING FOR SEVERE ENVIRONMENTS AND UNIQUE CONFIGURATIONS

Through the use of three-dimensional packaging techniques, the MIMS design is adaptable to a broad range of difficult applications where shock, vibration, restricted size, and unique configurations are encountered. For a custom designed MIMS, the physical size and configuration of the package is dictated by customer-supplied requirements for word capacity, bit length, shock and vibration, and the size and volume of the space available for the memory package. Typical three-dimensional packaging would allow a minimum of 0.5 cubic feet (4,096-word, 40-bit memory) and 2.0 cubic feet (16,384-word, 80-bit memory), exclusive of power supply. The physical volume requirements for a typical three-dimensional power supply are approximately 1.0 cubic feet (4,096-word, 40-bit memory) and approximately 2.5 cubic feet (16,384-word, 40-bit memory).

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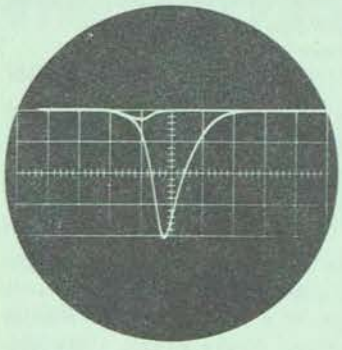
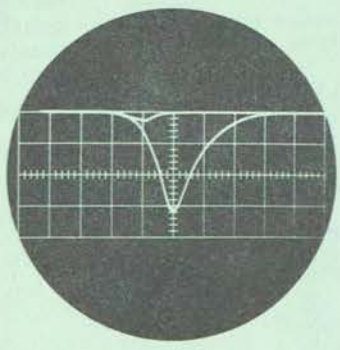
–55°C TO +100°C OPERATING TEMPERATURE RANGE

ISODRIVE core

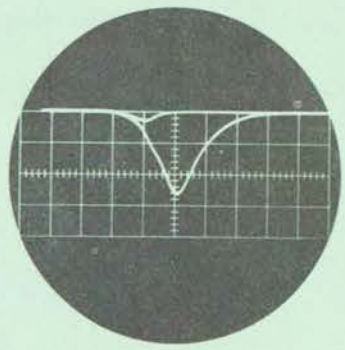
The heart of the MIMS Series is Electronic Memories' ISODRIVE® core—Type 46-100—a 40-mil ferrite core offering an excellent output signal over an operating temperature range of –55°C to +100°C without temperature stabilization or current compensation. The ISODRIVE® core features fast switching, high output, improved disturb ratio, increased tolerance to drive current drift, and increased signal-to-noise ratio at sampling time. This core, combined with the latest advances in silicon semiconductor technology, and utilized by a tightly-knit group of highly experienced core memory specialists, has resulted in the MIMS core memory series.



+100°C
Actual test oscillogram with core immersed in boiling water



+25°C
Actual test oscillogram with core at room temperature



–55°C
Actual test oscillogram, with core in dry ice and alcohol

FEATURES

Fast switching, high output. Improved disturb ratio allowing increased tolerance to drive current drift. Increased signal-to-noise ratio at sampling time. Excellent characteristics over –55°C to +100°C operating range without current compensating circuits.

RECOMMENDED OPERATING CONDITIONS

Temperature Range	–55°C to +100°C
Drive Pulse	900/450 ma turns
Pulse width (t_W)	2 μs
Pulse rise time (t_r)	0.1 $\pm$ 0.01 μs linear
Pulse fall time (t_f)	0.2 μs min.

TYPICAL OUTPUT SIGNALS

Temperature:	–55°C	+25°C	+100°C
Amplitude ONE (uV_1)	43 mv	59 mv	74 mv
Amplitude ZERO (dV_Z)	9 mv	10 mv	11 mv
Peaking Time (t_p)	0.27 μs	0.22 μs	0.18 μs
Switching Time (t_S)	0.54 μs	0.47 μs	0.41 μs

how to be sure you choose the proper MIMS

MIMS is the convenient way to designate the Modular ISODRIVE® Memory Series. MIMS core memories all operate from −30° to +80°C without driver compensation or stack heating. They are coincident current, with 2.5 μsec cycle times and 1 μsec access. This dramatic performance is accompanied by a reliability breakthrough—the heart of MIMS is Electronic Memories' ISODRIVE ferrite core—and silicon components have been used exclusively.

We can't picture a MIMS unit—each one is custom built and packaged. But, we can discuss in detail *the* MIMS designed to meet your requirements. That's why the MIMS Choosers Checklist. Just check your requirements below and send them along to us. We'll be in touch by return mail.

The **MIMS** Choosers Checklist:

MIMS core memories are available in any combination of the following characteristics:

MIL-SPEC
- ☐ MIL-E-16400D
- ☐ MIL-E-4158B
- ☐ MIL-E-5400E
- ☐ Non Mil-Spec

CAPACITY
- ☐ 1024 words
- ☐ 2048 words
- ☐ 4096 words
- ☐ 8192 words
- ☐ 16,384 words

WORD LENGTH
- ☐ 8-bits
- ☐ 20-bits
- ☐ 40-bits
- ☐ 60-bits
- ☐ 80-bits

PACKAGE
- ☐ Relay rack card cage
- ☐ High density package
- ☐ Custom configuration

ENVIRONMENT
- ☐ Temperature +___°C to −___°C
- ☐ Vibration ___cps ___g's
- ☐ Shock ___g's

APPLICATIONS
- ☐ Ground-mobile
- ☐ Ground—exposed
- ☐ Airborne
- ☐ Laboratory
- ☐ Shipboard
- ☐ Satellite
- ☐ Other_____

PACKAGE VOLUME
- ☐ .5 cu. ft.
- ☐ 1.5 cu. ft.
- ☐ 2 cu. ft.
- ☐ 5.5 cu. ft.
- ☐ ___cu. ft.

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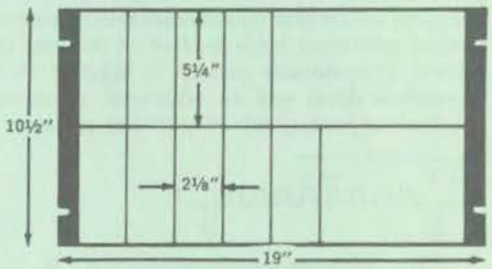
PROGRAMMED MAGNETICS TESTER

This series of precise test instruments has been specifically designed for the testing and evaluation of magnetic cores and circuits. They have been designed by an engineering group thoroughly familiar with both magnetic core technology and the latest advances in silicon transistor circuitry. When used by a knowledgeable magnetics specialist, Electronic Memories' Programmed Magnetics Testers are unusually valuable pieces of test instrumentation.

MODEL 100-SERIES TESTERS ARE COMPLETELY MODULAR, ALLOWING COST AND TEST PROGRAM FLEXIBILITY

Each Programmed Magnetics Tester consists of a series of economical, compact, high performance current pulse generators together with a current calibrator module, a power supply package, and an optional program generator package. The complete system is housed in a compact cabinet which may be rack-mounted or placed on a bench. The unit weighs approximately 35 pounds for easy portability. The system is unusually stable, with a high output impedance of the constant current drivers.



FIVE BASIC INTERCHANGEABLE MODULES PLUS A FIXED POWER SUPPLY MODULE

Four plug-in packages—negative driver, positive driver, univibrator and current calibrator — each occupy a 2⅛" by 5¼" modular unit. An optional plug-in program generator package is three units wide. The power supply package is four units wide and is a bolted-in unit. All power connections are made as the various packages are plugged in. The packages are rigidly retained by means of screws to the surface of the main housing. Signal interconnections between packages are made by miniature banana patchcords at the back of the unit and may be easily changed to achieve various functional configurations of the Magnetics Tester.

NEGATIVE DRIVER AND POSITIVE DRIVER have high output impedance for generating current pulses whose amplitude is continuously variable from 60 ma to 1200 ma. Rise and fall time, linear 10% to 90% is continuously variable from .050 μsec. to 2 μsec. Drivers may be operated from two separate signals and may be bussed together to feed a common load.

CURRENT CALIBRATOR for precise measurements of driver amplitude also sets accurate driver output to a prescribed value. A linear potentiometer allows direct dial readings in ma and mv. Visual comparison of monitored waveform to calibrated amplitude can be made on an oscilloscope. Currents up to 2.0 amperes can be measured.

UNIVIBRATOR package contains two univibrator circuits. Each circuit is variable over one or more decades. Other models with timing variations up to four decades (0.1 to 1000 μsec.) are available. An oscilloscope can be synchronized to the end of each delay period (beginning of each drive pulse).

PROGRAM GENERATOR has an oscillator with continuously variable frequencies from 1 kc/sec to 1 mc/sec. 8-phased signals trigger univibrators to operate drivers. Four driver channels may be switched in the eight time slots. Toggle switches place each driver in any, all, or none of the time slots.

POWER SUPPLY, a bolted in unit, will operate two negative and two positive drivers, four univibrators, a current calibrator and a program generator. The ac line voltage requirements are 115 v ±10%, 48 to 63 cps, single phase. Stop and start switches are used in self-programming mode.

TWO BASIC TESTER TYPES — SELF-PROGRAMMING AND PROGRAM-GENERATED — ARE DESCRIBED ON THE REVERSE OF THIS PAGE

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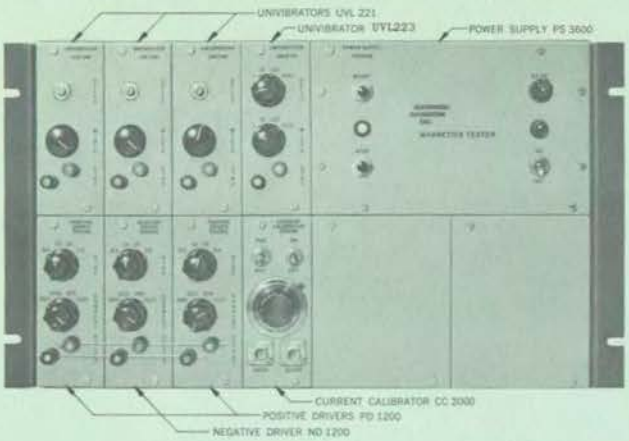
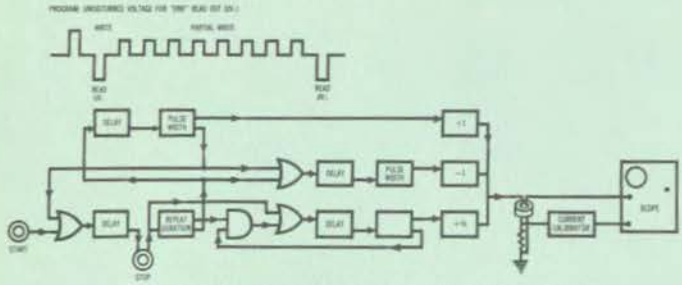


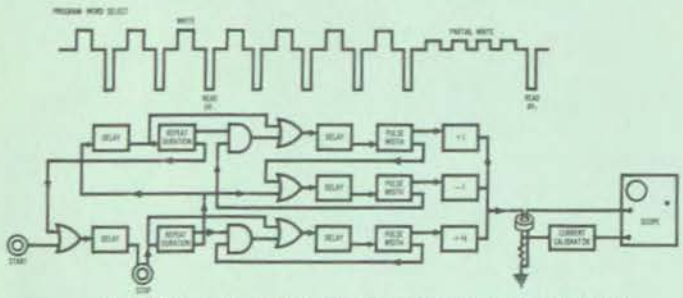
MODEL 102 SEMI-VARIABLE PROGRAM MAGNETICS TESTER

SELF-PROGRAMMING TESTER–MODEL 102

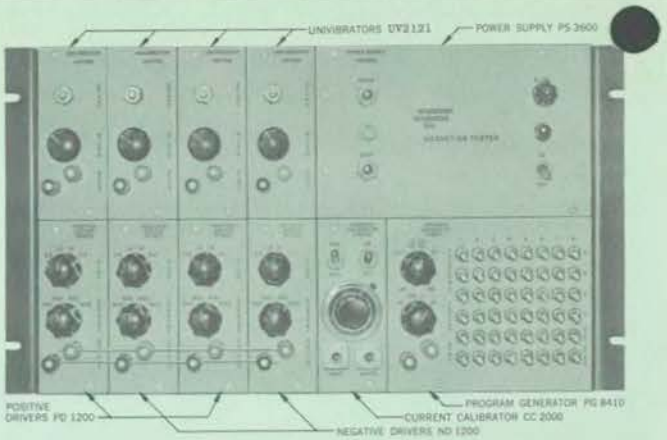
The least expensive and simplest model Magnetics Tester does not include the program generator module. However, interconnections can be made to allow self-generation of a pulse program. Program changes are accomplished by changing univibrator interconnections by means of miniature banana patchcord leads located at the rear of the unit. In general, a univibrator package is required for each negative or positive driver and an additional univibrator package is required for each group of repetitive pulses.



BLOCK DIAGRAM MODEL 102 MAGNETICS TESTER



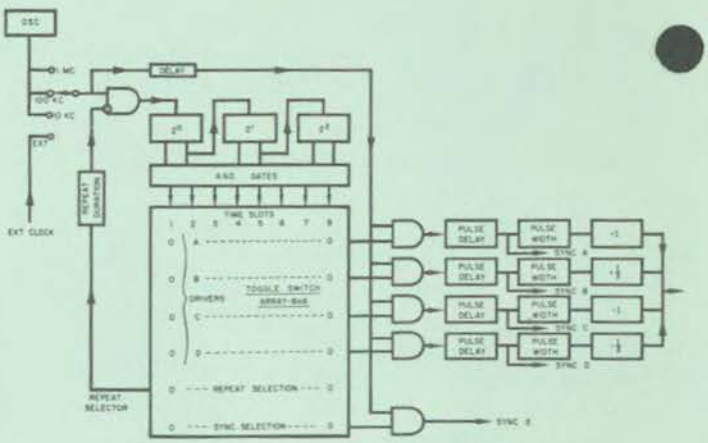
ADAPTATION OF MODEL 102 FOR WORD SELECT PROGRAM.



MODEL 150 VARIABLE PROGRAM MAGNETICS TESTER

PROGRAM-GENERATED TESTER–MODEL 150

This is the most flexible form of Magnetics Tester, in that it allows a virtually infinite variety of pulse programs to be initiated from switches on the front panel of the unit. A program generator package is used to control selection of programs. Where maximum efficiency is desired and/or a variety of tests and evaluations are to be performed, the Model 150 is particularly useful.



BLOCK DIAGRAM MODEL 150 MAGNETICS TESTER

PHYSICAL CHARACTERISTICS

Relay Rack Mounting or Bench Use

Height:	10½"	Depth:	10"
Width:	19"	Weight:	35 lbs.

Housing contains space for 16 modular units.

Modular unit width:	2⅛"
Modular unit height:	5¼"

Modular Plug-in Units:

Negative Driver	1 unit wide
Positive Driver	1 unit wide
Univibrator	1 unit wide
Current Calibrator/Chopper	1 unit wide
Program Generator (used only in Variable Program model)	3 units wide
Power Supply (bolted in)	4 units wide

ELECTRICAL CHARACTERISTICS FOR ALL DRIVERS

Current Amplitudes: Continuously variable from 60 ma to 1200 ma.

Current Rise Time: .050 μs to 2 μs continuously variable. —linear 10% to 90%.

Current Fall Time: Same as rise time.

Pulse Width: Continuously variable 0.1 μs to 10 μs.

Maximum Average Current per driver: 250 ma.

Output impedance is no less than 1000 ohms.

Maximum voltage drop across the load, 20 volts in either direction before serious cavitation of wave form appears.

Droop or rise in current amplitude during pulse is not more than 1%.

Positive Driver overshoot is less than 5% and occurs only for rise times faster than 0.1 μs.

Negative Driver overshoot is less than 1% and occurs only for rise times faster than 0.1 μs.

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MAGNETICS TESTER

ABBREVIATED SPECIFICATIONS

2 Models: **Model 102 Semi-Variable Program Magnetics Tester**
Model 105 Variable Program Magnetics Tester

Physical Characteristics

Relay Rack Mounting or Bench Use

Height:	10½"
Width:	19"
Depth:	10"
Weight:	30 lbs.

Housing contains space for 16 modular units.

Modular unit width:	2⅛"
Modular unit height:	5¼"

Modular Plug-In Units:

Negative driver	1 unit wide
Positive Driver	1 unit wide
Univibrator	1 unit wide
Current Calibrator/Chopper	1 unit wide
Program Generator	3 units wide (used only in Variable Program model)
Power Supply	4 units wide (bolted in)

Electrical Characteristics for all Drivers

Current Amplitudes: Continuously variable from 60 ma to 1200 ma.

Current Rise Time: .050 μs to 2 μs continuously variable.
— linear 10% to 90%.

Current Fall Time: Same as rise time.

Pulse Width: Continuously variable 0.1 μs to 10 μs.

Maximum Average Current per Driver: 250 ma.

Output impedance is no less than 1000 ohms.

Maximum voltage drop across the load, 20 volts in either direction before serious cavitation of wave form appears.

Droop or rise in current amplitude during pulse is not more than 1%.

Overshoot is less than 5% and occurs only for rise times faster than 0.1 μs.

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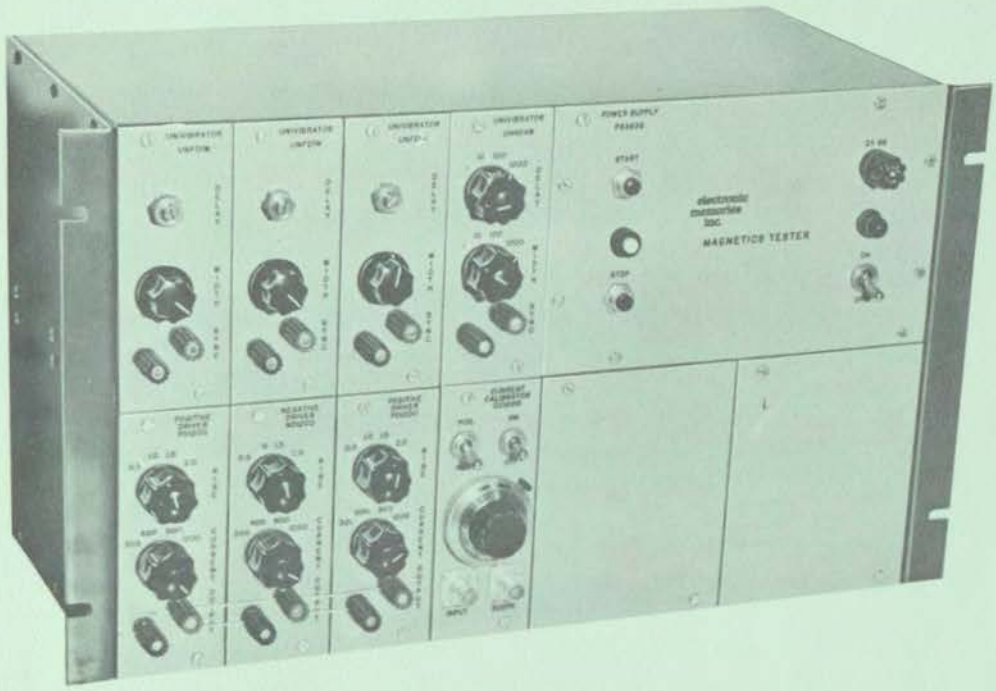
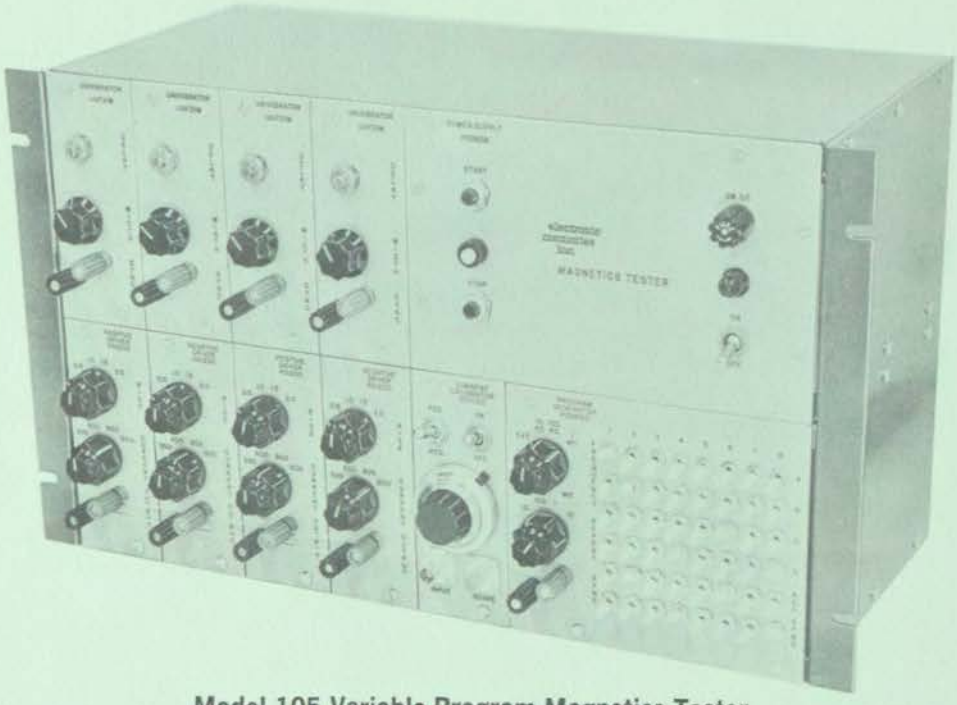


Model 102 Semi-Variable Program Magnetics Tester
(Program may be changed by reconnecting banana plugs in rear of the unit.)

Price — Approximately $4000.00



Model 105 Variable Program Magnetics Tester
(Program is controlled by switch panel on front of the unit.)

Price — Approximately $6000.00

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MAGNETICS TESTER
Model 100 Series

The 100 Series Magnetics Tester is a series of economical, compact, and high performance programmed current pulse generators specifically designed for testing and evaluation of magnetic cores and magnetic circuits. The units possess a high degree of stability with a high output impedance of the constant current drivers. It has been designed for the magnetics engineer by an engineering group thoroughly familiar with magnetic core technology and the latest advances in silicon transistor circuitry.

PHYSICAL CHARACTERISTICS

The complete Magnetics Tester system is housed in a compact cabinet which may be relay rack mounted or placed on a bench. The unit is 19" wide, 10-1/2" high, 10" deep over-all; and weighs approximately 35 pounds. The housing contains space for 16 modular units: a modular unit is 2-1/8" wide and 5-1/4" high.

The following plug-in packages each occupy a modular unit: Negative Driver, Positive Driver, Univibrator, Current Calibrator. The program generator is 3 units wide and the power supply is 4 units wide. All packages are plugged into the main housing except for the power supply, which is a bolted-in unit. The power connections are made automatically as the packages are plugged in. These packages are rigidly retained by means of screws to the front surface of the main housing. The signal interconnections between the packages are made by means of miniature banana patchcords in the back of the unit and may be easily changed to achieve various functional configurations of the Magnetics Tester.

GENERAL INFORMATION

The various tester models available are fabricated using modules which will be described in the following pages. The Magnetics Tester, Model 102, is the simplest and least expensive tester model. It consists of the housing, either rack-mounted or bench type, and the modules listed below:

1 module	(a)	Power Supply,	PS3600
1 module	(b)	Current Calibrator,	CC2000
3 modules	(c)	Univibrator,	UVL221
1 module	(d)	Univibrator,	UVL223
2 modules	(e)	Positive Driver,	PD1200
1 module	(f)	Negative Driver,	ND1200

The modules are mounted in the housing as shown by illustration Figure 1. The housing shown in Figure 1 is the housing for rack mounting. The bench type housing has hand grips on the side and rubber feet to support the unit.

The actual operation of the unit is best described by Figure 2, which shows a logic diagram of the Model 102 Magnetics Tester and a resultant pulse sequence.

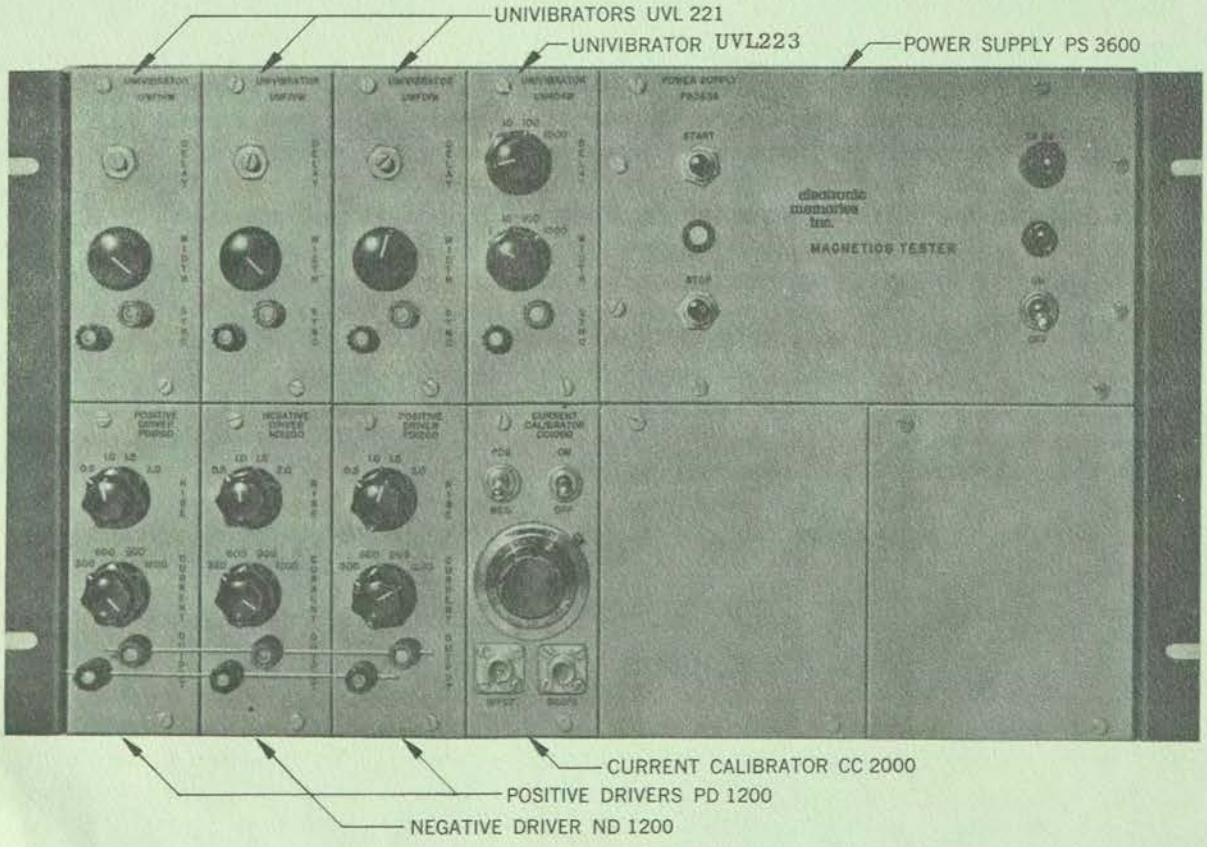

Fig. 1 Model 102 Semi-Variable Program Magnetics Tester. (Program may be changed by reconnecting banana plugs in rear of the unit.)

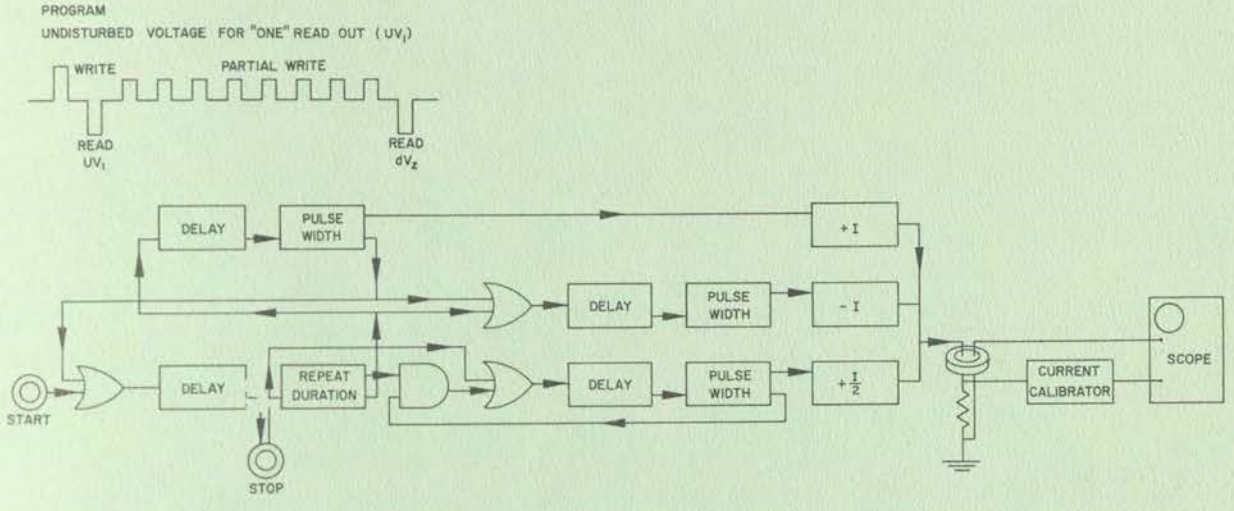

FIG 2 BLOCK DIAGRAM MODEL 102 MAGNETICS TESTER

The Model 150 Magnetics Tester is the most versatile of the available models. It consists of the housing, either rack mounted or bench type, and the modules listed below:

1 module	(a)	Power Supply,	PS3600
1 module	(b)	Current Calibrator,	CC2000
4 modules	(c)	Univibrator,	UV2121
2 modules	(d)	Positive Drivers,	PD1200
2 modules	(e)	Negative Drivers,	ND1200
1 module	(f)	Program Generator,	PG8410

The Model 150 is shown in Figure 3 and the modules are mounted in the unit as described in Figure 3.

The Model 150 logic diagram is shown in Figure 4. A pulse program is not shown for this model since a wide variety of possibilities exists.

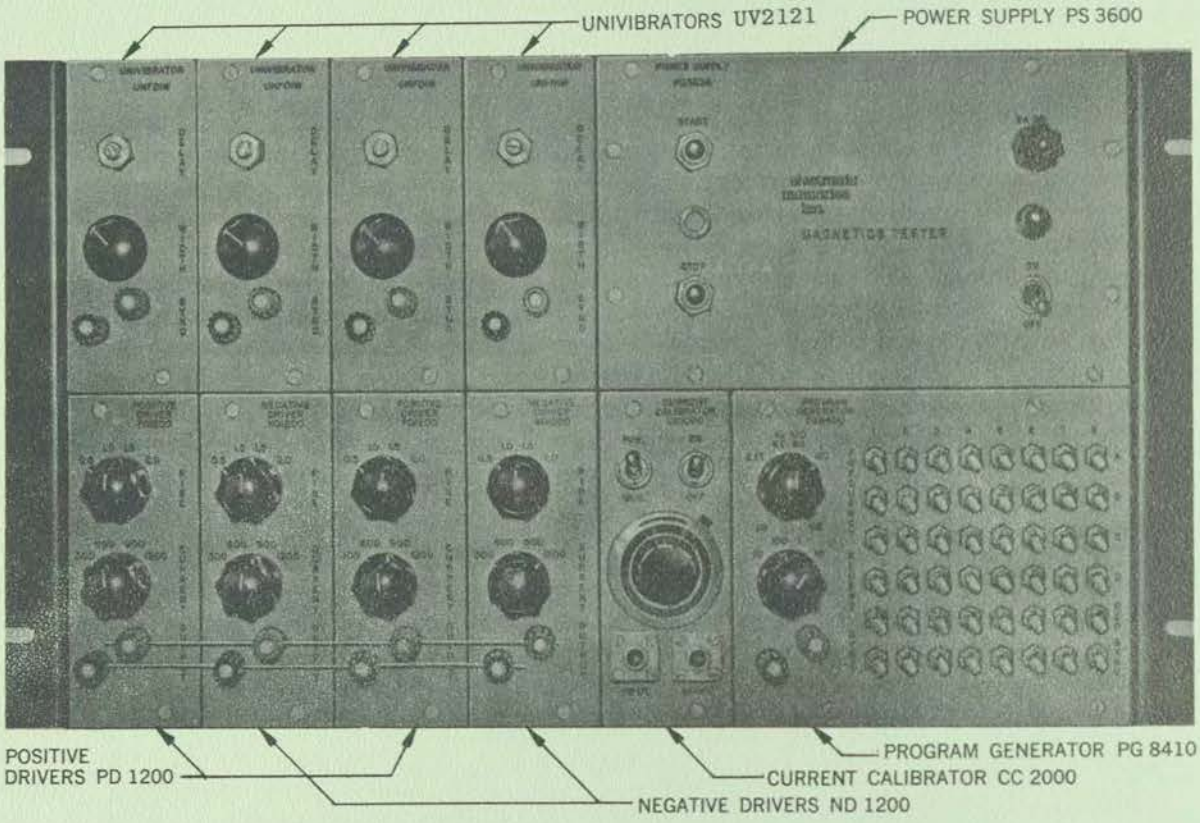

Fig. 3 Model 150 Variable Program Magnetics Tester. (Program is controlled by switch panel on front of the unit.)

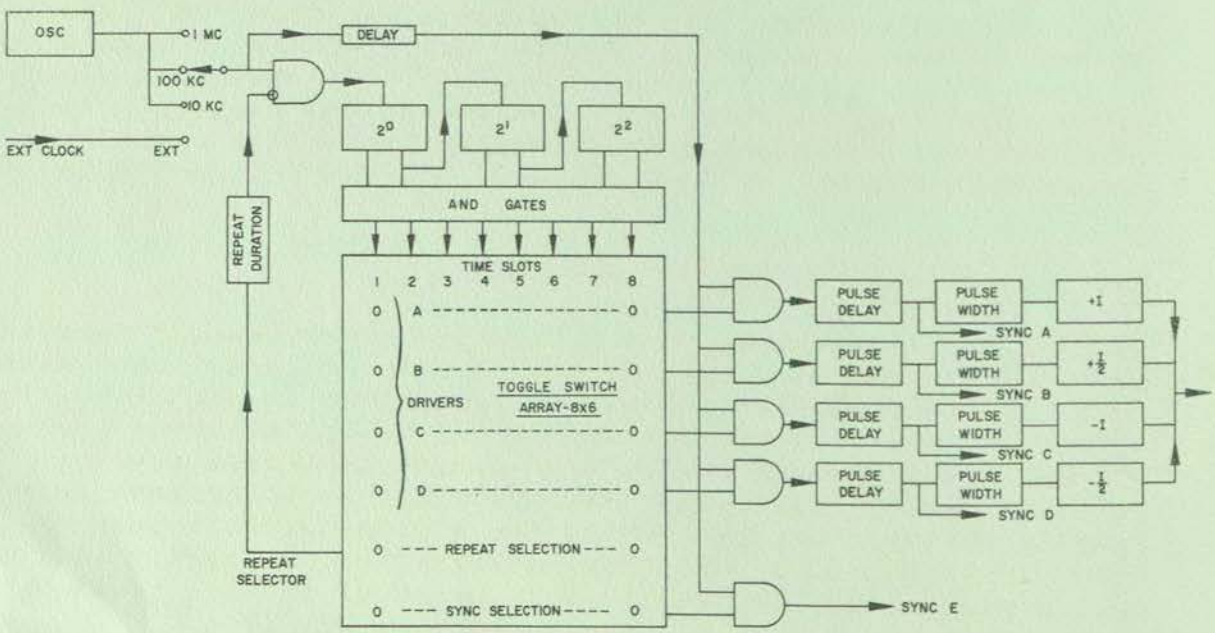

FIG 4 BLOCK DIAGRAM MODEL 150 MAGNETICS TESTER

ELECTRICAL INFORMATION

Negative Driver, ND1200

The negative driver is a stable constant-current driver with high output impedance for generating negative current pulses from 60 ma to 1200 ma. The current amplitude is continuously variable over this range. The fastest rise time obtainable is .050 micorsecond and is continuously variable up to 2 microseconds. The rise time is linear from 10% to 90% of the current pulse, and the fall time is similar to the rise time at each setting of the rise time control. The current amplitude and rise time are stable over long periods of operation and do not change due to interactions of controls if either one of the foregoing, the pulse width, or the repetition rate, is changed.

The maximum allowable average current which may be drawn from the driver is 250 ma. That is, if the amplitude control is set for 1000 ma, the maximum allowable duty cycle is 25%. The output impedance is no less than 1000 ohms. The voltage drop across the load may be as much as 20 volts before any serious cavitation of the current waveform occurs. When the driver is not operating the output terminal may be driven 20 volts in either direction. This is likely to happen when several negative and positive drivers are connected together to feed a common load. The delay times through two negative drivers are sufficiently similar so that two drivers may be operated in parallel for current pulses up to 2.4 amperes.

The droop or rise in the current waveform during the pulse is not more than 1% of the total current amplitudes. The overshoot is not more than 1% and occurs only for rise times faster than .10 microsecond. The driver has a two-term "OR" input so that it may be operated from two different input signal sources. The output from the driver is available from a pair of terminals on the front panel of the driver package. These terminals are so arranged that they may be easily bussed together when several drivers are used to feed a common load.

Positive Driver, PD1200

Similar in all respects to the negative driver except that the overshoot is not more than 5% and occurs for rise times faster than .100 microseconds. The positive driver is usually damped with a 100 ohm resistor across the output to achieve a clean current waveform when the voltage excursion across the load is small and the low output impedance can be tolerated. This damping resistor may be removed for a high output impedance of no less than 1000 ohms when operating into a highly variable dynamic load. At the present state of silicon trans-

istor development, the PNP silicon transistors used in the positive driver are not as good as the NPN transistors of the negative drivers. Therefore, at least for the near future, it is recommended that the better negative driver be used for reading the core where it is more important to maintain the pulse current waveform and the positive driver to write into the core.

Current Calibrator, CC2000

The current calibrator is used for precise measurements of the current amplitude from each driver or for accurately setting the current output from a driver to a prescribed value. A 1 ohm precision non-inductive resistor is inserted in the ground return of the current drivers and the current waveform is monitored as a voltage waveform across the resistor. A precise 1 volt source is generated within the current calibrator package and applied to a highly linear 10 turn Helipot so that the output voltage from the Helipot can be read directly on its calibrated dial in millivolts or milliamperes. A mechanical chopper is used to alternately present the monitored current waveform and the accurately known output of the Helipot to an oscilloscope in which their amplitudes may be precisely observed by comparison. The same current calibrator may also be used to accurately measure the output of a core in millivolts. The accuracy of the current calibrator is within ± 0.5% of the full scale reading. Two ranges are provided: X1 and X2. In the normal range, X1, the calibrated dial of the 10 turn potentiometer is read directly in millivolts or milliamperes, and the full scale value is 1000. The dial readings are multiplied by 2 in the X2 range which permits accurate measurements of currents up to 2.000 amperes. A polarity reversing switch is provided on the front panel so that either positive or negative going signals can be calibrated. A-c power to the mechanical chopper is provided through an on-off switch.

Univibrator, UVL221, UV2121, UV2323,UVL223

Each univibrator package contains two univibrator circuits for generating a delay and a pulse width. Usually a univibrator package is used with each driver so that the time positioning and pulse width of each current pulse is independently variable. Each univibrator circuit is variable in timing by means of a potentiometer over one of the following decade ranges: 0.1 to 1 microsecond, 1 to 10 microseconds, 10 to 100 microseconds, or 100 to 1000 microseconds. If more than one decade of timing control is re

quired, a dual concentric rotary switch is used to select the necessary timing capacitors in the univibrator circuit. Although a univibrator with all four decade ranges would fulfill all requirements of the Magnetics Tester system, the philosophy carried through here is to use the simplest combinations which would adequately do the job. This leads to simpler and more error-free operation.

The input circuit to the delay univibrator contains a sufficient amount of logical gating circuits to allow the Magnetics Tester system to be self-programming without an actual program generator. A pair of terminals is provided on the front panel of each univibrator package for synchronizing an oscilloscope at the end of each delay period which corresponds in time to the beginning of each drive pulse. Several of these synchronizing signals may be "OR"ed together by simply bussing them together when it is desired to trigger the oscilloscope from more than one drive pulse.

Self-Programming

The Magnetics Tester system in its simplest and least expensive form can be so interconnected to generate its own pulse program without an actual program generator. The various univibrators used to obtain the pulse widths and time delays are connected in a closed loop ring in order to produce and sustain the pulse program. Various repetitive pulses such as half-read and half-write pulses are generated by means of a univibrator feedback loop within a larger loop. These self-programmed Tester systems are semi-fixed program units in that the program may be changed by changing the interconnections of the univibrators. This is easily and quickly accomplished by means of miniature banana patchcord leads.

Some programs, such as those used for measuring uV_1 and dV_1 may be generated from very similar logical interconnections so that a simple switching arrangement may be devised to change the program more rapidly. In general, a univibrator package is required for each negative or positive driver and an additional univibrator package is needed for each group of repetitive pulses.

Program Generator, PG8410

The Magnetics Tester in its most flexible form employs a program generator to provide a virtually infinite variety of pulse programs which may be selected by means of switches on the front panel. The program generator has an oscillator whose frequency is continuously variable from 1 kilocycle to 1 megacycle per second. It may also be operated from an external pulse source in order that the Tester may be synchronized with some other piece of core test equipment or storage system.

A Counter is used to generate an 8-phased signal source for triggering the univibrators which in turn operate the drivers. As many as 4 separate driver channels may be switched in the 8 time slots. Each driver may be driven in any, all, or none of the time slots as desired. Four rows of 8 toggle switches are employed for this purpose. The counting action may be interrupted at any of the 8 phases resulting in a repetitive train of pulses being emitted from the selected time slot(s). A row of 8 toggle switches allows the generation of the repetitive pulse train in any of the 8 phases.

The time duration during which this repetitive action occurs is variable by means of a front panel control from 10 microseconds to 10 milliseconds. The number of these repetitive pulses is therefore dependent upon the setting of the repeat duration control and the oscillator frequency. A pair of terminals is provided on the front panel of the program generator for synchronizing an oscilloscope at the beginning of each selected time slot. This selection is accomplished by means of another row of 8 toggle switches.

Power Supply, PS3600

The power supply provides sufficient power for operating two negative drivers, two positive drivers, and any necessary number of univibrators, a current calibrator, and a program generator. Four drivers of the same polarity may be powered from a single power supply if the average pulse current per driver is limited to 125 ma.

Incorporated into the power supply are two push-button switches for starting and stopping the univibrator ring in the self programming mode. An indicator light is provided which glows when the univibrator ring is oscillating. The other controls are the power control switch, the ac line fuse, and the pilot light.

The Magnetics Tester operates from a 115 volt, single phase, AC power connection and requires approximately 1 ampere of current.

Tandem Operation

A Magnetics Tester with up to 8 drivers is available by coupling two units together. The compact size, the low cost, and the extreme flexibility of the unit make this arrangement feasible. Such an arrangement is available for both the self-programmed and forced programmed types.

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Thank you for your recent inquiry. We are pleased to enclose literature on the Magnetic Core Tester.

The long history of our personnel in the field of magnetic cores and memories has given us the experience and know-how to provide a quality product to you.

This series of Magnetic Core Testers will enable Electronic Memories, Inc. to provide the industry with a complete line of memory products -- from ferrite cores, arrays and stacks to complete memories and testers.

Prices on the Testers are as follows:

Model 102		
	Rack Mounted:	$4,500
	Bench Type:	$4,650
Model 150		
	Rack Mounted:	$5,950
	Bench Type:	$6,100

Prices of other models on request.

Delivery can be made approximately 30 days from order.

Please let us know how we may be of service to you, by contacting us or our representative nearest you.

Sincerely,

Jack Ogg
Product Manager

JO:yh
Enclosures

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WHO TOOK THE DESTRUCT OUT OF COINCIDENT CURRENT MEMORIES ?

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LOS ANGELES CALIF

U.S. POSTAGE
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RCA
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NEEDHAM 94 MASS
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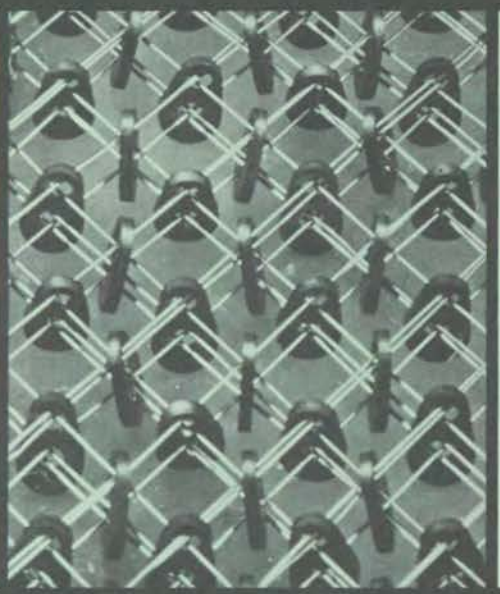
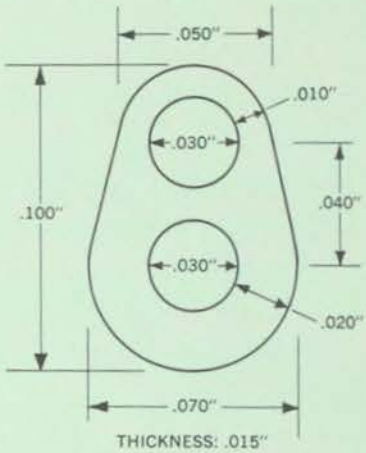


MECHANICAL SPECIFICATIONS



THICKNESS: .015"

THE SHMOO, THAT'S WHO !

Want to use the same drive circuitry for a non-destructive, coincident current core memory or for a "scratch pad" memory? Need a two hole core that can be easily oriented for automatic stringing and testing? Looking for a multi-aperture core with Read hole physical and electrical characteristics that match a 50mil toroid?

Better ask Electronic Memories about their 101-1002 transfluxor core.

The first customer to see this core said it looked like a "shmoo." The name stuck. So next time you hear a memory man say "shmoo," you'll know he's talking about a multi-aperture core especially designed for a non-destruct, coincident current memory application.

The "shmoo" is no scientific oddity. It's available, now, individually, in arrays and stacks, or in completely assembled memories. May we send you more complete information?

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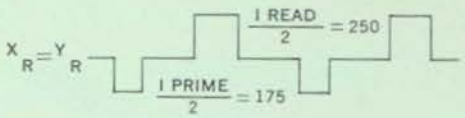
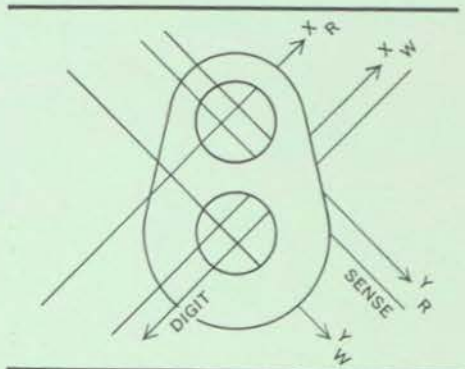
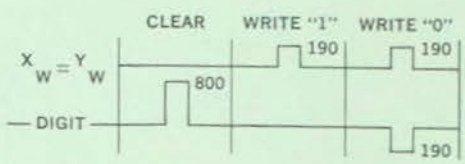
TYPICAL USE IN A MEMORY SYSTEM







td=2.0 μs tv=2.0 μs

TYPICAL OUTPUTS WHEN DRIVEN AS ABOVE AT 25°C

	uv (mv)	tp (μs)	ts (μs)	dvz (mv)
READ	79	.37	.59	20.

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MEMORY CORE CHARACTERISTICS SUMMARY

TYPE	SIZE (mils)	RECOMMENDED DRIVE CURRENTS @ 25°C			TYPICAL OUTPUT SIGNALS			
	OD/ID/Ht	Drive (ma turns)	Rise Time (μsec)	Pulse Width (μsec)	uV_1 (mv)	dV_Z (mv)	Peak Time (μsec)	Switch Time (μsec)
COINCIDENT CURRENT								
31-100	30/20/7	500/250	0.05	0.6	60	8	0.17	0.37
31-103	30/20/7	580/290	0.1	0.6	58	6	0.24	0.38
31-108	30/20/7	720/360	0.1	0.6	62	5	0.21	0.39
31-101	30/20/7	400/200	0.1	0.6	48	6	0.23	0.45
32-100	30/20/7	400/200	0.2	1.5	37	2	0.41	0.77
31-581	50/30/15	540/270	0.15	1.0	70	7	0.33	0.68
51-101	50/30/15	520/260	0.15	1.0	110	15	0.32	0.65
51-106	50/30/15	500/250	0.2	1.2	90	9	0.43	0.75
51-110	50/30/15	500/250	0.2	2.0	68	8	0.52	1.02
51-119	50/30/15	400/200	0.5	3.0	90	5	0.75	1.25
51-113	50/30/15	380/190	0.2	2.0	54	8	0.65	1.35
51-111	50/30/15	350/175	0.5	3.0	59	6	0.86	1.50
81-101	80/50/25	630/315	0.2	3.0	170	15	0.52	1.04
81-104	80/50/25	400/200	0.5	5.0	55	5	1.60	3.00
WORD SELECT								
31-105	30/20/7	380/95/90	0.1	0.12 & 0.4	35	6	0.10	0.175
51-114	50/30/15	450/130/120	0.1	0.2 & 0.4	75	16	0.11	0.23
51-109	50/30/15	550/160/140	0.1	0.2 & 0.4	120	25	0.15	0.25

(over)

MEMORY CORE CHARACTERISTICS SUMMARY (cont.)

TYPE	SIZE (mils)	RECOMMENDED DRIVE CURRENTS @ 25°C			TYPICAL OUTPUT SIGNALS			
	OD/ID/Ht	Drive (ma turns)	Rise Time (μsec)	Pulse Width (μsec)	uV_1 (mv)	dV_Z (mv)	Peak Time (μsec)	Switch Time (μsec)
LITHIUM CORES (For Medium Temperature Range Applications, -55°C to +85°C)								
34-100	30/20/7	540/270	0.2	1.5	27	2	0.42	0.75
54-100	50/30/15	820/410	0.2	1.5	75	9	0.43	0.8
ISODRIVE® CORES (For Wide Temperature Range Applications, -65°C to +125°C)								
36-101	30/20/9	650/325	0.2	1.5	36	3.5	0.32	0.5
46-100	40/28/8	900/450	0.1	2.0	59	10	0.22	0.47
56-102	50/30/15	1000/500	0.2	2.0	117	14	0.36	0.80

SWITCH CORES

100, 140, 180 mil sizes available.

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OCT - 7 65

MEMORY CORE CHARACTERISTICS SUMMARY

TYPE	SIZE (mils)	RECOMMENDED DRIVE CURRENTS @ 25°C			TYPICAL OUTPUT SIGNALS			
	OD/ID/Ht	Drive (ma turns)	Rise Time (μsec)	Pulse Width (μsec)	uV_1 (mv)	dV_Z (mv)	Peak Time (μsec)	Switch Time (μsec)
COINCIDENT CURRENT								
31-100	30/20/7	500/250	0.05	0.6	60	8	0.17	0.37
31-103	30/20/7	580/290	0.1	0.6	58	6	0.24	0.38
31-108	30/20/7	720/360	0.1	0.6	62	5	0.21	0.39
32-100	30/20/7	400/200	0.2	1.5	37	2	0.41	0.77
51-101	50/30/15	520/260	0.15	1.0	110	15	0.32	0.65
51-106	50/30/15	500/250	0.2	1.2	90	9	0.43	0.75
51-110	50/30/15	500/250	0.2	2.0	68	8	0.52	1.02
51-119	50/30/15	400/200	0.5	2.0	90	5	0.75	1.25
51-113	50/30/15	380/190	0.2	2.0	54	8	0.65	1.35
51-111	50/30/15	350/175	0.5	3.0	59	6	0.86	1.50
-101	50/30/15	540/270	0.15	1.0	70	7	0.33	0.68
81-101	80/50/25	630/315	0.2	2.0	170	15	0.52	1.04
81-104	80/50/25	400/200	0.5	5.0	55	5	1.60	3.00
WORD SELECT								
31-105	30/20/7	380/95/90	0.1	0.12 & 0.4	35	6	0.10	0.175
51-114	50/30/15	450/130/120	0.1	0.2 & 0.4	75	16	0.11	0.23
51-109	50/30/15	550/160/140	0.1	0.2 & 0.4	120	25	0.15	0.25
LITHIUM CORES (For Medium Temperature Range Applications, -55°C to +85°C)								
34-100	30/20/7	540/270	0.2	1.5	27	2	0.42	0.75
54-100	50/30/15	820/410	0.2	1.5	75	9	0.43	0.8
ISODRIVE® CORES (For Wide Temperature Range Applications, -65°C to +125°C)								
36-101	30/20/9	700/350	0.2	1.0	44	6	0.33	0.58
TRANSFLUXOR								
101-1002 (Shmoo)	.1/.07/.015	Read 500/250	0.2	2.0)	79	20	0.37	0.59
		Write 380/190	0.2	2.0)				
		Prime 350/175	0.2	2.0)				
		Clear 800	0.2	2.0)				
SWITCH CORES - 100, 140, 180 mil sizes available.								

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MEMORY CORE CHARACTERISTICS SUMMARY

TYPE	SIZE (mils)	RECOMMENDED DRIVE CURRENTS @ 25°C			TYPICAL OUTPUT SIGNALS			
	OD/ID/Ht	Drive (ma turns	Rise Time (μsec)	Pulse Width (μsec)	uV_1 (mv)	dV_z (mv)	Peak Time (μsec)	Switch Time (μsec)
COINCIDENT CURRENT								
31-103	30/20/7	580/290	0.1	2.0	58	6	0.24	0.38
31-101	30/20/7	420/210	0.1	0.6	55	8	0.20	0.40
38-101	30/20/7	470/235	0.1	0.5	30	4.5	0.22	0.43
58-100	50/30/15	720/375	0.1	1.0	83	10.5	0.22	0.42
51-101	50/30/15	520/260	0.15	1.0	110	15	0.32	0.65
51-106	50/30/15	500/250	0.2	1.2	90	9	0.43	0.75
1-110	50/30/15	500/250	0.2	2.0	68	8	0.52	1.02
51-113	50/30/15	380/190	0.2	2.0	54	8	0.65	1.35
51-111	50/30/15	350/175	0.5	3.0	59	6	0.86	1.50
81-101	80/50/25	630/315	0.2	3.0	170	15	0.52	1.04
81-104	80/50/25	400/200	0.5	5.0	55	5	1.60	3.00
WORD SELECT								
31-105	30/20/7	380/95/90	0.1	0.12 & 0.4	35	6	0.10	0.175
51-114	50/30/15	450/130/120	0.1	0.2 & 0.4	75	16	0.11	0.23
51-109	50/30/15	550/160/140	0.1	0.2 & 0.4	120	25	0.15	0.25
ISODRIVE® *								
36-100	30/20/9	600/300	0.2	1.5	35	5	0.40	0.85
46-100	40/28/8	900/450	0.1	2.0	59	10	0.22	0.47
56-101	50/30/15	1000/500	0.2	2.0	102	11	0.40	0.86
56-102	50/30/15	1000/500	0.2	2.0	117	14	0.36	0.80

* For Wide Temperature Range Applications (-55°C to +100°C)

DEFINITIONS

I = Drive Current Amplitude. Value of the flat top portion of current used to switch core.

I_p = Peak Amplitude Current Pulse. Overshoot value of drive current.

I_w = Write Current Pulse which is the value of current used to switch the core from the ZERO to ONE state.

I_r = Read Current Pulse which is the value of current used to switch the core from the ONE state to the ZERO state.

I_{pw} = Partial Write Current Pulse is the value of write current which magnetically disturbs the core in the ZERO state, but does not switch it to the ONE state. A core that has been subjected to one or more partial write pulses is defined as being in the disturbed ZERO state (dV_z).

I_{pr} = Partial Read Current Pulse is the value of read current which magnetically disturbs the core in the ONE state but does not switch it to the ZERO state. A core which has been subjected to one or more partial read pulses is defined as being in the disturbed ONE state (dV_1).

I_k = (knee) The value of I_{pw} (direct current mmf) required to reach the switching threshold of the non-recoverable flux, when applying an mmf in the direction to switch the remnant state.

$\frac{I_k}{I}$ = The disturb ratio is the knee current I_k divided by the full switching mmf (pulse current) used to switch the remnant state of the core.

t_o = Reference Time, designated as the time when the drive current pulse reaches 10% of I on the rise of the read pulse.

t_r = Rise Time of the drive current pulse from t_o to 90% of I.

t_w = Pulse Width, or the time the drive current pulse remains above the 90% level.

t_f = Fall Time of the drive current pulse from 90% to 10% of I.

t_p = Peaking Time. Time between t_o and peak output voltage for a ONE.

t_s = Switching Time. Time between t_o and the time where the output voltage has decreased to 10% of its peak value for a ONE.

uV_1 = Peak Output Voltage developed when a read current pulse I_r is applied to a core in the undisturbed ONE state.

dV_1 = Peak Output Voltage developed when a read current pulse I_r is applied to a core in the disturbed ONE state.

dV_z = Peak Output Voltage developed when a read current pulse is applied to a core in the disturbed ZERO state.

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FERRITE CORE SPECIFICATION

FAST SWITCHING
WORD SELECT CORE

Type 31-105

The FAST SWITCHING WORD SELECT CORE is intended for use in ultra-high speed word select memory systems having memory cycle times under 1 microsecond. The FAST SWITCHING WORD SELECT CORE may be used in either the partial flux switching mode or in the full flux switching mode.

MECHANICAL SPECIFICATIONS:

Outside Diameter	0.029 ± 0.001 inch
Inside Diameter	0.020 ± 0.001 inch
Thickness	0.0065 ± 0.0005 inch

ELECTRICAL SPECIFICATIONS FOR PARTIAL FLUX SWITCHING:

Typical Operating Conditions

Temperature: 25°C

Drive Pulse	Read (I_r)	Write (I_W)	Digit (I_D)
Amplitude	380 ma	95 ma	90 ma
Pulse Width	0.12 μs	0.4 μs	0.4 μs
Pulse Rise Time	0.1 μs	0.1 μs	0.1 μs
Pulse Fall Time	0.1 μs	0.1 μs	0.1 μs

Typical Output Signals

Temperature: 25°C

Switching Time (t_s)	0.175 μs
Peaking Time (t_r)	0.097 μs
Amplitude ONE (uV_1)	35 mv
Amplitude ZERO dV_z)	6.5 mv

GENERAL:

Cores are delivered 100% tested to mechanical and electrical specifications or to statistical quality level of AQL 0.015 or 6.5 as defined by MIL-STD-105B, Inspection Level II. Cores are electrically tested as defined by the Test Specifications on the next page.

CORE TEST SPECIFICATION

FAST SWITCHING
WORD SELECT CORE

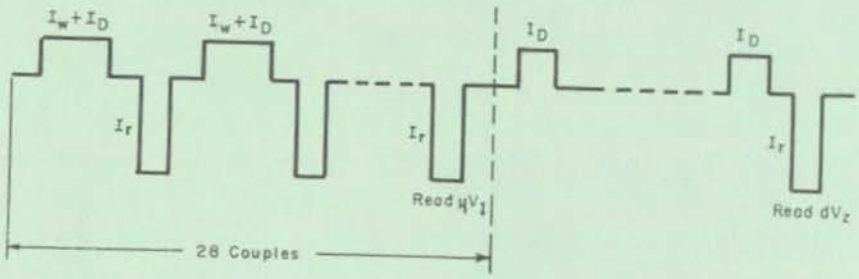
Type 31-105

ELECTRICAL TEST SPECIFICATIONSAAT 25°C ± 1°C:

	Drive Pulse	t_w	t_r 10% to 90% linear	t_f	
I_r	360 ± 3.6 ma	0.12 μs	0.1 ± 0.01 μs	0.1 ± 0.01 μs	Over-
I_w	85 ± 0.85 ma	0.4 μs	0.1 ± 0.01 μs	0.1 ± 0.01 μs	shoot
I_D	100 ± 1.0 ma	0.4 μs	0.1 ± 0.01 μs	0.1 ± 0.01 μs	and droop 1%

Pulse Program

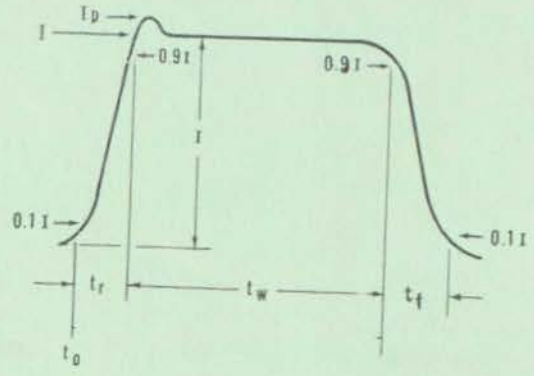
Pulse rate 200 kc

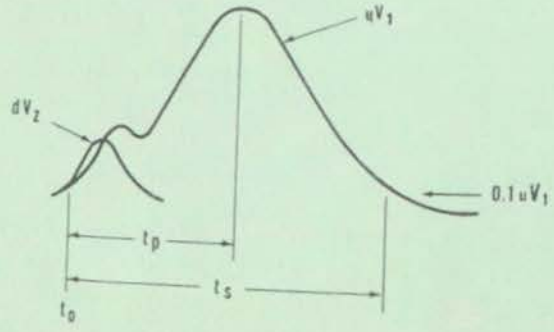


Output Test Signals:

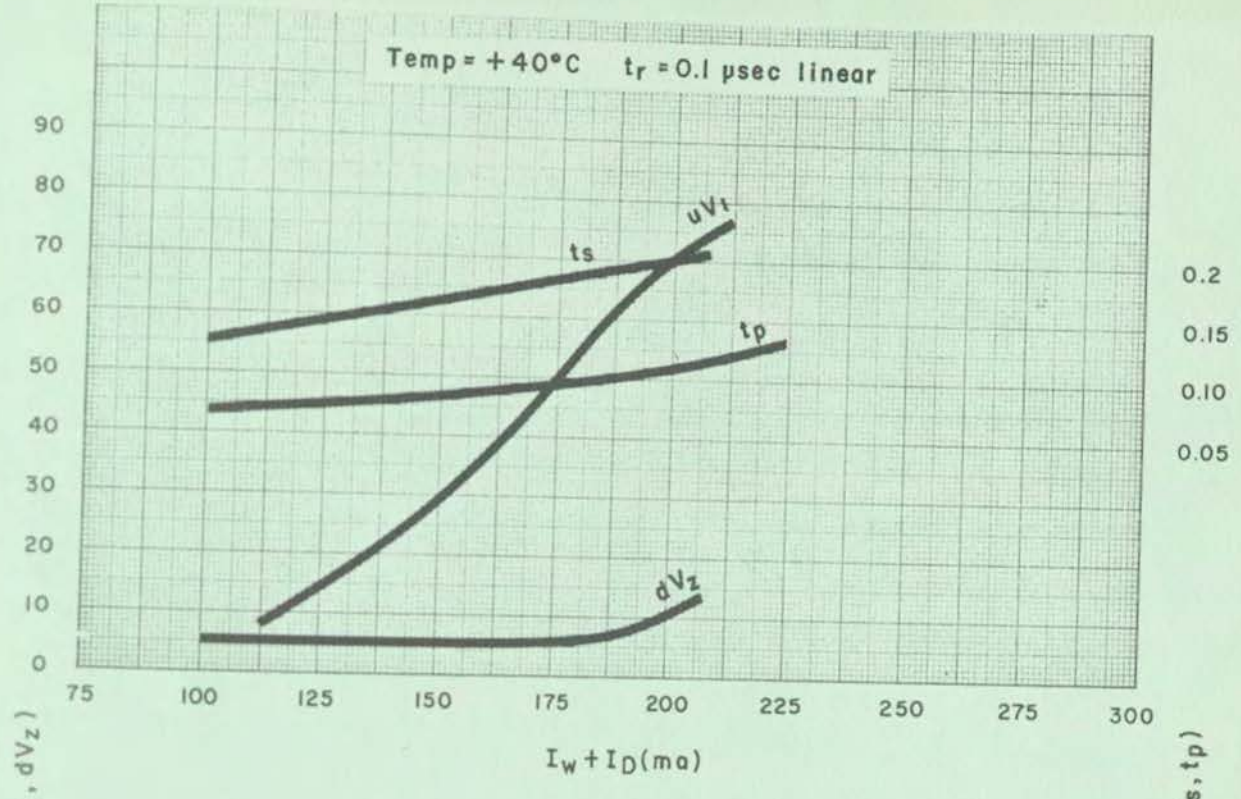
uV_1 ---------- 24 mv min.
dV_z ---------- 7.5 mv max.
t_p ---------- 0.1 ± .01 μsec.
t_s ---------- 0.190 μs max.

DEFINITIONS:

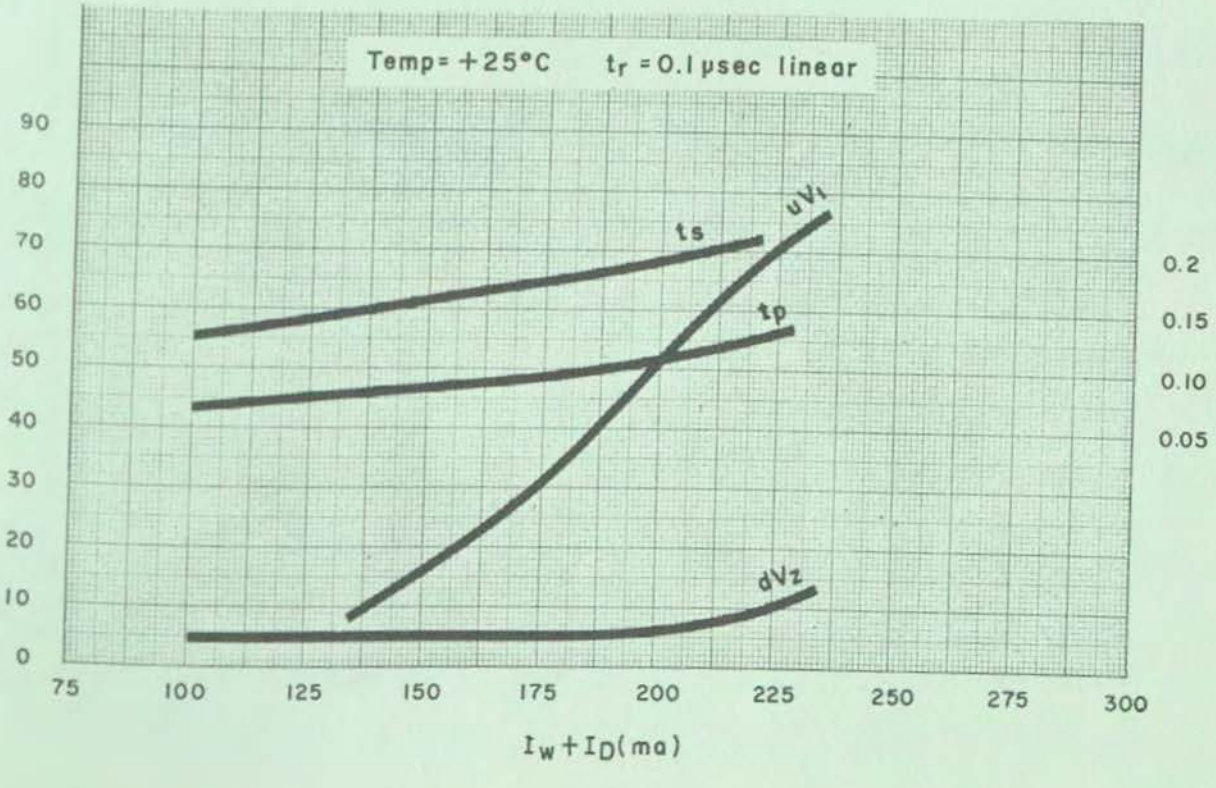




31-105 CORE PARAMETERS VS DRIVE



31-105 CORE PARAMETERS VS DRIVE



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DEFINITIONS

I = Drive Current Amplitude. Value of the flat top portion of current used to switch core.

I_p = Peak Amplitude Current Pulse. Overshoot value of drive current.

I_w = Write Current Pulse which is the value of current used to switch the core from the ZERO to ONE state.

I_r = Read Current Pulse which is the value of current used to switch the core from the ONE state to the ZERO state.

I_{pw} = Partial Write Current Pulse is the value of write current which magnetically disturbs the core in the ZERO state, but does not switch it to the ONE state. A core that has been subjected to one or more partial write pulses is defined as being in the disturbed ZERO state (dV_z).

I_{pr} = Partial Read Current Pulse is the value of read current which magnetically disturbs the core in the ONE state but does not switch it to the ZERO state. A core which has been subjected to one or more partial read pulses is defined as being in the disturbed ONE state (dV_1).

I_k = (knee) The value of I_{pw} (direct current mmf) required to reach the switching threshold of the non-recoverable flux, when applying an mmf in the direction to switch the remnant state.

$\frac{I_k}{I}$ = The disturb ratio is the knee current I_k divided by the full switching mmf (pulse current) used to switch the remnant state of the core.

t_o = Reference Time, designated as the time when the drive current pulse reaches 10% of I on the rise of the read pulse.

t_r = Rise Time of the drive current pulse from t_o to 90% of I.

t_w = Pulse Width, or the time the drive current pulse remains above the 90% level.

t_f = Fall Time of the drive current pulse from 90% to 10% of I.

t_p = Peaking Time. Time between t_o and peak output voltage for a ONE.

t_s = Switching Time. Time between t_o and the time where the output voltage has decreased to 10% of its peak value for a ONE.

uV_1 = Peak Output Voltage developed when a read current pulse I_r is applied to a core in the undisturbed ONE state.

dV_1 = Peak Output Voltage developed when a read current pulse I_r is applied to a core in the disturbed ONE state.

dV_z = Peak Output Voltage developed when a read current pulse is applied to a core in the disturbed ZERO state.

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FERRITE CORE SPECIFICATION

COINCIDENT CURRENT
MEMORY CORE

Type 34-100

The Type 34-100 COINCIDENT CURRENT MEMORY CORE is a 30 mil, fast switching core intended for use without temperature compensation. The core may be operated over any 80° range from -40°C to +100°C. The switching time characteristics of the Type 34-100 allow for its use in memory systems with cycle times of 4 to 5 microseconds.

MECHANICAL SPECIFICATIONS:

Outside Diameter	0.030 ± 0.0015 inch
Inside Diameter	0.020 ± 0.0015 inch
Thickness	0.007 ± 0.001 inch

ELECTRICAL SPECIFICATIONS:

Typical Operating Conditions @ 25°C	0.65	0.60
Disturb Ratio:	540/270	600/300 ma turns
Drive Pulse (I)	1.5 μs	1.5 μs
Pulse Width (t_w)	0.2 μs	0.2 μs
Pulse Rise Time (t_r)	0.2 μs	0.2 μs
Pulse Fall Time (t_f)		
Typical Output Signals @ 25°C		
Amplitude ONE (uV_1)	27 mv	40 mv
Amplitude ZERO (dV_z)	2 mv	2 mv
Peaking Time (t_p)	0.42 μs	0.40 μs
Switching Time (t_s)	0.75 μs	0.75 μs

GENERAL:

Cores are delivered 100% tested to mechanical and electrical specifications or to statistical quality level of AQL 0.015 or 6.5 as defined by MIL-STD-105C, Inspection Level II. Cores are electrically tested as defined by the Test Specifications on the next page.

CORE TEST SPECIFICATION

COINCIDENT CURRENT
MEMORY CORE

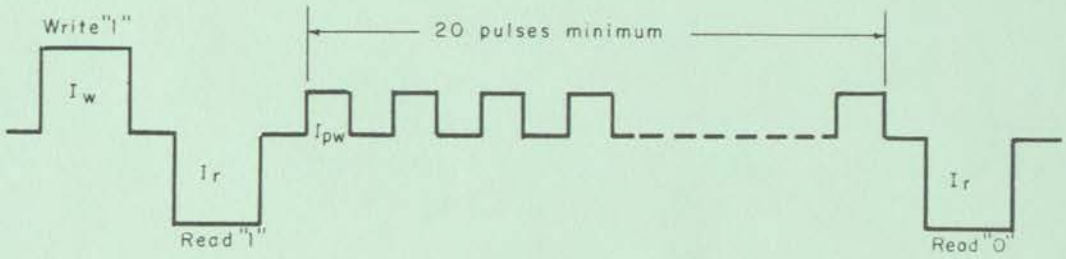
Type 34-100

ELECTRICAL TEST SPECIFICATIONS @ 25°± 1°C:

	Drive Pulse	t_w	t_r 10% to 90% linear	t_f	
I_r	530 ± 5.3 ma	3 μs	0.2 ± .02 μs	0.2 ± .02 μs	Over-shoot & droop ± 1%
I_w	530 ± 5.3 ma	3 μs	0.2 ± .02 μs	0.2 ± .02 μs	
$I_{pr}=I_{pw}$	345 ± 3.45 ma	3 μs	0.2 ± .02 μs	0.2 ± .02 μs	

Pulse Program

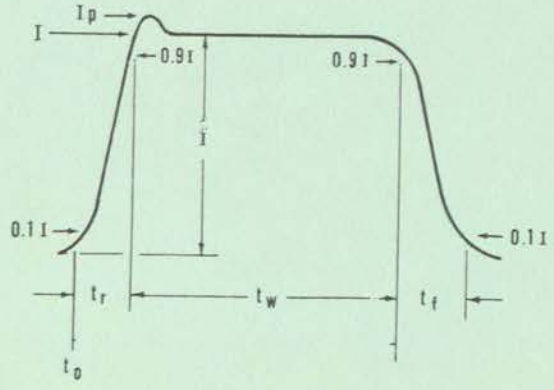
Pulse rate 20 kc.

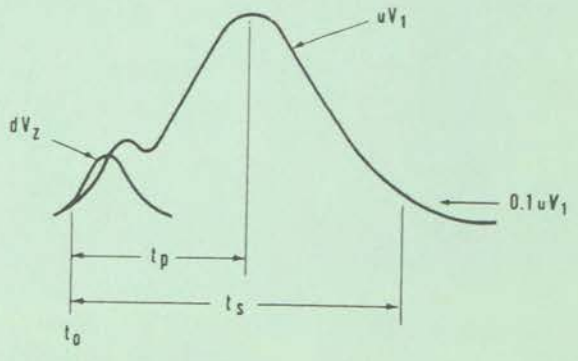


Output Test Signals:

uV_1	----------	20 mv min.
dV_Z	----------	5 mv max.
t_p	----------	0.43 ± .04 μs
t_s	----------	0.82 μs max.

DEFINITIONS:





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FERRITE CORE SPECIFICATION

ISODRIVE CORE
Type 36-101

The ISODRIVE CORE is a fast switching, high drive core intended for use in severe environments. The ISODRIVE CORE has an excellent disturb ratio over the temperature range of -70°C to +100°C. Current compensation of the drive system is not necessary.

MECHANICAL SPECIFICATIONS:

Outside Diameter	.031 ± .002 inch
Inside Diameter	.020 ± .002 inch
Thickness	.007 ± .001 inch

ELECTRICAL SPECIFICATIONS:

Recommended Operating Conditions

Temperature Range:	-70°C to +100°C
Drive Pulse (I)	700 mA turns
Pulse Width (t_w)	1.0 μs
Pulse Rise Time (t_r)	0.2 μs
Pulse Fall Time (t_f)	0.2 μs

Typical Output Signals

Temperature:	-70°C	+25°C	+100°C
Amplitude ONE (uV_1)	38 mv	44 mv	65 mv
Amplitude ZERO (dV_z)	6 mv	6 mv	6 mv
Peaking Time (t_p)	0.34 μs	0.33 μs	0.27 μs
Switching Time (t_s)	0.59 μs	0.58 μs	0.50 μs

GENERAL:

Cores are delivered 100% tested to mechanical and electrical specifications or to statistical quality level of AQL 0.015 or 6.5 as defined by MIL-STD-105C, Inspection Level II. Cores are electrically tested as defined by the Test Specifications on the next page.

CORE TEST SPECIFICATION

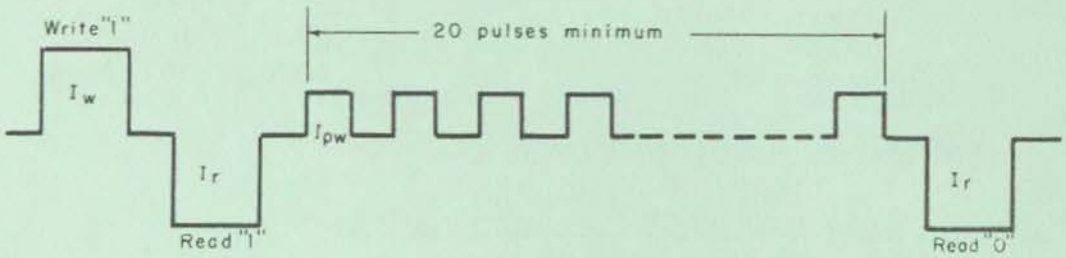
ISODRIVE CORE
Type 36-101

ELECTRICAL SPECIFICATIONS AT 25°C ± 1°C:

	Drive Pulse	t_w	t_r 10% to 90% linear	t_f	
I_r	650 ± 6.5 ma	1 μs	0.2 ± .02 μs	0.2 ± .02 μs	Over-shoot & Droop 1%
I_w	650 ± 6.5 ma	1 μs	0.2 ± .02 μs	0.2 ± .02 μs	
$I_{pr}=I_{pw}$	450 ± 4.5 ma	1 μs	0.2 ± .02 μs	0.2 ± .02 μs	

Pulse Program

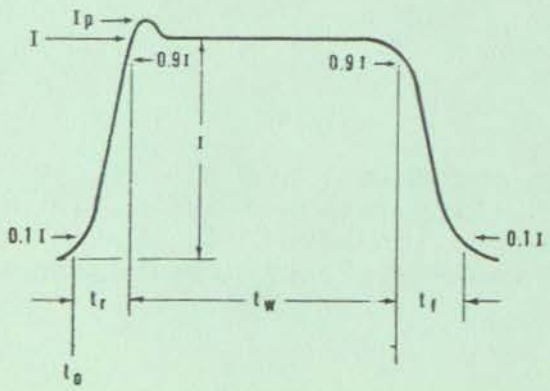
Pulse Rate 20 kc.

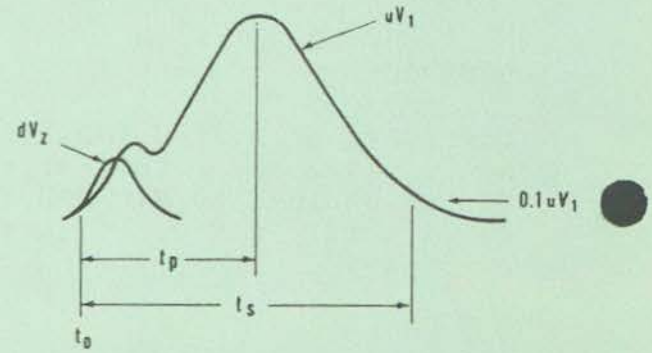


Output Test Signals:

uV_1	----------	30 mv min.
dV_z	----------	8 mv max.
t_p	----------	0.32 ± .03 μs
t_s	----------	0.60 μs max.

DEFINITIONS:





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FERRITE CORE SPECIFICATION

WORD SELECT CORE
Type 51-109

The WORD SELECT CORE is intended for use in very fast word select memory systems having memory cycle times up to 1 megacycle. The WORD SELECT CORE may be used in either the partial flux switching mode or in the full flux switching mode.

MECHANICAL SPECIFICATIONS:

Outside Diameter	0.050 ± 0.002 inch
Inside Diameter	0.030 ± 0.002 inch
Thickness	0.015 ± 0.002 inch
Die Fins	0.001 max

ELECTRICAL SPECIFICATIONS FOR PARTIAL FLUX SWITCHING:

Typical Operating Conditions

Temperature: 25°C

Drive Pulse	Read (I_r)	Write (I_w)	Digit (I_D)
Amplitude	550 ma	160 ma	140 ma
Pulse Width (t_w)	0.2 μs	0.4 μs	0.4 μs
Pulse Rise Time (t_r)	0.1 μs	0.1 μs	0.1 μs
Pulse Fall Time (t_f)	0.1 μs	0.1 μs	0.1 μs

Typical Output Signals

Temperature: 25°C

Switching Time (t_s)	0.25 μs
Peaking Time (t_p)	0.145 μs
Amplitude ONE (uV_1)	120 mv
Amplitude ZERO (dV_z)	25 mv

GENERAL:

Cores are delivered 100% tested to mechanical and electrical specifications or to statistical quality level of AQL 0.015 or 6.5 as defined by MIL-STD-105B, Inspection Level II. Cores are electrically tested as defined by the Test Specifications on the next page.

CORE TEST SPECIFICATION

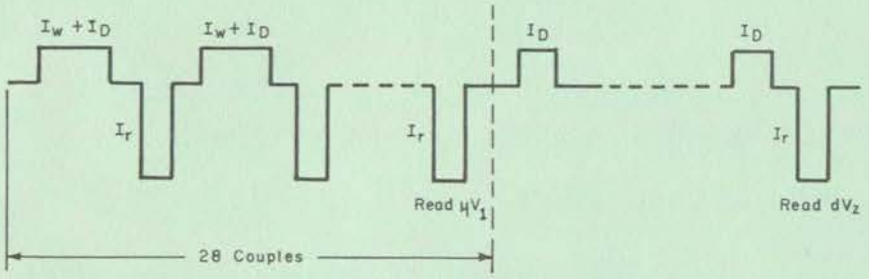
WORD SELECT CORE
Type 51-109

ELECTRICAL TEST SPECIFICATIONS AT 25°C ± 1°C:

Drive Pulse		t_w	t_r 10% to 90% linear	t_f	
I_r	500 ± 5 ma	0.2 μs	0.1 ± .005 μs	0.15 ± .0075 μs	Over-shoot and droop ± 3%
I_w	135 ± 1.4 ma	0.4 μs	0.15 ± .015 μs	0.15 ± .015 μs	
I_D	150 ± 1.5 ma	0.4 μs	0.15 ± .015 μs	0.15 ± .015 μs	

Pulse Program

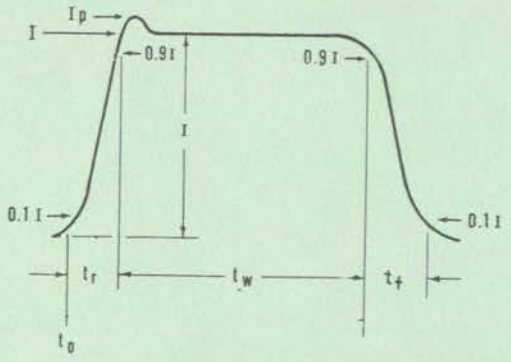
Pulse rate 200 kc

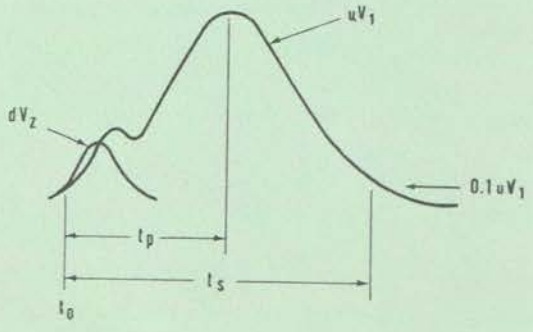


Output Test Signals

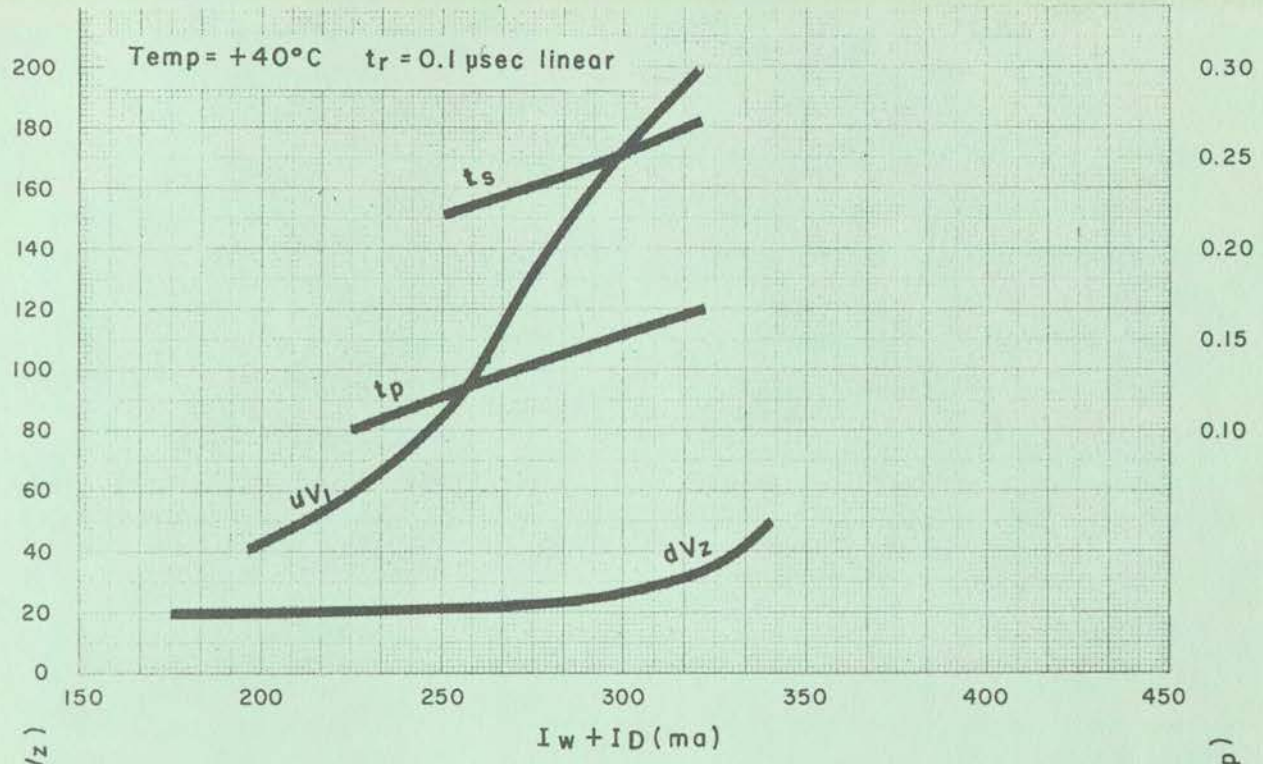
uV_1 --------- 85 mv min.
dV_z --------- 27 mv max.
t_p --------- 0.145 ± 0.005 μs
t_s --------- 0.25 μs max.

DEFINITIONS:

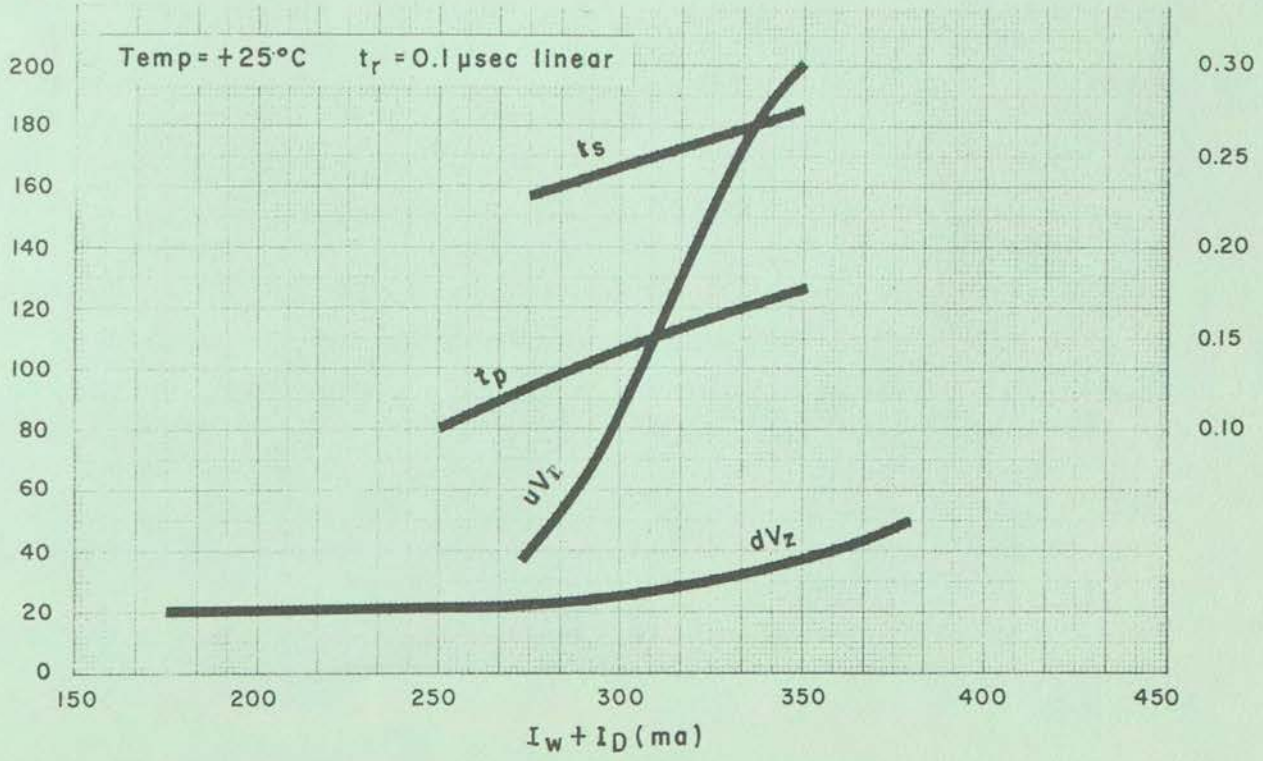




51-109 CORE PARAMETERS VS DRIVE



51-109 CORE PARAMETERS VS DRIVE



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DEFINITIONS

I = Drive Current Amplitude. Value of the flat top portion of current used to switch core.

I_p = Peak Amplitude Current Pulse. Overshoot value of drive current.

I_w = Write Current Pulse which is the value of current used to switch the core from the ZERO to ONE state.

I_r = Read Current Pulse which is the value of current used to switch the core from the ONE state to the ZERO state.

I_{pw} = Partial Write Current Pulse is the value of write current which magnetically disturbs the core in the ZERO state, but does not switch it to the ONE state. A core that has been subjected to one or more partial write pulses is defined as being in the disturbed ZERO state (dV_z).

I_{pr} = Partial Read Current Pulse is the value of read current which magnetically disturbs the core in the ONE state but does not switch it to the ZERO state. A core which has been subjected to one or more partial read pulses is defined as being in the disturbed ONE state (dV_1).

I_k = (knee) The value of I_{pw} (direct current mmf) required to reach the switching threshold of the non-recoverable flux, when applying an mmf in the direction to switch the remnant state.

$\frac{I_k}{I}$ = The disturb ratio is the knee current I_k divided by the full switching mmf (pulse current) used to switch the remnant state of the core.

t_o = Reference Time, designated as the time when the drive current pulse reaches 10% of I on the rise of the read pulse.

t_r = Rise Time of the drive current pulse from t_o to 90% of I.

t_w = Pulse Width, or the time the drive current pulse remains above the 90% level.

t_f = Fall Time of the drive current pulse from 90% to 10% of I.

t_p = Peaking Time. Time between t_o and peak output voltage for a ONE.

t_s = Switching Time. Time between t_o and the time where the output voltage has decreased to 10% of its peak value for a ONE.

uV_1 = Peak Output Voltage developed when a read current pulse I_r is applied to a core in the undisturbed ONE state.

dV_1 = Peak Output Voltage developed when a read current pulse I_r is applied to a core in the disturbed ONE state.

dV_z = Peak Output Voltage developed when a read current pulse is applied to a core in the disturbed ZERO state.

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FERRITE CORE SPECIFICATION

LOW DRIVE
COINCIDENT CURRENT CORE

Type 51-111

The Type 51-111 LOW DRIVE COINCIDENT CURRENT CORE is for use in memories of the medium speed class of 6 to 8 microseconds cycle.

MECHANICAL SPECIFICATIONS:

Outside Diameter	0.050 ± 0.002 inch
Inside Diameter	0.030 ± 0.002 inch
Thickness	0.015 ± 0.002 inch

ELECTRICAL SPECIFICATIONS:

Typical Operating Conditions

Temperature: 25°C

Drive Pulse	350/175 ma turns
Pulse Width (t_w)	3 μs
Pulse Rise Time (t_r)	0.5 ± 0.05 μs linear
Pulse Fall Time (t_f)	0.5 μs

Typical Output Signals

Temperature: 25°C

Switching Time (t_s)	1.5 μs
Peaking Time (t_p)	0.86 μs
Amplitude ONE (uV_1)	55 mv
Amplitude ZERO (dV_z)	5.5 mv

GENERAL:

Cores are delivered 100% tested to mechanical and electrical specifications or to statistical quality level of AQL 0.015 or 6.5 as defined by MIL-STD-105B, Inspection Level II. Cores are electrically tested as defined by the Test Specifications on the next page.

CORE TEST SPECIFICATION

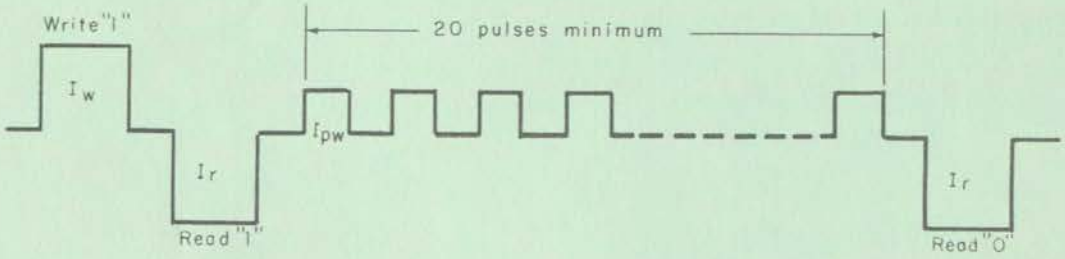
LOW DRIVE
COINCIDENT CURRENT CORE
Type 51-111

ELECTRICAL TEST SPECIFICATIONS AT 25°C ± 1°C:

	Drive Pulse	t_w	t_r 10% to 90% linear	t_f	
I_r	315 ± 3.15 ma	3 μs	0.5 ±0.05 μs	0.5 ±0.05 μs	Over-
I_w	315 ± 3.15 ma	3 μs	0.5 ±0.05 μs	0.5 ±0.05 μs	shoot
$I_{pr}=I_{pw}$	192 ± 1.92 ma	3 μs	0.5 ±0.05 μs	0.5 ±0.05 μs	and droop 1%

Pulse Program

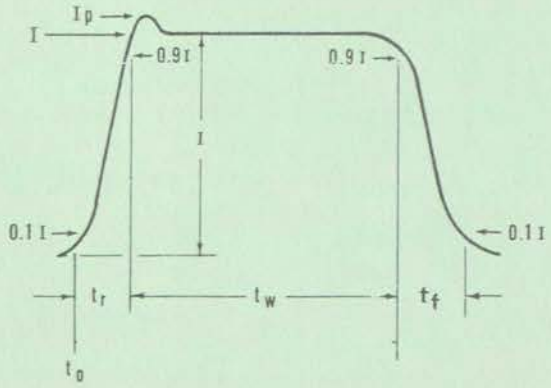
Pulse rate 20 kc

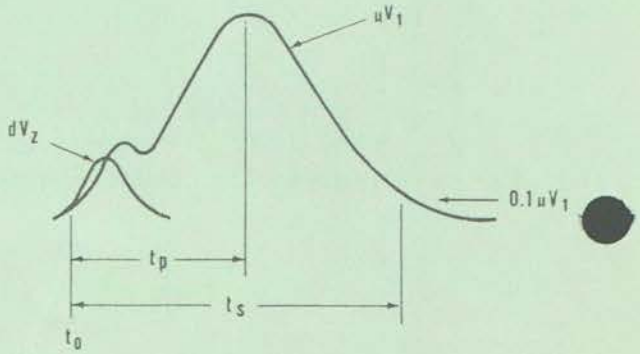


Output Test Signals:

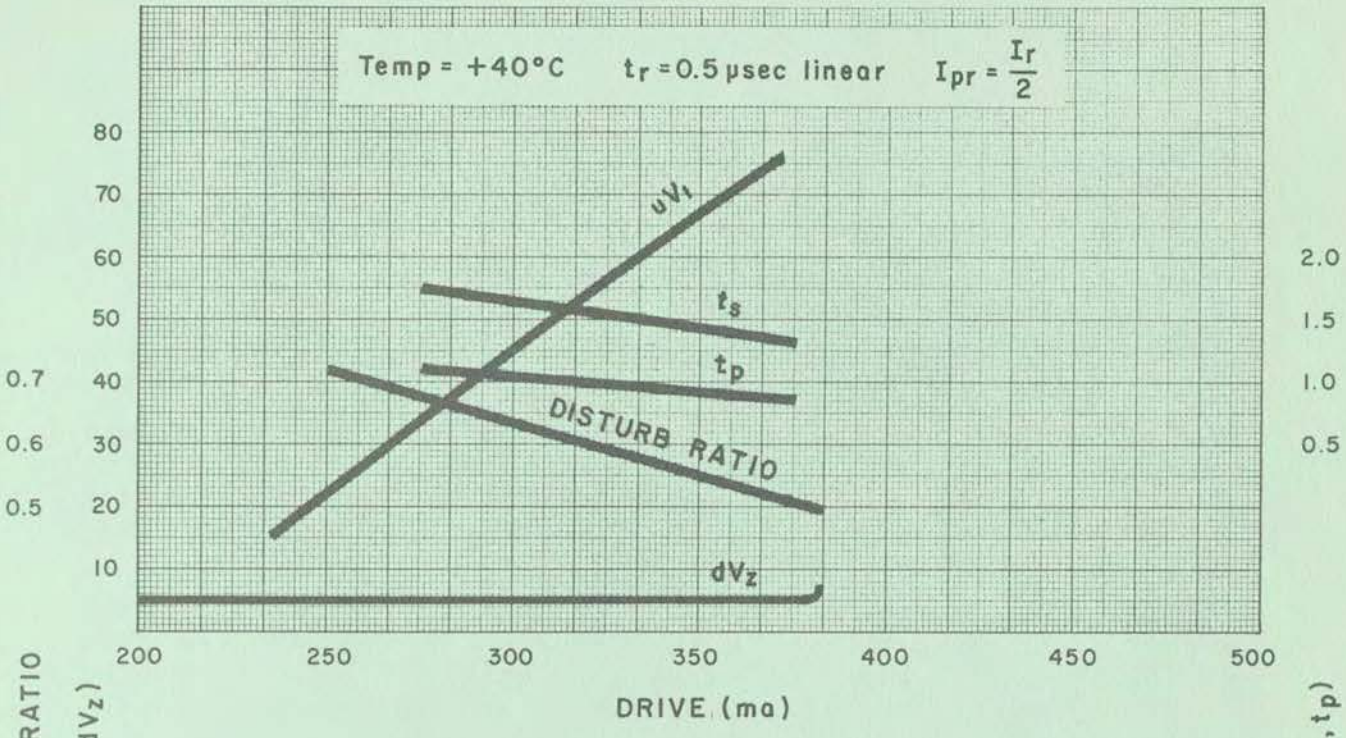
uV_1 --------- 37 mv min.
dV_z --------- 7.5 mv max.
t_p --------- 0.90 ± 0.05 μsec
t_s --------- 1.65 μsec max.

DEFINITIONS:

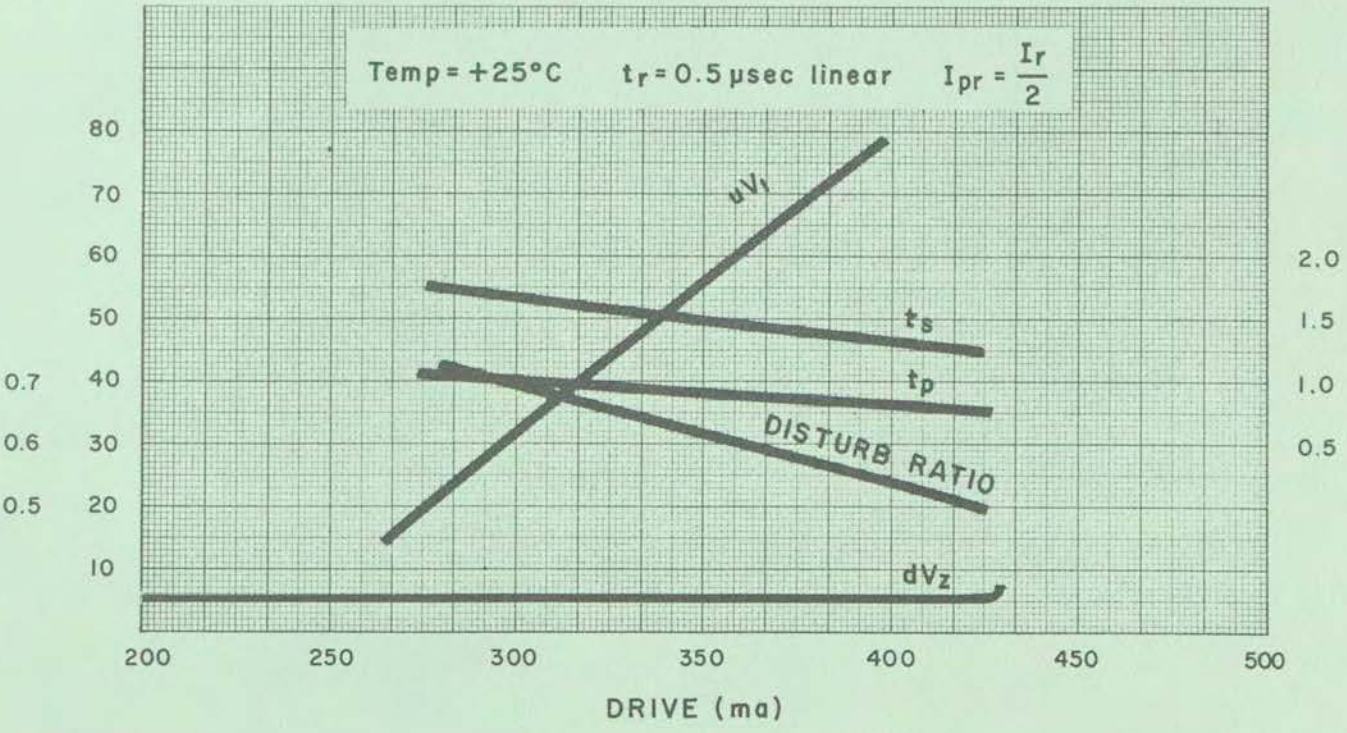




51-111 CORE PARAMETERS VS DRIVE



51-111 CORE PARAMETERS VS DRIVE



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DEFINITIONS

I = Drive Current Amplitude. Value of the flat top portion of current used to switch core.

I_p = Peak Amplitude Current Pulse. Overshoot value of drive current.

I_w = Write Current Pulse which is the value of current used to switch the core from the ZERO to ONE state.

I_r = Read Current Pulse which is the value of current used to switch the core from the ONE state to the ZERO state.

I_{pw} = Partial Write Current Pulse is the value of write current which magnetically disturbs the core in the ZERO state, but does not switch it to the ONE state. A core that has been subjected to one or more partial write pulses is defined as being in the disturbed ZERO state (dV_z).

I_{pr} = Partial Read Current Pulse is the value of read current which magnetically disturbs the core in the ONE state but does not switch it to the ZERO state. A core which has been subjected to one or more partial read pulses is defined as being in the disturbed ONE state (dV_1).

I_k = (knee) The value of I_{pw} (direct current mmf) required to reach the switching threshold of the non-recoverable flux, when applying an mmf in the direction to switch the remnant state.

$\frac{I_k}{I}$ = The disturb ratio is the knee current I_k divided by the full switching mmf (pulse current) used to switch the remnant state of the core.

t_o = Reference Time, designated as the time when the drive current pulse reaches 10% of I on the rise of the read pulse.

t_r = Rise Time of the drive current pulse from t_o to 90% of I.

t_w = Pulse Width, or the time the drive current pulse remains above the 90% level.

t_f = Fall Time of the drive current pulse from 90% to 10% of I.

t_p = Peaking Time. Time between t_o and peak output voltage for a ONE.

t_s = Switching Time. Time between t_o and the time where the output voltage has decreased to 10% of its peak value for a ONE.

uV_1 = Peak Output Voltage developed when a read current pulse I_r is applied to a core in the undisturbed ONE state.

dV_1 = Peak Output Voltage developed when a read current pulse I_r is applied to a core in the disturbed ONE state.

dV_z = Peak Output Voltage developed when a read current pulse is applied to a core in the disturbed ZERO state.

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FERRITE CORE SPECIFICATION

COINCIDENT CURRENT
MEMORY CORE

Type 54-100

The Type 54-100 COINCIDENT CURRENT MEMORY CORE is a 50 mil, fast switching, high drive, high output core intended for use without temperature compensation. The core may be operated over any 80° range from -40°C to +100°C. The switching time characteristics of the Type 54-100 allow for its use in memory systems with cycle times of 4 to 5 microseconds.

MECHANICAL SPECIFICATIONS:

Outside Diameter	0.050 ± 0.002 inch
Inside Diameter	0.030 ± 0.002 inch
Thickness	0.015 ± 0.002 inch

ELECTRICAL SPECIFICATIONS:

Typical Operating Conditions @ 25°C

Disturb Ratio:	0.65	0.60
Drive Pulse (I)	820/410	900/450 ma turns
Pulse Width (t_w)	1.5 μs	1.5 μs
Pulse Rise Time (t_r)	0.2 μs	0.2 μs
Pulse Fall Time (t_f)	0.2 μs	0.2 μs

Typical Output Signals @ 25°C

Amplitude ONE (uV_1)	75 mv	110 mv
Amplitude ZERO (dV_z)	9 mv	9 mv
Peaking Time (t_p)	0.43 μs	0.4 μs
Switching Time (t_s)	0.8 μs	0.76 μs

GENERAL:

Cores are delivered 100% tested to mechanical and electrical specifications or to statistical quality level of AQL 0.015 or 6.5 as defined by MIL-STD-105C, Inspection Level II. Cores are electrically tested as defined by the test specifications on the next page.

CORE TEST SPECIFICATION

COINCIDENT CURRENT
MEMORY CORE

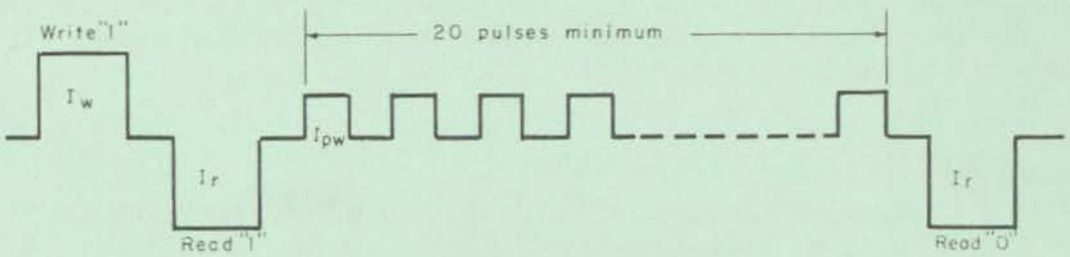
Type 54-100

ELECTRICAL TEST SPECIFICATIONS @ 25°± 1°C:

	Drive Pulse	t_w	t_r 10% to 90% linear	t_f	
I_r	900 ± 9.0 ma	2 μs	0.2 ± .02 μs	0.2 ± .02 μs	Over-shoot & droop ± 1%
I_w	900 ± 9.0 ma	2 μs	0.2 ± .02 μs	0.2 ± .02 μs	
$I_{pr}=I_{pw}$	540 ± 5.4 ma	2 μs	0.2 ± .02 μs	0.2 ± .02 μs	

Pulse Program

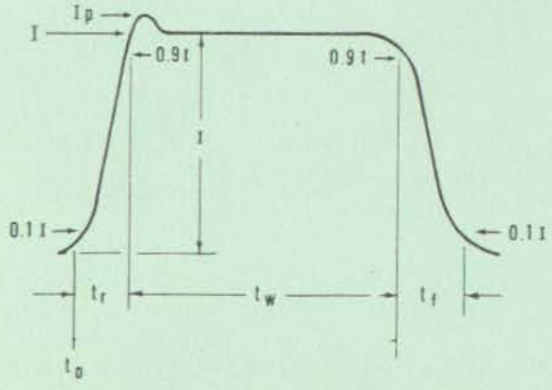
Pulse rate 20 kc.

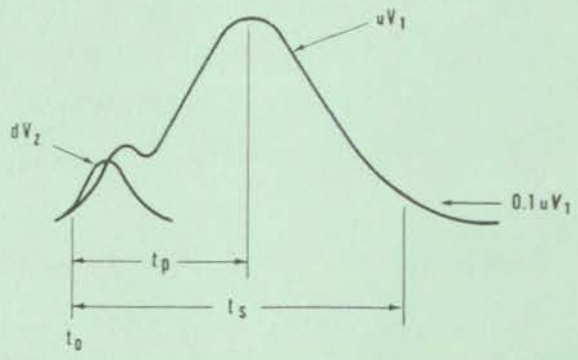


Output Test Signals:

uV_1	----------	95 mv min.
dV_z	----------	20 mv max.
t_p	----------	0.42 ± .04 μs
t_s	----------	0.9 μs max.

DEFINITIONS:





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Ferrite Core Specification

ISODRIVE CORE
Type 56-100

The ISODRIVE CORE is a fast switching, high drive, high output core intended for use in severe environments. The ISODRIVE CORE has a better disturb ratio over the temperature range of -55°C to +100°C than conventional cores have at 25°C. Current compensation of the drive system is not necessary.

MECHANICAL SPECIFICATIONS:

Outside Diameter	0.050 ± 0.002 inch
Inside Diameter	0.030 ± 0.002 inch
Thickness	0.015 ± 0.002 inch
Die Fins	0.001 max

ELECTRICAL SPECIFICATIONS:

Recommended Operating Conditions

Temperature Range	-55°C to +100°C
Drive Pulse	1000/500 ma turns
Pulse width (t_w)	2 μs
Pulse rise time (t_r)	0.2 ± 0.02 μsec linear
Pulse fall time (t_f)	0.3 μsec min

Typical Output Signals

Temperature:	-50°C	+25°C	+100°C
Switching time (t_s)	0.90 μs	0.80 μs	0.70 μs
Peaking time (t_p)	0.42 μs	0.36 μs	0.30 μs
Amplitude ONE (uV_1)	85 mv	117 mv	175 mv
Amplitude ZERO (dV_z)	14 mv	14 mv	16 mv

GENERAL:

Cores are delivered 100% tested to mechanical and electrical specifications or to statistical quality level of AQL 0.015 or 6.5 as defined by MIL-STD-105B, Inspection Level II. Cores are electrically tested as defined by the Test Specifications on the next page.

ELECTRONIC MEMORIES, INC.
Core Test Specification

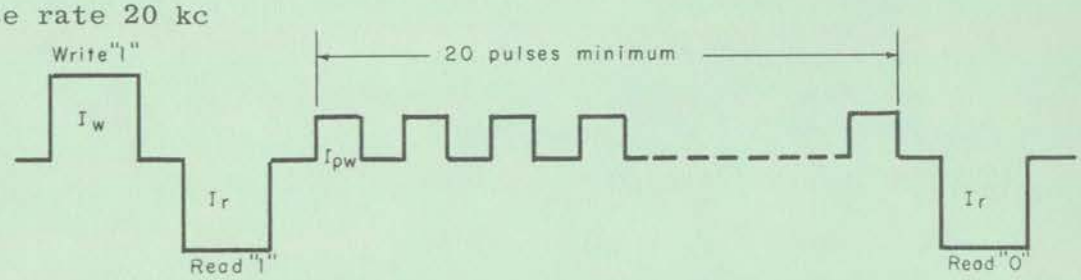
ISODRIVE CORE
Type 56-100

ELECTRICAL TEST SPECIFICATIONS AT 25°C ± 2°C:

Drive Pulse		t_w	t_r 10% to 90% linear	t_f	
I_r	1000 ma ±2 ma	10 µs	0.2 ±.01 µsec	0.2 ±.01 µsec	Over-shoot and droop ±1%
I_w	1000 ma ±2 ma	10 µs	0.2 ±.01 µsec	0.2 ±.01 µsec	
$I_{pr}=I_{pw}$	700 ma ±1 ma	10 µs	0.2 ±.01 µsec	0.2 ±.01 µsec	

Pulse Program

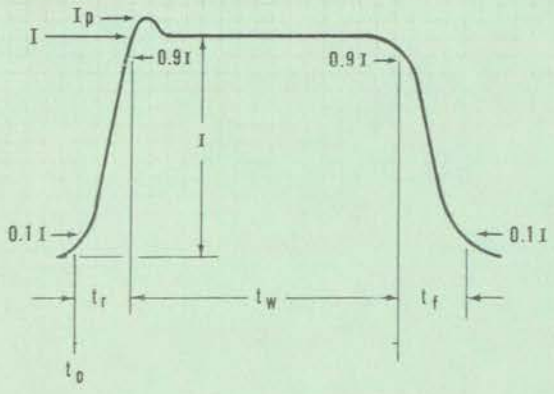
Pulse rate 20 kc

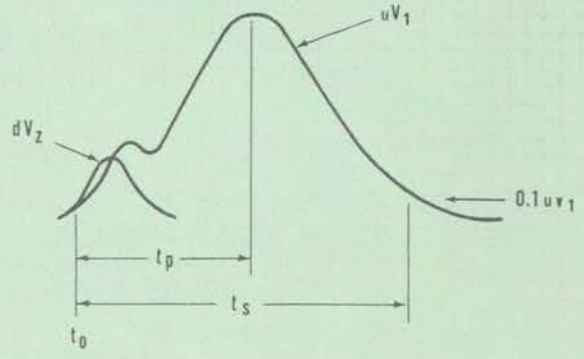


Output Test Signals

uV_1 -------- 90 mv min.
dV_z -------- 25 mv max.
t_p -------- 0.4 µsec ± .05 µsec
t_s -------- 0.9 µsec max

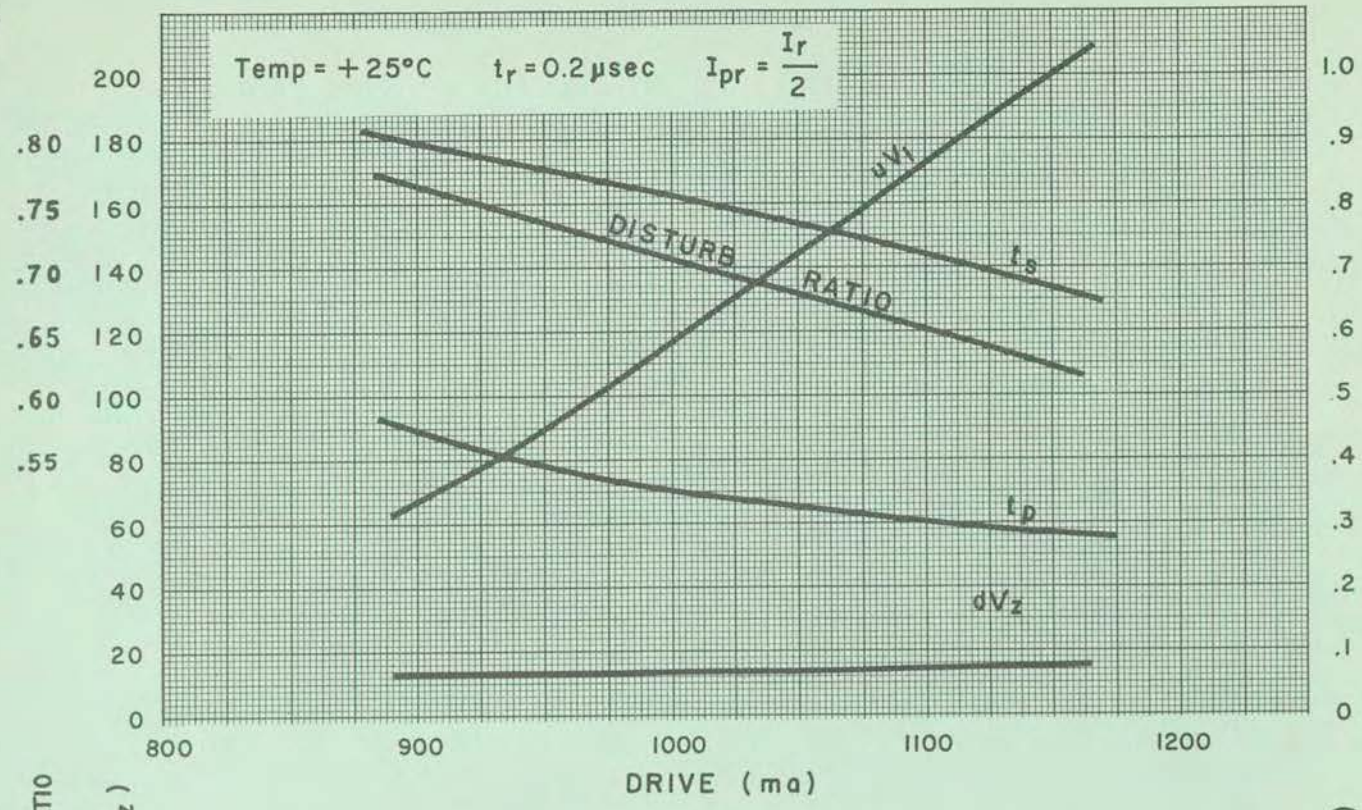
DEFINITIONS:





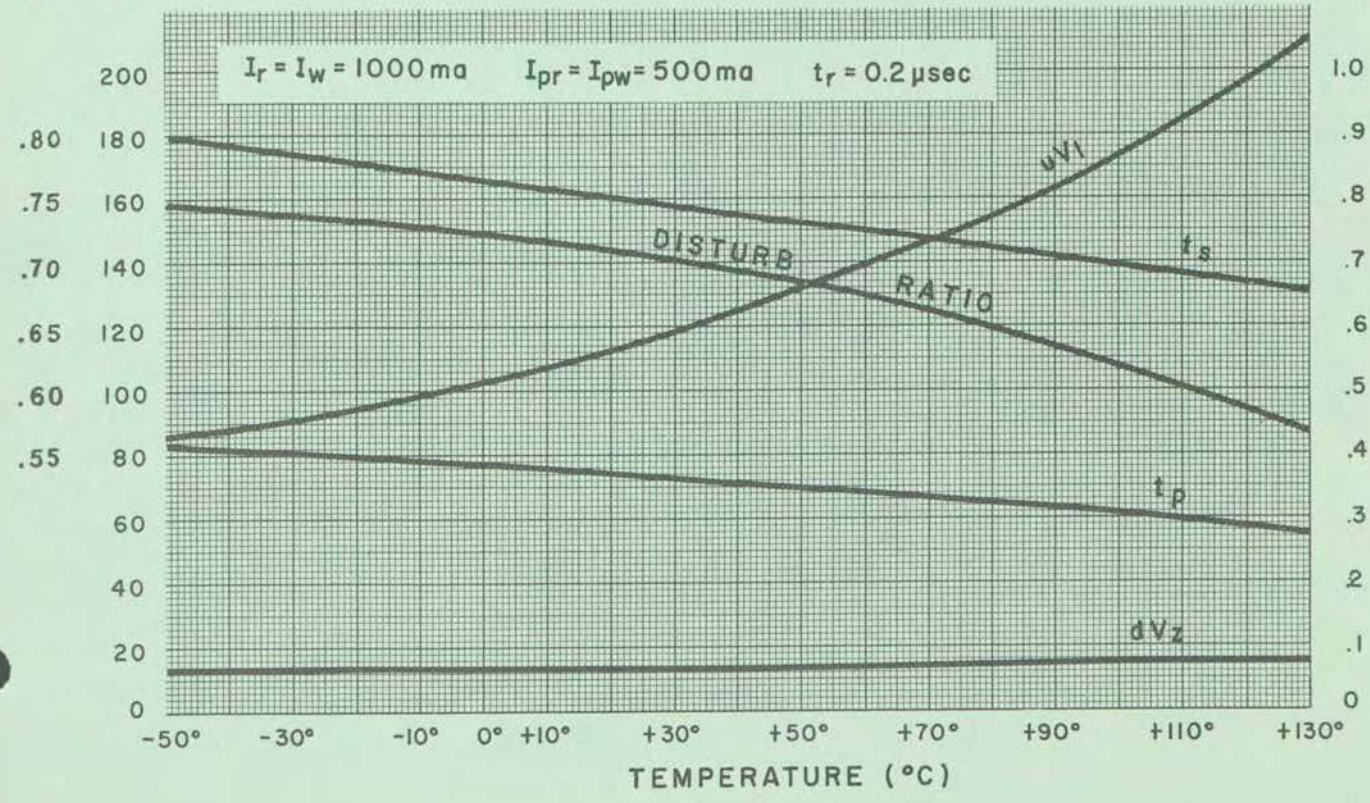
56-100 CORE PARAMETERS VS DRIVE

(Constant Temperature)



56-100 CORE PARAMETERS VS TEMPERATURE

(Constant Drive)



Core Test Specification

ISODRIVE CORE
Type 56-100

DEFINITIONS:

I = Drive Current Amplitude. Value of the flat top portion of current used to switch core.

I_p = Peak Amplitude Current Pulse. Overshoot value of drive current.

I_w = Write Current Pulse which is the value of current used to switch the core from the ZERO to ONE state.

I_r = Read Current Pulse which is the value of current used to switch the core from the ONE state to the ZERO state.

I_{pw} = Partial Write Current Pulse is the value of write current which magnetically disturbs the core in the ZERO state, but does not switch it to the ONE state. A core that has been subjected to one or more partial write pulses is defined as being in the disturbed ZERO state (dV_z).

I_{pr} = Partial Read Current Pulse is the value of read current which magnetically disturbs the core in the ONE state but does not switch it to the ZERO state. A core which has been subjected to one or more partial read pulses is defined as being in the disturbed ONE state (dV_1).

I_k = (knee) The value of I_{pw} (direct current mmf) required to reach the switching threshold of the non-recoverable flux, when applying an mmf in the direction to switch the remnant state.

$\frac{I_k}{I}$ = The disturb ratio is the knee current I_k divided by the full switching mmf (pulse current) used to switch the remnant state of the core.

t_o = Reference Time, designated as the time when the drive current pulse reaches 10% of I on the rise of the read pulse.

t_r = Rise Time of the drive current pulse from t_o to 90% of I.

t_w = Pulse Width, or the time the drive current pulse remains above the 90% level.

t_f = Fall Time of the drive current pulse from 90% to 10% of I.

t_p = Peaking Time. Time between t_o and peak output voltage for a ONE.

t_s = Switching Time. Time between t_o and the time where the output voltage has decreased to 10% of its peak value for a ONE.

uV_1 = Peak Output Voltage developed when a read current pulse I_r is applied to a core in the undisturbed ONE state.

dV_1 = Peak Output Voltage developed when a read current pulse I_r is applied to a core in the disturbed ONE state.

dV_z = Peak Output Voltage developed when a read current pulse is applied to a core in the disturbed ZERO state.

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FERRITE CORE SPECIFICATION

LOW FLUX CORE
Type 58-100

The LOW FLUX CORE is a medium drive, very fast switching core intended for use in coincident current memories in the 2 to 3 microsecond speed class. The core has excellent signal-to-noise properties when driven with a current pulse having a fast rise time. The LOW FLUX CORE exhibits excellent characteristics over a temperature range of -10°C to +55°C which allow for reasonable current compensation.

MECHANICAL SPECIFICATIONS:

Outside Diameter	0.050 ± 0.002 inch
Inside Diameter	0.030 ± 0.002 inch
Thickness	0.015 ± 0.002 inch
Die Fins	0.001 max

ELECTRICAL SPECIFICATIONS:

Typical Operating Conditions

Temperature	25°C
Drive Pulse (I)	750/375 ma turns
Pulse width (t_w)	1 μs
Pulse rise time (t_r)	0.1 ± 0.01 μsec linear
Pulse fall time (t_f)	0.2 μs

Typical Output Signals

Temperature	25°C
Switching time (t_s)	0.50 μs
Peaking time (t_p)	0.22 μs
Amplitude ONE (uV_1)	83 mv
Amplitude ZERO (dV_z)	10.5 mv

GENERAL:

Cores are delivered 100% tested to mechanical and electrical specifications or to statistical quality level of AQL 0.015 or 6.5 as defined by MIL-STD-105B, Inspection Level II. Cores are electrically tested as defined by the Test Specifications on the next page.

CORE TEST SPECIFICATION

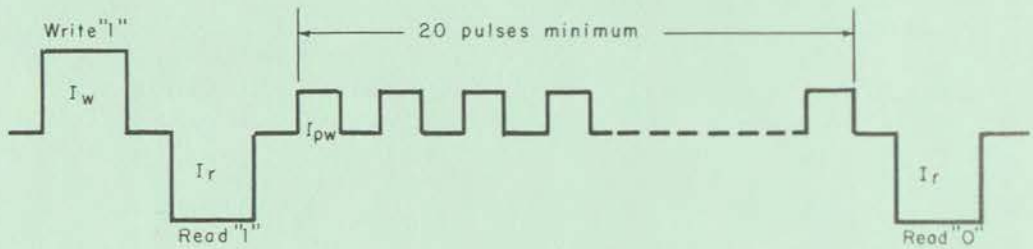
LOW FLUX CORE
Type 58-100

ELECTRICAL TEST SPECIFICATIONS AT 25°C ± 2°C:

	Drive Pulse	t_w	t_r 10% to 90% linear	t_f	
I_r	675 ± 6.75 ma	2 μs	0.1 ± .01 μsec	0.1 ± .01 μsec	Over-shoot and droop ±1%
I_w	675 ± 6.75 ma	2 μs	0.1 ± .01 μsec	0.1 ± .01 μsec	
$I_{pr}=I_{pw}$	405 ± 4.05 ma	2 μs	0.1 ± .01 μsec	0.1 ± .01 μsec	

Pulse Program

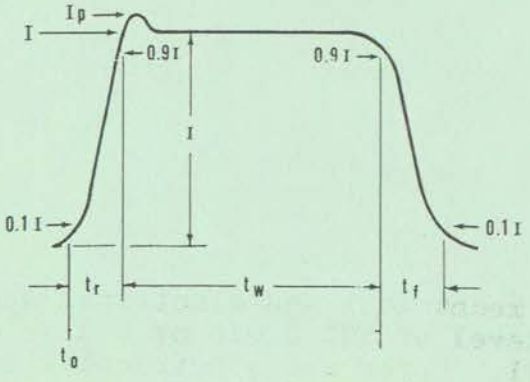
Pulse rate 20 kc

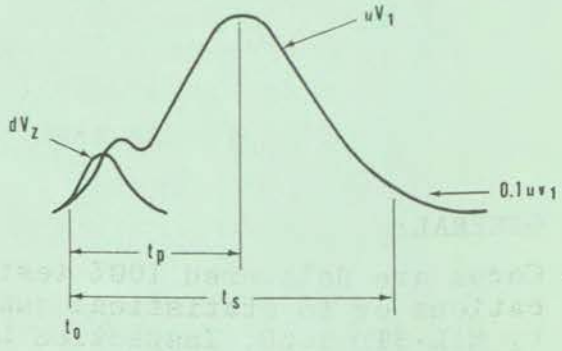


Output Test Signals

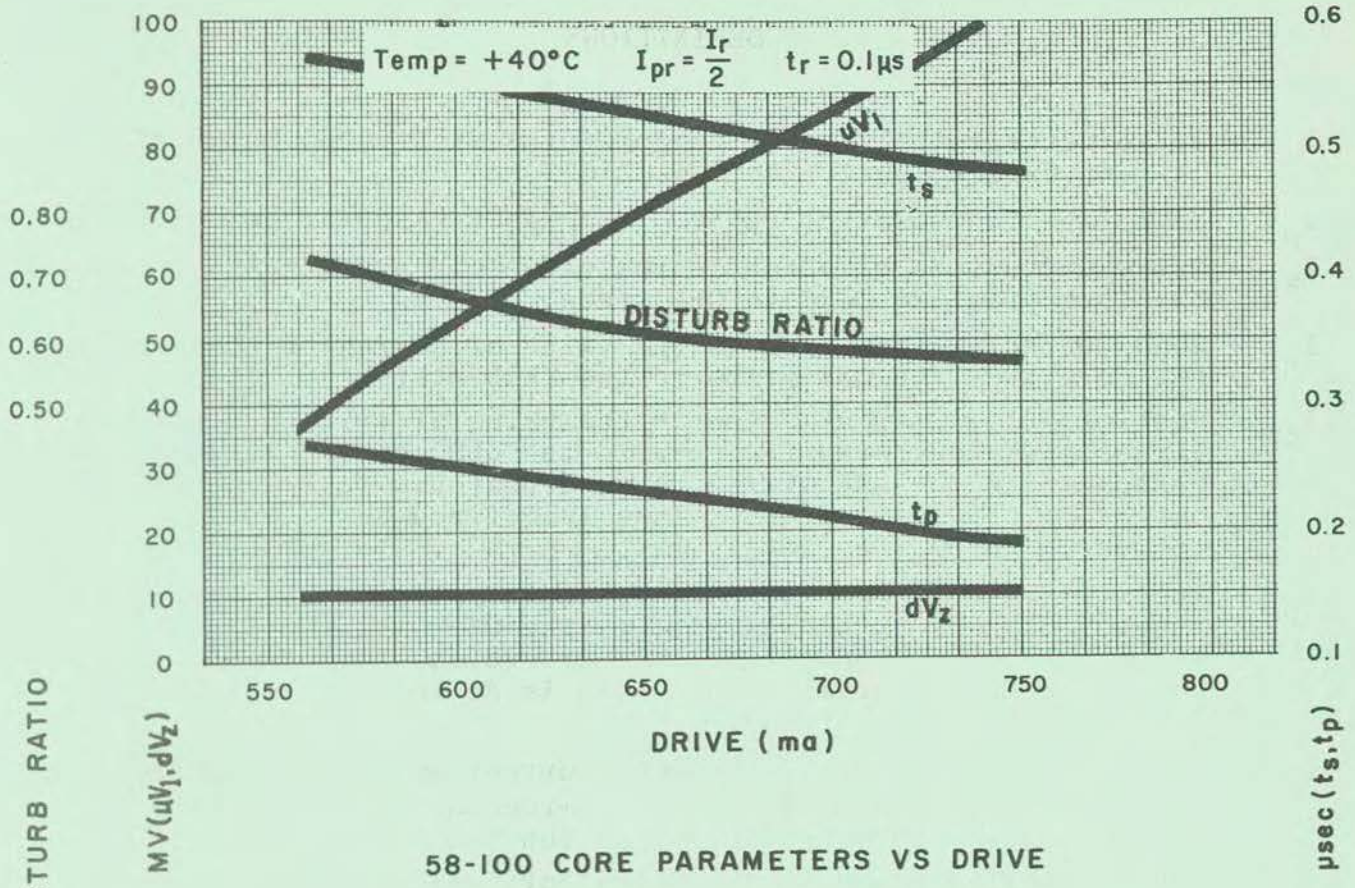
uV_1	---------	54 mv min.
dV_z	---------	14 mv max.
t_p	---------	0.25 ± .02 μs
t_s	---------	0.56 μs max.

DEFINITIONS:

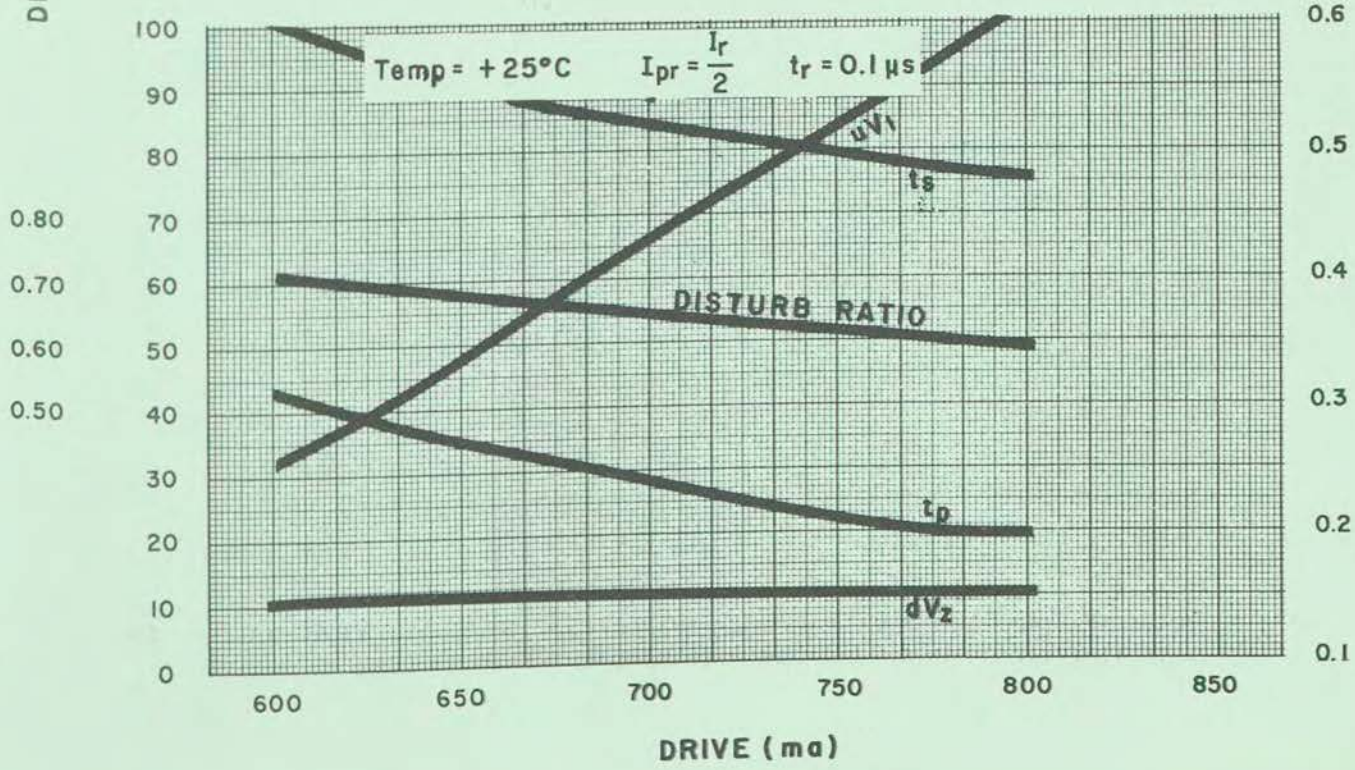




58-100 CORE PARAMETERS VS DRIVE



58-100 CORE PARAMETERS VS DRIVE



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DEFINITIONS

I = Drive Current Amplitude. Value of the flat top portion of current used to switch core.

I_p = Peak Amplitude Current Pulse. Overshoot value of drive current.

I_w = Write Current Pulse which is the value of current used to switch the core from the ZERO to ONE state.

I_r = Read Current Pulse which is the value of current used to switch the core from the ONE state to the ZERO state.

I_{pw} = Partial Write Current Pulse is the value of write current which magnetically disturbs the core in the ZERO state, but does not switch it to the ONE state. A core that has been subjected to one or more partial write pulses is defined as being in the disturbed ZERO state (dV_z).

I_{pr} = Partial Read Current Pulse is the value of read current which magnetically disturbs the core in the ONE state but does not switch it to the ZERO state. A core which has been subjected to one or more partial read pulses is defined as being in the disturbed ONE state (dV_1).

I_k = (knee) The value of I_{pw} (direct current mmf) required to reach the switching threshold of the non-recoverable flux, when applying an mmf in the direction to switch the remnant state.

$\frac{I_k}{I}$ = The disturb ratio is the knee current I_k divided by the full switching mmf (pulse current) used to switch the remnant state of the core.

t_o = Reference Time, designated as the time when the drive current pulse reaches 10% of I on the rise of the read pulse.

t_r = Rise Time of the drive current pulse from t_o to 90% of I.

t_w = Pulse Width, or the time the drive current pulse remains above the 90% level.

t_f = Fall Time of the drive current pulse from 90% to 10% of I.

t_p = Peaking Time. Time between t_o and peak output voltage for a ONE.

t_s = Switching Time. Time between t_o and the time where the output voltage has decreased to 10% of its peak value for a ONE.

uV_1 = Peak Output Voltage developed when a read current pulse I_r is applied to a core in the undisturbed ONE state.

dV_1 = Peak Output Voltage developed when a read current pulse I_r is applied to a core in the disturbed ONE state.

dV_z = Peak Output Voltage developed when a read current pulse is applied to a core in the disturbed ZERO state.

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FERRITE CORE SPECIFICATION

SWITCH CORE
Type 101-101

The Type 101-101 SWITCH CORE is a small switch core with good temperature characteristics designed for use in switching and current steering applications.

MECHANICAL SPECIFICATIONS:

Outside Diameter	0.100 ± 0.005 inch
Inside Diameter	0.070 ± 0.005 inch
Thickness	0.035 ± 0.005 inch

ELECTRICAL SPECIFICATIONS:

Temperature 25°C ± 2°C

Saturation Flux (B_s)	2380 gauss
Remanent Flux (B_r)	2140 gauss
Coercive Force (H_c)	0.58 oersted
Curie Temperature (T_c)	220°C

B_r/B_s ratio equals 0.95

Note: B_s, B_r, H_c determined by pulse method. t_r = 0.1 μs, t_w = 10 μs. B_s is technical saturation. (H max = 10 H_c)

GENERAL:

Cores are delivered 100% tested to mechanical and electrical specifications or to statistical quality level of AQL 0.015 or 6.5 as defined by MIL-STD-105C, Inspection Level II. Cores are electrically tested as defined by the Test Specifications on the next page.

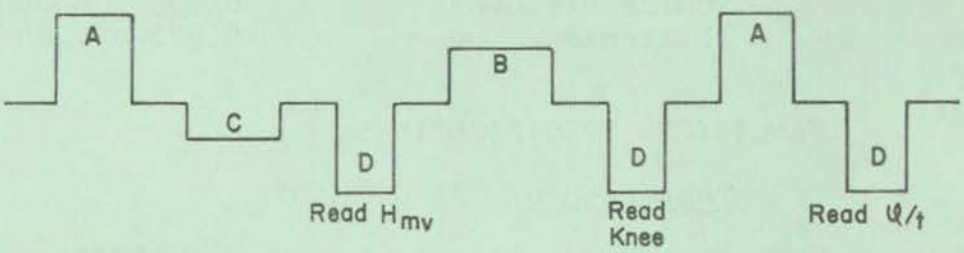
CORE TEST SPECIFICATION

SWITCH CORE
Type 101-101

ELECTRICAL SPECIFICATIONS AT 25°C ± 2°C:

	Drive Pulse	t_w	t_r 10% to 90% linear	t_f	
A	I_{reset} 2.4 ± .12 amps	10 μs	0.5 ± .05 μs	1.0 ± .1 μs	Over-shoot and droop ±2%
B	I_{knee} .250 ± .012 amps	100 μs	1.0 ± .1 μs	1.0 ± .1 μs	
C	I_{set} .300 ± .015 amps	100 μs	1.0 ± .1 μμs	1.0 ± .1 μs	
D	I_{read} 1.0 ± .05 amps	10 μs	0.5 ± .05 μs	1.0 ± .1 μs	

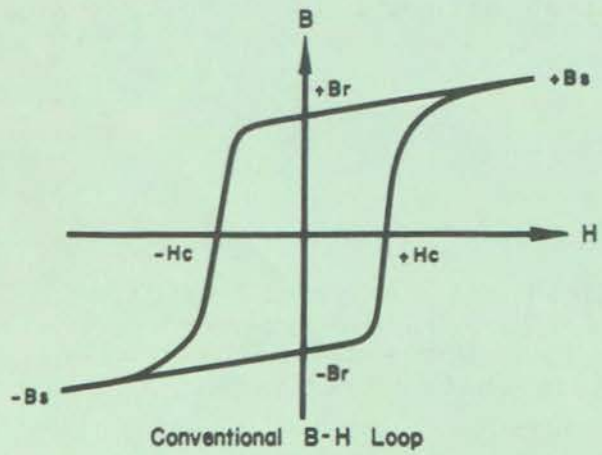
Pulse Program
Pulse rate 2 kc



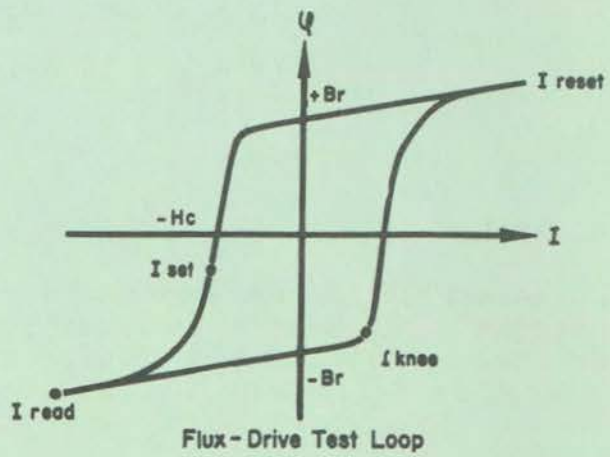
Output Test Signals: Output signals are read with an integrator with a time constant of 12 μs ± 1% (1/e value).

Read H_{mv}	5 mv min. 8 mv max.
Read Knee	2 mv max.
Read φ/t	12.7 mv ± .5 mv

DEFINITIONS:



Conventional B-H Loop

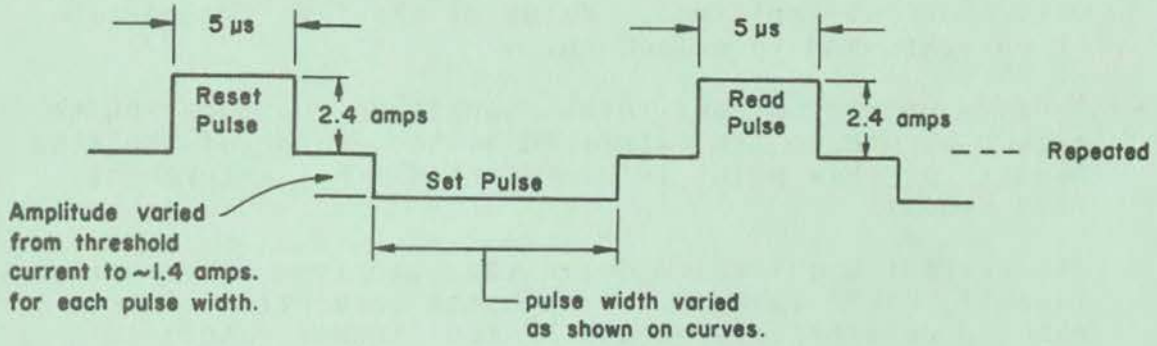


Flux-Drive Test Loop

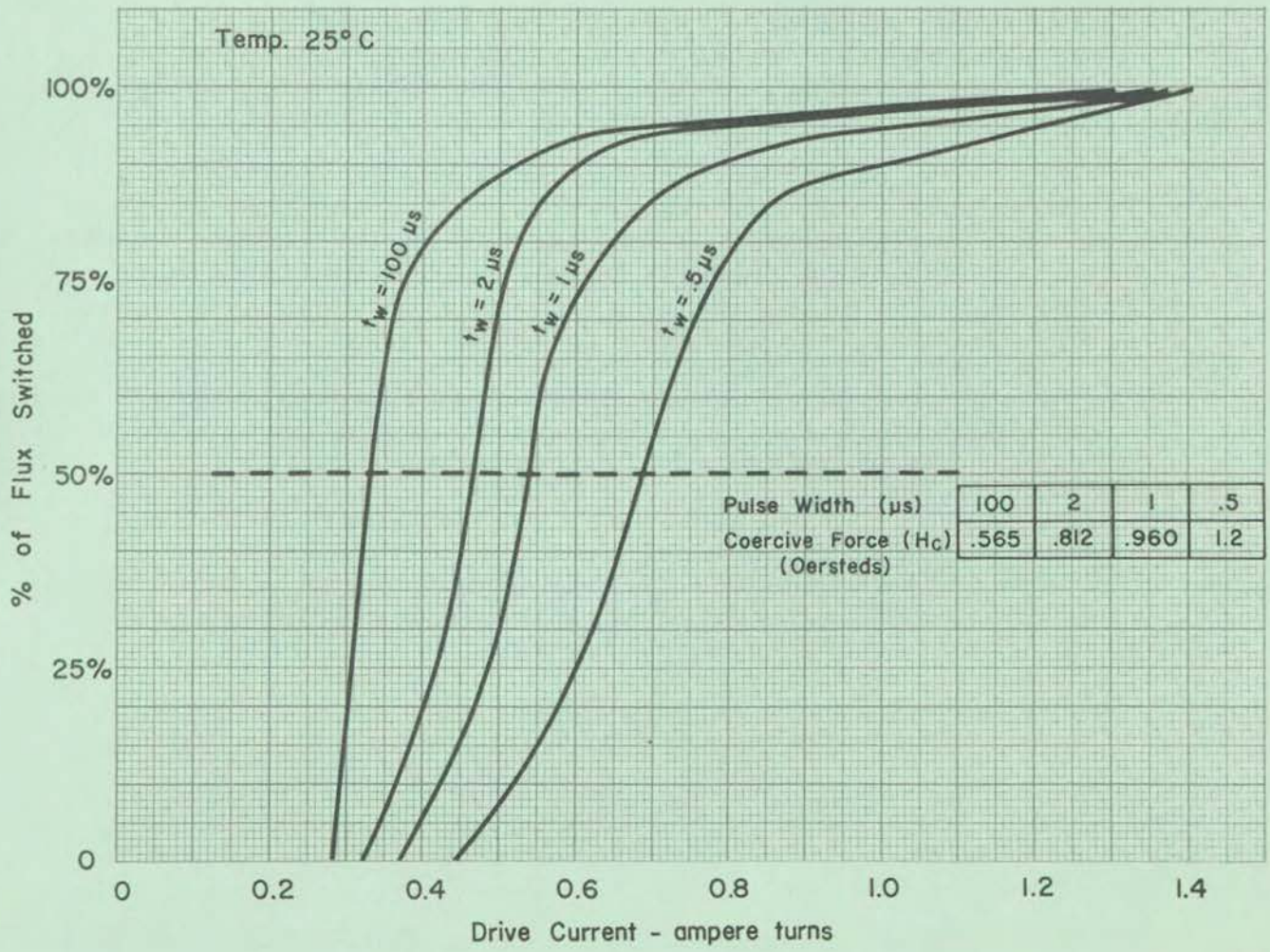
101-101 SWITCH CORE CHARACTERISTICS

FLUX TRANSFER AS A FUNCTION OF PULSE WIDTH SET CURRENT

Pulse Program: Pulse rate 2 kc.



Output signals are read with an integrator with a time constant of 12 µs ± 1% (1/e value).



Pulse Width (µs)	100	2	1	.5
Coercive Force (H_C) (Oersteds)	.565	.812	.960	1.2

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SWITCH CORE DEFINITIONS

I = Drive Current Amplitude. Value of the flat top portion of current used to switch core.

I_{reset} = A drive current of sufficient amplitude and duration to switch a core to its saturated state. Value of the flux density at this point is represented $\pm B_S$, saturation flux density.

I_{set} = The current required to drive the core from a remanent magnetic state towards the opposite saturation state, placing an arbitrary amount of flux (unsaturated) in the core.

I_{knee} = A current pulse of defined width having sufficient amplitude to cause the core to reach the switching threshold of the non-recoverable flux.

I_{read} = A current pulse of sufficient amplitude and duration to saturate the switch core in the direction opposite the reset current. This current is applied following a set current, knee current, or a reset current.

H_{mv} = The output of the switch core measured in millivolts at the output of an integrator with a time constant of 12 μs ± 1% (1/e value) when I_{read} current is applied to the core in the direction opposite the I_{reset} current. This is defined as a stable point in the high permeability region of switching, and is close to the H_c point.

H_c = The coercive force is the drive of defined pulse width necessary to bring the flux density of the core to zero (i.e.) 50% of saturation flux density.

$\varphi/_t$ = The flux output of the switch core measured in millivolts at the output of an integrator with a time constant of 12 μs ± 1% (1/e value) when I_{read} current is applied to a core in one saturated magnetic state driving it into the other saturated magnetic state.

t_o = Reference Time, designated as the time when the drive current pulse reaches 10% of I on the rise.

t_r = Rise Time of the drive current pulse from t_o to 90% of I.

t_w = Pulse Width, or the time the drive current pulse remains above the 90% level.

t_f = Fall Time of the drive current pulse from 90% to 10% of I.

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APPLICATION BULLETIN

NOV 26 63

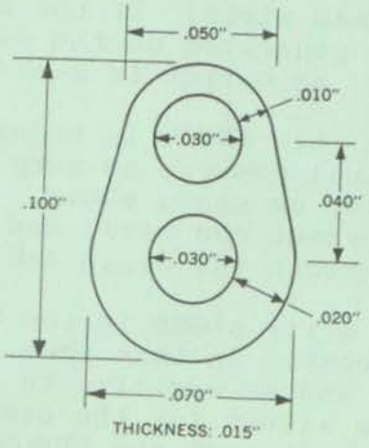
TYPE 101-1002
TRANSFLUXOR

The TYPE 101-1002 TRANSFLUXOR is a non-destructive readout (NDRO) device with switching characteristics that permit its use in arrays with coincident-current selection.

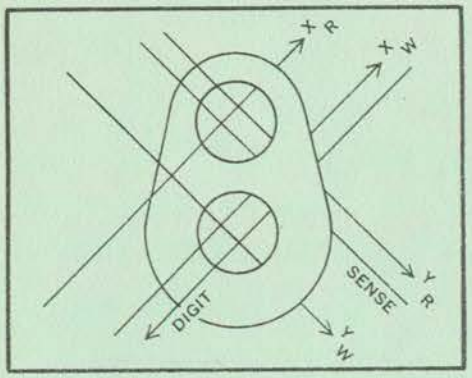
It is designed with two apertures of equal diameter, so placed that the cross-sectional area of ferrite material surrounding one aperture is approximately half that surrounding the other. This "shmoo"-shaped design results in improved switching properties when compared to the round or rectangular transfluxor.

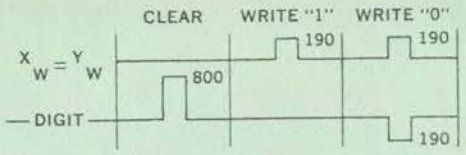
Because the 101-1002 has symmetry about a single axis, it can be positioned easily for array assembly, by manual or mechanical means.

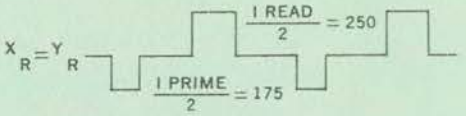
MECHANICAL SPECIFICATIONS



TYPICAL USE IN A MEMORY SYSTEM







TYPICAL OUTPUTS WHEN DRIVEN AT 25°C

	uv (mv)	tp (μs)	ts (μs)	dvz (mv)
READ	79	.37	.59	20.

THEORY OF OPERATION

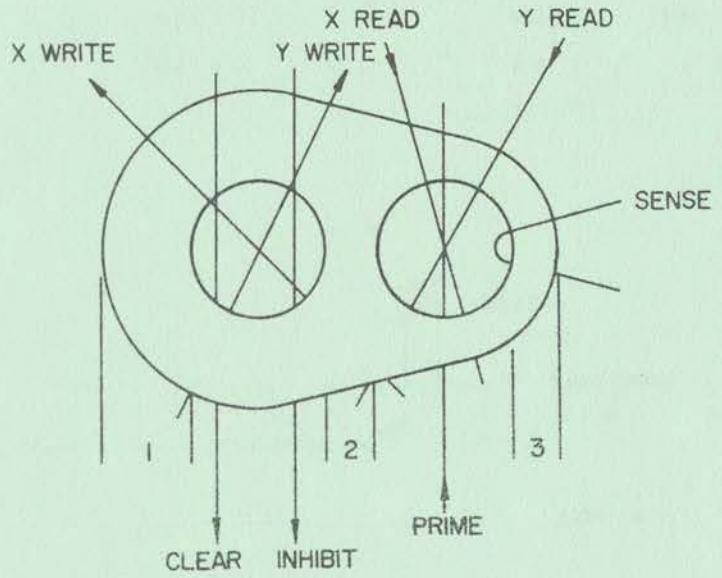
Figure I shows the SHMOO transfluxor and input signals required for operation. The information state (write) of the SHMOO is controlled by wires through the left aperture. A positive 2 μs pulse of 800 mA or greater through the clear wire sets the SHMOO to the ZERO state. Flux through the entire device is set in the clockwise (in the figure) direction. Legs 2 and 3, bounding the right aperture, have flux in the same direction (ZERO state).

To write a ONE, the X and Y write lines both carry a 2 μs pulse of 190 mA in the negative direction. To write a ZERO, the pulse on the clear line is repeated, followed by simultaneous 2 μs pulses of 190 mA in the negative direction on the X and Y write lines, and 190 mA in the positive direction on the inhibit wire.

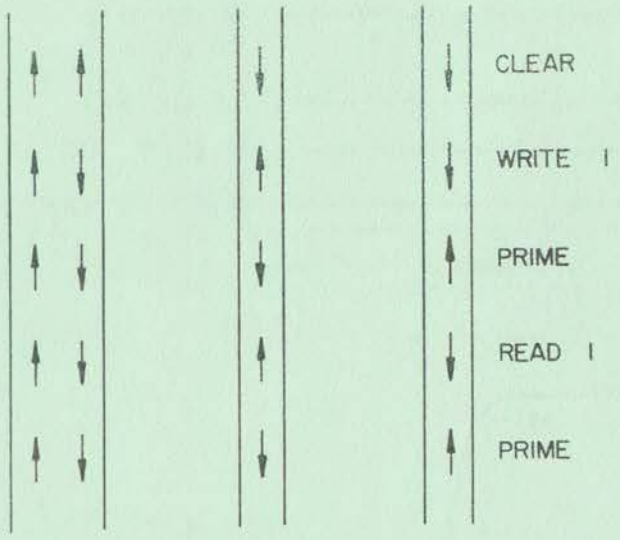
To read the SHMOO, it is first primed by a 350 mA pulse on the prime wire. The SHMOO is then read by simultaneous pulses of 250 mA on the X and Y read wires. If the device contained a ONE, an output pulse is generated on the sense wire. If the device contained a ZERO, no output is generated.

In the diagram opposite, the SHMOO is shown with 4 wires through each hole. In a practical memory, no more than 3 wires are required through each hole, as shown above. The inhibit and clear currents can both go through one wire, and the prime and read currents can both go through the X_{read} and Y_{read}.

It is also possible to write a ONE in the SHMOO by a combination of prime and digit current. In this case the digit current is in the negative direction and is additive to the prime current rather than subtractive. This allows for the design of a non-destructive system with only 4 wires through the SHMOO: Clear/Digit, X_{read}, Y_{read}, and Sense. This manner of operation is used at EMI for electrical test of the SHMOO.



FLUX PATTERN



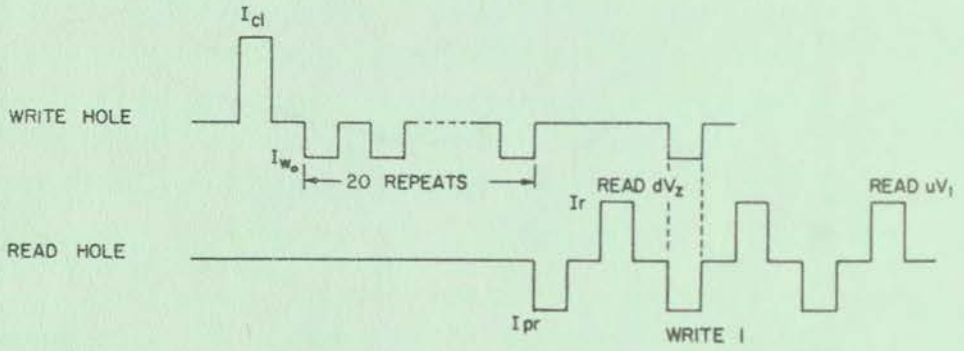
TEST SPECIFICATIONS

ELECTRICAL SPECIFICATIONS AT 25°C ± 1°C:

Drive Pulse		t_w	t_r 10% to 90% linear	t_f	
I_{cl}	700 ± 10 ma	2 μs	0.2 ± .02 μs	0.2 μs min.	
I_{w0}	240 ± 2.4 ma	5 μs	0.2 ± .02 μs	0.2 μs min.	Over-shoot & droop 1%
I_{pr}	325 ± 3.3 ma	5 μs	0.2 ± .02 μs	0.2 μs min.	
I_r	400 ± 4.0 ma	2 μs	0.2 ± .02 μs	0.2 μs min.	

Pulse Program

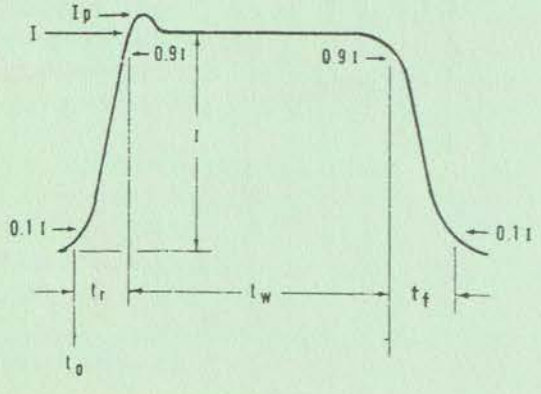
Pulse Rate 20 kc.

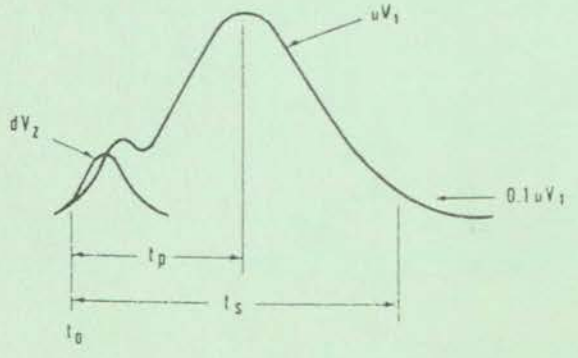


Output Test Signals:

uV_1	----------	50 mv min. 70 mv max.
dV_Z	----------	16 mv max.
t_p	----------	0.42 ± .05 μs
t_s	----------	0.85 μs max.

DEFINITIONS:



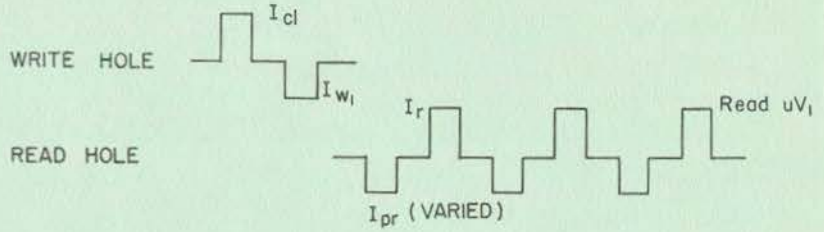


CHARACTERISTIC CURVES

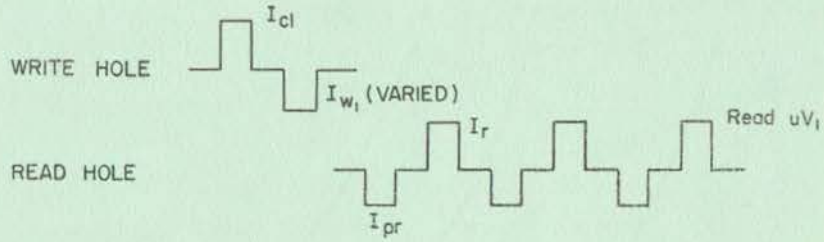
Programs Used in Generating Characteristic Curves

For all pulses, $t_w = 2.0\,\mu s$, $t_r = 0.2\,\mu s$

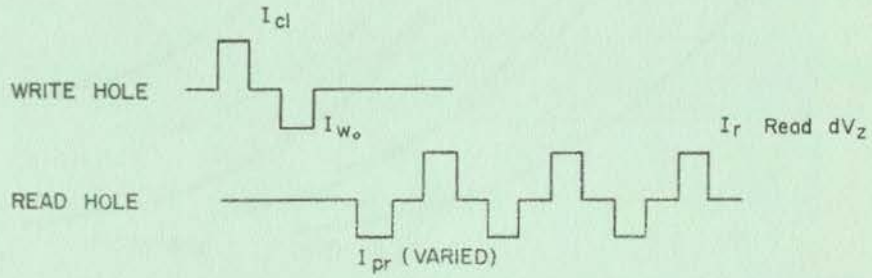
uV_1 vs I_{PRIME}



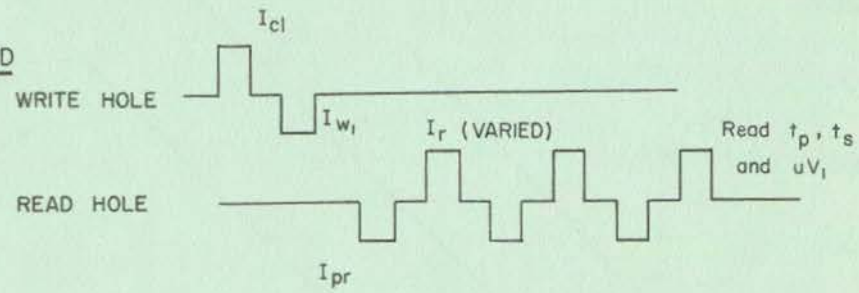
uV_1 vs I_{WRITE}



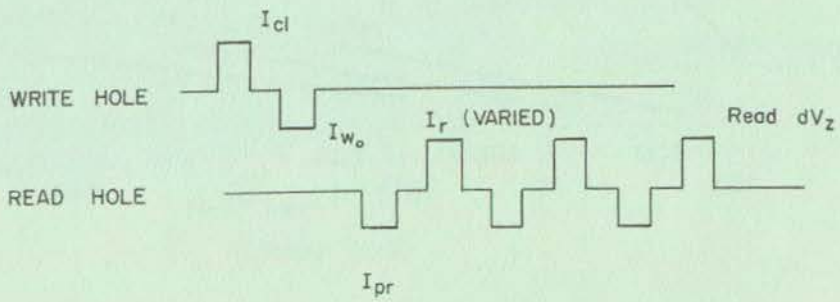
dV_Z vs I_{PRIME}



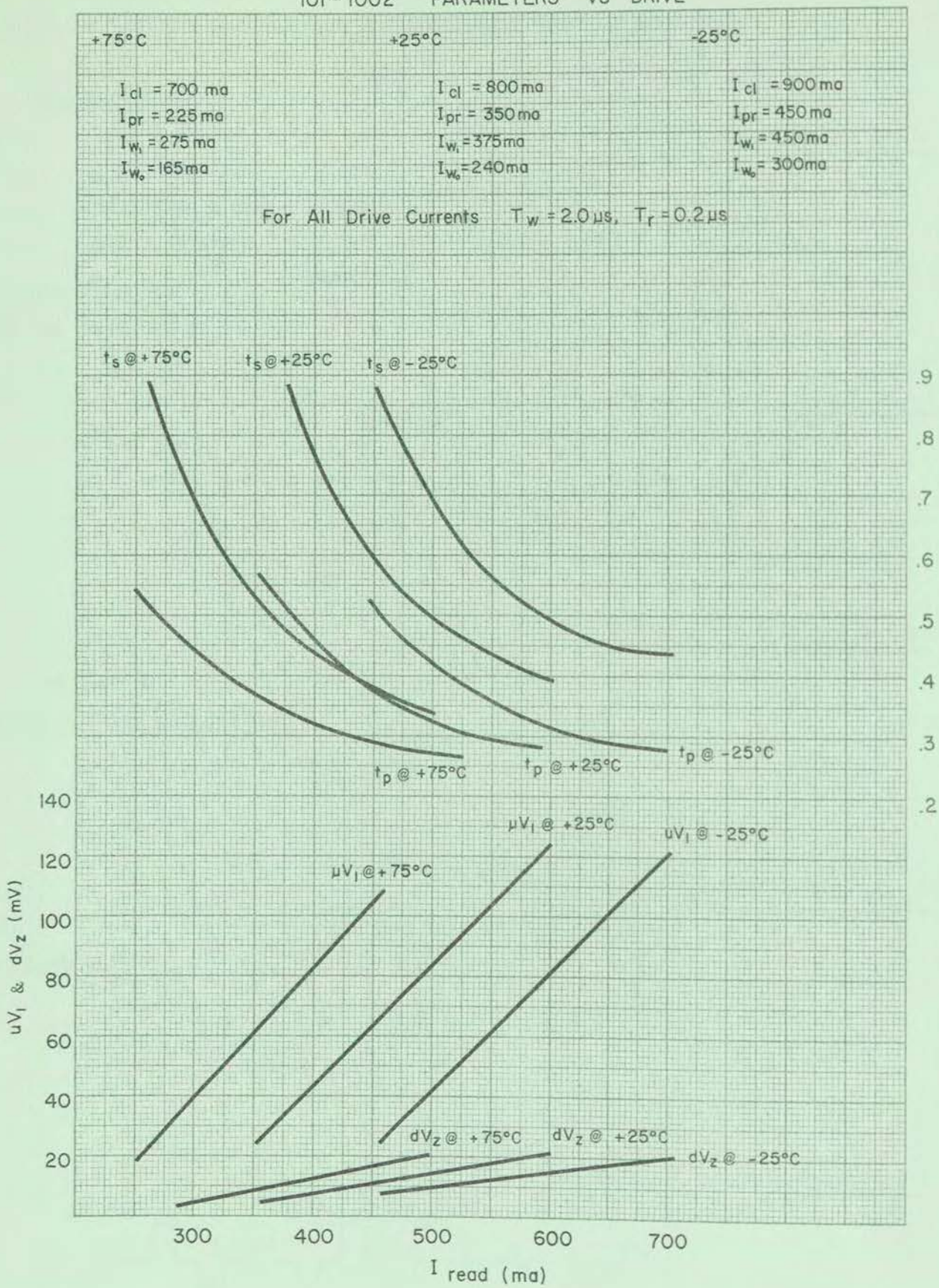
uV_1, t_p, and t_s vs I_{READ}



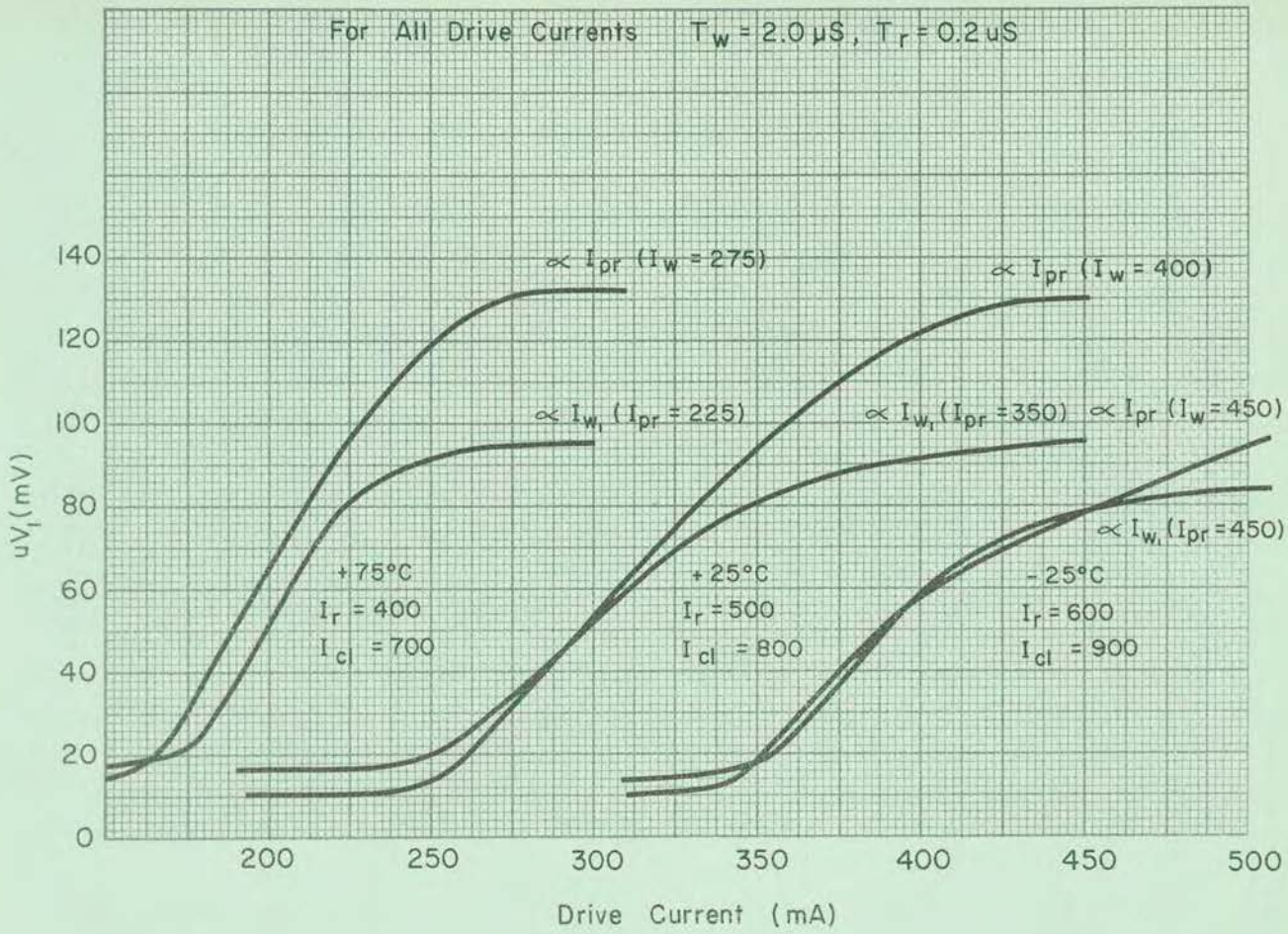
dV_Z vs I_{READ}

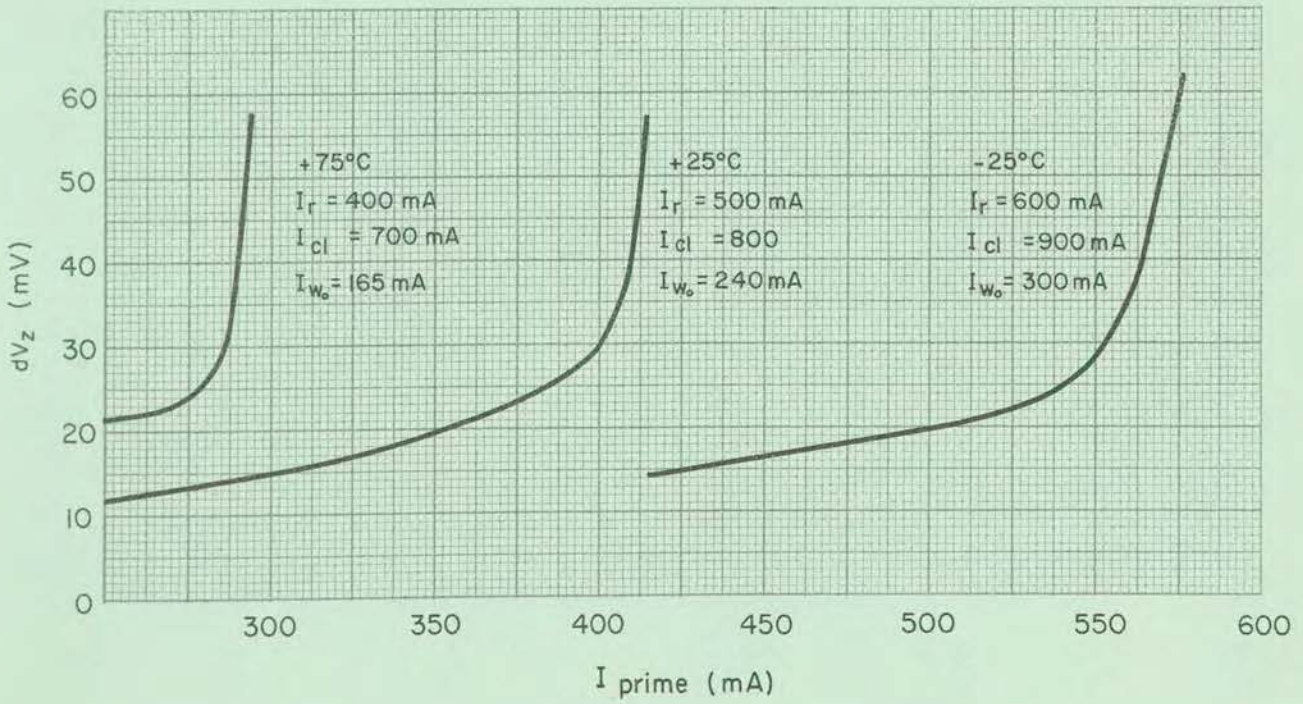


101 – 1002 PARAMETERS VS DRIVE



101 – 1002 PARAMETERS VS DRIVE





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TRANSFLUXOR DEFINITIONS

I = Drive Current Amplitude. Value of the flat top portion of current used to switch transfluxor.

I_p = Peak Amplitude Current Pulse. Overshoot value of drive current.

I_{cl} = Clear current which is the value of current used to switch transfluxor to the ZERO state.

I_{w1} = Current Pulse to write a ONE which is the value of current used to switch the transfluxor from the ZERO state to the ONE state.

I_{w0} = Current Pulse when writing a ZERO. This is the value of write current which magnetically disturbs the transfluxor in the ZERO state but does not switch it to the ONE state.

I_r = Read Current Pulse which is the value of current used to switch the transfluxor from the ONE state to the ZERO state.

I_{pr} = Prime Current which is the value of current used to set flux round the read hole in the prime direction ready for the next read current.

t_o = Reference Time, designated as the time when the drive current pulse reaches 10% of I on the rise of the read pulse.

t_r = Rise Time of the drive current pulse from t_o to 90% of I.

t_w = Pulse Width, or the time the drive current pulse remains above the 90% level.

t_f = Fall Time of the drive current pulse from 90% to 10% of I.

t_p = Peaking Time. Time between t_o and peak output voltage for a ONE.

t_s = Switching Time. Time between t_o and the time where the output voltage has decreased to 10% of its peak value for a ONE.

uV_1 = Peak Output Voltage developed when a read current pulse is applied to a transfluxor in the undisturbed ONE state.

uV_z = Peak Output Voltage developed when a read current pulse is applied to a transfluxor in the undisturbed ZERO state.

dV_z = Peak Output Voltage developed when a read current pulse is applied to a transfluxor in the disturbed ZERO state.

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FERRITE CORE SPECIFICATION

SWITCH CORE

Type 141-101

The Type 141-101 SWITCH CORE is a medium size switch core with good temperature characteristics designed for use in switching and current steering applications.

MECHANICAL SPECIFICATIONS:

Outside Diameter	0.140 ± 0.005 inch
Inside Diameter	0.090 ± 0.005 inch
Thickness	0.090 ± 0.005 inch

ELECTRICAL SPECIFICATIONS:

Temperature: 25°C ± 2°C

Saturation Flux (B_s)	2380 gauss
Remanent Flux (B_r)	2140 gauss
Coercive Force (H_c)	0.35 oersted
Curie Temperature (T_c)	220°C

B_r/B_s ratio equals 0.95 or greater.

Note: B_s, B_r, H_c determined by pulse method. t_r = 0.1 μs, t_w = 10 μs. B_s is technical saturation. (H_{max} is 10 H_c)

GENERAL:

Cores are delivered 100% tested to mechanical and electrical specifications or to statistical quality level of AQL 0.015 or 6.5 as defined by MIL-STD-105C, Inspection Level II. Cores are electrically tested as defined by the Test Specifications on the next page.

CORE TEST SPECIFICATION

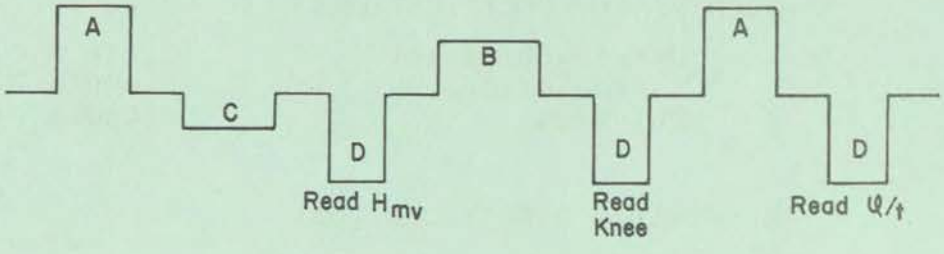
SWITCH CORE
Type 141-101

ELECTRICAL SPECIFICATIONS AT 25°C ± 2°C:

	Drive Pulse	t_w	t_r 10% to 90% linear	t_f	
A	I_{reset} 2.4 ± .12 amps	10 μs	0.5 ± .05 μs	1.0 ± .1 μs	Over-shoot and droop ± 2%
B	I_{knee} .240 ± .012 amps	100 μs	1.0 ± .1 μs	1.0 ± .1 μs	
C	I_{set} .290 ± .014 amps	100 μs	1.0 ± .1 μs	1.0 ± .1 μs	
D	I_{read} 1.25 ± .06 amps	10 μs	0.5 ± .05 μs	1.0 ± .1 μs	

Pulse Program

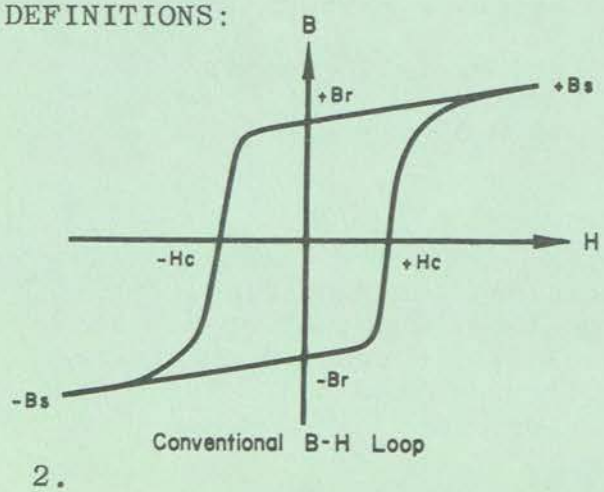
Pulse rate 2 kc



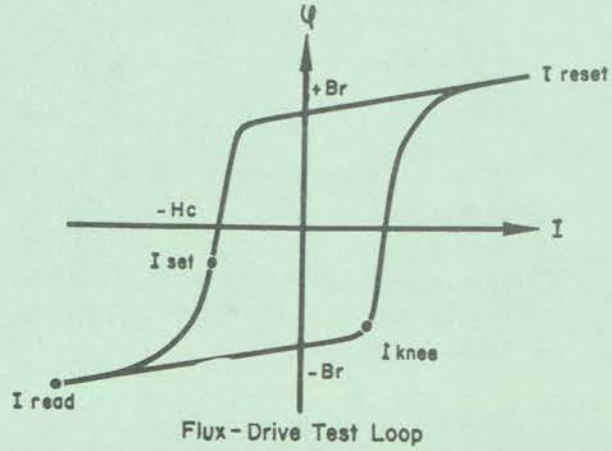
Output Test Signals: Output signals are read with an integrator with a time constant of 12 μs ± 1% (1/e value).

Read H_{mv}	----------	12 mv min. 18 mv max.
Read Knee	----------	5 mv max.
Read φ/t	----------	58 mv ± 1.5 mv

DEFINITIONS:



Conventional B-H Loop

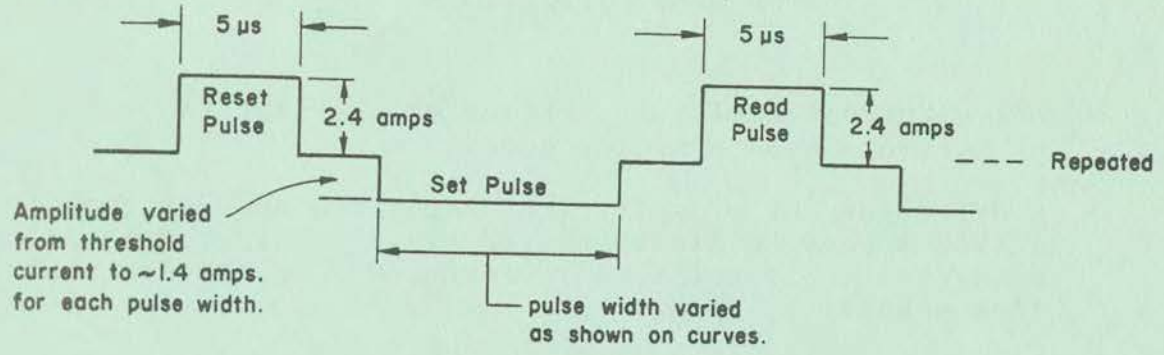


Flux-Drive Test Loop

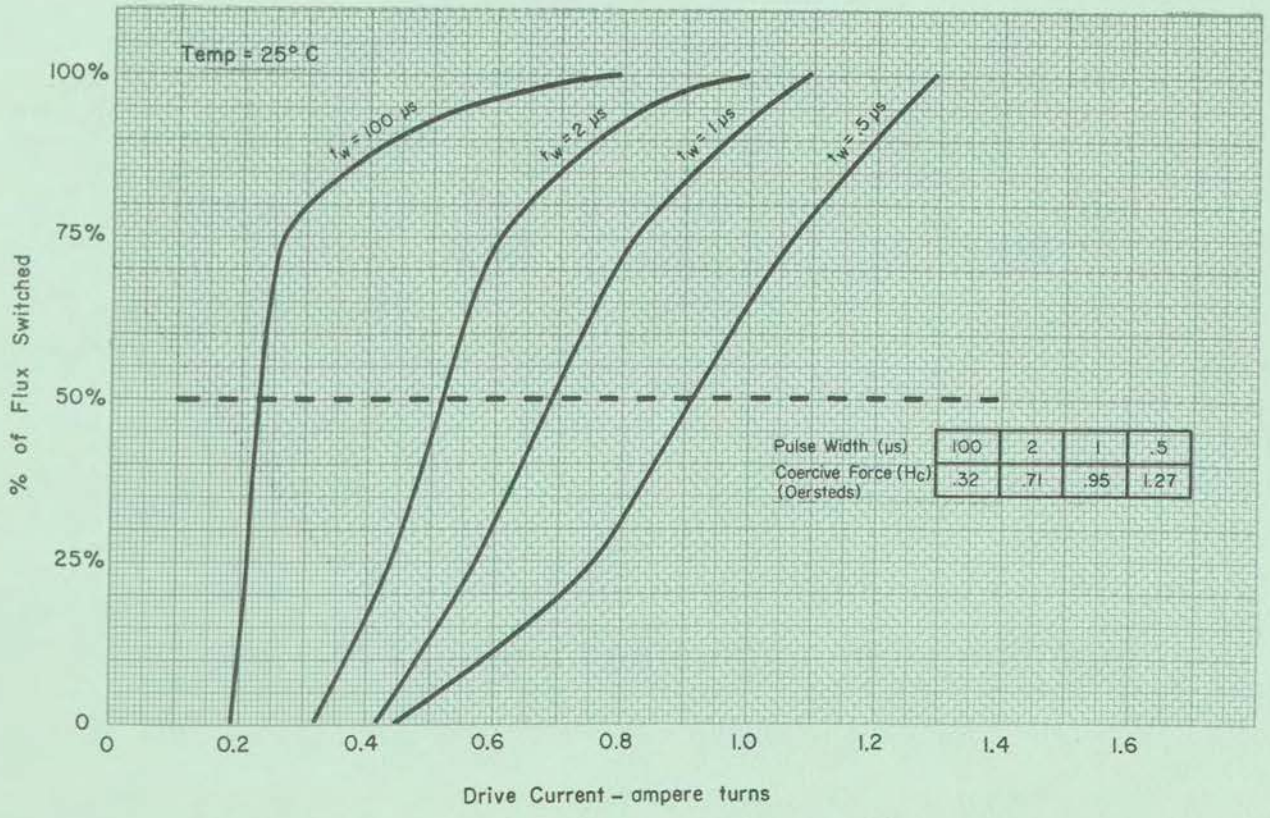
141-101 SWITCH CORE CHARACTERISTICS

FLUX TRANSFER AS A FUNCTION OF PULSE WIDTH SET CURRENT

Pulse Program: Pulse rate 2 kc.



Output signals are read with an integrator with a time constant of 12 µs ± 1% (1/e value).



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SWITCH CORE DEFINITIONS

I = Drive Current Amplitude. Value of the flat top portion of current used to switch core.

I_{reset} = A drive current of sufficient amplitude and duration to switch a core to its saturated state. Value of the flux density at this point is represented $\pm B_S$, saturation flux density.

I_{set} = The current required to drive the core from a remanent magnetic state towards the opposite saturation state, placing an arbitrary amount of flux (unsaturated) in the core.

I_{knee} = A current pulse of defined width having sufficient amplitude to cause the core to reach the switching threshold of the non-recoverable flux.

I_{read} = A current pulse of sufficient amplitude and duration to saturate the switch core in the direction opposite the reset current. This current is applied following a set current, knee current, or a reset current.

H_{mv} = The output of the switch core measured in millivolts at the output of an integrator with a time constant of 12 μs ± 1% (1/e value) when I_{read} current is applied to the core in the direction opposite the I_{reset} current. This is defined as a stable point in the high permeability region of switching, and is close to the H_c point.

H_c = The coercive force is the drive of defined pulse width necessary to bring the flux density of the core to zero. (i.e.) 50% of saturation flux density.

φ/t = The flux output of the switch core measured in millivolts at the output of an integrator with a time constant of 12 μs ± 1% (1/e value) when I_{read} current is applied to a core in one saturated magnetic state driving it into the other saturated magnetic state.

t_o = Reference Time, designated as the time when the drive current pulse reaches 10% of I on the rise.

t_r = Rise Time of the drive current pulse from t_o to 90% of I.

t_w = Pulse Width, or the time the drive current pulse remains above the 90% level.

t_f = Fall Time of the drive current pulse from 90% to 10% of I.

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FERRITE CORE SPECIFICATION

HI-MU TRANSFORMER CORE
Type 143-100

The Type 143-100 HI-MU TRANSFORMER CORE is a high mu core with excellent temperature characteristics designed expressly for transformer and blocking oscillator applications.

MECHANICAL SPECIFICATIONS:

Outside Diameter	0.140 ± 0.003 inch
Inside Diameter	0.090 ± 0.003 inch
Thickness	0.080 ± 0.003 inch

ELECTRICAL SPECIFICATIONS:

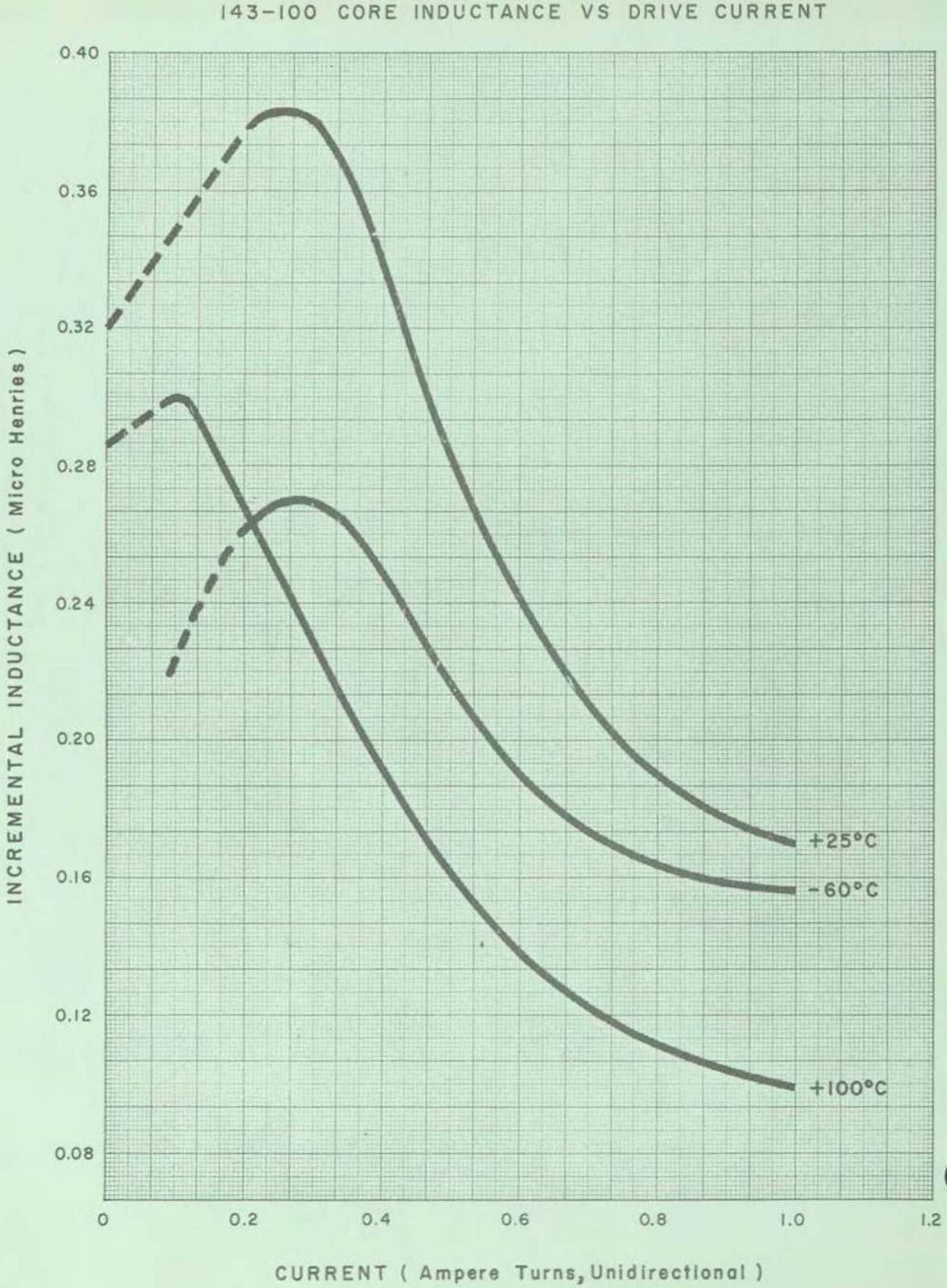
Temperature: 25°C ± 2°

Saturation Flux (B_s)	3600 gauss
Remanent Flux (B_r)	1800 gauss
Coercive Force (H_c)	0.7 oersted
Initial Permeability (μ_o)	1700
Curie Temperature (T_c)	175°C
Resistivity (Rho)	1 ohm-centimeter

Note: B_s, B_r, H_c determined by pulse method. t_r = 0.1 μs, t_w = 10 μs. B_s is technical saturation. (H max = 10 H_c) μ_o essentially constant 0°C to 100°C.

GENERAL:

Cores are delivered 100% tested to mechanical and electrical specifications or to statistical quality level of AQL 0.015 or 6.5 as defined by MIL-STD-105B, Inspection Level II.


143-100 CORE INDUCTANCE VS DRIVE CURRENT
INCREMENTAL INDUCTANCE (Micro Henries)
0.40
0.36
0.32
0.28
0.24
0.20
0.16
0.12
0.08
0
0.2
0.4
0.6
0.8
1.0
1.2
+25°C
-60°C
+100°C
CURRENT (Ampere Turns, Unidirectional)

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FERRITE CORE SPECIFICATION

SWITCH CORE

Type 181-101

The Type 181-101 SWITCH CORE is a large switch core with good temperature characteristics designed for use in switching and current steering applications.

MECHANICAL SPECIFICATIONS:

Outside Diameter	0.180 ± 0.005 inch
Inside Diameter	0.090 ± 0.005 inch
Thickness	0.090 ± 0.005 inch

ELECTRICAL SPECIFICATIONS:

Temperature: 25°C ± 2°C

Saturation Flux (B_S)	2380 gauss
Remanent Flux (B_r)	2140 gauss
Coercive Force (H_c)	0.35 oersted
Curie Temperature (T_c)	220°C

B_r/B_S ratio equals 0.95 or greater.

Note: B_S, B_r, H_C determined by pulse method. t_r = 0.1 μs, t_w = 10 μs. B_S is technical saturation. (H_{max} = 10 H_c)

GENERAL:

Cores are delivered 100% tested to mechanical and electrical specifications or to statistical quality level of AQL 0.015 or 6.5 as defined by MIL-STD-105C, Inspection Level II. Cores are electrically tested as defined by the Test Specifications on the next page.

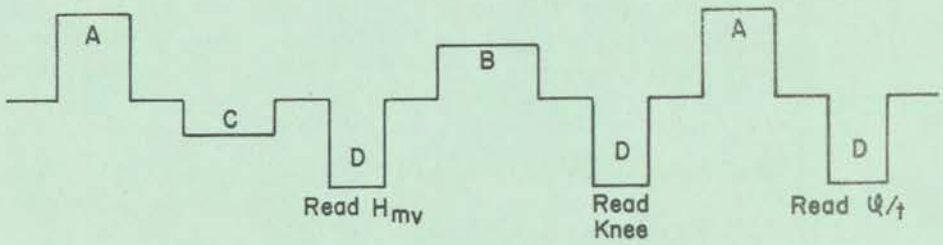
CORE TEST SPECIFICATION

SWITCH CORE
Type 181-101

ELECTRICAL SPECIFICATIONS AT 25°C ± 2°C:

	Drive Pulse		t_w	t_r 10% to 90% linear	t_f	
A	I_{reset}	2.4 ± .12 amps	10 μs	0.5 ± .05 μs	1.0 ± .1 μs	Over-shoot and droop ± 2%
B	I_{knee}	.250 ± .015 amps	100 μs	1.0 ± .1 μs	1.0 ± .1 μs	
C	I_{set}	.295 ± .020 amps	100 μs	1.0 ± .1 μs	1.0 ± .1 μs	
D	I_{read}	1.2 ± .06 amps	10 μs	0.5 ± .05 μs	1.0 ± .1 μs	

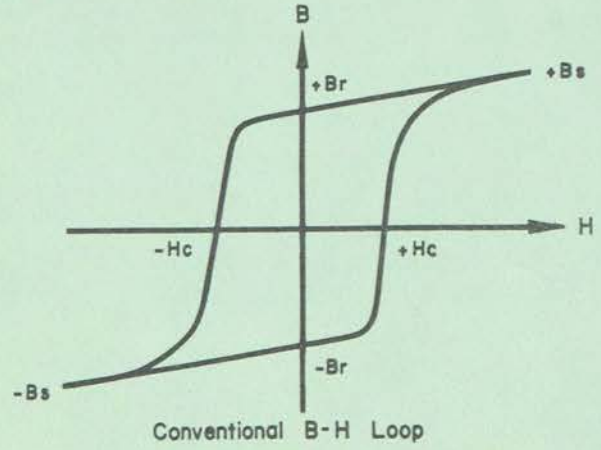
Pulse Program
Pulse rate 2 kc



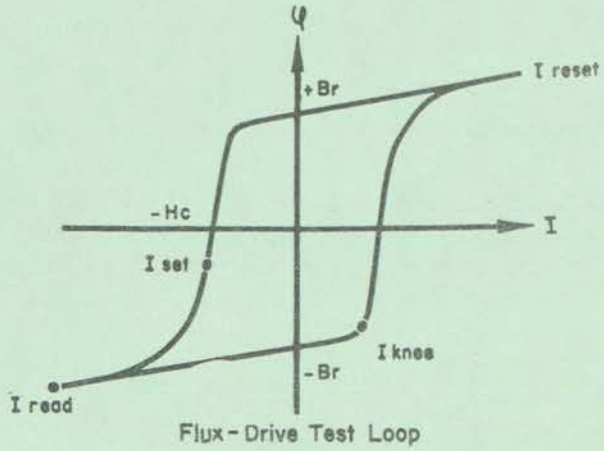
Output Test Signals: Output signals are read with an integrator with a time constant of 12 μs ± 1% (1/e value).

Read H_{mv}	----------	40 mv min. 50 mv max.
Read Knee	----------	6 mv max.
Read φ/t	----------	97 mv ± 2 mv

DEFINITIONS:



Conventional B-H Loop

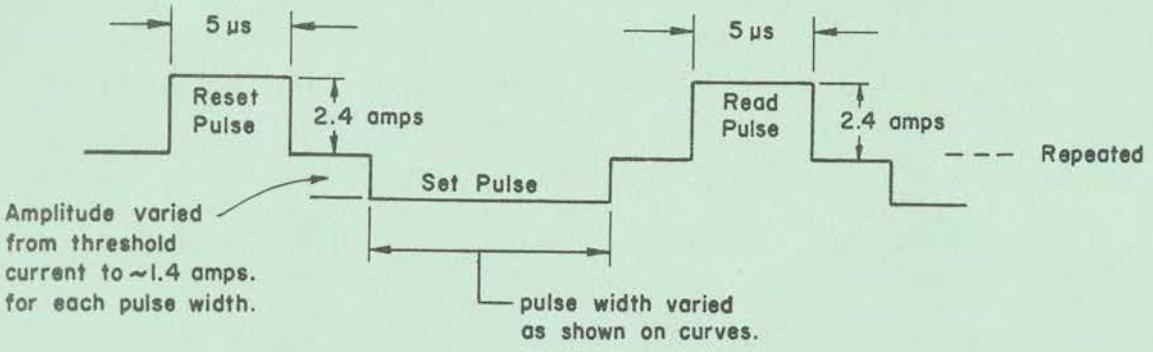


Flux-Drive Test Loop

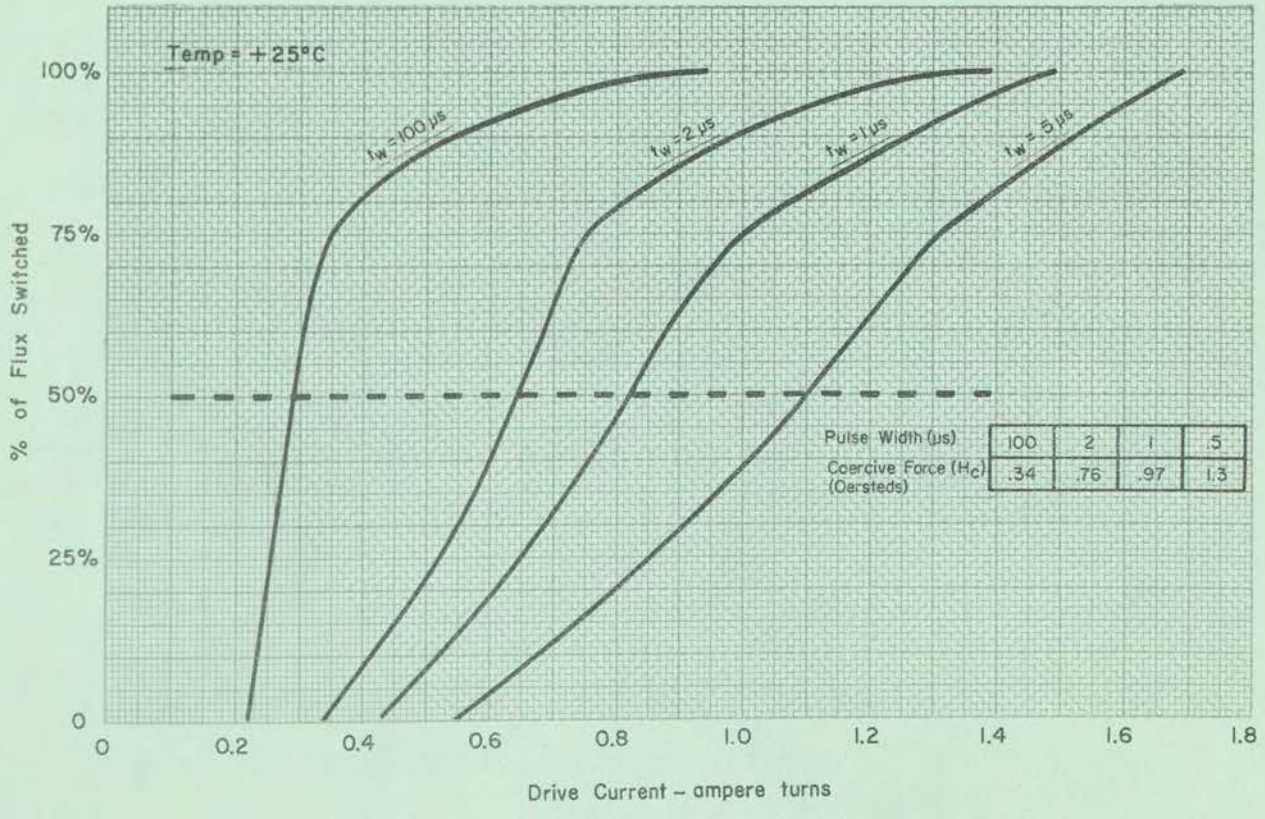
181-101 SWITCH CORE CHARACTERISTICS

FLUX TRANSFER AS A FUNCTION OF PULSE WIDTH SET CURRENT

Pulse Program: Pulse rate 2 kc.



Output signals are read with an integrator with a time constant of 12 µs ± 1% (1/e value).



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SWITCH CORE DEFINITIONS

I = Drive Current Amplitude. Value of the flat top portion of current used to switch core.

I_{reset} = A drive current of sufficient amplitude and duration to switch a core to its saturated state. Value of the flux density at this point is represented $\pm B_S$, saturation flux density.

I_{set} = The current required to drive the core from a remanent magnetic state towards the opposite saturation state, placing an arbitrary amount of flux (unsaturated) in the core.

I_{knee} = A current pulse of defined width having sufficient amplitude to cause the core to reach the switching threshold of the non-recoverable flux.

I_{read} = A current pulse of sufficient amplitude and duration to saturate the switch core in the direction opposite the reset current. This current is applied following a set current, knee current, or a reset current.

H_{mv} = The output of the switch core measured in millivolts at the output of an integrator with a time constant of 12 μs ± 1% (1/e value) when I_{read} current is applied to the core in the direction opposite the I_{reset} current. This is defined as a stable point in the high permeability region of switching, and is close to the H_c point.

H_c = The coercive force is the drive of defined pulse width necessary to bring the flux density of the core to zero. (i.e.) 50% of saturation flux density.

φ/t = The flux output of the switch core measured in millivolts at the output of an integrator with a time constant of 12 μs ± 1% (1/e value) when I_{read} current is applied to a core in one saturated magnetic state driving it into the other saturated magnetic state.

t_o = Reference Time, designated as the time when the drive current pulse reaches 10% of I on the rise.

t_r = Rise Time of the drive current pulse from t_o to 90% of I.

t_w = Pulse Width, or the time the drive current pulse remains above the 90% level.

t_f = Fall Time of the drive current pulse from 90% to 10% of I.

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Thank you for your recent inquiry. The information you requested is enclosed.

We look forward to the pleasure of supplying ferrite cores, arrays and stacks, or complete memory systems to you.

Please let us know how EMI may be of further assistance to you by contacting the office nearest you.

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NEW MEXICO
Southwest Electronic Industries, Inc.
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Albuquerque
Tel: (505) 255-2278
TWX: (505) 243-8407

NEW YORK
Advanced Components Corp.
119 Luther Avenue
Liverpool
Tel: (315) 472-7886
TWX: (315) 477-1090

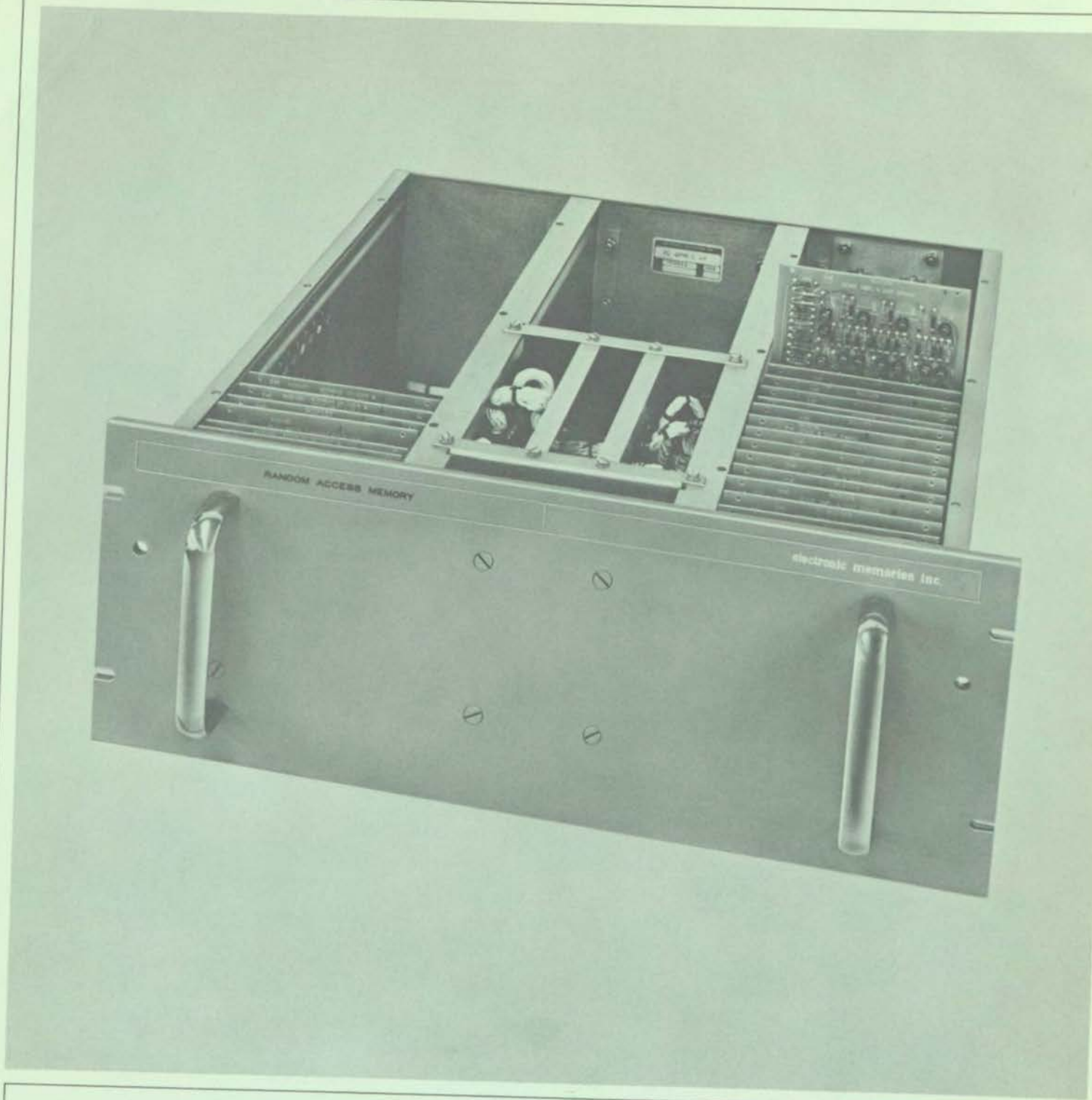
Advanced Components Corp.
21 Cleveland Avenue
Binghamton
Tel: (607) 723-7650

OHIO
Jay Engineering Company
1721 E. Third Street
Dayton
Tel: (513) CL. 3-2151
TWX: (513) 944-0256

Jay Engineering Company
4712 W. 130th Street
Cleveland
Tel: (216) 252-0486
TWX: (216) 252-7260

WASHINGTON
Myron R. Smith & Co., Inc.
6361 First Avenue South
Seattle
Tel: (206) PA. 5-1665

TEXAS
Southwest Electronic Industries, Inc.
183 Meadows Building
Dallas
Tel: (214) EM. 3-1671
TWX: (214) 899-9200



SEMS-4R CORE MEMORY SYSTEM

Capacity:	256 to 8192 words 6 to 40 bits per word
Speed:	4 μsec cycle time, 1 μsec access time
Operating Temperature Ranges:	−40°C to +85°C −20°C to +65°C 0°C to +50°C
Size:	17″ x 17″ x 7″ (19″ rack mounting)
Volume:	2023 cubic inches

Meets MIL shock, vibration and humidity specifications

electronic memories inc.
12621 Chadron Avenue, Hawthorne, California 90250
(213) 772-5201 / TWX: 213-647-5161

THE SEMS-4R

Volume: 2023 cubic inches

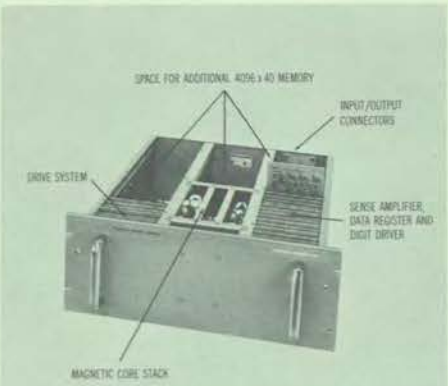
Capacity: 8192 words of 40 bits

Speed: Access time 1.0 μsec; 220,000 random memory cycles per second; cycle time 4.0 μsec

Environments: MIL-Q-9858, MIL-E-16400E, MIL-E-4158B, MIL-STD-810 for GSE

The SEMS-4R is a low cost, rack mounted, printed circuit memory providing high reliability in severe environments. A wide range of word capacities and bit sizes is available. The SEMS-4R may be obtained in three operating temperature ranges.

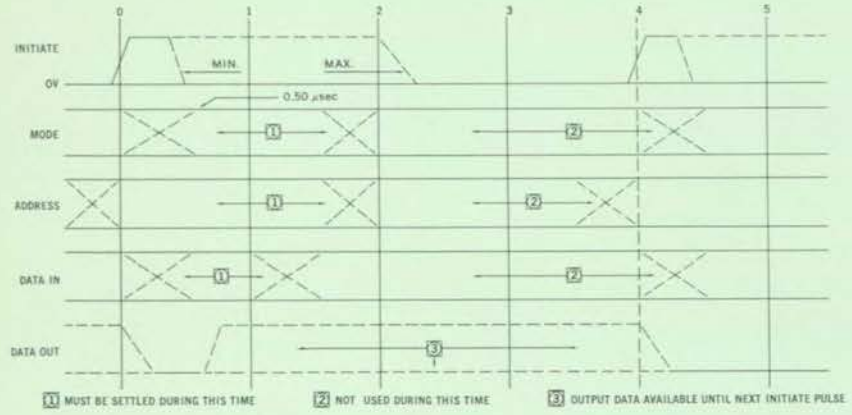
The memory system offers two functional options: sequential count and sequential interlace. Hardware options are rack mounting slides and power supply. The SEMS-4R is also available with a self-testing option. Special options to meet specific customer requirements can be arranged.

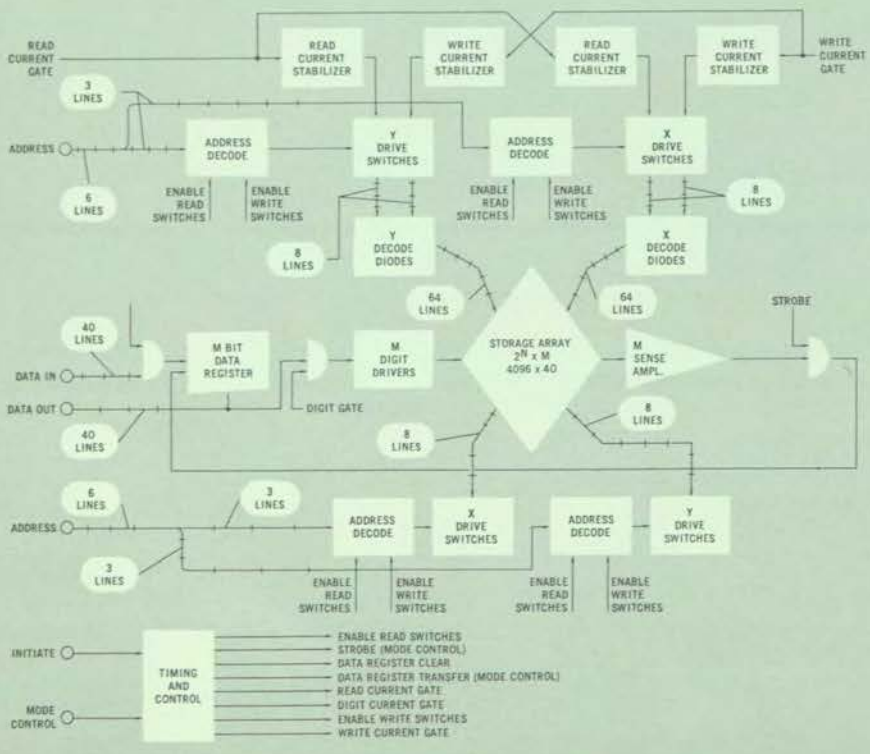


4096 x 40 SEMS-4R MEMORY SYSTEM

The SEMS-4R is designed for shipboard, mobile and ground-based military, industrial and commercial uses where speed, reliability and mobility are required design criteria.

TIME IN MICROSECONDS





SPECIFICATIONS

Storage Capacity	256, 512, 1024, 2048, 4096 or 8192 words of 6 to 40 bits
Operating Temperature	−40°C to +85°C −20°C to +65°C 0°C to +50°C
Storage Temperature	−62°C to +100°C
Altitude	50,000 ft.
Read/Restore Cycle Time	4.0 μsec
Clear/Write Cycle Time	4.0 μsec
Access Time	1.0 μsec
Operating Rate	0 to 250 KC
Input Signal Levels	Binary 0 = 0V to 0.5V Binary 1 = +4V to +7V
Output Signal Levels	Binary 0 = 0V to 0.25V Binary 1 = +5V to +6.5V
Input Currents	
A. Address	3 ma. max. for 1.5 μsec if line is in + state; 0 ma. if line is in 0 state
B. Mode Control	0.4 ma. in 0 state (CLEAR/WRITE), 0 ma. when in + state (READ/RESTORE)
C. Information	0 level — no current required + level — less than 1.0 ma.
D. Initiate	0 level — no current required + level — less than 1.0 ma.
E. Edge Current	In addition to the logic current required, approximately 9.0 ma. of edge current must be supplied to charge a capacity of approximately 200 μμf to effect a change from one logic level to another level within 100 nanoseconds
Output Current Information Lines	0 level — 0 current + level — +5 ma.

Input Signal Characteristics	Rise Time (μsec)	Width (μsec)
A. Address	.1	1.5 min.
B. Initiate	.1	0.2 to 2.0
C. Information Lines	.1	1.0 min.
D. Mode Control	level	level
Output Signal Characteristics		
Information	.1	2.0 min.

Power Requirement (4096 x 40)	55w at 4.0 μsec cycle time
Voltages Required	+15, +6, −3
Volume (8192 x 40)	2023 cubic inches
Weight (8192 x 40)	40 lbs.
Form Factor (8192 x 40)	17″ x 17″ x 7″ (19″ rack mounting)
Applicable Mil Specs	MIL-E-16400E, MIL-E-4158B, MIL-Q-9858
Vibration and Shock	MIL-STD-810 for GSE
Packaging	Encapsulated magnetics for severe environments Standard commercial magnetics for commercial environments

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2½-D memory operates in nanoseconds

Computer memory's unusual wiring scheme permits high-speed operation at low cost

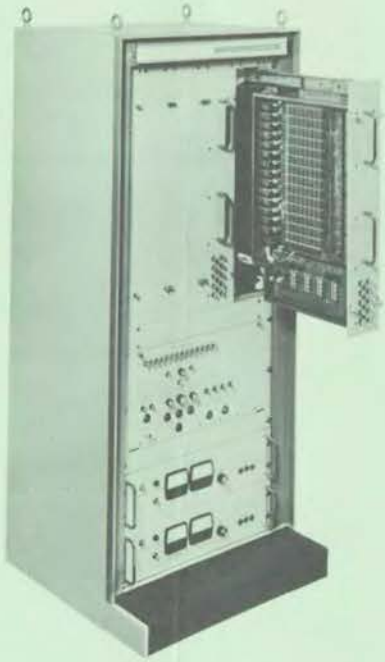
The world's fastest large-scale commercially available ferrite-core memory will make its debut at the Spring Joint Computer Conference in Boston, April 26 to 28. The Nanomemory 650, made by Electronic Memories, Inc., has a cycle time of 650 nanoseconds and an access time of 300 nanoseconds, for any of up to 16,384 words each of which may be as long as 84 bits.

This speed is attained with a 2½-dimensional organization, which combines the speed of a linear-select, or 2-D, design with the economy of a coincident-current, or 3-D, design. The cores are toroidal, similar to those in most conventional ferrite-core memories, with an outside diameter of 0.02 inch. The memory is faster than other big ferrite-core memories, and bigger than other fast memories, some of which are experimental only. [See p. 118; and Electronics, Dec. 28, 1965, p. 36, for example.]

The sketch below illustrates how the 2½-D combines the advantages of its 2-D and 3-D cousins.

A 2-D memory is organized as a single plane. It is expensive because, for high speed, a capacity of 2^n words requires decoding of n address bits.

Because a 3-D organization requires substantially less address decoding it is cheaper, but it is substantially slower. It is organized as a series of stacked planes; each plane contains one bit in each word contained in the memory.



In the 2½-D organization, the plane array resembles the 2-D; but the x-winding is doubled around to pass through two rows of cores. Current in the x-winding may pass in one direction or the other, depending on which of the two rows of cores is being addressed.

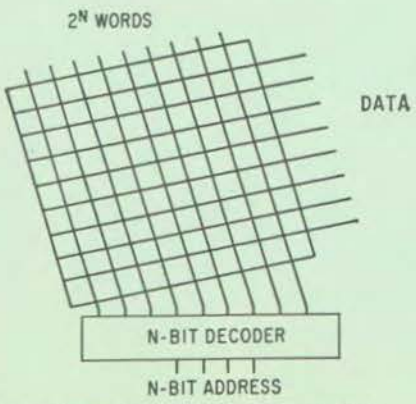
The Nanomemory 650 is complete with all electronic circuits in one package. However, only one side of the data register is available as output; if the user requires both 0 and 1 outputs, he must provide his own inverters in his own circuit package.

A price range of 6 to 8 cents per bit is quoted for the N-650. This comes to about $100,000 for the largest available size, 16,384 words by 84 bits.

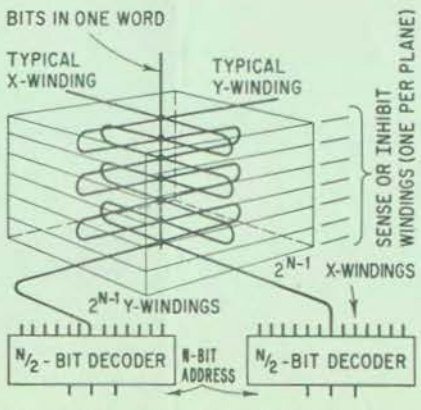
Specifications

Capacity	4,096, 8,192, or 16,384 words
Word length	8 to 84 bits
Operations	Read and restore Clear and write Read, modify and write (split cycle)
Cycle time	650 nanoseconds (read, write) 775 nanoseconds (minimum split)
Access time	300 nanoseconds
Input power	115 ±10 vac, 60 cps, single phase, 3 wire 700 watts normal, 1700 peak, typical (varies with word length)
Operating environment	+10° to +40° C., 90% relative humidity
Interface	Twisted-pair, either voltage or current. Either positive or negative voltage output (not both) !
Weight	350 pounds
Delivery	4½ to 5 months

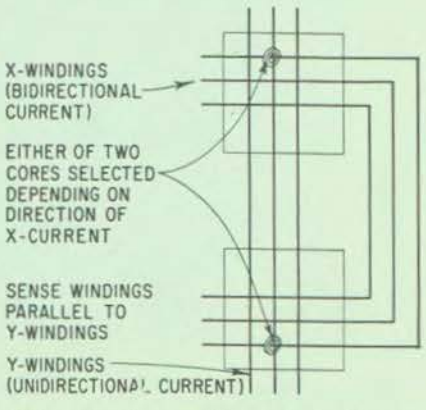
Electronic Memories, Inc., 12621 Chadron Ave., Hawthorne, Calif. 90250
Circle **350** on reader service card.



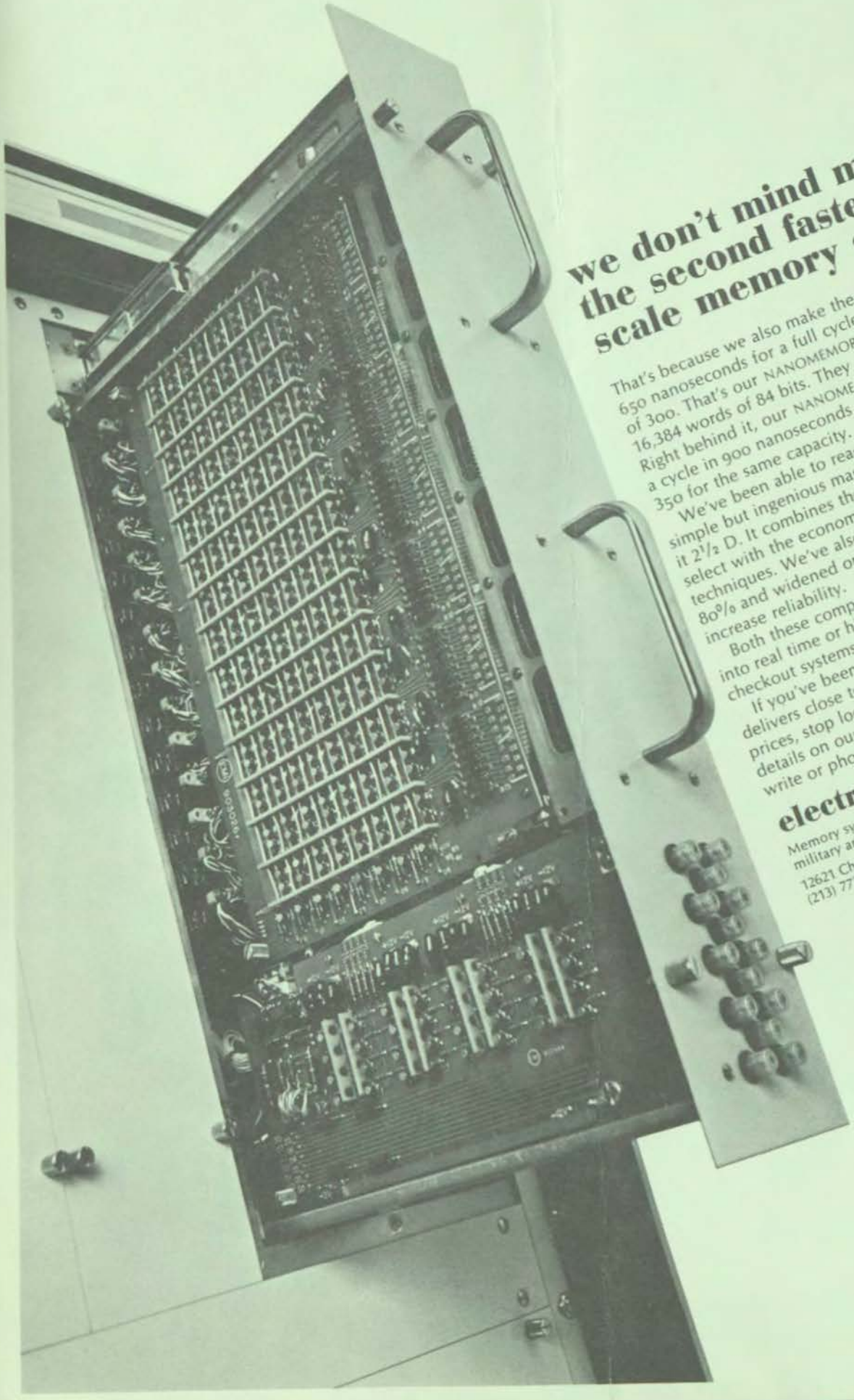
Two-dimensional organization is fast but quite expensive for large memories.



Three-dimensional organization is less expensive, but limited in speed.



Bidirectional current is part of address decoding in 2½-dimensional scheme.



we don't mind making the second fastest large scale memory system.

That's because we also make the fastest. How fast? 650 nanoseconds for a full cycle with an access time of 300. That's our NANOMEMORY™ 650. It handles up to 16,384 words of 84 bits. They don't come any faster. Right behind it, our NANOMEMORY 900 completes a cycle in 900 nanoseconds with an access time of 350 for the same capacity.

We've been able to reach these speeds by using a simple but ingenious magnetic organization. We call it 2½ D. It combines the speed potential of linear select with the economy of coincident current techniques. We've also reduced stack connections by 80% and widened operating margins to increase reliability.

Both these compact memory systems fit perfectly into real time or high speed computers and checkout systems.

If you've been looking for a memory system that delivers close to thin film speeds at magnetic core prices, stop looking. We've got two. For complete details on our NANOMEMORY 650 or 900, write or phone

electronic memories

Memory systems, stacks and cores for commercial, military and space applications
12621 Chadron Avenue, Hawthorne, California
(213) 772-5201

EMI 6176 4/66 1.5M