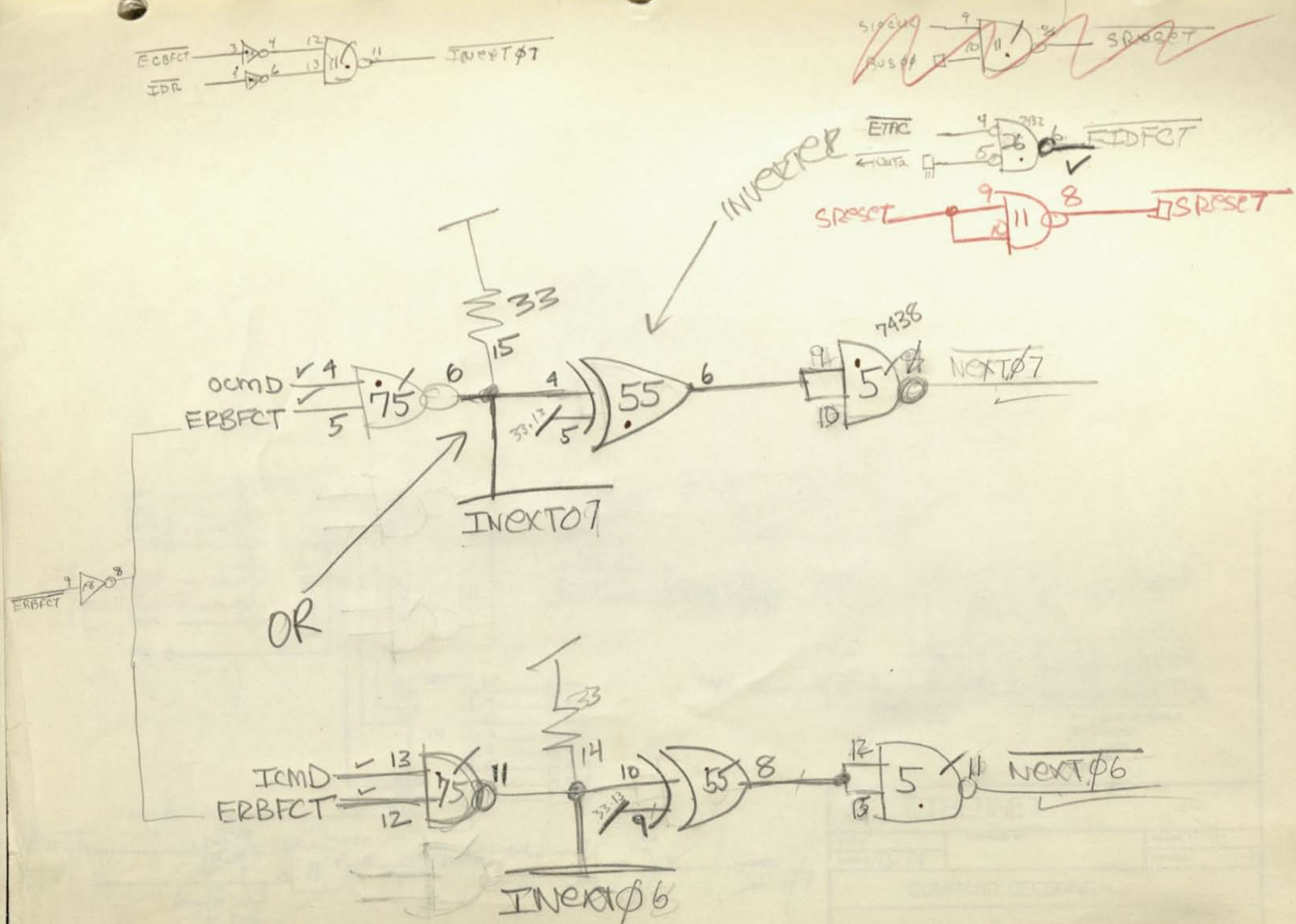
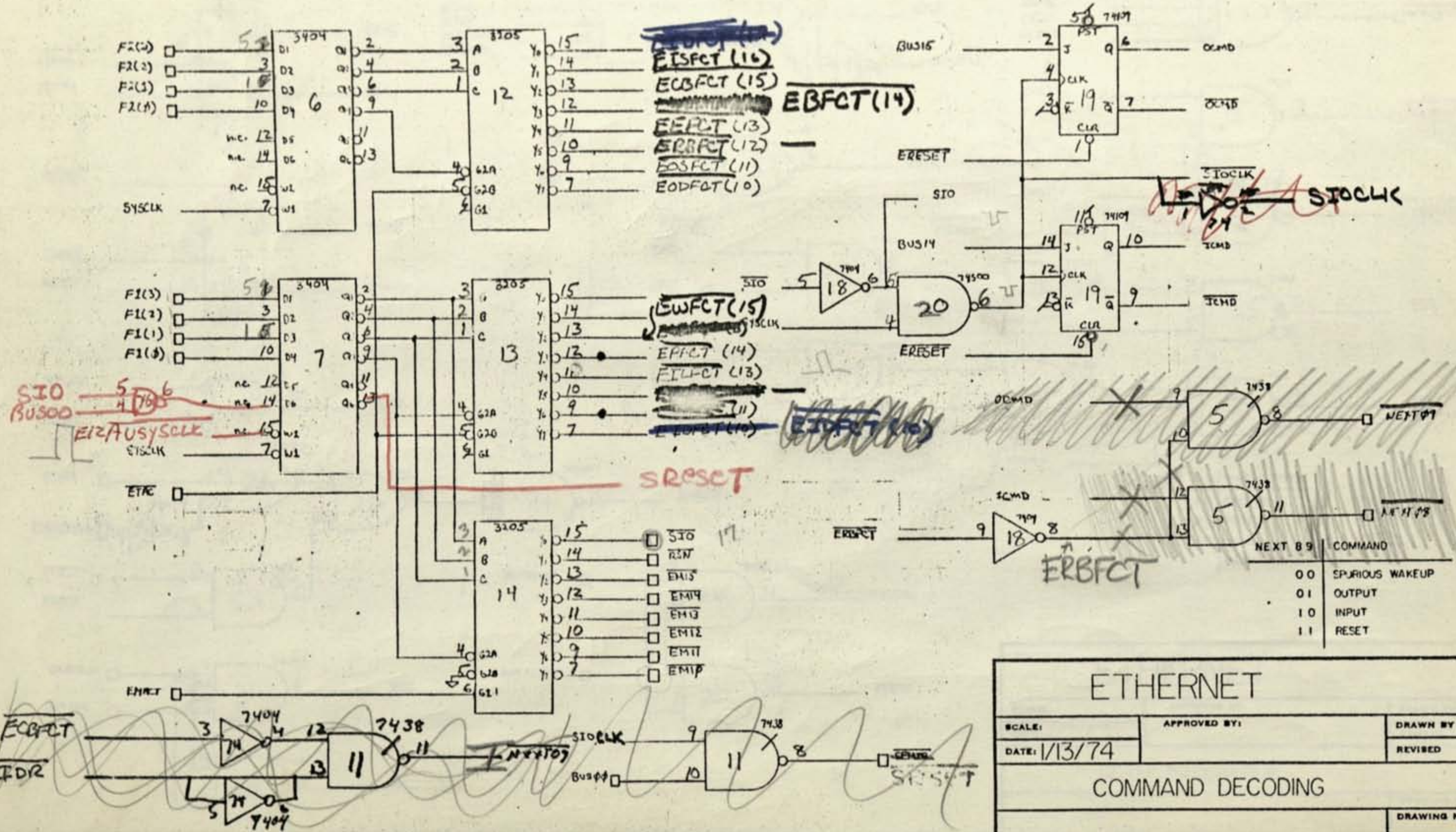


ECBFCT
IDR
INEXT07
SIOCLK
SRESET
ETAC
EIDFCT
INVERTER
SRESET
SRESET
7438
OCMD
ERBFCT
NEXT07
INEXT07
OR
ERBFCT
ICMD
ERBFCT
NEXT06
INEXT06



NEXT 89	COMMAND
00	SPURIOUS WAKEUP
01	OUTPUT
10	INPUT
11	RESET

ETHERNET

SCALE:

APPROVED BY:

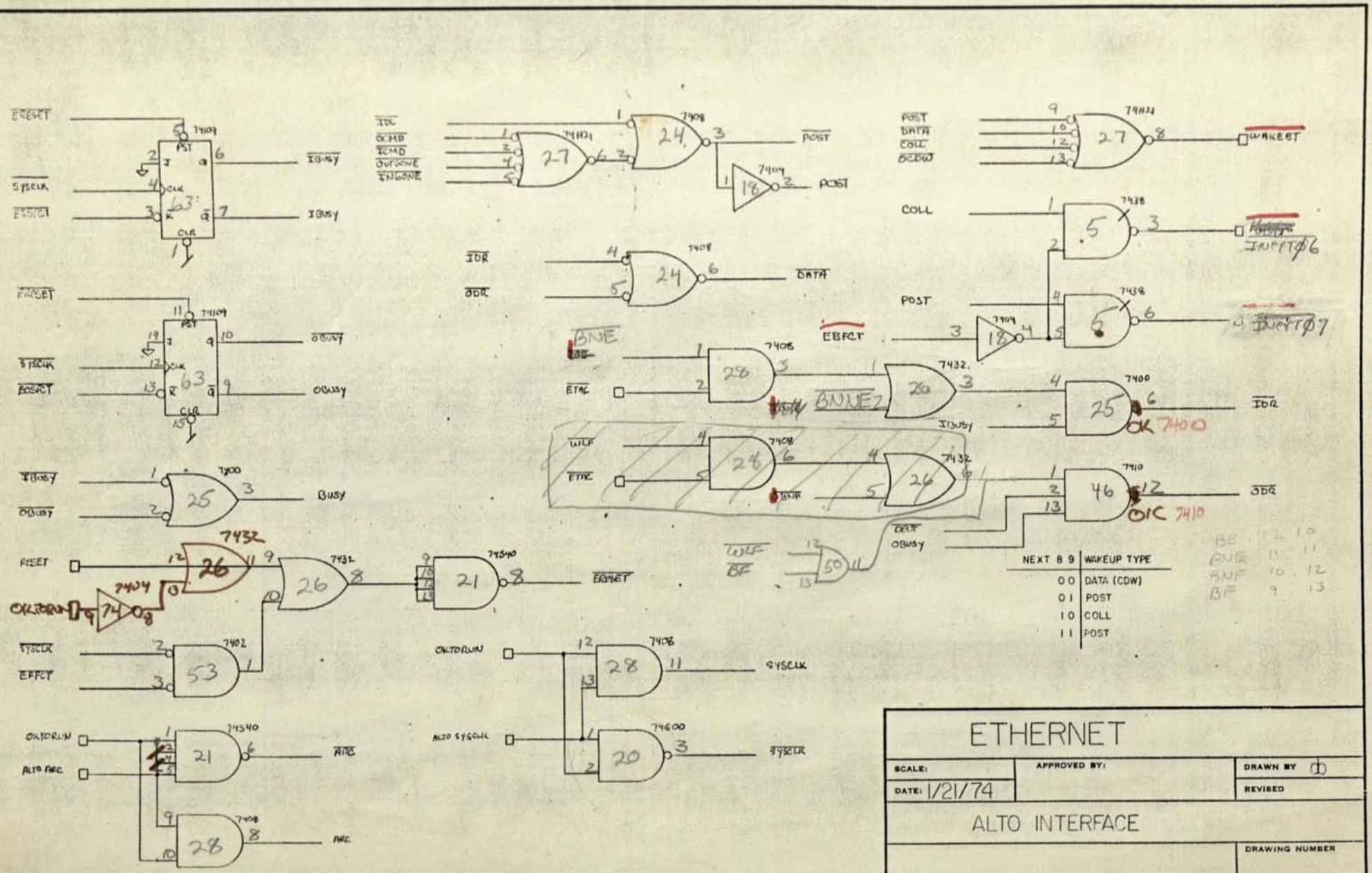
DRAWN BY ⓓ

DATE: 1/13/74

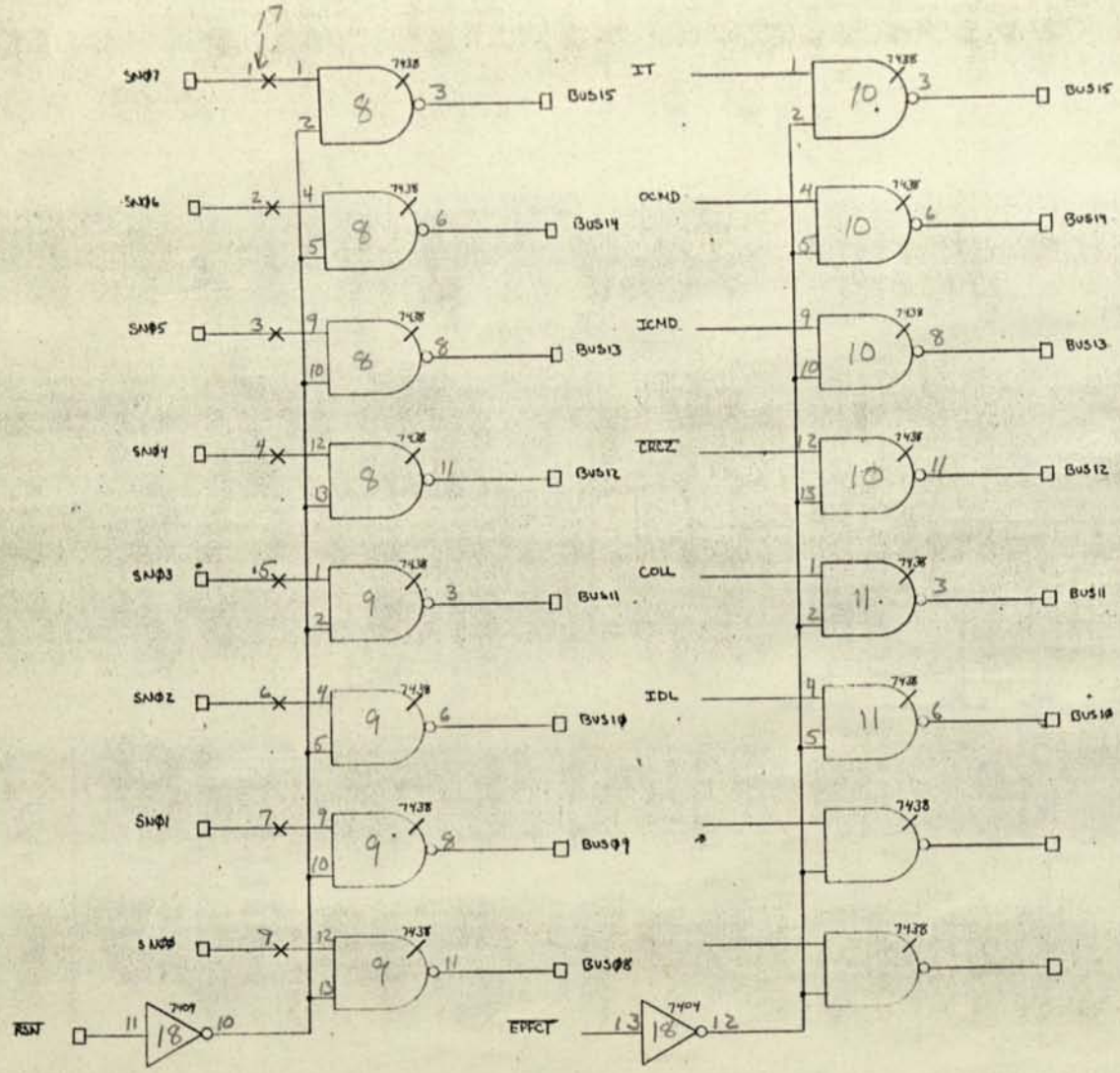
REVISED

COMMAND DECODING

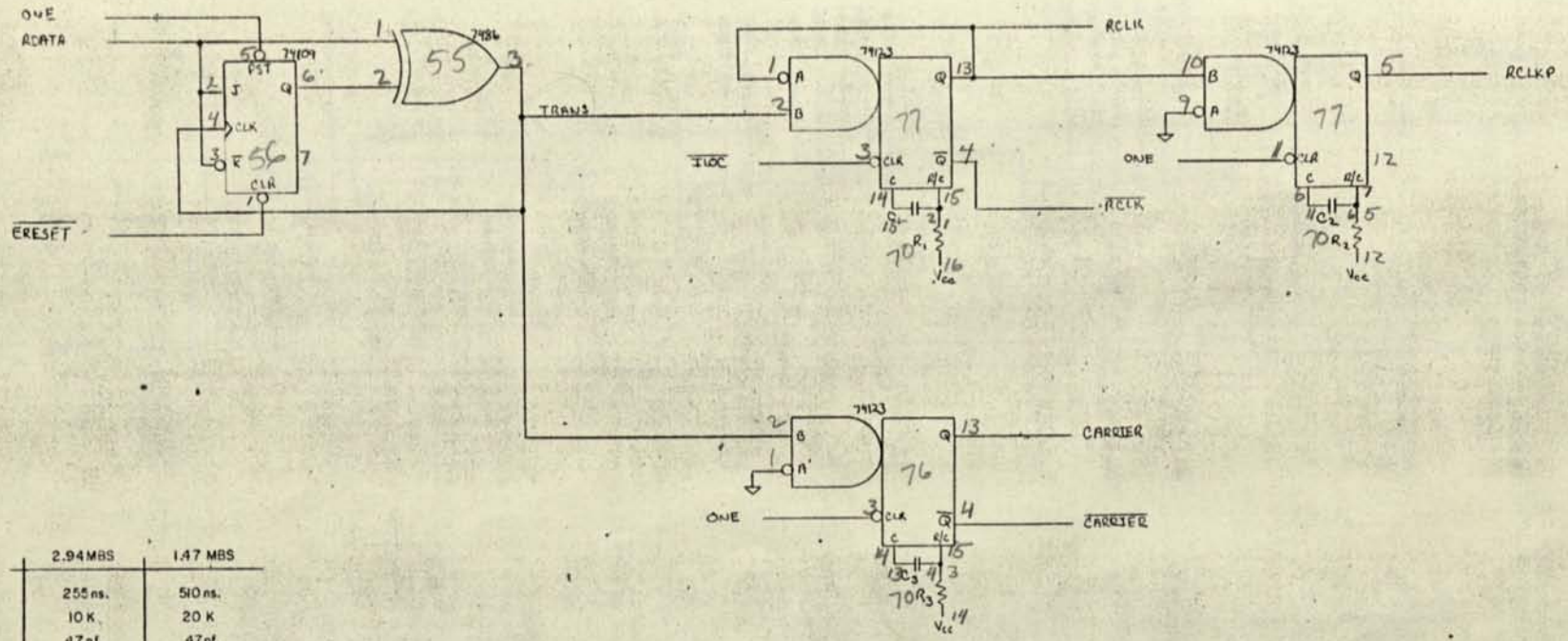
DRAWING NUMBER


ETHERNET
SCALE:
APPROVED BY:
DRAWN BY
DATE: 1/21/74
REVISED
ALTO INTERFACE
DRAWING NUMBER
NEXT 8 9 | WAKEUP TYPE
0 0 | DATA (CDW)
0 1 | POST
1 0 | COLL
1 1 | POST
BE 12 10
BNE 11 11
BNF 10 12
BF 9 13
PRINTED ON NO. 1000H CLEARPRINT

101111



ETHERNET		
SCALE:	APPROVED BY:	DRAWN BY db
DATE: 1/16/74		REVISED
SERIAL NUMBER & STATUS		
		DRAWING NUMBER



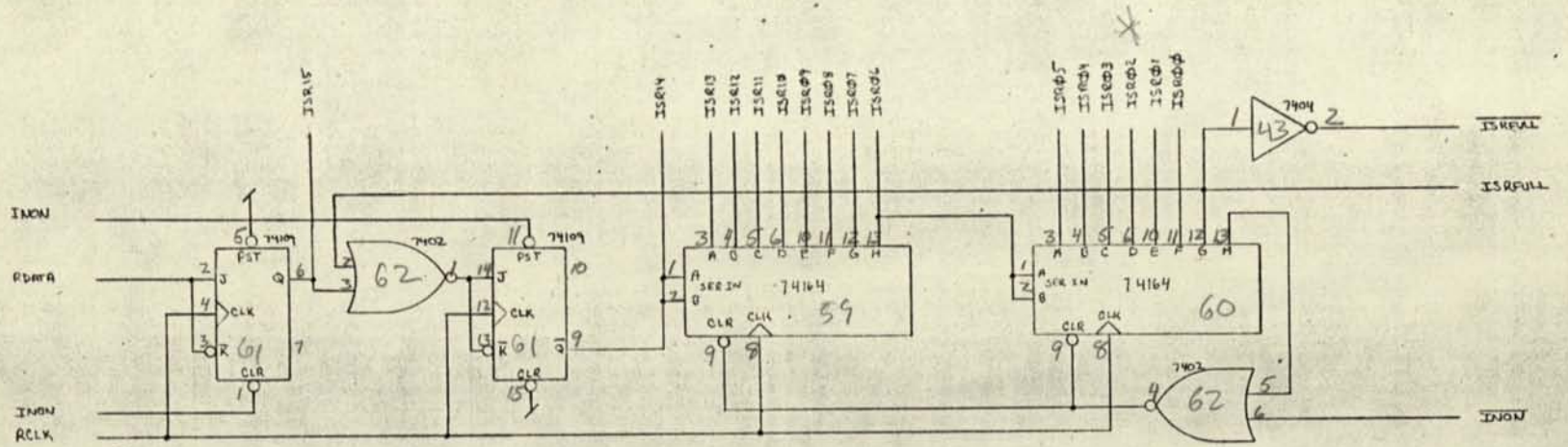
	2.94 MBS	1.47 MBS
T_1	255 ns.	510 ns.
R_1	10 K	20 K
C_1	47 pf.	47 pf.
T_2	170 ns.	340 ns.
R_2	5K	20K
C_2	68 pf.	33 pf.
T_3	425 ns.	850 ns.
R_3	20K	30K
C_3	39 pf.	62 pf.

ETHERNET

SCALE:	APPROVED BY:	DRAWN BY
DATE: 1/2/74		REVISED

PHASE DECODER

DRAWING NUMBER

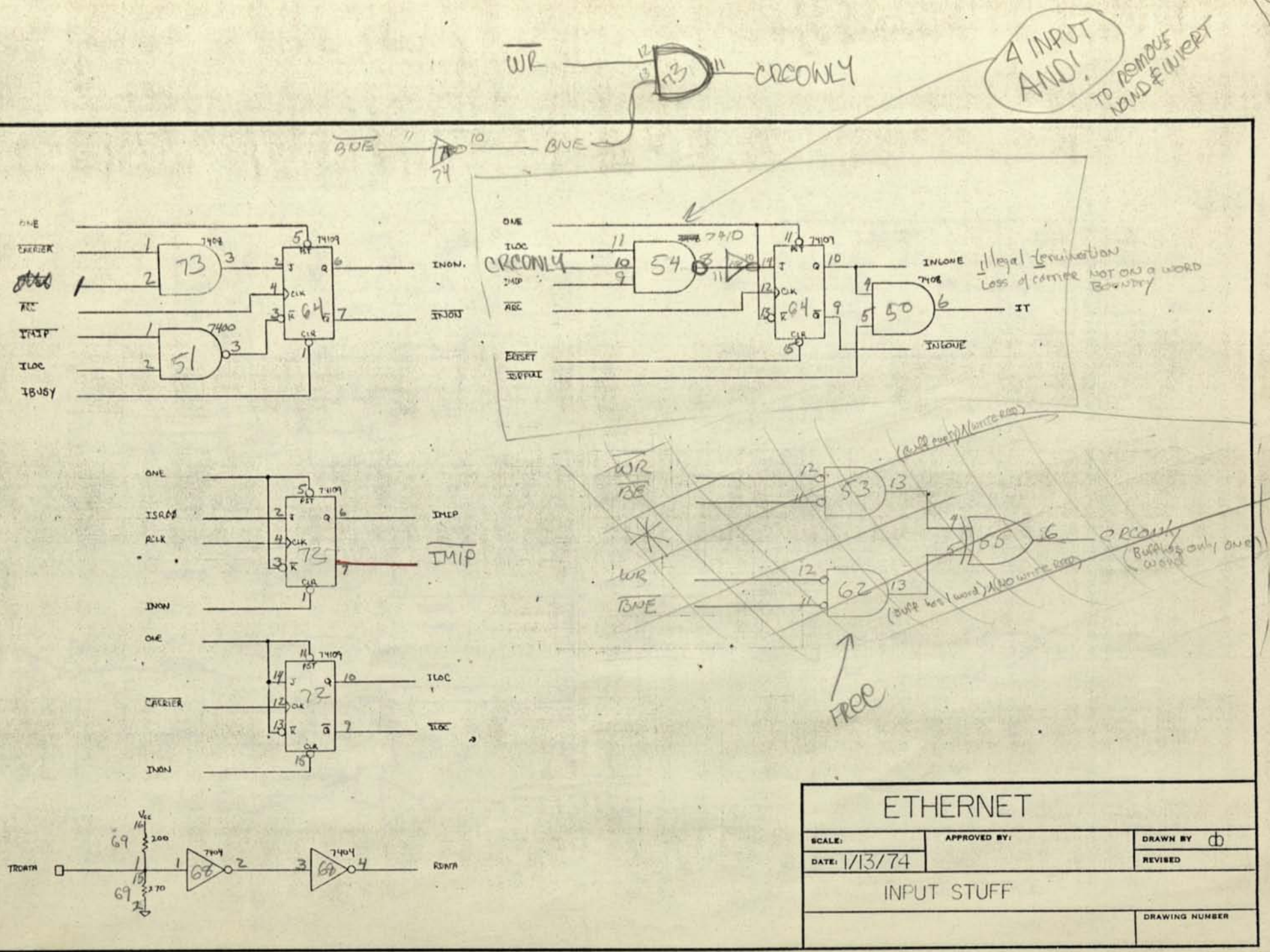


ETHERNET

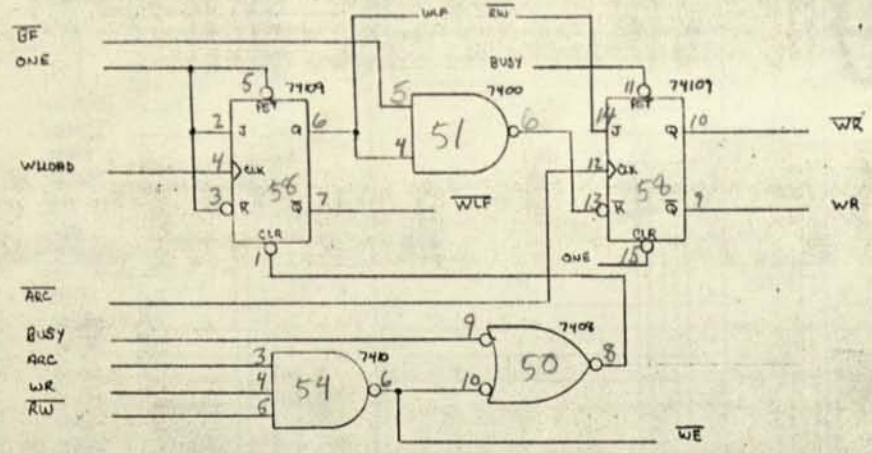
SCALE:	APPROVED BY:	DRAWN BY ch
DATE: 1/2/74		REVISED

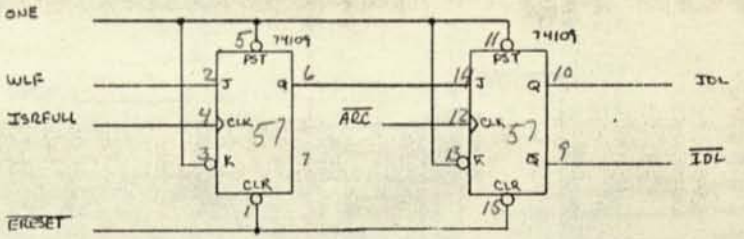
INPUT SHIFT REGISTER

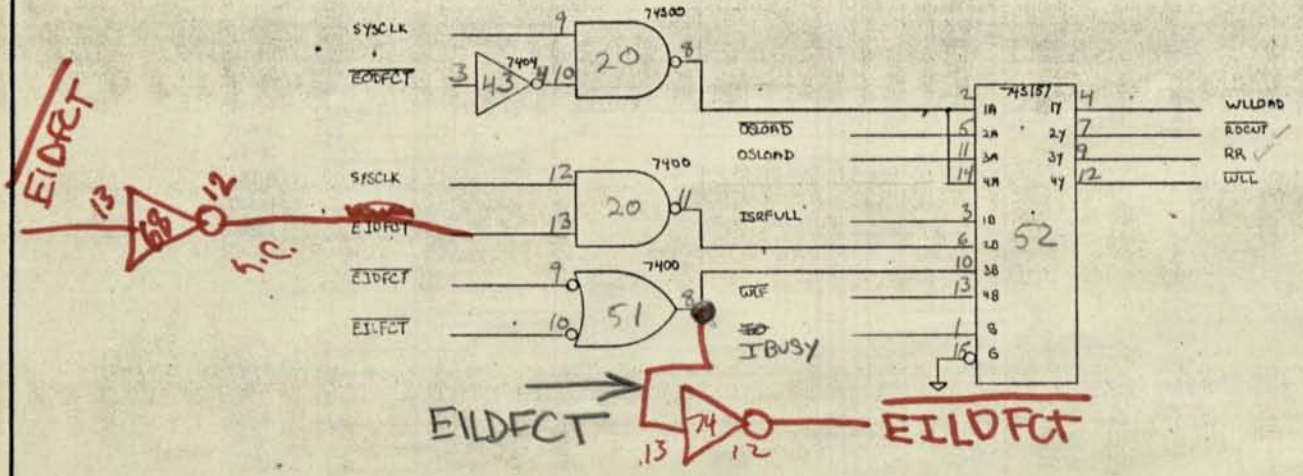
DRAWING NUMBER

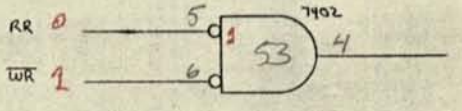


ETHERNET		
SCALE:	APPROVED BY:	DRAWN BY
DATE: 1/13/74		REVISED
INPUT STUFF		
		DRAWING NUMBER

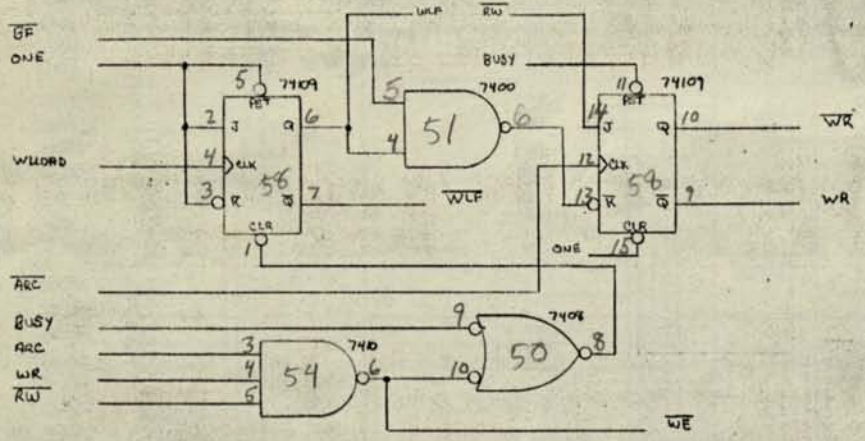


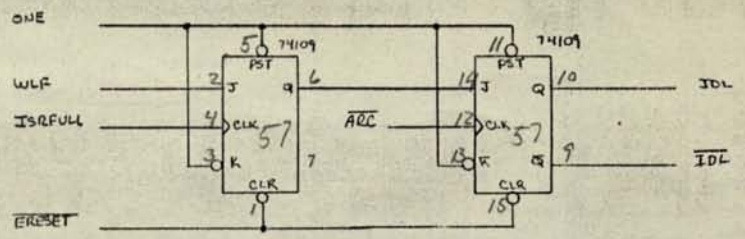


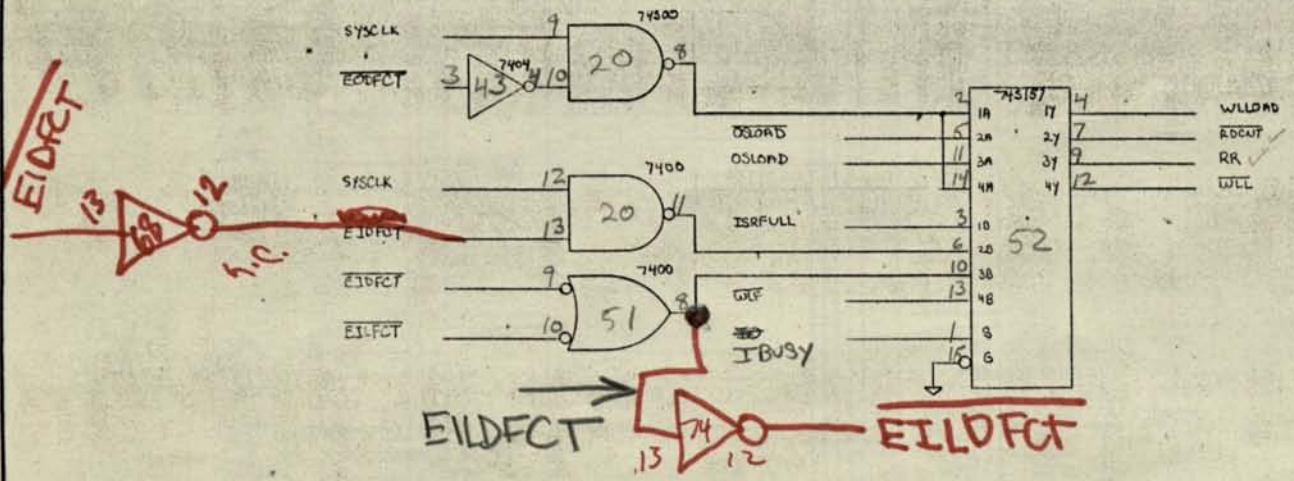


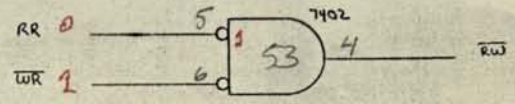


ETHERNET		
SCALE:	APPROVED BY:	DRAWN BY
DATE: 1/12/74		REVISED
BUFFER CONTROL		
		DRAWING NUMBER







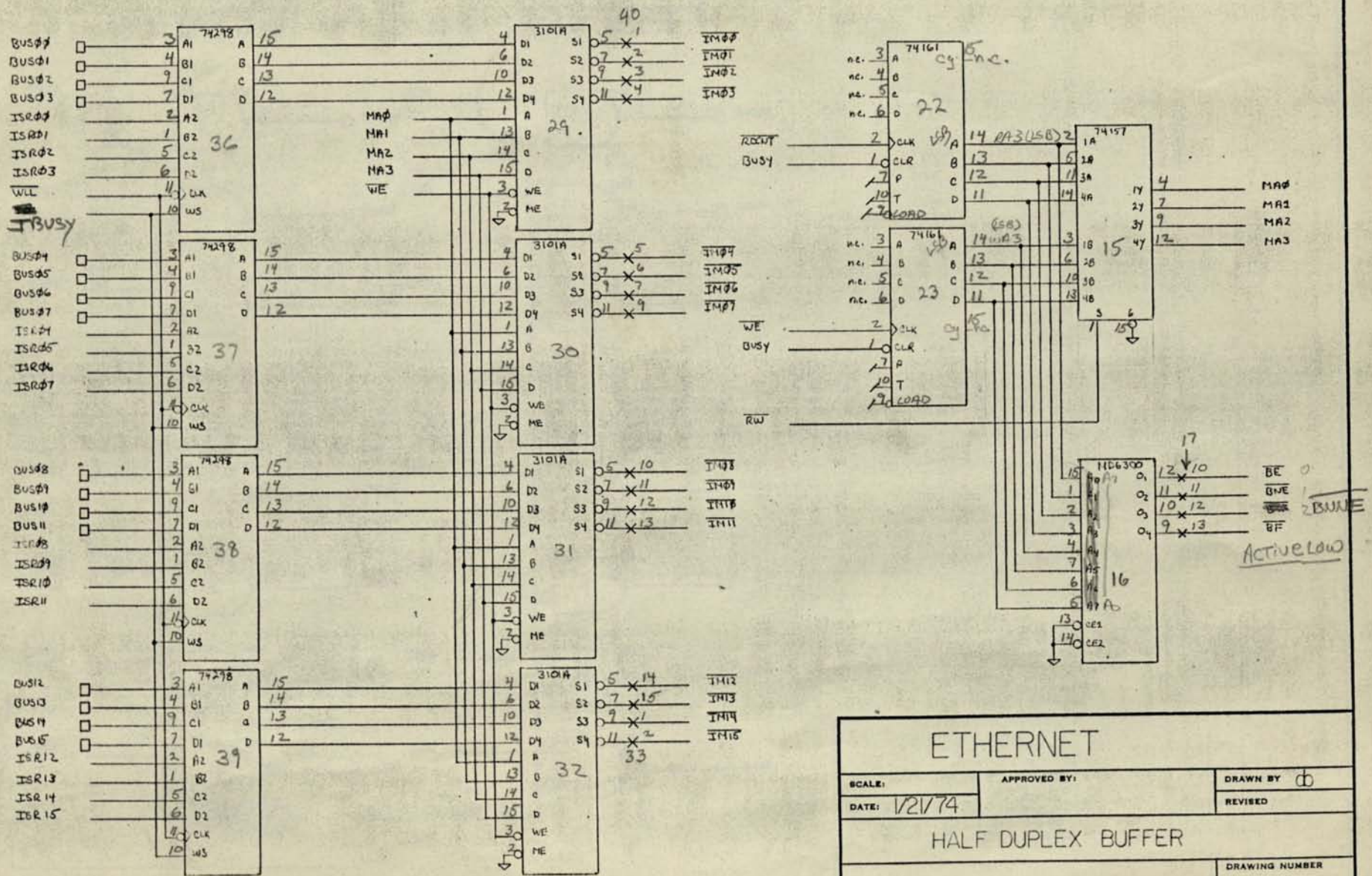


ETHERNET

SCALE:	APPROVED BY:	DRAWN BY
DATE: 1/12/74		REVISED

BUFFER CONTROL

DRAWING NUMBER

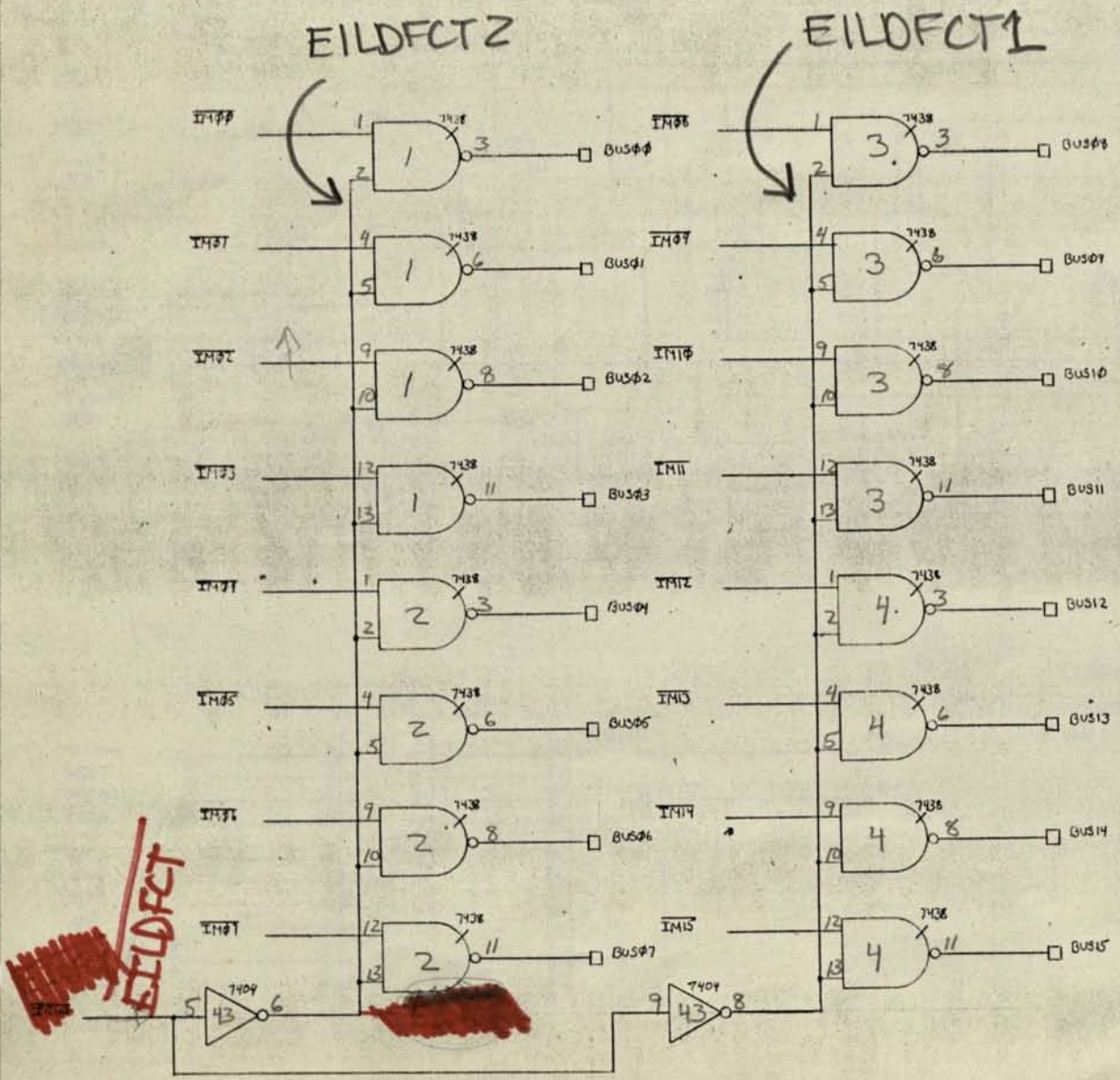


ETHERNET

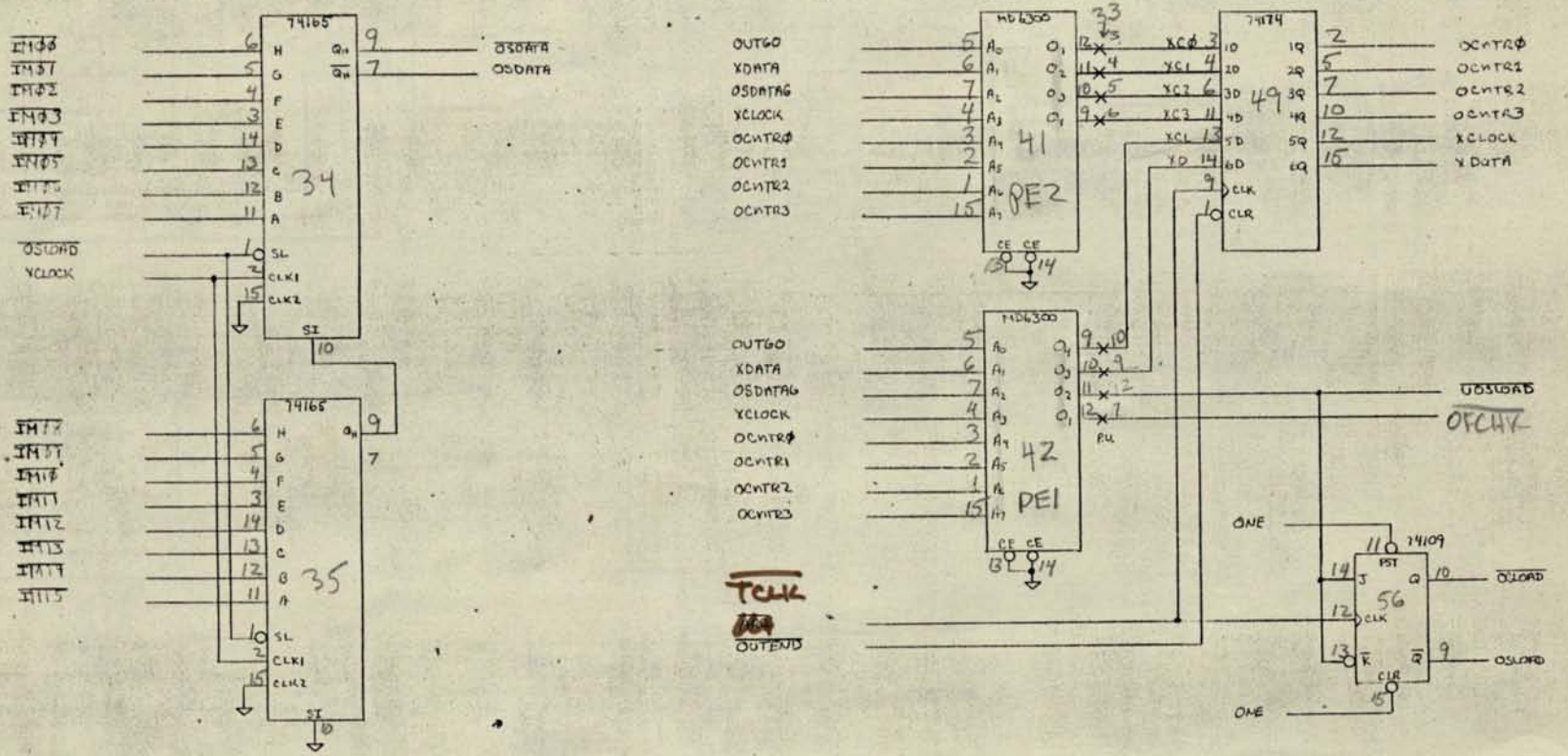
SCALE:	APPROVED BY:	DRAWN BY cb
DATE: 1/21/74		REVISED

HALF DUPLEX BUFFER

DRAWING NUMBER



ETHERNET		
SCALE:	APPROVED BY:	DRAWN BY cb
DATE: 1/3/74		REVISED
PROCESSOR BUS DRIVERS		
		DRAWING NUMBER

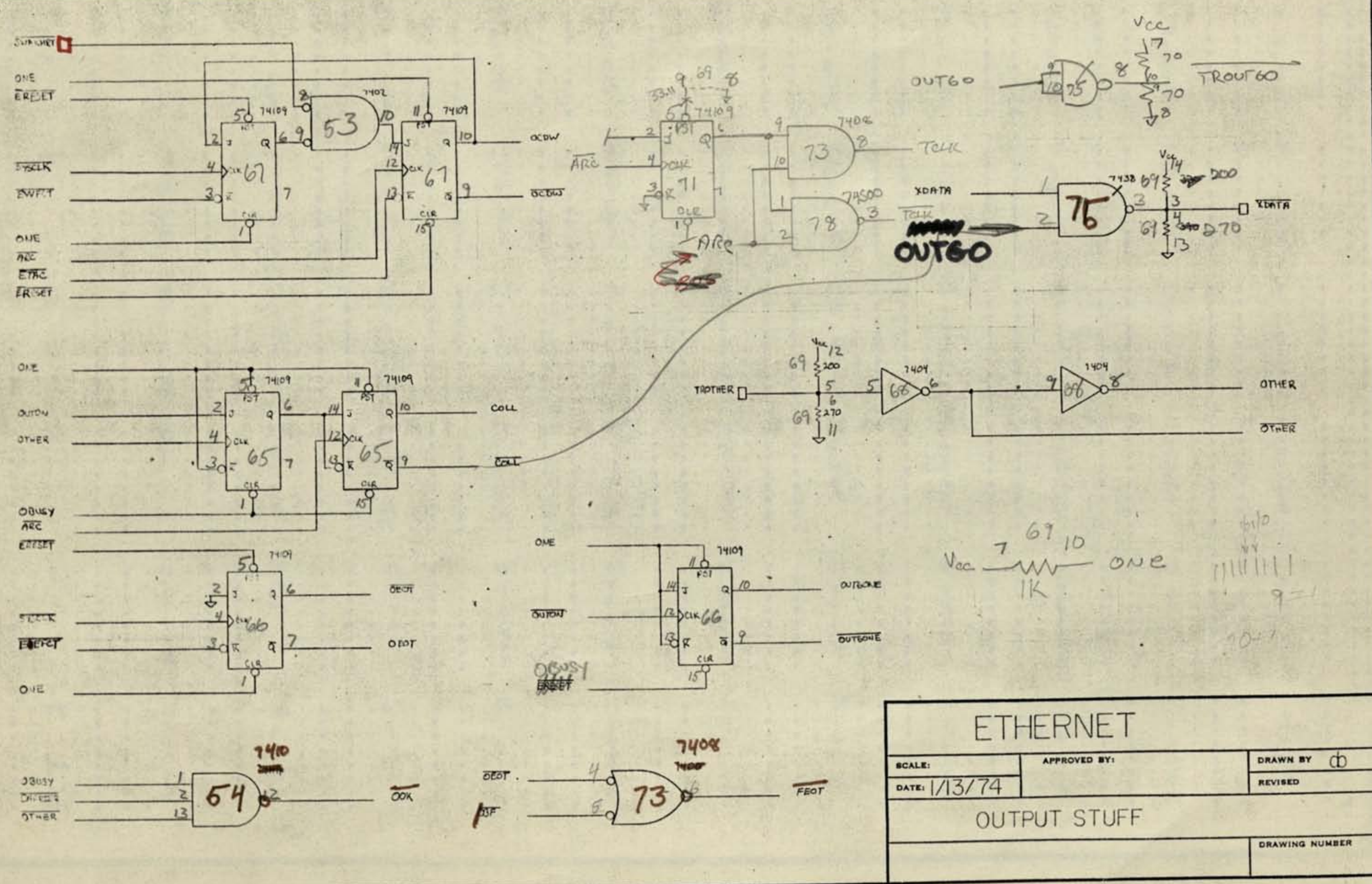


ETHERNET

SCALE:	APPROVED BY:	DRAWN BY cb
DATE: 1/2/74		REVISED

OUTPUT S.R. & PHASE ENCODER

DRAWING NUMBER



ETHERNET

SCALE:	APPROVED BY:	DRAWN BY cb
DATE: 1/13/74		REVISED

OUTPUT STUFF

DRAWING NUMBER

PRINTED ON NO. 1000H CLEARPRINT

1 7438	2 7438	3 7438	4 7438	5 7438	6 3404	7 3404
8 7438	9 7438	10 7438	11 7438	12 3205	13 3205	14 3205
15 74-57	16 MD6300	17 8888	18 7404	19 74-09	20 74S00	21 74S40
22 74-61	23 74-61	24 7408	25 7400	26 7432	27 74H21	28 7408
29 3-0-A	30 3-0-A	31 3-0-A	32 3-0-A	33 8888	34 74-65	35 74-65
36 7408	37 7408	38 7408	39 7408	40 8888	41 MD6300	42 MD6300
43 7404	44 2503	45 7457	46 7410	47 74-09	48 74-09	49 7474
50 7408	51 7400	52 7457	53 7402	54 7410	55 7486	56 74-08
57 74-09	58 74-09	59 74-64	60 74-64	61 74-08	62 7402	63 74-08
64 74-09	65 74-09	66 74-09	67 74-09	68 7404	69 PLT	70 PLT
71 74-09	72 74-08	73 7408	74 7404	75 7438	76 74-23	77 74-23
78 74S00	79	80	81	82	83	84 PLT

CONNECTOR:

16 – V_{cc}		1	GND
15 – spare		2	
14 – spare		3	
13 – spare		4	
12 – spare		5	
11 – TROTHER		6	
10 – $\overline{\text{TXDATO}}$		7	
9 – TRDATO		8	GND

* FILE CREATED 11-JUN-74 23:45:09
* ETHERNET2 MAIN WIRELIST

The chips run parallel to their names

	1	2	3	4	5	6	7
0	7438	7438	7438	7438	7438	I3404	I3404
7	7438	7438	7438	7438	I3205	I3205	I3205
14	74157	MD6300	B898-84	7404	74109	74S00	74S40
21	74161	74161	7408	7400	7432	74H21	7408
28	I3101A	I3101A	I3101A	I3101A	B898-84	74165	74165
35	74298	74298	74298	74298	B898-84	MD6300	MD6300
42	7404	MC8503	74157	7410	74109	74109	74174
49	7408	7400	74157	7402	7410	7486	74109
56	74109	74109	74164	74164	74109	7402	74109
63	74109	74109	74109	74109	7404	PLT84	PLT84
70	74109	74109	7408	7404	7438	74123	74123
77	74S00	-	-	-	-	-	PLT84
84	-	-	-	-	-	-	-

Chip 13=13: I3205 has unused groups: 3
Chip 28=28: SN7408 has unused groups: 2
Chip 53=53: SN7402 has unused groups: 4
Chip 55=55: SN7486 has unused groups: 4
Chip 62=62: SN7402 has unused groups: 4
Chip 71=71: SN74109 has unused groups: 2
Chip 76=76: SN74123 has unused groups: 2
Chip 78=78: SN74S00 has unused groups: 2 3 4

76.10 DOUBLE
76.2 76.7 NC

```
* FILE CREATED 11-JUN-74 23:48:40
* ETHERNET2          EDGE PINS

1     OKTORUN
2     RESET
3
4
5
6
7
8
9
10
11
12
13    AUSYSCLK
14
15
16
17
18    -SN00
19    -SN01
20    -SN02
21    -SN03
22    -SN04
23    -SN05
24    -SN06
25    -SN07
26
27
28
29
30    F1(0)
31    F1(1)
32    F1(2)
33    F1(3)
34
35
36    F2(0)
37    F2(1)
38    F2(2)
39    F2(3)
40
41    -SIO
42    -RSN
43    -EM15
44    -EM14
45
46    -EM13
47    -EM12
48    -EM11
49    -EM10
50
51
52
53
54
55
56
57
58
59
60
61
62    -SRESET
63    DBARC
64
65
66
67
68    -SWAKMRT
69
70
71
72    AUSYSCLK
73    TRDATA
74    TROTHER
75    -XDATA
76
77
78
79
80    BUS00
81    BUS01
82    BUS02
83    BUS03
84    BUS04
85    BUS05
86    BUS06
87    BUS07
88    BUS08
89    BUS09
90    BUS10
91    BUS11
92    BUS12
93    BUS13
94    BUS14
95    BUS15
96
97
98
99    EMACT
100   -ETAC
101
102
103   -WAKEET
104
105
106   -NEXT06
107   -NEXT07
108
109
110
111   'KDATA
112   INON
113   IBUSY
114   OBUSY
115   OUTON
116
117
118
119
120
121
122
```

$$ +:	6☆15	6☆13 7☆11 13☆15 61☆10 23☆5 22☆3 67☆7	6☆11 7☆14 12☆15 61☆7 23☆4 48☆7 65☆7	6☆14 7☆12 56☆7 57☆7 23☆3 47☆9 66☆7	6☆12 13☆7 77☆12 23☆15 22☆6 35☆7 66☆10	7☆15 13☆10 77☆4 22☆15 22☆5 34☆9	7☆13 13☆9 76☆13 23☆6 22☆4 71☆7	-3634	$
ARC:	78☆2	73☆12	54☆3	28☆10				-108	1
-ARC:	71☆4	64☆4 21☆6	64☆12	57☆12	58☆12	65☆12	67☆12	-376	2
AUSYSCLK:	28☆15	20☆1	E72					36	3
-BE:	43☆13	16☆12	17☆10					-134	4
-BF:	73☆5	51☆5	50☆15	16☆9	17☆13			-102	5
BNE:	73☆15	74☆12						-144	6
-BNE:	16☆11	17☆11	28☆1	74☆13				-118	7
-BNNE:	16☆10	17☆12	26☆2					-134	8
BUS00:	36☆3	1☆3	E80	11☆12				-448	9
BUS01:	36☆4	1☆6	E81					-464	10
BUS02:	36☆9	1☆10	E82					-464	11
BUS03:	36☆7	1☆13	E83					-464	12
BUS04:	37☆3	2☆3	E84					-464	13
BUS05:	37☆4	2☆6	E85					-464	14
BUS06:	37☆9	2☆10	E86					-464	15
BUS07:	37☆7	2☆13	E87					-464	16
BUS08:	38☆3	9☆13	3☆3	E88				-944	17
BUS09:	38☆4	9☆10	3☆6	E89				-944	18
BUS10:	3☆10	E90	11☆6	9☆6	38☆9			-1424	19
BUS11:	9☆3	3☆13	E91	11☆3	38☆7			-1424	20
BUS12:	39☆3	4☆3	E92	10☆13	8☆13			-1424	21
BUS13:	39☆4	4☆6	E93	10☆10	8☆10			-1424	22
BUS14:	39☆9	19☆14	4☆10	E94	10☆6	8☆6		-1408	23
BUS15:	39☆7	19☆2	E95	4☆13	10☆3	8☆3		-1408	24
BUSY:	25☆3	23☆1	22☆1	50☆11	58☆11			-80	25
-CARRIER:	54☆2	76☆4	73☆1	72☆12				-96	26
COLL:	65☆10	11☆1	5☆1					-128	27
-COLL:	27☆14	65☆9						-140	28

CRCDATA:	25*11	44*14						0	29
CRCGO:	51*14	48*10	25*12					-128	30
-CRCGO:	48*9	45*14	25*14					-128	31
CRCONLY:	73*13	54*12						-144	32
-CRCZ:	10*14	44*15						0	33
-DATA:	24*6	27*12						-140	34
DBARC:	28*11	21*5	E63					56	35
EBFCT:	18*4	5*2	5*5					-128	36
-EBFCT:	12*12	18*3						-84	37
ECBFCT:	11*14	74*4						-144	38
-ECBFCT:	12*13	74*3						-84	39
-EEFCT:	12*11	66*3						-84	40
EIDFCT:	68*14	20*15						-140	41
-EIDFCT:	51*11	68*15	26*6					-128	42
EILDFCT:	74*15	52*10 2*15	51*10 1*12	43*6 1*15	2*2 1*2	2*5 1*5	2*12	-160	43
-EILDFCT:	43*11	43*5	74*14					-128	44
EILDFCT1:	43*10	3*2 4*12	3*5 4*15	3*12	3*15	4*2	4*5	-32	45
-EILFCT:	13*11	51*12						-84	46
-EISFCT:	12*14	63*3						-84	47
-EM10:	E49	14*7						-100	48
-EM11:	E48	14*9						-100	49
-EM12:	E47	14*10						-100	50
-EM13:	E46	14*11						-100	51
-EM14:	E44	14*12						-100	52
-EM15:	E43	14*13						-100	53
EMACT:	E99	14*6						3	54
EODFCT:	20*12	43*4						-140	55
-EODFCT:	12*7	43*3						-84	56
-EOSFCT:	12*9	63*13						-84	57
EPFCT:	11*5	11*2	18*14	10*2	10*5	10*12	10*15	-64	58
-EPFCT:	53*3	18*15	13*12					-68	59
ERBFCT:	18*10	75*14	75*5					-128	60

EILDFCT
51*10
74*13
52*10

-ERBFCT:	12*10	18*11						-84	61
ERESET:	26*10	21*15	21*14	21*12	21*11			0	62
-ERESET:	67*5	67*15 63*5	66*5 56*1	64*15 24*12	57*15 19*1	57*1 19*15	63*11 21*10	-120	63
-ETAC:	E100	13*5	12*5	26*4	28*2	67*13		54	64
-EWFCT:	13*13	67*3						-84	65
F1(0):	E30	7*10						3	66
F1(1):	E31	7*1						3	67
F1(2):	E32	7*3						3	68
F1(3):	E33	7*5						3	69
F2(0):	E36	6*10						3	70
F2(1):	E37	6*1						3	71
F2(2):	E38	6*3						3	72
F2(3):	E39	6*5						3	73
FAST:	73*11	71*6	78*1					-124	74
-FEOT:	62*10	73*6						-144	75
GND001:	84*8	84*7	84*6	84*5	84*4	84*3		0	76
GND002:	84*2	84*1	83*8					0	77
GND003:	14*8	14*5						3	78
GND004:	56*8	63*14						16	79
GND005:	63*8	63*2						16	80
GND006:	68*7	75*7	75*8	76*1				16	81
GND007:	70*8	77*9						16	82
GND008:	62*7	69*11	69*8	69*2				0	83
GND009:	45*8	52*15						16	84
GND010:	16*14	16*13	9*8	9*7	2*7			32	85
GND011:	15*15	8*7	15*8					16	86
GND012:	24*7	31*2	31*8	32*2				6	87
GND013:	29*2	29*8	30*2					6	88
GND014:	43*7	43*8	44*3	44*5	44*6			6	89
GND015:	45*15	44*10	37*8					18	90
GND016:	42*14	42*13	35*8					32	91
GND017:	26*7	33*8	41*14	41*13				32	92

GND018:	35*10	28*7	28*8				16	93
GND019:	34*15	35*15	27*8	27*7	20*7		32	94
GND020:	71*8	71*3					16	95
GND021:	65*8	66*2					16	96
GND022:	54*7	61*8	69*13				0	97
GND023:	78*8	78*7					0	98
GND024:	81*8	74*7					0	99
GND025:	73*8	73*7					0	100
GND026:	67*8	60*7					0	101
GND027:	59*8	59*7					0	102
GND028:	55*8	55*7					0	103
GND029:	46*7	53*7	53*8				0	104
GND030:	44*7	51*7	51*8				0	105
GND031:	57*8	50*7					0	106
GND032:	18*7	25*7	25*8				0	107
GND033:	21*8	21*7					0	108
GND034:	4*7	11*7	11*8				0	109
GND035:	17*8	10*7					0	110
GND036:	5*8	5*7					0	111
GND037:	3*8	3*7					0	112
GND038:	1*8	1*7					0	113
IBUSY:	63*7	64*1 38*10	52*1 37*10	45*1 36*10	25*5	E113	39*10	0 114
-IBUSY:	25*1	63*6					-144	115
ICMD:	10*11	19*10	75*15				-128	116
-ICMD:	19*9	27*2					-140	117
IDL:	11*4	57*10					-144	118
-IDL:	24*1	57*9					-144	119
IDR:	11*15	74*6					-144	120
-IDR:	24*4	25*6	74*5				-128	121
ILOC:	72*10	51*2	54*13				-128	122
-ILOC:	77*3	72*9					-144	123
-IM00:	34*6	40*1	29*5	1*1			-118	124
-IM01:	34*5	40*2	29*7	1*4			-118	125

-IM02:	34☆4	40☆3	29☆9	1☆11			-118	126
-IM03:	34☆3	40☆4	29☆11	1☆14			-118	127
-IM04:	34☆14	40☆5	30☆5	2☆1			-118	128
-IM05:	34☆13	40☆6	30☆7	2☆4			-118	129
-IM06:	2☆11	30☆9	34☆12	40☆7			-118	130
-IM07:	2☆14	30☆11	34☆11	40☆9			-118	131
-IM08:	35☆6	40☆10	31☆5	3☆1			-118	132
-IM09:	35☆5	40☆11	31☆7	3☆4			-118	133
-IM10:	35☆4	40☆12	31☆9	3☆11			-118	134
-IM11:	35☆3	40☆13	31☆11	3☆14			-118	135
-IM12:	35☆14	40☆14	32☆5	4☆1			-118	136
-IM13:	35☆13	40☆15	32☆7	4☆4			-118	137
-IM14:	35☆12	33☆1	32☆9	4☆11			-118	138
-IM15:	35☆11	33☆2	32☆11	4☆14			-118	139
IMIP:	54☆11	72☆6					-144	140
-IMIP:	72☆7	51☆1					-144	141
INEXT06:	55☆10	5☆14	5☆15				-128	142
-INEXT06:	75☆13	55☆12	33☆14				-464	143
INEXT07:	55☆6	5☆11	5☆12				-128	144
-INEXT07:	11☆13	33☆15	55☆4	75☆6			-944	145
INGONE:	50☆4	64☆10					-144	146
-INGONE:	27☆5	64☆9					-140	147
INON:	E112	61☆11	61☆1	64☆6	72☆15	72☆1	16	148
-INON:	64☆7	45☆10	62☆6				-128	149
ISR00:	36☆2	72☆2	60☆13				-48	150
ISR01:	60☆12	36☆1					-64	151
ISR02:	60☆6	36☆5					-64	152
ISR03:	60☆5	36☆6					-64	153
ISR04:	60☆4	37☆2					-64	154
ISR05:	60☆3	37☆1					-64	155
ISR06:	37☆5	59☆15	60☆1	60☆2			-32	156
ISR07:	59☆14	37☆6					-64	157
ISR08:	59☆13	38☆2					-64	158

ISR09:	59*12	38*1						-64	159
ISR10:	59*6	38*5						-64	160
ISR11:	59*5	38*6						-64	161
ISR12:	59*4	39*2						-64	162
ISR13:	59*3	39*1						-64	163
ISR14:	39*5	61*9	59*2	59*1				-112	164
ISR15:	45*3	39*6	61*6	62*3				-112	165
ISRFULL:	43*1	57*4	52*3	60*14	62*2			0	166
-ISRFULL:	43*2	50*5						-144	167
IT:	10*1	50*6						-144	168
JUMPER:	71*5	69*9	33*11					32	169
MA0:	32*1	31*1	30*1	29*1	15*4			-148	170
MA1:	32*13	31*13	30*13	29*13	15*7			-148	171
MA2:	32*14	31*14	30*14	29*14	15*9			-148	172
MA3:	32*15	31*15	30*15	29*15	15*12			-148	173
-NEXT06:	5*3	5*13	E106					-960	174
-NEXT07:	5*6	5*10	E107					-960	175
OBE:	24*15	43*12						-144	176
OBUSY:	E114	46*15 63*9	66*15	65*15	65*1	50*1	54*1	32	177
-OBUSY:	25*2	63*10						-144	178
OCDW:	67*2	67*10						-144	179
-OCDW:	27*15	67*9						-140	180
OCMD:	10*4	19*6	75*4					-128	181
-OCMD:	19*7	27*1						-140	182
OCNTR0:	41*3	42*3	49*2					-128	183
OCNTR1:	41*2	42*2	49*5					-128	184
OCNTR2:	41*1	42*1	49*7					-128	185
OCNTR3:	41*15	42*15	49*10					-128	186
-ODR:	24*5	46*14						-144	187
-OEOT:	73*4	66*6	46*2					-128	188
OKTORUN:	74*11	28*12	28*14	21*1	20*2	E1		108	189
ONE:	71*1	71*2 72*11	66*13 72*3	72*14 72*5	64*13 64*5	64*11 57*13	72*13 57*11		

		57☆3 65☆11 66☆1 22☆9 48☆13 56☆15 61☆15 19☆11	57☆5 65☆3 63☆15 23☆10 48☆11 56☆11 61☆5 19☆3	58☆15 65☆5 63☆1 22☆10 48☆5 69☆10 67☆11 19☆5	58☆3 67☆1 21☆4 23☆7 47☆13 76☆3 13☆6	58☆2 66☆14 21☆2 22☆7 47☆11 77☆11 12☆6	58☆5 66☆11 23☆9 45☆13 47☆5 56☆5 19☆13	1542	190
-OOK:	62☆11	54☆14						-144	191
OSDATA:	25☆15	34☆7						-144	192
OSDATAG:	42☆7	41☆7	46☆6	45☆2				-112	193
OSLOAD:	56☆9	52☆11	51☆15	24☆14				-112	194
-OSLOAD:	34☆1	35☆1	56☆10	52☆5				-80	195
OTHER:	68☆10	65☆4						-128	196
-OTHER:	54☆15	68☆11	68☆6	73☆2				-112	197
-OUTEND:	49☆1	48☆1	48☆15	47☆15	24☆10			0	198
OUTGO:	75☆2	75☆12 42☆5	75☆11	48☆3	48☆2	47☆10	41☆5	-48	199
-OUTGONE:	50☆2	66☆9	27☆4					-124	200
OUTON:	65☆2	47☆6	47☆14	E115				-128	201
-OUTON:	66☆12	45☆11	46☆11	47☆7				-96	202
OUTRGO:	46☆4	48☆6						-144	203
-PESTOP:	47☆1	50☆3						-112	204
POST:	5☆4	18☆2						-144	205
-POST:	24☆3	18☆1	27☆11					-124	206
RCLK:	72☆4	59☆10 77☆1	61☆12	60☆10	61☆4	77☆10	77☆13	0	207
RCLKP:	77☆5	45☆6						-144	208
RDATA:	68☆4	61☆3	61☆2	55☆1	56☆2	56☆3		-80	209
-RDATA:	68☆3	68☆2						-144	210
-RDCNT:	52☆7	22☆2						-128	211
RESET:	E2	26☆14						16	212
RR:	52☆9	53☆5						-144	213
RSN:	18☆12	9☆2 8☆5	9☆5 8☆12	9☆12	9☆15	8☆15	8☆2	-32	214
-RSN:	18☆13	E42	14☆14					-84	215
-RW:	15☆1	58☆14	53☆4	54☆5				-112	216
SIO:	20☆5	18☆6						-140	217

-SIO:	14☆15	E41	18☆5					-84	218
SIOCLK:	74☆2	11☆11						-144	219
-SIOCLK:	20☆6	19☆12	19☆4	74☆1				-120	220
-SN00:	17☆9	9☆14	E18					16	221
-SN01:	17☆7	9☆11	E19					16	222
-SN02:	17☆6	9☆4	E20					16	223
-SN03:	9☆1	17☆5	E21					16	224
-SN04:	17☆4	E22	8☆14					16	225
-SN05:	17☆3	E23	8☆11					16	226
-SN06:	8☆4	17☆2	E24					16	227
-SN07:	8☆1	17☆1	E25					16	228
-SRESET:	E62	11☆10						-480	229
-SWAKMRT:	E68	53☆10						16	230
SYSCLK:	28☆13	20☆4	20☆14	20☆11	6☆7	7☆7		-94	231
-SYSCLK:	66☆4	67☆4	53☆2	63☆12	63☆4	20☆3		-56	232
TCLK:	46☆12	73☆10						-144	233
-TCLK:	49☆9	56☆12	48☆4	48☆12	47☆12	47☆4	78☆3	-24	234
TRANS:	56☆4	55☆3	76☆2	77☆2				-96	235
TRDATA:	84☆9	69☆15	69☆1	68☆1	E73			16	236
TROTHER:	84☆11	69☆6	69☆5	68☆5	E74			16	237
-TROUTGO:	75☆10	84☆12	70☆10	70☆9				-480	238
-UOSLOAD:	33☆12	42☆11	56☆13	56☆14				-118	239
VCC001:	69☆7	77☆16	70☆7	70☆12	70☆14			0	240
VCC002:	69☆12	69☆14	69☆16					0	241
-WAKEET:	E103	27☆10						-200	242
-WE:	54☆6	32☆3	31☆3	30☆3	23☆2	29☆3	50☆12	-100	243
WLF:	51☆4	58☆6	57☆2					-128	244
-WLF:	58☆7	52☆13	50☆14					-128	245
-WLL:	52☆12	39☆11	38☆11	37☆11	36☆11			-96	246
WLLOAD:	52☆4	58☆4						-128	247
WR:	54☆4	58☆9						-144	248
-WR:	53☆6	58☆10	73☆14					-128	249
XC0:	33☆3	41☆12	49☆3					-134	250

XC1:	33*4	41*11	49*4				-134	251
XC2:	33*5	41*10	49*6				-134	252
XC3:	33*6	41*9	49*11				-134	253
XCL:	33*10	42*9	49*13				-134	254
XCLOCK:	49*12	42*4	35*2	34*2	41*4	43*15	-80	255
-XCLOCK:	43*14	45*5	46*13				-128	256
XD:	33*9	42*10	49*14				-134	257
XDATA:	75*1	41*6	49*15	42*6			-112	258
-XDATA:	84*10	69*4	69*3	75*3	E75		-480	259
XXX001:	12*3	6*2					-97	260
XXX002:	12*2	6*4					-97	261
XXX003:	12*1	6*6					-97	262
XXX004:	12*4	6*9					-97	263
XXX005:	7*2	14*3	13*3				-94	264
XXX006:	7*4	14*2	13*2				-94	265
XXX007:	7*6	14*1	13*1				-94	266
XXX008:	7*9	14*4	13*4				-94	267
XXX009:	33*13	55*11	55*5				32	268
XXX010:	26*15	74*10					-144	269
XXX011:	26*11	26*13					-144	270
XXX012:	26*12	53*1					-144	271
XXX013:	24*2	27*6					-184	272
XXX014:	26*1	28*3					-144	273
XXX015:	25*4	26*3					-144	274
XXX016:	46*1	50*13					-144	275
XXX017:	55*2	56*6					-144	276
XXX018:	70*15	77*14					0	277
XXX019:	77*15	70*2	70*1				0	278
XXX020:	70*11	77*6					0	279
XXX021:	77*7	70*6	70*5				0	280
XXX022:	70*13	76*14					0	281
XXX023:	76*15	70*3	70*4				0	282
XXX024:	62*5	60*15					-64	283

XXX025:	62☆1	61☆13	61☆14	-128	284
XXX026:	62☆4	60☆11	59☆11	-128	285
XXX027:	68☆13	54☆10		-144	286
XXX028:	64☆14	68☆12		-144	287
XXX029:	64☆2	73☆3		-144	288
XXX030:	64☆3	51☆3		-144	289
XXX031:	58☆13	51☆6		-144	290
XXX032:	58☆1	50☆10		-112	291
XXX033:	20☆10	52☆14	52☆2	-168	292
XXX034:	52☆6	20☆13		-184	293
XXX035:	57☆14	57☆6		-144	294
XXX036:	22☆14	15☆2	16☆15	-128	295
XXX037:	22☆13	15☆5	16☆1	-128	296
XXX038:	15☆11	22☆12	16☆2	-128	297
XXX039:	15☆14	22☆11	16☆3	-128	298
XXX040:	23☆14	16☆4	15☆3	-128	299
XXX041:	15☆6	23☆13	16☆7	-128	300
XXX042:	23☆12	16☆6	15☆10	-128	301
XXX043:	23☆11	16☆5	15☆13	-128	302
XXX044:	29☆4	36☆15		-157	303
XXX045:	29☆6	36☆14		-157	304
XXX046:	29☆10	36☆13		-157	305
XXX047:	29☆12	36☆12		-157	306
XXX048:	30☆4	37☆15		-157	307
XXX049:	30☆6	37☆14		-157	308
XXX050:	30☆10	37☆13		-157	309
XXX051:	30☆12	37☆12		-157	310
XXX052:	31☆4	38☆15		-157	311
XXX053:	31☆6	38☆14		-157	312
XXX054:	31☆10	38☆13		-157	313
XXX055:	31☆12	38☆12		-157	314
XXX056:	32☆4	39☆15		-157	315
XXX057:	32☆6	39☆14		-157	316

XXX058:	32*10	39*13		-157	317
XXX059:	32*12	39*12		-157	318
XXX060:	47*2	62*12		-144	319
XXX061:	24*11	46*10		-144	320
XXX062:	48*14	24*13		-144	321
XXX063:	46*3	25*10		-144	322
XXX064:	46*5	25*13		-144	323
XXX065:	44*13	45*4		-158	324
XXX066:	44*1	45*7		-158	325
XXX067:	44*4	45*9		-158	326
XXX068:	44*12	45*12		-158	327
XXX069:	44*2	44*11		-14	328
XXX070:	47*3	51*13		-144	329
XXX071:	33*7	42*12		-150	330
XXX072:	34*10	35*9		-144	331
XXX073:	53*11	67*6		-144	332
XXX074:	67*14	53*12		-144	333
XXX075:	65*6	65*13	65*14	-128	334
'KDATA:	E111	26*5		16	335

* This card uses 751 wires

E1	OKTORUN	E2	RESET	E18	-SN00	E19	-SN01	E20	-SN02
E21	-SN03	E22	-SN04	E23	-SN05	E24	-SN06	E25	-SN07
E30	F1(0)	E31	F1(1)	E32	F1(2)	E33	F1(3)	E36	F2(0)
E37	F2(1)	E38	F2(2)	E39	F2(3)	E41	-SIO	E42	-RSN
E43	-EM15	E44	-EM14	E46	-EM13	E47	-EM12	E48	-EM11
E49	-EM10	E62	-SRESET	E63	DBARC	E68	-SWAKMRT	E72	AUSYSCLK
E73	TRDATA	E74	TROTHER	E75	-XDATA	E80	BUS00	E81	BUS01
E82	BUS02	E83	BUS03	E84	BUS04	E85	BUS05	E86	BUS06
E87	BUS07	E88	BUS08	E89	BUS09	E90	BUS10	E91	BUS11
E92	BUS12	E93	BUS13	E94	BUS14	E95	BUS15	E99	EMACT
E100	-ETAC	E103	-WAKEET	E106	-NEXT06	E107	-NEXT07	E111	'KDATA
E112	INON	E113	IBUSY	E114	OBUSY	E115	OUTON	1☆1	-IM00
1☆2	EILDFCT	1☆3	BUS00	1☆4	-IM01	1☆5	EILDFCT	1☆6	BUS01
1☆7	GND038	1☆8	GND038	1☆10	BUS02	1☆11	-IM02	1☆12	EILDFCT
1☆13	BUS03	1☆14	-IM03	1☆15	EILDFCT	2☆1	-IM04	2☆2	EILDFCT
2☆3	BUS04	2☆4	-IM05	2☆5	EILDFCT	2☆6	BUS05	2☆7	GND010
2☆10	BUS06	2☆11	-IM06	2☆12	EILDFCT	2☆13	BUS07	2☆14	-IM07
2☆15	EILDFCT	3☆1	-IM08	3☆2	EILDFCT1	3☆3	BUS08	3☆4	-IM09
3☆5	EILDFCT1	3☆6	BUS09	3☆7	GND037	3☆8	GND037	3☆10	BUS10
3☆11	-IM10	3☆12	EILDFCT1	3☆13	BUS11	3☆14	-IM11	3☆15	EILDFCT1
4☆1	-IM12	4☆2	EILDFCT1	4☆3	BUS12	4☆4	-IM13	4☆5	EILDFCT1
4☆6	BUS13	4☆7	GND034	4☆10	BUS14	4☆11	-IM14	4☆12	EILDFCT1
4☆13	BUS15	4☆14	-IM15	4☆15	EILDFCT1	5☆1	COLL	5☆2	EBFCT
5☆3	-NEXT06	5☆4	POST	5☆5	EBFCT	5☆6	-NEXT07	5☆7	GND036
5☆8	GND036	5☆10	-NEXT07	5☆11	INEXT07	5☆12	INEXT07	5☆13	-NEXT06
5☆14	INEXT06	5☆15	INEXT06	6☆1	F2(1)	6☆2	XXX001	6☆3	F2(2)
6☆4	XXX002	6☆5	F2(3)	6☆6	XXX003	6☆7	SYSCLK	6☆9	XXX004
6☆10	F2(0)	6☆11	+	6☆12	+	6☆13	+	6☆14	+
6☆15	+	7☆1	F1(1)	7☆2	XXX005	7☆3	F1(2)	7☆4	XXX006
7☆5	F1(3)	7☆6	XXX007	7☆7	SYSCLK	7☆9	XXX008	7☆10	F1(0)
7☆11	+	7☆12	+	7☆13	+	7☆14	+	7☆15	+
8☆1	-SN07	8☆2	RSN	8☆3	BUS15	8☆4	-SN06	8☆5	RSN
8☆6	BUS14	8☆7	GND011	8☆10	BUS13	8☆11	-SN05	8☆12	RSN
8☆13	BUS12	8☆14	-SN04	8☆15	RSN	9☆1	-SN03	9☆2	RSN
9☆3	BUS11	9☆4	-SN02	9☆5	RSN	9☆6	BUS10	9☆7	GND010
9☆8	GND010	9☆10	BUS09	9☆11	-SN01	9☆12	RSN	9☆13	BUS08
9☆14	-SN00	9☆15	RSN	10☆1	IT	10☆2	EPFCT	10☆3	BUS15
10☆4	OCMD	10☆5	EPFCT	10☆6	BUS14	10☆7	GND035	10☆10	BUS13
10☆11	ICMD	10☆12	EPFCT	10☆13	BUS12	10☆14	-CRCZ	10☆15	EPFCT
11☆1	COLL	11☆2	EPFCT	11☆3	BUS11	11☆4	IDL	11☆5	EPFCT
11☆6	BUS10	11☆7	GND034	11☆8	GND034	11☆10	-SRESET	11☆11	SIOCLK
11☆12	BUS00	11☆13	-INEXT07	11☆14	ECBFCT	11☆15	IOR	12☆1	XXX003
12☆2	XXX002	12☆3	XXX001	12☆4	XXX004	12☆5	-ETAC	12☆6	ONE
12☆7	-EODFCT	12☆9	-EOSFCT	12☆10	-ERBFCT	12☆11	-EEFCT	12☆12	-EBFCT
12☆13	-ECBFCT	12☆14	-EISFCT	12☆15	+	13☆1	XXX007	13☆2	XXX006
13☆3	XXX005	13☆4	XXX008	13☆5	-ETAC	13☆6	ONE	13☆7	+
13☆9	+	13☆10	+	13☆11	-EILFCT	13☆12	-EPFCT	13☆13	-EWFCT
13☆15	+	14☆1	XXX007	14☆2	XXX006	14☆3	XXX005	14☆4	XXX008
14☆5	GND003	14☆6	EMACT	14☆7	-EM10	14☆8	GND003	14☆9	-EM11
14☆10	-EM12	14☆11	-EM13	14☆12	-EM14	14☆13	-EM15	14☆14	-RSN
14☆15	-SIO	15☆1	-RW	15☆2	XXX036	15☆3	XXX040	15☆4	MA0
15☆5	XXX037	15☆6	XXX041	15☆7	MA1	15☆8	GND011	15☆9	MA2
15☆10	XXX042	15☆11	XXX038	15☆12	MA3	15☆13	XXX043	15☆14	XXX039
15☆15	GND011	16☆1	XXX037	16☆2	XXX038	16☆3	XXX039	16☆4	XXX040
16☆5	XXX043	16☆6	XXX042	16☆7	XXX041	16☆9	-BF	16☆10	-BNNE
16☆11	-BNE	16☆12	-BE	16☆13	GND010	16☆14	GND010	16☆15	XXX036
17☆1	-SN07	17☆2	-SN06	17☆3	-SN05	17☆4	-SN04	17☆5	-SN03
17☆6	-SN02	17☆7	-SN01	17☆8	GND035	17☆9	-SN00	17☆10	-BE
17☆11	-BNE	17☆12	-BNNE	17☆13	-BF	18☆1	-POST	18☆2	POST
18☆3	-EBFCT	18☆4	EBFCT	18☆5	-SIO	18☆6	SIO	18☆7	GND032
18☆10	ERBFCT	18☆11	-ERBFCT	18☆12	RSN	18☆13	-RSN	18☆14	EPFCT
18☆15	-EPFCT	19☆1	-ERESET	19☆2	BUS15	19☆3	ONE	19☆4	-SIOCLK
19☆5	ONE	19☆6	OCMD	19☆7	-OCMD	19☆9	-ICMD	19☆10	ICMD
19☆11	ONE	19☆12	-SIOCLK	19☆13	ONE	19☆14	BUS14	19☆15	-ERESET
20☆1	AUSYSCLK	20☆2	OKTORUN	20☆3	-SYSCLK	20☆4	SYSCLK	20☆5	SIO

20☆6	-SIOCLK	20☆7	GND019	20☆10	XXX033	20☆11	SYSCLK	20☆12	EODFCT
20☆13	XXX034	20☆14	SYSCLK	20☆15	EIDFCT	21☆1	OKTORUN	21☆2	ONE
21☆4	ONE	21☆5	DBARC	21☆6	-ARC	21☆7	GND033	21☆8	GND033
21☆10	-ERESET	21☆11	ERESET	21☆12	ERESET	21☆14	ERESET	21☆15	ERESET
22☆1	BUSY	22☆2	-RDCNT	22☆3	+	22☆4	+	22☆5	+
22☆6	+	22☆7	ONE	22☆9	ONE	22☆10	ONE	22☆11	XXX039
22☆12	XXX038	22☆13	XXX037	22☆14	XXX036	22☆15	+	23☆1	BUSY
23☆2	-WE	23☆3	+	23☆4	+	23☆5	+	23☆6	+
23☆7	ONE	23☆9	ONE	23☆10	ONE	23☆11	XXX043	23☆12	XXX042
23☆13	XXX041	23☆14	XXX040	23☆15	+	24☆1	-IDL	24☆2	XXX013
24☆3	-POST	24☆4	-IDR	24☆5	-ODR	24☆6	-DATA	24☆7	GND012
24☆10	-OUTEND	24☆11	XXX061	24☆12	-ERESET	24☆13	XXX062	24☆14	OSLOAD
24☆15	OBE	25☆1	-IBUSY	25☆2	-OBUSY	25☆3	BUSY	25☆4	XXX015
25☆5	IBUSY	25☆6	-IDR	25☆7	GND032	25☆8	GND032	25☆10	XXX063
25☆11	CRCDATA	25☆12	CRCGO	25☆13	XXX064	25☆14	-CRCGO	25☆15	OSDATA
26☆1	XXX014	26☆2	-BNNE	26☆3	XXX015	26☆4	-ETAC	26☆5	'KDATA
26☆6	-EIDFCT	26☆7	GND017	26☆10	ERESET	26☆11	XXX011	26☆12	XXX012
26☆13	XXX011	26☆14	RESET	26☆15	XXX010	27☆1	-OCMD	27☆2	-ICMD
27☆4	-OUTGONE	27☆5	-INGONE	27☆6	XXX013	27☆7	GND019	27☆8	GND019
27☆10	-WAKEET	27☆11	-POST	27☆12	-DATA	27☆14	-COLL	27☆15	-OCDW
28☆1	-BNE	28☆2	-ETAC	28☆3	XXX014	28☆7	GND018	28☆8	GND018
28☆10	ARC	28☆11	DBARC	28☆12	OKTORUN	28☆13	SYSCLK	28☆14	OKTORUN
28☆15	AUSYSCLK	29☆1	MA0	29☆2	GND013	29☆3	-WE	29☆4	XXX044
29☆5	-IM00	29☆6	XXX045	29☆7	-IM01	29☆8	GND013	29☆9	-IM02
29☆10	XXX046	29☆11	-IM03	29☆12	XXX047	29☆13	MA1	29☆14	MA2
29☆15	MA3	30☆1	MA0	30☆2	GND013	30☆3	-WE	30☆4	XXX048
30☆5	-IM04	30☆6	XXX049	30☆7	-IM05	30☆9	-IM06	30☆10	XXX050
30☆11	-IM07	30☆12	XXX051	30☆13	MA1	30☆14	MA2	30☆15	MA3
31☆1	MA0	31☆2	GND012	31☆3	-WE	31☆4	XXX052	31☆5	-IM08
31☆6	XXX053	31☆7	-IM09	31☆8	GND012	31☆9	-IM10	31☆10	XXX054
31☆11	-IM11	31☆12	XXX055	31☆13	MA1	31☆14	MA2	31☆15	MA3
32☆1	MA0	32☆2	GND012	32☆3	-WE	32☆4	XXX056	32☆5	-IM12
32☆6	XXX057	32☆7	-IM13	32☆9	-IM14	32☆10	XXX058	32☆11	-IM15
32☆12	XXX059	32☆13	MA1	32☆14	MA2	32☆15	MA3	33☆1	-IM14
33☆2	-IM15	33☆3	XC0	33☆4	XC1	33☆5	XC2	33☆6	XC3
33☆7	XXX071	33☆8	GND017	33☆9	XD	33☆10	XCL	33☆11	JUMPER
33☆12	-UOSLOAD	33☆13	XXX009	33☆14	-INEXT06	33☆15	-INEXT07	34☆1	-OSLOAD
34☆2	XCLOCK	34☆3	-IM03	34☆4	-IM02	34☆5	-IM01	34☆6	-IM00
34☆7	OSDATA	34☆9	+	34☆10	XXX072	34☆11	-IM07	34☆12	-IM06
34☆13	-IM05	34☆14	-IM04	34☆15	GND019	35☆1	-OSLOAD	35☆2	XCLOCK
35☆3	-IM11	35☆4	-IM10	35☆5	-IM09	35☆6	-IM08	35☆7	+
35☆8	GND016	35☆9	XXX072	35☆10	GND018	35☆11	-IM15	35☆12	-IM14
35☆13	-IM13	35☆14	-IM12	35☆15	GND019	36☆1	ISR01	36☆2	ISR00
36☆3	BUS00	36☆4	BUS01	36☆5	ISR02	36☆6	ISR03	36☆7	BUS03
36☆9	BUS02	36☆10	IBUSY	36☆11	-WLL	36☆12	XXX047	36☆13	XXX046
36☆14	XXX045	36☆15	XXX044	37☆1	ISR05	37☆2	ISR04	37☆3	BUS04
37☆4	BUS05	37☆5	ISR06	37☆6	ISR07	37☆7	BUS07	37☆8	GND015
37☆9	BUS06	37☆10	IBUSY	37☆11	-WLL	37☆12	XXX051	37☆13	XXX050
37☆14	XXX049	37☆15	XXX048	38☆1	ISR09	38☆2	ISR08	38☆3	BUS08
38☆4	BUS09	38☆5	ISR10	38☆6	ISR11	38☆7	BUS11	38☆9	BUS10
38☆10	IBUSY	38☆11	-WLL	38☆12	XXX055	38☆13	XXX054	38☆14	XXX053
38☆15	XXX052	39☆1	ISR13	39☆2	ISR12	39☆3	BUS12	39☆4	BUS13
39☆5	ISR14	39☆6	ISR15	39☆7	BUS15	39☆9	BUS14	39☆10	IBUSY
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40☆1	-IM00	40☆2	-IM01	40☆3	-IM02	40☆4	-IM03	40☆5	-IM04
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40☆12	-IM10	40☆13	-IM11	40☆14	-IM12	40☆15	-IM13	41☆1	OCNTR2
41☆2	OCNTR1	41☆3	OCNTR0	41☆4	XCLOCK	41☆5	OUTGO	41☆6	XDATA
41☆7	OSDATAG	41☆9	XC3	41☆10	XC2	41☆11	XC1	41☆12	XC0
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42☆3	OCNTR0	42☆4	XCLOCK	42☆5	OUTGO	42☆6	XDATA	42☆7	OSDATAG
42☆9	XCL	42☆10	XD	42☆11	-UOSLOAD	42☆12	XXX071	42☆13	GND016
42☆14	GND016	42☆15	OCNTR3	43☆1	ISRFULL	43☆2	-ISRFULL	43☆3	-EODFCT
43☆4	EODFCT	43☆5	-EILDFCT	43☆6	EILDFCT	43☆7	GND014	43☆8	GND014
43☆10	EILDFCT1	43☆11	-EILDFCT	43☆12	OBE	43☆13	-BE	43☆14	-XCLOCK
43☆15	XCLOCK	44☆1	XXX066	44☆2	XXX069	44☆3	GND014	44☆4	XXX067

44☆5	GND014	44☆6	GND014	44☆7	GND030	44☆10	GND015	44☆11	XXX069
44☆12	XXX068	44☆13	XXX065	44☆14	CRCDATA	44☆15	-CRCZ	45☆1	IBUSY
45☆2	OSDATAG	45☆3	ISR15	45☆4	XXX065	45☆5	-XCLOCK	45☆6	RCLKP
45☆7	XXX066	45☆8	GND009	45☆9	XXX067	45☆10	-INON	45☆11	-OUTON
45☆12	XXX068	45☆13	ONE	45☆14	-CRCGO	45☆15	GND015	46☆1	XXX016
46☆2	-OEOT	46☆3	XXX063	46☆4	OUTRGO	46☆5	XXX064	46☆6	OSDATAG
46☆7	GND029	46☆10	XXX061	46☆11	-OUTON	46☆12	TCLK	46☆13	-XCLOCK
46☆14	-ODR	46☆15	OBUSY	47☆1	-PESTOP	47☆2	XXX060	47☆3	XXX070
47☆4	-TCLK	47☆5	ONE	47☆6	OUTON	47☆7	-OUTON	47☆9	+
47☆10	OUTGO	47☆11	ONE	47☆12	-TCLK	47☆13	ONE	47☆14	OUTON
47☆15	-OUTEND	48☆1	-OUTEND	48☆2	OUTGO	48☆3	OUTGO	48☆4	-TCLK
48☆5	ONE	48☆6	OUTRGO	48☆7	+	48☆9	-CRCGO	48☆10	CRCGO
48☆11	ONE	48☆12	-TCLK	48☆13	ONE	48☆14	XXX062	48☆15	-OUTEND
49☆1	-OUTEND	49☆2	OCNTR0	49☆3	XC0	49☆4	XC1	49☆5	OCNTR1
49☆6	XC2	49☆7	OCNTR2	49☆9	-TCLK	49☆10	OCNTR3	49☆11	XC3
49☆12	XCLOCK	49☆13	XCL	49☆14	XD	49☆15	XDATA	50☆1	OBUSY
50☆2	-OUTGONE	50☆3	-PESTOP	50☆4	INGONE	50☆5	-ISRFULL	50☆6	IT
50☆7	GND031	50☆10	XXX032	50☆11	BUSY	50☆12	-WE	50☆13	XXX016
50☆14	-WLF	50☆15	-BF	51☆1	-IMIP	51☆2	ILOC	51☆3	XXX030
51☆4	WLF	51☆5	-BF	51☆6	XXX031	51☆7	GND030	51☆8	GND030
51☆10	EILDFCT	51☆11	-EIDFCT	51☆12	-EILFCT	51☆13	XXX070	51☆14	CRCGO
51☆15	OSLOAD	52☆1	IBUSY	52☆2	XXX033	52☆3	ISRFULL	52☆4	WLLOAD
52☆5	-OSLOAD	52☆6	XXX034	52☆7	-RDCNT	52☆9	RR	52☆10	EILDFCT
52☆11	OSLOAD	52☆12	-WLL	52☆13	-WLF	52☆14	XXX033	52☆15	GND009
53☆1	XXX012	53☆2	-SYSCLK	53☆3	-EPFCT	53☆4	-RW	53☆5	RR
53☆6	-WR	53☆7	GND029	53☆8	GND029	53☆10	-SWAKMRT	53☆11	XXX073
53☆12	XXX074	54☆1	OBUSY	54☆2	-CARRIER	54☆3	ARC	54☆4	WR
54☆5	-RW	54☆6	-WE	54☆7	GND022	54☆10	XXX027	54☆11	IMIP
54☆12	CRCONLY	54☆13	ILOC	54☆14	-OOK	54☆15	-OTHER	55☆1	RDATA
55☆2	XXX017	55☆3	TRANS	55☆4	-INEXT07	55☆5	XXX009	55☆6	INEXT07
55☆7	GND028	55☆8	GND028	55☆10	INEXT06	55☆11	XXX009	55☆12	-INEXT06
56☆1	-ERESET	56☆2	RDATA	56☆3	RDATA	56☆4	TRANS	56☆5	ONE
56☆6	XXX017	56☆7	+	56☆8	GND004	56☆9	OSLOAD	56☆10	-OSLOAD
56☆11	ONE	56☆12	-TCLK	56☆13	-UOSLOAD	56☆14	-UOSLOAD	56☆15	ONE
57☆1	-ERESET	57☆2	WLF	57☆3	ONE	57☆4	ISRFULL	57☆5	ONE
57☆6	XXX035	57☆7	+	57☆8	GND031	57☆9	-IDL	57☆10	IDL
57☆11	ONE	57☆12	-ARC	57☆13	ONE	57☆14	XXX035	57☆15	-ERESET
58☆1	XXX032	58☆2	ONE	58☆3	ONE	58☆4	WLLOAD	58☆5	ONE
58☆6	WLF	58☆7	-WLF	58☆9	WR	58☆10	-WR	58☆11	BUSY
58☆12	-ARC	58☆13	XXX031	58☆14	-RW	58☆15	ONE	59☆1	ISR14
59☆2	ISR14	59☆3	ISR13	59☆4	ISR12	59☆5	ISR11	59☆6	ISR10
59☆7	GND027	59☆8	GND027	59☆10	RCLK	59☆11	XXX026	59☆12	ISR09
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61☆5	ONE	61☆6	ISR15	61☆7	+	61☆8	GND022	61☆9	ISR14
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62☆5	XXX024	62☆6	-INON	62☆7	GND008	62☆10	-FEOT	62☆11	-OOK
62☆12	XXX060	63☆1	ONE	63☆2	GND005	63☆3	-EISFCT	63☆4	-SYSCLK
63☆5	-ERESET	63☆6	-IBUSY	63☆7	IBUSY	63☆8	GND005	63☆9	OBUSY
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64☆5	ONE	64☆6	INON	64☆7	-INON	64☆9	-INGONE	64☆10	INGONE
64☆11	ONE	64☆12	-ARC	64☆13	ONE	64☆14	XXX028	64☆15	-ERESET
65☆1	OBUSY	65☆2	OUTON	65☆3	ONE	65☆4	OTHER	65☆5	ONE
65☆6	XXX075	65☆7	+	65☆8	GND021	65☆9	-COLL	65☆10	COLL
65☆11	ONE	65☆12	-ARC	65☆13	XXX075	65☆14	XXX075	65☆15	OBUSY
66☆1	ONE	66☆2	GND021	66☆3	-EEFCT	66☆4	-SYSCLK	66☆5	-ERESET
66☆6	-OEOT	66☆7	+	66☆9	-OUTGONE	66☆10	+	66☆11	ONE
66☆12	-OUTON	66☆13	ONE	66☆14	ONE	66☆15	OBUSY	67☆1	ONE
67☆2	OCDW	67☆3	-EWFCT	67☆4	-SYSCLK	67☆5	-ERESET	67☆6	XXX073
67☆7	+	67☆8	GND026	67☆9	-OCDW	67☆10	OCDW	67☆11	ONE
67☆12	-ARC	67☆13	-ETAC	67☆14	XXX074	67☆15	-ERESET	68☆1	TRDATA
68☆2	-RDATA	68☆3	-RDATA	68☆4	RDATA	68☆5	TROTHER	68☆6	-OTHER

68☆7	GND006	68☆10	OTHER	68☆11	-OTHER	68☆12	XXX028	68☆13	XXX027
68☆14	EIDFCT	68☆15	-EIDFCT	69☆1	TRDATA	69☆2	GND008	69☆3	-XDATA
69☆4	-XDATA	69☆5	TROTHER	69☆6	TROTHER	69☆7	VCC001	69☆8	GND008
69☆9	JUMPER	69☆10	ONE	69☆11	GND008	69☆12	VCC002	69☆13	GND022
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70☆3	XXX023	70☆4	XXX023	70☆5	XXX021	70☆6	XXX021	70☆7	VCC001
70☆8	GND007	70☆9	-TROUTGO	70☆10	-TROUTGO	70☆11	XXX020	70☆12	VCC001
70☆13	XXX022	70☆14	VCC001	70☆15	XXX018	71☆1	ONE	71☆2	ONE
71☆3	GND020	71☆4	-ARC	71☆5	JUMPER	71☆6	FAST	71☆7	+
71☆8	GND020	72☆1	INON	72☆2	ISR00	72☆3	ONE	72☆4	RCLK
72☆5	ONE	72☆6	IMIP	72☆7	-IMIP	72☆9	-ILOC	72☆10	ILOC
72☆11	ONE	72☆12	-CARRIER	72☆13	ONE	72☆14	ONE	72☆15	INON
73☆1	-CARRIER	73☆2	-OTHER	73☆3	XXX029	73☆4	-OEOT	73☆5	-BF
73☆6	-FEOT	73☆7	GND025	73☆8	GND025	73☆10	TCLK	73☆11	FAST
73☆12	ARC	73☆13	CRCONLY	73☆14	-WR	73☆15	BNE	74☆1	-SIOCLK
74☆2	SIOCLK	74☆3	-ECBFCT	74☆4	ECBFCT	74☆5	-IDR	74☆6	IDR
74☆7	GND024	74☆10	XXX010	74☆11	OKTORUN	74☆12	BNE	74☆13	-BNE
74☆14	-EILDFCT	74☆15	EILDFCT	75☆1	XDATA	75☆2	OUTGO	75☆3	-XDATA
75☆4	OCMD	75☆5	ERBFCT	75☆6	-INEXT07	75☆7	GND006	75☆8	GND006
75☆10	-TROUTGO	75☆11	OUTGO	75☆12	OUTGO	75☆13	-INEXT06	75☆14	ERBFCT
75☆15	ICMD	76☆1	GND006	76☆2	TRANS	76☆3	ONE	76☆4	-CARRIER
76☆13	+	76☆14	XXX022	76☆15	XXX023	77☆1	RCLK	77☆2	TRANS
77☆3	-ILOC	77☆4	+	77☆5	RCLKP	77☆6	XXX020	77☆7	XXX021
77☆9	GND007	77☆10	RCLK	77☆11	ONE	77☆12	+	77☆13	RCLK
77☆14	XXX018	77☆15	XXX019	77☆16	VCC001	78☆1	FAST	78☆2	ARC
78☆3	-TCLK	78☆7	GND023	78☆8	GND023	81☆8	GND024	83☆8	GND002
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84☆6	GND001	84☆7	GND001	84☆8	GND001	84☆9	TRDATA	84☆10	-XDATA
84☆11	TROTHER	84☆12	-TROUTGO						

ETHERNET

PLATFORMS.

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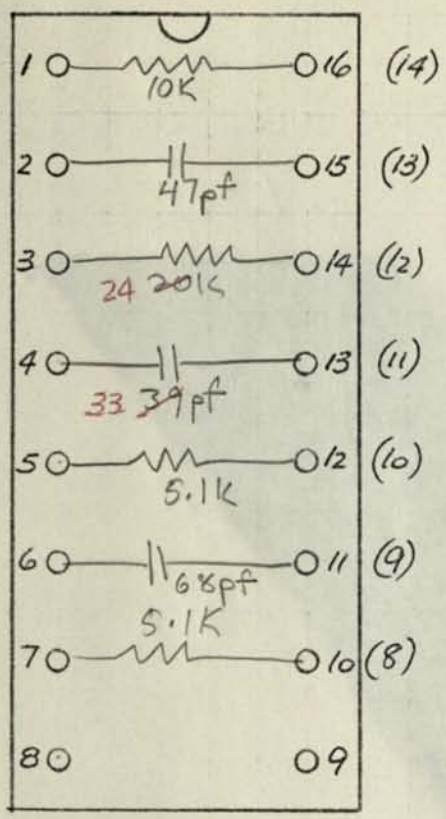

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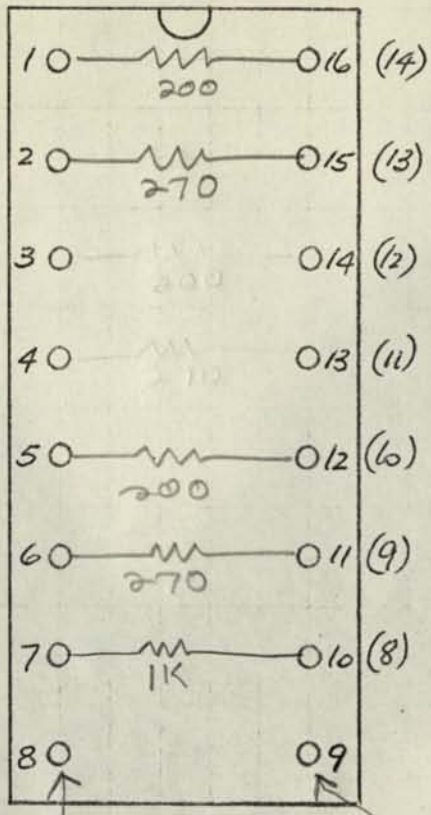

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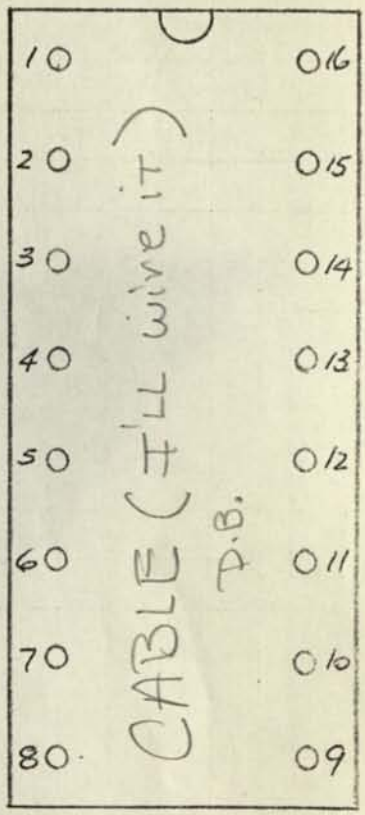
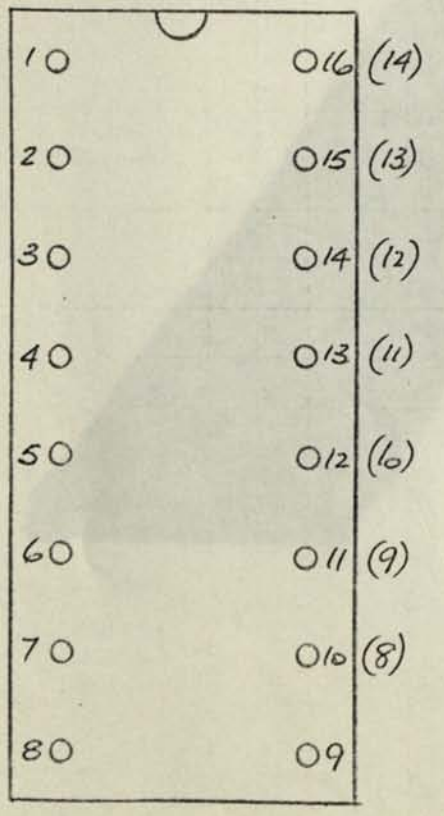
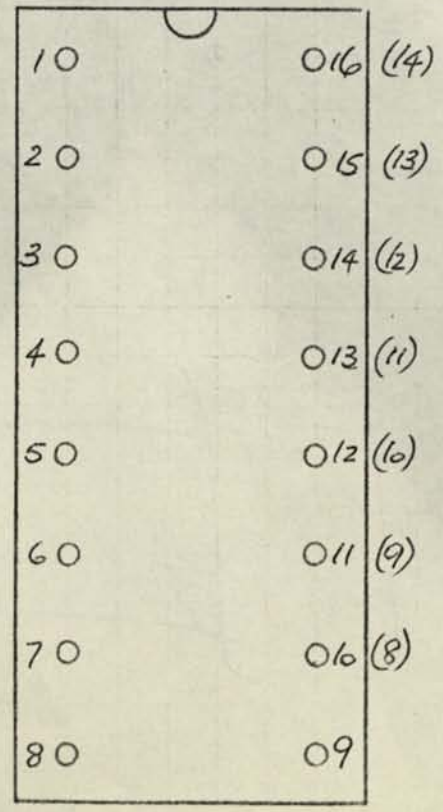
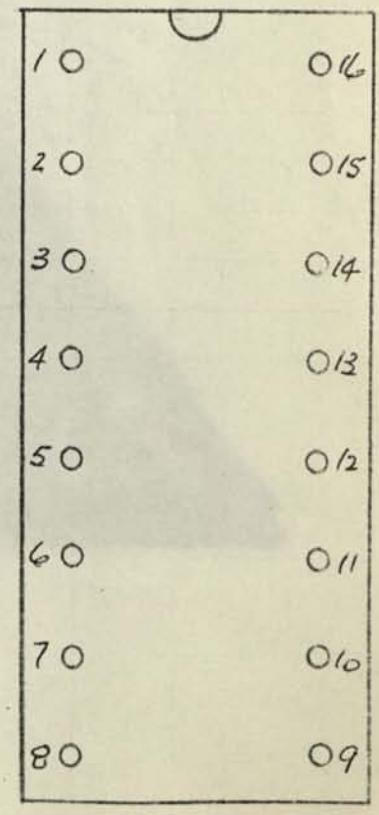








@PARC84

********** ETHERNET 2.0
********** DESIGN BY: D. BOGGS & R. METCALFE
** ALTO ** CARD NAME: ETHER2.0
********** FILE NAME: ETHERNET2.0
********** LAYOUT BY: D. BOGGS

********** UPDATED AFTER PROTOTYPE DEBUGGING 3/31/74

1=1: SN7438
2=2: SN7438
3=3: SN7438
4=4: SN7438
5=5: SN7438
6=6: I3404
7=7: I3404

8=8: SN7438
9=9: SN7438
10=10: SN7438
11=11: SN7438
12=12: I3205
13=13: I3205
14=14: I3205

15=15: SN74157
16=16: MD6300
17=17: B898-84
18=18: SN7404
19=19: SN74109
20=20: SN74S00
21=21: SN74S40

22=22: SN74161
23=23: SN74161
24=24: SN7408
25=25: SN7400
26=26: SN7432
27=27: SN74H21
28=28: SN7408

29=29: I3101A
30=30: I3101A
31=31: I3101A
32=32: I3101A
33=33: B898-84
34=34: SN74165
35=35: SN74165

36=36: SN74298
37=37: SN74298
38=38: SN74298
39=39: SN74298
40=40: B898-84
41=41: MD6300
42=42: MD6300

43=43: SN7404
44=44: MC8503
45=45: SN74157
46=46: SN7410
47=47: SN74109
48=48: SN74109
49=49: SN74174

```
50=50: SN7408
51=51: SN7400
52=52: SN74157
53=53: SN7402
54=54: SN7410
55=55: SN7486
56=56: SN74109

57=57: SN74109
58=58: SN74109
59=59: SN74164
60=60: SN74164
61=61: SN74109
62=62: SN7402
63=63: SN74109

64=64: SN74109
65=65: SN74109
66=66: SN74109
67=67: SN74109
68=68: SN7404
69=69: PLT84
70=70: PLT84

71=71: SN74109
72=72: SN74109
73=73: SN7408
74=74: SN7404
75=75: SN7438
76=76: SN74123
77=77: SN74123

78=78: SN74S00

84=84: PLT84

@

*** EDGE PINS **

OKTORUN: E1
RESET: E2

SRESET': E62
SWAKMRT': E68

SN00': E18
SN01': E19
SN02': E20
SN03': E21
SN04': E22
SN05': E23
SN06': E24
SN07': E25

F1(0): E30
F1(1): E31
F1(2): E32
F1(3): E33

F2(0): E36
F2(1): E37
F2(2): E38
F2(3): E39
```

```
SIO': E41
RSN': E42
EM15': E43
EM14': E44
EM13': E46
EM12': E47
EM11': E48
EM10': E49

AUSYSCLK: E72
DBARC: E63

XDATA': E75
TRDATA: E73
TROTHER: E74


BUS00: E80
BUS01: E81
BUS02: E82
BUS03: E83
BUS04: E84
BUS05: E85
BUS06: E86
BUS07: E87
BUS08: E88
BUS09: E89
BUS10: E90
BUS11: E91
BUS12: E92
BUS13: E93
BUS14: E94
BUS15: E95

EMACT: E99

ETAC': E100

WAKEET': E103

NEXT06': E106
NEXT07': E107

'KDATA: E111

INON: E112
IBUSY:E113
OBUSY: E114
OUTON: E115


** CABLE CONNECTOR **

GND:84.1,84.2,84.3,84.4,84.5,84.6,84.7
TROUTGO':84.12
TROTHER:84.11
XDATA':84.10
TRDATA:84.9


** COMMAND DECODING **


+:6.12,6.14,6.11,6.13,6.15
+:7.12,7.14,7.11,7.13,7.15
```

```
+:12.15,13.15,13.9,13.10,13.7
ONE:19.5,19.3,19.11,19.13,12.6,13.6
GND:14.5
F2(3):6.5
F2(2):6.3
F2(1):6.1
F2(0):6.10
F1(3):7.5
F1(2):7.3
F1(1):7.1
F1(0):7.10
ETAC':12.5,13.5
SYSCLK:6.7,7.7,20.4
SIO':14.15,18.5
RSN':14.14
EM15':14.13
EM14':14.12
EM13':14.11
EM12':14.10
EM11':14.9
EM10':14.7
EMACT:14.6
EWFCT':13.13
EEFCT':12.11
EBFCT':12.12
EOSFCT':12.9
EODFCT':12.7
EPFCT':13.12
EILFCT':13.11
ECBFCT':12.13
ERBFCT':12.10
EISFCT':12.14
:6.2,12.3
:6.4,12.2
:6.6,12.1
:6.9,12.4
:7.2,13.3,14.3
:7.4,13.2,14.2
:7.6,13.1,14.1
:7.9,13.4,14.4
SIO:18.6,20.5
SIOCLK':20.6,19.12,19.4,74.1
SIOCLK:74.2
BUS15:19.2
BUS14:19.14
ERESET':19.15,19.1
OCMD:19.6
OCMD':19.7
ICMD:19.10
ICMD':19.9

** BRANCH LOGIC **

SIOCLK:11.9
BUS00:11.10
SRESET':11.8

ERBFCT':18.9
ERBFCT:18.8,75.5,75.12
OCMD:75.4
ICMD:75.13

IDR':74.5
IDR:74.6,11.13
```

```
ECBFCT':74.3
ECBFCT:74.4,11.12

INEXT07':11.11,75.6,55.4,33.15
INEXT06':75.11,55.10,33.14

:33.13,55.9,55.5

INEXT07:55.6,5.9,5.10
INEXT06:55.8,5.12,5.13

NEXT06':5.11
NEXT07':5.8

ETAC':26.4
'KDATA:26.5
EIDFCT':26.6


☆☆  ALTO INTERFACE  ☆☆


GND: 63.2,63.14
ONE: 63.1,63.15
ERESET': 21.8,63.5,63.11
SYSCLK': 20.3,63.4,63.12,53.2
SYSCLK: 28.11
ARC': 21.6
ARC: 28.8
AUSYSCLK: 20.1,28.13
DBARC: 21.5,28.9
ONE:21.2,21.4
OKTORUN: 21.1,28.12,20.2,74.9,28.10
:74.8,26.13
:26.11,26.9
RESET: 26.12
EPFCT': 53.3
:53.1,26.10
ERESET: 26.8,21.9,21.10,21.12,21.13
EISFCT': 63.3
EOSFCT': 63.13
IBUSY': 63.6,25.1
IBUSY: 63.7,25.5
OBUSY': 63.10,25.2
OBUSY: 63.9,46.13
BUSY: 25.3
OCMD': 27.1
ICMD': 27.2
OUTGONE': 27.4
INGONE': 27.5
IDL': 24.1
:27.6,24.2
POST':24.3,18.1,27.9
POST: 18.2,5.4
EBFCT': 18.3
EBFCT: 18.4,5.5,5.2
COLL: 5.1
NEXT06': 5.3
NEXT07': 5.6
DATA': 27.10,24.6
COLL': 27.12
OCDW': 27.13
WAKEET': 27.8
BNE': 28.1
ETAC':28.2
BNNE': 26.2
```

```
:28.3,26.1
:26.3,25.4
:50.11,46.1
WLF':50.12
BF':50.13
OEOT': 46.2
IDR':25.6,24.4
ODR':46.12,24.5

** SERIAL NUMBER AND STATUS **

RSN':18.11
RSN:18.10,9.13,9.10,9.5,9.2,8.13,8.10,8.5,8.2
SN07':17.1,8.1
SN06':17.2,8.4
SN05':17.3,8.9
SN04':17.4,8.12
SN03':17.5,9.1
SN02':17.6,9.4
SN01':17.7,9.9
SN00':17.9,9.12
EPFCT':18.13
EPFCT:18.12,11.5,11.2,10.13,10.10,10.5,10.2
IT:10.1
OCMD:10.4
ICMD:10.9
CRCZ':10.12
COLL:11.1
IDL:11.4
BUS15:8.3,10.3
BUS14:8.6,10.6
BUS13:8.8,10.8
BUS12:8.11,10.11
BUS11:9.3,11.3
BUS10:9.6,11.6
BUS09:9.8
BUS08:9.11

** PHASE DECODER **

ONE:56.5,77.11,76.3
VCC:70.12,70.14
+:77.12,56.7
GND:77.9,76.1
RDATA:56.2,56.3,55.1
:56.6,55.2
ERESET':56.1
TRANS:55.3,56.4,77.2,76.2
ILOC':77.3
+:77.4
RCLK:77.1,77.13,77.10
:77.14,70.15
:77.15,70.2,70.1
RCLKP:77.5
:77.6,70.11
:77.7,70.6,70.5
+:76.13
CARRIER':76.4
:76.14,70.13
:76.15,70.4,70.3
```

** INPUT SHIFT REGISTER **

```
+:61.7,61.10
ONE:61.5,61.15
INON:61.11,61.1
INON':62.6
RDATA:61.2,61.3
RCLK:61.4,61.12,59.8,60.8
ISRFULL:60.12,43.1,62.2
ISRFULL':43.2
:60.13,62.5
:62.1,61.14,61.13
:62.4,60.9,59.9
ISR15:61.6,62.3
ISR14:61.9,59.1,59.2
ISR13:59.3
ISR12:59.4
ISR11:59.5
ISR10:59.6
ISR09:59.10
ISR08:59.11
ISR07:59.12
ISR06:59.13,60.1,60.2
ISR05:60.3
ISR04:60.4
ISR03:60.5
ISR02:60.6
ISR01:60.10
ISR00:60.11
```

** INPUT STUFF **

```
ONE:64.5,72.5,72.3,72.11,72.13,64.11,64.13,72.14
GND:69.2
CARRIER':73.1,72.12
OTHER':73.2
ARC':64.4,64.12
IMIP':51.1,72.7
CRCONLY:54.10,73.11
ILOC:51.2,72.10,54.11
IBUSY:64.1
INON:64.6,72.1,72.15
INON':64.7
ISR00:72.2
RCLK:72.4
IMIP:72.6,54.9
ILOC':72.9
TRDATA:68.1,69.1,69.15
RDATA':68.2,68.3
RDATA:68.4
ERESET':64.15
ISRFULL':50.5
:54.8,68.11
:68.10,64.14
INGONE:64.10,50.4
IT:50.6
INGONE':64.9
:73.3,64.2
:51.3,64.3
WR':73.12
BNE':74.11
BNE:74.10,73.13
```

☆☆ BUFFER CONTROL ☆☆

```
+:57.7
ONE:58.5,58.2,58.3,58.15,57.5,57.3,57.11,57.13
GND:52.15
BF':51.5
WLF:51.4,58.6,57.2
WLF':58.7,52.13
WLLOAD:58.4,52.4
ARC':58.12,57.12
:51.6,58.13
BUSY:58.11,50.9
RW':58.14,53.4,54.5
RR:53.5,52.9
WR':53.6,58.10
WR:58.9,54.4
ARC:54.3
WE':54.6,50.10
:50.8,58.1
SYSCLK:20.9,20.12
EODFCT':43.3
EODFCT:43.4,20.10
:20.8,52.2,52.14
OSLOAD':52.5
OSLOAD:52.11
:20.11,52.6
EIDFCT:20.13,68.12
EIDFCT':51.9,68.13
EILFCT':51.10
EILDFCT:51.8,52.10,74.13
EILDFCT':74.12
IBUSY:52.1
RDCNT':52.7
WLL':52.12
ISRFULL:57.4,52.3
ERESET':57.1,57.15
:57.6,57.14
IDL:57.10
IDL':57.9
```

☆☆ HALF DUPLEX RAM BUFFER ☆☆

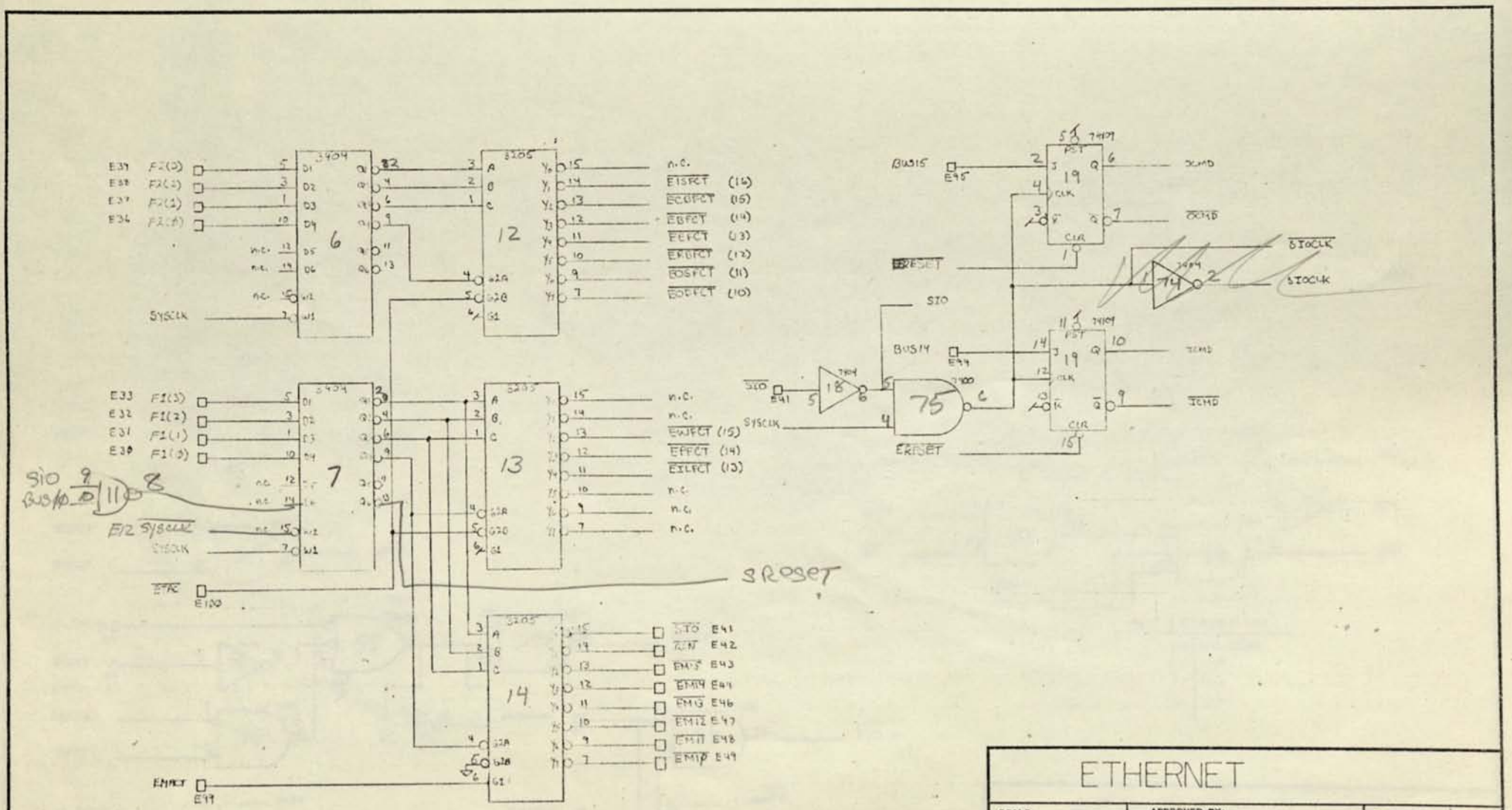
```
+:22.3,22.4,22.5,22.6,23.3,23.4,23.5,23.6,22.15,23.15
ONE:22.7,23.7,22.10,23.10,22.9,23.9
GND:29.2,30.2,31.2,32.2,15.15,16.13,16.14
IBUSY:36.10,37.10,38.10,39.10
WLL':36.11,37.11,38.11,39.11
WE':29.3,30.3,31.3,32.3,23.2
RDCNT':22.2
BUSY:22.1,23.1
RW':15.1
:22.14,15.2,16.15
:22.13,15.5,16.1
:22.12,15.11,16.2
:22.11,15.14,16.3
:23.14,15.3,16.4
:23.13,15.6,16.7
:23.12,15.10,16.6
:23.11,15.13,16.5
MA0:15.4,29.1,30.1,31.1,32.1
MA1:15.7,29.13,30.13,31.13,32.13
MA2:15.9,29.14,30.14,31.14,32.14
```

```
MA3:15.12,29.15,30.15,31.15,32.15
BE':16.12,17.10
BNE':16.11,17.11
BNNE':16.10,17.12
BF':16.9,17.13
BUS00:36.3
BUS01:36.4
BUS02:36.9
BUS03:36.7
BUS04:37.3
BUS05:37.4
BUS06:37.9
BUS07:37.7
BUS08:38.3
BUS09:38.4
BUS10:38.9
BUS11:38.7
BUS12:39.3
BUS13:39.4
BUS14:39.9
BUS15:39.7
ISR00:36.2
ISR01:36.1
ISR02:36.5
ISR03:36.6
ISR04:37.2
ISR05:37.1
ISR06:37.5
ISR07:37.6
ISR08:38.2
ISR09:38.1
ISR10:38.5
ISR11:38.6
ISR12:39.2
ISR13:39.1
ISR14:39.5
ISR15:39.6
:36.15,29.4
:36.14,29.6
:36.13,29.10
:36.12,29.12
:37.15,30.4
:37.14,30.6
:37.13,30.10
:37.12,30.12
:38.15,31.4
:38.14,31.6
:38.13,31.10
:38.12,31.12
:39.15,32.4
:39.14,32.6
:39.13,32.10
:39.12,32.12
IM00':29.5,40.1
IM01':29.7,40.2
IM02':29.9,40.3
IM03':29.11,40.4
IM04':30.5,40.5
IM05':30.7,40.6
IM06':30.9,40.7
IM07':30.11,40.9
IM08':31.5,40.10
IM09':31.7,40.11
IM10':31.9,40.12
IM11':31.11,40.13
IM12':32.5,40.14
```

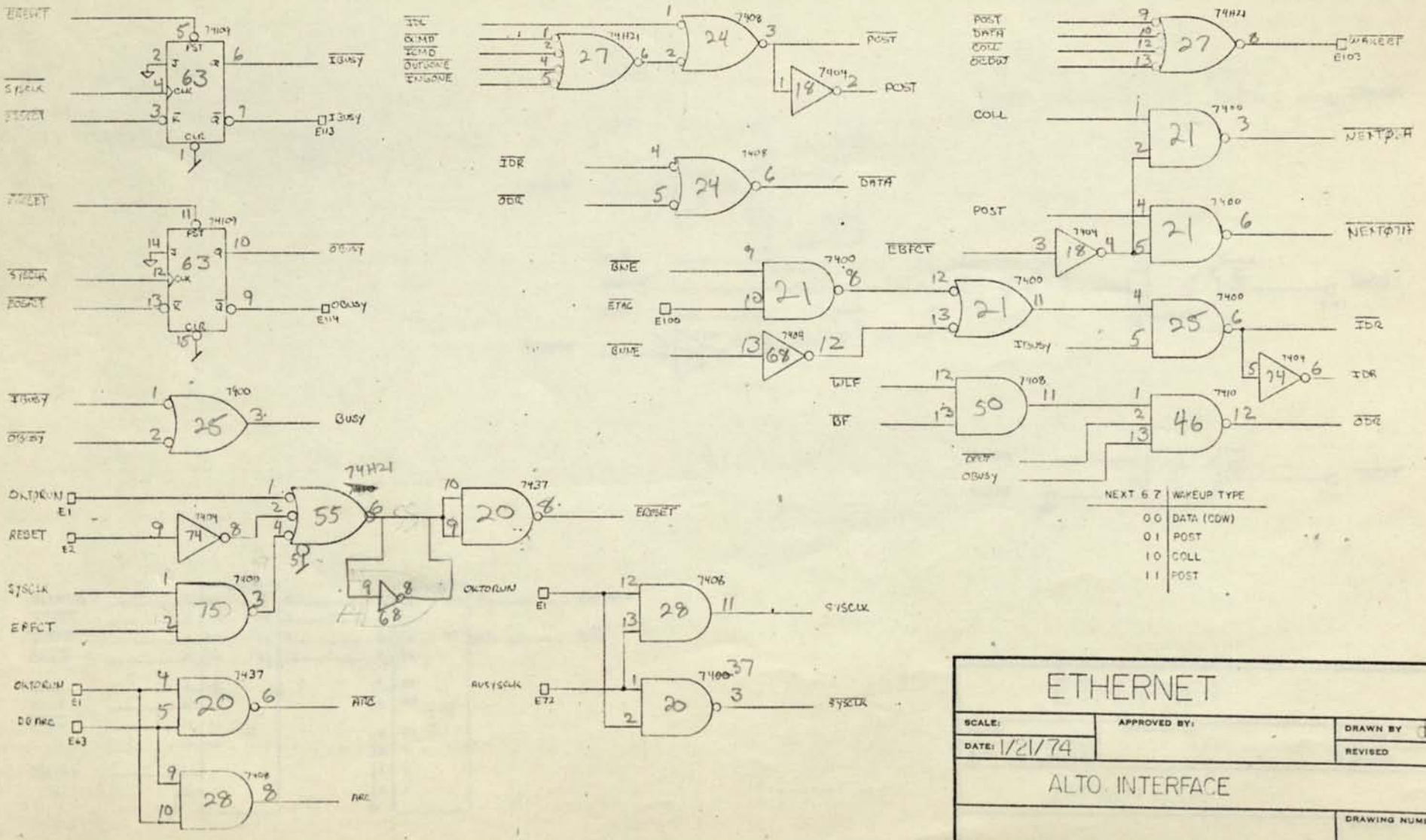
```
IM13':32.7,40.15
IM14':32.9,33.1
IM15':32.11,33.2

** PROCESSOR BUS DRIVERS **

EILDFCT':43.5,43.9
EILDFCT:43.6,2.13,2.10,2.5,2.2,1.13,1.10,1.5,1.2
EILDFCT1:43.8,4.13,4.10,4.5,4.2,3.13,3.10,3.5,3.2
IM00':1.1
IM01':1.4
IM02':1.9
IM03':1.12
IM04':2.1
IM05':2.4
IM06':2.9
IM07':2.12
IM08':3.1
IM09':3.4
IM10':3.9
IM11':3.12
IM12':4.1
IM13':4.4
IM14':4.9
IM15':4.12
BUS00:1.3
BUS01:1.6
BUS02:1.8
BUS03:1.11
BUS04:2.3
BUS05:2.6
BUS06:2.8
BUS07:2.11
BUS08:3.3
BUS09:3.6
BUS10:3.8
BUS11:3.11
BUS12:4.3
BUS13:4.6
BUS14:4.8
BUS15:4.11

** PHASE ENCODER CONTROL & CRC **

+:48.7
ONE:47.5,47.11,47.13,48.5,48.11,48.13,45.13
GND:45.15,44.6,44.8,44.5,44.3
TCLK':47.4,47.12,48.4,48.12
TCLK:46.10
FEOT':62.8
OOK':62.9
:62.10,47.2
OSLOAD:51.13,24.12
CRCGO:51.12,48.10,25.10
PESTOP':47.1
XCLOCK:43.13
ERESET':24.10
XCLOCK':43.12,46.11,45.5
OUTON':47.7,46.9,45.11
:46.8,24.9
OUTEND':24.8,47.15,48.1,48.15
OUTON:47.6,47.14
```

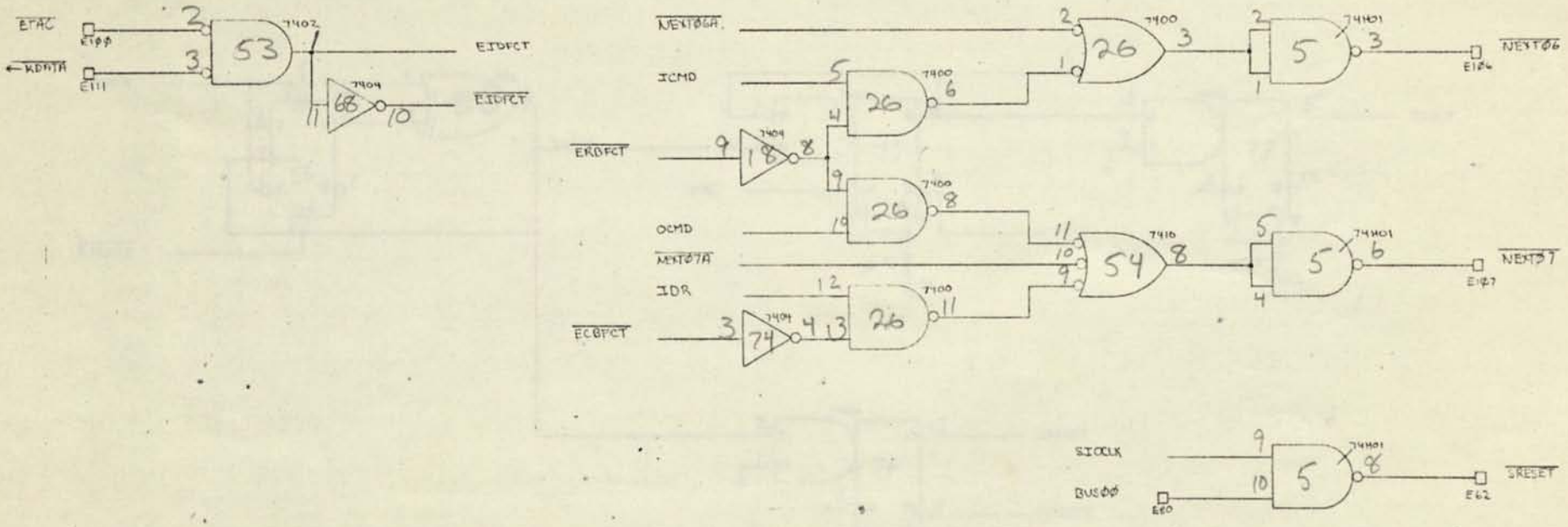
```
+:47.9
OUTGO:47.10,48.2,48.3
OUTRGO:48.6,46.4
BE':43.11
OBE:43.10,24.13
:24.11,48.14
CRCGO':48.9,25.12,45.14
CRCDATA:44.12,25.9
OSDATA:25.13
:25.8,46.3
:25.11,46.5
OSDATAG:46.6,45.2
ISR15:45.3
RCLKP:45.6
INON':45.10
:45.4,44.11
:45.7,44.1
:45.9,44.4
:45.12,44.10
CRCZ':44.13
:44.9,44.2
:51.11,47.3
IBUSY:45.1

** OUTPUT SR & PHASE ENCODER **

GND:35.15,34.15,35.10,41.13,41.14,42.13,42.14
ONE:56.11,56.15
+:35.7
TCLK':56.12,49.9
OUTEND':49.1
OSLOAD:56.9
OUTGO:41.5,42.5
XDATA:41.6,42.6,49.15
OSDATAG:41.7,42.7
OCNTR0:41.3,42.3,49.2
OCNTR1:41.2,42.2,49.5
OCNTR2:41.1,42.1,49.7
OCNTR3:41.15,42.15,49.10
UOSLOAD':42.11,33.12,56.14,56.13
:42.12,33.7
XD:42.10,33.9,49.14
XCL:42.9,33.10,49.13
XC0:41.12,33.3,49.3
XC1:41.11,33.4,49.4
XC2:41.10,33.5,49.6
XC3:41.9,33.6,49.11

IM00':34.6
IM01':34.5
IM02':34.4
IM03':34.3
IM04':34.14
IM05':34.13
IM06':34.12
IM07':34.11
IM08':35.6
IM09':35.5
IM10':35.4
IM11':35.3
IM12':35.14
IM13':35.13
IM14':35.12
```

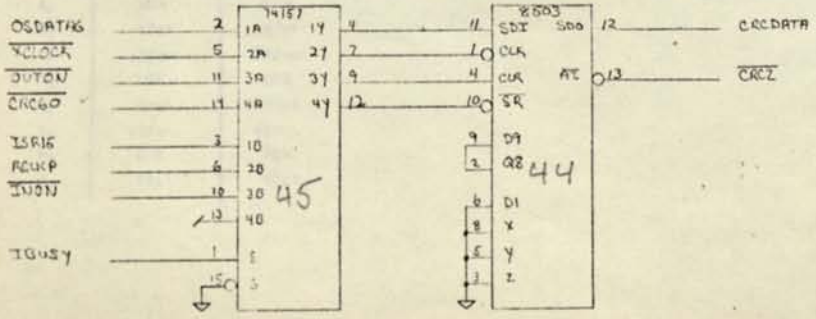
```
IM15':35.11
OSLOAD':34.1,35.1,56.10
XCLOCK:34.2,35.2,41.4,42.4,49.12
:35.9,34.10
+:34.9
OSDATA:34.7

** OUTPUT STUFF **

+:65.7,67.7,71.7
ONE:67.11,67.1,65.5,65.3,65.11,66.1,66.11,66.14,66.13,71.2,71.1,69.10
VCC:69.14,69.12,69.7
GND:69.11,69.13,66.2,71.3
ERESET':67.5,67.15,66.5
OBUSY:66.15
SYSCLK':67.4,66.4
EWFCT':67.3
ARC':67.12,65.12,71.4
ARC:78.2,73.10
ETAC':67.13
:67.6,53.9
:53.10,67.14
OCDW:67.10,67.2
OCDW':67.9
OUTON:65.2
OUTGO:75.2
OTHER:65.4,68.8
SWAKMRT':53.8
OBUSY:65.1,65.15,54.1
:65.6,65.14,65.13
COLL:65.10
COLL':65.9
EEFCT':66.3
OEOT':66.6,73.4
+:66.7
OUTON':66.12
+:66.10
OBUSY:50.1
PESTOP':50.3
OUTGONE':66.9,50.2
BF':73.5
FEOT':73.6
OOK':54.12
CARRIER':54.2
OTHER':54.13,68.6,68.9
TROTHER:68.5,69.5,69.6
XDATA:75.1
XDATA':75.3,69.3,69.4
FAST:71.6,73.9,78.1
TCLK:73.8
TCLK':78.3
JUMPER:71.5,33.11,69.9
TROUTGO':75.8,70.10,70.9
VCC:70.7
OUTGO:75.9,75.10

@
```



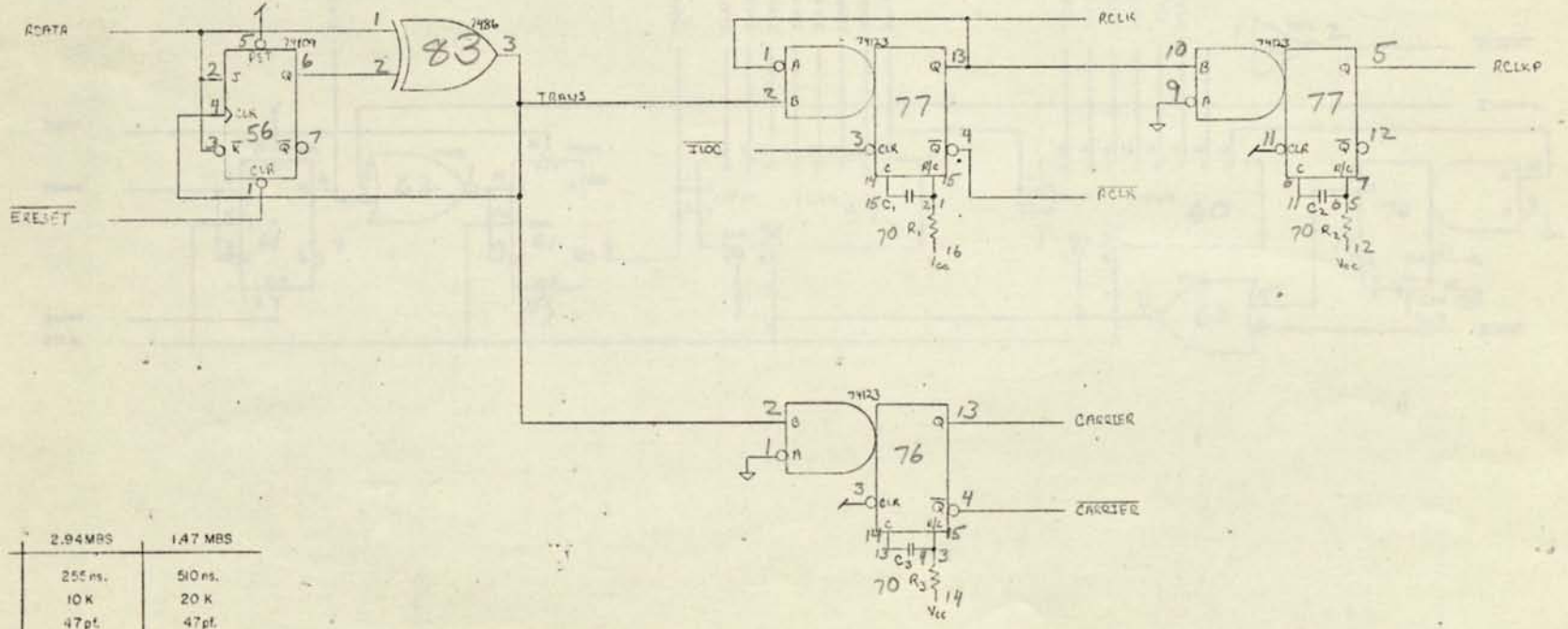
ETHERNET		
SCALE:	APPROVED BY:	DRAWN BY
DATE: 1/13/74		REVISED 3/20/74
COMMAND DECODING		
		DRAWING NUMBER







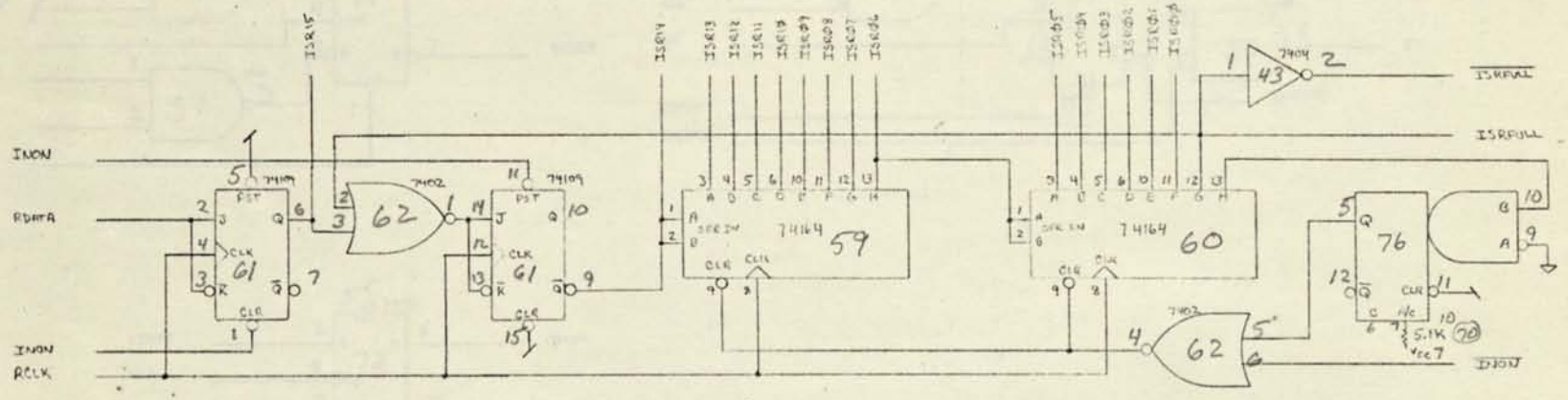
ETHERNET		
SCALE:	APPROVED BY:	DRAWN BY
DATE: 6/20/74		REVISED
BRANCH LOGIC		
		DRAWING NUMBER



	2.94MBS	1.47 MBS
T_1	255 ns.	510 ns.
R_1	10 K	20 K
C_1	47 pf.	47 pf.
T_2	170 ns.	340 ns.
R_2	5K	20K
C_2	68 pf.	33 pf.
T_3	425 ns.	850 ns.
R_3	20K	30K
C_3	39 pf.	62 pf.

ETHERNET

SCALE:	APPROVED BY:	DRAWN BY db
DATE: 1/2/74		REVISED
PHASE DECODER		
		DRAWING NUMBER

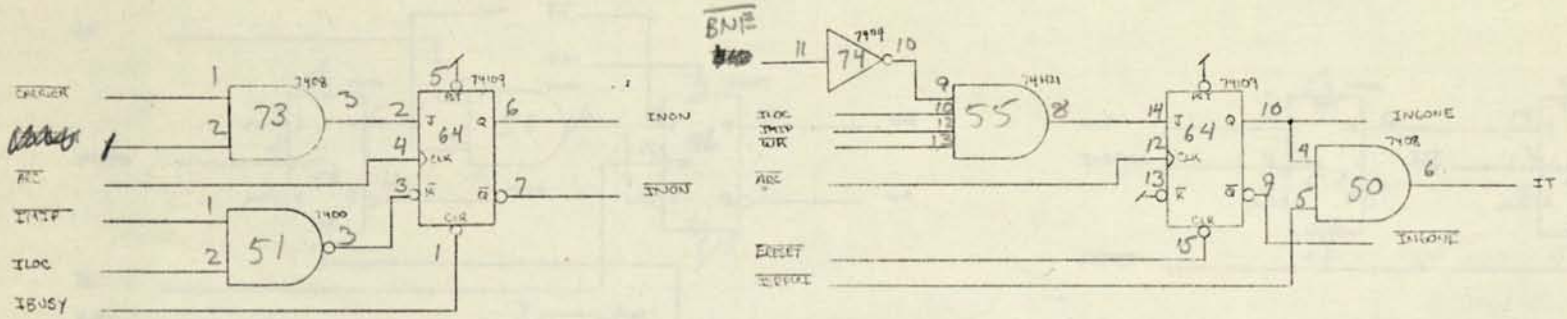


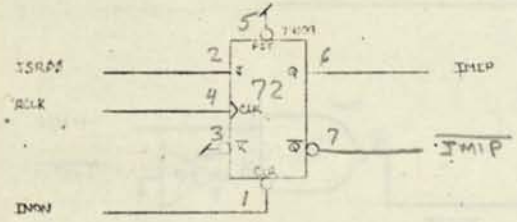
ETHERNET

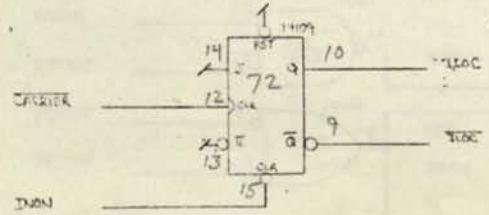
SCALE:	APPROVED BY:	DRAWN BY
DATE: 1/2/74		REVISED 6/7/74

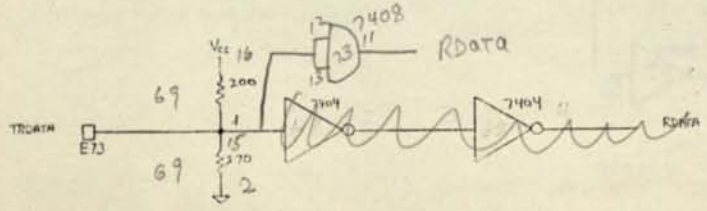
INPUT SHIFT REGISTER

DRAWING NUMBER

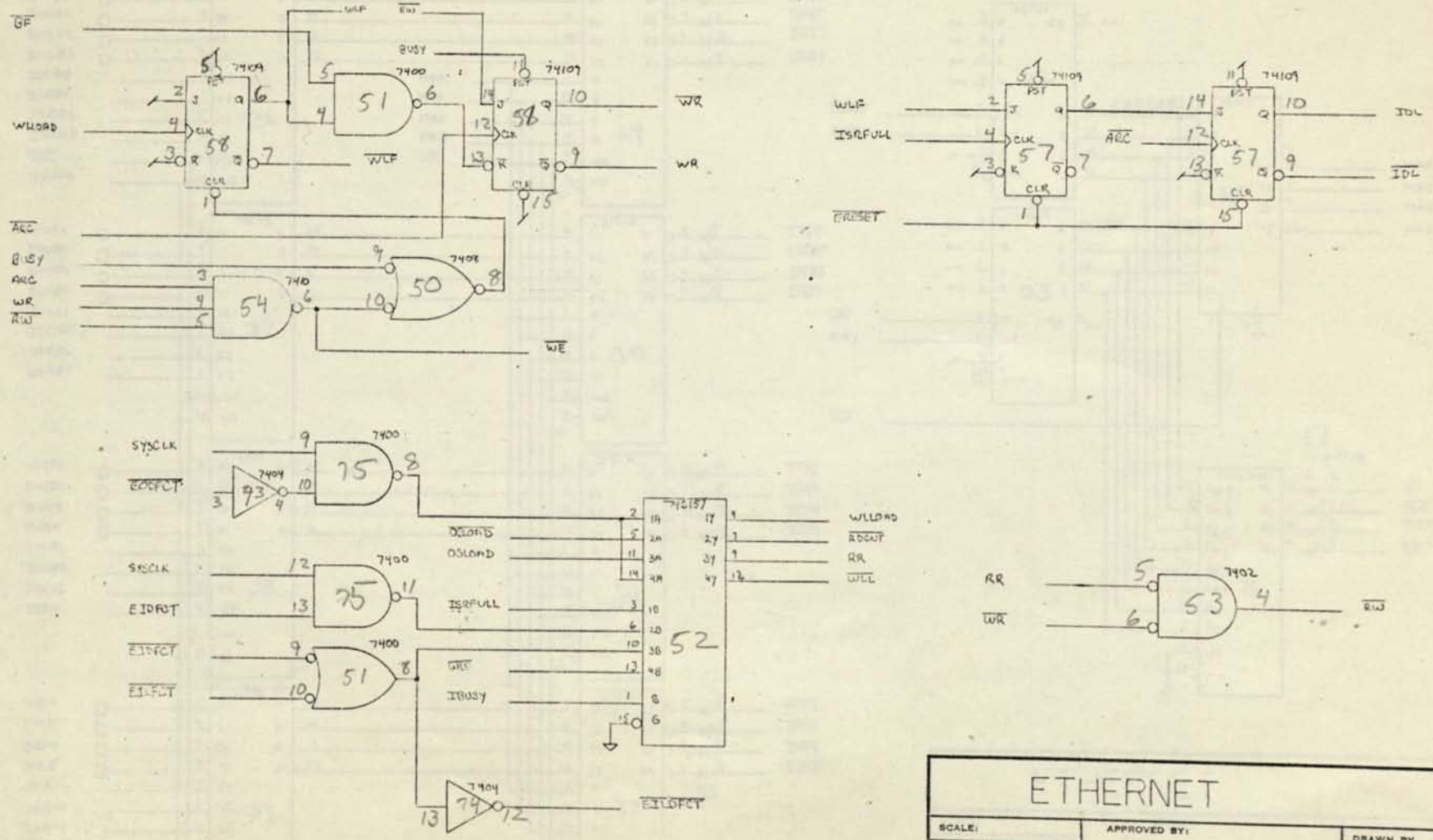




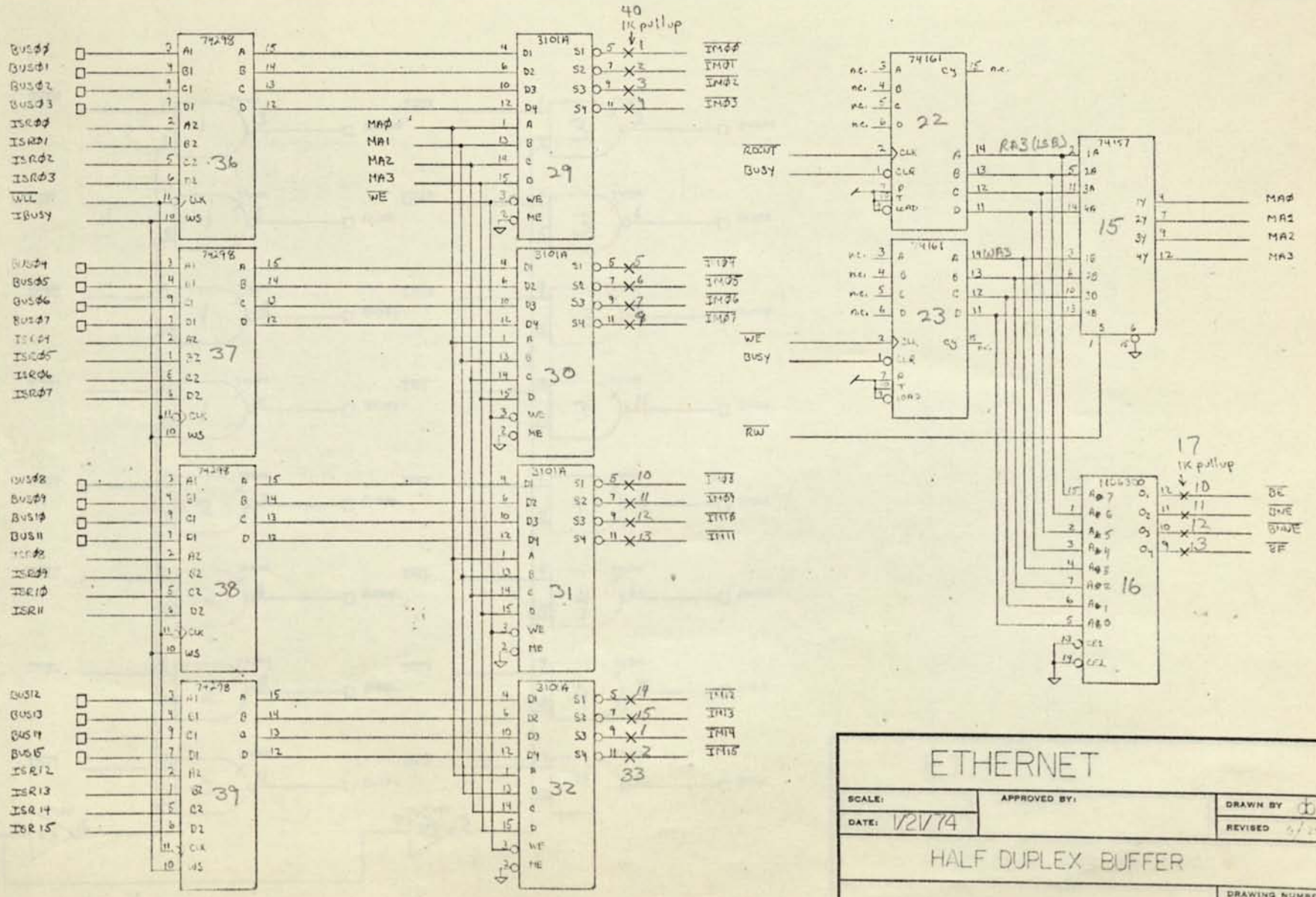




ETHERNET		
SCALE:	APPROVED BY:	DRAWN BY
DATE: 1/13/74		REVISED
INPUT STUFF		
		DRAWING NUMBER



ETHERNET		
SCALE:	APPROVED BY:	DRAWN BY
DATE: 1/12/74		REVISED
BUFFER CONTROL		
		DRAWING NUMBER

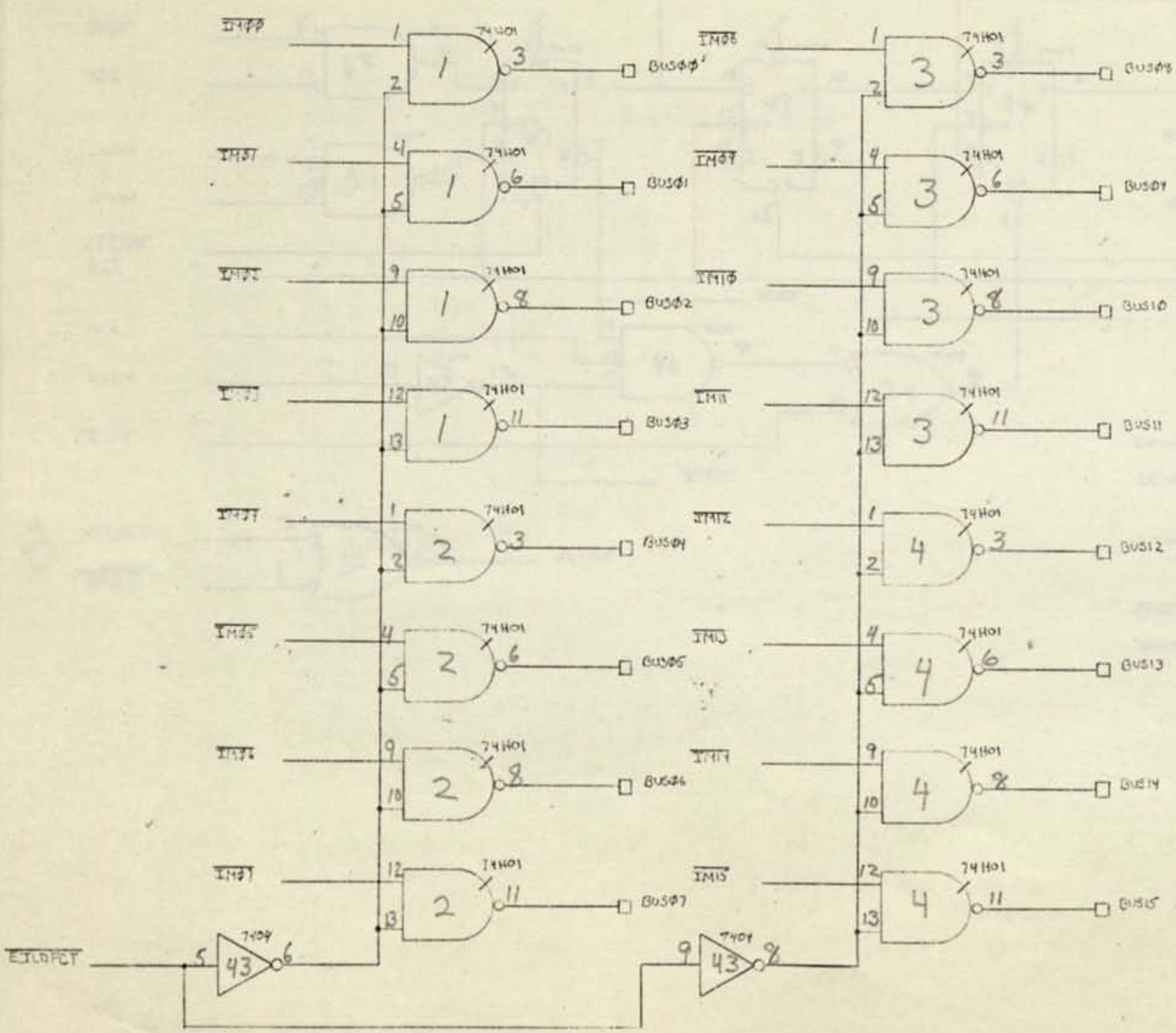


ETHERNET

SCALE:	APPROVED BY:	DRAWN BY	
DATE: 1/21/74		REVISED	

HALF DUPLEX BUFFER

DRAWING NUMBER



ETHERNET

SCALE:

DATE: 1/3/74

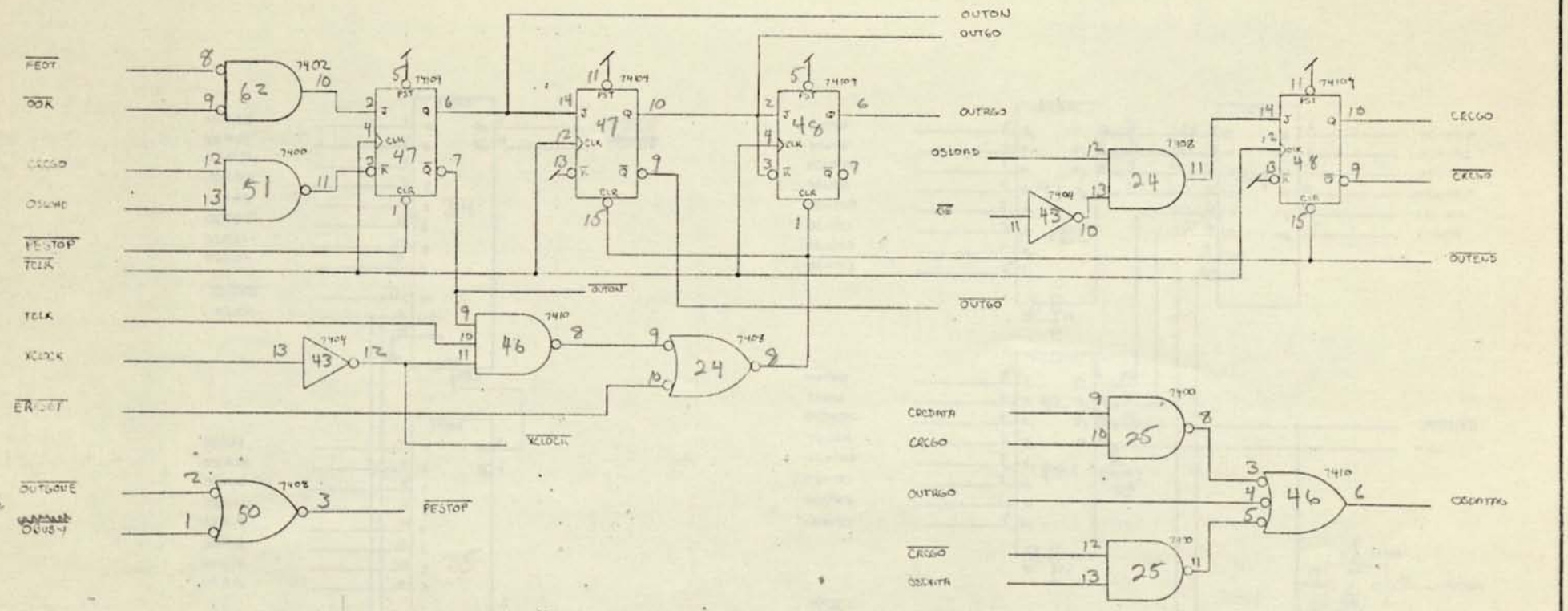
APPROVED BY:

DRAWN BY ⴷ

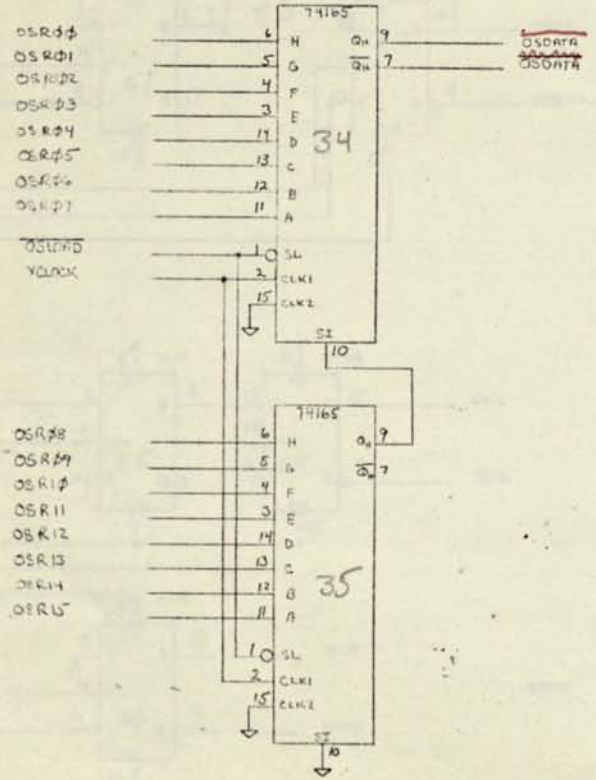
REVISED

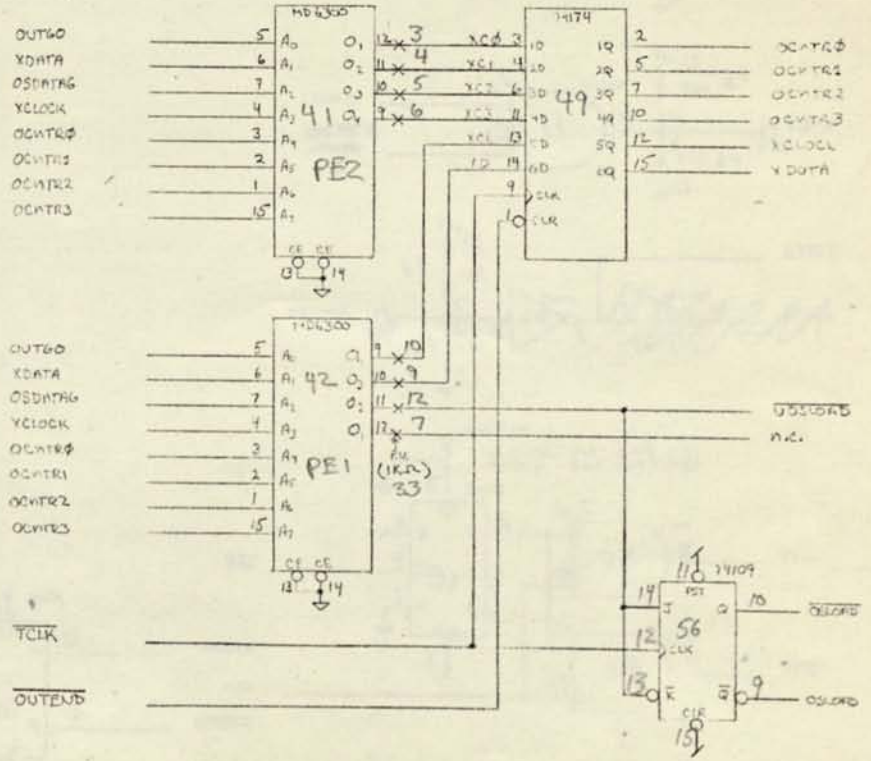
PROCESSOR BUS DRIVERS

DRAWING NUMBER



ETHERNET		
SCALE:	APPROVED BY:	DRAWN BY
DATE: 1/3/74		REVISED
PHASE ENCODER CONTROL		
		DRAWING NUMBER



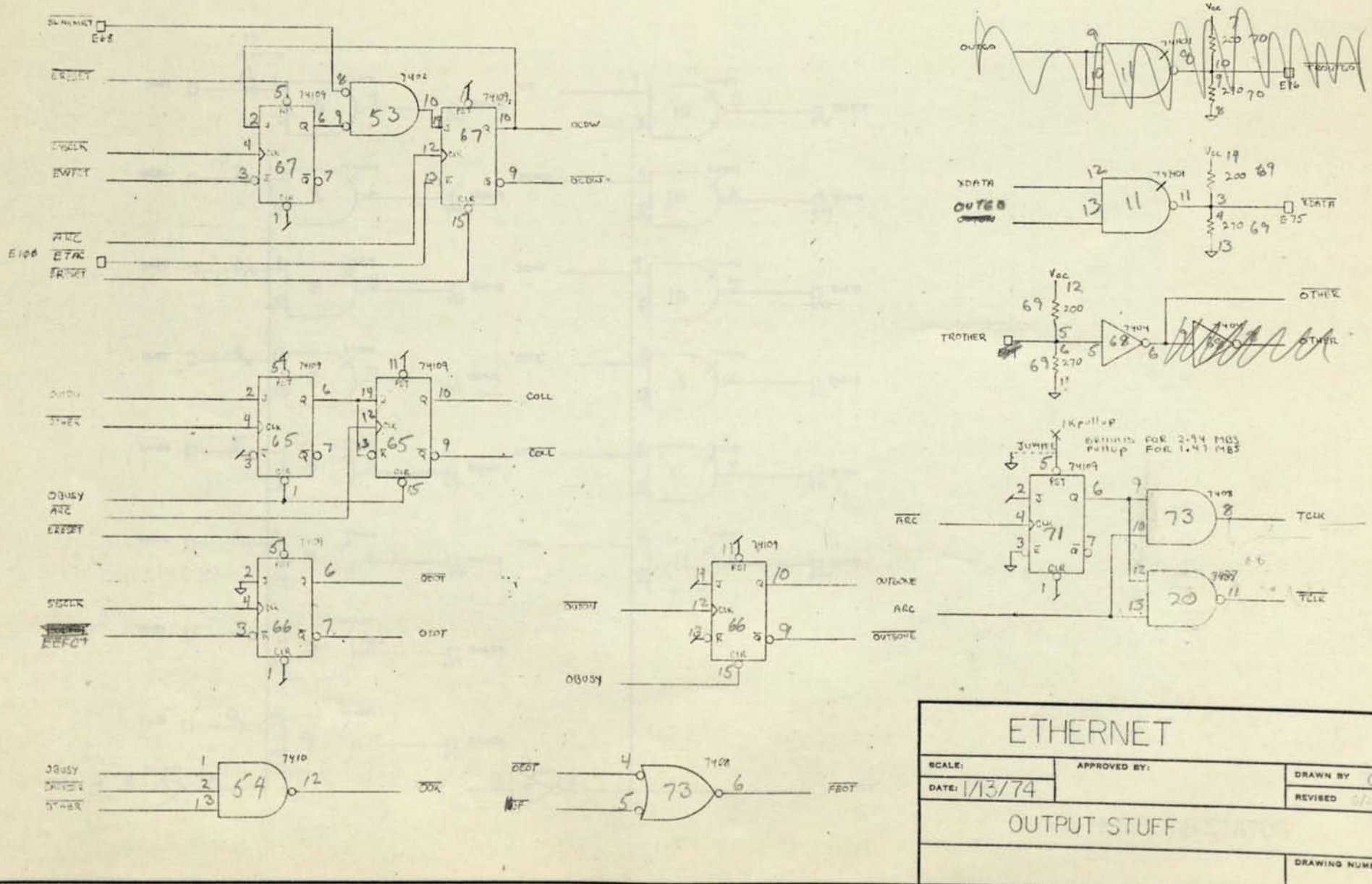


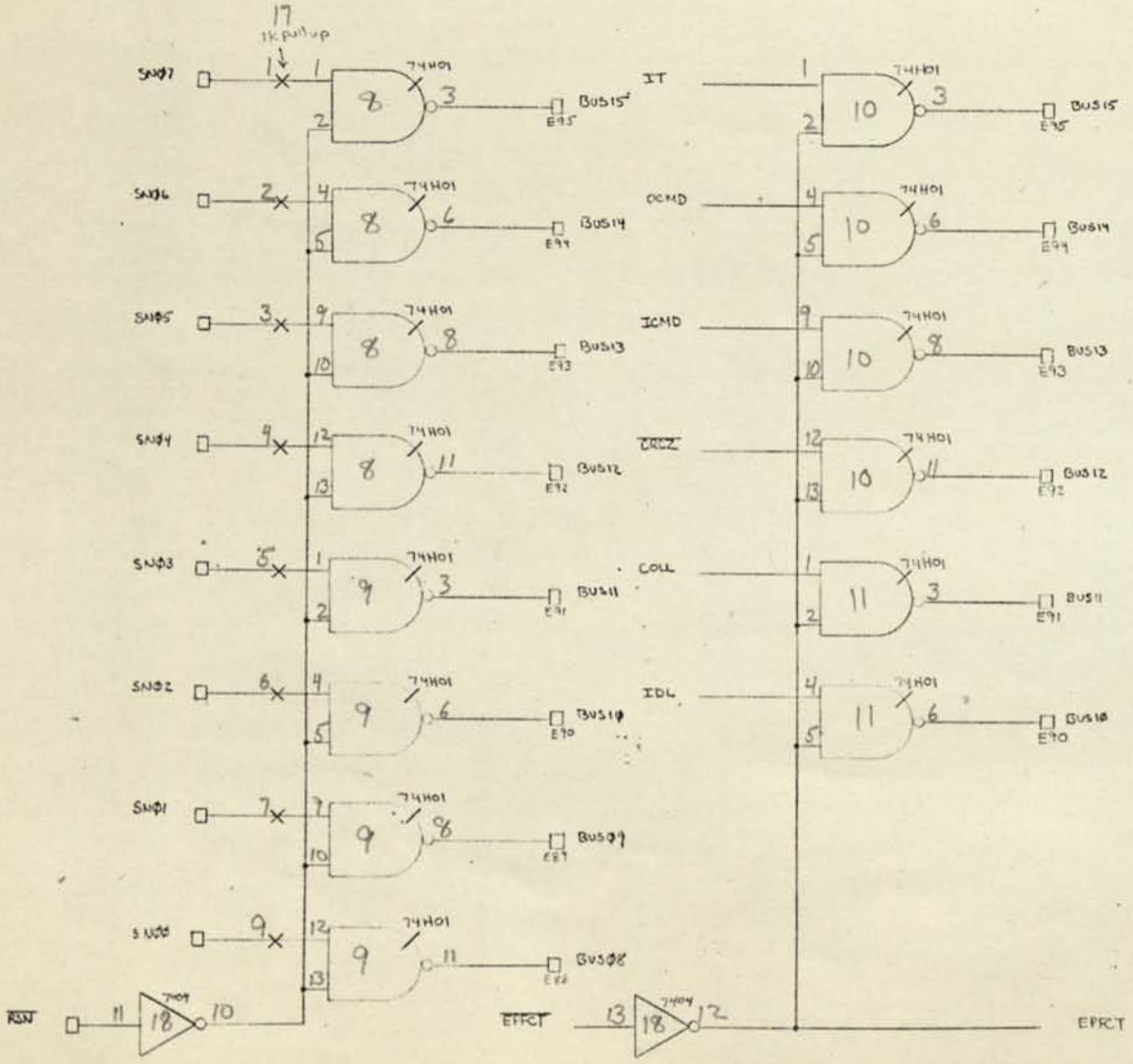
ETHERNET

SCALE:	APPROVED BY:	DRAWN BY
DATE: 1/2/74		REVISED 5/14/74

OUTPUT S.R. & PHASE ENCODER

DRAWING NUMBER


ETHERNET
SCALE:
APPROVED BY:
DRAWN BY
DATE: 1/13/74
REVISED
OUTPUT STUFF
DRAWING NUMBER
11X17 PRINTED ON NO. 1000H CLEARPRINT



ETHERNET

SCALE:	APPROVED BY:	DRAWN BY CD
DATE: 1/16/74		REVISED 6/22/74

SERIAL NUMBER & STATUS

DRAWING NUMBER

57	109	X X
58	109	X X
59	164	X
60	164	X
61	109	X X
62	7402	89/10 45/6 12/3
63	109	X X
64	109	X X
65	109	X X
66	109	X X
67	109	X X
68	04	1/2 3/4 5/6 9/8 11/10 13/12
69	COMP	
70	COMP	
71	109	1-8
72	109	X X
73	7408	12/3 45/6 89/10
74	7404	13/12 1/2 11/10 5/6 9/8 3/4
75	7400	123 45/6 89/10 1112/13
76	123	123/4 13
77	123	X X
78		
79		
80		
81		
82		
83	86	X X
84		

0	0	0
0	1	1
1	0	1
1	1	0

29	3101	X
30	3101	X
31	3101	X
32	3101	X
33	PU	3-10 1,2 12
34	165	X
35	165	X
36	298	X
37	298	X
38	298	X
39	298	X
40	PU	X
41	6300	X
42	6300	X
43	7404	5/6 9/8 3/4 11/10 17/13 1/2
44	8803	X
45	157	X
46	7410	9 10 5 4 12 1 8 5 6 3 2
47	74109	X X
48	74109	X X
49	74174	X
50	7408	8-10 12 3 4 5 6 11 12 13
51	7400	4-6 8-10 11 12 13 12 3
52	74157	X
53	7402	4 5 6 8 9 12 10 3
54	7410	3 4 5 6 2 13 12 X
55	~~PU~~	12 3
56	74109	7-15 8

1	H01	X X X X
2	H01	X X X X
3	H01	X X X X
4	H01	X X X X
5	H01	1-2 4-5 8-9 3 6 10
6	3404	X
7	3404	X
8	H01	X X X X
9	H01	X X X X
10	H01	X X X X
11	H01	1-3 4-6 X X
12	3205	X
13	3205	X
14	3205	X
15	157	X
16	6300	X
17	PU	10/13 1/9
18	7404	11/10 13/12 5/6 1/2 3/4 8/9
19	109	X X
20	7437	1-2 4-5 9-10 11-12 3 6 11 13
21	7400	1-2 4-5 X X 3 6
22	161	X
23	161	X
24	7408	11-12 8-9 1-2 4-5 13 10 3 6
25	7400	8-9 11-12 4-5 1-2 10 13 6 3
26	7400	X X X X
27	H21	X X
28	7408	8-9 11-12 10 13

```
;<METCALFE>ETHERNET.;12     5-MAR-74  9:35:05   EDIT BY METCALFE
;<METCALFE>ETHERNET.;2    27-JAN-73 16:23:12    EDIT BY METCALFE

;       ETHERNET ALTO MICROCODE, VERSION II, BOGGS AND METCALFE

;****** ADDRESSING CONSTRAINTS FOR ETHERNET MICROCODE
;       REPEATED WHERE USED

!3,4,EICDGO,EOREST,EIREST,ERBRES;
!3,4,EOEOK,EOEPST,EOECOL,EOEUGH;
!3,4,EODOK,EODPST,EODCOL,EODUGH;
!3,1,EPOST;
!3,1,EPOST0;
!3,1,ER3;
!1,2,EOINPR,EOINPN;
!1,2,EODMOR,EODEND;
!1,2,EOCTOK,EOCTZR;
!1,2,EOLDOK,EOLDBD;
!1,2,EIDMOR,EIDFUL;
!1,2,EIDOK,EIDPST;
!1,2,EIFIGN,EIDATA;
!1,2,EIFNBC,EIFBC;
!1,2,EIFCHK,EIFPRM;
!1,2,EIFOK,EIFBAD;
!1,2,EICTOK,EICTZR;
!1,2,EOCDW0,EIGO;
!1,2,EOCDW1,EOCDRS;
!1,2,EOCDWT,EOCDGO;

;****** R-MEMORY LOCATIONS

$ECNTR$R26;     COUNT OF WORDS YET TO BE PROCESSED IN MAIN LOOP
$EPNTR$R25;     POINTS AT WORD BEFORE THE WORD NEXT TO BE PROCESSED

;****** MICROCODE POST CODES (WITH MEANINGS)

$ESIDON$00;     INPUT FLOW DONE (MAY HAVE BEEN GOOD INPUT MSG)
$ESODON$01;     OUTPUT FLOW DONE (MAY HAVE BEEN GOOD OUTPUT MSG)
$ESIFUL$02;     INPUT BUFFER OVERFLOWED
$ESLOAD$03;     OUTPUT LOAD OVERFLOWED
$ESCZER$04;     WORD COUNT ZERO ON I/O COMMAND
$ESABRT$05;     FLOW ABORTED (SOMEHOW)
$ESNEVR$06;     CAN NEVER HAPPEN (HA)
```

```
;****** MAIN MEMORY LOCATION CONSTANTS

;                THE NEXT TWO MUST BE KEPT TOGETHER, EVEN ODD
$EPLOC $600;     POST LOCATION, GETS POST CODE WHEN OPERATION COMPLETES
$EBLOC $601;     INTERRUPT BIT LOCATION, BIT TO BE ORED INTO NWW ON POST

$EELOC $602;     EOT LOCATION, GETS COUNTER VALUE ON ALL POSTS
$ELLOC $603;     LOAD LOCATION, ZEROED ON SUCCESSFUL OUTPUT

;                THE NEXT TWO PAIRS MUST BE KEPT TOGETHER, EVEN ODD
$EICLOC$604;     INPUT BUFFER CONTROL (1/2), COUNT (ZEROED ON AOK)
$EIPLOC$605;     INPUT BUFFER CONTROL (2/2), POINTER
$EOCLOC$606;     OUTPUT BUFFER CONTROL (1/2), COUNT (ZEROED ON AOK)
$EOPLOC$607;     OUTPUT BUFFER CONTROL (2/2), POINTER

$ESLOC $610;     SERIAL NUMBER LOCATION, TO HOLD 8-BIT SERIAL NUMBER

$EEXTRA$611;     UNUSED EXTRA WORD WHOSE CONSTANT IS DEFINED
$ESPARE$612;     UNUSED SPARE WORD WHOSE CONSTANT IS DEFINED

;****** FUNCTION DEFINITIONS

;                                  FUNCTION 1'S
$EIDFCT$L000000,070010,000100;   INPUT DATA, F1=10
$EISFCT$L016011,000000,000000;   INPUT START, F1=11
$ELFCT $L000000,070013,000100;   INPUT LOOK FUNCTION,F1=13
$EPFCT $L000000,070014,000100;   F1=14, DEFINES THE BUS
$EWFCT $L016015,000000,000000;   WAKE-UP FUNCTION, F1=15

;                                  FUNCTION 2'S
$EODFCT$L026010,000000,124000;   F2=10, OUTPUT DATA
$EOSFCT$L024011,000000,000000;   F2=11, START OUTPUT
$ERBFCT$L024012,000000,000000;   REST BRANCH FUNCTION F2=12
$EEFCT $L024013,000000,000000;   EOT FCT, F2=13
$EBFCT $L024014,000000,000000;   BRANCH FUNCTION, F2=14
$ECBFCT$L024015,000000,000000;   COUNTDOWN BRANCH FUNCTION F2=15
```

```
;****** REST -- START HERE AT FIRST AND WHEN RESET THEREAFTER

;       BRANCH ACCORDING TO REST BRANCH FUNCTION (ERBFCT)
;              00  NON-COMMAND WAKE-UP (NO COMMAND ISSUED)
;                  JUMPED HERE FROM OUTPUT COUNT-DOWN CODE
;              01  OUTPUT START COMMAND FROM EMULATOR
;              10  INPUT START COMMAND FROM EMULATOR
;              11  RESET COMMAND FROM EMULATOR

;                                 EREST IS LOCATION 6 IN TASK INIT VECTOR
;                                 SHAKE PENDING BRANCH
EREST:  ERBFCT,MAR←EICLOC,:ER3; !3,1,ER3;
ER3:    :EICDGO;                !3,4,EICDGO,EOREST,EIREST,ERBRES;

ERBRES: L←ESABRT,:EPOST;        RESET COMMAND WHILE RESET, DO IT

;****** POST -- COME HERE TO POST CONDITIONS AND RESET DEVICE
;       FIND POST-CODE IN L
;       PUTS (POST-CODE,,HARDWARE STATUS) IN POST LOCATION

EPOST:  :EPOST0,MTEMP←LLCY8;    SHAKE PENDING BRANCH, FIXUP POST CODE
;                               !3,1,EPOST;     SHAKE FOUR-WAY BRANCH
;                               !3,1,EPOST0;    SHAKE FOUR-WAY BRANCH

;       PERMIT FOLLOWING WRITE-READ OPERATION WITH:
;              00  EPLOC  POST LOCATION
;              01  EBLOC  INTERRUPT BIT LOCATION

EPOST0: T←MTEMP;                GET SWAPPED POST CODE
        MAR←EELOC;              START WRITE OF EOT LOCATION
        T←377 OR T;             PREPARE TO "AND" IN POST CONDITIONS
        L←EPFCT AND T;          MERGE POST CODE AND DEV STATUS, RESET
        EPNTR←L,TASK;           SAVE POST CODE FOR LATER
        MD←ECNTR,EWFCT,:EPOST1; SCHEDULE WAKE-UP, WRITE COUNT
;                               EWFCT MUST FOLLOW TASK INSTRUCTION
;                               GIVE UP PROCESSOR FOR 0-37 MICROSEC

EPOST1: MAR←EPLOC;              START WRITE OF POST CODE
        T←NWW;                  PICK UP INTERRUPT WORD
;                               WASTE TWO CYCLES WAITING FOR MEMORY
        MD←EPNTR;               WRITE POST CODE
        L←MD OR T,TASK;         READ INTERRUPT BIT AND USE IT
        NWW←L,:EREST;           SIGNAL INTERRUPT AND GO TO REST
```

```
;****** INPUT REST -- BEGIN INPUT HERE

EIREST: SINK←EPFCT;             START HERE ON COMMAND, CLEAR DEVICE
        EISFCT,:EICDGO;         BEGIN INPUT NOW, OVER SETUP

;                               MIGHT COME HERE FROM OUTPUT CNTDWN
;                               0 OR 2 CYCLES WASTED HERE ON MEMORY
EICDGO: L←MD,BUS=0;             GET WORD COUNT AND CHECK FOR ZERO
        :EICTOK,T←MD-1;         !1,2,EICTOK,EICTZR;

EICTOK: ECNTR←L,L←T,TASK;       COUNTER SETUP, READY POINTER
EIFBUM: EPNTR←L,:EIFRST;        STASH POINTER, GET FIRST WORD

EICTZR: L←ESCZER,:EPOST;        ZERO WORD COUNT, POST
```

```
;****** INPUT FIRST WORD -- CHECK DESTINATION FOR "MATCH"

;       EBFCT - ETHERNET BRANCH FUNCTION
;               00  DATA WAKE-UP (I OR O) OR COUNT-DOWN WAKE-UP
;               01  POST WAKE-UP (I OR O)
;               10  COLLISION WAKE-UP (O ONLY)
;               11  POST OR COLLISION WAKE-UP (O ONLY)

;       SERIAL NUMBER FOR INPUT MESSAGE FILTERING
;               ESLOC=0: PROMISCUOUS, ACCEPT ALL MESSAGES
;               DESTINATION=0: BROADCAST MSG, ACCEPT IT
;               ESLOC=DESTINATION: MESSAGE TO US, ACCEPT, MATCH
;               17 CYCLES TO REJECT A MESSAGE (<<<10% MACHINE)

EIFRST: MAR←ESLOC;              START READ OF SERIAL NUMBER
        EBFCT;                  BRANCH IF NOT INPUT DATA WORD
;                               WASTE TWO CYCLES WAITING FOR MEMORY
        :EIFOK,L←MD,BUS=0;      GET SERIAL NUMBER, CHECK FOR ZERO
;                               !1,2,EIFOK,EIFBAD;
EIFOK:  :EIFCHK,MTEMP←L;        BRANCH, SAVE SERIAL NUMBER
;                               !1,2,EIFCHK,EIFPRM;

EIFBAD: L←ESABRT,:EPOST;        NOT THE FIRST WORD, POST

EIFPRM: :EIDATA;                PROMISCUOUS, ACCEPT MESSAGE

EIFCHK: T←ELFCT;                LOOK AT (DEST,SRC) WORD
        L←-400 AND T;           STRIP OFF SOURCE
        T←MTEMP,SH=0;           DEST=0 MEANS BROADCAST MESSAGE
        :EIFNBC,MTEMP←LLCY8;    BRANCH, BRING DEST TO RIGHT HALF
;                               !1,2,EIFNBC,EIFBC;

EIFBC:  :EIDATA;                BROADCAST MESSAGE, ACCEPT IT

EIFNBC: L←MTEMP-T;              DOES DEST MATCH OUR SERIAL NUMBER?
        SH=0;
        :EIFIGN;                BRANCH, IGNORE OR ACCEPT
;                               !1,2,EIFIGN,EIDATA;

EIFIGN: SINK←EPFCT;             IGNORE MESSAGE, RESET DEVICE
        EISFCT;                 START INPUT AGAIN
        L←EPNTR,TASK,:EIFBUM;   GO WAIT FOR FIRST WORD AGAIN
```

```
;****** INPUT MAIN LOOP

EIDATA: L←MAR←EPNTR+1,EBFCT;     START MEMORY AT POINTER PLUS ONE
        :EIDOK,EPNTR←L;          !1,2,EIDOK,EIDPST;
EIDOK:  L←ECNTR-1,BUS=0;         DEC COUNTER, CHECK FOR ZERO OR TROUBLE
        :EIDMOR,ECNTR←L,TASK;    !1,2,EIDMOR,EIDFUL;
EIDMOR: MD←EIDFCT,:EIDATA;       PICK UP WORD OF DATA, WRITE, LOOP
;                                5 CYCLES IS THE MINIMUM LOOP POSSIBLE
;                                15.6% OF MACHINE WHEN BLASTING

EIDPST: L←ESIDON,:EPOST;         INPUT STOPPED

EIDFUL: L←ESIFUL,:EPOST;         INPUT BUFFER OVERFLOW
```

```
;****** OUTPUT REST

EOREST: MAR←ELLOC;                  GET LOAD READ GOING
        NOP;                        WAIT FOR MEMORY
;                                   WASTE TWO CYCLES WAITING FOR MEMORY
        L←MD;
        SH<0,ECNTR←L;               LOAD OVERFLOW? STASH
        :EOLDOK,MTEMP←LLSH1;        BRANCH, UPDATE LOAD SOME
;                                   !1,2,EOLDOK,EOLDBD;

EOLDBD: L←ESLOAD,:EPOST;            LOAD OVERFLOW

EOLDOK: MAR←ELLOC;                  BEGIN LOAD UPDATE
        L←MTEMP+1;                  LOAD IS UPDATED
        MTEMP←L,TASK;               PREPARE TO TASK FOR A WHILE
        MD←MTEMP,:EORST1;           WRITE UPDATED LOAD
;                                   PENDING WAKEUP SHOULD TAKE

EORST1: L←R37;                      PICK UP RANDUM NUMBER (CLOCK)
        MTEMP←LLSH1;                TRANSFORM INTO SMALL RANDUM NUMBER
        L←MTEMP;
        MTEMP←LLSH1;
        L←MTEMP;
        MTEMP←LLCY8;
        T←ECNTR;                    PICK UP OLD LOAD
        T←377 . T;                  MAKE EFFECTIVE LOAD 8 BITS ONLY
        MAR←EICLOC;                 HAS AN INPUT BUFFER BEEN SET UP?
        L←MTEMP AND T;              RANDUM INTERVAL COUNTDOWN
        ECNTR←L;                    SETUP COUNT-DOWN FOR LOOP
        SINK←EPFCT;                 CLEAR DEVICE
        L←MD,BUS=0;                 INPUT BUFFER SETUP?
        :EOINPR;                    !1,2,EOINPR,EOINPN;

EOINPR: EISFCT,:EOCDWT;             START INPUT UNDER OUTPUT COUNTDOWN

EOINPN: :EOCDWT;                    JUST COUNTDOWN, NO INPUT
```

```
;****** COUNTDOWN LOOP

;       COUNTDOWN BRANCH FUNCTION
;               0  NOT AN INPUT DATA WAKE-UP
;               1  AN INPUT DATA WAKEUP, GO HANDLE INPUT

EOCDWT: ECBFCT;                     CHECK FOR ARRIVAL OF INPUT MSG
        :EOCDW0,EBFCT;              BRANCH, SOMETHING WRONG? (RESET?)
;                                   !1,2,EOCDW0,EIGO;
EOCDW0: :EOCDW1,L←ECNTR-1,BUS=0,TASK;
;                                   !1,2,EOCDW1,EOCDRS;
EOCDW1: ECNTR←L,EWFCT,:EOCDWT;      COUNT DOWN MORE (EVERY 37 MSEC)
;                                   !1,2,EOCDWT,EOCDGO;

EOCDRS: L←ESABRT,:EPOST;            BLASTED OUT OF COUNTDOWN LOOP (RESET?)

EIGO:   :EREST                      HANDLE INCOMING INPUT, UNDER COUNTDOWN

;****** SETUP FOR OUTPUT OF MESSAGE

EOCDGO: MAR←EOCLOC;                 START READ OF SIZE AND POINTER
        SINK←EPFCT;                 RESET HARDWARE (INPUT MAY BE ON)
;                                   WASTE TWO CYCLES WAITING FOR MEMORY
        L←MD,BUS=0;                 GET WORD COUNT AND CHECK FOR ZERO
        :EOCTOK,T←MD-1;             PICK AND DIDDLE POINTER
;                                   !1,2,EOCTOK,EOCTZR;

EOCTZR: L←ESCZER,:EPOST;            ZERO WORD COUNT

EOCTOK: ECNTR←L,L←T,TASK;           STASH COUNTER
        EPNTR←L,EOSFCT,:EODATA;     STASH POINTER, START DEVICE
```

```
;****** OUTPUT MAIN LOOP

EODATA: L←MAR←EPNTR+1,EBFCT;     START READ OF DATA WORD, WAKEUP?
        :EODOK,T←ECNTR-1,BUS=0; BRANCH, CNTDWN, CHECK FOR BUFFER EMPTY
;                                !3,4,EODOK,EODPST,EODCOL,EODUGH;
EODOK:  :EODMOR,EPNTR←L,L←T;     BRANCH, UPDATE POINTER
;                                !1,2,EODMOR,EODEND;
EODMOR: ECNTR←L,TASK;            BRANCH, UPDATE COUNTER
        EODFCT←MD,:EODATA;       RAM DATA OUT, SLEEP

EODEND: EEFCT;                   NO MORE DATA TO COME
        TASK;                    ONLY NOW BECAUSE EOFCT MUST TAKE EFFECT
        :EOEOT;                  WAIT FOR WAKEUP WHEN MSG IS GONE

EODPST: L←ESABRT,:EPOST;         SOMETHING WENT TERRIBLY WRONG

EODUGH: L←ESABRT,:EPOST;         ABOVE PLUS COLLISION

EODCOL: :EOREST;                 START OVER AFTER RANDOM COUNTDOWN
```

```
;****** OUTPUT EOT CODE

EOEOT:  EBFCT;                  CHECK WAKE-UP
        :EOEOK;                 START MEMORY ON LOAD CLEAR
;                               !3,4,EOEOK,EOEPST,EOECOL,EOEUGH;

EOEOK:  L←ESNEVR,:EPOST;        NEVER HAPPEN

EOEPST: L←ESODON,:EPOST;        POST

EOECOL: :EOREST;                START OVER AFTER RANDOM COUNTDOWN

EOEUGH: L←ESABRT,:EPOST;        HUH?
```

TRUTH

* FILE CREATED 3-JUL-74 15:07:12
* ETHERNET2 MAIN WIRELIST

The chips run parallel to their names

	1	2	3	4	5	6	7
0	74H01	74H01	74H01	74H01	74H01	I3404	I3404
7	74H01	74H01	74H01	74H01	I3205	I3205	I3205
14	74157	MD6300	B898-84	7404	74109	7437	7400
21	74161	74161	7408	7400	7400	74H21	~~7408~~ H
28	I3101A	I3101A	I3101A	I3101A	B898-84	74165	74165
35	74298	74298	74298	74298	B898-84	MD6300	MD6300
42	7404	MC8503	74157	7410	74109	74109	74174
49	7408	7400	74157	7402	7410	74H21	74109
56	74109	74109	74164	74164	74109	7402	74109
63	74109	74109	74109	74109	7404	PLT84	PLT84
70	74109	74109	7408	7404	7400	74123	74123
77	-	-	-	-	-	7486	PLT84
84	-	-	-	-	-	-	-

Chip 5=5: SN74H01 has unused groups: 4
Chip 11=11: SN74H01 has unused groups: 3
Chip 28=28: SN7408 has unused groups: 1 2
Chip 53=53: SN7402 has unused groups: 4
Chip 62=62: SN7402 has unused groups: 4
Chip 68=68: SN7404 has unused groups: 1 2
Chip 71=71: SN74109 has unused groups: 2
Chip 83=83: SN7486 has unused groups: 2 3 4

PLEASE SAVE

* FILE CREATED 3-JUL-74 15:26:10
* ETHERNET2 LOAD CHART

The chips run parallel to their names

	1	2	3	4	5	6	7
0	74H01	74H01	74H01	74H01	74H01	I3404	I3404
7	74H01	74H01	74H01	74H01	I3205	I3205	I3205
14	74157	AFIFO MD6300	B898-84	7404	74109	7437	7400
21	74161	74161	7408	7400	7400	74H21	~~7508~~ 74H08
28	I3101A	I3101A	I3101A	I3101A	B898-84	74165	74165
35	74298	74298	74298	74298	B898-84	~~PE2~~ MD6300	PE1 MD6300
42	7404	MC8503	74157	7410	74109	74109	74174
49	7408	7400	74157	7402	7410	74H21	74109
56	74109	74109	74164	74164	74109	7402	74109
63	74109	74109	74109	74109	7404	PLT84	PLT84
70	74109	74109	7408	7404	7400	74123	74123
77	-	-	-	-	-	7486	PLT84
84	-	-	-	-	-	-	-

Chip 5-5: SN74H01 has unused groups: 4
Chip 11-11: SN74H01 has unused groups: 3
Chip 28-28: SN7408 has unused groups: 1 2
Chip 53-53: SN7402 has unused groups: 4
Chip 62-62: SN7402 has unused groups: 4
Chip 68-68: SN7404 has unused groups: 1 2
Chip 71-71: SN74109 has unused groups: 2
Chip 83-83: SN7486 has unused groups: 2 3 4

B898-84 are 1K Backman 16 pin packages

pin numbers are AUGAT pins (1-16) NOT chip pins

ADD. E12 TO 7*15 SYSCLK
REM 75*6 TO 19*4
REM 75*6 TO 74*1 } SIOCLK
REM 74*2 TO 5*11
ADD 75*6 TO 19*4
REM 1*3 TO E80
REM E80 TO 5*12 } BUSØØ.
ADD E80 TO 11*12
ADD E80 TO 1*3
ADD 11*10 TO 17*14
ADD 7*14 TO 11*10
ADD 5*11 TO 5*12
ADD 5*12 TO 7*13
ADD TO 18*6

REM 75*2 TO 18*15
ADD 75*2 TO 10*15
REM 73*2 TO 68*6
REM 65*4 TO E74
REM 73*2 TO 65*4
ADD E74 TO 65*4
ADD 65*4 TO 68*6
ADD 73*2 TO 53*15

ETHERNET2.LA

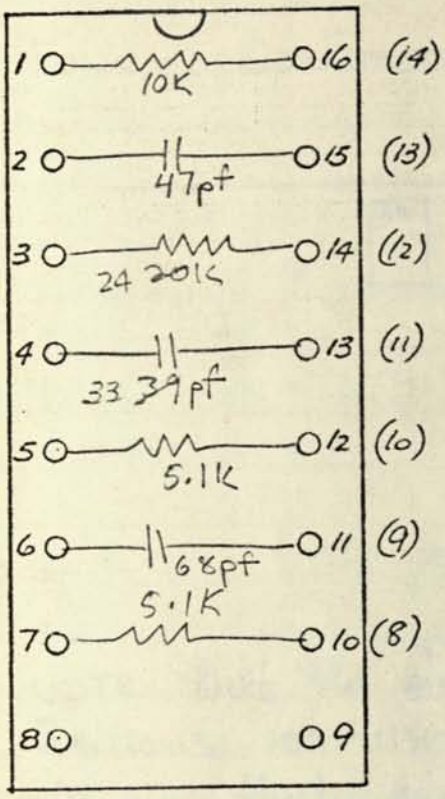
* FILE CREATED 3-JUL-74 15:26:03
* ETHERNET2 EDGE PINS

1	OKTORUN	62	-SRESET
2	RESET	63	DBARC
3		64	
4		65	
5		66	
6		67	
7	PLUS15	68	-SWAKMRT
8		69	
9		70	
10		71	
11		72	AUSYSCLK
12	-SYSCLK	73	RDATA
13		74	-OTHER
14		75	XDATA
15		76	OUTGO
16		77	
17		78	
18	-SN00	79	
19	-SN01	80	BUS00
20	-SN02	81	BUS01
21	-SN03	82	BUS02
22	-SN04	83	BUS03
23	-SN05	84	BUS04
24	-SN06	85	BUS05
25	-SN07	86	BUS06
26		87	BUS07
27		88	BUS08
28		89	BUS09
29		90	BUS10
30	F1(0)	91	BUS11
31	F1(1)	92	BUS12
32	F1(2)	93	BUS13
33	F1(3)	94	BUS14
34		95	BUS15
35		96	
36	F2(0)	97	
37	F2(1)	98	
38	F2(2)	99	EMACT
39	F2(3)	100	-ETAC
40		101	
41	-SIO	102	
42	-RSN	103	-WAKEET
43	-EM15	104	
44	-EM14	105	
45		106	-NEXT06
46	-EM13	107	-NEXT07
47	-EM12	108	
48	-EM11	109	
49	-EM10	110	
50		111	-←KDATA
51		112	INON
52		113	IBUSY
53		114	OBUSY
54		115	OUTON
55		116	
56		117	
57		118	
58		119	
59		120	
60		121	
61		122	

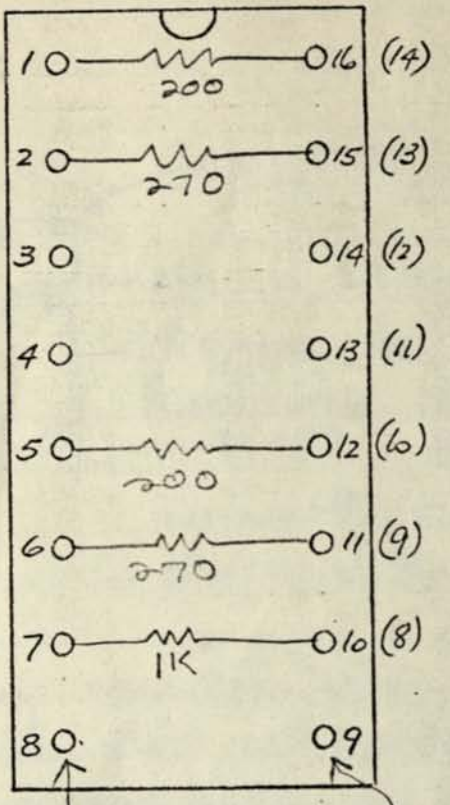
TRUET

PLATFORMS.

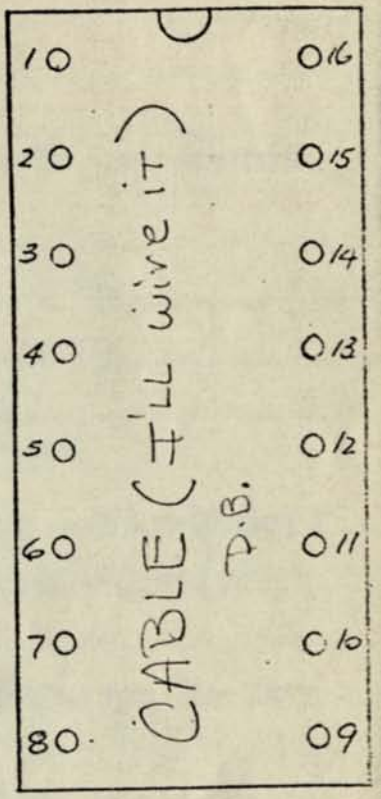
70



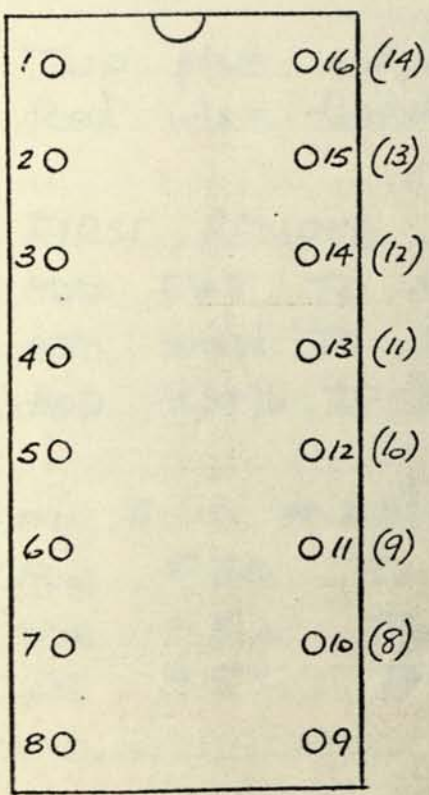
69

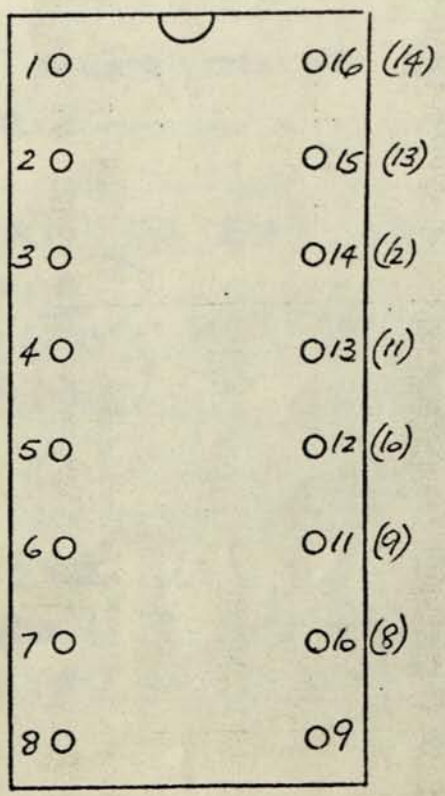


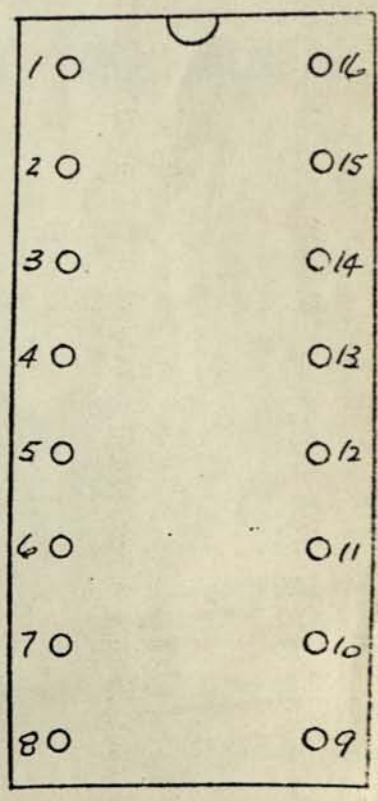
84



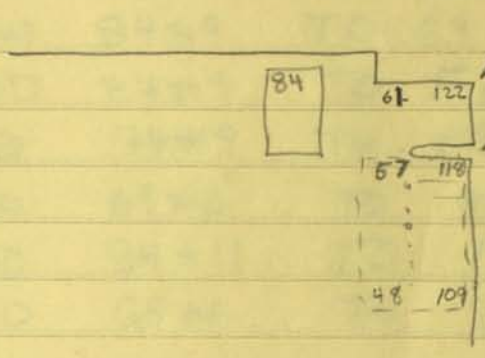
AUGAT PINS.
LEAVE these IN
(2 socket pins)







FUNNY CONNECTOR:



Remove the TWENTY CONNECTOR pins:
48-57 109-118

MOUNT the FUNNY with the short pins into the board & Solder.

NOTE that the FUNNY CONNECTOR pins that go into POSITIONS 109-118 are NOT ACCESSABLE.
the pins that are accessable will be called F48 - F57. You MUST SOLDER TO THESE, and wire-wrap the other ends

TWO pins supply power to the head. USE #26 ga Red wire for these. The pins:

FIRST REMOVE 84*15 TO E*7 (EDGE CONN)
ADD E*7 TO 84*14
② ADD 84*14 TO F57 (+15) } Red #26
① ADD 83*16 TO F49 (+5) }

NOW, BLUE #30 ga

② ADD F50 TO 82*8 }
④ ADD F52 TO 82*8 } GROUNDS
⑥ ADD F54 TO 83*7 }

⑤ ADD F51 TO 84*10 XDATA
REM 84*9 TO 69*15
⑤ ADD 84*9 TO F53 TDATA
ADD 84*9 TO 69*15
REM 69*6 TO 84*11
⑦ ADD 84*11 TO F55 TCLK
ADD 69*6 TO 84*11

BLUE #30

ADD the STANDARD WIRE FROM the EDGE CONNECTOR TO the VCC PLANE.

TWO of the "inaccessable" pins ON the FONNY CONNECTOR MUST be GROUNDED.
ON the VCC SIDE (BACK) of the board, SOLDER INSULATED WIRES (26 ga or larger) from:

F116 TO 83*8
F112 TO 82*8

NOTE THAT the LAYOUT PAGE HAS 14 WIRES TO CHANGE ON IT. THIS is the SRESET change that I gave you drawing for TO give TO H+M. It happened 2 weeks a/for the wire list.

BY MISTAKE I LOADED a 200Ω+270Ω resistor in 69 - they aren't used. DONT copy this.