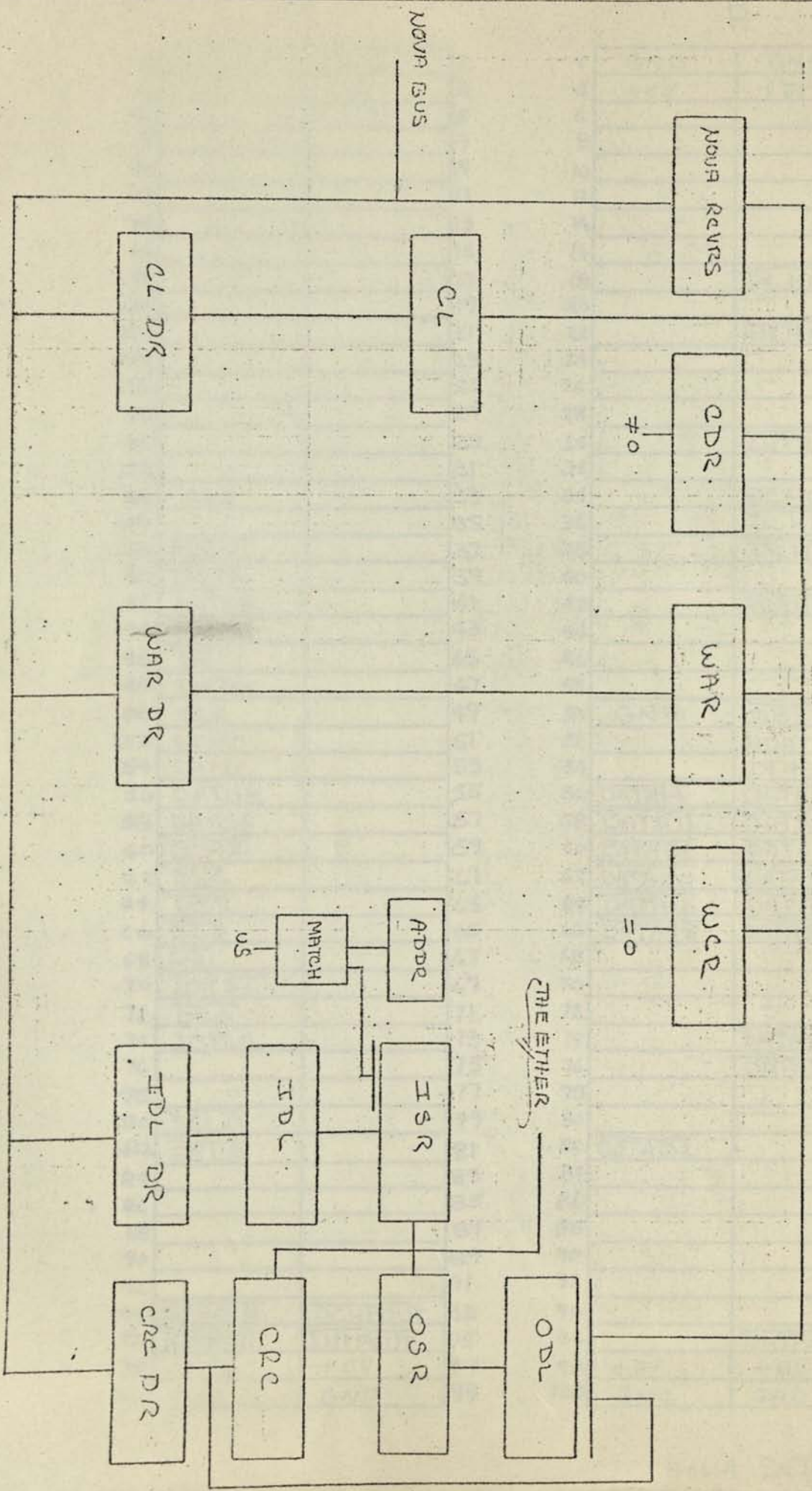


ETHERNET QUICK & DIRTY NOVA INTERFACE



NOVA EDGE PINS

A

2	GND	GND	1
4	+5V	+5V	3
6			5
8			7
10			9
12			11
14			13
16			15
18			17
20			19
22			21
24			23
26			25
28			27
30			29
32			31
34	GND		33
36			35
38	MSK0		37
40	INTA		39
42	DATIB		41
44	DATIA		43
46	DS3		45
48	DATOC		47
50	CLR		49
52	STRT		51
54	DATIC		53
56	DATOB		55
58	DATOA		57
60	DCHA		59
62	DS4		61
64	DS5		63
66	DS2		65
68	DS1		67
70	IORST		69
72	DS0		71
74	IOPLS		73
76			75
78			77
80	SELD		79

B

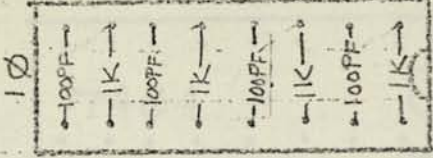
2	GND	GND	1
4	+5V	+5V	3
6			5
8			7
10			9
12			11
14			13
16			15
18		DCHM0	17
20			19
22		DCHM1	21
24			23
26			25
28			27
30		INTR	29
32			31
34		DCHO	33
36		DCHR	35
38		DCHI	37
40			39
42		ROENB	41
44			43
46			45
48			47
50	GND	OBXD	49
52		RDATA	51
54		OTHER	53
56	DATA14	DATA07	55
58	DATA11	DATA05	57
60	DATA08	DATA12	59
62	DATA00	DATA04	61
64	DATA13	DATA09	63
66	DATA15	DATA01	65
68			67
70			69
72			71
74		DATA03	73
76		DATA10	75
78			77
80			79

7474 17

7402 9

7438 1

7408 18



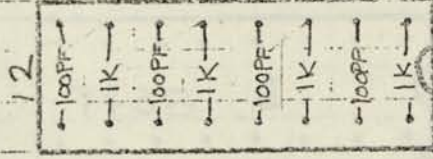
7410 2

7404 19

7430 11

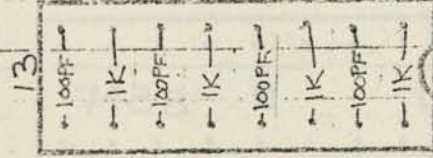
7404 10

7400 20



7410 4

7474 21



7410 5

7474 22

14

6

MD6300 23

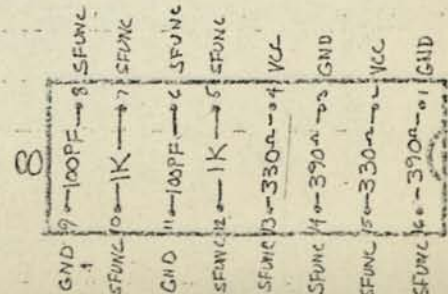
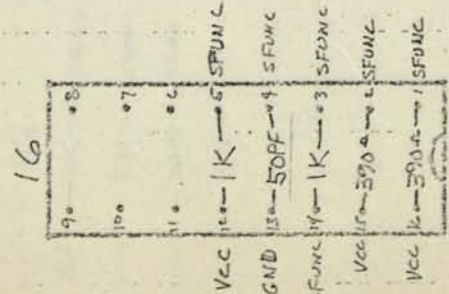
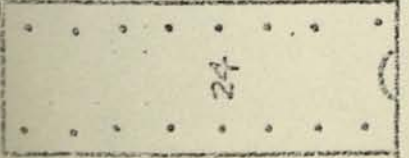
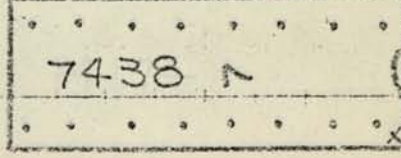
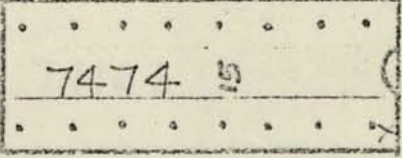
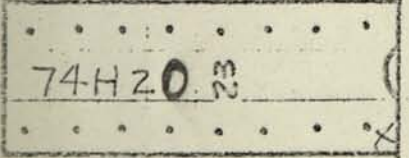
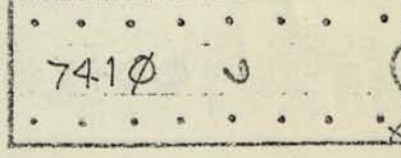
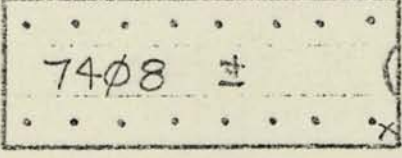
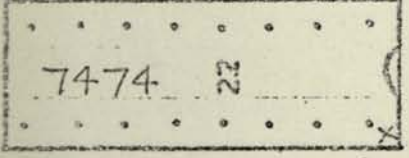
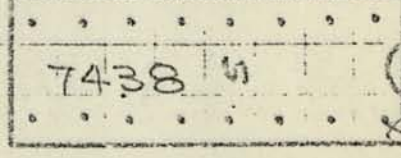
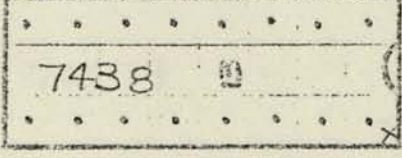
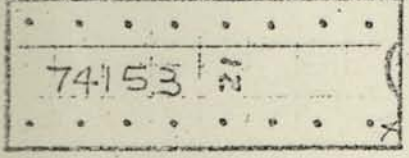
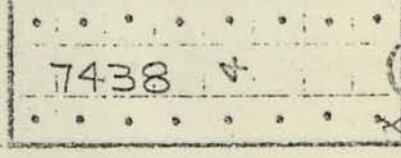
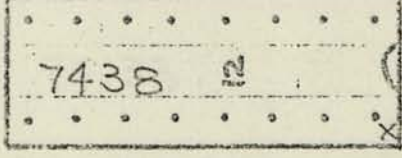
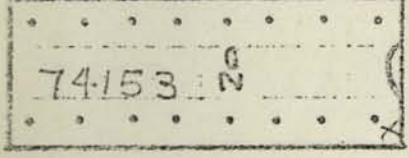
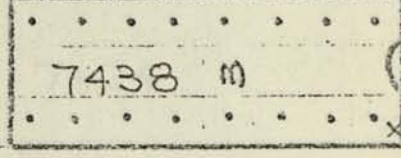
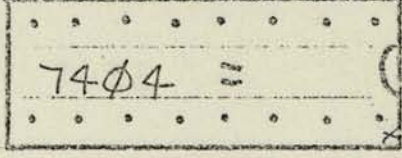
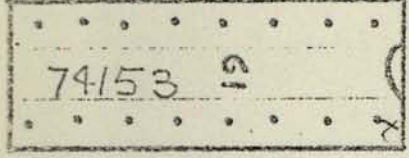
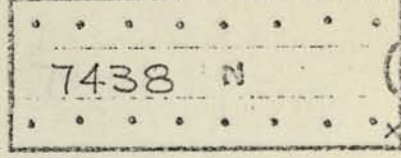
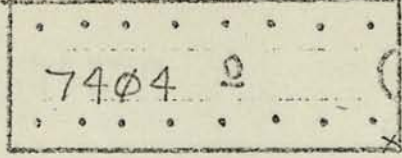
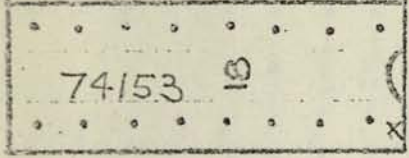
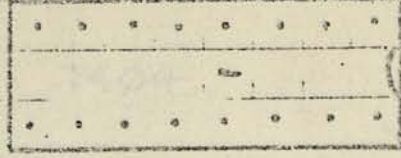
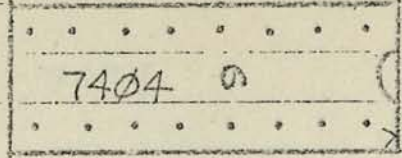
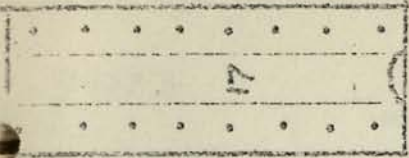
MD6300 15

B898-10-1 (390n)

24

16

8



74123 17

7474 9

7404 1

08
07
06
05
04
03
02
01

Vcc 13 → 1K → 4 SFUNC
SFUNC 19 → 10PF → 3 SFUNC
Vcc 15 → 2.5K → 2 SFUNC
Vcc 16 → 5K → 1 SFUNC

74279 10

74H11 2

7400 19

7432 11

7474 3

7408 20

74133 12

7474 4

7420 21

74279 13

7410 5

7410 22

7404 14

7400 6

74123 23

74123 15

74174 7

74 24

16

Vcc 9 → 1K → 8 SFUNC
Vcc 10 → 5K → 7 SFUNC
SFUNC 11 → 100PF → 6 SFUNC
Vcc 12 → 5K → 5 SFUNC
SFUNC 13 → 20PF → 4 SFUNC
Vcc 17 → 5K → 3 SFUNC
SFUNC 15 → 33PF → 2 SFUNC
Vcc 16 → 20K → 1 SFUNC

74 25

B.D.D

74191 17

74191 9

1

74298 18

74191 10

74153 2

74298 19

74191 11

74153 3

74298 20

74191 12

74153 4

74298 21

74191 13

74153 5

74165 22

74191 14

7400 6

74165 23

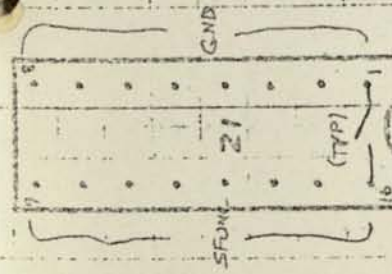
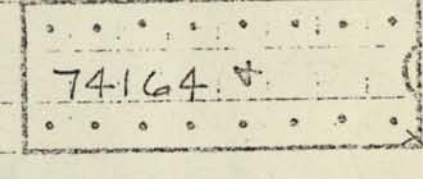
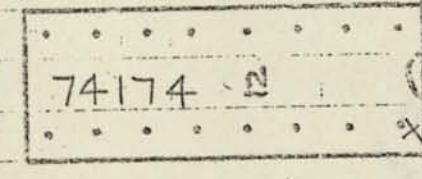
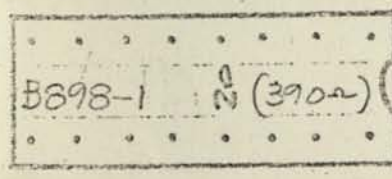
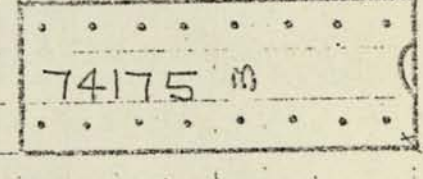
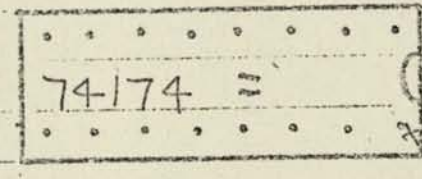
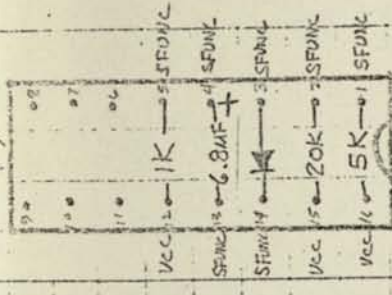
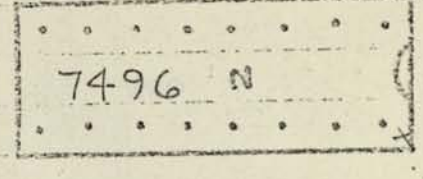
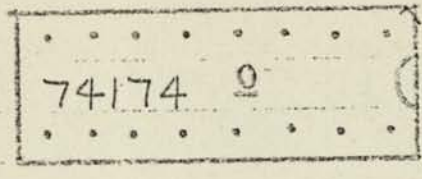
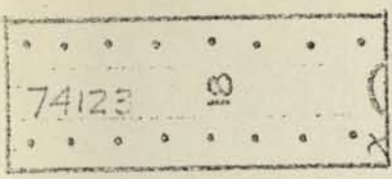
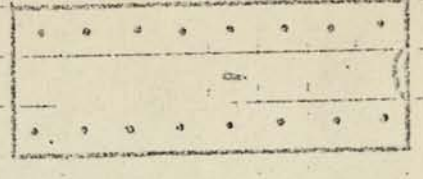
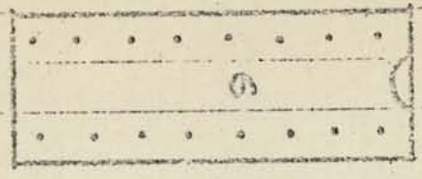
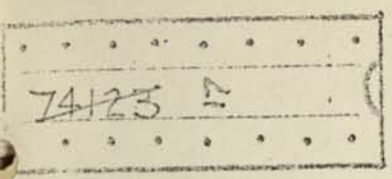
74191 15

7437 7

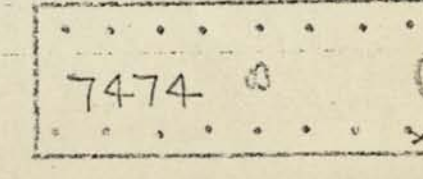
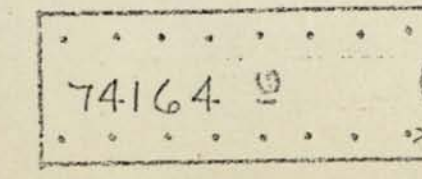
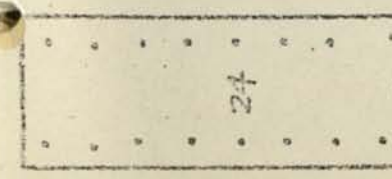
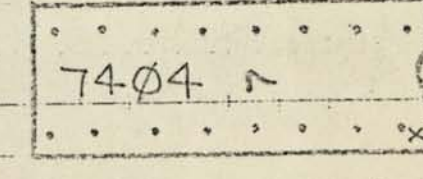
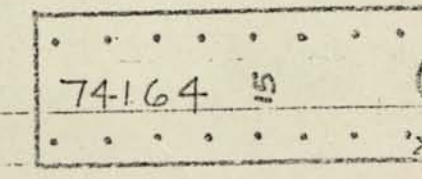
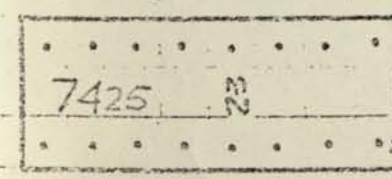
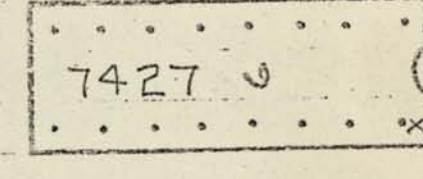
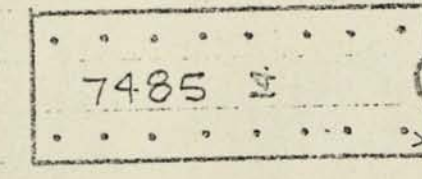
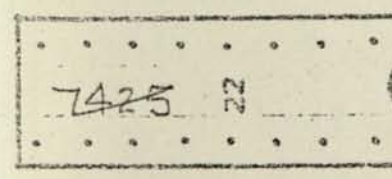
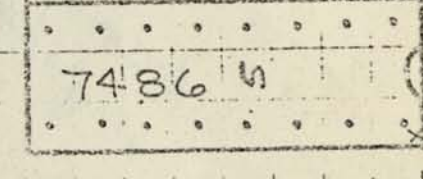
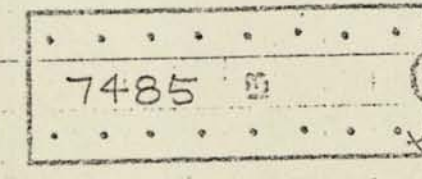
74157 24

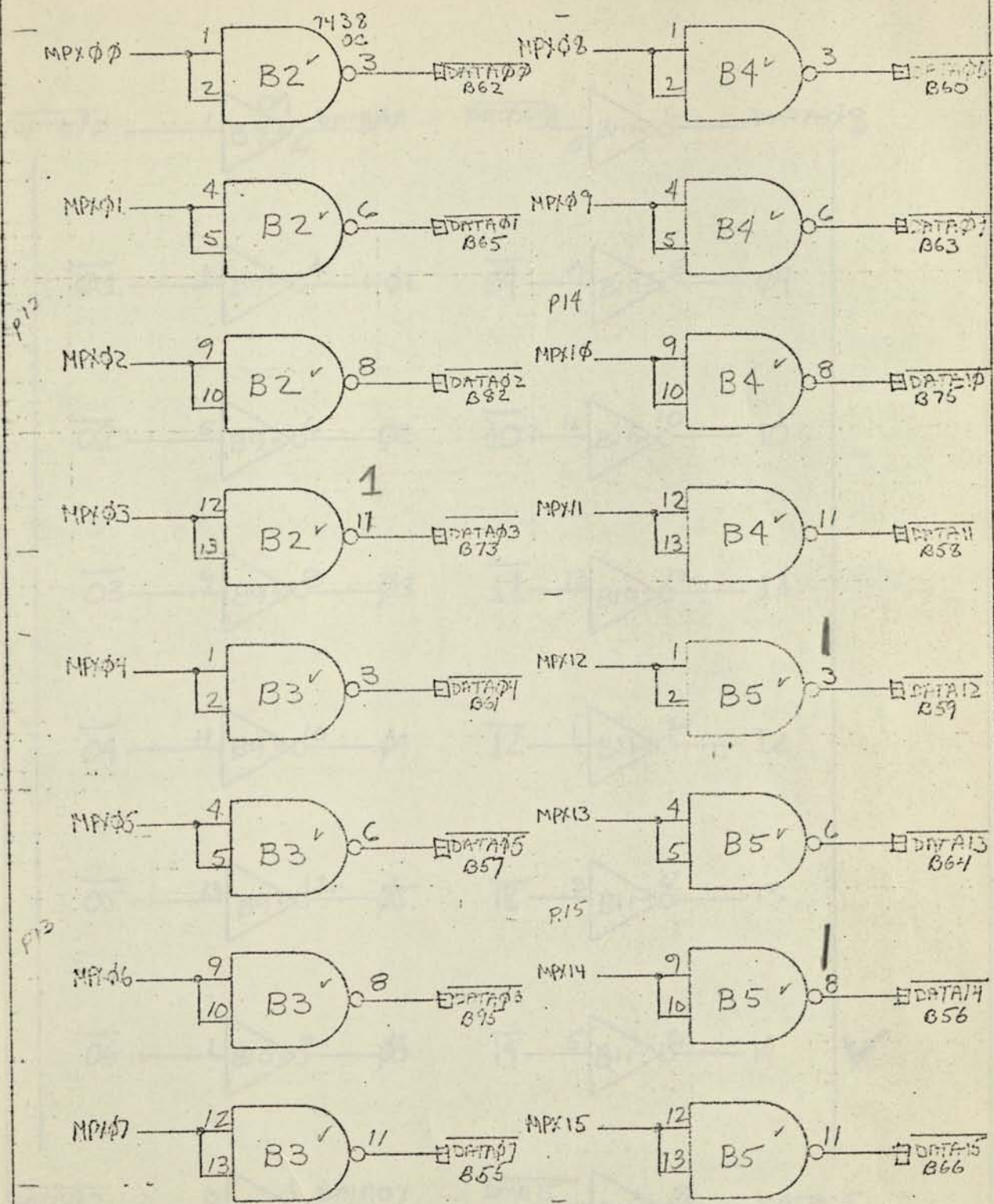
74191 16

7410 8



AMPTS (TOGGLE SWITCH)





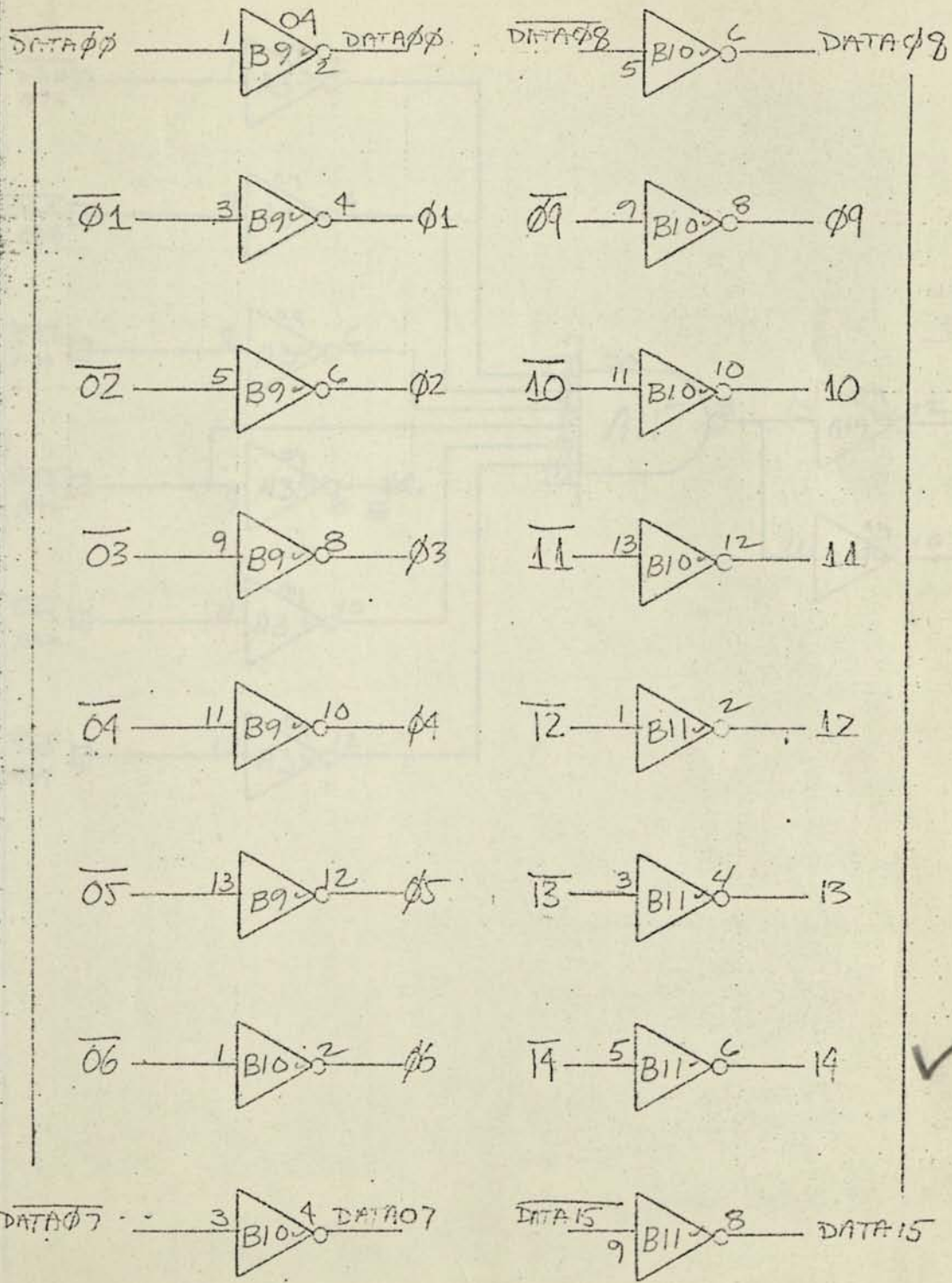
P13

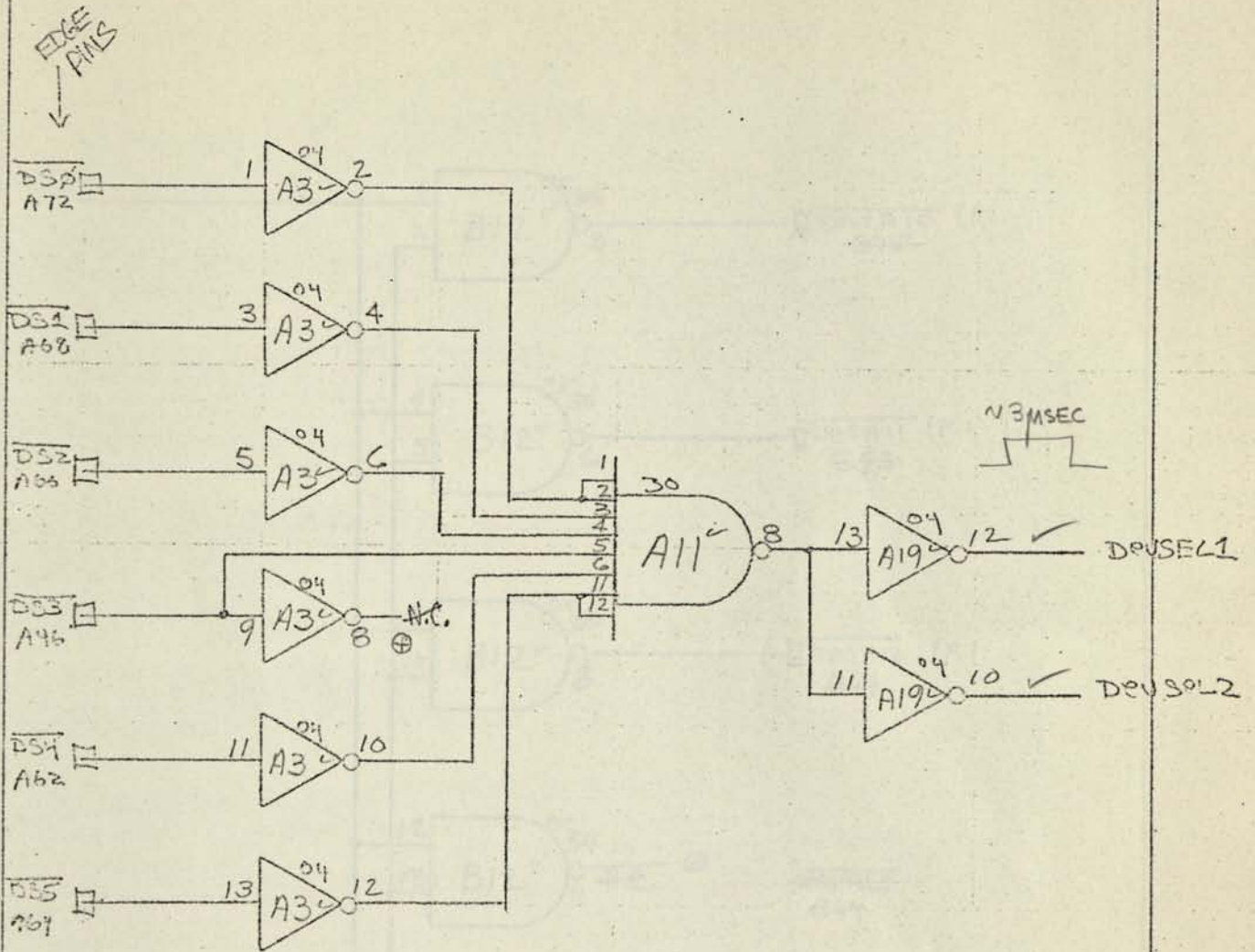
P14

P13

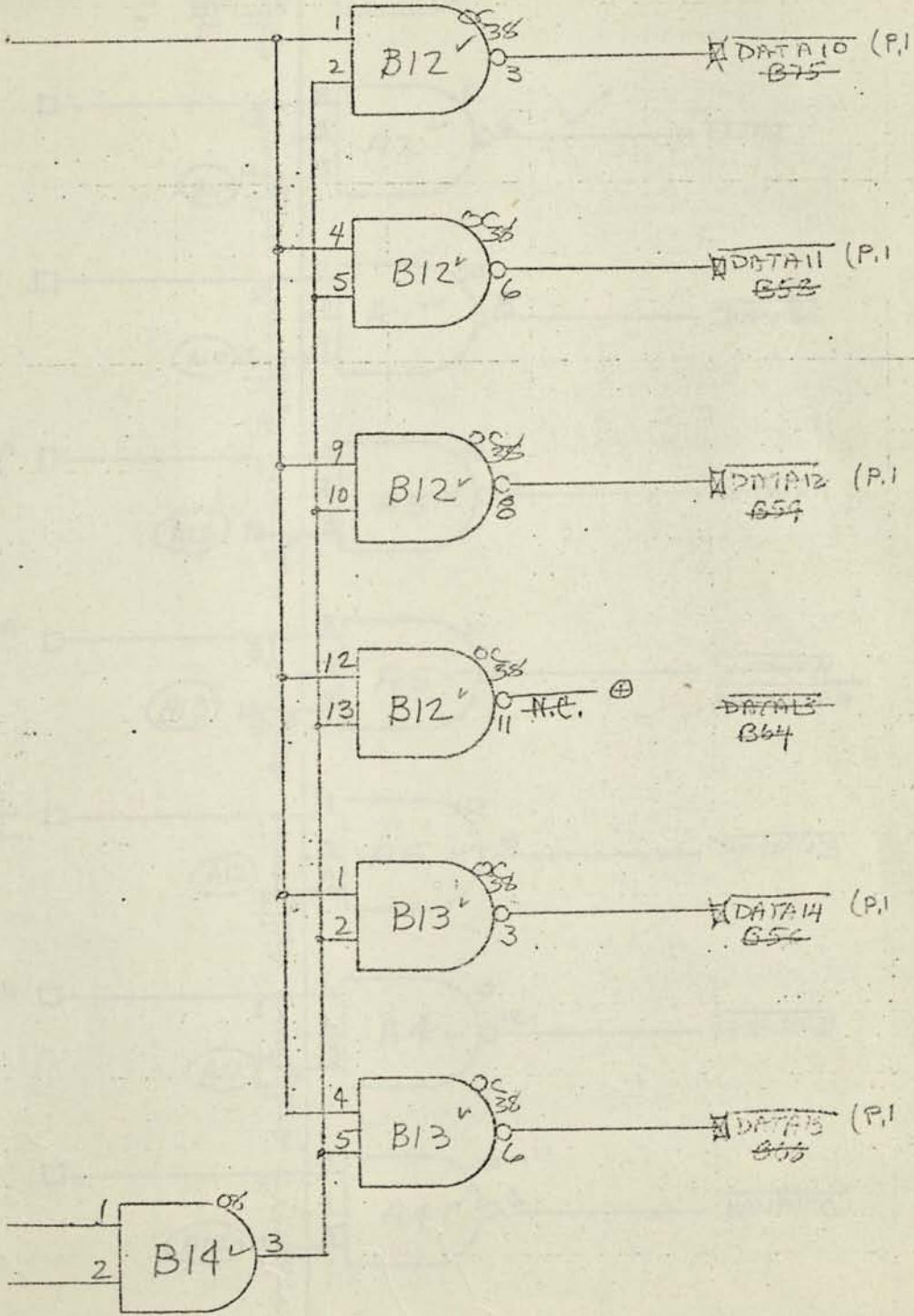
P15

- C16.9 1K C16.8 ONEA
- VCC → [resistor symbol] → C18.13 1K C18.4 ONEB
- F19.2 21K F19.5 ONEC
- VCC → [resistor symbol] → B16.12 1K B16.5 ONED

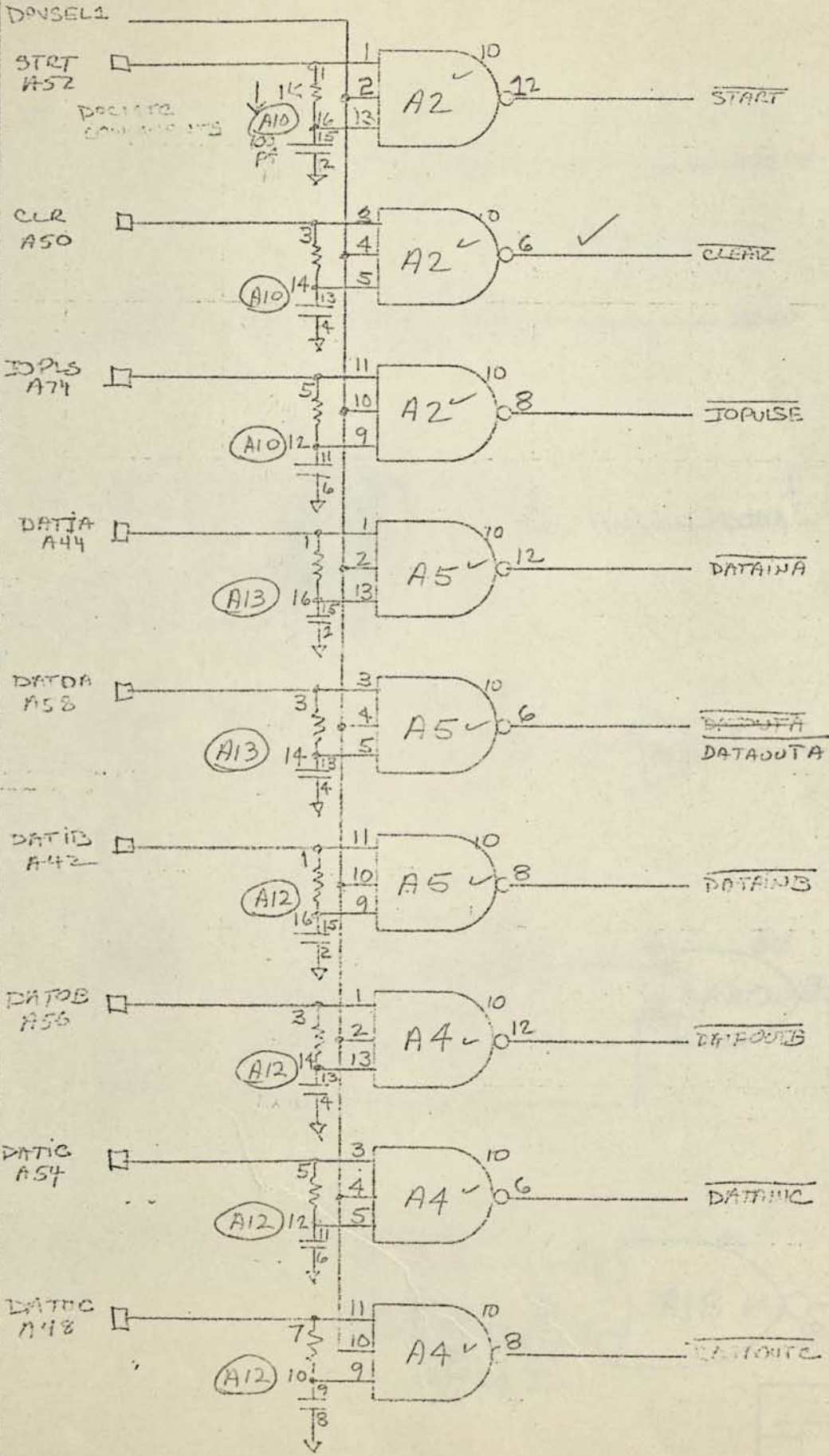


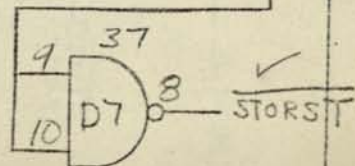
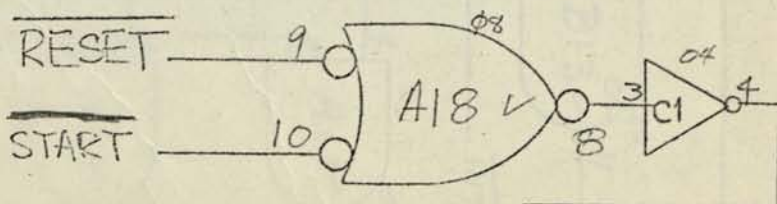
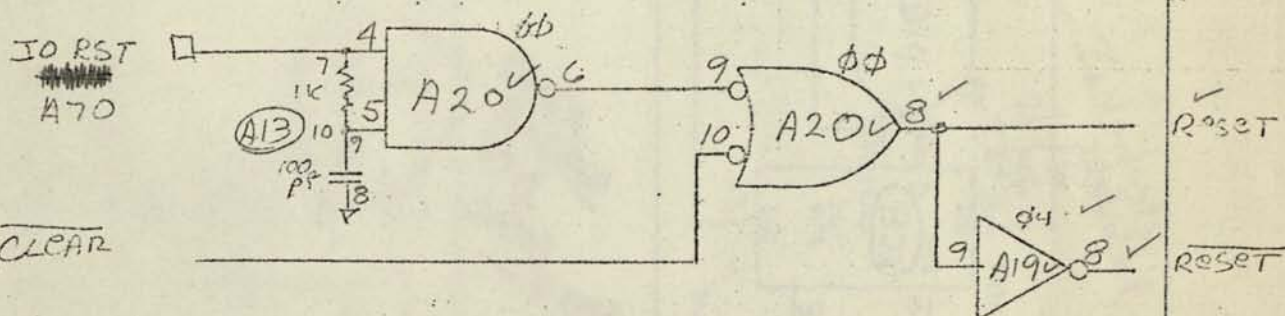
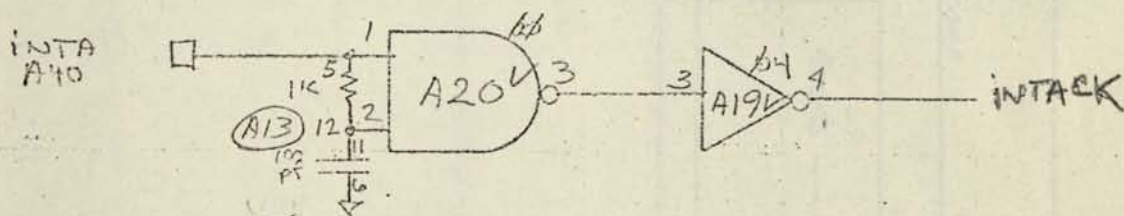
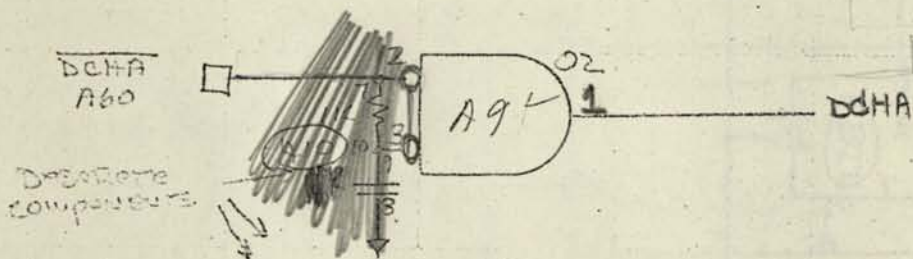
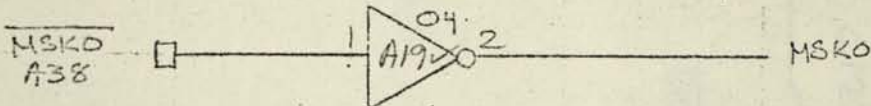
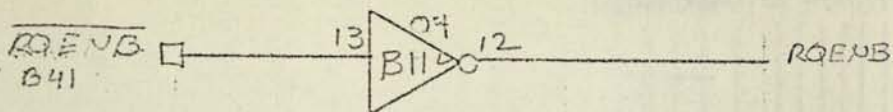


INTRPIN



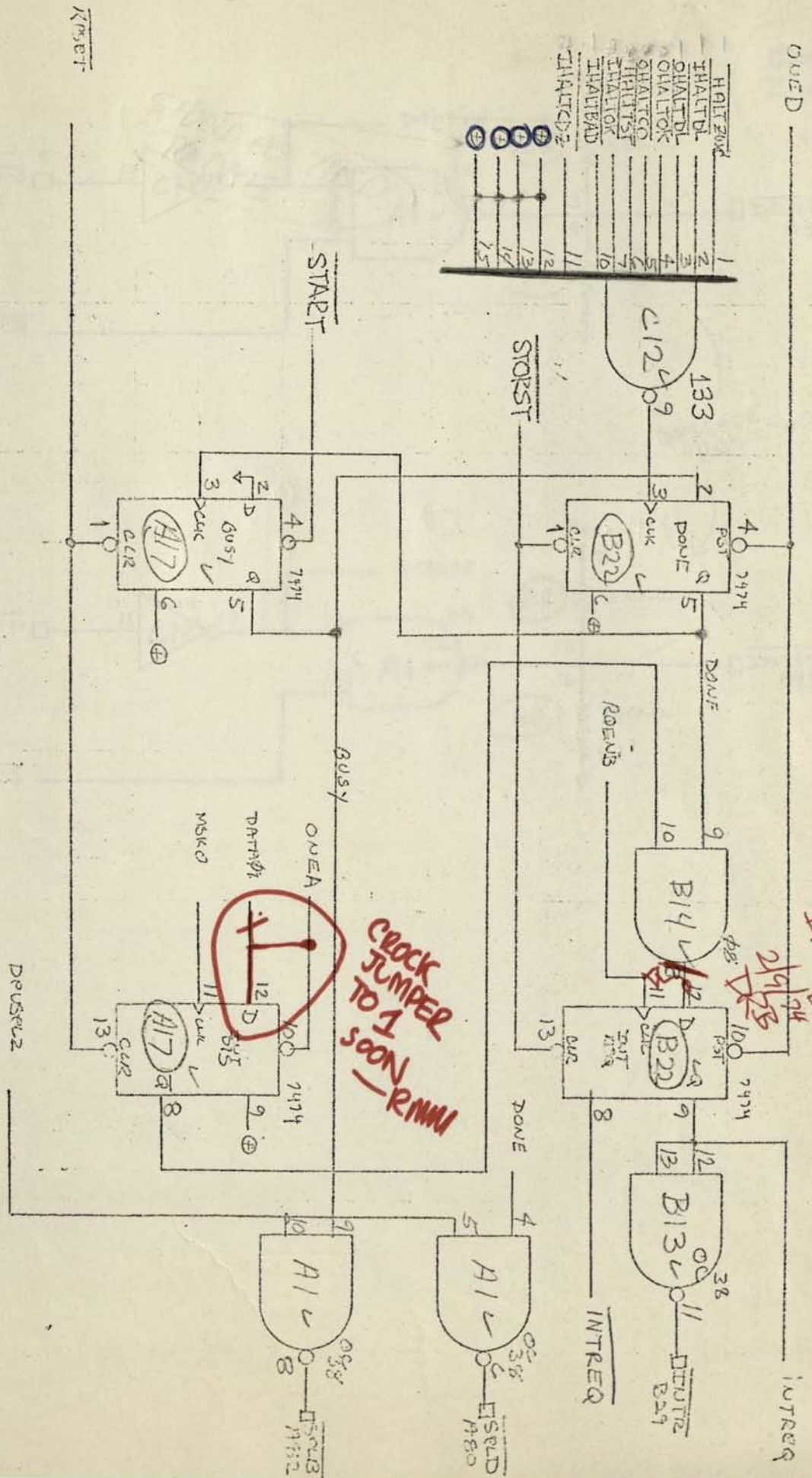
INTRACK
INTRCO



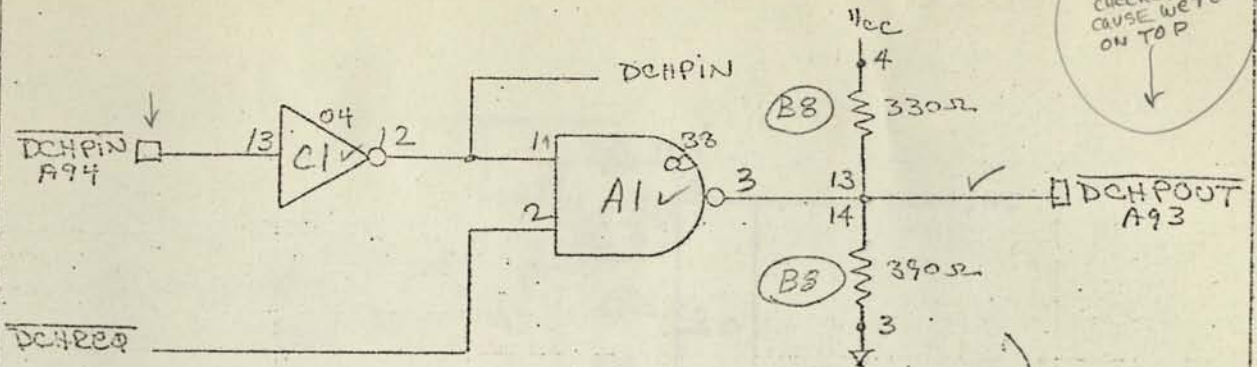


INTERRUPT CONTROL

00 REST
01 WORKING
10 CALLING
11 ←
0005

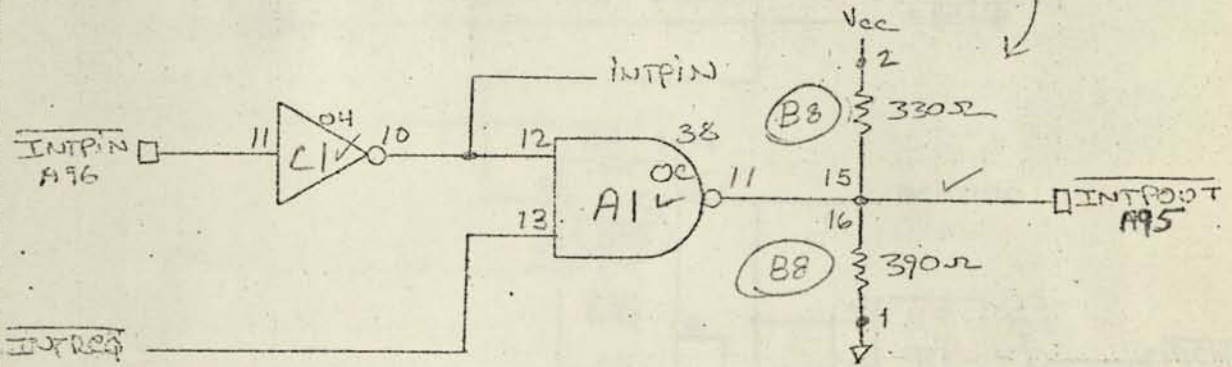


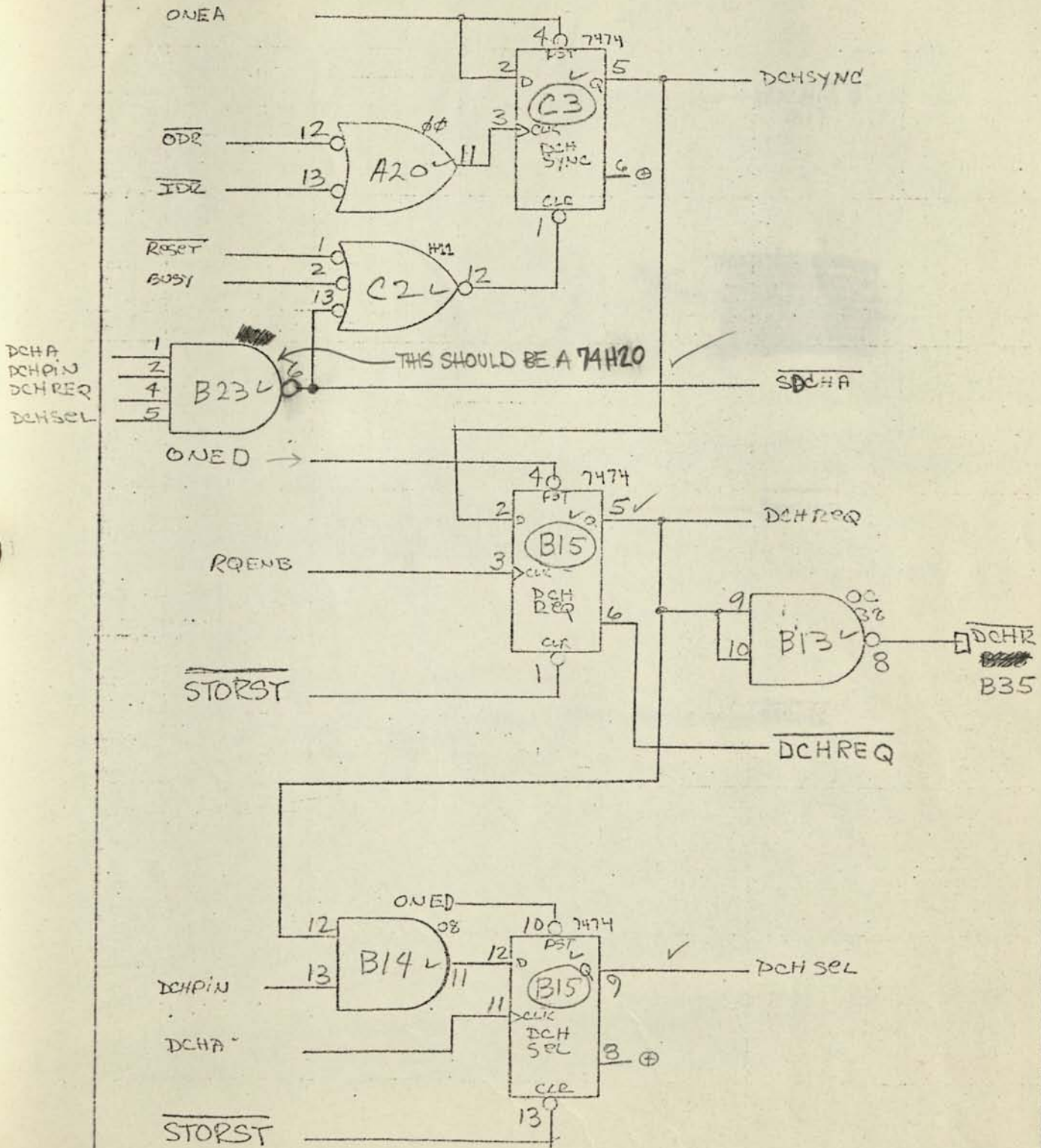
RESET



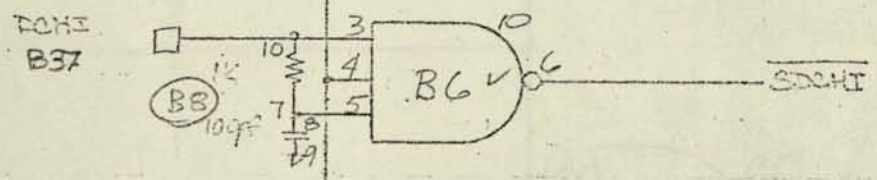
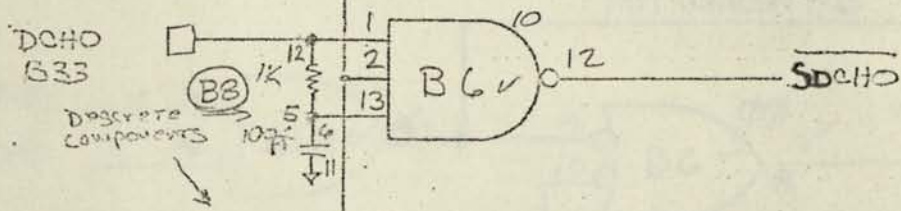
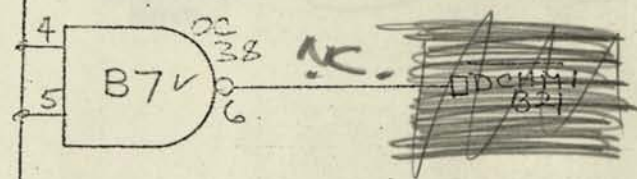
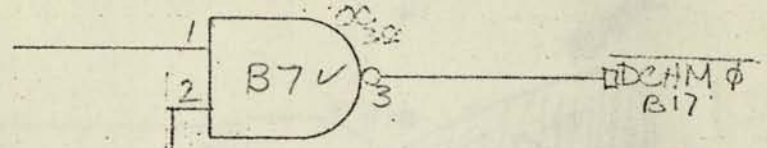
NOT CHECKED AOK
CAUSE WE'RE
ON TOP

DELETE
RESISTORS

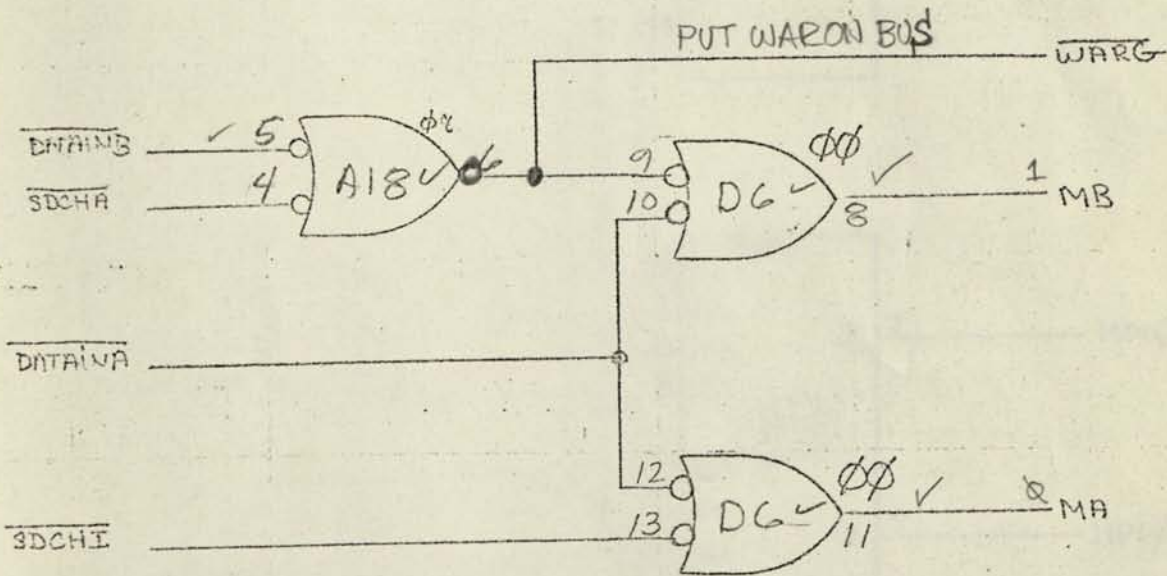
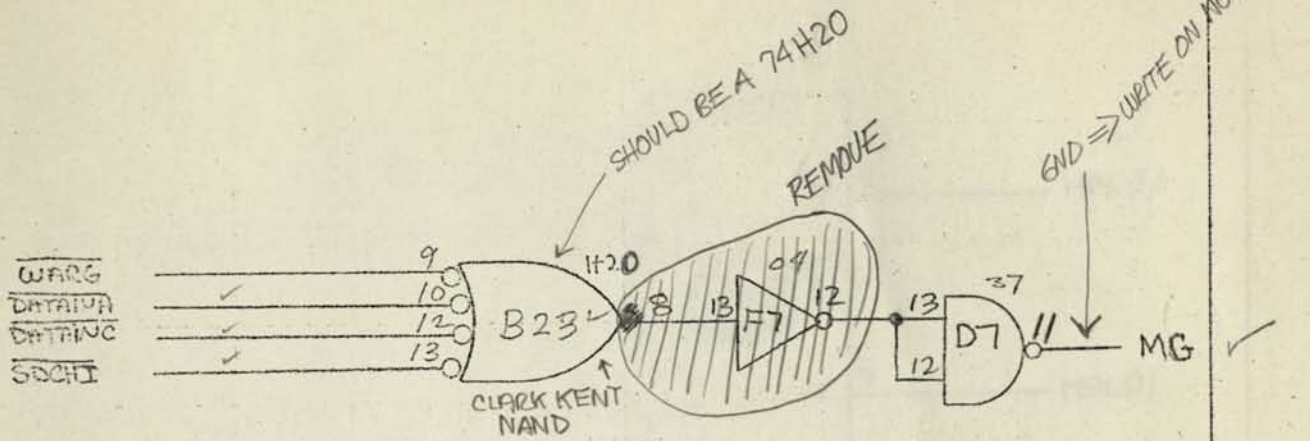




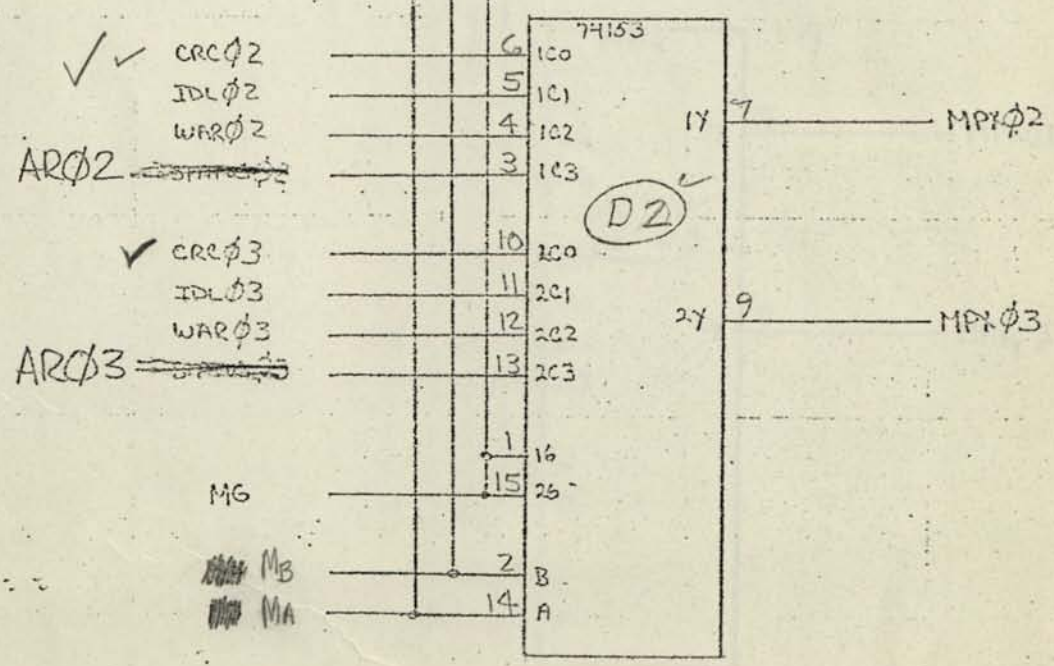
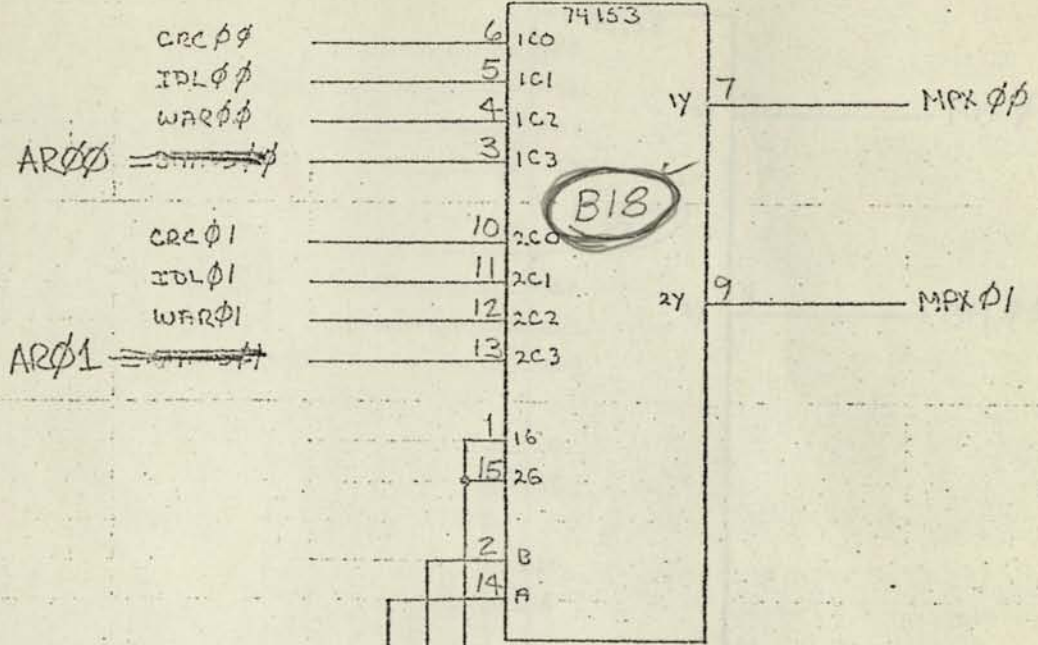
eye = ϕ
oh = 1
~~IO~~
Should be
IO

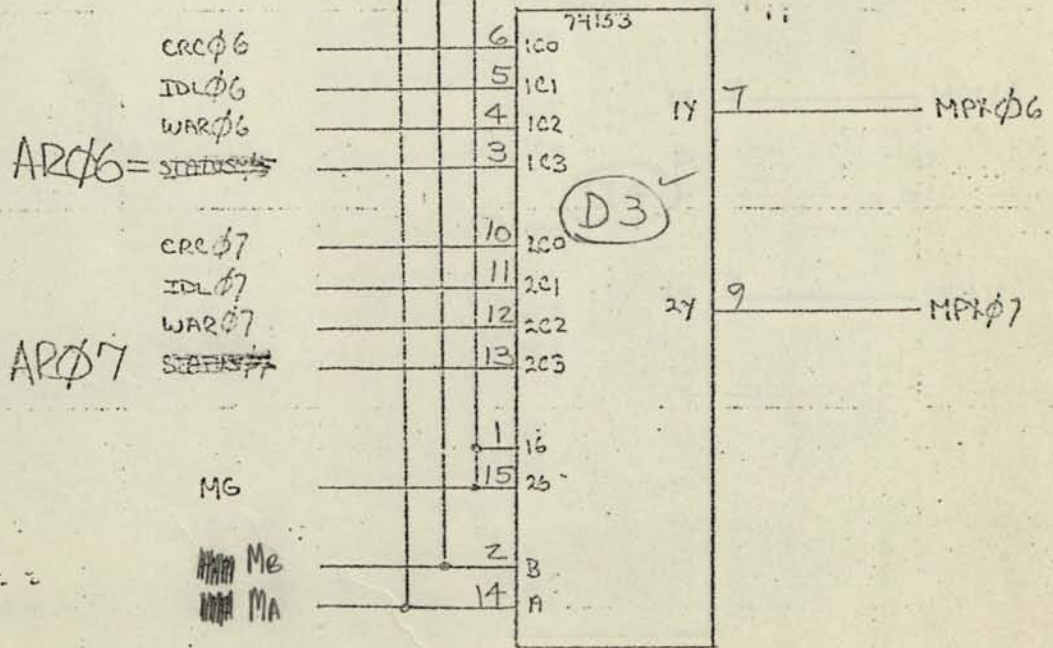
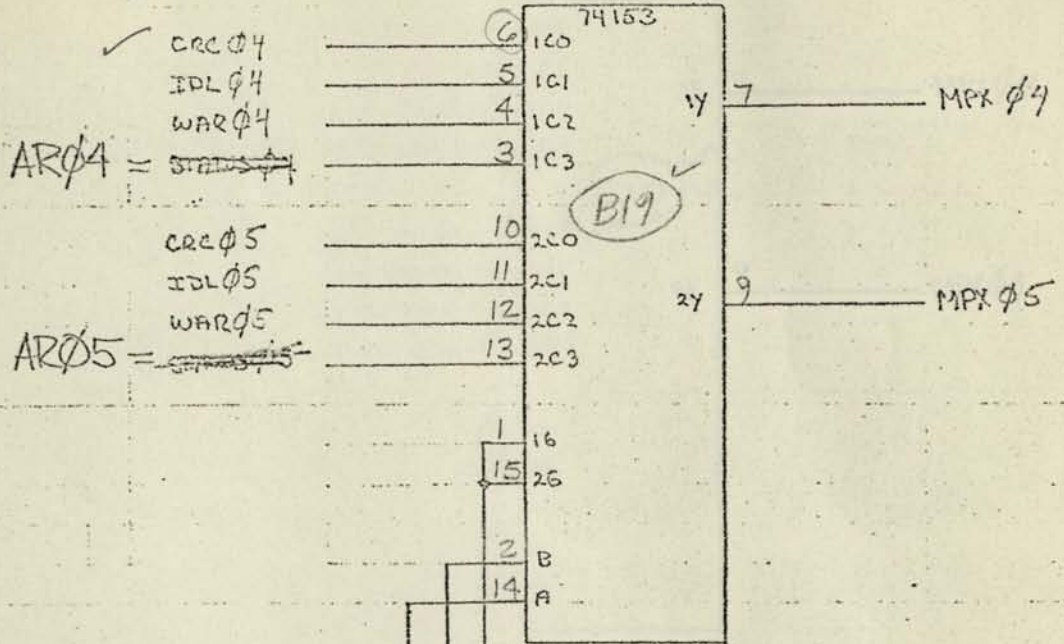


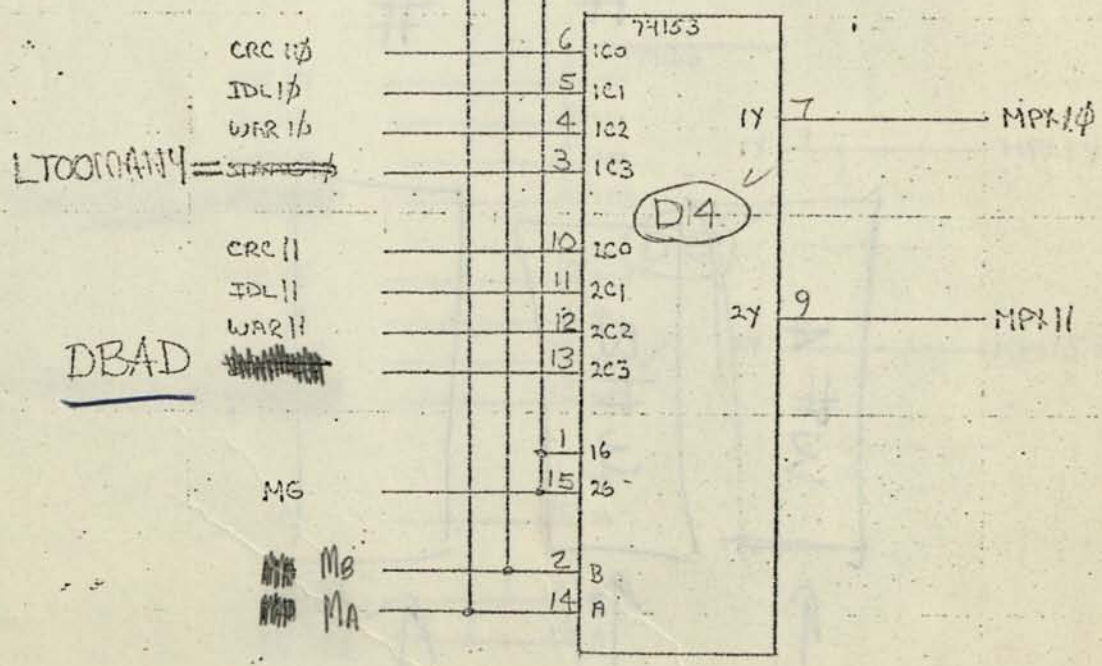
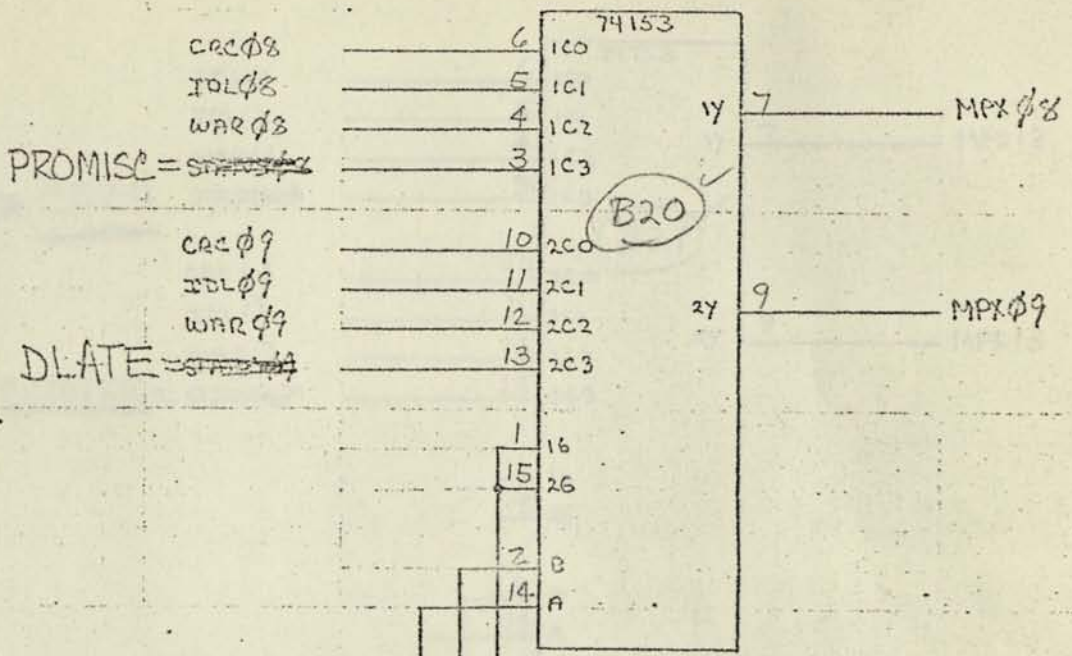
DCHSEL

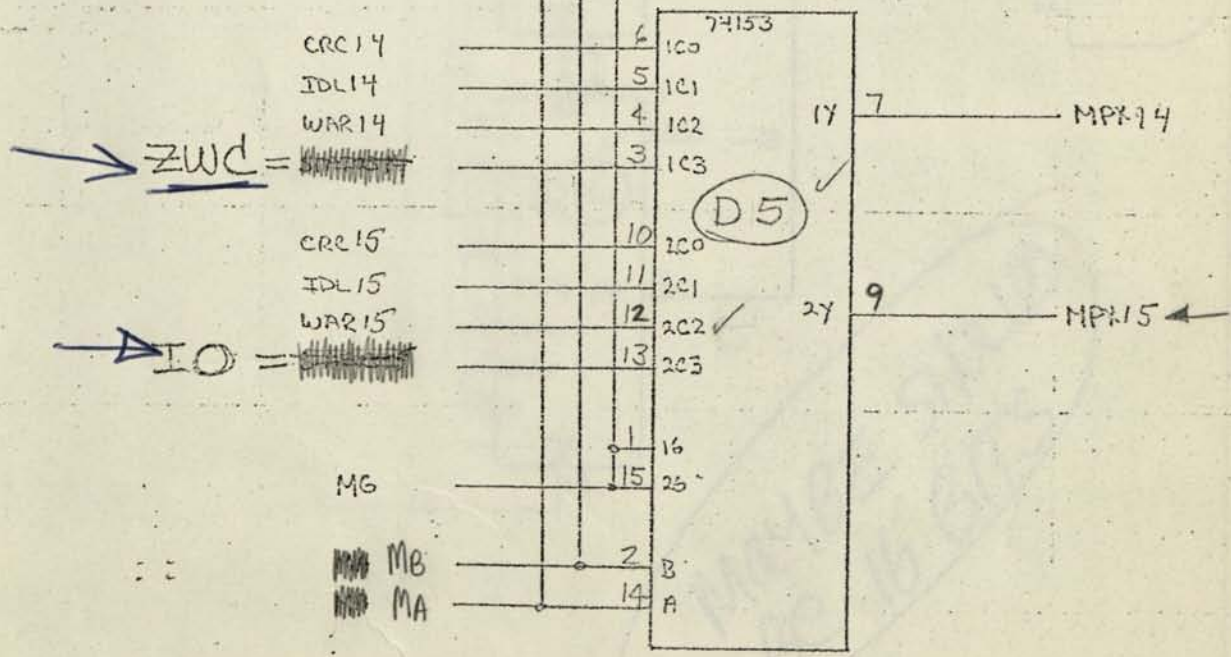
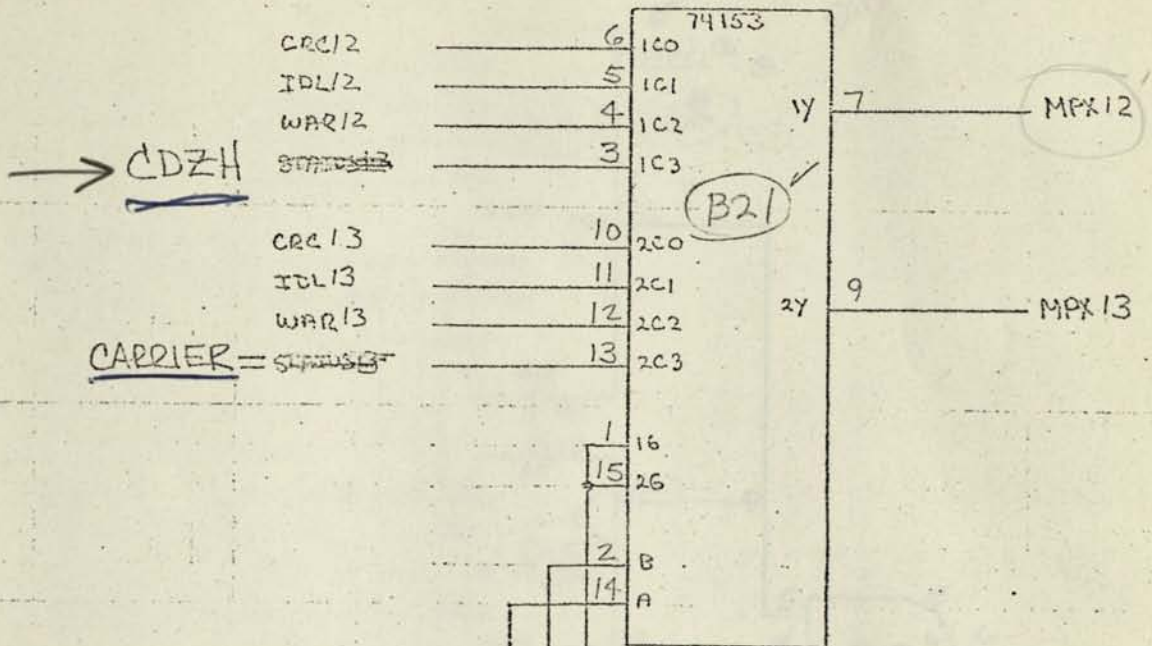


M+BA	OUT
00	CRC, DIC
01	IDL, SDCHI
10	WAR, DATA1B, SDCHA ←
11	STATUS, DIA

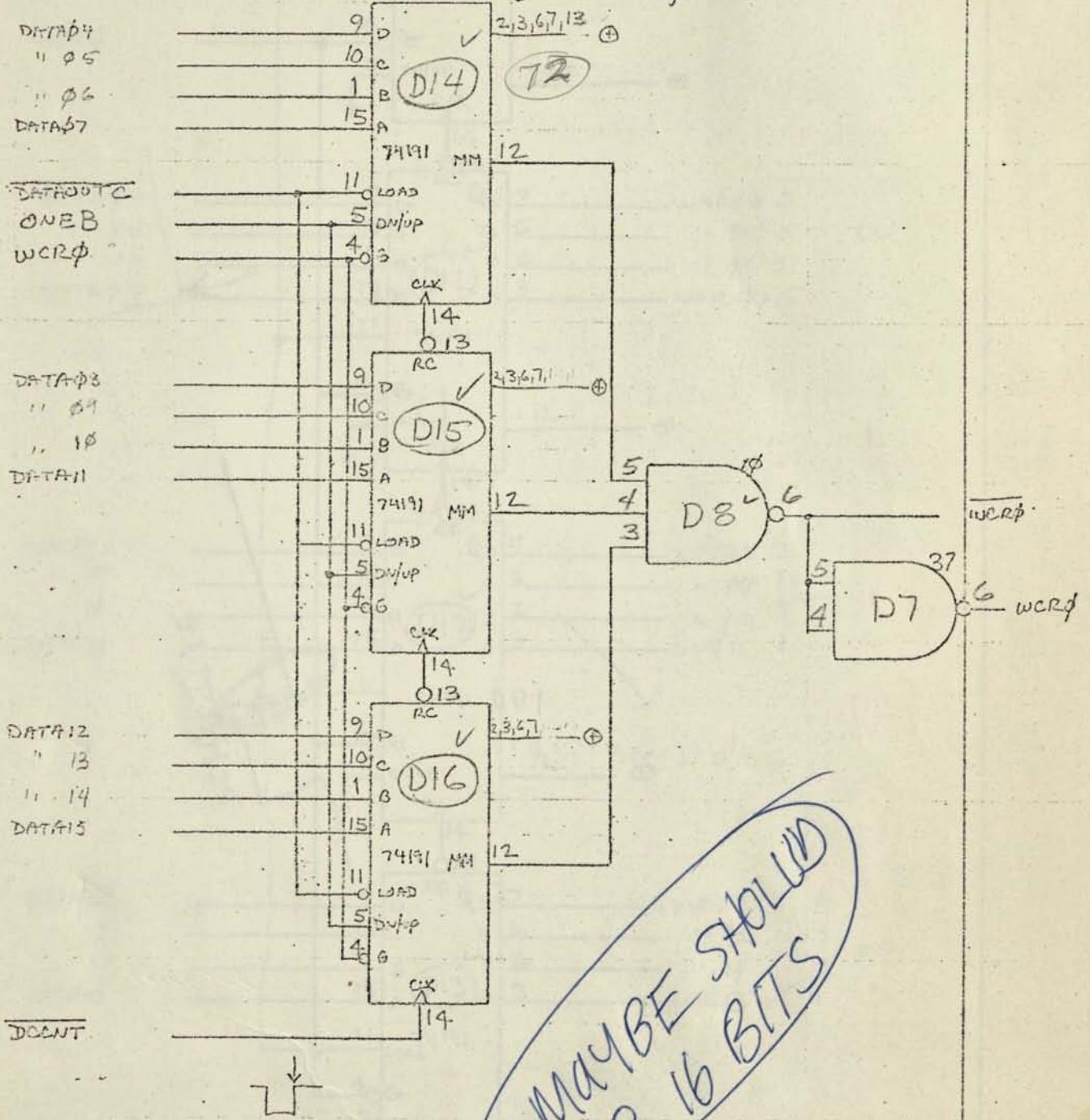




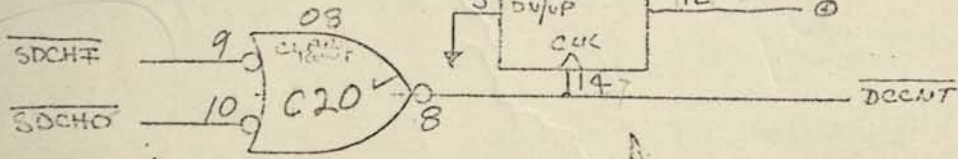
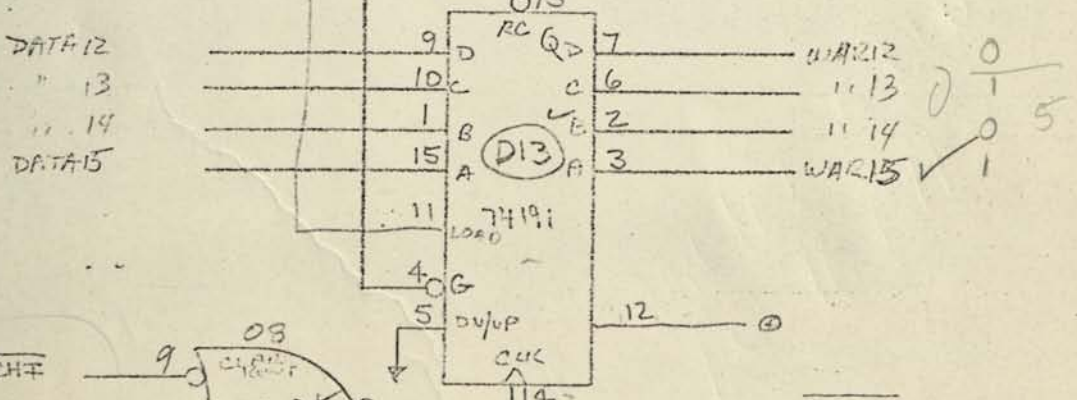
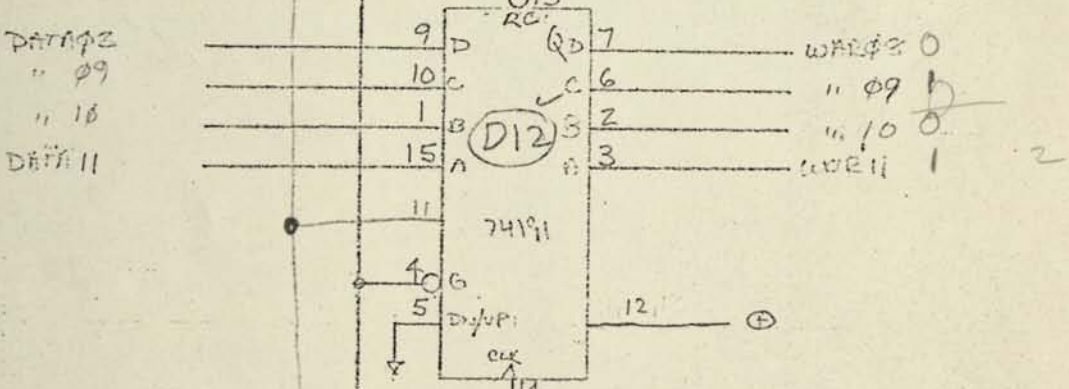
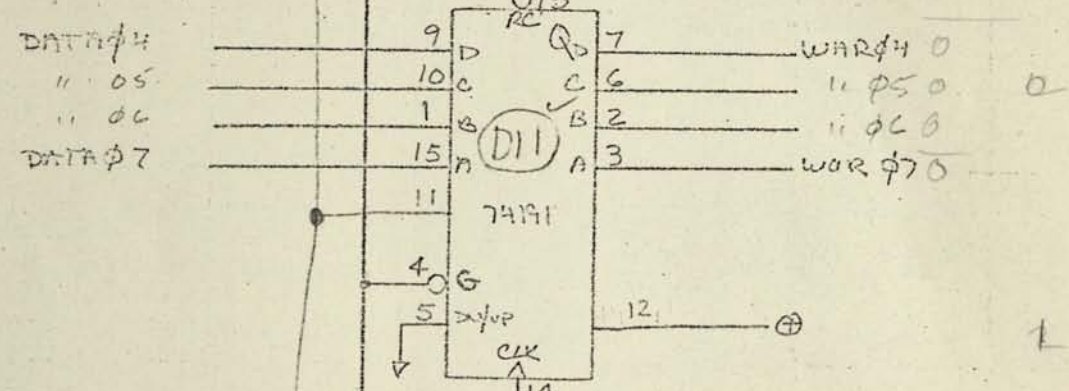
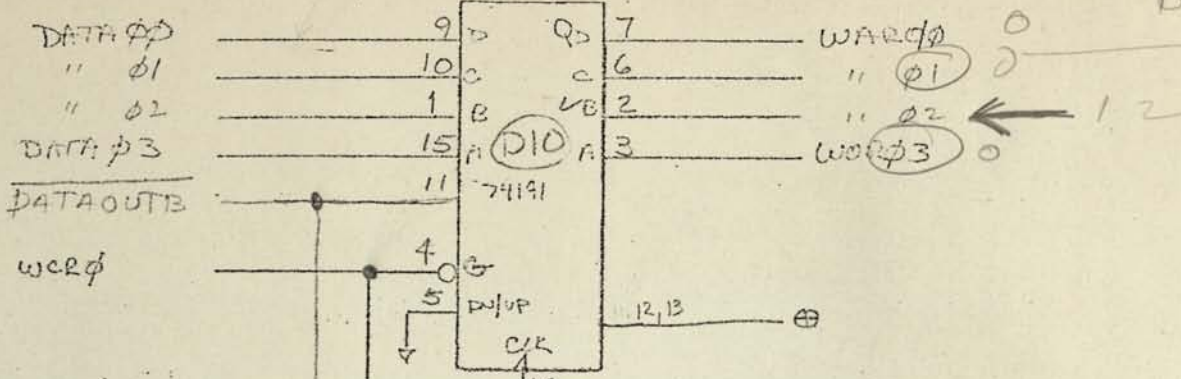




COUNTS DOWN TO ZERO AND STAYS THERE.



MAYBE SHOULD BE 16 BITS



WILL NOT COUNT UP IF WCR IS ZERO (0000).

0
0
1 2
0

0
0
0
0

1

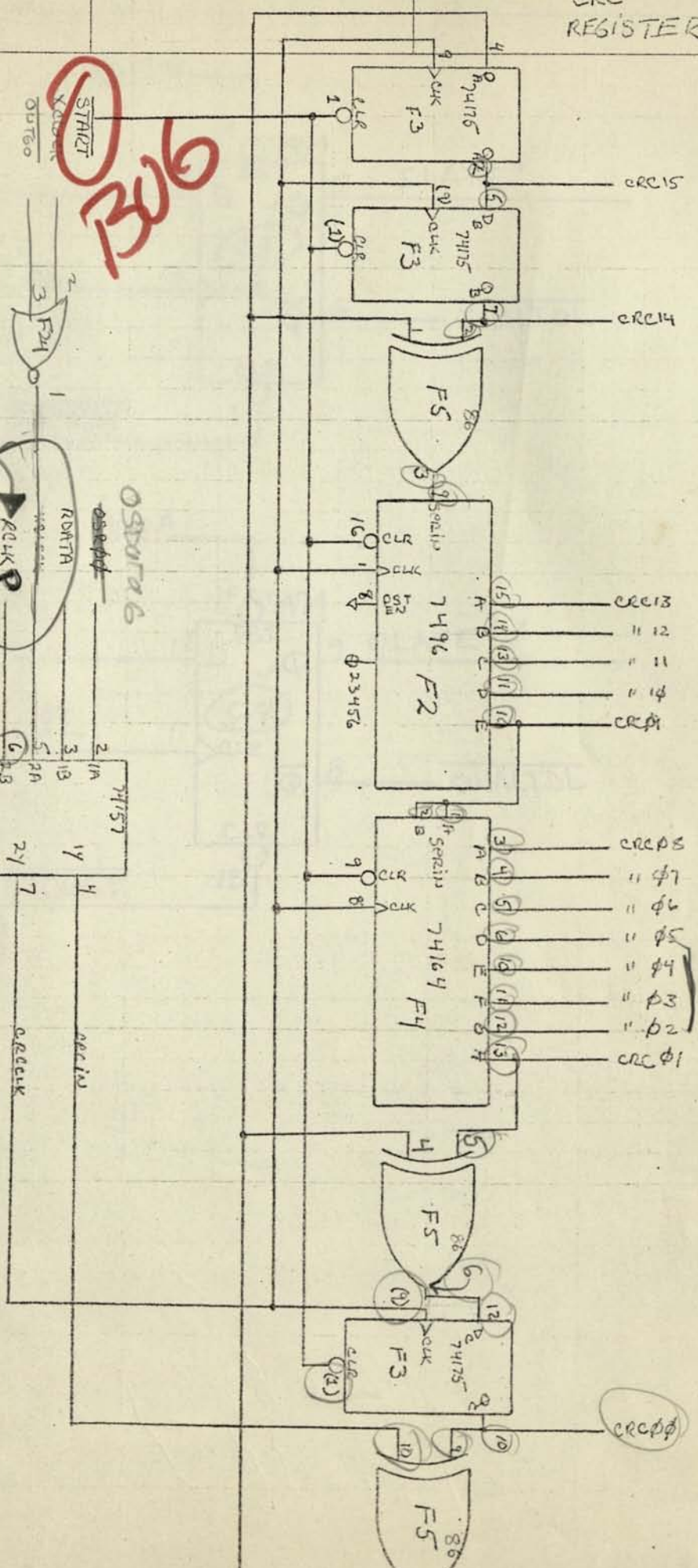
2

0
1
5
1

136113

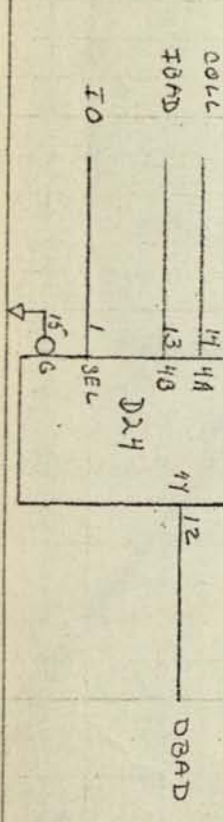
$X^{16} + X^{15} + X^2 + 1$

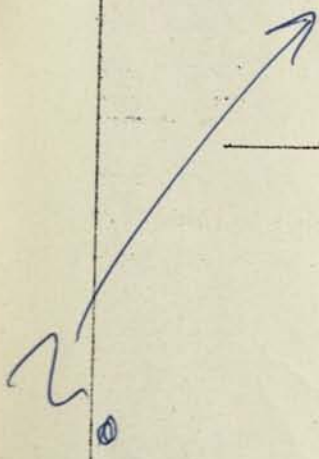
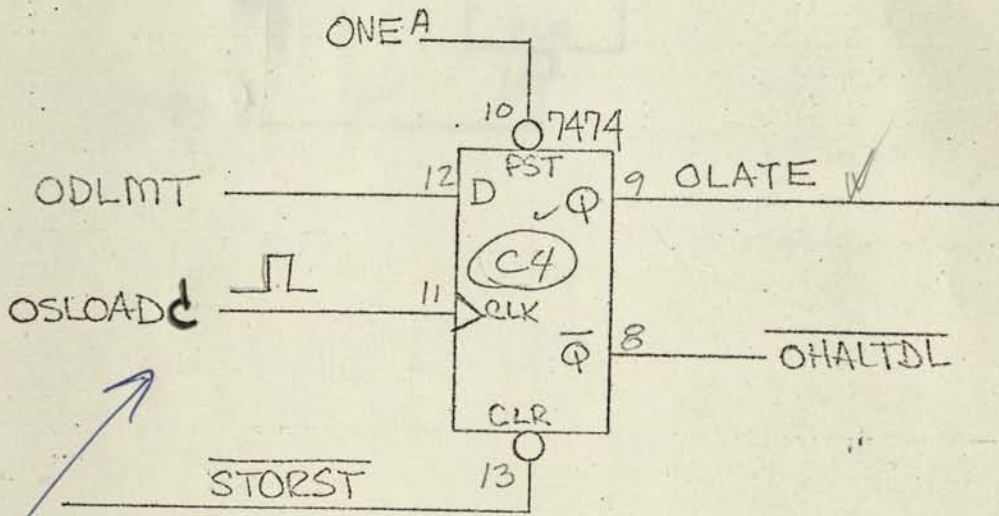
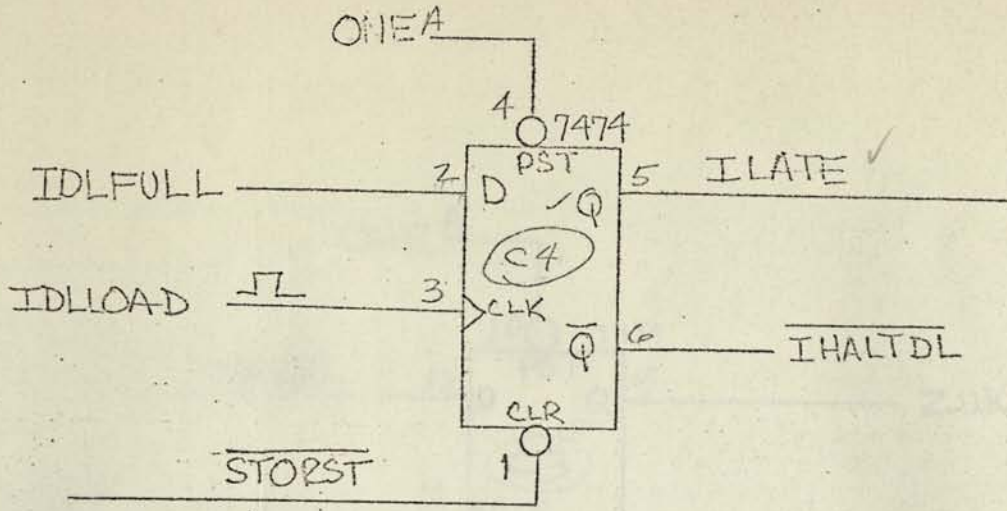
CRC REGISTER

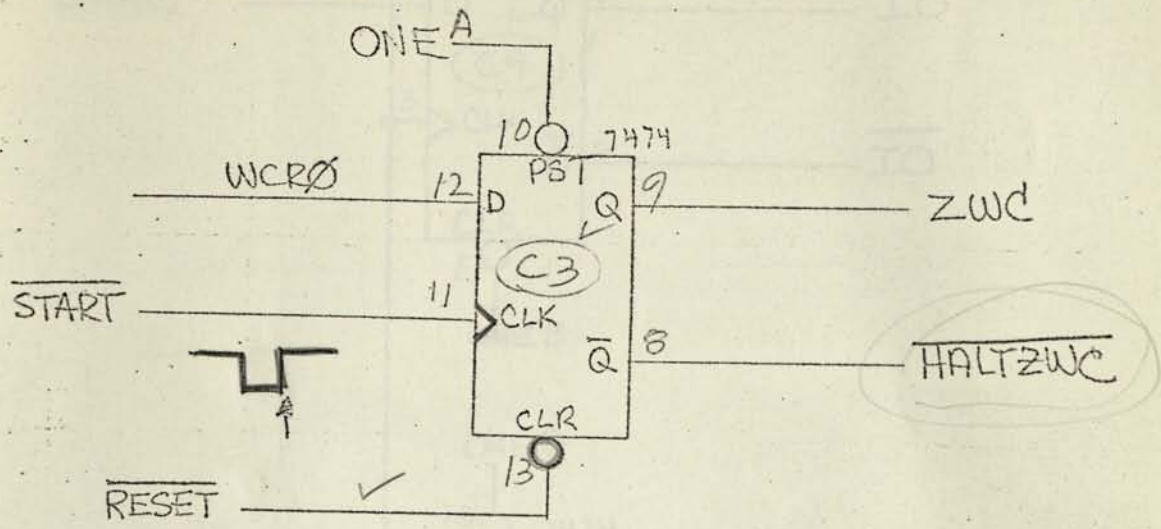


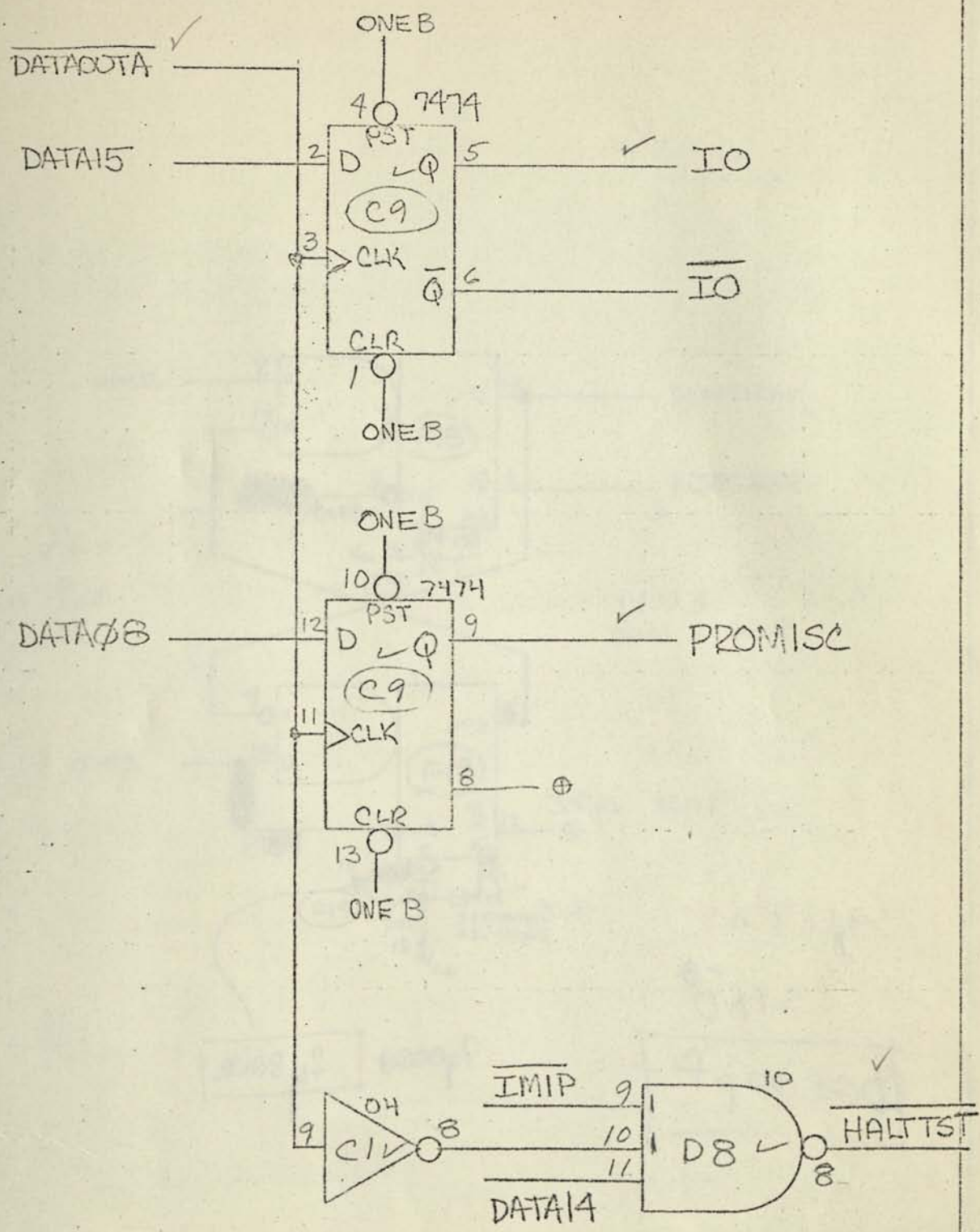
9361

DATA

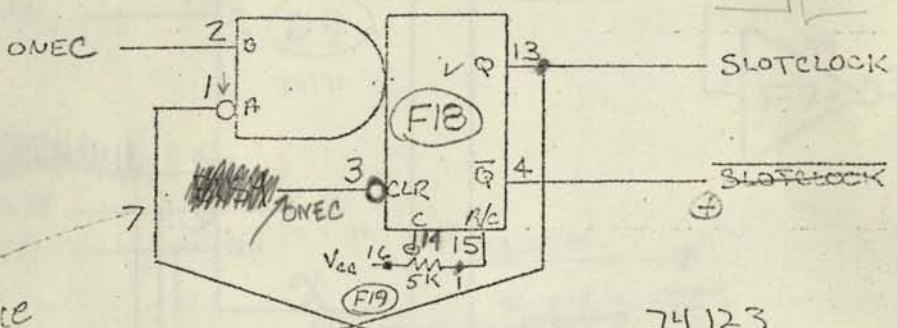






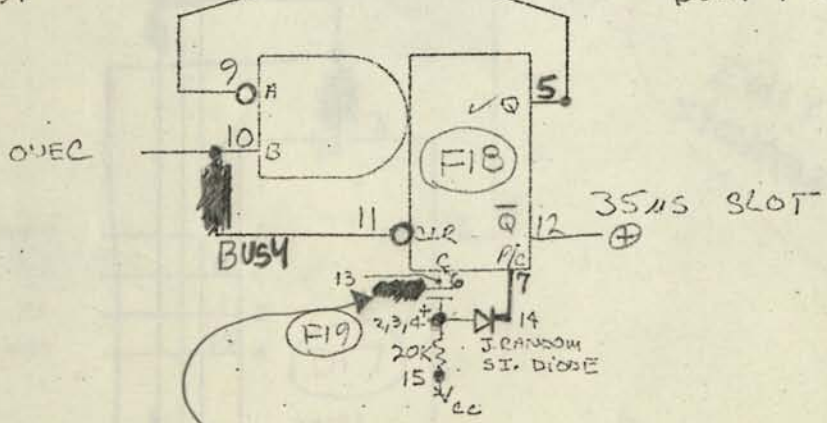


HALTS INPUT
IF NO MESSAGE
IN PROGRESS.
DONE! IF BUSY.

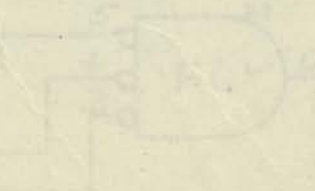


74123
Dual 1-SHOT

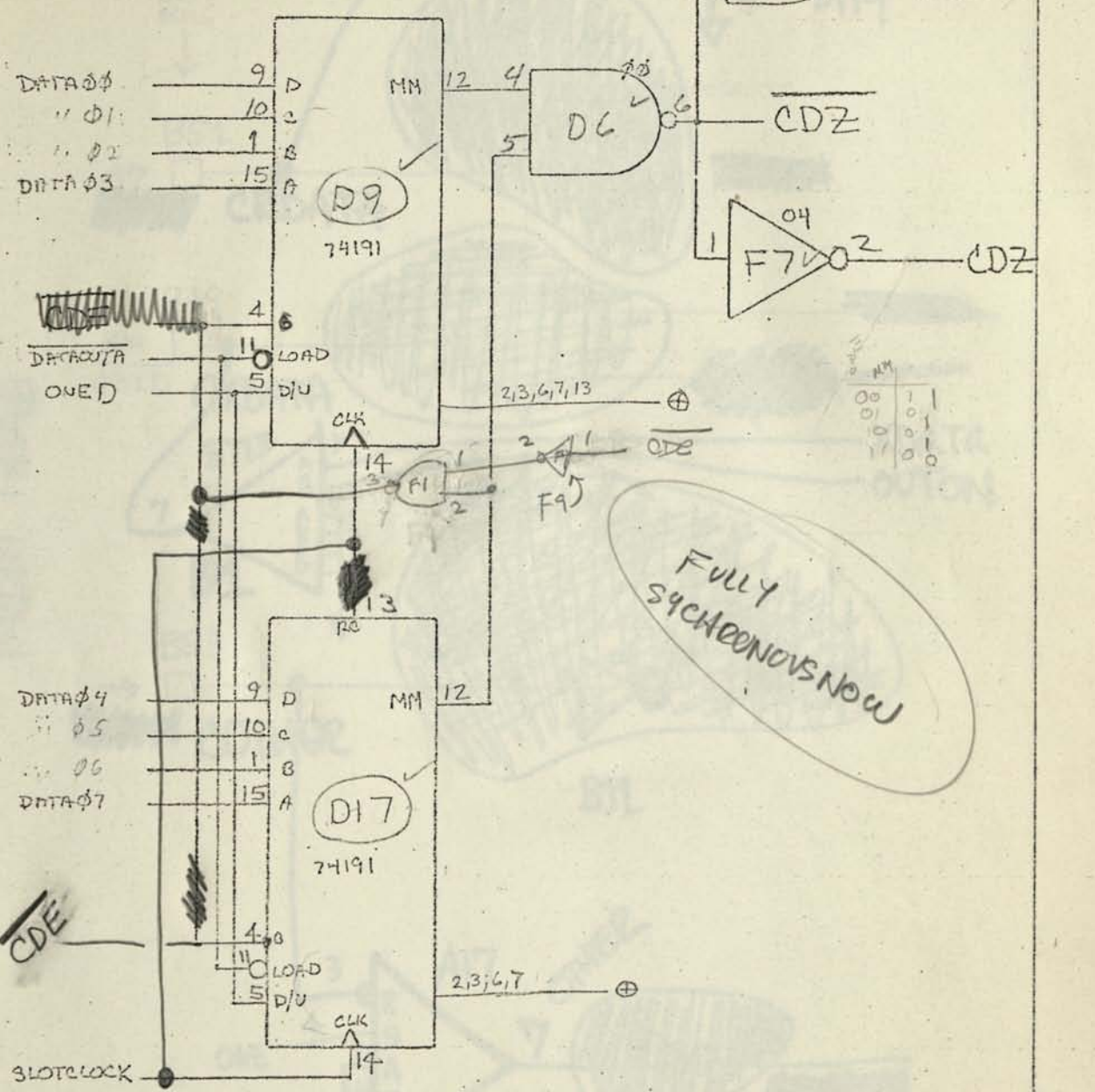
✓
ONLY TICs
WHEN DEVICE
IS BUSY



.0068 µf 6800pf

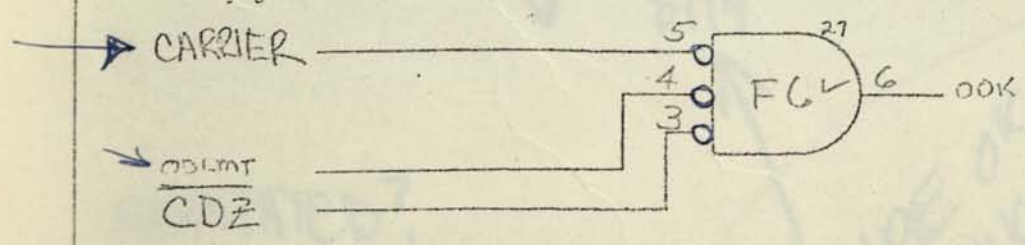


CARRIER

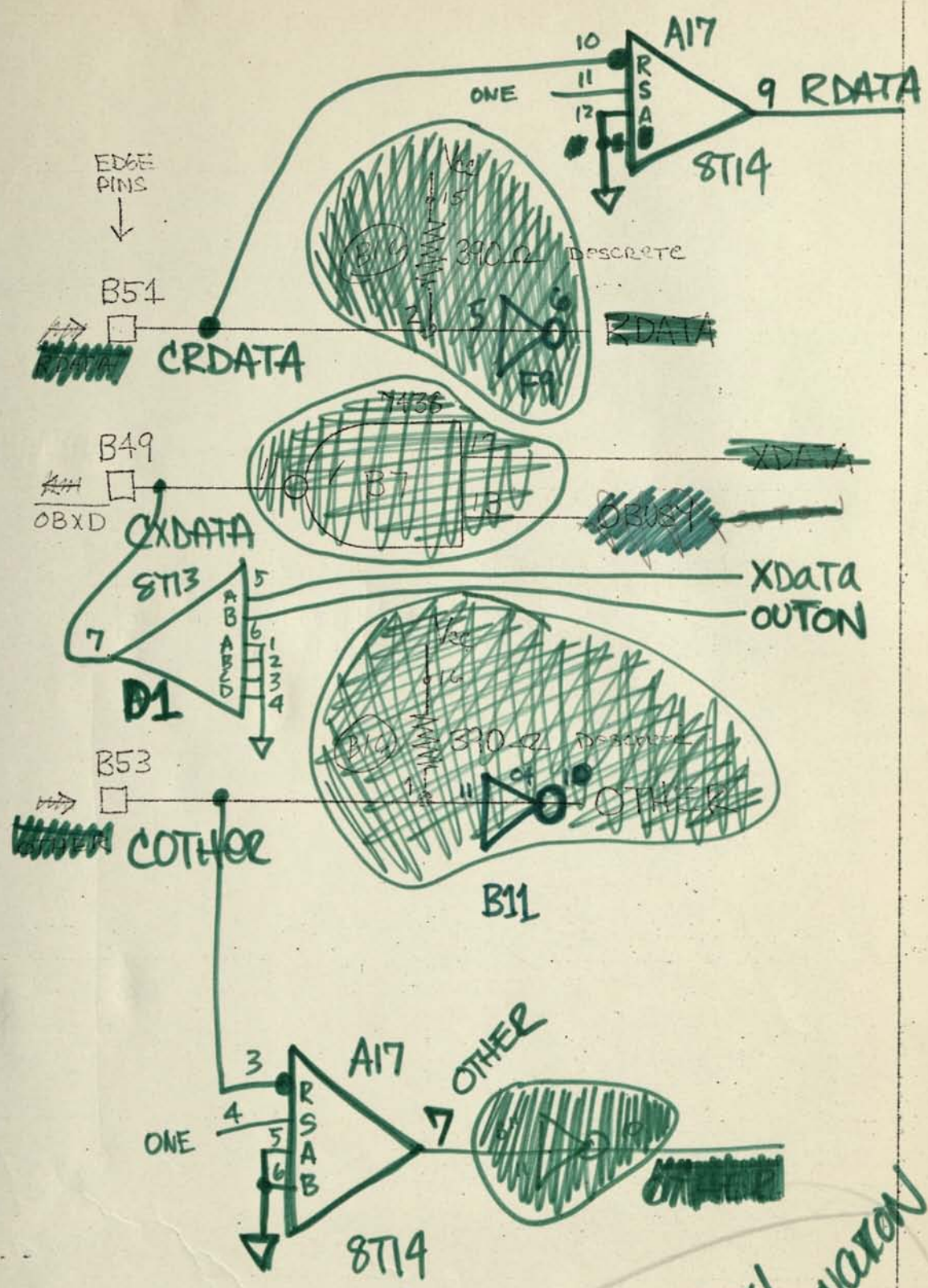


00	1
01	0
10	1
11	0

FULLY SYNCHRONOUS NOW



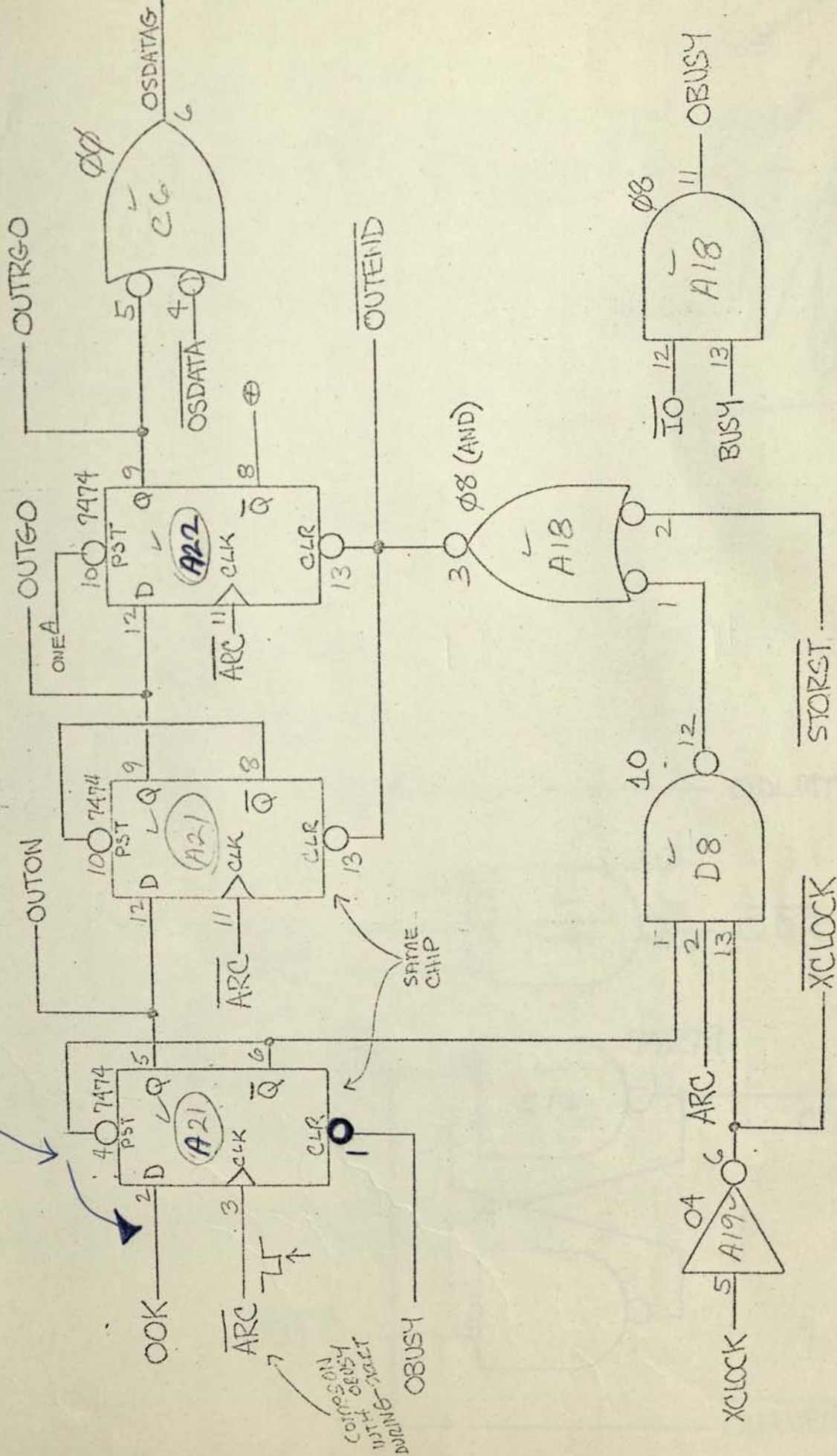
FROM HEAD

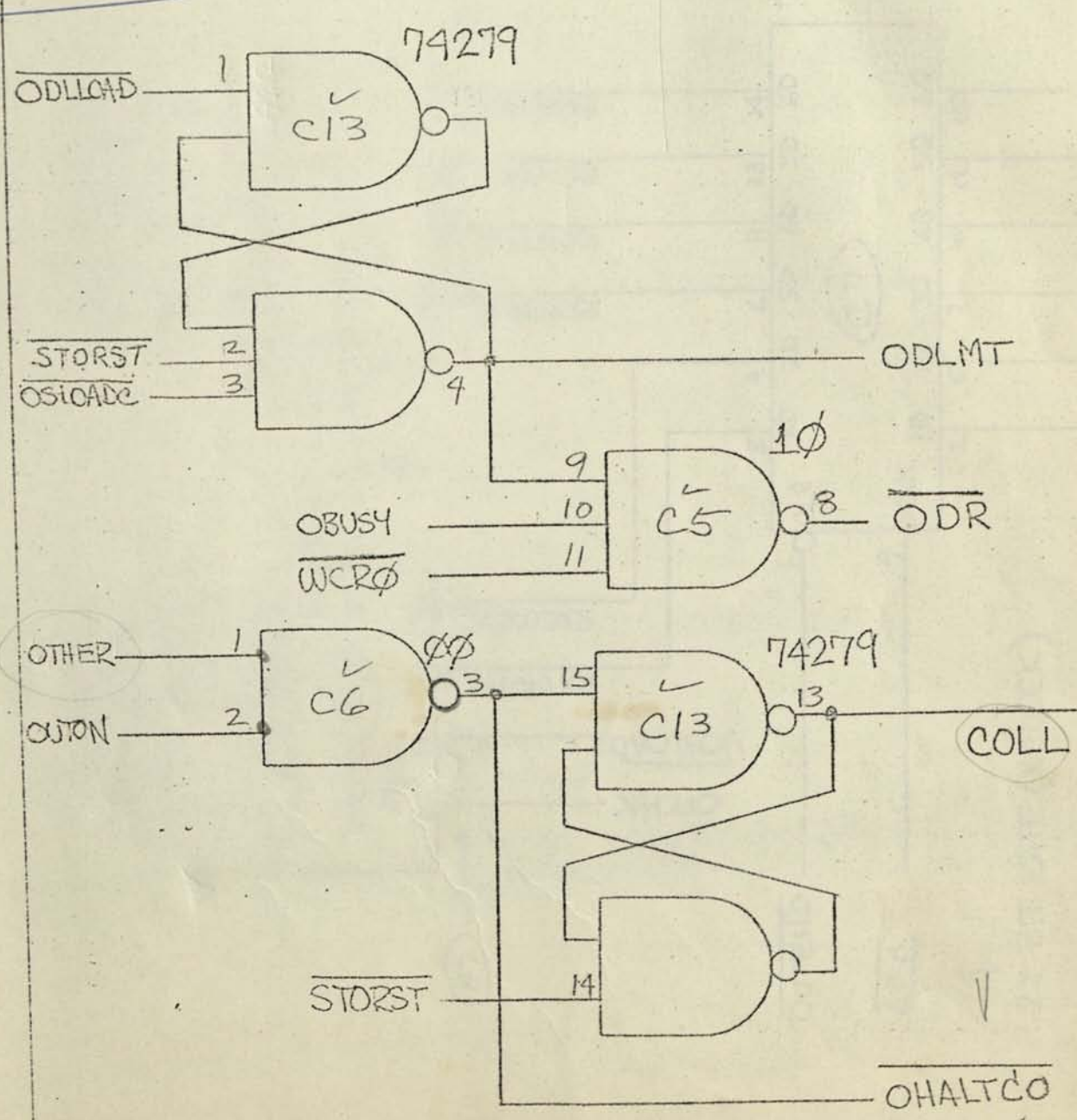
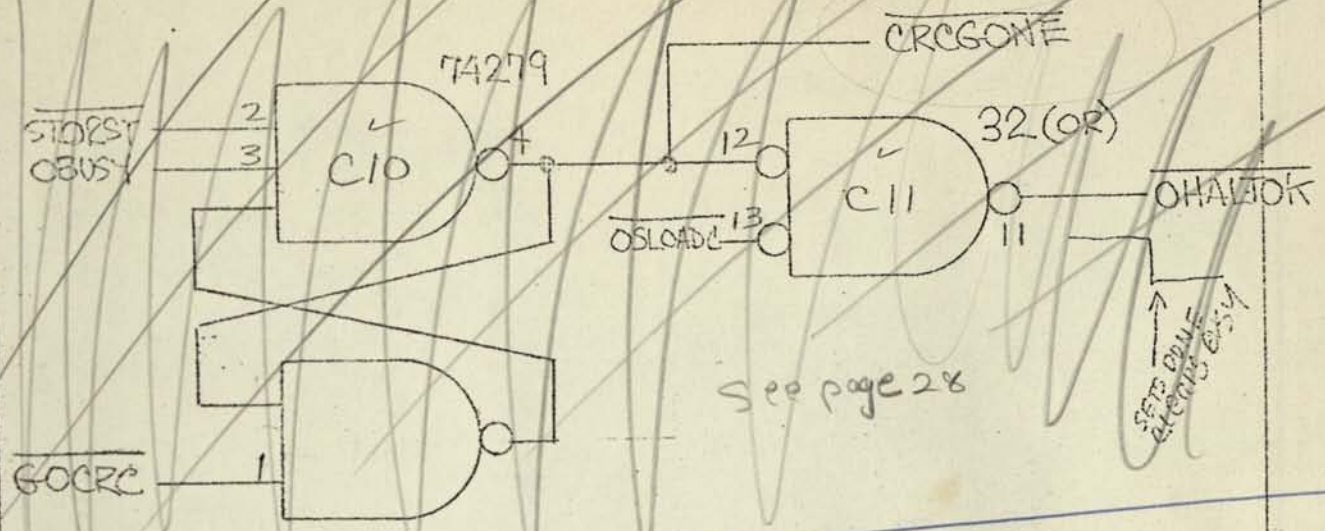


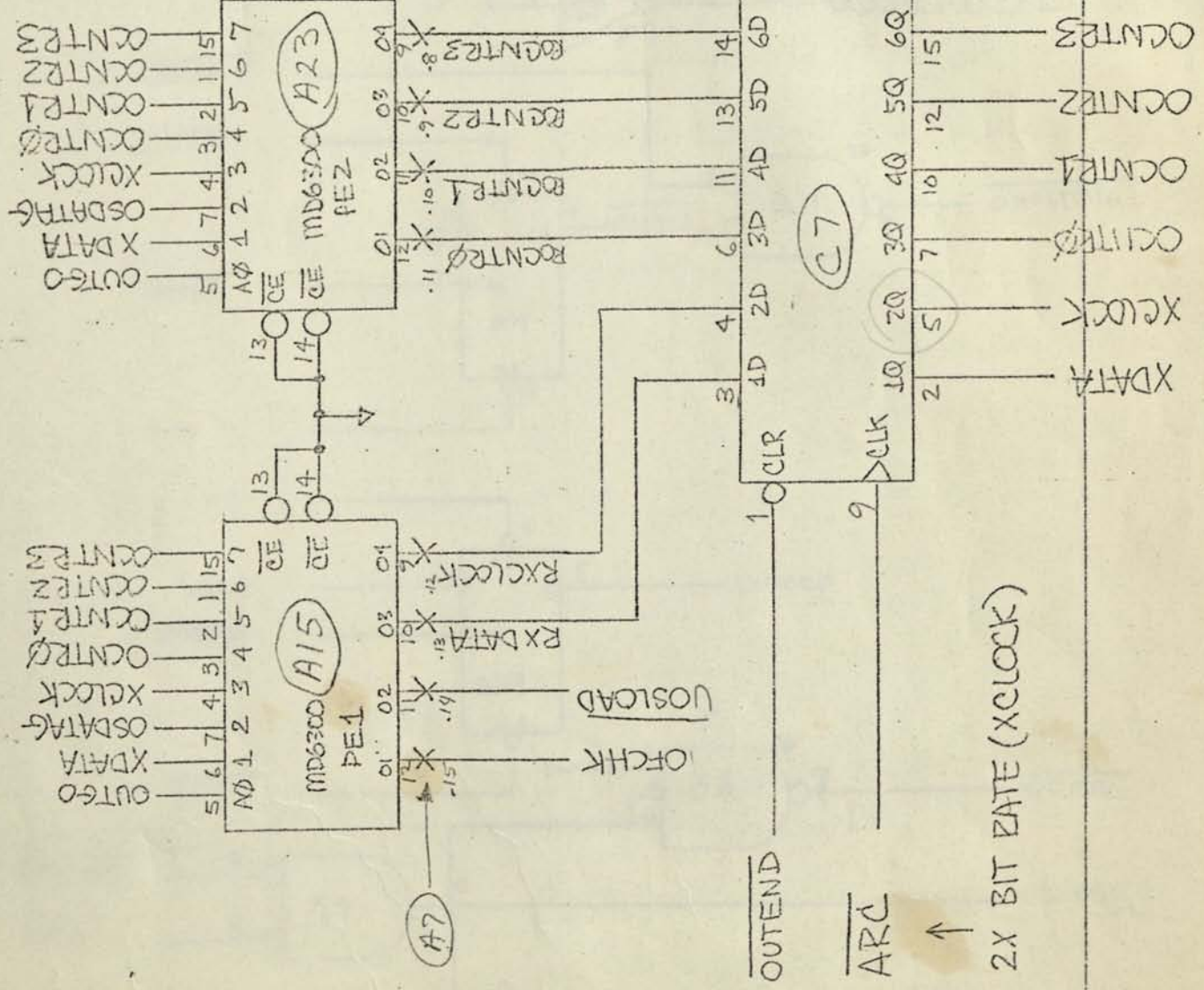
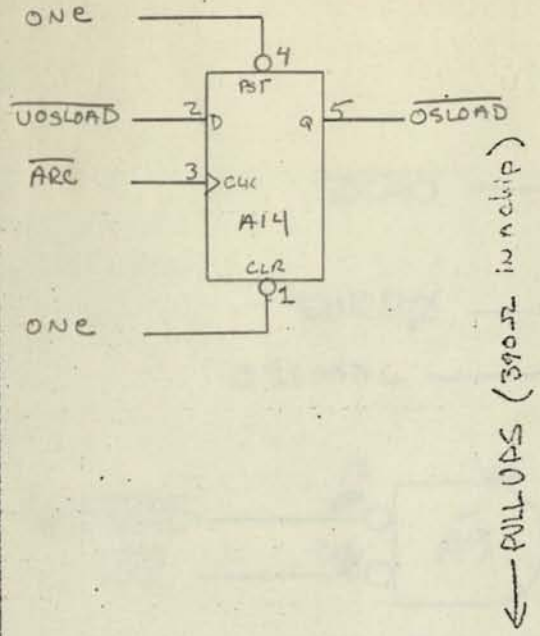
AMPUTATED?
RECONNECT?

MAYBE OK AS WAS WITH PROPER TERMINATION
7438

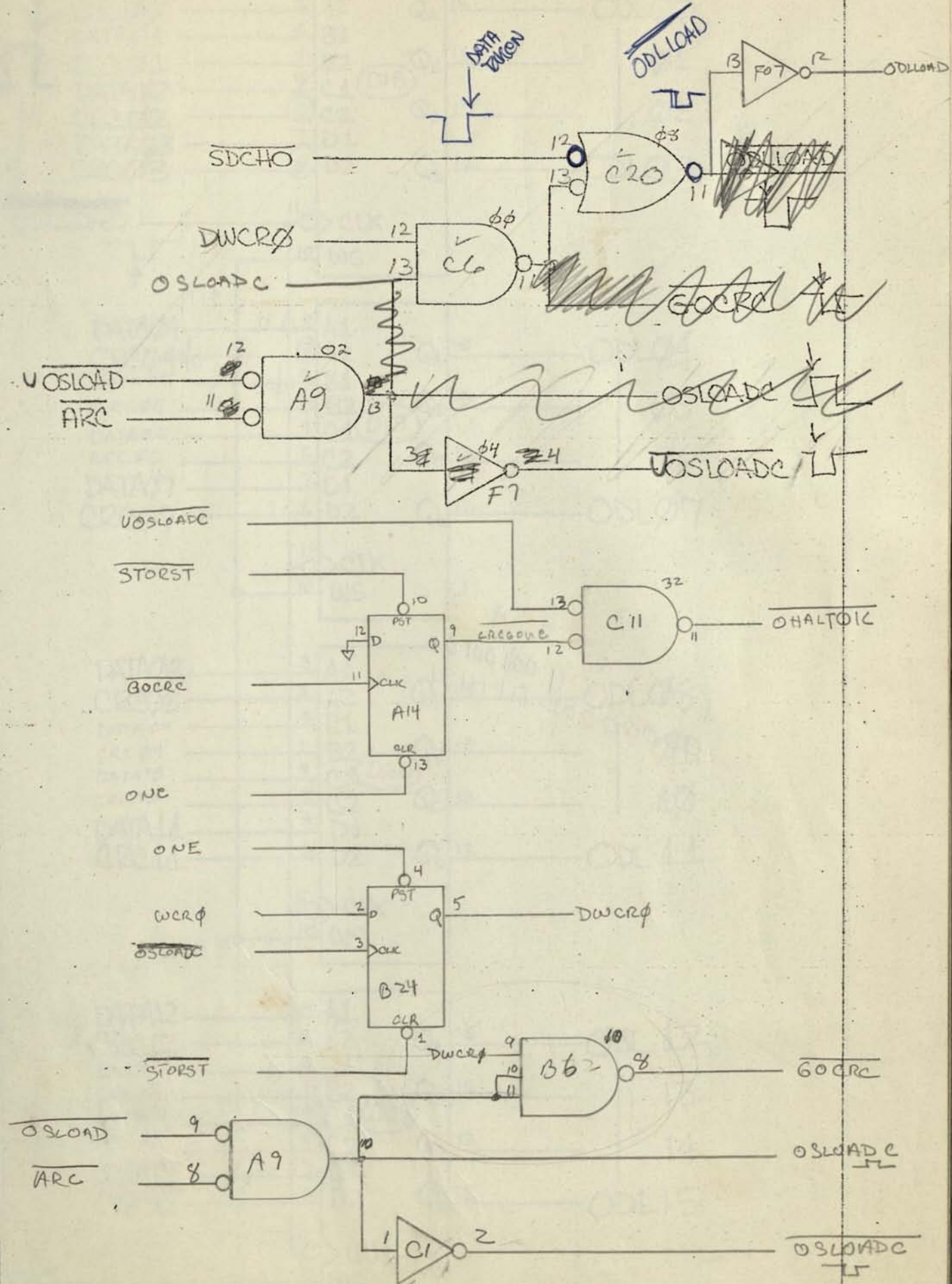
SYNCHRONIZATION POINT

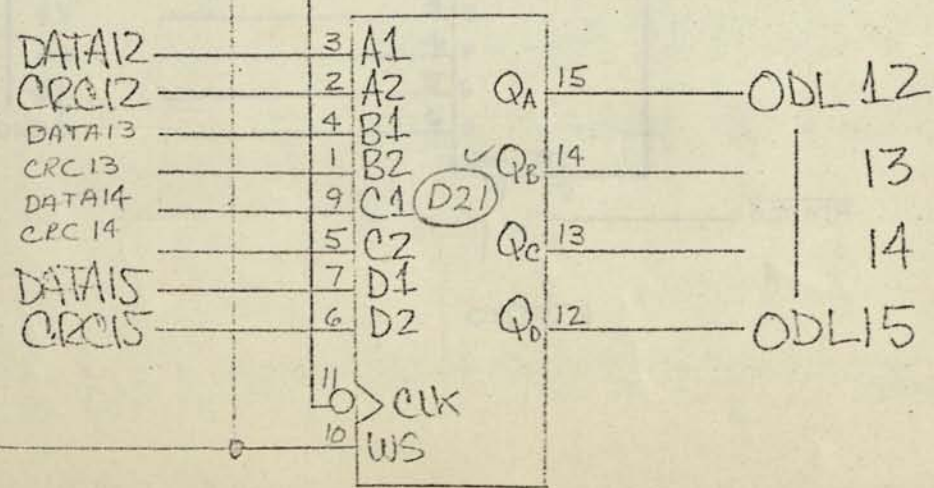
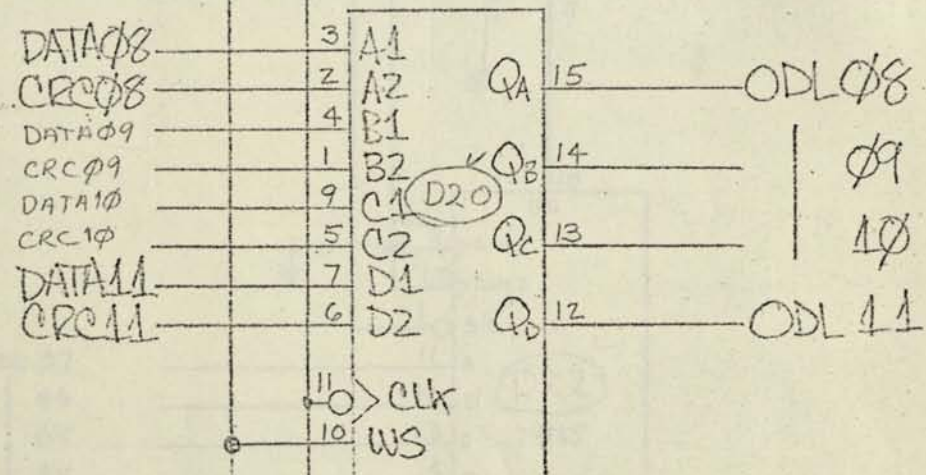
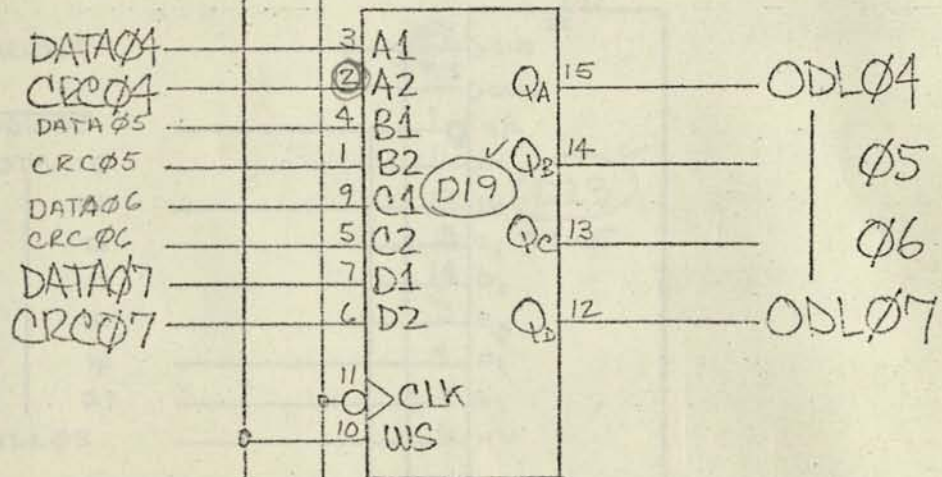
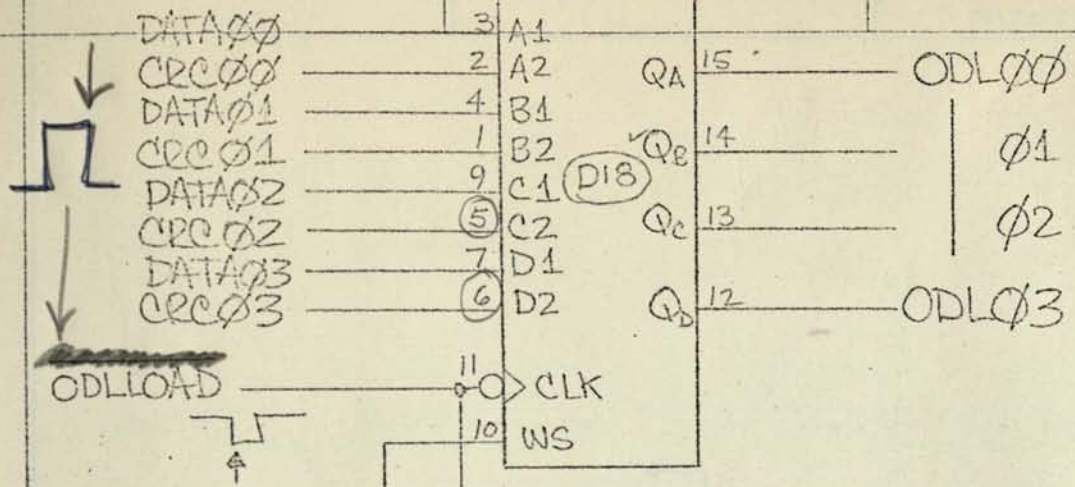




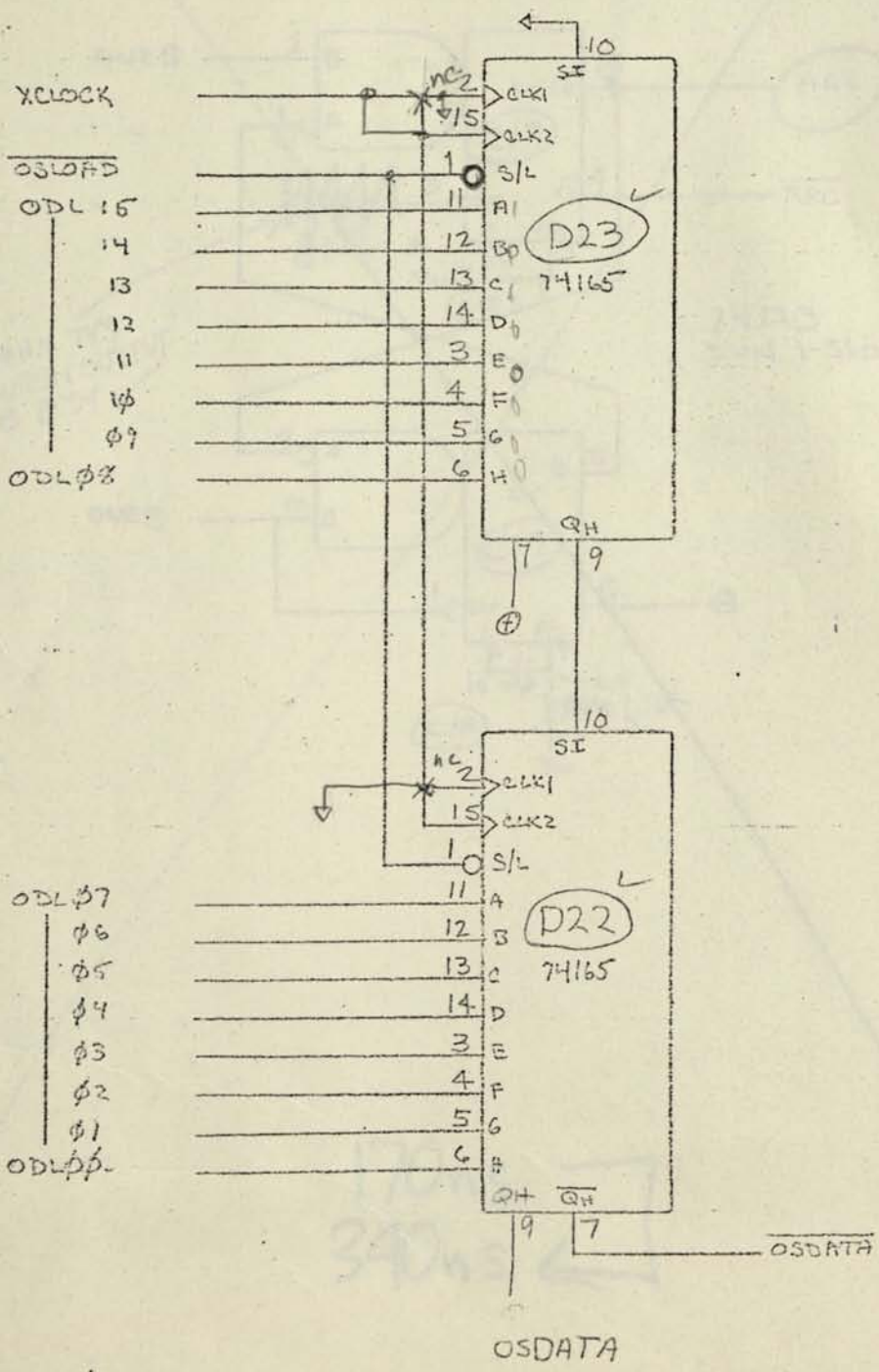


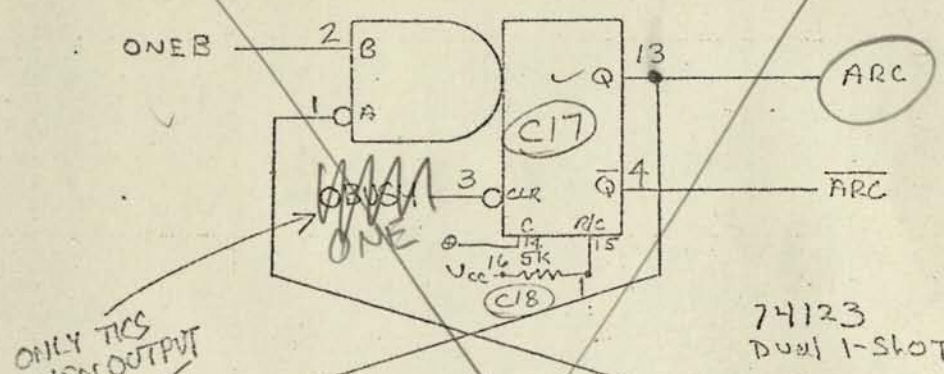
↑
2X BIT RATE (XLOCK)





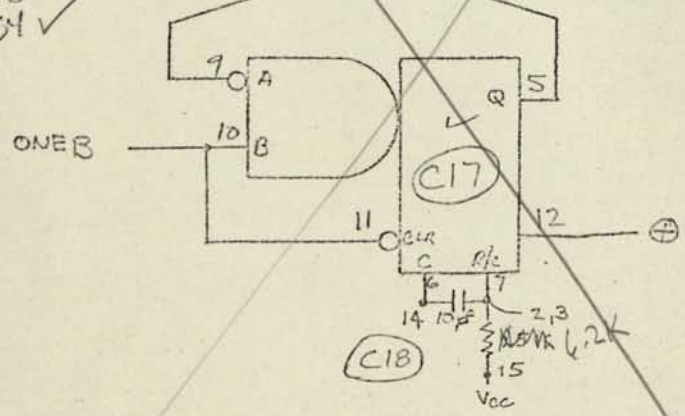
DUXCRO





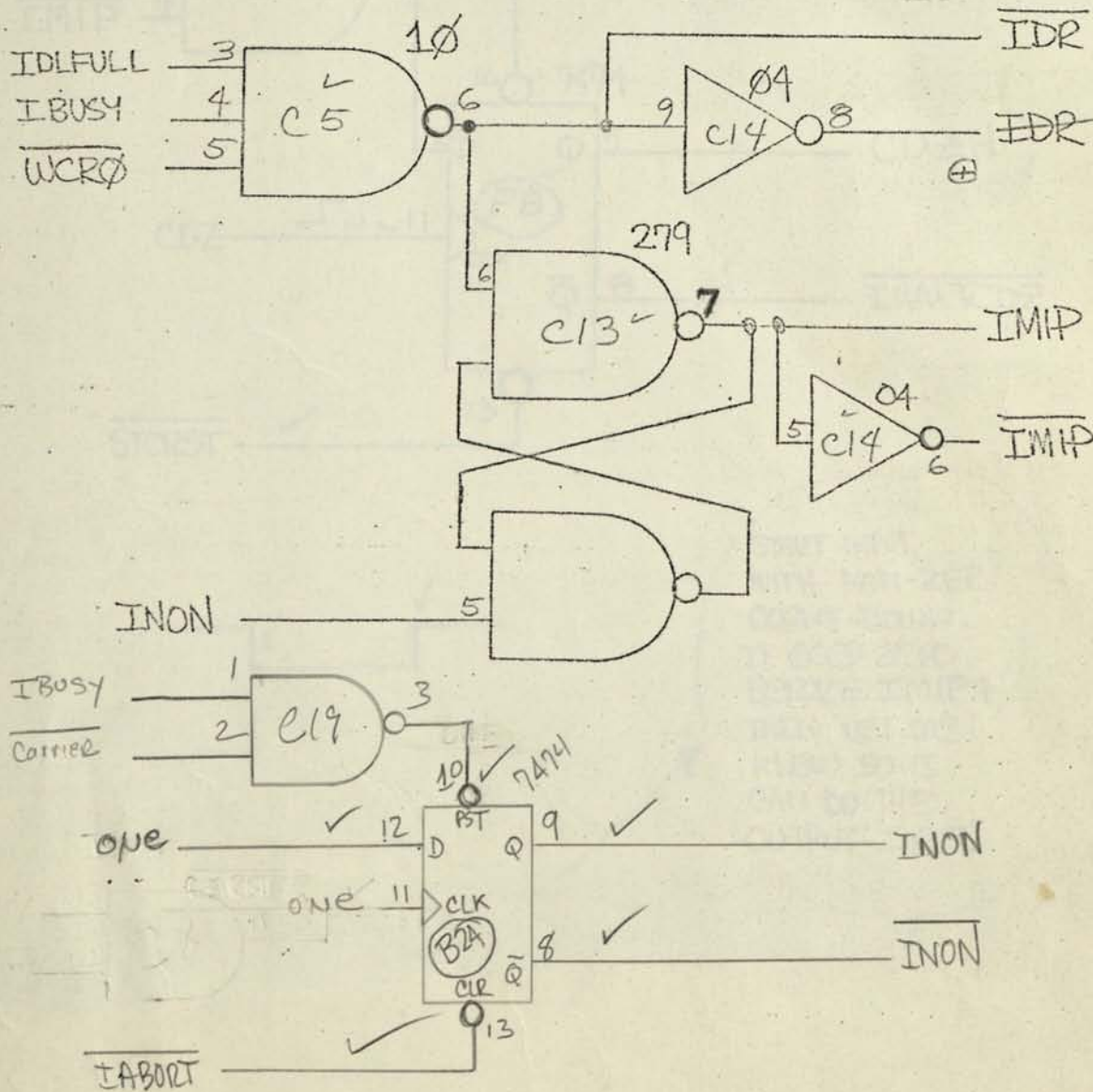
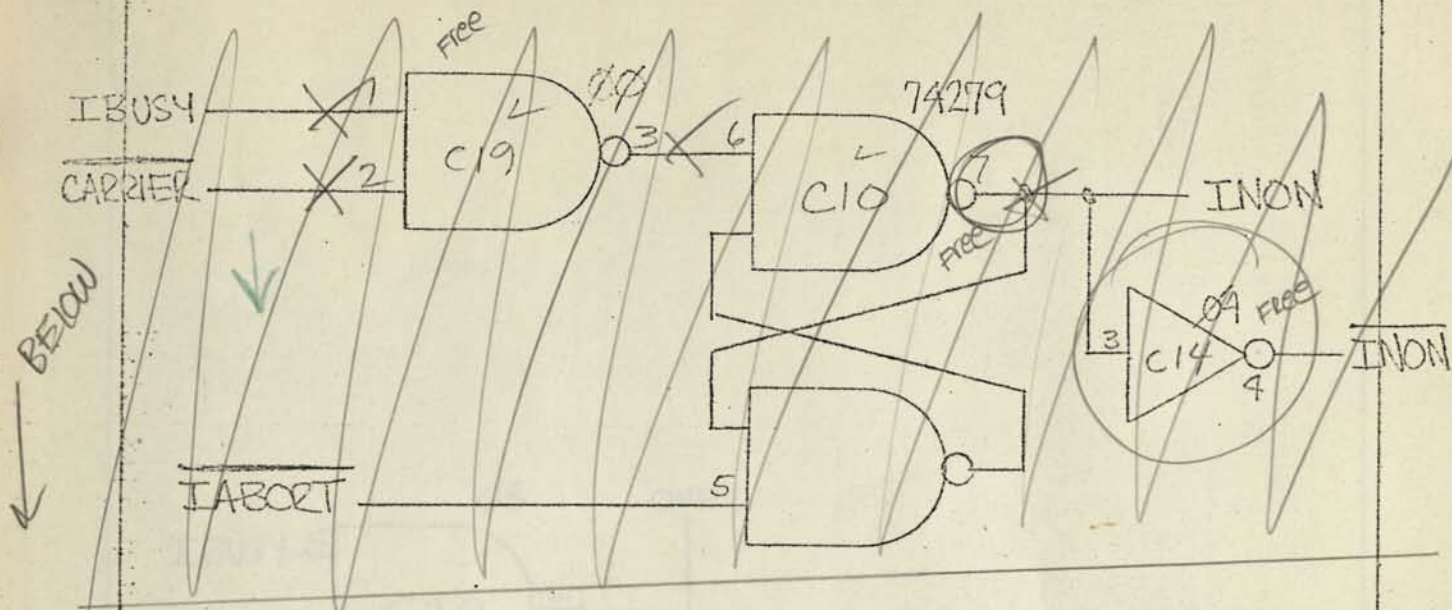
ONLY TICS
WHEN OUTPUT
IS BUSY ✓

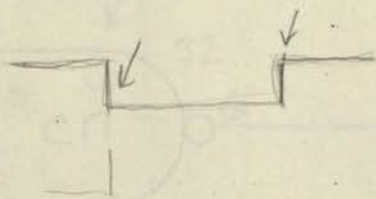
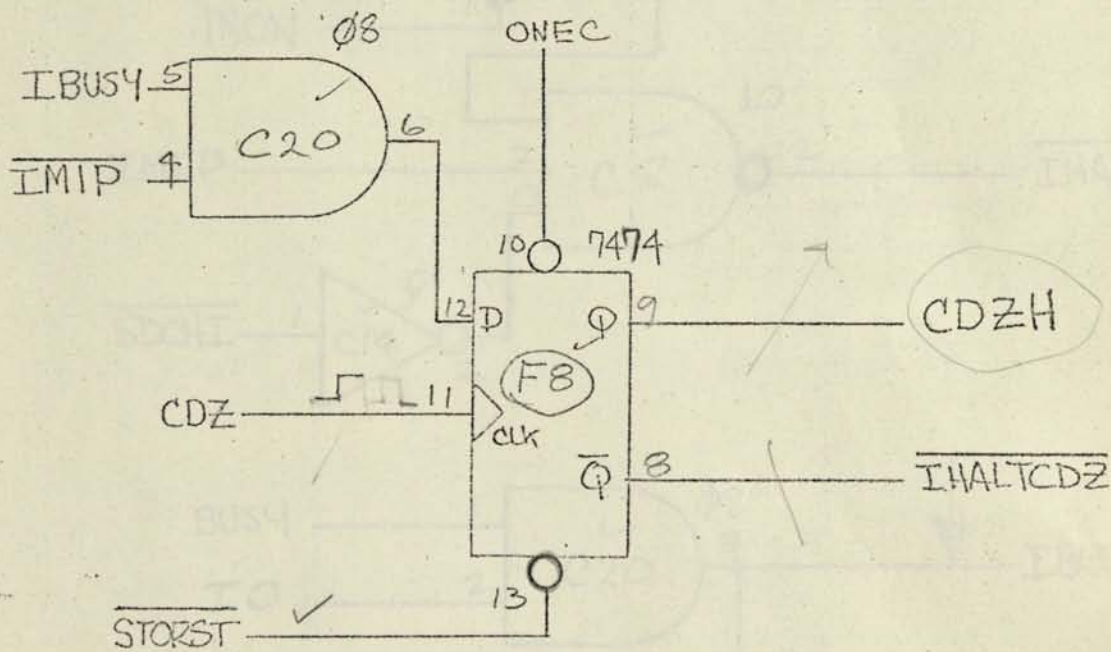
74123
Dual 1-SLOT



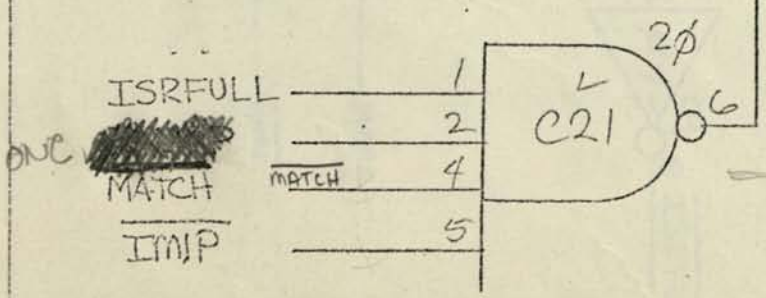
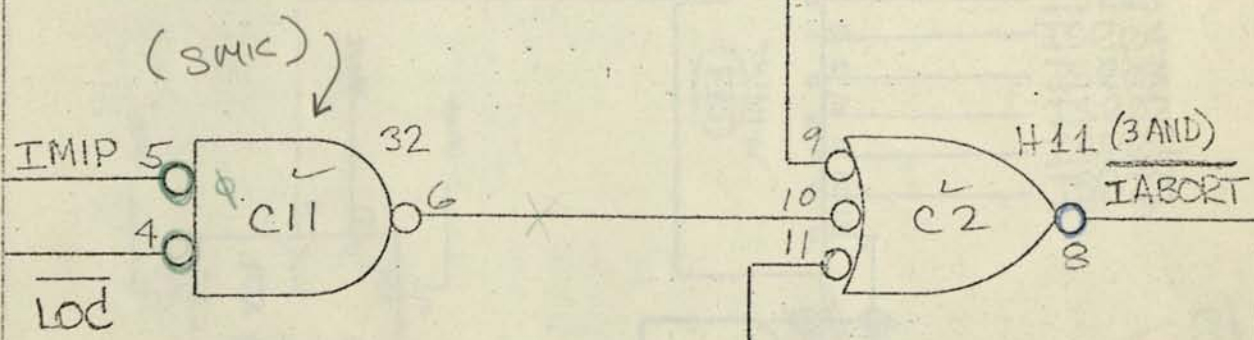
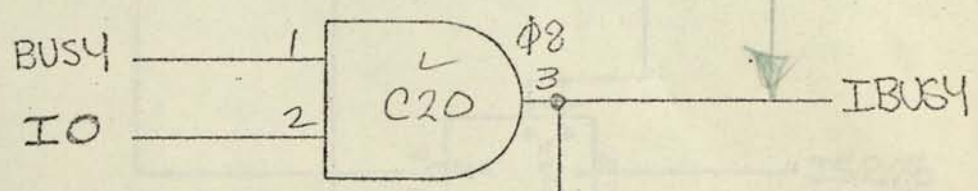
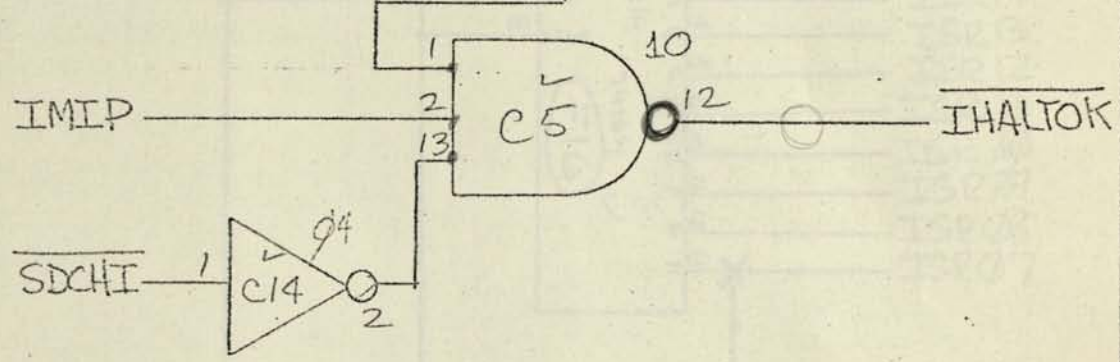
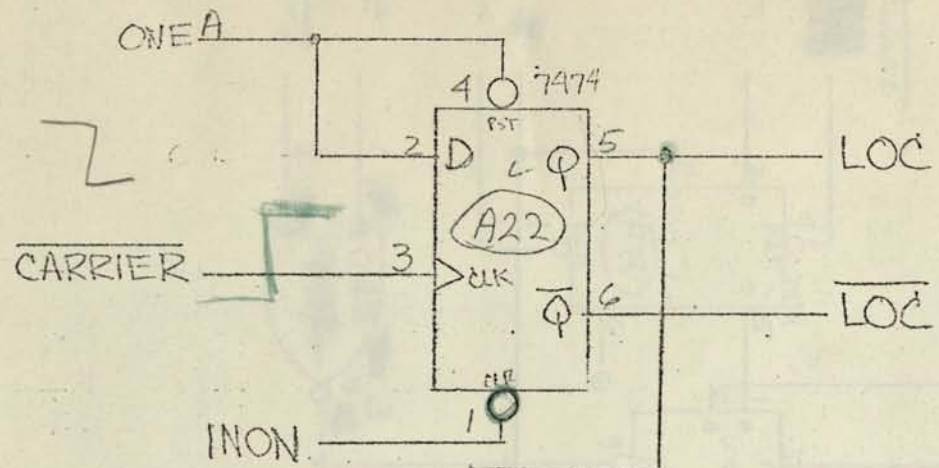
170ns
390ns

69 16009

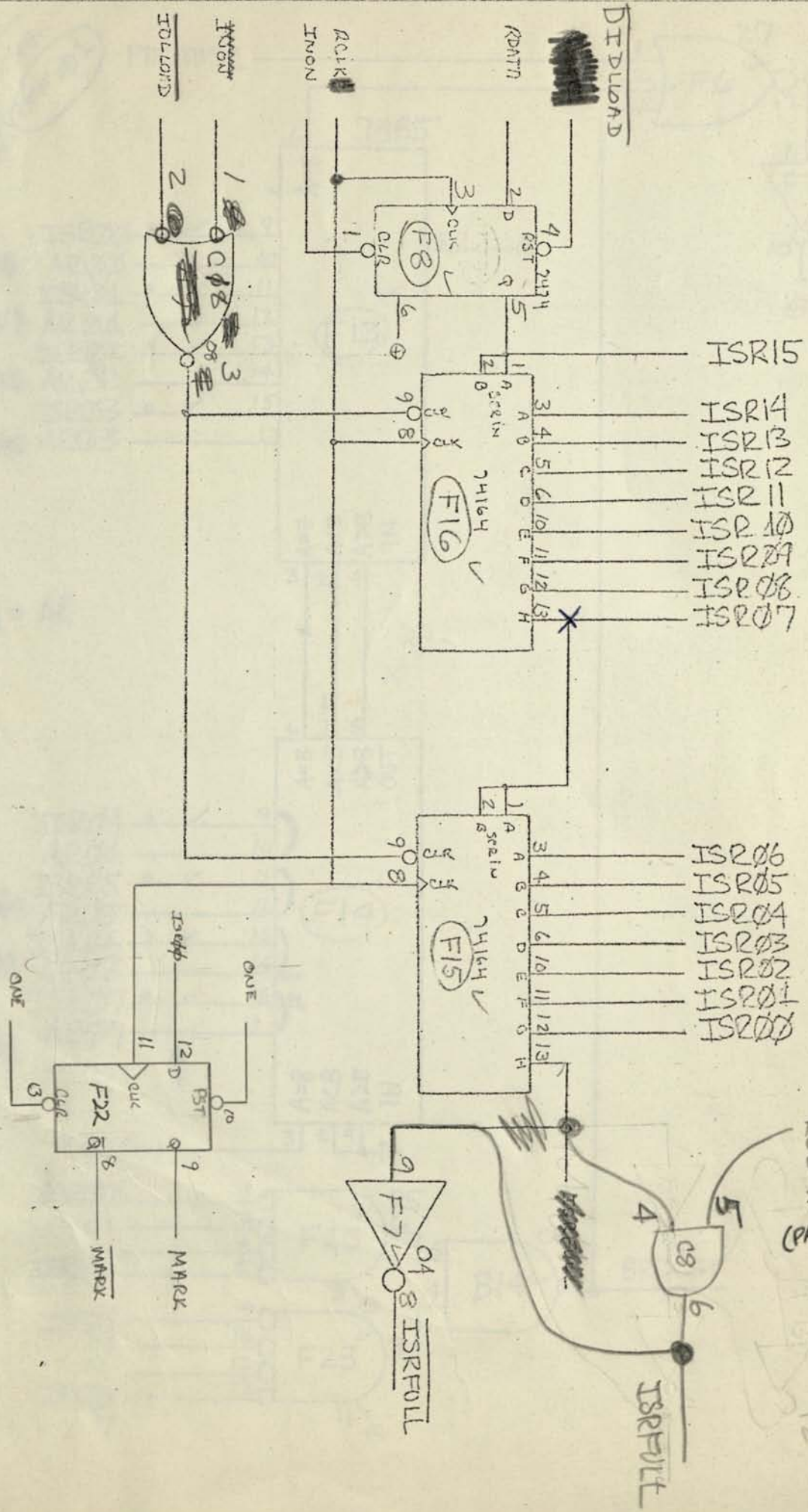




START INPUT WITH NON-ZER COUNT-DOWN. IF GOES ZERO BEFORE IMIP ↑, THEN LET ME KNOW SO I CAN DO THE OUTPUT I GOT.



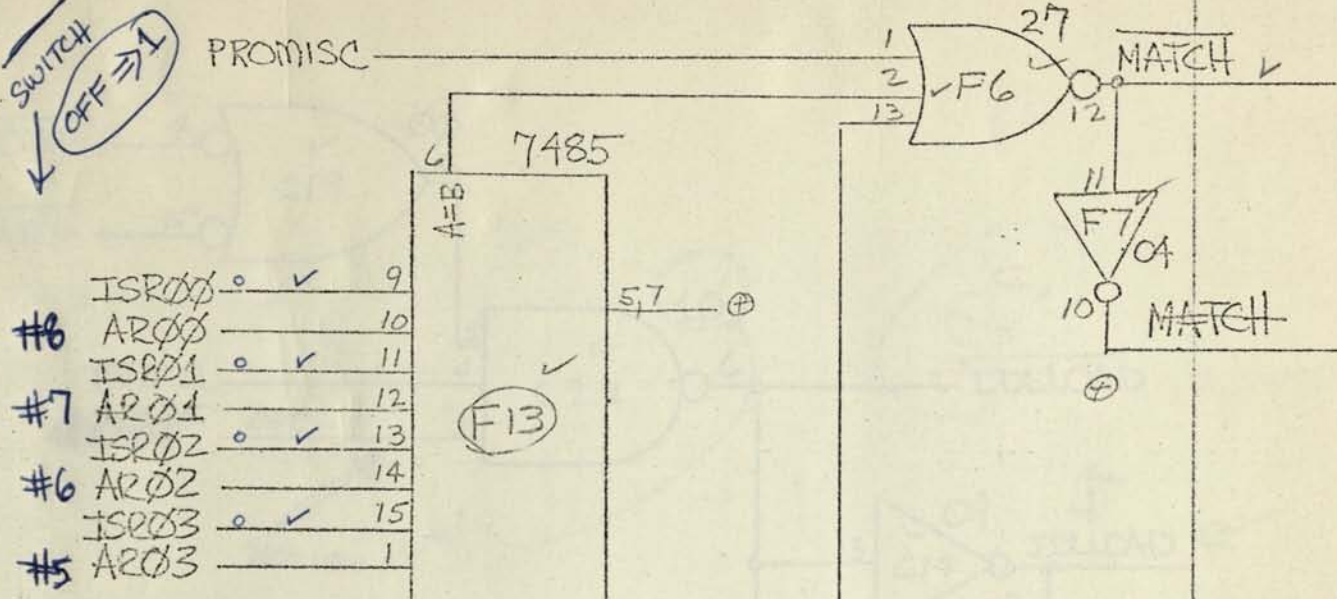
Fix 2



PULSE (PAGE 40)

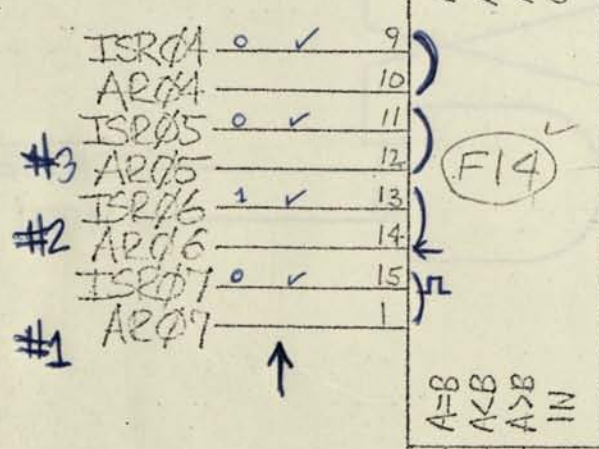
12

SWITCH
OFF → 1

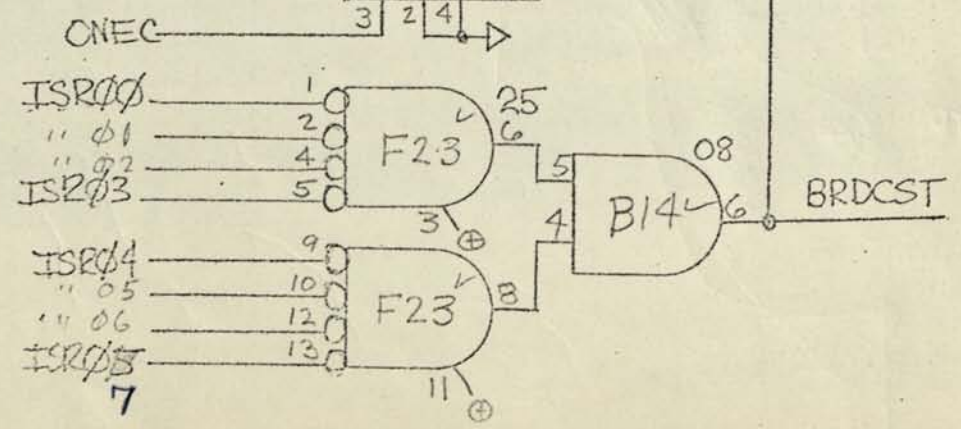


- #8 ISR00 ✓ 9
- AR00 10
- #7 ISR01 ✓ 11
- AR01 12
- #6 ISR02 ✓ 13
- AR02 14
- ISR03 ✓ 15
- AR03 1

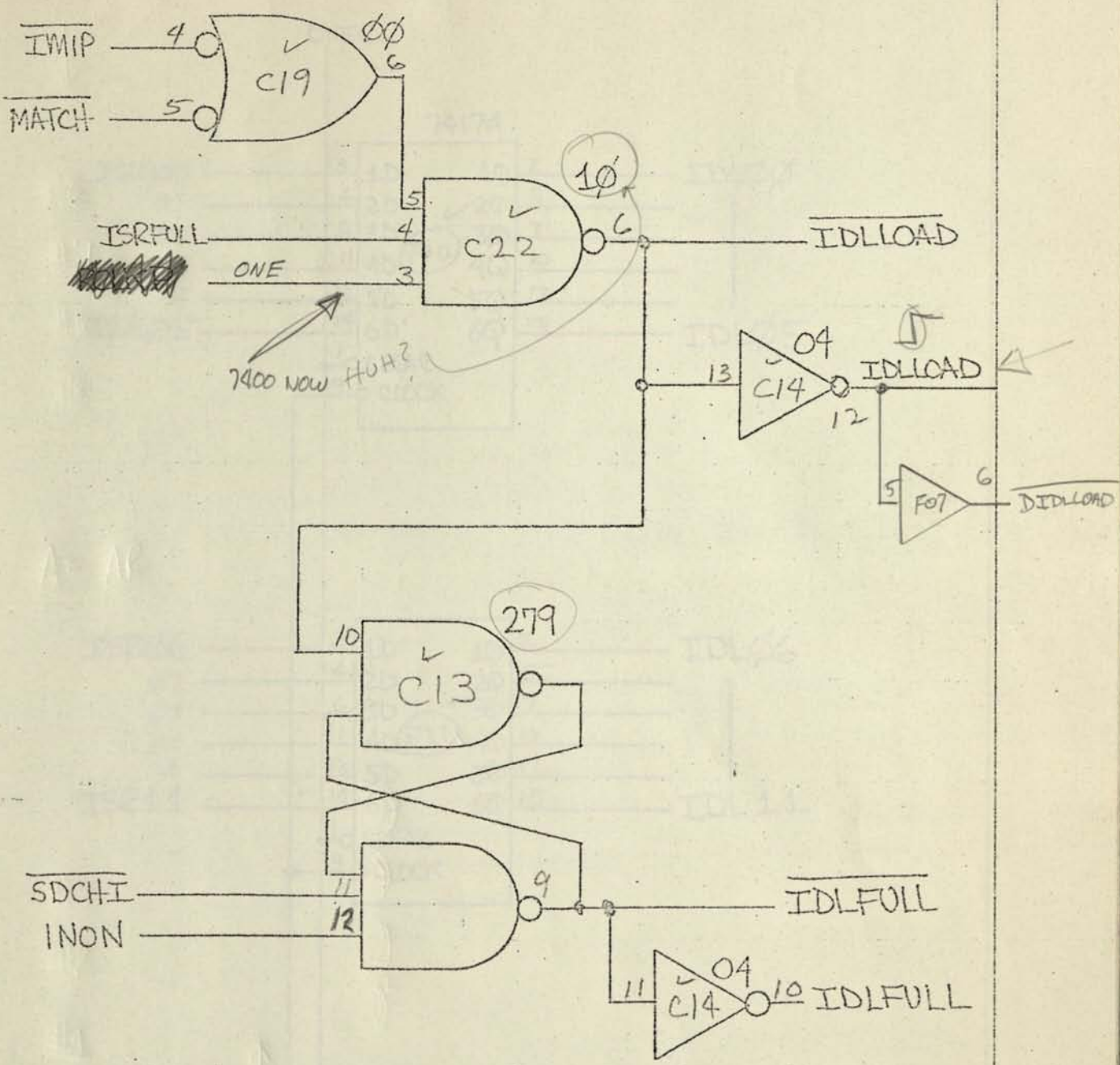
A = AR

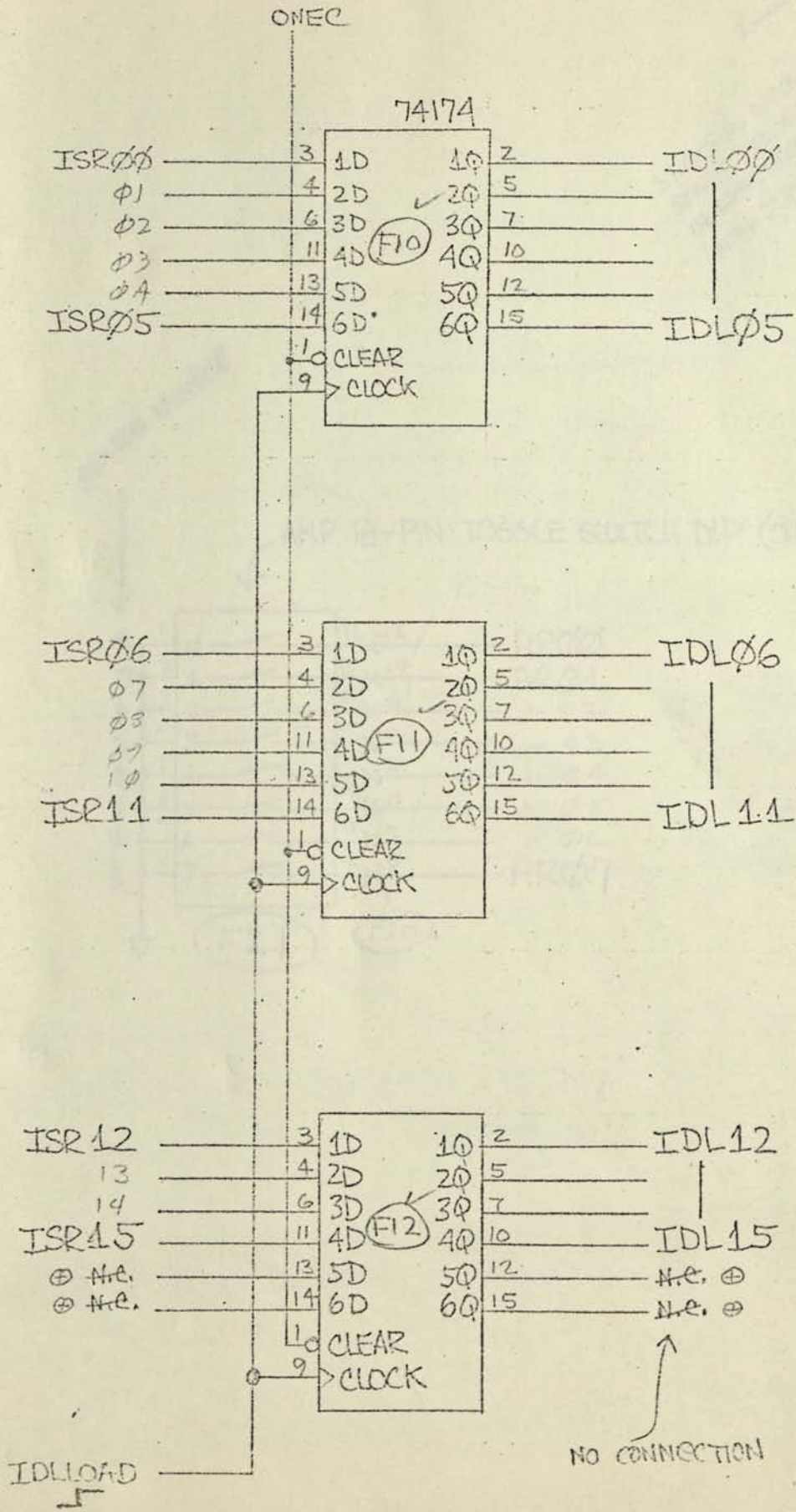


- ISR04 ✓ 9
- AR04 10
- #3 ISR05 ✓ 11
- AR05 12
- #2 ISR06 ✓ 13
- AR06 14
- ISR07 ✓ 15
- AR07 1



- ISR00 1
- " 01 2
- " 02 4
- ISR03 5
- ISR04 9
- " 05 10
- " 06 12
- ISR05 13



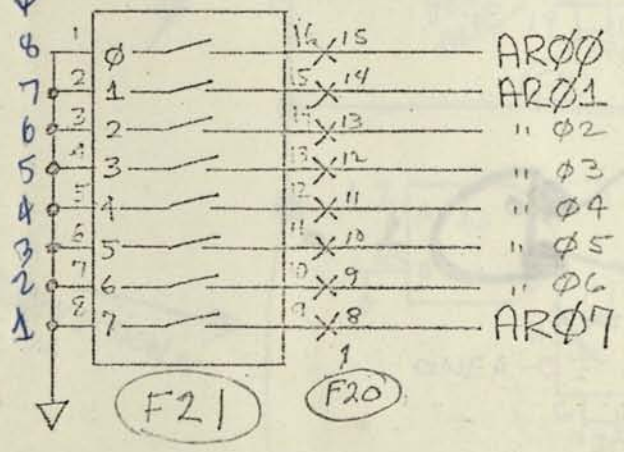


NOVA SERIAL NUMBER

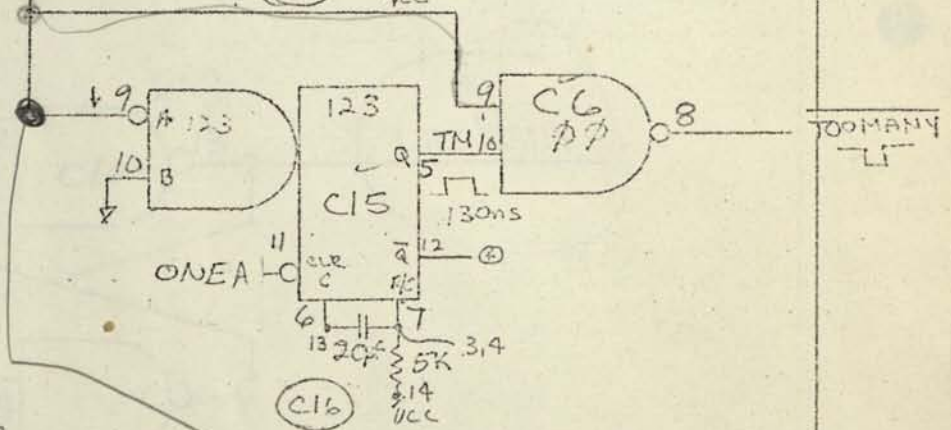
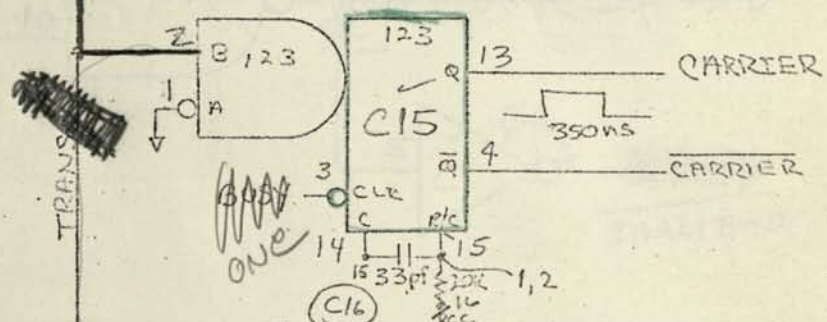
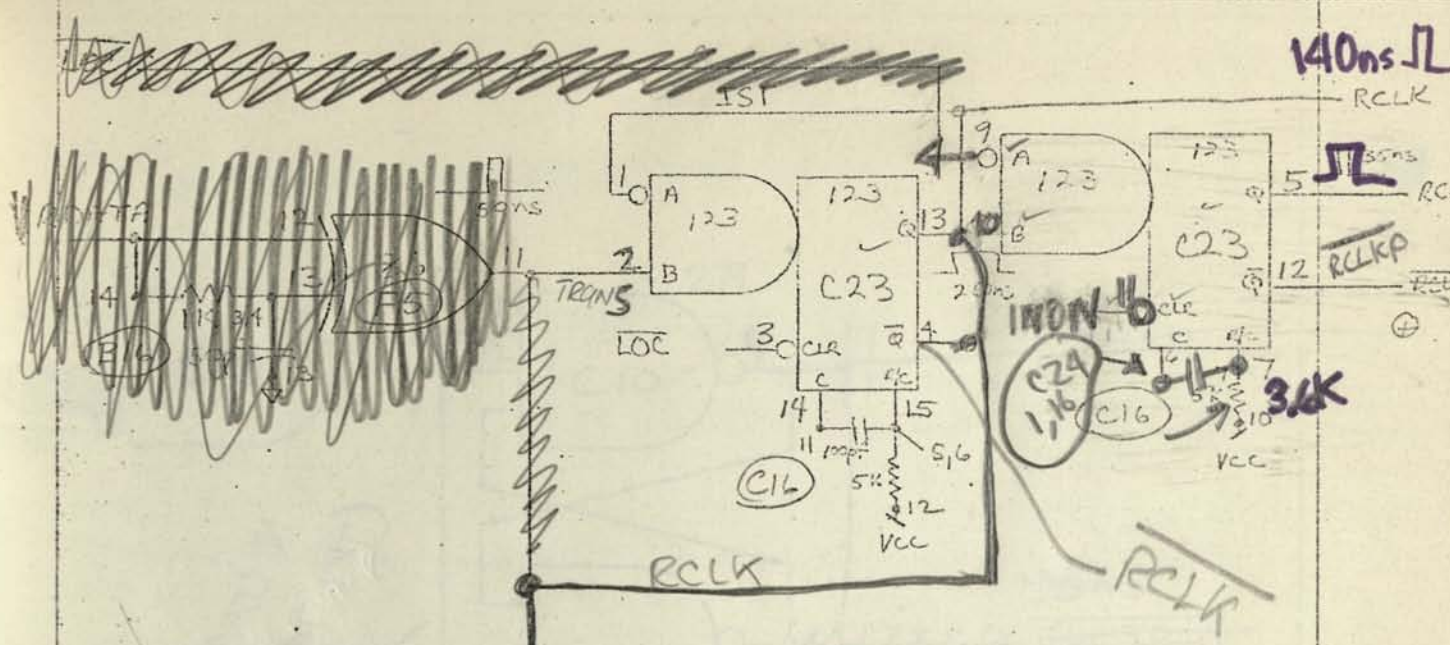
STICKS IN WRONG STATE SOMETIMES. IN PRACTICE, REPLACE WITH JUMPERS.

SWITCH NUMBER

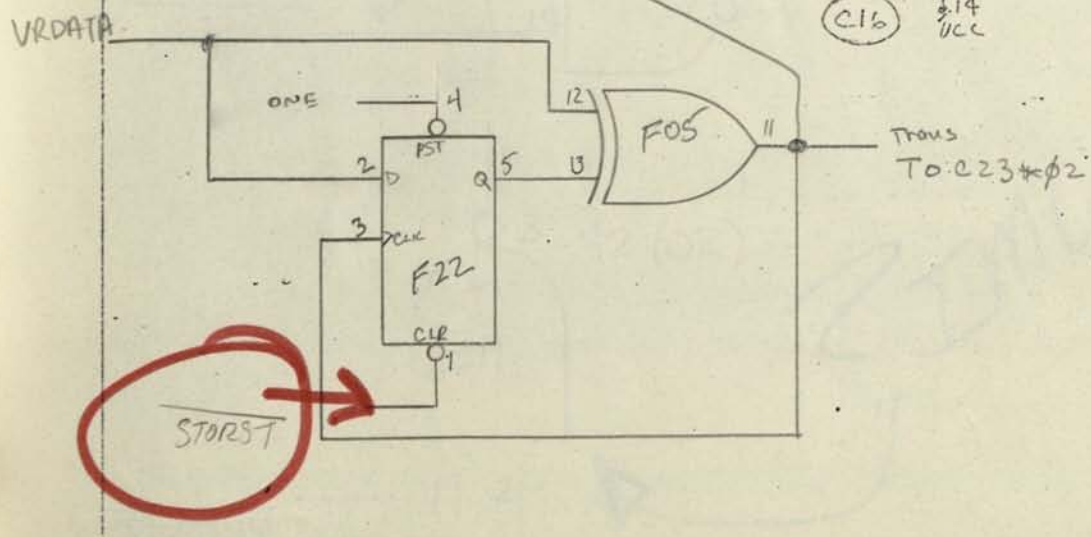
AMP 16-PIN TOGGLE SWITCH DIP (ONESLOT)

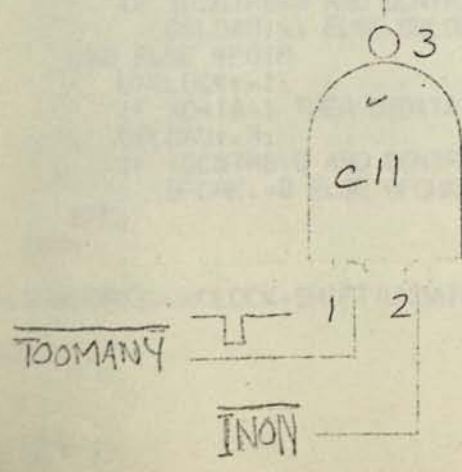
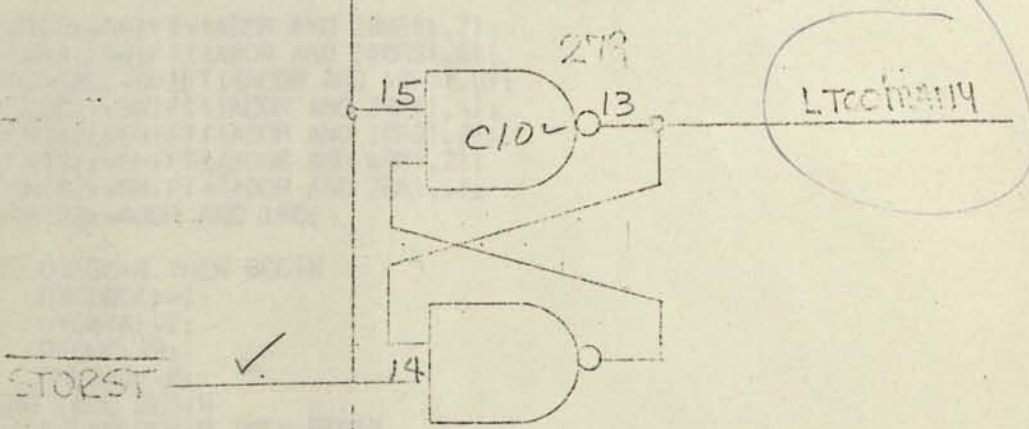
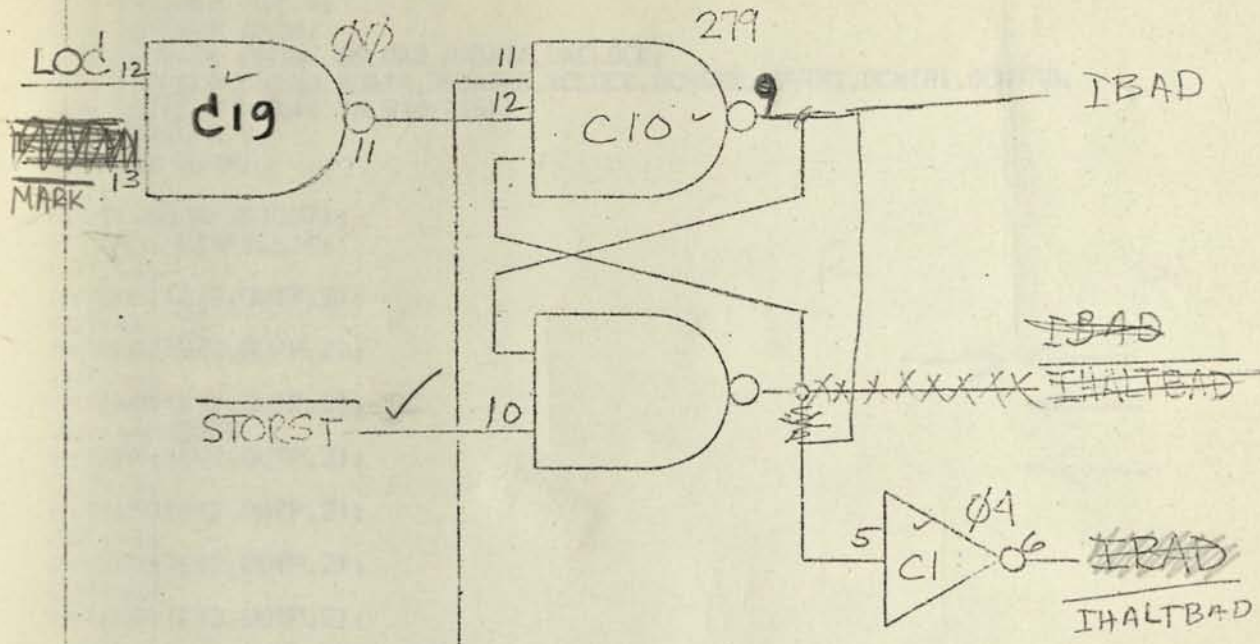


FIX? 40
140ns $\overline{\text{RCLK}}$

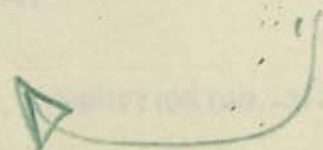


TRANSITIONS →





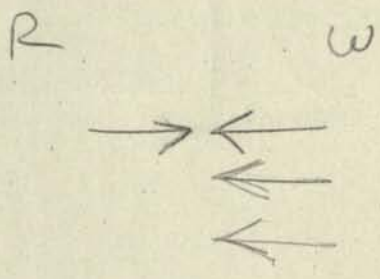
IMP



BEGIN
 COMMENT: ETHERNET OUTPUT PHASE ENCODER ROM PE1. MD6300
 8/25/73 DAVID BOGGS;

DIJN INTEGER OUT,V;
 DIJN INTEGER ADDR;
 DIJN INTEGER OFCHK,OSLOAD,UXDATA,UXCLOCK;
 DIJN INTEGER OUTGO,XDATA,OSDATAG,XCLOCK,OCNTR3,OCNTR2,OCNTR1,OCNTR0;
 DIJN INTEGER ARRAY VALS(0:255);
 DIJN INTEGER I;
 POINTER OUTP;

OUTP:=ADDRESS(OUT);
 OPEN(2,"BINFILE");
 OUT:=4;
 BYTEWRITE(2,OUTP,2);
 OUT:=1;
 BYTEWRITE(2,OUTP,2);
 OUT:=4;
 BYTEWRITE(2,OUTP,2);
 OUT:=40400R8;
 BYTEWRITE(2,OUTP,2);
 OUT:=2;
 BYTEWRITE(2,OUTP,2);
 OUT:=1;
 BYTEWRITE(2,OUTP,2);
 OUT:=0;
 BYTEWRITE(2,OUTP,2);



FOR I:=0 STEP 1 UNTIL 255 DO VALS(I):=0;

FOR ADDR:=0 STEP 1 UNTIL 255 DO BEGIN

OUTGO:=SHIFT((ADDR AND 200R8),7);
 XDATA:=SHIFT((ADDR AND 100R8),6);
 OSDATAG:=SHIFT((ADDR AND 40R8),5);
 XCLOCK:=SHIFT((ADDR AND 20R8),4);
 OCNTR0:=SHIFT((ADDR AND 10R8),3);
 OCNTR1:=SHIFT((ADDR AND 4R8),2);
 OCNTR2:=SHIFT((ADDR AND 2R8),1);
 OCNTR3:=ADDR AND 1R8;

IF OUTGO=0 THEN BEGIN

UXCLOCK:=1;
 UXDATA:=1;
 OFCHK:=0;
 OSLOAD:=0;

END ELSE BEGIN

IF XCLOCK=0 THEN BEGIN

UXCLOCK:=0;
 OFCHK:=1;
 IF OSDATAG=0 THEN UXDATA:=0 ELSE UXDATA:=1;
 IF (OCNTR0=0 AND OCNTR1=0 AND OCNTR2=0 AND OCNTR3=0) THEN
 OSLOAD:=1 ELSE OSLOAD:=0;

END ELSE BEGIN

UXCLOCK:=1;
 IF XDATA=1 THEN UXDATA:=1 ELSE UXDATA:=0;
 OSLOAD:=0;
 IF (OCNTR0=0 AND OCNTR1=0 AND OCNTR2=0 AND OCNTR3=1) THEN
 OFCHK:=0 ELSE OFCHK:=1;

END;

END;

Setup

Data

VALS[ADDR]:=UXCLOCK+SHIFT(UXDATA,-1)+SHIFT(OSLOAD,-2)+SHIFT(OFCHK,-3);

END;


```
FOR I:=0 STEP 1 UNTIL 255 DO BEGIN
  OUT:=1;
  BYTEWRITE (2,OUTP,2);
  OUT:=0;
  BYTEWRITE (2,OUTP,2);
  V:=VALS[I];
  OUT:=SHIFT(V,-12);
  BYTEWRITE (2,OUTP,2);
  END;
OUT:=0;
BYTEWRITE (2,OUTP,2);
CLOSE (2);
END
```

AD 0	0011
AD 1	0011
AD 2	0011
AD 3	0011
AD 4	0011
AD 5	0011
AD 6	0011
AD 7	0011
AD 10	0011
AD 11	0011
AD 12	0011
AD 13	0011
AD 14	0011
AD 15	0011
AD 16	0011
AD 17	0011
AD 20	0011
AD 21	0011
AD 22	0011
AD 23	0011
AD 24	0011
AD 25	0011
AD 26	0011
AD 27	0011
AD 30	0011
AD 31	0011
AD 32	0011
AD 33	0011
AD 34	0011
AD 35	0011
AD 36	0011
AD 37	0011
AD 40	0011
AD 41	0011
AD 42	0011
AD 43	0011
AD 44	0011
AD 45	0011
AD 46	0011
AD 47	0011
AD 50	0011
AD 51	0011
AD 52	0011
AD 53	0011
AD 54	0011
AD 55	0011
AD 56	0011
AD 57	0011
AD 60	0011
AD 61	0011
AD 62	0011
AD 63	0011
AD 64	0011
AD 65	0011
AD 66	0011
AD 67	0011
AD 70	0011
AD 71	0011
AD 72	0011
AD 73	0011
AD 74	0011
AD 75	0011
AD 76	0011
AD 77	0011
AD 100	0011
AD 101	0011

AD 102	0011
AD 103	0011
AD 104	0011
AD 105	0011
AD 106	0011
AD 107	0011
AD 110	0011
AD 111	0011
AD 112	0011
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AD 115	0011
AD 116	0011
AD 117	0011
AD 120	0011
AD 121	0011
AD 122	0011
AD 123	0011
AD 124	0011
AD 125	0011
AD 126	0011
AD 127	0011
AD 130	0011
AD 131	0011
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AD 141	0011
AD 142	0011
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AD 165	0011
AD 166	0011
AD 167	0011
AD 170	0011
AD 171	0011
AD 172	0011
AD 173	0011
AD 174	0011
AD 175	0011
AD 176	0011
AD 177	0011
AD 200	1100
AD 201	1000
AD 202	1000
AD 203	1000

AD 204	1010
AD 205	1001
AD 206	1000
AD 207	0111
AD 210	1110
AD 211	1101
AD 212	1100
AD 213	1011
AD 214	1010
AD 215	1001
AD 216	1000
AD 217	0111
AD 220	1111
AD 221	1110
AD 222	1101
AD 223	1100
AD 224	1011
AD 225	1010
AD 226	1001
AD 227	1000
AD 230	0111
AD 231	0110
AD 232	0101
AD 233	0100
AD 234	0011
AD 235	0010
AD 236	0001
AD 237	0000
AD 240	1110
AD 241	1101
AD 242	1100
AD 243	1011
AD 244	1010
AD 245	1001
AD 246	1000
AD 247	0111
AD 250	1110
AD 251	1101
AD 252	1100
AD 253	1011
AD 254	1010
AD 255	1001
AD 256	1000
AD 257	0111
AD 260	1111
AD 261	1110
AD 262	1101
AD 263	1100
AD 264	1011
AD 265	1010
AD 266	1001
AD 267	1000
AD 270	0111
AD 271	0110
AD 272	0101
AD 273	0100
AD 274	0011
AD 275	0010
AD 276	0001
AD 277	0000
AD 300	1110
AD 301	1101
AD 302	1100
AD 303	1011
AD 304	1010
AD 305	1001

AD 306	1000
AD 307	0111
AD 310	1110
AD 311	1101
AD 312	1100
AD 313	1011
AD 314	1010
AD 315	1001
AD 316	1000
AD 317	0111
AD 320	1111
AD 321	1110
AD 322	1101
AD 323	1100
AD 324	1011
AD 325	1010
AD 326	1001
AD 327	1000
AD 330	0111
AD 331	0110
AD 332	0101
AD 333	0100
AD 334	0011
AD 335	0010
AD 336	0001
AD 337	0000
AD 340	1110
AD 341	1101
AD 342	1100
AD 343	1011
AD 344	1010
AD 345	1001
AD 346	1000
AD 347	0111
AD 350	1110
AD 351	1101
AD 352	1100
AD 353	1011
AD 354	1010
AD 355	1001
AD 356	1000
AD 357	0111
AD 360	1111
AD 361	1110
AD 362	1101
AD 363	1100
AD 364	1011
AD 365	1010
AD 366	1001
AD 367	1000
AD 370	0111
AD 371	0110
AD 372	0101
AD 373	0100
AD 374	0011
AD 375	0010
AD 376	0001
AD 377	0000