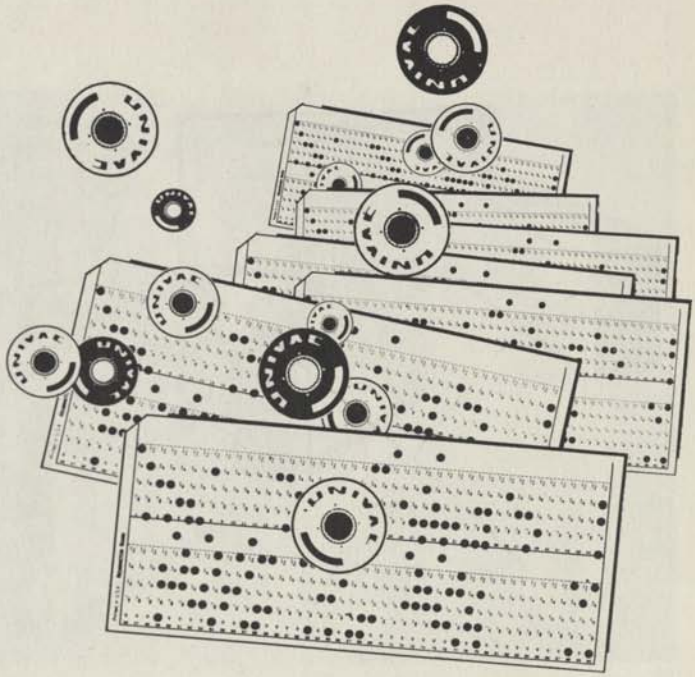
UNIVAC®
Solid-State 90

PROGRAMMING

UNIVAC Solid-State 90
MAGNETIC TAPE System



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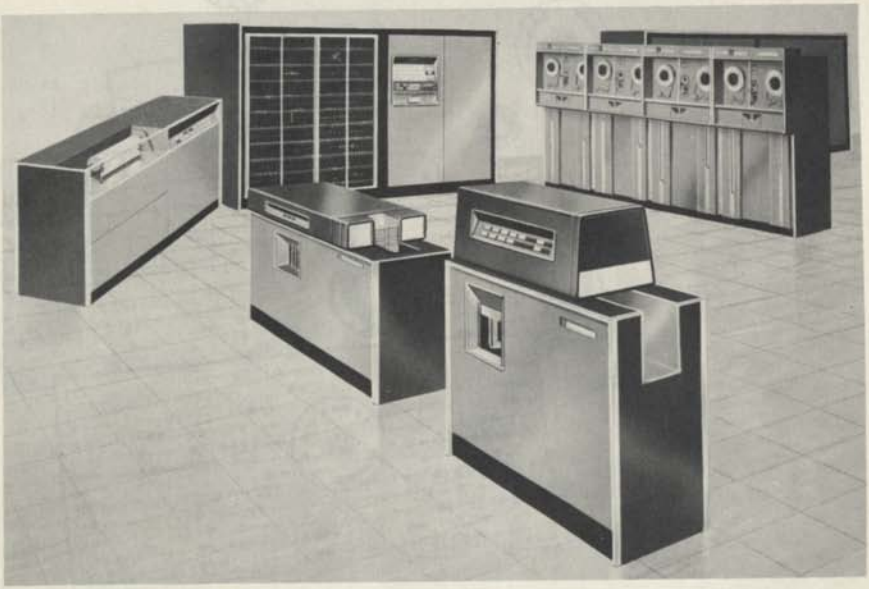
Preface



In its new UNIVAC Solid-State 90 Magnetic Tape System, Remington Rand has found the answer to all practical demands formerly met only by elaborate data automation devices. Powerful yet compact, the new system offers a variety of input-output media — metallic or plastic tape, punched cards, and printed hard copies. The UNIVAC Solid-State 90 Magnetic Tape System, moreover, combines the advantages of large-capacity drum storage with fast, accurate processing capabilities. The use of magnetic tapes as well as punched cards facilitates the permanent storage of lengthy records, and the reliability of all operations is assured by the magnetic-amplifier, solid-state circuitry. Finally, the cost of this advanced new system with large-scale capabilities places the UNIVAC Solid-State 90 Magnetic Tape System well within the medium range.

Contents

1. General Description and Features

The UNIVAC Solid-State 90 Magnetic Tape System is a general-purpose, digital-computing system capable of performing a wide range of data processing tasks requiring large volumes of input-output data. The system is composed of the Tape Synchronizer, with up to ten magnetic tape handling units; the High-Speed Reader; the Central Processor; the Read-Punch Unit; and the High-Speed Printer. Joined by electronic circuitry, the compact, easily operated units are sure, fast, and reliable.

INPUT

The main input devices are the Tape Synchronizer and the High-Speed Reader. The Tape Synchronizer, with as many as ten tape-handling devices, provides the system with a constant flow of data from tape. Data is read into the system from cards, at the rate of 450 cards per minute, by the High-Speed Reader.

PROCESSING

As well as performing the storage, logical, and arithmetic operations, the Central Processor coordinates the activities of the system, making full and simultaneous use of its input, output and processing abilities. Output emerges from this new UNIVAC System in either punched, printed, or taped form.

OUTPUT

In addition to serving as an input device, the Tape Synchronizer acts as an output device, since it permits the recording of data on magnetic tape at a speed of 100 inches per second at a recording density of 125 or 250 characters per inch. The Read-Punch Unit accomplishes punching at the rate of 150 cards per minute. In addition to punching output, the unit can be utilized to read data into the system. In fact, reading occurs as an integral part of every punching cycle, even when the unit is operating at maximum speed. Printing is performed on the High-Speed Printer at the rate of 600 lines per minute and may be executed in an almost limitless variety of formats.

FEATURES

- Metallic or Mylar* Tape input-output.
- 90-column punched-card input-output.
- Fast arithmetic and logic circuits. Transfer rate is 707,000 characters per second.
- 5,000-word magnetic drum storage. Each word consists of ten digits plus sign for a total of 50,000 digits of information storage.

** Mylar is a registered trademark of E. I. du Pont de Nemours & Co., Inc.*

- The UNIVAC Solid-State 90 Magnetic Tape System is completely internally programmed.
- The input and output units are buffered to ensure simultaneous read, write, print, punch, and compute operations.
- All internal word transfers are parity-checked.
- 1½ address logic. Each instruction consists of ten digits: the first two digits represent the instruction code, the next four digits represent the operand, and the last four digits represent the address of the next instruction.
- The system's 5,000-word storage capacity enables the user to combine many different programs (and consequently applications) into one run. In addition, it is possible to summarize and store intermediate results for further processing within the computer. This, in turn, eliminates intermediate summarization runs, collating, and sorting, which normally had to be done off-line.
- Microsecond calculating abilities permit the user to build additional operations, such as distributions, table look-ups, and so on, into a program without decreasing its overall efficiency.
- Because the system is basically a "bit machine," it can be programmed to perform many types of special manipulations. This ability permits the programmer to utilize exceedingly sophisticated programming. Bit manipulation allows the system to use a variety of input-output codes.
- The system's ability to perform programmed audits on all input-output information, and thus guarantee the accuracy of this information, eliminates costly off-line control listing runs.
- Simple solid-state circuits, standardized for production and ease of maintenance — the most reliable circuitry in existence.

The UNIVAC Solid-State 90 Magnetic Tape System combines the advantages of large-capacity storage, and microsecond access and processing with input-output units working simultaneously on-line and in balance. The user is able to reduce his costs quickly, because:

1. The UNIVAC Solid-State 90 Magnetic Tape System is less expensive to build and to maintain — and these savings are passed on to the user.
2. The UNIVAC Solid-State 90 Magnetic Tape System allows the user to update physical records while simultaneously creating management reports. It ensures economies of operation by eliminating costly intermediate processing runs — often a complete application can be accomplished in one run.
3. The UNIVAC Solid-State 90 Magnetic Tape System is easily programmed. An extensive repertoire of instructions provides wide programming flexibility.

CONCEPT OF DESIGN

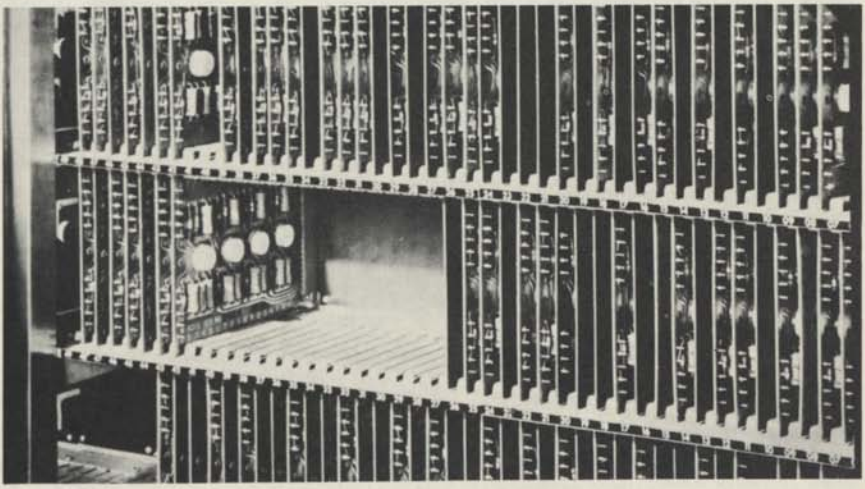
In 1948, Bell Laboratories, while conducting a series of experiments on crystal ionization, developed the transistor — a device which they found would reduce the costs of producing and maintaining their carrier equipment. The advantages of this device were multifold. The transistor was small, inexpensive, required very little power, generated little heat, and

was far more reliable than the vacuum tube. Instead of using an electron beam to transmit a pulse of information, as in conventional tubes, this device employed a *solid* grid which would transmit oscillations when pulsed.

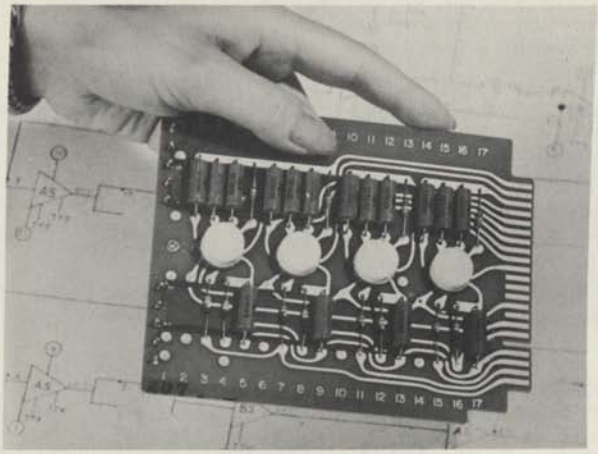
Remington Rand engineers realized early the potential of solid-state components. Why not, they reasoned, produce a computer which would combine the advantages of their systems with those of solid-state circuits? Furthermore, why not reduce costs by mounting those circuits on printed circuit cards the utility of which had already been proved in radar and other military electronics gear? By doing so, they could produce a high-speed, reliable, large-scale computing system at far less cost.

The result of this thinking was the prototype of the UNIVAC Solid-State Computer — the Cambridge Air Force Computer which Remington Rand installed for the armed services in 1956.

About the time that the basic specifications were being designed for the Cambridge Computer and its commercial counterpart, additional requirements, besides low costs, microsecond operating speeds, and reliability, also became critically important if the UNIVAC Solid-State 90 Magnetic Tape System was to become a commercial success. Paramount among these requirements was that of keeping the system as simple as possible for ease of customer operation, programming, and installation. Therefore, in the basic design specifications, all control circuits, not only for the computer, but also for the input-output units, were combined and built into the Central Processor.



These control sections consist of banks of printed solid-state circuit cards plugged into the front of the Processor. When called on by the program, some of these circuits execute the required arithmetic or logical operation. Others perform a check on the information, while still others coordinate and control the simultaneous operations of the three input-ouput units.



The above picture shows a typical printed circuit card. Although there are approximately one thousand printed circuits in the system, over 90 per cent of them are mounted on only eight types of solid-state cards. Thus, production is standardized, and maintenance is reduced to a relatively simple operation. Malfunctioning circuits are easily located, and removed from the Processor, and a new circuit card is quickly slipped into place. In addition to ease of production and maintenance, these solid-state circuits impart a high degree of operating reliability to the computer while reducing the power, cooling and space requirements of the system. As the superior reliability of solid-state circuitry eliminated the need for expensive duplicate self-checking circuits, in a similar fashion, the cost of duplicating off-line control circuits in the input-output units was also eliminated by combining them — that is, by making the same circuit do double or triple duty.

Another example of design simplicity was the use of a four level plus parity-bit machine code. In using this type of modified biquinary code, the design engineers ensured the maximum utilization of storage area. Furthermore, this code and the arithmetic and control circuits of the system most easily lent themselves to bit manipulation. Bit manipulation enables the machine to accept any type of coding — UNIVAC XS-3, punched-card alphanumerics, computer (machine biquinary), or any other type of statistical code which the user may require.

THE FULLY BALANCED SYSTEM

Because of the unique abilities of the UNIVAC Solid-State 90 Magnetic Tape System, the user can have fully balanced data-processing abilities — and have them at low operating costs. Not only is the system able to process large volume "bread and butter" operations economically, but also those applications previously avoided because of the excessive costs and time requirements. Now, in addition to the normal work-load requirements, the user can economically examine business problems by using such tools as linear programming, and Monte Carlo techniques or game theory to conduct inquiries into the entire field of Management and Operations Research.

2. Equipment Configuration

TAPE SYNCHRONIZER

Designed expressly for the UNIVAC Solid-State 90 Magnetic Tape System, the Tape Synchronizer directs the exchange of information between the Central Processor and magnetic tape storage. The Synchronizer then regulates the flow of input data read from tape into the system and of output data written onto tape from the Processor.

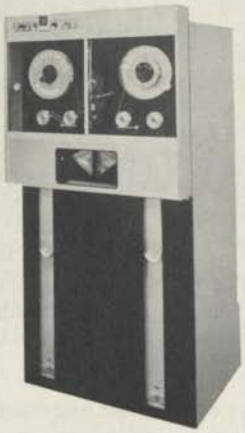
The instantaneous transfer rate of this information is 12,500 or 25,000 characters per second. For the transfer, the Synchronizer employs a full, 200-word buffer band on the high-speed drum. The five recording tracks of this band are served by four read-write heads per track.

All of the Synchronizer's activities are program-controlled.

METALLIC OR MYLAR TAPE

The tape itself is one-half inch wide and may be metallic or Mylar, used separately or in combination. The former is wound in reels of 1,500 feet, and the later, in reels of 2,400 feet. Tape reels are mounted on magnetic tape units called Uniservos II (described later). Tape speed and rewind speed are 100 inches per second. Reversal time is 600 milliseconds. Bits are recorded in parallel and characters serially at a density of 250 or 125 characters per inch. There are eight recording channels — one parity, two zone, four numeric and one sprocket. Thus, any 6-bit code plus an odd check bit may be employed — UNIVAC XS-3, standard Remington Rand card code, and USS-90 computer code.

TAPE FORMAT		
Tape Modes	UNIVAC USS-90	
Block Length	720 characters (UNIVAC block) 1,100 characters (1,000 data characters plus 100 signs) (USS-90)	
	@ 250 cpi	@ 125 cpi
Block Spacing	1.05 inches	2.4 inches
Start Time: Read Write	 12.05 ms 12.0 ms	 18.5 ms 18.8 ms
Stop Time: Read Write	 9.15 ms 11.1 ms	 16.25 ms 17.8 ms
Direction of Read	Forward and Backward	



MAGNETIC TAPE UNITS

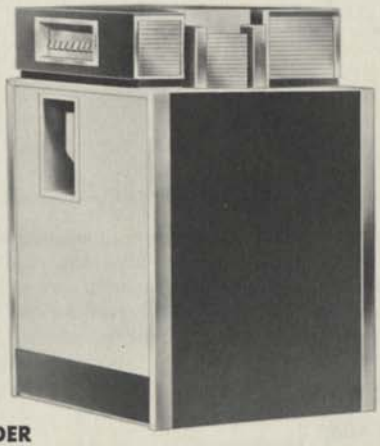
As many as ten magnetic tape units provide the UNIVAC Solid-State 90 System with extremely high-speed, accurate data input and output. Each unit may read data from tape moving in either a forward or backward direction, write on tape moving in a forward direction, and rewind its own tape.

The magnetic tape units are essentially the Uniservo II tape handling units that have proved so successful with other UNIVAC Systems. They are designed to permit fast tape mounting and ease of operation. A single switch on the front panel of each unit permits interchanging of metallic Unitape or Mylar tape as required.

A number of checks is provided to maintain the accuracy of information read or recorded in the various tape formats. Among them are the Forward and Backward Interlock Released Checks, the Control Check, the Information Transfer Check, the Tape Check, the Parity Check, and the Character-Count Checks. Moreover, bad spots in the tape are detected photoelectrically.

Reading and writing functions are controlled by program instructions stored within the Central Processor and coordinated by the Tape Synchronizer. Reading and writing are accomplished by magnetic read-write heads within each Uniservo. An erase head permits removing data from tapes entirely or in part. Old data is erased automatically before the recording of new data.

The Uniservo II will accommodate tape reels containing as much as 2,400 feet of Mylar tape or 1,500 feet of metallic Unitape. Tape wear is minimized by a plastic tape which is moved between the magnetic tape and the read-write heads. The plastic tape also removes dust and electrostatic charges from the magnetic tapes.



THE HIGH-SPEED READER

The High-Speed Reader is a major input component of the UNIVAC Solid-State 90 Magnetic Tape System. It reads data into the system from punched cards at a speed of 450 cards per minute.

This unit consists of a card input magazine, two read stations, and three output stackers. It also contains a motor to advance the cards and a monitoring control panel. Its operation is completely controlled by the program stored on the drum of the Central Processor. The presence of the two read stations permits the Processor to perform a complete verification and audit on all information entering the system.

OPERATION

Data cards stacked in the input magazine of the High-Speed Reader are fed into continuously revolving rollers that transport them through the two reading stations. Then, they are sent to one of the output stackers. During its course through the transport system, a

card conveys its contents to the computer when it is brush-sensed at each of the read stations in turn. Once inserted between the rollers a card moves without interruption until it reaches its designated stacker.

If it were possible to halt the Reader instantaneously in the midst of its card-cycling operation, the following situation would be revealed. To begin with, four cards would be committed to the system. The card labeled A, that was in transit from the input magazine, would be near the rollers, as shown in Figure 1. Depending on the exact stopping point in a cycle, the next two cards, designated B and C, would be either at or approaching each of the reading stations. The progress of the fourth card, labeled D, would have been suspended at some point on its way to an output stacker. Thus, it becomes apparent that the ability to feed, read, and select cards at the same time enables the High-Speed Reader to sustain its input speed at a maximum rate.

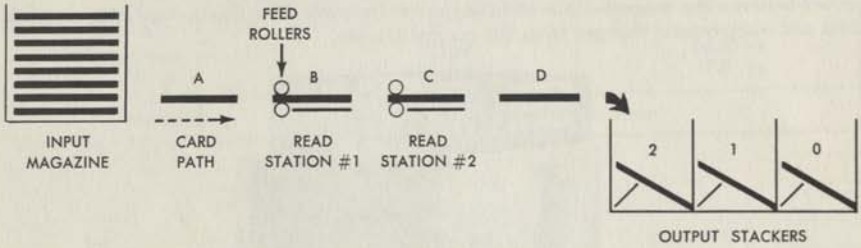


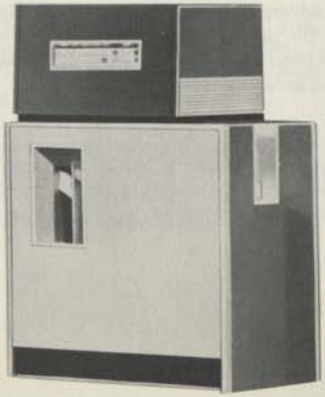
FIGURE 1. Functional Diagram of the Transport Mechanism of the High-Speed Reader

This entire cycle in the High-Speed Reader requires approximately 133 milliseconds to execute. However, because the unit is buffered, the Processor requires only three word times (.051 milliseconds) to initiate a card cycle, three more to execute the stacker select instruction, and 203 (3.45 milliseconds) to transfer both card images from the buffer band into main storage — a total of only 3.55 out of 133 milliseconds. With the buffers, therefore, it is possible to completely balance the system — executing simultaneous read, write, and compute operations while entering cards at the maximum rate of 450 per minute.

INPUT VERIFICATION AND AUDIT

Information sensed at Read Station #1 is compared with that sensed at Read Station #2. This comparison consists of a hole-by-hole (binary bit-by-bit) comparison within the Central Processor. Where required, this subroutine can be expanded to perform various auditing functions, such as a Modulus 11 Check Digit Verification, and so on. Error cards, therefore, can be detected at the time they occur and immediately outfiled into a designated stacker.

THE READ-PUNCH UNIT



The Read-Punch Unit is both an input and an output component of the UNIVAC Solid-State 90 Magnetic Tape System. It reads information from cards into the system or punches computed results at a speed of 150 cards per minute.

This unit consists of an input magazine, a first read station, a punch station, a second or post read station, and two output stackers. In addition, it contains its own motor and a monitoring control panel.

OPERATION

Since the Read-Punch Unit functions as both an input and output device, its card movement differs from that of the High-Speed Reader. Between the card cycles, except during the initial and final phases of a program, cards are disposed throughout this unit's transport system as follows:

Cards awaiting processing are stacked in the input magazine while three others, one at each station, are engaged as shown in Figure 2. This figure depicts Card B at the punch station. Figure 2 shows Card C and A at Read Stations #1 and #2 respectively.

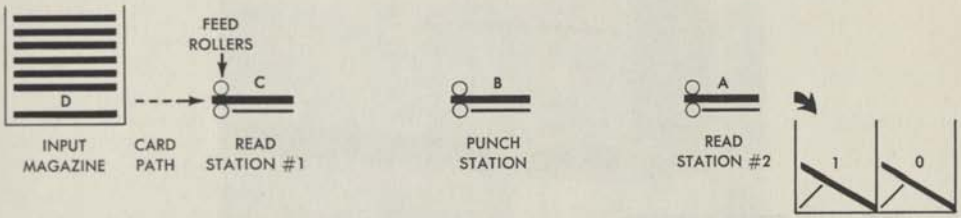


FIGURE 2. Functional Diagram of the Transport Mechanism of the Read-Punch Unit

When a card cycle instruction is given, a series of actions constituting a cycle is automatically performed. Output information is transferred from the storage band to the Punch Buffer, and the Central Processor is released for other operations. Card B is punched, and Cards A and C are sensed. All the cards are then advanced one station. The image of Card A is available for verification, and stacker selection may be performed.

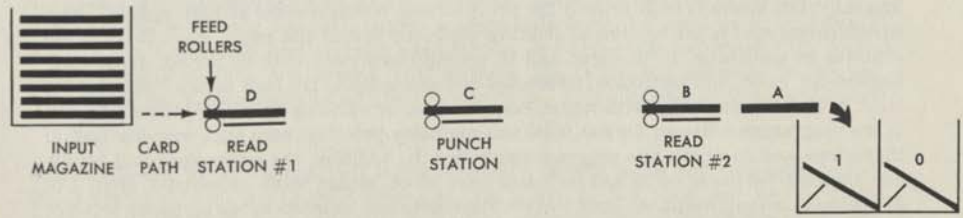
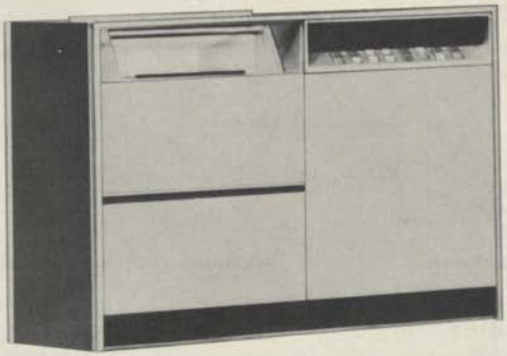


FIGURE 3. Functional Diagram of the Transport Mechanism of the Read-Punch Unit

Actual computer time required to load and unload the Read-Punch Unit buffer storage areas and to set up the required circuits for the stacker selection is approximately 1.7 per cent of the unit's card cycle time. Thus, while operating at 150 cards per minute (or at a 400 millisecond card cycle rate), the entire operation requires only 7.02 milliseconds of computer time. Therefore, there is ample time for:

1. Performing the hole-for-hole or pattern input-output audit.
2. Determining which stacker the card is to enter.
3. Computing.
4. Simultaneously operating the High-Speed Reader and the High-Speed Printer.
5. Sensing and punching at the continuous rate of 150 cards per minute.



THE HIGH-SPEED PRINTER

The High-Speed Printer is the same 600-lines-per-minute printer which has been used so successfully with the UNIVAC I and UNIVAC II Systems since 1954. The only difference between this and the previous models is that the control circuits are now inside the Central Processor. The Printer is optional with the UNIVAC Solid-State 90 Magnetic Tape System.

The function of this unit is to print output information, intermediate results, distributed accumulations and balances, and final reports. Like the other units, it is completely buffered and program controlled.

Basically, this device is built around 130 print wheels which revolve at high speeds. These wheels correspond to the horizontal printing positions across the page. Each print wheel contains 26 alphabetic, 10 numeric, and 15 special characters, such as period, dollar sign, ampersand, colon, and semicolon. Character spacing is ten to the inch across. Line spacing is six to the inch vertically with single, double, triple or variable spacing options available to the programmer. Report format, dual and multiline printing, zero suppressions, special characters, and so on are also program-controlled. In addition, the paper feed will handle any sprocket-fed paper up to and including card stock, either blank or printed, from 4 to 21 inches in overall width. At least five carbon copies can be made by using paper between

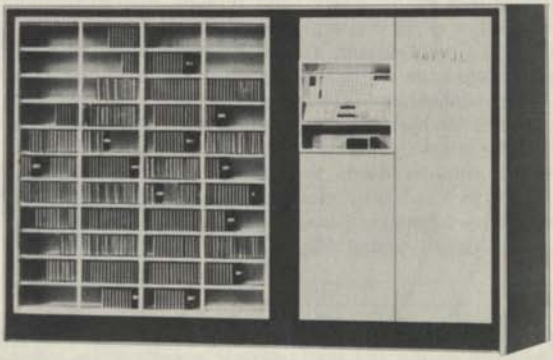
11 and 13.5 pounds in weight. The Printer will stop automatically on detection of a low paper supply. Moreover, impression control permits variation in the strength of the printing hammer stroke. And finally, fine vertical adjustments of the paper position may be made while the Printer is in operation. No plugboard is required.

OPERATION

The High-Speed Printer operates as follows:

1. Information to be printed is transferred by programmed instruction to the Print Buffer on the magnetic drum. Once this is accomplished, the computer is available for other operations.
2. The High-Speed Printer then advances the paper to the required printing line, prints the information and performs all the required checks. These consist of parity checks, comparisons of data to be printed with data stored in the buffer, and checks to see that all information has been printed.

Because this unit is essentially a wheel printer, the type fount produces clearly-printed copy similar to that printed by a typewriter or conventional punched-card tabulating equipment.



CENTRAL PROCESSOR

Under the guidance of an internally stored program, the Central Processor controls the many interdependent activities of the UNIVAC Solid-State 90 Magnetic Tape System and houses the main storage area as well. Adhering to the instructions in the control unit of the Central Processor, logical circuitry accepts data from the input units, transfers it between the arithmetic and storage components, and transmits processed data to the output units. Similarly, the control unit governs the arithmetic elements in the performance of such operations as addition, subtraction, multiplication, division, and logical comparisons.

Related directly to the control unit is the operator's control panel and keyboard, both of which are located on the Central Processor. By means of the panel and keyboard, the system's operations can be interrupted for the insertion of data or the display of the con-

tents of addressable registers or of any storage location. The design of the control panel and keyboard reduces to a few simple steps the formerly complex procedures of starting, intervention, error-detection, and corrective action.

Along with this thorough control, the Central Processor provides storage for 50,000 digits on its magnetic drum. Experience has proven that storage of such magnitude is able to accommodate large volumes of data and instructions while still reserving ample room for tables created during operation.

The Central Processor is extremely fast. It has a transfer rate of 707,000 characters per second. Thus, it is capable of performing 705,600 additions or subtractions per minute. These speeds are augmented by the programming flexibility of the computer. Registers A, X, and L are directly addressable. Finally, the presence of buffer test instructions eliminates time-consuming interlocks when the external units are not immediately available for processing.

MAIN STORAGE

The main storage area, located on the high-speed (17,670 rpm) magnetic drum, is divided into a high-speed and a standard access section as shown in Figure 4. These segments are further subdivided into bands. Every band in main storage accommodates 200 computer words, each consisting of 10 digits plus sign. Bands 1 through 20, the maximum access time of which is 3.4 milliseconds, comprise the standard access portion of the drum. The high-speed access sector, on the other hand, is composed of five bands with a maximum access time of .85 milliseconds. Standard access bands are equipped with one read-write head per band, while the high-speed access bands are serviced by four read-write heads, spaced at 90 degree intervals around the circumference of the bands. Since each storage band contains 200 computer words, the difference in access time between the high-speed and standard access sectors is accounted for by the number of read-write heads that service a band. Access time is important because it influences the programmer's choice of storage locations for both instructions and data.

BUFFER STORAGE

Buffer storage, which compensates for the disparity between the Central Processor's electronic speed of computation and the mechanical speed of the input-output units, is also located on the high-speed drum. There are seven buffers, one for the Tape Synchronizer, two for the High-Speed Reader, three for the Read-Punch Unit, and one for the High-Speed Printer. All input and output information flowing from main storage to the external units and vice versa must pass through these buffers. In this way, with the buffers acting as an intermediary, the main storage never becomes involved with the external units. Instead, the main storage communicates only with the buffers, which transmit or receive information at electronic speeds. Another advantage of buffer storage springs from the fact that it can send data to, or receive data from the external units automatically, thus leaving the computer control section free to continue directing the processing of data.

TIMING BAND

The timing band, also located on the magnetic drum, synchronizes the operations of the system by sending various types of timing pulses to the control, arithmetic, and input-output units. This band also controls the addressing of storage locations.

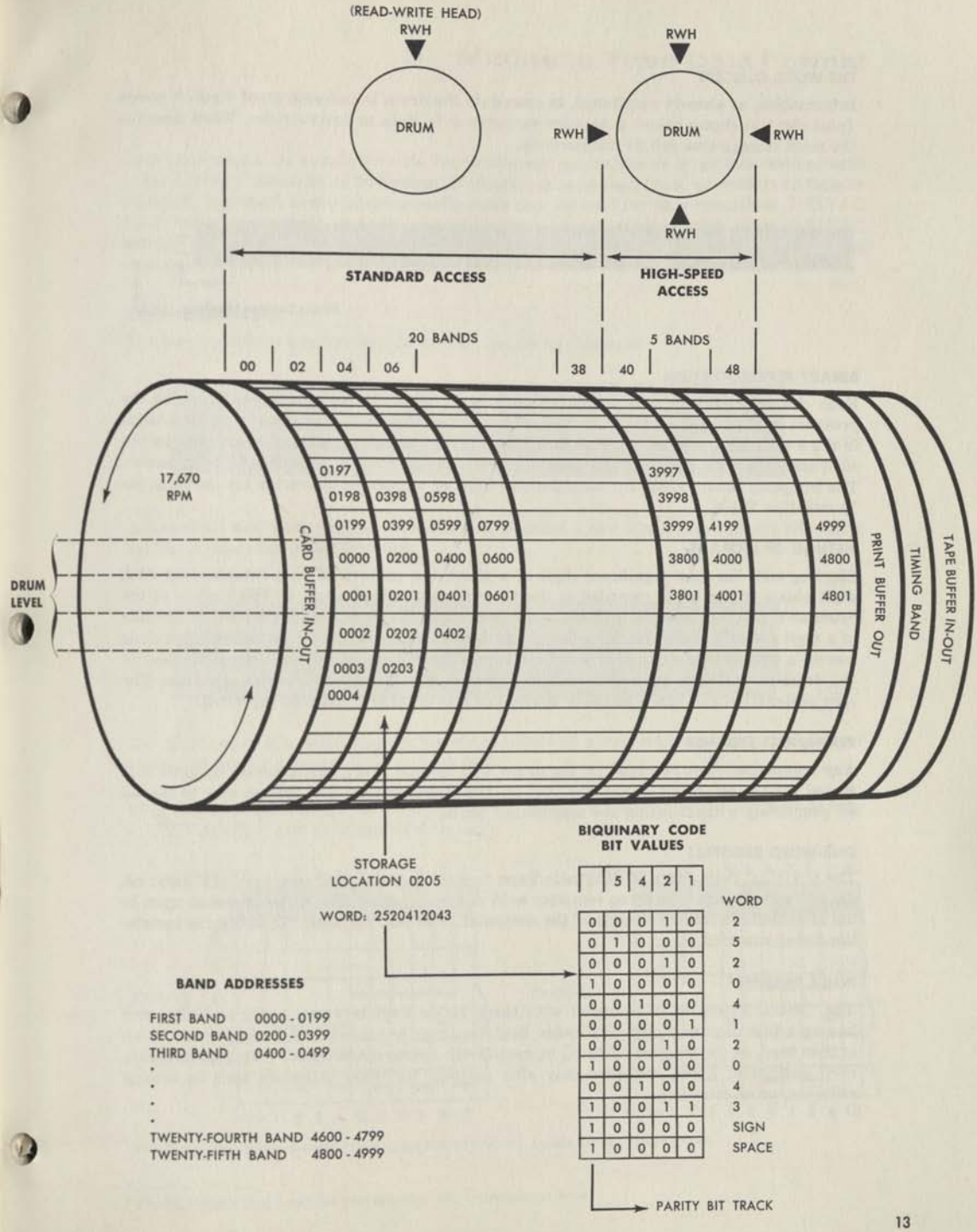
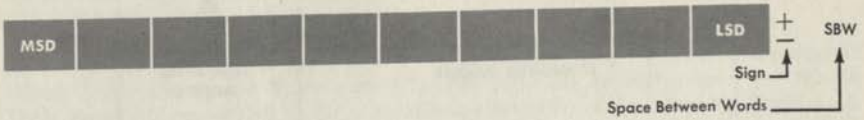


FIGURE 4. Magnetic Storage Drum

THE WORD CONCEPT

Information, as already mentioned, is stored on the drum in increments of 10-digit words (plus sign) as shown below. Computer words may be data or instructions. Word time for the main storage area is 0.17 milliseconds.



BINARY REPRESENTATION

Each character position of a computer word contains five binary positions in which the presence or absence of a bit has significance. Four of these bit positions represent a value in the 5 4 2 1 binary-coded decimal code. The fifth bit is a check bit and is assigned by the computer in such a way that the total number of binary "1's" in a digit is an odd number. The computer binary codes for each decimal digit or alphabetic character are shown in the Translation Table.

METHOD OF STORAGE

Starting with the most significant digit of a word, the pattern of bits representing each digit plus a parity bit is recorded in the form of magnetized spots on the surface of the drum as it revolves beneath the read-write heads. At the instant of writing, the five bits of a digit are entered in parallel across a band, each being deposited on a track, which is merely a further vertical subdivision of a band. The remainder of the word is written on the drum in the same manner — serially; that is, digit-by-digit, five bits at a time. The sign designation and space between words are also entered as part of the word.

PERMANENT STORAGE

Any magnetized spot recorded on the drum will remain there permanently or until it is erased for the recording of another spot on the same location. The system may be turned off completely without losing the magnetized spots.

ONE-WORD REGISTERS

The UNIVAC Solid-State 90 Magnetic Tape System contains four one-word registers: rA, rX, rL, and rC. The first three registers hold data or instructions to be operated upon by the arithmetic or control circuits of the computer. The last register, rC, holds the instruction being executed.

INDEX REGISTERS

The Central Processor is equipped with three Index Registers: rB_1, rB_2, and rB_3, each having a four-digit capacity. The Index Registers may be loaded with an increment which is then used, as the program directs, to modify the operand address of instructions before their execution. These registers may also be used for other purposes such as setting switches, or as counters.

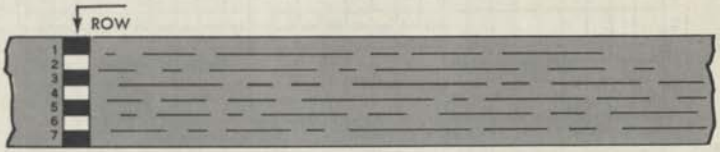
3. Magnetic Tape Data Format

Data must appear in computer code for arithmetic operations or magnitude comparisons in the UNIVAC Solid-State 90 System. Normally, data is read from, or written on tape in this code. However, any 6-bit-plus-parity code may be used for tape operations. UNIVAC XS-3 code, for example, may be employed when communication with other UNIVAC systems is required. For the purposes of illustration, UNIVAC XS-3 code is used for the most part, in the figures in this section.

TAPE CHANNELS

The tape is divided lengthwise into seven* recording channels.

A line of bit positions, one for each channel, is called a row. Each row contains bits representing a character of information.



Combinations of bits appearing within six positions of a row represent various character codes. The first or topmost bit is a check bit.

With the check bit disregarded, the numbers 1 through 9 and 0 appear in ten rows on tape in UNIVAC XS-3 and in computer code as:

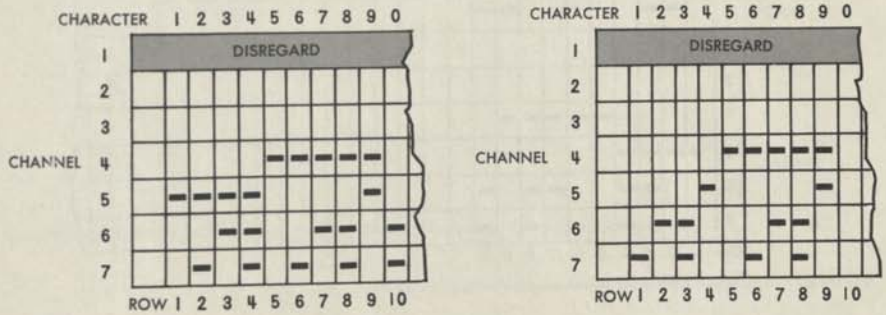


FIGURE 5. Numeric Representation on Tape in UNIVAC XS-3 Code and in Computer Code

* *The eighth channel, used for the sprocket bit, is irrelevant here.*

The alphabet in UNIVAC XS-3 code appears in 26 rows on tape thus:

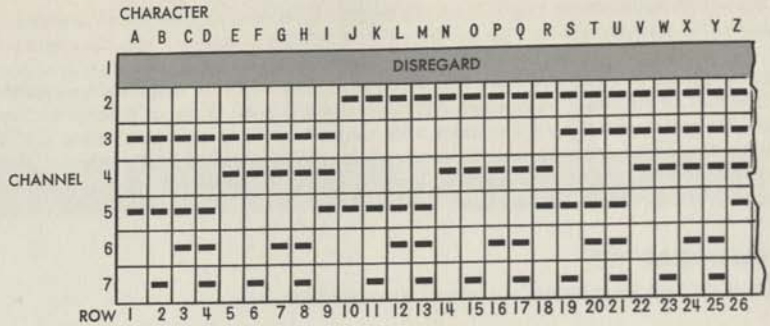


FIGURE 6. Alphabetic Representation on Tape

When the number of bits ("1's") present in a row is even, a parity bit is assigned to the first or check position. If the number of bits in a row is odd, no parity bit appears in that position. The numbers 1 through 9 and 0, and the alphabet are shown below in UNIVAC XS-3 code with parity bits.

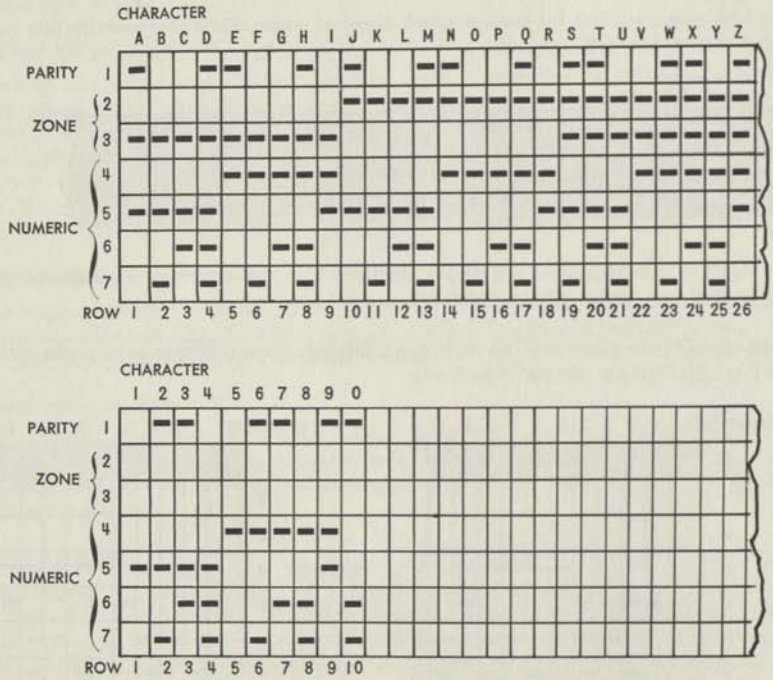


FIGURE 7. Numeric and Alphabetic Representation on Tape (with Parity Bits)

TRANSFER OF DATA BETWEEN TAPE AND BUFFER BAND

When transferred from tape to the buffer, the bits of a character are arranged by the Synchronizer in corresponding digit positions of two computer words. The zone bits (appearing in tape channels 2 and 3) are assigned to one of the words, called the primed word. The numeric bits (from channels 4, 5, 6 and 7) are placed in the other or unprimed word.*

Numbers 1 through 9 and 0 are arranged in two computer words in UNIVAC XS-3 code in this way:

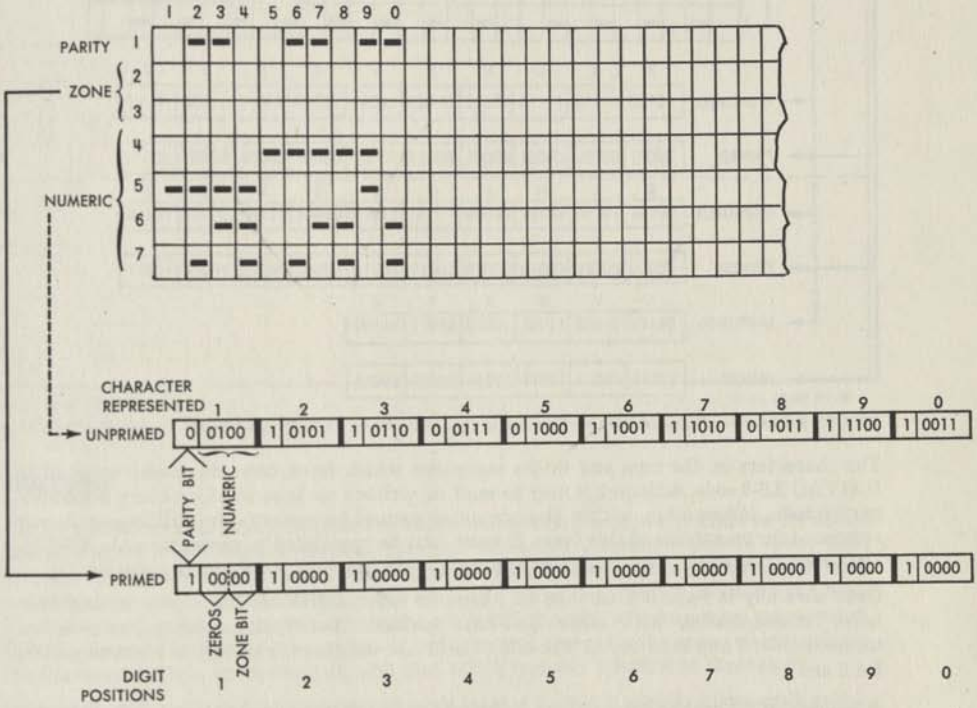


FIGURE 8. Numeric Representation on Tape and in the Computer in UNIVAC XS-3 Code

* *Although the Synchronizer checks the parity bit from tape, it assigns new parity bits for both the zone and numeric parts of a character for storage within the computer word.*

Figure 9 depicts three pairs of computer words containing the letters of the alphabet in UNIVAC XS-3 code.

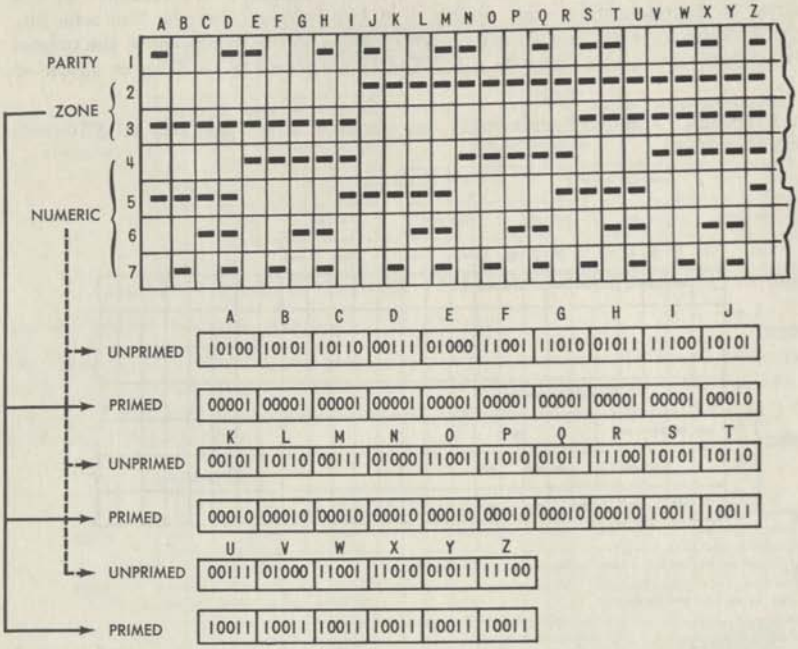


FIGURE 9. Alphabetic Representation on Tape and in the Computer in UNIVAC XS-3 Code

The characters on the tape and in the computer which have been discussed were all in UNIVAC XS-3 code. Although it may be read or written on tape in this or any 6-bit-plus-parity code, information within the computer cannot be operated on arithmetically nor compared for magnitude in this form. It must first be translated to computer code, USS-90. Data read from or written on tape in computer code, however, needs no translation.

Data normally is recorded on tape in computer code; UNIVAC XS-3 code is used only when communicating with other UNIVAC Systems. Word pairs in computer code are termed numeric and zone words. The bits of both are weighted from left to right as parity, 5 4 2 and 1.

A numeric word containing numbers 1 through 9 and 0 in computer code appears in the computer thus:

CHARACTER REPRESENTED	1	2	3	4	5	6	7	8	9	0
	P5421	P5421	P5421	P5421	P5421	P5421	P5421	P5421	P5421	P5421
NUMERIC	00001	00010	10011	00100	01000	11001	11010	01011	11100	10000

FIGURE 10. Numeric Representation in the Computer in Computer Code

In a similar manner, the 26 letters of the alphabet appear in computer code in six computer words, as shown in the section captioned "The 90-Column Punched-Card Format." The UNIVAC XS-3 and computer codes are listed in the Translation Table at the end of this manual.

4. The 90-Column Punched-Card Format

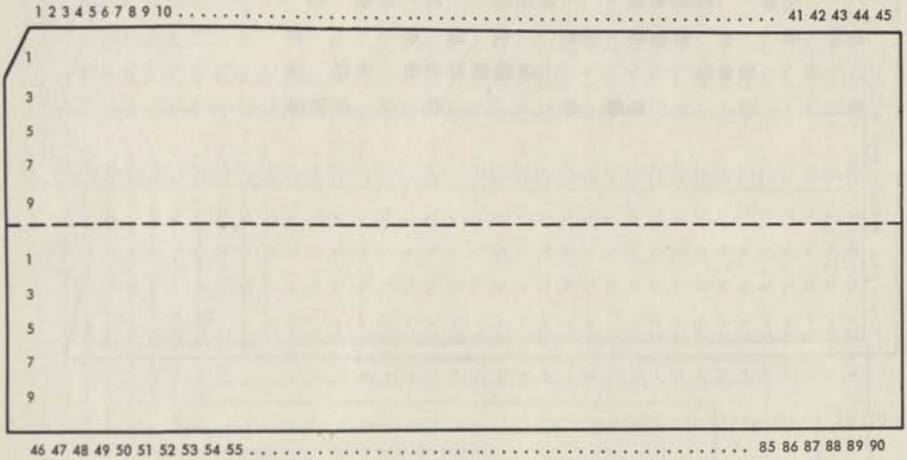


FIGURE 11. The 90-Column Punched Card

THE CARD

The 90-column punched-card is divided in half horizontally. The upper half (above the dotted line in Figure 11) contains vertical columns numbered 1 through 45; the lower half, columns 46 through 90. A group of vertical columns signifying a unit of information, such as an employee badge number or employee name in a payroll application, is known as a field. The number of columns comprising a field varies with the type of information represented. Usually, the card is divided into groups of ten columns, except for the group which includes the five columns from 41 through 45, and that which includes columns 86 through 90.

Each card half is divided into horizontal rows labeled 1, 3, 5, 7, and 9. Above each row 1, there is another, referred to as the 0 row.

REPRESENTING NUMERIC AND ALPHABETIC CHARACTERS

On the card, an odd decimal digit is represented by a single hole punched in the row with a corresponding value. Thus, 1 is represented by a punch in row 1; 3 by a punch in row 3, and so on. Even numbers are represented by a punch in row 9 and in the row having the value immediately preceding the number to be represented. Naturally, both the 9 and the other punch must fall in the same vertical column. In this way, 2 is represented by 9 and 1 punches; 4, by 9 and 3 punches, and so on.

The letters of the alphabet are represented on a card by a combination of 2 or more punches within the same vertical column. Figure 12 illustrates the alphabet punched on a 90-column card.

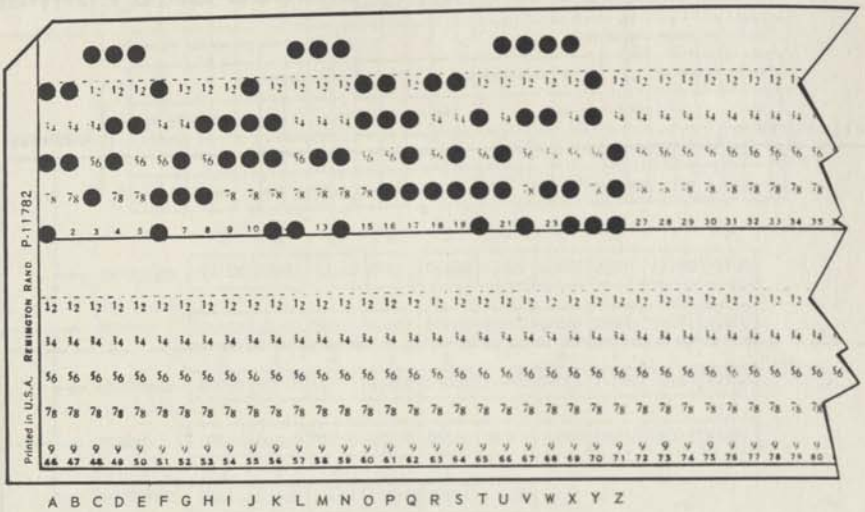


FIGURE 12. Alphabetic Character Representation

CARD CODE TO COMPUTER CODE

In 90-column card code the data from a ten-column card group occupies two computer words. The first digit positions of both words contain the information from the first column; the second digit positions, the information from the second column, and so on.

The computer word which represents the card positions 5, 3, 1, 0, is called the unprimed word. The word representing positions 9 and 7 is called the primed word. Figure 13 depicts the relationship as it applies to the numbers 1 through 9 and 0 punched in card code. It shows these numbers recorded from left to right in the first ten columns of a card and their appearance in two computer words in card code.

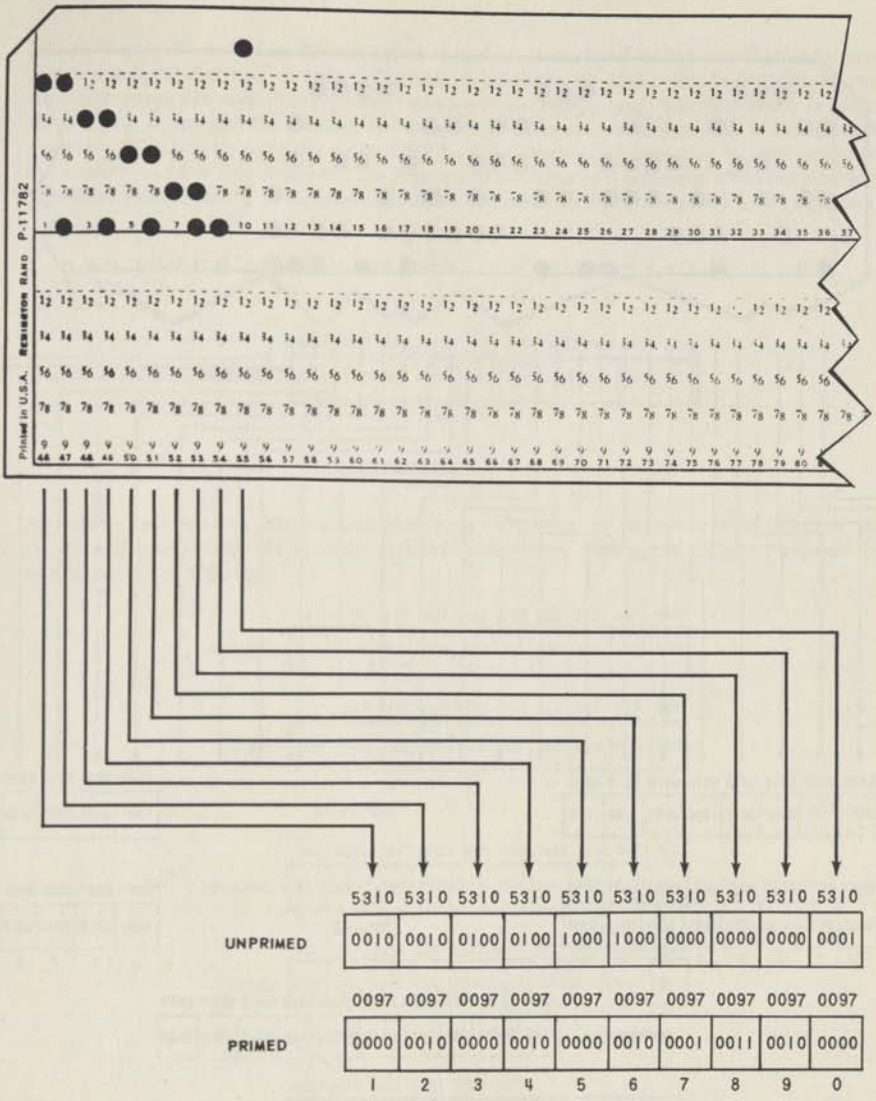


FIGURE 13. Numeric Representation on the Card and in the Computer in Card Code

It can be seen from the above figure and Figure 14 on the following page that both letters of the alphabet and the numbers 1 through 9 and 0 appearing in card code are represented in unprimed and primed digits. The four bits of each unprimed digit from left to right denote punch positions 5, 3, 1, 0. The bits of each primed digit represent punch positions 9 and 7. The two bit positions before 9 and 7 are zeros and are of no significance here.

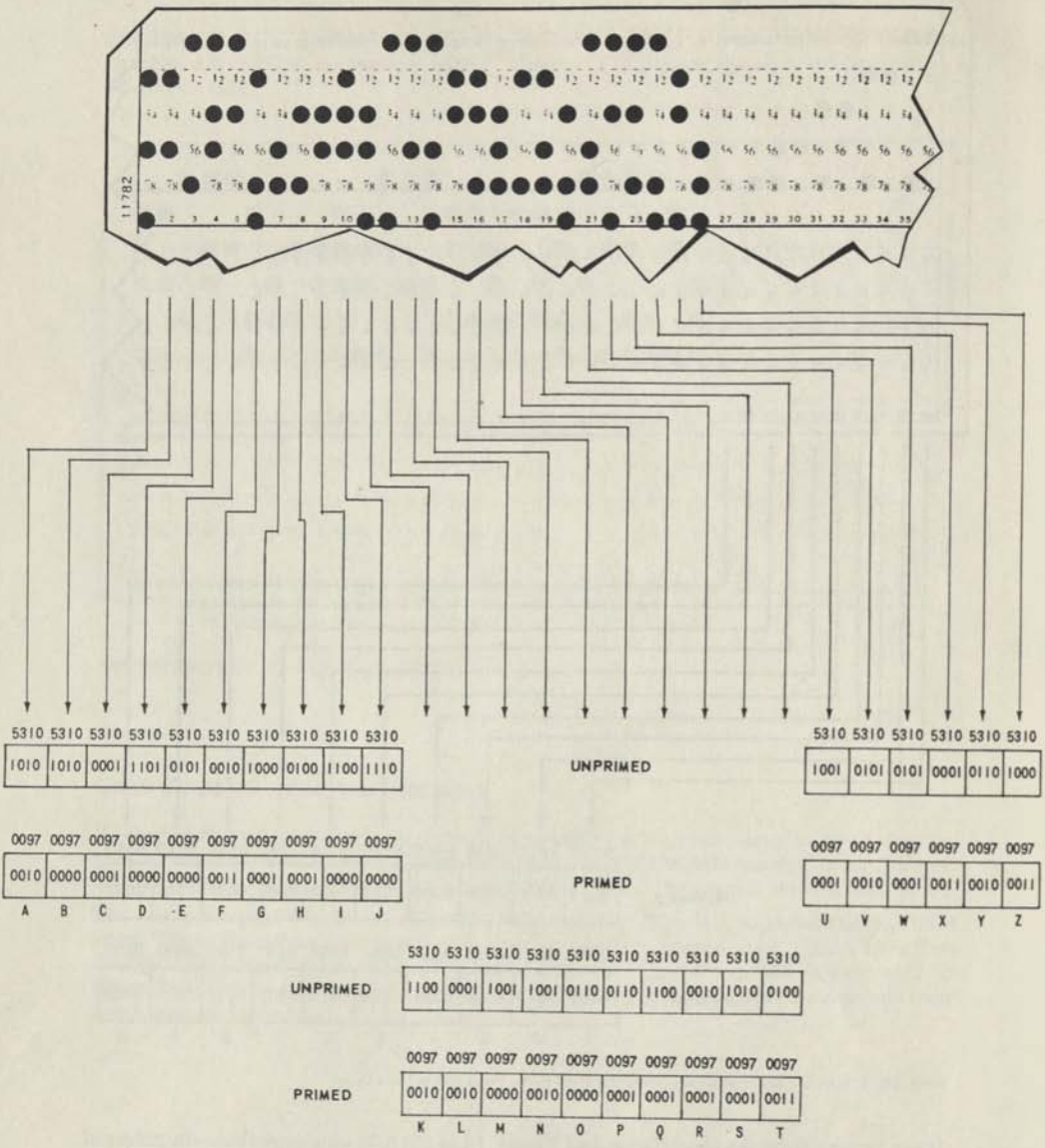


FIGURE 14. Alphabetic Representation on the Card and in the Computer in Card Code

When information coded in 90-column card code is translated to the modified biquinary that is the computer code for the UNIVAC Solid-State 90 Magnetic Tape System, two computer words are needed to represent a ten-column card group. The first word is called the numeric word, and the second, the zone word. The bit positions of both these words represent from left to right the value 5 4 2 1. With card-coded data that is numbers only, the numeric word is significant but the zone word contains zero bits only. Thus the numbers 1 through 9 and 0 would be represented in one computer word in *computer code* as follows:

	5421	5421	5421	5421	5421	5421	5421	5421	5421	5421
NUMERIC	0001	0010	0011	0100	1000	1001	1010	1011	1100	0000
	1	2	3	4	5	6	7	8	9	0

Alphabetic information when translated from 90-column to computer code requires the presence of bits in both the numeric and the zone words. Hence, the alphabet appears in *computer code* as follows:

	5421	5421	5421	5421	5421	5421	5421	5421	5421	5421
NUMERIC	0001	0010	0011	0100	1000	1001	1010	1011	1100	0001
ZONE	0001	0001	0001	0001	0001	0001	0001	0001	0001	0010
	A	B	C	D	E	F	G	H	I	J

	5421	5421	5421	5421	5421	5421	5421	5421	5421	5421
NUMERIC	0010	0011	0100	1000	1001	1010	1011	1100	0010	0011
ZONE	0010	0010	0010	0010	0010	0010	0010	0010	0011	0011
	K	L	M	N	O	P	Q	R	S	T

	5421	5421	5421	5421	5421	5421				
NUMERIC	0100	1000	1001	1010	1011	1100				
ZONE	0011	0011	0011	0011	0011	0011				
	U	V	W	X	Y	Z				

Certainly then, both the numeric and zone words must be considered in operations using computer-coded alphabetic information. Naturally, when a card field containing both numbers and letters is translated to computer code, both the numeric and zone words are meaningful.

SPECIAL SYMBOLS

Special symbols appear in the computer in *card code* as:

	5310	5310	5310	5310	5310	5310	5310	5310	5310	5310
UNPRIMED	1110	1111	1101	1011	1100	0011	1101	1111	1011	0000

	xx97	xx97	xx97	xx97	xx97	xx97	xx97	xx97	xx97	xx97
PRIMED	0010	0010	0001	0001	0011	0000	0010	0001	0000	0000
	.	$	—	#	/	*	,	&	%	Δ

The same symbols appear in *computer code* as:

	5421	5421	5421	5421	5421	5421	5421	5421	5421	5421
NUMERIC	0101	0101	0101	1111	0001	0110	0101	0111	0110	0110

	5421	5421	5421	5421	5421	5421	5421	5421	5421	5421
ZONE	0001	0010	0000	0001	0011	0010	0011	0001	0011	0000
	.	$	-	#	/	*	,	&	%	Δ

Other symbols appear in *computer code* as follows:

	5421	5421	5421	5421	5421	5421	5421	5421	5421	5421	5421
NUMERIC	0110	0000	1110	1111	1101	0111					

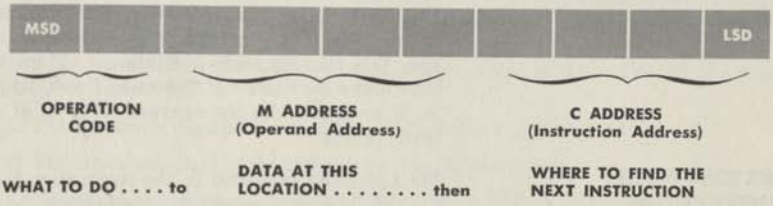
	5421	5421	5421	5421	5421	5421	5421	5421	5421	5421	5421
ZONE	0001	0011	0000	0000	0000	0000					
	:	+	;	'	(	)					

These and other symbols are found in the Translation Table at the end of this manual.

5. Instructions

GENERAL

The UNIVAC Solid-State 90 Magnetic Tape System employs a one and one-half address instruction code system with one instruction per computer word. The format of an instruction word is illustrated below:



The m address is usually the address of a word in storage. The operation code tells the computer what to do with this word; the c address is the storage location of the next instruction word. These fields may have different significance for some special instructions, as noted in the instruction definitions.

The m address of instructions can be modified through the use of an Index Register. Such modification adds one word time to the instruction cycle.

When a word is transferred from a storage location or register, the contents of the storage location or register from which the word was transferred remain unchanged.

When a word is transferred into a storage location or register, the previous contents of the location or register are erased, except in the 20 and 35 instructions.

INSTRUCTION CYCLE

A three- or four-step cycle (with an additional step if Index Registers are used) is associated with each instruction depending upon whether an operand is required from drum storage. If setting-up the instruction is considered the starting point, the instruction cycle is:

Staticize the Instruction	Index Register Modification (if any)	Search for the Operand	Execute the Instruction	Search for the Next Instruction
(1)	(2)	(3)	(4)	(5)

(1) STATICIZE THE INSTRUCTION: The instruction located by the previous search (5) is transferred from the drum location to the Static Register (operation code only) and register C (the entire word). This step requires one word time, which is .07 milliseconds.

(2) INDEX REGISTER MODIFICATION: When modification is indicated, the m address of the instruction is altered by the Index Register specified. This step requires one word time.

(3) SEARCH FOR THE OPERAND: If the first address part — the m address — of the instruction refers to a drum storage location, the address of the next available storage location on the drum is compared with the first address part of the contents of register C every word time until a match is obtained. Register C contains the entire instruction. If an operand is required from storage, this step requires a minimum of one word time and a maximum of 200 word times. Register A, X or L may be the operand address of most instructions.

(4) EXECUTE THE INSTRUCTION: The operation indicated in the instruction is performed. The time required depends upon the type of operation to be performed.

(5) SEARCH FOR THE NEXT INSTRUCTION: Every word time the address of the next available storage location on the drum is compared with the second address part — the c address — of the contents of register C until a match is obtained. This step requires a minimum of one word time.

ADDRESS MODIFICATION WITH INDEX REGISTERS

If an instruction is to be modified by the use of Index Registers, it must contain an indication of the Index Register to be used. The indication is a combination of the sign bit and the second or least significant digit of the operation code. Only the 4 bit of the 5 4 2 1 bits of this digit is used. Since this bit is not utilized in the least significant digit of any operation code, the normal execution of an instruction is not otherwise affected. The Index Register must be loaded initially with the desired increment.

The four combinations of the two bit-positions are interpreted as shown in the table below:

MODIFICATION TABLE

Sign Bit	0 5421	C 5421	Condition	Type of Modification
0	XXXX	X0XX	0	No modification
0	XXXX	X1XX	1	Modify with Index Register 1 (rB_1)
1	XXXX	X0XX	2	Modify with Index Register 2 (rB_2)
1	XXXX	X1XX	3	Modify with Index Register 3 (rB_3)

Normally the programmer is not concerned with these indications when he writes instructions. The specification is made in the translation key and is handled automatically by the load routine.

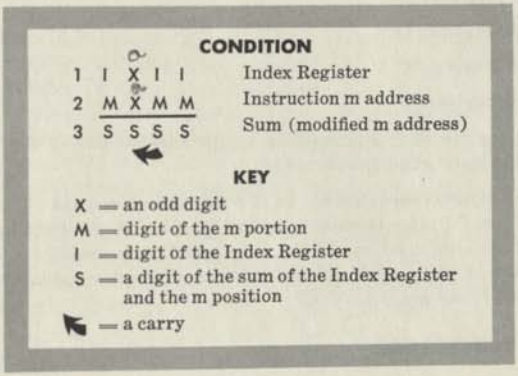
During the staticizing phase all instructions are examined for the presence of one of the above conditions. If condition 0 is found to be present, the modification phase is bypassed, and the instruction is executed in the normal manner with a three- or four-phase cycle. If condition 1, 2, or 3 exists, however, the second phase of the instruction cycle is the addition of the specified Index Register's contents to the m address of the contents of register C. The computer then searches for the new m address during the third phase, and the execution of instructions proceeds in the normal manner.

BAND MODIFICATION FEATURE

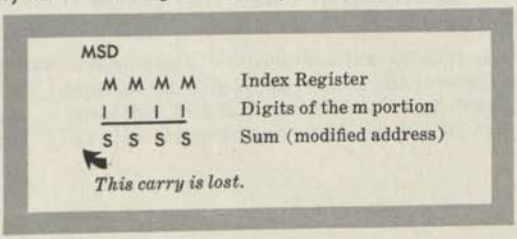
A band modification feature enables modification with Index Registers to be restricted to the same band in which it was initiated. If, during modification, the m address is altered to refer to another band, the computer will cause a return to the corresponding location in the original band. This band modification occurs when at least two of the following conditions are present:

1. The hundreds digit of the contents of the Index Register is odd.
2. The hundreds digit of the instruction's m address is odd.
3. During modification a carry occurs from the tens digit to the hundreds digit.

The figure below represents the conditions which, in combination, cause band modification to be effected.



Note: When the four digits of the m address are added to those of the Index Register, any carry from the most significant digit position is lost.



ADDRESSABILITY OF REGISTERS

As a result of their addressability, register A, X or L may be the m address of many, and the c address of all instructions. The sole restriction is that they cannot be used in the m portion of the 50, 60 and 65 orders, nor in the m portion of instructions which do not address a one-word storage location. The arithmetic registers are addressed by non-numeric digits in the least significant digit of c or m.

	LSD of m or c	
	BITS	DIGIT
rA =	0101	1/4
rX =	0111	3/4
rL =	0110	2/4

INSTRUCTION REPERTOIRE

The following pages contain descriptions of the instructions used with the UNIVAC Solid-State 90 Magnetic Tape System. In the descriptions, the following conventions are used:

- m represents the address of a storage location or register which usually contains the operand
- c represents the address of a storage location or register which usually contains the next instruction
- (m) represents the contents of a storage location or register
- rA represents register A
- rL represents register L
- rC represents register C
- rX represents register X

A dash substituted for the m or c portion of an instruction means the computer ignores that portion when the instruction is executed.

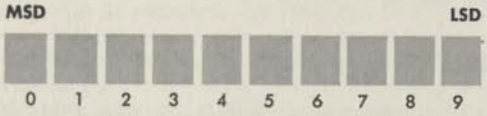
The timing for each instruction is shown in the right-hand column following the description of the instruction. Timing is shown as the number of word times required for the instruction cycle in minimum latency. One extra word time should be added when Index Register modification is to be accomplished. Timing in milliseconds can be obtained by multiplying the word times given by 0.017.

ARITHMETIC INSTRUCTIONS

		WORD TIME
70 m c	Add algebraically (m) to (rA) and place the sum in rA.	5
75 m c	Subtract algebraically (m) from (rA) and store the difference in rA.	5
85 m c	Multiply (rL) by (m) and store the 10 most significant digits of the product in rA and the 10 least significant digits in rX. Both rA and rX will have the sign of the product. Multiplication can be	5 plus the number of digits in the multiplier plus the sum of these digits.

shortened for multipliers having less than 10 significant digits by placing a sentinel just to the left of the most significant digit of the multiplier, m. This sentinel stops the multiplication after the last significant multiplier digit is used. Sentinel (0101 or 1101).

55 m c — Divide (m) by (rL). The quotient with sign is placed in rA unrounded, and the remainder is placed in rX. If the divisor is zero, or is equal to or less than the dividend, overflow occurs. A sentinel may be placed in rX to stop the division after the desired number of digits has been developed in the quotient. For the placement of the sentinel, the digit positions are numbered, *from left to right, 0 through 9*, instead of the usual way (1 through 10). — 5 plus two times the number of digits in the quotient plus the sum of the odd digit-positions in the quotient plus the sum of the nines complement of the even digit-positions in the quotient.



Digit position for division sentinel only

The sentinel (0101) is placed as follows:

PURPOSE	POSITION	
To develop 2 digits in the quotient —	2	All other positions must contain zeros
To develop 4 digits in the quotient —	4	
To develop 6 digits in the quotient —	6	
To develop 8 digits in the quotient —	8	

To develop 10 digits in the quotient, the contents of rX need not be changed, providing that the non-numeric bit combination (0101) is not present in rX. If there is a possibility that it is present, the program should fill rX with zeros.

NOTE: If an overflow occurs during the add, subtract or divide operations the next instruction is obtained from storage location c + 1. If the c address is on drum level 199, overflow will cause control to revert to the instruction on level 000 of the same band. Also, if an arithmetic register is used as the c address of an instruction which happens to cause overflow, the next instruction is still taken from the addressed register — after a delay of one word time.

TRANSFER INSTRUCTIONS

25	m c	Transfer (m) to rA.	4
*60	m c	Transfer (rA) to m.	4
05	m c	Transfer (m) to rX.	4
*65	m c	Transfer (rX) to m.	4
30	m c	Transfer (m) to rL.	4

* *m may not be register A, X, or L.*

			WORD TIME
*50	m c	Transfer (rL) to m.	4
77	—c	Transfer (rA)to rL.	3
06	m—	Clear rX to zero and set its sign storage to plus. Ignore c. Next instruction at m.	3
26	m—	Clear rA to zero and set its sign storage to plus. Ignore c. Next instruction at m.	3
31	m—	Clear rL to zero and set its sign storage to plus. Ignore C. Next instruction at m.	3
86	m—	Clear rA and rX to zero. The signs of rA and rX assume the sign of rL. The next instruction is at m.	14
23	m—	The contents of rC are transferred to rA. The next instruction is at m.	3

LOGICAL INSTRUCTIONS

BUFF

20	m c	Superimpose or buff the 1 bits of (m) onto (rA) and leave the result in rA. The sign of rA is undisturbed.	4

ERASE

35	m c	Change the bits in each digit position of (rA) to binary zero wherever (m) has a 0 bit in the corresponding bit position. The sign of rA is undisturbed.	4

Note: In the following shift instructions, the m has been replaced by onoo. For these instructions the n is always the second most significant digit of m.

RIGHT CIRCULAR SHIFT

32	onoo c m	Shift (rA) n digit positions to the right into rX which is also shifted to the right into rA. The sign is undisturbed. Index Register modification is not effective.	3 + n

LEFT SHIFT

37	onoo c m	Shift (rA) n digit positions to the left losing the most significant digits and bringing in zeros in the least significant digit positions on the right. The sign is undisturbed. Index Register modification is not effective.	3 + n

SKIP

00	m—	Skip to next instruction at address m.	2

* *m may not be register A, X, or L.*

EQUALITY COMPARISON

82 m c	Compare (rA) and (rL). If they are equal, transfer control to m; if they are unequal, program control passes to c.	3

MAGNITUDE COMPARISON

87 m c	Compare (rA) and (rL). If (rA) is algebraically greater than (rL), the next instruction is in m; if not, the next instruction is in C.	3

STOP

67 m c	Stop the computer. The computer stops with the stop instruction in rC, but before the search for the next instruction is started. Normally, when the computer is restarted, the first step will be to search for the next instruction specified by the c address. In this case, the m digits are ignored, and may be used as a code to indicate the reason for stopping. However, if desired, the m address may be used as an alternate restart location by depressing the m button on the control panel.	—

LOAD INDEX REGISTER

02 m c	Transfer the four digits comprising m into the specified Index Register. The same combination (see note) which indicates normal Index Register modification specifies the Index Register to be loaded.	3

INCREMENT AND UNLOAD INDEX REGISTER

07 m c	Using the address modification method, add the four digits comprising m to the contents of the specified Index Register. The sum is placed in the Index Register specified and also in the m portion of rA. The remainder of rA is cleared to zeros, and the sign of rA is set to plus.	4

NOTE: These two instructions will serve all three Index Registers. The same combination which indicates normal modification with Index Registers is used to specify the Index Register to be used. This combination of the sign bit and the 4 bit of the operation code's least significant digit has been explained under "Address Modification with Index Registers."

The m address of the 02, and of the 07, instruction does not refer to an actual storage location. If this address happens to be the same as that of an actual location, the contents of the location are not affected by the instruction.

CARD CODE TRANSLATION INSTRUCTIONS

		WORD TIME
12 — c	Translate from card code to computer code. Before the command is given, rA must contain the unprimed word and rX, the primed word of the field to be translated. After the command is executed, rA will contain the numeric and rX, the zone word in computer code. The signs are unchanged.	3
17 — c	Translate from computer code to card code. Before the command is given rA must contain the numeric, and rX, the zone word in computer code. After the command has been executed, the unprimed word of the card code is in rA and the primed word, in rX. Translation is effective for all alphanumeric character codes. The signs of rA and rX are positive.	3

XS-3 TRANSLATION INSTRUCTIONS

3/4 3 — c	Translate from UNIVAC XS-3 code to computer code. Before this command is given, rA must contain the numeric word of the data to be translated. The zone words are the same in both codes. The sign remains unchanged.	3
3/4 1 — c	Translate from computer code to UNIVAC XS-3 code. Before this command is given, rA must contain the numeric word of the data to be translated. The zone words are the same in both codes. The sign remains unchanged.	3

NOTE: Translation is effective for all 63 UNIVAC XS-3 codes. Actual translation is performed on the four numeric bits (Biquinary ⟷ XS-3). The zone bits are identical in computer and XS-3 codes.

INPUT INSTRUCTIONS (High-Speed Reader)

Figure 15 shows a functional diagram of the High-Speed Reader's transport mechanism and the high-speed magnetic drum, focusing on the relation between the read stations and the buffer area.

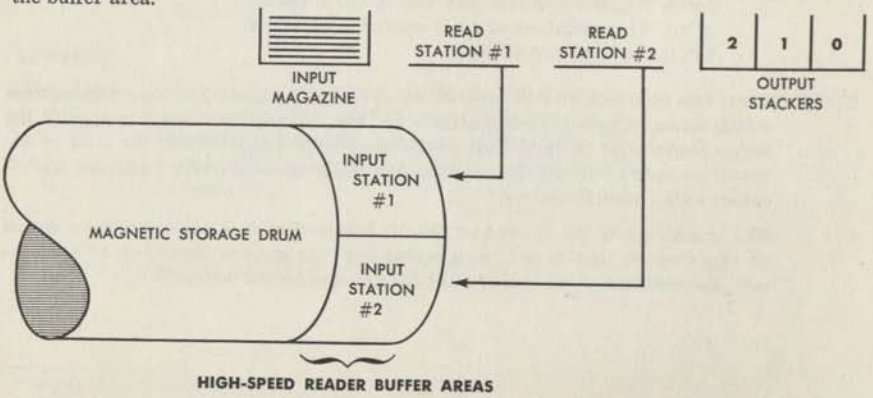


FIGURE 15. Relationship of Read Stations to Buffer

Cards are read at both stations simultaneously, automatically conveying their contents into the High-Speed Reader Buffer. The card images are not entered in sequential word positions on the buffer band, but instead are recorded in a fixed pattern called the High-Speed Reader Buffer Interlace. Five instructions direct the operation of the High-Speed Reader:

HIGH-SPEED READER CARD CYCLE

		WORD TIME
72 m c	This instruction initiates card movement in the High-Speed Reader by placing a card between the continuously revolving feed rollers. The card will be read at each station, in turn, and the data stored in the buffer band. The next instruction is at c. The computer is free to operate on other instructions during the moving and reading of cards. However, if a 72 instruction is given before the preceding 72 has begun to feed a card, the second 72 is not executed and (rC) go to rA. The next instruction is found at m.	3 — if executed 4 — if not

BUFFER TEST

42 m c	Test the High-Speed Reader Buffer. If it is loaded, (rC) go to rA. The next instruction is at m. If the buffer is not loaded, control is transferred to c and rA is not altered.	3 if c address taken, otherwise 4.

BUFFER UNLOAD

96 $\underbrace{\text{XX00}}_{\text{m}}$ c	Transfer the contents of the High-Speed Reader Buffer into the storage band according to its predetermined interlace pattern. The data is transferred untranslated. Only the two most significant digits of m (XX) designate the storage band while the two least significant digits of m are 00.	203

BUFFER UNLOAD AND TRANSLATE

96 $\underbrace{\text{XX01}}_{\text{m}}$ c	Unload the contents of the High-Speed Reader Buffer into the storage band designated by the two most significant digits of m. During the transfer, translate the data (as in the 12 instruction) to computer code. Only the two most significant digits of m (XX) denote the storage band to which the data is transferred. The two least significant digits of m must be 01.	207

NOTE: A special card image interlace pattern will be formed in storage if automatic translation is used.

STACKER SELECT

47 $\underbrace{\text{onoo}}_{\text{m}}$ c	Select the output stacker on the High-Speed Reader, (n = Stacker 0, 1, or 2). Timing: to operate on the card at the second read station, the instruc-	3

tion must be given within 120.8 milliseconds after the image is available in the buffer. If not, the card will enter the previously selected stacker. Index Register modification is not effective.

INPUT-OUTPUT INSTRUCTIONS (Read-Punch Unit)

Figure 16 depicts the functional relation between the Read-Punch Unit's transport system and the Read-Punch Buffers located on the high-speed drum.

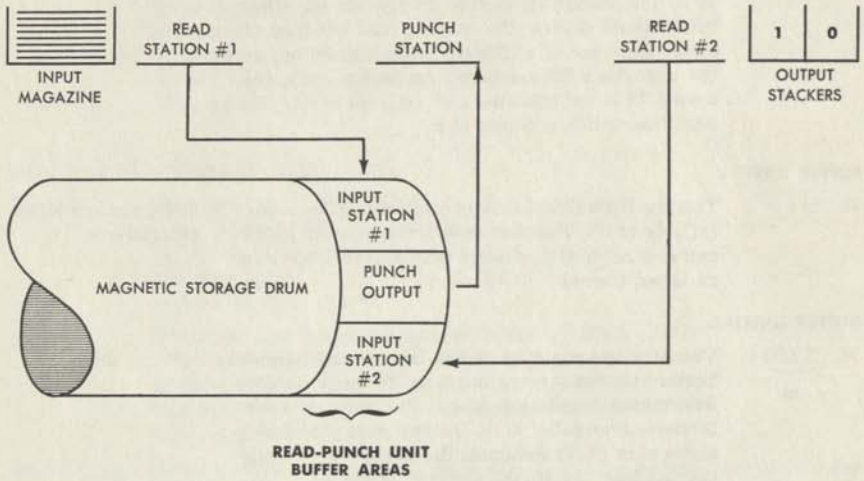


FIGURE 16. Relationship of Punch, Read Stations to Buffer

During a card cycle the card images read at the first and second read stations are simultaneously recorded on the Read-Punch Buffer. As in the High-Speed Reader, this information enters in conformance with the fixed interlace pattern of the proper buffers. Similarly, a fixed interlace pattern in the Punch Buffer will always contain the data to be punched. Six instructions direct the operation of the Read-Punch Unit:

BUFFER TEST

		WORD TIME
22 m c	Test the Read-Punch Input Buffer. If it is loaded, place (rC) in rA and the next instruction is at m. If the buffer is not loaded, control is transferred to address c where the next instruction is found. Register A is unaltered.	3 if c address taken, otherwise 4

BUFFER UNLOAD

46 XX00 c (m) — Transfer the contents of the Read-Punch Input Buffer into the storage band designated by the two most significant digits of m (XX). The two least significant digits of m are 00. The data is not translated. In storage the data is arranged according to an interlace pattern. — 203

BUFFER UNLOAD AND TRANSLATE

46 XX01 c (m) — Unload the contents of the Read-Punch Input Buffer into the storage band designated by the two most significant digits of m. During the transfer, translate the data, (as in the 12 instruction) to computer code. Only the two most significant digits of m (XX) denote the storage band to which the data is transferred, but the two least significant digits of m must be 01. — 208

NOTE: A special card image interlace pattern will be formed in storage if automatic translation is used.

CARD CYCLE — BUFFER LOAD

81 XX00 c (m) — Initiate card movement in the Read-Punch Unit and a storage-to-buffer transfer. The data is transferred unchanged. That is, the output card image (which should have been previously arranged in storage according to the interlace pattern) is transferred from the m band to the Punch Buffer. Two cards are sensed, their image being stored in the Read-Punch Input Buffer in the read interlace pattern. The Read-Punch Unit punches the data from the Punch Buffer. The unit will then advance the cards one station. The two most significant digits of the m address designate the storage band from which the data is transferred, and the two least significant digits of m are 00. — 103

CARD CYCLE — TRANSLATE

81 XX01 c (m) — Initiate card movement in the Read-Punch Unit and a storage-to-buffer transfer. Data is translated during the transfer. That is, the output card images (which should have been previously arranged in storage according to the interlace pattern) are transferred from the m band to the Punch Buffer. They are translated en route. Two cards are sensed, their image being stored in the Read-Punch Input Buffer in the read interlace pattern. The Read- — 208

Punch Unit punches the data from the Punch Buffer. All cards are then advanced one station. Only the two most significant digits of m (XX) designate the storage band from which the data is transferred, but the two least significant digits of m must be 01.

NOTE: A special card image interlace pattern will be formed in storage if automatic translation is used.

STACKER SELECT

57 — c	Select Output Stacker #1 in the Read-Punch Unit. This instruction must be given within 116 milliseconds after the Read-Punch Input Buffer is loaded if it is to operate on the card at the second read station; otherwise Stacker #0 is automatically selected. The m portion is ignored. Index Register modification is not effective.	3

OUTPUT INSTRUCTIONS (High-Speed Printer)

PRINTER TEST

27 m c	If the Printer is not busy, (rC) go to rA and control is transferred to address m. If the Printer is busy, control is transferred to c and rA remains unaltered.	3 if c address is taken, otherwise 4.

ADVANCE PAPER

16 $\underbrace{\text{oonn}}_{\text{m}}$ c	Wait until the previous Printer operation is completed. Then advance the paper in the Printer the number of lines indicated by the two least significant digits of m (nn), which can vary from 00 to 79. If the value of nn is in the fifties, sixties, or seventies a *binary* 5, 6, or 7 is used in place of biquinary. Once the paper movement is begun, the computer is free for other operations.	4

ADVANCE AND PRINT

11 $\underbrace{\text{XXnn}}_{\text{m}}$ c	Advance the paper nn lines (nn = 00 through 79) and print one line. While the paper advance is taking place, data is transferred from the storage band indicated by the two most significant digits of m (XX) to the Print Buffer. Registers A and X are used for the transfer and their previous contents are therefore destroyed. Before this instruction is given, data to be printed must be arranged	592

in the storage band (XX) according to the print interlace pattern. The computer is released for other operations as soon as the buffer band is loaded. To advance the paper 50 through 79 lines, the digits 5, 6, or 7 are coded in *binary* form and placed in the normal n position of the instruction.

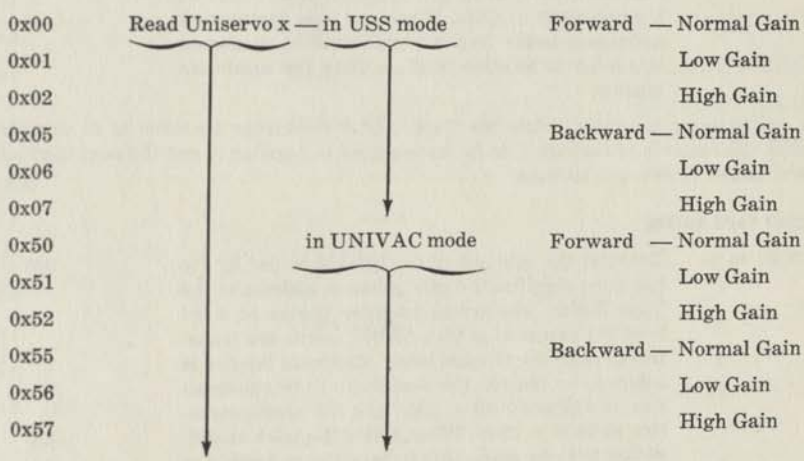
ZERO SUPPRESSION

62 — c — This instruction is used to suppress characters to the left of the most significant digit of a field. It operates on 6-bit computer code, with the numeric word in rA and the zone word in rX. Results are placed in rA and rX. Zeros (0000 0000) and commas (0011 0101) preceding the first significant digit are changed to blanks (0000 0110). — 4

INPUT-OUTPUT INSTRUCTIONS (Tape Synchronizer)

READ TAPE

*7/4 2 m c — Read one block of information from tape onto the Tape Buffer. The m portion designates the Uniservo, mode, density, direction, and gain as follow: (x indicates Uniservo number 0 through 9) — 17 (tape reversal adds 600 ms)



The last two digits of the m portion may be formed by adding the appropriate selection from the following:

0000 = USS mode	0000 = Forward	0000 = Normal Gain
0050 = UNIVAC mode	0005 = Backward	0001 = Low Gain
		0002 = High Gain

* *The Uniservo indication cannot be modified through the use of Index Registers.*

WRITE TAPE

*8/4 2	m c	Write one block of information from the Tape Buffer onto the tape. The m portion designates the Uniservo and pulse density as follows: (x indicates Uniservo number 0 through 9) 0x00 Write on Uniservo x—in USS mode —250 cpi 0x50 Write on Uniservo x—in UNIVAC mode —250 cpi 0x60 Write on Uniservo x—in UNIVAC mode —125 cpi	17

NOTE: An m address of 0x10 would cause a writing operation on Uniservo x in USS mode at 125 cpi, but this indication would not normally be used.

UNLOAD TAPE BUFFER

6/4 6	m c	Transfer the contents of the Tape Buffer to the storage band specified by the two most significant digits of the m address. The transfer of data is begun at word level 001 and ended at 000. All 200 words are transferred and arranged in the designated storage band according to a fixed interlace pattern. Minimum latency can be achieved by assigning the unload Tape Buffer instruction to location 0198 + 200n with the next instruction at location 0003 + 200n. Whenever this instruction undergoes Index Register modification, it should be placed at location 0197 + 200n for minimum latency.	205

A parity error occurring while the Tape Buffer-to-storage transfer is in progress will cause the contents of register C to be transmitted to register A and the next instruction to be obtained from c + 1 address.

LOAD TAPE BUFFER

3/4 6	m c	Transfer the contents of the band specified by the two most significant digits of the m address to the Tape Buffer. The actual transfer begins at word level 051 and ends at 050. All 200 words are transferred from the storage band. Minimum latency is achieved by placing the load Tape Buffer instruction at address 0048 + 200n and the next instruction at 0053 + 200n. When Index Register modification is to be used, this instruction is located at 0047 + 200n. If a parity error occurs during this data transfer the computer will stop.	205

BUFFER TEST

3/4 7	m c	Test the Tape Buffer to determine whether it is loaded, available, or in use. If it is loaded or available, transfer the contents of the Tape Error Flip-	3 if c address is taken, otherwise 5.

* *The Uniservo indication cannot be modified through the use of Index Registers.*

Flops into rL, and transfer (rC) into rA. The next instruction is at m. If the Tape Buffer is in use, control is transferred to c for the next instruction.

TEST UNISERVO

3/4 2 m c	If the Uniservo test indicates that a tape-handling instruction is in progress, control is transferred to c for the next instruction. Otherwise, when the Uniservos are ready for a new instruction, transfer the contents of rC into rA and proceed to m for the next instruction.	3 if c address is taken, otherwise 4.

REWIND TAPE

*6/4 2 m c	Rewind the tape to first block condition. The m portion designates the Uniservo and presence of interlock as follows: (x indicates Uniservo number 0 through 9) 0x00 Rewind Uniservo x without interlock 0x20 Rewind Uniservo x with interlock	600 ms.

SUMMARY OF INSTRUCTION CODES

ARITHMETIC:		WORD TIMES
70 m c	(m) + (rA)→ rA	5
75 m c	(rA)— (m)→ rA	5
85 m c	(rL)× (m)→ rA, rX	5+NDM+SDM
55 m c	(m) ÷ (rL)→ rA, rX	5+2NDQ+SODQ +SNCEDQ

TRANSFER:		
25 m c	(m) → rA	4
60 m c	(rA) → m	4
05 m c	(m) → rX	4
65 m c	(rX) → m	4
30 m c	(m) → rL	4
50 m c	(rL) → m	4
77 ----c	(rA) → rL	3
26 m----	0's → rA	3
31 m----	0's → rL	3
06 m----	0's → rX	3
86 m----	0's → rA, rX	14
23 m----	(rC) → rA	3

** The Uniservo indication cannot be modified through the use of Index Registers.*

		WORD TIME
TRANSLATE:		
12 ----c	90 CC : (rA), & (rX) → MC : rA, rX	3
17 ----c	MC : (rA), (rX) → CC : rA, & rX	3
3/4 3 – c	UNIVAC XS-3 (rA) → MC, rA	3
3/4 1 – c	MC (rA) → UNIVAC XS-3, rA	3
COMPARISON:		
82 $= \neq$	(rA) : (rL)	3
87 $> \leq$	(rA) : (rL)	3
EDIT:		
20 m c	Superimpose (m) on (rA) → rA	4
35 m c	Erase (m) from (rA) → rA	4
32 – n – – c	Shift → n, rA & rX	3+n
37 – n – – c	Shift ← n, rA	3+n
62 ----c	Zero suppress (rA)	4
SKIP, STOP:		
00 m----	Skip to m	2
67 ----c	Stop	Indefinite
INDEX REGISTER:		
02 m c	m → IR	3
07 m c	[m + (IR)] → IR, m of rA 0's → 0C & c of rA	4
READ-PUNCH (Input-Output):		
81 XX00 c	Θ INT → B, Sense, Punch, Move Cards	203
81 XX01 c	Θ INT Translate → B, Sense, Punch, Move Cards	208
46 XX00 c	(B) → I INT	203
46 XX01 c	(B) Translate → I INT	208
22 Yes No	Test: Buffer loaded? Yes, (rC) → rA	4, 3
57 – 1 – – c	Select Stacker #1 (Segregate)	3

		WORD TIME
HIGH-SPEED READER (Input):		
72 m c	Feed card, Sense	3
96 XX00 c	(B) → J INT	203
96 XX01 c	(B) Translate → J INT	207
42 Yes No	Test: Buffer loaded? Yes, (rC) → rA	4, 3
47 – n – – c	Select Stacker #0, 1 or 2 (Sort)	3
HIGH-SPEED PRINTER (Output):		
11 mmnn c	Advance nn Lines & Print from Band mm	592
16 – – nn c	Advance nn lines	4
27 No Yes	Test: Printer in operation? No, (rC) → rA	4, 3
TAPE SYNCHRONIZER (Input-Output):		
7/4 2 m c	1 Block Tape → Buffer	17
8/4 2 m c	1 Block Buffer → Tape	17
6/4 6 m c	(Buffer) → m	205
3/4 6 m c	(m band) → Buffer	205
3/4 7 m c	Test: Buffer loaded? Yes, Error FF → rL; (rC) → rA	4, 3
3/4 2 m c	Test: Universo busy? No, (rC) → rA, go to m	4, 3
6/4 2 m c	Rewind	600 ms

KEY:	
NDM	Number of digits in multiplier
SDM	Sum of digits in multiplier
2NDQ	Two times the number of digits in quotient
SODQ	Sum of odd digit-positions in quotient
SNCEDQ	Sum of nines complement of even digit-positions in quotient
– – – –	Ignore m or c or portion thereof
90 CC	90-Column Card Code
MC	Computer (Machine) Code
B	Buffer
INT	Interlace
OC	Operation Code

6. Programming Considerations

TAPE INSTRUCTIONS

INTERLOCK CONDITIONS FOR TAPE INSTRUCTIONS

Two major interlock conditions affect the execution of certain tape instructions. These instructions will stall after being staticized until the interlock condition is removed. Then the postponed instruction will be executed in normal fashion.

Tape Interlock

The tape interlock inhibits the execution of any tape-handling instruction (read, write, or rewind). When this interlock is in effect, the tape interlock flip-flop is in a "set" condition. Thus, the interlock is detectable in a program by a test instruction. The setting of the tape interlock is initiated by a read or write instruction during the internal execution phases. The tape interlock is released when the motion of the Uniservo has ceased and the read or write relays have been de-energized. Actually, the tape interlock is released at the expiration of a delay which allows the motion of the Uniservo to stop and the read-write relays to be de-energized.

Tape Buffer Interlock

The Tape Buffer interlock inhibits the execution of any buffer transfer instruction. This interlock condition is in effect whenever the Tape Buffer loaded-unloaded flip-flop is reset. The interlock is detectable in a program by a buffer test instruction.

The resetting of the Tape Buffer interlock is initiated by any of the following conditions:

Read instruction — while still under computer control.

Load buffer instruction — *if* preceded by a write or another load buffer instruction since the last completed write or unload buffer instruction. (Under control of buffer test extension flip-flop.)

NOTE: This load buffer instruction is *executed.*

Write instruction — while still under computer control *if* preceded by a load buffer instruction since the last completed write or unload buffer instruction.

Timed delay of 5.8 milliseconds after a write instruction.

The Tape Buffer interlock is released when the last character of a tape block is transferred out of the synchronizing register to the Tape Buffer in a reading operation, or to the magnetic tape in a writing operation.

SUMMARY OF EFFECT OF INTERLOCKS ON MAGNETIC TAPE INSTRUCTIONS

	NO INTERLOCKS	TAPE INTERLOCK ONLY	BOTH BUFFER INTERLOCK AND TAPE INTERLOCK
Read Tape	Normal Execution	Stall	Stall
Write Tape	Normal Execution	Stall	Stall
Rewind Tape	Normal Execution	Stall	Stall
Load Buffer	Normal Execution	Normal Execution	Stall
Unload Buffer	Normal Execution	Normal Execution	Stall
Test: Buffer Available	Yes Transfer to m address Error flip-flop → rL (rC) → rA	Yes Transfer to m address Error to m address → rL (rC) → rA	No Transfer to c address
Test: Input-Output Control Available	Yes Transfer to m address (rC) → rA	No Transfer to c address	No Transfer to c address

NOTE: When a magnetic tape instruction stalls on an interlock, its execution is postponed during the first execution phase, until the affecting interlock is released.

TIME OVERLAPPING PROVISIONS FOR TAPE INSTRUCTIONS

Parallel operation of certain magnetic tape functions is provided to improve performance.

Start Time/Stop Time Overlap

The start cycle of a read or write tape instruction may be initiated while the previously addressed Uniservo is coming to a stop (after the Tape Buffer interlock is reset) in the following cases:

A read following a write instruction ——
when a different Uniservo is addressed.

A write following a read instruction ——
when a different Uniservo is addressed.

Read or Write/Compute Overlap

After a read or write instruction is initiated (17 word times), internal instruction control is released to execute any other instruction (except interlocked tape instructions) during the time of reading or writing.

Rewind/Compute Overlap

Once a rewind instruction is initiated (approximately 600 milliseconds), the rewinding proceeds independently of internal instruction control, and any computer instruction can be executed with one major exception. Any tape-handling operation (read, write, or rewind) addressed to a rewinding Uniservo will not be initiated, and an error indication is made available. (Refer to the next page, "Error Conditions".) No interlocks are set and succeeding instructions proceed normally.

Load Buffer/Write Start Time Overlap

The option to overlap the start of a write operation (while tape is getting up to speed) with the loading of the Tape Buffer (with the data to be written) is provided. The main-storage-to-buffer transfer must be initiated (instruction staticized and the sentinel position at word level 049 reached) by a minimum of 6.2 milliseconds before the actual tape writing operation commences. The maximum time between the write instructions and the initiation of the main-storage-to-buffer transfer is 5.8 milliseconds.

TAPE BLOCK TIMES

	(Maximum Times in Milliseconds)							
	USS MODE				UNIVAC MODE			
	250 cpi		125 cpi		250 cpi		125 cpi	
	Read	Write	Read	Write	Read	Write	Read	Write
Start Time	12.05	12.0	18.85	18.8	12.05	12.0	18.85	18.8
Data Transfer	44.0	44.0	88.0	88.0	28.8	28.8	57.6	57.6
Stop Time	9.15	11.1	16.25	17.8	9.15	11.1	16.25	17.8
TOTAL	65.2	67.1	123.1	124.6	50.0	51.9	92.7	94.2

TAPE ERROR CONDITIONS

The error conditions arising in the magnetic tape units are handled under program control. No tape errors cause the Central Processor to stop automatically. Thus, when a tape error occurs, a control program will attempt to correct most conditions. If the control program is unable to correct the condition, an orderly halt, with all necessary consideration given to other input-output requirements (previously committed cards), will occur.

Existing error conditions on each tape-handling instruction are made available to program detection by executing a Tape Buffer test. At the time the buffer test passes (the buffer interlock is reset), the contents of the tape error flip-flops which have been set during the previous tape-handling instruction are transferred to register L.

Positioning of Error Indications in Register L

The following error conditions will place an indication in the most significant bit position (digit value 5) of the specified digit positions.

Sign Digit — Not used.

Least Significant Digit — FIR-BIR Check (FIBI)
Digit Position 10
Forward Interlock Released
Backward Interlock Released

When a tape-handling instruction (read, write, and rewind) is in the first instruction phase while the synchronizing and control circuitry is free (tape interlock is reset), and if no FIR-BIR signal is returned after a sufficient period of time (FIR-BIR), any of the following conditions is indicated:

Power off the selected Uniservo.
Uniservo not logically connected.
Uniservo plugboard malfunctioning.

Blown fuse in Uniservo.

Maintenance interlock on selected Uniservo.

Uniservo in process of rewinding.

Uniservo rewound with interlock.

Read or write thyratron already fired (read or write instruction).

Digit Position 9 — Not used.

Digit Position 8 — Control Check

Ensures that the proper read-write instruction is being executed, and indicates at least one of the following conditions:

Case 1: When a write instruction has been initiated and no Uniservo is in the write forward condition.

Case 2: When a write instruction has been initiated and no Uniservo is in the write condition with the clutch energized. (Protective ring in the selected reel.)

Case 3: When a read forward instruction has been initiated and no Uniservo is in the read forward condition.

Case 4: When a read backward instuction has been initiated and no Uniservo is in the read backward condition.

The tapes may move in the wrong direction. It is unlikely, however, that they will move at all.

Digit Position 7 — Information Transfer Check

This indication is set if the following conditions occur:

Synchronizer Register Overflow — when information is read from tape into the Synchronizer faster than it can be written on the buffer.

Synchronizer Register Underflow — when an attempt is made to write information on tape faster than it is supplied from the buffer.

Digit Position 6 — Tape Check

The normal UNIVAC tape check circuitry will provide this recognition of irregular pulses in the space between blocks.

Digit Position 5 — Input-Output Parity Check

In addition to the normal odd parity checking, a special check is made against all "1's" (1 11 1111) in the UNIVAC mode of recording.

Digit Position 4 — Less than 720 (1100) Check

This indication is given of less than a full block recording.

In UNIVAC mode — indicates 709 — 719 characters.

In USS mode — Forward — indicates 1087 — 1099 characters.
Backward — indicates 1088 — 1099 characters.

Digit Position 3 — Greater than 720 (1100) Check

This indication is given if more than a normal block is read (721 - 739 or 1101 - 1120 characters). If this is the only character-count error present, the error involves a single block with too many characters.

Digit Position 2 — Greater than 739 (1121) Check

This indication is given of more than a single block (740+ or 1122+ characters) recording — possibly two blocks. When this error is indicated, the >720 check is also turned on.

Digit Position 1 — Master Error Flip-Flop

If *any* recognizable error condition is present, this master indication is given, in the most significant digit position. The digit code produced is ¾ (0111).

Special Error Indication in Register L

The following error check will also place an indication into register L in the next to the most significant bit position (digit value 4) of digit position 2, if a buffer test instruction follows an erroneous buffer to main storage transfer.

Buffer to Main Storage Transfer Check

When a parity error occurs during a buffer to main storage transfer, this indicating flip-flop is set, controlling the acquisition of the next instruction from c + 1 address.

Timing of Error Indications

At the initiation of each new tape-handling instruction (read, write or rewind), all of the error flip-flops are reset. The General Clear button on the console will also clear the error flip-flops. During the first internal execution phase of the tape-handling instructions, the FIR-BIR Check (FIBI) is made. When an FIR-BIR error occurs, the FIBI flip-flop is set and the *instruction is not executed.* Control passes to the next instruction, and effectively, the erroneous tape-handling instruction is a skip. No interlocks are set.

After a tape-handling instruction is released from internal instruction control and is proceeding independently (with the proper interlocks set), the Control Check, Tape Check, Parity Check, and Character-Count Checks (< 720, > 720 > 739) are made and the appropriate error flip-flops are set. Should a Control Check error occur during a read instruction, the synchronizing circuitry waits for the characters to arrive from tape, but the tape does not move. Therefore, the tape interlock and tape buffer interlock are *never* reset, and the buffer test cannot pass.

INDEX REGISTERS

In the UNIVAC Solid-State System each Index Register has the capacity to hold four digits. Consequently, there is no restriction on the manner in which the operand address can be modified: for every possible modification there is a value that can be stored in an Index Register to effect the modification.

There are instructions to store initial values in the Index Registers and instructions to augment the contents of an Index Register by any increment desired. Thus, complete flexibility in the use of these registers is provided. The instruction that increments the con-

tents of an Index Register also delivers the result of the incrementation to register A, where it is readily accessible for testing. Consequently the Index Registers provide easy control for looping. Moreover the instruction always remains in its original form in main storage, even though in execution it may be modified by the contents of an Index Register. Therefore, an instruction can be called on again and again without the programmer's having to be concerned with whether or not it has been modified.

APPLICATION OF INDEX REGISTERS

The basic purpose of Index Registers is to make address modification a hardware, rather than a program, function. The result of this feature is, in effect, an expansion of main storage, since address modification, a significant characteristic of most programs, can be achieved with considerably fewer program steps.

Then too, the use of Index Registers often significantly decreases program running time. One example, a common operation in UNIVAC Solid-State routines, is the editing of alphanumeric information. The basic characteristic of this operation is processing the primed word of the information in exactly the same way as the unprimed word. If all instructions in editing routines that call on the data for operands specify an Index Register, the same instructions which are used to process the unprimed word can also be used to process the primed word at a negligible expenditure of time. This approach represents a 50 per cent saving in space for all such operations in a program.

MINIMUM LATENCY PROGRAMMING

In programming the UNIVAC Solid-State 90 Magnetic Tape System, the user need not concern himself with tedious timing considerations, since interlock and the various buffer tests prevent timing errors in coordinating operations of all the units. Moreover, the interlace patterns for tape and card images allow him to work on successive fields in a single drum revolution. To take complete advantage of the system's speed, however, the programmer will recognize that certain elementary timing factors should be included in a "tight" program. He will, for example, be aware that he can minimize the time needed to secure data from its storage locations. In computer terminology, he would want to "code in minimum latency."

Two features of the UNIVAC Solid-State 90 Magnetic Tape System enable the programmer to achieve minimum latency. To begin with, the one and one-half address instruction code specifies the address of both the operand and of the next instruction. The programmer can consequently arrange instructions in a pattern which effectively minimizes the time it takes to locate them for execution. Second, the 1,000 words of high-speed access storage reduce the maximum selection time of data stored there to only .85 milliseconds.

MINIMUM LATENCY RULES

Minimum latency, therefore, can be accomplished by means of the following simple rules:

THE FIRST RULE: For instructions having an m address . . .
The location of an instruction requiring an operand is m — 2. The address of the next instruction, c, is determined by adding, to the location of the m portion of the current instruction, only the time required for the third and fourth phases of the instruction cycle. Thus, the c address of an add instruction, for example, would be m + 3.

A brief example will illustrate the first rule. There is a data word in storage location 0020.

thus m = 0020

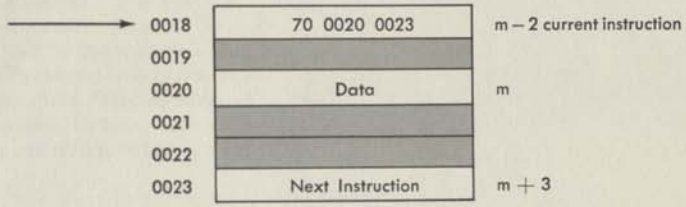
and m − 2=0018

Pursuing the first rule further, assume that the instruction in storage location 0018 is an add (70), in which the third and fourth phases consume 3 word times in minimum latency. According to the first rule, the address of the next instruction is fixed by adding 3 to m of the current instruction.

thus, since m = 0020

0020+3 = 0023, the location of the next instruction

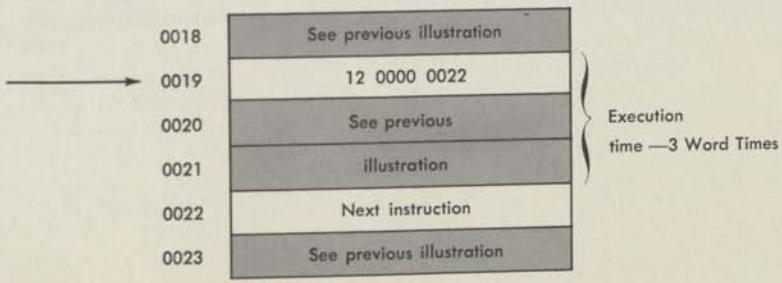
Consequently, to take advantage of minimum latency coding, an add instruction the m address of which is 0020 must be placed in 0018, while the next instruction is in 0023. A graphic presentation of the first rule appears below.



Normally, the shaded storage locations are also occupied with either data or instructions which are omitted here to emphasize the first rule of latency. The m and c portions of this instruction may be located in any other band at the same level.

The location of an instruction in which the m address is ignored is not computed with reference to the m address. Frequently, the address of such an instruction will have been determined by the fact that it was the c address of a previous instruction. Occasionally, the instruction may be interspersed with others, because its location happens to be one of those bypassed by the cycle of a previous instruction, such as those shaded areas in the foregoing illustration (0019, 0021, 0022).

THE SECOND RULE: For instructions which do not have an m address . . .
The c address of the instruction in which the m address is ignored is consequently governed by the location of the instruction itself. By adding to this address the number of word times required for the entire execution of the instruction, the location of the next instruction is determined. For example, if a translation instruction (12) is in location 0019, its c address should be 0022, because the entire execution takes three word times. Graphically this would appear as:



Certain instructions, such as the 11, 46, 96, and 81 should be placed in specific locations and should contain specific c addresses. These locations can be learned from the Minimum Latency Table, which also aids in using Rules 1 and 2.

GENERAL RULE: Instructions and data whose location in a standard access band would cause more than fifty word times to elapse before access to them is gained should be placed in a high-speed access band. Naturally, any of the addresses computed according to Rules 1 and 2 can be used on the high-speed access, as well as on the standard access bands. In using the high-speed access bands, the computed address can be added to 4000, 4200, 4400, 4600, and 4800. In addition, the address can be added to 4050, 4250, . . . 4850; 4100, 4300, . . . 4900; 4150, 4350, . . . 4950. These additional locations may be used because the high-speed access bands are serviced by four read-write heads which equalize the access time to the above addresses.

7. Installation

SPACE. The UNIVAC Solid-State 90 Magnetic Tape System requires only 750 square feet of floor space

AIR CONDITIONING. The UNIVAC Solid-State 90 Magnetic Tape System is primarily an air-cooled system. Fans or blowers built into the equipment take care of what little heat is generated by the motors and solid-state circuits. A small air conditioning system is built into the Processor to cool the drum. The number and type of components comprising any particular Solid-State System will affect the amount and rate of heat emitted. This and other variable factors, such as location and size of the room, will determine how much (if any) air conditioning is required.

POWER REQUIREMENTS. Power requirements can be met in most cases by the existing electrical outlets found in most office buildings. The system operates on conventional 220-volt single-phase lines. Power rating is 46.5 kva (with ten Uniservos). Where the user does not require the in-line High-Speed Printer, the power requirements will drop to 41.7 kva.

CONSTRUCTION. The entire system weighs slightly over 16,425 lb (with ten Uniservos). In most cases, architectural or structural changes (primarily shoring up the floor under the computer) are not required.

PERFORMANCE. Tests consisting of a series of diagnostic routines are conducted at the plant prior to shipment by the manufacturer. The system is shipped to the user only after the results of these tests meet with his approval. At the installation site, the equipment is checked out with a series of rigorous systems and services tests by Remington Rand engineers. Final customer acceptance is predicated upon the successful completion of these tests.

8. Specialized Applications

Low operating costs, high speeds, large storage capacity, and programming flexibility make the UNIVAC Solid-State 90 Magnetic Tape System an ideal solution to problems which heretofore created too much expense for many computer users.

ONE-TIME JOBS. Because of the programming, debugging, and computer expenses involved in conventional types of computers, management was often reluctant to request special reports. With the UNIVAC Solid-State 90 Magnetic Tape System, costs can be reduced to a point where the production of these reports is now economically feasible.

SMALL-VOLUME JOBS. For the same reasons as stated above, this was another processing area which previously proved to be exceedingly expensive. Today, however, the low operating costs of the system permit these jobs to be done at realistic cost levels. In many cases, because of the system's large storage capacity, many of these jobs can be combined with other applications and processed at practically no expense.

TABLE LOOK-UP OPERATIONS. One of the more costly types of computer operations is the Table Look-up. It is used within a given computer run primarily to distribute various types of information such as schedules, rate computations, or sales-analysis distributions. In conventional computers, tables require tremendous amounts of storage and consume large chunks of expensive computer time. With the 50,000-digit main storage and fast access time of the UNIVAC Solid-State 90 Magnetic Tape System, this type of operation is now relatively inexpensive.

STATISTICAL JOBS. The bit-manipulation feature of the UNIVAC Solid-State 90 Magnetic Tape System makes it an ideal solution for statistical jobs. For these operations, the card capacity can be increased by using specialized, rather than computer, codes. For example, each punching position in a card can be a yes or no answer to a specific question.

ENGINEERING, SCIENTIFIC APPLICATIONS. This is another good application area for the UNIVAC Solid-State 90 Magnetic Tape System. Heretofore, these applications were limited by storage capacity and arithmetic speed or by the tremendous costs for coding the programs.

MINIMUM LATENCY TABLE

Operation Code	I (Location of Instruction Word)	D (Location of Data – Operand)	C (Location of Next Instruction)
05 25 30	m – 2	m	m + 2
50 60 65	m – 2	m	m + 2
20 35	m – 2	m	m + 2
70 75	m – 2	m	m + 3
06 26 31 77	I		I + 3
82 87 02	I		I + 3
12 17 3/4 3 3/4 1	I		I + 3
57 47 72	I		I + 3
16 62 07	I		I + 4
32 37	I		I + 3 + n
3/4 2 22 27 42	I		I + 3 (c) ; I + 4 (m)
86	I	I + 14 = (NI)	
23	I	I + 3 = (NI)	
8/4 2 7/4 2	I		I + 17
85	m – 2	m	m + (3 + NDM + SDM)*
55	m – 2	m	m+(3+2NDQ+SODQ+SNCEDQ)*
11	Level 197		Level 189
81 (Untranslated)	Level 198		Level 001
96 (Untranslated)	Level 198		Level 001
46 (Untranslated)	Level 198		Level 001
96 (Translated)	Level 198		Level 005
81 (Translated)	Level 098		Level 106
46 (Translated)	Level 198		Level 005
3/4 6	048 + 200n		053 + 200n
	047 + 200n when	IR modification is indicated	
6/4 6	198 + 200n		003 + 200n
	197 + 200n when	IR modification is indicated	
3/4 7	I		I + 3 (c) – I + 5 (m)

KEY*

NDM = Number of digits in multiplier	**SDM** = Sum of digits in multiplier	**2NDQ** = Two times the number of digits in quotient	**SODQ** = Sum of odd digit-positions in quotient	**SNCEDQ** = Sum of nines complement of even digit-positions in quotient

TRANSLATION TABLE

Remington Rand	90-Column Code ⟷ Computer Code ⟷ UNIVAC XS-3 Code							
Punching Character	rX (Primed) XX97	rA (Unprimed) 5310	rX (Zone)	rA (Numeric)	Printing Character	(Zone)	(Numeric)	Character
0	0000	0001	0000	0000	0	0000	0011	0
1	0000	0010	0000	0001	1	0000	0100	1
2	0010	0010	0000	0010	2	0000	0101	2
3	0000	0100	0000	0011	3	0000	0110	3
4	0010	0100	0000	0100	4	0000	0111	4
5	0000	1000	0000	1000	5	0000	1000	5
6	0010	1000	0000	1001	6	0000	1001	6
7	0001	0000	0000	1010	7	0000	1010	7
8	0011	0000	0000	1011	8	0000	1011	8
9	0010	0000	0000	1100	9	0000	1100	9
A	0010	1010	0001	0001	A	0001	0100	A
B	0000	1010	0001	0010	B	0001	0101	B
C	0001	0001	0001	0011	C	0001	0110	C
D	0000	1101	0001	0100	D	0001	0111	D
E	0000	0101	0001	1000	E	0001	1000	E
F	0011	0010	0001	1001	F	0001	1001	F
G	0001	1000	0001	1010	G	0001	1010	G
H	0001	0100	0001	1011	H	0001	1011	H
I	0000	1100	0001	1100	I	0001	1100	I
J	0000	1110	0010	0001	J	0010	0100	J
K	0010	1100	0010	0010	K	0010	0101	K
L	0010	0001	0010	0011	L	0010	0110	L
M	0000	1001	0010	0100	M	0010	0111	M
N	0010	1001	0010	1000	N	0010	1000	N
O	0000	0110	0010	1001	O	0010	1001	O
P	0001	0110	0010	1010	P	0010	1010	P
Q	0001	1100	0010	1011	Q	0010	1011	Q
R	0001	0010	0010	1100	R	0010	1100	R
S	0001	1010	0011	0010	S	0011	0101	S
T	0011	0100	0011	0011	T	0011	0110	T
U	0001	1001	0011	0100	U	0011	0111	U
V	0010	0101	0011	1000	V	0011	1000	V
W	0001	0101	0011	1001	W	0011	1001	W
X	0011	0001	0011	1010	X	0011	1010	X
Y	0010	0110	0011	1011	Y	0011	1011	Y
Z	0011	1000	0011	1100	Z	0011	1100	Z
#	0001	1011	0001	1111	#	0010	0011	)
.	0010	1110	0001	0101	.	0001	0010	.
$	0010	1111	0010	0101	$	0010	0010	! (N.P.)
,	0010	1101	0011	0101	, Comma	0011	0010	:
Blank	0000	0000	0000	0110	Space (N.P.)	0000	0001	Space
+	0011	1010	0011	0000	+	0011	0011	+
:	0011	0110	0001	0110	:	0001	0001	,
*	0000	0011	0010	0110	*	0010	0001	" (N.P.)
%	0000	1011	0011	0110	%	0011	0001	Breakpoint
&	0001	1111	0001	0111	&	0001	0011	:
	0001	1101	0000	0101	—	0000	0010	—
/	0011	1100	0011	0001	/	0011	0100	/
)	0001	1110	0000	0111	)	0000	0000	Not used
'	0011	0111	0000	1111	' Apostrophe	0000	1101	' Apostrophe
;	0011	1110	0000	1110	;	0000	1110	@
(	0011	1001	0000	1101	(	0000	1111	(

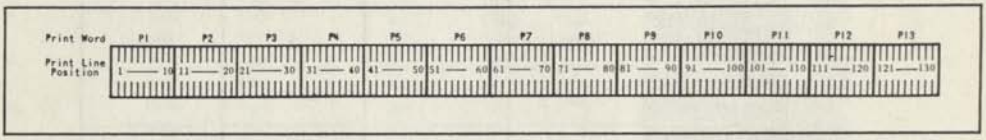
Note: N.P. refers to non-printing characters.

PRINT CHARACTER TABLE

NUMERIC	ZONE 00	ZONE 01	ZONE 10	ZONE 11
0111	)	&		
0110	Space	:	*	%
0101	— (Minus)	.	$	, (Comma)
0000	0			+
0001	1	A	J	/
0010	2	B	K	S
0011	3	C	L	T
0100	4	D	M	U
1000	5	E	N	V
1001	6	F	O	W
1010	7	G	P	X
1011	8	H	Q	Y
1100	9	I	R	Z
1111	' (Apostrophe)	#		
1110	;			
1101	(			

KEY TO PRINT INTERLACE TABLE

The 130 characters that can be printed on one line are divided into 13 10-digit print words. These words, and their corresponding print positions, are shown in the diagram. Before a print instruction is executed, the 13 print words are accumulated by program instructions on a specific main storage band in fixed word locations of the print interlace pattern.



To locate the interlace factor, the base of the symbol is P. The first subscript indicates the print line position, 1 through 13 (see diagram). The absence of an apostrophe refers to the unprimed or numeric word of a word pair in computer code. An apostrophe denotes the primed or zone word.

With this symbol, the corresponding interlace factor can be added to the m band of the print instruction to determine the placement of data to be printed.

INTERLACE TABLE
High-Speed Printer Interlace

LOCATION 00XX		LOCATION 01XX	
00 P1	50 P4	00	50
01	51	01	51
02	52	02	52
03	53	03 P7	53
04	54	04	54
05 P'1	55 P'4	05	55
06	56	06	56
07	57	07	57
08	58	08 P'7	58
09 P10	59	09	59
10	60	10	60
11	61	11	61
12	62 P13	12	62
13	63	13	63
14 P'10	64	14	64
15	65	15	65 P3
16	66	16	66
17	67 P'13	17	67
18 P6	68	18	68
19	69	19	69
20	70	20	70 P'3
21	71	21	71
22	72	22	72
23 P'6	73	23	73
24	74	24	74
25	75	25 P9	75
26	76	26	76
27	77	27	77
28	78	28	78 P12
29	79	29	79
30	80	30 P'9	80
31	81 P2	31	81
32	82	32	82
33	83	33	83 P'12
34	84	34 P5	84
35	85	35	85
36	86 P'2	36	86
37	87	37	87
38	88	38	88
39	89	39 P'5	89
40	90	40	90
41 P8	91	41	91
42	92	42	92
43	93	43	93
44	94 P11	44	94
45	95	45	95
46 P'8	96	46	96
47	97	47	97
48	98	48	98
49	99 P'11	49	99

KEY TO TAPE INTERLACE TABLE

A block of data read from or written on tape in the UNIVAC mode contains 72 pairs of words. Each word pair is composed of an unprimed and a primed word. A block in USS mode consists of 100 word pairs, each having a numeric and a zone word.

To locate the interlace factor for a word in any mode, a symbol with the base T is constructed. The subscript refers to the position of the word in the block, 1 through 72 in UNIVAC mode, and 1 through 100 in USS mode. The absence of an apostrophe indicates the unprimed or numeric portion. An apostrophe refers to the primed or zone portion.

With this symbol, the interlace factor for each word in a block may be found. Adding this factor to the m band specified in a read tape instruction provides the storage location of the data from a particular word of the tape block. The placement of output data which is to appear in a specific word in the tape block is also determined by adding the interlace factor to the m band of the write tape instruction.

NOTE: In a read backward operation, the format of the tape block is changed. Digits within a word are assembled in correct sequence. Word pairs, however, are assembled in the normal interlace in reverse sequence. That is, the first word read (actually the last word of the tape block) is stored in the locations for the first word pair. The second tape word read is stored in the interlace positions for the second word pair. This sequence continues until the last word read (actually the first word of the tape block) is placed in the positions for the last word pair.

INTERLACE TABLE
Tape Synchronizer Interlace

LOCATION				LOCATION			
Start	X000	94′	X050 19′	X100	44′	X150	69′
	01	1	51 26′	01	51	51	76
	02	63′	52 88′	02	13′	52	38′
	03	70	53 95	03	20	53	45
	04	32′	54 57	04	82′	54	7′
	05	39	55 64	05	89	55	14
	06	1′	56 26′	06	51′	56	76′
	07	8	57 33	07	58	57	83
	08	70′	58 95′	08	20′	58	45′
	09	77	59 2	09	27	59	52
	10	39′	60 64′	10	89′	60	14′
	11	46	61 71	11	96	61	21
	12	8′	62 33′	12	58′	62	83′
	13	15	63 40	13	65	63	90
	14	77′	64 2′	14	27′	64	52′
	15	84	65 9	15	34	65	59
	16	46′	66 71′	16	96′	66	21′
	17	53	67 78	17	3	67	28
	18	15′	68 40′	18	65′	68	90′
	19	22	69 47	19	72	69	97
	20	84′	70 9′	20	34′	70	59′
	21	91	71 16	21	41	71	66
	22	53′	72 78′	22	3′	72	28′
	23	60	73 85	23	10	73	35
	24	22′	74 47′	24	72′ — UNIVAC	74	97′
	25	29	75 54	25	79 End	75	4
	26	91′	76 16′	26	41′	76	66′
	27	98	77 23	27	48	77	73
	28	60′	78 85′	28	10′	78	35′
	29	67	79 92	29	17	79	42
	30	29′	80 54′	30	79′	80	4′
	31	36	81 61	31	86	81	11
	32	98′	82 23′	32	48′	82	73′
	33	5	83 30	33	55	83	80
	34	67′	84 92′	34	17′	84	42′
	35	74	85 99	35	24	85	49
	36	36′	86 61′	36	86′	86	11′
	37	43	87 68	37	93	87	18
	38	5′	88 30′	38	55′	88	80′
	39	12	89 37	39	62	89	87
	40	74′	90 99′	40	24′	90	49′
	41	81	91 6	41	31	91	56
	42	43′	92 68′	42	93′	92	18′
	43	50	93 75	43	100	93	25
	44	12′	94 37′	44	62′	94	87′
	45	19	95 44	45	69	95	94
	46	81′	96 6′	46	31′	96	56′
	47	88	97 13	47	38	97	63
	48	50′	98 75′	48	100′ — USS	98	25′
	49	57	99 82	49	7 End	99	32

KEY TO CARD INTERLACE TABLE

The 90-column punched card is represented in the computer as 20 words. Each group of ten columns forms a data word of two images called the unprimed and primed images. Each image is a computer word and is an exact representation of the holes appearing on a particular section of the card — a punch equals a "1" bit. The signs of all images are positive.

Row	Columns 1-10	11-20	21-30	31-40	41-45
0 1 3 5	0	1	2	3	4
7 9	0′	1′	2′	3′	4′
0 1 3 5	5	6	7	8	9
7 9	5′	6′	7′	8′	9′
	Columns 46-55	56-65	66-75	76-85	86-90

Any combination of punches may be represented within the computer; however translations instructions are provided only for the standard Remington Rand code. To locate the interlace factor the base of the symbol is:

I = input on the Read-Punch Unit

J = input on the High-Speed Reader

O = output on the Read-Punch Unit

The first subscript added to this base indicates the station; e.g. J_2 refers to input of the second read station of the High-Speed Reader. The second subscript refers to the column group on the card (see above).

The absence of an apostrophe refers to the unprimed word. An apostrophe indicates the primed word; e.g. O'_{12} refers to the primed word of card-column group #2 which is output on the first and only punch station of the Read-Punch Unit.

With a symbol such as this, the corresponding interlace factor can be added to the m band of the input or output instruction to determine the exact location of the card group within the computer.

To locate data which is automatically translated to computer code as it leaves the buffer, a similar procedure is followed. A symbol is constructed with a base and subscripts as indicated above. With translated data, however, the absence of an apostrophe indicates the numeric word, and the apostrophe, the zone word. The interlace factor can then be found in the columns of the interlace table which are headed "Translated."

INTERLACE TABLE
Read-Punch Unit Interlace

UNTRANSLATED				TRANSLATED			
Storage Location 00XX		Storage Location 01XX		Storage Location 00XX		Storage Location 01XX	
00	50	00	50	00	50	00	50
01	51	01 O10	51 O17	01	51	01 I10	51 I22
02	52	02	52	02 I15	52 I27	02	52
03 I'29	53 I'12	03	53	03	53	03 O'19	53 O'12
04	54	04 I'24	54 I'17	04	54	04	54
05	55	05	55	05	55	05	55
06	56	06 O'10	56 O'17	06	56	06 I'10	56 I'22
07	57	07	57	07 I'15	57 I'27	07	57
08 I10	58 I22	08	58	08	58	08 O10	58 O17
09	59	09 I15	59 I27	09	59	09	59
10	60	10	60	10	60	10	60
11	61	11 O15	61 O13	11	61	11 I20	61 I13
12	62	12	62	12 I25	62 I18	12	62
13 I'10	63 I'22	13	63	13	63	13 O'10	63 O'17
14	64	14 I'15	64 I'27	14	64	14	64
15	65	15	65	15	65	15	65
16	66	16 O'15	66 O'13	16	66	16 I'20	66 I'13
17	67	17	67	17 I'25	67 I'18	17	67
18 I20	68 I13	18	68	18	68	18 O15	68 O13
19	69	19 I25	69 I18	19	69	19	69
20	70	20	70	20	70	20	70
21	71	21 O11	71 O18	21	71	21 I11	71 I23
22	72	22	72	22 I16	72 I28	22	72
23 I'20	73 I'13	23	73	23	73	23 O'15	73 O'13
24	74	24 I'25	74 I'18	24	74	24	74
25	75	25	75	25	75	25	75
26	76	26 O'11	76 O'18	26	76	26 I'11	76 I'23
27	77	27	77	27 I'16	77 I'28	27	77
28 I11	78 I23	28	78	28	78	28 O11	78 O18
29	79	29 I16	79 I28	29	79	29	79
30	80	30	80	30	80	30	80
31	81	31 O16	81 O14	31	81	31 I21	81 I14
32	82	32	82	32 I26	82 I19	32	82
33 I'11	83 I'23	33	83	33	83	33 O'11	83 O'18
34	84	34 I'16	84 I'28	34	84	34	84
35	85	35	85	35	85	35	85
36	86	36 O'16	86 O'14	36	86	36 I'21	86 I'14
37	87	37	87	37 I'26	87 I'19	37	87
38 I21	88 I14	38	88	38	88	38 O16	88 O14
39	89	39 I26	89 I19	39	89	39	89
40	90	40	90	40	90	40	90
41	91	41 O12	91 O19	41	91	41 I12	91 I24
42	92	42	92	42 I17	92 I29	42	92
43 I'21	93 I'14	43	93	43	93	43 O'16	93 O'14
44	94	44 I'26	94 I'19	44	94	44	94
45	95	45	95	45	95	45	95
46	96	46 O'12	96 O'19	46	96	46 I'12	96 I'24
47	97	47	97	47 I'17	97 I'29	47	97
48 I12	98 I24	48	98	48	98	48 O12	98 O19
49	99	49 I17	99 I29	49	99	49	99

INTERLACE TABLE
High-Speed Reader Interlace

UNTRANSLATED				TRANSLATED			
Storage Location 00XX		Storage Location 01XX		Storage Location 00XX		Storage Location 01XX	
00	50	00	50	00	50	00	50
01 J10	51 J22	01	51	01	51	01	51
02	52	02 J15	52 J27	02	52	02	52
03	53	03	53	03 J'29	53 J'12	03	53
04	54	04	54	04	54	04 J'24	54 J'17
05	55	05	55	05	55	05	55
06 J'10	56 J'22	06	56	06	56	06	56
07	57	07 J'15	57 J'27	07	57	07	57
08	58	08	58	08 J10	58 J22	08	58
09	59	09	59	09	59	09 J15	59 J27
10	60	10	60	10	60	10	60
11 J20	61 J13	11	61	11	61	11	61
12	62	12 J25	62 J18	12	62	12	62
13	63	13	63	13 J'10	63 J'22	13	63
14	64	14	64	14	64	14 J'15	64 J'27
15	65	15	65	15	65	15	65
16 J'20	66 J'13	16	66	16	66	16	66
17	67	17 J'25	67 J18	17	67	17	67
18	68	18	68	18 J20	68 J13	18	68
19	69	19	69	19	69	19 J25	69 J18
20	70	20	70	20	70	20	70
21 J11	71 J23	21	71	21	71	21	71
22	72	22 J16	72 J28	22	72	22	72
23	73	23	73	23 J'20	73 J'13	23	73
24	74	24	74	24	74	24 J'25	74 J'18
25	75	25	75	25	75	25	75
26 J'11	76 J'23	26	76	26	76	26	76
27	77	27 J'16	77 J'28	27	77	27	77
28	78	28	78	28 J11	78 J23	28	78
29	79	29	79	29	79	29 J16	79 J28
30	80	30	80	30	80	30	80
31 J21	81 J14	31	81	31	81	31	81
32	82	32 J26	82 J19	32	82	32	82
33	83	33	83	33 J'11	83 J'23	33	83
34	84	34	84	34	84	34 J'16	84 J'28
35	85	35	85	35	85	35	85
36 J'21	86 J'14	36	86	36	86	36	86
37	87	37 J'26	87 J'19	37	87	37	87
38	88	38	88	38 J21	88 J14	38	88
39	89	39	89	39	89	39 J26	89 J19
40	90	40	90	40	90	40	90
41 J12	91 J24	41	91	41	91	41	91
42	92	42 J17	92 J29	42	92	42	92
43	93	43	93	43 J'21	93 J'14	43	93
44	94	44	94	44	94	44 J'26	94 J'19
45	95	45	95	45	95	45	95
46 J'12	96 J'24	46	96	46	96	46	96
47	97	47 J'17	97 J'29	47	97	47	97
48	98	48	98	48 J12	98 J24	48	98
49	99	49	99	49	99	49 J17	99 J29

SPECIFICATIONS

Physical Dimensions

UNIT	Dimensions (doors closed) LENGTH	WIDTH	HEIGHT	WEIGHT lb	WEIGHT lb/ft²
Central Processor	108″	32″	69″	3532	146.8
High-Speed Reader	51″	27″	49″	758	91.8
Read-Punch Unit	49″	27″	54″	1334	134
High-Speed Printer	72″	32″	51″	1613	101.4
Tape Synchronizer	108″	32″	69″	3300	137.7
Uniservo II	31″	30½″	69″	745	115.3
	Space Requirements (doors open)				
Central Processor	136″	118″	69″		
High-Speed Reader	51″	72″	49″		
Read-Punch Unit	75″	74″	79″		
High-Speed Printer	128″	68″	51″		
Tape Synchronizer	136″	118″	69″		
Uniservo II	31″	74″	69″		

Power Requirements

Frequency: 60 cycle ± 0.5% maximum deviation.
Voltage: 230-volt, single-phase, 3-wire with grounded neutral (115 v each line to ground).

	RATING	SERVICE LINE FUSE SIZE
Central Processor, High-Speed Reader — Read-Punch Unit	9.8 kva	70 amp
High-Speed Printer	4.7 kva	
*Tape Synchronizer	6.0 kva	175* amp
Uniservo II	2.6 kva each	

*Estimate handling 10 Uniservos

Remington Rand Univac
DIVISION OF SPERRY RAND CORPORATION

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