INTEROFFICE MEMORANDUM

TO: Multiprocessor Committee
Lorrin Gale
Gordon Bell

DATE: October 18, 1973

FROM: Stu Wecker

DEPT: Research and Development

EXT: 4366 LOC: 3-4

SUBJ: Multiprocessor Committee Meeting vol 11

The multiprocessor committee held its first meeting on Friday, October 12, to discuss the issues involved in multi-processor PDP-11 systems. The topics discussed were:

1. Do we want closely-coupled multi-processor systems?
2. Are they more reliable?
3. Is it cheaper to build a single faster processor?
4. What speed range should our product-line span?
5. How do we put multiple processors on a single Unibus?
6. How could RSX-11D use multi-processors?

For the loosely-coupled case we decided that no special hardware was needed and the issues were simply software network issues. For some applications closely-coupled systems seemed necessary where tasks were closely related sharing a common data base. Multiple processor systems didn't seem inherently more reliable then single processor ones especially if all of them were needed to perform a given task. Some people felt it was both cheaper and easier to simply build a faster -11 for increased computing power. The incremental throughput increases by adding 1 or 2 additional processors didn't give us any greater span of power then we have now from the 05 to 45. Bill Strecker had a proposal to put many processors on a single Unibus by using local caches to each processor to reduce total bus traffic. He has a scheme to solve the "stale data" problem. Craig Mudge and Dave Cutler wanted a multi-processor system to increase the available computing cycles for user tasks in RSX-11D. Tneir proposal is for an I/O processor to handle all I/O devices and the file system. All slow devices would be handled by the I/O processor and the data transferred through a DR-11B type interface. High speed mass storage devices would be connected via multi-port controllers to both processors so that transfers could be done directly into user address space on the main processor memory. It was felt that no more discussions were needed until some of the other architectural issues were nailed down; i.e., integrated controllers, caches, virtual addressing, etc.

SW:cw

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DIGITAL INTEROFFICE MEMORANDUM

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Lorrin Gale
Gordon Bell

DATE: October 18, 1973

FROM: Stu Wecker

DEPT: Research & Development

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SUBJ: Multiprocessor Considerations for Mid-Range 11 vol 11

It seems that "multi-processor systems" has become a key phrase in computing circles these days. Why it is remains a partial mystery, but people generally think that two or more of something must be better than one. In the case of computing where performance per dollar is a key evaluation criteria, multi-processor systems may or may not give the expected value of relative performance. There are many reasons for building multiprocessor systems. Some are:

1. More throughput--since each processor can execute X instructions per time, N processors can execute N times X instructions per time. This is very true but says nothing about the number of "useful" instructions; i.e., user mode vs. operating system, scheduling, etc....

2. High reliability--if a processor fails the system still runs, perhaps at some reduced level. This depends heavily on the operating system structure and the physical connections within the system. On the current-11 most failures take the bus also and the whole system. The operating system structure determines whether or not deadlocks and failures within critical code sections can be resolved. Maybe reliability is better addressed at a lower level; i.e., multi-voting logic, etc.

3. Incremental expandability--if each processor provides one unit of compute power then the system can be incrementally expanded one unit of power at a time. This depends heavily on statement 1 about useful power. Also, it seems that users may not want just a double or triple increase but perhaps a 10 fold one. Or is it cheaper to build a processor three times as fast compared to 3 processors and the interconnect hardware?

I may have sounded negative on multiprocessors but I rather intended to bring up the issues and stimulate some thought in the area. There are many issues to be considered and discussed before one can definitely say that multi-processing is a good thing. Now let us examine the various interconnection possibilities and their related problems.

Types of connections:

1. Closely-coupled--this is the classic multi-processor system we think about. The processors all share a commonly accessible memory from which they execute instructions.

2. Shared-coupled--the processors execute out of private memory and share some external medium for data transfer. This may be a shared disk, tape drive or even a block of memory.

3. Loosely-coupled--this is the computer network where all memory and mass storage are private and the processors are connected via a wire-type link and communication interface equipment.

Synchronization of access:

In order for the processors to successfully communicate and cooperate to perform a desired task they must synchronize their actions and accesses within the system. For connection types 1 and 2 this involves some lock/unlock mechanism so that each processor can interrogate and/or update system information without interruption by other processors. For memory systems this can be handled by read-pause-write type cycles at the hardware level and expanded into semaphores (P & V) and/or test-and-set type operations at the software level. For shared controllers or devices some type of switch and watchdog timers would provide the necessary protection. For connection type 3 the synchronization is explicit in the information flow since nothing is really shared for data storage but there is simply the sharing of a common data link.

Problems:

In connection types 1 and 2 there may be problems with potential failure within critical code sections (where a lock is active on a shared component of the system).

Interprocessor communication requirements:

To build a feasibly usable system where must be a mechanism to cause processors to examine the synchronization and cooperation system variables whenever some event of significance occurs within the system. This can be handled in a number of ways:

1. Private clocks--each processor has a clock which periodically interrupts it causing the processor to scan a system list or I/O table and take the appropriate decision branch.

2. Interprocessor interrupt--each processor can interrupt the other. The processor that "discovers" or is made aware of an event of significance notifies the other via this interrupt facility.

3. Remote console control--one processor has direct control over one or more of the others. It can effectively stop, reset pc, load registers and start another processor.

Processor relationships:

The multiple processors within a system can operate in two basic ways. The first is master where each processor runs within its own code (possibly shared) and handles all local traps, interrupts, etc. The processors cooperate but contend for resources, jobs to run, etc. by using some of the synchronization techniques described. The other is slave mode where a processor executes user type code but leaves all other handling, traps, interrupts, etc., up to the master. The slave more or less acts like an I/O device receiving its orders from some master processor.

Problems in -11's:

Some of the problems in close connection of -11's include:

1. Who gets interrupts?
2. Do BR's take precedence over NPR's.
3. I/O page absolute values:regs, PS,...

I hope these brief comments on multi-processor systems help to stimulate thought in this area. A basic point to be made here is that multiple processor systems are like systems with multiple anythings; i.e., disks, printers, etc. Namely, they are more resources of an entity called "processing capability". This is only useful in system where the processor capability is the bottleneck or where more may help some reliability issue.

SW:cw

digital INTEROFFICE MEMORANDUM

TO: Dick Clayton
Bruce Delagi
Lorrin Gale
Len Hughes
Larry Portner
Dave Stone

DATE: 10/31/73

FROM: Pete van Roekens PvR
Craig Mudge

DEPT: Medium/Large 11
Software Eng. -
11 Engineering

EXT: 4028, 5064

SUBJ: MULTI-PROCESSOR PDP-11 PROPOSAL

The subject proposal is attached.

Summary

This proposal presents a means of enhancing the cost/effectiveness of our hardware/software systems, extending the available physical memory, and potentially increasing the system's reliability by utilizing existing hardware and making relatively minor software changes.

Assumptions

The following assumptions are held to be relevant and true:

1. Processors and memory will continue to drop in cost relative to total system cost.

2. Software costs will continue to rise and therefore we:

    a. Should retain as much of it unchanged as possible.
    b. Should not introduce more complicated requirements into the coding of a user task.

3. It is possible to separate tasks performed in a single processor environment by a process structured multi-programming system into a multi-processor environment.

4. System's growth on a single processor PDP-11 is currently limited due to:

    a. Physical memory capacity.
    b. Complexity of software required for large systems with limited virtual address space.
    c. Unibus band width.

5. The PDP-11 line should be working towards new product glamour at minimal cost to extend its life by 5 or 10 years.

6. The evolving network systems and the eventual new product line require empirical data relative to combined hardware/software design that must be gathered in the near term. (i.e. we need measurements!)

Proposal

This proposal is divided into three phases. The first phase is reasonably well understood technically, although many details remain to be resolved. Measurement of this system will clearly guide us in determining the product viability and in setting the detailed direction of the remaining phases.

The proposal is based upon RSX-11M and RSX-11D for two major reasons:

a. Both are process structured multi-programming systems.
b. Both are building blocks in 11 Family systems.

Cost and Time Estimate

This effort would require two people for about three months to build and measure a Phase I prototype system. This will cost about $18K plus $10K for the additional linking hardware.

Phase II

Description

Phase II work consists of providing a mechanism to shift additional file related work load to the satellite processor. This would allow programs such as file transfer and conversion utilities, volume initialization routines, etc., to run in the satellite system.

Implementation

The same hardware indicated for Phase I obtains. The software work involves providing the mechanism in the host processor to allow the initiation of certain tasks in the satellite processor. Some form of operator or batch control appears to be the simplest mechanism. This could require specific processor designations in each request or could allow a general control statement to shift all requests for certain programs or classes of programs. The extreme case is where the host processor dynamically determines load and routes the program requests accordingly. We expect that we can provide some control which falls between the extremes cited.

Configuration Example

The configuration would be the same as for Phase I except that the satellite would be capable of running additional user tasks.

Cost and Time Estimates

This effort would require two people for about six weeks to build and measure a Phase II prototype system. The incremental cost is about $9K.

Phase III

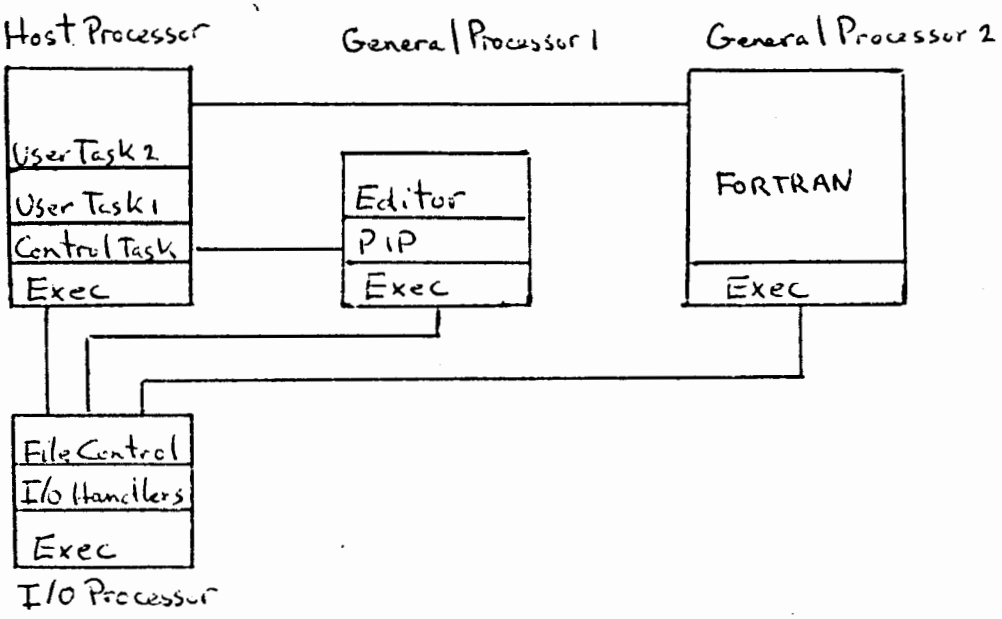
Description

Phase III work provides a logical extension to Phase II, namely to add multiple processors to the host/satellite pair.

Implementation

This implementation allows more than two processor/memory pairs in the system. The underlying principle is the same as with Phase II, that is work load presented to the system can be at the program level and given to another processor for execution

given a common file processor machine. An example of a software structure follows:



The hardware connections to actual devices becomes more complex because the RH-11 controller has only two ports. The I/O software becomes correspondingly complex. We do not know all of the implementation details. We do have some ideas and a set of problems to solve.

Configuration Example

All that can be said today is that we need the appropriate control paths and data paths to and from the I/O processor machine and to and from the host processor. These paths may vary depending on the usage of the specific machine, i.e. FORTRAN machine, Editor machine, etc.

Cost and Time Estimates

It seems clear that we have much to learn from Phases I and II before we will know enough to estimate Phase III, or in fact to know if it is worthwhile. A real guess is that about two people should work on this phase for about six months. This would bring the incremental manpower costs to roughly $36K.

Implications

Extensions of 11 Family Operating Systems

The proposed structure will allow DEC to extend in a completely compatible mode our major medium/large 11 operating systems with only relatively minor changes. The preceding implementation discussions have centered on the RSX-11D and RSX-11M Family.

These same two systems are planned as the software building blocks for the Extended BTS Family. Here too, a multi-processor approach will provide an upper end system. Finally, the potentiality exists for incorporating this approach into RSTS.

System Physical Memory Capacity Increased

Although the limits on physical memory per processor is not increased, the amount of physical memory available on a system increases with each processor/memory pair addition.

Program Structures Unchanged

Unlike some other multi-processor approaches the programmer constructs his programs in the same manner he would for a single processor system. This is because the units of work are separated at the program level.

Recommendation

The total funding required for this proposal is $73K. The time frame is about ten months for the complete effort with Phase I results in three months. There are risks of failure particularly as we approach the unknowns of Phase III. We strongly believe that the potential benefits greatly overshadow the potential risks and that therefore this proposal should be approved.

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Vol II - Reliability
C. Kaman 10/22/73

Reliability

The 11 engineering group has several ongoing investigations on improving the reliability of their product. After talking with them the following points became clear.

1. mechanical -
   a. first generation mechanical designs are not generally reliable, the lessons have not yet been learned for that design (or device)
   b. assembly is not done well; special tools are often needed, these must be made or bought and the production line people taught how to use them
   c. after making devices we often break them ourselves either in test or in delivering them to the customer

2. electrical -
   a. when a power supply dies it can damage the rest of the world (with voltage overloads, for instance) before it is switched off
   b. Unibus - besides the design problems described below the interaction with power supplies causes the entire system to fail if one unit fail
   c. Unibus - devices will be upgraded to allow them to be taken off line without powering down the entire system
   d. Unibus - stressing techniques (voltage and timing marginning) should allow removal of marginal conditions this should help the reconfiguration problem (i.e. being able to put a device on the bus without having to then shuffle devices to get the whole system running)
   e. layout - poor placement of parts can lead to shorts in manufacturing or electronic problems like crosstalk

3. engineering -
   a. designers field of understanding should be extended to include system considerations and manufacturing and field service views

4. software -
   a. reliability requires support by the systems software, this takes primary memory space at least
   b. hardware should report details of an error condition (when trapping to location 4, for instance); an error word of bit flags would be most useful

Vol II Reliability
C. Kaman 10/24/73

The attached pages explain the reliability issues as they are now understood. The porpose of our meeting is to gather additional points of view and technical ideas. It is felt by many that we must have a more reliable system from our next design.

The main objective we have is to produce an outline of what is needed for the different market areas and how we will provide those features, with an estimation of the cost. Lorrin needs this information for the report he is generating.

The following pages outline

1. the observations given me at a meeting with the 11 eng. reliability project, and
2. some of my own observations.

Aggenda :

1. specific issues
   - a. microdiagnostics and diagnostic aids
   - b. manufacturing aids to make a more reliable product (such as the extra gates used to bring out signals in the KL-10)
   - c. parity on busses, memory, and mass memory devices
   - d. remoted console use
   - e. peripheral repair without taking the system down
2. other global issues
   - a. keeping up with the competition (if any) in this area
   - b. multi-system configurations for increased reliability (these may be multi-processor or peripheral)

Outline of Comments Made at Meeting With 11 Eng. Reliability Group

Reliability

The 11 engineering group has several ongoing investigations on improving the reliability of their product. After talking with them the following points became clear.

1. mechanical -
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    b. assembly is not done well; special tools are often needed, these must be made or bought and the production line people taught how to use them
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    a. designers field of understanding should be extended to include system considerations and manufacturing and field service views

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    b. hardware should report details of an error condition (when trapping to location 4, for instance); an error word of bit flags

Some Observations

There are two reasons for our present concern with reliability:

1. several markets need dependible equipment, and
2. staffing field service at a high enough rate could limit our growth.

In addition, as the number of machines in service (i.e. in the world) grows the need for global optimization increases. That is, decisions must be made whether to build a more expensive unit which costs less to maintain or to continue to supply sufficient field service to maintain lower reliability, but initially less expensive, units.

The markets which need dependible systems (note - systems) are communications (the fastest growing segment of the company), industrial process control, and business data processing. Three aspects of reliability are identifiable: MTTF, MTTR, and error detection. The first two are related to system availability and the last to knowing that an error has been made. For instance, in business processing it is important not to make out checks when all the amounts are incorrect. In some applications detection is the major feature and MTTF/R are subordinate; in others availability is paramount (COMM and IPG).

At the present time training accounts for a large fractions of field service's costs, both dollars and manpower. If we cannot provide service for a machine we can not sell it, for the most part. Thus, at some point the speed with which we can acquire field service personnel and train them limits the company's growth. There are two ways to attack this problem :

1. build in better reliability to reduce the need for field service, and
2. include in the design aids to help field service indentify and fix problems when they arise.

The first approach moves the cost of repair in the field back to the manufacturing plant. This might be done without raising the cost to the customer. One way to do this is to build a more reliable system, another is to implement a field service policy (and a design philosophy) which favors factory repair. The fault must still be isolated in the field and, so, better fault isolation techniques are needed. The most desirable of these would both reduce the time to identify the fault and pinpoint it to the level necessary to allow the swapping of the bad unit for a good one (or whatever policy is to be employed). Among the approaches for achieving this which must be considered is the use of a remoted diagnostic center.

DIGITAL INTEROFFICE MEMORANDUM

TO: Lorrin Gale

CC: DISTRIBUTION

DATE: 10/23/73

FROM: Bob Stewart BS

DEPT: 11 Engineering

EXT: 3564 LOC: 1-2

SUBJ: ADDRESSING SUBCOMMITTEE REPORT

The committee spent most of its time discussing ways of extending virtual address space, while retaining basic PDP-11 compatibility. Several schemes involving 32 bit registers, use of mode 5 as an escape, extra spaces like I and D space, and others were discussed, but none looked useful.

The Strecker Extended Architecture proposal was discussed at length. Compared to other schemes discussed, it was felt to be a relatively clear extension to a 22 bit segmented and paged virtual address space. Dave Cutler and Ron Brender felt that it would be a reasonable system to build an operating system and FORTRAN on . One disadvantage is that the implementation cost of the hardware might be too high for a medium sized system (11/40 size). The other problem is that it would require extensive software rewriting. Bill Strecker and Dave Cutler agreed that it would take about 22 man-months of effort to get a version of RSX11-D ready for field test which used the new architecture to implement current features, that is to get back to ground zero. The effort required to actually use the new virtual address space was estimated only roughly. Dave Cutler estimated that the linker would require 9 man-months. Ron Brender estimated that FORTRAN (including OTS) would require 2 man-years of effort after the MACRO assembler was extended (easy) and the task builder was redone (not easy). Other work would be required in the storage allocator and other areas. Dave Cutler summarized by saying that it would probably be four years before extended virtual addressing had full operating system support. Bill Strecker feels that it should be more like three years, that is, one year after first ships.

The committee also discussed extending physical address space. On an integrated system such as 11/XX, it would be easy to extend the physical address space accessible to the processor's memory management unit (either the present type or the Strecker type) and the integrated Massbus controllers, so we talked about the

problem of Unibus NPR devices. Three solutions are possible. Defining a new bus to replace the Unibus has the advantage of being able to "do it right this time". The primary disadvantage is having to do new versions of lots of peripherals. Another possibility is to only allow the Unibus to address the lower 124K of physical address space. The advantage is simplicity; the disadvantage is that the operating system would have to copy buffers to and from the lowest 124K words to transfer them. The third possibility is a mapping box with several programmable relocation registers to convert Unibus addresses to physical addresses. This is relatively simple, since no protection is required. This scheme only works on an integrated system like 11/XX. One disadvantage is that this scheme represents another layer of complexity to deal with. This is the scheme that we recommend for extended physical addressing.

The committee did not spend time on memory technologies, as we felt that they were well understood compared to the addressing issues.

pl

DISTRIBUTION

Ron Brender
Jack Burness
Dave Cutler
John Levy
Steve Rothman
Bill Strecker
Stu Wecker

A minor technical point is that the size of a JSR push (subroutine call) would be determined by a bit in the status register. This would also apply to RTS, EMT's etc.

Jack

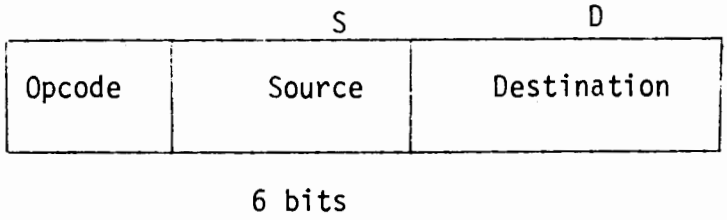
CC: Gordon Bell
Jim Bell
Dave Butler
Chuck Kaman
Bob Stewart

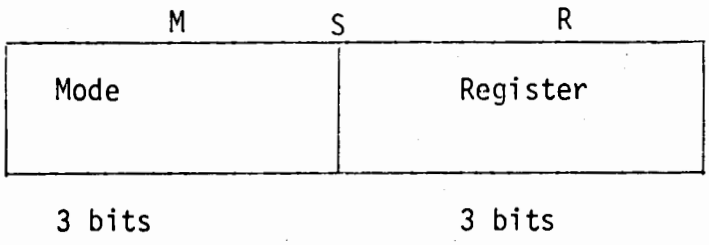
jmc

P.S. Since this memo was written, it has been decided that extended addressing (i.e. mode "5" escape) should be enabled by the status register bit.

EXAMPLE A

In a typical instruction, we have a source and a destination. The source is composed of three bits of mode, and three bits which determine the register to use. At present, mode '5' is not used (enough) to justify it's existance. This is auto decrement deferred.

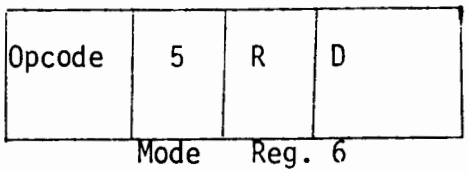




Mode = 5 not used

NEW FORMAT

If the source field in EXAMPLE A is mode 5, then the instruction is one of the new class of source instructions. The register field R of the original source is then decoded as follows:



R FIELD DECODING

The R field contains three bits, which I will call bits 0,1, and 2. The table below indicates the states and how they are decoded.

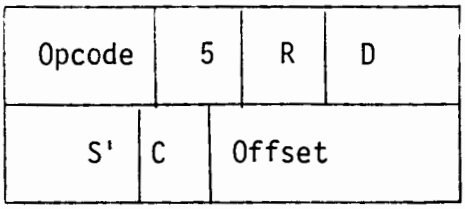
BITS 012

STATE

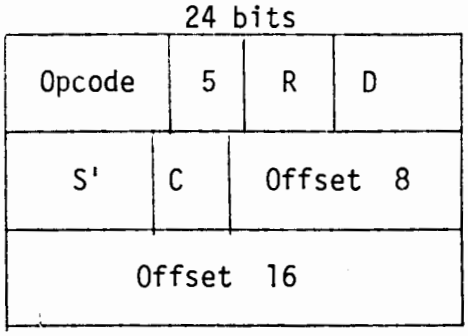
0	Source is 16 bits if word instruction, 8 if byte inst.
1	Source is 32 bits if word inst., 8 sign extended if byte
0	Reg. R' in S' is 16 bits wide (narrow index)
1	Reg. R' in S' is 32 bits wide (wide addressing)
0	There is one additional source word
1	There are two additional source words.

Note that we now control the size of the arithmetic, and the size of the index. The next word contains the new (or correct) source field S', which is decoded in the "normal" fashion. However, the offset, is added to the value of S', thus giving us an index of 24 bits. If bit 2 of R was a 0 (see above) then only 8 bits are added. This gives us small offsets on S'. (Mode 7 in S' is still immediate, but length implied in bit 2 of R).

If bit 2 of R = 0



If bit 2 of R = 1

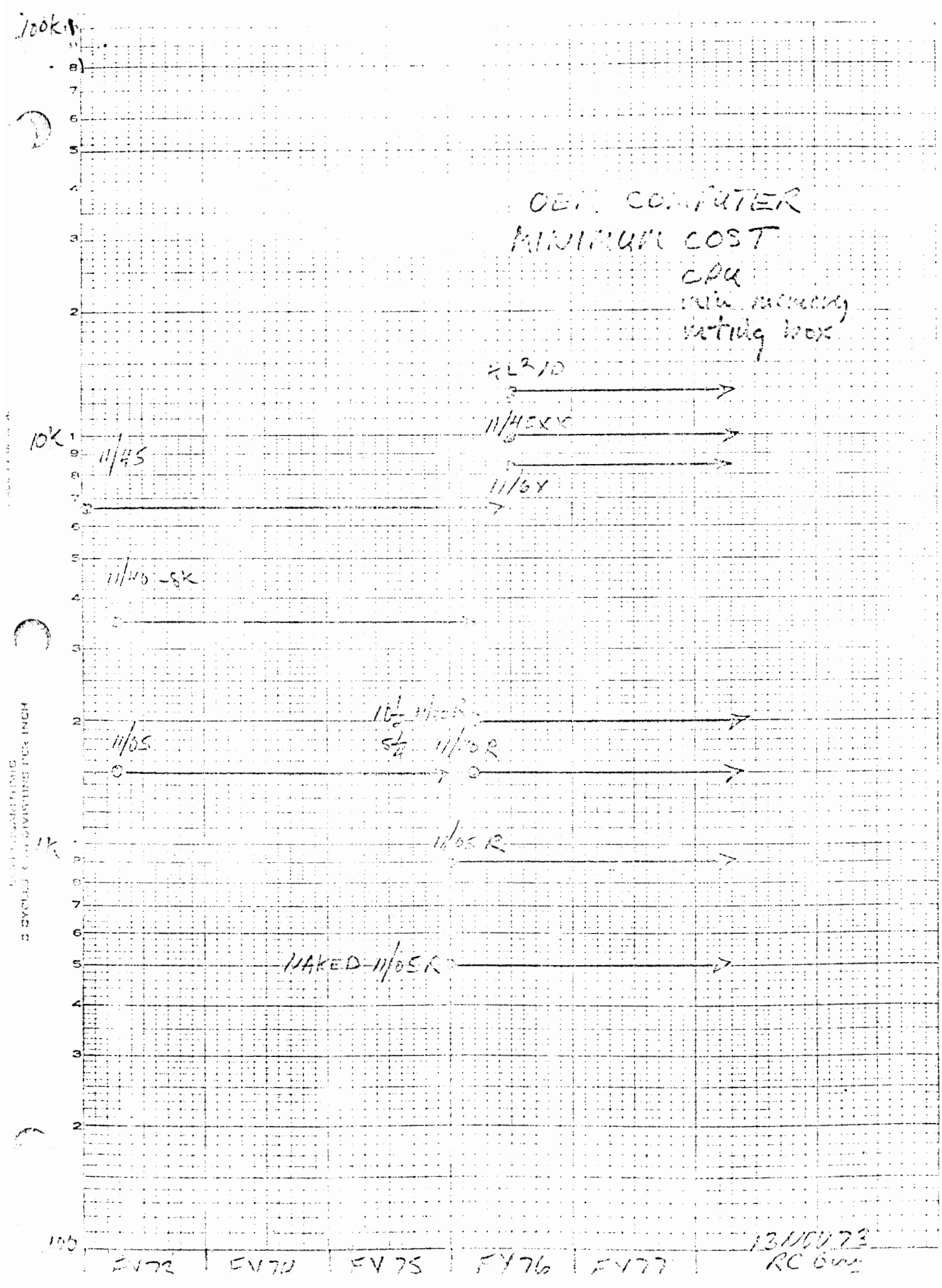


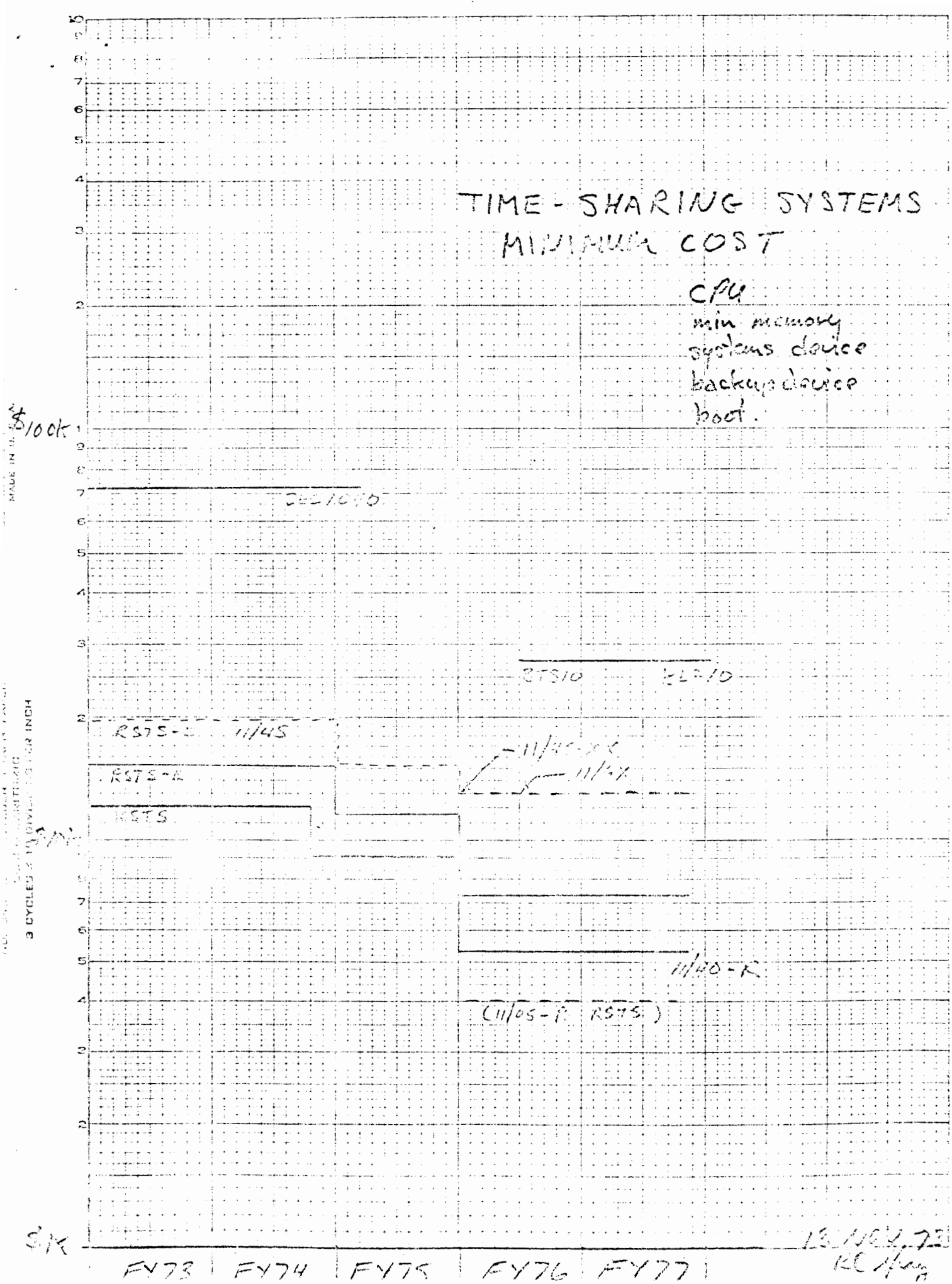
The C field contains additional information about the new source field S'. It is two bits long and decoded as follows:

BITS 01

STATE	0	Take R' "as is".
	1	Shift R' by context before using. Very nice feature
	0	If indirect, go indirect through 16 bits only
	1	If indirect, go through 32 bits, using new S' and C

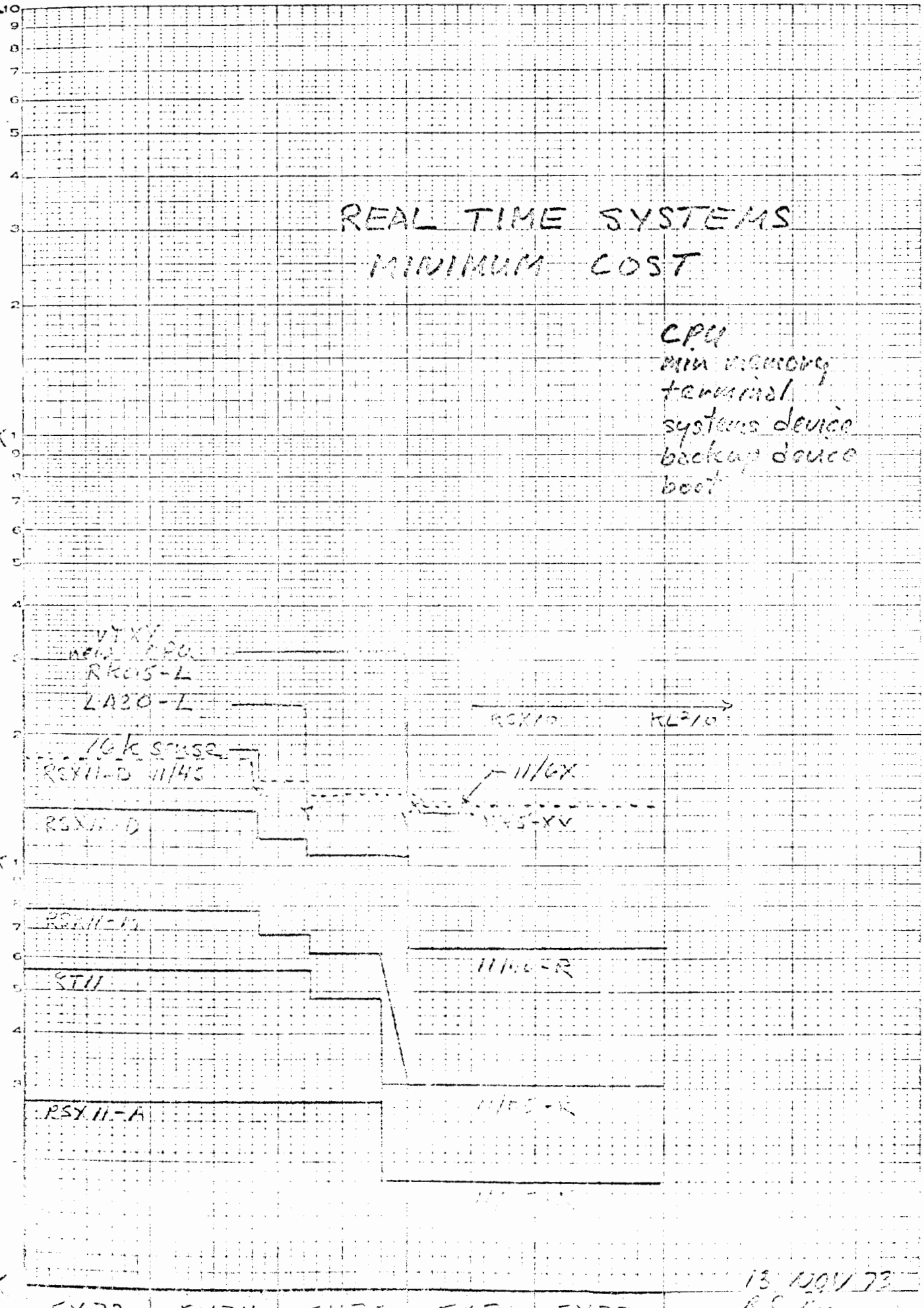
Well that's basically it. The destination is the size of the source, if not specified. The destination is also decoded if it has mode '5' specified. In that case the source is taken as the size of the dentination.


100K
10K
1K
100
OBC COMPUTER
MINIMUM COST
CPU
min memory
wiring box
+L²/D
11/45XX
11/45
11/60
11/40 -8K
11/05
11/05R
11/10R
11/05 R
NAKED-11/05K
FY72
FY73
FY75
FY76
FY77
13NOV73
RC 6m

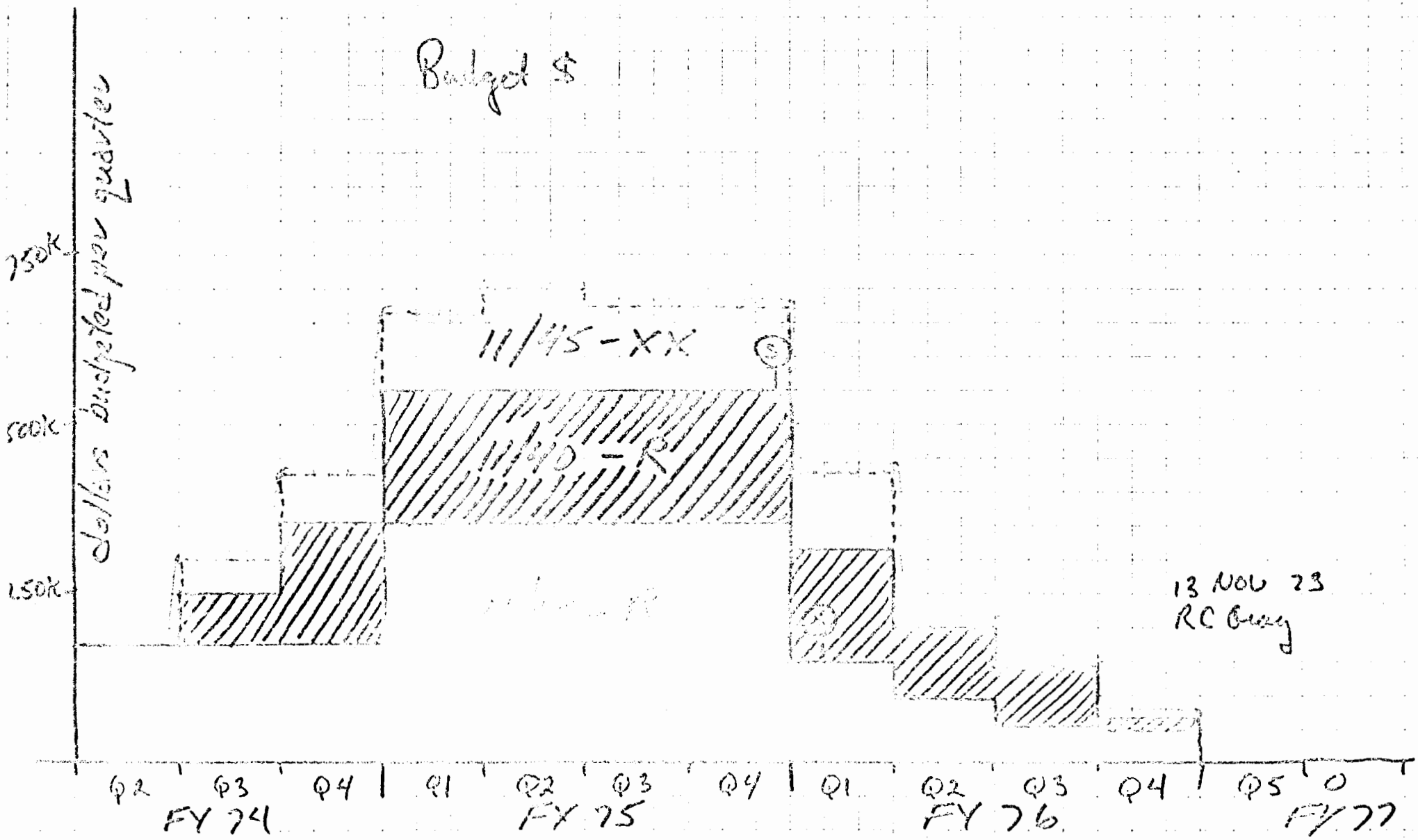

TIME-SHARING SYSTEMS
MINIMUM COST
CPU
min memory
systems device
backup device
boot.
$100K
$10K
$1K
DEC 10/10
DTS10
KL-10
RSTS-E 11/45
RSTS-E
RSTS
11/40-E
11/40-F
11/40-K
(11/05-F RSTS)
FY73
FY74
FY75
FY76
FY77
12/10/73
RC/fm

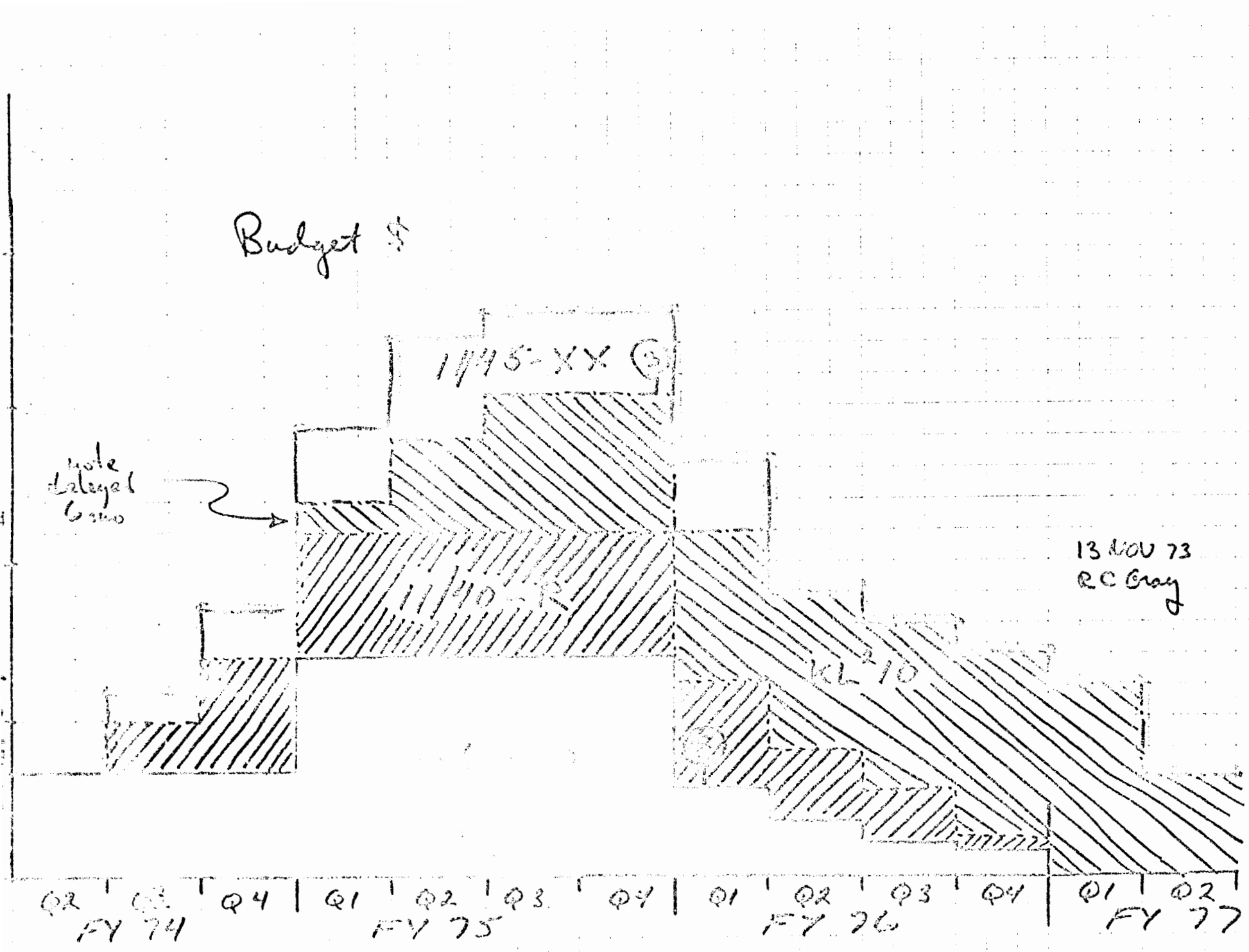
REAL TIME SYSTEMS
MINIMUM COST

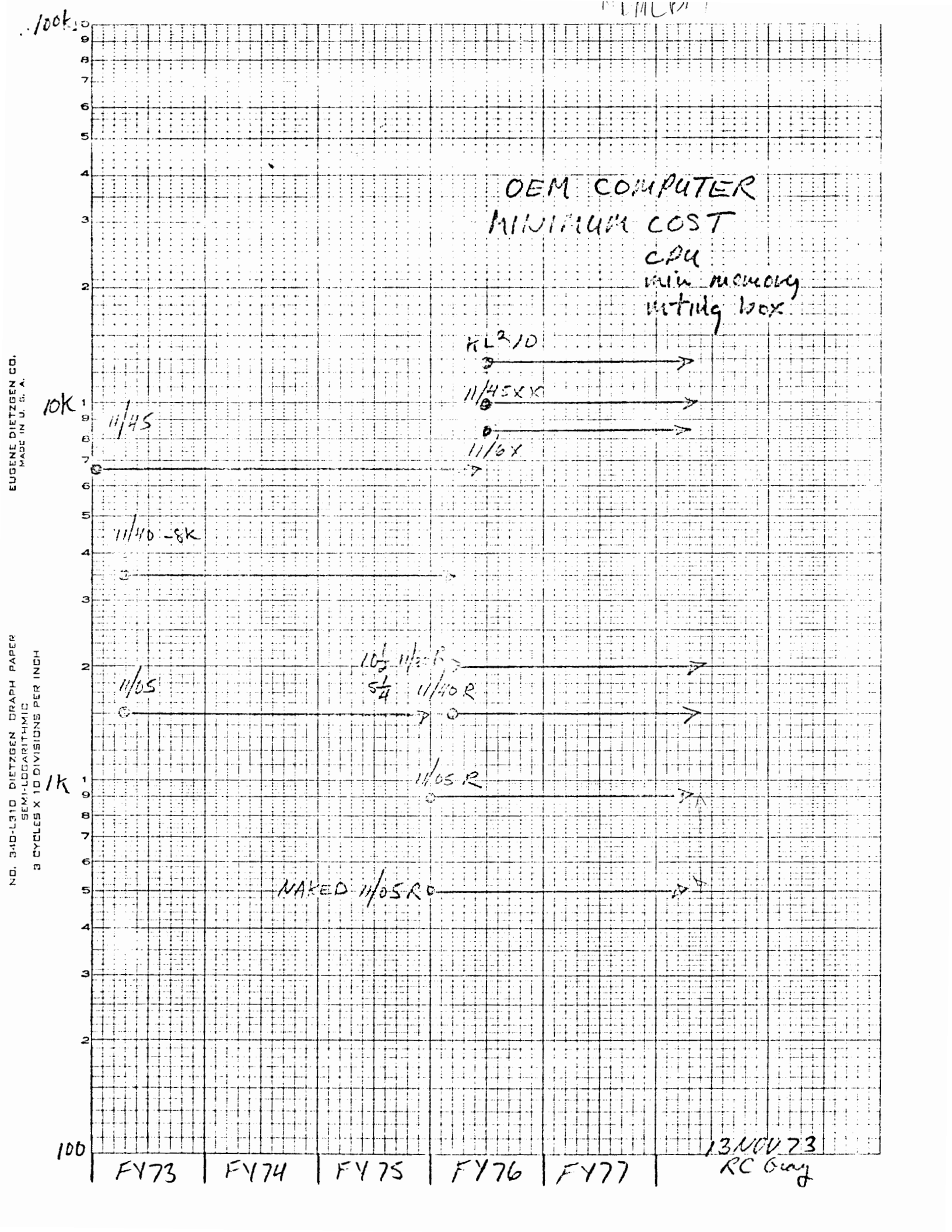
CPU
min memory
terminal
systems device
backup device
boot

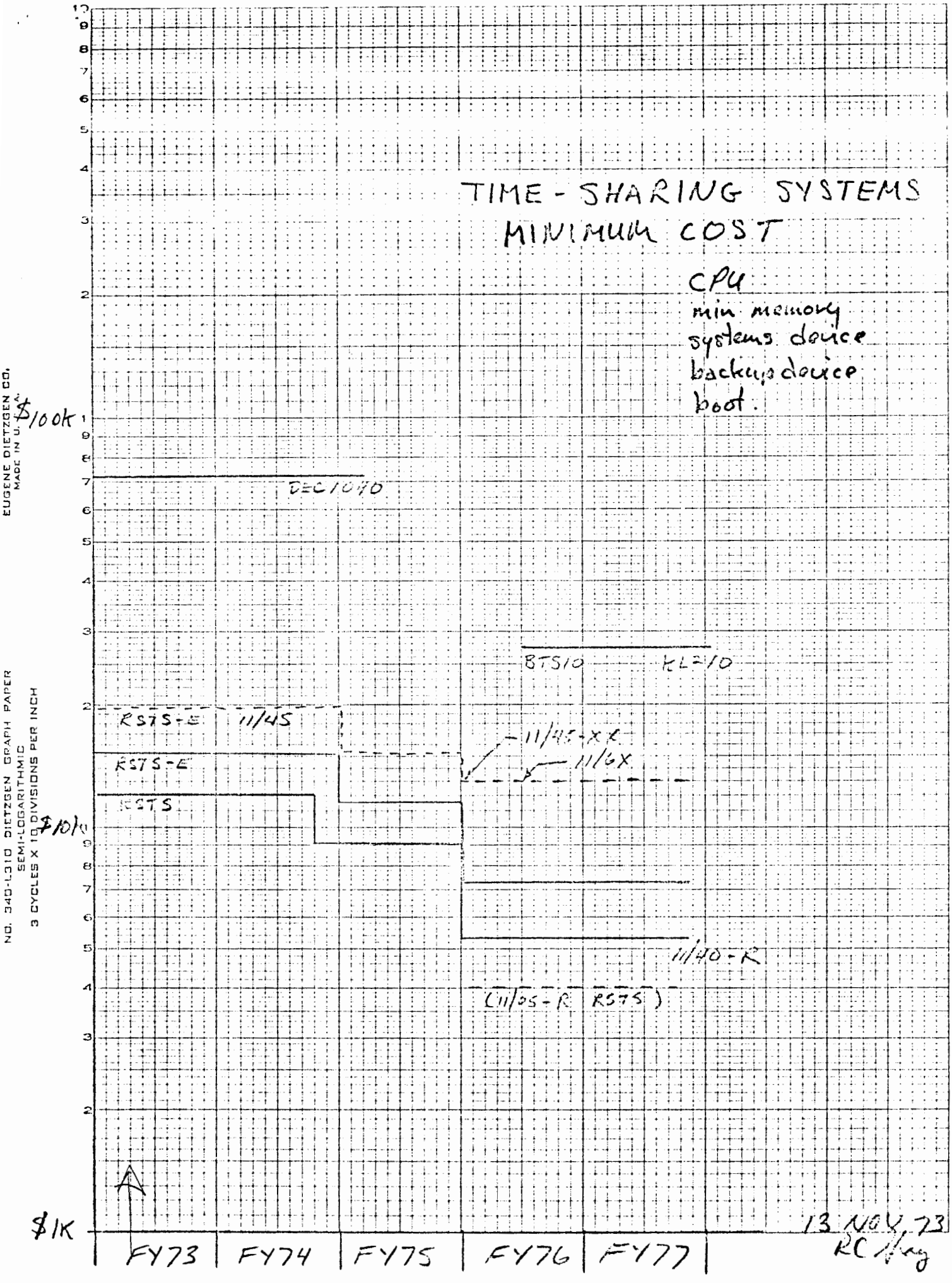


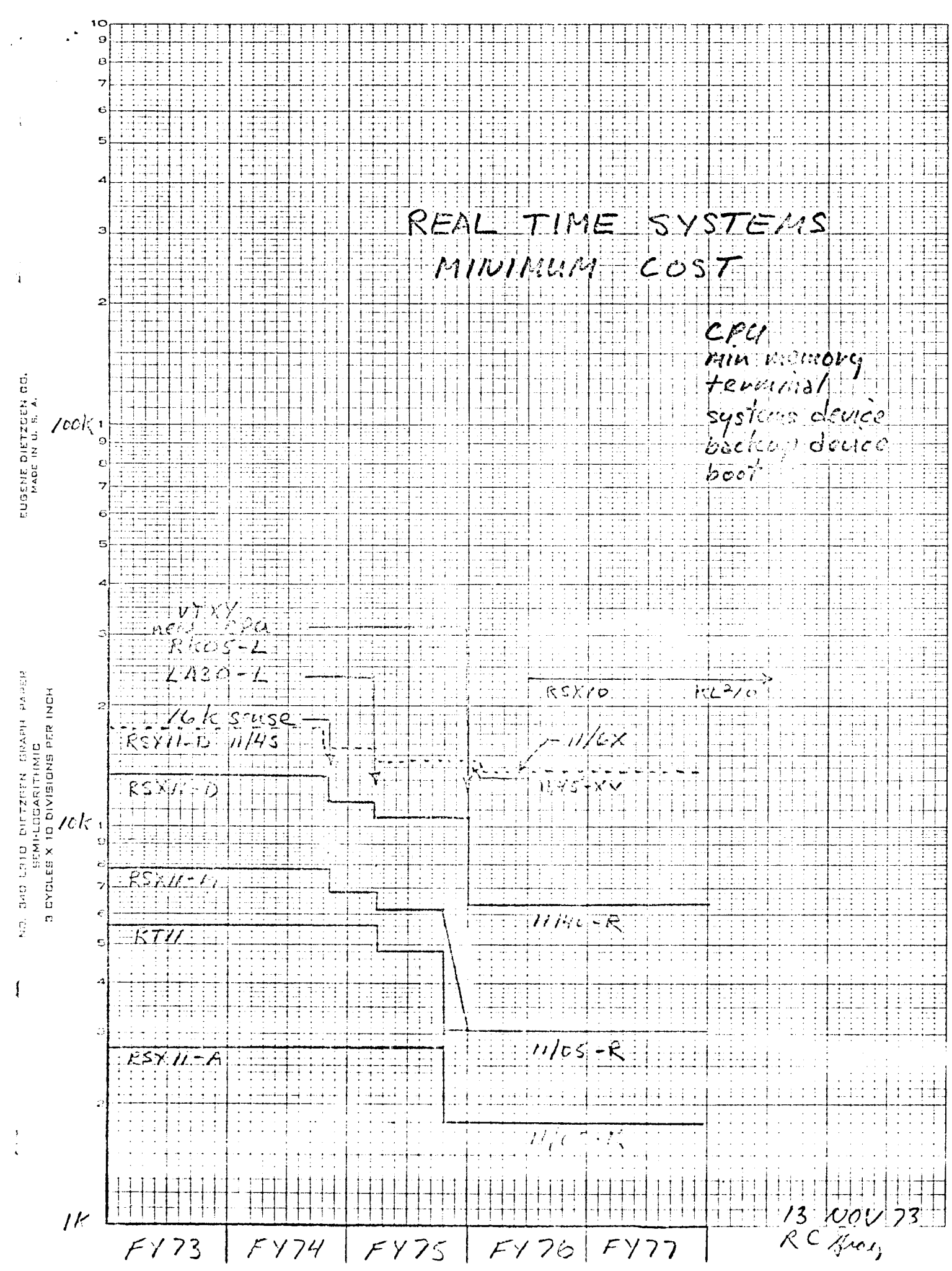
13 NOV 73
RC Rev.

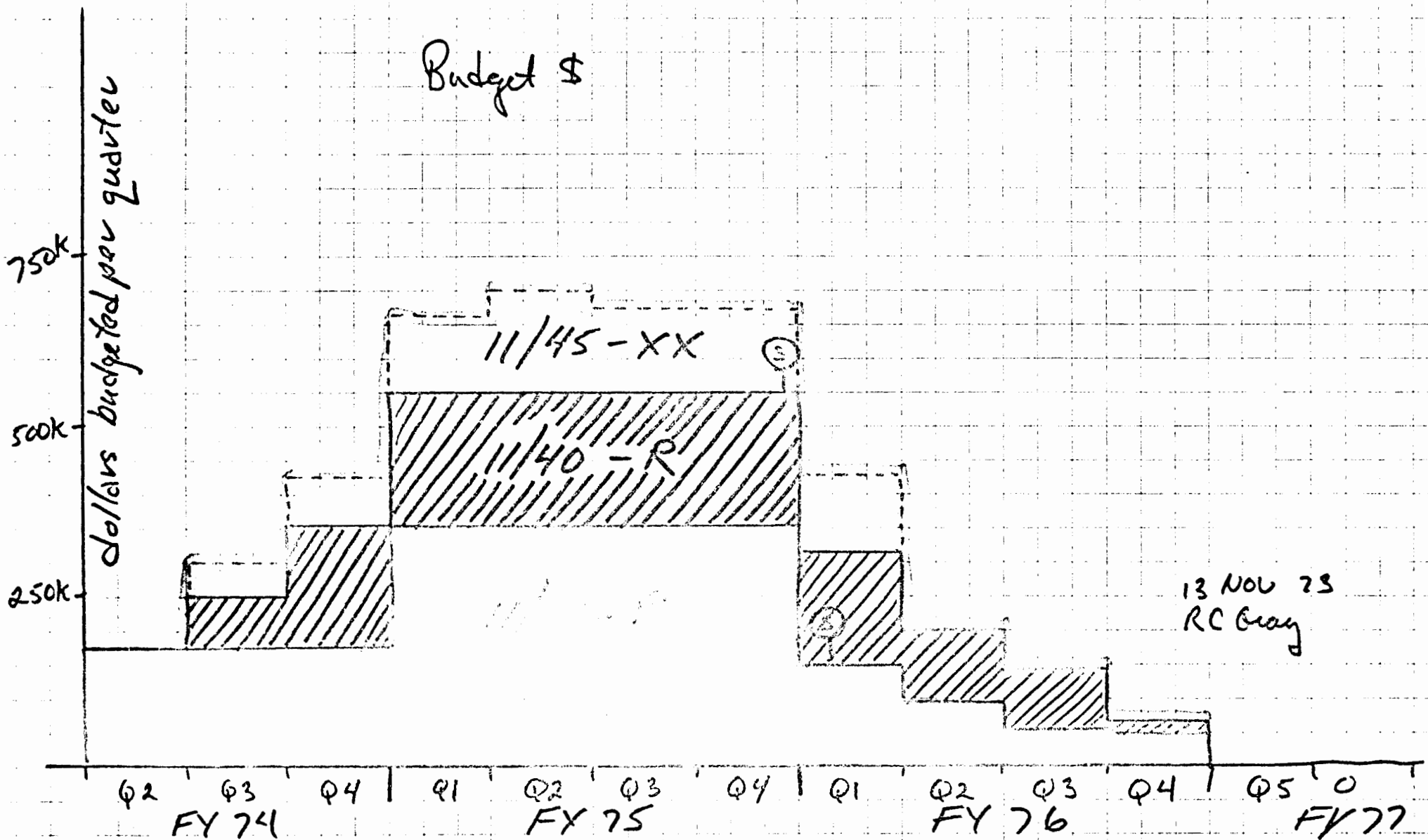

Budget $
Dollars budgeted per quarter
750K
500K
250K
11/15 - XX
Q2
Q3
Q4
Q1
Q2
Q3
Q4
Q1
Q2
Q3
Q4
Q5
FY 74
FY 75
FY 76
FY 77
13 NOV 23
RC Burg

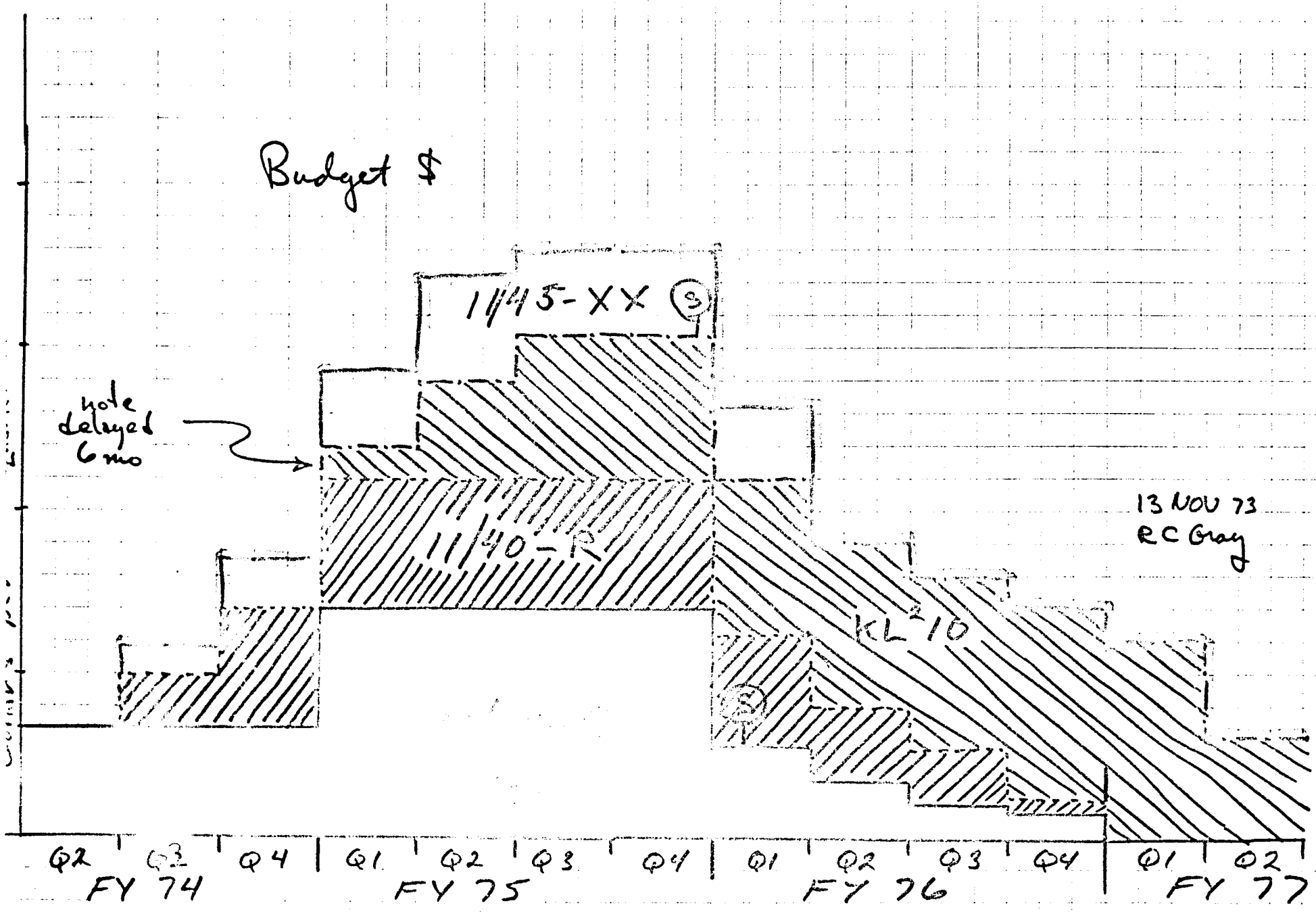

Budget $
1145-XX
Note Integral Gains
13 NOV 73
RC Gray
Q2
Q3
Q4
Q1
Q2
Q3
Q4
Q1
Q2
Q3
Q4
Q1
Q2
FY 74
FY 75
FY 76
FY 77


100K
10K
1K
100
OEM COMPUTER
MINIMUM COST
CPU
main memory
wiring box
KL²/10
11/45XX
11/60X
11/45
11/40 -8K
10½ 11/40R
5¼ 11/40R
11/05
11/05R
NAKED 11/05R0
FY73
FY74
FY75
FY76
FY77
13NOV73
RC Gray
EUGENE DIETZGEN CO.
MADE IN U.S.A.
NO. 340-L310 DIETZGEN GRAPH PAPER
SEMI-LOGARITHMIC
3 CYCLES X 10 DIVISIONS PER INCH

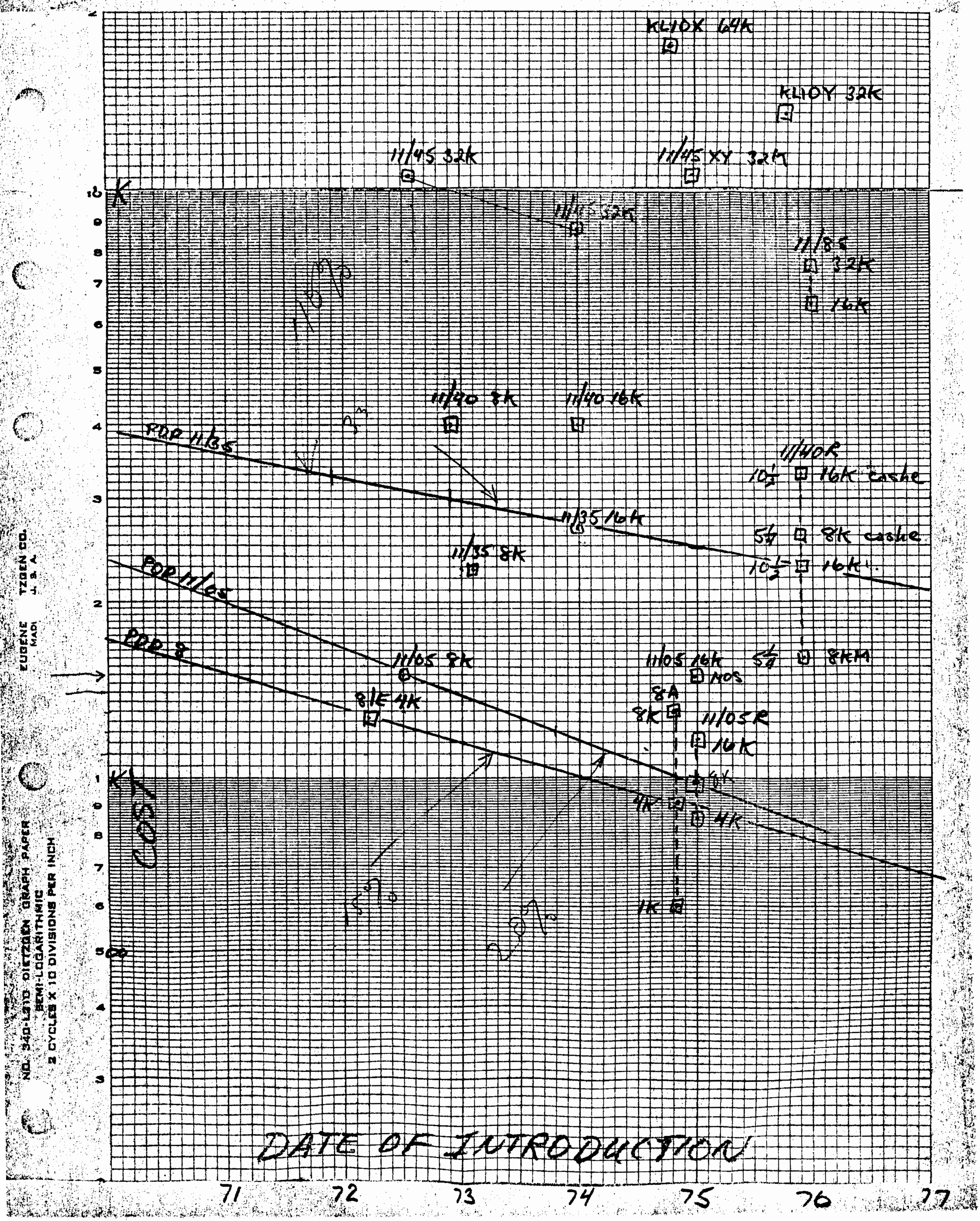



REAL TIME SYSTEMS
MINIMUM COST
CPU
min memory
terminal
system device
backup device
boot
100K
10K
1K
VTXY
RSX10
KL2/10
16k suse
RSX11-D
11/45
11/60
11/45-XV
RSX11-D
RSX11-M
11/40-R
KTII
11/05-R
RSX11-A
FY73
FY74
FY75
FY76
FY77
13 JUL 73
RC


Budget $
dollars budgeted per quarter
750k
500k
250k
11/45-XX
40-R
13 NOV 73
RC Gray
Q2
Q3
Q4
Q1
Q2
Q3
Q4
Q1
Q2
Q3
Q4
Q5
FY 74
FY 75
FY 76
FY 77


Budget $
1145-XX
note delayed 6 mo
1140-P
KL-10
13 NOV 73
RC Gray
Q2
Q3
Q4
Q1
Q2
Q3
Q4
Q1
Q2
Q3
Q4
Q1
Q2
FY 74
FY 75
FY 76
FY 77

KL21Φ	11/6X	11/45 ME	11/40R CACHE		11/40R NO CACHE	11/40L	11/05R	PRODUCT	
									1/9/73 ELAGI RAY ADE
									11/40L KL
—	.55	.44	0.8		1.0		5.2	PERFORMANCE MEASURE	ADD R,R 16
1.0	.70	1.3	2.4		3.0		11.7		ADD R,R 32/36
27	24	24			17.7		17.7		I/O BW-MB
65	64	56			17.7		17.7		MEM. BW-MB
24	22	16			16		16		VIRTUAL SIZE
24	22	20			16		16		PHYS. SIZE
ALL BUS PAR. MEM. BUS?	ALL BUS PAR mem. BUS	MEM PAR NO	MEM PAR		MEM PAR NO		MEM PAR CP ON UNI	FEATURES	RELIABILTY FEATURES
NO	NO	NO	11		YES (OPT)		NO		MULTI-PROC. HOOKS
									USER MICRO. PROG
DOS14	IID	11.M	IID	11.M	11.M	RT 11.M CORE	CMS*	11.M CORE	CONFIGURATIONS & MFG. COST OP. SYS
ALL	F,B COBOL	FTN BAS	F,B COB	FTN BAS	FTN BAS	FTN BAS	FTN BAS	FTN BAS	LANGUAGES
8.9	8.7	7.7	9.2	7.8	1.96	.79	.79	4.5	4.5 CPU
64K	64K	32K	64K	32K	32K	16K	8K MOS	8K	8K MEMORY
4Φ	4Φ	2Φ	0Φ	2Φ	4SL	4SL	-		- DISKS
4-VT	4-VT	VT-BP W/CT	4 - VT-BP	VT-BP	2-VTBP	VT-BP	-	CT VT-B	- TERMINALS
32.4	35.4	16.0	35.5	17.9	8.4	5.4	1.6	1.7	4.9 TOTAL ($K)
Q3		Q3		Q1			Q2		Q3 FIRST SHIP
76		76		76			76		75
.51		.25		.16			.25		.5 FY74 $M DEV
1.7		1.9		.79			1.1		1.5 FY75 $M DEV
3.5		3.7		1.4			2.0		2.1 TOTAL $M DEV
DL,XY 32K SEMI		DL,XY					VT-B Φ5L		DEPENDS ON
NW FULL MORE VIRT		HIGH SPEED				40% COST, EIS CACHE OPTION			1/2 COST COALS
MORE PHY.		I/O GW							
32 bit ARITH		LOW COST							
NEW INSTR		MORE PHY;							
		A, SPARE							
RE VA,									
+ ARR									



KL10X 64K
KL10Y 32K
11/45 32K
11/45 XY 32M
11/45 32K
11/85
32K
16K
11/40 8K
11/40 16K
PDP 11/35
11/40R
10½ 16K cashe
5¼ 8K cashe
10½ 16K
11/35 16K
11/35 8K
PDP 11/05
PDP 8
11/05 8K
11/05 16K
NOS
5¼ 8KM
8/E 4K
8A
8K
11/05R
16K
8K
4K
4K
1K
COST
DATE OF INTRODUCTION
71
72
73
74
75
76
77
NO. 340-L310 DIETZGEN GRAPH PAPER
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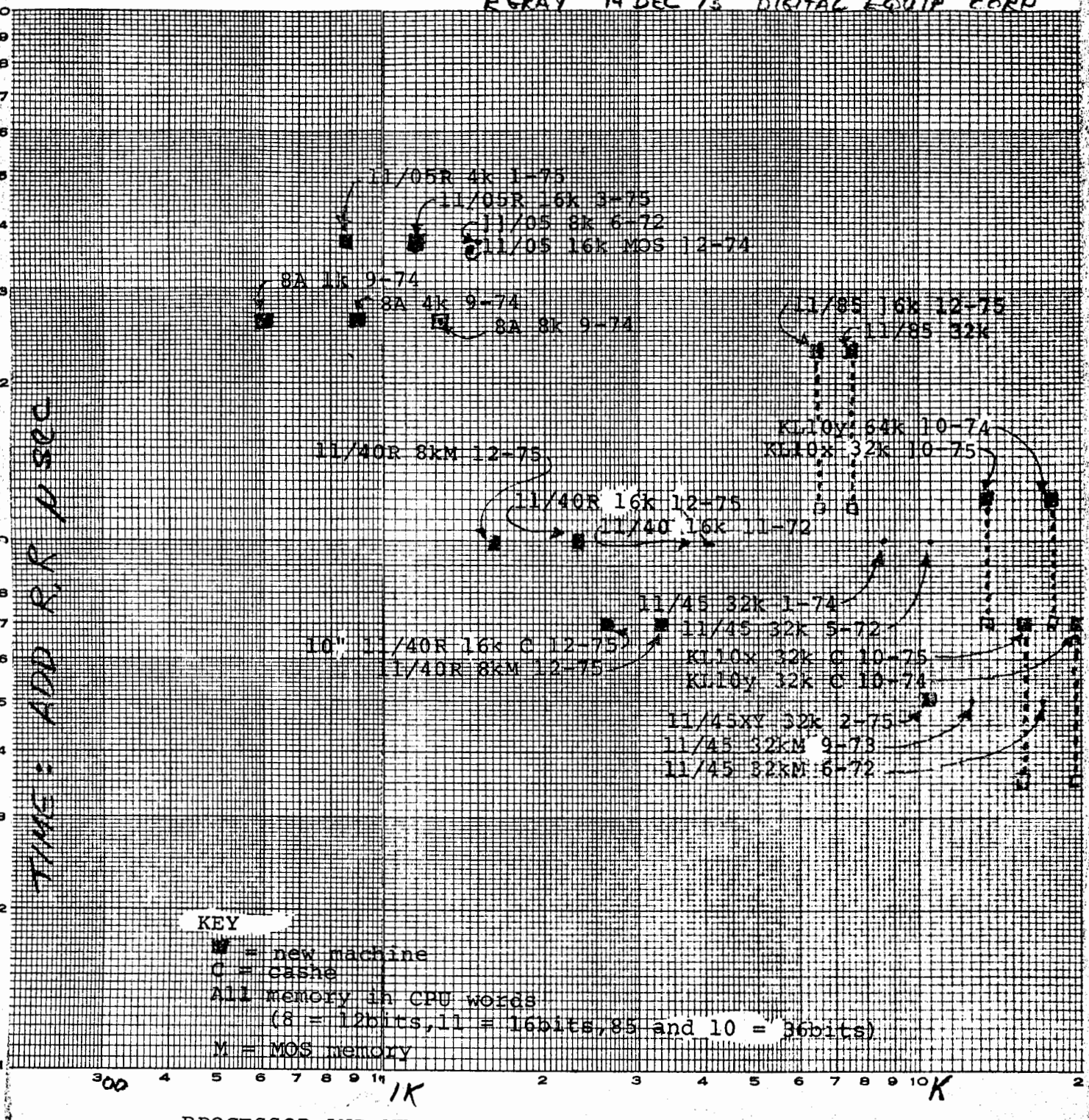
$P = nC^2$

R GRAY 14 DEC 73 DIGITAL EQUIP CORP



PROCESSOR AND MEMORY COSTS

CPU	BOX	MEM	BITS/WD	TYPE	Also Included	FCS	COST	ADD
8/E	10	4K	12	C		2/72	1.26	2.6
8/A	↓	1K	↓	M		9/74	.58	↓
↓	↓	4K	↓	↓		↓	.9	↓
↓	↓	8K	↓	↓		↓	1.3	↓
11/05	5	8K	16	C		6/72	1.5	3.7
↓	10	16K	↓	M		12/74	1.5	↓
11/05-R	5	4K	16	M		1/75	.85	3.7
↓	↓	16K	↓	↓		↓	1.15	↓
11/35	10	8K	16	C		2/73	2.3	.99
↓	↓	16K	↓	↓		12/73	2.7	↓
11/40	21	8K	16	C		11/72	4.0	.99
11/40R	5	8K	16	M		12/75	1.6	.99
↓	↓	↓	↓	↓	cache	↓	2.6	.7
↓	10	16K	↓	C		↓	2.3	.99
↓	↓	↓	↓	↓	cache	↓	3.3	.7
11/45	21	32K	16	C	KT	5/72	10.5	.99
↓	↓	↓	↓	↓	↓	11/74	8.7	.99
↓	↓	↓	↓	M	↓	5/72	17.0	.5
↓	↓	↓	↓	↓	↓	9/73	12.5	.5
11/45XY	21	32K	16	C	cache, KT	2/75	10.2	.5
11/85	21	16K	36	C		12/75	6.5	2.3
↓	↓	32K	↓	C		↓	7.5	2.3
KL10X	NA	64K	36	C		10/74	17.6	1.2
↓	↓	↓	↓	↓	cache	↓	21.0	.7
KL10Y	NA	32K	36	C		10/75	13.4	1.2
↓	↓	↓	↓	↓	cache	↓	16.9	.7

KEY

M = MOS memory
C = Core
Add - time in μsec
FCS = first customer ship

R Gray 14 Dec 73
Digital Equip Corp

digital INTEROFFICE MEMORANDUM

TO: Len Hughes
CC: Distribution

DATE: 12/3/73

FROM: Bob Gray

DEPT: 11 Engineering

EXT: 3444 LOC: 1-2

SUBJ: FORTRAN AND THE MIDI MARKET

The attached comments and statistics attempt to characterize the importance of and the relationship of FORTRAN at the midi computer level.

The material substantiates the belief that FORTRAN is important and that its importance is growing.

PDP15 EXPERIENCE WITH FORTRAN (PER ED WARGO)

All PDP-15's ship with FORTRAN and have since 1968 when the product was announced.

The shift over the past five years has been for customers to do more work in the FORTRAN language.

It is estimated today that, overall 40% of the programming with PDP-15's is done in FORTRAN.

PDP-11/45 EXPERIENCE WITH FORTRAN
(Various 11/45 Marketing Group Members)

FY74 Projections of systems with operating systems

With FORTRAN .	432	90%
Without FORTRAN	48	10%

(Of the 10% without FORTRAN, 1/2 are RSTS systems having BASIC.)

BENCHMARKS - Of some 150 benchmarks submitted, all but 2 or 3 were FORTRAN.

* 881 Total Ships - 49% get fortran - 5% get an operating system with no fortran - 46% get neither an operating system nor fortran

COMPETITION - Most are giving heavy promotion to FORTRAN - even though they are ads aimed at OEM and Computernik amounts. This includes Data General, Mod Comp, Data Craft and Varian.

Data General in particular seems to be pushing their customer base over to FORTRAN (maybe to ease the transition to an incompatible machine?).

PROJECTED MARKET AREA USE

INDUSTRIAL - Currently 50% FORTRAN. The Process Control and Manufacturing segments are almost 100% FORTRAN, with the Data Acquisition segment being almost 100% assembly. In two years, DA will be 50% FORTRAN.

OEM - Currently 40 - 45% FORTRAN and rising.

COMPUTATION - 90% FORTRAN, some can be converted to BASIC when interactive use is demanded.

Quantities of PDP-11 System Forecast for FY74

Languages Shipped	#	%
Assembly and FORTRAN	1511	44%
Assembly only	1399	40%
Assembly and Basic	306	9%
Basic only (RSTS and RSTS/E)	252	7%
TOTAL SYSTEMS WITH LANGUAGE		
Assembly	3216	93%
FORTRAN	1511	44%
Basic	558	16%

MCCRACKEN STUDY

D.D. McCracken Survey of Student High Level Language Use by College Students in First Computing Course (DATAMATION, May 1973)

FORTRAN	70%
BASIC	13%
PL/*	8%

EDP LANGUAGE PREFERENCES
(A.S. Philippakis Oct. 1973 DATAMATION)

Using % of users times their % use of the language we have the following ratings:

COBOL	59
Assembly	20
RPG	6
FORTRAN	5
PL/I	4
BASIC	1

The only language gaining in users was BASIC, where in the sample of 164 users, 5 used BASIC for the first time during the past 12 months.

40% of schools questioned believed FORTRAN would continue to be dominant in 5 to 10 years. 27% ranked the probability as low.

My impression is that FORTRAN since the early 60's has completely displaced Assembly in this market.

Note that FORTRAN is a sweet 16 years old and that PL/I and BASIC are both only 8 years old.

The probability is that by 1983 we would see a shift in distribution as follows:

BASIC	40%
PL/I	30%
FORTRAN	30%

Recall that most high schools (real, first computer course) use BASIC. BASIC, however, tends to be outgrown due to 1) subroutine restriction and 2) variable naming conventions.

The following ads appeared in Computer World and the 2 December 1973 Boston Globe:

LANGUAGE	GLOBE	COMPUTER WORLD
Assembly	24	6
COBOL	9	7
FORTRAN	3	
ALGOL	2	
PL/I	1	

This give some indication of where expansion is taking place - industry wide!

"Assembly" included all diagnostic and operating system positions.

digital INTEROFFICE MEMORANDUM

TO: Larry Wade

DATE: December 7, 1973

FROM: Nathan Teichholtz

DEPT: Engineering

EXT: 2533 LOC: 12-1

SUBJ: Normalized Fortran Performance (Current and Proposed Machines)

In an effort to make Fortran performance comparisons between some proposed machines a bit easier, I have updated and corrected some of the figures in my November 9 memo on this subject.

The attached tables give execution times for four benchmarks. In each case, the numbers were obtained by running the program on a known configuration, and then compensating this result to reflect proposed (or actual) performance differences. This makes it easier to compare numbers, but essentially adds no 'information' to the existing base; you should not, for example, interpret the KL1Ø numbers as anything but one-third of the corresponding KI1Ø times; where three-to-one is the expected performance ratio.

Table I gives the derived times; Table II gives the performance of all machines relative to the '11/F'.

TABLE II. PERFORMANCE RELATIVE TO '11F'

CPU	11/40R	11/45	11/F	KA10L	KA10L	KL10
OPTIONS/ MEMORY	CACHE NEW FIS KT11	MOS FPP KT11	CACHE FBOX			TOPS-10
COMPILER OPT. LEVEL	F/45 1*	F/45 1*	F/45 1*	F/10 1	F/10 3	F/10 3
HANOI (INTEGER)	2.8	1.7	1	3.9	1.8	.4
DG3 (FLOATING)	3.3	1.7	1	1.3	1	.25
FFT (FLOATING)	3.4	1.7	1	1.2	1	.24
SINGLE (FLOATING)	3.4	1.7	1	1.2	1.2	.3

* THE ACCOMPANYING NOTES ARE AN INTEGRAL PART OF THIS TABLE

TABLE I. DERIVED EXECUTION TIMES

CPU	11/40R	11/45	11/F	KA10L	KA10L	KL10
OPTIONS/ MEMORY	CACHE NEW FIS KT11	MOS FPP KT11	CACHE FBOX			TOPS-10
COMPILER OPT. LEVEL	F/45 1*	F/45 1*	F/45 1*	F/10 1	F/10 3	F/10 3
HANOI (INTEGER)	62.14	37.64	22.14	87	40.5	9
DG3 (FLOATING)	16.19	8.3	9.88	6.23	5.12	1.23
FFT (FLOATING)	8.75	4.31	2.54	2.91	2.49	.6
SINGLE (FLOATING)	8.0	4.0	2.35	2.91	2.91	.7

* THE ACCOMPANYING NOTES ARE AN INTEGRAL PART OF THIS TABLE

NOTES, BACKUP DATA, and ASSUMPTIONS

1. There is currently some confusion in the classification of compiler optimization levels within DEC. FORTRAN/45 is currently defined to be Level 2 on the Brender scale, which is a little above Level 1 on the Knuth scale. Knuth's classification scheme leaves much to be desired, and also fails to accurately describe FORTRAN-10. (See ABEL 100-310-119-00.)

   Never the less, there is some agreement that the level of optimization of FORTRAN/45 approximately equals that of FORTRAN-10 with optimization disabled; thus these comparisons (columns 1-4) reflect differences in hardware, rather than software technology. The remaining figures reflect the more extensive optimization capability of FORTRAN-10. It is not clear that it is practical or realistic to attempt to extend FORTRAN/45 to this level, owing to the large data base needed to effect such optimizations.

2. Timings for the 11/40R are based on simulated 11/40 timings, compensated for performance improvements due to cache and better FIS/FPP. The base times are from Knight's October 15 memo. Cache provides a 1.4 performance boost; a better FIS yields a 1.2 factor. This latter figure is almost all noise, since new FIS/FPP data was unavailable to me.

   The derived times were computed as integers;

   BASE ÷ 1.4 ÷ 1.2 x 1.2 = DERIVED TIME

   - 1.4 ÷ : CACHE IMPROVEMENTS
   - 1.2 ÷ : KT11 OVERHEAD
   - 1.2 x : FORTRAN OPTIMIZATION

   Floating point:

   INTEGER FACTOR ÷ 1.2

PROGRAM	KNIGHT'S TIME	DER. TIME
HANOI	87	62.14
DG3	27.2	16.19
FFT	14.7	8.75
SINGLE	13.4	8.0

3. Timings for 11/45 with MOS, parity, KT11, and FPP were derived from Rich Grove's figures for FORTRAN/45 running under DOS (i.e., no KT11 or parity) on a core based 11/45. Fudge factors here included:

MOS/CORE RATIO	1.7-1.3	(worse for floating point)
SEGMENTATION PENALTY	.83	(with MOS)
FORTRAN OPTIMIZATIONS	1-2	(Level 1 to Level 2)

The table below indicates the original and compensated times, and the value of the MOS/CORE ratio used, which is dependent on the extent of floating point work in the program.

	CORE/MOS	ORIGINAL	CORRECTED
HANOI	1.7	64	37.64
DG3	1.5	12.5	8.3
FFT	1.3	5.6	4.31
SINGLE	1.3	5.2	4.0

4. Timings for the 11/F were computed as 1/1.7 times the 11/45, MOS times. This seems to be a conservative assumption.

5. Timings for the KA1ØL, using FORTRAN-10 without optimization were derived from actual KI1Ø times, as measured on both CS/2 and SYSTEM #514. The latter was lightly loaded, CS/2 was moderately loaded, and reported times agreed. (Let's hear it for the DK1Ø!)

   The fudge factors applied were:

   INTEGER RESULTS:

KI/KA1Ø	.67
KA1Ø/KA1ØL	1.0

   FLOATING RESULTS:

KI/KA1Ø	.56
KA1Ø/KA1ØL	1.3

PROGRAM	KI1Ø	KA1ØL
HANOI	58	87
DG3-	4.5	6.23
FFT	2.1	2.91
SINGLE	2.1	2.91

6. Times for KA1ØL with all FORTRAN-10 optimization features are derived from actual KI times as above.

PROGRAM	KI1Ø	KA1ØL
HANOI	27	40.5
DG3	3.7	5.12
FFT	1.8	2.49
SINGLE	2.1	2.91

7. Times for KL1Ø with all FORTRAN-10 optimizations are derived from KI time; KL1Ø is assumed to be factor of 3 better.

PROGRAM	KI1Ø	KL1Ø
HANOI	27	9
DG3	3.7	1.23
FFT	1.8	.6
SINGLE	2.1	.7

INTEROFFICE MEMORANDUM

NOV 9 1973

TO: Bruce Delagi, Bob Gray, Len Hughes, Lorrin Gale

cc: Ron Brender, Norma Abel, Ashley Grayson, Gordon Bell, Larry Wade, Jack Burness

DATE: November 9, 1973

FROM: Nathan Teichholtz

DEPT: Engineering 12-1

EXT : 2533

SUBJ: FORTRAN/45 versus FORTRAN-10 Benchmark

The attached tables detail comparative execution speed and object code size for FORTRAN/45 (as predicted by Grove) and FORTRAN-10.

The FORTRAN/45 results were computed when FORTRAN/45 was planned to be a level 1 optimizer. (It has since changed scope to level 2.) Thus, from the standpoint of comparing machines, it's better to compare the FPU-inline results with non-optimized FORTRAN-10.

The -10 is more than twice as fast as the 11/45 in floating-point oriented FORTRAN programs, and about even with the 45 in integer operations (for integers that will fit in 16 bits). Integer*4 work on the 45 will incur time penalties not present on the 10. Floating point speed on the 11 suffers for two reasons:

(1) Each memory reference involves two memory operations

(2) Loop indicies require adjustment (usually multiplication by 4) before they can be used as array indicies. This problem is aggravated by the lack of a single word "shift left two places" instruction.

It should be noted that (1) would be helped by a 32 bit architecture, while (2) would not.

The data concerning program sizes is less complete and thus harder to draw conclusions from. (The problem is that only the speed-critical parts of each benchmark were hand-coded, and the remainder was left in "MOP" code; this has little effect on speed tests, but much impact on space measurements.) For three of the benchmarks, I have obtained:

a. total size (MOP instructions & hard code)
b. size of hard-coded portion
c. number of instructions in hard-coded portion.

From this data, it is possible to draw the following conclusions:

1. FORTRAN-10 programs are typically slightly more than half the size of the corresponding FORTRAN/45 code. F40 is slightly better in the code-size department than F10.

2. FORTRAN/45 is averaging 1.85 words/instruction, or about 30 bits/instruction, in the program sections where it was simulated. Whether it can maintain this average over an entire program is difficult to predict. For example, in the program "HANOI", the 11/45 hard-code accounts for 34 instructions, and 66 words out of a total size of 104 words. The KI10 version required 24 words (out of a total of 60) for the same part of the code. If we assume that the F-10 ratio of 24/60 will carry over to the 11, then the size of the 11-code for this module will be 165 words, or 2.8 times the FORTRAN-10 size!

There are a few things in the PDP-10 architecture which help FORTRAN in both speed and size considerations. A few of these are:

1. Ability to use "short" (18 bit) floating point immediate data. This helps with the simple (i.e., 1., 2.,...) floating point constants. (FORTRAN/45 does not seem to be pooling floating point literals; perhaps it should.)

2. Ability to set to 0 or -1 either a register or a memory location or both. I.e., the 11 code:

```
MOV   #-1,R0          ;A = R0 = -1
MOV   R0,A
```

   is simply:

```
SETOB R0,A            ;A = R0 = -1
```

   on the 10. FORTRAN-10 really uses this!

nb: After this memo was written, I received a copy of J. Burness' memo of 1 November on the same subject. Some of our "size" numbers differ; in general, I worked with entire modules, while Jack looked only at the hand-coded FORTRAN/45 sections. Our timings differ as well; my tests were run on CS/2 (a dual KI10) and 10-Marketing assures me my runtime includes much monitor overhead; i.e., the KI10 timings I measured are pessimistic with respect to the "real power" of the beast.

PROGRAM EXECUTION TIMES

(all times in seconds)

PROGRAM	MOP (45+FPP)	F45 (40+EIS)	F45 (40+FIS)	F45 (45+FPP)	F40 (KI10)	F10 (KI10)	F10/OPT (KI10)	DATACRAFT DC6024/5	MODCOMP ?
HANOI	184	87	87	64	64	58	27	80	230
DG3	27.7	85.3	27.2	12.5	4.9	4.5	3.7	-	-
FFT	10.3	22.9	14.7	5.6	2.5	2.1	1.8	-	-
SINGLE	12.2	65.1	13.4	5.2	3.4	2.1	2.1	11.6	9

PROGRAM SIZES

(all numbers are decimal words)

PROGRAM	MOP 45+FPP	F45 40+EIS	F45 40+FIS	F45 45+FPP	F40 KI10	F10 KI10	F10/OPT KI10
HANOI	76	66	66	104 / 66/34	55	64	60
DG3	88	130	133	295 / 104/56	127	171	175
FFT	342	433	449	? / 311/?	208	223	217
SINGLE	98	220	210	220 / 157/86	110	118	118

NOTES:

1. Sizes for MOP (45+FPP), F45 (40+EIS), F45 (40+FIS) do not include entire program, but only selected parts thereof. Comparisons between first 3 columns and last four are meaningless.

2. Notation for FORTRAN/45 (45+FPP) column is:

$$\frac{\text{total code size}}{\text{simulated F45 code/\# instructions in simulated code}}$$

3. Sizes indicated do not include variable and array storage.

/ale

digital INTEROFFICE MEMORANDUM

TO: The Little King

CC: Gordon Bell

DATE: November 1, 1973

FROM: Jack Burness

DEPT: Micro Products Development

EXT : 4902 11-2

SUBJ: FORTRAN COMPARISONS

Attached you will find two tables comparing the Fortrans on the PDP-10 and the PDP-11.

In making these comparisons, I used four Fortran programs which were previously used to estimate the performance of the "new" PDP-11/45 Fortran over the existing PDP-11 Fortran which uses threaded code. The four programs are HANOI, DG3, FFT, and SINGLE. HANOI is the standard "tower of HANOI" game, and uses integer arithmetic and arrays. DG3 is a standard Data General Benchmark. FFT is a fast fourier transform program. SINGLE is an integration program. Thus the mixture of programs may be described as "adequate". Besides, I had no desire to hand-assemble Fortran programs. The timings for the PDP-11 Fortrans were gotten from a document. The sizes and PDP-10 timings are my own. The programs were run at least twice on the PDP-10 to make sure that they were approximately correct.

I generally find such tests come up with vague answers. For example, the PDP-11 is shown to be about as bit efficient as the PDP-10, in terms of code produced. (Note: The variable sizes were not included, but literals were). This is because of the existing problems with the PDP-11. They are (once again): lack of context indexing, lack of small literals in one word, and lack of small offsets in one word. It is interesting to note that the KA10 is comparable to the 11/45 in both bits used and speed. This is due to the fact that the PDP-10 is fetching twice as many instruction bits at a time. If we went to a wider data path, the 11/45 timings might be reduced anywhere from 20% to 33%. Cache's would speed things up somewhat, but they can be added to any computer.

I would like to conclude by saying that the PDP-10 Fortran does a better job than the PDP-11 Fortran, and that accounts for a good deal of the performance of the KA10. I believe that if the programs were recoded in assembly, that the PDP-11 would gain far more than the PDP-10 would.

Jack

attached

jmc

CORE REQUIREMENT SUMMARY

The following table is a memory size comparison between four different Fortran programs. The "new" PDP-11/45 fortran was compared against the existing PDP-10 optimizing compiler. For the PDP-10, there are two major entries. The first is of the form:

num1 + num2

where num1 is the number of words of PDP-10 instructions used, and num2 is the number of off line literals used. It is necessary to include this because a good deal of the PDP-11's code includes in-line literals, and a comparison would be unfair. The second entry under the PDP-10 is the number of bits used. This is (num1 + num2) *36. This maybe taken into account, because while the PDP-10 may use less words, its words are far bigger than the PDP-11's.

The PDP-11 has essentially the same entries, except that it has one more. That is of the form:

num3 + num4

and it comes between the two previously described entries. It is merely num1 and num2 divided by 2. Since 32 (2 * 16) is almost 36, this also gives us another ballpark means of comparing the two machines. This additional entry has nothing to do with the goodness or badness of building a 32 bit eleven, and should not be construed as such. I'm merely saving the reader a mental division which he would naturally be inclined to do.

Please note that the program"FFT" has three entries. The reason for this is because there is a main program and a subroutine. The third entry is merely the total of the two.

	PDP-10		PDP-11/45		
PROGRAM	WORDS	BITS	WORDS	**WORDS**	BITS
HANOI	24+Ø	864	64+Ø	32+0	1024
DG3	54+2	2016	71+2	35½+1	1168
FFT	45+3	1728	110+2	55+1	1792
	130+1	4716	222+2	111+1	3584
	175+4	6444	332+4	166+2	5376
SINGLE	52+2	1944	119+11	59½+5½	2080

PERFORMANCE SUMMARY

The following table is a speed (i.e. CPU timing) comparison of different Fortrans on different machines. Four Fortran programs were used. The first Fortran in the table is the existing "MOP" fortran. The programs were run on a PDP-11/45 with core and FPU. The second Fortran is the "new" 11/45 Fortran. The four programs were "hand-coded" into PDP-11 assembly in the same manner as the compiler will. Thus it is really an estimate, but it should be a very good one. The third Fortran is the existing PDP-10 Fortran running on a KA10. The compiler was set to "optimize". The forth column is an estimate of the speed if the program was run on a KI10 (which I haven't been able to do because of various circumstances). The speed differential between the KA10 and KI10 was assumed to be 2. The fifth column is the expected performance of the full blown KL10, with caches, etc. It is expected to be approximately 6 times faster than the KA10.

PROGRAM	EXISTING MOP FOR.	NEW 11/45 FORTRAN	KA10 FORTRAN	KI10 FORTRAN	KL10 FORTRAN	
HANOI	184	64	79	39.5	13.2	(in seconds)
DG3	27.7	12.5	8.3	4.15	1.39	
FFT	10.3	5.6	4.31	2.16	.72	
SINGLE	12.2	5.2	5.75	2.88	.96	

M I D - H I R A N G E

P D P - 1 1 S T R A T E G Y

May 16, 1974

Bill Demmer

STRATEGY OBJECTIVES

- EXTEND AND PROTECT PRESENT BUSINESS AREAS
- INTEGRAL PART OF TOTAL DEC SYSTEMS STRATEGY
- PROVIDE FOLLOW ON PRODUCTS TO THE 11/40 AND 11/45
- COVER RANGE FROM LOWER PRICE TO HIGHER PERFORMANCE
- EXPLOIT CURRENT SOFTWARE BASE
- INCREASED PRICE/PERFORMANCE VIA MEMORY TECHNOLOGY, MACHINE ORGANIZATION, AND ARCHITECTURAL ENHANCEMENTS
- CAPITALIZE ON THESE TO MEET COMPETITION, PARTICULARLY FROM NEW 32 BIT SYSTEMS

DEC MARKET DESCRIPTION

FIRST 9 MONTHS OF FY74 NOR -

TOTAL PDP-11 FAMILY	$131M
MID - HI RANGE CONTRIBUTION	$108M
PERCENT CONTRIBUTION	83%

APPROXIMATE DEC PRODUCT LINE DISTRIBUTION

PRODUCT LINE	11/40	11/45
OEM	48%	25%
LDP	12	25
COMMUN.	17	15
BUSINESS	6	15
INDUSTRIAL	12	10
OTHER	5	10

CUSTOMER PERCEPTION OF 32 BIT MACHINES

- EMOTIONAL ISSUE - THE NEW THING THAT EVERYONE IS COMING OUT WITH.
- GREATER PRECISION.
- INCREASED THRUPUT.
- PRICE DIFFERENTIAL BETWEEN 16 AND 32 BIT MACHINES IS MINIMAL FOR GREATER CAPABILITY.
- CAPABILITY FOR LARGE INSTRUCTION SET.
- SUPPOSED TO HAVE MANY REGISTERS FOR FAST CONTEXT SWITCHING.
- SHOULD HAVE MORE SOPHISTICATED I/O STRUCTURE.
- MUST BE COMPATIBLE WITH 16 BIT MEMBERS OF SAME COMPUTER FAMILY.

M O D C O M P

SELLING STRATEGY OF MODCOMP:

"THE POWER OF A 32 BIT MACHINE FOR 16 BIT PRICE".

- SYSTEM SIZE UP TO 256K - 16 BIT WORDS.
- 16 SETS OF 16 GENERAL PURPOSE REGISTERS FOR RAPID CONTEXT SWITCHING.
- A PROGRAM DIRECTLY ADDRESSES UP TO 128K WORDS.
- DATA PATHS EXTERNAL TO PROCESSOR ARE 16 BITS.
- MULTIPROCESSOR CONFIGURATIONS VIA 4 PORT CORE.
- SINGLE AND DOUBLE PRECISION FPP.
- EXCELLENT R.T. OPERATING SYSTEM.
- PRICE ABOUT 10% LOWER THAN 11/45 (BEFORE LARGE DISCOUNTS).

I N T E R D A T A

SUMMARY OF 7/32:

- 32 BIT CPU CAPABLE OF RESOLVING 24 BIT ADDRESS.
- EACH 32 BIT INSTRUCTION FETCH REQUIRES TWO MEMORY CYCLES.
- DATA PATHS EXTERNAL TO PROCESSOR ARE 16 BITS.
- DOES NOT SUPPORT DOUBLE PRECISION FLOATING POINT.
- NOT MODULAR: 4 TYPES OF BUSSES

  SEPARATE BUS FOR EACH DMA DEVICE
- 7/32 UPWARD COMPATIBLE FOR 7/16.
- 7/32 WITH 8K CORE IS APPROXIMATELY $10K.

RUMORED 8/32:

- 32 BIT MEMORY BUS.
- SEMICONDUCTOR.

DATA GENERAL

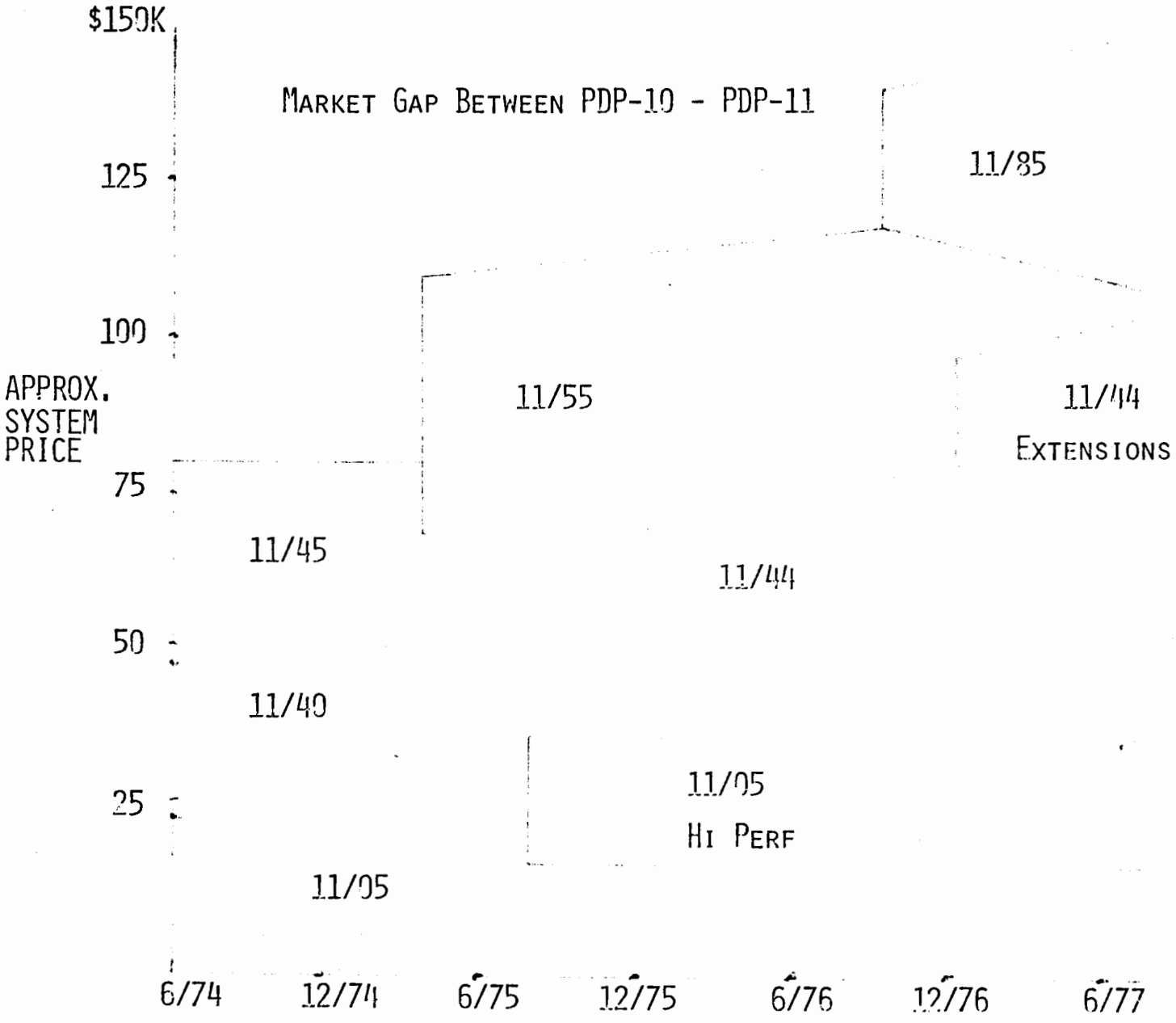
840:

- 16 BIT CPU ADDRESSES A MAXIMUM PHYSICAL ADDRESS SPACE OF 128K THRU MEMORY MANAGEMENT.

NEW 32 BIT COMPUTER:

- NEW ARCHITECTURE (E.G., NOT NOVA DESIGN)
- 200 NS CYCLE TIME - SUPPORTS CORE, BIPOLAR, MOS.
- SWITCH SELECTABLE TO USE 16 OR 32 BIT MODE.
- IS MICROPROGRAMMABLE.
- CAN EMULATE NOVA INSTRUCTION.
- GOOD FORTRAN MACHINE (WILL EVENTUALLY HAVE BASIC AND COBOL).
- WILL HAVE R.T. OPERATING SYSTEM, LIKE RSX11D.
- PRICE ABOUT 25% LOWER THAN 11/45.

PDP-11 PRODUCT STRATEGY



11/55

INCREASED SYSTEM PERFORMANCE - 11/45 PRICE

- INTERNAL CPU PERF - CACHE MEMORY HIERARCHY

  11/45 - 980 NS

  11/55 - 400 NS (2.4 IMPROVEMENT FACTOR)

- I/O THRUPUT AND BANDWIDTH

  32 BIT MEMORY BUS

  INTEGRATED MASSBUS CONTROLLERS

- PROGRAMMING THRUPUT

  EXTENDED MEMORY ATTACHMENTS -
  UP TO 2 M WORDS

  PHYSICAL MEMORY ADDRESSING -
  22 BITS

- RELIABILITY - MAINTAINABILITY

  MEMORY SYSTEM PARITY CHECKING

11/55 PLAN

STATUS

DESIGN COMPLETE

SPEC AND BUSINESS PLAN AVAILABLE

KEY MARKETING DATES

ANNOUNCE	10/74
FIRST CUSTOMER SHIP	3/75
FULL 11/55 SOFTWARE AVAILABLE	SUMMER/75

KEY ENGINEERING CHECKPOINTS

START BREADBOARD TEST	6/1/74
FIRST PASS BOARD LAYOUT COMPLETE	9/15/74
START PROTOTYPE TEST	10/15/74
SHIP SYSTEM TO PROGRAMMING DEVELOPMENT	11/30/74
LIMITED BOARD RELEASE COMPLETE	12/15/74

OUTSTANDING ISSUES

INITIAL PROGRAMMING SUPPORT

FY75 DEVELOPMENT FUNDS

B A S E 1 1 / 4 4

INCREASED SYSTEM PERFORMANCE - COMPARABLE COST WITH 11/40

- INTERNAL COST/PERF.		PERF.	FY76	FY78
11/40	16K CORE	1100NS	$2700	$2600
	32K CORE	1200NS	$2900	$2750
11/44	16K MOS	600NS	$2650	$2250
	32K MOS	600NS	$3520	$2800

- SYSTEM THRUPUT - 2 X 11/40

  4 MHz MEMORY BUS

  3 INTEGRATED MASSBUS CONTROLLERS

  UP TO 128K (4K CHIP) MEMORY

- INITIAL OPTIONS

  FLOATING POINT

  ASCII CONSOLE

- KEY MARKETING DATES

ANNOUNCE	6/75
FIRST CUSTOMER SHIP	12/75

11/44 STATUS

ALTERNATIVES UNDER STUDY

- DECEMBER WOODS MEETING OBJECTIVE - $1850 (16K MEMORY)
- MAJOR PRODUCT ALTERNATIVES

	PERF.	FY76 COST	
		16K	32K
A. 11/05 HI PERF (CORE)	1100NS	$1725	$1925
B. REDEFINED 11/44 (MOS)	950NS	$2220	$3090
C. REPRICED 11/35 (CORE)	1100NS	$2000	$2200

CURRENT THINKING

- SMALL 11 STRATEGY PRODUCT (11/05 HI PERF) SATISFIES $1850 PRODUCT NEED.
- 11/40 REVENUES SEVERAL TIMES 11/35 (5:2 BUILD RATE) AND 11/44 PLAN BEST PROTECTS THIS BUSINESS.

11/44 EXTENSIONS

FEATURES

- VIRTUAL ADDRESS SPACE EXPANSION
  DEFINITION AVAILABLE 5/74

- MULTIPROCESSING
  BUS DESIGN AND PACKAGE CONSIDERED
  IN BASE DESIGN

- USER MICROCODE CAPABILITY
  SPACE AND DATA PATH HOOKS IN BASE
  DESIGN

FIRST CUSTOMER SHIP - 12/76

MAJOR RISKS

- NEW OPERATING SYSTEM SUPPORT REQUIRED
  FOR MP AND VAS EXPANSION

- MAGNITUDE OF ECO TO INCORPORATE FEATURES

11/85

BRUCE DELAGI

11/85 - "A CHEAP 10"

WHY:
- CLEAN SOLUTION TO VIRTUAL ADDRESS SPACE PROBLEM
- VERY GOOD FORTRAN PERFORMANCE
- LANGUAGES, UTILITIES, & FILES CAPABILITIES OF DECSYSTEM 10 AT LOW COST

WHY NOT:
- MIGRATION DIFFICULTIES FOR OUR PDP-11 CUSTOMERS
- IS THERE OVERLAP WITH THE 11/44?
- WHAT IS THE PERFORMANCE OF DECSYSTEM 10 MONITORS WITH RESPECT TO:
  - SMALL SYSTEMS (E.G. 32K AND NO DRUM)
  - "REAL TIME APPLICATIONS"

MIGRATION & THE 11/85

DEC PERIPHERALS - RP04, TU16, RK06, ...
(MASSBUS AND SERIAL BUS PERIPHERALS)

USER DESIGNED INTERFACES
- OPTIONAL UNIBUS
- "DR11C" INTERFACE TO SERIAL BUS

FILES INTERCHANGE
- PHYSICAL COMPATIBILITY
- "READALL" AND "WRITEALL" TO GET ALL BITS OFF MEDIA
- "FILEX" TO INTERPRET "FOREIGN" FILE STRUCTURES
- ACCESS TO FILES OF ASCII DATA QUITE GOOD, BINARY ARRAYS FEASIBLE, MIXED DATA TYPES UP TO THE USER

PROGRAMS
- FOR NEW APPLICATIONS, WHAT OLD CODE IS MOVED

11/85 GOALS

FIRST CUSTOMER SHIP: FALL '76 AT CURRENT FY75
DEVELOPMENT BUDGET

SYSTEM MANUFACTURING COSTS: $ 19K

- 64 K WORDS OF MEMORY - $ 9.6K ($1.2K PER 8K)
- 2 - 160 M BIT SPINDLES - $ 2.2K (2 RP03 EQUIVALENT)
- CPU, BOX, AND POWER SYSTEM - $ 5.0K
- ASYNCHRONOUS LINE MULTIPLEXER - $ 0.6K (SERIAL BUS)
- TERMINAL, CASSETTE, FAX PRINTER - $ 0.4K
- FINAL (BASIC) ASSY & TEST - $ 2.5K (15%)

PERFORMANCE ALTERNATIVES (RAW SPEED)

- (1) KI (1400 NS "ADD IMMEDIATE") - $3500
- (2) 2 X KI (700 NS "ADD IMMEDIATE") - $5000

ALTERNATIVE #2 IS 1/2 OF KL-CACHE PERFORMANCE

COSTS SHOWN ARE FOR CPU, BOX, AND POWER SYSTEM

RAS - NOT YET QUANTIFIED

PERFORMANCE

RAW SPEED _ SEE ABOVE

LANGUAGE _ 2 - 3 X FASTER THAN /55 WITH FORTRAN IV PLUS
(FOR "KI PERFORMANCE" MACHINE USING FORTRAN 10)

VIRTUAL ADDRESS SPACE: 1 MBYTES

MEMORY BANDWIDTH: BUS, ON THE ORDER OF 250 NS PER 36 BIT WORD (INTERLEAVED)

PHYSICAL ADDRESS SPACE: 1 M WORDS AT 4K MOS DENSIFIES
(DESIGN FOR 16 M WORD WITHOUT CPU OR DEVICE OR CONTROLLER CHANGES)

SMALL SYSTEMS MEETING
APRIL 5, 1973
ROOM 21
PARKER ST.
TIME --- 1 PM

STEVE TILDEN
5-5 JAN 3.78
APRIL 5, 1973

FUTURE OF SMALL 16-BIT SYSTEMS REPORT

This report attempts to encourage discussion on the future direction of Digital's 16-bit small computer systems. A basic assumption is that most marketeers of small PDP-11 minicomputers are interested in pedaling an approximately identical core configurations providing the price for this standard product is competitive. For perspective, the first section of this report lists three core configurations along with their projected manufacturing cost in FY-74, the DEC list price, and the Data General list price. A breakdown of the 11/05 cost is also given.

Software is often the reason given for buying DEC small systems. Section II of this document briefly discusses the effect of the operating system on the performance of the MASS storage systems device.

Section III discusses the various options for building a more economical small systems package. The goals for a new small systems package are several:

a. Increase saleability to maintain premium price.

b. Decrease manufacturing cost to increase margin.

c. Increase volume capability to increase total dollars.

d. Increase systems reliability to decrease warrantee cost and boost company image.

Section I - Competitive Perspective

Table I-1 lists the cost and list price breakdown for the hardware components of three typical systems:

a. Disk operating system with 16K of memory and 1 RKØ5 and 1 cassette drive.

b. Dectape operating system with 8K of memory and 1 TU56.

c. Cassette operating system with 8K of memory.

Note that there is only a $1200 manufacturing cost difference between the Disk operating system and the Dectape operating system, but the list price difference is 10.6K.

Table I-2 contains a projected cost breakdown for the PDP 11/05LA 8K word computer. Note that the standard cost as of 12/5/72 was $1825. The reduction to $1401 is based on a reduction in core memory cost projected by Bob Savell in his report dated 1/10/73, reduced cost of the CPU modules of $64 due to Ø wire layouts, and slightly reduced fabrication due to the introduction of die castings. Based on present manufacturing quality, which is resulting in a less than 4% failure rate of the basic unit in Westminister as received from Puerto Rico and a reasonable parts flow, it is not unreasonable that the $1400 price will be met. The high quality is an indication that the

manufacturing procedures in Puerto Rico are being executed with reasonable precision. The November manufacturing price of the 11/05 was approximately $1900. No information from Puerto Rico yet.

The Data General prices appear to be in-line with our manufacturing cost if one considers the mark-up on the DECtape Operating System. The mark-up on the Disk Operating System is 4.25 while the mark-up on the DECtape Operating System is 3.23.

TYPICAL SYSTEMS

	Mfg. Cost	DEC Selling Price	Competition Selling Price (Data Genera
1. Disk Operating System			
PDP 11/05 w/8K memory	1401.42	6,495*	5,400
10½" Box	150.00		
TA11 plus TU60	829.26	3,900	
RKØ5	1650.00	5,100	5,000
RK11D	420.03	5,900	1,700
LA3ØS	1355.00	3,195	1,400
DD11	70.00		
H96ØCA (cabinet)	258.35	700	
861B (power control)	78.12		
MM11L w/8K memory	485.00	4,400	4,100
Systems Integration	670.00		
	$7,367.18	29,690	17,600
2. DECtape Operating System			
PDP 11/05 w/8K memory	1401.42	6,495	
TU56 (new price will be $900)	1160.00	4,700	Same
TC11	1358.00	4,000	
H96ØCA (cabinet)	258.35	700	As
861B (power control)	78.12		
LA3ØS	1355.00	3,195	Above
Systems Integration	560.00		
	**$6,170.89	19,090	17,600
3. Cassette Operating System			
PDP 11/05 w/8K memory	1401.42	6,495	5,400
TU6Ø	708.92		2,750
TA11	120.34	3,900	
LA3ØS	1355.00	3,195	1,400
Systems Integration	360.00		
	$3,945.68	13,590	9,550

* Sales price of 10½" box not yet specified.

** With new TU56...$5,910.89

Table I-1

	Standard FY74 Cost	FY74 Volume/ Year
PDP 11/05 (8K Logic)	$1,401.42	4,000 systems
CPU 2 Modules		
M7261	144.27	
M7260	146.98	
8K Memory 3 Modules (MM11L)	485.00	
Package (5¼" box)	130.06	
(10½" box)	& 50.00	
Backplane	85.00	
Console (Bezel)	6.00	
(Etch Board)	73.04	
Power Supply	121.33	
Test and Assembly	171.12	

Table I-2

Section II - Effect of Software on the System Price

The standard hardware system should be capable of running a supported operating system. The hardware and software then become building blocks both for OEMs and in-house vertical markets. The design of the operating systems grossly effects:

a. Minimum memory size

b. Minimum on-line MASS storage

c. Minimum acceptable systems device performance

As shown in Table II-1, DOS-11 requires from 3 to 5 times more on-line storage than RT-11. RT-11 supports either Dectape or RK-11 as the systems device in 8K while DOS does not support Dectape and effectively requires 16K to support the RK-Ø5.

Table II-2, copied from a report by Roger Dow dated 3/23/73, shows that a medium performance floppy disk has enough storage to support the RT-11. As of this date, there have been no experiments that indicate that the floppy is reliable as a systems device, and indeed, the 2400 bit per inch density of the MEMOREX unit is questionable. However, to discount the floppy at this time would be premature.

	RT-11	DOS
Dynamic Swapping Required to run utilities	Yes in less then 16K	Yes
Min Memory	Runs in 8K supported MASS Storage Units	Requires 16K to support RKØ5
Monitor	10K	36K
Link	.2K	8K
Macro	8K	8.5K
Edit	4K	3.25K
ODT	1.5K	2.25K
PIP	2K	6.5K
BASK	8K	
FORTRAN		86.5K
FORTRAN LIB		30.5K
Totals	35.5K	181.5K

Table II-1

SPECIFICATIONS

Composite specs are shown for low, medium, and high performance floppy disks. RKØ5(L) is a composite of the present and future product.

		Floppy Disks			Cassette (dual)	DECtape (dual)	DECpack
Parameter	Units	Low	Medium	High*	TU60	TU56	RKØ5(L)
Storage Capacity	words	40K	80K	150K	40K	128K	1200K
Data Transfer Rate	usec/wd	500	80	15	4000	200	11
Avg. Access Time	msec	2000	400	60	45sec	16sec	50ms
Rotation Time	msec	700	160	33			40
Track-Track Time	msec	80	20	5			
Drive Cost		$500	$800**	$1500	$708.92	$1160	$1650
Medium Cost		$4	$7	$15	$5	$5	$65

In general, the max access time is twice the avg. access time.

* The high performance floppy disk looks more like a disk pack, is about an inch thick, and is rigid.
**Estimated at $500

Table II-2

Section III - Development of the Standard Small System

If the assumption that a way to maximize profit is to develop a standard small system is true, then it is appropriate to propose a project plan. We should examine several alternatives which may include such extremes as a completely new architecture or just a change in pricing stradegy. For the purpose of this report, radical changes in architecture are not considered. It is also assumed that a change in price stradegy must, in some reasonably short time, be followed by at least an alteration of our production efforts. Options are listed and discussed below.

a. Change hardware only as a response to the needs of production and emphasize changes in the production procedures. This approach seems to ring of motherhood. However, there are indications that competition is beginning to offer more cost effective products in areas that we consider to be our basic market. Also, using the example of the 8B, the potential cost reduction by modern packaging techniques can reduce present costs by factors of 2 to 3. Picking up 20% to 30% in cost by better manufacturing techniques is a reasonable goal.

b. A reasonable project is to fit CPU, memory, and standard peripheral controllers into a 10½" table top or rack mount package. If possible, the MASS storage drive should also mount in the same chassis. This may be possible for cassetts or floppy disks, but unlikely for TU-56s or RK-Ø5s.

Included in the standard box might be the following:

a. CPU

b. 8K of MOS memory standard. Expansion space for 24K. For customers with powerfail requirements up to 8K CORE may be substituted for 8K of MOS.

c. MASS storage controller

d. Expansion space for 5 to 8 small peripheral type options.

A goal for the standard system package would be to reduce the cost of each component including the box, CPU, memory, power supply, console, and standard device controllers.

POTENTIAL DEVELOPMENT PROJECTS:

Backplane - A reasonable discipline might be to require all standard peripherals and memory to interface to the UNIBUS via a single double connector. This is expecially true if all or most devices are single board options. A change in the UNIBUS connections would be required, internal to the standard box because of the BUS grant problem.

Electrical Modifications.....20K

Mechanical (use ELFAB type block).....70K (20K for DIE)

Package - Die cast box with moulded supports for backplane, fan, console, etc. Possibly share tooling cost with 8B box.

Mechanical.....100K

Memory - A. Redesign of core memory to *Plessy type package.....100K

B. 8K or 16K MOS system on single module.....100K**

Peripheral Developments

A. Revive inexpensive Dectape control. Dectape control should be built on at most 2 modules for a reduction in manufacturing cost of $1000 over present control.....75K

---

* = A separate, but parallel, effort to develop mother board mounting philosophy

** = Bob Savell's report of 1/10/73 estimates 60K. Even 100K is less than 1% of anticipated sales. 500K is a more believable number.

B. Floppy Disk and control - this assumes that floppy is purchased outside for at least the first year of production.

Control.....75K

Floppy Disk Introduction.....8ØK

Power Supply

A. Use Chirper supplies as required.....10K

B. Develop special purpose power supply for minimum cost in standard package. The Chirper modularity and versatility cost dollars.....75K

CPU - The present 11/05 CPU consists of two modules which are functionally divided as shown in Table III-1. It should be noted that the serial TTY control occupies over 20% of the M7260 module A redesigned UART chould reduce the TTY control to one or two chips. The Unibus control and associated logic requires approximately 60% of the M7261 module. Five/Sixths of the Unibus controls are small scale IC's or low density MSI. The first reaction by many is to propose general purpose data path LSI chips. In fact, the data path represents only 15% of the CPU because reasonably general purpose high density IC's exist for the data path, (ie: ALU's, scratch pads, etc.). It is the irregular custom logic which requires the most volume with existing IC's.

Similarly, the UART is so general purpose that it doesn't include some of the simpler features found on the KL-11 or DC-11.

CPU Options:

1. Alter CPU design only to improve reliability, testability, and manufacturing yield. Potential cost reduction - $15 to $20 per module.

   Engineering Cost.....30K

2. Build 3 board faster 11/05

   a. Byte ops only 200-400nsec then word ops vs. present 4.8 microsec difference.

   b. Max NPR latency 3.5 micro sec. vs. 7 micro sec.

   c. All instructions speeded up by a factor of 1.5 to 2.

   d. Programmable stack limit register

   e. Hooks for EAE, etc.

   Engineering Cost.....75K

3. Simulate PDP-11 with Microprocessor..150K

   This project has a high risk of producing a product with unacceptable cost/performance ratio.

4. LSI-11 - Build special UART and bipolar LSI Unibus control and other LSI devices to reduce 11/05 type processor to a single board.

   Engineering Cost.....750K

Similarly, the UART is so general purpose that it doesn't include some of the simpler features found on the KL-11 or DC-11.

CPU Options:

1. Alter CPU design only to improve reliability, testability, and manufacturing yield. Potential cost reduction - $15 to $20 per module.

   Engineering Cost.....30K

2. Build 3 board faster 11/05

   a. Byte ops only 200-400nsec then word ops vs. present 4.8 microsec difference.

   b. Max NPR latency 3.5 micro sec. vs. 7 micro sec.

   c. All instructions speeded up by a factor of 1.5 to 2.

   d. Programmable stack limit register

   e. Hooks for EAE, etc.

   Engineering Cost.....75K

3. Simulate PDP-11 with Microprocessor..150K

   This project has a high risk of producing a product with unacceptable cost/performance ratio.

4. LSI-11 - Build special UART and bipolar LSI Unibus control and other LSI devices to reduce 11/05 type processor to a single board.

   Engineering Cost.....750K

5. PDP-11 Minus

a. Advantages

1. lower cost to LSI chips

2. faster single instruction execution speed

b. Disadvantages

1. new diagnostics and system software required.

Processor Engineering costs including

basic diagnostics.....150K

Remaining Software.....∞

Function	#Chips	
M726ØC*		
16 bit Parallel Data Path	34.7	
Condition Cores and byte Rotates	14.7	
Instruction Register	3.0	
Primary IR DECODE	9.8	
Secondary IR DECODE	5.3	
Serial line - TTY Control	19.75	
M7261F*		
Microprogram	14.42	LSI
Microprogram Branch Control	12.42	
Unibus Control	22.9	SSI
BR Arbitration Logic	6.0	
Drivers and Receivers	11.0	SSI
Slave Processor	4.0	
Stack Overflow	5.0	SSI
Int Address Detection	11.0	LSI
Power Fail & Auto Restart	8.75	SSI
Line Clock	5.17	SSI
CPU Oscillator	5.67	SSI

* Total Chip count by function is 5 or 6 dips less than actual count on module due to fragmentation and spares allowance.

Table III-1

Suggested Projects	Time Scale
1. Build small system from available parts which includes 10½" PDP 11/05, RK11D, RKØ5, TA11, and 16K memory. The 16K memory might be two MM11L's or one MM11V. The MM11V would require some power supply and backplane work.	July, 1973
2. Work with Western Digital to produce microprocessor PDP 11 and memory which mounts on one module.	24 months
3. Build 8Kx16 MOS memory on one hex module.	12-15 months
4. Build Ø5 and peripheral controllers in 8B box. Mount TU6Ø or TU56 or Floppy on box.	12-15 months
5. Serial line - multi-drop project for Tom's Terminal.	12-15 months
6. Serial Computer bus for multiprocessor and peripheral interconnection.	24-36 months
7. Floppy Disk Evaluation	?

STANDARD II

SYSTEMS PROPOSAL

B. Delagi
S. Tolcher

April 10, 1973

STANDARD 11 SYSTEMS PROPOSAL

The following PDP-11 Systems are considered to be core configurations which would be manufactured by volume production and supplied to the Market Groups in the same manner as disks or IA3Ø's are provided today. The internal goal is to decrease the manufacturing cost of our low-end systems; the external goal, particularly in the OEM area, is to increase the Digital content of the systems we ship.

I should emphasize that the RKØ5I is a device which Grant Saviers discussed as a possibility only. System #4, which has a projected ship date of July, 1975, has the greatest risk, but probably the greatest potential for major cost reduction over today's products.

MAINLINE SMALL PDP-11 SYSTEMS

System #1 - Available July, 1973

System #1 includes only standard components

	Mfg. Price
11/05 CPU in 10½" box	11ØØ
16K Core Memory	97Ø
RK11D plus RKØ5	2ØØØ
TA11 plus TU6Ø	829
BM792YB	6Ø
DD11	7Ø
FA&T	3ØØ
	$5329

Statistics of Interest

Rack Space .....26¼ inches
Additional space in box.....1 spc slot
Additional slots.....2 spc slots

****

System #2 - Available December, 1973

	Mfg. Price
System #1 minus memory	4359
16K Sense Memory	635
Reduction in FA&T	- 4ØØ
	$4594

****

System #3 - Available December, 1974

	Mfg. Price
11/05 CPU - New box with integral TU6Ø Minus console (includes System FA&T)	1195
16K MOS Memory	6ØØ
RKØ5(L)	1ØØØ
LA3Ø(L)	55Ø
	$3345

****

System #4 - Available July, 1975

	Mfg. Price
Integrated CPU - RK control electronics for RK - Serial multidrop line and serial computer bus	73Ø
16K MOS	3ØØ
Tom Stockebrand's Terminal	2ØØ
2 RKØ5I's	75Ø
FA&T	2ØØ
	$2189

System #1	July, 1973	$5329
System #2	December, 1973	4594
System #3	December, 1974	3345
System #4	July, 1975	218Ø

Step 3 cost ~ 1M from Step 2
Step 4 cost $1.2M from Step 3
Step 4 cost $1.5M from Step 2

Suggested procedure is not to do step 3...this eliminates RKØ5L in favor of a 10M word 1 sec device for low end, and RPØ5 for high end.

	Storage	Cost	Worst Case Track Access
RKØ5	25m bits	13ØØ	^ 7Ø msec?
RKØ5L	6Øm bits	75Ø	^ 7Ø msec?
RKØ5I	1Øm bits	375	^ 1sec

None of the above disks is media or program compatable

Steve Teicher

Small 11

- Proposed Schedule
- Product Specification Assumptions
- Free Association Questions

8/22/73

PROPOSED SCHEDULE FOR SMALL 11

The proposed schedule, at least for the remainder of Q1 and Q2, can be broken down into distinct tasks. All of the tasks have overlapping Start and Completion dates with design reviews scheduled at critical decision points. The tasks cannot be mutually exclusive and interactions will be necessary for success.

1. Preliminary System Specification and Product(s) Spec. (Assumptions)
   These assumptions will be distributed today and will be reviewed by September 7. The final specification of both product and system should be available by the beginning of Q3.

2. Simulation
   This task has already begun and will involve configuring a micro-processor simulator, writing and assembling the source micro-code for both the basic 11 and extended instruction set, and defining I/O flow and Unibus interface logic diagrams. The system simulator should be running with assembled micro-code by November 16, and evaluated by December 3. Note that this phase will deal only with the system as a logical unit rather than as an electrical one.

3. Design, Breadboard, and Test
   This task which should begin by November 5, will evaluate and test the actual electrical characteristics of the logic that has been simulated. It will involve building test vehicles and determining the optimal form factors for the final hardware. This task will continue into late Q3 when sample CPU chips will be available from the vendor. The chip specification will be completed by December 3.

4. Mass Storage Controller
   The design and integration of a Mass Storage Controller (Floppy Disk Controller) into the Small 11 system is in the preliminary specification phase at present. The schedule for the design, breadboard, test, simulation and integration will parallel tasks 1, 2, and 3, and a working breadboard is expected by the end of Q3.

5. Manufacturing Plan
   The specification of the manufacturing plan will be started in the second half of Q2, and will involve component, process, manufacturing and test engineering. An integrated build and test plan, including cost estimates and materials schedules, will be available for review by the middle of Q3.

6. Parallel Tasks
   A differentiation between the maximum or high end and low end Small systems will begin after the preliminary specifications are available The high and low end products will have common tasks, but may have different schedules for completion. Other parallel tasks which will not be started until early Q3 included Power Supply, Package, and a Maintenance console implimentations.

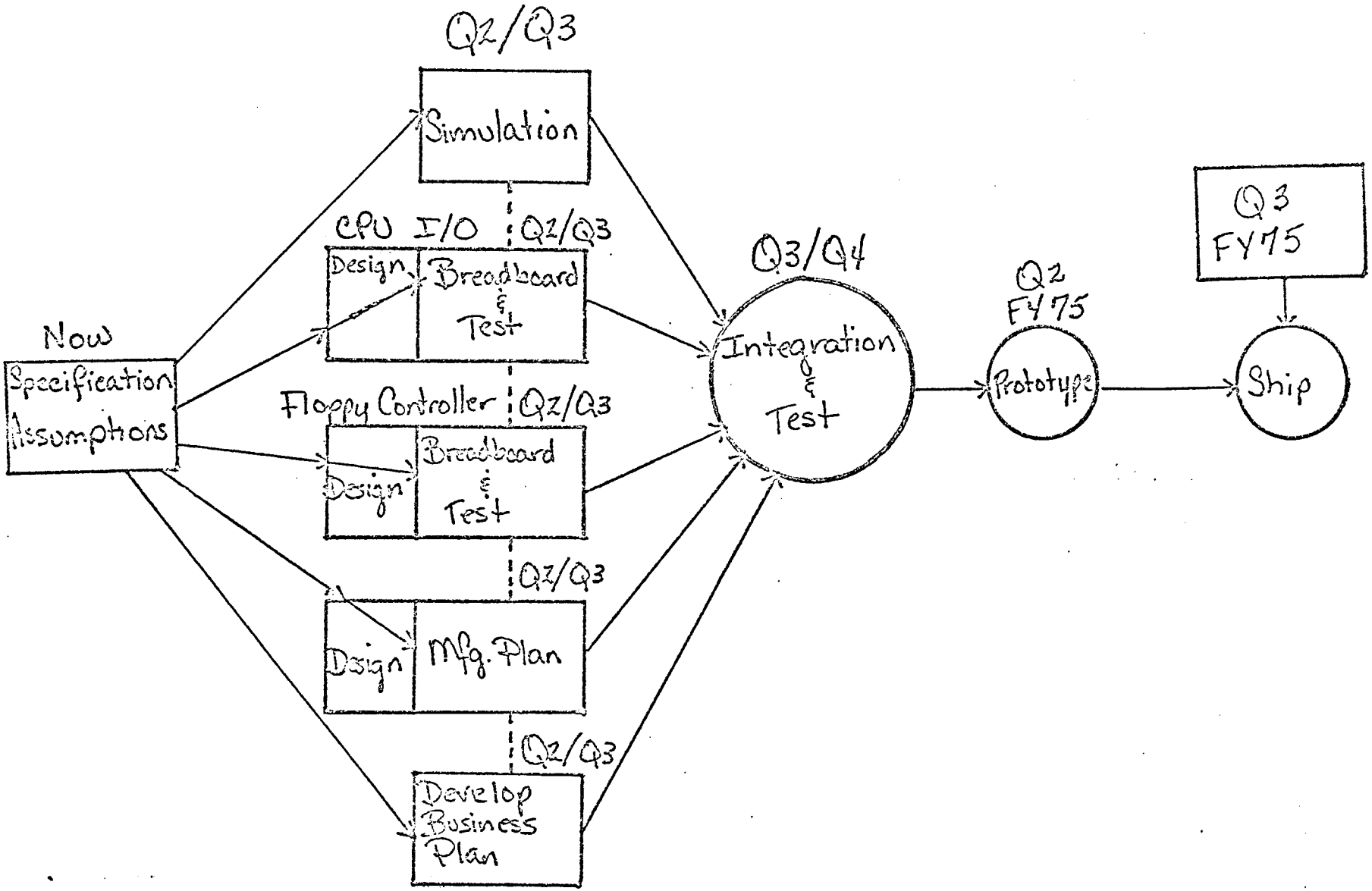
7. Business Plan

The business plan for the next Small-ll needs to be well thought out far in advance of production start-up because:

a. The potential volumes are lØ times greater than previous products that have the same function.
b. The cost, performance, and modularity tradeoffs need to be made earlier in the design cycle than for previous products.
c. The freedom to alter the product just prior to production start-up will be limited.

The product specification assumptions permit us to begin the design task with more-or-less reasonable goals. The first pass at a detailed business plan, scheduled for January 1974, will include feedback from the design efforts.

/ssb


Q2/Q3
Simulation
CPU I/O
Q2/Q3
Design
Breadboard & Test
Now
Specification Assumptions
Floppy Controller
Q2/Q3
Design
Breadboard & Test
Q2/Q3
Design
Mfg. Plan
Q2/Q3
Develop Business Plan
Q3/Q4
Integration & Test
Q2 FY75
Prototype
Q3 FY75
Ship

Product Specification Assumptions

1. Production Volume - Standard Systems 2K/month - traditional UBUS peripherals

   Small Systems 2K/month - no UBUS

   Modules 2K/month -

   6K processors/month

2. Performance - The Ø5 presently has a 300 nsec microcycle. DOS will run if microcycle increased to 400 nsec on RF disk. This says that a machine 33% slower could run standard software. This was tried with Ø5 breadboards in 1972. Tests should be rerun on Ø5 test system. We should probably modify disk driver for same system to report latency errors and measure latency errors vs. Ø5 processor speed running a large variety of programs.

   Basic assumptions without better data is that new processor will be acceptable at 70% of Ø5 speed.

3. Multiply/Divide - This feature is offered by competition and in some applications, makes up for lack of brute force processor speed. Ideally, we would like 11/40 instruction set plus EIS. Minimum acceptable is integer multiply of two 16-bit numbers. Next level would be divide a 32 bit number by 16 bit number. Next level would be multiple shifts. If EIS and FIS cannot be fully emulated, then perhaps a normalize instruction should be considered.

   Problems with multiply-divide include increased BR latency and difficulty in refresh of the memory.

4. Compatability - Ideally, any software which runs on the 11/05 should run on the new machine. Variances from this norm are positive if they include new 11 instructions found on the 11/40 or 11/45 and negative if they cause software modifications.

   There are first estimates that some operations are difficult to maintain compatable. Some of these are:

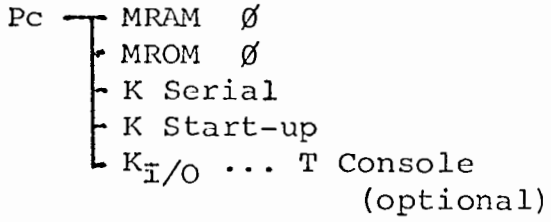
   a. Stack overflow
   b. Bus error traps
   c. Addressing of PSW and console SW register
   d. T-bit trap code additional instruction execution time

   For the minimal module, the first pass design will include no extra logic to support compatability.

For the module which has a UBUS interface, the attempt will be to maintain maximal compatability consistant with the goal of no more than a 30% decrease in performance. Duane will estimate performance using a Gibson mix or consistant benchmark.

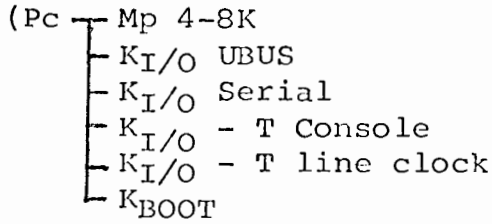
5. Configurations:

a. Minimal module -



1. Includes:
   -Processor
   -Some RAM
   -Some ROM
   -Serial line
   -Method of bootstrapping
   -Method of attaching console or maintenance terminal
2. Uses:
   -The minimal module should fit inside of the VTXY
   -The minimal module should be of some use to the communications group.
   -There should be at least a third potential use for the minimal module in some DEC product.
3. Expandability:
   -Ideally, the minimal module is a subset of bigger systems.
   -However, this constraint will not be applied for initial designs because it may be too much of a compromise.
   -As a minimum, it should be possible to add additional memory and additional serial lines to the smallest system.
   -A next level of complexity is to be able to add a Unibus interface module or peripheral other than serial lines.
4. Cost Goals:
   $200...with CPU chip price of $60.

b. PDP-11/05 Processor-Memory-Serial Line Replacement



1. Includes:
   -Processor with multiply/divide
   -4K - 8K RAM
   -Serial line
   -Line clock
   -PWR - fail
   -Console interface
   -Full UBUS interface with 4 BR levels and NPR
   -Bootstrap that eliminates need for console.
2. Uses:
   -Lower cost - replacement of 11/05 processor and memory in unit similar in function to presently sold machine

3. Expandability:
   -Mos Memory should be expandable on the WDC bus
   -Core memory and other peripherals should fit on the UBUS.
   -Maximum memory size will be 28K.
4. Cost Goals:
   Module with 4K-$450
   Module with 8K-$540
   } Assume $60 price for CPU and $6 price for 4K RAM

   Systems including box and $800 power supply w/o console.

c. Small System - Pc
   - Mp 4-8K
   - Ms Floppy
   - $K_{I/O}$ Serial
   - $K_{I/O}$ UBUS
   ETC.

1. Includes:
   -Everything in item B plus floppy disk control and drive.
2. Uses:
   -Low entry standard system in traditional market place.
3. Expandability:
   - Same as item B
4. Cost:

Item B	$800
Floppy Control	$200
Floppy Drive	$250 - $500
	$1250 - $1500

/ssb

Free Association Questions That May Arise Concerning the Next Small-11

1. In the trade-off of speed for cost, what is the shape of the curve and what is the lower limit where the performance is so poor that the product that we sell is only marginally useful? It is possible that we could get some indication of this when we modify the Ø5 lab system to run slow. We also need to examine the upper end of performance that will be available because of other technologies.

2. Can we live with some incompatability in the area of I/O? For instance, I assume that the low speed reader is a thing of the past. Some other KL-11 features may not be required.

3. Should the WDC bus be extended off the board? In other words, should we encourage the use of the WDC bus for peripheral controllers?

4. Should we concentrate any effort on the design of UBUS interface chips? This project has seemed to be secondary to our other efforts. Perhaps we should spend more time on the design of serial interface chips. A neat thing would be a UART type chip which sends and receives "transparent ASCII".

5. Should we spend time attempting to add features such as:

   a. Multiply/divide,
   b. Floating-point,
   c. Transcendental functions,
   d. FFT,
   e. Etc.?

6. Potential uses exist for multiple CPU's on the same bus. For instance, a second CPU could be used as a "channel controller" for peripherals or as a I/O multiplexer. Presently the addition of a second CPU requires some rather fancy control logic, but it may be possible given that we know something about the phase of the CPU clock. Some questions are as follows:

   a. Is the bandwidth to memory sufficient that a second CPU does not slow the system down to unacceptable performance?
   b. Should the microprogram of the 2nd or nth CPU be specialized for the task at hand?
      1. What is the criteria for deciding when a CPU should be specialized?
      2. Can the special microprogram be contained in an additional control chip?

7. While thinking about item 6b, I realized that the addition of a 2nd control chip enables one to think of a shift mode instruction which enables the entire instruction set to be interpreted in a completely

different manner by the second control chip. This would work similar to the way in which we originally visioned the control for the GT4Ø before it was decided that this device be a Unibus option.

8. What is the relationship of the CPU and mem and serial I/O on a module vs. the PM module of Jim O'Loughlin's? In fact, if the new 11 module is pinned for the SPC slots, it might replace the PM module directly. Is this goal worth giving up easier repair? What does the PM give up to be SPC compatable?

9. What are the estimated power supply requirements in terms of voltages and currents? Is it possible to generate new MOS voltages from our existing supplies with an on-the-module converter? Is this economic?

10. How important is battery backup? Should the power to the memory be separated such that it may be powered at a reduced refresh rate for long periods of time by a small battery? Should this battery be mounted on the module? How long is an acceptable storage time? Should we use fast recharge NICADS?

11. A very neat presentation for the Disk Woods Meeting was cost-per-bit vs. time with total storage volume as a parameter. What are similar measures for small-11 system that graphically illustrate value of product?

    a. cost/system vs. time with instr/sec as a parameter.
    b. cost/system vs. time with # wds/file access as a parameter.

12. For the very high volume OEM, the utmost in modularity is for him to buy chips. At that point, we are not very competitive even if we sell WDC chips because:

    a. Very little use is made of our capital investment.
    b. We don't know how to sell chips. There are a completely different set of problems associated with chip pedaling that we have not yet faced and that chip vendors understand fairly well.

    How modular does the system have to be to get the bulk of the higher profit OEM minimal system business? In fact, is there significant minimal system business or is this really a dream? I suppose some feedback will be received from the PM project although, I am not convinced that this is a major effort so far. The PM project goal is almost two orders of magnitude lower in volume than the small 11 plan.

13. What questions would I ask if I were a DEC customer considering the purchase of this new device?

    a. Can it do my job with a reasonable safety margin?
    b. What is the minimal piece that I have to buy to do my job?

c. How is this minimal piece expanded? Do I throw it away or can I add chunks as I need them? What is the effect of adding chunks on my software?

d. What tools does DEC provide for both software and hardware development?

e. What are the provisions for maintenance of both DEC hardware and the unique stuff that I add?

f. If I integrate the system from the module level, how does the DEC system compare in convenience with modules or integrated circuits from other companies? In my last job, I decided to build my own modules from TTL-MSI rather than use the logic products stuff. Criteria:

1. Does the DEC approach simplify my components testing? By how much?
2. Do I still have to buy a significant number of components even if I buy the DEC modules?
3. Does the DEC approach reduce my systems cost?
4. Does the DEC approach reduce my time to market?
5. Does the DEC approach enable me to take advantage of modern technology? The last time I considered DEC modules, they were a hinderence in the use of MSI and the DEC connector appeared to be less efficient than several other alternatives. It appeared to me that DEC was encumbered by history.
6. How much do I believe the story that DEC insulates me from the IC vendor? DEC pays the IC vendor less than distributor price and charges me more. Would not the IC vendor actually prefer to sell parts to me through the distributor.
7. If I buy IC's and build my own system, I can second source most parts. Is DEC dependable enough to do without a second source? Do the DEC patents insulate them from the competitive market to an extent that they are sluggish in the development of cost performance effective products.
8. Can I make use of the DEC design discipline by reading their literature and still save money by building my own stuff?
9. Other issues include training, documentation, and consultant availability.
10. Can I trust DEC to deliver reliable modules and eliminate inspection, or do I just trade IC inspection for module inspections?

g. The DEC salesman explains that the higher DEC prices are due to the cost of our field service and software support which I don't plan to use. Is this insurance worth the price? Can I expect to remain competitive if my supplier, DEC, believes that they must always charge a premium even though their manufacturing cost is probably lower than their competition.

h. It is already evident that DEC is no longer the technology leader in the small machine market. Is this because DEC is wisely conservative or because DEC is sluggish?

14. More questions about modules:

a. What is the absolute minimum number of chips required using the WDC chip set that puts some RAM, some ROM, a serial line, and some way of starting up the system on a module?
b. What is the minimum that I must add to a. to enable the expansion of the system to include more serial lines and more memory, but no other service?
c. How big is a Unibus interface that optimizes the performance of our standard devices with the WDC chips? Will it be possible to run standard UBUS mass storage devices? Will communication options work? Are there any devices that won't work?
d. What is the most effective form factor for modules? A better way to ask this question might be--What is the effect of form factor on the product?

Form factor effects:

1. Testing - module and systems level
2. Assembly cost of module and systems
3. Repair cost in factory and field
4. Modularity - flexibility
5. Reliability
6. Environmental tolerance
7. Design time of printed circuit board
8. Mechanical assembly cost
9. Connector cost.

/ssb

Task Group B - Engineering Related to implimenting a cost reduced replacement for the present PDP-11/Ø5

1) Small 11 Engineering - Mike Titelbaum, Duane Dickhut, Al Marsh

2) Manufacturing Engineering - Ron Cajolet, Dave Widder

3) Test Engineering - Art Berner, Joe Zeh

4) Mech. Engineering - Dave Nevala

5) P.S. Engineering - Paul Rey

6) Board Shop - Les Goldman

Task Group C - Associated Groups necessary to ensure that product is successfully placed in Manufacturing

1) Small 11 Engineering - Mike Titelbaum, Duane Dickhut, Al Marsh

2) Drafting/Layout - Roger Pothier

3) New Products - George Bundy

4) Tech Pubs - Roy Clark

5) Production - Ron Marchetti
6) Central 11 Engineering

The above groups have been logically divided into areas with respect to the immediacy of their task completion and by the detailed intercommunication that must exist for task success. This task division coincides with the attached project schedule which is attached for your review and comments.

Also attached is a milestone schedule prepared by Western Digital Corporation which culminates in the delivery of twenty CPU chip sets. It is attached for reference purposes and may possibly change if the dates are found to be unattainable. The dates will only be changed by mutual agreement of Western Digital and Digital Equipment communicated by Mike Torla.

/alw

THIS PACKAGE CONTAINS THE FOLLOWING INFORMATION:

	ITEM	AUTHOR
1.	MINUTES OF 9/5 MEETING OF THE 11 HARDWARE PRODUCTS COMMITTEE	BRUCE DELAGI
2.	CHANGES TO THE SMALL 11 HARDWARE PLAN	STEVE TEICHER
3.	10½ INCH BOX STUFF	BOB ARMSTRONG
	REPLACING BA11D CHASSIS	JOHN BUZYNSKI
	10½ INCH BOX SCHEDULE	
	PDP-11 SPACE/POWER SURVEY	
4.	11/05L SECTION	MIKE TITELBAUM STEVE TEICHER
5.	Small 11 Support Budget	Bob Armstrong

NEXT MEETING OF THE 11 HARDWARE PRODUCTS COMMITTEE WILL BE:

MONDAY, 9/17/73, 9 AM, PK3-2, STAN OLSEN'S CONFERENCE ROOM

INTEROFFICE MEMORANDUM

TO: Distribution
cc: John Swanson
Rob VanNaarden

DATE: 10 September, 1973

FROM: Bruce Delagi BD

DEPT: 11 Engineering

EXT : 3563

SUBJ: Minutes of 9/5 Meeting of the 11 Hardware Products Committee

Next Meeting will be 17 September at 9:00 am in the PK3-2 Conference Room. (Stan Olsen's conference room)

1. Irwin Jacobs and Robin Frith were absent.

2. The agenda for the next meeting will be:
   a) small machine budget and project overview - S. Teicher
   b) 16K sense and 10½" box business plan - R. vanNaarden
   c) Min 11: goals (why best), method of establishing specification, backup strategies for identified risks - S. Teicher

3. Agenda for the 1 October meeting will be:
   a) large system plans - Len Hughes
   b) List of products, product managers, project plan dates - B. Delagi

4. Agenda for the 8 October meeting will be:
   a) Standard system business plan - J. Swanson, E. Kramer
   b) Field Service Documentation - C. Spector (with help from J. Swanson, L. Hughes, H. Long)
   c) Communications (Shared Projects) Plan - Don Alusic

5. A clarification of our charter: All major changes in project business plans with respect to specifications or schedule should be reviewed and approved by this group (and passed to the Corporate Products Committee for their okay).

6. We invited Lorrin Gale to be a member of this group on the grounds that he would shortly be responsible for a major piece of the 11 product strategy. Dave Stone voiced objection that: 1) the scope of the committee would become too large; 2) the 4 hardware engineers in the group would spend all the air time discussing gates, nanoseconds, and other irrelevant esoterica.

Others in the group shared the second objection. Resolution was that Lorrin would become a member but that technical issues should always be discussed in some other forum and boiled down before being brought here.

7. Bruce presented a budget overview:

Income

TAX on 11 NOR	$4800 K
Dick Clayton Spec. Tax	500 K
Dick Clayton Spec. Proj.	200 K
98# (Tax on Corp.Nor)	60 K
	$5560 K

Outgo

Development		$2447K
Small Systems (RK, TA finish, Min 11)	$441.5K	
Standard System	146.7K	
Medium Computers (Massbus, 11/XX)	783.1K	
8K Core on a Hex	99.0K	
Communications (Synchronous Line units)	372.4K	
Reliability	604.1K	
	2446.8K	
Support		$3213
Cost of goods	$1100K	
Other support	2113K	
	$3213	
		$5660K

Changes in this budget will have to be made if

a) we continue at our current pace with WDC (original plan called for slower development)

b) We develop the 10½" box version of the 16K sense memory (currently in progress).

Len Hughes will discuss the impact of a $150K budget reduction in his area as part of his presentation on large 11 system developments on 1 October.

8. Charlie Spector will discuss whether there is sufficient budget and manpower now allocated to 11/40 support with Steve Teicher, and if he feels there isn't, he'll come back to this group with a recommendation of what project to cut (stop or delay) or where to get the money from.

9. A list of projects, product managers, project managers, project plan due dates as currently known is attached.

Distribution List:

Don Alusic, 5-3
Gordon Bell, 12-1
Dick Clayton, 5-2
Bruce Delagi, 1-2
Robin Frith, 5-2
Bill Hanson, 1-4
Len Hughes, 1-2
Irwin Jacobs, 5-3
Andy Knowles, 5-2
Ed Kramer, 5-5
Bob Lane, 5-3
Phil Laut, 12-1
John Leng, 5-5
Bill Long, 5-2
Julius Marcus, 5-3
Joe Meany, 5-2
Gerry Moore, 5-3
Bob Puffer, 1-3
Charlie Spector, 5-5
Dave Stone, 12-2
Steve Teicher, 1-3
Bob Thompson, PK3-2
Brad Vachon, PK1
Jerry Witmore, PK2

/jlu

CHANGES TO SMALL-11 HARDWARE PLAN

During Q1, the management focus of 11-Engineering has been on understanding the needs of the low-end, 16-bit market. We are still lacking a great deal of data, and there is a debate on even which questions to attempt to answer. We are motivated to understand the market because:

A. New technologies available to our competitors seems to enable them to encroach further into our market.

B. There is a strong feeling, as yet unsupported by finantial evidence, that investments by DEC in these same technologies may enable us to develop new markets which are much larger in units and total dollars than our present sales base while, at the same time, protecting our market share.

In addition to the above, we have finally decided to solve some of the problems that have been facing us for at least the past year. A specific example is the new project that we have initiated for mounting the 16K sense memory in a 10½" chassis.

Task Changes

The additional planning coupled with fate and some data, have produced changes in the charter of our group. The original 11 Hardware Plan, on which the budget was based, was prepared by Bruce Delagi and discussed in April, 1973. At that time, there was no indication that we would be able to build an LSI-11 for delivery in FY75. There was also very little pressure to mount the not yet tested 16K sense memory in our 10½" computer boxes. The Floppy Disk had specifically been rejected as a Digital product in the near future. Now, let's examine the present status:

A. We are within days of signing a contract for an LSI-11 chip set which may provide us with an 11/05 replacement as early as Q2 of FY75 and, more likely, by Q3 of FY75. In fact, as most of you know, we are already proceding with the vendor as if the contract has been signed.

B. We are proceding with a project that has a dual goal of enabling the use of the new 16K sense memory in a 10½" chassis and of providing a more useful 10½" expander box than the present 11/35 package. Strong motivation for this effort arises from the Data General announcements of June.

C. The Floppy Disk has become a must product. In fact, to my knowledge, the only widely discussed business plan for all of our new Small-11 projects was produced by Mike Tomasic for the Floppy Disk.

Resources have thus far been shifted rather than added:

In fact, we have been unsuccessful in staffing to fulfil the original requirements. This failure is entirely due to our own lack of emphasis on recruiting, and in no way due to any corporate red tape or other typical excuse. We are becoming more aggressive and I believe that we will be fully staffed early in Q2. However, we have had to shelve at least two projects, and I forsee very little possibility for reviving them in our group during FY74. In order to revive them anywhere would require a reallocation of budget because as this report will show, the increases mor than use up the resources saved by the shelved projects.

Cancelled Projects:

A. Single Module EAE - This was to have been a single hex module replacement for the KE11A which now occupies an entire system unit or 4 Quad modules. The staff for this project has been assigned to the 10½" box project.

Pros	Cons
1. Several large volume OEMs such as Tektronix (150 machines/yr) wanted it.	1. Odds are 3 to 1 that a program compatable KE11A would not fit on a hex module using standard MSI logic.
2. It might be a good thing for the lab market.	2. As the 11/35, 11/40, and 11/45 and even the new Small-11 have their own integral equivalent to the KE11A, the single module EAE would only sell with the 11/05 and as add ons to the 11/20.
	3. The present KE11A fits into the 10½" 11/E10 and will work with the 5¼" machines with the KE mounted in a BA11ES.

B. Unibus Chips - These chips were to have replaced the common part of most peripheral controllers. A justification for this project is contained in an 8/23/73 Roger Cady memo entitled "Background Data on Product Costs". Exhibit 2 from Roger's memo is attached to this document. The resourses for this project have been assigned to the 11/05L.

Changes to Small-11 Hardware Plan

Pros	Cons
1. These chips would reduce the board area required to interface to the Unibus.	1. They might not reduce the cost of interfacing to the Unibus. 2. They would not fit into existing device controller designs and the rate of development of new Unibus peripherals is reasonably low at this point in time. 3. It is not at all obvious that it makes sense to redesign existing controllers to use the new chips.

Please understand that I am convinced that the above projects should have been cancelled anyway. Someone else may have a different list of PRO's.

Altered Projects

A. Prom Reliability - This project was probably budgeted larger than necessary. In addition, we should now examine reliability studies by significant vendors. I believe that these studies can be verified for a low price.

B. Support Group Changes - Our support group has picked up the responsibility for maintaining the 11/35 and 11/40. Even though we also acquired the budget and project manpower, an additional task was placed on our support management.

Summerized Changes for Spending Plan (dated 8/16/73)

Project	Q1	Q2	Q3	Q4	Total
Single Board EAE	--	(10.2)	(27.0)	(32.3)	(69.5)
Unibus Chips - Project never budgeted by Quarter. Shown in April plan as 114K, but not shown as a savings because not included in budget print out dated 8/16/73.					
PROM Reliability - Actual cost of PROM Reliability will be 10K in Q3. Most of this will be spent with a test lab to evaluate the vendors report	--	(8.6)	--	(19.8)	(28.4)
Analog Support	--	5.0	5.0	5.0	15.0
Small-11 (11/05L)	(1.5)	19.2	66.1	49.0	132.8

Project (con't)	Q1	Q2	Q3	Q4	Total
New 10½" Box	--	56.7	48.6	16.0	121.3
Total...	(1.5)	57.1	87.7	12.9	171.2
Floppy - The evaluation project was budgeted at 40K. Without a schedule, my rough estimate is that the control should be budgeted at 100K.					60.0
					231.2

Comments on Spending Plan

The total spending plan for the Small-11 shows a tremendous growth from Q1 to Q2.

	Q1	Q2	Q3	Q4	Total
Small-11	31.0	112.5	168.0	186.5	498.0

Part of this is due to a 50K charge to the vendor. The remainder is made possible in large part due to the resources freed up by the cancellation of the 8B. It should be quite clear that it would have been difficult to build the 8B and the new Small-11 in parallel. However, we have now gone from famine to feast on service group support.

The spending plan for the 10½" box is also hard to believe. However, the project personnel has been bootlegged during Q1. In fact, the Q1 project staff consisted of several high cost consultants.

The Floppy project plan has not been established because the drive project engineer has not been chosen. I did estimate the 11-controller cost at 100K, but this cannot be scheduled by quarter without the drive project schedule.

/ssb

*Includes 11/05 backplane and ECO's to 11/05 and 11/35

SPENDING PLAN (See reverse side for detail description)

DISCRETE PROJECT New 10½" Box | 2 | 0 | | 0 | | 7 | 5 | 6 | 9 |

$ = 000 omitted ie.5600=5.6 ie.500=.5 ie.5000=5.0 ie.Amounts less than $100 are not acceptable

		CC #	Act. Code		FISCAL YEAR				
					Q1	Q2	Q3	Q4	Total
Model Shop	Tays*	324	E						
Design Drafting	Tays*	325	E		1.0	5.0	5.0		11.0
Information Services	Tays*	327	E				3.0	3.0	6.0
DEC System 10 Sftwr. Eng.	Conklin	341	E						
Small Systems Sftwr. Eng.	Ellson	342	E						
Application Software Eng.	Cohen	343	E						
PDP-11 Software Engineering	Stone	344	E						
Diagnostic Engineering	Horovitz	345	V						
Research and Devel. Group	Bell	346	E						
A/N Display Development	Doane	303	E						
DEC 10 Product Planning	Fagerquist	304	E						
Medical Systems Engineering	Segal	305	E						
eset 11 Software	Lane	306	E						
Typeset 8 Development	Fiore	307	E						
Mechanical Engineering	St. Amour	330	E			2.0	3.0		5.0
Electrical Mfg. Eng.	Cudmore	331	E						
Mechanical Mfg. Eng.	St. Amour	332	E						
PDP-11 Communications	Stockebrand	349	E						
Logic Products Engineering	Moffa	357	E						
PDP-10 Engineering	Wilhelm	359	E						
Software Distribution Center	Mullane	365	E						
Traditional Product	Milton	376	E						
PDP-11/45 Engineering	Delagi	378	E				2.0		2.0
Disk Engineering	Saviers	379	E						
Printer - Paper Tape Eng.	Corell	383	E						
Magnetic Tape Engineering	Lawrence	384	E						
Special Projects	Puffer	386	E						
DEC System 10 Center	Gwinn	390	E						
Memories Power Supplies	Savell	392	E			4.7	1.4		6.1
Print Shop	Dombrowik	550	N			1.7			1.7
Test Equipment Engineering	Cudmore	360	E						
Acton Labs	Vendor						3.0		3.0
Small-11 Engineering	Teicher	395				26.0	24.2	10.0	60.2
New Products		329				8.0	15.0	3.0	26.0
Contingencies		399	G						
TOTAL					1.0	47.4	56.6	16.0	121.0

*Manager has more detailed planning form which can be used to develop these line items.

SPENDING PLAN (See reverse side for detail description)

DISCRETE PROJECT Small-11 (FY-74) | 2 | ø | ø | 7 | 5 | 2 | 6 |

. = 000 omitted ie.5600=5.6 ie.500=.5 ie.5000=5.0 ie.Amounts less than $100 are not acceptable

		CC #	Act. Code		FISCAL YEAR Q1	Q2	Q3	Q4	
Model Shop	Tays*	324	E				4.0	4.0	8.0
Design Drafting	Tays*	325	E				8.0	16.0	24.0
Information Services	Tays*	327	E						
Field Service New Prod Ztns		73W				3.0	3.0	6.0	12.0
DEC System 10 Sftwr. Eng.	Conklin	341	E						
Small Systems Sftwr. Eng.	Ellson	342	E						
Application Software Eng.	Cohen	343	E						
PDP-11 Software Engineering	Stone	344	E						
Diagnostic Engineering	Horovitz	345	V			8.0	8.0	8.0	24.0
Research and Devel. Group	Bell	346	E						
A/N Display Development	Doane	303	E						
DEC 10 Product Planning	Fagerquist	304	E						
Medical Systems Engineering	Segal	305	E						
eset 11 Software	Lane	306	E						
peset 8 Development	Fiore	307	E						
Mechanical Engineering	St. Amour	330	E			3.0	9.0	9.0	21.0
Electrical Mfg. Eng.	Cudmore	331	E			3.0	3.0	3.0	9.0
Mechanical Mfg. Eng.	St. Amour	332	E						
PDP-11 Communications	Stockebrand	349	E						
Logic Products Engineering	Moffa	357	E						
PDP-10 Engineering	Wilhelm	359	E						
Software Distribution Center	Mullane	365	E						
Traditional Product	Milton	376	E						
PDP-11/45 Engineering	Delagi	378	E						
Disk Engineering	Saviers	379	E						
Printer - Paper Tape Eng.	Corell	383	E						
Magnetic Tape Engineering	Lawrence	384	E						
Special Projects	Puffer	386	E						
DEC System 10 Center	Gwinn	390	E						
Memories Power Supplies	Savell	392	E		2.1	12.1	23.0	23.0	60.2
Print Shop	Dombrowik	550	N						
Small-11 Eng *	Teicher	395	E		21.0	59.0	74.0	84.0	238.0
Hardware Software Tools	McCarthy	34A			2.5	11.3	10.0	7.5	31.3
Process Engineering	Cajolet	339			2.4	8.0	8.0	8.0	26.4
I [illegible] Engineering	O'Connor	360				2.1	12.0	12.0	26.1
New Products		329				3.0	6.0	6.0	15.0
TOTAL					31.0	112.5	168.0	186.5	495.0

*Manager has more detailed planning form which can be used to develop these line items.
Increases in Q2, Q3, & Q4 are partly due to vendor payments.

DEC 1-(637)-1338-N373

Small-11 Manpower Budget FY-74 (Assumptions)

	CC		1 M	1 $(K)	2 M	2 $(K)	3 M	3 $(K)	4 M	4 $(K)	5 TOTAL $(K)	6
1	324	Model Shop										1
2		?50/Model	-		-			4.Ø		4.Ø		2
3		100 Model										3
4		+ Prod. Model										4
5								4.Ø		4.Ø	8.Ø	5
6												6
7	325	Design Drafting										7
8		Draftsman 1	-		-		.5	2.Ø	1	4.Ø		8
9		Draftsman 2	-		-		.5	2.Ø	1	4.Ø		9
10		Layout 1	-		-		.5	2.Ø	1	4.Ø		10
11		Layout 2	-		-		.5	2.Ø	1	4.Ø		11
12							2	8.Ø	4	16.Ø	24.Ø	12
13												13
14	329	New Products										14
15		Eng. 1	-		.5	3.Ø1		6.Ø	1	6.Ø		15
16					.5	3.Ø1		6.Ø	1	6.Ø	15.Ø	16
17												17
18	33Ø	Mech. Eng.										18
19		Eng. 1	-		.3	3.Ø1		9.Ø	1	9.Ø		19
20					.3	3.Ø1		9.Ø	1	9.Ø	21.Ø	20
21												21
22	331	Components Eng.										22
23		Eng. 1	-		.5	3.Ø	.5	3.Ø	.5	3.Ø		23
24					.5	3.Ø	.5	3.Ø	.5	3.Ø	9.Ø	24
25												25
26	339	Process Eng.										26
27		Mfg. Eng. 1	.3	2.41		8.Ø1		8.Ø	1	8.Ø		27
28			.3	2.41		8.Ø1		8.Ø	1	8.Ø	26.4	28
29												29
30	34A	Software Eng.										30
31		Feshkens	.3	2.51		7.5	.3	2.5	-			31
32		Programmer 1	-		.5	3.81		7.5	1	7.5		32
33			.3	2.51	.5	11.3	1.3	10.Ø	1	7.5	31.3	33
34												34
35	345	Diagnostic Prog.										35
36		Eng. 1	-		1	8.01		8.0	1	8.0		36
37					1	8.01		8.0	1	8.0	24.Ø	37
38												38
39												39
40												40

9/6/73

Small-11 Manpower Budget FY-74 (Assumptions)

	CC		1 M	1 $(K)	2 M	2 $(K)	3 M	3 $(K)	4 M	4 $(K)	5 TOTAL $(K)	6
1	36Ø	Test Engineering										
2		Eng. 1	–		.3	2.11		7.Ø1		7.Ø		
3		Tech. 1	–		–		1	5.Ø1		5.Ø		
4			–		.3	2.12		12.Ø2		12.Ø	26.1	
5												
6	392	Memorics/Power										
7		Supplies										
8		P.S. Eng. 1	–		.3	2.11		7.Ø1		7.Ø		
9		P.S. Tech. 1	–		–		–	.5	3.Ø .5	3.Ø		
10		Mem. Eng. 1	.3	2.11		7.Ø1		7.Ø1		7.Ø		
11		Mem. Tech. 1	–		.5	3.Ø1		6.Ø1		6.Ø		
12			.3	2.11.8		12.13.5		23.Ø3.5		23.Ø	6Ø.2	
13												
14	395	Small 11 Sys. Eng.										
15		Titelbaum	1	7.Ø1		7.Ø1		7.Ø1		7.Ø		
16		Dickhut	1	7.Ø1		7.Ø1		7.Ø1		7.Ø		
17		Marsh	1	7.Ø1		7.Ø1		7.Ø1		7.Ø		
18		Q2 Eng. (2)	–		2	14.Ø2		14.Ø2		14.Ø		
19		Tech. 1	–		1	6.Ø1		6.Ø1		6.Ø		
20		Tech. 2	–		.5	3.Ø1		6.Ø1		6.Ø		
21		Q3 Eng.	–		–		1	7.Ø1		7.Ø		
22		Materials				15.Ø		20.Ø		3Ø.Ø		
23			3	21.06.5		59.Ø8		74.Ø8		84.Ø	238.Ø	
24												
25	73W	Field Service										
26		F.S. Eng. 1	–		.5	3.Ø .5		3.Ø1		6.Ø		
27					.5	3.Ø .5		3.Ø1		6.Ø	12.Ø	
28												
29												
30												
31												
32												
33												
34												
35												
36												
37												
38												
39												
40												

INTEROFFICE MEMORANDUM

TO: Gordon Bell
Andy Knowles
Dave Nevala
Ken Olsen
Joe St. Amour
PDP-11 Hardware Products Committee

DATE: September 7, 1973

FROM: Bob Armstrong

DEPT: Small Systems 11 Engineering

EXT : 4186

SUBJ: Replacing the BA11-D Chassis

A series discussions have occurred recently regarding the reasons for, and requirements of a new 10½" chassis (and/or power supply) to replace the existing BA11-D. Although the BA11-D is now being shipped in the form of 11/35 and 11/05 CPU's, there are several requirements which it doesn't meet.

1. It doesn't contain voltages necessary to power the new 16K memory (MM11-U).
2. Due to current limitations, there are severe restrictions over what can be configured in a single box. For this reason, it is not being shipped as a PDP-11 expansion chassis.

The intent of this memo is to provide some continuity for our decisions to this point and the future.

We surveyed the space necessary to provide a reasonable system versus the power required for its worst case configuration. Using existing parts, 4 system units would never provide a salable product without an expansion chassis. Six system units provides a powerful system, but requires configuration rules due to insufficient power with worst case loading. Five system units satisfies both requirements as a sufficient stand-alone system with the capability of powering any combination of peripherals with a reasonable (and possibly, coolable) amount of power. Pertinent data from these surveys are provided.

Having chosen the space requirements and approximate power consumption, we have several alternatives in packaging the system.

1. New supply in existing chassis - The new supply could either be a total new design or repackage of existing regulators.
2. New chassis with existing regulators.
3. DEC standard system packages.

We have discussed with various committees, the problems and advantages of using the proposed standard boxes. It appears now that there is no way for us to both meet our system unit and power requirements as well as shipping product in a minimum time using that box. Between chassis and power supply design, we feel that redesigning the mechanical package would provide a superior product for several reasons:

1. Length of design cycle - committment to redesign the supply would give us product to ship in 9 - 12 months, whereas, mechanical redesign yields 6 - 8 months.
2. Development innovation and experience - design of a new supply would provide no significant improvement over existing ones unless new technologies are used. There is a project designing new technology supplies, but with no firm product release date. We can make use of the experience gained through cooling the existing box as well as many of the new ideas in tooling, card guides, module handles, etc. gained so far in work on the standard box.
3. Standard pieces - a new supply would be an additional part which would have to be built and spares stocked in the field. Typically, the mechanical chassis is not stocked, and would provide little effect on field service. We also hope to use the new standard power distribution harnesses (11/40, 11/45) to ease system assembly and field add-on orders.

   Our plan now is for 11 Engineering to design a new chassis that will accept the existing building-block regulators used in the PDP-11/40 and 11/45. The new box will replace the BA11-D for the 11/35 and 10½" 11/05 and replace the BA11-ES as the PDP-11 10½" expansion chassis capable of accepting HEX modules. It will remain independent from future corporate standard boxes.

The two main questions still remaining for this, or perhaps any box, are cooling and cabling. Both of these should be answered upon completion of a prototype chassis and air flow measurements.

Future tasks will be as follows:

1. John Buzynski will issue an Engineering schedule and budget to allow design of a reliable, producable product.
2. Charlie Valliant will continue his box design with help from Dave Nevala where necessary, and build a prototype as soon as feasible. Tests including flow measurements, system configuration problems, power distribution, cabling, etc. shall be performed according to a written and distributed test plan.
3. All of us connected with the project should keep an open mind to new ideas from any source. New proposals should be presented to John or myself, and hopefully, not argued on all levels.
4. I shall supervise the writing of the business plan with assistance from OEM marketing.

/ssb

PDP-11 Space/Power Survey

1. Existing Pieces...

   A. 11/05CPU - (New backplane, unspecified)
      2 Hex Modules
      1 Double Maint. Module
      1 Double TTY Connector
      2 Double Terminator

   B. 11/35 CPU - (Already exists for 11/40)
      8 Hex Module Slots
      1 Quad TTY Interface
      1 Double Terminator

   C. MM11U - (Exists for 11/40, 11/45)
      3 Hex Modules
      1 Quad Module
         Note: This cannot be packaged as a single system unit. MM11U's must be combined together or with other modules and packaged as a 9 slot S.U.

   D. Options -
      These are either Single or Double S.U.'s as specified.

2. Minimal System - 4 System Units?

   A. 11/05 - (This depends on Backplane Configuration)
      #1 CPU + 1 SPC (1 S.U.)
         16-32K MM11U (2 S.U.)
         Optional (1 S.U.)
      #2 CPU + 16K MM11U + 3 SPC (2 S.U.)
         Optional (2 S.U.)

   B. 11/35 (with internal options)
      #1 CPU (2 S.U.)
         16-32K MM11U (2 S.U.)
         Optional (Ø S.U.)
      #2 CPU (2 S.U.)
         16K MM11U + Optional 5 slots (2 S.U.)

   With 4 S.U.'s and 32K MM11U, there are no optional S.U.'s with an 11/35 and one with an 11/05. Marketing has decided that neither 16K max. memory nor Ø optional S.U.'s (11/35) is sufficient to sell stand-alone boxes, and that 5 S.U.'s is a minimum configuration.

3. Power Requirements

   Options with worst case power requirements (See list, next page).

4. System Power Requirements - 5 System Units (+5 split is made between the second and third S.U.)

   A. 11/05 - The 11/05 backplane will probably be CPU, 16K MM11U, 3 SPC's.

	+5V	+15V	-15V	+20V	-5V
CPU	8	.05	.25		
16K	6.1			4.4	.51
3 SPC's	6	.15	.75		
2 Term	2.5				
Total 11/05	22.6	.2	1.0	4.4	.51

OPTIONS

	Unit	Amps +5V	Amps +15V	Amps -15V	Amps +20V	Amps -5V
1.	11/35 (with internal options)	20	.05	.25		
2.	11/05	8	.05	.25		
3.	Bus Terminator	1.25				
4.	RK11-D (1 S.U.)	7.5				
5.	DJ11 (1 S.U.)	5		.48		
6.	DV11 (2 S.U.)	8.5	1			
7.	16K MM11U (active)	6.1			4.4	.51
8.	16K MM11U (standby)	4.5			.56	.41
9.	1 SPC	2	.05	.25		
10.	Parity Control	1.2				
11.	DA11-F Bus Window	5				

System #1 11/05, DV11, RK11D

	+5V	+15V	-15V	+20V	-5V
11/05	22.6	.2	1	4.4	.51
DV11	8.5	1			
RK11D	7.5				
Total System	38.6	1.2	1	4.4	.51
		+ 5 Split - 22.6, 16			

System #2 11/05, DA11-F, 32K MM11U

	+5V	+15V	-15V	+20V	-5V
11/05	22.6	.2	1	4.4	.51
DA11-F	5				
32K	9			1.12	.82
Total System	36.6	.2	1	5.52	1.33
		+5 Split - 22.6, 14			

B. 11/35

System #1 11/35, 32K MM11U, RK11D

	+5V	+15V	-15V	+20V	-5V
11/35	20	.05	.25		
32K	10.6			4.96	.92
RK11D	7.5				
2 Term	2.5				
Parity	1.2				
Total System	41.8	.05	.25	4.96	.92
		+5 Split - 21.25, 19.55			

System #2 11/35, 32K MM11U, 4 SPC's

	+5V	+15V	-15V	+20V	-5V
11/35	20	.05	.25		
32K	10.6			4.96	.92
4SPC's	8	.2	1		
2 Term	2.5				
Parity	1.2				
Total System	42.3	.25	1.25	4.96	.92

+5 Split - 21.25, 20.05

C. Expansion Chassis

System #1 16 SPC's, RK11-D

	+5V	+15V	-15V	+20V	-5V
16 SPC's	32	.8	4		
RK11D	7.5				
1 Term	1.25				
Total System	40.75	.8	4		

+5 Split - 16, 24.75

System #2 64K MM11U (Parity), 4 PC's

	+5V	+15V	-15V	+20V	-5V
16K (active)	6.1			4.4	.51
48K (standby)	13.5			1.68	1.23
2 Parity	2.4				
4 SPC's	8	.2	1		
1 Term	1.25				
Total System	31.25	.2	1	6.08	1.74

+5 Split 11.8, 19.45

System #3 20 SPC's

	+5V	+15V	-15V	+20V	-5V
20 SPC's	40	1	5		
1 Term	1.25				
Total System	41.25	1	5		
		+5 Split 16, 25.25			

5. System Power Requirements - 6 S.U. (+5 Split 1 is between third and fourth S.U. - Split 2 is between second and third S.U.)

A. 11/05 - Worst Case + 4 SPC's

System #1

	+5V	+15V	-15V	+20V	-5V
5 SU System #1	38.6	1.2	1	4.4	.51
4 SPC's	8	.2	1		
Total System	46.6	1.4	2	4.4	.51
		+ 5 Split 1-30.1, 16.5			
		+5 Split 2-22.6, 24			

System #2

	+5V	+15V	-15V	+20V	-5V
System #2	36.6	.2	1	5.52	1.33
4 SPC's	8	.2	1		
Total System	44.6	.4	2	5.52	1.33
		+5 Split 1 - 27.6, 17			
		+5 Split 2 - 22.6, 22			

B. 11/35

System #1 + 4 SPC's

	+5V	+15V	-15V	+20V	-5V
System #1	41.8	.05	.25	4.96	.92
4 SPC's	8	.2	1		

B. 11/35 con't

	+5V	+15V	-15V	+20V	-5V
Total System	49.8	.25	1.25	4.96	.92
		+5 Split 1 - 28.75, 21.05			
		+5 Split 2 - 21.25, 28.55			

System #2 + 4 SPC's

	+5V	+15V	-15V	+20V	-5V
System #2	42.3	.25	1.25	4.96	.96
4 SPC's	8	.2	1		
Total System	50.3	.45	2.25	4.96	.96
		+5 Split 1 - 29.25, 20.75			
		+5 Split 2 - 21.25, 28.75			

C. Expansion Chassis

System #1 20 SPC's and RK11-D

	+5V	+15V	-15V	+20V	-5V
20 SPC's	40	1	5		
RK11D	7.5				
1 Term	1.25				
Total System	48.75	1	5		
		+5 Split 1 - 24, 24.75			
		+5 Split 2 - 16, 32.75			

System #2 96K MM11U + 3 Parity

	+5V	+15V	-15V	+20V	-5V
16K Active	6.1			4.4	.51
80K Standby	22.5			2.8	2.05
3 Parity	3.6				
11 Term	1.25				
Total System	33.7			7.2	2.56
		+5 Split 1 - Impossible			
		Split 2 - 11.8, 22.1			

System #3 24 SPC's

	+5V	+15V	-15V	+20V	-5V
24 SPC's	48	1.2	6		
1 Term	1.25				
	49.25	1.2	6		

+5 Split 1 - 24, 25.25
+5 Split 2 - 16, 33.25

6. Conclusions...

A. 4 S.U.'s cannot provide sufficient space to sell a stand-alone unit. Requiring an expansion chassis means customers should buy the 21" box.

B. 5 S.U.'s - Can be sold stand alone. Worst case power:

+5V	+15V	-15V	+20V	-5V
42.3	1.2	5	6.08	1.74

Worst Case +5 Split - 25.25

C. 6 S.U.'s - Provides powerful systems but mechanically more difficult to cool. Worst Case Power:

+5V	+15V	-15V	+20V	-5V
50.3	1.4	6	7.2	2.56

Worst Case +5 Split 1 - impossible system
- of possibles - 30.1
+5 Split 2 - 33.25

These numbers should be referenced to the existing regulators:

H744 = +5V @ 25 Amps
H745 = -15V @ 10 Amps
H754 = +20V @ 8 Amps, -5V @ 1 Amp
54-9730 = +15V @ 3 Amps +AC10, DC10

Using two H744's, one H745, one H754 and one 54-9730, there are only a few places we significantly violate the power requirements for the 5 or 6 S.U. box. The 5 S.U. box violates the +5 split when 20 SPC's are

configured all with worst case +5. This would never occur in practice. The 6 S.U. box violates the -5V limit at 2.56Amps with 6 MM11U's. This is a possible configuration and must be avoided. The 6 S.U. also violates the +5 split with 33.25 amps. Reasonable systems still violate this split consistantly with approximately 28 Amps. This must also be avoided.

The 6 System Unit box therefore again requires configuration restrictions which make it very difficult to use as an expansion box, limits the air intake hindering cooling, provides no clear way to split the +5V for ease in distributing power, and is not required by marketing as a product. Limiting the box to 5 system units solves the above problems as well as provides sufficient space.

/ssb

Small-11 PDP-11/05L

Attached to this document, find the following:

1. A short memo describing my understanding of the project scope.
2. A short outline.
3. A first pass engineering schedule.
4. A Design Review Committee proposal.

A detailed breakdown of the FY74 budget is attached to a document entitled "Changes in Small-11 Hardware Plan" dated 9/7/73.

You will not find a very important document entitled "Business Plan". Among other things. the business plan should examine the several alternative products and predict their value. I am committed to publish the business plan in January 1974. Actually, I believe that I must be able to justify the project in terms that, at least, I understand well before that date. At this point in time, the project is proceeding based on the collective "gut-feel" that it is the proper approach, or at least, that the potential gains are very great compared to the certain risk of delay.

This project will cost 500K in FY74, and 1.2M total before the first ships in Fiscal January, 1975.

/ssb

SCOPE OF THE 11/05L PROJECT

Based on our present data, I predict that the cost of a replacement for the present 11/05 using the Western Digital N-channel chips to be in the neighborhood of $800 to $1000 for an 8K machine versus $1660 for the present design. As the comparison in figure 1 shows, a large piece of the savings results directly from changes to the CPU and memory. In fact, the reduction in size of the CPU and memory has indirect cost savings in other areas because the number of parts is reduced, the amount of power is reduced, etc. The reduction in the number of parts required by the CPU and memory should, if we believe history, have a positive effect on reliability.

Two other factors to consider are performance and compatability. Our present estimate is that instruction for instruction, the 11/05L will run 30% slower than the 11/05. However, we also believe it possible to build into the 11/05L the capability of executing the 11/40 plus EIS instruction set. FIS and memory management are, of course, not included. The 11/05L version of EIS would not be an option and would run much slower than in the true 11/40. Still, the effect would be that a multiply instruction in the 11/05L will take much less time than the software routine in the present 11/05. Performance comparisons between the 11/05 and 11/05L will therefore, be heavily task dependent. Including the several new 11/40 instructions and EIS in the basic 11/05L, also saves a few words of main memory for some applications. Given all of this complexity, I am assuming that for first order effects that the additional instructions in the 11/05L compensate for its slower operation.

Compatability is important because relatively small changes in the operation of the new machine have massive effects on software and peripherals. Even if these changes are an improvement over the present 11-family characteristics, massive improvements are required to offset the hardware and software conversion costs. Fortunately for the 11/05L project, there is already enough variation in the 11-family that it may be possible not to add many new "features". However, the size and cost reductions are likely to require some changes. Our job is to identify these as early as possible and carefully determine their consequences.

Conclusions on Project to Replace the 11/05

We can decrease manufacturing cost of an 11/05 replacement by up to a factor of two over the existing machine, decrease the number of parts by a factor of four to five, increase reliability, and for many applications, maintain performance. This project would make sense even without a very detailed business plan if it was going to be completed in the next month or two. Conjecture is that it makes sense even if the product is delivered in January, 1975.

Procede to Design 11/05 Replacement

Until such time as more data is generated, it makes sense to procede with the design of the 11/05L which includes the WDC contract. The gain of a few months in the time to market far outweighs the risk that our conjectures are way off target.

Additional Product and Market Opportunities

LSI seems to offer us magical opportunities to develop new products for new markets. However, we must be very careful not to commit large expenditures to develop products for markets we don't understand with the same flippancy with which we start the 11/05L project. In some sense, the business plan for a project like the 11/05L consists of the history of DEC. To extend this to consumer products sold thru Sears Catalog or even to standard systems is dangerous.

Item #2: consists of an outline for a report that has not yet been written. This document is now the beginning of my business plan which I have committed to fully develop by January, 1974.

How does this affect the WDC contract?

As the business plan is developed, we may realize that the WDC parts need to be modified to include additional features beyond the 11/40 plus EIS instructions. We may even find that WDC uses the wrong technology. We encounter a financial obligation to WDC which begins now at 50K and in April or May may increase to 700K. This is considered in my schedule of having a thorough business plan in January.

Will our group consider abberations of the WDC chips?

Yes, but not immediately. At this time, implimenting the 11/40 plus EIS instruction set and designing a hex module that contains the CPU, serial line, line clock, 4K of memory, and a Unibus control appears to be a gigantic but worthwhile challenge. It is very important that this new machine be instruction set and bus compatable with prior machines. Compatability is in fact, a major challenge as we have learned before, because the fine points of instruction execution tend to be implimentation dependent. In fact, a criteria for designing a new architecture is likely to be when new technologies make compatability with the past prohibitive or inefficient.

On the other hand, designing a Floppy Disk Control or other device controller with the WDC chips is probably easier than designing the basic PDP-11 because compatability with the past is not required. I believe that many other abberations are of a similar nature.

We are therefore proceding to design the basic processor first. We are accepting the risk that we may have overlooked some feature that is required for a device controller, etc. We now believe that we must concentrate our efforts on understanding what we believe will be the primary and most difficult use of the WDC chips. I believe that we will be in a position to examine some other product ideas in six months. Until then, I like Steve Rothman's suggestion that Jim Bell review the WDC specification and develop other uses for the WDC parts.

/ssb

Figure 1

ROUGH COST COMPARISON BETWEEN 11/05 AND 11/05L

11/05	11/05L	Item & Comment
120	60	Backplane (possibly reduce number of slots and allow system units. Use ELFAB blocks).
130	75	Power Supply (180W to 100W)
900	400	4K and CPU
950	500	8K and CPU
100	20	Console (Remove switches and add bootstrap ala Gordon Bell).
20	0	Harness (Remove)
85	50	Box
200	50	FA&T
45	45	Misc.
1600-4K	700-4K	
1650-8K	800-8K	

DANGER: Much more data is needed to build confidence into the 11/05L estimate.

This document contains thoughts which should be useful in the preparation of a business plan.

OUTLINE FOR 11/05L PROJECT DESCRIPTION

Presumed Goals

A. Provide a lower cost small PDP-11 system to protect the low end of the demand end-user business

B. Provide a PDP-11 entry into the computer plus memory on-a-board market.

C. The new system should be a binary compatable PDP-11 because:

   1. Building a PDP-11 is not significantly more costly than other 16-bit approaches.

   2. Given #1, it is in our interest, and our customers interest, to offer more economic but compatable products.

   3. A compatable PDP-11 with Unibus offers us the maximum flexibility in that we have peripherals and software already developed.

D. The new system should be designed for a ship rate minimum of 1000 per month and a maximum of 15,000 per month.

Can a PDP-11 be built from LSI chips economically?

Microprogramed implimentation techniques with the use of ROMS or Programed Logic Arrays for instruction decode have significantly changed the method for evaluating the cost of a machines architecture.

Western Digital (WDC)

A. WDC has offered to build a two (2) or three (3) chip n-channel dynamic MOS PDP-11 that may run at 50 to 70% of the speed of an 11/05.

B. WDC has experience in implimenting complex logic in MOS which we do not; therefore, we should be able to get to market sooner using WDC.

C. Of all the chip vendors that we have visited to date, WDC appears to offer the best balance of business situation and technical capability.

D. Most of the work that we do in conjunction with the WDC chip set will be applicable for either bipolar or MOS processors built elsewhere.

II. Pitfalls of using WDC chips.

A. There is some potential that we will not find out that the product that WDC claims to be able to build is a poor performer until very late in the project. As AMI can attest, even the experts are often wrong in the state-of-the-art LSI business.

B. If the center of our business required that the machine have 11/40 performance, then the n-channel MOS approach doesn't make sense.

C. As we are resource limited, working with WDC will cost us time in building a bipolar LSI processor.

D. Why consider bipolar LSI?

1. Bipolar circuits are four (4) to five (5) times faster than MOS and are capable of driving reasonable loads.

2. The performance of bipolar chips is easier to predict than the performance of MOS chips.

3. It is easier to second source static circuits as opposed to dynamic circuits. Fast MOS requires dynamic circuit techniques while bipolar circuits are almost certain to be static.

E. Why not use bipolar now?

1. Until recently, bipolar "foundries" have been reluctant to build chips of the complexity required.

2. Several high density, low power, bipolar processes are being developed but they are approximately two (2) years behind MOS.

3. In general, bipolar processes require more MASK steps than MOS; therefore, the yields for complex chips is supposed to be lower in bipolar. However, several vendors are developing processes which reduce MASK steps or increase the allowable MASK slop for bipolar chips. None of these new procedures has been tested to our knowledge.

F. There are other MOS processes that we will examine, but we do not anticipate that they will be available to us in the same time frame as WDC.

1. RCA, Intersil, and several other firms have a process called CMOS which has higher speed and more drive capability than n-channel, but is higher density than current bipolar. Andy Knowles invited RCA to visit in August but RCA did not respond.

trip to the West Coast.

2. Inselek in New Jersey and North American Rockwell in California have a process called Silicon-on-Saphire (SOS). This is a process in which the substrat itself provides dielectric isolation between transistors. Vendors who have it claim that it provides almost the speed of bipolar, but until recently, they have not even been able to make transistors. We should still investigate Inselek, but don't expect much hope yet.

IV. There are other considerations besides the CPU chip-set which affect the appearance, price, and marketability of the next small PDP-11 system.

A. Potential Products.

1. Chip sets - Several people have suggested that DEC sell unmounted chip sets thru Bill Hogan's group. I question this effort because I do not see that we add value to the chips and I don't believe that our salesmen know how to sell chips.

2. Computer and Memory On-A-Board (PC-Mp)

This product is really a low cost system although some speak of it as a "naked-mini". The PC-MP can actually be used as a computer system with only the attachment of a terminal or other I/O device. It does involve the use of our capital investment in both building and testing.

This product certainly does not justify our investment in an LSI-11. The Pc should be an 8 or 11 only if it is a fall out of a bigger project. I believe that this will happen.

3. 11/05 Replacement - To maintain our traditional market, we must plan to replace the 11/05 with a more cost competitive product within the next 1½ to 2 years. One suggestion is that the new machine be optimized around a small system in which the CPU with build-in multiply-divide, UBUS control, and Floppy control be constructed in the equivalent space of two (2) hex modules. The basic computer box would contain the above plus one (1) or two (2) Floppy drives. The manufacturing cost of this product would be roughly the same as today's 11/05, but functionally, it would compare to a DOS system with reduced storage. The definition of a barebones machine would be changed slightly.

COMPUTER: = Pc - Mp_{4K}
└Msz Floppy Drives - 100k words ez.
└ $K_{I/O}$ -ASYN Serial Line

4. Smart Terminal...

We propose that the new 11 be built into Model C of the Stockebrand terminal along with some form of mass storage. There are strong arguments that the mass storage unit should be the Floppy Disk.

This product is slightly different in appearance from, but similar in function to, many systems that we now sell for program preparation or data entry. It may have strong appeal in the OEM market for jobs similar to credit card checking or to the AVIS Wizzard type of function.

Some questions to consider:

a. Should the Unibus be available from the smart terminal as it is on the GT40? Our first thought was no, but this may be a hasty decision. Availability of the UBUS presents some mechanical problems but has potential gains in the attachment of peripherals or customer interfaces.

b. Should the terminal designed to be clustered rather than one (1) computer per one (1) terminal? I believe that we already have this product.

c. Should the terminal be designed to emulate an IBM or other popular product used for data entry?

d. Etc.

5. Briefcase Computer System (BCS)

We believe that it will be possible to build an 8K computer, a keyboard, plus a floppy control and drive into a briefcase sized package that is not unacceptably heavy to be hand-carried. This device would display onput on a standard TV set and would use Floppy Disk cartridges as an interchange media.

Potential users:

a. Traveling salesmen - every motel has a TV set.

b. Small businessmen

c. Scientists - a powerful extension of the slide rule.

d. School children

e. Housewives would form computer-program-of-the-month club. Programs would help optimize such things as food budget, money management, etc.

f. Sports enthusiast - Boatsmen in particular would like to interface it to their electric compass, depth finder, and radio direction finder

g. Recreational uses would be too numerous to mention. There are already a variety of games which use Digital logic to drive a TV display. To try one such game, visit Giovani's restaraunt on Rt. 9 in Framingham.

Problems - Price:

Today, we are not able to project that the price of random access memory will be sufficiently low. Mass storage is already available in the form of audio tape or TV tape recorders. It would appear that a low performance Floppy could be built for $100 if we desired.

- Marketing:

We could overcome all technical problems if we could project the size of the market and the market size elasticity vs. price and function.

V. Where do we go from here?

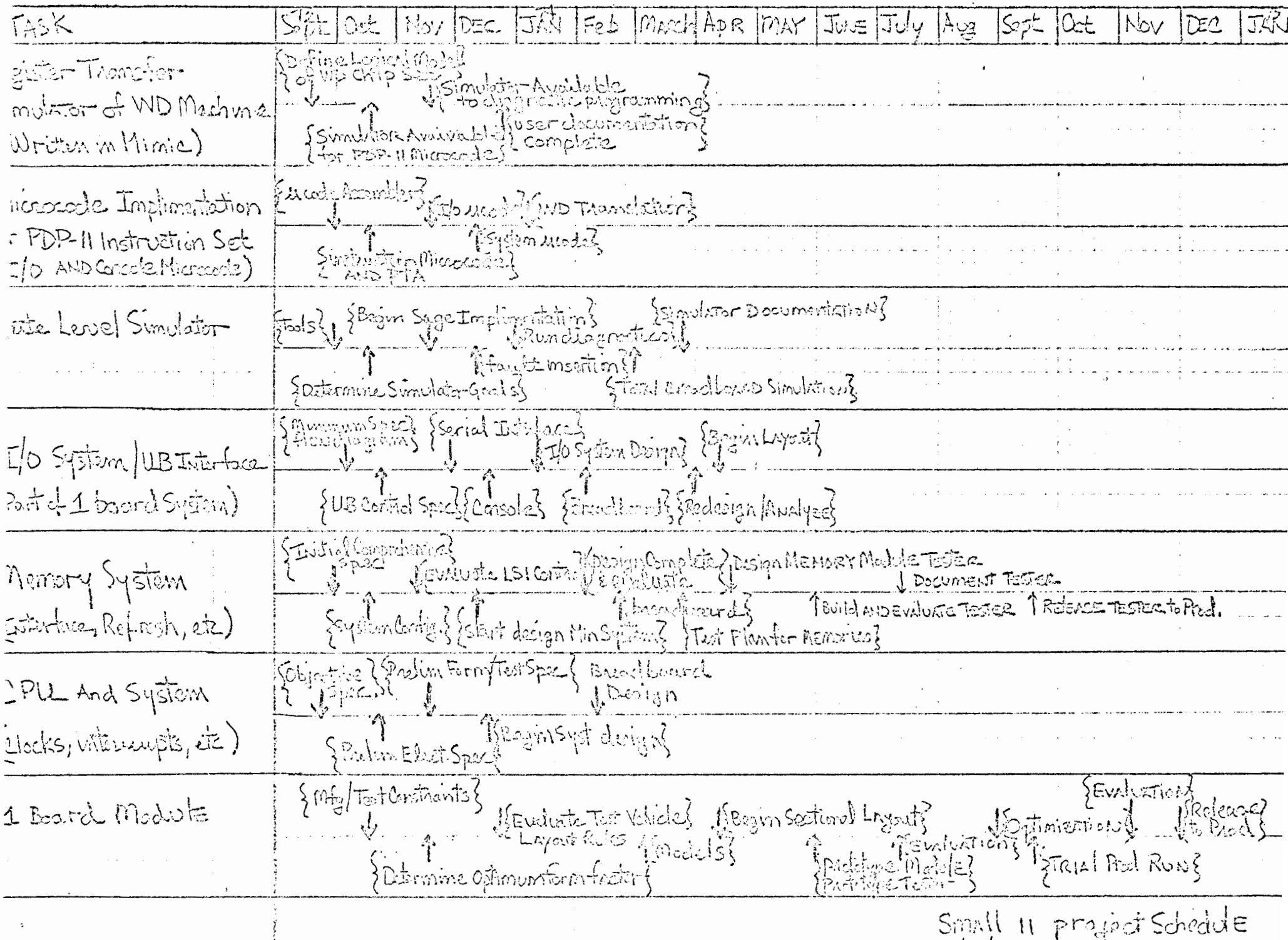
A. It is clear that we must develop the tools to deal with the next generation of technology. Developing technology will fast replace our current products with lower cost alternatives. We can either watch this happen or join-in and extend our markets.

B. Traditional DEC procedures suggest that the best way to measure success in the development of a new technology or new market is to make both short term and long term profits in the process. Vendors such as WDC can help us accomplish the goal of short term profits. In the long term, we will most likely manufacture our own integrated circuits. A beginning in this path is being made by Henry Lemaire.

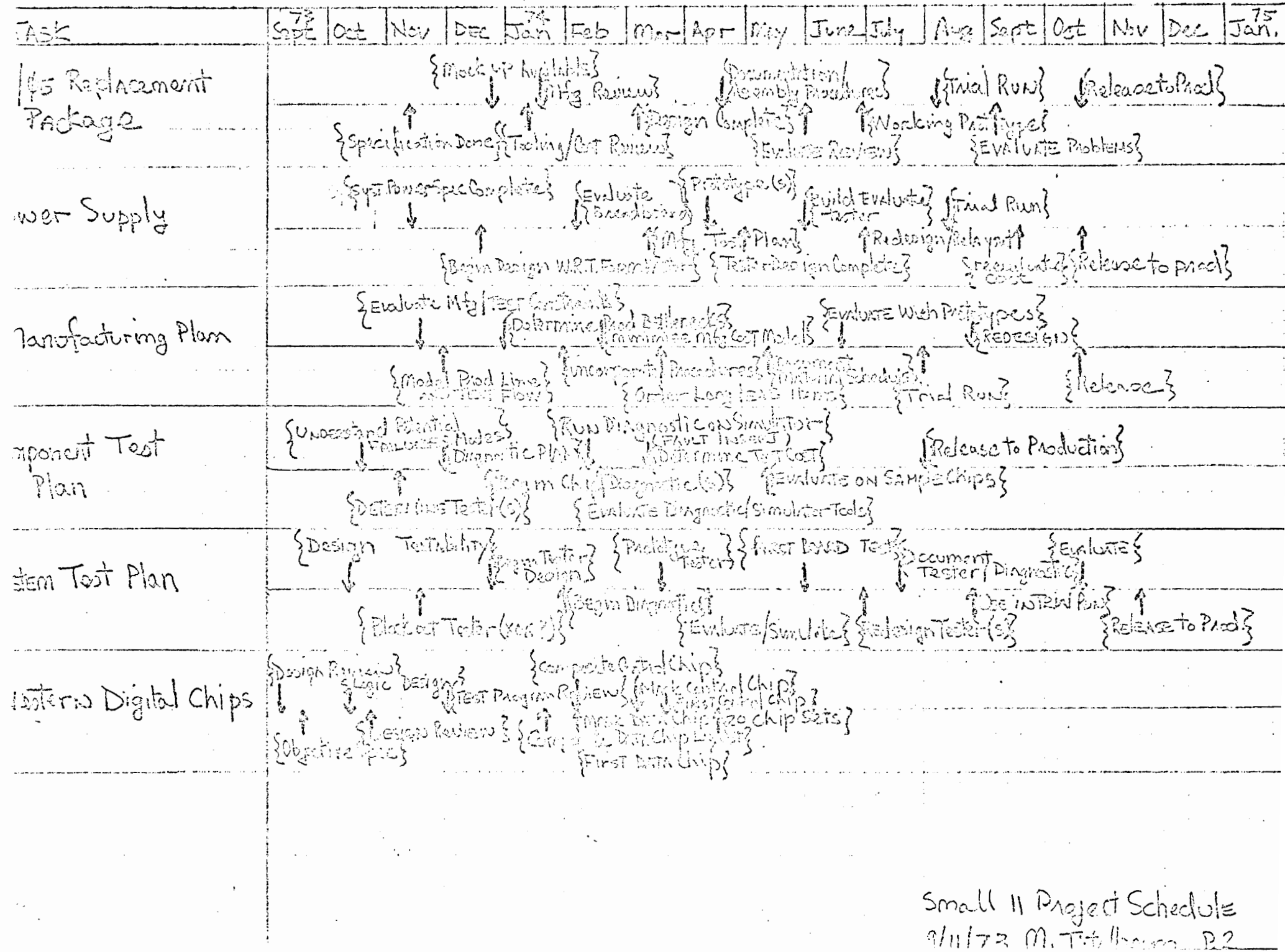
C. Our group and others such as Lorrin Gale's crew, are learning how

to translate our traditional requirements for computer systems into higher technology and potentially higher volume, higher profit products. We will also feed back to present marketing groups and to others, suggestions on different products which will may suggest the development of a new customer base.

A basic reason for the new engineering efforts required for LSI or even more standard high volume approaches is that the cost of mistakes in the final product is very great. The possibility of ECO's costing several millions of dollars and the shutting down of a high volume production line make a few hundred thousand dollars of extra engineering cost small insurance. In fact, with MOS-LSI, a large effort is necessary just to be aware of the risk at any point in time that the final design might not be functional.



Small II project Schedule



Small II Project Schedule
9/11/73 M. Title Name P2

SMALL 11 Project Schedule - Attachment

There are some tasks that are not explicitly shown on the attached project schedule. The tasks are ones which cannot logically be scheduled at this time. For example, by the time the business plan is finalized we will have determined a mutually acceptable maintenance philosophy and general field service plan. At that time we will also submit a schedule for manuals and technically distributable documents as well as application and user notes. Design reviews are described in a separate document and will be held monthly to discuss problems and implimentations.

It is also implied that the schedule is rigid and cannot be changed. The classic flaw with the rigid schedule is that interdependencies develop which may bring certain tasks to a halt unless another has been completed. We have observed this many times before. Yet we are open to inputs and responses and will make the necessary changes to this schedule as the project progresses. One thing is clear and that is, if Western Digital succeeds with their own ambitious undertaking we must be ready with the tools and designs for our own product.

WDC/DEC MILESTONE SCHEDULE (ITEM 1A)

	Design Review	-	September 5, 1973
	Objective Specification	-	September 17, 1973
a.	Logic Design	-	October 5, 1973
	Design Review	-	October 17, 1973
	Test Program Review	-	November 16, 1973
b.	Composite Layout		
	Data Chip	-	January 14, 1974
	Control Chip	-	February 15, 1974
c.	Mask		
	Data Chip	-	January 21, 1974
	Control Chip	-	February 22, 1974
d.	First Devices		
	Data Chip	-	February 1, 1974
	Control Chip	-	March 1, 1974
e.	20 Sets	-	March 29, 1974

INTEROFFICE MEMORANDUM

TO: Dick Amann
(Eng. Comm. Rep.)
Henry Ancona
(11 Hardware Prod. Comm.)

DATE: September 11, 1973

FROM: M. Titelbaum

DEPT: 11 Engineering

EXT: 3477 LOC:

SUBJ: 11/Ø5 Design Reviews

The design review function for the next small 11 can be looked upon as being made up of two groups. The first group, composed of members of the 11 hardware products committee, will be responsible for reviewing the project plan, overall design goals, business plan and monitoring our progress toward reaching these goals. The second group, composed of members from allied design groups, will be available to technically evaluate and influence the design of this potentially very high volume product.

The first technical design review was held on Thursday, September 6 and will meet approximately once per month for the next six months. Ken Fine representing the VTXY was chosen as chairman and secretary for this meeting. Minutes from this meeting will be distributed this week. The other members of the committee are listed along with the groups that they represent and their experience areas.

Steve Rothman -	Central 11 Engineering	- PDP-11 System Problem
John Levy -	" " "	- Multi-CPU Configurations
Don Vonada -	" " "	- 11/45 MOS Memory Systems
Bob Kusik -	Microproducts	- Gate Level Logic Simulation
Al Wallack -	LPD	- Unibus Interface Design
Vince Bastiani-	Communications	- Communication implications
Herve Lavoie -	Graphics	- PDP-11 Applications

Groups represented and experience areas (cont'd)

Phil Goldman	- Memory	- Core and MOS Memory Expert
Ron Marchetti	- Production	- Experienced High Volume Pro
John Bloem	- Logic Products	- Micro CPU implimentations

There are others who should attend these design reviews but the above core group should remain intact as much as possible. Anyone with inputs or questions about the project should contact either Steve Teicher or Mike Titelbaum. The next design review is tentatively scheduled for October 4.

There are other groups which I will refer to as task or work groups to distinguish them from the design review groups. It is with these task groups at weekly meetings that we hope to:

1. Discuss Progress of each task with the associated tasks.
2. Discuss specific problems and allow for group solutions if necessary.
3. Revise schedules or update completion dates if necessary.
4. Ensure that task group is not proceeding tangentially from the overall design goals.

Task Group A - Engineering Related directly to MicroCpu, Memory, Interface and Testing.

1) Small 11 Engineering - Mike Titelbaum, Duane Dickhut, Al Marsh
2) Diagnostic Programming - Walter Manter, Fred Straight
3) Software Engineering - Mike McCarthy, Len Feshkens
4) Test Engineering - Ed Gianetto, Art Berner
5) Memory Engineering - Phil Goldman, George Hitz

The above task group will be responsible for a one board implimentation of a PDP-11 central processor with 4K of MOS memory.

INTEROFFICE MEMORANDUM

TO: Bob Gray
Dave Peters

DATE: November 1, 1973

FROM: Steve Teicher

DEPT: Small 11 Systems Engineering

EXT: 3175 LOC: 1-3

SUBJ: 11/Ø5R Product Summary

1. Goals - In Order of Priority:

   (a) Provide a replacement for the 11/Ø5 which will be competitive for the 2 1/2 to 3 year period beginning January 1975.
   (b) Assist Manufacturing in the development of test and repair methods consistant with the shipment of 5000 Small-11 systems per month.
   (c) Participate in the development of a new set of computer-aided design engineering tools which have utility for devices already in production as well as for new products.
   (d) Provide building blocks for a range of products which include the SMALL-11 system or PERSONAL-11 at one level of complexity and the NAKED-11 at another level.
   (e) Provide a series of rather general purpose, micro-programmable, microcomputer chips which may be needed to build smart controllers, calculators, and other to be determined products.

2. Configuration:

   (a) 11/Ø5R:
      I. 5 1/4 inch package
      II. 1-DD11B contains CPU & 8K parity memory & 3 free SPC slots.
      III. 1-space for 4 slot system unit.
      IV. 1-CPU with serial line, EIA and TTL outputs, 110 to 2400 baud via crystal oscillator, line clock, bootstrap, ASCII console interface, power fail auto restart. 8K MOS memory mounts on daughter card. CPU executes 11/4Ø instruction set plus EIS.
      V. 100W to 750W PS with battery backup.
   (b) NAKED-11:
      (Item IV above)

3. System Manufacturing Cost:

   (a) CPU & Memory - $500

(b) Above plus box and power supply - $800 to $900

4. Development (Engineering) Cost:

FY74	500K
FY75 to First Ship in January 1975	700K
FY75 Total	1.4M
FY76	300K
FY77	100K

5. Applications:

(a) Present 11/Ø5 OEM and End User market.
(b) NAKED-11 hits in smart terminals and is useful as smart controller for both OEM vertical markets.

6. Problems Solved:

(a) Cost reduces 11/Ø5 by ~50%. This is necessary to be able to compete next year in the market we own.
(b) Permits the economic sale of NAKED PDP-11 processors plus memory.
(c) Helps to reduce impact of ADD-ON memory vendors. Each 4K memory increment up to 16K (if possible) consists of 25 chip matrix mounted on a daughter module and costing less than $200.
(d) Provides a set of building block microprocessor chips.

7. Weaknesses:

(a) Performance: Probably 30% slower than present 11/Ø5. Hardware multiply/divide will help.
(b) High Risk Technology: Best method of implementation requires LSI chips. If LSI chips efforts fail several features such as multiply/divide will not be available.

8. Configuration Information:

			Mfg. Cost
(a)	NAKED-11	CPU & serial line & line clock & 8K parity memory	$ 500
(b)	11/Ø5R	Above plus box, backplane, power supply	800 to 900
(c)	11/E1ØR (CPU, memory and option controllers all fit in 5 1/4" box)	11/Ø5R	900
		RK11D	494
		RKØ5	1300
		LA3ØL (estimate)	500
		TU6Ø	1060
		TA11	
		Cabinet	200
		Sub-Total	$4454

		Mfg.Cost
	Integration Cost (12%)	$1068
	Total	$5522
(d) 11/ElØR'	11/Ø5R	900
	Floppy & Control	750
	VT5Ø (my guess)	300
		$1950

9. Development Information:

Project Includes: LSI chips, 4K RAM evaluation and MOS memory system, simulation development, extensive testor development, manufacturing line specification, and a packaging effort.

Funds will be expended to backup LSI efforts; but not all features will be available without LSI and manufacturing price will be greater.

10. Schedule:

Start Design	-	August 1973
Operate Prototype	-	July 1974
Limited Release	-	September 1974
Public Announcement	-	October 1974
First Shipment	-	January 1975 (Volume 300/month)
Release to Production	-	March 1975 (Volume 1000/month)

digital INTEROFFICE MEMORANDUM

TO: John Fisher

DATE: April 25, 1974

FROM: Steve Teicher

DEPT: Small 11 Engineering

EXT: 3175 LOC: 1-3

SUBJ: Small 11 Product Plan

Objectives

1. Protect and Increase Digitals' penetration into the small computer systems market where we are now successful.

2. Without compromising objective number 1, build products that will establish a strong position in the computer component market.

Strategies

1. Milk the present PDP-11 family which consist of processors, and interconnect system, and many peripherals.

   a. Solve the mix and match problems between boxes, memories and power supplies.
   b. Use new boxes and power supplies to reduce production cost. Make decisions on economics.
   c. Define and engineer a low cost backplane that is suitable for processors, memories, and small peripherals.
   d. Engineer new MOS and Core memories with the goals of low cost, low power consumption, and sensible ~~purchasing~~ packaging
   e. Recognize that we cannot define a low cost processor that can serve the entire spectrum of low end customers. We can plan for a series of processors that are interchangeable, are each optimized for a particular characteristic plus low cost, and for the most part are each built with available TTL parts. It is necessary to engineer the product, the manufacturing method, and the service method for this to be practical.

2. Develop a new PDP-11 system that uses the benefit of new technology to reduce the cost of peripherals as well as the processor and memory. The Unibus will probably not be used to connect the processor, memories, and the high volume peripherals. Some programming incompatabilities are likely to occur, but a goal is to understand the impact of these incompatabilities and to insure that this impact on our customers is palatable.

Tactics

1. Make sure that we have a new product to introduce in the fall of 1974.

2. Develop a method such as a customer profile for aiding the salesman in selling the correct product.

3. Be prepared to sell products at any level, i.e. chips, modules, and systems.

COMMENTS ON WESTERN DIGITAL AND THE WD CHIP SET....

1. WESTERN DIGITAL HAS SENT US A NEW SCHEDULE WHICH SAYS THAT WE CAN RECEIVE WORKING CHIP SETS IN SEPTEMBER AND PRODUCTION VOLUMES IN DECEMBER. I BELIEVE THAT THE DECEMBER DATE IS OPTIMISTIC. I BELIEVE THAT WE WILL RECEIVE WORKING CHIPS IN THE SEPTEMBER-OCTOBER TIME FRAME AND PRODUCTION IN Q3. THIS MEANS THAT WE WILL BE ABLE TO SHIP PRODUCT USING THE WD CHIPS DURING LATE Q4.

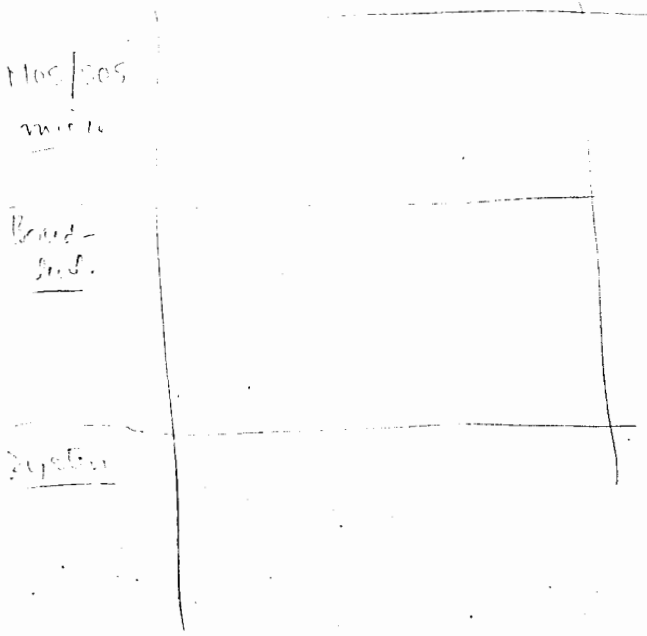
2. WE ARE PUTTING MORE PRESSURE ON WESTERN DIGITAL TO PROVIDE US WITH TECHNICAL AND SCHEDULE INFORMATION. BILL ROBERTS HAS AGREED TO PROVIDE US WITH A SCHEDULE UPDATE EVERY SECOND WEEK. WE ARE BEGINNING TO ADDRESS THE TESTING ISSUE TOGETHER. WE HAVE ASKED THEM AND THEY HAVE AGREED TO PROCESS OUR N-CHANNEL TEST PATTERNS. THIS SHOULD PROVIDE US WITH A DATA POINT ON THEIR 4K PROCESS. HOWEVER, THIS DATA POINT WILL NOT BE CONCLUSIVE UNLESS THEY FAIL VERY BADLY.

3. WE KNOW THAT WE HAVE NOT DESIGNED THE MOST COST EFFECTIVE SYSTEM WITH THE WD CHIPS. NOW THAT WE REALIZE THAT IT IS NEITHER POSSIBLE NOR NECESSARY TO COVER THE ENTIRE LOW-END MARKET WITH ONE PROCESSOR MODULE, WE CAN BEGIN TO MAKE MORE INTELLIGENT COST, PERFORMANCE, COMPATABILITY TRADEOFFS.

4. WE BELIEVE THAT WE NOW HAVE THE CAPABILITY TO WORK WITH ANOTHER VENDOR IN ADDITION TO WD ON A POSSIBLE CUSTOM PROJECT THAT WILL ENABLE US TO BUILD SYSTEMS WITH LSI THAT INCLUDE PROCESSORS, MEMORIES, AND PERIPHERAL CONTROLLERS.

STEVE TEICHER

APRIL 29, 1974



SIGNIFICANT PRODUCT GAPS EXIST BOTH ABOVE AND BELOW THE PDP 11/05

WE BELIEVE THAT A SERIES OF PDP-11/05 MODULE OPTIONS CAN COST EFFECTIVELY WIDEN THE PDP-11/05'S APPEAL IN THE JUNGLE

PROCESSOR MODULE OPTION CONSTRAINTS ARE DESIGNED TO EMPHASIZE:

A. LOW INTRODUCTION COST
B. LOW MANUFACTURING COST
C. SIMPLE CONFIGURATION RULES
D. LIMITED OPPORTUNITY FOR ONE-PLUS

MAJOR THRUSTS OF THE SMALL-11 PROGRAM WILL BE TO

A. SIMPLIFY CONFIGURATION BY EVENTUALLY FORCING PROCESSORS, MEMORIES, AND OPTIONS INTO A COMMON BACKPLANE.

B. PERMIT THE USE OF COST EFFECTIVE 16K AND 32K SENSE EMORIES IN ALL PDP 11/05 CONFIGURATIONS.

C. ADD MOS MEMORY AT THE 4K AND 8K LEVELS IN STEP WITH COMPETITION.

D. IMPROVE MANUFACTURING TECHNIQUES TO REDUCE COST AND TO IMPROVE RELIABILITY.

E. PLAN FOR MANUFACTURING VOLUMES CONSISTENT WITH THE CORPORATE BUSINESS PLAN.

APPROXIMATE INTRODUCTION COST OF CPU MODULE OPTION

ASSUMPTIONS:

1. PROCESSORS FIT ON TWO HEX MODULES OR LESS.
2. PROCESSORS ARE PIN FOR PIN COMPATABLE AS FAR AS BOXES, MEMORIES, AND PERIPHERALS ARE CONCERNED.
3. MODIFICATION TO SYSTEMS SOFTWARE AND TO DIAGNOSTICS REQUIRES 1 QUARTER OR LESS FOR THE OEM MARKET.

TASK	COMMENTS	COST ($K)
PAPER DESIGN	1 QTR. FOR 2 ENG.	14
SIMULATION	1 QTR. FOR 1 PROG.	7
BREADBOARD	2/3 QTR. FOR 2 TECH.	8
P C LAYOUT	6-15 WEEKS	2.3-5
DRAFTING	1 QTR. FOR 1 MAN	5
PROTO DEBUG AND MARGINING	1 QTR. FOR 3 MEN	21
GR TEST PROGRAM	1 QTR. FOR 1 PROG.	7
MANUALS	100 PAGES @ 100/page	10
MFG START-UP	PROCEDURES, TESTING, PARTS	20-40
SPARES*	500 @ $150-$300 EACH	75-150
SOFTWARE REV.		0-20
	SUB-TOTAL	169.3-287
	ADDITIONAL TOLERANCE +10%	17-29
	TOTAL ESTIMATED COST	186.3-316

*Spares are shipped only slightly ahead of customer machines; therefore the full cost is encountered only if product success.

LONG TERM PLAN FOR SMALL-11 FAMILY

1. RECOGNIZING THAT TECHNOLOGY AFFECTS PROCESSORS, MEMORIES, AND PERIPHERALS, WE MUST DESIGN COST EFFECTIVE REPLACEMENTS FOR SMALL SYSTEMS. ONE SUCH SYSTEM WILL BE A PDP 11 PROCESSOR INTEGRATED INTO A VT5X OR A LA36.

2. WE MUST ATTEMPT TO PROVIDE SMOOTH TRANSITIONS BETWEEN OLD AND NEW TECHNOLOGIES.

3. WE MUST CONTINUALLY EXAMIN THE MOTHER*HOOD PHRASE, COMPATABILITY------

TOTAL CORPORATE 11/05 CPU FORECASTS

Type/Description	1976 Units No.	1976 Units %	1976 Avg. $/ CPU	1976 Dollars No.(KK)	1976 Dollars %	1977 Units No.	1977 Units %	1977 Avg.$/ CPU	1977 Dollars No.(KK)	1977 Dollars %
11/05, Current	8,700	50%	$8,000	$70	50%	-	-	-	-	-
11/05 R/WD	2,200	15%	$8,000	$18	13%	8,200	30%	$8,000	$66	27%
11/05 C, Cost	2,600	15%	$5,000	$13	9%	8,400	30%	$5,000	$42	17%
11/05 M, Memory Expansion	1,500	10%	$14,000	$21	15%	5,400	20%	$14,000	$76	31%
11/05 P, Performance, Speed	1,600	10%	$11,000	$18	13%	5,500	20%	$11,000	$61	25%
TOTAL	16,600	100%	$8,400	$140	100%	27,500	100%	$8,900	$245	100%

digital INTEROFFICE MEMORANDUM

TO: Steve Teicher
Joe Meany

CC: Gordon Bell
Dick Clayton
Marv Cothran
Andy Knowles
Bill Long

DATE: 4/25/74

FROM: Mike Tomasic

DEPT: PDP-11/05 OEM Marketing

EXT: 3867 LOC: PK 3-1

APR 29 1974

SUBJ: LOW-END PDP-11 FAMILY

With the concern regarding the 11/05R WD effort, I would like to propose a series of three 11/05 CPU module designs. These 11/05 CPU designs would all be interchangeable, and all utilize the same:

1. Core or MOS Unibus Memory
2. Core or MOS power supplies
3. 5-1/4" or 10-1/2" chassis
4. Backplane logics

The prime goal of the three designs would be to maintain low cost, while offering the customer one additional significant feature. By holding memory, power supplies, chassis and backplanes constant, both development and manufacturing costs would be minimum while offering our customers several low cost 11/05 CPU alternatives. These alternatives could be more acceptable to the customer needs in different markets, not trying to force one general purpose design on all customers requiring low cost.

1. 11/05C: Cost optimized design, with goal of a single hex CPU module. This design shall not have a console, serial communication line, or line frequency clock, all standard features of the current 11/05.

The 11/05C shall be our low price highly advertised door entry OEM CPU. It is a viable design for high volume cost conscious customers, such as Motorola's motel management system and Mosler's teller system.

2. 11/05 M: Memory expansion to 64 K, potentially 124 K, with a goal of two hex CPU modules. This design shall not have a serial communication line, or possibly a line frequency clock.

continued . . . .

The 11/05 M shall be our low price CPU with memory management subset. It is a viable design for high volume cost conscious customers who need memory expansion beyond 28 K, such as Applicon's automatic drafting system, CMC's key to disk system, and Radiation's typesetting system.

3. 11/05 P: Performance speed (similar to 11/35) with a goal of two hex CPU modules. This design shall not have a serial communication line, or possibly a line frequency clock.

The 11/05 P shall be our low price CPU with fast performance. It is a viable design for high volume cost conscious customers who need performance, such as Tektronix and Time Data/General Radio in the laboratory market.

The combination of both speed and memory expansion does not appear possible with minimum two hex module CPU maintaining low cost, therefore this requirement must be provided by the new 11/44 with 5 to 7 hex module CPU with medium cost.

/b

To: Steve Teicher
From: Mike Tomasic
Subj: Low end PDP-11 Family

11/05 CPU SUMMARY

Type	Feature	No.CPU Hex Boards	Console	Serial Communication Line	Line Frequency Clock	Market
11/05	Current	2	Included	Included	Included	General purpose low cost
11/05 R/WD	EIS/FIS	2	Included/ Option	Included	Included	General purpose low cost 11/05 replacement
11/05 C	Low Cost	1	Option	Option	Option	High volume low cost commercial/industrial applications (Motorola, Mosler)
11/05 M	Memory Expansion to 64 K/124 K	2	Included/ Option	Option	Included ?	Large memory low cost commercial/industrial applications (Applicon, CMC, Radiation, Periphonics)
11/05 P	Performance, 11/35 speed	2	Included/ Option	Option	Included ?	High speed low cost laboratory applications (Tektronix, General Radio, Time Data)

G. Bell
for Thurs. Breakfast
Meeting

SMALL 11 STRATEGY

Steve Teicher
May 2, 1974

TABLE OF CONTENTS

Cover Letter

Within this document, you will find what I believe to be a reasonable Small-11 strategy, which will enable us to proceed with aggressive engineering developments both with existing and new technologies. We are attempting to make optimum use of our ability to lay out, manufacture, and test modules. We want to simplify but to broaden the appeal of current technology products. We have been and shall continue to work with Manufacturing and Field Service to design more reliable products, and we believe that this is consistent with our strategy.

I emphasize that the strategy that we propose is not complete. We need to develop it with you. I do believe that we understand enough to pursue responsible product development and to design enough flexibility into our product definitions to permit reasonable response to new ideas. We should be able to make effective use of the Technology Product Committees that Gordon Bell has suggested.

Please note that I am generally opposed to changes in product definition which lengthen schedules or increase product cost by the one-plus approach. In fact, my product strategy specifically addresses the "one-plusers" and gives them room to operate without affecting what others may believe are the main stream products.

SMALL 11 STRATEGY

I. Introduction

The delay in the 11/05R schedule has encouraged us to re-examine our low-end strategy, which should have been done anyway. I believe that our thoughts are more clear today and that we should alter our plans to take advantage of this new insight.

When we conceived the 11/05R, we thought in terms of a single replacement product for the PDP11/05. For some reason that I cannot remember, we believed that we could specify a CPU and memory that would have such enormous appeal that we could build an entire factory to ship this item in high volume. Even if we could eliminate the technical risk for any specification that could be generated, it should have been obvious to us that the electronics business is not sufficiently stable for this strategy to be accepted by the market.

Perhaps we were lulled into complacency by the fact that we intended to use LSI or 4K RAM memories. Perhaps, we were enamoured with the $500 price that I quoted so often. We should all understand that for the near future 4K MOS RAM's are a competitive plague upon us. As soon as TI, MOSTEK, and others begin delivering parts in reasonable volumes, the cost advantages that we now have in core memories over our competition will evaporate in the 4K and 8K systems. The investment to build memory systems with good MOS chips is considerably less than that required to assemble and test core memory systems. Even the biggest skeptics now will admit that MOS memory technology will develop much faster than did core memory technology. Very few of us would be able to be convinced that Digital could avoid shipping product with 4K MOS memory in calendar 1975, even though we might feel more comfortable to wait longer.

Microprocessors and LSI also appear to be developing faster than Digital would like. We have an entire line of product that is designed around TTL-SSI and MSI circuits. Low-density TTL logic encourages the trade off of bus width for logic complexity, because often wires cost less than multiplexers with SSI or even early MSI. I could cite many examples of the architecture of any of our products which take great advantage of the implementation technology. Microprocessors and LSI may force us to take drastic steps such as re-engineering all of our peripheral controllers and rewriting much of our software. We are clearly justified in using the Andy Knowles punch line, "Such is life in the jungle."

Issues that shall be addressed in this document include:

A. Short-Term Low-End PDP-11 Strategy.

B. The Effect of LSI on Short- and Long-Term Strategies.

C. Should we build some other 16 bit computer other than the PDP-11.

I believe that product planning for the low end to be a full-time job that cannot be adequately served by a functional manager, such as myself, or a product support group, such as currently found in many product lines. Just as some of the market groups have lured the equivalent of product strategist, I have hired a product manager whose first full-time job will be to coordinate the low-end strategy and match our development efforts to what the market groups want to sell and to what the customers of the market groups want to buy. I hope that this document, along with the comments of the market groups, will provide a starting point for Ed Steinfeld. I shall continue to accept full responsibility for the actions of the group that I manage.

II. Low-End Market Assumptions

I believe that a basic fact of life of the low-end market is that the simplest, most specific product generally wins over the more general and complex product. This rule is violated only when it is possible to build a general product that has such wide appeal that it can be manufactured in very large volumes, and this fact of large volume production is a major factor in the product's low cost. The danger in attempting to design low-end general purpose products is the phenomenon of "one-plus." It is very easy to believe that any small incremental addition to a product will have great market appeal while any subtraction is a disaster. We often one-plus products without even an attempt to evaluate the cost of the added features versus the resultant increase in sales.

The "ONE-PLUS" phenomenon is quite understandable when we look deeper into our product strategy. To the best of my knowledge, we have avoided having two products, in the same price class, that have slightly different characteristics. The engineer and marketeer feel that they have only one shot at the market, so they build in all the hooks that they can conceive as insurance against failure. This insurance adds cost to every product that we ship and detracts from many of our major goals such as reliability and easy maintenance.

11/05 Price Class Customers Are in Different Businesses

Tektronix builds test equipment, Motorola builds hotel reservation systems, Applicon builds IC layout tools, and I could go on. Very few of us would argue that all 11/05 customers need the same size disk or even the same size memory. There is certainly some possibility that the characteristics of the central processor required by General Radio and Tektronix could differ from that required by Motorola.

There are several methods that have been chosen to tailor the computer system needs to the customer. The Cadillac approach says that we sell PDP 11/45's with bipolar memory to everyone. Unfortunately, the module cost of the 11/45 processor alone is roughly 7 times greater than the cost of the PDP 11/05 CPU. Furthermore, the power of the 11/45 is not realized unless the system is configured with high performance peripherals.

The PDP-11/40 is the compromise, modular machine. The cost of the basic processor without options is hopefully low enough so that we get the entry level customer and we become very happy when he buys floating point and memory management. This approach works with some percentage of our customers who are not quite so sure of their system needs. They are willing to buy the expansion hooks as a form of insurance. There should be no doubt that the expansion hooks and the extra performance built into the 11/40 cost money. Cost comparisons will be displayed later in this document.

The most successful approach, for the high volume OEM, should be to sell the customer exactly what he needs and nothing more. The high volume OEM should understand his applications in enough depth to be able to predict his system requirements with great precision. Obviously, there are some limits of customization which are better solved by having a limited range of standard products just as General Motors has an extensive but not infinite range of different automobiles.

Furthermore, we need to place some guidelines on where we should have different products for different market requirements and where we standardize on items across all markets. We want to avoid different products or subassemblies where different versions:

A. Do not increase the function of a product in a market segment.

B. Do not affect the cost or adversely affect the cost of dealing with a market segment.

C. Do not offer us access to a reasonably large group of potential customers.

D. Do not fit smoothly into our high volume production areas. For instance, a market segment that required processors to be built on spherical modules should be carefully examined.

We want to encourage product differences where they:

A. Greatly increase our competitive position by enabling us to narrow the range of a given product and aim it at a large market segment.

B. Broaden the utility of the standard corporate subassemblies and increase the economies of scale. For instance, if I can selectively add a small widgit to an 11/XX and increase its sales by 1000 per month, then we do get a tremendous gain for the whole company if you believe that the learning curve for the 11/XX is a function of cumulative volume.

Obviously, we want to plan for product differences in areas that cost us the least pain. The corrollary is that if we do not plan for product variation and our competitors discover a significant hole in our strategy, we will:

a. Be forced to engineer catch up products that do not quite fit. For instance, we clearly did not plan to use the 16K sense memory in other than 11/45's and PDP 10's. Unfortunately, competition forced us to reconsider this strategy and we now have the 10½ inch cabinet.

b. Loose market share and feel very dumb.

III. Short-Term Plan for Effectively Covering the Low-End 16-Bit Computer Market

We need to recognize that, in the short term which includes the next 12 to 18 months of development and up to 2 years of sales time, we are going to observe a confused migration towards exotic products, such as microprocessors; but I do believe that we shall continue to observe a large acceptance of more conventional small computer systems. If we are careful, I believe that we can--with a reasonably small investment--milk the conventional small system business. Furthermore, I propose that we already have most of the more expensive to develop tools for selling into market in terms of peripherals and software. All we need is a convenient means of assembling equipment and perhaps several mid-life kicher products.

Our proposal for a family of low-end 16-bit PDP-11 processors should have the following effects:

A. Mike Tomasic estimates that the family of low-end processors should increase sales from 25% to 50% over the single CPU approach. This represents a large increase in memory and peripheral business which consist of PDP-11 standard products.

B. By consolidating small processors, most memories, and most peripherals into a common backplane, we should greatly simplify the configuration rules for the salesman. The new TPS power supply has sufficient capability to operate most small systems that fit in the 9-slot system unit that we propose, and it can power all flavors of core and MOS memory that we shall manufacture, except the MM11L. The MM11L will be exactly replaced by a new 8K core memory that is designed for the new backplane.

C. Simplification of the configuration rules, via the common backplane, will also significantly reduce and increase the utility of our inventory at all levels, including finished goods.

D. By thinking about and planning for a family of 16-bit processors that interchangeably fit into common mechanics, we are establishing a known cost for the introduction of product variations. The cost of this approach is to restrict the PIN OUTS of processor modules and to limit them to interfacing to peripherals and memory via the Unibus. The latter restriction already exists in the PDP-11 family. The former restriction, we believe, does not significantly add to our production cost for processors that consist of two or fewer hex modules.

E. As we know that backplanes are a significant factor in system reliability and require engineering that is in excess of their appearance, restricting the number of backplanes should be an advantage.

11/05 Processor Family

The PDP11/05 processor family will have at least 3 members in addition to the present CPU. They are described on notes by Bob Armstrong on the 4 following pages of this memo. The total engineering cost for the 3 processor modules alone is 422K in FY75. This does not include the cost of the backplane. power supply, or memories. However, these components would be designed and shipped independent of the processor modules. The ship date for the three products is shown on the schedule on Page 9b. You should note that there is a learning curve for introducing new modules just as there is for manufacturing. We believe that if the three modules were done in separate groups, the cost would be 600K rather than 422K in FY75. Also, note that 2 of the processors can be shipped in FY75.

digital INTEROFFICE MEMORANDUM

TO:

DATE: April 30, 1974

FROM: Bob Armstrong

DEPT: Small-11 Engineering

EXT: 4186 LOC: 1-3

SUBJ: 11/05 FAMILY

Low-Cost 11/05

The goal of this design is a minimal cost PDP-11 CPU that is instruction set compatible with the 11/05, with Power Fail/Auto restart and full Unibus control, but minus Serial Line control and Line Clock. The programmer's console is a Unibus option. Components used in the design should be all standard parts. Testing shall be an important design constraint with early evaluation on new module testers (GR) iterating the design. An IC count goal is 120 IC's allowing packaging to be on a single hi-density or two very low-density Hex modules.

Memory Management 11/05

With completion of the basic design of the low-end machine, we will begin work on an 11/05 expansible to 64 or possibly 128K of directly addressible address (memory) space. The CPU will use the optimized architecture of the low-end machine, also program compatible, using the same programmer's console and basic set of components as the low end. The layout shall expand to two Hex modules, the second module coupled to the first through intermodule connectors so that the pair can be substituted for a low-end processor. The memory management scheme should be supported by RSX11M. It may be a subset of the 11/40 memory management.

High-Speed 11/05

The third CPU of the 11/05 family is a high-speed version of the low-end CPU execution speed compatible with the 11/40. The constraints of the memory management CPU still remain; i.e., program compatible with 11/05, programmer's console is an option, use of standard parts, limit of two hex modules, plug compatible with the low-cost version. Hardware Multiply/Divide should be included, and EIS or FIS will be considered. Instruction speed shall be improved through look ahead fetches, wider and more effective microbranching, better data paths, and high speed components. The CPU will not contain a serial line or internal options other than Power Fail.

/sv

Summary and Schedule

MODEL: Low Cost PDP-11/05

GOALS: Minimize PDP 11/05 Entry Price, standard DEC components

ANNOUNCEMENT DATE: Target, September 1, 1975

DELIVERY DATE: January 31, 1975

FEATURES: Low cost CPU with Power fail/auto restart and full Unibus speed at least equal to 11/05.

Memory Size

Physical 28K

Virtual Same

I/O

Bandwidth (Unibus)

Buses Supported Unibus only

Multiprocessor Support No

Instruction Speed 2-2.5us for ADD R, R

Other enrichments Console sold as Unibus option

RELIABILITY:

CONFIGURATION: 1 or 2 hex modules, minimizing cost

COST: CPU ≈ $200

Prod. Mgr: Steve Teicher, x3175

Eng. Mgr:

Proj. Eng: Bob Armstrong, x4186

This CPU supports memory parity.

MODEL: Memory Management PDP 11/05

GOALS: Low cost 11/05 expendable to 64 128K memory

ANNOUNCEMENT DATE: Target, September 1, 1975

DELIVERY DATE: April 30, 1975

FEATURES: Low cost CPU with Power fail/auto restart, full Unibus, and memory expansion, management to 64-128K

Memory Size

Physical 28K

Virtual 64-128K

I/O

Bandwidth (Unibus)

Buses Supported Unibus only

Multiprocessor Support No

Instruction Speed 2-2.5us, for ADD R, R

Other enrichments Console sold as Unibus option

RELIABILITY:

CONFIGURATION: 2 Hex modules connected by intermodule connectors

COST:

Prod. Mgr:

Eng. Mgr:

Proj. Eng:

s CPU supports memory parity.

MODEL: High Speed PDP 11/05

GOALS: Low cost faster 11/05, speed ≈ 11/40

ANNOUNCEMENT DATE: Target, December 1, 1975

DELIVERY DATE: July 31, 1975

FEATURES: Low cost, faster 11/05 CPU with Powerfail/Autorestart, full Unibus, no internal options, hardware Multiply/Divide, speed approximately compatible with 11/40.

Memory Size

Physical 28K

Virtual Same

I/O

Bandwidth (Unibus)

Buses Supported Unibus only

Multiprocessor Support No

Instruction Speed lus. for ADD R, R

Other enrichments Console sold as Unibus option

RELIABILITY:

CONFIGURATION: 2 Hex modules connected by intermodule connectors

COST: CPU 0≃ 300-400

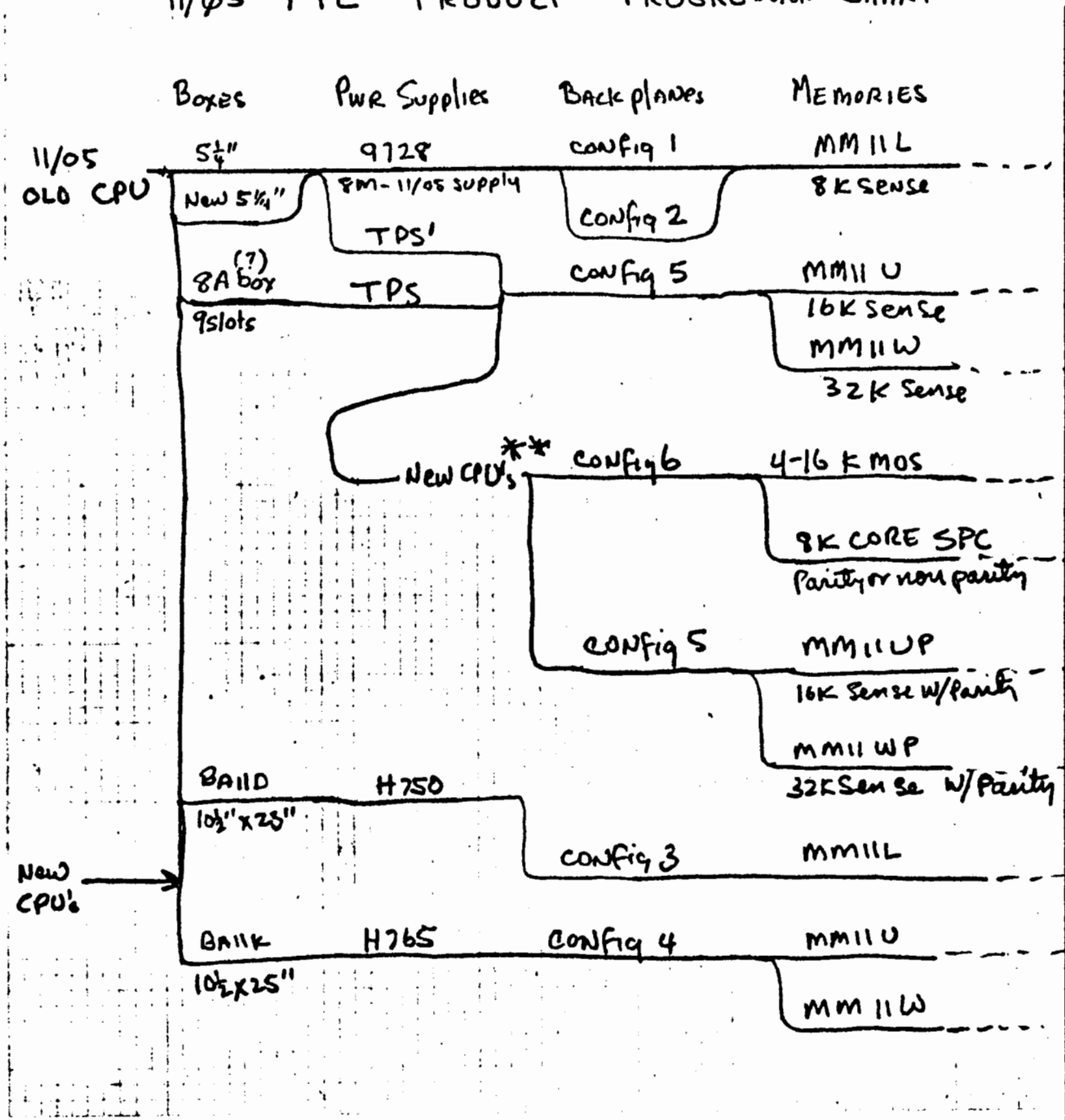
Prod. Mgr: Steve Teicher, x3175

Eng. Mgr:

Proj. Eng: Bob Armstrong, x4186

11/05 TTL PRODUCT PROGRESSION CHART

7/5/74



	Possible SHIP DATE	Cost of 4K unit	She Term Survivors
	6/72	1630	
		1800 TO 2000	
	Q2 75		
		2100 TO 2300	
	Q3 75		
		*	
	Q3-75		✓
	Q4-75		✓
	Q3-75		✓
	Q3-75		✓
		1721 TO 1861	
		2118 TO 2358	
	Q2-75		✓
		2468 TO 2710	
	Q3-75		✓

— * See TTL Series Summary —

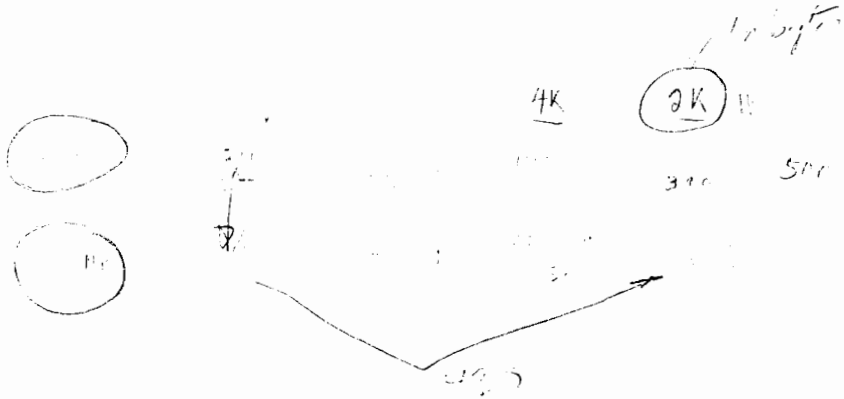
** All new CPU's respond to parity —

11/05 TTL Series Summary

Cost and Details of Basic Shippable Unit

Model	CPU	Box Metal Fans Slides	Power Supply	Memory 4K	Backplane	Console	Misc.	Total	# of SPC Slots	(In box) Max. Memory	Cost with Max. Memory	ADD R_1R	
11/05 KA 5¼" box Config. 2	350	60	130	522	100-150	90-110	308-378	1630	4	8K	1692	3.7 usec.	
11/05 HA 5¼" box Config. 1	350	60	130	522	100-150	90-110	308-378	1630	1	16K	2276	3.7 usec.	
11/05 MC 10½" box 23" length	350	129	222	522	100-150	90-110	308-378	1721-1861	3 sys units	28K[2]	3647-3787	3.7 usec.	1. Includes MM11-F 2. 16K fits in processor backplane 3. In addition to the processor, there is space for 3 system un
New Products													
11/05 16K sense 10½" box	350	Q2-75 130	390	16K min 750-850	100-150	90-110	308-378	2118-2358	3 SPC + 3 sys units	28K[1]	2468-2710	3.7 usec.	1. Assumes MM11W
Proposed Products Avail.													
11/05- 16K sense in old 5¼" box	350	Q3-75 60	TPS 155-165	16K min 750-850	100-150	90-110	308-378	1813-2063	3 SPC	28K[1]	2165-2415	3.7 usec.	1. Assumes MM11W
11/05 - low ball - CPU New box 4K MOS	168-190	Q3-75 35	155-165	4K min 403-229[3] 316 Avg.	60-120[2]	0	250-308	897-1221	6-7 SPC's	28K		2.5 usec.	1. Fewer modules should b easier to assemble 2. Backplane simpler 3. Average price should b reached 9 mos. after first shipment. Low price in 1976.
11/05 Memory management	300-350	Q4-75 35	155-165	4K min 403-229[3] 316 Avg.	60-120[2]	0	250-308	1029-1431	6 SPEC's	*		2-2.5 usec.	
11/05 High Speed	300-400	Q1-76 35	155-165	4K min 403-229[3] 316 Avg.	60-120[2]	0	250-308	1029-1481	6 SPEC's	28K		1-1.2 usec.	Gordon Bell would like high-speed machine to have floating point. Multiply Devide seems likely

*Address space = 128K, memory allotted 124K.
Max. memory in box 96K.



PROJECT SCHEDULE

PROJECT(S) LOW END - DETAIL
SHORT DESCRIPTION

BY P. ARMSTRONG
DATE 5/3/74

PROJECT SCHEDULE

BY
DATE

MONTH (½ Month per Block)	A	A	m	m	J	J	J	J	A	A	S	S	O	O	N	N	D	D	J	J	F	F	m	m
LETTER CODE FOR MONTH			Q	4	'74				Q1	'75														
CPU DESIGN	SYSTEM BLOCKS	MICRO-CODE, CC -	BRANCH-DETAIL	FINAL PRINT	MODIFICATIONS				ECO CONTROL															
SIMULATION					INPUT PRINTS	DEBUG - LOW LEVEL	CHANGES - DETAIL																	
PROTO	CIRCUITS	PIECES - (BR → BG)	INTEGRATE BLAST RUNS	DEBUG	RUN ALL DIAGNOSTICS SYSTEMS SOFTWARE																			
PC LAYOUT									1ST PASS		2ND PASS - LR													
MANUALS									BEGIN LOW END AND SYSTEM		PROOF - UPDATE PREPARE FINAL		PRINTING											
CONSOLE	Conceptual →	DESIGN - print set	wire wrap proto	LOW DENSITY LAYOUT																				
LOW END OPTIONS		SIMPLE DCII + RIMFIL BOOTSTRAP, PWR UP START																						
PROD START-UP											25 CPU'S FOR FIRST PASS - WIRES		FINAL TEST - INTEGRATE -		SHIP FIRST SYSTEMS									

DESIGN STEPS	System Design	Design	Layout	Assembly	Test	Pilot Assy.	Pilot Test	Producesign	Layout	Assembly	Test	Pilot Assy.	Pilot Test	Production
0 Start Design	1 Spec. & Sched. Done	2 Design Dwgs. Done	3 Start Assembly	4 Operate Proto.	5 Start Redesign	6 Limited Release	7 Operate Pilot	8 Acceptance 1st Ship.	2 Prodgn Rel. Done	3 Start Assembly	4 Operate Proto.	5 Start Redesign	6 Limited Release	7 Operate Pilot	8 Acceptance 1st Ship.	9 Prod. Release

*If "Test" ends with Accumulated Errors that require rework, appropriate design steps such as re-desid Errors that require rework, appropriate design steps such as re-design, relayout, etc. should be inserted until it is expected that "test" will terminate with Limited Releated until it is expected that "test" will terminate with Limited Release.

PROJECT SCHEDULE

PROJECT(S) MEM MANAGEMENT
SHORT DESCRIPTION

BY BOB ARMSTRONG
DATE 5/3/74

PROJECT SCHEDULE

BY
DATE

MONTH (½ Month per Block)	J	J	A	A	S	S	O	O	N	N	D	D	J	J	F	F	M	M	A	A	M	M	J	J
LETTER CODE FOR MONTH				Q1-15																				
MM. CPU	SPEC MM. FEATURES		BLOCKS - HOOKS TO CPU		FINAL PRINTS WITH MM		MODIFICATIONS																	
SIMULATION							ADD MM TO LOW END		DEBUG - LOW LEVEL		CHANGES DETAIL													
PROTO				BUILD LOW END WITH HOOKS			ADD M.M		DEBUG		RSX11M RT11													
PC LAYOUT											1ST PASS		2ND PASS - LR											
MANUALS											BEGIN MM SUPPLIMENT TO SYSTEM		PRINT											
DIAGNOSTICS											NEW DIAG. FOR M M.													
PROD START UP													25 CPUS (WIRES)		FINAL TEST -		FIRST SHIP							

DESIGN STEPS: System Design | Design | Layout | Assembly | Test | Pilot Assy. | Pilot Test | Production Design | Layout | Assembly | Test | Pilot Assy. | Pilot Test | Production

0 Start Design
1 Spec. & Sched. Done
2 Design Dwgs. Done
3 Start Assembly
4 Operate Proto.
5 Start Redesign
6 Limited Release
7 Operate Pilot
8 Acceptance 1st Ship.
9 Prod. Release
2 Design Rels. Done
3 Start Assembly
4 Operate Proto.
5 Start Redesign
6 Limited Release
7 Operate Pilot
8 Acceptance 1st Ship.
9 Prod. Release

*If "Test" ends with Accumulated Errors that require rework, appropriate design steps such as re-design, relayout, etc. should be inserted until it is expected that "test" will terminate with Limited Release.

*If "Test" ends with Accumulated Errors that require rework, appropriate design steps such as re-design, relayout, etc. should be inserted until it is expected that "test" will terminate with Limited Release.

PROJECT SCHEDULE

PROJECT(S) HI - SPEED CPU -

SHORT DESCRIPTION

BY [illegible]

DATE 5/3/74

PROJECT SCHEDULE

BY

DATE

MONTH (½ Month per Block)	O	O	N	N	D	D	J	J	F	F	M	M	A	A	M	M	J	J	J	J	A	A	S	S
LETTER CODE FOR MONTH		Q2-76																						
H.S. DESIGN	NEW DATA PATH MUL/DIV		MICRO CODE		FINAL PRINTS		MODIFICATIONS						ECO CONTROL											
SIMULATION							INPUT PRINTS		DEBUG															
PROTO							BUILD CPU		DEBUG		SOFTWARE													
PC LAYOUT												1ST PASS			2ND PASS									
MANUALS												BEGIN H.S. SUPP.			PRINTING									
DIAGNOSTICS												CREATE SPECIAL												
PROD START UP															25 CPUs (WIRES)		FINAL TEST - INTEGRATE			FIRST SHIP				

DEC 13-0001-1000-M1171

DESIGN STEPS	System Design	Design	Layout	Assembly	Test	Pilot Assy.	Pilot Test	Production	Design	Layout	Assembly	Test	Pilot Assy.	Pilot Test	Production
	0	1	2	3	4	5	6	7	8	2	3	4	5	6	7	8	9
	Start Design	Spec. & Sched. Done	Design Dwgs. Done	Start Assembly	Operate Proto.	Start Redesign	Limited Release	Operate Pilot	Acceptance 1st Ship.	Prod. Rel.	Design Done	Start Assembly	Operate Proto.	Start Redesign	Limited Release	Operate Pilot	Acceptance 1st Ship.	Prod. Release

*If "Test" ends with Accumulated Errors that require rework, appropriate design steps such as re-design, relayout, etc. should be inserted until it is expected that "test" will terminate with Limited Release.

*If "Test" ends with Accumulated Errors that require rework, appropriate design steps such as re-design, relayout, etc. should be inserted until it is expected that "test" will terminate with Limited Release.

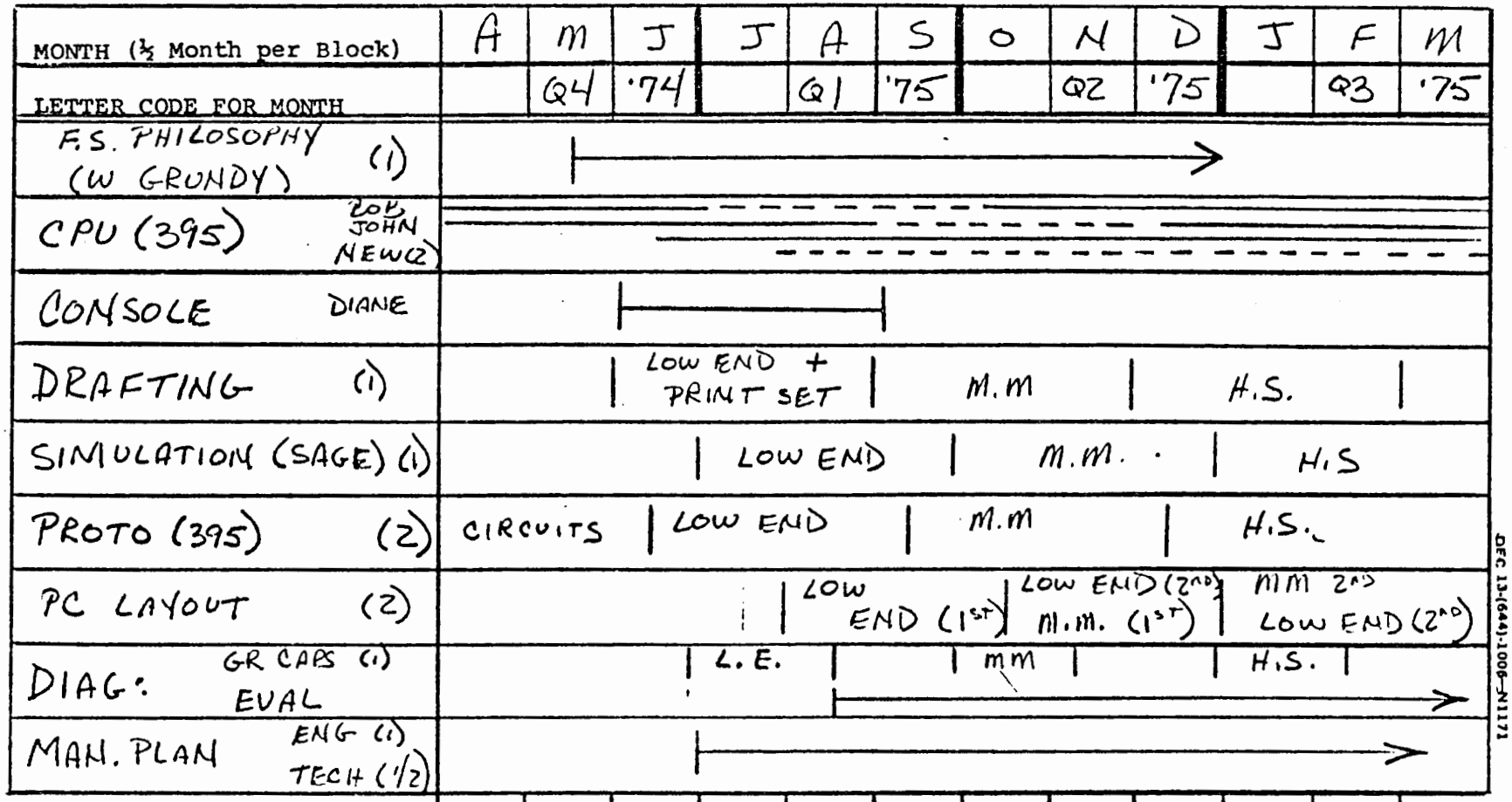
PROJECT SCHEDULE

PROJECT(S) 11/45 SERIES (FAMILY)

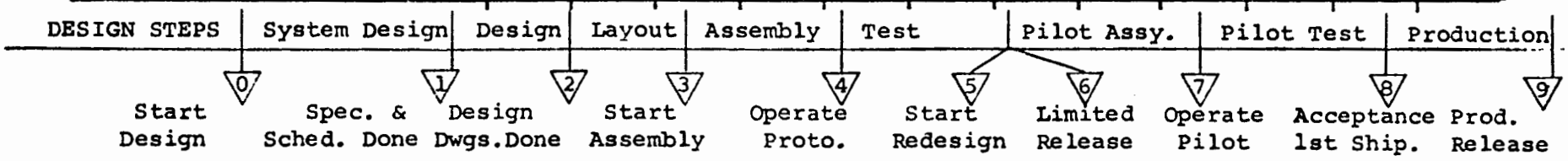
SHORT DESCRIPTION PEOPLE CHART

BY BOB ARMSTRONG

DATE MAY 3, 1974



DEC 13-(664)-1006-N1171



*If "Test" ends with Accumulated Errors that require rework, appropriate design steps such as re-design, relayout, etc. should be inserted until it is expected that "test" will terminate with Limited Release.

PROJECT SCHEDULE

PROJECT(S) 11/45 SERIES — BY Bob Armstrong

SHORT DESCRIPTION PEOPLE CHART — DATE 5/3/74

MONTH (½ Month per Block)	A	M	J	J	A	S	O	N	D	J	F	M
LETTER CODE FOR MONTH		Q4	'74		Q1	'75		Q2	'75		Q3	'75
MODEL SHOP								10			10	
INF. SERVICES						→						
R PLATZ - Reliability								LOW BALL + SYSTEM (2)			mm	H.S.
MANUALS (1)						SYSTEM MANUAL LOW END CPU		MM			H.S.	

DEC 13-(6441)-1006—N1171

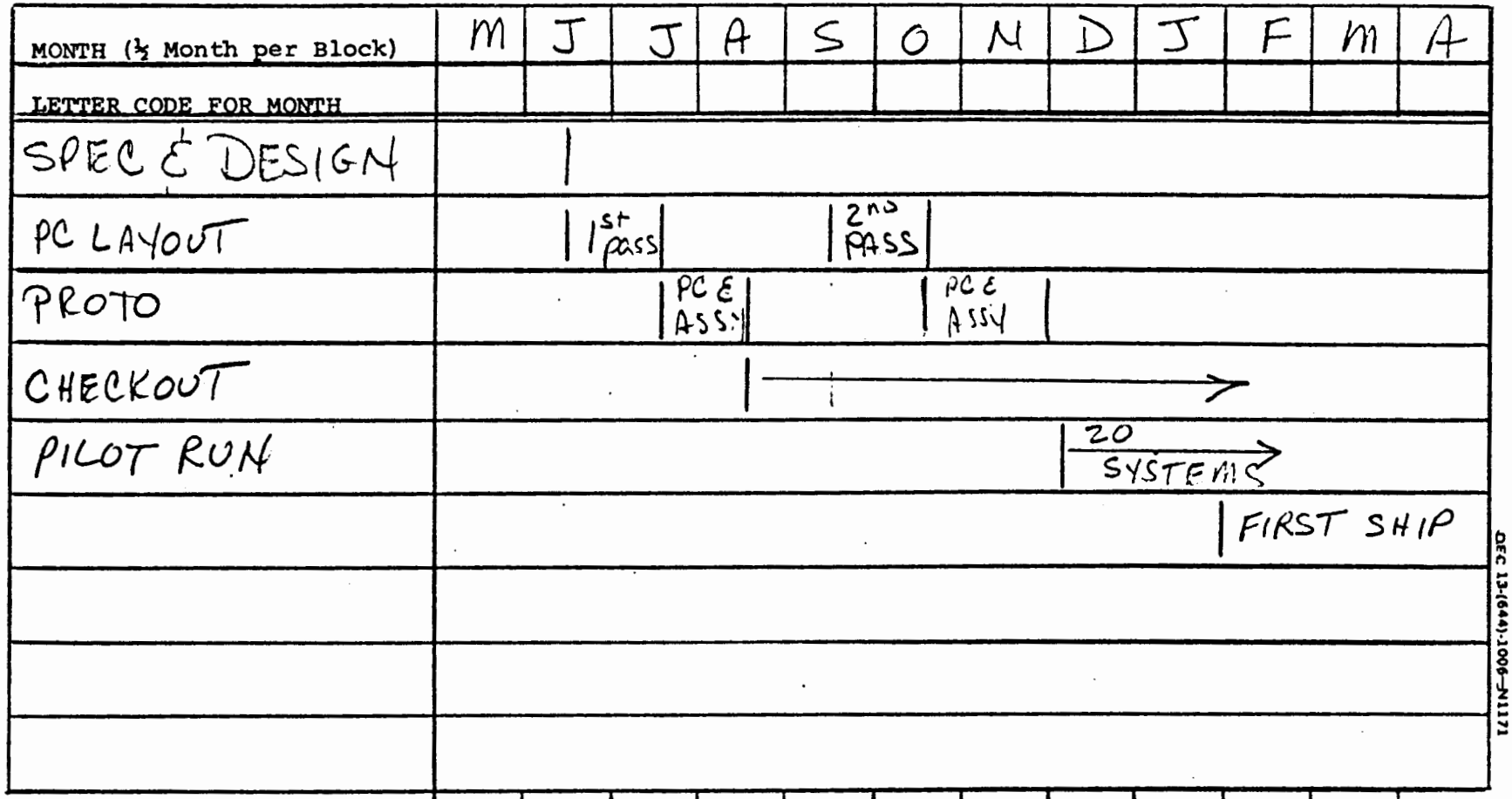
DESIGN STEPS	System Design	Design	Layout	Assembly	Test	Pilot Assy.	Pilot Test	Production
	0	1	2	3	4	5	6	7	8	9
	Start Design	Spec. & Sched. Done	Design Dwgs. Done	Start Assembly	Operate Proto.	Start Redesign	Limited Release	Operate Pilot	Acceptance 1st Ship.	Prod. Release

*If "Test" ends with Accumulated Errors that require rework, appropriate design steps such as re-design, relayout, etc. should be inserted until it is expected that "test" will terminate with Limited Release.

PROJECT SCHEDULE

PROJECT(S) MOS MEMORY — BY DAVE CANE

SHORT DESCRIPTION — DATE



DESIGN STEPS | System Design | Design | Layout | Assembly | Test | Pilot Assy. | Pilot Test | Production

0 Start Design
1 Spec. & Sched. Done
2 Design Dwgs. Done
3 Start Assembly
4 Operate Proto.
5 Start Redesign
6 Limited Release
7 Operate Pilot
8 Acceptance 1st Ship.
9 Prod. Release

*If "Test" ends with Accumulated Errors that require rework, appropriate design steps such as re-design, relayout, etc. should be inserted until it is expected that "test" will terminate with Limited Release.

Memory Strategy

MOS 4K RAM's will most likely be available for shipment in product in Calendar 1975. We currently have purchase orders for 100,000 parts on the books of Texas Instruments and MOSTEK. We presently believe that MOSTEK will deliver in excess of 30,000 parts in 1974 and that they can deliver sufficient quantity for our use in 1975. I have absolutely no confidence in Texas Instruments, but this may be a personal prejudice.

Currently, Dave Cane from Memory Engineering, is designing an MOS memory that interfaces to the Unibus. His cost estimate for 4, 8, and 16K by 18 memories with parity is as follows:

	4Kx18	8Kx18	16Kx18
Control circuits	46	50	58
Printed cir card	27	27	27
Assembly	10	15	17
Testing	15	15	20
Repair	20	20	30
Sub Total	118	127	152
RAM's 1975 price (15.69-11.58)	282-208	564-416	1129-833
Incoming Inspection	3	7	14
	403-329	698-550	1295-999

The above costs for MOS memory assume that Texas Instruments does not deliver in 1975. If TI delivers and their price towards the middle of 1975 approaches their original quote of $8 per chip, then the prices will be as follows:

	4Kx18	8Kx18	16Kx18
MOS Memory System at $8/chip	265	446	742

MOSTEK's Berry Cash believes that, during the second half of Calendar 1976, 4K RAM's would sell to companies such as DEC for $6 per chip.

	4Kx18	8Kx18	16Kx18
MOS Memory System at $6/chip	229	350	598

Peter Durant's estimate for the new 8K optimized cost effective core memory is as follows:

	$		$
4K x 16	495	4K x 18	557
8K x 16	520	8K x 18	582

The existing MM11U costs approximately $750.00. All of the above core memories require 75 watts or more, while MOS requires under 20 watts for up to 16K x 18.

Using the worst case price of $15.69, which is the average price that MOSTEK will quote over the first 100K parts, the 4K MOS memory with parity is approximately $90 lower in cost than the equivalent DEC 4K core memory without parity. If TI should deliver at $8 per chip, then we will be in trouble at 8K and in the latter half of 1976 even 16K core will not be cost effective.

We could pray that MOS memory is delayed, but I do not believe that we can bet our memory business on MOSTEK's and TI's combined failure.

Stretch Core Technology

We intend to stretch core technology as far as it will go in the PDP 11/05 series. The MM11U, 16K sense, and MM11W, 32K sense, memories are both more cost and space effective than the MM11L. In addition, we have reason to believe that the new memories will be more reliable than the MM11L. The MM11U, MM11W, and the new 8K core, all use the same power supply voltages. A comparison is shown below:

	Size	Form Factor	Power Supply Voltages
MM11U	16K x 16(18)	43 hex 1 quad	+20, -5, +5
MM11W	32K x 16(18)	3 hex 1 quad	+20, -5, +5
New 8K	(4)8K x 16(18)	1 hex } mother 1 quad } daughter card	+20, -5, +5

The new 8K memory is designed to plug into our new common backplane, while the MM11U and MM11W require dedicated backplane wiring. The TPS power supply being designed for the 11/05R will power any of the above memories. Geoff Potter knows that this is his job.

MEMORY, BACKPLANE, POWER SUPPLY

MIX AND MATCH TABLE

Backplane	Use	Memory Types	Other
11/05 config 1	5¼ inch 05 box	Up to 2 MM11 L's	1 SPC slot
11/05 config 2	5¼ inch 05 box	1 MM11 L	3 SPC slots
11/05 config 3	10½ inch 05 box	2 MM11 L's	0 SPC slots
11/05 config 4	10½ inch 05 box	1 MM11U or 1 MM11 W	3 SPC slots
		NEW	
11/05 config 5	5¼ inch 05 box	1 MM11U or 1 MM11W	3 SPC slots
11/05 config 6	Any box	Up to 32K of new 8K or 96 K of MOS per backplane	Memory plugs into SPC slots. 05 processor plus 16K of MOS occupies up to 3 of 9 slots; General system could have have 6-7 SPC devices.

Power Supplies

Config 1, Config 2	54-09728 regulator
Config 3	H750
Config 4	H765
Config 5, Config 6	TPS, TPS', or H765

TPS' = TPS circuits on different etch board. This is required to fit TPS type of supply into the 11/05 5¼ inch box.

Cost Comparisons

CPU Module cost comparisons:

Present 11/05	$
M7260	181
M7261	169
	350
11/40 Basic	
M7231	125
M7232	108
M7233	99
M7234	104
M7235	95
	531
Memory Mgmt. M7236	153
EIS M7238	162
FIS M7239	59

11/45 Basic	$
M8100	301
M8101	256
M8102	195
M8103	301
M8104	258
M8105	120
M8106	203
M8109	246
M8116	79
	1,959

Confidence in Price & Specifications	Proposed	Space	Equivalent 11/40	Space
90%	05 Low Ball	168-190 1 slot	531	5 slots
60%	05 Memory Mgmt.	300-350 2 slots	684	6 slots
60%	05 High Speed	300-400 2 slots	531-752	5-7 slots

When the above chart lists the equivalent 11/40 CPU modules, the word equivalent needs some definition. The 05 Memory management CPU will not be the full KT11. The memory management circuit in the 05 will be essentially whatever fits in 35 IC's that allows the 05 to address 128K of memory. We shall consult with the Software group in an attempt to have RSX11M "support" the reduced memory management scheme. Craig Mudge claims that he can specify a subset memory management that costs less than $50 to implement.

Taken from Teitelbaum.

IV. The Effect of LSI

Let there be no doubt that LSI and microprocessors will have a major effect on the low-end 16-bit computer market. For instance, one of our bigger 11/05 customers, Motorola, has informed us that they intend to use their own M6800 microprocessor chips to essentially replace the 11/05 in their hotel reservation system. They claim to have working prototype systems using the LSI chips at their plant in Phoenix.

Without additional data, I would bet that in 3-5 years up to 80% of the Iron OEM customers would purchase microprocessors instead of our TTL 11/05's. I don't believe that we can salvage a significant portion of this market simply by mounting LSI processor parts and MOS memory in our traditional PDP-11 systems. The attack of LSI is far too pervasive throughout the processor, memory, and peripherals, to be staved off by clumsy implementations such as we had planned in the 11/05R.

As I mentioned earlier, our computers, peripherals, and even our software is designed around TTL-SSI technology. For instance, many of our diagnostic programs depend on the existence of the lights and switches console. The console is clearly very costly when the entire processor is buried in a VT51. Someone in Field Service has suggested that we implement the console in logic, which is an added cost to every machine, to avoid the one time charge of changing diagnostics. In fact, when we speak of traditional diagnostics, we are still thinking in terms of TTL-SSI systems. Processors are already selling for under $1000. The HP-65 sells for $700. Does anyone doubt that the HP65 is repaired only at depots? Processor modules will also only be repaired at depots.

The same Field Service memo that mentioned using logic to emulate the switch register also noted that there are about 50 old diagnostics of interest to the 11/05. I argue that for the size systems that are of interest to the LSI-11, 4 or 5 diagnostics must suffice and that these will have to be newly written to deal with the LSI peripheral controllers.

Everyone who has touched a BOWMAR or HP calculator should believe that LSI technology exists. The HP-65 is a stored program computer with magnetic card storage. The Motorola M6800 is a flexible, building block chip set in the tradition of the PDP-11. The Rockwell SOS process will allow dramatic speed improvements for microprocessors. RCA is planning an SOS processor that will outperform the 11/05 and probably the PDP8E. Using SOS memories, it should be possible to build a 32K x 16 memory that dissipates approximately 10 watts and that has roughly a 200μsec access time.

LIFE IN THE JUNGLE

Should We Now Abandon the PDP 11

I believe that there are many approaches for integrating LSI into the DEC product plan. Lorrin Gale has proposed the SX24. He states that the SX24 will be 1/2 price and twice the performance of any PDP-11 when interfaced with mass storage, communications, printer, and memory.

In order to pursue this argument, I need to list the chip counts for the interfacing of the WD chips to the Unibus.

Function	# of IC (or equivalent)	Cost	
WD Chips	4 (+1 for EIS/FIS)	$ 90.00 (Avg.)	
Clock Circuitry	8	15.00	
WD Bus Buffer	4	5.00	
UB ADDRESS DATA REG DR/REC	17	15.00	
Power Fail	8	4.00	
UB Control DR/RCVRS	15	6.00	
PSW ADDRESS DETECTION	5	4.00	
UB BR/BG Arbitration and Control	12	7.00	
NPR/NPG	4	1.00	
	73 + 4 WD Chips	147.00	Including WD set.
		+ 17.00	EIS/TIS
		164.00	

Hardware, to execute the entire PDP-11 instruction set including EIS and FIS, with the exception of the capability to directly address the PSW and switch register, requires only 18 of the above 73 devices in addition to the 4 LSI chips. While it is certainly possible to program other instruction sets in the LSI, chips, it is a mistake to assume that other instruction sets are simpler to implement without careful examination. Today's 11/05 processor requires 200 IC's to implement the CPU, Power fail, Serial line, Line clock, 4-level interrupts, and the hooks for multiprocessors. The TTL 11/05 low-ball processor, proposed by Bob Armstrong, will require between 120 and 130 chips for the CPU, power fail, and 4-level interrupts, The PDP 8A CPU requires 113 chips.

Proposal Is to Change Bus Structure but Retain Instruction Set

As I have just attempted to illustrate, the Unibus interface is a costly item with the WD chip set. This is likely to be a characteristic of the Unibus with almost any LSI implementation because:

1. The Unibus has 56 signal lines, and the equivalent performance can be obtained with fewer signal lines and hence fewer IC pins.

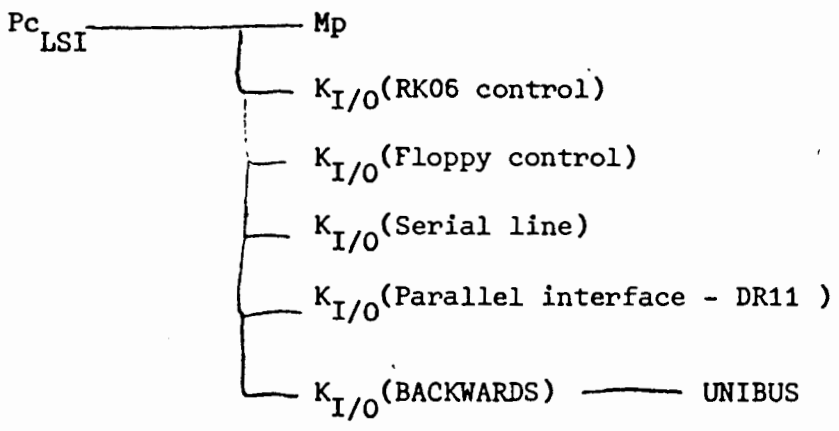
2. The Unibus is designed to operate with extended systems of many cabinets. The drive necessary for this is not required in most systems constructed entirely with LSI chips. Furthermore MOS, the best technology for LSI, has very limited drive capability.

3. The basic protocol of the Unibus is inefficient when operating with memories. For instance, on transfers of DATA to memory, MOS memories can accept the address long before they can accept DATA. The Unibus protocol displays address and data simultaneously, which effectively wastes time and bus lines. Time is wasted because the processor has to wait for the data to be accepted by the memory before proceeding. If the address could have been displayed earlier than the data, then the memory would be ready to accept data sooner than if the address and data were displayed simultaneously.

4. The interrupt structure of the Unibus is designed to operate with reasonably large systems.

5. Etc.

We believe that we could build a PDP-11 system minus Unibus that could run much of the present RT11 and RSX11M software. Such a system would resemble The diagram below:



The $K_{I/O}$ (BACKWARDS) would be an option similar to the DW8E It would permit the use of some limited set of Unibus peripherals with the new machine. The only reason that I suggest altering or changing the Unibus is that we can now demonstrate that LSI is not ammenable to the wide Unibus. I do not suggest that this approach makes sense for a TTL - SSI machine in order to reduce cost. To believe that any 16-bit machine will occupy less chips than the PDP-11, one has to thoroughly understand the design. For instance, the 12-bit simple PDP-8 is not signifcantly smaller than the 16-bit complex PDP-11.

It is interesting to note that the 11/44 group has developed a screaming fast PDP-11 implementation that depends upon scrapping the Unibus as the main memory attachment. Furthermore, the projection is that the 11/44 will not be larger than the 11/40 CPU.

I will admit that if we were building our first 16-bit processor in 1974, we probably should not choose a PDP-11. However, today we have built and shipped 5 PDP-11's and have designed at least twice that many. Bob Armstrong has designed 4 PDP-11's himself. You were not aware of it, but there have been two vastly different PDP-11/05's shipped during the past two years. If we complete our development plans, Bob will complete 3 more PDP-11 designs during FY75. Thus far, Bob has made significant progress on each redesign. The difference between # 4 and # 5 is that # 5 contains fewer chips and has twice the performance of # 4.

Let's Have a Contest

Lorrin has proposed a computer system with limited expansion capabilities. I propose that we attempt to use the same ground rules in examining the PDP-11. We simply need to fill in the chart below:

	# Chips	Cost	Fortran Benchmark
PDP-11 like system that runs RT11 with 3 man-months of software mods			
SX24 system with same peripherals as above			

My contention is that the PDP-11-like system will be close to the SX24 in performance and cost. Furthermore, we know enough about PDP-11 features that we can evaluate trade-offs where the SX24 would be a new ball game. If the SX24 was a 32-bit machine it might make more sense.

Please understand that the PDP-11-like system may require new peripheral controllers to be competitive in cost to the SX24, but this is indeed how the SX24 gets its low cost.

A Plan for Action

We intend to do the following:

0. Implement an interface between the WD chips and the Unibus that enables the chips to run system software with as few modifications as possible.

1. Define several other interfaces between the WD chip set and the Unibus. Each of these would have different performance characteristics and different incompatibilities with the PDP-11 of today. For each of these, we need a software modification cost, a performance measure, and a production cost for hardware.

2. Define a system with the WD chips that includes memory, serial interface, and a floppy interface. For this we need to estimate software implications, controller production cost, controller engineering cost, system cost, and system performance.

3. Define an option for the above system that interfaces to Unibus peripherals.

4. Define a system of chips in another technology, possibly SOS, that is compatible with the WD bus. This system of chips will include peripheral controllers.

5. Along with Roy Moffa, I propose to define a module motherboard in which the daughter board options are the LSI chips that get defined in Number 4.

6. Along with Ed Correll and Tom Stockebrand, I propose to define a system that includes LSI processor buried into terminals.

I believe that the above work can be substantially planned by August 1974, and that profit from pieces of the project should be realized in FY76. For instance, as a tool we might succeed in extending our low-end markets. We shall succeed if the development and manufacturing capability that we possess is coupled with intelligent planning and good marketing.

Thank you for your attention.

APPENDIX A

How Is My Strategy Reflected in Our Development Budget

Our group has collectively prepared a budget that covers:

	Amount	% of Total
1. Support of existing products and integration of memories, power supplies, and boxes	505K	22
2. Development of TTL processor series	422K	19*
3. Continued work with Western Digital and further LSI system development	1076K	48
4. As yet not identified but expected	200K	9

*My attitude is that we cannot yet abandon the development of products for the customers who will buy almost $70M during FY75. Furthermore, I firmly believe that we will require a cooperative effort by several groups to smoothly guide the transition. I suggest the following roles for the coordination of various engineering efforts during FY75.

Function	Functional Manager	Product Manager	Project Engineer	Production Manager
1. Specification of chip set systems. Development of at least 1 general purpose NAKED module. Coordination of basic software modifications with hardware Responsibility for generation of Incoming inspection procedures and module test.	Steve Teicher	Ed Steinfeld	Dick Spencer	George Bundy
2. Completion of WD chip set and development of 1 Unibus module and 1 non-Unibus module. Coordinate with above.	Steve Teicher	Ed Steinfeld	M. Titelbaum	George Bundy
3. Integration of LSI chip set system into LA36	Ed Correll	-	-	-

Function	Functional Manager	Manager	Project Engineer	Manager
4. Integration of LSI chip set system into VT51	Russ Doane Tom Stockebrand	Bob Anundson	Ken Fine	-
5. Development of additional NAKED module systems	Roy Moffa	Mike Gutman	-	-
7. Development of Multidrop chip specification	Vince Bastiani			

Function	Functional Manager	Circuit Eng.	Simulation Manager	Vendor Manager	Layout Manager
8. Actual chip implementation by best available means. Includes logic design, circuit design, simulation, etc.	Lorrin Gale	-	Bob Kusik	-	-

An important question to be asked is: "Why am I proposing to continue with any TTL development when microprocessors are just around the corner?" I believe the answer is that many of our customers are also being surprised by the rapidity of the turn-on to LSI. Both they and we would like to buy time to manage the transition in an orderly manner. By investing roughly 18 to 20 per cent of our low-end development funds in continuing TTL-MSI system development, we should be able to offer more price/performance attractive products to our current customers while we develop LSI products.

APPENDIX B

digital INTEROFFICE MEMORANDUM

TO: Steve Teicher

DATE: May 8, 1974

FROM: Mike Titelbaum

DEPT: Small-11 Engineering

EXT: 3175 LOC: 1-3

SUBJ: Small 11's With the WD Chip Set

Overview

Over the past few months, by using the Mimic simulator we have determined that the WD chip set can be a good emulator of the 11 instruction set. By using the Fortran instruction mix analysis developed by Bill Strecker, we have been able to do performance comparisons between the WD based machine and the existing 11/05. By comparison, the WD machine can be overall from 5 to 25% slower than the existing 11/05 depending upon the configuration in which we put it. The attached Table 1 prepared by Duane Dickhut summarizes the instruction execution times with discussion about configuration. Later, I will detail the cost implications of these configurations.

The WD configuration with 1K words of control ROM will be able to execute the basic 11 instruction set, including 11/40 instructions. Microcode for EIS/FIS has been written allowing the WD machine to execute these 11 instructions 2 to 5 times faster than an equivalent software routine on the 11/05 (See attachement). The Microcode for EIS/FIS can be contained in 512 ROM WORDS (1 chip).

Initial Designs

Our original thinking was to design the WD chip set into a system consisting of:

	Chip Count	Cost (Chips)
8K x 18 MOS MEMORY	67	$ 432.00 @ 12.00/4K chip
MOS MEMORY Parity Controller	32	
Serial Communications Line	30	$ 100.00 (AVG. .70/chip)
Line Clock	10	
Unibus Interface	72	
WD Chips & Support (1 chip set)	20+	$ 100.00

At the time, we believed that this configuration could be designed into a module system consisting of one hex board with two daughter boards containing the MEMORY System and WD chip set, respectively. After going through the detailed design of the above system, we concluded that:

1. The only item that could be unbundled from the above would be the memory array card.

2. We could probably not layout a hex module with 142 16 pin equivalents as described above.

3. The system without integral memory and just the WD chip set, SCL, LC, would not satisfy the low-end market for raw iron machines.

4. We would be trying to incorporate at one time two new technologies--WD Chip Set/4K x 1 RAM which had high risk. If one technology failed, we could not profit from the success of the other.

Where We Are

Given that we wanted to unbundle the WD chip set from the memory and peripherals and still be able to replace the existing 05, we have looked at a design that:

1. Minimized the number of chips necessary to have the WD chip set execute PDP-11 instructions and communicate with Unibus peripherals.

2. Minimized the cost of the above system without greatly affecting the performance of the system. Our goal is still to execute instructions not less than 20% of 11/05 speed.

The issues we now face revolve around the compatibility features of a WD chip set machine not in the instruction execution areas but in talking to the Unibus and coping with Unibus compatibility features. We have examined and tried to justify each feature on the basis of cost, chip count, and its impact on existing software and hardware systems.

Below is presented the data from our current design and the approximate chip cost for each feature.

Function	# of IC (or equivalent)	Cost	
WD Chips	4 (+1 for EIS/FIS)	$ 90.00	(Average)
Clock Circuitry	8	15.00	
WD Bus Buffer	4	5.00	
UB ADDRESS DATA REC DR/REC	17	15.00	
Power Fail	8	4.00	
UB Control DR/RCVRS	15	6.00	
PSW ADDRESS DETECTION	5	4.00	
UB BR/BG Arbitration and Control	12	7.00	
NPR/NPG	4	1.00	
		147.00	Including WD set.
		+ 17.00	EIS/FIS
		164.00	

I have about 90% confidence in these numbers, since I believe that they can be reduced by 5 or 10% by minimization; but there are still no features that have been included to facilitate testing. The design as described in the previous table corresponds to configuration 4 on the attached performance table. The table indicates that this machine will be approximately 20-25% slower than the existing 11/05 using core or MOS memory on the Unibus.

If we break down the numbers from the previous table, we find that approximately half of the 73 chips are comprised of holding registers and drivers as well as receivers for Unibus signals. This is the price we have to pay to talk to the Unibus. (About 25% are used to perform BR, NPR arbitration and control and powerfail. The other 25% is used to buffer and control the WD chip set.)

The additional feature of hardware error detection of Unibus errors, such as DATA time out and odd address errors, is not included in the previous table. We believe it will cost us about 8 to 10 chips and approximately $4 more. If these errors occur in the system as presently designed, there will be no trap generated.

We are looking at the features of the machine closely to determine their impact on system sofware. RT-11 and RSX-11M could run on the previously described minimal machine with about three to six man-months in software modification. We are trying to determine as best as we can the tradeoffs that can be made. For example, the PSW address detection circuitry can be removed, and access to the PSW can be implemented through the addition of an SPL instruction that sets or clears the priority level in the PSW directly. This would save 5 chips from the minimal design and cost essentially nothing, since it could be implemented in microcode. The cost of this change, though, would be realized in changes to existing software, both ours and our customers'. It is this cost of incompatibility that we are investigating.

We also now have sufficient simulation data to be able to ask how sensitive the low-end market is to price and performance. For example, we can add additional Microcode (1 more ROM @ $17.00) to speed up double operand instruction by 900 nsec. We may also be able to squeeze the Microcode down to one ROM chip and sacrifice performance by 30 to 50%. I believe, though, that these performance questions can only be accurately answered once we have received devices from WD and examined their performance characteristics, since WD has yet to run their first wafers.

Where To Go From Here

Western Digital has slipped their original schedule which indicated that we would have prototype devices here last February. They are now in the process of generating the Masks for the Data chip and will have working plates for the other two devices by the second week in June. According to the latest schedule received from Steve Stuart dated May 6, WD plans to have functional prototype sets running by September 15. Also, according to the schedule attached, we can have 100 functional sets in house by October 15. We will probably see the first chip in early July.

This slippage has forced us to look very closely at many items that we previously had underestimated. For example, I believe both WD and ourselves have not yet realized the full extent of device testing that will be required. Our own efforts on a hardware simulator for chip evaluation will not be available until mid-June. We now have the opportunity to simulate at the gate level our Unibus interface design and be able to utilize the results of the simulation to make design changes before releasing the module. The additional time has allowed us to run systems software on the RT simulator to further verify our microcode and make system performance measurements with simulated Unibus peripherals

The additional time will allow us to design the system for a higher reliability than we have previously experienced. We are going through the analysis now of WD's process and will have DEC's test pattern wafers, processed by WD, here for analysis by the end of the month. With the data gathered from the existing 11/05 reliability study done by Rich Olsen, as well as the process analysis, we should be able to increase the reliability of the 11/05R by at least a factor of two to three.

Our plan for the WD chip set will be as follows:

1. We should continue our present minimal design for a one Module CPU that executes the 11/40 instruction set including EIS, FIS and runs RT-11 and RSX-11M. This design will allow us to evaluate in a system environment the WD chip set. It will give us a CPU that we can build for under $200 and also sell in the naked market.

2. The above implies that we continue our efforts in developing and using the tools for chip and board evaluation.

3. Using the WD chip set as a base design, incorporate it into a system that may not utilize the Unibus. This system may have additional LSI controllers and could be buried in terminals, analog frontend systems, or in dedicated applications gear.

11/05R Performance (Microseconds)

	Present 11/05	Config #1	%	Config #2	%	Config #3	%	Config #4	%
MOV R,R (010001)	3.1	2.7	+13%	3.3	-06%	3.6	-16%	3.6	-16%
MOV (R),R (011001)	4.6	3.6	+22%	4.2	+09%	4.8	-04%	4.8	-04%
MOV R,(R) (010011)	6.1	4.5	+26%	5.1	+16%	5.7	+07%	5.7	+07%
MOV A,B (016767)	9.5	9.3	+02%	9.9	-04%	11.4	-20%	11.4	-20%
ADD (R),R	4.6	3.6	+22%	4.2	+09%	4.8	-04%	4.8	-04%
BR (made)	2.6	2.7	-8%	2.7	-8%	3.0	-15%	3.0	-15%
(not made)	1.9	2.7	-42%	2.7	-42%	3.0	-58%	3.0	-58%
Overall Speed Estimate (According to Fortran Instruction Mix)		-3% to-5%		-10% to -15%		-20% to -25%		-20% to -25%	

onfig #1: Old Design stopping clock, updating PSW only when needed, internal memory.

Config #2: No clock stopping, T.I. memory chips, internal memory, updating PSW after every instruction.

Config #3: No clock stopping, Mostek memory chips, internal memory, updating PSW after every instruction.

Config #4: No clock stopping, Unibus memory, updating PSW after every instruction.

Config. #3 to #4 are equivalent performance-wise. All times based upon 300ns WD micro-cycle.

EIS/FIS 05/05R Comparisons (Time in usec)

	05 (Software)	05R (Microcode)
Floating Point		
ADD	388	100
MULT	831	120
DIV	1110	150
Integer		
MULT	300	75
DIV	400	120

DEC MICROPROCESSOR SCHEDULE

ip Description	WDC Part No.	Working Plates	First Wafers	12 Functional Sets*	100 Functional Sets	1000 Functional Sets
DATA	CP1611B	May 12, 1974	June 7, 1974	September 15, 1974	October 15, 1974	December 15, 1974
CONTROL	CP1621B	June 6, 1974	June 30, 1974	September 15, 1974	October 15, 1974	December 15, 1974
MICROM	CP1631B	June 9, 1974	June 30, 1974	September 15, 1974	October 15, 1974	December 15, 1974

*Assumes one iteration of all designs

SBS May 6, 1974

MODEL: PDP11/05R REVISED TO: April 30, 1974

GOALS: To incorporate LSI technology to reduce the cost and increase the reliability of an 11/05 type processor on a single hex module.

ANNOUNCEMENT DATE: October 31, 1974

DELIVERY DATE: Target, April 30, 1974

FEATURES:

Memory Size

Physical 28K (31K with special memory)
Will be able to use 4k or 8k MOS or 4k or 8k core.

Virtual Same

I/O

Bandwidth

Buses Supported Unibus Only

Multiprocessor support

Instruction Speed - 3.7 usec - 4.0 usec for Add R, R

Other enrichments - EIS/FIS optional as an additional ROM
Serial line device replaces lights and switches console

RELIABILITY: factor of 2 to 3 better than existing 11/05

CONFIGURATION: 5¼" package: space for between 6 and 8 boards with SPC pinning. Programmers console is extra.

COST: Target cost is $948 for 4K (going down to $700 by 1/77)
$1098 for 8K. (Subtract $100 from each for no battery backup)

Prod. Mgr: Steve Teicher

Engr. Mgr: Steve Teicher Ext. 3175

Proj. Engr: Mike Titelbaum Ext. 3477

digital INTEROFFICE MEMORANDUM

NOV 02 1973

TO: Lorrin Gale

DATE: October 31, 1973

FROM: Jim O'Loughlin

DEPT: Micro Products Development

EXT : 5455 11-2

SUBJ: LOW TO HIGH END - NEW PDP-11/40
(FIRST DRAFT - Add Comments as Desired)

Probable characteristics of a new PDP-11/40 machine are presented. The machine is ordered toward a high performance/price ratio and would exist in two configurations

The processor, common to both configurations, would operate at PDP-11/40 speed or greater and would have an integral EIS instruction set (slower than PDP-11/40 as extra data paths would not be provided). The minimum processor requires larger (more words) control store, the LSI'ing of IR DECODE and UNIBUS CONTROL, and Unibus Control ordered toward cache memory and a usual release of the Unibus rather than acquisition as in the present PDP-11/40. Basic processor speed would exist in the minumum processor set, some cost advantages would occur because of fewer modules. The low cost situation is left to the new PDP-11/05 machines. A major increase in speed occurs as a function of the cache memory for the high end machine.

This PDP-11/40 postulation does not address itself to the 32 bit PDP-11 question except to make it an option in the system configuration, and unavailable on the minimum configuration. Really feel, however, that 32 bitness even as an option, might compromise low cost. But is a 16 bit PDP-11 competitive against a 32 bit machine?

Distribution List:

Gordon Bell	Chuck Kaman
Jack Burness	Bob Kusik
Roger Cady	Rony Elia-Shaoul
Jim Beatty	Mike Titelbaum
Bob Gray	Len Hughes

Low To High End - New PDP-11/40
(First Draft)

Configuration 1. Minimum

- three hex modules for processor
- no lights and switches console, use integral UART with pad console terminal, no DL11 cost in basic system
- minimum back panel that might specifically exclude high performance options such as FIS, User Microprogramming or Cache Memory
- minimum box (probably 10½) with inexpensive power supply (we usually lose here)
- self diagnostic capability might exist to isolate one of three modules or at least indicate that a load operation can properly occur from the console terminal.
- integral,slow EIS instructions using existing data paths and extra words in the micro control
- separate Unibus option with traditional lights and switches console for maintenance security blanket, or remote operation
- logic hooks for all the high speed, expensive options desired for the upper end configuration using these same three hex modules
- successful LSI chips must occur for IR DECODE and UNIBUS control to reach the three hex module size, otherwise four modules
- data paths similiar to present PDP11/40 with 74S series logic used for speed
- cost for the three modules to approximate the cost for four present PDP11/40 modules, $635
- cost for a nine slot back panel to accommodate processor and 8K of memory similiar to PDP11/05, $152
- production line capable of shipping to either a stockroom or directly to a customer, no second system charge upon a basic machine

Low to High End - New PDP-11/40

(First Draft)

Configuration 2: System

- same characteristics as Configuration 1 except that the back-panel, box and power supply may differ to accomodate options
- cache memory option with that amount of memory that will fit upon a single board (probably 1K words) and use to advantage the faster data paths
- floating point processor option with additional control store and data paths to implement a PDP-11/45 floating point subset (some feeling that this should be buried in the basic control store and slowly use basic processor data paths)
- probable multiple processor option upon the Unibus control to allow multiple processors
- probable user micro programming option with a read/write control store and a general micro branch on low data path byte
- probable 32 bit instruction option if such an instruction format is adapted for the new PDP-11/45
- memory management option compatable to present KT11-D or variant version adopted by new PDP-11/45
- backpanel to accomodate the above options in addition to real time clock (integral?), maintenance modules and disk controller
- single board disk controller (RK05 subset?) to allow system integration at the processor back panel level
- box and power supply ordered toward a minimum (single,short?, cabinet) system, probably 10½ box
- basic production area ordered toward a shippable machine instead of a stock room machine subject to further system integration charges

digital INTEROFFICE MEMORANDUM

TO: Bruce Delagi
Bob Gray (Please redistribute)
Jega Arulpragasam
Charlie Spector (Market Inputs?)

DATE: 12/7/73

FROM: Jim O'Loughlin

DEPT: 11 Engineering

EXT: LOC: 1-2

SUBJ:STATEMENT OF THE PDP-11/40R (TODAY)

The following represents the goals, characteristics, and means of achieving the PDP-11/40R machines. No major differences exist from the November 9, 1973 memo, "The PDP-11/40R Machines", presented at the November Woods Meeting. New information and changes of emphasis are noted.

A three or four board base processor fits into two packages of differing capability:

- 5¼" box with 8K MOS Memory (optional cache, but otherwise limited expansion) for a low cost machine.
- 10½" box with 16K Sense Memory and expansion capability (cache memory, slow PDP-11/45 floating point instructions, memory management) for a high performance machine.

The new processor is ordered toward being small enough for 5¼" and fast enough to realize the advantage of the cache memory.

Three areas require further resolution.

- Should the physical address of the Unibus be expanded? How?
- Should the Maintenance Option (Unibus Parity) replace the Unibus ordered Multiprocessor Option?
- What is the present emphasis on the eternal conflict between small size, low cost and speed?

I. PERFORMANCE AND COST GOALS:

BASIC MACHINE	PERFORMANCE[1,4] ADD R,R	PERFORMANCE[1,4] MOV R+,R	COST[4]	
Present 10½" PDP11/35 (8K Core Memory. EIS optimal at $275)	990ns	2300ns	$2752	Direct Std. Product Build Cost
New 5¼" PDP11/40R (Integral EIS, 8K MOS, no Cache)	990ns[2]	2300ns[2]	$1618	Parts plus 15% FA&T
	(-0%)	(-0%)	(-41%)	
New 5¼" PDP11/40R (Integral EIS, 8K MOS Cache)	(815ns)x1.1[3]	(1310ns)x1.1[3]	$2668	
	(-9%)	(-37%)	(-.3%)	

SYSTEM MACHINE	PERFORMANCE[1.4] ADD R,R	PERFORMANCE[1.4] MOV R+,R	COST[4,5]	
Present PDP11/40 with 16K Core, Dual RK05's and ASR33 Terminal	990ns	2300ns	$8367	Direct Std. Product Build Cost
New 10½" PDP11/40R with 16K Sense, Cache, Dual RK05L, LA100 and Model B Terminal	(815ns)x1.1[3]	(1310ns)x1.1[3]	$5002	Parts plus 15% FA&T
	(-9%)	(-37%)	(-40%)	

NOTES

1. ADD R,R is approximately 1% of instructions, MOV is approximately 20% of instructions.

2. Assume poorer MOS Memory access time completely balance improved processor cycle times.

3. A hit ratio of 0.9 is assumed for 1K of cache memory, block size 1.

4. % are expressed relavent to existing machine.

5. Majority of system cost reductions come from new peripheral designs.

II. SYSTEM STRUCTURE

Processor - Three or four hex boards, internal UART, maybe integral line clock, EIS is standard lights and switch console is not available except as a Unibus option. Various options are available with the processor in certain boxes. Cache and Line Clock available in both boxes. Big box options include a PDP-11/45 FIS subset, KT11-D type Memory Management, K11L-A Stack Limit, and space for a Maintenance Console. Interest does not appear to exist for a Unibus multiprocessor option but does exist for a Maintenance Option (Unibus Parity, Last PC Storage, Error Status Word).

Instructions - PDP-11/40, except that FIS instructions are replaced with PDP-11/45 FIS subset. EIS instructions are standard in the basic machine, although slower.

Address- Same PDP-11/40 virtual address limiting with a KT11-D physical address expansion possible. Are expansions desired to memory management addresses? Mapping box on NPR's or memory?

Unibus - Same with cache memory option, perhaps easing bandwidth problem somewhat. Expansion of signals for Unibus parity & phy. address.

Peripherals - Many new peripherals now under development required: dual RK disks with single board controller; LA100 and Model B Terminal, new 10½" standard box, new PDP11/05R box and 8K MOS and 16K Sense Memories.

Expansion - Unlike the present KD11-A processor which is equally expandable in the PDP-11/35 or PDP-11/40, the 5¼" box will not have room for processor options (cache excepted). Will not pay for space or power.

III. MEMORIES

New 8K MOS memory required for low cost machine with the present 16K, or proposed 32K, Sense used in the system machine. Optional cache memory (1K or 1 hex board, whichever comes first) is used to speed both machines. A hit ratio of 0.9 is estimated by Research and Development Group for a block size of one. The cache memory must indicate, in 150ns, it has data, and provide the data in 225ns.

IV. BUS

Present Unibus with possible expansion for Unibus Parity and Physical Address expansion. No precise plan, except that present peripherals are compatable, memory must accomodate extra address, however. (See attached Physical Address memo.)

V. OPTIONS

Besides the processor options already noted, several other new products are needed, especially for the system machine. These include the dual cartridge disk, the LA100 and the Model B Terminal. Major system savings come from these units.

VI. TECHNOLOGY

The processor requires S Series and multilayer board upon one module (its data path) and the LSI'ing of Unibus control and IR decode. The custom LSI chip(s) for Unibus control is also desired by the PDP-11/05R project. A three board machine does not happen unless the LSI's are done. A single board disk controller may also depend upon a slave Unibus LSI.

VII. PACKAGING

The 5¼" box comes from the PDP-11/05R project and the 10½" box comes from the new standard box project. If a 21" box is desired. the present PDP-11/45 box should be upgraded (cost reduced). Do not believe that the project should create any new boxes! Modules will be present hex modules. Should the optional Unibus Console be mounted or a cabled pad-type console?

VIII. RELIABILITY AND SERVICE FEATURES

Mean time to repair must be improved on the system machine, while not affecting the cost of low end machines. Maintenance Option is discussed in an attached memo.

digital INTEROFFICE MEMORANDUM

TO: Bruce Delagi
Bob Gray (Please redistribute)
Paul Jansen

Steve Rothman
Dave Cutler

DATE: 11/30/73

FROM: Jim O'Loughlin

DEPT: Micro Products Development

EXT: 5455 LOC: 11-2

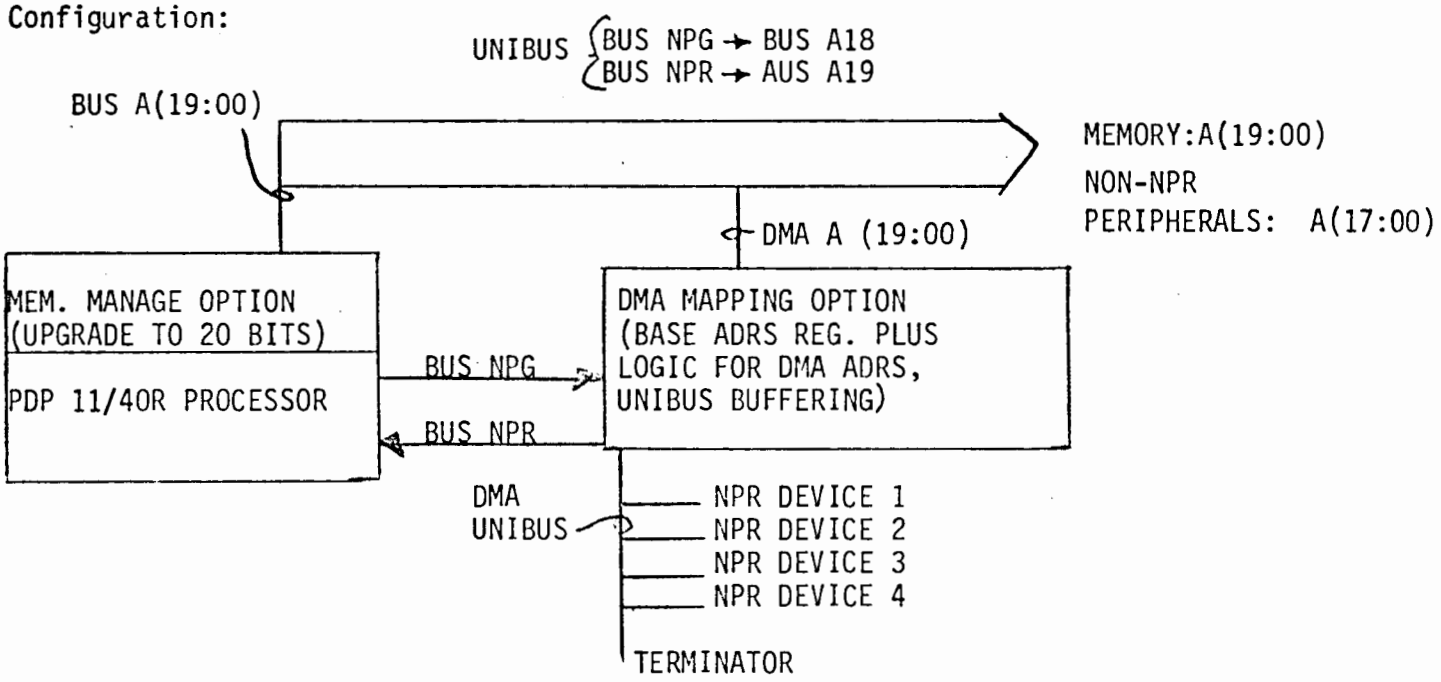
SUBJ: EXPANSION OF PDP 11/40R PHYSICAL ADDRESS

A simple expansion scheme allowing a physical address of a million bytes (20 address bits) on a PDP 11/40R was investigated. Inputs received from Paul Janson, Steve Rothman and Dave Cutler. The scheme must be simple as it only solves the physical address problem (not virtual),and is still liable to the 32 bit machine citicism of being complex. The present KT11-D module has its Page Address Register expanded by 4 bits, constraint and signal reallocation (2 bits) occur on the Unibus to prevent peripheral redesign, and a DMA Mapping Option must be created.

The DMA Mapping Option requires a processor loaded base address concatenated with part of the 18 bit peripheral DMA address; this provides an expanded address but slows DMA transfers (+100ns). This System Unit option would interface a limited mumber of DMA devices to the Unibus and would have to be adjacent to the processor back panel. Configuration, cost, and salient characteristics are noted on the attached block diagram.

Do we want to further corrupt Memory Management for the few applications requiring one million bytes of memory? Selling further complexity against 32 bit simplicity seems difficult. Can apply effort to speed up present RT11-D to some extent.

Configuration:



Characteristics:

1. Unibus unchanged in cable and all peripherals except PDP 11/40R Processor and DMA Mapping Option.

2. Only Processor and DMA addresses are expanded to 20 bits; Memories addresses are also expended. The peripheral addresses for status and control remain as 18 bit addresses and repeat four times in the address space. (Slight programming problems may occur.)

2. The NPR Unibus retains present Unibus characteristics (address of 18 bits and serial priority). The DMA Mapping Option offset only the DMA transfer addresses, most other Unibus signals are merely buffered to prevent a spur electrical loading upon the main Unibus.

Cost:

1. Development costs to upgrade Memory Management Option (2K) and create DMA Mapping Option ($60K).

2. Estimated Manufacturing Costs:

Upgrade of Memory Management : +$5 (from $150)
DMA Mapping Option:

System Unit Backplane	$80
Hex Adder and Control Module	$160
Unibus Terminators	20
	$265

digital INTEROFFICE MEMORANDUM

TO: Gordon Bell
Roger Cady
Bruce Delagi
Bob Gray (Please redistribute)
Ralph Platz

DATE: 12/5/73

FROM: Jim O'Loughlin

DEPT: 11 Engineering

EXT: LOC: 1-2

SUBJ: RELIABILITY FOR THE PDP-11/40R

Initial inputs on PDP-11 reliability indicate a greater concern for quick error isolation and repair rather than absolute error-free operation. This is the most important next thing the PDP-11/40R can do after providing PDP-11/45 performance at PDP-11/05 price. While not conceeding the low price iron market, we should realize that we do sell service, convience and reliability, (IBM type things) especially at the mid to high PDP-11/40 level.

The following preliminary suggestions are made:

1. The processor can provide in left-over (if any) microcontrol words a check upon the data path operation. This might be done automatically upon a LOAD ADRS or START console function. If a memory location is dedicated and known upon each system, a data transfer might also be tested. Cost is minimal if left-over microcontrol words exist, some cost is associated with display of the error condition. Believe that any reliability efforts that cause four modules instead of three modules are self defeating. Questions: Does the proposed elimination of a standard switch and light console compromise error isolation? Is the processor of little concern in the overall reliability picture that minimum effort should be expended?

2. Unibus Parity has been avoided for some time, but appears key to any isolation scheme involving transient or intermittant bus failures. This option will never happen until a processor committs to do it; the PDP-11/40R should do it, especially if it is the only new mid-range PDP-11.

3. Ralph Platz suggested several possibilities and triggered the idea of a single board reliability type option. We do single board options very well, and it avoids burdening the low end machine with unwanted cost. The board might include: Unibus parity (item 2) upon data, address and control; a program

readable Status Register for individual indication of "Trap to 4" errors; and on-going storage of last PC's to allow isolation of errors or recovery. Do not believe parity for the processor should be included unless the illusion of it is important. Would prefer micro-diagnostics for processor checking (Item 1).

4. More than an incidental committment is necessary to these reliability schemes. They involve PDP-11 definitions of response that go across all PDP-11 machines; they require future peripheral upgrade (Unibus Parity); and they require a diagnostic and system software committment. General issues must be settled as these schemes represent more than just a PDP-11/40R feature.

5. A number of reliability items concern the box and power supply. A problem exists here, in that the PDP-11/40R plans to use other machines' boxes and power supplies. Very critical is the 5¼" box which has to cost little for the PDP-11/05R derating the power supply and providing logic for isolation of DCLO errors may not be possible.

pl

INTEROFFICE MEMORANDUM

TO: Bob Gray
Lorrin Gale

DATE: November 9, 1973

FROM: Jim O'Loughlin

DEPT: Micro Products Development

EXT : 5455 11-2

SUBJ: THE PDP-11/40R MACHINES

My subjective formatted inputs are noted below:

Product Goals

Improve the performance/price ratio of the PDP-11/40 across its market range in four ways:

1. A three or four hex module PDP-11/40 with somewhat less cost and a major increase (30%) in speed with optional Cache Memory, slow EIS and UART standard, no lights and switches console;
2. A minimum configuration using above processor, 8K MOS Memory and the new low cost PDP-11/05R box and power supply in a limited expansion situation(9 slots for everything), low cost "pig iron";
3. A standard system configuration with versatile expansion capability including FIS (a PDP-11/45 subset), Cache Memory, integral (to back panel) disk control, and Memory Management;
4. An ability to build and ship off basic production lines with a single FA & T cost.

The machine is made high speed with cache memory to keep the product viable against the 32 bit machines. Multiprocessor hooks and User Microprogramming (in place of FIS) are also included. (These last options are ill defined).

Product Configuration

The new processor is based upon the present PDP-11/40 with 74S logic in a revised data path, more micro control words, and the LSI'ing of IR Decode and Unibus Control logic. Cache Memory is optional but is necessary to realize

the advantage of the high speed 74S logic Data Path. Minor improvement in ADD R,R time (815ns, 18% faster than present 990ns) is coupled with a more general improvement on multiple memory access instruction times, MOV R +,R for example (1310ns, 43% faster than present 2300ns). A hit ratio of approximately 90% for a 1K Cache of block size of one is applied against those improvements.

System Manufacturing Costs

Manufacturing costs for the basic processor modules and backplane is $787 compared to a present PDP-11/40 cost of $915. The use of the integral UART saves console costs ($120) and DL11 costs ($160). The minimum and standard systems are noted below:

Minimum System (9 slots)

Processor	$787
8K MOS Memory	400
5¼ " Box and power supply	220
Misc. and FA & T	211
	$1618

Standard System (5 system units)

Processor	$787
16 core memory	800
New 10½" box and power supply	385
LA100 and model 8 terminal (Cassette & display)	1400
RK05 load control	700
Cabinet	268
	$4350
FA & T (15%)	652
	$5002

Versatile Add-On's

Replace 16K with 32K Sense + parity	$400
Parity	100
* RK05L	500
Floating point (FIS)	260
* Cache	700
KT11	208
Second terminal	700
	$2868
FA & T (20%)	573
	$3442

* Most likely additions to minimum system

Typical System = Standard System + Versatile Add On's
= $ 8444

Development Time

Ship the processor in Q1 of Fiscal 1976 (approximately 18 to 21 months) with dependance upon several groups within the company to meet schedules. Disk (RK05L) estimated to be ready in Q2 of Fiscal 1976. Major concern is the time required for custom LSI chip for Unibus Control (appears PDP-11/05R may also want this chip). Manpower for the processor design and processor ordered options (Cache, FIS, KT, Multi Processor Hooks, User Microprogramming, Remote Console) is approximatly 10 engineers/techs. Money is as follows: $250K for Fiscal '74; $800K for Fiscal '75; $600K for Fiscal '76; with an additional $200K for LSI expenses and production line equipment. Total cost is $1850K which seems a bit high, could be lower on a second pass.

Project depends upon several other projects: the PDP-11/05R box; the new 10½" box; 8K MOS Memory; LA100 and Model B terminal; 32K Sense Memory and the RK05L disk.

Applications:

Present and future PDP-11/40, PDP-11/35 markets, high end of PDP-11/05 market, low end of PDP-11/45 market. (A yet-to-be defined multiple bus configuration of this processor might extend upward into the PDP-11/45 market).

Problem Overcome:

Present EIS becomes integral,and machine speed is increased; cost reduced. The FIS becomes a PDP-11/45 subset, User Microprogramming and Multiple Processor ability are provided in some form. Must eliminate double FA & T costs with standard systems shippable from the basic build area.

Weaknesses:

Can a high speed PDP-11 remain viable against the new 32 bit machines which easily accomodate expanded memory addressing and floating point operations? End systems above depends upon many projects and a custom LSI chip.

Jim

jmc

digital INTEROFFICE MEMORANDUM

TO: Gordon Bell
Roger Cady
Dick Clayton
Bruce Delagi
Jim O'Loughlin
Bill Strecker
Len Hughes

DATE: August 2, 1973

AUG 02 1973

FROM: Bob Stewart BS

DEPT: 11 Medium Scale Computers

EXT : 3564

SUBJ: CACHE MEMORY FOR THE PDP-11/40

While studying the results of some cache simulation runs done by Bill Strecker for the 11/XX study, I noticed that even a rather small cache gives results which might be adequate for many applications. For example, a 256 word, direct mapping, one word per block cache has a hit rate above 60% for typical PDP-11 programs. This size of cache only requires about 26 bipolar memory chips, and the entire mechanism could probably be squeezed onto one hex board. If a cache of this type were applied to an 11/40, on at least 60% of the processor's read references the data would be available at about the time MSYN would normally be set, thus saving the memory access time, bus driver and receiver delays, and cable delays. Programs would probably execute 30% faster.

Mechanization could be done as follows. When the processor asserts BBSY, the cache would watch the processor's physical address bus. When the processor attempted to do a read, if the address matched one in the cache MSYN would be prevented from setting, the data would be put on the appropriate processor bus, and the processor would continue. If the address did not match a cache address, the processor would do the bus cycle, and when the data arrived, it would be copied into the cache, replacing the previous contents. On write cycles, if the address matched a cache address the data would be copied into the cache as it was being written into main memory on the Unibus. If the address did not match a cache address, the cycle would be ignored by the cache.

If the processor was not asserting BBSY, the cache would monitor the Unibus. DATI's would be ignored, and DATO's which matched a cache address would be copied in the cache.

This organization should ensure that both the cache and main memory always have valid data, while requiring only minimal changes to the processor. If a higher hit ratio is desired, it might be possible to fit a 512 word cache, requiring 50 bipolar memory chips, on one hex board. This should give at least a 75% hit ratio. A 1024 word cache, using 25 1024 bit bipolar chips, should give an 85% hit ratio. These chips are relatively expensive.

bjw

digital INTEROFFICE MEMORANDUM

TO: Distribution List

DATE: November 16, 1973

FROM: Jim O'Loughlin

DEPT: Micro Products Development

EXT: 5455 LOC: 11-2

NOV 20 1973

SUBJ: Woods Meeting Impact on PDP-11/40R (What I Heard and What to Do)

1. The potentially stronger PDP-11/05R reduces the marketing need for the PDP-11/40R to be three boards and extremely low price. Hopefully such PDP-11/05R features as PDP-11/05 speed, the PDP-11/40 instruction set, optional EIS and parity does not compromise its low cost for low end PDP-11 business nor the low cost non-PDP-11 controller business (in house and customer?). Three boards and low cost are still desirable goals from a business, reliability, packaging and speed point of view; this goal is only slightly compromised by probable improved PDP-11/05R performance.

2. A stronger impact upon only three boards and low cost is the desire than the PDP-11/40R covers the low to mid market range of the PDP-11/45. (Some type of multiprocessor configuration or configurations would cover the mid to upper market range of the PDP-11/45.) Still must balance this replacement of the PDP-11/45 with the PDP-11/35 "pig iron" market.

3. Both EIS and FIS can be slow, but it is very important that the FIS be a complete PDP-11/45 subset and not a partial. This should happen even if super slow (first trade-off) or more than one hex board (second trade-off).

4. The price gap noted between the PDP-11/45XX and the PDP-11/40R is over emphasized. The minimum PDP-11/40R has neither cache or memory management which was standard on the PDP-11/45XX. More realistic performance/price ratios are noted below:

PDP-11/45XX	$10K x 0.4μs/instr = 4.0K $ μs/instr.
PDP-11/40R	$1.6K x 0.9μs/instr. = 1.4K $μs/instr.
PDP-11/40R & cache	$2.4K x 0.6μs/instr. = 1.4K $μs/instr.
PDP-11/40R, cache & memory management	$2.6K x 0.7μs/instr. = 1.8K$ μs/instr.

5. Given that the performance/price of the PDP-11/45XX really isn't so bad (even better for FPP), can't a simple cache memory scheme be effected on the PDP-11/45 in less than 18 months We need the speed of the PDP-11/45 now, we will still need it (enhanced if possible) while we develop the application ordered PDP-11/40X dual processor systems. Such a project would also extend our return on the relatively high investment in the PDP-11/45.

6. Multiple processors appear to be in, enven though we don't seem to know very much about them. The cencept is attractive if we support and understand the system. It can extend PDP-11 performance in a cost effective way, it may even regain our image of being an innovator. Dave Stone's inputs indicate that this support must extend into applications and include extensive software. Do we want this? And if we move only into certain areas we need a fairly fast general machine - the PDP-11/45 with cache.

7. Among the multiple-processor problems is what bus to use. Can the Unibus be used for dual processors with cache or must a 32 bit memory and disk bus be used? The first is a small multi-processor step within the PDP-11/40R project: the second really a new machine (especially if a 32 bit FPP is made). In any case the PDP-11/40R, hopefully, survives intact with only "inexpensive hooks" required.

8. Reliability is important with low Mean Time To Repair (MTTR) being more important than data integrity or operation with out failures. Since the PDP-11/40R may be theonly new mid to high range PDP-11, it must concern itself with the problem. Unfortunately the problem is not especially processor ordered, but is more system, Unibus and peripheral ordered.

9. No apparent objection exists to the user microprogramming option occuring in place of FIS. No great demand exists anyways. Perhaps the option should be done just to stop the complaints about not having it. Then we can see if anyone really wants it.

12/73

MEDIUM SCALE COMPUTER DEVELOPMENT

TABLE OF CONTENTS

GOALS FOR MEDIUM SCALE

COMPUTER DEVELOPMENT

PERFORMANCE

a. More computation/dollar in CPU
b. More space for programs and data
c. High swapping and file access rates
d. Expansion to more than one processor (close coupled)

RELIABILITY

a. Less vulnerable to failure
b. Better detection of a failure
c. Quicker repair time

SOFTWARE ENHANCEMENTS

a. Encourage users away from machine language code by offering a cost-effective high-level language alternative
b. Expand on DEC's expertise with real time and time sharing systems by offering a system in the price range of $70K to $200K.
c. Provide a cost-effective system for controlling networks of minicomputers.

ALTERNATIVES and CONCLUSIONS

1. The 11/F is a PDP-11 compatible CPU whose basic processor is defined today as a stripped 11/45 with the addition of a cache, a new multiprocessor capable bus, and MOS memory. An optional feature will provide for increased memory capacity plus about a 70% performance increase in Fortran programs over the base machine which has an internal performance equivalent to the /45 with a significantly higher bus bandwidth. This is the planned approach.

2. A derivative of the 10 family (KA10L) provides a lower engineering risk alternative whose base cost/performance is near that of the 11F, but would not get the Fortran performance of the 11/F. The marketing risk of not being 11 compatible is believed to be quite significant and this would only be partially overcome if a new real-time operating system (RSX-10) were to be developed. The engineering risk is increased if it is necessary to try to use the 11 I/O instructions in conjunction with the basic 10 architecture. Since this approach appears to be the next-best alternative, additional detail is provided in this package.

3. The use of multiprocessors of existing or modified existing 11/4X processors was considered but was not pursued due to the lower cost/performance factors and the significant programming support that need be developed. (While the 11/F will be able to exploit any multiprocessing support forthcoming, it is not completely dependent upon it).

4. To reduce the product cost of the minimum system, consideration was given to attaching an optional Fortran processor to the new memory bus along with a base 11/F processor. Since the Fortran processor would be required to handle 11 machine language instructions also, its cost would be similar to that of the base processing unit plus it would require all the multiprocessing programming support mentioned in alternative #3 above.

5. Due to the total cost and time of developing almost an entire new software library, very little effort was devoted to defining a new basic 32-bit word architecture to satisfy the immediate product goals. However, since there is a major addressing deficiency in the present 11 architecture, and since there seems to be developing a continuous marketing spectrum from the small mini to the high performance midi, it is proposed that an effort be established to define an architecture that can:

a) Provide direct addressability to all hierarchical levels of storage, as well as span the breadth of products required.

b) Incorporate a compatibility mechanism for today's architecture.

c) Be oriented toward exploiting LSI in both memory and logic areas.

It is essential that this multiyear effort be initiated soon if only on a several-man effort during the next year.

WRD:rml

W. R. Demmer
12/7/73

I. 11/F OVERVIEW

A. 11 Compatible Base Machine

1. The base machine is compatible with 11/40 EIS & KT-11D (does not have supervisor mode or I & D space as on the 11/45 with KT-11C).

2. Achieves 450 usec ADD R,R through the use of 11/45 technology and Cache memory.

B. Increased Memory Size

1. The physical address space is increased to 2 megawords by removing all memory from the Unibus and implementing the extra 4 bits in the KT-11D's Address Registers.

C. Increased Program Address Space

1. The virtual address space is increased for a set of op codes that will implement high level language constructs. Thus, FORTRAN programs will run in a larger virtual machine. Programs written in PDP-11 machine language will run in a 32K virtual machine.

D. Increased I/O Throughput

1. Higher I/O throughput is achieved by using a high speed 32 bit synchronous bus between cache & backing store memory. The bandwidth of this bus is 5 times greated than the Unibus. Unibusses and Massbusses are interfaced to this bus (see Diagram A).

E. Extendable to Multiprocessing

1. A new bus protocol allows more than one processor to be connected to the memory bus.

F. More Cost Effective FORTRAN Execution

1. The 11/45 floating point op. codes are used to implement a set of high level language constructs. This along with minor changes to the FORTRAN compiler allows faster execution and more compact object code.

G. Minimum System Cost

1. 7K for CPU with Cache, Unibus interface and 16K of memory.

2. 8K for CPU with Cache, FORTRAN extension, Unibus interface and 16K of memory.

11/F MEMORY AND I/O

INTRODUCTION

The 11/F system is being proposed with a new bus which interconnects all system components. The bus structure is not tied specifically to the 11/F processor, but is intended to provide a commensurate I/O and instruction stream capacity.

The proposed bus is aimed specifically at the following goals:

(a) Create a reliable, diagnosable communication medium.

(b) Increase memory-to-I/O and memory-to-processor bandwidth by a factor of 5 over the Unibus.

(c) Enlarge the physical address space to at least 2^{24} bytes.

(d) Remove the bus arbitration function from the processor and pave the way for clean multiprocessor coordination.

Principal features of the bus are:

1. Synchronous transmission, using clock signals from the "arbitrator" module.

2. 32 bit wide data path, with check code.

3. 150 ns cycle time.

4. Two memory access modes:

   (a) Single (32-bit) word, requires two separate transmissions, one for address, the second for data, and

   (b) Block mode, in which an initial address and length is transmitted to the memory system, after which the memory interface keeps track of where the following data words are to be stored (or fetched from).

5. I/O controllers and processors are treated identically by the arbitrator (allowing multiple processors and/or many I/O controllers, with controllers eventually containing "processor" capabilities).

The arbitrator and the four different bus interfaces are described below.

BUS ARBITRATOR

The arbitrator allocates bus transmission cycles, and generates the bus clocking signals. (The arbitration algorithm is not yet determined.)

Processors, Massbus controllers, and Unibus controllers are treated alike. Each of them may initiate a memory access request and they may transmit control or status information to each other.

Memory is recognized separately, and has highest priority for bus usage (to transmit a word in response to a fetch request).

The arbitrator also monitors bus error conditions, generates an interrupt to a processor when an error occurs, and displays error status information.

CACHE/BUS INTERFACE

The functions of this interface are:

1. Does memory fetch and store operations on demand of the processor (through the cache mechanism).

2. "Eavesdrops" on all memory store operations, in order to allow the cache to invalidate or update its contents.

3. Handles program-initiated transfers to I/O controllers (Unibus and Massbus), to other processors, and to memory control (such as error status).

4. Receives interrupt messages from I/O controllers and the arbitrator.

5. Responds to status/control transfers from other processors.

Accesstime to memory on a fetch, using typical core stacks, should be approximately 900 ns (6 bus cycles) composed of: 1 cycle for bus access, 1 to transmit address, 3 cycles wait for core stack access (about 400 ns.), 1 cycle to transmit data. (Bus access could take longer when there is a conflict with another processor or an I/O controller.)

Assuming a cache effective access time of 350 ns, and a conserative hit ratio of 85%. we obtain an average access time of 433 ns. (0.85 x 350 + 0.15 x 900).

UNIBUS INTERFACE

The I/O page (upper 4K words of Unibus address) is accessible to processors through the Unibus interface.

BR's originating on the Unibus are transformed into interrupt messages and sent to a processor.

NPR traffic originating on the Unibus is mapped into the memory system, using four mapping registers in the Unibus interface. Block transfers from and to Unibus devices are limited to a length of 32K 16-bit words.

No memory may be attached to the Unibus.

The Unibus interface contains the Unibus priority arbitrator.

Errors detected on Unibus transmissions (if detection is implemented) are signalled by interrupting a processor.

MASSBUS INTERFACE

Massbus device registers are visible to processors through the Massbus interface. (256 device registers is the maximum possible on a single Massbus.) Control of the interface itself is by writing into separate control registers. Status is read by a request - reply sequence.

Block transfers to and from memory are initiated and controlled by the Massbus interface. Maximum data transfer rate is limited by the Massbus.

Interrupts to a processor are generated by the Massbus interface in response to end-of-transfer and to attention conditions in devices.

MEMORY/BUS INTERFACE

Memory is presumed to be made of either a MOS matrix or 16K or 32K word core stacks.

The memory interface contains more logic than usual, in order to reduce total bus transmissions on high speed block transfers. The

number of concurrent block transfers supported by a memory will depend upon the implementation (2 is probably sufficient).

Block transfers from Unibus devices. being slower would be done with single (32-bit) word transmissions.

Single word access may perform fetch, store or read/modify/write cycles.

11/F FORTRAN ENHANCEMENTS

1. MOTIVATION

Better cost-performance on FORTRAN execution than the 11/45 is a widely stated marketing goal in the medium-scale computer (MSC) area.

Improving speed without enlarging address space is inconsistent in MSC (a 64 x 64 array of 32-bit numbers completely fills a PDP11 32K data space). Hence 11/F allows bigger data areas and bigger programs.

We want to reduce customer software costs by making higher-level-language programming more attractive. Both of the stated objections to such programming (slow execution of compiled code and large object programs) are attacked. User-programming costs deserve our attention more in MSC than in the small-computer market.

The development will be a joint hardware/software effort. Compiler technology and frequency-of-use data will determine which FORTRAN constructs are implemented in micro-code. We believe that we can succeed in this design interaction and that this is the direction in which the industry is moving.

Language-directed design has been done by Burroughs (beginning with the B5000). The 11/F architecture is also influenced by Iliffe's Basic Language Machine at ICL and Manchester University's MU5.

Why FORTRAN? It is the major higher-level language in our market; it is a well-defined language; and DEC expertise in its implementation is strong. Bob Gray's memo(12/3/73) provides some data on its importance in our markets.

2. ADDRESSING

A program's address space is enlarged to 8M words (24-bit addresses) from 32K words (16-bit addresses).

A descriptor technique was chosen because of its suitability for implementing high-level languages. In 11/F, all structured data, e.g., vectors and matrices, are addressed indirectly through descriptors. A descriptor contains, as well as a 24-bit address, information on data type and structure. For example, an array descriptor is

	matrix descriptor	data type (integer 16, integer 32, real 32, real 64, byte, etc.)	24-bit address of first element	row dimension	column dimension

The descriptor contents are used in subscript calculation, bounds checking, type checking, and type determination for arithmetic.

Other descriptors are used to access and describe vectors, subroutines, parameters, programs, equivalenced data, etc.

3. PERFORMANCE

The most frequently executed FORTRAN constructs,e.g.,

simple assignment
subscripting
DO-loop-control
IF-statements

are implemented in microcode.

New instructions, for example, "fetch-through-descriptor" and "end-do", are added to the 11 instruction set.

The frequency-of-use data has also derived other new instructions, e.g., "load-literal", a 16-bit instruction containing a 6-bit literal which will handle 98% of the literal needs currently using 32 bits.

The execution speed, excluding I/O, of FORTRAN programs on 11/F is compared with existing and planned products in the following estimates:

System #	Availability	SYSTEM			COST (CPU + memory) in 11/F Units	EXECUTION TIME in 11/F Units		COST X TIME	
		CPU	Memory	Compiler		Integer	Floating Point	Integer	Floating Point
1	now	11/45+FP11	core	MOP	.93	7.8	6.6	7.3	6.1
2	now	"	MOS	"	1.4	3.9	3.9	5.5	5.5
3	Q3'75	"	core	F45	.93	3.4	2.9	3.2	2.7
4	Q3'75	"	MOS	"	1.4	1.7	1.7	2.4	2.4
5	Q1'77	KA10L	core	F10	.85	3.9	1.2	3.3	1.0
6	Q1'77	"	core	F10*	.85	1.8	1.	1.5	.85
7	Q1'77	11/F	Cache & core	11/F	1.	1.	1.	1.	1.
8	Q1'77	11/F	"	11/F*	1.	.5	.83	.5	.83

*Optimized

We have predicted the performance improvement of 11/F by a weighted comparison of execution speeds for several FORTRAN constructs.

A small, fast descriptor store (managed with conventional cache algorithms) will be used to reduce the descriptor fetch overhead.

4. EVALUATION

Because the proposal is concerned with enhancing program execution per se, it is much easier to evaluate than one concerned with operating-system-performance enhancement. With the latter, system performance must be measured, rather than just program performance.

At the beginning of the development period we will build the necessary simulators and program instrumentation to answer such questions as:

1. How much instruction code space is saved by the new instructions.
2. How much extra code space is needed for descriptors.
3. How much time do FORTRAN programs spend in I/O.

The language-directed design method depends crucially upon the frequency-of-use data being sufficiently representative and detailed. The initial period will attack both aspects; in particular, we need a much finer resolution of data types, subscripting, and assignment statements than we have in our current data.

The major weakness at this stage is that very little time has been spent on the relocation/protection scheme. Hence, the implications for current operating-systems software, e.g., RSX/11D, are not understood at all well.

5. EXTENSIBILITY

The following extensions are possible:

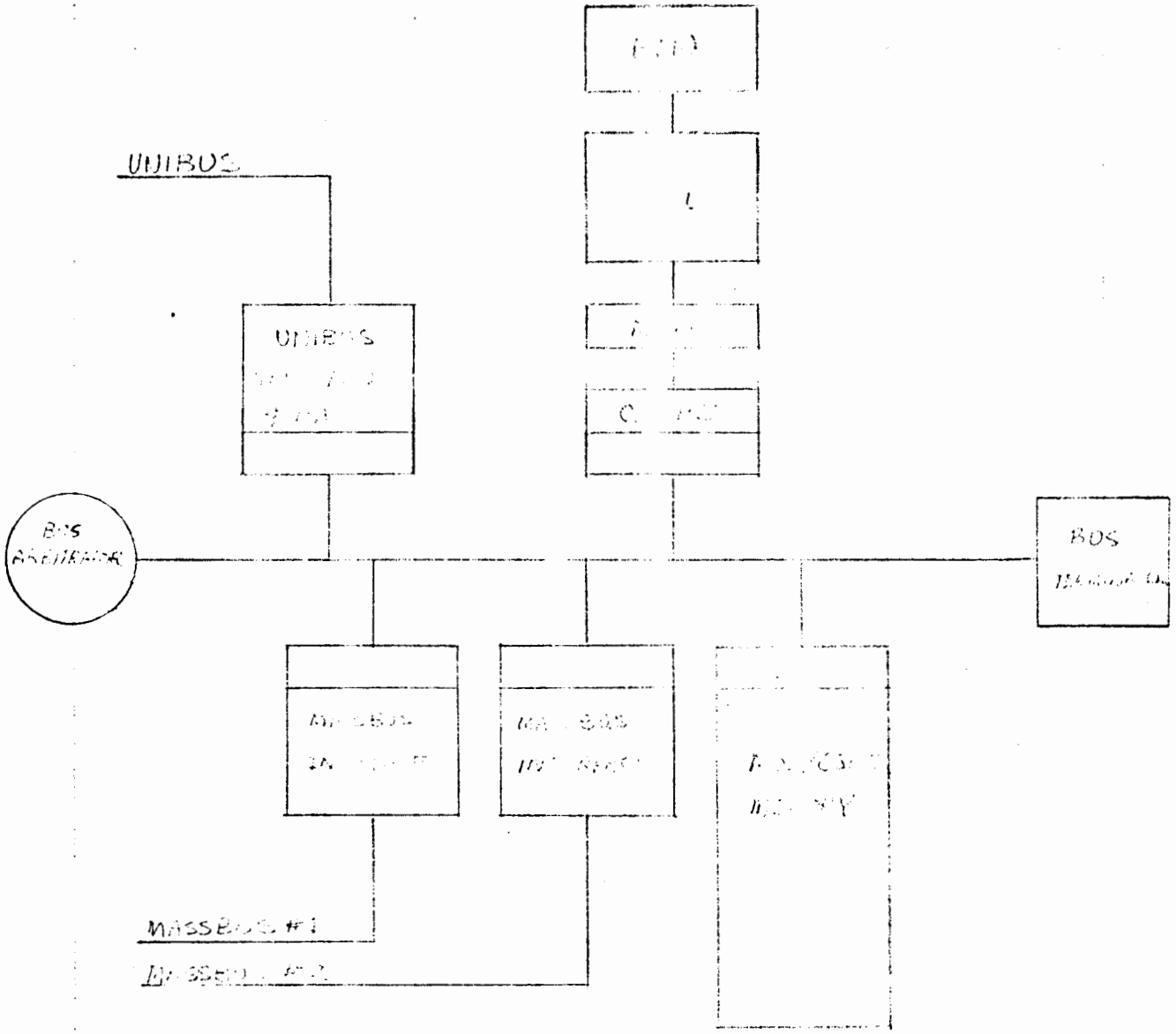
1. Support of new ANSI FORTRAN
2. Adaptable to COBOL, BASIC, even PL/I
3. Adaptable to a systems-implementation language
4. Some program debugging aids are more cost-effective on this machine, e.g., subscript-bounds checking and dumps which reflect the programmer's data structures and program at the source level.

11/F CONFIGURATIONS, ITEMIZED, NO PERIPHERALS

1. Minimum	1 CPU and Cache	2300
	1 Unibus	250
	1 Internal Bus	1200
	8K x 32 Bits MOS Memory	800
	Cabinet, Power Supply, Backpanel	1900
	Labor and Overhead	700
		$7150
2. "Standard"	1 CPU and Cache and Map and FTN	3850
	1 Unibus	250
	1 Internal Bus	1200
	64K x 32 Bits Core Memory	3600
	2 Massbus Controllers	1600
	Cabinet, Power Supply, Backpanel	1900
	Labor and Overhead	1000
		$13400
3. Large	1 CPU and Cache and Map and FTN	3850
	1 CPU and Cache and Map	2600
	4 Unibusses	1000
	1 Internal Bus, Extended	2400
	4 Massbus Controllers	3200
	128K x 32 Bits Core Memory	7200
	Cabinets, Power Supply, Backpanels	3800
	Labor and Overhead	2000
		$26050

NOTES: None of these systems has a console.

System #1 has no FORTRAN features.



("STANDARD" CONFIG.)

11/F Software Strategy

There are three major areas of implication for Software Engineering in the 11/F project.

1. Design level interaction during the engineering phase to optimize the hardware for Fortran execution.

2. Implementing Fortran support for 11/F by building a new code generation phase for the F45 compiler (the new in-line Fortran currently scheduled for 3/75 delivery).

3. Modifications to RSX-11D to support the new hardware.

There are, of course, unknowns with this approach in each of the above areas, and there are also corresponding risks. The major risk, as of today, is whether we fully understand item #3, that is, can we really make RSX-11D operate on this new hardware, with a "reasonable" amount of effort and end up with a product which we can really sell as being "compatible" with the current RSX-11D? Will it be perceived by customers as the next step up? The technical issues behind this risk is tied up with the implementation of extended virtual addressing and the interactions between the processor box and the Fortran-box (FBOX).

The risk with item #1 is caused by the need on one hand to get someone like Ron Brender involved very quickly and on the other hand not jeopardizing the Fortran/45 project.

There is relatively small risk with item #2; Fortran/45 is designed for flexibility in code generation, for an eventuality such as 11/F. The impact here is whether it affects the current F45 project.

For completeness, the following areas are the ones I see that impact RSX-11D.

a. implementation of extended virtual address capabilities.
b. interaction with the Fortran-box.
c. control of the UNIBUS peripherals via the new UNIBUS controller.
d. straight forward support for the integral mass bus controllers.
e. utilization of new instructions which are designed for enhancing RSX-11D performance.

Software Costs

At this stage I believe we can draw the bounds on the software costs. Until the architecture is completed, we cannot evaluate the full implications for RSX-11D. A basic assumption is that the project lasts for 24 months with Software Engineering involvement from the beginning.

Fortran

The best case assumes one person to work the evaluation/design issues for the first two quarters, followed by two men to write code generator and supporting routines.

The worst case means that OTS is completely rewritten and the code generator is more complex. This effectively adds 1½ man years.

	FY74	FY75	FY76		TOTAL
Best Case	$17K	68K	34K	=	119K
Worst Case	$25K	102K	51K	=	178K

RSX-11D

The best case assumes a level of effort like that applied for the Strecker/Wecker proposal (24 man-months). In addition there is support for the mass bus and UNIBUS, adding another man-year.

The worst case means that the basic addressing and memory management scheme causes us to rewrite RSX-11D (RSX-11D is strongly tied to the 11/40 memory management architecture). Given that RSX-11M is a rewrite and is being implemented with about 5 man years of programming for the first release and probably another 5 man years after the first release, a significant change for the 11/F could cost us a rewrite. A rewrite the third time should cost less, but there is added complexity.

	FY74	FY75	FY76		TOTAL
Best Case	$17K	102K	34K	=	153K
Worst Case	34K	170K	34K	=	238K

Summary Costs

	FY74	FY75	FY76	TOTAL
Best Case	$34K	170K	68K	272K
Worst Case	$59K	272K	85K	416K

digital INTEROFFICE MEMORANDUM

TO: Lorrin Gale
Bob Gray

CC: Bruce Delagi
Rony Elia-Shaoul
Len Hughes

DATE: November 13, 1973

FROM: Jim O'Loughlin

DEPT: Micro Products Development

EXT: 5455 LOC: 11-2

SUBJ: PDP-11/40X MACHINE

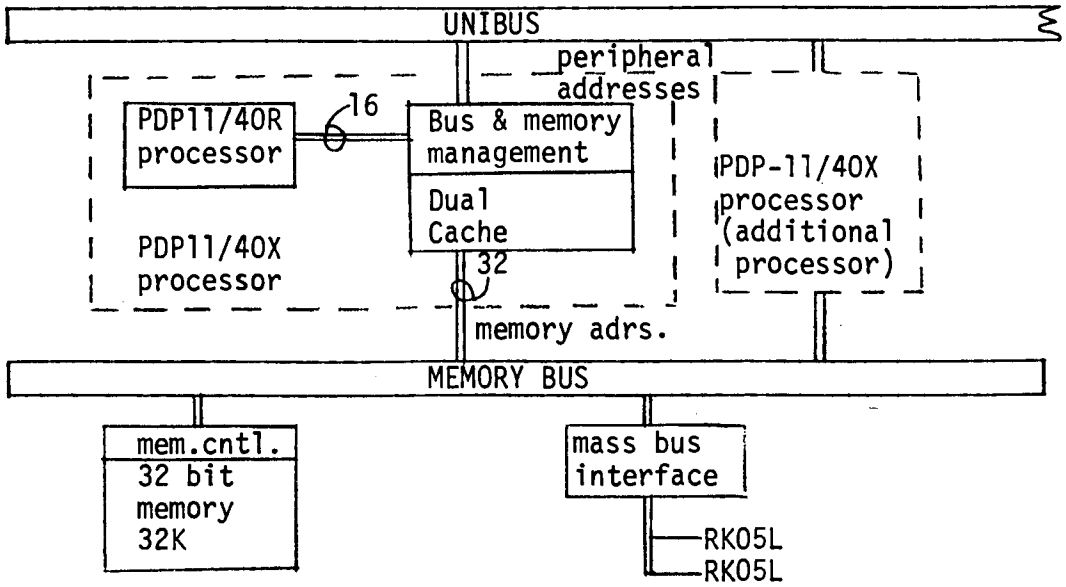
In the interest of completeness, this machine is offered as an alternative to developing a new 32 bit PDP-11/45 type machine. Many major questions need to be answered concerning hardware and software.

Product Goals

Extend the performance of the PDP-11/40R into the mid and high PDP-11/45 range with a wider (32 bit) memory bus having multiple processors. A single base processor (PDP-11/40R) is developed as the next machine with bus and multiple processor system techniques eliminating the need for a follow-on PDP-11/45 (and attendant hard decisions on 32 bit instruction and memory management). Future PDP-11 large machines would be ordered toward multiprocessor configurations; this is a major committment requiring hardware system and software support.

Product configuration

The base PDP-11/40R processor is expanded by its multiprocessor option, dual Cache Memory, as well as a Dual Bus Interface Unit. A PDP-11/45 backplane would accomodate the processor modules, the processor option modules of the standard PDP-11/40R System, and the 32 bit memory bus, memory and Mass Bus Interface. Probable block diagram is noted below.



The PDP-11/40R machine remains a 16 bit processor, the memory bus increases machine bus bandwidth by 2 for the 32 bitness and perhaps by 2 or 3 for synchronous block transfers. Instruction execution times remain the same as for the PDP-11/40R with the dual cache memory increasing the hit ratio from 90% to 95%.

System Manufacturing Costs

Rough estimates of cost would include a PDP-11/45 backplane and cabinet (21") with some quantity of 32 bit memory. Incremental cost associated with additional processor. Probable component costs are noted below.

Processor #1 9 slots	PDP-11/40R modules	$635
	Bus, memory management modules (2 hex)	300
	Dual cache (1K x 16 bits) x2	1400
	Floating point (FIS)	260
	Multiprocessor	170
	Console terminal (ASR33)	936
		3701
	PDP-11/45 backplane (only 28 slots)	580
	PDP-11/45 cabinet and power supplies	1764

(continued on next page)

6 slots	Memory (32K sense x 16) x 2	$2400
1 slot	Memory-bus control board	170
3 slots	Mass bus interface (3 hex)	500
1 slot	Disks-Dual RK05L and Cntrl	1200
		10,315
	FA & T (25% because of multiprocessors)	2,579
	TOTAL	12,894
Processor #2 8 slots	Second processor and console terminal	3,701
	FA & T (25% because of multiprocessors	925
	TOTAL	17,520

Note that above estimates of slot usage completely fills the PDP-11/45 type backpanel. Expansion of the 32 bit bus must be in backpanel, more memory means a larger backpanel.

Development Time

The ramifications of multiprocessor systems leads to the following estimates. The system could be ready 9 to 12 months after the PDP-11/40R if a parallel effort (starting now) is made upon the multiprocessor and 32 bit bus issue. These issues impact upon multiple processor controls proposed for the PDP-11/40R and PDP-11/05R. Three new hex modules, a new bus and backpanel would require 4 engineer/technicians plus two system architects. No software estimates are given in time because no committment to multiple processor operation exists. Given that software is necessary, the cost of this machine would approximate the cost of a new machine development ($1500K) even though it is "only" a combination of existing (PDP-11/40R) machines.

Applications

Present mid and high end of PDP-11/45 sales if the speed advantages of multiprocessors are met. The PDP-10 dual processor suggests that the limit on computer power increase may be 1.5. (and that is with rewritten software by a group with extensive multi user experience).

Problem Overcome

The following problems are addressed (do not know if they are overcome):

1. Bus bandwidth is increased except that the Mass Bus 18 bit path may be somewhat of a bottleneck.

2. Doing a new PDP-11/45 with brute force speed is avoided. Some minor costs savings results. Manpower might remain free for a new architecture machine.

Weaknesses

A number of weaknesses have been noted throughout and are summarized below:

1. Multiple processor goals are unknown, support for system responsibility does not presently exist.

2. Present PDP-11/45 machine may exceed capability of a multi-processor configuration if the PDP-10 experience is any guide.

3. Cost for the project is fairly high and does consume manpower.

4. Absolutely no committment exists for multiprocessor software.

5. Multiprocessoring will exist at a lower level on the unibus between PDP-11/40R and PDP-11/05R, how many want or need it on a 32 bit bus?

Jim

jc

digital INTEROFFICE MEMORANDUM

TO: Bruce Delagi
David Stone
Bob Gray

DATE: November 9, 1973

FROM: Larry Wade

DEPT: Software Engineering

EXT: 3689 LOC: 12-2

SUBJ: PDP-11/6X Proposal

1. Goals -

   a. Provide features of 11/XX, namely
      - low cost, high speed memory
      - more physical address
      - solve fast peripherals problem

   b. Increase virtual address beyond 32K

   c. Provide 32 bit integer arithmetic

   d. New instructions for increased operating system and language performance.

2. Configuration -

   Add R,R (16 bits) is 550 nsec.
   Add R,R (32 bits) is 700 nsec.
   I/O bandwidth is 24 mb
   Memory bandwidth is 64 mb
   Virtual space is 2^{22} bytes (streker proposal)
   Physical space is 2^{22} bytes
   New instructions to support new memory management
   32 bit integer arithmetic added via enhancements to FPP
   Selected instructions added to improve RSX-11D performance (i.e., context switch) and Fortran performance (i.e., subscripting instruction)

3. System Manufacturing Cost

   $35K for typical system in 1976

4. Development

   Time to ship 2 years
   Cost to build 3.25M - Engineering
   .15M - Programming mandantory, to first release
   .5-1.0M - Follow-on programming

   Cost to first ship
   3.25M - Engineering
   .15M - System programming
   $3.4M

Follow-on programming $.15M-$5.0M, depending on what new software (operating system, compiler is built).

Assumptions:

Cost to build 11/45 was $2.5M @ 2 years. 11/6X has new challenges, but has a stronger base to build on, so project could be completed in same time as 11/45. Costs are assumed 30% higher due to inflation and increased amount of work done to build a new product (checkout, diagnostics, etc.).

Programming for first ship is minimal and defined as "Make RSX-11D work" (2 man years) and do some system evaluation (2 man years).

Follow-on programming starts with making Fortran/45 support it (4 man years) and can include writing a new operating system and a COBOL compiler.

5. Applications

All current 11/45 markets
High end 11/45 OEM system markets
Computation market
New markets running large, dedicated applications needing lots of computing power.

6. Problems solved

- Allows 11/45 to run at speed
- Extends physical address space
- Supports high speed I/O devices
- Extends virtual address space
- Provides 32 bit integer arithmetic
- Provides an answer to 32 bit competition

7. Weaknesses

- Large development costs
- Doubtful whether software can utilize new features at time of first shipments.
- Means a redesign of the 11/45
- Strains the family concepts even more
- Pushes our systems into a size where it is costly to support
- No easy upgrade for existing 11/45 customers
- It does not provide relief for op code space problems
- Sales department survey indicates we do not need it

8. Cost Data

Minimum 11/6X costs (RSX-11M)
same as 11/ME, except
CP + cache + KT = 7.7K

Typical 11/6X cost (RSX-11D)

CP + cache + FP + KT =	8.7K
rest same as 11/ME =	21.7K
	30.4K
15% integration	4.6K

12/73

KA1ØL OVERVIEW

A. Cost Reduced PDP1Ø CPU

By using 11/4Ø technology, the PDP1Ø CPU can be manufactured at about 6.5K

B. Large Memory Size

With KL1Ø compatible paging, a physical address size of 512K 36 bit words will be available

C. Large Program Address Space

A virtual address space of 256K words is available using standard PDP1Ø instructions

D. I/O Features

1) The I/O system will support transfer rates of 2 μsec and 3 μsec per 36 bit words without seriously degrading the CPU performance

2) Supports Unibus and Massbus peripherals only

E. Executes PDP1Ø Programs

1) The KA1Ø instruction set will be implemented with hardware support of double precision floating point

2) The PDP1Ø I/O instructions will be changed so that the Unibus is supported without including a PDP11 CPU. This will permit most 1Ø programs to run

3) Require a new RSX1Ø operating system for real time support

F. No Multiprocessors

The KA1ØL design as proposed precludes multiprocessing. To incorporate it would require approximately $2K additional hardware for an adequate bussing arrangement plus a cache needed to maintain processor performance.

digital INTEROFFICE MEMORANDUM

TO: Bruce Delagi
Len Hughes
John Levy
Craig Mudge
Charlie Spector

DATE: 12/5/73
FROM: Bob Stewart/Steve Rothman
DEPT: 11 Engineering
EXT: 3564/ LOC: 1-2
2815

SUBJ: SMALL TEN PROPOSAL, FIRST PASS

CONFIDENTIAL

INTRODUCTION

This is a proposal for a moderate cost, moderate performance computer system which uses PDP-10 software and PDP-11 peripherals. It has two somewhat incompatible goals.

One goal is to take advantage of available PDP-10 timesharing software and low cost PDP-11 peripherals to provide a timesharing system in the $50K to $250K price range. This would eliminate the need to write a new timesharing system for the PDP-11 by making use of the extensive software investment sunk into the PDP-10.

The other goal is to counter competition from 32-bit minicomputers in the 11/45 market. This proposal does not address this goal very well. The competitive aspects of this market seem to require an extremely low cost, stripped down processor with no paging, floating point, or console. Also, the PDP-10 has no good software for the real time market, which currently represents about three fourths of 11/45 sales.

We had intended to do a careful cost study of this project but we quickly found ourselves up to our effluent duct in alligators. The cost estimates should be considered as plus or minus 30%.

No further mention is made of the interesting management issues involved in determining which piece of the company will design, build, maintain, and sell the hardware and software mentioned in this proposal.

PROCESSOR

The instruction set will be similar to the KL10. The KL10 extensions to the KA10 instruction set, such as double precision floating point and long integer, will run very slowly. If these extensions turn out to be more than a mere matter of microcode, some of them will be left out. The I/O instructions will be completely different from the normal PDP-10 set, since they will be controlling a Unibus and its hangers-on, rather than PDP-10 peripherals. No other extensions to the instruction set will be considered.

The processor is intended to run at about the same speed as the KA-10 on commonly used instructions. The internal data path will be 36 bits wide.

No provision is made for multiprocessor systems of any type. No PDP-11 is needed to run the Unibus or act as a console.

Paging will be included in a manner similar to the KL-10, but with only one virtual address space instead of 32. The user virtual address space is 256K x 36 bits. Content switching will not require software loading of large numbers of page registers.

We intend to make every effort to use an LA or VT type device as the console and not provide a switches and lights panel.

I/O transfers will be done on built-in Massbus controllers discussed separately or on the Unibus. The Unibus will be controlled by the processor, and will be useable by either interrupt or NPR devices. The data width will be 16 bits, compatible with current PDP-11 peripherals. Note that the Unibus cannot be used to load a binary program image, since it can only access 32 of the 36 bits in a word. Standard Unibus memory parity will be provided just in case any devices which detect the parity code are ever built.

As alternatives, an 18 bit data transfer could be performed, with no parity, or an 18 bit transfer could be performed with memory parity if BR7 and BG7 were used for the extra bits.

Since the Unibus address space is too small to access all memory a mapping box will be provided which will split the Unibus address space into 2K byte pages to match the processor page size. Each of these 128 pages will be mappable to any page in memory, thus providing scatter-read gather-write capability.

The processor physical size is expected to be about 16 hex boards. The cost is expected to be about $6.5K including cabinet and DEC-writer, but no memory or memory control.

No provision for cache is included. The processor data paths and control will be designed to run with normal memory and will not necessarily go any faster if memory access time becomes very small.

No provision for using normal PDP-10 memory or peripherals is provided.

The processor-memory path will be protected by address and data parity. The internal processor paths will not contain pairty, redundancy, or self-checking Maintainability features including test points and extra microcode will be provided where appropriate without excessive cost.

MASSBUS CONTROLLER

Controllers will be provided to interface Massbus devices to the system. Data transfers will occur direct to memory, with address and data parity, while control transfers will be on the Unibus.

At least one controller capable of transferring over one halfword per microsecond will be provided. Other controllers will be capable of over one halfword per three microseconds. The fast controller is intended to handle any swapping device, while the others handle disk packs or tape driver. It is assumed that the RK06 will be interfaced to the Massbus.

If physical space permits the slow controller will be able to select control of two or more Massbuses, although only one will be able to transfer at once. As an alternative, several logically separate slow Massbus controllers could be provided, with higher concurrency, but also higher manufacturing cost and greater physical size, possibly leaving no room for memory in the basic box.

The controllers will not go through the Unibus mapping box. Instead, they will pull in a physical address-word count word from memory to provide scatter-read gather-write. The full implications are not understood yet and this is subject to change.

The controllers will not be program compatible with either the RH-11 (different address space) or the RH-10 (different I/O structure).

The controllers are expected to cost about $1K for the fast version

SMALL TEN MEMORY SYSTEM

The memory system is based on the 32K sense core memory presently being developed. We are assuming the basic 32K by 19 bit (halfword plus parity) memory runs at 1 microsecond cycle time and costs $1000. The minimum system memory size would be 16K 36 bit words, which would take two memory cycles per word. One memory could be added to make a 32K by 36 bit memory, where each 32K chunk contained half a PDP-10 word. This 32K by 36 memory would fit in the CPU box. Memory could be expanded outside the basic box in 32K by 36 bit increments to a maximum of 512K PDP-10 words. (one million PDP-11 words).

The 32K sense memories would be attached to between one and four buses each of which would have 20 data/addresslines plus several control lines. Addresses would be transmitted to the memories, and then two 18 bit halfwords of data would be transmitted in the appropriate direction. All address and data transfer busses would include parity. These buses would attach to a three port memory control which is packaged internally with the CPU. This memory control interfaces to the CPU, Massbus controller, and Unibus Mapping box.

The total data rate through the memory control could get to approximately 500 ns per 36 bit word (2 megacycles) in the larger systems. This would be partitioned as one word per microsecond to the CPU (1 megacycle), one word per two microseconds to the Massbus Controller (1/2 megacycle) and one word per two microseconds to the Unibus Mapping Box. Note that many times the Unibus Mapping Box will only be able to use 1/2 of each PDP-10 word fetched, so that the effective rate for the Unibus port is probably one Unibus word per 1.5 microseconds.

The cost of the memory control should be about $550, plus $175 for each of the four bus interfaces. The table below summarizes the memory system cost of typical systems:

	16K Minimum	32K	64K	512K Maximum
Cost	$1725	$2775	$4900	$33250
Number of 32K x 19 Memories	1	2	4	32
Available data Rate, 36 bit word	2 us/word .5 megacycles	1 us/word 1 megacycle	.5 us/word 2 megacycles	.5 us/word 2 megacycles

dgdlab INTEROFFICE MEMORANDUM

TO: Bruce Delagi

DATE: 11/1/73

FROM: Len Hughes/Rony Elia-Shaoul

DEPT:

EXT: LOC:

SUBJ: KL^{2}10 PROPOSAL

1) PRODUCT GOALS:

- Design a PDP-10 that can be manufactured at the cost of the 11/45.
- Compete against 32 bit machines from XDS, MODCOMP, INTERDATA, DG(?).
- Run existing PDP-10 software with minimal changes.
- Package for an office environment.

2) PRODUCT CONFIGURATION:

- PDP-10 CPU
- Add AC to AC in 1.0 usec.
- Design center would be a 16 user general timesharing system running TOPS 10 or VIROS.
- May require a real time system for network environment.

3) SYSTEM MANUFACTURING COST:

RSX10 - $49.7K
BTS10 - $66.9K

4) DEVELOPMENT:

- 2 years to 1st ship
- 25 people
- ~~$2.5~~ million development cost

5) APPLICATIONS:

- Computation and Commercial
- Central CPU in Network for LDP and IPG
- OEM iron market(?)

6) PROBLEMS SOLVED:

- Uses an existing timesharing monitor.
- No virtual addressing problems.

APPLICATIONS BY PRODUCT

1) COMPUTER CENTER MACHINE:
   - Lots of small jobs.
   - Fast compile time.
   - Interactive Basic and batch FORTRAN and COBOL.
   - Interactive FORTRAN would be a bonus.

2) ENGINEERING DEPARTMENT MACHINE:
   - Run canned programs.
   - Execution speed important.
   - Needs large virtual address space.
   - FORTRAN and BASIC.
   - Canned programs should be sharable.
   - COBOL would be a bonus.

3) COMMERCIAL MACHINE:
   - Used for order entry, inventory, payroll, etc.
   - Requires COBOL to generate canned programs.
   - Canned programs should be sharable.
   - Large data base.
   - Reliable hardware and software.

4) NETWORK:
   - Response time important.
   - Number crunching and scheduling.
   - Large data base.
   - Large virtual address space.
   - Interactive BASIC and fast executing FORTRAN.
   - Would be desirable to have interactive FORTRAN to aid in program development.
   - COBOL would be a bonus in industrial environment.

FEATURES REQUIRED:

- FORTRAN, COBOL and BASIC that run under timesharing monitor that are optimized for compile time and have good diagnostic aids. This allows for fast program development and would be ideal for "COMPUTER CENTER MACHINE". Compilers should be sharable.

- FORTRAN and COBOL compilers that run under batch monitor that optimize execution speed. This generates the object code for the canned programs. The object code generated should be sharable.

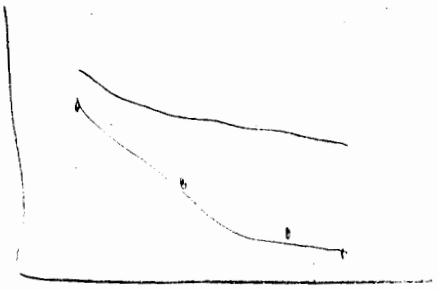
- Canned programs that run under timesharing monitor.

- No bus bandwidth problems.
- Has existing FORTRAN and COBOL compilers that are sharable and generate sharable object code.

7) WEAKNESSES:

- Does not allow easy upgrade from 11/45 customer base.
- High entry cost compared to Interdata. $10K
- May require RSX10 development.

- cost to put software in?



SYSTEM COST BY COMPONENTS

RSX10

CPU and 2 MASSBUS CNTLS	9.5
64K MEMORY	6.8
LA30	.7
DH11 and 4 TERMINALS	5.3
2 RK06 MOVING HEAD DISKS	2.7
TM02 and 2 TU16 DRIVES	6.9
300 LPM PRINTER	8.5
1000 CPM READER	3.0
CAB	1.0
	44.4
12% INTEGRATION	5.3
	49.7

BTS10

CPU and 3 MASSBUS CNTLS	10.0
96K MEMORY	10.2
LA30	.7
DH11 and 16 TERMINALS	13.7
RS04	3.0
2 RK06 MOVING HEAD DISKS	2.7
TM02 and 2 TU16 DRIVES	6.9
300 LPM PRINTER	8.5
1000 CPM READER	3.0
CAB	1.0
	59.7
	7.2
	66.9

ASSUMPTIONS:

- CPU 15 brds, 11/45 cab and PS, 1105-R and 16K memory @8.5K.
- Core memory 3.4K for 32K X 36 bits.
- DH11 @2.5K and terminals @0.7K.
- Massbus controller @0.5K.

INTEROFFICE MEMORANDUM

TO: Bruce Delagi
Len Hughes

DATE: 10/30/73

FROM: Bob Stewart BS

DEPT: 11 Engineering

EXT: 3564 LOC: 1-2

SUBJ: 11/XX PRODUCT SUMMARY

1. Goals - provide low cost high speed memory for the 11/45
   - solve fast peripherals problem for the 11/45

2. Configuration - processor is basically an 11/45
   ADD R,R time is 440 nsec with KT-11C on
   compared to 400 nsec with bipolar memory
   main memory is 16K sense core
   sold in 32K word chucks
   maximum is 256K words
   cycle time is one microsecond
   design center is medium RSX-11D configuration
   software will be RSX-11D, RSTS/E, BTS

3. System Manufacturing Cost - $52K for typical RSX-11D configuration

4. Development - 1.5 years to first ship on July 30, 1975
   10 people from 11 engineering
   $3/4 million budget to ship

5. Applications - anyplace needing a high performance, low cost PDP-11, particularly OEM and Computation

6. Problems Solved - lets 11/45 run at speed with reasonable cost
   expands physical address space
   allows high speed Massbus devices

7. Weaknesses - does not provide add-ons for current 11/45
   marketing problem selling 32K chunks of memory
   does not solve virtual addressing problem

CONFIGURATION INFO

Minimum System

CPU, Memory Management (not optional), 32K words of 16K sense core memory, 1K word bipolar cache, cabinet

TYPICAL RSX-11D SYSTEM

CPU	In	
FPP	CPU	$14K
KT	BOX	
CACHE		
DUAL MASSBUS CONTROL		
64K CORE $3K		
LA30 CONSOLE DEVICE		
FOUR VTXY TERMINALS		4.4K
DH-11		4.0K
TWO RK06's		2.7K
TM02		1.3K
TWO TU16's		5.6K
LP-01J 132 col. 300 LPM		8.5K
CD-11		3.0K
BOXES, CABS....		1.0K
		44.5K
+15% INTEGRATION		6.7K
		$51.2K

For RSTS/E, add four VTXY's for $56.2K.
For BTS also add another 64K of memory at $3K and another cab at $1K for $59.1K.

DEVELOPMENT INFO

Project includes:

Cache memory 1024 words, bipolar, three port (Fastbus, Massbus, Unibus), parity.

Main memory, 256K words, 16K sense core, parity.
Mostly a packaging and bussing design.
Dual Massbus controller, interfaced closely with cache.
Changes to KT-11C to increase physical address space.
Changes to processor boards if needed.
New, lower cost backplane.

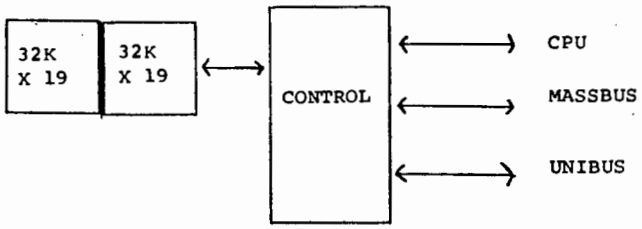
FISCAL YEAR	1974		1975				1976
	Q3	Q4	Q1	Q2	Q3	Q4	Q1
Manpower (CC367)	5	8	10	10	10	10	10
Budget K$	41	80	113	159	130	128	103

GOALS AND UNGOALS

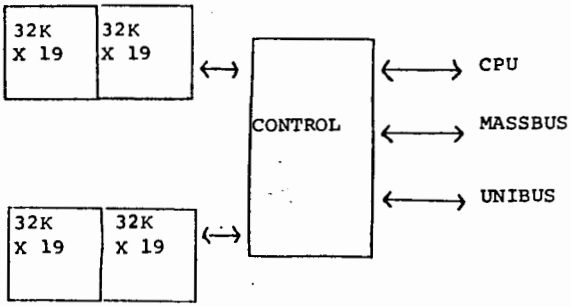
The basic intent is to create a fast, inexpensive, single-processor high-end system.
Typical programs using the basic 11/45 instruction set should run about 10% slower than an 11/45 with bipolar memory, with memory management on in both cases.
The manufacturing cost should be about $2K more than a system using core memory only.
The system should run Massbus devices with a one microsecond per word transfer rate.
The system should handle 256K words of memory.
Speed with memory management off is not of primary importance.
Multiprocessor systems is not a primary goal.
Virtual Address Space is not expanded.
No new instructions are provided.
The design center system will not be compromised to provide a low-ball.

	11/XX	11/40R
Basic processor boards, backplane	$3600	$787
KT-11	$ 750 not optional	$208
FP-11	$1400	$260
CACHE	$1100 not optional	$700
MASSBUS CONTROL	$1200 two Massbuses	$850 RH-11
5¼" box with power supply	____	$220
new 10½" box with power supply	____	$385 ($940 today 10½" box)
cabinet	____	$268
21" box with power supply and cabinet	$1300	____
8KW memory	____	$400 mos
16KW memory	____	$800 16k sense
32KW memory	$1500 16k sense	
console	$ 220 not optional	____
parity	included	$100

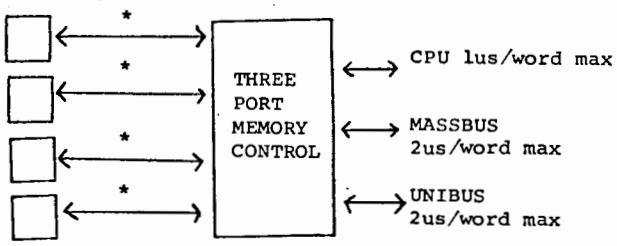
32K CONFIGURATION:



64K CONFIGURATION:



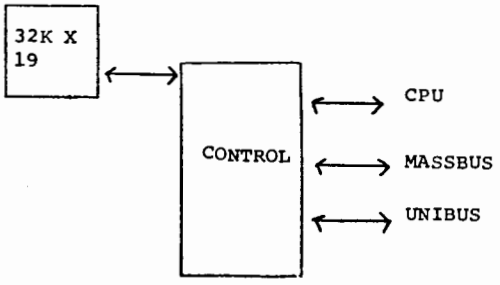
MEMORY SYSTEMS CONFIGURATION:



32K by 19 bit
memories, max 8 per bus

* 25 to 30 were buses; one required

16K CONFIGURATION:



Larry Wade is investigating the software aspect of this proposal, and a section of software will be included in future revisions, if any.

KA-10L CONFIGURATIONS, ITEMIZED, NO PERIPHERALS

1.	Minimum	1 CPU, floating point, Unibus	2250
		1 Memory Control	500
		16Kx38 core memory	1000
		Cabinet, power supply, backpanel	1900
		Labor and Overhead	700
			$ 6350
2.	"Standard"	1 CPU, floating point, Unibus, paging	2550
		1 Memory Control	500
		64kx38 core memory	3800
		1 Quad Massbus Control	1800
		Cabinet, power supply, backpanel	1900
		Labor and Overhead	1000
			$11550
3.	Large	1 CPU, floating point, Unibus, paging	2550
		1 Memory Control	500
		1 Quad Massbus Control	1800
		1 Swapping Massbus Control	800
		128kx38 core memory	7600
		Cabinet, power supply, backpanel	3800
		Labor and Overhead	2000
			$19050

NOTES: None of these systems include consoles

KA10L Software Strategy

There are two alternatives with respect to basic operating system software. One is to orient the product towards the computation market and offer timesharing. Such a strategy would use the VIROS operating system or a core squeezed version of it. The other alternative is to market it in the industrial markets as an RSX-11D compatible product at the higher levels such as command and Fortran interfaces.

VIROS Alternative

VIROS is a state-of-the-art operating system featuring demand paging. The system size is very hard to quantify since it is paged. Expectations are that it would be on the order of 20K for a "typical" KL10 system. VIROS is designed on the assumption that a drum is available on system.

The easiest thing to do would be to use VIROS "as-is" for the operating system. The minimum configuration would include 64K and a drum (RSØ4 or RSØ3). The software engineering costs for this would be small and be related to performance evaluation, consulting and releasing (these services would likely be required for any major product so are not included here).

Because of the likely "small system" nature of the product it would be desireable to tune VIROS to make the tradeoffs in favor of space and against time. The belief is that the structure of VIROS lets one make such tradeoffs and the benefits are proportional to the time you spend doing them. Pete Conklin suggested that a level of effort on the order of 3-5 man years would reduce that size by .6-.75 (to 12K-15K). Included within this effort would be specific changes to operate without a drum, using an RKØ6 or RPØ4 instead. It is not known what the performance penalities are.

RSX-10 Alternative

This alternative suggests offering an RSX-11D compatible system. Compatibility applies to higher level language (FORTRAN), operator interfaces and the environmental issues in general. There would be no bit level compatibility because of the word length differences and, current installations operating on a PDP-11 based system would have to rewrite their machine language routines. Steve Mikulski believes that about 60% of his current systems use Fortran and about 40% use machine language.

The belief is that RSX-11D could be implemented on the KA10L system for probably about the same cost as RSX-11M. There is an obvious learning curve advantage since this would be the fourth implementation (RSX-15, RSX-11D, RSX-11M, RSX-10). There are some unattractive constraints in this project because the designers have to be compatible at every level with something else and there is little design freedom. For instance, RSX-10 would have to be compatible with either TOPS-10 or VIROS file systems and user interface. In addition RSX-11D imposes its constraints and concepts.

Costs

	FY74	FY75	FY76	
VIROS (as-is)	$17K	$ 34K	$34K	; evaluation, releasing
VIROS (shrinked)	$34K	$102K	$68K	; shrink, release
RSX-10	$34K	$170K	$85K	

Note:

The issues of PDP-10/PDP-11 compatibility impact this project. For example, the above costs do not include changing the user-mode PDP-10 software which assumes the current command interface. Presumably we would go to the "DEC Standard Interface" at this point in time and retrofit RSX-11D. These costs are not included here.

INTEROFFICE MEMORANDUM

TO: Distribution

DATE: October 1, 1973

FROM: Gordon Bell GB 12-1

DEPT: Engineering

EXT : 2236

SUBJ: PREJUDICES ON NEXT MID-HIGH-END 11

A machine is probably designed with four major (often conflicting) types of constraints.

1. User/applications--what he wants (or we can get him to want).

2. Hardware technology--what we build from.

3. Systems-software--what is needed to get the performance, and user capabilities.

4. Implementation technique--what architectural styles are around to build from.

5. Project structure

Right now, I see specific values for these constraints:

1. User/Applications

   A. Systems reliability appears to be our biggest problem--together with poor diagnosability (serviceability).

   B. Our major markets include: communications, industrial, and business. All are high reliability markets. To an extent, timesharing in a scientific or computational market is less demanding; but it is highly appreciative of high system uptime.

   C. In the OEM-systems area, a hot-box is desired; at low cost. This conflicts with "B" to some extent.

   D. Need for good interconnection with other computers and systems (e.g. 370). In most applications of interest, this machine will rarely stand by itself.

   E. Lower programming cost. I have gotten inputs from systems OEM's (e.g. Applicon, Boeing, and Industrial Nucleonics) saying this.

   F. Specializable to certain applications and languages.

   G. Good performance and cost/performance over a range of system sizes. The 11/45 did this with MOS, and bipolar options. (A little more foresight, and the 11/40 could have been implemented as a multiprocessor 11/05 or removing something from 11/40.)

2. Hardware technology. These items not present with 11/45. Better bipolar and MOS memories; ECL; and slow LSI. The recent Signetics, bipolar LSI chips are rather small (and dull). They do have a programmable logic array that could be interesting.

3. System software.

   A. Here we have much experience in monitors and languages. Our array of monitors (including the new 10 and the MCP research monitor for the 11) should permit us to do this one right.

   B. Languages. We have knowledge regarding Fortran of all sizes and shapes.

   C. Implementation (system building) languages -- BLISS experience + others (PL/11, XPL).

4. Implementation techniques. There are several basic ideas which are and have been in use, which we might adopt.

   A. Multiprocessors. Symmetrical dual processors have been employed for over 10 years. Since 1970, computers with up to 4 processors have been built. The large multiprocessor system (e.g. 16 processors) is probably beyond our ability to effectively utilize them.

   B. The cache structure has been used since 1969 in Model 85. Many machines use it now.

   C. Multiple cache structure for microprogramming. If we have a user microprogrammed structure; a problem of fetching microwords exists which is similar to normal programs. Namely, microprograms can be relatively large, and unbounded.

   D. User microprogramming. This is probably a misnomer. A 2-level machine where one level is for microprograms (or the first level interpreter) and the second level for languages (e.g. 11, or FORTRAN-execution) appears to have a factor of 2 gain.

   E. Reasonably general purpose emulation. I'd like to see an 11, FORTRAN, NOVA, 8, etc. as some of the target machines which will be interpreted well. Certainly, with our spending a million or so on COBOL-11, we ought to consider executing it half way fast.

F. Diagnostic, ASCII string consoles. We've been working on this at DEC for some time. This also helps in checkout, but it also makes multiprocessors easier to do and control.

G. 16 vs 32 bits. Who cares? the market?

H. An eventual CCD or magnetic bubbles backing-store.

I. Very clean interconnection with networkable-type communications options.

J. Higher reliability Unibus options and structures. Here we can have better busses and/or switches for the Unibus options.

5. Project structure.

The only other prejudice I have about the project now is that software (diagnostics and systems-type) must be more tightly integrated. As a minimum, the software and hardware engineers should sit togther.

GB:mjk

Distribution

Jim Bell
Roger Cady
Dick Clayton
Bruce Delagi
Lorrin Gale
Len Hughes
Chuck Kaman
John Levy
Craig Mudge
Dave Peters
Dave Stone
Steve Teicher

cc: Ken Olsen

attach to New-11 Proposal.

Carnegie-Mellon University

Inter-Office Correspondence

To: Professors Bell, Fuller, McCredie, Reddy, Wulf.

From: Dileep Bhandarkar

Date: September 26, 1973

Subject: Performance Estimates for C.mmp

****

*

The original C.mmp report (Bell et al, 1971) contains graphs showing the memory access rate (MpAR) expected for C.mmp. However, some of the parameters (viz. tp,ta,tw) do not accurately reflect the actual values in the current implementation. A major difference is that the PDP-11/20 has an average processing time of 1150 ns. I calculated this value based on the instruction mix obtained from Aygun's DAME. Also, though the memory has a rewrite time of 400 ns, each module is 8-way interleaved. Thus, for 7 out of 8 cases the rewrite time is effectively zero, assuming random access within a module. With a switch delay of 200 ns and 50 ns delay for Dmap, the effective system parameters are:

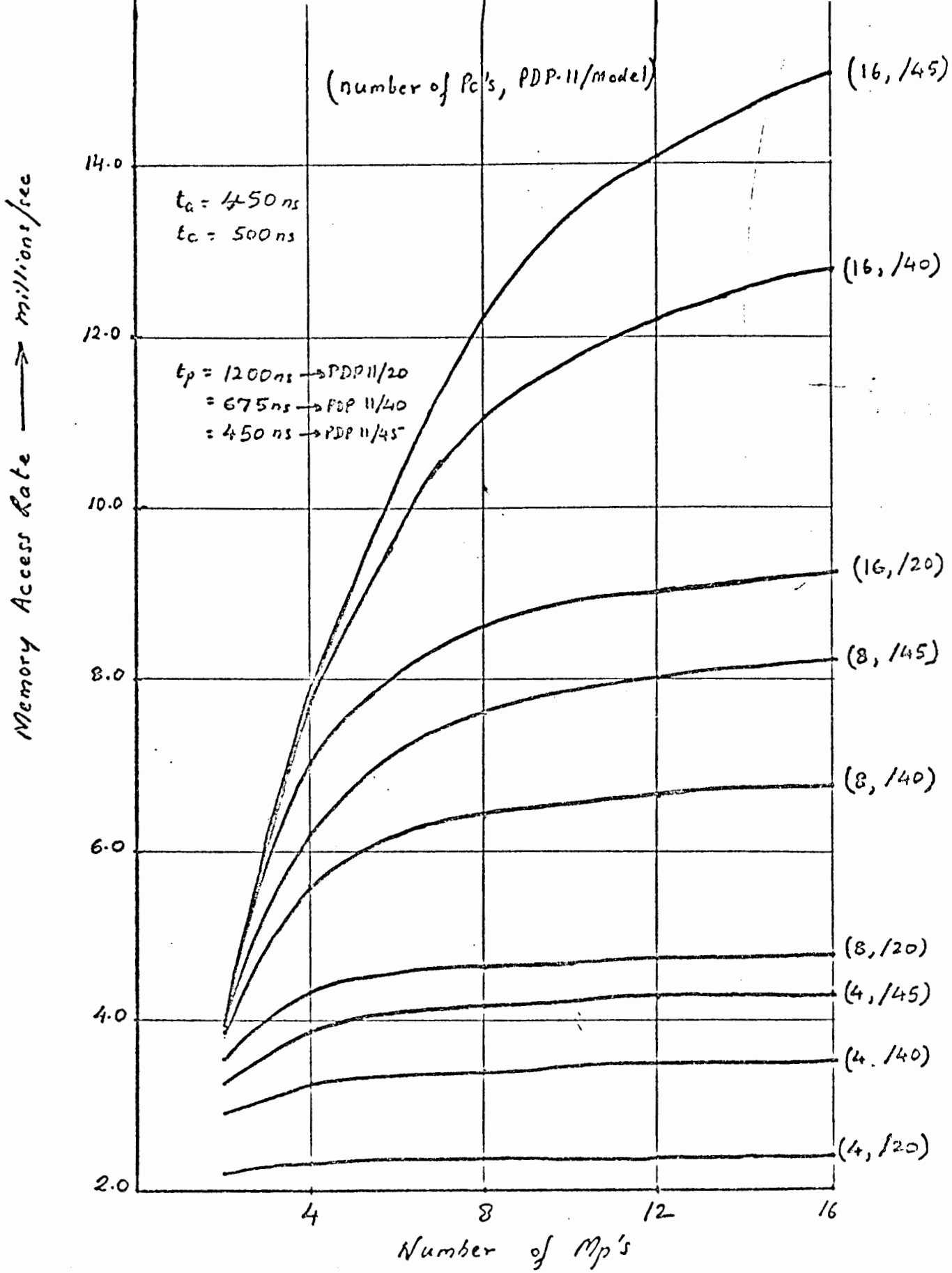
tp = 1150 + 50 = 1200 ns
ta = 250 + 200 = 450 ns
tw = 50 ns

The PDP-11/40 and /45 have typical processing times of 625 and 400 ns, yielding effective values of tp equal to 675 ns and 450 ns.

A graph showing the MpAR for the 3 Pc models as a function of the number of Pc's and nuber of Mp's is appended.

If a private cache (150 ns access time) is provided for each Pc, the improvement over a cache-less 16x16 system is shown below.

Hit Ratio	Percent Improvement		
	11/20	11/40	11/45
0.5	14%	24%	33%
0.7	20%	35%	50%


(number of Pc's, PDP-11/model)
(16, /45)
(16, /40)
(16, /20)
(8, /45)
(8, /40)
(8, /20)
(4, /45)
(4, /40)
(4, /20)
t_a = 450 ns
t_c = 500 ns
t_p = 1200 ns → PDP 11/20
= 675 ns → PDP 11/40
= 450 ns → PDP 11/45
14.0
12.0
10.0
8.0
6.0
4.0
2.0
4
8
12
16
Memory Access Rate → millions/sec
Number of Mp's

INTEROFFICE MEMORANDUM

TO: Products Committee
PL Managers
OC
Marketing Managers
Engineering Managers

DATE: July 18, 1973

FROM: Gordon Bell

DEPT: Engineering 12-1

EXT : 2236

SUBJ: COMMENTS ON BASIC HARDWARE COMPONENTS WE DO NOT HAVE--
(WHEN) WILL WE NEED THEM?

Please rank as to need and time scale:

A Highly Reliable Computer - I believe this is the largest possible product we are overlooking. Also, it would not fail, and given a failure, would tell the user. There is no interest. It appears applicable to Business, Industrial and Computation. It can be built at about a cost of 50% more than our machines. It would have an actual MTBF of several years.

Typewriter - quality printing - useful in business, typeset, PDP-10, LDP (perhaps), Education - needed to produce high-quality reports and manuscripts. Can be achieved by a typewriter, high quality line printer or high-resolution, dot matrix printer. Can use within DEC.

Graphics printing - typesetting (for proofs and eventual photo-offset), Business, LDP, and Graphics. Permits figures to be made in line. Books can be output direct. Ads can be set directly.

Magnetic or Xerography Printing - Can satisfy 2 above. Also is inherently fast.

Touch Tone Input Detector - Useful with synthesizer because it converts any touch tone phone into a computer terminal.

Voice Synthesis - Business (interactive inquiry) Industrial (feedback at terminal), Education (for CAI), Communications and terminals. Can (should) ignore or buy out until need develops.

Voice/Recognition - wait

Computer Output on Microfilm-COM - hopefully we can avoid. Too much is being written when COM is used, with no hope of it being read. Can be used for high quality printing.

Document Reader (Optical Character Recognition) - Business (EDP) processing. Hopefully unnecessary. Once document is in human readable form only this is needed. We should not encourage this because it adds another link with no error checking in data transmission process.

Tablet Input - Business, graphics, laboratory. What is needed here? The resolution continues to improve. Good input method.

Signal Processing (FFT, convolution, etc.) - LDP, Medical, Scientific real time, very sophisticated industrial and new OEMS. Could be quite useful. The basis of many products from spectrum analyzers for vibration testing to speech synthesizers. A low cost, high performance unit might be very attractive to OEM's (e.g. Tektronix).

Desk Calculators (and low cost terminals) - leave alone per se. By using their production techniques they may be useful as:

a. Low cost terminal devices (e.g. RT01, RT02).

b. Consoles on all computers (eliminates present consoles).

Cable TV CATV interface - (Eventual interest when 2-way TV occurs, with computers in homes).

Video Tape Record/Playback - See CATV

Colour TV - might offer UK version.

Voice/Recognition - wait

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Cable TV CATV interface - (Eventual interest when 2-way TV occurs, with computers in homes).

Video Tape Record/Playback - See CATV

Colour TV - might offer UK version.

High Resolution Video - Useful for much text. (Typesetting, Business?, and CAI (EDU). Progress should be monitored, and possibly applied when practical. Fundamentally a cluster - terminal scheme. Alternative to our analog graphics. This is required to get book-like characteristics/use. (We are watching MIT effort closely).

Card Readers and Punches - with 80, 90 or 96 columns. Let's all take an oath to eliminate them. Buy out.

Specialized Card Reader - use when market dictates. Buy out. We could build one for about $25.

Laser and Large photo stores - no interest (markets) that require them now.

Charge Coupled Devices and Magnetic Bubble Memories - not yet practical from a cost standpoint. Will first have to replace RS-series disks. Looks like 75 at least.

Floppy Disk - Business, Lab, PDP-10, OEM, Industrial. A fundamental interchange and recording medium, like cards and papertape, but with ability to be a systems device replacing our cassettes and DEC tape.

Read Mostly Memory - Nitride MOS. Capability to change, but fundamentally permanent when written. Better than core with respect to power off.

INTEROFFICE MEMORANDUM

TO: Distribution

DATE: August 28, 1973

FROM: Gordon Bell

DEPT: Engineering

EXT : 2236

SUBJ: MULTIPROCESSORS--WE PROBABLY SHOULD GO (OR SHOULD HAVE GONE) THERE

With each implementation of PDP-11 processor, it becomes clearer how difficult and expensive (design) they are to implement. Also, unless we spend a lot (e.g. 11/45) high performance ones are difficult to build. Sometime ago we probably should have moved appreciably to multiprocessors.

In my Board of Directors Report, some of the alternatives were outlined for new, larger 11's. A paper (Bill Wulf and I authored) was given in the Board Report (available) which discusses multiprocessors. Bill Strecker of our research staff did the first analytic work predicting the performance of such configurations--and a recent extension of this work pointed out the following trivial case for an 11/20: Up to three 11/20 processors (or slower equivalents--e.g. 11/05) can be attached to a single UNIBUS and interleaved memories. This has been shown theoretically, by simulation, and recently at CMU by experiment. The experimental results with 1, 2, and 3 processors with a 450 ns access memory including bus delays, is:

# Processors	Memory Access $X10^6$ Sec.	Performance (in 11/20 units)	System Cost	Cost-Effectiveness Cost/$X10^6$ Accesses
1	.62	1	1700	2800
2	1.15	1.85	2100	1800
3	1.42	2.4	2500	1750

Namely, putting two 11/05's on a single bus has a dramatic effect on performance and cost-effectiveness. Up to three 11/05's will still increase performance and cost-effectiveness. Four processors begin to saturate the bus and memory (here about .7 us), and little additional performance increase is obtained and the cost-effectiveness begins to increase again.

Using this method, we could have obtained 11/40 and 11/45 performance with a single design since the dynamic performance range from 11/05-11/45 is only about 5 (ignoring floating point).

The point is: we should move into multiprocessors instead of re-engineering processors to cover a range!

Although the paper by Wulf and I show a number of the problems in doing this, the following table outlines some pros and cons.

TABLE OF PROS AND CONS REGARDING MULTIPROCESSORS
(in retrospect to the 11-family)

Pros	Cons
1. General market appeal	Education needed before they can be fully utilized
2. Highly cost-effective	Programming dependent
3. User may configure a system with right processing capacity (i.e. system grows with his load).	
4. We design, produce, stock, and sell fewer types	Problem of floating point and memory management options
5. Higher static reliability	Possibly larger system lowers reliability
6. Greater reliability	Faulty component hard to find
7. Voting designs possible for extreme reliability	Loss of performance

GB:mjk
Attachment
Distribution
Products Committee
Programming Research Group
Roger Cady
Bruce Delagi
Win Hindle
Len Hughes
Bill Long
Julius Marcus
Ken Olsen
Bob Stewart
John Swanson
Ed Kramer
Steve Teicher

INTEROFFICE MEMORANDUM

TO: Board of Directors

DATE: August 13, 1973

FROM: Gordon Bell

DEPT: Engineering

EXT : 2236

SUBJ: SMALL PDP-11's AND LARGE PDP-11's--WHEN WILL WE BE HIT IN THE LARGE ARENA? WHAT IS OUR PLAN FOR 11/45? LET's SEPARATE THEM!

We have been fortunate to occupy a unique position with the 11/45 in which it has been the dominant high performance minicomputer since its introduction. This occurred because:

1. The logic technology used to implement it was the latest (first to use TTL/Schottky);

2. Floating point arithmetic was built in giving it high performance on scientific and higher level language such as BASIC and FORTRAN;

3. Memory management--which allowed software to take advantage of speed;

4. It was one of early machines to use MOS and bipolar memory.

It has been on the market 1 1/2 years. Its backlog is long, and only now are we beginning to see competitive machines which will have at least the characteristics outlined above. The newly rumored (Marcus) Interdata machine is 32 bits, and we expect DG to announce a competitive machine. The DG machine could be an impressive one from a raw speed standpoint, because of its possible simpler structure. Also, there have been a number of 24 bit machines which do quite well against the 11 from a performance standpoint--fortunately for us, the companies are small and there is an aura about 16-bits. Now, as we begin to develop software, we should be able to maintain a competitive edge--but, we must think about the alternatives for a higher performance in this price range.

The easy alternatives that come to mind are:

1. Let the small KL10 do it. They have much good software, and machine features, if it could be priced right. Since a KL10 includes at least one 11/40, will it meet the cost objectives we need (whatever they are)?

2. Let us evolve the 11/45 or 11/40.

   A. User microprogramming--we are looking at improving the performance for certain tasks using the 11/40 with a modification to allow much user microcode. This would run (as a primitive machine) faster than a bipolar 11/45 for a particular small task.

B. Get back on the track with multiprocessors. We were building a multiport memory which would permit multiprocessor computers to be built. I hear the project has been dropped. I favor continuing this project post haste, because it gets us the high performance rapidly by production instead of clever redesign; permits more reliable machines to be built; provides what I think the market is going to want; and finally allows the 45 to be upgraded gracefully. The attached paper (see Appendix M) by Bill Wulf and myself, gives a pretty good case for this structure and why we feel it is the right way to go. The CMU system is now operating with 4 processors, and the 16 processor switch is being brought up now. (Appendix M)

C. Use the CMU switch structure and design for multiprocessors.

D. Add a cache memory to the 11/40 or 11/45. Fundamentally, this is not incompatible with the multiprocessor ideas. In fact, they go well together since memory interference in the switch will be reduced.

3. A new PDP-11/65 which would be based on a 32-bit word. It would have to solve some of the addressing problems which have been encountered in the current 45, and fundamentally would almost give a factor of 2 in performance for the same technology. One would build a 16-bit machine. To build this machine now from either ECL or TTL/Schottky would probably not be wise because of new higher density LSI availability.

4. Use smaller (slower chips) and make a very large multiprocessor.

5. Hold off until much larger scale bipolar integrated circuits become available. We believe that it will be substantially easier to build an 11 on a small number of LSI chips which have performance at the same level as the 40 or possibly 45 within the next year. We are (mildly) interacting with semiconductor vendors to follow the availability of such parts. Although we are uncertain about the availability, although it is becoming increasingly clear that such a part will come into existence. We must interact with Semi to get what we want.

   If we assume that these chips will be available in one year, then it is conceivable that we would still use multiprocessors to gain performance. This would be highly desirable from a user's viewpoint, since we assume that the processor chip costs will go to zero, then the memory and peripheral costs dominate. In order to have a well balanced system (cost-effective), then many processors can be added (since the cost is small). (This point is illustrated in looking at the CMU C.mmp paper by Wulf and I, which gives graphs of cost effectiveness with processors.)

6. Loosely Coupled Networks--with this strategy, we would not worry so much about high performance computers, but instead would design a structure by which a number of computers of arbitrary performance could be interconnected and do load sharing. Although I believe we should do this, I am not certain about the time scale, and how close we can come to meeting performance goals of a single computer. I believe computers will have this structure in a few years. Could we base a development on this approach now?

digital INTEROFFICE MEMORANDUM

TO: Bob Gray

CC: Bruce Delagi
Len Hughes

DATE: 11/13/73

FROM: Craig Mudge

DEPT: 11 Engineering

EXT: 5064 LOC: 1-2

SUBJ: PDP-11 PRODUCT PLANNING AND PDPNEXT

I. INTRODUCTION

At your request I have written down some of my thoughts on where the new DEC system family, which I refer to as PDPnext, will differ from our current machines.

I submit these points as another set of factors against which the new 11 product proposals should be considered. Some proposals will give us more relevant experience for tackling PDPnext than others.

My discussion is necessarily more strategic than technical; I hope that it does not appear too presumptious.

I have looked at the problem from marketing, selling, and programming viewpoints and argue that PDPnext will be different in at least the following respects:

1. Migration - it will emulate some existing architectures.

2. It will be tailorable to specific application areas.

3. It will be easier to program.

4. It will be designed and supported from a total systems, not traditional minicomputer, viewpoint.

II. NEW CHARACTERISTICS OF PDPNEXT

These characteristics result from a maturing of the user community, the need to maintain our current phenomenal growth rate, and technology (hardware and software) trends.

1. The product will be tailorable to special applications

For economic reasons (manufacturing, development, and system software costs) we will use a more general purpose architecture to cover our expanded market.

We have experience in tailoring hardware: the 11 family spans a performance range, the KL10 has a business

instruction set. However, we have not always maintained compatibility. In software I see many more special purpose application languages being designed, e.g., for banking, education, billing. Translator writing systems (or compiler generators) is a software technology which is here now; we could reduce our costs of producing compilers for a myriad of languages and could also offer a TWS as a product.

2. The new system family will emulate some existing machines.

   Our own customer base (20000 PDP-8's, 10000 11's and 300 10's) can provide a lot of replacement business; reprogramming would lose many customers.

   We will be moving into markets where installations have a huge investment in software; a salesman who talks reprogramming will be thrown out. The move to decentralization of corporate data processing (potentially valuable to us because it increases the demand for small machines) does not simplify the reprogramming problems seen by the corporate computer services manager. Should we consider emulating S/360?

   Many of our new customer prospects will be first-time computer users. Their assessment of us will be higher if they see a tangible commitment to user software problems, namely that we offer security to our existing customer base.

   It is a messy problem, but unavoidable. IBM is facing it in designing its S/360-370 successor (they call it migration). Not only is instruction set compatibility required, but also file conversion (the 11 has an 8-bit byte, our others don't) to the new machines' data format and new operating system file format.

3. Performance measurement tools will be provided as part of the product.

   We need to recognize the measuring trend in the maturing user community and master the relatively new field of performance measurement.

4. A DEC re-orientation to total customer needs is needed.

   Much of what I have said can be cast as "taking on IBM head-on". To be successful in taking away customers from IBM and sharing first-time users with them, we must be more concerned with not just the products we deliver, but how we deliver them.

   My observations of our customers, particularly those who are used to IBM support, are confirmed by the September "DATAMATION" user survey. We ranked first (IBM last) on product-performance per dollar, but ranked second last (IBM first) on after-sales service.

   We can maintain our position as the best in the business in supplying raw iron (IBM can't do a minicomputer well, i.e., cheaply), but we must also move towards a more systems-oriented view in designing PDPnext and planning its support. For example, we must develop much more respect for standards and compatibility, we must provide error detection and correction options for commercial users, we must design better human-engineered command languages. Some offerings will cost more, but it seems that many users are prepared to pay for user benefits.

5. Some operating systems functions will be in hardware.

   Some, but only a few, relative to higher level language constructs. Operating systems are still very specific to particular machines; the only element of commonality, and hence the only safe bet for hardware support, is process management (process scheduling, switching, etc.).

   Protection facilities will not only be more comprehensive in scope, but will have a much finer resolution - data base systems will demand protection down to the record level.

6. PDPnext will be easier to program.

   This will result from a large virtual address space and user programming and systems implementation in a high level language. The influence of recent work in programming methodology on language-directed architecture is discussed next.

III. PROGRAMMING METHODOLOGY

Programming is now being studied systematically and data on programmer productivity is becoming available. Moreover, Dijkstra's structured programming is being accepted as a breakthrough in writing correct programs. The new methodologies depend in part on using high level languages with particular language constructs (the structuring primitives) and in part on observance of a systematic discipline (for example, programming by stepwise refinement).

The user community is becoming aware of this work and welcoming it as a solution to its programming mess.

A traditional view of an architecture supporting a high level language says that (1) compiled code must execute efficiently, and (2) that it must allow efficient compilation down its machine language. The growing emphasis on correctness in programs will displace (1) somewhat and substitute understandability as a goal.

The implications of the work in programming methodology are not only on hardware but on software. Our software will be much more carefully designed from a human engineering viewpoint. Two examples are (1) the underlying machine will intrude less (program diagnostics, for example, will be translated into the terminology of the user programming language), and (2) principal user interfaces, such as job control languages, will become either standardized or syntactically compatible with the programming language in use.

Interactive program development will become the usual form of program development. The phrase "programmer workbench" to describe the programmer's console, library support, systems support, etc., carries the right connotations. There will be more than one language translator per language, e.g., an interpreter for interactive debugging and a compiler for production execution. An incremental compiler (it avoids producing a new object code file for each source code change by structuring the object code as a chained list, with each node being a set of object code instructions corresponding to one source code statement) provides an alternative. It provides fast response time and good diagnostics during debugging but the user does not incur the high execution-time cost inherent in interpretation.

The architecture might help; for example, memory might be structured more to reflect the dynamic nature of files in a highly interactive system. The I/O architecture might reflect the needs of a large number of terminals; perhaps more user-oriented terminals will be developed.

Obviously, the discussions above apply to our own DEC programming activities - system software, applications software, and hardware-diagnostics software. Within IBM, structured programming is gradually spreading. Moreover, an internal systems implementation language has been used for some S/370 software and for applications programming.

IV. SUMMARY

Of the characteristics of PDPnext which I have discussed, I view the following as the most difficult to achieve:

1. Migration from existing machines,

2. Tailorable to specific application areas,

3. A DEC re-orientation to total customer needs.

The remaining characteristics:

4. Easier to program,

5. Performance measurement tools provided,

6. Some operating system functions in hardware,

I see as being easier to achieve.

pl

OCT 23 1975

Objectives of Next Machine

- Market influences — reliability, perf., cost, better lang, when CCD, need for innovation
- desirability of a range

what we have that no one else has

Constraints

- technology - components to build from
- techniques

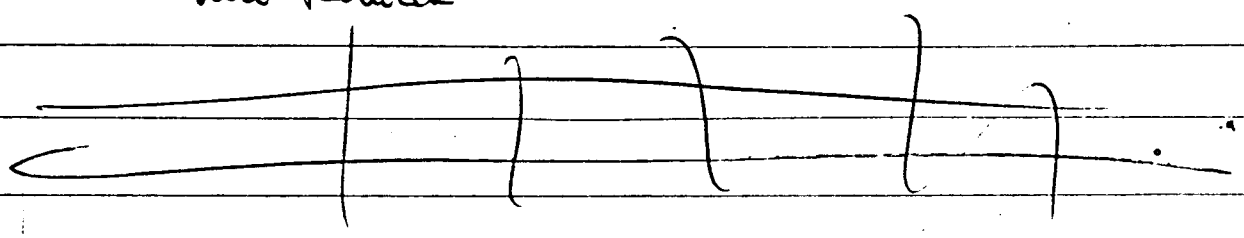
PMS, ISP (w/ user μ code), reliability

The Thing

Evaluate

features, cost, speed, compatability, range

new features



		1350 cost/size	10^6 develop cost / time to market (mos.)	perf.	reliable	user μcode
05 L	repackaged (16K mem?)	~~16K~~ no console	.25 / 9 mos	.8	0	0
40 L	repack/partial redesign (layout)		.5 / ~~13~~	1.8	0	0
05+cache+WCS (cmu)	multi P, WCS, ½μs w/ cache, reliability		.75 / 12-15	2,3, [5, 6.5] 2P 3P	1	1
42 SK	redesign 40S all features; Massbus		1.25 / 18	2, 3.2, [5.4 7.2]	1	1
45 cache	ext. physical addr.; cache; Massbus		.75 / 15	5	0	0
32 bit	32 bit data path & bus; extend address	45 cost	2+.5-2 / 24	6-7.5	1	1
10 stuff	el cheapo 1φ	16K wds ~~5.6K~~	2+.5 / 24	~~KA~~	?	0
46	SW address ext. 45 cached		1.00+.25 / 15	5	0	1
05 F	2bd / relayout		.5 / 13	1.2-	0	0
04	1bd 05		1+ / ~~18~~		0	0
~~01~~	WD	~~$.8K~~ / 4K	1 / 15	~~.5~~	0	0

so hours treat attribute	cost	Mem size physical/virtual	reliability	performance	configuration	compatability	floating point other operations	availability hrs up/day
elephone	unimportant	>128 ~~11/45~~ 11/40	very high & dual for redun.	moderate	multi P RP (dual K) RS, RK, RP	must	no	24
ompetition	competitive	>128 >128	OK	high	RK, RP TTY's; LPT	high level lang. (HLL)	yes	
EM (low)	very low	11/05	OK	cost/perf given low cost	nil	yes	no	
EM system	low	11/40	can stand improvement	cost/perf.		yes	maybe	18-24
siness/TS	unimportant	11/40	improvement/ detection	11/40 OK	RK+RP & ~~LPT~~ TTY's	HLL	no/decimal /string	
DU (high school + junior coll.)	important	11/40	OK	11/40 OK	RK & multi TTY	HLL	no	
DP	important	~~>128~~ 11/40	OK	important	RK, TTY, D/A, A/D	yes	maybe	
ND	moderate	11/40	very important	moderate 11/40	A/D, D/A discret I/O disks	yes	maybe	24
OMM	moderate	>128 11/40	very important	more than 11/40	disks, multi P TTY	yes		24

also how treat attribute

	Innovation
telephone	reasonable (BTL)
computation	speed & space
OEM (low)	high
OEM system	high
business / TS	no
EDU (high school + junior college)	no
LDP	yes
IND	no
COMM	WCS / moderate

NOV 20 1973

To: Gordon Bell
Topic: next-11-who-does-what theory

From: Chuck Kaman
Date: Nov. 19, 1973

Continuing with the discussion we had on groups doing what they like ... There seem to be three possible groups who can and/or want to do a machine. Of these, two are definitely capable of succeeding (that is, actually building a product, although it might not be exactly what we need). The first of these is the Jim O'Loughlin school. They now wish to make an 11/40 class machine on three boards. 11/45 floating point would be an option and the data path (and maybe ROM) for it would occupy another board. The denser ROM's available may allow packaging with the base machine although the speed of these larger ones is poor. There is also the feeling among this school that the floating point can be relatively slow; therefore, it may be included in the base machine in slow form. The WCS option is to be supported only by default (i.e. no inclusion of generally useful data path features for user microprogramming). In addition, they wish to leave out floating point if user WCS is supplied on the argument that the backplane slot is too high a price to pay. Now that caches are understood one will be included as an option to make the machine run almost twice as fast. Multiprocessing ? ans. ?. This school has definite thoughts on manufacturability and reliability as would be expected.

The second of the likely to succeed is Bob Stewart and group who wish to make a fast 11. He, at one time, would have jumped at the chance to make a 100ns 11 or perhaps slow down to 200ns if he had to. Now the accepted project is the 11 ME (memory extension). This is to be the 11 with 45 I/O for greater bandwidth (use of fastbus) and a cache. A few bits added to the KT11C (present 11/45 memory management) allow addressing more physical memory. Using the present 11/45 boards and FPU has a good taste. The cache would be the base for a second processor, probably to be run in PDP-10 style since we know how to write the software. The projected project duration of 18 months seems quite long but they have done a thorough investigation and that may be a realistic figure (?).

Both of these projects are realistic in goals and are being done by people who have the detailed knowledge to carry them off. The only questionable point is whether or not Jim O'L can reduce the 11/40 to three boards without the use of custom I/O which I believe he will have a great deal of difficulty drumming up enthusiasm for using. At present the SOS PLA of North American Rockwell is not second sourced. He will probably need it or there would be essentially no new chips to help reduce the count. Ingenuity may save something, but two boards ? Stewart's project is straightforward and has a minimum of risk. Delagi would probably manage it although he might be tempted by the third project.

The third project is the KL^2 -10 which I will denote KLL to simplify typing. Its advocates are presently Dick Clayton and Len Hughes. In terms of talent this would seem to be enough to start. It is fortunate that the leadership is strong because the project is more risky than the others. It could be done in the 10 engineering group but there is some feeling that the result would be higher priced than necessary and that they would end up supporting it like a big machine rather than a mini. I am not so sure about this. In any event, if the mini engineers were to do a 10 they would have to learn a lot of 10 lore. This might be done by sitting a technical historian and critic like Allen Kent with them. On the technical side - the machine is alternately KA and KI instruction set and speed. At present the only estimate of the manufacturing cost was derived by Rony by removing features from the KL and backing off to S series logic. I believe his figure is high but nothing can be said until the specifications are set forth and some investigating is done. I believe there is some room to trade off. In spite of some people's enthusiasm for the project a more thorough analysis of how it would compete in the market two to two and one half years from now may be in order. This might impact the decision to include KA or KI (L) paging/protect.

Given the resources available we may not be able to do these three. The people are willing and able (for the most part). With the slightest encouragement I believe this is what will end up being built. Dick Clayton's success history would probably make a KLL happen if he pushes for it. If he does not then I doubt it will happen.

objectives and why

fast context switch - for real time response

reliability - for specific markets (communications, industrial products, KL-10 from ends (i.e. consoles))

extend memory space - use Strecker-Wecker proposal and present UNiBUS by using both address and data lines in READ's and rippling on the address lines for writes; the operation which takes longer is a write, but it is relatively rare and it would not be increased more than 20% (for the ripple); of course, this cannot be used on a general ll Unibus(TM) because the memory would not respond correctly to the ripple

also, memory beyond the first 128K words could be placed on a special Unibus which acted as described above, I/O would go to the classic Unibus; the extended memory could be on a different bus

can we mix devices on the Massbus - particularly different speed disks and tapes

do we want the Strecker-Wecker proposal and, or, (which) the present memory management (i.e. if one then which, else both)

Some Observations

There are two reasons for our present concern with reliability:

1. several markets need dependible equipment, and
2. staffing field service at a high enough rate could limit our growth.

In addition, as the number of machines in service (i.e. in the world) grows the need for global optimization increases. That is, decisions must be made whether to build a more expensive unit which costs less to maintain or to continue to supply sufficient field service to maintain lower reliability, but initially less expensive, units.

The markets which need dependible systems (note - systems) are communications (the fastest growing segment of the company), industrial process control, and business data processing. Three aspects of reliability are identifiable: MTTF, MTTR, and error detection. The first two are related to system availability and the last to knowing that an error has been made. For instance, in business processing it is important not to make out checks when all the amounts are incorrect. In some applications detection is the major feature and MTTF/R are subordinate; in others availability is paramount (COMM and IPG).

At the present time training accounts for a large fractions of field service's costs, both dollars and manpower. If we cannot provide service for a machine we can not sell it, for the most part. Thus, at some point the speed with which we can acquire field service personnel and train them limits the company's growth. There are two ways to attack this problem :

1. build in better reliability to reduce the need for field service, and
2. include in the design aids to help field service indentify and fix problems when they arise.

The first approach moves the cost of repair in the field back to the manufacturing plant. This might be done without raising the cost to the customer. One way to do this is to build a more reliable system, another is to implement a field service policy (and a design philosophy) which favors factory repair. The fault must still be isolated in the field and, so, better fault isolation techniques are needed. The most desirable of these would both reduce the time to identify the fault and pinpoint it to the level necessary to allow the swapping of the bad unit for a good one (or whatever policy is to be employed). Among the approaches for achieving this which must be considered is the use of a remoted diagnostic center.

Cached Microcode

Consider a microcontrol, piped as in the 11/40 for speed. Consider the ROM/ACS address space in a cached environment. The low locations are used for ROM and ROM extensions by users; the high locations for the alterable control store. The object is to trace the actions to see how the cached ACS works, and it it does. In order to facilitate running in a multi-task environment a task field of 8 bits (256 tasks) is appended to the cache control field of the ACS. An addressible register in the I/O page holds the number of the present task. A task of zero will match any task. There may be other special task numbers with special matching qualities. The action of the cached ACS is to look up the microword addressed by the microPC then try to match the cache control and task fields. If the match fails a disable level is bussed to disable all state change in registers.[1] The clock is free running and knows nothing about this. One a failure the desired microword is known to not be in the microstore and so must be moved there from main memory by a short transfer program in the base ROM. In this way microinstructions are moved to the high speed ACS on demand. Experiments reported on by Burroughs at COMPCON 72 indicate that caching microinstructions works as well as caching user level instructions. No one has (to my knowledge) appended task bits and used them in the task tag also. Unless a program needs a lot of microinstructions in a short space of time and there is much task switching there should be no problem. The benefit of the task bits is that the state of the machine does not include the contents of the microstore. Note that microcode is assumed to be pure code. Anyone who writes self-modifying microcode will have to wait for a later model for hardware support.

The problems with this approach center around two aspects of the ACS. First, when a microinstruction is not present and must be moved in a complex control sequence must return control to the base ROM and then be able to return to cause execution of the interrupted sequence. Second, the microprogram may have started an I/O transfer but not completed it when the need to move in another microword was detected. The bus is therefore tied up and cannot be used preventing continuation. An additional problem, but at a lower level of concern compared to the other two, is that performance will be degraded by all the cache loading and the interrupt latency will therefore be (greatly) increased.

what can be done and why -

-no basic reduction unless merge EIS and FIS

-can add system throughput, features and flexibility since understand better

-use 10-90 philosophy, add 10% in cost to get 90% of a feature or improvement (example, a relatively small cache of simple structure gets most of the benefits to be derived), the KL-10 went further than necessary

-have more software and user inputs on system problems than on the last go-around

breakthroughs ? -

-none since 40

-TTL S is less expensive so that the cost may be worth the investment for increased performance; technology is forcing us to add performance since we cannot greatly effect cost in any way and technology lets us add speed at a relatively low cost (additional cost, that is)

-saving chips in the data path helps little since it is a small fraction of the machine; even so, if a half width path or a simpler path were used the amount of control might increase to compensate, not to mention slightly reduced performance

-11's do little processing, mostly data movement, so there is little to remove in the way of computation (i.e. in a trade of chips of path for more control and somewhat slower)

-the only real question is whether any of the methods of the 05 can be used in the 40 or are they too slow ?

custom technology -

-no

-risky, bipolar LSI is not yet here, the devices presently being talked about with confidence are no more than 200 gates with noises in the 300-500 gate region

-40 pins is not much and mounting many of these on a board may be a problem

new technology -

-ECL ? May be too expensive and not needed for a mid range machine

-PLA's ? Only one fast one is available (National). Signetics may be too far away and we do not know how reliable a programmable one would be.

-ideas : here we have made advances (cache, ASCII console, microdiagnostics, task oriented variable microprogramming, integrated controller, multiple processors

For what is dynamic microprogramming useful ?

The answer given applies equally well to static microprograms (those stored in ROM's) for the most part. In some applications the ability to load the microprogram of choice allows a necessary dimension in added flexibility. This is obviously true for large microprograms or those which need frequent modification. One is, in essence, ECO'ing the computer so that not having to blast a ROM chip is so desirable as to be necessary.

Since microcode is cached it is possible to write very large microprograms. Even if a software simulator is supplied to aid debugging additional corrections will probably still have to be made after the microprogram is run on the hardware. Another aspect is the desirability of allowing many different tasks to use their own microcode. In this case the cache with task identifying bits can be used to allow microprogramming in a multi process environment. In both cases described above the control store must be alterable.

Specific applications of microprogramming on the 11/40 level of machine include

1. adding instructions - decimal; move, translate and test; subscripting; byte and word string ; list processing (structured data)
2. interpreters - other machines (this requires hardware support to be fast), often called emulation; support of high level languages
3. diagnostics - called microdiagnostics, these allow testing the machine at a lower level than functional diagnostics (instruction level)
4. extension of machine architecture - performance monitoring; trap on conditions not now defined for PDP-11's; I/O channels; redundent calculation for reliability (error detection)

Objectives of the Design and Why They Were Chosen

The specific features needed to achieve the desired qualities in an 11/40 follow-on are listed with the reasons for chosing them.

Unibus(TM) compatibility - *so Digital and customers can use all present peripheral devices*

Unibus(TM) is the only bus (i.e. the main bus for both memory and peripherals) - *to save dollars and complete redesigns*

enhance performance - *to maintain cost-performance since the cost will not be reduced*

allow multiple processors and allow enhancing present model systems by adding new processor(s) as additional processing unit(s) - *for greater throughput, functional decomposition of processing, and reliability; also, ability to enhance old systems is good for image*

be fully compatible with the present 11/40 and/or 11/45 - *software compatability to save reprogramming*

integrate MASSBUS(TM ?) controller - *to allow new mass memory devices on the system at low cost*

include 11/45 compatible floating point in the basic instruction set - *to reduce the number of software releases, improve the 11/40 floating point*

variable microprogramming - *allows emulating, customizing, and tuning for specific applications*

Which machine did we choose and why -

We chose the 11/40 follow-on which is defined as an 11/40 cost machine with enhanced performance and greater configuration flexibility. I do not believe that a submicrosecond PDP-11 can be built for more than 10% less than the present 11/40. Some options, notably the teletype control, can be integrated into the processor as was done in the 11/05, but the data path, microcontrol and bus interface would remain substantially the same. The only approach I see to effect the design at all is to make only the most used instructions fast. But, I do not see how a significant amount of logic would be saved. By integrating EIS and FIS some savings in the data path should be achieved. Also, the larger ROM's now available should also save space. Note that space, saved by reducing the number of chips needed, is the important dimension. Chips imply space (which relates to board cost), power (which is paid for by the Watt), interconnections (which relates to manufacturing cost), and testing (which is labor intensive). I have often said that the 11/40 is at the knee of the cost-features curve. Enough is included in the machine to allow implementation of powerful instructions. For the lack of ROM space and because EIS and FIS were made options this curve was never followed.

- *the 11/40 has the classic minicomputer feel*
- *system level business is presently centered around the 40*
- *this is the highest level system supportable by a simple system architecture, for more performance an 11/45 approach with separate busses for memory and I/O is needed, this raises the cost of the system as a whole as the rest is selected to balance the architectural philosophy*
- *reasonable performance is needed on all applications but since a Unibus based system is not processor bound for this level of processor or above there is no need to further enhance the processor*
- *if more processing power is needed and the application is suitable multi-processor systems can be constructed*
- *by being 11/40 compatible there is little software development for either Digital or users, this is important as the cost of software is rising rapidly*

To: GB

From: Chuck Kaman

Oct. 19, 1973

OCT 19 1973

The attached pages explain the reliability issues as they are now understood. The porpose of our meeting is to gather additional points of view and technical ideas. It is felt by many that we must have a more reliable system from our next design.

The main objective we have is to produce an outline of what is needed for the different market areas and how we will provide those features, with an estimation of the cost. Lorrin needs this information for the report he is generating.

The following pages outline

1. the observations given me at a meeting with the 11 eng. reliability project, and
2. some of my own observations.

Aggenda :

1. specific issues
   a. microdiagnostics and diagnostic aids
   b. manufacturing aids to make a more reliable product (such as the extra gates used to bring out signals in the KL-10)
   c. parity on busses, memory, and mass memory devices
   d. remoted console use
   e. peripheral repair without taking the system down
2. other global issues
   a. keeping up with the competition (if any) in this area
   b. multi-system configurations for increased reliability (these may be multi-processor or peripheral)

Outline of Comments Made at Meeting With 11 Eng. Reliability Group

Reliability

The 11 engineering group has several ongoing investigations on improving the reliability of their product. After talking with them the following points became clear.

1. mechanical -
    a. first generation mechanical designs are not generally reliable, the lessons have not yet been learned for that design (or device)
    b. assembly is not done well; special tools are often needed, these must be made or bought and the production line people taught how to use them
    c. after making devices we often break them ourselves either in test or in delivering them to the customer

2. electrical -
    a. when a power supply dies it can damage the rest of the world (with voltage overloads, for instance) before it is switched off
    b. Unibus - besides the design problems described below the interaction with power supplies causes the entire system to fail if one unit fails
    c. Unibus - devices will be upgraded to allow them to be taken off line without powering down the entire system
    d. Unibus - stressing techniques (voltage and timing marginning) should allow removal of marginal conditions this should help the reconfiguration problem (i.e. being able to put a device on the bus without having to then shuffle devices to get the whole system running)
    e. layout - poor placement of parts can lead to shorts in manufacturing or electronic problems like crosstalk

3. engineering -
    a. designers field of understanding should be extended to include system considerations and manufacturing and field service views

4. software -
    a. reliability requires support by the systems software, this takes primary memory space at least
    b. hardware should report details of an error condition (when trapping to location 4, for instance); an error word of bit flags would be most useful

Some Observations

There are two reasons for our present concern with reliability:

1. several markets need dependible equipment, and
2. staffing field service at a high enough rate could limit our growth.

In addition, as the number of machines in service (i.e. in the world) grows the need for global optimization increases. That is, decisions must be made whether to build a more expensive unit which costs less to maintain or to continue to supply sufficient field service to maintain lower reliability, but initially less expensive, units.

The markets which need dependible systems (note - systems) are communications (the fastest growing segment of the company), industrial process control, and business data processing. Three aspects of reliability are identifiable: MTTF, MTTR, and error detection. The first two are related to system availability and the last to knowing that an error has been made. For instance, in business processing it is important not to make out checks when all the amounts are incorrect. In some applications detection is the major feature and MTTF/R are subordinate; in others availability is paramount (COMM and IPG).

At the present time training accounts for a large fractions of field service's costs, both dollars and manpower. If we cannot provide service for a machine we can not sell it, for the most part. Thus, at some point the speed with which we can acquire field service personnel and train them limits the company's growth. There are two ways to attack this problem :

1. build in better reliability to reduce the need for field service, and
2. include in the design aids to help field service indentify and fix problems when they arise.

The first approach moves the cost of repair in the field back to the manufacturing plant. This might be done without raising the cost to the customer. One way to do this is to build a more reliable system, another is to implement a field service policy (and a design philosophy) which favors factory repair. The fault must still be isolated in the field and, so, better fault isolation techniques are needed. The most desirable of these would both reduce the time to identify the fault and pinpoint it to the level necessary to allow the swapping of the bad unit for a good one (or whatever policy is to be employed). Among the approaches for achieving this which must be considered is the use of a remoted diagnostic center.

APPENDIX 1
OVERVIEW OF PRESENT CHARTS AND PROCESSES

Name	Who	What	Forecast	Spec	Central	Computer Based	Goals and Comments	Problems
Red Book	Prod. Mgmt. Devel. Plan Cont. Plan	MACRO Product Strategy & Devel. Allocation	No	In Back up only	Yes	No	Formalize, rationalize, and communicate MACRO Product Development Strategy. Semi-annual major effort includes inputs from product lines.	Too broad for lots of detail history oriented. Very sens data, fundamental corporate
Business Plan	Prod. Mgmt.	Latest Spec Mkt. Plan PL buy in, etc.	Yes	Yes		No	Both history document and formal decision process for specific product. Includes plans and buy in from all groups associated with product.	Grows over time, often must summary. Product, not syste ented.
Corporate Long-Range Plan & Format	Product Lines (Curtiss)	Forecast based on current products	Yes PL only	?	Yes	Yes	Product forecasts are a quantization of PL long-range forecast.	Can it tie to Manufacturing Marketing goals hard to ch
Yellow Book	Central Development	First and last date, status lots of #'s	No	No	Yes	No	Status of projects cause manager to focus monthly on his responsibilities. Some communication. Some cost focus.	Inconsistent format and con forecast focus.
G.B. ROI	PDP-10	Financial analysis of product	Yes PM only	No	No	Yes	Pricing Business Plan	Needs rewriting.

APPENDIX 2

BACKGROUND & PRESENT REPORTS

A) ORIGINAL MAGIC CHART PROPOSAL

B) YELLOW BOOK TIME LINE OF CURRENT AND ORIGINAL FCS FOR MAJOR PRODUCTS

C) PRODUCT INFORMATION FROM YELLOW BOOK

D) FIRST SHEET OF CURRENT LONG RANGE PRODUCT LINE FORECAST SUMMARY

To: Jack Brown, Arnie, Phil, Larry Wade, Bob Curtis + [illegible]

Cc: OOD, Mal Johnston, Paul Baum, Bill Thompson

2/3

DATE 06-05-74 DISTRIBUTION

~~to~~ Jack, here's some background. Please get with group ~~Bob Curtis / Bill Thompson / I~~ to address how-to

* *

PLEASESEND TO: BILL THOMPSON PK3-2

* *

~~[illegible]~~ design, build and install these.

Gordon

FROM: GORDON BELL

[Magic Charts For Engineering] ← alias

SUBJ: BURKE'S LONG TERM PLAN DEVELOPMENT CHARTS

TO: Lou Burke

I've asked Ron Kronenberg to get with you to make a first pass at a program and system to automate these charts. Given your first pass, they should be easy to automate. The goals of such a program are: ho ho

1. Add the formality that people believe is missing in current system.

2. Generate the many reports we may want that aren't possible by hand.

3. Shorten delay time from input to reports.

4. Make it easy for product lines to do their ordering by having the program interactive. (It should be possible to have a PLM use it directly, or via an indirect input as the current system)

A PL or PM can interact, but reports are generated each 6 months, based on their last inputs. As I see it, there are 2 basic files:

A. Product Definition Files--input by product and/or Engineering Manager. Defines a product, co-components needed for it to be useful (ie, relationship to system and controllers-simplified), availability, price, cost, development cost (t), MTBF.

Each entry can be changed as the product evolves. There are really 4 types of things which can be forecast: software and what it supports; components (eg. disks, CPU's); co-components (eg, controllers); and systems. Possibly systems should be treated as macros--with expansion to specific values--eg. Mid-11 (RSX-11M, 64K, 2RK05). It's not clear how systems should be handled. Product Lines can define new

Note much of this appears in the file of my ROI program.

products.

B. Product Line Orders - They can order each 6 months, based on current status of products, They can define new components and systems. They can only look at summary orders for products, and cannot look at other product lines. They get an explosion to see if their orders make sense for their business forecast.

There are numerous reports of interest:

1. Area products (eg, disks). Latest orders in next 4-6 years for each product (see Burke's example sheet)

2. Area product definitions.

3. Total development plan by area, Status of each product and availability for those products which have business plan.

4. Potential products under examination (non-approved status).

5. Product Changes. Reports only changes since last report.

6. Product line order for a particular year broken down by product and system.

7. A product history. Orders and definitions for each forecast period.

8. Product line orders (+) for a given (usually latest) forecast. The summary gives PL NOR (roughly).

Security

How do we find out who accesses this?
How do we limit the reports?
Is there a report for each running of the program which states information extracted and by whom?

Compatibility

The input format when used manually should be the same as the Manufacturing charts. Get the poop (instruction manual, formats, etc.) on their charts--especially the charts a year later.
May 20, 1974.

Time Scales

The products might ideally be each 3, 6, or 12 months, but a fixed 6 months is probably OK. Update would occur each 6 months, byut is there any reason to limit it?

2-92

ENGINEERING FORECAST FOR RS1011 FH DISK — PREPARED ON 24-APR-74

Project No: 10-000 Proposal Date: 01-Jun-73 Approved: Products Committee 01-Oct-73

Product Manager: John Discus Project Engineer: Hy Density

Description: 10 megaword FH disk, 1ms avg access, 1us xfer rate

Goals: Improve performance of VIROS, RSX, RSTS Operating Systems

Requested by: Disk Steering Group; Software Engineering

HISTORY:	START DESIGN	OPERATE PROTO	LIMITED RELEASE	PUBLIC ANNOUNCE	FIRST CUST. SHIP	PRICE ($/UNIT)	MFG. COST ($/UNIT)	COMMENTS
01-Jun-73	Jul 73	Jul 74	Dec 74	Jan 75	Mar 75	$22,500	$1,500	Original Plan
01-Oct-73	Jul 73	Jul 74	Dec 74	Jan 75	Mar 75	$22,500	$3,000*	2ms avg access
01-Apr-74	Jul 73	Oct 74*	Mar 75*	Apr 75*	May 75*	$22,500	$5,000*	New price, sched

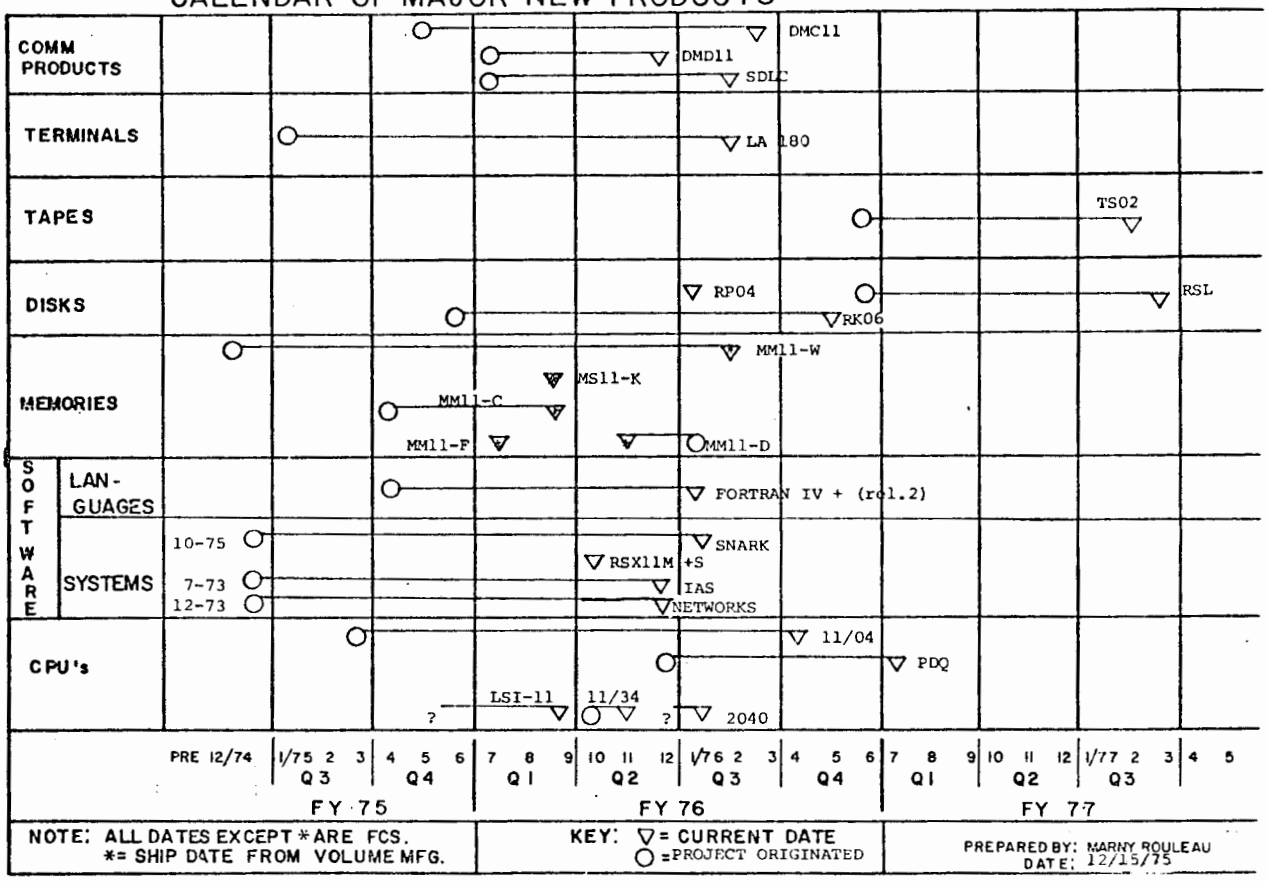
PRODUCT LINE	FORECAST DATE	FY74 Q4	FY75 Q1	FY75 Q2	FY75 Q3	FY75 Q4	FY76 Q1	FY76 Q2	FY76 Q3	FY76 Q4	FY77 Q1	FY77 Q2	FY77 Q3	FY77 Q4	FY78 Q1	FY78 Q2	FY78 Q3	FY78 Q4	FORECASTER
DECsys-10	01-Oct-73				5	20	25	30	30	35	40	40	45	45	45	45	50	50	J. Leng
	01-Apr-74				0	25	25	30	30	35	40	40	45	45	45	45	50	50	J. Leng
LDP-11/45	01-Oct-73				2	4	6	6	7	7	6	7	8	9	7	7	6	10	L. Data
	01-Apr-74				0	10	3	3	8	1	9	1	1	2	4	1	1	8	Anna Log
IND-11	01-Oct-73						2	2	2	4	3	3	3	5	4	4	4	6	R.T. Exec
	01-Apr-74							2	2	4	3	3	3	5	4	4	4	6	R.T. Exec
TOTAL	01-Oct-73				7	24	33	38	39	46	49	50	56	59	56	56	60	66	TOTAL
	01-Apr-74				0	35	28	35	40	40	52	44	49	52	53	50	55	64	TOTAL

FIGURE 4 SAMPLE FORAMT FOR PRODUCT PLAN CHARTS

/ale

2-93

CALENDAR OF MAJOR NEW PRODUCTS



0.5

2-B

CALENDAR OF NEW PRODUCTS

Product	FCS Now	FCS November Yellow Book	Mfg. Planning HVM Date	Description	Additional Information on Pages
Large Computers					
2040	-	-	1/76	DECsystem-20 with KL10 Processor	6.3.1, 8.3.1
RH20/RP04/RS04	-	-	1/76	DECsystem-20 Controller	No Report
SNARK	-	-	-	DECsystem-20 Operating System	No Report
Medium Computers					
IMP	Q1,FY77	Q1,FY77	7/76	11/45 Performance CPU. 11/40 Replacement	8.2.4, 8.2.8.1
MM11/W/WP	2/76***	2/76***	2/76	32K Core Memory	6.1.3.1.1, 8.1.3.1.1
MM11-D/DP	Shipping	11/75*	11/75	16K Core on 1" Board	6.1.3.1.1
RK06	5/76	5/76	6/76	15 Mbyte Cartridge Disk Drive	6.1.10.1, 8.1.4.1
LA180	2/76	2/76	2/76	180cps Dot Matrix Printer	6.1.6, 8.1.6.2
FORTRAN IV+ (Rel.2)	1/76	1/76	-	FORTRAN for 11/45	7.1.2.1, 9.1.2.1
RSX-11M(Rel.2)	Shipping	Shipping	-	Event Driven RTS for 11/10-40-45	No Report
Networks	12/75	10/75		Operating System Interconnector	7.1.2.1, 9.1.2.2
IAS	12/75	12/75		Interactive Application System	7.1.2.1, 9.1.2.1
RSX-11S	Shipping	Shipping		Core Based RTS for PDP-11	No Report
Small Computers					
11/04	-	-	12/75	Low Cost 11/05 Replacement	6.1.10.1,
11/34	-	-	12/75	11/40 Replacement	
LSI-11	Shipping	9/75	9/75	Microprocessor 11/40. No UNIBUS	6.2.2.4,
MM11-C/CP	Shipping	Shipping	9/75	8K Core on 1" Board	6.1.3.1.1

1.4.0

ENGINEERING GROUP Memory Systems Engineering
MANAGER G. Morris

DATE 12/12/75
PAGE 2 OF 2

PROJECT SUMMARY

*Information updated from last report.

PROJECT # MODEL #	PROPOSER, DATE	SHIP DATE PROPOSED, EXPECTED	DEVELOP $ BUDGET, ACTUAL	MFG ENG $ BUDGET, ACTUAL	CURRENT MANPOWER INTERNAL, EXTERNAL	MFG COST PROPOSED, EXPECTED	MFG YIELD PROPOSED, ACTUAL	PROD. RATE PROPOSED ACTUAL	STATUS	DESCRIPTION AND COMMENTS
E98-05161 (32K MOS WITH ECC)	R. Morris 6/26/75	Q1'77	180.4K/ 26.2K*		4	.19¢/bit .19¢/bit		450/Qtr.	Design	Design review held early in December. Action items center around Field Service issued and choice of backplanes.
E98-05158 64K Core	R. Morris 6/26/75	Q3'77	220.0K/ 37.3K*		3	.11¢/bit .11¢/bit		600/Qtr.	Design	Evaluation of new core has flashed the green light. Hard design is proceeding.
E98-05160 2-1/2D Prototype	R. Morris 6/26/75	N.A.	117.1K/ 77.9K*		4	≤.06¢/bit		N.A.		Stack assembly continues. Modules are well along. All hardware will be assembled and ready for evaluation by 1/1/76.
E98-07258 Advanced Memory Technology	R. Morris 6/26/75	N.A.	65.1K/ 5.9K*		1-2	N.A.		N.A.	Continuing	Conceptual design of various LSI-11 has been done based on the 14 mil core. We will review with appropriate people to determine smart thing to do.

6.1.3.1.2

EN-1014A-13-R1073-(644)

2-C-2

7.5.1-c

ENGINEERING GROUP Printer Engineering
MANAGER Ed Corell

DATE 12/5/75
PAGE 1 OF 1

PROJECT SUMMARY

*Information updated from last report.

PROJECT # MODEL #	PROPOSER, DATE	SHIP DATE PROPOSED, EXPECTED	DEVELOP $ BUDGET, ACTUAL	MFG ENG $ BUDGET, ACTUAL	CURRENT MANPOWER INTERNAL, EXTERNAL	MFG COST PROPOSED, EXPECTED	MFG YIELD PROPOSED, ACTUAL	PROD. RATE PROPOSED ACTUAL	STATUS	DESCRIPTION AND COMMENTS
9806690 Print-Head	Abe Gershnow	1/75	837.8K* 917.6K*	31.1K 57.2K*	2,0	$53	95%	1000/mo.	Production Start-Up	Heads presently being built, tested and shipped to Phoenix.
9806830 LA180	Art Williams 6/74	4/76	1496.7K* 865.2K*	39.9K* 24.7K*	4,0	$750	90%	1000/mo	Production Start-Up	First production build Oct. 1975 First shipments from Phoenix in February.
9805122 LA35 and LA35, LA36 Options	None	11/75	349.5K* 301.4K*	3.2K* 2.6K*	3,0 3,0	-	95%	-	Production Start-Up	Additional people added. Schedule stabilized.
LPP Printer Project	None	4/76			2,0	-	-	50/mo.	Evaluation	All people hired. Evaluation in progress. Two month schedule slip due to vendor delay.

6.1.6

2-C-3

SOFTWARE SYSTEM RELEASE DEFINITION TABLE
(Future releases are best estimates only)

	R1	R2	R3	R4	R5	R6	R7
RT-11	V01-15 9/73	V02 11/74	V02B 6/75	V2C[1] 1/76	V3 9/76		
RSX-11M	V01 11/74	V02 9/75	V03 6/76	V04 4/77			
RSX-11S	V01 9/75	V02 6/76	V03 4/77				
RSX-11D	V2A 5/73	V4A 3/74	V4B 1/75	V6A 6/75	V6B 11/75	V6C Q1/FY77	
COMTEX	V1 6/72	V2 7/73	TC/D[3] 6/75				
DOS/BATCH	V4A 10/71	V08-02 11/72	V08-08 4/73	V09-19 10/73	V09-20C 5/74	V10-01 5/75	V10-02 Q2/FY76
IAS	V1 12/75	V2 3/76	V3 1/77				
RSTS-11	V3C-32 3/72	V4A-12 10/72	V4B[4] 4/75				
RSTS/E	V05-21 7/73	V5B-24 11/74	V5C-01[5] 3/75	V6A 7/75	V6B 9/76	V07 Q1/FY78	
MUMPS-11	V1B 1/73	V2A 9/73	V3A 12/74	V3B 10/75			
TOPS-10	V5.07 8/74	V6.01 11/74	V6.02 8/75	V6.03 Q2/FY77			
TOPS-20	V1 1/76	V2 Q3/FY77					
OS-8	V1 7/71	V2 10/72	V3 5/74	V3B 7/75	V3C 11/75		
RTS-8	V1 5/74	V2 10/75					
COS-300	V3.112 3/72	V3.07 3/74					

1 Predominantly for supporting the LSI-11.

3 Front end concentrator based on COMTEX to interface to RSX-11D.
4 Bug fix release for old customers only.
5 Prerelease available internally 1/75 for RJP04 support only. Distribution medium is 9 channel magtape and RK05 only.

SOFTWARE SUPPORT OF NEW DEVICES

(For planning purposes only; some dates are best estimates)

DEVICE	Date Avail for Soft Debug: WORKING UNIT	Date Avail for Soft Debug: PRODUCTION	PUBLIC ANNOUNCE	1ST SHIP	RT11	RSX-11M RSX-11S	RSX-11D	COMTEX		IAS	RSTS-11	RSTS/E	MUMPS-11	TOPS-10	TOPS-20	OS/8	RTS/8	COS-300	PLAN REF #
								OPTION: TAPES											
TJU16		NOW	ANC'D	NOW	NOW	NOW	NOW	-		R1	-	NOW	R4	-	R1	-	-	-	-
RX11/RXØ1		NOW	ANC'D	NOW	NOW	NOW	-	-		-	-	NOW [3]	-	-	-	-	-	-	-
RX8/RXØ1		NOW	ANC'D	NOW	-	-	-	-		-	-	-	-	-	-	NOW	R2	- [5]	-
TU47				Q2,77	*	*	*	NO SOFTWARE MODS -			-	*	*	-	-	-	-	-	-
TM8E/TSØ3			ANC'D	NOW	-	-	-	-		-	-	-	-	-	-			-	-
TS11/TSØ2																			
RXV11/RXØ1		Q2/76	9/75	11/75	R4	NOW	-	-		-	-	-	-	-	-	-	-	-	-
TMB-11		12/75		4/76	*	*	*	NO SOFTWARE MODS -		*	-	*	*	-	-	-	-	-	004

3 Not as distribution medium or system disk

5 Supported under COS-31Ø (6/75) by Business Products

2-C-5

Appendix G.
(first page of 7)

DIGITAL EQUIPMENT CORPORATION
LONG RANGE PRODUCT FORECAST
FY'75-FY'79
BOB CURTISS, CORPORATE PLANNING
TRANSFER COST AND MIP IN THOUSANDS
COPFOP.RPT
10/13/75

Old Money Runs

	1975			1976			1977			1978			1979		
	QTY	TOTMLP	TOTTRC	QTY	TOTMLP	TOTTRC	QTY	TOTMLP	TOTTRC	QTY	TOTMLP	TOTTRC	QTY	TOTMLP	TOTTRC
CLASS K OPTIONS															
8A	400	520	320	4410	5733	3263	5311	5842	3107	4717	4717	2524	3392	3392	1815
8E	330	857	351	1001	1992	1065	446	981	570	88	194	112	106	233	135
8M.F.	0	0	0	900	1341	811	144	215	156	24	36	26	24	36	26
LSI11	0	0	0	62	61	27	8065	6452	2282	10291	7718	1811	10161	7621	1788
LSI-X	0	0	0	0	0	0	0	0	0	1036	934	208	6010	5409	1202
11/04	0	0	0	949	1114	1034	4340	4998	4253	5242	5903	4822	2000	2250	1840
11/R	0	0	0	0	0	0	0	0	0	623	1432	623	4589	10554	4589
11/S	0	0	0	0	0	0	0	0	0	1917	2300	958	6762	8115	3381
11/05	80	200	124	168	509	260	0	0	0	0	0	0	0	0	0
11/10	434	1085	638	1322	3965	2313	439	1317	768	68	203	118	1020	3060	1785
11605	0	0	0	520	2859	826	3179	15896	4546	4575	20586	6176	2002	9009	2703
11A40	0	0	0	115	807	205	1530	9179	2448	1586	7942	2398	1877	9384	2834
11/35F	262	2177	623	551	5836	1309	120	1272	285	0	0	0	0	0	0
11/35S	157	1288	321	296	2444	608	60	492	122	0	0	0	0	0	0
11/35J	105	754	177	138	990	232	30	216	51	0	0	0	0	0	0
11/40	595	3035	714	968	4939	1162	294	1499	353	113	578	136	16	82	19
11/45	345	7888	1899	203	4645	1118	23	516	124	14	320	77	4	91	22
11/50	23	526	115	11	251	55	6	137	30	4	91	20	0	0	0
11/70	34	1016	358	722	21835	7182	986	29098	9489	711	20986	6829	606	17881	5819
11/PDQ	0	0	0	920	11954	3216	3749	46664	13122	5301	63017	18555	4732	56784	16562
11/XY	0	0	0	0	0	0	0	0	0	38	450	0	981	11771	2943
11/32	0	0	0	0	0	0	19	323	82	691	11739	2969	2146	36474	9011
11/85	0	0	0	0	0	0	9	153	38	15	253	63	20	337	84
KK8-AA	0	0	0	120	96	26	100	80	22	0	0	0	0	0	0
INDIA (14)	335	4690	1629	425	5950	2321	220	3080	1201	0	0	0	0	0	0
CPU TOT	0	24436	7468	0	77322	27038	0	128611	43049	0	149998	48426	0	182482	56558
CLASS F OPTIONS															
KC8-AA	0	0	0	1580	632	174	2900	1160	319	3000	1200	330	2200	880	242
KD83	0	0	0	32	19	3	34	20	4	37	21	4	44	26	5
KM8-AA	330	165	44	394	197	46	550	220	64	540	216	63	510	204	59
8A-EXP	0	0	0	175	175	53	600	600	180	600	600	180	400	400	120
DK8-EP	0	0	0	28	21	5	32	24	6	37	27	7	46	34	8
DKC8-AA	330	165	41	2035	1017	275	3500	1400	438	3570	1428	446	2690	1076	336
KE8E	40	52	7	48	62	10	20	26	4	0	0	0	0	0	0
BE8A	0	0	0	40	26	6	46	30	7	53	34	8	66	43	10
KW11L	505	177	9	574	201	7	652	298	11	1126	394	15	1397	489	18
KW11P	75	52	8	600	560	62	1244	871	96	1810	1267	139	2371	1660	183
KE11E	316	465	68	646	952	113	656	965	114	780	1155	137	1081	1589	188
FFPP	20	206	46	27	216	49	197	1579	987	275	2199	1374	401	3210	2006
KA11A	5	34	5	34	252	69	0	0	0	0	0	0	0	0	0
BA11L	0	0	0	841	479	160	2800	1596	532	4725	2693	898	5600	3192	1064
BA11R	0	0	0	32	50	26	1244	1952	995	2084	3272	1667	2479	3893	1983
DD11-D	0	0	0	547	137	37	2800	700	190	5400	1350	367	6400	1600	435
M-7850	0	0	0	703	632	42	2500	2250	150	4000	3600	240	5000	4500	300
11V BOX	0	0	0	0	0	0	4000	5200	1164	5000	6575	1480	7250	9534	2146
KUPDQ#	0	0	0	55	221	55	441	1764	441	579	2316	579	721	2884	721

FIGURE 1

DEVELOPMENT PROCESS
(Function of Time)

PRODUCT PHASE	ACTIVITIES (AND GATE TO NEXT PHASE)	BUSINESS PLAN PHASES
Preconcept	Request to study by PC, PLM, Dev. Mgr., etc.	
	--Development Manager approves--	
Study (1/4-1/2 year)	PRODUCT MANAGER APPOINTMENT	
	--TPGC approves--	
Proposal (1/4-1/2 year)		Original Business Plan Development with sales projection.
	--TPGC recommends; PLMC reviews; PC approves--	
Design and Tool (1-2 years)	Design Reviews by Eng. Committee Mfg./Eng. Committee reviews Mfg. Plan	Manufacturing part Support part (training & service) Sales part
	--TPGC recommends; PC revies; PLMC approves--	
Produce, Sell Support (2-3 years)	--TPGC recommends; PC approves--	--Rejuvenation plan (redesign)
	--TPGC recommdns; PLMC approves--	
Rejuvenate (1-2 year)		Traditionalize plan.
	--TPGC recommends; PLMC approves--	
Traditionalize (? years)		
	--TPL Manager recommends; PLMC approves--	
Death (4 1/2 - 8 yrs)		

CORPORATE POLICY MEMORANDUM

NUMBER 75-8
REVISION
Page 1 of 4

DATE: November 20, 1975
FROM: John Fisher
DEPT: Administration
EXT: 4515
LOC/MAIL STOP: ML 12/1 A-50

ML121 00080 HDQ 644 POL-1
GORDON BELL ML12/A51
D.E.C. BUILDING 12-1

SUBJ: MARKETING COMMITTEE/OOD INTERFACE

DEC's product strategy is determined through an interaction of the Marketing Committee and the Office of Development. The purpose of this policy is to define the formal procedures for product decisions between these groups.

SUMMARY

Interaction regarding products occurs at two levels:

- the strategic level
- the individual product level

Strategic review will consist of:

Continuation of the process started last spring with the Red Book strategy.

Namely on a semi-annual basis:

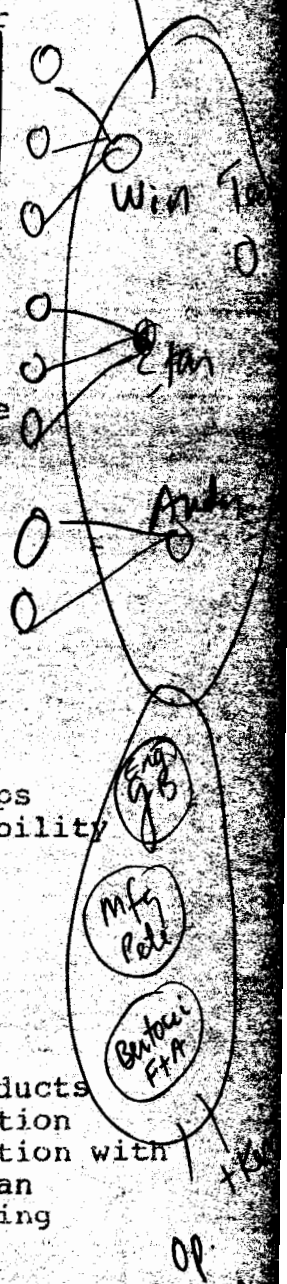
Propose updates to strategy	- OOD
Review strategy	- key Product Lines
Approve and/or require changes to strategy	- Marketing Committee

Individual product review consists of:

Institution of a formal review process in which the steps are clearly defined and which allows considerable flexibility regarding the time investment by the various management committees in the Company. The reason for this is that not every product is a hot issue all the time and this feature allows focus on the hot issues.

INTERACTION AT THE INDIVIDUAL PRODUCT LEVEL

This is the process whereby business plans for the major products are prepared by the Product Manager and reviewed. The intention of this process is to communicate the most amount of information with the least amount of hassle. A six to eight page business plan summary will be the information that is circulated. Supporting information in excess of the summary will be published in an



Corporate Policy Memorandums are prepared at the request and approval of the Operations Committee. This Policy was prepared by Phil Laut - Engineering Finance who can answer questions concerning the contents. Managers receiving the Policies should communicate them within their group.

CORPORATE
POLICY MEMORANDUM

DATE: November 20, 1975
FROM: John Fisher
DEPT: Administration
EXT: 4515
LOC/MAIL STOP: ML 12/1 A-50

appendix that will not be distributed but will be available upon request for the people who want it. Attached are a summary flow chart that describes where the information goes and a more detailed chart that shows content and purpose of the various documents.

PROCEDURES

There are a couple of things that we can do to make the process effective:

1. Documents will be distributed to the various groups and committees. An oral presentation will not be scheduled unless requested.

2. One OOD Staff Meeting per month will be set aside for review of business plans.

3. Prior to OOD approval (where shown on the summary flow chart), the business plan will be distributed to OOD members and to cognizant managers in Manufacturing, Field Service and Software Support, as applicable. A minimum of two weeks will exist between distribution of the business plan and the scheduled review at OOD. The purpose of the two week period is to allow recipients of the business plan to review it in their groups and to decide whether to call for a presentation by the initiator at the next OOD monthly review of business plans.

4. The process can start in two ways. In cases where the proposed product is part of the approved strategy, all that is needed is distribution of the applicable section of the strategy document as notification that work is starting. In cases where a product that is not included in the current strategy is proposed what is required to start the process is a brief (two page) document defining the business and technical justification for the proposed design.

For certain Key products our policy encourages competing design efforts. Funding in such cases will be limited to prototype development and a choice between the alternatives will occur before funds are committed for production start-up.

Distribution of Product Planning Information

Summary Flow Chart

Phase #	Product Phase Name	Flow Chart for Written Material
None	Before the beginning	Semi-annual strategy update reviewed by key Product Line Managers. Approved by Marketing Committee.
0	Preliminary Planning	Two Page Rough Plan → OOD for Approval → PLM & MC for information and if requested, for review.
1	Design	Phase I Business Plan → PSG for Opinion → OOD for Approval → PLM & MC for information and if requested, for review.
2	Prototype Build and Debug	Phase II Business Plan Including Manufacturing Plan → PSG for Opinion → OOD for information and if requested, for review. → M/E Committee for Approval → PLM for information and if requested, for review.
3	Production Start-up	Pricing Proposal → PLM & MC for Approval
4	On-going Production	Changes in production rates are caused by and monitored by the forecast/commit system. Changes in price are approved at PLM and Marketing Committee. Product life data is reviewed quarterly by product managers for any indicated requirement to phase out products.

The purpose of this chart is to list at the summary level, the four phases of product development and to show the written material that will be published at the end of each phase.

Phil Laut
9/17/75
/ale

Distribution of Product Planning Information

Chart I

Phase #	Phase Name	Events Needed to Progress to Next Stage	Documentation Planning and Approval to Progress to Next Stage	Purpose of Documentation	Originator of Documentation	Routing of Documentation	Events that Occur During this Phase
None	Before the beginning	Idea - Generation of Development Strategy	None	None	None	None	
0	Preliminary Planning	Generation of brief preliminary plan	Two pager (preliminary plan). OOD Approval	To allow early management review of new designs. To communicate to OOD and the rest of the Company about what is being designed. To allow determination of whether proposed design agrees with current strategy or whether strategy needs to be revised.	Product Manager/or initiator if Product Manager not appointed	Product Manager , or initiator; sends to OOD (Phil Laut). The two pager will be reviewed at monthly OOD and decision will be communicated to originator. Subsequent distribution to Bill Thompson for Marketing Comm. and Product Line Mgrs. Comm.	Appoint Product Manager. Establish design team.
1	Design	Chose implementation for design	Phase I Business Plan. OOD Approval	To communicate the anticipated business impact of the proposed implementation. Business Plan at this stage would have firm data on the technical characteristics of the proposed product, like performance, features and cost and firm data on engineering expenses. Volume, price, cost and reliability information will by nature be preliminary.	Product Manager	Product Manager presents at Product Steering Group (PSG). Product Manager sends to OOD (Phil Laut) for approval. Phase I Business Plan will be reviewed at monthly OOD and decision will be communicated to originator. Subsequent distribution to Bill Thompson for Marketing Committee and Product Line Manager's Committee.	Generate specifications. Complete paper design. Build breadboard. Design review.
2	Prototype build and debug	Operating Prototype	Phase II Business Plan including Manufacturing Plan. M/E Committee Approval	To communicate final Business Plan for the product before the major capital equipment and inventory commitments are made. To communicate the planned steps to achieve high volume manufacture.	Product Manager Manufacturing Mgr.	Product Manager presents at Product Steering Group (PSG), sends to OOD (Phil Laut) for information. Subsequent distribution to PIM. M/E Committee approves (Arny Goldfein).	Build and debug prototype. Design of manufacturing process. Buy initial tooling. Manufacturing cost estimate by cost accounting.
3	Production Start-up		Pricing Proposal Marketing Committee Approval	Obtain approval from Marketing Committee for the price and announcement of a new product.	Product Manager	PIM Committee Marketing Committee (Bill Thompson)	Implement manufacturing process. Pilot production. Buy final tooling. Write necessary marketing guides, brochures and other documentation.
4	On-going production		Changes in production rates are caused by and monitored by the forecast/commit system. Changes in price are approved at PIM and Marketing Committee. Product life data is reviewed quarterly by product managers for any indicated requirement to phase out products.		Product Manager	PIM Committee Marketing Committee	Public Announcement. Market introduction. On-going manufacture and sale.

Phil Laut
2/7/75
ms

81

digital

INTEROFFICE MEMORANDUM

TO: OPS Committee LOC/MAIL STOP

DATE: February 9, 1976
FROM: G. Bell/D. Clayton
DEPT: Computer Systems Development
EXT: 2236/3638
LOC/MAIL STOP: ML12/A51 - ML5/E71

SUBJ: WOODS DISCUSSIONS ON CHARTS

Attached are several pieces of material to help focus discussions on the question of Marketing-Development communications.

1. Memo on Present & Proposed Processes and Goals.
2. Proposed Product Status Chart.
3. Appendix 1 Overview of Present Charts & Processes.
4. Appendix 2 Background & Present Reports.
   a) Original Magic Chart Proposal
   b) Yellow Book Time Line of Original and Current FCS for Major Products.
   c) Product Info From Yellow Book
   d) First Sheet Of Current LR Product Line Forcast Summary.

digital

INTEROFFICE MEMORANDUM

TO: Operations Committee
cc: COD

DATE: February 9, 1976
FROM: Gordon Bell/Dick Clayton
DEPT: Computer Systems Development
EXT: 3638
LOC/MAIL STOP: ML5/E71

SUBJ: "MAGIC" MARKET - Development Charts

For some time, we have all said it would be smart to have some sort of chart system between Marketing and Development. Our perception is "Charts" are the physical embodyment of some process between the organizations. A number of processes and chart like documents exist today. The current question seems to be: What new processes or process modifications are in order to operate more effectively over the next 1-4 years.

Below is the table of current process-documentation pairs. A quick glance suggests that we have a great deal of information flowing, but it is relatively difficult to integrate and understand.

Current Process - Document Pairs

Red Book Process and Family Plan back up.
Product Business Plans.
Yellow Book.
Product Line Long Range Plans and Forecasts
Product Line Manufacturing Forecast.

Before posing a solution to the "Chart" problem, it might be appropriate to list some possible goals for process improvement between Product Lines and Development. A few that come to mind are:

More Trust, Lower Hassle
Longer Term Focus (Development and Marketing)
Better Development Management.
More Integrated Development Strategies.
Better buy in by Market Groups.
More Visability to MACRO Product Strategies.
More Visability to MACRO Marketing Strategies.

Proposal For Product Status Charts

The expanded "Red Book" process is probably making as much progress as we can currently stand on the issues of strategy integration and

moving the time focus out. A major current problem seems to be the trust issue.

By clearly showing the medium term product strategy in terms of those product characteristics most critical to a Product Line, it should be possible to reduce hassle and build trust; thereby, allowing work on the real problems.

Format

1) Up to 3 pages showing recently released or future released (up to 24 months) major Hardware products. Chart should show name, product manager, unit cost, and planned ship volume.

2) Major Software products shown on a Time Line diagram (Unit cost and volume generally not critical to product lines)

3) One page of back up per product that shows history of cost, volume, and spec of the product (honestly, what has really happened over time).

4) Timing (once per quarter?).

Questions

1) Security

2) Format for distribution (Yellow Book, New list, etc.)

3) Different goals, data, timing, etc.

4) Doesn't address Product Line buy in.

Systems

There is a major need to focus on our products as collections of hardware, software, and services. It seems that many Product Lines sincerely wish to communicate about products and product strategies at this more integrated level. COD owes a clear proposal for implementing system management in a way that provides such a focus without unduely removing Product Lines from influencing development or isolating developers from the customers.

We are preparing such a proposal and expect its implementation after the present "Red Book" cycle.

PROPOSED:

PRODUCT STATUS CHARTS

SECTION 1 SOFTWARE TIME LINE DIAGRAM

SECTION 2 HARDWARE PRODUCT COST & SCHEDULE

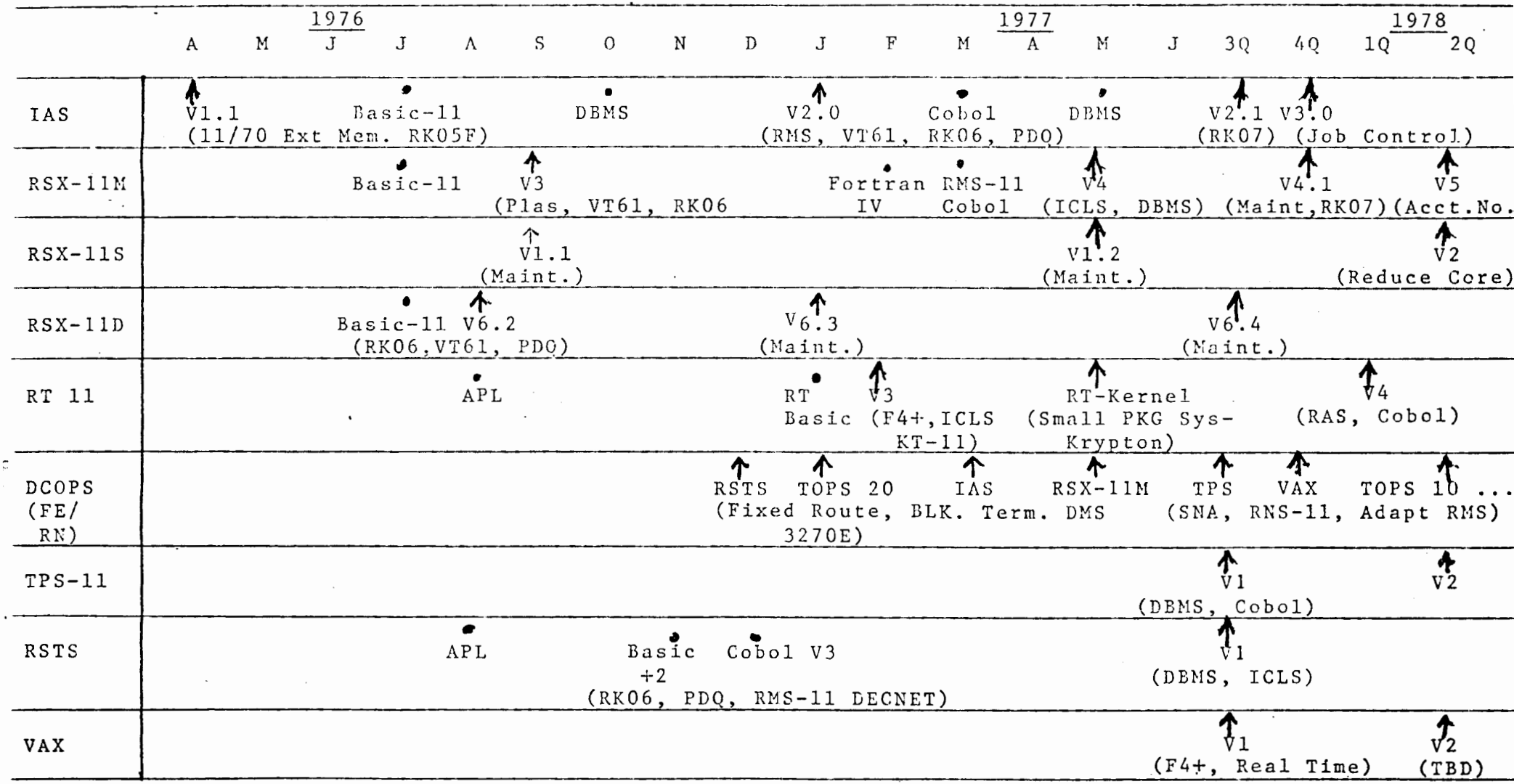
SECTION 3 HARDWARE PRODUCT HISTORY

SECTION 4 SOFTWARE PRODUCT HISTORY

The attached material has been assembled as an example of a possible format for product status charts. Your response and suggestions are solicited. This particular set of material was collected rather rapidly and in some cases is technically incorrect. Please work with the format not the content of this particular set of data.

Dick Clayton
2/8/76

SOFTWARE ENGINEERING & MAJOR RELEASES



LEGEND: ↑ Major Release

• Unbundled Major Products

Product Name	Estimated Transfer Cost/ Date	Volume① to Customer (Units) FY 76 Q3	FY 76 Q4	FY 77 Q1	FY 77 Q2	FY 77 Q3	FY 77 Q4	Product Manager
Peripherals								
RX01	$ 1,000/Q1 77	1,700	2,200	2,000	2,300	2,500	2,800	P. Bauer
TS03	1,700/Q3 76	115	125	145	135	135	170	C. Ju
TU16	3,200/Q3 76	290	375	345	350	300	300	C. Ju
TU10W	3,350/Q2 77	335	310	230	200	165	175	C. Ju
RK05	1,500/FY 77	2,225	2,370	1,620	1,500	1,500	1,400	K. Srivastava
RK05F	1,500/FY 77	0	0	250	350	450	500	K. Srivastava
RK06	2,300/FY 77	0	0	25	350	700	1,000	S. Orr
RP04	11,600/FY 77	550	625	375	290	255	265	K. Smith
RP05	11,800/FY 77	0	60	200	290	325	350	K. Smith
RP06	12,400/FY 77	0	80	120	160	265	290	K. Smith
RPR02	3,800/FY 77	200	265	175	140	30	35	K. Smith
RS04	6,000/FY 77	40	50	45	50	50	55	K. Smith
VT50	570/Q4 76	1,685	1,385	1,100	1,185	1,000	1,010	M. Wurster
VT52	600/FY 77	1,365	2,335	2,440	2,795	3,365	3,675	A. Dziejma
VT61	930/FY 77	110	290	545	585	740	810	A. Dziejma
VT Copier	260/FY 77	175	350	1,085	1,500	2,000	2,000	C. Blasi
LA36	745/Q3 76	9,600	11,950	9,500	11,000	12,000	13,500	A. Huefner
LA180	800/FY 77	0	300?	1,000	3,000	4,000	6,000	C. Bickoff
CPU's								
LSI-11	360/FY 77	4100		6,000	6,000	6,000	6,000	L. Halio
11V03②	2,700/Q3 77	300		375	375	400	500	L. Halio
Momzur③	1,275/Q2 78	0			0			L. Halio
Krypton								
Floor Unit	1,845/Q2 78	0				0		L. Halio
Table Top	2,118/Q4 78	0				0		L. Halio
11/04	1,600/FY 77	300	500	600	700	800	900	M. Tomasic
11/34	2,200/FY 77	100	500	800	900	1,000	1,100	M. Tomasic
11/IMP(PDQ)	3,650/Q4 77	0	0	20	150	400	700	R. Gray
11/70	12,100/FY 76	175	220	200	220	230	250	J. Carnes
VAX								
Star A	9,000/Q4 78	0				0		B. Delagi
Star B	3,000/Q1 79	0				0		B. Delagi

Product Name	Estimated Transfer Cost/ Date	Volu to Customer (Units) FY 76 Q3	FY 76 Q4	FY 77 Q1	FY 77 Q2	FY 77 Q3	FY 77 Q4	Product Manager
CPU's								
FP11-C	$ 1,180/Q3 76	40	160	200	240	240	240	J. Carnes
Memory								
MF/MM11WP (32k Core)	1,368/ 1,114/FY 76	141	616	1,647	1,792	1,745	1,871	C. McCarthy
MJ11BE (64k Core)	2,150/FY 76	0	120	53	400	450	500	C. McCarthy
MM11CP (8k Core)	484/FY 76	300	300	300	300	300	300	C. McCarthy
MM11DP (16k Core)	651/FY 76	1,500	4,000	3,500	3,000	3,000	3,000	C. McCarthy
MS11JP (16k MOS)	487/FY 77	600	800	700	700	800	1,000	C. McCarthy
MS11AP (4k B/P)	970/FY 76	200	700	400	300	200	?	C. McCarthy
MMV11A (4k Core)	328/FY 76	1,400	900	600	600	600	600	C. McCarthy
MSV11B (4k MOS)	168/FY 76	1,700	1,900	2,200	4,000	5,000④	3,500	C. McCarthy
COMM								
DZ11 (8 lines,ASYN)	485/FY 77	813				3,332		T. Lauck
DU11 (single ln,SYN)	210/FY 77	1,098				861		T. Lauck
DUP11 (single ln,SYN)	230/FY 77	270				771		T. Lauck
DMC11 (single ln,SYN)	583/FY 77	164				578		T. Lauck
DV11 (16 Lines,SYN)	2,596/FY 76	289				330		T. Lauck

Notes:
① If single figure, entire period covered
② Including DS-311
③ Product being redefined. No P/L or Engineering funds presently.
④ Introduce 16K MOS

11/70 (Formerly 11/55)

Product Mgr.: Janice Carnes

Definition: The 11/70 was conceived of as a high end, PDP-11 with emphasis on system throughput, at 11/45 cost; having the 11/45 instruction set and floating point unit. A 2 KB bipolar cache provides effective memory cycle times of less than 400 ns. Physical memory is expandable to 2MB (with a planned expansion to 4MB). In addition to the PDP-11 UNIBUS, a high-speed 32 bit I/O bus has been added for high throughput performance (5.8 MB bandwidth). Later, after FCS, a project was started to improve the floating point speed, which resulted in the FP11-C with a speed of 2½ times the FP11-B. Another major design goal of the 11/70 was emphasis on R.A.S.

Date:	Announce:	FCS:
1/74	12/74	3/75
12/74	2/75	4/75
Actual	2/75	4/75

Xfer cost: CPU, cab, PWR, 64KW

Date:	Cost/Date:	
1/75	$14,372/FY'75	estimated
1/75	$12,286/FY'76	estimated
5/75	$14,357/FY'75	actual
8/75	$12,100/FY'76	actual

MM 11 DP

Product Mgr.: M. Gutman/C.McCarthy

Definition: 16K X18 core memory option used with the DD11C,D backplanes (11/04, 11/34, 11/PDQ)

Date:	Projected First Ship From Mem. Volm Mfg.	Projected FY'76 Transfer Cost
10/74 (near start of program)	10/75	$598
6/75 (2 months prior to LR)	11/75	$654
12/75 (First ship from Mem.Vol.Mfg.)	12/75	$661
Now - Final Standard & Transfer cost for FY'76		$651

11/IMP (formerly 11/PDQ, will become 11/60)

Product Mgr.: Bob Gray

Definition: High mid-range 11 family processor & package. 128K word, cache with writeable control store, μ programmed slow FPU (FPP not FIS) and optional high speed floating point (2 x 11/45). New corporate cabinet, added features for serviceability.

Date:	Announce:	FCS:	Comments:
11/74	9/75	12/75	11/OK
12/74	9/75	1/76	change to PDQ
4/75	9/75	1/76	
6/75	9/75	2/76	
9/75	5/76	6/76	
10/75	7/76	9/76	

Mfg.Cost: CPU, PWR, backplane, 16K memory*

Date:	Cost/Date:	Comments:
11/74	$2,700/6/76	11/OK Decision Model (ENG)
4/75	$2,935/7/76	Mfg/Engr Est (4 modules)
10/75	$3,210/3/77	Mfg(6 modules)Corp card cage

* no parity, bootstrap or serial interface

NOTE TWO MAJOR Changes in Strategy accompanied early product plans

PGA

TS03

Product Mgr.: Chester Ju

Definition: Low performance magtape system using TU10 controller (TMB11) and software compatible with TU10. 12½ ips, 800 bpi, 9 track using 7" reels.

Date:	Announce:	FCS:
10/74	2/75	6/75
2/75	3/75	6/75
2/76	3/75	6/75

Mfg. Cost: (Drive + controller)

Date:	Cost:	Date:	
2/75	2700	6/75	
6/75	2700	12/75	
2/76	2200	5/76	use TMB11 controller

TU16

Product Mgr.: Chester Ju

Definition: 45 ips, 10½" reel, 800/1600 bpi, vacuum column magtape system. Uses massbus controller.

Date:	Announce:	FCS:
7/73	?	2/74
3/74	7/74	8/74
12/74	7/74	8/74

Mfg.Cost:

Date:	Cost:	Date:	
2/76	3200	7/76	
2/76	3000	1/77	volume increase + new costing

RX01

Product Mgr.: P.A. Bauer

Prod. Description: Low cost, high reliability I/O and systems device. Stores 256K bytes on each of 2 drive mechanisms. Average access time 450 msec. Soft error rate $>10^9$ bits per error.

Date:	Announce:	FCS:	Cost/Date
1/15/74		12/74	$1115/6/75
3/31/74		3/75	
6/30/74	1/75	3/75	
9/30/74	1/75	4/75	
12/18/75	5/75	7/75	$1050/FY'76
3/31/75	5/75	5/75	$1050/FY'76
6/30/75	5/75	5/75	$1050/FY'76
9/30/75			$1050/FY'76
12/31/75			$1050/FY'76

RK06

Product Mgr.: Steve Orr

Definition: A 14MB capacity, top loading moving head disk with RP04/RP05 recording technology and data recovery.

Date:	Announce:	FCS:	Cost/Date:	Comments:
12/73	-	6/75	$1,000/6/76	-
3/74	-	-	-	-
6/74	-	-	-	-
9/74	-	-	-	-
12/74	4/76	4/76	$1,500/3/77	-
3/75	4/76	4/76	$1,500/3/77	-
6/75	4/76	4/76	$1,700/3/77	(1)
9/75	-	7/76	$2,512/FY'77 Avg	(2)
12/75	6/76	7/76	$2,512/FY'77 Avg	
2/76	7/76	7/76	$2,512/FY'77 Avg	(3)

Notes:

1.) Increased labor rates
Increased BOM costs
Added Purchasing burden

2.) Reduced FY'77 volume due to schedule slip
Added $200 lo-Bay cost
Added $200 contingency
Increased purchasing burden on parts
Increased BOM costs

3.) RSX-11M shipments support moves from 7/76 to 10/76

COPIER HISTORY

Product Manager: Chuck Blasi

Definition: Moist electrolytic (facsimile type) scanning printer which can copy full screen or line-at-a-time.

Date	Announcement Date	F.C.S.	Comments
6-73	9-74	10-74	
12-73	9-74	10-74	
6-74	Announced	10-74	
7-74	Announced	5-75	Eng. & Design Problem
5-75	Announced	7-75	Parts slippage
7-75	Announced	10-75	Blocking problem
12-75	Announced	12-75	1st customer ship

Cost Targets:

Date	Transfer Goal or Cost	
6-73	$100	
9-74	$150	
7-75	$300 for FY'76	$170 for FY'77
Today	$450 for FY'76	$250 for FY'77

PRODUCT DESCRIPTION: IAS

IAS Ver. 1.1
- RSX-11D V6B functionality
- 11/70 full memory
- RP04 track offset
- Terminal synchronization
- RP06 Support
- RK05F Support

IAS Version 2
- VT61 Support
- RSX-11S Generation under IAS
- RMS-11 Support
- DBMS Support
- DECNET Support
- MCR BATCH translator
- RX01 Support
- PDQ Verification

IAS Ver. 2.1
- Maintenance
- RSL

IAS Ver. 3.0
- Resource Alloe
- Multi-stream Batch
- Transaction MTR
- Job Control
- Dynamic Bod Block
- Auto config.
- File Routing
- RSL

PRODUCT DESCRIPTION: REAL TIME

RSX-11M Ver.3
RSX-11S Ver.1.1
- Ansi Magtape
- Batch
- I/O Spooling
- RK06 Support
- PDQ Verification
- Error logging documentation
- Extended files
- VT61 support
- VAS

RSX-11M Ver. 4
RSX-11S Ver. 1
- ICLS
- Batch
- I/O spooling
- WCS Support
- MP Base
- RSL

RSX-11M Ver. 4.1
RSX-11S Ver. 1.3
- Maintenance

RSX-11M Ver. 5
RSX-11S Ver. 2
- Accounting
- On-line Diag.
- Re-entrant Looking
- RSX-11S off-line utilities

RSX-11D Update
- RSX-11S Generation under RSX-11D
- RK06 Support
- RP06 Support
- RK05F Support
- VT61 Support
- PDQ Verification

PRODUCT DESCRIPTION: DCOPS 1

FEATURES

- Local front end for terminals and concentrators
- Remote concentrator/batch station
- Route through of user messages - fixed routing
- Support of character and block terminals
- Topology specified at sysgen
- IBM 3270 Emulation

HARDWARE SUPPORTED

- PDP-11/04, 05, 10, 34, ~~40, 45, 50, 55, 70~~
- DMC11 (host interface and synchronous links)
- DTE20 (host interface to DEC-20)
- DZ11 (terminals only)
- DUP11
- DV11 (synchronous only)
- DL11
- Comm IOP (for DUP11 and DZ11 only)
- Memory (16K to 128K)
- LP11
- LP20
- ~~LA180~~ LA11
- CR11

TERMINALS

- LA36, LT33, LT35
- VT50, 50H, 52, 61
- 2741
- Autobaud detection

PRODUCT DESCRIPTION: RT11

Today RT-11 V02C has the following characteristics.

- Simple to use for system programmer, but not entry-level computer user.
- Excellent response times.
- Documentation poorly organized.
- Not yet self-installing.
- Hardware is accessible to user.
- Designed for assembly-language user, but primarily used for high-level languages.
- Functionality lacking in a few key areas.
- Serving as base for several multi-user applications (REMOTE, MU BASIC, COS 350).
- Single-job monitor primarily used.
- Certain components are poorly done and are causing support problems.

RT-11 V03 (Changes from V02C)

Add compatible high-level command language; re-organize and improve documentation; add reliability and servicability features; add necessary multi-user support functionality (KT-11 support, multi-terminal support); add high-level language tools (debugger, more powerful linker); create simple SYSGEN; add network support; make single-job monitor more modular and customizable, re-engineer problem components (magtape, PIP); track new hardware support new languages as available.

RT-11 V04 (Changes from V03)

Improve error handling; add optional Q and A interface; improve network support; improve single-job monitor modularity and reliability; re-engineer problem components; improve documents, add new documents for more novice user; add compile-load-and-go option to FORTRAN ; support new languages as available (e.g., small-11 COBOL); track new hardware.

RT-11 V05 (Changes from RT-11 V04)

Improve documentation; add CAI self-instructing option; improve reliability by re-engineering problem components; make system self-supporting; track new hardware.

Note that a key element of this strategy is the constant re-engineering of components to improve their usability, reliability, and human engineering.

PRODUCT DESCRIPTION: DCOPS 2

FEATURES

- All release 1 features; plus:
- SNA interface (probably 3767 emulation)
- SNA interface (probably 3790 emulation) (12/77)
- Increased use of Comm IOP for greater capacity
- User-written application tasks
- Static adaptive routing
- Dynamic re-configuration of topology
- Added RAS features
- RMS-11 support

HARDWARE SUPPORTED

- PDP-11/03
- DLV-11
- DZ11-V
- DUP11-A (LSI-11 sync interface)
- DU11
- DQ11
- DH11
- Comm IOP (additional functions and devices)
- Memory (16K to 1,024K)

LATER RELEASE FEATURES

- Enhanced dynamic topology
- DBMS support
- Adaptive routing
- Disk queueing
- Terminal to terminal message switching
- Network manager console
- Network security officer console

MS got my copy + attach for me to discuss with KAT

digital INTEROFFICE MEMORANDUM

TO: Gordon Bell

DATE: January 14, 1974

FROM: Nathan Teichholtz

DEPT: Engineering

EXT: 2533 LOC: 12-1

SUBJ: DEC's Goals

+ Products must
- x2 also cat. prof. peri
- add cable, not in
any others

1. Do straight (arithmetic) as multiply

2. Be who proposes does!

JAN 14 1974

It's high time that we had an objective statement of goals, as in your January 4 memo. While I have a few concerns about the goals stated in your memo, my major concern is that we have an even greater need for a statement of market goals, as opposed to product goals. For planning purposes, both types of goals are needed. Is someone in Ted's group addressing this problem?

General goals are useful during the early stages of product development in that the engineers doing design work all have the same basis for making trade-offs not constrained by product-specific goals. I'm not sure that your far-reaching statement on software goals is useful in this context; it sounds to me like an "all good things, no bad things" statement. In particular:

Preliminary design - earlier

0. Why is "state of the art" software necessarily good? Historically, it has taken us several hardware generations to make our software as good as we'd like it (i.e., the PDP-10 experience).

1. Should our software use fewer hardware resources than our competitors'? Who are our competitors -- IBM or DG? How do we resolve the proper level of software resources to provide, given that each software resource "costs" some hardware? This is where the "marketing goals" would be useful.

Relative to some of the other points you raise in your memo:

2. Your comment about competitive products under the $200K system price excludes the -10. I don't see why the goals stated shouldn't apply to that product as well as the mini's.

3. In order to understand the competitive position of our products, I think we must look not only at the "instantaneous" state of our competition, but also at the long term trends for price and performance for similar products. All too often, we come out with "yesterday's

products tomorrow"; part of this phenomenon is due to our failure to allow for our competitors' development activities occurring in parallel with our own.

/ale

JAN 1 [illegible]

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FROM: GORDON BELL

fndm

FEB 07 1974

~~Here is a draft of goals I'd like to propose. Please comment regarding vagueness, additions, etc.~~

DEC'S PRODUCT GOALS

fm. Bell

The computer is the most significant invention for humankind. Its eventual effect will allow a nearly pollution free environ-

so far the computer (your memos) and the copying machine (my memos) have done more to pollute rivers than they have done to reduce pollution by their secondary effects. (at least your memo's are recyclable).

ment, by permitting information to be stored in reusable forms with very small utilization of energy, and ultimately allow transactions to occur by moving information rather than people or information media (a large amount of personnel and paper movement will be essentially eliminated). Also by using algorithms, it can efficiently encode information for transmission--thus saving time, memory, and information transmission links. Our business is fundamentally to supply state-of-the-art, highly competitive, computer systems which can be used widely. It is important that the machines (computers) be widely understood within the corporation together with their use and limitation.

General Product Goals

Provide highly competitive, state-of-the-art products in the system price range below $200K, that permit us to be the leader in selected markets. Most generally, our systems provide capabilities (peripherals and programs) to permit the machines to be used either directly by people or by other machine-readable processes. We should avoid promulgating systems which use cards and paper; both are ecologically poor, decouple the user, and introduce long delays and error-prone steps. Thus, both low cost, real time, and stand alone interactive systems are needed, together with higher capability shared systems for multiprogrammed real time and interactive use. That is, both ends of the spectrum accomplish same ends: low cost stand alone; and low cost by sharing.

The emphasis on products for the OEM automatically permits internal product line users to also be leaders. Basically, this LEADERSHIP should have the following goals:

1. Raw iron basic CPU's, primary memories, and CPU options. All ranges of price (and corresponding performance).

2. Peripherals which we manufacture. Our peripherals should be competitive enough to be used on all mainframes (including competitors) in our market. They should be OEMable, and DEC should not be considered a captive market for them.

3. Systems which are a combination of 1 and 2, and 4

4. Software (unbundled) which makes systems fundamentally that are characteristics of a leader. That is, the software should be substantially state of the art, using less hardware resources than competitor systems, while doing a better job with the resources they manage. We must use the fact that we have a wide, dynamic price range of products, and have an integrated family of programs that can be used substantially across this range with only minor attention to re-programming.

It would be a better goal to make them more easily maintained, modified; more fail safe; more human engineered,

Specific Shorter Term Product Goals

1. SOFTWARE STANDARDS AND COMPATIBILITY. Move toward hardware and software systems that are upward and downward compatible with one another through user languages, command languages, files, communications, and other information media. (This permits user mobility across systems, ease of understanding, less ambiguity in definition at all levels, and the basis of intermachine communication. Finally, future machine designs are less constrained.)

2. HIGH LEVEL LANGUAGES. The leading edge users OEM appear to have programming needs similar to our own systems programming. We must have an aggressive plan to move to better interpretation of higher level languages.

3. BETTER UTILIZATION OF SOCIETIES RESOURCES. In accordance with the general corporate philosophy, we should design products which are relatively pollution free. Such designs may take several forms: less parts, greater electrical efficiency, capability to turn off the component by the system when not in use, and lower acoustical noise levels.

I think the primary goal is still cost or cost performance.

4. KNOWLEDGE OF THE PRODUCT AND LEADERSHIP. Foremost, we must be realistic and understand the products we design in terms of their competitive position--ie., we must first be honest with ourselves. This understanding takes the form of knowing price, cost, yield, reliability, and all the relevant user performance specifications. In this way, we can access our technological position, and move through future developments to be in a leadership position!

5. SMALLER NUMBERS OF HIGHER QUALITY DESIGNS. Through larger size and higher production volumes, our engineering, particularly with respect to producibility, must constantly improve. Fundamentally, the best improvements will come about through doing fewer things, better. Three basic attacks will be used:

   a. Evolutionary products - better evolve standard products, particularly shared use of packages, power supplies, consoles, busses (and common peripherals), and cabinet hardware in order to get effectively lower prices through higher volumes.

   b. Revolutionary products and processes - we should attempt to move toward products and processes which provide significant (at least factor of 2) improvement over status quo.

not steepness!

must invest in mfg equipment

must do better engr.

c. Common processes - there must be increased emphasis in the process area with full automation an ultimate, although perhaps idealized, goal for module production, test, and burn-in.

This automation also includes the goal of fully automatic FA&T--where a centralized machine is managing the checkout and reporting.

PROFESSIONAL ENVIRONMENT PHILOSOPHY AND GOALS

People and Their Learning

The basis of the goods and services DEC sells is its people. It is necessary for the DEC personnel to understand computer science and be abreast of the rapidly evolving technology, engineering, and utilization of machines. Clearly our people must constantly learn through formal university level training (which we will encourage in various ways), formal classes (including those where individuals can progress to different skill levels), informal personal learning, sabbaticals, and any other formal or informal programs that may develop. Because of the very diversity of learning environments and opportunities, it is important that DEC should not endorse any particular one. The burden on personal technical development, however, must rest with the individuals and their managers; and people must have the skills to produce worthwhile goods and services.

Computer Engineering and Computer Science

Computer Engineering is the dominant discipline for machine design. It is used with other engineering and professional disciplines. Computer Science also contributes, and has been defined as the study of computers and includes virtually all of the phenomena surrounding computers--their structure, behavior, and evolution, as well as their fundamental and evolving uses. Computer Science now comprises machines, languages, operating systems, and basic algorithm used over a broad range of user problems. Thus, it is also close to mathematics, and other engineering disciplines, and to society. Although most of us are not computer scientists, but rather engineers (of varying basic disciplines) and other professionals, Computer Science is important to us. Our own research group is fundamentally applied, identifying the emerging concepts which will be important in near term future machines, and seeing that we have the understanding to apply the principles when they mature. The other role of our research is to provide deep consultation on products, and to insist that products use appropriate techniques which will keep them at the state of the art and be correct.

Rewards

Engineers will be measured against the plans (goals) they establish. It is management's responsibility to establish these goals. It is the responsibility of all engineering management to insist that rewards are on the basis of the goals and the goal levels.

Technical, Business, and Managerial Tracts — See IBM's salary mechanism!

We will provide an environment where the outstanding engineer, who has contributed to products or process, is rewarded on the basis of professional achievement and not on the number of people he manages. Such an engineer must maintain high professional standards and achievements. DEC will provide an environment for the engineer desirous of management responsibility to achieve it. In fact, since we are a rapidly evolving industry, DEC will endeavor to encourage capable engineers to learn formal management skills so that it can be a highly trained company in terms of both products and management.

Patents

The primary output of the company is its goods and services. Patents are often a useful way to increase a product's life and protect it from immediate (undue) competition. It is the responsibility of the engineer to bring useful patentable ideas to the corporation's attention for these purposes. Also, new ideas in other areas of DEC are openly solicited.

Publications

Publications about products (and techniques used with products) can prove useful to the acceptance of a product by the community of users. DEC encourages professoinals to write articles and give seminars as a method of interacting with professional communities, formulating and consolidating ideas, promoting products, etc. However, since the publications are not our main product, an individual and his manager must decide whether a publication is worthwhile.

The publication of articles requires significant time. When an individual takes on the writing of an article in his (and the company's) name, it should be done so with the same considerations as any other project. Professionals from the Public Relations department can be contacted to help in the formulation and checking of articles, but they should not be considered as ghost writers. Authorship of articles is normally on the basis of those who do the work contributing to the product or idea--as such, it is a form where the writer achieves recognition outside of the company environment. AMEN!

Physical Environment

The engineer must be provided with an environment which is conducive to work, and relatively hassle-free in terms of accomplishing his task. Hassling should be confined to product definition and product design review. Once a project is in progress, all groups, who have agreed to provide support, must do so in accordance with the agreement. Similarly, projects must define their service needs well in advance of the need.

GB:mjk

we've got to get more explicit on how we decide to do one project vs. some other.

B.

DATE 01-04-74 DISTRIBUTION WRITER PAGE 0001

To: Gordon Bell, Dave Peters, Dick Clayton, Bob Puffer, Bruce Delagi
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Heron file notes from G. Bell

JAN 28 1974

FROM: GORDON BELL

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DEC'S PRODUCT GOALS

The computer is the ~~most~~ a significant invention for humankind. Its eventual effect will allow a nearly pollution free environ-

Not clear -

In fact the computer like the printing press and the XEROX machine increases man's propensity to publish. Hope fully the information published will be better interpreted because the reader will have access to computerized models to aid in his reading of new data.

A problem is that the computer tends to ~~drop~~ build a wider gap between the high and low IQ members of our society. Never before has man had such a powerful tool for controling the ~~masses~~ population. I believe that the computer may be a significant a factor for destruction or construction as fission.

ment, by permitting information to be stored in reusable forms with very small utilization of energy, and ultimately allow transactions to occur by moving information rather than people or information media (a large amount of personnel and paper movement will be essentially eliminated). Also by using algorithms, it can efficiently encode information for transmission--thus saving time, memory, and information transmission links. Our business is fundamentally to supply state-of-the-art, highly competitive, computer systems which can be used widely. It is important that the machines (computers) be widely understood within the corporation together with their use and limitation.

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I resent being called a machine readable process.

Why do computer people insist on separating hardware and software when they talk about Sales?

Why is this the rule? Why can't a product line sell a product?

Poorly worded

Is this good?

I propose that internal product lines be permitted to purchase processors as well as peripherals from outside of Digital. The only rule is that prior to each outside purchase the product line must present their reasons before the Operations Committee or their designate.

Specific Shorter Term Product Goals

1. SOFTWARE STANDARDS AND COMPATIBILITY. Move toward hardware and software systems that are upward and downward compatible with one another through user languages, command languages, files, communications, and other information media. (This permits user mobility across systems, ease of understanding, less ambiguity in definition at all levels, and the basis of intermachine communication. Finally, future machine designs are less constrained.)

This = Implimentation dependent

2. HIGH LEVEL LANGUAGES. The leading edge users OEM appear to have programming needs similar to our own systems programming. We must have an aggressive plan to move to better interpretation of higher level languages.

3. BETTER UTILIZATION OF SOCIETIES RESOURCES. In accordance with the general corporate philosophy, we should design products which are relatively pollution free. Such designs may take several forms: less parts, greater electrical efficiency, capability to turn off the component by the system when not in use, and lower acoustical noise levels.

Presumably if we are competitive we shall build machines which optomize whatever society currently wants to optomize. This year it is energy not pollution. Next year it will be light and paper so we'll build printers which spit out braille on granite.

4. KNOWLEDGE OF THE PRODUCT AND LEADERSHIP. Foremost, we must be realistic and understand the products we design in terms of their competitive position--ie., we must first be honest with ourselves. This understanding takes the form of knowing price, cost, yield, reliability, and all the relevant user performance specifications. In this way, we can access our technological position, and move through future developments to be in a leadership position!

Yea !

5. SMALLER NUMBERS OF HIGHER QUALITY DESIGNS. Through larger size and higher production volumes, our engineering, particularly with respect to producibility, must constantly improve. Fundamentally, the best improvements will come about through doing fewer things, better. Three basic attacks will be used:

   a. Evolutionary products - better evolve standard products, particularly shared use of packages, power supplies, consoles, busses (and common periherals), and cabinet hardware in order to get effectively lower prices through higher volumes.

   b. Revolutionary products and processes - we should attempt to move toward products and processes which provide significant (at least factor of 2) improvement over status quo.

c. Common processes - there must be increased emphasis in the process area with full automation an ultimate, although perhaps idealized, goal for module production, test, and burn-in.

This automation also includes the goal of fully automatic FACT--where a centralized machine is managing the checkout and reporting.

PROFESSIONAL ENVIRONMENT PHILOSOPHY AND GOALS

We should do as much R&D in the areas of management and people development as we do in software or hardware. People are our most important asset and we treat them as if they exist only for the company whereas in truth the company exists only because of the people.

People and Their Learning

The basis of the goods and services DEC sells is its people. It is necessary for the DEC personnel to understand computer science and be abreast of the rapidly evolving technology, engineering, and utilization of machines. Clearly our people must constantly learn through formal university level training (which we will encourage in various ways), formal classes (including those where individuals can progress to different skill levels), informal personal learning, sabbaticals, and any other formal or informal programs that may develop. Because of the very diversity of learning environments and opportunities, it is important that DEC should not endorse any particular one. The burden on personal technical development, however, must rest with the individuals and their managers; and people must have the skills to produce worthwhile goods and services.

Computer Engineering and Computer Science

Computer Engineering is the dominant discipline for machine design. It is used with other engineering and professional disciplines. Computer Science also contributes, and has been defined as the study of computers and includes virtually all of the phenomena surrounding computers--their structure, behavior, and evolution, as well as their fundamental and evolving uses. Computer Science now comprises machines, languages, operating systems, and basic algorithm used over a broad range of user problems. Thus, it is also close to mathematics, and other engineering disciplines, and to society. Although most of us are not computer scientists, but rather engineers (of varying basic disciplines) and other professionals, Computer Science is important to us. Our own research group is fundamentally applied, identifying the emerging concepts which will be important in near term future machines, and seeing that we have the understanding to apply the principles when they mature. The other role of our research is to provide deep consultation on products, and to insist that products use appropriate techniques which will keep them at the state of the art and be correct.

Rewards

Engineers will be measured against the plans (goals) they establish. It is management's responsibility to establish these goals. It is the responsibility of all engineering management to insist that rewards are on the basis of the goals and the goal levels.

Technical, Business, and Managerial Tracts

Yes!!

We will provide an environment where the outstanding engineer, who has contributed to products or process, is rewarded on the basis of professional achievement and not on the number of people he manages. Such an engineer must maintain high professional standards and achievements. DEC will provide an environment for the engineer desirous of management responsibility to achieve it. In fact, since we are a rapidly evolving industry, DEC will endeavor to encourage capable engineers to learn formal management skills so that it can be a highly trained company in terms of both products and management.

Patents

The primary output of the company is its goods and services. Patents are often a useful way to increase a product's life and protect it from immediate (undue) competition. It is the responsibility of the engineer to bring useful patentable ideas to the corporation's attention for these purposes. Also, new ideas in other areas of DEC are openly solicited.

Publications

Publications about products (and techniques used with products) can prove useful to the acceptance of a product by the community of users. DEC encourages professionals to write articles and give seminars as a method of interacting with professional communities, formulating and consolidating ideas, promoting products, etc. However, since the publications are not our main product, an individual and his manager must decide whether a publication is worthwhile.

The publication of articles requires significant time. When an individual takes on the writing of an article in his (and the company's) name, it should be done so with the same considerations as any other project. Professionals from the Public Relations department can be contacted to help in the formulation and checking of articles, but they should not be considered as ghost writers. Authorship of articles is normally on the basis of those who do the work contributing to the product or idea--as such, it is a form where the writer achieves recognition outside of the company environment.

I believe that we are approaching the size where we should think about a company organized, refereed, journal similar to the RCA review, IBM Systems Journal, ETC.

Physical Environment

The engineer must be provided with an environment which is conducive to work, and relatively hassle-free in terms of accomplishing his task. Hassling should be confined to product definition and product design review. Once a project is in progress, all groups, who have agreed to provide support, must do so in accordance with the agreement. Similarly, projects must define their service needs well in advance of the need.

GB:mjk

We need to develop a system whereby low level managers and supervisors can make significant decisions and relate the ~~effd~~ effects of their decisions to the company's Objectives. At first glance I am very much in favor of the Texas Instrument Objectives, Strategies, and Tactics System. This system combines the best parts of small and large corporations to produce a very dynamic atmosphere where people can ~~are~~ be important.

Budgeting Process

FEB 14 1974

DATE 12-17-73 DISTRIBUTION WRITER PAGE 0001

PLEASESEND TO: JULIUS MARCUS PK3-1

COPY: AL BERTOCCHI, WIN HINDLE, PETE KAUFMANN, KEN OLSEN, DICK CLAYTON, IRWIN JACOBS, BOB LANE, BILL LONG, LARRY PORTNER, BRAD VACHON, BRUCE DELAGI, BOB LANDER, NAT TEICHHOLTZ, JOHN FISHER, TED JOHNSON, ANDY KNOWLES, STAN OLSEN, BILL HOGAN, ED KRAMER, JOHN LENG, GERRY MOORE, JACK SHIELDS, BILL THOMPSON, BOB PUFFER, PHIL LAUT, GORDON BELL

cc Ron Rogers PYE

FEB 19 1974

FROM: GORDON BELL

SUBJ: BUDGETING SCHEMES (PROCESS) FOR ENGINEERING (PRODUCTS)-- STATUS

Possible allocation schemes (and variants):

1. Status quo--whatever that was. Does anyone know since Bill Thompson's getting out of loop?

2. Have Operations Committee allocate funds into gross categories? Allocate within these categories on a product group-by-group basis. Here, I'd like to staff this to provide direction based on analysis.

FEB 19 1974

I generally agree with your presentation and central goal of having volume more firmly committed before a project is started. Lets work toward that goal, but lets not change our ways too fast or will take too long to make up our minds (i.e., be over advised). As the P.C.'s understand they must put more staff, skill and judgment into central eng. inputs, we can go forward in the direction you propose. Mod

3. Get rid of the development part of the 2% money. Make this truly shared like shared funding, and then allocate in detail on the basis of purchase orders from the various product lines.

4. Hassle everyone by getting all PLM's to agree to all products. An extension of last year's hassle which Dick Clayton presided over.

5. Put all funds into 2%--figure out how to allocate them.

6. Move to a 2-tier corporate structure with products managers responsible for producing products to a given cost at a volume they have sold to product line (Market Product Line) managers. The financial incentive would be appropriately placed on the product group to get purchase orders--not promises.

I'm seeing a plethora of projects and products, and lots of directions with respect to products. All of these are substantially beyond our budget, and I can't believe the PL's are going to sell all of this stuff that they think is now so great and important.

For example, I (memory group) am trying to go out of control (ie., spending beyond current budget level on the basis of the product direction I got from the Memory Wood's Meeting). Until I did the planning, it wasn't obvious that we were so really far behind in the development of memories--which accounts for 30% of revenue with about 2% of resources. Now we are having to really fund a second memory group, as MOS may become viable as the main memory. Also, we have to get there with respect to better packaging.

As I see it, there is a hodge-podge method of funding (outside PL control and responsibility):

1. 2% supposedly shared across all PL's--but we try to fairly allocate on basis of VOR (eg., small versus large).

2. 2% for misc.--research, DECUS, standards (within PL control). Also, engineering tools are done here (design aids).

3. 11-shared. PL's get together and decide on all the projects and how they are to be allocated across PL's.

4. Constortium--2 or more PL's decide on a product.

5. Only a single PL. (Work done by central group or PL group).

6. Overhead in engineering group. Programming develops its

tools in this fashion.

7. Manufacturing. Design product by trying to build it. Some test equipment design and diagnostics are done here.

8. Field Service. Similar to manufacturing.

The fiscal 74 shared-11 budgeting was presided over by Dick Clayton. Although I look at this as being the supreme sacrifice to Digital, Bill Long and Ed Kramer suspect self-preservation on Dick's part. At any rate, if the budgeting method continues in the present style, Bill Long has agreed to do FY75 to insure some low end products.

For some of the central 2% money, Bob Puffer, Bill Thompson and I figured out the total last year, and then gave me the dregs for memory. Bob Savell did an admirable job scrounging money from all the product line managers to get a memory development program together, but at the last minute Eduman pulled out his $2000 from the consortium, and we had to cancel many projects.

Here, memory has been ineffective in "selling" projects. I believe we have to reformulate the process in order to carry it out and make some reasonable decisions. Fundamentally, the pie is too big to work in a single group, with all the competing consumers and producers. Also, there is a gross inconsistency in the use of 2% funds: development, shared, research, tools, UECUS. Systems and peripherals are done in an asynchronous fashion. Certainly the development part of 2% should be handled exactly like all the rest of the shared development--although that mechanism isn't good enough.

There are a very large number of conflicts for funds:

1. We need substantially more money to do the dual development of both MOS and core memories in the event MOS becomes viable in 2 years.

2. There is a possibility of developing 4 products in the tape area. (The growth and use probably won't support it), but the one drive we do manufacture in house has to be chosen carefully to get good utilization across a good number of the PL's--and be as profitable.

3. The mean time between plan changes in the disk area is about 4 months; we have gone from RP04, RP05, RK05L to an RP04 (2 of them), RK06, and RX01 to finally the preceeding out with an RK05LL. There is still another disk that will be forthcoming. (Each time, some new cost/technology/idea input causes a change.) The current budget (need) is significantly greater than before, and we barely currently

have no real way of affecting change.

4. There is a task force looking at a very low end system. The product range is increasing. They too will need money.

5. We have projects come up that were buyouts, that we now want to manufacture. These strain the existing budget--and in effect are simply cost reduction programs for components.

6. There is a strain on engineering due to high volume.
7. The LSI funding, direction, effort is a near disaster. There is no funding for this. Each day I get about 2 requests to find out what we're doing. It's easy to say-- NOTHING! The little money for it gets dribbled away.

SUMMARY

Budgeting (and resources allocation) is constantly with us. We must tune up the mechanism again to work to a more effective budgeting scheme. The pressures for changes are severe in new core, MOS, disk, and tape memories, LSI technology, several other peripherals, cpu's, etc. I'm really distressed that we do not measure or estimate the return before these projects get started. Once budgeted, we rarely stop a project (although one occasionally does get deflected to something good).

GB:mjk

digital INTEROFFICE MEMORANDUM

TO: John Fisher

DATE: January 31, 1974

FROM: Phil Laut

DEPT: Engineering

EXT : 4308

SUBJ: ALGORITHMS TO AID IN MAKING ENGINEERING BUDGETS

This is a description of the possible algorithms that could be used to aid in defining engineering budgets. The basic idea is to look at the amount of money produced by the various products now being sold, and as a first approximation reinvest a portion of that money into similar kinds of products.

CAVEATS

This process provides first approximation only. This process only tells us where to spend the money to continue today's business and therefore some money must be set aside to finance development of the kinds of products that don't produce any income today because we don't have them.

ALGORITHMS

There are really two issues in developing budgeting algorithms--the base and the rate.

The base refers to defining what money is generated from existing products, and the rate refers to what portion of that money we are willing to reinvest.

Alternatives for Defining the Base

		Pros	Cons
1.	Gross Equipment Sales	Simplest	Does not consider manufacturing cost.
2.	Net Operating Revenue	More realistic than 1, in that it considers varying discount level.	More complicated than 1, and does not provide very different answers.
3.	Manufacturing Cost	Much of the engineering effort is related to reducing manufacturing cost, so there is an argument that we ought to spend the most where it costs the most.	No consideration of pricing.
4.	Gross Margin (Gross sales less direct manufacturing cost)	Realistic in that this provides the most accurate measure available of the amount of money generated by a class of products.	Somewhat complicated.

My vote would go for #4 even considering the complexity, because my guess is that we are a year away from automating product (as opposed to product line) accounting which makes it impossible to update any algorithm more often than quarterly. Given a quarterly update, a little more complexity does not cost much.

Alternatives for defining the rate

The primary issue surrounding the rate is whether it is fixed or variable across products. If the gross margin is used to define the base, then I would favor a fixed rate across products.

Although engineering per sales dollar may be inherently bigger in high end products, using gross margin to determine the base would help us ensure that high end products are priced to recover engineering costs.

PL:mjk

1	2	3	4	5	6
PATH	STEPS ON THE PATH	WHAT IS NEEDED TO PROCEED TO NEXT PATH	WHO TO SELL TO PROCEED TO NEXT PATH	COMMITMENTS THAT RESULT FROM APPROVAL TO GO TO NEXT PATH	S T A N D A R D S
Start	Get inputs and data from wherever needed and write them down	Written concept.	Your boss. Products Committee acts as appeal board.	To continue with proposal and business plan Sometimes a small amount of development dollars	No prescribed format for written concept
Preliminary Design	Feasibility design Product definition Market research Understand alternatives and choose one.	Proposal and Business Plan. Two X two method.	Products Committee. Product Line Managers Committee. (Info.copy) Operations Committee has veto power.	Most of development dollars	STD proposal and Business Plan
Design	Implementation of alternative selected in business plan	Operating engineering prototype	If product is approximately equal to proposal then Manufacturing/Engineering Committee; if not then Products Committee w/updated proposal.	Production build up dollars, tooling *	
Pilot Production	Clean up prints, order limited number parts, define assembly and test procedures.	Business Plan	Product Line Managers Committee	Inventory dollars *	STD Business Plan Same as above but updated.
Product Test	Test (in-house and field) of pilot production units major inventory buildup	Volume production	Manufacturing/Engineering committee or manager via user reports.	Sales and field service expenses	
Support volume	Production support	Phase out plan - considering customers (especially OEM's) who may require product	Product Line Managers Committee	Withdraw product	

NEEDED TO ANNOUNCE A PRODUCT: (This is shown separate from the development path because the timing of announcements is often market related.)

1. Operating Prototype
2. Cost estimate by Cost Accounting
3. Manufacturing plan
4. Software plan
5. Updated business plan
6. Configuration plan
7. Approval of Product Line Managers Committee
8. Approval of Operations Committee (Non-waiverable)

* Analog for Software Projects

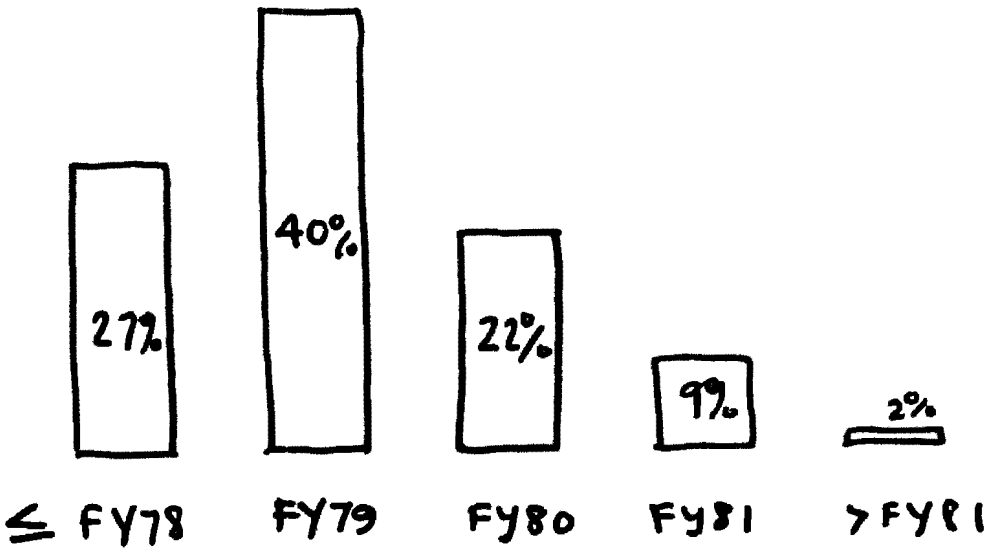
add software piece: also Std. Bus. Plan

DEC ENGINEERING - MAY '78

cgB

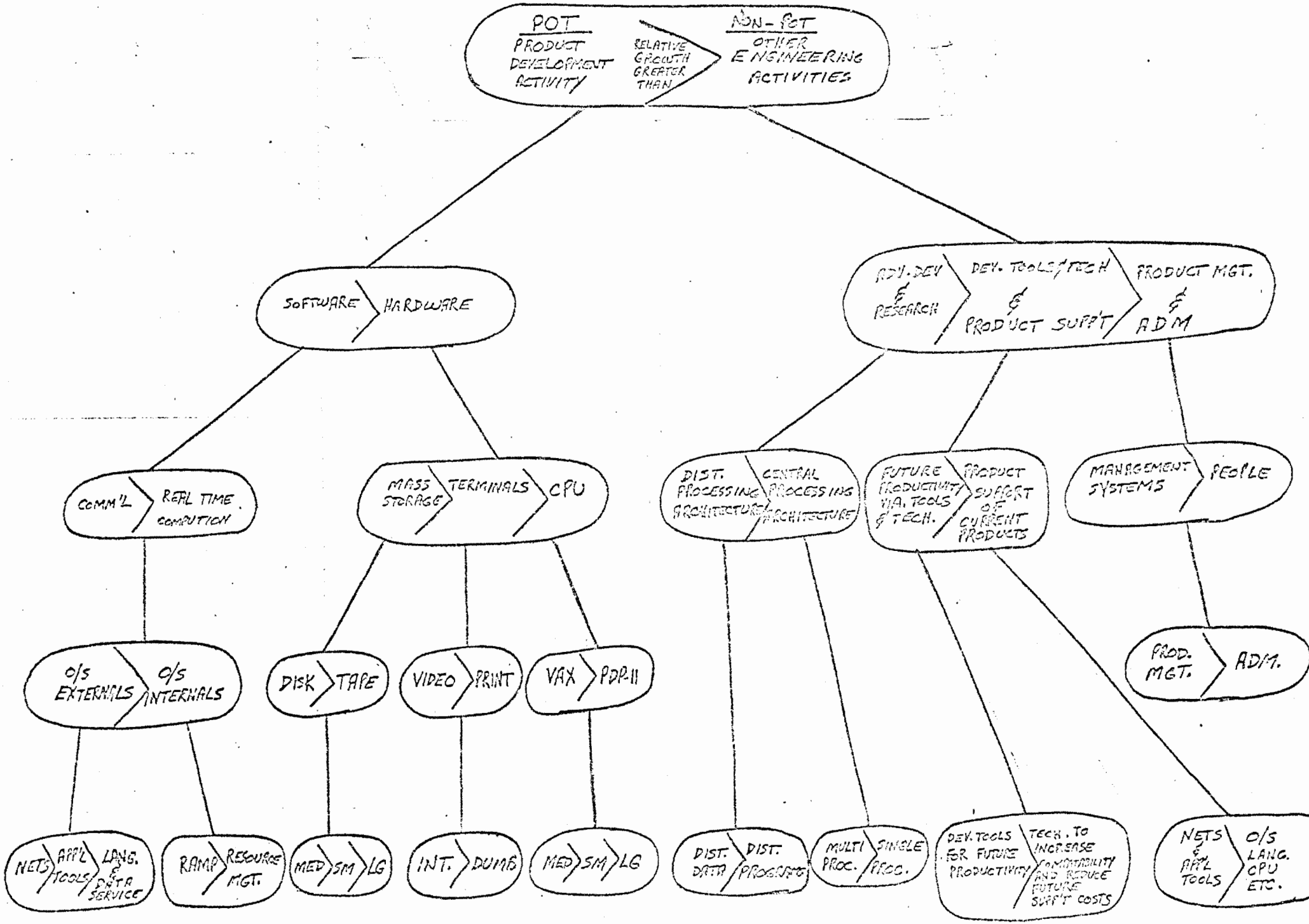
- OPERATIONS
  (PEOPLE, PLACES, $, ENG. SUPPORT)
- R & ADV. DEV.
- MFG. ENG. & LSI; MEMORIES
- MASS STORAGE
- TERMINALS & SMALL SYSTEMS; PKG. & PWR; SYSTEM'S ENG.
- 11 & VAX-11 BASE SYSTEMS
- 10/20 BASE SYSTEMS
- SOFTWARE
  - TECH. BASE & ARCH.
  - NETWORKS
  - REAL TIME & COMPUTATION
  - COMMERCIAL

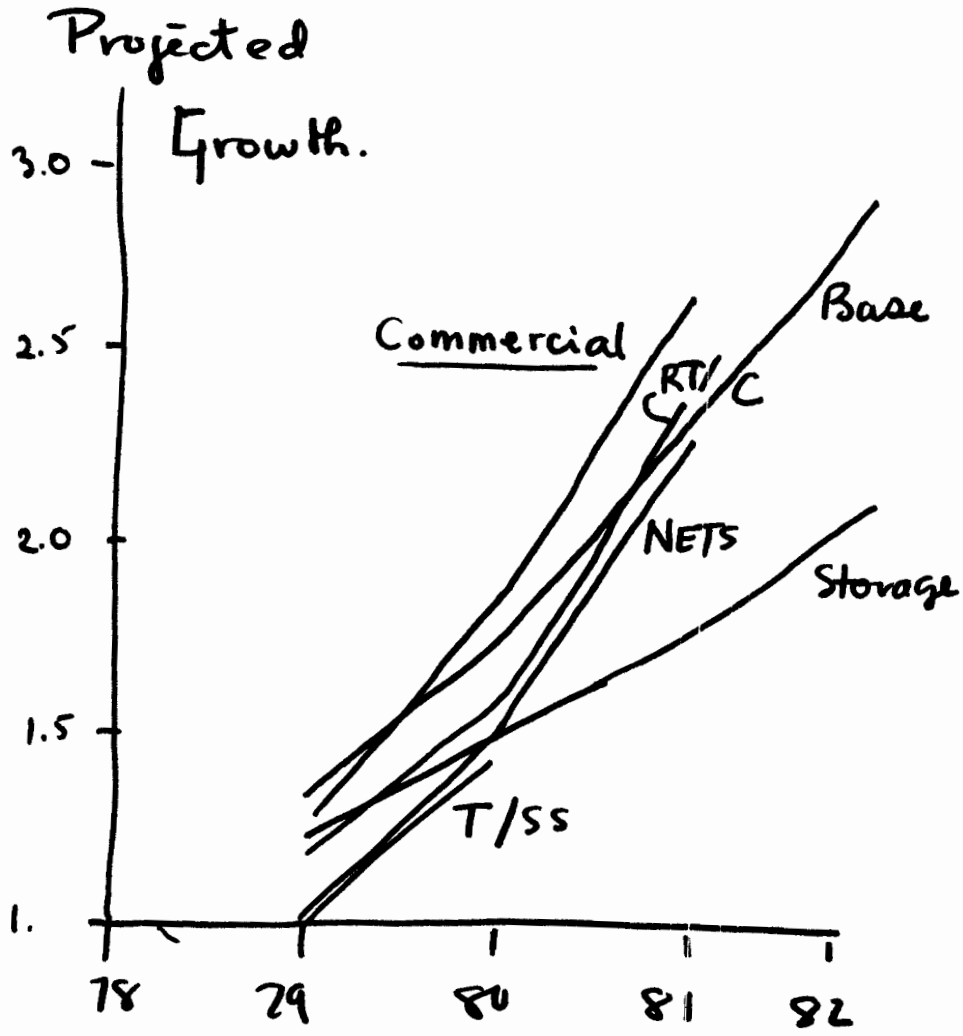
Engineering
Spending
Product Ship Date



APPENDIX I

INTUITIVE REASONING USED WHILE DEVELOPING THE FUNDING TARGETS SHOWN IN APPENDIX I




Projected
Growth.
3.0
2.5
2.0
1.5
1.
Commercial
RT/C
Base
NETS
Storage
T/SS
78
79
80
81
82

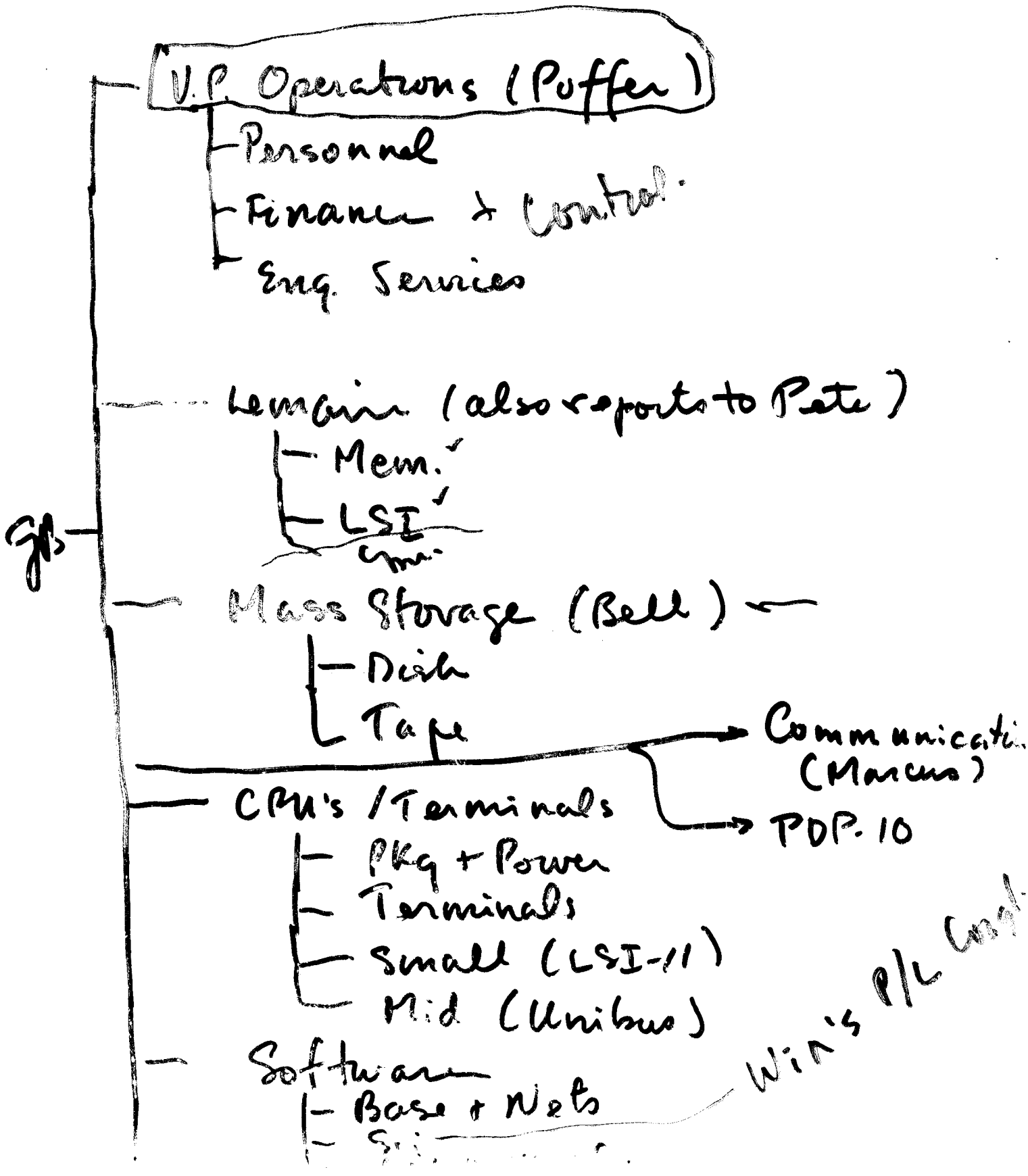
What do you think of the people and place as a place to work?

~~Is work an~~

- How does DEC differ from ~~what~~ your expectations?

- How would you change DEC to be a better place to work?

- Do you intend to work here after graduation?


V.P. Operations (Puffer)
Personnel
Finance & Control
Eng. Services
Memories (also reports to Pete)
Mem.
LSI
Mass Storage (Bell)
Disk
Tape
Communicati...
(Marcus)
PDP-10
CPU's / Terminals
Pkg + Power
Terminals
Small (LSI-11)
Mid (Unibus)
Software
Base + Nets
Win's P/L Cont...

Eng. (GBell)

VP Operations (Puffer)

- Personnel
- PLANNING (+ Processes)
- Finance + Control (PECUNIARY)
- SPACE (PLACE)
- Eng. Services + Comptation (Processes, Processing)

-- Semiconductor / Memory Mfg. + Eng (Lemaire)

- Semiconductors
- Memories

— Mass Storage

- Disks
- Tapes

— CPU's + Terminals (Clayton)

- PKg + Power
- Terminals
- Small Systems (≤ Q bus)
- Mid (Unibus)
- Systems Test / ARCH.

—— COMMUNICATIONS I/O (MARCUS)

------ PDP-10 Eng.

—— SOFTWARE (PORTNER)

- BASE — SVCS + SDC
- NETS
- SCIENTIFIC / RT / COMPUTATION
- COMMERCIAL

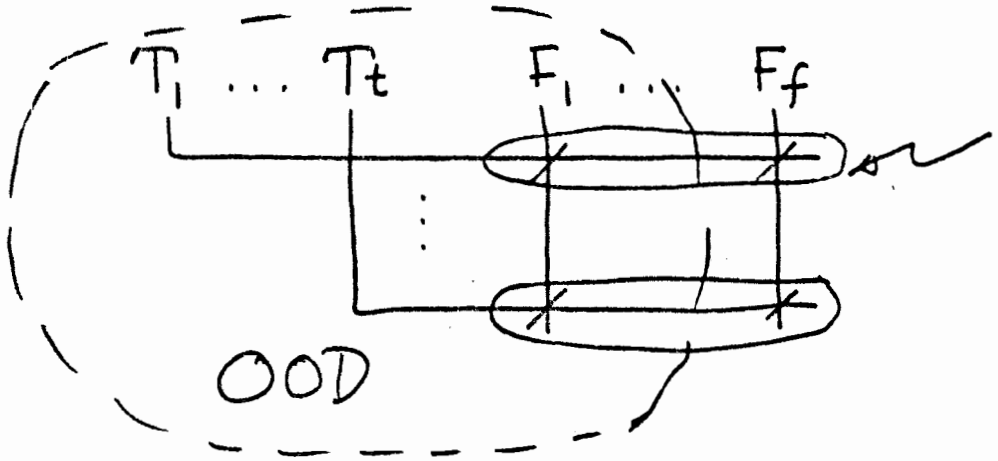
(R+D)

GB
8/10/77

How Are We Organized?

gis May 9, 197

- Functionally by skills (eg. drafting) and by technology (eg. disk mem.) with Matrix Mgmt. via Technology using Skills



How do we Measure Output?

- Mostly by "Success" of product ≃ NOR!
  - Schedule
  - $. develop and $. cost
  - Performance of Product (eg. reliability, function, ... ,
  - Rarely as/ agreement.
  -
- Gut feel
  - Truly useful • Does it feel good? (Weak link)
  - Adds evaluation dimension
  - Doesn't lose Sales for Other Systems.

Ideas Source / Constraints

≈ f(level-of-integration)

Pull
- Users ≈ Developers
- Standards ≈ Users

SW.
- Developers ≈ Users

Hdw.
- Mfg. Process Constrained

Push
- Basic Semiconductors / Magnetics

Internal / external competition

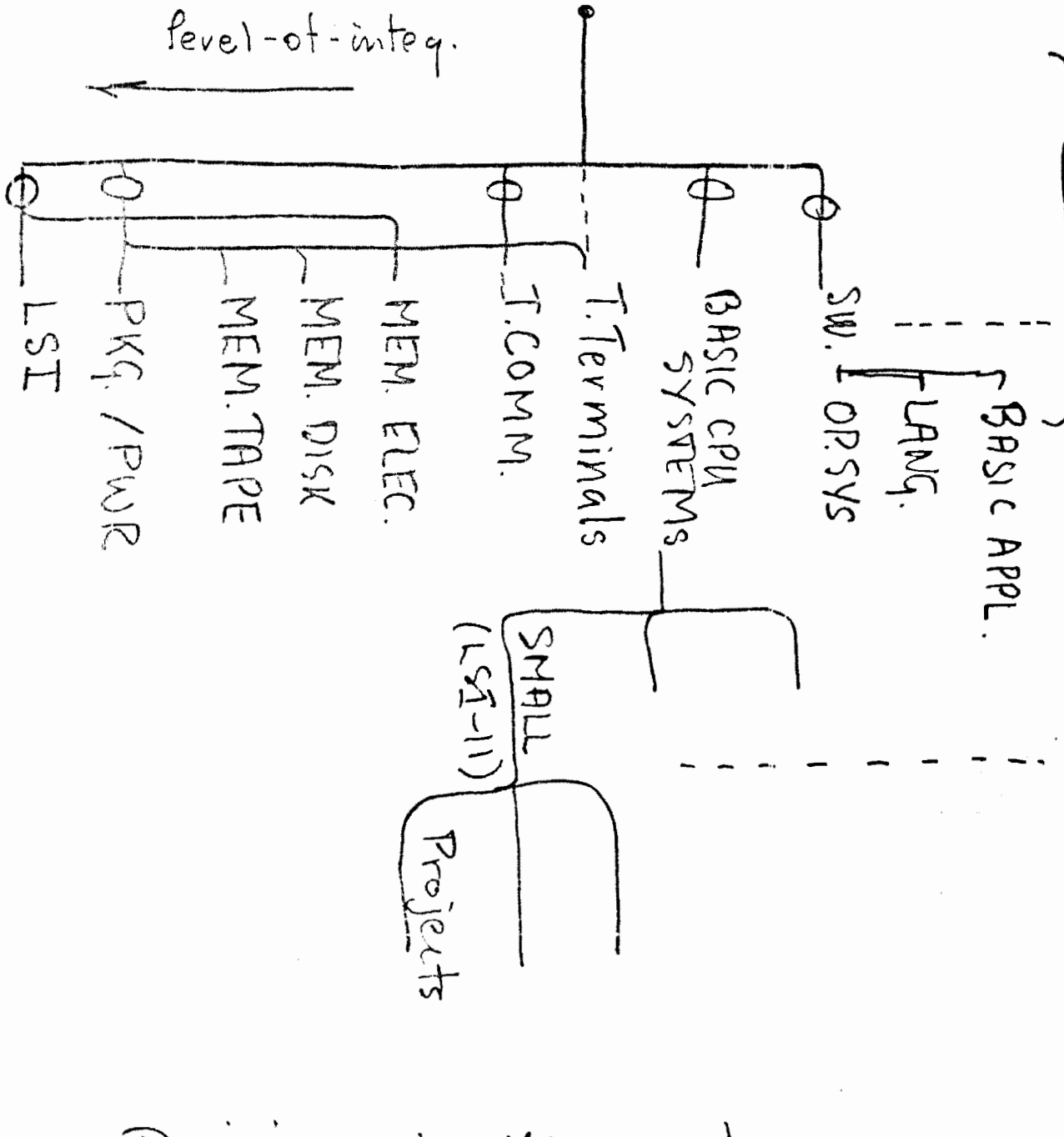
Virtual R & D

Make / Buy Advocates

"Standard" Development

Can I Understand / Use it?

Not be a pioneer.



Proposer / Decide
(Producer) (Consum
OOD → MC+P/L
- Allocation of Product
by: SIZE / technology
time (5) / Tools
→ [Rev. by Products Comm.]

Technology Group → MC+P/L
- Alloc. into Projects
(size etc.)
→ [Review by PSG's]

Project → OOD/MC/P/L

- Mgmt. of Product Design
[Bus Plans]

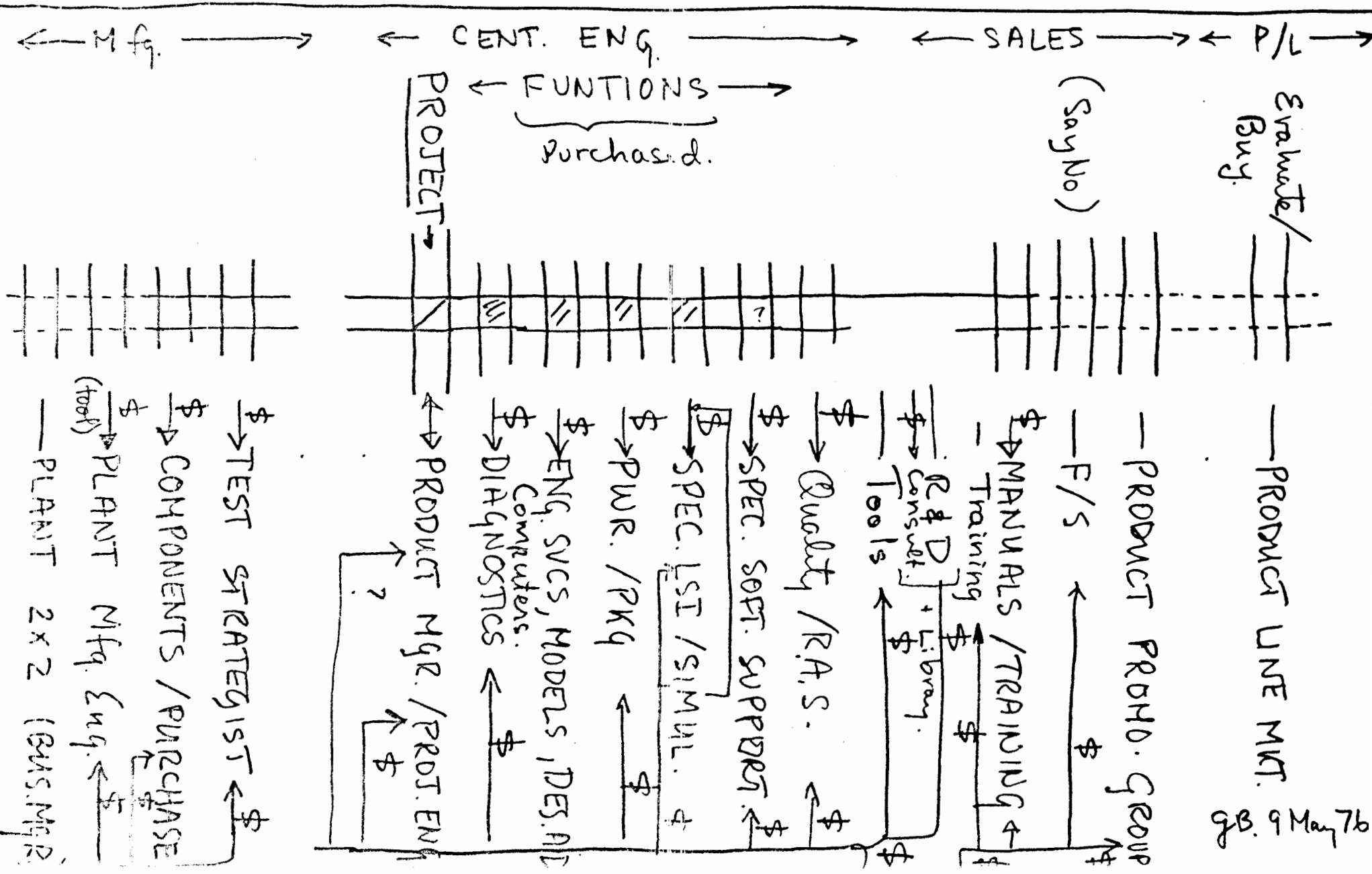
Decision-making at
[3-levels] of OOD ("OOD -- Technology Area - Project")

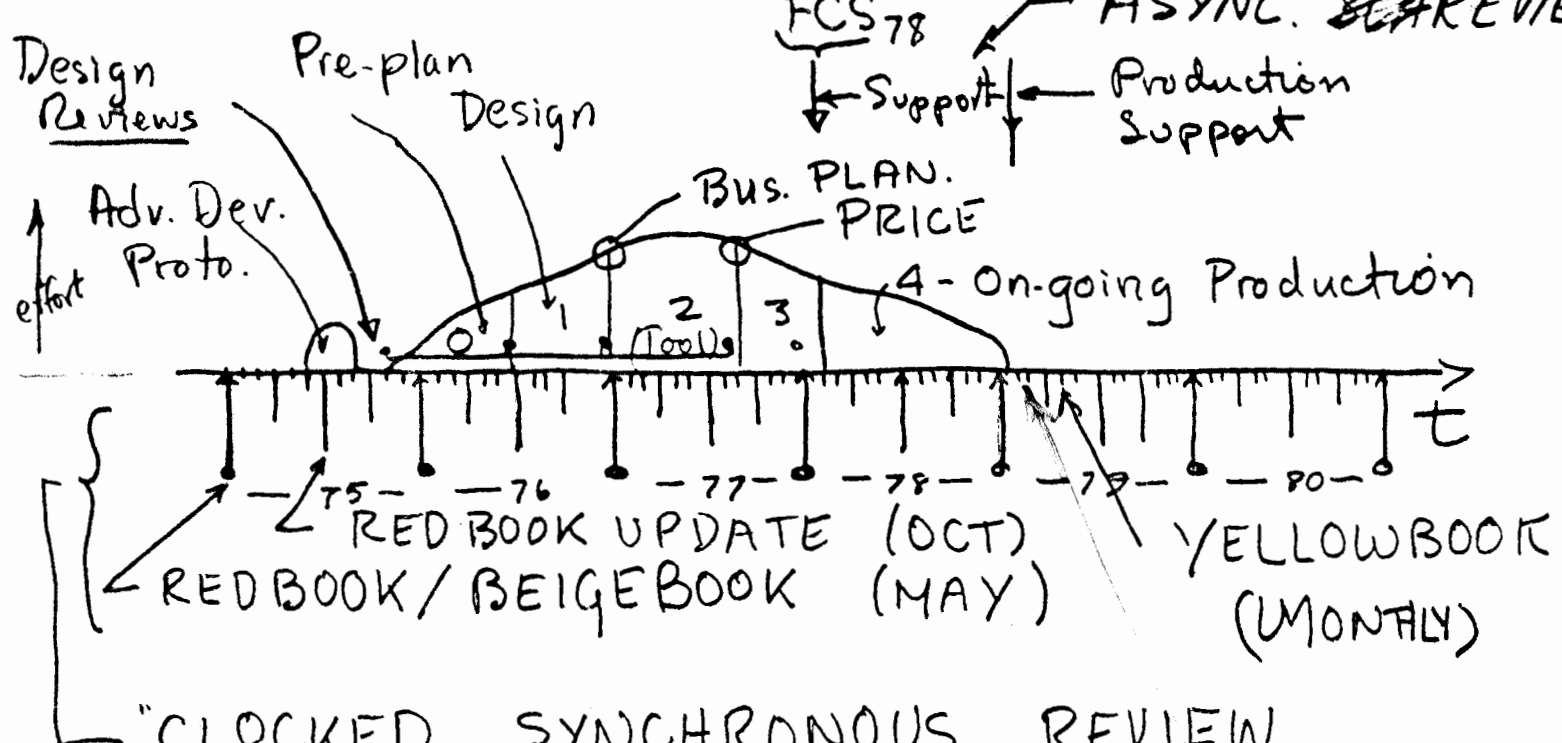
GB May 9, 1976.

Project MATRIX

Projects are formed from Matrix of Functional / Product Skills.

(Matrixed person has: 2 bosses, lives with project, skill orientation) and Many functions are outside Central Eng.





Project Effort vs. time.

Reviews:

SYNCHRONOUS

- Redbook
- Redbook update
- Yellow Book (status update)

Asynchronous (Project Based)

- Prototype (Adv. Dev.). {Idea Generation}.
- Prel. Plan. {Alternatives to select from}.
- Design Reviews (Measures/monitors Project)
- Business Plans (Reviews)
  - 2 page (to go into design)
  - To go ahead
  - To produce
  - To build/sell
- PSG monitor

gb May 9, 1976.

NEW TECHNOLOGIES TO BE ASSIGNED, WATCHED, AND ASSIMULATED

(IN PRIORITY) *-REQUIRES ORGANIZATIONAL/PERSON CHANGE

*COMPUTERS THAT ARE ULTRA RELIABLE, DON'T FAIL, AND/OR REPAIR THEMSELVES ⇒ FS/ENG./R&D

SEMICONDUCTOR TECHNOLOGY ⇒ STRENGTHEN ASAP IN CPU + SEMI GROUPS

ELSI FOR LARGE COMPUTERS

ELSI FOR SMALL COMPUTERS

*TERMINALS (HIGH QUALITY PRINTING, ALL TERMINALS ⇒ GRAPHICS) ⇒ ?

*TERMINALS:DETERMINE SMART/DUMB BOUNDRY ⇒ ADV. DEV. + TERMINALS

*MULTI-PROCESSOR/MULTI-COMPUTERS SYSTEMS ⇒ PROJECT HOME NEEDED!

VIRTUAL MEMORIES--HIGH AND ESPECIALLY LOW END ⇒ ADV. DEV.+ GROUPS?

*MOVEMENT OF HARDWARE/SOFTWARE BOUNDRY TO MORE COMPLEXITY IN

HARDWARE ⇒ COMM, DISKS, TAPE, TERMINALS + ADV. DEV.

*MEMORY HIERARCHIES IN SUB-SYSTEM ⇒ DISK SUBSYSTEMS GROUP.

ULTRA RELIABLE SOFTWARE ⇒ ADV. DEV.??

BETTER HUMAN ENGINEERING ⇒ R & D? TECHNICAL AUDIT?

ADVANCED MEMORIES: CCD, ELECTRON BEAM ⇒ ADV. DEV.?/ MEMORY GROUP

TV TECHNOLOGY (CABLES, VIDEO DISK, COLOR MOUNITOR) ⇒ ADV.DEV.

HIGH SPEED, LOW COST, SERIAL LINK (E.G. CATV, FIBERS, COMP) ⇒ ?

COMPUTER USE IN OFFICE ⇒ ADV.DEV. + BUS PRODUCTS + COMM.

BETTER INTERFACE TO CONTINUOUS (ANALOG) DOMAIN ⇒ ADV.DEV.

SIGNFICANTLY EASE USE OF COMPUTERS (E.G. APPLICATIONS PROGRAM GENERATION) ⇒ R.

VOICE I/O ⇒ R

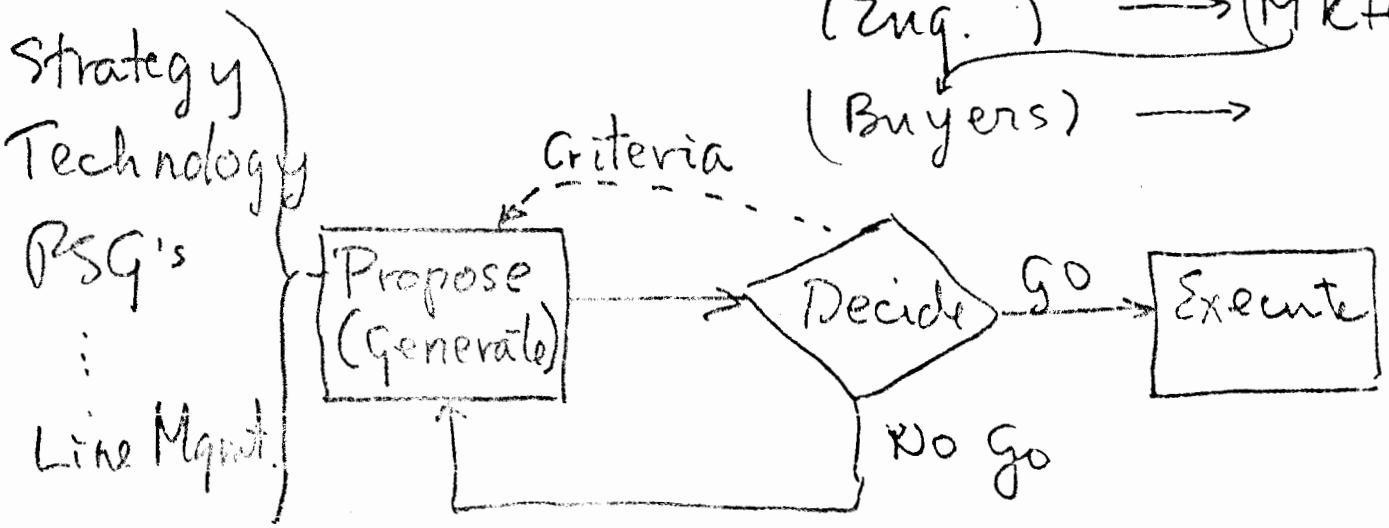
GB
11/6/75

DECISION-MAKING WITHIN OOD

GB
May 9, 1976

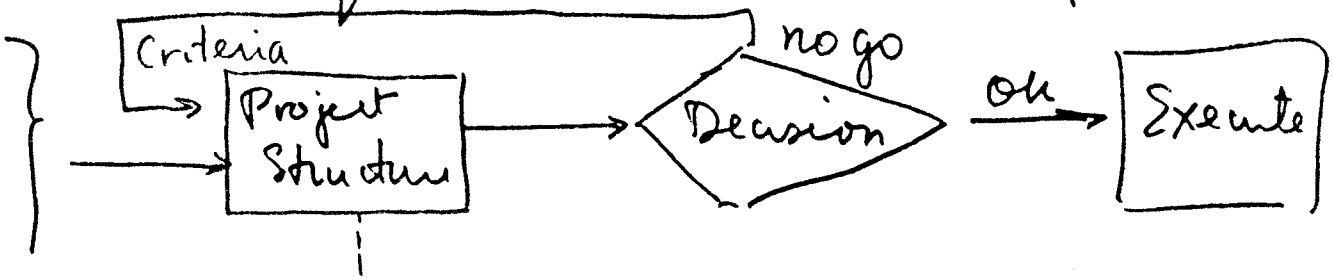
- Fundamentally no substitute for Hi-Q. Person(s)
- Basically decisions are made according to Model set forth by Ken and Op. Comm.
- Carry forward notion of a (decision) process & attempt to form structures (Organize) such that: Individuals can propose and have decided such that individuals are responsible to do. (i.e. he who plans, does).

- Process requires: Producers → Consumers
  (generators) → (Testors)
  (Designers) → (Evaluators)
  (Eng.) → (MKters)
  (Buyers) → →



Techniques for Decision-making

May 9, 1976.



Inputs (Comm.) ——→ monitor fcn.

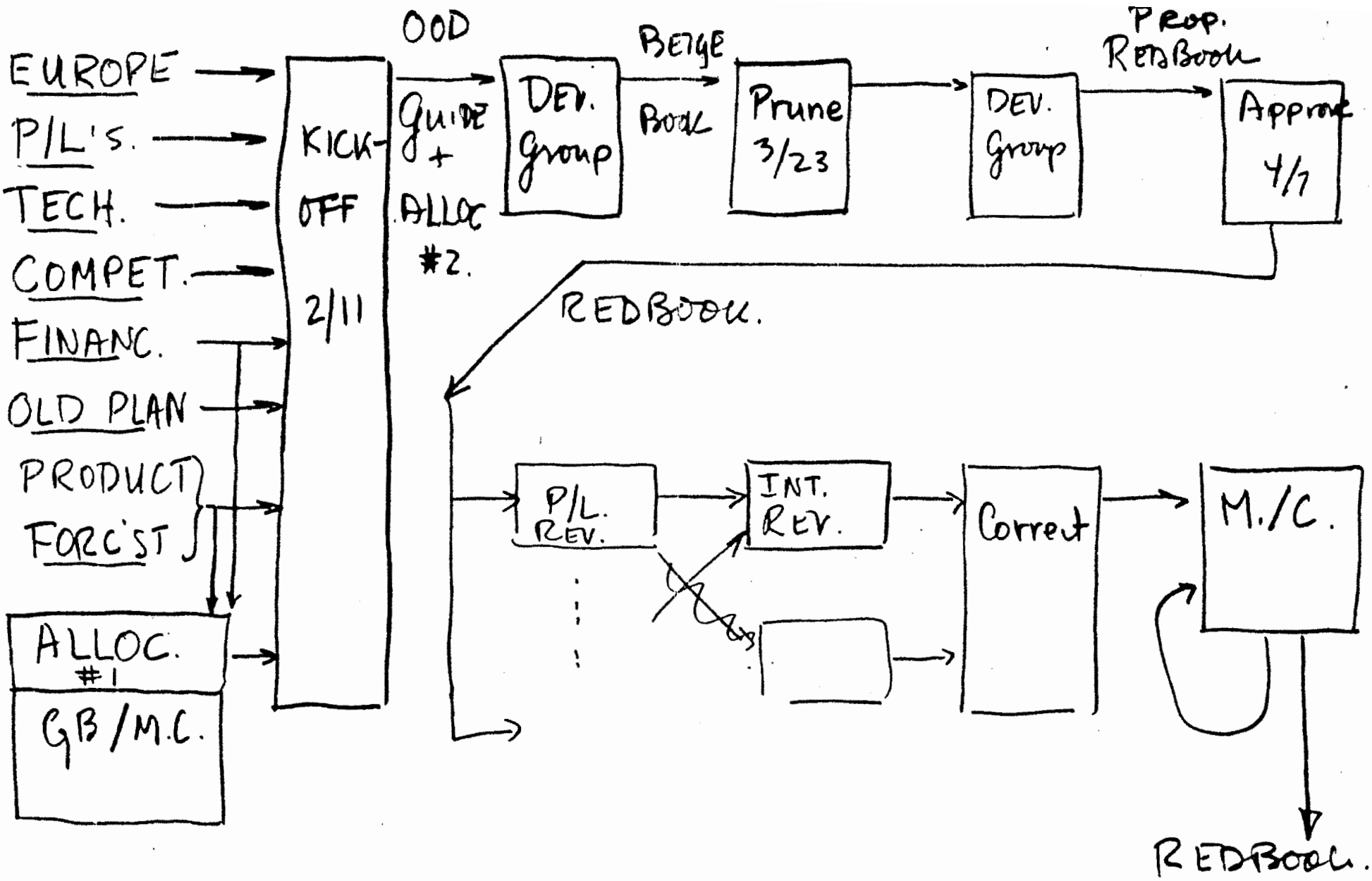
- 5 year strategic plans, (Budget allocation)
  Redbook. ; Meetings
  DEC Stds. / Policies / processes (eg. approval process).
  DEC Goals (roi program).
  Competitive ideas
  Technology base: R&D; Idea; Invention
  → Market Requirement (Need). Psg.
  Specify Action ... i.e. Tell 'em. + Manage

STRUCTURE / MANAGE {Team, Task force, Committee, Indiv.)

Organiz. Engineering. / Matrix / Move People (skills)
Educate / Train
Consultants. Or Get 1 or 2 Good People.

Monitor
Yellow books, Redbooks, PSG's.

Decision
Specify Problem, Goals, Constraints, Evaluation Criteria

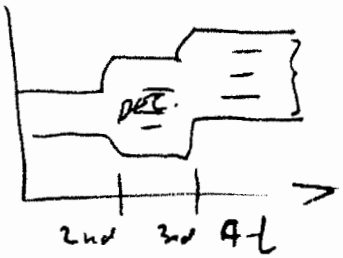


8-QTR. ROLLING REDBOOK. PROCESS.

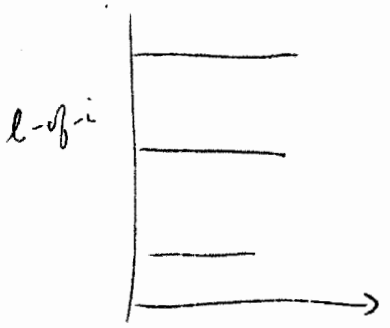
(EACH 2 QTR'S).

GB 2/28/76

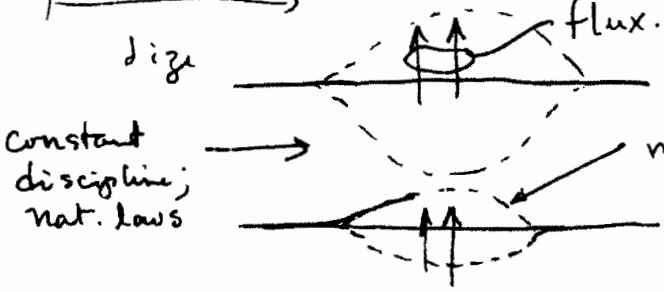
Shein Discussion

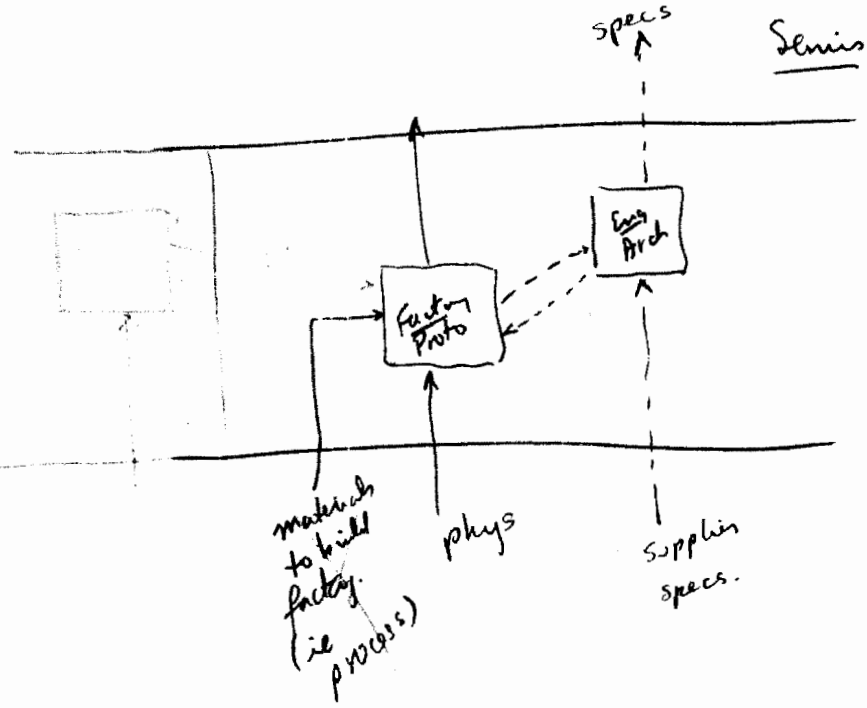


Calculator
- proj. -
- human eq. -
- Semis, Leds, MB.
- base calculator need ←



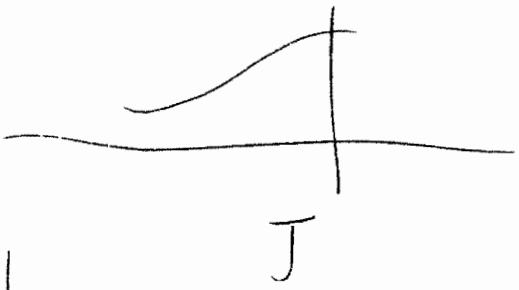
Engineer's mobility ~ greatest leaning;
- greatest new tech from below – push.
- " new applic. " above – pull.

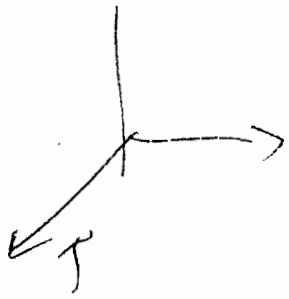




Semis / Disks improve due to clarity of goal – hence clear flux.

⇒ 1~2 dimensional perf. meas.





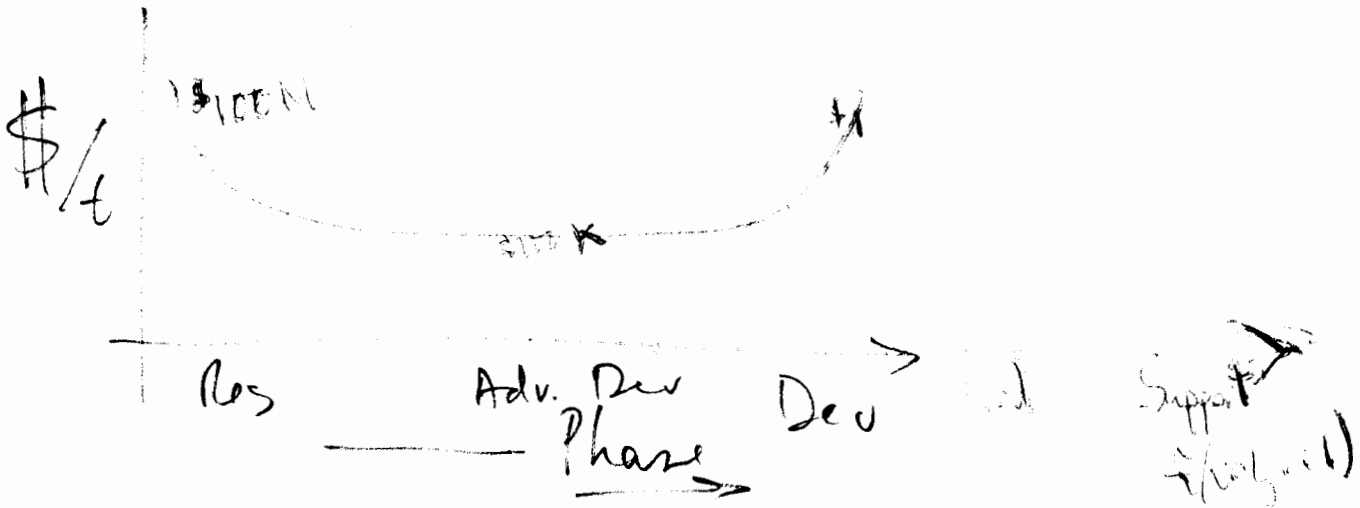
→ what "type" does what job?
- where is "right" plane (level) to be? for Eng. – security; leaning?
- How can one move levels? ↗ ↘ ; rarely ↘
- How does I manage a project or ensemble of projects to avoid obsolety engineers; or designing obsolete products?
- what a "location theory" for a complex structure like this?
- appropriate bosses & for each level are?

4/6/77

Jim

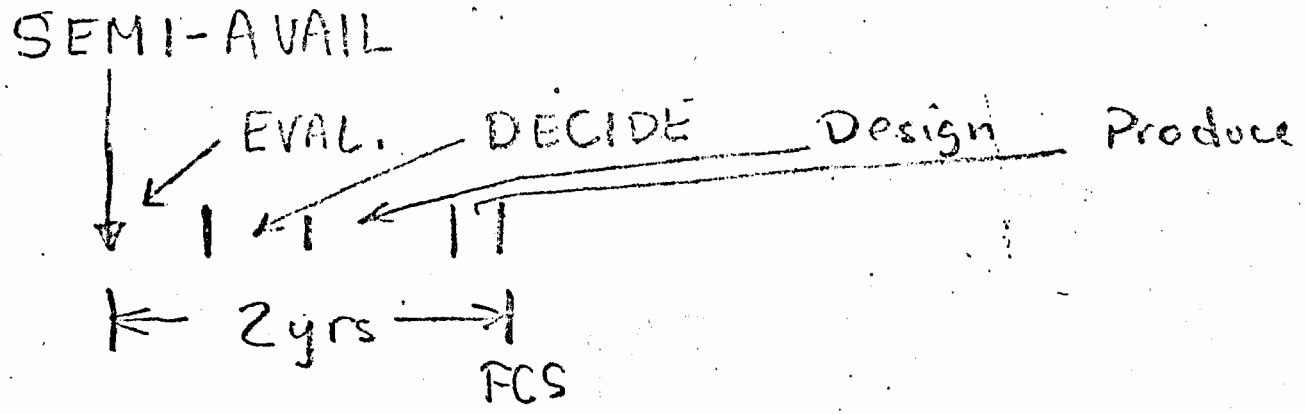
Did the curve you

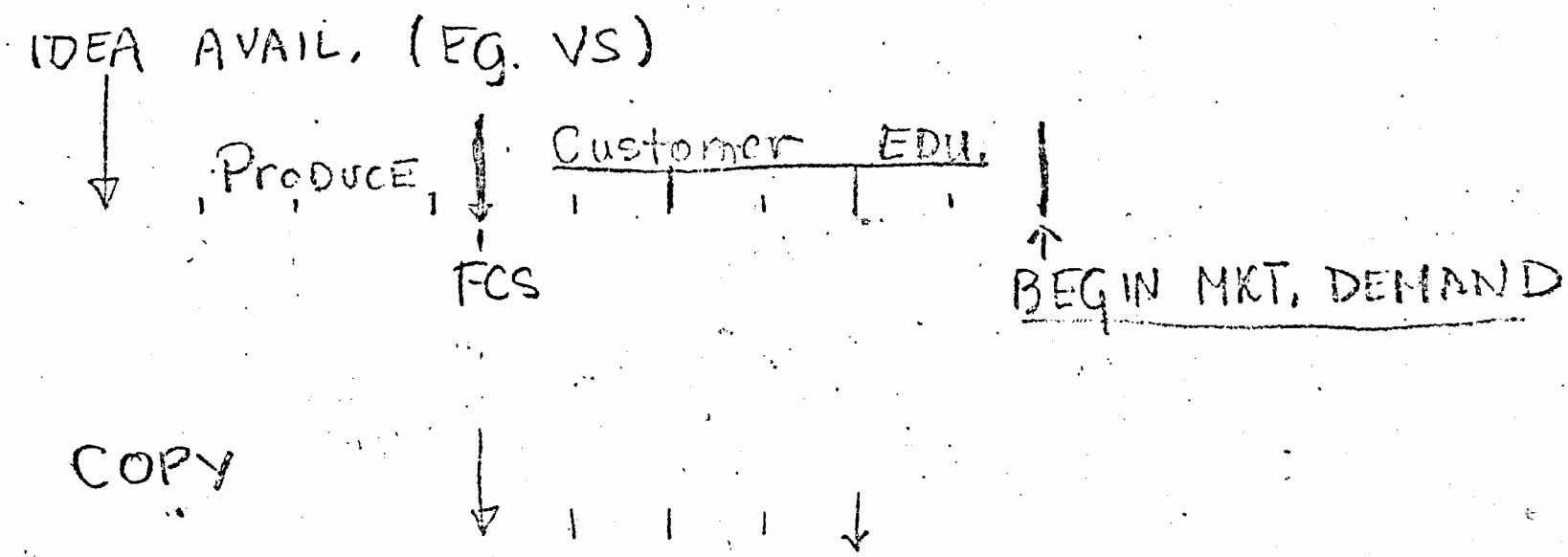
draw for $



have any data points for various things (eg. bubbles, semis, tires)

Gordon.


SEMI-AVAIL
EVAL.
DECIDE
Design
Produce
2yrs
FCS


IDEA AVAIL. (EG. VS)
PRODUCE
Customer EDU.
FCS
BEGIN MKT. DEMAND
COPY
FCS - COPY SHIP

GB 2/2/76

PROCESS

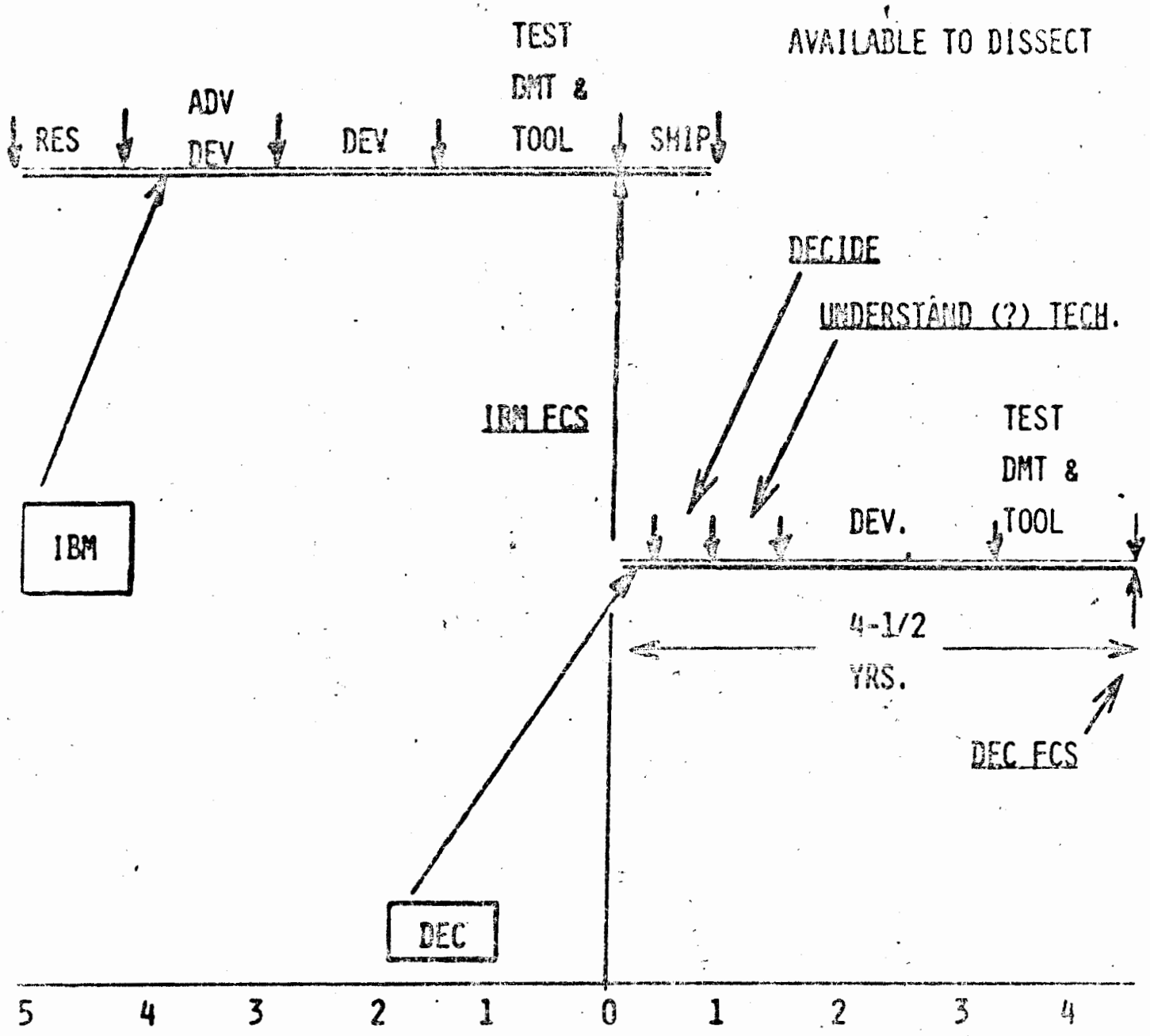
LINE-YEARS (T)

multi-disciplin

PROCESS	SOFTWARE (OS, LANGUAGES)	CPU (LARGE)	DISK
RESEARCH	0-20	1-10	1-10
DISCLOSURE PATENTS			
TECHNOLOGY ADVANCED DEVELOPMENT	1/2-2	1-2	1-2
PEOPLE (ISS, MRX)			
(schedulable) DEVELOPMENT	1-2	1-2 ANNOUNCE MKT DEMAND	>2 ANNOUNCE MKT DEMAND
TOOL-UP			
TEST, TOOL & DMT	1/4-1/2	1/2-1	1
FCS			
SHIP	1/4-1/2	1/4-1/2	1/4-1/2
EDUCATE & USE	1/2-5 MKT DEMAND	1/2	0

Commod

Education / understand (MKT)



TIMES FOR IBM/DEC DISKS

→ Museum.
→ Space (control plans
→ ufilm: film
→ product test.
~~Bl~~ & Critique
→ Set up Set com on Computer + anal
→ Presents, instructs, etc.

KO
→ my son and CSS.
→ Engs only do budget
→ Market no dem good.
→ We need a style box! Don't ask them.
- Lincoln lab syndrome.

Ken — I'm terrified Want your help! | Jim Repn

- Group should not become decoupled ... work

Monitoring to get development changed.

- Group should get (push ~~defer~~ adv. dev. into various

Transfer Groups (since they're ~~more~~ responsible).

- {Should / Will} we have a more isolated group for R/D? (New Hampshire?).

→ IBM.

→ Intel

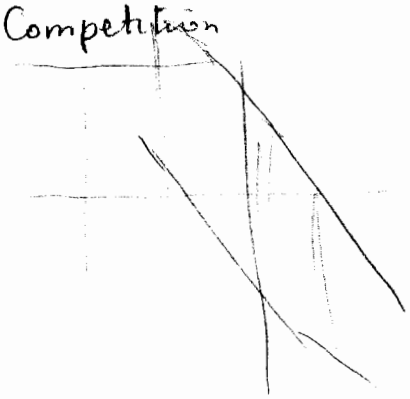
Talk

- Xerox →
- Universities: Stanford; Cal Tech; →

~~Infiltrating~~

- Infiltrating development with knowledge →
- ~~for~~

Competition



where are we going?

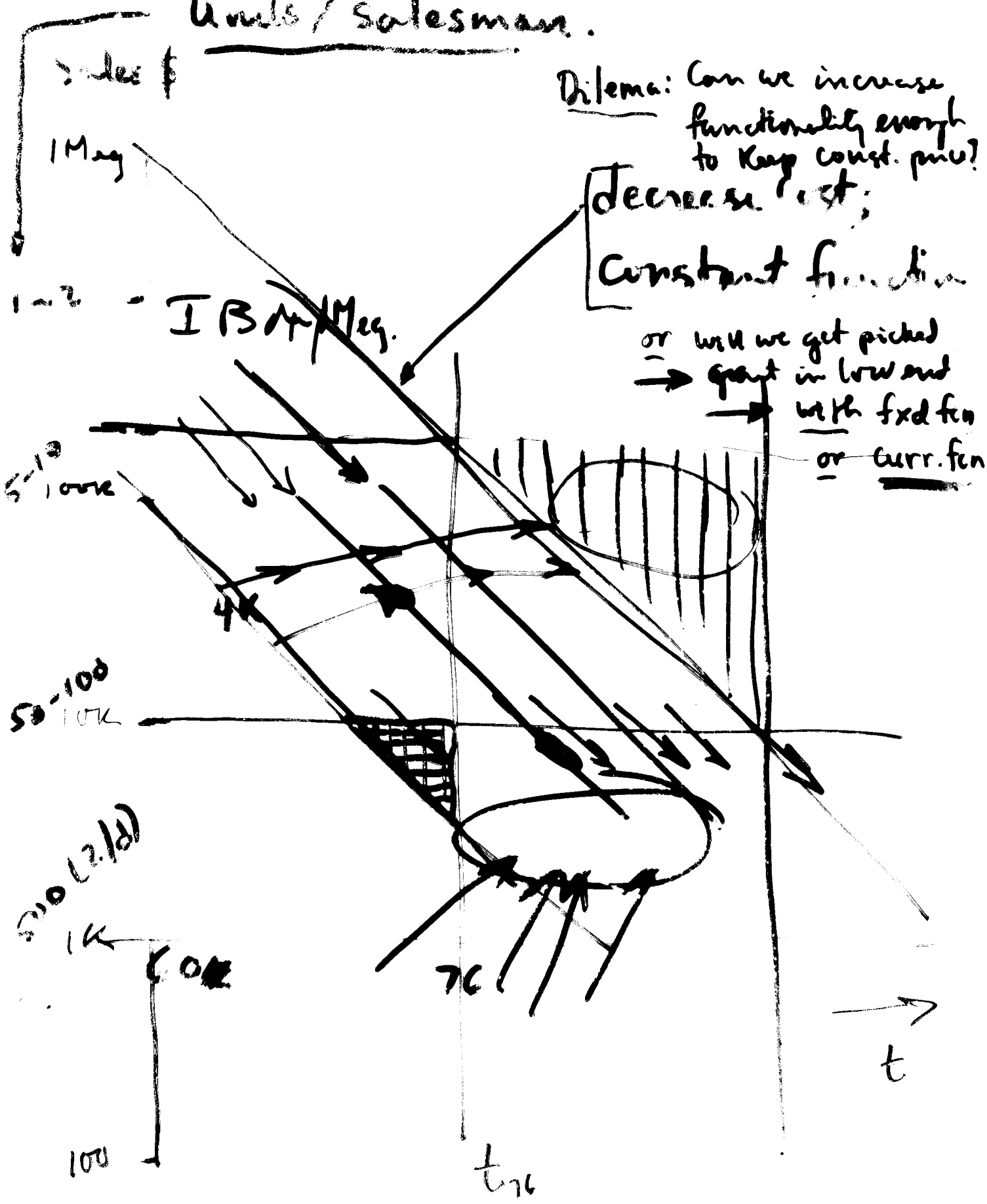
Get you to worry with me: 2 times.

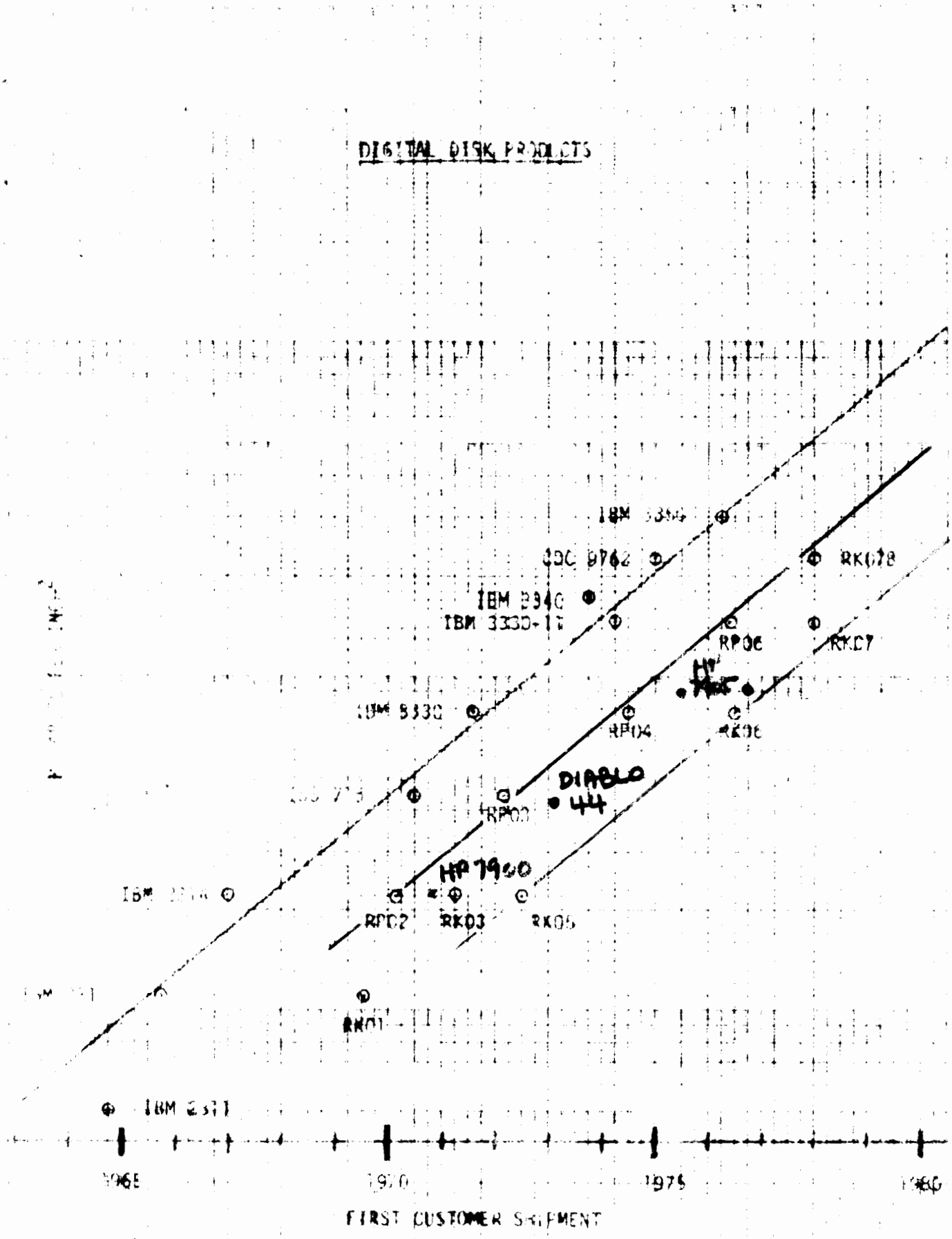
→ not competitive → [can we get out of hole?

→ ~~good~~ backlog. ~~Will~~ Will new products be good enough?

→ Complacency

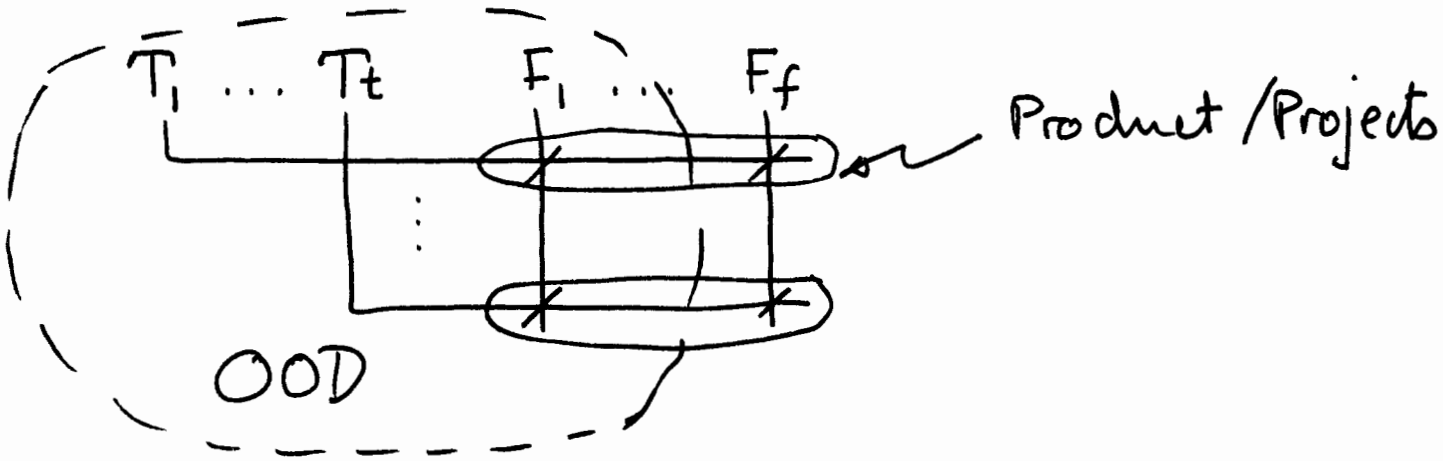
R/D problem:


Units / Salesman.
Dilema: Can we increase functionality enough to keep const. price?
Decrease cost;
Constant function
or will we get picked
grant in low end
with fxd fcn
or curr. fcn
IBM/Meg.
1 Meg
1-2
5-10
10K
50-100
10K
500 (2.5)
1K
100
70
t
t_{70}


DIGITAL DISK PRODUCTS
IBM 3340
DEC 9762
RK078
IBM 3340
IBM 3330-11
RP06
RK07
IBM 3330
RP04
RK06
DIABLO
44
RP03
HP 7900
RP02
RK03
RK05
RK01
IBM 2311
1965
1970
1975
FIRST CUSTOMER SHIPMENT

How Are We Organized? [PEOPLE] GB May 9, 1974

- Functionally by skills (eg. drafting) and by technology (eg. disk mem.) with Matrix Mgmt. via Technology using Skills



How do we Measure Output?

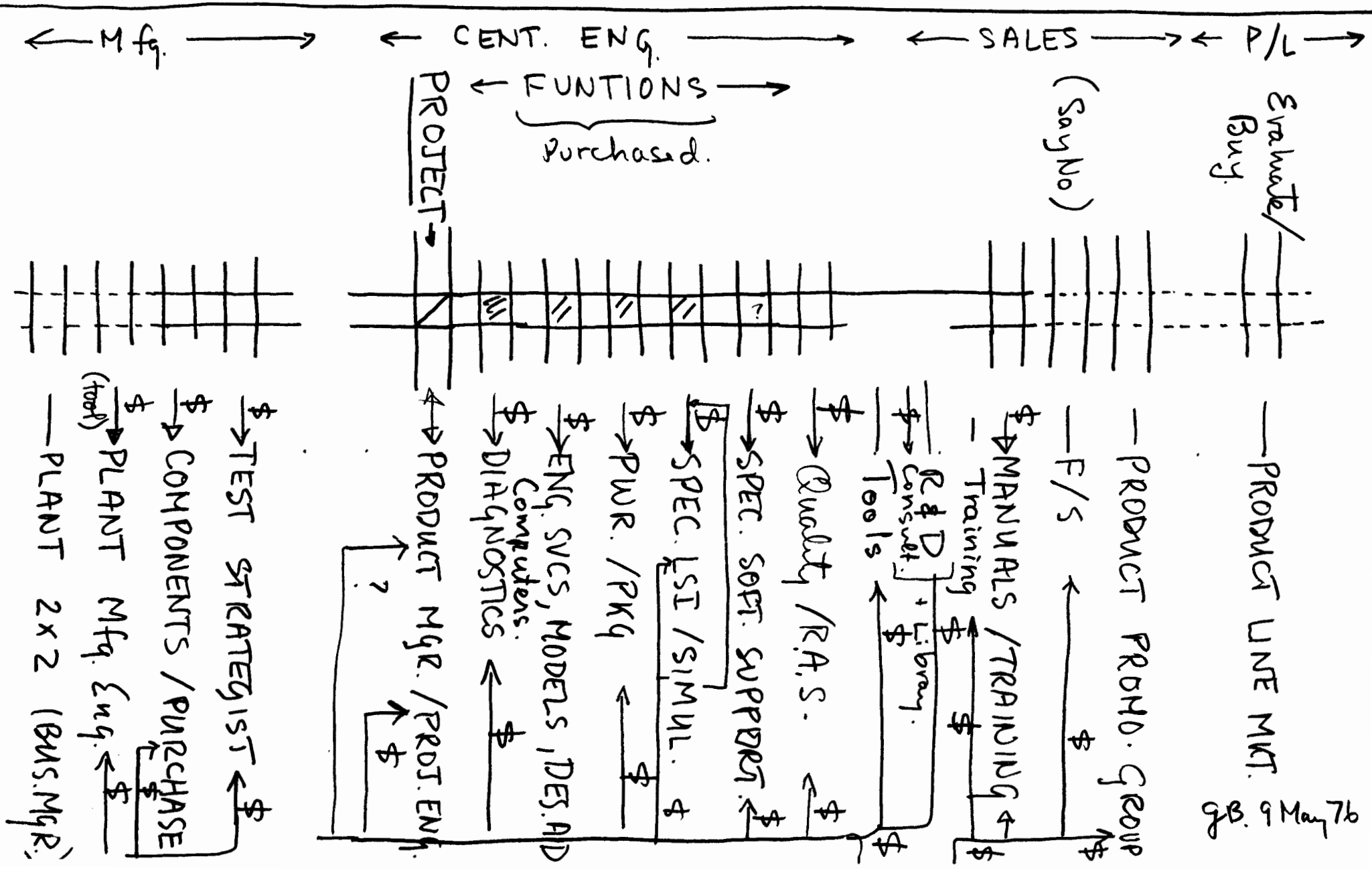
- Mostly by "success" of product ≈ NOR!
  - Schedule
  - $. develop and $. cost
  - Performance of Product (eg. reliability, function, ...)
  - Rarely as/ agreement.
  -
- Gut feel
  - Truly useful • Does it feel good? (Weak link)
  - Adds evaluation dimension
  - Doesn't lose Sales for Other Systems.

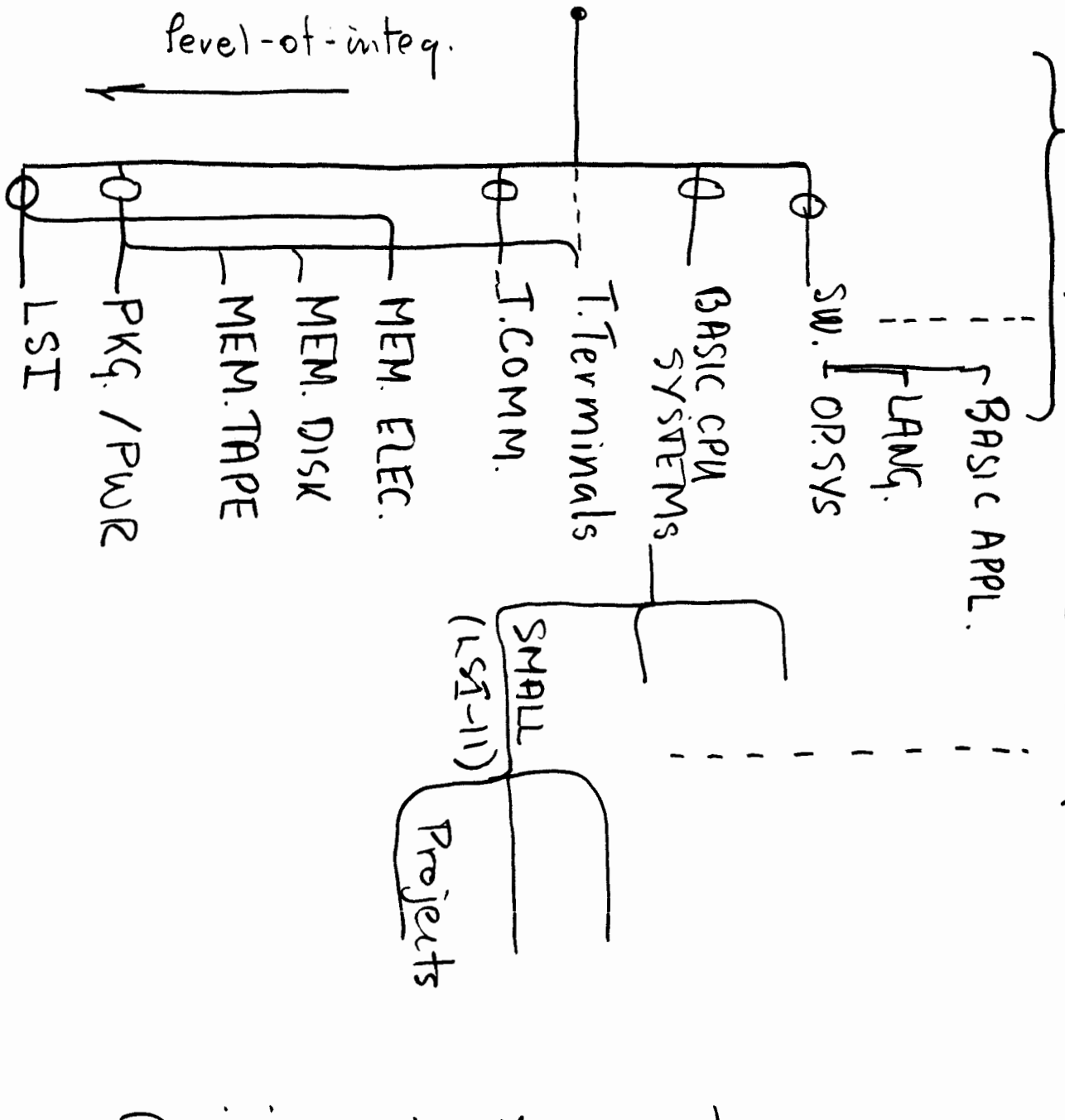
Project MATRIX

Projects are formed from Matrix of Functional / Product Skills.

(Matrixed person has: 2 bosses, lives with project, skill orientation)

and Many functions are outside Central Eng.





Proposer / Decider

(Producer) (Consumer)

OOD → MC+P/L

- Allocation of Products by: SIZE / technology / time (5) / Tools

→ [Rev. by Products Comm.]

Technology Group → MC+P/L

- Alloc. into Projects (size etc.)

→ [Review by PSG's]

Project → OOD/MC/P/L

- Mgmt. of Product Design

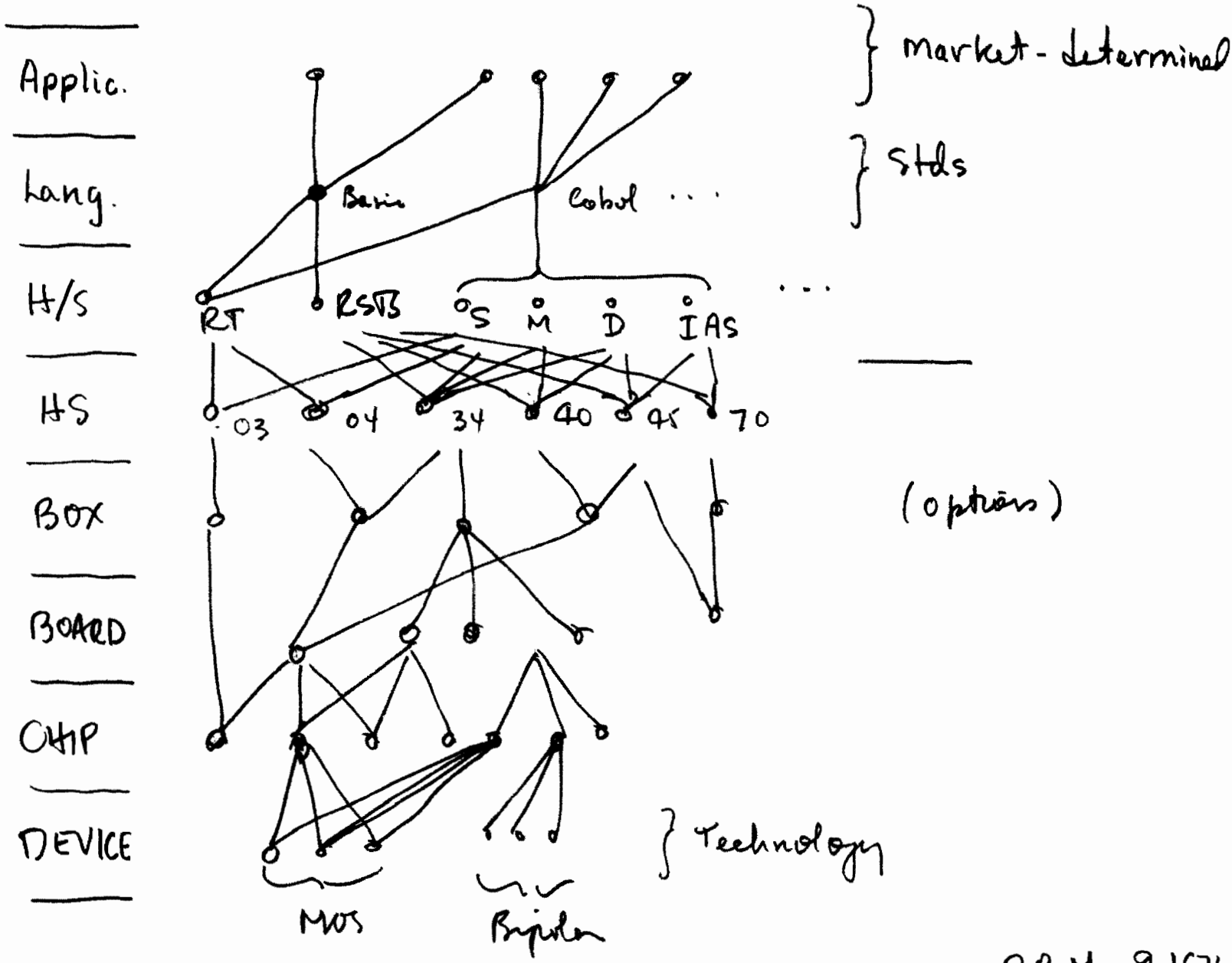
[Bus. Plans]

Decision-making at 3-levels of OOD (OOD - Technology Area - Project)

GB May 9, 1976.

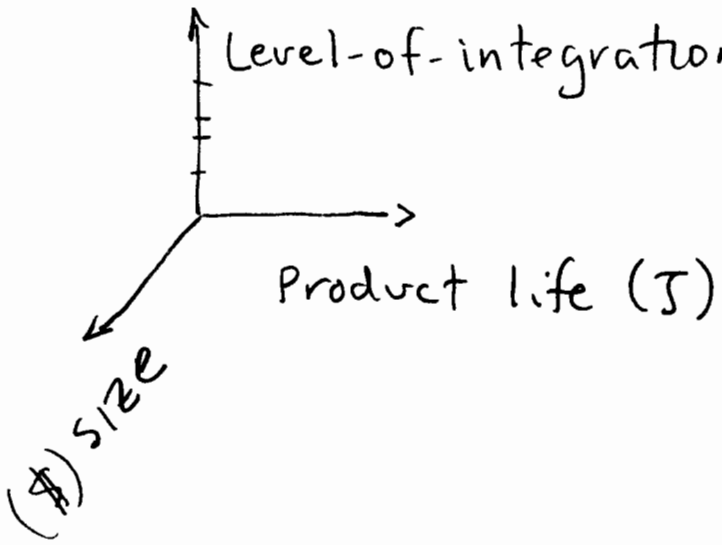
THE PRODUCT: Allocate Resources in Size, life cycle (T), level-of-integ.

Computer System Development IS A Network (NOT JUST A Tree-structured HIERARCHY) OF 8 DISTINCT LEVELS. (IN ESSENCE, A PROJECT MAY DEPEND ON 1 OR MORE SUB PROJECTS AND A PROJECT MAY AFFECT SEVERAL SUCCESSOR PROJECTS)



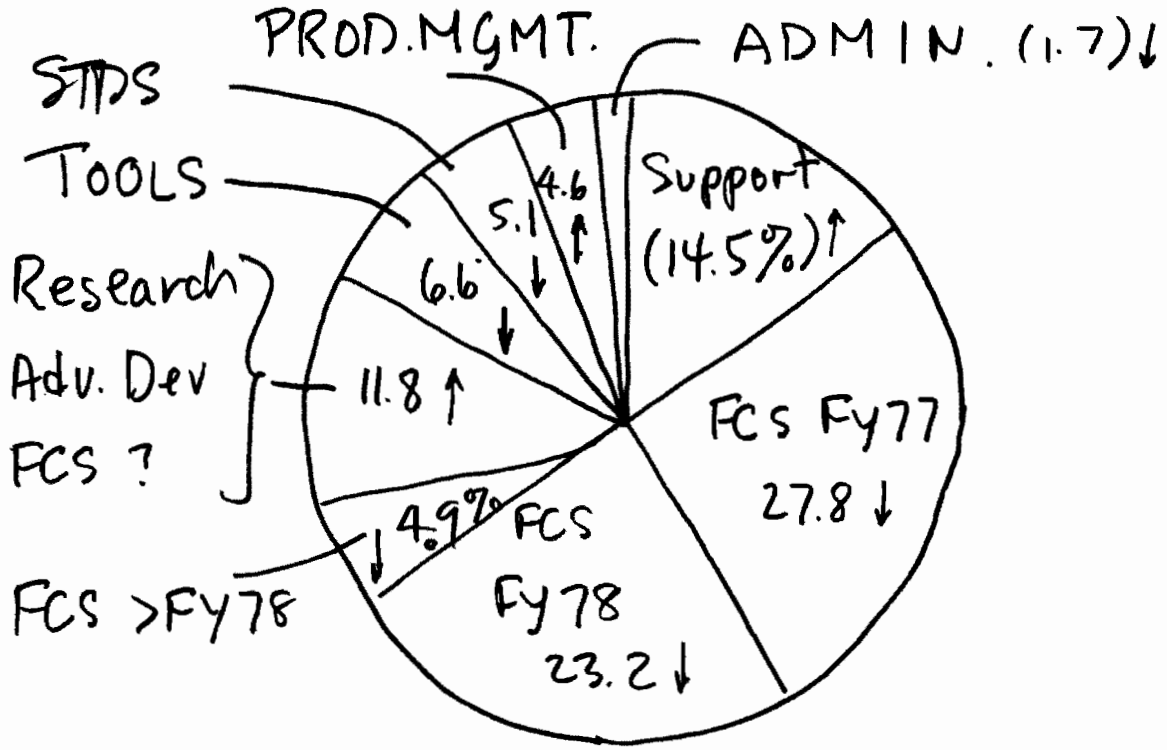
GB May 9, 1976

OOD MGMT IS FUNDAMENTALLY RESOURCE ALLOCATION IN SPACE

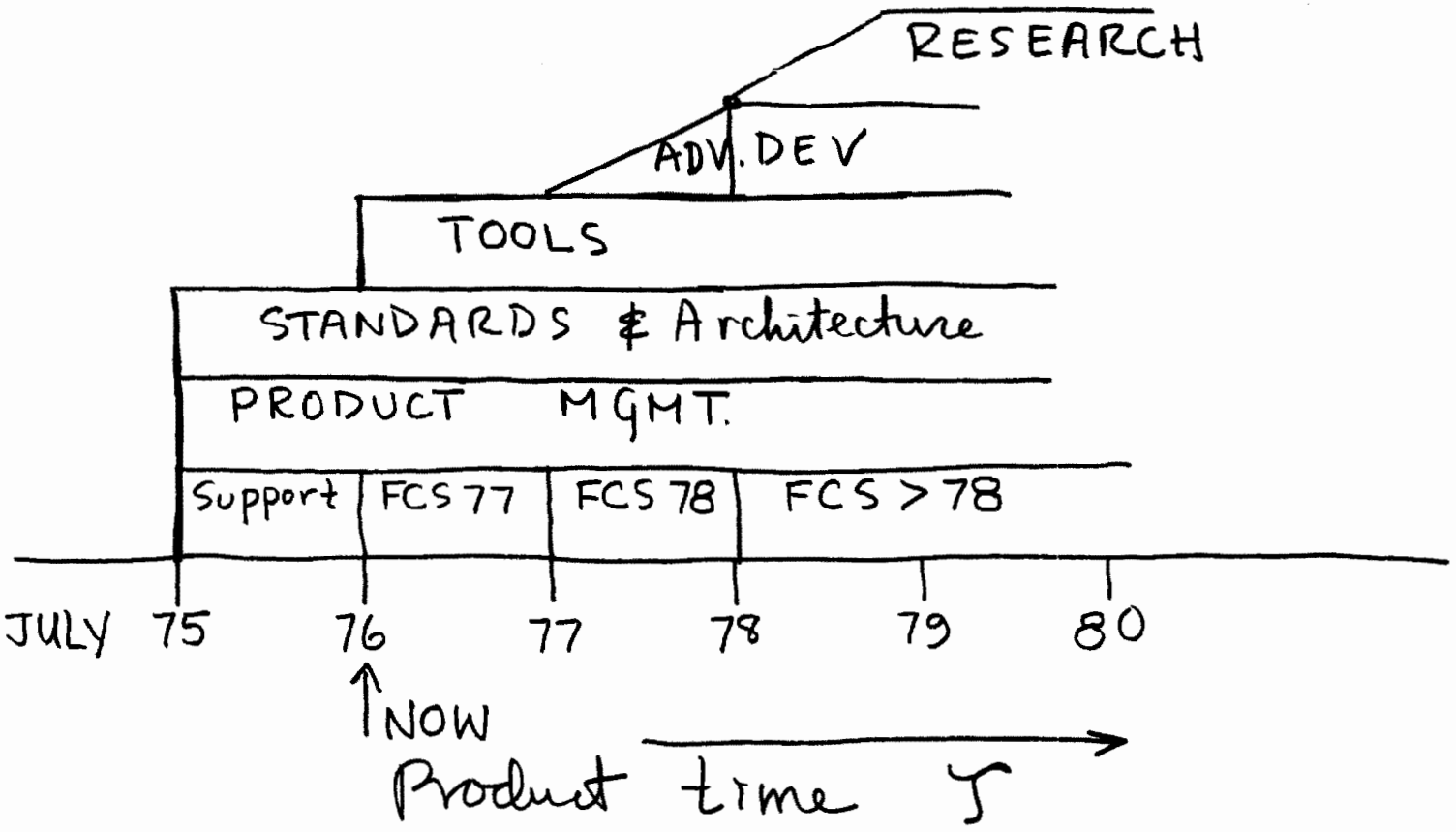


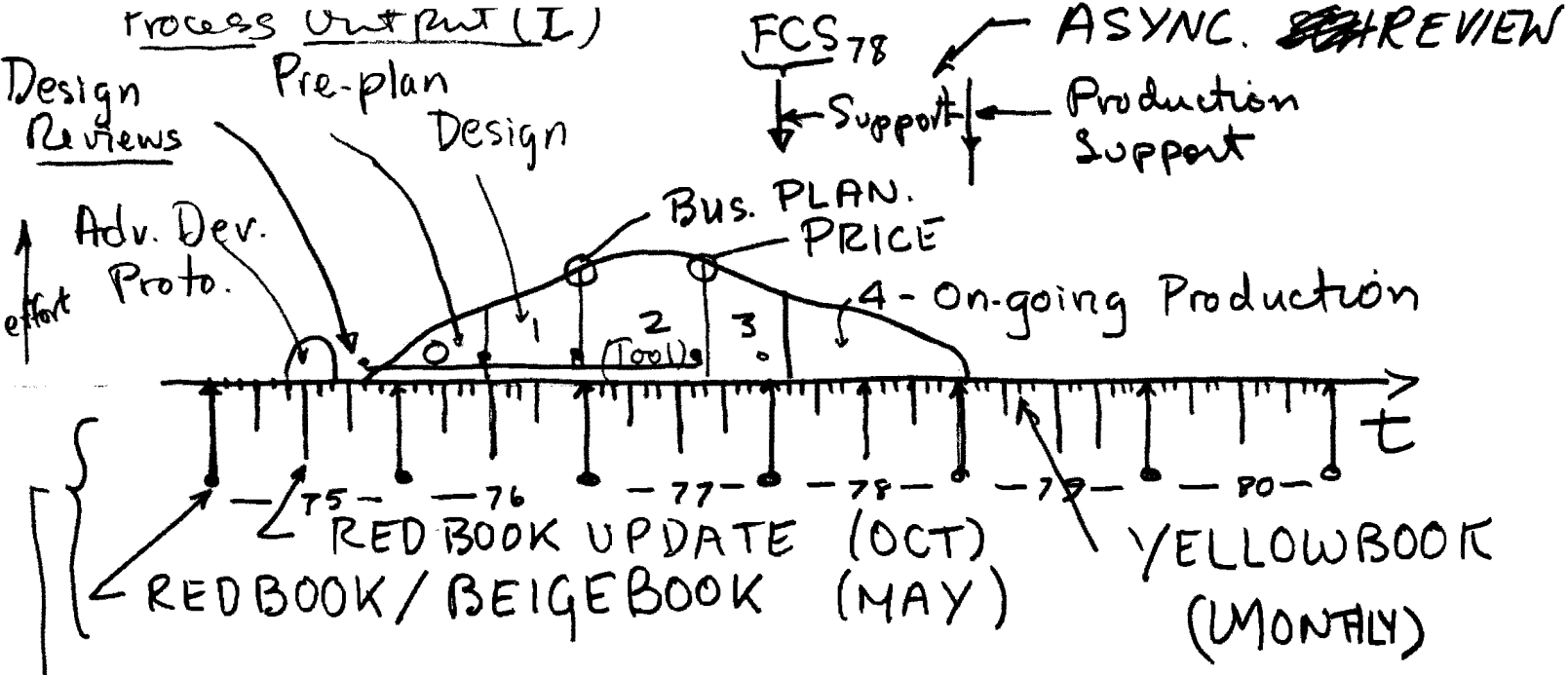
Resources Measurement Categories gb in time (T) dimension.

May 9, 1976



FY 77 Budget. (Trend FY 78)





Project Effort vs. time.

Reviews:

SYNCHRONOUS

- Redbook
- Redbook update
- Yellow Book (status update)

Asynchronous (Project Based)

- Prototype (Adv. Dev.). {Idea Generation}.
- Prel. Plan. {Alternatives to Select from}.
- Design Reviews (Measures/Monitors Project)
- Business Plans (Reviews)
  - 2 page (to go into design)
  - To go ahead
  - To produce
  - To build/sell.
- PSG monitor

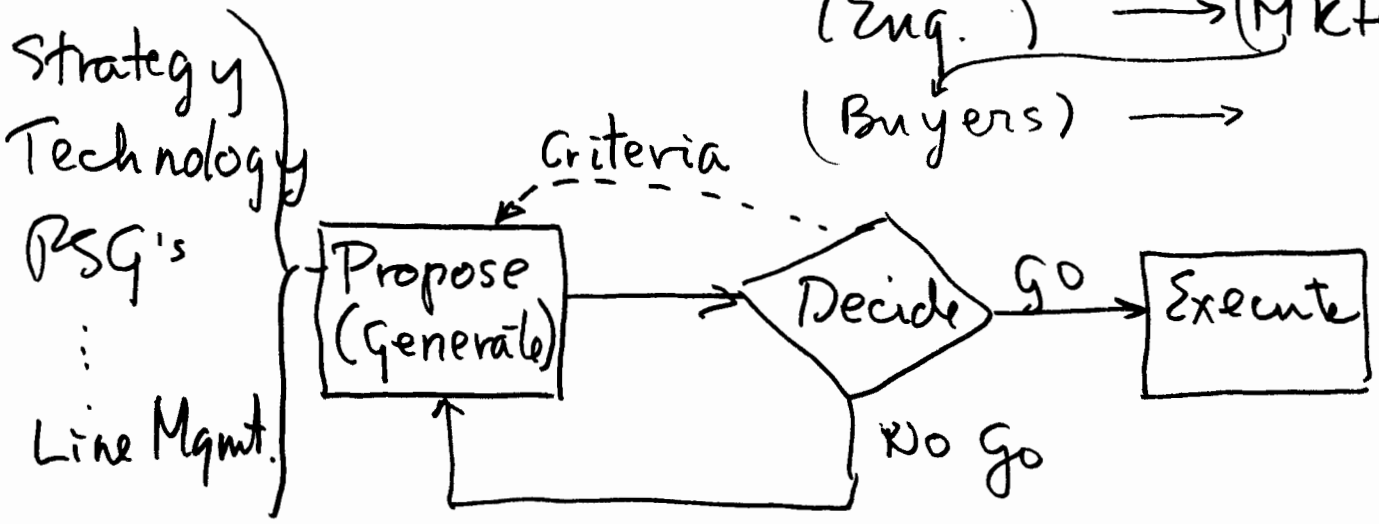
gb May 9. 1976.

DECISION-MAKING WITHIN OOD

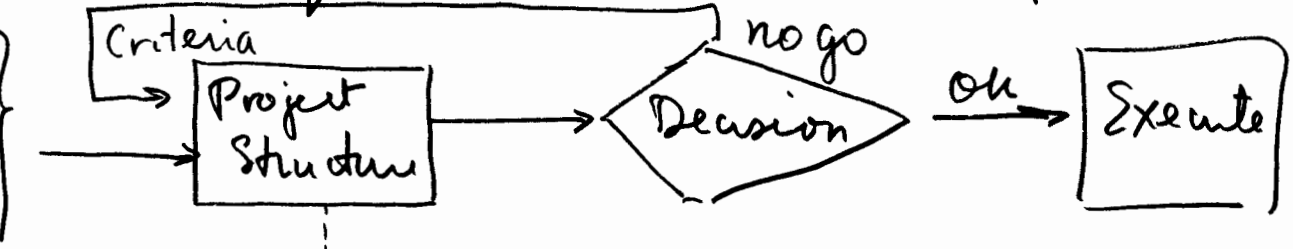
GB
May 9, 1976

- Fundamentally no substitute for Hi-Q. Person(s)
- Basically decisions are made according to model set forth by Ken and Op. Comm.
- Carry forward notion of a (decision) process & attempt to form structures (organize) such that: Individuals can propose and have decided such that individuals are responsible to do. (i.e. he who plans, does).

- Process requires: Producers → Consumers
  (generators) → (Testors)
  (Designers) → (Evaluators)
  (Eng.) → (MKters)
  (Buyers) → →



(General) Techniques for Decision-making May 9, 1976.



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Decision

Specify Problem, Goals, Constraints, Evaluation Criteria

(tradeoffs)

GB 9 May 76

Problems in Decision-making

We are significantly Market driven (via PSG's, MKters, etc.).
As we get larger, it is harder to Recover from poor MKT-based (Persons) ~~Dec~~ Recommendations vs. Tech. risk.

Examples:

→ Don't write down Goals, etc. hence instability
→ Don't move out far enough (mP)
→ Don't understand new mkt. (LSI-11)
→ Don't understand Systems we'll Sell (eg. Size on 11/70)
→ Don't understand changing mkt. (optimize R~R vs. Real Performance).
→ "Mill Around", No Clear decision/Test (CIS).
→ Overall the developers want to be heros ... i.e. building anything is OK. and avoids risk of Project Cancel. (eg. Unicorn)
→ Don't understand risk of a fully peopled company. Mfg. ... F/S. — hence minimum product cost, max. user (etc.) Cost.

CONTROL (DECISIONS) VIA FUNDING gfb 9 May 76

- **PROJECT DIRECT** (Hdw., SOFT, Hdw+ Soft.)

  Memory (electronic, disk, tape), Comm., terminals, CPU's, Operating Systems, Languages.

.

.

- **PROJECT SUPPORT** (Fully purchased Services)

  Drafting, Model shops, Consulting, Computers, EDP.

.

- **PROJECT SUPPORT WITH TECHNOLOGY BASE**

  LSI, PKG., POWER, DIGGNOSTICS, QUALITY
  - Purchasing, Components, testing, tool-up
  - Manuals, Training.

.

.

- **Open loop**

  Tools, Standards, Researeh, Adv. Dev.
  Library, Program library.
  Field Service, Software Support, Training.

(Tradeoffs)

GB 9 May 76

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CONTROL (DECISIONS) VIA FUNDING gfb 9 May 74

- PROJECT DIRECT (Hdw., SOFT, Hdw+Soft.)

  Memory (electronic, disk, tape), Comm., terminals, CPU's, Operating Systems, Languages.

- PROJECT SUPPORT (Fully purchased Services)

  Drafting, Model shops, Consulting, Computers, EDP.

- PROJECT SUPPORT WITH TECHNOLOGY BASE

  LSI, PKG., POWER, DIGGNOSTICS, QUALITY
  - Purchasing, Components, testing, tool-up
  - Manuals, Training.

- Open loop

  Tools, Standards, Research, Adv. Dev.
  Library, Program library.
  Field Service, Software Support, Training.

SPACE PERSON. Updates LONG-RANGE SPACE PLAN

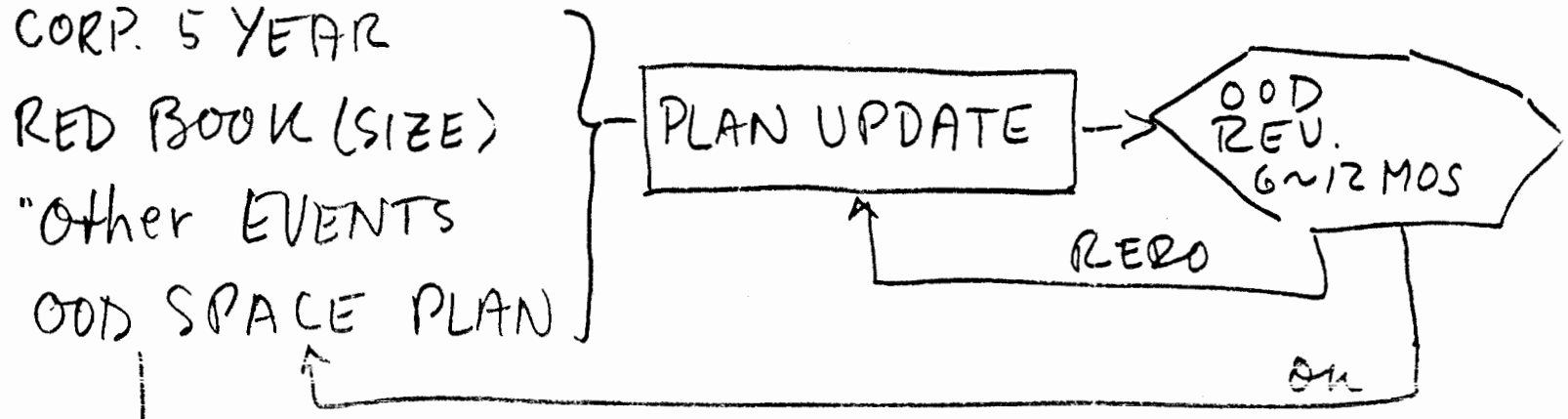
GUIDELINES

WHO/GOES WHERE

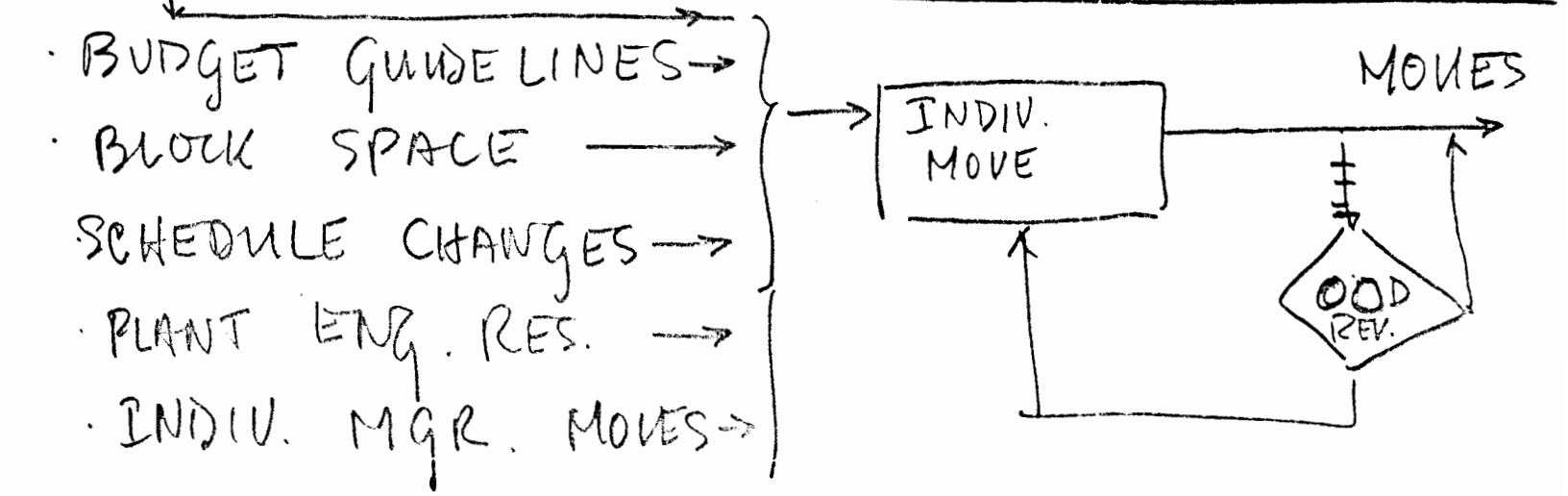
ASSIGNS SPACE

WORKS WITH INDIVIDUAL MGRS

INTERFACES PLANT ENG.



LONG-RANGE PLAN. (STRATEGY)



TACTICAL MOVES

SPACE PROCESS

9 May 76 GD

SPACE PERSON. Updates LONG-RANGE SPACE PLAN

GUIDELINES

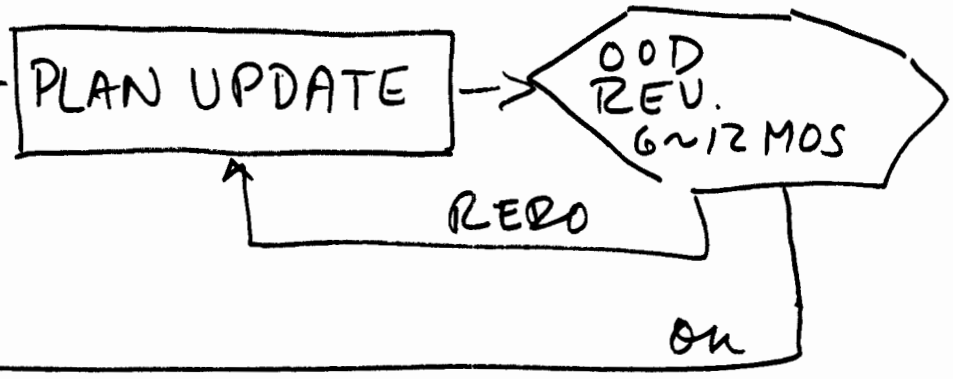
WHO/GOES WHERE

ASSIGNS SPACE

WORKS WITH INDIVIDUAL MGRS

INTERFACES PLANT ENG.

GUIDELINES
CORP. 5 YEAR
RED BOOK (SIZE)
"Other EVENTS
OOD SPACE PLAN



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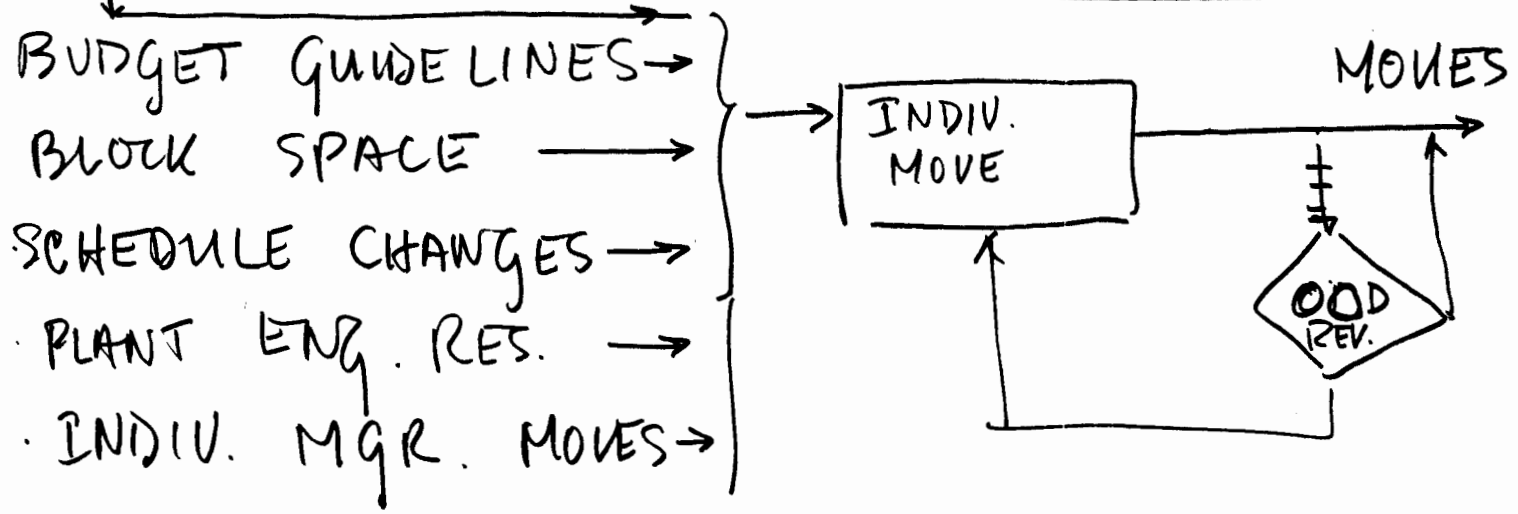


TACTICAL MOVES

Phase		Semi Annual Approval
0	PRE-PLAN	2p. Plan ⟶ OOD ⟶ PL/MC Info.
1	DESIGN	ϕ1 Bus. Plan → PSG (opinion) ⟶ OOD ⟶ PL/MC Info.
2	PROTO BLD/ DEBUG.	ϕ2 Bus/MFG. Plan → PSG (OPINION) ⟶ OOD (INFO) ⟶ M/E Appr. →
3	PROD. ST.- UP	PRICE PR. ⟶ PLM/MC Approve.
4	SUPPORT	· Prod. Mgr. Changes ⟶ OOD (INFO) → PLM/MC Approve

PRODUCT PLAN / Approval Process.

2/28/76.

SB.

OOD (Cent. Eng.).

GB--- Museum. Fy 77.

--- Pecuniary, Place, Prod. K.
20 / 1M (PL). EDP Support, Library

-- Personnel (M.A.) + Education
20 /

--- LSI + Sim. & Elect. Mems. (HL)
/ 1.6M / 1.78M - Worcester. / 2.1M

--- Comm.
25 / 1.3M.

--- Terminals, Disk, Tape, PS,
13/14 - 77
Eng. Svc., CAB.

--- HDw. Systems
150 (INC. VAX) / 128.

--- SOFTWARE
1,000 / 32.75M - 77

Real time
(IEM client

---- 10 Eng.

digital

INTEROFFICE MEMORANDUM

TO: Gordon Bell

DATE: May 4, 1976
FROM: Bill Thompson
DEPT: Corporate Planning
EXT: 3779
LOC/MAIL STOP: ML 12-1 F/41

MAY 4 1976

SUBJ: MY NOTES ON KEN'S REQUEST FOR THE WOODS

The stated objective of the Woods discussion with the OOD is: How decisions are made. The request has been that you lead the discussion with Larry, Bob and Dick giving you the necessary support. The format suggested was that you discuss inputs taken, how they are used, and how basic decisions are made within the group.

We used words like: casual, simple, and spontaneous as a method of approach. The stated goal is to clarify the process in the OOD's mind first and then, as a by-product, to do so with others.

After we have completed a discussion on how decisions are made, we will then progress to a discussion on the Systems Proposal that Dick would have outlined in advance for review. The final subject of the day will be a culmination of the Red Book process. I believe it has gone to the point where most issues have been totally resolved or at least discussed to the point that they are becoming ho-hum. We should have the following three objectives in the Woods:

(a) OOD's modifications to the Red Book strategies based upon the inputs they have heard.

(b) An agreement amongst the group as to what portions of the strategy really require further work over the next six months.

(c) A discussion on how effective the Red Book process has been and what modifications the Operations Committee or the Marketing Committee would like to see the next time around.

/a Org. —
Process — RB
Sys. mgmt

Teach (Explain what dev is really like.
.. .. .. proces is

- Groups of decisions
- How do we measure

G. Bell

digital INTEROFFICE MEMORANDUM

TO: Operations Committee

DATE: April 27, 1976

FROM: Bill Thompson

DEPT: Corporate Planning

EXT: 3779 LOC: ML 12-1 F/41

APR 28 1976

SUBJ: MAY WOODS

It has been decided that we will meet for an Operations Committee Woods on both May 10 and May 11. The meeting will be held in Pete Kaufmann's conference room. The subjects as currently outlined are:

MONDAY: This day will pretty much be set aside as an old fashioned Woods to discuss broader issues and strategies of where you are going. The only two issues that have been tentatively identified are:

(a) What will be happening to your job over the next five years, and how do you expect to change to meet it?

(b) A review of the decision making within OOD. The three key members of the OOD and Gordon have been asked to explain how they make decisions within their group.

TUESDAY: The Tuesday morning session will start off with a presentation and discussion by Coopers and Lybrand who have been invited by Al Bertocchi to give you their inputs gathered as a result of a meeting with the corporation as a consultant rather than as an auditor.

The second item to be discussed is the conclusions on the Red Book strategies. You have identified issues, and the OOD will present their conclusions to your issues.

A more complete agenda will be published momentarily.

/a Bill / Ken

We've just reviewed this at OOD & don't believe it's too useful to present. Our decision making is carefully patterned to be just like the Operations Committee.

Gordon.

digital

INTEROFFICE MEMORANDUM

TO: Bill Thompson ML12-1/F41

cc Bell / Clayton
Partner

DATE: April 26, 1976
FROM: Ken Olsen
DEPT: Administration
EXT: 2300
LOC/MAIL STOP: ML12-1/A50

SUBJ: DECISION MAKING IN OOD

At the next Woods Meeting, I would like to have the three key members of OOD and Gordon Bell explain to us how decision making is accomplished in OOD. Who is responsible for space, salary reviews, personnel, and for all the decision making technically and, in general, the organization chart of the group.

/ma

cc: Gordon
Bob
Dick
Harry

I will schedule this for some time on May 10th will confirm exact time shortly

CB
4-26

APR 28 1976

Seems to me that the answer is really very simple. "It's done just like the Operations Committee."

Bob Puffer

- Organisation
- In/Out.
- Process

2 hrs.
- System Mgmt.

- Redbook pr.
  +
  . RB Process Critique

- Explain what dev. is really like.
- " Dev. process that are invisible.

→ Teach... them
⇒ who's running admin? [ ]

How do we measure products ??

→ Groups of decisions: ~~How do~~

Administration

⇒ Kinds
- Space
- Product.
- SDC
- Edu
- Personnel.

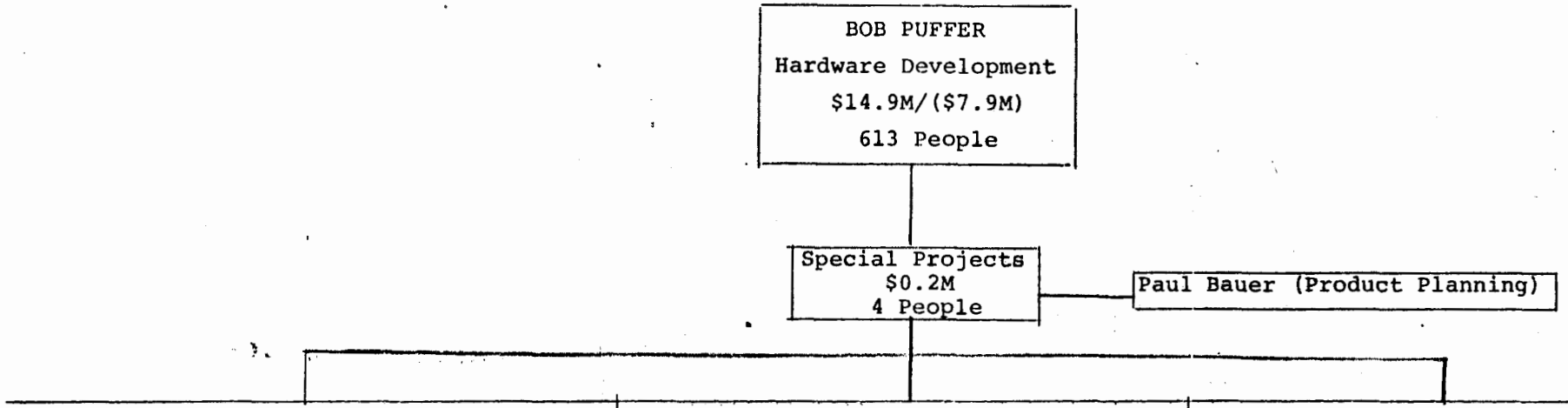
→ Interrupt vs Clocked !

GB 10 Feb. 76

What / Who	Spec. Problems	additional PL input	Other Instructions ——— ≡ new direction
	Low end strategy!		whether Q-bus, VAX-11 phasing & VM
11 Cent.	serial Bus, UM? RAS, mProcessor Soft. support	SYSTEMNESS; VAX prob Q vs 11/34 mP ← multi-drop, RJE, IOP vs Front end	Fund spec. LSI. PAX & VM Need (esp. to end) (commercial ISP) Arch. Plan non-exist. Modem understanding, Front end, multidrop, cabling, character handling.
11- Comm.			
Core	} Profit margin decline		} Phaseover? Battery backup.
Semi			CCD and other electronic M's... to reduce cost, get uniqueness
Simulation	Users must!	none.	Need profit goals.
LSI Eng		none	Need profit goals. Get $ from projects
LSI Worc.		none	Need profit goals.
11 Soft	Profit! VM?	SYSTEMNESS, multidrop	RAS; mP; Database; lookout PL/1. Applic. Technology.
Stds.	~~Not competitive in Bits/$ for each~~	Compatibility	coding; Language use; 11 → VAX (Assmbly)
~~Soft~~. Tech	Charge for Users! Poor Service!	—	Tools & measures. Hdware support system. SDC Factory!
Disk	Not competitive! Need better PM	Biggest problem.	R&D outside of Disks | Second disk group! Priority: RK06, RSL, Backups, RK08
Printers	LA120	multidrop, Letter	get front end tech + arch, else we track!
Display	LA Follow on	↓ 600+LPM perfect Print	} Integrate. Stds, technology,
Tape.	Poor profit	Stan's residue	NO Architecture! Need plan.
	~~Best~~ Poor Perform.	Reliability, NOT Profit matters	Buy out reliable products; Hold on ~~their~~ product till idea comes
Diag.		—	Who they?
Admin.	Tech. staff to overlook/check	—	Need procedures/process to go down. Space; Product check; Profit PUSH
Misc	—	—	Magic charts | AUTOMATE OOD.
Des. Auto.		—	Hold tite
Spec. Proj.		—	Hires needed!
P/S		Improve	Critical. Should Buy out more.
R & D	PL/1 on back burner	—	Backup on mem. RAS, multi Pc; Data Base; Applic.
Pkg.		Improve	Busses, Arch., VM. Real Turf issues! Sell services!
UL CSA		—	more Emphasis + integration
Components		—	Be helpful, not hassle

gB 10 Feb 76

what / who	# Products growth	2nd Src	Profit	Product Mgmt	Project Mgmt
11-Central	=↑ serial	=	C+-B-	µ-B, lo-A, Mid B, High A VAX-B-	µ-C+, lo-A+, Mid-D+, Hi A VAX-A-
11-Comm. (INCL. F.E.)	=↑ Modem	=↑	B+	B-	B-
Core	↓	↓	A	A	B+
Semi	=↑	↓	B	A	B-
Simulation	↑			C	A-
LSI-Eng.	↑		D+	C	C+
LSI-Worc.					
11-Soft	↑	↑	↑D+	RT-B, M-B+, D-C-, IAS-D RSTS B+	RT-A, M-A, D-C+, I AS-B+ ~~IAS~~ RSTS B+
$tds	↑				B+-A-
Soft. Tech.	↑				C-
Dich	=↑	↑	A-	05 C-, 06-C-, RP-A- RSL-B	05 C-, 06 B-, 08 D, RP A RSL-B+
Printers	↑	=↑	C+	A Future C+	A Future B-/
Display	↑	=↑	C	5x B+, copier, 61-C	5x B+, copier C-, 61 C+
Tape	=↑	↓	B+	Floppy A, Tapes C	Floppy A, Tape D
Diagnostic					? ⇒ C
Admin	↑				C
Misc					-
Des. Autom.	=				C
Spec. Proj.	↑				C-
P/S.	=↓				C
R+D	↑				A-
Pkg.	↓				B-
UL CSA	↑				B-
Components	=				C+



DISK ENGINEERING
Grant Såviers, Mgr.
$6.6M - 81 People

Paul Badum	RSL Eng. & Product Mgmt.
Steve Orr	RK06/07 Product Mgmt.
Kevin Smith	RPR02/03/04/05/06 RS03/04 Product Mgmt.
Keshava Srivastava	Support Engineering RK05 Product Mgmt.
Phil Arnold	RK06 Engineering
Bob Jack	RK07 Engineering
Demetrios Lignos	RSL Control, RK611, RP05/06, MBA's
Mike Riggle	Technology/Advanced Product Development
Bob Rottmayer	Components Eng.

TAPE ENGINEERING
Bob Peyton, Mgr.
$2.0M - 37 People

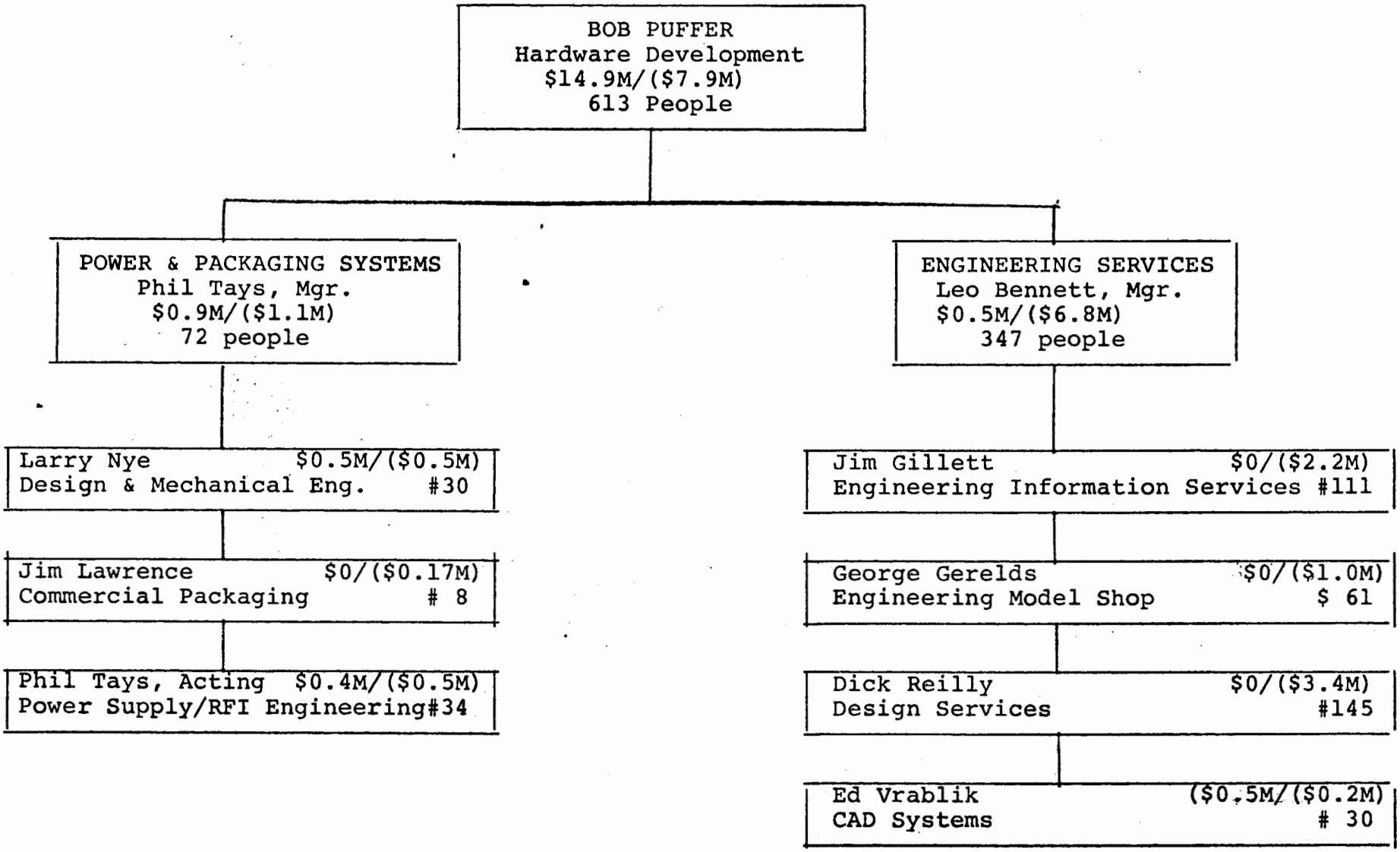
Chet Ju	Small Tape Product Mgmt.
Ed Siegmann	Large Tape Product Mgmt.
Heinz Findeisen	Small Tape Engineering
John Hess	Large Tape Engineering
Bill Smith	Engineering Support
Chuck Youse	Floppy Disk

TERMINALS ENGINEERING
Ed Corell, Mgr.
$4.7M - 72 People

Alan Dziejma	Terminals Product Mgmt.
Ken Fine	Architecture
Abe Gershnow	LA00 Engineering
Mike Leis	VT/DK Engineering
Tom Stockebrand	Support Engineering
Art Williams	Printer/Copier/ LA120 Engineering

Code: $-Direct/Indirect - FY77 Budget
#-No. of people as of May 1, 1976

R. W. Puffer
5-6-76



Code: $-Direct/Indirect - FY77 Budget
#-No.of people as of May 1, 1976

R. W. Puffer
5-6-76

Proposed Criteria For Evaluating Project Proposals and Business Plans

TECHNICAL

Produce price performance improvement of about two is required to justify a significant engineering expenditure,

I.e., the proposed product is at least 50% cheaper or twice the performance of existing products.

General purpose use across many markets.

MARKETING

Realistic commitment from Marketing groups of the volume they plan to sell.

FINANCIAL

20% profit before tax to net revenue and 20% after tax return on assets.

FORMAT

Existence of a one page summary.

Internally consistent and complete document.

Understandable by a person not well versed in your field.

Phil Laut
2/21/74
/ale

Explanation of product Financial Statements

The purpose of this document is to describe in detail, the financial statements that are used to measure the profit and loss of major products,

Scope

The financial statements measure all revenue and expense related to a product, Those classes of expense (selling and G&A) that are not accountable by product are omitted,

Description of Line Numbers

Line #	Name	Description
1	Bookings	# units booked into the order processing system in Maynard during the fiscal period, (Net of cancellations,)
2	Shipments	# units shipped and billed to customers from the U,S, or from Ireland, Shipments to sales subsidiaries are counted as sales when the subsidiary is invoiced,
5	Bookings	Dollar value of Line 1 in thousands of dollars,
6	Sales at List Price	Product of units shipped times list price in thousands of dollars,
7	Discounts	Amount allowed off list price due to system discounts,
8	Allowances	Amount allowed off list price due to special deals, (Discounts and allowances may be budgeted together,)
9	Net Sales	Line 6 less Line 7 less Line 8,

Description of Line Numbers (continued)

Line #	Name	Description
13	Manufacturing Cost	Actual direct cost of manufacture. For hardware products, it is the manufacturing costs incurred in volume production. The cost of Final Assembly and Test at the system level is not included. This is equivalent to Pink Book cost. For software products, it is the direct cost of the media and documentation that the customer receives.
11	Manufacturing Start-up Cost	For hardware products only. This is the cost incurred by manufacturing to get a new product into production.
12	Warranty Cost	For hardware products only. This is the cost of Field Service during the first three months after delivery. It is charged based on Field Service hours at the rate of $22,50 per hour.
15	Gross Margin	Line 9 less Line 10 less Line 11 less Line 12.

Description of Line Numbers (continued)

Line #	Name	Description
16	Engineering Expense	Expense of product design and implementation taken from discrete project reports.
17	Software Support Expense	For software products only. Related to the time spent by Software Support for all Product Support as well as training. Does not include pre-sales software support.
20	Other Expense (describe)	Spare.
25	product Contribution to G&A, selling, marketing expenses and profit	Line 15 less Line 16 less Line 17 less Line 20.
26	Percent Contribution to Net Sales	25 divided by 9.
28	Direct Capital Equipment	Dollar value of capital equipment required that is directly attributable to the product.

Phil Laut
1/8/75
/ale

Approximate discounts and allowances by Product Line as a percent of Gross Sales:

OEM	31%
OEM 11/05	31%
OEM 11/35	31%
OEM 11/45	22%
Sub-total OEM	28%
Components	35%
LDP-Biomedical	7%
Industrial	9%
Education	4%
Engineering Computation	3%
PDP-15	4%
Typeset	10%
Communications	12%
Business	7%
DECsystem-10	10%
Software Services	--
Other	--
TOTAL	13%

Phil Laut
1/8/75
/ale

D I G I T A L INTEROFFICE MEMORANDUM -->TED JOHNSON

SUBJ: COMMITTEE ENGINEERING

DATE: 30-Mar-76
FROM: GORDON BELL
EX: 2236
MS: ML12/A51

To: Andy Knowles
CC: Marketing Committee, Ken Olsen

Re question of Committee Engineering:

Committee Engineering is generally bad and it frustrates me, a former designer, probably worse than anyone else. Our sheer size and need to communicate with market groups, mfg., F.S., software support etc. does something to reinforce that the individual doesn't matter or have the ultimate responsibility too often.

This style almost came down from group work of Eckert, Mauchley, von Neuman, Burks, Goldstine for the first computer--and much subsequent work has been "team" oriented due to large number of disciplines. None of those guys could build a machine alone!

There are many pieces of our Engineering: some parts are too committee oriented, I can give views piece-by-piece. The "grading" I gave to Marketing Committee for funds this year tended to reflect fads--and "success". Overall I believe in the 1 or 2 individuals who are at the design center of a product as the dominant drive. When it gets too many "designers" it's bad...and nothing comes out (or only slowly). When it gets a bad designer(s) in its midst things are also bad. In a draft choice, I'll trade 1 (great) designer (we have maybe 10 in company) for many average ones, their associated managers and overhead structures that are relatively easy to come by, but are harder to get something from...and "look like" a committee.

I'm willing (and mean) to "represent" engineering with a decision when there's a hassle. My frustration with committee marketing is not being able to get a stable decision! you versus Stan versus Ted versus Jim. I'd like to talk with someone who can be serious about and speak for "Marketing" when the key strategy and detailed tactical questions are decided. It frustrates me by not being able to work substance versus superficial organizational (territorial) issues that usually can't be resolved.

GB:mjf

Gordon

I don't think I believe this is inherently a committee problem today. It seems to me the instability is just as much on the dev. side. Discuss? Ted

MAY 6 1976

C O M P A N Y C O N F I D E N T I A L

Product Business Plan
Financial Section
(000s)

Product:
Product Manager:
Date:

Line #			Actual Q1	Plan Q2	Q3	Q4	FY75	Q1	Q2	Q3	Q4	FY76	FY77	FY78	FY79	FY80
1	U	Bookings														
2	U	Shipments														
5	$	Bookings														
6	$	Sales at List Price														
7	$	Discounts														
9	$	Net Sales														
10	$	Mfg. Cost														
11	$	Manufacturing Start-up Cost														
12	$	Warranty Cost														
15	$	Gross Margin														
16	$	Engrg. Expense														
17	$	SW Supp Expense														
20	$	Other Expense (describe)														
25	$	Product Contribution to S&A, selling and mktng expenses and profit,														
25		% Contribution to Net Sales														
26	$	Direct Capital Equipment														
		Design Start(ed):														
		Shipments Start(ed):														

Description of Product:

List Price: $
Manufacturing Cost: $
Warranty Cost Per Unit $
Software Support Per Unit: $

Phil Laut, 1/8/79

C O M P A N Y C O N F I D E N T I A L

Sales and Shipment Forecasts

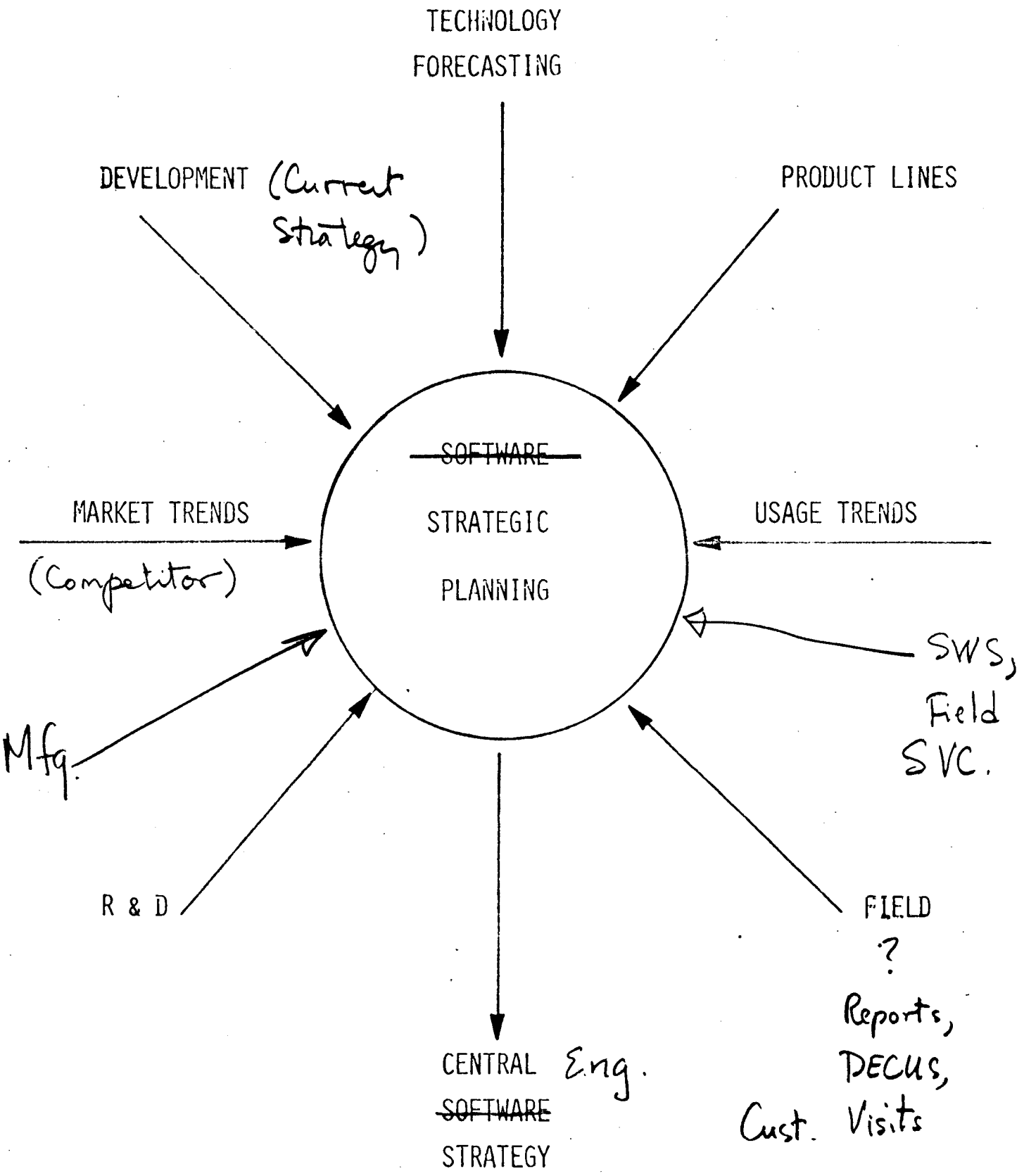
Product Line	<-----FY75-----> Q1	Q2	Q3	Q4	FY75	<-----FY76-----> Q1	Q2	Q3	Q4	FY76	FY77	FY78	FY79	FY80
OEM-P														
# Units Shipped														
Gross Dollars														
Discounts and Allowances %														
Net Sales														
OEM 11/03 Small 11														
# Units Shipped														
Gross Dollars														
Discounts & Allowances %														
Net Sales														
OEM 11/35 Med. 11														
# Units Shipped														
Gross Dollars														
Discounts & Allowances %														
Net Sales														
OEM 11/45 Large 11														
# Units Shipped														
Gross Dollars														
Discounts & Allowances %														
Net Sales														
Sub-total OEM														

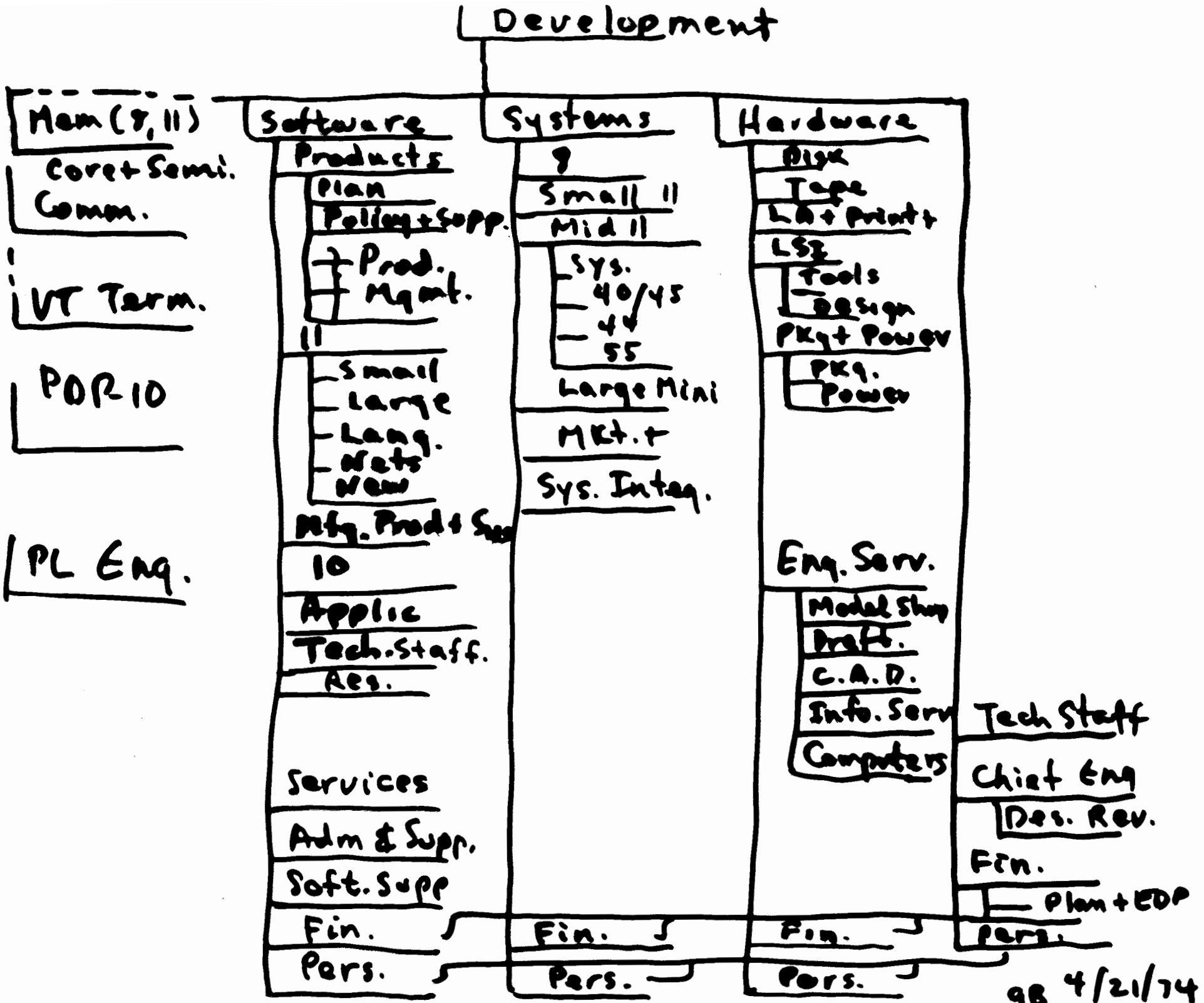
Product Line	<-----FY75-----> Q1	Q2	Q3	Q4	FY75	<-----FY76-----> Q1	Q2	Q3	Q4	FY76	FY77	FY78	FY79	FY80
Components														
# Units Shipped														
Gross Dollars														
Discounts & Allowances %														
Net Sales														
LDP-Biomedical														
# Units Shipped														
Gross Dollars														
Discounts & Allowances %														
Net Sales														
Industrial														
# Units Shipped														
Gross Dollars														
Discounts & Allowances														
Net Sales														
Education														
# Units Shipped														
Gross Dollars														
Discounts & Allowances %														
Net Sales														

Product Line	FY75 Q1	FY75 Q2	FY75 Q3	FY75 Q4	FY75	FY76 Q1	FY76 Q2	FY76 Q3	FY76 Q4	FY76	FY77	FY78	FY79	FY80
Eng, Computation														
# Units Shipped														
Gross Dollars														
Discounts & Allowances %														
Net Sales														
PDP-15														
# Units Shipped														
Gross Dollars														
Discounts & Allowances														
Net Sales														
Typeset														
# Units Shipped														
Gross Dollars														
Discounts & Allowances %														
Net Sales														
Communications														
# Units Shipped														
Gross Dollars														
Discounts & Allowances %														
Net Sales														

Product Line	FY75 Q1	FY75 Q2	FY75 Q3	FY75 Q4	FY75	FY76 Q1	FY76 Q2	FY76 Q3	FY76 Q4	FY76	FY77	FY78	FY79	FY80
Telco														
# Units Shipped														
Gross Dollars														
Discounts & Allowances %														
Net Sales														
Business														
# Units Shipped														
Gross Dollars														
Discounts & Allowances %														
Net Sales														
DECsystem-10														
# Units Shipped														
Gross Dollars														
Discounts & Allowances %														
Net Sales														
Software Services														
# Units Shipped														
Gross Dollars														
Discounts & Allowances %														
Net Sales														

Product Line	<FY75 Q1	Q2	Q3	Q4	FY75>	<FY76 Q1	Q2	Q3	Q4	FY76>	FY77	FY78	FY79	FY80
other														
# Units Shipped														
Gross Dollars														
Discounts & Allowances %														
Net Sales														
TOTAL														


TECHNOLOGY
FORECASTING
DEVELOPMENT (Current Strategy)
PRODUCT LINES
~~SOFTWARE~~
STRATEGIC
PLANNING
MARKET TRENDS
(Competitor)
USAGE TRENDS
SWS, Field SVC.
Mfg.
R & D
FIELD
?
Reports, DECUS, Cust. Visits
CENTRAL Eng.
~~SOFTWARE~~
STRATEGY


Development
Mem (8, 11)
Core + Semi.
Comm.
VT Term.
PDP 10
PL Eng.
Software
Products
Plan
Policy + Supp.
Prod. Mgmt.
11
Small
Large
Lang. + Sets
New
Mfg. Prod + Sup
10
Applic
Tech. Staff.
Res.
Services
Adm & Supp.
Soft. Supp
Fin.
Pers.
Systems
9
Small 11
Mid 11
Sys. 40/45
44
55
Large Mini
Mkt. +
Sys. Integ.
Fin.
Pers.
Hardware
Disk
Tape
Lab + Print +
LSI
Tools
Design
Pkg + Power
Pkg. Design
Power
Eng. Serv.
Model Shop
Drafts.
C.A.D.
Info. Serv
Computers
Tech Staff
Chief Eng
Des. Rev.
Fin.
Plan + EDP
Pers.
Fin.
Pers.
9B 4/21/74

OOD. Organizational Direction

- - - PEOPLE

PECUNIARY CONTROL, PLACE, PRODUCTS SUMMARY, PROCESS TOOLS (E.G. PERT)

TECHNICAL STAFF--ARCHITECTURE?, STANDARDS, PATENTS AND TECHNOLOGY PURCHASE ≈ 6 + (R+D)?

- - - SEMICONDUCTORS AND ELECTRONIC MEMORIES (DESIGN & MFG.)

MANUFACTURING INTERFACE

- ELECTROMECHANICAL MEMORIES
- UNIT RECORD DEVICES
- PACKAGING AND POWER
- ENGINEERING SERVICES

} INCLUDES---SOFTWARE SUPPORT AND MEMORY SUB-SYSTEMS

LEVEL OF INTEGRATION ↓

SMALL SYSTEMS AND TERMINALS

- LA
- VT
- GRAPHICS
- PACKAGED SYSTEMS

} INCLUDES---SOFTWARE SUPPORT

CPU'S — INTERFACE TO COMM.
INTERFACE TO FS

SOFTWARE---INTERFACE TO SWS

P/L INTERFACE (APPLICATIONS) ---10/15---SHOULD THIS BE TO CPU SYSTEMS?

- CSS
- COMMERCIAL GROUPS
- REAL TIME PRODUCT LINES--IPG & LDP
- COMPUTATION

9=7+2---

GB
11/75

INTER-GROUP INTERFACES

0. GENERAL TECHNIQUES

   PEOPLE ROTATION

   USE CONTROLS ($)

   COUPLE VIA MATRIX TO OTHER ORGANIZATION

   SEGMENT BUSINESS TO DECOUPLE ENGINEERING (I.E. DECENTRALIZE --COUPLE ENGINEERING TO A "DIVISION")

   PHYSICAL LOCATION

1. MANUFACTURING

   HOW DO WE SUPPORT DEFOCUSED FACTORIES?

   MOVEMENT OF PEOPLE TO SUPPORT AND/OR DESIGN AT THE FACTORY IN COMMODITY (I.E. TECHNOLOGY)-ORIENTED AREAS (E.G. DISKS, TAPE, DUMB TERMINALS, MEMORY)
   MUST CO-HABIT WITH MFG.ENG. (TEST ENG.; PROCESS ENG., ETC.)

2. PRODUCT/LINE

   HOW DO DESIGNERS HAVE UNDERSTANDING OF USE? (ROTATION AND P/L TASKS)

   CHARTS

   MUST MATRIX WHERE COMMUNICATION IS POOR!

   WILL BECOME A JUNGLE WITH "50 PRODUCT LINES"
   NEED CLOSER LIAISON WITH P/L ENGINEERING

3. FIELD SERVICE

   QUALITY ADV. DEVELOPMENT

   RAISE

   JOINT BUY-IN MATRIX

4. SOFTWARE SUPPORT (SEE F/S)

5. CSS $\Rightarrow$ MATRIX

   USE AS EARLY WARNING AND ADV. DEVELOPMENT GROUP.

6. EUROPE AND CANADIAN PRODUCTS!

GB 11/6/75

ID#0302

digital interoffice memorandum

Subject: **Basic Corporate Product Development Strategy**

To: OOD, OOD Direct Reports,
Corporate Meeting Attendees

Date: 18 OCT 78
From: Gordon Bell
Dept: OOD
Loc: ML12-1/A51 Ext: 223-2236

follow up 11/1/78

The attached slides were presented at the corporate meeting on October 13, reflecting our main product direction. These support what the Operations Committee has decreed to be our key product development goal:

> Provide a compatible set of VAX and 11 distributed computing products so a user can compute (in a transparent fashion) in any of the following styles and sizes without reprogramming (or extra work):
>
> . As a single user within terminal
>
> . Small, local shared system for a group
>
> . Large system serving several groups

As you can see the theme is:

> . Simplicity (of base hardware and software architecture)
>
> . Distributed processing like no other vendor now, or is likely to provide (especially IBM)
>
> . Terminals for everyone, with compatible computers placed appropriate to the task or organization

Any comments?

GB:ljp

Attachments

BELL (ATT/BELL LAB) GROUP BUILDING PBX'S

AS A CUSTOMER PUT IT ON WEDNESDAY:

- "ONLY YOU HAVE THE BASIC ARCHITECTURE IN VAX TO COVER THE RANGE WE NEED FOR DISTRIBUTED PROCESSING. WHY DON'T YOU BUILD IT?

- GIVE US A IRULY COMPATIBLE RANGE OF VAX MACHINES.
  DON'T CORRUPT IT (LIKE YOU DID ON THE 11). WE WANT A RANGE OF MACHINES:

  - 10 X IBM 3033
  - CURRENT 780
  - VAX-ON-A-CHIP (FOR TERMINAL USE)

- SW BASE >> HARDWARE BASE (CPU'S ARE 4% OF COST)

- WE MUST HAVE RELIABLE, SECURE COMPUTERS FOR SYSTEMS WE INTEND TO BUILD."

- THEY'LL FUND US TO WORK ON NEBULA AND THE VAX CHIP!

DUPONT HAS THE SAME REQUIREMENTS

THIS IS WHERE WE'RE HEADED!

GB
ID#25

Why we must have only One Architecture

1. It's the only way to build the type of Distributed Processing System described in the Goal. By having identical systems everywhere, we avoid all interface disparities, conversion, and getting different results. A user can compute (statically or dynamically assigned) in any location with no re-compile, changes, etc.
2. Reduce Design, Manufacturing and field costs — (we can save $ or invest in applications)

   A 10% learning curve means:
   10% less cost for 2 × the volume; or
   10% more cost for 2 identical products.
   (More products probably don't generate incremental NOR)
3. Aside from IBM, the more successful, high growth companies have a single architecture. (DG; Prime and even HP to some extent) versus. (Burroughs, CDC, Univac, Honeywell — although they do have 1 now!)
4. IBM is vulnerable and can't get to Dist. Proc. as I believe users want & need it. I.e. they have 360/370, new 8100, 32/34, Series 1, S 3...15, S 7, 5100/5110, and will need a computer in a terminal. I don't think even they are big enough to co-ordinate / use all these!

Why base strategy on VAX?

1. Designed it for a very wide range of implementations → 1000:1
   (We could go 10~20× bigger than the 780 w/o changes)
2. Architecture
   - 32-bits of addressing ⇒ # of objects an instruction can access = 4 gigabytes
   - Small page size to fit in terminal-type applications and very small (μ-level) systems → the ideal personal Computer!
   - good encoding - twice better than (and Tops 20) 370, while having big addresses
     - × for squeezing into small system.
     - × for high perf., less bits to move around from disk ↔ main memory.

     (implies 2× cost, or 3 years of memory cost reduction at 20%/year to get same cost.)
   - Data-types for encoding & power.
   - 8-bit bytes → IBM said so in 1964.
   - Builds on 11 user base & allows 11 implementations at low end in a phase-over.
   - Builds off 11 Demand Curve (versus lower 10/20

STRATEGY FOR PRODUCTS (81-82)

- A MINIMUM OF HARDWARE AND SOFTWARE VAX AND 11 SYSTEMS WITH: APPROPRIATE SIZE/AND COMPATIBILITY PRICED DISKS.
- PHASING OVER TO A VAX-ONLY STRATEGY BY 1985, OR WHEN APPROPRIATE
- STAYING BELOW $250K SELLING PRICE (IN ORDER TO KEEP MACHINES AND BUYING WITH THE USE).

BASE HARDWARE

LEVEL OF MACHINE	VAX	11
CENTRAL	780 -> SUPERSTAR* (AT 200K LEVEL)	(NOTE COMPETES WITH LEN HUGHES' SEI SEL ECL MACHINE)
GROUP	COMET/HYDRA	11/74; 11/74 MP -> 0 (USE COMET)
SMALL GROUP	NEBULA*	11/44 -> FONZ REPLACEMENT
PERSONAL	LSI-VAX*	FONZ
EMBEDDED CONTROL		TINY

*NOT DOING AGRESSIVELY NOW!

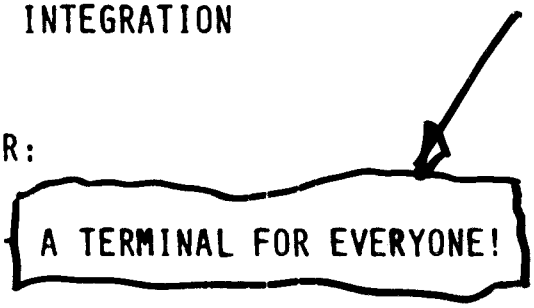
GB
ID#21

BASE HARDWARE OPTIONS

- MODERN, MULTI-DROP, HIGH-SPEED COMMUNICATIONS FOR '80S INTERCONNECTING:
  - TERMINALS, PERIPHERALS (E.G. LINE PRINTER) AND SMALL-SYSTEMS

    PERMITS DROP-SHIP AND CUSTOMER INTEGRATION

- TERMINALS WITH SOFTWARE SUPPORT FOR:
  - DUMB, BLOCK MODE AND LOW COST
  - OFFICE
    - LETTER/HIGH QUALITY PRINT (WITH GRAPHIX/FAX) FOR ELECTRONIC MAIL
    - PAGE CRT FOR WORD PROCESSING (STAN), AND
  - ANALYST (LENG) - GRAPHIX CALCULATOR/WORD PROCESSOR
    - THE MODERN (VECTOR, MATRIX, TABULAR) CALCULATOR AND DISPLAY
  - FACTORY ENVIRONMENT
    - COMPATIBLE AND LOW COST TERMINALS
    - DISTRIBUTED PROCESSING TO PROCESS INTERFACE



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ID#23

BASE SOFTWARE

- LESS 11 ENHANCEMENTS (I.E. DECREASING OR SUSTAINING FUNDS)

  IAS, RSTS, HI-END RT; USE M, SCS, TRAX AS BASE FOR COMPATIBILITY WITH VAX. THAT IS, PROGRAMS MUST BE ABLE TO MIGRATE FROM 11'S TO VAX!

- LAYERED, MODULAR O/S FOR SPECIFIC APPLICATIONS (COMMON PROGRAM INTERFACE; COMMON UTILITIES AND LANGUAGES; COMMON DRIVERS)

  - VMS - GP BASE; ADD BATCH
  - TIMESHARING
  - TRAX-32 FOR TRANSACTION PROCESSING
  - TUNED REAL TIME
  - BASIC+ WITH EXPORT/IMPORT AND RSTS INTERFACE, FACILITIES AND UTILITIES - AT CURRENT PERFORMANCE LEVEL - PROTECT USER PROGRAMS. THIS IS OUR BIGGEST USER BASE.
  - FILE, DISTRIBUTED DATA BASE AND NETWORK TO SUPPORT DISTRIBUTED PROCESSING GIVING ABILITY TO COMPUTE/STORE IN ANY NODE.

- Must be concerned with TRAX, I&S, SCS, M+ & VMS migration.

GB
ID#22

D I G I T A L INTEROFFICE MEMORANDUM

DIST:

Annette Albright	TW/E16	Ted Baker	MR1-2/E78
Paul Bauer	ML3-3/B91	Dick Becker	ML1-3/E58
Gordon Bell	ML12-1/A51	Jim Bell	ML3-2/E41
Leo Bennett	ML4-4/E99	Ron Bingham	MR1-2/E85
Peter Christy	ML12-3/A62	Dick Clayton	ML12-2/E71
Brian Croxon	TW/C04	Jim Cudmore	ML1-5/E30
Bill Demmer	TW/D19	Michel Depeyrot	ML3-3/B91
Mike Donnelly	ML3-3/E54	Ulf Fagerquist	MR1-2/E78
Ed Fauvre	MK-2/E6	Lorrin Gale	TW/D19
Bill Green	ML1-4/B34	Mike Gutman	ML21-2/E32
Bill Heffner	TW/C10	Steve Heiser	MR1-2/E37
Per Hjerppe	MR1-2/E78	George Hoff	MR1-2/E47
Bill Howerton	ML12-3/A62	Bob Hranek	ML1-5/B98
Bob Jack	ML1-3/E58	Bill Johnson	ML21-3/E87
Justin Kelleher	ML12-3/A62	Bill Kelly	ML3-6/E95
John Kevill	ML1-3/E58	Oleh Kostetsky	ML5-5/E39
Mitchell Kur	ML12-2/A16	Bernie Lacroute	TW/A08
Richard Leslie	MR1-2/E78	Tomas Lofgren	MR1-2/E89
Jim Marshall	TW/A03	Ed McDonough	MO-2
John Meyer	ML12-1/A11	John Miville	MR1-2/E78
Gene Mondani	ML1-5/E30	Ken Nisbet	TW/D19
Stan Pearson	ML12-2/E38	George Plowman	ML5-5/E97
Larry Portner	ML12-3/A62	Bob Puffer	ML12-2/E38
Larry Rasile	ML12-2/E71	Mike Riggle	ML4-1/B32
John Rose	ML12-3/A62	Geoff Sackman	ML1-4/A97
Frank Sanjana	ML12-2/E71	John Sartory	ML4-4/E99
Grant Saviers	CZ	Dick Snyder	MR1-2/E37
Joe St. Amour	ML1-5/E29	Steve Sur	MR1-1/A43
Phil Tays	ML11-4/E53	Mike Tomasic	ML12-2/E71
Pete van Roekens	TW/E07	Jane Ward	ML12-3/A62
George Wood	AC/E44		
Steve Coleman	PK3-1/M28	Pierre-Yves Tiberghien	GE
Ken Olsen	ML12-1/A50	Win Hindle	ML5-2/A53
Bill Long	ML5-2/A53	Helmuth Coqui	ML12-1/F41
Al Bertocchi	PK3-2/A56	George Chamberlain	MS/B80
Al Crawford	PK3-2/F34	Ed Finn	MS/B87
John Fisher	PK3-2/A93	Joe Gaffney	MR2-L/A89
Al Mullin	PK3-2/F40	Ed Schwartz	MS/F17

DIST: Continued

	Shel Davis	PK3-1/C21	Romney Biddulph	PK3-1/C21
	Barry Burns	PK3-1/C18	Ron LeBleu	PK3-1
	George Rossi	PK3-1/C16	John Sims	ML1--5/B15
	Geraldine Weathers	ML1-5/B15	Ted Johnson	PK3-2/A55
	Dennis Bjork	PK3-2/Pole 3B	Bruno Durr	PK3-2/S56
	Gene Gross	PK3-2/A55	Carl Janzen	AK
	Gerry Moore	PK3-2/A66	Jack Shields	PK3-2/A58
Jean-Claude	Peterschmitt	GE	Geoff Shingles	GE
	Bobby Choonavala	GE	Dick Pascal	PK3-2/A66
	Bill Steul	GE		
	Andy Knowles	ML5-2/A53	Gus Ashton	PK3-2/M18
	Dick Berube	PK3-2/M18	John Leng	MR1-1/A65
	Larry Bornstein	ML5-2/A53	Si Lyle	MR1-1/M42
	Ward MacKenzie	PK3-1/A60	Al Pilon	MR1-1/A65
	Jim Pitts	PK3-1/M51	Joel Schwartz	MR2-4/M51
	Harvey Weiss	MR1-1/M85	Jerry Witmore	PK3-1/M40
	Julius Marcus	MK1-2/C37	Roger Cady	MK1-1
	Jack Clifford	MK1-2/F35	Bob Hughes	MK
	Irwin Jacobs	MK1-2/H32	Harvey Jones	ML1-4/A98
	Bill Kiesewetter	MR1-1/M81	Clem Lamarre	MK1-2/F35
	Charlie Spector	ML5-2/M17		
	Stan Olsen	MK1-2	John Alexanderson	NQ
	Jack Gilmore	MK1-1/J14	John Holman	PK3-1/P84
	Ed Kramer	MR2-4/A67	Pat Kress	MK1-2/E33
	Bob Lane	MK1-2/B11	Les Strauss	MR2-2/F21
	Jack Smith	ML1-4/F31	Henry Crouse	ML1-5/B98
	Bill Hanson	ML1-4/P11	Dave Knoll	ML1-4/P14
	Bill Thompson	ML12-1/F41	Sheldon Aronoff	ML12-1/F41
	Joe Fargano	ML1-4/P11	Dan Infante	ML1-4/F31
	Mitch Kur	ML12-2/A16		

digital

INTEROFFICE MEMORANDUM

TO: DISTRIBUTION

DATE: 14 JUNE 78
FROM: Stanton Pearson
DEPT: Eng. Strategic Planning
EXT: 3-2424
LOC/MAIL STOP: ML12-2/E38

SUBJ: SPRING 78 PRODUCT/MARKET LONG RANGE PLANS (RED BOOK I)

This is your copy of the Spring 78 Red Book I, which describes the strategic product development plans for Central Engineering for FY79-81.

These plans have been developed by the six product/market POTS, which have been formed to couple market needs and technology. They allocate $45.6 million in FY79 engineering cost (which is over half of the Central Engineering budget and about one-third of Digital's total engineering investment). The plans and funding will be reviewed and approved by the Engineering Board of Directors (EBOD), a subcommittee of the Marketing Committee with representation from product lines and Central Engineering chaired by Andy Knowles.

RECOMMENDATIONS

Based on analysis of the plans, Engineering Strategic Planning makes the following recommendations to the Engineering Board of Directors:

1. Market Requirements

   A. Further definition of the degree of compatibility required between various DEC operating systems to meet market requirements should be provided by the applications POTS.

   B. Further definition of the degree of Communications & Network functionality and performance between various DEC operating systems should be provided by the application POTS.

2. Funding Expectations

   Product development funding expectations for FY80 and 81 should be developed during Q1,FY79 by EBOD and the POTS.

3. Tools To Aid The Investment Tradeoff Process

   A. The capability to project and track the revenue related to a product or Product/Market segment should be developed for use as a metric in comparing alternative uses of product development funds.

B. We should invest in a model to evaluate the impact of various product development efforts on system performance for use as a metric in comparing alternative uses of product development funds.

4. Systems I/O Strategy

The product development strategy for systems I/O should be reviewed during Q1,FY79 by EBOD. This includes systems bus strategy, intelligent sub-system strategy (NDS) and software I/O architecture strategy.

Interfaces

Central Engineering Operational Plans (Beige Books) for each line organization describe the tactical plans for implementing specific products described in the Product/Market strategies.

If you have further questions, please call:

Overall:	S. Pearson	(3-2424)
	D. Quimby	(3-6743)
Commercial Applications:	E. Fauvre	(264-5622)
	G. Reyer	(264-5974)
Real Time/Computation:	B. Heffner	(247-2091)
	J. Mileski	(247-2172)
Base Systems:	B. Demmer	(247-2112)
	F. Sanjana	(3-3150)
Small Systems & Terminals:	D. Clayton	(3-4353)
	A. Dziejma	(3-5156)
Networks/Communications:	G. Plowman	(3-3329)
	C. Stein	(3-7941)
Storage Systems:	G. Saviers	(3-4520)
	K. Sills	(3-5805)

NOTE:

Hydra is not included in this document.

Hydra (32 bit Multiprocessing project) is currently budgeted at $4M for FY79.

The FY79 requirements for Hydra are being developed between TELCO and Central Engineering for presentation to EBOD in July.

I N T E R O F F I C E M E M O R A N D U M

TO: DISTRIBUTION

DATE: 14 JUNE 78
FROM: Stanton Pearson
DEPT: Strategic Planning
EXT: 3-2424
LOC/MAIL STOP: ML12-2/E38

SUBJ: SPRING 78 PRODUCT/MARKET LONG RANGE PLANS (RED BOOK I)

This is your copy of the Spring 78 Red Book I, which describes the strategic product development plans for Central Engineering for FY79-81.

These plans have been developed by six product/market groups called POTs, which have been formed to couple market needs and technology capability in product planning. They allocate $45.6 million in FY79 engineering cost, over half of the Central Engineering budget and about one-third of Digital's total engineering investment. The plans and funding will be reviewed and approved by the Engineering Board of Directors (EBOD), a subcommittee of the Marketing Committee with representation from product lines and Central Engineering chaired by Andy Knowles.

Recommendations

Based on analysis of the plans, Strategic Planning makes the following recommendations.

1. Further definition of the degree of compatibility required to meet market requirements should be provided by the application POTs.

2. Product development funding expectations for FY8Ø and FY81 should be developed over the next two quarters by EBOD.

3. The capability to project and track the revenue received directly from a product, and other incremental revenue attributable to the product, should be developed to act as a metric in comparing alternative uses of product development investment.

4. Strategic Planning's observations and concerns, in the Summary section, are presented so that EBOD can consider taking action or delegating the task of inretigating and formulating a recommendation.

Interfaces

Central Engineering Operational Plans (Beige Books) for each line organization describe the tactical plans for implementing specific products described in the Product/Market strategies.

If you have further questions, please call:

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	C. Stein	(3-7941)
Storage Systems:	G. Saviers	(3-4520)
	K. Sills	(3-5805)

SPRING '78 PRODUCT/MARKET LONG RANGE PLAN

(RED BOOK I)

Contents

TU70, 800/1600 BPI, 200 IPS tape drive

TU72, 1600/6250 BPI, 125 IPS tape drive

TU77, 800/600 BPI, 125 IPS tape drive, FCS Q2/FY79

TU78, 1600/6250 BPI, 125 IPS tape drive, FCS FY81

UDA, UNIBUS Disk Adapter (Small NDS), FCS FY82

UNIBUS, PDP-11 standard bus

UNIFONZ, Fonz-based 11/04 replacement system

VAX, 32-bit processor family, including 11/780 (STAR), 11/780 MP, COMET, NEBULA, LSI/VAX, and SUPERSTAR

VMS, virtual management system software for VAX family

VT52, current video terminal

VT61, VT62, soft copy smart terminals for specific markets/applications

VT100, soft copy terminal successor to VT52

Winchester, integrated head/disk technology

X.25, communication transport mechanism standard

I. Summary

[redacted]

INTRODUCTION

This year's Red Book reflects the formation of six POT groups to couple market needs and technology capabilities in product development plans for the following Product/Market segments:

- Commerical Applications
- Real Time/Computation Systems
- Base Systems
- Network Software and Communications Hardware
- Small Systems and Terminals
- Storage Systems

Each POT is steered by a team of about 12 people, with the intent to have balanced representation from product lines and Central Engineering.

The six POT strategic plans for FY79-81 are included in Sections II-VII.

Section I is a management overview of the POT plans, including highlights of the individual POT plans, strategy elements common to several POTs, major products planned for development, analysis of investment and POT revenue expectations, progress on issues identified in the Spring 77 Red Book, and Strategic Planning's observations and concerns.

Section VIII includes as background information a glossary for the other seven sections and a full Product Calendar, which will be used as the baseline for Yellow Books during FY79.

POT PRODUCT STRATEGY DOMAINS

Each POT is responsible for developing the product strategy and approving the funds allocation for development in a different section of the product/market space. Following is a brief description of these domains. For a more detailed description of products in development see the product calendar in Section VIII.

Commercial Applications

- Operating System: RSTS/E
- Programming Languages: BASIC Plus 2, COBOL, DIBOL
- File/data base management software: RMS, DBMS
- Commercial pre-configured system products: Small Commercial System (SCS)
- Transaction processing: TRAX
- Commercial applications tools and software utilities important to the commercial market

Real Time/Computation Systems (RT/C)

- Operating systems: RT-11, IAS, RSX-11M, M+(MP), and S
- Programming languages: FORTRAN, DOD standard language, BASIC-11, MACRO, APL
- Real time applications tools and software utilities important to the real time/computation market

Base Systems

- PDP-11 UNIBUS processors and pre-configured system products
- VAX processors and pre-configured system products
- Main memories, power and packaging for the above
- UNIBUS and MASSBUS
- Operating system kernels from which several operating systems can be developed (application-independent system resource allocation capability) for PDP-11 and VAX processors
- Multiprocessing

Terminals and Small Systems (T/SS)

- PDP-11 QBUS processors and pre-configured system products
- Main memory, power and packaging for the above
- QBUS
- Hard copy terminals and line printers
- Soft copy (video) terminals
- Intelligent terminals

Network Software and Communications Hardware (N/C)

- DECnet and protocol emulators for non-DEC equipment
- Communications hardware: interfaces, modems
- Communications protocols

Storage Systems

- Floppy disks
- Small, medium, large rigid disks
- Small, medium, large tapes
- Intelligent subsystems for mass storage devices
- Mass storage subsystem handlers and drivers
- Mass storage device diagnostics

SUMMARY OF POT STRATEGIES

This section contains Strategic Planning's summary of the POT strategies, based on the POT Long Range Plans and discussions with POT representatives. For additional information or more detail, please refer to the individual POT plan.

Base Systems

Extend the VAX CPU family down in cost as fast as resources permit, with 11/780 functionality as the CPU standard.

Maintain the competitiveness of the PDP-11 CPU family in the short run by improving mid to high-end COBOL performance and protecting midrange exposure to limited physical address space.

Maintain long-term PDP-11 competiveness with improved price/performance products, setting essentially 11/74 functionality as the PDP-11 CPU standard.

Respond to market requirement for improved availability with PDP-11/74 MP as earliest entry. Continue development of VAX-11/780 MP for high availability where applications are not predictable for effective segmentation, and establish a task force to recommend a system topology for continuous operation where applications are predictably segmented.

Use 16K MOS RAM chips in main memory, and make error checking and correcting (ECC) memory available on all CPUs. Track 64K MOS RAM chip development.

Focus on compatibility of software, external busses, and architecture to preserve cumulative user and DEC investment. Force adherence to the K2 (PDP-11) and VMS (VAX) kernels to avoid operating system proliferation.

Increase focus on systems through Corporate Packaged Systems, and by designing and manufacturing to lead in selected configurations.

Evolve longer-term to a corporate UNIBUS replacement to correct increasing competitive exposure to interconnect functionality, performance, cost and data integrity as a major artery of the business.

Commercial Applications

Develop a broad spectrum of commercial products, using 32-bit processors for mid to high end and 16-bit processors for low end.

Target industry leadership in transaction processing through TRAX and in small commercial systems through SCS-11.

Maintain competitiveness of mid to high end PDP-11 products while developing the 32-bit mid-to-high end product line.

Move toward supplying a more complete solution to end-user problems by shifting our investments away from systems-level tools, such as operating systems, and towards applications-oriented tools such as data base management systems.

Networks/Communications

Develop the communication functionality of each operating system to a uniform base level, selectively enhancing some with additional functionality as defined by market requirements.

Design toward user transparency to transport level (inter-node) line protocol differences among DEC (NSP, DDCMP), IBM (SNA), and common carriers (X.25).

Shift focus from intercomputer communications to intercomputer data management.

Use one standard protocol for all communication interconnect capability to minimize required number of products, maintaining flexibility for foreign machine connection through use of writable control store microcode in intelligent line interface boards.

Real Time/Computation

Maintain leadership in a DEC traditional market with a large cumulative investment in software by enhancing FORTRAN and file utilities and improving reliability and ease of use. Create a 16-bit distributed real time system model and tools.

Lay the foundation for evolution to 32 bits, phasing over as market demand shifts from 16 bits. Develop 32-bit real time and host support for network systems.

Prevent specification lock-out by implementing a real-time language (DOD-1, Pascal, PL/1).

Test the multiprocessing market with the 11/70 MP.

Storage Systems

Develop intelligent subsystems (NDS and Small NDS) to improve availability, data integrity functionality and configurability of storage subsystems, differentiate DEC products and reverse proliferation of device controllers for all classes of disk and tape.

In mid and high range storage subsystems, combine fixed disks (for capacity, cost, and reliability) with removable disks and tapes (for interchange, data backup, software distribution, and personal storage).

In low end subsystems offer removable floppy or rigid disks.

Improve competitiveness of medium disks, which are projected to produce more revenue than other disk classes, by investing in new disk technology introduced by IBM in high-end products, and migrating the technology to medium disks fast enough to meet or beat competition.

Compete in high end disks through intelligent subsystems, early buyout and/or manufacturing license, or early reverse engineering to manufacture an equivalent product. Evolve toward building high-end disks as resources permit.

Build rigid and floppy low-end disks; pursue AZTEC rigid low-end disk development and track floppy disk technology development.

Provide industry standard compatible tapes through 6250 BPI group code recording (GCR) technology.

Review the use of price as a strategic alternative to accelerated new product development, due to cost of engineering development, value on timeliness of product introduction, and relatively short product life at introduction price.

Terminals and Small Systems

Capture a higher percentage of terminal ports shipped on DEC systems for DEC terminals. Protect and grow independent base terminal business.

Enter the intelligent terminal business. Protect low end and enhance mid to high end total systems through use of intelligent terminals.

Focus on general purpose base and intelligent terminals, leaving application-specific terminals for product line engineering.

Supply T-11 and F-11 chip sets for DEC internal use, and T-11 and F-11 boards and boxes for external sale.

Reduce transfer cost through emphasis on dock-mergeable or drop-shippable products.

COMMON STRATEGY ELEMENTS

Each POT's strategy is its response to its particular product/market space. Five elements seem to have broader significance, since they appear in one form or another in several POT plans.

Compatibility

Four POT plans show some emphasis on product compatibility. Base Systems calls for fixed architecture and hardware functionality, adherence to use of operating system kernels, and compatibility of software and external busses.

Commercial Applications' strategy is based on a spectrum of compatible products and compatibility for migration of existing customers to new products. In Network/Communications, common base level communication functionality, complete line interconnect capability derived from a standard protocol, and transparency to the communication carrier system all drive toward compatibility. Storage Systems will move toward compatible mass storage interfacing with intelligent subsystems.

Availability

Availability as a goal, or mechanisms to improve system availability, appear in all POT plans. Base Systems' approach is through multiprocessing and ECC memory capability. Commercial Applications stresses the need for availability in transaction processing systems, as well as low support cost for their area as a whole.

Network diagnostics and maintainability are included in the Network/Communication plan. Real Time/Computation addresses reliability and ease of use, and Terminals and Small Systems includes reliability and cost of support among its key leverage factors. Storage Systems' intelligent subsystems will increase data integrity and improve diagnostic capability.

Protecting and Fine-tuning

Five POTs refer to protecting or fine-tuning existing products. Both Base and Commercial state the need for protecting PDP-11 processors, and Base also proposes evolving to a long-term UNIBUS replacement. RT/C will maintain market leadership through existing product enhancements. Storage Systems intends to review strategic pricing of its products. Terminals and Small Systems mentions protecting its base terminals and low end systems business.

Breadth

A broad range of products is not explicitly mentioned in all POT plans, but seems to be a strategy element in five. Commercial's first market goal is to maintain a broad spectrum of products from $5K to $300K. Base Systems' processors are planned to cover the range between Small Systems and Large Computers. Small Systems and Terminals is expanding its range of processors and terminals, and adding intelligent terminals.

Storage Systems' strategy provides for a full range of disk and tape products. Network/Communications' intention is to develop a range of capability from straightforward communication to intercomputer data management.

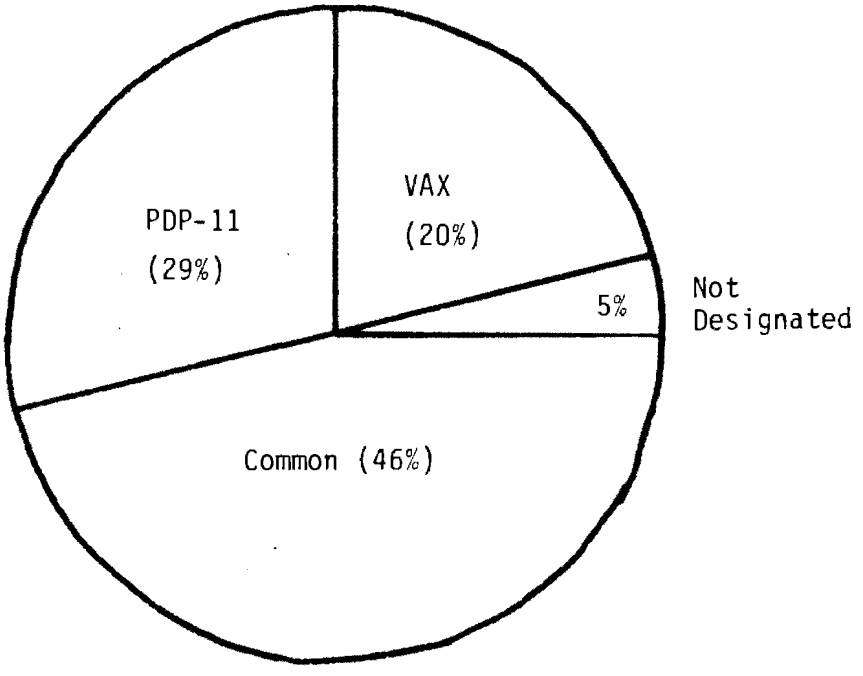
New Thrusts

The product plans of five POTs include significant new product thrusts. Base Systems is moving toward multiprocessing products, and calls for central development of new memory technologies. Commercial is developing the Small Commercial System. Network/Communications intends to move its program focus to intercomputer data management. Storage Systems is pursuing the AZTEC low-end rigid disk and intelligent mass storage subsystems. Small Systems and Terminals is entering the intelligent terminal market.

SUMMARY PRODUCT CALENDAR

On the following page are twenty-six products, each over $500K in FY79 development cost, that represent 70% of total FY79 Central Engineering product development. The remaining 30% supports an additional 45+ products.

Products specific to the PDP-11 family account for 29% of FY79 development, while VAX family products are 20%. Common products such as peripherals and DECnet will use 40% of FY79 product development, and 50% is not designated at this time.



Distribution of FY79 Central Engineering
Product Development Investment ($45.6M total)

TOP 26 POT PRODUCTS

FY79 Engineering Development Cost over $500K

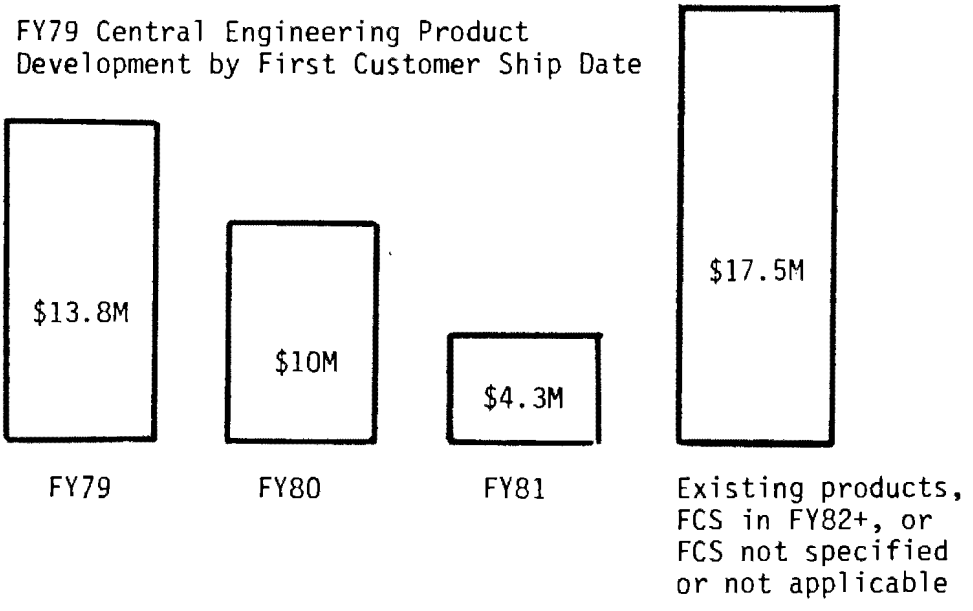
		FCS Date	FY79 Cost ($K)	POT
PDP-11 Family				
FONZ	Higher performance LSI-11 chip set successor	12/78	1,975	T/SS
Small Commercial Systems	Small business systems software package for lower cost and entry in COBOL market (includes small COBOL and ADE-1)	Q1,FY80	1,257	Commercial
11/74, 74MP	Corp. cabinet 11/70 with commercial instruction set and multiprocessing extensibility	Q3/FY79	1,450	Base
11/44	11/34 processor plus commercial instruction set, physical address extension	Q4/FY79	1,200	Base
K2 Kernel	Operating system kernel for mid to high-end PDP-11s	n/a	1,050	Base
TRAX	Dedicated transaction processing system (V1 FCS 7/78)	Q4/FY79 (V2,T)	858	Commercial
11/68	Lower-cost 11/74 replacement	Q4/FY80	850	Base
Tiny-11	Lower cost LSI-II successor	on hold	750	T/SS
Unifonz	Fonz-based 11/04 CPU replacement	Q1/FY80(t)	500	Base
Other PDP-11	(17 products)		3,405	
TOTAL PDP-11 FAMILY			13,295	
VAX FAMILY				
Comet	Midrange VAX CPU: two-thirds 11/780 performance at one-third 11/780 cost	Q1/FY80	3,200	Base
VMS Kernel	Operating system kernel for VAX family	n/a	1,700	Base
11/780, 780 MP	High end VAX CPU: twice 11/780 performance in native mode (11/780 shipped 12/77)	n/c	1,550	Base
COBOL-79	High performance native mode compiler	FY81	598	Commercial
Other VAX	(10+ products)		2,148	
TOTAL VAX FAMILY			9,196	
Common				
R80	143 MB fixed disk drive	FY80	2,870	Storage
DECnet	Advanced network functionality	n/a	2,700	N/C
50MB Removable	Low cost RK07 (cartridge disk) replacement	FY81	1,435	Storage
LA00	Low cost 300 baud hard copy terminal	11/78	1,400	T/SS
RL01/02	5/10 MB cartridge disk drive and controller (RL01 shipped 12/77)	Q4/FY79 (RL02)	1,135	Storage
IT-100	Intelligent Terminal Family	n/c	990	T/SS
NDS	Intelligent subsystem for disks and tapes	FY81	920	Storage
LA120 & Options	1200 baud hard copy terminal	9/78	900	T/SS
TU77/78	Large tape (125 IPS, 1600/6250 BPI), family	Q4/FY79 (TU78)	763	Storage
RP07/07+/08	Large (292-542 MB) fixed disk	Q3/FY79 (RP07) FY80 (RP07+/08)	675	Storage
RK07	Medium (28MB) cartridge disk	3/78	580	Storage
VT100	Display terminal successor to VT54	9/78	515	T/SS
TS04	Small tape (45 IPS, 800/1600 BPI)	FY79	514	
Other Common	(18+ products)		5,484	
TOTAL COMMON			20,881	
TOTAL 11, VAX, and COMMON			43,372	
Not designated			2,228	
TOTAL PRODUCT DEVELOPMENT			45,600	

FINANCIAL HIGHLIGHTS

The relationship between planned engineering investment and expected impact on future revenues should be a factor in evaluating product/market plans. However, as several POTs have based their revenue projections on the total revenue of systems sold with their products, the comparative analysis that can be done is limited.

The four charts on the next two pages show the Central Engineering budget for FY78, the current planned budget for FY79, and trial solutions for the budget in FY80 and FY81. The trial solutions are offered as a reference point for POT planning, and may be changed as POT plans and priorities vary. POTs are shown as six categories under Product Development, with the POT budgets distributed among Central Engineering line managers by the POTs.

The total FY79 POTs budget of $45.6M will begin to produce revenue as shown in the following illustration of cost by product first customer ship date:



About 30% of FY79 product development supports products with FY79 FCS, 22% is for products to ship in FY80, and 9% for products with FCS in FY81. The relatively short-range emphasis of these product plans is complemented by Advanced Development ($7.1M), Research ($1.8M), and Development Tools ($8.3M) which have a longer-range payoff.

Functional Line Mgr. / ENG. ACTIVITY	CLAYTON	DEMMER	KEVILL	CUDMORE	MARCUS	PORTNER	PUFFER	BELL	UNALLOC.	FY78 TOTAL
Product Dev.										
Comm'l						4815				4815
RT/C						659				659
Base Sys.		7437		700		1560				9697
Sm Sys & Term	7600		500	300	100					8500
Net Comm					1100	2060				3160
Storage			9600							9600
Sub Total	7600	7437	10100	1000	1200	9094				36431
Research				700				1328		2028
Adv. Dev.	1700	340	1800	1800	100	222				5962
Prod. Support	2544	1213	600	300	400	2587				7644
Prod. Mgt.	1211	502	400	100	79	849				3141
Adm.	240	324					4002			4565
Dev. Tools	1700	182		1000		1990	1430			6302
Sub Total	7395	2561	2800	3900	579	5648	5432	1328		29643
Unallocated									*1000	1000
Total FY78	14995	9998	12900	4900	1779	14742	5432	1328	1000	67074

* TEWKSBURY RESERVE

Functional Line Mgr. / ENG. ACTIVITY	CLAYTON	DEMMER	KEVILL	CUDMORE	MARCUS	PORTNER	PUFFER	BELL	UNALLOC.	FY79 TOTAL
Product Dev.										
Comm'l						6000				6000
RT/C						2100				2100
Base Sys.	1000	8150		400		2950			500	13000
Sm Sys & Term	7455		450	150		600			345	9000
Net Comm					800	2700				3500
Storage			11220	210		570				12000
Sub Total	8455	8150	11670	760	800	14920			845	45600
Research								1800		1800
Adv. Dev.	1040	725	2250	1400	100	600			*1000	7115
Prod. Support	3700	2075	525	500	500	3700				11000
Prod. Mgt.	1510	800	475	200	100	1100				4185
Adm.	200	165	150				5300			5815
Dev. Tools	2200	200		2100		2585	1200			8285
Sub Total	8650	3965	3400	4200	700	7985	6500	1800	1000	38200
Unallocated									1200	1200
Total FY79	17105	12115	15070	4960	1500	22905	6500	1800	3045	85000

*RESEARCH AND ADVANCED DEVELOPMENT RESERVE 4-18-78

Functional Line Mgr. / ENG. ACTIVITY	CLAYTON	DEMMER	KEVILL	CUDMORE	MARCUS	PORTNER	PUFFER	BELL	UNALLOC.	FY80 TOTAL
Product Dev.										
Comm'l										7.8
RT/C										2.6
Base Sys.										14.3
Sm Sys & Term										10.8
Net Comm										4.2
Storage										15.6
Sub Total										55.3
Research										1.3
Adv. Dev.									1.3*	9.9
Prod. Support										13.0
Prod. Mgt.										5.0
Adm.										6.9
Dev. Tools										9.6
Sub Total	10.3	4.6	4.2	5.0	0.9	9.5	7.8	2.1	1.3	45.7
Unallocated										5.0
Total FY80										106.0

* RAD

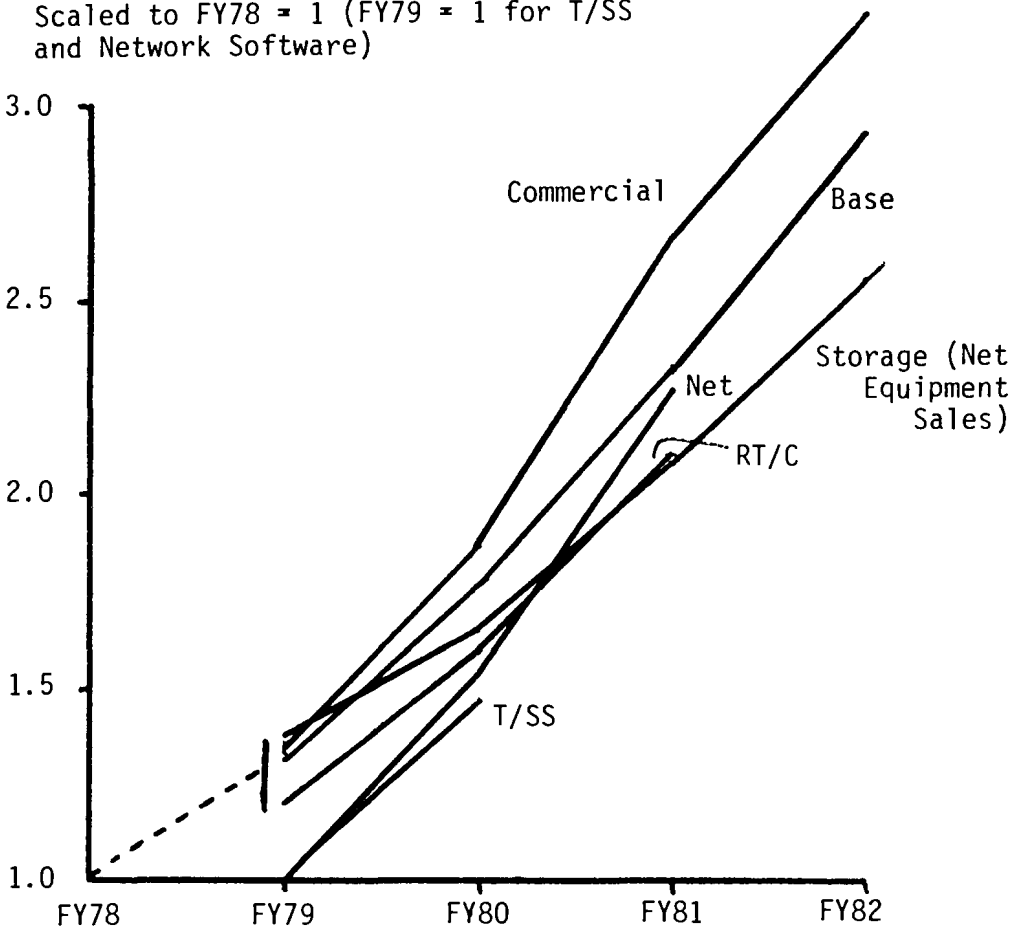
Functional Line Mgr. / ENG. ACTIVITY	CLAYTON	DEMMER	KEVILL	CUDMORE	MARCUS	PORTNER	PUFFER	BELL	UNALLOC.	FY81 TOTAL
Product Dev.										
Comm'l										10.1
RT/C										3.3
Base Sys.										16.6
Sm Sys & Term										13.5
Net Comm										5.0
Storage										20.0
Sub Total										68.5
Research										2.6
Adv. Dev.									1.7	11.6
Prod. Support										15.9
Prod. Mgt.										6.1
Adm.										8.5
Dev. Tools										11.8
Sub Total	12.6	5.8	5.4	6.3	1.2	11.7	9.2	2.6	1.7	56.5
Unallocated										7.0
Total FY81										132.0

* RAD

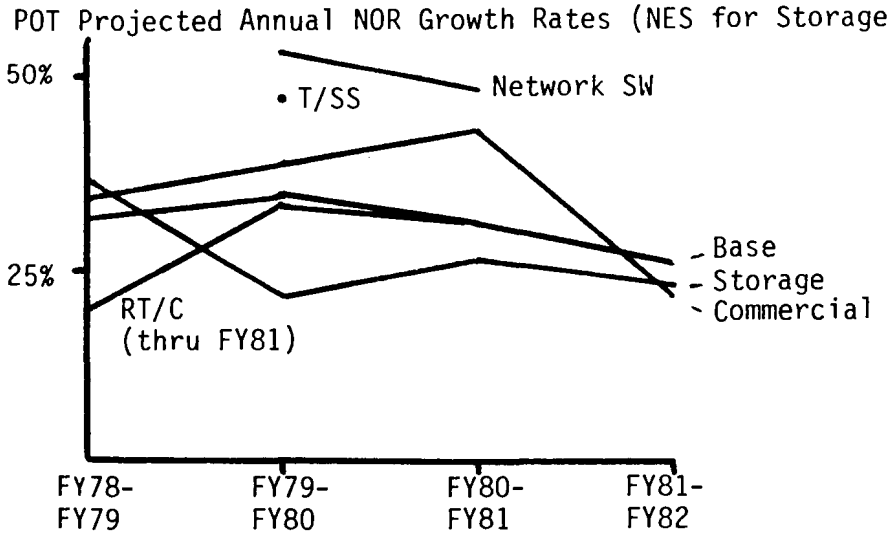
On the following page are two graphs representing POT revenue estimates. In the first graph, the revenues have been scaled to compare FY79-82 projections to FY78 estimates for each POT, to minimize the impact of accounting for revenue by systems (Network Software and Terminals and Small Systems is scaled to an FY79 baseline).

The second graph shows projected revenue growth as estimated by the POTs. Three of the FY78-FY79 grow rates are over 30%, while current corporate estimates are in the mid - 20's. In the FY79-FY81 time frame, T/SS, Network Software and Commercial estimate growth rates of 36 - 50+%, Base and RT/C estimate 30-35%, and Storage 20-25%.

POT Projected Net Operating Revenue
Scaled to FY78 = 1 (FY79 = 1 for T/SS
and Network Software)



POT Projected Annual NOR Growth Rates (NES for Storage)



OBSERVATIONS AND CONCERNS

Following are Strategic Planning's observations and concerns based on POT plans and discussions with POT representations and Central Engineering staff.

1. Product development funding for FY80 and FY81 is an issue in three plans. RT/C and Network Software/Communication Hardware feel that they will require funding in excess of the published trial solution. Storage Systems has analyzed their expected revenue growth and questions whether product development funding growth is adequate to support it.

   Realistic funding expectations will be a key input to long-range plans next year, as development opportunities will exceed available product development funds.

2. External bus strategies may require some clarification. Base Systems raises as an issue the stability of Small Systems and Terminals' decision not to implement a quad board QBUS FONZ processor as an important factor in deciding whether to implement UNIFONZ. Base Systems also proposes a long-term UNIBUS replacement, which would impact VAX and PDP-11 processors, including present QBUS machines.

3. The Base Systems POT plan shows a graph of processors in price versus performance and functionality space. The current and planned mid-to-high end processors (NEBULA, 11/68, COMET, 11/70, 11/74, 11/780) are closer to each other in this representation than has historically been the case.

   Commercial Applications' strategy is to sell mid-to-high end VAX systems and low-end PDP-11 systems, and Real Time/Computation intends to phase over to 32 bits as market demand shifts from 16 bits.

   Given the application POTs' strategies to shift to 32 bits, is the level of investment in the 11/68 the best use of product development funds?

4. Part of the Network Software and Communication Hardware POT strategy is to move toward intercomputer data management. The POT is investigating to avoid aggressively pursuing high end network capability at the expense of the low end, where competitive products and typical user entry level could leave DEC vulnerable to a competitive gap due, for instance, to reduced line efficiency caused by line protocols.

5. Revenue growth projections for POT plans range as high as 50% per year, compared to a corporate projection in the mid - 20's.

6. Several 16 and 32 bit multiprocessing products are included in the Red Book. The HYDRA 32 bit multiprocessing project is currently funded by Telco and is not included in POT plans. A corporate group may be needed to coordinate multiprocessing development for high availability or performance on 16 and 32 bit processors.

7. Given technology trends to increasing circuit and power density, are power and packaging receiving due attention?

8. Real Time/Computation, due to funding constraints and the absence of any specific requirements, assumes that other POTs' planned products (DECnet, DBMS, RMS, commercial languages) will not require changes to RT/C's operating systems. Other POTs should review their requirements and funding alternatives.

9. Development of products using CCD and bubble memory has appeared in previous plans, but appears this year only in Storage Systems' NDS. Are CCD and bubble technologies being pursued?

II. Commercial

digital

INTEROFFICE MEMORANDUM

TO: Stan Pearson

DATE: 23 MAY 1978
FROM: Glenn Reyer
DEPT: Commercial Engineering Plannin
EXT: 45974
LOC/MAIL STOP: MK1-2/D3

SUBJ: COMMERCIAL POT INFORMATION
FOR SPRING REDBOOK

INTRODUCTION

The POT has been concentrating primarily on finalizing an FY'79 budget to date. That budget is reflected in the Planning Calendar attached. The basis for the work of the POT during this period has been the Commercial Group System Plan prepared by the Commercial Product Lines last June. The emphasis of the POT at this point in time is to take that Plan and revise it to reflect a Corporate commercial strategy. Our intention is to complete this activity by the end of Q1 FY'79. The POT also recognizes its obligation to integrate this plan with that of LCG over a period of time.

MARKET GOALS

- Maintain a BROAD SPECTRUM of COMPATIBLE PRODUCTS as a key competitive strength for DIGITAL from $5K Intelligent Terminals through $300K Midi-Computers.

  Customers want to minimize application development costs and serve wide ranges of volume requirements. We will strengthen our competitive position by offering a family of 4-5 systems (1-128 users) that are upwardly compatible for application programs and files.

- Show a continuing COMMITMENT to CURRENT CUSTOMER BASE by maintaining product compatibility throughout its evolution where necessary by providing easily used migration tools to help customers move to newer products; and by maintaining support for older products. Our customers have a large investment in Application Software and Training. Show the customer that Digital is sensitive to his investment in our technology and that we will help protect that investment; if possible, by making new systems compatible - if not by making migration easy.

- Do not abandon our current General Purpose/Time-sharing Base, which has been a source of significant growth for Digital, as we move into newer markets such as Small Systems and Transaction Processing.

- Support the Corporation's Improved ROA Objectives through products engineered for lower Manufacturing, Sales and Support costs.

  Reduce the number of commercial systems offered to the above-mentioned families. Produce packaged systems that meet 80%-90% of customer requirements to reduce inventory and forecasting problems. Pre-tested configurations that work and have known performance should reduce warranty and A/R costs.

- Achieve a competitive position in Systems Performance for Commercial applications which is on a par with Digital's performance leadership in the Scientific/Computational area.

  Systems that are one half in performance relative to competition cost a lot to sell. We do not have to be the fastest in all areas but should target for ± 10% of competition unless there is no additional cost to get more.

- FOCUS on INDUSTRY LEADERSHIP in TRANSACTION PROCESSING through High Availability, Performance, Data Integrity and Security with a DISTRIBUTED PROCESSING approach. This is our chance to establish an image in the marketplace early when it is easy to do. We will also focus on SMALL COMMERCIAL SYSTEMS usable by the novice computer user.

The POT intends to continue to refine these goals particularly in the area of high availability, low end systems, uniqueness strategy, non goals, profitability, market share and service revenue goals.

COMMERCIAL POT DEVELOPMENT STRATEGY

In FY'79, follow a SURVIVAL Strategy in the mid-to-high-end 11 family in order to protect our mainstream business while we begin to build momentum in the 32-bit area (in both development and sales). This implie short-term, "hole-fill" oriented product development for 16-bit mid- and high-end products, and basic product development for the 32-bit area.

Simultaneously, in FY'79, ramp up our development efforts on commercial systems to replace CTS-300 and provide the basis for continued aggressive development and marketing of low-end commercial products in future years.

In FY'80, introduce our first cross-product commercial Small System, continue moderate level of effort in the 32-bit area; and maintain an aggressive sales posture on 16-bit mid-and high-end products while reducing investment by focusing on competitively targeted high-impact, low-cost enhancements to existing systems.

In FY'81, begin shift in emphasis to 32-bits for the mid- and high-end, focusing on solid migration capabilities, and begin winding down 16-bit development. Maintain aggressive development on low-end 16-bit products focusing on upwards and downwards compatibility. Ramp up our efforts on application tools across the board and begin to pursue an application software strategy especially at the low-end, as budget constraints allow.

Beyond FY'81, shift major Corporate-wide emphasis away from basic software development towards availability, application tools and applications. Concentrate on products and related sales tools which are geared to customer solutions, low sales and support costs.

Two major alternatives to this strategy have been investigated at various times. First, in June 1977 as part of the Commercial Group Systems Plan an alternative strategy to continue to enhance CTS-300 and RSTS as a general purpose commercial base was rejected as a long term strategy because of the general feeling that technologically these products did not have the expansion capability and flexibility that would be necessary in order to remain competitive in the three to five year period. More recently, the alternative of moving more aggressively to a 32-bit base for the mid-to high-end commercial systems was investigated by the Commercial POT and was rejected as a high risk technological alternative in light of the current business situation. The current strategy implies a gradual change in product emphasis over the next two to four years in the mid-to high-end product space from a 16-bit to a 32-bit base. The eventual goal as suggested by this strategy is to have a single compatible family of commercial products using 16-bit architecture at the low-end and 32-bit architecture at the mid-to high-end.

ASSUMPTIONS & IMPLICATIONS

MARKETS:

The Commercial POT has used a model segmenting markets into three generic application areas: General Purpose, Transaction Processing and Real Time/ Communications. The characteristic of these segments is described in the attachment titled "Commercial Market Segmentation". The POT intends to refine the segmentation and to analyze Digital's current position and future opportunities in each of these segments over the next few months, with concentration on the General Purpose and Transaction markets.

COMPETITION:

The POT believes that the major competitive influences within the next two years will come from IBM, HP and DG. The POT is also concerned with the impact that TANDEM is having in our markets. We expect to remain in "catch-up" mode relative to these companies for at least the next two years.

For the longer term, we must address the implications of satellite technology, the potential impact of the Japanese consortium threatening from above with "370 on a chip" technology, and the small companies, particularly micro manufacturers now developing systems capability, threatening from below. We will also watch Prime, Wang, Honeywell, Burroughs, NCR, CDC and UNIVAC for signs of threatening activity.

The majority of the POT activity relative to competitive analysis is yet to be done. We intend to perform the initial analysis on our major short-term competitors during the next few months.

TECHNOLOGY:

The POT has been operating on the implicit assumption that the completeness of our software tools and their performance will be the key priorities for the next two years. We are in "catch-up" mode in these areas in order to provide basic, entry-level capability for the Commercial Market. Beyond this two-year period, we are assuming that a stabilization of internal architectures and a shift in investment emphasis will enable us to concentrate on systems capability which is closer to the customer's solution, which is more approachable to a wider range of potential computer users, and which addresses internal efficiencies of manufacturing process, sales and support costs.

Specific long-term technological issues include:

- a commercial terminal strategy
- marketing and engineering strategies that help reduce manufacturing costs, especially at the low end
- systems salable, supportable and usable for the novice computer user
- storage technologies and their effect on the above
- communications technologies and their effect on the above
- whether the 32-bit architecture is a viable and cost effective architecture for the low end as an alternative to the current 16-bit low-end strategy.

REVENUE

The POT is currently collecting more accurate and detailed revenue data by the market segments defined. Current data available is based on Q1 FY'78 budgets and is attached under Commercial NOR forecasts.

INVESTMENT

Investment data is included with the Product Calendar attached. In general, the POT believes that the Commercial budget is so constrained as to provide NO flexibility in terms of exploring new opportunities in the low-end, 32-bit and applications areas. (Our FY'79 budget includes only a portion of our SURVIVAL items.) We have major exposures in terms of our ability to invest in commercially-oriented terminals, high-availability, 32-bit software, migration tools, application tools and commercial utilities.

RISKS and EXPOSURES

- Our ability to discipline ourselves to complete our basic systems tools in an expeditious fashion and shift our innovative energies away from basic computer architecture towards application tools and user solutions for the Commercial Market. Will the competition force us to invest in new architectures?

RISKS and EXPOSURES (con't)

- Our ability to market, sell and support Commercial systems competitively.

- The effects of Satellite Communications and 360/370 software availability on low-cost hardware on our mainline mini-computer business.

- The viability of low-end business from a Sales and support viewpoint. Resolution of the question of the long-term implications of indirect vs. direct distribution channels for small systems.

- Higher than expected investment to become viable and remain competitive in the Commercial market.

/kc

COMMERCIAL MARKET SEGMENTATION

	General Purpose	Transaction Processing	Real Time, Sensor Based Communication
Environment	o Multiple Independent Applications	o Optimized to Large No. of Terminals Doing Small No. of Jobs	o Fixed Functic o Communication
Oriented Toward	o Fast Program Development	o Production Environment (Response in Seconds)	o Performance (Response in Microseconds)
Use Wants	o Ease of Use	o Ease of System Modification o Sophisticated System Management	o To Get Close Hardware for Tunability o Building Bloc Approach
System Allocation	o Time Slice for Equal Resource Allocation	o Event Driven for Resource Allocation	o Event Driven for Resource Allocation
Control By	o User (Terminals Control System)	o System Controls Terminals	o System Controlled Production Environment
Will Pay For	o Average Security and Availability	o High Security and Availability	o High Security and Availability

COMMERCIAL NOR FORECASTS

BASED ON Q1 FY'78 BUDGET PASS

BUS, DDP, TELCO, IPG, OEM, G/A, W/P	78	79	80	81	82
32-BIT	2.7	28.5	95.4	265.7	483.6
LARGE-16 (11/60,11/70, 11/74)	165.3	190.2	217.3	229.8	147.4
MID-16 (11/34,11/44P,11/68)	203	272.6	333	374	281
SMALL-16 (11/03, FONZ, (Q,U, NO BUS)	56	75.7	134.5	243.3	430.7
SUBTOTAL	427	567	780.2	1112.8	1342.7
MDP/LDP (NO BREAKOUT)	19	32	48	72	100
TOTAL	446	599	828.2	1184.8	1442.7

PRODUCT FAMILY	PRODUCT NAME	DESCRIPTION	ANNC. DATE	FCS DATE	FY'78 $K	FY'79 $K	TOTAL $K	PROD. MGR.	DEV. MGR.
16-BIT MID+HIGH END	PDP-11 COBOL	ANSI-74 COMPLIANT COBOL V4A/V4B - PERFORMANCE RELEASES WITH PACKED DECIMAL DATA TYPE	Q2FY'79 (V4A/V4B)	Q2FY'79 Q3-V4B	142.6	183.9	326.5	PIETRAVALLE	HAM
	RMS-11	CROSS-SYSTEM COMPATIBLE SEQUENTIAL, RELATIVE, MULTIKEY ISAM FILE MANAGEMENT	Q2FY'79 (V1.5)	Q2FY'79	247.9	337.2	585.1	PIETRAVALLE	DALEY
	BASIC-PLUS 2	COMPILER SYSTEM FOR THE LANG. "BASIC", (DEC STANDARD)	JUNE '76	SEP'77	106.7	0	106.7	PIETRAVALLE	HAM
	FAST BACKUP	RP07 FAST BACKUP(1) UTILITY FOR RSTS/EV7A	N/A	RSTS/ EV7A		61.3	61.3	PIETRAVALLE	DALEY
	DBMS-11	CODASYL COMPLIANT DATA BASE MGMT.	FY'77	JAN'77	154.1	--	154.1	PIETRAVALLE	
16-BIT LOW END	SMALL COBOL	ANSI STANDARD COBOL FOR SCS-11	Q4 FY'79	Q1FY'80 (2)	216.9	275.9	492.8	PIETRAVALLE	HAM
32-BIT	COBOL-11/VAX	NATIVE EXECUTION OF	Q2FY'79	Q2FY'79	179.7	92	371.7	PIETRAVALLE	HAM
	RMS-32	COBOL-11 RMS-11 COMPATIBLE FILE MANAGEMENT FOR VAX	Q2FY'79 (ISAM)	Q3FY'79 (ISAM)	355.7	367.8	723.5	PIETRAVALLE	HAM
	SORT	HIGH PERFORMANCE FILE SORT FOR VAX	Q2FY'79	Q3FY'79	97.0	76.6	173.6	PIETRAVALLE	HAM
	BASIC+2 COMPILER	BASIC LANGUAGE COMPATIBLE WITH PDP-11 BASIC-PLUS-2	Q4 FY'79	Q1 FY'80	191.3 --	306.5	497.8	PIETRAVALLE	HAM
	COBOL-79	NATIVE HIGH PERFORMANCE COBOL FOR VAX	FY'81	FY'81	223.6	597.7	821.3	PIETRAVALLE	HAM
	DBMS-32	CODASYL COMPLIANT DATA BASE MGMT FOR VAX	FY'81	FY'81	--	183.9	183.9	PIETRAVALLE	
	EDITOR/VAX	DEC STD. EDITOR FOR VAX	N/A	VMS	--	30.7	30.7	PIETRAVALLE	HAM
	VAX/OTS	COMMON RUNTIME SUPPORT	N/A	N/A	241.9	183.9	425.8	PIETRAVALLE	HAM

PRODUCT FAMILY	PRODUCT NAME	DESCRIPTION	ANNC. DATE	FCS DATE	FY'78 $K	FY'79 $K	TOTAL	PROD. MGR.	DEV. MGR.
16 BIT MID+HIGH RANGE	DATATRIEVE-11	INQUIRY LANGUAGE/ REPORT WRITER FOR RMS-11K	OCT.'77	JAN'78	174.9	46	220.9	PIETRAVALLE	HAM
	CIS	SOFTWARE SUPPORT FOR PDP-11 COMMERCIAL INS. SET	N/A	N/A	206.8	--	206.8	PIETRAVALLE	HAM
	EDITOR	COMMON IMPLE. ON PDP-11 SYSTEMS & VAX COMPLIANT TO DEC EDITOR STD.	N/A	N/A	53	--	53.0	PIETRAVALLE	HAM
32 BIT	VAX TAPE ACP	ANSI TAPE SUPPORT FOR VMS V1.0	N/A	VMSV1	54.6	--	54.6	PIETRAVALLE	HAM
	VAX LDM R1A	CHECKOUT LANGUAGE & UTILITIES UNDER VAX COMPAT. MODE	N/A	VMSV1	24.6	--	24.6	PIETRAVALLE	HAM

PRODUCT FAMILY	PRODUCT NAME	DESCRIPTION	ANNC. DATE	FCS DATE	FY'78 $K	FY'79 $K	TOTAL $	PROD. MGR.	DEV. MGR.
16-BIT LOW END	SCS-11	SMALL BUSINESS SYSTEM SOFTWARE, CONSISTING OF PACKAGED RSX-11M BASED O/S (PRE-SYS-GENED) AND SMALL FILE MANAGER (UPWARDLY COMPATIBLE WITH RMS)	Q4FY'79	Q1FY'80 (2)	365	736	1101	WEBBER	MORGAN
	ADE-11	APPLICATIONS DEVELOPMENT FACILITY ORIENTED TO FIRST-TIME END-USER MARKETPLACE AS WELL AS IMPROVING PROGRAMMER PRODUCTIVITY BY DEC OEM'S/DISTRIBUTORS - BUNDLED WITH SCS-11	Q4FY'79	Q1FY'80 (2)	46	245	291	WEBBER	MORGAN
16-BIT MID & HIGH END	RSTS V7A	THIS RELEASE FEATURES SUPPORT OF LARGE FILE (OVER 65K BLOCKS), SHARED LIBRARIES (RMS), DISK CACHING, NEW DEVICE SUPPORTS AND CONTINUED AVAILABILITY OF SMALL (64KW) RSTS CONFIGURATIONS W/V6C FUNCTIONALITY	Q2FY'79	12/78	369	307	676	WEBBER	DALEY
	RSTS V6C		Q4FY'78	12/77	270	---	270	WEBBER	DALEY
	RSTS V7B	THIS RELEASE FEATURES IMPROVED SPOOLER, BACK-UP, AND BATCH FEATURES AND IMPROV. IN THE RSTS TASK BUILDER, AS WELL AS NEW DEVICE SUPPORT	----	----	---	199	199	WEBBER	DALEY

PRODUCT FAMILY	PRODUCT NAME	DESCRIPTION	ANNC. DATE	FCS DATE	FY'78 $K	FY'79 $K	TOTAL $	PROD. MGR.	DEV. MGR.
16-BIT MID TO HIGH END	TRAX	DEDICATED TRANSACTION PROCESSING SYSTEM	5-2-78	7-31-78	$818.5	858	1.676.5	JOHNSON	HAM
32-BIT	COMM. VAX (TRAX-32)	T.P. MONITOR FOR VMS TRAX INTERFACE BLOCK TERMINAL SUPPORT RSTS CONVERTER AIDS HUMAN ENGINEERING ENHANCEMENTS (3)	------	FY'81 (3)	54.6	305	359.6	JOHNSON	DALEY/ HAM
					4594	5193.4			

PRODUCT CALENDER NOTES

(1) Coordinational Issue with RT/C POT on Fast Backup/ Restore for RSX11M and TRAX to be worked.

(2) FCS for SCS-11, ADE-11, and Small COBOL are dependant on availability of CIS/FONZ system. Q-BUS vs. U-BUS implementation tradeoffs will affect this date.

(3) Preliminary planning data only.

III. Real Time/Computation

RT/C OVERVIEW

RT/C PRINCIPLES

Our market is mature and having been serviced by DEC since its inception implies that we have been a driving force. Our goals include maintaining that leadership position across a broad range of applications and directing our development efforts to accomplish that before moving into other areas such as specific applications.

We have 3 products: RT for single users, RSX for multi real time user environment and VMS for computation. We are investing in real time software for VMS such that, as the hardware evolves and migrates downward, we can introduce it as an effective RT/C product.

RT/C CONCERNS

The RT/C POT is concerned that due to the past investment made in RT/C products and the market maturity, that there may be a tendency to minimize the need for an aggressive development plan. Our perspective should be that of "bootstrapping" our efforts into new, critical products over the next few years which requires an aggressive plan and cannot use past investments as a leverage point. The key areas requiring a significant effort are:

a) 32-bit real time and host support for network systems. This requires effort much beyond our past 16-bit investments.

b) Pressure to maintain FORTRAN leadership; not by enhancing F4+, but by aggressively producing a mainframe FORTRAN.

c) Defining and creating a 16-bit distributed real-time system model and tools for continued revenue available from a large 16-bit market (i.e., LEVELØ DECNET).

d) An aggressive response to implementing a real-time language (DOD-1, Pascal, PL1) to prevent a lock-out from happening.

These key areas are under review for prioritization, however, we must point out that without the resources to implement a more aggressive RT/C development effort over the next 2-3 years, we will not only be in a position well behind the competition on 32-bit systems, but lack the current system enhancements needed to maintain viable PDP-11 offerings.

RT/C FY81 GOALS

A.

A. Maintain Leadership by enhancing Fortran and file utilities and establishing a stable environment across our 16-bit operating systems making them more reliable and easier to use.

We are testing the MP market with the 11/70 and laying the foundation for a major 32-bit thrust. We expect to respond in a timely manner to any DOD language specification as it will become a lockout specification.

B. Rejected Alternatives: We have currently excluded immediate development of new languages (PL1, BLISS, APL, DOD) due to funding limitations, however, we feel this creates a "hole" in the high end PDP-11 strategy and will require re-assessment and prioritization of FY80+ development funds.

C. Exposures: We are reviewing our long range strategy in the context of other POT's plans. The following issues will be worked and resolved.

.Need a model for "distribution" R/T which includes micro CPU's, DECnet, and distributed I/O.

.Mid-range system phase-over
(hardware: 11/70 - 11/68 -COMET)
(software: IAS/D - K2 -VMS)

.New hardware integration such as CPU features, NDS, large memories.

.Small system VMS to provide host for bounded systems.

.Develop real-timeness in VAX products. (Define needs).

.Evaluate need for comprehensive (mainframe) Fortran for VAX.

.Must produce a timely new language capability.

RT/C ASSUMPTIONS AND IMPLICATIONS

A. Markets are driven by price and performance. We expect an evolution to 32-bits with its leverage. The base of our users will expand and as such require servicing more, less sophisticated users. As a result, ease of system use and overall system RAMP are important factors.

B. Competition is led in technology by IBM due to their investment level. DEC is a reasonable "target" for others to shoot at and compounded by our broad approach to the marketplace. Traditional competitors, (HP, DP, IBM) will continue with a broad approach. Emerging competitors (Prime, Tandem, Modcomp) will carve out specific areas to apply their offerings such as virtual memory, MP and fast real-time. Our response must include continued product breadth (no gaps) with enhancements to our offerings. Also, the timely support of new products and response to market standards will be important.

C. Technology is producing both new 16-bit and 32-bit systems along with a distributed approach to applications as low end costs are driven down. We must clarify our understanding of the high-end PDP-11 strategy in the context of other POT plans and either modify our current strategy of phasing over to 32-bits, or modify the CPU strategy away from high end 16-bit offerings, as their functionality is beyond the support scope of our current offerings. We must also concentrate on understanding and defining our real-time approach to networks which appear to have impact on development plans. A fundamental requirement along with a simpler master/slave approach.

PRODUCT CALENDAR (Figure 1)

The project list for FY79 development is attached as Figure 1. The 2 new products are: 32-bit real-time (scheduled to be available with COMET), and RSX11-MP (2nd half of FY79 with the MP hardware.

BUDGET ASSUMPTIONS AND RISKS

We are assuming that other POT's future products will not require changes to the RT/C operating system (i.e., DECnet, Commercial Languages, RMS/DBMS) and that there are not further cuts in the budget. Our contingency is built into our 32-bit development effort, not current products.

Any further cuts will have significant impact in the short term plan. The level of funding from other POTS remains fixed:

$720K	Mass Storage
$600K	S/S Terminal
$1050K	Base Pot

Current product contigency must be funded by the product lines directly.

RT/C REVENUE (Figure 2)

The attached revenue charts show that based upon projections from the product lines, new products will have a significant impact on revenues in the FY81 timeframe. Most significant is the 32-bit R/T program. Note also, that additional revenues can also be attributed to the high-end 16-bit system if coupled with an enhanced version of RSX11M, supporting larger memories and address features of 11/70 class systems and the 11/68 being developed.

RT/C POT INVESTMENT

The pie-chart is self explanitory. The bulk of the available development dollars used for existing products with 29% on the 32-bit R/T effort to support our FY81 strategy. Resources allow only 6% available for long term investment. The MP effort will slide into the 32-bit area within the next 2 years if the test effort on 16-bits is successful.

FRAMEWORK

We expect to continue to exploit current product strengths and integrate new products into our offerings. We have deferred significant effort on a new DOD language as the specification is still volatile. We anticipate reacting in a timely manner within a year. Our short term effort is directed toward integration of the 32-bit offerings, particularly COMET with good user level capability and documentation for the implementation of R/T applications and migration from the high-end PDP-11 base.

External factors include IBM as the technology leader, and we are monitoring vertically oriented competitors to assure we maintain an aggressive response.

PLAN TO MAINTAIN CURRENT POSITION

We view our current 16-bit offerings as mature and stable. Exploiting will consist of new device support, minor enhancements and making them easier to use. Our plan includes rounding out ou our languages and increasing reliability to reduce the SPR rate. MP will be tested on the 11/70 as a limited product to minimize the risks. The 32-bit R/T effort will include both driver and documentation system testing. Utilities will be "cleaned-up" and a fast backup capability for large disk subsystems.

We can enhance our position with effort in the following areas:

- Small systems VMS package to use in developing RT11 applications for bounded systems.

.PDP-11 source level debug package for F4+.

.High end 11 system to exploit 22-bit address capability (11/44, 11/48, 11/68).

ADDITIONAL DATA

Two revenue charts are included which illustrate the phase in of 32-bit systems. They both represent normalized revenue and the % of revenue by product class.

RT/C PROJECTS FOR FY79

	PROJECT	SUPPORT	COMMITTED	SURVIVAL	TOTAL
REAL TIME POT	RSX-11M+P	-	122	-	122
	D/IAS	61+138	178	60	437
	RSX-11M	414	-	107	521
	RT-11	302	408	-	710
	FILES/UTILITIES	381	123	183+62 (COM POT)	687+62
	FORTRAN IV	215	-	-	215
	FORTRAN IV+	245	218	123	586
	APL	-	-	-	0
	DOD-1	-	-	-	0
	WCS TOOLS	-	-	-	0
	MACRO-11	61	-	-	61
	BASIC-11	302	-	-	302
	VAX RT/C	-	-	600	600
		2119	1049	1073+62	4241+62

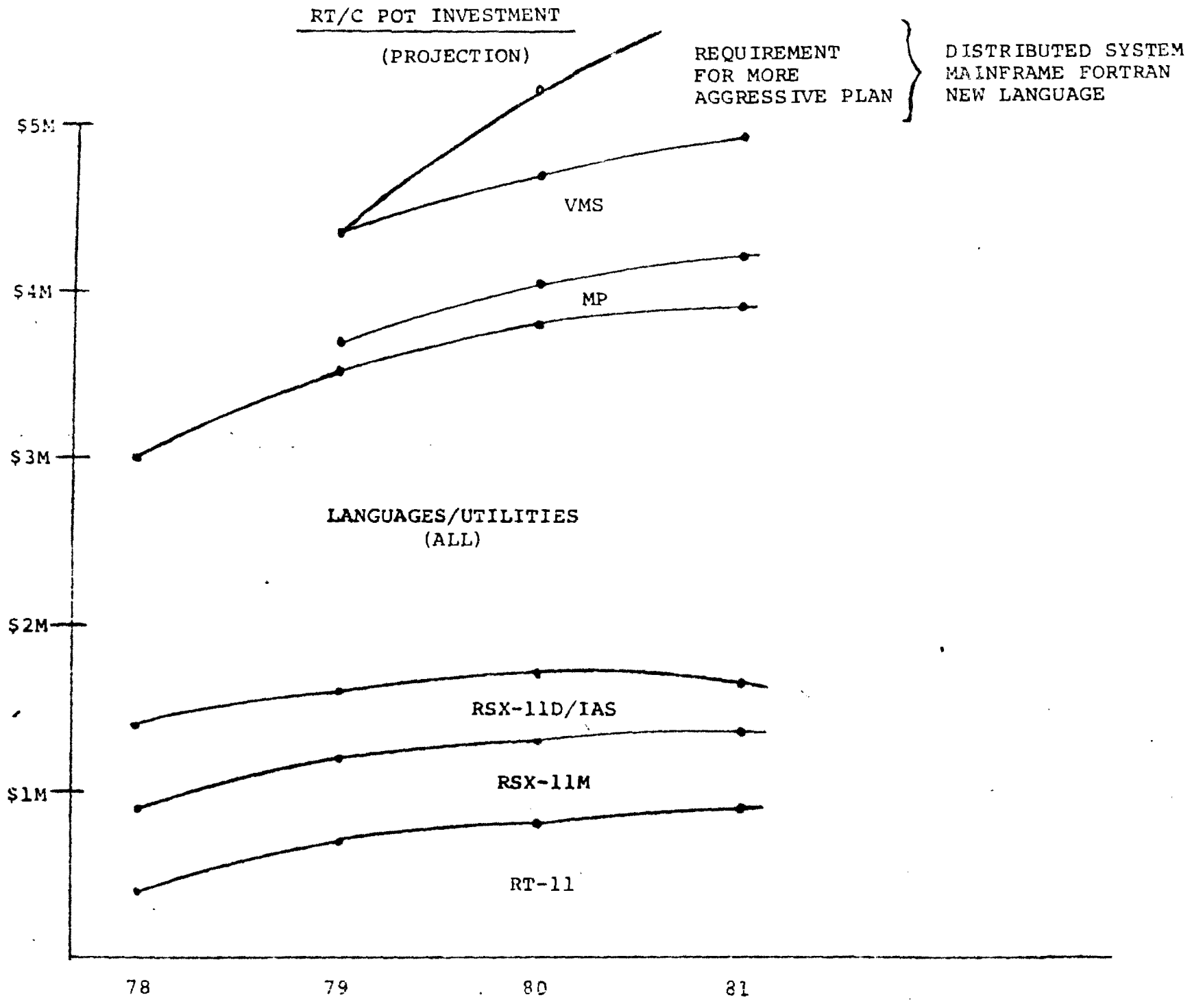
420 - VAX RT/C
60 - VAX F4P Extension
120 - Contingency

2122

(OOD 1700 PL91 200) (RT POT 2100)

RT/C POT FUNDS

FIGURE - 1


RT/C POT INVESTMENT
(PROJECTION)
REQUIREMENT
FOR MORE
AGGRESSIVE PLAN
DISTRIBUTED SYSTEM
MAINFRAME FORTRAN
NEW LANGUAGE
$5M
$4M
$3M
$2M
$1M
VMS
MP
LANGUAGES/UTILITIES
(ALL)
RSX-11D/IAS
RSX-11M
RT-11
78
79
80
81

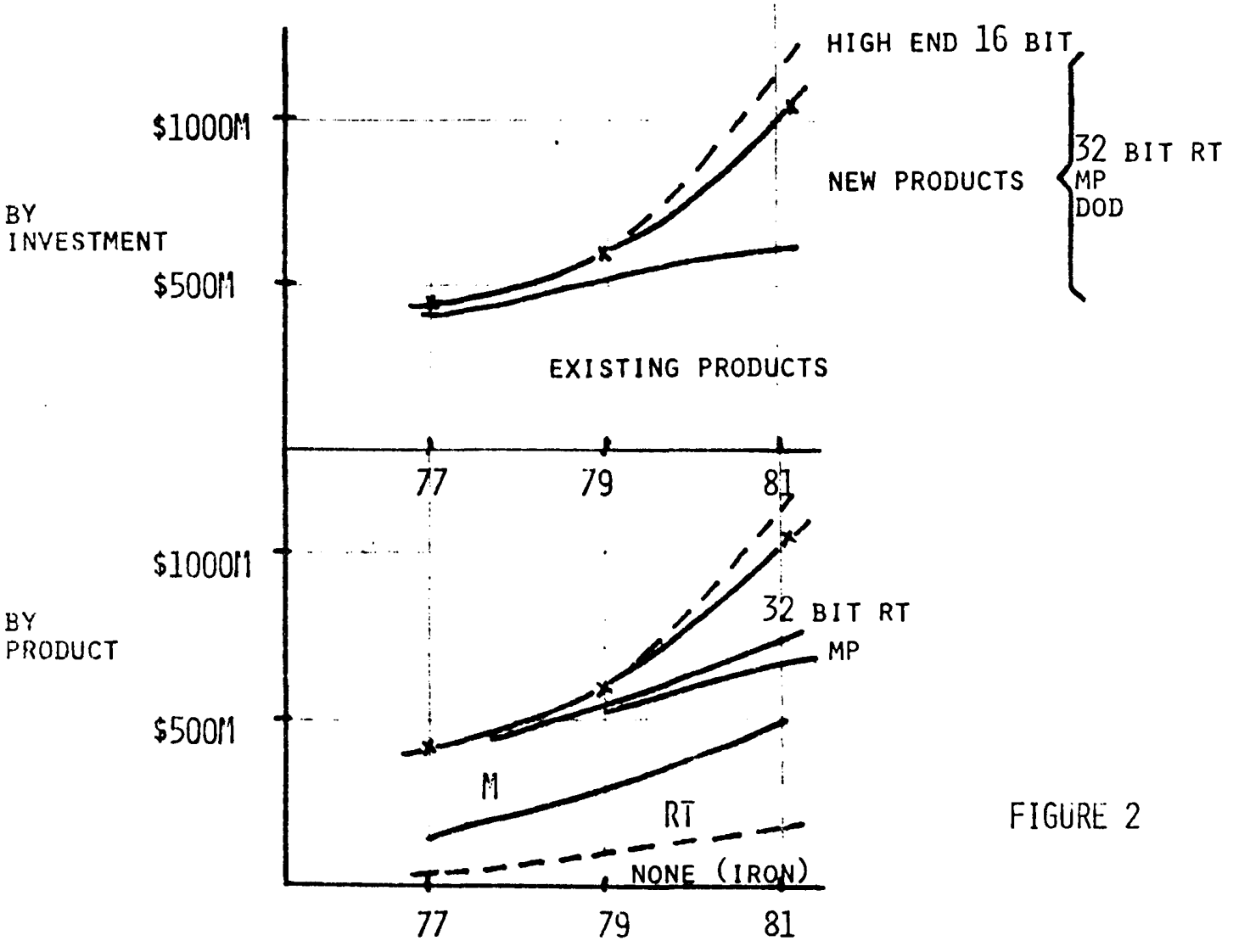
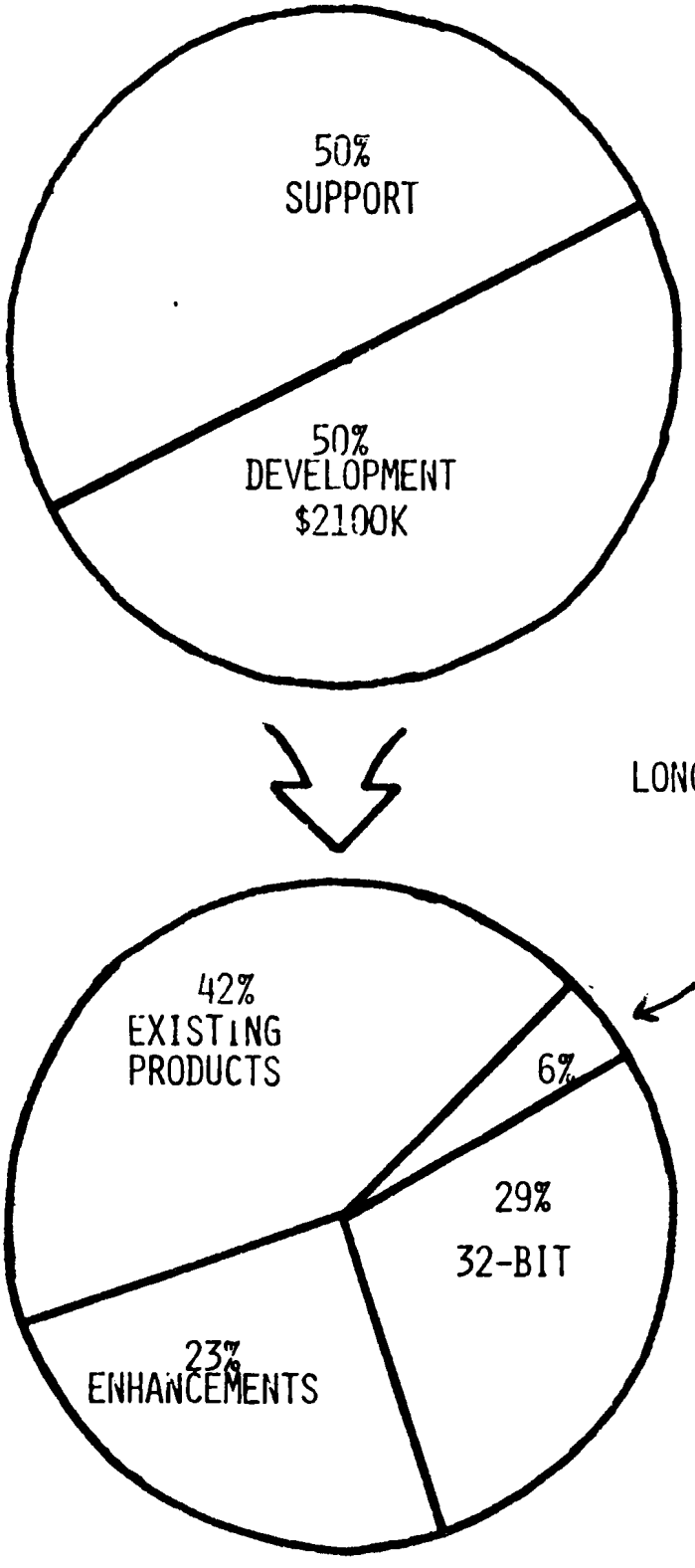


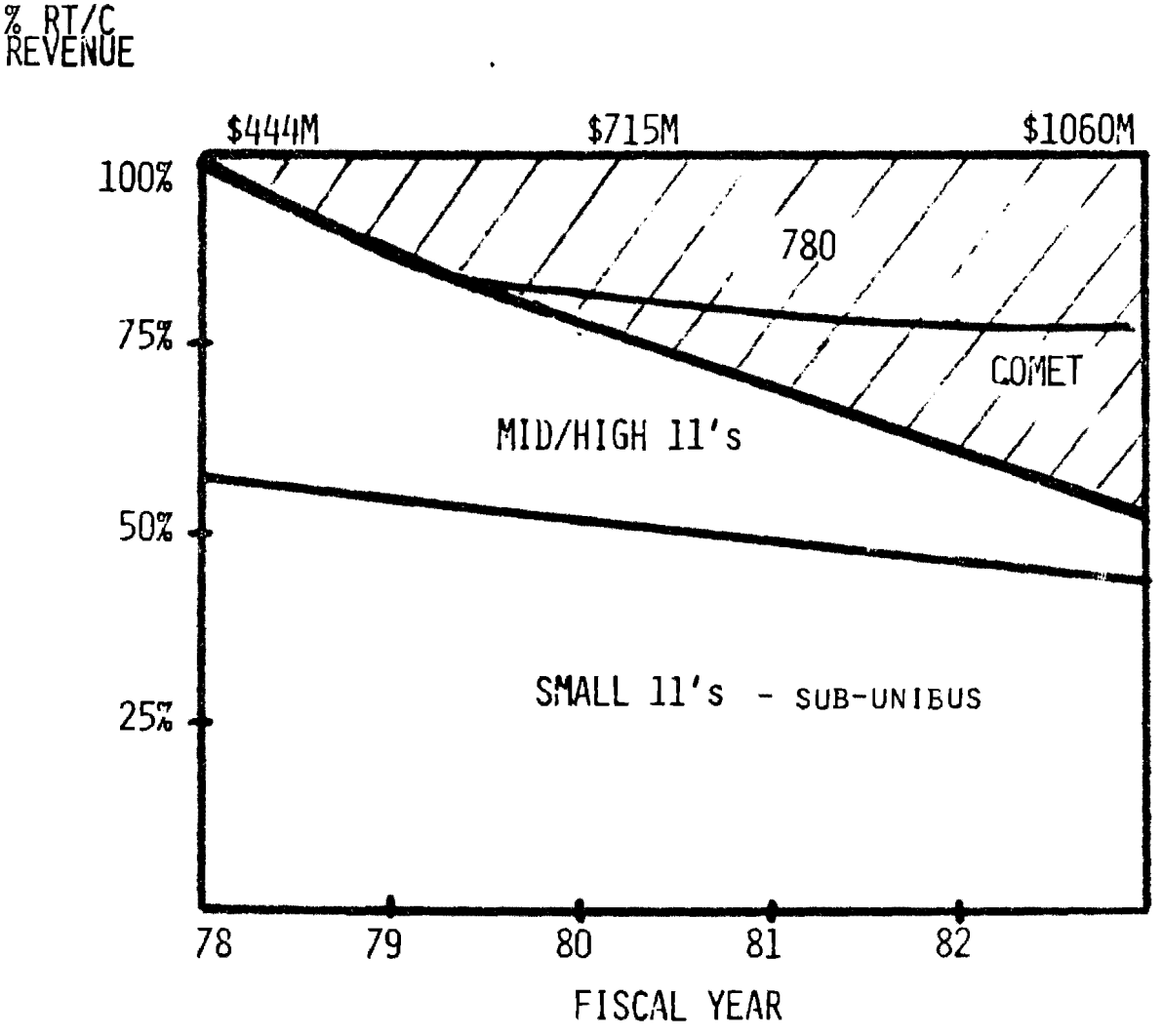
FIGURE 2

FIGURE - 2

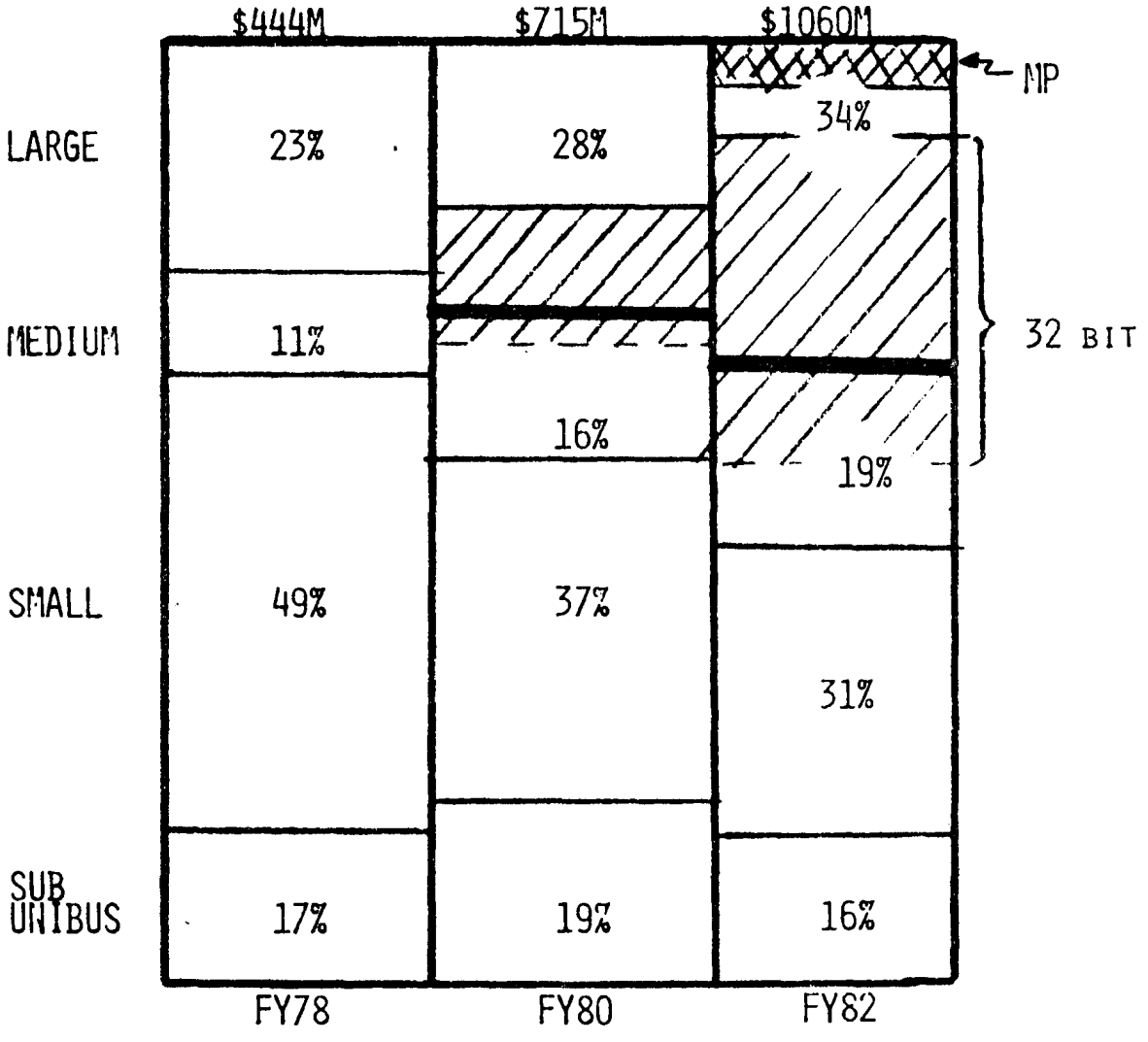
RT/C FY79 POT INVESTMENT



RT/C REVENUE PROJECTION



RT/C NOR PROJECTION
BY CPU CLASS



32 BIT: FY80 = 20%
FY82 = 35%

3/16/78

DRAFT
REV 4
17 May 1978

BASE SYSTEMS POT

LONG RANGE PLAN

SPRING 78

1.Ø GLOSSARY OF TERMS

11/44	Medium UNIBUS11 CPU extending the 11/34A
11/48	Medium UNIBUS11 CPU replacing 11/34A & 44
11/68	Large UNIBUS11 CPU replacing 11/6Ø, 7Ø & 74
11/74	Enhanced 11/7Ø for CIS & mP capabilities
CCD	Charge Coupled Device memory technology
CERBERUS	Codename for 11/74 mP project
CIS	Commercial Instruction Set
COMET	Medium VAX11 CPU, next down from 11/78Ø (STAR)
CPU	Central Processor Unit
EBAM	Electronic Beam Addressable Memory technology
FCS	First Customer Ship
FONZ	CPU chip set successor to LSI11
FPP	Floating Point Processor
HMOS	Higher-level NMOS technology
IT	Intelligent Terminal
LSI	Large Scale Integrated semiconductor circuit
LSI/VAX	Low-end VAX11 CPU next down from NEBULA
MASSBUS	High-performance controller-device interconnect
MBM	Magnetic Bubble Memory technology
MOS	Metal Oxide Semiconductor technology
mP	Multi Processor
NEBULA	Small VAX11 CPU, next down from COMET
NMOS	N-channel or Nitride MOS technology
PAX	Physical Address eXtension of 11/7Ø origin
PMI	Processor-Memory Interconnect, generic
PULSAR	Codename for LSI11 mP project
RAM	Randomly Addressable Memory
RDS	Remote Diagnosis Service
SUPERSTAR	Large VAX11 CPU successor to 11/78Ø (STAR)
TTL	Transistor-Transistor Logic
UNIBUS	Standard PDP11 family interconnect
UNIFONZ	Small FONZ-based UNIBUS11 CPU replacing 11/Ø4
VMS	Virtual Management System software for VAX11

2.0 PRODUCT CALENDAR

TITLE	DESCRIPTION	FCS as of SPRING77	FCS as of SPRING78
VAX11			
COMET	o Base CPU with integral warm-FPP & CIS and optional WCS o Hot-FPP option	Q4,FY79t	Q1,FY80 Q1,FY80t
PDP11			
KK11A	Cache option for 11/34A	Q1,FY79t	Q4,FY78
11/74	Corp cab 11/70 with CIS option & mP Extensibility	Q1,FY79t	Q3,FY79
11/74mP	CERBERUS 11/74 mP under RSX11M-PLUS	Q1,FY79t	Q3,FY79
11/44	Extended 11/34A with PAX & CIS options	-	Q4,FY79
UNIFONZ	FONZ-based 11/04 CPU (board) replacement with integral warm-FPP & CIS	-	Q1,FY80t
11/68	Lower-cost 11/74 CPU replacement	-	Q4,FY80t
11/48	Higher performance 11/44 & 34 CPU replacement at UNIFONZ cost	-	FY81-2t
MEMORIES			
MSIIL	16K MOS chip upgrade for 11/04-34	Q1,FY79t	Q1,FY79
MS780D	16K MOS chip upgrade for 11/780	-	Q1,FY79
MKA11	4K MOS chip memory for 11/74	Q4,FY78	Q3,FY79
MS11KC	16K MOS chip upgrade for 11/74	Q1,FY79t	Q4,FY79t
MS11M	ECC 16K MOS chip memory for 11/44		Q4,FY79

Note: t=targetted (vs committed)

3.0 ASSUMPTIONS & IMPLICATIONS

Markets

- Overall market competitiveness and growth can be secured by top down evolution of the 32-bit VAX11 family and ensuring the vitality of the 16-bit PDP11 family underneath.

- Continued leadership in traditional real-time & computation markets can be realized by VAX11 & PDP11 positioning with VAX11 establishing quickly in applications requiring large program performance or richer functionality.

- Performance and commitment to commercial markets can be strengthened by (COBOL-supported) PDP11 CIS extensions particularly in the high-end and additionally by VAX11 commercial software developments.

- Cumulative investments in volume or software-leveraged markets will impede PDP11 migration to VAX11 and require PDP11 (lower-cost) evolution to overlap more with VAX11 than might otherwise be necessary.

- Improved availability trends can be expected to shift to continuous availability in a larger part of the on-line and real-time markets or become a major selling feature. This requires the formulation and implementation of an appropriate and aggressive product strategy.

Competition

- IBM will move closer to minicomputer price-performance trends across the range. Successors to Series 1 (high-performance), System 34 (improved functionality), 370/115 & 125 (E Series virtual memory) will challenge starting 1978.

- DG will introduce a 32-bit machine around the end of 1979.

- HP will concentrate on lower-cost & functionality extensions to the 3000 & 21MX's up to the 1980's atleast.

- Traditional 16-bit competitors will all provide minicomputer evolutions at lower cost mostly.

- TANDEM could set the high-availability market place with their multiprocessor offering.

Technology

- Semiconductor LSI is the driving force on CPU & memory developments, eg:

Custom NMOS	CPU: UNIFONZ	FCS Q1,	FY80	
TTL Gate Array	COMET	Q1,	FY80	
Off-The-Shelf	11/68	Q4,	FY80	
Off-The-Shelf	NEBULA		FY81	Provisional
Custom HMOS?	11/48		FY81-82	Provisional
Custon HMOS?	LSI/VAX		FY82	Provisional
ECL Gate Array	SUPERSTAR		FY82	Provisional
16K MOS RAM's	MEMORIES		FY78	
64K MOS RAM's	MEMORIES		FY81	Provisional

4.0 PRODUCT GOALS & STRATEGIES

4.1 VAX11

Extend the VAX11 family down in cost from the 11/780 at constant functionality:

COMET
- o leadership midrange 32-bit CPU
- o FCS Q1, FY80
- o 65% 11/780 performance at 35% cost
- o 16MB physical memory addressing
- o integral CIS, warm FPP & RDS-hooks
- o optional hot FPP & WCS
- o system & box packaging
- o PMI, MASSBUS & UNIBUS
- o TTL gate array LSI technology

Products in an advanced development or conceptual stage through FY79 are:

NEBULA
- o earliest low-cost 32-bit CPU driven by distributed processing
- o FCS FY81
- o trade-off performance for 50% COMET cost

LSI/VAX
- o 32-bit microprocessor entry
- o FCS FY82
- o some 25% COMET performance and cost

SSTAR
- o leadership high-end 32-bit successor to 11/780
- o FCS FY82
- o some twice 11/780 performance at 65% cost

4.2 PDP11

Correct midrange exposure to physical memory address space, and -
Improve midrange and high-end performance for COBOL computation:

11/44
- o build on 11/34A as lowest-cost midrange base
- o FCS Q4, FY79
- o 20% faster than 11/34A at small (5%) additional cost
- o 4MB physical memory addressing with PAX
- o PAX & CIS additions to 11/34A FPP & cache options
- o built-in CERBERUS mP hooks (only), like 11/74
- o box packaging
- o PMI & UNIBUS

11/74
- o enhanced 11/70 for commercial performance & CERBERUS multiprocessor extensibility
- o FCS Q3, FY79
- o CIS addition to FPP option
- o field upgradable to CERBERUS mP
- o corporate cabinet repackaging

Standardize on the revised PDP11 CIS specification for improved performance through extended data type support.

4.2 PDP11 (Cont.)

Maintain longer-term PDP11 competitiveness. Provisional product definitions are:

UNIFONZ
- o earliest small UNIBUS CPU by capitalizing on FONZ chip technology for 11/04 & lower-half 11/34A replacement.
- o FCS Q1, FY80
- o performance of 90% base 11/34A, 10% 11/34A FPP & 10% 11/44 CIS, all at 11/04 cost
- o integral warm FPP & CIS on single CPU board
- o board replacement for 11/04 & 34 CPU's with common packaging
- o PAX hooks (only) & system packaging under evaluation
- o custom LSI MOS (FONZ)

11/68
- o high-end 11/74 replacement at lower cost
- o FCS Q4, FY80
- o 11/74 performance and functionality at $4.5K base CPU (box) & 256KB memory cost or always less than 50% 11/74 cost.
- o integral warm-FPP & RDS-hooks
- o CIS & hot-FPP (1.5 FP11E speed) options
- o built-in CERBERUS mP hooks (only), like 11/74
- o system & box packaging
- o PMI, MASSBUS and UNIBUS
- o LSI off-the-shelf technology

11/48
- o building-block approach to UNIBUS CPU replacement in the UNIFONZ to 11/68 space.
- o FCS FY81-82
- o custom LSI (HMOS?) converged with FONZ chip successor

4.3 MULTIPROCESSING

Productize CERBERUS 11/74 multiprocessor under RSX11M-PLUS for FCS Q3, FY79 as earliest response to high-performance improved-availability markets.

Continue 11/780 multi-port memory development for FCS Q3, FY79.

Design a CERBERUS-like 11/780 multiprocessor offering higher availability with high performance for applications where load sharing requirements are high and not predictable for effective application segmentation.

Establish a task force to identify the system topology in greater depth to satisfy those applications that require continuous operation and where the application is generally predictably segmented.

Continue PULSAR LSI11-based advanced development (non-POTS funded) for more understanding of a multiprocessor approach to a general purpose product set for the future.

4.4 MAIN MEMORIES

MOS RAM is the dominant technology for main memory

- o upgrade all MOS memories from 4K to 16K chips by FY79 for major bit-cost reduction.
- o track 64K chip development and cost-effective availability, probably FY81/82

Introduce ECC capability across the range with optional availability for small UNIBUS CPU's ie 11/Ø4, 34 & UNIFONZ

Continue centrally-funded evaluation of new technologies (eg MBM, CCD, EBAM) fitting in the price gap between MOS & disc storage for optimum memory hierarchy architectures. Current product strategy does not incorporate such new technologies.

Maintain aggressive technology tracking and pricing posture

4.5 ARCHITECTURE & COMPATIBILITY

Focus on software and external bus compatibility across the broadest range of CPU and system families

Keep architectures sufficiently fixed to provide products resulting from historic cumulative investments, internal & external.

Settle on 11/74 functionality less Dual Registers & Stack Limit Register as the internal standard for PDP11 CPU software compatibility. Hold on to 11/78Ø functionality as the VAX11 CPU standard.

Avoid Operating System proliferations by forcing adherence to the RSX11M & K2 Kernels for PDP11's (except the Low End) and the VMS Kernel for VAX11's.

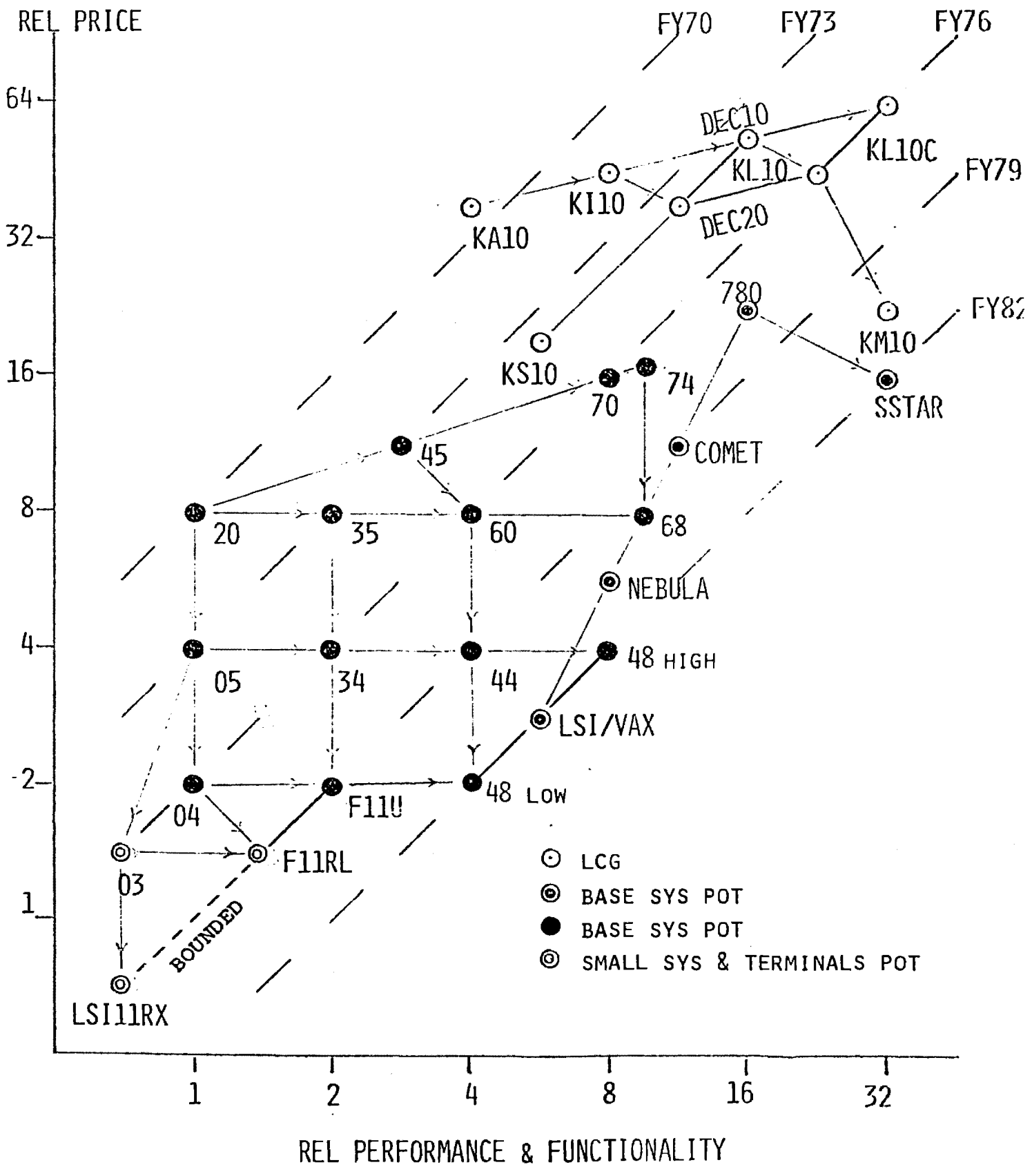
Evolve longer-term to a corporate UNIBUS replacement to correct increasing competitive exposure to interconnect functionality, performance, cost and data integrity as a major artery of the business.

4.7 SYSTEMS FOCUS

Push Corporate Packaged Systems as the process and tool for improved focus on the systems business.

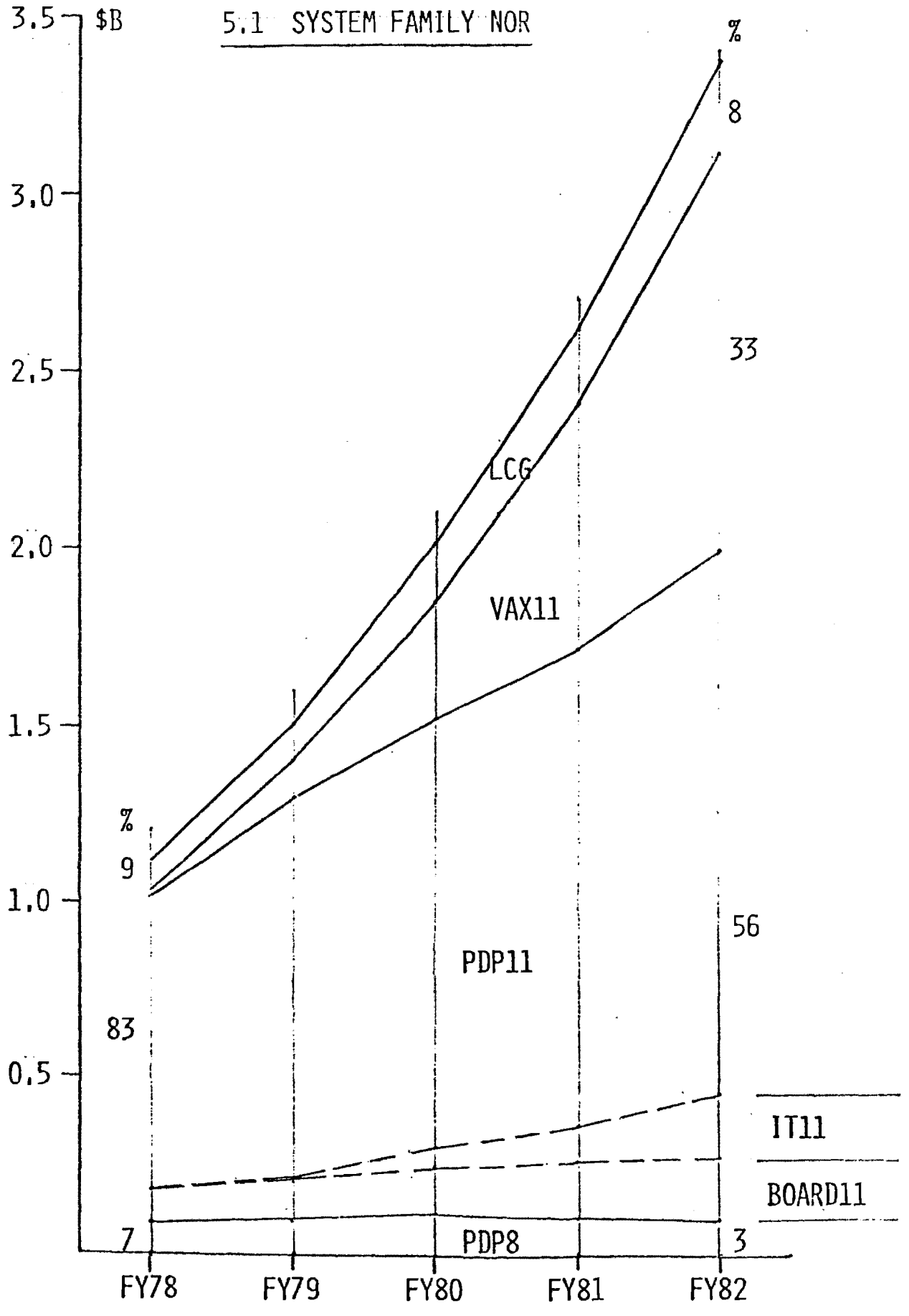
Use system design and manufacture to lead in selected system configurations.

4.8 CPU FAMILIES: PRICE & PERF POSITIONING

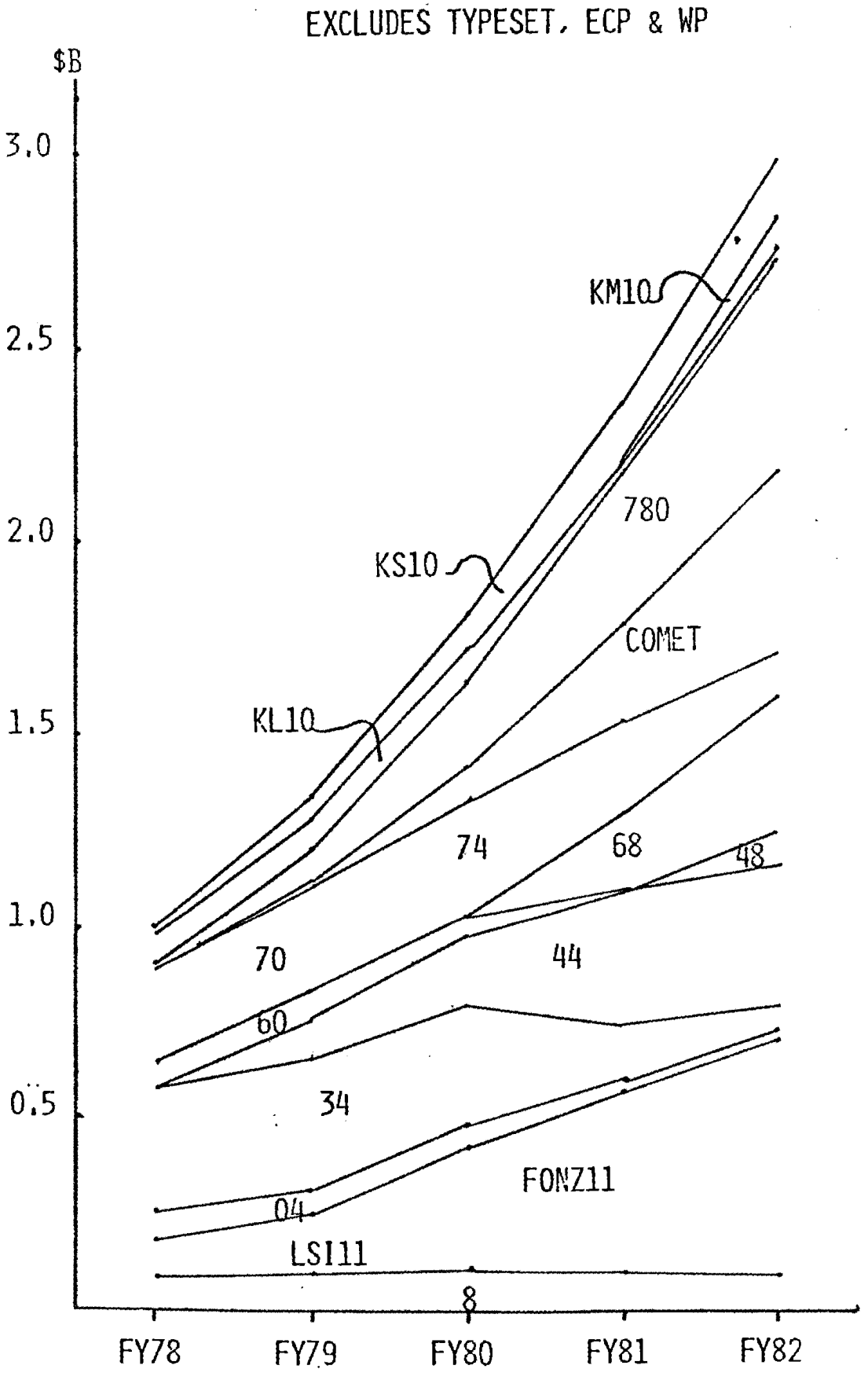


5.0 REVENUES

5.1 SYSTEM FAMILY NOR



5.2 SYSTEM NOR BY CPU



6.0 INVESTMENT ($M)

PROGRAM	FY78	FY79	FY80
11/780	2.4?	0.6	-[4]
VMS	2.0?	1.7	1.5[4]
COMET	2.3?	3.2	1.0
NEBULA	-	-	1.3
SUPERSTAR	-	-	1.3
11/780mP	0.3	0.95	-
11/74 mP	Note 1	0.55	-
Collective mP (FY80)	-	-	2.5
K2 Kernel	0.5?[2]	1.05	0.5[4]
Standard Systems	0.2	0.4	0.4
11/74	0.7[3]	0.9	-
11/68	0.3	0.85	1.9
11/60 (62)	0.3	-	-
11/48	-	0.2	2.0
11/44P	0.8	1.2	0.3
UNIFONZ	-	0.5	0.2
Memories	0.9?	0.4	0.6
Contingency	-	0.5	0.5
TOTAL	10.7?	13.0	14.0
Annual Growth	-	21.0%?	8.0%

Note:
1. $1M TELCO funding
2. Plus $0.4M TELCO funding
3. Plus $0.2M DDP funding
4. Assumes $0.5M Product Support funding by non-POTS each

7.0 MAJOR ISSUES

Is the 11/68 CPU cost aggressive enough? To be reviewed.

Do we need a multiprocessor solution, PULSAR or its like, to mainstream CPU development? PDP11 only? Is PULSAR advanced development funding stable or adequate enough through FY79?

Can SUPERSTAR and KM10 (next high-end DEC20) be the same base CPU?

Interconnect strategies, specifically QBUS vs UNIBUS, are being worked but are taking a long time to reach any reasonable corporate concensus.

How stable is the Small Systems & Terminals POT strategy to not develop a quad QFONZ successor to the 11/03? A reversal might impact UNIFONZ strategy.

APPENDIX : SYSTEM NOR BY CPU

CPU	SYSTEM NOR $M					
	FY78	FY79	FY80	FY81	FY82	TOTAL
PDP8	80	90	111	100	91	472
BOARD11	87	113	138	155	178	671
IT11	--	6	41	100	180	327
03, UNIFONZ	72	107	219	300	347	1045
04, 05	81	80	66	41	19	287
34, 35	324	344	305	150	71	1194
44, 48	--	101	183	335	417	1036
60	60	63	56	17	2	198
68	--	--	40?	233	410	683
70, 74	253	292	258	201	122	1126
PDP11 TOTAL	877	1106	1306	1532	1746	6567
COMET	--	2	89	256	470	817
780	8	80	215	383	547	1233
VAX11 TOTAL	8	82	304	639	1017	2050
KS10	7	46	102	132	146	433
KL10	94	80	65	55	22	316
KM10	--	--	--	15	88	103
LCG TOTAL	101	126	167	202	256	852
TOTAL	1066	1404	1888	2473	3110	9941

NOTE: EXCLUDES TYPESET, ECP & WP

Education
Products
Group

education products for the globe

digital

18 April 78

TO: Stan Pearson
Bruce Delagi

FROM: Al Dziejma Strategy Manager, T/SS POT
Jerry Witmore Chairman, T/SS POT

SUBJECT: T/SS REDBOOK STRATEGY DOCUMENT

Enclosed is a revised (as of last Friday's POT Meeting) Strategy Document.

Future POT Meetings will focus on major issues and their impact two to three years out.

JW:kb
Enclosure

XC: Dick Clayton

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T/SS STRATEGY

	NOR		DEV. EXP.	
	79	80	79	80
BASE TERMINALS	135	160	3130	4400
INTELLIGENT TERMINALS	26	66	990	2100
CHIPS, BOARDS, RACK & STACK	60	80	2575	6000
SMALL SYSTEMS	63	128	1490	
LINE PRINTERS	50	56	170	500
CONTINGENCY			645	800
TOTAL	334M	490M	9000K	13800K

T/SS STRATEGY

MARKETS SERVED

- DEC SYSTEMS TERMINALS REQUIREMENTS (ALL DEC MARKETS).
- INDEPENDENT: DUMB, SMART AND INTELLIGENT TERMINALS MARKETPLACE.
- LOW-END OF OEM AND END-USER MARKETS. (BOARDS TO SMALL SYSTEMS, BOUNDED AND RACK/STACK).

COMPETITION

- SYSTEMS COMPETITION (I.E., IBM, DG, BASIC FOUR, HP, WANG).
- COMPONENTS COMPETITORS (I.E., INTEL, T/I, ZILOG, MOTOROLA).
- TERMINAL COMPETITORS (I.E., TELETYPE, LEAR SEIGLER, TI, ETC.).
- INTELLIGENT TERMINAL (I.E., SYCOR, ADDS, DATAPOINT, ETC.).

T/SS STRATEGY

WHERE WE ARE TODAY: C/E PRODUCTS ONLY

- DUMB TERMINALS

  HARD COPY: LA36
  SOFT COPY: VT52

  - INDEPENDENT TERMINAL BASE
  - DEC SYSTEMS

- SMART TERMINALS

  VT61
  VT62

  - MARKET/APPLICATION SMART TERMINALS

- INTELLIGENT TERMINALS

  NONE

  - NEW MARKET/PRODUCT OPPORTUNITY

- RACK & STACK

  PROCESSOR: LSI 11
  BOXES: 11/03L
  PERIPHERALS: RX01, RL01
  PRINTERS: LA180

  - GENERAL PURPOSE COMPONENTS FOR VOLUME & END-USER MARKETS.

- SMALL SYSTEMS

  11V03
  11V03L

  - PRE CONFIGURED SYSTEMS FOR VOLUME & END-USER MARKETS.

T/SS STRATEGY

WHERE WILL BE BE IN FY79/80: (CONSTRAINED C/E DEVELOPMENT 9.0)

- DUMB TERMINALS

  HARD COPY: LA120, LA00
  SOFT COPY: VT100

  - INDEPENDENT TERMINAL BASE- & DEC SYSTEMS

- SMART TERMINALS

  VT100 (EDITING VERSION)

  - PRODUCT LINES MUST FUND MARKET/APPLICATION SPECIFIC SMART TERMINALS

- INTELLIGENT TERMINALS

  IT100 A (NO MASS STORAGE)
  IT100 B (TU58 MASS STOR)

  - SOFT COPY TERMINAL BASED SYSTEM. BOUNDED BY COMPONENET PACKAGING & AVAILABLE SOFTWARE.
  - ALLOWS NEW BUSINESS TO BE REALIZED.

- RACK & STACK

  PROCESSOR: LSI11, FONZ 11 DUAL, T-11 CHIP
  BOXES: 11/03L
  PERIPHERALS: TU58, RX02, RL01/02
  PRINTERS: LA180

  - GENERAL PURPOSE COMPONENTS FOR OEM & END-USERS P/L'S.

- SMALL SYSTEMS

  11V03L, 11T03L, (LSI-11 WITH RX02 AND RL01)
  11V23, 11T23 (F-11 WITH RX02 AND RL01)

  - PRE CONFIGURED SYSTEMS FOR VOLUMI & END-USER MARKETS.

T/SS STRATEGY

KEY STRATEGY ELEMENTS

DUMB TERMINALS:

- CAPTURE DEC'S SYSTEMS TERMINAL BUSINESS.
- PROTECT AND GROW EXISTING INDEPENDENT BASE TERMINAL BUSINESS.
- EXPLOIT BASE TERMINAL TECHNOLOGY TO SUPPORT PARALLEL EFFORT IN INTELLIGENT TERMINALS.
- FOCUS ON GENERAL PURPOSE RATHER THAN APPLICATION SPECIFIC TERMINALS.
- MAXIMIZE COMMON TECHNOLOGY BETWEEN HARD AND SOFT COPY TERMINALS FOR VOLUME AND DEVELOPMENT BENEFITS.

INTELLIGENT TERMINALS:

- ENTER A NEW BUSINESS TO DEC.
- PRODUCE A GENERAL PURPOSE INTELLIGENT TERMINAL, USING THE PDP11 ISP THAT IS COMPETITIVE WITH THE INDEPENDENT INTELLIGENT MANUFACTURERS FOR FCS IN FY79.
- PROTECT LOW-END OF DEC'S EXISTING BUSINESS FROM EROSION BY INTELLIGENT TERMINAL MANUFACTURER.
- ENHANCE DEC'S TOTAL SYSTEM OFFERING TO THE MEDIUM AND LARGE COMPUTER BUYER.

T/SS STRATEGY

KEY STRATEGY ELEMENTS

COMPONENTS (BOARDS):

- ENTER MARKETPLACE WITH LOW COST IMPLEMENTATION OF PDP-11 INSTRUCTION SET (T-11) AND EXPAND WITH HIGHER PERFORMANCE IMPLEMENTATION (F-11).

(BOXES)

- PROVIDE DIRECT REPLACEMENT FOR 11/03 BOXES WITH SAME PERFORMANCE & LOWER COST.

(PERIPHERALS)

- PROVIDE PRICE/PERFORMANCE OPTOMIZED MASS STORAGE PERIPHERALS.(I.E. COMPETITIVE PERFORMANCE & PRICE)

- PRODUCT MUST BE DOCK-MERGEABLE/DROPSHIPPABLE

T/SS STRATEGY

KEY LEVERAGE FACTORS

- HIGH VOLUME REQUIRED IN ORDER TO MEET COST GOALS.
- CORPORATE COMPONENT PURCHASING POWER COMBINED WITH FOCUSED PLANTS.
- PRODUCT RELIABILITY/SERVICEABILITY
- DISTRIBUTOR CHANNELS
- PDP11 HARDWARE AND SOFTWARE COMPATIBILITY
- ABILITY TO MANUFACTURE, OR LICENSE, ALL REQUIRED COMPONENTS.
- COST OF SALES AND SUPPORT.
- TIME TO MARKET
- SHORT DELIVERY TIME
- PRODUCT STABILITY
- EASE OF USE
- WEIGHT AND PHYSICAL SIZE
- PHASE-IN/PHASE-OUT IMPACT

T/SS STRATEGY

FACTORS AFFECTING STRATEGY

- RAPID TECHNOLOGY CHANGES ARE FORCING SHORTENED PRODUCT LIFETIME.
- PRODUCT COMPROMISE REQUIRED IN ORDER TO SERVE VOLUME AND DEC SYSTEMS MARKETS.
- COMPROMISE REQUIRED IN ORDER TO LEVERAGE TECHNOLOGY ACROSS BASE TO INTELLIGENT TERMINALS.
- MANY COMPETITORS ARE IN A FOCUSED BUSINESS.
- LACK OF CONTROL OVER DISTRIBUTION CHANNELS.
- LARGE INVESTMENT REQUIRED IN MANUFACTURING STARTUP.
- NEED FOR LONG TERM COMMITMENT TO MANUFACTURING.

T/SS STRATEGY

ISSUES

- THE NET FUNDING LEVEL IS TOO LOW AND CAUSES STRATEGIC DISPERSION, VIA MANY P/L FUNDED POINT PRODUCTS (RXT-11) ETC.
- PROPOSED ELIMINATION OF QUAD FONZ FORCES STRATEGIC DECISION OF "Q" BUS SYSTEMS FUTURE.
- DELAY OF T-11 FORCES REEVALUATION OF INTELLIGENT TERMINAL AND BOARD PRODUCTS AND STRATEGY. (SHIFT TO FONZ)
- NO VERY LOW COST SOFT COPY TERMINAL FUNDED.
- SMALL SYSTEM EVOLVING TO BOUNDED SMALL SYSTEM (RXT11), (IT100). MUST RESOLVE INTELLIGENT TERMINAL VERSUS SMALL SYSTEM.
- NO MICRO PRODUCTS SOFTWARE FUNDED.
- NO LONGER ABLE TO COMPROMISE PRODUCT COST/FUNCTIONALITY IN ORDER TO SERVE ALL MARKETS.
- NO DIRECT LINE PRINTER PRODUCTS FUNDED.

VI. Networks and Communications

SPRING RED BOOK

NETWORKS/DISTRIBUTED SYSTEMS

MAY 5, 1978

TABLE OF CONTENTS

SECTION I

DECNET

I. DECNET SOFTWARE

1 ASSUMPTIONS AND IMPLICATIONS

1.1 Markets

A. Chief buying influences and requirements, now and later.

1) The desire to share resources between two or more systems is the major provocation for our customers. This takes two forms:

+ The user with an installed system who finds he needs or wants to share data or programs with a neighbor system or a larger system

+ The user who plans an application based on multiple systems sharing resources.

Both types of users are interested in minimized communications costs; control of central data centrally; local control of the processing resource so the local user has a high sense of ownership. The latter user is interested in tailoring each local system to the needs of that application using micro, mini, midi, or maxi computers and RT, Timesharing, or Transaction Processing operating systems where needed.

2) A second major influence is the promise of a networking capability to the user as a protection for today's investment. Many DEC customers will buy our systems because we have DECnet even though they will not buy DECnet today. It is our commitment to networks and Distributed Processing as demonstrated by DECnet and interconnect products that attracts them and ties them to us over the long run.

3) Those IBM customers who want to distribute a process from their mainframe to a stand-alone system, but want to share data between the system and the mainframes. Emphasis is not on networks per se, but on the ability to maintain coherence with the data base. This provokes the need for IBM interconnect protocol emulators.

B. Segmented Description of the Market

1) Stand-alone systems -- not distributed. Characterized by single processor with single terminal access, batch or interactive operation. This is the portion of the market not addressed by networks.

2) Distributed Access Systems -- Characterized by a central processing system accessed by multiple terminal locations; terminals can be batch, interactive, or mixed. Objective is to provide access to system from work locations, while maintaining central processing and data base.

   a. Local Multiple Access -- All terminals local to central system; no communications lines used.
   b. Remote Multiple Access -- Terminals are geo--raphically dispersed from central system location; communication lines used to connect terminal locations to central location.
   c. Concentrators, Multiplexors, and Front-end Processors -- Augment remote multiple access systems to reduce comm and comm processing costs.
   d. Preprocessing without data base -- Intelligent processors provide limited pre-checking of transactions in order to reduce communications traffic, and thereby comm. costs.

   Digital's offerings in this area are DECsystem 10's and 20's, RSTS/E systems, and TRAX. In addition, our protocol emulators allow Digital's systems to interface with large mainframe offerings to provide Distributed Access.

3) Distributed Processing Systems -- Characterized by multiple processors and multiple data bases. Objective is to locate computing power and data bases in closer proximity to work locations, with some or most of processing performed independently of any other processor.

   a. Autonomous Multiple processor Systems -- Application problem is divided among several autonomous processors and data bases, with no communications links between them.
   b. Semi-autonomous Multiple processor Systems -- Computing load and data base are split between several processors with communications links between processors. Each transaction may be handled locally or sent to one or more other processors.
   c. Intelligent Pre-processor with DataBase -- Substantial pre-processing of transactions including access to local database. Some transactions handled locally, others sent to central system.

Digital has focussed its traditional non-network business in 3a above. Single processor systems were sold as autonomous systems with no networks.

Our sophisticated customers provided their own comm capability leading them into b. or c. DECnet Phase II products impact 3b and 3c above, today and in the future.

1.2 Competition

A. Current versus Projected Positioning and their Emphasis.

Currently, we can position ourselves with two types of competition:

+ Those that have network software (IBM, HP, Modcomp)

Of these three only IBM has a network architecture. HP offers similar features to DNA but has no over-riding architecture. SNA is a terminal-oriented architecture with all network knowledge located in the central 370 host. Because of its relative inefficiencies, IBM users have been slow to accept SNA, although we believe SNA is here to stay. IBM's resources and account control will assure that. Our SNA facilities ensure that we can participate in the Distributed Access environment.

HP has diverse network software for the HP3000, HP1000, and the 21MX. They offer advanced functionality (routing, virtual terminals), but lack a consistent architecture. They do an excellent job of marketing the limited products and operating systems by aiming at specific market segments. We appear to have higher maintainability and better performance than HP's offering today. HP will grow in strength and remain a strong contender over time.

MODcomp offers high performance networks with a high comm capabilities and very limited network capabilities. Their key is market focus in the high performance network areas - process control and sensor-based lab areas. They have been successful in taking some large government network business away from DEC. Again, this is a case of marketing a limited capability well against our broader approach.

+ Those with no network software (DG, PRIME).

  These companies compete with us using "roll-your-own" comm software in special cases where DECnet or IBM internetworks don't have any impact. In addition, DG's 3780 package is superior to our 2780 protocol emulators. We must continue to watch these companies since they are on a rapid growth curve and will someday have the resources to compete in this business.

In the future, we are positioning ourselves to compete with IBM and HP with the assumption that if we win consistently against them, we will control a large share of the market.

B. Estimate of Competitors' Spending for Development

IBM	significantly more than DEC
HP	less than DEC on the whole but more on a per product basis.
Modcomp	significantly less than DEC

C. Emerging Competitors.

Primarily, at the low end, we see Datapoint, Harris Wang and other intelligent terminal vendors aiming at our low end products. IBM is certainly emerging as a mini computer supplier, and if GSD is able to break away from SNA and offer a more general network strategy, they will represent formidable competition. Honeywell is expected to make a major network offering in the next year, but it is not clear the extent to which they will compete with us. Microprocessor manufacturers also would seem to be potential emerging competitors.

D. Consequences.

Digital has positioned itself as a principal supplier of network software, through the introduction of DNA. We represent one of the three key interconnect mechnisms today (the other two are SNA and X.25). Because of our product problems in the past, we are now perceived as having backed away from this leadership. Therefore we must:

+ Aggressively sell and market our existing products. We have received a commitment for funding from the Marketing Committee to help us in this domain.

+ Enchance our current products to meet the promises we made in 1976. The strategy portion of this document deals with this subject.

1.3 Technology

A. Technological Assumptions

Basic system cost will continue to decline, and interconnect will become easier, leading to increased demand for distributed computing and to larger networks.

The use of public packet switched networks based on X.25 will become increasingly attractive as a means of interconnecting DEC systems over the next 3-5 years. However, these networks will remain only one of several communications facilities a customer can select from, with his choice determined by his geographical and traffic requirements and common carrier rate structures. ATT's announcement of ACS, based on X.25, is expected to generate considerable legal activity as to be a non-facility for the FY '80- FY '81 time period. Thus, the major thrust of X.25 will be in Europe and Canada.

The current international effort to build a complete standard network architecture based upon X.25 will not result in product requirements in the three year framework, but will impact the state of distributed computing beyond that time-frame. Until then, the primary use of X.25 will be DEC to DEC and possibly DEC to IBM communication.

IBM's SNA will stabilize and become a significant network architecture with which we must interface. Other network architectures will not become significant factors in the market place to which we must interface.

The technology for building the transport portion of a computer network which routes messages over a combination of dedicated, circuit switched and packet switched facilities exists today and can be implemented through advanced development. Providing network security through an integrated application of the Data Encryption standard will be in a similar state within two years.

The technology for distributed access to disjoint data bases is now becoming available. However, providing transparent access to a highly available distributed data base is still a research topic. Current work is being done in the R&D area to help us get an understanding of this complex subject. More aggressive funding will be necessary in the future to allow us to grow in this area.

The economics of LSI technology and minimal requirements for network interconnect will continue to require a sub-low-end solution for bright/intelligent terminals which interface through a host, as distinguished from a low-end solution for small systems which interface as self-contained network nodes.

Local distribution through contention networks (e.g. Ethernet) may come out of the research stage and require incorporation into product strategy. Therefore, we shoul track this technology for potential applicability.

B. Exposures and Opportunities

The lack of standardization of higher level interfaces across operating systems is a technical/organizational issue which may impede ease of user migration and our use of common firmware implementations.

A breakthrough in the distributed data base technology would represent an opportunity or exposure depending on where the breakthrough developed and its market timing.

The industry wide adoption of a complete standard network architecture built on X.25 would greatly increase the market for distributed computing, while reducing the value of propritory architecture such as DNA. We must track standardization efforts to insure that they are consistent with our philosophy and that our product strategy reflects their progress.

2. PRODUCT/MARKETING GOALS AND STRATEGIES

2.1 Goals

The major emphasis by FY '81 is to have:

a) Transport mechanism transparency - that is the user should be able to transport data through DNA, X.25 or SNA transparently between his application programs

b) Common subset of file transfer across the network - some subset of our files structures must be available to all our systems over the network.

c) Good network diagnostics - our products must be highly maintainable with low MTTR.

d) Enter the distributed data base area - a pilot project at least to allow distributed data bases as well as files.

e) Have network terminal support.

2.2 Strategies

By FY '81, our transport mechanisms will include DNA, SNA and X.25. The general interconnect must be transparent to the user. We will have co-resident protocols and a common subset of file transfer across the network. This requires much more network diagnostics and fault isolation techniques.

Because of our large number of operating systems in the next three years, we will adopt the following strategy:

+ Some set of systems will be built to basic level of comm functionality and then be maintained.

+ Some set will be enhanced with additional functionality and serve as kernels for future growth.

+ Some set will be built on those kernels with our focus on applications and user interface.

The three new technology areas, investigation of which will be started in FY '79, are Distributed Access for DBMS type data, application focus (understanding how our current tools are used) and the terminals area. The technology is at the point where we should have these capabilities by FY '81.

2.3 What Have We Rejected

We have rejected the concept that DNA is the only transport mechanism needed for DEC in the distributed computing market and will offer both X.25 and SNA.

We have re-evaluated the concept of providing all operating systems with equal functionality and have decided to level off on certain systems once a base level of interconnectability has been achieved.

We have decided to provide limited functionality early where the technology for full functionality is several years away. Two examples are the homogeneous system virtual terminal and one-hop routing planned in FY '79. The heterogeneous system virtual terminal and complex routing will be introduced during 1980.

2.4 The Pivotal Issues?

In expanding the program to include other transport mechanisms, several issues arise: These are:

SNA	-	How do we support the product with all the IBM operating systems? Is it possible to provide a totally transparent interface for SNA? How do we deal with SNA Level 3, Level 4 incompatibilities?
X.25	-	This activity is currently funded by the product lines and not as a corporate product Unless it becomes a corporate product and so funded, it will not meet the distributed systems program goals. Today there is not enough funding for this effort.
Network Support	-	How do we get the field trained to support all our products. What tools are needed and when?

With the strategy to level off specific operating systems, we must expand some basic communciation functionality first. The issues are:

a) Which systems stabilize at what level of functionality?

b) What topology problems does this creat in FY '80 and 81?

c) Are we mature enough to really make this happen?

With all of the product spectrum, how do we sell our products? We have network profiles, customer support plans, and P/L sign off in place now. Is this enough? Do we have the dicipline to implement this?

With distributed access technology available by FY '81, the interaction between networks, RMS/DBMS must be understood in FY '79. Resources must be made available to attach this problem.

2.5 Change in Emphasis

There is basically no change expected in the market except for expansion because of greater user awareness, and better understanding through experience on our part. This has caused a change in our product offerings (e.g. , X.25, SNA, distributed database) and how we interact with the rest of the company. As a result, in FY '78 we broadened our program scope to invest time and resources to address our involvement with Software Services, Field Services, Promotion, and other operating systems groups, Sales, Educational Services, and the Product Lines. We consider the Sales, Support, and Promotion areas to be as crucial to our product's success as the Development activities.

3. PRODUCT CALENDAR

The Product Calendar (see EXHIBIT 1) represents an in-process snapshot of the current product evolution. More work is necessary to refine this thinking and integrate it with the various operating system strategies beyond FY '79. For this reason it must be considered preliminary at this time. However the requirements to publish are real, and it can serve at least as a point of departure for further planning.

4. REVENUE

4.1 Revenue in FY '81 Compared to Now?

In Q1 of FY '78 we compiled a business forecast for DECnet and our internet products. It showed that roughly 40% of our revenue came from DEC to IBM while 60% came from DEC to DEC. Since then X.25 has become more widely accepted and we would see about 25% of our DEC to DEC business going to X.25. From this assumption we get the following node forecasts:

	FY79	FY80	FY81	TOTAL	%
DEC - DEC (DNA)	1160	1580	1912	4652	50
DEC - DEC (DNA+X.25)	0	175	638	813	9
DEC - IBM (SNA+BSC)	780	1210	1830	3820	41
			TOTAL	9285	100%

4.2 Effect of New Products?

Products with strong market pull will have an effect sooner than those instigated by technology push. Other features are knock-offs -- we must have them to stay around. The following features are classified:

Market Pull	Tech Push	Knock-off
X.25	Routing	SNA
Virtual Terminals	Security	
Low End DECnet	Maintainability	
Auto-dial		
Multi-drop		

4.3 Lost Revenue

The following represents possible lost revenue to the company:

The major un-done (or unfunded) project in FY '79 is an X.25 corporate product. The revenue will probably be covered by the TELCO-direct product, at least in part for the short term. However, there are several aspects of the product that a P/L direct product need not address as major issues:

+ Documentation
+ Support Plans
+ Promotion
+ Universality of Approach
+ Adaptability

The longer these issues are unaddressed, the larger the backing of development costs to ultimately address them. It will cost us more in FY '80 to make the TELCO X.25 project a corporate product than if we do it in FY '79.

5. INVESTMENT

5.1 Flexibility to Respond To the Unexpected?

There is virtually no flexibility in our present funding. In addition, we invest only $200K for advanced development in FY '79. This is inadequate in an area so needing advanced development. We are constrained heavily by the size of our budget. Our requested funding has been cut by $300K to $3.5M for Hardware and Software. We are very tight in matching our investment dollars to our broad range of products.

5.2 Costs to Complete Projects in Place by the End of FY '78

	OOD $	POT $
Product Management.	$340	$ 60
Architecture/Adv. Dev.	200	-
Product Support.	400	-
Contingency	-	200
Phase II Product Development in place	-	2172
(DECnet M/S, D/IAS, RT SCS, TPS, M+, VAX (V1.0) 3270/3780-VAX)		
Product Development to start (VAX V2.0)		268
TOTAL --	$ 940	$ 2700

Project funding for FY '80 has not yet been determined by the POT. This process will be done once the FY '79 budgets are solidified.

DECNET PRODUCT CALENDAR

OP SYS	FY79	FY80	FY81
RSX-11M	DNA (Autodial, Multidrop, improved File Access, Simple Routing)	SNA X.25 Corp. Product DNA (Complex routing, RMS interface, simple VT)	Expanded File Access Perhaps Dist. DBMS
RSX-11S	SNA X.25, 3271 P/L Direct	All products coresident together	X.29 for term handling
M+	DNA (Same as RSX-11M) 3271	Same as RSX-11M	Same as RSX-11M
TRAX	DNA (M-like in maint. mode, TASK-TASK for TST) 3271 P/L Direct	X.25 Transparent Transport DNA Expansion for SCS	SNA Transparent Transport
SCS	DNA (Phase II DECnet only) 3271	DNA Expansion to M Level Expand User interface for TRAX	X.25 Low End SNA
TOPS-20	Total P/L Funding DNA (TASK-TASK, File XFER, RJE, Block Mode Terms)	Expanded DNA to Routing, Homogeneous VT X.25 Corporate Funding	SNA Interface Expanded DNA X.29 for Term Handling
PDP-11	DNA (Phase II DECnet)	DNA Expansion RT-11 X3, X28	Low End SNA
VMS	DNA Same as M/S 3271/3780 with Trans I/F Expanded Device Support	DNA Same as RSX-11M X.25	SNA X.29 for Term Handling Perhaps Dist. DBMS
RSX-11D IAS	DNA Same as M/S	Maintenance Only	Maintenance Only
RSTS	DNA (Autodial, Multidrop, Homo Virtual Terminals, Add'e Device Support) 3271	DNA File Access thru RMS Additional Device Support	Maintenance Only
RT-11	DNA (Autodial, Multidrop)	DNA (Homo VT to RSX only) Emphasis switched to PDP-11	Maintenance only

EXHIBIT 1

SECTION II

COMMUNICATIONS HARDWARE

II. COMMUNICATIONS HARDWARE

1. Markets

1.1 Communications hardware exists for the purpose of allowing a serial interconnect between two machines. These machines can be either a computer or a terminal over local or remote (common carrier links) which are usually asynchronous and computer-to-computer links over local, remote and multipoint, which are usually synchronous links. As the terminals become more and more computer-like (intelligent terminal), more and more synchronous links per machine will be required.

Communications hardware can be defined as existing in three areas. The first is that of a peripheral to a host CPU where the host CPU performs all the communications process. This has been the traditional market for DEC communication products and is the one we have focused our entire effort on. This peripheral hardware must cover a range of low performance to high performance, to encompass the communications needs of machines from 11/70 and VAX to 11/04's.

Communications hardware can also be defined as a complete system with CPU which is utilized to off load the host CPU (front end). While this can and is often made of general purpose CPU's with normal peripherals, it is a specialized market which some specialized vendors (e.g., COMTEM) perceive as CPU's built expressly for that purpose.

While DEC utilizes communications hardware coupled with small CPU's (11/40) to front end machines such as PDP-10's, we have not developed the concept for the smaller 11 series because of the high cost involved which can only be justified on large machines. We have also not chosen to market such systems for use on other large CPU's since that involves heavy application programming effort and software customizing of systems.

The last segment of the communications hardware business can be defined as the stand-alone system which provides a specific service (TDM's, concentrators) which are utilized to reduce line costs. These stand-alone products again have not been part of a communications hardware strategy because of the turnkey nature of the business and the lack of a sales force dedicated to that market.

Our participation to date has been as a supplier of peripheral interfaces to our computers.

1.2 Technology

The following technology assumptions can be made:

(a) Advancing technology permits the medium and low end to benefit from smart microprocessor-based communication interfaces which have already proven their ability to improve performance and simplify communication software at the high end.

(b) This will allow a large cost reduction in the front end machines making them more viable for the mid-range machines (i.e., the front-end machines become a microprocessor on the same bus).

(c) The very low-end peripheral communications market will be gradually phased out in favor of bounded systems which integrate the communications function within them.

The availability of smart communication interfaces (KMC-11's) implies that we must quickly move a portion of the driver software into the intelligent interface. If we do not, our software system performance will not keep pace with competition since they will have done this.

Also, we must move into the modem area to thwart the effect of add-on vendors for the communications peripheral and provide more DEC-added value to our systems.

2. Product Goals and Strategy

2.1 Goals -- The product goals can be outlined as follows:

(a) Complete the family of low cost UNIBUS interfaces. Where added performance is required, a KMC or DMC microprocessor will be utilized to enhance performance.

(b) Where specific intelligent high-volume products can be defined, use the KMC microprocessor to perform those functions and provide the front-end functions with this technique.

(c) Develop a set of compatible, intelligent multi-point DDCMP interfaces and adaptions for both UNIBUS- and QBUS-based systems and for terminals. These products will provide an intelligent error-free interconnect mechanism for both local and remote networks and will integrate the line driving function within the device. This will provide ease of connectability for all DEC systems and terminals. This is shown in Fig. 1.

(d) Continue to develop a modem capability for higher speed modems and to have this modem capability at the CPU end as well as the terminal end.

Table 1 shows the funded projects which meet these goals.

2.2 Strategies/Alternatives

We have chosen to base our complete interconnect capability on a high level protocol throughout the interconnect space rather than optimize comm devices for a particular type of application (local only). This leads to some inefficiency and non-optimized products, but does lead to fewer product types. For example, a cimpler protocol could have been utilized for the local connection. This would have resulted in a lower cost local-only product, but more different products to produce forecast and support.

We have also concentrated for our own DEC interconnect, on the DDCMP protocol to assure that we will not be driven by outside influences. We understand that we must maintain connectability with other vendors, and have assured that our basic hardware has the right features and will implement foreign machine connection in writable control store microcode within our microprocessor driven interfaces.

3. Product Calendar

Product	Description	Goals From 2.1	FY	FY79 Cost($K
DZ11-H	DZ11 with increased modem control capability	a	'79	60
DML11	4-line synchronous mux	a	'79	230
DMP11	UNIBUS full DDCMP synchronous interface with local line driver	b-c	'79	220
DMV11	Q-BUS full DDCMP synchronous interface with local line driver	b-c	'80	200
KMC11-B	Enhanced KMC11	a-b	'80	40
DMV-11	Microcode Development	b-c	'80	50

- (funding limit FY '79)

Product	Description	Goals From 2.1	FY
212 Modem	1200 BPS full duplex asynchronous modem	d	'81
801 Dialer	Allows CPU to originate dialing	d	'80
New DL11	Enhanced DL11 to eliminate variations	a	'80
Terminal Module	Interface to intelligent terminals to allow connection to DEC CPU's easily	c	'81
Low cost KMC	PDP-11 ISP version of KMC lower in cost	a	'81
Low cost DMP	Lower cost DMP product	a	'81
201 Modem	Synchronous modem for inclusion in DEC systems	d	'81
Modem card cage	Rack mount of modems in CPU's to add greater value to DEC interfaces	d	'81

4. Revenue

Communications hardware in FY '78 represents a $60 million business for UNIBUS alone. This revenue can be expected to maintain and even increase as a percentage of system sales, with the greater emphasis on distributed processing and networking. Even at a constant percentage of CPU business, communications hardware is expected to represent a $100 million business by FY '81.

5. Investments

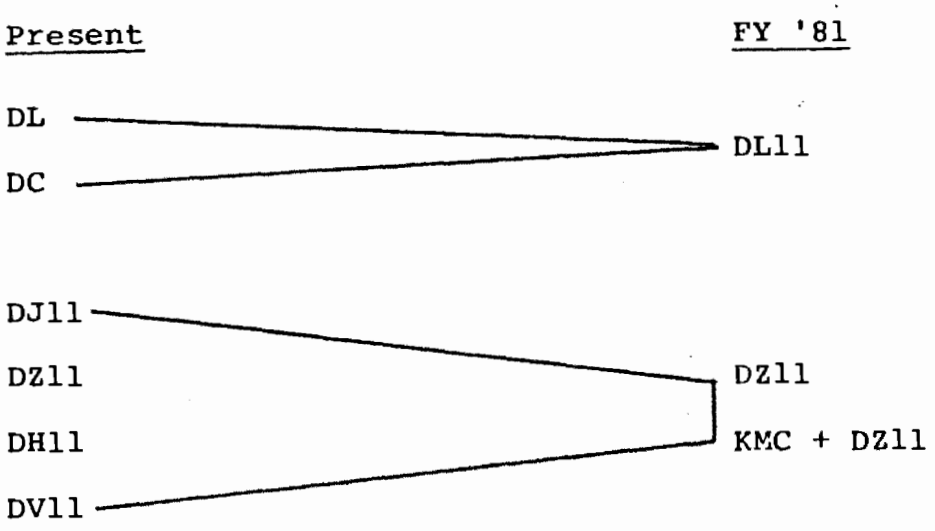
The costs to complete communications hardware projects in place by end of FY '78 are:

	OOD $	POT $
Product Management	100K	
Advanced Development	90K	
Product Support	510K	
Contingency		40K
Product Development		760K
	700K	800K

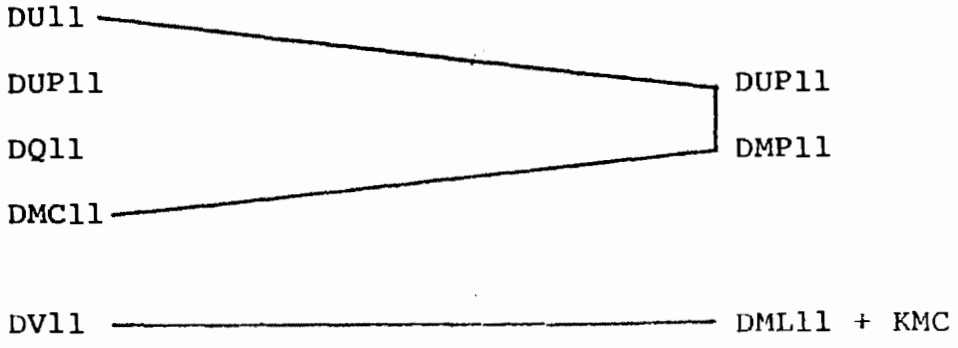
APPENDIX A

Product Evaluation

UNIBUS ASYNCHRONOUS

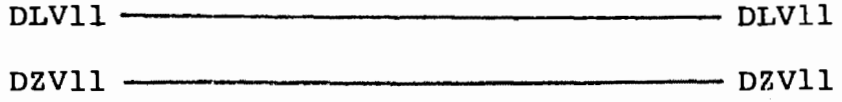


UNIBUS SYNCHRONOUS

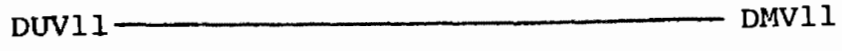


Q-BUS

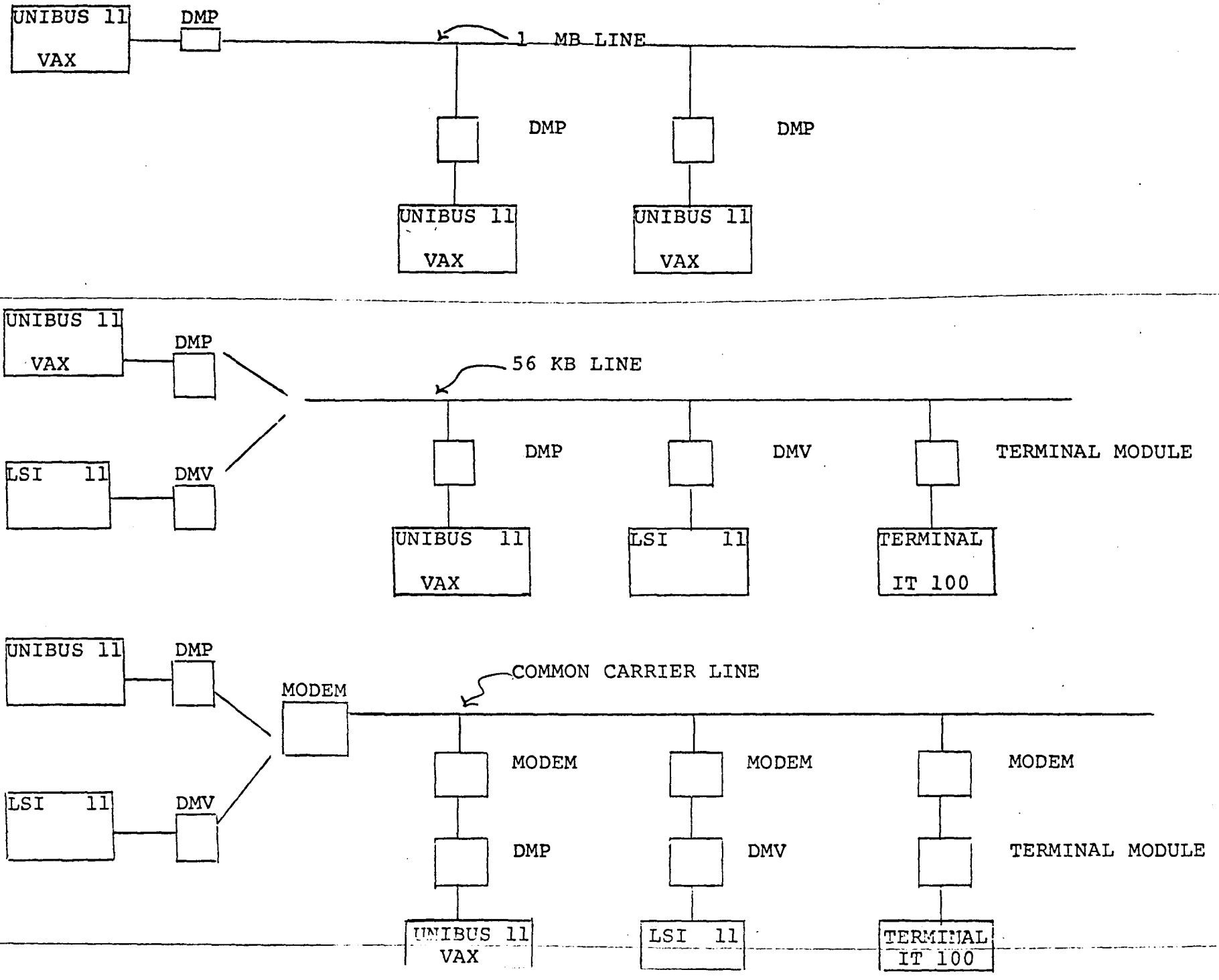
Asynchronous



Synchronous



COMPLET ONNECTABILIT F DEC SYSTEM



VII. Storage Systems

STORAGE SYSTEMS

RED/BEIGE BOOK

A Summary of Mass Storage Business Strategies, Product Tactics, and Competitive Trends

May 23, 1978

COMPANY CONFIDENTIAL

Ken Sills
ML1-3/E58
DTN: 223-5805

STORAGE SYSTEMS RED/BEIGE BOOK

TABLE OF CONTENTS

DESCRIPTION OF RANDOM ACCESS PRODUCTS

DEVICE	FORMATTED CAPACITY (Mb)	FIXED/ REMOVABLE	FCS	INTERFACE METHOD (1)	TRANSFER COST ($)(2)
BLOCK FORMATTED TAPE					
TU58	.25	R	Q2,FY79	TU58	200
FLOPPY DISKS					
RX01	.25	R	shipping	QB,UB,OB	744 (FY79)
RX02	.5	R	Q1,FY79	QB,UB,OB	-
RX03	1	R	Q4,FY79	QB,UB,OB	900
RX0X	2-4	R	?	QB,UB,OB	1000 (?)
LOW-END DISKS					
RK05J/F	2.5/5	R/F	shipping	QB,UB,OB	1400
RL01	5.2	R	shipping	QB,UB,OB	1119 (FY79)
RL02	10	R	Q4,FY79	QB,UB,OB	1250 (FY79)
50Mb Removable	50	R	FY81	NDS	1500-2500 (3)
AZTEC	4-8	R	FY81t	QB,UB	500
MID-RANGE DISKS					
RK06	14	R	shipping	UB	2366 (FY79)
RK07	28	R	shipping	UB	2445 (FY79)
RM02	67	R	shipping	MB	6127 (FY79)
RM03	67	R	shipping	MB*	6152 (FY79)
150Mb Removable	150	R	FY80 (?)	NDS	5000-8000 (4)
R80	143	F	FY80	MB,NDS (5)	4400,2700
R81	286	F	FY81t	NDS	2700
HIGH-END DISKS					
RP04	88	R	shipping	MB	10800
RP05	88	R	shipping	MB	11100
RP06	176	R	shipping	MB	10700
RP07	292	F	Q1,FY80	MB	9300
RP07+/08	542	F	FY81	MB/NDS	10000
FIXED HEAD DISKS					
RS03/04	0.5,1.0	-	shipping	MB,UB	5000
CONTROLLERS					
NDS	N/A	N/A	FY81	NDS	2000
Small NDS (UDA)	N/A	N/A	FY80	UB	500

NOTES:
1. QB = Q-BUS OB = OMNIBUS UB = UNIBUS MB* = CPU INTEGRAL MB ONLY (NO RH11)
   MB = MASSBUS OR UB VIA RH11 NDS = NEW DISK SYSTEM
2. All costs are the projected averages of first 3 years shipments except otherwise noted.
3. The 50Mb removable transfer cost is based on RL05 ($1500) or RK08 ($2500)
4. The 150Mb removable transfer cost is based on RP06/NDS ($8000) or RM04 ($5000)
5. The first year of R80 shipments will be Massbus only

DESCRIPTION OF 1/2" TAPE PRODUCTS

Tape Drive	Density (BPI)	Speed (IPS)	FCS	Interface Bus	Slave Transfer Cost* ($000) Master/Slave
TS03	800	12.5	shipping	UB	2.0/1.6
TS04	800/1600	45	FY79	UB	2.7/2.7
TU10	200/556/800	45	shipping	UB	3.5/3.0
TE16	800/1600	45	shipping	MB	5.3/3.0
TU45(CSS)	800/1600	75	shipping	MB	7.4/5.0
TU70(LCG)	800/1600	200	shipping	-	35.0/12.0
TU72(LCG)	1600/6250	125	shipping	-	35.0/12.0
TU77	800/1600	125	Q2,FY79	MB	9.0/6.5
TU78	1600/6250	125	FY80	MB	12.0/7.5
TS6250	1600/6250	22-45	FY81t	NDS	6.5/3.3

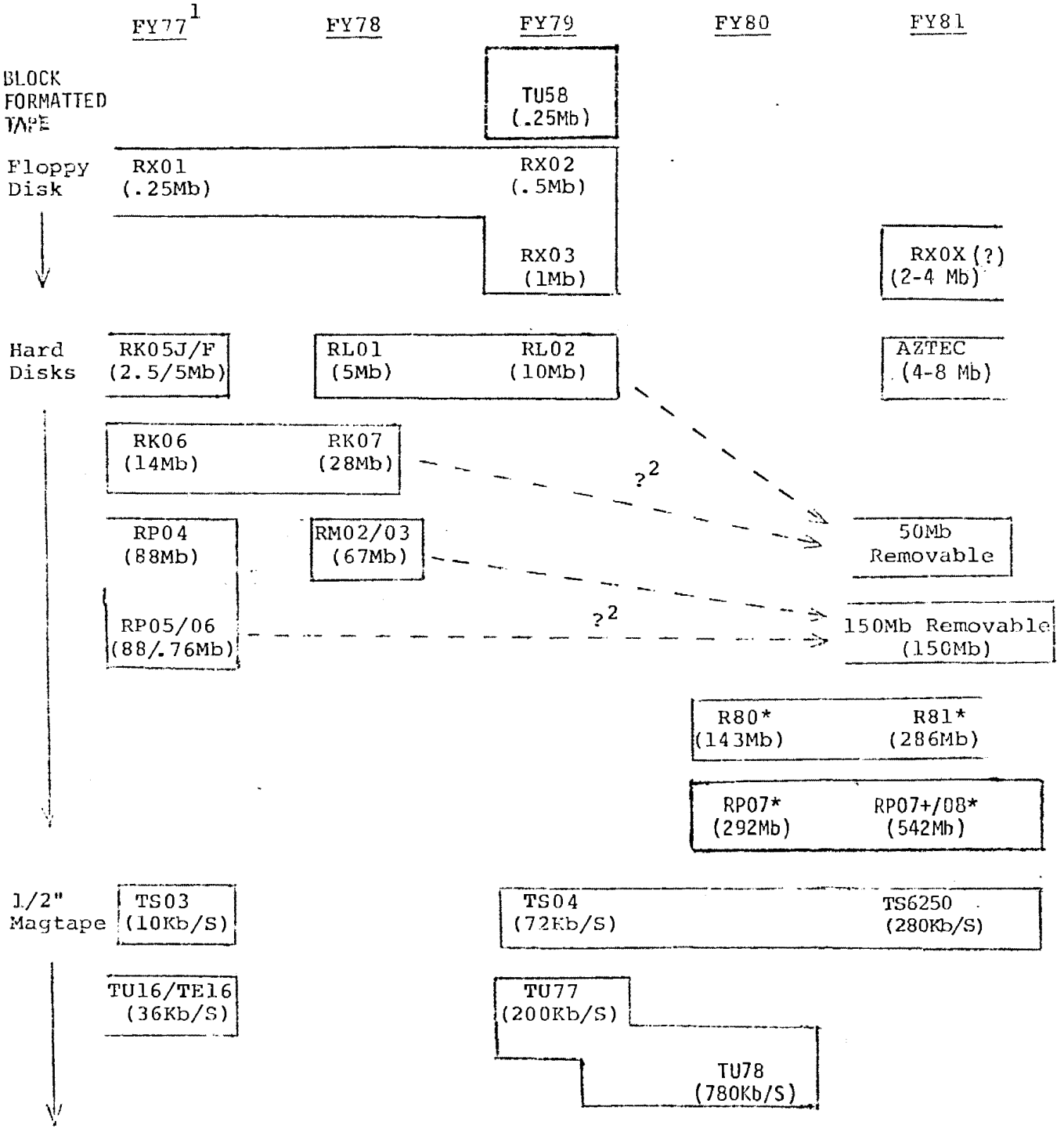
UB = Unibus

MB = Mass Bus or UB via RH11

NDS = New Disk System

* Costs of future products are targets

MASS STORAGE PRODUCT TIMING AND FAMILIES
(Available At End Of Fiscal Year)



* Fixed media disk drive

1. All available products shown to establish baseline
2. Only 1 family will evolve to FY81 product. Decision is currently being analyzed.

II. BASIC MASS STORAGE STRATEGIES

A. Strategy:

We must invest in, and build on, the latest available IBM disk technology. It is required for competitive mid-range disks which are projected to be the largest revenue producing disk class. This technology is the foundation for building new disks across the entire product spectrum.

Comment:

We cannot afford to be competitive in both fixed and removable media mid-range and high-end disks. Our resource limited strategy is to lead in fixed media in the mid to upper capacity ranges. We are concerned about the resulting removable media competitive hole and how rapidly our customers will accept fixed media.

This fixed media technology is currently "Winchester" which is a head/media technology that allows lower head flying heights with resultant higher recording densities. The media is lubricated and allows contact start/stop of the lightly loaded heads. The benefit of Winchester is high reliability at low cost/byte. The first DEC built product to employ this technology is the R80.

B. Strategy:

We must and can build both competitive rigid and flexible products at the low-end by exploiting both DEC and IBM technologies. This assumes that IBM will continue to introduce new technology at the high-end and migrate it downwards over time.

Comment:

We will continue to emphasize low-end disk development. However, we cannot afford to pursue both flexible and rigid technologies. We have selected the rigid technology AZTEC over the RX0X and are concerned about the increased risks, limited alternatives, and our competitors' substantial efforts on high capacity flexible media. The exposure is that floppies offer a less expensive and more "shelf storable" media for personal storage and software distribution.

We can be competitive, and in fact, offer leadership low-end hard disk products by migrating high end technologies or developing new technologies into low-end products faster than competition. The RL family and AZTEC low-end efforts are examples of this strategy.

In general, DEC volumes of low-end storage products are sufficiently high to allow manufacturing economies of scale to produce costs close to those of IBM.

C. Strategy:

It is difficult to build high-end disk products that are cost competitive to IBM. Therefore, we must use a combination of tactics:

1. Subsystem intelligence.

2. Aggressive early buyout or early reverse engineer/license.

Comment:

The difficulty in being cost competitive to IBM is that IBM introduces new technologies in high-end disk products first. IBM also has much greater unit volumes producing manufacturing economies. Since there are several reliable sources of large disk products (e.g. Memorex, ISS/Sperry Univac, Control Data), we will buy their basic product offerings for early introduction (e.g. RP07). We will also differentiate our large disk offerings from competition by using subsystem intelligence (e.g. NDS).

D. Strategy:

Our position is to be able to evolve into building high-end disks. This is not a change in the current priorities which dictate buyout of high-end disks. The build/buy decision is based on:

1. Availability of development and manufacturing resources.

2. Competitiveness and reliability of suppliers.

3. Business economics:

   - Product Line contribution
   - Return on assets
   - Cash flow
   - Unit volumes
   - etc.

Comment:

High-end disks are defined as those having more than four platters. There is some question as to whether DEC's volumes for this size of drive (billions of bytes in 1980's) will warrant the high development expense associated with it. However, we will continue to evaluate the financial attractiveness of such an investment.

E. Strategy:

We must offer 6250 GCR technology 1/2" tape products as they will be the industry interchange standard. We will build a low-end 1/2" tape competitive product for low entry cost, and buy-out at the high end for complete product coverage.

Comment:

The first low-end GCR (group code recording) product will be the TS6250. Due to funding limitations, it will not be as competitive as we desire. The buy-out product offering is the TU78 (which succeeds the very costly TU72). Strategy statements C and D are equally applicable to tape products.

F. Strategy:

We will maintain a floppy offering, competitive with the independents, by tracking capacity increases.

Comment:

Insufficient development funding precludes floppy disk development past the RX03 1 Mb product at this time. The level of funding for advanced floppy disk development will only maintain the nucleus of the team, track technology, and develop basic techniques pertinent to any new floppy disk development.

G. Strategy:

Because of the high risks, we will pursue both the RX0X and AZTEC with one product emerging as a lower cost replacement for the RL01.

Comment:

The product line preference is for the AZTEC (higher media cost, higher performance, relative to floppy). Advanced floppy disk product development will proceed at a minimal level.

H. Strategy:

Our long term strategy is to build intelligent storage subsystems combining both tape and disk products.

Comment:

The first offering of the NDS intelligent controller will probably not include tape. However, the mix of disk and tape is planned for future generations. Off-line (relative to the host CPU) archival backup and other off-line storage manipulation tasks are recognized as an attractive feature as well as being critical to the availability of the total system.

I. Strategy:

Strategic pricing will be reviewed by the POT. It will consider:

1. Competitive situation.

2. Total in-field costs

   - Manufacturing investment
   - Spares cost
   - Training
   - Introduction costs
   - Development costs
   - Inventory
   - Phase-in/phase-out costs

3. Contribution, ROA and other Product Line measurements.

Comment:

For example, this is recognition of the fact that buy-outs can be priced with significantly lower markup than DEC builds, and still have excellent profitability. Another pertinent example is that the life of products can be profitably extended by dynamically lowering the price over time.

J. Strategy:

We must be able to rapidly respond to all relevant IBM mass storage announcements by early buy and analysis of the entire IBM subsystem.

Comment:

Insufficient funding will preclude us from acting on this strategy without reprioritization of projects. We believe that an IBM large disk announcement is imminent and that this disk will use advanced technologies which could be profitably reverse-engineered into the products which we manufacture.

III. GENERAL MASS STORAGE SUBSYSTEM TACTICS

The following general tactics address the implementation of the previously outlined Mass Storage strategy.

A. Offer very low entry cost random access storage by employing block formatted tape cartridges

Market these products in several ways:

1. Component Level - These "kit" sales will be accomplished in conjunction with component level CPU sales. Markets encountered are generally highly skilled OEM's who embed our small CPU's and now micro-peripherals within their product. The top end of these applications would be more prone to floppy based systems for access time.

2. Rack Mounted - The major market here is for use in development systems for our intelligent terminal business. Other uses include industrial applications where bays of A-D type equipment are needed for monitoring processes but the mass storage needs are minimal, i. e. for program loading or data exchange for down line processing.

   Another potential here is to replace 1/2" tape on disk based systems where the tape drive was used only for program loading and update.

3. Imbedded in Other Products

   a. Intelligent terminals - for local processing and business management. In these situations entry cost and size of the TU58 will be key features.

   b. Store and forward buffer - for local store and forward buffer as well as archival storage in message transmission applications. The low end of this market will be served by electronic RAM storage; however, for both archival and data security reasons block formatted tape will exhibit a higher level of acceptance.

   c. Software and diagnostic update - when embedded within our larger CPU products block formatted tape will become a corporate solution for a multitude of update distribution media types.

      A major embellishment of this capability will be the use of block formatted tape by our OEM's to distribute both application program updates as well as sell new software features.

d. Personal media - A major segment of the block formatted tape market is personal media. In this application, programmers will use dumb terminals for program development but will want to retain a copy of their program by dumping the software onto a small media which they will carry away.

B. Offer low-end subsystems with only removable floppy or hard disks for the following reasons:

- A two drive removable disk subsystem offers significant performance and availability advantages at a small cost over "fixed plus removable" on a single spindle.

- The amount of data backed-up or archived is usually economically managed with floppy or cartridge disk media.

- Fixed media disks using Winchester technology do not have significant cost advantages over removable media in low cost subsystems (See Section B which follows).

We will, however, continue to examine a F+R disk as the "50Mb removable" product offering. The F+R product offers the lowest entry cost for a backed-up subsystem, albeit at the expense of performance and availability.

C. Offer mid-range subsystems with:

- primarily, fixed and removable disks

and

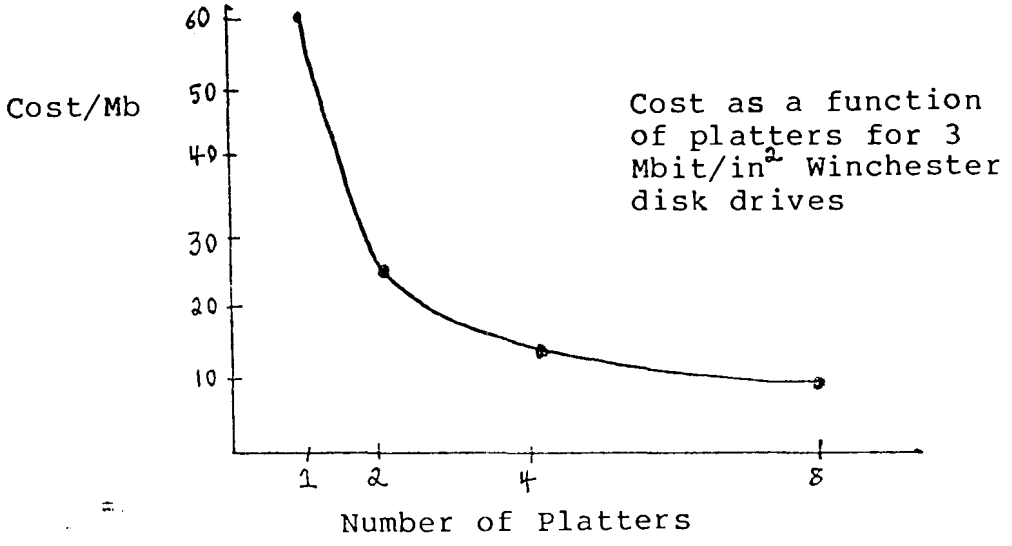
- secondarily, fixed disk and low cost tape

The rapidity of the evolution to the fixed disk and tape subsystem will depend on the attractiveness of our backup routines and on how fast our customers begin to feel comfortable with not having removable disks on their systems. IBM is currently making this transition with their low-end customer base.

1. Fixed media for:

a) Capacity - the typical Digital medium and large interactive application has data permanently mounted on 75% of the available disk drives, i.e., 75% of the on-line data in a typical application is amenable to fixed media.

b) Cost - "Designed from scratch" mid-range fixed media disk drives produce a cost/byte saving of over 50% compared to a removable media disk of equal capacity. In particular, Winchester technology disk drives using the HDA, or head/disk assembly principle become very economical in the 2 to 4 platter range. A cost model used by the Mass Storage Group demonstrates this fact:



Cost as a function of platters for 3 Mbit/in^2 Winchester disk drives

c) Reliability - the more sealed environment of a fixed media drive reduces susceptibility to harmful contamination. There is also no potentially damaging human handling. These factors result in a fixed media drive MTBF which is typically double that of its removable counterpart.

2. Removable media for:

a) Interchange, i.e., transfer of data from one system to another.

b) Data backup - this is particularly important when fixed media drives are used, since the "fixed data" cannot be backed up by simply putting the pack or cartridge on the shelf.

c) Software distribution - on qualified low cost media devices on systems which are configured without tape. Where frequent software updates are expected, disk is still an inferior distribution media having a media price which is an order of magnitude greater than tape. (The TU58 cartridge is an ideal software update medium.)

d) Portable storage, e.g., a user mounted personal data base or program library.

3. Magnetic tape for:

a) Archival costs - where considerable archival storage or backup is required, the media cost of tape becomes attractive.

b) Interchange - to other DEC or other manufacturers' systems using industry standard format.

c) Software distribution - tape is a more cost effective distribution medium given it is already on the system.

d) Processing - certain applications process data sequentially and can effectively use tape. Tape is an ideal device for journaling of transactions, an increasingly important backup method.

D. Where fixed and removable subsystems are configured, maintain a basic subsystem fixed/removable ratio of less than 10X, and aim for 2X to 5X. The ratio will increase on larger capacity subsystems since it is felt that the subsystem removable capacity need only be sufficient to hold 50% of the software distribution requirement, i.e., distribute software on a maximum of two physical media. This ratio goal assumes:

1. Large systems with archival backup requirements will use tape due to the lower media cost.

2. Volume backups will become less frequent due to new incremental backup and journal routines.

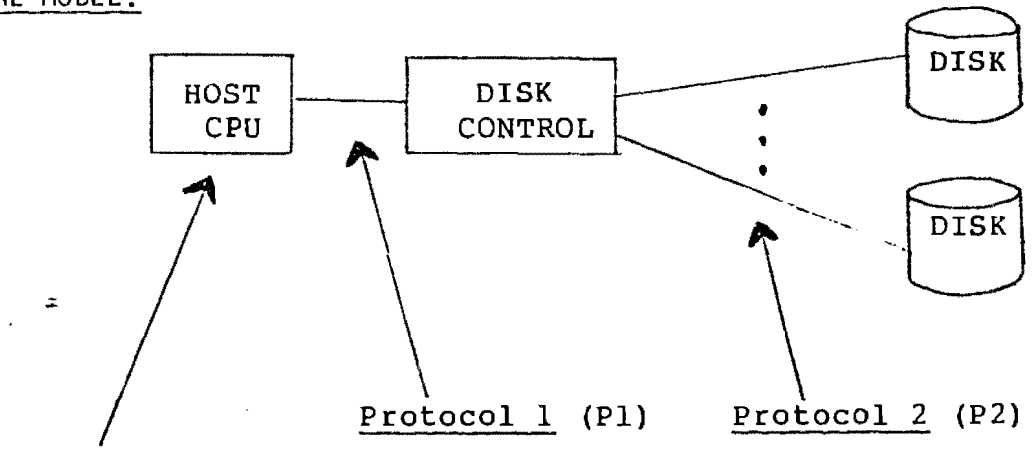
E. Offer high-end subsystems with primarily, fixed disk and high performance tape. Removable disks will be added where the "removability" feature is required. We believe that this class of system will usually require tape for one or more of the previously mentioned reasons. It is therefore unlikely for removable disks to be used as a primary backup device, especially given the very large capacities (>500Mb) per spindle that are "just around the corner". The removable disk, if needed, will probably hold databases for tasks that are executed infrequently.

Coupling the above with the fact that large removable disks are more costly on a per byte basis and less reliable than fixed media, we have concluded that removable disks larger than the current RP06 are not warranted. This belief is supported by talks with our vendors and customers.

F. Evolve to a Unified Mass Storage Subsystem Strategy. This will lower development costs (hardware and software), allow a high level of configuration flexibility at overall lower product costs, and produce generally higher functionality subsystems. The first phase of this evolution involves disks, with tape products being integrated into the standardized subsystem at a later date. The integration of tape is an advanced development in FY'79 and, therefore, will not be explored further in this discussion.

The disk controller strategy has three specific performance/functionality levels, each of which conforms to two distinctly specified communication protocols:

GENERAL MODEL:



Protocol 1 (P1)

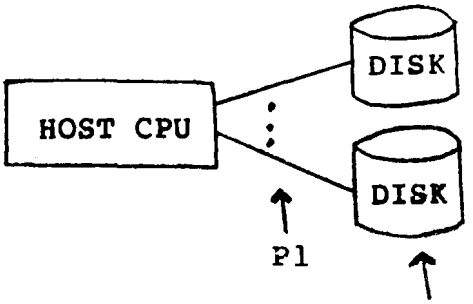
one device class (e.g., disk) driver/ handler

subsystem oriented control messages, status replies, and parallel data transfers

Protocol 2 (P2)

device level control, status replies, and serial data transfers

Level 1 - lowest entry cost for price sensitive small systems, low performance, low functionality

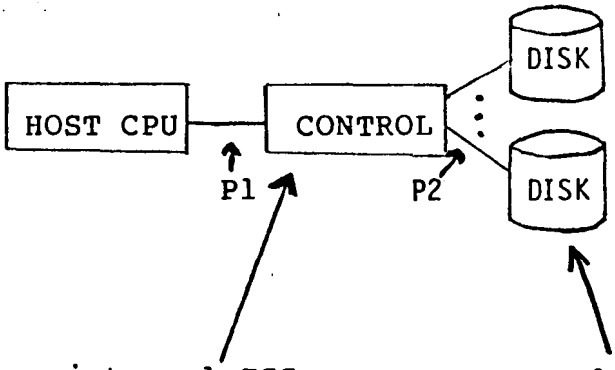


disks
AZTEC
50 MB Rem (?)

controller
none

Integrated control and drive electronics containing ECC and drive diagnostics. Possible shared logic and cooling with multiple spindles sharing one box.

Level 2 - economical low to mid-range subsystem where high performance and availability are not critical



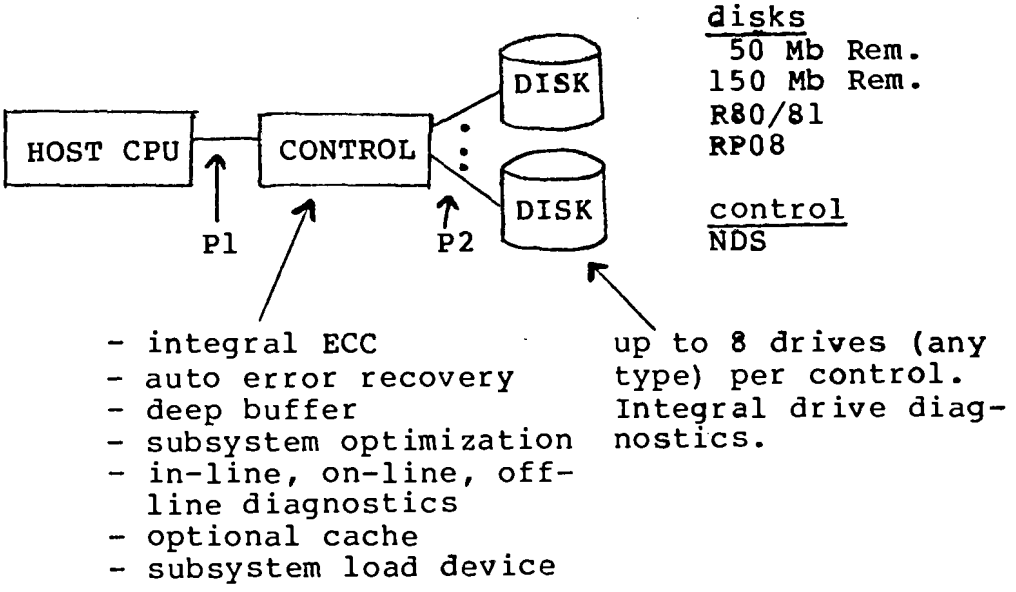
disks
50 Mb Rem.
150 Mb Rem.
R80/81
RP08

control
Small NDS (UDA)

- integral ECC
- auto error recovery
- small buffer
- off-line diagnostics

goal of up to 4 drives (any type) per control. Integral drive diagnostics

Level 3 - high performance and functionality intelligent subsystem for state-of-the-art mass storage applications



G. Operate with a "seven product strategy" in the FY79/80 timeframe. These seven products (product families) cover the entire range of Mass Storage requirements:

RX02/03	floppy disk
RL01/02	low-end cartridge disk
RK07	mid-range cartridge disk
RM03	mid-range high performance disk
RP06/07	high-end disks
TS03/04	low cost 1/2" magtape
TU77/78	high performance 1/2" magtape

H. Four removable disk products will be necessary in the future. The spacing is such that each successively larger subsystem has a cost that is about two to three times its predecessor.

	Approximate Cost	Capacity (Mb)
1. Dual Floppy (or AZTEC) subsystem	$1000	<10
2. Dual RL02 subsystem	2500	20
3. Dual 50Mb drive subsystem	5000	100
4. Dual 150Mb drive subsystem	14000	300

Cost effectiveness for the 150Mb product is not a high priority goal. In fact, there are no development funds in the FY79 plan for this class of product but several promising opportunities are being explored. The potential volumes of the large removable are highly dependent on the customers' acceptance of fixed media, a factor for which we do not have a quantitative feel for at this time.

I. Do not develop new, dedicated or optional fixed head disks. There are better alternatives on the horizon to satisfy current, very expensive fixed head disk applications.

1. Solid-state devices - bubbles and CCD's are significantly more reliable and will soon be more economical than fixed head disks. These solid state products will find immediate application as very fast swapping devices, and possibly as disk caches.

2. Fixed-head option on Winchester technology disk drives - lower cost/Mbyte than dedicated fixed head drives but significantly lower cost/performance than CCD's (to be used a subsystem controlled cache) or even main memory (MOSRAM). A fixed head option of 1-2 Mb is insufficient size for either a paging device or fast store for index tables. The way to efficiently utilize a memory of this size is to manage it as a disk cache. However, using a FHO as a high priority swapping or cache device would "paralyze" the moving head portion of the disk since the disk generally cannot seek while the fixed head area is transferring or in latency wait.

IV. MASS STORAGE PRODUCT TACTICAL PLAN

A. Block Formatted Tape

The horizon of personal portable media has been expanded by the introduction (6/5/78) of DECTAPE II, the TU58. Initial application will be in the PDT 11-130, a new intelligent terminal.

In a cost effective way ($218 for dual drive component level in FY'79) the TU58 will:

1. Provide a new low-end entry level of mass storage in support of a new entry level of intelligent terminals.
2. Provide mass storage capability that is price compatible with our component level CPU sales.
3. Provide a corporate software update distribution solution.
4. Provide a corporate diagnostic and/or microcode update distribution solution.

The TU58 strategy is to:

1. Maintain 4:1 cost/performance with Digital floppy products.
2. Provide a product small in physical size for easy mounting within other terminals.
3. Be block addressable to encourage systems applications.
4. Sacrifice media cost to obtain lowest possible unit entry cost.
5. Minimize power requirements and complexity.

B. Floppy Disks

The strategy in the floppy disk area is to:

1. Exploit standard media.
2. Extend the systems market space downward (e.g., the success of the DS310, 11V03 and VT78).
3. Cover the low-end market space with the smallest number of products.
4. Offer broadly applicable, low cost, high reliability volume products.
5. Be cost and technology competitive with the independents.

Floppy disk cost/performance is improving at approximately 50%/year. This extremely high rate is reflected in "frontier" products, i.e. the best offering in the marketplace, which double in capacity every year for the same $900 cost for a two drive subsystem.

We will track these increases by offering in FY79 the RX02 double density .5 Mb drive and the RX03 double density, double sided 1.0 Mb drive.

The major contingency in the RX03 Q4 FCS commitment is availability of heads from outside vendors which solve the industry wide two-sided media wear problem. The acceptance of a lower specification level for media wear in RX03 applications is another alternative. The technology to design such heads is not a part of the RX03 project, as our plan is to continue to procure floppy heads.

The RX03 is committed to maintaining IBM compatibility. However, a major issue is at what density this compatibility exists, since the RX03 will write floppies which can be read on RX01 and RX02 drives. There are several areas of conflict here which are being investigated. Also, multiple opportunities for RX03 "enhancement" exist:

1. Universal power supply.
2. RX02 cost.
3. Better packaging, cooling.
4. RX02 field upgrade.
5. Better serviceability.

However, these changes to the product will impact both the development cost and schedule.

Larger floppies than the RX03 cannot go into full product development at this time due to funding limitations. In addition, the access time of the RX02 and RX03 will be identical to the RX01 (175 Ms). Several of the competition have recently introduced floppies with seek times of less than 100 Ms. This compromise is, again, based on funding limitations.

C. Low-end Disks (1 platter devices)

The RL01 is a significant improvement over the RK05 in cost, performance, and reliability. However, the RL01 is relatively no closer to the "frontier" (set by IBM's low-end fixed media products) than the RK05 was at its introduction. The RL02 enhancement which will be shipped in the latter half of FY79 will move us much closer.

The RL02 will be the last "RL" class product to use the RL11, RLV11, and RL8A controllers. Future RL extensions will be NDS compatible, or may possibly have an integral controller.

Advanced development is proceeding on the AZTEC. The goal of the AZTEC is RL01/02 capacity, performance, and functionality at 50% of the cost. Reducing cost at the very low-end is difficult and requires radically new technologies. We expect the AZTEC to be transferred to a product development team in the latter half of FY79.

Funding limitations have prevented the RL04 concept from going forward on schedule. Since the RL04 schedule will slip given the current funding level, a study is currently being done to determine the best product to design given available resources in FY79. We have determined that the next "step up" from RL01/02 and AZTEC capacities is about 50 Mb per drive. There are several alternative ways to get to 50 Mb. Several attributes of alternative programs are relatively compared:

	Est. Product Cost (± 20%)	Development Cost ($ millions)	FCS
1. RL Family Extension	$1,500	2-3	FY81
2. RK Family Extension	2,500	1-2	FY80
3. Fixed + Removable	2,000	3-4	FY81

A fixed + removable product would serve the "lowest entry cost backed-up system" market requirement. Alternatives 2 and 3 are technically mid-range disk products.

In any case, Mass Storage believes in, and is committed to, the strategic goal to attain a leadership position in low-end disk products by the early 1980's.

D. Mid-Range Disks (2-4 platter devices)

The RK07 is significantly more competitive than the RK06 and will be a good product offering thru FY80. Further extensions to the RK family are possible but, with the exception of the 50 Mb possibility discussed in the previous section, are not being considered at this time. This is because allocation of scarce resources to an expensive in-house development effort of a >100 Mb removable drive is considered to be a poor investment.

The RM03 is off to a flying start. It has met with a high level of customer acceptance, has essentially obsoleted the RP04/05, and has impacted the RP06. CDC is beginning the development of an RM04 which is totally RM03 device level interface compatible (except for pack) and has twice the capacity. The RM04 would be available for us to FCS at the end of FY80. Current perceived problems with the RM04 specification are:

1. Probable low unit volumes for DEC.

2. No on-board diagnostics.

3. Minimal error data transmitted from drive (same as RM03).

4. Little parts commonality with RM03

We will continue to study the RM04 concept but no development funds have been allocated in FY79.

Question: Given CDC's commitment and the momentum of the RM03, can we now not offer an RM04?

The R80 fixed media, Winchester technology drive is the largest program for Mass Storage Development in FY79. It is designed to provide a highly competitive mid-range foundation. The mechanics of the R80 are being designed to be extendable to an R81 at double capacity. The 61 Mb 2 platter depopulated version of the R80 is still technically feasible but it is questionable whether this is a necessary product. The 61 Mb product is less than 50% of the capacity of the 143 Mb 4 platter version but is about 75% of the cost.

The R80 will be initially offered as a Massbus product by replacing the CDC drive in the RM03. Although this configuration has a cost which is over 50% more costly than the "OEM box" version, the OEM box requires an NDS controller for interconnect. It is probable that none of the NDS family will be available at R80 FCS. In addition, first year shipments of the R80 will be limited to about 1,000 units. The Massbus configuration is an excellent way to limit demand during production phase-in.

E. High-end Disks (>4 platter devices)

Since the RM03 has effectively replaced the RP04/05, the RP06 is the only economically viable "high-end" disk product currently offered. As the competitive graph (see Section VI) shows, the RP06 is not very price competitive with other systems manufacturers' high-end products. The RP07 fixed media product with FY'79 FCS will alleviate this situation.

The RP07 family of buyouts from ISS consists of the RP07 at 292 Mb with a Massbus interface, the RP07+ at 542 Mb with a Massbus interface, and the RP08 at 542 Mb with an NDS interface. The RP07 and RP07+/08 are 6 to 12 months earlier than the R80 and R81, respectively. However, since the R80 family are DEC built products, the R80 and R81 are more cost effective than the RP07 and RP07+/08, respectively. In addition, it is usually more attractive, given equal cost/Mb, to put a given capacity of data on multiple spindles for better performance and availability. Therefore, there is some question as to which members of the RP07 should be introduced, if any. LCG has expressed a strong demand for the RP07, so that program will continue. However, several RP07 program benchmarks have not been met and the scheduled FCS is now realistically Q1, FY80.

The RP07+/08 are essentially backup programs to the R81. The RP07+ will also effectively meet the large storage requirements of those older systems which do not support NDS (the R81 is planned for NDS only). The RP07+/08 program will continue but will undergo periodic go/no-go reviews based on its projected competitiveness vis-a-vis the R81.

As was discussed in earlier chapters, there is a need for an RP06 class removable product in the early 1980's. There are several alternatives for the "150 Mb removable" product which are relatively compared:

		Estimated Startup Costs	Product Cost	Future Feasible Markup*	FCS
1.	Current RP06	None	$10,700	2X	Shipping
2.	RP06 with NDS interface**	$1-3M	8,000 estimate	3X	FY'80
3.	RM04 on NDS	$4-6M	5,000 estimate	5X	FY'81

* A $25K price in early 1980's is competitive.

** No interchange with existing RP06.

Since the market demand for this product is relatively low (given an R80), no development funding has been allocated in FY'79 forcing alternative 1. However, alternatives 2 and 3 are being studied and the respective vendors have been asked to quote.

F. Disk Subsystems

The disk subsystems strategy as outlined in Section III-F is aimed at a small number of generalized controllers that replace the current practice of a different controller for every drive/bus combination. Two explicit projects are underway - NDS (New Disk System) and Small NDS. The cost goals are $2,000 and $500, respectively. The major functionalities of NDS and Small NDS are also outlined in the Section III-F diagrams.

The strategic reasons for building the NDS family of products are:

1. Software Standardization - One device class drive/handler and one set of diagnostics for the majority of new disk drives. Disk level diagnostics will reside within the disk and also be written only once.

2. Hardware Standardization - A significant saving in hardware development costs by not having to develop device/bus specific controllers.

3. Packaging - Advanced technology will produce high functionality products on fewer boards relative to today's disk controllers.

4. Subsystem Cost - Large subsystems ($\geq$ 4 drives) will be considerably more cost competitive than with Massbus architecture.

5. Performance - "Large" NDS will have closely coupled hardware/software optimization of disk subsystem activities that has the potential to significantly improve subsystem performance.

6. Error Correction - A new, powerful error correction algorithm will be implemented in a hybrid hardware/software system. This ECC will enable evolution to higher disk densities at a faster rate than without it, due to effective handling of media defects.

7. Memory Hierarchies - The disk cache concept is well understood and, as an option, will provide outstanding improvement to access time to data.

8. RAMP - Comprehensive, consistent error recovery will be done by the controller transparent to the operating system. Multiport at both drive and controller levels in "Large" NDS will support high availability configurations. Internal diagnostics running at in-line, on-line and off-line levels will efficiently isolate faults to a field replacable unit.

9. Competition - The NDS family will be required as a competitive response to known developments underway. Memorex has announced a CCD disk cache. Many of the independent subsystem suppliers already offer "intelligent" controllers.

The strategic reason for building "Small NDS" (alternatively known as UDA, Unibus Disk Adapter) is to offer a low cost alternative to NDS where its extensive set of features is not required, e.g., for small low-end and mid-range disk subsystems.

Functionality being considered for the second NDS product includes:

1. Magtape control.

2. File and data-base management.

3. Auto backup, journaling, shadow-recording.

4. Encryption and file compression.

5. Bad block handling.

6. etc.

The feasibility of inclusion of these features will be the subject of a joint advanced development study in FY'79.

The major outstanding issues for the NDS programs are:

1. Host interconnect strategy - how to efficiently and reliably connect to a number of different CPU architectures.

2. Relative schedules of NDS and "Small NDS" - Which should be introduced first? Will the earlier "lock-in" the protocols used by the latter? This is a goal so we must carefully specify the protocol of the first product.

These issues will be solved in FY'79 by Disk Product Development in conjunction with Computer Systems Development and the Base Systems POT.

G. 1/2" Magnetic Tape

The TS04 offers three times the cost/performance of the TU10 and five times that of the TS03. Consequently, it will replace the demand for these products and become our primary 1/2" Tape offering for small/medium systems. The TE16 will also be impacted but to a lesser extent, due to continuing

requirements for a 45 ips Massbus drive. The TS04 will be offered in the traditional fashion (including cabinet) as well as in a "no cab" version for the price sensitive OEM market. The TS04 is presently on hold status pending solution of design problems. The design is basically sound but significant redesign will be required prior to introduction to manufacturing. Schedule and program cost (FY'79 funding) will be reassessed by June 1978. FCS is expected last half of FY'79.

The TU77, at 125 ips, will replace demand for the TU45 and fill the gap between the TE16 and TU70 on the Massbus. This product will go a long way to relieve the current pressure caused by the poor reliability image of the TU45 and the extremely high subsystem cost of the TU70. The TU77 is from the same drive family as the TU78, but will not be field upgradable due to different vacuum systems, capstans, and read/write circuits. We are presently attempting to negotiate a contract with a supplier (Pertec) to establish a proper business relationship and firm pricing. If this is successful by early June, we expect to announce the TU77 in Q1 FY'79 and ship in Q2 FY'79.

The thrust of the TU78 program is towards providing DEC with a very competitive 6250 BPI, GCR product which will allow more successful competition at the high end. This product will replace demand for the TU70 and TU72 due to cost/performance improvements of more than 3X. The TU78 moves DEC much closer to the industry frontier established by IBM and STC and will establish DEC as the price leader at the subsystem level (including controller). Additionally, the TU78 provides a basis for migrating the GCR technology downward to provide more competitive products at the low end. Until the contract is negotiated (TU77 above), it is difficult to commit product cost and FCS. Early FY'80 FCS is most likely.

The first low-end GCR offering will be the TS6250, which is planned to use the TU78 formatter (TM78) and TS04 mechanics. We will not design a third generation low cost formatter for the TS6250 due to funding limitations. This will force the product cost goal to $5,000, where it is felt that a one-third improvement to $3,500 would be possible with a lower cost GCR formatter. Due to funding limitations and TS04 schedule slip, this program may not be started until FY'80. FCS is targeted for last half FY'81 on NDS.

V. ADVANCED DEVELOPMENT STRATEGY

In general, it is our goal to stay as close on IBM's heels as possible and ahead of all competitors other than IBM. We are probably fifth in the U.S. on mass storage development expenditures, i.e., behind IBM, CDC (i.e., MPI and CPI), Memorex, and Sperry/Univac (i.e., ISS and tape division). A goal to technologically pull ahead of CDC, Memorex and Univac therefore demands a carefully chosen strategy.

The factors which may be used to distinguish a good product from a lesser product are: cost, size (capacity), system throughput, time of introduction, portability of media, portability of drive, entry cost, data integrity, reliability, system versatility, features, tolerance to environmental stresses, etc. Our emphasis in Advanced Development is in these directions.

Our plan is to:

1. Concentrate on technologies which are quicker and less expensive to develop.

2. Avoid work in areas where we can buy near state-of-the-art components at reasonable cost.

3. Learn good outside technology rather than develop all of our own.

4. Capitalize on our strengths and volume.

5. Bypass work on technologies which are expected to be superceded.

6. Use cooperative developments where a mutual advantage exists.

7. Exploit technologies where constraints of IBM compatibility slow down competitors.

MASS STORAGE FY79 ADVANCED TECHNOLOGY DEVELOPMENTS

TECHNOLOGIES WE ARE DEVELOPING	EXPECTED ULTIMATE BENEFIT (DRIVE LEVEL)	DIFFICULTY	PER STRATEGY NO.	FY'79 EMPHASIS
Plated media	4-8X capacity/$	High	4,5,7	Strong
Improved modulation/ demodulation	2-4X capacity/$	Medium	1,3,7	Strong
Video tape	Potential backing/ archiving store	Medium	2,3,5,6,7	Modest
Microprocessor compensated servo control	Supports high track density	Modest	1,3,4,7	Modest
Disk cache	2-6X throughput and access time improvement	Medium	1,4	Completing
LSI'd electronics	10-20% cost reduction, supports other technologies	Medium to High	2,3,4,6	Medium
Improved positional accuracy mechanics	Supports density increases	Medium	3	Medium
Dynamic mechanical analysis tools	Supports density increases	Medium	3	Medium
Small diameter disk	Low entry cost, 2X throughput improvement, portable media	Medium	4,7	Strong
File backup, bad blocking, system features, tape, etc.	System cost reduction, customer features	Medium	4	Strong
Servo reference repeatability	Supports small disk density increases	Modest	4,7	Medium
Composite Head	1½X density of Winchester monolithic head	Medium	1,3,4,7	Strong
Phase Error Testing	Necessary for support of high density recording	Medium	1,4	Strong
Servo Writer Development	Support of high track densities	Medium	1,4	Strong
Thin Film Head	2X increase in density over Winchester head	High	3,6	Modest
Modular Test Equipment	Family of test equipment for future disk drives	Low	1,4	Strong
Vertical Loading Head	Makes high density test available in removeable products	Medium	1,4,7	Strong

Technologies We Are Not Internally Developing

Because of availability of components or good outside technology or technology trades or heavy investment vs. limited life, we do not intend to invest much time in the following technologies: servo control philosophies, basic circuits, spindles, conventional floppy and disk heads, particulate media, head design models (thin film), pack drive motors, blowers, packaging hardware, interconnect hardware, power supplies, SSI and MSI, 1/2" tape and compatible floppies.

Planned Breadboard Testbeds:

R81 - Med. capacity, 2 X 3350 density - evaluation complete Q3 FY'79.

AZTEC - small dia. disk, 2 X 3350 density - evaluation complete Q4 FY'79.

? - 4 X 3350 density - evaluation complete Q4 FY'80.

NDS2 - Supports disk cache - evaluation complete Q2 FY'79.

NDS3 - Bad blocking, backup, tapes, etc. - evaluation complete FY'80.

Video tape - On NDS - ?

VI. A STORAGE SYSTEMS POT FY79 PRODUCT DEVELOPMENT FUNDING WITH HISTORY ($000)

	ACTUAL FY77	PROJECTED FY78	BUDGET FY79
RX02/03	600	625	425
RX0X	-		205
TOTAL FLOPPY	600	625	630
RL01/02	1560	2376	1135
AZTEC	-	-	183
50 Mb REMOVABLE	-	480	1435
TOTAL SMALL DISK	1560	2856	2753
RK06/07	2750	1749	580
RM02/03	725	829	150
R80	100	1030	2870
R81	-	-	235
TOTAL MEDIUM DISK	3575	3608	3835
RP07 FAMILY	100	259	675
TOTAL LARGE DISK	100	259	675
TE10/TE16/TM03	600	50	
TS04	710	875	514
TS6250	-	-	260 (3)
TOTAL SMALL TAPE	1310	925	774
TU77/78	510	975	763
TAPE STANDARDS (1)	-	-	155
TOTAL LARGE TAPE	510	975	918
SMALL NDS	-	-	215
NDS	-	397	920
TOTAL INTELLIGENT SYSTEMS	-	397	1135
HANDLERS & DRIVERS			570
CCD CACHE & BUFFER	-	-	210
TOTAL NON-MASS STORAGE	950	900	780 (4)
CONTINGENCY (2)	-	-	500
TOTAL STORAGE SYSTEMS POT	8605	10545	12000

1. In project spending FY77/78
2. Allocated to projects by end of years FY77/78
3. TS6250 product development start may slip to FY80 due to TS04 program
4. VAX diagnostics in project spending for first time in FY79

VI. B MASS STORAGE GROUP - FY79 FUNDING WITH HISTORY ($000)

	ACTUAL FY77	ESTIMATED FY78	BUDGET FY79
PRODUCT DEVELOPMENT			
Storage Systems POT	7655	9645	11220
Terminals/Small Systems POT	-	455	450
Total	7655	10100	11670
ADVANCED DEVELOPMENT			
Servo & read/write		440	336
Mechanics		305	356
Mass storage systems		320	425
Heads & media	791	280	409
LSI		250	266
Flexible media		0	140
AZTEC		60	324
Total	791	1655	2256
PRODUCT SUPPORT	680	380	525
PRODUCT MANAGEMENT	167	370	475
ADMINISTRATION	N/A	N/A	150
GRAND TOTAL	9293	12505	15076

VI. C. Impact of FY79 Funding Level - Our Concerns

The Storage Systems POT and Mass Storage management have reviewed the impact of the FY79 funding plan. At the current funding level, which is significantly lower than requested, we are in serious jeopardy of losing competitive position. In particular:

1. Exposed Flanks - Areas of potential, but not highly probably, competitive pressure.

   a. Massbus Cache - Memorex has announced a CCD cache product for the IBM channel. ISS/Univac and STC are working on similar products. We have given up the ability of upgrading the large number of Massbus disk subsystems in the field by not pursuing this project. Our first hierarchical subsystem will be NDS in FY'81.

   b. Video Technology - Video tape has the capability of becoming an economical random-access storage device for very large amounts of data. The word-processing market has an immediate need for such a device. SONY has approached us and is anxious to develop a "computer-grade" video recorder. Funding limitations preclude all but a low level advanced development effort in FY'79.

   c. RX0X Floppy Disk - We are on a course which over time would put us out of the competitive floppy business. Present funding only allows us to finish the RX02; complete the Rx03, but on a less aggressive than desirable work schedule; and do minimal advanced development work through FY'79 on any subsequent high density or higher performance floppy product. We consider AZTEC advanced development of an ultra low cost hard disk to be a very risky program given no funded backup plan.

   d. Mid-Range Removable Disks - We have essentially stopped all future development of mid-range removable disk products. We are on the uncomfortable course of having no funding for product successors to the RM03 and RP06. In the long range this will create a competitive selling problem, the magnitude of which is unknown because we are unable to accurately forecast the customer shift to fixed media disks.

2. A Gap in Product Tactics - Removable NDS companion for R80.

   We have substantially reduced the RL04 development plan. This has forced us to redefine the product (the rule being "if later then necessarily better") and recognize that the RK07 will have to meet the demand for this capacity class of product through FY81.

   Between this and not funding mid-range removable disks, there will be no removable disk companion with an NDS interface for R80 when it ships on NDS. The opportunity exists for modification of a current disk (e.g., RK07), or acceleration of a new one (e.g., 50 Mb removable), to be packaged with the R80 in a subsystem which has both architectural and packaging elegance.

3. Major Exposures - Areas with highly probable future problems.

   a. Media and Head Investment - Even though it is not POT funded, we are concerned about reduction in Storage Systems Advanced Development, such that FY79 becomes a zero growth year. It is important to understand that only through significant investment in Advanced Development in past years are we to the point where we can design and build reasonably competitive products.

      We expect major technological shifts in the head and media area. We have minimal funding to seriously pursue these technologies and are dependent on financially marginal head suppliers (AMC, Infomag) and captive media suppliers (Memorex, Univac, CDC) for technological advances and manufacturing capacity. Based on conservative corporate NOR forecasts and derived needs for heads and media, it is unlikely that adequate external capacity will be available to us in the FY'82 timeframe. Considering our potential competitive posture with existing suppliers and their internal demand, a severe availability situation could develop sooner. Because of the long lead time and process intensive nature of these businesses, substantial funds need to be allocated in FY'79 for development and pilot manufacturing operations if we are to avoid catastrophe in the early 80's.

   b. I/O Interconnect - The lack of a coordinated effort and funding for a new mass storage bus is compromising NDS data integrity (if Unibus used), schedule, and standardization goals. The distributed processing nature of future mass storage transactions requires a modern, low cost, multiple master, high performance bus. The Massbus has

served well, but is technologically obsolete and must be replaced by a bus that is architecturally compatible with new CPU's and mass storage subsystems.

c. TS04 Technical Problems and FY'79 Funding - During final engineering design verification testing and initial DMT, a number of design related problems were identified. Manufacturing start-up is on engineering hold pending solution of these problems. Much additional effort is being applied to the project and it is estimated that FY'79 funding will be in excess of $1.0M rather than the $440K budgeted. To continue the program will require the diverting of additional funds. Total program cost and schedule will be reproposed in June.

4. Areas Where Acceleration is Desired and Feasible

a. Small NDS (UDA) - The allocated level of funding explicitly slows development by three to six months. FCS of Small NDS to coincide with the R80 will be impossible.

b. Mid-Range Removable Buyout - See 1d. Funding should be allocated to begin development of a buyout product in FY'79.

c. 50 Mb Removable - See 2.

d. We are less aggressive on low-end ½" tapes than is desired which will cause us to have higher manufacturing costs than we should. In particular, the TS6250 is estimated at $5,000 instead of $3,500.

e. We are unable to sufficiently fund longer term advanced products such as Small NDS, AZTEC, and R81. This will slip the schedule of these products. They are critical to the success of the Mass Storage business in future years.

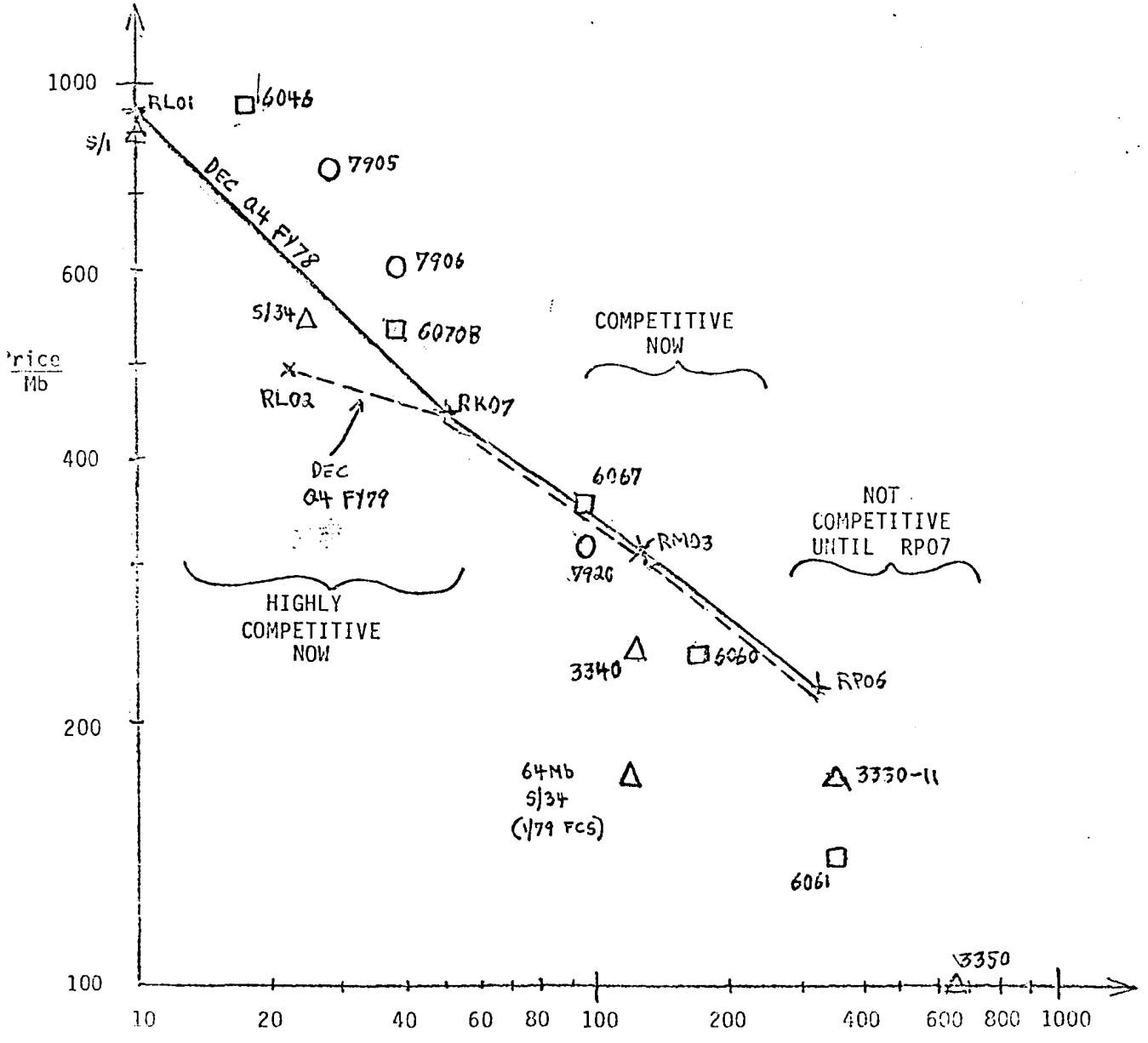
f. We will be unable to start product development on the very desirable intelligent controller subsystem that will integrate both tape and disk technology into a single mass storage subsystem.

In further support of Storage Systems, it is important to note that we have significantly underfunded development proportional to revenue production. Storage Systems accounts for about 1/3 of corporate revenue. In addition, an ever increasing share of system sales is dependent on Storage System price performance instead of central processor price performance. We seriously believe that more than 1/9 of our corporate engineering investment is necessary to maintain this 1/3 of revenue stream.

VI D. THE MASS STORAGE BUSINESS - COMPARISONS TO OVERALL DEC GROWTH

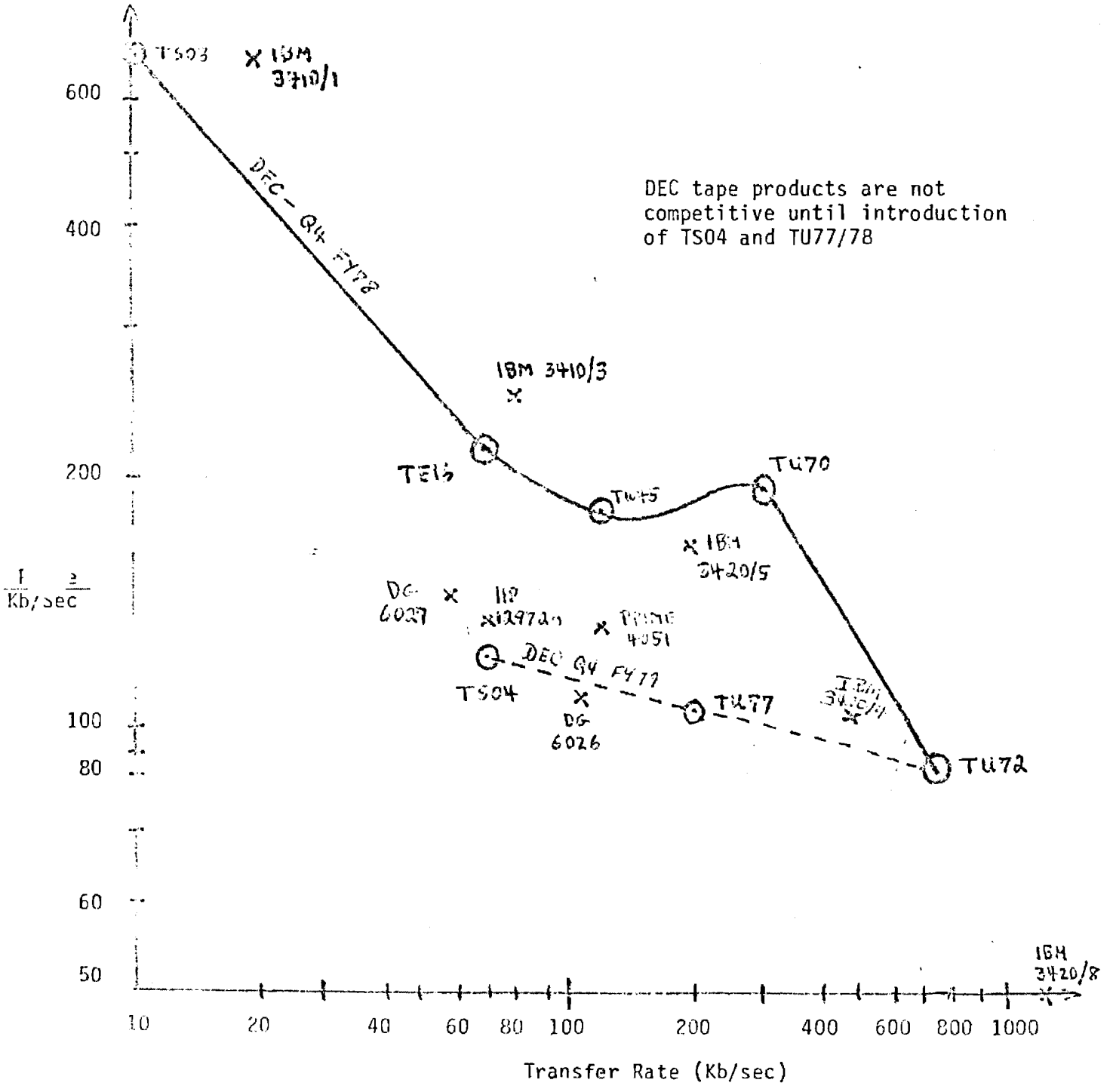
	FISCAL YEAR						
CORPORATE PLAN	76	77	78	79	80	81	82
CORPORATE NOR	736	1059	1420	1748	2096	2520	3033
LESS SERVICE & OTHER REVENUE	(149)	(212)	(298)	(367)	(440)	(529)	(637)
CORPORATE NES	587	847	1122	1381	1656	1991	2396
LESS SOFTWARE NES	(23)	(42)	(67)	(97)	(132)	(179)	(240)
HARDWARE NES	564	805	1055	1284	1524	1812	2156
TRANSFER COST OF HARDWARE NES	215	293	378	451	541	650	783
+ 15% FA&T BURDEN	32	44	57	68	81	98	117
HARDWARE CGS	247	337	435	519	622	748	900
% OF HARDWARE NES	44%	42%	41%	40%	41%	41%	42%
CENTRAL ENGINEERING DEVELOPMENT SPENDING	34	46	67	85	106	132	
LESS SOFTWARE DEVELOPMENT SPENDING	(8)	(10)	(15)	(23)	(28)	(37)	
HARDWARE DEVELOPMENT SPENDING	26	36	52	62	78	95	
MASS STORAGE PLAN							
TAPE TRANSFER COST	12	18	28	35	37	47	52
FLOPPY + DISK TRANSFER COST	39	63	89	124	157	197	247
TOTAL MASS STORAGE COST	51	81	117	159	194	244	299
+ 15% FA&T BURDEN	8	12	18	24	29	37	45
TOTAL MASS STORAGE CGS	59	93	135	183	223	281	344
MASS STORAGE NES (2.5 X NET MARKUP)	148	233	337	458	557	702	860
AS % OF HARDWARE NES	26%	29%	32%	36%	37%	39%	40%
MASS STORAGE DEV. SPENDING - POT & NON-POT	6.5	9.3	12.5	15.1	19.3	24.8	
AS % OF MASS STORAGE NES	.044%	.040%	.037%	.033%	.035%	.035%	
AS % OF HARDWARE DEV. SPENDING	25%	26%	24%	24%	25%	26%	

VII. A PRICE COMPETITIVENESS OF DEC DISK OFFERINGS - FY78 AND FY79



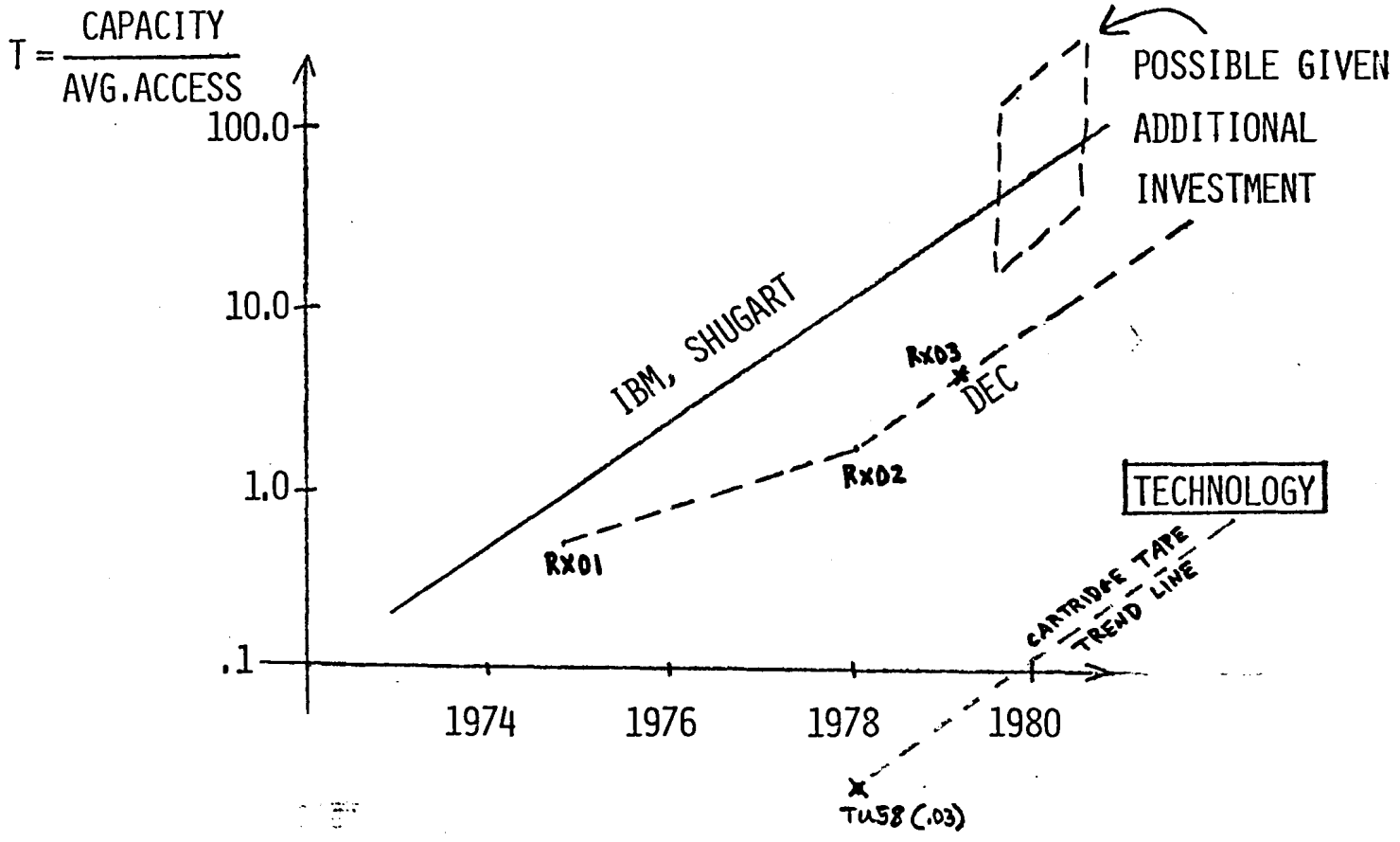
Notes: 1. Price is the price of a dual drive subsystem
2. All competition products are currently available. For purposes of FY79 comparison it is reasonable to assume competitive advances will be made.

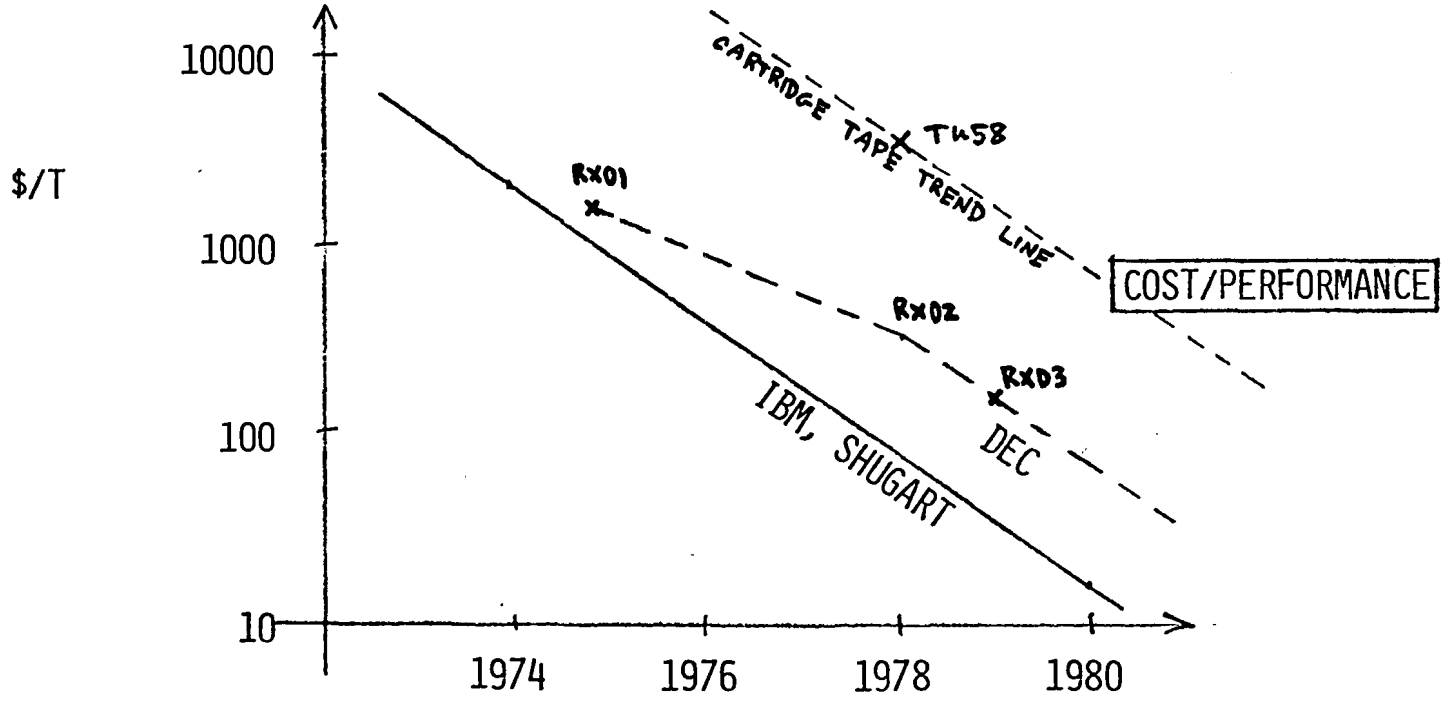
VII. B PRICE COMPETITIVENESS OF DEC 1/2" TAPE OFFERINGS - FY78 AND FY79



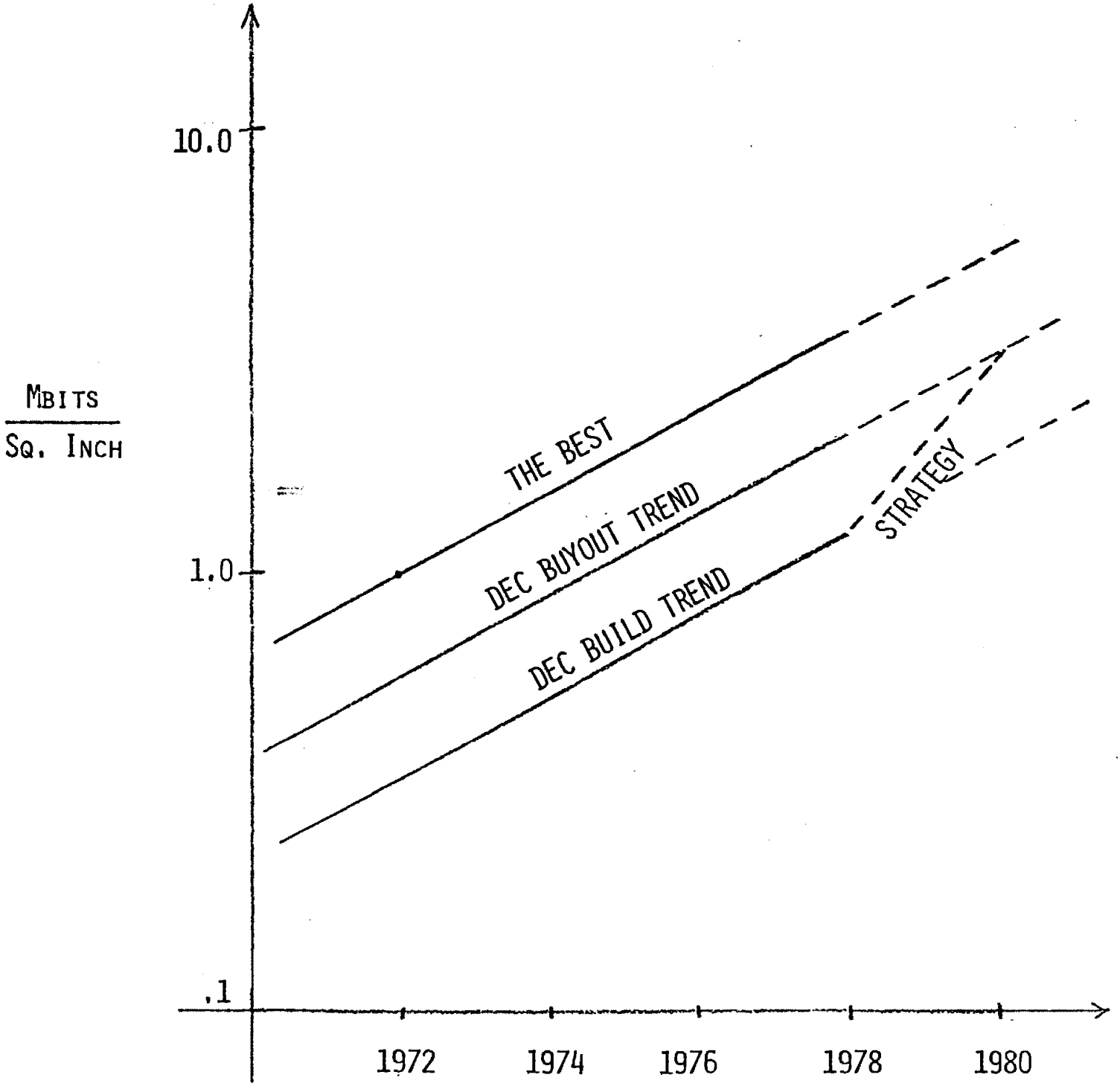
Notes:
1. Price is a weighted average of master and slave drives which assumes 1.4 drives/subsystem.
2. All competition products are currently available. For purposes of FY79 comparison it is reasonable to assume competitive advances will be made.

VII. C FLOPPY DISK TECHNOLOGY AND COST/PERFORMANCE TRENDS

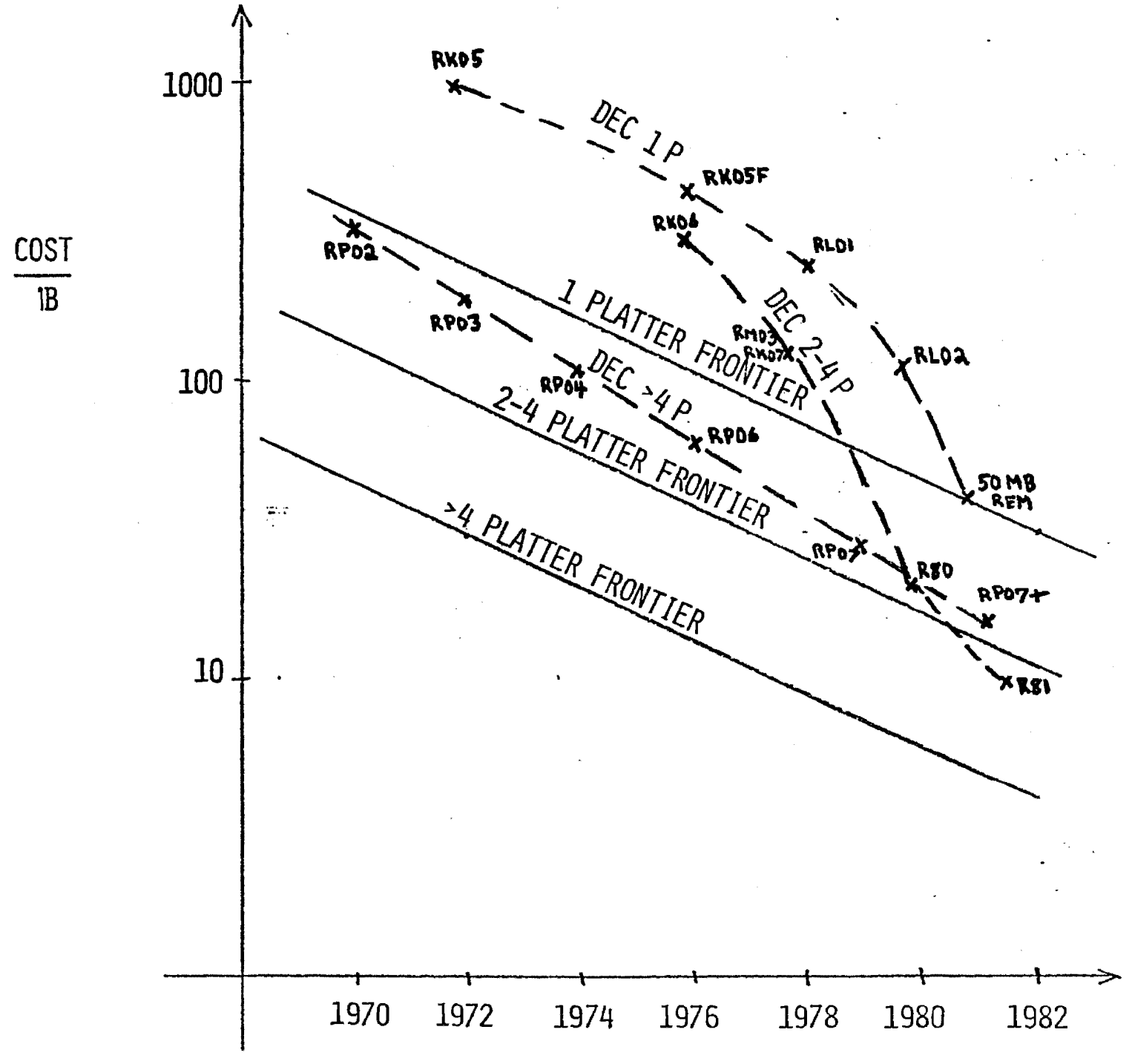




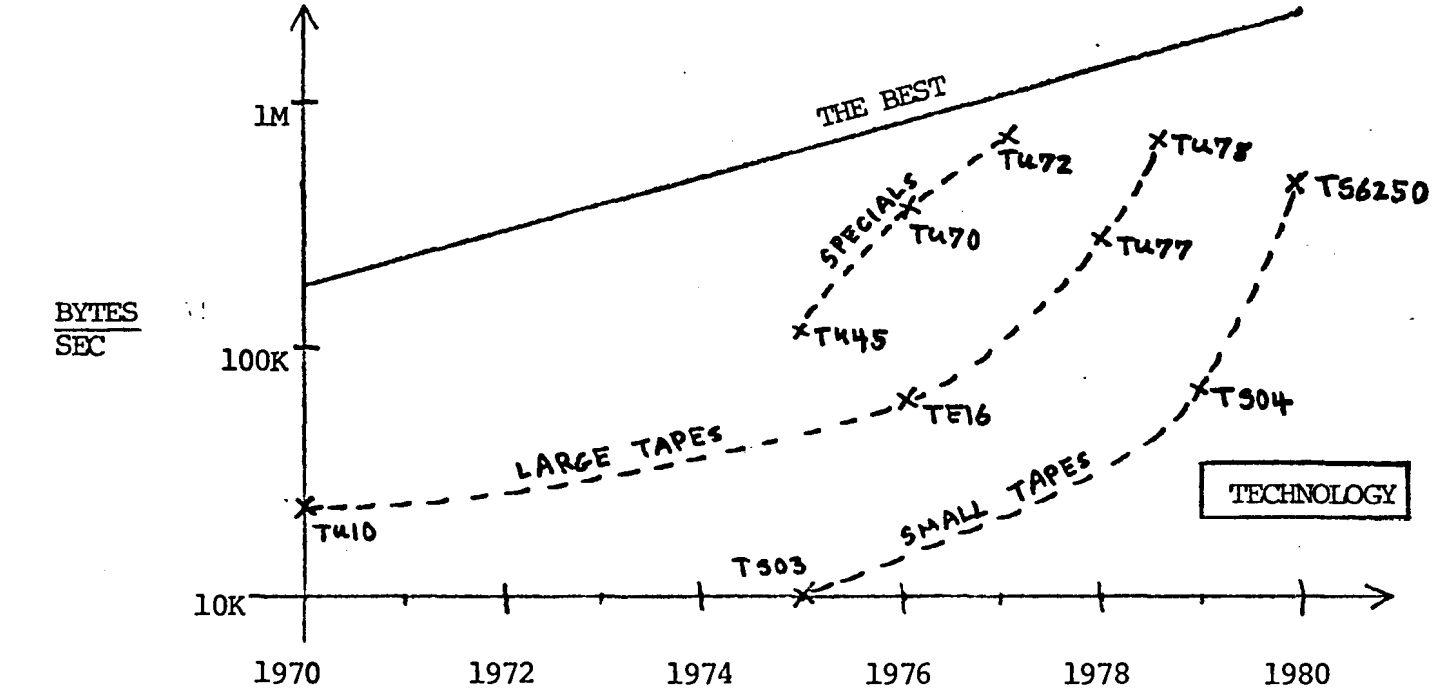
HARD DISK TECHNOLOGY TRENDS

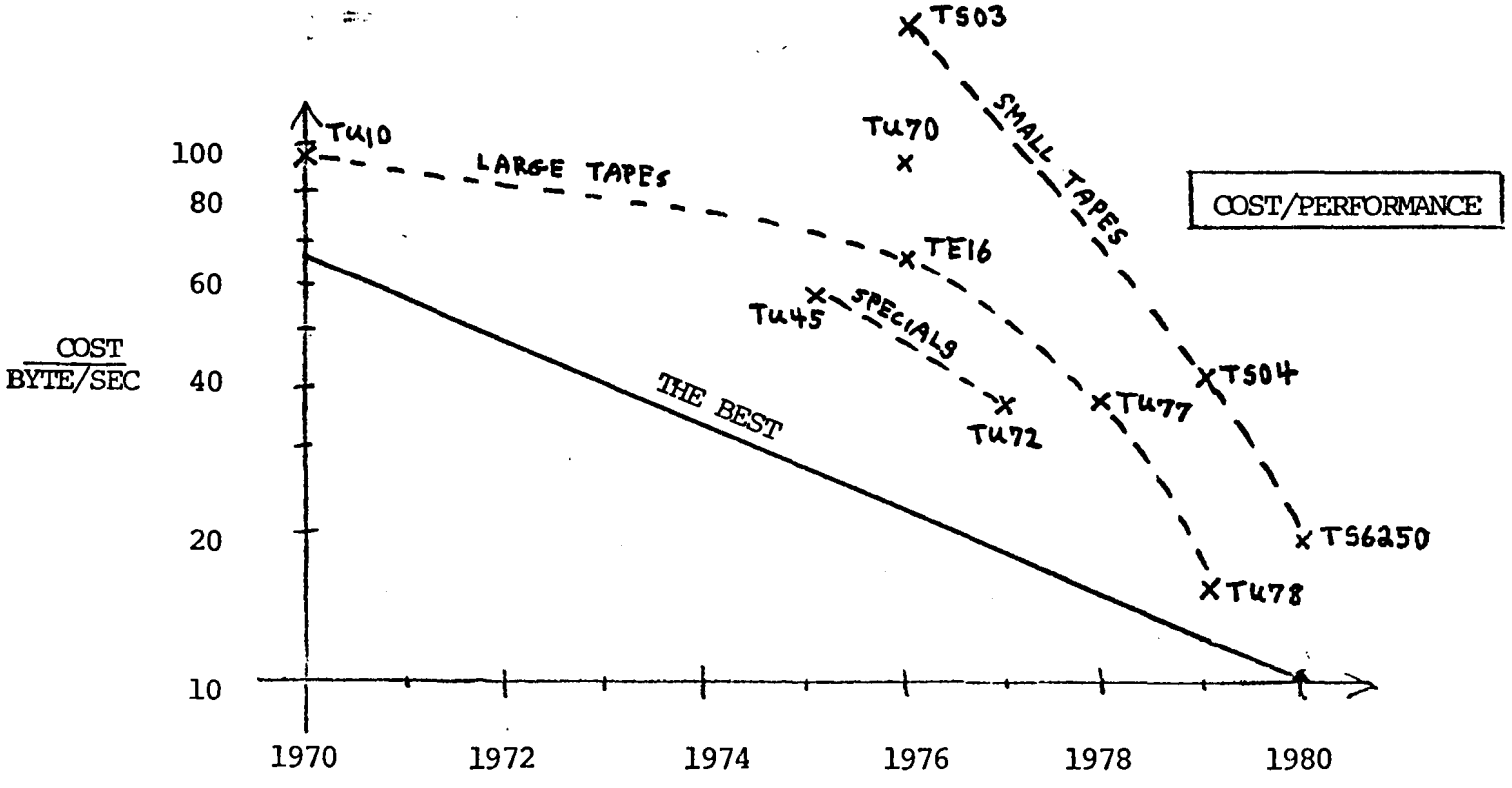


DISK COST/MB TRENDS



MAG TAPE TECHNOLOGY AND COST/PERFORMANCE TRENDS





NOTE: ALL COSTS ARE WEIGHTED AVERAGE OF MASTER AND SLAVE BASED ON 1.4 DRIVES PER SUBSYSTEM

BASE SYSTEMS POT
PRODUCT CALENDAR as of 5/30/78

PRODUCT FAMILY	PRODUCT NAME	DESCRIPTION	FCS DATE	EST. FY78 COST	EST. FY79 COST	EST. TOTAL COST	PRODUCT MANAGER	ENGINEERING ORGANIZAT'N
	BASE Contingency		n/a		500			Unallocated
	Memories	Includes MS11KC, MS11L, MSM11M, MK11, MKA11, MS780D	n/a	900	400			Cudmore
	Packaged Standard Systems		n/a	200	400		B. Flynn	Clayton
11	K2 Kernel	OS kernal for PDP-11s, except low end	n/a	500	1050			Portner
11	Unifonz	Fonz-based 11/04 CPU (board) replacement with integral warm-FPP and CIS	Q1/FY80(T)		500		J. Hamilton	Demmer
11/34	11/44	Central Processor, 11/34 functionality and performance plus CIS, PAX	Q4/FY79	800	1200		B. Fifield	Demmer
11/34	MS11L	16K MOS upgrade for 11/04-34	Q1/FY79		(Mem.)		M. Gutman	Cudmore
11/34	MS11M	16K ECC MOS for 11/44			(Mem.)		M. Gutman	Cudmore
11/48	11/48	Higher-performance 11/34 & 44 replacement at 11/34 cost	FY82(T)		200			Demmer
11/68	11/68	Lower-cost 11/74 CPU replacement	Q4/FY80(T)	300	850		T. Sherman	Demmer
11/70	11/74	Corp. cabinet 11/70 with CIS option and multiprocessing extensibility	Q3/FY79	700	900		M. Powell	Demmer
11/70	11/74 mp	CERBERUS 11/74 multiprocessor under RSX-11M+	Q3/FY79		550		M. Powell	Clayton
11/70	MK11	Singleport MOS memory for 11/70	03/78		(Mem.)		M. Gutman	Cudmore

PRODUCT FAMILY	PRODUCT NAME	DESCRIPTION	FCS DATE	EST. FY78 COST	EST. FY79 COST	EST. TOTAL COST	PRODUCT MANAGER	ENGINEERING ORGANIZAT'N
11/70	MKA11	Singleport MOS memory for 11/74	Q3/FY79		(Mem.)		M. Gutman	Cudmore
11/70	MS11KC (was MS11K Prime)	16K MOS memory upgrade for 11/70, 11/74	Q4/FY79(T)		(Mem.)		M. Gutman	Cudmore
VAX	11/780	32-bit system with twice 11/70 performance, equal performance in 16-bit compatibility mode.	12/77(S)	2400	600		B. LaCroute	Demmer
VAX	11/780 mp	Sys Eng			50			Clayton
VAX	11/780 mp	Hardware		300	600			Demmer
VAX	11/780 mp	Software			200			Portner
VAX	11/780 mp	Architecture			100			Demmer
VAX	Comet	Mid range VAX system: one third 11/780 cost, two thirds performance; warm-FPP and CIS	Q1/FY80	2300	3200	6900	D. Best	Demmer
VAX	LSI/VAX		FY82					
VAX	MS780D	16K MOS memory upgrade	Q1/FY79		(Mem.)		M. Gutman	Cudmore
VAX	Nebula	11/780 functionality, 5% of 11/780 performance at 10% of the price, LSI system	FY81(T)					Demmer
VAX	Superstar	Higher performance and functionality than 11/780, lower price	FY82					
VAX	VMS Kernal	OS kernal for VAX-11s	n/a	2000	1700			Portner

COMMERCIAL SYSTEMS POT
PRODUCT CALENDAR as of 5/30/78

PRODUCT FAMILY	PRODUCT NAME	DESCRIPTION	FCS DATE	EST. FY78 COST	EST. FY79 COST	EST. TOTAL COST	PRODUCT MANAGER	ENGINEERING ORGANIZAT'N
	Contingency				605			Portner
11	ADE-1	Application development facility oriented to first-time end user marketplace, as well as improving programmer productivity by OEMs, distributors (bundled with SCS-11)	Q1/FY80	46	245	291	T. Webber	Portner
11	BASIC Plus 2	DEC standard BASIC compiler	09/77	107	0	107	R. Pitetravalle	Portner
11	COBOL	ANSI compliant COBOL V4A/V4B; performance releases with packed decimal data type (V4B FCS Q3/FY79)	Q2/FY79 (V4A)	143	184	327	R. Pietravalle	Portner
11	Datatrieve 11	Inquiry language/report writer for RMS-11K	01/78	175	46	221	R. Pietravalle	Portner
11	Fast Back-up	RP07 fast backup utility for RSTS/E V7A	n/a		60	60	R. Pietravalle	Portner
11	RMS-11	Cross-system compatible sequential, relative, multi-key ISAM file management	Q2/FY79 (V1.5)	248	337	585	R. Pietravalle	Portner
11	RSTS V7a	Support of large files (greater than 65K blocks), shared libraries (RMS), disk caching, new device support, continued availability of small (64K) RSTS/E configuration with V6C functionality	12/78	369	307	676	T. Webber	Portner
11	RSTS V7B	Improved spooler, backup, and batch features, and improvements in the RSTS task builder, and new device support	n/a		199	199	T. Webber	Portner

PRODUCT FAMILY	PRODUCT NAME	DESCRIPTION	FCS DATE	EST. FY78 COST	EST. FY79 COST	EST. TOTAL COST	PRODUCT MANAGER	ENGINEERING ORGANIZAT'N
11	SCS-11	Small business systems software consisting of packaged RSX-11M based OS and small file manager (upward compatible with RMS)	Q1/FY80	365	736	1101	T. Webber	Portner
11	Small COBOL	ANSI standard COBOL for SCS-11	Q1/FY80	217	276	493	R. Pietravalle	Portner
11	TRAX	Dedicated transaction processing system	07/78 (V1)	819	858	1677	C. Johnson	Portner
VAX	BASIC Plus 2 Compiler	For native mode VAX execution, compatible with PDP-11 BASIC Plus 2	Q1/FY80	191	307	498	R. Pietravalle	Portner
VAX	COBOL-11/VAX	Native mode execution of COBOL-11	Q2/FY79	180	92	372	R. Pietravalle	Portner
VAX	COBOL-79	Native mode high performance for VAX	FY81	224	598	821	R. Pietravalle	Portner
VAX	Commercial VAX	Transaction processing monitor for VMS -- TRAX interface (TRAX-32)	FY81	55	305	360	C. Johnson	Portner
VAX	DBMS-32	CODASYL compliant data base management for VAX	FY81		184	184	R. Pietravalle	Portner
VAX	EDITOR/VAX	DEC standard editor for VAX			30	30	R. Pietravalle	Portner
VAX	OTS	Commercial run-time support for VAX subsystems		242	184	426	R. Pietravalle	Portner
VAX	RMS-32	RMS-11 compatible file management for VAX	Q3/FY79 (ISAM)	356	368	724	R. Pietravalle	Portner
VAX	SORT-32	High performance file sort/merge for VAX		97	77	174	R. Pietravalle	Portner

NETWORK/COMMUNICATION POT
PRODUCT CALENDAR as of 5/30/78

PRODUCT FAMILY	PRODUCT NAME	DESCRIPTION	FCS DATE	EST. FY78 COST	EST. FY79 COST	EST. TOTAL COST	PRODUCT MANAGER	ENGINEERING ORGANIZAT'N
Comm HW	DML11	Four-line synchronous multiplexer	FY79		230			Marcus
Comm HW	DMP11	UNIBUS full DDCMP synchronous interface with local line driver	FY79	256	220	500	A. Brind	Marcus
Comm HW	DMV11	QBUS full DDCMP synchronous interface with local line driver	08/79		200	250	A. Brind	Marcus
Comm HW	DMV Microcode	Redesign to make DMV more compact	FY80		50			Marcus
Comm HW	DZ11-H	Additional Modem Control for DZ11	FY79	39	60	187	A. Brind	Marcus
Comm HW	KMC11-B	Enhanced KMC-11 intelligent interface	FY80		40		A. Brind	Marcus
Nets	DECnet	Advanced network functionality for RSX-11M, S, M+, TRAX, SCS, TOPS-20, VMS, IAS, RSTS, RT-11 (see also Red Book)			2700		D. Loveland	Portner

REAL TIME/COMPUTATION POT
PRODUCT CALENDAR as of 5/30/78

PRODUCT FAMILY	PRODUCT NAME	DESCRIPTION	FCS DATE	EST. FY78 COST	EST. FY79 COST	EST. TOTAL COST	PRODUCT MANAGER	ENGINEERING ORGANIZAT'N
	FORTRAN IV+	RMS, VAX, ANS standards, maintenance, enhancement	2H/FY79 (V2)		341		R. Brown	Portner
11	Files and Utilities	Maintenance, enhancement			306		K. Friedrich	Portner
11	IAS	High end general purpose TS, RT, and Batch system, incorporating RSX-11D, PLAS, New Device Support	12/78 (V3)	319	238	500	A. McCray	Portner
11	RSX-11M	High performance sensor based real time. Features to include new device support, ease of use and improved real time performance.	2H/79 (V3.2)		107		K. Friedrich	Portner
11	RSX multiprocessing	Multiprocessor software for 11/70 mp	2H/79		122		K. Friedrich	Portner
11	RT-11	Continued development as kernal, and new device support.	2H/79		408		D. Strauss	Portner
VAX	32-bit Real Time	DR-780 software, FORTRAN IV+ enhancements, KMC-11 tools, OS mods, RT Users Guide, WCS tools, contingency	Q1/FY80(T)		600		Best/McCray	Portner

STORAGE SYSTEMS POT
PRODUCT CALENDAR as of 5/30/78

PRODUCT FAMILY	PRODUCT NAME	DESCRIPTION	FCS DATE	EST. FY78 COST	EST. FY79 COST	EST. TOTAL COST	PRODUCT MANAGER	ENGINEERING ORGANIZAT'N
	Contingency		n/a		500	n/a		Kevill
	Handlers and Drivers		n/a		570			Portner
	Tape Standards		n/a		155	n/a		Kevill
Floppy	RX02/03	.5 MB/1.0 MB Floppy (RX03 FCS Q4/FY79)	Q1/FY79 (RX02)	625	425	2000	L. Powell	Kevill
Floppy	RX0X	Track floppy technology	n/a		205		L. Powell	Kevill
Lg Dsk	RP07/07+/08	292 MB/542 MB fixed disk family (RP07+, 08 FCS FY80)	Q3/FY79 (RP07)	259	675	1600	P. Feresten	Kevill
Lg Tape	TU77/78	125 IPS 1600/6250 BPI tape family (TU78 FCS Q4/FY79)	Q2/FY79 (TU77)	975	763	2500	P. Feresten	Kevill
Md Dsk	R80	143 MB fixed media drive, Massbus and NDS	FY80	1030	2870	7000	K. Sills	Kevill
Md Dsk	R81	286MB drive, NDS	FY81		235	2500	K. Sills	Kevill
Md Dsk	RK07	28MB cartridge disk	03/78	400	580	1000	K. Srivastava	Kevill
Md Dsk	RM02/03	67MB Disk drive, Unibus (RM02), Massbus (RM03) (RM03 FCS 10/77)	04/78 (RM02)	829	150	2000	K. Smith	Kevill
Sm Dsk	AZTEC	5-8 MB drive	FY81		183			Kevill
Sm Dsk	RL01/02	5 MB/10 MB Cartridge drive and controller (RL02 FCS Q4/FY79)	12/77 (RL01)	2376	1135	6000	W. Galusha	Kevill

PRODUCT FAMILY	PRODUCT NAME	DESCRIPTION	FCS DATE	EST. FY78 COST	EST. FY79 COST	EST. TOTAL COST	PRODUCT MANAGER	ENGINEERING ORGANIZAT'N
Sm Dsk	50 MB Removable	50 MB cartridge drive (low cost RK07 replacement)	FY81	480	1435	4000	W. Galusha	Kevill
Sm Tape	TS04	45 IPS 800 or 1600 BPI, Unibus	09/78	875	514	2000	E. Siegmann	Kevill
Sm Tape	TS6250	22-45 IPS 1600/6250 BPI	FY81		260		E. Siegmann	Kevill
Systems	NDS	Intelligent Subsystem	FY81	400	920	3000	K. Sills	Kevill
Systems	CCD Cache and Buffer	CCD array and controller, and RAM buffer, for NDS	n/a		210	300	M. Gutman	Cudmore
Systems	Small NDS	One board Unibus control, NDS protocols	FY81		215	500	K. Sills	Kevill

PRODUCT FAMILY	PRODUCT NAME	DESCRIPTION	FCS DATE	EST. FY78 COST	EST. FY79 COST	EST. TOTAL COST	PRODUCT MANAGER	ENGINEERING ORGANIZAT'N
	Contingency				345			Unallocated
	Misc. Small Systems				300			Clayton
	Systems Products	11T03L, 11V03L, Mfg. Intro., PEL, etc.	n/a		670		H. Allard	Clayton
11/23	11/23	Boxed Fonz double, replaces 11/03 (higher performance and same cost); 11V23 with RX02, 11T23 with RL01					G. Dulaney	Clayton
Fonz	Chip Enhancements	MIC, CIS chips			625		G. Dulaney	Clayton
Fonz	Chips	Completion of DAT, CTL, MMU			920		G. Dulaney	Clayton
Fonz	Double & Boot	Double height CPU and bootstrap module, component of 11/23			200		G. Dulaney	Clayton
Fonz	Fonz11	Higher performance LSI 11/Qbus Successor, board level	12/78	1753		4000	G. Dulaney	Clayton
Fonz	Memory	64K MOS, CCD/BBL			150		M. Gutman	Cudmore
Fonz	Quad	Quad with space for CIS, ROM diagnostic, WCS, FP11, KW11, Boot, SLU			0		G. Dulaney	Clayton
Fonz	WCS	F-11 WCS breadboard			0		G. Dulaney	Clayton
Hd Copy	LA00	Low cost, table top, 300 baud hard copy terminal	11/78	1420	1400	3260	D. Cotton	Clayton

PRODUCT FAMILY	PRODUCT NAME	DESCRIPTION	FCS DATE	EST. FY78 COST	EST. FY79 COST	EST. TOTAL COST	PRODUCT MANAGER	ENGINEERING ORGANIZAT'N
Hd Copy	LA120	1200 baud, fully optioned hard copy terminal	09/78	1400	800	2400	P. Maas	Clayton
Hd Copy	LA120 opt	Includes 11 wire head, video option, 212 integration, protocol board integration, option packaging and BSR	9/78		100		P. Maas	Clayton
Hd Copy	LA1200	1200 baud, 120 cps LA00			315		P. Maas	Clayton
Hd Copy	Line Printer	Line printer evaluation	n/a		170			Clayton
IT	IT100 B&C SW	Intelligent terminal software	03/79	400	600	900		Portner
IT	IT100 A&B HW				220		M. Wurster	Clayton
IT	IT100 C HW	Includes development of Toby board (see RLT-11)			170		M. Wurster	Clayton
IT	RLT-11	Disk based intelligent terminal (product space same as IT100D).			0		E. Glazer	Clayton
IT	TU58 (was TAXX)	256 byte cartridge	11/78		450		L. Powell	Kevill
Tiny	Shoebox	T-11 bounded system			220		D. Dezzani	Clayton
Tiny	Tiny11	Lower cost LSI 11 successor for terminal applications	On hold	700	750	1500	D. Dezzani	Clayton
Video	VT100	Display terminal successor to VT5X	09/78		515		E. Glazer	Clayton

GLOSSARY (The intention is to describe usage rather than to define. First Customer Ship is shown for products in development.)

11 family, 16-bit PDP-11 processors, including:

11/03, low-end QBUS CPU

11/03L, large cabinet 11/03

11V03, packaged 11/03 system

11/23, improved performance 11/03 replacement, same price, using Fonz double board, FCS ?

11V23, packaged 11/23 system (RX02 floppy), FCS ?

11T23, packaged 11/23 system (RL01 disk), FCS ?

11/34, midrange CPU

11/44, 11/34 with commercial instruction set and physical address extension, FCS Q4/FY79

11/48, higher-performance 11/34 and 11/44 replacement at 11/34 cost, FCS FY82

11/60, midrange CPU

11/68, lower-cost 11/74 replacement, FCS Q4/FY80

11/70, current high-end 16-bit PDP-11 processor

11/74, 11/70 with commecessor, twice 11/70 performance in native mode, equal to 11/70 in compatibility mode

11/780MP, multiprocessing 11/780

150 MB removable, NDS disk product, FCS FY80

50 MB removable, NDS disk product, FCS FY81

6250 GCR, industry interchange standard tape products, 6250 BPI, group code recording technology

ADDS, Applied Digital Data Systems, Inc., terminal manufacturer

APL, high-level programming language

ATT, American Telephone & Telegraph

AZTEC, 4-8 MB removable rigid low-end disc, FCS FY81

Baud, data transfer rate in bits per second

BISYNC, IBM's synchronous communication protocol

BLISS, system software development tool

Bounded System, system designed with pre-defined limits to configuration extensibility

BPI, bits per inch, density of tape storage

Bubble, magnetic domain (bubble) memory technology

CCD, charge coupled device memory technology

CDC, Control Data Corporation, CPU, disk, etc., manufacturer

CEREBUS, code name for the 11/74 MP project, FCS Q3/FY79

CIS, commercial instruction set for improved COBOL performance

COMET, medium VAX CPU, next down from 11/780, FCS Q1/FY80

CPU, central processing unit

CTS-300, commercial operating system for DIBOL program development and execution

DBMS, data base management system

DC11, dual asynchronous line interface

DDCMP, Digital Data Communications Message Protocol

DG, Data General

DH11, 16 line programmable asynchronous multiplexer

DIBOL, Digital Business Oriented programming Language

DJ11, 16 channel asynchronous multiplexer

DL11, asynchronous line interface

DLV11, QBUS asynchronous line interface

DML11, four-line synchronous multiplexer, FCS FY79

DMP11, UNIBUS full DDCMP synchronous interface with local line driver, FCS FY79

DMV11, QBUS full DDCMP synchronous interface with local line driver, FCS FY80

DMA, direct memory access

DNA, Digital Network Architecture

Dock-merge, bring products or components together for shipment as a system without full Final Assembly and Test Procedure

DOD, language to be specified for all Department of Defense contracts

DQ11, synchronous (BISYNC) DMA interface

Drop-ship, ship products or components directly from manufacturing or warehouse location without Final Assembly and Test Procedure

DS-310, commercial packaged system

Dumb Terminal, terminal that includes no integral processing capability

DU11, synchronous interface

DUP11, non-DMA synchronous line interface for DDCMP, SDLC, HDLC, BISYNC

DUV11, QBUS synchronous line interface

DV11, synchronous/asynchronous 16 line multiplexer

DZ11, 8-line asynchronous interface with modem control

DZV11, QBUS 4-line asynchronous interface

D/IAS, See IAS

EBAM, Electronic Beam Addressable Memory technology (e.g., BEAMOS)

F4+, FORTRAN IV Plus programming language

FCS, first customer ship date

FHO, fixed head option for disks

Floppy, flexible disk medium, diskette

Fonz (F-11), higher performance LSI-11 QBUS replacement, FCS 12/78

FPP, floating-point arithmetic instruction processor

GCR, group code recording tape technology

GSD, IBM's General Systems Division, marketer of Series 1 and System/3

Hard copy, terminal producing printed output

HDLC, Higher Data Link Control communication protocol

HMOS, higher-level NMOS technology

HP, Hewlett-Packard

IAS, large multi-user time-sharing operating system with real time capability, incorporating RSX-11D

Interface, intermediary between a device controller and the processor bus

IPS, inches per second, tape travel speed

Iron, hardware sold without supporting software

IT, intelligent terminal, a terminal with programmable processing capability
IT100, family of intelligent terminals

K2, operating system kernel for RSX-11M+

Kernel, operating system base including application-independent system resource allocation capability, to be used as nucleus of an operating system family (e.g., K2 Kernel, VMS Kernel)

KMC11, intelligent interface

LA00, low cost table-top 300 baud hard copy terminal, FCS 11/78

LA36, hard copy terminal

LA120, 1200 baud, fully optioned hard copy terminal, FCS 9/78

LA180, hard copy printer

LA1200, 1200 baud LA00, FCS ?

LDP, Laboratory Data Processing

LSI, large scale integration semiconductor circuits

LSI-11, current PDP-11 LSI chip set

LSI/VAX, low-end VAX CPU, next down from NEBULA, FCS FY82

MASSBUS, high performance controller-device interconnect

MB, Mb, megabyte

MBM, magnetic bubble memory technology

MDP, Medical Data Processing

MLP, Maynard List Price

MOS, metal oxide semiconductor technology

MP, mP, multiprocessor

MUX, data multiplexor

M+, operating system, enhanced functionality of RSX-11M, short for RSX-11M+

NDS, intelligent subsystem to control disk and tape drives, FCS FY81

NEBULA, small VAX CPU, next down from COMET, FCS FY81

NMOS, N-channel or nitride MOS technology

OEM, original equipment manufacturer, incorporates DEC products into his own products for sale including significant added value

OS, operating system

Packaged System, preconfigured base system sold as a single product

PAX, physical address extension to overcome maximum memory addressable in a 16-bit machine

PL/1, high-level programming language

PMI, processor-memory interconnect, generic

Protocol, the predefined exchanges between system elements necessary for communication of data

QBUS, lower cost standard bus for low-end PDP-11 CPUs

PULSAR, code name for LSI-11 multiprocessor project

Rack & Stack, general purpose components for OEM and end-user product lines

R80, 143 MB fixed disk drive, FCS FY80

R81, 286 MB fixed NDS disk drive, FCS FY81

RAM, random access memory

RAMP, reliability, availability, maintainability program

RDS, remote diagnosis service

RK05J/F, 2.4 MB removable/5 MB fixed low-end disk drives

RK06/RK07, 14 MB/28 MB removable mid-range disk drives

RL01, 5.2 MB removable low-end disk drive

RL02, 10 MB removable low-end disk drive, FCS Q4/FY79

RM02/RM03, 67 MB removable mid-range disk drives

RMS, ISAM file management system

RP04/RP05, 88 MB removable high-end disk drives

RP06, 176 MB removable high-end disk drive

RP07, 292 MB fixed high-end disk drive, FCS Q3/FY79

RP07+, 542 MB fixed high-end disk drive, FCS FY80

RP08, 542 MB fixed high-end NDS disk drive, FCS FY80

RS03/RS04, .5MB/1.0MB fixed head disk drives

RSTS, RTST/E, high performance time sharing operating system

RSX, RSX-11D, M, M+, or S operating system

RSX-11D, see IAS above

RSX-11M, real time multiprogramming operating system

RSX-11M+, RSX-11M functionality with multiprocessing capability

RSX-11MP, see RSX-11M+

RSX-11S, small execute-only operating system, requires host RSX-11M system

RT, RT-11, low-end real-time operating system

RT/C, Real Time/Computation Systems POT

RX01, .25 MB floppy disk

RX02, .5 MB floppy disk, FCS 8/78

RX03, 1.0 MB floppy disk, FCS Q4/FY79

RX0X, 204 MB floppy disk, FCS ?

RXT-11, bounded system developed with product line funds, same product space as IT100D

SBI, Synchronous Backplane Interconnect for VAX-11/780

SCS, Small Commercial System, FCS Q1/FY80

SDLC, IBM's Synchronous Data Line Control communication protocol

SNA, IBM's System Network Architecture

Smart terminals, non-programmable terminals with some processing capability

Soft copy, terminals that display text without printing it

SS/T, Small Systems and Terminals POT, (also T/SS)

STC, Storage Technology Corporation

SUPERSTAR, large VAX successor to 11/780, lower cost and improved performance, FCS FY82

TDM, time-division data multiplexor

TE16, 800/1600 BPI, 45 IPS tape drive

TI, T/I, Texas Instruments

Tiny, T-11, lower cost LSI-11 successor for terminal applications, FCS ?

TOPS-20, DECsystem 20 operating system

TPS, transaction processing system, now called TRAX

TRAX, transaction processing system

T/SS, Terminals and Small Systems POT (also SS/T)

TS03, 800 BPI, 12.5 IPS tape drive

TS04, 800/1600 BPI, 45 IPS tape drive, FCS FY79

TS6250, 1600/6250 BPI, 22-45 IPS NDS tape drive, FY81

TTL, transistor-transistor logic technology

TU10, 200/556/800 BPI, 45 IPS tape drive

TU45, 800/1600 BPI, 75 IPS tape drive

TU58, 256 byte cartridge, FCS 11/78

digital

INTEROFFICE MEMORANDUM

TO: Distribution

DATE: 24 AUGUST 1979
FROM: Paul Bauer
DEPT: Eng. Opers.
EXT: 3-6581
LOC/MAIL STOP: ML3-3/B91

SUBJECT: 1979 ENGINEERING STRATEGY STATEMENT (Red Book)

This is your copy of the 1979 Engineering Strategy Statement, which describes the product development plans for Central Engineering.

This plan has been developed by five systems/product development groups which were formed to begin implementation of the Basic Product Strategy. This Strategy, previously circulated and approved by the Board of Directors, calls for our timely transition to a series of computers employing a single 32 bit architecture, with the necessary terminals, storage, software, and network products to successfully compete in the market of the 1980's.

This document outlines our initial implementation plans. A copy of the Basic Product Strategy is also included.

During FY80, our strategy efforts will be devoted to providing more of a systems focus for easier coupling to the generic market group strategies. The challenge to engineering will be to provide this systemness while still responding to the ongoing technological changes.

If you have further questions, or require further information, you can contact these people responsible for the various elements of the plan:

Red Book	Paul Bauer Dave Quimby
CSD	Dick Clayton Stan Pearson
MSD	Bill Demmer Bernie Lacronte
LSG	Ulf Fagerquist Per Hjerppe
Software	Bill Johnson Jack Mileski
Storage	Grant Saviers Mike Gutman

CENTRAL ENGINEERING

STRATEGIC PLANS

RED BOOK

8/20/79

Copy Number 316

Issued to Pete Hempe

C O M P A N Y C O N F I D E N T I A L

A. Summary

INTRODUCTION

This Red Book represents Engineering's statement of the strategy developed during the last two quarters of FY79, in response to the Basic Product Strategy.

In addition to this Summary section, a copy of the Basic Product Strategy is included in Section B, and the strategies for each Engineering product development area (Small, Mid-range and Large Systems, Storage, and Software) in Sections C through G.

The Summary section includes the following:

A Central Engineering budget summary (page A-2).

For each of the five product development areas, a summary of its strategy and of its budget (page A-4 through A-14). While these summaries have not been reviewed with the strategy authors, we believe they accurately reflect the strategies.

Gospel charts showing the positioning of systems, storage subsystems, and operating systems for FY79 and for FY82 based on the strategies described in this Red Book (pages A-15 through A-20).

A baseline Product Calendar, drawn from the Red Book strategies, that will be tracked against during FY80 in the Yellow Book. In general, the Product Calendar includes products costing over $200K in FY80 development; some programs that will incur major expense in subsequent years are included even though under $200K in FY80 (pages A-21 through A-32).

CENTRAL ENGINEERING

FY80 BUDGET SUMMARY

($M)

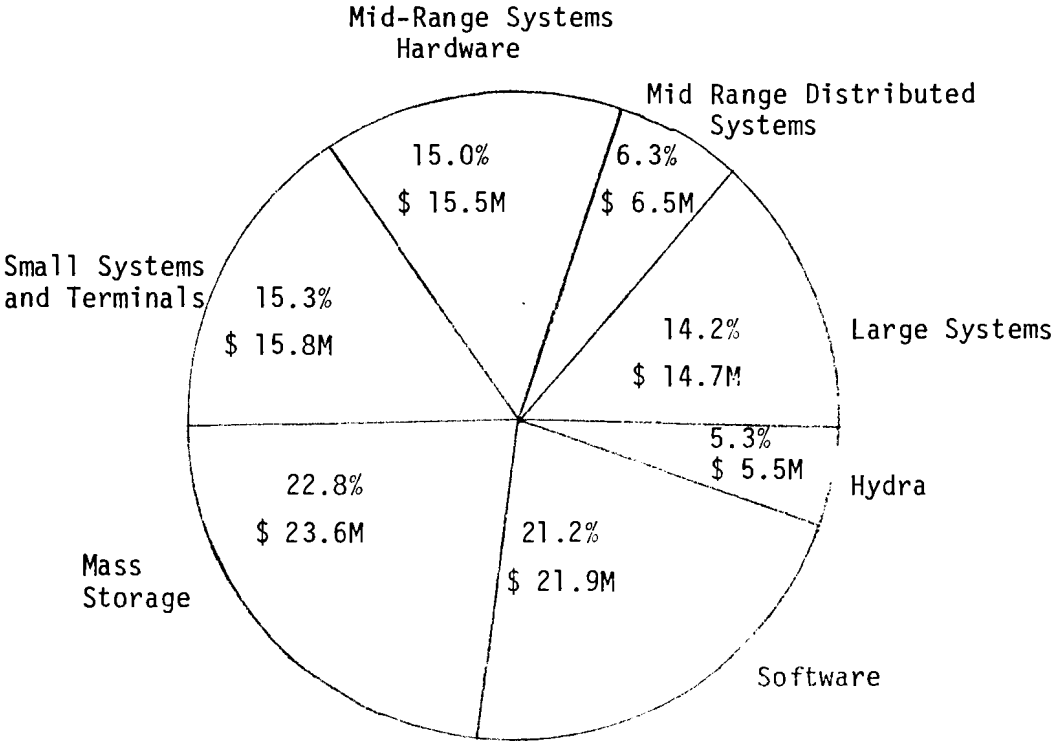
SOFTWARE	21.9
Hydra	5.5
Mass Storage	23.6
Small Systems	15.8
Med Systems Hardware	15.5
Dist. Systems	6.5
Large Systems	14.7
	103.5
All other eng. including	
Non-devel.	26.9
Unallocated	1.0
TOTAL	131.4

Central Engineering

FY80 Major Non Development Budgets

GROUP	MANAGER	FY80 BUDGET ($M)
LSI	Jim Cudmore	2.9
R&D	Jim Bell	2.2
Tech. Op.	John Holman	6.9
Tech. Dir.	Sam Fuller	1.4
Central Eng. Mgmt.	Larry Portner Gorden Bell	10.9
European Eng.	Dick Clayton	0.4
RAD/TRAD	Sam Fuller	2.2
		26.9

CENTRAL ENGINEERING FY '80 BUDGET SUMMARY



SOFTWARE, COMMUNICATIONS HARDWARE, & HYDRA

Emphasize VAX in mid-range and high-end software:

- focus new development on VAX
- reduce investment in nature PDP-11 and TOPS Software (RSTS,RX-11D, IAS, RT-11, RSX-11M, TOPS-10)
- complete more recent PDP-11 and TOPS Software (TRAX, RSX-11M PLUS, TOPS-20)

Invest in outer layers (languages, ease of use, etc.) of PDP-11 and TOPS product sets to maintain the customer base.

Develop compatible products:

- single VAX implementation of file structures, languages, applications, utilities, etc.
- new products designed for compatible VAX/PDP-11/TOPS user interfaces
- tools, aids, and documentation to support migration from PDP-11 to VAX and TOPS to VAX for existing products

Offer a superior distributed processing architecture (DNA) for our products, plus interconnect capability to IBM and public networks.

Make our software products easier to use:

- improve the human interface with non-procedural programming tools, and more accessible command languages, query languages, error messages, utilities, and documentation
- develop targeted products such as TRAX, MINC, SCS/RSTS
- simplify installation and improve serviceability

Meet the market requirements for high availability systems:

- RSX-11M PLUS on 11/74 MP
- TOPS multiprocessor systems
- HYDRA for leadership 32-bit high availability

SOFTWARE, COMMUNICATIONS HARDWARE AND HYDRA BUDGET

	FY80	FY81	FY82
Technical Systems	$ 3.5M	$ 3.9M	$ 4.7M
VAX Business Systems Enhancements	3.1	5.3	5.6
32 Bit Base Systems	2.6	3.1	3.8
RSTS	2.0	1.6	1.2
DEC-DEC Communications	1.9	2.7	0.8
16 Bit Base Systems	1.8	2.4	2.9
Information Management	1.8	3.1	2.1
Communications Hardware	1.8	2.0	1.7
DEC-IBM Communications	1.2	0.9	0.2
Terminal Software	1.2	1.4	1.7
Transaction Processing	1.0	1.7	1.9
Small Software Components	0.5	1.5	1.8
36/32 Bit Coexistence	0.2		
TOTAL Major Programs	$22.7M	$30.0M	$28.4M
Product Management/Planning	1.7		
Advanced Development	0.9		
Tools & Technology	0.6		
DECnet Certification	0.6		
Commercial Quality Management	0.5		
Systems Assurance	0.2		
Architecture	0.1		
Variance to be managed	(0.4)		
TOTAL Software & Comm. Hardware	$26.9M		
HYDRA	5.5	6.0	
TOTAL	$32.5M		

STORAGE SYSTEMS

Low End

Maintain hard disk leadership:

- migrate high-end technologies to low end
- develop new low-end technologies

Buy out flexible disks to achieve competitive parity.

Explore opportunities for cost-effective block mode ¼" tape with larger capacity.

Develop memory modules with standard RAMs and semi-custom LSI, integral control, and emphasize low-cost.

Mid-Range

Build "Winchester" technology base, and sustain investment in imbedded servo technology, to reach a highly competitive position in fixed disks. Maintain a timely buy out position in large removable disks.

Examine buy/build alternatives for cost competitive industry compatible ½" tape offering.

Evaluate new technologies for low cost, non-compatible backup and archival storage.

Move toward DEC standard peripheral interconnect.

Develop memory modules with ECC, integral and non-integral control, using standard RAMS and custom/semi-custom LSI.

High End

Buy out or license high-end disks from PCM-like developers to reduce IBM cost/MB lag from five to two years. Enhance competitiveness with high performance, intelligent storage subsystem attachments.

Buy out, with option to build, highest performance industry compatible ½" tape, pursue cost reduction through LSI.

Develop memory modules with ECC and non-integral control, using standard RAMS and custom/semi-custom LSI. Evaluate use of serial and partially good devices.

STORAGE SYSTEMS

	FY80	FY81	FY82
Low end development	$4.1M*		
Mid-range development	6.9	$15.4M	$10.6M
High end development	4.0		
Advanced development	3.4	4.1	4.9
Product management	0.8	1.0	1.2
Product support	1.6	2.0	2.5
Administration	0.5	0.7	0.7
Tools	1.7	1.9	2.0
Contingency	0.6	4.4	15.0
	$23.6M	$29.5M	$36.9M

* $2.2M for RL04/Aztec included in Low-End. Subject to EBOD review

CSD SMALL SYSTEMS & TERMINALS

LSI Chip Development

Develop a range of LSI CPU kernel chips:

- support current F-11 chip set for use in small and lower mid-range systems
- add an I/O map module for 2-mode extended addressing (PAX) in small systems*
- complete T-11 chip for use in very low end systems, terminals, and controllers, and evaluate follow-on products
- develop a chip set (J-11) with PDP-11/70 (74) performance and functionality for systems providing high-end PDP-11 capability at low-end cost (see PDP-11/xx in Mid-Range Systems plan, 11T73 in Small Systems)

Systems

Plan and integrate market-related software/hardware packages, based on product line identification of target packages and market needs:

- cost effective integrated hardware systems to satisfy common requirements
- added value to be supplied by OEMs or end user product lines
- applications solutions developed in CSD only under product line sponsorship

Enhance F-11 based systems capability by FY81 through extended addressing (PAX).

Provide higher performance and functionality in small PDP-11 systems, boxes, and boards in FY83 using the J-11 chip set (see Chips above), and the Backplane Interconnect/Network Interconnect (BI/NI) architecture.

Provide small VAX-11 systems in FY85-86 using the micro VAX chip set.

Introduce lower entry cost systems in FY81 based on the T-11 chip set and highly integrated packaging.

Provide engineering support for product line funded PDP-8 development.

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* In September, the status of BI/NI will determine the 11/23 and 11/24 strategy: 11/23 PAX and Unibus 11/24, or BI/NI 11/24 and no 11/23 PAX.

Video Terminals

Build on the VT100 modularity base:

- editing
  - VT132 in FY80
  - VT131 in FY81 at lower cost
- graphics
  - VT125 in FY81
  - VT225 in FY 82 with color
- programmability
  - VT211 in FY 82
- multidrop block mode communications
  - VT162 in FY80 for TRAX
  - VT131 in FY81
  - VT211 in FY82
- resolution (advanced development)

Reduce entry cost, with product line leadership and funding as appropriate:

- VT100 → VT101 in FY81 → VT 200 in FY82
- VT132 → VT131 in FY81

Printing Terminals

Build on impact dot matrix technology:

- graphics
  - LA34-V in FY81
- high resolution
  -LA24 in FY81

Reduce entry cost with LA12 personal portable terminal.

Introduce a full functionality 200 CPS family of terminals (LA200) in FY82, with block mode multidrop communication capability, to replace LA34/38, LA24 and LA120.

Introduce the lower cost LP25 300 line per minute printer, and the LP26 600 line per minute printer.

CSD BUDGET

Product Line Funding Not Included

	FY80		FY81	
DEVELOPMENT				
Chips	$2.9M		$4.2M	
Systems	1.0		1.6	
Video Terminals	1.3		1.5	
Print Terminals	3.4	8.7	4.1	11.3
SUPPORT				
Chips			0.3	
Systems	0.7		0.9	
Video Terminals	0.4		1.1	
Print Terminals	0.9	2.0	1.0	3.3
RESEARCH & ADV. DEV.				
Chips	0.8		0.3	
Systems	0.3		0.4	
Video Terminals	0.9		0.9	
Print Terminals	0.5	2.5	0.8	2.4
ADMINISTRATION				
Chips	0.1		0.2	
Systems	0.4		0.4	
Video Terminals	0.1		0.2	
Print Terminals	0.2		0.3	
Planning, PM, & Admin.	0.8	1.6	0.8	1.9
TOTAL Small Systems & Terminals		$14.8M		$18.9M
FUNCTIONAL ENGINEERING				
Systems engineering	1.9		2.6	
Power & pks systems	1.5	3.4	1.5	4.1
MECHANICAL ENGINEERING		0.2		0.2
TOTAL CSD		$18.3M		$23.2M

MID RANGE SYSTEMS

Complete PDP-11 processors currently under development:

- 11/74MP
- 11/44
- 11/24*

Implement a PDP-11 family replacement processor (PDP-11/XX) with 11/74 functionality and performance at 11/24 cost, based on the LSI-11/70 chip set, by FY83.

Develop and maintain a family of three 32 bit machines, interconnectable via an interprocessor bus or DECnet, to cover the $20K to $250K system price range:

- 11/780, replaced by Venus (Large Systems product) at 3.5 X 11/780 performance in FY82
- Comet (11/750), offering .6/.7 X 11/780 performance in FY80
- Nebula at .2/.3 X 11/780 performance in FY81, replaced at constant cost in FY84/85 by an LSI VAX-based machine or new technology applied to Nebula

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* In September, the status of BI/NI will determine 11/23 and 11/24 strategy: 11/23 PAX and Unibus 11/24, or BI/NI 11/24 and no 11/23 PAX.

MID-RANGE SYSTEMS

	FY80	FY81	FY82
VAX Systems	$ 7.2M	$10.7M	$11.8M
PDP-11 Systems	3.1	2.3	2.3
I/O Interconnect	0.8		
Advanced Development	0.9	1.9	2.0
Product Management	1.2	1.3	1.4
System Performance	0.3	0.3	0.5
Packaged Systems	0.6	0.7	0.6
Engineering Services	0.6	---	---
Administration	0.7	---	---
Contingency	0.1	1.0	1.5
TOTAL	$15.3M	$18.0M	$20.0M

LARGE SYSTEMS

Develop Venus-32 as a VAX-11/780 follow-on:

- 3.5 X 11/780 performance, supports VMS, PDP-11 compatibility mode, and SBI
- comparable price $99K entry, $180K design center system prices

Provide short-term growth for DEC system customers within the 36-bit space:

- 2080 processor, higher performance replacement for KL at comparable cost
- interconnect and homogeneous networking support

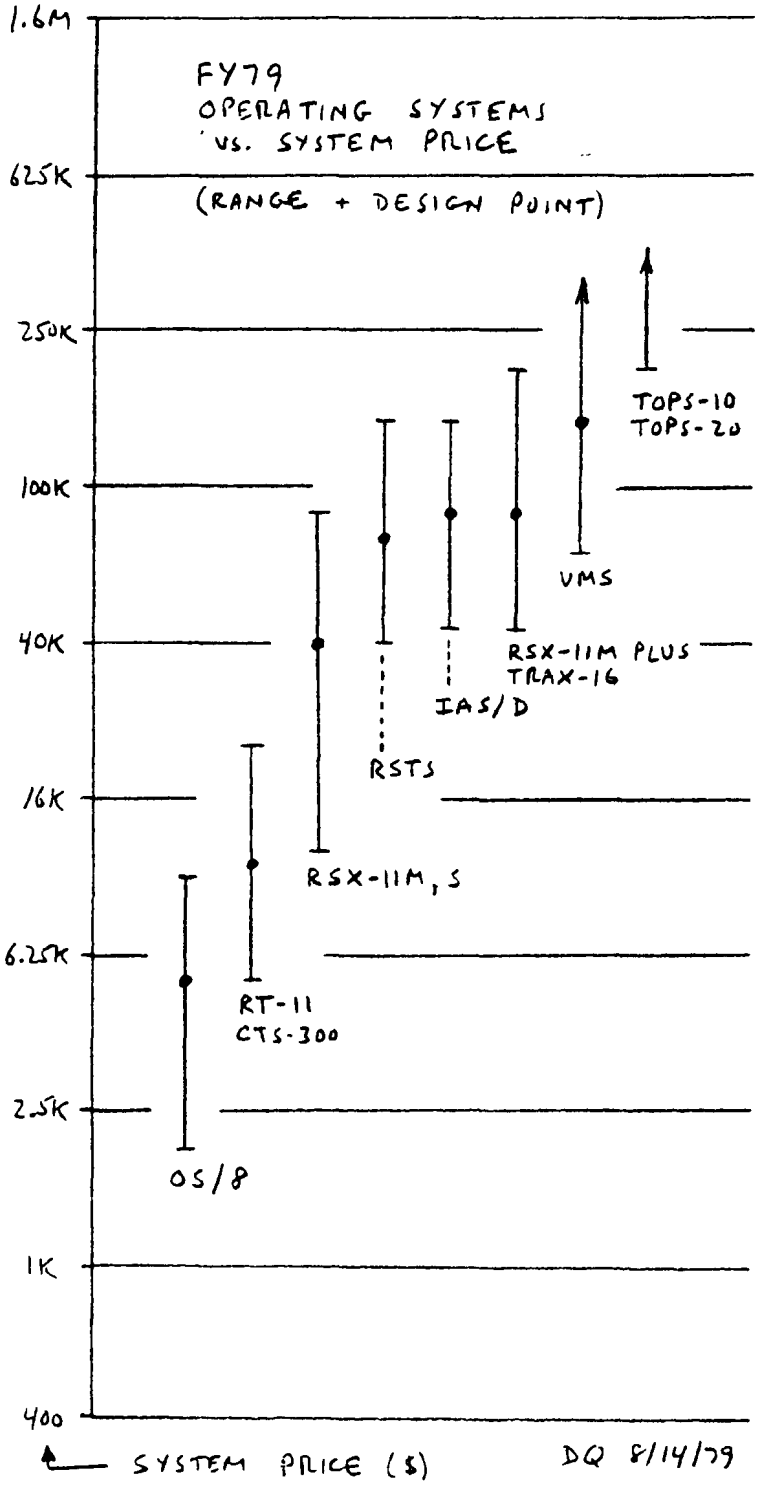
Facilitate long-term growth of DEC system customers using 32-bit systems:

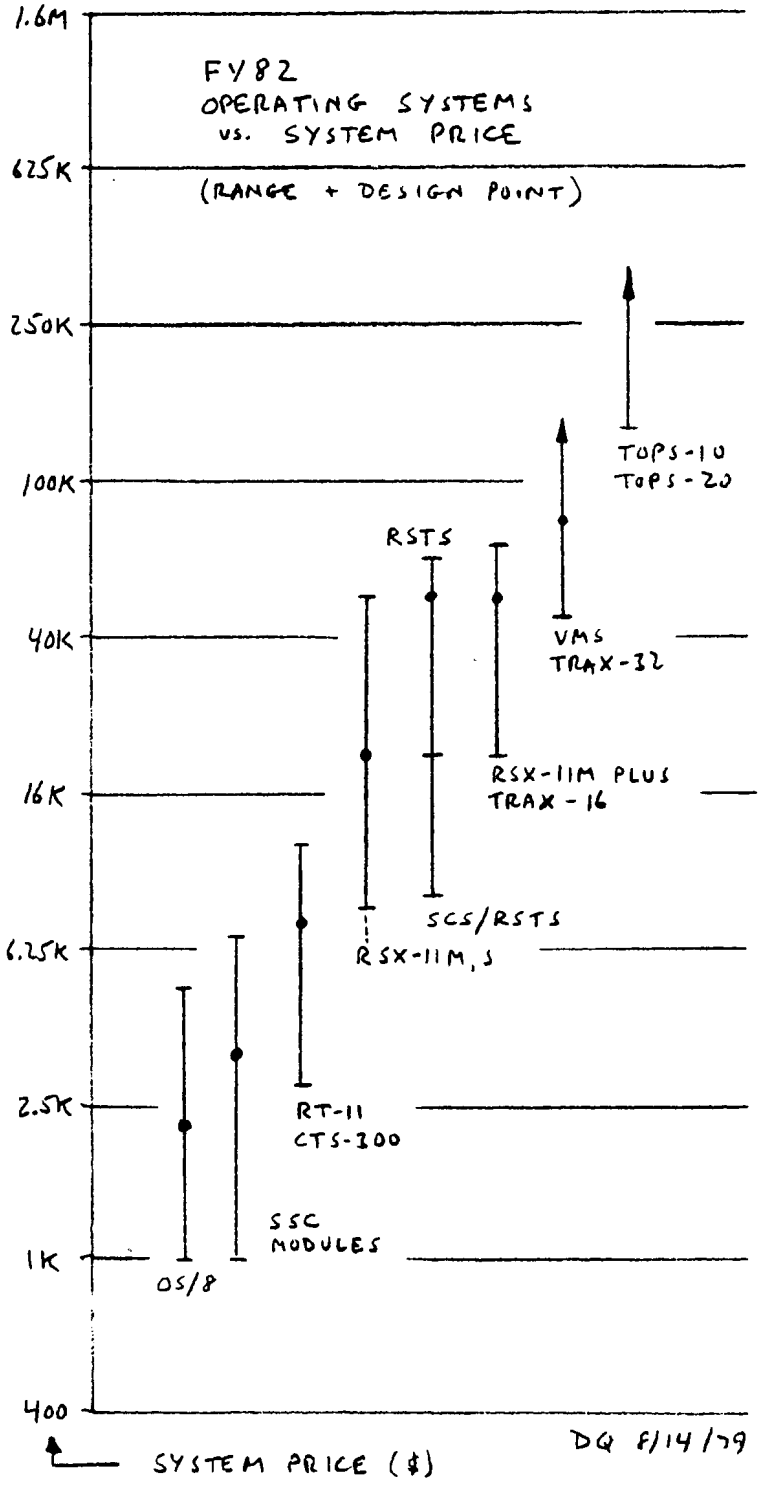
- applications languages syntactically compatible between 36 and 32 bit systems, where feasible.

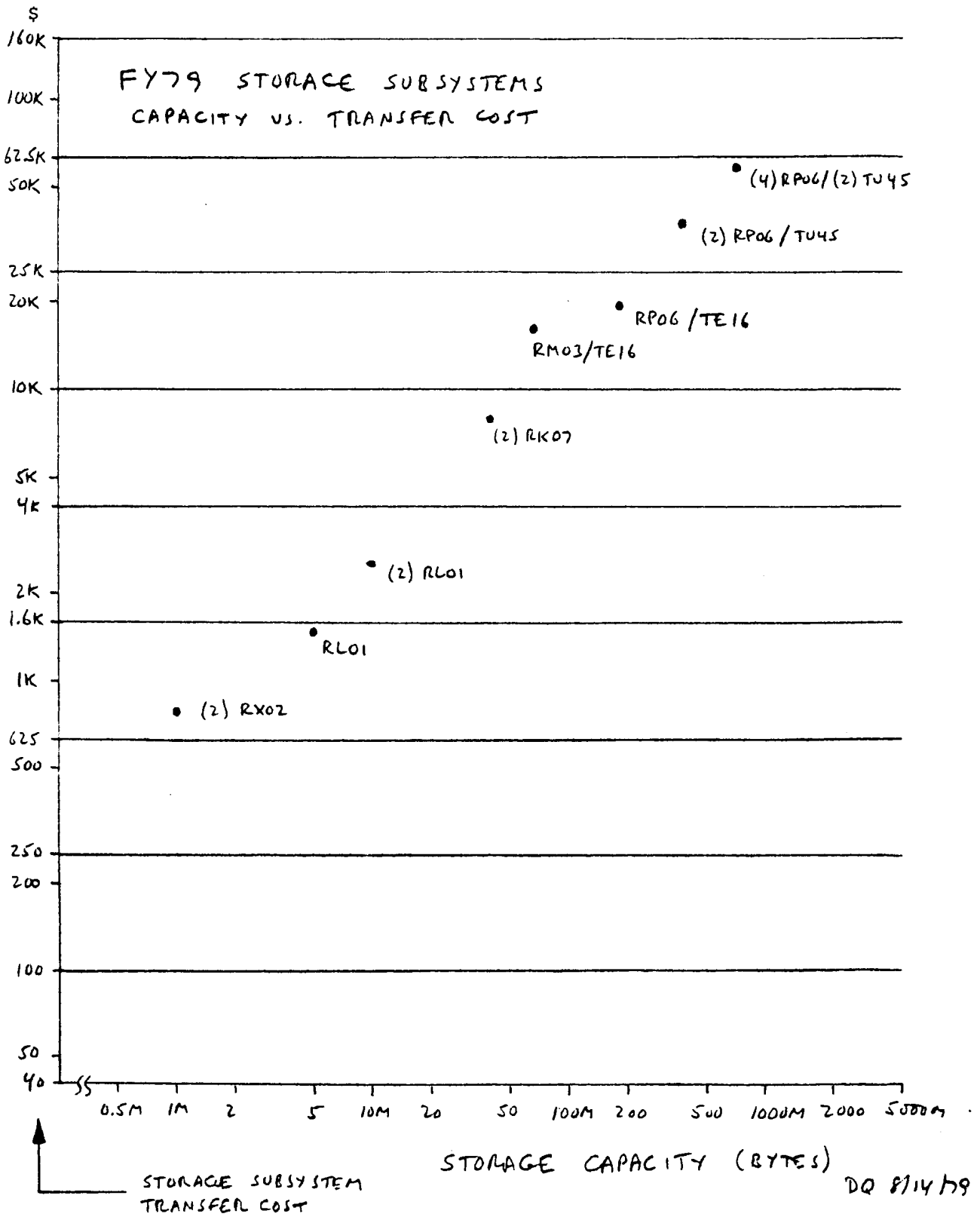
- heterogeneous networks for co-existence of 36 and 32 bit systems in a distributed processing configuration.

LARGE SYSTEMS BUDGET

	FY80	FY81	FY82
Venus	$ 3.9M	$ 5.5M	$ 4.0M
32 Bit Software	.4	.7	1.5
2080 (KL+)	1.6M	2.8M	2.5M
KL Service	1.0	1.0	----
KL, KS Hardware Support	1.0	1.1	1.2
36 Bit Software	3.0	3.5	3.0
Computers	2.2	3.4	2.9
Product Management	0.5	0.6	0.7
Research & Ana. Dev.	0.4	0.8	2.0
Administration	0.5	0.7	0.8
Contingency	0.5	1.4	7.5
TOTAL	$15.0M	$20.6M	$26.4M







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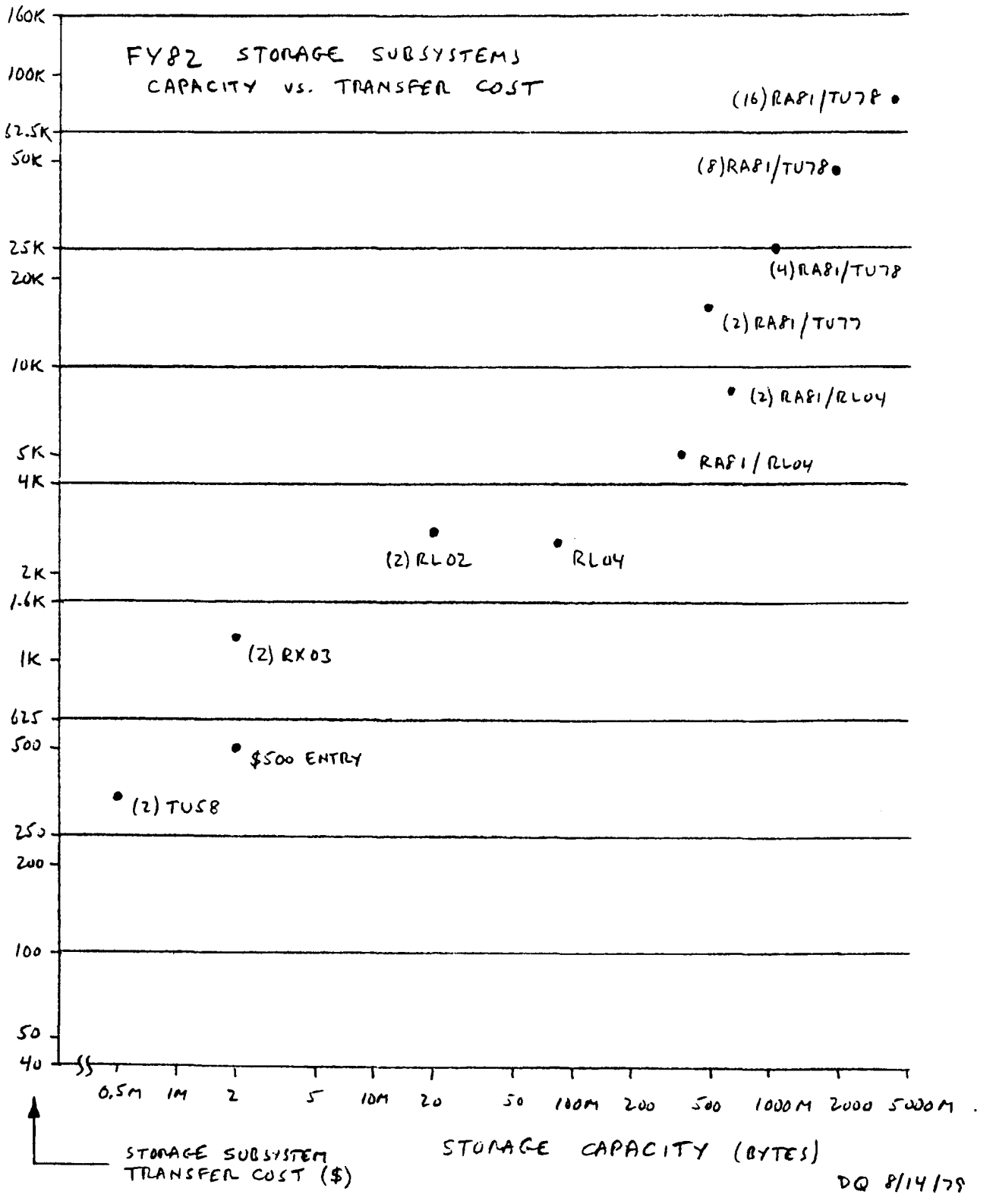

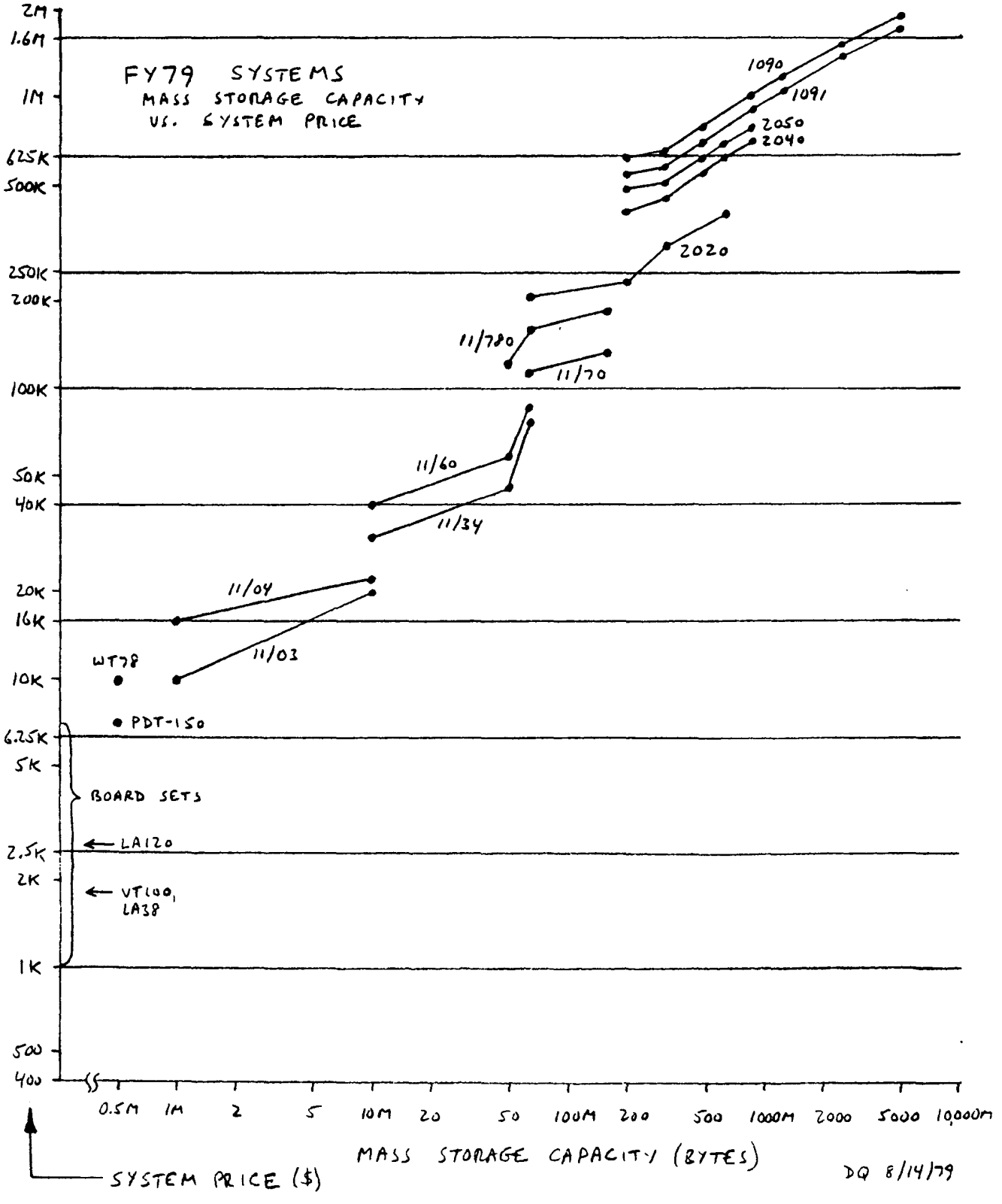

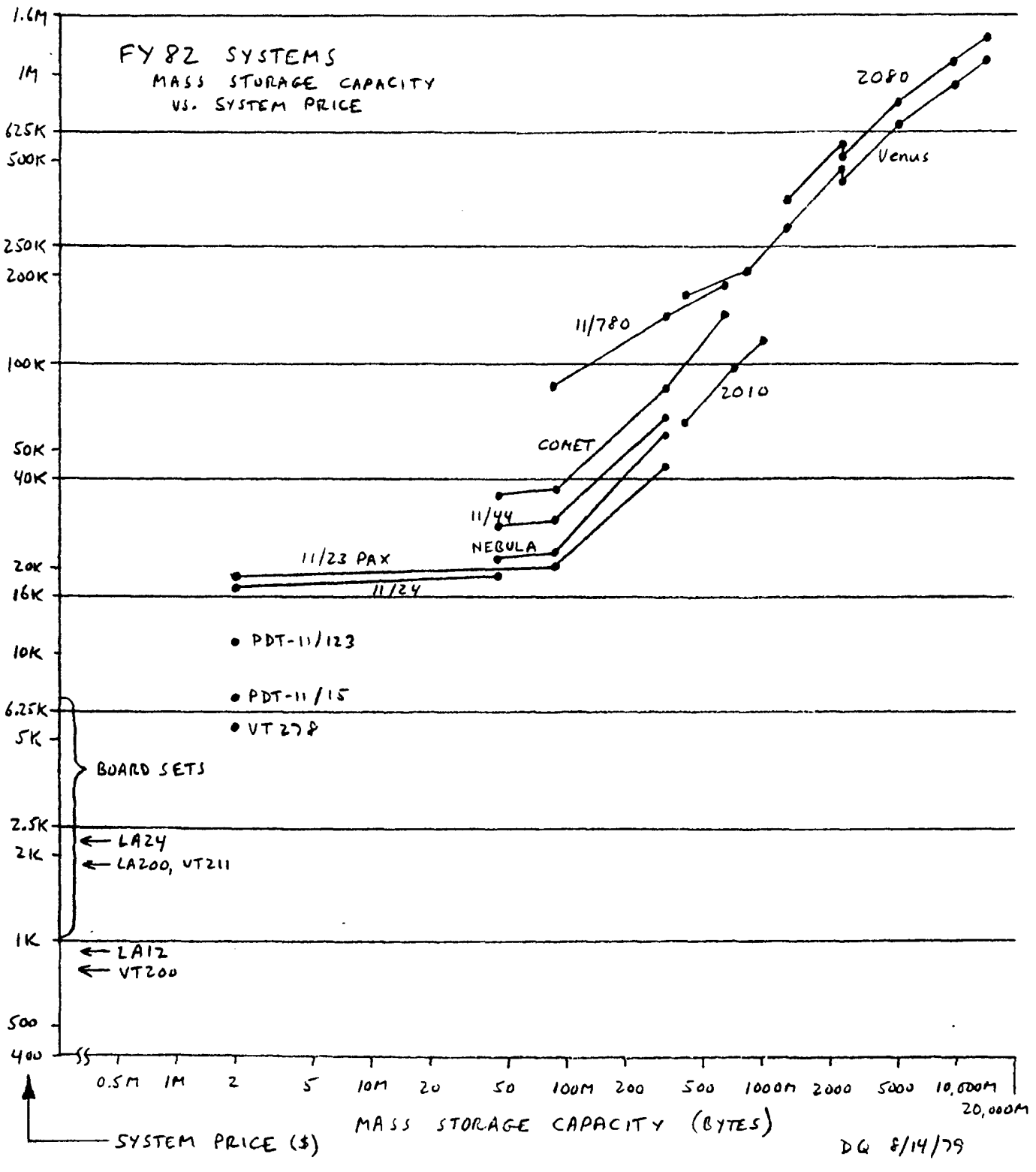

SOFTWARE & COMMERCIAL HARDWARE PRODUCT CALENDAR		FCS	EST. FY80 COST ($K)	PRODUCT MANAGER
32 bit Base Systems				
VMS V2.0	Comet and Nebula processors, other new devices, DECnet/VAX Phase III, enhanced file capability, native mode utilities		2617	Kathy Norris
VAX Business Systems Enhancements				
COBOL-79	VAX high end product replacing COBOL-74	1H, FY81	743	Dan D'Urso
BASIC-PLUS 2 V1.7				
CATS	Commercial Application Terminal Management System: forms, block mode, multidrop, including VT162 support		429	Roseann McLean
Object Time System (OTS) Run-Time Support Environment			462	Dan D'Urso
INFORMATION MANAGEMENT				
Datatrieve - 32	VAX implementation of inquiry/ report generation system with program-level access for native mode languages	1H, FY81	215	---
RMS-32	Enhancements to the basic VAX file system, including layered software support		215	---
DBMS-32		1H, FY82	429	---
TRANSACTION PROCESSING				
TRAX-32	VAX implementation of TRAX in a pure layered product		182	Cliff Conneighton
TRAX V2.0	Round out key TRAX features: full DECnet, 2280/3780, more terminals	1H, FY81	528	Cliff Conneighton
TECHNICAL SYSTEMS				
Fortran IV Plus	VAX implementation supporting ANSI-77 standard		260	Reid Brown

SOFTWARE & COMMERCIAL HARDWARE PRODUCT CALENDAR		FCS	EST. FY80 COST ($K)	PRODUCT MANAGER
Pascal Plus	VAX implementation		341	Reid Brown
MP enhancements	Extensions to RSX-11M for 11/74 MP support	1H, FY80	245	Steve Paavola
RT-11 V4.0	11/23, 11/24, 11/44 processors, other new device support, new sysgen, improved help file, PDT and very small system run time enhancements		325	Judi Hall
Small-M	Small RSX-11M enhancements for 11/23 and PDT		620	Steve Paavola
RSTS				
SCS/RSTS	Small business systems enhancements to RSTS: smaller configurations, ease of use, layered product	1H, FY81	479	Tony Jarmolych
ADE	Application development for SCS/RSTS	1H, FY81	280	Tony Jarmolych
Small Cobol		1H, FY81	330	Tony Jarmolych
Terminal Software				
FMS V2.0	Second question PDT software, migration to RSTS, RSX-11M, RSX-11M+, and VMS	2H, FY80	455	Bob Nusbaum
PDT Support	PDT V2.0 software, foreground communications, upgraded documentation		260	Bob Nusbaum
Small Software Components				
SSC/Pascal	Set of linkable Standard Software Components (SSC) for support of low-end run-time applications, PASCAL as implementation language, and application development support under RT-11		520	---
DEC - DEC COMMUNICATIONS				
DECnet Phase III	Routing, multidrop, remote terminals, and autodial networks functionality	1H, FY80 (RSX-11M, M+, CMS) 2H, FY80 (TRAX) 1H, FY81 (RSTS) 602		Stephan Johnson

SOFTWARE & COMMERCIAL HARDWARE PRODUCT CALENDAR		FCS	EST. FY80 COST ($K)	PRODUCT MANAGER
DECnet Phase IV	X.25 enhancement, X.25 support, network terminals, network management tools and services, Network Communications Controller	1H, FY81 (NCC)	204	Stephan Johnson
COMMUNICATIONS HARDWARE				
DMP11	Synchronous interface for Unibus, DDCMP protocol, multi-drop support for TRAX and other mid/high end systems		250	Dave Cleveland
DMV11	Synchronous interface for Qbus systems, DDCMP protocol, similar to DMP11		280	Dave Cleveland
HYDRA				
Hydra Systems	Multicomputer systems composed of VAX family processors configured for high availability/data integrity applications	2H, FY81	4,585	Ed Slaughter
Mercury	Family of communications subsystems, standard on Hydra and Venus, will also work with 11/780, Comet, Nebula, 2080. Up to 64 high-speed (9.6 - 56 KB/sec) sync/async lines per subsystem. Supported in VMS Release 3.	2H, FY81	915	M. Ressler
11/780 ICCS	High speed interprocessor link for 11/780	1H, FY81	(included in HYDRA & mid-range systems)	B. LaCroute/D. Rogers
Comet ICCS	High speed interprocessor link for Comet	Q2/Q3, FY81	(included in HYDRA)	B. LaCroute /D. Rogers

STORAGE SYSTEMS PRODUCT CALANDER

		FCS	VOLUME AVAILABILITY	EST. FY80 COST ($K)	PRODUCT MANAGER
Low End					
TU58	Very low cost .25MB block mode tape cartridge drive	Q1,FY80	Q3,FY80	100	C. Moeder
RL02	10MB disk, twice RL01 capacity at same cost, using existing RL01 controllers, for 11/23 through 11/44 class systems	Q2, FY80	Q2, FY80	514	W. Galusha
RX02	.5MB single sided double density floppy dist, RX01 compatible, for systems through 11/34 class	-	Shipping	260	P. Goldman
RX03	1MB double side, double density floppy disk, RX01 compatible, possibly RX02 compatible, to replace upgrade RX01 and RX02 in most applications.	Q1, FY81	Q2, FY81	950	P. Goldman
Aztec	30-42MB 8" fixed plus removable Winchester disk with integral control, at half RL02 cost (currently in advanced development)	2H, FY82	1H, FY83	2225	-
MSV11-K/L	64KB (250KB with 64K chips) dual height memory, replace MSV11-D/E, 22 bit addressing and Unibus CSR parity compatibility	Q1, FY81	Q3, FY81	100	C. LaRock
Mid-Range					
TS11 (was TS04)	45 lps, 1600 bpi IBM compatible tape drive with integral formatters, for 11/34 through 11/70 Unibus system.	Q1,FY80	Q2, FY80	300	K. Sills
RM80	128MB fixed Winchester disk, for Massbus	Q3, FY80	Q4, FY80	3429 (incl. RAPs)	K. Smith

Mid-Range (con't)		PCS	VOLUME AVAILABILITY	EST. FY80 COST	PRODUCT MANAGER
RA80	128MB fixed Winchester disk, using DEC Standard Disk Bus (SDB), for Unibus (via UDA) and ICCS (via HSC-50).	Q2, FY81	Q3, FY81	(in RM80)	K. Smith
RA81	250-400 MB fixed Winchester disk (enhanced RA80) for Unibus (via USA) and ICCS (via HSC-50).	Q1, FY82	Q2, FY82	570	K. Smith
RL04 *	84 MB fixed plus removable disk for Unibus (vis UDA) or ICCS (via HSC-50).	Q1, FY82	Q2, FY82	2225	W. Galusha
UDA	Standard Disk Bus (SDB) to Unibus interface for up to 4 RL04, RA80, RA81.	Q2, FY81	Q3, FY81	1122	
TS6250	6250 bpi, GCR, IBM compatible tape drive for under $5000 transfer cost.	2H, FY82	1H, FY83	850*	P. Peresten
MS11-M Upgrade	64K RAM, LSI ECC chip capacity for maximum capacity of 1MB per memory module.	1H, FY81	2H, FY81	156	C. LaRock
11/750 Upgrade	64K RAM capability for maximum capacity of 1MB per array.	1H, FY81	2H, FY81	232	C. LaRock
11/780 Upgrade	Double chip count and 64K RAM capability for maximum capacity of 1MB per array.	1H, FY81	2H, FY81	183	C. LaRock
High End					
RM05	256 MB, removable buyout disk for Massbus.	Q1, FY81	Q2, FY81	500	
TU77	125 cpi, 800/1600 bpi IBM compatible tape drive, to replace TU45 in 11/70 and larger systems.	Q4, FY79	Q1, FY80	100	P. Peresten
TU78	124 cps, 1600/6250 bpi IBM compatible tape drive, with 625 bpi GCR capability, for 11/780 and larger systems.	Q2, FY81	Q3, FY81	1000	P. Peresten

High End Cont'd

		FCS	VOLUME AVAILABILITY	COST	PRODUCT MANAGER
RP07 (was RP07+)	516 MB fixed disk with integral Massbus interface for 11/70 and larger systems. Optional dual access.	Q2, FY81	Q3, FY81	500	P. Feresten
HSC-50	Intelligent storage subsystem control interfacing Standard Disk Bus (SDB) devices. (RL04 , RA80, RA81) to the ICCS bus. Error correction internal diagnostics, optional cache.	Q3,FY82	2H, FY82	1929	J. Woelbern

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* To be reviewed Q1, FY 80 by EBCD

SMALL SYSTEMS & TERMINALS PRODUCT CALENDAR		FCS	EST. FY80 COST ($K)	PRODUCT MANAGER
Chips:				
T-11(Tiny-11)	Single-chip PDP-11 for controllers and low-end systems	Q3, FY80	1200	---
F-11 (FONZ-11)	PDP-11 chip set with 11/34 functionality and near 11/34 performance at 11/03 cost	Shipping	600	G. Delaney
J-11 (LSI-11/70)	PDP-11 chip set with 11/70 (74) functionality and performance at 11/03 cost, based on BI/NI for low end systems	FY83[t]	1150	---
Micro VAX	VAX-11 chip set	FY85-86[t]	650	---
Systems				
11T23,11V23	11/23 systems with dual RL01 (T) or RX02 (V) ($FY80 includes 11/23 and 11/03 box funding)	Q2, FY80	224	H. Allard
11/23P Module*	Board-level 11/23 processor with 4MB addressing (PAX) and CIS	Q1, FY81[t]	539	H. Allard
11T23P,11V23P*	11/23P systems with dual hard (T) or floppy (V) disks	Q1, FY81[t]		
KMV11	F-11 based programmable communications controller. 2 synchronous 19.2KB lines with modem control.	Q1, FY81[t]	210	D. Quimby
PDT-11/15	Lower cost PDT-150 product using T-11 and VT101	FY81[t]	60	---
Video Terminals:				
VT100 printer Port	Serial port for hard copy output	Q3, FY80	168	D. Reed
VT101	Low cost ($350) VT100 (was VT100L)	Q1, FY81[t]	658	D. Reed
VT131	VT101 with block mode and editing functionality	Q1, FY81[t]	included in VT101	D. Reed

SMALL SYSTEMS & TERMINALS PRODUCT CALENDAR

		FCS	EST. FY80 COST ($K)	PRODUCT MANAGER
VT125	VT100-based graphics terminal, supports firmware based protocol	Q1, FY81[t]	167	J. Cox
VT200	Super low cost ($200) VT100	FY82[t]	245	D. Cotton
VT211	Block mode, multidrop video terminal with programmable extension capabilities, using T-11 as controller, at VT100 cost.	FY82[t]	440	J. Cox
Print Terminals:				
LA34	Low cost, table top 30 CPS interactive dot matrix terminal	Shipping	100	W. Seaver
LA34-V	Low speed graphics printer (formerly LA34G)	Q1, FY81[t]	62	W. Seaver
LA12	Personal 30 cps portable terminal	Q1, FY81[t]	1100	
LA24	High resolution dot matrix printer	Q2, FY81[t]	800	D. Cotton
LA200 family	Block mode, multidrop 200 cps terminal family, replacing LA34/78, LA24, LA120, using T-11 as controller	Q2, FY82[t]	1100	D. Cotton
LP25	300 LPM band type line printer, 25% lower cost than LP05	Q2, FY80	300	T. Dundon
LP26	600 LPM band type line printer	Q2, FY81	300	T. Dundon
Product Line Funded				
PDT-11/123	Higher performance PDT-150 follow-on using F-11, Qbus backplane, and dual floppy disks	Q3, FY80	400	Commercial Group
HG120	PDP-8 chip set		150	PDP-8 (?)

SMALL SYSTEMS & TERMINALS PRODUCT CALENDAR

		FCS	$FY80	Development Manager	Product Manager
VT278	PDP-8 CPU in VT100, 3 times VT78 processor performance, packaged with dual floppy discs, for single user small business systems	Q1, FY81[t]	1009		PDP-8 (?)
VT378	VT278 with bubble memory and TV58 cartrige tape instead of floppies		497		PDP-8 (?)
VK100	Keyboard packaged controller for external color or B/W monitor, including bit mapped graphics	Q1, FY81[t]	523		ECS
VT162	Block mode fixed functionality terminal for TRAX, using F-11	Q4, FY80	260		Commercial Group
VT132	VT100 with editing functionality	Q1, FY80			DCG

* 11/23 PAX reaches a decision point in September: depending on the status of Backplane Interconnect/Network Interconnect (BI/NI), BI/NI 11/24 may replace 11/23 PAX.

MID-RANGE PRODUCT CALENDAR

		FCS	VOLUME AVAILABILITY	EST. FY80 COST ($K)	PRODUCT MANAGER
PDP-11 11/74 MP	Shared memory multi-processor version of 11/70 using high availability packaging	Nov 79	Feb 80	854	M. Powell
11/44	PDP-11/34 class processor with 22 bit addressing, 1 MB physical memory, and optional CIS, to replace low end 11/60 and high end 11/34.	Nov 79	Mar 80	860	T. Sherman
11/24	F-11 based processor for Unibus market. Will be implemented either as a Unibus processor or a Backplane Interconnect (BI) processor - decision scheduled for September.	on hold	---	550	M. Torla
VAX Comet (11/750)	VAX processor .6 to .7 X 11/780 performance, with CIS and Unibus, 8 MB memory capability optional floating point accellerator and Massbus	Dec 79	Jun 80	3033	D. McInnis
NEBULA	VAX processor, .2 to .3 X 11/780 performance, CIS, 3 MB memory capability, optional floating point accellerator. Unibus at FCS, Backplane Interconnect (BI) FY82.	Q1/Q2 FY81	Q3/Q4 FY81	2505	L. Phillipon
EXTENDED FLOATING POINT	Micro code to support extended floating point exponent range for 11/780 and Comet.	Q2, FY80 (11/780)	Q2/FY80 (11/780)	420 (includes 300 PL)	A. Avery/D. McInnes
MA 780	Multiport memory for up to 4 VAX-11/780 processor	Nov 79	N/A	269	A. Avery
DR 780	High speed 32 bit parallel interface with software driver for VAX-11/780	Q3, FY80	N/A	342	A. Avery
MA 750	Multiport memory for up to 4 VAX-11/750 (Comet) processors			284	D. McInnes
DR 750	High speed 32 bit parallel interface for VAX-11/750 (Comet)			357	D. McInnes

LARGE SYSTEMS PRODUCT CALENDAR

		FCS	VOLUME AVAILABILITY	EST. FY80 COST	PRODUCT MANAGER
32 BIT					
Venus 32	VAX processor with 3.5 X 11/780 performance at comparable cost, supporting new I/O architecture (ICCS, HSC-50, Mercury). PDP-11 compatibility mode and SBI for 11/780 migration.	Q2, FY82	Q4,FY82	3905	C. Gibson
APL		?		167	A. Toth
STORAGE					
STC 8650	1200 MB Buyout disk drive	Q4, FY80		169	J. Viula
36 BIT					
2080 (KL+)	Higher performance replacement for KL processor at comparable cost, runs TOPS-10 and TOPS-20.			1538	
TOPS-10 7.00	Symmetric multiprocessor (SMP) support and RAMP features for existing dual KI or KL sites only	Q2, FY80	N/A	305	M. Tseng
TOPS-10 7:01	General release with SMP and new device support, RAMP features, 2020 network support	Q4, FY80	N/A	392	M. Tseng
TOPS-20 REL 4			N/A	480	L. Hruby
TOPS-20 REL 5			N/A	179	L. Hruby
FORTRAN V6	Native mode operation on DEC system-20s, improved performance with RAMP	Mar 80	N/A	114	A. Toth
FORTRAN V7	ANS '78 standard features for transportability with VMS Fortran, interface to RMS.	Jun 81	N/A	78	A. Toth

LARGE SYSTEMS PRODUCT CALENDAR

		FCS	VOLUME AVAILABILITY	EST. FY80 COST	PRODUCT MANAGER
COBOL 68/74 V12A/V13	Stabilized product with improved I/O performance, both compilers on one tape, interface to RMS-20.	Q4, FY81	N/A	264	A. Toth
DBMS V.6	Improved quality, ease of use, and price/performance	Q4, FY80	N/A	208	A. Toth
DBMS V.7	Improved functionability with data dictionary, extensibility features for dynamic change	FY 81	N/A	86	A. Toth
RMS-20	File management compatible with 32 and 16 bit RMS implementations; COBOL and FORTRAN interfaces planned, currently interfaces to BASIC PLUS 2			111	A. Toth

SOFTWARE & COMMERCIAL HARDWARE PRODUCT CALENDAR		FCS	EST. FY80 COST ($K)	PRODUCT MANAGER
32 bit Base Systems				
VMS V2.0	Comet and Nebula processors, other new devices, DECnet/VAX Phase III, enhanced file capability, native mode utilities		2617	Kathy Morris
VAX Business Systems Enhancements				
COBOL-79	VAX high end product replacing COBOL-74	1H, FY81	743	Dan D'Urso
BASIC-PLUS 2 V1.7				
CATS	Commercial Application Terminal Management System: forms, block mode, multidrop, including VT162 support		429	Roseann McLean
Object Time System (OTS) Run-Time Support Environment			462	Dan D'Urso
INFORMATION MANAGEMENT				
Datatrieve - 32	VAX implementation of inquiry/ report generation system with program-level access for native mode languages	1H, FY81	215	---
RMS-32	Enhancements to the basic VAX file system, including layered software support		215	---
DBMS-32		1H, FY82	429	---
TRANSACTION PROCESSING				
TRAX-32	VAX implementation of TRAX in a pure layered product		182	Cliff Conneighton
TRAX V2.0	Round out key TRAX features: full DECnet, 2280/3780, more terminals	1H, FY81	528	Cliff Conneighton
TECHNICAL SYSTEMS				
Fortran IV Plus	VAX implementation supporting ANSI-77 standard		260	Reid Brown

SOFTWARE & COMMERCIAL HARDWARE PRODUCT CALENDAR

		FCS	EST. FY80 COST ($K)	PRODUCT MANAGER
Pascal Plus	VAX implementation		341	Reid Brown
MP enhancements	Extensions to RSX-11M for 11/74 MP support	1H, FY80	245	Steve Paavola
RT-11 V4.0	11/23, 11/24, 11/44 processors, other new device support, new sysgen, improved help file, PDT and very small system run time enhancements		325	Judi Hall
Small-M	Small RSX-11M enhancements for 11/23 and PDT		620	Steve Paavola
RSTS				
SCS/RSTS	Small business systems enhancements to RSTS: smaller configurations, ease of use, layered product	1H, FY81	479	Tony Jarmolych
ADE	Application development for SCS/RSTS	1H, FY81	280	Tony Jarmolych
Small Cobol		1H, FY81	330	Tony Jarmolych
Terminal Software				
FMS V2.0	Second question PDT software, migration to RSTS, RSX-11M, RSX-11M+, and VMS	2H, FY80	455	Bob Nusbaum
PDT Support	PDT V2.0 software, foreground communications, upgraded documentation		260	Bob Nusbaum
Small Software Components				
SSC/Pascal	Set of linkable Standard Software Components (SSC) for support of low-end run-time applications, PASCAL as implementation language, and application development support under RT-11		520	---
DEC - DEC COMMUNICATIONS				
DECnet Phase III	Routing, multidrop, remote terminals, and autodial networks functionality	1H, FY80 (RSX-11M, M+, CMS) 2H, FY80 (TRAX) 1H, FY81 (RSTS) 602		Stephan Johnson

SOFTWARE & COMMERCIAL HARDWARE PRODUCT CALENDAR		FCS	EST. FY80 COST ($K)	PRODUCT MANAGER
DECnet Phase IV	X.25 enhancement, X.25 support, network terminals, network management tools and services, Network Communications Controller	1H, FY81 (NCC)	204	Stephan Johnson
COMMUNICATIONS HARDWARE				
DMP11	Synchronous interface for Unibus, DDCMP protocol, multi-drop support for TRAX and other mid/high end systems		250	Dave Cleveland
DMV11	Synchronous interface for Qbus systems, DDCMP protocol, similar to DMP11		280	Dave Cleveland
HYDRA				
Hydra Systems	Multicomputer systems composed of VAX family processors configured for high availability/data integrity applications	2H, FY81	4,585	Ed Slaughter
Mercury	Family of communications subsystems, standard on Hydra and Venus, will also work with 11/780, Comet, Nebula, 2080. Up to 64 high-speed (9.6 - 56 KB/sec) sync/async lines per subsystem. Supported in VMS Release 3.	2H, FY81	915	M. Ressler
11/780 ICCS	High speed interprocessor link for 11/780	1H, FY81	(included in HYDRA & mid-range systems)	B. LaCroute/D. Rogers
Comet ICCS	High speed interprocessor link for Comet	Q2/Q3, FY81	(included in HYDRA)	B. LaCroute /D. Rogers

STORAGE SYSTEMS PRODUCT CALANDER

		FCS	VOLUME AVAILABILITY	EST. FY80 COST ($K)	PRODUCT MANAGER
Low End					
TU58	Very low cost .25MB block mode tape cartridge drive	Q1,FY80	Q3,FY80	100	C. Moeder
RL02	10MB disk, twice RL01 capacity at same cost, using existing RL01 controllers, for 11/23 through 11/44 class systems	Q2, FY80	Q2, FY80	514	W. Galusha
RX02	.5MB single sided double density floppy dist, RX01 compatible, for systems through 11/34 class	-	Shipping	260	P. Goldman
RX03	1MB double side, double density floppy disk, RX01 compatible, possibly RX02 compatible, to replace upgrade RX01 and RX02 in most applications.	Q1, FY81	Q2, FY81	950	P. Goldman
Aztec	30-42MB 8" fixed plus removable Winchestet disk with integral control, at half RL02 cost (currently in advanced development)	2H, FY82	1H, FY83	2225	-
MSV11-K/L	64KB (250KB with 64K chips) dual height memory, replace MSV11-D/E, 22 bit addressing and Unibus CSR parity compatibility	Q1, FY81	Q3, FY81	100	C. LaRock
Mid-Range					
TS11 (was TS04)	45 lps, 1600 bpi IBM compatible tape drive with integral formatters, for 11/34 through 11/70 Unibus system.	Q1,FY80	Q2, FY80	300	K. Sills
RM80	120MB fixed Winchester disk, for Massbus	Q3, FY80	Q4, FY80	3429 (incl. RAPa)	K. Smith

Mid-Range (con't)		FCS	VOLUME AVAILABILITY	EST. FY80 COST	PRODUCT MANAGER
RA80	128MB fixed Winchester disk, using DEC Standard Disk Bus (SDB), for Unibus (via UDA) and ICCS (via HSC-50).	Q2, FY81	Q3, FY81	(in RM80)	K. Smith
RA81	250-400 MB fixed Winchester disk (enhanced RA80) for Unibus (via USA) and ICCS (via HSC-50).	Q1, FY82	Q2, FY82	570	K. Smith
RL04 *	84 MB fixed plus removable disk for Unibus (vis UDA) or ICCS (via HSC-50).	Q1, FY82	Q2, FY82	2225	W. Galusha
UDA	Standard Disk Bus (SDB) to Unibus interface for up to 4 RL04, RA80, RA81.	Q2, FY81	Q3, FY81	1122	
TS6250	6250 bpi, GCR, IBM compatible tape drive for under $5000 transfer cost.	2H, FY82	1H, FY83	850*	P. Feresten
MS11-M Upgrade	64K RAM, LSI ECC chip capacity for maximum capacity of 1MB per memory module.	1H, FY81	2H, FY81	156	C. LaRock
11/750 Upgrade	64K RAM capability for maximum capacity of 1MB per array.	1H, FY81	2H, FY81	232	C. LaRock
11/780 Upgrade	Double chip count and 64K RAM capability for maximum capacity of 1MB per array.	1H, FY81	2H, FY81	183	C. LaRock
High End					
RM05	256 MB, removable buyout disk for Massbus.	Q1, FY81	Q2, FY81	500	
TU77	125 cpi, 800/1600 bpi IBM compatible tape drive, to replace TU45 in 11/70 and larger systems.	Q4, FY79	Q1, FY80	100	P. Feresten
TU78	124 cps, 1600/6250 bpi IBM compatible tape drive, with 625 bpi GCR capability, for 11/780 and larger systems.	Q2, FY81	Q3, FY81	1000	P. Feresten

High End Cont'd

		FCS	VOLUME AVAILABILITY	COST	PRODUCT MANAGER
RP07 (was RP07+)	516 MB fixed disk with integral Massbus interface for 11/70 and larger systems. Optional dual access.	Q2, FY81	Q3, FY81	500	P. Feresten
HSC-50	Intelligent storage subsystem control interfacing Standard Disk Bus (SDB) devices. (RL04 , RA80, RA81) to the ICCS bus. Error correction internal diagnostics, optional cache.	Q3,FY82	2H, FY82	1929	J. Woelbern

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* To be reviewed Q1, FY 80 by EBOD

SMALL SYSTEMS & TERMINALS PRODUCT CALENDAR		FCS	EST. FY80 COST ($K)	PRODUCT MANAGER
Chips:				
T-11(Tiny-11)	Single-chip PDP-11 for controllers and low-end systems	Q3, FY80	1200	---
F-11 (FONZ-11)	PDP-11 chip set with 11/34 functionality and near 11/34 performance at 11/03 cost	Shipping	600	G. Delaney
J-11 (LSI-11/70)	PDP-11 chip set with 11/70 (74) functionality and performance at 11/03 cost, based on BI/NI for low end systems	FY83[t]	1150	---
Micro VAX	VAX-11 chip set	FY85-86[t]	650	---
Systems				
11T23,11V23	11/23 systems with dual RL01 (T) or RX02 (V) ($FY80 includes 11/23 and 11/03 box funding)	Q2, FY80	224	H. Allard
11/23P Module*	Board-level 11/23 processor with 4MB addressing (PAX) and CIS	Q1, FY81[t]	539	H. Allard
11T23P,11V23P*	11/23P systems with dual hard (T) or floppy (V) disks	Q1, FY81[t]		
KMV11	F-11 based programmable communications controller. 2 synchronous 19.2KB lines with modem control.	Q1, FY81[t]	210	D. Quimby
PDT-11/15	Lower cost PDT-150 product using T-11 and VT101	FY81[t]	60	---
Video Terminals:				
VT100 printer Port	Serial port for hard copy output	Q3, FY80	168	D. Reed
VT101	Low cost ($350) VT100 (was VT100L)	Q1, FY81[t]	658	D. Reed
VT131	VT101 with block mode and editing functionality	Q1, FY81[t]	included in VT101	D. Reed

SMALL SYSTEMS & TERMINALS PRODUCT CALENDAR

		FCS	EST. FY80 COST ($K)	PRODUCT MANAGER
VT125	VT100-based graphics terminal, support# firmware based protocol	Q1, FY81[t]	167	J. Cox
VT200	Super low cost ($200) VT100	FY82[t]	245	D. Cotton
VT211	Block mode, multidrop video terminal with programmable extension capabilities, using T-11 as controller, at VT100 cost.	FY82[t]	440	J. Cox
Print Terminals:				
LA34	Low cost, table top 30 CPS interactive dot matrix terminal	Shipping	100	W. Seaver
LA34-V	Low speed graphics printer (formerly LA34G)	Q1, FY81[t]	62	W. Seaver
LA12	Fersonal 30 cps portable terminal	Q1, FY81[t]	1100	
LA24	High resolution dot matrix printer	Q2, FY81[t]	800	D. Cotton
LA200 family	Block mode, multidrop 200 cps terminal family, replacing LA34/78, LA24, LA120, using T-11 as controller	Q2, FY82[t]	1100	D. Cotton
LP25	300 LPM band type line printer, 25% lower cost than LP05	Q2, FY80	300	T. Dundon
LP26	600 LPM band type line printer	Q2, FY81	300	T. Dundon
Product Line Funded				
PDT-11/123	Higher performance PDT-150 follow-on using F-11, Qbus backplane, and dual floppy disks	Q3, FY80	400	Commercial Group
HG120	PDP-8 chip set		150	PDP-8 (?)

SMALL SYSTEMS & TERMINALS PRODUCT CALENDAR

		FCS	$FY80	Development Manager	Product Manager
VT278	PDP-8 CPU in VT100, 3 times VT78 processor performance, packaged with dual floppy discs, for single user small business systems	Q1, FY81*	1009		PDP-8 (?)
VT378	VT278 with bubble memory and TV58 cartrige tape instead of floppies		497		PDP-8 (?)
VK100	Keyboard packaged controller for external color or B/W monitor, including bit mapped graphics	Q1, FY81*	523		ECS
VT162	Block mode fixed functionality terminal for TRAX, using F-11	Q4, FY80	260		Commercial Group
VT132	VT100 with editing functionality	Q1, FY80			DCG

* 11/23 PAX reaches a decision point in September; depending on the status of Backplane Interconnect/Network Interconnect (BI/NI), BI/NI 11/24 may replace 11/23 PAX.

MID-RANGE PRODUCT CALENDAR

		FCS	VOLUME AVAILABILITY	EST. FY80 COST ($K)	PRODUCT MANAGER
PDP-11 11/74 MP	Shared memory multi-processor version of 11/70 using high availability packaging	Nov 79	Feb 80	854	M. Powell
11/44	PDP-11/34 class processor with 22 bit addressing, 1 MB physical memory, and optional CIS, to replace low end 11/60 and high end 11/34.	Nov 79	Mar 80	860	T. Sherman
11/24	F-11 based processor for Unibus market. Will be implemented either as a Unibus processor or a Backplane Interconnect (BI) processor - decision scheduled for September.	on hold	---	550	M. Torla
VAX Comet (11/750)	VAX processor .6 to .7 X 11/780 performance, with CIS and Unibus, 8 MB memory capability optional floating point accellerator and Massbus	Dec 79	Jun 80	3033	D. McInnis
NEBULA	VAX processor, .2 to .3 X 11/780 performance, CIS, 3 MB memory capability, optional floating point accellerator. Unibus at FCS, Backplane Interconnect (BI) FY82.	Q1/Q2 FY81	Q3/Q4 FY81	2505	L. Phillipon
EXTENDED FLOATING POINT	Micro code to support extended floating point exponent range for 11/780 and Comet.	Q2, FY80 (11/780)	Q2/FY80 (11/780)	420 (includes 300 PL)	A. Avery/D. McInnes
MA 780	Multiport memory for up to 4 VAX-11/780 processor	Nov 79	N/A	269	A. Avery
DR 780	High speed 32 bit parallel interface with software driver for VAX-11/780	Q1, FY80	N/A	342	A. Avery
MA 750	Multiport memory for up to 4 VAX-11/750 (Comet) processors			234	D. McInnes
DR 750	High speed 32 bit paraliel interface for VAX-11/750 (Comet)			357	D. McInnes

LARGE SYSTEMS PRODUCT CALENDAR

		FCS	VOLUME AVAILABILITY	EST. FY80 COST	PRODUCT MANAGER
32 BIT					
Venus 32	VAX processor with 3.5 X 11/780 performance at comparable cost, supporting new I/O architecture (ICCS, HSC-50, Mercury). PDP-11 compatibility mode and SBI for 11/780 migration.	Q2, FY82	Q4,FY82	3905	C. Gibson
APL		?		167	A. Toth
STORAGE					
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36 BIT					
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TOPS-10 7:01	General release with SMP and new device support, RAMP features, 2020 network support	Q4, FY80	N/A	392	M. Tseng
TOPS-20 REL 4			N/A	480	L. Hruby
TOPS-20 REL 5			N/A	179	L. Hruby
FORTRAN V6	Native mode operation on DEC system-20s, improved performance with RAMP	Mar 80	N/A	114	A. Toth
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		FCS	VOLUME AVAILABILITY	EST. FY80 COST	PRODUCT MANAGER
COBOL 68/74 V12A/V13	Stabilized product with improved I/O performance, both compilers on one tape, interface to RMS-20.	Q4, FY81	N/A	264	A. Toth
DBMS V.6	Improved quality, ease of use, and price/performance	Q4, FY80	N/A	208	A. Toth
DBMS V.7	Improved functionability with data dictionary, extensibility features for dynamic change	FY 81	N/A	86	A. Toth
RMS-20	File management compatible with 32 and 16 bit RMS implementations; COBOL and FORTRAN interfaces planned, currently interfaces to BASIC PLUS 2			111	A. Toth

B. Strategy

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OOD/Gordon Bell
Last Edit:1/10/79 - Wed Latest edit: 8/13/79 Mon

GB0001/17

BASIC PRODUCT STRATEGY UPDATED SUMMER 1979

Provide a set of homogeneous distributed computing system products so a user can interface, store information and compute, without re-programming or extra work in many styles and the following computer system sizes:

- as a single user computer within a terminal;
- at a small, local shared computer system; or
- via a large central computer or network.

Achieve a single VAX, distributed computing architecture by 1985 (as measured by revenue)through:

- focusing on homogeneous distributed computing with varying computing styles including high availability and ease (economy) of use as the DEC advantage;
- building new 11 hardware to fill the product space below VAX;
- having a new better, physical bus structure and transition plan to replace Q and U busses.
- building new 11 software products that also run on VAX; and
- developing software for 11-VAX migration and 11 base protection.

Provide essential standard IBM and help set international network interfaces.

Define, and make clear statements internally and to our users about programming for DEC compatibility. Tighten DEC user interface standards for editors, forms management, application terminals, command languages, DEC dialects of languages like BASIC, applications languages.

Provide general applications-level products that run on 8, 10/20 and 11/VAX-11 above the language-level to minimize user costs, including:

- word processing, electronic mail, and profession-based CRT-oriented calculators;
- transaction processing and data base query;
- general libraries, such as PERT, simulation, etc. aimed at many professions that cross many institutions (industry, government, education, home); and
- general management libraries for various sized business.

Provide specific profession (e.g. electrical engineering, actuarial statistician) and industry (e.g. drug distributor, heavy manufacturer) products as needed via the product line groups.

Provide cost-effective 8, 10/20 systems through:

- building hardware that runs current operating systems; and
- making market support and DEC-standard language enhancements.

This strategy is intended to cover the full range of DEC's future products. Since technology shifts rapidly and market opportunities emerge that we don't now understand, it may be necessary to provide non-compatible, point products. These should be proposed and reviewed accordingly.

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Essence and Rationale of the Strategy

The essence of the strategy is simplicity through adopting a single architecture. This simplicity is needed so that we can build the network and distributed processing structures which our customers are now demanding. The strategy is an evolutionary result of the 1975 choice to extend the 11 architecture and cover its customer base.

Given that the architecture and early customer acceptance are in place, the strategy moves to build our subsequent products on VAX, while continuing to sell 8's, 10/20's and 11's. Focus is imperative in order to avoid the redundant development efforts across base hardware and software, and to move development to fully distributed computing and to applications. The strategy also minimizes manufacturing and field start-up costs and takes advantage of the learning effect by moving to a single architecture.

The motivations for the homogeneous architecture are numerous and include the customer desires for a range of products on which to build products (in the case of OEMs) and applications (in the case of end users). Such a range in size and over time, allows planning and investment of software and it permits computers to be associated with various organizational units (eg. central group, small group, office, the person, or the home) on an "as needed" basis. Although, superficially it appears to be possible to have numerous architectures that are segmented by size and by market, the user requirements to cross both size and applications boundaries are significant. In fact, given that IBM is segmenting its products both by size and application, the main strengtn of the strategy is to have a single architecture with which a user can be comfortable rather than bounded by a manufacturer segmentation.

The most compelling reason for basing the strategy on the single VAX architecture, besides the technical excellence of the product is the belief that we can not build the truly distributed computing system of the 80's with heterogenous architectures. It is possible to build distributed computing networks as we do today, but the homogeneous architecture approach insures that programs may be assigned to any node, where they will give the same results. There is no need for the organizational and computation overhead signified by different manuals, separate training, recompilation of programs, and translation of data among machines in the network.

This strategy is aimed at beating the competition using our existing highly tuned minicomputer hardware and software to support and grow our existing user base. It provides us with a unique offering in the marketplace of the '80's which is likely to be based on the defacto standard IBM 360/370 architecture and the ensuing defacto architectures coming from the semiconductor companies. Since VAX is fundamentally better than either of these architectures, we must make it the standard architecture via transition from the PDP-11, which has been the standard architecture of the 70's.

The strategy is aimed at high volume through multiple channels of distribution, versus a more stable, low growth through support of an existing multi-system, customer base.

BASIC STRATEGY DO NOT COPY
OOD/Gordon Bell B-3
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How Can We Win Against IBM?

IBM has or will have: both constant and a decreasing cost a 360/370 line new in the $100 K to $10 M price range with lots of plug compatible competitors, several operating systems to support, a large backlog; a newly announced 8100 for Distributed Processing around the mainframe; RPG-based System 32/34/38 for Distributed Processing and as a Mainframe for small organizations; the aging Systems 3 to 15 for Distributed Processing; the System 1 for the would-be minicomputer buyer; the possibly defunct 5100-series Personal Computers for the scientist, engineer, analyst and small business; and several inevitable products for computing in the terminal. All of these are incompatible, except for the fact that they speak some dialect of SNA. Products are relatively segmented to customer classes and different languages are used to enforce segmentation and hinder application mobility. Finally, they've sold via DPD and GSD, with Office Products no doubt looking on and waiting for typewriter-type entry for electronic mail and word processing.

The 8100 is a radical departure from IBM pricing as 0.5 Megabytes of primary memory and a 60 Megabyte disk are $ 29 K. Memories on all machines are similarly priced. We repriced as a result. The 8100 is exactly in the price range of the systems we sell and where we make most of our revenue. It is the second product in this price range within a year; the Series 1 minicomputer family patterned after the 11/04-11/34 was the first product. The 370 (via the 43xx series) is clearly either in or is coming into our space this go-around or next generation (1984). On the surface, the product is low priced, with lots of capability, but it also has a new communications structure (versus the one we have used substantially unchanged since 1961). This structure permits easy peripheral and terminal interfacing for both the office and factory environment. There is an extensive range of peripherals, terminals and communications to the 360/370. Since the product is sold by DPD, the strategy seems to keep account control and to make the money on software and the numerous locked-in, generally overpriced hard to emulate terminals.

SNA seems finally under control and we must be concerned because it has future built-in capability (e.g. word processing, typesetting, packetized voice). Their strategy seems to be to slowly unfold it, make it the standard, pay no attention to other standards and to make everyone follow their gyrations. A strategy based on being tightly coupled to them (e.g. with terminal emulation or fully compatible across the board) is really risky. We must interface to them "carefully" and be very, very aggressive in our own interconnect plans (both in performance and capabilities). We must collaborate with ATT and the international standards community to set standards.

We must watch how the System 38 is used vis a vis its 48-bit address because it can lock us out and cause others to generate many dead end architectures. It may be a E/H series follow-on breadboard. We can't succumb to this.

Terminals have to play a major part because we can get the cost and volume to lower our system costs. We have to follow the strategy and push co-existence with our earlier systems, but homogeneous networks must be understood and pushed. VAX has to be kept tight with emphasis on performance to avoid the O/S proliferation of IBM (and 11's). Also, the tightness represents the performance/cost edge we have over the 370.

How Can We Win Against Other Competition?

There are established competitors too, such as DG, HP and Prime. DG and Prime have very simple, single architectures and have been most profitable and have grown most rapidly. HP is converging on a single architecture around the 3000, but it will have to be extended eventually. The NOVA will also be extended. The large manufacturers (Univac, Honeywell and Burroughs) which operate with an established base are less profitable, have grown slowly and have multiple, poor architectures. Honeywell, with a simple, but adequate minicomputer architecture seems to be doing well by selling minis to its old line, mainframe base. There is no evidence that they're developing or pursuing the mainframe business actively.

There are probably more significant threats from the companies that can be easily founded to build systems into OEM Winchester disks by using the newly announced zero-processor-cost, 16-bit microprocessors which have 22-bit address spaces and 11/34-11/45 performance. These architectures need to be extended for multiprogramming and to handle larger virtual memories, but many point products, such as RSTS, can be built easily and cheaply and can quite possibly target a specific existing, trained user base.

There are also the Japanese and TI which can be lumped together because of their similar behavior. Both believe in targeted, high-volume products with forward pricing. Neither have an adequate architecture. TI is strictly limited to 16-bits with almost no escape the Japanese are aimed at the 360/370 using U.S. companies (e.g. Service Bureaus) to distribute hardware, and at high volume point products that will go into stores, no doubt.

The strategy supports very high volumes for dumb, pre-programmed (smart) and programmable (intelligent) terminals using the 11 until VAX is appropriate in terms of price and functionality. In the mid and high priced minis, the strategy is compatibility and volume, phasing as appropriate from 11 to VAX. For example, since there is not a high priced 11 after the 11/74 and the 11/44, there is a phasing to VAX (through COMET) and lower priced 11's based on 11 microprocessor implementation. The question here will be how fast we can provide high performance microprocessors using HMOS and narrower line VLSI technologies.

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PRODUCTS IN 1981-82

HARDWARE COOMPONENTS

HMOS LSI, with first "test" product

Interconnection hierarchy with software compatibility
- 1-10 Mhz and/or 10-100 Mhz inter-computer bus ICCS;
- 50+ Khz comm.-compatible multidrop for terminals, peripherals, and small systems;
- 0.3-19.2 Khz comm.-compatible for low cost terminals.

Significant competitive memories
- Solid state modules for software
- Low end floppies and low cost tape
- Removeable and low cost disk RL04
- Hi-volume mid- and hi-end disks in R80/R81 with backup

Terminals for everyone!
- Low cost (dumb) and block mode (VT162)
- Office environment for quality printing, electronic mail, and move to full-page text as quick as possible
- Professional using graphics (and/or color) with target application software
- Factory environment terminals and interface systems

HARDWARE SUBSYSTEMS

- Remoteable printers, job entry, concentrators, sensor-control
- Communications concentrator - Mercury
- Memory (Hierarchy) Management - HSC50 for high end
  for R80/R81, RL04, tape and disk cache

KERNEL SYSTEMS based on processor-disk-communications (see family tree figure)

780 replaced by Venus (const. price >3x performance)
- 780 - Memory Manager - Comm. Concentrator
- 780 - Multiprocessor
- 780 - RP/R80-81 + RL02-04
- 780 - RK/RL04

Comet - RP/R80-81 + RL
Hydra (Including Memory Manager - Comm. Concentrator)

Nebula - R80-81 + RL
Nebula - RL02/RL04 (higher cost, quick to market personal computer)

LSI VAX - RL04 - Graphics Terminal (personal computer)

11/70 with no hi end replacement
- 11/70 - multiprocessor
- 11/70 - RP/R80

11/44 replaced by HMOS LSI-11 with >256 Kbytes (J-11) and 11/70 performance
11/44 - RP/R80-81 + RL
11/44 - RL

11/24 - Unibus Fonz RL based on new backplane replaced by HMOS >256 Kbyte
11/23 - Q-Fonz RL
11/23 - Q-Fonz - RX (floppy)

PDT Fonz - RX (floppy)
PDT Fonz - TU58

Tiny chips,

SOFTWARE

Diminish the 11 software investment for mature products (RSTS, IAS, MUMPS) and provide only minor enhancements to recent 11 based products (TRAX, PDT Software) to extend the market life and limit the VAX transition risk. Orient new development on VAX and 20 toward IBM compatibility and explicitly invest in tools designed to permit easy customer movement between VAX and 20. DEC 20 development will be aimed at timesharing, high level tools and applications support. Shift the bulk of the PDP-11 software investment to VAX, tracking VAX hardware and aggressively moving to round out commercial capability.

Develop a single VMS operating system to span the product range if technically and operationally feasible; "low end" products will mask the VMS capability for the unsophisticated users or, if efficiency demands, new code compatible at all interfaces with compilers and utilities will be developed. VMS will offer full mainframe capabilities allowing concurrent batch transaction, processing, and time-sharing, along with limited real-time.

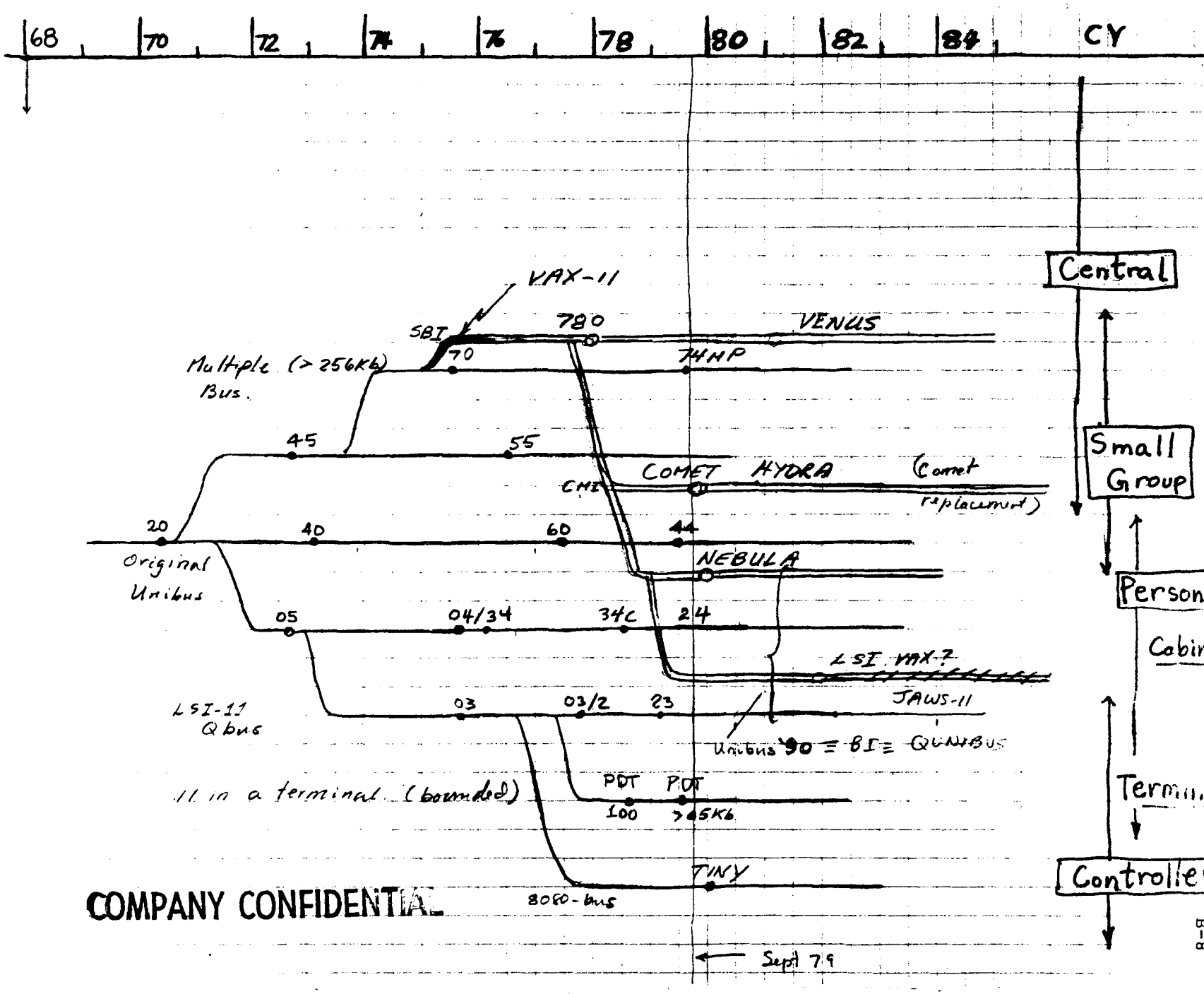
- Provide superior data-base capabilities in the two - three year time frame.
- Focus on data access and data manipulation tools for the non-programmer, heavily based on graphics terminals.
- Provide word processing and electronic mail as applications on the general purpose VAX systems.
- Data integrity will be a feature available independent of high-availability (non-stop) operation through Hydra.
- High-availability (Hydra) will be a standard attribute of VAX systems at the customer option.

. Fire-wall funds to stimulate acquisition of cross-industry applications packages. Provide industry specific applications via internal development or acquisition. Leverage field resources by investing heavily in product quality assurance and self installing systems capacity including remote software update and diagnostic strategies.

. Move systems-level code for 11 based software (RSTS, TRAX) to VAX compatibility mode if technically or strategically viable (under investigation now) otherwise provide user-level compatibility via native mode VMS layered products.

. Shift DECNET strategy to international standards and stronger IBM interconnect and VAX binary image compatibility for distributed processing; constrain PDP-11 DECNET FUNCTIONALITY EXTENSIONS; speed up DEC 20 DECNET capabilities.

. Converge on ease of DEC 20 to VAX movement through common language definitions, (common implementations where feasible), common user-level utilities and data conversion routines. For each new DEC 20 or VAX customer, as time progresses, make the movement between systems more attractive.



COMPANY CONFIDENTIAL

CENTRAL SOFTWARE ENGINEERING RED BOOK

July 6, 1979

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TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

I. INTRODUCTION

A. Product and Functional Scope

The products covered by this Red Book include all PDP-11 and VAX software, communications hardware, and the HYDRA program. Also included are advanced development, tools, administration, and Product Management. Specifically excluded are all hardware not described above, diagnostics software, PDP-8 software, 36 bit software, and all Product Line funded software.

B. Basic Product Strategy

The basic product strategy (derived from the new corporate strategy) is to aggressively invest to achieve a significant industry-wide position in distributed computing. Our engineering efforts will be concentrated on two fronts: (a) developing hardware and software architecture built on the VAX technology; (b) broadening DEC's product capability for interconnection with IBM's SNA, ATT's ACS, and the major public value-added networks. On non-32-bit architectures, engineering efforts will be restricted to the very low-end products (for example, components and terminals), and to the product modifications and new products necessary to hold our existing customer base while we migrate the bulk of that base to 32-bit architecture by 1985.

II. DEVELOPMENT STRATEGY

A. Statement of Strategy

The key statements of the Central Software Strategy are as follows:

1. Aggressively support the new corporate strategy. This translates into the following elements:

   a. Shift the emphasis of the middle and high end PDP-11 software investment into the 32-bit domain.

   b. Focus our new development efforts primarily on the 32-bit architecture.

   c. Achieve 32-bit software homogeneity via single implementations of file structures, languages, applications, communications, utilities, documentation, etc.

d. Reduce the investment in mature 16- and 36-bit software (e.g. RSTS, RSX-11D/IAS, RT-11, RSX-11M, and TOPS-10). Complete the functionality of the more recent new product efforts (e.g. TRAX-16, TOPS-20, and RSX-11M-PLUS). Maintain the 16- and 36-bit market base by investing in the outer layers of the product set (particularly languages, ease of use, tools, etc.).

2. Provide the industry's broadest range of compatible products. More specifically:

   a. Provide single 32-bit implementations of all software products.

   b. Strive for compatibility across 16-, 32-, and 36-bit architectures as a key goal on all new product efforts.

   c. For existing 16- and 36-bit products, develop aids, tools, and documentation to ease movement to 32-bit architecture.

3. Establish a significant industry position in distributed processing. More specifically:

   a. Complete existing communication efforts on middle to high-end 16- and 36-bit systems. Minimal enhancements thereafter.

   b. Aggressively develop Digital Network Architecture (DNA) on 32-bit and 11-based terminal products.

   c. Launch a major thrust in the development of foreign interconnects, in particular IBM's BSC and SNA protocols; AT&T's ACS, and the major public networks (Telenet, Datapac, Transpac, and Euronet).

4. Be the industry leader in ease of use. More specifically:

   a. Provide a single user interface on new layered product implementations.

   b. Develop non-procedural programming tools for external and in-house usage.

c. Develop products for minimal installation effort and enhanced serviceability.

d. Develop more vertically targeted and tailored products (e.g. TRAX, MINC, SCS/RSTS etc.).

e. Expend aggressive efforts on human factors - in particular on command languages, query language interfaces, error messages, utilities and documentation.

5. Develop and introduce industry competitive high-availability/reliable systems: More specifically:

a. Complete the 16-bit effort and introduce RSX-11M-PLUS on the 11/74 multi-processing configurations.

b. Complete high availability work on 36-bit equipment.

c. Develop a leadership product on 32-bit architecture via the HYDRA program.

6. Maintain an aggressive technology thrust via selected advanced development efforts.

B. Constraints

The key constraint is budgetary. The FY80 software allocation does not support achievement of leadership positions in all stated goal areas. As a result, some measure of risk in the 16-bit arena is being assumed in order to allow for the strategic allocation of monies to the 32-bit area. In addition, Product Lines will continue to carry the burden of funding applications level products and tools. Finally, the Software Advanced Development program will be less aggressive than desired.

C. Rationale

1. Market.

The market drive on Digital's software strategy is highly influenced by a combination of the following key technical and economic forces:

a. semiconductor price/performance improvements

b. increasing software complexity

c. demand elasticity

d. increased customer economic sophistication

These forces result in the market driving for greater functionality and less cost, higher performance, greater reliability and availability, and the design tools required to make computing systems available to non-computer oriented personnel.

2. Competition

The competitors are numerous. From a long range point of view, however, Digital's market position, size, and corporate strengths provide us with an enviable standing against most of them. The threatening competitors, in the long run, are IBM and the micro vendors (the semiconductor houses and the Japanese). Digital has traditionally enjoyed a position of competitive software superiority in our chosen market space. Continued superiority depends on these key activities:

a. Emphasizing a superior hardware and software computer architecture (VAX).

b. Maintaining and enhancing the breadth and compatibility of the over-all set of product offerings.

c. Achieving a significant industry-wide position in distributed processing via a combination of a "we are different and better" approach (utilizing unique Digital distributed processing architecture) with the ability to simultaneously co-exist with IBM, ATT, and the domestic and foreign public value added networks.

d. Developing competitive information management capabilities.

e. Developing easier to use products for non-computer personnel.

3. Technology

The dramatic performance/price improvements due to semiconductor technology need no elaboration. This is the prime motivator to move aggressively toward the wide word, large addressing architecture. In the software domain, however, an inverse relationship is occurring. Software costs are rising faster than programmer productivity. Also, due to increased customer demands for greater function, software complexity and lead times are increasing. Because preservation of our own and our customers' software investment is critical to the maintenance of customer base loyalty, compatibility takes on increasing importance. Given a major move from 16- to 32-bit architectures, the balance between (a) protecting (and leveraging) the marketplace's estimated $5B investment in PDP-11 software and (b) moving to a technologically superior architecture as quickly as possible, must be carefully orchestrated. The quickest and least risky method of moving a large customer base from one architecture to another, without opening the door to competition, is via compatible 16/32-bit product offerings plus an aggressive program to build the marketplace's inventory of VAX software.

4. Digital Strengths

From a strictly software point of view, inherent Digital strengths lie in the breadth of the product offering, our on-line orientation, the potential of the VAX architecture, and the relatively large and loyal customer base. The latter strength necessitates placing a high priority on protection of our existing 16- and 36-bit base. The others suggest an aggressive distributed processing thrust based on VAX. As previously discussed, the balance during the transition is critical.

D. Changes From Last Year

The current strategy incorporates three basic changes to the Software Engineering strategy of Spring, 1978.

1. A much more aggressive shift to implementing 32-bit systems functionality.

2. The emphasis on incorporation of terminals, IBM, ATT/ACS and other foreign interconnects into the distributed processing strategy.

3. The movement of small business system software (SCS-11) from implementation on an RSX-11M base to a RSTS base.

III. PRODUCT AND PROGRAM DEVELOPMENT TACTICS

The major programs of Software Engineering and associated FY80 budgets are depicted in Figure 1. Each program is graphically depicted in three dimensions. First is the level of budget required to simply survive in the marketplace (maintenance and meeting our existing commitments only). Secondly, is the level of investment required to maintain current competitive positioning. Thirdly, (the area in white) is the recommended level of activity required to improve our competitive position. The broad line is the FY80 budget level allocated for each program.

Appendix I contains the back-up information on each program. This includes a short program/product definition, the key Product Line beneficiaries and target markets, the FY80 tactical strategy for the program, and the FY80 dollars for each of the program's key components. FY81 and FY82 dollar requirements are also included, where they were available.

Appendix II contains the target dates for availability of key components of the major programs.

IV. BUDGETS

A. Assumptions

1. The Central Software strategy assumes that all new processors within the respective 16- and 32-bit architectures will be software compatible and run existing software without change.

2. It is assumed that all hardware development (CPUs, disks, terminals, etc.) requiring software changes have been negotiated and agreed to. Any changes induced after 4/13/79 will require funding from the organization inducing the change. In particular, the mass storage budget was increased by $2M+ and a new interconnect strategy has been proposed. Software Engineering does not have resources budgeted for either of these activities in FY80.

V. FY80 BUDGET ANALYSIS

A. Budget by Size

The expenditure of FY79 and FY80 dollars categorized by size is depicted in Figure 2.

B. Budget by Activity

The FY79 and FY80 budget represented by the activities of maintenance, development, advanced development, and "other" is shown in Figure 3.

C. Budget by Architecture

Figure 4 depicts the FY79 and FY80 expenditures by architecture.

D. Budget by Product Area

The budget by product area (languages, communication, database and applications, and executive interface software) is depicted in Figure 5.

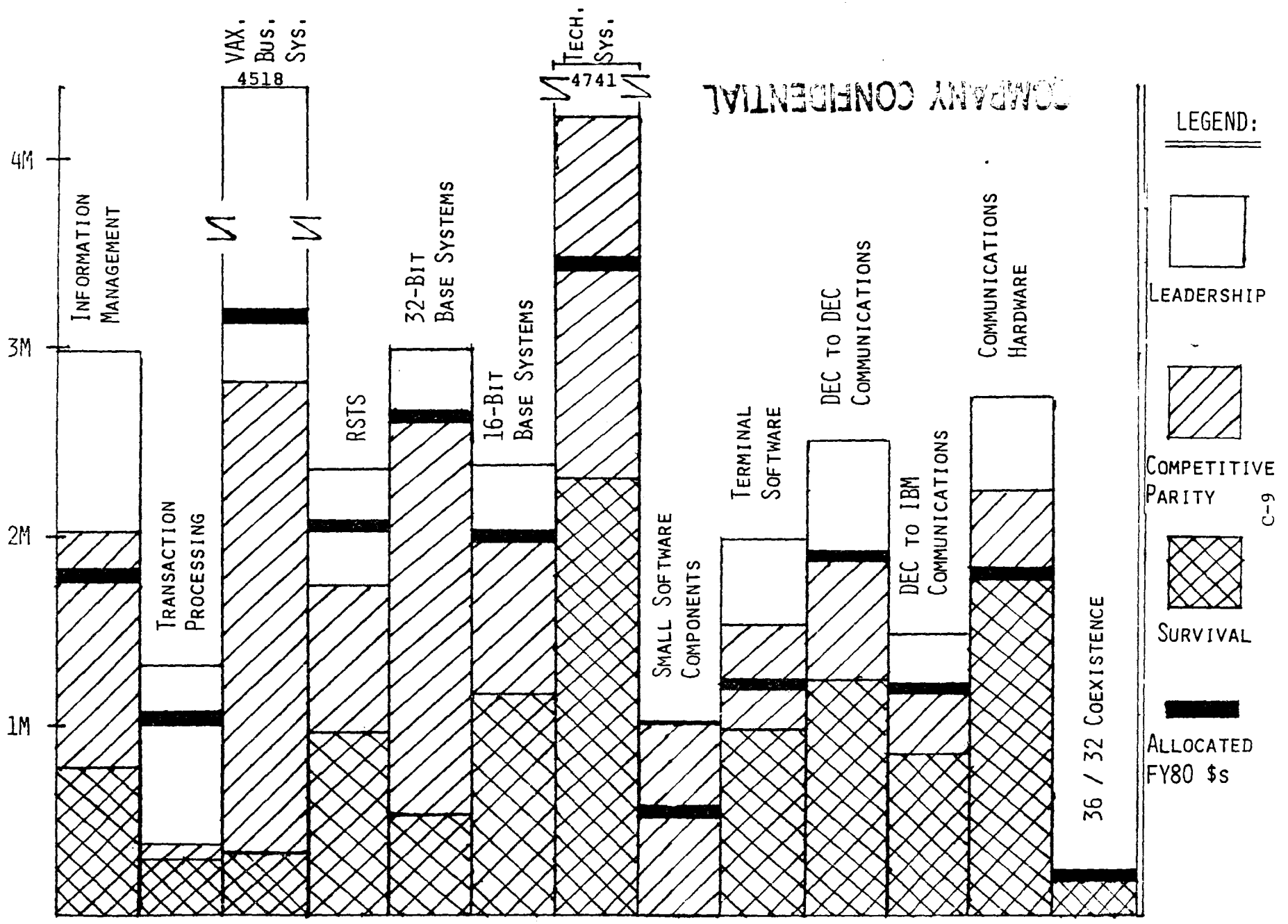
Note: The Software Engineering rollup (exclusive of HYDRA) of 27,315K is 399K over the official OOD budget of 26,916K. It is our intention to enter FY80 with a 399K over spend plan and manage it to within the official budget based on the actuals incurred.

VI. KEY PRODUCT OPPORTUNITIES NOT FUNDED

The following high priority elements of key programs have not been funded (or are underfunded) under the FY80 allocation:

- Communications Hardware and Software, especially for non-DECnet connectivity and distributed application (e.g. electronic mail).
- Information management (Database software, related query languages, etc.).
- Competitive Leadership in 16-bit area.
- Aggressive intelligent terminal and very small system software.
- Applications.

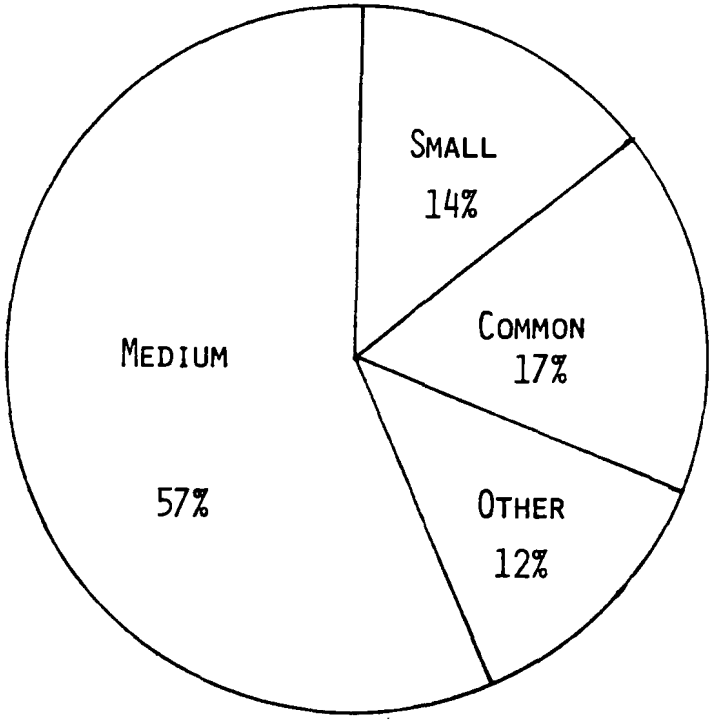
See Appendix III. for the more detailed "Get/Don't Get" List.



MAJOR PROGRAMS

FIGURE 1

FIGURE 2 (BUDGET BY SIZE) *



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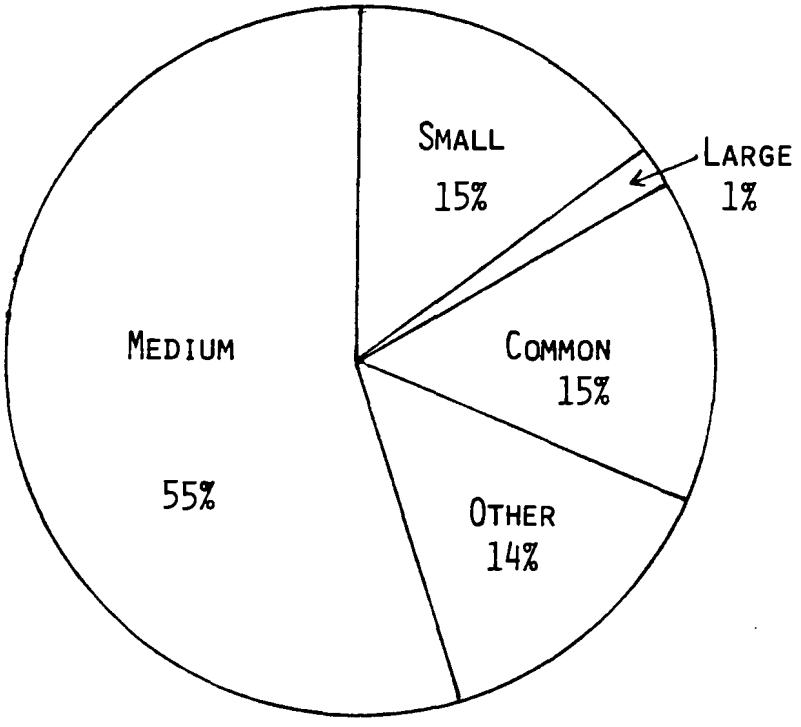
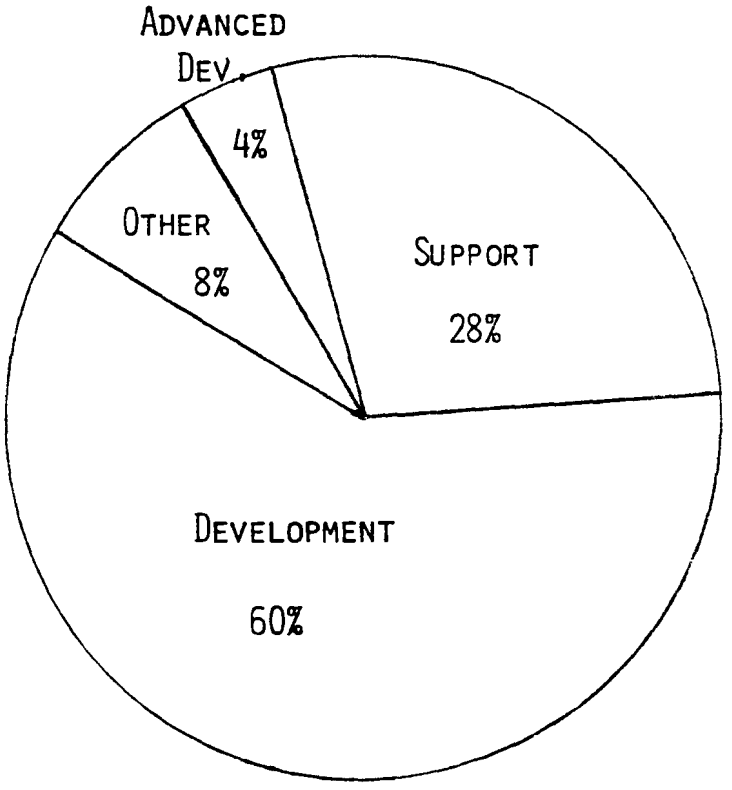


FY80 (27315)

* EXCLUDES HYDRA

FIGURE 3 (BUDGET BY ACTIVITY) *



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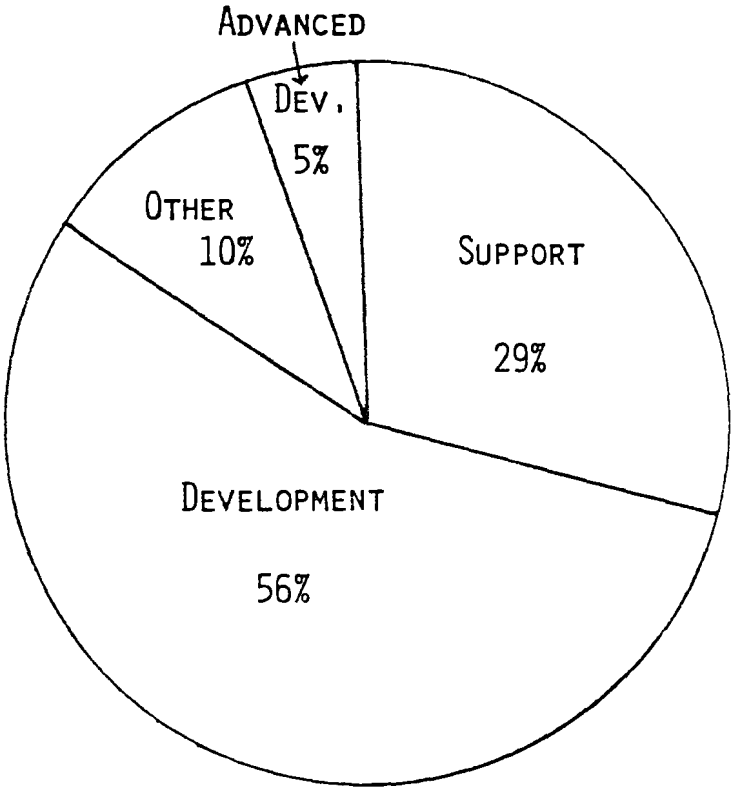
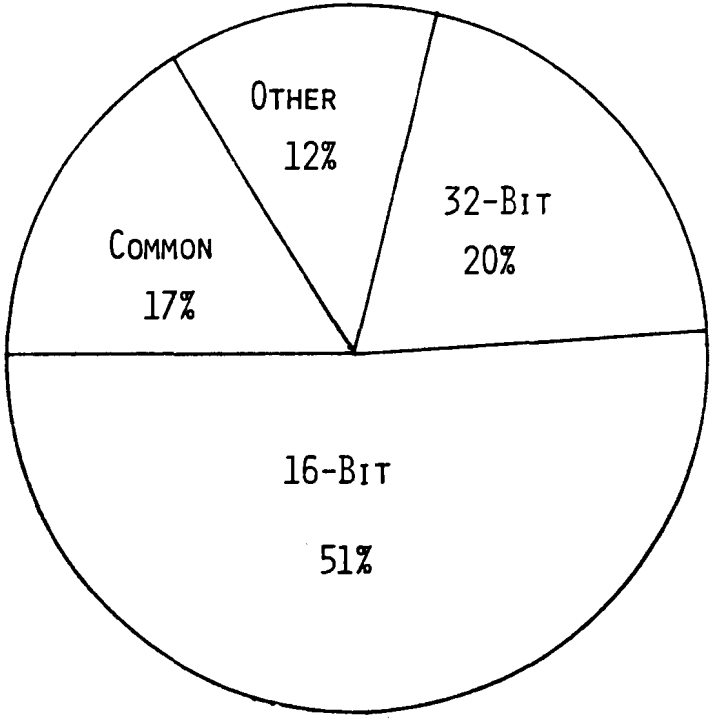


FY80 (27315)

* EXCLUDES HYDRA

FIGURE 4 (BUDGET BY ARCHITECTURE) *



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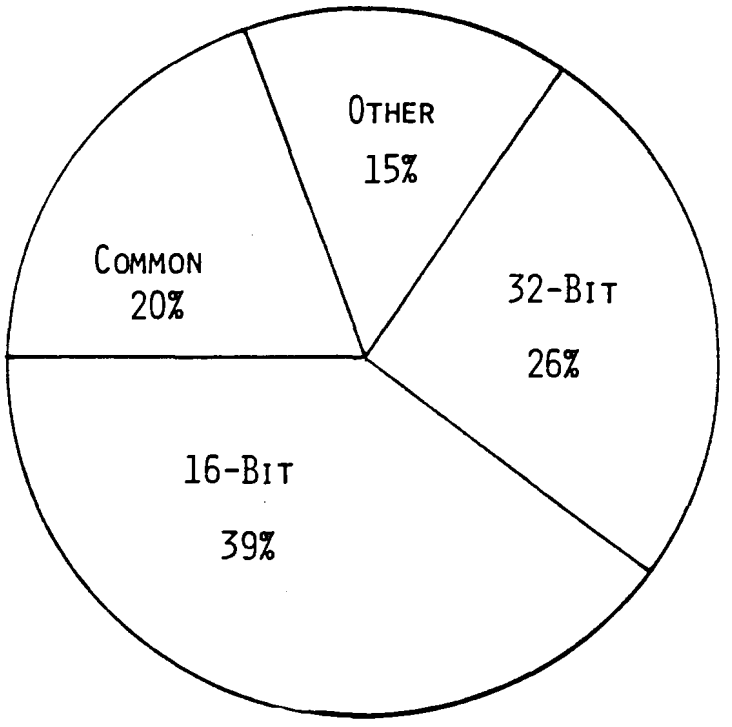
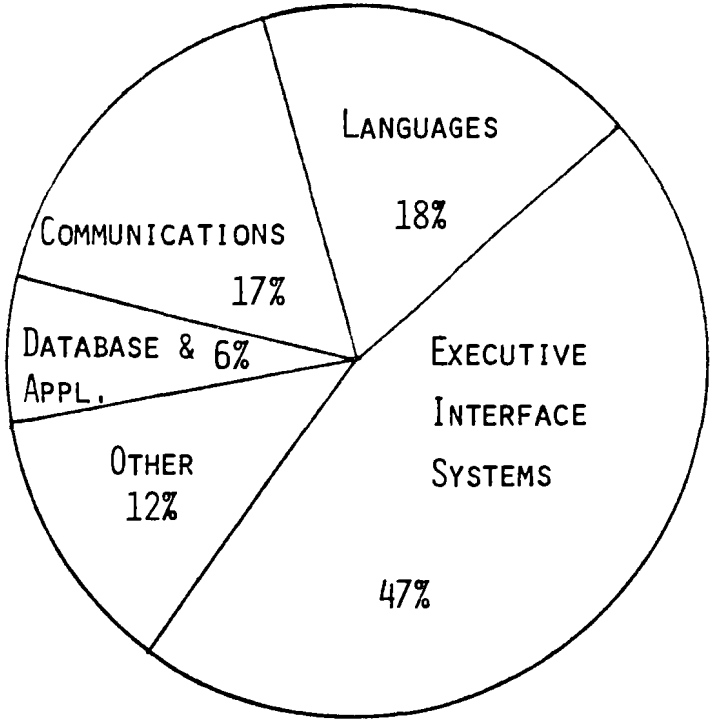


FY80 (27315)

* EXCLUDES HYDRA

FIGURE 5 (BUDGET BY PRODUCT AREA) *



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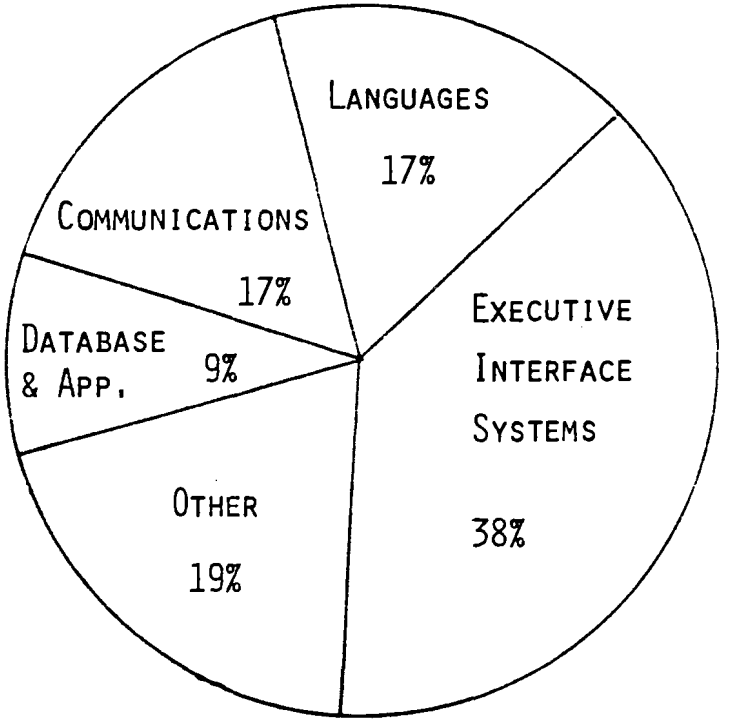


FY80 (27315)

* EXCLUDES HYDRA

APPENDIX I

PROGRAM DESCRIPTIONS

COMMERCIAL LANGUAGES

DEFINITION

COBOL, BASIC-PLUS, and BASIC-PLUS-2.

MARKETS/PRODUCT LINES

All Commercial Group Product Lines

All Technical Group Product Lines

FY80 TACTICS

COBOL

- Do COBOL-79 as VAX high-end product replacing COBOL-74.
- Small COBOL fills low-end on RSTS and RT-11.
- COBOL-11 mid-range product eventually replaced by COMET/NEBULA.
- Increased IBM compatibility through translation utilities and added compiler functionality.

BASIC

- Provide the "interactivity" of BASIC-PLUS on BASIC PLUS-2.
- Begin rewrite of BASIC PLUS-2 in BLISS for performance, maintainability, better interactivity, and extensibility.
- Plan for ROM BASIC PLUS-2 subset for low-end after FY80.
- Insure small BASICs are subsets of larger BASICs.
- Build validation library to enforce compatibility.
- High-end will be VAX high-volume BASIC PLUS-2 (150+ user system).

BUDGET

Included in programs for VAX business system enhancements and RSTS.

INFORMATION MANAGEMENT

DESCRIPTION

A set of products that collectively provide basic and advanced facilities for management of data and access to it. Included are RMS file system, DATATRIEVE data inquiry and report generation system, DBMS Codasyl Data Base Management System, and DDMF for distributed relational facilities.

MARKETS/PRODUCT LINES

All Commercial Group Product Lines

All Technical Group Product Lines

FY80 TACTICS

- Use RMS as the basis for all data management products.
- Continue to enhance RMS as the mainline, basic file system; add extended capabilities to support layered products.
- Do DATATRIEVE-32 with program level access for native mode languages to enhance the competitive image of our data management products.
- Initiate DDMF (Distributed Data Management Facility) as a response to S/38 and entry into the distributed relational area. Initially includes a DATATRIEVE-32 remote access facility via DECnet and a Data Dictionary/Directory facility.
- Continue development of DBMS-32 and maintenance of DBMS-11, providing access to DBMS-11 data through DATATRIEVE-11.

SURVIVAL

	FY80	FY81	FY82
DBMS-32 MAINTENANCE	---	---	77
RMS-32 SUPPORT	130	140	154
DATATRIEVE-32 MAINTENANCE	---	70	77
DDMF-32 MAINTENANCE	---	70	77
DBMS-11 MAINTENANCE	66	70	77
RMS-11 SUPPORT	585	210	154
DATATRIEVE-11 MAINTENANCE	33	70	77
	814	630	693

COMPETITIVE PARITY

	FY80	FY81	FY82
DATATRIEVE	215	280	308
DDMF-32	116	210	231
RMS-32 ENHANCEMENTS	215	---	---
DBMS-32	429	851	374
* RMS-32 HASHED 7 CHAINED	99	53	---
* RMS FILE DESIGN MANUAL	33	---	---
* IBM TAPE CONVERSION	99	33	---
	975	1427	913

LEADERSHIP

	FY80	FY81	FY82
* DIST. DATA MGMT. SERV.	330	490	539
* VAX BACK-END DBMS	132	132	---
* RMS-11 REMOTE ACCESS	190	53	---
* IBM REMOTE FILE ACCESS	173	280	---
* DATATRIEVE DATA ENTRY	83	70	---
	0	1025	539
	1789	3082	2145

* NOT FUNDED IN FY80 AND NOT INCLUDED IN ROLL UP

TRANSACTION PROCESSING

DEFINITION

Facility to address dedicated, high volume, business-oriented online transaction processing in a fashion which takes maximum advantage of system performance (within the constraints of a layered product) and which directly addresses data integrity, availability, programmer and user productivity specifically for this application class.

MARKET/PRODUCT LINES

All Commercial Group Product Lines

FY80 TACTICS

- o V1.1 in shortest possible timeframe to alleviate node-pool restrictions and solve the "system hang" problem.
- o V2.0 to round-out key TRAX features such as full DECnet, 2780/3780, greater number of terminals.
- o Initiate development of TRAX-32, assuring proper design hooks in base VMS for TRAX-32 to be a pure layered product on VAX.

SURVIVAL

	FY80	FY81	FY82
TRAX-16 MAINTENANCE	264	280	308
	264	280	308
COMPETITIIVE PARITY			
TRAX V1.1	66	---	---
	66	0	0
LEADERSHIP			
TRAX V2.0	528	667	492
TRAX-32	182	730	1120
* FOREIGN TERMINAL SUPPORT	297	---	---
	710	1397	1612
	1040	1677	1920

* NOT FUNDED IN FY80 AND NOT INCLUDED IN ROLL UP

VAX BUSINESS SYSTEMS ENHANCEMENTS

DEFINITION

Total, effective, top to bottom family of commercial systems eventually from single user LSI/VAX to Venus with a range as homogeneous as possible ($5K to $250K). Initially targeted as follow-on and upgrade path for RSTS and then as vehicle for mainline commercial thrust for:

- Information Management
- Productivity
- Ease of Use
- Distributed Processing
- Transaction Processing
- Applications (Generic and Industry)
- High Availability
- Office Automation
- Standard Commercial Languages

MARKETS/PRODUCT LINES

"Mini-mainframe" for mid-size companies

Distributed processing vehicle for larger companies

All Product Lines having commercial processing requirements.

FY80 TACTICS

- Build layered products such as COBOL, BASIC-PLUS-2, SORT, DATATRIEVE, RMS as commercial functionality enhancements to the base VMS product set.
- Add a Commercial Application Terminal Management System (CATS) to address forms, block mode, multidrop, screen orientation, and other commercial terminal features.
- Focus on conversion programs, emulation facilities, and documentation to provide the user with adequate tools to insure smooth migration from, or co-existence with, RSTS systems.
- Plan for an aggressive internal testing/field test program to insure a smooth introduction of the transition to VAX in the commercial market.

VAX BUSINESS SYSTEM ENHANCEMENTS (Continued)

SURVIVAL

	FY80	FY81	FY82
COBOL MAINTENANCE	66	140	154
BASIC MAINTENANCE	50	140	154
SORT/EDT MAINTENANCE	66	70	77
OTS MAINTENANCE	99	140	154
CATS MAINTENANCE	---	140	308
	281	630	847

RSTS REPLACEMENT (SURVIVAL - Continued)

BASIC-PLUS AME & DOC.	114	68	71
BASIC-PLUS-2 V1.7	429	408	391
CATS - INCLUDING VT162	462	490	308
SYSTEM INTEG. (TESTING & DOC.)	248	314	403
OBJECT TIME SYSTEM	462	665	827
BATCH STREAM CONV. PGM.	129	---	---
* KMC 2780/3780 & 3271	99	---	---
	1844	1945	2000
	2125	2575	2847

* NOT FUNDED IN FY80 AND NOT INCLUDED IN ROLLUP

VAX BUSINESS SYSTEM ENHANCEMENTS (Continued)

COMPETITIVE PARITY

	FY80	FY81	FY82
SORT-MERGE	99	140	154
EDITOR	33	---	---
* SNA AND IBM VIRTUAL TERMINALS	400	440	500
* NETWORK MANAGEMENT TOOLS	66	210	385
	132	790	1039

LEADERSHIP

COBOL-79	743	740	693
VAX DEBUGGER	132	66	66
* IBM COBOL CONVERTER	161	44	---
* FIPS FLAGGER	99	26	---
* COBAID	132	---	---
* GENERALIZED MENU INTERFACE	165	89	---
* PROGRAM DEV. ENVIRONMENT	198	107	---
* COBOL/BASIC SPE (INCREMENTAL)	66	---	---
* RPG-III	---	463	500
* BASIC +2 V.2	---	420	462
	875	1955	1721
	3132	5320	5607

* NOT FUNDED IN FY80 AND NOT INCLUDED IN ROLLUP

DEFINITION

The current mainline, general purpose product for middle to high-end commercial minicomputer business, supporting multi-language timesharing and general purpose computing.

MARKETS/PRODUCT LINES

All Commercial Group Product Lines

EPG, GIS

FY80 TACTICS

- Support current releases of COBOL, RMS, SORT, BASIC-PLUS-2, DECnet and KMC 2780/3780 and 3271.
- Plan a maintenance release for support of 11/24 after V7.0.
- Release FMS-11, DATATRIEVE V2.0, and FORTRAN IV-PLUS as key FY80 enhancements to the RSTS system.
- Replan the SCS strategy for implementation on a RSTS base, in a program tentatively labeled SCS/RSTS, by reducing the minimum system configuration, making it easier to use, and selectively adding layered products - including Small COBOL and ADE.

SURVIVAL

	FY80	FY81	FY82
COBOL-11 MAINTENANCE	281	245	154
SMALL COBOL MAINTENANCE	66	140	154
BASIC MAINTENANCE	330	175	77
ADE MAINTENANCE	50	70	77
SORT/EDITOR-11 MAINTENANCE	33	35	20
RSTS MAINTENANCE	198	210	154
	958	875	636

COMPETITIVE PARITY			
SMALL BUS. SYS. ENHANCEMENTS	479	340	246
* RSTS V7.1	297	---	---
	479	340	246
LEADERSHIP			
ADE	280	124	33
SMALL COBOL	330	268	272
	610	392	305
	2047	1607	1187

* NOT FUNDED IN FY80 AND NOT INCLUDED IN ROLLUP

32-BIT BASE SYSTEMS

DEFINITION

This program includes the definition, design, implementation, documentation, release, and product support of the VMS Base System.

The strategy of the 32-bit Base Systems Program is to provide a high quality general-purpose 32-bit software product that will provide a foundation for layered products. The system design goal is a high performance, open-ended, competitive architecture with emphasis on reliability and high availability.

MARKET/PRODUCT LINES

The 32-bit Base System will provide the software foundation to be the primary revenue generator in the 1980's for the Technical, Commercial, and Computer Product Groups Markets.

FY80 TACTICS

The tactical plans for FY80 include maintaining VMS V1.0 and V1.5, development of V2.0, and planning features beyond V2.0. The VMS V2.0 plans include support of the COMET hardware, other VAX-11/780 hardware extensions, new devices, and RMS-32 and ACP enhancements.

SURVIVAL

	FY80	FY81	FY82
VMS SUPPORT	585	---	---
	585	702	843

COMPETITIVE PARITY

	FY80	FY81	FY82
VMS-COMET, NEBULA New devices, DECnet/VAX, Files - chained access etc., Exec. enhancements	1767	---	---
VMS-PERFORMANCE EVALUATION	590		
Native mode utilities	*(325)		
WCS Tools, Disk Quotas, Directory Wildcarding VMS Fast Backup/Restore Utility			
	2032	2438	2925
	====	====	====
	2617	3140	3768

* NOT FUNDED IN FY80 AND NOT INCLUDED IN ROLLUP

16-BIT BASE SYSTEMS

DEFINITION

This program includes the definition, design, implementation, documentation, release, and product support of the K2 16-Bit Base System. K2 is the base system for TRAX, and RSX-11M+.

The strategy of the 16-Bit Base Systems Program is to provide high quality general-purpose 16-Bit Software Products, provide foundations for layered systems in both the Traditional and Commercial Markets.

FY80 TACTICS

The tactical plans for FY80 include the maintenance and support of the K2 base system. Development plans include new device drivers, fast backup/restore for RSX systems, maintenance for TRAX and 11M+ base levels and TRAX/M+ base level convergence.

SURVIVAL

	FY80	FY81	FY82
DRIVER SUPPORT	195	---	---
FILES & UTILITIES SUPPORT	455	---	---
K2 SUPPORT	520	---	---
	1170	1584	1900

COMPETITIVE PARITY

	FY80	FY81	FY82
NEW DRIVERS	400	---	---
FAST BACKUP/RESTORE UTILITY	195	---	---
K2/TRAX BASE LEVEL CONVERGENCE	65	---	---
* ODS II M/M+	260	---	---
* K2 EXTENSIBLE COMMAND LANG., UNIBUS I/O LEVELING, etc.	130	---	---
	660	792	950
	1980	2376	2850

* NOT FUNDED IN FY80 AND NOT INCLUDED IN ROLLUP

TECHNICAL SYSTEMS

The strategy of the Technical Systems Program is to maintain general-purpose and RT/C leadership in the DEC traditional markets. These markets are strategically dependent upon 16-bit systems through FY81. Beginning in FY81, COMET 32-bit Systems will become more significant. These systems range from RT-11 at the low-end through RSX-11M, M+ and VMS at the high-end. Technical language development is a significant part of this strategy.

FY80 TACTICS

The tactical plans for FY80 include supporting 16-bit Technical Systems, (RT-11, RSX-11M, RSX-11M+, IAS, RSX-11S) and introduction of COMET based systems. Development of RT-11 V4.0 is planned as well as development on RSX-11M/M+. The RSX-11M/M+ development will be focused at new device drivers, maintenance, minor enhancements and ease of use. The major portion of the new development investment is aimed at providing new technical language capability for 32-bit VMS systems and improved technical language capability for 16-bit software systems.

SURVIVAL

	FY80	FY81	FY82
RSX-11M+ SUPPORT	130	---	---
IAS SUPPORT	385	*(150)	---
FORTRAN IV+/VAX SUPPORT	195	---	---
RSX-11M/S SUPPORT	520	---	---
FORTRAN IV+ SUPPORT	195	---	---
APL SUPPORT	65	---	---
RT-11 SUPPORT	390	---	---
BASIC-11 SUPPORT	195	---	---
FORTRAN-IV SUPPORT	195	---	---
	2120	2550	3060

*NOT FUNDED IN FY80 AND NOT INCLUDED IN ROLLUP

COMPETITIVE PARITY

	FY80	FY81	FY82
FORTRAN IV+/VAX ANSI-77	260	---	---
PASCAL PLUS	341	*(211)---	---
MP ENHANCEMENTS	245	---	---
FORTRAN IV+ ANSI-77	130	---	---
RT-11 V4.0	325	---	---
SMALL-M FOR FONZ/RT-11 ACP	260	---	---
* FORTRAN IV ANSI-77	195	---	---
* IMPROVED/NEW BASIC-11	195	---	---
	1350	1620	1944

LEADERSHIP

ADA	65	78	94
* EXPLOIT U-CODE	130	---	---
* APL/VAX **	195	---	---
* FORTRAN IV MAINFRAME	65	---	---
* PASCAL ON RSX SYSTEMS	195	---	---
* FORTRAN IV+/VAX EXTENSIONS	65	---	---
* TRAX/MP HOOKS	130	---	---
	65	78	94
	3535	3930	4716

* NOT FUNDED IN FY80 AND NOT INCLUDED IN ROLLUP

** APL/SF ON VMS FUNDED BY LSD IN MARLBORO

SMALL SOFTWARE COMPONENTS

DEFINITION

The purpose of the Small Software Components Program is to get competitive with the system level software offerings of the semiconductor houses.

MARKET/PRODUCT LINES

Primarily TOEM, LDP and CPG

FY80 TACTICS

The tactical plans for FY80 include providing competitive software for boards and boxes - namely: SSC/PASCAL (a set of application linkable Standard Software Components interfacing with a low-end systems implementation language). Also planned are: RT-11 support of SHOEBOX, preconfigured memory only systems, and support of the T-11 processor.

SURVIVAL

	FY80	FY81	FY82
	0	---	---
COMPETITIVE PARITY			
SSC/PASCAL	716	(196)* --	---
* TECHNICAL PERSONAL COMPUTER	179	---	---
* FIXED FUNCTION APPLICATIONS**	150	---	---
* SHOEBOX-RT**	130	---	---
* T-11**	65	---	---
	520	1488	1786
LEADERSHIP			
* LARGER MENU OF LANGUAGES and Application Tools	---	---	---
	0	1488	1786
	520	1488	1786

* NOT FUNDED IN FY80 AND NOT INCLUDED IN ROLL UP.

** PROBABLY WILL BE P.L. FUNDED.

TERMINAL SOFTWARE

The strategy of the Terminal Software Program is to keep Digital competitive in the terminal business. This includes intelligent and nonintelligent terminals. Ease of use and ease of installability are key to the success in this market.

MARKET/PRODUCT LINES

The Computer Products Group is a prime beneficiary of the terminal software program. Most other market groups will benefit either directly through the marketing of PDT's or indirectly through the marketing of systems with FMS-11 capability.

FY80 TACTICS

The tactical plans for FY80 include the migration of the FMS-11 product to other 16-bit operating systems, (RSTS, RSX-11M, RSX-11M+ and VMS), terminal architecture work (HY/SW/Firmware), and the development of second generation PDT software (FMS V2, RT-11 communications enhancements and commercial capabilities).

SURVIVAL

	FY80	FY81	FY82
PDT SUPPORT	260	---	---
TERMINAL ARCHITECTURE	260	---	---
FMS-11 EXTENSIONS	455	---	---
	975	1170	1404

COMPETITIVE PARITY

DISTRIBUTED INTELLIGENT TERMINAL	65	---	---
RT - EMULATORS	114	---	---
* BASIC - ROM	195	---	---
* MICRO - ISAM	195	---	---
	179	215	258

LEADERSHIP

* EXPLOIT LANGUAGES (PASCAL, FORTRAN)	390	---	---
	1154	1385	1662

* NOT FUNDED IN FY80 AND NOT INCLUDED IN ROLLUP

NETWORKS AND COMMUNICATIONS

OVERALL THREE YEAR STRATEGY

Provide hardware and software products that allow our customers to:

A. Build networks of Digital unique products with the ability to access transactions, files, databases, systems or terminals from any system or terminal in the network, independent of location.

   1. Maintain a single central network architecture (DNA) that includes both Digital and public network protocols, thus allowing transparent shift from one communications technology to another without application software change.

   2. Shift investment from general interconnect across the total DEC product space to focus on 32-bit architecture and the low-end of the 16-bit architecture. Confine the investment in middle to high-end 16- and 36-bit architectures to migration and compatibility features.

   3. Exploit microprocessor communications hardware technology to develop a family of intelligent interfaces which will allow increasingly greater layers of the networks protocols to be supported independent of the host computer system. Through this strategy we will be able to focus our investment on higher level user services.

B. Build networks of Digital and IBM systems with the ability to transport files, databases and transactions between any two systems in the network.

   1. Integrate IBM protocols into the central Digital architecture (DNA). Provide cost effective BSC interconnect to assure long term IBM connectability and to demonstrate long term commitment to this area.

   2. Assure compatibility between Digital and IBM files, databases and transaction messages.

   3. Migrate the major IBM protocols into an intelligent interface, making DEC to DEC and DEC to IBM connection compatible and user transparent.

C. Provide interconnect across major public network offerings and local private data networks.

D. Develop distributed applications (unfortunately, FY80 funding constraints prohibit an aggressive Central Engineering program here). PL funding is being sought to bring an Electronic Mail product to market.

DEC TO DEC COMMUNICATIONS

DEFINITION

A family of software products that allow Digital unique systems to exchange data in the form of records, files, status, programs, and to synchronize the scheduling of programs and resources in remote systems.

PRODUCT LINE/MARKETS

DECnet is a corporate product set, sold by most Product Lines.

FY80 TACTICS

The basic approach to the FY80 plans in DEC to DEC interconnection is best summarized by:

DECnet Phase III

Complete the network functionality of routing, multidrop, remote ("virtual") terminals, and autodial in the RSX-11M/ RSX-11M+, RSTS/E, TRAX, VMS, and TOPS 20 systems. Eventually, work towards optimizing homegeneous 32-bit VAX networks.

Low-End Communications

PDT's and very small systems require efficient network and communications capability. The present approach of DECnet is not acceptable for the long term because it is overkill. DECnet will be modified to achieve a minimum overhead implementation specifically tailored to meet the needs of the low-end product space.

Value Added Interconnect

A key element of the strategy is to provide transparent and compatible interconnection to the emerging value added communications capabilities such as support of Public Packet Networks and AT&T's ACS. Digital's Network Architecture (DNA) has been designed to allow a standard packet protocol, like X.25, to make virtual connections over the packet network look like physical connections.

X.25 protocols will be utilized to achieve computer to computer interconnection in DATAPAC using RSX-11M. Extensions to this product to include Transpac and Telenet support are currently underway and these will complete early in FY80.

Value Added Interconnect (Continued)

It will also be necessary to develop the X.29 terminal interface.

System Independent Communications

A FONZ-11 based intelligent communications controller, that will operate at speeds up to 56 kb, is under development. It will have sufficient resources to singularly support any required protocol (e.g., DNA, BSC, SNA, X.25).

Over the long term it will be necessary to develop a family of Intelligent Network Controllers that provide a cost effective solution for packaging multiple communications protocols in hardware, essentially allowing all of the networking and communications functionality to move outboard. This effort is currently in the advanced development and architecture stages and will result in a complete sub-system design within FY80.

Post Phase III

Following the Phase III effort, the strategy is to concentrate on very large topologies (1000+ nodes) and local networks requiring cost effective/ease of use capabilities. This will enable DEC to support the theme of a "computer for everyone". To accomplish this, effort will be directed toward improved routing and congestion control algorithms, efficient local network architecture, more effective file access capabilities, and significant emphasis on network management tools and support services.

DEC TO DEC COMMUNICATIONS (Continued)

SURVIVAL

	FY80	FY81	FY82
COMPLETE PHASE III ON M, M+, VMS (Routing, Multidrop, Terminals, Autodial)	602	---	---
EXTEND X2511M TO INCLUDE TELENET, EURONET	124	---	---
LOW-END DECnet (PDT)	124	68	---
MAINTENANCE	390	528	300
	1240	596	300

COMPETITIVE PARITY

	FY80	FY81	FY82
START PHASE IV DECnet ON PDT, M, VMS (X.25, X.29, Network Terminals, Network Management, NCC)	204	1088	---
ARCHITECTURE (Large Networks, Virtual Terminals, DNA/X.25, ACS, Local Networks)	186	204	225
ADVANCED DEVELOPMENT (Congestion Control, DNA/X.25, Virtual Terminals, NCC2)	248	528	300
	638	1820	525

LEADERSHIP

* LOCAL X25	62	136	---
* HDLC	124	136	---
	0	272	---
	===	===	===
	1878	2688	825

* NOT FUNDED IN FY80 BUDGET AND NOT INCLUDED IN ROLL UP

DEC TO IBM COMMUNICATIONS

DEFINITION

A set of software products that allow Digital to communicate with IBM systems at both file and transaction level through implementation of IBM's interconnect protocols (Bisync and SNA).

MARKET/PRODUCT LINES

The requirement to connect to IBM is needed by all major market sectors.

FY80 TACTICS

Starting in FY80, we will be shifting a significant percentage of our resources to IBM Interconnect. The IBM focus will be directed toward the following areas:

1. BISYNC

   We will be concentrating on consolidating the Bisync emulated products into the following categories:

   a. Software only protocol emulators for 2780/3780. A common design base will be used for all systems and will result in the most optimum short term approach to provide 2780/3780 capability across a broad range of DEC systems (PDT through VAX).

   b. IBM 3270 support. This will also concentrate on a common implementation (probably using the KMC11).

   c. Development of a PDP-11 ISP communications controller. We will pursue an approach, based on the use of FONZ-11 technology, to outbound all key BISYNC protocol emulators.

2. SNA

Since SNA is still evolving, and since it is critical that we be able to interface to it, we must have an approach that deals with both the present as well as the future direction that IBM will take. We plan the following three step approach:

A. Develop a 3790 emulator on RSX-11M.

B. Using the available microprocessor technology developed for the BSC emulators, migrate SDLC (and other appropriate layers) to the new Network Communications Controller (NCC).

C. Do the architecture and advanced development work necessary to track and understand IBM SNA as it evolves. Emphasis will be placed on studying their product technology (e.g. System 38, 4300, 8100, Series H, etc.) as well as their network architecture specifications to ensure we have attractive and competitive solutions on a systems basis.

DEC TO IBM

SURVIVAL

	FY80	FY81	FY82
3780, on M, M+, TRAX,	124	68	---
3270 (BSC) on PDT	62	---	---
3270 (BSC) on VMS	124	---	---
COMPLETE 3790 P.E. on RSX-11M	31	---	---
3780 ON RSTS	93	---	---
HASP ON VMS	124	---	---
BSC IN NCC	124	---	---
MAINTENANCE	177	204	150
	859	272	150

COMPETITIVE PARITY

	FY80	FY81	FY82
ARCHITECTURE			
SNA integration into DNA	62	68	75
3270 Virtual Terminal Support	62	---	---
3270 (SNA) on PDT	62	204	---
3790/8100 on VMS	124	136	---
	310	408	75

LEADERSHIP

	FY80	FY81	FY82
* MASTER 3270 TERMINAL SUPPORT ON VMS	132	---	---
* SNA IN NCC	186	204	---
	0	204	0
	===	===	===
	1169	884	225

* NOT FUNDED IN FY80 AND NOT INCLUDED IN ROLLUP

COMMUNICATIONS HARDWARE

DEFINITION

Provide hardware communications interfaces. Also provide consultant expertise in communications technology to other groups within Digital.

PRODUCT LINES BENEFICIARIES/MARKET:

All Product Lines

FY80 TACTICS

Complete the DMP-11 in order to provide a DDCMP, multi-drop device to provide synchronous communications capability for Unibus systems. This capability is needed for transaction processing systems such as TRAX and all mid-range/high end systems which need to provide effective terminal and multidrop system support.

The DMV-11 will be the complement to the DMP-11 for Qbus systems.

Complete the cost reduced version of the asychronous multiplexed communications (DZ11-H). It will include full modem control.

Provide a 100% compatible replacement device for the DMC-11 in order to improve the reliability and reduce support cost. The tactic to be followed here is to use the M8207 being designed for the DMP-11, and rewrite the present DMC-11 microcode.

As part of our support effort, we have assumed responsibility for COMM LINE TESTS required by Field Service and manufacturing for link level testing.

Develop a cost effective bit-stuff capability for the low-end. This device is fundamentally a single line synchronous device, at up to 56 kbps, and costing less than $130 to manufacture.

Develop a single line 56 kb synchronous device with a PDP-11 ISP and sufficieent RAM to support any protocol implementation (DNA, SNA, BISYNC, X.25, etc.). This device will be a single board (hex) implementation and will cost less than $500 to manufacture. It will be based on the FONZ-11 communications design presently contained in the VT-162.

Develop a PDP-11 ISP (QUAD) card ($300 transfer cost) for the QBUS machines. This will allow one communications hardware configuration, to support multiple protocols, on the QBUS. This device will replace the DMV multi-drop development.

Provide a family of intelligent communication controllers that combine synchronous and asychronous capabilities on a single board which plugs into a box configuration and ranges from $300 to $3000 in transfer cost.

High production volume/low speed modems have been developed and are being used in terminals and boxes. This effort will continue and be funded by the Product Lines. Corporate business plans will be developed for this area. Issues of manufacturing, distribution and support will be resolved. The prime focus for FY80 will be the 212 full duplex two wire modem. The auto-call (DN01) card and 103 modem box will also be combined.

An Auto Call product will be an outgrowth of our present modem efforts and will replace the present DN11. This capability is necessary to provide remote, unattended operation that is critical to the commercial market place.

Advanced development will address the low cost local interconnect as well as data encryption, security, modems and fiber optics areas.

COMMUNICATIONS HARDWARE

SURVIVAL

	FY80	FY81	FY82
DZ11H (ASYNCH. MUX.)	100	---	---
DMC11 (V2)	90	---	---
DMP11 (MULTIDROP DDCMP)	250	---	---
QBUS FONZ-11 INTERFACE (NCC)	60	100	---
UNIBUS FONZ-11 INTERFACE (NCC)	250	150	---
LOW COST BIT STUFF FOR QBUS	163	---	---
ADVANCED DEVELOPMENT	106	250	---
SUPPORT, Standards, ECO Vouchers	487	750	900
DMV11	280	---	---
	1786	1250	900

COMPETITIVE PARITY

	FY80	FY81	FY82
* LOW COST COMM. CONTROLLER FOR VAX	150	50	---
* AUTODIAL UNIT	96	---	---
* 212 MODEM	202	66	---
	0	116	---

LEADERSHIP

* HIGH SPEED INTERCONNECT (AD)	200	250	300
* MODEMS (AD)	100	150	200
* FIBRE OPTICS (AD)	200	250	300
	0	650	800
	1786	2016	1700

* NOT FUNDED IN FY80 BUDGET AND NOT INCLUDED IN ROLLUP

HYDRA *

DEFINITION

The HYDRA program will provide system offerings which will enable Digital to secure and develop the dominant position in the high availability/data integrity market. The components developed to satisfy the above requirements may be selectively utilized across the range of VAX systems to increase system availability and/or data integrity. The basis for development is a multicomputer system composed of VAX family processors interconnected by a high speed interprocessor link. Additional components will be developed as required in order to meet high availability requirements. Software utilized will be extensions of the standard VMS operating system.

MARKET/PRODUCT LINES

MDC and TELCO are expected to be the major beneficiaries initially. Over the long term, the remaining Commercial Product Lines will also benefit.

FY80 TACTICS

Address high availability market with ICCS and a layered VMS software product.

LEADERSHIP

FY80	FY81	FY82
5535	6000	---
====	====	
5535	6000	

* FOR A MORE DETAILED DESCRIPTION OF THIS PROGRAM, PLEASE CONTACT PETER VAN ROEKENS.

36/32-BIT COEXISTENCE

DEFINITION

Evolve the 36-bit business to a 36/32-bit coexistence environment by FY85. 36-bit systems will be maintained and utilized for compatibility with the existing base, while 32-bit systems will provide increasing functionality for both the existing base and new customers.

MARKET/PRODUCT LINES

All Product Lines marketing 36-bit equipment.

FY80 TACTICS

Evolve the requirements and product plans for VMS support of the coexistence strategy.

Begin the development of the tools necessary to make the 36/32-bit interconnected systems strategy viable.

	FY80	FY81	FY82
RMS-20/RMS-32 Convergence	120K		
36/32-BIT DATA INTERCHANGE UTILITY (DIU)	80K		
* APL/SF on VAX	156K**		
	=======	===	===
	200K	N/A	N/A

* SEE LSD RED/BEIGE BOOKS FOR FURTHER DETAIL.

** NOT INCLUDED IN ROLL UP.

APPENDIX II.

SCHEDULE OF MAJOR PROGRAMS

SCHEDULE OF MAJOR PROGRAMS

	PROGRAM	TARGET DATE
1.	DECNET PHASE III	
	M/M+/VMS	1H FY80
	TRAX/PDT	2H FY80
	RSTS	1H FY81
2.	IBM INTERCONNECT	
	2780/3780 (TRAX/SCS/M/M+)	1H FY80
	2780/3780 RSTS	1H FY80
	3271 (VMS/PDT)	2H FY80
	BSC (NCC)	1H FY81
	SNA 3790 (M/M+)	1H FY80
	SNA 8100	1H FY81
	SNA (PDT/3270)	2H FY81
3.	X.25 M/M+/VMS	2H FY80
4.	NETWORK COMM. CONTROLLER (NCC)	1H FY81
5.	RSX-11M+/MP	1H FY80
6.	PDT V2 (INCL. 11M SUPPORT)	2H FY80
7.	HYDRA	2H FY81
8.	SCS/RSTS	1H FY81
9.	VAX BUSINESS SYSTEMS EXTENSIONS - PHASE 1 (COBOL-79/SORT/MERGE/DATATRIEVE)	1H FY81

SCHEDULE OF MAJOR PROGRAMS

(Continued)

	PROGRAM	TARGET DATE
10.	TRAX V2.0	1H FY81
11.	DBMS-32	1H FY82
12.	11/780 ICCS	1H FY81
13.	COMET ICCS	Q2/Q3 FY81
14.	MERCURY	1H FY81
15.	HYDRA	1H FY82

APPENDIX III.

FY80 GET / DON"T GET LIST

CENTRAL SOFTWARE ENGINEERING

SOFTWARE PRODUCT GETS

32-BIT SOFTWARE	FY80($000)
VMS	2617
Includes:	
Maintenance	
Technical Consulting to other groups	
Quarterly Auto Patch Kits	
Crash Dump Analyzer	
New HW Support (COMET, HYDRA, NEBULA, ICCS, DML, DMP, PDT, DR750, MA750, VT100, KMC-DUP, RXOX on UNIBUS, etc.)	
DECnet Phase III	
Files (Chained access, file allocation/retention/ disk mgmt. control, multivolume swap/page/ temporary sort files).	
Exec. enhancements (diskless VMS, resource allocation and control, AME support).	
Performance Evaluation	
Native Mode Utilities	
WCS Tools	
Disk Quotas, Wildcard Directory	
Shadow recording, common journaling	
Fast Backup/Restore Utility	
RMS-32	345
DATATRIEVE-32	165
DBMS-32	429
Distributed Data Mgmt. Facility (DDMF)	116
COBOL-79	743
COBOL-74 (Maintenance)	66
BASIC +2	429
BASIC PLUS (AME)	164
Sort/Merge-32	99
Editor-32	99
APL*	--*
PASCAL PLUS-32	130
ADA-32 (DOD-1)	65
FORTRAN IV PLUS	455
Common Object Time System	561
VAX Debugger	132
VMS Programmers Workstation *	--*
HYDRA	5535

* SEE LSD RED BOOK

CENTRAL SOFTWARE ENGINEERING

SOFTWARE PRODUCT GETS

(Continued)

32-BIT SOFTWARE (Continued)	FY80 ($000)
TRAX-32	182
Commercial Applications Terminals Subsystem (CATS)	462
RSTS to VMS Batch Stream Conversion	129
Systems Integration, Test and Documentation (RSTS/VMS)	248
36/32 Interconnect (RMS & Data Interchange Utility)	200
16-BIT SOFTWARE	
TRAX-16	858
RSTS	198
SCS/RSTS	479
ADE	330
Small COBOL	396
RSX-11M/S	520
Includes: Maintenance & Maintenance Releases; Field Support Tools (e.g. Auto Patch, Documentation improvements, etc.); Performance improvements; Easier Sysgen	
Small RSX-11M Environmental Enhancements (for 11/23 and PDT)	260
Kernel 2 (K2) Support	585
Includes: Common Code Support for TRAX-16, M+, 11/74 MP; New Hardware Support; TRAX-16 Base Level Integration Enhancements	
RSX-11M PLUS	375
Includes: Product Release and Support; Post VI MP Enhancements	
IAS (Maintenance Only)	235

CENTRAL SOFTWARE ENGINEERING

SOFTWARE PRODUCT GETS

(Continued)

16-BIT SOFTWARE (Continued)	FY80 ($000)
Mass Storage Drivers	595
Common Files/Utilities (25-30 of them)	650
Includes: Maintenance and Enhancements Certification in New System Releases 16-Bit Backup/Restore Utility	
RMS-11	585
DBMS-11 (Maintenance Only)	66
DATATRIEVE-11	83
Forms Management System (FMS-11)	455
Includes: Maintenance FMS V2.0 FMS Migration to M, M+, SCS/RSTS, VMS	
COBOL-11 (Maintenance)	281
BASIC+/BASIC+2 (Maintenance)	330
Sort/Editor (Maintenance	33
FORTRAN IV PLUS (Selected ANS-77 Features)	325
APL-11	65
RT-11	715
Includes: Support Field Support Tools (Auto-patch, error logging) Usability (New Sysgen, Installation Manual, Improved Help File) Software Support Manual New HW Support (11/23, 11/24, 11/44, TS04, RL02, RX03, etc.) PDT and Very Small System Run Time Environment Enhancements	

CENTRAL SOFTWARE ENGINEERING

SOFTWARE PRODUCT GETS

(Continued)

16-BIT SOFTWARE (Continued)	FY80 ($000)
BASIC-11 (Maintenance)	195
FORTRAN IV (Maintenance)	195
PDT Support	260
Includes: Maintenance; PDT V2.0 Software; Foreground Communications; Upgraded Documentation; Performance Analysis	
RT Emulator on RSX-11M (for PDT Dev.)	114
Terminal Architecture	260
Distributed Intelligent Terminal	65
SSC/PASCAL	520
Includes: Linkable Standard SW Components (SSC) for support of run time only dedicated applications (e.g. milling machine); An Implementation Language (PASCAL); Applications Development Environment under RT-11	
DEC - DEC COMMUNICATIONS	
DECnet Maintenance	390
DECnet Phase III on M, M+, VMS, TRAX, RSTS	602
X.25 Extensions on RSX-11M (Telenet, Euronet)	124
DECnet PDT Enhancements	124
Start DECnet Phase IV on PDT, M, M+, VMS	204
Includes: X.25 Enhancements; X.29; Network ("virtual") Terminals; NCC; Network Management	

CENTRAL SOFTWARE ENGINEERING

SOFTWARE PRODUCT GETS

(Continued)

DEC - IBM COMMUNICATIONS	FY80 ($000)
Maintenance	177
3780 on M, M+, TRAX	124
3270 (BSC) on PDT	62
3270 (BSC) on VMS	124
3790 Emulator on RSX-11M (Completion Effort)	31
3780 on RSTS	93
HASP on VMS	124
BSC in NCC	124
COMMUNICATIONS HARDWARE	
Support, Standards, ECOs	487
DZ11H (Async. Mux.)	100
DMC11 (V2) - DMR11	90
DMP11 (Multidrop DDCMP)	250
QBus FONZ Interface (NCC)	60
UNIBUS FONZ Interface (NCC)	250
Low Cost Bit Stuff for QBus	163
DMV11	280
OTHER	
Advanced Development	1272
Includes:	
PL/1	
Distributed Data Processing (DDP) Program	
Network Congestion Control	
NCC2	
NDA/X.25	
Human Factors	
Architecture	612
Tools and Technology	609
DECnet Certification	558
Systems Assurance	180
Product Management/Planning	1709
Comm'l Quality Management	528

CENTRAL SOFTWARE ENGINEERING

SOFTWARE PRODUCT DON'T GETS

32-BIT SOFTWARE	($000)
RMS-32 File Design Manual	33
RMS-32 Hashed and Chained	99
IBM Tape Conversion	99
RMS-11 Remote Access	190
IBM Remote File Access	173
DATATRIEVE Data Entry	83
Back End DBMS	132
IBM COBOL Converter	161
FIPS Flagger	99
COBAID	132
Generalized Menu Interface for VMS	165
SNA and IBM Virtual Terminals	400
KMC 2780/3780/3271	99
Incremental Performance Analysis	132
More Aggressive PASCAL-PLUS	325
More Aggressive TRAX-32	400

16-BIT SOFTWARE	
TRAX-16 Foreign Terminal Support	297
SCS-11 on RSX-11M	1182
SCS Features on RT/CTS-300	300
RSTS V7.1 (not SCS/RSTS)	297
ADA-11 (DOD-1)	195
PASCAL-11 on M, M+, RSTS	195
Micro-Isam (RT/PDT)	195
ROM/BASIC for PDTs	195
K2 (M+/MP/TRAX) Unibus I/O Leveling	130
ODS-II on M, M+/TRAX	260
MP Auto-Reconfiguration	277
ANS-77 for F4	195
TRAX-16 Multi-Processor	130
16-Bit WCS Exploitation	130
Fixed Function Appl. System *	150*
Personal Computer Software	179
Memory Only RT	130
T-11 Support *	65*
Electronic Mail Product	350

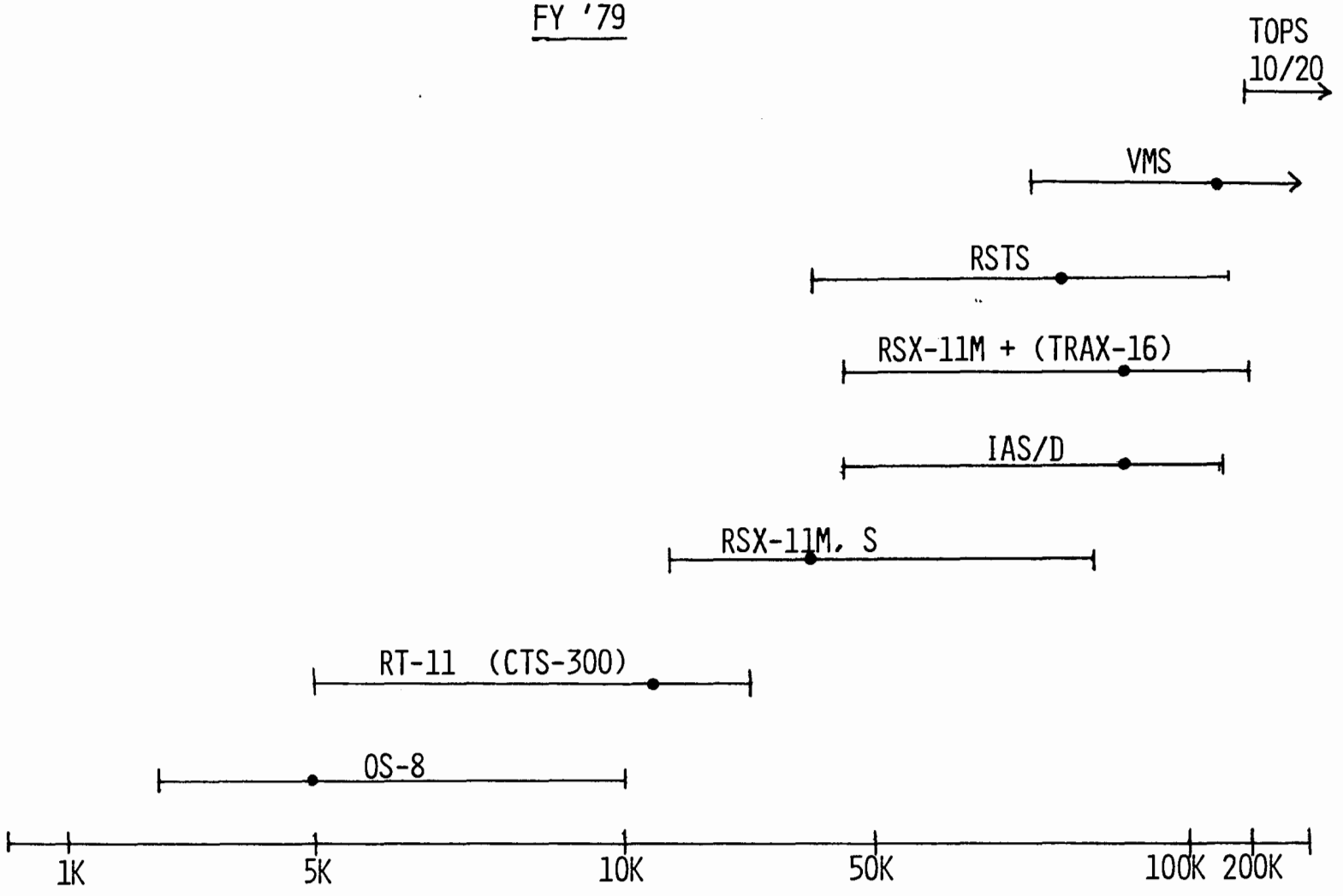
* MAY BE P.L. FUNDED

DECnet / COMMUNICATIONS	($000)
Local X.25	62
HDLC	124
Master 3270 Support on VMS	132
SNA in NCC (for all operating systems)	186
Network Management Tools	132

COMMUNICATIONS HARDWARE	
Low Cost Comm. Controller for FAX	150
Autodial Unit	96
212 Modem	202
High Speed Interconnect (Advanced Dev.)	200
Modems (Advanced Dev.)	100
Fiber Optics (Advanced Dev.)	200

OPERATING SYSTEM DESIGN POINTS & RECOMMENDED * RANGE

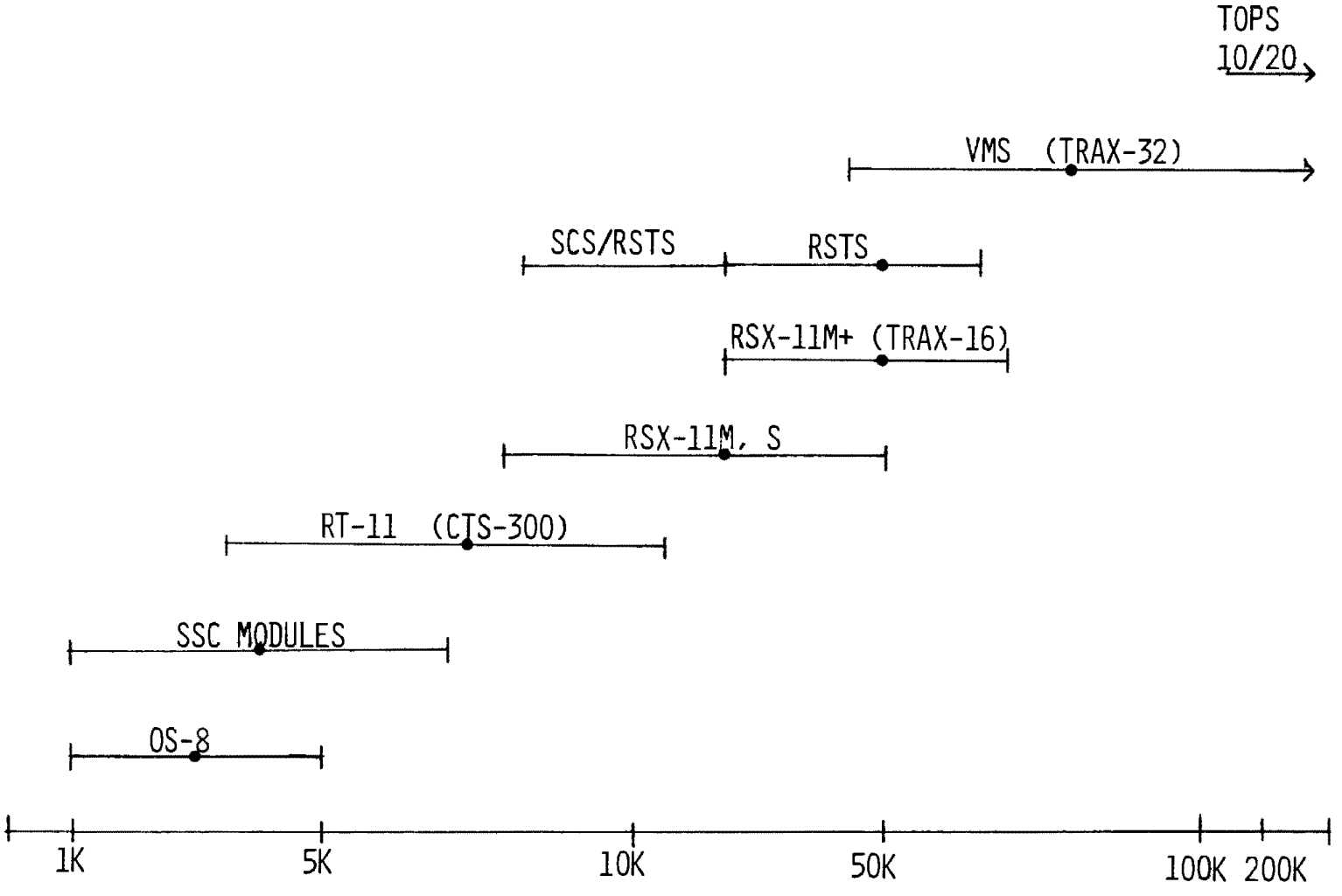
FY '79



* NOT ABSOLUTE MIN., MAX.

OPERATING SYSTEM DESIGN POINTS & RECOMMENDED * RANGE

FY'82



* NOT ABSOLUTE MIN., MAX.

STORAGE

SYSTEMS

REDBOOK

A SUMMARY OF STORAGE STRATEGIES,

PRODUCT TACTICS,

AND COMPETITIVE TRENDS

JULY, 1979

M. S. GUTMAN

ML3-6/E94

DTN: 223-5285

TABLE OF CONTENTS

INTRODUCTION

A. SCOPE

STORAGE SUBSYSTEMS ENCOMPASS THE AREAS OF DISK, TAPE, ATTACHMENTS, AND MEMORY. THEIR STRATEGIES, TACTICS, COMPETITIVE POSITIONS AND TECHNOLOGIES ARE ADDRESSED IN THREE SEGMENTS: LOW-END, MID-RANGE, AND HIGH-END.

B. DEFINITIONS

THE ABOVE THREE SEGMENTS HAVE BEEN DEFINED IN TERMS OF COMPUTER SYSTEM SELL PRICES:

LOW-END:	COMPUTER SYSTEMS WHICH WILL SELL FROM 0-$25K*
MID-RANGE:	COMPUTER SYSTEMS WHICH WILL SELL FROM $25K*-$250K
HIGH-END:	COMPUTER SYSTEMS WHICH WILL SELL FROM $250K AND UP

*THIS BOUNDARY MAY BE ADJUSTED TO $16K IN THE FUTURE

C. BASIC CORPORATE PRODUCT STRATEGY

THE BASIC CORPORATE PRODUCT STRATEGY (G. BELL MIGRATION/COEXISTENCE STRATEGY) DOES NOT MAKE ANY SPECIFIC STATEMENTS RELATIVE TO STORAGE. THE STORAGE STRATEGY DOES SUPPORT THE "SYSTEM" PRODUCT CONCEPT AND, THEREFORE, SHOULD SUPPORT, AND NOT BE IN CONFLICT WITH, THE CORPORATE PRODUCT STRATEGY.

GOALS - STORAGE SYSTEMS DEVELOPMENT

1. Develop and/or acquire competitive storage components, devices, and attachments that primarily match the systems needs of the corporation and that are secondarily saleable in the components marketplace.

2. Be in a leadership position relative to our systems, third party, and selected components competition, recognizing that generally, IBM has a dominating lead.

3. Encourage the establishment of broader distribution channels for storage products at both the systems and components levels.

4. Track storage technologies and provide a memory hierarchy of winners for the systems that we sell.

5. Emphasize the quality, reliability, and ease of use of our products.

6. Measure ourselves as our customers measure us and evolve our metrics as our customers or markets evolve. Although storage products are primarily technology driven, we recognize that availability, cost of ownership, and cost/performance are primary metrics.

STORAGE STRATEGY

A. LOW-END

1. DISK: MAINTAIN LOW COST REMOVABLE HARD DISK LEADERSHIP AND REACH COMPETITIVE PARITY IN FLEXIBLE DISK

   COMMENT: LEADERSHIP IN HARD DISK DEPENDS ON:

   A. CONTINUED MIGRATION OF HIGH-END TECHNOLOGIES INTO THE LOW-END FASTER THAN COMPETITION.
   B. DEVELOPING NEW TECHNOLOGIES INTO THE LOW-END FASTER THAN COMPETITION.

   RESOURCE LIMITATIONS HAVE FORCED A CHOICE BETWEEN HARD AND FLEXIBLE DISK DEVELOPMENT - WITH HARD DISK PREVAILING. COMPETITIVE CAPACITY FLEXIBLE PRODUCT OFFERINGS WILL BE OBTAINED BY TIMELY BUYOUT IN THE NEAR TERM WITH LICENSING POTENTIAL TO MEET VOLUME AND COST OBJECTIVES.

2. TAPE: <1/2" TAPE IS A LEADERSHIP POINT PRODUCT. EXAMINE FOLLOW-ON OPPORTUNITIES.

   COMMENT: CONTINUE TO EXPLORE OPPORTUNITIES FOR COST EFFECTIVE BLOCK MODE 1/4" TAPE PRODUCTS. EMPHASIS SHIFT FROM SMALL (256KB) TO LARGER CAPACITIES.

3. ATTACHMENTS: PRIMARY NEED FOR LOW-ENTRY COST SUPPORTS MOVEMENT TOWARD INTEGRATED ATTACHMENT AND SHARING OF HOST CPU POWER AND PACKAGING.

4. MEMORY: MAINTAIN LEADERSHIP THROUGH TIMELY UTILIZATION OF INDUSTRY AVAILABLE RAM'S AND SEMI-CUSTOM LSI.

   COMMENT:

   A. THIS SEGMENT WILL CONTINUE TO BE PREDOMINATELY INTEGRAL CONTROL AND STORAGE PER MEMORY MODULE WITH EMPHASIS ON LOW COST

   B. CONTINUED EVALUATION OF NEW TECHNOLOGIES (E.G., BUBBLES) AND THEIR IMPACT ON THE LOW-END DISK/TAPE OFFERINGS AND FUTURE MEMORY HIERARCHIES.

STORAGE STRATEGY (CONTINUED)

B. MID-RANGE

1. DISK: CONTINUED TECHNOLOGY INVESTMENT TO REACH A HIGHLY COMPETITIVE POSITION IN FIXED DISKS AND MAINTAIN TIMELY BUYOUT POSITION IN LARGE REMOVABLE DISKS.

   COMMENTS:

   A. "WINCHESTER" TECHNOLOGY BASE IS BEING BUILT AND WILL SUPPORT OUR PRODUCT OFFERINGS ACROSS THE CAPACITY SPECTRUM.

   B. SUSTAINED INVESTMENT IN IMBEDDED SERVO TECHNOLOGY COULD LEVERAGE A PROPRIETARY TECHNOLOGY INTO LEADERSHIP REMOVABLE DISK PRODUCTS.

2. TAPE: ESTABLISH COMPETITIVE INDUSTRY COMPATIBLE 1/2" TAPE OFFERING. CONTINUE TO EXPLORE NON-COMPATIBLE TECHNOLOGIES.

   COMMENT:

   A. EXAMINE BUY/BUILD ALTERNATIVES TO REACH 1600/6250 BPI COMPETITIVENESS.

   B. EXAMINE NEW TECHNOLOGIES FOR LOW-COST NON-COMPATIBLE BACKUP AND ARCHIVAL STORAGE

3. ATTACHMENTS: NEED FOR COST EFFECTIVENESS, FLEXIBILITY IN NUMBER AND TYPE OF STORAGE PRODUCTS ATTACHED SUPPORTS CONTINUED DIRECTION TOWARD DEC STANDARD PERIPHERAL AND CORPORATE INTERCONNECTS.

4. MEMORY: MAINTAIN LEADERSHIP THROUGH TIMELY UTILIZATION OF INDUSTRY AVAILABLE RAM'S, SEMI-CUSTOM AND CUSTOM LSI.

   COMMENT:

   1. THIS SEGMENT WILL SEE BOTH INTEGRAL AND NON-INTEGRAL CONTROL AND STORAGE.

   2. OPPORTUNITY FOR LSI COST SAVINGS EXISTS DUE TO ECC USAGE IN THIS SEGMENT.

STORAGE STRATEGY (CONTINUED)

C. HIGH-END

1. DISK: ACHIEVE A TWO YEAR TIME-TO-MARKET LAG ON IBM (≈5 YEAR COST/MB LAG) THROUGH TIMELY BUYOUT, AND EFFECTIVE ATTACHMENTS.

   COMMENT: IT IS UNLIKELY THAT ENVISIONED RESOURCES WILL PERMIT INVESTMENTS LARGE ENOUGH TO BE TECHNOLOGICALLY COMPETITIVE WITH IBM IN THE HIGH-END. ALTHOUGH LICENSING OR REVERSE ENGINEERING ARE LOWER COST AND RISK ALTERNATIVES TO TECHNOLOGY INVESTMENTS, IT APPEARS THAT OUR RESOURCES ALSO FALL SHORT OF FUNDING THESE CHOICES. TO REMAIN AS CLOSE AS POSSIBLE TO IBM WE MUST PURCHASE LARGE DISK PRODUCTS AS THEY BECOME AVAILABLE FROM PCM-LIKE DISK DEVELOPERS. SYSTEM COMPETITIVENESS CAN BE ENHANCED WITH HIGH PERFORMANCE, INTELLIGENT ATTACHMENTS. (IF IBM CONTINUES TO PURSUE THE DUAL ACTUATOR COURSE (3370), OUR RA81 PROGRAM MAY PROVIDE US WITH THE ABILITY TO CUT THE LAG DOWN TO LESS THAN 3 YEARS.)

2. TAPE: CONTINUE BUY APPROACH TO HIGH PERFORMANCE INDUSTRY COMPATIBLE 1/2" TAPE.

   COMMENT: EMPHASIS CONTINUES ON PURCHASE WITH OPTION TO BUILD, COST REDUCTION THROUGH LSI, AND USE OF MORE INTELLIGENT CONTROL.

3. ATTACHMENTS: CONTINUE TOWARDS HIGH PERFORMANCE, COST EFFECTIVE, REMOTELY DIAGNOSABLE INTELLIGENT STORAGE SUBSYSTEM ATTACHMENT.

4. MEMORY: MAINTAIN LEADERSHIP THROUGH TIMELY UTILIZATION OF INDUSTRY AVAILABLE RAM'S, SEMI-CUSTOM, AND CUSTOM LSI.

   COMMENT:

   A. THIS SEGMENT WILL USE PRIMARILY NON-INTEGRAL CONTROL AND STORAGE MODULES.

   B. LSI COST REDUCTIONS EFFECTIVE IN ECC AND INTRICATE CONTROL AREAS.

   C. OPPORTUNITY EXISTS FOR STORAGE COST REDUCTIONS THROUGH USE OF SERIAL AND PARTIALLY GOOD MEMORY DEVICES.

PROGRAM AND PRODUCT DEVELOPMENT TACTICS

A. LOW-END

1. TU58:

The TU58 offers very low entry cost random access 1/4MB storage by employing block mode formatted tape cartridges. It is intended to be sold in three ways:

A. Component Level - to OEM's who will embed this micro-peripheral within their equipment.

B. Rack mount - DEC development system sales, systems with minimal Mass Storage need, program loading and update.

C. Embedded - in intelligent terminals, store and forward buffers, software and diagnostic updates and personal media applications.

Transfer Cost: (FY '80)	$390 (dual rack mount)
FCS:	Q1 FY '80
Volume availability:	Q3 FY '80

2. RL02:

The 10MB RL02 offers double the RL01 capacity at approximately the same cost (or one-half the cost/MB), and utilizes the embedded servo techniques used in the RL01. It is intended as the main storage companion for the 11/23 through the 11/44 class of systems and utilizes the existing RL11, RLV11, and RL8A controllers. RL02 and RL01 cartridges are not format compatible.

Transfer Cost: (FY '80)	$1020 (w/o control)
FCS:	Q2 FY '80
Volume Availability:	Q2 FY '80

3. RX02

The RX02 is an 8" single sided, 1/2MB, double density floppy disk. It is industry standard format, and will read and write RX01 diskettes under program control and can be switch configured to emulate RX01. The RX02 is a systems device storage subsystem for CPU's up through the 11/34 class. The RX02 is a DEC design.

Transfer Cost: (FY '80)	$850 (DUAL, without attachment)
FCS:	Q2 FY '79
VOLUME AVAILABILITY:	Q4 FY '79

4. RX03:

The RX03 is an 8" double sided, 1MB, double density floppy disk. It is industry standard format and will read and write RX01 diskettes. (A design goal is to make it RX02 compatible as well.) This product is a buyout mechanism with DEC designed electronics. It will use the same packaging as the RX02. The RX03 is meant to replace/upgrade the RX01 and RX02 in most applications.

Transfer Cost: (FY '81)	<$1300 (DUAL)
FCS:	Q1 FY '81
Volume Availability:	Q2 FY '81

5. AZTEC: (Development funded through Q1 FY '80 - to be reviewed by EBOD at that time)

AZTEC is currently envisioned (due out of advanced development Q3 FY '80) as utilizing removable Winchester technology with 8" hard disk oxide media. Capacity estimate is from 30MB to 42MB, fixed plus removable. The minimum goal is >RL02 capacity and performance at half the cost. Control is integral.

Transfer Cost: (FY '82)	<$1000t
FCS:	2H FY '82
Volume Availability:	1H FY '83

6. MSV11K/L:

The MSV11K/L is a replacement for the MSV11D/E and provides 22 bit address decoding, unibus CSR parity software compatibility and will utilize the 64K RAM when available. It is a dual height module with 128KB to 256KB capacity capability.

Transfer Cost: (FY '81)	$1150 (256KB)
FCS:	Q2 FY '81
Volume Availability:	Q3 FY '81

7. FONZ-11 STANDARD ARRAY: (Funded by CSD)

This array is for use in large capacity FONZ based systems. The control will talk to multiple arrays over a private memory bus. This array is a dual height module with 128KB to 512KB capacity using 16K AND 64K RAM's respectively.

	128KB (16K)	512KB (64K)
Transfer Cost: (FY '81)	$489	$2159
FCS:	Q1 FY '81	Q2 FY '81
Volume Availability:	Q2 FY '81	Q3 FY '81

B. MID-RANGE

TS11 (was TS04)

The TS11 is a 45 ips, 1600 bpi, IBM compatible 1/2" tape drive with very extensive self-diagnostic capability. This drive is intended for use in systems ranging from 11/34's through 11/70's and contains an integral formatter. Interface is to the Unibus.

Transfer Cost: (FY '80)	$3865 (w/o cab.)
FCS:	Q1 FY '80
Volume Availability:	Q2 FY '80

2. RM/RA80

The R80 is a 128MB family of fixed disk drives, developed internally, utilizing Winchester technology. This family represents the backbone of mid-range systems storage.

The RM80 is the first of this family and will be interfaced to the Massbus using the current RM03-type MBA. The second of the family is the RA80 which will be interfaced to the Unibus via the UDA and the ICCS bus via the HSC-50. The RA80 will contain the DEC Standard Disk Bus (SDB).

	RM80	RA80
Transfer Cost: (FY '81)	$4600 (with MBA)	$2700 (without control)
FCS:	Q3 FY '80	Q2 FY '81
Volume Availability	Q4 FY '80	Q3 FY '81

3. RA81

The RA81 is an enhancement of the RA80 with at least double areal density, resulting in a 250-400MB fixed disk drive. The RA81 will also be interfaced utilizing the UDA and HSC-50. Mechanical, electrical, test equipment, and manufacturing process will be as similar to the RA80 as possible.

Transfer Cost (FY '82)	$3000t (without control)
FCS:	Q1 FY '82
Volume Availability:	Q2 FY '82

4. RL04 (Development funded through Q1 FY '80 - to be reviewed by EBOD at that time)

RL04, as currently envisioned, is an 84MB, two platter, (42MB fixed, 42MB removable), rack mounted, top loaded, embedded servo technology disk system. It is an extension of the RL01/RL02 family but utilizes the Standard Disk Bus interface to attach to the Unibus through UDA or the ICCS bus through HSC-50.

Transfer Cost: (FY '82)	$1650
FCS:	Q1 FY '82
Volume Availability:	Q2 FY '82

5. UDA

The UDA is the first in a family of Mass Storage attachments which provide Standard Disk Bus to Unibus attachment. The UDA provides a Unibus to Standard Disk Bus interface on two hex modules and will be used with RL04, RA80, and RA81 storage products. Each UDA can attach up to four storage products. (Attachment to BI is also a goal.)

Transfer Cost: (FY '81)	$800
FCS:	Q2 FY '81
Volume Availability	Q3 FY '81

6. TS6250 (Development funded through Q1 FY '80 - to be reviewed by EBOD at that time)

This program is to provide low cost (<$5000) 6250 bpi, GCR, IBM compatible 1/2" tape drive. Buy/build possibilities for both mechanism and electronics will be explored. Cost reduction of the TU78 electronics is also a possibility. A closer look at the 1600 bpi product area will be made (including the IBM 8809) to determine if additional work is required in this area as well.

Transfer Cost: (FY '82)	<$5000t
FCS:	2H FY '82
Volume Availability:	1H FY '83

7. MS11-M (64K)

Upgrade of the MS11-M (11/44 Memory) to utilize the 64K RAM and to use the LSI ECC chip if available. Maximum capacity will become 1MB per Memory module, including ECC.

Transfer Cost: (FY '81)	(1MB) $4637
FCS:	1H FY '81
Volume Availability:	2H FY '81

8. 11/750 UPGRADE (64K)

Array evaluation, controller revisions and power supply changes required to upgrade the COMET CPU to utilize Memory using 64K RAM's. Maximum capacity will be 1MB per array.

Transfer Cost: (FY '81)	(1MB) $4404
FCS:	1H FY '81
Volume Availability:	2H FY '81

9. 11/780 UPGRADE (64K)

Array redesign to double the chip count and utilize both 16K and 64K RAM's. Resultant maximum capacity will be 512KB or 2MB per array.

	512KB (16K)	2MB (64K)
Transfer Cost: (FY '81)	$1232	$8142
FCS:	1H FY '81	1H FY '81
Volume Availability:	2H FY '81	2H FY '81

10. NEBULA (Funded by MSD)

The Nebula contains a WCS module having a 16K X 24 Writable Control Store, 256KB of 64K RAM memory, system clock and console control. A second module, the memory-I/O controller, has memory timing and control, memory mapping, and bus arbitration. It will drive up to 4 additional memory arrays, each having 1MB capacity and using 64K RAM devices.

	WCS & 256KB	CONTROL	1MB ARRAY
Transfer Cost: (FY '81)	$1647	$636	$4404
FCS:	Q1 FY '81	Q1 FY '81	Q1 FY'81
Volume Availability:	Q2 Fy '81	Q2 FY '81	Q2 FY '81

C. HIGH-END

1. TU77

The TU77 is a 125 ips, 800/1600 bpi high performance 1/2" IBM compatible tape transport. This drive features include auto load and auto threading, is intended to replace much of the TU45 volume and be used in 11/70 and larger systems. This is a drive buyout and an in-house formatter build.

Transfer Cost: (FY '80)	$8700 (Master), $6900 (Slave)
FCS:	Q4 FY '79
Volume Availability:	Q1 FY '80

2. TU78

The TU78 is a 125 ips, 1600/6250 bpi high performance 1/2" IBM compatible tape transport. This program includes a buyout mechanism and an in-house formatter (TM78) design and build. It will be used on 11/70 and larger systems (a backup program with STC is being pursued through CSS).

Transfer Cost: (FY '81)	$11000 (Master), $7200 (Slave)
FCS:	Q2 FY '81
Volume Availability:	Q3 FY '81

3. RP07 (Formerly RP07+)

The RP07 is a buyout Winchester Technology 516MB fixed media disk system which includes integral Mass Bus interface and extensive internal diagnostics. It will attach to 11/70 and larger systems utilizing the appropriate RH controller. A substantial amount of remote diagnosability has been designed into this drive. Dynamic dual access capability is provided as an option (several backup potentials are possible with three major disk vendors).

Transfer Cost: (FY '81)	$11000
FCS:	Q2 FY '81
Volume Availability:	Q3 FY '81

4. RM05

The RM05 is a 256MB, removeable, buyout disk drive interfaced to the Massbus via the MBA. This product has some commonality to the RM03 but requires a new pack (RM05P). It will be utilized on the 11/70 through the 2060 CPU's using the appropriate RH control.

Transfer Cost: (FY '81)	$11000
FCS:	Q1 FY '81
Volume Availability:	Q2 FY '81

5. HSC-50

The HSC-50 is an intelligent storage subsystem control which interfaces the RL04, RA80, and RA81 to the ICCS Bus (attachment to BI is also a goal). It is a microprocessor based subsystem, capable of handling multiple disks, with provision for extension to tapes, buyout disk drives, etc., provides extremely high performance, extensive error correction, internal diagnostics capability, and optional cache features. System utilization includes 11/780, Hydra, Venus, and 2080.

Transfer Cost: (FY '82)	$3700t
FCS:	Q3 FY '82
Volume Availability:	2H FY '82

6. VENUS ARRAY (Funded by LCG)

The VENUS memory array will utilize 64K dynamic RAM's and a new dual multiplexor chip on an extended hex board containing 256K X 39 memory.

Transfer Cost:	TBD
FCS:	Q4 FY '82
Volume Availability:	Q2 FY '83

NON-PRODUCT DEVELOPMENT

A. ADVANCED DEVELOPMENT PROGRAMS (FY '80 $3400)

1. SYSTEMS

A. I/O Architecture - Moving files system functionality into storage subsystems. Continued interconnect work.
B. Further LSI in UDA and HSC. BI interface introduction to Storage. Develop standard tape interface.
C. Hierarchies - system integration, simulation, evaluation
D. LSI test vehicles in subsystems
E. ECC test vehicles in subsystems

2. LSI

A. Complete Serdes
B. Read/write data chip
C. Start several of the following LSI programs (not all)
   1. Standard disk bus
   2. VLSI of UDA channel
   3. Disk read/write
   4. TU5800/Floppy read/write
   5. Data separation
   6. Tape read/write

3. ADVANCED MECHANICS AND MECHANICS SYSTEMS

A. Flex Pivot - Prove or abandon two proposed pivot strategies
B. Continued enhancements to SAP_

4. ADVANCED READ/WRITE, CODES, SERVOS

A. Continued evaluation of heads and media
B. Continue search for and evaluation of better mod/demod codes - maximum liklihood and partial response codes
C. Search for best tape code
D. Select best cartridge tape and floppy code for high density
E. Continued advanced disk read/write system development
F. Start advanced tape and floppy read/write system development
G. Restart advanced ECC work
H. Continue advanced servo work

5. AZTEC

A. Complete first generation bread board, addressing entry cost, loadable Winchester head, integral purging blower, etc.
B. Support transfer to product development
C. Start next generation - increased electronics integration, R/W LSI, plated media

6. VIDEO TAPE AND CONTROL

A. Continue and complete VTR advanced development
B. Continue work with Sony and Panasonic
C. Work to first pass electronics and microcode
D. Work out first generation spec and architecture
E. Demo and evaluate system applications.

7. ADVANCED MEMORIES

A. Complete evaluation of small stager - bubbles and TU58
B. Continue testing of the CCD/bubble emulator
C. Provide system test vehicles for bubbles and support circuits
D. Work out best bad loop and error control strategies

8. VIDEO DISKS

A. Interface and evaluation of Philips consumer video disk
B. Work out system control, R/W system, data formatting, etc.
C. Continue to track new, emerging R/W technologies.

9. HEADS

A. Aztec - loadable for use with Winchester technology, including gimbal and load spring
B. Tape - modification of existing heads to be TS11 compatible
C. Floppy - advanced floppy head evaluation
D. RL - head evaluation and qualification
E. Thin Film - evaluation of new heads as they become available
F. Low Flying Heads - evaluation and application of new information to our products - R81, etc.
G. Composite Head - evaluation of composite material heads as an alternative to thin film heads - to be used in conjunction with high-performance media

10. MEDIA

A. Aztec - development of a removable cartridge
B. Floppy and Tape - evaluation of new media
C. RL - evaluation of new media
D. Plated Disk - evaluation and/or development of plated media for future disk program--R81 disk, advanced Aztec. May need to support pilot manufacturing.

11. OTHER

A. Ferrite Development - materials and process development to permit DEC to produce hot pressed MnZn and NiZn ferrites.
B. Magnetic Modeling - of magnetic cores for conventional, composite and thin film head analysis .

B. TOOLS (FY '80 $1655K)

1. DYNAMIC RAM EVALUATION AND QUALIFICATION

Ongoing evaluation and qualification of main memory 4K, 16K, and 64K dynamic RAM's and the support of incoming inspection.

2. STATIC RAM EVALUATION AND QUALIFICATION

Ongoing evaluation and qualification and incoming inspection support for static RAM's used in cache, writable control store, buffers, terminals and CPU's.

3. LIFETEST SYSTEM/ARRAY DEVELOPMENT

Construction of new capacity, maintenance and data - logging of existing capacity, for reliability measurements and vendor selection, MTBF prediction, for dynamic and static RAM's, CCD and bubbles, operated in a system environment.

4. DEVICE/SYSTEM TEST EQUIPMENT ENGINEERING

Strategize and develop the necessary engineering and manufacturing test equipment for large, high speed RAM's, and bubbles.

5. BUBBLE DEVICE EVALUATION AND QUALIFICATION

Evaluation and qualification of 92K, 256K, and 1M bit bubble devices and incoming inspection support.

6. COMPETITIVE EQUIPMENT EVALUATION

Evaluation of storage related competitive products (tape, disk, memory, attachments).

ISSUES, CONCERNS, AND CONSTRAINTS

1. ISSUES

A. THE FOLLOWING PRODUCTS WERE NOT FUNDED (THE DON'T GETS) FOR FY '80 DEVELOPMENT.

1. $500 ENTRY (INCA) FLOPPY DISK
2. TU5800 - >10MB 1/4" CARTRIDGE TAPE
3. QDA - Q BUS TO STANDARD DISK BUS ATTACHMENT
4. VIDEO TAPE - FOR ARCHIVAL STORAGE
5. CUDI - PCM PORT FOR HSC-50

ITEMS 1, 2, AND 4 ARE STILL BEING PURSUED AS TO FEASIBILITY WITHIN ADVANCED DEVELOPMENT.

B. THE CORRECT REMOVABLE MEDIA STRATEGY FOR THE CORPORATION IS NOT YET UNDERSTOOD. FOR THIS REASON THE RL04, AZTEC, AND TS6250 HAVE BEEN FUNDED THROUGH Q1 FY '80 TO PERMIT AN EXTENSIVE AND INTENSIVE TASK FORCE REVIEW OF THIS SUBJECT, TO INCLUDE THE FOLLOWING AREAS OF CONCERN:

1. DATA BACKUP AND ARCHIVING
2. DATA INTERCHANGE
3. SOFTWARE DISTRIBUTION
4. SYSTEM SIZE (FUNCTIONALITY, COST, PACKAGING)
5. APPLICATION (MARKET)
6. SOLID STATE (IMPACT ON SMALL STORAGE DEVICES)
7. OPERATING SYSTEMS
8. PRICE/PERFORMANCE

2. CONCERNS

A. AS WE REFOCUS OUR LOW-END EFFORTS INTO EVEN LOWER COST SYSTEMS, THE NEED FOR PRODUCTS LIKE THE $500 ENTRY SMALL FLOPPY WILL BECOME MORE PRESSING. WE BELIEVE WORK SHOULD HAVE BEGUN IN FY '80 TO GET PRODUCTS READY - BUT FUNDING LEVELS DID NOT PERMIT THIS TO OCCUR. (CAN THE NEED FOR <$100 STORAGE BE FAR AWAY?)

B. VIDEO TECHNOLOGY MAY BE THE ANSWER TO LOW COST ARCHIVAL STORAGE IN THE NEAR FUTURE. AGAIN THIS YEAR THIS PROGRAM HAS BEEN LIMITED TO ADVANCED DEVELOPMENT DUE TO ITS RELATIVELY LOW PRIORITY AND FUNDING LIMITATIONS.

C. FLOPPY SYSTEMS
WILL ULTIMATELY GROW IN SIZE TO 3 TO 5MB PER DISKETTE. NO FOCUS FROM THE PRODUCT LINES IN THIS AREA TODAY MAY ONCE AGAIN PUT US IN THE UNENVIABLE POSITION WE FOUND OURSELVES IN WITH THE RX03 - A YEAR OR MORE LATE TO MARKET.

D. HSC-50 HAS CONTINUED TO RECEIVE A GREAT DEAL OF ATTENTION. FURTHER ENERGY MUST BE EXPENDED TO INSURE THAT HIGH END ATTACHMENTS (CUDI), TAPE AND INDUSTRY STANDARD INTERFACED DISKS CAN BE EFFECTIVELY ATTACHED.

E. WE ARE CURRENTLY RE-EVALUATING OUR BUYOUT STRATEGY, ASSESSING WHETHER OR NOT WE ARE BUYING THE RIGHT PRODUCTS FROM THE RIGHT VENDORS.

F. THE SYSTEMS GROUP MUST HELP IN THE TIME ALIGNMENT OF ALL SEGMENTS OF A SYSTEM--CPU, TAPE, DISK, SOFTWARE, AND ATTACHMENTS. THERE IS SO MUCH TIME MOVEMENT NOW BETWEEN THESE ELEMENTS THAT IT IS ALMOST IMPOSSIBLE TO ANNOUNCE WITH COMPLETE CERTAINTY ALL WILL BE AVAILABLE.

3. CONSTRAINTS

A. FUNDING (OR LACK THEREOF) HAS FORCED MANY TRADEOFFS TO BE MADE BY STORAGE, SYSTEMS, AND THE PRODUCT GROUPS DURING THE FY '80 FUNDING PROCESS. A CLEAR INPUT FROM ALL PRODUCT GROUPS WAS THAT STORAGE WAS UNDERFUNDED. WE HOPE THAT THE "SYSTEM FOCUS" WILL HELP REMOVE THIS CONSTRAINT FOR THE FUTURE.

B. THE LACK OF SOLID AND SUBSTANTIATED PRODUCT GROUP INPUTS CONCERNING STORAGE WAS MUCH IN EVIDENCE THROUGHOUT THE FY'80 FUNDING PROCESS. THE PRODUCT GROUPS MUST FOCUS ON WHAT THEIR MARKETS WILL NEED THREE TO FIVE YEARS OUT SO THAT WE MAY PUT IN PLACE A BETTER SET OF ADVANCED AND PRODUCT DEVELOPMENTS IN ORDER TO BE PROPERLY RESPONSIVE.

FY '80 STORAGE BUDGET

COMMITTED PROJECTS*:	$15031K
ADVANCED DEVELOPMENT:	3400
PRODUCT MANAGEMENT:	830
PRODUCT SUPPORT:	1601
ADMINISTRATION:	490
TOOLS:	1655
CONTINGENCY:	586
	$23593

*COMMITTED PROJECTS:

LOW-END

TU58	$100K
RL02	514
RX02	260
RX03	950
AZTEC/RL04**	2225
MSV11H/L	100

MID-RANGE

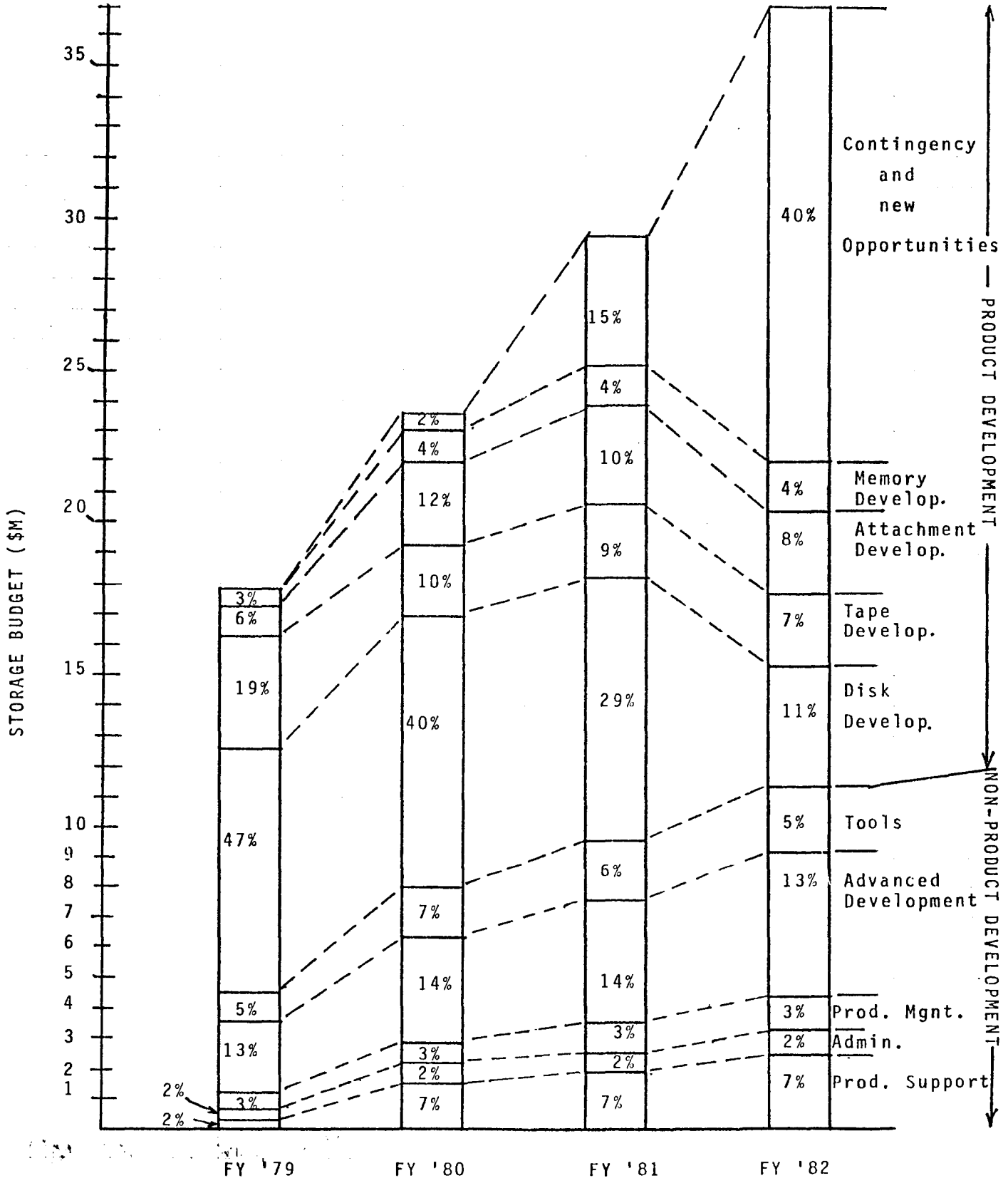
TS11	300
RM/RA80	3429
RA81	570
RL04/AZTEC**	(2225)
UDA	1133
TS6250**	850
MS11-M (64K) UPGRADE	156
COMET (64K) UPGRADE	232
11/780 (64K) UPGRADE	183

HIGH-END

RM05	500
TU77	100
TU78	1000
RP07	500
HSC-50	1575
HSC CACHE	354
	$15031K

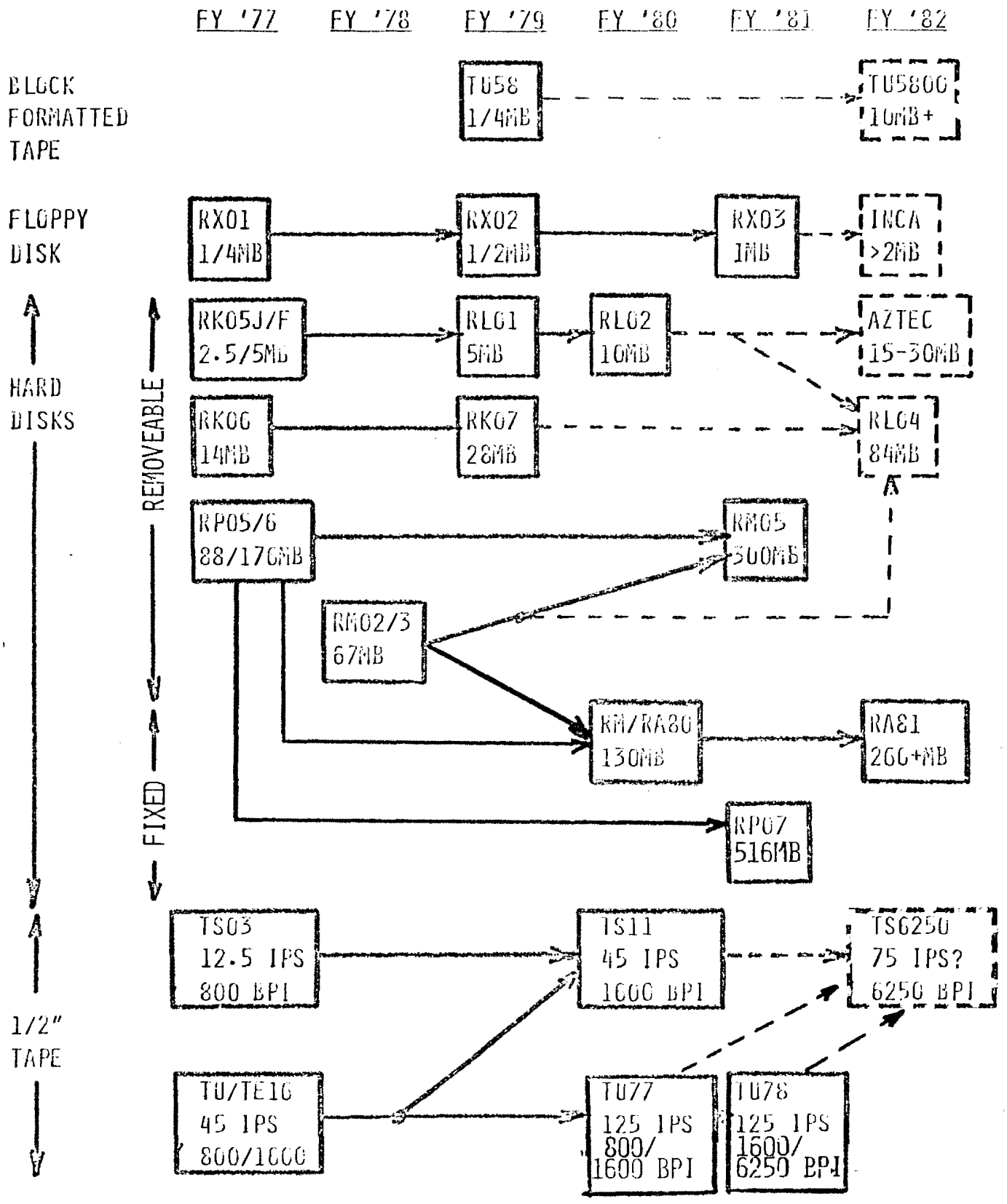
** FUNDED THROUGH Q1 FY '80 - SUBJECT TO EBOD REVIEW

FY '79-82 STORAGE SPENDING/PROJECTIONS



M.S. GUTMAN

STORAGE PRODUCT MIGRATION



STORAGE PRODUCT CALENDAR

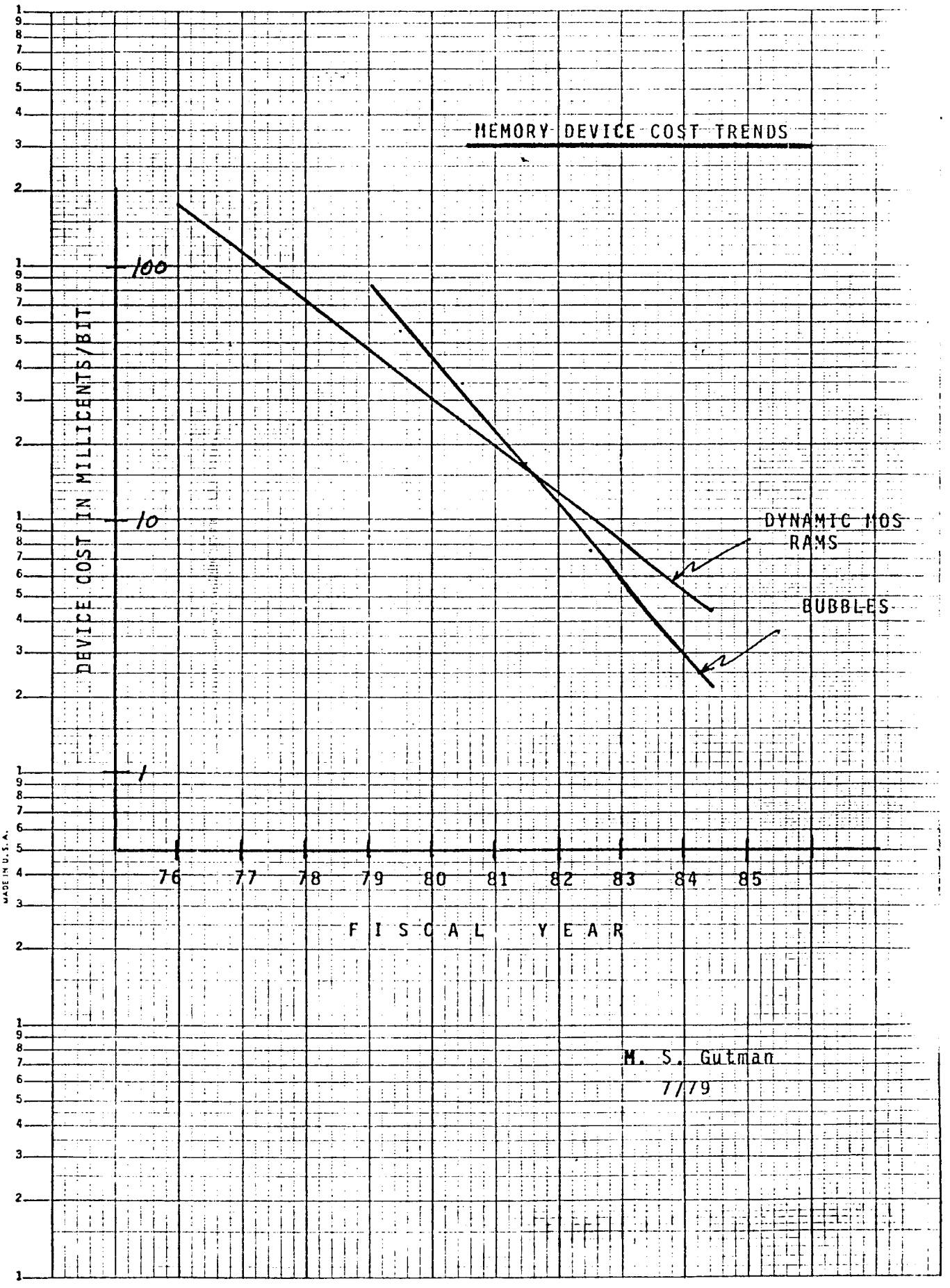
PRODUCT	DESCRIPTION	FCS**	TRANSFER COST***
LOW-END			
TU58	1/4MB BLOCK MODE CARTRIDGE TAPE	Q1 FY '80	$390 (DUAL)
RL02	10MB REMOVEABLE DISK DRIVE	Q2 FY '80	$1020
RX02	1/2MB DOUBLE DENSITY FLOPPY DRIVE	Q2 FY '79	$850 (DUAL)
RX03	IMB DOUBLE DENSITY, DOUBLE SIDED FLOPPY	Q1 FY '81	$1300 (DUAL)
AZTEC*	30-42MB REMOVEABLE 8" DISK DRIVE	2H FY '82	$1000t
MSV11K/L	64KB-256KB DUAL HEIGHT MEMORY FOR F-11	Q2 FY'81	$1150 (256KB
FONZ ARRAY	128KB-512KB DUAL HEIGHT ARRAY FOR 11/23	Q1 FY '81	$489/$2159
MID-RANGE			
TS11	45IPS, 1600BPI 1/2" IBM COMPATIBLE TAPE	Q1 FY '80	$3865
RM/RA80	128MB FIXED DISK, MBA/SDB INTERFACE	Q3 FY '80 Q2 FY '81	/$4600/ $2700
RA81	250-400MB FIXED DISK, SDB INTERFACE	Q1 FY '82	$3000
RL04*	42MB FIXED/42MB REMOVEABLE DISK DRIVE	Q1 FY '82	$1650
UDA	STANDARD DISK BUS TO UNIBUS ATTACHMENT	Q2 FY '81	$800
TS6250*	75-125IPS(?) 6250BPI 1/2" IBM COMPATIBLE TAPE	2H FY '82	$5000t
MS11-M(64K)	64K UPGRADE OF 11/44 MEMORY TO IMB/ARRAY	1H FY '81	$4637
11/750(64K)	64K UPGRADE OF 11/750 MEMORY TO IMB/ARRAY	IH FY '81	$4404
11/780(64K)	64K UPGRADE OF 11/780 MEMORY TO 2MB/ARRAY	IH FY '81	$8142
NEBULA	16K X 24 WCS & 256KB MEMORY, CONTROL	Q1 FY '81	$2283
HIGH-END			
RM05	256MB REMOVABLE DISK DRIVE, MBA INTERFACE	Q1 FY '81	$11000
TU77	125IPS, 800/1600 1/2" IBM COMPATIBLE TAPE	Q4 FY '79	$8700
TU78	125IPS, 1600/6250 1/2" COMPATIBLE TAPE	Q2 FY '81	$11000
RP07	516MB FIXED DISK DRIVE, INTEGRAL MBA	Q2 FY '81	$11000
HSC-50	INTELLIGENT STANDARD DISK BUS TO ICCS BUS ATTACHMENT	Q3 FY '82	$3700
VENUS(64K)	256K X 39 64K ARRAY	Q4 FY '82	TBD

* FUNDED THROUGH Q1 FY '80 - SUBJECT TO EBOD REVIEW

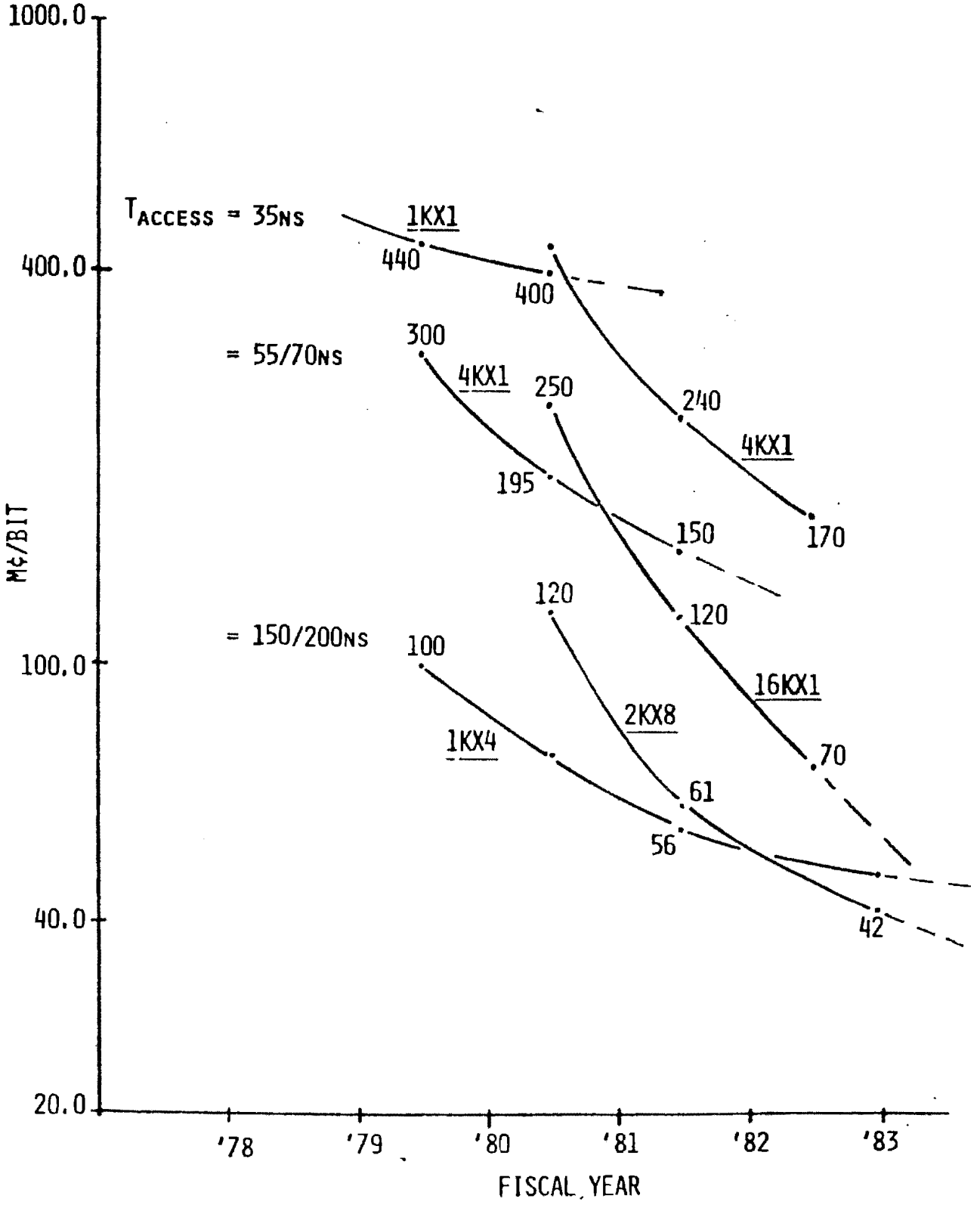
** ALL 64K MEMORY PRODUCTS GATED BY 64K DEVICE AVAILABILITY

*** WITHOUT INTERFACE - UNLESS STATED OTHERWISE

M. S. GUTMAN
7/79

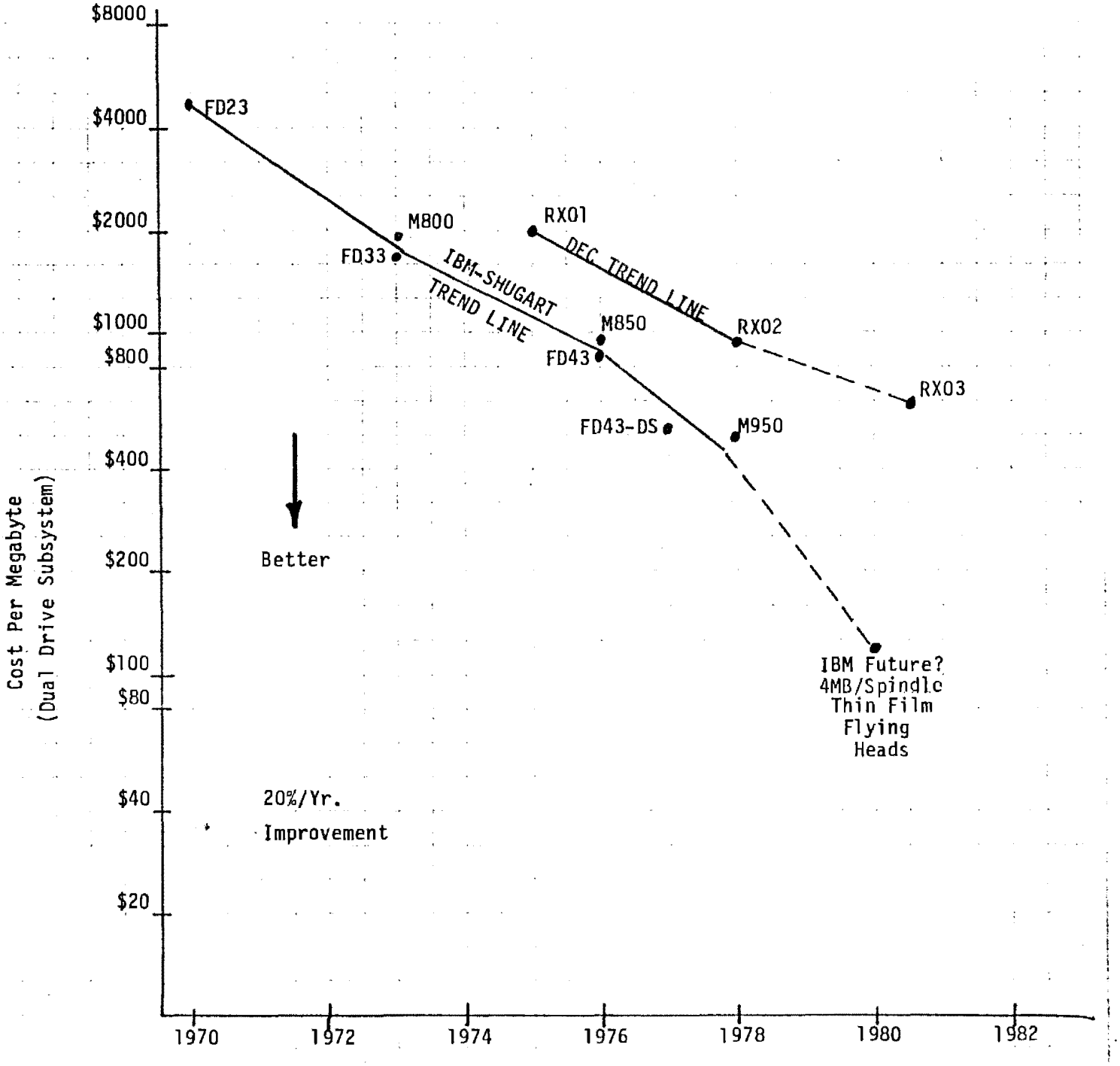


HIGH/MEDIUM/LOW SPEED STATIC DEVICE COST TRENDS



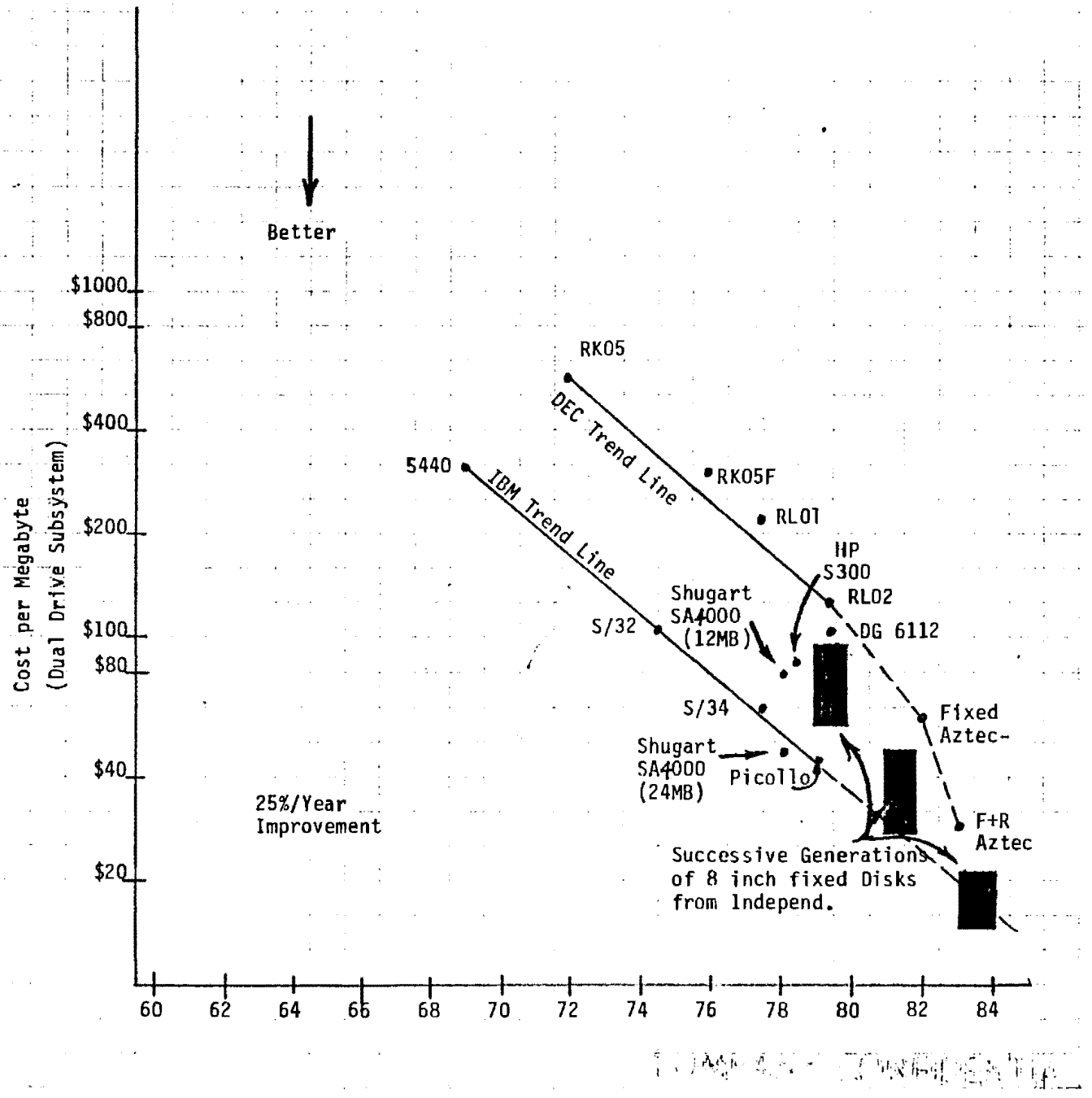
(R. MORRIS--5/16/79)

FLOPPY DISK COST-PERFORMANCE TRENDS



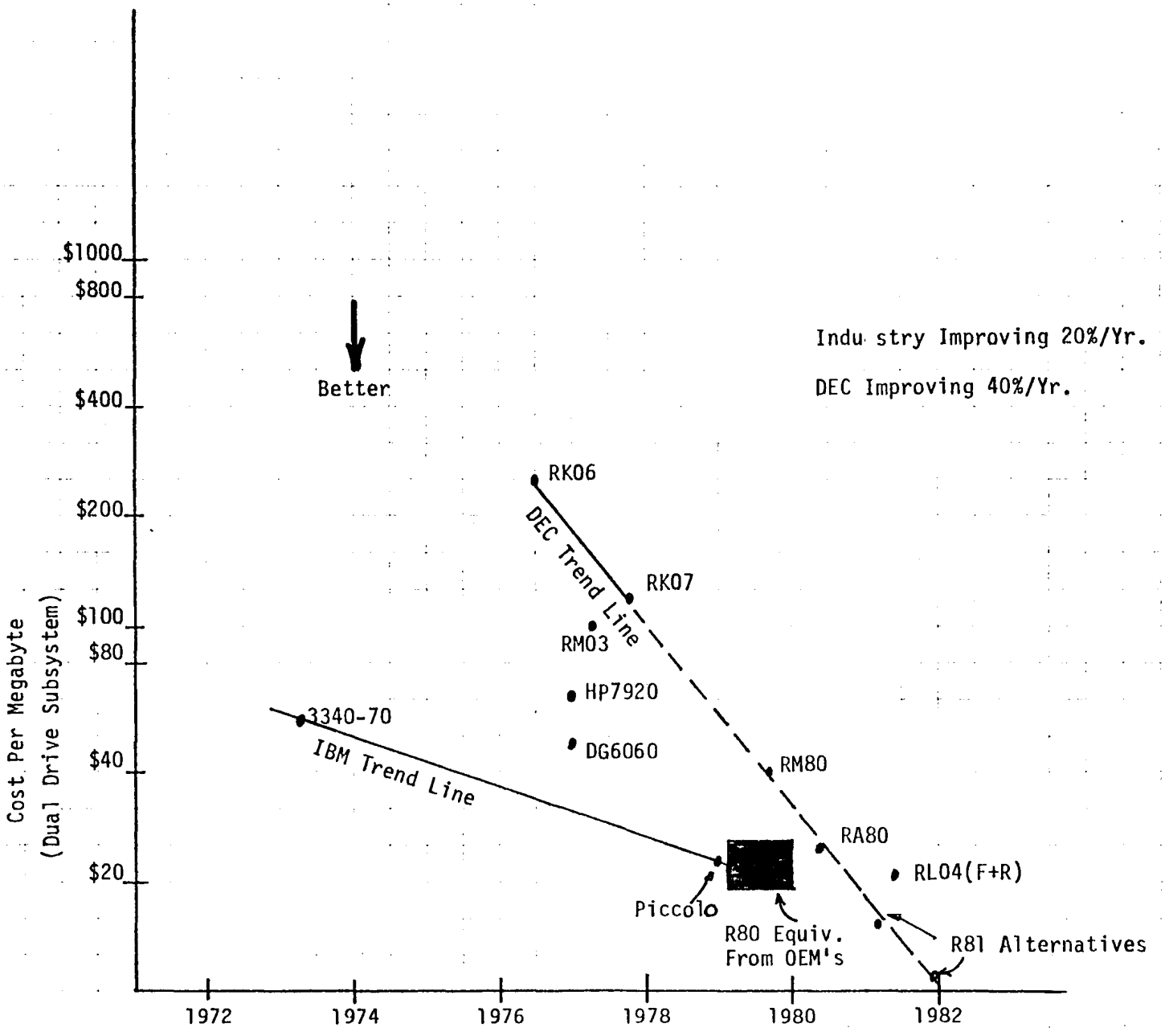
K.Sills
8/7/79

SMALL DISK COST-PERFORMANCE TRENDS



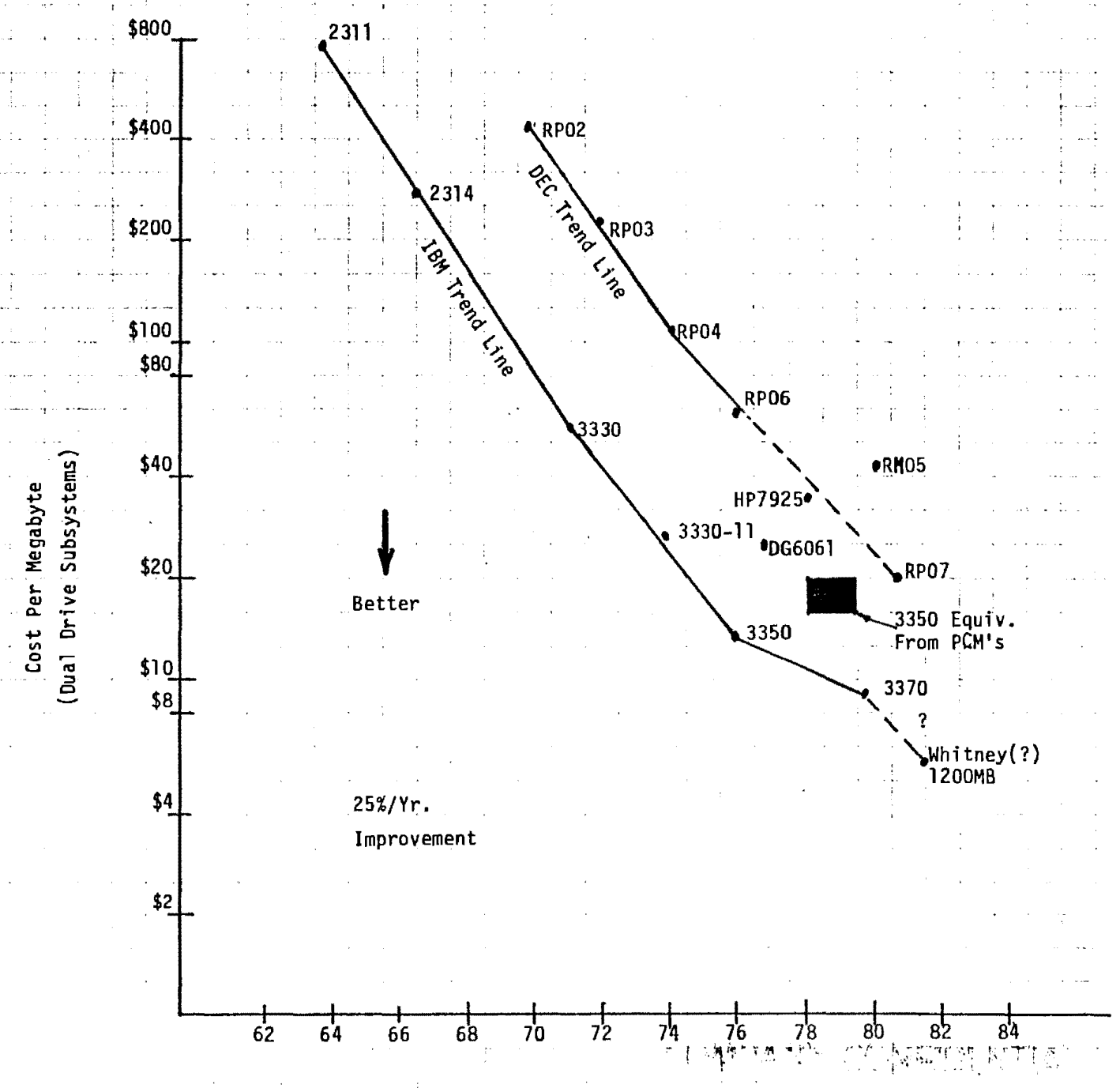
K. Sills
8/7/79

MEDIUM DISK COST PERFORMANCE TRENDS



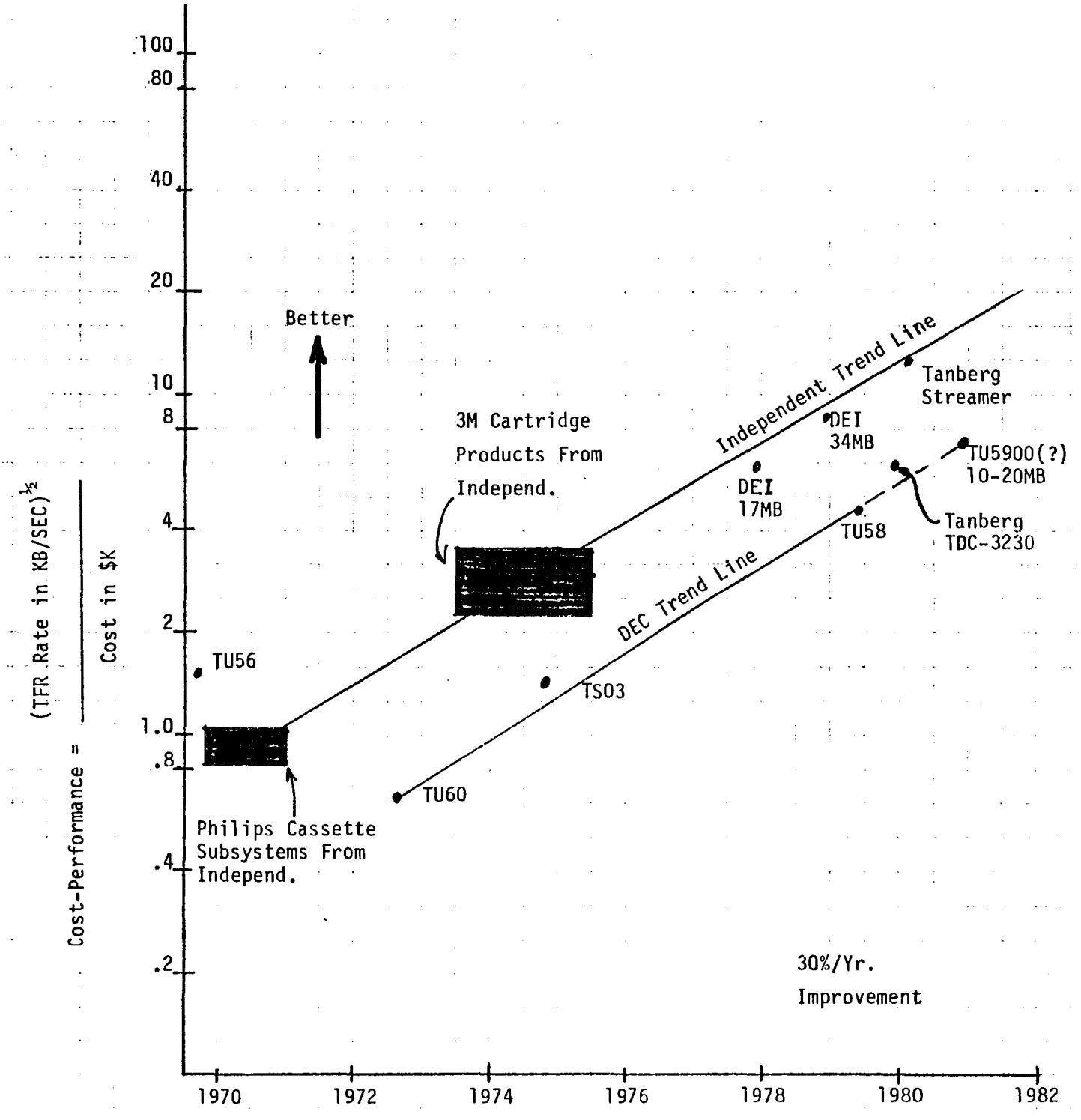
K. Sills
7/20/79

LARGE DISK COST-PERFORMANCE TRENDS



K.Sills
7/20/79

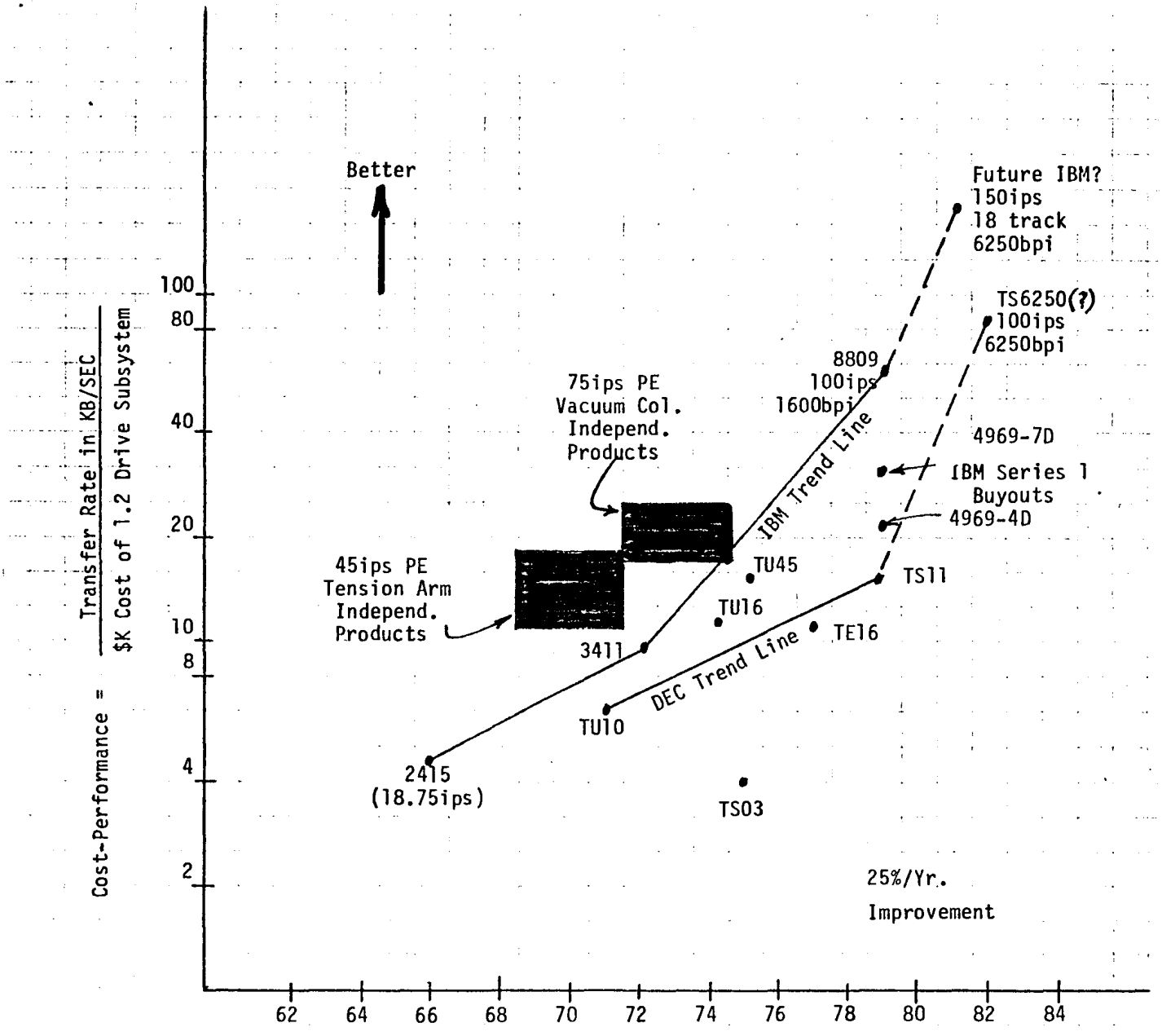
CASSETTE/CARTRIDGE TAPE COST-PERFORMANCE TRENDS



First Customer Ship - Calendar Year

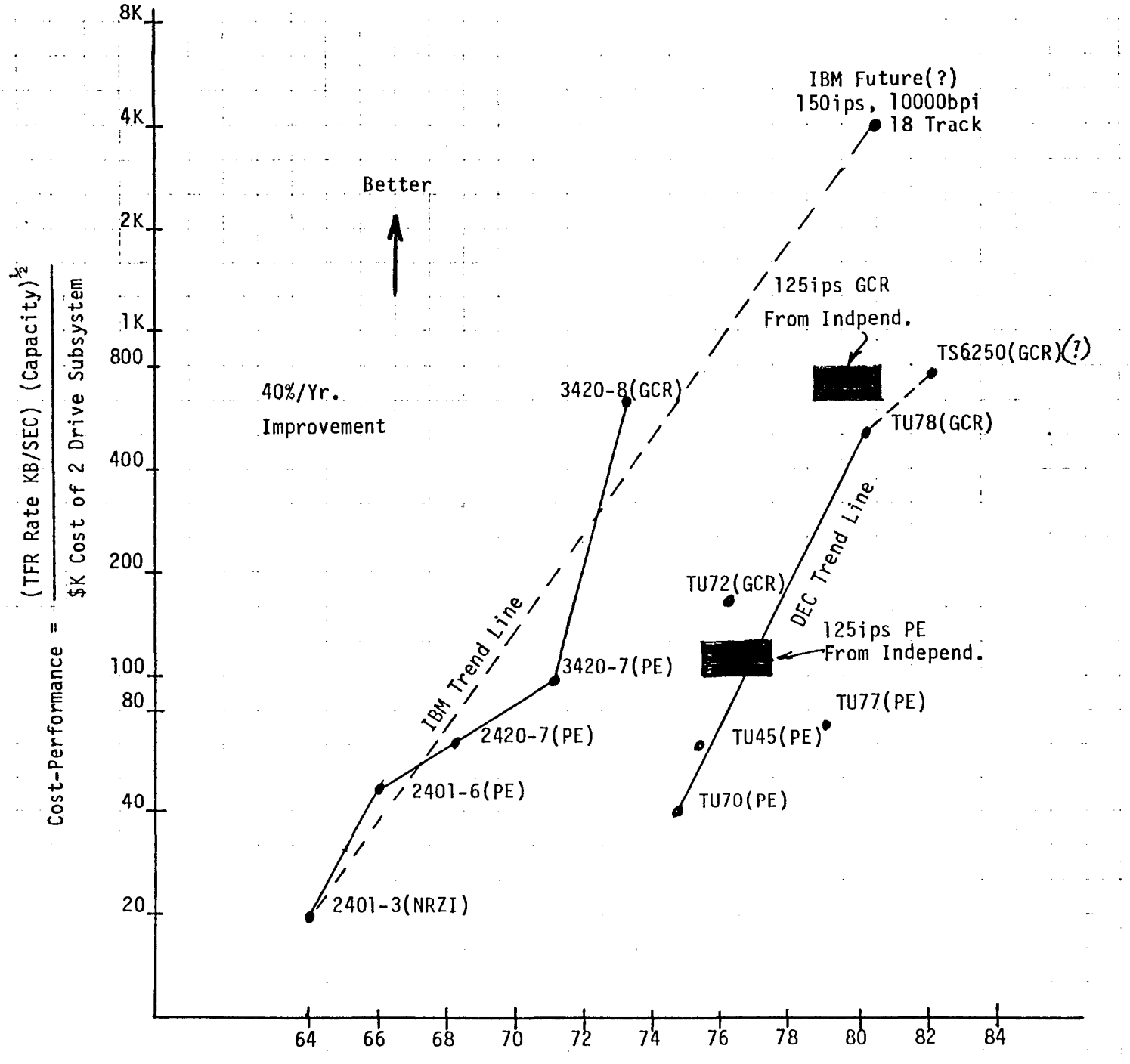
K.Sills
7/20/79

SMALL ½" MAGTAPE COST-PERFORMANCE TRENDS



K.Sills
7/20/79

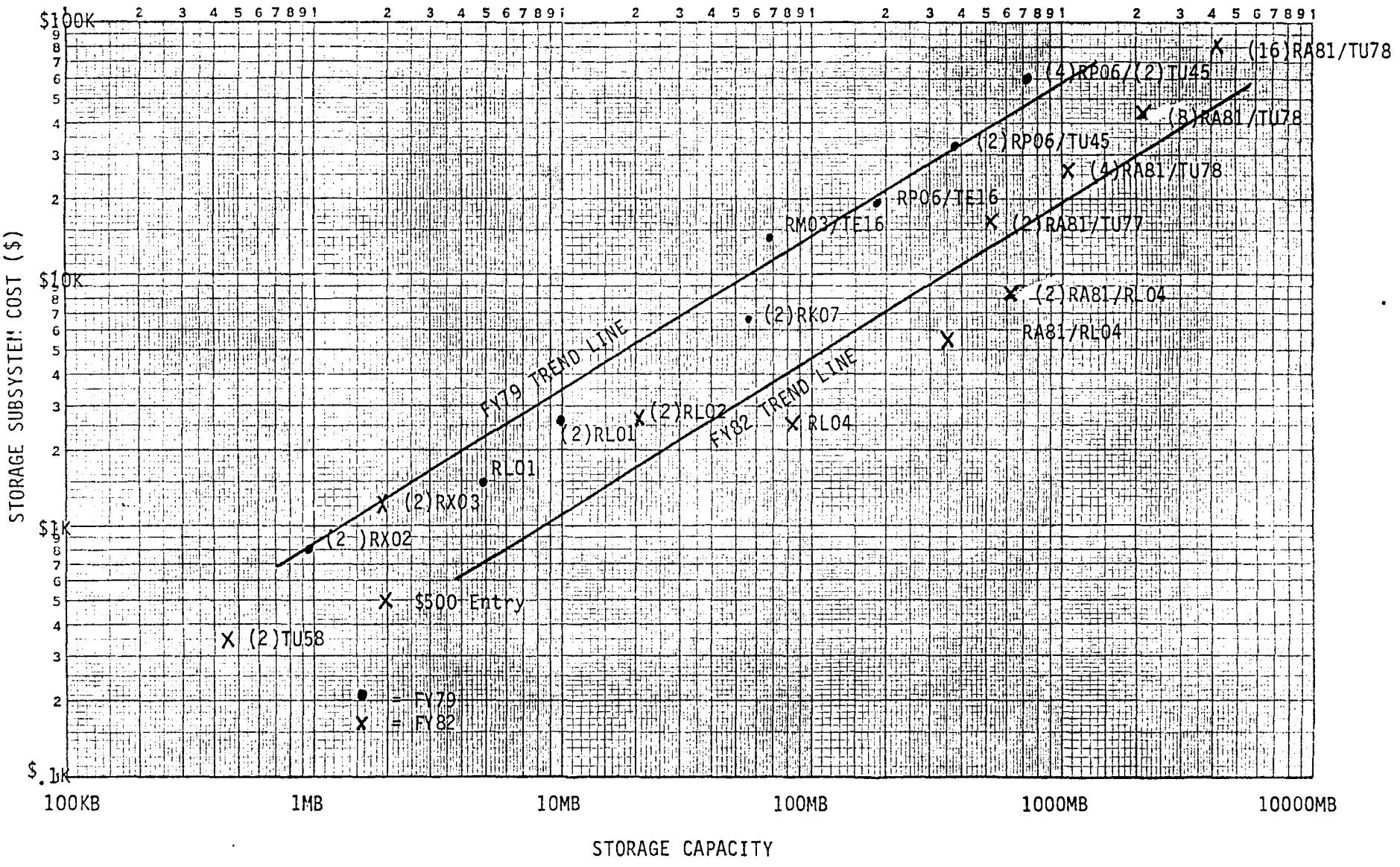
LARGE ½" MAGTAPE COST-PERFORMANCE TRENDS



First Customer Ship - Calendar Year

K.Sills
8/7/79

GOSPEL CHART: STORAGE SYSTEM COST VS. CAPACITY



MSG 3/79

E. Small Systems

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INTEROFFICE MEMORANDUM

TO: Distribution

DATE: 20 June 1979
FROM: Eli Glazer
DEPT: CSD
EXT: 3-4434
Loc/Mail Stop: ML12-2/E71

SUBJECT: CSD RED BOOK

This CSD Red Book is an end of FY79 snapshot of product and functional engineering commitments for FY80 and FY81. It is to be used by Product Lines, Field Sales and Service, Manufacturing, other Central Engineering Groups, and Corporate Management as a base strategy document during FY80. Its intent is to help achieve a better understanding of the Central Engineering view of its objectives in Small Systems, Terminals, Chips, Systems Engineering, and Power/Packaging.

Prepared by: Eli Glazer

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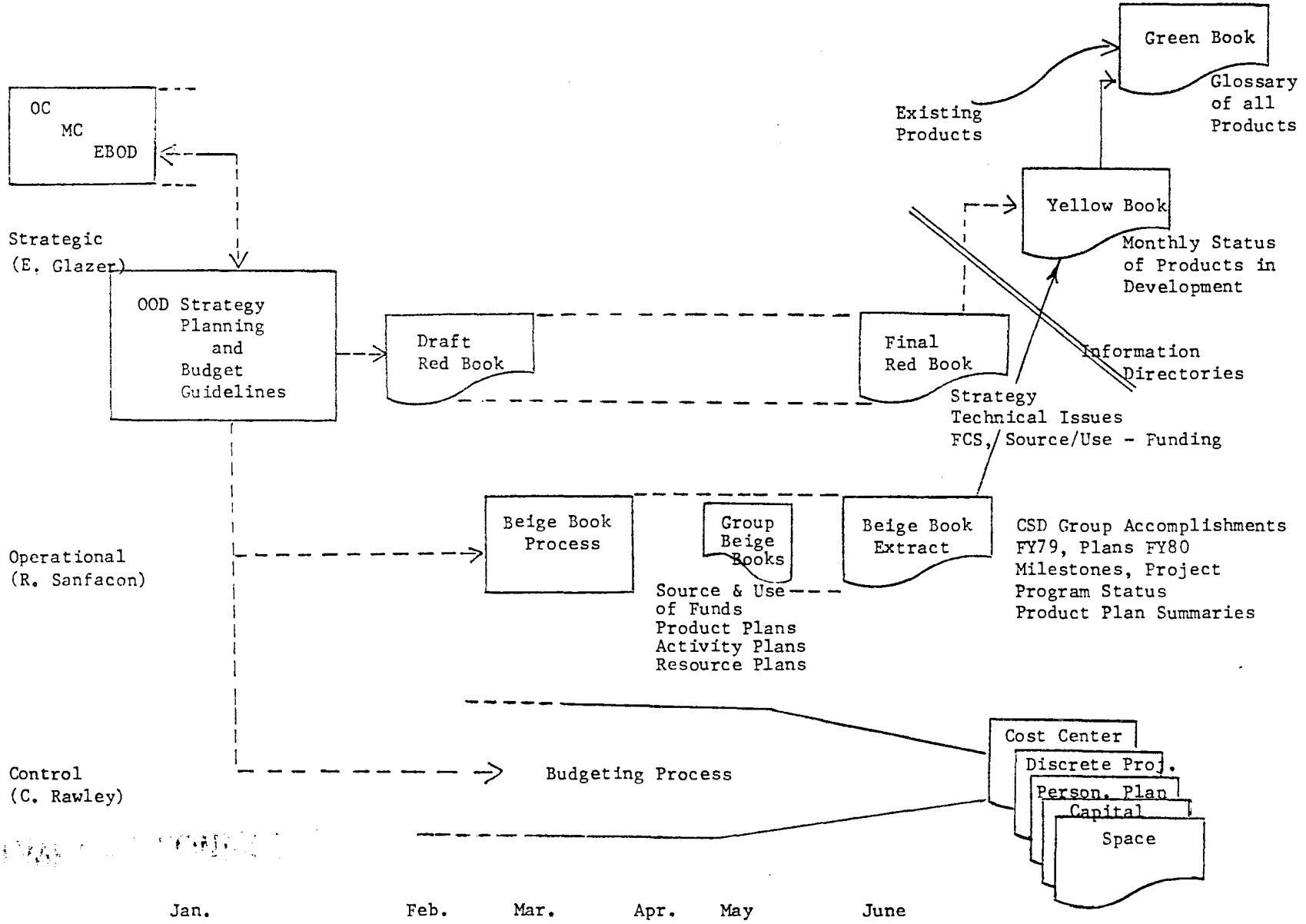
6/26/79

ENGINEERING PLANNING PROCESS FY79 - CSD
DOCUMENTATION FLOW



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FY79
CSD RED BOOK

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Appendix

MANAGEMENT OVERVIEW
COMPUTER SYSTEMS DEVELOPMENT RED BOOK
JUNE 1979

This Red Book is the strategic statement for the product development and functional engineering portions of CSD. Product development represents the central Small Systems and Terminals Engineering of the Corporation and is segmented by:

I. Systems - CPU's and Packages
II. Video Terminals
III. Printing Terminals and Printers
IV. Chips - Semiconductor Components

This strategy is stated in terms of objectives, product targets and financial and budgetary trends.

Functional Engineering consists of:

V. Systems
VI. Power and Packaging

This strategy is stated in terms of objectives by strategic responsibility and financial/budget data and trends.

While CSD accepts the responsibility for being an integration and planning focus for small systems and terminals, less than one-third the corporate budget for this space resides in CSD. The remaining parts of the budget reside in the Mass Storage, Communications and Software Engineering groups along with the several product line engineering groups. Strategic responsbilities are shared by all the groups having budget responsibility for Small Systems and Terminals products.

Systems Packages

The product development thrust for Small Systems and Terminals is to continue the existing thrust of modular flexible computer component engineering which supports bus structured and rack and stack organization of packages or systems. The CPU architecture emphasized is the PDP-11 now with evolution toward VAX in FY85-FY86. At the planning level, increasing attention is being addressed towards integrated total solutions, tools, and production base end products. These products will be targeted to make cost effective use of operating system and applications software previously only available in mid and higher range systems packages.

Very Small Systems and Terminals

The use of increased intelligence inside terminals and the targeting of integrated terminal-like products with systems level functionality has been started in the product lines with WT78 and PDT11/150 type products. Central Engineering developments of video and hardcopy terminals with high levels of functionality through the use of microprocessor controllers are an integral part of the strategy. The high volume cost engineered terminal design will become the housing of future integrated systems packages. Single or possibly multi-chip CPU's, based on the PDP-11 will be the intelligence of choice in these smallest computer packages of the future. The first Central Engineering developments of these integrated products were started with the PDT11/110 and PDT11/130 and will be continued in FY81 with the PDT11/15, a T-11 based intelligent terminal. The next major generation of high functionality terminal products, the LA200 and VT211 families will use the T-11 as the control intelligence. These will be systems like in functionality and have programmable personalities. Features and functons incorporated in these products must be determined by a careful study of market needs. Editing, block mode-communications and graphics will be some of the family of features possible in these new products.

MARKET COMMENTS

An analysis of data provided by the product lines to Bob Steingart (Small Systems Analysis, May 14, 1979) shows the following:

Business**	Annualized Growth* Rate from FY79	FY85* NOR	% of FY85 NOR	% of FY79 NOR
Terminals	26%	$ 364M	5.2%	5.1%
End User Small Systems	51%	$1009M	14.6%	4.7%
OEM/Components Small Systems and Components	29%	$ 725M	10.6%	8.7%

The data further shows that 90% of the growth in the End User segment comes from products which are sold as solutions as opposed to tools or production bases. (Market Study for CSD, May 1979, by Robin Frith).

The growth of End User compared to OEM corroborates findings of the Low End Task Team of the Summer of 1978.

INVESTMENT COMMENTS

The bulk of our central developments continue to be in the traditional modular product orientation. An increasing emphasis at the planning and integration levels is occurring. Software Engineering has committed to projects that are applications/solutions oriented. An increasing portion of product line investments appear to be directed toward applications solutions.

Spending for Planning and Product Management through FY81 assumes increasing efforts in integration and systems level long-range planning focus and a corresponding increase in efficiency of operation resulting in a level spending at about 12% for the present CSD organization. Product development and advanced development represent about 56% of the ongoing CSD budget, with support engineering at about 12% to 14%. The functional engineering group strategy is to decentralize activities and their overall percent of spending is declining at about 1% per year.

The current bottoms-up CSD plan for "committed" projects matches the EBOD guideline within several percent, but the CSD planned budget exceeds the guidelines by approximately 10% in FY82.

* Based on normalizing the 30% per year overall corporate growth indicated in the data collected by Bob Steingart, to a 25% per year growth assumption.

** Determined by which product line submitted the data for Small Systems and Products which are defined by 0-$25K typical price range, includes systems packages based on the PDP-8, VT278 White Tornado, TINY-11, LSI-11, FONZ-11, 11/03, 11/04, and 11/23 CPU's as well as boards, boxes and component terminals.

CSD - SMALL SYSTEMS AND TERMINALS

SUMMARY OF MAJOR CHANGES FROM

FEBRUARY RED BOOK

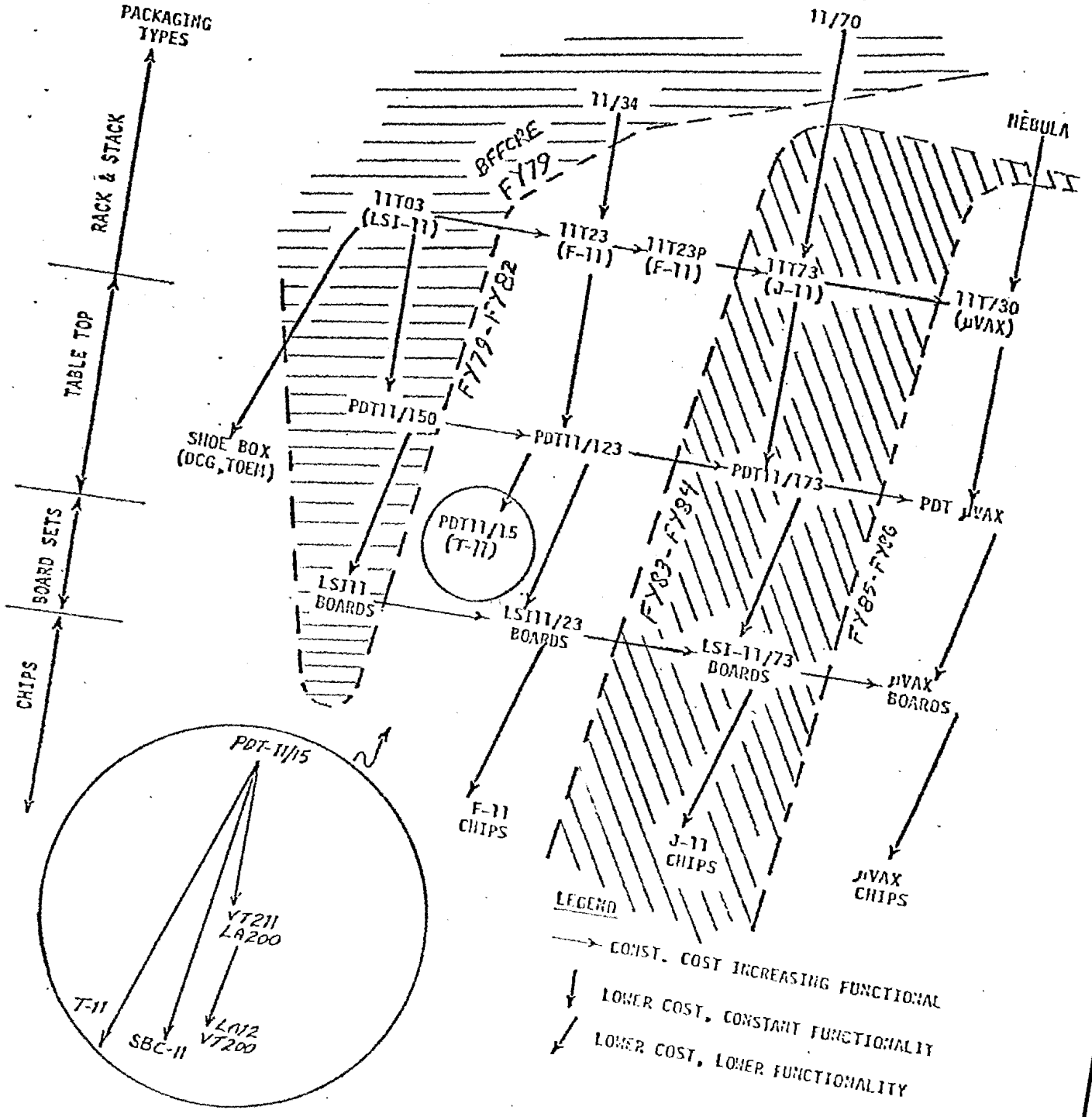
ADD:

- o J-11 (LSI-11/70) advanced development program for an 11/70 class (i.e., functionality and performance multi-chip CPU. This single chip set will be used in the range of small to medium 16-bit systems.
- o BI/NI advanced development for a new backplane interconnect and network interconnect for implementation with the J-11 CPU chipset or sooner. The intent is for this to become the next interconnect discipline merging small and medium (Q-Bus or Unibus) into a single structure, valid to 1990.
- o High resolution dot matrix impact printing terminal

DELETE:

- o 3-mode PAX extensions to F-11
- o Centrally funded PDT11/123 - modular Q-Bus tabletop packaged system (this packaging will be P/L funded)
- o Typewriter terminal

PRODUCT POSITIONING AND EVOLUTION OF THE SMALL CPU AND SYSTEMS FAMILY



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SUMMARY OF SMALL SYSTEMS AND TERMINALS
FY80 PROGRAM - (SEE GLOSSARY FOR DEFINITIONS)

CATEGORY	FY80 PROJECT	FCS	$K	FY81 PROJECT	FCS	$K
				T-11	Q3FY80	800
Support	F-11	Q3FY79	600	F-11	Q3FY79	300
	11/23, 11/03		224	11T23P, 11V23P	Q1FY81e	
	11T23, 11V23	FY79	Incl. above	DRV11-J	Q2FY80	
	VT100	Q4FY78	400	VT101	Q1FY81e	
	PDT11/110, 130	Q4FY79		VT131	Q1FY81e	
	VT162	Q4FY80		VT125	Q1FY81e	1100
	LA34, LA36	Q1FY79		LA24	Q2FY81e	
	LA120	Q1FY79	850	LA34V	Q1FY81e	1000
	LP25	Q2FY80		LP26	Q2FY81e	
Central Development	T-11	Q3FY80	1200	J-11 (LSI-11/70)	FY83e	2000
	2-mode PAX/CIS CPU Module Set	Q1FY81e	539	BI/NI	FY83e	500
	KMV11	Q1FY81e	210	PDT11/15	Q4FY81e	350
	11T23P, 11V23P	Q1FY81e	Incl. above	8 Line Asynch	Q2FY81e	100
	DRV11-J	Q2FY80	29	VT211	FY82e	700
	VT125	Q1FY81e	167	VT225	FY82e	
	VT100 (Printer Port)	Q3FY80	168	LA24	Q2FY81e	360
	VT200	FY82e	245			
	LP26	FY81e	250	LA34G	Q1FY81e	20
	LA24(HRDM)	Q2FY81e	800	LA12	Q1FY81e	1500
	LA34V (Graphic Prntr.)	Q1FY81e	62	LA200	Q2FY82e	1900
	LA200	Q2FY82e	1100	LP26	FY81e	275
	LA12	Q1FY81e	1100			
	LA34	FY79	100			
P/L Funded Development	VT101, VT131	Q1FY81e	658	VT200	Q4FY82e	1000
	PDT11/123		400			
	VK-100	Q1FY81e	523			
	VT278	Q1FY81e	1009			
	VT132	Q1FY80				
	VT162	Q1FY80				
Advanced Development	J-11(LSI-11/70)	FY83	1150	uVAX	FY85-FY86	1400
	uVAX	FY85-FY86	650	A/D Chips Misc.		300
	A/D Chips Misc.		100			
	BI/NI	FY83e	270	New Print Techniques		800
	PDT11/15	FY81e	60			
	VT200	FY82e		Integral Hard Copy		450
	VT225	FY82e				
	VT211	FY82e	440			
	New Print Techniques	FY82+	538	Other Video R&D		455
	VT378(P/L Funded)		497			
	Integral Hard Copy		100			
	Other video R&D incl.					

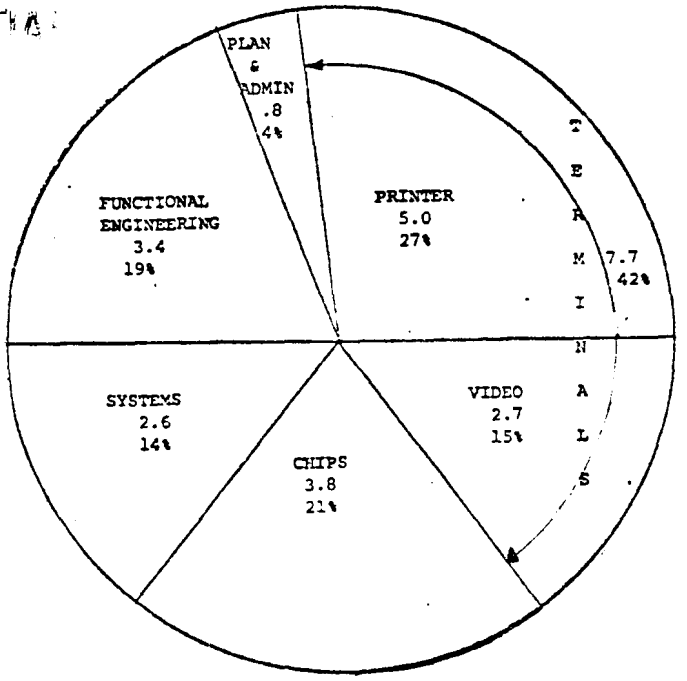
NOTE: 1. The previous designation for LA34-V was LA34G and for KMV11 was Intelligent Comm. 2. VT101 and VT131 were previously designated as the VT100L and VT132L.

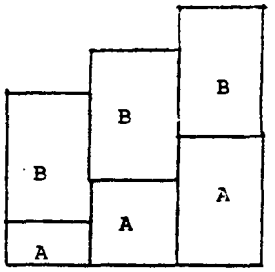
CATEGORY	FY80 PROJECT	FCS	$K	FY81 PROJECT	FCS	$K
Related Central & P/L Developments & Support	TU58		100	AZTEC (?)		
	RL02		514	RL04 (?)		
	RX02		260	QDA (?)		
	RX03		950			
	AZTEC (?)		1530			
	RT11 (V4)	Q3FY80	715			
	Terminals SW (Incl. FMS-11V2)	FY80	1040			
	SSC/PASCAL (formerly MICROS/PASCAL)	FY80	715			
	BASIC-11/ MACRO-11		195			
	ROM BASIC		195			
	MICRO ISAM	FY80	195			
	Fixed Function Terminal		150			
	Shoe Box RT		65			
	T-11		65			
	VT211 Firmware		65			
	O/S78		146			
	RT8/8		81			
	OS/8		81			
	8/11		65			
Not Included	Dual Height F-11 CPU with CIS/PAX		3500			
	QDA		262			
	TU5800		800			
	TS04 Q-bus		200			
	Dual Height F-11 CPU with CIS (no PAX hooks)		400			
			600			
	$500 cost PDT		1000			
	SW for 2-mode PAX for RSTS-E and RSX-11M		130			

*From CSD VT211 budget

COMPUTER SYSTEMS DEVELOPMENT - FUNDING PER ORGANIZATION

FY'79 - FY'81
($ MILLIONS)

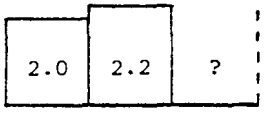




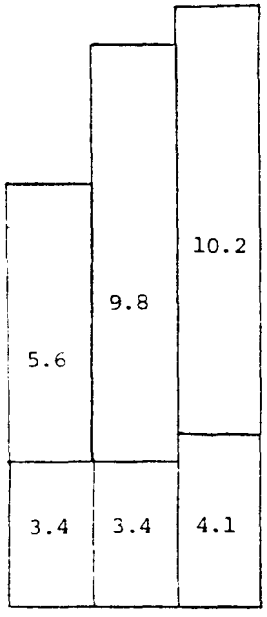
A = OOD FUNDING
B = NON OOD FUNDING

FY80 OOD SPENDING DISTRIBUTION IN CSD

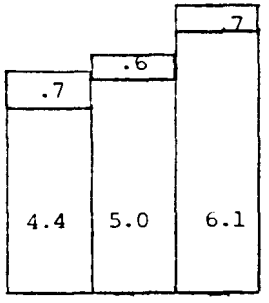
* = INCLUDES .2M FOR MECHANICAL ENG. IN FY80 & FY81



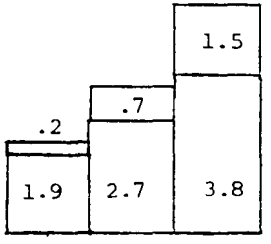
8 - SYSTEMS
(P/L FUNDED)



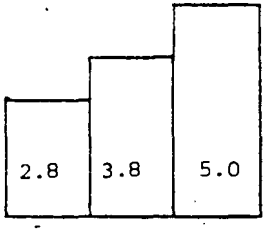
FUNCTIONAL ENGINEERING



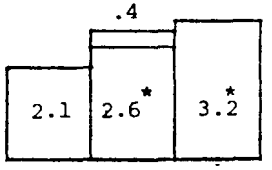
PRINTERS



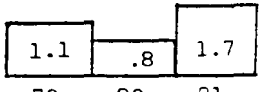
VIDEO



CHIPS

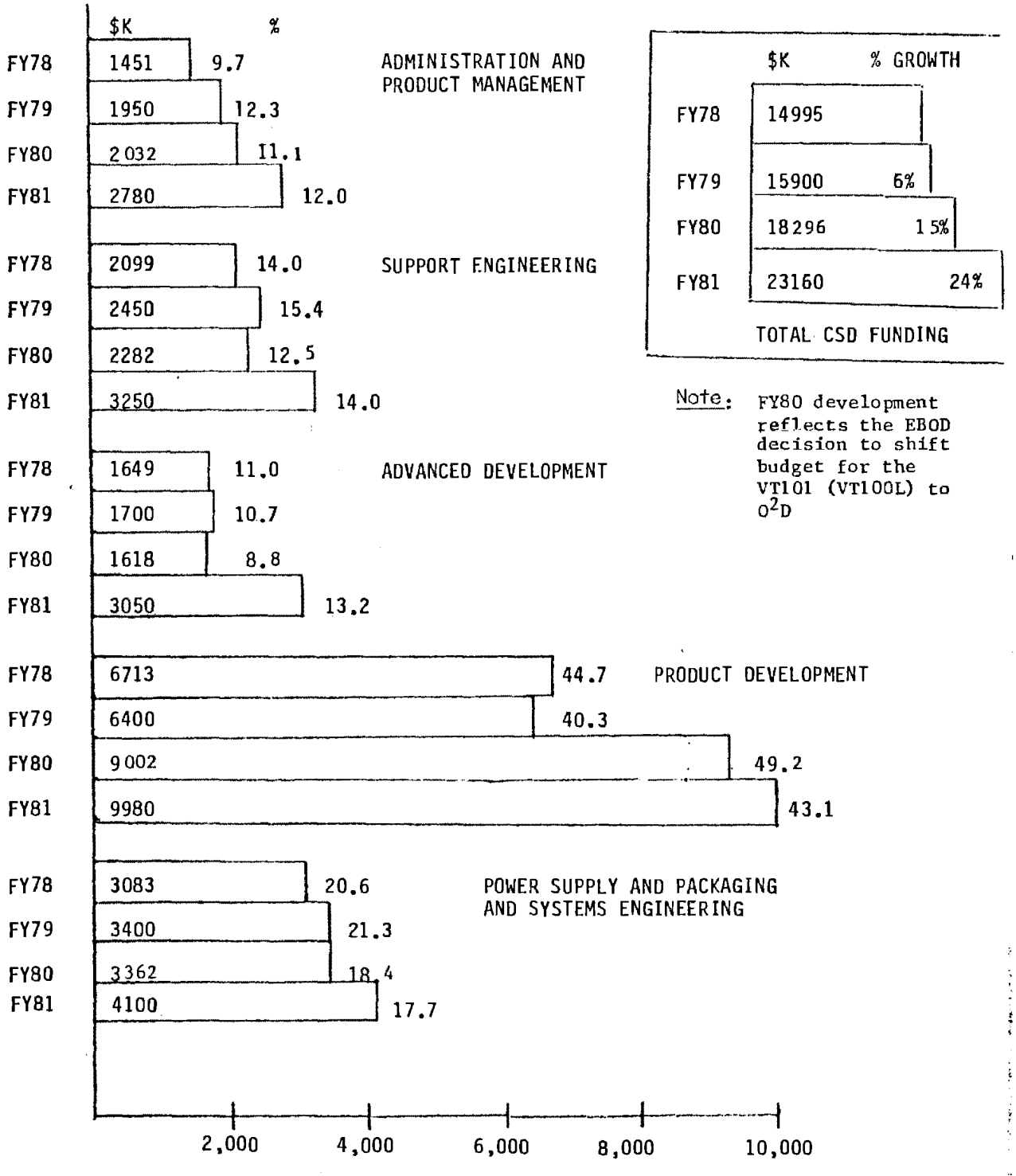


11 - SYSTEMS



PRODUCT PLANNING AND ADMINISTRATION

CSD CENTRALLY FUNDED SPENDING
BY ACTIVITY
(THOUSANDS $)



	$K	% GROWTH
FY78	14995	
FY79	15900	6%
FY80	18296	15%
FY81	23160	24%

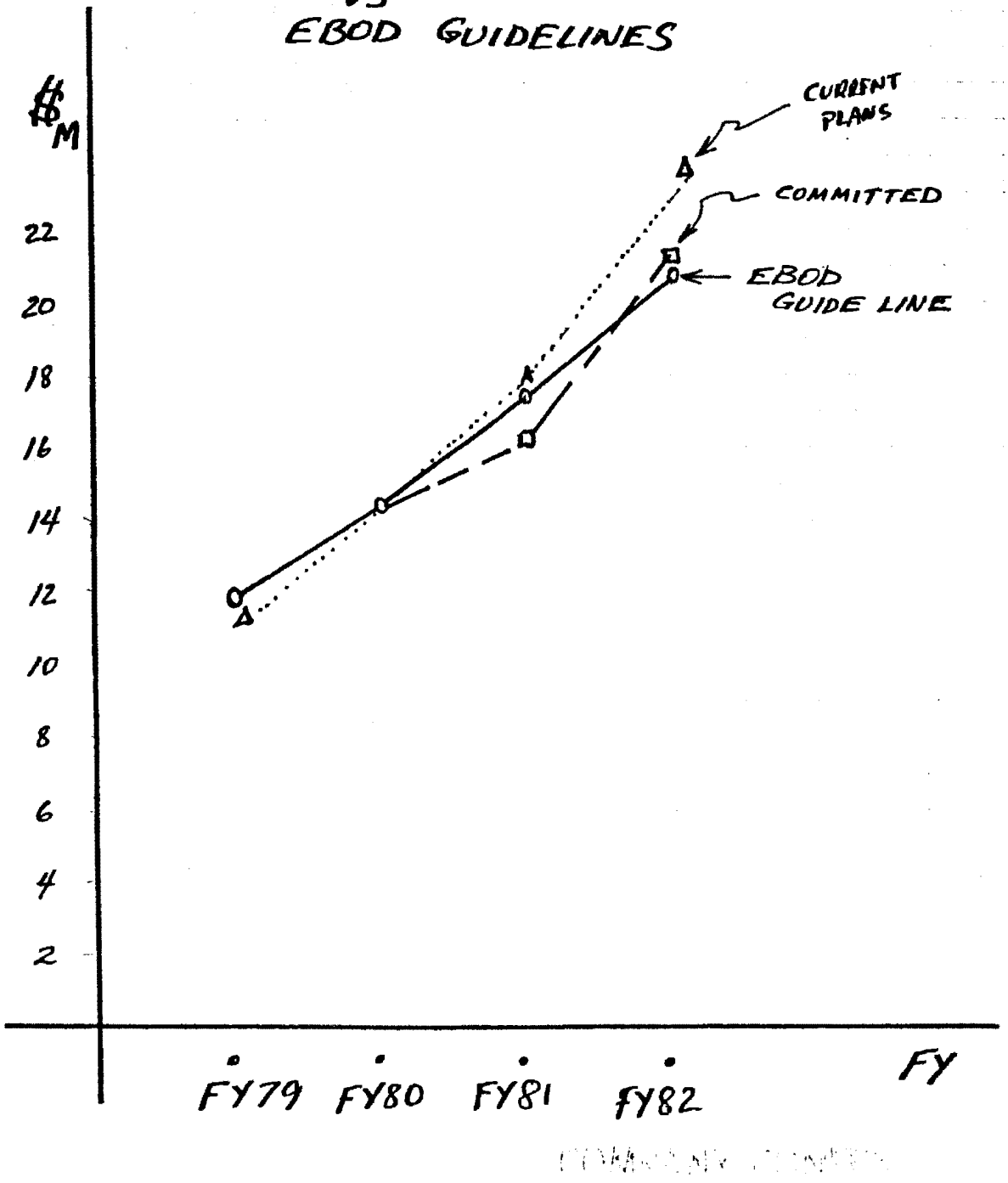
TOTAL CSD FUNDING

Note: FY80 development reflects the EBOD decision to shift budget for the VT101 (VT100L) to O^2D

SNAP SHOT OF FY79 THRU FY82
O^2D + P/L
SMALL SYSTEMS/TERMINALS
MAJOR PROGRAM SPENDING IN CSD

MAJOR PROGRAMS	$M FY 79	80	81	82
TOTAL SUPPORT	2.5	2.3	3.3	3.6 - 4.3
VAX	--	.7	1.4	3.5
LSI 11/70	--	1.2	2.1	2.0 - 3.0
FONZ	1.2	.6	.3	--
T-11	.7	1.2	.5	--
R/S Q-BUS PACKAGES	.2?	.2	.2	--
Q-BUS MODULES CPU, PAX, CIS COMM, MEMORY	.6?	.8	.3	--
BOUNDED SM PDT'S, ETC.	?	.05	.5	1.0
BI/NI	--	.3	.8	1.5
VT100, PDT11/110, 130	1.3			
VT211	--	.44	.7	1.5
ARCH/GRAPHICS	?	.3	.3	1.0
VT125	.2	.167	.15	--
VT101, 131	.1	.7 (P/L)	--	--
VT200	--	.250	1.000(P/L)	2.5(P/L)
LA12	--	1.1	1.5	1.0 - 1.7
LA200	--	1.1	1.9	.9 - 1.0
LA120, 34, 38, 24	2.0?	.8	.4	--
LP	.2	.3	.3	.3
PDP8 (ALL PROJECTS)	1.5(P/L)	2.2(P/L)	.5(P/L)	?
TOTAL MAJOR PROGRAMS (O^2D + P/L)	10.5?	14.7	16.2	18.8 - 21.3

CSD SMALL SYSTEMS & TERMINALS COMMITTED & PLANNED FUNDS TO BE SPENT BY O²D VS EBOD GUIDELINES



NOTE: THE COMMITTED PROGRAM IN FY80 & FY 81 ASSUMES NO GROWTH IN ADMN OR R&D

I. SYSTEMS

Systems Segment Objectives

- o Emphasize the planning and integration of market-related software/hardware packages
- o Couple to aggressive P/L's who can identify their target packages and market characteristics
- o Develop and integrate an LSI-VAX into our market-related packages by FY85-FY86
- o Enhance the Fonz systems capability to address 4MB by FY81
- o Provide a full range of boards, boxes and systems by FY83 based on:
  1. LSI-11/70 Chip Set
  2. A new backplane interconnect and network interconnect (BI/NI)
  3. Merge of Q-bus and Unibus structures into the BI/NI architecture
- o Continue the concept of modular packaging for small systems
- o Introduce highly integrated very small systems using the T-11 processor in FY81. Move towards highly integrated terminal like products with systems like functionality and programmability
- o Provide engineering support for P/L investments in our PDP8 family

Systems Product Tactics

Support FY80

11V23	Q-bus system, 256KB max., RX02, 30" cabinet (support in FY80)
11T23	Q-bus system, 256KB max., RL01, 40" cabinet (support in FY80)

New Development FY80

BI/NI	A new architectures I/O bus for future peripherals and ease of drop ship connection to a system product (Advanced Development in FY80). This interconnect will be used in place of the Q-bus PAX implementation if, by September, the design proves to be a feasible alternative.
Extended memory for small systems	CPU contains hooks for 22-bit addressing, kernal and user mode, but with only I space. CPU also contains CIS, KW11-L, DL11, boot on a quad form factor. 2nd board (quad) contains I/O map logic and memory drive. This new CPU will work with a Q-bus only backplane for $\leq$ 256KB configurations (see rationale, Appendix)
*128KB dual memory array	Use of the 16K chip on a dual (FY80) with parity for use with parity for use with 2-mode PAX CPU. (Not for Q-bus use. Comparable Q-bus memory is the MSV11-J, H)
11T23P	11T23 type system approx. 2MB addressing, RL02, includes the KDF11-P quad module using F-11 CPU supporting 4MB addressing

*Additions since February 1979

TERMINALS/SMALL SYSTEMS STRATEGIC FOCUS

I. SYSTEMS (continued)

New Development FY80 (continued)

KMV-11 Intelligent Comm.	Synchronous communications interface for the Q-bus, F-11 based intelligence contains 2 ports at 19.2KB

P/L Funded Development FY80

*PDT11/123	VT100 + 4x4 Q-bus backplane + Fonz-11 CPU follow-on from PDT 11/150, includes PDT11/150 style product with Fonz CPU, Q-bus internal, RX03, dual boot, down line loader and/or bootstrap. (Funding from Commercial Group expected - $400K)
VT278	Single user Small Business System PDP8 based. Runs Word Processing and DIBS applicatons software

New Development FY81

*512KB dual memory array	Use of the 64K chip on a dual high module (FY81) with parity for use with 2-mode PAX CPU. Use of ECS error correction functions need to be determined. Not for Q-bus use. Comparable Q-bus memory is the MSV11-?-256KB)
*Async. Comm.	8-line asynch. serial line interface (P/L funded)
PDT11/15	System based on the T-11 chip ($350K funding in FY81 by CSD)

Future Development Targets

*11T73	A hard disk based system based on the J-11 chip set. This project begins with the BI and NI interconnects
VAX11/730	uVAX system product

*Additions since February 1979

Engineering Manager
John Clarke

CSD SYSTEMS GROUP

Major Strategic Elements:

- o Emphasize the planning and integration of market-related software/hardware packages. Get P/L's to identify target packages.
- o Develop and integrate an LSI-VAX into our market-related packages by FY85-FY86.
- o Enhance the Fonz systems capability to address 4MB by FY81 and full 11/44 compatibility by FY83.
- o Emphasize use of modular components rather than development of point products.
- o Use packaging and lower cost mass storage to lower entry package pricing.

Systems Strategy

A major development in our systems strategy is the intent of CSD to develop a range of cost effective integrated hardware systems to satisfy the common requirements across OEM and End User Product LInes. These hardware packages will satisfy the need of program development and/or production run time market needs, with added value to be supplied by OEM's or the End User Product Lines.

The CSD systems level design function will address the issue of optimum configuration forecast/planning and, in particular, the following tradeoffs:

a. Functionality vs. Performance
b. Cost of ownership vs. Product Cost
c. Modularity vs. Manufacturability
d. Ergenomics vs. Cost
e. Extensibility vs. Product Cost

While conventional wisdom may suggest certain design relationships, the underlying assumption of this intended effort is to analyze needs based on a pro-active interaction with P/L's and understanding of end use. The development of applications solutions in CSD is a NON goal except as sponsored by a product line.

Exclude

- o PDP-11/110 and PDT-11/130 replacements with 0^2D funds.

Dependency

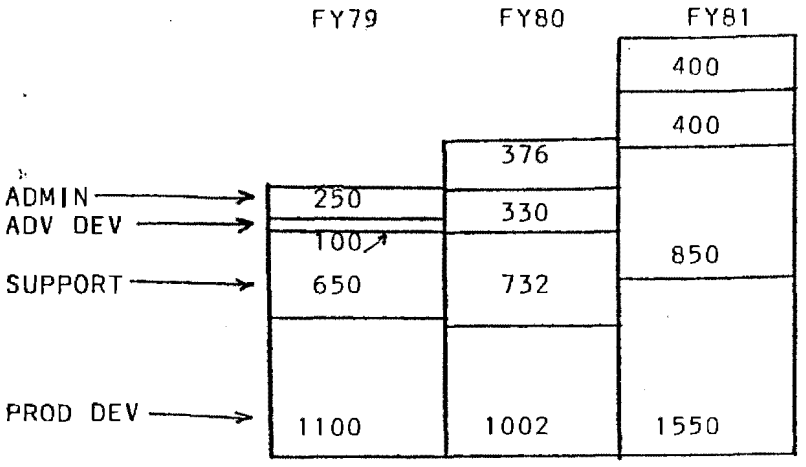
- o Product Line funding to do fast floating point FPF-11; for the F-11.
- o Driver software to support O/S beyond RT-11.
- o Low cost disk products (RX03, AZTEC, Qbus adaptor), tapes for small systems.

New Tactical Elements

- o Begin the design of a new low end I/O architecture in advanced development, 1) match the design of smart controllers in future peripherals, 2) facilitate drop ship goals through use of external connectors.
- o Release a PDT-11/150 replacement product using RX03, Qbus and KDF11-V.

Major Risks

- o Software support for operating systems capable of being run on the F-11 based small systems.
- o Disk products matching the small systems need.
- o Market driven definitions of kernal configurations.



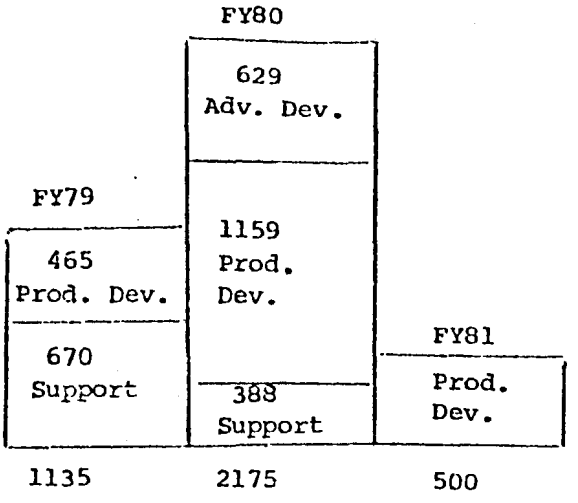
TOTAL OOD	2100	2440	3200
P/L FUNDED	----	400	----
MECH. ENG.	----	200	200

MAJOR PROGRAMS	FY80 OOD	FY80 P/L	FY81 OOD	FY81 P/L
Packaged, Floor Mounted R/S Sys 11V23 & 11T23 (2-mode PAX in FY81)	224		200	
CPU and I/O map modules for R/S Sys. with 2-mode PAX.	439			
Memory Array with 16K/64K chip 64KW/256KW double high board	100		150	
PDT11/123, PDP11/150 follow-on using Q-Bus internals & RX02		400		
Intelligent communications	210			
Asynchronous Communications			100	
PDT 11/15			350	
New I/O Low End Bus, BI/NI interconnect			500	
DRV-11J block mode multi-drop	29			
R80/RL04 Mass Storage Interface			250	
Adv. Dev. (BI/NI & PDT11/15)	330		400	
Support	732		850	
Administration	376		400	
	2,440	400	3,200	
Mechanical Engineering	200		200	

PDP-8

PRODUCT LINE FUNDING

(THOUSANDS $)



PROGRAM SUMMARY

	BUDGET $K	
	FY80	FY81
Omnibus Support	268	-0-
VT78 Support	120	-0-
H6120	150	-0-
VT278	1009	500
VT278 Adv. Dev.	497	-0-
H6120 Decwriter Adv. Dev.	131	-0-
	2175	500

II. VIDEO TERMINALS

Video Terminals Segment Objectives

- o Build on the VT100 modularity base
- o Add functionality in graphics, editing, color, resolution, programmability, and the features for multipdrop block mode communications
- o Couple with leadership P/L for lower entry level system targets

Video Terminals Product Tactics

Support FY80

Video	VT100, VT162, PDT11/110, PDT11/130

New Developments FY80

VT100 Options	Printer Port
VT125	VT100 plus graphics, runs REGIS protocol or alternative firmware based protocol (e.g., VT105, Tektronix 4010, etc.)
VT211	Full functionality video terminal (i.e., block mode, multidrop) plus programmable extension capabilities all at cost equal to the VT100 (Advanced Development in FY80)
VT200	Super low cost VT100 (1/3 cost of VT100)

P/L Funded FY80

VT100L	Low cost VT100 (partially funded by CSD) (60% VT100 cost)
VT132L	Block mode editing version of VT100L
VT132	Editing version of the VT100 (DCG funded)
VK100 Terminal	Bit mapped graphics control in a keyboard drive external B/W or color monitor (VK100 - ECS funded) uses an 8085 uP. Runs a REGIS protocol.
VT162	Block mode fixed functionality terminal for TRAX. Uses Fonz CPU, 16K "user space" + 12K ROM (Commercial Group funded)

New Developments FY81

VT225	Color version of the VT125
VT266	High resolution functionality variation of the VT211

VIDEO TERMINALS

Engineering Manage
Len Halio

Strategy

- Build on the VT100 modularity base
- Add functionality in graphics, editing, color, resolution programmability and the features for multidrop-block mode communication
- Follow P/L leadership and funding for lower entry level pricing (VT101, VT200). NOTE: A June EBOD decision has been made to transfer P/L funding to Central Engineering that will cause the VT101 to be focused as a corporate product.

Excluded

- Toby
- Specialized keyboards
- Support external modification of VT100 microcode
- Fund second sources for VT100 chips, tools, testers (Manufacturing should take action)

Dependencies

- Product line funding FY1980 723K; FY1981 1500K (est.)
- VT100 host system software
- Modem development
- Printer mechanism

Competition

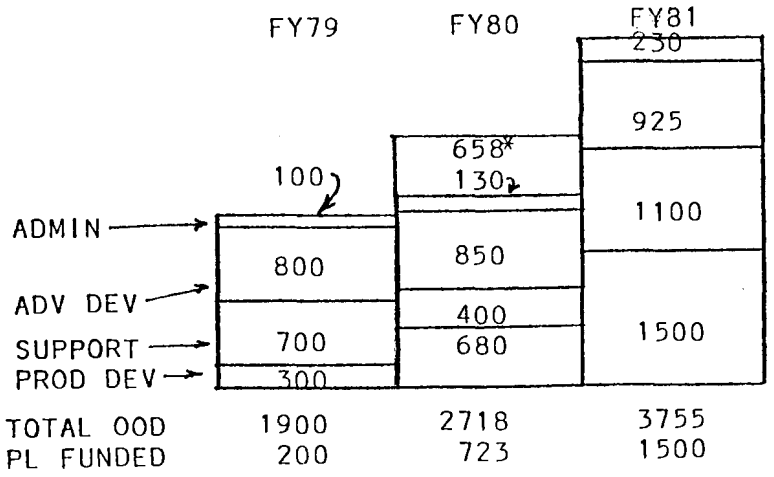
- Dumb/Smart CRT's - Lear Siegler, Hazeltine H.P.
  Applied Digital Data Systems, IBM
- Non Intelligent Terminals - ADDS Ann Arbor, BeeHive, Data General Hazeltine, H.P., IBM, Infotron, Lear Siegler, Perkin-Elmer, Teletype
- Price trend DEC - VT05 $2800, VT52 $2000, VT100 $1900, VT100L $1085 (1/80), VT200 $600 (1/81)
- Market grows at approximately 21% a year

Key Issues, Risk

- Need low cost continuous manufacturing process. Labor cost key issue in future cost of manufacture
- Pressure in the marketplace to lower cost of ownernship
- The future trend is towards less cost erosion and increased functionality
- Risk of consumer t.v. manufacturer entering very low cost video terminal
- Very high uncertainty of market demand leading to large upside ship potential. This creates the need for second source material strategies, larger inventory build plans.

Financial 79-81

OOD FUNDING (Thousands $)



* VT101 (VT100L) added to OOD from P/L funding

(Thousands $)

Program Summary	FY80 OOD	FY80 P/L	FY81 OOD	FY81 P/L
Product Development				
VT100 (Printer Port)	168			
Graphic Architecture	100		250	
VT125 Graphic terminal	167	200	150	
VT101, VT131 Low cost	658			300
VT200	245			1,000
VT211			700	
Uncommitted			400	
VK100 (Educational terminal)		523		200
	1338K	723K	1,500K	1,500

(Thousands $)

Advanced Development	FY80 OOD	FY80 P/L	FY81 OOD	FY81 P/L
Color, high resolution and other video techniques	200		275	
VT211 Programmable terminal	440			
R&D flow through	110		200	
Integral graphic hard copy	100		450	
Uncommitted				
	850K	-0-	925K	-0-
Support	400		1,100	
Administration	130		230	
TOTAL	2,718K	723K	3,755K	1,500K

TERMINALS/SMALL SYSTEMS STRATEGIC FOCUS

III. PRINTING TERMINALS

Printing Terminals Objectives

- o Deliver a high resolution DOT MATRIX input terminal in FY81
- o Increase functionality including multidrop block mode and graphics to our terminals products
- o Open new markets with a low priced personal portable terminal
- o Explore, via Advanced Development, letter quality and new printing technologies

Printing Terminals Product Tactics

Support FY80

Printing Terminals	LA34, LA38, LA120
LP25	300 line per minute band printer, 25% lower cost than LP05

New Developments FY80

LP26	600 line per minute band printer
LA12	Personal portable terminal at 30 cps
LA200	Family of 1200 baud terminals Full functionality (i.e., block mode - multidrop) terminal at 200 cps. LA120 follow-on + additional features.
LA24 (HRDM)	High resolution dot matrix approximately 200 cps
LA34G	Low speed graphics printer, graphics version of the LA34

PRINTING TERMINALS/LINE PRINTERS

Strategy

- Build on impact dot matrix technology. Add multi drop block mode and graphics functionality to line of printing terminals product
- Do a high resolution dot matrix printing terminal; LA24
- Introduce new, lower cost 300 LPM printer (LP25); add corporate 600 LPM printer (LP26)
- Open new markets with personal portable terminal; LA12

Excluded

- Video options (available for product line funding 400K) provides CRT functionality to a printing terminal

Dependencies

- Communication hardware
- Software, operating systems support

Competition

Line printers, Mainframe manufacturers, minicomputer and small business systems, and independent printer manufacturers - Data Products, G. E., Centronics, DataPrinter

Terminals, Many small suppliers, but domination by few large ones (T.I., TTY, IBM, DEC, ITT, Siemans)

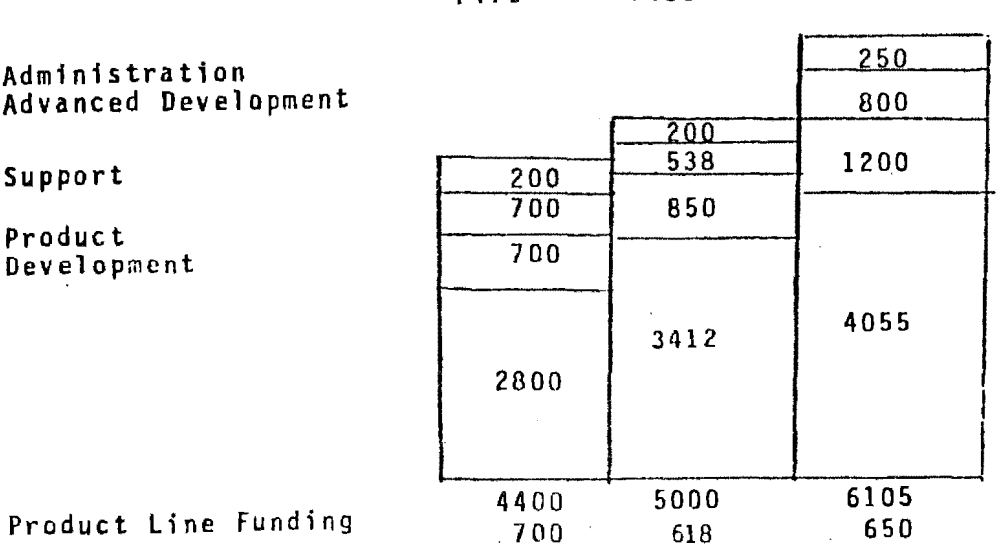
Key Issues, Risk

- What is manufacturing strategy for very high volumes/lower possible cost, i.e., do we build in Far East, etc.?
- Can we develop multiple products from same development effort? (i.e., build one basic terminal with graphics, communications, high quality print, etc., as family members)
- Can we open new markets/channels of distribution to fuel growth? (e.g., personal portable market)
- Can we minimize/eliminate impact of parasite "system houses" supplying line printers for our systems

PRINTERS, TERMINALS/LINE PRINTERS

Financial 79-81

OOD FUNDING (Thousands $)



Program Summary

	BUDGET FY80	FY81
LA34	100	-
LA12	1,100	1,500
LA200	1,100	1,900
LA34G (Graphic Printer)	62	20
LA24 (HRDM)	800	360
Video Option	-	-
Line Printer	250	275
Adv. Dev.	538	800
Support	850	1,000
Eng. & Product Management	200	250
TOTAL OOD FUNDED	5,000	6,105
VT162	260	-
DCG Support	55	150
Manufacturing Support	303	500
TOTAL P/L	618	650
TOTAL OOD & P/L	5,618	6,755

IV. CHIPS

Chips Segment Objectives

- o Begin the advanced development for a VLSI-VAX kernal by FY85-FY86
- o Complete the T-11 for use as an 11 ISP CPU wherever possible as a system microprocessor and/or controller
- o Do an LSI-11/70 for the low end Medium Systems for FY83. Base the system architecture on a new interconnect
- o Strongly influence the development of good design tools
- o Strongly influence the use of 11 ISP architecture everywhere possible, (i.e., controllers, microprocessor options, point systems, etc.)

Chips Product Tactics

Support

F-11	Fonz-11 multi-chip CPU, 11/34 performance 256KB addressing limit

New Developments FY80

T-11	Single chip LSI-11 using NMOS, 11/34 performance 64KB addressing limit
*J-11	Multi chip CPU with 11/70 functionality and performance also known as the L70 or the LSI-11/70
uVAX	LSI VAX chipset

*Additions since February 1979

CSD SEMICONDUCTOR LSI CHIP DEVELOPMENT

Mike Titelbaum
2/18/79

Strategy Elements

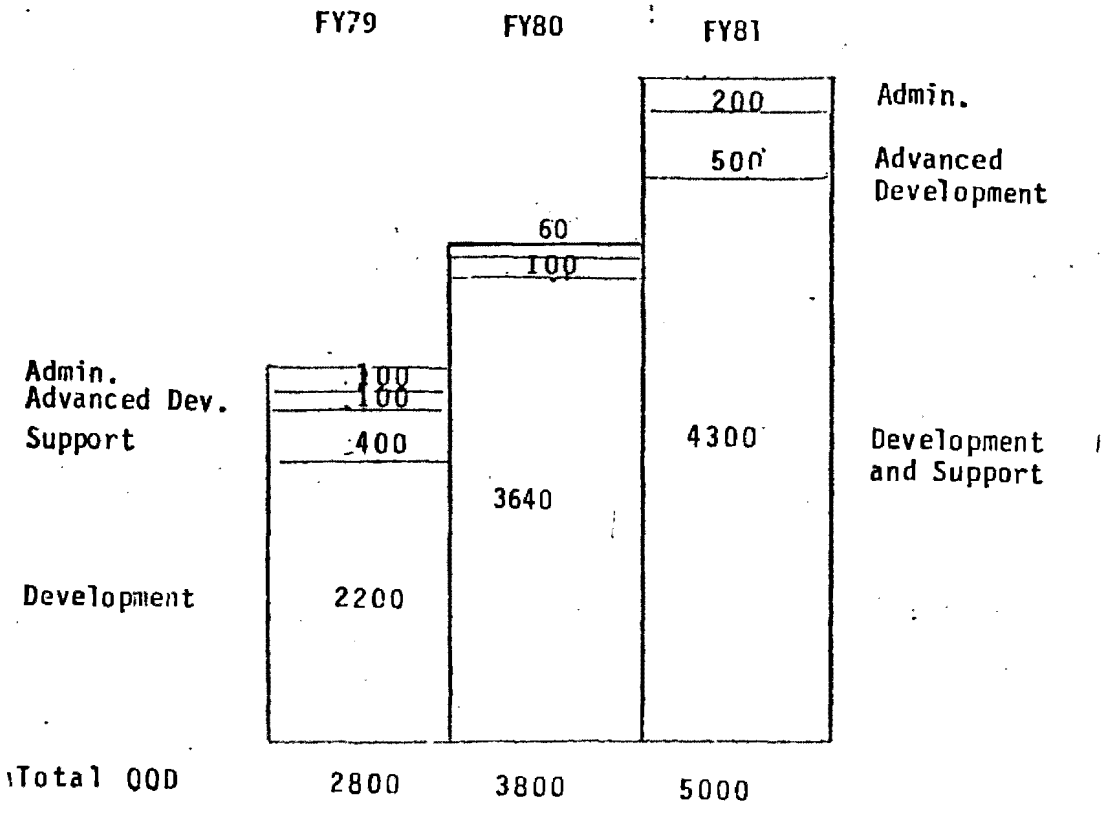
- Do not invest in extending the base FONZ chip set functionality to complete 11/44 functionality, but do an I/O map module in the systems segment to provide only 2-mode PAXed FONZ systems.
- Provide factory and user support of existing FONZ set.
- Invest in a new LSI chip set to provide 11/70(74) performance and functionality for low end and mid-range systems for FY83 and beyond.
- Begin advanced development on LSI VAX chips in the Technology, Design Process and Tools in FY80.
- Complete T-11 chip development and provide user and applications level support for DEC System and Controller products. Evaluate the T-11 follow on. This probably implies integrating more system functions on the base CPU chip or developing other systems chips to support the use of the T-11 in systems packages and/or controllers.

Assumptions, Risks and Implications

- 11/70 CPU performance is required to support PDP-11 FY83 and beyond system performance (KIPS, I/O and Users) that extended FONZ (44 functionality) cannot - ASSUMPTION
- The LSI 11/70 program requires approximately $3-4MB greater development cost over 4 year program life than extending FONZ set - RISK
- It makes sense to do 11/70 class chip set in preparation for LSI VAX set (2 times FONZ complexity for 70 versus 4 times for LSI VAX) - ASSUMPTION
- Doing 11/70 class chip set will de-focus LSI VAX resources for some time (0< <1 year) - RISK

CHIPS FY79-FY81 FINANCIAL DATA

(Thousands $)



Project Funding	$K FY80 OOD	FY80 P/L	FY81E OOD	FY81E P/L
1. uVax Advanced Development	650		1,400	
2. Complete T-11	1240		800	
3. Complete and Support Fonz	600		300	
4. LSI-11/70, J-11	1,150		2,000	
5. Advanced Development	100		300	
6. Administration	60		200	
	3,800	-0-	5,000	-0-

SYSTEMS ENGINEERING

Herb Shanzer 2/9/79

DEFINITION OF RESPONSIBILITIES & STRATEGY

SYSTEM EVALUATION:	- Resolves system integration issues (hardware, peripheral interface, software). - Lead the development of test strategies for release of more complex systems level products to Manufacturing.
SYSTEMS INTERCONNECT:	- Technical expertise and consultation on signal integrity. - Advanced interconnect technology (Fiber Optics). - Coordinate and standardize system interconnect issues.
PERFORMANCE TOOLS AND METHODOLOGIES:	- Modeling and analysis of new product design alternatives prior to start of development. - Development of tools for workload generation and data analysis to assist in product measurement. - Increase tool emphasis on database and distributed systems.
PRODUCT MEASUREMENT:	- Measure performance of developed products-positioning vis-a-vis: competition, current and future products. - Emphasize coordination and support of corporate product measurement activites.
MANUFACTURING SUPPORT:	- Assist system manufacturing in isolating strategic problems and coordinate with cognizant engineering groups for solution. - Major projects are coordinated test and release process (SPT) and systems level dock merge.
PACKAGED SYSTEMS:	- Integration, documentation and release to manufacturing of corporate Packaged Systems. - Transfer function to design groups as generic cross-systems issued are resolved.
MECHANICAL SYSTEMS ENGINEERING:	- Supports Packaged Systems and development groups focusing on cabling, cooling and mechanical integration. - Migrated to development groups with Packaged Systems.

KEY ISSUES

1. The group's activities are driven by the existence of high quality technical expertise. These people are difficult to find in any case, the changing of charters and goals to track decentralization makes this even harder.

2. We have started building a base of tools for use in Systems Performance Analysis and Systems Evaluation. To date, almost all of our tool funding has gone into development; we now must start a maintenance effort. As our tool base grows, this maintenance effort becomes increasingly significant and a decreasing proportion of our tool funding will be available for new development.

3. Funding for FY80 precludes significant work on performance tools for database and distributed systems, since short term requirements for product positioning are higher priority.

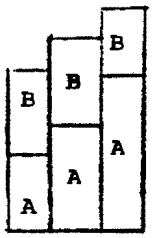
4. Maintaining close central coordination of our decentralized bus development efforts.

5. Maintaining commonality of system mechanical components and packaging techniques as these functions decentralize.

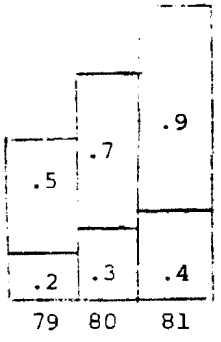
SYSTEMS ENGINEERING -SPENDING PER MAJOR ACTIVITY

FY'79 - FY'81

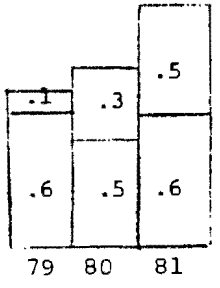
(MILLIONS $)



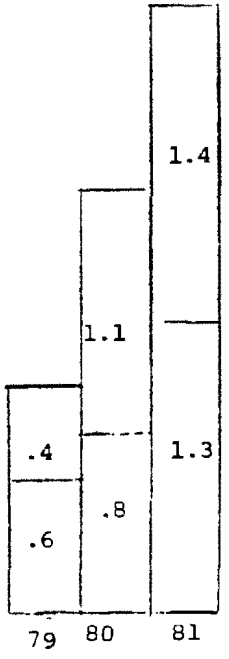
A: CENTRALLY FUNDED
B: EXTERNALLY FUNDED



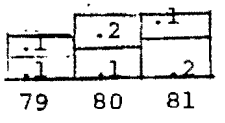
SYSTEMS EVALUATION



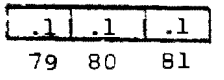
SYSTEMS INTERCONNECT



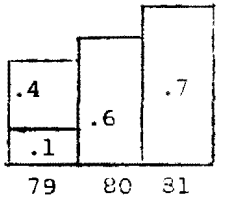
SYSTEMS PERF. ANALYSIS



SYSTEMS INTERGRATION



SYSTEMS ENG ADMINISTRATION (CENTRALLY FUNDED)



PACKAGED SYSTEMS (EXTERNALLY FUNDED 80,81)

COMPANY CONFIDENTIAL

Phil Tays
10 Feb. 79

POWER AND PACKAGING SYSTEMS
RESPONSIBILITIES AND STRATEGY

Power Supply Management

. Product Design

Definition - Design, develop and integrate into manufacturing effective power conditioning and distribution systems.
Strategy - Become part of product team (on site where possible) and obtain secondary or product funding.

. Cross-Product Development and Support

Definition - Integrate broad needs into common families of power products.
Strategy - Design products for consolidated manufacturing process using sharted engineering development funding. Develop support in manufacturing and coordinate plant activities from central engineering.

. Tools, Standards and Advanced Development

Definition - Develop and document common tools, techniques and high technology products to allow effective remote design.
Strategy - Administer central funds to promote technology transfer and reduce risk at product design time.

Central Consulting and Design

. Industrial Design

Definition - Provide consulting and design services for corporate product and graphic design, and act as component engineering for labels.
Strategy - Provide central management for and coordinate development of Digital's product families' image and human factors.

. Electrical and Mechanical Consulting, Tools, Standards and Advanced Development

Definition - Provide high-technology consulting, development tools, and standards or guidelines together within coordinated advanced development of new technology for mechanical design.
Strategy - Maintain and expand high-technology expertise, consulting and testing to provide effective pay-as-you-go service to product designers.

. Mechanical Packaging Design and Support

Definition - Provide effective cabinets, enclosures and mechanical design services to central groups or wide base of users.
Strategy - Centrally drive cross-product design and provide effective coordination with manufacturing and field service, and support high volume common mechanical products.

. Hardware Design Assurance

Definition - Insure electromagnetic compatibility and electrical integrity of Digital products, monitor and interpret international requirements.
Strategy - Coordinate Digital hardware standards and monitor or influence external requirements.

Phil Tays
10 Feb. 79

POWER AND PACKAGING SYSTEMS

Key Issues

1. I am concerned about manufacturing's ability to provide technical expertise, assembly and test consolidation, and funding to support mature high volume power supplies.

2. The decentralization of power supply engineering is diluting a very scarce resource - our high technology design team. The central/site roles will depend heavily on our ability to staff both at the individual contributor and management level.

3. The role clarification for the central and site activities seems unusally difficult with much activity subject to shift as the use of central funding becomes clear.

4. We are continuing to emphasize "defensive engineering" where tradeoffs are made in favor of flexibility and generally unbounded products. We need more central emphasis on the efficient use of corporate resources, standards and guidelines, and consolidation of common high-volume manufacturing.

5. We need to find alternate funding sources for advanced development and high technology consulting projects to aggressively minimize high risk areas before we start product specific design.

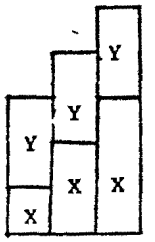
6. Decentralization will require a greatly expanded coordination effort at a time when central funding is being reduced. We need to establish clear guidelines for tradeoffs among cross-products development and support, high-technology advanced development, and coordination of the engineering process and site activities.

POWER & PACKAGING SYSTEMS
SPENDING PER COST CENTER

(A) FY79 INCLUDES TWKS

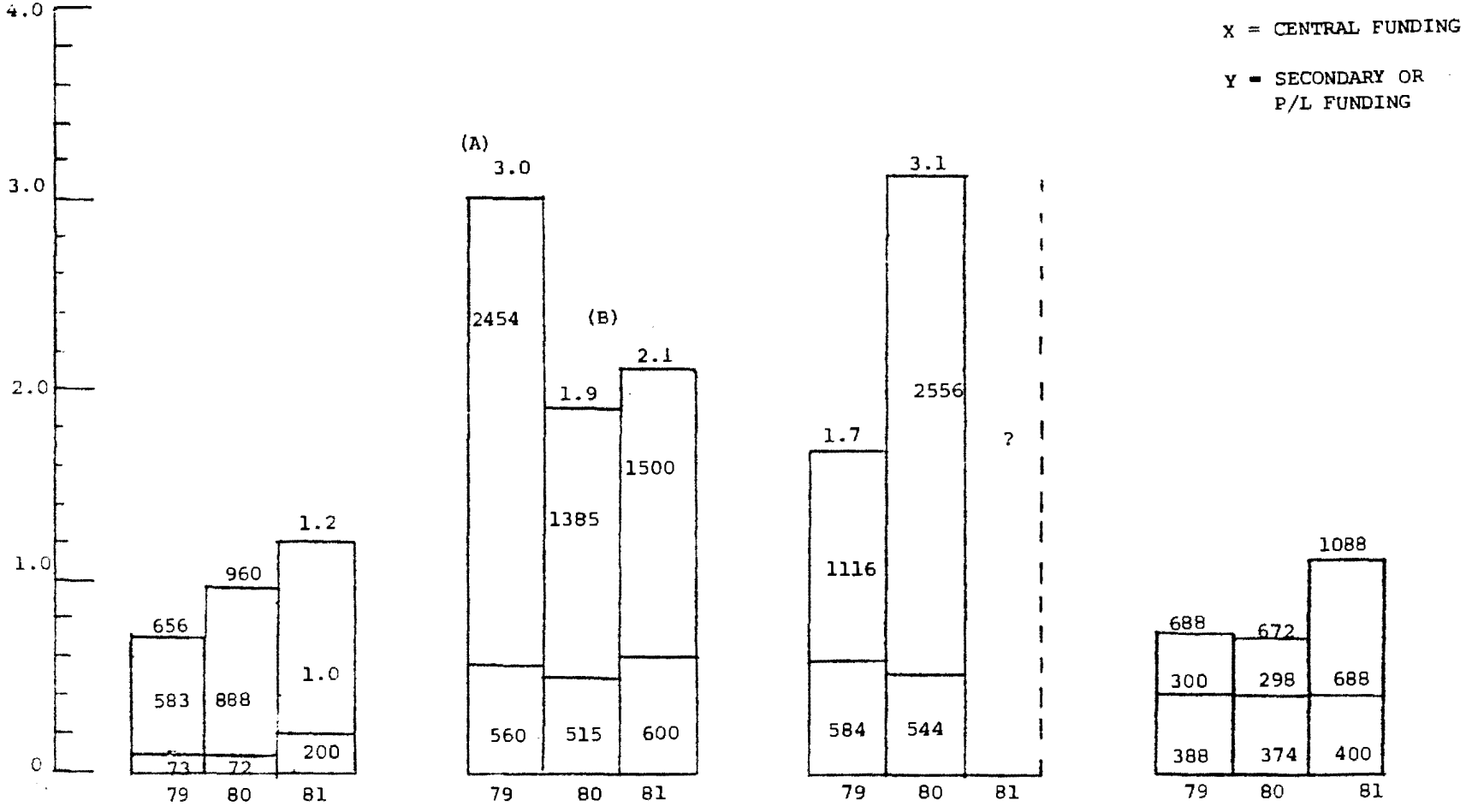
(B) FY80 DOES NOT INCLUDE TWKS

(C) FY80 NEW ORG CONSISTS OF
CENTRAL MECH, INDUSTRIAL PKG.
INTERCONNECTION DEV, ENVIRONMENTAL



X = CENTRAL FUNDING

Y = SECONDARY OR
P/L FUNDING



ADMINISTRATION

Personnel

- Strengthen CSD through a series of organizational development plans
- Implement an effective employee relations program
- Install consistent performance appraisal techniques across all CSD groups
- Provide an effective human resource plan to meet the needs generated by CSD growth plans

Finance/Control

- Charter for providing management with the tools whereby they can control the performance of their business
- Given the charter stated above, the strategy will be to decentralize the control function down to the level where the decisions are made
- Finance will develop the necessary organization and tools to give to the manager:
  - Quality data
  - Rapid feedback
  - Assistance in decision making and priority setting

Planning and Product Management

- Develop the planning and review processes, manage the processes
- Manage the product through its life cycle
- Develop and communicate technology position
- Manage the interrelation of CSD with Digital's other functional organizations
- Chairing corporate Research and Development Steering Committee

APPENDIX I

FY80 CHARTER FOR COMPUTER SYSTEMS DEVELOPMENT (Strategic Responsibilities)

Terminals (Support, Product Development, Advanced Development)

- Print
- LPT
- Video

Small Systems

- Integration Planning
- Components (Boards/boxes split 50/50 with DCG)
- Chips to support above systems especially MOS PDP-11 Microprocessors and VAX Microprocessors
- Support of computer store with PDP-8 microprocessor systems

Manage evolution of Terminals to become Small Systems

Packaging and Power Supplies

- Decentralization strategy (Including central nucleus and process management for corporate integration)
  - Power Supplies
  - Industrial Design
  - Mechanical Design
  - Cabinets
  - Shipping Packaging
  - RFI and Safety Standards
  - International Regulations

Systems Engineering (Central nucleus and decentralized strategy)

- System performance modeling and measurement
- Bus maintenance of existing Busses (U, Q and Mass) including new product qualification
- Development and implementation of Systems parameter test concepts PMT at FA&T level (for variable configuration products)

APPENDIX I

CSD FUNCTIONAL ENGINEERING

CHARTERS AND EMPHASIS

SYSTEM ENGINEERING

- o Provides assistance and support to development groups in the design of well integrated, manufacturable systems.

- o Provides corporate leadership in the: development of tools and methodologies for systems analysis and evaluation - development of system test and release processes - coordination and standardization of system interconnect and signal integrity issues.

- o Provide assistance and support in performance analysis and evaluation to development groups, product lines and software support.

- o Major emphases are generic functions rather than related to one product. Concentration will be on activities that require a centralized critical mass of technical expertise and/or resources.

POWER AND PACKAGING SYSTEMS

- o Provides corporate leadership in defining centralized/decentralized roles for electrical and mechanical design groups addressing: power supply and power distribution design, industrial design, high-technology consulting, cross-products power and packaging, hardware design assurance and testing.

- o Provides design assistance on a pay-as-you-go (sub-contract) basis to groups who desire central support for reasons of: critical mass, control of broad (multi-user) design issues, efficiency, technology transfer, and coordination.

- o Emphasis in the central roles for the future will be:

  - Cross-product support and development
  - High technology consulting, development, standards and guidelines and conformance to international regulations
  - Drive to consolidate the power supply and enclosure business
  - Central testing resource and development of common tools
  - Drive to consolidate and coordinate manufacturing effort, and optimize the engineering hardware development processes

APPENDIX II

SYSTEMS MANUFACTURING GOALS

It is the goal of the Small Systems group to optimize the design of the small systems around a kernal package. A corollary goal is to manufacture these kernal systems as high volume products.

Options for these systems will be drop shippable and cables plugged into receptacles on the kernal system.

Field, or customer integration of these options is a goal. FA&T integration is a definite NON goal.

APPENDIX III

Gil Steil
Engineering Manager

FY80 SOFTWARE STRATEGY

The FY80 software strategy is to:

(1) Fully support our established products: RT-11, RSX-11/M, BASIC-11, Fortran IV, Fortran IV+, and FMS-11 on RT-11 (new in FY79).

(2) Make minor enhancements to these products, especially RT-11 and RSX-11/M (the latter will be repackaged and repriced for the low end).

(3) Make a major effort to properly support our terminal products in our software. As a part of this effort, FMS-11 (our new forms capability) will be migrated to RSX-11/M, RSX-11/M+, SCS-11 and VAX/AME.

All the above will be funded by OOD. Additionally, the following products will be available for development with product line funds:

(1) Micros/Pascal (716K): A single product--this package will provide us with competitive, state-of-the-art operating system and higher level language support for fixed function application development on boards and boxes. Completes the support now provided by RSX-11/M and RT-11.

(2) Fixed function terminals (150K): Sample fixed function applications on very low cost hardware. Important for reality testing our hardware plans and our software development tools.

(3) ROM BASIC (195K) and Micro ISAM (195K): A ROMable, interactive, low end BASIC interpreter, and an indexed file capability. Essential to complete our software offering for the high volume, low cost intelligent terminal market.

APPENDIX IV

SUMMARY ON NET/COMM FOR SMALL SYSTEMS AND TERMINALS

Provide a Terminals/Small Systems network strategy for the 1980's that will:

- o Optimize (communications costs, local dialogues, speed, etc.) the connectio of DEC terminals to DEC systems. This should provide the uniqueness ove competitive product offerings and encourage the use of our terminals and smal systems.
- o Optimize the connection of DEC's small systems to IBM. The range of DE terminals will themselves interface to DEC's small systems and not to IBM.
- o Provide the flexibility (standard options, user modifiable, etc.) for DE terminals/small systems to be connected to systems other than DEC.
- o Provide a migration path for DEC customers as the DEC system environment move to message at a time transmission[+] versus character at a time transmission.
- o Investigate the requirements and technology to provide cost effective local connections for small, medium and large numbers of DEC terminals/smal systems.

TERMINAL STRATEGY

- o The connection of DEC terminals to DEC systems should be optimized to provide unique features and benefits that cannot be provided by competitive suppliers.
- o Design terminals so that standard options will optimize connection of DE terminals to public data networks.
- o Provide minimum communications functions necessary to allow terminal flexibility to be of a higher priority than the incremental cost necessary t provide those features.
- o Shift the thrust of our terminal development to provide message leve capabilities (e.g., block mode) and provide a migration path for character mode terminals to behave as message oriented terminals.
- o Provide transparency to user over various communications services (block mode vs. character mode, local vs. remote, etc.).

[+]Sometimes known as block mode, buffered terminal or packet mode.

II-2

LOW END MASS STORAGE
PRIORITIZED PROJECT RECOMMENDATIONS

PRIORITY	ENGR FY80	BUDGET TOTAL	RATIONALE SUMMARY	EXPECTED USER P/L's												
				TOEM	COEM	LDP	DCG	WP	TEL	TVPE	MSG	CSI	ESG	EPG	STORE	
1. RX03	$500K	$900K	- Maintain competitive posture in - Allow entry level multi-user floppy systems - Offer IBM interchange at 1MB level	x	x		x	x							x	
2. Aztec 8" Disk	$1959K	$8M	- Building block product fox mix or match with TU, RX or RL - Permits table top and customer installable multi-user systems in mid 80's - Lowest entry level hard disk - Price/performance leadership product	x	x	x	x	x	x	x	x	x	x	x	x	
3. INCA $500 2MB	$326K	$3.29M	- Low media cost/low cost of ownership - Personal/transportable/fileable storage - Lowest cost disk subsystem for mid-80's - Lowest cost 1 MB software distribution media - Needed to gain parity with floppy trends	x	x		x	x							x	
4. RL04 F+R 84 Mbytes	$3.035M	$8.0M	- Most competitive mid-range disk - R80 removable companion	x	x	x	x	x	x	x	x	x	x	x	x	
5. QDA	$282K	$882K	- Needed to allow R80, RL04	x	x	x			x	x	x	x	x	x		

PRIORITY	FY80	TOTAL	RATIONALE SUMMARY
1. RX03	$500K	$900K	- Maintain competitive posture in - Allow entry level multi-user floppy systems - Offer IBM interchange at 1MB level
2. Aztec 8" Disk	$1959K	$8M	- Building block product fox mix or match with TU, RX or RL - Permits table top and customer installable multi-user systems in mid 80's - Lowest entry level hard disk - Price/performance leadership product
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4. RL04 F+R 84 Mbytes	$3.035M	$8.0M	- Most competitive mid-range disk - R80 removable companion
5. QDA	$282K	$882K	- Needed to allow R80, RL04 attachment to more powerful Q-bus CPU's
6. TU5800	$800K	$2.35M	- Lowest cost archive companion to low end disks - Low cost software distribution of large operating systems (VMS, RSX) - Low cost system interchange
7. Competitive Analysis Ongoing	$300K	-	- Needed to insure independent analysis - Insure timeliners of response
8. R80			- See large systems Mass Storage Rationale

Appendix VI

PROJECTS GLOSSARY

NOTE THAT TRANSFER COSTS AND FCS DATES FOR PRODUCTS WHOSE FCS IS FY81 AND BEYOND SHOULD BE TREATED AS TARGETS AND/OR ESTIMATES

Note: Transfer costs and FCS dates f products whose FCS is FY81 and beyond should be treated as targets and/or estimates

		FCS	Xfer Cost	MLP
Table Top Systems:				
PDT 11/110	VT100 + TIM module set 30 KW max.	Q3 FY79	$2000	$4900
PDT 11/130	VT100 + TIM module set + TU58 30 KW max.	Q3 FY79	$2300	$6000
PDT 11/150	RX01 drive (single or dual) + TIM module set in table top package w/VT100 30KW max.	Q2 FY79	$2600	$8100
PDT 11/15	Uses T-11 as a CPU in place of LSI-11 & 8085 uP's on the TIM board of a PDT11/150 (includes VT100L and floppy disk)	Q4 FY81	$1700	
VT103	VT100 + 4 x 4 Qbus backplane + KD11-HA 28 KW max.	Q1 FY80		
PDT 11/123	VT100 + 4 x 4 Q-Bus backplane + KDF11-AB or new F-11 CPU, 128 KW max. (funded by the commercial P/L), dual RX03	Q3 FY80	$2600	
Bounded Systems:				
VT78	VT-52 + CMOS 8, 16 KW (PDP-8)	Q1 FY78	$2250	
VT278	VT100 + 6120 CPU, 16-32 KW, RX01/RX02 VT278 with RX03	Q3 FY80	$1400 $1600 - $1900	
SBS-11	VT-100L + single board computer using T-11 32 KW	Q4 FY80		
SBS11-X	VT-100L + single board computer using XT-11 128 KW		TBD	
VT378	VT278 with bubble memory + TU58 in place of floppy disk		$1500	

PROJECTS GLOSSARY

Tapes:		FCS	Xfer Cost	MLP
TU58	Block replaceable cartridge tape, 0.25mb/drive	In prod.	$250	$1000
TS04	IBM compatible tape, 45 IPS, 800/1600BPI (FCS on Unibus is Q1 FY80)	Q4 FY80	$3000	$12000
TSV11	Qbus controller for TS04	Q3 FY80	$100	$400 (es
TU5800	Large capacity cartridge tape, 10mb/drive	Q3 FY81	N/A	N/A
Communications:				
DLV11J	Four line non-multiplexed SLU	In prod.	$120	$460
DXV11	Eight line multiplexed SLU (replaces DZV11)	Q4 FY81	$150	$600
DUV11	Low cost bit stuff Q-bus synch interface			
KMV11 (Intelligent Comm.)	2 synchronous 19.2KB communications lines with programmable protocol, includes Level 1 modem controls, F-11 micro processor based. (Assumes compatible drive software by DECnet Software development group.)			

Note: Transfer costs and FCS dates for products whose FCS is FY81 and beyond should be treated as targets and/or estimates

PROJECTS GLOSSARY

Software:		FCS	Xfer Cost	MLP
RT11	Single user real time operating system, 16KW-64KW	In prod.		$2760
RT-11 V4	Stabilized version of RT-11 with updates for PDP-11/12, RX03, RL02, etc. Ability to support a foreground communications task	FY80		
ROM BASIC	A new low end BASIC capable of execution from read-only memory, with the following characteristics: small, fast, commercial features			
MICRO ISAM	2KW resident, supports random and multi-key ISAM support for intelligent terminals with slow mass storage	FY80		
SCC/PASCAL	Standard System Components contains essential operating systems primitives that can be linked with a stand-alone application; PASCAL for use as a higher level language for ease of programming; both for use in a specialized configuration (i.e., sub-system features) and an in-circuit emulation capability	FY80		
RT/RSX Emulator	Ability for RSX-11M to be used for development of applications for RT-11 and PDT's.	FY80		
Small Systems Support	BASIC-11/MACRO-11			
Small Systems Applications	Shoebox-RT, five tailored shoebox systems not requiring mass storage (will use SSC/PASCAL?)			
Small Systems Consultation	T-11 software consultation for the T-11 CPU team. Fixed function terminals--examine five sample applications (for DCG Terminals Group)			

Note: Transfer costs and FCS dates for products whose FCS is FY81 and beyond should be treated as targets and/or estimates

		FCS	Xfer Cost	MLP
Terminals Software	Coordinated software support for DEC's line of terminals			
VT211 Firmware	Firmware support for the T-11 when used in lieu of the 8085 in a terminal			
RSX11M	Multi-user real time operating system, 64KW-512KW	In prod.		$5500
SCS11	Commercial variant of RSX11M, 64KW-128KW	Q3 FY80		$5500
11/34 Unix V6	Multi-user timesharing operating system, developed and used by AT&T, 64KW-128KW	N/A		
IAS	Multi-user timesharing operating system, 128KW-2MW			
RSTS/E	Multi-user timesharing operating system, 128KW-2MW	In prod.		
Unix V7	Multi-user timesharing operating system, developed and used by AT&T, 128KW-2MW	N/A		
RSX11M+	Multiprocessor variant of RSX11M, 128KW-2MW	Q4 FY79		
KSOS	Secure Unix, 128KW-2MW			
MCF	Military Computer Family Architecture			
VMS	VAX Virtual Memory Operating System, 256KW - 8 MW	In Prod.		

Note: Transfer costs and FCS dates for products whos FCS is FY81 and beyond should be treated as targets and/or estimate

PROJECTS GLOSSARY

Disks		FCS	Xfer Cost	MLP
RX02	Double density single side floppy disk, 0.5mb/spindle. (2 drives + controller)	Q2 FY79	$900	$3900
RL02	Double density removable hard disk, 10mb/spindle (2 drives - controller)	Q2 FY80	$2700	$9000
RX03	Double density double sided floppy, 1 0mb/spindle, compatible with RX01, uses RX02 interface	Q1 FY81	$900	$4000
R80	Fixed media four platter Winchester disk, 130mb/spindle (FCS on Unibus is Q4 FY80)	Q3 FY80	$2700 (est)	$10000
QDA	Qbus controller for R80/RL04/R81 (FCS of Unibus versions is current form factor is dual quad boards Q4 FY80)	?	$500 (est)	$2000 (est
RL04	Octal density fixed-plus-removable hard disk 84 mb/spindle	FY82	$2000	$8000
AZTEC	Small hard disk, very low cost, 20-40mb	FY82-FY83	$1300 (est)	$5000 (est
R81	Double or quad density fixed media Winchester disk, 260-520mb/spindle	FY83	N/A	N/A

Note: Transfer costs and FCS dates for products whose FCS is FY81 and beyond should be treated as targets and/or estimates

Video Terminals:		FCS	Xfer Cost	MLP
VT125	Graphics function Video Terminal in a VT100 (P/L funded)	Q1 FY81	$900	
VT225	Color version of VT125	FY82		
VT132	Editing function Video Terminal in a VT100 (DCG funded)	Q1 FY80	$700	
VT101 (was VT100L)	Low Cost VT100 (DCG funded)	Q1 FY81	$350	
VT131 (was VT132L)	VT100L with block mode and editing functionality	Q1 FY81	$450	
VT200	Super Low Cost VT100	Q4 FY82	$200	
VT211	Full functionality Video Terminal with block mode, multidrop) plus programable extension capabilities	Q4 FY81	$600	$2000
VT266	66 line high quality version of VT211	FY83		
EPG(EDU)Terminal (VK100)	Bit mapped graphics control in a keyboard drives an external B/W or color monitor (ECS funded)	Q1 FY81	$350	
VT162	Block mode fixed functionality terminal for TRAX. Uses FONZ CPU, 16K "user space" + 12K ROM (Commercial Group funded)	Q4 FY80	$850	$2500
Printing Terminals:				
LA34/LA38	30 CPS Printing Terminal	Q3 FY79	$470-$570	
LA34-L/LA38-L	Enhancements to LA34/LA38	Q3 FY80		
LA120	1200 Baud terminal	Q2 FY79	$835	

Note: Transfer costs and FCS dates for products whose FCS if FY81 and beyond should be treated as targets and/or estimates.

PROJECTS GLOSSARY

		FCS	Xfer Cost	MLP
LA200	Full functionality (i.e., block mode, multidrop) terminal family at 200 CPS. Replaces LA34/38, LA24, LA120, etc.	Q2FY82 Q2 FY82	$300 (Basic unit)	
LA12	Personal portable terminal 30CPS	Q1 FY82	$200 (Basic unit)	
LQP	Advanced development of a letter quality typewriter terminal, not a planned product	FY 83 (?)	$500	
LA24 (HRDM)	High resolution dot matrix printing terminal	Q2 FY81	$800	
LA34-V	Low speed graphics printer, formerly LA34G	Q1 FY81	$600	
LP25	300 IPM line printer band type	Q2 FY80		
LP26	600 IPM line printer band type	Q2 FY81		

Note: Transfer costs and FCS dates for products whose FCS is FY81 and beyond should be treated as targets and/or estimates

FEATURES/FUNCTIONS
OF
SYSTEM TYPE: 11TO3, HARD DISK BASED

	DELIVERY IN FY	79	80	81	82	83	84	85
	CPU	LSI-11	F11	F11 CIS PAX		L70		VAX
	REL PERF	1	2.5	2.5		7.5		6
	FUNDED BY	02D	02D	02D		02D		02D
KB	MEM MIN.	64	128	128		256		512
	MEM MAX.	64	256	2MB		4MB		16MB?
	CCD/BBL's							
MB	FLOP MIN.							
	FLOP MAX.							
MB	DISK MIN.	10	20	20	(AZTEC) 40			
	DISK MAX.	20	40	40	80			
	ASYNC MIN	4	4	8				
	ASYNC MAX.	4	8	16				
	SYNC MIN.	1						
	SYNC MAX	1	2					
	INTELL. COM			2				
	TAPE							
	PRINTER	LA120 LA180 LP05	LP25	LP26				
	PUB. BUS	Q				NI		NI
	AVAIL SLOT	2.1	2.0	3.0				
	O/S	RT-11 11S	11M MUMPS + PREV YEAR	SCS-11 RSTS/E + PREV YEARS		RSTS/E TRAX UNIX KSOS + PREVIOUS YEARS		VMS?
	SELL $	18K	20K	20K	20K	20K		

BI= NEW BACKPLANE INTERCONNECT (NOT FOR PUBLIC USE)
NI= NETWORK INTERCONNECT

APPENDIX VIII

FEATURES/FUNCTIONS
OF
SYSTEM TYPE: 11V03 - MODULAR - FLOPPY BASED

Note:
R/S Cabinet
Merges with
Table Top

	FY	79	80	81	82	83	84	85
				PDT11/123				
	CPU	LSI-11		F-11 PAX/CIS	SAME AS FY 81			
	REL PERF	1		2.5				
	FUNDED BY	02D		02D&PL				
KB	MEM MIN.	16		128				
	MEM MAX.	64		256				
	CCD/BBL's							
MB	FLOP MIN.	1/2		1				
	FLOP MAX.	2		4				
MB	DISK MIN.				(AZTEC)			
	DISK MAX.				40 80			
	ASYNC MIN.	1	SAME AS FY79	1				
	ASYNC MAX.	4		4				
	SYNC MIN.	1						
	SYNC MAX.	1						
	INTELL. COM			2				
	TAPE				SAME AS FY 81			
	PRINTER	LA120 LP05		LA120 LP25				
	PUB. BUS	Q						
	AVAIL. SLOT	2.1		1.0				
	O/S	RT-11 RSX 11S		SCS-11 RSX 11M	SAME AS FY 81			
	TABLE TOP	NO		YES				
	SELL $	10K		10K				

FEATURES/FUNCTIONS
OF
SYSTEM TYPE: TABLETOP BOUNDED 11 ISP

	FY	79	80	81	82	83	84	85
		PDT11/150	PDT250		PDT11/15	PDT/15	VT211?	
	CPU	LSI-11			T-11	T-11		
	REL PERF	1-2/LSI-11			2.5	2.5		
	FUNDED BY	DCG	DCG		02D	02D		
KB	MEM MIN	16	16		64	64		
	MEM MAX	60	60		64	64		
	CCD/BBL's					256KB		
MB	FLOP MIN	1/4	1		1			
	FLOP MAX	1/2	2		2			
MB	DISK MIN			SAME AS FY80		SAME AS FY80		
	DISK MAX							
	ASYNC MIN	1	1		3			
	ASYNC MAX	4	4		3			
	SYNC MIN	1	1		1			
	SYNC MAX	1	1		1			
	INTELL COM	0	0		0			
	TAPE					TU58		
	PRINTER	LA120		LP25		LA12		
	PUB. BUS							
	AVAIL. SLOT							
	O/S	RT2 RT-11 CTS300	RT2 RT-11 CTS300		SAME AS PREV. YEARS			
	SELL $	10K	10K		$6K	$6K		

PDP8 ISP BASED SYSTEMS
"TABLE TOP"

	FY	79	80	81	82	83	84	85
		VT78	VT278	VT278	VT378			
	CPU	6100	6120	6120	6120			
	REL PERF	1	3	3	3			
	FUNDED BY	PL	PL	PL	PL			
	MEM MIN		16KW	16KW	16KW			
	MEM MAX	32KW	32KW	32KW	32KW			
MB	FLOP MIN	1/4	1/2	1	1			
	FLOP MAX	1/2	1	2	2			
MB	DISK MIN							
	DISK MAX							
	BUBBLES				256KB			
	ASYNC MIN	1	1	1	1			
	ASYNC MAX		3	3	3			
	SYNC MIN	1	0	0	0			
	SYNC MAX		2	2	2			
	INTELL COM							
	TAPE				TU58			
	PRINTER	LA180 LQP	LA34	LA34	LA34			
	PUB BUS	NO						
	AVAIL SLOT							
	O/S	O/S 78	SAME	SAME	SAME			
		DIBS	AS	AS	AS			
		WPS	79	79	79			
	SELL $	10K	5K	5K	5K			

**Advanced Development Project
*Shows programs committed with CSD funds or other DEC group funds
(?) In question

REVENUE AVAILABILITY OF CSD PRODUCT TARGETS AND DEPENDENT DEVELOPMENTS

PRODUCT ELEMENT FY	HARDWARE PACKAGE & KEY COMPONENTS CSD	SOFTWARE SW	STORAGE MS	COMMUNICATIONS N/C	TERMINALS PRINTERS CSD	CHIPS CSD
FY80	11T23* VTXX8(6120)* 11V23* FPF-11	RT-11(V4)*, F-IV* RSX-11M*, F-IV+* BASIC-11*, FMS-11(V2)* MICROS/PASCAL+ ROM BASIC+, MICRO ISAM+ Shoebox, T-11 Support	RL02* TU58*	DECNET Phase IV* Intelligent Communications Module*	VT132(DCG) VT162(COMM'L) LP25* VT100 Options*	F-11* CIS*
FY81	PDT11/123* 11T23P$_2$* PDT11/15	Fixed function terminal software for a personal technical & commercial computer. 5 fixed functional terminal sized applications	RX03* TS04(Qbus)? Qbus adaptor for R80 & RL04(+?)	8 Line asynch interface*	VT125 VT100L(DCG) LA34(Graphics)* VK100(ECS) LA24(HRDM)* LP26*	T-11
FY82		25 Terminal sized applications+	AZTEC(?) RL04(?) R800(?)	Integral Modem* DECNET Phase IV	VT200+(DCG) VT211* LA200* LA12*	
FY83	11T73(LSI-11/70)	Micros-32+ (for VAX)	R81Q(?) RX0?(2MB)(?)		LQP**	LSI-11/70
FY84	11T73(?)			DECNET Phase V		
FY85 -FY86	VAX11/730*					MICRO-VAX*

Appendix XII
5/4/79
E. G.

RATIONALE BEHIND EXTENDED MEMORY ON SMALL SYSTEMS

The following is a distillation of the rationale behind the PAX or extended memory program in the small systems plan.

Key Assumptions

Intelligent Comm. and new disks will be done for the Q-bus whether or not PAX is done.

If PAX is done, then CIS is a low cost development. Commercial Systems using it will save approximately 10K in resident library space and downward compatibility of COBOL operating code will be achieved. (Otherwise, recompilation of the source will be required for the smaller satellite system when part of a distributed systems network.)

Large memory space on small systems will considerably enhance the number of terminals possible on a small system and make feasible the use of floppies where not now possible. Increased memory space will offset the advantage TI will gain by using bubbles as a floppy "cache" or as a floppy substitute. Two factors are important; one is floppy wear and the second is access time.

Our OEMs have already extended LSI-11 memory beyond 256kb--they already are aware of the benefit of having large memories on small systems.

The 64kb chip will cause a technology push towards greater than 256kb.

The LSI11/70 will not be available as a system until FY83 (the plan). But we are too early in this program to be more than 50% confident of this date.

The consensus of all of the technical engineering people is that uVAX will not be available as a system until FY85-FY86. An earlier uVAX will not benefit by the appropriate process need to achieve the cost performance goals separating that product and Nebula I or Nebula II.

Doing PAX on a double will either result in significant incompatibility with our current systems (ok for the DCG market) or require LSI chip design at a cost that is 3 to 4 times the planned cost of the PAX project proposed.

The introduction of the IBM Series 1 as an OEM product and 15% discount as well as the initial entry price of $5K to $6K (down from $15K) will create a strong push for a Low End processor with greater than 256kb address space.

RATIONALE BEHIND EXTENDED MEMORY ON SMALL SYSTEMS (continued)

Given the above assumptions and the planned revenue stream in this space, then it is believed that we will not have the right product to meet the needs for several hundred million dollars of NOR in the FY81 to FY83 timeframe. This is for the product line groups to verify for themselves.

No new software is needed for support of options beyond that which is already being done for less than 256kb small systems.

The software effort for supporting RSTS-E on the Q-bus and for supporting RSX-11M and RSTS-E for systems greater than 256kb is small. (The current estimate reported by Jack Mileski is $65K for creating support for RSX-11M or RSTS-E or a total of 130K for both operating systems).

This effort will not delay work on the new interconnect for the LSI11/70 and uVAX. If the new interconnect BI proves feasible, earlier implementation will be considered. This includes use for the F-11 extended memory.

The components engineered by CSD will be required by the tabletop or PDT 11/150 follow-on. Packaging will be sponsored/engineered by the Commercial Group.

The applications software and marketing input for the $5K PDT type product will not be available til FY81.

Appendix XII

PRO - CON

PRO

Permits us to compete in FY81 - FY83 time when "Small Systems" will be expected to offer >256kb capability

Avoids proliferation of non-standard PAX schemes by our OEM's

Keep the memory business for our small systems with DEC

Enhances and increases reliability of floppy based systems

Increases number of users on a shared small system from

2 to 4 floppy based
8 to 16 hard disk based (unverified assumption)

Permits use of very low cost memory array boards

CON

Creates another memory bus (P-BUS) which will use another memory board part

Delays the engineering of a $5K target sell price bounded system

Software or disk developments could yield a greater NOR benefit

Is not totally compatible with DCG form factors

DIGITAL

INTEROFFICE MEMORANDUM

TO: Dick Clayton

DATE: 19 JUNE 1979
FROM: Stanton Pearson
DEPT: Planning & Product Management
EXT: 3-2424
LOC/MAIL STOP: ML12-2/E71

SUBJECT: 1979 ACCOMPLISHMENTS VS. PLAN AND FY80 PLANNED ACCOMPLISHMENTS

The last year has been a year of accomplishments for CSD. These accomplishments had a manageable share of operational problems, a small number of which we are still working on.

We announced several significant products including the LA34/38, LA120, VT100, and the LSI23. All of these products are forecasted to achieve a minimum of 100,000 units in their lifetime.

We succeeded in shipping software to support our products at FCS. Forms Mgt (FMS) and the Key Editor (KED) were available at FCS of the PDT-11 and VT100, operating systems will be ready for FCS of the 11/23.

Additional technologies were loaded into the front end of the product pipeline such as: graphics architecture, microprocessor architecture, new printing concepts and techniques and some human factors in software that should improve the "ease of use" of future products.

We are moving along the strategic directions articulated in the FY78 Red Book and are continuing to broaden these strategies to include more of the "TOTAL SYSTEM" market requirements. This means better coupling between CPU, Software, Storage and Comm/Nets Planning at the Engineering level and the Product Lines at the Market level.

The content, schedule and budget of all major programs occurred essentially within the plan established last year. Three of the most significant challenges that we faced in FY79 were:

- Building the organization
- Managing the synchronization between Market demand, Product Line forecast and Manufacturing capacity. Products effected by this were VT100, LA34, LA120 and LSI-11
- Decentralization of the Functional Engineering effort (Pwr. Pkg. Systems Interconnect, etc.) has been a major effort in FY79.

  We expect the transfer of the Functional Engineering responsibility to other groups in Central Engineering during FY80. This will allow for a significantly more focused management effort on our primary mission for Small Systems and Terminals.

During late FY78 and earlier FY79 we have seen the addition of some senior management talent in the finance area. This strengthening of the finance group has been very instrumental in allowing us to be essentially on budget for all major CSD programs.

In the personnel area, we initiated a human resource planning activity that resulted in a restructuring of the CSD organization for FY80. Some key features of the re-organization are to achieve better balance of the workload across key managers, better alignment of responsibilities with future goals, a more focused coupling of key technology and product capabilities.

In the planning area we have replaced several people who left the organization towards the end of FY78 and early FY79. We have also split the effort into three areas of focus (a) planning methods and coordination (b) 2 to 5 year long range planning (c) Product Management which focuses on the 0 to 2 year time frame with an emphasis towards product introduction and marketing support and (d) operations management which focuses on program management techniques and review against the content and schedule of major programs.

Key factors to be managed in FY80 are:

1. The smooth transition of the Service Groups into other parts of Central Engineering so we can better concentrate on our primary mission of delivering Small Systems and Terminal Products to our markets.

2. Continue to strengthen our linkage to the Manufacturing, Product Lines and Field Support organizations at both the Strategic and Operational levels. This will require specific attention at the market demand vs. manufacturing capacity boundary.

3. Towards the end of FY80 the Chip Manufacturing and Engineering operations will be re-locating to the new Hudson facilities. We must plan for, and manage, the implementation of this re-location so it does not impact the manufacturing capacity for the LSI-11 and LSI-23 or the engineering schedules for Tiny-11, Fonz memory extensions and VLSI-70.

4. Due to a very aggressive set of semiconductor engineering programs, coupled with a tight DEC human resource availability, we have elected to sub-contract the development of the VLSI-70 program to Harris Corp. We view the Harris decision to be a lower technical, but higher management, risk worth taking.

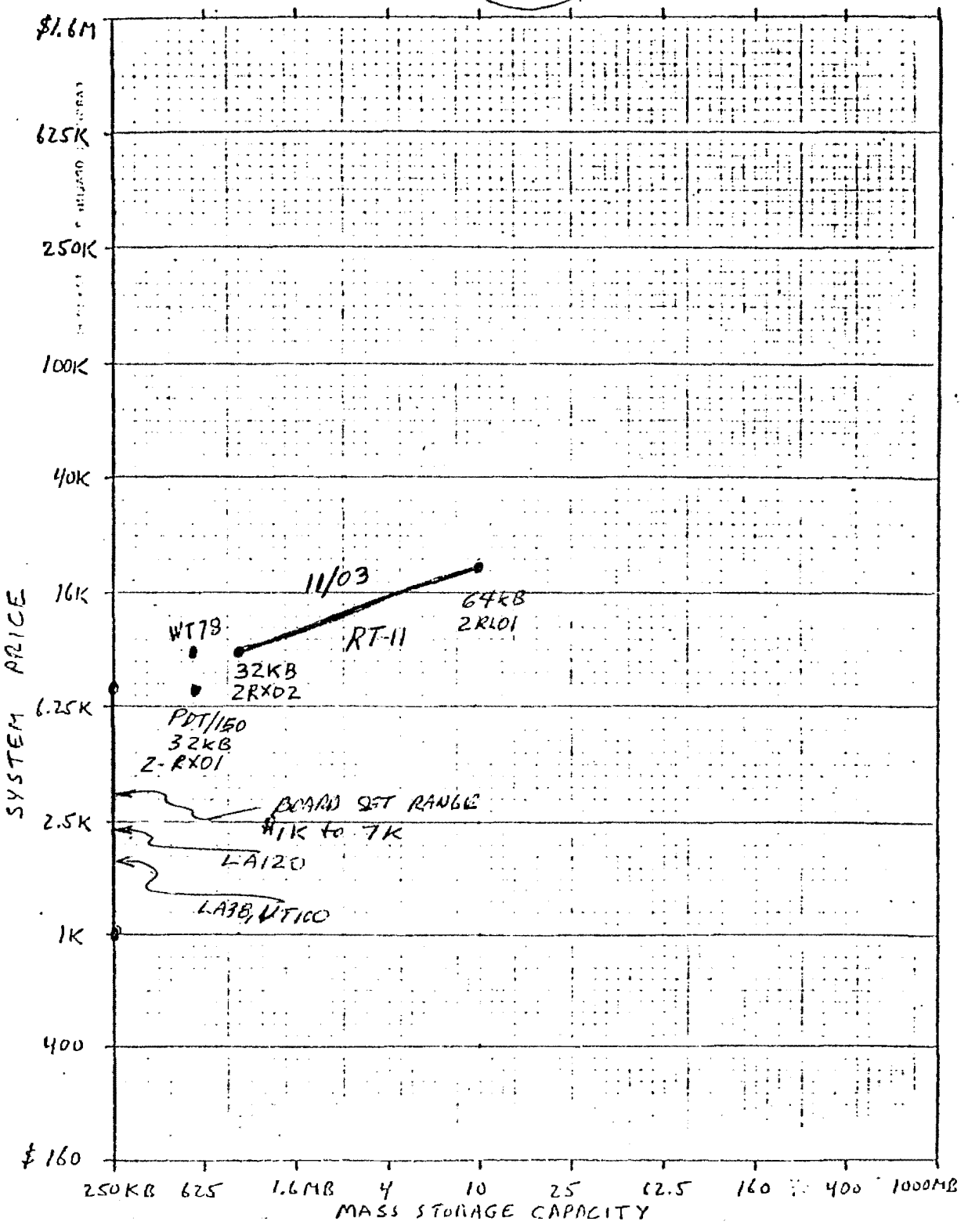
5. Our ability to locate, recruit and retain key personnel has been a challenge in FY79 and must be aggressively managed in FY80, so it does not become a problem.

   The area of primary concern is Semiconductor Engineers.

4. SMALL/MID/LARGE SYSTEMS PRICE VS. STORAGE CAPACITY

FY79

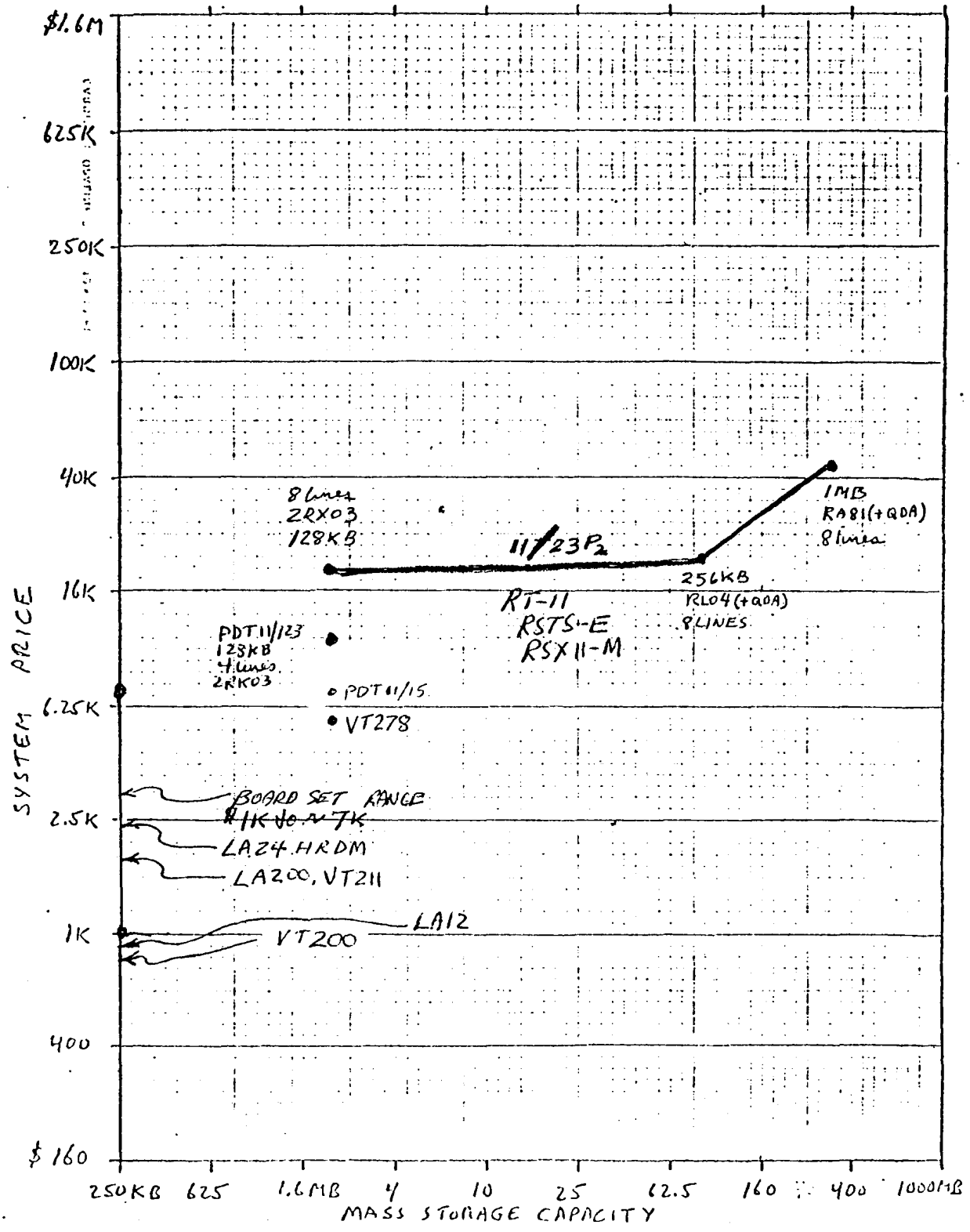
APPENDIX XIV



4. SMALL/MID/LARGE SYSTEMS PRICE vs. STORAGE CAPACITY

APPENDIX XV

(FY82)



PLANNING AND PRODUCT MANAGEMENT
BALLPARK ESTIMATE OF LIFE SPAN
COST AND VOLUME EXPECTATIONS

PRODUCT	AVERAGE TRANSFER COSTS ($)	LIFETIME BUILD TOTAL (THOUSANDS OF UNITS)	LIFE SPAN (FY)
Chips and Chipsets			
LSI-11	40	200	78 83
F-11	25-90	500-1000	80-87
T-11	6-20	1000-3500	81-88
J-11	100	300-1000	83-88
uVAX	Undefined*	>500	84 90
Rack and Stack Systems			
11/03	3K-5K	26-29	76-81
LSI-11/23	3K-5K	50-65	80-85
LSI-11/70	3K-5K	125-175	83 90
Table Top Systems			
PDT 11/130	1700	80-100	79-84
PDT 11/150	2100		79-84
PDT 11/123	2000-2600		81 86
PDT 11/15	1700		81 86
Printer Terminals			
LA36	660-800	200	75-81
LA120	750-800	175-225	79 84
LA12	250-350	200-400	82-88
LA200	300-450	400-600	83-88
LA24	475-550	25-40	81-83
LA34/38	375-575	300	79-84
Video Terminals			
VT52	625	50	74-80
VT100-VT131	600-700	300-325	79-84
VT101-VT132	350 425		
VT211	600-700	400 600	82-88
VT200	200		83-87
VK200	100		83 87

*100-150 Target

GLOSSARY OF INTERCONNECT TERMINOLOGY

1. Overview

Network Interconnect (NI) used to join computers, workstations, intelligent terminals, low end real-time subsystems, etc., in a local area network. The important characteristics of the NI are: (1) low cost, (2) long length (1 kilometer), (3) moderate bandwidth (1 megabit/sec.), (4) a large number of drops (64), (5) electrical isolation, and (6) data integrity. The NI ultimately replaces the DMP-11 (for local use) and the DEC Dataway.

Backplane Interconnect (BI) used to join a processor to integral I/O controllers, I/O bus adapters, or other processors. The important characteristics of the BI are (1) low cost, (2) short length (.5 meters), (3) high bandwidth (6 megabyte/sec.), (4) a moderate number of drops (16), and (5) data integrity. The BI ultimately replaces the Unibus, Qbus, and other private backplanes.

ICCS - A Computer Interconnect (CI) used to join closely coupled high end computers, mass storage subsystems (e.g., HSC-50), real time subsystems, and communication subsystems (e.g., Mercury). The important characteristics of the CI are (1) moderate length (100 m), (2) high bandwidth (6 megabyte/sec.), (3) moderate number of drops (16), (4) electrical isolation, and (5) data integrity. The CI ultimately replaces the PCL-11B and (together with D and E below) the Massbus.

Storage Interconnect (SI) used to join disk drives to controllers. The important characteristics of the SI are (1) high bandwidth (3 megabytes/sec.), (2) moderate length (10 m), (3) functionality needed to properly partition controller/drive logic, and (4) data integrity. The SI ultimately replaces a number of drive specific interconnects.

Memory Interconnect (MI). The MI is the processor-memory interconnect. In many of DEC's systems, the MI and BI are physically the same. For example, the Unibus is used as both a BI and MI in the PDP-11/34. The 11/70 memory bus is an example of an MI that is separate from the BI. The key characteristic of an MI is that it have the cost/performance characteristics required for the system being built.

Integrated Circuit Interconnect (II). The drive requirements of common MI's and BI's are not compatible with buses driven from LSI integrated circuits and so another level of interconnects has emerged. The Intel 8080 bus (TTL), the DEC F11 MOS bus and the Comet W bus are examples of II's. Pinout and power consumption are the critical constraints on II's.

Device Interconnect (DI). Used to join terminals and terminal like devices to computer systems.

Interconnect Hierarchy (DI, NI, SI, CI, BI, NI, II)

Note: The above was borrowed from the Interconnect Task Force report presented at Stratton Mountain

CSD MAJOR PROGRAM SPENDING FY80,81,82

SUMMARY BY ORGANIZATION
($K)

	FY80 OOD/OTHER	FY81 OOD/OTHER	FY82* OOD/OTHER	NOTES
CHIPS	4524/0	6005/0	7860/0	incl. Microvax&Microwar
11 SYSTEMS	2722/400	3347/0	4105/0	incl. Mech.Eng.
8 SYSTEMS	0/2175	0/1300	0/750	'81&'82 are Wag's
VIDEO	2806/723	3755/1500	3505/2500	incl. VT100 for.char.se
PRINTERS	5000/618	6105/650	4040/750	
PLANNING	483/0	555/0	639/0	
ADMIN	556/0	639/0	735/0	
LSI STAFFING	(350)/0	--	--	
HUDSON INCREMENT	--	1000/0	2000/0	assumes Bldg#2 in 6/81
CSD TOTAL	15741/3916 19,657	21406/3450 24,856	22885/4000 26,885	

* FY82 includes only continuation of FY81 efforts - no new starts; the FY81 figures are current commitments plus PDT11/15 ($350K); BI/NI ($500K); RL Interface ($250K); VT211 ($700K) which are basically moving from Adv. Dev'l in FY80 to Product Dev'l in FY81. IN ESSENCE THE ABOVE THREE YEAR PROJECTION INCLUDES ONLY NOMINAL NEW PROGRAM STARTS BETWEEN NOW AND FY82.

CSD MAJOR PROGRAM SPENDING FY80,81,82

ORGANIZATION/PRODUCT	FY80	FY81	FY82	
CHIPS/APPOLLO	650/0 *	1400/0	3500/0	
MICROWARE	724/0	905/0	1131/0	(25%growth assumed
T-11	1240/0	800/0	--	
F-11	600/0	300/0	--	
J-11	1150/0	2000/0	2500/0	
ADV DEV'L	100/0	400/0	500/0	(25%growth assumed
ADMIN	60/0	200/0	230/0	(15%growth assumed
CHIPS TOTAL	4524/0	6005/0	7861/0	
11SYSTEMS/11V23;11T23 R/S	224	200		
CPU; I/O MODULES FOR R/S SYS W. 2 MODEPAX	439			
MEM. ARRAy W. 16/64K CHIP	100	150		
PDT 11/123	0/400			
INTEL COMMUN	210			
ASYNCH COMMUN		100		
PDT 11/15		350	1000	
I/O LOW END BUS; BI/NI		500	1000	
DRV - 11J	29			
R80/RL04 MASS STORAGE INTERFACE		250		
ADV DEV'L	330	400	500	
SUPPORT	732	850	975	(15% growth assumed)
ADMIN	508	547	630	(15% growth assumed)
SYSTEMS SUBTOTAL	2572/400	3347/0	4105/0	
MECH. ENG.	150/0			
11 SYSTEMS TOTAL	2722/400	3347/0	4105/0	
8 SYSTEMS/OMNIBUS SUPPT	/268	/200	/200	
VT 78 SUPPT	/120			rough estimates
H6120	/150	/ 50		for 81,82 assum
VT278	/1009	/500	/400	phase out of 8's
VT278 ADV DEV'L	/497	/500	/150	by FY83
H6120 DECwriter ADV DEV'L	/131	/50		
8 SYSTEMS TOTAL	0/2175	0/1300	0/750	

* X/Y WHERE X REPRESENTS OOD FUNDING AND Y REPRESENTS OTHER FUNDING

CSD MAJOR PROGRAM SPENDING FY80,81,82

ORGANIZATION/PRODUCT	FY80	FY81	FY82	
VIDEO TERM/VT100 PR.PT	168/0			
GRAPH ARCH.	100/0	250/0	1000/0	
VT125	167/200	150/0	--	
VT101	640/0	0/300	--	
VT200	245/0	0/1000	0/2500	
VT211		700/0	1500/0	
VK100	0/523	0/200		
VIDEO DEV'L		400/0		
COLOR, HI/RES, ADV DEV	200/0	275/0		
VT211 ADV DEV	440/0	--		
R&D FLOW THRU	110/0	200/0	240/0	(20% growth assum
INTEG. H. COPY	100/0	450/0		
SUPPORT	400/0	1100/0	500/0	Finance Estimate
ADMIN	130/0	230/0	265/0	(15% growth assum
VIDEO SUBTOTAL	2700/723	3755/1500		
VT100 FOREIGN CHAR SET	106/0	--	--	
VIDEO TOTAL	2806/723	3755/1500	3505/2500	
PRINTER TERM/LA34	100/0		0	
LA12	1100/0	1500/0	1350/0	
LA200	1100/0	1900/0	950/0	
LA34G	62/0	20/0		
LA24 (HRDM)	800/0	360/0	0	
VIDEO OPTION	--	--	--	
LINE PRINTER	250/0	275/0	300/0	
VT162	0/260			
ADV DEV'L	538/0	800/0		
ADMIN	200/0	250/0	290/0	
OOD SUPPORT	850/0	1000/0	1150/0	(15% growth assum
DCG " "	0/55	0/150	0/175	
MFG " "	0/303	0/500	0/575	
PRINTER TOTAL	5000/618	6105/650	4040/750	
PLANNING	483/0	555/0	639/0	assume 15% growth
ADMIN	556/0	639/0	735/0	assume 15% growth
LSI CONTINGENCY	(350)/0	0/	0/	
		1000/0	2000/0	HUDSON INCREMEN
CSD TOTAL	15,741/3916	21,406/3450	22,885/4000	

F. Mid-Range Systems

MID RANGE SYSTEMS

FY80 RED BOOK

BJL2.8 - 8 Jun 79

TABLE OF CONTENTS

I. INTRODUCTION

A. Product and Functional Scope

The Mid-range Systems cover the historical core of Digital's minicomputer business in the OEM, Scientific/Computation and Commercial Market places.

The product space in the iron OEM environment ranges from the $4,000 PDP-11/04 box to the $98,000 cpu only VAX-11/780. The system product space, expressed in terms of packaged systems offerings, ranges from the $21,000 PDP-11/04 with RT-11 to the $190,000 VAX-11/780 with VMS, RP06 and TU45. The area of responsibility assigned by charter to the Mid-range Systems Group is delimited at the low end by the Unibus machines boundary and at the high end by the average system selling price boundary of $150,000 for a single VAX processor. *

B. Basic Product Strategy

The implementation of the Corporate Strategy, (i.e. focus on distributed processing and high availability systems, convergence towards a single 32 bit architecture by 1985, center of DEC business in systems below $250K, protection of the existing PDP-11 and DEC10/20 customers base) is the framework within which the Mid-range Systems has been developed. The tactics used to achieve the goal is to apply technology to the PDP-11 products in order to reduce the cost, and to collapse the number of offerings into one (FY83 time frame) while fixing the functionality and performance at the PDP-11/74 level. At the same time a similar technology tactic is applied to backfill the PDP-11 price space with 32 bit products starting at the high end and moving downwards. A single operating system based on the RSX-11M/RSX-11S model is assumed for the 32 bit family. All 32 bit processors can be connected in a Distributed Topology via high speed busses.

* NOTE: THE BOUNDARY DEFINITION OF THE MID-RANGE SYSTEMS SPACE HAS BEEN MODIFIED DURING THIS RED BOOK PROCESS. THE OVERALL STRATEGY DESCRIBED IN THIS DOCUMENT HAS NOT CHANGED. THE IMPLEMENTATION OF THE VENUS PRODUCT HAS BEEN MOVED INTO THE LSG SPACE. REFERENCES TO VENUS IN THIS DOCUMENT ARE NOW IN THE CONTEXT OF AN OVERALL STRATEGY NOT THE SPECIFIC IMPLEMENTATION OF THE PRODUCT.

II. DEVELOPMENT STRATEGY; RELATIONSHIP TO BASIC PRODUCT STRATEGY

A. Statement of Strategy

The first element of the strategy is to complete the PDP-11 products currently under development, then to collapse the offerings onto one product in FY83 using the Small Systems JAWS-11 chip set as a base.

The second element of the strategy is to develop and maintain/enforce over time a leadership family of THREE 32 bit machines interconnectable between themselves via a Distributed Topology BUS and DECNET to cover the $20K to $250K systems price range. Included in this effort is the articulation and management of a new I/O structure necessary to augment the total system cost/performance effectiveness and manufacturability.

The third element is to work the definition of LSI VAX with the Small System Development group, and the definition of the High end machine with the Large System group

B. Major Constraints

A significant constraint in implementing the strategy lies in the scarcity of VMS resources who are needed to participate in the system design, implementation of software and checkout of the systems.

Another constraint is related to our ability to shift engineering talents from a rack and stack design/implementation approach to a system orientation.

The implementation of "total systems" is further constrained by our ability as a corporation to integrate the manufacturing piece early in the product development cycle with a high degree of stability and predictability (e.g. transfer costs, volume availability).

The cost/performance of the systems we produce is greatly affected by the mass storage components which are used, and as such we are highly dependent on the availability of leadership mass storage devices and I/O interconnect schemes.

The last, but not least, constraint addressed here is related to the nature of the business we are in, i.e. maximum flexibility required for the OEM and some LDP applications v.s. greater system cost effectiveness with a loss of flexibility for most of the end user applications.

C. Areas not covered by strategy

Highly focused products, targeted for a specific type of application (e.g. word processing) are not addressed by the proposed strategy because it is not understood whether or not they can be identified from a marketing point of view and generate the required return on investment. No effort, outside of Advanced Development, is planned for the implementation of Secure Systems.

No effort is planned to integrate Software Functionality into hardware in order to improve performance and/or protect our investment.

D. Rationale

1. Market

The Mid-range System Products are targeted to be used by the Technical and Commercial Products Group. The personality of the sytems which are shipped/sold to customers in diverse applications is achieved by applying hardware options (i.e. FPA, CIS, single v.s. multiple channels) to a base machine and software functionality (i.e. FORTRAN, COBOL, DBMS etc..).

The three VAX machines strategy for the $20K - $250K range has been arrived at through analysis of historical data, competitive offerings and our ability (as well as competitors') to design systems which span a functionality and price range of 2 to 2.5.

An overlap between 16 bit, 32 bit and 36 bit products is perceived as necessary during the transition phase to a single architecture strategy to protect our customer base.

2. Competition

The competitive pressure is perceived to come from the following directions:

a) Targeted applications/computing philosophy by companies such as TANDEM in the High Availability area. Our solution has to be based on the 11/74 Mp today and Hydra in the long run. Articulating our response will be a marketing challenge.

b) Traditional 16 bit computer manufacturers such as DG, HP who are increasing the cost performance effectiveness of their systems by applying technology and/or software functionality. (Cost of Mass Storage devices will be a significant issue).

c) Traditional 16/32 manufacturers such as INTERDATA, SEL PRIME, low end of IBM and DG in the future. COMET, NEBULA offerings are the cornerstone of our response to INTERDATA and SEL in the OEM business (i.e. low cost + family breadth).

Increased software functionality in VMS layered products is required to address the IBM, HP thrust and PRIME to a certain extent.

Given the current and near future functionality/performance of our products (11/780, VMS, COMET in particular) PRIME can probably be countered best thru aggressive marketing.

d) Semi conductor manufacters who are developing low cost 16 bit and 32 bit chip products which in turn can be used to build systems. (e.g. Intel Ahola project).

Our strategy is to bring competitive technology in house (gate array, ECL Macro gate array) and emphasize our ability to design systems and software to support them.

e) Impact of distributed office systems such as the XEROX ETHERNET project.

f) Last but not least, IBM whose new products are coming down in our traditional business space.

3. Technology

The technology factors can be split into the tradional ones such as semi conductor advances and new computing approaches.

a) Semi Conductors

The approach is to track memory technology, (16K, 64K chips etc.) and incorporate new advances where economically attractive. The design of new circuits/chips is being pursued actively (gate array, ECL gate array, LSI). The strategy is to have in house capabilities backed up by second sources.

b) New Computing Approaches

The Distributed Processing Technology (as well as high availability) is addressed in the context of Hydra, DECNET and new I/O Architecture. Our future 32 bit products are designed to incorporate this capability in the hardware sense, and in the VMS base software.

The wider word length machines concept (for minicomputers and micro) is gaining rapid acceptance. The VAX architecture has put us in a leadership position which we need to exploit in our marketing effort.

c) The usage of fiber optics, video disks technologies in our systems need to be monitored closely.

d) Technology for Mass Storage devices is assumed to be part of the Mass Storage Red Book.

e) The impact of ACS on our business can be dramatic and will require close monitoring.

4. Digital Strengths and Weaknesses

Strengths:

- Hardware and operating systems architecture (PDP-11, 11/45, VAX, RSTS, RSX, TRAX, VMS).

- System performance leadership primarily carried by the cpu component and RAMP features.

- Breath of products and familiness. (DEC10/20, PDP-11 -----> VAX).

- Volume Manufacturing Capabilities.

- RAMP Features, RD capabilities.

- Approachable systems (DCL, Datatrieve, MINC etc.).

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Weaknesses:

- Perhaps less than optimal product overlaps.
- Long response time to exploit leadership of new products (e.g. PDT, VAX, DECNET).
- Weak (improving) performance characterization effort leading to the positioning of our products v.s. competition.
- Investment in Mass Storage and I/O interconnect technologies.
- Quick marketing exploitation of NEW products.
- Database products.
- More sophisticated software support policies.

E. Changes from last year strategy

Five major changes have occured in the product strategy space:

1. Reduction of the number of cpu developments (11/68, 11/48, 11/74 CIS).

2. Launching of the Hydra program to address the distributed and high availability applications.

3. Formalization of the long term strategy.

4. Redefinition of Mid-range Systems boundary.

5. Formulation of an I/O interconnect strategy. (refer to Bill Johnson document "APRIL INTERCONNECT TASK FORCE REPORT" dated 17 April 1979 for details).

III. PROGRAM AND PRODUCT DEVELOPMENT TACTICS

A. Major Products Planned for Development

a) 11/74 MP

The 11/74 MP is a multi-processor version of the 11/70 using a shared memory approach and high availability packaging techniques.

The 11/74 MP is planned to be offered in packaged systems configurations with 2, 3 and 4 processors and the RSX-11M+ software.

Xfer cost:	$ 28 K (2 cpu's, Mem, Mp hardware)
FCS:	November 1979
Volume Availability:	February 1980

b) 11/70

The 11/70 will continue to be offered as the main high end 16 bit product. The 16K MOS ECC Memory will be offered on the PDP-11/70 in the Q1 FY80 time frame.

c) VAX-11/780

Four enhancements to the 11/780 are under development.

The MA-780 is a multiport shared memory capability which will allow two processors initially (4 later) to share data and code (software supported). Two copies of the operating systems are required, one for each processor. No special packaging and/or software for high availability is included.

The MA-780 is targeted for the simulation market and highly sophisticated technical customers. A COMET version is also under development.

Xfer Cost:	$ 8.5K
FCS:	November 79
Volume Availability:	N/A (low volume option)

The DR-780 is a high speed 32 bit parallel interface (6Mb/Sec data rate) allowing the interconnection of 2 VAX-11/780 cpu's in a point to point arrangement. It also provides the vehicle for our customers to interface special devices (e.g. array processors, graphics systems etc..) to the 11/780. A software driver is provided with this option.

A COMET version is also under development.

Xfer Cost:	$ 2.2K
FCS:	Q3 FY80
Volume Availability:	N/A (low volume option)

Up to 4 Unibusses will be allowable on the 11/780 (instead of one today). This capability provides a higher system thru-put for Unibus devices such COM options and terminals. This feature is already supported in VMS.

Xfer Cost:	$ 2.1K
FCS:	Q4 FY79
Volume Availability:	N/A (low volume option)

Extended Floating Point exponent range is being developed for the 11/780. This effort was dictated by competitive pressure (PRIME, IBM, UNIVAC) in the scientific/computation market place.

The new capability includes two data types. The first is a larger range, slightly lower precision form of double precision (= CDC, UNIVAC, exceeds IBM). The second is a very large range, very high precision quadruple precision form (= CRAY-1, similar to IBM X-Format).

The capability will be phased into the product as a purchasable ECO. A COMET version is also under development.

Xfer Cost:	N/A (microcode)
FCS:	Q2 FY80 if funded
Volume Availability:	Same as FCS

A low cost entry system 11/780 proposal (Technical Product Group request) has been approved. This will allow us to bring the entry system to $99K from $128K.

Xfer Cost:	$24.2K
FCS:	8 months after funding
Volume Availability:	3 months after FCS

d) 11/44

The PDP-11/44 product can be looked at as a PDP-11/34 with increased addressing capability (22 bit vs 18 bit), larger physical memory (1Mb vs. 256Kb) and a commercial instruction set option. The product will be offered both in an OEM (10 1/2" box) and packaged system configurations. It is intended to replace the low end 11/60 business and the high end 11/34 business.

Xfer Cost:	$ 9.2K (2 x RL02 system); $ 4.6K (box)
FCS:	November 1979
Volume Availability:	March 1980

e) 11/24

The 11/24 strategy has been altered as a result of the June 12, 1979 EBOD meeting. The 11/24 as defined prior to the June 12 decision was based on the F11 chip set, included a Unibus, CIS option and up to 256 Kb of memory (no PAX). The product was to be offered both in an OEM and packaged systems configurations.

The cost and schedule goals were:

Xfer Cost:	$ 5.8K (2 x RL02 system); $ 1.9K (box)
FCS:	December 1979
Volume Availability:	May 1980

The new strategy is as follows:

a) Introduction of the current 11/24 to manufacturing has been postponed until September 1979.

b) The PAX Qbus and CIS projects will continue until September 1979.

c) A new engineering effort based on the F11 chip set 11/24 packaging and new backplane interconnect "BI" has been launched.

d) In September a decision will be made to either productize the 11/24 "BI" product and to not PAX the Qbus and not productize the current 11/24 or to release the current 11/24 and PAXed Qbus.

The long term strategy is highly focused on the "BI", schedule cost and software implications are elements which need to be understood between now and September.

f) COMET

COMET is the second member of the VAX Family; it uses a new circuit technology (gate array), backplane technology (press pin), has a single UNIBUS and up to 3 busses (such as Massbuses). Maximum memory with 16K chips is 2Mb (8Mb with 64K chips). The system runs VMS (Release 2) and will be offered in OEM (box) and packaged systems versions. CIS is integral to the base machine. A floating point accelerator is planned as an option. Performance (whetstone, US Steel) is targeted at .6/.7 x 11/780.

Xfer Cost:	$12K (2 x RL02 System); $ 7K (box)
FCS:	December 1979
Volume Availability:	June 1980

g) NEBULA

NEBULA is the third member of the VAX Family; it uses conventional technology (bit slice) and commercially available parts. The memory system is designed for 64K chips (16K chip arrays can also be used). It is a UNIBUS machine initially; the New I/O bus is planned for FY82. Maximum memory is (3Mb) using 64K chips. CIS is integral to the base machine. A floating point accelerator is planned; runs VMS. The product will be offered in an OEM box and packaged systems. Performance (Whetstone, US Steel) is targeted at .2/.3 x 11/780.

Xfer Cost:	$ 6K (2 x RL02 system); $ 1.8K (box)
FCS:	Q1/Q2 FY81
Volume Availability:	Q4/Q3 FY81

This is for reference only. The project is being addressed in the LSG Red Book.

h) VENUS [FOR REFERENCE ONLY]

VENUS is an 11/780 replacement machine in terms of cost; the design center is set at $180 MLP (MKup = 4) for a cpu, 2Mb memory, 1 RP07, 1 TU78, 16 asynchronous lines.

The performance (Whetstone, US Steel) is targeted at 3.5 x 11/780.

The technology used is the same as D36 (i.e. ECL Macro gate array).

An SBI is provided so that MA780, DR780 need not be re-engineered.

This product is perceived as necessary to maintain leadership in the $120K - $250K range.

Xfer Cost:	$25K (entry); $45K (typical)
FCS:	Q1 FY82
Volume Availability:	Q3 FY82

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i) Unibus Option Cabinet

A standard unibus options cabinet designed for COMET, 11/44, 11/24, NEBULA expansion; it is built around the new corporate 40" high 22" wide cabinet and the 11/44 processor box.

Xfer Cost:	$ 1.3K
FCS:	December 1979
Volume Availability:	May 1980

j) I/O Interconnect

The first element of the development effort is to build a high speed (10Mb/Sec), message oriented bus (ICCS) to connect COMET processors in a HYDRA configuration. The same bus will be used to connect the HSC50 mass storage subsystem to VAX processors and the HYDRA developed COM subsystem (MERCURY). COMET is the first product which is planned to have the ICCS capability.

The other developments revolve around the definition of a new bus (the backplane interconnect "BI"), a low cost serial bus "NI" and the implementation of new peripheral controllers for these buses.

k) System Performance Measurement

A System Performance Measurement and positioning plan has been developed for MSD by System Engineering (Terry Potter/Paul Kampas group).

- Single User Positioning. (One RT/Scientific and one Commercial workload)

RSTS:	11/24, 11/44,
RSX:	11/24, 11/44,
VMS:	COMET, NEBULA
HP-3000/33	

- Multiuser Positioning (one RT/Scientific and one Commercial workload)

RSTS:	11/24, 11/44,
RSX:	11/24, 11/44,
VMS:	COMET, NEBULA

NOTE: It is assumed that 11/780 positioning will have been completed in FY79.

Same level of effort should be applied to TOPS-20 for 2020, 2060.

Corporate $ are needed to purchase/lease an IBM S/38 and do comparative studies.

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l) Packaged Systems

The engineering packaged system effort for MSD products will be carried out by Systems Engineering (Herb Shanzer).

11/44	RL02 RL02 RK07 RK07 RK07 TS04 RM02 TS04 R80	11/70	RK07 RK07 RM03 TU77 RP06 TU77 RP07 TE16 R80 TS04	NEBULA	RL02 RL02 R80 TS04 RK07 RK07
				11/74 MP	RM03 TU77 RP06 TU77 RP07 TU77 R80 R80
11/24 RL01 RL01 RL02 RL02 RP07 TU77	RX02 RX02 RK07 RK07	11/60	RL02 RL02 RK07 RK07		
1134A	RL02 RL02	COMET	RL02 RL02 RK07 RK07 RM03 TS04 RP06 TU77 RP07 TU77 R80 TS04	11/780	RM03 TU77 RP06 TU77 RP07 TU77
				11/780	MULTIPORT MEMORY

Common cabinet for tapes and disks (RL02, RK07, RM03, R80, TS04, TU77).

Central Packaged Systems Product Management will be integrated in the Mid-range and Small Systems groups.

m) PDP-11/XX

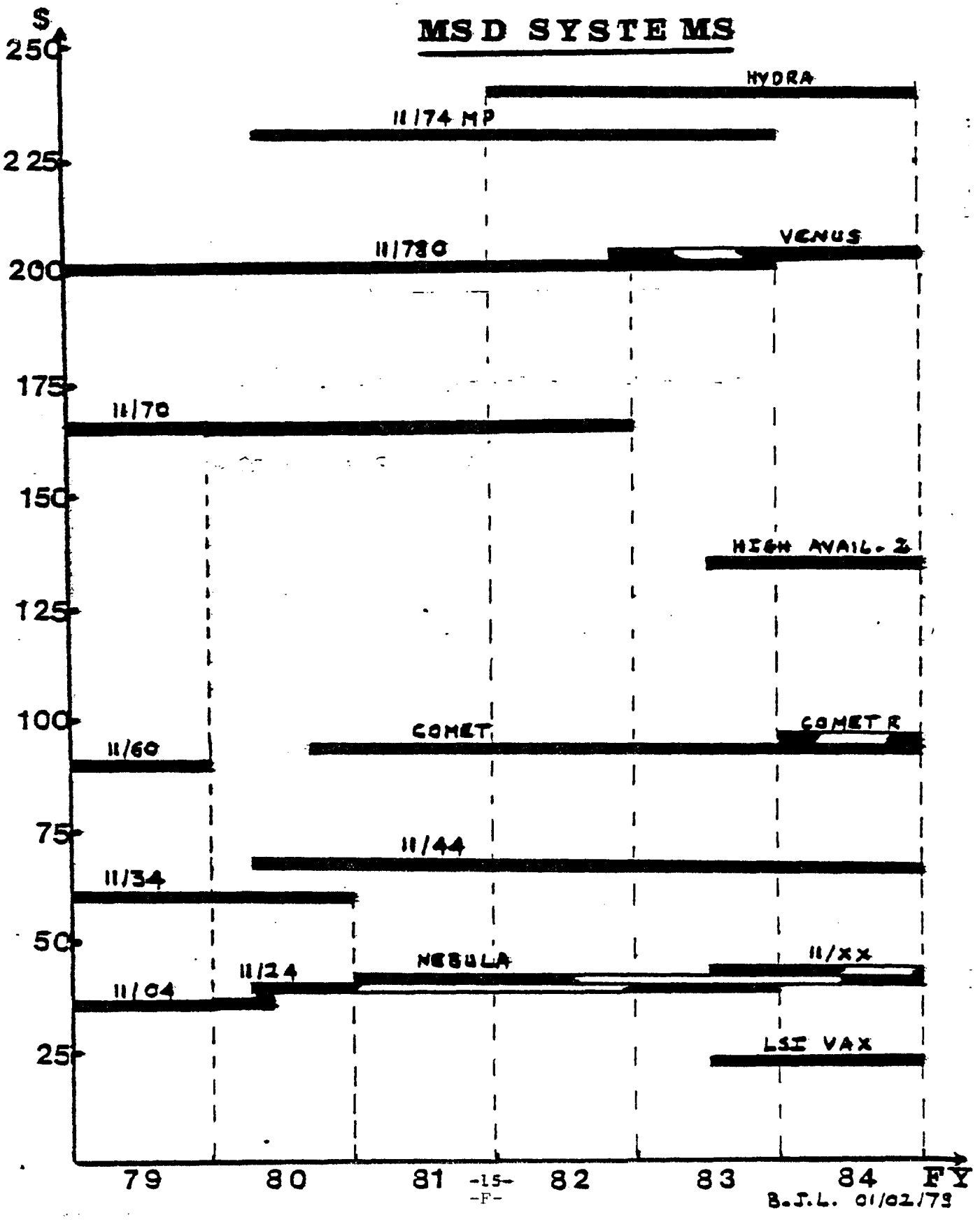
The PDP-11/XX is a 16 bit machine with the functionality and performance of a PDP-11/74 and the cost of an 11/24.

It will use the JAWS-11 chip set (Small Systems) as the base to build a system product in the FY83 time frame using the same approach as for the FONZ/11/24 projects.

n) LSI/VAX - NEBULA Replacement

A system product based either on the LSI VAX chip set or new technology applied to NEBULA to provide a constant cost (same functionality, greater performance) replacement to NEBULA in the FY84/85 time frame.

MSD SYSTEMS



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FY80 BUDGET

COMMITTED PROJECTS:	$ 7,680 K
I/O INTERCONNECT:	$ 760 K
ADVANCED DEVELOPMENT:	$ 885 K
PRODUCT MANAGEMENT:	$ 1,150 K
SYSTEM PERFORMANCE:	$ 250 K
PACKAGED SYSTEMS:	$ 620 K
NEW DEVELOPMENT:	$ 2,625 K
ENGINEERING SERVICES:	$ 550 K
ADMINISTRATION:	$ 680 K
CONTINGENCY	$ 100 K
	$15,300 K *

* Reflects transfer of $ 400 K to Mass Storage.

COMMITTED PROJECTS

11/74 MP COMPLETION AND SUPPORT	:	$ 854 K
11/780 SUPPORT, DR780, MA780/750	:	$ 1,226 K
COMET COMPLETION, SUPPORT DR750, BOX, WCS TOOLS	:	$ 3,390 K
SUPPORT FOR 11/05, 35, 04, 34 11/60, 24, 44, 11/70	:	$ 700 K
11/44 COMPLETION	:	$ 860 K
11/24 COMPLETION	:	$ 550 K
COMMON UB EXPANDER CAB	:	$ 100 K
	:	$ 7,680 K

NEW DEVELOPMENT PROJECTS

NEBULA + NEW I/O **	:	$ 2,505 K
11/780 AND COMET WARM EXTENDED *	:	$ 120 K
FLOATING POINT RANGE		
		$ 2,625 K

* $300K Additional of Product Line Funding

** Includes funding for all LEM Power Supply Development which was was common to NEBULA, 11/24 and MINNOW

DON'T GET PROJECTS

11/780		
	DUAL 780 ON SBI	$ 150 K
	STANDARD DISK INTERFACE	$ 150 K
	HIGH PERFORMANCE TAPE INTERFACE	$ 250 K
COMET		
	SECOND UBA	$ 180 K
11/780 AND COMET		
	COMMERCIAL INSTRUCTION SET ENHANCEMENTS	$ 250 K
NEBULA		
	MOVE SCHEDULE IN BY ONE QUARTER (I.E. Q4 FY80/Q1 FY81)	$ 300 K
11/24	DISCRETE PAX	$ 400 K
11/44	HOT FLOATING POINT	$ 500 K
11/XX	EARLIER (FY82)	$ 650 K
	NEW 5 1/4" BOX:	$ 500 K

FY81 BUDGET

PRODUCT SUPPORT AND ENHANCEMENTS		: $ 4,450K
11/74 MP	: $ 250K	
11/780	: $ 300K	
COMET	: $2,500K	
11/44	: $ 200K	
11/24	: $ 200K	
11/04,34,60,70,24,44	: $1,000K	
MAJOR NEW PROGRAMS		: $ 8,500K
NEBULA (UNIBUS)	: $1,200K	
NEBULA (NEW I/O)	: $1,600K	
ICCS/DEVICE CONTROLLERS	: $3,000K	
PDP-11/XX	: $ 600K	
LSI VAX	: $ 100K	
COMET II	: $2,000K	
ADVANCED DEVELOPMENT		: $ 1,900K
PRODUCT MANAGEMENT		: $ 1,250K
SYSTEM PERFORMANCE		: $ 250K
PACKAGED SYSTEMS		: $ 650K
CONTINGENCY		: $ 1,000K
		$18,000K

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FY82 BUDGET

PRODUCT SUPPORT AND ENHANCEMENTS		: $ 3,050K
11/74 MP	: $ 250K	
11/780	: $ 300K	
COMET	: $ 1,000K	
11/04,34,24,44,60,70	: $ 1,000K	
NEBULA	: $ 500K	
MAJOR NEW PROGRAMS		: $11,500K
ICCS/DEVICE CONTROLLERS	: $ 2,500K	
NEBULA FOLLOW ON	: $ 2,000K	
11/XX BASED ON JAWS/L70	: $ 1,000K	
LSI VAX	: $ 1,000K	
COMET II	: $ 4,500K	
ADVANCED DEVELOPMENT		: $ 2,000K
PRODUCT MANAGEMENT		: $ 1,350K
SYSTEM PERFORMANCE		: $ 500K
PACKAGED SYSTEMS		: $ 600K
CONTINGENCY		: $ 1,500K
		$20,000K

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IV. NON PRODUCT DEVELOPMENT

A. Product Support Strategy

The strategy is to NOT offer new peripherals for cpu's which have been replaced by a new offering. Selective addition of new peripherals to older machines might be required; this should be done on a case by case basis only.

64K chip based memory systems are not planned for the 11/70, 11/780; we have assumed that replacement products (VENUS in FY82 and PDP-11/XX in FY83) would be used instead; i.e. the 64K chip memory would be justified on the 11/70 and 11/780 only to cost reduced them and would arrive too late in the life cycle to be effective). See Section III for details on support costs.

B. Advanced Development

FY80 ($ 885K)

Under the assumption that SSE will be developing the chip sets for our next generation products i.e., JAWS-11 and LSI-VAX, our effort in FY'80 will be directed in the following areas:

1. Support SSE to ensure applicability of their products to our system needs. This support will also aid in the transfer to MSD for our future use of the CAD tools and design methodology developed for these programs.

2. Develop system architectures around these chip sets for products that make us leaders in the single user scientific computer market as well as in distributed processing networks.

3. In developing the above systems we will pay special interest to the following areas:

   I/O Architecture
   Memory Hierarchies (both in structures and device utilization)
   Physical Integration
   Manufacturability
   Field Installation and Service
   Software Applicabiliity

4 Study of Semiconductor Technologies for various cost/performance trade-off relative to different size machines. A determination of the appropriate solution for the COMET replacement; is it gate arrays or custom, HMOS, I^2L, ECL, or schottkey TTL?

5 Study of the power & packaging technologies of bounded systems. (i.e. the integral packaging of CPU's perpherials, comm gear etc..) Evolution from modules, backplanes, interconnections racks, boxes, cabinets that improve the overall packaging density of complete systems.

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6 The study of diagnostics, RAMP, fault-tolerent, self-repairing philosophies to enhance the maintainability and availability of systems.

7 Tools development in process, that allows the flow of product development from design and straight into manufacturing process tools. (SUDS.SAGE.IDEA.ER)

FY81 ($1,900K)

1. Continued development of system oriented products with special emphasis on potential special products such as Data Base and Array Processors.

2. Migration of VLSI technology and CAD tools into MSD products.

3. Investigation of exotic power system and packaging techniques for use on the next generation of VLSI products.

Based upon the initial studies started in FY'80 one could see work occurring in some specific areas i.e.

- Examination of MOSAIC-II or alternatives
- Refrigerated packaging schemes
- Migration tools to VAX

which would lead to advance product development, such as:

- CCD/BUBBLE low cost store for VMS (Architectural/Firmware solution)
- Fiber Optics Link and Switch exchange for ICCS

V. ISSUES AND CONCERNS

- Stability of the strategy.

- High dependency on Mass Storage devices in order to provide cost/performance effective systems.

- Availability of new parts such as 64K memory chips and PAL for NEBULA.

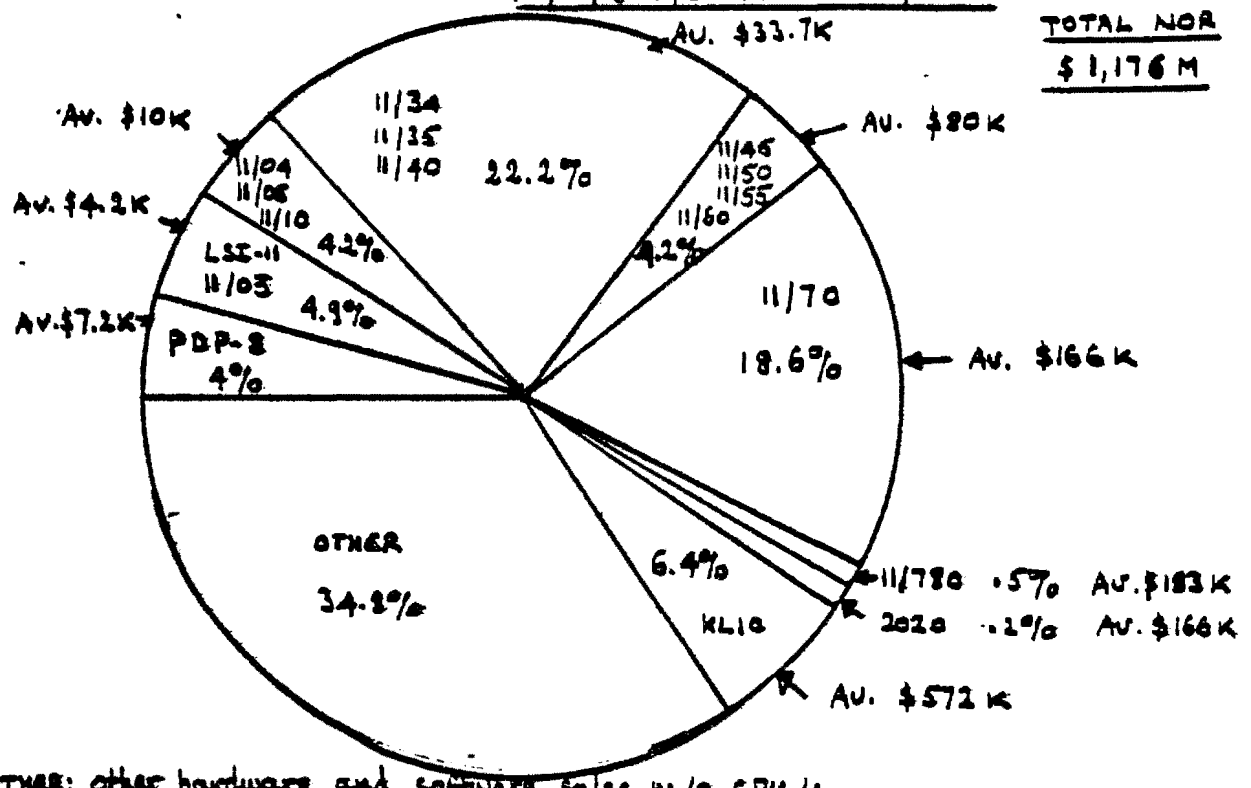
- Management of the New I/O Interconnect Architecture (coordination and agreement of the many groups involved in making the undertaking successful; mass storage, terminals, communication, software).

- High dependency on a single O.S. for VAX and availability of VMS resources.

- We are assuming that the Small Systems Group will be developing the JAWS-11 and LSI-VAX Chip Set.

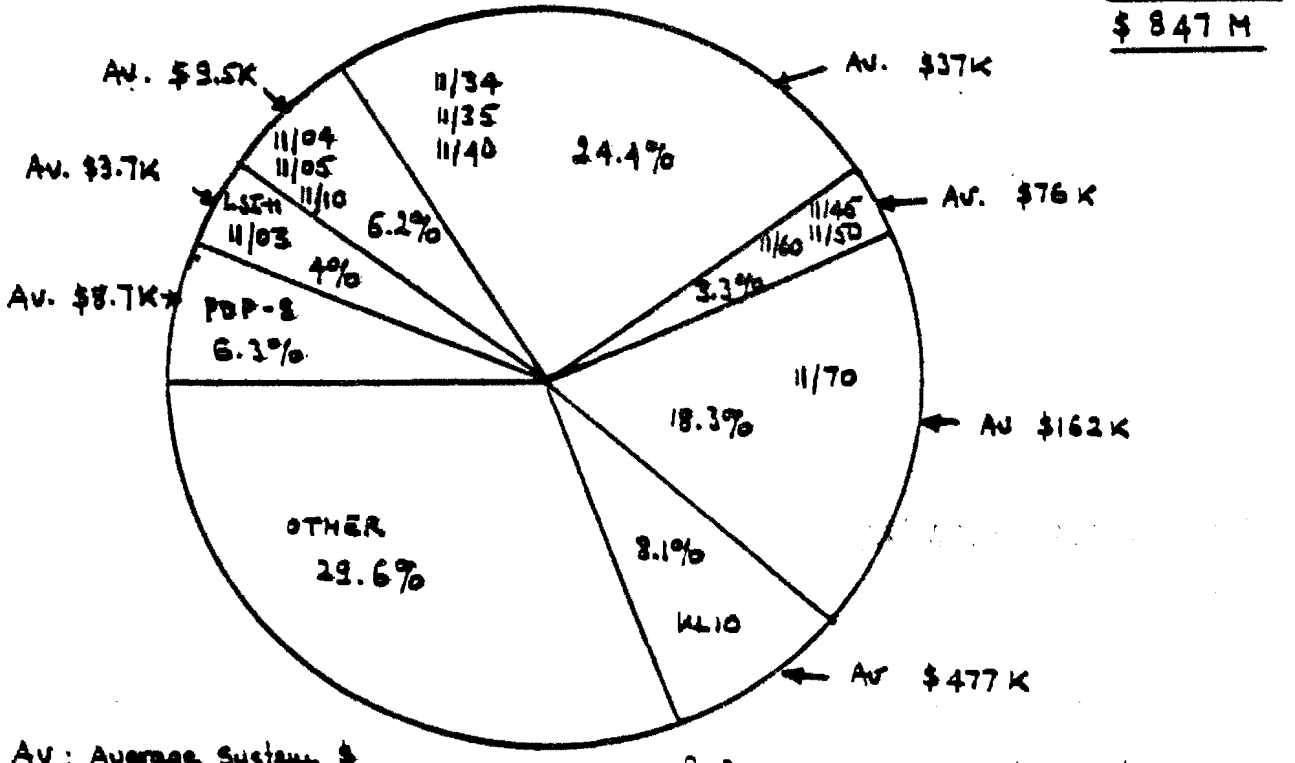
- Depending on cost/performance effective communication hardware and software for distributed, commercial and scientific processing.

FY 78 SYSTEM NOR BY CPU



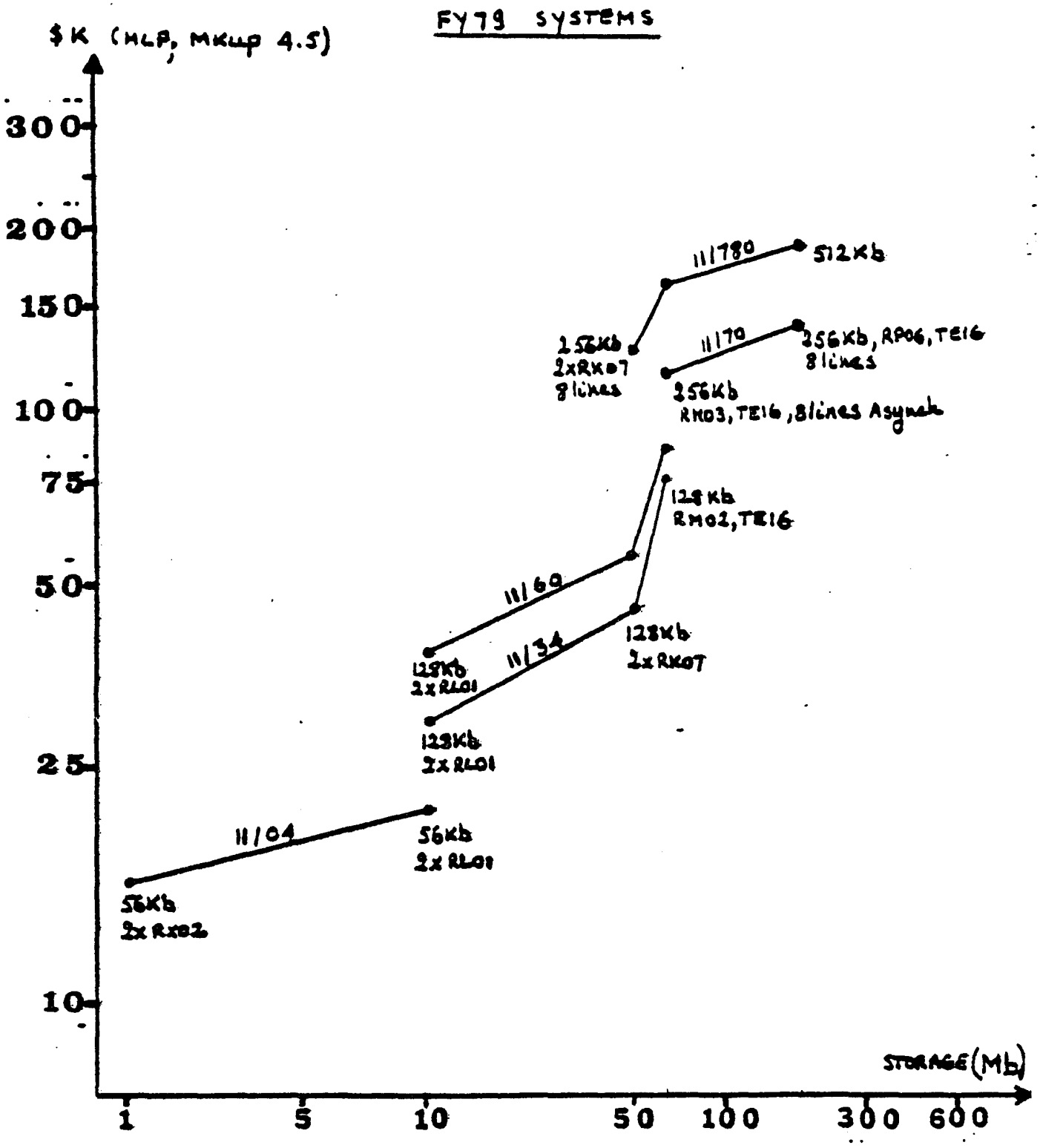
OTHER: other hardware and software sales w/o CPU's.

FY 77 SYSTEM NOR BY CPU



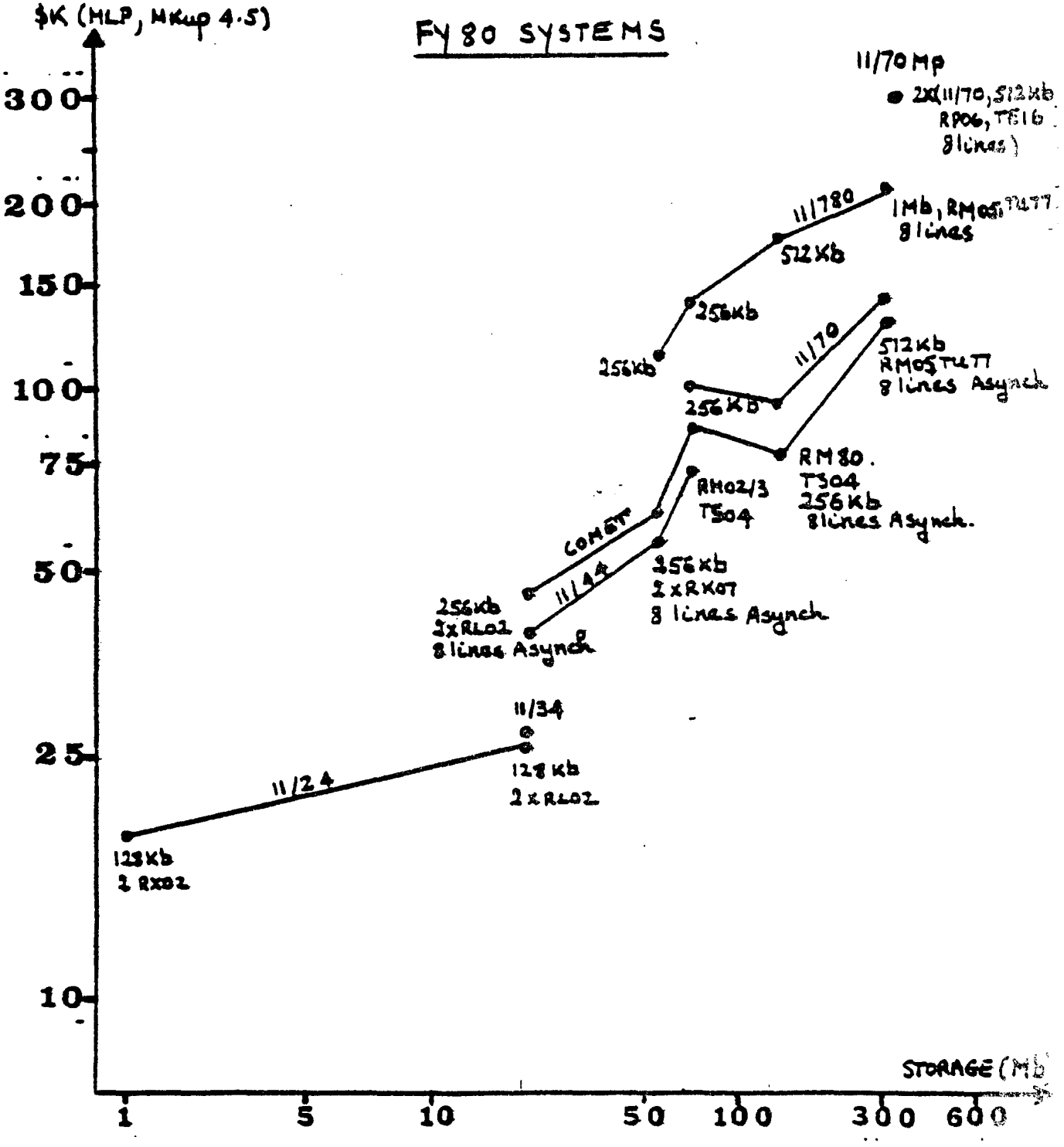
Av: Average System $
NOR: NOR generated by system and options which are on same purchase order

FY79 SYSTEMS

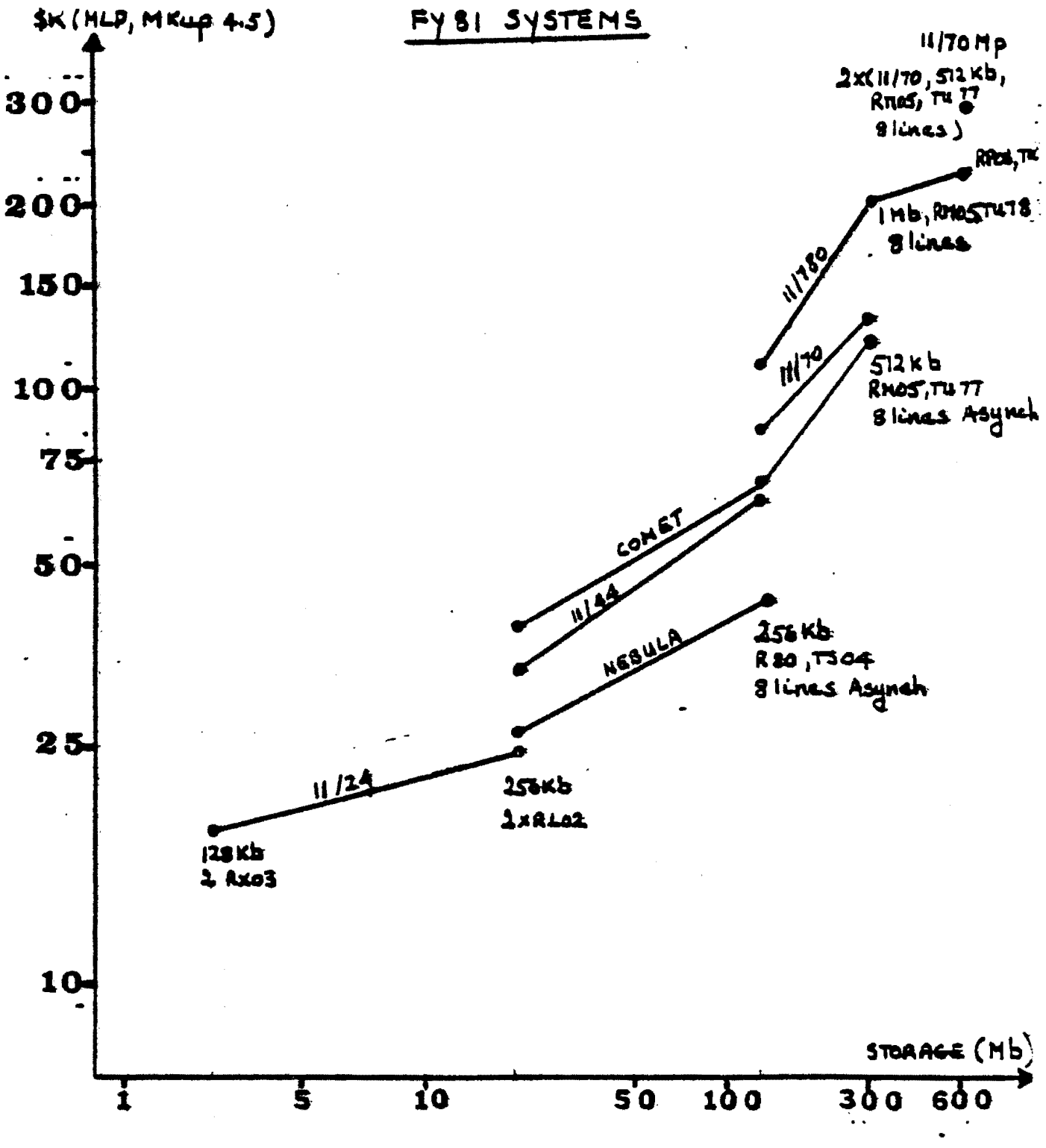


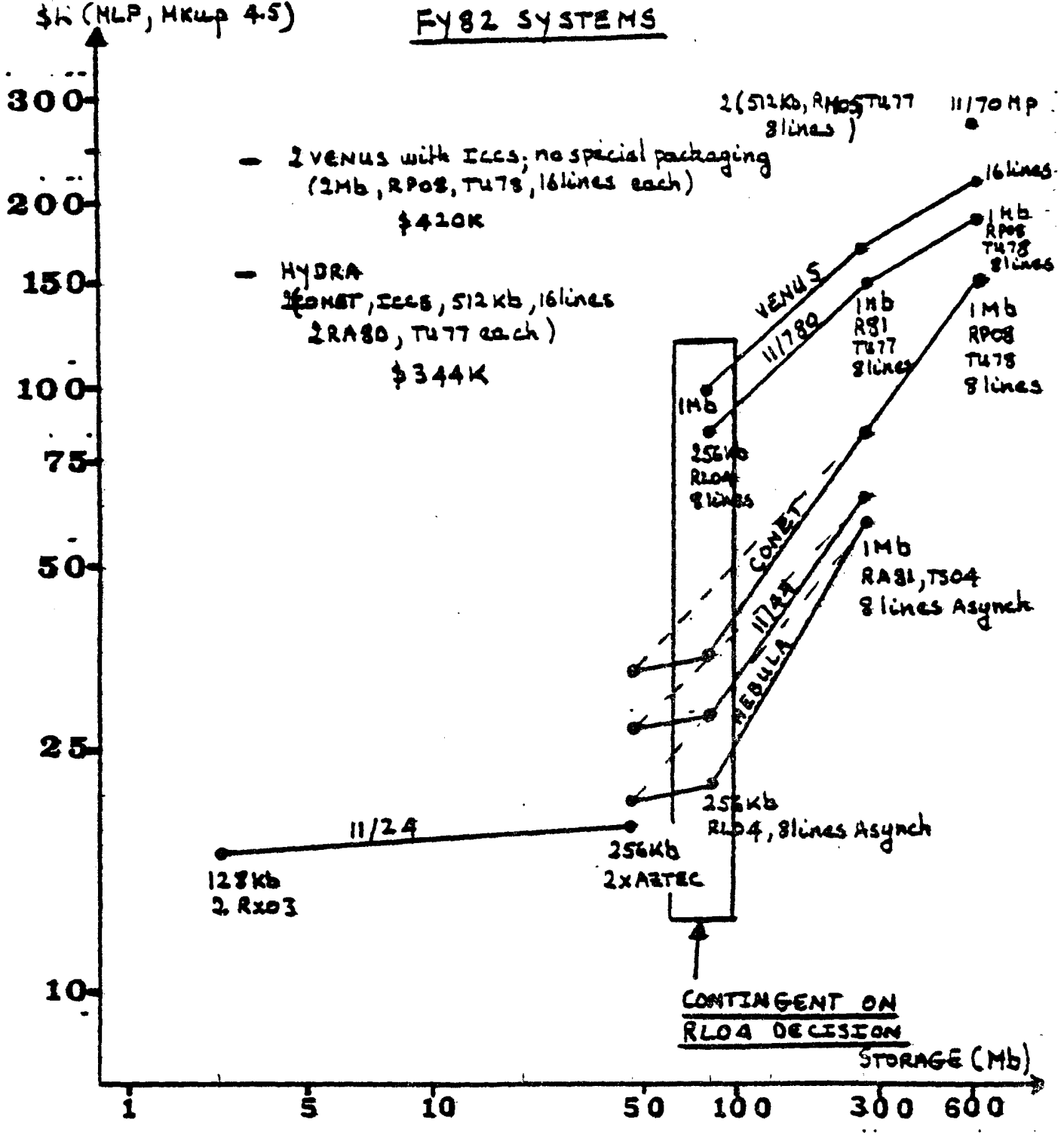
- Note: No Software included
- MKup standardized at 4.5

FY 80 SYSTEMS



• Assumed 10% Reduction in xfer cost


$K (MLP, MKup 4.5)
FY 81 SYSTEMS
300
200
150
100
75
50
25
10
1
5
10
50
100
300
600
STORAGE (Mb)
11/70 Mp
2x(11/70, 512 Kb, RM05, TU 77
8 lines)
RM05, TU
1 Mb, RM05 TU78
8 lines
11/780
11/70
512 Kb
RM05, TU 77
8 lines Asynch
COMET
11/44
NEBULA
256 Kb
R80, T304
8 lines Asynch
11/24
256Kb
2xRL02
128 Kb
2 Rx03


$K (MLP, MKup 4-5)
FY82 SYSTEMS
300
200
150
100
75
50
25
10
1
5
10
50
100
300
600
STORAGE (Mb)
2 (512Kb, RM05, TU77, 8 lines)
11/70 MP
- 2 VENUS with Iccs; no special packaging (2Mb, RP08, TU78, 16 lines each)
$420K
- HYDRA
CONET, Iccs, 512 Kb, 16 lines
2 RA80, TU77 each)
$344K
VENUS
11/780
16 lines
1Mb
RP08
TU78
8 lines
1Mb
RP08
TU78
8 lines
1Mb
RA81
TU77
8 lines
1Mb
RL04
8 lines
CONET
11/785
HEBULA
1Mb
RA81, T504
8 lines Asynch
256Kb
RL04, 8 lines Asynch
11/24
128Kb
2 Rx03
256Kb
2 x AZTEC
CONTINGENT ON
RL04 DECISION

digital

INTEROFFICE MEMORANDUM

TO: DISTRIBUTION

DATE: June 25, 1979
FROM: Anne Toth
DEPT: LSG Product Management
EXT: 231-6119
LOC/MAIL STOP: MR1-2/E78

SUBJ: RED BOOK, ENCLOSURE

Enclosed find the Spring 1979 Draft Red Book. Due to recent major shifts in the strategy, it was not possible to produce the final document at this time. Sections on VENUS 32, 2080, Communications and Peripherals will be supplied within a month, along with more detail in existing sections. A cursory review of VENUS 32 is included in the summary, 2080 is included in the DECSYSTEM-20 Section, and Languages for 32-bit Systems is briefly treated in the 36-bit Languages Section.

A chapter describing the changes in strategy from the last Red Book will also be supplied as part of the final Red Book.

Your comments on both the structure and content of this document will be appreciated.

sa
Enclosure

R E D B O O K

S T R A T E G Y

SPRING 1979

D R A F T

TABLE OF CONTENTS

LARGE SYSTEMS GROUP RED BOOK SUMMARY

Charter

Responsible for the development of Digital's high-end 32 and 36-bit system.

Goals

Our goals are to:

a) Maintain large systems focus with 32/36 bit products and distributed systems.

b) Maintain as much as possible of the installed 36-bit base for Digital in a way that makes a contribution.

c) Direct new application large systems customer to VAX.

- larger programs
- price/performance for specific application

d) Maintain 36-bit focus on existing markets.

Strategy

32-bit systems

Provide a VAX 11/780 follow-on system (VENUS-32) to maintain and further expand the installed PDP-11 and VAX base.

36-bit systems

Provide a clear growth path to maintain DEC-10/20 user base satisfaction.

Short Term

Provide a competitive 36-bit product (2080) and peripherals to maintain our customer base, with emphasis on:

- price/performance
- homogeneous networks/interconnect

Long Term

Provide interconnectability to help our customer base grow with 32-bit systems with emphasis on:

- syntactic compatibility of application languages where feasible
- heterogeneous networks for 32/36 bit growth path

The major emphasis will be on interconnect and offering growth through distributed processing.

Markets

32-bit system (VENUS-32)

VENUS-32 will address the following market segments:

1. Scientific Computation
2. Real Time Computation
3. Transaction Processing
4. General Purpose Commercial EDP
5. General Purpose Timesharing

These market segments will be served by the following product lines:

TECHNICAL GROUP:

TOEM:	scientific and real-time computation
LDP:	scientific and real-time computation
MSG:	real-time computation, general purpose commercial EDP
ESG:	general purpose timesharing, scientific computation
ECS:	general purpose timesharing
GSG:	all segments

COMMERCIAL GROUP:

COEM: general purpose commercial EDP
CSI: general purpose commercial EDP, transaction processing, general purpose timesharing
MDC: general purpose timesharing, real-time computation
T&UG: real-time computation, general purpose timesharing, general purpose commercial EDP

36-bit systems

The 36-bit system focus will be on existing markets and in the case of TOPS-10 based systems on existing customers.

The following market segments will be served:

1. Scientific Computation
2. Real-Time Computation
3. General Purpose Timesharing

These market segments will be served by the following product lines:

TECHNICAL GROUP:

LDP: Scientific and real-time computation
ESG: General purpose timesharing, scientific computation
ECS: General purpose timesharing
GSG: General purpose timesharing

COMMERCIAL GROUP:

CSI: General purpose timesharing
MDC: General purpose timesharing

6/25/79 1.45

BUDGET SUMMARY

		ESTIMATES	
32 BIT	FY80	FY81	FY82
VENUS	$3.9M	$5.5M	$4.0M
32 SOFTWARE	.4M	.7M	1.5M
COMPUTERS	.7M	.9M	1.1M
ADMIN	.25M	.45M	.55M
PRODUCT MGMT	.24M	.30M	.35M
R&D (H/W & S/W)	.4M	.8M	2.0M
CONTINGENCY	.5M	1.0M	6.5M
SUBTOTAL	$6.4M	$9.65M	$16.0M
36 BIT			
2080	$1.6M	$2.8M	$2.5M
KL SERVICE	1.0M	1.0M	--
KL,KS,H/W	1.0M	1.1M	1.2M
SOFTWARE	3.0M	3.5M	3.0M
COMPUTERS	1.5M	1.6M	1.8M
ADMIN	.2M	.2M	.25M
PRODUCT MGMT	.24M	.3M	.35M
CONTINGENCY	--	.40M	1.0M
SUBTOTAL	$8.6M	$10.90M	$9.9M
TOTAL 32 + 36	$15.0M	$20.55M	$26.4M

FY80 BUDGET

- 32 BIT	$ 6,400
- 36 BIT	8,600
TOTAL (OOD)	$15,000

32 BIT FY80 BUDGET STATUS

VENUS 32	$3,905K
32 SOFTWARE	405K
COMPUTERS	700K
ADMIN	250K
PRODUCT MGMT	240K
R & D (H/W + S/W)	400K
CONTINGENCY	500K
TOTAL	$6,400K

FY80

SOFTWARE 32-BIT BUDGET

PROJECT	
APL	$167K
APL TEST SYSTEM	75
APPLICATION PROGRAMMER WORK STATION	163
TOTAL	$405K

36-BIT BUDGET

PRIORITIES

1. KL RAMP
2. INTERCONNECT
3. 2080
4. SUPPORT CURRENT PRODUCTS
5. STAY COMPETITIVE
6. NEW FEATURES

FY80

KL MAINTAINABILITY

TECH DOC	$ 68K
DIAGNOSTICS	121K
HARDWARE + ECO	332K
SUBTOTAL H/W	521K
RSX20F	182K
TOPS-10 7.01	132K
TOPS-20 REL 4	157K
TOPS-20 REL 5	76K
SUBTOTAL S/W	547K
TOTAL KL MAINTAINABILITY	$1068K

FY80

TOPS-20 BREAKDOWN

EXCL. COMPUTERS

RELEASE 4 MONITOR	$ 253K
LOOSELY COUPLED SYSTEMS	720
RELEASE 4 DECNET	70
RELEASE 5 DECNET	103
IBM COMM.	72
TOTAL	$1218K

FY80

TOPS-10 BREAKDOWN

EXCL. COMPUTERS

TOPS-10 7.00	$100K
TOPS-10 7.01	260K
TOPS-10 7.00/7.01 COMM.	205K
TOPS-10 IBM	72K
SUBTOTAL	$637K

FY80

LANGUAGES 36 BIT BUDGET

EXCL. COMPUTERS

PROJECT		
APL-V2/V3	(V.2)	--
APL TEST SYS.		--
DBMS V6/V7	(V.6)	294
MACRO/LINK V5/V6	(V.5)	62
COBOL 79		--
COBOL 68/74 V12A/V13		264
FORTRAN 78		193
BASIC +2 V3		--
PROG. W/S V1		--
BLISS-36		--
AUTOPATCH V1/2		138
UETP V2		--
REL. ENGR.		195
BENCHMARKS		--
TOPS-20 SIMULATION		--
TOTAL		$1146K

FY80

HARDWARE

QUALIFICATIONS	24
REL 4/7.01 COMM.	53
PROD. SUPPORT	459
INT'L REG.	24
1090 MOS	--
MX20	--
MCA TECHNOLOGY	--
DOLPHIN 36	--
MASS STORAGE	323
MF20 EXT. ADDON	100
TOTAL	983

6/22/79 10/1.47

36 BIT FY80 BUDGET STATUS

($K)

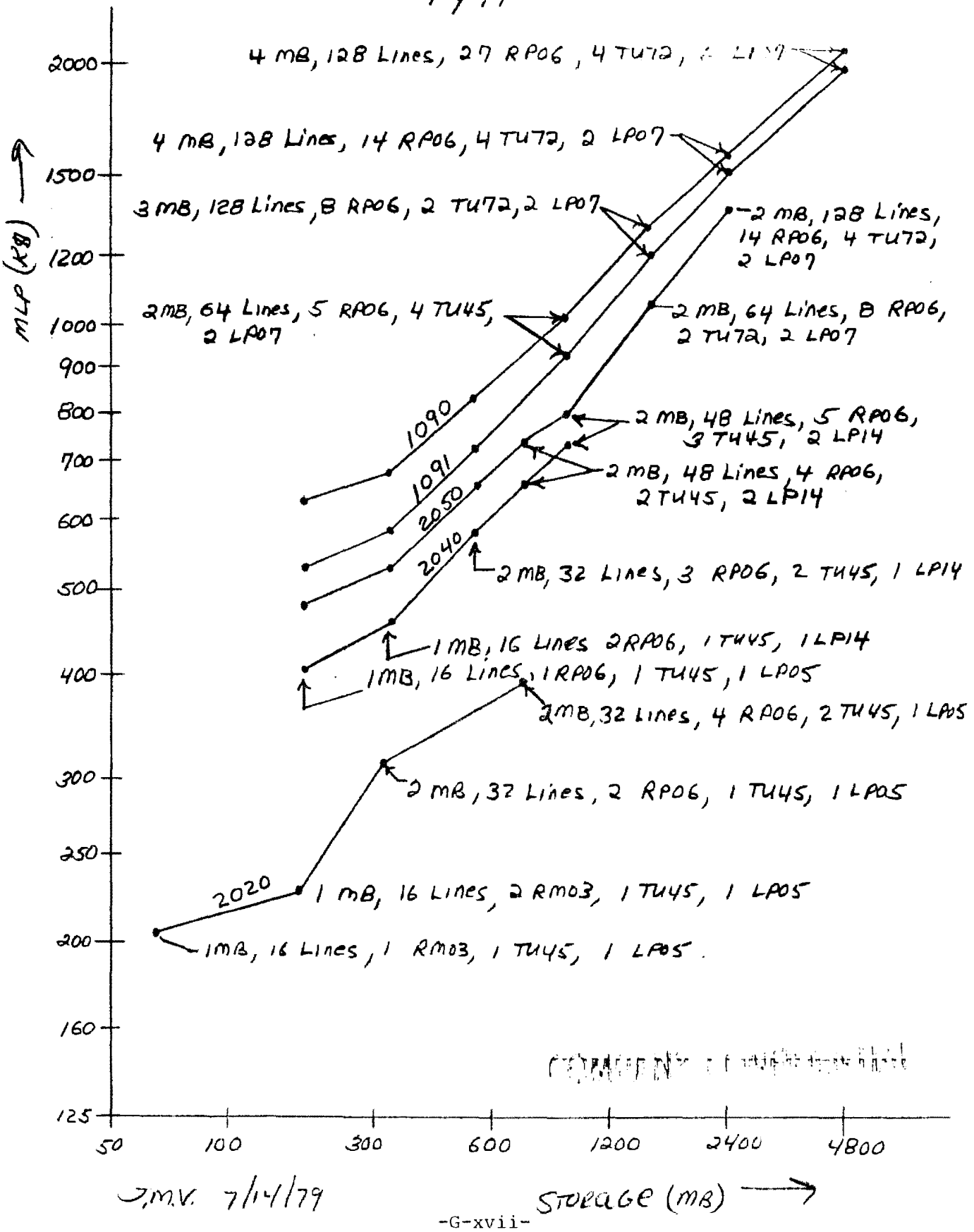
KL SERVICE	$1068
KL/KS H/W SUPPORT	983
SOFTWARE	3001
2080 (KL+) INCL. S/W	1538
COMPUTER LAB	1570
ADMINISTRATION	200
PRODUCT MANAGEMENT	240
CONTINGENCY	---
TOTAL	$8600

36-BIT HARDWARE

OUT

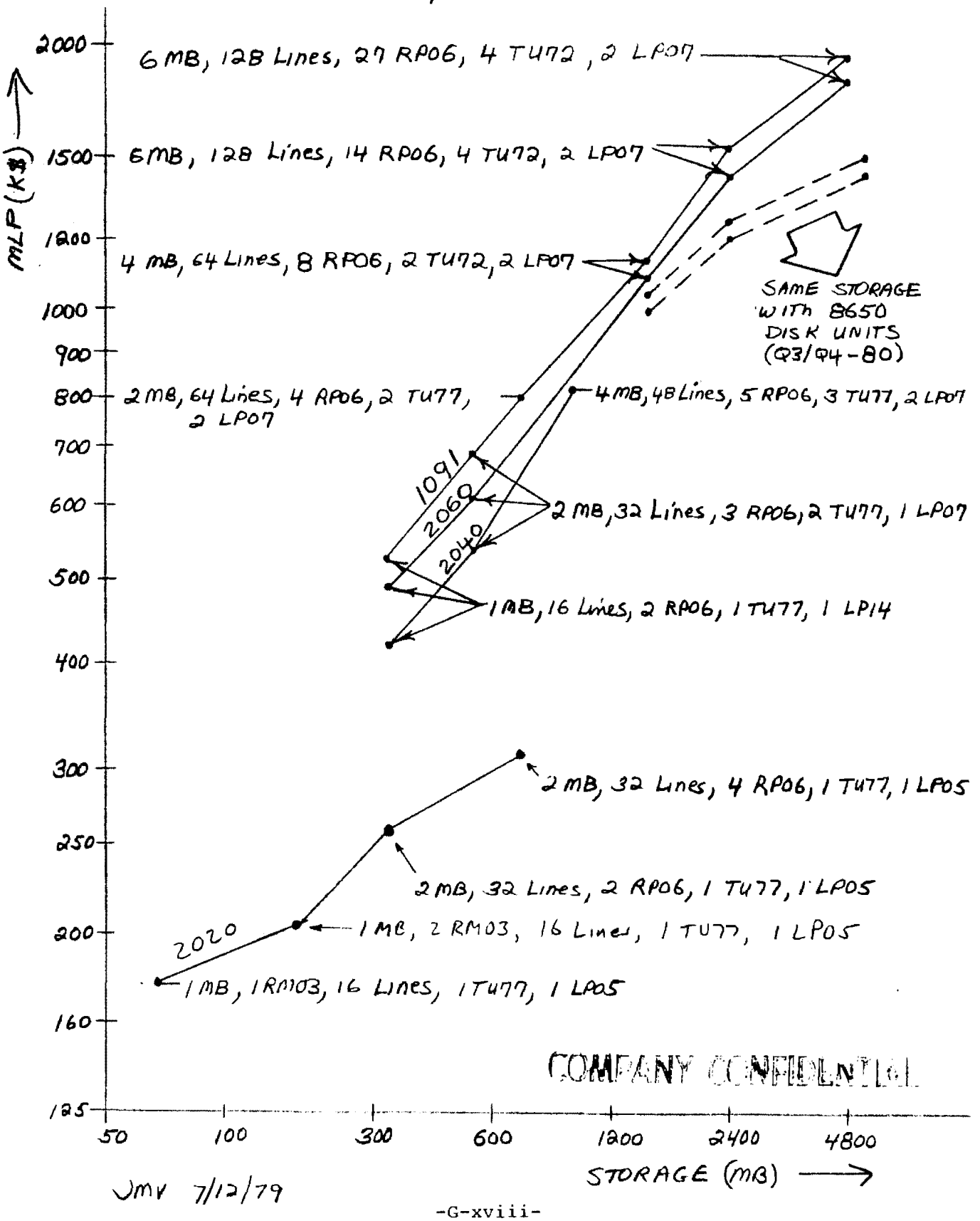
MX20	$206K + $200K COMPUTERS
MOS ON 1090	105K
VT132, 162	11K
DOCUMENTATION	64K
RM80	42K

FY 79



J.M.V. 7/14/79

FY80



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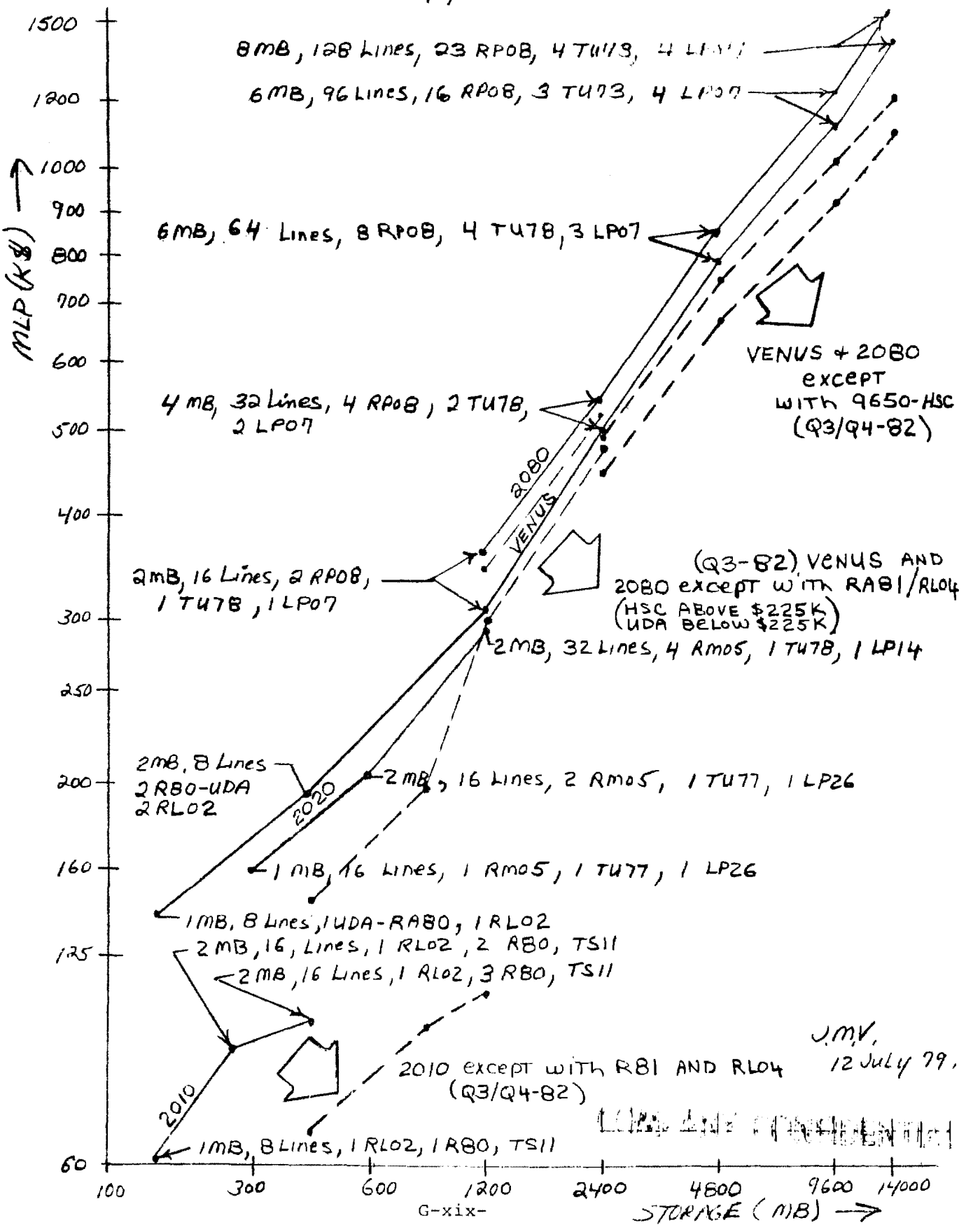

FY82
MLP (K$)
1500
1200
1000
900
800
700
600
500
400
300
250
200
160
125
60
100
300
600
1200
2400
4800
9600
14000
STORAGE (MB)
8MB, 128 Lines, 23 RP08, 4 TU78, 4 LP07
6MB, 96 Lines, 16 RP08, 3 TU78, 4 LP07
6MB, 64 Lines, 8 RP08, 4 TU78, 3 LP07
4 MB, 32 Lines, 4 RP08, 2 TU78, 2 LP07
VENUS + 2080 except with 9650-HSC (Q3/Q4-82)
2080
VENUS
2MB, 16 Lines, 2 RP08, 1 TU78, 1 LP07
(Q3-82) VENUS AND 2080 except with RA81/RL04 (HSC ABOVE $225K UDA BELOW $225K)
2MB, 32 Lines, 4 RM05, 1 TU78, 1 LP14
2MB, 8 Lines 2 RB0-UDA 2 RL02
2020
2MB, 16 Lines, 2 RM05, 1 TU77, 1 LP26
1MB, 16 Lines, 1 RM05, 1 TU77, 1 LP26
1MB, 8 Lines, 1UDA-RA80, 1 RL02
2MB, 16, Lines, 1 RL02, 2 RB0, TS11
2MB, 16 Lines, 1 RL02, 3 RB0, TS11
2010 except with R81 AND RL04 (Q3/Q4-82)
2010
1MB, 8 Lines, 1 RL02, 1 RB0, TS11
J.M.V.
12 July 79.

1.0 DECsystem-10 STRATEGY

D R A F T

DECsystem-10 RED BOOK STRATEGY

A. PRODUCTS/CHARTER

The DECsystem-10 is Digital's largest system both in configuration size and capacity. It is a general purpose interactive system which has mature software, namely TOPS-10. This operating system is available on the following system types:

1090
Dual 1090
1091
2020

The charter for the DECsystem-10 is to continue to serve its present customer base. It will continue to share compatible software with the DECSYSTEM-20 and offer increased capacity in the future with the 2080.

B. STATUS

1. Present Markets -

The DECsystem-10 is active in all Digital markets except for OEM's.

Education Market - The approachability and interactive nature of the DECsystem-10's provide an excellent learning environment for the students. University administrations find TOPS-10's ease-of-programming, capacity and batch processing facilities well suited to their needs.

Scientific and Engineering Markets - TOPS-10 has real time support for data collection and data analysis. It offers favorable FORTRAN and APL functions for arithmetic processing. The interactive timesharing characteristics of TOPS-10 facilitates program development. The availability of Engineering-specific applications software makes the DECsystem-10 family highly competitive engineering data processing systems.

Financial and Commercial Markets - Commercial data service companies rely upon the timesharing capacities of TOPS-10 for their business. TOPS-10's ability to support remote data entry devices and to communicate with other systems makes it invaluable to geographically dispersed manufacturers and retailers.

Federal Government Market - The ease of programming and interactive nature of TOPS-10 make it very attractive to many government agencies. Their programming staff are able to develop advanced networks under TOPS-10, a feature which is not available from any other vendor.

The flexibility of TOPS-10 is a feature which many customers employ to enhance, create, configure and design special purpose systems. Customers in different DEC markets have built their own transaction processing systems which provide them with a competitive edge. The ability of TOPS-10 to run on DECSYSTEM-20 hardware such as the 1091 and the 2020 combines the best advantages of mature software and new hardware.

2. Product/Market Coverage -

The DECsystem-10 customers' growth requirements are such that they are looking for twice the capacity in 3-5 years. More than half of these customers own KL based systems. They can be offered increased capacity through symmetric multi-processing (SMP) and within the next three years, the 2080 and loosely coupled systems via the InterComputer Connection System (ICCS).

Today, the 1091 is offered as a growth path for customers interested in hardware consolidation and long term investment in Digital Products.

The 2020 running TOPS-10 is an attractive offer to customers who have invested in a large-10 and need distributed computing power which can interact with their central system.

The DECsystem-10 family of products will be aggressively marketed to existing customers and markets. Factors which enhance the market edge for DECsystem-10's are:

- The Corporate commitment to DECnet will be part of TOPS-10 development.
- TOPS-10 and TOPS-20 will have joint language development.

3. Active Projects -

Symmetrical Multiprocessing (SMP) (KL10-D only)
Mountable Device Allocator (MDA)
Tape Labeling (ANSI recognition)
DECsystem-10 Network Communications on 2020
1091 MOS Memory
DX20/TU70/TX02/TX05 on 1090 internal channels
TU77 on KL10 and KS10
Multipathing on DECsystem-10 networks
High Density Fixed Media Disk (KL10 and KS10)
GCR Tape Drives
KL Replacement (2080)
Total DECNET Certification
Reliability requirements (Service Enhancement Project, Section 5.2)
Performance Tools
No KA Support V. 7.01
No KI Support V. 7.02

Product Schedule

		Release
1.	Provide support for MF20 Memory on 1091 KL10-EH + MF20-LM (+LK) KL10-EC + MF20-LC	7.01
2.	Provide suppport for ANF-10 on the 2020.	7.01
3.	Provide for support of ANSI Tape Label recognition.	7.01
4.	Provide for support of Mountable Device Allocator (MDA) as per University of Oslo specification.	7.01
5.	Incorporate reliability functions according to LSG Service Enhancement Project.	7.00/ 7.01/ 7.02
6.	Last KA Release	6.03A
7.	VT100 Support	7.02
8.	Support TU78 on KL10's.	7.02
9.	Provide console FE Support on 1090 a la TOPS-20	7.02

10.	Incorporate GALAXY Version 4.	7.01
11.	Upward compatability with previous Rel. 6.03A when connected in DECsystem-10 networks.	7.01/ 7.02
12.	The next release of TOPS-10 will be the last release for KI's (single and dual)	7.01
13.	Retain hooks for DA28 within TOPS-10	7.01

4. Projects Funded/Inactive

5. Present Funding

C. ENVIRONMENT

1. Marketplace - Installed Base - The current market is moving toward larger and larger configurations. The suppliers of plug compatible peripherals have been very successful in offering lower priced hardware to meet this need. DEC is meeting the market requirements for disbursed computation, remote job entry, terminal concentration, and networked central processors DECsystem-10 network communications.

   Approximately 30% of our present customer base consists of KA and KI installations. They have made a significant investment in TOPS-10 and the DECsystem-10 hardware. We can now offer them a near term growth path to the 1091 or the single or dual processor 1090. Today, there is no clear path from the DECsystem-10 family to the VAX/VMS group of products. This is a critical problem affecting both DECsystem-10 and DECSYSTEM-20 families. Our customers are understandably wary. DEC's intentions and strategies must be clearly and very carefully communicated in a very timely manner.

2. Competition -

   Digital continues to share the market with IBM. So far, we have successfully competed with our lower prices. However, their recent 4300 family announcement is extremely price competitive from the hardware perspective. Nevertheless, on a systems price basis, Digital still has the edge. Our products provide more capacity, better interactive computing, lower cost communications, software, and support.

The larger mini-computers on the market today provide LSG's customers with attractive alternatives. 32-bit systems, including the VAX, provide number crunching, real time functions at a price which cannot be matched by the KL or KS.

3. Technology -

The technology level for components of KL10 and KS10 based systems are uneven. This is because they were not developed on a systems level; rather, each component was developed somewhat independently and later assembled into a system. Some resultant problems are 1091's or 2020's are configured with non-competitive mass storage devices. Requirement to configure tapes on a system as a media exchange for software and diagnostics places the 2020 at a disadvantage in the entry level marketplace.

The relationship between price and technology also poses an issue for DEC. IBM sells memory at $15,000 per megabyte. We currently market memory at $70,000 per megabyte.

In order to protect our installed base, the next DEC-10 machine (2080) must include advances in total system design for availability, maintainability and performance.

D. STRATEGY

1. Market Strategy -

1.1 Short Term Strategy

- Stabilize software development for KA and KI based systems. These actions will allow us to concentrate our resources on the KL.
- Announce symmetric multi-processing for 1090 systems. Emphasize capacity, performance, availability, and lower operation costs.
- Announce network support under the 2020. Emphasize distributed computing, source development, and network capabilities.
- Capitalize on mature software.
- Focus on optimized configurations, namely the 1091 for upgrades and the 2020 for distributed processing.

- Focus on present features and future trends under TOPS-10 such as distributed processsing, language transportability, and communications compatibility.

1.2 Long Term Strategy

- Provide for 1090 and 1091 growth with loosely coupled systems using the ICCS.
- Provide for TOPS-10 and TOPS-20 interconnect.
- Focus on TOPS-10 to VMS interconnect to provide both growth and coexistance with VMS-based systems.
- For the 2080, implement networking and interconnect in loosely coupled networks.
- Over 70% of the currently installed LSG base is TOPS-10. We must protect this very loyal base and make it clear that we are not forcing them to convert to VMS. The key word in the long term strategy should be co-existence. The corporate strategy to develop systems interconnect facilities reinforce the feasibility of continuing with TOPS-10 interconnected with VMS and other systems.

2. PRODUCT DEVELOPMENT STRATEGY

2.1 Short Term Strategy - The next release of TOPS-10, V. 7.00, will support symmetric multiprocessing (SMP). The target date of this release is Q2 FY80. It will be available to presently dual KL sites who need to increase their systems capacity. Briefly, SMP is software which will support two KL10 processors sharing memory, mass storage and communication front ends. They will use a single re-entrant monitor. RAMP features will also be part of this release. TOPS-10 V. 7.00 will only be available to presently dual KI or KL sites.

A general release of TOPS-10 which will have the SMP facility in it is Version 7.01. The target date is Q4 FY80. TOPS-10 Version 7.01 will be the last TOPS-10 to support KI based systems. For KL based systems, there will be at least one more release of TOPS-10, namely Version 7.02. The fact that we will be distributing two major releases within the next two years substantiates our commitment to the TOPS-10 customer base.

Further evidence of our continued support for TOPS-10 customers is the planned inclusion into TOPS-10 V.7.01 of DECsystem-10 network communications for the 2020. This release is compatible with the corporate strategy to emphasize distributed processing. TOPS-10 sites can decentralize and protect their software investment with a low cost system.

-10 7.01 will support MOS memory on the 1091. This product relieves the lack of core memory and is a direct response to the 4341 attacks on the -10 installed base.

2.2 Term Strategy -

- Fulfill commitments to present customers.
- Protect present market share.
- Software compatibility with other systems.
- Systems interconnect.
- Improved hardware technology.

3. ASSUMPTIONS

- No major strategic changes in the next 5 years.
- TOPS-10 will run on 2080.
- DEC will make it possible and appealing for installed DEC-10 sites to include VMS.
- SMP will be tested to run on two processors only.
- KI's and external memory bus devices stabilized on 7.01.
- TOPS-10 Release 7.02 will run on KL10, KS10, only.
- New developments for hardware support after 7.01 (disk, tapes, memory, multiport).
- By 1985, VMS will fulfill the requirements for a large operating system.

4. RISKS

- o TOPS-1Ø user may not choose to invest in other DEC products.
- o Growth in system capacity may not be adequate.
- o Technology advances may reduce the competitiveness of DEC-1Ø products.
- o Development time may miss market opportunity.
- o VMS will not meet market requirements and/or hardware specifications by 1985.

2.0 DECSYSTEM-20 STRATEGY

DECSYSTEM-20 RED BOOK STRATEGY

A. CHARTER AND GOALS

1. CHARTER - The DECSYSTEM-20 is DEC's high-end family of multi-purpose timesharing systems ranging in price from $200,000 to $2 Million and ranging in performance from 400 KIPS to 2,000 KIPS. The products in this space are the 2020, 2040, 2060 and 2080 all running TOPS-20.

2. GOALS - To meet our customers needs while maintaining a 20% profit contribution.

   a. Keep all DEC-20 customers for DEC.

   b. Develop 40% per year add-on business from existing customer base.

   c. Grow customer base by 20% per year to targeted customer.

   d. Sell a combination of 20's, VAX's, and 11's to customers.

B. STATUS:

1. Present Markets: The DEC-20 is following the leadership of the older DEC-10 products in five markets.

   a. Educational, scientific, and general purpose timesharing in universities and colleges. The DEC-10/20's are #1 in large system, instructional timesharing.

   b. Commercial timesharing service bureaus. The DEC 10/20's have 20% of this market.

   c. The DEC-2020 coupled with the MARS application package is selling well as an administrative system for small public school districts.

   d. Commercial-end-user in-house timesharing. DEC-20's are being bought to replace outside timesharing services.

   e. Government in-house timesharing.

2. Product Market Coverage:

a. Educational Timesharing Market - The DECSYSTEM-20's strengths in this marketplace are its reliable hardware and software and easy-to-use, easy-to-learn and easy-to-operate software which allows inexperienced users, typical in education, to use the system.

The major weakness in this market is the price/performance ratio. Systems must be able to perform well with large numbers of attached terminals. The TOPS-20 system cost-per-terminal is higher than TOPS-10 cost-per-terminal. Thus TOPS-20 does not attract TOPS-10 customers. It is hoped that the expanded MOS memory capability will address this problem. The 2080 and multiprocessors with shared peripherals and a single interface to users could also address this weakness.

At the low end, the 2020 cost-per-terminal is too high. Therefore, the 2020 does not effectively compete in this market.

b. Commercial Service Bureau Masrket - Strengths - Same strengths as above. Weaknesses - This market requires very competitive hardware. The DEC-20 typically was lower priced than IBM in this market, but today, the DEC-20 is barely at price parity with the IBM 4300 in an interactive environment. This marketplace has a need for a configured-system priced in the $50K to $150K range with mainframe functionality. The MINNOW addressed this marketplace, but with the cancellation of that product, a cost reduced 2020 could perhpas fulfill this market requirements. If not, we may loose this market.

c. Educational Administration in Public School Districts Market - Same strengths as above. The 2020 with the MARS application package meets the needs of this market. (U.S. only)

d. Commercial End User Market - Building on our leadership in large-scale multi-purpose timesharing and our strength of reliable, easy-to-use systems, the DEC-20 is successful in the Commercial market as a large in-house timesharing system supporting analysis, forecasting, modeling and software development. Our CODASYL standard DBMS puts us in a good position in this market. The product weaknesses are:

1. Distributed data management capability which will allow users simple access to data libraries (tape and disks) located at dispersed processor sites.

2. Transaction processing and message handling.

3. Graphics and intelligent terminal capabilities.

3 - 5. Active/Inactive Projects and Funding: See Attached

C. ENVIRONMENT:

1. Marketplace - Present Trends

a. Users are becoming more dependent on computers. Reliability and response time are becoming even more important to customers.

b. Staff to support the hardware and software is more expensive than the cost of the hardware. Products must be easy-to-use, easy-to-learn, easy-to-operate, and easy-to-service, so that customers can feel in control of their EDP expenses.

c. Experienced DEC-20 programmers are, and will always be, in short supply. Again, easy-to-use, easy-to-learn systems are a competitive must. Good documentation and self-paced manuals are a requirement so that inexperienced users can learn the system fast. Also, maintenance of software is more expensive than its development. Therefore, software products should be easy-to-update and easy-to-understand.

d. Peripherals have grown to be the most expensive part of the system equaling 50% to 70% of the hardware cost, depending upon configuration.

e. Decreasing cost of hardware will put computers and terminals directly in contact with more and more office workers. Thus, transparency of hardware and operating systems is important. users will want their terminals to have the ability to access data located on various systems.

f. With the advent computers, the amount of information capable of being stored has grown, but the complexity of information retrieval has increased exponentially. However, timely information is, and always has been, crucial to business success. Computer systems should be able to speed up feedback, not slow it down.

g. In order to control computer costs and take advantage of tax and investment credits and to increase data privacy, large commercial and government institutions are purchasing their own computers for in-house timesharing.

h. Customers want to utilize the benefits of intelligent terminals.

2. Competition - Present Trends

a. Total System Price/Performance Ratio:

The DECsystem-10/20's have been successful because they have had a unique market niche. Over the last ten years, the systems have been bigger than the Mini's and smaller than the traditional mainframes. The system prices bracket the space between $.5 million to $1 million where few mini and mainframe competitors have been. Not only that, but the systems offer the functionality of a mainframe but retain the interactiveness of a personal computer.

This successful market niche is attracting competitors. Mainframe suppliers are offering the same functionality on lower priced hardware (the IBM 4300 Series). Minicomputer vendors are offering large mini's with greater functionality (HP3000, VAX-11). Today's products can be successful by promoting current functionality and the 15 years experience in the marketplace. But new competitive hardware both at the high end and low end of the family is necessary if we are to hold our customers until VAX and 11's can attract customer base. Otherwise, profits will erode.

b. Competitive Peripherals

The DEC-20 does not have competitive peripherals. Since peripherals now account for 50-70% of system cost, considerable revenue is being passed on to the competition. Maintenance costs are also out-of-line.

3. Technology - Present Trends:

   Technology is reducing the cost of processing power by 30% per year. As this happens, processing power can be brought closer and closer to the user. Simple tasks will be given cheap processing on a chip (intelligent terminals). Medium level processing will be done by minicomputers (intelligent controllers for communications and for data base management --tapes and disks). Large scale processing will still be handled by very large processors. Networking the various processors together is a requirement.

D. PRODUCT DEVELOPMENT STRATEGY

Short-term Strategy

1. Implement KL RAMP features as soon as possible to maintain product profitability over remaining life cycle.

2. Develop TOPS-20 into a mature operating system capable of sustaining large system revenue until VAX family fits customer needs: Performance, operating environment, and DECNET improvements.

Long-term Strategy

1. Develop price/performance processors at high and low end of family -- 2080 and price-reduced 2020 -- to immediately address competitive situation.

2. Continue to implement RAMP features with particular emphasis on network-oriented RAMP (system sleep, etc.) to decrease total system cost.

3. Develop network capabilities to support high-speed local links and slow long-distance capabilities. Implement network virtual terminals, routing, terminal concentration and network virtual disks (transparent network). This will allow customers to take advantage of the low-cost mini and micro processors.

3.0 36-BIT LANGUAGES STRATEGY

36-BIT LANGUAGES STRATEGY

A. PRODUCTS/CHARTER

All language products developed by DEC for 36-bit computer systems come under the charter of this section, including data base languages and applications. Most of these products are funded by Central Engineering. Some of these products are funded and/or managed by Product Lines. Also included are a few products developed (for DEC) by outside vendor/contractors.

Our objective is to provide application development facilities for a wide range of applications. Some factors:

Applications' areas are defined by the Product Lines' target markets.

Upgrades are required to maintain competitiveness as well as conform to standards.

Good documentation is part of a good language product.

Ease-of-use is a principal factor.

Maintenance releases support the customer.

Products List		Projects Not Funded
ALGOL	DBMS	BLISS-36
APL	IQL	DMPLUS
BASIC	MCS-10	ITMS
BLISS-10	RMS-20	RPG II
COBOL	SORT/MERGE	TCS-20
FORTRAN	TRAFFIC-20	

B. STATUS

1. Present Markets -

At the present time 36-bit systems are used in Education, Federal Systems, Engineering, Data Services and Commercial installations. The proportion of installed systems by dollar-volume and product line is as follows:

Education	$153M	30%
Commercial End User	100M	20%
Data Services	93M	18%
Federal Systems	81M	16%
Engineering	69M	14%

These numbers are for the installed base as of Dec. 31, 1978, and are calculated on average system selling price as follows:

1040	-	$550 K
1060	-	650 K
1080	-	750 K
1090	-	750 K
2040	-	400 K
2050	-	525 K

Due to changes in product line responsibility for accounts over the years we can't tell from this what the proportion of different types of applications is in the field. An informal survey taken at DECUS in late 1978 indicates usage of various languages. We had 64 responses from TOPS-10 users and 28 responses from TOPS-20 users. (The number of systems in the field at that time was approximately 450/T-10's, and 250/T-20's.) The proportion of sites using each product follows.

LANGUAGE	10's	LANGUAGE	20's
FORTRAN	95%	FORTRAN	78%
COBOL	78%	COBOL	60%
BASIC	72%		
BLISS-10	41%	BASIC	53%
ALGOL	39%	BASIC+2	28%
APL	30%	BLISS-10	28%
		APL	21%
		AGOL	7%
DBMS	17%	TRAFFIC-20	32%
IQL	8%	IQL	17%
		DBMS	13%
		CPL	3%
MACRO	89%	MACRO	82%

This distribution does not necessarily duplicate precise distribution in the field, but is indicative of the general trend.

2. Product/Market coverage-
3. Active Projects
4. Projects Funded/Inactive
5. Present Funding

} See Charts starting next page

PRODUCTS	FCS		INVESTMENT BY 'FY'					STATUS/ FUNDING
	50%	90%	80	81	82	83	84	
UNFUNDED 36-BIT LANGUAGE PROJECTS								
BLISS - 36			60					MUST FUND 1ST YR MAINT
BASIC + 2/20 V3	12/79		38					
TCS - 20 V1	3/80	5/80	190					
TCS - 20 V2			63	252				
PRODUCTS IN MAINTENANCE - NO FUNDING NEEDED								
ALGOL	MAINTENANCE →							
MCS - 10	MAINTENANCE →							
TRAFFIC - 20	MAINTENANCE →							
CPL	MAINTENANCE →							

PRODUCTS	FCS		INVESTMENT BY 'FY'					STATUS/ FUNDING
	50%	90%	80	81	82	83	84	
FUNDED 32-BIT LANGUAGE PROJECTS								
ADA			49					R & D
APL			167	167	84			IN DEVELOP-MENT
PROGRAMMER WORK STATION			163					
DATA INTERCHANGE UTILITY			76					
RMS - 20	--	--	111					
FUNDED 36-BIT LANGUAGE PROJECTS								
COBOL	12/80	6/81	264	132	MAINTENANCE	---->		IN DEVELOP-MENT
FORTRAN V6	3/80		114					
V7	6/81		78	146	MAINTENANCE	---->		IN DEVEL-OPMENT
DBMS V6	4/80	7/80	208					IN DEVEL-OPMENT
DBMS V7			86	294	MAINTENANCE	---->		IN DEVEL-OPMENT
MACRO/LINK	3/81	6/81	62	12				
PL-FUNDED 36-BIT PROJECTS								
EXTENDED EXPONENT/ESG			85					

PRODUCTS	FCS		INVESTMENT BY 'FY'					STATUS/ FUNDING
			80	81	82	83	84	
UNFUNDED PRODUCTS 3RD PARTY PROJECTS								
ITMS DOCUMENTATION			30					
RPG II DOCUMENTATION			30					
DM-PLUS DOCUMENTATION			30					
3RD PARTY PRODUCTS NO FUNDING NEEDED								
IQL								
CONTRACT PROJECTS								
APL TEST SYSTEM			75					TO BE STARTED/FY'80
EXTENDED EXPONENT ESG FUNDING			85	12				IMSL

C. ENVIRONMENT

1. Marketplace-

General decrease in the price and size of hardware brings software to the forefront in importance. The labor-intensive nature of software development causes software costs to grow with respect to hardware costs. Creative user-oriented software that lowers the users' S/W development costs is appreciated more by the knowledgeable buyer. Competitive battles will be shifting increasingly from hardware to software areas.

Users in the administrative/commercial areas have generally needed more ease-of-use in systems, languages, applications, documentation and training. With the availability of more and better software in the field and vigorous efforts from independent software houses, users have become aware that the use of computers can be made easier, and many customers now specifically look for and demand ease-of-use. In addition, the wider use of

computers is causing a shortage of computer personnel, and widespread acceptance of the computer as a personal tool is beringing more non-computer specialists in direct contact with the computer. The result is a general demand for ease-of-use and reliability, which is present in the technical computing areas as well as in the commercial sector.

Growth requirements and the state of technology are bringing acceptance of distributed systems. Bringing the needed accessibility and reliability to distributed systems is the software designer's major challenge for the early eighties.

2. Competition -

The major competitive issue for the 36-bit marketplace is the announcement of the IBM 4331 and 4341 systems, along with significant changes in IBM's delivery of services to customers. IBM is clearly preparing to shift the emphasis to software as the steady producer of income, and to cut support expenses and staff thru the Phone Centre.

Prime, and to a smaller extent Harris Corp., seem to be about to invade our territory and need close watching in the language realm. We need to take a clue from the use of sales literature by our competition, particularly IBM.

3. Technology-

The growth trend of the late 70's is toward distributed processing. The idea has been talked about for several years. In the early 80's the idea becomes reality, as communication hardware and data lines become more reliable and cost effective, while market understanding and acceptance are rising.

The combination of increasing technical know-how and increasing competition have created an atmosphere where ease-of-use is an expected and appreciated feature of every system. It is especially important in commercial areas, but is required to a much greater extent than in the past for the technical markets, also.

Greater memory sizes become possible and expected due to the rapid decrease in the price of various memory modules. Skillful use of increased memory size can bring about improved performance, given proper software design. The onus here is on system software--handlers, swapping, buffering, etc., and on utilities.

D. STRATEGY

1. Market Strategy -

1.1 Short-term Strategy-

Sell to present markets, new and existing users.

Sell with software: wide choice of languages and applications; mature, high quality languages; good interactive capability; application software availability.

Market ease-of-use, especially on TOPS-20.

Market maturity, highly evolved features especially on TOPS-10.

Especially when selling against IBM, emphasize software price/performance.

1.2 Long-term Strategy

Sell 36-bit systems to the existing user base.

Encourage system expansion with 32-bit processors where appropriate. Promote good interactive capabilities; ease-of-use; mature, reliable, high-quality software; availability of application packages; capacity for growth.

Heterogeneous communication software will be the main vehicle for such growth.

Syntactic compatibility between 32-bit and 36-bit based languages and other compatible software will make growth via heterogeneous systems relatively easy. Conversion aids will be available.

1.3 Assumptions

The sales force will be trained and will understand buy into Corporate product development and market strategy.

The sales force will gain good understanding of the role of software in systems' sales.

1.4 Risks

The sales force may not understand the marketing and product development strategy and the role of software.

2. Product Development Strategy

2.1 Short-term Strategy

Meet customer commitments such as Extended Exponent in FORTRAN, validation for FORTRAN and COBOL, performance improvements in COBOL, BASIC and FORTRAN, etc.

Continue meeting the needs of the 36-bit markets with general technical and administrative software.

Plan appropriate communication software language interfaces.

Stabilize development on languages with the next release where possible. Syntactic compatibility with VMS langauges is a primary goal of stabilization.

Stabilization is to be carried out in such a way as to minimize disruption and inconvenience to customers. Changes in features that would necessitate rewriting of existing programs will be installed with a software switch wherever possible, so that users will not be forced to reprogram, but may choose to use the new features, or not use them as they wish.

Actively participate in, reinforce and help with any programs initiated by Product Lines to raise the level of software knowledge in the salesforce, especially in understanding the strategy and the role of software in the market. Provide assistance to Product Lines in preparing instructional materials and sales aids for the salesforce.

2.2 Long-term Strategy

Prepare to meet Large Systems marketplace requirements with 32-bit systems by 1985.

Prepare for syntactic compatibility and data conversion requirements of 36-bit based languages.

Develop appropriate communications software language interfaces for closely-coupled homogeneous and loosely coupled heterogeneous distributed systems by 1983.

3. Assumptions

It is assumed that VMS software will reach TOPS-10 functionality in all major aspects before 1983.

It is assumed that market acceptance of distributed systems will continue to increase.

4. Risks

There is a major risk, that rapid development by competing vendors might cause TOPS-10/20 language offerings to become obsolete faster than presently expected.

E. PROJECTS FUNDED BY CENTRAL ENGINEERING

Functions Supplied

Strategic Reason for Implementing and

Relationship to Goals

APL V2

Goals - Quality product, maintain customer base. Prepare for 'ongoing maintenance status'.

Strategy - Provide a competitive 36-bit product with improved price/performance. Stabilize product.

Functionality - Functional enhancements of features as requested by customers. Native-mode operation on 20's for improved speed performance.

FORTRAN V6

Goals - Quality product; maintain customer base. Get ready to stabilize.

Strategy - Provide improved speed, performance and reliability. Reduce technical risk for next ANSII standard release.

Functionality - Native mode on 20's. Reliability and maintainability enhancements. Foundation work for ANS'78 FORTRAN Standard.

FORTRAN V7

Goals - Maintain 36-bit base and provide an alternate growth path with a quality product. Prepare for ongoing maintenance status.

Strategy - Transportability with VMS FORTRAN through FORTRAN-78. Stabilize 36-bit software. Provide a competitive product.

Functionality - ANS'78 standard features implemented. S/W option switch for features that could necessitate reprogramming otherwise.

DBMS V6

Goals - Maintain installed 36-bit base. Improve RAMP.

Strategy - Provide a competitive product with improved quality, ease-of-use and price/performance.

Functionality - Finish implementation including load test performane analysis and field tests, also documentation and SQM.

DBMS V7

Goals - Maintain 36-bit base with a quality product. Fulfill commitments. Prepare for 'ongoing maintenance' status.

Strategy - Provide improved functionality and price performance i.e., stabilize DBMS, prepare to shift engineering focus.

Functionality - Improved functionality with data dictionary, extensibility features for dynamic change. Continued performance tests and enhancements. (partial compliance with latest ANSII specifications) Stabilize on TOPS-10 and TOPS-20.

COBOL 68/74 WITH SORT

Goals - Quality products, fulfill commitments. Prepare for 'long term maintenance' status.

Strategy - Stabilize at 68/74 level. Maintain customer base with improved price/performance.

Functionality - Improve I/O performance. Stabilize product. Fix minor deficiencies for Federal Qualification Tests.

F. PROJECTS FUNDED BY PRODUCT LINES

EXTENDED EXPONENT

Goals - Fulfill commitment to Phillips; also appreciated by other customers, good stabilization feature.

Strategy - Quality performance feature.

Functionality - ANS'78 standard features implemented. S/W option switch for features that could necessitate reprogramming otherwise.

G. PROJECTS NOT FUNDED

BASIC+2 V3

Goal - Fulfill commitments shift engineering effort to other projects.

Strategy - Stabilize at present level with REL files - a major expandability feature.

Functionality - Complete RELfiles feature, stabilize product.

TCS

Goal - May become necessary for maintaining 36-bit base in general systems, in present markets.

Strategy - Meet customer commitments, provide a competitive product.

Functionality - General transaction processing system including screen formatting and queueing, planned for high throughput transaction oriented applications, to be supported on VT-62's.

Not funded yet, due to lack of adequate market focus/interest from the Commercial product lines.

BLISS-36

Goals - To maintain 36-bit base for DEC.

Strategy - Allow users to write system programs in BLISS-36, which can be easily converted to BLISS-32, for future growth with 32-bit systems.

Functionality - System implementation language.

Not funded. The $60K requested is for first year maintenance. The product is implemented and fully documented.

Not funded by product lines- probably due to relatively low priority.

sa

6.0 PERIPHERALS

D R A F T

LSG PERIPHERAL SUBSYSTEMS STRATEGY

STRATEGY:

* Improve high-end mass storage technological position; provide IBM comparable offerings within 1 year of IBM availability.

* Evolve to highly functional I/O complex that assumes data management and device dependent functions.

* Leverage software investment and protect against competitive encroachments by unbundling system device software and device diagnostic software.

* Aggressive hardware pricing.

* Reduce people costs and improve productivity with automated mechanisms for backup, archiving, and data interchange.

* Improve availability--all devices dual/multi-ported.

* Stabilize older products faster--focus on a much narrower range of hardware for testing new S/W products.

ASSUMPTIONS:

* LCG developes products or pursues own co-development with peripheral vendors in order to satisfy high end requirements where products developed by Central Engineering do not meet large computer systems needs.

* Cost of hardware not expected to be competitive advantage now or in future.

* Software costs go up.

* Hardware costs go down

* People costs become major portion of downtime cost.

* Markets seek automated computer operations

* End user and capacity trends same

* Intelligent controllers viable

JMV
5-23-79

LARGE SYSTEMS DISK STRATEGY

PLANNING PERIOD

This strategy covers the next generation of offerings through FY'81. The direction for the generation beyond is covered in Figure #1, attached.

CAPACITY

STC 8650	1200 MB	Large databases; High End and Midrange
RP07+	600 MB	Mid range

TIME TO MARKET

High end gap reduced to one year
Mid range lags 2½ years
Low end gap at 1½ years

COST

High end parity within 10% of IBM
Mid range cost competitive
Low end competitive

COVERAGE

Complete:

Low end gap
RP06 must suffice as mid range
Proposed 15% to 20% price reduction
No high end product until 8650

ANNOUNCEMENT SCHEDULE

STC 8650	6-8 mos (Q2 - FY'80)
RP07+	18-24 mos (Q2 - FY'81)

DEVELOPMENT

No new hardware for 8650
RP07+ per plan

FCS SCHEDULE

STC 8650	Q4 - FY'80
RP07+	Q2 - FY'81

SYSTEMS		1090	1091	2040	2060	2020
8650	1200 MB*	X	X	X	X	
RP07+	600 MB	X	X	X	X	

Note:

* VAX will support RP07+. 8650 could be supported with no new hardware development; however, there are no current plans.

TACTICS

- Support corporate RP07+ and integrate into TOPS
  In FY'80 Budget ($84K)

- Integrate and introduce STC 8650
  In FY'80 Budget
  FY'80 Engineering cost $169K
  FCS - Q3/Q4 - FY'80

- Corporate convergence - support and evolve to HSC 50/ICCS in FY'82 per plan (See Figure #1)

    - VENUS

    - 2080

  Eliminates IBM controller high cost and establishes an intelligent controller for distributed systems data bases

7.0 VENUS-32 STRATEGY

D R A F T

VENUS 32 RED BOOK STRATEGY

SUMMARY

The corporate strategy is to converge on a 32-bit architecture by FY85 with the center of business in systems having MLP less than $250,000. Focus will be given to development of systems for distributed processing and for high availability.

Between now and the mid-1980's the marketplace will demand computer system products that are cost- and performance-effective, easy to use, secure, highly reliable, and family oriented. The products must support distributed processing with interconnections to systems of many vendors and to packet switched networks. They must be laden with rich software (languages, data management, utilities, applications).

Key focus has to be on life cycle cost of ownership for the total system including hardware and software.

VENUS is a product at the high end of the VAX family pyramid during the FY82-85 timeframe. It will meet the market's requirements with product development priorities as follows:

#1 - design center at $180K MLP with performance at 3.5 times VAX-11/780
#2 - new I/O architecture based on ICCS, HSC50, and MERCURY
#3 - SBI capability for -11/780 migration
#4 - FCS in Q2 FY82; volume in Q4 FY82
#5 - entry level system at $99K MLP
#6 - significant RAMP improvements
#7 - system options
#8 - large system

The VENUS system product is an excellent offering to the traditional Digital markets ---scientific, real-time, timesharing. For transaction processing and for general purpose commercial EDP, VENUS will also be a strong product with the continued development of software products appropriate to those market segments.

The VENUS system product will be compatible with the VAX family architecture. It will use the single VAX family operating system, VAX/VMS. VAX-11/780 migration is supported, and PDP-11 compatibility mode is maintained.

The technology for the VENUS design is ECL Macro Cell Gate Array.

Transfer cost goal for an entry level system is $25K.

9.0 SOFTWARE SERVICES STRATEGY

D R A F T

SOFTWARE SERVICES STRATEGY

MT 1/9

A. PRODUCTS/CHARTERS

Software Services (SWS) is a DEC internal service organization which also offers customers an array of services. It provides expert advice to Digital's field software support personnel and reviews technical literature and courses meant for them and for the customers. Software Services helps software development in conducting field tests and issuing maintenance releases. The expertise in the support organization is also available to the product lines for pre-sales activities and special projects. Resident consultants are available to help customers with new system set-up, conversion or other special projects. Service planninng and new service development are functions of SWS.

The Charter of Software Services (SWS) is to aid four groups:

1. Customers of the Large Systems Group
2. Software Development Engineering
3. Field Software Service organization including residents and consultants
4. Product Lines

Present Products

- Support Planning for DEC's field organization
- Software Consulting for customers
- Warranty Support (Hot Line) of Field Specialists
- Post Warranty Support (Annual Service) for customers
  - Software Patches via the DISPATCH
  - Software Updates
  - Software Documentation
  - Software Notebooks
- Software Training for SWS and customers
- On-site support for critical situations

B. STATUS

1. Present Markets

The most active LSG markets for SWS are post warranty support for KL-based systems and warranty support for KS-based systems. The DECSYSTEM-20 area generates the majority of consulting contracts.

The markets for SWS are naturally the same ones for the software products themselves. For example, DBMS support is in high demand by markets which rely on DBMS such as mass retailers and universities. Increased system sales into the Commercial Market and the Commercial customers' characteristics has increased the urgency of offering greater range, quantity, quality and speed of services.

Traditionally, DEC customers and field personnel were invited to participate in the support of DEC software. However, these groups in the Commercial markets are no longer willing nor able to perform this role. There is a widening gap between the perceived needs and SWS' offerings today.

Customers in the Engineering and Federal markets tend to be more sophisticated and knowledgeable of DEC products so their demand for service is comparatively stable.

2. Product/Market Coverage

Although Software Services' offerings to all markets are the same, the actual level of services vary according to the following parameters:

- Geography - DEC customers and personnel in the North American continent have the best access to the services. Markets in other locations suffer from logistics and communications problems.

- Software product status - The condition of the code itself, namely the number of patches required in order to conform to the SPD, greatly influences the allocation of SWS resources.

- Demand - Those customers who are not subject to geographic restrictions who also are demanding tend to receive more attention than other, less active customers.

- Hardware Availability - The dearth of KA and KI-based resources within DEC necessitates the cessation of support for these systems by 1981.

- Product Proliferation - The great number and diversity of software products offered by DEC poses support problems. Some products fulfill the esoteric needs of a small market. Other products are generated by third parties but marketed by DEC. Though the same support as for standard DEC Software is offered for such products, the actual resources required to support third party software may not be justifiable nor available.

New services and enhancements to present services are proposed. These are:

(1) Service Enhancement Project - This contains several components which includes both hardware and software. It is proposed to Walter Manter. Parts a and b are approved and will be implemented in FY'80. Some highlights of this project are:

a. Software Product Services (formerly DSMS) - This is a major offering by Product Line 009 under the direction of Mike Sanderson. It will ultimately cover all DEC software over the next few years, with TOPS-20 being the first LSG product. This is presented to the Policy Pricing Committee (PPC) on June 18, 1979.

b. Software RAMP features - RAMP is the acronym for Reliability, Availability, Maintainability, Performance. Each engineering project has included project-specific tasks to improve these four product characteristics. TOPS-10 V. 7.00 and TOPS-20 Release 4 will both be released with a large number of RAMP features.

c. Microfiche DISPATCH - This is a proposal to repackage the information in the software DISPATCHs. All the information will appear on microfiche, one product on one fiche. That is, COBOL will have its own fiche as will TOPS-20. Each product's fiche will accummulate all fixes since the last general release and will be a super set of its predecessor.

d. Support Criteria - SWS negotiates with Software Engineering during the software development period to produce a list of quantitative criteria. These must be met in order for the final product to receive support. How these are to be achieved is also negotiated and SWS sometimes shares the tasks.

(2) Decentralized Telephone Support - Telephone back-up of field specialists will be decentralized away from Marlboro. Each region has implemented such a service at the regional office.

(3) Customer Support by Phone - For NORAM and Canada, phone support of customers who are under warranty or annual support will be available from the Regional Diagnostic Center (RDC) in Colorado Springs. This Telephone Support Center (TSC) is presently planned for announcement in September and implementation in October. LSG operating systems will be covered by this service at a future date.

(4) 90-Day Software Warranty - This proposal has been approved for announcement in September and implementation in October. It institutes a true 90-day warranty in that after this period, there are no services other than the annual maintenance offered by PL 91 and consulting services offered by PL 90.

(5) Support-Sensitive pricing of Software - This proposal is in embryonic state. The target is to have three separate prices for any single software product:

a. Full price which includes software kits and support.
b. Lower price which includes the software kit but no support.
c. Lowest price which is the software alone with no kit and no support.

(6) Free-standing updates - This is also embryonic and is analogous to the Binary Update Program (BPUS) in the mini business. Software updates will be offered for a discrete price independent of a service package.

It is an imperative from customer input, competitive analysis and our own experience that we offer varied levels of support. As a consequence of entering the applications market, we must provide more specialized support. On the other hand, the industry trend toward more "common" uses of computing power by less sophisticated users through computer networks compel us to make available system-wide support packages as well as individual service modules. In the next 5 years, we should develop coherent support paradigms for complex networks of computers. A recent industry survey of support services (conducted by DEC) shows us ranking rather low in this area. We must expend a focused effort in the support services to protect our present markets and ensure the success of our future market strategies. The proposals (above) are positive steps toward meeting market needs in the next 2 years.

The essential element in any successful support services is quality software. Therefore, a strong and enduring commitment to improve the quality of the software must go in tandem with any service endeavors.

3. Active Projects - Below are FY79 projects which are on-going or recently completed.

   - TOPS-10 V. 7.00 Field Test - 3 persons, full time, plus management overhead. SWS team remains at field test for a week to support installation, ANF-10 and RAMP features, train customer DP staff.

   - TOPS-20 Rel. 4 Field Test - Support of DECnet, RSX-20F and bisynch.

   - DBMS V.5A - SWS dedicated resources (instead of Software Development) to produce maintenance release.

   - DECnet Compatible Port - Certification of DECnet protocol to RSX-11M.

   - MACRO/LINK V.4A - SWS generated maintenance release instead of SWE.

   - MPB Field Test - Conducted by SWS in conjunction with MACRO/LINK release. Last release of MPB.

   - CLAS V.3 - Inclusion of LSG data into SWS data base.

   - Autopatch V.1 - Defining usage procedures for development project. Develop methods of packaging and testing of distribution tape.

   - Regional Support Centers - establishment of field backup expertise in every North American region.

4. Projects Funded/Inactive

5. Present Funding

C. ENVIRONMENT

1. Marketplace

Software's technological advances and prices are exceeding those of hardware in the DP market in general, and in DEC LSG's existing markets. As a direct consequence, software support is becoming an important and lucrative business. The increasing complexity of the software and its applications, balanced by LSG's expansion into markets with less sophisticated customers, necessitates both more expert support and more basic services. The trend is to offer an array of support services which has the flexibility to be "customized" to individual needs.

The service market is expanding and there are myriad opportunities which are worthy of investigation.

2. Competition

Though Digital's LSG Support Services does not overtly compete head-on with IBM, given that IBM dominates 70% of the market, we are de facto in direct competition merely by being in the same markets. Of course, we have other less formidable competitors in the service area, namely, Honeywell, Hwelett-Packard, Control Data, etc.

An extensive survey of support services was conducted by the Software Services Group in Marlboro from 1977 through 1978. Of the 7 vendors analyzed, of which DEC LSG is one, we ranked towards the bottom in offering and delivering innovative, quality services. UNIVAC ranked beneath us with the comment that their service products were "8 to 10 years behind the industry norm". This survey is recommended for more details about our competition.

3. Technology

The following are support needs which can be met with near term advances in software technology.

- Customer support by telephone, aided by on-line data bases of reported problems and respective resolutions.
- Software which is compatible with heterogeneous networks of hardware configurations thereby reducing support complexity and costs.
- Automated collection and dissemination of machine-readable problem reports and respective resolutions, expecially across oceans.

- Improved system security mechanisms which simultaneously facilitate remote problem-diagnosis and cure.

- Improved software self-diagnosis and fault tolerance.

- Develop automated, machine readable patching tools.

D. STRATEGY

1. Market Strategy

1.1 Short Term Strategy

- Meet customers' demands for:

  - Access to our support expertise
  - Rapid response to critical problems

- Hierarchial rather than concentric support.

- Align the policies within and among DEC groups.

- Help improve the software products themselves.

- Variable pricing of software according to service level.

1.2 Long Term Strategy

- Incorporate all DEC software into standard service packages and modules.

- Create new services to support the corporate strategy.

- Realize significant revenue from software and associated services.

2. Product Development Strategy

2.1 Short Term Strategy

- Respond to demands using presently available resources as much as possible. Conservative new spending.

- Catch up to industry trends and major competitors.

- Adjustment of service processes rather than generating wholly new service products.

2.2 Long Term Strategy

- Synchronous development of software and associated services, e.g., heterogeneous networks and their support.

- Deliver service products which are highly competitive but not leading the industry.

3. Assumptions

- DEC will continue to increase the quality (not functions) of 36-bit Software.

- DEC will continue to fund service developments for 36-bit software.

- DEC will incorporate 36-bit software into new service offerings.

- No dramatic changes in LSG market profile.

- No dramatic changes in competitors' offerings.

4. Risks

- De-emphasis of 36-bit systems.

- Ignorance of VMS development and markets.

These two factors complement each other in aggravating the risks of:

a. Discontinuous/incompatible levels of support.

b. Technology-constrained support offerings.

E. PROJECTS FUNDED

GB0005/48

d i g i t a l interoffice memorandum

Subject: 1990's Space Strategy and Plan: Let's Write it Down!

To: 1990's Committee

CC: Ken Olsen, ML10-2/A50
George Chamberlain, MS/B80
OOD

Date: 11/5/79 Mon
From: Gordon Bell
Dept: OOD
Loc: ML12-1/A51 Ext: 225-2236

BACKGROUND AND MOTIVATION

After the last OC, it became clear that we need a better way to work on space. Having reviewed the file on our 1990 strategy, I think I see the problem... namely, it isn't written down in any coherent way, and merely consists of some implicit notions that we are going to have centers spring up in different places depending on needs, deals, etc. Also it barely covers 1983! We argue violently about particular sites, buildings, etc. in a completely unstructured fashion, because there is not agreement on the conceptual framework or strategy. Also, it is inherently difficult because we aren't really sure what the organization will look like in 1990.

We can always change it, but first: WRITE IT DOWN!

AN OUTLINE FOR THE STRATEGY AND PLAN

0. Organizational design assumptions (if they appear to be important)

1. Location of population assumptions as they relate to travel, energy, cost of living and labour. Especially necessary for manufacturing part

2. Needs vs time (The emphasis will be on writing and validating a model for all the groups and company as a whole)

3. Our goals and constraints in regard to:
   .Site types (their names, site types and sizes)
   .Site tennants (policies as to who cohabits)
   .Building standards

4. Plans for alternative ways to satisfy the needs versus time

5. An index of definitions

CHARACTERIZING THE GOALS AND CONSTRAINTS

We must decide on these in order to stop the hassle on individual plans. Here, a constraint is something that we intend to never violate, for example, no buildings greater than 600 Ksf, or start a new cluster outside of Mass, NH. Equally important are targets or goals which we expect to attain, these include statements like minimize future growth in Mass. by no new sites beyond x, y, ... z (actually list them to avoid ambiguity). In order to fully understand this, let me urge you to look at the document I used to control the design of VAX; the summary with my comments is attached.

Although I don't know what they are, I would like to get the Space group to pull these together and I would review them for consistency and applicability before the 1990 group goes over them. Let me suggest the following:

Constraints

All campuses (clusters) should be at least two functions and preferrably more.

Market oriented Product Lines should co-exist with their own market specific engineering, sales support, and service support.

Hardware and Software Engineering, Service Support, Market Support should cohabit for base products.

No single office buildings greater than 600 Ksf should be built.

Sales and Service (Hardware and Software) cohabit at every level and site.

All sites which are DEC built are selected on basis for at least a factor of 2 growth, and preferrably a factor of 4. Here, I assume a 12% growth in group size will handle a capacity growth of 26%. Note 12% doubles every 6 years. If we start a site at say 2/3 capacity and grow it a factor of 3 in size (or 4.5 in population) would give about 14 years of growth on a site!

Goals

Mfg and Eng should cohabit for process intensive designs. Examples:

- .LSI chip design (eg. Comet chips, Fonz)
- .print part of technology
- .tape and disks
- .tape and disk heads and media

Integrate high volume and FAT plants such that the tradeoff between standard and special product is possible and measureable.

Move to more clusters (giving more freedom of functional choice).

Move to clustering of implicit divisions when all possible.

CHARACTERIZING THE SITES AND TENNANTS

It is important to separately characterize the types of spaces (sites) and the tennants (occupants). Let me propose these site names, by size:

1. Clusters (campuses) 1-3 Msf
2. Satellites (buildings or sites that operate to another satellite or cluster) 100-500 Ksf
3. Field sites ? Ksf

The tennant typings are:

1. Heterosite with multiple functions
2. Heterosite operating implicitly or explicitly as a division
3. Homogesite holds a single function
4. Homogesite of Manufacturing and Engineering for process intensive products
5. Homogesite for Sales and Service

SPECIFIC PLANS, HOW THEY MIGHT GROW AND HOW THEY RELATE TO GOALS

Location	Host/Tennants	size (now) [Msf]	(max) [Msf]
HETEROSITE CAMPUSES			
Maynard	HQ (OOP, OOD, OOM, Sales, F/A), Misc. P/L	1.8	1.8
Merrimac	Comml and Computer Product P/L	.6	1.8
Marlboro	Tech P/L, LSGE, Term and micro P/L	.7 (1.3)	72.0
Andover	SVC and Mfg. (violates sales/svc coupling goal)	?	1.8
HOMOGESITE CAMPUSES (Violates Constraint for a Campus)			
Salem	FAT (violates volume/FAT coupling goal)	.6	1.2
Phoenix	Terminals volume (violates Mfg./ Eng. coupl. goal)	?	?
HETEROSITE SATELLITE			
Hudson	Mfg. / Eng of Semis	.3	.6?
Colorado	Mfg. / Eng. of disks	.3	1.3?
HOMOGESITE SATELLITES			
Twksbry	Hardware Base/FS support (violates HW/SW couple)	.2	.2?
Spitbrk	Base SW (needs SWS and HW coupling)	.2	.6?
Acton	Mfg. engineering		
Westboro	Mfg. engineering satelite to Acton		
Nortboro	Warehouse		
Westfld	Mfg.		
Westmntr	Mfg FAT (violates volume/FAT coupling goal)		
FIELD HETEROSITES			
Acton	GIA	.07 (.1)	.3

GB:swh
Attachment

GB1.S1/6

digital interoffice memorandum

SUBJ: OFFICE OF CENTRAL ENGINEERING (OCE) DESIGN GOALS AND CONSTRAINTS

To: Gwen Bell, ML12-1/A51
Paul Benigni, ML11-4/E53
Mary Jane Forbes, ML12-1/A51
Sam Fuller, ML3-5/H33
Mitch Kur, ML12-2/A16
Si Lyle, ML12-1/T39
Charlie Picarello, ML12-1
Larry Portner, ML12-1/T32
Dick Schneider, ML11-4/E53

Date: 1/5/79 Fri 3:00:43
From: Gordon Bell
Dept: OOD
MS: ML12-1/A51 Ext: 223-2236
EMS: @CORE

Definitions:

G - Goal: a value that a design will attempt to achieve or exceed.
C - Constraint: a limit that a design can't exceed.
I - Implication: given a goal or constraint, one of the consequences.
D - Decision: a value of a design parameter that has been selected.
R - Remark: comment on a statement.
A - Alternative: some possible choices.
F - Fact: almost synonomous with an external constraint, eg., the OCE is in the mill.
CF - Conflict: can exist between goal/constraint/ implication/fact and demands resolution.

G - A well-designed open office that can and will be used as an example.

G - Measure ROI on all changes and designs.

G - Select from alternative designs before making decisions.

G - Keep within these goal statements and use them as a working document.

G - Keep within design guidelines established on a corporate basis.

G - Develop individual room/area design goals and objectives from these based on all of central engineering.

F - The OCE will be in 12-1.

G.1 Be the central intelligence for central engineering, setting the style and pace for the environment for working as well as the work output.

#1 C.1.1 Link OCE with all engineering groups.

#2 F.1.1 OCE includes the following:
Gordon Bell + 4 support
Larry Portner + 1 support
C. Picarello (war room manager) + 1 support
Si Lyle (product manager) + 5 support
Mitch Kur (engineering controller) + 1 support
Sam Fuller (technical director) + 1 support
Visitor work station
Conference room + waiting area with telephone
War room
Kitchen + food serving area
Bathrooms (also must service 10-2)

#3 CF.1.1 Given the present division of 12.1 the group cannot be contiguous unless the dividing hallway is removed.

I.1.1 Develop a war room for strategies that works as a communications and strategy center.

I.1.2 Provide an image of appropriate use of high technology for major high tech customers.

CF.1.1 "War room" will have to be secure and yet will have examples of new technology that may be interesting to customers.

C.1.2 Interrelate to corporate wide planning for DEC with appropriate links and connections.

G.2 Experiment with latest technologies in computing, communications, energy conservation, and building materials in order to improve productivity.

I.2.1 Record the process in order to learn from this experiment and make further improvements.

#4 I.2.2 Integrate use of ems, word processors, large screen video and latest communication modes into OCE for maximum use.

C.2.1 Use DEC machines to push their limit.

I.2.3 Willing to experiment with one of a kind and prototypes to better fit DEC machines into office environments.

R.2.1 Charter of Industrial Design does not include new machine adaptations and additional charter may need to be applied for.

C.2.2 All staff will be no more than 1 chair turn away from a terminal.

#5 CF.2.1 Use of inter-related machinery in mill will demand connecting with cables "dangling" and raises a special problem issue.

C.2.3 Minimize operational costs by reduced air conditions and use of natural lighting.

D.2.1 Use task vs overhead lighting.

D.2.2 Put switches on all lights.

C.2.4 Design for minimizing maintainence costs without exorbinant startup expenses.

#6 C.2.5 Conserve the basic mill structure, erring on the side of simplicity vs. Victorian refurbishing of any kind.

C.2.6 Look to new technology that minimizes energy and materials, eg., replacing paper with film, film with disks.

C.2.7 Be able to change over time with changing technologies and organizational structures while facilitating ongoing use.

G.3 Satisfy human needs.

I.3.1 Emphasize that humans are the masters of the machines. Integrate the use of machines and high technology with the visual, auditory, and physiological comfort of the individual.

I.3.2 Consider interactions and functions for assigned tasks to minimize wasted time.

I.3.3 Develop an integrated aesthetic style for OCE that fits within any corporate guidelines and also allows differentiation in "room" styles within OCE.

C. 3.1 Fit a variety of behavior patterns and individual needs, but confine individual tastes to discrete areas and use of nomadic items -- nothing attached.

CF.3.1 Consider the need for privacy and the needs for links and communication -- work out these conflicts on a generic and not on individualized bases.

~~Attachment~~

COMPANY CONFIDENTIAL

Preliminary Draft for Commment by Digital Engineering Community

HEURISTICS AND COMMENTS FOR BUILDING GREAT PRODUCTS

Gordon Bell, Vice President, Engineering

Product goodness is somewhat like pornography, it can't fully be described, but we're told people know it when they see it. If we can agree on heuristics about product goodness and how to achieve it - then we're clearly ahead. Five sets of dimensions for building great products need be attended to (roughly in order of importance):

- a responsible, productive and creative engineering group;
- product and design metrics (competitiveness);
- design goals and constraints;
- product evolution, revolution and death; and
- the ability to get the product built and sold.

ENGINEERING GROUP

As a company managed primarily by engineers, groups are encouraged to form and design products. With this right, are responsibilities.

The Team must have:

- a chief designer/chief programmer to formulate and lead the resolution of the problems encountered in the design; No matter how large the project, it must be lead from a "single head". We often make two errors in leadership: having no clear technical leader/problem resolver, and abdicating to a committee.

  Committees do not do design! They are never held responsible, nor are they rewarded or punished. Committees can review.

- management who understand the product space and who has engineered successful products; The two most important jobs are:
  - making sure that everyone knows their job; and
  - setting and reviewing work on a timely basis, ie. MBO.
- team skills and resources to implement the proposal so that we adhere to the cardinal rule of Digital, "He Who Proposes, Does"; A plan must include the chief designer, team, project organization and resources (eg. computers). Supporting skills and disciplines are essential in the respective product areas, eg. ergonometrics, acoustics, radiation, microprogramming, data bases, security, reliability.
- an understanding of the design, design production (eg. CAD) processes, and manufacturing processes; Learning curves apply to all processes! The organization must be staffed with people who understand the product, the design process (CAD and management discipline) and the production introduction process. One or two out of three isn't enough.

Behaviorally, the team must:

- do it right the first time; Being correct has the highest payoff everywhere: timeliness, quality, lack of rework, and mfg. cost.

- execute the project in a timely fashion; Virtually ALL of our projects are late because we start too late, don't get it done on time because some critical invention is required, take too long to get it introduced, etc. For the very long, very late projects, the failure is lack of planning, tools and organization. Finally, people burn out. This suggests we:
  - limit projects to two years by a small team. We often make an aggressive business plan, then hire the team. They then find out they have neither tools nor technology to do the project.
  - not predicate a project on scheduling inventions in the design, process and CAD areas. If we can't see how to do the work in 2 years, then let's not start the project! This means the product must be cut down to fit the tools, people and process. Advanced developement is to insure that we can do development.
- have a written design methodology that includes: all design processes in the form of manuals, design conventions, conflict resolution, criteria for task completion, PERT structure, etc.;
- be open and have external reviews, and clearly written product descriptions for inspection; For new product areas, we require breadboards in addition to the above heuristics. When the product gestation time equals the generation time, a full advanced development effort is the only way to be successful.
- start small, be reviewed and grow on its demonstrated success;
- learn, in order to handle the increase in complexity that comes with technology. Until there's a formal sabbatical program, individuals would do well to consider taking the equivalent of a semester of technical courses each 10 years.
- have an organization & process to check itself — "always get a second opinion".

PRODUCT METRICS KNOWLEDGE includes:

- products for which there'll be no competitor;
- all product cost metrics (cost, cost of ownership, cost to operate and use);
- all product performance and cost/performance metrics; These are the goodness measures of a product and tell how easily it will be to sell, and if we have improved. Cost and performance is measured against a state-of-the-art line represented by the first shipment of a more advanced product. Alternatively, when there's no direct comparison, the time goodness is determined from the day the product could have shipped. For example, because of parts availability, Nebula and CT could have shipped two and three years ago based on component availability.
- reasons why the product will succeed against present and likely future competition; sure success in the market is to introduce a needed function (eg. 32-bit address) by which all other products have to be measured.
- major competitor products by cost, performance and functionality; This should cover the past and future five years.
- leading edge, innovative, small company products;
- productivity, quality and design process metrics for projects.

DESIGN GOALS AND CONSTRAINTS

Design constraints are generally set as various kinds of standards. These are useful because they limit the choice of often trivial design decisions, and let us deal with important free choices, the goals.

Goals are vitally important because they target our uniqueness.

Poor "mind-set" standards can create poor products, even though they may have made sense at one time. The historical English measures is a good case in point. Currently, the 19" rack and the metal boxes Digital makes to fit in them, and then ship on pallets to customers, act as constraints on building cost-effective PDP-11 Systems. This historical "mind set" standard often impedes the ability to produce products that meet the 20% per year cost decline curve.

- Goals and constraints must be written down and updated from the day the project starts. Virtually every product failure and period of product floundering is a result of no clear goals and constraints since everyone has a different idea of the product.
- A product can only have a few goals and constraints. The ranking is usually: it must work and have improved cost of ownership, be the shortest time to market, highest performance and lowest cost.

We must adhere to standards which we either follow or set!

- If a standard exists, follow it or change it for all! We lost the IEEE Floating Point format. It is likely we will eventually have to support it.
- If a standard is forming go all out to set it. When formed, then follow it. We didn't make DDCMP a standard. When HDLC came, we didn't use it. The result: expensive, low performance products.

Standards can be grouped into four distinct sets:

- DEC Engineering Standards; These cover most physical structures and design practice for producibility, and assimilate critical external standards, such as UL, VDE, and FCC.
- professional society, industry and area information processing standards, from EIA, CBEMA, ECMA, ANSI, ISO etc. such as Cobol '74, Codasyl, IEEE 488;
- defacto industry wide information processing and communication standards such as IBM SNA, Visicalc;
- standards implied by the architecture of existing DEC products to insure our customer software investments are preserved include:
    - architecture of computers, terminals, mass store and communications links; Our current ISP's include 8, 11's, 10/20, VAX, 8048, 8080, 8086, 68000; VT52, VT100, keyboards, Regis; MCP; HDLC, CI, NI, SI.
    - physical interconnect busses for computers and for interconnecting them CT, Q, U, NI, CI, etc. These insure that future system products can evolve from component and computer options between generations.
    - operating system interface file commands, command language, human interface, calling sequence, screen/form management, keyboard, etc.

- Products must be designed for easy translation into in any natural language since we are an international company.
- All products must have be customer installable and maintainable.
- Portability is an important goal. Personal computers must be portable! We must achieve this for all systems ASAP!

WHEN TO CREATE, WHEN TO EVOLVE AND WHEN TO STOP PRODUCTS

Engineering is responsible for designing evolutionary products in our markets AND for producing products that are natural to our tradition of supplying the most interactive, cost-effective computing. If a new product such as personal computing emerges and we do not have a product, engineering has failed, independent of being asked for it!

Given all the constraints, can we ever create a new product, or is everything just an evolutionary extension of the past? If revolutionary do we know or care where product ideas come from? The important aspect about product ideas is:

- Ideas must exist to have products! If we don't have ideas to redefine or extend a market, then we should not build a product.

It is hard to determine whether something is an evolution or just an extension. The critically successful products are likely to occur the second time around. Some examples: PDP 6,KA10,KI10,KL10,2080; Tops 10,Tenex,TOPS20; PDP5,8,8S,8I/L,8E/F/M; OS8-RT11; 11/20,40,34,44; RSX-A... M, M+; TSS-8,RSTS; various versions of Fortran, Cobol and Basic follow this; LA30,36,120; VT05,50/52,100, 101 etc.; RK05,RL01/2.

- A product tree MUST be maintained by each engineering group showing roots, gestation time and life.

Goodness and Greatness

All products whether they be revolutionary, creating a new base, or evolutionary, should:

- be elegant and high quality: Russ Doane's working definition is: "every feature contributes two benefits", like a double pun. Quality means no excess. Elegant, high quality designs, do double duty with a minimum use of resources. Quality is also the absence of errors, by being right the first time so that it doesn't have to be inspected or redone.
- offer at least a factor of two in terms of cost-effectiveness over a current product; We have classic failures because a CPU cost has been minimized, only to find the total system cost has barely changed 10% and the total cost to the customer is only 5% lower! If each product is unique then we will have funds to build good products.
- be based on an idea which will offer an attribute or set of attributes that no existing products have; For example, the goals and constraints for VAX included factor of two algorithm encoding and also offering ability to write a single program in multiple languages. VT100 got distinction by offering 132 columns and smooth scrolling.
- build in generality, and extensibility: Historically we have not been sufficiently able to predict how applications will evolve, hence generality and extensibility allow us and our customers to deal with changing needs. Extendable products also permit mid-life kickers to products. We have built several dead end products with the intent of lower product cost, only to find that no one wants the particular collection of options. In reality, even the $200 calculators offer a family of modular printer and mass storage options. For example, our 1-bit PDP-14 had no arithmetic ability, nor could it be a general purpose computer.

As customers used it, ad hoc extensions were needed to count, compare, etc. and it finally evolved into a really poor, general purpose digital computer.

- be a complete system, not piece parts; The total system is what the user sees. A word processing system for example includes: memory, keyboard, tube, modems, cpu, documentation including how to unpack it, the programs, table (if there is one, if not then the method of using at the customer table), and shipping boxes.
- be a great system because the components are great; We should not depend on system markups and software functionality to cover poor components and high overhead.
- if we don't make it, buy it; We must carefully decide what components to make versus buy. It is very hard for an organization to be competitive without competing in the marketplace, hence unless we sell it, we should buy it.

Product Evolution

A product family evolution is described on page 10 of Computer Engineering along the paths of lower cost, and relatively constant performance; constant cost and higher performance; and higher cost and performance. In looking at our successful evolutions:

- lower cost products require additional functionality too; A lower cost product, with constant performance or constant function is risky because a new customer base and new way of marketing may be required. Some other company may, however, be successful with the concept. The PDP-8, based on new technology, was radically more successful than its higher priced predecessor, the PDP-5, because it was 2/3 the price and 6 times more performance. The PDP-8/S was a failure at 2/3 the price and 15 less performance than the PDP-8. There are similar stories about the LA 34, VT50/52 and PDT as replacement products.
- constant cost, higher performance products are likely to be the most useful; Economics of use, the marketing channel and customer base are already established and a more powerful system such as the LA120 will allow higher productivity (see Computer Engineering for the understanding and economics). In the 11's there was a successful evolution: 20, 40, 34 anChied 44. Not the 60. The 11/70 was probably our greatest success; it was billed as a mid-life kicker to the 11/45-55.

Revolutionary New Product Bases

- A new product base, such as a new ISP, physical interconnection, Operating System, approach to building Office Products, must start a family tree from which significant evolution can occur. The investment for a point product is so high that the product is very likely not to payoff. In every case where we have successful evolutionary products, the successors are more successful than the first member of the family. Point products with no follow-on will probably fail all roi tests.

Product Termination

- A product evolution is likely to need termination after successive implementations, because new concepts in use have obsoleted its underlying structure. All structures decay with

evolution, and the trick is to identify the last member of a family, such as the 132 column card, and then not build it. This holds for physical components, processors, terminals, mass storage, operating systems, languages and applications. Some of the signs of product obsolescence:

- It has been extended at least once, and future extensions render it virtually unintelligible.
- Better products using other bases are available.

SELLING AND BUILDING THE PRODUCT

"Buy in" of the product can come at any time. However, if all the other rules are adhered to, there is no guarantee that it will be promoted, or that customers will find out about it and buy it. Some rules about selling it:

- it has to be producible and work, AND be useful to software; This, although seemingly trivial rule, is often overlooked when explaining why a product is good or not. If it is a piece of hardware that requires software to support it, the hardware must be available to the programmers who must support it. Software engineers approach new hardware with much caution! The often ask: is it significant? is it needed? why isn't it compatible with the past? If a hardware is viewed with distrust by software engineers it may be met with the same distrust by customers!
- a business plan with orders and marketing plans from several marketing persons and groups needs to be in place; Just as it is unwise to depend on a single opinion in engineering for design and review, it is even more important that several different groups are intending to sell the product. Individual marketers are just as fallible as unchecked engineers. This rule can and must be violated for revolutionary products!
- never build a product for a single customer, although a particular customer may be used as an archetype user; predicating a product on one sale is the one sure way to fail! Paraphrasing a remark by former GM executive Charles Wilson: if it's good for General Motors, it may only be good for GM.
- it must be done in a timely fashion according to the committed schedule, price and functions as previously described;
- it must be understandable and easy to use. The small size, complete hardware books were the DEC trademark that established the minicomputer. We must revive these such that a particular user never need access more than one. Simplicity must be the rule for our documentation.

What heuristics are missing? What heuristics do you disagree with?

What heuristics could be removed? reordered?

Could I please have your feedback before this becomes a final draft?

3/13/82 Sat 19:47:01 GB3.S2.5

8—
11

Death of the 8

We've been preaching the WPS Strategy for years.

- ~~Fr~~
- Problems inherent in 8 arch.
  - addressing, only 32K (of 48K bytes), by impl. I suspect we'll pay much more than for 64K bytes
  - can't readily make efficient use of lower cost 64K rams
  - Really evolved to be a Kludge!
- Kludge

Write

SINGLE USER SYSTEM CONCEPTS

- STRONG EMPHASIS ON DISPLAY QUALITY, EASE OF DATA ENTRY, PACKAGING, AND USER INTERFACE SOFTWARE TO ENHANCE THE INTERACTIVE ENVIRONMENT

- A SINGLE USER OWNS THE TOTAL RESOURCES OF A SINGLE, FULL FUNCTIONALITY COMPUTER (E.G. VAX)

- RAPID EXCHANGE OF USER FILES VIA PERSONAL MEDIA OR NETWORK ALLOWS THE COMPUTER TO BE SHARED

- A SINGLE USER COMPUTER INCLUDES INTEGRATED CONTROLLERS FOR MASS STORAGE, DISPLAY & DATA ENTRY, AND NETWORK PORT

- A NETWORK LINKS ADDITIONAL SINGLE USER COMPUTERS AND CENTRALIZED DISK SERVERS TO EXPAND SYSTEM CAPACITY

- PRINTER SERVERS, AND OTHER SPECIALIZED/EXPENSIVE FUNCTIONS ARE SHARED VIA THE NETWORK TO EXTEND CAPABILITY

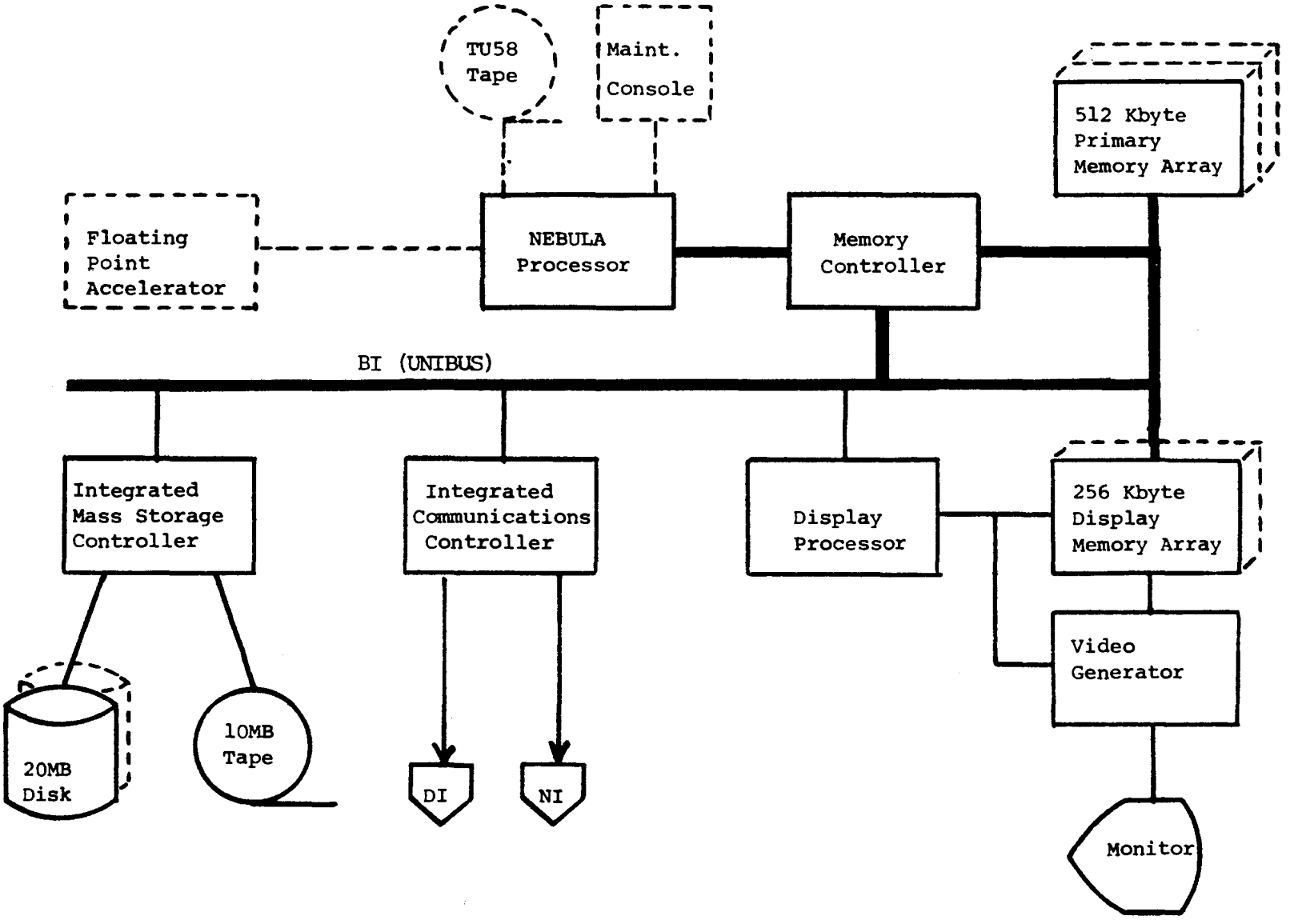
HARDWARE FUNCTIONAL SPECIFICATION SUMMARY

- NEBULA PROCESSOR WITH 0.5 - 1.0 MB MEMORY
- INTEGRATE DISPLAY CONTROLLER, INCLUDING DISPLAY PROCESSOR, BIT MAP, AND MONITOR INTERFACE PLUS
  - 768 X 1024 X 2 B/W MONITOR OR
  - 768 X 512 X 8 COLOR MONITOR
- INTEGRATED MASS STORAGE CONTROLLER
  - 20+ MB FIXED MEDIA 8" WINCHESTER DISK
  - 10+ MB 3M CARTRIDGE TAPE
- INTEGRATED NETWORK PORT
  - 3 - 8 MBAUD NI (ETHERNET)
  - 9.6 KBAUD DI INTERFACE TO KEYBOARD AND GRAPHICS INPUT DEVICE (MOUSE)
- WORKSTATION FORM FACTOR

DISPLAY SUBSYSTEM

- o INTEGRATED 80 COLUMN TEXT AND FULL GRAPHICS CAPABILITY
- o MEDIUM RESOLUTION, HIGH QUALITY RASTER SCAN MONITORS
  - FULL COLOR 768 X 512, 8 BIT-PLANE 19" DISPLAY
  - MONOCHROME GRAY-SCALE 768 X 1024, 4 BIT-RANGE 15" DISPLAY
- o HIGH PERFORMANCE GRAPHICS DISPLAY PROCESSOR
  - EXECUTES EXTENDED "PARALLEL REGIS" GRAPHICS ISP
    - POINT, VECTOR, CURVE, AREA GRAPHICS GENERATION
    - FULLY PARAMETERIZED, SOFT FONT/SYMBOL MANIPULATION
  - COMMAND INTERFACE VIA DMA OVER BI/UNIBUS
  - PERFORMANCE
    - 1 PIXEL/MICROSECOND VECTOR DRAWING RATE (10K/SEC, 100PT)
    - 16 PIXELS/MICROSECOND BLOCK-MOVE RATE (20K CHAR/SEC, 16 X 16)
- o INPUT DEVICE CONTROL
  - TABLET, MOUSE, TRACKBALL, KEYBOARD USER INTERFACE
- o DEVICE SOFTWARE SUPPORT
  - SIGGRAPH/CORE "GRAPHICS LANGUAGE" FUNCTIONALITY
  - DEC/REGIS INTERFACE FROM APPLICATIONS SOFTWARE

NP Aug 29 1979



SINGLE USER VAX COMPUTER

Can I ask for a terminal / computer for my use here?

SEP 24 1979

B: Gordon Bell → Bob Glorioso → Bruce Delagi

79WR31K-220

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INTEROFFICE MEMO

I'd like to present

TO: Distribution

DATE: 29 AUG 79
FROM: Wayne Rosing
DEPT: MSD Advanced Sys. Dev.
EXT: 247-2322
LOC/MAIL STOP: TW/B02

SUBJ: Single User VAX Computing

I am pleased to announce the formation of a Steering Group to be responsible for guiding the development of personal single user computing within DEC. A number of us in Tewksbury, as well as other areas of the Corporation, feel strongly that a significant new market opportunity is opening up for Digital in the early part of the upcoming decade. We want to be prepared with a complete offering of hardware and software products in this area, and so I'm requesting help from a number of different areas in the DEC community. If these individuals listed below can join our effort it would be most appreciated.

My secretary will be contacting you in a few days to confirm your availability and to schedule our first meeting.

This Steering Group will meet under "Rosing's Rules" until such time as the group chooses to change its style of doing business. It is our intent that this group not become a task force whose members feel it is their responsibility to lock themselves in a room and solve problems. Rather, we would like this group to act in the mode of identifying where the problems are and what coordination and activity needs to go on; and then to act as a chartering body to form task forces or other such groups to actually go out and work the detailed issues. In this mode, I don't think any participant will feel that this activity is making extreme demands on their time. I for one have lost all patience with large unproductive meetings and wish to avoid them like the plague.

Proposed Steering Group:

Nat Parke, Chairman
Peter Christy
Sam Fuller
Peter Hurley
Dick Hustvedt
Rick Peebles
Eric Peters
Dave Rodgers
Wayne Rosing

After we have had a chance to meet a few times and get our definitions straight so that we can really talk intelligently about the subject, I propose that we add to our activity a representative from each of the product line groups.

/bc

Distribution:

Gordon Bell
Dick Clayton
Bill Demmer
Ulf Fagerquist
Bill Johnson
Andy Knowles
Jim Marshall
Bill Heffner
George Plowman

79NP31K-259

digital

SEP 26 1979

INTEROFFICE MEMORANDUM

TO: Gordon Bell

CC: Jim Marshall w/o Encl.
Wayne Rosing w/o Encl.

DATE: 25 September 1979
FROM: Nat Parke
DEPT: MSD Advanced Sys. Dev.
EXT: 247-2039
LOC/MAIL STOP: TW/B02

SUBJ: Single User VAX Project

Enclosed is a selection of memorandums relating to the Single User VAX project. I have marked sections of interest. I am anxious to have you aware of the scope of this project, our sensitivity to corporate strategy and our effort to draw upon the broadest set of resources available to get the job done.

/bc

Enclosures

Gordon — FYI. We intend to benefit from other people's experience, especially Xerox. Nat

79NP31K-166-8/22

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I N T E R O F F I C E M E M O

TO: Jim Marshall

CC: SUTC Project Team
Wayne Rosing
Bill Strecker
Sam Fuller

FROM: Nat Parke
DATE: 27 June 1979
DEPT: MSD Advanced Systems Dev.
EXT: 247-2039
MS/LOC: TW/B02

SUBJECT: MIT VISIT - 7 MAY 1979

Sam Fuller, Bill Strecker, and I spent a day at MIT, coordinated by Al Vezza (LCS) to see and discuss two projects: The LISP machine at AIL with Rich Greenblat and Tom Knight; the NU terminal at LCS with Steve Ward.

The LISP Machine

The LISP language environment was described as involving sophisticated storage management, language layers, and demanding applications such as the scientific package maxsyma. The thrashing encountered on heavily loaded DEC-10s was considered to be unacceptable. Adding more 10s was viewed as a temporary fix-loading grows, saturation sets in and the expansion cycle repeats. Thus the LISP machine concept was launched in 1974 in response to the limitations perceived in a DEC-10 time sharing system. It is a personal computing philosophy based on the following premises:

1. Hardware costs are tending toward $0.
2. Tightly coupled graphics are invaluable.
3. Disk access speeds don't scale.
4. Protection issues are mitigated.
5. High subjective value is placed on resource ownership.

The attached figure outlines the current configuration. There is substantial computing power (900 ICS, C.1974), high resolution display (CPT, 800 X 1024, text/graphics), 512KB memory, 80MB local disk, and port to an 8Mbaud network (Chaosnet). The processor front ends each of the integrated controllers (display, disk, and network) under WCS.

Some 40 machines at $30K a copy are to be built for use within the MIT community and about 6 machines have been built to date. Commenting on cost bounds, productivity gains might justify a $50K capitalization per person in a few cases and a $10K figure opens up a big market.

Results? The LISP environment is impressive - pictorial editors, exceptional quality display, network backup - all beginning to work together to give a user a strong sense of dialogue and access. It is

interesting to note that these user level attributes stand on their own to be valued, rejected or otherwise critiqued without having to pass judement on LISP the language.

In summary, there is an opportunity to capitalize on 5 years of personal computing experience at AIL. Discussing the LISP machine implementation with Tom Knight at lunch, it was quite clear that numerous architectural details, not just generalities, are directly relevant to the Single User VAX project at DEC.

NU Terminal

Ref. NU: The LCS Advanced Node, Steve Ward et.al , MIT LCS, 28 Feb 1979.

During the afternoon: Steve Ward gave a relatively formal viewgraph presentation on the NU Terminal that closely followed the above reference - thus no need to repeat many details here.

First, an aside. What I find significant is that in terms of gross intent, the NU Terminal and the LISP machine are fellow travelers. The two MIT projects emphasized many of the same themes and prioritizes we believe important to the Single User VAX project, viz. single user directed; strong interactive support; integrated processor, display, storage, and network functions. Various announcements extend the list: the Xerox Alto, the Onyx System, the Three Rivers PERQ, the Terak terminal. In short, the concept is being widely ratified. Its only a matter of time until a more worthy competitor offers a complete interpretation of the basic concept.

Though the NU terminal follows the basic concept, there are some particular points to be noted: emphasis on modular construction; range of configurations (from graphics terminals to substantial systems); independent technology evolution in subsystems; growth of baseline capability paced by evolution of high volume LSI technology; not tailored to specific applications or culture; priority on quick payoff where the overriding goal is distribution of a quantity of working machines to the MIT community as soon as possible.

Most important, perhaps, is the emphasis on strong user support at the non-machine interface. Steve Ward's describes it as "high bandwidth user interaction, high resolution graphics, single system semantics, powerful internode communication."

The hardware is specifically the following: 8086 processor, 64KB memory, 10MBytes/sec. backplane bus, 800 x 1024 line B/W CPT display, and 8Mbaud Chaosnet port. Extension allows 10-50MB disk, multiprocessors, and accerlartors.

Finally, the NU project commits to a substantial and concurrent development of a base-level operating system called TRIX, quite extensively described in the reference. Some central ideas are summarized as follows:

1. Rooted in the MULTICS and UNIX culture, particularly the latter.

2. Generalizes and unifies some of the essential UNIX constructs, rectifying some perceived difficulties.

3. Two fundamental structural elements: Processes and Streams.

4. Processes include all traditional objects - files, directories, devices, etc.

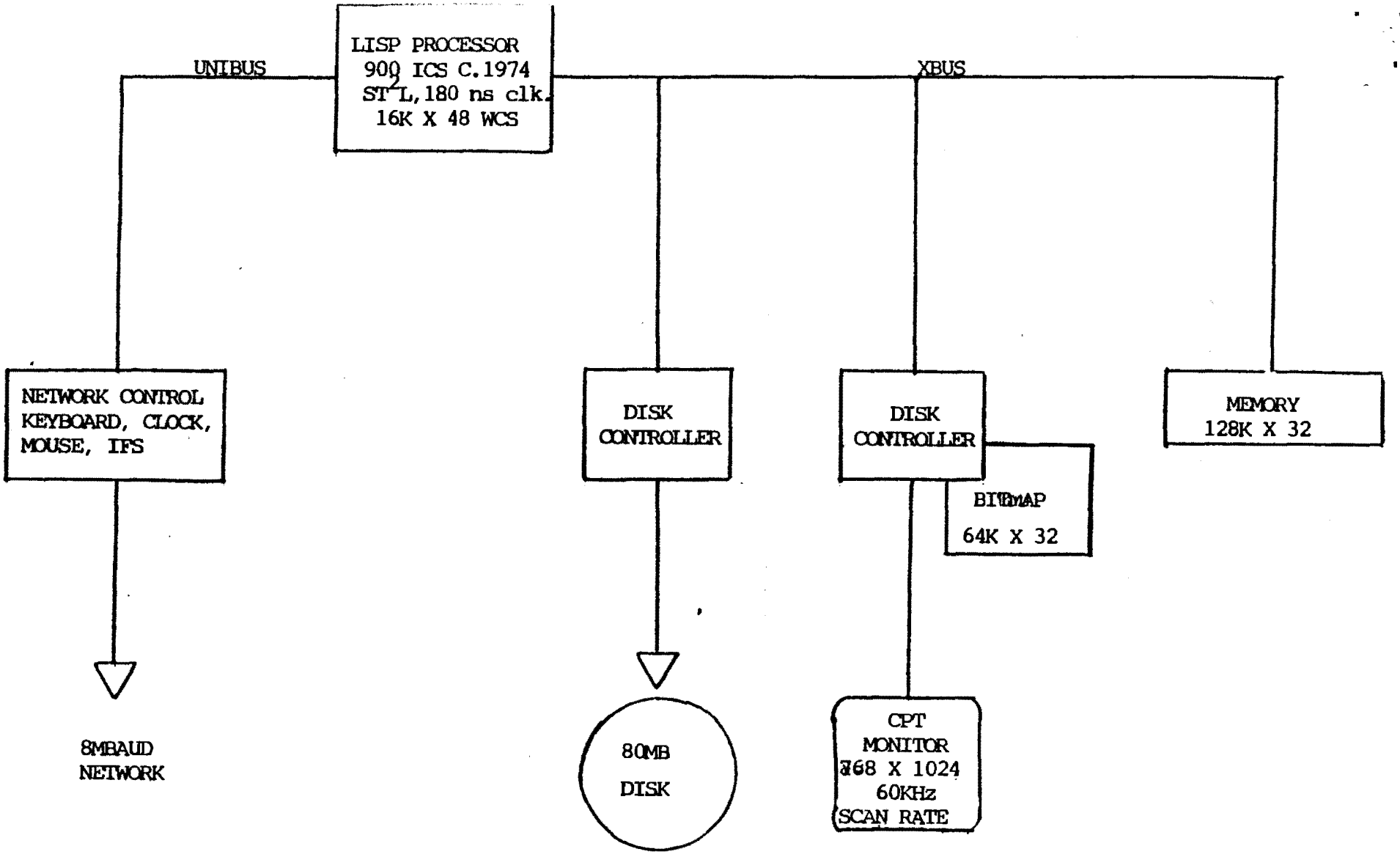
5. Streams are assymetric (Master - Slave), full duplex communication paths linking processess.

6. Semantics are associated with streams.

TRIX then proceeds to build a highly structured scheme on the basic abstractions: naming conventions, environments, shells, and other such entities - taking care to define a few special case functions where structure gets in the way of efficiency.

In summary, the hardware appears straightforward, notable for a judicous selection of technologies, and systematic engineering directed toward practical goals. The software, TRIX, is the more creative, lengthy effort - significant as another reminder of UNIX's popularity.

NGP/djl



LISP MACHINE BLOCK DIAGRAM

Gordon - FYI, please note sections marked. Nat

79NP31K-139-7/43

d i g i t a l

INTEROFFICE MEMO

TO: Jim Marshall

CC: Don Freniere
Wayne Rosing
John Sofio
Bill Strecker
Joe Winn

DATE: 5 June 1979
FROM: Nat Parke NSP
DEPT: MSD Advanced Systems Dev.
EXT: 247-2039
LOC/MS: TW/B02

SUBJECT: MONTHLY STATUS REPORT - MAY

M.I.T. Visit

Sam Fuller, Bill Strecker, and I spent a day at M.I.T., coordinated by Al Vezza (LCS) to see and discuss: The LISP machine at AIL with Rich Greenblat and Tom Knight; the NU terminal at LCS with Steve Ward. The following points summarize a fruitful day:

1. The LISP user environment (operating system, editors,terminal facilities, network facilities, etc.) is impressive. Independent of any prior judgment about LISP as a language, there is much to learn from AIL's experience with the integration of high performance display (text and graphics), substantial computing power, local mass storage, network interface, and support software ----- all in the hands of a single user.

2. The NU machine is also interesting as a project that explores the functionality of network terminal nodes, high resolution graphics (CPT monitor), modular hardware structure, migration across non-homogeneous processors (8086 -- Z8000 -- 8800), and UNIX based operating system concepts (TRIX).

3. We intend to meet with Dick Eckhouse to plan follow on interaction with M.I.T. In Al Vezza's view, LCS is open to any proposals we might wish to put forth - consulting agreements, grants, joint ventures, etc.

Visits to M.I.T. and Stanford this past month plus involvement with the CMU proposal suggest the notition of a working set of relationships with all the major computer science universities viz. CMU, M.I.T., Stanford, Berkley, and Caltech. Over time these relationships could grow to the point where there is a sustained level of investment and return. I have already started to capitalize on DEC's stature in the university community to help front-end the Single User VAX project. There is great leverage here and I plan to pursue

this opportunity in coordination with others already active such as Dick Eckhouse, Rich Peebles, Bob Kusik, Chuck Kaman,as well as Bill Strecker and Sam Fuller.

SOUTHWEST/WEST COAST TRIP

Don North and I made a SUTC oriented trip to the following places:

1. DEC Albuquerque. Only a few people including Joel Kaufman and Mat Tynan are actually involved in Southwest Advanced Development Engineering (SWAVE). The day included: Tom Stockebrand's staff meeting, a briefing on our SUTC project, an update on their video experiments, and a tour of the plant.

2. Stanford CSL. Forest Basket coordinated a very productive day at CSL. Several topics were discussed at some length: The follow on graphics system to the VGT; the SUTC Display functional specification; Stanford's integrated DA system (CALMOS, SCALD, and SUDS-2, etc.); collected comments on VMS from Stanford and other universities.

3. Signetics. Bob Reid (DEC account manager) coordinated another productive day. Several specific topics were on the agenda: The ISL gate array; FPLA related developments; S i g n e t i c s strategic planning to support key EDP customers competing with IBM.

4. Evans and Sutherland, Salt Lake City. Jim Callan (Marketing Support Manager) guided us through a day in the life of an OEM including: Overview of E & S hsitory and the high end graphics marketplace; demonstrations of the flights simulation and picture systems; discussion of DEC products and E & S's future requirements. (I might also add that those DM reports are real - high regard for our products; actue frustration with our service.)

LSI VAX (STICKS TERMINALS)

Caltech's 11/03 software has been converted, assembled and loaded into the 11/04 of the first terminal, the display controller modules are scheduled for wire wrap in early June; hardware turn-on is scheduled for 18 June 79.

The latest delivery date for the first Hitachi monitor is the end of June. We are having great difficulty confirming this date and pinning down delivery commitments for the remaining two units. Hitachi monitors currently gate July completion for all three STICKS terminals. We had hoped to supply VT100's with the terminals and we are still attempting to improve a September delivery date.

Jack Burness is having equally difficulty in transferring Caltech software to CAD5/6. SIMULA source code has been secured from DECUS and Jack is rebuilding the SIMULA compiler from scratch in attempt to identify the incompatabilities between the Caltech and Tewksbury versions.

SINGLE USER VAX

Project subplans have been written for each of the functional areas of the project. Current status is as follows:

Display. After digesting many documents and verbal comments from sources both internal and external to DEC, Don North has drafted a fucntional specification. We reviewed it with Forest Basket at Stanford and confirmed that it is generally consistant with his current philosophy.

We have also identified the need for REGIS extensions to Charle Rupp that are required handle multiple bit planes, and the transposition of planar objects. We plan to review our implementation plans in detail with Charle and Len Halio now that our analysis of high end display requirements has begun to firm up.

We are convinced that high band width between the display subsystem and the NEBULA host is essential to achieving a dynamic, interactive user environment. In this light, the recent BI development is encouraging, offering the possiblity of bandwidth, address space, and the standardization necessary to migrate the SUTC display to other systems. We are also looking forward to the prospect of having Forest Basket (Stanford) and Bob Sproul (CMU) periodically in residence in Tewksbury. I view their role as two part: first, as a source of practical guidance to the SUTC project; second, as co-developers of the general graphics architecture and software structure required to bind graphics subsystems to applications. These structures are implied by REGIS (viewed as a graphics communications protocol) but are not specifically realized in the current GIGI implemenation.

Mass Storage. A pair of Shugart fixed media disk drives and a pair of DEI 3M cartridges tape drives have been ordered for the test bed. We will also want to order and evaluate a pair of 210mm micro disks when they become available in the fall. In the meantime, we are examining the numerous alternatives for coupling disk and tape together as an integrated subsystem.

The current tack is to view the tape purely as a personal and archieving media. Access need only be sequential but must be capable of total volumn transfer of 10MB in 2 minutes or less to eliminate the need for a removable disk media. We have probed various drive, cartridge, and head vendors to confirm feasability; all the technical aspects have been demonstrated individually but not collectively. Tape Engineering has been urged to follow up on DEI's offer to work with us. Beyond the rudiments of disk and tape drives there are

numerous interesting and unresolved systems issues: disk vs. tape formats; disk-to-tape volumn ratios, disk management schemes, parallel access schemes for high density tapes, error control and so on. We are convinced that an innovative solution exists and we are coordinating a broad set of disciplines - from materials to operating systems - to find it.

Operating System. Dave Sager continues his effort to establish basic VMS credentials. He is working with Hustvedt and Company on Release 2 system builds to gain experience; he has also gone through the exercise of writing and debugging a display oriented I/O driver. In the processs we believe we understand how bit maps properly fit within the VAX memory architecture.

Applications/Demos. As we proceed to make the rounds through the product lines, we are pursuing two objectives: 1. defintion of functionality requirements; 2. identifying sources of benchmarks and demonstrations programs. We are finding considerable support for the system attributes described in the original project plan with some specific exceptions. TOEM, understandbly, requires the ability to integrate additional devices into the system; ESG is concerned about display dynamics and inadequate disk capacity.

We are also beginning to look at the more technically orientated commercial applications; there is an interesting match between SUTC and factory process monitoring and data collection market addressed by MDC. Wayne Uejio will be driving an information gathering process indefinitely - probing the product lines, organizing visits to customer field sites, translating useful insights into system requirements, gathering together usable software, and finally patching together demo software to exercise and evaluate the system.

Network Port. This activity is on hold until Art Lim is free from the LSI-70 task and until the interconnect strategy, and the NI in particular, are futher articulated.

Finally, we are pursuing, with Bill Zimmer, a tie in between SUTC and the approachable machine project in R&D, and we are asking Dick Eckhouse to look into an NSF grant to Cornell to study graphics.

WORKLOAD CHARACTERIZATION

Software monitor kits have been distributed to 20 software specialists. Each specialist will install the monitors on approximately three systems in the field. Plans include quick-turn-around of statistical data for the cooperating users as well statistical data collected for the project on the utilization of computer resources. The immediate project objective is anaytical data on computer performance, with synthetic benchmarks to follow in FY80 pending further funding. Otherwise, Cheryl Wiecek continues design of the NEBULA memory controller simulator.

MONITORING

Product line monitoring continued this month. Meetings were held with TOEM, Graphic Arts, and the Federal Systems Group to establish contact and exchange information.

Nat

NGP/djl

Gordon — FYI, please note sections marked. Nat

79NP31K-167-8/23

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I N T E R O F F I C E M E M O

TO: Jim Marshall

CC: Don Feniere
Wayne Rosing
John Sofio
Bill Strecker
Joe Winn

FROM: Nat Parker
DATE: 27 June 1979
DEPT: MSD Advanced Systems Dev.
EXT: 247-2039
MS/LOC: TW/B02

SUBJECT: MONTHLY STATUS REPORT - JUNE

Semiconductor Technology Planning

In May, I visited Signetics to discuss two specific developments reported elsewhere: the ISL gate array and FPLA related components. As a means of generalizing interaction on advanced development issues, Signetics has proposed initiating a specific process for coordinating advanced product and process planning with the long range needs of key customers such as DEC. Signetics explains the rationale as follows: Philips has designated Signetics as the principal site for developing VLSI for the EDP marketplace (as opposed to focus in Europe on the consumer market) and Philip is appropriating $15M to Signetics in CY79-80 to further support this role. Signetics sees its future success directly tied to its key customers ability to compete effectively against IBM. To address this perception, Signetics is establishing an EDP strategy planning function (John Woodman, Manager). This function is to be closely allied with the the Advanced Development Laboratory, formerly a broad-scope, general R & D group. In turn, a new R & D group more oriented toward fundemental technology is being formed, partly composed of staff from Europe (Eindhoven) to facilitate technology transfer from Philips. Signetics has requested an opportunity to make a substantive presentation to DEC, Tewksbury in August and I have committed to coordinate the meeting.

Single User VAX

Project momentum and belief in the project's significance continues to grow. As an advanced development vehicle, it addresses at a minimum three issues believed to be important: system integration and bounding, graphics as a means of elevating user interaction to a new plateau, and full-function computing as a terminal in a network environment. At last count there are at least seven good Single User Computers examples that generally adhere to a basic formula, though there is considerable variation in performance, sophistication, and cost. Over the past several months, the project team has engaged in substantial dialogue with

the product lines and several universities. With the Single User concept established and the key functional objectives well on the way to resolution, the project is bearing down on the detail mechanics of a first-pass hardware implementation. The pivitol milestone is a stand-alone breadboard running by December. Activity in specific areas is summarized as follows:

Displays: In deference to standardization, we plan to interface to the BI rather than NEBULA's extended data path. More than any other subsystem, the display controller benefits from the overlap gained from an integral processor with DMA capability, and the BI is the interface of preference. Having agreed to supporting a corporate standard for graphics primitives, time has come for all concerned to specify a graphics language based on REGIS. We can then proceed to block out a dispaly controller implementation. Given that the microarchitecture envisioned is RAM controlled and flexible, the language defintion need not be complete or final.

Mass Storage: We are following the numerous microdisk announcements made at NCC as well as the further exploitation of the 3M tape cartridge by DEI. The need for Aztec and TU5900 continues to be felt. With respect to the December milestone, we are planning to adapt a Shugart 14" disk to the same modified CDC interface adopted by the NEBULA IDC. We also intend to replicate some of the DEI tape drive electronics to achieve parallel operation but will not seek, at this time, to have the tape heads or mechanics modified to achieve higher performance. We also intend to evaluate one or more microdisks as they become available. We continue to be dependent on Mass Storage to establish a strategy that develops the disk and tape drives ultimately needed.

Operating System: Aside from consolidating knowledge of VMS, Dave Sager spent the past month helping to resolve issues relating to the integrated subsystems.

Applications/Demos: Wayne Uejio continues to focus on establishing PL interest. Contact continues with MDC and ESG. A formal presentation to LDP/MDP is planned for July. We expect the upcoming conference on computer mapping at Harvard and the SIGGRAPH conference in Chicago to futher our insights into potential markets for Single User VAX.

Network Port: This activity remains on hold until the NI strategy takes further shape.

Finally, we are hoping to finalize a consulting contract with Forest Basket at Stanford in the near future.

WORKLOAD CHARACTERIZATION

The NEBULA memory controller simulator is operational. The paper on PDP-11 performance simulation has been accepted at the

Conference on Simulation, Measurement and Modeling of Computer Systems.

INTERNAL MONITORING

No significant events.

NGP/djl

Gordon — FYI, please note sections marked, Nat

79NP31K-192-8/47

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I N T E R O F F I C E M E M O

TO: Jim Marshall

CC: Don Freniere
Wayne Rosing
Bill Strecker

FROM: Nat Parke
DATE: 31 July 1979
DEPT: MSD Advanced Systems Dev.
EXT: 247-2039
MS/LOC: TW/B02

SUBJECT: MONTHLY STATUS REPORT - JULY

Single User Vax

Display Subsystem: Don North is formalizing the functional requirements in written form, available for review in early August. We continue to maintain our commitment to fit within an overall corporate architecture. A recent periodic meeting with Charle Rupp and Len Halio has resulted in a memorandum from Charle that formally acknowledges Single User Vax's need for a parallel architecture definition. It complements the pre-exsisting serial form of the REGIS architecture. Single User Vax will continue to drive "parallel REGIS" as a corporate interface, subject to review through continued contact with R&D and Video Engineering. In regard to high performance video hardware development, a CPT-like 1000 line B/W monitor from Monoterm is under evaluation with the intent of acquiring rights for production in the far-east, pending support from the Word Processing Product Line. There is no equivalent color effort to date; Single User Vax is the likely candidate for driving the P/Ls to support it.

Mass Storage Subsystems: Dave Sager and Lewis Costas have worked out most of the conceptual details for combining fixed disk with 3M cartridge tape. With Tape Engineering decommitting from assigning an engineer to work with us, we now bear the responsibility for modifying a DEI drive to write 4 tracks parallel (vs. serial) at 90 ips (vs. 30 ips). To date, the DEI drive electronics have been reverse engineered and documented, writing at 90 ips has been demonstrated as feasable, and a 4-track read/write board has been designed to fit the single track board space. The trick is the elimination of track select logic, and various circuits that cope with read-after-write capability, no longer needed because tapes are verified during rewind. A 12X tape throughput improvement appears possible that more nearly matches normal (average fragmentation) disk performance. We have not yet identified any obstacles to achieving our goal of moving a single user with 10 Mbyte of file space on and off a system in 60 sec. or less. A functional specification is being written for review in mid-August.

Operating System: There was no VMS related activity to report this month.

Operating System: There was no VMS related activity to report this month.

Network Port Subsystem: With regard to the interconnect media, we are anticipating resolution through closure on a licencing agreement with Xerox for Ethernet II as the NI. With regard to the implementation of a port, we are looking to Dave Rodger's group to implement an NI-to-BI port in an acceptable form factor. The NI remains key to the full realization of the Single User Vax concept and the project will document functional requirements for both the NI hardware and software as the project evolves.

Applications/Demos: In parallel with continuing efforts to tabulate potential applications and adaptable software for demos, Wayne Uejio has undertaken the task of defining the essential features of a graphics (display/pictorial) editor and its bearing on VMS and other closely related utilities. To put our review of editor needs in DEC context we are also attempting to account for all other projects that might have some relevance, e.g. FMS-11, SPASM, CATS, and several activities in R&D. It's fairly evident at this point that there is no adequate baseline that supports the evolutionary development of a display editor. Because this fundementally different style of editor is crucial to the success of Single User Vax, we intend, with the help of Sam Fuller, Rick Peebles and others, to make the need visible and to convince O^2D and Software Engineering to allocate adequate resources to develop the essential software, needed for single user systems.

Consulting: I look forward to Forest Baskett joining the Single User Vax project as a consultant starting in August '79 and continuing through at least FY80. Currently on the staff of the Computer Systems Lab and SLAC at Stanford, Forest has extensive, substantive background in both hardware and software system development, particularly in the graphics systems and operating systems areas. Of particular note is Forest's comprehensive access to information relating to interactive, single-user oriented systems. In relation to the Single User project, I am looking for Forest to function as a convincing advocate of the basic goals, as an individual contributor to architecture definition, and, in role of a realtive outsider, as a hard-nosed, forthright critic of our efforts. Initially, I expect Forest to address the hardware architecture of the test-bed, specifically the graphics subsystem. Next on the agenda is the display editor and its impact on VMS and related utilities. Beyond that his attention will migrate outward to the network and related software.

Sticks Terminals

All Hitachi monitors have been delivered and the first set of wire wrap modules have returned from Acton. With no further external factors to contend with, I expect checkout to proceed smoothly and first delivery to be made in mid-August. I would hope to see this project wrapped up by early September.

Workload Characterization

Cheryl Wiecek continues work on the VAX trace program, expanding the scope of data collection and adding further structure and documentation....With additional revisions made, the NEBULA Memory Controller Simulator is producing preliminary results.....Paul Lego has partially completed modification of the Bluefish Simulator to model J-11 performance. First results indicate a 5% margin over 11/70 on the PRIME benchmarks....Finally, Wayen Uejio is writing a final report on the RSTS Monitor project. Arrangements are being made for SPA to continue to generate reports based on collected tapes now that our direct involvement has terminated as of the end of FY79....As of next month, AD activity in the workload characterization and performance simulation areas will be reported through Wayne Rosing.

Internal Monitoring

No significant events this month. As of next month AD activity in this area will be reported through Wayne Rosing.

Signetics Strategy Planning Meeting

As of the end of July, the meeting is confirmed to take place 16 August 1979 and it will include key engineering representation from the Signetics factory as requested.

Nat

NGP/djl

Gordon – FYI, please note sections marked.
Nat

79NP31K-226 10/10

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INTEROFFICE MEMO

TO: Wayne Rosing

CC: Don North
Lewis Costas
Dave Sager
Wayne Uejio

DATE: 5 SEPT 1979
FROM: Nat Parke
DEPT: MSD Advanced Sys. Dev.
EXT: 247-2039
LOC/MAIL STOP: TW/B02

SUBJ: MONTHLY STATUS REPORT - AUGUST

Single User VAX

Display Subsystem: Work on the functional specification has been temporarily interrupted by the Sticks Terminal project. Don North should have the specification completed and available for review by mid-September.

There are three concurrent display hardware development projects that are oriented toward graphics and committed to architectural compatibility: VK100, VT125, and Single User VAX Display. VS(V)-11 is excepted because it is a CSS product, essentially a VS60 replacement, and stroke-vector oriented. To date, the burden of drafting, reviewing, and revising the necessary architectural documentation has been carried almost entirely by Charle Rupp (R&D - VK100), and Tom Powers (Video Engineering - VT125), with help from Don North (Mid-Range Advanced Systems Development - Single User VAX). I am concerned that there is little evidence of broader corporate interest in the efforts of the three key participants. Numerous DEC organizations will soon be confronted with the need to relate application objectives to the evolving architecture standards. An acceptance process must take place concurrently. I propose that O^2T (Sam Fuller) sponsor the graphics architecture definition activity and help give it the visibility and importance that it deserves. As graphics oriented terminals become increasingly integral to general computing, it seems appropriate to attach formal support and control to graphics architecture analogous to that attached to VAX architecture.

The Single User VAX project has been seeking an experienced hardware designer to implement the display subsystem and to supervise the overall design and integration of the testbed. We have extended an offer to a qualified candidate and expect the offer to be accepted.

Mass Storage Subsystem: The modification of the DEI tape drive is proceeding well. Dave Sager has developed an efficient 8-to-9 group code and a circuit design that supports four-track parallel recording at 90 ips. A lot of thought and analysis has gone into understanding tape flux transitions, bit pattern sensitivity, data recovery, and the subtle tradeoffs involved in moving from single track MFM to four-track group recording. A four-track Read/Write electronics PC board has been laid out to fit the single-track board space. Etch is preferred to the alternative of re-engineering the DEI mechanical package to place a larger wire-wrap board proximate to the tape head. Design of a serial-parallel interface is now underway. The plan is to partition the logic onto three wire-wrap duals and to "bolt" a 3-slot block to the back of the DEI drive. We hope to have the DEI drive fully modified and working by mid-October.... Meanwhile, Lewis Costas is learning SUDS and creating a database for the Shugart-to-SMD personality card.... Finally, Dave Sager has completed a first draft of the Mass Storage Subsystem functional specification and has circulated it for review by the project team.

Network Port: No activity this month.

Software: From the outset, the Single User VAX project has recognized that hardware and software requirements must be defined concurrently. Both aspects of functionality are viewed as integral to the product concept. Now that the Single User VAX concept has gained some visibility within DEC, it is time to further pursue a course of action that achieves resource integration across organizations. As proposed by Wayne Rosing, a high level steering group is being formed to consider the full implication of the project, to evolve a comprehensive strategy, and to sponsor the activities required to implement the strategy. I view the steering group as a specific means of strengthening the project's ability to take responsibility for systems engineering. First on the agenda is the designation of a task force to define an integrated software development plan and to bind together a relatively disjoint collection of current activities addressing VMS, user interfaces, demos, and applications.

In the meantime, I have taken some specific action relative to software:

1. Rick Peebles and I made a joint presentation to Bill Johnson's staff. We made an explicit request for a software advanced development project to complement the

Tewksbury hardware project. We received a clear commitment to address our request. We came away with a number of leads to follow up: Dick Snyder's interest in getting involved, a request to explain the relationship between profession based services (as defined by Rick Peebles) and personal computing (as defined by Andy Knowles), Bill Keating's request for more information on Xerox Alto, and a request to meet again with Bill Johnson in September.

2. An agreement has been reached with Ken Lodding in Commercial Engineering to work on the Single User VAX project. This agreement is supported by Bob Daley and Doug McKlean who holds responsibility for human interface development and Commercial VAX. I view our token funding as a gesture to seed further software development. Commercial Engineering will fund Ken through December and Single User VAX will fund him through the balance of FY80. My immediate objective is the application of Ken's dialogue simulation tool, SPASM, to the creation of interactive demos that illustrate Single User VAX's visual interface capabilities and application potential. Long term, this relationship gives us a tangible entree into the commercial planning process and a means of influencing the development of management oriented, creative problem solving applications that augment the traditional transactional and production oriented applications that exist today.

LDP/MDP Presentation:

We made a well-received presentation on Single User VAX to LDP/MDP on 1 August '79. At least one listener expected a modest scheme to attach a VT125 to a NEBULA, not the more comprehensive program we outlined. Our timing was opportune; the long range planning group (2-5 years out) is just beginning to think about MINC-like systems based on VAX architecture, integrated disk-tape mass storage, and up-graded display functionality. Aside from the clarification of small points, two areas of discussion stood out: the subsystem attachment issue (also raised by TOEM) and the user support issue. Regarding attachments, our current position is that Single User VAX will only support memory expansion, disk substitution at the SDI interface, a laser printer interface and a network (NI) port. Market objectives and packaging economics dictate these constraints. However, the BI is the planned internal interface for Single User VAX subsystems and there is no

technical obstacle to integrating Single User VAX subsystems into standard packaged systems. Regarding user support, LDP is quite sensitive to the post-delivery, cost-of-sale cost element in relation to the product sell price. To determine profitability at a given sell price, they need to predict a projected incurred cost-of-sale based on a user self-sufficiency model that considers factors such as user installation, system documentation, support software, self maintenance, etc. In short, we can expect LDP to require that Single User VAX meet certain product maturity criteria before they commit to selling it. The bottom line: our speculation on an FY82 introduction seems early to them rather than late.

Sticks Terminals:

17 August '79 was black Friday. We concluded that the electrical implementation of the current display hardware was inadequate. The Caltech design is operational at Caltech and the DEC copy was built to the furnished prints. But our 16K RAM bit-map implementation did not adhere to mandatory guidelines for layout, power distribution and decoupling. We are in the middle of a three week crash effort to rebuild the system. The new approach combines two MS11K modules with minimally redesigned control logic, properly laid out on a new wire wrap board. At the two week point, the control logic has been reworked and entered into a SUDS database. We are now dealing with the DEC process for getting NC tapes and wire wrap service and find it exceedingly difficult to get fast response. We are keeping the pressure on and we are planning on a double shift effort to debug the rebuilt system. Although there is an ongoing parallel effort to upgrade the original modules, we do not expect that effort to succeed.

Signetics Strategy Planning Meeting:

The meeting took place as planned on 16 August 1979. Little information was presented that went beyond that normally disclosed to a preferred customer such as DEC. Nevertheless, there was a chance to meet with Signetics at some length with the intention of continued interaction in the future. There was a follow-up meeting in Gordon Bell's office during the late afternoon, and two meetings in Tewksbury the next day--one to review current problems with the COMET Gate Array and one to explore the proper conditions for a future joint gate array development.

/bc

Nat

Gordon - FYI, specifically page #2

Nat

79NP31K-231 10/13

| d | i | g | i | t | a | l |

INTEROFFICE MEMO

TO: Forest Baskett

CC: Jay Connor
Sam Fuller
Jim Marshall
Wayne Rosing

DATE: 7 September 1979
FROM: Nat Parke Nat
DEPT: MSD Advanced Sys. Dev.
EXT: 247-2039
LOC/MAIL STOP: TW/B02

SUBJ: Consulting Agreement and Open Purchase Order for the Single User VAX Project

Overview

Forest - this memorandum is primarily addressed to you and covers prior events, future expectations, and some mechanics. The CCs relate to the open purchase order (Jay Connor), the underlying contract (Sam Fuller) and approval (Jim Marshall and Wayne Rosing).

Brief History of Events and Circumstances

Mid-Range Advanced System Development's decision to develop Single User VAX arose in part from recent interest in personal computing expressed by several major computer science universities, viz., CMU, MIT and Stanford. Our introduction through Sam Fuller and the subsequent identification of mutual interests was a natural outgrowth of Sam's ties with CMU, Stanford, and DEC-Tewksbury. Your experience in operating systems, displays systems, and research-oriented computing, as well as your specific familiarity with VAX and other DEC products, are directly relevant to the Single User VAX project. Several meetings, telephone conversations, and information exchanges substantiate that an informal consulting relationship has already been established. Although an informal consulting relationship might be expected to continue indefinitely, I would like to enter into the formal consulting agreement that we discussed during your last visit here in Tewksbury. The agreement provides financial compensation in return for a more regular and sustained contribution to the achievement of specific project objectives.

Purpose and Scope of a Consulting Agreement

In general, I am seeking advice on the definition of the functional requirements for Single User VAX and practical

guidance on implementation. In a consulting capacity, I would expect you to review architecture and design documentation, participate in project meetings from time to time, provide access to pertinent information within Stanford and the University Community at large, prepare short memorandums that articulate specific insights and viewpoints, and engage in other tasks that might occur to either one of us and are agreeable to both.

Outline of Specific Work

I see three segments of work, each addressing areas of functionality; order and duration follow the overall project schedule.

Near-term (July '79 - June '80). The focus is on the Single User VAX hardware testbed, specifically the integrated subsystems: display, printer, mass storage, and network port. Emphasis will be on the display and printer. Early consulting equates to participation in a corporate level terminal architecture (broad sense) definition process that addresses the following factors: SIGGRAPH core standard, processor-display/printer interfaces (graphics language (REGIS)), user-processor interface (command language), and graphics/text display objectives (function, quality and performance) specifically for Single User VAX. Early consulting also includes, at a lower level of effort, review of the Mass Storage approach, and comment on the Network hardware that is being developed elsewhere in DEC. Later consulting equates to advice and guidance on Single User VAX hardware implementation with emphasis on the display and printer subsystems.

Mid-term (October '79 - TBD). The focus is on the total software needed to support Single User VAX. Consulting equates to participation in a corporate level personal computing (professional sense) software architecture definition process that adresses the following areas: operating system, file system, command interpreter, user interface, utilities, application interfaces, applications (services).

Long-term (TBD - TBD). The focus is on the network environment and the distributed processing oriented functionality not addressed in a stand-alone context. The specific nature of consulting is TBD.

Administrative Information

The foregoing outline of work is meant to serve as a general indication of expected involvement. Individual tasks and deliverables are to be specified largely by verbal agreement and modified by mutual consent as seems desirable. Timely payment for services rendered is not binding on these specific verbal agreements and is solely related to the presentation of invoices for time expended and expenses.

I have requested DEC to write an open purchase order for the balance of FY80 (October '79 through June '80) not to exceed $13.5K total, including consulting time and travel expenses, all to be charged to #E020-02242. Payment should be 10 days net upon receipt of invoice rendered monthly. Information needed for inclusion in the open purchase order should be abstracted from this memorandum. The basis for the open purchase order is a standing contract, negotiated at prior date by Sam Fuller, Manager, Office of Technology. This contract contains a description of fees, procedures for payment restrictions on information disclosure, and conditions for terminating the open purchase order.

/bc

Nick

DIGITAL

INTEROFFICE MEMORANDUM

Nat Park
Tom Dundon
Bill McDonough
Dave Sager
Wayne Uejio
Art Williams

DATE: 11 September 1979
FROM: Walt Tetschner
DEPT: Terminals Engineering
EXT: 6788
LOC/MAIL STOP: ML5-3/E12

SUBJ: PRINTER ENGINEERING/MSD NIP MEETING

The purpose of this note is to document the conclusions that I believe we reached at our 7 September meeting.

1. Definition of the NIP architecture should be a joint Printer Engineering/MSD effort. Distribution of Intelligence between the printer controller and host needs to be thought out and specified.

2. MSD will serve as the link to the CMU, Stanford and Caltech work being done in this area.

3. The 300 dots/inch vs 240 dots/inch issue needs to be thoroughly addressed. Xerox has standardized at 300; and IBM, Siemens and most everyone else has gone to 240 dots/inch. Can our system be layered so that fonts and form generators from either world could be transfered to our system.

4. We will get together again when we have the Canon printer at Maynard, which should be in a few weeks.

WT:ljf

Gordon — FYI. Also, I have asked Forest Beckett to put together an information package relevant to laser printers — interfaces, fonts, etc.

Nat

Gordon — FYI NAP

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+---+---+---+---+---+---+---+

INTEROFFICE MEMO

TO: Doug McLean

CC: Ken Lodding
Jim Marshall
Rick Peebles
Wayne Rosing
Dave Sager
Wayne Uejio

DATE: 14 September 1979
FROM: Nat Parker NGP
DEPT: MSD Advance Sys. Dev.
EXT: 247-2039
LOC/MAIL STOP: TW/B02

SUBJ: 30 August 1979 Meeting

This memorandum summarizes two areas of discussion: Ken Lodding's involvement in the Single User VAX project and the relevance of Single User VAX to Commercial Engineering interests.

Ken Lodding's Involvement

My understanding is as follows: Ken Lodding's far term objective is contribution to color graphics applications development at DEC. Near term, there is no funded project within Commercial Engineering that adequately meets his requirements. The Single User VAX project offers an acceptable alternative because of the emphasis on graphics functionality and the planned support of color graphics applications in the future. Given Ken's background and interests, Wayne Uejio and I proposed two task areas that seemed appropriate: Application and extension of SPASM to simulate user interfaces; the definition and development of a screen editor as an outgrowth of the first task and as part of the overall Single User VAX software effort. Pending resolution of administrative and funding issues, Ken accepted the proposal for several reasons. The assignment is interesting in its own right; it capitalizes on SPASM; it builds a foundation for later work on color graphics. Commercial Engineering supports an assignment on Single User VAX because the project is sympathetic to Commercial Engineering interests as well as Ken's career objectives. In view of the above, we arrived at the following agreement. Ken Lodding will work on Single User VAX for the balance of FY80, funded by Commercial Engineering through December, funded by Distributed and Mid-range Systems from January through June.

Relevance of Single User VAX to Commercial Engineering Interests

I gave you an overview of the Single User VAX project's background, functional objectives, approach, project content, dependencies and commitment to corporate goals. Among the several points emphasized, you keyed on human engineering and the user interface as particularly important. I agreed to follow up on

this area of interest with Jay Nickerson. We discussed potential Commercial Engineering involvement in the Single User Computing Steering Group and the need for us to stay in contact. We explored some philosophical and definitional issues: The continuum of user terminal definitions from dumb to intelligent to self-sufficient as single user computers; the continuum of interconnects from dedicated lines to local networks; the range of implied computing styles from hierarchical (host-terminals) to cooperative (single user computers - network servers). We also explored the potential for single user computers (VAX form in particular) in commercial markets. A distinction was made between "routine vs. creative applications" (my particular choice of words by which I means the difference between conventional batch and transactional data processing vs. analytical and interpretive data processing). Creative applications relate to managers and other professionals such as financial analysts (your example). You cited the drive toward relational data bases. I suggested that the development of graphics-based tools directed toward more flexible and effective data presentation might follow. The implementation of tools directed toward local data manipulation (by the user) might be the next goals. These tools would be algorithmic in nature, employing graphics and menus to soften the programming requirements for non-programmers.

As I reflect on our meeting and summarize what I recollect, the term, "creative computing" continues to evoke in my mind the right feeling for some future opportunities. I look forward to pursuing the concept further with you.

/bc

Larry Gil Stel BT, Bob Glass. + ml

digital

INTEROFFICE MEMORANDUM

FYI

TO: Andy Knowles

C.C. Mike Tomasic

DATE: 13 August 1979
FROM: Dick Strauss
DEPT: Corporate Marketing
EXT: 3-6746
LOC/MAIL STOP: ML12-2/A16

AUG 27 1979

SUBJECT: PERSONAL COMPUTERS

Let's get OMSI - Pascal 2 on PDT and then write some — products!

We are scheduled to get together on August 21 at 2:00 to discuss:

- The attached list of Applications
- My progress with the pilot program
- Interrelationship between electronic mail post office and personal computers
- Heathkit WH89
- RX02 on PDT 150 for the stores
- → Where does application software come from?
- PDT 150 commercial software

See you then!

/jeb

Gordon Bell

The arrow points to the key question. How do we — get a series of applications done so we have "a product to market called a personal computer."

Let's discuss this —

Andy 8/21/79

PERSONAL COMPUTER APPLICATIONS

NO PRIORITIES

Electronic Mail Related Applications:

- word processing
- data entry - forms processing
- draft entry
- display reprocessing
- calendar
- tickler file
- mail entry
- mail pickup
- running monthly report
- scheduling meetings
- airlines/hotel reservations
- weather reports
- calculator
- stockmarket
- international time
- phone book (directory)
- currency conversion
- library book order
- health insurance forms
- trip expense reports
- system "help" messages
- order entry
- "trouble desk system" (e.g. Field Service at each unit with electronic mail to LARS)
- ROI calculations

Games

- trivia quiz
- chess
- bridge
- art
- biorhythms
- adventure
- star trek
- cribbage
- backgammon
- slot machine
- etc.

Other Application Areas:

- programmers workbench
- slide preparation
- table to graphics conversion
- accounts receivable
- accounts payable
- "checking account"
- inventory
- keyless entry
- handicapped person terminal
- educational machine
- income tax preparation
- electronic funds transfer
- recipes/diet
- medical consulting
- real estate
- sports scores
- buy by computer advertising
- lottery
- restaurant/book/movie reviews
- agricultural information
- career/personnel placement
- first aid
- maps
- consumer information
- credit checking
- computer controlled microfilm retrieval
- cryptology
- navigation
- communication/information center
- environmental control system
- security systems
- statistical packages
- cash register

SUPPLEMENT TO THE HEATHKIT ELECTRONIC CENTER CATALOG NO. 81

New H89 desk-top personal computer in one compact unit

- Floppy disk storage
- Smart video terminal
- Two Z80 microprocessors
- 16K RAM expandable to 48K
- Professional keyboard

Now in one compact, desk-top computer, you can have all the power and built-in peripherals needed for any personal computing task. The new 8-bit All-in-One Computer makes it easy to computerize your home or business. It's loaded with convenience features that make it easy to program and operate.

Smart Video Terminal

The All-in-One Computer has one of the most sophisticated terminals ever designed. Both terminal and computer have their own Z80 microprocessors, so terminal never shares processor power with computer, as do most desk-top computers. That makes this terminal capable of a multitude of high-speed functions.

Heavy-duty professional keyboard

All terminal functions can be controlled by keyboard or software. Eight user-definable keys let you program your own special functions. Baud rates of up to 19,200 are keyboard selectable.

Direct cursor addressing lets you insert and delete characters and lines anywhere on the screen and gives you line graphics capability from keyboard or computer.

Sharp screen image

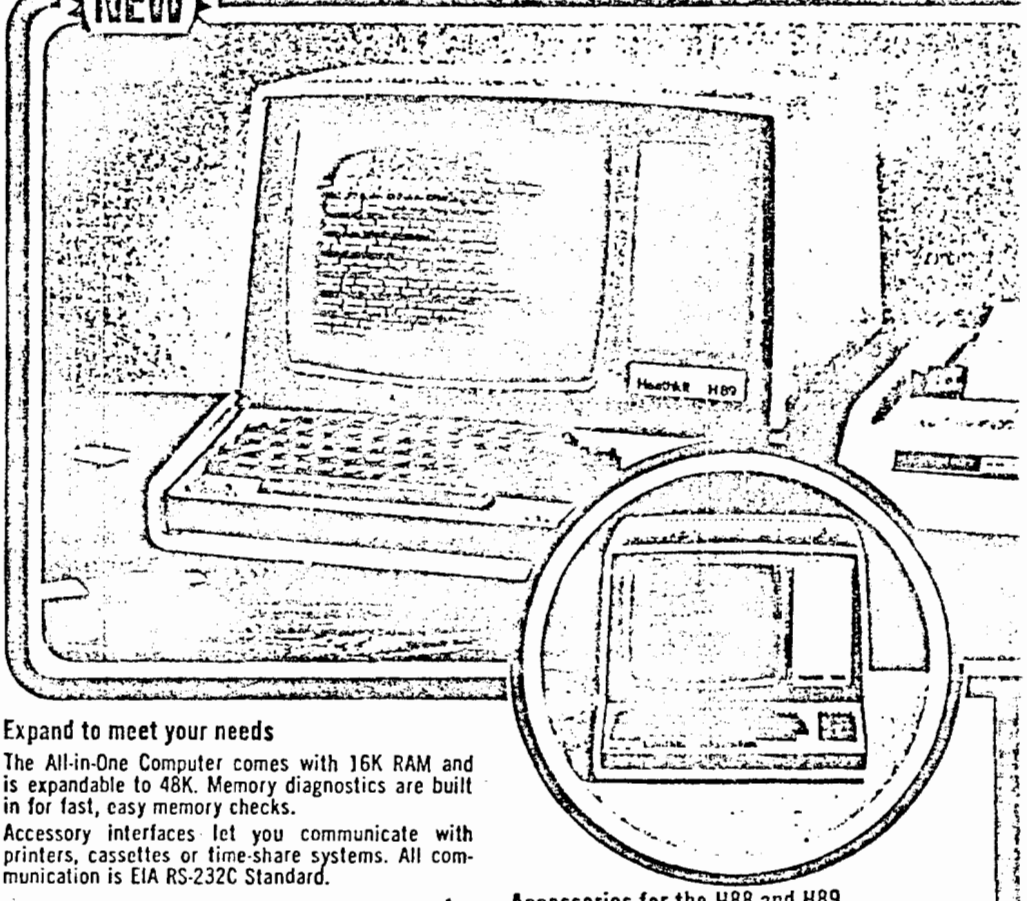
12-inch diagonal cathode ray tube produces clear, easy-to-read characters. The format of 25 lines by 80 characters includes upper and lower case letters, formed by a 5 by 7 dot matrix. Lower case letters with descenders use a 5 by 9 dot matrix.

Built-in Floppy Disk System

The floppy system makes this a true All-in-One Computer and gives you limitless storage capacity for programs and data. Each 5¼-inch diskette contains 102K bytes of storage area, enough to hold entire files. The WANGCO 82 single-drive system gives you high-speed access to any piece of information. Programs can be loaded in seconds from the keyboard. Data can be accessed and updated instantly.

SEE THEM NOW AT YOUR HEATHKIT ELECTRONIC CENTER

NEW



Expand to meet your needs

The All-in-One Computer comes with 16K RAM and is expandable to 48K. Memory diagnostics are built in for fast, easy memory checks.

Accessory interfaces let you communicate with printers, cassettes or time-share systems. All communication is EIA RS-232C Standard.

H89 All-in-One Computer with floppy disk system. Includes audio cassette interface (H88-5). Kit H89, Shpg. wt. 86 lbs. 1650.00

WH89 All-in-One Computer, factory assembled and tested version of above. Does not include audio cassette interface. 2295.00

H88 All-in-One Computer, without floppy disk system. Includes audio cassette interface (H88-5). Kit H88, Shpg. wt. 59 lbs. 1250.00

Accessories for the H88 and H89

H88-2 16K Memory Chip Set. Two sets bring the system up to full 48K RAM capacity (one included with H88). Shpg. wt. 1 lb. 150.00

H88-3 Two-port Serial I/O Interfaces with any serial peripheral. Shpg. wt. 2 lbs. 85.00

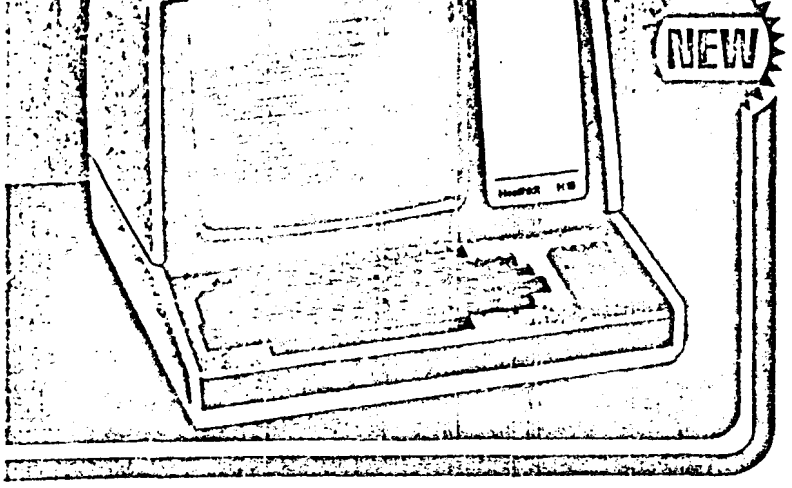
H88-4 Floppy Disk System with drive and interface for H88. Shpg. wt. 22 lbs. 490.00

H88-5 Audio Cassette Interface. Included with H88/H89 Shpg. wt. 2 lbs. 95.00

ECP-3801 Cassette Recorder/Player. Assembled 60.00

H89-17 Systems Software for All-In-One Floppy Disk. For complete description, see H8-17 on page 31. Shpg. wt. 14 lbs. 100.00

H88-18 Cassette Systems Software for the All-In-One Computer includes Extended Benton Harbor BASIC, Assembly Language (HASL-8), Text Editor (TED-8), and Console Debugger (BUG-8). Shpg. wt. 13 lbs. 20.00



New Heathkit H19 Microprocessor-based "Smart" Video Terminal

$695.00 Kit

- Z80 microprocessor-based for fast, efficient data handling
- Full professional keyboard in familiar typewriter format
- Extremely wide bandwidth monitor for easy-to-read images
- Complete ASCII set with upper and lower case characters

The H19 Video Terminal is a top-of-the-line general-purpose peripheral designed for use with the Heathkit H8 and H11A computers or with any EIA RS-232C Standard interface. Its powerful Z80 microprocessor makes it ideal for a variety of high-speed data handling tasks calling for a reliable, compact desktop CRT terminal. It effectively combines ease and convenience of operation with top quality components, modern styling and Heath engineering.

Separate numeric keypad

The familiar typewriter format enables you to start right in programming from the heavy duty keyboard. The terminal's 32 separate functions can be controlled from keyboard or computer. A special 12-key numeric pad in calculator format lets you make fast, easy entry of arithmetic programs.

Eight separate user-definable function keys

Baud rates of up to 19,200 are keyboard selectable for easy changes. Eight user-definable keys let you program your own special functions. The H19 prints the entire ASCII character set, including upper and lower case letters. The print format is 25 lines by 80 characters. Addressable blinking cursor lets you make corrections or edit anywhere on the screen. Reverse video lets you emphasize any portion of the screen by reversing white on black.

Bright, clear readout

The big 12" diagonal CRT has outstanding resolution for a bright, clear readout. The terminal also displays 33 different graphic characters that can be arranged for a variety of graphic displays and effects.

Quiet, fan-free operation

Compact structural foam cabinet withstands the rigors of daily use. A removable top gives you quick access to circuitry for easy servicing. Convection cooled power supply assures quiet, fan-free operation.

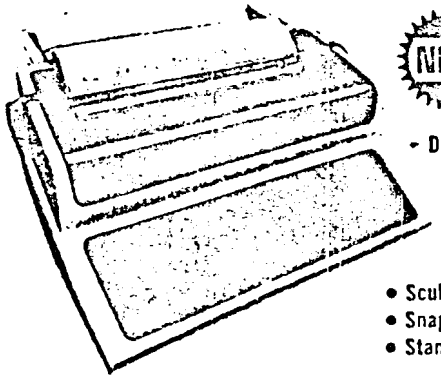
The combination of sophisticated functions, quality design and price make the new H19 the ideal choice for hobbyist or business owner.

Kit H19, Shpg. wt. 54 lbs. 695.00

Factory Assembled and Tested Version of above.
WH19, Shpg. wt. 40 lbs. 995.00

H19 SPECIFICATIONS: CRT: 12" Diagonal, P4 phosphor. Display Size: 6½" high x 8½" wide. Character Size: 0.2" high x 0.1" wide (approx.). Character Set: 128 characters (95 ASCII and 33 graphic). Character Type: 5x7 dot matrix (upper case), 5x9 dot matrix (lower case with descenders). Keyboard: 80 keys (60 alphanumeric, 12 function) plus a 12-key numeric pad. Cursor: Blinking, non-destructive underline. Cursor Controls: Up, down, left, right, home, CR, LF and tab. Cursor Addressing: relative and direct. Tab: standard 8-column tab. Refresh Rate: 60 Hz. Erase Functions: erase page, erase to end of line, erase to end of page. Scroll: auto or line/page freeze. Bell: audible alarm on receipt of control G. Video: normal and reverse using an escape sequence. Interface: EIA RS-232C at 110 to 19,200 baud. Communications Mode: full or half duplex. Parity: even, odd, stick or none. Operating Temperature: 0-40°C ambient. Power Requirements: 105-135 or 200-270 VAC, 50/60 Hz, 45 watts. Dimensions: 13" H x 17" W x 20" D. Net Weight: 45 lbs.

LA34 DEC Writer Desktop Computer Teleprinter



- Designed for convenience and reliability of operation

$1295.00

- Sculptured keyboard
- Snap-in cartridge ribbon
- Standard platen paper advance

The convenient desktop design of the LA34 DEC Writer IV makes it the ideal teleprinter for virtually all office applications. This small, lightweight terminal is designed throughout for simplicity and convenience of operation. The LA34 prints the full 128 character ASCII set with switch selectable 110 and 300 baud rates. It offers true 30 cps print speed, adjustable line spacing, and clear printing through a 9 x 7 dot matrix head. A major feature is the variable character size of the LA34. Character width can be adjusted from a standard 10 characters per inch to 16½ characters per inch. And because the LA34 is designed like a standard typewriter, the operator can easily change space, tab, margin and baud rate settings. Other features include standard sculptured keyboard, cartridge ribbon change, automatic line feed and quiet operation. Comes complete with EIA RS232C standard interface. 7" H x 22" W x 15½" D. For 120 VAC, 60 Hz.

WH34 DEC Writer IV, Fully Assembled and Tested.
Shpg. wt. 30 lbs. 1295.00

CAT Acoustic Modem

Cat Modem by Novation lets your computer talk to other computers over standard telephone lines. Also communicates with any Bell 103 compatible modem. Designed especially for small computers, the Cat Modem lets business people work at home; lets hobbyists communicate and even exchange programs.

WH-13, Fully assembled and tested, Shpg. wt. 3 lbs. 195.00

16K Word Memory Module. Provides 16K dynamic MOS random access memory. Fully assembled and tested. Max. memory capacity of H11A is 30K.
WHA-11-16, Fully assembled and tested, Shpg. wt. 2 lbs. 480.00

32K Word Memory Module. Identical to 16K memory above, but contains an additional 16K of memory. Fully assembled and tested. Max. memory capacity of H11A is 30K.
WHA-11-32, Fully assembled and tested, Shpg. wt. 2 lbs. 995.00

Heathkit Electronic Center
165 Worcester Avenue
Wellesley, MA 02181
Phone: (617) 237-1510
Route: 9 at Jct. 128

For the loca
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Retail price
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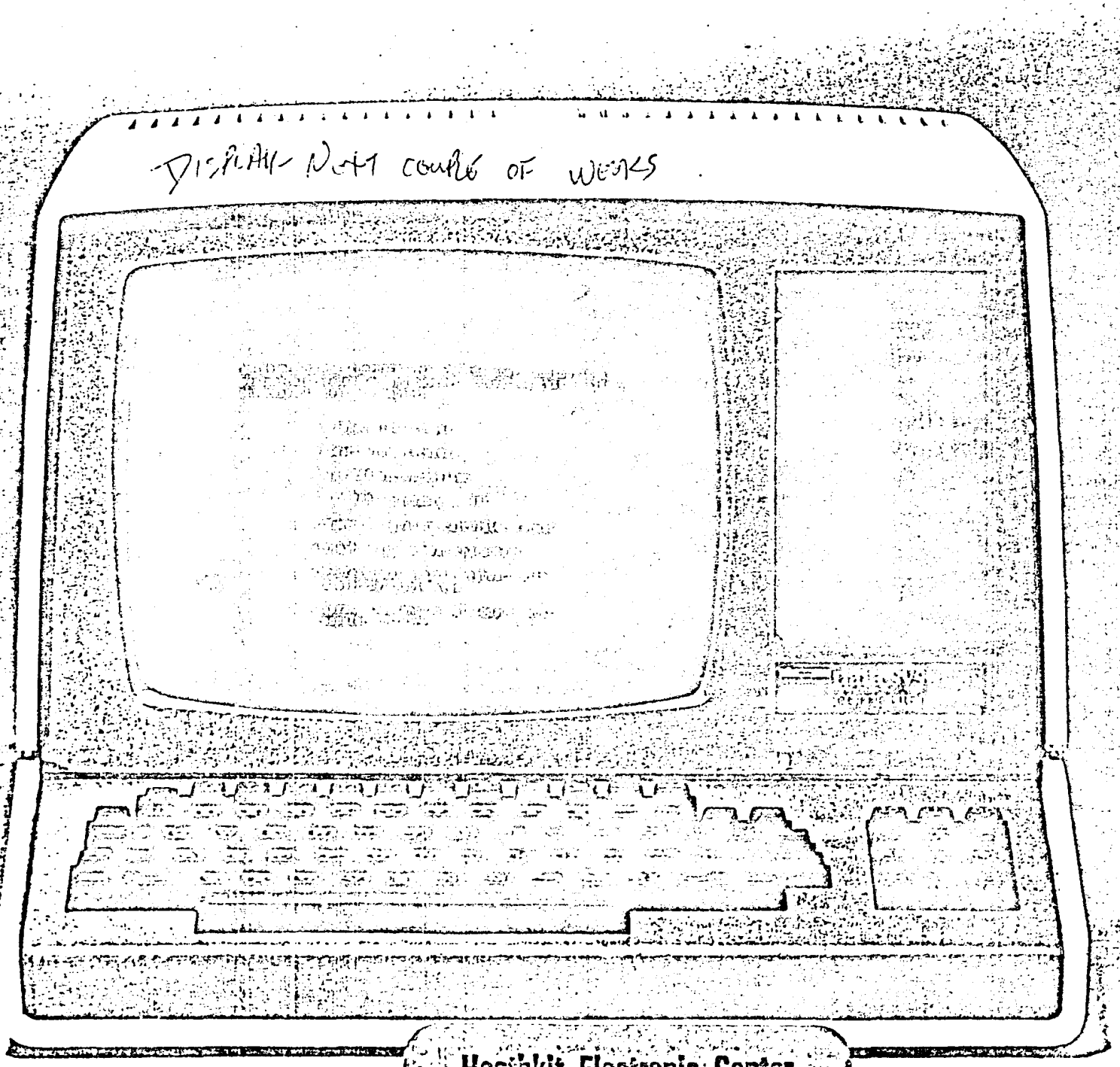
Prices and s
Schlumberger
or pictorial errors.

wh89 all-in-one computer

featuring built-in floppy and smart video terminal



wh89 all-in-one computer

The All-In-One Computer brings you all the power and built-in peripherals needed for any business computing task — all in one compact, desk-top cabinet. The All-In-One Computer can take over many of the tasks now being done by your clerical staff. Its disk storage system can reduce whole filing cabinets to convenient 5¼-inch disks. It's easy to program, easy to operate and it can save you money in many ways.

The smart video terminal has its own Z80 microprocessor. It never shares processor power with the computer, as do most desk-top computers. That makes this terminal capable of a multitude of high-speed functions.

The heavy-duty electronic keyboard is in familiar typewriter format to make operation easier. All terminal functions can be controlled by keyboard or software.

The numeric keypad, in calculator format, permits fast, easy entry of arithmetic data. Shifted functions give you direct cursor positioning for insertion and deletion of lines and characters.

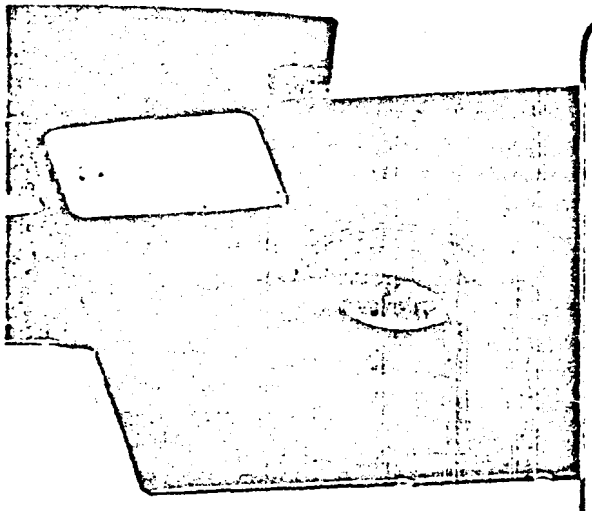
The 12-inch CRT produces clear, easy-to-read characters. 25 lines by 80 characters include upper and lower case letters.

Floppy disk storage makes this a true All-In-One Computer and gives you limitless storage capacity for programs and data. Each 5¼-inch diskette has more than 102K bytes of storage area, enough to hold entire files. Programs can be loaded in seconds from the keyboard. Data can be accessed and updated instantly.

The All-In-One Computer comes with 16K RAM and is expandable to 48K. Memory diagnostics are built in for fast, easy memory checks.

Accessory interfaces let you communicate with printers or other serial peripherals systems. All communication is EIA RS-232 Standard.

The All-In-One Computer speaks the language of today's most popular software. It runs programs written in MICROSOFT™ BASIC and ASSEMBLER Languages. That includes scores of practical programs for business and education.



accessories

16K Memory Chip Set lets you expand RAM. Two additional chip sets bring the Computer to full capacity of 48K. **Order No. H88-2.**

Two-port Serial I/O lets you communicate with H-14 Line Printer or any serial peripheral, or time-share systems via MODEM. **Order No. H88-3.**

Operating Systems Software includes extended Benton Harbor BASIC, 2-pass absolute assembler, text editor to prepare source code for BASIC and other languages, console debugger for easy debugging, and a full set of disk utility programs for convenient file manipulation. **Order No. H8-17.**

Microsoft BASIC includes IF–THEN – ELSE control structure for more highly-structured programming. Features powerful edit and file management facilities, string processing functions, automatic line numbering and renumbering, and much more. **Order No. H8-21.**

Word Processing, when used with a letter quality printer, allows you to enter, edit, store, and print information. Ideal for letters, reports, or for storing and editing copy. **Order No. H8-40.**

specifications

CPU and memory:

Processor:	Z80.
Clock:	2.048 MHz.
Memory:	16K bytes RAM (expandable to 48K.) 8K for systems ROM and RAM. 8K reserved.

display:

CRT:	12" diagonal, P4 phosphor.
Display Format:	25 lines of 80 characters.
Display Size:	6.5" high x 8.5" wide.
Character Size:	0.2" high x 0.1" wide (approximate).
Character Type:	5 x 7 dot matrix (upper case); 5 x 9 dot matrix (lower case with descenders).
Keyboard:	72 keys (60 alphanumeric, 12 function control) plus a 12-key numeric pad.
Cursor:	Blinking, nondestructive underline.
Cursor Controls:	Up, down, left, right, home, CR, LF, back space, and tab, from keyboard or computer.
Cursor Addressing:	Relative and direct.
Tab:	Standard 8-column tab.
Refresh Rate:	60 Hz at 60 Hz/50 Hz at 50 Hz line frequency.
Edit Functions:	Insert and delete character or line.
Erase Functions:	Erase page, erase to end of line, and erase to end of page.
Bell:	Audible alarm on receipt of ASCII BEL.
Video:	Normal and reverse by character.

general:

Power Requirements:	120/240 volts @ 50/60 Hz at 90 watts max.
Size:	13" high x 17" wide x 20" deep.
Weight:	50 lbs.
Operating Temperature:	10° to 35° Celsius.
Storage Temperature:	0° to 35° Celsius.

DEC® USERS: MICROBOL® IS HERE!

MICROBOL was developed by the same software innovator who designed and implemented the BLIS/COBOL® operating system for NOVA® class minicomputers. MICROBOL makes business application development easier than ever for PDT-11/150, LSI-11 and PDP-11 class minicomputers.

MICROBOL represents a dramatic departure from conventional programming methods, and brings application development within reach of end users.

MICROBOL takes full advantage of DEC's new VT-100 CRT, and uses the PDT-151 dual floppy disk with maximum efficiency.

If you have struggled with other programming languages and complicated operating systems, you are bound to appreciate the ease and simplicity of MICROBOL. You will be able to achieve fast results in developing and modifying business applications, without lengthy compilation delays.

Although MICROBOL offers unprecedented simplicity, it is also a powerful business operating system, compatible with LSI-11 and PDP-11 processors when used in conjunction with the VT-100 or equivalent CRT.

MICROBOL is self contained, incorporating its own multi-user operating system and language processor. The single user version requires only 32KB, half of which is available as user program space. Since MICROBOL is memory resident, requiring no overlays, all disk space is available for data and for application program segments.

MICROBOL even permits the programmer to construct his own higher level commands and define his own vocabulary. Many MICROBOL commands perform functions that require laborious program sequences in other languages.

For example: The 'ACCEPT' Command permits full text editing and scrolling within memory pages; the 'PROMPT' Command permits sophisticated screen formatting and data entry, under control of easy to change PROMPT Tables; the 'FORMAT' Command accomplishes complex data movement, under control of easy to change FORMAT Tables. These tables, as well as the procedure portion of MICROBOL, can be altered literally within seconds.

MICROBOL combines, as integral parts of its dedicated operating system, the facilities for data entry, word processing (supports the Spinwriter ™); and business application development and production.

Applications written on request!

MICROBOL, INC. • 711 E. Semoran Blvd., Suite 118
Altamonte Springs, FL 32701 • 305-834-0408

NOV 1 1979

79WR31K-313 11/23/EMS

| d | i | g | i | t | a | l |

INTEROFFICE MEMO

TO: Gordon Bell

CC: Bill Demmer
Jim Marshall
Nat Parke

DATE: 30 October 1979
FROM: Wayne Rosing
DEPT: D&MS Advanced Dev.
EXT: 247-2322
LOC/MAIL STOP: TW/B02

SUBJ: SUTC Prices

Estimated SUTC subassembly component transfer costs are (FY82):

1.	256KB NEBULA/Box/PS	$2.4K
2.	256KB ECC Memory	.6K
3.	20MB Fixed Disk	1.1K
4.	10MB 3M Tape Cart.	.6K
5.	Mass Storage Control	.4K
6.	NI Port	.4K
7.	1024x768 B/W Monitor	.4K
8.	512x768 Color Monitor	1.0K (?)
9.	Bit Map/Video Generator/ Color Map/Display Control	1.1K
10.	Extra Bit Plane	.7K
11.	Keyboard	.1K
12.	Mouse	.1K
13.	Cabinet, BA&T	.75K

A basic black and white 1024x768 3 level gray scale vertical (full page) SUTC in a workstation similar to the word processor, table, NI, and disk, but no tape or extra memory has a cost of:

Simple B/W System $6.75K Xfer cost

Add to that a second plane for 15 level gray scale:

Full B/W System $7.35K Xfer cost

Instead, use a 512 line x 768 wide color system (8 logical planes, 4096 possible colors) and the cost is:

Full Color System $8.15 Xfer cost

The options are:

Additional Memory	$.6K/.25MB
3M Tape Cartridge	.6K
20MB Disk Expansions	1.1K

On the Single system the percentages are:

CPU, Memory, IO	42%
Mass Storage	22%
Packaging	11%
Monitor, Video, Keyboard	25%
	100%

There are many reasons why multiple planes of memory are required, even in the B/W system, especially for handling split screen smooth scrolling and for multi-zone "overlap" of documents on the screen.

Nat Parke and I are aware that the above prices are high--but we need to begin somewhere. When microVAX is here and the monitors are in mass production, this kind of functionality will be a lot cheaper. In the meantime, we can use SUTC internally and sell it externally for CAD applications and areas who need it (CMU-SPICE, for example.)

We are 105 percent committed to work within the framework of REGIS/GIGI to evolve a standard architecture that will be compatible and to ensure that the design center of the high end graphics architecture is migratable to commodity products as technology allows.

draft

1980's SECRETARY
by Mary Jane Forbes

Since the word processor came into the office at DEC, there have been subtle changes in our profession.

Job descriptions will begin to reflect these changes. Each step in the the secretarial career path will stand out more clearly--starting with the ability to create and edit on a machine, to using the machine to organize the office (i.e. filing and retrieval), to integrating all aspects of the office and being the nerve center for all departmental information and communcations.

This means the 1980's secretary, to climb that career ladder, must be inquisitive, a self-starter, (not content to merely process what is given, but to find the best way), willing to help train new secretaries for the 1980's--they can't get this in schools yet--so there will be well qualified candidates to fill your job as you move up.

Word Processing has removed many of the mundane jobs from our profession--xeroxing, collating, stapling, addressing. They give us needed time to get the work out without the frazzled syndrome plus we can do it more creatively. We have to get our priorities straight. Naturally our boss comes first--but if you catch yourself saying, "I would like to do that but I don't have time", you may be in the frazzled trap. The truth is YOU CAN'T AFFORD NOT TO TAKE THE TIME OR MAKE THE TIME. Your work will always be there, the chance to learn may not. There are plenty of career-conscience secretaries who will pass you by and get that new job, because they know how to set their priorities and are willing to put in a few extra hours to make things better/easier in the long run.

The 1980's secretary must read. WPS and EMS are HERE! They are tools limited only by OUR knowledge and understanding of them. The secretary learning how to operate a word processor will only retain about a quarter of the material in the manual. After you are comfortable with the machine, go back and read the manual again--you will be amazed at what it has to offer. Six months after the first reading, go thru it again and again the next year.

Talk with your peers about how they do things. Discuss ways you can work together--standardize your procedures. If you all file the same way, retrieval becomes a snap. Archival records are automatically in systematic order across the group.

Questions to ask yourself: with EMS, what routine should be followed for filing what messages should be kept on EMS file, what should be transferred to WP? If you create on WPS and send EMS at what point do you add the EMS header? When is it not cost effective to send EMS, i.e. cheaper to Xerox a 4 page document than recipients printing it out? With WPS, if you aren't automatically getting page numbers (\p); or not using a 2-letter code for your memo header (i.e.<<mh>>); not using list processing to produce labels, then it is time to REREAD the manual.

We need a place for an exchange of ideas on how to handle these new machines in our work environment. If you come up with a routine that works well for you, please send it to "Secretarial Views, 1980's

Secretary", PK2-1/B11; or via EMS to "1980's SECRETARY: @CORE". We can then publish these ideas plus start an office procedure manual that might one day be used as a selling aid for DEC's Word Processing Product Line.

We now have a tool to stretch our minds and imagination. Are you ready for the challenge, the excitement of our 1980's office? Are you keeping pace?

EMS TIPS--TIME SAVERS

- Request distribution lists be set up for staff members, committee members.
- Type in last name first--system will fill in the rest, or give a choice, if more than one user with same last name.
- Shift 6 will get you out of memo header routine, returning you to COMMAND>
- Use I[INQUIRY] feature when you need a badge #, CC#, to complete a form.
- When A[NSWERING] a message, do not use automatic CC to all prior recipients unless they have a NEED TO KNOW. This causes junk mail.
- EMS has pre-set tabs every 8 spaces if you need tabs.

Reference Material

1) RETRIEVAL, AN OFFICE PROCEDURE FOR A SECRETARY USING A DEC WORD PROCESSING SYSTEM Forbes, ML12-1/A51
2) EMS INSTRUCTIONS--COMMAND MODE ONLY--this is intended as an aid until the manual is issued. Forbes, ML12-1/A51
3) SELF-PACED OPERATOR TRAINING MANUAL, Ordering Processing, Bedford, Mass. (249-2276) $100 each
4) Latest version of WPS software: Steve Woodward, 223-7564. Give him your system configuration, i.e. WS78, WS200. He will give you the order number for SDC (Carl French, 223-2808). Ask Steve for the SPD for the version you want (Software Product Document--explains new features).

OCT 26 1979

digital

INTEROFFICE MEMORANDUM

TO: Gordon Bell

DATE: 25 OCT 79
FROM: Tom Vlach Tom
DEPT: D&MS
EXT: 264-5190
LOC/MAIL STOP: MK1-1/N34

SUBJECT: ELECTRONIC MAIL

I read your memo of 18 October, and I agree that EMS is the key entry vehicle into office automation. It seems to be the missing link that allows data processing and office processing to co-exist in harmony in a distributed environment.

I have attached for your review a strategy document I prepared on Electronic Mail. I would appreciate your feedback.

If electronic mail had been fully implemented in DIGITAL, including word processing, I could have sent you this document automatically.

/eb

DISTRIBUTION:

Don Alusic	MK1-1/N34
Rich Andreoli	MR2-4/F19
John Buckley	MK1-2/K36
Peter Christy	ML12-3/A62
Steve Coleman	ML12-1/F41
Ralph Dement	PK1/A10
Dan Deufel	MR1-2/H22
Paul Dickson	ML3-2/E82
Bob Dockser	MK1-2/N38
Frank Duffy	PK1/F60
Dick Easton	MK1-1/E25
Raff Ellis	MR2-4/M79
Bob Erickson	PK1/F60
Sam Fuller	TW A08
Dell Glover	MR2-4/M51
Earl Haight	MK1-1/E25
Joanne Hartley	MK1-2/K34
Peter Janca	MK1-1/D29
Jackie Kahle	MK1-2/K36
Rich Kalin	MK1-2/102
Len Kawell	TW/D08
Jim Kelley	MK1-2/H32
Ken King	ML3-2/E41
Ran Khare	MK1-1/D29
Alan Kotok	ML3-5/H33
Dana LaJoie	MR1-1/M85
Si Lyle	MR1-1/M42
Ward MacKenzie	PK3-1/A60
Bob Maguire	MK1-1/D29
Bob McGeary	MK1-1/J14
Steve Meidell	PK3-1/M34
Jerry Melnick	PK1/F60
Clair Messier	PK1/F60
Steve Mikulski	ML5-2/E50
Helen Nayar	MR1-1/M85
Dave Oran	MR1-2/H22
Rich Pietravalle	MK1-2/L35
Peter Schay	ML5-2/M17
Joel Schwartz	MR2-4/M51
Dick Strauss	ML12-2/A16
Jerry Todd	PK3-1/S52
Dave Tolman	ML12-3/A62
Bob Travis	MK1-1/J14
Harvey Weiss	MK1-2/K36
Jim Willis	MK1-2/H32
Jeff Wilson	ML12-2/E71
Jerry Witmore	PK3-1/M40
Steve Woodward	ML1-5/M83
Carroll Wright	ML5-5/E92

d i g i t a l

INTEROFFICE MEMORANDUM

TO: DISTRIBUTION

DATE: 10 OCT 1979
FROM: Tom Vlach Tom
DEPT: D&MS
EXT: 264-5190
LOC/Mail: MK1-1/N34

SUBJ: ELECTRONIC MAIL MARKET REQUIREMENTS AND STRATEGIES

Please review and comment on the attached document. The material contained herein sets the stage for a product requirements document which in turn leads to specifications and, finally, a product. Your interest and feedback are most appreciated.

ELECTRONIC MAIL

MARKET REQUIREMENTS AND STRATEGIES

Thomas L. Vlach
Distributed &
Mid-range Systems
10 OCT 79

COMPANY CONFIDENTIAL

TABLE OF CONTENTS

1.Ø SUMMARY

The purpose of this document is to define the market requirements for DIGITAL's electronic mail system called DECmail. DECmail will be marketed primarily to FORTUNE 5ØØ companies. These organizations are actively investigating office of the future concepts, and monies are currently being allocated and spent to implement pilot programs. Other markets include educational institutions and OEM'S.

The announcement of DECmail will be an important signal to the user community that DIGITAL intends to play an active role in the evolution of the office of the future. DECmail affords DIGITAL a low cost/low risk opportunity to enter this emerging market.

It is recommended that DECmail be promoted as an office automation application that operates in a distributed processing environment. The product then captures the essence of two major themes for the 8Ø's, office automation and distributed processing.

DECmail should be sold to DIGITAL's traditional sophisticated customers who can provide the necessary support to insure the success of the program. It is essential that DECmail be capable of being sold and supported with existing pre-and-post sales resources. In particular, grandiose "office of the future" sales situations involving naive customers that require high levels of DIGITAL support must be avoided.

Even though DECmail will be marketed to sophisticated users, the mail interface should be designed for use by both naive and sophisticated users. The pilot projects that DECmail will be sold into, hopefully, will be managed by sophisticated computer people. The users, however, may well be managers and professionals who have little or no computer expertise.

2.0 MARKET TRENDS

To be successful as a product, DECmail must be positioned so as to fit into the emerging plans of the FORTUNE 500 companies for office automation and distributed processing. These plans are evolving according to the following scenario:

Interactive Computing:

The concept of a CPU with a multiplicity of terminals (both dumb and intelligent) is the key element that will be found throughout the facilities of these customers. The CPU will support both interactive and batch processing. IBM's announcements of the 4300 and 8100 verified this beyond any doubt.

Networking:

These CPU's will interconnect via a private communications network such as DECnet or SNA. This is certainly true within a single facility. The connection of remote facilities could be accommodated via the same architecture or via services such as ACS, TELENET, or SBS. Cost will decide which remote link is used. In any event, the services of ACS or TELENET will be used to link homogeneous networks (DECnet or SNA) to computer services not available within the company (i.e., the multiplicity of data bases that are starting to become available).

Productivity:

The acquisition of office automation equipment will be justified on anticipated productivity improvements. There is a very strong feeling, but little concrete proof, that computer equipment can improve the productivity of office workers (clerical, professional and managerial). Early sales of office automation equipment will be treated as pilot projects whose main purpose is to prove that productivity gains are possible.

Office Environment:

The office environment is a very broad term that includes but also extends far beyond the classical office. The managers and professionals who work on the factory floor, in warehouses, or in laboratories, also have office automation requirements. The computers that now control these environments will also be expected to support electronic mail. It is unlikely that dedicated CPU's will be purchased for electronic mail unless justified by heavy usage.

Flexible/Expandability:

Customers will be looking to purchase systems that are flexible, expandable, and which offer general purpose computing capability. A system that only supports electronic mail has limited market potential. Electronic mail must be able to run concurrently in a multiplicity of system environments including timesharing, transaction processing, real time, and batch. Word processing is an application that will frequently co-exist with and complement electronic mail.

Customers will select office automation vendors on the basis of products that are demonstrably expandable. These customers might purchase a new system or expand an existing one to experiment with electronic mail, expecting other services to become available. These might include:

Calendar Keeping
News announcements
Spelling verification
Expanded filing
Directory services
Desk Calculator
and many more.

A further flexibility requirement is that of a single terminal that can perform all of the office functions, including the connection to foreign systems. The current scenario in which a worker needs multiple terminals for word processing, data processing, and DEC vs. IBM processing, is not an acceptable long term solution.

Integrated Processing:

In the 80's, systems that can support data processing, text/word processing, and electronic mail, will capture the major portion of the market. The applications that are built, such as transaction processing, word processing, and memo handlers, must share a common file system. Information must be able to move freely between these applications, avoiding awkward conversion mechanisms.

Users:

Electronic mail and office automation are products that tap a large user base that has never used computers. To be successful, early systems must be warm and friendly. Complicated command sequences with rigid syntaxes and curt error messages must be avoided. The pyschology of fear and frustration will play an important role in the acceptance or rejection of early systems. Mail systems must be designed with the naive, non-computer user in mind, yet it must also provide optional expanded functionality for the sophisticated user.

3.0 PRODUCT CHARACTERISTICS

Based on the market trends discussed in the previous section, the following characteristics are deemed to be critical to the success of DECmail.

Reliability:

This means system reliability. The system must be available to the users and must perform in a consistent manner. Severe response times or unexplained system crashes will convince dubious users that computers are unreliable.

Ease of Use:

It is hard to say enough about this subject. Since many of the initial sales of DECmail will be in pilot office automation projects, user acceptance is critical. If the users reject the system because it is too hard to use, the project will fail.

Supportable/Maintainable:

Pre and post sales support plans must be developed that are sensitive to the user environment. Selling cycles into existing DEC accounts could be short, while new accounts will probably have long cycles. Documentation and support tools must be developed to meet the needs of naive users.

Multiple Functions:

Customers will be looking for as much functionality as possible. A mail system that also supports a calendar keeper and a document handler would be very attractive. An alternative could be a mail system with integrated word processing capability.

Expandability:

The marketing message must stress expandability in several dimensions. The system can be expanded via expanding the network or adding more users or new features. The design of DECmail as a layer product with distinct electronic post office and user mail functionality is consistent with the goals of expandability.

Hardware Requirements:

Ultimately, DECmail should be offered on all of DIGITAL's major hardware systems; 10's, 20's, 11's, and VAX'. Given funding constraints and the practicalities of getting a product to market in a reasonable time period, it is likely that only 11's and VAX' will be supported. Terminal support must be flexible and must include both hard and soft copy devices, including non-DIGITAL equipment such as Teletypes. DECmail will appeal to many customers who own their own terminals, but might purchase a new CPU to experiment with electronic mail. Both dial-in and dedicated lines must be supported.

Software Requirements:

The following is a list of key software requirements:

- Layered product under DIGITAL's unmodified operating systems.
- No restrictions on other co-resident applications.
- RMS file support.
- DECnet interconnection.
- Directory support.
- Simple editor for naive users.
- Access to other editors (TECO, RUNOFF, KED) for sophisticated users.
- Memo reading, writing, sending and filing routines.
- Word processing support using the DX protocol.

By building DECmail as a layered product, the flexibility exists to also package dedicated mail nodes in either a stand-alone or distributed environment.

4.0 PRODUCT POSITIONING/PROMOTION

Decmail offers two major marketing themes. One theme is office automation. Electronic mail is a key requirement in office automation. DIGITAL can signal its intent in this area by promoting electronic mail. The other theme is distributed processing. DECmail, as it is currently conceived, is an important tool that can be used to implement applications in a distributed processing environment. The electronic post office concept residing in each node of a DECnet system gives users a powerful tool to implement applications. Indeed the electronic mail (user mail) system is one such application. Users will have access to the electronic post office to implement others.

5.0 PRICING

There are two views that can be taken on pricing. If DECmail is sold primarily as add-on software to an existing DECnet system, a license fee of $5K or less (per node) is probably all the market will bear. WANG is selling their mail system for $2K per node. If DECmail is heavily promoted as an office automation product and forms the basis of a new DECnet sale, a much higher price can probably be commanded. An application product like DECmail could easily command a $20K fee. CCA charges $40K for COMET. However, by charging a $20K license fee, users will expect high levels of support. The $5K license fee is consistent with our current support program, and is also consistent with most of the software license fees charged by DIGITAL.

6.0 PRODUCT LINE SELLING

DECmail will be actively sold in the Commercial, Technical, and Word Processing Product Lines. Although the FORTUNE 500 companies are expected to account for the majority of sales, many other opportunities exist. Both technical and commercial OEM's could use DECmail to help sell into new accounts. Educational institutions are heavy users of interactive computing and, given their experiences with ARPANET mail, would be eager for DECmail.

7.Ø PRODUCT EVOLUTION

As an office automation product, DECmail will be successful only if new functionality is continually being added to the product. The following is a non-exclusive list of features being discussed in the marketplace. Some might be included at FCS while others will be included in future releases.

Calendar Keeping
News Announcements
Spelling Verification
Expanded filing
Directory services
Desk Calculator
TWX/TELEX Support
ACS Support
SNA Support
High availability configuration
Expanded terminal support
Reminder system
Sorting/merging
Graphics support
Audio support

APPENDIX

ELECTRONIC MAIL - DIGITAL's DEFINITION

Electronic mail is a very popular term in the computer world. It is generally understood to be a mechanism whereby information (data) is electronically transmitted between two or more users. In this broad context, a wide variety of technologies, such as TWX/TELEX, facsimile, and message switching, fall under the general heading of electronic mail.

More recently, electronic mail is receiving wide attention, being viewed as a terminal oriented system used by managers, professionals, and clerical workers. A CRT or hard copy terminal is used to generate and send memos and documents to other users on the system. In some cases, all users are connected to a single computer, while in other cases, multiple computers exist in a network. In this context, electronic mail is viewed as a partial replacement for both inter-office mail and telephones. The goal of such a system is to improve office productivity.

Electronic mail, as conceived within DIGITAL, supports two major themes; distributed processing and office automation. The electronic post office portion of DECmail is a tool that can be used to build applications in a distributed processing environment. The following is a partial list of the applications that could be implemented once the post office is in place:

- Memo handlers
- File Transfer
- Inquiry/Response Transactions
- Facsimile transfer
- Store and forward voice transmission

This portion of DECmail is a tool in the classical sense. The user must add additional software to form a usable product.

The user mail (memo handler) portion of DECmail is an end-user application....a turnkey system for office automation. Users can approach terminals and, without any additional programming, begin using the system to create, send, read, and file memos.

Thus:

DECmail = ELECTRONIC POST OFFICE (distributed processing tool)
+ USER MAIL SYSTEM (office automation application)

/eb

Unix Closeness ⇒ Economy + Sharing

Small firm ≠ small org. in a large firm

Talk
- Defs.
- CMU/MIT view of pers.
- Is it different than interactive computing?
- VAX-based & why.
- The hardware + it's (evolution)
- Goals & Constraints
- Data-types
- QBE
- what it would do.
- IBM results.
- Research approach.
- Living on the machine.
- Getting an archetype for proto. for each "feature"

why no surprises? / without increase / with flow?

Which Applic
What is to be put on a C
How (t)
Why (t)

Steve Ward
high res. graph
high bw interact
simple sys. semantics
powerful interrupt scheme

Goals:
- Self-Documenting by menu driven vs. help
- Consistency calls (Multics/Grimes)

Lots of macro processors (facility for employing one set of symbols with another)

to check out research (Test fraud disk system)

News, bulletin, poster, tickler, scratch

Take ... page ... Tour

System like BBN built for Database + tables + graphs for drug. (Input)

Plans (Has the directory and access calls, arch

Knows if a fact is Plans

Total Copy Center
Does, Bcst, Dist

Memo vs Mail vs Billboard
Folder for > 5 users s.t. put in system + non-subscribers get it direct

Expense forms

Remember (Tickler

Def.
Office Automation
Personal C.
C in the home
Small, Business - Cognetics
Small-Business

Profession-Based System.
Engineers

Process 5-1-11a 6-7:30 -1½
5
1:30-4:30 - 3
1

PROFESSION-BASED SYSTEM - Gordon Bell MAIL ANALYSIS
October 1 thru October 11 (9 working days)

DOC TYPE		DIST #	# PAGES EACH DOC	TOTAL # PAGES	COULD BE EMS?	SENT VIA EMS	OFF-SITE
SUMMARY		# docs to read					
OOD/STAFF	28	336	72	835	16	3	3
OC	19	226	162	1,938	5	2	1
MKT CO	5	96	72	1,068	0	1	1
EMS/ARPA	12	100	12	100	0	12	0
EBOD	2	18	3	23	1 Both	1	1
FINANCE	3	237	94	11,786	1	0	0
SIGNATURE	4	4	4	4	-	-	-
MUSEUM	6	7	11	14	2	1	4
DP		3	5	15	0 even cold.	0	1
FROM OUTSIDE	11	11	44	44	0	0	11
MEMOS GEN	10	382	48	726	6	0	4
	6	25	11	54	4	0	1
TECH MEMOS	23	415	65	2,437	11	5	14
RE CUSTOMER	3	61	74	3,966	1	0	1
F/U	3	3	3	3	2	0	1
PERSONNEL	19	1,266	34	1,483	12	3	4
FYI	22	684	51	2,364	11	6	4
TECH REPORTS	19	432	336	6,467	3	0	8
DEC JUNK MAIL	11	8,766	454	482,926	0	0	2
GRAND TOTAL	206	13,072	1,555	516,252	75	34	61

NOTE:

1. Outside junk mail:

Newspapers	7	Magazines	6
Technical Bulletins	23	Other	14

2. Decision to "Could have been sent EMS" based on size and type of document.

GB0005/2
10/12/79

DOC TYPE		DIST #	# PAGES EACH DOC	TOTAL # PAGES	COULD BE EMS?	SENT VIA EMS	OFF-SITE
OOD:							
Agenda	1	14	2	28	0	1	0
KO	1	3	4	12	1	0	0
Staff	1	14	2	28	1	0	0
	1	14	9	126	0	0	0
	1	14	1	14	1	0	0
	1	14	4	56	0	0	0
	1	3	3	9	0	0	0
	1	5	1	5	1		1
	1	14	10	140	0		0
	1	14	3	42	0		0
	1	4	1	4	1		0
	1	6	1	6	1		1
	1	14	3	42	0		0
	1	20	4	80	0		0
	1	6	1	6	1		0
	1	26	1	26	1		0
	1	6	2	12	1		0
	1	14	1	14	1		1
	1	4	7	28	0		0
	1	14	3	42	0		0
	1	4	1	4	1		0
	1	2	2	4	1		0
	1	21	1	21	1		0
	1	14	1	14	0	1	0
	1	5	1	5	0	1	0
	1	12	1	12	1		0
	1	18	1	18	1		0
	1	37	1	37	1		0
	28	336	72	835	16	3	3
EBOD							
General	1	13	1	13		1	1
	1	5	2	10	1		0
	2	18	3	23	1	1	1
MARKETING COMMITTEE							
Package	1	12	45	540	0		0
General	1	18	1	18	0	1	1
	1	15	4	60	0		0
	1	44	8	352	0		0
	1	7	14	98	0		0
	5	96	72	1,068	0	1	1
DIGITAL PRESS	1	3	5	15	0		1

DOC TYPE	DIST #	# PAGES EACH DOC	TOTAL # PAGES	COULD BE EMS?	SENT VIA EMS	OFF-SITE
FINANCE						
General	1	44	2	88	1	0
	1	26	26	676	0	0
Yellow Bk.	1	167	66	11,022	0	0
	3	237	94	11,786	1	0	0
SIGNATURE	1	1	1	1	0	0
	1	1	1	1	0	0
	1	1	1	1	0	0
	1	1	1	1	0	0
	4	4	4	4	0	0	0
MUSEUM	1	2	3	6	0	0
	1	1	1	1	0	0
	1	1	4	4	0	1
	1	1	1	1	1	1
	1	1	1	1	1	1
	1	1	1	1	0	1	1
	6	7	11	14	2	1	4
OUTSIDE	1	1	1	1	0	1
	1	1	2	2	0	1
	1	1	1	1	0	1
	1	1	1	1	0	1
	4	4	5	5	0	0	4
OUTSIDE TO BE ANSWERED						
	1	1	1	1	0	1
	1	1	6	6	0	1
	1	1	23	23	0	1
	1	1	3	3	0	1
	1	1	1	1	0	1
	1	1	1	1	0	1
	1	1	4	4	0	1
	7	7	39	39	0	0	7

DOC TYPE	DIST #	# PAGES EACH DOC	TOTAL # PAGES	COULD BE EMS?	SENT VIA EMS	OFF-SITE
MEMOS GENERAL						
General	1	4	1	4	1	0
	1	8	7	56	0	1
(Simulation Center of Competence)	1	107	1	107	1	1
	1	1	18	18	0	1
	1	2	13	26	0	0
	1	5	1	5	1	0
Prod.Announc	1	235	2	470	1	0
	1	4	1	4	1	0
	1	6	1	6	1	1
	1	10	3	30	0	0
	10	382	48	726	6	0	4
MEMOS TO BE ANSWERED						
General	1	4	1	4	1	0
	1	1	2	2	1	0
	1	7	3	21	0	0
Proofs	1	7	3	21	0	0
	1	3	1	3	1	1
	1	3	1	3	1	0
	6	25	11	54	4	0	1
TECHNICAL MEMOS						
	1	40	2	80	1	0
	1	3	2	6	0	1	0
	1	1	1	1	0	0
	1	4	1	4	1	1
	1	8	4	32	0	0
	1	14	1	14	1	1
	1	20	3	60	0	1	1
	1	4	2	8	1	0
	1	1	1	1	1	1
	1	2	2	4	1	0
RSTS/VAX Review	1	78	1	78	1	1
	1	11	5	55	0	1
RM05 Bus.Pl	1	105	15	1575	0	0
	1	34	11	374	0	1
	1	10	3	30	0	1
	1	6	1	6	0	1	0
	1	24	1	24	1	1
	1	17	2	34	1	1
	1	6	1	6	1	1
	1	3	1	3	1	0
	1	12	1	12	0	1	1
	1	3	1	3	0	1	1
	1	9	3	27	0	1
	23	415	65	2,437	11	5	14

DOC TYPE	DIST #	# PAGES EACH DOC	TOTAL # PAGES	COULD BE EMS?	SENT VIA EMS	OFF-SITE
CUSTOMER						
	1	5	1	5	1	1
General	1	1	1	1	0	0
Slippage rep.	1	55	72	3960	0	0
	3	61	74	3966	1	0	1
REPLIES/RETURNED/F/U						
General	1	1	1	1	0	1
	1	1	1	1	1	0
	1	1	1	1	1	0
	3	3	3	3	2	0	1
PERSONNEL						
	1	22	1	22	0	1	1
	1	4	6	24	0		0
	1	8	2	16	1		0
	1	14	1	14	0	1	0
	1	1	1	1	0		0
Org. Annou.	1	306	1	306	1		0
	1	21	1	21	1		0
	1	2	7	14	0		0
Org. Annou.	1	76	1	76	1		0
	1	22	1	22	1		0
	1	34	1	34	1		0
	1	30	1	30	1		0
	1	1	1	1	1		1
	1	100	1	100	1		0
Org. Annou.	1	295	1	295	1		1
US Pop.Rep.	1	59	4	236	0		0
Org. Annou.	1	109	1	109	1		0
Org. Annou.	1	75	1	75	0	1	0
	1	87	1	87	1		1
	19	1266	34	1483	12	3	4
FYI						
	1	27	1	27	0	1	0
	1	27	2	54	0	1	0
	1	29	1	29	0	1	0
Multi-cpu memos of interest	1	189	2	378	1		1
	1	26	1	26	1		0
	1	10	1	10	1		0
	1	6	1	6	1		1
FS Install QC Report	1	147	7	1029	0		0
	1	34	11	374	0		1
	1	1	1	1	1		0
	1	6	1	6	1		0
	1	12	1	12	1		0
	1	2	1	2	1		0
	1	1	3	3	0		0

DOC TYPE		DIST #	# PAGES EACH DOC	TOTAL # PAGES	COULD BE EMS?	SENT VIA EMS	OFF-SITE
FYI Contin.	1	27	1	27	0	1	0
	1	31	1	31	0	1	0
	1	1	1	1	1		0
	1	1	1	1	1		0
	1	27	1	27	0	1	0
	1	14	7	98	0		0
Automation Seminar	1	52	4	208	0		1
	1	14	1	14	1		0
	22	684	51	2364	11	6	4
TECHNICAL REPORTS							
	1	17	2	34	1		1
HW/SW Coor. Matrix	1	70	24	1680	0		1
	1	15	8	120	0		1
	1	11	9	99	0		1
	1	1	48	48	0		0
Eng.Com.	1	52	2	104	1		0
	1	9	3	27	0		0
	1	48	4	192	0		0
	1	6	16	96	0		1
	1	5	12	60	0		1
	1	1	16	16	0		0
Eng.Com.	1	49	2	98	1		0
	1	17	20	340	0		0
	1	42	5	210	0		0
	1	4	6	24	0		1
	1	38	8	304	0		0
	1	1	26	26	0		0
	1	25	91	2275	0		1
	1	21	34	714	0		0
	19	432	336	6467	3	0	8
DIGITAL JUNK MAIL							
	1	23	5	115	0		1
DEC STDS MICROFICHE LIST	1	450	1	450	0		0
	1	1	89	89	0		0
SYS MAN. PL WAIVER	1	69	21	1449	0		0
SALES UPDATE	1	6500	64	416,000	0		0
SOFTWARE NEWS	1	1300	47	61,100	0		0
Software Eng. Montly Rep.	1	20	100	2000	0		0
	1	1	33	33	0		1
CAD Newsletter	1	400	4	1600	0		0
	1	1	45	45	0		0
	1	1	45	45	0		0
	11	8766	454	482,926	0	0	2

DOC TYPE	DIST #	# PAGES EACH DOC	TOTAL # PAGES	COULD BE EMS?	SENT VIA EMS	OFF-SITE
EMS-ARPA						
1	1	1	1	0	1	0
1	1	1	1	0	1	0
1	5	1	5	0	1	0
1	1	1	1	0	1	0
1	11	1	11	0	1	0
1	27	1	27	0	1	0
1	5	1	5	0	1	1
1	7	1	7	0	1	0
1	27	1	27	0	1	0
1	14	1	14	0	1	0
1	1	1	1	0	1	0
1	Subscri.	1		0	1	0
---	---	---	---	---	---	---
12	100	12	100	0	12	0
OC						
1	1	1	1	1		0
1	4	3	12	0		0
1	14	3	42	0		0
1	14	1	14	1		0
1	15	16	240	0		0
1	14	3	12	0		0
1	48	3	144	0		0
1	15	2	30	1		0
1	17	1	17		1	0
1	4	1	4	1		0
1	1	13	13	0		0
1	1	5	5	0		0
1	15	4	60	0		0
1	12	42	504	0		0
1	2	3	6	0		1
1	1	2	2	1		0
1	20	1	20	0	1	0
1	14	19	266	0		0
1	14	39	546	0		0
----	----	----	----	----	----	----
19	226	162	1938	5	2	1

JUNK MAIL

Newspapers - 7
Magazines - 6
Technical Bulletins - 23
Other - 14

MAY 1 1 1982

COMMERCIAL SYSTEMS ENGINEERING

WHO ARE WE?

* HARDWARE/SYSTEMS DEVELOPMENT
* LOCATED IN MERRIMACK
* PART OF SOFTWARE ENGINEERING
* REPORT TO CCEG MANAGER (BOB DALEY)

WHO DO WE WORK FOR (FUNDED BY)?

* PRODUCT LINES	-	72%
* JOHNSON	-	15%
* LACROUTE	-	11%
* AVERY	-	2%

TO EMC

Please find attached a set of slides on Central Comm'l Hardware Engineering. Please advise me whether Harvey Brian come to EMC is worthwhile.

BJ

Brian Fitzgerald
3/1/82

MAY - 6 1982

COMMERCIAL SYSTEMS ENGINEERING

WHAT DO WE DO?

* INTEGRATE PRODUCTS ACROSS DEC BOUNDARIES (TECHNICAL OR ORGANIZATION)
* DEVELOP SYSTEMS FOR COMMERCIAL MARKETS
* DEVELOP OPTIONS FOR COMMERCIAL MARKETS
* GIVE TECHNICAL SUPPORT TO PRODUCT LINES
* PROVIDE DIAGNOSTIC & DRAFTING SERVICES

RECENT EXAMPLES OF OUR WORK:

PRODUCT	SPONSOR
LQP02 & SHEET FEEDER	WORD PROCESSING
VTC	CATS PROGRAM
CUSTOMER INSTALLATION	COEM
DECMAIL INTERCONNECT	OFFICE PROGRAM
SGB (BELGIAN BANK) SYSTEM	CSI
OPTION DIAGNOSTICS	TIG
DECWORD CONFIGURATIONS	OFFICE PROGRAM
TEMPEST PACKAGING DESIGN	GSG
DECMATE HOT LINE	WORD PROCESSING
OFIS CONFIGURATIONS	OFFICE PROGRAM
NI TESTER DIAGNOSTICS	DIST. SYSTEMS

COMMERCIAL SYSTEMS ENGINEERING

Q - WHAT IS SYSTEMS INTEGRATION?

A - COMBINING AND CONNECTING THE RIGHT SET OF COMPONENTS TO PERFORM A USEFUL JOB.
(ALSO - FILL IN THE MISSING PIECES)

Q - WHAT ARE THE COMPONENTS OF A SYSTEM?

A - ALL OF THESE:

HARDWARE COMPONENTS	SOFTWARE COMPONENTS	SERVICE COMPONENTS
KERNAL MACHINE	OPERATING SYSTEM	PRODUCT INFORMATION
CPU	MONITOR	DATA SHEETS
DISK	UTILITIES	SITE PREP GUIDE
TAPE	DBMS	SALES CONFIGURATORS
USER I/O	LANGUAGES	SERVICE TOOLS
PRINTER	DATATRIEVE	INSTALLATION MANUAL
TERMINAL	COBOL	FUNCTIONAL DIAG.
INTERCONNECT	APPLICATIONS	TRAINING
DECNET	WORD PROCESSING	TECHNICAL MANUALS
CX/DX	DIBS	INTERCONNECT PRIMER
.	.	.
.	.	.
.	.	.

SYSTEM INTEGRATION DEFINES ALL THE PIECES AND BINDS THEM TOGETHER

V

SO THAT

THE CUSTOMER SEES ALL OF OUR COMPONENTS AS ONE PRODUCT

COMMERCIAL SYSTEMS ENGINEERING

ISSUE - SHOULD WE REPORT TO SOME CENTRAL HARDWARE ENGINEERING GROUP?

PROS

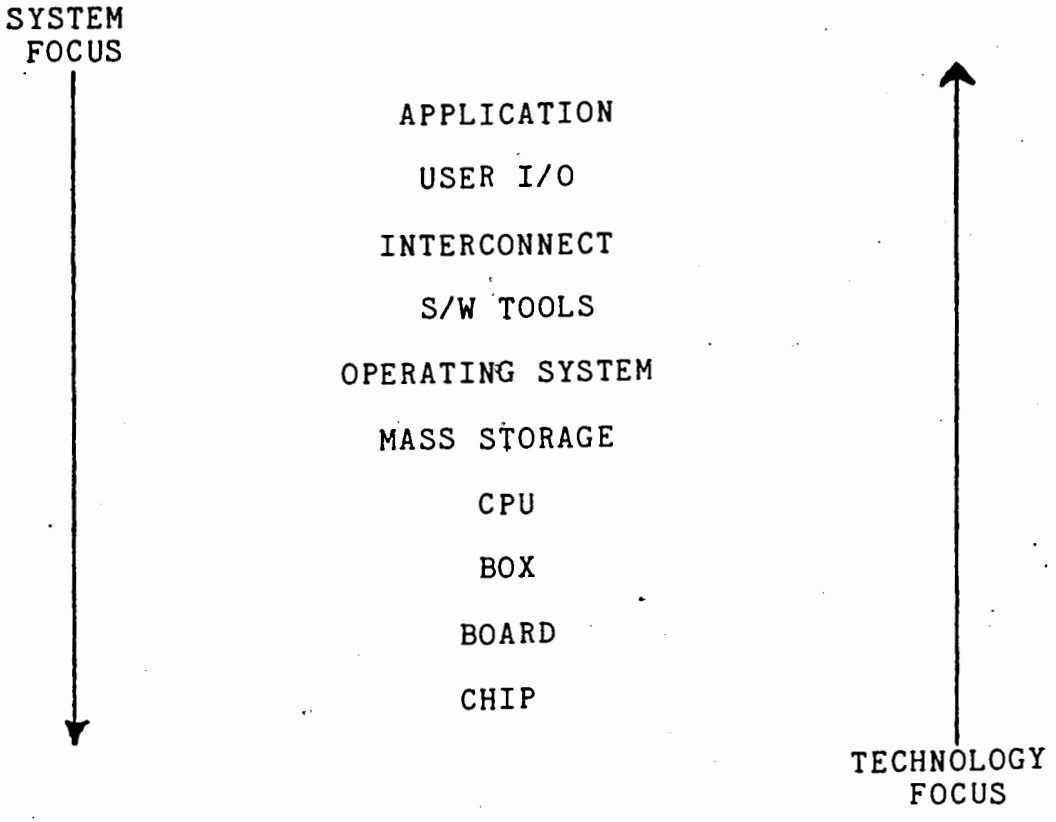
- CENTRAL GROUP WOULD GAIN SYSTEM ENGINEERING EXPERTISE AND EXTRA RESOURCES
- COMMERCIAL SYSTEMS ENGINEERING WOULD GAIN NEW SOURCE OF FUNDS

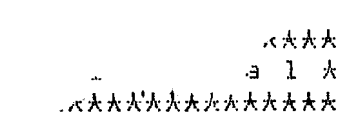
CONS

- NO COMMON GROUND WITH ANY SINGLE HARDWARE GROUP
  - SYSTEMS INTEGRATION CROSSES BOUNDARIES BETWEEN CENTRAL GROUPS
  - SYSTEM REQUIREMENTS COME FROM SOFTWARE APPLICATIONS
- CENTRAL GROUP WOULD HAVE TO ASSUME RESPONSIBILITY FOR PRODUCT LINE SUPPORT
  - PRODUCT LINES DON'T WANT TO HAVE TO RE-CREATE THEIR OWN ENGINEERING RESOURCE
  - CENTRAL GROUPS HAVE TECHNOLOGY FOCUS NOT MARKET FOCUS
- COMPLICATES MANAGEMENT STRUCTURE
  - ALL OUR SPONSORS ARE IN GREATER MERRIMACK

COMMERCIAL SYSTEMS ENGINEERING

SYSTEM FOCUS VS TECHNOLOGY FOCUS





TO: JACK SMITH

cc: see "CC" DISTRIBUTION

DATE: WED 28 APR 1982 3:25 PM EDT
FROM: RON SMART
DEPT: CORPORATE PLANNING
EXT: 223-7011
LOC/MAIL STOP: ML10-1/F41

SUBJECT: ENGINEERING INVESTMENT STRATEGY - HELP NEEDED?

There is pressure to squeeze the Engineering Budget, combined with competitive and market pressure on us to give priority investment to certain strategic products. To be able to resolve this dilemma, a coherent market/product prioritization is required. That is, we have to understand what strategic market segments are available and then we have to estimate their relative importance to us. This "corporate guidance" can then be used along with the Engineering cost and feasibility estimates to decide:

* What to accelerate.

* What to drop.

* Whether to increase or decrease the overall Engineering Budget.

These decisions can't possibly be made by meetings of the parties who are contesting for the investments. However, these parties can clarify the size of the investments and can help estimate the probabilities that the investments will pay off in real products and met schedules. That is, the peer review capability of Engineering can be used to evaluate the liklihood of results from the investments. Don't depend on them to prioritize the importance of the projects.

We keep trying to run DEC as a democracy of high performing teams and we should. However, we also owe those teams a little corporate leadership. I'm willing to help with an analysis of our strategic markets and their relative importance to us. Delagi could help. Etc.

As a test case, following on the Office Automation presentation to the WOODS in Mount Royal, these people are coming back as requested with recommendation for accelerated investment. They will be on your calendar momentarily. This is only one of several strategic product issues. Next will be the low-price high-availability product, then probably interconnect/clustering, maybe microVAX, etc.

mr

JTION:

xGORDON BELL	RICK CORBEN	WIN HINDLE
TED JOHNSON	LARRY PORTNER	

****
digital
****

INTEROFFICE MEMORANDUM

TO: AL BERTOCCHI

CC: Gordon Bell
Jack Smith
Bill Thompson

DATE: 28 APRIL 1982
FROM: JOE REILLY
DEPT: CE FINANCE
EXT: 223-6883
LOC/MAIL STOP: ML12-2/A16

SUBJ: ENGINEERING PRODUCT ANNOUNCEMENTS

Al, attached are the major products by categories we will announce starting with the May announcement and continuing throughout FY83. Please note the following:

- Engineering Cost/Date is in $ MEG.
- Manufacturing Cost Estimates are in $ K.
- Advertising for combination of Low-End systems is $22MEG/per Bob Lane's office.
- Data collection came from Yellow Book, Engineering Budget, and Individual Managers. Where data differed, the most conservative dates were used.
- In some cases advertising/promotion costs are not applicable (i.e., Disks/Tapes/Software).
- Software has so many products some of them were categorized as enhancements.
- FRS = First Revenue Ship.
- Some products have a low Engineering investment because they are using another product's previously developed technology.
- Some products are buyouts.
- Software announcement dates on average are three months prior to FRS.

JR

DISK1:1.57

MAJOR PRODUCTS

	ANNOUNCE DATE	FRS	PRODUCT MANAGER	ENG COST/ DATE ($M)	COST MFG (XFER)($K)	ADV. PROMO COST
SYSTEMS						
11/730 NEBULA	Q4-82	Q1-83	PHILIPPON	8.3	6.5	
2080 JUPITER	Q2-83	Q4-83	R. FIORENTINO	15.0	180.0(AUG SYST)	400-600K (EST)
CT100 FAMILY	Q4-82	Q1-83	E. LAZAR	14.0	3.2	
DECMATE II	Q4-82	Q2-83	J. COX	.6	1.1(83)	22M
RAINBOW 100	Q4-82	Q2-83	B. FOLSOM	1.5	1.2(84)	
LCP-5	Q4-82	Q4-83	N. RICH	1.0	2.9	120K
WORKSTATIONS						
AGATE	Q3-83	Q4-83	N. KHAN		4.5	N/A
ONYX (VS100)	Q2-83	Q2-83	N. KHAN	2.8	2.5	N/A
OPAL (VS500)	Q4-82	Q2-83	N. KHAN		25.0	N/A

MAJOR PRODUCTS

	ANNOUNCE DATE	FRS	PRODUCT MANAGER	ENG COST/ DATE ($M)	COST MFG (XFER)($K)	ADV. PROMO COST
TAPES AND DISKS						
RX50	Q4-82	Q2-83	D. LESLIE	3.3	.330	N/A
RD50	Q4-82	Q2-83	I. LYLES	1.1	.950	N/A
RC25(AZTEC)	Q2-83	Q4-83	J. FORDE	6.3	3.0	N/A
RA81	Q4-82	Q1-83	K. SMITH	2.9	4.8 (84)	N/A
RA60(PINON)	Q4-82	Q2-83	K. SMITH	5.5	3.7 (85)	N/A
HSC-50		Q4-83	K. SMITH	7.3	7.7 (85)	N/A
TU80	Q2-83	Q3-83	B. NAAS	.1	-	N/A
TU81	Q3-83	Q1-84	B. NASS	.5	-	N/A
UDA-52	Q3-83	Q4-83	K. SMITH	-	-	N/A
TA78	Q3-83	Q4-83	J. SWAN	.7	-	N/A

MAJOR PRODUCTS

	ANNOUNCE** DATE	FRS	PRODUCT MANAGER	ENG COST/ DATE ($M)
SOFTWARE				
16 BIT OPERATING SYST ENHANCEMENTS	-	-	MANY	17.9
16 BIT LAYERED PRODUCTS ENHANCEMENTS	-	-	MANY	3.7
32 BIT				
VMS 3.0	-	Q4-82	T. KEMPSELL	
VMS 3.B	-	Q4-83	T. KEMPSELL	15.0
SMALL VMS V.1	-	Q4-83	T. KEMPSELL	
CAT/TMS/VTC V.1	-	Q3-83	H. SNYDER	1.1
TPSS V.1	-	Q3-83	B. LYONS	.9
VAX 11 APL V.1	-	Q1-83	R. MATUS	.2
VAX 11 RDMS V.1	-	Q4-83	A. MOEDER	.3
VAX 11 DEC/CMS V.1	-	Q4-82	C. BRADLEY	.2
VAX 11 C V.1	-	Q4-82	R. MACLEAN	.2
32 BIT LAYERED PRODUCT ENHANCEMENT	-	-	MANY	2.4
DIST SYS				
DECNET SOFTWARE (INCLUDING EHTERNET)	-	-	MANY	4.0
X-25 IBM INTERNET	-	Q3-83	MANY	.8
OFFICE VAX	-	-	B. STEWART	4.3*
OFFICE CT	-	Q3-83	R. GRIFFIN	.4*
36 BIT OPER SW	-	-	MANY	1.2
36 BIT COMM SW	-	-	S. PASSON	.4

*$ IN OFFICE VAX ALSO APPLIES TO OFFICE CT BUT CAN'T BE SPLIT OUT.
**ON AVERAGE 3 MONTHS PRIOR TO FRS.

MAJOR PRODUCTS

	ANNOUNCE DATE	FRS	PRODUCT MANAGER	ENG COST/ DATE ($M)	COST MFG (XFER)($K)	ADV. PROMO COST
TERMINALS/PRINTERS						
VT199	Q2-83	Q3-83	G. KEELER	0	.450	-
VT201	Q2-83	Q3-83	G. KEELER	.7	.650	-
VT210	Q2-83	Q1-84	G. KEELER	2.0	.950	-
LA50	Q4-82	Q4-83	D. COTTON	.2	.250	-
LN01	Q4-82	Q2-83	D. COTTON	.1	10.3	-
LA100KSR	Q4-82	Q1-83	D. COTTON	3.0	.750	-
SYSTEM OPTIONS						
CI780	Q4-82	Q3-82	P. CHEN	3.4	4.5	-
ETHERNET PROD FAM						
PLUTO	Q4-83	Q1-84	M. RESSLER	1.0	4.5	-
UNA	Q4-83	Q4-83	D. CLEVELAND	.6	1.0	-
CHIPS						
J11	Q4-82	Q4-83	E. BALCH	.7	.120	120K

APR 22 1982

digital

INTEROFFICE MEMO

TO: Gordon Bell
Jim Cudmore
Jeff Kalb
Joe Reilly
Jack Smith

DATE: 15 APR 82
FROM: Steve Teicher S Teicher (2'00)
DEPT: SEG Administration
EXT: 4900
LOC/MAIL STOP: HL2-2/N07
ENG. NET ADDRESS: CHIPS::TEICHER

SUBJECT: SEG FUNDING ALLOCATION

The current forecasted spending for SEG for FY82, overall is $30M, divided as follows:

OOD	$ 17.4M
E97	6.1M
User	6.5M
	$ 30.0M

For FY83, accounting changes*, plus EBEAM**, operation, add 2.5M to SEG expenses, over FY82. Vendor payments for FY83 are not forecasted to be significantly lower than FY82, and in fact may be higher due to J-11 and ROM/RAM start-up.

Therefore, a flat run rate, i.e. no additions to headcount would be as follows:

$ 30M base	+	$ 2.5M accounting changes + EBEAM	+	$ 3M inflation + increased depreciation due to equipment received mid to end FY82	=	$35.5M

Checking this number with our actual run rate data, including exisiting people plus outstanding offers, also yields $35.5M. This also checks with a detailed bottoms-up budget for each project.

In addition, we are currently short critical engineering skills in CAD, Layout, design, and process -

	Engineer	Tech	College	Implications of not Hiring
CAD	8		11	Delays to Scorpio, Nautilus
Scorpio	11	2	3	Delays to Scorpio
J-11 FPA	1			Delay to J-11
VT200	1			Risk to VT200 upper chip
Advanced Development				
RTL Structures	1			Lack of technical conver. for NANOVAX
Process	2			Strategy of Photo Eng. for ZMOS and CMOS
	24	2	14	

If we were to execute our hiring plans, our spend rate for FY83 would be $38M. We believe this should be allocated as follows:

OOD	$ 22.0M
User	9.0M
E97	7.0M
	$ 38.0M

We are continually examining how to reduce expenses, and be more efficient. For instance, we believe by squeezing, we can get an additional $1.5M worth of work out of our people, which we plan to use to support an effort to increase the number of chips we produce in SEG. Our target is 1 chip a month by the end of FY83 and 2 chips per month by the end of FY84.

At this time, it is far easier to get more work done, than to reduce expenses. The reason for this is that we do not have redundant CAD efforts, etc., so while we have difficulty dropping a program, adding another development that makes use of a common program, or even a common layout is possible.

Steps that we are taking or will be taking to maximize investment effect.

A. We are centralizing control of computer resources to improve service, and to reduce costs.

B. We are carefully examining make-buy decisions in CAD, and do our best to take the most economic path, considering development, support, and usage costs.

C. We are working with Manufacturing to eliminate redundant operations in the process development space, if and where this exists.

D. We are explicitly developing semiconductor processes, methods of design, CAD tools, etc., that are aimed at reducing the cost of time of chip development.

Finally

We are continuing to examine our numbers, and our plans. We would like to suggest two things:

A. That our total budget be firmed up quickly, including OOD, E97,and User. There is sufficient instability in the environment keeping any part of the plan up-in-the-air delays work. We have detailed project-by-project plans to facilitate this process of reviewing and firming the budget.

B. We be allowed to present plans and progress to those of you in management who have the time, interest, and skills to give us feed-back. While we believe that we are headed in a direction that will add significantly to the products and the technological capabilities of Digital, we welcome suggestions of how to do even better.

* Site allocations of $1M were in FY82 charged to Manufacturing and in FY83, charged to Engineering.

** EBEAM was operating only for one quarter in FY82.

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* d i g i t a l *
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TO: EMC:

cc: CHARLES PICARIELLO

DATE: THU 22 APR 1982 10:30 AM EST
FROM: JOHN ROSE
DEPT: ENG/ADMIN
EXT: 223-3745
LOC/MAIL STOP: ML12-2/T54

SUBJECT: OPERATING PLANS - BEIGE BOOKS

We are embarked on generating an updated set of beige books (multi-year operating plans) by Peg and staff groups to issue by 1 Aug. 82. I think we need them as a vehicle for communicating our plans. My questions to you guys are:

1) Do we generate these plans by the old Peg organization structure as currently planned, or by the new EMC organizational structure?

2) Do we need to publish a set of staff beige books for Personnel and finance? Will a set of committed metrics and MBO's from the staf to EMC suffice for staff beige books?

John

22-APR-82 10:29:54 S 31010 EMML

EMML MESSAGE ID: 5101173459

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* d i g i t a l *
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TO: EMC:

DATE: WED 21 APR 1982 5:43 PM EST
FROM: JACK SMITH
DEPT: MFG ADMINISTRATION
EXT: 223-2231
LOC/MAIL STOP: ML1-4/A54

SUBJECT: CUTTING

The latest Product Line MOR projections for FY83 are in. When overlaid against total Corporate spending projections, we come up short. First pass would indicate we must cut 30M from the Engineering budget targets we had set a couple of weeks back. At our next meeting, please come prepared to discuss alternatives for cutting this 30M. Do not limit your alternatives to product areas you directly manage. Let's plan on working this as a "Total Engineering Management issue".

CAG:1.129

21-APR-82 17:54:10 S 26366 EMC1

EMC1 MESSAGE ID: 5101010353

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* d i g i t a l *
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TO: OPERATIONS COMMITTEE:

cc: PERS MGMT COMM:

DATE: FRI 23 APR 1982 9:07 AM EST
FROM: SHEL DAVIS
DEPT: CORP PERSONNEL
EXT: 223-2838
LOC/MAIL STOP: PK3-1/C21

SUBJECT: IMPLEMENTING WOODS MEETING DECISION - WORKFORCE ISSUES

COMPANY CONFIDENTIAL

This memo confirms our discussion at the April Woods on the work force issues we face. Here are the steps we agreed to take to manage these issues:

1) Identify and take appropriate action with respect to non-performers. Your action plans should be reported to Chuck Poe, U.S. Employment Manager, after-the-fact through your Group Personnel Managers. (We decided on this step as a simple way of assuring ourselves that this part of our plan has indeed been implemented.) It will be important to have the identification of non-performers accomplished quickly so that the steps that follow can be addressed effectively and with credibility.

2) Create a list of good extra people (in excess of your current and near-term needs) in time for the May Budget Woods.

3) Create a list of hiring needs in time for the May Budget Woods.

4) Within your part of the company, roll up lists 2 and 3 and submit a copy of these lists to Chuck Poe through your Group Personnel Managers.

5) Develop action plans.

Ownership for the resolution of these staffing issues clearly rests with line management. The Personnel function will play a leadership role. We are creating a U.S. Employment Information Center to play a clearing house and linkage role. I am asking each Group Personnel Manager to effectively communicate with the Center on extra people and hiring needs. The Center will aggregate the information, provide analyses, and make specific recommendations to the Operations Committee.

I am asking each of you to clearly communicate this to your staffs and to effectively implement steps 1-4 above. Working together, we will implement step 5 in as simple and efficient a way as possible.

GO BURT DECGRAM ACCEPTED S 11427 O 222 25-APR-82 16:26:23

****
* d i g i t a l *
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TO: JACK SMITH

cc: EMC:

DATE: SUN 25 APR 1982 5:18 PM EDT
FROM: GORDON BELL
DEPT: ENG STAFF
EXT: 223-2236
LOC/MAIL STOP: ML12-1/A51

SUBJECT: SHARPENING UP OUR WORKFORCE

Jack,
Would you lead us through this one as a veteran?

In addition, I think we agreed to have two types of budget, one assuming that there could be no movement of low performers and one assuming that we did not have these people. I think we have to do this in the process. List 2 should be rated according to capability (rating).

ATTACHED: MEMO;63

****
* digital *
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TO: see "TO" DISTRIBUTION

cc: JOHN ROSE

DATE: WED 21 APR 1982 8:25 AM EST
FROM: SAM FULLER
DEPT: SA&T
EXT: 225-6060
LOC/MAIL STOP: HL2-3/N11

SUBJECT: SUMMARY OF FY83 BUDGET FOR SA&T

We have begun planning to run SA&T in FY83 within the proposed $11.9M budget, rather than our original $12.6M. However, there are several factors I need to apprise you of.

1. We will hold RAD funding in FY83 at the FY82 spending level, $1.5M.

2. The groups within SA&T will continue with their same level of external funding as they have now. (We are continuing to work to simplify this by getting multiyear commitments in some cases, and move project groups out of SA&T and into the funding PEG groups in other cases. I feel I can manage these two items.

However, I need your commitment ASAP on the funding for the West Coast Research Lab. John Rose will provide $.5M for fitup, etc., but I need your approval for the additional $1.0M out of the Technology pot. Please advise.

/ic
SF11:27

"TO" DISTRIBUTION:

*GORDON BELL JOSEPH KELLY JACK SMITH

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* d i g i t a l *
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TO: *GORDON BELL
JACK SMITH

DATE: FRI 23 APR 1982 4:22 PM EST
FROM: JOSEPH REILLY
DEPT: CE FINANCE
EXT: 223-6883
LOC/MAIL STOP: ML12-2/A16

SUBJECT: FY82 ACTUALS

RLO/D1/S9/4.28

I want to let you know that our Q4 spending rate will bring us over budget. This has clearly been Forecast in the Redbook.

	ACT/FOR	BOD	VARIANCE
ACT Q1	54.9	55.5	.6
ACT Q2	58.6	60.5	1.9
ACT Q3	67.3	66.0	<1.3>
FOR Q4	77.5	72.5	<5.0>
	258.3	254.4	<3.8>

Q3 we overspent by $1.3 MEG. About $1 MEG was mischarged (production materials, etc.). That will be cleared out in Q4. I have about 1.2 MEG contingency in our Q4 Forecast.

The majority of our overspendings is a result of the combination of a poor Terminals/Workstation plan along with the acceleration of projects as agreed to in December.

CENTRAL ENGINEERING SPENDING

	YTD Q3/82		FORECAST Q4		FULL YEAR 82	
GROUP	ACTUAL	FAV (UNFAV) BOD	ACTUAL	FAV (UNFAV) BOD	ACTUAL	FAV (UNFAV) BOD
PSD	5.3	.6	3.6	(.8)	8.9	(.2)
TERM & W	21.9	(3.0)	9.7	(.6)	31.6	(3.6)
32 BIT	17.0	(.2)	6.9	(.2)	24.0	(.2)
DIST SYST	12.1	.1	4.9	-	17.0	-
LSG	19.9	.1	8.3	(.3)	28.0	-
STORAGE SYS	30.6	.1	13.2	(.6)	43.8	(.5)
SEG	11.7	1.1	4.5	-	16.2	1.1
SOFTWARE	34.2	(.2)	13.8	-	48.0	(.2)
SA&T	7.0	.4	3.0	-	9.9	.2
TOPS	4.7	.7	1.9	-	6.6	.6
PTD	5.6	(.4)	1.6	.3	7.1	-
CENTral	10.7	1.5	4.9	-	15.6	(.1)
MISC	-	.4	1.2	(2.8)	1.2	(.8)
TOTAL	180.7	1.2	77.5	(5.0)	258.2	(3.7)

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TO: JACK SMITH

cc: *GORDON BELL
JOSEPH REILLY
CAROL REID

DATE: FRI 16 APR 1982 4:39 PM EST
FROM: BILL DEMMER
DEPT: 32 BIT SYSTEMS
EXT: 247-2112
LOC/MAIL STOP: TW/D19

SUBJECT: FY83 BUDGET

I have reviewed the FY83 budgets for the major development programs in the 32 bit area and have concluded additional Product Line or other funding beyond Scenario A will be necessary to meet all the objectives expected of these products and that we cannot reduce their spending plans without impacting them. A comparison of the FY82 and FY83 spend plans for these projects are shown in the attached. While this shows a significant increase it should be noted that about $14M of the FY83 funds will actually be spent outside of Tewksbury and that it is reasonable to expect these development projects to proceed as planned if we can find the critical design resources.

Realizing that we are faced with a major funding problem across Engineering and that we must sacrifice some activity and plan for some productivity improvements, I am recommending that we cut back our Advanced Development plan and reduce other Non-Development and contingency funds ($9M total) by $2M or 20+% from these areas.

Given the state of the Engineering Budget I am sorry I can not be more responsive to the overall need, but if Digital wants to proceed with its current 32 bit Strategy, I cannot accept any further reductions. We of course can lower the priority of this strategy. However, given the corporations dependency on the 32 bit Products to support one-half of the corporation's revenues throughout the last half of the 80's it would appear unwise to further reduce the number of products in our strategy. Therefore, I urge that you approve the modifications proposed in this memo.

Carol Reid our Financial Manager has done a spending analysis based upon our Q4FY82 spending rate which indicates the feasibility of achieving our FY83 plan if you or Joe have any concerns in this area.

Jack I would be happy to conduct a review of the 32 bit Development Programs for you, if you believe we still must make further cuts across Engineering. Meanwhile I will reaffirm our priorities for this list of programs as any furhter reductions must come out of one of them rather than impacting them all. I would also like to see if we can get a formalized statement of priorities for all Engineering programs.

WHD:eg
HLC 1.37

[redacted]

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* d i g i t a l *
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TO: JACK SMITH

cc: *GORDON BELL
JOSEPH REILLY
CAROL REID

DATE: FRI 16 APR 1982 4:39 PM EST
FROM: BILL DEMMER
DEPT: 32 BIT SYSTEMS
EXT: 247-2112
LOC/MAIL STOP: TW/D19

SUBJECT: FY83 BUDGET

I have reviewed the FY83 budgets for the major development programs in the 32 bit area and have concluded additional Product Line or other funding beyond Scenario A will be necessary to meet all the objectives expected of these products and that we cannot reduce their spending plans without impacting them. A comparison of the FY82 and FY83 spend plans for these projects are shown in the attached. While this shows a significant increase it should be noted that about $14M of the FY83 funds will actually be spent outside of Tewksbury and that it is reasonable to expect these development projects to proceed as planned if we can find the critical design resources.

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WHD:eg
RLG 1.37

	FY82	FY83	
Current VAX	10.4M	10.0M	
Scorpio	5.0	8.0	
Nautilus	2.1	6.6	
MicroVAX	-	2.0	
VAXStations	2.6	6.5	
FCC	.9	1.5	
CI Cost Reduction	-	.8	
	21.2M	36.0M	
Advanced Development	1.2	2.2*	
Non Development	5.5	5.0*	*Proposal - Reduce by $2M
Contin/Var	1.0	1.8*	
	26.9M	45.0M	
16 Bit-Dist Sys FCC	-	1.5	
Overall 32 Bit Prog Contin.	-	.5M	
	26.9M	40.0M	(Includes approx $2.5M of P/L funds)

Please reference Carol Reid's ems of Thursday, April 15, 1982, 5:27 p.m. attached.

ATTACHED: MEMO;98

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* digital *
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TO: BILL DEMMER

DATE: THU 15 APR 1982 5:27 PM EST
FROM: CAROL REID
DEPT: D&MS FINANCE
EXT: 247-2800
LOC/MAIL STOP: TW/D19

SUBJECT: Q4 SPEND RATE VS. FY83 BUDGET

I have analyzed 32 bit Systems FY83 budget requirements from the prospective of our Q4FY82 spend rate.

Our last Q4FY82 forecast (using February results) indicates we will spend $6724K in Q4. Adjusting this for Q4 product line funding ($1078K) and the 14 week quarter brings the spend rate to $7245K. In addition, we will be reversing $750K in prototype expenses bringing our run rate up to $7995K. If we assume a 5% increase from Q4 to Q1 (actuals are higher from quarter to quarter but due to productivity improvements, I am assuming low) and a quarterization such that Q1 is 21% of the total year, 32 bit spending for FY83 becomes $39,576. It is important to remember that in our Scenario A request was $2.3M for PCC, Chip and Board Software and 32 bit program funding which we were requesting for 16 bit, Distributed Systems, and Software. Adding that to our spend rate brings us to $42209K. The specific calculations are shown below.

It is obvious from this analysis that the $6M cut to our FY83 budget cannot support existing programs let alone acceleration of Nautilus, Scorpio and Workstations.

32 Bit Systems

FY83 Spending
Using Q4FY82 Run Rate

February Q4 Forecast	6724	(may change after receipt of Q3 results)
Plus: P/L Funding	+1078	
	7802	
Adjustment for 13 wk quarter	7245	
Plus: Prototype credits in Q4	+ 750	
Q4 run rate	7995	
Q4 to Q1 increase assumed 5%	8395	

If Q1 is 21% of FY83 total,

then FY83 total	39970
Plus: Funds requested for other groups	
FCC for 16 bit, Dist. Sys.	+1293
Chip and board S/W	+ 700
32 Bit Program	+ 500

	42269

Looking at our FY82 spend plan (including product line funding) versus our FY83 budget, you can see that most of the expected growth is in the new products groups (Nautilus, Scorpio and Workstations). The FY83 spend plan column indicates that some of the development groups require product line funding to meet their Scenario A product goals.

	Spend Plan FY82	FY83 Scenario A Budget	Spend Plan FY83
Nautilus	$2.1M	$6.0M	$6.0M
Scorpio	5.0	6.2	6.0
Workstation	2.6	6.3	6.3
Micro VAX	-	2.0	2.0
Current VAX	10.4	10.6	10.6
FCC	.9	1.5	1.5
Cost Reduced CI	-	.8	.6
Adv Development	1.2	2.2	2.2
Non-Development	5.5	5.0	5.0
Contingency & Variance	1.0	1.0	1.0
	----	----	----
	28.9	42.6	45.0
16 Bit/Dis. Sys FCC & Elec	-	1.5	1.5
32 Bit Program Contingency	-	.3	.3
	----	----	----
	28.9	44.4	46.8**

**Includes approx. $2.5M from product lines.

APR 20 1982

5.48

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* D I G I T A L *
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INTEROFFICE MEMORANDUM

TO: Jack Smith

CC: PEG
Rick Corben

DATE: 16 April 82
FROM: MIKE GUTMAN
DEPT: PSD
EXT: 223-5285
LOC/MAIL STOP: ML12-2/E71

SUBJECT: ENGRG FUNDING

We are in the process of killing all the gains we've made over the last two years in funding of engineering. Last year went very well because we:

1. Did not disturb the base plan which we we're already executing.
2. We asked GVPC to help us prioritize the new opportunities (B & C scenarios).
3. We spent time reviewing our scenarios with the Product Groups.

The results were great - expectations and resources were far better matched up, and the work we had started was not disturbed.

The way we're headed right now will do us in - our resources and the expectations will become monumentally misaligned - and we'll pay for it in hassle and replanning for years to come.'

Let's go back to last years progress. I think we can do it in two weeks if we try.

1. Get our plans into A, B, C Scenarios.
2. Review them (once more) with Product Groups.
3. Present to GVPC for decision.

/df

WPS USERS - Enter HP mode and then type <CR>
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TO: *GORDON BELL
JACK SMITH
cc: see "CC" DISTRIBUTION

DATE: FRI 10 APR 1982 1:44 PM EST
FROM: STEVE BEHRENS
DEPT: SOFTWARE ENG
EXT: 225-4505
LOC/MAIL STOP: ML12-3/A62

SUBJECT: FUNDING FOR CMU

The CMU project is not in Software Engineering's plan for the budget (see attached memo: Bill Johnson to Gordon Bell, Jack Smith). This project is in the beginning stages of negotiations. We hope to conclude these negotiations shortly so that the joint venture can begin in July 1982.

The estimated FY83 funding for this operation is approximately $2.0 million to cover both Digital personnel and funding to CMU to aid Digital in various advanced development projects, especially in the area of personal computer networking. Additional funding will also be required for establishing a facility in Pittsburg and for relocation.

This memo constitutes a formal request for FY83 funding for this project.

SAL:DE

****
ATTACHMENT:

TO: GORDON BELL
JACK SMITH
cc: BILL DEMMER
BOB DOCKSER

DATE: TUE 13 APR 1982
FROM: BILL JOHNSON
DEPT: SOFTWARE DEV
EXT: 225-3982
LOC/MAIL STOP: ML12-3/A62

SUBJECT: HERE'S WHAT'S HAPPENING

Here's what I have going:

1. Win reviewed and felt comfortable with the special stock.

2. Ulf and Bill will provide alternative E budget needs. They really can't live with the allocation. CMU is NOT in my plan for the budget.----------->NOTE! Bernie has no special request.

3. FY84-85-86-87 - Software Engineering is proposing a strategy in this space with budget to match.

4. Ulf, Bill, Bernie and I will meet to look at "groups we fund," "should manage" or "should group together." This is during our cancelled Jungle meeting. Can you wait for our feedback before any org. changes in Sam's,

Hoffman's, Thompson's shop?

5. Bill Demmer will pursue the Cray research as requested.

6. Bill Demmer will be in charge overall. Bocksor will be managing software.

I'm planning on a great vacation.

"CC" DISTRIBUTION:

STEVE BEHRENS
BILL JOHNSON
ED BOCKSER
JOSEPH KELLY
OWEN FISK

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* d i g i t a l *
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MEMORANDUM

TO: GORDON BELL
JACK SMITH

CC: Rick Corben

DATE: 14 APRIL 1982
FROM: JOE REILLY
DEPT: CE FINANCE
EXT.: 223-6883
LOC/MS: ML12-2/A16

SUBJECT: BUDGET UPDATE

A poll at my Staff meeting revealed the following budget update:

GROUPS THAT AGREE WITH PROPOSAL	GROUPS THAT DISAGREE WITH PROPOSAL	HAVE NOT HEARD
16-BIT	36-BIT	LSI
TERM. & WORK.	32-BIT	NEW SITES
DIST. SYS.	SOFTWARE	EURP. ENG.
TOPS	STORAGE	EXTERNAL RESOURCES
PTD		
SA&T		
CENTRAL		

Friday, 4/16/82, is the date the Groups are to respond to us with their official word. We will then put in place a process to close this budget.

Additional requests over and above the "A Scenario" are building in the system. My feeling is that we should address them after we look in the "A Scenario"

Requests not included in "A Scenario":

-- West Coast Facility
-- Acceleration of some 16-Bit programs
-- Additional Terminals & Workstations projects

JR
RL0.4.20

WPS USERS - Enter HP mode and then type <CR>
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TO: JACK SMITH

cc: see "CC" DISTRIBUTION

DATE: THU 15 APR 1982 9:16 AM EST
FROM: DICK CLINTON
DEPT: ENGRG. FINANCE
EXT: 223-1932
LOC/MAIL STOP: ML12-2/A16

SUBJECT: RE: CLOSING THE ENGINEERING BUDGET - "CENTRAL" GROUP

RLO/DISK1/SECT5/2.25

The "Central Group" will deliver its FY83 "A" scenario commitments within the new (lower) budget of $15.9M.

	ORIGINAL	RECOMMENDED NEW	
CENTRAL:			
OOD SALARY, FRINGE, SECS	2600	2700	4% CUT (MAY NOT BE POSSIBLE)
STOCK OPTIONS	2690	2690	NO CUT
P.M. (COREEN'S GROUP)	500	400	20% CUT
HANDOFF'S (TAXES)	1450	1520	UP, PUSHING BACK
DELAGI PROJECTS	120	75	40% CUT
VANROEKEN'S PROJECTS	165	75	60% CUT
CAD AND UNALLOCATED	1607	1145	
FINANCE (REILLY)	2667	2480	7% CUT ON NO-ADD PLAN(MAY NOT BE POSSIBLE)
PERSONNEL (BORNSTEIN)	2275	2115	7% CUT
ADMIN (ROSE)	2902	2700	7% CUT ON NO-ADD PLAN (MAY NOT BE POSSIBLE)
	17,196	15,900	8% CUT

The "recommendations" are established as aggressive targets. Since the Finance and Admin "original" plans were zero population growth, further cuts of 7% may be difficult. The proposed cut of OOD Salary is subject to confirmation by JS/GB.

Managers of each group should examine whether the "recommendation" is acheivable, and confirm by April 30.

15-APR-82 09:15:30 S 19600 EMML

EMML MESSAGE ID: 5160469962

"CC" DISTRIBUTION:

*GORDON BELL
BRUCE DELAGI
PETER VAN ROEKENS
LARRY BORNSTEIN
JOSEPH REILLY
RICK COREEN
JOHN ROSE

****
* d i g i t a l *
****

MEMORANDUM

TO: AL BERTOCCHI
AMIT NANAVATI

DATE: 9 APRIL 1982
FROM: JOE REILLY
DEPT: CE FINANCE
EXT.: 226-6883
LOC/MS: ML12-2/A16

SUBJECT: F&A TARGETS

The following is in response to your memo of 10 March 1982 to Gordon Bell.

		JAN 82	APR 82	FY83*	FY84	$8B
FINANCE	WC1&2	8	9	10	11	16
	Consultants	8	9	12	14	22
	Analysts	66	64	74	82	92
	Accountants	10	11	13	15	17
	Managers	30	31	32	33	34
		122	124	141	155	181
MIS**	WC4		139	142	145	169
	WC1&2		113	119	124	145
	TOTAL		252	261	269	314
FACILITIES**						
	WC4		29	36	63	76
	WC1&2		55	85	147	176
	TOTAL		84	121	210	252
OFFICE SERVICES**						
	WC4		8	10	14	20
	WC1&2		16	20	36	52
	TOTAL		24	30	50	72

* Delta from current to FY83 for Finance Headcount will be inside hires only.

2 - Fin. Dev. Prog.	1 - New Facilities
1 - Conversion	2 - New Mfg. Board Shop
7 - Replacements	2 - Growth
2 - General Ledger	

** Prime factor driving growth in these areas is the geographical dispersion of Engineering into new sites inside and outside of New England. Computer Operations, Applications Programmers, Maintenance, Office Services, Security, etc.

JR
1.1.40
Revised 4/12/82 by Rose for Bertocchi and Amit.

****
* Digital *
****

TO: JACK SMITH

cc: *GORDON BELL
JOSEPH REILLY
CAROL REID

DATE: FRI 16 APR 1982 4:39 PM EST
FROM: BILL DEMMER
DEPT: 32 BIT SYSTEMS
EXT: 247-2112
LOC/MAIL STOP: TW/D19

SUBJECT: FY83 BUDGET

I have reviewed the FY83 budgets for the major development programs in the 32 Bit area and have concluded additional Product Line or other funding beyond Scenario A will be necessary to meet all the objectives expected of these products and that we cannot reduce their spending plans without impacting them. A comparison of the FY82 and FY83 spend plans for these projects are shown in the attached. While this shows a significant increase it should be noted that about $14M of the FY83 funds will actually be spent outside of Tewksbury and that it is reasonable to expect these development projects to proceed as planned if we can find the critical design resources.

Realizing that we are faced with a major funding problem across Engineering and that we must sacrifice some activity and plan for some productivity improvements, I am recommending that we cut back our Advanced Development plan and reduce other Non-Development and contingency funds ($9M total) by $2M or 20+% from these areas.

Given the state of the Engineering Budget I am sorry I can not be more responsive to the overall need, but if Digital wants to proceed with its current 32 Bit Strategy, I cannot accept any further reductions. We of course can lower the priority of this strategy. However, given the corporations dependency on the 32 Bit Products to support one-half of the corporation's revenues throughout the last half of the 80's it would appear unwise to further reduce the number of products in our Strategy. Therefore, I urge that you approve the modifications proposed in this memo.

Carol Reid our Financial manager has done a spending analysis based on our Q4FY82 spending rate which indicates the feasibility of achieving our FY83 plan if you or Joe have any concerns in this area.

Jack I would be happy to conduct a review of the 32 Bit Development programs for you, if you believe we still must make further cuts across Engineering. Meanwhile I will reaffirm our priorities for this set of programs as any furhter reductions must come out of one of them rather than impacting them all. I would also like to see if we can get a formalized statement of priorities for all Engineering programs.

eg
1.37

32 Bit Program Spend Plans

	FY82	FY83
Current VAX	10.4M	10.8M
Scorpio	5.0	8.0
Nautilus	2.1	6.6
MicroVAX	-	2.0
VAXStations	2.8	6.3
FCC	.9	1.5
CI Cost Reduction	-	.8
	21.2M	36.0M
Advanced Development	1.2	2.2*
Non Development	3.5	5.0*
Contin/Var	1.0	1.8*
	26.9M	45.0M
16 Bit-Dist Sys FCC	-	1.5
Overall 32 Bit Prog Contin.	-	.3M
	26.9M	46.8M (Includes appro $2.5M of P/L funds)

*Proposal - Reduce by $

Please reference Carol Reid's ems of Thursday, April 15, 1982, 5:27 p.m. attached.

ATTACHED: MEMO;98

****
* d i g i t a l *
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TO: BILL DEMMER

DATE: THU 15 APR 1982 5:27 PM EST
FROM: CAROL REID
DEPT: D&MS FINANCE
EXT: 247-2806
LOC/MAIL STOP: TW/D19

SUBJECT: Q4 SPEND RATE VS. FY83 BUDGET

I have analyzed 32 Bit Systems FY83 budget requirements from the prospective of our Q4FY82 spend rate.

Our last Q4FY82 forecast (using February results) indicates we will spend $6724K in Q4. Adjusting this for Q4 product line funding ($1078K) and the 14 week quarter brings the spend rate to $7245K. In addition, we will be reversing $750K in prototype expenses bringing our run rate up to $7995K. If we assume a 5% increase from Q4 to Q1 (actuals are higher from quarter to quarter but due to productivity improvements, I am assuming low) and a quarterization such that Q1 is 21% of the total year, 32 Bit spending for FY83 becomes $39,976. It is important to remember that in our Scenario A request was $2.3M for FCC, Chip and Board Software and 32 Bit program funding which we were requesting for 16 Bit, Distributed Systems, and Software. Adding that to our spend rate brings us to $42269K. The specific calculations are shown below.

It is obvious from this analysis that the $6M cut to our FY83 budget cannot support existing programs let alone acceleration of Nautilus, Scorpio and Workstations.

32 Bit Systems

FY83 Spending
Using Q4FY82 Run Rate

February Q4 Forecast	6724	(may change after receipt of Q3 results)
Plus: P/L Funding	+1078	
	7802	
Adjustment for 13 wk quarter	7245	
Plus: Prototype credits in Q4	+ 750	
Q4 run rate	7995	
Q4 to Q1 increase assumed 5%	8395	

If Q1 is 21% of FY83 total,

then FY83 total	39976	
Plus: Funds requested for other groups		
FCC for 16 Bit, Dist. Sys.	+1293	
Chip and Board S/W	+ 700	
32 Bit Program		+ 300
		42269

Looking at our FY82 spend plan (including product line funding) versus our FY83 budget, you can see that most of the expected growth is in the new products groups (Nautilus, Scorpio and Workstations). The FY83 spend plan column indicates that some of the development groups require product line funding to meet their Scenario A product goals.

	Spend Plan FY82		FY83 Scenario A Budget		Spend Plan FY83	
Nautilus		$2.1M		$6.0M		$6.6M
Scorpio	5.0		6.2		8.0	
Workstation		2.8		6.3		6.3
Micro VAX		-		2.0		2.0
Current VAX		10.4		10.8		10.8
FCC		.9		1.5		1.5
Cost Reduced CI	-		.8		.8	
Adv Development	1.2		2.2		2.2	
Non-Development	3.5		5.0		5.0	
Contingency & Variance	1.0		1.8		1.8	
		26.9		42.6		45.0
16 Bit/Dis. Sys FCC & Bldg		-		1.5		1.5
32 Bit Program Contingency		-		.3		.3
		26.9		44.4		46.8**

**Includes approx. $2.5M from product lines.

****
* d i g i t a l *
****

TO: JACK SMITH

cc: *GORDON BELL
BILL JOHNSON
DAVE SAWIN

DATE: FRI 16 APR 1982 4:58 PM EST
FROM: ULF FAGERQUIST
DEPT: LS DEV
EXT: 231-6408
LOC/MAIL STOP: MR1-2/E78

SUBJECT: FY83 BUDGET

In order to continue to aggressively push to meet our product delivery goals, I need a 10% incremental FY83 allocation.

I would like to review a proposal for a way that we can approach this exposure while giving you maximum control of spending exposure at any time.

I'd like to have an in depth review of the finance strategies in the two programs - VENUS and JUPITER - including cash flow for capital and material.

APR 12 1982

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* digital *
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MEMORANDUM

TO: ENG STAFF
CE CONTR. STAFF
JACK SMITH

DATE: 9 APRIL 1982
FROM: JOE REILLY
DEPT: CE FINANCE
EXT.: 223-6883
LOC/MS: ML12-2/A16

SUBJECT: CE HEADCOUNT - FISCAL MARCH

The following attachments represent activity for fiscal March. In total our net adds have slowed down.

	FISCAL MARCH	WEEKS 4&5 FISCAL MARCH	Q3 TOTAL
HIRES	87	28	215
TERMINATIONS	27	9	112
NET TRANSFERS	23	< 2>	134
TOTAL NET ADDS	83	17	237

Our growth in March was primarily in Software, Terminals & Workstations, Storage Systems, and LSG. In addition, Terminals & Workstations has opened eighteen (18) requisitions since March 12. Terminals & Workstations is clearly creating a spending run rate issue for themselves as we approach our FY83 budget.

JR
RL0.4.13

CE HEADCOUNT - FISCAL MARCH

NEW REQUISITIONS SINCE 3/12/82

	ADDITION	REPLACEMENT
AVERY	13	5
GUTMAN	1	3
DEMMER	1	3
LACROUTE	--	1
FAGERQUIST	--	4
FULLER	--	1
HOLMAN	--	--
JOHNSON	2	--
SAVIERS	--	--
BORNSTEIN	--	--
REILLY	--	--
THOMPSON	2	3
BELL	--	
TOTAL	19	20

JR
4/09/82
RLO.4.12

CE ENGINEERING

GROUP	BEGIN. POP.	NEW HIRES	TERMINA- TION	NET TRANS.	DELTA	ENDING POP.	LOA
AVERY	469	12	3	17	26	495	2
GUTMAN	95	--	--	1	1	96	--
DEMMER	493	14	--	< 9>	5	498	10
LACROUTE	201	2	1	< 2>	< 1>	200	3
FAGERQUIST	554	9	2	8	15	569	6
FULLER	166	--	4	5	1	167	3
HOLMAN	404	3	4	3	2	406	6
JOHNSON	1369	27	3	< 1>	23	1392	16
SAVIERS	601	14	4	2	12	613	4
BORNSTEIN	132	1	1	< 1>	< 1>	131	2
REILLY	33	--	--	< 1>	< 1>	32	--
BELL	59	--	1	4	3	62	--
THOMPSON	503	5	4	< 3>	< 2>	501	7
TOTAL*	5079	87	27	23	83	5162	59

* Includes LOA, Total Will Thompson.
Does not include Offshore people.

4/09/82
JR
RL0.4.11

APR 13 1982

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* d i g i t a l *
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INTEROFFICE MEMORANDUM

TO: Rick Corben

CC: Joe Reilly
Jack Smith
Gordon Bell
Bill Johnson

FROM: Steve Behrens/Bob Dockser
DEPT: SWE Finance/Planning & Ops
EXT: 223-4385/223-5315
LOC: ML12-3/A62
ACCESS: EMS or TS1::BEHRENS
DATE: 9 April 1982

SUBJECT: SOFTWARE ENGINEERING AND EUROPEAN ENGINEERING

The present Base Plan for Software Engineering still does not provide funding for CMU, Seaboard (32 Bit Chip and Board shortfall) and SUVAX. These projects have been approved but have never been properly funded, as shown in our "March 1982 Presentation for Operations Committee Review." (See attachment.) Software Engineering plans to resubmit a request for these funding dollars by April 16th. Until these funding issues are resolved, Software Engineering cannot make a product delivery commitment.

The present Base Plan for European Engineering causes no changes in the product deliverables for this group.

SAB:de
Attachment

CENTRAL SOFTWARE ENGINEERING

UNFUNDED PROJECTS/ACTIVITY FY82-FY84

($ in 000s)

	FY82	FY83	FY84
APPROVED - FUNDED - AWAITING TRANSFER OF DOLLARS			
Human Factors	60	90	--
SUBTOTAL	60	90	0
APPROVED - NOT PROPERLY FUNDED			
32 Bit Chip & Board (Shortfall)	--	702	793
CMU	--	2000	4000
SUVAX	--	750	900
SUBTOTAL	0	3452	5693
NOT APPROVED			
32 Bit European Language Adaption	--	800	800
Graphics	--	550	576
DECPlot	--	300	350
SUBTOTAL	0	1650	1726
TOTAL INCREMENT	60	5102	7419

SAB:de:1/25

APR 9 1982

digital INTEROFFICE MEMORANDUM

TO: Eng. Staff
FM's

DATE: 9 April 82
FROM: Jim Lawless
DEPT: Central Eng. FP&A
EXT: 223-5811
LOC/MAIL STOP: ML12-2/A16

SUBJ: ENGINEERING BUDGET - FY83

REFERENCE: JACK SMITH'S BUDGET MESSAGE OF APRIL 2, 1982

I wanted to communicate to you the results of Jack's budget recommendations compared with your Scenario A requests and your existing '83 baseplan budgets shown in our update as of 3/31/82.

The enclosed table shows this information with the respective variance from your submitted plans. Note the overall budget decrease of $7.6M from $346.6M to $339.0M.

My plans are to make no moves toward updating your budgets until after any appeals are made as suggested in Jack's memo. Remember you have until April 16 to either go along with the recommended budget or to take issue with it.

Enclosure

/svb

CENTRAL ENGINEERING BUDGET
DIRECT FUNDING

	82	83 SCENARIO A REQUEST	83 BASE AT 3/31/82	RECOMMENDED BUDGET 4/2/82	------VARIANCES------ FROM SCENARIO A REQUEST	FROM BASE AT 3/31/82
PRODUCT ENGINEERING GROUPS						
16 BIT - GUTMAN	8,676	14,443	12,343	13,500	<943>	1,157
TERMINALS & WORKSTATIONS - AVERY	27,868	34,517	34,517	34,500	<17>	<17>
32 BIT - DEMMER	23,613	44,410	37,910	38,000	<6,410>	90
DISTRIBUTED SYSTEMS - LACROUTE	17,047	21,019	21,019	21,000	<19>	<19>
LARGE SYSTEMS GROUP - FAGERQUIST	28,008	33,718	33,718	32,700	<1,018>	<1,018>
STORAGE SYSTEMS DEVELOP. - SAVIERS	43,237	56,768	56,907	52,400	<4,368>	<4,507>
SOFTWARE - JOHNSON	47,468	67,315	63,868	61,300	<6,015>	<2,568>
COMPONENT GROUPS						
SEMICONDUCTOR ENGINEERING - TEICHER	17,382	20,931	16,437	16,400	<4,531>	<37>
TECHNICAL OPERATIONS - HOLMAN	7,292	8,480	8,480	7,500	<980>	<980>
PROCESS TECHNOLOGY DEVELOP.- THOMPSON	8,843	9,238	7,641	7,600	<1,638>	<41>
OTHER ENGINEERING GROUPS						
SA&T - FULLER	10,151	12,783	12,783	11,900	<883>	<883>
ADMINISTRATION - BELL/PORTNER	14,108	17,099	17,241	15,900	<1,199>	<1,341>
NEW SITES - ROSE	893	13,426	13,284	10,000	<3,426>	<3,284>
EUROPEAN ENGINEERING - JOHNSON	1,300	1,520	1,520	1,400	<120>	<120>
TECHNOLOGY EXTERNAL RESOURCES - METZGER	1,334	1,540	1,401	1,400	<140>	<1>
CONTINGENCY	<2,697>	17,350	2,188	-	<17,350>	<2,188>
GENERAL TECHNOLOGY		5,400	5,347	3,500	<1,900>	<1,847>
UNALLOCATED			-	-	-	-
STRATEGIC PROGRAM ASSISTANCE		10,000	-	10,000	-	10,000
PRODUCTIVITY IMPROVEMENT TARGET		<43,353>	-	-	43,353	-
	254,523	346,604	346,604	339,000	<7,604>	<7,604>

ENG STAFF

BILL AVERY	ML12-2/E71
GORDON BELL	ML12-1/A51
LARRY BORNSTEIN	PK3-1/C21
DICK CLINTON	ML12-2/A16
RICK CORBEN	ML12-1/T39
JIM CUDMORE	HL2-2/M11
BRUCE DELAGI	ML2-2/T88
BILL DEMMER	TW/D19
ULF FAGERQUIST	MR1-2/E78
SAM FULLER	HL2-3/N11
MIKE GUTMAN	ML12-2/E71
JOHN HOLMAN	ML23-2/T36
BILL JOHNSON	ML12-3/A62
JEFF KALB	HL2-2/M11
BERNIE LACROUTE	TW/A08
JOE REILLY	ML12-2/A16
JOHN ROSE	ML12-2/T54
GRANT SAVIERS	ML3-6/E94
JACK SMITH	ML1-4/A54
STEVE TEICHER	HL2-2/N07
WILL THOMPSON	QI-1/E21
PETE VAN ROEKENS	ML12-3/A62

FM'S

STEVE BEHRENS	ML12-3/A62
DICK CLINTON	ML12-2/A16
DON CROWTHER	ML3-5/T71
BRUCE GREEN	ML12-2/A16
DICK HASLETT	QI-1/E22
KEN JONES	ML23-2/T36
JIM LAWLESS	ML12-2/A16
DAVID MARKEY	ML5-2/T86
RAY MERCIER	HL1-1/008
LEO MERTA	HL2-3/N11
CAROL REID	TW/D19
DAVE SAWIN	MR1-2/G5
ED SAWYER	ML3-6/E94
MARY ANN SERRA	ML12-2/E71

4/5/82

TO: JACK SMITH

cc: *GORDON BELL

DATE: FRI 9 APR 1982 4:25 PM EST
FROM: GRANT SAVIERS
DEPT: STORAGE SYSTEMS
EXT: 223-9762
LOC/MAIL STOP: ML3-6/E94

SUBJECT: STORAGE FY'83 BUDGET COUNTER PROPOSAL

Your "arbitrary" process yielded a SSD FY'83 cut of 6%. I propose a 5% cut for SSD for the following reasons:

As part of my productivity review preparation, SSD completely bottoms up replanned FY'83, taking major reductions as a result of productivity improvements in several areas. The net reduction was 5.3% or $3000M. Our goal was to cut more.

At this reduced budget, we believe we can deliver the base plan as originally proposed, except for a less aggressive internal development in 8" hard disks, where we are manpower limited and have numerous buy out opportunities. Within the reduced budget, we've added two programs not in the base plan, the HSC Dual Ported and a UDA50 performance enhancement called UDA52. These amount to significant (several $100K) incremental work.

At the same time we see clear competitive needs and excellent opportunities such as Data Base Machines and Mass Storage, Accomplishments for both of these programs are currently under constrained in FY'83.

So, I propose:

1. We take a 5.3% cut (or not replanning) we get no productivity win, this is the maximum cut we'd accept (except...).

2. We agree to this budget with outside hiring approvals calculated to me. We will commit to fill all possible openings internally. Considering SSD's historically excellent performance to budget, I believe this is an appropriate delegation.

3. We will continue to pursue additional productivity enhancements and divert freed resources to our highest priority opportunities.

In FY'83, we are delivering an incredible number of new products:

RA60
RA81
TU20
TA78
UDA52
HSC50
AZTEC
RD/RX box and controller
RD50
RD51

"X50
64K SAM's (everywhere)

Simultaneously, with this new product load, we've got to get started on some FY'85 FRS programs, or it's clear that the FY'83 competitive lead will be cost to CDC and FUJITSU.

We want to help with the profit problem, but let's not churn SSD, where we've got good output and a good plan for the future.

Also, in looking at your "arbitrary" reductions, by PSG, it's clear that reduction percentages varied widely. I do not understand why Storage should take the biggest hit to the original FY'83 plan. Please note that we did not receive significant funds in the January increment to the engineering budget and thus because SSD was on plan, we did not contribute to the "problem". I'd like to understand your thinking on this issue.

FGS:mah

P.S.

I've got some suggestions for areas that could be reduced without affecting product output and would be also to put some work into this with you and Gordon.

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* d i g i t a l *
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TO: OPERATIONS COMMITTEE:

cc: MIKE GUTMAN

DATE: FRI 9 APR 1982 8:57 AM EST
FROM: KEN OLSEN
DEPT: ADMINISTRATION
EXT: 223-2301
LOC/MAIL STOP: ML10-2/A50

SUBJECT: REASON FOR PRODUCT LINE MANAGERS

****
FOR EYES OF OPERATIONS COMMITTEE MEMBERS ONLY - NOT TO BE COPIED; NOT TO BE DISTRIBUTED, AND SHRED BEFORE YOU HAVE A CHANCE TO READ IT TWICE
****

As we organize the marketing discussion for next week's Woods meeting and for the State of the Company meeting in May, it becomes clear that we are badly missing someone and a team to have and develop and propagate a vision for 16-bit computers. As we did after we abolished the 36-bit Product Line, many people claim the right to sell 16-bit machines, and many, many people give advise and pass judgement and make decisions about phasing it out of the immediate future and projecting its demise.

The results aren't any more successful than they were with the 36-bit machines. The salesmen and the rest of the Company hear about how the VAX is going to wipe it out, hear about how the machines will not be supported, and sense the lack of vision and enthusiasm. The results grow on themselves.

Meanwhile Hewlett-Packard is relatively slow in all areas except 16-bit applications, particularly for business. We have a catalog of tremendous successes in business administrative areas along with scientific and industrial areas for our various 16-bit machines and so many of the customers love them. The attitude we project is that it would be immoral to sell these again because they are obsolete now that we have the 32-bit machine. Where can one go except to Hewlett-Packard for a modern 16-bit machine which the customer is enthusiastic about.

We broke the Company into Product Lines because I had the belief that planning groups, management groups, or individuals cannot have a vision or enthusiasm for more than two or three products or markets. When things are done simply or by everyone, only a very small number of things can be done with vision. The vision is held by one person or one small team, and it's not held by a group or company marketing team.

We'd better organize ourselves again for the 16-bit market as we did last year for the 32-bit market, or we'll end up giving the key part of our history to Hewlett-Packard.

KHO/ep
KO1:S10.69

UP2
VFS USERS - Enter HP mode and then type <CR>
****
* d i s i t a l *
****

TO: PSD STAFF:

cc: see "CC" DISTRIBUTION

DATE: MON 1 MAR 1982 2:14 PM EST
FROM: MIKE GUTMAN
DEPT: PSD
EXT: 223-5265
LOC/MAIL STOP: ML12-2/E71

SUBJECT: MEETINGS WITH PRODUCT GROUPS

$ 7.100

Here are the action items which need to be followed up from the first three meetings:

1. COMMERCIAL (Marcus)

   A. With aggressive Nebula pricing RSTS sales for Commercial will go to zero. Only CCEM selling to installed base will have market. Action item: CHUCK - We'd better have a hard look at RSTS sales. Should we continue making investment here? Should this be product line funded or remain central? Also, PETER, implication from this is no RSTS/NI. OK? (Probably needs a team of people to discuss what we owe our RSTS customers - CHUCK).

   B. LCP and Pluto. I didn't understand this discussion. PETER, did you? What is action item if any?

   C. OFIS on "M" not needed. CHUCK, what is implication?

   D. We asked: "Is what PSD doing sufficient to provide commercial with $150M in revenue (LCP) in FY84?" They owe us answer.

2. TECHNICAL END USER (Hindle)

   A. Deeply concerned about the lack of real-time performance on VMS. JESSE/DON - set up meeting with Strauss as coordinator to talk about current 11 and J11 real-time performance. Also Don, tell them about the work you are doing on 11 front end to VAX. They are interested - maybe throw a few bucks your way? Their concern centers around SEL, Perkin Elmer with micro front ends. Harvey Weiss and John Buckley seem most interested.

   B. Concerned about the software support spending. Feel they are paying for it but not getting the revenue. MIKE working this. CHUCK, remind me to bring you up to date on meeting with BJ.

   C. No RSX on OFIS - CHUCK?

   D. TEU wants UNIX strategy clearly stated - CHUCK.

   E. Need to get Strauss' data on investment/NOR - MIKE.

   F. Observation - TEU has no plans to sell systems below $50K.

Their 16 bit stuff will be Unibus.

G. ORION with FPA doesn't make sense - MIKE/PETER - need to keep pressure on this issue to get it funded.

H. Their words and their votins was inconsistent. Action?

5. TECHNICAL VOLUME GROUP (MacKenzie)

A. Shift RT spending to Microposer Pascal. CHUCK - fundins issue here is beins worked in your MPP sessions, but there is an impact on CTS-300 isn't there?

B. Discussion about misration of 16 bit to VAX. Sarles asreed to sive us a more complete expression of the misration needs. VMS not supportins M4.1 and M+ seems like a whole - CHUCK?

C. Customers would like DEC to support UNIX, don't Just want C, want UNIX - CHUCK.

D. Disk requirements seem small for Unibus. Very little need in the 100+ MB class. HERB - seems like an issue you and WALT/SUSAN ought to discuss.

E. Reiter says he'd like a 10 1/2" box for ORION rather than a 5 1/4" + an expansion box. HERB - this needs to be understood.

F. Essential issues - Fundins FPA, PETER/MIKE, multiprocessors (0); DON/HERB/JESSE, Microposer Pascal, CHUCK.

4. SMALL SYSTEMS - Meetins on 3/3.

5. OTHER ISSUES - The Product Groups voted on all Enslneerins Scenario A items. Those receivins very few votes should be looked into. For PSD these were (of a total possible of 8 votes):

1 Vote: FMS-11 Rewrite - CHUCK
1 Vote: RSTS/NI Support - CHUCK/PETER
2 Votes: RSTS enhancements - CHUCK
2 Votes: RT Enhancements - CHUCK
2 Votes: COBOL-81 Replace COBOL-11 - CHUCK
2 Votes: RT New Devices - CHUCK
3 Votes: RSTS New Devices - CHUCK
3 Votes: Fortran Full ANSI-77 - CHUCK
3 Votes: Sort-11 Rewrite - CHUCK

/df

"CC" DISTRIBUTION:

&GORDON BELL	WALT COLBY	RICK CORBEN
ELI GLAZER	WIN HINDLE	SUSAN JANCOURTZ
WARD MACKENZIE	JULIUS MARCUS	LARRY PORTNER

MAR 19 1982

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d i g i t a l
+------------+

INTEROFFICE MEMORANDUM

TO: Bill Demmer, Grant Saviers, Bernie Lacroute, Ulf Fagerquist, Steve Teicher, Mike Gutman, Bill Avery, Bill Johnson, Bruce Stewart, Jeff Kalb
CC: Rick Corben, Joe Reilly, Gordon Bell

DATE: 18 March 1982
FROM: Eli Glazer
DEPT: CORP. PRODUCT MGMT.
EXT: 3-4434
LOC/MAIL STOP: ML12B-T61

SUBJECT: SLIDE OVERVIEW FOR OPERATION COMMITTEE REVIEW - 18 MAR 1982

I prepared the attached slide (mostly from your "Presentations For O.C. Review" documents) as a last minute exercise from Gordon. He used it to support his overview at the March 18 Operations Committee Woods. I will be happy to make corrections to the slide, for the record.

One observation - it is clear that groups do not present a consistent high level format of data information from which the attached slide could be derived. Please refer to the 32b data as a good example of a summary format which requires very little interpretation (page 21 - 32B Section POCR, copy attached).

EG:kr4.10

ENGINEERING DEVELOPMENT SUMMARY

PRODUCT	ENG $M Σ '83 -'85	NOR $B Σ'82 -'86	NOR $B LIFETIME
11/780, 11/750, 11/730	28.1	12.8	17.9
VENUS	42.4	1.8	10.2
NAUTILUS	23.8	.2	11.9
SCORPIO	22.0	.3	6.0
MICROVAX	13.0	?	?
VMS FAMILY SOFTWARE	95.5*	↑	↑
ALL 11'S TO 11/23+		4.0	4.5*
LCP 5, 8 (F-11 BASED)	3.3	.3	1.3*
ORION U, Q (J-11 BASED)	9.4	.4	2.4*
168 SOFTWARE	44.4	↑	↑
AZTEC I & II	17.2	1.4@	5.7
HSC & BSA CHANNELS/ADAPTORS	14.2	.3	.8
RA81, RAXX, RAXY (LARGE DISKS)	33.1	1.3	7.7
TA78, TU80, TU/TA81 (IND. TAPES)	4.2	1.2	2.5
SM. DIAM. DISKS (RX, RD)	9.6	1.3	1.8
SHRIMP (5 1/4" WINI)	5.4	-	3.0
MAYA (SM HI CAPACITY TAPE)	13.9	.1	3.3
RA60 (PINION & REMOVABLE DISK)	4.1	1.0	1.7
CT/CAT/DECMATE II	52.2	9.8*	?
TOTAL VIDEO FAMILY	26	1.8	4.2
TOTAL HARDCOPY	29.3	1.5	2.2
WORKSTATION (INCL. 32B, ETC.)	15.6	.6	1.6
U.Q BUS OPTIONS +1.4			
NI. ETHERNET HDW +3.9			
DECNET & X.25 SW +2.3			
SERVERS & GATEWAYS +3.0			
TOTAL DISTRIBUTED SYSTEMS	°75.2	↑?	↑?
36 BIT SYSTEMS PROGRAM	33.4	.7	1.6
CTAB/OFFICE +2.2			
TOTAL OFFICE PROGRAM	23.5	?	?
COEXISTANCE 20/VAX +1.0			
TOT. COEXIST., TOOLS, X-PROD. SW	8.5		
SEMICONDUCTOR PRODUCTS	31.7**		
SEG TOOLS & ADV DEV	19.7**		
PROCESS TECHNOLOGY	31.5		

NOTES:

? No estimate of revenue
↑ Included in systems revenue
@ Most of the disk revenue is included in the systems revenue
+ FY83 $M
* Eli Glazer estimate
o Includes all Non-Product Expenses
** Does not include manufacturing process engineering investment

INVESTMENT AND REVENUE IMPACT- 32-BIT ($M)

PRODUCT	FY82	FY83	FY84	FY85	REVENUE IMPACT FY82 TO FY86	REVENUE IMPACT LIFE-TIME
11/780 & ATLAS	4.3	3.5	4.8	4.6	5356	6606
11/750	2.5	4.0	2.6	2.1	4905	7070
11/730	2.6	3.3	2.6	.6	2486	4219
VENUS	11.8	15.3	16.4	10.7	1763	10171
SCORPIO	5.8	6.2	7.9	7.9	332	6107
SCORPIO BD					UNKNOWN	UNKNOWN
NAUTILUS	2.7	6.0	9.0	8.8	230	11873
HI-END WKS	2.1	.9	-	-	298	447
LO-END WKS	-	5.4	6.0	3.3	255	1159
MICROVAX	-	2.0	3.7	5.0	UNKNOWN	UNKNOWN
NEW PRODUCTS	-	-	-	15.0	UNKNOWN	UNKNOWN
NON-PRODUCT	7.7	11.5	14.2	18.0	-	-
TOTAL SCENARIO A	35.4	58.1	67.2	76.0	15625	47652

PRELIMINARY

****
* d i g i t a l *
****

TO: RICK CORBEN
GVPC:
PEG:
JACK SMITH

DATE: MON 11 JAN 1982 8:35 PM EST
FROM: GORDON BELL
DEPT: ENG STAFF
EXT: 223-2236
LOC/MAIL STOP: ML12-1/A51

SUBJECT: ENG. PROJECTS STRUCTURING (DRAFT), PLS COMMENT

Everyone has their own priorities and agenda for MOCW. I'd hope we can segment our thinking into various kinds of issues ranging from schedule slips of products we intend to introduce in May to strategic questions as to how we're going to compete with the Japanese 5th Generation systems.

Let's minimize the review of current projects simply to allow the people to continue to work "flatout". Status only reports.

There may be tactical, mid-course corrections to 1-3 year projects underway that we should deal with.

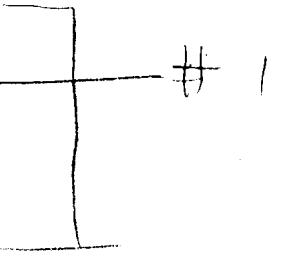
Finally, there are some very important decisions that will affect products over the next 10 years such as VAX physical interconnect. I believe the most important issue is our basic ability to design competitive (timely, cost-effective) products.

Here's my list, relatively prioritized, by category:

PROJECT STATUS AND UPDATES (0-2 years)
1. Local networking (NI, Pluto, gateways, broadband)
2. Large clusters (CI, 2080, HSC, 780, Atlas, HYDRA)
3. VT's (which one next?), LA, CT, Suvax, and LCP's for May
4. Nebula
5. J-11
6. Venus

TACTICAL CONCERNS (1-4 years)
1. Scorpio (project organization, process, CAD)
2. Nautilus (time to market versus product cost)
3. Low end mass storage and tapes
4. CTAB/OFIS and small OFIS CT

STRATEGIC OPPORTUNITIES (0-10 years) in priority
1. Engineering Capabilities to design and introduce products
   a. Designer skills for complex systems eg. Venus, Scorpio
   b. Semiconductor capability and effectiveness
   c. Competitive, timely engineering process for std. products
   d. CAD capability and effectiveness by site
   e. Physical interconnect evolution
   f. Packaging
2. VAX- vs Scorpio and J
3. VAX busses, packaging, options and PMS structures (eg. BI)
4. PC's and PCC's (Clusters of Personal Computers)
   a. Ethernet vs a standard HDLC multidrop for cluster I/C
   b. PCC software for CTAB, Ofis and servers



    c. PC servers for foreign PCs
    d. Competitiveness of 17+ bit, PDP-11 architecture
5. Lo end disk area make versus buy
6. Big VAX
7. Competitive Communication Components
8. Providing systems in a commodity hardware/software environment
9. 5th Generation computing

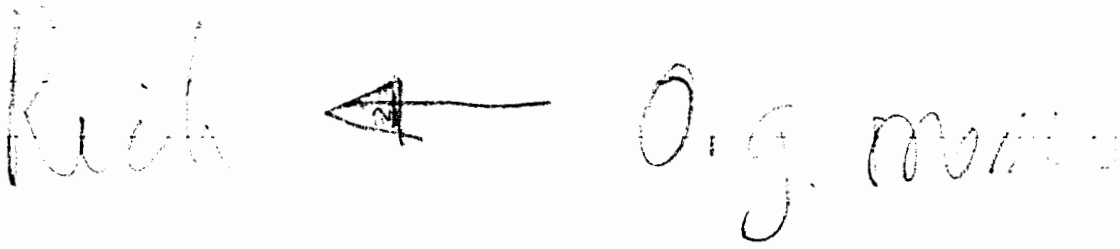
I'd sure like to make certain these issues do get addressed.

Could I get some feedback here as to completeness and priority?

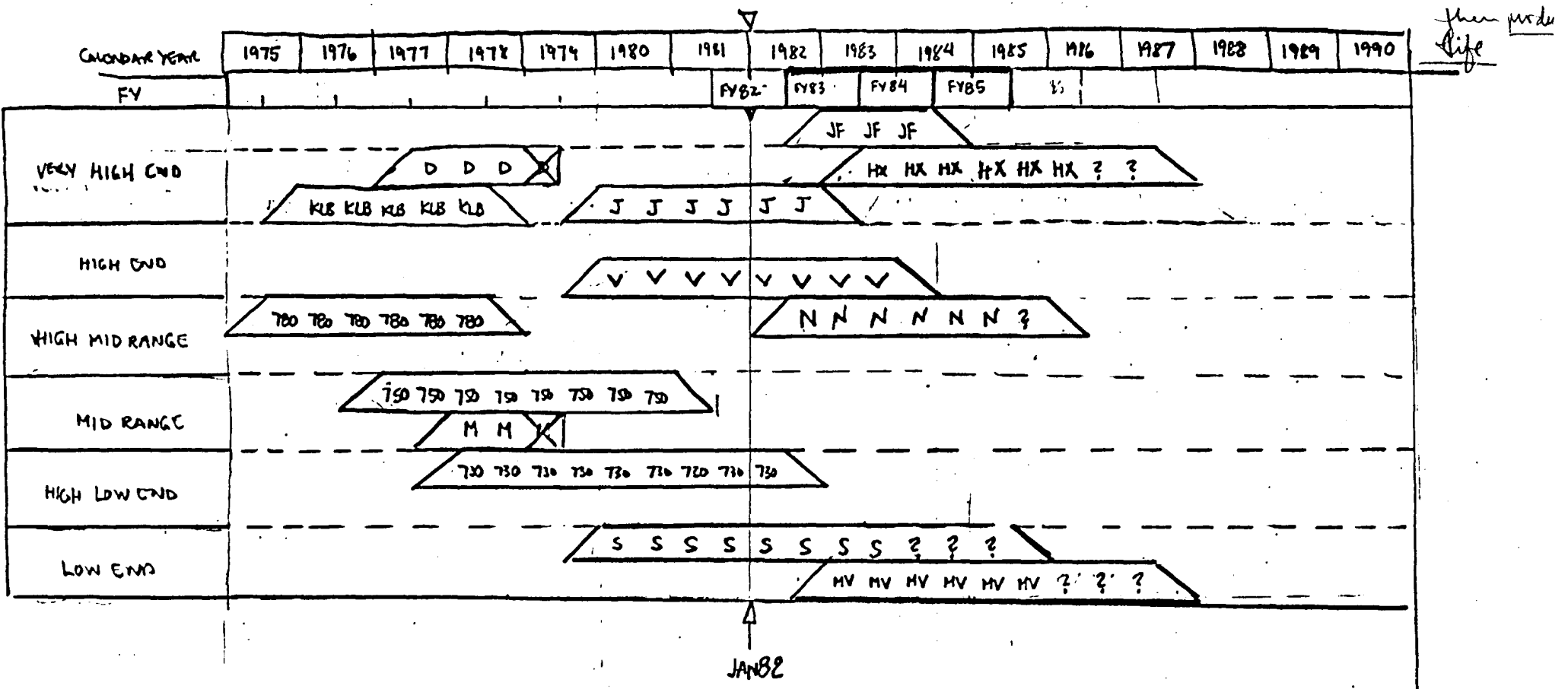
Comparision of Fundins

Category	May 76 (FY77)	March 82 (FY 82)
Development	55.9	50.4
next year	27.8	
year after	23.2	
>2 years	4.9	
Support	14.5	10.1
Product Management	4.6	2.9
Product total	75	63.4
Advanced Development	11.8	5.9
Research	?	1.4
Tools	6.6	4.7
Standards and architecture	5.1	2.2
A/D,research,tools, stds.	23.5	14.1
Process ensineerinns		.7
Manufacturins process		2.2
Finance		1.9
Personnel		1.8
Unallocated/contingency/space		5.3
Central Administration	1.7	
Group Adminstration		13.5 (seperated)

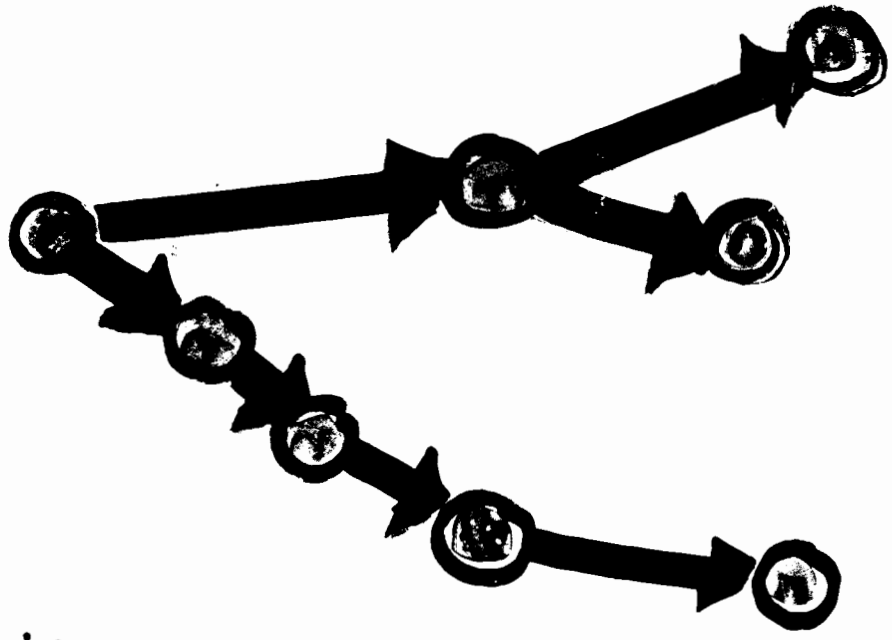
	Ay	780=1.0	$K			
2020	'77	0.7	200 - 300			
2040	'77	2.0	300 - 500		77-78	—
2060	'77	3.3	500 - 1200		79-80	—
SMP	'79	6.0	1200 - 1800		81-82	—
JUP	'83	16.0	500 - 1200		83-84	—
780	'79	1.0	200 - 400		85-86	—
750	'81	0.6	80 - 200			
730	'83	0.3	50 - 100			
VEN	'85	4.0	250 - 600			
NAV	'86	2.5	100 - 250		100	
SCO	'85	0.7	35 - 120		80 14 64 13 50 40 32 26 20 16	1 2 3 4 5 6 7 8
170	'76	0.5	80 - 120			
123	? '78	0.13	14 - 30	85		
144	'80	0.4	45 50 - 100	77 8		
124	'81	0.2	30 - 60			
123+	'82	0.2	16 - 45			
D-U	'85	0.6	35 - 80			
D-Q	'85	0.5	17 - 50			
L8	'84	0.2	15 - 20			
L5	'84	0.13	10 - 16			



" MUST START TO (MUST) FINISH "?



VAX
"NEWSTARTS"



1975 1980 1985

VAX

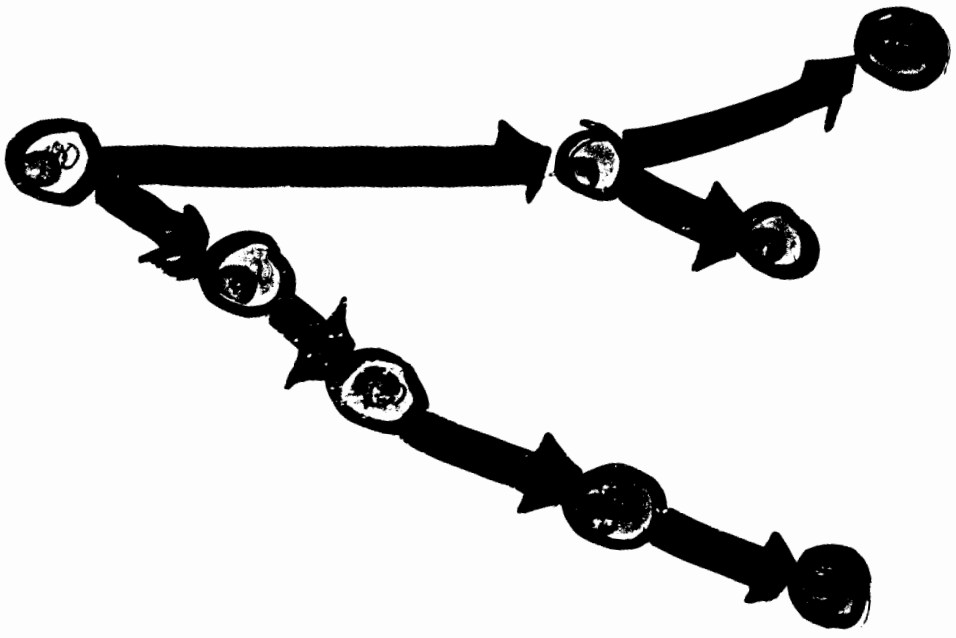
"NEW COMPLETES (RCS)"

1975

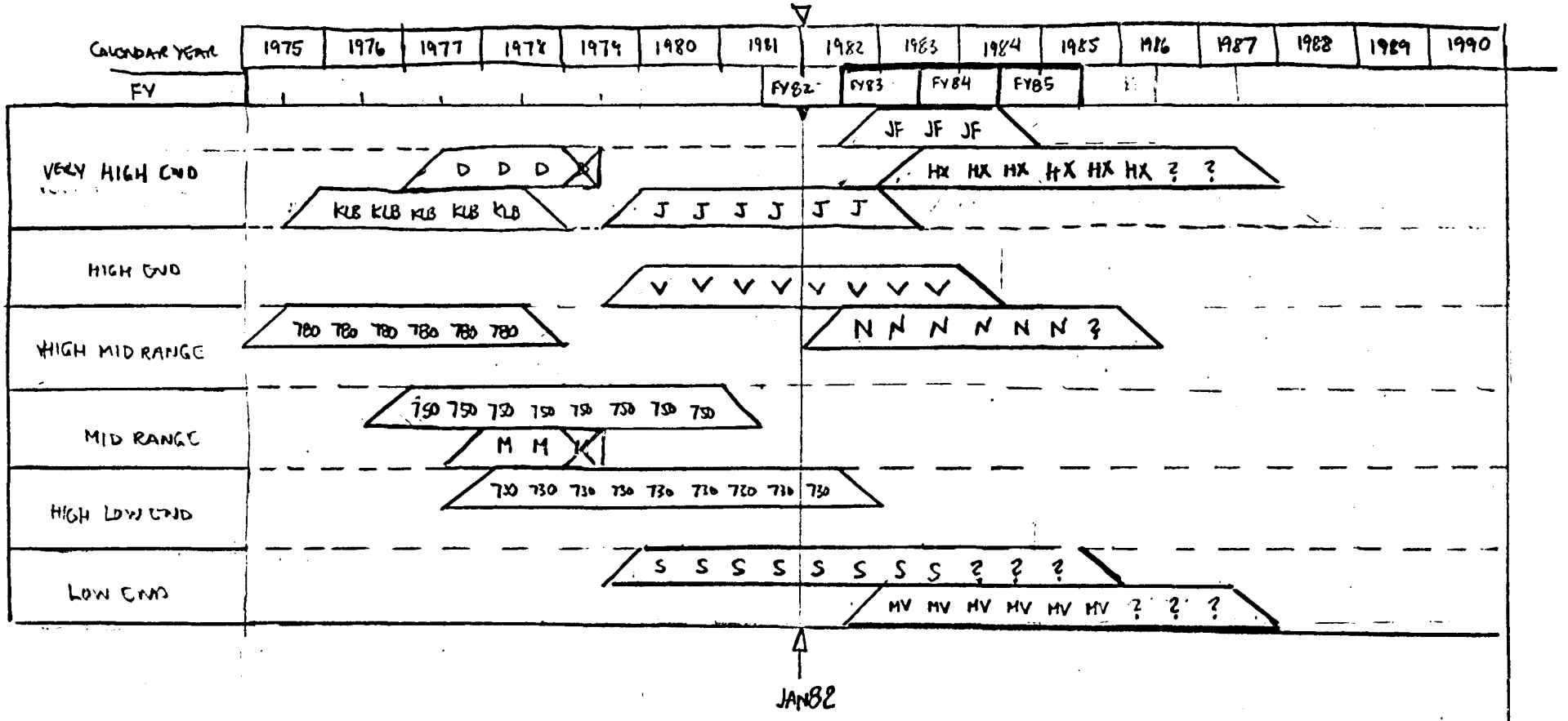
1980

1985

1990



" MUST START TO (MUST) FINISH "?



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* d i s i t a l *
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TO: see "TO" DISTRIBUTION

cc: ELI GLAZER
TGM STAFF:

DATE: FRI 19 FEB 1982 4:25 PM EST
FROM: DICK STRAUSS
DEPT: TECHNICAL GROUP
EXT: 231-7196
LOC/MAIL STOP: MR1-1/A65

SUBJECT: PART II TG RESPONSE TO ENGINEERING BASE PLAN (CON'T)

Software Engineering:

We well understand that only a few people can muck around in the internals of an operating system at once. How can we possibly expect to support in version 3B:

- 3 new CPUs (Scorpio, Nautilus, Venus)
- A new phase of DECnet (Phase IV including Ethernet)
- Security
- Mydra availability features
- Many new disks and tapes
- Workstations (SUVAX)
- CFIS
- Hopefully, some load sharing features

We have a real fear that in fact all this will not be done in time.

We see a lot of unmanaged overlap between CFIS, VAX MAIL, VAX Workstations, TPSS, and FMS that must be understood so we know what we are doing to our system interfaces for our users. We require a single, managed user interface strategy which is held to.

CI Cluster/Network Management is our highest priority need from V3B of VMS. Specifically, we need products to respond to the following requirements:

- Heterogeneous CPU's (not necessarily high availability)

- Cluster Management (including load balancing)

- Performance optimization tools

- User/system independence throughout cluster

We do not see a coherent strategy for servers (file, print, etc) on the CI and NI. This is a need we are already hearing from customers. Implicit in this will be a need for mass storage devices significantly larger than we are now planning.

The Basic Language must be modified to be in accord with the FIPS requirements.

We need commitments for CDD on Fortran, Pascal, and Ada.

We see insufficient need to justify spending on CATS and TPSS.

UNIX is not part of our strategy. Please stop the current ad hoc support by Engineering of the UNIX customer/computer science community. (We do not mean the TIG support function). The Engineering effort should be focused on putting UNIX features on VMS.

We have to reduce our spending on 16 bit operating systems. We must have a goal of eliminating Engineering expense for two of the four 16 bit operating systems in FY83, and eliminating expense for a third one in FY84.

DFIS:

We feel strongly that we will not have a positive productivity message for professionals in the version 1 product. We sell systems, not software, so we need a product that is excellent enough to sell another entire computer system. The other possibility is to create enough market pull to motivate our customers to buy DFIS software for their current system through A&SG or another distribution channel. DFIS V1 does not fulfill these requirements. Is it worth making DFIS V1 a valid saleable product by slipping its introduction date?

For Digital to announce an DFIS product without integrated graphics weakens our system integration message. What can be done to get graphics in V1?

The specific issues between the Technical Group and the DFIS program are well known and need not be reiterated here. The bottom line is the current product is aimed at the professional, manager, and secretary. It excels at none of these targets. Our first need is a product which excels at meeting the professional's needs.

Storage:

Our principle business throughout the 80's is projected to be networks of workstations and servers, and shared 32 bit CPU's. Aztec appears too bulky and expensive for the former, and too small for the latter. The Technical Group cannot justify an Aztec product.

We currently support taking a storage leadership position in the $50-400K system range, and buyouts above and below that. Therefore, we do not see the incremental benefit of building the RD52.

CT and Terminals:

We view CT initially as a professional workstation. At first release, the product lacks essential functionality in the software such as Fortran, Native Fire Basic, Word Processing, and Screen Graphics Operators. These specific concerns have been voiced previously.

In the terminal space, we feel that there is a significant demand from our customers for a full page of text with graphics. There is almost no demand for 1/2 page. Let's cancel the half page project and put all of our effort on full. Furthermore, we sell systems with terminals, and we have little demand for a terminal less expensive than the VT100.

Overall, the LA100 looks like an exciting product for integration of text and graphics. When will we have software to support it?

We need full Regis support on CT.

Remaining Summary Issues:

BEB - Could we decide not to do the BI and save the money set aside for chip development.

16 Bit - Orion without a floating point accelerator is a waste of time and money.

I thought we decided to only do a Unibus Orion last year at this time. That still appears to be a valid decision.

We see very limited need for the LCP products.

In the two years I have been involved in this process, I think Engineering has evolved to a point where their developments are a great deal closer to meeting our needs. The lines of communication are excellent, and Engineering now appears to have a fine management team.

By virtue of our orientations, there will always be a set of needs which will not be covered, and we will continue to bring them to light to assure we are doing the optimal things. Questioning from every point of view is the Digital way. Let's continue to keep the channels open, let's continue to question, and most of all, let's continue to win.

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* d i g i t a l *
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TVG

TO: RICK CORBEN

cc: TVG STAFF:
TVG-MSTAFF:

DATE: SUN 21 FEB 1982
FROM: LINDA SARLES
DEPT: TR
EXT: 223-3293
LOC/MAIL STOP: TP/TR

SUBJECT: CORRECTIONS TO TVG INPUTS TO ENG BASE PLAN

The TVG lists of concerns we generated were incorrectly communicated to you on Friday. Please use the following as our final input:

1. SCORPIO
   * What are we getting?
   * Are there enough funds to cover the proposal to Operations Committee?
   * Need FPA at FCS
   * Need PGA one year after FCS as previously agreed. Accelerate from FY87 to FY86
   * No BI modules funded (COMBO and LESI excluded)

2. J-11 (ORION)
   * FPA not funded - essential for the product

3. MICRO-VAX
   * Is the product adequately funded?

4. MULTI-PROCESSING and HIGH AVAILABILITY
   * Need capabilities beyond 11/750/780 and HSC-XX. These solutions are too expensive.
   * Inexpensive, simple HSC-XX needed
   * High availability NAL is desired
   * Multiprocessing is a requirement on the Q-Bus to capture new designs in the component marketplace. Multiprocessing being driven by TVG and ...; however, the 16-bit program office should be staffed to assure common architecture between boards and system Q-Bus products.

5. MASS STORAGE
   * UDA-52 should not be necessary
   * Separate RAXX from RAXY; then accelerate RAXX and drop RAXY (RA60 follow-on)
   * Accelerate MAYA to FY85 and take funds from RX-52 and YANKEE.
   * Do RD51 but don't do RD50
   * Put tape support back into the UDA

6. NEBULA
   * Short product life which we can't live with unless the following enhancements are added:
      1. IDC support of R81

1. Bisynch Support for the Combo board is required.

2. Need Pollux or KMS for increased SNA Gateway performance.

3. We must be able to connect large numbers of terminals to a VAX (500+). Neither Pluto or Pluto Jr. will allow this. Cost/performance issues for Pluto/Pluto Jr. must be resolved.

4. We would like to see more aggressive broadband development. We need to understand all the NI vs. broadband issues.

5. Network security is an important issue. Is the $34K in advanced development adequate to address this problem?

6. Don't do any further RSTS network development. This includes NI support and RSTS access to all gateways.

7. Remote DECNET for CT is required. Currently, only DECNET .. the NI is planned.

8. CT access to the SNA Gateway is required.

9. CX/EX is an important short term product. Support should be consolidated in one group.

10. A coordinated file server effort is required. Which group is responsible?

11. A T carrier interface to PBXs (including Siemens) is required. This will be a unique initial need and could solve the problem of connecting a large number of terminals connected to VAX.

12. We need bi-directional parallel between the SNA Gateway and ISN.

32-BIT SOFTWARE

1. CATS and FMS are diversing products. With CATS funded at $2M, is $800K necessary for FMS?

2. We should be investing in fourth generation languages by extending Datatrieve. All the proposals were in scenario B.

3. Development of a resource dictionary should be pursued. This is also a scenario B proposal.

4. We support Engineering's proposal for MFS (Multi-function system). This should provide a better user interface and integration. (DEC's answer to the IBM System 36.)

5. Shadowing is required for Massbus disks. Currently it is only available with HSC which is too expensive for some applications.

2. BBU for time-of-day clock for automatic restart
3. Testing of UDA-50 in CPU backplane
4. Documentation for public access to internal bus

7. SOFTWARE - MICRO PASCAL
   * Key 16 bit products for the 80's are RSX11-M+ and MicroPower/PASCAL. RT11 wil be phased out.
   * Need a multiuser development system for MicroPower/Pascal to insure its success.
   * Use RT-11 enhancements funding for the development of MicroPower/Pascal multiuser development system
   * Limit RT funding to RD/RX device support

OTHER CONCERNS

1. 11/782
   * What are future plans to improve this product?
   * Should have funding for 64K memory boards

2. ANE
   * Funding not obvious to keep ANE in sync with RSX-11M and to fix deficiencies

21-FEB-82 19:15:20 8 310? RCRD

MLOG MESSAGE ID: 0185138064

Comnl.

(*********)
* d i s i t o l *
(*********)

TO: RICH DORBERT

DATE: MON 22 FEB 1982 4:36 PM EST
FROM: GARY J ECKROTH
DEPT: COMM MKTG
EXT: 264-7956
LOC/MAIL STOP: MK1-2/N38

SUBJECT: POSITION STATEMENTS

Following are the issues that should be discussed at Thursday's PEG meeting. I will distribute this memo and the 0, 1, 2 ratings to CPLMC and Marcus' Staff. I am assuming that you are putting a package together for PEG members. These statements are the result of reviews with CPLMC and Marcus' Staff.

VAX-11 PROGRAM

1. We would like to see a single strong Engineering focus on high availability. High availability for Nebula is also needed.

2. We need to be able to connect large numbers (5000+) of terminals to a VAX system. There are no products to address this problem.

3. We are not comfortable with the current schedule. Will additional funding accelerate the schedule or is this too risky?

4. Joint Engineering/Manufacturing/Customer Services audits are a positive step and should receive more visibility.

5. The Program Office is thinking of pieces as opposed to systems. A greater systems approach is needed for budgeting and system planning.

STORAGE PROGRAM

1. Maya is too little too late. Yankee is also too far out. What are buyout alternatives?

2. Optical Disks appear to have considerable potential. A project should be funded from technology funds to investigate them.

3. Need a project to put Data Management software (RDMS) into the MSC.

4. Mini Aztec appears to be a better alternative to RDBI.

DISTRIBUTED SYSTEMS

6. Need distributed Datatrieve for CT.

7. Need full support for EPI. There seems to be some confusion as to whether the support is planned.

8. There is a need to support a large number of Videotex terminals on VAX.

16-BIT

1. Minimize funding for 16-bit products. Concentrate on new device support and maintenance. The exception is when enhancements are applicable to the CT.

OFIS PROGRAM

1. Two DECPLOTs are planned and unfunded. We need one to cover both DF and OFIS.

2. Better integration with VIA, Distributed Systems and CT is required. These products must be integrated.

3. OFIS on MSX-11M is not needed.

4. The OFIS software architecture should accomodate IBM in areas such as higher level document protocols.

5. There is a lack of planned on VAX Office Products. We need support for voice, image, print servers and integration with VAX Information Management. All of these are unfunded.

6. Wide carriage printer support is needed.

TERMINALS AND CONNECTIONS

1. Need PLP and CEPT Graphics.

2. Need funding to develop a print server.

3. Most DEC software only understands character mode terminals. There are no plans to support the intelligent block mode VT200.

4. Concern about the overlap of VT200 and CT25.

5. Need access from CT to the SNA Gateway.

6. Need IBM file/data interface software that is compatible with IBM's personal computer software when it is available.

7. A CT should be able to emulate a VT125 in order to run DECPLOT on VAX.

.(R&&&&&&&&&&&&&&&R)$
! d l s i t e r !
'&&&&&&&&&&&&&&&&&'

TO: see 'TC' DISTRIBUTION

cc: see 'IC' DISTRIBUTION

DATE: TUE 23 FEB 1988 9:47 PM EST
FROM: RICK CORSEN
DEPT: CORP PRODUCT MGMT
EXT: 223-3123
LOC/MAIL STOP: ML12-1/-T39

SUBJECT: MARKET GROUP SURVEY -- OVERVIEW

As a part of the process leading to the Engineering review at Operations Committee in March, a survey of four Market Groups was conducted. Each was asked to rate the business significance of Engineering projects on the following scale:

0 - No business significance
1 - Some business significance
2 - Substantial importance to business

In addition, each Market Group was invited to submit a summary of issues and concerns. All but the Small System Group elected to do so.

In order to provide rapid distribution, the results are being distributed as a set of file DVS manual

OVERVIEW
BUYER Info
TECH Env Info
TECH Volume
CAPITAL

Summary of Results (This Memo)
Detail Ratings by Project
Feasible Elaborations
Feasible Elaborations
Attribute Distribution

DSA ACCELERATION FY86 SOO 2 2 2 6

* because of EMS memo size restrictions, the explanation for the above asterisks had to transmitted as a part of the memo titled "MARKET GROUP SURVEY -- OVERVIEW".

/JOB
RC1,97,5

"TO" DISTRIBUTION:

ART CAMPBELL	MIKE GALLUP	ROSE ANN GIORDANO
SVPC:	MARCUS DIR REPTS:	BILL MORRISE
PEG:	JOEL SCHWARTZ	BRUCE STEWART
TECH. GROUP STAFF:	TVG STAFF:	

"CC" DISTRIBUTION:

GARY J ECKROTH	ENSPPC:	ELI GLINER
DICK RISLOVE	TIMC:	TVG-MSTAFF:

0 – No Bus
1 – moderate
2 – Necessary

****
* d i g i t a l *
****

TO: see 'TO' DISTRIBUTION

cc: see 'CC' DISTRIBUTION

DATE: TUE 23 FEB 1982 [illegible]:48 PM EST
FROM: RICK CORBEN
DEPT: CORP PRODUCT MGMT
EXT: 223-6123
LOC/MAIL STOP: ML12-1/-T39

SUBJECT: MARKET GROUP SURVEY -- SURVEY DATA

	FRS DATE	FY83 K $'S	T E U	T V G	C M G	S S G	S U M
16-BIT PROGRAM							
[illegible]ION V. 0	Q4FY84	4200	0	2	1	2	5
LCP-[illegible]	Q4/Q1FY83	1200	0	2	1	2	5
LCP-8	H1FY84	500	0	1	1	2	4
UNA (Q-BUS NI ADAPTOR)	Q4FY83	400	[illegible]	2	0*	1	[illegible]
RSTS ENHANCEMENTS		200	0	0	0	1	1
SUBSETS	Q2FY83					2	
SMALL BATCH AND UTILITIES	Q1FY84					2	
RSTS NI SUPPORT	H1FY84	200	0	0	0	1	1
RSTS NEW DEVICES		1100	0	0	1	2	3
RSX ENHANCEMENTS		900	[illegible]	1	0	2	[illegible]
PLACE M AND M+	[illegible]FY83					1	
ENHANCED BACKUP	Q1FY83					2	
RMS-11 PORTAL [illegible] USER SPACE	Q2FY84					1	
RSX NEW DEVICES		100	0	2	1	1	[illegible]
RT ENHANCEMENTS		300	0	0	0	1	1
EXTENDED MEMORY	Q4FY83					1	
NEW BACKUP	Q4FY83					1	
CUSTOMER INSTALLATION	Q4FY83					0	
RT NEW DEVICES		500	0	0	0	2	2
FORTRAN FULL ANSI-77	Q1FY84	300	1	1	1	0	3
COBOL-81 REPLACE COBOL-11	Q4FY83	300	0	0	1	1	2
BASIC-PLUS-2 TRACK STANDARDS	Q2FY84	300	1	1	1	1	4
[illegible]DMS-11 REWRITE	Q4FY83	100	0	2	0	1	3
FMS-11 REWRITE	Q3FY84	500	0	1	0	0	1
32-BIT PROGRAM							
11/780							
64K CHIP	Q2FY83	142	2	2	2	2	8
CI CLUSTERS/HI AVAILABILITY		800	2	1	2	0	5
COMMUNICATIONS SWITCH	FY83	330	2	0	2	1	5
11/750							
CI750	Q1FY84	1106	2	0	2	0	4
FP750	SHIPPED	84	2	2	1	0	5

PACKAGED SYSTEMS	FY83	201	2	2	2	2	8
UNA/LUA	?	200	2	2	1	1	6
DW750	04FY82	298	1	2	2	0	6
11/730							
CDM3C	04FY82	375	2	2	2	2	8
BATTERY BACKUP	03FY83	375	2	2	1	0	5
PACKAGED SYSTEMS	FY83	200	2	2	2	2	8
VENUS							
DEVELOPMENT	FY84	15300	2*	0	2	1	5
NAUTILUS							
DEVELOPMENT	FY85	6049	2*	2	2	2	8
SCORPIO							
DEVELOPMENT	FY85	6200	2*	2	2	2	8
WORKSTATION							
DEVELOPMENT							
- HIGH END SUNSET WORKSTATION	02FY83	700	2	2	1	0	5
- LOW END WORKSTATION	04FY83	5450	2	1	1	1	5
MICRO-VAX							
START-UP		1300	1	1	1	1	5
CHIP & BOARD SOFTWARE		1500	1	2	1	1	5
CLUSTER/NI AVAILABILITY (SUBSET PART OF 11/780 PROGRAM)							
II CLUSTERS	3rFY83				2	2	
NI AVAILABILITY	1QFY84				2	1	
64-BIT SOFTWARE							
VMS	FY82	5000	1	1	1	1	5
VAX11 RMS	FY83	1211	2	2	2	2	8
VAX11 PL/1		801	0	0	1	0	1
MACRO (WITH INTEGRITY)		5903	0	0	1	0	1
SMALL 32-BIT		1300	1	1	2	1	6
VAX11 FTL		890	2	1	2	2	7
VAX11 DEBUGGER		115	1	1	2	1	6
VAX11 SORT/MERGE	FY83	193	1	1	2	1	6
VAX11 EDITOR	FY83	158	1	2	2	2	8
VAX CROSS LAN TEST		90	2	1	2	0	5
VAX11 APL		332	2	0	1	0	3
VAX11 BASIC		890	2	1	2	2	7
VAX11 COBOL	FY82	980	1	0	2	2	5
VAX11 FORTRAN	FY82	413	2	2	1	1	6
VAX11 PASCAL V1.2		---					
VAX11 PASCAL V2.0	FY83	493	2	2	1	0	5
ADA	FY83	574	2	2	1	0	5
ADA PSE		332	2	2	1	0	5
DATS	FY83	2037	0	0	2	0	2
IPSP	FY83	2052	0	0	2	0	2
INS ARCHITECTURE		268	1	0	2	0	3
VAX11 DBMS	FY84	1352	1	0	2	1	4
LOOP32	2/83	425	2	0	1	1	4
RDMS-32	4Q83	1057	2	1	2	2	7

DTC/DSMF-32	FY83	759	2	1	2	2	7
Data/Task Mgmt		---			2		
VTC	FY82	---			1		
RMS-32		600	0	0	*	0	0

32-BIT PROGRAM

JUPITER SYSTEM

JUPITER HARDWARE (2020)	FY84	7075	1	0	0	0	1
JUPITER T20/COMM		1096	2	0	0	0	2
NI PLUTO		93	2	0	0	0	2
JUPITER HSC-50		119	2	0	0	0	2
JUPITER/20 COMM		576	2	0	0	0	2
JUPITER TOPS-10		0					

32-BIT SOFTWARE

APLEA	FY83	100	1	0	1	1	1
MACRO/RAL	FY83	50	1	0	0	0	1
FORTRAN-77	FY83	400	1	0	1	1	1

16-BIT GRAPHICS

DIGITAL PLOTTER SUPPORT		261	2	0	0	1	1
PLT29		197	1	0	0	*	1

16-BIT COMM SOFTWARE

DECNET-11 L.A.		75	2	1	0	0	1
X.29		80	2	1	0	0	2

TERMINALS & TRANSMITTING PRODUCTS

DT Series

DTC11	Q1FY83	6379	1	1	2	1	5
DTC05	Q1FY84	663	1	1	2	1	5
DT Software	Q1FY84	1874	2	1	2	2	7
DTKA (MI ADAPTOR FOR DT)		500	2	1	2	2	7

PRINTING

LA100RO	Q3FY83	800	2	1	1	2	6
LOW COST RO--BUYOUT	FY83	200	0	1	1	2	4
LOW COST RO--BUILD	FY85	1100	0	1	1	0	2
ELECTRONIC PRINTERS							
- EP1 (10-12 PPM)	Q2FY85	200	2	0	2	1	5
- EP3 (5-6 PPM)	FY86	700	2	0	2	0	4
KEYBOARDS (LA/VT/CT 200)		200	2	2	2	*	6

VIDEO

VT200-DX (LOW COST)	Q3FY83	1200	2	2	2	2	8
VT200-H (HALF-PAGE)	Q4FY83	2950	0	2	1	2*	5
VT200--FULL PAGE	Q1FY85	800	2	2	2	2	8
VT200 CUSTOM LSI	N/A	1100	2	2	1	1	6
VT200 SYSTEMS REF. MANUAL & PROGRAMMER'S MANUALS	N/A	150	2	2	1	1	6
VT200 INTERACTIVE I/O OPTIONS							

(LIGHT PEN/TABLET, ETC.)	N/A	235	2	2	1	1	6

OFIS PROGRAM

DECmail V1.1	Q1FY83	419	2	0	2	2	6
VAX/OFFICE R1	Q2FY83	1600	1	0	2	2	5
OFFICE/FRENCH	Q3FY83	100	1	0	1	2	4
OFFICE/GERMAN	Q3FY83	100	1	0	1	2	4
VAX/OFFICE R2	Q4FY83	---			2	2	
VAX/OFFICE R3	FY84	---			2	2	
RSX11M+/OFFICE R1	Q4FY83	200	0	0	0	2	2
CTAB/OFFICE R1	Q4FY83	2200	1	0	2	2	5
CTAB/OFFICE R2	FY84	---			2	2	
CTAB/OFFICE R3	FY84				2	2	

NOTE: Allocation of FY'83 spendins to specific releases is especially arbitrary in the case of OFIS.

DISTRIBUTED SYSTEM PRODUCTS

(Glossary of terms on p. 10 of Distributed Systems section in 'Presentstions to Operations Committee--March 1982")

LNIBUS OPTIONS							
HDLC SUPPORT IN LMP	H1FY84	250	1	1	1	0	3
DMZ32	H1FY84	PL FUNDED	1		2		
QBUS OPTIONS							
DZV-8	H1FY84	400	0	1	1	2	4
HDLC SUPPORT IN DMV	H1FY84	250	0	1	0	0	1
NI HARDWARE							
TRANSCEIVER	1/83	40	2	2	2	0	6
UNA	4/83	640	2	2	2	0	6
TRANSCEIVER POWER SUPPLY	H1FY84	100	1	1	1	0	3
PLUTO	?/83	1070	2	1	0*	0	3
LSI QNA	FY84	250	0	2	0	0	2
INTELLIGENT UNA	FY84	400	2	2	1	0	5
PLUTO JR.	H1FY85	600	2	1	0*	0	3
LNI	Q1FY84	300	2	2	2	0	6
BROADBAND TRANCEIVER	H2FY84	500	2	2	2	0	6

NOTE: MSI QNA is funded out of PSD.
CTNA is funded out of CT Program.

DECNET							
DECnet RSX (PIV & NI)	Q3FY84	422	1	2	1	2	6
DECnet VAX (PIV & NI)	Q4FY83	1200	2	2	2	2	8
DECnet E (PIV & NI)	H2FY84	500	0	0	0	2	2
X.25 (STANDALONE PSI PRODUCTS)							
VAX PSI	3/82	60	2	1	2	1	6
RSX PSI	3/83	100	1	1	1	1	4
SERVERS							
SERVER BASE	Q4FY83	568	2	1	0	1	5

ROUTER-	Q1FY84	283	2	1	2	1	6
X.25 GATEWAY	6/84	440	2	1	2	0	5
SNA GATEWAY(NON NI)	2/83	484	2	0	2	0	4
SNA GATEWAY(NI)	Q4FY84	460	2	0	2	0	4
TERMINAL CONC.	9/83	560	2	1	0*	0	3
XEROX GATEWAY	H2FY85	309	0	0	0	0	0

CROSS SYSTEM COEXISTENCE SOFTWARE

20/VAX COEX COMPUTERS		220	2	0	0	0	2
20/VAX DATA CONVERSION SUB		73	2	0	0	0	2
20/VAX DJU		293	2	0	0	0	2
20/VAX MSG TRANS SYST/NTS		219	2	0	0	0	2
20/VAX REMOTE FILE ACCESS		142	2	0	0	0	2
20/VAX REMOTE SPOOLING & BATCH		73	2	0	0	0	2
GRAPHICS		556	1	2	1	0	4

STORAGE SUBSYSTEM

HSC50	Q3FY83	2240	2	2	1	0	5
HSC70/71	Q2FY85	1125	2	2	2	2	8
HSC70	Q4FY83	1160	0	2	1	2	5
HSC50	Q4FY83	1170	1	1	2	2	7
HSC70	Q4FY83	720	1	1	2	2	7
HSC70	Q2FY85	1111	1	1	2	1	5
HSC70/71	7/84	1120	2	1	2	1	6
HSC70	Q3FY85	560	1	1	0	1	3
HSC70	Q4FY85	1120	1	1	0	1	3
HSC70	Q2FY84	1120	1	1	2	1	5
HSC70	Q3FY84	560	1	1	2	1	5
HSC70	Q2FY86	1120	1	1	2	1	5
HSC70	FY86	1120	1	2	0	2	5
HSC70	Q3FY85	720	0	1	1	2	4
HSC	Q4FY85 (WITH BACK)		2		2	2	6
HSC	FY87	560	1	1	0	1	3
HSC CACHE	Q4FY86	1120	2	0	2	1	5
HPIMP	FY87	?			1		
HSC (SI TO SI ADAPTER)	Q4FY87	0		2	2		
HSC	Q2FY85	2060	0	1	2	2	5
RX50/53	Q3FY85	600	0	2	1	2	5

ITEMS NOT IN BASE PLAN

VMS FPA		500	*	2	2	0	4
HIGH AVAILABILITY MODULA		?		2	2	0	4
RA70 (DEMAND BKG. FIRMDEL)				1	2	1	4
DECFLEX				0	2	1	3

SURVEY BACKGROUND INFORMATION

The survey list submitted to the Market Groups contained 142 Engineering products with deliverables. In general, R/D-funded projects, pure maintenance spending, ECO funding, FCC activities, contractual or legal commitments, advance development, tool/process development, research, and other non-product activities were excluded. The dollar figures for FY'93 were intended to give a rough feeling of project scale. The rules for allocating dollars to individual Engineering products are not consistent across the groups so precise comparisons should be avoided.

The sum of the ratings from each Market Group for a particular product gives a rough feeling for the business significance of that project. The values range from 0 to 8. Projects such as Scorpio, UMS; and RAE1 were rated 8 (a 2 from each of the four Market Groups). Two-thirds of all projects rated 4 or higher. Two received no support. The distribution of the "scores" was

0	1	2	3	4	5	6	7	8
11%	7%	16%	9%	9%	20%	19%	9%	11%

There are a few points to keep in mind in interpreting the results. The Lands Easter Group skirted through our survey net. Neither the JSS nor the T&T Market Groups analyzed their R/D in developing their rationale. By the time the problem was discovered it was too late to fix. Obviously, this caused lower ratings for Ba-Bit Program products and possibly for others such as the six 20/vAX Cross Section Maintenance products.

Items were also inconsistently used in the way each Market Group ranked projects. Some rated only products with normal programs in FY 93, but a few gave ratings even to products with zero programs. Also, some Groups were willing to rate components of a product, rather than discard the bunch. All the individual Market Group ratings are shown, but a 0 is counted only for those products which three or more Groups rated.

Finally, the Market Groups wanted to rate five areas which were not in Engineering's base plan. They are shown on the Survey Data documents but are not included in the table above.

THE LOWER RATED PROJECTS

0 Rating (No Support from any Market Group)

32-Bit Sys- FMS-32

Dist. Sys - Xerox Gateway

1 Rating (One Market Group Rates as 1 -- Some Significance)

16 Bit Sys- RSTS NI
RT Enhancements
FMS-11 Rewrite

32-Bit Sys- VAX-11 PL/I

Dist. Sys - HDLC for DMV

36-Bit Sys- Jupiter Hardware
APLSF
Macro/Link
FORTRAN V, 7
KLIPA

2 Rating (Two Market Groups Rate as 1 -- Some Significance)

16-Bit Sys- DOS11-P

Term & JO - Low-Cost RT--Build

3 Rating (Three Market Groups Rate as 1 -- Some Significance)

32-Bit Sys- FORTRAN Full ANSI

Libraries - Various

Dist. Sys - HDLC Support for DMP
Transceiver Power Sup.

4 Rating (Four Market Groups Rate as 1 -- Some Significance)

Utility for Users Front End

Disk Sys - DEC F11

5 Rating (One Market Group Rates as 1 -- Questionable Significance)

16-Bit Sys- RSTS Enhancements
RT Nav. Services

MP-Bit Sys- Macro (Interrupt)
DMA
TF68

32-Bit Sys - Peripheral Products
GPIB - ASR-11/23/GPIB
Dist. Sys - LSI DMA
Ethernet
Cross Sys - 8 Bit/16 Products

SURVEY DATA FOOTNOTES

Because of IMS memo size restrictions, the interpretation of the asterisks in the Survey Data is presented here.

16-BIT PROGRAM

OVERALL -- "The Commercial Group supports minimizing PDP-11 investments. One exception is where it carries over to the CT."

ORION -- "1" for Qbus Orion; "2" for Unibus (Small System Group)

QNA (QBUS NI ADAPTER) -- "QNA is not needed to connect to Qbus systems. The only possible need is if Engineering is building file servers, gateways out of Qbus systems." (Commercial Group)

32-BIT PROGRAM

[illegible]

[illegible]

[illegible] -- See Technical [illegible] (Corporate [illegible])

[illegible] -- "CATS and FMS-32 [illegible] ... [illegible] two products that are almost [illegible]." (Commercial Group)

[illegible]

[illegible] -- [illegible] field. Presumably, [illegible] support for the product [illegible] the [illegible], but no one from [illegible] to provide [illegible].

[illegible] -- "If [illegible] for VAX" (Small System Group)

DISTRIBUTED SYSTEMS

PLUTO
PLUTO, JR.
TERMINAL CONCENTRATOR -- "Pluto as a gateway is needed as a 2. Pluto as a terminal concentrator in its current implementation is a zero. Must be redefined to be useful." (Commercial Group)

ITEMS NOT IN BASE PLAN

J-11 FPA -- "Orion without a floating point accelerator is a waste of time and money." (Tech Eng User Group)

[illegible] DISTRIBUTION:

JAY CAMPBELL
SVPC:
PSD:
TECH. GROUP STAFF:

MIKE GALLUP
MARCUS DIR ACPTS:
JOEL SCHWARTZ
TVG STAFF:

ROSE ANN GIORDANO
BILL NORRIDE
BRUCE STEWART

CC: DISTRIBUTION:

JARY J ZOKROTH
DICK RISLOVE

ZMGPPC:
TGMC:

ELI GLAZER
TVG-ASTAFF:

The followins is offered as a summary of the Technical Group's issues with the Ensineerins Base Plan as presented in the March, 1982 "Presentation for Operations Committee Review".

Tech

Ensineerins Financial Overview:

The Technical Group has an issue with the 16 Bit Prosram allocation. Ensineerins spendins in FY82 for 16 bit products soes from 3.1% of 16 bit NOR with a 3 vear offset to 4.52% for FY84 spendins. This product should be milked as a cash cow, not increasinsly invested in.

The 32 bit expenditure in FY83 appears correct, however, srowth of only 15% to FY84 and a reduction of 18% to FY85 is outrasseous. This certainly does not relate properly to our revenue expectations. We see nearly a 100% srowth in 32 bit business per vear. What is a realistic three vear spendins plan?

There are questions as to whether our lons term business expectations are properly aligned with the rapidly increasing investment in storage. This must be more fully explored over the next vear.

32 Bit Investment:

The majority of VAX customers for the 1980's already own one VAX. Our customers are acutely aware of the lons term implication every time they buy a computer system. The investment the customer is makins in software, plus the applications he is busins are required to be safe over time. The familiarity the users accumulate with the system should have a lons term payoff. The customer expects us to allow him over time to: continue to distribute his system, increase his systems MIPS, and move users between systems with little or no disruption. The latter we can satisfy these expectations, the lonser the customer stays with Digital. Unfortunately, because of the presentation of the 32 bit strategy as projects and CPU's, and the same for storage, communications, and software, we have trouble feelins comfortable that our product direction is meetins the customer's lons term investment requirements.

There appears to be an overlap between Venus and Nautilus. Where we are talkins about $50-100 million develop projects, we have to be sure we have sufficient market for multiple products. It certainly appears two Nautilus attached tosether sive us sreater power than the Venus with less cost at about the same FCS. Although Venus will do better in

single large program execution, I doubt that market justifies the product. Can we get through the next 2 years without spending a total of $50 million on those two overlapping products? Time to market is the top priority in this space. Technical customers buy early in the life cycle of a product of this class because of their performance requirements.

We seem to be losing focus on the real time data [illegible] the real time needs of our laboratory, government, and other technical markets. What is the plan to move the real time customer onto our 32 bit products? Right now the product groups are focusing their development on this space.

We need high speed access to our 32 bit CPUs. We need a CI gateway to a high speed industry standard bus (like hyperchannel). Also, we need high bandwidth DMA access to 32 bit products in the 30-40 Mbytes/sec range.

When will we see a plan, and where is the funding for a Scorpio Based Workstation? What effort does the change in Scorpio strategy have on workstations? This product is a survival issue in the laboratory space.

Distributed Systems:

The Technical Group will not be able to sell local area networks the same way we have previously sold computers. We are going to have to understand the additional features and benefits we offer our customers with an Ethernet Network versus the traditional minicomputer with terminals. Announcing the Ethernet products nearly a year before availability makes us uncomfortable about properly presenting the products to our customers. We must figure out how we are going to package network offerings. How can Engineering help the product groups through this difficult transition?

Why do we continue to invest in Q Bus communication? Is there proper business justification? We don't see any.

"TO" DISTRIBUTION:

KICK CORBEN PEG: TECH. GROUP STAFF:
TGMC:

+------------+
d i g i t a l
+------------+

INTEROFFICE MEMORANDUM

TO: Participants in the PEG/GVPC Staff Meetings

DATE: 5 March 1982
FROM: Eli Glazer
DEPT: CORP. PRODUCT MGMT.
EXT: 3-4434
LOC/MAIL STOP: ML12B-T61

SUBJECT: ATTACHED DRAFT MINUTES

The following are DRAFT sets. Some preliminary review by members of the PEG organization has taken place. No one in the Market Groups has yet had a chance to review these minutes. Please communicate all corrections to me as soon as possible. I recommend all serious misinterpretations be clarified directly with GVPC.

I intend to issue a corrected set of minutes by approximately Friday, March 12th. If you need copies of referenced material, please call my office.

EG:kr4.5

DISTRIBUTION:

PEG:	Andy Knowles & Staff	Julius Marcus & Staff
W. MacKenzie & Staff	Win Hindle & Staff	Ted Johnson
Ron Smart	ENGPPC:	Joe Reilly

+------------+
d i g i t a l

INTEROFFICE MEMORANDUM

EG:kr3.46

TO: PEG: ENGPPC:

DATE: 2 March 1982
FROM: Eli Glazer
DEPT: CORP. PRODUCT MGMT.
EXT: 3-4434
LOC/MAIL STOP: ML12B-T61

SUBJECT: DRAFT OF PEG/GVPC COMML GRP MINUTES FEB 25 8:30-NOON

DRAFT PEG/COMML GRP MINUTES FEB 25 8:30-NOON

ATTENDEES: Bill Avery, P. Courtin, Gordon Bell, Bill Demmer, D. Fernald, Bill Johnson, M. Gutman, J. Marcus, B. Lacroute, G. Saviers, John Adams, Bob Flynn, Ted Johnson, Walt Hanstein, Don Harbner, Ray Mercier, E. Glazer, R. Corben, G. Eckroth, D. Rislove

ATTACHMENTS OR REFERENCE DOCUMENTS:

MARKET GROUP SURVEY FM CORBEN (FEB 23)
POSITION STATEMENTS FM EKROTH (FEB 22)
AGENDA

ACTION ITEMS:

WHO/WHEN	WHAT
1) Rislove	Comml definition of 500+ terminal application (i.e., MAIL, VIDIOTEX, TRANSACTIONS, etc.).
2) Eckroth	General RSTS End of Life Spec. Especially with respect to communications. To be worked with CONKLIN
3) Lacroute	Drive review of VTC and PLUTO overlap. Define performace objectives of PLUTO.
4) Rislove	RISLOVE to input Comm'l MKT Spec for LAN (Local Area Network) Protocols, Performace, Installation Issues. Data to be directed to LACROUTE
5) Lacroute/FRI. (2/26?)	Draft of Broadband, Baseband and Total LAN approach, Handbook due from task force (ADAMS, ROGERS, et al.).
6) Rislove	Aid LACROUTE in defining MKT Spec for LAN (i.e., Protocol, Response Times, Performance, etc.).

ACTION ITEMS:

WHO/WHEN	WHAT
7) Courtin/APR 15 (?)	Proposal on T-Carrier for PBX to company using outside vendor. LACROUTE and COURTIN will drive to resolution and follow
8) Saviers	SAVIERS and JOHNSON to each assign one person to see ~~that~~ shadowing ~~is~~ CAN be included in the microcode of the UDA.
9) Rislove	Communicate Comml's view of high productivity language tools
10) Fernald	Update the projection of 16Bit systems planned shipments for the Commercial Group.
11) B.JOHNSON/MAR 15 (?)	Converge the DECPLOT/GRAPHICS developments between the OFIS and Data MGT Development groups. Proposal due in several weeks. RILSOVE will monitor for Commercial Group.
12) Avery	Produce a roadmap (i.e., issue definition, goals, alternatives, etc.) for voice products.
13) Courtin	Provide AVERY with help in defining the mkt objectives involving Videotex applications
14) Avery	Resolve standard vs special keyboards
15) Rislove	Help AVERY in defining the spec for PLP and CEPT (Videotex Graphics Protocols). Represent Comml on VT125 Graphic Compatibility issues.
16) T.Johnson	Ask National Account Managers about need for compatiblity with IBM personal computers. What are the potential issues in their accounts?

The topics generally follow Gary Eckroth's February 22nd memo.

TOPIC	DISCUSSION
********** 32BIT PROGRAM **********	
High Availability in 32b Program	RISLOVE: Not a Tandem. COURTIN: Nebula on CI. LACROUTE: On the NI? DEMMER: Current program excludes a low-end high availability. SCA software should be utilizable at low end for consistancy. COURTIN: There is a multi market group task force considering the topic.

TOPIC	DISCUSSION
500+ Terminals to a VAX System	MARCUS: EMS, Videotex, Transaction Processing are all different. Don't care about a 500+ transactions processing. COURTIN: We limit ourselves to about 64 terminals on a VAX. LACROUTE, BELL: Factors are the number of users, duty cycle, active vs passive. Use of PLUTO type approach. COURTIN: Need to put PLP, Videotex protocols on the VT100 so that only one terminal needs to be on a desk (see ACTION ITEM 1).
Scorpio Schedule	COURTIN: 16b business is fading fast, we have a 32b low end problem. DEMMER: Chip cannot be accelerated. Systems could be accelerated by a quarter (3 months).
Joint Goals	ECKROTH: This part of the 32b program is a very positive step.
Program Office should increase systems approach	ECKROTH: Use approach of 16b Office interaction with P.G.'s as a model. O'KEEFE: We did not get response to incremental revenue questions (?).
Nebula Pricing and RSTS	MARCUS: With Nebula pricing we'll see RSTS - 16b systems go away. P.CONKLIN: How much should be invested in RSTS? MARCUS: Commercial will define what needs to be done to RSTS. We must keep customer commitments (see ACTION ITEM 2).

********** DISTRIBUTED SYSTEMS **********

Communications Concentration and Router	RISLOVE: Resolve overlap of VTC, PLUTO and 11/23 communications application. LACROUTE: PLUTO with 16 lines will transfer at $4.5K, with 32 lines at $6K. PLUTO is most effective with, forms, WPS, EMS ... for off loading CPU. Need to define PLUTO functionality (see ACTION ITEM 3). LACROUTE: I do not see the LCP-5 as a solution. CONKLIN: I'll monitor that from the stand point of the 16b program.
Bisynch on Combo board SNA gateway performance baseband and broadband	LACROUTE: Agreed but what do we give up to get it? ECKROTH: That is a function of performance. LACROUTE: We're working with OEMS to get a product as fast as possible 3M baud looks good, 10M baud is possible. A draft of the LAN (Local Area Network) handbook is due February 26. Engineering needs a marketing party line on customer needs and questions. MARCUS: Customers don't know what questions to ask (see ACTION ITEMS 4 and 5).

TOPIC	DISCUSSION
Network security	LACROUTE: Project plan is done and will be distributed. ADAMS: Access control applications software is being done in the Software Engineering Group.
Remote DECNET for CT	ADAMS: Should bw do a software DDCMP? MARCUS: How many protocols does DIGITAL need? I'd like direct SNA support within CT. LACROUTE: 3270 is what is needed. MARCUS: We need to define location of the machines and decide what are the best protocols. This has an impact on CT and OFIS. LACROUTE: Mail and file transfers are the applications being looked at. COURTIN: We know what the applications are what we don't know are the number of lines, performance, speed and response times. MARCUS: Customers are confused. Let's define 1)document protocol (e.g., SNA/3270); 2)wiring the building; 3)where are the files; 4)where are the editors; 5)security; 6)network functionality; 7)IBM interconnect; and 8) performance. LACROUTE: I'd drive this with commercial input from RISLOVE (see ACTION ITEMS 4, 5, and 6).
CX/DX focus	BJ: CX/DX belongs to the OFIS program.
Coordinate file servers effort	LACROUTE: LAN task force (STRECKER, TRAVIS, MILLER, ADAMS, ROGERS, LACROUTE, LAUCK, et. al.) will report in about one month.
T-Carrier to PBX's	LACROUTE & COURTIN: Northern Telecom joint proposal in 4 to 5 weeks (see ACTION ITEM 7).
Bidirectional SNA gateway and IBM	COURTIN: CI DECNET performance is poor. LACROUTE: The goal is to improve DECNET performance by a factor of 2.

********** SOFTWARE ENGINEERING **********

CAT and FMS are diverging	BJ: CATS is layered on FMS; they will converge.
Fourth Generation languages and resource dictionary	MARCUS: High productivity tools are needed. RISLOVE: Fourth generation language and DATATREIVE extensions are a higher priority than the resource dictionary but both are in Scenario B and not being proposed.
Multifunction (MFS) proposal DEC's answer to the IBM System 38	BJ(?): We'll be making a statement to the company.

TOPIC	DISCUSSION
Shadowing on MASSBUS disks	BJ and SAVIERS: Each of us will assign a person to see that shadowing is done in the microcode (see ACTION ITEM 8).
Distributed DATATREIVE for CT	MARCUS: Let's define it once and do it that way forever. BJ: A proposal is coming for distributed functionality with DATATREIVE and editing as examples.
EPI - "Electronic Printer software"	AVERY: Craig James, program manager, owns that. Definition and schedule are being developed.
Large number of VIDEOTEX terminals on VAX	BJ: Bruce Parker will demo next month in Spit Brook. AVERY: Do we have a party line for DEC involvement with VIDEOTEX? COURTIN: I'll help. We already have a lot of equipment involved with VIDEOTEX applications (see ACTION ITEM 13).
Goodness	MARCUS: We've got the best 32Bit hardware and software ... and networks with the most flexibility and best performance.

********** OFFICE SYSTEMS PROGRAM **********

Two DECPLOTS one for DP and one for OFIS	MARCUS: What is DEC going to offer graphics? AVERY: Terminal Software Strategy task force (STRECKER, et. al.) is two months from a report. They will cover the graphics objective. The task force deals with a terminals software strategy only (i.e., OS/terminal communication, etc.). MARCUS: DECPLOT could be a marketplace standard. BJ: Proposal is due in two weeks for how a single DECPLOT will be done (see ACTION ITEM 11).
VIA integration with Distributed Systems and CT	BJ: That's part of the terminals and terminals architecture issue.
OFIS on RSX-11M is not needed	No comments
OFIS should accomodate IBM high level document protocols	BJ: This is part of OFIS architecture. LACROUTE: Offer some software on the IBM machine as a special support service like the SNA service (being?) planned.
VOICE, IMAGE, PRINT SERVERS, etc	MARCUS: VOICE needs defining and a road map (e.g., digital analog, etc.). What will the product set be? AVERY: I'll do it (see

TOPIC	DISCUSSION
	ACTION ITEM 12).
Wide Carriage Support	MARCUS: The accountants produce spread sheets so big they call the bedsheets. We can't sell unless our software supports 158 to 212 characters/line. BJ: The Office program is looking into this.
********** STORAGE SYSTEMS **********	
MAYA, YANKEE	SAVIERS: MAYA is 100MB with the performance of a TU15. We're looking into pulling FRS into Q1FY85 from Q4FY85. The market is tape for the 5 1/2 form factor. MARCUS: What is the competition? alternatives? SAVIERS: Floppies in the near term. AZTEC is a better solution for LCP8. I am not comfortable with our 5 1/4 form factor products. We have no effort in the 3" form factor product category. ECKROTH: File servers will impact the need for 5 1/4 back up devices. GUTMAN: Volume back up versus file back up will resolve the issue. SAVIERS: We need a delivery mechanism for 10's of MBytes of software and training. MARCUS: We need long term solutions for the distribution problem.
Optical Disks	SAVIERS: Optical audio disks are a potential. We need an entreprenur to define the product. The high $ end is write once, the low end is replicated media. Customer services is doing an Industrial Interface to CT. A 4 Gigabyte write once optical disk is $40K to 60K sell price. Xerox wants to OEM a 1 Gigabyte disk for $5K cost. NOTE that an RA81 and TU81 can offer 1/2 GB at the same cost as a write once optical disk.
RDMS in HSC	SAVIERS: That's in advanced development. We're working with INTEL and universities for LSI versions of a solution.(?) We will propose an acceleration of the project.
Mini AZTEC vs RD52	SAVIERS: The next generation of 5 1/4 form factor needs more work on VLSI to work with 5 1/4 drives. MARCUS: Here the role of file servers needs to be defined.
********** TERMINALS AND WORKSTATIONS **********	
Special vs Standard keyboards	AVERY: One keyboard for all applications is a goal. MARCUS: Clerks will not buy complicated keyboards (see ACTION ITEMS 14).

TOPIC	DISCUSSION
PLP and CEPT graphics protocols	(See ACTION ITEMS 1 and 15).
Funding for a Print Server	LACROUTE: Isn't this a small system with some applications software. AVERY: Is there an application other than with clusters? RISLOVE: This is on shared printer as a resource in one office.
Block mode terminals	LACROUTE: DMP code has been changed to HDLC or SDLC. ECKROTH: What are systems going to do with block mode terminals? AVERY: We need a terminals software group. BJ: We are setting up a system to look at performance limitations of "servers."
Overlap of CT25 and VT200	BJ: The full spectrum of use of intelligent to dumb terminals needs to be defined. (?)Let's forget about intelligent terminals because in three years the CT will be cheap enough so that the intelligent terminal is not required. JOHNSON, AVERY, LACROUTE: Once you do block mode, then the basic dumb terminal must do it. Block mode as an option makes no sense. AVERY: A VT200 with 1/2 page graphics costs $900; without block mode it's $750 to $800. BJ: RISLOVE should talk to DAILY, LACAVA, and MCINTYRE about the terminal architecture.
Need for compatiblity with the IBM file/data personal computer software	AVERY: We could go third party as in SNA applications. T.JOHNSON: We could ask our National Account Managers about the penetration and compatibility need with IBM personal computers. MARCUS: The commercial customer base is dominated by IBM.
CT emulation of the VT125	AVERY: CT emulation of the VT125 is a product goal. MARCUS: Can we demonstrate that now? RISLOVE: I'll represent commercial needs with respect to VT125 needs.

********** 16B SYSTEMS **********

Commerical group requirements	MARCUS: Let's define exactly what the 16B requirement is for the Commercial Group (see ACTION ITEM 10). GUTMAN: We're prepared to build 300 to 400 11/70 systems for customer availability after

TOPIC DISCUSSION

October 83 (next key FCC cutoff date).

********** GENERAL **********

MARCUS: Is the chip investment right?
MARCUS: Office pieces must be discussed. ULYSSUS may have been overlooked but is needed to make OFIS work.

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INTEROFFICE MEMORANDUM

TO: PEG: ENGPPC:

EG:kr4.2
DATE: 3 March 1982
FROM: Eli Glazer
DEPT: CORP. PRODUCT MGMT.
EXT: 3-4434
LOC/MAIL STOP: ML12B-T61

SUBJECT: DRAFT OF PEG/TECH END USER GRP MINUTES 25 FEB 1-5PM

DRAFT PEG/TECH END USER GRP MINUTES FEB 25 1:00-5:00PM

ATTENDEES: Bill Avery, Win Hindle, Bernie Lacroute, Grant Saviers, Rick Corben, Don Harbner, Herb Shanzer, Walt Hanstein, Mary Altenhof, Ray Mercier, Dick Strauss, John Buckley, Harvey Weiss, Bill Long, Bill Demmer, John O'Keefe, Bob Trocci, Mike Gutman, Ulf Fagerquist, Eli Glazer, Cecilia d'Oliveira, John Adams, Bob Flynn, Bill Johnson, Ted Johnson, and Ed Schmidt.

ATTACHMENTS OR REFERENCE DOCUMENTS:

MARKET GROUP SURVEY FM CORBEN (FEB 23)
TG RESPONSE TO ENGINEERING BASE PLAN (FEB 19)
AGENDA

ACTION ITEMS:

WHO/WHEN	WHAT
1) John O'Keefe	DR780 COST ISSUE (?) Report by Kurt Friedrich on I/O performance of VMS
2) Bill Johnson	I/O, real time performance studies to be distributed - will come out in Sales Update
3) Bernie Lacroute	The standards for an interface to NI will be published (?)
4) Bill Johnson	MARY ALTENHOF to document concerns about V3A and TREVOR will get back
5) Harvey Weiss	Will see that a Technical Group character set is defined
6) Mike Gutman	Will review 0 and 1 voted items to test impact on budget
7) Bill Avery	Will get help from Technical Group on the specification for a CT Tech Workstation

TOPIC	DISCUSSION

The topics in the first part of the minutes generally follow Dick Strauss' memo of February 19.

********** 32BIT PROGRAM **********

Dual Nautilus vs Venus product overlap	FAGERQUIST: Design simulation of Venus shows a 4.2 to 4.4 times VAX11/780 performance which is better than expected. We are still looking at a dual Nautilus. STRAUSS: The performance data on a dual Nautilus and Venus are needed to fine tune the Technical Group's decision on Venus.
32b Real Time hardware and software	O'KEEFE: The DR780 cost is continuing to be worked. Kurt Friedrich will report on the overall speed/performance of this option. DEMMER: NEBULA is comparable to an 11/44 for hardware and software I/O performance. HINDLE: What is the real time band width requirement? B.JOHNSON: There's nothing inherent in VAX/VMS software that prevents good response time. We will distribute studies of the VAX/VMS I/O performance. HINDLE: Is there anything in the B & C scenarios for high speed I/O on 32b systems? GUTMAN: We're doing an advanced development J-11 front end study. O'KEEFE: We took lack of response from the Market Groups on the DR750H as a reason to cut back on it's development.
Scorpio Workstation	O'KEEFE: FY84 and FY85 systems allocations seem smaller because we are working on FY83 budget problem. There will be more Scoprio product projects in 84 and 85. DEMMER: We need input on the Scorpio 85 type workstation.

********** DISTRIBUTED SYSTEMS **********

How to sell LAN (local area network)	LACROUTE: We are working with the service ogranizations to deliver a proposal shortly.
Limit Q-BUS communi-cations options	GUTMAN and LACROUTE: The Technical Volume Group and Small Systems Group requires the product.
Consistent NI	(See ACTION ITEM 3). B.JOHNSON: What operating systems should support NI? STRAUSS: VMS, CT, RSX (Unibus).

TOPIC	DISCUSSION
********** SOFTWARE ENGINEERING **********	
When V3B VMS	B.JOHNSON: June 83. 12 months after V3A. ALTENHOF: RDMS support in V3B (see ACTION ITEM 4).
Manage the User interface	B.JOHNSON: One type of universal interface is not suitable for all types of users. STRAUSS: TPSS menu vs Commercial is inconsistent (?).
CI/CLUSTER Management	DEMMER: Recognize need for heterogenious cluster support including load balancing, but I'm not sure when. (B.JOHNSON: Needs to communicate CI/CLUSTER management objectives.)
Server Strategy	LACROUTE: I am chairing the task force to define the server architecture and components etc. We're several months away. The first specification will be for a VMS or RSX via DECnet and NI (?).
FIPS BASIC, common data dictionary (CCD) for FORTRAN, PASCAL, and ADA	B.JOHNSON: I need to get my engineers inputs.
NO CATS or TPSS	No comment
NO AD HOC UNIX support	B.JOHNSON: Engineers answering questions are supporting TIG. GUTMAN: The UNIX engineering task force will come to a party line recommendation in about 30 days.
Cut 16b O.S. support from CE budget	STRAUSS: Get down to RSX and MICROPASCAL. GUTMAN: The issue is: how agressive should phase out timing be? The Technical Group 16b systems business is $167M in FY82 and $153M in FY84. JOHNSON and GUTMAN: We are working the software support, after warranty, engineering support cost with the service organization.
********** STORAGE SYSTEMS **********	
AZTEC	STRAUSS: The Technical Group is not profitable in the $20K to 50K sell price range except for multiple systems. WEISS: GSG did not vote 'no' for AZTEC.

TOPIC	DISCUSSION
Develop for $50K-400K system range. Buy out elsewhere	SAVIERS: We're competitive with the IBM 3380 with multiple RA81's on a cost per megabyte and on a megabyte per cu. ft. GUTMAN: We need to communicate the multiple RA81 competitiveness. WEISS: Did not realize we were that competitive. SAVIERS: Are FIP's I/O standards a problem with government sales? WEISS: No, because we're a volume contract supplier, we are an exception.
********** CT and TERMINALS **********	
First release of CT doesn't have Technical Workstation function-ality	AVERY: Need help with definition (see ACTION ITEM 7).
Full Page sooner no Half Page	AVERY: Are you sure with respect to Europe? Cost will go up by a factor of 2 (?). STRAUSS: Customers will pay the higher price for Full Page. AVERY: Please test with your customers. WEISS: Why the cost difference? AVERY: Half Page is off the shelf technology components. Full Page components are very expensive. We've looked at buyouts as well. STRAUSS: Terminals software. B.JOHNSON: AVERY and I are working the architecture (for Full Page?). AVERY: The issues of higher functionality include graphics, character types, multiple windows, etc., which cannot be done on a 12 inch monitor.
LA100 Support	STRAUSS: We need mixed graphics and text utility software.
REGIS support on CT	STRAUSS: The problem is you cannot run the CT as a standalone and as a REGIS graphics device. VT125 emulation is not enough. BILL WISE will work with AVERY and JOHNSON. AVERY: I've got to understand the multiple use issue.
Low cost RO	HINDLE: Doesn't seem to be supported by the product groups as an engineering project. AVERY: The technology is needed in-house for high volume manufacturing issues.
********** REMAINING ISSUES **********	
BI Chips	SAVIERS: Is there a need for high BW I/O?

TOPIC	DISCUSSION
	STRAUSS: We need fast I/O in the 20MHz to 30MHz bandwidth range to do satelite data aquisition, particle physics and graphics. WEISS: We used to be leader with VAX and don't want to lose the market. DEMMER: The BI is basic to the Scorpio structure. It is the board interface of the future and the bus structure for future systems. HINDLE: We need a Technical Group task force to define the real time need (ACTION ITEM for STRAUSS?).
ORION without FPP is a waste	GUTMAN: Agreed, it's a $1.5M budget problem.

********** OFFICE SYSTEMS **********

Not enough features for the Technical Market	STEWART: Charlotte flow control permits integrating tools for the professional. We're working on getting graphics into Version 1. WEISS: Can we integrate Graphics and Text?
Integrated graphics and text in OFIS is needed	STEWART: We have a Graphics and Text print-out capability now. Use of the dictionary is not optimum now. Who can I interface with in the Technical Group for details? (STRAUSS for follow-up?) JOHNSON: OFIS on RSX? STRAUSS: No. WEISS: Need to research the value of OFIS on RSX. STEWART: Last year the Tech End User Group said no to a technical character set in WPS. HINDLE: Let's get it defined now (see ACTION ITEM 5).

********** GENERAL - CANDIDATES FOR CUTBACK **********

STRAUSS: Here's my FY83 cut recommendations - $26M+

TECHNICAL GROUP	FY83 $M
Cut 16b spending to 3.1% of NOR in FY86	9.0
Do NO CATS, TPSS, NOR TMS	5.4
NO RX52, 53 or RD52	2.7
No Half Page	2.95
Stop PL/1	.6
No XRX Gateway	.3
No LO Cost RO	1.3
No BI Chips	1.0
No HYDRA	3.0
No OFIS for secretary or manager	
Stop VENUS/NEBULA overlap	---
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TOPIC	DISCUSSION
	Approximately $ 26.0M
16B Issues	GUTMAN: What the TG needs to do is tell us is how you rate high priority items (marked 2), so we can compare with other Market Groups. HINDLE: Mike can you review the "1" votes to see if cuts are possible? GUTMAN: I'm doing that. WEISS: Should be offer RSX-11 at $50 a copy with the F-11 chip set just as we're doing with RT-11 on the T-11 chip. GUTMAN: Being worked with LLOYD FUGATE.
HYDRA	HINDLE: What about the status of HYDRA? O'KEEFE: The HYDRA budget also includes Cluster management and load balancing. HINDLE: The 32b program needs to educate the company on this. CATS and TPSS were not supported well by the survey.
********** COMMENTS FROM THE PRODUCT GROUPS **********	
	HINDLE: I'd like each P.G. manager to summarize his views.
LDP	LONG: Our future is in the Real Time area. There is no follow on to MINC and no low-end front end. Data collection must be fast enough. Instruments on the laboratory bench must connect to the computer. GUTMAN: A front end-11 might be the answer. LONG: Regarding OFIS, 40% of our sales are in the corporate labs and 60% in universities. They tend to be associated with defined tasks.
ECS	TROCCI: Text and integrated graphics beyond graphics and WPS is a key need. Schools need baseband and/or broad band local connections. We also need a common single terminal user interface to avoid need to retrain on new DEC products.
ESG	ABBOTT GILMAN: We cannot sell less than $50K transactions profitably. AVERY: We need to write down the Tech Workstation need (see ACTION ITEM 7).
	SAVIERS: Uncomfortable about the $50K boundry. HINDLE: That's an organizational SSG charter type issue. If it's wrong, we'll change it. We can sell multiples profitably.

TOPIC	DISCUSSION
	B.JOHNSON: Your customers are the technology gate keepers. We often learn alot from their feedback. We may not get this via SSG. SAVIERS: and LACROUTE: The Tech Group often sells the seed products that lead to future success.
GSG	WEISS: We aim at being the best supplier of SECURE, DISTRIBUTED, DATA MANAGEMENT systems. We are leaders in communications, interconnect, networking hardware and software. We need to retain leadership in relational database management with the right hardware for large databases and heirarchical storage. Concerns are with communications, networking, multiprocessing.
The LAN issue	We're not going fast enough in delivery of the ETHERNET product. GUTMAN: Can we buy LAN hardware? WEISS: MITERNET is running; we may have to support that before ETHERNET. BYU and LRL have integrated WPS and graphics. We must still pay attention to the technologists (?).
	B.JOHNSON: What about the knowledge BASED Systems - specifically LISP, INTERLISP?
MSG	ALTENHOF: Our presence in the departments is with distributed systems. We must use our networking strength. Hospitals are behind the times. ETHERNET can help solve their problems. CT is a product for the HOSPITAL. We must build systems not pieces. Medical is losing to TANDEM.
COMPETITION	HINDLE: Can we identify the competition? SAVIERS: We're ok with components. Systems are a problem. TROCCI: Australia has been a test bed for Japan.
STABILITY	JOHNSON: Last year we made changes three months after we closed on the engineering budget. Can we live with our decisions? CORBEN: When the PEG managers know the Product Group business models, they can do a better job at trade-off's.
	GUTMAN: On a scale of 1 to 10, how do you feel about your knowledge of the engineering plan? HINDLE: I feel 10 now, but it decays rapidly. GUTMAN: I feel a 2 on the P.G. business models.

TOPIC	DISCUSSION
	GENERAL: We need to get together to do this kind of PEG - MKT GROUP exchange.

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INTEROFFICE MEMORANDUM

EG:kr4.3
TO: PEG: ENGPPC:
DATE: 3 March 1982
FROM: Eli Glazer
DEPT: CORP. PRODUCT MGMT.
EXT: 3-4434
LOC/MAIL STOP: ML12B-T61

SUBJECT: DRAFT OF PEG/TECH VOL GRP MINUTES 26 FEB 1-5PM

DRAFT PEG/TECH VOL GRP MINUTES FEB 26 1:00-5:00PM

ATTENDEES: Bill Avery, Bill Demmer, Bill Johnson, Jack MacKeen, Don Harbert, John Adams, Bob Flynn, Steve Midel, Lloyd Fugate, Roy Moffa, Hannes Reiter, Herb Shanzer, Cecilia d'Oliveira, Walt Hanstein, Linda Sarles, Ward MacKenzie, Mike Gutman, Graham (for Bruce Osterling), Rick Corben, Eli Glazer

ATTACHMENTS OR REFERENCE DOCUMENTS:

MARKET GROUP SURVEY FM CORBEN (FEB 23)
TVG RESPONSE TO ENGINEERING BASE PLAN FM L. SARLES (FEB 21)
Slide Presentation Set - presented at meeting.

ACTION ITEMS:

WHO/WHEN	WHAT
1) Linda Sarles	Write down what is exactly meant by bus, software cultural etc compatibility in the TVG world.
2) Steve Midel	Market requirement documents from TOEM will be distributed this week.
3) Hannes Reiter	Better definition of need for a two 5 1/4 inch boxes versus a 10 1/2 box with lot of expansion.
4) Herb Shanzer	Review the need for RX based 11/23 PLUS type systems.
5) Linda Sarles	Continue to work on high availability task force (using Nebula's not on CI).

GENERAL DISCUSSION ON THE MEETING FORMAT

Ward opened the meeting with a general discussion of the business model of TVG using slides referenced above. Linda Sarles, Hannes Reiter and Lloyd Fugate followed with a discussion of the three TVG

TOPIC	DISCUSSION

Reiter and Lloyd Fugate followed with a discussion of the three TVG market segments, 32B, 16B and MICROS. There was a spirited dialog during the entire presentation between the presenter, his or her market group colleagues and the PEG managers present. Ward and Linda closed the meeting by reviewing the TVG feedback to the proposed engineering plan. the minutes that follow represent extracts from the discussion during the meeting.

TOPIC	DISCUSSION
Compatibility	ADAMS: How many cutomers use AME mode (VMS utility for RSX-11 compatibility)? SARLES: Don't know, but it gets us in the door. ADAMS: Priviledged code? SARLES: A lot! GUTMAN: What do you mean by compatibility? SARLES: Architecture, busses, instruction set, etc. JOHNSON: What leverage do we have in moving customers from 11's to VAX? Languages, Tools? At what level are the compatibility requirements? MIDEL: Cultural as well (see ACTION ITEMS 1 and 2). SARLES: Customers want to be vendor independent. JOHNSON: Give them two languages and their locked in.
UNIX and C	GUTMAN: What about UNIX and C? SARLES: Customers want to see a full C with UNIX compatibility. They say do it all or its not worth it.
32bit competition and 16bit to 32bit migration	SARLES: PERKIN ELMER leads, then INTEL and MOTOROLA with 32bit chips. Even box and board customers are looking at non-DEC chip alternatives because we do not have low-end 32b alternatives. (The company strategy was to build the high end VAX first which made us vulnerable at the low end 32bit market.)
32bit and 16bit TVG volumes (pg 26-28)	GUTMAN: Let's be sure we don't triple count. The risk is we end up with a low volume ORION U or Q or 32b product. SHANZER: I need input on 5 1/4 inch box versus 10 1/2 box would kill need for a 5 1/4 inch expansion box. GUTMAN: Is there a need for an RA81 ORION? WARD and FUGATE: That's a 3% to 5% need. REITER: 20% of our 11/34's still use RL01's.
MICROS Market Model	FUGATE: INTEL created and encouraged

TOPIC	DISCUSSION
	standardization and second sourcing on their design, to grow rapidly. DEC kept it designs and architecture proprietary. The make or buy decisions are unique to each volume customer and depend on the kind of engineering resources owned by the customer. A wide range. SHANZER: Need to review the need for RX based 16b systems. FUGATE: Yes. GUTMAN: Does MICROPOWER need communications software support? FUGATE: Our customers do their own. MICROPOWER is for dedicated real time run time use. Customers need to optimize their investment in engineering, training, experience and tools. JOHNSON: If we had the MICROVAX development tools in place, we could lock in some DEC 32b "design ins."
**** GENERAL DISCUSSION ... REFER TO LINDA SARLES FEB 21 MEMO ****	
CT	AVERY: Why isn't TVG selling CT's? MACKENZIE: It doesn't fit the TVG market model. It is interesting that one of TVG OEM's, ADEX(?) went to the use of an Apple for an application. MIDEL: Customers might want to develop software added value and ask for drop shipment of the CT. MACKENZIE: CT's will be sold by SSG.
DECnet	ADAMS: Will DECnet become more important to our OEM customers? MACKENZIE: Yes, over time ETHERNET will become more adaptable to OEM networks.
High Availability	SARLES: I am working with COURTIN on high availability including need for shadowing. SAVIERS: BJ and I are each supporting the examinations of the UDA to see if shadowing can be added and supported in the operating systems (see ACTION ITEM 5). MACKENZIE: Remember that CSS and TVG customers are already using multiprocessor - high availability type configurations. (The need has been established in the DEC OEM customer base.) SARLES: A key would be a dual port disk. REITER: There is a proposal for a package developed in Europe, for a high availability software package. The cost is $200K. JOHNSON: Sound like a real bargin if it works.
FPA on Scorpio and ORION (J-11)	MACKENZIE: J-11 and Scorpi are useless in our market without FPA. DEMMER: I

TOPIC	DISCUSSION
	understand we are resource limited in the Semiconductor Engineering area. GUTMAN: I own the J-11 FPA issue. It is not in our A scenario. MACKENZIE: I'll get on my soapbox! If the corporation makes TVG pay for it, we're just sweeping it under the rug one more year. The corporation should view this as a strategic corporate wide decision.
MICROPOWER	GUTMAN: Not in scenario A. FUGATE: It's clearly a tool to keep customers in the DEC family and especially with PDP-11's.

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INTEROFFICE MEMORANDUM

EG:kr4.4
TO: PEG: ENGPPC:
DATE: 4 March 1982
FROM: Eli Glazer
DEPT: CORP. PRODUCT MGMT.
EXT: 3-4434
LOC/MAIL STOP: ML12B-T61

SUBJECT: DRAFT OF PEG/SM SYS GRP MEETING MINUTES 3 MAR 8:30-NOON

DRAFT OF PEG/SM SYS GRP MEETING MINUTES 3 MAR 8:30 - NOON

ATTENDEES: Andy Knowles, Mike Gallup, Joel Schwartz, Rick Corben, Bill Johnson, Bill Demmer, Bill Avery, John O'Keefe, Barry Folsom, Dick Loveland, Mike Gutman, Peter Conklin, Bob Flynn, Bernie Lacroute, John Adams, Don Harbert, Walt Hanstein, Bruce Anderson, Cecilia d'Oliveira, Jerry Hornik, Larry Portner, Bruce Stewart, Eli Glazer.

REFERENCE MATERIAL:

MARKET SURVEY MEMO FM R. CORBEN (23 FEB)

ACTION ITEMS:

WHO/WHEN	TOPIC
1) Mike Gutman	PDP-11 software strategy for each O.S. is being written down. Get a better set of definitions to SSG for evaluation of Market Survey inputs.
2) M. Gallup/Avery(?)	Get Market Survey data on the 16b program issues back to GUTMAN.
3) Bernie Lacroute March 3	The decision is now not to put DECnet Version 4 on RSTS!
4) Bob Flynn	The Storage program has cut YANKEE from it's plan, so as to accelerate MAYA.
5) Bill Johnson	I will look at a development system using C on VMS as a tool for the low-end. To get input from SCHWARTZ on the software requirement for SSG.
6) Bill Avery	Will work with LACROUTE to define the SSG distributed systems needs (SCHWARTZ, FOLSOM will support AVERY).

Spanish. (ALFONSO GAJATE can be a resource.)

Discussion format - Bill Avery put up a slide of the SSG survey input for each program which was then open for general discussion.

TOPIC	DISCUSSION
	********** 16BIT PROGRAM **********
QNA	GUTMAN: Why a 1 vote on QNA? GALLUP: 3720/SNA would be higher. Now it would be 0 for RSTS systems. LACROUTE: Let's not re-do the IAS scene. KNOWLES: Who's selling RSTS? GALLUP: COEM today. GUTMAN: With NEBULA pricing commercial says RSTS will go away. GALLUP: We can't say we will not need to support new devices. PORTNER: Is the issue the sale of new systems? GALLUP: Yes, not add-ons. CONKLIN: Support of existing customers? KNOWLES: Only 5% or less get networked. CONKLIN: If we pull DECnet-E accounts and check them out, we can make a clean decision. LACROUTE: Separate the QNA decision from RSTS-E support with more DECnet. GALLUP: If QNA is for use as a cluster file server, then vote would be 2. GALLUP: Extended memory has no applicability to the OEM environment. KNOWLES: Let's be firm about do we want it or not. GALLUP: If we have to be more precise than 0, 1, or 2, we need a better look (see ACTION ITEMS 1 and 2).
Software	HORNIK: The issue on SORT-11 is the support of new data types. JOHNSON: Rewrite is a very small part of the cost; maintenance is cheaper if we rewrite. GUTMAN: We will get out a better definition of projects -- SSG will get back a better statement of need. GALLUP: No need for ORION Q - we'll get data back to GUTMAN.
DECnet and RSTS	LACROUTE: We are now not putting DECnet phase 4 on RSTS! AVERY: Can we do a PDP-11 software migration strategy to CTAB? GUTMAN: We are writing down the PDP-11 software strategy for each O.S. SHANZER: LCP and ORION may be "TVG only" products.
	********** STORAGE PROGRAM **********
Cartridge Tapes	FLYNN: We're planning to cut YANKEE and put more funding to MAYA (the 5 1/4 inch form

TOPIC	DISCUSSION
	factor cartridge product). KNOWLES: BILL AVERY are we planning to use it? FLYNN: MAYA is needed when you need 40MB and up. GUTMAN: You can't back-up a 'mini' onto floppies. The issue is back-up on a file/document basis or to do it on a volume basis. The MAYA looks like the lowest cost, best approach for volume back-up. Really no other good alternatives. FLYNN: With YANKEE dollars, we move MAYA to Q4FY85. The MAYA technology group says Q1FY85 is possible with more funding. AVERY: What about industry standards? GUTMAN: Fixed and removable Winchesters are expensive and the objective with MAYA is to drive costs down (target $500 or less for MAYA potential with high-end at $900. Also it's a cheap media - also potential for 200Mb capacity). GUTMAN: SHRIMP FRS has high risk. FOLSOM: IRWIN drive in FY84? GUTMAN: They are expensive, MAYA still stands up well. We have a great back-up device today with RL02. Let's sell it. FLYNN: Cost reduction is the target on RX52/53. FOLSOM: Back-up is still the issue. GUTMAN: 1Mb floppy versus 1/2M makes no difference. CTAB has software that will help in the beginning. AVERY: File servers are a solution for the clusters. GUTMAN: The risk of pulling YANKEE is the issue of expensive IBM compatability alternatives. GALLUP: Correct. YANKEE type back-up is key, but it doesn't have to be lowest cost.
	********** SOFTWARE PROGRAM **********
Tools for the low-end	KNOWLES: The compatible PASCAL is important and the 0 vote is wrong. GALLUP: Agreed. SCHWARTZ: The technical user will use Fortran. KNOWLES: C on VAX is an important development tool for the low-end. SCHWARTZ: Why isn't it on list? CORBEN: It's a TIG project. JOHNSON: I'll look at low-end development system of C on VMS and RSX. KNOWLES: The votes do not reflect what SSG needs a development tool. ATARI and APPLE (use VAX and) want quality tools for development. JOHNSON: Who'll get back to me on the software requirement for SSG? KNOWLES: SCHWARTZ.
	********** DISTRIBUTED SYSTEMS **********
IBM support	GALLUP: We filled this out, the survey, from COEM's point of view. SCHWARTZ: We have to

TOPIC	DISCUSSION
	get back to you. GALLUP: COEM did not respond from a CT position. LACROUTE: ? is needed for VT200? We will not do DECnet-E (?). SCHWARTZ: IBM support? LACROUTE: It's not in the plan for CT. KNOWLES: We need it. SCHWARTZ: Outside source? JOHNSON: Do you want to have control? We should do it inside. KNOWLES: Right. Emulaters and IBM Gateways are both critical. SCHWARTZ: Going outside is a time to market issue. ADAMS: For Gateway? LACROUTE: Who do we work with to straighten this out? KNOWLES: BILL AVERY (with FOLSOM, SCHWARTZ, et. al.). ADAMS: PLUTO Gateway software at bottom of DP list. LACROUTE: Broadband is a data only network median and not a systems interconnect (see ACTION ITEM 6).
	********** OFIS PROGRAM **********
Foreign Languages	KNOWLES: Where is foreign being done? SCHWARTZ: Spanish? STEWART: In Europe (Dave Stone). JOHNSON: We're working with Europe and GIA. SCHWARTZ: Spanish will be dominant minority in the USA. KNOWLES & SCHWARTZ: We'll give you a party line (ALFONSO is a candidate for helping) [see ACTION ITEM 5]. KNOWLES: What's in OFIS release 1 (CTAB/OFFICE R1)? STEWART: Complete WPS, good mail, and whatever we can on administrative functions. WPS is like WPS-8 and added functionality, such as use in command and menu mode. STEWART: The other releases are not specified. AVERY: Who does the foreign documentation? STEWART: That's a Dave Stone commitment. JOHNSON: The OFFICE Engineering Program has money in the engineering for documentation. KNOWLES: Be sure you don't depend on the US product group for money for foreign documentation. STEWART/JOHNSON: Understood. We are keeping control of the first few releases for quality.
	********** 32B PROGRAM **********
MICROVAX	DEMMER: Why aren't you interested in high availability? GALLUP: We don't see it today. FOLSOM: Why is MICROVAX low in priority? GALLUP: Not enough visibility to project. SCHWARTZ and FOLSOM: We clearly need MICROVAX in the future. SCHWARTZ:

TOPIC	DISCUSSION
	We'll be in trouble with 68000 if we don't have a MICROVAX. DEMMER: You should expect a FY85 time frame for product use. SCHWARTZ: There will be heat in FY84! DEMMER: It's not a money issue now; it's a resource issue. Goal to announce in a year. KNOWLES: The mythology is a problem with world thinking that 68000 is the future.
********** TERMINALS AND WORKSTATIONS **********	
Low cost RO	KNOWLES: It doesn't make sense to do the low-cost RO build at 1.1M for FY83. AVERY: It's really a cost reduced LA100 with higher functionality compared to the Japanese RO products today. KNOWLES: The interactive I/O on VT200 should be a 2 not a 1.
Intelligent Terminal	JOHNSON Software is complex. Why not do a dumb and a CT versus an intelligent terminal? CAMPBELL: The issue is can we have competitive product in the terminals market-place?
Half vs Full Page	KNOWLES: I wouldn't do Half Page. AVERY: Lot's of Full Page engineering is in the Half Page project. Today, it's a factor of 2:1 in cost $900 vs $2000. We are working to Full Page today as a workstation. FOLSOM: We should do Full Page and put the rest of the money in dumb terminals. KNOWLES: Right. AVERY: I'll work the alternatives. The software is major. The issues are really wide open. JOHNSON: I'm for dumb and CT on intelligent and intermediate. PORTNER: Let's size out the whole thing. Dumb vs CT. KNOWLES: It's a high and low end issue.
********** DISCUSSION OF ITEMS NOT IN SCENARIO A **********	
	SCHWARTZ: Technical customers are key as to why we need FPA. GUTMAN: Commercial people seem not to want J-11 systems any more -- perhaps we'll be able to cut the commercial specifi- cations (CIS) and reinvest in FPA.
	JOHNSON: DECPLOT (comments not understood: editor).
********** 36B - COEXISTANCE **********	
	KNOWLES: All 36b is untouchable. JOHNSON: I own coexistance funding. CORBEN: ~~EE~~ The LCG's absence in ~~$~~ voting was noted in the survey results that were sent out.

TOPIC	DISCUSSION
	********** GENERAL COMMENTS **********
	There is a dichotomy. KNOWLES: Two types of customers for personal computers. 60% are Fortune 1300 - Systems and newtworks and IBM. They want us to support them totally. 40% are the small business guy who needs only standalone (no communications and only marginal functionality with respect to interconnects and development tools....?). Volume will be 500,000 in a few years, then 60% will be a big part of that. I've visited Aetna, John Deere, Combustion Engineering, etc. LACROUTE: Let me summarize, you have three types of customers: 1)standalone small business; 2) local area DEC networks (will be a technical environment) and 3) IBM network 3270. KNOWLES: Correct.
Portable type CT	CAMPBELL: The opportunity of the portable OSBORNE type product is important... KNOWLES: Let's get the MAY-JUNE announcement thing done. OSBORNE is $1795, ours is $452 (?) cost with Japanese proposal and uses T-11. GUTMAN: Is there a commodity low profit market? CAMPBELL: It's not low functionality. KNOWLES: Portability is really desirable, low cost is not an issue. I think we would do the high quality at not the lowest cost.

Comparision of Funding

Category	May 76 (FY77)	March 82 (FY 82)
Development	55.9	50.4
next year	27.8	
year after	23.2	
>2 years	4.9	
Support	14.5	10.1
Product Management	4.6	2.9
Product total	75	63.4
Advanced Development	11.8	5.9
Research	?	1.4
Tools	6.6	4.7
Standards and architecture	5.1	2.2
A/D, research, tools, stds.	23.5	14.1
Process engineerinng		.7
Manufacturing process		2.2
Finance		1.9
Personnel		1.8
Unallocated/contingency/space		5.3
Central Administration	1.7	
Group Adminstration		13.5 (seperated)

REQUIRED FOR 16.4% OPERATING PROFIT @ $4.6B NOR

- PLANNING UNITS AT STRATEGIC PLAN CONTRIBUTION MARGINS
- MANUFACTURING AT LAST JUNE FY83 BOD % RELATIONSHIP
- CORPORATE ENGINEERING AT FY82 % NOR
- OTHER CORPORATE SERVICE/WW PRODUCT GROUP STRATEGIC EXPENSE AT Q3 RATE
  INFLATION OFFSET BY PRODUCTIVITY IMPROVEMENT

5 APRIL 1982
S. ARONOFF

RISKS IN MEETING 16.4% OPERATING PROFIT GOAL

- HARDWARE STRATEGIC PLAN CONTRIBUTION MARGINS NOT ACHIEVEABLE
  - HALLWAY CONVERSATIONS
  - FY82 PERFORMANCE

- $75M EXPOSURE IN CORPORATE MANUFACTURING CHARGE
  - OVER CAPACITY

- CORPORATE SERVICES/WW PRODUCT GROUP STRATEGIC EXPENSE
  - ATTRITION REQUIRED TO HOLD AT Q3 LEVEL

5 APRIL 1982
S. ARONOFF

FY83 PROFIT MODEL

		TO REACH FY83 GOAL		WITH RISKS
NOR		$4600M		$4600M
US+GIA DIR MARGIN	@ 40.7%	1007	@37.7%	933
EUROPE DIR MARGIN	@ 37.5%	309	@34.5%	285
CUST. SERV PLCM	@ 23.6%	307	SAME	307
TOTAL MARGIN		1623		1525
OTHER COST OF SALES		34	SAME	34
GENEVA EXP		25	SAME	25
CORP MFG + PROJECTS		147	+$75M	222
PG STRATEGIC EXP		168	INFLATION	180
WARRANTY HQ		63	INFLATION	67
CORPORATE ENGINEERING		305	SAME	305
OTHER CORP. SERV.		125	INFLATION	132
OPERATING PROFIT	$	756		560
	%	16.4%		12.2%
NOR		4900		4900
OPERATING PROFIT	$	848		644
	%	17.3%		13.1%

5 APRIL 1982
S. ARONOFF

CONVERTING RISK DOLLARS TO HEADCOUNT REDUCTIONS

SPENDING GOALS	AT 16.4% OP GOAL	RISKS	$ Δ
HDW PG STRATEGIC EXP	$168M	$180M	$12M
CORP MFG CHG + PROJECTS	147	222	75
WARRANTY HQ	63	67	4
CORP SELLING	17	18	1
CORP MKT/ADV (US)	17	18	1
PERSONNEL	13	15	2
F&A (EXCL EUROPE)	63	66	3
OTHER G&A	6	6	-
SPENDING RISKS			$98M
CONTRIBUTION MARGIN RISK			98
TOTAL RISK			$196M

ATTRITION REQUIRED TO MEET PROFIT GOAL

ATTRITION TO OFFSET SPENDING RISKS	*2450 PEOPLE
ATTRITION TO OFFSET CONTRIBUTION MARGIN RISK	*2450
TOTAL	4900 PEOPLE

* 40K PER PERSON INCREMENTAL COSTS

5 APRIL 1982
S. ARONOFF

ENG STAFF

BILL AVERY	ML12-2/E71
GORDON BELL	ML12-1/A51
LARRY BORNSTEIN	PK3-1/C21
DICK CLINTON	ML12-2/A16
RICK CORBEN	ML12-1/T39
BRUCE DELAGI	ML2-2/T88
BILL DEMMER	TW/D19
ULF FAGERQUIST	MR1-2/E78
SAM FULLER	HL2-3/N11
MIKE GUTMAN	ML12-2/E71
JOHN HOLMAN	ML23-2/T36
BILL JOHNSON	ML12-3/A62
BERNIE LACROUTE	TW/A08
LARRY PORTNER	ML10-2/T32
JOE REILLY	ML12-2/A16
JOHN ROSE	ML12-2/T54
GRANT SAVIERS	ML3-6/E94
JACK SMITH	ML1-4/A54
STEVE TEICHER	HL2-2/N07
WILL THOMPSON	QI-1/E21
PETE VAN ROEKENS	ML12-3/A62

FM'S

STEVE BEHRENS	ML12-3/A62
DICK CLINTON	ML12-2/A16
DON CROWTHER	ML3-5/T71
CHUCK FISCHER	HL2-2/N07
BRUCE GREEN	ML12-2/A16
DICK HASLETT	QI-1/E22
KEN JONES	ML23-2/T36
JIM LAWLESS	ML12-2/A16
DAVID MARKEY	ML5-2/T86
RAY MERCIER	HL1-1/S09
LEO MERTA	HL2-3/N11
CAROL REID	TW/D19
DAVE SAWIN	MR1-2/E78
ED SAWYER	ML3-6/E94
MARY ANN SERRA	ML12-2/E71

3/15/82

MAR 31 1982

digital INTEROFFICE MEMORANDUM

TO: Engineering Staff
FM's
Eli Glazer
Jim Wade

DATE: 30 March 82
FROM: Jim Lawless
DEPT: Central Eng. FP&A
EXT: 223-5811
LOC/MAIL STOP: ML12-2/A16

cc: Ron Aronson

SUBJ: ENGINEERING BUDGET UPDATE AS OF MARCH 31, 1982

The enclosed update shows the budget transfers made through March 31, 1982.

Enclosure

/svb

SUMMARY OF CHANGES TO FY82 ENGINEERING PROJECT EXPENSE BUDGET

	BASE 2/26/82	DOUBLE OCCUPANCY ASSISTANCE	ADDITIONAL SEATTLE/ READING RELOCATION	WESTBORO INVENTORY STARTUP	BASE 3/31/82	
GUTMAN-16 BIT	8676	13			8689	16 BIT-GUTMAN
AVERY-TERM & WS	27998				27998	TERM & WS-AVERY
AVERY-CT	-				-	CT-AVERY
DEMMER-32 BIT	23613				23613	32 BIT-DEMMER
LACROUTE-DIST SYS	17047				17047	DIST SYS-LACROUTE
FAGERQUIST-LSG	28008				28008	LSG-FAGERQUIST
SAVIERS-STORAGE	43237			15	43252	STORAGE-SAVIERS
TEICHER-SEG	17382				17382	SEG-TEICHER
JOHNSON-SOFTWARE	47371		464		47835	SOFTWARE-JOHNSON
HOLMAN-TOPS	7292				7292	TOPS-HOLMAN
THOMPSON-PTD	7118				7118	PTD-THOMPSON
FULLER-SA&T	5837				5837	SA&T-FULLER
FULLER-RAD	1518				1518	RAD-FULLER
FULLER-CORP RES	2966				2966	CORP RES-FULLER
PORTNER-CENTRAL	7449		<324>		7125	CENTRAL-PORTNER
REILLY-FINANCE	2319				2319	FINANCE-REILLY
BORNSTEIN-PERSONNEL	1949				1949	PERSONNEL-BORNSTEIN
ROSE-ADMIN	2709				2709	ADMIN-ROSE
ROSE-NEW SITES	500	<13>	<140>	<15>	332	NEW SITES-ROSE
EXT RESOURCES	1334				1334	EXT RESOURCES
WADE-EURO ENG	1300				1300	EURO ENG-WADE
PORTNER-CONTINGENCY	<1100>				<1100>	CONTINGENCY-PORTNER
GENERAL TECH	-				-	GENERAL TECH
TOTAL	254523	-	-	-	254523	

3/30/82--RL06/5.8

SUMMARY OF CHANGES TO FY83 ENGINEERING PROJECT EXPENSE BUDGET

	BASE 2/26/82	JAPAN TECHNOLOGY TRANSFER	BASE 3/31/82	
GUTMAN-16 BIT	12343		12343	16 BIT-GUTMAN
AVERY-TERM	34117		34117	TERM-AVERY
AVERY-CT	400		400	CT-AVERY
DEMMER-32 BIT	37910		37910	32 BIT-DEMMER
LACROUTE-DIST SYS	21019		21019	DIST SYS-LACROUTE
FAGERQUIST-LSG	33718		33718	LSG-FAGERQUIST
SAVIERS-STORAGE	56768	139	56907	STORAGE-SAVIERS
TEICHER-SEG	16437		16437	SEG-TEICHER
JOHNSON-SOFTWARE	63868		63868	SOFTWARE-JOHNSON
HOLMAN-TOPS	8480		8480	TOPS-HOLMAN
THOMPSON-PTD	7641		7641	PTD-THOMPSON
FULLER-SA&T	7014		7014	SA&T-FULLER
FULLER-RAD	1969		1969	RAD-FULLER
FULLER-CORP RES	3800		3800	CORP RES-FULLER
PORTNER-CENTRAL	9397		9397	CENTRAL-PORTNER
REILLY-FINANCE	2667		2667	FINANCE-REILLY
BORNSTEIN-PERSONNEL	2275		2275	PERSONNEL-BORNSTEIN
ROSE-ADMIN	2760		2902	ADMIN-ROSE
ROSE-NEW SITES	13426		13284	NEW SITES-ROSE
EXT RESOURCES	1540	<139>	1401	EXT RESOURCES
WADE-EURO ENG	1520		1520	EURO ENG-WADE
PORTNER-CONTINGENCY	2188		2188	CONTINGENCY-PORTNER
GENERAL TECH	5347		5347	GENERAL TECH
TOTAL	346604	-	346604	

3/30/82--RL06/5.9

SUMMARY OF CHANGES TO FY84 ENGINEERING PROJECT EXPENSE BUDGET

	BASE 2/26/82	JAPAN TECHNOLOGY TRANSFER	BASE 3/31/82	
GUTMAN-16 BIT	8992		8992	16 BIT-GUTMAN
AVERY-TERM	40828		40828	TERM-AVERY
AVERY-CT	-		-	CT-AVERY
DEMMER-32 BIT	36841		36841	32 BIT-DEMMER
LACROUTE-DIST SYS	23635		23635	DIST SYS-LACROUTE
FAGERQUIST-LSG	34749		34749	LSG-FAGERQUIST
SAVIERS-STORAGE	69213	164	69377	STORAGE-SAVIERS
TEICHER-SEG	17781		17781	SEG-TEICHER
JOHNSON-SOFTWARE	76662		76662	SOFTWARE-JOHNSON
HOLMAN-TOPS	7821		7821	TOPS-HOLMAN
THOMPSON-PTD	8084		8084	PTD-THOMPSON
FULLER-SA&T	8037		8037	SA&T-FULLER
FULLER-RAD	2373		2373	RAD-FULLER
FULLER-CORP RES	4294		4294	CORP RES-FULLER
PORTNER-CENTRAL	10674		10674	CENTRAL-PORTNER
REILLY-FINANCE	3024		3024	FINANCE-REILLY
BORNSTEIN-PERSONNEL	2572		2572	PERSONNEL-BORNSTEIN
ROSE-ADMIN	3138		3138	ADMIN-ROSE
ROSE-NEW SITES	18050		18050	NEW SITES-ROSE
EXT RESOURCES	1779	<164>	1615	EXT RESOURCES
WADE-EURO ENG	1780		1780	EURO ENG-WADE
PORTNER-UNALLOC	28374		28374	UNALLOC-PORTNER
PORTNER-CONTINGENCY	25000		25000	CONTINGENCY-PORTNER
GENERAL TECH	12000		12000	GENERAL TECH
TOTAL	445701	-	445701	

3/30/82--RL06/5.10

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* d i g i t a l *
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TO: *GORDON BELL
JACK SMITH
cc: CAROL GAULT
DOTTIE HOUCK

DATE: THU 22 APR 1982 12:52 PM EST
FROM: JOSEPH REILLY
DEPT: CE FINANCE
EXT: 223-6883
LOC/MAIL STOP: ML12-2/A16

SUBJECT: RUN RATE

Our current run rate using Q3 Annualized puts us at a level of $311MEG (See Attached). I suspect our Q4 run rate would put us at a level of $320MEG.

ADDITIONAL RISKS:

- ECO risk in Terminals & Workstations.
- ULF cannot do his "A Scenario" for his March budget.
- No contingency in our Run Rate numbers.
- 32-Bit needs more people to deliver its "A Scenario".
- Japan, Carnegie West Coast not in run rate.

SUMMARY:

With good management and luck we may be able to deliver our "A Scenario" for $346.6. However, the Low End wants to add and accelerate projects.

If we are to cut out $30MEG more, we should immediately freeze all internal and external hiring with the exception of college hires, cut projects and delay some of our facility projects.

ENGINEERING SPENDING GROWTH

Q	CC SPEND'G. $	% DELTA	PROJECT	% DELTA	HEADCOUNT	% DELTA
Q1	$ 57.9		$ 54.9		$ 4662	
Q2	61.7	6.5	58.6	6.7	4925	5.6
Q3	69.7	12.9	66.3	13.1	5162	4.8
Q4 Est.	75.8	8.7	72.0	8.6	5362	3.8

	ANNUALIZED Q3	FY83 INFLATION	FY83 RUN RATE
PAYROLL	$ 138.0	$ 15.2	$ 153.2
FRINGE	30.0	.5	30.5
OCCUPANCY	21.2	2.1	23.3
DEPRECIATION	18.4	2.5	20.9
PROJECT MATERIAL	18.4	2.5	20.9
OPERATING SUPPLIES	9.6	1.0	10.6

TRAVEL & MEETINGS	6.8	.7	7.5
RELOCATION/HIRING	3.2	.3	3.5
OTHER	33.2	3.3	36.5
TOTAL	$ 278.8	$ 28.1	$ 306.9

ADD

266 College Hires at $40K Salary/Fringe	$ 10.6
John Rose Facilities	10.0
GROSS COST CENTER SPENDING	$ 327.5
Redbook Project Spending 95% CC Spending	$ 311.0

CENTRAL ENGINEERING
PROJECT RUN RATE
FY83

GROUP	TOTAL YEAR PROJECTS	Q4 @ 93%	Q4 ANNUALIZED RUN RATE	CURRENT PLAN	SCENARIO "A"
PSD	8.7	3.0	12.0	12.3	14.4
CT/TERM	30.9	8.8	35.2	34.5	34.5
32-BIT	23.6	6.2	24.8	37.9	44.4
D/S	16.9	4.5	18.0	21.0	21.0
LSG	28.0	7.6	30.4	33.7	33.7
STORAGE	43.2	12.3	49.2	56.9	56.8
SEG	17.0	4.2	16.8	16.4	20.9
SOFTWARE	47.8	12.8	51.2	63.9	67.3
SA&T	10.1	2.8	11.2	12.8	12.8
TOPS	6.7	1.7	6.8	8.5	8.5
PTD	7.2	1.9	7.6	7.6	9.2
SUB TOTAL	240.1	65.8	263.2	305.5	323.5
CENTRAL	12.9	3.4	13.6	17.2	17.1
EUROPE ENG	1.3	.4	1.6	1.5	1.5
EXT. RESOURCES	1.3	.5	2.0	1.4	1.4
SITES	.3	.3	1.2	13.3	13.4
GEN TECH				5.3	5.4

CONTINGENCY	1.1	1.6	6.4	2.2	<15.7>
TOTAL	257.0	72.0	288.0	346.6	346.6

RL0.4.26
EMML MESSAGE ID: 5161173561

APR 1? 1982

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* digital *
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INTEROFFICE MEMORANDUM

TO: Gordon Bell
Joe Reilly
Jack Smith

DATE: March 15, 1982
FROM: Oleh Kostetsky
DEPT: Operations Analysis
EXT: 223-3704
LOC: ML12-3/A62

cc: Larry Portner
Bill Thompson

SUBJECT: CENTRAL ENGINEERING INFLATIONARY TRENDS--ANALYSIS, PROJECTION, IMPLICATIONS AND SUGGESTED ACTION ITEMS.

For several years, much of the Western World has been caught up in a strong inflationary spiral. In this environment, critical resources were often scarce. Scarcity of this type often presented us with the choice of paying more now or waiting and possibly losing market share. In a growth oriented environment coupled with exterior inflation and scarcity it was reasonable to expect that relative emphasis would shift away from cost control toward getting the people, space, material, equipment needed in order to compete. The following study shows that our adaptation to this reality has engendered a steep increase in the cost per person in Central Engineering over the last 4 years.

During the last 6 months the world has begun to move toward a situation where inflation is coming down and most of the formerly scarce resources are available in abundance. Much effort on the part of governments and industries is being directed toward the reduction in the rates of inflation. For the first time in history, major unions have agreed to renegotiate labor costs downward. Hopefully, we are able to adapt to this new state of affairs before we are faced with the reduction in competitiveness so evident in the auto industry.

The purpose of the following analysis is not to criticize the results of the past but to motivate us to more quickly adapt to the new realities confronting us.

OVERALL IMPLICATIONS AND CONCLUSIONS

Cost per person has been increasing at a steep rate over the FY'78-FY'82 time frame (average compounded growth rate of 17.8-19.5% per year). If this trend continues, we will need an increase in budget from a FY'82 total of $237-270 million to $485-579 million in FY'86 just to retain our current personnel. To continue to add people at the FY'78-FY'82 growth rate, would require a $780-998 million budget for FY'86. If external inflation abates and the dollar continues strong on world markets and we do not take immediate action to stem the internal per person inflationary trends, we may find ourselves in an uncompetitive position.

DETAILED IMPLICATIONS

1. The average salary for a person employed by Engineering has been increasing at an average yearly compounded growth rate of 11.2-12.9% during the FY'78-FY'82 time frame.

2. The per person cost of Fringe Benefits has been increasing at an average yearly compounded rate of 14.6-16.3% during the FY'78-FY'82 time frame. In fact the per person growth rate here seems to be accelerating.

3. The per person cost of Occupancy, Depreciation, Leasing has been increasing at an average yearly compounded rate of 26.5-28.4% during the FY'78-FY'82 time frame. In fact the per person growth rate here seems to be accelerating.

4. "Other" expenses (telephone and other cross-charges from outside groups such as Field Service and Manufacturing) has had the largest growth rate (average compounded growth rate of 47.2-49.5% per year during the FY'78-FY'82 time frame). However, there is some evidence of deceleration in the growth rate in the latter part of this period.

5. The % of people defined to be direct (Engineering Supervisors, Technicians, Writers and Engineers) has been a steady 51-53% over the FY'78-FY'82 time frame. The % of labor $'s charged to DIRECT seems to also be level over most of this time frame. There does not seem to be a significant increase in % of $'s spent on overhead activities.

DETAILED CONCLUSIONS

If this trend were to continue:

(a) Cost per person would rise from $47.1-49.9K in FY'82 to $96.3-106.8K in FY'86.

(b) The average salary of a person working in Central Engineering would rise from $22.9-24.3K in FY'82 to $35.0-39.5K in FY'86.

(c) The average salary plus fringe of a person working in Central Engineering would rise from $27.9-29.6K in FY'82 to $43.6-49.5K in FY'86.

(d) Even a compounded growth rate in budget of 30% per year, which would increase the FY'82 budget of $237-270 million to $677-772 million in FY'86, would allow for only a modest people growth rate of 7.4-8.7% for the FY'82-FY'86 time frame. This is substantially less than the 12.6-14.6% growth rate in people experienced in the FY'78-FY'82 time frame. Continued people growth rates at the 12.6-14.6% levels would require a FY'86 budget of $780-998 million.

(e) If the Central Engineering budget growth is reduced from historic growth levels and current cost per man inflation were to continue, it would be difficult to meet our product goals without heroic improvements in productivity.

POSSIBLE CORRECTIVE ACTION ITEMS

We must find ways to reduce the rates of increase. Possible first steps:

(a) Significantly reduce the average % in salary increases allowed during the upcoming salary planning exercise.

(b) Increase the deductible on the John Hancock major medical policy from $50 (to $250 or so). The $50 of 10 years ago is not the $50 of today.

(c) Charter an in-depth analysis of what has been going on with "Other" expenses. This is a very confusing area with millions of offsetting expenses flowing through a myriad of accounts and categorized in a confusing manner on our financial reports.

(d) Set up a committee to develop proposals to reduce Occupancy cost increases.

(e) Set up a committee to develop proposals to reduce the Supplies, Materials, Tools cost increases.

(f) Put a freeze on Fringe "improvements" for the duration.

(g) Create a supplemental stock option plan specifically directed at difficult-to-find and difficult-to-keep classes of employee. This can make it easier to keep key people without undue escalation of overall salary expenses.

POSSIBLE IMPLICATIONS OF CORRECTIVE ACTION ITEMS

If these (or other) corrective steps result in the following reduction in the rates of internal inflationary growth:

(a) Reduction in Average Salary growth from an expected 11.2-12.9% to 8% per year.

(b) Reduction in Fringe Cost Per Person growth from an expected 14.6-16.3% to 8% per year.

(c) Reduction in Relocation and Hiring Cost Per Person growth from an expected 31.6% to 14% per year.

(d) Reduction in Supplies, Materials, Tools Cost Per Person growth from an expected 21.1-22.5% to 20% per year.

(e) Reduction in Occupancy, Depreciation, Leases Cost Per Person growth from an expected 26.5-28.4% to 24% per year.

(f) Reduction in Travel and Meetings Cost Per Person growth from an expected 31.6-33.8% to 20% per year.

(g) Reduction in "Other" Cost Per Person growth from an expected 34.4% to 20% per year.

then:

(a) The Total Cost Per Person growth rate would be reduced from an expected 19.6-21.0% to 13.9% per year.

(b) The Total Cost Per Person in FY'86 would be reduced from an expected $96.3-106.8K to $79.2-84.0K.

(c) The budget required to maintain the current level of personnel would fall from an expected $485-579 million to $399-455 million in FY'86.

(d) The budget required to maintain the current people growth rates of 12.6-14.6% would fall from an expected $780-998 million to $641-785 million in FY'86.

SUMMARY

Without the management of factors affecting the rates of increase in cost, future cost per person numbers could force us into an uncompetitive position. Once the rates assert themselves, our options for controlling the resultant cost levels are limited. If rates of change are not managed, the cost control burden becomes one of limiting people growth and striving for productivity improvements. However, productivity improvements of heroic proportions would be required to keep pace with inflationary rates of this magnitude. The projections inherent in this analysis show that it would take a doubling in productivity every four years just to keep pace with historic internal inflation rates. When cost per person numbers escalate at these very high rates, we find that all groups tend to complain of a shortage of people and find it difficult to invest in technology designed to improve tomorrow's productivity. Thus, without the management of the rates of cost increase we will find ourselves without the means to do the job or the means to raise productivity to do the job.

On the other hand, if we could find ways to reduce the average internal inflation rate down to a more manageable 14% per or so, the Total Cost Per Person for FY'86 would be reduced from an expected 100K to a 80K range and current budget projections could support historical people growth rates.

This analysis indicates that we must establish a strong management focus to reduce and continuously control these rates of change.

METHOD

1. Calculated cost per person for various categories of cost for FY'1978, FY'1980-81.

2. Estimated cost per person for various categories of cost for FY'82 using actuals for the first 8 months of this fiscal year and latest budget numbers for the balance of the year.

3. Calculated the average compounded rate of growth from FY'78 to FY'82 for each category of cost. Use these growth rates to make initial projections of FY'82-FY'86 growth rates.

4. Calculated the rates of the rates of change for various time frames and modified the rate of change projections derived in 3. above in order to take significant evidence of acceleration of deceleration into account.

5. Projected the average cost per person for FY'86 by applying the growth rates calculated in 3. and 4. above against their respective category of cost and adding up the results obtained for each category. Did this for two sets of assumption as to what FY'82 expenses and headcount will end up at.

6. Calculated budget requirements using cost per person projections obtained in 5. above assuming (a) no headcount growth (b) headcount will grow at historic rates.

7. Did a similar analysis and projection of Central Software Engineering data as a check. The results were remarkably similar.

I. ASSUMPTION SET I.

CENTRAL ENGINEERING - EXPENSES ($millions)

DESCRIPTION	FY'78	FY'79	FY'80	FY'81	EST. FY'82	COMPOUND GROWTH RATE FY'78-FY'82	PROJECTED FY'86 IF FY'82-FY'86 PEOPLE GROWTH RATE CONT. AT FY'78-82 LEVEL: PROJECTED FY'86	PROJECTED COMPOUND GROWTH RATE FY'82-FY'86
DIRECT LABOR + LABOR PORTION OF CONTRACT PEOPLE(EST.)	29.1		43.4	57.8	74.6	26.5%	209.3	29.4%
INDIRECT LABOR + OT PREMIUM	17.9		33.3	43.9	57.1	33.6%	159.8	29.3%
FRINGE + FRINGE PORTION OF CONTRACT PEOPLE(EST.)	9.0		14.0	20.2	28.6	33.5%	90.6	33.4%
RELOCATION AND HIRING	0.8		2.1	2.0	5.0	58.1%	25.2	49.8%
SUPPLIES, MATERIALS, TOOLS	6.2		13.2	13.2	24.5	41.0%	94.4	40.1%
OCCUPANCY, DEPRECIATION, LEASES	7.7		15.4	23.2	36.9	48.0%	172.8	47.1%
TRAVEL AND MEETINGS	1.6		4.1	5.8	8.4	51.4%	47.6	54.3%
OTHER	4.6		11.7	27.6	35.1	66.2%	198.1	54.1%
TOTAL	76.9		137.3	193.7	270.2	36.9%	997.8	38.6%

CENTRAL ENGINEERING - PEOPLE

NUMBER OF DIRECT DEC PEOPLE	1486	1768	2141	2316	2658	15.7%		
ESTIMATED NUMBER OF CONTRACT PEOPLE	293		106	142	215	-7.5%		
DIRECT PEOPLE	1779		2247	2458	2873	12.7%	4955	14.6%
INDIRECT PEOPLE	1359	1594	1999	2216	2544	17.0%	4388	14.6%
TOTAL PEOPLE	3138		4246	4674	5417	14.6%	9343	14.6%
% DEC DIRECT TO TOTAL DEC	52.2%	52.2%	51.7%	51.1%	51.1%		51.0%	
% DIRECT (INCLUDING CONTRACT) TO TOTAL	56.7%		52.9%	52.6%	53.0%		53.0%	
% LABOR $ CHARGED TO DIRECT	61.9%		56.6%	56.8%	56.6%		56.7%	

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I. ASSUMPTION SET I. (continued)

CENTRAL ENGINEERING - COST PER PERSON ($1000)

DESCRIPTION	FY'78	FY'79	FY'80	FY'81	EST. FY'82	COMPOUND GROWTH RATE FY'78-FY'82	PROJECTED FY'86	PROJECTED COMPOUND GROWTH RATE FY'82-FY'86
SALARY	15.0		18.1	21.8	24.3	12.9%	39.5	12.9%
FRINGE	2.9		3.3	4.3	5.3	16.3%	9.7	16.3%
RELOCATION AND HIRING	0.3		0.5	0.4	0.9	31.6%	2.7	31.6%
SUPPLIES, MATERIALS, TOOLS	2.0		3.1	2.8	4.5	22.5%	10.1	22.5%
OCCUPANCY, DEPRECIATION, LEASES	2.5		3.6	5.0	6.8	28.4%	18.5	28.4%
TRAVEL AND MEETINGS	0.5		1.0	1.2	1.6	33.8%	5.1	33.8%
OTHER	1.3		2.8	5.9	6.5	49.5%	21.2	34.4%
TOTAL	24.5		32.3	41.4	49.9	19.5%	106.8	21.0%

CENTRAL ENGINEERING - PER CENT OF TOTAL

DIRECT LABOR + LABOR PORTION OF CONTRACT PEOPLE(EST.)	37.9		31.6	29.8	27.6	-7.6	21.0	-6.6
INDIRECT LABOR + OT PREMIUM	23.3		24.3	22.7	21.1	-2.4	16.0	-6.7
FRINGE + FRING PORTION OF CONTRACT PEOPLE (EST.)	11.6		10.2	10.4	10.6	-2.2	9.1	-3.7
RELOCATION AND HIRING	1.1		1.5	1.0	1.9	14.6	2.5	7.1
SUPPLIES, MATERIALS, TOOLS	8.1		9.6	6.8	9.1	3.0	9.5	1.1
OCCUPANCY, DEPRECIATION, LEASES	10.1		11.3	12.0	13.7	7.9	17.3	6.0
TRAVEL AND MEETINGS	2.1		3.0	3.0	3.1	10.2	4.8	11.6
OTHER	5.8		8.5	14.3	13.0	22.4	19.9	11.2
TOTAL	100.0		100.0	100.0	100.0	100.0	100.0	100.0

Maintenance of FY'82 headcount would require a FY'86 budget of $578.5 million (5417 people x $106.8K).

Maintenance of historic people growth rate of 14.6% would require a FY'86 budget of $997.8 million (9343 people x $106.8K).

An annual budget growth of 30% would provide for a FY'86 budget of $771.7 million which would allow for a FY'86 headcount of 7226 ($771.7 million divided by $106.8K per person), which would amount to a 7.4% compounded people growth rate.

I. ASSUMPTION SET I. (continued)

CENTRAL ENGINEERING - PER PERSON AVERAGE YEARLY GROWTH RATES

	FY'78-FY'80	FY'80-FY'82	FY'81-FY'82	FY'78-FY'82
LABOR	9.8%	15.9%	11.5%	12.8%
FRINGE	6.7%	27.6%	23.3%	16.3%
RELOCATION AND HIRING	29.1%	34.2%	125.0%	31.6%
SUPPLIES, MATERIALS, TOOLS	24.5%	20.5%	60.7%	22.5%
OCCUPANCY, DEPRECIATION, LEASES	20.0%	37.4%	36.0%	28.4%
TRAVEL AND MEETINGS	41.4%	26.5%	33.3%	33.8%
OTHER	46.8%	52.4%	10.2%	49.5%
TOTAL	14.8%	24.3%	20.5%	19.5%

II. ASSUMPTION SET II. (conservative)

CENTRAL ENGINEERING - EXPENSES ($millions)

DESCRIPTION	FY'78	FY'79	FY'80	FY'81	EST. FY'82	COMPOUND GROWTH RATE FY'78-FY'82	PROJECTED FY'86 IF FY'82-FY'86 PEOPLE GROWTH RATE CONT. AT FY'78-82 LEVEL: PROJECTED FY'86	PROJECTED COMPOUND GROWTH RATE FY'82-FY'86
LABOR	47.0		74.3	93.4	115.5	25.2%	283.3	25.1%
FRINGE	9.0		13.6	18.6	25.1	29.2%	69.6	29.0%
RELOCATION AND HIRING	0.8		2.0	1.8	4.4	53.1%	21.9	49.4%
SUPPLIES, MATERIALS, TOOLS	6.2		12.8	12.1	21.5	36.5%	74.5	36.4%
OCCUPANCY, DEPRECIATION, LEASES	7.7		14.9	21.3	32.4	43.2%	132.8	42.3%
TRAVEL AND MEETINGS	1.6		4.0	5.3	7.4	46.6%	36.4	48.9%
OTHER	4.6		11.3	25.4	30.8	60.9%	161.1	51.2%
TOTAL	76.9		133.0	178.0	237.0	32.5%	779.6	34.7%
TOTAL PEOPLE	3138		4246	4674	5036	12.6%	8095	12.6%

CENTRAL ENGINEERING - COST PER PERSON ($1000)

DESCRIPTION	FY'78	FY'79	FY'80	FY'81	EST. FY'82	COMPOUND GROWTH RATE FY'78-FY'82	PROJECTED FY'86	PROJECTED COMPOUND GROWTH RATE FY'82-FY'86
LABOR	15.0		17.5	20.0	22.9	11.2%	35.0	11.2%
FRINGE	2.9		3.2	4.0	5.0	14.6%	8.6	14.6%
RELOCATION AND HIRING	0.3		0.5	0.4	0.9	31.6%	2.7	31.6%
SUPPLIES, MATERIALS, TOOLS	2.0		3.0	2.6	4.3	21.1%	9.2	21.1%
OCCUPANCY, DEPRECIATION, LEASES	2.5		3.5	4.6	6.4	26.5%	16.4	26.5%
TRAVEL AND MEETINGS	0.5		0.9	1.1	1.5	31.6%	4.5	31.6%
OTHER	1.3		2.7	5.4	6.1	47.2%	19.9	34.4%
TOTAL	24.5		31.3	38.1	47.1	17.8%	96.3	19.6%

Maintenance of FY'82 headcount would require a FY'86 budget of $485.0 million (5036 x $96.3K).

Maintenance of historic people growth rate of 12.6% would require a FY'86 budget of $779.6 million (8095 x $96.3K).

An annual budget growth of 30% would provide for a FY'86 budget of $676.9 million which would allow for a FY'86 headcount of 7029 which amounts to a 8.7% compounded people growth rate.

II. ASSUMPTION SET II. (continued)

CENTRAL ENGINEERING - PER PERSON AVERAGE YEARLY GROWTH RATES

	FY'78-FY'80	FY'80-FY'82	FY'81-FY'82	FY'78-FY'82
LABOR	8.0%	14.3%	14.5%	11.2%
FRINGE	5.0%	25.0%	25.0%	14.6%
RELOCATION AND HIRING	29.1%	34.2%	125.0%	31.6%
SUPPLIES, MATERIALS, TOOLS	22.5%	19.7%	65.4%	21.1%
OCCUPANCY, DEPRECIATION, LEASES	18.3%	35.2%	39.1%	26.5%
TRAVEL AND MEETINGS	34.2%	29.1%	22.2%	31.6%
OTHER	44.1%	50.3%	13.0%	47.2%
TOTAL	13.0%	22.7%	23.6%	17.8%

III. TAKE ACTION TO REDUCE INFLATIONARY GROWTH (applied against ASSUMPTION SET I.)

TAKE ACTION TO REDUCE COST PER PERSON RATES AS FOLLOWS:

LABOR Cost growth rate reduced to 8.0% per year
FRINGE Cost growth rate reduced to 8.0% per year
RELOCATION AND HIRING Cost growth rate reduced to 14.0% per year
SUPPLIES,MATERIALS,TOOLS Cost growth rate reduced to 20.0% per year
OCCUPANCY,DEPRECIATION,LEASES Cost growth rate reduced to 24.0% per year
TRAVEL AND MEETINGS Cost growth rate reduced to 20.0% per year
OTHER Cost growth rate reduced to 20.0% per year

PROJECTED RESULT:

CENTRAL ENGINEERING - TOTAL EXPENSES ($millions)

DESCRIPTION	FY'78	FY'82	COMPOUND GROWTH RATE FY'78-FY'82	PROJECTED FY'86 IF FY'82-FY'86 PEOPLE GROWTH RATE REMAINS AT FY'78-FY'82 LEVEL: PROJECTED FY'86	PROJECTED COMPOUND GROWTH RATE FY'82-FY'86	PROJECTED FY'86 IF FY'82-FY'86 PEOPLE GROWTH RATE HELD TO 0%: PROJECTED FY'86	PROJECTED COMPOUND GROWTH RATE FY'82-FY'86
LABOR	47.0	131.7	29.4%	309.3	23.8%	179.3	8.0%
FRINGE	9.0	28.6	57.2%	67.3	23.9%	39.0	8.0%
RELOCATION AND HIRING	0.8	5.0	40.9%	14.0	29.4%	8.4	14.0%
SUPPLIES,MATERIALS,TOOLS	6.2	24.5	47.8%	86.9	37.2%	50.4	20.0%
OCCUPANCY,DEPRECIATION,LEASES	7.7	36.9	55.3%	150.4	42.1%	87.2	24.0%
TRAVEL AND MEETINGS	1.6	8.4	50.8%	30.8	38.4%	17.9	20.0%
OTHER	4.6	35.1	66.2%	126.1	37.7%	73.1	20.0%
TOTAL	76.9	270.2	36.9%	784.8	30.5%	455.3	13.9%

CENTRAL ENGINEERING - HEADCOUNT

TOTAL PEOPLE	3138	5417	14.6%	9343	14.6%	5417	0.0%

CENTRAL ENGINEERING - PER PERSON EXPENSES ($1000)

DESCRIPTION	FY'78	FY'82	COMPOUND GROWTH RATE FY'78-FY'82	MANAGED PROJECTION FY'86	MANAGED COMPOUND GROWTH RATE FY'82-FY'86
LABOR	15.0	24.3	12.9%	33.1	8.0%
FRINGE	2.9	5.3	16.3%	7.2	8.0%
RELOCATION AND HIRING	0.3	0.9	31.6%	1.5	14.0%
SUPPLIES,MATERIALS,TOOLS	2.0	4.5	22.5%	9.3	20.0%
OCCUPANCY,DEPRECIATION,LEASES	2.5	6.8	28.4%	16.1	24.0%
TRAVEL AND MEETINGS	0.5	1.6	33.8%	3.3	20.0%
OTHER	1.3	6.5	49.5%	13.5	20.0%
TOTAL	24.5	49.9	19.5%	84.0	13.9%

IV. TAKE ACTION TO REDUCE INFLATIONARY GROWTH (applied against ASSUMPTION SET II.)

TAKE ACTION TO REDUCE COST PER PERSON RATES AS FOLLOWS:

LABOR Cost growth rate reduced to 8.0% per year
FRINGE Cost growth rate reduced to 8.0% per year
RELOCATION AND HIRING Cost growth rate reduced to 14.0% per year
SUPPLIES,MATERIALS,TOOLS Cost growth rate reduced to 20.0% per year
OCCUPANCY,DEPRECIATION,LEASES Cost growth rate reduced to 24.0% per year
TRAVEL AND MEETINGS Cost growth rate reduced to 20.0% per year
OTHER Cost growth rate reduced to 20.0% per year

PROJECTED RESULT:

CENTRAL ENGINEERING - TOTAL EXPENSES ($millions)

				PROJECTED FY'86 IF FY'82-FY'86 PEOPLE GROWTH RATE REMAINS AT FY'78-FY'82 LEVEL		PROJECTED FY'86 IF FY'82-FY'86 PEOPLE GROWTH RATE HELD TO 0%	
	FY'78	FY'82	COMPOUND GROWTH RATE FY'78-FY'82	PROJECTED FY'86	PROJECTED COMPOUND GROWTH RATE FY'82-FY'86	PROJECTED FY'86	PROJECTED COMPOUND GROWTH RATE FY'82-F6'86
LABOR	47.0	115.5	25.2%	252.6	21.6%	157.1	8.0%
FRINGE	9.0	25.1	29.2%	55.0	21.7%	34.1	8.0%
RELOCATION AND HIRING	0.8	4.4	53.1%	12.1	28.8%	7.4	14.0%
SUPPLIES,MATERIALS,TOOLS	6.2	21.5	36.5%	72.0	35.3%	44.6	20.0%
OCCUPANCY,DEPRECIATION,LEASES	7.7	32.4	43.2%	122.0	39.4%	76.6	24.0%
TRAVEL AND MEETINGS	1.6	7.4	46.6%	25.1	35.7%	15.3	20.0%
OTHER	4.6	30.8	60.9%	102.0	34.9%	63.9	20.0%
TOTAL	76.9	237.0	32.5%	641.1	28.2%	399.0	13.9%

CENTRAL ENGINEERING - HEADCOUNT

TOTAL PEOPLE	3138	5036	12.6%	8095	12.6%	5036	0.0%

CENTRAL ENGINEERING - PER PERSON EXPENSES ($1000)

	FY'78	FY'82	COMPOUND GROWTH RATE FY'78-FY'82	MANAGED PROJECTION FY'86	MANAGED COMPOUND GROWTH RATE FY'82-FY'86
LABOR	15.0	22.9	11.2%	31.2	8.0%
FRINGE	2.9	5.0	14.6%	6.8	8.0%
RELOCATION AND HIRING	0.3	0.9	31.6%	1.5	14.0%
SUPPLIES,MATERIALS,TOOLS	2.0	4.3	21.1%	8.9	20.0%
OCCUPANCY,DEPRECIATION,LEASES	2.5	6.4	26.5%	15.1	24.0%
TRAVEL AND MEETINGS	0.5	1.5	31.6%	3.1	20.0%
OTHER	1.3	6.1	47.2%	12.6	20.0%
TOTAL	24.5	47.1	17.8%	79.2	13.9%

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SUBJECT: ENGINEERING PROJECT LISTS - PART I

********** PART I OF II **********

The following is the first draft of the Engineering project list. It is for use by the Market Groups in surveying their P/Gs on the business importance of each item. Engineering Groups should review the list and submit any corrections by Thursday at 5:00PM so that I can have a final version for our Market Group/Program Office meeting on Friday afternoon (3PM, ML2-2, RAD Conference Room).

The philosophy in assembling the list was to identify Engineering-funded projects with product deliverables. In general, pure maintenance spending ECOs, FCC, and other legal or contractual committments were excluded. Similarly, Engineering advance development, tool/process development, research, and other non-product items were left out. The dollar figures shown for FY'83 are intended to give a gross feeling of project scale. The rules for allocating dollars to individual Engineering projects are not consistent across the groups so precise comparisions should be avoided.

/jdm
RC1.S6.46

	FRS	FY'83 K$
16-BIT PROGRAM		
ORION U, Q	Q4FY84	4300
LCP-5	Q4/Q2FY83	2800
LCP-8	H1FY84	500
QNA	Q4FY83	500
RSTS SUBSETS	Q2FY83	100
RSTS SMALL BATCH & UTILITIES	Q1FY84	100
RSTS NI SUPPORT	H1FY84	100
RSX ENHANCED BACKUP	Q2FY83	---
RT EXTENDED MEMORY	Q4FY83	100
RT NEW BACKUP	Q4FY83	100
RT CUSTOMER INSTALLATION	Q4FY83	100
MICRO-POWER HOSTED BY RSX & VMS	Q4FY83	---
FORTRAN FULL ANSI-77	Q1FY84	300
COBOL-81 REPLACE COBOL-11	Q4FY83	400
BASIC-PLUS-2 TRACK STANDARDS	Q2FY84	300
RMS-11 REMOVAL FROM USER SPACE	Q2FY84	500
SORT-11 REWRITE	Q4FY83	100

FMS-11 REWRITE	Q3FY84	500
32-BIT PROGRAM		
11/780		
64K CHIP	Q2FY83	142
CI CLUSTERS/HI AVAILABILITY		800
COMMUNICATIONS SWITCH	FY83	330
11/750		
CI750	Q1FY84	1106
FP750	SHIPPED	84
PACKAGED SYSTEMS	FY83	201
UNA/UDA	?	200
DW750	Q4FY82	288
11/730		
COMBO	Q4FY82	375
BATTERY BACKUP	Q3FY83	375
PACKAGED SYSTEMS	FY83	200
VENUS		
DEVELOPMENT	FY84	15300
NAUTILUS		
DEVELOPMENT	FY85	6049
SCORPIO		
DEVELOPMENT	FY85	6200
WORKSTATION		
DEVELOPMENT		
- HIGH END BUYOUT WORKSTATION	Q2FY83	900
- LOW END WORKSTATION	Q4FY83	5400
MICRO-VAX		
START-UP		1300
CHIP & BOARD SOFTWARE		700
CLUSTERS/HI AVAILABILITY*		
CI CLUSTERS	Q4FY82	
HI AVAILABILITY	Q4FY83	
*BUDGET PART OF 11/780 PROGRAM		
32-BIT SOFTWARE		
VMS	4QFY82	5806
VAX11 RMS	4QFY82	1201
VAX11 PL/1		601
HYDRA (DATA INTEGRITY)		3003
SMALL 32-BIT		1802
VAX11 RTL		890
VAX11 DEBUGGER		574
VAX11 SORT/MERGE	4QFY83	133
VAX11 EDITOR	4QFY83	265
VAX CROSS LAN TEST		90

VAX11 APL		332
VAX11 BASIC		890
VAX11 COBOL	4QFY82	980
VAX11 FORTRAN	4QFY82	413
VAX11 PASCAL V1.2		---
VAX11 PASCAL V2.0	1QFY83	493
ADA	FY83	574
ADA PSE		332
CATS	2HFY83	2037
TPSS	2HFY83	2058
IMS ARCHITECTURE		268
VAX11 DBMS	2QFY84	1352
CDD-32	6/82	425
RDMS-32	4/83	1057
DTR/DDMF-32	2HFY83	759
CATS/TPSS ARCH		---
VTC	2QFY83	---
CHIP & BOARD		800
PASCAL-11		81

36-BIT PROGRAM

JUPITER SYSTEM		
JUPITER HARDWARE (2080)	1QFY84	7075
JUPITER T20/COMM		1096
NI PLUTO		83
JUPITER HSC-50		119
JUPITER/20 COMM		576
JUPITER TOPS-10		0
36-BIT SOFTWARE		
APLSF	3QFY83	100
MACRO/LINK	FY83	40
FORTRAN V7	3QFY83	400
36-BIT HARDWARE		
CURRENT PRODUCT SUPPORT		691
KLIPA		107
36-BIT COMM SOFTWARE		
DECNET-10 3.0		72
X.29		83

"TO" DISTRIBUTION:

JOHN ADAMS	JACK BUCKLEY	CONDON @MK12
PETER F CONKLIN	GARY J ECKROTH	GEORGE EVANS
DAVE FERNALD	BOB FLYNN	LLOYD FUGATE
MIKE GALLUP	ROBERT JOSEPH	GARY KEELER
JOHN O'KEEFE	BILL PICOTT	DICK RISLOVE
DAVID STROLL	DICK STRAUSS	GEORGE THISSELL

FMS		1308
GRAPHICS		555

STORAGE PROGRAM

RA81 & SWFT	Q1FY83	2343
RD50/51	Q2FY83	425
AZTEC	Q4FY83	6160
HSC50	Q4FY83	5170
TA78	Q4FY83	720
RA60 & SWFT	Q3FY83	4011
TU81/TA81	Q483	1000
TU80	Q3FY83	450
UDA-52	Q4FY83	1300
RX50	Q2FY83	609
RAXX & SWFT	Q3FY86	4296
MAYA	FY86	1575
AZTEC II	Q4FY85	250
RAXY	Q3FY86	(WITH RAXX)
YANKEE	FY87	500
HSC CACHE	Q4FY84	1000
SHRIMP	FY87	0
BSA	Q4FY87	0
RD52	Q2FY85	2080
RX52/53	Q3FY85	600

/jdm
RC1.S6.47

"TO" DISTRIBUTION:

JOHN ADAMS	JACK BUCKLEY	CONDON @MK12
PETER F CONKLIN	GARY J ECKROTH	GEORGE EVANS
DAVE FERNALD	BOB FLYNN	LLOYD FUGATE
MIKE GALLUP	ROBERT JOSEPH	GARY KEELER
JOHN O'KEEFE	BILL PICOTT	DICK RISLOVE
DAVID STROLL	DICK STRAUSS	GEORGE THISSELL

ENGINEERING DEVELOPMENT SUMMARY

PRODUCT	ENG $M '83 -'85	NOR $B '82 -'86	NOR $B LIFETIME
11/780, 11/750, 11/730	28.1	12.8	17.9
VENUS	42.4	1.8	10.2
NAUTILUS	23.8	.2	11.9
SCORPIO	22.0	.3	6.0
MICROVAX	13.0	?	?
VMS FAMILY SOFTWARE	95.5*	^	^
ALL 11'S TO 11/23+		4.0	4.5*
LCP 5, 8 (F-11 BASED)	3.3	.3	1.3*
ORION U, Q (J-11 BASED)	9.4	.4	2.4*
16B SOFTWARE	44.4	^	^
AZTEC I & II	17.2	1.4@	5.7
HSC & BSA CHANNELS/ADAPTORS	14.2	.3	.8
RA81, RAXX, RAXY (LARGE DISKS)	33.1	1.3	7.7
TA78, TU80, TU/TA81 (IND. TAPES)	4.2	1.2	2.5
SM. DIAM. DISKS (RX, RD)	9.6	1.3	1.8
SHRIMP (5 1/4" WINI)	5.4	-	3.0
MAYA (SM HI CAPACITY TAPE)	13.9	.1	3.3
RA60 (PINION & REMOVABLE DISK)	4.1	1.0	1.7
CT/CAT/DECMATE II	52.2	9.8*	?
TOTAL VIDEO FAMILY	26	1.8	4.2
TOTAL HARDCOPY	29.3	1.5	2.2
WORKSTATION (INCL. 32B, ETC.)	15.6	.6	1.6
U.Q BUS OPTIONS +1.4			
NI. ETHERNET HDW +3.9			
DECNET & X.25 SW +2.3			
SERVERS & GATEWAYS +3.0			
TOTAL DISTRIBUTED SYSTEMS	o75.2	^?	^?
36 BIT SYSTEMS PROGRAM	33.4	.7	1.6
CTAB/OFFICE +2.2			
TOTAL OFFICE PROGRAM	23.5	?	?
COEXISTANCE 20/VAX +1.0			
TOT. COEXIST., TOOLS, X-PROD. SW	8.5		
SEMICONDUCTOR PRODUCTS	31.7**		
SEG TOOLS & ADV DEV	19.7**		
PROCESS TECHNOLOGY	31.5		

NOTES:

? No estimate of revenue
^ Included in systems revenue
@ Most of the disk revenue is included in the systems revenue
+ FY83 $M
* Eli Glazer estimate
o Includes all Non-Product Expenses
** Does not include manufacturing process engineering investment

****
* d i g i t a l *
****

TO: see "TO" DISTRIBUTION

cc: PEG:

DATE: WED 10 FEB 1982 3:44 PM EST
FROM: RICK CORBEN
DEPT: CORP PRODUCT MGMT
EXT: 223-3123
LOC/MAIL STOP: ML12-1/-T39

SUBJECT: ENGINEERING PROJECT LIST - PART II

********** PART II **********

	FRS	FY'83 K$
TERMINALS & WORKSTATIONS PRODUCTS		
CT Family		
CT100	Q1FY83	8379
CT25	Q1FY84	662
CT CLUSTERS	Q1FY84	1694
PRINTING		
LA100RO	Q3FY83	500
LOW COST RO--BUYOUT	FY83	200
LOW COST RO--BUILD	FY85	1100
ELECTRONIC PRINTERS		
- EP1 (10-12 PPM)	Q2FY83	200
- EP3 (5-6 PPM)	FY86	700
KEYBOARDS (LA/VT/CT 200)		200
VIDEO		
VT200-QX (LOW COST)	Q3FY83	1200
VT200-H (HALF-PAGE)	Q4FY83	2950
VT200--FULL PAGE	Q1FY85	800
VT200 CUSTOM LSI	N/A	1100
VT200 SYSTEMS REF. MANUAL & PROGRAMMER'S MANUALS	N/A	150
VT200 INTERACTIVE I/O OPTIONS (LIGHT PEN/TABLET, ETC.)	N/A	235
OFIS PROGRAM		
DECmail V1.1	Q1FY83	419
VAX/OFFICE R1	Q2FY83	1600
OFFICE/FRENCH	Q3FY83	100
OFFICE/GERMAN	Q3FY83	100
VAX/OFFICE R2	Q4FY83	---
VAX/OFFICE R3	FY84	---
RSX11M+/OFFICE R1	Q4FY83	200
CTAB/OFFICE R1	Q4FY83	2200
CTAB/OFFICE R2	FY84	---
CTAB/OFFICE R3	FY84	

NOTE: Allocation of FY'83 spending to specific

releases is especially arbitrary in the case of OFIS.

DISTRIBUTED SYSTEM PRODUCTS*

*(See Glossary of terms attached)

UNIBUS OPTIONS		
HDLC SUPPORT IN DMP	H1FY84	250
DMZ32	H1FY84	PL FUNDED
QBUS OPTIONS		
DZV-8	H1FY84	400
HDLC SUPPORT IN DMV	H1FY84	250
NI HARDWARE		
TRANSCEIVER	1/83	40
UNA	6/83	640
TRANSCEIVER POWER SUPPLY	H1FY84	100
PLUTO	9/83	1070
LSI QNA	FY86	250
INTELLIGENT UNA	FY86	400
PLUTO JR.	H1FY85	600
LNI	Q1FY84	300
BROADBAND TRANCEIVER	H2FY84	500

NOTE: MSI QNA is funded out of PSD,
CTNA is funded out of CT Program.

DECNET		
DECnet RSX (PIV & NI)	Q3FY84	422
DECnet VAX (PIV & NI)	Q4FY83	1200
DECnet E (PIV & NI)	H2FY84	500
X.25 (STANDALONE PSI PRODUCTS)		
VAX PSI	6/82	60
RSX PSI	3/83	100
SERVERS		
SERVER BASE	Q4FY83	568
ROUTER	Q1FY84	283
X.25 GATEWAY	6/84	440
SNA GATEWAY(NON NI)	2/83	484
SNA GATEWAY(NI)	Q4FY84	460
TERMINAL CONC.	9/83	560
XEROX GATEWAY	H2FY85	209

CROSS SYSTEM COEXISTENCE SOFTWARE

COEX COMPUTERS	220
DATA CONVERSION SUB	73
DIU	293
MSG TRANS SYST/MTS	219
REMOTE FILE ACCESS	142
REMOTE SPOOLING & BATCH	73

FMS	1308
GRAPHICS	555

STORAGE PROGRAM

RA81 & SWFT	Q1FY83	2343
RD50/51	Q2FY83	425
AZTEC	Q4FY83	6160
HSC50	Q4FY83	5170
TA78	Q4FY83	720
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TU81/TA81	Q483	1000
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RX50	Q2FY83	609
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MAYA	FY86	1575
AZTEC II	Q4FY85	250
RAXY	Q3FY86	(WITH RAXX)
YANKEE	FY87	500
HSC CACHE	Q4FY84	1000
SHRIMP	FY87	0
BSA	Q4FY87	0
RD52	Q2FY85	2080
RX52/53	Q3FY85	600

/jdm
RC1.S6.47

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ENGINEERING DEVELOPMENT SUMMARY

PRODUCT	ENG $M '83 -'85	NOR $B '82 -'86	NOR $B LIFETIME
11/780, 11/750, 11/730	28.1	12.8	17.9
VENUS	42.4	1.8	10.2
NAUTILUS	23.8	.2	11.9
SCORPIO	22.0	.3	6.0
MICROVAX	13.0	?	?
VMS FAMILY SOFTWARE	95.5*	^	^
ALL 11'S TO 11/23+		4.0	4.5*
LCP 5, 8 (F-11 BASED)	3.3	.3	1.3*
ORION U, Q (J-11 BASED)	9.4	.4	2.4*
16B SOFTWARE	44.4	^	^
AZTEC I & II	17.2	1.4@	5.7
HSC & BSA CHANNELS/ADAPTORS	14.2	.3	.8
RA81, RAXX, RAXY (LARGE DISKS)	33.1	1.3	7.7
TA78, TU80, TU/TA81 (IND. TAPES)	4.2	1.2	2.5
SM. DIAM. DISKS (RX, RD)	9.6	1.3	1.8
SHRIMP (5 1/4" WINI)	5.4	-	3.0
MAYA (SM HI CAPACITY TAPE)	13.9	.1	3.3
RA60 (PINION & REMOVABLE DISK)	4.1	1.0	1.7
CT/CAT/DECMATE II	52.2	9.8*	?
TOTAL VIDEO FAMILY	26	1.8	4.2
TOTAL HARDCOPY	29.3	1.5	2.2
WORKSTATION (INCL. 32B, ETC.)	15.6	.6	1.6
U.Q BUS OPTIONS +1.4			
NI. ETHERNET HDW +3.9			
DECNET & X.25 SW +2.3			
SERVERS & GATEWAYS +3.0			
TOTAL DISTRIBUTED SYSTEMS	°75.2	^?	^?
36 BIT SYSTEMS PROGRAM	33.4	.7	1.6
CTAB/OFFICE +2.2			
TOTAL OFFICE PROGRAM	23.5	?	?
COEXISTANCE 20/VAX +1.0			
TOT. COEXIST., TOOLS, X-PROD. SW	8.5		
SEMICONDUCTOR PRODUCTS	31.7**		
SEG TOOLS & ADV DEV	19.7**		
PROCESS TECHNOLOGY	31.5		

NOTES:

? No estimate of revenue
^ Included in systems revenue
@ Most of the disk revenue is included in the systems revenue
+ FY83 $M
* Eli Glazer estimate
o Includes all Non-Product Expenses
** Does not include manufacturing process engineering investment

* * * * * * * * *
* d i g i t a l *
* * * * * * * * *

MEMORANDUM

TO: Win Hindle
Bill Thompson

CC: Gordon Bell
Jack Smith
Rick Corben

DATE: 2 APRIL 1982
FROM: JOSEPH REILLY
EXT: 223-6883
DEPT: CE FINANCE
LOC/MS: ML12-2/A16

SUBJECT: ENGINEERING DEVELOPMENT SUMMARY - IRR'S

Attached FYI are the internal rates of return for the products that correspond with Gordon's presentation to the Operations Committee.

Please note the following:

- IRR does not recognize that some products 'piggyback' on the investment of others (i.e., the DMR11 used a lot of the development technology of the DMP11).
- The IRR'S will change sometimes significantly as BURPS are updated with changes (i.e., pricing, volume, timing, etc.).

RLO.4.10

ENGINEERING DEVELOPMENT SUMMARY
IRR'S

GROUP	PRODUCT	IRR %	MOST RECENT RUN DATE
32-BIT	11/780	53	2/82
	11/750	45	2/82
	11/730	63	2/82
	VENUS	41	12/81
	NAUTILUS	--	Available Q1 FY83
	SCORPIO	--	Available Q4 FY82
	MICROVAX	--	Available Q4 FY83
	WORKSTATION	--	Available Q4 FY83
16-BIT	11/24	71	11/80
	11/44	89	3/79
	11/23+	91	1/82
	LCP-5	59	2/82
	LCP-8	85	12/81
	ORION-U	147	9/81 (1st pass soft)
	ORION-Q	147	9/81 (1st pass soft)
STORAGE	AZTEC I	39	3/82
	AZTEC II	--	N/A
	HSC-50	35	11/81
	BSA	--	N/A
	TA78	--	N/A
	TU80	33	1/82
	TU/TA81	--	N/A
	RX50	29	9/81
	RD50	67	12/81
	SHRIMP	--	N/A
	MAYA	--	N/A
	RA60	41	3/82
	RA80	47	3/82
	RAXY	--	N/A
	RAXY	--	N/A
TERMINALS & WORKSTATIONS	CT-100	48	11/81
	VT100	33	6/80
	VT101/102/131	55	4/81

GROUP	PRODUCT	IRR %	MOST RECENT RUN DATE
TERMINALS & WORKSTATIONS	VT210	65	2/82
	LA100	47	11/80
	LA12	37	6/81
	LA120	31	6/80
	LA36	31	6/80
	LA180	31	6/80
	LA34	23	6/80
DISTRIBUTED SYSTEMS			
U/Q BUSOPTIONS			
	DMR11	53	10/80
	DPV11	25	8/80
	DMP11	19	9/81
	D232	39	4/81
	DMV11	16	9/81
	DMF32	83	3/82
NI ETHERNET H/W			
	TRANSCEIVER	39	1/82
	PLUTO HDW	--	Available Q4 FY82
	UNA	43	
DECNET S/W			
	RSX V3.1	60	2/82
	RSX V4.0	--	Available Q2 FY83
	VMS V3.B	--	Available Q2 FY83
	CT	--	Available Q4 FY83
SERVERS & GATEWAYS			
	PLUTO SYST	--	Available Q3 FY83
32-BIT	JUPITER	35	1/82
SOFTWARE			
OF15 PROGRAM			
	DECMAIL	46	3/82
	OFIS/VMS	36	3/82
	OFIS/CTAB	16	3/82
	OFIS/RSTS	55	3/82

ENGINEERING DEVELOPMENT SUMMARY

PRODUCT		ENG. $M '83 - '85	IRR
11/780, 11/750, 11/730		28.1	
VENUS		42.4	
NAUTILUS		23.8	
SCORPIO		22.0	
MICROVAX		13.0	
VMS FAMILY SOFTWARE		95.5*	
ALL 11'S TO 11/23+			
LCP 5, 8 (F-11 BASED)		3.3	
ORION U, Q (J-11 BASED)		9.4	
16B SOFTWARE		44.4	
AZTEC I & II		17.2	
HSC & BSA CHANNELS/ADAPTORS		14.2	
RA81, RAXX, RAXY (LARGE DISKS)		33.1	
TA78, TU80, TU/TA81 (IND. TAPES)		4.2	
SM. DIAM. DISKS (RX, RD)		9.6	
SHRIMP (5 1/4" WINI)		5.4	
MAYA (SM HI CAPACITY TAPE)		13.9	
RA60 (PINION & REMOVABLE DISK)		4.1	
CT/CAT/DECMATE		52.2	
TOTAL VIDEO FAMILY		26.0	
TOTAL HARDCOPY		29.3	
WORKSTATION (INCL. 32B, ETC.)		15.6	
U.Q BUS OPTIONS	+ 1.4		
NI. ETHERNET HDW	+ 3.9		
DECNET & X.25 SW	+ 2.3		
SERVERS & GATEWAYS	+ 3.0		
TOTAL DISTRIBUTED SYS.		75.2	
36 BIT SYSTEMS PROGRAM		33.4	
CTAB/OFFICE	+ 2.2		
TOTAL OFFICE PROGRAM		23.5	
COEXISTANCE 20/VAX	+ 1.0		
TOT. COESIST., TOOLS, X-PROD. SW		8.5	
SEMICONDUCTOR PRODUCTS		31.7**	
SEG TOOLS & ADV DEV		19.7**	
PROCESS TECHNOLOGY		31.5	

* Eli Glazer Estimate

** Does not include manufacturing process engineering investment.

RL0.4.9 - April 1982

	Direct	CE	
uPG	4.3	3.3	
Toem		2.2	
WP		10.8	
TPG.	10.1	}	
MSG.	1.8		
LDP	5.5		
TPL	1.0		
ECS	1.6		
ESG	2.9		
GSG	2.8		
LGG.	1.4		
Coem.	4.0		
esa	.9		
PGi	4.5		
MDC	5.3		
TiG	6.6	3.8	
AsfG			
ESS	6.		
	58.7	20.1	

****
* d i g i t a l *
****

TO: OPERATIONS COMMITTEE:

cc: GROUP CONTROLLERS:

DATE: MON 10 MAY 1982 5:19 PM EDT
FROM: SHELDON ARONOFF
DEPT: CORP FIN PLNG & ANAL
EXT: 223-8707
LOC/MAIL STOP: MS/G15

SUBJECT: MAY BUDGET WOODS

This is to confirm the conversation at today's Operations Committee on the FY83/84 Budget Proposals.

The proposals as submitted are unacceptable.

- Volumes look high compared to current order rates and uncertainty in the economy.
- Strategic Plan Direct margin goals have not been achieved by most of the Planning Units. (Product Groups, Europe)
- Spending generally does not meet the 11% per annum productivity improvement goal established by Operations Committee.

Operations Committee members and/or their direct reports will present revised proposals at the May Woods that meet the agreed to goals.

The proposals will make visible the following:

- Rationale justifing the volume proposal, including visibility on quarterly ramps.

- Spending meeting the 11% per annum productivity improvement test agreed to by Operations Committee.

- Specific investments that prevent achieving the direct margin goal and/or the productivity improvement goal, with clear indications of their cost/benefit.

- The highly recommended lists, by category, and the annual dollars tied to same.

- The performance standards established in the group to distinguish exceptional performance from satisfactory performance and from unsatisfactory performance.

Detailed changes to Budget proposals can be accepted through tommorrow noon by the budget system. The data, as of that time, will be incorporated into the Budget Package to be distributed to Operations Committee later this week.

However, I will process revised commitments communicated to me via memo/EMS through Monday, May 17. This will allow me to have available for Operations Committee a "base" corporate proposal at the Woods.

lms

timelines IS NOT Schedule

EG:kr4.10

ENGINEERING DEVELOPMENT SUMMARY

PRODUCT	ENG $M Σ'83 -'85	NOR $B Σ'82 -'86	NOR $B LIFETIME
~~11/780~~, ~~11/750~~, 11/730 /11/782	28.1	12.8	17.9
VENUS	42.4	1.8	10.2
NAUTILUS	23.8	.2	11.9
SCORPIO (incl. chip) B-/D B/B+	22.0	.3	6.0
MICROVAX	13.0	?	?
VMS FAMILY SOFTWARE — A/B+	95.5*	↑	↑
ALL 11'S TO 11/23+		4.0	4.5*
LCP 5, 8 (F-11 BASED)	3.3	.3	1.3*
ORION U, Q (J-11 BASED)	9.4	.4	2.4*
16B SOFTWARE	44.4	↑	↑
AZTEC I & II B+/C+	17.2	1.4@	5.7
HSC & BSA CHANNELS/ADAPTORS A/B-	14.2	.3	.8
RA81, RAXX, RAXY (LARGE DISKS) A+/A	33.1	1.3	7.7
TA78, TU80, TU/TA81 (IND. TAPES) C/C	4.2	1.2	2.5
SM. DIAM. DISKS (RX, RD)	9.6	1.3	1.8
SHRIMP (5 1/4" WINI) ? B-/	5.4	-	3.0
MAYA (SM HI CAPACITY TAPE) ?	13.9	.1	3.3
RA60 (PINION & REMOVABLE DISK) A/A	4.1	1.0	1.7
CT/CAT/DECMATE II B/D	52.2	9.8*	?
TOTAL VIDEO FAMILY B/D	26	1.8	4.2
TOTAL HARDCOPY B+/B	29.3	1.5	2.2
WORKSTATION ~~(INCL. 328, ETC.)~~ B/C	15.6	.6	1.6
U.Q BUS OPTIONS — B/B +1.4			
NI. ETHERNET HDW — B/C +3.9			
DECNET & X.25 SW — ~~B/B+~~ ~~+2.3~~ A-/B+			
SERVERS & GATEWAYS — +3.0			
TOTAL DISTRIBUTED SYSTEMS B-/C+	°75.2	↑?	↑?
36 BIT SYSTEMS PROGRAM 20 to SW A+/C+ C+/B	33.4	.7	1.6
CTAB/OFFICE Offic +2.2 — B+/B+			
TOTAL OFFICE PROGRAM PW WPS — ~~23.5~~ B-/C-		?	?
COEXISTANCE 20/VAX +1.0			
TOT. COEXIST., TOOLS, X-PROD. SW	8.5 A	B-	
SEMICONDUCTOR PRODUCTS ~~B/B~~ B-/C+	31.7**		
SEG TOOLS & ADV DEV — B+/B	19.7**		
PROCESS TECHNOLOGY	31.5		

(except Semi Slip)

NOTES:

? No estimate of revenue
↑ Included in systems revenue
@ Most of the disk revenue is included in the systems revenue
+ FY83 $M
* Eli Glazer estimate
o Includes all Non-Product Expenses
** Does not include manufacturing process engineering investment

PRODUCT	ENG. AM Σ '83-'85	NORTH Σ '82-'86	NORTH LIFETIME
11/780, 11/750, 11/730	28.1	12.8	17.9
VENUS	42.4	1.8	10.2
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16B SOFTWARE	44.4		
AZTEC I & II	17.2	1.4	5.7
HSC + BSA ADAPTORS	14.2	.3	.8
RA81, RAXX, RAXY (LARGE DISKS)	33.1	1.3	7.7
TA78, TU80, TU/TA81 (INDUSTRY TAPES)	4.2	1.2	2.5
SM. DIAM. DISKS (RX, RD)	9.6	1.3	1.8
SHRIMP (5¼" WINI)	5.4	—	3.0
MAYA (SM HI CAPACITY TAPE)	13.9	.1	3.3
RA60 (PINION + REMOVABLE DISK)	4.1	1.0	1.7
CT/CAT/DECMATE II	52.2	9.8*	
TOTAL VIDEO FAMILY	26	1.8	4.2
TOTAL HARDCOPY	29.3	1.5	2.2
WORKSTATION (INCL 32B etc)	15.6	.6	1.6
U.Q BUS OPTIONS +1.4			
NI - ETHERNET HDW +3.9			
DECNET + X.25 SW +2.3			
SERVERS & GATEWAYS +3.0			
TOTAL DISTRIBUTED SYSTEMS	⊖75.2		
36 BIT SYSTEMS PROGRAM	33.4	.7	1.6
CTAB/OFFICE +2.2			
TOTAL OFFICE PROGRAM	23.5		
COEXISTANCE 20/VAX +1.0			
TOTAL COEX., TOOLS, CROSS PRODUCT. SW	8.5		
SEMI CONDUCTOR PRODUCTS	31.7**		
SEG TOOLS & ADV DEV	19.7**		
PROCESS TECHNOLOGY	31.5		

* EG estimate | + FY83 $M | ⊖ INCLUDES ALL NON PRODUCT EXPENSES | ** ?

the corridor talk at most OEM trade shows deals with just that issue. His advice to emerging OEMs: "Pick a vertical market, stick to it and do a good job, and you won't have a problem."

Daniel Vertrees, vice president for Digital Systems of Florida, one of the larger OEMs, agrees. By developing specialized DEC-based systems for certified public accountants, law offices and contractors, Vertrees says his company has been able to carve out markets which DEC, with its general-purpose software, has yet to penetrate. With $37 million in sales in 1981 and "shooting for $50 million in 1982," Digital Systems is DEC's "number-one stepchild, whether they like it or not," Vertrees says.

Sandra Kurtzig, president of ASK Computer Inc., Hewlett-Packard's largest OEM, says most hardware vendors are dying to get into ASK's two main markets — turnkey systems utilizing manufacturing and financial-management software. She notes that end users are "buying solutions, not hardware," however, and that gives ASK the edge — from both technological and marketing standpoints — over the computer makers. In addition, an OEM such as ASK, which buys hardware from HP and DEC, is not limited to any one vendor's product line, but can match its own software to a customer's needs and/or hardware preference.

With all the problems ahead, no one is likely to give up too soon on the OEM minicomputer sector — least of all Data General, ranked by IDC second, after DEC, in OEM shipments and third in revenues. According to Donald McDougall, acting general manager of Data General's Technical Products Division, "Productivity-related products used in computer-aided design and manufacturing, numerical control, robotics and automatic test equipment" will be the OEM "areas that are going to be the most interesting" for minicomputer makers in the next five to 10 years.

Board business booming

After minicomputers, board-level, or single-board, computers represent the next biggest tier of OEM business After slowing down somewhat in th early months of the recession, sal suddenly rebounded in the fou quarter of 1981, reports Ral Gilman, a senior analyst at Dataq Inc.

Robert Brannon, general man

Financial data on the top OEM minicomputer makers

	Totals for the company or for the closest division that includes OEM minicomputers		Total company revenues ($ million)	Cost of sales (mfg. cost as % of sales)	Per employee		R&D as a % of total revenues
	Sales ($ million)	Net income (% of sales)			Total revenues	Net income	
Computer Automation	$ 75.6	2.2%	$ 75.6	50.8%	$65,796	$1,480	9.6%
Data General	736.9	6.9%	736.9	51.9%	50,386	3,464	10.1%
Digital Equipment	3,198.1	10.7%	3,198.1	55.6%	50,763	5,449	7.9%
General Automation	86.5	N.A.	124.9	66.0%	69,000	68	3.8%
Gould	1,846.1	5.2%	1,846.1	N.A.	N.A.	N.A.	N.A.
Harris	258.6	8.4%	1,551.5	65.8%	60,136	4,031	5.3%
Hewlett-Packard	1,771.0	9.7%	3,578.0	47.6%	55,906	4,875	9.7%
Honeywell	1,773.7	6.3%	5,351.2	64.0%	55,211	2,675	6.9%
IBM	19,109.0	13.4%	29,070.0	41.3%	81,902	9,320	5.5%
Modular Computer	87.2	1.3%	87.2	N.A.	N.A.	N.A.	N.A.
Perkin-Elmer	232.5	5.4%	1,115.8	56.5%	72,447	5,072	7.5%
Prime Computer	364.8	10.3%	364.8	43.8%	78,686	8,127	7.5%
Sperry	2,707.4	6.2%	5,427.2	60.2%	58,687	3,385	6.2%
Tandem	208.4	12.7%	208.4	36.3%	76,336	9,725	8.6%
Texas Instruments	1,064.0	1.5%	4,206.0	77.0%	50,242	1,296	5.2%

Data based on latest annual report ending before Dec. 31, 1981

N.A.—not available

****
* d i g i t a l *
****

TO: CE CONTR. STAFF:
EMC:
PEG:

DATE: TUE 18 MAY 1982 9:13 AM EDT
FROM: JOE REILLY
DEPT: CE FINANCE
EXT: 223-6883
LOC/MAIL STOP: ML12-2/A16

SUBJECT: FY'83 BUDGET

RLo:SECT6/5.42

The EMC approved the following budget:

GROUP	
16 Bit	13.5
Terminals & WS	34.5
32 Bit	42.0
Distributed Systems	21.0
LSG	36.7
Storage	53.9
Software	61.3
SEG	20.9
TOPS	7.5
Process Tech	9.2
SA&T	11.9
Sites	10.0
Central & Other	19.7
West Coast	
CMU	4.5
Japan	
TOTAL	346.6

SUMMARY

- All groups will deliver their 'A' Scenario.
- New requests must be funded by tradeoffs of current scenario.
- There is no Contingency or General Technology Fund.
- Japan, CMU, West Coast total cannot exceed 4.5 MEG.
- Each group will quarterize their own numbers.

18-MAY-82 09:20:57 S 2494 EMML

ENGINEERING OVERVIEW

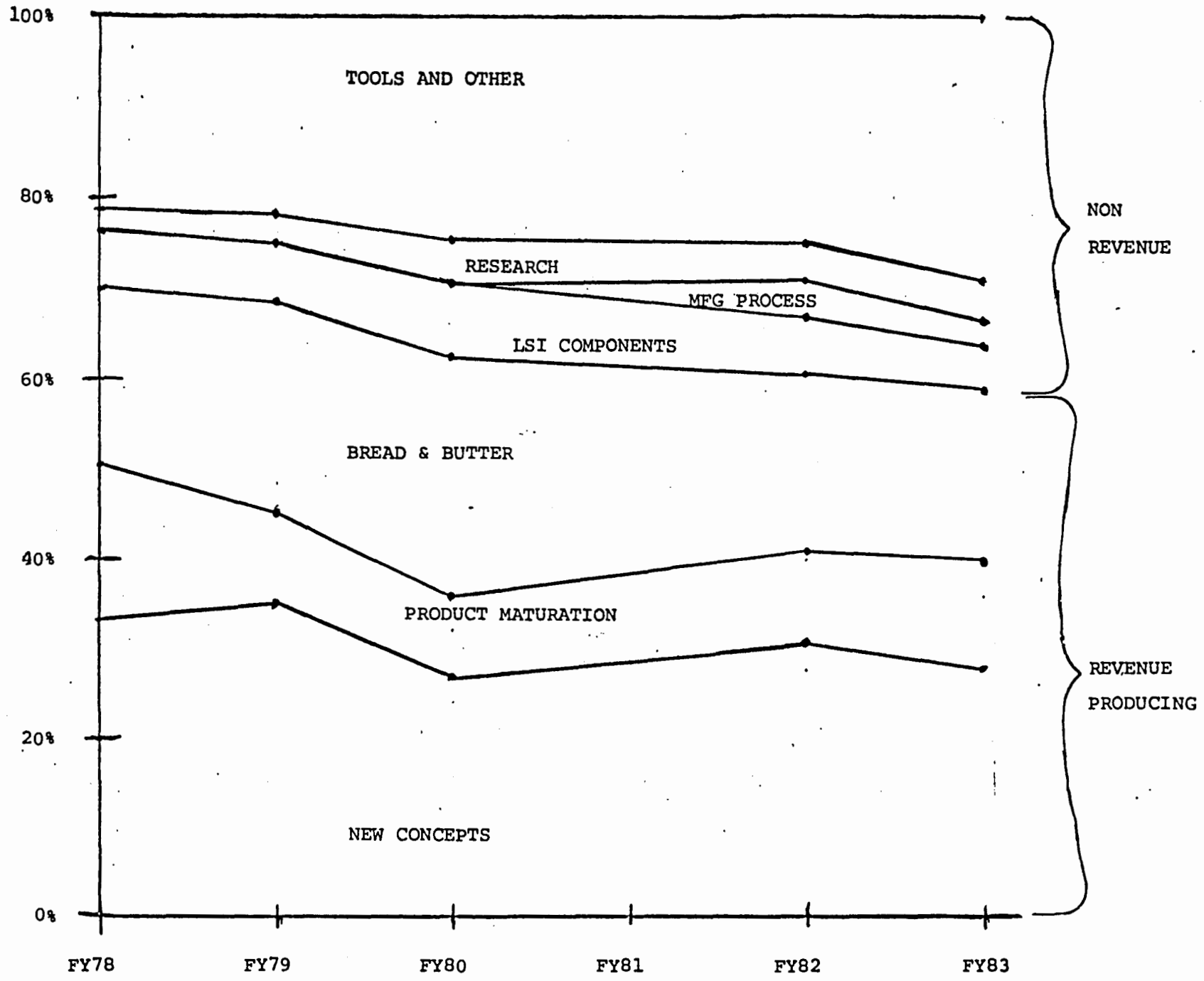
- CATEGORY SPENDING
- INVESTMENT VS. REVENUE SPENDING
- COST STRUCTURE CHANGES
- PEOPLE GROWTH PROFILE
- COMPETITIVE SPENDING
- BUDGET BY MAJOR GROUP
- PEOPLE ADDS BY TYPE

CATEGORY OF ENGINEERING INVESTMENT

REVENUE/NON-REVENUE CATEGORY	TYPE OF ENGINEERING	EXAMPLES
REVENUE GENERATING ENGINEERING PROJECTS	• EMERGING CONCEPTS	- LA36 - VIDEO IN 1973 - VAX IN 1975 - LSI-11 IN 1976 - ETHERNET IN 1981 - CT IN 1982
	• PRODUCT MATURATION	- MICRO PASCAL SW - VMS IN 1980 - DECNET SW - VT101 IN 1981
	• BREAD & BUTTER	- DEC 10/20 IN 1975 - PDP-11 IN 1976 - VMS IN 1982 - PRINTERS LA100
NON-REVENUE ENGINEERING PROJECTS	• COMPONENT*	- SEMI-CONDUCTOR*
	• PROCESS	- MFG PROCESSES AND SYSTEMS
	• ADVANCED RESEARCH	- GENERALLY UNDER SAM FULLER'S "SATR" DIRECTION
	• TOOLS AND MISCELLANEOUS	- CAD - ENGINEERING PARTS LIBRARY

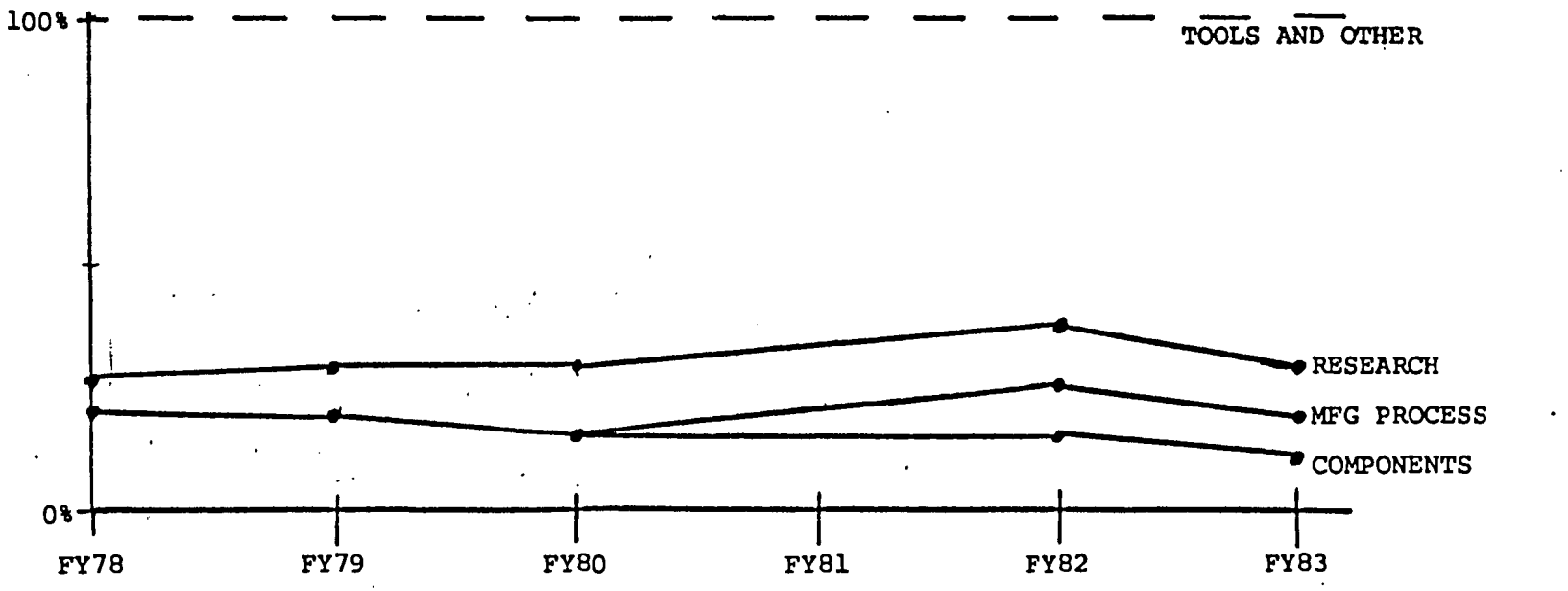
*COULD INCLUDE CHIPS AS AN EMERGING REVENUE PRODUCT

EG:kr4.14

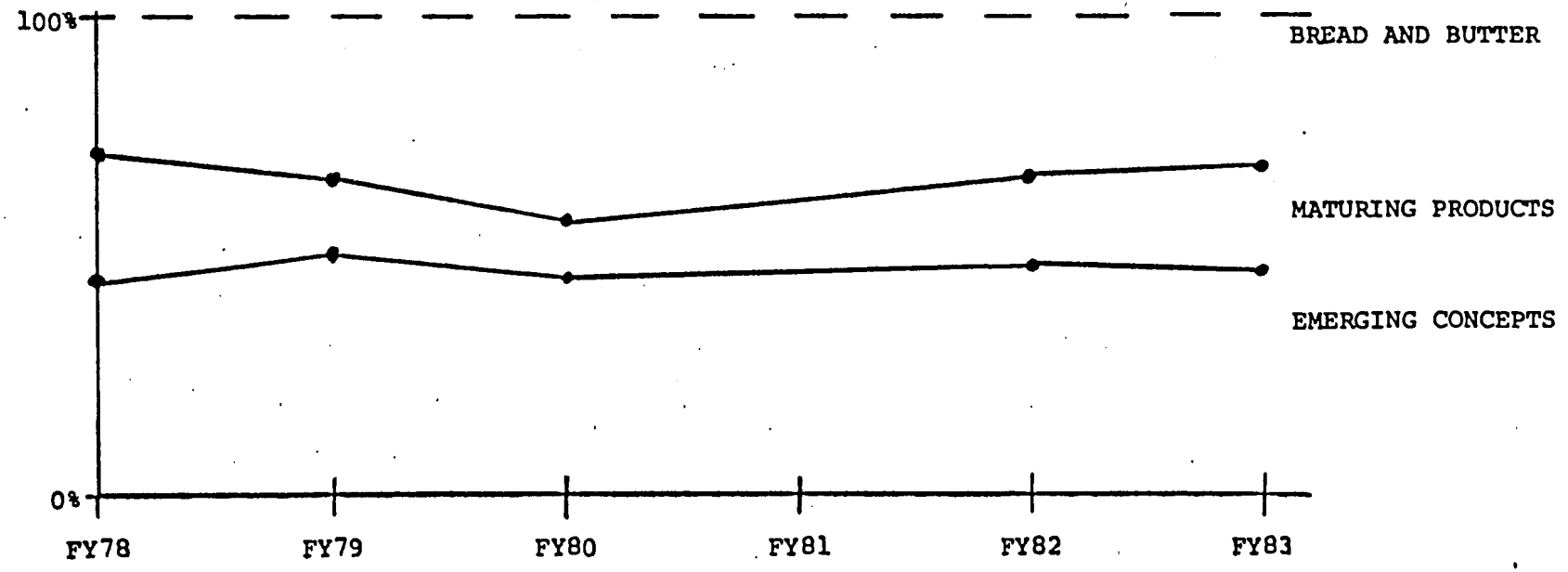


% OF INVESTMENT BY REVENUE GROWTH CATEGORY

NON REVENUE



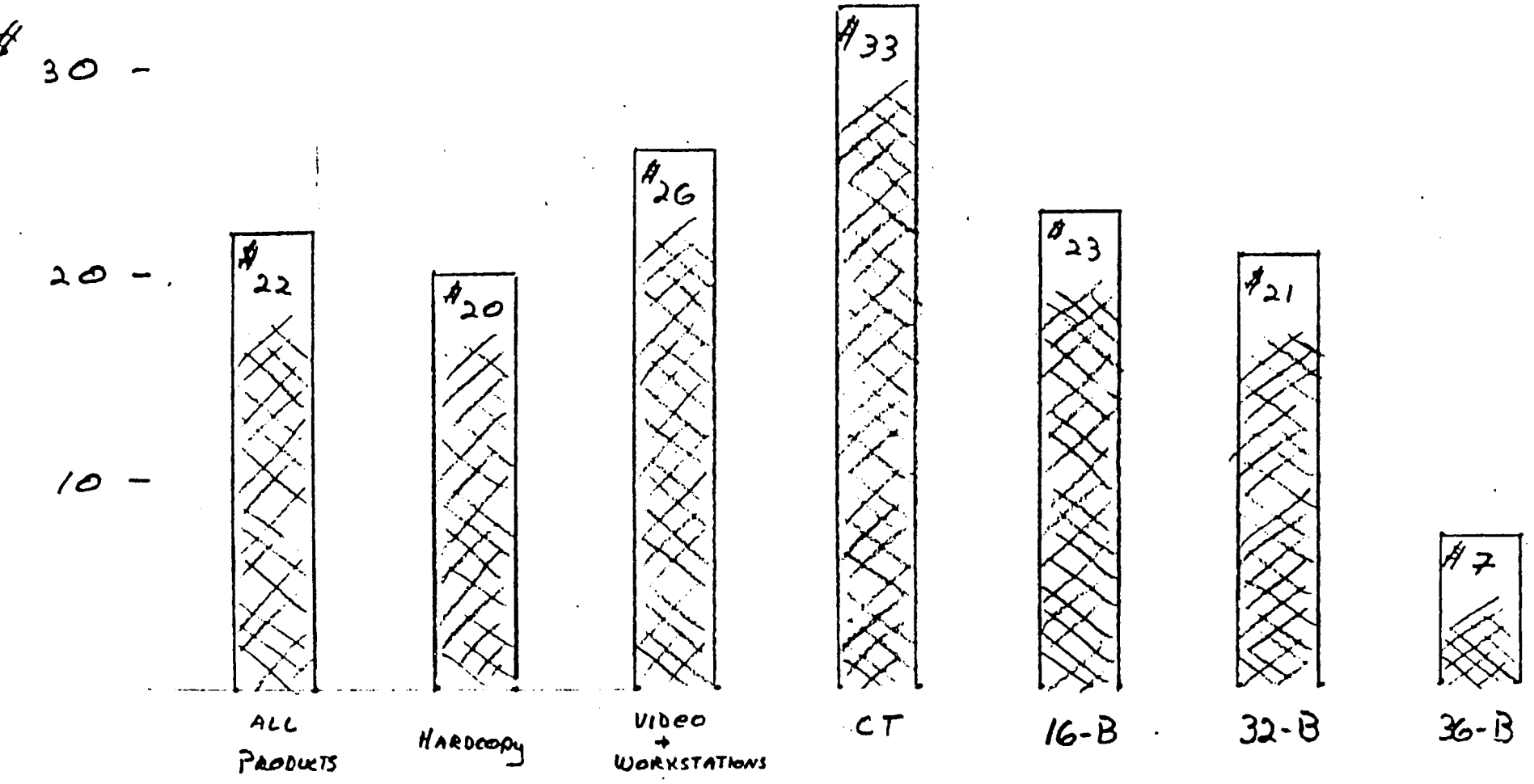
REVENUE



% OF INVESTMENT WITHIN REVENUE AND NON REVENUE CATEGORIES

Revenue per Dollar of E&G Investment

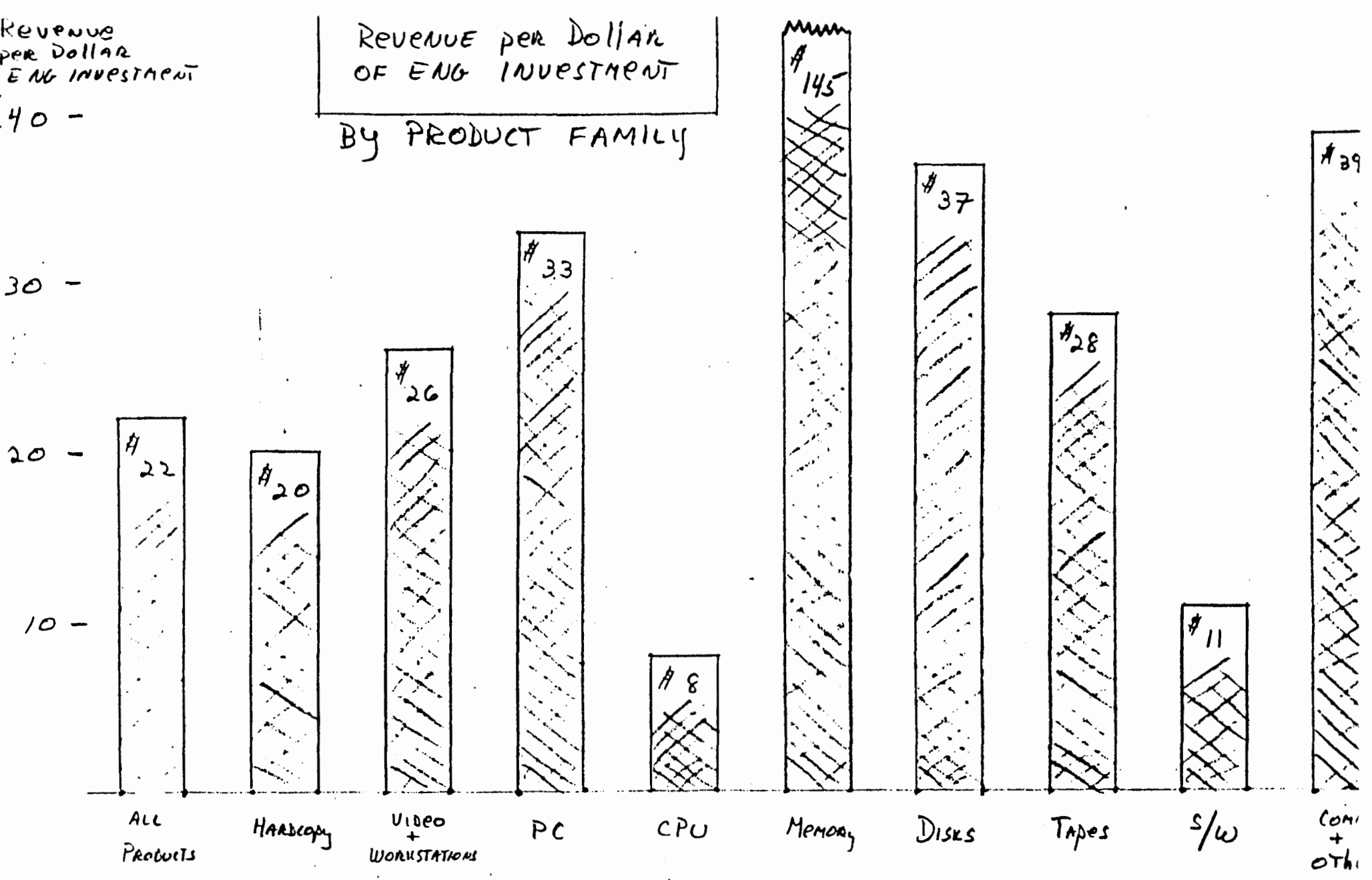
By ARCHITECTURE



T Equipment Sales							
e Annual 84→86)	# 7500	200	500	1150	1450	4000	250
E&G Investment	# 346	10	19	35	62	186	34

D. Clinton

Revenue per Dollar of ENG Investment
By Product Family

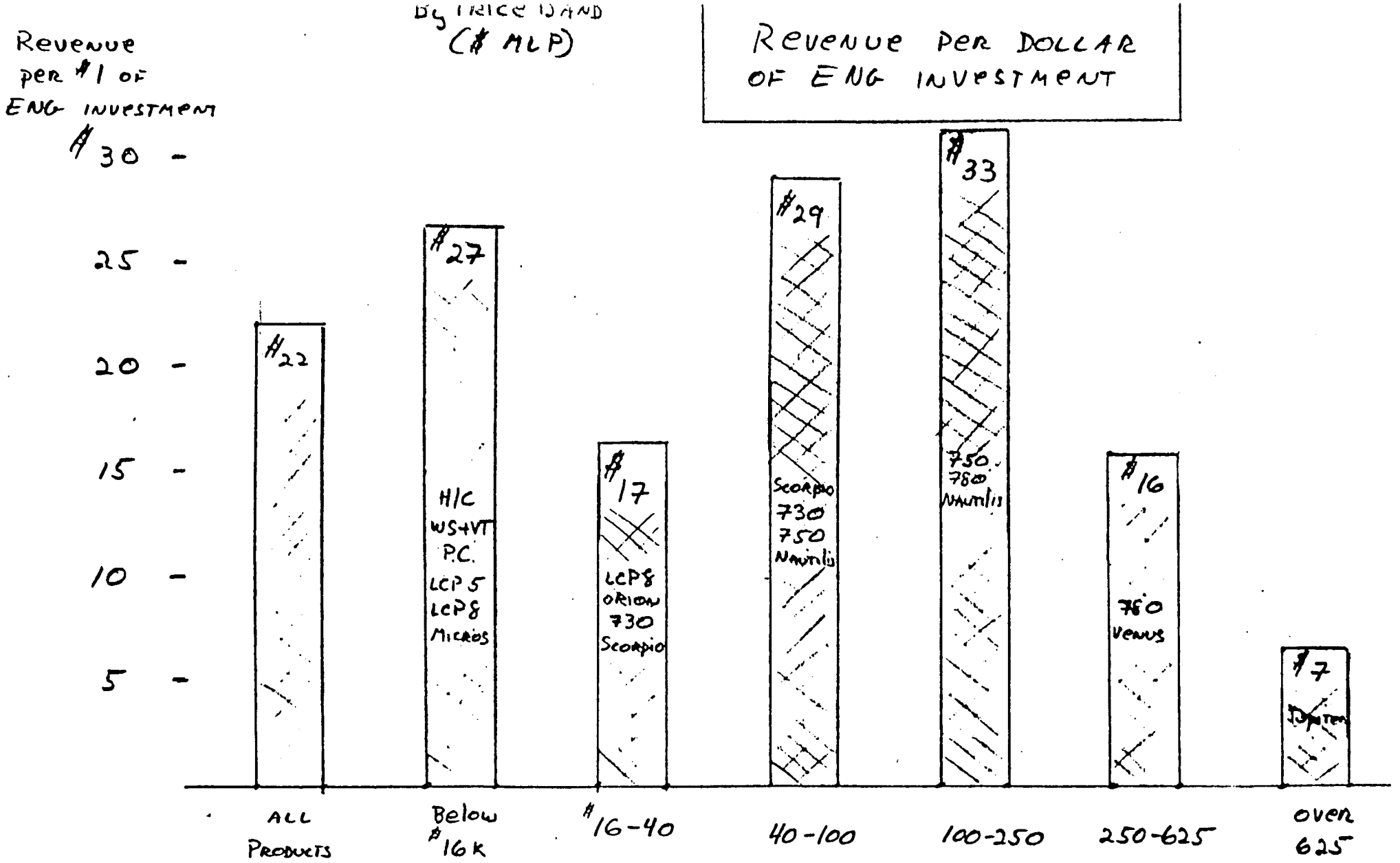


	All Products	Hardcopy	Video + Workstations	PC	CPU	Memory	Disks	Tapes	S/W	Com + Oth
Equip. Sales (ANN 84→86)	$7500	200	500	1150	950	725	2000	225	850	90
ENG Investment	$346	10	19	35	117	5	54	8	75	2

D. Clinton

By Price Band
(# MLP)

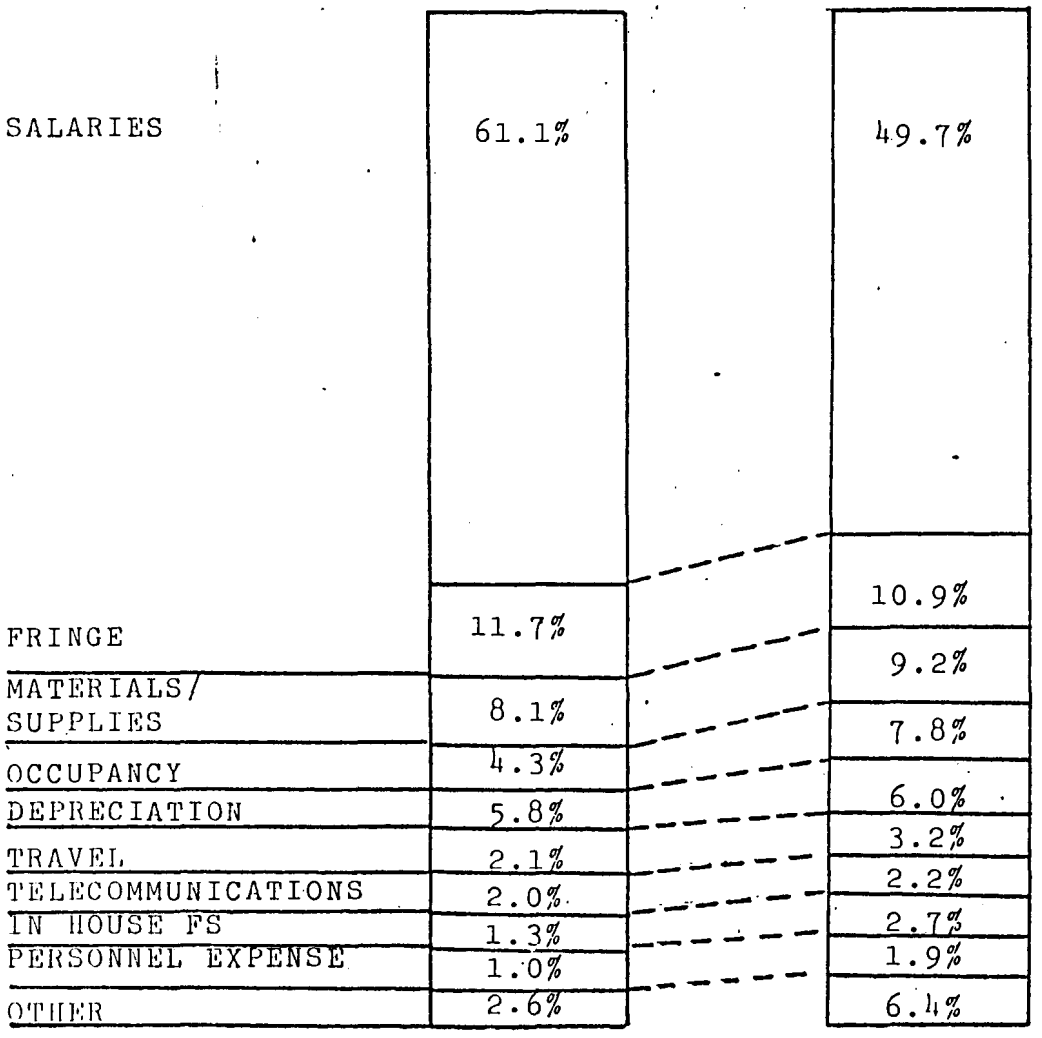
Revenue per Dollar of ENG Investment



	ALL Products	Below #16K	#16-40	40-100	100-250	250-625	over 625
et Equipment Sales ie annual 84→86)	$7500	2400	900	1600	1000	1400	250
3 ENG Investment	346	88	54	55	30	85	34

D. Clinton

CENTRAL ENGINEERING
COST STRUCTURE PROFILE
FY'78 - FY'82



FY'78
$ 79.6M

FY'82
$ 270.2M

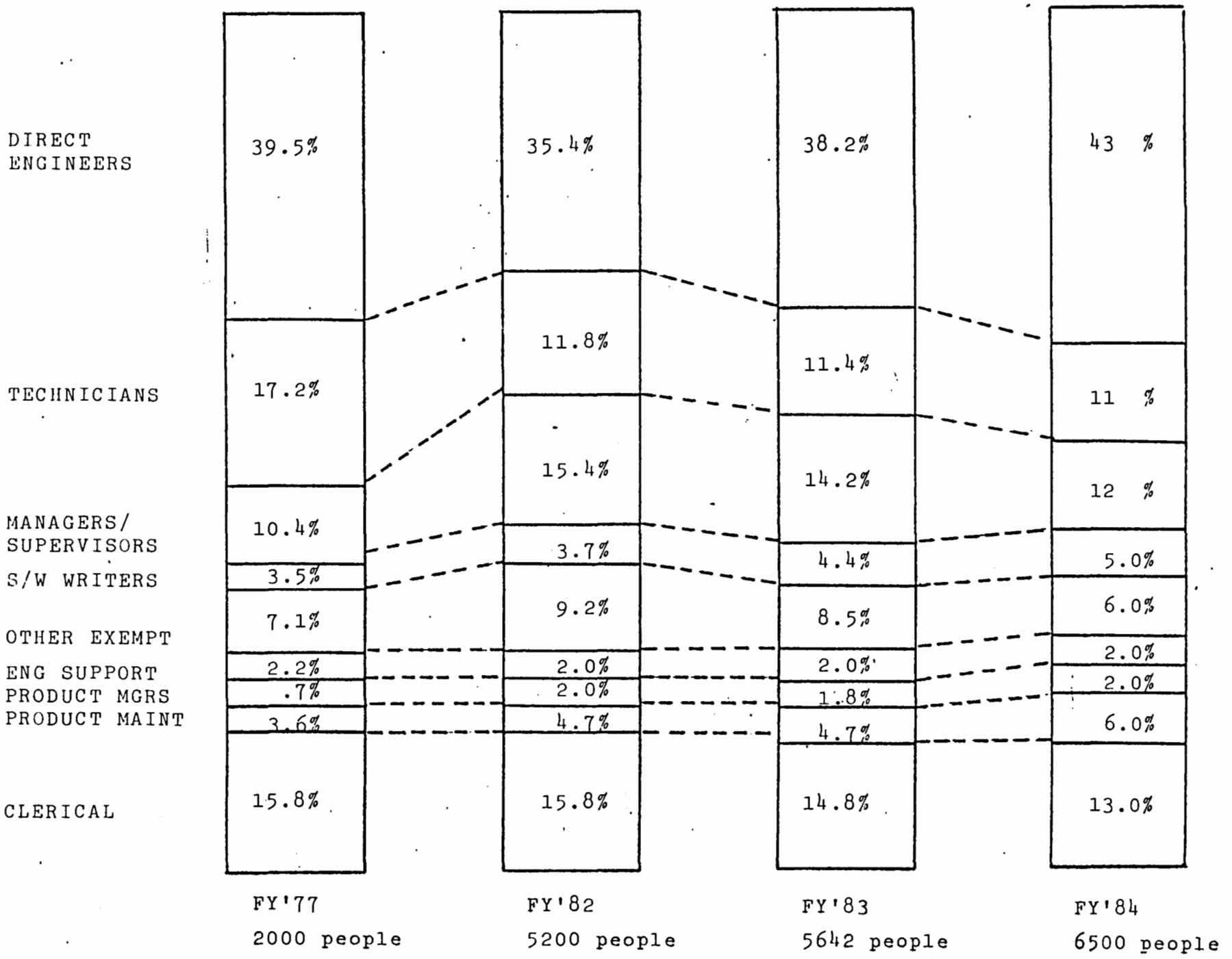
SALARIES	29.3
FRINGE	33.6
MATERIALS/ SUPPLIES	41.0
OCCUPANCY	59.5
DEPRECI-ATION	37.5
TRAVEL	51.4
TELECOMMU-NICATION	39.5
IN HOUSE FS	48.0
PERSONNEL	58.1
OTHER	68.7

COMPOUNDED GROWTH RATE	36.9%

WHAT IS DRIVING OUR CHANGING COST STRUCTURE?

- EXPANSION/DECENTRALIZATION
- NEW PRODUCTS
- TOOLS FOR NEW TECHNOLOGIES
- PRODUCTIVITY TOOLS
- INTER AND INTRA SITE COMMUNICATIONS
- INCREASE IN CAPITAL INTENSITY AND RESULTING LAB SPACE
- UTILIZATION AND COST OF INTERNAL SERVICES RISING SHARPLY

ENGINEERING PEOPLE PROFILE



	FY 71	FY 72	FY 73	FY 74	FY 75	FY 76	FY 77	FY 78	FY 79	FY 80	FY 81	EST. FY82	EST. FY83
APPLE	-	-	-	-	-	-	-	7.6	7.5	6.2	NA		
BURROUGHS	5.0	5.1	5.1	5.6	5.9	5.7	5.8	5.8	6.0	6.7	6.5		
COMMODORE	-	-	-	-	-	1.5	3.0	4.1	5.0	5.3	4.5		
CONTROL DATA	5.8	4.4	5.1	5.8	4.0	4.3	4.8	5.8	6.6	6.6	NA		
DATAPOINT	31.6	14.8	4.6	5.2	5.8	5.6	6.2	7.2	7.8	8.7	NA		
DIGITAL	11.4	10.7	9.4	8.7	9.1	7.9	7.5	8.1	7.7	7.9	7.9	9.2	9.4
DATA GENERAL	10.2	10.4	11.2	10.2	10.8	10.3	10.2	10.1	10.0	10.0	10.1		
HONEYWELL	7.0	6.9	6.7	6.5	5.9	5.0	5.2	5.2	5.6	6.0	6.9		
HP	10.5	9.2	8.6	7.9	9.1	9.6	9.2	8.9	8.6	8.8	9.7		
IBM	6.5	7.1	6.6	7.0	6.6	6.2	6.3	6.0	5.9	5.8	5.5		
INTEL	16.9	14.7	6.9	7.8	10.6	9.2	9.9	10.4	10.1	11.3	14.8		
NCR	3.5	3.8	2.9	3.7	3.9	4.0	5.0	5.3	5.7	6.1	6.7		
PRIME	-	-	31.9	10.8	7.7	6.9	6.1	8.3	7.9	7.6	7.5		
SPERRY	5.4	5.5	5.7	6.0	5.3	4.9	5.1	5.3	5.7	5.8	6.1		
TANDEM	-	-	-	-	-	168.5	14.2	8.9	8.3	8.0	8.6		
TI	-	-	-	4.1	3.7	4.4	4.7	4.4	4.2	4.6	5.2		
WANG	2.5	4.3	3.8	3.3	4.4	4.4	4.9	4.4	5.1	6.7	7.8		
FUJITSU									10.1	9.4	9.2		
TOSHIBA									3.3	3.6	3.5		
NEC									4.5	5.1	4.7		
HITACHI									3.6	3.7	3.8		

SOURCE: COMPETITIVE ANALYSIS SYSTEM; FINANCIAL STRATEGY GROUP

COMPETITIVE R&D SPENDING

COMMENTS:

- DEC'S R&D % HIGH IN EARLY 70'S

FY71	11.4%
FY72	10.7%
FY73	9.4%

- OUR STRONG COMPETITORS ARE INVESTING IN R&D

	FY81
FUJITSU	9.2
H/P	9.7
WANG	7.8 (UP FROM 4.4 IN FY78)

- IBM SHOWS 5.5% IN FY81 HOWEVER WHEN THEIR NOR IS ADJUSTED TO "IF-SOLD" BASIS THEY APPEAR HIGHER THAN DEC

- OTHER COMPETITORS OVERSTATE R&D

	EXTERNAL REPORTING	INTERNAL REPORTING
DATA GENERAL	10.0%	7.1%
BURROUGHS	6.5%	5.1%

ENGINEERING BUDGET

GROUP	($M)
16 BIT	13.5
TERMINALS & WS	34.5
32 BIT	42.0
DISTRIBUTED SYSTEM	21.0
LSG	36.7
STORAGE	53.9
SEG	20.9
TOPS	7.5
PROCESS TECH	9.2
SA&T	11.9
SITES	10.0
CENTRAL & OTHER	19.7
WEST COAST	
CMU	4.5
JAPAN	
	346.6

ENGINEERING BUDGET

PEOPLE ADDS

DIRECT ENGINEERS	306
SOFTWARE WRITERS	61
TECHS	30
OTHER *	45
	442

*JANITORS, GUARDS, NURSES, CLERICAL FOR NEW FACILITIES

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* d i g i t a l *
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TO: see "TO" DISTRIBUTION

DATE: WED 26 MAY 1982 7:41 AM EDT
FROM: GORDON BELL
DEPT: ENG STAFF
EXT: 223-2236
LOC/MAIL STOP: ML12-1/A51

SUBJECT: REVIEW OF PRODUCTS AND PROJECTS WE SHOULDN'T BE DOING

EMC is going to do a full scale review of the projects we are doing and have to do a forced ranking of the projects in order to reduce the engineering budget.

I'd like to solicit a listing of the non-critical things from within engineering, especially our senior consulting engineers who know about both the quality and timeliness of them.

Some of the things that come to mind to be reviewed critically in the area of software revolve around make versus buy. Here, I am tremendously impressed with the CT program to get software such as NPL running on CT. Also, Personal Software is going to put their software on CT. These are major efforts ... need them, yet could not possibly have staffed up to get them done.

Some of the programs that I definitely do not think we should be doing are: DECSET (buy both TEX and SCRIBE); ANY manufacturing programs... we should buy all them ala ESG and test them; ADE (NPL and Visicalc are alternatives); DAWN; VISICALC (buy it!); PASCAL (we have one and ours is late and doesn't use the common compiler). APL... is it going to come out? I hesitate to mention it, but then there are the 4000 incompatible mail systems... any idea of how to deal with this one?

Conversely, there are languages such as RPG that should have been finished when we have the alternative to do it based on COBOL. I want to understand the function of the Commercial Systems Hardware group too.

Ken has raised concern about the plethora of experts running around, with tin cups that every group feels obliged to have. Of particular concern to me in this regard is ID and human factors and performance folks. The experts seem to take the need to design away from the designers who don't have to worry now about estetics, form or its usability.

These were just a few things that came to mind in the middle of the nite. Could I get a list of the projects and efforts that you think are unnecessary, redundant, going nowhere and that could be eliminated?

"TO" DISTRIBUTION:

RON BRENDER DAVE CUTLER DICK HUSTVEDT

PETER JESSEL	JESSE LIPCON	ROBERT MCKENZIE
AVRAM MILLER	PEG:	JACK SMITH
BILL STRECKER	STEVE TEICHER	WALT TETSCHNER

****
* digital *
****

TO: *GORDON BELL
JACK SMITH

DATE: THU 22 APR 1982 9:26 AM EST
FROM: GRANT SAVIERS
DEPT: STORAGE SYSTEMS
EXT: 223-5765
LOC/MAIL STOP: ML3-6/E94

SUBJECT: FY'83 BUDGET

Here's my list of "opportunities":

1. Central Engineering Admininstration-Reduce the staff. There are a few funtions (YE, Plans library, etc.) that are worthwhile, but I don't see a need for more than 1 or 2 super administrators to do the work. I note a few folks are looking for work, so it may be that I don't understand your plan. All "process" folks should go, along with EORC.

2. External Resources- There is substantial growth planned for central "watchers", technology circles, etc., I'd propose to cut the $1.5M plan by 50%, but not in the direct purchasing support of the development groups.

3. Westwing- The proposed premium over commercial aviation allocation to Puffer and me is $910K. (almost double FY'82!) Let's sell it!

4. Engineering MIS- I believe we lack some badly needed systems but also believe that existing management is having difficulty getting beyond the Popular Science "Managing Information as a Resource" level it's been at for some time.

5. The "centralized" diagnostic activity being started by Holman/Honsko should not be done.

FGS:pgh

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* d i g i t a l *
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TO: *GORDON BELL
JACK SMITH

DATE: FRI 14 MAY 1982 11:02 AM EDT
FROM: JEFF KALB
DEPT: LSI
EXT: 225-4025
LOC/MAIL STOP: HL2-2/M11

SUBJECT: OBSERVATIONS ON BUDGET CUTTING

* * * * * * * * *
* *
* d i g i t a l * INTEROFFICE MEMORANDUM
* *
* * * * * * * * *

TO: Gordon Bell
Jack Smith

DATE: 14 May 1982
FROM: Jeff Kalb
DEPT: LSI Administration
EXT: 225-4025
LOC: HL2-2/M11

SUBJECT: OBSERVATIONS ON BUDGET CUTTING

Per your request, I have jotted down my observatons on budget cutting. They are derived from 3 major budget cuts I've witnessed. In one case, upper management may direct program cuts and consoliidations. In the second, a much larger organization, there was a combination of upper management making cuts and middle management following the example by making further cuts with some squeezing. In the third, upper management just tried to squeeze again and again and opposed any real program cuts. The first two were successful and actually rejuvenating, while the third was a disaster. The first two got rid of marginal people (it was they who were left hanging) while the last resulted in a loss of a lot of the best people. Below are specific observations.

I'm obviously bias, so keep that in mind, but I subscribe to Peter Drucker's quote "Priorities are easy, it's posteriorities - what not to do - that's tough." With that:

A. Squeeze Budgets.

- Easiest for management to execute - could be claimed to be the only way.
- Slows down all/most programs, and generally out of proportion to the cuts.
- Pits people against each other with no resolution process, and tends to consume lots of energy.
- Probably the best way if you're convinced that its a very

short term problem.
- Takes a long time for people to get back to work - when that does happen, it's usually because of a structural or program change which has been made to free up energy.
- Transmits a bad message - Management doesn't know what to do either.
- People with the most fat in their budgets suffer the least. Promotes the wrong behavior
- Puts the pain and responsibility for coping at the lower levels where most people feel helpless anyway.
- Tells people you don't believe them when they told you how much a program cost.

Summary - Despite the fact that there really is fat in every budget, the people don't believe it and feel management is at fault. They waste an awful lot of energy on each other and the system.

B. Cut Programs.

- Creates direct pain for programs involved
- Risks alienation of specific people, especially the Program Management.
- Completely logical approach to the other 90% of the people.
- Shows willingness of management to take the responsibility (saying no always puts a Manager on a limb)
- Puts people in a mode of helping you find the cuts as an alternative to total program cuts if they really believe your wrong. This won't happen unless people believe management can say no and act.
- Eliminates the "can't be done" pushback. You may not be able to do it for less, but you can sure not do it.
- Tends to be short lived pain. Fellow workers have sympathy for each other and the good people get quickly absorbed on other projects. Non-performers - and peers know who they are - are left hanging and end up being the ones who get shuffled out the door.
- In aggragate, tends to give direction to the engineering process on the theory that the programs that didn't get cut are the ones management likes. People learn fast. They'll assign a direction even if you couldn't verbalize it.
- Transmits the message that "I believe you when you say it cost this much, but I have a prerogative not to do it at all."

Summary - I believe we have tons of fat in the budget, but the people who actually have to execute it don't. Squeezing budgets gives everyone the excuse not to succeed. Cutting programs transmits a no nonsense message.

JCK

★★★★★★★★★★★★★★★★★
★ d i g i t a l ★
★★★★★★★★★★★★★★★★★

TO: ANDY KNOWLES
JULIUS MARCUS
cc: OPERATIONS COMMITTEE:
RON SMART

DATE: MON 17 MAY 1982 10:03 AM EDT
FROM: KEN OLSEN
DEPT: ADMINISTRATION
EXT: 223-2301
LOC/MAIL STOP: ML10-2/A50

SUBJECT: ENGINEERING BUDGET

The Engineering Budget is going to be an important issue during the Woods Meeting this week. Will you make a list of all Business, Small Office, Big Office and OFIS software projects that are planned or underway, including buyouts. Please put them in chart form by category of software and machine and at each intersection put down where it is being done, whether it is being bought outside or done inside, and money spent in 1983.

KHO:ml
KO1:S11.37

****
* d i g i t a l *
****

TO: AL BERTOCCHI

CC: GORDON BELL
JACK SMITH
BILL THOMPSON

DATE: 21 MAY 1982
FROM: JOE REILLY
DEPT: CE FINANCE
EXT: 223-6883
LOC/MAIL STOP: ML12-2/A16

SUBJECT: ENGINEERING PRODUCT ANNOUNCEMENTS (UPDATE)

Al, Attached are the major products by categories we will announce starting with the May announcements and continuing throughout FY83. This chart has been updated to reflect total Engineering Investment versus Engineering Investment To Date and New Product Start-Up Investment versus Transfer Cost.

Please note the following:

- Software has so many products some of them were categorized as enhancements.
- FRS = First Revenue Ship.
- NPSU = New Product Start-Up (Mfg. Expense).
- Some products are buyouts.
- Software announcement dates on average are three months prior to FRS.
- Jupiter and Nebula are fully loaded with CPU Development, Software Development, Memory Development and total overhead. However, they don't include the investment in Disks and Tapes. These are shown separately under Disks and Tapes to avoid double counting.

JR4.50

MAJOR PRODUCT

	ANNOUNCE DATE	FRS	PRODUCT MANAGER	TOTAL ENG INVESTMENT ($M)	MFG NPSU	ADV PROMO COST
SYSTEMS						
11/730 NEBULA	Q4-82	Q1-83	PHILLIPON	38.5	3.9	-
2080 JUPITER	Q2-83	Q4-83	R. FIORENTINO	49.0	4.9	400-600K (Est)
CT100	Q4-82	Q1-83	E. LAZAR	22.7	12.5	
DECMATE II	Q4-82	Q2-83	J. COX	4.4	1.1	22M
RAINBOW 100	Q4-82	Q2-83	B. FOLSOM	12.9	1.6	
LCP-5	Q4-82	Q4-83	N. RICH	4.2	2.1	120K
WORKSTATIONS						
AGATE	Q3-83	Q4-83	N. KHAN	-	-	N/A
ONYX (VS100)	Q2-83	Q2-83	N. KHAN	5.0	1.3	N/A
OPAL (VS500)	Q4-82	Q2-83	N. KHAN	1.4	0.5	N/A

JR4.46

MAJOR PRODUCT

	ANNOUNCE DATE	FRS	PRODUCT MANAGER	TOTAL ENG MFG INVESTMENT ($M)	NPSU	ADV PROMO COST
TERMINALS/PRINTERS						
VT193	Q2-83	Q3-83	G. KELLER	1.7	.6	-
VT201	Q2-83	Q3-83	G. KELLER	2.5	1.1	-
LA50	Q4-82	Q4-83	D. COTTON	.4	-	-
LN01	Q4-82	Q2-83	D. COTTON	1.3	.1	-
LA100KSR	Q4-82	Q1-83	D. COTTON	4.6	.3	-
SYSTEM OPTIONS						
CI780	Q4-82	Q3-82	P. CHEN	7.6	.8	-
ETHERNET PROD FAM						
PLUTO	Q4-83	Q1-84	M. RESSLER	6.7	.9	-
UNA	14-83	Q4-83	D. CLEVELAND	6.1	.2	-

MAJOR PRODUCTS

	ANNOUNCE DATE	FRS	PRODUCT MANAGER	TOTAL ENG INVESTMENT ($M)	MFG NPSU	ADV PROMO COST
TAPES & DISKS						
RX50	Q4-82	Q2-83	D. LESLIE	5.9	2.7*	-
RD50	Q4-82	Q2-83	I. LYLES	3.5	0.7	-
RC25 (AZTEC)	Q2-83	Q4-83	J. FORDE	16.7	6.7	-
RA81	Q4-82	Q1-83	K. SMITH	11.8	1.8	-
RA60 (PINON)	Q4-82	Q2-83	K. SMITH	23.0	3.6	-
HSC-50	Q1/Q2-83	Q4-83	K. SMITH	25.1	1.6	-
TU80	Q2-83	Q3-83	B. NAAS	1.7	0.5	-
TU81	Q3-83	Q1-84	B. NASS	5.2	0.8	-
UDA-52	Q3-83	Q4-83	K. SMITH	(Not Est)	(Not Est)	-
TA78	Q3-83	Q4-83	J. SWAN	4.3	1.0	-

*Based on 503K ships.

MAJOR PRODUCT	ANNOUNCE** DATE	FRS	PRODUCT MANAGER	TOTAL ENG INVESTMENT ($M)
SOFTWARE				
16-BIT OPERATING SYSTEM ENHANCEMENTS	-	-	MANY	55.9
16-BIT LAYERED PRODUCTS ENHANCEMENTS	-	-	MANY	39.3
32-BIT				
VMS 3.0	-	Q4-82	T. KEMPSELL	
VMS 3.B	-	Q4-83	T. KEMPSELL	129.0
SMALL VMS V.1	-	Q4-83	T. KEMPSELL	
CAT/TMS/VTC V.1	-	Q3-83	H. SNYDER	6.8
TPSS V.1	-	Q3-83	B. LYONS	5.4
VAX 11 APL V.1	-	Q1-83	R. MATUS	1.2
VAX 11 RDMS V.1	-	Q4-83	A. MOEDER	2.7
VAX 11 DEC/CMS V.1	-	Q4-82	C. BRADLEY	2.7
VAX 11 C V.1	-	Q4-82	R. MACLEAN	2.0
32-BIT LAYERED PRODUCT ENHANCEMENT	-	-	MANY	18.0
DISTRIBUTED SYSTEMS				
DECNET SOFTWARE (INCLUDING ETHERNET)	-	-	MANY	4.7
X-25 IBM INTERNET	-	Q3-83	MANY	2.4
OFFICE VAX	-	-	B. STEWART	4.7*
OFFICE CT	-	Q3-83	R. GRIFFIN	.9*
36-BIT OPER SW	-	-	MANY	2.6
36-BIT COMM SW	-	-	S. PASSON	4.5

*$ IN OFFICE VAX ALSO APPLIES TO OFFICE CT BUT CAN'T BE SPLIT OUT.
**ON AVERAGE 3 MONTHS PRIOR TO FRS.

WPS USERS - Enter HP mode and then type <CR>
★★★★★★★★★★★★★★★★
★ d i g i t a l ★
★★★★★★★★★★★★★★★★

TO: OPERATIONS COMMITTEE:

cc: see "CC" DISTRIBUTION

DATE: WED 26 MAY 1982 11:34 AM EDT
FROM: TONY WAIN
DEPT: CORP FIN PLNG & ANAL
EXT: 223-8537
LOC/MAIL STOP: MS/G15

SUBJECT: HEADCOUNT ANALYSIS

At Win's request, the headcount analysis originally scheduled for discussion at the June 1 O.C. meeting has been postponed.

A copy of the analysis, which is being developed by your Group Personnel Managers, should be submitted to CFP&A on June 10 along with the final BOD proposals. It will be reviewed at the June 16 - 17 O.C. Woods.

lms

"CC" DISTRIBUTION:

LARRY BORNSTEIN
GROUP CONTROLLERS:
JOHN SIMS

JACK FUSCO
GRP PERSONNEL MGRS:

GR PLANNING MGRS:
CHUCK POE

★★★★★★★★★★★★★★★★
★ d i g i t a l ★
★★★★★★★★★★★★★★★★

Ken Tyn Jack Larry or Joe ?

TO: OPERATIONS COMMITTEE:

cc: see "CC" DISTRIBUTION

DATE: MON 24 MAY 1982 5:25 PM EDT
FROM: TONY WAIN
DEPT: CORP FIN PLNG & ANAL
EXT: 223-8537
LOC/MAIL STOP: MS/G15

Bornstein is pulling this together for you, TW

SUBJECT: HEADCOUNT ANALYSIS FOR JUNE 1 O.C.

Attached is a form for your use in reviewing headcount projections from now through the end of FY83 per Operations Committee agreement last week. This is scheduled for discussion at the June 1 O.C. and is a summary of data previously requested in Shel Davis' EMS dated April 23, 1982.

The instructions for completing the attached format are as follows:

- COLUMN 1 lists the major functions in the exempt and non-exempt wage categories. "Job Family" codes (e.g., D = Data Processing, E = Engineering, etc.) provide the basis for this data. If you have headcount that does not fit one of the categories, use the "Other" category and indicate the job function.

- Enter into COLUMN 2 the number of people, by Function, in your organization as of the close of business on May 21, 1982 (last Friday). The total should be consistent with your latest headcount forecast.

- Indicate in COLUMN 3 the number of people now in your organization who belong on the "Highly Recommended" list. This number should ultimately be supported by a list of names as requested in Shel Davis' EMS.

- Enter into COLUMN 4 the number of net additions to headcount planned for your organization from May 21, 1982 through the end of FY83.

- Compute your desired ending headcount for FY83, as follows, and enter into COLUMN 5:

  Ending FY83 Headcount = Current Headcount
  - Highly Recommended List
  + Net Additions

  This computation assumes that all highly recommended people will be placed outside of your organization.

A summary of this data will be incorporated into the final BOD submission on June 10.

If you have any questions, please contact your Group Personnel Managers.

lms

HEADCOUNT ANALYSIS

ORGANIZATION: _____

CURRENT HEADCOUNT (AS OF 5/21/82)	-	HIGHLY RECOMMENDED LIST	+	NET PLANNED ADDS	=	DESIRED END FY83 HEADCOUNT

EXEMPT

MARKETING
ENGINEERING
MANUFACTURING
FIELD TECHS
INSTRUCTORS
SALESPEOPLE
F&A
FACILITIES
PERSONNEL
MIS
OTHER (SPECIFY)

SUBTOTAL: EXEMPT

NON-EXEMPT

SECRETARIES
CLERICALS
PRODUCTION WORKERS
ORDER ADMIN
FACILITIES
OTHER (SPECIFY)

SUBTOTAL: NON-EXEMPT

TOTAL HEADCOUNT

"CC" DISTRIBUTION:

LARRY BORNSTEIN
GROUP CONTROLLERS:
JOHN SIMS

JACK FUSCO
GRP PERSONNEL MGRS:

GR PLANNING MGRS:
CHUCK POE

Rich these are the corrections the %'s line up even better than the last numbers EG

"BACK OF ENVELOPE"
FY83 CENTRAL ENGINEERING INVESTMENT
COMPARISON WITH FY82 THROUGH FY86 CUMULATIVE REVENUE

PROGRAM	FY83 ENGINEERING	CUMULATIVE (UNDISCOUNTED) NOR FY82 THRU FY86
16BIT	17% ~~19%~~	30%
32BIT	64% ~~72%~~	54%
36BIT	4% ~~5%~~	4%
TERMINALS & WORKSTATIONS	14% ~~15%~~	11%

FIGURE 1
EG:kr3.29.1

REV A
2/9/82

"BACK OF ENVELOPE"
FY83 CENTRAL ENGINEERING INVESTMENT
BREAKDOWN BY PROGRAM
$M

SYSTEM PROGRAM / ENG ORGANIZATION	16B	32B	36B	TERMINALS & WORKSTATIONS	TOTAL
GUTMAN	12.3				
AVERY				34.5	
DEMMER		44.0			
FAGERQUIST		19.0	12.5		
SUBTOTAL	12.3	63.0	12.5	34.5	122.3
LACROUTE (DP)[1]	3.4	17.6			21.0
JOHNSON (SW)[2]	19.4	44.5			63.9
SAVIERS (SSD)[3]	8.6	45.7		4.0	58.3
TEICHER (SEG)[4]	5.1	9.2		2.1	16.4
TOTAL	48.8	180.0	~~12.5~~ ~~40.6~~	~~251.9~~ 40.6	281.9
%	~~19.4%~~ 17.3%	71.5% 63.9%	~~5%~~ 4.4%	~~100%~~ 14.4%	100%

NOTE 1: Allocated in proportion to 16B and 32B Engineering Expense.
NOTE 2: Allocated according to projects within SW Engineering.
NOTE 3: Allocated according to primary program office 16B, 32B Engineering Expense, except for identifed Terminals & Workstations projects.
NOTE 4: Allocated in proportion to primary program office investment in 16B, 32B and Terminals & Workstations.
NOTE 5: The remaining part of the Engineering expense for FY83 is treated as overall support for the programs.

FIGURE 2

Rev A

WPS USERS - Enter HP mode and then type <CR>
****
* d i g i t a l *
****

TO: *GORDON BELL
JACK SMITH
cc: JOE REILLY
RON SMART

DATE: THU 27 MAY 1982 12:20 PM EDT
FROM: RICK CORBEN
DEPT: CORP PRODUCT MGMT
EXT: 223-3123
LOC/MAIL STOP: ML12-1/-I39

SUBJECT: ENGINEERING INVESTMENT REVIEW

Gordon wants to complete the entire review of Engineering investment (including Product Group Engineering) before he leaves for Japan on June 20. I gave Ron Smart a copy of the memo which describes the chart formats which EMC will use for the material due on June 9. He will try to get Win to issue the same memo with the same deadline for the Product Groups. (You may want to convey your support to Win since I do not see any other way to get the data as fast.)

Even on this schedule, you will be incredibly rushed (especially if you want some insight from the process prior to the OC Woods on June 16). The only way that we could meet Gordon's timeframe w[illegible] something like the following:

Wednesday, June 9 -- Charts describing engineering investment due from EMC managers and Product Groups. (We would have to arrange "instant" distribution.)

Friday, June 11 -- EMC Staff groups meet individually to discuss data and make recommendations. (Obviously, discussions prior to the availability of the formal documents is advisable and encouraged.)

Monday, June 14 -- EMC meets to discuss and develop Engineering recommendations.

Wednesday, June 16 and 17 -- OC Woods

Friday, June 18 -- Perhaps, a final EMC meeting with Gordon to develop final conclusions and plans.

I have not checked anyone's calendar since it is obvious that this process would require massive disruption to people's plans. Do you want to install this grueling schedule? Any ideas for alternate approaches?

RC1.S8.34

MAY 27 1982

digital INTEROFFICE MEMORANDUM

TO: Eng. Staff
CE Controller Staff
Eli Glazer
Jim Wade

DATE: 26 May 82
FROM: Jim Lawless
DEPT: Central Eng. FP&A
EXT: 223-5811
LOC/MAIL STOP: ML12-2/A16

cc: Ron Aronson

SUBJ: ENGINEERING BUDGET UPDATES FY83 AND FY84

Enclosed are the latest budget updates reflecting all changes made thru the Operations Committee meeting the week ending May 21.

The major changes, of course are those reflected in Joe Reilly's memo of May 18 and the recent Operations Committee decrease of $4.6M.

Enclosures

/svb

SUMMARY OF CHANGES TO FY83 ENGINEERING PROJECT EXPENSE BUDGET

	BASE 4/30/82	COMBINE CT WITH TERM. & WS	COMBINE SA&T, RAD, & CORP. RES.	COMBINE EUROPE ENG. & SOFTWARE	MAY 18 ADJ. PER REILLY MEMO	BASE 5/18/82	MAY O.C. ADJ.	SHREWSBURY PROPERTY TAX ASSISTANCE	BASE 5/21/82	
GUTMAN-16 BIT	12343				1157	13500	<179>		13321	16 BIT-GUTMAN
AVERY-TERM & WS	34117	400			<17>	34500	<458>		34042	TERM & WS-AVERY
AVERY-CT	400	<400>				-			-	
DEMMER-32 BIT	37910				4090	42000	<557>		41443	32 BIT-DEMMER
LACROUTE-DIST SYS	21019				<19>	21000	<278>		20722	DIST SYS-LACROUTE
FAGERQUIST-LSG	33718				2982	36700	<487>		36213	LSG-FAGERQUIST
SAVIERS-STORAGE	56907				<3007>	53900	<715>	13	53198	STORAGE-SAVIERS
TEICHER-SEG	16437				4463	20900	<277>		20623	SEG-TEICHER
JOHNSON-SOFTWARE	63868			1520	<4088>	61300	<818>		60482	SOFTWARE-JOHNSON
HOLMAN-TOPS	8480				<980>	7500	<99>		7401	TOPS-HOLMAN
THOMPSON-PTD	7641				1559	9200	<122>		9078	PTD-THOMPSON
FULLER-SA&T.	7014		5769		<883>	11900	<158>		11742	SA&T-FULLER
FULLER-RAD	1969		<1969>			-			-	
FULLER-CORP RES	3800		<3800>			-			-	
BELL-CENTRAL	9397				1108	10505	<139>		10366	CENTRAL-BELL
REILLY-FINANCE	2667				33	2700	<35>		2665	FINANCE-REILLY
BORNSTEIN-PERSONNEL	2275				<160>	2115	<28>		2087	PERSONNEL-BORNSTEIN
ROSE-ADMIN	2902				78	2980	<39>		2941	ADMIN-ROSE
ROSE-NEW SITES	13284				<3284>	10000	<133>	<13>	9854	NEW SITES-ROSE
EXT RESOURCES	1401				<1>	1400	<18>		1382	EXT RESOURCES
WADE-EURO ENG	1520			<1520>		-			-	
CONTINGENCY	2188				<2188>	-			-	
GENERAL TECH	5347				<5347>	-			-	
WEST COAST CMU JAPAN	-				4500	4500	<60>		4440	WEST COAST CMU JAPAN
TOTAL	346604	-	-	-	<4>	346600	<4600>	-	342000	

5/26/82--RL06/5.46

SUMMARY OF CHANGES TO FY84 ENGINEERING PROJECT EXPENSE BUDGET

	BASE 4/30/82	COMBINE SA&T, RAD, & CORP. RES.	COMBINE EUROPE ENG. & SOFTWARE	SHREWSBURY PROPERTY TAX ASSISTANCE	BASE 5/21/82	
GUTMAN-16 BIT	8992				8992	16 BIT-GUTMAN
AVERY-TERM & WS	40828				40828	TERM & WS-AVERY
DEMMER-32 BIT	36841				36841	32 BIT-DEMMER
LACROUTE-DIST SYS	23635				23635	DIST SYS-LACROUTE
FAGERQUIST-LSG	34749				34749	LSG-FAGERQUIST
SAVIERS-STORAGE	69377			14	69391	STORAGE-SAVIERS
TEICHER-SEG	17781				17781	SEG-TEICHER
JOHNSON-SOFTWARE	76662		1780		78442	SOFTWARE-JOHNSON
HOLMAN-TOPS	7821				7821	TOPS-HOLMAN
THOMPSON-PTD	8084				8084	PTD-THOMPSON
FULLER-SA&T	8037	6667			14704	SA&T-FULLER
FULLER-RAD	2373	<2373>				
FULLER-CORP RES	4294	<4294>				
BELL-CENTRAL	10674				10674	CENTRAL-BELL
REILLY-FINANCE	3024				3024	FINANCE-REILLY
BORNSTEIN-PERSONNEL	2572				2572	PERSONNEL-BORNSTEIN
ROSE-ADMIN	3138				3138	ADMIN-ROSE
ROSE-NEW SITES	18050			<14>	18036	NEW SITES-ROSE
EXT RESOURCES	1615				1615	EXT RESOURCES
WADE-EURO ENG	1780		<1780>			
UNALLOCATED	28374				28374	UNALLOCATED
CONTINGENCY	25000				25000	CONTINGENCY
GENERAL TECH	12000				12000	GENERAL TECH
TOTAL	445701	-	-	-	445701	

5/26/82--RL06/5.48

ENG STAFF

BILL AVERY	ML12-2/E71
GORDON BELL	ML12-1/A51
LARRY BORNSTEIN	PK3-1/C21
DICK CLINTON	ML12-2/A16
RICK CORBEN	ML12-1/T39
JIM CUDMORE	HL2-2/M11
BRUCE DELAGI	ML2-2/T88
BILL DEMMER	TW/D19
ULF FAGERQUIST	MR1-2/E78
SAM FULLER	HL2-3/N11
MIKE GUTMAN	ML12-2/E71
JOHN HOLMAN	ML23-2/T36
BILL JOHNSON	ML12-3/A62
JEFF KALB	HL2-2/M11
BERNIE LACROUTE	TW/A08
JOE REILLY	ML12-2/A16
JOHN ROSE	ML12-2/T54
GRANT SAVIERS	ML3-6/E94
JACK SMITH	ML1-4/A54
STEVE TEICHER	HL2-2/N07
WILL THOMPSON	QI-1/E21
PETE VAN ROEKENS	ML12-3/A62

CE CONTROLLER STAFF

STEVE BEHRENS	ML12-3/A62
KEVIN CHAMBERS	CF2-3/J24
DICK CLINTON	ML12-2/A16
DON CROWTHER	ML3-5/T71
JEFF HABER	ML12-B/B93
DICK HASLETT	QI-1/E22
JIM LAWLESS	ML12-2/A16
WALTER LEFLORE	ML3-4/E95
DAVID MARKEY	ML5-2/T86
RAY MERCIER	HL1-1/008
CAROL REID	TW/D19
JOE REILLY	ML12-2/A16
DAVE SAWIN	MR1-2/G3
ED SAWYER	ML3-6/E94
MARY ANN SERRA	ML12-2/E71

MAY 27 1982

****
* digital *
****

TO: EMC

CC: PEG

DATE: 25 MAY 1982
FROM: JOE REILLY/
RICK CORBEN
DEPT: CE FINANCE
EXT: 223-6883/3123
LOC/MAIL STOP: ML12-2/A16

SUBJECT: ENGINEERING INVESTMENT ANALYSIS FOR OC

Jack has asked us to facilitate the process to fulfill the OC request. The request is to review and analyze the total Corporate Engineering Investment.

Attached is the process we will use in Central Engineering along with the format each group will supply.

Please submit a completed version to Rick Corben ML12-1/T39 by, Wednesday, June 9.

GOAL:

To review and analyze the Engineering Investment in order to identify opportunities for project consolidation and more efficient utilization of our resources.

PROCESS:

(1) Each group generates the attached chart.

(2) We will then distribute total data to each Engineering group.

(3) Each EMC Staff will review the entire package, identify significant overlaps, and proposal recommendations with a five percent (5+%) savings target.

(4) EMC will review the recommendations of each group.

(5) At the same time P/Ls will provide us the same data about their projects and EMC will fold it into our analysis.

(6) A consolidated proposal will be brought to Operations Committee.

(P.S. At this time SEG, PTD and Central won't be included.)

GUIDELINES

- Group your projects into high level entities.

  (e.g., VAX 117/50

- Software - Group projects so they exceed $500K annual budget.

- Software - NPSU and service start-up are not expected.

- Projects still in phase zero may not have all the data request. Please supply whatever data is available.

- Include in Product Support any maintenance or support expense not covered in the Product Development section.

- Other Engineering includes any expenses not covered by Product Development, Advanced Development.

- Chart III is for Hardware. Chart IV is for Software.

- NPSU = Manufacturing New Product Start-Up.

JR4.51

CHART I

PRODUCT DEVELOPMENT

Product Name & Summary Description & Summary Prioritized	Current Phase	FRS	IRR %	NOR Lifetime $B	ENG EXP Lifetime $M	NPSU $M	SERV. Summary $M	'82	'83	'84

CHART II

PRODUCT SUPPORT

PROJECT NAME AND SUMMARY DESCRIPTION PRIORITIZED	ENGINEERING BUDGET $M '82	'83	'84
ADVANCED DEVELOPMENT	'82	'83	'84
OTHER ENG EXPENSE	'82	'83	'84
TOTAL EXPENSE			

JR4.52

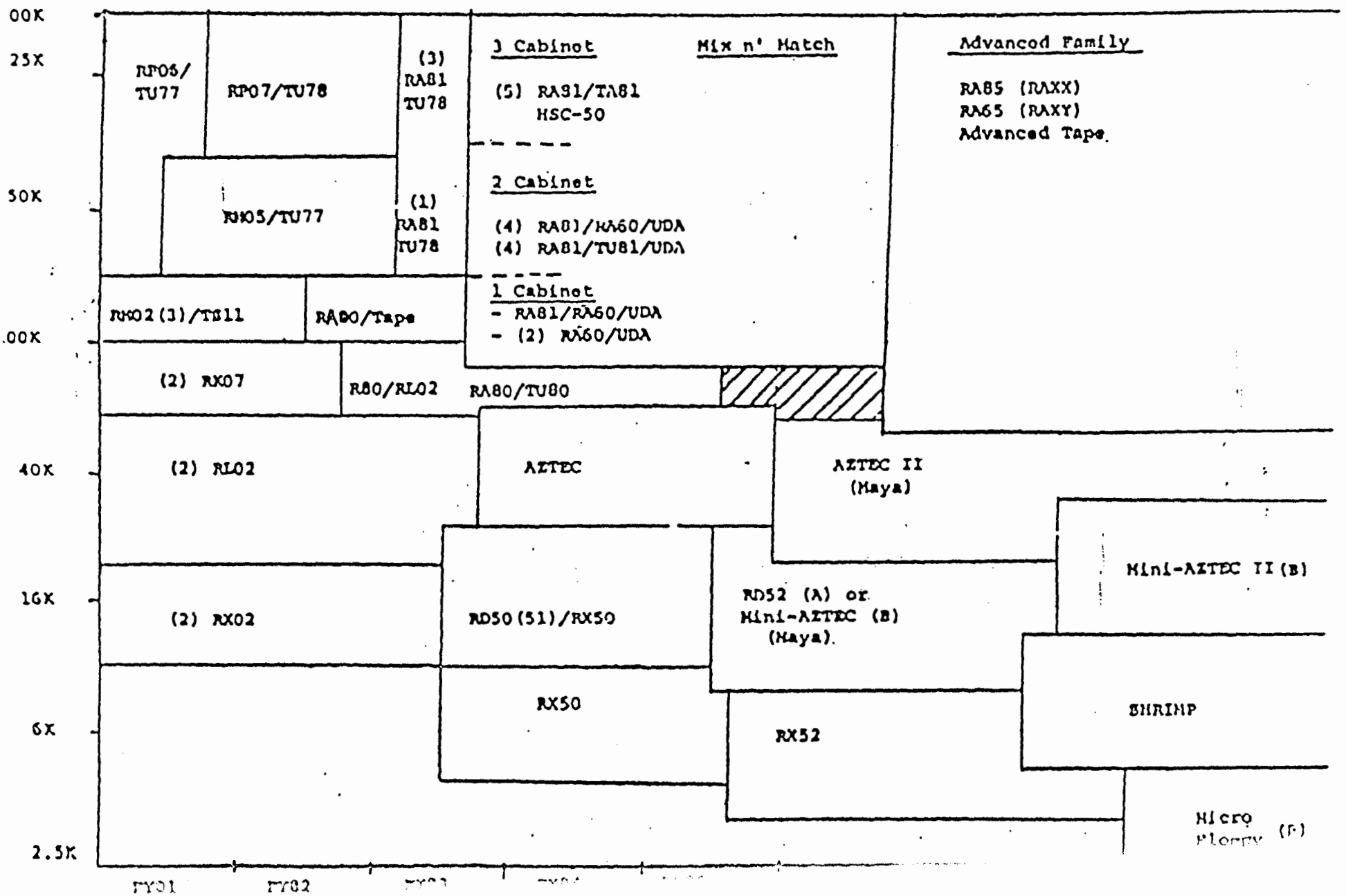
CHART III

SYSTEM/PRICE BAND CHART

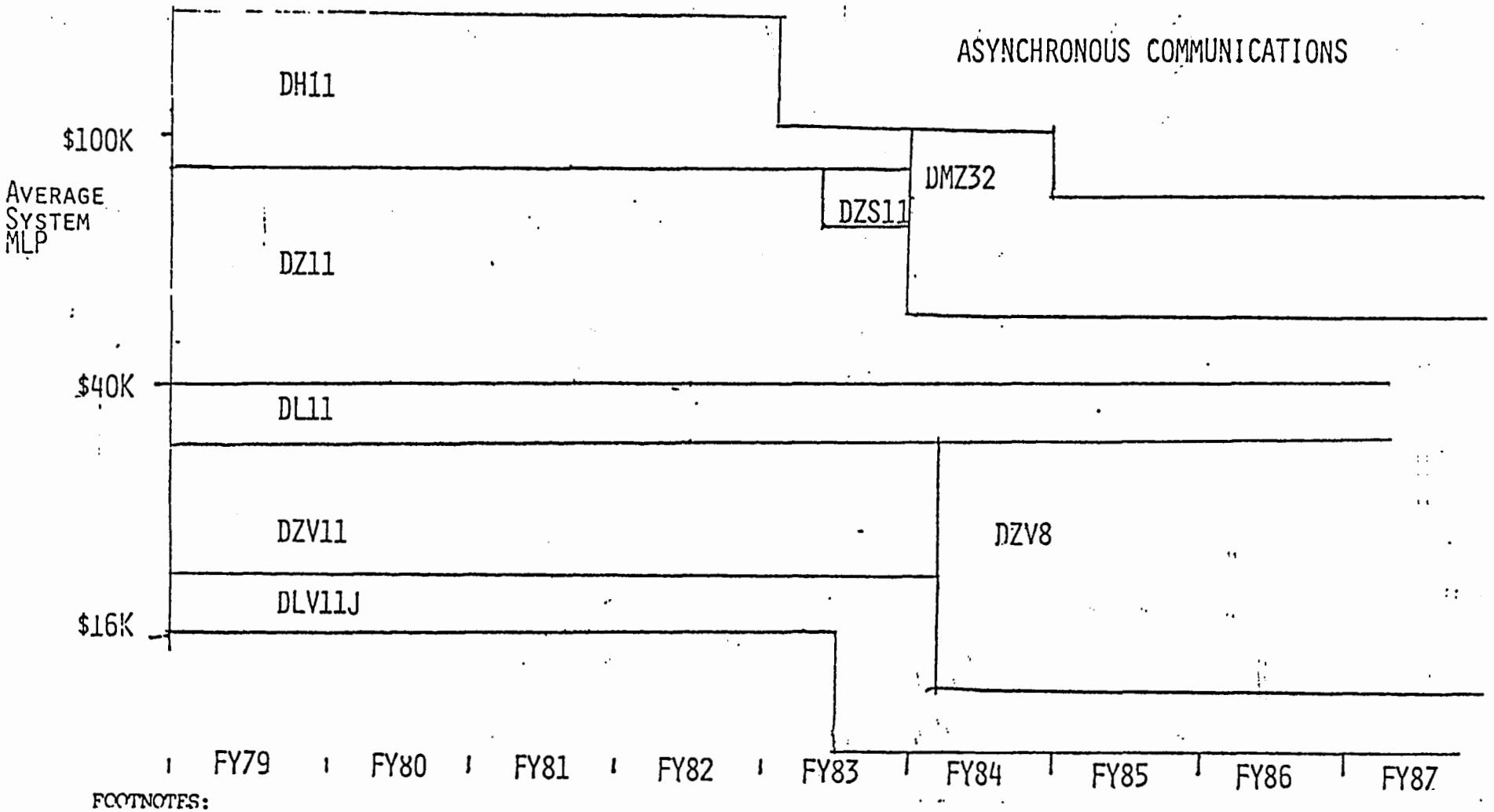
This will allow you to position your product development graphically to related products.

An example of the desired format is attached. Low-End products can use transfer cost rather than systems price.

STORAGE SUBSYSTEM PLAN (SCENARIO A,B) - 12/81



PDP-11 SYSTEMS



FOOTNOTES:

	DH11	DL11	DLV11J	DMZ32	DZ11	DZS11	DZV11	DZV8
RS232/RS423/20MA.	232/20	232	423	423	232/20	232	232	423
MAX # OF LINES:	16	1	4	8	8	8	4	8
MAX SPEED: (K BAUD)	9.6	9.6	19.2	19.2	9.6	9.6	9.6	19.2
DMA OUTPUT	X			X				X
SILO INPUT	X			X	X	X	X	X
FULL MODEM CTL & SPLIT SPEED	X			X				X

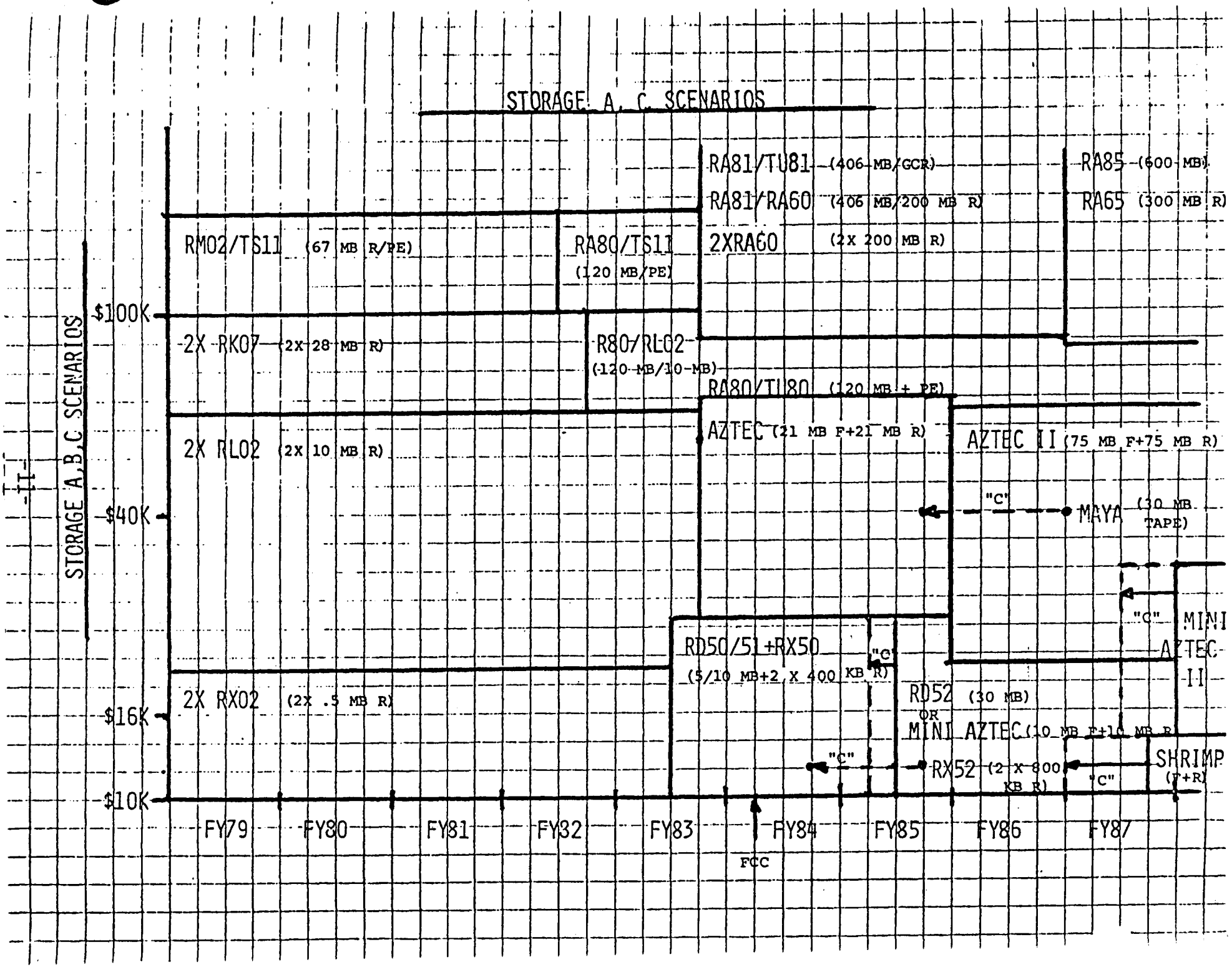

STORAGE A, C SCENARIOS
STORAGE A,B,C SCENARIOS
$100K
$40K
$16K
$10K
RA81/TU81 (406 MB/GCR)
RA81/RA60 (406 MB/200 MB R)
2XRA60 (2X 200 MB R)
RA85 (600 MB)
RA65 (300 MB R)
RM02/TS11 (67 MB R/PE)
RA80/TS11 (120 MB/PE)
2X RK07 (2X 28 MB R)
R80/RL02 (120 MB/10 MB)
RA80/TU80 (120 MB + PE)
2X RL02 (2X 10 MB R)
AZTEC (21 MB F+21 MB R)
AZTEC II (75 MB F+75 MB R)
"C"
MAYA (30 MB TAPE)
"C"
MINI AZTEC II
RD50/51+RX50 (5/10 MB+2 X 400 KB R)
"C"
2X RX02 (2X .5 MB R)
RD52 (30 MB)
OR
MINI AZTEC (10 MB F+10 MB R)
"C"
RX52 (2 X 800 KB R)
"C"
SHRIMP (F+R)
FY79
FY80
FY81
FY32
FY83
FY84
FY85
FY86
FY87
FCC

CHART IV

SOFTWARE

For each Software project in your Product Development section explain the following:

- What new functionality is being added by this project?
- Why is it required?
- Discuss the relative positioning with products of similar functionality if any?

```
%%%%%%%%%%%%%%%%%
% d i s i t a l %
%%%%%%%%%%%%%%%%%

TO: see "TO" DISTRIBUTION                DATE: FRI 19 FEB 1982  4:25 PM EST
                                         FROM: DICK STRAUSS
cc: ELI GLAZER                           DEPT: TECHNICAL GROUP
    TGM STAFF:                           EXT:  231-7196
                                         LOC/MAIL STOP: MR1-1/A65

SUBJECT: PART II TG RESPONSE TO ENGINEERING BASE PLAN (CON'T)
```

Software Engineering:

We well understand that only a few people can suck around in the internals of an operating system at once. How can we possibly expect to support in version 3B:

- 3 new CPUs (Scorpio, Nautilus, Venus)
- A new phase of DECnet (Phase IV including Ethernet)
- Security
- Hydra availability features
- Many new disks and tapes
- Workstations (uVAX)
- DFIS
- Hopefully, some load sharing features

We have a real fear that in fact all this will not be done in time.

We see a lot of unmanaged overlap between DFIS, VAX Mail, VAX Workstations, TPSS, and FMS that must be understood so we know what we are doing to our system interface for our users. We require a single, managed user interface strategy which is held to.

CI Cluster/Network Management is our highest priority need from V3B of VMS. Specifically, we need products to respond to the following requirements:

- Heterogeneous CPU's (not necessarily high availability)

- Cluster Management (including load balancing)

- Performance optimization tools

- User/system independence throughout cluster

We do not see a coherent strategy for servers (file, print, etc) on the CI and NI. This is a need we are already hearing from customers. Implicit in this will be a need for mass storage devices significantly larger than we are now planning.

The Basic Language must be modified to be in accord with the FIPS requirements.

We need commitments for CDD on Fortran, Pascal, and Ada.

We see insufficient need to justify spending on CATS and TPSS.

UNIX is not part of our strategy. Please stop the current ad hoc support by Engineering of the UNIX customer/computer science community. (We do not mean the TIG support function). The Engineering effort should be focused on putting UNIX features on VMS.

We have to reduce our spending on 16 bit operating systems. We must have a goal of eliminating Engineering expense for two of the four 16 bit operating systems in FY83, and eliminating expense for a third one in FY84.

OFIS:

We feel strongly that we will not have a positive productivity message for professionals in the version 1 product. We sell systems, not software, so we need a product that is excellent enough to sell another entire computer system. The other possibility is to create enough market pull to motivate our customers to buy OFIS software for their current system through ASSC or another distribution channel. OFIS V1 does not fulfill these requirements. Is it worth making OFIS V1 a valid saleable product by delaying its introduction date?

For Digital to announce an OFIS product without integrated graphics weakens our system integration message. What can be done to get graphics in V1?

The specific issues between the Technical Group and the OFIS program are well known and need not be reiterated here. The bottom line is the current product is aimed at the professional, manager, and secretary. It excels at none of these targets. Our first need is a product which excels at meeting the professional's needs.

Storage:

Our principle business throughout the 80's is projected to be networks of workstations and servers, and shared 32 bit CPU's. Aztec appears too bulky and expensive for the former, and too small for the latter. The Technical Group cannot justify an Aztec product.

We currently support taking a storage leadership position in the $50-400K system range, and buyouts above and below that. Therefore, we do not see the incremental benefit of building the RD52.

CT and Terminals:

We view CT initially as a professional workstation. At first release, the product lacks essential functionality in the software such as Fortran, Native Fips Basic, Word Processing, and Screen Graphics Operators. These specific concerns have been voiced previously.

In the terminal space, we feel that there is a significant demand from our customers for a full page of text with graphics. There is almost no demand for 1/2 page. Let's cancel the half page project and put all of our effort on full. Furthermore, we sell systems with terminals, and we have little demand for a terminal less expensive than the VT100.

Overall, the LA100 looks like an exciting product for integration of text and graphics. When will we have software to support it?

We need full Regis support on CT.

Remaining Summary Issues:

SES - Could we decide not to do the SI and save the money set aside for chip development.

16 Bit - Orion without a floating point accelerator is a waste of time and money.

I thought we decided to only do a Unibus Orion last year at this time. That still appears to be a valid decision.

We see very limited need for the LCP products.

In the two years I have been involved in this process, I think Engineering has evolved to a point where their developments are a great deal closer to meeting our needs. The lines of communication are excellent, and Engineering now appears to have a fine management team.

By virtue of our orientations, there will always be a set of needs which will not be covered, and we will continue to bring them to light to assure we are doing the optimal things. Questioning from every point of view is the Digital way. Let's continue to keep the channels open, let's continue to question, and most of all, let's continue to win.

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* d i g i t a l *
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TVG

TO: RICK DORSEN

DATE: SUN 01 FEB 1982
FROM: LINDA BARLES
DEPT: TR
EXT: 223-3293
LOC/MAIL STOP: TP/TR

cc: TVG STAFF:
TVG-MSTAFF:

SUBJECT: CORRECTIONS TO TVG INPUTS TO ENG BASE PLAN

The TVG lists of concerns we generated were incorrectly communicated to you on Friday. Please use the following as our final input:

1. SCORPIO
   * What are we getting?
   * Are there enough funds to cover the approval to Operations Committee?
   * Need FPA at FCS
   * Need DSA one year ahead. FCT as presently owned. Accelerate from CY87 to CY86
   * No BI scaled funded (SCHEC and LSSI omitted)

2. J-11 (CRIOR)
   * FPA not funded - essential for the product

3. MICRO-VAX
   * Is the product adequately funded?

4. MULTI-PROCESSING and HIGH AVAILABILITY
   * Need accessibilities beyond 8175(750) and HSC-XX. These solutions are too expensive.
   * Inexpensive, simple HSC-XX owners
   * High availability Nebula desired
   * Multiprocessing is a requirement so that T-Bus be capture new designs in the subsequent generations. Multiprocessing being driven by TVG dual marketing; however, the 16-bit program office should be staffed to assure common architecture between Q-Bus and system Q-Bus products.

5. MASS STORAGE
   * UDA-52 should not be necessary
   * Separate RAXX from RAXY; then accelerate RAXX and drop RAXY (RA60 follow-on)
   * Accelerate MAYA to FY85 and take funds from RX-52 and YANKEE.
   * Do RD51 but don't do RD50
   * Put tape support back into the UDA

6. NEBULA
   * Short product life which we can't live with unless the following enhancements are added:
     1. IEC support of RB1

1. Bisynch Support for the Combo board is required.

2. Need Pollux or KMS for increased SNA Gateway performance.

3. We must be able to connect large numbers of terminals to a VAX (500+). Neither Pluto or Pluto Jr. will allow this. Cost/performance issues for Pluto/Pluto Jr. must be resolved.

4. We would like to see more aggressive broadband development. We need to understand all the NI vs. broadband issues.

5. Network security is an important issue. Is the $34K in advanced development adequate to address this problem?

6. Don't do any further RSTS network development. This includes NI support and RSTS access to all gateways.

7. Remote DECNET for DT is required. Currently, only DECNET .. the NI is planned.

8. DT access to the SNA Gateway is required.

9. CX/BX is an important short term product. Support should be consolidated in one group.

10. A coordinated file server effort is required. Which group is responsible?

11. A T carrier interface to PBXs (including Ethernet) is required. This will be a growing retail need and could solve the problem of connecting a large number of terminals connected to VAX.

12. We need bi-directional capability between the SNA Gateway and IBM.

32-BIT SOFTWARE

1. CATS and FMS are diversing products. With CATS funded at $2M, is $800K necessary for FMS?

2. We should be investing in fourth generation languages by extending Datatrieve. All the proposals were in scenario B.

3. Development of a resource dictionary should be pursued. This is also a scenario B proposal.

4. We support Engineering's proposal for NFS (Multi-function system). This should provide a better user interface and integration. (DEC's answer to the IBM System 36.)

5. Shadowing is required for Massbus disks. Currently it is only available with HSC which is too expensive for some applications.

2. BBU for time-of-day clock for automatic restart
3. Testing of UDA-50 in CPU backplane
4. Documentation for public access to internal bus

7. SOFTWARE - MICRO PASCAL
   * Key 16 bit products for the 80's are RSX11-M+ and MicroPower/PASCAL. RT11 will be phased out.
   * Need a multiuser development system for MicroPower/Pascal to insure its success.
   * Use RT-11 enhancements funding for the development of MicroPower/Pascal multiuser development system
   * Limit RT funding to RD/RX device support

OTHER CONCERNS

1. 11/782
   * What are future plans to improve this product?
   * Should have funding for 64K memory support

2. ANE
   * Funding not obvious to keep ANE in sync with RSX-11M and to fix deficiencies

21-FEB-82 19:15:20 5 2107 RC82

DLC6 MESSAGE ID: 0155138264

Comnl.

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*********************
* d i s i t o l *
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TO: RICH DORBEN

DATE: MON 22 FEB 1982 4:35 PM EST
FROM: GARY J ECKROTH
DEPT: COMM MKTG
EXT: 264-7956
LOC/MAIL STOP: MK1-1/N38

SUBJECT: POSITION STATEMENTS

Following are the issues that should be discussed at Thursday's PEG meeting. I will distribute this memo and the 0, 1, 2 ratings to CPLMC and Marcus' Staff. I am assuming that you are putting a package together for PEG members. These statements are the result of reviews with CPLMC and Marcus' Staff.

VAX-11 PROGRAM

1. We would like to see a single strong Engineering focus on high availability. High availability for Nebula is also needed.

2. We need to be able to connect large numbers (5000) of terminals to a VAX system. There are no products to address this problem.

3. We are not comfortable with the Cluster schedule. Will additional funding accelerate the schedule or is there too much risk?

4. Joint Engineering/Manufacturing/Customer Services tools are a positive step and should receive more visibility.

5. The Program Office is thinking of pieces as opposed to systems. A greater systems approach is needed for budgeting and system planning.

STORAGE PROGRAM

1. Mass is too little too late. Yankee is also too far out. What are buyout alternatives?

2. Optical Disks appear to have considerable potential. A project should be funded from technology funds to investigate them.

3. Need a project to put Data Management software (RMS) into the HSC.

4. Mini Aztec appears to be a better alternative to RSS.

DISTRIBUTED SYSTEMS

6. Need distributed Datatrieve for CT.

7. Need full support for EPI. There seems to be some confusion as to whether the support is planned.

8. There is a need to support a large number of Videotex terminals on VAX.

16-BIT

1. Minimize funding for 16-bit products. Concentrate on new device support and maintenance. The exception is when enhancements are applicable to the CT.

OFIS PROGRAM

1. Two DECPLOTs are planned and unfunded. We need one to cover both DF and OFIS.

2. Better integration with VIA, Distributed Systems and CT is required. These products must be integrated.

3. OFIS on MSX-11M is not needed.

4. The OFIS software architecture should accomodate IBM in areas such as higher level document protocols.

5. There is a lack of licensed VAX Office Planner. We need support for voice, image, print servers and integration with VAX Information Management. All of these are unfunded.

6. Wide carriage printer support is needed.

TERMINALS AND WORKSTATIONS

1. Need PLP and DECPT Graphics.

2. Need funding to develop a print server.

3. Most DEC software only understands character mode terminals. There are no plans to support the intelligent block mode VT200.

4. Concern about the overlap of VT200 and CT25.

5. Need access from CT to the SNA Gateway.

6. Need IBM file/data interface software that is compatible with IBM's personal computer software when it is available.

7. A CT should be able to emulate a VT125 in order to run DECPLOT on VAX.

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* d i g i t a l *
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TO: see 'TC' DISTRIBUTION

cc: see 'CC' DISTRIBUTION

DATE: TUE 23 FEB 1982 9:47 PM EST
FROM: RICK CORSEN
DEPT: CORP PRODUCT MGMT
EXT: 223-3123
LOC/MAIL STOP: ML12-1/-T39

SUBJECT: MARKET GROUP SURVEY -- OVERVIEW

As a part of the process leading to the Engineering review at Operations Committee in March, a survey of four Market Groups was conducted. Each was asked to rate the business significance of Engineering projects on the following scale:

0 - No business significance
1 - Some business significance
2 - Substantial significance to business

In addition, each Market Group was invited to submit a summary of issues and concerns. All but the Small Custom Group elected to do so.

In order to provide rapid distribution, the results are being distributed as a set of five DPS memos:

OVERVIEW	Summary of Results (This Memo)
BLAISE DATA	Detail Activity by Project
TECH EAL USER	Positive Observations
TECH VOLUME	Position Statements
CONFIDENTIAL	Personnel Discussions

* Because of EMS memo size restrictions, the explanation for the above asterisks had to transmitted as a part of the memo titled "MARKET GROUP SURVEY -- OVERVIEW".

/Jam
RC1,97,5

"TO" DISTRIBUTION:

ART CAMPBELL
GVPC:
PEG:
TECH. GROUP STAFF:

MIKE GALLUP
MARCUS DIR REPTS:
JOEL SCHWARTZ
TVG STAFF:

ROSE ANN GIORDANO
BILL MORRIS
BRUCE STEWART

"CC" DISTRIBUTION:

GARY J ECKSTH
DICK BISLOVE

EDGPPC:
TPMC:

ELI GLAZER
TVG-STAFF:

0 - No Bus
1 - Moderate
2 - Necessary

****
* d i s t e l *
****

TO: see 'TO' DISTRIBUTION

cc: see 'CC' DISTRIBUTION

DATE: TUE 22 FEB 1983 9:46 PM EST
FROM: NICK CORSEN
DEPT: CORP PRODUCT MGMT
EXT: 223-6123
LOC/MAIL STOP: ML12-1/-T39

SUBJECT: MARKET GROUP SURVEY -- SURVEY DATA

	FRS DATE	FY83 K $'S	T E U	T V D	C M G	S S G	S U M
16-BIT PROGRAM							
VAXON U. C	04FY84	4300	0	2	1	2*	5
LSI-3	01/02FY82	1800	0	0	1	2	3
LLL-B	01FY84	500	0	1	1	2	4
UNA TOOLS W2 ADAPTOR	04FY83	200	0	2	0*	1	3
RDTB ENHANCEMENTS		200	2	0	0	1	2
SUBSETS	02FY83					2	
SMALL BATCH AND UTILITIES	01FY83					0	
CETS W2 SUPPORT	01FY84	200	0	0	1	1	1
CFIS VAX DEVICES		1100	0	0	1	2	3
VAX ENHANCEMENTS		400	2	1	0	0	1
MERGE H AND M+	04FY83					1	
ENHANCED BACKUP	03FY83					2	
AVAIL REPORT FROM USER SPACE	02FY84					2	
VAX CMS DEVICES		100	0	2	1	1	3
RT ENHANCEMENTS		300	0	0	0	1	1
EXTENDED MEMORY	04FY83					2	
VAX BACKUP	04FY83					1	
CUSTOMER INSTALLATION	04FY83					0	
NT NEW DEVICES		500	0	0	0	2	2
FORTRAN FULL ANSI-77	01FY84	300	1	1	1	0	3
COBOL-81 REPLACE COBOL-11	04FY83	100	0	0	1	1	2
BASIC-PLUS-2 TRACK STANDARDS	02FY84	300	1	1	1	1	4
DSM-11 REWRITE	04FY83	100	0	2	0	1	3
RMS-11 REWRITE	03FY84	500	0	1	0	0	1
32-BIT PROGRAM							
11/780							
64K CHIP	02FY83	142	2	2	2	2	8
CI CLUSTERS/HI AVAILABILITY		800	2	1	2	0	5
COMMUNICATIONS SWITCH	FY83	330	2	0	2	1	5
11/750							
11730	01FY84	1106	2	0	2	0	4
FP750	SHIPPED	84	2	2	1	0	5

PACKAGED SYSTEMS	FY83	201	2	2	2	2	8
UNA/UDA	?	200	1	2	1	1	5
DW750	Q4FY82	299	1	2	2	0	6
11/730							
CDI80	Q4FY82	375	2	2	2	2	8
BATTERY BACKUP	Q3FY83	375	2	2	1	0	5
PACKAGED SYSTEMS	FY83	200	2	2	2	2	8
VENUS							
DEVELOPMENT	FY84	15300	2*	0	2	1	5
NAUTILUS							
DEVELOPMENT	FY85	6049	2*	2	2	2	8
SCORPIO							
DEVELOPMENT	FY85	6200	2*	2	2	2	8
WORKSTATION							
DEVELOPMENT							
- HIGH END BUYOUT WORKSTATION	Q2FY83	900	2	2	1	0	5
- LOW END WORKSTATION	3QFY83	5400	2	1	1	1	5
MICRO-VAX							
START-UP		1330	1	1	1	1	4
CHIP & BOARD SOFTWARE		1500	1	2	1	1	5
CLUSTERS/HI AVAILABILITY (SUBSET OF 11/730 PROGRAM)							
CI CLUSTERS	4QFY84				2	1	
HI AVAILABILITY	2QFY87				2	1	
32-BIT SOFTWARE							
ZSD	FY82	5324	1	1	1	1	4
VAX11 RMS	FY81	1211	2	0	2	2	6
VAX11 PL/1		621	0	0	1	0	1
HYDRA (DATA INTEGRITY)		1903	0	0	1	0	1
SMALL 32-BIT		1302	1	1	2	1	5
VAX11 RTL		890	2	1	2	2	7
VAX11 DEBUGGER		1118	1	1	2	1	5
VAX11 SORT/MERGE	FY83	1103	2	1	1	1	5
VAX11 EDITOR	FY83	365	2	2	2	2	8
VAX CROSS LAN TEST		90	2	1	2	0	5
VAX11 APL		332	2	0	1	0	3
VAX11 BASIC		890	2	1	2	2	7
VAX11 COBOL	FY82	950	1	0	2	2	5
VAX11 FORTRAN	FY82	413	2	2	1	1	6
VAX11 PASCAL V1.2		---					
VAX11 PASCAL V2.0	FY83	493	2	2	1	0	5
ADA	FY83	574	2	2	1	0	5
ADA PSE		332	2	2	1	0	5
DSTS	FY83	1037	0	0	2	0	2
IPSF	FY83	2058	0	0	2	0	2
IMS ARCHITECTURE		268	1	0	2	0	3
VAX11 DPPS	FY84	1352	1	0	2	1	4
UNIX32	4/82	425	2	0	1	2	5
RDMS-32	4/83	1057	2	1	2	2	7

DTE/DMF-32	FY83	759	2	1	2	2	7
DMF8/TF58 MACH		---			2		
CTC	FY82	---			1		
DHS-32		800	0	0	*	0	0

32-BIT PROGRAM

JUPITER SYSTEM

JUPITER HARDWARE (2080)	FY84	7075	1	0	0	0	1
JUPITER T30/COMM		1096	2	0	0	0	2
XI PLUTO		83	2	0	0	0	2
JUPITER HSC-50		119	2	0	0	0	2
JUPITER/20 COMM		576	2	0	0	0	2
JUPITER TOPS-10		0					

32-BIT SOFTWARE

APLEP	FY83	110	1	1	1	1	4
MACRO/LINK	FY83	40	1	1	0	1	3
FORTRAN-77	FY83	400	1	1	1	1	4

32-BIT FIELD USE

STARGET PRODUCT SOFTWARE		261	1	0	0	1	2
CLIFF		107	1	0	0	0	1

16-BIT COMM SOFTWARE

DECNET-11 S/W		70	1	1	0	0	2
X.29		23	1	1	0	0	2

TERMINALS & WORKSTATION PRODUCTS

VT Series							
VT50H	Q1FY82	$379	1	1	2	1	5
VT52	Q1FY84	160	1	1	2	1	5
CT CLUSTERS	Q1FY84	1074	2	1	2	2	7
CTAA (NI ADAPTER FOR CT)		599	2	1	2	2	7
PRINTING							
LA100RO	Q3FY83	500	2	1	1	2	6
LOW COST RO--BUYOUT	FY83	200	0	1	1	2	4
LOW COST RO--BUILD	FY85	1100	0	1	1	0	2
ELECTRONIC PRINTERS							
- EP1 (10-12 PPM)	Q2FY83	200	2	0	2	1	5
- EP3 (5-6 PPM)	FY86	700	2	0	2	0	4
KEYBOARDS (LA/VT/CT 200)		200	2	2	2	*	6

VIDEO

VT200-GX (LOW COST)	Q3FY83	1200	2	2	2	2	8
VT200-H (HALF-PAGE)	Q4FY83	2950	0	2	1	2*	5
VT200--FULL PAGE	Q1FY85	800	2	2	2	2	8
VT200 CUSTOM LSI	N/A	1100	2	2	1	1	6
VT200 SYSTEMS REF. MANUAL & PROGRAMMER'S MANUALS	N/A	150	2	2	1	1	6
VT200 INTERACTIVE I/O OPTIONS							

(LIGHT PEN/TABLET, ETC.)	N/A	235	2	2	1	1	6

OFIS PROGRAM

DECmail V1.1	Q1FY83	419	2	0	2	2	6
VAX/OFFICE R1	Q2FY83	1600	1	0	2	2	5
OFFICE/FRENCH	Q3FY83	100	1	0	1	2	4
OFFICE/GERMAN	Q3FY83	100	1	0	1	2	4
VAX/OFFICE R2	Q4FY83	---			2	2	
VAX/OFFICE R3	FY84	---			2	2	
RSX11M+/OFFICE R1	Q4FY83	200	0	0	0	2	2
CTAB/OFFICE R1	Q4FY83	2200	1	0	2	2	5
CTAB/OFFICE R2	FY84	---			2	2	
CTAB/OFFICE R3	FY84				2	2	

NOTE: Allocation of FY'83 spending to specific releases is especially arbitrary in the case of OFIS.

DISTRIBUTED SYSTEM PRODUCTS

(Glossary of terms on p. 10 of Distributed Systems section in "Presentations to Operations Committee--March 1982")

UNIBUS OPTIONS							
HDLC SUPPORT IN DMP	H1FY84	250	1	1	1	0	3
DMZ32	H1FY84	PL FUNDED	1		2		
QBUS OPTIONS							
DZV-8	H1FY84	400	0	1	1	2	4
HDLC SUPPORT IN DMV	H1FY84	250	0	1	0	0	1
CI HARDWARE							
TRANSCEIVER	1/83	40	2	2	2	0	6
CNA	6/83	640	2	2	2	0	6
TRANSCEIVER POWER SUPPLY	H1FY84	100	1	1	1	0	3
PLUTO	9/83	1070	2	1	0*	0	3
LSI CNA	FY86	250	0	2	0	0	2
INTELLIGENT CNA	FY86	400	2	2	1	0	5
PLUTO JR.	H1FY85	600	2	1	0*	0	3
LNI	Q1FY84	300	2	2	2	0	6
BROADBAND TRANCEIVER	H2FY84	500	2	2	2	0	6

NOTE: MSI CNA is funded out of PSD;
CINA is funded out of CI Program.

DECNET							
DECnet RSX (PIV & NI)	Q3FY84	422	1	2	1	2	6
DECnet VAX (PIV & NI)	Q4FY83	1200	2	2	2	2	8
DECnet E (PIV & NI)	H2FY84	500	0	0	0	2	2
X.25 (STANDALONE PSI PRODUCTS)							
VAX PSI	6/82	60	2	1	2	1	6
RSX PSI	3/83	100	1	1	1	1	4
SERVERS							
SERVER BASE	34FY83	568	2	1	0	1	4

ROUTER-	Q1FY84	283	2	1	2	1	6
X.25 GATEWAY	4/84	440	2	1	2	0	5
SNA GATEWAY(NON NI)	2/83	484	2	0	2	0	4
SNA GATEWAY(NI)	Q4FY84	460	2	0	2	0	4
TERMINAL CONC.	9/83	560	2	1	OK	0	3
XEROX GATEWAY	M2FY85	309	0	0	0	0	0

CROSS SYSTEM COEXISTENCE SOFTWARE

20/VAX COEX COMPUTERS		220	2	0	0	0	2
20/VAX DATA CONVERSION SUB		73	2	0	0	0	2
20/VAX DIU		293	2	0	0	0	2
20/VAX MSG TRANS SYST/MTS		219	2	0	0	0	2
20/VAX REMOTE FILE ACCESS		142	2	0	0	0	2
20/VAX REMOTE SPOOLING & BATCH		73	2	0	0	0	2
GRAPHICS		556	1	2	1	0	5

DECnet PRODUCTS

DNA1	Q1FY85	2343	2	2	1	2	1
DDCMP/S1	3QFY83	923	2	2	1	2	8
NETED	Q4FY82	6160	0	2	1	2	9
DCP80	Q1FY83	5170	2	1	0	2	7
NCP	Q4FY83	750	1	1	0	1	7
DNA3	Q3FY83	4411	1	1	2	1	1
DNA1/DNA3	4Q84	1000	2	1	2	1	1
DTU	Q3FY83	420	1	1	0	1	4
DNA-II	Q1FY84	1000	1	1	1	1	5
NXDU	3QFY83	500	1	0	1	0	2
DNTN	Q3FY84	4210	1	1	2	1	6
DNTN	FY86	1070	1	2	0	0	3
DECnet IV	Q4FY85	350	0	0	1	2	3
DNA2	Q1FY85	(WITH DNA1)	1		1	1	3
YANKEE	FY87	500	1	1	0	1	3
HSC DACHE	2QFY84	1000	2	0	2	1	5
SHRIMP	FY82	0			1		
HSC (SI TO SI ADAPTER)	Q4FY87	0		1	1		
DN62	Q2FY85	2080	0	1	2	2	6
RX62/63	Q3FY85	600	0	2	1	2	5

ITEMS NOT IN BASE PLAN

J-11 FPA		500	?	2	1	0	2
HIGH AVAILABILITY NEXULA		?		2	1	0	3
DN200 (CONSYSTEM DIG. NUMBER)				1	1	1	3
DECPLOT				0	2	1	3

SURVEY BACKGROUND INFORMATION

The survey list submitted to the Market Groups contained 142 Engineering projects with deliverables. In general, P/G-funded projects, pure maintenance spending, SCD funding, FCC activities, noncontractual or legal commitments, advanced development, tool/process development, research, and one-of-a-kind activities were excluded. The dollar figures for FY'83 were intended to give a rough feeling of project scale. The rules for allocating dollars to individual Engineering projects are not consistent across the groups so precise comparisons should be avoided.

The sum of the ratings from each Market Group for a particular project gives a rough feeling for the business significance of that project. The values range from 0 to 8. Projects such as Scorpio, VMS and RA81 were rated 8 (a 2 from each of the four Market Groups). Two-thirds of all projects rated 4 or higher. Two received no support. The distribution of the "scores" was

0	1	2	3	4	5	6	7	8
1%	7%	14%	9%	9%	20%	15%	8%	11%

There are a few points to keep in mind in interpreting the results. The Lands Sustain Group skipped through our survey net. Neither the 383 nor the "81" Market Groups included that P/G in developing their ratings. So the time the problem was discovered, it was too late to fix. Obviously, this caused lower ratings for Ga-Sin Program projects and possibly for others such as the six 20/VAX Cross System Peripherals projects.

Dollars were also normalized in the way each Market Group did their ratings. Some rated only projects with numerical spending in FY 83, but a few gave ratings even to projects with pure dreams, wish, some Groups also rolled up sub-components of a project, rather than diluted the bonds. All the individual Market Group ratings are shown, but a dot is asterisked only for those projects which three or more Groups rated.

Finally, the Market Groups wanted to rate five items which were not in Engineering's base plan. They are shown in the Survey Data documents but are not included in the tally above.

THE LOWER RATED PROJECTS

0 Rating (No Support from any Market Group)

32-Bit Sys- PMS-32 — Dist. Sys - Xerox Gateway

1 Rating (One Market Group Rates as 1 -- Some Significance)

16 Bit Sys- RSTS NI — 36-Bit Sys- Jupiter Hardware
RT Enhancements — APLSF
FMS-11 Rewrite — Macro/Link
32-Bit Sys- VAX-11 PL/I — FORTRAN V. 7
Dist. Sys - HDLC for DMV — KLIPA

2 Ratings (Two Market Groups Rate as 1 -- Some Significance)

16-Bit Sys- COBOL-81 — Term & WS - Low-Cost RS--Build

3 Ratings (Three Market Groups Rate as 1 -- Some Significance)

16-Bit Sys- FORTRAN Full ANSI — Dist. Sys - HDLC Support for DMF
Libraries - Various — Transaction Power Sup.

4 Ratings (Four Market Groups Rate as 1 -- Some Significance)

16-Bit Sys- Basic Trans. DLC. — Dist. Sys - X25 PSI

5 Ratings (One Market Group Rates as 2 -- Substantial Significance)

16-Bit Sys- RSTS Enhancements — 36-Bit Sys- Compiler Projects
RT New Devices — DF10 - KBA-11M/OFFICE
32-Bit Sys- Nodra (Internet) — Dist. Sys - LSI DMC
Data — DECnet/E
TP68 — Cross Sys - 8-16/PDX Products

SURVEY DATA FOOTNOTES

Because of EMS page size restrictions, the interpretation of the
responses in the Survey Data is presented here.

[illegible] PROGRAM

OVERALL -- "The Commercial Group supports minimizing PDP-11
investments. One exception is where it carries over to the
CT."

ORION -- '1' for Qbus Orion; '2' for Unibus (Small System Group)

QNA (QBUS NI ADAPTER) -- "QNA is not needed to connect to Qbus
systems. The only possible need is if Engineering is building
file servers, gateways out of Qbus systems." (Commercial Group)

[illegible] PROGRAM

[illegible]
[illegible]
[illegible] -- See Technical End User Group issue about [illegible] ENS.

[illegible] -- "CATS and PNS-11 are dimensions, who invest close to 40% in
two products that are almost the same." (Commercial Group)

[illegible] [illegible]

[illegible] -- "I, Small System Group, [illegible] [illegible] in this
field. Presumably, all individual [illegible] based on their
support for the product using the DataCenter but no one from
ISG was available to provide information."

[illegible] -- "If needed for VAX" (Small System Group)

DISTRIBUTED SYSTEMS

[illegible]
PLUTO, JR.
TERMINAL CONCENTRATOR -- "Pluto as a gateway is needed as a 2. Pluto
as a terminal concentrator in its current implementation is a
zero. Must be redefined to be useful." (Commercial Group)

ITEMS NOT IN BASE PLAN

[illegible] FPA -- "Orion without a floating point accelerator is a waste of
time and money." (Tech End User Group)

"[illegible] DISTRIBUTION:

JOE CAMPBELL	MIKE GALLUP	ROSE ANN GIORDANO
GVPC;	MARCUS DIX REYES;	BILL MORRIS
PCD;	JOEL SCHWARTZ	BRUCE STEWART
TECH. GROUP STAFF;	TVG STAFF;	

TCC DISTRIBUTION;

GARY J ECKROTH	EMGPPC;	ELI GLAZER
DICK RISLOVE	TGMC;	TVG-MSTAFF;

The following is offered as a summary of the Technical Group's issues with the Engineering Base Plan as presented in the March, 1982 "Presentation for Operations Committee Review".

Tech

Engineering Financial Overview:

The Technical Group has an issue with the 16 Bit Program allocation. Engineering spending in FY82 for 16 bit products goes from 3.1% of 16 bit NOR with a 3 year offset to 4.52% for FY84 spending. This product should be milked as a cash cow, not increasingly invested in.

The 32 bit expenditure in FY83 appears correct, however, growth of only 15% to FY84 and a reduction of 18% to FY85 is outrageous. This certainly does not relate properly to our revenue expectations. We see nearly a 100% growth in 32 bit business per year. What is a realistic three year spending plan?

There are questions as to whether our long term business expectations are properly aligned with the rapidly increasing investment in storage. This must be more fully explored over the next year.

32 Bit Investment:

The majority of VAX customers for the 1980's already own one VAX. Our customers are acutely aware of the long term implication every time they buy a computer system. The investment the customer is making in software, plus the applications he is buying are required to be safe over time. The familiarity the users accumulate with the system should have a long term payoff. The customer expects us to allow him over time to: continue to distribute his system, increase his systems MIPS, and move users between systems with little or no disruption. The better we can satisfy these expectations, the longer the customer stays with Digital. Unfortunately, because of the presentation of the 32 bit strategy as projects and CPU's, and the same for storage, communications, and software, we have trouble feeling comfortable that our product direction is meeting the customer's long term investment requirements.

There appears to be an overlap between Venus and Nautilus. Where we are talking about $50-100 million develop projects, we have to be sure we have sufficient market for multiple products. It certainly appears two Nautilus attached together give us greater power than the Venus with less cost at about the same FCS. Although Venus will do better in

single large program execution, I doubt that market justifies the product. Can we get through the next 2 years without spending a total of $50 million on those two overlapping products? Time to market is the top priority in this space. Technical customers buy early in the life cycle of a product of this class because of their performance requirements.

We seem to be losing focus on the real time data acquisition/analysis hardware and software. The real time needs of our laboratory, government, and other technical markets. What is the plan to move the real time customer onto our 32 bit products? Right now the product groups are focusing their development on this space.

We need high speed access to our 32 bit CPUs. We need a CI gateway to a high speed industry standard bus (like hyperchannel). Also, we need high bandwidth DMA access to 32 bit products in the 30-40 Mbytes/sec range.

When will we see a plan, and where is the funding for a Scorpio Based Workstation? What effort does the change in Scorpio strategy have on workstations? This product is a survival issue in the laboratory space.

Distributed Systems:

The Technical Group will not be able to sell local area networks the same way we have previously sold computers. We are going to have to understand the additional features and benefits we offer our customers with an Ethernet Network versus the traditional minicomputer with terminals. Announcing the Ethernet products nearly a year before availability makes us uncomfortable about properly presenting the products to our customers. We must figure out how we are going to package network offerings. How can Engineering help the product groups through this difficult transition?

Why do we continue to invest in Q Bus connunication? Is there proper business justification? We don't see any.

"TO" DISTRIBUTION:

NICK CORBEN
TGMC:

PEG:

TECH. GROUP STAFF:

digital

INTEROFFICE MEMORANDUM

TO: Participants in the PEG/GVPC Staff Meetings

DATE: 5 March 1982
FROM: Eli Glazer
DEPT: CORP. PRODUCT MGMT.
EXT: 3-4434
LOC/MAIL STOP: ML12B-T61

SUBJECT: ATTACHED DRAFT MINUTES

The following are DRAFT sets. Some preliminary review by members of the PEG organization has taken place. No one in the Market Groups has yet had a chance to review these minutes. Please communicate all corrections to me as soon as possible. I recommend all serious misinterpretations be clarified directly with GVPC.

I intend to issue a corrected set of minutes by approximately Friday, March 12th. If you need copies of referenced material, please call my office.

EG:kr4.5

DISTRIBUTION:

PEG:	Andy Knowles & Staff	Julius Marcus & Staff
W. MacKenzie & Staff	Win Hindle & Staff	Ted Johnson
Ron Smart	ENGPPC:	Joe Reilly

+------------+
d i g i t a l

INTEROFFICE MEMORANDUM

EG:kr3.46
TO: PEG: ENGPPC:
DATE: 2 March 1982
FROM: Eli Glazer
DEPT: CORP. PRODUCT MGMT.
EXT: 3-4434
LOC/MAIL STOP: ML12B-T61

SUBJECT: DRAFT OF PEG/GVPC COMML GRP MINUTES FEB 25 8:30-NOON

DRAFT PEG/COMML GRP MINUTES FEB 25 8:30-NOON

ATTENDEES: Bill Avery, P. Courtin, Gordon Bell, Bill Demmer, D. Fernald, Bill Johnson, M. Gutman, J. Marcus, B. Lacroute, G. Saviers, John Adams, Bob Flynn, Ted Johnson, Walt Hanstein, Don Harbner, Ray Mercier, E. Glazer, R. Corben, G. Eckroth, D. Rislove

ATTACHMENTS OR REFERENCE DOCUMENTS:

MARKET GROUP SURVEY FM CORBEN (FEB 23)
POSITION STATEMENTS FM EKROTH (FEB 22)
AGENDA

ACTION ITEMS:

WHO/WHEN	WHAT
1) Rislove	Comml definition of 500+ terminal application (i.e., MAIL, VIDIOTEX, TRANSACTIONS, etc.).
2) Eckroth	General RSTS End of Life Spec. Especially with respect to communications. To be worked with CONKLIN
3) Lacroute	Drive review of VTC and PLUTO overlap. Define performace objectives of PLUTO.
4) Rislove	RISLOVE to input Comm'l MKT Spec for LAN (Local Area Network) Protocols, Performace, Installation Issues. Data to be directed to LACROUTE
5) Lacroute/FRI. (2/26?)	Draft of Broadband, Baseband and Total LAN approach, Handbook due from task force (ADAMS, ROGERS, et al.).
6) Rislove	Aid LACROUTE in defining MKT Spec for LAN (i.e., Protocol, Response Times, Performance, etc.).

ACTION ITEMS:

WHO/WHEN	WHAT
7) Courtin/APR 15 (?)	Proposal on T-Carrier for PBX to company using outside vendor. LACROUTE and COURTIN will drive to resolution and follow
8) Saviers	SAVIERS and JOHNSON to each assign one person to see ~~that~~ shadowing ~~is~~ can be included in the microcode of the UDA.
9) Rislove	Communicate Comml's view of high productivity language tools
10) Fernald	Update the projection of 16Bit systems planned shipments for the Commercial Group.
11) B.JOHNSON/MAR 15 (?)	Converge the DECPLOT/GRAPHICS developments between the OFIS and Data MGT Development groups. Proposal due in several weeks. RILSOVE will monitor for Commercial Group.
12) Avery	Produce a roadmap (i.e., issue definition, goals, alternatives, etc.) for voice products.
13) Courtin	Provide AVERY with help in defining the mkt objectives involving Videotex applications
14) Avery	Resolve standard vs special keyboards
15) Rislove	Help AVERY in defining the spec for PLP and CEPT (Videotex Graphics Protocols). Represent Comml on VT125 Graphic Compatibility issues.
16) T.Johnson	Ask National Account Managers about need for compatiblity with IBM personal computers. What are the potential issues in their accounts?

The topics generally follow Gary Eckroth's February 22nd memo.

TOPIC	DISCUSSION
********** 32BIT PROGRAM **********	
High Availability in 32b Program	RISLOVE: Not a Tandem. COURTIN: Nebula on CI. LACROUTE: On the NI? DEMMER: Current program excludes a low-end high availability. SCA software should be utilizable at low end for consistancy. COURTIN: There is a multi market group task force considering the topic.

TOPIC	DISCUSSION
500+ Terminals to a VAX System	MARCUS: EMS, Videotex, Transaction Processing are all different. Don't care about a 500+ transactions processing. COURTIN: We limit ourselves to about 64 terminals on a VAX. LACROUTE, BELL: Factors are the number of users, duty cycle, active vs passive. Use of PLUTO type approach. COURTIN: Need to put PLP, Videotex protocols on the VT100 so that only one terminal needs to be on a desk (see ACTION ITEM 1).
Scorpio Schedule	COURTIN: 16b business is fading fast, we have a 32b low end problem. DEMMER: Chip cannot be accelerated. Systems could be accelerated by a quarter (3 months).
Joint Goals	ECKROTH: This part of the 32b program is a very positive step.
Program Office should increase systems approach	ECKROTH: Use approach of 16b Office interaction with P.G.'s as a model. O'KEEFE: We did not get response to incremental revenue questions (?).
Nebula Pricing and RSTS	MARCUS: With Nebula pricing we'll see RSTS - 16b systems go away. P.CONKLIN: How much should be invested in RSTS? MARCUS: Commercial will define what needs to be done to RSTS. We must keep customer commitments (see ACTION ITEM 2).

********** DISTRIBUTED SYSTEMS **********

Communications Concentration and Router	RISLOVE: Resolve overlap of VTC, PLUTO and 11/23 communications application. LACROUTE: PLUTO with 16 lines will transfer at $4.5K, with 32 lines at $6K. PLUTO is most effective with, forms, WPS, EMS ... for off loading CPU. Need to define PLUTO functionality (see ACTION ITEM 3). LACROUTE: I do not see the LCP-5 as a solution. CONKLIN: I'll monitor that from the stand point of the 16b program.
Bisynch on Combo board SNA gateway performance baseband and broadband	LACROUTE: Agreed but what do we give up to get it? ECKROTH: That is a function of performance. LACROUTE: We're working with OEMS to get a product as fast as possible 3M baud looks good, 10M baud is possible. A draft of the LAN (Local Area Network) handbook is due February 26. Engineering needs a marketing party line on customer needs and questions. MARCUS: Customers don't know what questions to ask (see ACTION ITEMS 4 and 5).

TOPIC	DISCUSSION
Network security	LACROUTE: Project plan is done and will be distributed. ADAMS: Access control applications software is being done in the Software Engineering Group.
Remote DECNET for CT	ADAMS: Should bw do a software DDCMP? MARCUS: How many protocols does DIGITAL need? I'd like direct SNA support within CT. LACROUTE: 3270 is what is needed. MARCUS: We need to define location of the machines and decide what are the best protocols. This has an impact on CT and OFIS. LACROUTE: Mail and file transfers are the applications being looked at. COURTIN: We know what the applications are what we don't know are the number of lines, performance, speed and response times. MARCUS: Customers are confused. Let's define 1)document protocol (e.g., SNA/3270); 2)wiring the building; 3)where are the files; 4)where are the editors; 5)security; 6)network functionality; 7)IBM interconnect; and 8) performance. LACROUTE: I'd drive this with commercial input from RISLOVE (see ACTION ITEMS 4, 5, and 6).
CX/DX focus	BJ: CX/DX belongs to the OFIS program.
Coordinate file servers effort	LACROUTE: LAN task force (STRECKER, TRAVIS, MILLER, ADAMS, ROGERS, LACROUTE, LAUCK, et. al.) will report in about one month.
T-Carrier to PBX's	LACROUTE & COURTIN: Northern Telecom joint proposal in 4 to 5 weeks (see ACTION ITEM 7).
Bidirectional SNA gateway and IBM	COURTIN: CI DECNET performance is poor. LACROUTE: The goal is to improve DECNET performance by a factor of 2.

********** SOFTWARE ENGINEERING **********

CAT and FMS are diverging	BJ: CATS is layered on FMS; they will converge.
Fourth Generation languages and resource dictionary	MARCUS: High productivity tools are needed. RISLOVE: Fourth generation language and DATATREIVE extensions are a higher priority than the resource dictionary but both are in Scenario B and not being proposed.
Multifunction (MFS) proposal DEC's answer to the IBM System 38	BJ(?): We'll be making a statement to the company.

TOPIC	DISCUSSION
Shadowing on MASSBUS disks	BJ and SAVIERS: Each of us will assign a person to see that shadowing is done in the microcode (see ACTION ITEM 8).
Distributed DATATREIVE for CT	MARCUS: Let's define it once and do it that way forever. BJ: A proposal is coming for distributed functionality with DATATREIVE and editing as examples.
EPI - "Electronic Printer software"	AVERY: Craig James, program manager, owns that. Definition and schedule are being developed.
Large number of VIDEOTEX terminals on VAX	BJ: Bruce Parker will demo next month in Spit Brook. AVERY: Do we have a party line for DEC involvement with VIDEOTEX? COURTIN: I'll help. We already have a lot of equipment involved with VIDEOTEX applications (see ACTION ITEM 13).
Goodness	MARCUS: We've got the best 32Bit hardware and software ... and networks with the most flexibility and best performance.

********** OFFICE SYSTEMS PROGRAM **********

Two DECPLOTS one for DP and one for OFIS	MARCUS: What is DEC going to offer graphics? AVERY: Terminal Software Strategy task force (STRECKER, et. al.) is two months from a report. They will cover the graphics objective. The task force deals with a terminals software strategy only (i.e., OS/terminal communication, etc.). MARCUS: DECPLOT could be a marketplace standard. BJ: Proposal is due in two weeks for how a single DECPLOT will be done (see ACTION ITEM 11).
VIA integration with Distributed Systems and CT	BJ: That's part of the terminals and terminals architecture issue.
OFIS on RSX-11M is not needed	No comments
OFIS should accomodate IBM high level document protocols	BJ: This is part of OFIS architecture. LACROUTE: Offer some software on the IBM machine as a special support service like the SNA service (being?) planned.
VOICE, IMAGE, PRINT SERVERS, etc	MARCUS: VOICE needs defining and a road map (e.g., digital analog, etc.). What will the product set be? AVERY: I'll do it (see

TOPIC	DISCUSSION
	ACTION ITEM 12).
Wide Carriage Support	MARCUS: The accountants produce spread sheets so big they call the bedsheets. We can't sell unless our software supports 158 to 212 characters/line. BJ: The Office program is looking into this.
********** STORAGE SYSTEMS **********	
MAYA, YANKEE	SAVIERS: MAYA is 100MB with the performance of a TU15. We're looking into pulling FRS into Q1FY85 from Q4FY85. The market is tape for the 5 1/2 form factor. MARCUS: What is the competition? alternatives? SAVIERS: Floppies in the near term. AZTEC is a better solution for LCP8. I am not comfortable with our 5 1/4 form factor products. We have no effort in the 3" form factor product category. ECKROTH: File servers will impact the need for 5 1/4 back up devices. GUTMAN: Volume back up versus file back up will resolve the issue. SAVIERS: We need a delivery mechanism for 10's of MBytes of software and training. MARCUS: We need long term solutions for the distribution problem.
Optical Disks	SAVIERS: Optical audio disks are a potential. We need an entreprenur to define the product. The high $ end is write once, the low end is replicated media. Customer services is doing an Industrial Interface to CT. A 4 Gigabyte write once optical disk is $40K to 60K sell price. Xerox wants to OEM a 1 Gigabyte disk for $5K cost. NOTE that an RA81 and TU81 can offer 1/2 GB at the same cost as a write once optical disk.
RDMS in HSC	SAVIERS: That's in advanced development. We're working with INTEL and universities for LSI versions of a solution.(?) We will propose an acceleration of the project.
Mini AZTEC vs RD52	SAVIERS: The next generation of 5 1/4 form factor needs more work on VLSI to work with 5 1/4 drives. MARCUS: Here the role of file servers needs to be defined.
********** TERMINALS AND WORKSTATIONS **********	
Special vs Standard keyboards	AVERY: One keyboard for all applications is a goal. MARCUS: Clerks will not buy complicated keyboards (see ACTION ITEMS 14).

TOPIC	DISCUSSION
PLP and CEPT graphics protocols	(See ACTION ITEMS 1 and 15).
Funding for a Print Server	LACROUTE: Isn't this a small system with some applications software. AVERY: Is there an application other than with clusters? RISLOVE: This is on shared printer as a resource in one office.
Block mode terminals	LACROUTE: DMP code has been changed to HDLC or SDLC. ECKROTH: What are systems going to do with block mode terminals? AVERY: We need a terminals software group. BJ: We are setting up a system to look at performance limitations of "servers."
Overlap of CT25 and VT200	BJ: The full spectrum of use of intelligent to dumb terminals needs to be defined. (?)Let's forget about intelligent terminals because in three years the CT will be cheap enough so that the intelligent terminal is not required. JOHNSON, AVERY, LACROUTE: Once you do block mode, then the basic dumb terminal must do it. Block mode as an option makes no sense. AVERY: A VT200 with 1/2 page graphics costs $900; without block mode it's $750 to $800. BJ: RISLOVE should talk to DAILY, LACAVA, and MCINTYRE about the terminal architecture.
Need for compatiblity with the IBM file/data personal computer software	AVERY: We could go third party as in SNA applications. T.JOHNSON: We could ask our National Account Managers about the penetration and compatibility need with IBM personal computers. MARCUS: The commercial customer base is dominated by IBM.
CT emulation of the VT125	AVERY: CT emulation of the VT125 is a product goal. MARCUS: Can we demonstrate that now? RISLOVE: I'll represent commercial needs with respect to VT125 needs.

********** 16B SYSTEMS **********

Commerical group requirements	MARCUS: Let's define exactly what the 16B requirement is for the Commercial Group (see ACTION ITEM 10). GUTMAN: We're prepared to build 300 to 400 11/70 systems for customer availability after

TOPIC DISCUSSION

October 83 (next key FCC cutoff date).

********** GENERAL **********

MARCUS: Is the chip investment right?
MARCUS: Office pieces must be discussed. ULYSSUS may have been overlooked but is needed to make OFIS work.

+------------+
d i g i t a l
+------------+

INTEROFFICE MEMORANDUM

TO: PEG: ENGPPC:

EG:kr4.2
DATE: 3 March 1982
FROM: Eli Glazer
DEPT: CORP. PRODUCT MGMT.
EXT: 3-4434
LOC/MAIL STOP: ML12B-T61

SUBJECT: DRAFT OF PEG/TECH END USER GRP MINUTES 25 FEB 1-5PM

DRAFT PEG/TECH END USER GRP MINUTES FEB 25 1:00-5:00PM

ATTENDEES: Bill Avery, Win Hindle, Bernie Lacroute, Grant Saviers, Rick Corben, Don Harbner, Herb Shanzer, Walt Hanstein, Mary Altenhof, Ray Mercier, Dick Strauss, John Buckley, Harvey Weiss, Bill Long, Bill Demmer, John O'Keefe, Bob Trocci, Mike Gutman, Ulf Fagerquist, Eli Glazer, Cecilia d'Oliveira, John Adams, Bob Flynn, Bill Johnson, Ted Johnson, and Ed Schmidt.

ATTACHMENTS OR REFERENCE DOCUMENTS:

MARKET GROUP SURVEY FM CORBEN (FEB 23)
TG RESPONSE TO ENGINEERING BASE PLAN (FEB 19)
AGENDA

ACTION ITEMS:

WHO/WHEN	WHAT
1) John O'Keefe	DR780 COST ISSUE (?) Report by Kurt Friedrich on I/O performance of VMS
2) Bill Johnson	I/O, real time performance studies to be distributed - will come out in Sales Update
3) Bernie Lacroute	The standards for an interface to NI will be published (?)
4) Bill Johnson	MARY ALTENHOF to document concerns about V3A and TREVOR will get back
5) Harvey Weiss	Will see that a Technical Group character set is defined
6) Mike Gutman	Will review 0 and 1 voted items to test impact on budget
7) Bill Avery	Will get help from Technical Group on the specification for a CT Tech Workstation

TOPIC	DISCUSSION

The topics in the first part of the minutes generally follow Dick Strauss' memo of February 19.

********** 32BIT PROGRAM **********

Dual Nautilus vs Venus product overlap	FAGERQUIST: Design simulation of Venus shows a 4.2 to 4.4 times VAX11/780 performance which is better than expected. We are still looking at a dual Nautilus. STRAUSS: The performance data on a dual Nautilus and Venus are needed to fine tune the Technical Group's decision on Venus.
32b Real Time hardware and software	O'KEEFE: The DR780 cost is continuing to be worked. Kurt Friedrich will report on the overall speed/performance of this option. DEMMER: NEBULA is comparable to an 11/44 for hardware and software I/O performance. HINDLE: What is the real time band width requirement? B.JOHNSON: There's nothing inherent in VAX/VMS software that prevents good response time. We will distribute studies of the VAX/VMS I/O performance. HINDLE: Is there anything in the B & C scenarios for high speed I/O on 32b systems? GUTMAN: We're doing an advanced development J-11 front end study. O'KEEFE: We took lack of response from the Market Groups on the DR750H as a reason to cut back on it's development.
Scorpio Workstation	O'KEEFE: FY84 and FY85 systems allocations seem smaller because we are working on FY83 budget problem. There will be more Scoprio product projects in 84 and 85. DEMMER: We need input on the Scorpio 85 type workstation.

********** DISTRIBUTED SYSTEMS **********

How to sell LAN (local area network)	LACROUTE: We are working with the service ogranizations to deliver a proposal shortly.
Limit Q-BUS communi-cations options	GUTMAN and LACROUTE: The Technical Volume Group and Small Systems Group requires the product.
Consistent NI	(See ACTION ITEM 3). B.JOHNSON: What operating systems should support NI? STRAUSS: VMS, CT, RSX (Unibus).

TOPIC	DISCUSSION
********** SOFTWARE ENGINEERING **********	
When V3B VMS	B.JOHNSON: June 83. 12 months after V3A. ALTENHOF: RDMS support in V3B (see ACTION ITEM 4).
Manage the User interface	B.JOHNSON: One type of universal interface is not suitable for all types of users. STRAUSS: TPSS menu vs Commercial is inconsistent (?).
CI/CLUSTER Management	DEMMER: Recognize need for heterogenious cluster support including load balancing, but I'm not sure when. (B.JOHNSON: Needs to communicate CI/CLUSTER management objectives.)
Server Strategy	LACROUTE: I am chairing the task force to define the server architecture and components etc. We're several months away. The first specification will be for a VMS or RSX via DECnet and NI (?).
FIPS BASIC, common data dictionary (CCD) for FORTRAN, PASCAL, and ADA	B.JOHNSON: I need to get my engineers inputs.
NO CATS or TPSS	No comment
NO AD HOC UNIX support	B.JOHNSON: Engineers answering questions are supporting TIG. GUTMAN: The UNIX engineering task force will come to a party line recommendation in about 30 days.
Cut 16b O.S. support from CE budget	STRAUSS: Get down to RSX and MICROPASCAL. GUTMAN: The issue is: how agressive should phase out timing be? The Technical Group 16b systems business is $167M in FY82 and $153M in FY84. JOHNSON and GUTMAN: We are working the software support, after warranty, engineering support cost with the service organization.
********** STORAGE SYSTEMS **********	
AZTEC	STRAUSS: The Technical Group is not profitable in the $20K to 50K sell price range except for multiple systems. WEISS: GSG did not vote 'no' for AZTEC.

TOPIC	DISCUSSION
Develop for $50K-400K system range. Buy out elsewhere	SAVIERS: We're competitive with the IBM 3380 with multiple RA81's on a cost per megabyte and on a megabyte per cu. ft. GUTMAN: We need to communicate the multiple RA81 competitiveness. WEISS: Did not realize we were that competitive. SAVIERS: Are FIP's I/O standards a problem with government sales? WEISS: No, because we're a volume contract supplier, we are an exception.
********** CT and TERMINALS **********	
First release of CT doesn't have Technical Workstation function-ality	AVERY: Need help with definition (see ACTION ITEM 7).
Full Page sooner no Half Page	AVERY: Are you sure with respect to Europe? Cost will go up by a factor of 2 (?). STRAUSS: Customers will pay the higher price for Full Page. AVERY: Please test with your customers. WEISS: Why the cost difference? AVERY: Half Page is off the shelf technology components. Full Page components are very expensive. We've looked at buyouts as well. STRAUSS: Terminals software. B.JOHNSON: AVERY and I are working the architecture (for Full Page?). AVERY: The issues of higher functionality include graphics, character types, multiple windows, etc., which cannot be done on a 12 inch monitor.
LA100 Support	STRAUSS: We need mixed graphics and text utility software.
REGIS support on CT	STRAUSS: The problem is you cannot run the CT as a standalone and as a REGIS graphics device. VT125 emulation is not enough. BILL WISE will work with AVERY and JOHNSON. AVERY: I've got to understand the multiple use issue.
Low cost RO	HINDLE: Doesn't seem to be supported by the product groups as an engineering project. AVERY: The technology is needed in-house for high volume manufacturing issues.
********** REMAINING ISSUES **********	
BI Chips	SAVIERS: Is there a need for high BW I/O?

TOPIC	DISCUSSION
	STRAUSS: We need fast I/O in the 20MHz to 30MHz bandwidth range to do satelite data aquisition, particle physics and graphics. WEISS: We used to be leader with VAX and don't want to lose the market. DEMMER: The BI is basic to the Scorpio structure. It is the board interface of the future and the bus structure for future systems. HINDLE: We need a Technical Group task force to define the real time need (ACTION ITEM for STRAUSS?).
ORION without FPP is a waste	GUTMAN: Agreed, it's a $1.5M budget problem.

********** OFFICE SYSTEMS **********

Not enough features for the Technical Market	STEWART: Charlotte flow control permits integrating tools for the professional. We're working on getting graphics into Version 1. WEISS: Can we integrate Graphics and Text?
Integrated graphics and text in OFIS is needed	STEWART: We have a Graphics and Text print-out capability now. Use of the dictionary is not optimum now. Who can I interface with in the Technical Group for details? (STRAUSS for follow-up?) JOHNSON: OFIS on RSX? STRAUSS: No. WEISS: Need to research the value of OFIS on RSX. STEWART: Last year the Tech End User Group said no to a technical character set in WPS. HINDLE: Let's get it defined now (see ACTION ITEM 5).

********** GENERAL - CANDIDATES FOR CUTBACK **********

STRAUSS: Here's my FY83 cut recommendations - $26M+

TECHNICAL GROUP	FY83 $M
Cut 16b spending to 3.1% of NOR in FY86	9.0
Do NO CATS, TPSS, NOR TMS	5.4
NO RX52, 53 or RD52	2.7
No Half Page	2.95
Stop PL/1	.6
No XRX Gateway	.3
No LO Cost RO	1.3
No BI Chips	1.0
No HYDRA	3.0
No OFIS for secretary or manager	
Stop VENUS/NEBULA overlap	—
	=======

TOPIC	DISCUSSION
	Approximately $ 26.0M
168 Issues	GUTMAN: What the TG needs to do is tell us is how you rate high priority items (marked 2), so we can compare with other Market Groups. HINDLE: Mike can you review the "1" votes to see if cuts are possible? GUTMAN: I'm doing that. WEISS: Should be offer RSX-11 at $50 a copy with the F-11 chip set just as we're doing with RT-11 on the T-11 chip. GUTMAN: Being worked with LLOYD FUGATE.
HYDRA	HINDLE: What about the status of HYDRA? O'KEEFE: The HYDRA budget also includes Cluster management and load balancing. HINDLE: The 32b program needs to educate the company on this. CATS and TPSS were not supported well by the survey.
********** COMMENTS FROM THE PRODUCT GROUPS **********	
	HINDLE: I'd like each P.G. manager to summarize his views.
LDP	LONG: Our future is in the Real Time area. There is no follow on to MINC and no low-end front end. Data collection must be fast enough. Instruments on the laboratory bench must connect to the computer. GUTMAN: A front end-11 might be the answer. LONG: Regarding OFIS, 40% of our sales are in the corporate labs and 60% in universities. They tend to be associated with defined tasks.
ECS	TROCCI: Text and integrated graphics beyond graphics and WPS is a key need. Schools need baseband and/or broad band local connections. We also need a common single terminal user interface to avoid need to retrain on new DEC products.
ESG	ABBOTT GILMAN: We cannot sell less than $50K transactions profitably. AVERY: We need to write down the Tech Workstation need (see ACTION ITEM 7).
	SAVIERS: Uncomfortable about the $50K boundry. HINDLE: That's an organizational SSG charter type issue. If it's wrong, we'll change it. We can sell multiples profitably.

TOPIC	DISCUSSION
	B.JOHNSON: Your customers are the technology gate keepers. We often learn alot from their feedback. We may not get this via SSG. SAVIERS: and LACROUTE: The Tech Group often sells the seed products that lead to future success.
GSG	WEISS: We aim at being the best supplier of SECURE, DISTRIBUTED, DATA MANAGEMENT systems. We are leaders in communications, interconnect, networking hardware and software. We need to retain leadership in relational database management with the right hardware for large databases and heirarchical storage. Concerns are with communications, networking, multiprocessing.
The LAN issue	We're not going fast enough in delivery of the ETHERNET product. GUTMAN: Can we buy LAN hardware? WEISS: MITERNET is running; we may have to support that before ETHERNET. BYU and LRL have integrated WPS and graphics. We must still pay attention to the technologists (?).
	B.JOHNSON: What about the knowledge BASED Systems - specifically LISP, INTERLISP?
MSG	ALTENHOF: Our presence in the departments is with distributed systems. We must use our networking strength. Hospitals are behind the times. ETHERNET can help solve their problems. CT is a product for the HOSPITAL. We must build systems not pieces. Medical is losing to TANDEM.
COMPETITION	HINDLE: Can we identify the competition? SAVIERS: We're ok with components. Systems are a problem. TROCCI: Australia has been a test bed for Japan.
STABILITY	JOHNSON: Last year we made changes three months after we closed on the engineering budget. Can we live with our decisions? CORBEN: When the PEG managers know the Product Group business models, they can do a better job at trade-off's.
	GUTMAN: On a scale of 1 to 1Ø, how do you feel about your knowledge of the engineering plan? HINDLE: I feel 1Ø now, but it decays rapidly. GUTMAN: I feel a 2 on the P.G. business models.

TOPIC	DISCUSSION
	GENERAL: We need to get together to do this kind of PEG - MKT GROUP exchange.

digital

INTEROFFICE MEMORANDUM

EG:kr4.3

TO: PEG: ENGPPC:

DATE: 3 March 1982
FROM: Eli Glazer
DEPT: CORP. PRODUCT MGMT.
EXT: 3-4434
LOC/MAIL STOP: ML12B-T61

SUBJECT: DRAFT OF PEG/TECH VOL GRP MINUTES 26 FEB 1-5PM

DRAFT PEG/TECH VOL GRP MINUTES FEB 26 1:00-5:00PM

ATTENDEES: Bill Avery, Bill Demmer, Bill Johnson, Jack MacKeen, Don Harbert, John Adams, Bob Flynn, Steve Midel, Lloyd Fugate, Roy Moffa, Hannes Reiter, Herb Shanzer, Cecilia d'Oliveira, Walt Hanstein, Linda Sarles, Ward MacKenzie, Mike Gutman, Graham (for Bruce Osterling), Rick Corben, Eli Glazer

ATTACHMENTS OR REFERENCE DOCUMENTS:

MARKET GROUP SURVEY FM CORBEN (FEB 23)
TVG RESPONSE TO ENGINEERING BASE PLAN FM L. SARLES (FEB 21)
Slide Presentation Set - presented at meeting.

ACTION ITEMS:

WHO/WHEN	WHAT
1) Linda Sarles	Write down what is exactly meant by bus, software cultural etc compatibility in the TVG world.
2) Steve Midel	Market requirement documents from TOEM will be distributed this week.
3) Hannes Reiter	Better definition of need for a two 5 1/4 inch boxes versus a 10 1/2 box with lot of expansion.
4) Herb Shanzer	Review the need for RX based 11/23 PLUS type systems.
5) Linda Sarles	Continue to work on high availability task force (using Nebula's not on CI).

GENERAL DISCUSSION ON THE MEETING FORMAT

Ward opened the meeting with a general discussion of the business model of TVG using slides referenced above. Linda Sarles, Hannes Reiter and Lloyd Fugate followed with a discussion of the three TVG

TOPIC	DISCUSSION

Reiter and Lloyd Fugate followed with a discussion of the three TVG market segments, 32B, 16B and MICROS. There was a spirited dialog during the entire presentation between the presenter, his or her market group colleagues and the PEG managers present. Ward and Linda closed the meeting by reviewing the TVG feedback to the proposed engineering plan. the minutes that follow represent extracts from the discussion during the meeting.

TOPIC	DISCUSSION
Compatibility	ADAMS: How many cutomers use AME mode (VMS utility for RSX-11 compatibility)? SARLES: Don't know, but it gets us in the door. ADAMS: Priviledged code? SARLES: A lot! GUTMAN: What do you mean by compatibility? SARLES: Architecture, busses, instruction set, etc. JOHNSON: What leverage do we have in moving customers from 11's to VAX? Languages, Tools? At what level are the compatibility requirements? MIDEL: Cultural as well (see ACTION ITEMS 1 and 2). SARLES: Customers want to be vendor independent. JOHNSON: Give them two languages and their locked in.
UNIX and C	GUTMAN: What about UNIX and C? SARLES: Customers want to see a full C with UNIX compatibility. They say do it all or its not worth it.
32bit competition and 16bit to 32bit migration	SARLES: PERKIN ELMER leads, then INTEL and MOTOROLA with 32bit chips. Even box and board customers are looking at non-DEC chip alternatives because we do not have low-end 32b alternatives. (The company strategy was to build the high end VAX first which made us vulnerable at the low end 32bit market.)
32bit and 16bit TVG volumes (pg 26-28)	GUTMAN: Let's be sure we don't triple count. The risk is we end up with a low volume ORION U or Q or 32b product. SHANZER: I need input on 5 1/4 inch box versus 10 1/2 box would kill need for a 5 1/4 inch expansion box. GUTMAN: Is there a need for an RA81 ORION? WARD and FUGATE: That's a 3% to 5% need. REITER: 20% of our 11/34's still use RL01's.
MICROS Market Model	FUGATE: INTEL created and encouraged

TOPIC	DISCUSSION
	standardization and second sourcing on their design, to grow rapidly. DEC kept it designs and architecture proprietary. The make or buy decisions are unique to each volume customer and depend on the kind of engineering resources owned by the customer. A wide range. SHANZER: Need to review the need for RX based 16b systems. FUGATE: Yes. GUTMAN: Does MICROPOWER need communications software support? FUGATE: Our customers do their own. MICROPOWER is for dedicated real time run time use. Customers need to optimize their investment in engineering, training, experience and tools. JOHNSON: If we had the MICROVAX development tools in place, we could lock in some DEC 32b "design ins."
**** GENERAL DISCUSSION ... REFER TO LINDA SARLES FEB 21 MEMO ****	
CT	AVERY: Why isn't TVG selling CT's? MACKENZIE: It doesn't fit the TVG market model. It is interesting that one of TVG OEM's, ADEX(?) went to the use of an Apple for an application. MIDEL: Customers might want to develop software added value and ask for drop shipment of the CT. MACKENZIE: CT's will be sold by SSG.
DECnet	ADAMS: Will DECnet become more important to our OEM customers? MACKENZIE: Yes, over time ETHERNET will become more adaptable to OEM networks.
High Availability	SARLES: I am working with COURTIN on high availability including need for shadowing. SAVIERS: BJ and I are each supporting the examinations of the UDA to see if shadowing can be added and supported in the operating systems (see ACTION ITEM 5). MACKENZIE: Remember that CSS and TVG customers are already using multiprocessor - high availability type configurations. (The need has been established in the DEC OEM customer base.) SARLES: A key would be a dual port disk. REITER: There is a proposal for a package developed in Europe, for a high availability software package. The cost is $200K. JOHNSON: Sound like a real bargin if it works.
FPA on Scorpio and ORION (J-11)	MACKENZIE: J-11 and Scorpi are useless in our market without FPA. DEMMER: I

TOPIC	DISCUSSION
	understand we are resource limited in the Semiconductor Engineering area. GUTMAN: I own the J-11 FPA issue. It is not in our A scenario. MACKENZIE: I'll get on my soapbox! If the corporation makes TVG pay for it, we're just sweeping it under the rug one more year. The corporation should view this as a strategic corporate wide decision.
MICROPOWER	GUTMAN: Not in scenario A. FUGATE: It's clearly a tool to keep customers in the DEC family and especially with PDP-11's.

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d i g i t a l
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INTEROFFICE MEMORANDUM

EG:kr4.4

TO: PEG: ENGPPC:

DATE: 4 March 1982
FROM: Eli Glazer
DEPT: CORP. PRODUCT MGMT.
EXT: 3-4434
LOC/MAIL STOP: ML12B-T61

SUBJECT: DRAFT OF PEG/SM SYS GRP MEETING MINUTES 3 MAR 8:30-NOON

DRAFT OF PEG/SM SYS GRP MEETING MINUTES 3 MAR 8:30 - NOON

ATTENDEES: Andy Knowles, Mike Gallup, Joel Schwartz, Rick Corben, Bill Johnson, Bill Demmer, Bill Avery, John O'Keefe, Barry Folsom, Dick Loveland, Mike Gutman, Peter Conklin, Bob Flynn, Bernie Lacroute, John Adams, Don Harbert, Walt Hanstein, Bruce Anderson, Cecilia d'Oliveira, Jerry Hornik, Larry Portner, Bruce Stewart, Eli Glazer.

REFERENCE MATERIAL:

MARKET SURVEY MEMO FM R. CORBEN (23 FEB)

ACTION ITEMS:

WHO/WHEN	TOPIC
1) Mike Gutman	PDP-11 software strategy for each O.S. is being written down. Get a better set of definitions to SSG for evaluation of Market Survey inputs.
2) M. Gallup/Avery(?)	Get Market Survey data on the 16b program issues back to GUTMAN.
3) Bernie Lacroute March 3	The decision is now not to put DECnet Version 4 on RSTS!
4) Bob Flynn	The Storage program has cut YANKEE from it's plan, so as to accelerate MAYA.
5) Bill Johnson	I will look at a development system using C on VMS as a tool for the low-end. To get input from SCHWARTZ on the software requirement for SSG.
6) Bill Avery	Will work with LACROUTE to define the SSG distributed systems needs (SCHWARTZ, FOLSOM will support AVERY).

Spanish. (ALFONSO GAJATE can be a resource.)

Discussion format - Bill Avery put up a slide of the SSG survey input for each program which was then open for general discussion.

TOPIC	DISCUSSION
	********** 16BIT PROGRAM **********
QNA	GUTMAN: Why a 1 vote on QNA? GALLUP: 3720/SNA would be higher. Now it would be 0 for RSTS systems. LACROUTE: Let's not re-do the IAS scene. KNOWLES: Who's selling RSTS? GALLUP: COEM today. GUTMAN: With NEBULA pricing commercial says RSTS will go away. GALLUP: We can't say we will not need to support new devices. PORTNER: Is the issue the sale of new systems? GALLUP: Yes, not add-ons. CONKLIN: Support of existing customers? KNOWLES: Only 5% or less get networked. CONKLIN: If we pull DECnet-E accounts and check them out, we can make a clean decision. LACROUTE: Separate the QNA decision from RSTS-E support with more DECnet. GALLUP: If QNA is for use as a cluster file server, then vote would be 2. GALLUP: Extended memory has no applicability to the OEM environment. KNOWLES: Let's be firm about do we want it or not. GALLUP: If we have to be more precise than 0, 1, or 2, we need a better look (see ACTION ITEMS 1 and 2).
Software	HORNIK: The issue on SORT-11 is the support of new data types. JOHNSON: Rewrite is a very small part of the cost; maintenance is cheaper if we rewrite. GUTMAN: We will get out a better definition of projects -- SSG will get back a better statement of need. GALLUP: No need for ORION Q - we'll get data back to GUTMAN.
DECnet and RSTS	LACROUTE: We are now not putting DECnet phase 4 on RSTS! AVERY: Can we do a PDP-11 software migration strategy to CTAB? GUTMAN: We are writing down the PDP-11 software strategy for each O.S. SHANZER: LCP and ORION may be "TVG only" products.
	********** STORAGE PROGRAM **********
Cartridge Tapes	FLYNN: We're planning to cut YANKEE and put more funding to MAYA (the 5 1/4 inch form

TOPIC	DISCUSSION
	factor cartridge product). KNOWLES: BILL AVERY are we planning to use it? FLYNN: MAYA is needed when you need 40MB and up. GUTMAN: You can't back-up a 'mini' onto floppies. The issue is back-up on a file/document basis or to do it on a volume basis. The MAYA looks like the lowest cost, best approach for volume back-up. Really no other good alternatives. FLYNN: With YANKEE dollars, we move MAYA to Q4FY85. The MAYA technology group says Q1FY85 is possible with more funding. AVERY: What about industry standards? GUTMAN: Fixed and removable Winchesters are expensive and the objective with MAYA is to drive costs down (target $500 or less for MAYA potential with high-end at $900. Also it's a cheap media - also potential for 200Mb capacity). GUTMAN: SHRIMP FRS has high risk. FOLSOM: IRWIN drive in FY84? GUTMAN: They are expensive, MAYA still stands up well. We have a great back-up device today with RL02. Let's sell it. FLYNN: Cost reduction is the target on RX52/53. FOLSOM: Back-up is still the issue. GUTMAN: 1Mb floppy versus 1/2M makes no difference. CTAB has software that will help in the beginning. AVERY: File servers are a solution for the clusters. GUTMAN: The risk of pulling YANKEE is the issue of expensive IBM compatability alternatives. GALLUP: Correct. YANKEE type back-up is key, but it doesn't have to be lowest cost.
	********** SOFTWARE PROGRAM **********
Tools for the low-end	KNOWLES: The compatible PASCAL is important and the 0 vote is wrong. GALLUP: Agreed. SCHWARTZ: The technical user will use Fortran. KNOWLES: C on VAX is an important development tool for the low-end. SCHWARTZ: Why isn't it on list? CORBEN: It's a TIG project. JOHNSON: I'll look at low-end development system of C on VMS and RSX. KNOWLES: The votes do not reflect what SSG needs a development tool. ATARI and APPLE (use VAX and) want quality tools for development. JOHNSON: Who'll get back to me on the software requirement for SSG? KNOWLES: SCHWARTZ.
	********** DISTRIBUTED SYSTEMS **********
IBM support	GALLUP: We filled this out, the survey, from COEM's point of view. SCHWARTZ: We have to

TOPIC	DISCUSSION
	get back to you. GALLUP: COEM did not respond from a CT position. LACROUTE: ? is needed for VT200? We will not do DECnet-E (?). SCHWARTZ: IBM support? LACROUTE: It's not in the plan for CT. KNOWLES: We need it. SCHWARTZ: Outside source? JOHNSON: Do you want to have control? We should do it inside. KNOWLES: Right. Emulaters and IBM Gateways are both critical. SCHWARTZ: Going outside is a time to market issue. ADAMS: For Gateway? LACROUTE: Who do we work with to straighten this out? KNOWLES: BILL AVERY (with FOLSOM, SCHWARTZ, et. al.). ADAMS: PLUTO Gateway software at bottom of DP list. LACROUTE: Broadband is a data only network median and not a systems interconnect (see ACTION ITEM 6).
	********** OFIS PROGRAM **********
Foreign Languages	KNOWLES: Where is foreign being done? SCHWARTZ: Spanish? STEWART: In Europe (Dave Stone). JOHNSON: We're working with Europe and GIA. SCHWARTZ: Spanish will be dominant minority in the USA. KNOWLES & SCHWARTZ: We'll give you a party line (ALFONSO is a candidate for helping) [see ACTION ITEM 5]. KNOWLES: What's in OFIS release 1 (CTAB/OFFICE R1)? STEWART: Complete WPS, good mail, and whatever we can on administrative functions. WPS is like WPS-8 and added functionality, such as use in command and menu mode. STEWART: The other releases are not specified. AVERY: Who does the foreign documentation? STEWART: That's a Dave Stone commitment. JOHNSON: The OFFICE Engineering Program has money in the engineering for documentation. KNOWLES: Be sure you don't depend on the US product group for money for foreign documentation. STEWART/JOHNSON: Understood. We are keeping control of the first few releases for quality.
	********** 32B PROGRAM **********
MICROVAX	DEMMER: Why aren't you interested in high availability? GALLUP: We don't see it today. FOLSOM: Why is MICROVAX low in priority? GALLUP: Not enough visibility to project. SCHWARTZ and FOLSOM: We clearly need MICROVAX in the future. SCHWARTZ:

TOPIC	DISCUSSION
	We'll be in trouble with 68000 if we don't have a MICROVAX. DEMMER: You should expect a FY85 time frame for product use. SCHWARTZ: There will be heat in FY84! DEMMER: It's not a money issue now; it's a resource issue. Goal to announce in a year. KNOWLES: The mythology is a problem with world thinking that 68000 is the future.
********** TERMINALS AND WORKSTATIONS **********	
Low cost RO	KNOWLES: It doesn't make sense to do the low-cost RO build at 1.1M for FY83. AVERY: It's really a cost reduced LA100 with higher functionality compared to the Japanese RO products today. KNOWLES: The interactive I/O on VT200 should be a 2 not a 1.
Intelligent Terminal	JOHNSON Software is complex. Why not do a dumb and a CT versus an intelligent terminal? CAMPBELL: The issue is can we have competitive product in the terminals market-place?
Half vs Full Page	KNOWLES: I wouldn't do Half Page. AVERY: Lot's of Full Page engineering is in the Half Page project. Today, it's a factor of 2:1 in cost $900 vs $2000. We are working to Full Page today as a workstation. FOLSOM: We should do Full Page and put the rest of the money in dumb terminals. KNOWLES: Right. AVERY: I'll work the alternatives. The software is major. The issues are really wide open. JOHNSON: I'm for dumb and CT on intelligent and intermediate. PORTNER: Let's size out the whole thing. Dumb vs CT. KNOWLES: It's a high and low end issue.
********** DISCUSSION OF ITEMS NOT IN SCENARIO A **********	
	SCHWARTZ: Technical customers are key as to why we need FPA. GUTMAN: Commercial people seem not to want J-11 systems any more -- perhaps we'll be able to cut the commercial specifi- cations (CIS) and reinvest in FPA.
	JOHNSON: DECPLOT (comments not understood: editor).
********** 36B - COEXISTANCE **********	
	KNOWLES: All 36b is untouchable. JOHNSON: I own coexistance funding. CORBEN: ~~EE4~~ The LCG's absence in the voting was noted in the survey results that were sent out.

TOPIC	DISCUSSION
	********** GENERAL COMMENTS **********
	There is a dichotomy. KNOWLES: Two types of customers for personal computers. 60% are Fortune 1300 - Systems and newtworks and IBM. They want us to support them totally. 40% are the small business guy who needs only standalone (no communications and only marginal functionality with respect to interconnects and development tools....?). Volume will be 500,000 in a few years, then 60% will be a big part of that. I've visited Aetna, John Deere, Combustion Engineering, etc. LACROUTE: Let me summarize, you have three types of customers: 1)standalone small business; 2) local area DEC networks (will be a technical environment) and 3) IBM network 3270. KNOWLES: Correct.
Portable type CT	CAMPBELL: The opportunity of the portable OSBORNE type product is important... KNOWLES: Let's get the MAY-JUNE announcement thing done. OSBORNE is $1795, ours is $452 (?) cost with Japanese proposal and uses T-11. GUTMAN: Is there a commodity low profit market? CAMPBELL: It's not low functionality. KNOWLES: Portability is really desirable, low cost is not an issue. I think we would do the high quality at not the lowest cost.

Comparision of Funding

Category	May 76 (FY77)	March 82 (FY 82)
Development	55.9	50.4
next year	27.8	
year after	23.2	
>2 years	4.9	
Support	14.5	10.1
Product Management	4.6	2.9
Product total	75	63.4
Advanced Development	11.8	5.9
Research	?	1.4
Tools	6.6	4.7
Standards and architecture	5.1	2.2
A/D, research, tools, stds.	23.5	14.1
Process engineerinng		.7
Manufacturing process		2.2
Finance		1.9
Personnel		1.8
Unallocated/contingency/space		5.3
Central Administration	1.7	
Group Adminstration		13.5 (seperated)

REQUIRED FOR 16.4% OPERATING PROFIT @ $4.6B NOR

- PLANNING UNITS AT STRATEGIC PLAN CONTRIBUTION MARGINS
- MANUFACTURING AT LAST JUNE FY83 BOD % RELATIONSHIP
- CORPORATE ENGINEERING AT FY82 % NOR
- OTHER CORPORATE SERVICE/WW PRODUCT GROUP STRATEGIC EXPENSE AT Q3 RATE
  INFLATION OFFSET BY PRODUCTIVITY IMPROVEMENT

5 APRIL 1982
S. ARONOFF

RISKS IN MEETING 16.4% OPERATING PROFIT GOAL

- HARDWARE STRATEGIC PLAN CONTRIBUTION MARGINS NOT ACHIEVEABLE
  - HALLWAY CONVERSATIONS
  - FY82 PERFORMANCE

- $75M EXPOSURE IN CORPORATE MANUFACTURING CHARGE
  - OVER CAPACITY

- CORPORATE SERVICES/WW PRODUCT GROUP STRATEGIC EXPENSE
  - ATTRITION REQUIRED TO HOLD AT Q3 LEVEL

5 APRIL 1982
S. ARONOFF

FY83 PROFIT MODEL

		TO REACH FY83 GOAL		WITH RISKS
NOR		$4600M		$4600M
US+GIA DIR MARGIN	@ 40.7%	1007	@37.7%	933
EUROPE DIR MARGIN	@ 37.5%	309	@34.5%	285
CUST. SERV PLCM	@ 23.6%	307	SAME	307
TOTAL MARGIN		1623		1525
OTHER COST OF SALES		34	SAME	34
GENEVA EXP		25	SAME	25
CORP MFG + PROJECTS		147	+$75M	222
PG STRATEGIC EXP		168	INFLATION	180
WARRANTY HQ		63	INFLATION	67
CORPORATE ENGINEERING		305	SAME	305
OTHER CORP. SERV.		125	INFLATION	132
OPERATING PROFIT	$	756		560
	%	16.4%		12.2%
NOR		4900		4900
OPERATING PROFIT	$	848		644
	%	17.3%		13.1%

5 APRIL 1982
S. ARONOFF

CONVERTING RISK DOLLARS TO HEADCOUNT REDUCTIONS

SPENDING GOALS	AT 16.4% OP GOAL	RISKS	$ Δ
HDW PG STRATEGIC EXP	$168M	$180M	$12M
CORP MFG CHG + PROJECTS	147	222	75
WARRANTY HQ	63	67	4
CORP SELLING	17	18	1
CORP MKT/ADV (US)	17	18	1
PERSONNEL	13	15	2
F&A (EXCL EUROPE)	63	66	3
OTHER G&A	6	6	-
SPENDING RISKS			$98M
CONTRIBUTION MARGIN RISK			98
TOTAL RISK			$196M

ATTRITION REQUIRED TO MEET PROFIT GOAL

ATTRITION TO OFFSET SPENDING RISKS	*2450 PEOPLE
ATTRITION TO OFFSET CONTRIBUTION MARGIN RISK	*2450
TOTAL	4900 PEOPLE

* 40K PER PERSON INCREMENTAL COSTS

5 APRIL 1982
S. ARONOFF

ENG STAFF

BILL AVERY	ML12-2/E71
GORDON BELL	ML12-1/A51
LARRY BORNSTEIN	PK3-1/C21
DICK CLINTON	ML12-2/A16
RICK CORBEN	ML12-1/T39
BRUCE DELAGI	ML2-2/T88
BILL DEMMER	TW/D19
ULF FAGERQUIST	MR1-2/E78
SAM FULLER	HL2-3/N11
MIKE GUTMAN	ML12-2/E71
JOHN HOLMAN	ML23-2/T36
BILL JOHNSON	ML12-3/A62
BERNIE LACROUTE	TW/A08
LARRY PORTNER	ML10-2/T32
JOE REILLY	ML12-2/A16
JOHN ROSE	ML12-2/T54
GRANT SAVIERS	ML3-6/E94
JACK SMITH	ML1-4/A54
STEVE TEICHER	HL2-2/N07
WILL THOMPSON	QI-1/E21
PETE VAN ROEKENS	ML12-3/A62

FM'S

STEVE BEHRENS	ML12-3/A62
DICK CLINTON	ML12-2/A16
DON CROWTHER	ML3-5/T71
CHUCK FISCHER	HL2-2/N07
BRUCE GREEN	ML12-2/A16
DICK HASLETT	QI-1/E22
KEN JONES	ML23-2/T36
JIM LAWLESS	ML12-2/A16
DAVID MARKEY	ML5-2/T86
RAY MERCIER	HL1-1/S09
LEO MERTA	HL2-3/N11
CAROL REID	TW/D19
DAVE SAWIN	MR1-2/E78
ED SAWYER	ML3-6/E94
MARY ANN SERRA	ML12-2/E71

3/15/82

MAR 31 1982

digital INTEROFFICE MEMORANDUM

TO: Engineering Staff
FM's
Eli Glazer
Jim Wade

DATE: 30 March 82
FROM: Jim Lawless
DEPT: Central Eng. FP&A
EXT: 223-5811
LOC/MAIL STOP: ML12-2/A16

cc: Ron Aronson

SUBJ: ENGINEERING BUDGET UPDATE AS OF MARCH 31, 1982

The enclosed update shows the budget transfers made through March 31, 1982.

Enclosure

/svb

SUMMARY OF CHANGES TO FY82 ENGINEERING PROJECT EXPENSE BUDGET

	BASE 2/26/82	DOUBLE OCCUPANCY ASSISTANCE	ADDITIONAL SEATTLE/ READING RELOCATION	WESTBORO INVENTORY STARTUP	BASE 3/31/82	
GUTMAN-16 BIT	8676	13			8689	16 BIT-GUTMAN
AVERY-TERM & WS	27998				27998	TERM & WS-AVERY
AVERY-CT	-				-	CT-AVERY
DEMMER-32 BIT	23613				23613	32 BIT-DEMMER
LACROUTE-DIST SYS	17047				17047	DIST SYS-LACROUTE
FAGERQUIST-LSG	28008				28008	LSG-FAGERQUIST
SAVIERS-STORAGE	43237			15	43252	STORAGE-SAVIERS
TEICHER-SEG	17382				17382	SEG-TEICHER
JOHNSON-SOFTWARE	47371		464		47835	SOFTWARE-JOHNSON
HOLMAN-TOPS	7292				7292	TOPS-HOLMAN
THOMPSON-PTD	7118				7118	PTD-THOMPSON
FULLER-SA&T	5837				5837	SA&T-FULLER
FULLER-RAD	1518				1518	RAD-FULLER
FULLER-CORP RES	2966				2966	CORP RES-FULLER
PORTNER-CENTRAL	7449		<324>		7125	CENTRAL-PORTNER
REILLY-FINANCE	2319				2319	FINANCE-REILLY
BORNSTEIN-PERSONNEL	1949				1949	PERSONNEL-BORNSTEIN
ROSE-ADMIN	2709				2709	ADMIN-ROSE
ROSE-NEW SITES	500	<13>	<140>	<15>	332	NEW SITES-ROSE
EXT RESOURCES	1334				1334	EXT RESOURCES
WADE-EURO ENG	1300				1300	EURO ENG-WADE
PORTNER-CONTINGENCY	<1100>				<1100>	CONTINGENCY-PORTNER
GENERAL TECH	-				-	GENERAL TECH
TOTAL	254523	-	-	-	254523	

3/30/82--RL06/5.8

SUMMARY OF CHANGES TO FY83 ENGINEERING PROJECT EXPENSE BUDGET

	BASE 2/26/82	JAPAN TECHNOLOGY TRANSFER	BASE 3/31/82	
GUTMAN-16 BIT	12343		12343	16 BIT-GUTMAN
AVERY-TERM	34117		34117	TERM-AVERY
AVERY-CT	400		400	CT-AVERY
DEMMER-32 BIT	37910		37910	32 BIT-DEMMER
LACROUTE-DIST SYS	21019		21019	DIST SYS-LACROUTE
FAGERQUIST-LSG	33718		33718	LSG-FAGERQUIST
SAVIERS-STORAGE	56768	139	56907	STORAGE-SAVIERS
TEICHER-SEG	16437		16437	SEG-TEICHER
JOHNSON-SOFTWARE	63868		63868	SOFTWARE-JOHNSON
HOLMAN-TOPS	8480		8480	TOPS-HOLMAN
THOMPSON-PTD	7641		7641	PTD-THOMPSON
FULLER-SA&T	7014		7014	SA&T-FULLER
FULLER-RAD	1969		1969	RAD-FULLER
FULLER-CORP RES	3800		3800	CORP RES-FULLER
PORTNER-CENTRAL	9397		9397	CENTRAL-PORTNER
REILLY-FINANCE	2667		2667	FINANCE-REILLY
BORNSTEIN-PERSONNEL	2275		2275	PERSONNEL-BORNSTEIN
ROSE-ADMIN	2760		2902	ADMIN-ROSE
ROSE-NEW SITES	13426		13284	NEW SITES-ROSE
EXT RESOURCES	1540	<139>	1401	EXT RESOURCES
WADE-EURO ENG	1520		1520	EURO ENG-WADE
PORTNER-CONTINGENCY	2188		2188	CONTINGENCY-PORTNER
GENERAL TECH	5347		5347	GENERAL TECH
TOTAL	346604	-	346604	

3/30/82--RL06/5.9

SUMMARY OF CHANGES TO FY84 ENGINEERING PROJECT EXPENSE BUDGET

	BASE 2/26/82	JAPAN TECHNOLOGY TRANSFER	BASE 3/31/82	
GUTMAN-16 BIT	8992		8992	16 BIT-GUTMAN
AVERY-TERM	40828		40828	TERM-AVERY
AVERY-CT	-		-	CT-AVERY
DEMMER-32 BIT	36841		36841	32 BIT-DEMMER
LACROUTE-DIST SYS	23635		23635	DIST SYS-LACROUTE
FAGERQUIST-LSG	34749		34749	LSG-FAGERQUIST
SAVIERS-STORAGE	69213	164	69377	STORAGE-SAVIERS
TEICHER-SEG	17781		17781	SEG-TEICHER
JOHNSON-SOFTWARE	76662		76662	SOFTWARE-JOHNSON
HOLMAN-TOPS	7821		7821	TOPS-HOLMAN
THOMPSON-PTD	8084		8084	PTD-THOMPSON
FULLER-SA&T	8037		8037	SA&T-FULLER
FULLER-RAD	2373		2373	RAD-FULLER
FULLER-CORP RES	4294		4294	CORP RES-FULLER
PORTNER-CENTRAL	10674		10674	CENTRAL-PORTNER
REILLY-FINANCE	3024		3024	FINANCE-REILLY
BORNSTEIN-PERSONNEL	2572		2572	PERSONNEL-BORNSTEIN
ROSE-ADMIN	3138		3138	ADMIN-ROSE
ROSE-NEW SITES	18050		18050	NEW SITES-ROSE
EXT RESOURCES	1779	<164>	1615	EXT RESOURCES
WADE-EURO ENG	1780		1780	EURO ENG-WADE
PORTNER-UNALLOC	28374		28374	UNALLOC-PORTNER
PORTNER-CONTINGENCY	25000		25000	CONTINGENCY-PORTNER
GENERAL TECH	12000		12000	GENERAL TECH
TOTAL	445701	-	445701	

3/30/82--RL06/5.10

TO: ENG STAFF [illegible]

DATE: [illegible]
FROM: [illegible]
DEPT: [illegible]
EXT: [illegible]
LOC/MAIL STOP: [illegible]

SUBJECT: CLOSING THE ENGINEERING BUDGET

The Productivity and Market Group reviews did not produce any simple solutions to our Engineering budget problem. In the current business climate we cannot afford to back away from any of our product delivery commitments and the Corporation cannot afford a $390M Engineering budget. Simply stated, we have to get out the products on schedule for less cost. [illegible]

[illegible]

[illegible]

[illegible]

1. Request additional budget [illegible] product [illegible] direct engineers [illegible] the product commitments. [illegible] explained in Appendix [illegible] reviewed [illegible]

2. [illegible]

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* d i g i t a l *
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TO: *GORDON BELL
JACK SMITH
cc: CAROL GAULT
DOTTIE HOUCK

DATE: THU 22 APR 1982 12:52 PM EST
FROM: JOSEPH REILLY
DEPT: CE FINANCE
EXT: 223-6883
LOC/MAIL STOP: ML12-2/A16

SUBJECT: RUN RATE

Our current run rate using Q3 Annualized puts us at a level of $311MEG (See Attached). I suspect our Q4 run rate would put us at a level of $320MEG.

ADDITIONAL RISKS:

- o ECO risk in Terminals & Workstations.
- o ULF cannot do his "A Scenario" for his March budget.
- o No contingency in our Run Rate numbers.
- o 32-Bit needs more people to deliver its "A Scenario".
- o Japan, Carnegie West Coast not in run rate.

SUMMARY:

With good management and luck we may be able to deliver our "A Scenario" for $346.6. However, the Low End wants to add and accelerate projects.

If we are to cut out $30MEG more, we should immediately freeze all internal and external hiring with the exception of college hires, cut projects and delay some of our facility projects.

ENGINEERING SPENDING GROWTH

Q	CC SPEND'G. $	% DELTA	PROJECT	% DELTA	HEADCOUNT	% DELTA
Q1	$ 57.9		$ 54.9		$ 4662	
Q2	61.7	6.5	58.6	6.7	4925	5.6
Q3	69.7	12.9	66.3	13.1	5162	4.8
Q4 Est.	75.8	8.7	72.0	8.6	5362	3.8

	ANNUALIZED Q3	FY83 INFLATION	FY83 RUN RATE
PAYROLL	$ 138.0	$ 15.2	$ 153.2
FRINGE	30.0	.5	30.5
OCCUPANCY	21.2	2.1	23.3
DEPRECIATION	18.4	2.5	20.9
PROJECT MATERIAL	18.4	2.5	20.9
OPERATING SUPPLIES	9.6	1.0	10.6

TRAVEL & MEETINGS	6.8	.7	7.5
RELOCATION/HIRING	3.2	.3	3.5
OTHER	33.2	3.3	36.5
TOTAL	$ 278.8	$ 28.1	$ 306.9

ADD

266 College Hires at $40K Salary/Fringe	$ 10.6
John Rose Facilities	10.0
GROSS COST CENTER SPENDING	$ 327.5
Redbook Project Spending 95% CC Spending	$ 311.0

CENTRAL ENGINEERING
PROJECT RUN RATE
FY83

GROUP	TOTAL YEAR PROJECTS	Q4 @ 93%	Q4 ANNUALIZED RUN RATE	CURRENT PLAN	SCENARIO "A"
PSD	8.7	3.0	12.0	12.3	14.4
CT/TERM	30.9	8.8	35.2	34.5	34.5
32-BIT	23.6	6.2	24.8	37.9	44.4
D/S	16.9	4.5	18.0	21.0	21.0
LSG	28.0	7.6	30.4	33.7	33.7
STORAGE	43.2	12.3	49.2	56.9	56.8
SEG	17.0	4.2	16.8	16.4	20.9
SOFTWARE	47.8	12.8	51.2	63.9	67.3
SA&T	10.1	2.8	11.2	12.8	12.8
TOPS	6.7	1.7	6.8	8.5	8.5
PTD	7.2	1.9	7.6	7.6	9.2
SUB TOTAL	240.1	65.8	263.2	305.5	323.5
CENTRAL	12.9	3.4	13.6	17.2	17.1
EUROPE ENG	1.3	.4	1.6	1.5	1.5
EXT. RESOURCES	1.3	.5	2.0	1.4	1.4
SITES	.3	.3	1.2	13.3	13.4
GEN TECH				5.3	5.4

CONTINGENCY	1.1	1.6	6.4	2.2	<15.7>
TOTAL	257.0	72.0	288.0	346.6	346.6

RL0.4.26
EMML MESSAGE ID: 5161173561

APR 1? 1982

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INTEROFFICE MEMORANDUM

TO: Gordon Bell
Joe Reilly
Jack Smith

DATE: March 15, 1982
FROM: Oleh Kostetsky
DEPT: Operations Analysis
EXT: 223-3704
LOC: ML12-3/A62

cc: Larry Portner
Bill Thompson

SUBJECT: CENTRAL ENGINEERING INFLATIONARY TRENDS--ANALYSIS, PROJECTION, IMPLICATIONS AND SUGGESTED ACTION ITEMS.

For several years, much of the Western World has been caught up in a strong inflationary spiral. In this environment, critical resources were often scarce. Scarcity of this type often presented us with the choice of paying more now or waiting and possibly losing market share. In a growth oriented environment coupled with exterior inflation and scarcity it was reasonable to expect that relative emphasis would shift away from cost control toward getting the people, space, material, equipment needed in order to compete. The following study shows that our adaptation to this reality has engendered a steep increase in the cost per person in Central Engineering over the last 4 years.

During the last 6 months the world has begun to move toward a situation where inflation is coming down and most of the formerly scarce resources are available in abundance. Much effort on the part of governments and industries is being directed toward the reduction in the rates of inflation. For the first time in history, major unions have agreed to renegotiate labor costs downward. Hopefully, we are able to adapt to this new state of affairs before we are faced with the reduction in competitiveness so evident in the auto industry.

The purpose of the following analysis is not to criticize the results of the past but to motivate us to more quickly adapt to the new realities confronting us.

OVERALL IMPLICATIONS AND CONCLUSIONS

Cost per person has been increasing at a steep rate over the FY'78-FY'82 time frame (average compounded growth rate of 17.8-19.5% per year). If this trend continues, we will need an increase in budget from a FY'82 total of $237-270 million to $485-579 million in FY'86 just to retain our current personnel. To continue to add people at the FY'78-FY'82 growth rate, would require a $780-998 million budget for FY'86. If external inflation abates and the dollar continues strong on world markets and we do not take immediate action to stem the internal per person inflationary trends, we may find ourselves in an uncompetitive position.

DETAILED IMPLICATIONS

1. The average salary for a person employed by Engineering has been increasing at an average yearly compounded growth rate of 11.2-12.9% during the FY'78-FY'82 time frame.

2. The per person cost of Fringe Benefits has been increasing at an average yearly compounded rate of 14.6-16.3% during the FY'78-FY'82 time frame. In fact the per person growth rate here seems to be accelerating.

3. The per person cost of Occupancy, Depreciation, Leasing has been increasing at an average yearly compounded rate of 26.5-28.4% during the FY'78-FY'82 time frame. In fact the per person growth rate here seems to be accelerating.

4. "Other" expenses (telephone and other cross-charges from outside groups such as Field Service and Manufacturing) has had the largest growth rate (average compounded growth rate of 47.2-49.5% per year during the FY'78-FY'82 time frame). However, there is some evidence of deceleration in the growth rate in the latter part of this period.

5. The % of people defined to be direct (Engineering Supervisors, Technicians, Writers and Engineers) has been a steady 51-53% over the FY'78-FY'82 time frame. The % of labor $'s charged to DIRECT seems to also be level over most of this time frame. There does not seem to be a significant increase in % of $'s spent on overhead activities.

DETAILED CONCLUSIONS

If this trend were to continue:

(a) Cost per person would rise from $47.1-49.9K in FY'82 to $96.3-106.8K in FY'86.

(b) The average salary of a person working in Central Engineering would rise from $22.9-24.3K in FY'82 to $35.0-39.5K in FY'86.

(c) The average salary plus fringe of a person working in Central Engineering would rise from $27.9-29.6K in FY'82 to $43.6-49.5K in FY'86.

(d) Even a compounded growth rate in budget of 30% per year, which would increase the FY'82 budget of $237-270 million to $677-772 million in FY'86, would allow for only a modest people growth rate of 7.4-8.7% for the FY'82-FY'86 time frame. This is substantially less than the 12.6-14.6% growth rate in people experienced in the FY'78-FY'82 time frame. Continued people growth rates at the 12.6-14.6% levels would require a FY'86 budget of $780-998 million.

(e) If the Central Engineering budget growth is reduced from historic growth levels and current cost per man inflation were to continue, it would be difficult to meet our product goals without heroic improvements in productivity.

POSSIBLE CORRECTIVE ACTION ITEMS

We must find ways to reduce the rates of increase. Possible first steps:

(a) Significantly reduce the average % in salary increases allowed during the upcoming salary planning exercise.

(b) Increase the deductible on the John Hancock major medical policy from $50 (to $250 or so). The $50 of 10 years ago is not the $50 of today.

(c) Charter an in-depth analysis of what has been going on with "Other" expenses. This is a very confusing area with millions of offsetting expenses flowing through a myriad of accounts and categorized in a confusing manner on our financial reports.

(d) Set up a committee to develop proposals to reduce Occupancy cost increases.

(e) Set up a committee to develop proposals to reduce the Supplies, Materials, Tools cost increases.

(f) Put a freeze on Fringe "improvements" for the duration.

(g) Create a supplemental stock option plan specifically directed at difficult-to-find and difficult-to-keep classes of employee. This can make it easier to keep key people without undue escalation of overall salary expenses.

POSSIBLE IMPLICATIONS OF CORRECTIVE ACTION ITEMS

If these (or other) corrective steps result in the following reduction in the rates of internal inflationary growth:

(a) Reduction in Average Salary growth from an expected 11.2-12.9% to 8% per year.

(b) Reduction in Fringe Cost Per Person growth from an expected 14.6-16.3% to 8% per year.

(c) Reduction in Relocation and Hiring Cost Per Person growth from an expected 31.6% to 14% per year.

(d) Reduction in Supplies, Materials, Tools Cost Per Person growth from an expected 21.1-22.5% to 20% per year.

(e) Reduction in Occupancy, Depreciation, Leases Cost Per Person growth from an expected 26.5-28.4% to 24% per year.

(f) Reduction in Travel and Meetings Cost Per Person growth from an expected 31.6-33.8% to 20% per year.

(g) Reduction in "Other" Cost Per Person growth from an expected 34.4% to 20% per year.

then:

(a) The Total Cost Per Person growth rate would be reduced from an expected 19.6-21.0% to 13.9% per year.

(b) The Total Cost Per Person in FY'86 would be reduced from an expected $96.3-106.8K to $79.2-84.0K.

(c) The budget required to maintain the current level of personnel would fall from an expected $485-579 million to $399-455 million in FY'86.

(d) The budget required to maintain the current people growth rates of 12.6-14.6% would fall from an expected $780-998 million to $641-785 million in FY'86.

SUMMARY

Without the management of factors affecting the rates of increase in cost, future cost per person numbers could force us into an uncompetitive position. Once the rates assert themselves, our options for controlling the resultant cost levels are limited. If rates of change are not managed, the cost control burden becomes one of limiting people growth and striving for productivity improvements. However, productivity improvements of heroic proportions would be required to keep pace with inflationary rates of this magnitude. The projections inherent in this analysis show that it would take a doubling in productivity every four years just to keep pace with historic internal inflation rates. When cost per person numbers escalate at these very high rates, we find that all groups tend to complain of a shortage of people and find it difficult to invest in technology designed to improve tomorrow's productivity. Thus, without the management of the rates of cost increase we will find ourselves without the means to do the job or the means to raise productivity to do the job.

On the other hand, if we could find ways to reduce the average internal inflation rate down to a more manageable 14% per or so, the Total Cost Per Person for FY'86 would be reduced from an expected 100K to a 80K range and current budget projections could support historical people growth rates.

This analysis indicates that we must establish a strong management focus to reduce and continuously control these rates of change.

METHOD

1. Calculated cost per person for various categories of cost for FY'1978, FY'1980-81.

2. Estimated cost per person for various categories of cost for FY'82 using actuals for the first 8 months of this fiscal year and latest budget numbers for the balance of the year.

3. Calculated the average compounded rate of growth from FY'78 to FY'82 for each category of cost. Use these growth rates to make initial projections of FY'82-FY'86 growth rates.

4. Calculated the rates of the rates of change for various time frames and modified the rate of change projections derived in 3. above in order to take significant evidence of acceleration of deceleration into account.

5. Projected the average cost per person for FY'86 by applying the growth rates calculated in 3. and 4. above against their respective category of cost and adding up the results obtained for each category. Did this for two sets of assumption as to what FY'82 expenses and headcount will end up at.

6. Calculated budget requirements using cost per person projections obtained in 5. above assuming (a) no headcount growth (b) headcount will grow at historic rates.

7. Did a similar analysis and projection of Central Software Engineering data as a check. The results were remarkably similar.

I. ASSUMPTION SET I.

CENTRAL ENGINEERING - EXPENSES ($millions)

DESCRIPTION	FY'78	FY'79	FY'80	FY'81	EST. FY'82	COMPOUND GROWTH RATE FY'78-FY'82	PROJECTED FY'86 IF FY'82-FY'86 PEOPLE GROWTH RATE CONT. AT FY'78-82 LEVEL: PROJECTED FY'86	PROJECTED COMPOUND GROWTH RATE FY'82-FY'86
DIRECT LABOR + LABOR PORTION OF CONTRACT PEOPLE(EST.)	29.1		43.4	57.8	74.6	26.5%	209.3	29.4%
INDIRECT LABOR + OT PREMIUM	17.9		33.3	43.9	57.1	33.6%	159.8	29.3%
FRINGE + FRINGE PORTION OF CONTRACT PEOPLE(EST.)	9.0		14.0	20.2	28.6	33.5%	90.6	33.4%
RELOCATION AND HIRING	0.8		2.1	2.0	5.0	58.1%	25.2	49.8%
SUPPLIES, MATERIALS, TOOLS	6.2		13.2	13.2	24.5	41.0%	94.4	40.1%
OCCUPANCY, DEPRECIATION, LEASES	7.7		15.4	23.2	36.9	48.0%	172.8	47.1%
TRAVEL AND MEETINGS	1.6		4.1	5.8	8.4	51.4%	47.6	54.3%
OTHER	4.6		11.7	27.6	35.1	66.2%	198.1	54.1%
TOTAL	76.9		137.3	193.7	270.2	36.9%	997.8	38.6%

CENTRAL ENGINEERING - PEOPLE

NUMBER OF DIRECT DEC PEOPLE	1486	1768	2141	2316	2658	15.7%		
ESTIMATED NUMBER OF CONTRACT PEOPLE	293		106	142	215	-7.5%		
DIRECT PEOPLE	1779		2247	2458	2873	12.7%	4955	14.6%
INDIRECT PEOPLE	1359	1594	1999	2216	2544	17.0%	4388	14.6%
TOTAL PEOPLE	3138		4246	4674	5417	14.6%	9343	14.6%
% DEC DIRECT TO TOTAL DEC	52.2%	52.2%	51.7%	51.1%	51.1%		51.0%	
% DIRECT (INCLUDING CONTRACT) TO TOTAL	56.7%		52.9%	52.6%	53.0%		53.0%	
% LABOR $ CHARGED TO DIRECT	61.9%		56.6%	56.8%	56.6%		56.7%	

450

I. ASSUMPTION SET I. (continued)

CENTRAL ENGINEERING - COST PER PERSON ($1000)

DESCRIPTION	FY'78	FY'79	FY'80	FY'81	EST. FY'82	COMPOUND GROWTH RATE FY'78-FY'82	PROJECTED FY'86	PROJECTED COMPOUND GROWTH RATE FY'82-FY'86
SALARY	15.0		18.1	21.8	24.3	12.9%	39.5	12.9%
FRINGE	2.9		3.3	4.3	5.3	16.3%	9.7	16.3%
RELOCATION AND HIRING	0.3		0.5	0.4	0.9	31.6%	2.7	31.6%
SUPPLIES, MATERIALS, TOOLS	2.0		3.1	2.8	4.5	22.5%	10.1	22.5%
OCCUPANCY, DEPRECIATION, LEASES	2.5		3.6	5.0	6.8	28.4%	18.5	28.4%
TRAVEL AND MEETINGS	0.5		1.0	1.2	1.6	33.8%	5.1	33.8%
OTHER	1.3		2.8	5.9	6.5	49.5%	21.2	34.4%
TOTAL	24.5		32.3	41.4	49.9	19.5%	106.8	21.0%

CENTRAL ENGINEERING - PER CENT OF TOTAL

DIRECT LABOR + LABOR PORTION OF CONTRACT PEOPLE(EST.)	37.9		31.6	29.8	27.6	-7.6	21.0	-6.6
INDIRECT LABOR + OT PREMIUM	23.3		24.3	22.7	21.1	-2.4	16.0	-6.7
FRINGE + FRING PORTION OF CONTRACT PEOPLE (EST.)	11.6		10.2	10.4	10.6	-2.2	9.1	-3.7
RELOCATION AND HIRING	1.1		1.5	1.0	1.9	14.6	2.5	7.1
SUPPLIES, MATERIALS, TOOLS	8.1		9.6	6.8	9.1	3.0	9.5	1.1
OCCUPANCY, DEPRECIATION, LEASES	10.1		11.3	12.0	13.7	7.9	17.3	6.0
TRAVEL AND MEETINGS	2.1		3.0	3.0	3.1	10.2	4.8	11.6
OTHER	5.8		8.5	14.3	13.0	22.4	19.9	11.2
TOTAL	100.0		100.0	100.0	100.0	100.0	100.0	100.0

Maintenance of FY'82 headcount would require a FY'86 budget of $578.5 million (5417 people x $106.8K).

Maintenance of historic people growth rate of 14.6% would require a FY'86 budget of $997.8 million (9343 people x $106.8K).

An annual budget growth of 30% would provide for a FY'86 budget of $771.7 million which would allow for a FY'86 headcount of 7226 ($771.7 million divided by $106.8K per person), which would amount to a 7.4% compounded people growth rate.

I. ASSUMPTION SET I. (continued)

CENTRAL ENGINEERING - PER PERSON AVERAGE YEARLY GROWTH RATES

	FY'78-FY'80	FY'80-FY'82	FY'81-FY'82	FY'78-FY'82
LABOR	9.8%	15.9%	11.5%	12.8%
FRINGE	6.7%	27.6%	23.3%	16.3%
RELOCATION AND HIRING	29.1%	34.2%	125.0%	31.6%
SUPPLIES, MATERIALS, TOOLS	24.5%	20.5%	60.7%	22.5%
OCCUPANCY, DEPRECIATION, LEASES	20.0%	37.4%	36.0%	28.4%
TRAVEL AND MEETINGS	41.4%	26.5%	33.3%	33.8%
OTHER	46.8%	52.4%	10.2%	49.5%
TOTAL	14.8%	24.3%	20.5%	19.5%

II. ASSUMPTION SET II. (conservative)

CENTRAL ENGINEERING - EXPENSES ($millions)

DESCRIPTION	FY'78	FY'79	FY'80	FY'81	EST. FY'82	COMPOUND GROWTH RATE FY'78-FY'82	PROJECTED FY'86 IF FY'82-FY'86 PEOPLE GROWTH RATE CONT. AT FY'78-82 LEVEL: PROJECTED FY'86	PROJECTED COMPOUND GROWTH RATE FY'82-FY'86
LABOR	47.0		74.3	93.4	115.5	25.2%	283.3	25.1%
FRINGE	9.0		13.6	18.6	25.1	29.2%	69.6	29.0%
RELOCATION AND HIRING	0.8		2.0	1.8	4.4	53.1%	21.9	49.4%
SUPPLIES, MATERIALS, TOOLS	6.2		12.8	12.1	21.5	36.5%	74.5	36.4%
OCCUPANCY, DEPRECIATION, LEASES	7.7		14.9	21.3	32.4	43.2%	132.8	42.3%
TRAVEL AND MEETINGS	1.6		4.0	5.3	7.4	46.6%	36.4	48.9%
OTHER	4.6		11.3	25.4	30.8	60.9%	161.1	51.2%
TOTAL	76.9		133.0	178.0	237.0	32.5%	779.6	34.7%
TOTAL PEOPLE	3138		4246	4674	5036	12.6%	8095	12.6%

CENTRAL ENGINEERING - COST PER PERSON ($1000)

DESCRIPTION	FY'78	FY'79	FY'80	FY'81	EST. FY'82	COMPOUND GROWTH RATE FY'78-FY'82	PROJECTED FY'86	PROJECTED COMPOUND GROWTH RATE FY'82-FY'86
LABOR	15.0		17.5	20.0	22.9	11.2%	35.0	11.2%
FRINGE	2.9		3.2	4.0	5.0	14.6%	8.6	14.6%
RELOCATION AND HIRING	0.3		0.5	0.4	0.9	31.6%	2.7	31.6%
SUPPLIES, MATERIALS, TOOLS	2.0		3.0	2.6	4.3	21.1%	9.2	21.1%
OCCUPANCY, DEPRECIATION, LEASES	2.5		3.5	4.6	6.4	26.5%	16.4	26.5%
TRAVEL AND MEETINGS	0.5		0.9	1.1	1.5	31.6%	4.5	31.6%
OTHER	1.3		2.7	5.4	6.1	47.2%	19.9	34.4%
TOTAL	24.5		31.3	38.1	47.1	17.8%	96.3	19.6%

Maintenance of FY'82 headcount would require a FY'86 budget of $485.0 million (5036 x $96.3K).

Maintenance of historic people growth rate of 12.6% would require a FY'86 budget of $779.6 million (8095 x $96.3K).

An annual budget growth of 30% would provide for a FY'86 budget of $676.9 million which would allow for a FY'86 headcount of 7029 which amounts to a 8.7% compounded people growth rate.

II. ASSUMPTION SET II. (continued)

CENTRAL ENGINEERING - PER PERSON AVERAGE YEARLY GROWTH RATES

	FY'78-FY'80	FY'80-FY'82	FY'81-FY'82	FY'78-FY'82
LABOR	8.0%	14.3%	14.5%	11.2%
FRINGE	5.0%	25.0%	25.0%	14.6%
RELOCATION AND HIRING	29.1%	34.2%	125.0%	31.6%
SUPPLIES, MATERIALS, TOOLS	22.5%	19.7%	65.4%	21.1%
OCCUPANCY, DEPRECIATION, LEASES	18.3%	35.2%	39.1%	26.5%
TRAVEL AND MEETINGS	34.2%	29.1%	22.2%	31.6%
OTHER	44.1%	50.3%	13.0%	47.2%
TOTAL	13.0%	22.7%	23.6%	17.8%

III. TAKE ACTION TO REDUCE INFLATIONARY GROWTH (applied against ASSUMPTION SET I.)

TAKE ACTION TO REDUCE COST PER PERSON RATES AS FOLLOWS:

LABOR Cost growth rate reduced to 8.0% per year
FRINGE Cost growth rate reduced to 8.0% per year
RELOCATION AND HIRING Cost growth rate reduced to 14.0% per year
SUPPLIES,MATERIALS,TOOLS Cost growth rate reduced to 20.0% per year
OCCUPANCY,DEPRECIATION,LEASES Cost growth rate reduced to 24.0% per year
TRAVEL AND MEETINGS Cost growth rate reduced to 20.0% per year
OTHER Cost growth rate reduced to 20.0% per year

PROJECTED RESULT:

CENTRAL ENGINEERING - TOTAL EXPENSES ($millions)

DESCRIPTION	FY'78	FY'82	COMPOUND GROWTH RATE FY'78-FY'82	PROJECTED FY'86 IF FY'82-FY'86 PEOPLE GROWTH RATE REMAINS AT FY'78-FY'82 LEVEL: PROJECTED FY'86	PROJECTED COMPOUND GROWTH RATE FY'82-FY'86	PROJECTED FY'86 IF FY'82-FY'86 PEOPLE GROWTH RATE HELD TO 0%: PROJECTED FY'86	PROJECTED COMPOUND GROWTH RATE FY'82-FY'86
LABOR	47.0	131.7	29.4%	309.3	23.8%	179.3	8.0%
FRINGE	9.0	28.6	57.2%	67.3	23.9%	39.0	8.0%
RELOCATION AND HIRING	0.8	5.0	40.9%	14.0	29.4%	8.4	14.0%
SUPPLIES,MATERIALS,TOOLS	6.2	24.5	47.8%	86.9	37.2%	50.4	20.0%
OCCUPANCY,DEPRECIATION,LEASES	7.7	36.9	55.3%	150.4	42.1%	87.2	24.0%
TRAVEL AND MEETINGS	1.6	8.4	50.8%	30.8	38.4%	17.9	20.0%
OTHER	4.6	35.1	66.2%	126.1	37.7%	73.1	20.0%
TOTAL	76.9	270.2	36.9%	784.8	30.5%	455.3	13.9%

CENTRAL ENGINEERING - HEADCOUNT

TOTAL PEOPLE	3138	5417	14.6%	9343	14.6%	5417	0.0%

CENTRAL ENGINEERING - PER PERSON EXPENSES ($1000)

DESCRIPTION	FY'78	FY'82	COMPOUND GROWTH RATE FY'78-FY'82	MANAGED PROJECTION FY'86	MANAGED COMPOUND GROWTH RATE FY'82-FY'86
LABOR	15.0	24.3	12.9%	33.1	8.0%
FRINGE	2.9	5.3	16.3%	7.2	8.0%
RELOCATION AND HIRING	0.3	0.9	31.6%	1.5	14.0%
SUPPLIES,MATERIALS,TOOLS	2.0	4.5	22.5%	9.3	20.0%
OCCUPANCY,DEPRECIATION,LEASES	2.5	6.8	28.4%	16.1	24.0%
TRAVEL AND MEETINGS	0.5	1.6	33.8%	3.3	20.0%
OTHER	1.3	6.5	49.5%	13.5	20.0%
TOTAL	24.5	49.9	19.5%	84.0	13.9%

IV. TAKE ACTION TO REDUCE INFLATIONARY GROWTH (applied against ASSUMPTION SET II.)

TAKE ACTION TO REDUCE COST PER PERSON RATES AS FOLLOWS:

LABOR Cost growth rate reduced to 8.0% per year
FRINGE Cost growth rate reduced to 8.0% per year
RELOCATION AND HIRING Cost growth rate reduced to 14.0% per year
SUPPLIES,MATERIALS,TOOLS Cost growth rate reduced to 20.0% per year
OCCUPANCY,DEPRECIATION,LEASES Cost growth rate reduced to 24.0% per year
TRAVEL AND MEETINGS Cost growth rate reduced to 20.0% per year
OTHER Cost growth rate reduced to 20.0% per year

PROJECTED RESULT:

CENTRAL ENGINEERING - TOTAL EXPENSES ($millions)

				PROJECTED FY'86 IF FY'82-FY'86 PEOPLE GROWTH RATE REMAINS AT FY'78-FY'82 LEVEL		PROJECTED FY'86 IF FY'82-FY'86 PEOPLE GROWTH RATE HELD TO 0%	
	FY'78	FY'82	COMPOUND GROWTH RATE FY'78-FY'82	PROJECTED FY'86	PROJECTED COMPOUND GROWTH RATE FY'82-FY'86	PROJECTED FY'86	PROJECTED COMPOUND GROWTH RATE FY'82-F6'86
LABOR	47.0	115.5	25.2%	252.6	21.6%	157.1	8.0%
FRINGE	9.0	25.1	29.2%	55.0	21.7%	34.1	8.0%
RELOCATION AND HIRING	0.8	4.4	53.1%	12.1	28.8%	7.4	14.0%
SUPPLIES,MATERIALS,TOOLS	6.2	21.5	36.5%	72.0	35.3%	44.6	20.0%
OCCUPANCY,DEPRECIATION,LEASES	7.7	32.4	43.2%	122.0	39.4%	76.6	24.0%
TRAVEL AND MEETINGS	1.6	7.4	46.6%	25.1	35.7%	15.3	20.0%
OTHER	4.6	30.8	60.9%	102.0	34.9%	63.9	20.0%
TOTAL	76.9	237.0	32.5%	641.1	28.2%	399.0	13.9%

CENTRAL ENGINEERING - HEADCOUNT

TOTAL PEOPLE	3138	5036	12.6%	8095	12.6%	5036	0.0%

CENTRAL ENGINEERING - PER PERSON EXPENSES ($1000)

	FY'78	FY'82	COMPOUND GROWTH RATE FY'78-FY'82	MANAGED PROJECTION FY'86	MANAGED COMPOUND GROWTH RATE FY'82-FY'86
LABOR	15.0	22.9	11.2%	31.2	8.0%
FRINGE	2.9	5.0	14.6%	6.8	8.0%
RELOCATION AND HIRING	0.3	0.9	31.6%	1.5	14.0%
SUPPLIES,MATERIALS,TOOLS	2.0	4.3	21.1%	8.9	20.0%
OCCUPANCY,DEPRECIATION,LEASES	2.5	6.4	26.5%	15.1	24.0%
TRAVEL AND MEETINGS	0.5	1.5	31.6%	3.1	20.0%
OTHER	1.3	6.1	47.2%	12.6	20.0%
TOTAL	24.5	47.1	17.8%	79.2	13.9%

****
* digital *
****

TO: see "TO" DISTRIBUTION

cc: PEG:

DATE: WED 10 FEB 1982 3:35 PM EST
FROM: RICK CORBEN
DEPT: CORP PRODUCT MGMT
EXT: 223-3123
LOC/MAIL STOP: ML12-1/-T39

SUBJECT: ENGINEERING PROJECT LISTS - PART I

********** PART I OF II **********

The following is the first draft of the Engineering project list. It is for use by the Market Groups in surveying their P/Gs on the business importance of each item. Engineering Groups should review the list and submit any corrections by Thursday at 5:00PM so that I can have a final version for our Market Group/Program Office meeting on Friday afternoon (3PM, ML2-2, RAD Conference Room).

The philosophy in assembling the list was to identify Engineering-funded projects with product deliverables. In general, pure maintenance spending ECOs, FCC, and other legal or contractual committments were excluded. Similarly, Engineering advance development, tool/process development, research, and other non-product items were left out. The dollar figures shown for FY'83 are intended to give a gross feeling of project scale. The rules for allocating dollars to individual Engineering projects are not consistent across the groups so precise comparisions should be avoided.

/jdm
RC1.S6.46

	FRS	FY'83 K$
16-BIT PROGRAM		
ORION U, Q	Q4FY84	4300
LCP-5	Q4/Q2FY83	2800
LCP-8	H1FY84	500
QNA	Q4FY83	500
RSTS SUBSETS	Q2FY83	100
RSTS SMALL BATCH & UTILITIES	Q1FY84	100
RSTS NI SUPPORT	H1FY84	100
RSX ENHANCED BACKUP	Q2FY83	---
RT EXTENDED MEMORY	Q4FY83	100
RT NEW BACKUP	Q4FY83	100
RT CUSTOMER INSTALLATION	Q4FY83	100
MICRO-POWER HOSTED BY RSX & VMS	Q4FY83	---
FORTRAN FULL ANSI-77	Q1FY84	300
COBOL-81 REPLACE COBOL-11	Q4FY83	400
BASIC-PLUS-2 TRACK STANDARDS	Q2FY84	300
RMS-11 REMOVAL FROM USER SPACE	Q2FY84	500
SORT-11 REWRITE	Q4FY83	100

FMS-11 REWRITE	Q3FY84	500
32-BIT PROGRAM		
11/780		
64K CHIP	Q2FY83	142
CI CLUSTERS/HI AVAILABILITY		800
COMMUNICATIONS SWITCH	FY83	330
11/750		
CI750	Q1FY84	1106
FP750	SHIPPED	84
PACKAGED SYSTEMS	FY83	201
UNA/UDA	?	200
DW750	Q4FY82	288
11/730		
COMBO	Q4FY82	375
BATTERY BACKUP	Q3FY83	375
PACKAGED SYSTEMS	FY83	200
VENUS		
DEVELOPMENT	FY84	15300
NAUTILUS		
DEVELOPMENT	FY85	6049
SCORPIO		
DEVELOPMENT	FY85	6200
WORKSTATION		
DEVELOPMENT		
- HIGH END BUYOUT WORKSTATION	Q2FY83	900
- LOW END WORKSTATION	Q4FY83	5400
MICRO-VAX		
START-UP		1300
CHIP & BOARD SOFTWARE		700
CLUSTERS/HI AVAILABILITY*		
CI CLUSTERS	Q4FY82	
HI AVAILABILITY	Q4FY83	
*BUDGET PART OF 11/780 PROGRAM		
32-BIT SOFTWARE		
VMS	4QFY82	5806
VAX11 RMS	4QFY82	1201
VAX11 PL/1		601
HYDRA (DATA INTEGRITY)		3003
SMALL 32-BIT		1802
VAX11 RTL		890
VAX11 DEBUGGER		574
VAX11 SORT/MERGE	4QFY83	133
VAX11 EDITOR	4QFY83	265
VAX CROSS LAN TEST		90

VAX11 APL		332
VAX11 BASIC		890
VAX11 COBOL	4QFY82	980
VAX11 FORTRAN	4QFY82	413
VAX11 PASCAL V1.2		---
VAX11 PASCAL V2.0	1QFY83	493
ADA	FY83	574
ADA PSE		332
CATS	2HFY83	2037
TPSS	2HFY83	2058
IMS ARCHITECTURE		268
VAX11 DBMS	2QFY84	1352
CDD-32	6/82	425
RDMS-32	4/83	1057
DTR/DDMF-32	2HFY83	759
CATS/TPSS ARCH		---
VTC	2QFY83	---
CHIP & BOARD		800
PASCAL-11		81
36-BIT PROGRAM		
JUPITER SYSTEM		
JUPITER HARDWARE (2080)	1QFY84	7075
JUPITER T20/COMM		1096
NI PLUTO		83
JUPITER HSC-50		119
JUPITER/20 COMM		576
JUPITER TOPS-10		0
36-BIT SOFTWARE		
APLSF	3QFY83	100
MACRO/LINK	FY83	40
FORTRAN V7	3QFY83	400
36-BIT HARDWARE		
CURRENT PRODUCT SUPPORT		691
KLIPA		107
36-BIT COMM SOFTWARE		
DECNET-10 3.0		72
X.29		83

"TO" DISTRIBUTION:

JOHN ADAMS	JACK BUCKLEY	CONDON @MK12
PETER F CONKLIN	GARY J ECKROTH	GEORGE EVANS
DAVE FERNALD	BOB FLYNN	LLOYD FUGATE
MIKE GALLUP	ROBERT JOSEPH	GARY KEELER
JOHN O'KEEFE	BILL PICOTT	DICK RISLOVE
DAVID STROLL	DICK STRAUSS	GEORGE TH1SSELL

FMS		1308
GRAPHICS		555

STORAGE PROGRAM

RA81 & SWFT	Q1FY83	2343
RD50/51	Q2FY83	425
AZTEC	Q4FY83	6160
HSC50	Q4FY83	5170
TA78	Q4FY83	720
RA60 & SWFT	Q3FY83	4011
TU81/TA81	Q483	1000
TU80	Q3FY83	450
UDA-52	Q4FY83	1300
RX50	Q2FY83	609
RAXX & SWFT	Q3FY86	4296
MAYA	FY86	1575
AZTEC II	Q4FY85	250
RAXY	Q3FY86	(WITH RAXX)
YANKEE	FY87	500
HSC CACHE	Q4FY84	1000
SHRIMP	FY87	0
BSA	Q4FY87	0
RD52	Q2FY85	2080
RX52/53	Q3FY85	600

/jdm
RC1.S6.47

"TO" DISTRIBUTION:

JOHN ADAMS	JACK BUCKLEY	CONDON @MK12
PETER F CONKLIN	GARY J ECKROTH	GEORGE EVANS
DAVE FERNALD	BOB FLYNN	LLOYD FUGATE
MIKE GALLUP	ROBERT JOSEPH	GARY KEELER
JOHN O'KEEFE	BILL PICOTT	DICK RISLOVE
DAVID STROLL	DICK STRAUSS	GEORGE THISSELL

ENGINEERING DEVELOPMENT SUMMARY

PRODUCT	ENG $M '83 -'85	NOR $B '82 -'86	NOR $B LIFETIME
11/780, 11/750, 11/730	28.1	12.8	17.9
VENUS	42.4	1.8	10.2
NAUTILUS	23.8	.2	11.9
SCORPIO	22.0	.3	6.0
MICROVAX	13.0	?	?
VMS FAMILY SOFTWARE	95.5*	^	^
ALL 11'S TO 11/23+		4.0	4.5*
LCP 5, 8 (F-11 BASED)	3.3	.3	1.3*
ORION U, Q (J-11 BASED)	9.4	.4	2.4*
16B SOFTWARE	44.4	^	^
AZTEC I & II	17.2	1.4@	5.7
HSC & BSA CHANNELS/ADAPTORS	14.2	.3	.8
RA81, RAXX, RAXY (LARGE DISKS)	33.1	1.3	7.7
TA78, TU80, TU/TA81 (IND. TAPES)	4.2	1.2	2.5
SM. DIAM. DISKS (RX, RD)	9.6	1.3	1.8
SHRIMP (5 1/4" WINI)	5.4	-	3.0
MAYA (SM HI CAPACITY TAPE)	13.9	.1	3.3
RA60 (PINION & REMOVABLE DISK)	4.1	1.0	1.7
CT/CAT/DECMATE II	52.2	9.8*	?
TOTAL VIDEO FAMILY	26	1.8	4.2
TOTAL HARDCOPY	29.3	1.5	2.2
WORKSTATION (INCL. 32B, ETC.)	15.6	.6	1.6
U.Q BUS OPTIONS +1.4			
NI. ETHERNET HDW +3.9			
DECNET & X.25 SW +2.3			
SERVERS & GATEWAYS +3.0			
TOTAL DISTRIBUTED SYSTEMS	o75.2	^?	^?
36 BIT SYSTEMS PROGRAM	33.4	.7	1.6
CTAB/OFFICE +2.2			
TOTAL OFFICE PROGRAM	23.5	?	?
COEXISTANCE 20/VAX +1.0			
TOT. COEXIST., TOOLS, X-PROD. SW	8.5		
SEMICONDUCTOR PRODUCTS	31.7**		
SEG TOOLS & ADV DEV	19.7**		
PROCESS TECHNOLOGY	31.5		

NOTES:

? No estimate of revenue
^ Included in systems revenue
@ Most of the disk revenue is included in the systems revenue
+ FY83 $M
* Eli Glazer estimate
o Includes all Non-Product Expenses
** Does not include manufacturing process engineering investment

****
* d i g i t a l *
****

TO: see "TO" DISTRIBUTION

cc: PEG:

DATE: WED 10 FEB 1982 3:44 PM EST
FROM: RICK CORBEN
DEPT: CORP PRODUCT MGMT
EXT: 223-3123
LOC/MAIL STOP: ML12-1/-T39

SUBJECT: ENGINEERING PROJECT LIST - PART II

********** PART II **********

	FRS	FY'83 K$
TERMINALS & WORKSTATIONS PRODUCTS		
CT Family		
CT100	Q1FY83	8379
CT25	Q1FY84	662
CT CLUSTERS	Q1FY84	1694
PRINTING		
LA100RO	Q3FY83	500
LOW COST RO--BUYOUT	FY83	200
LOW COST RO--BUILD	FY85	1100
ELECTRONIC PRINTERS		
- EP1 (10-12 PPM)	Q2FY83	200
- EP3 (5-6 PPM)	FY86	700
KEYBOARDS (LA/VT/CT 200)		200
VIDEO		
VT200-QX (LOW COST)	Q3FY83	1200
VT200-H (HALF-PAGE)	Q4FY83	2950
VT200--FULL PAGE	Q1FY85	800
VT200 CUSTOM LSI	N/A	1100
VT200 SYSTEMS REF.		
MANUAL & PROGRAMMER'S MANUALS	N/A	150
VT200 INTERACTIVE I/O OPTIONS		
(LIGHT PEN/TABLET, ETC.)	N/A	235
OFIS PROGRAM		
DECmail V1.1	Q1FY83	419
VAX/OFFICE R1	Q2FY83	1600
OFFICE/FRENCH	Q3FY83	100
OFFICE/GERMAN	Q3FY83	100
VAX/OFFICE R2	Q4FY83	---
VAX/OFFICE R3	FY84	---
RSX11M+/OFFICE R1	Q4FY83	200
CTAB/OFFICE R1	Q4FY83	2200
CTAB/OFFICE R2	FY84	---
CTAB/OFFICE R3	FY84	

NOTE: Allocation of FY'83 spending to specific

releases is especially arbitrary in the case of OFIS.

DISTRIBUTED SYSTEM PRODUCTS*

*(See Glossary of terms attached)

UNIBUS OPTIONS		
HDLC SUPPORT IN DMP	H1FY84	250
DMZ32	H1FY84	PL FUNDED
QBUS OPTIONS		
DZV-8	H1FY84	400
HDLC SUPPORT IN DMV	H1FY84	250
NI HARDWARE		
TRANSCEIVER	1/83	40
UNA	6/83	640
TRANSCEIVER POWER SUPPLY	H1FY84	100
PLUTO	9/83	1070
LSI QNA	FY86	250
INTELLIGENT UNA	FY86	400
PLUTO JR.	H1FY85	600
LNI	Q1FY84	300
BROADBAND TRANCEIVER	H2FY84	500

NOTE: MSI QNA is funded out of PSD, CTNA is funded out of CT Program.

DECNET		
DECnet RSX (PIV & NI)	Q3FY84	422
DECnet VAX (PIV & NI)	Q4FY83	1200
DECnet E (PIV & NI)	H2FY84	500
X.25 (STANDALONE PSI PRODUCTS)		
VAX PSI	6/82	60
RSX PSI	3/83	100
SERVERS		
SERVER BASE	Q4FY83	568
ROUTER	Q1FY84	283
X.25 GATEWAY	6/84	440
SNA GATEWAY(NON NI)	2/83	484
SNA GATEWAY(NI)	Q4FY84	460
TERMINAL CONC.	9/83	560
XEROX GATEWAY	H2FY85	209

CROSS SYSTEM COEXISTENCE SOFTWARE

COEX COMPUTERS	220
DATA CONVERSION SUB	73
DIU	293
MSG TRANS SYST/MTS	219
REMOTE FILE ACCESS	142
REMOTE SPOOLING & BATCH	73

FMS	1308
GRAPHICS	555

STORAGE PROGRAM

RA81 & SWFT	Q1FY83	2343
RD50/51	Q2FY83	425
AZTEC	Q4FY83	6160
HSC50	Q4FY83	5170
TA78	Q4FY83	720
RA60 & SWFT	Q3FY83	4011
TU81/TA81	Q483	1000
TU80	Q3FY83	450
UDA-52	Q4FY83	1300
RX50	Q2FY83	609
RAXX & SWFT	Q3FY86	4296
MAYA	FY86	1575
AZTEC II	Q4FY85	250
RAXY	Q3FY86	(WITH RAXX)
YANKEE	FY87	500
HSC CACHE	Q4FY84	1000
SHRIMP	FY87	0
BSA	Q4FY87	0
RD52	Q2FY85	2080
RX52/53	Q3FY85	600

/jdm
RC1.S6.47

"TO" DISTRIBUTION:

JOHN ADAMS	JACK BUCKLEY	CONDON @MK12
PETER F CONKLIN	GARY J ECKROTH	GEORGE EVANS
DAVE FERNALD	BOB FLYNN	LLOYD FUGATE
MIKE GALLUP	ROBERT JOSEPH	GARY KEELER
JOHN O'KEEFE	BILL PICOTT	DICK RISLOVE
DAVID STROLL	DICK STRAUSS	GEORGE THISSELL

ENGINEERING DEVELOPMENT SUMMARY

PRODUCT	ENG $M '83 -'85	NOR $B '82 -'86	NOR $B LIFETIME
11/780, 11/750, 11/730	28.1	12.8	17.9
VENUS	42.4	1.8	10.2
NAUTILUS	23.8	.2	11.9
SCORPIO	22.0	.3	6.0
MICROVAX	13.0	?	?
VMS FAMILY SOFTWARE	95.5*	^	^
ALL 11'S TO 11/23+		4.0	4.5*
LCP 5, 8 (F-11 BASED)	3.3	.3	1.3*
ORION U, Q (J-11 BASED)	9.4	.4	2.4*
16B SOFTWARE	44.4	^	^
AZTEC I & II	17.2	1.4@	5.7
HSC & BSA CHANNELS/ADAPTORS	14.2	.3	.8
RA81, RAXX, RAXY (LARGE DISKS)	33.1	1.3	7.7
TA78, TU80, TU/TA81 (IND. TAPES)	4.2	1.2	2.5
SM. DIAM. DISKS (RX, RD)	9.6	1.3	1.8
SHRIMP (5 1/4" WINI)	5.4	-	3.0
MAYA (SM HI CAPACITY TAPE)	13.9	.1	3.3
RA60 (PINION & REMOVABLE DISK)	4.1	1.0	1.7
CT/CAT/DECMATE II	52.2	9.8*	?
TOTAL VIDEO FAMILY	26	1.8	4.2
TOTAL HARDCOPY	29.3	1.5	2.2
WORKSTATION (INCL. 32B, ETC.)	15.6	.6	1.6
U.Q BUS OPTIONS +1.4			
NI. ETHERNET HDW +3.9			
DECNET & X.25 SW +2.3			
SERVERS & GATEWAYS +3.0			
TOTAL DISTRIBUTED SYSTEMS	°75.2	^?	^?
36 BIT SYSTEMS PROGRAM	33.4	.7	1.6
CTAB/OFFICE +2.2			
TOTAL OFFICE PROGRAM	23.5	?	?
COEXISTANCE 20/VAX +1.0			
TOT. COEXIST., TOOLS, X-PROD. SW	8.5		
SEMICONDUCTOR PRODUCTS	31.7**		
SEG TOOLS & ADV DEV	19.7**		
PROCESS TECHNOLOGY	31.5		

NOTES:

? No estimate of revenue
^ Included in systems revenue
@ Most of the disk revenue is included in the systems revenue
+ FY83 $M
* Eli Glazer estimate
o Includes all Non-Product Expenses
** Does not include manufacturing process engineering investment

* * * * * * * * *
* d i g i t a l *
* * * * * * * * *

MEMORANDUM

TO: Win Hindle
Bill Thompson

CC: Gordon Bell
Jack Smith
Rick Corben

DATE: 2 APRIL 1982
FROM: JOSEPH REILLY
EXT: 223-6883
DEPT: CE FINANCE
LOC/MS: ML12-2/A16

SUBJECT: ENGINEERING DEVELOPMENT SUMMARY - IRR'S

Attached FYI are the internal rates of return for the products that correspond with Gordon's presentation to the Operations Committee.

Please note the following:

- IRR does not recognize that some products 'piggyback' on the investment of others (i.e., the DMR11 used a lot of the development technology of the DMP11).
- The IRR'S will change sometimes significantly as BURPS are updated with changes (i.e., pricing, volume, timing, etc.).

RLO.4.10

ENGINEERING DEVELOPMENT SUMMARY
IRR'S

GROUP	PRODUCT	IRR %	MOST RECENT RUN DATE
32-BIT	11/780	53	2/82
	11/750	45	2/82
	11/730	63	2/82
	VENUS	41	12/81
	NAUTILUS	--	Available Q1 FY83
	SCORPIO	--	Available Q4 FY82
	MICROVAX	--	Available Q4 FY83
	WORKSTATION	--	Available Q4 FY83
16-BIT	11/24	71	11/80
	11/44	89	3/79
	11/23+	91	1/82
	LCP-5	59	2/82
	LCP-8	85	12/81
	ORION-U	147	9/81 (1st pass soft)
	ORION-Q	147	9/81 (1st pass soft)
STORAGE	AZTEC I	39	3/82
	AZTEC II	--	N/A
	HSC-50	35	11/81
	BSA	--	N/A
	TA78	--	N/A
	TU80	33	1/82
	TU/TA81	--	N/A
	RX50	29	9/81
	RD50	67	12/81
	SHRIMP	--	N/A
	MAYA	--	N/A
	RA60	41	3/82
	RA80	47	3/82
	RAXY	--	N/A
	RAXY	--	N/A
TERMINALS & WORKSTATIONS	CT-100	48	11/81
	VT100	33	6/80
	VT101/102/131	55	4/81

GROUP	PRODUCT	IRR %	MOST RECENT RUN DATE
TERMINALS & WORKSTATIONS	VT210	65	2/82
	LA100	47	11/80
	LA12	37	6/81
	LA120	31	6/80
	LA36	31	6/80
	LA180	31	6/80
	LA34	23	6/80
DISTRIBUTED SYSTEMS			
U/Q BUSOPTIONS			
	DMR11	53	10/80
	DPV11	25	8/80
	DMP11	19	9/81
	D232	39	4/81
	DMV11	16	9/81
	DMF32	83	3/82
NI ETHERNET H/W			
	TRANSCEIVER	39	1/82
	PLUTO HDW	--	Available Q4 FY82
	UNA	43	
DECNET S/W			
	RSX V3.1	60	2/82
	RSX V4.0	--	Available Q2 FY83
	VMS V3.B	--	Available Q2 FY83
	CT	--	Available Q4 FY83
SERVERS & GATEWAYS			
	PLUTO SYST	--	Available Q3 FY83
32-BIT	JUPITER	35	1/82
SOFTWARE			
OF15 PROGRAM			
	DECMAIL	46	3/82
	OFIS/VMS	36	3/82
	OFIS/CTAB	16	3/82
	OFIS/RSTS	55	3/82

ENGINEERING DEVELOPMENT SUMMARY

PRODUCT		ENG. $M '83 - '85	IRR
11/780, 11/750, 11/730		28.1	
VENUS		42.4	
NAUTILUS		23.8	
SCORPIO		22.0	
MICROVAX		13.0	
VMS FAMILY SOFTWARE		95.5*	
ALL 11'S TO 11/23+			
LCP 5, 8 (F-11 BASED)		3.3	
ORION U, Q (J-11 BASED)		9.4	
16B SOFTWARE		44.4	
AZTEC I & II		17.2	
HSC & BSA CHANNELS/ADAPTORS		14.2	
RA81, RAXX, RAXY (LARGE DISKS)		33.1	
TA78, TU80, TU/TA81 (IND. TAPES)		4.2	
SM. DIAM. DISKS (RX, RD)		9.6	
SHRIMP (5 1/4" WINI)		5.4	
MAYA (SM HI CAPACITY TAPE)		13.9	
RA60 (PINION & REMOVABLE DISK)		4.1	
CT/CAT/DECMATE		52.2	
TOTAL VIDEO FAMILY		26.0	
TOTAL HARDCOPY		29.3	
WORKSTATION (INCL. 32B, ETC.)		15.6	
U.Q BUS OPTIONS	+ 1.4		
NI. ETHERNET HDW	+ 3.9		
DECNET & X.25 SW	+ 2.3		
SERVERS & GATEWAYS	+ 3.0		
TOTAL DISTRIBUTED SYS.		75.2	
36 BIT SYSTEMS PROGRAM		33.4	
CTAB/OFFICE	+ 2.2		
TOTAL OFFICE PROGRAM		23.5	
COEXISTANCE 20/VAX	+ 1.0		
TOT. COESIST., TOOLS, X-PROD. SW		8.5	
SEMICONDUCTOR PRODUCTS		31.7**	
SEG TOOLS & ADV DEV		19.7**	
PROCESS TECHNOLOGY		31.5	

* Eli Glazer Estimate

** Does not include manufacturing process engineering investment.

RL0.4.9 - April 1982

	Direct	CE
uPG	4.3	3.3
Toem		2.2
WP		10.8
TPG.	10.1	3
MSG.	1.8	
LDP	5.5	
TPL	1.0	
ECS	1.6	
ESG	2.9	
GSG	2.8	
LGG.	1.4	
Coem.	4.0	
esi	.9	
PGi	4.5	
MDC	5.3	
Tig	6.6	3.8
AS+G		
ESS		
	6.	
	58.7	20.1

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* d i g i t a l *
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TO: OPERATIONS COMMITTEE:

cc: GROUP CONTROLLERS:

DATE: MON 10 MAY 1982 5:19 PM EDT
FROM: SHELDON ARONOFF
DEPT: CORP FIN PLNG & ANAL
EXT: 223-8707
LOC/MAIL STOP: MS/G15

SUBJECT: MAY BUDGET WOODS

This is to confirm the conversation at today's Operations Committee on the FY83/84 Budget Proposals.

The proposals as submitted are unacceptable.

- Volumes look high compared to current order rates and uncertainty in the economy.
- Strategic Plan Direct margin goals have not been achieved by most of the Planning Units. (Product Groups, Europe)
- Spending generally does not meet the 11% per annum productivity improvement goal established by Operations Committee.

Operations Committee members and/or their direct reports will present revised proposals at the May Woods that meet the agreed to goals.

The proposals will make visible the following:

- Rationale justifing the volume proposal, including visibility on quarterly ramps.

- Spending meeting the 11% per annum productivity improvement test agreed to by Operations Committee.

- Specific investments that prevent achieving the direct margin goal and/or the productivity improvement goal, with clear indications of their cost/benefit.

- The highly recommended lists, by category, and the annual dollars tied to same.

- The performance standards established in the group to distinguish exceptional performance from satisfactory performance and from unsatisfactory performance.

Detailed changes to Budget proposals can be accepted through tommorrow noon by the budget system. The data, as of that time, will be incorporated into the Budget Package to be distributed to Operations Committee later this week.

However, I will process revised commitments communicated to me via memo/EMS through Monday, May 17. This will allow me to have available for Operations Committee a "base" corporate proposal at the Woods.

lms

timelines IS NOT Schedule

EG:kr4.10

ENGINEERING DEVELOPMENT SUMMARY

PRODUCT	ENG $M Σ '83 -'85	NOR $B Σ '82 -'86	NOR $B LIFETIME
~~11/780~~, ~~11/750~~, 11/730 /11/782	28.1	12.8	17.9
VENUS	42.4	1.8	10.2
NAUTILUS	23.8	.2	11.9
SCORPIO (incl. chip)	22.0	.3	6.0
MICROVAX	13.0	?	?
VMS FAMILY SOFTWARE —	95.5*	↑	↑
ALL 11'S TO 11/23+		4.0	4.5*
LCP 5, 8 (F-11 BASED)	3.3	.3	1.3*
ORION U, Q (J-11 BASED)	9.4	.4	2.4*
16B SOFTWARE	44.4	↑	↑
AZTEC I & II	17.2	1.4@	5.7
HSC & BSA CHANNELS/ADAPTORS	14.2	.3	.8
RA81, RAXX, RAXY (LARGE DISKS)	33.1	1.3	7.7
TA78, TU80, TU/TA81 (IND. TAPES)	4.2	1.2	2.5
SM. DIAM. DISKS (RX, RD)	9.6	1.3	1.8
SHRIMP (5 1/4" WINI)	5.4	-	3.0
MAYA (SM HI CAPACITY TAPE)	13.9	.1	3.3
RA60 (PINION & REMOVABLE DISK)	4.1	1.0	1.7
CT/CAT/DECMATE II	52.2	9.8*	?
TOTAL VIDEO FAMILY	26	1.8	4.2
TOTAL HARDCOPY	29.3	1.5	2.2
WORKSTATION ~~(INCL. 32B, ETC.)~~	15.6	.6	1.6
U.Q BUS OPTIONS — +1.4			
NI. ETHERNET HDW — +3.9			
DECNET & X.25 SW — ~~+2.3~~			
SERVERS & GATEWAYS — +3.0			
TOTAL DISTRIBUTED SYSTEMS	°75.2	↑?	↑?
36 BIT SYSTEMS PROGRAM	33.4	.7	1.6
CTAB/OFFICE +2.2			
TOTAL OFFICE PROGRAM	~~23.5~~	?	?
COEXISTANCE 20/VAX +1.0			
TOT. COEXIST., TOOLS, X-PROD. SW	8.5		
SEMICONDUCTOR PRODUCTS	31.7**		
SEG TOOLS & ADV DEV	19.7**		
PROCESS TECHNOLOGY	31.5		

NOTES:

? No estimate of revenue
↑ Included in systems revenue
@ Most of the disk revenue is included in the systems revenue
+ FY83 $M
* Eli Glazer estimate
o Includes all Non-Product Expenses
** Does not include manufacturing process engineering investment

PRODUCT	ENG. AM Σ '83-'85	NOR*B Σ'82-'86	NORB LIFETIME
11/780, 11/750, 11/730	28.1	12.8	17.9
VENUS	42.4	1.8	10.2
NAUTILUS	23.8	.2	11.9
SCORPIO	22.0	.3	6.0
MICROVAX	13.0		
VMS FAMILY SOFTWARE	95.5*		
ALL 11'S TO 11/23+		4.0	4.5*
LCP 5,8 (F-11 BASED)	3.3	.3	1.3*
ORION U,Q (J-11 BASED)	9.4	.4	2.4*
16B SOFTWARE	44.4		
AZTEC I & II	17.2	1.4	5.7
HSC + BSA ADAPTORS	14.2	.3	.8
RA81, RAXX, RAXY (LARGE DISKS)	33.1	1.3	7.7
TA78, TU80, TU/TA81 (INDUSTRY TAPES)	4.2	1.2	2.5
SM. DIAM. DISKS (RX, RD)	9.6	1.3	1.8
SHRIMP (5¼" WINI)	5.4	—	3.0
MAYA (SM HI CAPACITY TAPE)	13.9	.1	3.3
RA60 (PINION + REMOVABLE DISK)	4.1	1.0	1.7
CT/CAT/DECMATE II	52.2	9.8 *	
TOTAL VIDEO FAMILY	26	1.8	4.2
TOTAL HARDCOPY	29.3	1.5	2.2
WORKSTATION (INCL 32B etc)	15.6	.6	1.6
U.Q BUS OPTIONS + 1.4			
NI - ETHERNET HDW + 3.9			
DECNET + X.25 SW + 2.3			
SERVERS & GATEWAYS + 3.0			
TOTAL DISTRIBUTED SYSTEMS	⊖75.2		
36 BIT SYSTEMS PROGRAM	33.4	.7	1.6
CTAB/OFFICE +2.2			
TOTAL OFFICE PROGRAM	23.5		
COEXISTANCE 20/VAX +1.0			
TOTAL COEX., TOOLS, CROSS PRODUCT. SW	8.5		
SEMI CONDUCTOR PRODUCTS	31.7 **		
SEG TOOLS & ADV DEV	19.7 **		
PROCESS TECHNOLOGY	31.5		

* EG estimate | + FY83 AM | ⊖ INCLUDES ALL NON PRODUCT EXPENSES

** ?

the corridor talk at most OEM trade shows deals with just that issue. His advice to emerging OEMs: "Pick a vertical market, stick to it and do a good job, and you won't have a problem."

Daniel Vertrees, vice president for Digital Systems of Florida, one of the larger OEMs, agrees. By developing specialized DEC-based systems for certified public accountants, law offices and contractors, Vertrees says his company has been able to carve out markets which DEC, with its general-purpose software, has yet to penetrate. With $37 million in sales in 1981 and "shooting for $50 million in 1982," Digital Systems is DEC's "number-one stepchild, whether they like it or not," Vertrees says.

Sandra Kurtzig, president of ASK Computer Inc., Hewlett-Packard's largest OEM, says most hardware vendors are dying to get into ASK's two main markets — turnkey systems utilizing manufacturing and financial-management software. She notes that end users are "buying solutions, not hardware," however, and that gives ASK the edge — from both technological and marketing standpoints — over the computer makers. In addition, an OEM such as ASK, which buys hardware from HP and DEC, is not limited to any one vendor's product line, but can match its own software to a customer's needs and/or hardware preference.

With all the problems ahead, no one is likely to give up too soon on the OEM minicomputer sector — least of all Data General, ranked by IDC second, after DEC, in OEM shipments and third in revenues. According to Donald McDougall, acting general manager of Data General's Technical Products Division, "Productivity-related products used in computer-aided design and manufacturing, numerical control, robotics and automatic test equipment" will be the OEM "areas that are going to be the most interesting" for minicomputer makers in the next five to 10 years.

Board business booming

After minicomputers, board-level, or single-board, computers represent the next biggest tier of OEM business After slowing down somewhat in th early months of the recession, sal suddenly rebounded in the fou quarter of 1981, reports Ral Gilman, a senior analyst at Dataq Inc.

Robert Brannon, general man

Financial data on the top OEM minicomputer makers

	Totals for the company or for the closest division that includes OEM minicomputers		Total company revenues ($ million)	Cost of sales (mfg. cost as % of sales)	Per employee		R&D as a % of total revenues
	Sales ($ million)	Net income (% of sales)			Total revenues	Net income	
Computer Automation	$ 75.6	2.2%	$ 75.6	50.8%	$65,796	$1,480	9.6%
Data General	736.9	6.9%	736.9	51.9%	50,386	3,464	10.1%
Digital Equipment	3,198.1	10.7%	3,198.1	55.6%	50,763	5,449	7.9%
General Automation	86.5	N.A.	124.9	66.0%	69,000	68	3.8%
Gould	1,846.1	5.2%	1,846.1	N.A.	N.A.	N.A.	N.A.
Harris	258.6	8.4%	1,551.5	65.8%	60,136	4,031	5.3%
Hewlett-Packard	1,771.0	9.7%	3,578.0	47.6%	55,906	4,875	9.7%
Honeywell	1,773.7	6.3%	5,351.2	64.0%	55,211	2,675	6.9%
IBM	19,109.0	13.4%	29,070.0	41.3%	81,902	9,320	5.5%
Modular Computer	87.2	1.3%	87.2	N.A.	N.A.	N.A.	N.A.
Perkin-Elmer	232.5	5.4%	1,115.8	56.5%	72,447	5,072	7.5%
Prime Computer	364.8	10.3%	364.8	43.8%	78,686	8,127	7.5%
Sperry	2,707.4	6.2%	5,427.2	60.2%	58,687	3,385	6.2%
Tandem	208.4	12.7%	208.4	36.3%	76,336	9,725	8.6%
Texas Instruments	1,064.0	1.5%	4,206.0	77.0%	50,242	1,296	5.2%

Data based on latest annual report ending before Dec. 31, 1981

N.A.—not available

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* d i g i t a l *
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TO: CE CONTR. STAFF:
EMC:
PEG:

DATE: TUE 18 MAY 1982 9:13 AM EDT
FROM: JOE REILLY
DEPT: CE FINANCE
EXT: 223-6883
LOC/MAIL STOP: ML12-2/A16

SUBJECT: FY'83 BUDGET

RLo:SECT6/5.42

The EMC approved the following budget:

GROUP	
16 Bit	13.5
Terminals & WS	34.5
32 Bit	42.o
Distributed Systems	21.o
LSG	36.7
Storage	53.9
Software	61.3
SEG	2o.9
TOPS	7.5
Process Tech	9.2
SA&T	11.9
Sites	10.o
Central & Other	19.7
West Coast	
CMU	4.5
Japan	
TOTAL	346.6

SUMMARY

- All groups will deliver their 'A' Scenario.
- New requests must be funded by tradeoffs of current scenario.
- There is no Contingency or General Technology Fund.
- Japan, CMU, West Coast total cannot exceed 4.5 MEG.
- Each group will quarterize their own numbers.

18-MAY-82 09:20:57 S 2494 EMML