"THE RIGHT BOOKS TO WRITE IN"

NATIONAL FIGURING BOOK
56-800 SERIES

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<tr>
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<tr>
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<tr>
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<td>56-802</td>
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<tr>
<td>56-820</td>
<td>20 Columns</td>
</tr>
</tbody>
</table>

ALL COLUMNAR RULINGS WITH UNITS

WHEN YOU NEED ANOTHER BOOK, ORDER FROM YOUR STATIONER BY SPECIFYING NUMBER ABOVE.

Made in U. S. A.
<table>
<thead>
<tr>
<th>Site</th>
<th>Date</th>
<th>Meeting</th>
<th>Page</th>
<th>Date</th>
<th>Meeting</th>
<th>Page</th>
</tr>
</thead>
<tbody>
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</tbody>
</table>
Dear Tom,

Per our conversation of this week, I am enclosing a copy of Avco’s tentative specification requirements for a power transistor.

Avco is interested in giving us a development contract for this type of unit.

The dollar figure they talked about is $25K to $50K. For this they would expect about 12 units for evaluation in six to eight months.

They would also consider something in the area of $1,000 each for the first 50 units and $100 each for subsequent orders.

P.S.I. has looked at their spec but as yet they have made no definite proposal.

I promised Avco an answer by November 16, 1962.

Regards,
Bernie

Gordon E. Moore

Final Call bay after you look at this.
TRANSMITTER REQUIREMENTS

High Power

One device or max. of 3 in parallel

Power Output (R.F.)

45 watts min. at \( V_{cc} = 22 \) VDC

Class of Operation

AB Linear

\( V_{cc} \)

23 volts standard
18 to 30 volts service

Frequency

60 kHz

Power Gain

10 dB max. over frequency range

Neutralization

None

Emitter Tuning

None
**Collector**

Collector DC and RF isolated from case. RF isolation impedance of 500 ohms min. over frequency range.

**Mounting**

Stud

**Leads**

Axially or collector separated from base and emitter as much as possible.

**Collector Efficiency (RF out vs. DC in)**

45 percent min. at max. drive.

**Material**

Silicon

**Distortion**

Output intermodulation distortion products shall be at least 35 db below one of (2) two equal amplitude desired tones; the amplitude of the tones such that the peak envelope power output can be from 0 to 40 watts at Vcc = 25 VDC and the tone frequencies can be anywhere in the 3 - 50 me range but separated from each other by 500 cps.

**DC Beta Gain**

15 min.

**Temperature**

Operating: -45°C to +85°C
Storage: -65°C to +100°C
TRANSISTOR REQUIREMENTS

Low Power

One device

Power Output (RF)

4 watts min. at $V_{cc} = 28$ VDC

Remaining requirements same as for high power device.

Problems:

D.C. & RF isolation from case

Axial leads

4 watts at 88 Mc Can AB, must meet something at 4 Mc, discrimination.
Review of Four Dome data - 11/15/62

Our primary epiterial is not quite there - it is only 150m away and it has been for 40 yrs.

On triple different, Mt. View is nothing.

On Western, 17, 12, 27e on 3 mm, at 7000 feet to collect. Name and south face prominent.

Lye 710205

Plain material: 35% in third one.

Some material of many sides thin. soil in conclusion for finer dimensions.
Meeting 11/19/62

C.M. Mack 96

D.E. Met on epipolar development:
1. for low power
2. for high speed

The materials:
- Conductive 632-em p-type
- L.P.
- 0.52-em legs
- 10-12-pik thick
- 1000°C A
- (RT-1 mini)
- X59 with ula.

\[ V_T \]
\[ C_{m} \text{ mS} \]
\[ C_{m} \text{ mS} \]
\[ R_s \]
\[ V_{th} \text{ (caply)} \] \approx 10\%

\[ \text{PCT} \times \text{p/f} \] 60mA @ 10mV
\[ V_c \text{ p/f} \] < 5mV

# of rows: \( \rightarrow \) (of gates) \( \rightarrow \) \( \rightarrow \) \( \rightarrow \) 1

We have also a test vehicle which makes for different gate geometries.

Most are of separate Justice in m. These have geometries like:

\[ \text{Scale: } 1:4 = 0.001'' \]

These violate the rules for metal cuts.
February Production

<table>
<thead>
<tr>
<th>Date</th>
<th>Action</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nov. 19</td>
<td>Define Objective</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Define Objective</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Evaluate Contender</td>
<td></td>
</tr>
</tbody>
</table>

11/19
1. Define Objective
2. Breadboard contender
3. Evaluate Contender

12/1
4. Start layout of Contender Max. 2 types, 1 prime
2 G₂ + (R), alternate
2 G₂ only.
5. Masks complete - 12-21 for GR
Masks complete - R Jan. 1

Mar. 1 Test Spec
Test Spec

F.M. < a⁻¹ A⁻¹/₂ (hₜₑₘₐₓ - hₜₑₘᵦₖ) / hₜₑₘᵦₖ

Rₐₗₜₜ max - Rₐₗₜₜₕᵦₖ min
Rₐₗₜₜₕᵦₖ min
DRIFT STUDIES OF SURFACE POTENTIAL CONTROLLED F.E.T.

Otto Leistiko

I. OBJECT
A. To make a stable surface potential controlled field effect transistor.
B. To understand the mechanism that causes the change in channel current, under set conditions, with time.

II. For the experiments, the viewpoint will be adopted that the cause of drift is intimately connected with the dielectric between the surface gate and channel, and that the dielectric is SiO₂. The regions of the dielectric to be investigated in detail are:
C. Surface of the dielectric
B. Bulk of the dielectric
A. The interface of the dielectric and channel region.

III. Since there are a great many factors which affect the structure of the dielectric and its immediate surroundings, we will consider each region separately. The following is a list of processes and effects which can be associated with each region, more or less.
A. The interface of the dielectric and channel.
   1. The dopants used in the starting material
      a. Al-P, Al-Sb, Al-As, Ga-P, Ga-Sb, Ga-As or others, epitaxial
   2. Surface preparation before first oxidation
      a. Special cleaning, Formic - \textit{H}_2\textit{O}_2
      b. Short oxidation - strip off then oxidize again
   3. Agglomeration of fast diffusing in purities
      a. Gold
      b. Nickel
   4. Oxide growth
      a. Dry \textit{O}_2
      b. Steam \textit{O}_2
   5. Regrown oxide
B. Bulk of the dielectric
   1. Oxide growth
      a. Dry \textit{O}_2
      b. Steam \textit{O}_2
      c. Temperature
   2. Regrown oxide
3. Impurities in the oxide resulting from starting material and process
   a. Al
   b. Ga
   c. B
   d. P
   e. OH

C. Surface of the dielectric
   1. Cleanliness
      a. Special cleanliness throughout process
      b. Special cleaning before last very high temperature step
      c. Special cleaning before last high temperature step
   2. Impurities resulting from process
      a. Al (metalizing)
      b. B
      c. P

IV. The experimental procedure for making the device will be that of having a standard
    process then making variations to either lessen or accentuate the drift characteristics.
    A. Standard Process
      1. Resistivity
      2. Cleaning wafers, (TCE, acetone, H₂O igepal)
      3. Chemical polish (CP-6)
      4. Special cleaning prior to oxidation (Formic acid - H₂O₂)
      5. Outdiffusion (T=1250, dry O₂)
      6. 1st mask
      7. Clean wafers
      8. Isolation predep (T=1200, Boron)
      9. 2:1 HF dip
     10. Isolation diffusion (dry O₂)
     11. 2nd mask
     12. Clean wafers
     13. Contact predep (T=805 Phosphorous)
     14. Clean wafers
     15. Ni plate and Getter (T=1100, dry Ar, O₂)
     16. 3rd mask or contact oxide remove (quench control)
     17. Clean wafers, 2:1 HF just prior to
     18. Metal evaporation (Aluminum, double 60 mg, on glass slides, outgas)
     19. 4th mask
     20. Clean wafers
21. Metal alloy (T=580°, dry N₂)
22. Back lap
23. Dice
24. Mount, bond, lead weld (Au-Si, 1 mil Al-Si wire, thermo compression)
25. Bak out (dry N₂)
26. Can (dry N₂)

B. Run 1. Purpose - Effect of ultra clean techniques, introduction of as little OH ions as possible.
   1. Use standard process

Run 2. Purpose - Effect of oxide grown with steam
   1. Standard process - substitute steam O₂ for dry O₂ at steps 5, 10

Run 3. Purpose - Effect of Phosphorous
   1. Omit contact predept, steps 12, 13, 14

Run 4. Purpose: Agglomeration of Ni at interface?
   1. Step 15. Ni plate, getter and quench from 1100°C
   2. Step 15. No nickel, slow pull in dry As, O₂

Run 5. Purpose: Effect of gold
   1. Diffuse in Au prior to beginning standard process
   2. Diffuse in Au instead of Ni getter step 15

Run 6. Purpose: Effect of regrown, supposedly uncontaminated, oxide and variation of oxide thickness
   1. Remove oxide and regrow prior to step 15. Ni plate and getter.

V. EVALUATION

A. Select 20 good dice with scope
   1. Measure BV₆₆, I₀, oxide gate unshorted

B. Mount the 20 selected dice
   1. Measure BV₆₆, I₀, V₉₈, V₁₀₉, V₈₆, I₆₆ at 10 volts

C. Bake out and can as in IV, A, 25-26
   1. Measure BV₆₆, I₀, V₉₈, V₁₀₉, I₆₆ at 10 volts, G (of oxide gate) at 0 volts
   2. Select four typical units and plot on x-y recorder I₀ vs V₀, V₉₈

D. Preliminary age the four selected units for approximately 16 hours (overnight)
   1. Conditions: V₀ = const, V₉₈ = const, T = const
   2. Plot I₀ vs time
   3. Store with all leads shorted

E. Select one device from the four. After having accumulated four devices (representing four different runs), plot the following:
1. $I_{SD}$ vs time at $T = -50^\circ C, +50^\circ C, +100^\circ C$
   $V_{SD}$ = const, $V_G$ = const
2. $I_{SD}$ vs time at different fields
   $V_{SD}$ = const, $T$ = const

VI. Schedule of time for device fabrication and evaluation

<table>
<thead>
<tr>
<th></th>
<th>RUN</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4A</th>
<th>4B</th>
<th>5A</th>
<th>5B</th>
<th>6A</th>
<th>6B</th>
</tr>
</thead>
<tbody>
<tr>
<td>A. Fabrication</td>
<td>Start</td>
<td>8-21</td>
<td>8-22</td>
<td>8-22</td>
<td>8-23</td>
<td>8-23</td>
<td>8-27</td>
<td>8-27</td>
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<tr>
<td></td>
<td>Finish</td>
<td>9-5</td>
<td>9-5</td>
<td>9-5</td>
<td>9-5</td>
<td>9-12</td>
<td>9-12</td>
<td>9-13</td>
<td>9-13</td>
<td></td>
</tr>
<tr>
<td>B. Selection of devices V - A, B, C, D</td>
<td>Start</td>
<td>9-6</td>
<td>9-7</td>
<td>9-10</td>
<td>9-11</td>
<td>9-12</td>
<td>9-13</td>
<td>9-14</td>
<td>9-17</td>
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<tr>
<td></td>
<td>Finish</td>
<td>9-10</td>
<td>9-11</td>
<td>9-12</td>
<td>9-13</td>
<td>9-17</td>
<td>9-18</td>
<td>9-19</td>
<td>9-20</td>
<td>9-21</td>
</tr>
<tr>
<td>C. Age</td>
<td>Start</td>
<td>9-17</td>
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<td>9-17</td>
<td>10-5</td>
<td>10-5</td>
<td>10-5</td>
<td>10-5</td>
<td>10-5</td>
<td>10-5</td>
</tr>
</tbody>
</table>

* Assumes only one Varian recorder for data taking
Otto has said that a similar structure with the reaction \( V-1 \) diffusion that did not change at 1500°C and above.

The diffusion by having a separate oxide cut out is then a dip.

He said, "It will be tried."

A series of 6 runs were set up:

Structure:

![Diagram of a structure with scale 1" = 1.00 mm]

### Results

**10 V Vcd, both gates grounded, to stabilize.**

Then put -4 V on each gate. Junction gate grounded.

- **Init**
- **50 s**

The model fits:

\[ I_s - I_{os} = A e^{-t\tau_2} + B e^{-t\tau_1} \]

On one device stated in detail, \( \tau_2 < \tau_1 \)

The magnitude of \( I_s - I_{os} \) is strongly temperature-dependent.
11/20/62 - Review of ORNL's nickel resonator, signed the date of 1/21.

Dave Talbert: Review of our data

80 runs of 4 before and - air @ 150°C most of time
180°C 1/3 part of the time

- The process:
  1. filament 0.1 microns wide, chips
     thickness = 1 min. [untitled 0 x 10⁻⁶ \text{ mm}]

  Method: laser burn to melting @ 200°C + air

  Use the nickel testable.

  Monitor near 1/2 x 1/4" are on a similar substrate strip,

  60 mm used Al contacts, but get reversibly

  laser treated Al and Au-Al u no apparent improvement.

  Monitor can be stopped at the desired value. 

  KMER marked and sticked (electric)

  The liquid is poured

  into the tube and the metal

  sticked at the interface.

  When the Al surfer (not Alumina) is not followed by Al metal stick (NiAl)

  KM removed by heat with a furnace (130°C). This is an undesirable step containing

  salt oxides in the pool. This appears to be

  heat treated for 5 min at 580°C. (Al, Al alloy)

  Resistance increase ~ 4-5% immediately upon exposure to air.

  Can use a paper with heat procedure to date, 68 period

  Color, etc.

  64

  5.1

  5.0

  0 across one row

  Pip in center is typical, but not always, April 53-62 or

  one roof.
This is to advise the status of the above subject as of 11/14/62.

Jack Smith, Elmer Biegel, and I had a meeting on this day with the intent to finalize our position, formulate a sales plan which we could follow and propose to IBM and--generally--get some decisions made by both companies before the end of this month. The intent was to get Harold Rudder in Poughkeepsie on the phone with all of us, after checking several points internally, to get a commitment from IBM which could enable us to make some plans.

Previous to the call we decided prices, answers to their questions regarding specs, the position we would take regarding delivery rate, and what test results we could show them in a few weeks. Unfortunately, Harold Rudder went home ill that day and we were unable to get the decision. Hence the reason for this memo to you requesting follow-up in my absence.

Charlie Sporck verified that we could build up to a production rate of 1,000 per week with 90 day lead time and that 250 on the first order should be no problem, because R & D has many wafers going through right now. Charlie got this from Phil Fergus.

Elmer Biegel has the specifications we can agree to over and above those which were initially provided IBM (maximum temperature permissible, maximum dissipation, etc.). Approximately 50 devices are presently being placed back on life test (were observed after two or three days) to observe the long term stability with temperature and power. These test results will be promised to IBM by Jack Smith as a wedge to get them to commit a purchase order.

Jack Smith will take it upon himself to get the order to us as soon as he goes back to Poughkeepsie.

As of today it has not been determined where this device will be produced, but Charlie Sporck will make that decision when necessary. Some equipment is necessary in whatever plant is chosen to produce these devices in volume and this will have to be decided.

It is our intention to get an order for at least 100 pieces (hopefully 200 to 250 pieces) out of them for the initial purchase. It is Jack Smith's opinion that this is probably the largest volume semiconductor we can hope to sell IBM in the next year or two and represents the largest dollar potential. Jack bases his opinion on the fact that he lived through the Texas Instruments’ fiasco on the 1N2175 with which
IBM Card Reader Phototransistor (XFT-3)

IBM was never satisfied, but continued to buy in spite of themselves. They need a good card reader desperately, and Jack is quite optimistic that ours will be the best thing they can buy--resulting in orders for hundreds of thousands.

It is doubtful that we will see orders for more than 100,000 during 1963 which would sell for about $2.00 each. Eventually these will have to get well under $1.00 in very large quantities, but we made the initial quote (see IBM file) high to maintain a negotiating level from which to bargain.

Regards,

M. H. Phelps

MHP: JG
All units were looked at and canned.
A few failed.

Aiming at 10K, ran 5-10K except for a few units. Ran on 10 samples in ~24h in one run.
The area all process capability with 1mil thin look like ±30%
Fine-mesh measurements look like only 20ppm to 4% to wide.
Early results seem very promising. Looks like much higher resistance film?

Stability:

<table>
<thead>
<tr>
<th>T (°C)</th>
<th>t (h)</th>
<th># (in)</th>
<th>h (in)</th>
<th>break</th>
<th>years</th>
</tr>
</thead>
<tbody>
<tr>
<td>500</td>
<td>25</td>
<td>500</td>
<td>10</td>
<td>7</td>
<td>3/fail in 1y</td>
</tr>
<tr>
<td>500</td>
<td>10</td>
<td>500</td>
<td>10</td>
<td>9</td>
<td>1/fail in 1y</td>
</tr>
<tr>
<td>500</td>
<td>100</td>
<td>1000</td>
<td>10</td>
<td>8</td>
<td>1/fail in 1y</td>
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<tr>
<td>500</td>
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<td>250</td>
<td>10</td>
<td>8</td>
<td>2.0+ for 1 year</td>
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<tr>
<td>100</td>
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<td>10</td>
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<td>25</td>
<td>250</td>
<td>10</td>
<td>10</td>
<td>0</td>
</tr>
</tbody>
</table>

All runs failure look like mechanical problem in the film -
debonded, bubble, etc.

Randomly some held up to 3 times look pretty good - non-minted

At 200°, the units shifted much more. At 200°C many at the end of 1000. At 300°C they go up and down all on the map.

All runs found in storage (~10%) were for problem other than moisture.

All runs failures were in the micrones.
The strong " " " " " "

K
Heated substrates resulted in even greater changes during heat treatment. He agreed roughly on strange shifts.

A few samples:

If alloy is at 550°C, one cannot get a non-shrink resistance. For example, at 446°C, 55°C depending upon degree of current.

At 580°C, this is less of a problem after 2 min, but at 550°C, which is comparable to the rest of the cells, this is a problem — until bake-out.

With the mask designed to check catalysis, there is no contact resistance at obtainable levels compared to 150°C — after bake-out.

Problems:

1. Poor life failure mode — must be eliminated.
2. Drift
3. Lack of predictability of the R's from the monitor
4. Spread on wafer.

Dr. Dur. note:

H.R. needs the things for 4 Y amp.

Dr. Elliot plans:

1. Look for cause of flaw.

Bo note:

1. Habitat temp
2. Living in a vacuum.
Dave Tallent will do a little more of "thank" midmorning expected
Epitaph meeting, 11/20/62  
(Reference, 11/19/62 - book II, p. 144-146)

Still - Body problem with 511Hx.

1st run of 2 pumps has been going fine so far.

Graphite - We are using the correct one.

Hand has a single pump showing that E 50 miles means that
there is a e-c short problem (E 51/40 -> 940 with CP-8).

Surfaces:

We do ~20 wafer at a time in CP-6.

CP-8 would be 5 wafers at a time.

Evaluation of 1341 - We gave the 6 wafers.

Note: The copper runs are not too far off.

Our runs show much greater spread around a 2 hour but
an awful lot more new-to-new spread.

Restriping and surface rejects are way down.

Our stuff from ~ 80% of "stuff" within spec.
<table>
<thead>
<tr>
<th></th>
<th>Present R &amp; D</th>
<th>Present Production</th>
<th>New reactor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silane</td>
<td>distilled SiHCl3 &gt;10.2 cm n-type</td>
<td>impure SiHCl3 variable, high p</td>
<td>Pure Si : Cl4</td>
</tr>
<tr>
<td>Hydrogen</td>
<td>Pd penfined 2ppm H2O</td>
<td>Photoreactor ~50ppm H2O</td>
<td>Pd penfined</td>
</tr>
<tr>
<td>Surface prep.</td>
<td>CP-8</td>
<td>CP-6 + HAC</td>
<td>CP-6 + HAC</td>
</tr>
<tr>
<td>In situ treatment</td>
<td>Pure HCl etch</td>
<td>none</td>
<td>HCl + Si Cl4 etch</td>
</tr>
<tr>
<td>Silane feed</td>
<td>liquid, visible</td>
<td>liquid, visible</td>
<td>H2 activation @ 0°C</td>
</tr>
<tr>
<td>Doping</td>
<td>added to silane</td>
<td>added to silane</td>
<td>From HCl to H2</td>
</tr>
<tr>
<td>Type operation</td>
<td>needle, reduced</td>
<td>dispersed, reduced</td>
<td>needle, etched</td>
</tr>
</tbody>
</table>
Items still to be checked on new reactor:

a) Is the material at least as good as 13.41, 13.21, 50-6?
b) Can it make 7000 material?
c) What is the production spread on thickness and p?
d) How flexible is the machine to change p?
e) What is the effect of substrate doping?
f) Can quartz plates be added without problems?

Items where our present production systems could be improved:

g) Switch to distilled 5:1 HCl from R&D still.
h) Re-install old still at baking level to supply 5:1 HCl.
i) Include provision for vapor etch with straight HCl.
j) Change to volume control or positive pump liquid feed.
k) Substrate wafers to maximize sensitivity spreads.
l) Eliminate handling of wafers with metatogen.
m) Purify hydrogen.
EPITAXIAL PRODUCTION IMPROVEMENT MEETING -

Held: 11-6-62

Summary of Proposals:

1. Begin use of distilled trichlorosilane as soon as system can be fabricated and installed under direction of R&D.

2. Insure use of standard CCT graphite mandril.

3. Determine if present etch used by Materials gives pitting as compared to CP-6 etch.

4. Evaluate results of R&D 1341 runs using their distilled silane and wafers grouped in a resistivity range of 0.0062 - 0.0075 ohm cm.

5. Materials present results of 1341 yield from standard production.


7. Materials present vapor etching data.

8. Materials report on results of using tighter resistivity grouping of antimony substrates.

9. Miscellaneous improvements for production area:

   (a) insure flowmeter control values after flowmeters.

   (b) install coil stabilizers.

   (c) place extra envelopes over mandrils when etching.

   (d) use quartz flasks for distilled silane.
Vapor etching:

Scherzer tried to use SiHCl₃ + HCl. He was able to get some polishing action.

We also showed that some types of and are removed, but that others are not.

HCl etch at a std should be considered.

We have data on evaluation on Al₂, 3, and Al₂.

Scherzer on his new reactor:

Measured SiAl consumption in one day. Et 231. 16/17th.

Capacity = 135 present/hr.

At this rate, one reactor handles all the n type.

Surface:

At 6 - 1/4

Best Mach = 0.0 0.1 stage, pit free except for.
Metalization protection - Page for Meting.

M.D. SiO an extra layer for FeF on life test as cured at 70-75°C.

- Use Al for mask against SiO etch
- 100 parts HN03, 35 parts HF
- KPF - cold again on lids

This represents two additional masking steps and two preparations.

50 gates @ 125°C - no problem yet

Tried to do the etch with a single chamber masking.

Etch with HF, NH4F, HAc + H2O + HNO3 + H2O2

Units were evaporated thru a mask. No problems related to that monoxide have been found.

Glass:

Spray pyroceram with an acetone than a metal mask.

Very thin ~ 0.1 mil - very hard.

Identify @ ~450°C in N2.

Problems:

10 flow out of the glass into paste existing.

Schedule on exp. thru month:

Decide today on mask to cover glass with pyroceram.

Run low next week

After this by next week after next.
A possible real improvement to the existing spec is possible
with sparsity. As I have already mentioned, this could even be done
without changing the balance point. This does, however, mean making
minimum use of the sparsity.

On next week's list to perform due to prior
S-alarm agent.

**New Family**

| 10 cm  | 3 mm w-stiff |

Objectives (in order of importance):  

1. \(< 10.5\)  
2. \(< 5.5\)  
3. \(> 200\) m w worst case  
4. \(-55^\circ C < T_a < 125^\circ C\)  
5. \(F_0 = F/I_0 = 5\)

Design acceptance tolerances:

| \(R\) (2 mil) | \(+20\)%  
| \(R\) (1 mil) | \(+35\)%  
| R melting | \(+5\)%  
| R temp rise | \(+2\)%

Mask tolerances:

- Metal strip: 1 mil min
  - 0.25 mil @ any point for \(h < 3\) mil
  - 1 mil @ any point if not critical
  - 0.5 mil @ any point for length > 2 mil
  - 1.0 mil from selective cut to active area
  - 0.25 mil cut position
  - Full 1 mil align on theme

### Circuit possibilities

1. **NOR adding**
2. **NAND**
Seeks circuit possibilities: (Inverted MECL)

This does everything that MECL does, only at lower power.

This looks like @ ~5 mW on-site, 10 mW late, 40 mW worst case or later.

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0+12V
10 units were presented to data on them.

Then were all the PTA (large geometry) type.

Units look good except for 0-shift. This is an order of magnitude too high.

Sensitivity is repeatable 255 mv/100

Zero - 0.38 F.S + 0.09% (range 10)

Heptane: 0.01 heating < 0.170

Normal heptane 1st cycle - 0.35 F + 1.02 @ 270° (5 minutes)

- 0.11 F + 0.97 @ 250° (5 min)

3rd
- 0.06 & 56 from 270°
- 0.09 & 100% for 150° unit

Zero shift - 0.05 F to 270°, but not linear.

The PTA gage, still needs some checkling to balance the bridge.

New models using new technique will be made.

Problems:
1. High temp joint between Si diaphragm & block
   a) High temp epoxy - not will leave in a couple of weeks.
   b) Electron beam welding.
   c) Glass has not worked well - an engineering off problem.

N.P. thinks that this is not serious. We will assume that if
nothing unusual is done that the high temp epoxy works.

2. Need data on shake, rattle & roll
   a) Vibrator, 1g or 2g, and no free < 20 kec?
   b) Mechanical shock
   c) Thermal shock

3. Life test
   a) High Temp, high P 150% P & full T
   b) Equipment
   c) Pressure cycling
   d) Life cycling
The P2B nodes are sending for a pilot run.
There is the possibility of a hot (wipe out under) flash bộtrgen.
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**Remarks:** Epitaxial N

**Type:** Channel

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*TO-5 standard*
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<td>64</td>
<td>3.0</td>
<td>310</td>
<td>4.1</td>
<td>1.4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>1</td>
<td>64</td>
<td>3.0</td>
<td>310</td>
<td>4.1</td>
<td>1.4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>1</td>
<td>64</td>
<td>3.0</td>
<td>310</td>
<td>4.1</td>
<td>1.4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>1</td>
<td>64</td>
<td>3.0</td>
<td>310</td>
<td>4.1</td>
<td>1.4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>1</td>
<td>64</td>
<td>3.0</td>
<td>310</td>
<td>4.1</td>
<td>1.4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>1</td>
<td>64</td>
<td>3.0</td>
<td>310</td>
<td>4.1</td>
<td>1.4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>1</td>
<td>64</td>
<td>3.0</td>
<td>310</td>
<td>4.1</td>
<td>1.4</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**
- No unit numbers provided.
- All data entries are in milliamps ($mA$) and volts ($V$).
- $B_{105}$, $I_{05}$, $g_m$, $V_{E10V}$, $R_{N}$, $I_{05}$, and $V_{D5=5V}$ are all in milliamperes ($mA$) and volts ($V$).

**Remarks:**
- EPITAXIALS
- FAIRCHILD SEMICONDUCTOR CORPORATION
- TAKEN BY: B. Worley
- EQUIPMENT: [Signature]
- REQUESTED BY: P. Parringer
- FORM 5757A Rev. 5.60
FET Wing to review spurious 11/27/62

Status:

Material: cal. 6

\[ P = 1.5 \, \text{cm} \]

\[ t = 3 \mu (2.5 - 3.2) \text{ by gram count} \]

Substrate: 0.2 - 0.3 \, \text{cm}

V1 variation of 20\% on a wafer 50\% around a row

There is only 4 rows - and one of these is only 2 rows.


take 1 row as control for V1 and powers adjusted for the bias under the assumption that while constant in thickness rather than doping.

Status of wafer (from observed material)

<table>
<thead>
<tr>
<th>FET</th>
<th>1</th>
<th>1st dig then</th>
<th>post of digit</th>
<th>- all from one epitaxial run</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/80</td>
<td>2</td>
<td>1st dig Cleat</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>1/35</td>
<td>3</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>1/40</td>
<td>4</td>
<td>T.C. in both lap</td>
<td>1st dig then cleat by 1/40</td>
<td></td>
</tr>
<tr>
<td>1/50</td>
<td>5</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>1/60</td>
<td>6</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>1/75</td>
<td>7</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>1/80</td>
<td>8</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

Test noted:

<table>
<thead>
<tr>
<th>9</th>
<th>2nd mark</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>2nd mark</td>
</tr>
<tr>
<td>11</td>
<td>2nd mark</td>
</tr>
</tbody>
</table>

These were dipped.

Other by feelers were 0 - 2\%, a similar process.

23 wafers were all from one test chip.

Life test data:

ashed at 200\% C. After 10 minutes at 420
had 150 qu. up from -5 to -100. - But that's open hand out over the weekend.

Lenz's data:

no failure in 60 hr at 100\% by oxidation an
after minute.
Material:

Your ~100 good copies during the next week
New reactor, Sterling Rd. ~300 mW, ~5 copies from each run to be held as backup, remove 3 to do during next couple of weeks.
Make one or regular reactor on Metro View.

Summary:

Get + to do work at 9:00 to get run at a schedule
For Rene after ~100 representatives will ASAP to get test.
ROBE Meeting 11/27/62

Light density: 4200 mm = 5/5 mm²
Small quantity in mask area (~ 25)
UL mask = 50-60 / 55 mm² on regular stuff
some of the, #2s, #5s, #7s, #9s on ~ 10.
(Small area in #6s, #8s, #10, and #12 areas)

Chrome mask: being played up on 4200 because of potential problems
with scalloped edges.
Some #1250's made is #1150 in #1150 had fall low density.
Examining them showed no special concordance with making
accidents, but a whole long of study problems.

Methyl Brute: RD is seeing it on polarization yet.

Chrome mark stability - Kevin

A separation of ~ 3 mile between chrome mask and edge gave a very
very fine edge.
Someone that one of the can be gotten with photographic mask.

It is true that there is more len of resistance build
the chrome mask than with the emulsion mask.

Suggestion
1. Not sure optimal for results of whole content is good. Pro. Dev.
2. Try less #6s, #10s, #7s, #12s, #13s
3. Debates plan altitude
4. Later

It is suggested that this problem might be a multiple reflection problem.
Paul is laying out experiments to look at last time's pipe problem.

A buffer after pledge, before diffusion was cut in half. Dyes were checked before and after. (200 ml and)

<table>
<thead>
<tr>
<th>Substrate</th>
<th>Before</th>
<th>After</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total</td>
<td>50</td>
<td>51</td>
</tr>
<tr>
<td>Pipe</td>
<td>14</td>
<td>25</td>
</tr>
<tr>
<td>non-BC</td>
<td>5</td>
<td>12</td>
</tr>
<tr>
<td>in enzyme</td>
<td>11</td>
<td></td>
</tr>
</tbody>
</table>

Mr. Sany concluded that this is a significant source of pipe.

Next meeting on Monday afternoon - 2:00
Section Meeting: 11/28/62

Chrom masks

Equipment: An etch jig plate holder

Need ~ 28 in of 2 type

Ren ~ 2000

Jig getting outside

Quantitative study of pin hole.

A large quantity of plates must be checked.

We will make a diligent count of pinholes and correct as indicated.

Chrom mask making is in pilot line room 3 there room.

Mask making.

Need stopping with replacement.

Accuracy on machine is better going from 1 to 0 with 0 to 1.

Can get a total spread of - feet & 1/2 type. It is also faster than

Can do 4/min better than 5.5/min. This accounts for the result of faulty

mask Saddles.

The mask will be made outside.

The model.
Section Meeting: 11/28/62

Chrome mask
Equipment Mark Engraving
etch pattern
Etch Etch

Chrome mask:
Equipment: An etch jig plate holder
Needed 28 ea 0.2 type - Rein 17 - Jig plating 1 unit

Quantitative plots of pin hole:
A large quantity of plates must be checked.

We will make a testing plate, of pin holes and continue to deduce the individual.

Chrome mask making is in pilot line room. There is not

Mask making:
Needed spring with replacement. Accuracy on machine is better going from 1 to 0, with 0 to 1.
Can get a total speed of 5 feet of 12 laps. It is also fast, thinning,
Can do 20/min rather than slow 5.5/min. This capacity is used where panels are required.

The machine will be used next week.

Engel
Meeting: 11/28/62

Chrome masks:
Equipment: Ana etch jugs, plate holder.

- Need 28 sets of 2 jugs.
- Iron Solder - jugs getting spots.

Quantitative study of plating.
- A large quantity of plates must be checked.

Chrome mask making in pill fire room. There is room.

Mask making:
- Need sporting mask replacement.

Accuracy on machine is better going from 1 to 0 with 0 → 1.
Can get a little spread if go to 0.5 or 1.
Can do 7/10 min rather than 5.5/10 min. This accounts in the result offully

The new stop will be ready next week.

The manual Solar camera is out of scale. It must be re-zeroed.

We should see if we can get out of bread. Also a column in 10 mil.

Engage on pinholes:
Work to start line.
Expriement to evaluate diffusin content of substance "into film"

Take grown film - bed for exam to

If these follow PDT, then a D in good number

Film thickness:

We have several techniqns

Regal - Mr.
Dick
Steve
E.
Profile duration from flat

The wide polished surface will do the job. It will be done.

Reference on Conc.

Before Peter goes on vacation we want to answer the question:

To be the diffusin content in the film higher than in
the substrate as film grown at an low a tempere?

at the regular growth temp?
scale emits follows:

\[ \beta \text{ distribution: } \left[ 0^\circ \text{ to } 5^\circ \right] \]

\[ \beta \text{ distribution: } \left[ 60^\circ \text{ to } 90^\circ \right] \]

\[ \text{max } (120^\circ) \]

Questions?

- Can yield on beam?
- What if S - planet?
- Yields?
- He uses 70 mil clip (m 75 mm)
- Old yield?

Essentially all the logic done on all can be done with these.

\[ 17 \text{ mil at } -55^\circ \text{C} \]
\[ 24 \text{ mil at } 125^\circ \text{C} \]

- Consideration:
  - Cut beam or DCTL and influence of family
  - Change in logic.
  - Problem of coping a C to an S - untested.
  - Overdriving or - underdriving.
  - Mismatch in logic.
  - People using parallel gates are in trouble.

Third point is the bond to G element. Another need:

- S clip page
- 50% yield up bond to G element.人人 need

A second run is in the mill. We didn't know about it, but it will not be thin in the next few days.

This does not preclude a direct set-up. If we were making a new family, it would build their good yields and 100%.
Furnish an optical chart.

For paper gaskets, a light bake brought out
in T121, optical. All high-β devices

1. GYgata = optical window; +10°C 6/1 or an array
   get 90°F, 50°C, 20 mm Hg @ 125
   0 mm Hg @ 55.
   Est 775°C yield to a peak, and B's for 30-40 in.
   10 mm, 19 mm tip
   1

2. Slag at 575°C, grid selection, take yield to 65% done.

3. Optical in T1-1 Kelt 575°C in belt Re (a)

Did some reporting upon some the apparent low temperature Arrhenius that looked
like T = 0. There is no formation of the advantage at these out.

Possible paths

0 -+ d

0 -+ b -+ d

0 -+ a -+ c -+ d

0 -+ e -+ e'

O in present

a is mm epi GY Kelt, 85°C R - Re, 1.0 = 450
b " " " " " 575 55

C " epi T -1 250 P

D " " " 575
Review 7-transit:

& VCE $51 \text{ res }

GY
e

Only 1 unit of the test vehicle had all four testors, look-up after assembly. On this one -- the 3 can better than 6 Y or VCE.

<table>
<thead>
<tr>
<th>VCE</th>
<th>51</th>
</tr>
</thead>
<tbody>
<tr>
<td>21</td>
<td>175</td>
</tr>
<tr>
<td>22</td>
<td>190</td>
</tr>
<tr>
<td>6Y1</td>
<td>200</td>
</tr>
<tr>
<td>6Y2</td>
<td>225</td>
</tr>
</tbody>
</table>

Of 11, 6 Y1/2, range 170-230 mm
Of 6 7/2, range 175-220 mm

The Z's, as expected had less noise. There were no extremes.

GY Xsre - go go for std echo.

New family:

The charters looked rough. 35 10,5 5.5, 200 may be end of the question.

5 mm, 10 mm, 50th look possible, but again different.
P.F. — Raindown on line pipe work — up to lose diffusion.

Lockleys @ Schudy believe there is an atmospheric contamination. He thinks they are a diffusion phenomenon.

1. If not a diffusion layer and starting at same time as get a cylindrical pipe, $C_s > C_s, T_{pf} > T_{pf}$
2. If $T_{pf} > T_{pf}$, $C_s > C_s$, get an ellipsoid.
3. If $T_{pf} > T_{pf}$, $C_s < C_s$, get

Points, experimental are numbered:

1. The incidence of pipe is in a function of bulk doping. It gets large with increasing bulk doping. The observation is based on many studied runs, no split runs.
   But long points out that 4265 to more than 1000, he found.
   P.F. will either find data on a split run. Either old, or he will re-do.

2. In every case (n20 pipe) the electron probe has shown $P_e$ lower up to 1000 ppm.

3. The silicon concentration does not seem to drop more than a few percent at most. (Perhaps suscubad that they do not represent a separate phase.) On some recent samples it looks more like 10%.

4. Many of the pipes show a pink fluorescence. U/C feels that this is about certainly a glass layer.

Typical light emission on breakdown.

P: --- Blue fluorescence

5. Approximately half of the pipe have shown being not able — Ca, Zn, Fe, Ni.

6. Deviate spots of metal exist on the surface of the wire. Very patchy, but it does not necessarily associate with pipes.

7. In the metal Fe.Ni. carbide and Ca+Zn associate.

8. The metal are being found on steel surfaces.
To: D. Yost
R. Fouquet
N. Walker
R. Robinson
S. Fok (R&D)

From: Paul Hill

Subject: Minutes - Chrome Masks 4200, November 23 Meeting on Resuming Chrome Mask Usage.

Subject of Meeting: Re-instating 4200 use of chrome masking in production.

1) Major objection to current usage:
   a) Oxide cutout resolution is poorer than those obtained from emulsion masks (see exhibit I).
   b) The effects of pattern resolution as in exhibit I may have significant parameter shifts as yet unknown.
   c) A production classification yield loss is possible due to irregular oxide cut-out patterns.
   d) Belief that irregular edges tended to increase KPR lifting during aluminum etching.

2) Approach the chrome mask implementation:
   a) Run no more chrome masks until classification yields of chrome mask vs. emulsion mask units have been evaluated.
   b) On the basis of Process Development work showing degree of irregular oxide cut-out patterns is a matter of degree to which mask image and wafer contact is made, run no more chrome masks until the contact problem is solved (mechanical masking). See exhibit II.

3) Required:
   a) Pressure pad for wafer on mechanical alignment (N. Walker).
   b) Classification results on 3000 wafers processed on 4200 line with chrome masks, (R. Fouquet).
   c) Test on degree of scallop edges vs. parameter change or degradation (R. Robinson).
   d) De-bug pressure pad mechanical masking device of item (a) and equip 4200 masking stations with the device.

4) On 4500 devices the same requirements are assumed to also apply.
KEY TO EXHIBITS

EXHIBIT I - Oxide Cut-Out Resolution at 500x

<table>
<thead>
<tr>
<th>Fig. No.</th>
<th>Subject</th>
</tr>
</thead>
<tbody>
<tr>
<td>61</td>
<td>4200 Base pattern using emulsion mask</td>
</tr>
<tr>
<td>62</td>
<td>4200 Base pattern using chromium mask</td>
</tr>
<tr>
<td>63</td>
<td>4200 Emitter pattern using emulsion mask</td>
</tr>
<tr>
<td>64</td>
<td>4200 Emitter pattern using chromium mask</td>
</tr>
</tbody>
</table>

EXHIBIT II - 1340, 4th Mask Pattern at 200x

<table>
<thead>
<tr>
<th>Fig. No.</th>
<th>Subject</th>
</tr>
</thead>
<tbody>
<tr>
<td>33</td>
<td>1340 Chromium Mask</td>
</tr>
<tr>
<td>34</td>
<td>Oxide etched wafer showing progressively</td>
</tr>
<tr>
<td>35</td>
<td>Poorer edge definition from the left (Fig. 34)</td>
</tr>
<tr>
<td>36</td>
<td>To the right (Fig. 36) edge of a warped wafer</td>
</tr>
</tbody>
</table>
9. Edge dedication do not complete with pipe.

10. We can now develop the small circular dedication pipe in all 1-sided safer (on then). This has been seen in un-sided safer.

Phil thinks there are important in pipes.

11. Pipe are made by putting screen salt on 1.00 to 10.00 R.-m. Any $10.2$ cm got pipe? This are put on c atomica. Can tell c spoke

now shown.

Program:

1. Take 5 samples at all stages for 2 electron probe.
2. Take 5 loops in Core length melt superfluous.
3. Surface contamination studies

12. Pipe manually have wind createState. State last show pipe.

Lang program

1. Split between first pipe or process.
2. Project medium:

- Weak area are speed again 1 with edged to beam doping.

Special: Image to void observation sharp and edged edge and compact density.

2. Mark beam exit to label c state edge.

3. Stop and re-join

3. He Ni plotting edge at (es impert? )

- Corrected Ni.

4. Putting during bore degenerative

- Make half pitch core to compare.

5. Meet again in 5 weeks 1 day - Jan 8.
Thin film matrix for jet int

Resolution on 100 - 200 R / C

Candidates:
1. Nickel
2. Cr-SiO ceramic
3. Aluminum (planning data not available)
4. Ta - we know nothing at present

Nickel:
No 300°C substrates seem to cause problems.

2. Most like on foil. Shoot here
   a) density control from ambient target.
   b) Microstructure of film.
   c) Fraunhofer contrast.
   d) Substrate contrast?

Cr-SiO - ceramic:

We have used 2 sources and electric beam heating. R/10: 500-20000 Hz

But unexpectedly:
Eutonic on Cr-Co or can be done with Al negative.
F.C. ~ 200-250 ppm @ 5% R.
Old substrate temp. Al phase change by 50°C

The only possibility to (that I can see) to get thin working is to
got into the monitored system.
Prepared program.

Get to a reliable film also 4.5 variance predicted to within 1%. 

1. High substrate temp.
2. Controlled oxygen ambient during cap

Check those out this week. After that we will get the rest checked out.

Hoping Zippy has done one ½ mil winter + H2O (2L) + boc
12-9010 or 9-1790
10-9010 or 12-790
Dec 4, 1962 - Fortin Refueling Meeting

New reactor evaluation:

First 1311 evaluated at 33% cure, 66% cure, 3 thought to be within range - they are.

The evaluation at suggests conductivity refers you like

Summary:
1321 - 1311 being done

From now on, they will run ~10%/w on the new reactor. Dick Cole feels that by the end of December, a majority of the N+H material will be run on the new machine.

Scholten says that 0.2% difference in I0 between 1321 and 1311.

1341 line might accept 10% next week.

It looks like we are evolving into this system rapidly. Change will be exhilarating.

Curt System:
running 50% out of 53.7% material
58-59% on m-4pro
the 1313 material made the other high

20 p-p is a problem, still a 30° spread of T.
My agenda for today.

Last time everything hinged on the new reactor evaluation and estimates of time necessary to switch & after decision to switch.

A. 1st discussion - Evaluation of new reactor system
   a) % of run
   b) type
   c) results then evaluation
   d) device

2nd discussion of further evaluation required?

3rd date for decision concerning switch

4th time scale for switch after past du decision

B. Discussion of advisability of making changes in the existing systems in view of A above

1st present status
   a) overall yield
   b) targetability
   c) e.g.

2nd possible changes to consider
   a) still installation
   b) HCl vapor etch
   c) silicon feed system
   d) new reactor flange system
   e) better temp distribution
Need ~100 pieces of 3 different circuits.

Package: flat

Conclusions:

If this is the latest jet of thing and type likely to be around in the next 1-2 months, we shall have to get in touch with the relevant departments.

Let's think more about this, etc., etc.
34 Epitaxial project review  Rev. 12/5/62

Frank on problem:

Surface preparation:

tin nit HCl etching continue give unacceptable.
Our Cr-8 etch seem to be as good as any.

Thin nit steel is being studied as variables. (tonic is doing)
2. rate of removal 5% HCl and HCl flows.
A powerful technique to plotgraph defects is now available.

1. Evaluation

Thickness methods being compared,
Sb doping: the technique is working. We have no data on that is consistent.

Die down substrate affects on profile of n-type films.

1. On bar high 0,60 on high P
2. Sb doped substrate, Sb purity approximately 0.006, 0.05
3. As 0.006, 0.05
4. P " " " maybe?

Film contraction - the good idea.

3. System:
4. " High 0,60 or liquid feed:
5. " High 0,60 result, not advantage at present

4. Equipment:
We want to end up with

1. D.D. with their own seats

2. Facility for

   a) Restroom/amenities block
   b) Food shelter
   c) Agent shelter
   d) Other

+ Other materials

build in Lewis.

Nov.

a) Put service at present #2 RF to #3 with new water
b) Order W.C. tester for installation in #3 (60 days)
c) Get quoted to clean up the #2 portion to this need
d) Training to run in #2

Dec.

a) Finish NF for a RF ground level
b) Get either people!


Out 30 days

a) Consider adding two more W.C. testers, one for
   #2, #4, one for service, etc.
Surface study at metal-semiconductor interface under very selective conditions (often etched).
A single crystal of Si was cleaved in the vacuum system while Au was being evaporated. Thus an atomically clean Au-Si contact was achieved. The thickness of the Au film evaporated was ~ 330 Å as monitored by the resistance monitor. Using a concentrated solution of black wax in T.C.E. in a syringe, small dots of black wax were put on the Au film without touching or scratching it. Au film outside the dots was etched away, thus obtaining islands of Au on Si. Capacitance as a function of bias was measured and diffusion voltage was determined. This is plotted in Fig. 1 (which is similar to Atalla's plot) if we use the ordinate \( (\Phi_M - \Phi_{Si}) \) on the right, and if we use the ordinate on the left, we get a plot of diffusion voltage versus the Fermi level in Si as suggested by Sah. The 45° straight line corresponds to zero charge in surface states, i.e., \( Q_{ss} = 0 \). For n-type Si without the oxide, we will have Au on surface and \( Q_{ss} < 0 \). Thus, the diffusion voltage \( V_o \) given by

\[
V_o = \Phi - (\Phi_F + \Phi_p) + \frac{2\pi N_D k^2}{K_s} - \frac{4\pi Q_{ss}}{K_s}
\]

will be larger for Au-Si (cleaved-not oxidized) case than for Au-Si (oxidized) case. To verify this, the other half of the cleaved Si crystal was oxidized in room air for ~ 72 hours (left over the week-end). A Au film, again ~ 330 Å thick, was evaporated on the cleaved-oxidized Si surface and the above procedure repeated. The diffusion voltage obtained for this case is plotted in Fig. 1 which is found to be less than that obtained for the cleaved-not oxidized Si surface.

On p-type Si without oxide, we should have Au\(^+\) on surface and \( Q_{ss} > 0 \). Thus the diffusion voltage \( V_o \) for Au-p Si (cleaved-not oxidized) case should be less than for Au-p Si (oxidized) case. A p-type Si crystal is being obtained in the proper shape to do this part of the experiment.
The above measurements were also done on photoresisted Si surface, which was previously oxidized. The diffusion voltage obtained is plotted in Fig. 1. Also plotted in Fig. 1 is the diffusion voltage for samples obtained by displacement plating of gold on "N" type silicon by the technique previously reported by Bittmann. Gold ions are added to the oxide etch in this process. The gold displaces Si atoms as the oxide is etched off the Si surface.

The Spectral photoresponse of the various units was determined with Rudy Dyck's help using his experimental setup. The general behavior of the Response per incident photon versus $\lambda$ (in $\mu$) curve is similar to that published by Crowell et. al (Phys. Rev. 127, 2006 (1962)). Response measurements done by Crowell et. al and by us are in arbitrary units and not absolute. A plot of square root of response per incident photon versus photon energy (in ev) would yield the threshold energy for the Au-Si barrier. Crowell et. al find a value of 0.795 for the Au-Si (cleaved) case from a set of curves for different Au thicknesses whereas our value comes out to be about 1 ev as determined from data on one Au film thickness, i.e., 330 Å. Data for other Au film thicknesses will be obtained soon from which the mean free path for "hot" electrons in the Au film can be estimated.

The cleaving jig developed some trouble recently crushing rather than cleaving the Si crystals. It has been re-designed.

II. METAL BASE TRANSISTOR

A. Schottky Emitter

Schottky emission from Si-Au junction or In-CdS junction will be used for emitter. CdS has been obtained which will be evaporated on the metallized glass slides at first and diode characteristics will be studied. Tungsten boats are being coated with $\text{Al}_2\text{O}_3$ from which CdS will be evaporated (resistance heating). Electron beam evaporation will be done when the gun is installed in the system.
B. Collector

CdS will be used as a collector when Si-Au is used as an emitter and vice-versa for these initial studies.

C. Contact Problems

Since Au lifts off the SiO₂ surface, an annular ring of Al over SiO₂ will be used as a support for Au film and to prevent the lifting of the latter. This method gave an unexpected bump in the I-V plot of Au-Si surface barrier diode as observed sometime ago by us. This bump has not been investigated in detail yet. However, a modified etching procedure is being tried to see whether we still observe the bump or not. This involves oxidation of Si, evaporation of Al on SiO₂ layer and then etching holes through Al and SiO₂ layers simultaneously in one etching step. A run is in process.

III. SCHOTTKY EMITTER DIFFUSED BASE SILICON TRANSISTOR

This idea, first proposed by C. T. Sah, consists of diffusing a very shallow base on which a Schottky emitter is used. A run has been started with the help of Gary Parker in which Au-Si will be used as a Schottky emitter.

IV. ELLIPSOMETER

The table for the ellipsometer arrived minus a few parts. It is understood that, at the time of writing this report, the missing parts plus the right parts in place of wrong ones have arrived and the assembly of the table is under way. Messrs. Rudolph & Sons are supposed to call us any day now when they put the ellipsometer on the plane because we are supposed to go to the airport and pick it up.
$\Phi = 4.70$

$X_{Si} = 4.05$

$\frac{1}{e^2}$ intercept = $V_0$

$= \Phi_M - \Phi_{Si}$

$= \Phi_M (X + V_F) + \frac{2\pi q N_D K S^2}{K_s^2} - \frac{4\pi S Q_{ss}}{K_s}$

$\Phi_M = 4.70$ for Au

0.54 eV

0.35 eV

Cleaved Si

Cleaved-Oxidized Si

Photoresisted Si

Displacement Plating
November 30, 1962

Meer #1 (Platinum - 1 and 1/2)

R. Hoffman

A. Safenn

\[ \sqrt{R} \]

\[ 10 \times 10^{-2} \text{ to the cm. } 359.14 \]

\[ E_{ev} \]

0.7 0.9 1.1 1.3 1.5

1.7 1.9 2.1 2.3 2.5
CLEANED AND OXIDIZED
Au on Si
9-21-62
A. Saxena
C. Bittmann

$V$ (Volts)

$V_0 = 0.98$ volts
MBTC 3 (cleaned - not oxidized)

\[ E_{ev} \]

\[ \sqrt{R} \]
MBTC 3
Au on Si
CLEAVED
(NOT OXIDIZED)

V_D (volts)

\frac{1}{C^2}

V_D = 0.52 volts

Nov. 26, 1962
C. Bittman
A. Saxena.
I. MAGNETIC FILMS

A. $\frac{H_c}{H_k} \sim 1$ is presently not available at $H_c, H_k$ of 5 - 10.

Solutions: (1) adjustment of evaporation parameters
(2) adjustment of impurities in the alloys
(3) substrate surface control.

B. Array uniformity requires improvement.
Solutions: (1) above (1)
(2) above (3)

Requirements: 1 vacuum system (18" bell)
1 experienced engineer or MTS
1 experienced technician.

II. PROTOTYPE DEVELOPMENT

A. Adherence at Ag-SiO$_2$ and SiO-Cu: interfaces are poor and maybe the permalloy - SiO interfaces also.

Solutions: (1) Improvement of technique
(2) Variation of insulators and conductor materials
(3) Variation of etching solutions

B. Pinholes are due to atmospheric dirt, substrate imperfections and SiO splatter.

Solutions: (1) Dust free hood and a good method
(2) Substrate coatings (SiO)
(3) Splatter preventing source for SiO

C. Masking and Etching procedures have to combine mechanical and photoresist masking. Need a KPR remover compatible with copper or use another metal for conductors. Need etching solutions that will not lift the films.

Solutions: (1) Need better etching solutions
(2) Will have to use thicker aluminum films for conductors.

Requirements: 1 Vacuum system (18" bell)
1 Experienced engineer or MTS
2 Experienced technicians.
III. FUNDAMENTALS

A. Magnetic films and switching behavior are not understood.
Solutions: (1) Bitter pattern observation of domains
(2) Correlation of magnetic and metallurgical properties
(3) Correlation of stress and magnetic properties
(4) Sensitive torquemeter measurements
Requirements: Sensitive torquemeter
1 experienced MTS

IV. PRACTICAL SYSTEM AND JIGGING FOR "PILOT LINE" MEMORIES

Requirements: 1 large vacuum system
1 experienced engineer
1 experienced technician
THIN FILM DEPOSITION

The present rate of progress in solving the formidable problems of deposition of film and conductor arrays makes timely completion of a thin film memory as previously proposed unlikely (per memo "Development Plan for a Magnetic Thin Film Memory" to V. H. Grinch dated 8/31/62 by H. A. Perkins). Aside from the delay in acquiring the requisite thin film technology, the effectiveness of circuit and system design is greatly hampered by lack of a memory film array model. The locally available film technology is being reviewed in an attempt to provide a useful interim model of lower storage density which does not require high coercivity magnetic material or a deposited conductor matrix (the most formidable problems at present). The intention is to provide a test vehicle hopefully permitting effective circuit and system work to continue while deposition problems either are solved or the probable eventual limits of our thin film capability are more clearly defined.

Since 30 x 60 spots exhibit some switching on the dynamic tester, and presumably should have $H_C$ compatible with $H_D$, the following program should be pursued for the next few weeks (also mask exists):

1. Lay down Cu-SiO-Cu to finish present experiment until electromagnetic is ready.
2. Lay down Ag-SiO-HiFe (30 x 60) (spots thru mask)
   a. To evaluate spots over ground plane dynamically
   b. To permit making an overlay breadboard so that some approximation of the storage matrix problem is available for circuit and system development.
3. Lay down Ag-SiO-HiFe in continuous films,
   a. Evaluate etched with looper and dynamic tester
   b. Etch 30 x 60, and 10 x 20 spots and re-evaluate
4. Determine means to get $H_C$ as high as we are able with other usable film properties (hopefully > 5 oe).
5. Determine techniques to get rid of pinholes thru oxide so that conductors may be evaporated on assumption that (1) above will disclose such a problem.
6. After (4) and (5) are solved, try to make complete 1x1 spot and conductor array per proposed design.

12/4/62
THIN FILM DEPOSITION

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1. Lay down Cu-SiO-Cu to finish present experiment until electromagnet is ready.
2. Lay down Ag-SiO-NiFe (30 x 60) (spots thru mask)
   a. To evaluate spots over ground plane dynamically
   b. To permit making an overlay breadboard so that some approximation of the storage matrix problem is available for circuit and system development.
3. Lay down Ag-SiO-NiFe in continuous films.
   a. Evaluate unetched with looper and dynamic tester
   b. Etch 30 x 60, and 10 x 20 spots and re-evaluate
4. Determine means to get \( H_C \) as high as we are able with other usable film properties (hopefully > 5 oe).
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6. After (4) and (5) are solved, try to make complete 1x1 spot and conductor array per proposed design.

12/4/62
We are way short handed!

Many problems:

Perlman suggests:
Prot and am at getting large rats to try.

Ned need high He

Boles thinks that aim is count unpurities all now He.
Jay Study: The problem:

1. Adhesion
2. Spinal Ice @ 300°C
3. Popping of spinal during testing - EC problem, some points.jp (50 ± 3 for g)

300°C @ 350 bar

1150 1540 0 failure 15 IECO
96 301
87 112 IECO 2 catalyst 1 IECO
12/17/62, horse foot

Pyramids

I'm a bit confused by the information on the pyramid. There are 2 main pyramid.

1. All 2 pyramid are 15.8 cm. 12

2. 1 pyramid is 6.5 cm. 12

For the purpose of our experiment, both pyramid are 12 cm. In the experiment, the pyramid are

Some of the pyramid have a top area above the pyramid's surface, which indicates a real evidence of preferential diffusion.

The pyramid in the corresponding area are in ratio - 5:1

By etching away, it is evident that the pyramid are followed and shadowed by the substance that completes the

Some preliminary evidence (and some hypothesis) suggest that this is called shadowing because of material shadowing pattern. A 90° angle is on top of a 90°.

Legend is that a △ gets △. Where are seen △ at starting formation, the function A don't intersect at a point.

In order to write with △ on the A plane, we need the total 90°.
December 10, 1962  -  Preliminary

It's a pity we have to... short supply of... 
We are already behind schedule.

New stuff:

High Speed: We have a couple of good possibilities:

1. Instead of our old way of looking at... D, talk about... 10 ns... well, look at... 3 m/s, talk speed.

If the current sense resister will temperature, this has a good chance.

Also 2 resistors... 109

One reference block was obtained. Reference and
using 1312.2

By adding the red line feedback, sharpen the output and help
the swing at scaled conditions.

One can go further.

Be a little bit...
Design Rules

Resistors:

R₁: center-tapped 2 mil wide diffused P-type - 100 Ω
R₂: (a) 1 mil wide diffused P-type - 100 Ω
    (b) N-type epitaxial region
R₃: 2 mil wide diffused P-type - 100 Ω
R₄: 2 mil wide 1500 Ω - tapped for three 500 Ω resistors - diffused P-type - 100 Ω

Idea for a 500 Ω Resistor:

[Diagram of resistor design]

- Contact to be made to the (shaded) N-type epitaxial layer.
- Striped area is isolated.

P-type Substrate

Transistors:

A. 1 square = 0.25 mil

<table>
<thead>
<tr>
<th>Isolated</th>
</tr>
</thead>
<tbody>
<tr>
<td>metal</td>
</tr>
</tbody>
</table>

Type A: Collector - 1 x 3 mil
1/8 mil from base.

Base - 3.75 x 3 mil with 0.75 x 2 mil cutout 1/2 mil from bottom and edges.

Emitter - 1.5 x 2 mil, 1/2 mil from edges, with 1/2 x 1 mil cutout centered.
B.

The type-B transistor is similar to the type-A, the difference being that the emitter and base cutouts are made \( \frac{3}{2} \text{ mil} \) shorter (e.g. \( \frac{3}{2} \times \frac{3}{2} \) & base \( \frac{3}{2} \times \frac{3}{2} \)) so that the entire transistor can be made \( \frac{3}{2} \text{ mil} \) narrower.

In both cases the collector metal need only cover its cutout; the emitter metal should always overlap by \( \frac{3}{4} \text{ mil} \) on all sides; the base metal should overlap \( \frac{3}{4} \text{ mil} \) when possible. Two metal conductors may pass no less than \( 1 \text{ mil} \) from one another except for very short distances when absolutely necessary this may be made \( \frac{3}{4} \text{ mil} \) (e.g. between base contact \& emitter contact).

The isolation region can be brought to \( 1\frac{3}{4} \text{ mil} \) from diffused devices and can be only \( \frac{3}{4} \text{ mil} \) wide.

The diagram shows the probable pad layout for a gate and a flip-flop.
MIL-II HIGH SPEED

3.5 to 7.5 nanoseconds @ 12 mw. - T. = 5570 ± 125 µ sec

@ 3.5 ns - F/0 = 1; @ 7.5 ns - F/0 = 5.

With all solid lines:
3 input gate.
With dotted lines, and
Removing circled
transistor: Flip-Flop.
We should forget & gate off.
Do hand out & a push-off vector to get 35 mV for 25 mV across.

Dec 17, 1962

HSG -
forget to- epistemic logic for resistors can set gate at 50 mV cents.

first of propriety FSC / elite.

1. CML - (G-FF) for alone.
   2) forget the 15th = 12/19
   Machine & finish = 1/14, plot it/make (my mate) ASM
   Date & Dia out = 1/25
   1st two runs made = 17/4 - for these meeting.

2. test vehicle - 2/14 tolerance 0.01 mV, 7/14 mV.
   Note & fact (1/4) 8th priority make 7/4 from the 3/14 completion by 3/11, etc.

3. Reference voltage block for CML - wait for Gates to see voltage.

4. Low power family = 2X3 GATE, BINARY. - chat liquids on Jan 7 &
   go-go-go decision

5. ML-1 R element -
   Maybe title them cut

6. Binary ML selected
   Have chat determined 7/4, rough design 1/4. We will do here common
   as your evaluation move are these.

7. Autentic low power gate (2-3 sim gate)

8. For next time - 1/7/63

   - Ron

10. CML C-made a schedule - Ron

11. Discussion of low power family - Jan + Bob

12. Chat 0 & liquid in by then for ML-1 R element - Jan
Dec 18, 1962  -  Section Meeting

KPR Joint - Don Bean

1. Basic resolution study KOER KPA KNER

2. Small geometry edge definition by one of 6 bill 5. Contribution
   crater, compute results in next few days.

3. Cleaning cycle evaluation of test chamber.

M. He is doing work with a blocked image that is transparent to visible
   and opaque to x-rays.

Mbeku meeting:

S&R shut down at 4pm. Need geometry preference being done.

Sensor settings are not reproducible.

Today check the possibility of setting the control unit to minimize this error.

Try to use Radek bend light to see with the S&R camera.

Manual Camera used to test various parts.

File being cut down.
Jan 15, 1962  - General Meeting

New Items:

Notting some fall out from film appeals to this... bundle... 10 or 14 path.

John Schuster will see the abstracts re I for... 11.

Tea will give more picture of chronin.

CP 66 in CP 8 and... dental pils.

How were will try CP 8.

Next: John will... at surface

\*

For next time:

Then:

Before CP after... Med. pol - Roger etc.

We will supply... but much polished material.

Film gone on... much much.

We:

Juncture's evaluation

One pop.

We go etch... and ...

CP 6, CP 8, CBN Med, Med. pol.

Next meeting: Jan 15
Dec 20 - Small geometry reliability

Of 675 units called 1340, 163 were 1341.
25 failed at Life (all conditions)
15 were 1341
10 were 1340

Let 6137 were 75/75 1341a - 6 failures, 3 were 1340, 300°C, 1000 hours

<table>
<thead>
<tr>
<th></th>
<th>300</th>
<th>200</th>
<th>0</th>
<th>1.75</th>
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<tbody>
<tr>
<td>1340</td>
<td>0.25</td>
<td>0.75</td>
<td>4.25</td>
<td></td>
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<tr>
<td>1341a</td>
<td>0.25</td>
<td>0.75</td>
<td>4.25</td>
<td></td>
</tr>
<tr>
<td>1341</td>
<td>0.25</td>
<td>0.75</td>
<td>4.25</td>
<td></td>
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</table>

All ICB0s are between 50 ma and 100 ma.

Bell phone from NSTC

<table>
<thead>
<tr>
<th></th>
<th>50K</th>
<th>50K</th>
<th>50K</th>
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<tbody>
<tr>
<td>1340</td>
<td>5OK</td>
<td>&gt;50K</td>
<td>50K</td>
</tr>
<tr>
<td>1341</td>
<td>5OK</td>
<td>&gt;50K</td>
<td>12K</td>
</tr>
</tbody>
</table>

The 200°C data certainly seems to suggest that test equipment is not at fault.
Jan 26 — Look at the Xfer Plan

Put needs — assemble — test

Mike Draganic can do now. We will talk with him re: possibility.

We will get a different body.

Have these tasks:
- Fat
- Hel-assembly, assembly
- Test — obelisk

There will be tried in Lab and Xfer.

Required order:

1st product to be done an 8-100 or 8-500. Bide time to get this ASAP.
Negro staff meeting
12/27/63
List for Jim fest.
List of plans for Dr. Needle discussion.
<table>
<thead>
<tr>
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<tr>
<td>Transistors (Si)</td>
<td>106</td>
<td>120</td>
<td>160</td>
<td>210</td>
<td>250</td>
<td>250</td>
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<td>150</td>
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<td>5</td>
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<td>Inst: (Big Test Machines)</td>
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<td>13</td>
<td>15</td>
<td>18</td>
<td>22</td>
<td>26</td>
<td>30</td>
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<td>Lab Eqpt. (Pulse Gen. (D, V, M. (D. C. Amp.)</td>
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<td>65</td>
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<td>95</td>
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<td>12</td>
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</tr>
</tbody>
</table>

GEM/VHG
12/13/62
1/263 - Preplanning meeting meeting

Small geometry:

- Decide Oct 24/63

ABC 0000 - 3 a day by 1/31

xyz 0001 - 3 a day by 1/31

1127 0002 - 3 a day by 1/31

0003 3 est 11/62, ready 1/1

1210

1211

1310 drop 10/27

1311

1321

1322

1324

1221 drop 10/29

1240

1243

1350

1340

1341

1450

3010

3011

3111

U-1

NPM

4200

4205

4300 (target? flexible)

4011 ASAP

4016

4111 to develop, assemble

3001 - 3096 drop immediately

PHP - Power

6266 - # where?

7000 - Where?

SCR-1 (very)

SCR-3 (IBM)
U-10

The failure rate at 80V, 150°C fail at random tends to be high, the median is 1.28.

Try the opposite polarity PET 2, -2.

Step stress - added.

Until we get a fix, we are out of the PET sessions.

1311 - Some runs have C633 soft at Smith diffuser.
        ~20% more than a good bond difference.

1321 - does not have this problem.
        Only real difference is a 2-step bond diffuser 1311 and
        1-step on 1321.

1211 - Heater problem - electrical leakage.

3111 - Failed up.
        Pulls ~30 mV sec, but accept to 20
        Material should be a little thinner than 9-12 cellulose.

12-21 - Stagged, pack 2002.

1450 - Hard to make to spec. Bed for current.
        Low rate, low noise.

NEW

41016 - Being made as per previous adamble.

No consistency, but fine knowledge on units.

Spec characterization by 2/1. File up to 2000/July.

41011 - Drop
1712-1713 - 1 man per day - Continue to aim @ 5x1 week.

There is a reliability problem on these (??)

- 2000w @ 100°C
- 100v @ 160°C
- 1/10

No fail on added lead CR points.

(Three Northern Electric units listed good under life - They were high voltage and presumably failed.

Ellen will test life test 1713.

Characterize by 1/15.

---

45/1

200, 300 stats
- op. (10v) 100°C 1500 mv

(signed) O 300

35/1 - Data sheet out

---

6205

6206 - Had lead bond problem. 1st unit out this week @ 200 will go to op. as 2nd die not yield (730 vs 2 for us)

Application to get a 300 unit vs repl. code

Characterization by 2/15.

7000 - 150 units gain to far 60 of these units tested.

7005 is still fighting others. @ N.O. will get @ 5 man.

3/11, Characterization is lower purity than others.

This is expected as we because HP-9 make must be used.

- Make new stock
- With lead at N.O. & get 750 watts

1) SCR - 1
- Run 2 at Feb 15th 10:30 @ 9/16" stock

2) SCR - 3 (25W) -
Jan 3, 1963 - Resistor

Nichrome:

Work on annealing after evaporation:

<table>
<thead>
<tr>
<th>Temp (°C)</th>
<th>Temp (°F)</th>
</tr>
</thead>
<tbody>
<tr>
<td>300</td>
<td>572</td>
</tr>
<tr>
<td>400</td>
<td>752</td>
</tr>
<tr>
<td>500</td>
<td>932</td>
</tr>
</tbody>
</table>

Only conclusion: Change in R during alloying went down on last 3 runs - up on 8th.

Run not well split.

\[ \text{RTK} = 150 - 350 \text{ except 500° run an 500 - 600 ppm.} \]

<table>
<thead>
<tr>
<th>Plan:</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Make a film that will not change during alloying</td>
</tr>
<tr>
<td>a) IV, high-intensity</td>
</tr>
<tr>
<td>b) Arg, D in a CO atmosphere</td>
</tr>
<tr>
<td>c) Alloy in vacuum</td>
</tr>
</tbody>
</table>

Check on data in two weeks when CTS come back.

Comment: 300 - 400 ppm

Add $\text{Al}_2 \text{O}_3 \text{KOR}$

A constant problem exists, they must be "flooded." Then to

"L" line 6 min spaced.
Visit of Applicant - Eugene Meieran

Eugene Meieran - Ph.D. Metallurgy, February 1963 - plans to visit with us on Wednesday, December 19, to discuss employment possibilities with various members of our Technical Staff. A copy of his personnel file is attached for your information.

In order to make his visit as enlightening as possible for all concerned, the following schedule of activities should, if possible, be followed on the day of his visit:

10:00 - 10:30 Don Palmer
10:30 - 12:00 Meet with Gordon Moore, Worden Waring and Tom Sah in Executive Conference Room.
12:00 - 1:30 Lunch with available members of above group.
1:30 - 3:00 Worden Waring and members of his group.
3:00 - 4:00 Tom Sah and members of his group.
4:00 - 4:30 Gordon Moore
4:30 Don Palmer

In order to complete Meieran's personnel file, the attached evaluation form should be completed and returned to me within two days after your meeting with him.

Your help in making his visit a pleasant one will be appreciated.

Donald Palmer

Distribution:
Gordon Moore
Tom Sah
Worden Waring
APPLICANT EVALUATION FORM

Applicant's name

Last Name: MEIERAN
First Name: Eugene
Middle Name: -

Ph.D. Metallurgy

Degree: Metallurgy
Expected: February 1963
Date of Interview: December 19, 1962

Please give us a brief statement regarding your evaluation of applicant's experience and technical competence:

_________________________________________________________________________________

In your opinion, do you feel that applicant should be considered for employment with Fairchild? Definitely ______ Perhaps ______ No ______

If you do recommend him for employment, in what area(s) do you feel he could contribute the most:

_________________________________________________________________________________

Any other comments you might wish to make concerning applicant:

_________________________________________________________________________________

_________________________________________________________________________________

_________________________________________________________________________________

Date: ________________________________
Signature of Interviewer: ________________________________

(Please complete form and return to Don Palmer, Personnel, R&D Department, within two days after interview)
**PROFESSIONAL APPLICATION BLANK**

**PROFESSIONAL ACTIVITIES**

List Memberships in Professional, Honorary and/or Engineering Societies

- **AIME, ASM, Tau Beta Pi, Phi Lambda Upsilon, Sigma Xi, AEC Fellow**

List Patents Applied for and/or Granted

- "In the Bacterial Lateral to the Determination of a New Pole Figures Technique."

List Publications Authored or Co-Authored

<table>
<thead>
<tr>
<th>Name and Address of School</th>
<th>Major and Minor</th>
<th>Letter Grade Average</th>
<th>Dates of Attendance</th>
<th>Diploma or Degrees</th>
<th>Why Did You Leave?</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLEVELAND HEIGHTS HIGH SCHOOL</td>
<td>SCIENCE</td>
<td>B+</td>
<td>1952-1955</td>
<td>DIPLOMA</td>
<td>GRADUATE</td>
</tr>
<tr>
<td>PURDUE UNIVERSITY</td>
<td>METALLURGY</td>
<td>B+</td>
<td>1955-1959</td>
<td>B.S.</td>
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</tr>
<tr>
<td>MIT, CAMBRIDGE, MASS</td>
<td></td>
<td>B+</td>
<td>1959-</td>
<td>S.M.</td>
<td>STILL HERE</td>
</tr>
<tr>
<td>GRADUATE SCHOOL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GRADUATE SCHOOL</td>
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<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>SPECIAL TRAINING</td>
<td></td>
<td></td>
<td></td>
<td></td>
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EMPLOYMENT BACKGROUND

Complete information on all employment and periods of unemployment during last 10 years must be given. List present or most recent employer. Work back. Include periods of unemployment.

<table>
<thead>
<tr>
<th>Company</th>
<th>Address</th>
<th>Type of Business</th>
<th>Telephone</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATOMICS INTERNATIONAL</td>
<td>De Soto Ave.</td>
<td>Metallurgy Research</td>
<td></td>
</tr>
<tr>
<td>YOUR JOB TITLE(S)</td>
<td>From Mo./Yr. To Mo./Yr.</td>
<td>RATE OF PAY PER</td>
<td></td>
</tr>
<tr>
<td>Research Engineer</td>
<td>6/60 9/60</td>
<td>$600 Month Week Hour</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Rate of Pay per</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Month</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Week</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Hour</td>
</tr>
<tr>
<td>DESCRIBE PRIMARY DUTIES:</td>
<td>Phase diagrams of metal-gas system (exact detail)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

What Did You Like Most? | What Did You Dislike?

How Many Employees Did You Supervise? | What Were Their Job Titles?

Your Supervisor's Name and Title | May We Contact Him or others in This Company for Reference?

Mr. Don Atkins, Supervisor, Dept. 713-35 | YES NO

EMPLOYMENT BACKGROUND

<table>
<thead>
<tr>
<th>Company</th>
<th>Address</th>
<th>Type of Business</th>
<th>Telephone</th>
</tr>
</thead>
<tbody>
<tr>
<td>GENERAL ELECTRIC</td>
<td>Evendale, Ohio</td>
<td>Aerospace Engine Develop</td>
<td></td>
</tr>
<tr>
<td>ANP DIVISION</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>YOUR JOB TITLE(S)</td>
<td>From Mo./Yr. To Mo./Yr.</td>
<td>RATE OF PAY PER</td>
<td></td>
</tr>
<tr>
<td>Research Engineer</td>
<td>6/59 9/59</td>
<td>$990 Month Week Hour</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Rate of Pay per</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Month</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Week</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Hour</td>
</tr>
<tr>
<td>DESCRIBE PRIMARY DUTIES:</td>
<td>Deploy high temperature corrosion resistant materials</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

What Did You Like Most? | What Did You Dislike?

How Many Employees Did You Supervise? | What Were Their Job Titles?

Your Supervisor's Name and Title | May We Contact Him or others in This Company for Reference?

Mr. Jim McCarty, Supervisor, Dept. | YES NO

 PAGE 2
EMPLOYMENT BACKGROUND

Address: Ercikud Ave.
Type of Business: Research Metallurgy

YOUR JOB TITLE(S)
Technician

From Mo./Yr. To Mo./Yr.
6/57 7/57
RATE OF PAY PER
Month Week Hour

DESCRIPTION PRIMARY DUTIES:
Metallurgy research - structure & properties of Titanium Alloys

What Did You Like Most?
What Did You Dislike?

How Many Employees Did You Supervise?

Your Supervisor's Name and Title
Dr. Allen

May We Contact Him or others in this Company for Reference?

YES NO

MILITARY SERVICE WITH U.S. ARMED FORCES

Branch of Service

Rank at Discharge

Date Entered

Date Discharged

Type of Discharge

Are You Receiving A Pension?

Selective Service Classification

Reserve Status

CITIZENSHIP

Are You a Citizen of the U.S.?

(If No, Please Answer The Following Questions)

A. HAVE YOU A LEGAL RIGHT TO REMAIN PERMANENTLY IN THE UNITED STATES?

B. DO YOU INTEND TO REMAIN PERMANENTLY IN THE UNITED STATES?

C. HAVE YOU APPLIED FOR NATURALIZATION PAPERS?

D. HAVE YOU EVER BEEN ARRESTED OR INTERNED AS AN ENEMY ALIEN?

SECURITY CLEARANCE

Have You Ever Applied for Security Clearance?

If Yes, What Classification?

Agency

Current?

Have You Ever Been Denied Security Clearance?

If, Yes, Explain Fully

Do You Know of Any Reason Why You Might Be Denied Security Clearance?

PERSONAL DATA

Date of Birth

Height

Weight

Have You Any Physical Limitations?

Color of Eyes

Color of Hair
MARITAL STATUS

- Single  
- Married  
- Remarried  
- Separated  
- Divorced  
- Widowed

<table>
<thead>
<tr>
<th>Is Your Spouse Employed?</th>
<th>YES</th>
<th>NO</th>
</tr>
</thead>
<tbody>
<tr>
<td>If Yes, Name of Company</td>
<td>Harvard University</td>
<td></td>
</tr>
<tr>
<td>Kind of Work</td>
<td>Secretary</td>
<td></td>
</tr>
</tbody>
</table>

DEPENDENTS

<table>
<thead>
<tr>
<th>NAME</th>
<th>Relationship</th>
<th>Age</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mr. Rosalind Meieran</td>
<td>Wife</td>
<td>24</td>
</tr>
</tbody>
</table>

REFERENCE

<table>
<thead>
<tr>
<th>NAME</th>
<th>Position</th>
<th>Employer</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dr. Morris Cohen</td>
<td>Professor</td>
<td>MIT</td>
<td>MIT, Cambridge, Mass</td>
</tr>
<tr>
<td>Dr. David Thomas</td>
<td>&quot;</td>
<td>&quot;</td>
<td>&quot;</td>
</tr>
<tr>
<td>Mr. Joseph Greenblatt</td>
<td>Engineer</td>
<td>Self</td>
<td>2569 Sycamore Rd.</td>
</tr>
<tr>
<td>Prof. R. Schubmann</td>
<td>Professor</td>
<td>Purdue University</td>
<td>Indianapolis, Ind.</td>
</tr>
</tbody>
</table>

AFFIDAVIT

I expressly waive all provisions of law prohibiting any physician, person, hospital, or other institution that has or may hereafter attend or furnish me with treatment from disclosing to Fairchild any knowledge or information thereby acquired. Further, I agree to the performance of a medical examination by a company designated physician and understand that medical approval must be obtained before employment can be effected.

I authorize all schools which I attended and all previous employers to furnish to Fairchild my record, reason for leaving, and all information they may have concerning me, whether or not it is contained in their records. I hereby release them and Fairchild from all liability for any damage whatsoever arising therefrom.

I certify that I have never been a member of any organization that advocates or has advocated the overthrow of the constitutional government of the United States.

I agree to sign a contract of employment upon employment or at any time requested thereafter on the company's usual form and abide by the provisions thereof.

I understand that, in the event of my employment by Fairchild, I shall be subject to discharge if any of the information I have given in this application is false or if I have failed to give any material information herein requested.

INTERVIEWER'S COMMENTS

DATE

<table>
<thead>
<tr>
<th>Job Title</th>
<th>Rate</th>
<th>Shift</th>
<th>Starting Date</th>
<th>Dept.</th>
<th>Section</th>
<th>For Dept.</th>
<th>For Personnel</th>
</tr>
</thead>
</table>

PAGE 4
OUTGOING MESSAGE

ADDRESSEE: REGISTRAR
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
CAMBRIDGE 39, MASSACHUSETTS

ORIGINATOR: DONALD PALMER
DEPT: PERSONNEL EXT: 301

MESSAGE INFORMATION:

MR. EUGENE S. MEIERAN BORN DECEMBER 23, 1937 INDICATES ON HIS EMPLOYMENT APPLICATION THAT HE EXPECTS TO RECEIVE HIS PH.D. DEGREE IN METALLURGY APPROXIMATELY LATE 1962 OR EARLY 1963 STOP WOULD YOU PLEASE VERIFY THIS INFORMATION BY RETURN COLLECT WIRE STOP WOULD ALSO APPRECIATE BEING ADVISED HIS CLASS STANDING IF YOU RANK STUDENTS THIS MANNER STOP THIS INFORMATION WILL BE HELD STRICTEST CONFIDENCE STOP

DONALD PALMER

Eugene Stuart Meieran currently registered at MIT. He expects to complete requirements for degree of Doctor of Science in field of metallurgy in February '63. Rank in class not available.

W. D. Wells
Associate Registrar
Mr. Donald Palmer, Personnel Manager  
Fairchild Semiconductor Corporation  
4001 Junipero Serra Boulevard  
Palo Alto, California

Subject: Mr. Eugene S. Meieran

Dear Mr. Palmer:

In reply to your letter of November 12, I can recommend Eugene Meieran very highly for employment on your Technical Staff. Meieran is now completing his thesis for the Doctorate in Metallurgy at MIT, and he is giving a good account of himself. His work on electron microscopy and preferred orientations is first-class, requiring both experimental skill and fairly sophisticated interpretation.

Meieran knows how to keep his eye on the ball, and as a result he has made excellent progress in his graduate program. At first, he seemed to be disconcerted by the rapid pace here, but after a while he demonstrated that he could hold his own with the best of the graduate students here.

You will find that Meieran has drive, perseverance, and a sincere desire to find meaning in what he is doing. He knows how to design research projects and follow through. However, he is still a young man, and benefits from senior advice and encouragement from time-to-time.

Sincerely yours,

Morris Cohen
Mr. Donald Palmer  
Personnel Manager  
Fairchild Semiconductor Corp.  
4001 Junipero Serra Blvd.  
Palo Alto, California  

Dear Mr. Palmer:

I am writing concerning the application of Mr. Eugene S. Meieran for employment with your organization. He has given my name as a reference.

Meieran has been carrying out his graduate work at MIT under my supervision since he arrived from Purdue in 1958. Meieran has a strong interest in x-ray diffraction, electron diffraction, experimental crystallography, and related fields. He has a particular knack for devising equipment to do experiments in these fields. His most recent experience has been with transmission electron microscopy of tungsten, which is closely associated with the diffraction problems that are of such interest to him. He has made significant contributions to our work in this area.

Meieran is also competent theoretically, but he is more reluctant to apply himself there than in experimental studies. However, he shows increasing interest in crossing the lines between experimental and theoretical work.

Meieran is an intense individual, occasionally to the irritation of others. However, he has worked in the electron microscopy laboratory quite successfully in the past year or two, and I think he appreciates the results of cooperation better than ever before.

Sincerely,

David A. Thomas  
Associate Professor of Metallurgy
To: Paul Hill
From: Dick Robinson
Subject: Standard Masking, Micrologic

Project: No. 48 - Standard Masking Procedure, Micrologic
Object: Evaluate Standard Masking (30 cs. KPR) for Micrologic and Implement if feasible.
Summary: This report contains the results of comparison of production micrologic masking with standard masking by process development for the same micrologic patterns. The present production method was found to give superior pattern fidelity on the etched wafers.

Method: All pattern measurements were made with a calibrated filar eye piece at 500X. Resistor bar widths were measured at the bottom of the oxide cutout and at the center of the bar. The mask measurements were made for a previous report (Project No. 39 - Review of Mask Manufacturing Methods, December 14, 1962). The three largest wafers from each run were selected for comparison and all samples were from the center 10 patterns of row 13, μ L Mask H-60-Y-3 (the row with three missing patterns). The runs for comparison were selected at random, the line runs from whatever was available on the date the measurements were made and the standard mask runs from four runs masked by Process Development.

Data: Nomenclature
\[ \bar{X} = \text{mean of 10 measurements, mil.} \]
\[ s = \text{sample standard deviation, mil.} \]

<table>
<thead>
<tr>
<th>Line Masks:</th>
<th>( \bar{X} )</th>
<th>( s )</th>
<th>( \bar{X} )</th>
<th>( s )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistor</td>
<td>( s )</td>
<td></td>
<td>( s )</td>
<td></td>
</tr>
<tr>
<td>1.</td>
<td>2.029</td>
<td>0.008</td>
<td>2.032</td>
<td>0.016</td>
</tr>
<tr>
<td>2.</td>
<td>2.038</td>
<td>0.008</td>
<td>2.031</td>
<td>0.012</td>
</tr>
<tr>
<td>3.</td>
<td>2.031</td>
<td>0.010</td>
<td>2.027</td>
<td>0.013</td>
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</table>

<table>
<thead>
<tr>
<th>Process Dev. Mask:</th>
<th>( \bar{X} )</th>
<th>( s )</th>
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</thead>
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<tr>
<td>Resistor</td>
<td>( s )</td>
<td></td>
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<tr>
<td>1.</td>
<td>2.044</td>
<td>0.017</td>
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<tr>
<td>2.</td>
<td>2.044</td>
<td>0.023</td>
</tr>
<tr>
<td>3.</td>
<td>2.031</td>
<td>0.018</td>
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</tbody>
</table>
Line Masked Wafers:

<table>
<thead>
<tr>
<th>Run No.</th>
<th>Resistor</th>
<th>( \bar{X} )</th>
<th>( s )</th>
<th>( \bar{X} )</th>
<th>( s )</th>
<th>( \bar{X} )</th>
<th>( s )</th>
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</thead>
<tbody>
<tr>
<td>HY 237</td>
<td>1</td>
<td>2.003</td>
<td>0.034</td>
<td>1.888</td>
<td>0.036</td>
<td>1.974</td>
<td>0.043</td>
</tr>
<tr>
<td>(12-7-62)</td>
<td>2</td>
<td>2.022</td>
<td>0.027</td>
<td>1.917</td>
<td>0.044</td>
<td>2.006</td>
<td>0.027</td>
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<td></td>
<td>3</td>
<td>2.020</td>
<td>0.029</td>
<td>1.920</td>
<td>0.032</td>
<td>2.006</td>
<td>0.022</td>
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<tr>
<td>HY 272</td>
<td>1</td>
<td>1.947</td>
<td>0.028</td>
<td>1.923</td>
<td>0.036</td>
<td>1.929</td>
<td>0.032</td>
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<td>(12-17-62)</td>
<td>2</td>
<td>1.965</td>
<td>0.018</td>
<td>1.940</td>
<td>0.038</td>
<td>1.946</td>
<td>0.037</td>
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<td>3</td>
<td>1.964</td>
<td>0.017</td>
<td>1.931</td>
<td>0.029</td>
<td>1.940</td>
<td>0.047</td>
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</table>

Standard Masked Wafers (Process Development):

<table>
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<tr>
<th>Run No.</th>
<th>Resistor</th>
<th>( \bar{X} )</th>
<th>( s )</th>
<th>( \bar{X} )</th>
<th>( s )</th>
<th>( \bar{X} )</th>
<th>( s )</th>
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</thead>
<tbody>
<tr>
<td>HY 245</td>
<td>1</td>
<td>1.668</td>
<td>0.085</td>
<td>1.808</td>
<td>0.035</td>
<td>1.826</td>
<td>0.044</td>
</tr>
<tr>
<td>(12-10-62)</td>
<td>2</td>
<td>1.708</td>
<td>0.086</td>
<td>1.815</td>
<td>0.041</td>
<td>1.833</td>
<td>0.040</td>
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<tr>
<td></td>
<td>3</td>
<td>1.691</td>
<td>0.077</td>
<td>1.831</td>
<td>0.037</td>
<td>1.834</td>
<td>0.033</td>
</tr>
<tr>
<td>HY 245</td>
<td>1</td>
<td>1.892</td>
<td>0.026</td>
<td>1.852</td>
<td>0.031</td>
<td>1.854</td>
<td>0.043</td>
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<tr>
<td>(12-17-62)</td>
<td>2</td>
<td>1.923</td>
<td>0.025</td>
<td>1.887</td>
<td>0.037</td>
<td>1.884</td>
<td>0.044</td>
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<td>0.028</td>
<td>1.890</td>
<td>0.031</td>
<td>1.889</td>
<td>0.047</td>
</tr>
</tbody>
</table>

Analysis of Results:

The data show that standard masked wafer patterns are smaller than the specified 2.00 mil. by a greater amount than line masked wafers. This can be also seen by comparing mean mask size with mean etched image size:

\[
\begin{array}{ccc}
\text{Mask} & \text{Image} & \text{Difference} \\
\text{Line Mask} & 2.030 & 1.958 = 0.072 \text{ mil.} \\
\text{Standard Mask} & 2.040 & 1.834 = 0.206 \text{ mil.} \\
\end{array}
\]

Conclusions and Recommendations:

1. The present micrologic process should be retained where etched pattern dimensions are critical (base, emitter, and oxide removal masks).

2. Standard masking could be used for isolation masks if pinhole reduction is required since image size is not as critical for these masks.

Dick Robinson
Process Development
Royle meeting: 13/62

1. List of people
2. Write a yearly progress report compared with goals.
3. Feb 1 meeting
1. at gate - epil
   Mean 5
   1st run broke of (1 good, 1 bad) - 1st tube open
   bad spread on mandrel - 5-15 μ"!

2. 11/20 VCESAT ~ 15+ solution - chilren less

2 other runs (1 in emittor, 1 in base)

2 runs at 5 μ" ~
~ 20 runs in no run @ Aa 0.075μ"
1 run in emittor
1 run in base diffuser

[Table]

1. Presumably, the G4 Xs are perfect for the previous has been offset by A/H.

2. Buy box, wait to see that 10μ" spread

4. 5μ" leaking plate will be used.

3.

State of stuff:
ALICY

G, S, "H review of process
2 run of G's is evaluation (Sample)
R₀ ~ 650
R₁ ~ 550
Rest of moves kept as

C, plot, doing the other apertures, modes
INTERNAL CORRESPONDENCE
FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

TO: L. G. Reis
FROM: H. B. Grutchfield
DATE: February 8, 1963
CC: B. C. Knudson

SUBJECT: Results of Tests to Evaluate the Model Proposed to Explain "Secondary Breakdown" in Transistors

Purpose

To document the results of tests conducted to evaluate the model proposed to explain secondary breakdown in transistors.

Conclusions

The test results agree with the results predicted by considering a one-dimensional transistor model in which the $V_{BE}$ at any operating condition with a forward biased base-emitter diode, is assumed to vary in a random manner as a function of lateral displacement from a reference point on the junction.

Summary of Tests and Results

Six TC4016's were selected at random from a bucket of unclassified units. The units were checked for opens and shorts. However, the only criteria used to select the devices to be used was that each unit have an $V_{CEO} \geq 80$ volts. No attempt was made to match $h_{FE}$'s or $V_{BE}$'s.

The units were then soldered into a 2" x 1" x 1/2" copper heat sink and wired for parallel operation. Each emitter was brought out separately so that a resistor could be connected in series with the individual emitters.

The thermal resistance of each individual transistor was measured in a heat dissipating bath biased at $V_{CB} = 10$ V and $I_E = 0.1$ A. Values were:

<table>
<thead>
<tr>
<th>Unit No.</th>
<th>$\theta (\degree C/W)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>39</td>
</tr>
<tr>
<td>2</td>
<td>37.4</td>
</tr>
<tr>
<td>3</td>
<td>37.4</td>
</tr>
<tr>
<td>4</td>
<td>39.8</td>
</tr>
<tr>
<td>5</td>
<td>40.5</td>
</tr>
<tr>
<td>6</td>
<td>35.4</td>
</tr>
</tbody>
</table>
The thermal resistance was then measured at a constant $I_E = 0.5$ A at several collector voltages on the paralleled devices; first with no resistor in the emitters, next with a one ohm resistor in each emitter, and finally with a 10 ohm resistor in each emitter. The results are plotted in Figure 1.

Next, the emitter current of each individual unit was measured, first with no resistor in the emitters and then with a 10 ohm resistor in each emitter. Again, the total $I_E = 0.5$ A. The results are plotted in Figure 2.

It can be seen, by comparing Figures 1 and 2, that the increase in thermal resistance with no resistor in the emitters is a result of current "hogging" by device #5. The cause of the high thermal resistance at low collector voltages with a 10 ohm resistor in each emitter can also be seen -- device #3 is "hogging".

Figure 3 shows the thermal resistance as a function of collector voltage at $I_E = 0.5$ A for a different group of six TC4016's mounted in an identical manner. The current would appear to be more evenly distributed in this group. (This group was destroyed before the current distribution could be measured.) Nevertheless, the effect of the stabilizing resistors can be clearly seen.

The secondary breakdown voltage of the unit depicted in Figures 1 and 2 was measured with and without the stabilizing resistors. The total emitter current was again 0.5 A. Secondary breakdown occurred at $V_{CB} = 20$ V with no emitter resistors; at $V_{CB} = 50$ V with a 10 ohm resistor in each emitter. The secondary breakdown voltage was also measured on each individual device at $I_E = 0.25$ A. With the exception of device #5, secondary breakdown occurred at a collector voltage of 26 V to slightly in excess of 30 V. Secondary breakdown occurred on device #5 at $V_{CB} = 18$ V.

The secondary breakdown characteristics of the unit shown in Figures 1 and 2, without stabilizing resistors, is similar to some of the poorer 7000's and 6206's measured by the author. The characteristic of the unit shown in Figure 3 is similar to the better 6206's.
SIX TC 4016'S MOUNTED IN PARALLEL ON HEAT SINK
THERMAL RESISTANCE IN TCE BATH, θ VS. V_{CB}
I_E = 0.5 A.
(UNIT #2)
Fig. 2

SIX TC4016'S MOUNTED IN PARALLEL ON HEAT SINK (*2)

I_e VS. V_{CB}

NO RESISTOR IN EMITTER

10 OHM RESISTOR IN EACH EMITTER

I_e (mA)

V_{CB} (Volts)
SIX TC4016'S MOUNTED IN PARALLEL ON COPPER HEAT SINK (+1)
THERMAL RESISTANCE, $\theta$ vs. $V_{cb}$ AT CONSTANT $I_e = 0.2$ A.
(TCE BATH)
Integrated NAND Alternatives

Circuit #1

Circuit #2

Circuit #3
Output Voltage $V_{out}$ and Lead Current Drawn at Output $I_L$

Input Voltage to Circuits #s 1, 2, & 3

Temperature $= +125^\circ C$
Revision or GY revisited:
1. G mesh

Often flattering problems not solved in large geometry.
No means for small yet.

We will supply a G small geometry for a mate.

Now still fighting problems in film. We are confused.

2. Pipe problems

a. Original oxide thickness appears to need 70 yield - 50% to 6 feet in 65 @ 4

b. More yield at bare diffusion (old pattern)

Iron yielding: 78,000 psi in 57% at 1 bar.

c. Sharper gradient at step helps.

d. It seems to help to do O as fast as 12.50 a bar.

:: A pilot test to look at the effect of all of these on direct yield is being attempted. This is a 6-7 week cycle test in argon production lines.

1. 30% against 2. larger sample.

A pilot line on the 4799 is running handling is running (i.e., potential output).

70% Throttling - No P before retention or other additions.

But a slow before after 13 diffusion. We get them?

Or some older men pipe in here as P and finally 9 month.

drop in Si.
Phil Hunt will look for prints back p N by 50c.
PnP reliability meeting - Mte, Vrtn.

4511 @ 200°C, 20V - just but any unit failed - charmed

Tested all PnP
4511 @ 200°C tested bad
every tested good 1746, 3511,

Tested @ 200°C, the silicon last.
Meeting 1/15/63

New matter:

Only 1341 will accept it - up to 20% of total. New is being supplied now because materials are to suit until it looks good. It still has a lot of bugs. Need also priority to supply materials again by about the end of this week.

Material problems:

1. Surface appearance.

Date shows that this is more work to report transfer as for As over $50.

It looks to me like one possible thing to make:

1. Need to start 1341 material
2. To get data from him
3. Then from West sample
4. To give sample to
5. To get evaluation
6. 15 weeks - to change
7. 16 weeks of resistance (small) in resistance
8. 8 weeks fairly doing a flange on another
9. For the big system.

What about going there for large or running them.

Large: 596 in 20 or 20, 500 in 20. We will put an order for 20.

Large: 5800 and lots to set up.

Diamond is nice and good.

R&D will check out the proper underpinning.

On substituting:

- Subs. of metal: 50%
- Subs. of carbon: 60%
- Subs. of iron: 80%

Hank, will bring a re-do to check substitutes.

Next meeting scheduled in 4 weeks. Have cell in 2.
Metalization - Ag - C1

We have been able to substitute @ 10". Start C1 swap 600 cc substitute.

I think if multiple heating isn't good, try to start Ag.

No subsequent alloy cycle.

We have been able to replace for Phile's some small geometry units - call him.

Some may still come.

We are sending 206 coupon for Phile to metallograph

We have done:

6.21 1/2 in x .340 x .321 in

Inserted set up,

Somewhat less substitute T

Marvin think there is no reason now for getting demin resistance now

Being done:

1. Make ~500 units (6.21 in) then. These will be put on the shelf ready for the attached metal. Yield will also go to be collected during final assembly.

Units by 11/26 at present, to go to 500 in.

2. Small geometry - It is not clear that we have all some small units - Smaller or similar ?

3. M.I. will check at An necessary for demin

4. 4000's - as all make some

Date can ~6 units 30K's strung - remained good.

Certified - all ok. - 260/2651 (date 1321)

And An call.

Our world has started in on

On 11/22/63 I looked at Phile's data on 100 units for 2000 hr @ 375 C. Book looked good,

but that was some USE pattern.
Please fill in your schedule for the following and give it to me (leave with Helen) by 12:00 today:

1. Mask layouts for Micrologic elements to Sam
   
   **My original date to be beaten** | **Your date as of now**
   --- | ---
   G - This week | Yesterday
   H - Today | Today
   C - Next Wednesday | Next Tuesday (1/22/63)
   B - Next Friday | Next Friday (1/25/63)
   F - One week after the H (also 4 input G & 2 input G alt.) | 1/29/63

2. When will S's be thru -- please give best guess.
   
   **Die sort-1st units** | **rest of run** | **evaluation**
   --- | --- | ---
   1st run | Wed.-Thurs (1/23 - 24) | 1/25 | 1/31 no test spec
   2nd run | 1/31/63 | 2/1 | 2/8
   3rd-5th | 2/4 | 2/8 | 2/12 - 2/15
   (3rd run) | (5th run) | 2/5 - 2/8

**Thanks.**

G. E. M.
To: G. E. Moore
From: J. P. Ferguson
Subject: Material Requirements for Epitaxial µL

Date: January 17, 1963

CC: V. Grinich
     C. Sporck
     D. Farina
     C. Plough
     D. Cole

The following schedule comprises the R&D contribution to the supply of material for the epitaxial micrologic evaluation:

<table>
<thead>
<tr>
<th>Wafers/week</th>
<th>Week Beginning</th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1/28</td>
<td>2/4</td>
<td>2/11</td>
<td>2/18</td>
</tr>
<tr>
<td>Sb &amp; Epitaxy at R&amp;D</td>
<td>75</td>
<td>75</td>
<td>75</td>
<td>75</td>
</tr>
<tr>
<td>Sb at R&amp;D, Epitaxy</td>
<td>75</td>
<td>150</td>
<td>150</td>
<td>150</td>
</tr>
</tbody>
</table>

Continue until no longer needed

At present, the only pre-dep mask available is that of the S element. Hence, all of the material until about 2/4 will be for this element. After that, the material will be split as pre-dep masks for the other elements become available so that units of each element type will be available for characterization as soon as possible.

C. Plough plans on having his Sb furnace in operation by 2/1/63. At that time he will begin supplying wafers to Stierlin Road.

The material specification is as follows:

- Wafer Size: 1-1/4" max.
- Wafer Thickness: 180-220 µ
- Substrate Resistivity: 3-6Ω - cm "P" type
- Layer Thickness: 10µ + 2
- Layer Resistivity: 3/3 - .6 Ω cm "N" type

Sb pre-dep V/I: $\approx 4 \Omega/cm$

It is most important that all the material used meets these specifications since undue variations in Sb pre-dep V/I, layer thickness and layer resistivity will significantly affect the electrical specifications which may be guaranteed.
Ministry "policy" meeting - 11/8/63

Action from last meeting:

1. Egl. on the flight has been retired - flight 1BT 1 nov.
2. Remain in lieu of assigned to do.
3. On met.
   1. Optical glass to get for
   2. Ask for a certificate in after 250 km

4. Check on Anca land on flat package
Jan 18, 1963  Meeting concerning something on PL products

1. Date on SP

2. Date on 64 (CB)

3. Any other deficiencies of this. Do because that the mesh are which is made

Ron Fleming:

4. Run made to date - are only canned
   Off the good weighs, leakage there isolation was good
   CB CPW ran 15-20 P trapped
   Goin' problem of evaluating the value & units, quite linear
   That will require a complete age change to get yields on 1BP

On the 23'4th run we have some channel problems. No channels
   appeared during catalysis; before catalysis through Coldpoint.

Yield data on GB - it was to be a great plug in anyway
   Internal table for correlation needed charging

7 run out  - had high resistors
   Other than had been doing right, but some cosmetic problem
   17 only 1 run that was good - in gett
   Should give a 40% yield to agree with lab at nom T.
   Higher flow of nitrogen &

All mesh shall be designed for final tone "E" (27.5 dB)

Conclusion on GB:

1. Run to prevent GB male and feed problems are
2. Change mesh on long reactor - Bussy
### HIGH FREQUENCY PROJECT PLANS

<table>
<thead>
<tr>
<th>PROJECT</th>
<th>GOAL</th>
<th>1963</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Saturating Switches:</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1. 1200°C gold with diffused emitter-NPN</td>
<td>$\tau_s \leq 2$ nsec.</td>
<td>F</td>
</tr>
<tr>
<td>2. Heavily doped substrate, epitaxially</td>
<td>$\tau_s \leq 2$ nsec.</td>
<td>F</td>
</tr>
<tr>
<td>grown base</td>
<td>$\tau_s \leq 20$ nsec.</td>
<td></td>
</tr>
<tr>
<td>a. NPN</td>
<td>Sat. and non-sat.</td>
<td></td>
</tr>
<tr>
<td>b. PNP</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3. Inverted structure NPN</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4. CDC, 2 stripe, three input gate, nichrome</td>
<td></td>
<td></td>
</tr>
<tr>
<td>resistors optional</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5. Minimum $\tau_s$ PNP, reverse biased</td>
<td>$\tau_s \leq 20$ nsec.</td>
<td>F</td>
</tr>
<tr>
<td>junctions</td>
<td>4011 performance</td>
<td></td>
</tr>
<tr>
<td>6. One ampere driver</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7. Other impurities on epit. substrate</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>R.F. Transistors and Diodes:</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1. Straight size reduction, majority base</td>
<td>.1 mil stripes and spacing</td>
<td>F</td>
</tr>
<tr>
<td>one device</td>
<td>2-3 kmc.</td>
<td>D</td>
</tr>
<tr>
<td>2. High $f_T$ device (Sandia contract)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>a. All diffused</td>
<td></td>
<td></td>
</tr>
<tr>
<td>b. Surface Barrier emitter</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3. FT-0006 aggregate</td>
<td>2.5 watt at 500 mc</td>
<td>D</td>
</tr>
<tr>
<td>4. FT-0007 aggregate</td>
<td>5.0 watt at 500 mc</td>
<td>D</td>
</tr>
<tr>
<td>5. Harmonic generation diodes</td>
<td>Misc. geometries</td>
<td></td>
</tr>
<tr>
<td>a. FD-7 w-w/o gold, different layer</td>
<td>and structures</td>
<td></td>
</tr>
<tr>
<td>thicknesses</td>
<td>F</td>
<td></td>
</tr>
<tr>
<td>b. FD-6 w-w/o gold, different layer</td>
<td>F</td>
<td></td>
</tr>
<tr>
<td>thicknesses</td>
<td>F</td>
<td></td>
</tr>
<tr>
<td><strong>Low Current Devices (Low Noise):</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1. Inverted NPN/PNP</td>
<td>$h_{FE} \geq 10$ at 1 na</td>
<td>F</td>
</tr>
<tr>
<td>2. Guard ring structure</td>
<td>$h_{FE} \geq 10$ at 1 na</td>
<td>F</td>
</tr>
<tr>
<td>PROJECT</td>
<td>GOAL</td>
<td></td>
</tr>
<tr>
<td>---------</td>
<td>------</td>
<td></td>
</tr>
<tr>
<td>CHARACTERIZATION:</td>
<td>1963</td>
<td></td>
</tr>
<tr>
<td>1. Stripline</td>
<td>FMAMJJASOND</td>
<td></td>
</tr>
<tr>
<td>2. Aggregate interconnection inductance</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3. Co-axial</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4. Aggregates in BeO power package</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
20 ± 15\% m

10-90\% ± 15\% m & mm

Peak ± 10\%
Jan 23, 1963

High frequency device project

Dat manner:

1. Work on low loss stages. NM logic - worth more.
2. Work toward active post. Looking possible.
3. Develop fiber drive - fairly straightforward.
4. CDC gets - straight forward.

R.F. Transistors and diodes:

1. The 0.1 mil test vehicle could.
2. High for device for diode.
3. High from 1.6 drive - what should we do?

Back-up work needed:

1. Upside down assembly technique.
2. Other manurics.
3. 

Discrete chip obt:

1. Test rebuild - an idle band limited signal amplifier. S/P A. F. N. I.
Schedule of Work

1. Sit part
   a) NPN 528 \\
   b) PNP 18 ns (45 deg) \\
   c) NDG diode \\
   d) PMOS diode

2. For current - low noise

3. Made band d-c coupled amp (against dip)

4. R.F. preamplifier
   a) band-limited
   b) 0.1 us Vehile
   c) from RF \\
   d) power doubler
March 24th, 1963

6-B. all maybe used, 5,6,8,7,9,11 maybe made

no possible drop on 5th 1/4 drop 2/4

It feels like So. Mnt is 20 m. above. If this is the case then 5 must be done.

Feed to Bob Graham, he would rather stay with the
fallout for 1A-6, 89G. if he thinks he can sell them for an A.

Action:

The sample of 50 units from each of 11 runs will be

measured for 1A, 89G. But run out of 4" yield correlated test

and again to 1A, 89G. by temp extreme measurements.

Also for B units

In addition we want reasons for complete rejection.

Plough will present resistors and Beta speed data.

As soon as possible Bob Schultz will get yield on what

would happen if we did not limit on compatibility by parallelling

old 1A to GB.

Farries will run impeller plot on a sample of cat. A corral

A=6 V.

Agree: on data as of next me talk 10-19 73.

No makers changes on the GB.

Epitaxial will run with its present bar resistor.
Minutes:

Van feels that copy camera will do the memory away job. He will do the text job.
Epitaxial Project Review 1/23/63

Carry on surface preparation:

Sanded, laser, a stage of polishing, reprinted, and electron microscopy.

There are still the little bumps (or pits?) that carry across everything. Looking at sterling A D mental often after etch, it is all covered in semi-clean spots.

We now can get a good polish on Si:

Lap on 30 grit, then 1 ppm for small mini. To get good and flat.

- 1 hr of milk with 600
- 0.1 hr of etch with 600 or 2002
- 30 min total removed

Then are scratched free to work light and dark field.

Rocks on evaluation:

1. Thickness measurements

\[ \text{oxide} \] \[ \text{Epi} \]

\[ \text{substrate} \]

The IR "always" reads thicker, even than one gets by paper extraction of the dark etched stains.

Rings were made with Sb,Hb 0s, Au at 1177 and 1080 in. up to 1160.

We get identical gradients over about 5 m length.
It looks like the profile is even function. The Sn or Se sample are in fair agreement with solid state diffusion.

On the Sn m As exp.

As X .006 10

Sn .01 20

Confin the debut by chem analysis.

The grown films will be high resistivity m and p.

One of the p type will be used for Hall mobility. Cite lab.

This will be done in ~ 3 weeks.

Yam m vapor etch

add 0.2

H2 & Te

0.0 0.3 0.6 0.9

rate 

10

vol

0.0 0.1 0.2 0.3 0.4 0.5
1. Power - No work planned beyond what we are
   2. High frequency - Strip line looks better than
   the coax.

3. 70-18 glass on a back-up for Hong Kong. This is necessary because
   they use a glass multiform which breaks after operating at 10-5.

4. MyView is completely over to their own flat package.
   Special problem - doing something similar on very strong on non-developed flow.

5. Metallization
   a) Silk screen
   b) Plate metal

6. Box Assembly eliminating the little union and a built chip assembly.
   Problem (for your darn)
   1. Contact, area, build-up
   2. Insulator, on, plane
   3. Fine line pattern
   4. Joining of contact to substrate
   Fine grand summary of the face down

Benji's fig - you'd then be able to put a
ball in perform right side up assembly.
   a) Au balls
   b) Ag pads
   c) Bond perform

1st priority - solid package or no separate little union
2nd is separate chip assembly
3rd is assembly of package to system

7. We have agreed on a simple approach to the HP-3 package

5,
CML: Scales has the test vehicle laid out - a circuity from "bit" to "bit" multiplex. It has 108 GEP 's.

Nothing else to do until the element concert.

Scales will write up design.

New R-element design. This is the long-missing NAND memory.

The test vehicle should be a stage doubler and a fast one on the same chip.
The channel problem:

Lewis: Suggestion on heat treatment of O-containing material.

The channel fits the temp dependence.

Lewis: Some channels in the oxide states within the Si. It disappears upon F.

There is a geometry effect. This will be checked out.

Proposed experiments to distinguish mechanism:

1. Strip & react
   Return etch & react.

2. Increase channel via p-depo or high p n-lot has few channel.

We have no experiments to distinguish between the two proposed mechanisms.

PNP channel problem - anodic oxide.

Len Carlson:

1. After doped oxide by anodic - all groups had channels.

   Resolution: After diffusion - units being canned.

   Data will start coming out soon.

   Life data on a) P-on ageing.

   (We can strip and re-grow oxide by anodic for this)

   b)
Anodic oxide, cont

On anodic FET's:

Some pages that they are stable at 300°C storage or not for thermal
humidity. Do not use the anodic FET's that are higher or anodic FET's, but
are not changing so much.

The pages:

1. Find out what it is to see what happens.
2. Try 5.0

Other items:

1. There is a reduction of pips on SCR's with applied anodic oxide. This is next
   defined as phase above then pristine.
   - Ten Omika data.

2. Be sure to re-set the pitch.
3. Triad for 4200 (Bill O'Kelley)
4. Triad for some of the transistor stuff
5. Cigarette - Man
Making Sanity summary:

Definition:

Compatibility:

The new chug can be plugged into a system made with the old units in any combination, and the new system will continue to function over the entire temperature range.

Absolute compatibility:

Compatibility will always be assured because of the test specification of the new chug.

Statistical compatibility:

Compatibility depends upon the extreme likelihood of getting a unit worst case, but is not guaranteed by the specification.

Customer specifications:

All these numbers on the data sheets and in special customer specs that are guaranteed on an individual unit. This does not include "typical" numbers.

Internal specifications:

These internal tests which are performed in order to assure that the customer specifications are achieved.
Questions:

µL
GB
Epi

There is one yield (~1028) that is absolutely compatible with µL.

This is probably some yield of Epi to µL, that is. But because of the internal test of Epi means of Clamp VCE, VBE, that does not meet internal specifications.

Because we looked at -- not least it is in the right direction -- the CG and Epi may be absolutely compatible.

Resolved:

1. Nothing shall stand in the way of making an optimum genetic family tested and priced to gain optimum yield of performance.

This will involve changes in test points initially as well as new external spectra.

There will be no yield of smite absolutely compatible with µL.

There will be a yield (perhaps very low) that is compatible with CB12.

2. It shall be necessary to produce for an indefinite period limits that are absolutely compatible with µL.

This can be

a) The GB structure perfectly tested
b) A new genetical structure destined to gain compatibility. This is useful only to be able to completely drop the old technology.
Continuing, \( \left( \frac{2.76}{R_C} \right) (1000)(R_{SAT}) \leq 190 \), or \( R_C \) must be \( \geq 14 \) or \( 15 \) \( R_{SAT} \) for good yield.

\( R_C/R_{SAT} \) was greater than 15 in most of the units to date, excluding an \( R_{SAT} \) tail; it appears that initially material should stay on the low side and \( R_C \) in the 540 - 620 \( \Omega \) area for optimum yield to \( F_0 = 5 \).

7. Tabulated distributions are given:

<table>
<thead>
<tr>
<th>RUN #</th>
<th>100</th>
<th>102</th>
<th>103</th>
<th>104</th>
<th>105</th>
<th>106</th>
<th>116</th>
<th>117</th>
<th>130</th>
<th>134</th>
<th>137</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_C ) 10%</td>
<td>600</td>
<td>640</td>
<td>610</td>
<td>610</td>
<td>570</td>
<td>570</td>
<td>610</td>
<td>620</td>
<td>560</td>
<td>550</td>
<td>550 ( \Omega )</td>
</tr>
<tr>
<td>( R_C ) 50%</td>
<td>700</td>
<td>710</td>
<td>690</td>
<td>690</td>
<td>670</td>
<td>660</td>
<td>680</td>
<td>660</td>
<td>610</td>
<td>610</td>
<td>610 ( \Omega )</td>
</tr>
<tr>
<td>( R_C ) 90%</td>
<td>800</td>
<td>800</td>
<td>780</td>
<td>760</td>
<td>770</td>
<td>740</td>
<td>760</td>
<td>710</td>
<td>730</td>
<td>690</td>
<td>690 ( \Omega )</td>
</tr>
</tbody>
</table>

\( \beta \) 5 mA 10% (1 Pin) 48 45 35 30 45 30 25 26 24 30 35

\( \beta \) 50% (1 Pin) 80 70 60 50 75 62 50 38 43 50 65

\( \beta \) 90% (1 Pin) 120 125 90 70 130 120 80 59 62 100 130

| \( R_{SAT} \) 10% (1 Pin) | 29 | 28 | 28 | 31 | 27 | 25 | 26 | 25 | 30 | 26 | 27 \( \Omega \) |
| \( R_{SAT} \) 50% (1 Pin) | 34 | 35 | 36 | 36 | 34 | 35 | 28 | 28 | 40 | 33 | 34 \( \Omega \) |
| \( R_{SAT} \) 90% (1 Pin) | 40 | 42 | 50 | 43 | 39 | 44 | 34 | 35 | 48 | 40 | 38 \( \Omega \) |

<p>| ( V_{SAT} ) 10% (1 Pin) | .149 | .140 | .160 | .160 | .150 | .147 | .142 | .145 | .172 | .140 | .170 ( \text{V} ) |
| ( V_{SAT} ) 50% (1.5V) | .173 | .180 | .180 | .210 | .180 | .187 | .165 | .158 | .223 | .190 | .190 ( \text{V} ) |
| ( V_{SAT} ) 90% (( V_{BE} )) | .217 | .210 | .250 | .230 | .210 | .244 | .189 | .182 | .269 | .230 | .230 ( \text{V} ) |</p>
<table>
<thead>
<tr>
<th>Run</th>
<th>100</th>
<th>102</th>
<th>103</th>
<th>104</th>
<th>105</th>
<th>106</th>
<th>116</th>
<th>117</th>
<th>130</th>
<th>134</th>
<th>137</th>
<th>TOTAL % of TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>TOTAL TESTED</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Good FO = 5 Mk II &lt;</td>
<td>50</td>
<td>49</td>
<td>50</td>
<td>40</td>
<td>50</td>
<td>50</td>
<td>48</td>
<td>41</td>
<td>50</td>
<td>528</td>
<td>100%</td>
<td></td>
</tr>
<tr>
<td>Good μEE but bad Mk II 25°C FO5</td>
<td>0</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>NET GOOD 25°C FO5</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Good -55°C Not Good 25°C FO5</td>
<td>9</td>
<td>3</td>
<td>5</td>
<td>1</td>
<td>7</td>
<td>7</td>
<td>2</td>
<td>0</td>
<td>1</td>
<td>8</td>
<td>22</td>
<td>65%</td>
</tr>
<tr>
<td>Good +125°C Not Good 25°C FO5</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>3</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td>Good -125°C Not Good 25°C FO5</td>
<td>10</td>
<td>4</td>
<td>6</td>
<td>2</td>
<td>8</td>
<td>10</td>
<td>3</td>
<td>0</td>
<td>1</td>
<td>9</td>
<td>25</td>
<td>81%</td>
</tr>
<tr>
<td><strong>NET GOOD +125°C -55°C</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Good FO = +4 Mk II</td>
<td>28</td>
<td>25</td>
<td>16</td>
<td>3</td>
<td>32</td>
<td>20</td>
<td>19</td>
<td>4</td>
<td>3</td>
<td>12</td>
<td>27</td>
<td>189%</td>
</tr>
<tr>
<td>Good μEE but bad Mk II 25°C FO4</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>-1</td>
<td>0</td>
<td>1</td>
<td>3</td>
<td>0</td>
<td>9 +9 -1</td>
</tr>
<tr>
<td><strong>NET GOOD 25°C FO4</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Good +125°C Not Good 25°C FO4</td>
<td>30</td>
<td>26</td>
<td>17</td>
<td>4</td>
<td>32</td>
<td>21</td>
<td>19</td>
<td>3</td>
<td>3</td>
<td>15</td>
<td>27</td>
<td>197%</td>
</tr>
<tr>
<td>Not Good +125°C Not Good 25°C FO4</td>
<td>4</td>
<td>3</td>
<td>4</td>
<td>3</td>
<td>3</td>
<td>2</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>3</td>
<td>49%</td>
</tr>
<tr>
<td><strong>NET GOOD -55°C</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Good FO = +4 Mk II</td>
<td>30</td>
<td>25</td>
<td>16</td>
<td>3</td>
<td>32</td>
<td>20</td>
<td>19</td>
<td>4</td>
<td>3</td>
<td>12</td>
<td>27</td>
<td>189%</td>
</tr>
<tr>
<td>Good μEE but bad Mk II 25°C FO5</td>
<td>0</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>NET GOOD +125°C -55°C</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total Rejects Units Mk II FO5</td>
<td>43</td>
<td>47</td>
<td>45</td>
<td>40</td>
<td>46</td>
<td>44</td>
<td>48</td>
<td>50</td>
<td>49</td>
<td>35</td>
<td>28</td>
<td>485%</td>
</tr>
<tr>
<td>Verified Marginal Reject Units FO4 &amp; FO5</td>
<td>31</td>
<td>25</td>
<td>26</td>
<td>24</td>
<td>20</td>
<td>17</td>
<td>26</td>
<td>11</td>
<td>12</td>
<td>11</td>
<td>15</td>
<td>228%</td>
</tr>
<tr>
<td>Not Verified, Not Marginal Reject Units</td>
<td>11</td>
<td>22</td>
<td>19</td>
<td>16</td>
<td>26</td>
<td>27</td>
<td>22</td>
<td>30</td>
<td>28</td>
<td>24</td>
<td>13</td>
<td>257%</td>
</tr>
</tbody>
</table>

**Changes by Verification at +25°C**

<table>
<thead>
<tr>
<th>Changes by Verification at +25°C</th>
<th>+2</th>
<th>+1</th>
<th>+1</th>
<th>+3</th>
<th>+2</th>
<th>0</th>
<th>+2</th>
<th>+3</th>
<th>0</th>
<th>+13</th>
</tr>
</thead>
</table>

**Changes by Verification at +55°C & +125°C**

<table>
<thead>
<tr>
<th>Changes by Verification at +55°C &amp; +125°C</th>
<th>+3</th>
<th>+2</th>
<th>+6</th>
<th>+3</th>
<th>+5</th>
<th>+1</th>
<th>+3</th>
<th>+2</th>
<th>+2</th>
<th>+4</th>
</tr>
</thead>
</table>

**Mk II Rejects Iₐ5 (Rₑ MAX)**

| Mk II Rejects Iₐ5, Pass Iₐ5/ₐ₈/OFF | 32  | 41  | 34  | 32  | 30  | 25  | 31  | 21  | 11  | 10  | 278 | 53% |

**Mk II Rejects Iₐ4**

| Mk II Rejects Iₐ₄, Pass Iₐ₄/ₐ₈/OFF | 1   | 4   | 1   | 4   | 0   | 0   | 0   | 0   | 0   | 0   | 10  | 2%  |

**VBE Rejects, Mk II**

| VBE rejects, Mk II | 18/80 | 11/33 | 33/33 | 17/39 | 29 | 30  | 46/49 | 44  | 29 | 22  | 316/34 |

**Verified VBE Rejects 25°C**

| Verified VBE Rejects 25°C | 49/7/16 | 1/17 | 1/17 | 1/12 | 1/8 | 1/9 | 1/10 | 1/9 | 2/11/11 | 1/11 | 2/11/2 | 1/10/1 |

**Verified VBE Rejects -55°C**

| Verified VBE Rejects -55°C | 49/7/16 | 1/17 | 1/17 | 1/12 | 1/8 | 1/9 | 1/10 | 1/9 | 2/11/11 | 1/11 | 2/11/2 | 1/10/1 |

**Mk II Changed Decision**

| Mk II Changed Decision | 4/20 | 2/16 | 2/3 | 2/3 | 2/0 | 0/0 | 0/3 | 0/0 | 0/3 | 0/0 | 12  | 2%  |

**VBE Rejects, Passing VBE Mk II**

| VBE Rejects, Passing VBE Mk II | 3   | 0   | 3   | 0   | 1   | 1   | 0   | 0   | 2   | 0   | 10  | 2%  |

**Probable VBE Rejects (both Pass and Fail Vₐ₈/BE)**

| Probable VBE Rejects (both Pass and Fail Vₐ₈/BE) | 3   | 1   | 7   | 0   | 1   | 8   | 0   | 15  | 3   | 6   | 44  | 8% |

**ALL OTHER REJECTS**

| ALL OTHER REJECTS | 0   | 0   | 0   | 1   | 0   | 1   | 0   | 0   | 1   | 0   | 3   | <1% |

**Good Iₐ₅ Mk II**

| Good Iₐ₅, Bad Vₐ₈ Mk II | 18  | 7   | 14  | 8   | 19  | 25  | 19  | 29  | 11  | 30  | 40  | 220 |

**Good Iₐ₄ Mk II**

| Good Iₐ₄, Bad Vₐ₈ Mk II | 9   | 5   | 10  | 6   | 15  | 19  | 17  | 25  | 9   | 24  | 18  | 128 |

**Good Iₐ₄ Mk II**

| Good Iₐ₄, Bad Vₐ₈ Mk II | 48  | 42  | 49  | 36  | 55  | 50  | 50  | 47  | 41  | 50  | 517 | 98% |

**Good Iₐ₄ Mk II**

| Good Iₐ₄, Bad Vₐ₈ Mk II | 18  | 18  | 30  | 31  | 16  | 21  | 31  | 46  | 44  | 29  | 22  | 316 |

**NOTE 1:** For example, in Run 103, on FO = 5 pass, Mark II rejected 33 units for VBE (V₀), on FO = 4 pass, 31 units. 17 units of the 33 were verified in μEE; 16 were not since prior data indicated very low beta. 15 of 17 were reject in μEE at 25°C; 12 of 17 were verified reject at -55°C. This would be reported as +2 Change by Verification at 25°C and +3 Change by Verification at -55°C, +125°C.
TO:  D. Yost  
FROM:  D. Talbert  

1. Micrologic process is frozen as is.
2. C. Plough's people will test the 11 GB runs to new 25°C specs. This includes FO = 5 and FO = 4.
3. R. Seed's people will test rejects from "2" at -55°C through 125°C to analyze cause. This will also determine additional yield added by temperature testing.
4. C. Plough's people will gather process data from these runs.
5. Epitaxial micrologic will transfer with present R & D process including bar resistors.

DT:af

D. Talbert
Marching meeting - 1/29/63

Date on the first 11 runs of gates (GB) presented and discussed.

The only run that was in the range of desired logins (9.137) was consistent with our original estimate of 50% yield to 75.

Sells propose changing loading factor for GB

<table>
<thead>
<tr>
<th></th>
<th>old μL</th>
<th>new GB</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>3, 4, 5</td>
<td>2.5, 3, 3</td>
</tr>
</tbody>
</table>

If we do this, we will get (with the present mask)

<table>
<thead>
<tr>
<th></th>
<th>μL</th>
<th>CB</th>
<th>Rc</th>
<th>RμL</th>
<th>R = \frac{4U_{in}}{5 I_m} = \frac{5}{1} \text{m}</th>
</tr>
</thead>
<tbody>
<tr>
<td>NOT</td>
<td>10%</td>
<td>36%</td>
<td>670</td>
<td>1.3</td>
<td></td>
</tr>
<tr>
<td>opt for GB</td>
<td>Alt I</td>
<td>35%</td>
<td>86%</td>
<td>640</td>
<td>1.8</td>
</tr>
<tr>
<td>opt for old μL</td>
<td>Alt II</td>
<td>45%</td>
<td>65%</td>
<td>570</td>
<td>1.8</td>
</tr>
</tbody>
</table>

What shall we do about the optimal resistor to be compatible as much as possible with the GB?

- Update our notes.
- Please have summary.

Action items:

- Start mask change - Plough for Alternates I
- Muffar (Cornell) to be starting today.
- Seeds will get a test chip for GB at tomorrow.
- Data sheet revision will be started.
- Plowmen will look at optimal resistor to see if optimum.
- Update at functional testing.

ES " " " 
A. High Power Capability FT-7000

Present production goes at 20-35 watts 20% at 100°C 8.3 kV (5 kV b.i.)

We have made many good 7000's on Fairchild epitaxial material. We have on hand, T.I. and Westinghouse.

Three possibilities:
1. Wide base - to reduce with bulk.
2. Aggregate with limiting resistor - to balance for...
3. Dimer epitaxy - to lower Vc.

I am discussing the possibility of an epic base; it is far from being pointed out that an SCR material (150 volt) get a spread of 5-220.

D. Lamond says that the MIT's View P diffusing system is much more on one on many devices. (Using 100 volts diffusion to get 50% density.)

Price recommends making an epitaxial 6206 designed as an optimum 22 volt unit.

Our power problem:

1. Bailout the region 85 volt, 6200, 6205 to make solid device.

2. Make a power device above 85 volt, deem the 7500.

B. MIT is getting non-gro. device that meet their specs, but they don't like them because of very broadline VCE (AT).

Some similar epitaxy units were made, unfortunately they had too high P mounts, so ran into limiting velocity problems.

Our power problem:
1. Aim at the complement of 85 volt NM, down the 7500.
2. Keep MIT happy.
C. FT-8000 - Make sure there is a significant improvement in sensitivity.

D. High voltage device - proc 2000 V 2000 pΩ.

E. SCR-1 - More a good lamp, high rectified.
   a) IBM part (1025 and similar)
   b) High voltage.

F. SCR-3

---

Question: Which structure to keep?

When will Mt. View be ready?
Rogel says that she is under the impression that generator and outdiffused are nearly equal.

No real information on the medium.

Jack Rabell will get units from the Rogel and try to photoprobe.

Seith mentions that looks good for the first 10 we have so far.

These were made identically with the outdiffused devices, except for a separate grid removed before etching.

Rabell has tested some of these (13 good ones).
FET TESTS IN PROGRESS

A. Variations of oxide characteristics
1. No N⁺ gettering N: — i.e., no P (melted)
2. N⁺ and gettering in single step (almost none, failed)
3. Strip oxide and re-oxidize pyrolytically (of course)
4. Strip oxide and re-oxidize anodically
5. Strip oxide, etch slightly, and re-oxidize anodically (study)
6. Getter and N⁺ pre-dep, pyrolytically oxidize before oxide removal mask (still with)
7. Strip and evaporate SiO₂ (just study)
8. CP-6 etching of failed units to see if failure point has thin oxide

B. To check effect of metal-over-oxide
1. More Otto Leistiko circular units to Mt. View
2. Extra oxide via pyrolytic to minimize possibility of pinhole penetration by metal
3. Chromium metallization (dar + failed)
4. No metal over junction
5. Big base 0-1

C. Miscellaneous tests
1. P channel (unit on failed)
2. Base doping level isolation
3. Surface stabilization
4. No top gate
SHORT SUMMARY OF FET LIFE TEST - January, 1963 (B. Barranger)

The Fet life tests are divided into three groups; Outdiffused, Epitaxial and Special Runs for L. Ragle.

Outdiffused:

The first life test consisting of twenty units from three runs were 100% failures after 12 hours under 30 v reverse bias at 100°C. 10 v leakages ranged from 1 uA to 2 mA, the majority between 100 and 500 uA. Subsequent test of 5 runs under the same conditions were recorded hourly. Within one hour, most unit showed a 100% increase in leakage and within four hours, 80% had leakages over 1 uA. At twelve hours, all but two (of 25 units total) had leakages over 10 uA.

The failure mode appeared to be a classical channel which did not pinch-off completely. With time (and increased leakage) the pinch off became less prominent until it was hardly noticable.

Epitaxial

The first three runs (actually three test wafers) showed a marked improvement over the outdiffused runs. Run # 2 completed a 1000 hour 30 v, 150°C stress without any problems. The other two runs produced failures at various times, anywhere from 50 to 700 hours. All other runs (13 in all) showed 80% failures at various times. Because of space limitation, a run was removed upon reaching 80% failure rate.

The failure mode was similar to the outdiffused except for a more prominent pinch-off. But it too tended to become less prominent with time.

Special Runs from L. Ragle

The only run worth mentioning is # 9 which is gettered with phosphorous rather than nickle. Three groups were received as follows:

(10 units) Group 1. Completed 1000 hours at 30 v, 150°C with no problems.
(10 units) Group 2. Two failures at 100 hours. The eight others completed 1000 hours without other problems.
(10 units) Group 3. 5 of 10 failures up to 130 hours (still in progress)
Short Summary of FET Life Test - January, 1963 (B. Barranger) - continued

Others

Phosphorous vs nickle gettered epitaxial - no difference.

Double-gatted (circular geometry).
Kerrnic generation - Kerrnic Gen.
Skeaker - Oke
Neg resistance gadget - Problem 4
- Green

No one is talking about anything broadband or tunable.
Summary of data

Scale 125°C, 1 ma, Ni + MnNi, got 100% failure.

After... - original

Same 125°C, 1 ma, 15 units, all failed in 100 hours, all 15 units.

The function that goes soft first in the one under forward bias.

From our data:

3/10 @ 100 ma, 125°C for 23 hrs P-got $ & failed

0/6 @ 100 ma, 125°C Ni-got $ failed (72, 34)

Once found to going pink @ 100 ma and 125°C (think it held in a 125°C source problem)

"All this data is on glass encapsulated units.

Of the 3 units we had failed, one had removed after 48 hours

Pulverize at S.R. has done some step stress at various T using I$_2$ as the stress.

At high temp, everything copped out.

Possible problems:

1. The whole package. - Run 1240, 1243, 1253

2. The Ni getting is bad. - Run some Ni came.
The crew of the EOD 6 is in trouble.

These are bad for the mission.

Except for these, conditions don't look good.

Yielding on B4

- from duplex C200
- from "C 100"

"Yield" = \( \frac{7}{4} \), 75%

\( \frac{9}{4.3} \), 90%

No one talks about sensitivity or band-limited multiplexing.

Let the Dept. of Comm. form joint info for Slt.

We must:

a) Center to look at our capability
b) Pick a more specific objective
c) Get our design capability better tied down.
Feb 11, 1963 - Film review
Ref p 50 (Jan 3)

Rickman:

White evaporate fast from a W wire.
Rexy is now using an Inconel wire.

At -330°C substrate temperature Waite made a run that had a very low, very non-uniform over a wafer, say 10-30 a/10 m. It was stiff. Alleging didn't help.

At higher T, during alloy the film goes down in R.

O₂ can be bled in. The more O₂, the greater the change during alloying.

The only encouraging thing is that no runs made at 2 x 10⁻⁵ mbar of H₂ or O₂ changed relatively slightly during alloying.

Rexy agrees on the W evaporated line.
He did come from a vacuum line @ ~ 2 x 10⁻⁵.

The spread is still primarily systematic across a wafer - on all good films.
More known why - is it not too slow due to geometry or film.

Rexy has data on 125°C life test @ 10001/cm² - look good.

Waite has shown that contarte first in part the way it fly - they burn out too soon.

H.R. has reproducibility runs (9 of them covering the whole substrate range, mostly of 350-450°C).
**Title:** Change of resistance of Nichrome resistors during 2min 580°C alloying cycle

<table>
<thead>
<tr>
<th>Run No.</th>
<th>Substance Temp</th>
<th>Vf before alloying</th>
<th>Mean R before all</th>
<th>Mean R after all</th>
<th>10%-99% spread before all</th>
<th>10%-99% spread after all</th>
<th>Mean ΔR: Ratte-Ratte</th>
<th>10 percent of ΔR</th>
<th>90 percent of ΔR</th>
<th>TCR</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>≈ 250°C</td>
<td>40 - 45a</td>
<td>18.9k</td>
<td>17.9k</td>
<td>10.4% (2a) 14%</td>
<td></td>
<td>-5.3%</td>
<td>-7.2%</td>
<td>0%</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>≈ 320°C</td>
<td>31 - 33a</td>
<td>14.3k</td>
<td>12.9k</td>
<td>7.5% 4.5%</td>
<td></td>
<td>-10.1%</td>
<td>-12.2%</td>
<td>-8%</td>
<td></td>
</tr>
<tr>
<td>36</td>
<td>≈ 420°C</td>
<td>24 - 27a</td>
<td>2.01k</td>
<td>2.14k</td>
<td>3.5% 4%</td>
<td></td>
<td>+6%</td>
<td>+5%</td>
<td>+7%</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>≈ 450°C</td>
<td>22 - 24a</td>
<td>9.4k</td>
<td>10.15k</td>
<td>10% (2a) 13%</td>
<td></td>
<td>+10.3%</td>
<td>+7.8%</td>
<td>+13.2%</td>
<td></td>
</tr>
<tr>
<td>38</td>
<td>≈ 500°C</td>
<td>32 - 36a</td>
<td>2.67k</td>
<td>3.01k</td>
<td>3.75% 4.0%</td>
<td></td>
<td>+12.4%</td>
<td>+10.6%</td>
<td>+15.2%</td>
<td></td>
</tr>
</tbody>
</table>
Nichrome films evap. in a residual oxygen atmosphere

<table>
<thead>
<tr>
<th>Run Nr.</th>
<th>Substrate</th>
<th>Temp</th>
<th>O₂- pressure</th>
<th>Mean ρ before all</th>
<th>Mean ρ after all</th>
<th>10% - 90% area before all</th>
<th>10% - 90% area after all</th>
<th>Mean AR after all</th>
<th>10 percentile AR</th>
<th>90 percentile AR</th>
<th>TCR</th>
</tr>
</thead>
<tbody>
<tr>
<td>33-34</td>
<td>Ni-Cr wire</td>
<td>450°C</td>
<td>3.10⁻⁵</td>
<td>41.50</td>
<td>41.50</td>
<td>could not be etched</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>40</td>
<td>Ni-Cr wire</td>
<td>30°C</td>
<td>3.10⁻⁵</td>
<td>600 (5%)</td>
<td>1.15</td>
<td>10%</td>
<td>7%</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>35</td>
<td>Ni-Cr wire</td>
<td>450°C</td>
<td>3.10⁻⁵</td>
<td>1.80</td>
<td>1.56</td>
<td>3.1%</td>
<td>3.2%</td>
<td>-13%</td>
<td>-14%</td>
<td>-12%</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>Tungsten</td>
<td>450°C</td>
<td>3.10⁻⁵</td>
<td>air</td>
<td>3.10</td>
<td>10.8%</td>
<td>-0.7%</td>
<td>+1.6%</td>
<td>170-250</td>
<td>220-260</td>
<td>102</td>
</tr>
<tr>
<td>29</td>
<td>Tungsten</td>
<td>450°C</td>
<td>8.10⁻⁵</td>
<td>8.94</td>
<td>7.14</td>
<td>12.2% (2a)</td>
<td>9.9%</td>
<td>-21.5%</td>
<td>-20%</td>
<td>-23.4%</td>
<td>102</td>
</tr>
</tbody>
</table>
Reproducibility: Best point looks like evaporation from a Ni on a "pure" vacuum at ~ 400°C substrate, H.R.

Process quantity: (good wink)

Null hypothesis: It is due to a dirty vacuum system.

Hypothesis: Use H.R. jig in various systems for good comparison.

Effect of crude order — those that have been thinning something out.

Variation across wafer.

Potato: It is geometry.

Experiment:
1) Measure geometry on Ni across wafer
2) Compare data of the different wafers, wafer.

It would be useful to measure different resistor variation across the wafer and to life but these H.R. will come with QPf on the advisability of doing this.
Feb 11, 1963 - Funtanil Vapor Etch

Clean up the old solvency system to get rid of everything in the way of problems.

Measure ratio and perfection of films.

Other films, cont 2/11/63

B. Beem closed oxide (V1 = 30)
Diffused for 1 hr total (15 min by 15 min wet)

1000°F, 750°F, 20 min get 2.33× (balanced, high green)

We ~ 100% for pure oxide.

P. closed oxide (P0 for V1 = 0.7-0.9)
Diffused @ 1000°F for jet process

1000°F, 750°F, 20 min get ≤ 184% Applied looks pretty good.

There has been no problem with the NFR - no problem.

Problem:
1. Contamination without analyng
2. Aligned with X-killing best treatment
3. No lost data
4. How do it with 2 grain oxide
Feb 11, 1963 - Other film resistors

- 1. S: thin film
- 2. Coned
- 3. SnO2
- 4. TaN

TaN + SnO2 are unstable as espotted.
SnO2 will stabilize @ ~900C. Film is from Sn+77%Bi.
SnO2: After we went to do any more, we decided to spray.
Tantalum can (+W) coat 'bipolar' S', surface. - We will send some.

TaN: Still too early to tell. We are way off on p, ~10^-5 off - ten times.

Corona: Ca+SiO2
On early tests one separate source by electron bombardment:
Now we have flash evaporation from a heated TaO (or Al) boat.
p in 10^-7 on range.

Problem:
1. Etching
2. Bad change on heat cycling - down 50% or so.

Possibly some spike allowing combined with a subsequent anneal to
value & will try it.

Si thin film:
550°, 750°, 850°, 950° reaction temperature
At 550° got a uniform film which shows
they do both thin and at 650.
Film is quite good, but perform poorly.

At higher temperature the film look terrible
After in an environment for greatly different 2.0 arthritis,
Outside need forming.

One run came thin that required no forming.
Some runs, for 8 hr @ 500°, no - almost no change.
Out of Wolfer, the largest change from ~5%.
Meeting again tomorrow

Manpower - add a girl.

An interesting point comes.

We will take the periodics even down further.

Optical java:

Art Engvall will examine the economics and see if changes can be made, instead of cost.

You will recommend on a mark check program.
This has problems of vapor action. By Au doping this can be made small, but leakage goes up to 1% and probably an undesirable level.

New structure

Using this structure a BCD matrix as can get it @ 500 V/m.

It showed the other polarity for compatibility with process. This begins to settle some problems for logic because it makes the ground line the SB difference before exiting which is too long. Especially because the input must be 10%, long.

No good diodes were found here and yet been made.

I feel this project is useful, but much more useful is to put pipe on the Dev. Rev. section is the IBM shift an old project.

At 1596.

In the run out, an all forego seem from 500 - 1000 mm and 99.8% count myself kept pieces don't fit together, relation of the problem.

Some life test done on forego (A.)
Feb 13, 1963 - Join Angel Sundown on Adaptive Systems

This can also be done on the a film with existing back...

...plein plate is probably a fundamental...and does not this.

It turns out that these are many companies are doing adaptive...even the magnetic array takes -1/n^2/2 - i.e., 30% on tape sand core.

Possible uses:
1. Voice control to a computer (e.g., automatic computer)
Self Organizing Systems - 1962

Contents
1. The Organization of Organization
   O. G. Selfridge - Lincoln Lab.
2. On Self Organizational Systems
   V. D. Mesarovic - Systems Research Center
   Case Institute
3. Self Organization in the Time Domain
   D. M. MacKay - University of Keele
   England
4. Neurological Models & Integrative Processes
   W.S. McCalloch, Arbel, Cowan - RLE, M.I.T.
5. Information Input Overload
   J. G. Muller - Mental Health Research Institute
   University of Michigan
6. Internation Simulation: An Example of A Self-OS.
   H. Lutkyow

7. On the Automatic Formation of a Computer Program Which Represents a Theory
   Saul Amarel

8. Optimization Through Evolution & Recombination
   H. J. Bremermann

9. Natural and Artificial Synapses
   L. D. Harmon

10. On Probabilistic Push-Down Storages
    M P Schützenberger

11. Concerning Efficient Adaptive Systems
    John H. Holland

Northwestern University
RCA Labs.

Math Dept
U of Cal, Berkeley

BTL - Mich.

Harvard Med School

Communications Technical Lab.
U of Michigan
L. Brillouin
Columbia U.

13. Majority Logic and Problems of Probabilistic Behavior
Saburo Muroga
IBM Research.

14. Interaction Between a Group of Subjects and an Electronic Automation
 to Produce a DOS for Decision Making
Gordon ankles
(System Research Ltd.)
England

15. Cybernetic Ontology and Transcendental Operations
Gottwald Dinesche
Elec Eng Res Lab, U of Illinois

16. Some Problems of Basic Organization in Problem-Solving Programs
Allen Newell
Carnegie Inst of Tech.

17. Training Sequences for Mechanized Induction
R. J. Solomonoff
Gator Company, Calif.

18. Adalines - BW
SU

19. A Comparison of Several Perception Models
Frank Rosenblatt
Cornell U.

20. A New Class of Multilayer Series-Coupled Perceptions
Alan D. Konheim
IBM Research.
21. A Test for Linear Separability As Applied to Self Organizing Machines
   Richard C. Singleton

22. Function Algebra and Propositional Calculus
   Karl Meyer
   Illinois Tech

23. Some Similarities Between the Behavior of a Neural Network Model & Electrophysiological Experiments
   B. C. Forsey
   Frieder Lab
1962, COSOS

Lincoln, MIT, III
Case
England
Michigan U
Northwestern
RCA
Cal Berkeley
BTL
Harvard
Columbia
IBM
Cornell
Illinois
Stanford-SRI
Carnegie
jali
I. General Information

2. Testing (counseling)

3. Demographic - General example - Example of counseling

4. Rating Restriction - Reduce, etc.

5. Procedure: 

   - Four-card sorting, face-down, face-up, etc.

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III Implementation
A. Transistor
   & E set
   Aeronesonics 2nd
   SRI (Ted Brain)
B. SHAMAC (Crafton)
   SU
   SRI
   Cornell-Rosenblatt
   Matrix
   Thin Films
C. Memistor
   SU - MC
D. Diode - not very promising
   BTL - TRE out of business
E. Speculation
   Fieldode - RCA
   Reversible Path - SU (Beadle) Sandia, Spex-General
   Heber Nash - SU
   Ferroelectric - Pulvar, Holl
F. Neuistor
   Melpar
   SRI
   SU
IV  Digital simulations - definitely an important competitor

5 U
Lockheed - Melcor
IBM - Well have at 50

II  Hardware simulations
BTL - Harmon
Adaptive
Acton
Melpar

II  COSOS projects - readings edited by Yorita

III  Theory - non adaptive implementation
Philco  (Post Office)
RCA
IBM
Melpar
MIT
Pamigee  Problem Solvers
Prentice
Feb 13

Date: 4/4/44

Data on hole

100 psi, 125 °, glass in hole, $, a, $.

<p>| | | | |</p>
<table>
<thead>
<tr>
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<tbody>
<tr>
<td></td>
<td>glass</td>
<td>f-settled</td>
<td></td>
</tr>
<tr>
<td>$</td>
<td>&quot;</td>
<td>Ni</td>
<td>0</td>
</tr>
<tr>
<td>AS</td>
<td>&quot;</td>
<td>Moke</td>
<td>1</td>
</tr>
<tr>
<td>AS</td>
<td>10-5</td>
<td>none</td>
<td>1</td>
</tr>
</tbody>
</table>

12 after 45 min.
No failure out 110
7 out of 10
7 out of 110

(2 normal stream temp)

(5 normal stream temp)
Epitaxial defects 2/18/63

Summary

Pyramidal raised triangle came after growth (defect). The low defect S.P.
A hole defect can be found crystallographically.

'P' from an impurity or substrate

1. SiO₂ as evaporated anodic film, 200 Å thick, at the hole, in the
oxide growth of P is along. The hole came from voids - 10% inferior.

2. 200 Å SiO₂ anodic laver over Pt is then an ordinary laver.

3. SiO₂ as anode or to a much poluted anode gave Pt's like the film.

4. Themed steel pits (made in A in a different manner) on Pt's, but it stills the defect
that lave like

5. N. themed steel pits did not make Pt's

6. Al₂O₃ - 3Pt - loosed with Pt's

7. Mg +

8. SiC

9. Ni

10. Copper was residues shown some

11. CaCO₃ + NaOH & CaO + will make Pt's, but especially a lot of axial triangle

12. Chemical steel pits are small manehines, for many exagles.

In any case, we still have a Pt problem. Even on our best films we saw a few per wafer on the average.
We will not be satisfied until there is < 0.1 per run.
INTERNAL CORRESPONDENCE

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

TO: Distribution  
DATE: February 18, 1963  

FROM: V. H. Grinich  

CC: G. E. Moore

SUBJECT: Microcircuitry
Minutes of Meeting held February 18, 1963

In order to minimize the amount of repetition we will review action items that were discussed at the January 29th meeting on μL Review and then proceed on to new business.

Items from μL review held January 29, 1963

Policy Decisions 1 and 2: The two policy decisions that were stated in the minutes of the January 29 meeting were re-emphasized and all parties agreed to it. In addition it was stated that we would closely evaluate the epitaxial versions of μL elements by means of bringing out a lead from the base of at least one transistor in order to monitor resistance, and also to get a closer handle on transistor characteristics.

This will allow us to establish a base for any further modifications that may be deemed desirable.

Action Items from January 29 minutes

Item 1) 10 units of the GBY elements (double dog bone resistors) were evaluated with good results in regard to resistance ratios and turn on voltage. GBZ, SBZ and HBZ masks exist (these are hybrid resistors with some dog bone and some slip contact resistors). 40% classifications yield has been obtained with the SBZ, however. SBYs, HBYs and other of the family will be stepped as soon as the GBY units are completely evaluated. This is all being done through Mountain View in Production and Applications Engineering.

Item 2) Epitaxial material was supplied to Mountain View from R & D. However, due to Mountain View's other commitments they did not feed back information or take the data as to die sort yield for the epitaxial "S" element. Yields on present HSG-3 epitaxial units are 50-80% hard breakdown at $V_{CC} = 5V$.

Item 3) Completed by Applications Engineering.

Item 4) Work under way by Applications Engineering.

Item 5) The present minimum geometry layout will be evaluated before any modifications are considered.

Item 6) Work order in process.

Item 7) SBY units need to be evaluated before this can be recorded.

Item 8) Epitaxial material was sent to Mountain View as discussed under Item 2. New runs are near die sort in R & D.
The following new business was discussed:

1) Current Mode Logic Gate is at metallizing.

2) Discussion of new design for higher speed current mode gate was concluded with a decision that we will bring out extender tabs on both sides of the present current mode gate in order to evaluate ways of getting temperature compensation within each device, and at the same time allow us to operate with a 500Ω in place of a 5000Ω resistor. We expect to be able to get with this new circuit at 1200 µV dissipation 3.5 nsec delay for a fan out of 1 and 7.5 nsec for a fan out of 5.

3) Discussion of yield on DPD circuits showed the following results have been obtained in Mountain View. For the R element with 40 wafers into the line, 12 wafers made it to metallizing, giving 96 devices at pre-sort from which 14 finished units were accepted by DPD. For the adder circuit 440 wafers provided 39 finished units; for the four input gate 220 wafers provided 147 finished units. Before we make any epitaxial masks for the DPD circuits we will get more yield information on the epitaxial S element.

4) Discussion of the binary circuit using storage diode steering indicates that we have some problems in getting a tight control with both a minimum and maximum on the diode storage time. It appears that we will need 10 microns collector region thickness (distance from diode junction to isolation junction) in order to obtain 100 nsec effective life time. Some minimum beta on the pnp transistor is a sufficient condition to imply we have the life time but because of emitter efficiency effects it may not be a necessary condition.

There will not be a Microcircuitry meeting on Monday, February 25. Notice will be sent out prior to the next meeting so there will be no mixup.
Jennie would like to continue to track down the cause.

1. Other contamination
2. Thin film around a known contaminant.

Yim:

Washing in J film growth with a 10 min slow step, 0.1-0.4 rpm.

A density independent of T growth.

We will observe stacking faults in order to see if we can see any correlation.
Section Meeting 2/9/65

The S/R camera has been frozen to small (10 x 10 mil) plates now.

We are going to try some Scottish green for large plates coming out.

Some Belgian plate are being tried.
# Weekly New Product Status Report

**Small Geometry Section**

**Received:** W/E 2/17/63

**FEB 18 1963**

**GORDON E. MOORE**

<table>
<thead>
<tr>
<th>Project</th>
<th>Engineer</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>3111</td>
<td>Botte</td>
<td>APPLICATIONS STILL EVALUATING THE MOST RECENT RUNS. القرينة IS DEFINITELY OUR BIGGEST PROBLEM ON THIS DEVICE. RESULTS FROM 1050°C COLD DIFFUSED AND PYROLYTICALLY OXIDIZED RUNS SHOULD BE AVAILABLE BY 2/25/63. APPLICATIONS LIFE TEST DATA ON RUN #6 SHOW NO FAILURES AFTER 500 HRS.</td>
</tr>
<tr>
<td>0000/1</td>
<td>Shanken</td>
<td>NON-EPITAXIAL 0000'S (5.1-5.6 52 cm) STARTED IN 12/11/63 GROUP DURING THE WEEK. FIRST RUNS SHOULD BE AT DIE SORT BY 3/1/63 AND AT CLASSIFICATION BY 3/15/63.</td>
</tr>
</tbody>
</table>

CC: T. Say
    V. Grunich
    G. Moore
    C. Spoor
    D. Yost
    B. Shultz
    B. Knudsen
    P. Keegun

R. Graham
W. Richmond
R. Cole
P. Himst

Date Revised 2/18/63

Signed [Signature]
<table>
<thead>
<tr>
<th>No.</th>
<th>Name</th>
<th>Status</th>
</tr>
</thead>
</table>
| 0002 | Roter | First Mt. View run will be at die sort on 2/19/63. It was made using material manufactured at Sterling Co and looked quite good at T-84. At least 2 more FSC runs should reach die sort by the end of the week. The last 5 runs started at R-0 (using Merck wafers) gave practically no yield at die sort and the 2 Merck runs in process at Mt. View also look bad. The exact problem with the Merck material has not been determined as yet. Life test on the 0002 is behind schedule due to problems in applications.
TO: D. Yost  
FROM: P. Lamond  
SUBJECT: NEW PRODUCTS SCHEDULE - SMALL GEOMETRY SECTION  

The following is an updated schedule for the introduction of new products in the Small Geometry area:

<table>
<thead>
<tr>
<th>Product</th>
<th>Dates</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000/1 AG C &amp; RF</td>
<td>2-11-63</td>
</tr>
<tr>
<td>1340/41 Replacement</td>
<td>5-1-63</td>
</tr>
<tr>
<td>3 x 1312 TO5 -5 leads</td>
<td>5-1-63</td>
</tr>
<tr>
<td>0008 T.F.D.</td>
<td>6-1-63</td>
</tr>
<tr>
<td>I.B.M. S.C.R.</td>
<td>8-1-63</td>
</tr>
</tbody>
</table>

Product in M.V.

| 2-11-63  | 5-1-63  | 5-1-63  | 6-30-63 | 8-30-63 |

PL:af

2/11/63

cc: C. Sporck  
J. Sentous  
J. P. Ferguson (R&D)
The product planning meeting

From Bingham and Austin - 2/11/63

Order into lead & 2/11
1340/41 replacement
3 x 1312 - 105-5 leads & C6
000 & T.E.D.
26M & S.F.R.

12/21 - ?
1/50 - any of bought up.

"The student"
3111 - flying

We should plan the student family.

FET's - not sunk crew

P.N.P.

*1511
1713 - buy for trouble, but now little use. Rating problem for 1702?
3511 - both good
1702 - bring up.
2500 - note and complete like your ?

6205
6006
7000

Super Stor

4116 - 4201

S.C.R - I.B.M.
- H.U.
Pre-meeting notes

1. Simple cut and backfill

   a. cut
   b. mask metal stack
   c. rinse stack
   d. grow epitaxial
   e. 

2. Cut and backfill with an additional diffusion step between D and E

   D1. 
   D. 
   D1. 
   D. 

   This one has the potential problem of not allowing adequate cleanup between diffusion and growth.

3. Cut and backfill, controlled doping

   D. grow heavy n-type (As doped)
   D. doped to lightly doped
**ENGINEERING DATA**

<table>
<thead>
<tr>
<th>RUN</th>
<th>WATER</th>
<th>YIELD</th>
<th>YIELD</th>
<th>TYPICAL</th>
<th>TYPICAL</th>
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<tr>
<td></td>
<td></td>
<td>NECO</td>
<td>NECO</td>
<td>hfe</td>
<td>LVCN</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>@ 5V</td>
<td>&lt;100uA</td>
<td>5mA</td>
<td>5mA</td>
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<th>DE.</th>
<th>OP.</th>
<th>GR.</th>
<th>TYPE No.</th>
<th>CL.</th>
<th>TE.</th>
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<th>DATE</th>
<th>ELAPSED</th>
<th>SP.</th>
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<th>YIELD</th>
<th>TYPICAL</th>
<th>TYPICAL</th>
<th>X:</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>NECO</td>
<td>NECO</td>
<td>hfe</td>
<td>LVCN</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>@ 5V</td>
<td>&lt;100uA</td>
<td>5mA</td>
<td>5mA</td>
<td></td>
</tr>
</tbody>
</table>

**REMARKS**
Metallized Water yield Group: (Epitaxial Gate)
<table>
<thead>
<tr>
<th>Run Unit No.</th>
<th>Wafer No.</th>
<th>Yield Iceo &lt;10mA @ 5V</th>
<th>Yield Iceo &lt;100mA @ 5V</th>
<th>Typical hFE 5mA</th>
<th>Typical LVFe hFE 5mA</th>
<th>Xi Epitaxial Layer Thickness (Mg)</th>
</tr>
</thead>
<tbody>
<tr>
<td>HSG3-15</td>
<td>A</td>
<td>46</td>
<td>52</td>
<td>60-160</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td></td>
<td>B</td>
<td>42</td>
<td>51</td>
<td>50-170</td>
<td>13</td>
<td></td>
</tr>
<tr>
<td></td>
<td>C</td>
<td>60</td>
<td>64</td>
<td>55-65</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>A</td>
<td>42</td>
<td>42</td>
<td>80-100</td>
<td>13</td>
<td></td>
</tr>
<tr>
<td></td>
<td>B</td>
<td>75</td>
<td>78</td>
<td>70-100</td>
<td>18</td>
<td></td>
</tr>
<tr>
<td></td>
<td>C</td>
<td>62</td>
<td>67</td>
<td>-</td>
<td>14</td>
<td>34-38 Mv</td>
</tr>
<tr>
<td></td>
<td>D</td>
<td>68</td>
<td>61</td>
<td>50</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td></td>
<td>E</td>
<td>68</td>
<td>86</td>
<td>80-100</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>X</td>
<td>0</td>
<td>0</td>
<td>~200</td>
<td>2-4 Mv</td>
<td>27 Mv</td>
</tr>
<tr>
<td></td>
<td>Y</td>
<td>0</td>
<td>0</td>
<td>~200</td>
<td>2-4 Mv</td>
<td></td>
</tr>
</tbody>
</table>

These yields include all wafers which reached alloy except first three runs.
Yin:

A. Draw junctions

- Label 0.2 cm p substrate
- 0.3 cm n from 5-9
- 3µ of 1.5 cm

Get "black" more closer to a - 80% of 10cm long
These are grown for FET people - no feed back

B. 0.2 µ 0.1 µ 0.02 p - type substrate
- Grow 1.5 cm in n
- 0.5 cm in p

Get 8-16 "line"
- 2.5 - 3.5 µ "width"
- (2000 - 4000 µ² cm⁻² cm⁻¹ cm⁻¹)

Get BL if 100 cm c.h., 10-20 cm other

On 4 X section, only one drawn parallel junction. The collector, emitter all on the map

C. 12 cm N

- 1.2 cm P 5-10 µ
- 12 cm N (3µ)

do nickel diffusion N+ grid
- Grow 4-5 µ of 1-2 µ cm N type
- P - type nickel

D. Many other diffused or grown structure
- Grow 10 µ of 0.572 cm N

- fork make
Epi structure, cat
FET

After growth there is some evidence of lateral growth.

There are detailed run photos on everything.

On end matching, problem in the oxide as a problem.

Oxidemetal structure:

None have been done on cat and fill.

Things we would like:

1. Cut and backfill, put with light doping, large gentle (see p. 90), own dif. epitaxial insulating layer

2. Grow GaAs for test later

3. Insure epitaxial for proper Xtra

4. Pour Xtra - need 35 psi, for metal, each problem

5. Upscale Xtra Xtras (will grow different layer)

This is an important device in my activity.

6. 600 psi, very close control of aluminum. Melt diffusion

7. Study P N-type growth, > 200 ohm

8. Cut and backfill for isolation
Agenda for Project Review Meeting

Tuesday-2/26, 9:00 a.m.
Special Epitaxial Device Structures

The purpose of the meeting is to discuss and plan efforts to make advanced device structures not presently needed specifically by device development projects, but of interest when capability is established.

Agenda:

9:00 Wigton & Yim on special structures that have been made with photos and data.

9:30 Group discussion of other structures of interest.

10:30 Preparation of plan to make certain structures and assignment of device development responsibility to evaluate or use after structures have been shown feasible.

11:00 Adjournment

Please have all data summarized for efficient presentation.

List: (Participants)

A. Davis
P. Ferguson (3)
V. Grinich
T. Sah
H. Wigton
E. Yim

GEM: hb
<table>
<thead>
<tr>
<th>Exp'nt No.</th>
<th>Objective</th>
<th>Method</th>
<th>Decision to Make</th>
<th>Results</th>
<th>Analysis and Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Determine pipe density and oxide thickness as pipe increments during processing.</td>
<td>Use 3, 5, and 7 fringes thicknesses, and observe pipe density as processing proceeds.</td>
<td>Relation of 0, thickness to pipe density or pipe occurrence at various processing stages. (4200)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.</td>
<td>Determine effects of oxide cut out slopes as dopant barrier at junction areas.</td>
<td>Use sloped and sharp oxide cut-outs, observing differences in pipe density as processing proceeds.</td>
<td>Relation of oxide cutout sharpness as dopant barrier in junction areas. (4200)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3.</td>
<td>Determine if boron doped oxide is permitting faster diffusion of phosphorous than believed, such that doped oxide is not an efficient phosphorous mask.</td>
<td>Compare original boron doped oxide pipe density with stripped and regrown oxide after base and emitter diffusion.</td>
<td>Effectiveness of doped oxide as a mask against phosphorous. (4200)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4.</td>
<td>Determine if a thick oxide before boron doping of oxide is effective as oxide mask against phosphorous doping (compliment to Exp'nt 3).</td>
<td>Compare thick and thin oxides for pipe density after phosphorous diffusion.</td>
<td>Effectiveness of oxide thickness as compensation against phosphorous penetration of boron doped oxide. (4200)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5.</td>
<td>Determine if pipes near junction not detected in early processing expand by lateral diffusion into junction area.</td>
<td>Arrange oxide-steam time cycle to yield equal 0, thickness, but different X, and longer diffusion times of two groups, forcing lateral expansion of &quot;close-in&quot; pipes into junction area.</td>
<td>Magnitude of &quot;close-in&quot; pipes not detected at base diffusion on completed device. (4200)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6.</td>
<td>Determine amount of pipe-type contamination is associated with Ni plating operations.</td>
<td>Compare groups with Ni plated vs. no nickel, and Ni plated vs. Ni evaporation.</td>
<td>Magnitude of pipe generation associated with Ni plate solutions and possible alternate nickeling procedures.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### NPN Simplification Process

<table>
<thead>
<tr>
<th>Original Objectives</th>
<th>Process Steps</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. High Yield</td>
<td>1. Diffusion</td>
<td>2. Std. Diffusion</td>
</tr>
<tr>
<td></td>
<td>4. Ambient</td>
<td>4. Bad</td>
</tr>
</tbody>
</table>

**Method used**

1. ALL Std Diffusion Practices
2. ALL Std Masking Practices
3. No in process testing or cleaning, Cycle time = 5 days
4. Waters YPR Coated when not in Furnace

**Results**

1. Yield As Good or Better than Std.
2. Cost Low, due to Yield and Short Process time
**NPN Simplification Process  12-31-62**

No in Process testing or cleaning

Total Time Cycle For Wafer Fab = 5 days

<table>
<thead>
<tr>
<th>Item</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Run size will be equal to Base Pre-dep. Limit</td>
</tr>
<tr>
<td>2.</td>
<td>Will be loaded direct to oxidation boat</td>
</tr>
<tr>
<td>3.</td>
<td>Steam flux cleaned for each run</td>
</tr>
<tr>
<td>4.</td>
<td>Air dry in dark, dust free container</td>
</tr>
<tr>
<td>5.</td>
<td>Masking operators start at 0600</td>
</tr>
<tr>
<td>6.</td>
<td>Base Pre-dep boat loading done in masking room and carried under cover into furnace</td>
</tr>
<tr>
<td>7-8</td>
<td>Std. Process</td>
</tr>
<tr>
<td>9</td>
<td>Same as #4</td>
</tr>
<tr>
<td>10</td>
<td>New Mask</td>
</tr>
<tr>
<td>11</td>
<td>Under cover direct from 2nd mask</td>
</tr>
<tr>
<td>12</td>
<td>K.P.R Nickel process in place of Black wax</td>
</tr>
<tr>
<td>15</td>
<td>Direct to Topside metal, no testing</td>
</tr>
<tr>
<td>16</td>
<td>Rough Al metal system</td>
</tr>
<tr>
<td>17</td>
<td>Same as #4</td>
</tr>
<tr>
<td>19</td>
<td>Only testing station in process</td>
</tr>
</tbody>
</table>
NPN Simplification Process

1 to 4 Continuous Same day

1. Run Make Up
2. Etch CPb
3. Oxidize 1220°C 1 HR.
4. KPR Spin Dry

5 to 9 Continuous Same day

5. 1st Mask
6. Base Pre-dep M. Borate
7. 10:1 HF
8. Base Diff
9. KPR Spin Dry

10 to 14 Continuous Same day

10. 2nd Mask
11. Emitter Pre-dep
12. KPR No wax Nickel System
13. Diff 40
14. KPR Spin Dry

15 to 17 Continuous

15. 3rd Mask
16. Rough Top metal
17. KPR Spin Dry

18. KPR Mask + Alloy

19. Test 84
NPN Ni Plate

1. 2nd Mask
2. Dry 1/2 HR
3. P305 Pre dep
4. 5 min Running DI water
5. 5 min Spin Dry

30 c/s KPR Coat
6. Dry 5 min 90°C
7. Expose 10" mev 20" CA
8. Dev. std.
9. Dry 20 min

Bake 160°C 25 min
10. Oxide Etch 2 min
11. KPR Clean
12. Ni 93°+ 1 min
13. DIFF 40
# Simple Process

**Die Sort Sample BY 4200 Line**

<table>
<thead>
<tr>
<th>Run #</th>
<th>Die In</th>
<th>E.C</th>
<th>E.B</th>
<th>Soft</th>
<th>Pipes</th>
<th>Good</th>
<th>%</th>
<th>Factory Ave</th>
</tr>
</thead>
<tbody>
<tr>
<td>EK #1</td>
<td>531</td>
<td>25</td>
<td>20</td>
<td>57</td>
<td>132</td>
<td>297</td>
<td>59</td>
<td>38</td>
</tr>
<tr>
<td>EK #2</td>
<td>412</td>
<td>60</td>
<td>6</td>
<td>54</td>
<td>132</td>
<td>160</td>
<td>38</td>
<td>34</td>
</tr>
<tr>
<td>EK #3</td>
<td>210</td>
<td>17</td>
<td>1</td>
<td>5</td>
<td>83</td>
<td>104</td>
<td>49</td>
<td>32</td>
</tr>
<tr>
<td>EK 4A</td>
<td>400</td>
<td>-</td>
<td>3</td>
<td>15</td>
<td>185</td>
<td>187</td>
<td>46</td>
<td>34</td>
</tr>
<tr>
<td>EK 4B</td>
<td>400</td>
<td>10</td>
<td>5</td>
<td>15</td>
<td>150</td>
<td>220</td>
<td>55</td>
<td>34</td>
</tr>
<tr>
<td>EK 5A</td>
<td>300</td>
<td>34</td>
<td>8</td>
<td>91</td>
<td>98</td>
<td>119</td>
<td>39</td>
<td>31</td>
</tr>
<tr>
<td>EK 5B</td>
<td>602</td>
<td>75</td>
<td>10</td>
<td>43</td>
<td>154</td>
<td>319</td>
<td>53</td>
<td></td>
</tr>
</tbody>
</table>

**Exc 6** Rejected After Emitter Pre-dep

**Exc 7** /

**Exc 8** Rejected After Emitter Pre-dep

**Exc 9**

**Exc 10**
### Simple Process to Std. 4200 Process

**ALL Die Sort Data Obtained BY 4200 Line**

<table>
<thead>
<tr>
<th>Week of</th>
<th>Die Sort Percent</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-8-63</td>
<td>Std Die Sort</td>
</tr>
<tr>
<td>1-7-63</td>
<td>Std Die Sort</td>
</tr>
<tr>
<td>1-14-63</td>
<td>Std Die Sort</td>
</tr>
<tr>
<td>1-21-63</td>
<td>Std Die Sort</td>
</tr>
<tr>
<td>1-28-63</td>
<td>Std Die Sort</td>
</tr>
</tbody>
</table>

Simple Process =
Simple Process to Std. 4200 Process

All Die Sort Data BY 4200 Line

<table>
<thead>
<tr>
<th>Week</th>
<th>Die Sort Percent</th>
</tr>
</thead>
<tbody>
<tr>
<td>04</td>
<td></td>
</tr>
</tbody>
</table>

2-11-63

Std Die Sort
Paul presented a pipe picture in his report.

Sang

From data on oxide thickness, etc., a run was made to try seals, oxides, etc. A die cast yield of 62% was obtained.

Production has a very good condition for hearth v. removable pipe.

Control flow with minimal process - mean residence time

The percentage of pipe in die residue is then

Percent of rejects: 10%

Agenda for: Paul Hill and I will get together to discuss an agenda for a meeting in a week.
Feb 26, 1963  

1. What is the effect of Ga.

The Ga cycle: (due after 2nd week)

5 min present in N2

Table below compares Ni and 50 µm

<table>
<thead>
<tr>
<th>Cycle</th>
<th>5 min</th>
<th>10 min</th>
<th>20 min</th>
<th>30 min</th>
<th>40 min</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 - Na</td>
<td>1.3</td>
<td>1.5</td>
<td>1.8</td>
<td>2.0</td>
<td>2.5</td>
</tr>
<tr>
<td>0 - N2</td>
<td>0.3</td>
<td>0.4</td>
<td>0.6</td>
<td>0.8</td>
<td>1.0</td>
</tr>
</tbody>
</table>

Other cells similarly - long. 3rd cycle, 100.

Table: Ga cycle completed in 25 min @ 60 V, 1 V/min - see above table.

Typically 10 to 15 min treatment, down again on alloy.

2. Oxide trimming.

A 0.1 line per curve-twin nickel content, but they are thin.

From 1/16 to 7/16 (256 cm)
maintain 10V, 90 V, 2/16

3. Detects power.

5+ 90 V, 2/16
The purpose of the meeting is to review the effects of structural changes which have been made and evaluated in planar PNP devices in an attempt to eliminate the channel problem and planning of program to evaluate other structural changes in the light of various models of channel causes.

**Agenda:**

3:30 Statement of problem and review of prehistoric data - (Moore).

3:40 Review of more recent data on oxide cut and gallium treatment - (Carlson).

4:00 Summary of life testing results with respect to channels on 1740 and 4511 - (Reis or Grutchfield).

4:30 Discussion of other hard data from group.

4:40 Discussion to generate structural changes worth considering from group.

5:00 Preparation of plan to make and evaluate recommended structural changes.

Please have all data summarized for efficient presentation.

GEM:hb
List: (Participants)
L. Carlson
P. Ferguson (3)
V. Grinich
H. Grutchfield
L. Reis
T. Sah (3)
A man is about to lose effort - amid understanding, not it for PNP for competence.

40°F solution
Active that program - an positive.
The double peak is not associated with twinned oxide.

3. Of 10 units with twinned cathode only (60 Epp - 50) 5 developed 0.1-0.3 µm channels, during life.

Intensification

1740 - 1741 The only channel he has seen were when Ba was properly left out.

4511 Or O2 stream, form 100°C, reduced form 180°C, CB bias.

All of our PNP's were put in same condition. Only BS 4511 and 1712 developed problems.

The Ba treated units show a large increase of low current decrease aging (e.g. 100°C, 300°C).

4511 (heating)

At one channel by poor lift elements them by 50°C age.

A lot of the channel get to be

(trip could cause a poor lift effect)

Competition coming - T.I. / AFC - growing - large channel, don't grow.

Fang has done a run that was 100 metal, no Ba and low (no problem?) yet. There are 1741 200,000 m, 200, 300°C at age. These run on the 20-30°C range mostly with a few to 60°C.

Heat treatment in 100°C. After young diffusing step.

All into 5; before diffusion. No good result.

Positive Antidi after channel. 

Morphol - no mull.

We might have morphol (no 4511 in to try - had.

Chemical
Small Geometric product planning  Feb 27, 1963

1312 - This has a 150° C Icc pattern. This is evidently common to all optical units.

Other problem are only getting 70% of 150° C spec. They can't be correlated out.

1311 - Not Icc isn't meet 170° C -about 10% fail this 150° C spec. There can't be correlated out.

1211 - Wiped out completely on 1st Icc in this.

1210 n must be made again.

3111 - A basic open today. It has a lot Icc pattern.

- 30°C CEO
- 60°C 450
- 500mA 3.5ms
- 10
- 450sec 40ms off
- 200 sec, 150° C Icc

We feel this, we must step on CEO 750 off.

On 20-30 volt units will meet all the closedoff issue.

0000 - There is an optical material problem. On nothing but our REO first material non other a good yield.

0000 - Not being taped at Medliner, but die will be out on 3/9 and shipped Monday.

We go to CEO's in plates by 9:50

Make same in WR package.

... - Wait for strip line package.

121 - Nothing but evaluation of what we now have.

1450 - doesn't look like much, I don't see it.

40-100 at 100% yield (O.C. 3). If we look at O.C. 3, it looks good at 100 yrs. U.H. thinks it should fly.

1250 - Fly

1340, 1341 - Worth like a cast saline solution in 70% method.

Our best yield of 1340 is 40 to yield to 2N705.
COC are down - no good. We will make a mask for an intermediate. We will change, maybe, nothing else.

PNP

4571
3511
1713

4571 - Want Monitran devices can take 40 or 80 V, LUCEO.
We will run some 40 or 80. You will get some that have developed channels in Photos and work.
There is a real potential problem in LUCEO in the glass package.

3511 - A production product 2N2695, 2N2696.

1713 - It is producible @ 1.5 of 400 V, 6, 000 m.

400 m, 15 @ 2.2
700 m, 15 @ 2.5
800 m, 15 @ 3.0
1200 m, 15 @ 3.5
1600 m, 15 @ 4.0
1800 m, 15 @ 4.5

165°C ambient, 100 or 180. The developed small channels.

1702 - Wait until we find out what held acceptance
in. We just a few more one 1713.

6205 - Dead
6206 - 80 or LVCEO 15 volt device) @ 200 m
This has the cold metal box problem.

Emphasis - TI 2N1560 (and whatever) - obsolete

TI 2N2150 (a lamp device)
M.H. 2N2634 (good amplifier or lamp)

The 6206 has a double break type not @ 2 amps which is undesirable.

We will make 6206’s to go on them, and sell them.
Spec the thing four R 6206

1e
7006 - in 9/16

SCR (small) IBM had an offer - Easy done.

Anybody - IBM guaranteed if everyone met before
let's all work - I'll see what's going on this one of the
first 800 units.

SCR - ( camp, 400v) - Like yours @ 400. This looks like

7500 - No action.

NPN - Large geometry

4011/16 - A good move in snow. Out in 4 weeks.

H201 - We will look at some files. Had 4011 that

product. Do need to do more. Will inform.

We are now concerned about the low current problems.

We will quit out - option of time, reconfiguration, across anything.

Schultz, Feygan, Steven (now), Baldwin. For operational testing.

4H11 - Being run. It came out of the woods.

150 or 4205 - For season things. - Being run.

E = 4207
DC Current Gain Versus Collector Current

4201 hrs - Solid Curve

Collector Current (Ic)

Vce = 10 volts

4201
4011
4200

0 10μA 100μA 1mA 10mA 100mA 1A
<table>
<thead>
<tr>
<th>Run</th>
<th>No. Unit</th>
<th>Vgo</th>
<th>$I_{t=0}$</th>
<th>$I_{t=1000}$</th>
<th>%ΔI</th>
<th>$I_{t=1000}$ junction 0 1000hr</th>
</tr>
</thead>
<tbody>
<tr>
<td>62-11-10A getter 1100°C 11min Stem</td>
<td>3</td>
<td>-4</td>
<td>7.2</td>
<td>-26</td>
<td>-33</td>
<td></td>
</tr>
<tr>
<td>+O₂ 140min deg N₂</td>
<td>3</td>
<td>-8</td>
<td>1.9</td>
<td>-25</td>
<td>-34</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Run</th>
<th>No. Unit</th>
<th>Vgo</th>
<th>$I_{t=0}$</th>
<th>$I_{t=1000}$</th>
<th>%ΔI</th>
<th>$I_{t=1000}$ junction 0 1000hr</th>
</tr>
</thead>
<tbody>
<tr>
<td>62-11-10AA Getter Same above plus 1100°C 15min CO</td>
<td>3</td>
<td>-4</td>
<td>7.5</td>
<td>-5</td>
<td>-6</td>
<td></td>
</tr>
<tr>
<td>62-11-10B Repeat 10A above</td>
<td>1</td>
<td>-4</td>
<td>1.808</td>
<td>-2.7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>62-11-10BB Repeat 10BB above</td>
<td>1</td>
<td>-4</td>
<td>6.49</td>
<td>-0.8</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| 62-12-3A 1100°C 15min(N₂) | 5 | -4 | 8 | -8 | -16 |

| 3B 15min (O₂) | 5 | -4 | 3μa | -6 | -8 | 3.5μa | 3.4μa |

| 3C 15min (CO) | 10 | -4 | 5ma | 0 | 0 |

| 150°C $V_{EB}=20v$ | 1 | -12 | 1.105 | -32.1 | -35.7 | 1.6μa | 1.6μa |

| Selected 3C (CO) clear appearance | 5 | -12 | 0.25 | -6 |
| poor mosaic | 5 | -12 | 0.25 | -12 |

| 3D 25min CO | 5 | -12 | 0.5 | -26 |
| 3E 60min CO | -5 | -4 | 2.5 | -15 |

1. % large (A) Small channel
2. No CO
3. Higher Vgo with NoCO
### SCFET

\[ V_{G1} = 0 \]

![SCFET Diagram](image)

<table>
<thead>
<tr>
<th>Run</th>
<th>No. Unit</th>
<th>( V_{SD} )</th>
<th>( V_{G2} )</th>
<th>( I_D )</th>
<th>100 %</th>
<th>220 %</th>
<th>1000 %</th>
<th>( T_{C} )</th>
<th>( I_{G1} )</th>
<th>( I_{G1} )</th>
<th>( I_{G1} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>62-11-7B</td>
<td>5</td>
<td>10</td>
<td>-4</td>
<td>0.25</td>
<td>-1.9</td>
<td>-6</td>
<td>-5</td>
<td>25°C</td>
<td>0.02 mA</td>
<td>1-300 mA</td>
<td></td>
</tr>
<tr>
<td>anodic</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>62-12-1A</td>
<td>5</td>
<td>10</td>
<td>-12</td>
<td>1.4</td>
<td>0</td>
<td>-4</td>
<td>0</td>
<td>25°C</td>
<td>0.02 mA</td>
<td>1-300 mA</td>
<td></td>
</tr>
<tr>
<td>CO-gettered</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>62-12-4A</td>
<td>5</td>
<td>10</td>
<td>-12</td>
<td>1.2</td>
<td>0.9</td>
<td>0</td>
<td>0</td>
<td>25°C</td>
<td>0.02 mA</td>
<td>1-300 mA</td>
<td></td>
</tr>
<tr>
<td>CO-gettered</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>62-12-1A</td>
<td>5</td>
<td>10</td>
<td>-12</td>
<td>1.5</td>
<td>-40</td>
<td>150</td>
<td>2.6 mA</td>
<td>1.6</td>
<td>150</td>
<td>0.1 µA</td>
<td>0.1 µA</td>
</tr>
<tr>
<td>4A</td>
<td>5</td>
<td>2</td>
<td>-20</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Feb 28, 1963 - SCFT and GPT design
Should be SCD (ie, MOST)

1. ...outdiffusion generally good channel.

2. SCFT circuit

3. SCD

The three have the same general drift will time

All the SCD's made to date are NPN with a long channel at t=0. This is thought to be a faulty process here.

On all these structures the CO gathered units didn't drift much -1.5 to 3. 11 units gave some return. There is 1 long drift over data.

For long CO treatment, the data is not very encouraging.

Leads:

...will try field electrode
a) int. amp gain
b) new everything
Art will claim that the correlation between drift and impurity is definite. He still sees in his hole only impurities.

First check with no 360 channels, have looked at show the points drop drift, etc.

\[ I(t) \]

\[ V(t) \]

Sudden loss (except the step) looks like ion drift on the surface. It is possible a constant problem. We should tie this defect to an output effect. It possible —
TO: List
FROM: Gordon E. Moore
SUBJECT: Agenda for Project Review Meeting

Thursday-2/28, 1:30 p.m.
Surface Controlled Field Effect Devices

The purpose of the meeting is to review progress which has been made in making stable surface controlled field effect devices and to plan program both with respect to individual devices and integrated circuits.

Agenda:

1:30 Review of recent data on reliability - (Tremere and Leistiko).
2:00 Review of recent data on reliability and old Rabinovitch data - (Lewis).
2:30 Group discussion of reliability data including what additional tests need to be made.
3:00 Plan for work to be done on SCFET.
3:45 Review of data on SCFET integrated digital circuitry - (Wanlass).
4:15 Discussion of potential of integrated SCFET circuitry.
4:45 Plan for additional work on SCFET integrated circuitry.

Please have all data summarized for efficient presentation.

GEM:hb
List: (Participants)
P. Ferguson
V. Grinich
O. Leistiko
A. Lewis
T. Sah
D. Tremere
F. Wanlass
W. Waring
W. H. W. was left out of this group and finds that they go with only one side set with A.C. Once with A.C. leads have much better (i.e. non-Cathode-ray) but still drift.

W. H. W.

The problem is the need for high currents because of high voltage.

Made of same stuff as left-hand scheme, these are made of 0.5 to 1.5 mm thick.

790 to 990 per cent in a year,
and 50% after cleaning.

A year pulse fibre from.

---

Get some electronic evaluation help for Frank!

If you make

[Diagram of circuit element]
We need ~ 75 night / week.

We will send all in express S'ain roof form.

In 3 weeks 1st O's come out.

They are shooting 2 cars/day this week:

1.5

For now send A.E. at least 1.0 units (fan size) of their preliminary evaluation. This should take until 3/6/63.

To Application:

Red units: 6' - 2 from total of 6 runs
Prod. 11

Red units: 5' - 100 from total of 6 runs
Prod. 11

Red units: 5' - 100 from total of 6 runs
Prod. 11

Red units: 6' - 2 from total of 6 runs
Prod. 11
<table>
<thead>
<tr>
<th>PROJECT</th>
<th>Breadboard</th>
<th>Masks In</th>
<th>Runs Started</th>
<th>Units Out</th>
<th>Unit Requirements</th>
<th>REMARKS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Autonetics dual NAND gate</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>3/22</td>
<td>80</td>
<td>R&amp;D test vehicle</td>
</tr>
<tr>
<td>2. Litton VAX NPN driver</td>
<td>3/29</td>
<td>4/5</td>
<td>4/19</td>
<td>5/17</td>
<td>80</td>
<td></td>
</tr>
<tr>
<td>3. Litton VAX preamplifier</td>
<td>4/5</td>
<td>4/12</td>
<td>4/26</td>
<td>5/24</td>
<td>80</td>
<td></td>
</tr>
<tr>
<td>4. MIT sense amplifier</td>
<td>4/12</td>
<td>4/19</td>
<td>5/3</td>
<td>5/31</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>5. Litton VAX NPN/PNP driver</td>
<td>4/26</td>
<td>5/3</td>
<td>5/17</td>
<td>6/14</td>
<td>80</td>
<td></td>
</tr>
<tr>
<td>7. Litton flip-flop - Chip B</td>
<td>5/17</td>
<td>5/24</td>
<td>6/7</td>
<td>7/5</td>
<td>80</td>
<td></td>
</tr>
<tr>
<td>8. Rem-Rand 3-input buffer</td>
<td>6/7</td>
<td>6/14</td>
<td>6/28</td>
<td>7/26</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>9. Autonetics general purpose amplifiers</td>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>0</td>
<td>Finish chips</td>
</tr>
<tr>
<td>10. Autonetics power switch</td>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

3/19/63
This is to announce the formation of a Custom Integrated Circuitry Group in the Device Development Section.

The purposes of establishing this group are as follows:

1. To train a nucleus of people for the design and production of custom integrated circuits.

2. To supply sample quantities of custom integrated circuits on an interim basis.

This group will report to Phil Ferguson. John Sentous, on assignment from Mountain View, will be Group Leader. He will have responsibility for:

1. Scheduling and producing custom circuits using R&D fabrication and Mountain View assembly insofar as possible.

2. Arranging for capability in Mountain View to take over this custom circuitry in late 1963.

The technology employed in making these custom circuits will be restricted to that which we are reasonably confident will be ready for transfer to production when the facility is installed. R&D will define the boundaries of this technology.

It is possible that other custom circuits will be made as test vehicles to allow R&D to experiment with the inclusion of new technology. In such cases, these circuits will be the responsibility of regular R&D personnel.

The pilot line capacity to be committed to the custom circuitry group is that necessary to start ~ 150 wafers per week. New masks at a rate of ~ one every two weeks can be accepted by R&D mask making for custom circuitry needs.

Since only circuits upon which one can expect production-worthy yields will be accepted, this should result in adequate samples, both for internal evaluation and for delivery of quantities up to ~ 100 to customers.
INTERNAL CORRESPONDENCE

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

TO: Jack Kabell
    Phil Ferguson
FROM: V. H. Grinich

DATE: March 4, 1963

SUBJECT: Project Review Schedule on Photo Transistors
          Tuesday, March 5 at 3:00 p.m.

Please prepare a written summary on the following material with the
schedule given below:

1) Chip fabrication with yield information and process permutations.
2) Packaging status and proposed variations.
3) Hard reliability data.

We would like to have 10 copies of all hard data available for
distribution at the meeting. The schedule calls for:

3:00-3:15 p.m.   Discussion on Fabrication by Warren Wheeler
3:15-3:45 p.m.   Packaging Discussion by Jack Kabell
3:45-4:30 p.m.   Reliability Data by Jack Kabell

VHG: ef
## Heat Treatment Experiments on the VP3

(500°C, 1 HR, N₂)

<table>
<thead>
<tr>
<th>Run No.</th>
<th>Remarks</th>
<th>No. Tested</th>
<th>Percent * Channeled</th>
<th>Percent with V&lt;sub&gt;CEO&lt;/sub&gt; &lt; 40V</th>
</tr>
</thead>
<tbody>
<tr>
<td>26</td>
<td>Ni</td>
<td>6 dice</td>
<td>0</td>
<td>17</td>
</tr>
<tr>
<td>30</td>
<td>Ni</td>
<td>7 &quot;</td>
<td>43</td>
<td>28</td>
</tr>
<tr>
<td>32</td>
<td>Ni</td>
<td>8 &quot;</td>
<td>0</td>
<td>12</td>
</tr>
<tr>
<td>38</td>
<td>Ni; 20% yield</td>
<td>6 &quot;</td>
<td>33</td>
<td>83</td>
</tr>
<tr>
<td>38A</td>
<td>No Ni; 11% yield</td>
<td>10 &quot;</td>
<td>20</td>
<td>30</td>
</tr>
<tr>
<td>39</td>
<td>Ni</td>
<td>10 &quot;</td>
<td>10</td>
<td>30</td>
</tr>
<tr>
<td>50</td>
<td>No Ni; 20% yield</td>
<td>10 &quot;</td>
<td>0</td>
<td>30</td>
</tr>
<tr>
<td>50A</td>
<td>No Ni; pyro. after em. diff</td>
<td>8 &quot;</td>
<td>0</td>
<td>38</td>
</tr>
<tr>
<td>49A**</td>
<td>Before Al; one chip.</td>
<td>38</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>49A**</td>
<td>Closed ring oxide removal around base; before Al; one chip</td>
<td>34</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>49A**</td>
<td>Closed ring; Al dot on emitter</td>
<td>27</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

*Actually, percent with channel currents > 100nA.

**These were baked at 530°C instead of 500°C.

Only those units had not been the 200° for 18 hours did not stabilize.
CHANNEL POSITIONS IN YP3 FAILED UNITS

METHOD OF DETERMINATION: BLUE LIGHT SPOT PROBING

I. UNMOUNTED DICE BAKED AT 500°C FOR 1 HR IN N₂, RUN #20

II. EPOXY-PACKAGED UNITS LIFE-TESTED AT 85°C FOR 9 DAYS (100% HUMIDITY, ~100 ft.-c.)

- 440 mA, CHANNEL
- 15 mA, CHANNEL

R.H/HP
3/5/63
YP-3  PROJECT REVIEW

Chip Fabrication

Fifteen runs of YP-Series completed through Die Sort. Yield data tabulated on separate sheet. Runs after #29 have not been completely sorted and are being used for experimental purposes.

Chip Problems

- Softs after metal. Changed alloy to 550°C - 4 min. Was 580°C.
- Shorts on packaging. Thin oxide - return to two hour oxide of XP-3.
- Al reaction with N+ and Ni region.

Experiments now in progress to determine causes of chip instability with temperature.

1. No metal over E.B. junction and oxide cut.
2. Metal vs No Metal.
3. Hot stage work and sectioning by W. Wandry.
# DIE SORT YIELD AND P.K.G.

<table>
<thead>
<tr>
<th>YP-#</th>
<th>% Die Sort</th>
<th>% P.K.G.</th>
<th>Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Lost at E.D.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>70%</td>
<td>56%</td>
<td>Soft epoxy</td>
</tr>
<tr>
<td>3</td>
<td>Lost at Experimental Silicone varnish</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Experimental complete ring - lost at E.D. and package experiments.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Lost at E.D.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>52%</td>
<td>76%</td>
<td>57%</td>
</tr>
<tr>
<td>7</td>
<td>38%</td>
<td>64%</td>
<td>80%</td>
</tr>
<tr>
<td>8</td>
<td>Lost at E.D.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>Data not available</td>
<td>61%</td>
<td>87%</td>
</tr>
<tr>
<td>10</td>
<td>58%</td>
<td>53%</td>
<td>73%</td>
</tr>
<tr>
<td>11</td>
<td>52%</td>
<td>70%</td>
<td>89%</td>
</tr>
<tr>
<td>12</td>
<td>Lost at E.D.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>Lost at E.D.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>62%</td>
<td></td>
<td>Did not bond</td>
</tr>
<tr>
<td>15</td>
<td>Did not bond properly</td>
<td>61%</td>
<td>(Changed to Bc†-3)</td>
</tr>
<tr>
<td>16</td>
<td>Base overdif.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>Channeled</td>
<td></td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>21%</td>
<td></td>
<td>Did not bond</td>
</tr>
<tr>
<td>19</td>
<td>33%</td>
<td>50%</td>
<td>0% High Id</td>
</tr>
<tr>
<td>20</td>
<td>Lost?</td>
<td></td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>29%</td>
<td>39%</td>
<td>77%</td>
</tr>
<tr>
<td>22</td>
<td>19%</td>
<td></td>
<td>No bondable</td>
</tr>
<tr>
<td>23</td>
<td>15%</td>
<td></td>
<td>Alloy trouble</td>
</tr>
<tr>
<td>24</td>
<td>9%</td>
<td></td>
<td>Alloy trouble</td>
</tr>
<tr>
<td>25</td>
<td>51%</td>
<td>28%</td>
<td>96%</td>
</tr>
<tr>
<td></td>
<td>47%</td>
<td>33.3%</td>
<td>Experimental 550 Alloy</td>
</tr>
</tbody>
</table>

P.K.G. = LTV + Glass
PACKAGING - HERMETIC

1. Silver leads. Mold pyroceram with Face Plate-lead bond okay - 560°C - Can't mold pyroceram.

2. Silver leads - Glass sandwich - Preform Block - Okay except (A) too expensive and (B) devices failed in devitrification cycle. 

3. Copper leads - Glass Sandwich - Poor bonding properties and bond strength.

4. Logic Package - 48 dice from several runs packaged in flat package with standard aluminum lead attach, glazing and devitrification. Result - 2 dice electrically good. Failures randomly distributed between opens, softs, channels, shorts.

5. 48 Bare dice through devitrification cycle. Result - 27 no change - 6 soft. 15 substantial decrease in $V_{ceo}$ $(>10\%)$ 

6. Now investigating cause of Heat Treat induced changes. (R. Dyck) - and possibility of short time high temperature bonding to Face Plate for composite Package.

PLASTIC PACKAGE

1. Channel Investigation indicates trouble starts at collector contact and spreads across base - (R. Dyck).

2. Teflon Jacket package being investigated.
LIFE TEST DATA

PLASTIC PACKAGES -

Run # 6 - 9 - 10 - 11  100% failed by CB leakage.
  # 7  6 out of 20 failed by C.B. leakage.
  Total  90 units failed by C.B. leakage.

To - 18 Package  23 units on test approximately 2000 hours.
                 Data attached. 2 went open. One showed large
                 increase in Id.

To - 5 and Epoxy  Data attached. 2000 hours. All increased
                 in Id.
<table>
<thead>
<tr>
<th></th>
<th>LIFE TEST 1</th>
<th>HEADER MOUNT</th>
<th>YP-3 1</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>3 Dec. I₁</strong></td>
<td>1.35 Ma</td>
<td>1.35 Ma</td>
<td>7.0 na</td>
</tr>
<tr>
<td></td>
<td>2.40</td>
<td>2.30</td>
<td>.56</td>
</tr>
<tr>
<td></td>
<td>1.65</td>
<td>1.75</td>
<td>2.2</td>
</tr>
<tr>
<td></td>
<td>1.20</td>
<td>1.20</td>
<td>2.0</td>
</tr>
<tr>
<td></td>
<td>1.20</td>
<td>open</td>
<td>8.1</td>
</tr>
<tr>
<td></td>
<td>.82</td>
<td>.80</td>
<td>.70</td>
</tr>
<tr>
<td><strong>1 March I₁</strong></td>
<td>1.10</td>
<td>open</td>
<td>.45</td>
</tr>
<tr>
<td></td>
<td>1.35</td>
<td>1.30</td>
<td>1.6</td>
</tr>
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<td>1.70</td>
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</tr>
<tr>
<td></td>
<td>1.60</td>
<td>1.55</td>
<td>2.8</td>
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<td>2.10</td>
<td>1.80</td>
<td>1.6</td>
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<td>1.45</td>
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<td></td>
<td>1.40</td>
<td>1.40</td>
<td>24.5</td>
</tr>
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<td></td>
<td>.54</td>
<td>.45</td>
<td>16.5</td>
</tr>
<tr>
<td></td>
<td>1.82</td>
<td>1.75</td>
<td>1.3</td>
</tr>
<tr>
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<td>.37</td>
<td>.35</td>
<td>2.0</td>
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<tr>
<td></td>
<td>1.25</td>
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<td>1.45</td>
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<td>1.20</td>
<td>1.38</td>
<td>18.0</td>
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<tr>
<td></td>
<td>1.35</td>
<td>1.48</td>
<td>1.9</td>
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<tr>
<td></td>
<td>2.10</td>
<td>2.15</td>
<td>2.3</td>
</tr>
<tr>
<td></td>
<td>2.65</td>
<td>3.60</td>
<td>.52</td>
</tr>
<tr>
<td><strong>1 March Iₐ</strong></td>
<td></td>
<td>open</td>
<td>.8</td>
</tr>
<tr>
<td></td>
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<td></td>
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</tr>
</tbody>
</table>
**EPOXY ON HEADER  XP-3**

<table>
<thead>
<tr>
<th></th>
<th>$I_1$ 12/5</th>
<th>$I_1$ 3/1</th>
<th>$I_d$ 12/5</th>
<th>$I_d$ 3/1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>.30 ma</td>
<td>.30 ma</td>
<td>100 na</td>
<td>110 na</td>
</tr>
<tr>
<td></td>
<td>.28</td>
<td>.30</td>
<td>32</td>
<td>43</td>
</tr>
<tr>
<td></td>
<td>.72</td>
<td>.65</td>
<td>85</td>
<td>140</td>
</tr>
<tr>
<td></td>
<td>.23</td>
<td>.22</td>
<td>16</td>
<td>22</td>
</tr>
<tr>
<td></td>
<td>.35</td>
<td>.35</td>
<td>460</td>
<td>610</td>
</tr>
</tbody>
</table>

Room Temp. Set. Epoxy
Attached is the schedule of presently planned custom integrated circuit work to be performed at R&D. You will notice that the Radiation and the IBM CHL and DTL circuits are not included since the Radiation circuits are being done as information becomes available and the IBM circuits are actually proprietary products.

In general, custom circuits will be handled in the same manner as is proposed for the normal factory operation, i.e., with John Hulme doing the breadboarding and circuit checkout. This will include all circuits for which the necessary components have adequate epitaxial kit counterparts. At present, this will include transistors, diodes, resistors and junction capacitors and, within a month, should be expanded to include MOS capacitors and NPN/PNP combinations. While the custom work is being done at R&D we will consider every technique which has been shown to be feasible as fair game for use.

When a circuit is selected as a test vehicle, as in the case of the high voltage Litton VAX driver, it will remain the responsibility of Ruegg or Farina. All other circuits will be the responsibility of Sentous.

Since we are only able to commit 150 wafers/week into the process it will be desirable to cut off immediately any circuit which encounters problems of such a magnitude as to necessitate brute force as a means of completing the order. Also, repeat requirements will tend to reduce the number of new circuits which may be attempted.

There will be a status review every Friday morning at 8:30 at R&D between Hulme, Sentous, and appropriate R&D people.

JPF: jh
End.
March 5, 1963  XP-3 Project Review Meeting

Wheeler: On the die.

We have made a lot of processing changes in an attempt to turn high β.

Duffy: Photo-pulling of channel shows the unwanted patterns in accompanying chart. Note that the channel does not cross the line 51.

Note on the epoxy - packaged units that all channels start from the same contact yields.

Units were dropped in channel current (X10^{-2} or X10^{-3}) by vacuum baking. From this no gain or change in channel extent by photo-plate.

Units or no channel are all in plate regions.

Kafell

Some units have teflon on 111 die under epoxy in old type package.

---

Proposed directions:

A. Package

1. Epoxy on teflon & glass face plate - lack of data

2. A glass plate metalized with built up Ag ball.
   - lack of data built upon glass
   - current technique
   - reliability
   - life test

3. Thin Mn-Ag coated film & Sn nodule.

Other minor cold upset square tube.
B. The die

We have a die in the 70-18 package;
we have no die for packaging at >400°C.
Units will use epoxy loblub; one method is epoxy next bed.

end of present effort

Lehty - 20%
Ullman - 75%
Weller - 25%
Sighe - (Cont'd, as needed)
From "Eddies" - 5%
Hill - 30%

Our customer would be delighted if we don't deliver.
Epitaxial kit parts:

KT-A, a 2x2 emitter X-bar

KT-4, 4 isolated X-bars of different geometry

XL-7, a pair of isolated T-like common collector T-1/2

The std. epi technology
March 22, 1963 - Pressure Sensor Answer

Ref p 17

One PTC has been put together. It has been tested and looks "good" with respect to 170 mV/sent.

Problems?

Ref p 17

Major problems:

1. The gadget has a Zero offset. This must be balanced out.

   New ways are suggested
   a) Mounting of diaphragm on ring with jig to pre-stress to eliminate the flat layer.

2. A check technique such as applying a large offset on one leg to try to adjust after assembly to the ring.

3. We are unsure which way to turn to enter this market.

   a) We need an odd-ball power supply - rectifier a current source

Program:

1. Make 25 units as an schedule for life testing etc.
2. Make some 0-offset units.
3. Make data on the 25 and
4. Sample of 0-offset units by June 1.
This must be lithoed to all APN or possibly with a separate PDP input device.

Proprietary Drug.
PROJECT REVIEW

PROJECT 4140

I. DIAPHRAGM FABRICATION

A. Wafer Preparation
1. Yields
2. Loss
   Reason: Breakage, wedging, and size control.
3. Straight service yield _______ 45 %.
4. Supervising process ______ and actual work ______ 72 %.

B. Mechanical Polishing
1. Problems -

C. Wafer Area - Crystal Uniformity -
1. R&D - poor.
2. S. Rd. - small, but more uniform.

D. Processing
   Major Process Permutations -
1. Phos. Gettering - Yield to new spec. 25% (1457 device total) = 1.77 Dia./wafer
2. No Phos. Gettering - Yield to new spec. 2.5% (745 devices total)
3. Crystal orientation - <111>, <110> - no final data.
4. Mapping - Time required
   10 min. full wafer; 20 min., chips.
5. Mounting, Marking - 5 min/wafer.
6. Alignment and cutting - with a coin die cutter
   10 min/Dia. for 100 psi (1 mil./min).
   Yield - 50%
   Loss cause - breakage, cutting and cleaning.
   Learning curve - operator dependent.
   Forecast - 80% - (Bob Brand).
   Yield electrical - Problem -
   Soft after cutting - no. Al. Note: % (Run 26, 0%; Run 24, 100%)
   With Al. ______ 100 %.

8. Lead Bond - 4 in 1 out
II. PACKAGE FABRICATION

   50 complete - except plating.
   Estimated cost ......................... $ 1.41 (500)

2. Spacers - 50 due 3-19-63 ............ $ .99 "

3. Plugs - Electrical
   50 in house ........................... $ 6.00 "

4. Sintered Plugs
   100 in house ........................... $ .10 "

5. Silicon Rings - 35 in house
   20 oxidized - pyrolytic ............... $ 5.00 "

6. "O" Rings - Buna N.
   50 in house ........................... $ .30 "

7. Solder seal - Induction - Built and
tested 5 packages - 4 to burst.
   Burst pressure - 5000 psi
   All sustained for 1 min. at 5000 psi.

8. Assembly Techniques
   a. R.D. seal. H.T. epoxy - 400°F. cure (215°C) Checked on PTB
      and PTA + 1 PTC. PTB gave 100% bond yield.
   b. Lead welds - Problem solved by new spacer design. No yield data yet.
   c. Final seal - Induction soldered in secs with 15 mil preform.

III. P.T.B. DATA + P.T.C.

    N.P. Data Sheets.

IV. P.T.C. SCHEDULE
INTERPRETATION OF HAMMOCK-SLUNG DATA

PTB-1
Excluding the two extremes (150 and 74 mv), the total spread of zero outputs is 20 mv. This would indicate that by proper mask redesign, one could produce diaphragms with a zero balance of less than 10 mv with 75% yield. But consider -

PTB-28
Once again, eliminating the two extremes, we see a tight distribution (11 mv total spread). However, the average imbalance here differs from the average imbalance of run PTB-1 by 65 mv. An explanation exists: Devices on a single working plate match each other quite well, whereas a comparison of devices between working plates shows lack of reproducibility.

PTB-20
Exclude the worst case. Average imbalance is improved over PTB by at least 50 mv. Spread is worse (40 mv). Explanations exist for the worse spread, but will be deferred at present on the grounds of insufficient data.

Note on PTC Header Yield:
Wafers with 25 good devices on them were backside mechanically scribed. 9 devices met electrical specifications on subsequent die sort. 5 devices survived hammock slinging.
<table>
<thead>
<tr>
<th>Unit No.</th>
<th>Linearity</th>
</tr>
</thead>
<tbody>
<tr>
<td>PTB-6</td>
<td>-0.50%</td>
</tr>
<tr>
<td>PTB-11</td>
<td>-0.40%</td>
</tr>
<tr>
<td>PTB-12</td>
<td>-0.45%</td>
</tr>
<tr>
<td>PTB-13</td>
<td>-0.49%</td>
</tr>
<tr>
<td>PTB-3</td>
<td>-0.47%</td>
</tr>
<tr>
<td>PTC-1</td>
<td>-0.36</td>
</tr>
</tbody>
</table>
### Pressure vs. Temperature (With Emphasis on Hysteresis)

<table>
<thead>
<tr>
<th>Unit No.</th>
<th>Sensitivity Before Test (mV)</th>
<th>Sensitivity After 200°F (mV)</th>
<th>Sensitivity After -20°F (mV)</th>
<th>Zero Before Test (mV)</th>
<th>Zero After 200°F (mV)</th>
<th>Zero After -20°F (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PTA-17-13</td>
<td>271.78</td>
<td>286.35</td>
<td></td>
<td>0.03</td>
<td>-4.95</td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>Unit took 27mV shift at 98°C</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PTB-3</td>
<td>222.15 (c)</td>
<td>231.23</td>
<td></td>
<td>-1.12</td>
<td>-2.41</td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>Shift between 200°C, 3200 psi @ 24°C</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PTB-6</td>
<td>256.11</td>
<td>261.46</td>
<td></td>
<td>0.96</td>
<td>1.64</td>
<td></td>
</tr>
<tr>
<td>PTA-22-2</td>
<td>302.72</td>
<td>299.38</td>
<td></td>
<td>-1.11</td>
<td>-2.56</td>
<td></td>
</tr>
<tr>
<td>PTA-22-3</td>
<td>263.19</td>
<td>263.38</td>
<td></td>
<td>0.05</td>
<td>0.06</td>
<td></td>
</tr>
<tr>
<td>PTA-22-4</td>
<td>291.31</td>
<td></td>
<td></td>
<td>Short to case</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PTB-11</td>
<td>290.49</td>
<td>290.63</td>
<td>290.66</td>
<td>0.03</td>
<td>0.00</td>
<td>-1.75</td>
</tr>
<tr>
<td>PTB-12</td>
<td>245.20</td>
<td>245.82</td>
<td>245.80</td>
<td>0.18</td>
<td>-1.09</td>
<td>2.91</td>
</tr>
<tr>
<td>PTB-13</td>
<td>295.35</td>
<td>295.38</td>
<td>295.61</td>
<td>2.43</td>
<td>1.18</td>
<td>1.39</td>
</tr>
<tr>
<td>Unit No.</td>
<td>$V_{\text{out}} \pm 10$ Volts in (mv)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>------------</td>
<td>--------------------------------------</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PTB-1-A-1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>- 2</td>
<td>84</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>- 3</td>
<td>15.0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>- 4</td>
<td>90</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>- 5</td>
<td>95</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>- 6</td>
<td>97</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>- 7</td>
<td>104</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>- 8</td>
<td>74</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PTB-28-4-1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>- 2</td>
<td>163</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>- 3</td>
<td>152</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>- 4</td>
<td>130</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>- 5</td>
<td>163</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>- 6</td>
<td>229</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**AVERAGE = 93 mv**
(excluding the two extremes)

**AVERAGE = 158 mv**
(excluding the two extremes)
## PTC Hammock-Slung Headers

<table>
<thead>
<tr>
<th>Unit No.</th>
<th>$V_{out} @ 10$ Volts in (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PTC-20-2-1</td>
<td>58</td>
</tr>
<tr>
<td>-2-2</td>
<td>20</td>
</tr>
<tr>
<td>-5-1</td>
<td>32</td>
</tr>
<tr>
<td>-5-2</td>
<td>60</td>
</tr>
<tr>
<td>-8-1</td>
<td>280</td>
</tr>
</tbody>
</table>

Average = $42\frac{1}{2}$ mV  
(excluding single worst case)
## PTA Burst Tests

<table>
<thead>
<tr>
<th>Unit No.</th>
<th>Linearity (%)</th>
<th>Hysteresis (%)</th>
<th>Burst Pressure (psi)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>400 psi</td>
<td>600 psi</td>
<td>800 psi</td>
</tr>
<tr>
<td>PTA-15-3</td>
<td>-.52%</td>
<td>-.75%</td>
<td>-.92%</td>
</tr>
<tr>
<td>PTA-15-6</td>
<td>-.51%</td>
<td>-.74%</td>
<td>-.93%</td>
</tr>
<tr>
<td></td>
<td>-.50%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PTA-15-1</td>
<td>-.43%</td>
<td>-.65%</td>
<td>-.83%</td>
</tr>
</tbody>
</table>

*CRACKED @ 1050 PSI*
To: Meeting Attendees

From: N. Zinker

Subject: NOTES FOR PRESSURE TRANSDUCER PROJECT REVIEW MEETING MARCH 19, 1963

1. Due to new specification for devices (>30 volts breakdown hard; leakage < 20 nano amps at 30 volts) time was lost trying to find devices which meet the specification. This problem appears to be resolved by using phosphorous gettering. Up to six usable diaphragms per wafer have been obtained from the most recent wafers. This phase of the schedule is dependent on our ability to get devices with the desired electrical characteristics.

2. Diaphragm cutting and ball bonding schedules are dependent on scraping the deposited metal leads as a temporary fix. This fix may not be adequate for the following reasons:

   a. Empirical evidence shows that devices which have good electrical characteristics on the wafer do not meet diode specification after diaphragm cutting. In addition, creepers have been generated; and since there is insufficient knowledge about this phenomenon acceptance or rejection of these devices is uncertain.

   b. Empirical evidence also shows that dice which were scraped and had good electrical characteristics before ball bonding had degraded after ball bonding.

Suggested corrections:

   a. Cutting diaphragms to the originally required diameter (.210 in) instead of the new diameter (.203 in). This will eliminate the need for lead scraping since the old diameter did not cut through the metalized area, which is the initial cause of the problem. The diaphragm would then be mounted on the annular ring using a locating rig, eliminating the need for a counter-bored annular ring (which increased the cost of the fabrication of the annular ring).

   b. Redesigning the metalizing mask so that the leads are shorter. Hence the leads will not be cut during the diaphragm cutting process. A new set of masks must then be stepped.
3. Spacer and case fabrication schedule is dependent on the ability of outside sources to meet the required tolerances. A reason for not meeting the completion date on the original schedule was due to the inability of the lowest bidder (Jet Fittings) to satisfactorily machine the parts. The substitute machine shop (Swiss Precision) was able to fabricate and deliver satisfactory cases. They are now working on the spacers, and it is expected that they will meet the required tolerances. Therefore, they appear to be a suitable source for the fabrication of cases and spacers.

4. Final transducer assembly schedule is dependent on R. Brown's induction soldering unit being available when it is required. All final assembly fixtures have been designed to fit his unit.
PTC-10A-4-1

ZERO BALANCE vs. TEMPERATURE

36.0
35.5
35.0
34.5
34.0
33.5
33.0

70 100 150 200 250

TEMPERATURE (°F)

ZERO SHIFTS = 0.0063%/°F

0.1% of 250 mV

DATA SHEET NO5.
S, 6, 7, AND 8

3/20/63

KEUFFEL & ESSER CO.
MADE IN U.S.A.

3/21/63 Nolan E. Pearson
PTC-10A-4-1

LINEARITY vs. TEMPERATURE

LINEARITY
(% F.S.)

-25
-20
-15
-10
-5

TEMPERATURE (°F)

70 100 150 200 250

3/20/63

DATA SHEET

NOS. 5, 6, 7, 8

3/21/63  Nolan C. Parsons
PTC-10A-4-1

SENSITIVITY vs. TEMPERATURE

SENSITIVITY (mV)

2.25

2.20

2.15

70 100 150 200 250

TEMPERATURE (°F)

SENSITIVITY SHIFT = 0.034%/°F
(CONSTANT CURRENT)

3/22/63 DATA SHEET

NOS. 5, 6, 7, 8

3/21/63 Notation
The strength check for the NAND logic does not look reliable. Other possibilities are:

a) a different layout, the volume of R-type.
   I don't like this.

b) a p-type p-substrate substitute for long cut-off.

c) copper etch & backfill

Some more circuit work is needed to show that the possibility of making the device will do the job. Until then, no more work to be made.

Gates will be out in ~3 weeks, but the usefulness is dependent upon the possibility of making the R.

The series-gated R-element is in the mill (late) ~2 weeks.

Still considering a C-implanted S-element for a line-compatible device.

To be printed.

No came out ~2 slow than expected.

As made: 
-11.5
mod. 0.1 
-8.5

Bandgap: 
-5.5

Not filled.
Some report on old data on the quality of the
grain junction:

Hank will see that an evaluation report gets run periodically to
evaluate the competitive surface defect density on a continuing
cbasis.

(Didn't feel that he can buy much better surface (on pitz)
than he can grow).

(Get Cole on tech report list) - especially in these spindles.

New lesson:

Old machine is still running. It has a pit problem.

1) We should be concerned with pit removal and compensating.

2) What is nature of system. We don't know.

Cole needs an additional react. We will try trade off.

We can supply SiCl for awhile.
Fig. I

To scope
Vertical Input

Powerstat
0-130 v. AC.

117 v. AC.

To scope
Horizontal Input

9 meg Ω
½ w.

2500 Ω
1 w.

550 Ω
2 w.

10 kΩ
5 w.

Power Transformer
200-0-200 v.

3.5 mil
diameter, size necessary to calibrate.
Mask making:

Mask alignment check has been stopped - no problem since Sept 26 and that was an old machine.

Matrix stepping is good to < 0.1 mil.

The multiple>>>>>> geometric one is in.

We are using many more plates than needed.

Protractor printing is being tried. —— Needs layout of project.

The original many jobs are do-able (0.5 mil line). They keep changing — now are to a 20" x 10" array.

Optical alignment jig:

TP3 20B1
E21 21X/0.50
50 X Red.
Resolution 0.02 mil
Reduction made 3-19-63
Mainly 2 problems:

1. He mixed better solution.
2. Worked i.e. it.

History:
The first for ADAM (15 MO ago)
But ADAM in my FD-1 is less soluble at high temp. The problem is
In R, 1909 ADAM 10" by FD-1 & 12, from a variety of mechanisms.
Also R of ADAM alone is > FD-1.

Now trying to convert FD-1 and FD-7 to it.

On FD-1
C about 2% in <1 on regular plates. Stable @ 200°C.

Test 379

Problem:
1. High C at 130
2. IR stability N.5. or Triglycol
3. Mechanical failure
4. Recovery of mechanical failure + p. failure
for no apparent reason.

Now we will Sn-cell calib:

Now be going to different calib. (Ni: 4x20 mil) the
Mechanical failure look improved.

Diameter of bottom of dot is ~ 6.7 mil by keeping smaller than 6
At 200°C C is stable
At 300°C C is stable - then in eutectic C & Fe - 3.6% Fe
Action Items:

FD-1

1. JPF will try the new assembly technique for the imp. @ center.

2. Jeffek will try to plate other materials to say where we put No. 1 (Figures & amp) and one other. Before &

3. Joe Brown will bring down some of these units with unusual rate capability.

We will evaluate electrically & analytically for mechanism.

4. Postulate that drift amount simply is seen for IR drift. Check

For the fig. will we want a constant?

The kind: Pd - Ru
Pd - Au
Ni

Problem are
He should layout a "blue" eye
for forming, express a dignit facility tone.

After this, less companion.
### Table I

Resistance change during alloying (2 min $N_2, 580^\circ C$) for different substrate temperatures

<table>
<thead>
<tr>
<th>Run RNC#</th>
<th>Date Evaporated</th>
<th>Date Alloyed</th>
<th>Substrate Temp. (°C)</th>
<th>10-90 Percentile Spread % Before All.</th>
<th>After All.</th>
<th>R(after) - R(before) (%)</th>
<th>TRC ppm/oC</th>
</tr>
</thead>
<tbody>
<tr>
<td>42</td>
<td>1/25</td>
<td>2/7/63</td>
<td>400°</td>
<td>7.9</td>
<td>7.6</td>
<td>-3.1</td>
<td>60-140</td>
</tr>
<tr>
<td>43</td>
<td>1/29</td>
<td>2/7</td>
<td>600°</td>
<td>24.0</td>
<td>27.0</td>
<td>+38.5 +31.0 +59.8</td>
<td>20-180</td>
</tr>
<tr>
<td>45</td>
<td>1/30</td>
<td>2/7</td>
<td>500°</td>
<td>18.3</td>
<td>19.5</td>
<td>+42.0 +35.8 +49.2</td>
<td>30-290</td>
</tr>
<tr>
<td>46</td>
<td>1/31</td>
<td>2/8</td>
<td>410°</td>
<td>4.82</td>
<td>4.1</td>
<td>+0.57 -0.75 +2.0</td>
<td>80-120</td>
</tr>
<tr>
<td>47</td>
<td>2/1</td>
<td>2/8</td>
<td>310°</td>
<td>6.15</td>
<td>4.47</td>
<td>-4.1 -3.5 -5.2</td>
<td>100-150</td>
</tr>
<tr>
<td>48</td>
<td>2/5</td>
<td>2/15</td>
<td>300°</td>
<td>5.77</td>
<td>8.86</td>
<td>+2.7 +2.0 +5.2</td>
<td>40-100</td>
</tr>
<tr>
<td>50</td>
<td>2/7</td>
<td>2/15</td>
<td>350°</td>
<td>2.95</td>
<td>3.52</td>
<td>-0.7 -0.25 +0.5</td>
<td>90-130</td>
</tr>
<tr>
<td>51</td>
<td>2/11</td>
<td>2/15</td>
<td>350°</td>
<td>2.90</td>
<td>3.20</td>
<td>+6.1 +5.7 +6.5</td>
<td>50-90</td>
</tr>
<tr>
<td>52</td>
<td>2/12</td>
<td>2/15</td>
<td>300°</td>
<td>4.33</td>
<td>9.38</td>
<td>+6.1 +3.2 +11.2</td>
<td>60-200</td>
</tr>
<tr>
<td>53-A</td>
<td>2/13</td>
<td>2/15</td>
<td>400°</td>
<td>4.54</td>
<td>3.98</td>
<td>+7.6 +7.1 +8.0</td>
<td>50-90</td>
</tr>
<tr>
<td>53-B</td>
<td>2/13</td>
<td>2/15</td>
<td>400°</td>
<td>3.94</td>
<td>3.07</td>
<td>+2.4 +1.8 +3.4</td>
<td>10-100</td>
</tr>
<tr>
<td>54</td>
<td>2/13</td>
<td>2/18</td>
<td>340°</td>
<td>5.32</td>
<td>5.03</td>
<td>+21.7 +20.2 +22.8</td>
<td>90-190</td>
</tr>
<tr>
<td>56</td>
<td>2/14</td>
<td>2/18</td>
<td>340°</td>
<td>3.34</td>
<td>3.19</td>
<td>+4.7 +4.3 +5.1</td>
<td>90-150</td>
</tr>
<tr>
<td>57</td>
<td>2/14</td>
<td>2/19</td>
<td>360°</td>
<td>4.31</td>
<td>4.04</td>
<td>+4.2 +3.8 +4.6</td>
<td>80-160</td>
</tr>
<tr>
<td>58</td>
<td>2/15</td>
<td>2/19</td>
<td>320°</td>
<td>6.35</td>
<td>5.50</td>
<td>+6.8 +6.2 +7.6</td>
<td>40-80</td>
</tr>
<tr>
<td>59</td>
<td>2/15</td>
<td>2/19</td>
<td>380°</td>
<td>4.47</td>
<td>4.02</td>
<td>+6.9 +6.1 +7.5</td>
<td>50-310</td>
</tr>
<tr>
<td>60</td>
<td>2/18</td>
<td>2/20</td>
<td>340°</td>
<td>4.89</td>
<td>5.07</td>
<td>+12.5 +11.7 +13.3</td>
<td>80-120</td>
</tr>
<tr>
<td>61</td>
<td>2/18</td>
<td>2/26</td>
<td>380°</td>
<td>6.58</td>
<td>5.67</td>
<td>+11.2 +10.3 +12.4</td>
<td>40-140</td>
</tr>
<tr>
<td>62</td>
<td>2/18</td>
<td>2/26</td>
<td>340°</td>
<td>3.24</td>
<td>3.23</td>
<td>+17.5 +16.7 +18.3</td>
<td>30-110</td>
</tr>
</tbody>
</table>

4/4/63
### Nichrome

**Vacuum Evapn. Conditions vs. Change during Alloy Sublim. S**

<table>
<thead>
<tr>
<th>T(°C)</th>
<th>ΔR (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>25°</td>
<td>-1.3 +35</td>
</tr>
<tr>
<td>25°</td>
<td>+5.1 +10</td>
</tr>
<tr>
<td>100°</td>
<td>+18 +30</td>
</tr>
<tr>
<td>150°</td>
<td>+20 +27</td>
</tr>
<tr>
<td>200°</td>
<td>-2.7 -20</td>
</tr>
<tr>
<td>200°(305)</td>
<td>-7.8 -25</td>
</tr>
<tr>
<td>480°</td>
<td>-4.5 -16</td>
</tr>
<tr>
<td>600°</td>
<td>~10X</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>T(°C)</th>
<th>ΔR (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>380°</td>
<td>-4.0 -20</td>
</tr>
<tr>
<td>391-380 V</td>
<td>+19.8 +20.7</td>
</tr>
<tr>
<td>380-340</td>
<td>+6.7 -8.8</td>
</tr>
<tr>
<td>380-320</td>
<td>+8.9 +17</td>
</tr>
<tr>
<td>390-360</td>
<td>-7.1 +7.1</td>
</tr>
</tbody>
</table>

### Oxygen

<table>
<thead>
<tr>
<th>P0₂ (Torr)</th>
<th>T(°C)</th>
<th>ΔR (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2·10⁻⁵</td>
<td>50°</td>
<td>-24.7 +7.0</td>
</tr>
<tr>
<td>2·10⁻⁵</td>
<td>80°</td>
<td>0 +12.0</td>
</tr>
<tr>
<td>5·10⁻⁵</td>
<td>50°</td>
<td>-46.5 -59</td>
</tr>
<tr>
<td>1·10⁻⁴</td>
<td>60°</td>
<td>-70.5 -75</td>
</tr>
<tr>
<td>5·10⁻⁵</td>
<td>210</td>
<td>-74.5 -75</td>
</tr>
</tbody>
</table>

### Carbon Monoxide

<table>
<thead>
<tr>
<th>PCO (Torr)</th>
<th>T(°C)</th>
<th>ΔR (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2·10⁻⁵</td>
<td>70°</td>
<td>-28.4 -46.5</td>
</tr>
<tr>
<td>1·10⁻⁴</td>
<td>50°</td>
<td>-28.4 -34.6</td>
</tr>
<tr>
<td>2·10⁻⁵</td>
<td>130°</td>
<td>-35.5 -50.5</td>
</tr>
<tr>
<td>1·10⁻⁵</td>
<td>50°</td>
<td>+20.0 +21</td>
</tr>
<tr>
<td>S</td>
<td>300-260</td>
<td>-18.5 -23</td>
</tr>
<tr>
<td>2·10⁻⁵</td>
<td>200°</td>
<td>-46.5 -52</td>
</tr>
<tr>
<td>1·10⁻⁵</td>
<td>300-225</td>
<td>-33.5 -49</td>
</tr>
</tbody>
</table>

-tkw
4 April 63
Regrettably, the reproducibility data showed general pretty good results, but it correlated with nothing except date of operation.

In the revised system we did this run, 

\[
\begin{array}{c|c}
\Delta R_{\text{min}(2)} & \Delta R_{\text{max}(2)} \\
-4.0 & -2.0 \\
+19.8 & +20.7 \\
\end{array}
\]

As far as we know, there are done identical.

The experiment to correlate RC geometry was undetermined. One is good, one is bad, and one is difficult.

Aware that in useful life is likely to vary essentially from day to day.

In reviewing the power we do not know what the problem, while different, depending on vacuum purity, is indicated. At their time an end run is required.

"Note in the book,"

\[\text{Feb 20} 82/0 - \text{Bob Wallace thinks it is better.}\]

1. "Spent film of Ni6."
2. Try Ta spent film.

"Note / will try a double AI to check out the need for alloy.
All is for NiCu.\]
Meeting on chb modifers - staffoff 4/8/63 Mr. S.

Mr. Smith 5/27
Mr. Smith 6/10
Mr. Smith 7/18

1. Clarify room, amp, sump problems
2. S.S. Chart, chart, chart
3. Block, Chart, Chart, amp
4. High Beam Def. amp
5. A.M. Def. amp
6. Current Source
7. Voltage ref.
8. Voltage Comp
9. S.T. cell replacement
10. try amp
11. F.E.T. op. amp
12. V to I converter
13. Yield land d.c. amp, (found?, not)
14. Try frequency modifier
15. F.E.T. decade amp
16. 7.5 volt Simon
17. D.M.V.
18. Spot check power supply

Mr. Smith 6/17
Mr. Smith 7/1

On program: Make 10 ea w R&D, follow as necessary.

On the D.M.V., the problem
1. Is there a capacitor problem? — Kell — Russell

We will turn out a weekly status report every Friday.

Acting
1. Pie chart
2. Objetive given to bank
3. Test C. problem 6/14
4. Send plans to check out

Pie chart will be a line sketch.
To: Distribution
From: V. H. Grinich
Subject: Instrumentation Circuit Modules
Minutes of Meeting held April 8, 1963

The following is a list of the items discussed with a description of the package in which they will be available, and a date indicating a time by which sales personnel will receive samples for distribution to customers:

<table>
<thead>
<tr>
<th>No.</th>
<th>Product</th>
<th>Date Sales Samples Available</th>
</tr>
</thead>
<tbody>
<tr>
<td>1*</td>
<td>General Purpose Amplifier (replace FP65), Epoxy Pack.</td>
<td>5/27</td>
</tr>
<tr>
<td>2*</td>
<td>Solid State Chopper Operational Amplifier (redesign to eliminate FET), Card &amp; Can</td>
<td>6/10</td>
</tr>
<tr>
<td>3</td>
<td>Photo-chop. STAB Operational Amplifier</td>
<td>7/18</td>
</tr>
<tr>
<td>4*</td>
<td>High Gain Differential Amplifier (need greater output) Epoxy Pack.</td>
<td></td>
</tr>
<tr>
<td>5*</td>
<td>AC Differential Amplifier, Epoxy Pack</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Current Source</td>
<td>6/3</td>
</tr>
<tr>
<td>7*</td>
<td>Voltage Ref.</td>
<td>7/22</td>
</tr>
<tr>
<td>8*</td>
<td>Voltage Comp.</td>
<td>7/8</td>
</tr>
<tr>
<td>9*</td>
<td>Standard Cell Repl.</td>
<td></td>
</tr>
<tr>
<td>10*</td>
<td>Log Amplifier</td>
<td></td>
</tr>
<tr>
<td>11*</td>
<td>FET Operational Amplifier</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>V to I Conv.</td>
<td>6/17</td>
</tr>
<tr>
<td>13*</td>
<td>Wide Band DC Amplifier</td>
<td>7/7</td>
</tr>
<tr>
<td>14</td>
<td>Low Frequency Sweep Generator</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>Lab Decade Amplifier</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>Functional Generator</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>Digital Voltmeter</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>Power Supply ISO</td>
<td></td>
</tr>
</tbody>
</table>

The following action items were discussed. The name in parentheses after the item indicates the person responsible for providing information. The date after the person's name indicates the time at which a memo giving the results of the action item should be sent to the same distribution as these minutes are sent:

1) Instrumentation Marketing to provide input regarding desirable package arrangements, including colors, marking, etc. (C. Ness & R. Randolph) 4/15/63

2) R&D will present Instrumentation Marketing with a preliminary objective
spec on Items 4, 10, 11, 12 and 18. The specs on Items 4, 12 and 18 will be issued by April 15 and those on 10 and 11 will be issued on April 22. Item 9 will be issued August 15 (this awaits our precision potentiometer arrival and use). (J. Kabell) 4/15, 4/22 and 8/15.

3) Instrumentation Marketing will send copies of all objective specs and data sheets to R&D prior to final printing so that R&D will have an opportunity to modify if necessary. (G. Ness and R. Randolph)

4) E. Russell and J. Kabell are to resolve the capacitor temperature coefficient problem by finding a person who will look over all the existing data and do the necessary experiments to resolve the questions on the present ramp capacitor. (E. Russell and J. Kabell) Report due 4/22

5) E. Russell will assign Doug Johnson to work on the debugging of the two other DVM chassis under R&D supervision. This assignment to take place as soon as possible. (E. Russell)

6) R&D will issue objective specs on 14, 15 and 16. (J. Kabell) 4/29

7) Weekly status reports will be issued by Instrumentation and R&D concerning modules that are in pilot production. These status reports should be written and issued on Friday and should be one 8-1/2" x 11" sheet of paper. Items for reporting are assigned as follows, with the exception of Item 5. This item was left in "no man's land" since no schedule or objective spec has been proposed. At the next meeting it will be a point of business to resolve this question of Item 5.

(M. Norby, Instrumentation)-------------------Items 1, 2, 3, 6, 7, 8 and 13
(H. Borden, R&D)--------------------------Items 4, 9, 10, 11 and 12.

The next meeting will be held at 8:00 a.m., Monday, April 29, in my office.
All solid state (no mech. chopper, no tubes)
All silicon
No chopper drive required

<table>
<thead>
<tr>
<th>SOLID STATE OPERATIONAL AMPLIFIER</th>
</tr>
</thead>
</table>

**GAIN:**

<table>
<thead>
<tr>
<th>Open Loop</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>D.C.</td>
<td>$2 \times 10^6$ (Min.)</td>
</tr>
<tr>
<td>Gain-Bandwidth-Product</td>
<td>$2MC$ (Min.)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Closed Loop (Unity Gain)</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{in} = R_f = 10K$</td>
<td>-3dB at 1.5MC</td>
</tr>
</tbody>
</table>

**INPUT:**

<table>
<thead>
<tr>
<th>Temperature Drift</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>-20°C to +80°C, less than 10μV/°C</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Voltage Offset</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Less than 200μV</td>
<td>Can be adjusted to zero with external pot.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Current Offset</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Less than 200pA</td>
<td>Can be adjusted to zero with external pot.</td>
</tr>
</tbody>
</table>

**NOISE:**

| Less than 100μV RMS, (referred to summing junction, bandwidth 0 to 1KC. $R_f = R_{in} = 100K$) |

**OUTPUT:**

<table>
<thead>
<tr>
<th>Output Current</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>2mA at ±24V</td>
<td></td>
</tr>
<tr>
<td>7mA at ±10V</td>
<td></td>
</tr>
<tr>
<td>10mA at 0V</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Output Impedance</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Less than 30Ω</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>POWER REQUIREMENT</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>+30V 30mA 1% regulation</td>
<td></td>
</tr>
<tr>
<td>-30V 30mA 1% regulation</td>
<td></td>
</tr>
</tbody>
</table>
Free thinking:
Many conductive sheets

Making the 10K thick, conductive layer looks like the best way to go.

Another way: make a preform
and glaze
non-conductive

tube

Probably the easiest to try in this case the pyrex, conductive glass

Add pyrex
stick a little

Add conductive glass

Assemble in a ceramic lead
1713 - Dry mud

1965- $10 appear to be an around five
  Q1. What happens under other life test conditions - GF tube - mother?
  Q2. What range of GA treatment is needed?

We (R&I) feels that from what we now know it is important
to continue to keep high voltage products.
Suggest a "joint effort" will between us club out

7500 - Our optimal long problem of thickness, etc, are on.
get agreed of 10 x 10 / 20 lbs.
In order for the product we must clean up
the channel & material.
from like a min of 4-6 mo.

SCR-2- Unit looks good a final check is underway.
Need to life test for new borderline
Problem: Require and special processing
  2MO MIN to life test
  od 3-6 MO to perform well.
April 10, 1963

WADC REPORT

Description of Approach and Progress During the Reporting Period:

During the reporting period two runs of UIV geometry FET's were finished successfully! The first UIV devices obtained had the following typical d-c characteristics: $I_{SDO} \geq 0.5 - 1.5 \text{ mA}$, $V_P \geq 1.5 - 2.5 \text{ volts}$, $gm \geq 1,000 - 2,000 \mu\text{mhos}$, and $BV \geq 8.5 \text{ volts}$.

Currently the Y-parameters are being measured, and some initial results will be given in the third quarterly engineering report.

The d-c characteristics meet every expectation for the UIV geometry devices save break-down voltage and are in line with theoretical predictions. The 8.5 volt break-down of the first UIV's is due to a higher-than-desired top gate impurity concentration. This concentration has been reduced considerably, and recent UIV FET's have break-down voltages ranging from 25 to 50 volts, other characteristics remaining about the same.

Using the identical starting material and diffusion schedule, but substituting the UIII mask set, one can expect about a two fold increase in $gm$ and $I_{SDO}$; whereas $V_P$ and $BV$ will remain unchanged.

Three UIII geometry FET device runs have been started which are being diffused the same way as the successful UIV's.

Mr. Bill Edwards, contracting officer, made a visit to the R & D laboratory of Fairchild Semiconductor on March 15, 1963. The integrated cascode was discussed with him as a very promising solution to the contract objectives. The cascode approach to a high input impedance FET device is quite independent from the approach now being pursued. Several low noise UI geometry FET's were sent to Mr. Edwards for his possible evaluation of the cascode idea.
WADC Report

Anticipated Work for April 1963:

In the next reporting period VIII runs now being processed should be completed, and at the same time additional runs will be started. In the a-c evaluation area Y-parameter and voltage gain measurements will be made on UIV devices.

Cumulative Percent Completion Toward Contract Objectives

(65% - Don't forget accumulated hours).
Equivalent Circuit
WAYNE KERR BRIDGE
SIMPLIFIED CIRCUIT DIAGRAM
"Y" Parameter J165

Measured at

Vgs = 0 Volts
Vds = 6 Volts
\[ Y_{12} = \frac{1}{2\pi fC_{cl}} \]

For:
\[ C_{cl} = 5 \mu F \]

\( \Delta \) \( Y_{12} \) - Wayne Kerr Bridge

\( \Phi \) \( Y_{12} \) - G. R. Bridge

\( + \) \( Y_{12} \) - Wayne Kerr Bridge

\( \times \) \( Y_{12} \) - G. R. Bridge

\( 5 \times Y_{12} \)
\[ Y_{11} = \frac{9}{m_0} - 2 \pi f \cdot C \cdot d \]

For \( m_0 = 2.00 \mu \text{m} \cdot \text{Hz} \)

\[ C = 5 \times 10^{-6} \]

- \( \Delta Y_{11} \) - Wayss Kerr
- \( \square Y_{11} \) - From Ye16 (W.R.)
- \( \bigcirc Y_{11} \) - G.R.
- \( + Y_{11} \) - Wayss Kerr
- \( \times Y_{11} \) - From Ye16 (W.R.)
- \( \bigotimes Y_{11} \) - G.R.
No text content is present in the image.
For $V_{in} = 10 \text{V}$

$V_o = 100 \text{ mV}$

$G_V = \frac{V_o}{V_i}$
Routine XFE 62-10-6A

K Folding by 50 units

I0
(mA)

Percent Less Than Ordinate
Run XFE 62-10-6A
50 units
April 10, 1963

FET Status

An outdiffused run with structures as shown in figs. 1, 2 and 3 has recently failed. It was desired to have no metal touching oxide but, due to the dimensions of the FET, the bonds not only touched the oxide but, in most cases, also crossed the junction. More units are presently being bonded with 0.4 mil wire in an attempt to isolate the metal contacts. One other outdiffused run and one epitaxial run are in the latter stages of processing and will be out by 15 April 1963.

Two runs of outdiffused circular geometry have been tested. One had no failures at 1000 hours and the other had two failures at 170 hours, but the alignment was poor on this run. We will start immediately five more runs of this geometry to obtain more extensive data.

Opaque prints of our 1-12 mil circle masks will be available this afternoon. These will be used to check out the structures shown in figs. 1 thru 5 and will be of sufficient size to allow containment of bond areas by the metallization.

In addition, new sets of masks are being designed, really a modification of other circular designs, to incorporate separate gate contacts, cut oxide over N-channel, N+ wider than metallization. The option will also be provided for oxide removal over all gate area, a la Amelco. Of necessity, this device will be much larger than the U-I.

The P channel units are surviving on life test, but the initial run had 0 hour nanoamp leakages and equivalent noise resistances of 5-6 MΩ. The leakages have decreased by a factor of 5-10 by 81 hours.
Field Effect Meeting 4/10/63

B. citrus device from 1 AAC an typ. 5.
- Dis of the band 8 "fail" at various
tones, G failure is described as high 1000 goto at 1 max 30
22V, 20°C

All other tests are at 50V, 150°C.

It appear to me that in order for this to fly it is
necessary that be established that adequate adequate reliability and:

- About adequate reliability

\[ \leq 170/1000 \text{ hr under any condition within rating} \]

Program:

1. Hentity effort check out to see alg difference - test 10 gravity.
2. Move p-channel and collect data.
3. After data is done (Jul 6) then new mesh.
Discussion of RHN on signal loop proposed for
10 MC logic gate.

Requirements: Delivery of 25 ea of 5 chks in 6 mo.
additional units at end of year.

a) 2 dl gate - 5-mil NOR
b) gate expander
c) Flip-flop - a "r" element i all extra garbage
d) Delay element - a 1-bit & an external expander
e) Four gate - (gate & output, filter) for out of 30; 60 alg
on clock delay

These are for all signal loop field date equipment. They will
do also be the high speed one for 5050's present custom.

Questions to answer:
1. Can we take on this job? - yes - JPF
2. If we can, is it worth taking on? - yes - JPF
3. Shall we take it on? - yes - JPF.

JPF says this looks good on the basis that he can
use it to lay DTL, a present idea of highest speed, and
then review review on the DTL, which is adequate, if
necessary.

Potential in 50,000,000 units
We will die off all the control units.
4/17/63 - PNP & power product planning meeting

ECO6 - Immediate action

Date sheet posted by 4/30. Ship a group in week of
at least one

38F @ 500 ma at room temp for test.

Temperature:
- 95% of rated chr @ 80V
- 85% of rated chr @ 100V
- 80% of rated chr @ 125V

M.O. with lining, type at 100% & 60% - Results on Apr 30
- Aim at 15-20 cents then load with pipe
- 66% need to date on P/D levels
- 4 - 8-60 levels TC

The VCB(30) in lift with shog in case or plate to an emittance of structure.
- Gasket is tight with emittance of material included. Will have
  by next meeting.
- Will have 2000 in place in 3 weeks on emittance
  need 2000 for demonstration.

R&D will look at these.

There is a need for a lightning power device. We need to look at it.

This is a device to reduce power with lightning.

Overall wants to reduce 65%. As yet we have no method of doing
this yet. Start a looking at thin from the point of view of some metal.

R&D should look at some of the new methods for thinning pipe.

BN will take out thin on B/C.

Please lets thin all competitive samples the local.

7006 - M/U has started 2-1/2 min. more out. Exactly like 620C
  except for mask.

U6 & B7 think that the extra iron will be tried, so it is not really
  worth doing.

M/U think we should be better off than the limited competition.

It will be in 7-1/2 emittance at 30 units.

Schedule 6 rooms with new mask using called in emittance rates will
be out in 30 days.
8000 - JPF thinks we should only work on either SCR or the big SCR, but not both.

SCR-3 3amp, 400 v
We are ok on all but VAC. Frank is fixing up to make sure.
R&D will run in parallel until MxV is running.

SCR - IBM
Did they ship 800 R10 units? Not likely known.
Because we assume later, we might get on 800,000 units.
Marketing will

SCR-1 200 v, 1amp - maybe after SCR-3

7506 - Our get channel in life. The product must solve high security problem.

1713 - In production, can get 10,000 lead cubes per week at 95c.
Begins for 20'd.
- Announcement of May 2006

1702 - Chi is faster than the 0.2 delay above 100 ns, the capital region.
If we can 3-stripe.
As MxV opens an ad and an marketing make we consider.

0005 - 50,000 still do all in life. 0.351%, "51" for open.
We have made 6 runs of 3511's that looked ok.

For current data.
4/18/63 – Meeting at

A cht. (p. 105)

Sitting chts:

Dr. Davis: Where are we in the process? Yes, we asked the

service, we [sic] own colleague, [name], to take

negotiations.

Preamp. – Here’s what we have so far. The director, the

director. When we agree on a cht, then can be re-scheduled.

Our Medac Opund will be straightened out.
They want a prep. delay that is 7 stages or 35 stages totaling 25 ms. 

<table>
<thead>
<tr>
<th>&quot;Flip Flop&quot; (Note R)</th>
<th>6ms</th>
<th>12ms</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate</td>
<td>25</td>
<td>250</td>
</tr>
<tr>
<td>Power Gate</td>
<td>25</td>
<td>25</td>
</tr>
<tr>
<td>Gate Expander</td>
<td>25</td>
<td>75</td>
</tr>
<tr>
<td>Delay Element</td>
<td>25</td>
<td>25</td>
</tr>
</tbody>
</table>

What have we headed now?

1. The gate (except last gate) - 12 ms @ 10 mw

2. The flip flop (headboarded, except for storage inside) @ 10 mw

Then looked marginal at regular pow. Need higher pow to good able.
Meeting on MOST - 4/22/63

Single unit:

No facing problems except those of flat surface

rectangular region

On one of our devices we have evidently had problems etching all the
wires on the etch plate square before re-etching. This has been the
limitation on the number of wires it can hold.

In a hardening wire gate we should bring out 4 levels.

These seem to be no problem controlling the 1000F oxide, a value that
was chosen because it is a nice rounded number.

On line 6, it is in line 0 or 920.

Red ink spill on paper is "a hell of a lot better." Than black, - look.

12-millimeter slub has very thick, 0.020 in. This sounds fine;
track the resistivity per centimeter.

In prose: 4 flat levels

1) Variety of oxide thickness

As soon as

As soon as we get some of these experiments through, we will be
ready for reproducibility runs.

Reliability data

-09

3.024

-0 C 105°C get some initial drift after stables.
Other polarity, complementary devices, individual studies.

We still cannot make new condenser at OUs. To date, our best result has been around three.

(We - We could use a guy here to learn to make.)

OUs will try to get a guy here to build one.

Complementary situations in one area.

(Nothing new being done.)

Money away
Defects:

1. Imperfections
2. Macropore pit defects (vesicles) - most amazing new

3. \[ \text{Mark} \]

4. \[ \text{Mark} \]

5. \[ \text{Mark} \]

Merging to follow.

They have been consistent in tracking Macropore Pit Defects

Some observations needed:

1. Surface contaminant
2. Austenite condition
3. \[ \text{Mark} \] Points in surface that do not stick a powder like the rest
4.\[ \text{Mark} \] Crystalline defects
5. \[ \text{Mark} \]

- \[ \text{Contamination artifact} \]
- \[ \text{Ripple etching} \]
- \[ \text{Surface condition} \]
- \[ \text{Variation in the retractor} \]
- \[ \text{Flow of the solution} \]
- \[ \text{Tilt gradient} \]

Crater:

Crater in a tightly collimated flux. Blade got out and removed with tweezers.

Such a particle is also shown as a red spot in the grid.

Thus are brown, obviously air- or contamination. Keep up to 5 ppm in argon.

Mess: Irregularly in substrate making round dents.

Pavement:
1. Bed Hz
2. \[ \text{Mark} \]
The purpose of the meeting is to review the experiments and results that have been obtained recently on the origins and elimination of imperfections in silicon epitaxial films, the effect of substrate surface preparation on the film perfection and the characteristics, properties, and origin of stacking faults in these films.

AGENDA:

10:00  A general and brief outline of the results obtained.  (Tucker)

10:30  Stacking faults.  (Tucker)

11:00  Effect of substrate surface preparation.  (Barry)

11:30  Experiments and results of elimination of defects.  (Davis, Barry & Yim)

Please have all data summarized and important data and photographs reproduced each for 10 copies for efficient presentation.

C.T. Sah

Solid State Physics Section

CTS:jt

List: (Participants)

R. Tucker  H. Wigton  D. Barry  E. Yim
A. Davis  C. Bittmann  P. Flint  J. Gordon
J. Lawrence  A. Grove  A. Roder  W. Shepherd
SUBJECT: PREPARATION OF PERFECT SUBSTRATE

The preparation of a perfect substrate in this project is interpreted as the preparation of flat silicon wafers free of scratches and pits.

Several methods are available to prepare substrate material; chemical etching, mechanical polishing, mechanical-chemical polishing, and anodic polishing. The only method to obtain flat surfaces, however, is the mechanical polish procedure. Therefore, this report will be limited to experiments in mechanically polishing silicon.

The procedure for mechanically polishing silicon consists of 1 1/2 hour polish or Buehler silk with cerium oxide on the Lapmaster followed by a 1/2 hour polish on Buehler microcloth with zirconium oxide on the AO bowl polisher. Before polishing, the wafers are mounted on a steel block, lapped flat at least 90 μ of material removed to get below saw damage.

Several experiments were performed to improve the mechanically polished surface.

1. Use of 1/4 micron diamond on Buehler microcloth with kerosene lubricant on AO polisher.
2. Cerium oxide on silk on the Lapmaster for 1 1/2 hour.
3. Cerium oxide on silk for 1 1/2 hour followed by 1/4 hour on microcloth with lustrox (a zirconium oxide precipitated solution).
4. Cerium oxide on pellon cloth on Highland Park for two hours.
5. Cerium oxide on pellon cloth on Highland Park for 1 1/2 hour followed by 1/2 hour on microcloth with cerium oxide on Highland Park.
6. Shamvra (MgO) on microcloth on AO polisher followed by 1 1/2 hour on silk with cerium oxide on Lapmaster.
7. Zirox (zirconium oxide) on microcloth on AO polisher 1/2 hour followed by 1 1/2 hour on silk with cerium oxide on Lapmaster.

The results obtained in all cases is strongly dependent on the lapped surface obtained before mechanical polish is initiated, chipped edges and non-flat lapped surfaces lead to scratches or uneven polishing. The procedure using zirconium oxide on microcloth on the bowl polisher tends to round out the edges of the lapped wafer. Then, a final polish on silk on the Lapmaster with cerium oxide produces a polished surface practically free of scratches and other surface blemishes. This procedure seems to give the best results to date.
I. To eliminate defects which are associated with dusts and other foreign particles on substrate surface, drying and loading are carried out in the positive pressure hood with clean air.

II. To eliminate pyramids, the following HCl vapor etching steps are used:

Step 1: 20 minute zero point HCl vapor etch @ 1175-1180°C optical;
Step 2: 5 minute slow growth with HCl vapor;
Step 3: fast growth to obtain desired film thickness.

In the following table, partial pressures and meter settings for the growth cycle are presented:

<table>
<thead>
<tr>
<th>Step</th>
<th>$P_{H_2}$</th>
<th>$P_{HCl}$</th>
<th>$P_{SiHCl_3}$</th>
<th>2 SCFM $H_2$ meter reading</th>
<th>0.15 SCFM $H_2$ meter reading</th>
<th>ml $SiHCl_3$ per min.</th>
<th>μ Si deposited</th>
</tr>
</thead>
<tbody>
<tr>
<td>Step 1</td>
<td>0.924</td>
<td>0.0116</td>
<td>0.00195</td>
<td>100</td>
<td>55</td>
<td>0.5</td>
<td>0</td>
</tr>
<tr>
<td>Step 2</td>
<td>0.991</td>
<td>0.008</td>
<td>0.00196</td>
<td>100</td>
<td>45</td>
<td>0.5</td>
<td>+ 0.16</td>
</tr>
<tr>
<td>Step 3</td>
<td>0.995</td>
<td>0</td>
<td>0.0047</td>
<td>100</td>
<td>0</td>
<td>1.2</td>
<td>1.0</td>
</tr>
</tbody>
</table>

Photographs, substrates, epitaxial films and electrical results are presented.
2 c) Substrate oxidized (steam, 1200°C, 2 hrs) and stripped prior to epitaxy.

2 d) Substrate oxidized (pyrolytic) and stripped prior to epitaxy.
Stacking fault study.

Case 1: 5/7

1st row nearest edge:
28
- 26 soft (2SF)
- 1DB (1F)
- 1soft (15F)
- 24 good

2nd row:
- 20ft (1D, 1 good)
28
- 1DB
- 1short
- 24 good

3rd row:
28
- 20DB (2SF)
- 26 good (25F, 1SF)

Stacking faults (6) → 2: soft
1: short
2*: Double bridged
1: good

Defective junctions (10) → 5: stacking fault
1: other defect
4: no apparent defect
Run 4 - 394
Chem polish wafers.
Stacking faults (10) → 6: double breakdown
2: soft
2: good
Defective junctions (34) → 8: stacking faults
6: other defects
20: no apparent damage
Mech. polished wafers.
Stacking faults (22) → 16: double breakdown
2: soft
4: good
Defective junctions (41) →
18: stacking faults
4: other defects
19: no apparent defects
Totals.
Stacking faults (38) → 24: double breakdown
6: soft
1: short
7: good
Defective junctions (85) → 38: stacking faults
11: other defects
36: no apparent defects
5a) Control - steam oxidized and stripped prior to epitaxy.

5b) Strained wafer, steam oxidized, prior to epitaxy.

5c) Control - argon atm. 15 min @ 1200°

5d) Strained wafer, argon atm. 15 min @ 1200°
2 a. Control wafer (mechanically polished substrate).

2 b. Substrate heated for 20 minutes in argon at 920°C
1 a). Control wafers: mechanically polished substrate,
zero etch 20 min, slow dep. 5 min, fast dep. 18 min \( \rightarrow \sim 25 \mu \). 

1 b). Substrates etched in dilute CPG (HAC diluent) to remove \( \sim 5 \mu \) prior to epitaxy.
3 a) Control: mechanically polished substrate.

3 b) Substrate etched to remove ~1 µm prior to epitaxy.
3. Substrate etched to remove ~ 20 µm prior to epitaxy.

4. Stacking faults grown over a smeared region on substrate.
April 21, 1941

Stacking Faults:

1. H. K. F. (This is probably all the N.A. cases are)
2. 3 N.A. cases
3. 1 L. K. F. (Large number)
4. 1 S. K. F. (Small number)
5. 1 S. K. F. (Small number)
6. No strain adjacent to edge of defect

Sometimes the O. M. O. remove defects like rust-like (but not always)

Peter D. thinks these are inclusions in the substrate.

For a reply in the note, like so:

We have a reactor that has two positions that make 30%:

a particular pattern!!

Stacking Faults:

Metallic polishing, usually not used, unless late.

A light abrasive etch helps (see 6a)

2 or more of 1 rate range, still define it.

Possible Cause:

1. Mechanical strain at surface of substrate - not deliberate.
2. Sometime

Stacking faults do not necessarily occur randomly, but can at high density among phase boundaries. They can be observed in any material.

The question is this: 5 out of 8.4 reactors tested these years, 10 had size 3 and 6 stacking faults, 5 of the 10 had one constant size of the 6 stacking faults.
Epistle. District report, cont.

Per Barry: [Substitute preparation.]

Even the best marketed product requires fine testing. Wigan thinks this time is lost for testing when more goes.

(See written report)
The NPN Planar Section Product Planning Meeting will take place on April 24 at 4:00 pm in the Large Conference Room. The following items will be discussed for all devices listed:

1. Status of production - Product Manager
2. Discussion of Characteristics - Applications
3. Production Schedule, Present and Future Sales - Marketing

- **PRODUCT**

  - **0000/0001**
  - Packaging of 0001 - P. Ferguson

  - **0002**
  - Reliability - Applications

  - **1312**
  - New 2N Number - Applications/Marketing

  - **0014**
  - New 2N Number - Applications/Marketing

  - **3011**
  - Competitive Devices - Applications/Marketing

  - **1221**
  - Objective Specifications - Applications/Marketing

  - **FET**
  - Status - P. Ferguson

  - **4011**
  - Status - P. Lamond

  - **4111**
  - Objective Specifications - Applications/Marketing

  - **4206**
  - Objective Specifications - Applications/Marketing

  - **4207**
  - Objective Specifications - Applications/Marketing

  - **New Devices**

  - **EO17** - P. Ferguson

**Distribution List:**

- T. Bay
- W. Richmond
- P. Ferguson
- R. Shultz
- R. Graham
- C. Sporck
- V. Grinich
- D. Valentine
- B. Knudson
- D. Yost
- G. Moore

Pierre R. Lamond, Head
NPN Planar Section
INTERNAL CORRESPONDENCE
FAIRCHILD SEMICONDUCTOR CORPORATION

TO: See Distribution

FROM: C. E. Sporck

SUBJECT: Results of NPN Large Geometry
Product Planning Meeting
February 26, 1963

No significant changes will be made in these instructions without the knowledge
and agreement of the writers.

4011 - 16 - Three split runs to be made by factory to compare these

4201

Ferguson to look at present 4011 devices to explain
poor low current beta performance.

Moore, Ferguson, Shultz, Graham and Grinich to decide
upon definition of optimum family of devices by 3/29/63.

4111 - Units out by 3/8/63, there evaluation will determine any
application.

4207 - 150 V $V_{CEO}(4205)$ 1 run/wk. Units to Applications by
mid April. Volume requirements in last five months. Use TC package.

T. Bay

G. Moore

C. Sporck

RECEIVED
MAR 6 - 1963
V. H. GRINICH
No significant changes shall be made in these instructions without the knowledge and agreement of the writers.

1312 - Now a production product. Will not have 2N's written around this product at this time. When product is well established and in good inventory position, optimum 2N's will be written.

1311 1211 - Production products. Have hot I_CBO problem. R & D will look at this problem in addition to the product group.

The 1210 will be rescheduled for special requirements.

3111 - Now running in production. This product will be announced at the IRE.

0002 - 35 mil die, gold bonds and TC package. Running 20 wafers out/week. Product should have sufficient life test data for announcement around end of March.

0000 0001 - Working directly on 0000. Will have dice at die sort by 3/4/63. Will send die sorted dice to Hong Kong by 3/8/63.

Some units will be assembled at Mountain View in TM packages.

Volume will be 20 wafers out/week by 3/11/63.

Product will be waiting for characterization by Applications.

The 0001 will wait until 0000 is established.

FET - Under development at R & D.

1221 - Marketing and Applications to decide by 3/11/63 what should be done with this product.

1450 - Dropped - stop all work.

CDC Core Driver - R & D to make recommendation on possible device to fill this requirement.
Small Geometry
Product Planning Meeting

Distribution
R. Cole
P. Ferguson
R. Fouquet
R. Graham
V. Grinich
B. Knudson
P. Lamond
J. Magarian
B. O'Keefe
M. Oudewaal
W. Richmond
J. Sentous
R. Shultz
R. Smullen
D. Valentine
D. Yost

T 13
T. Bay

G 14
G. Moore

C. Sporck

COMPANY PRIVATE
## R&D DEVICE DESIGNATION

<table>
<thead>
<tr>
<th>DEVICE NO.</th>
<th>FUNCTION</th>
<th>NPN/ PNP</th>
<th>A&lt;sub&gt;c&lt;/sub&gt;</th>
<th>A&lt;sub&gt;e&lt;/sub&gt;</th>
<th>NO. BASES</th>
<th>NO. EMIT.</th>
<th>GEOM.</th>
<th>MIN. OXIDE CUT</th>
<th>LV&lt;sub&gt;ceo&lt;/sub&gt;</th>
<th>REMARKS</th>
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<tbody>
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<td>0000</td>
<td>RF AGC</td>
<td>NPN</td>
<td>10.8</td>
<td>1.50</td>
<td>3</td>
<td>2</td>
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<td>.35</td>
<td>50</td>
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<td>RF</td>
<td>NPN</td>
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<td>1.50</td>
<td>3</td>
<td>2</td>
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<td>.35</td>
<td>25</td>
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<td>Power RF</td>
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<td>12</td>
<td>12</td>
<td>8</td>
<td></td>
<td>.50</td>
<td>25</td>
<td>1.0 W at 500 mc aggregate</td>
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<td>.245</td>
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<td>5.0 W at 500 mc aggregate</td>
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<td>.35</td>
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<td>25</td>
<td>4.5</td>
<td>4</td>
<td>2</td>
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<td>.25</td>
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<td>FT-1221 re-design</td>
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<td>21.3</td>
<td>4.5</td>
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<td>10</td>
<td>8</td>
<td></td>
<td>.35</td>
<td>12</td>
<td>Film driver</td>
</tr>
</tbody>
</table>
0000 to 70,000 - aiming at 100% yield.
For present - because of welcome supply - new only the entertainment
version.
Due to real test ed problems.
0001 - Still needs 

We have evaluated in hand-made pieces. The supply from outside
is not yet established. Est 1 mo. Make 7,000 more, 12/18 instead.

0002 - Make with 

75% to 750 mm 0.500 mc.
Make to make sure we need to do.

75% to 750 mm 0.500 mc.
of close to good dc.

We will make some 0002 a in step line plug.

1312 - 13 000 24th for now.

0014 - CDC like it ok.

3011 - 3 mm are at test 34
3 mm might be used - Aim at 50 Vdc.

Very much for later replacement.

1221 - Run the angle base again now.

For 4-channel device are still wide.

The P-1 are for now and, both dr 1 mm, V-1 structure.

4011 - Being run for 4W122 (old 3011) experimental. Not thinks the mask might
be good. Also there are more problems in loading.

4111 - By the next meeting we will define the device

Summary of George Ports.

Finite will run split 4201-3011.
Double growth tech. & 60 -
1. There is a great deal of uncertainty in the measurements.
2. The high temp. is fluid-like the polyedrally.
3. Reaction of arsenic departs from being many fringes.

The capacitance measurements are not working well at all. Can the surface tension disturb the agreement at all contrast.

- It is necessary to get together with CBS to see if the test in going.

Is there any selective diffusion transport into the film? (As the polyedrally.

There is no apparent transport of Br 0 0 0 into growing film.

Wighton:

Rate of deposition = k(y - \frac{y}{0.72})

The deposition is controlled by

\[ H_2 + SiCl_2 \rightarrow 2HCl + Si \]

One thing is a totally different.

\[ SiHCl_3 + H_2 \rightarrow SiHCl_4 + \]

The rate limiting step is

\[ SiHCl_3 \rightarrow SiCl_2 + HCl \]
HCl ETCHING STUDIES

H. Wigton

PROJECT 128 - SILICON EPITAXIAL FILM

For deposition with no HCl added, the best equation is

\[ r_D = \left(1 - 0.347 \ln \frac{y_0}{0.0027} \right) y_0 \]  \hspace{1cm} (1)

in which

- \( r_D \) = deposition rate in microns/minute
- \( y_0 \) = partial pressure of SiHCl\(_3\) in the entering H\(_2\) in atmospheres

Etching with HCl and H\(_2\) only is best expressed by the relationship

\[ r_E = 0.438 \times 10^3 \left( \frac{x_A^2}{0.36 + 2x_A} \right) \]  \hspace{1cm} (2)

in which

- \( r_E \) = etching rate in microns/minute
- \( x_A \) = partial pressure of HCl in the entering H\(_2\) gas in atmospheres

The reaction when both HCl and SiHCl\(_3\) are added appears to be kinetically limited by the conversion of SiHCl\(_3\) to SiCl\(_2\) and equilibrium

\[ \text{SiCl}_2 + H_2 \rightleftharpoons \text{Si} + 2\text{HCl} \]  \hspace{1cm} (3)

limited by the reaction

\[ \text{SiCl}_2 + H_2 \rightleftharpoons \text{Si} + 2\text{HCl} \]  \hspace{1cm} (4)

The forward reaction is stopped by the addition of HCl sufficient to balance the activities in equation (4) if approximately 15% of the initial SiHCl\(_3\) is assumed converted to SiCl\(_2\). This is several orders of magnitude less HCl than would be required to stop the overall reaction.
When both \( SiHCl_3 \) and \( HCl \) or both \( SiCL_4 \) and \( HCl \) are added, the rate is controlled by the relationship
\[
v = k (y - \frac{x^2}{K})
\]
where:
- \( v \) is the deposition or etch rate in microns/min,
- \( k = 1.15 \times 10^{3} \) is the diffusion or reaction constant,
- \( y \) is the partial pressure of \( SiHCl_3 \) in the gas film in atmospheres,
- \( x \) represents \( \rho^* \), the equilibrium activity coefficient of \( SiHCl_3 \) on the surface,
- \( \frac{x^2}{K} \) is the concentration of \( SiHCl_3 \) on the surface,
- \( x \) is the partial pressure of \( HCl \) (atmospheres),
- \( y_0 \) is the partial pressure of \( SiCL_4 \) or \( SiHCl_3 \) entering in atmospheres,
- \( y = c_1 y_o \), \( y = c_1 y_o (1 - c_3) \), \( y = (c_1)(c_2) (1 - c_4) \) for \( SiHCl_3 \),
- \( c_1 \) is the reaction constant, mols \( SiHCl_3 \)/mol \( SiHCl_3 \),
- \( c_1 = 0.28 - 0.30 \),
- \( c_4 \) is the number of \( SiHCl_3 \)/mol \( Si \) deposited/mol \( Si \) entering,
- \( y = (c_1)(c_2) (1 - c_4) \) for \( SiCL_4 \),
- \( c_2 \) is the reaction constant, mols \( SiHCl_3 \)/mol \( SiCL_4 \),
- \( c_2 = 0.9 \),
- \( c_3 + c_4 = 1.4 \),
- \( \frac{x^2}{K} \) is the concentration of \( SiHCl_3 \) on the surface,
- \( k = 1.15 \times 10^{3} \) is the diffusion or reaction constant.

To avoid trial and error, the following rearrangement can be used for \( SiCL_4 \)
\[
v = 1.15 \times 10^{3} \left[ \frac{0.195 y_o - x (x + 2.4 y_o)}{1.45 + 1.15 \times 10^{3} (10.7 y_o + 2.1 r 10^{4} y_o + 9 (k) 10^{-3})} \right]
\]
Sample Calculation

Silicon deposition run zero HCl added

Basis 1 minute; 2.5 mols H2 added 0.87 ml/min Silicon

\[
\begin{align*}
V &= 0.63 \text{ mols } Si \text{ deposited} \\
\text{Mols SiCl}_4 &= \frac{0.87 \times 1.5 \times 10^{-3}}{170} = 7.7 \times 10^{-3} \\
\end{align*}
\]

\[
\begin{align*}
y_0 &= \frac{7.7}{2.5} = 3.1 \times 10^{-3} \\
c_1 &= \frac{V_0 \times 2.8 \times 10^{-3}}{y_0 \times 2.5} = 0.225 \\
\end{align*}
\]

\[
\begin{align*}
V &= 0.63 = 10^{-3} \left( \frac{y_0 \times 10^{-3}}{x_0^2} \right) \left( \frac{x_0^2}{10^{-3}} \right) = 10^{-3} \left( 3 \times 775 \times \frac{3.1 - 0.9}{2} \right) \times 3.1 - 0.6
\end{align*}
\]

\[
\begin{align*}
y &= y_0 \left( 1 - c_1 \right) \left( c_2 \right) \left( c_1 \right) \left( \frac{2 - c_1}{2} \right) \\
\text{Assume } c_2 &= 0.9
\end{align*}
\]

\[
\begin{align*}
v &= 4y_0 c_4 + y_0 c_2 + y_0 c_1 = 2.1y_0 \\
x^2 &= \frac{4.2}{72} \times 10^{-5} = 0.06 \times 10^{-3}
\end{align*}
\]

\[
\begin{align*}
10^{-3} \frac{\Delta x}{\Delta y} &= \frac{0.63}{1.15} = 1.15 \text{ Check } c_2 = 0.9 \text{ as assumed}
\end{align*}
\]

Silicon "zero" point (no etch or deposit)

\[
\begin{align*}
\Delta y &= \sqrt{3.25 \times 10^{-4}} = 1.8 \times 10^{-2} \text{ (from curve)} \\
\Delta x &= y_0 \left( 1 + 3 \right) = 10^{-3} \left( 3.1 \right) \left( 1 \right) \left( 1.3 \right) \left( 0.85 \right)
\end{align*}
\]

\[
\begin{align*}
\Delta x &= 0.70 \times 10^{-3}
\end{align*}
\]

\[
\begin{align*}
\Delta x &= y_0 \left( 1 + 3 \right) = 10^{-3} \left( 3.1 \right) \left( 1 \right) \left( 1.3 \right) = 0.405 \times 10^{-2}
\end{align*}
\]

\[
\begin{align*}
\frac{x^2}{y_0} &= \frac{2.25 \times 10^{-4}}{1.72} = \frac{1.67 \times 10^{-4}}{1.70 \times 10^{-3}} \neq 0.70 \times 10^{-3}
\end{align*}
\]

Close enough
HCl Corrected 5, HCl₁₃ etch Data

H₂ flow 100% 4" meter glass ball 2.5 g mol/min
10 psig
HCl flow on ½" meter w SS ball temp = 1170° optical
24 psig

HCl, H₂ only

<table>
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<tr>
<th>r</th>
<th>HCl meter</th>
<th>ml HCl/min</th>
<th>pHCl</th>
<th>P₂HCl</th>
<th>X₀</th>
<th>X²(10⁴)</th>
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<td>-1.43</td>
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<td>115</td>
<td>Different temp</td>
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0.50 ml/min 5, HCl₁₃ 2x10⁻³ = X₀

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<th>HCl meter</th>
<th>ml HCl/min</th>
<th>pHCl</th>
<th>P₂HCl</th>
<th>X₀</th>
<th>X²(10⁴)</th>
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1.0 ml/min 5, HCl₁₃ 4x10⁻³ = Y₀

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<th>HCl meter</th>
<th>ml HCl/min</th>
<th>pHCl</th>
<th>P₂HCl</th>
<th>X₀</th>
<th>X²(10⁴)</th>
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<tbody>
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<td>3.75</td>
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FIG. 2

Antimony
P = 0.11 sci
Ga 1250°C, 15 min

$C_2 = 6.5 \times 10^{17}$ cm$^{-3}$
(Run # 47)

$C_2 = 10$ pm
(Run # 43)

Dash
15.9 μ
Dash
20.4 μ

Run # 1-456, Wafer # 3

COMPANY PRIVATE
Fig. 3

$C_0 = 6.2 \times 10^{17} \text{ cm}^{-3}$ (Run #47)

$C_2 = 10^{19} \text{ cm}^{-3}$ (Run #45)

Run # 1-456, Wafer #6

Arsenic

Ga at 1280°C, 16 min

FIG. 3
Fig. 7

Ga @ 1250°C, 15 min

$C_2 = 10^{18}$ cm$^{-3} - 10^{19}$ cm$^{-3}$

dash $J = 9.02 \mu A$

$C_{sub} = 4.5$

$P = 0.009 - 0.015$

COMPANY PRIVATE
TO: List
FROM: C. T. Sah
DATE: April 18, 1963
CC: G. E. Moore, V. H. Grinich

SUBJECT: Agenda for Project Review Meeting
Thursday, April 25, 1963 - 8:30 A.M. to 10:55 A.M.
Impurity Diffusion & Growth Kinetics of Silicon Epitaxial Film Growth
Project 128

The purpose of the meeting is to review the data of impurity profile in epitaxial films and to review the data and model of etching and growth rate of films.

AGENDA:
8:30 Presentation of experimental data of impurity profile for various growth and etching conditions with the various profiling techniques. (Roder)
9:30 Summary of etching and growth rate data and outline of an analysis of the data and the model employed. (Wigton)
10:55 Meeting adjourned

Please have all data summarized and important data and photographs reproduced each for 10 copies for efficient presentation.

C. T. Sah
Solid State Physics Section

CTS:jt

List: (Participants)
A. Roder
H. Wigton
R. Tucker
D. Barry
C. Bittmann
A. Davis
J. Gordon
A. Grove
W. Shepherd
E. Yim
\[ C = k \frac{1}{(V+V_0)^{\frac{1}{2}}} \]

\[ \frac{dc}{du} = \frac{1}{2} k \frac{1}{(V+V_0)^{\frac{3}{2}}} \quad u \gg V_0 \quad \frac{dc}{du} \sim \frac{k}{V^2} \]
### 1962 EXEMPT TERMINATIONS

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Note * --Department was unable or unwilling to complete last column.
**Summary of Experiments**

**EK 1 - 10**

<table>
<thead>
<tr>
<th>Run #</th>
<th>Start Run Date</th>
<th>Wafers Started</th>
<th>Wafers Lost Intentionally</th>
<th>Wafers Lost in Process</th>
<th>Die Sort BVces &gt; N0V</th>
</tr>
</thead>
<tbody>
<tr>
<td>EK 1</td>
<td>1-2-63</td>
<td>50</td>
<td>7</td>
<td>11</td>
<td>2-Etch 1-2nd Mask 5-Ni Plate 3-4th Mask</td>
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<td>1-7-63</td>
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<td>1-Ni Plate 1-3rd Mask</td>
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<td>16</td>
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<td>1-Base Diff 2-Ni Plate 2-3rd Mask 2 Metal</td>
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<td>2-Metal 2-Mask</td>
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<td>6</td>
<td>2-4-63</td>
<td>50</td>
<td><em>Rejected at 2nd Mask due to severe Boron Pitting</em></td>
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<tr>
<td>7</td>
<td>2-11-63</td>
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<td>6</td>
<td>9</td>
<td>1-Oxidation 2-3rd Mask 6-4th Mask</td>
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<tr>
<td>8</td>
<td>2-18-63</td>
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<td><em>Rejected at 3rd Mask due to residue from chromic acid bath which could not be removed</em></td>
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<td>9</td>
<td>2-25-63</td>
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<td>47</td>
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<td>3-Base Diff 2-Ni Plate 3-Mask</td>
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### Summary of Experiments

**E.K. 11-20**

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<tr>
<th>Run #</th>
<th>Start Run Date</th>
<th>Wafer Started</th>
<th>Wafer Lost Intentionally</th>
<th>Wafer Lost In Process</th>
<th>Die Sort BVEES&gt;70V</th>
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<td>69.3%</td>
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<tr>
<td>12</td>
<td>3-27-63</td>
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<td>4</td>
<td>0</td>
<td>62.0%</td>
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</tr>
<tr>
<td>13</td>
<td>4-1-63</td>
<td>50</td>
<td>11</td>
<td>2</td>
<td>72.0%</td>
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<tr>
<td>14</td>
<td>4-15-63</td>
<td>25</td>
<td>4</td>
<td>8</td>
<td>70.0%</td>
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</tbody>
</table>

- Etch
- 1st Mask
- 2nd Mask
- 3rd Mask
# Analysis of Die Sort

**E.K. Runs 1-10**

<table>
<thead>
<tr>
<th>Run #</th>
<th>Run Start Date</th>
<th>Dice In</th>
<th>Good Dice %</th>
<th>Losses by Cause</th>
<th>Total %</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Low B.D BV &lt;=70V</td>
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<td>Shorts</td>
<td>Softs</td>
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<tr>
<td>E.K. 1</td>
<td>1-2-63</td>
<td>531</td>
<td>56</td>
<td>24.8</td>
<td>8.4</td>
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<td>1-7-63</td>
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<td>Lot rejected for boron pits at 2nd mask</td>
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# Analysis of Die Sort 90

**E.K. 11-20**

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<th>Run Start Date</th>
<th>Dice In</th>
<th>Good Dice %</th>
<th>Losses by Cause</th>
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<td>Low B.D. B.V. &lt;= 70V</td>
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<td>20</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Run #</td>
<td>Date Started</td>
<td>Dice Checked</td>
<td>No. of Pipes</td>
<td></td>
</tr>
<tr>
<td>--------</td>
<td>--------------</td>
<td>--------------</td>
<td>--------------</td>
<td></td>
</tr>
<tr>
<td>E.K. 1</td>
<td>1-2-63</td>
<td>50</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>1-7-63</td>
<td>50</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>1-14-63</td>
<td>50</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>4-A</td>
<td>1-21-63</td>
<td>50</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>4-8</td>
<td>1-21-63</td>
<td>50</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>5-A</td>
<td>1-29-63</td>
<td>50</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>5-B</td>
<td>1-29-63</td>
<td>50</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>2-4-63</td>
<td>—</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>2-11-63</td>
<td>50</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>2-18-63</td>
<td>—</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>2-25-63</td>
<td>50</td>
<td>19</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>3-11-63</td>
<td>50</td>
<td>20</td>
<td></td>
</tr>
</tbody>
</table>
# Pipe Count

**E.K 11-20**

<table>
<thead>
<tr>
<th>Run #</th>
<th>Date Started</th>
<th>Dice Checked</th>
<th>No of Pipes</th>
</tr>
</thead>
<tbody>
<tr>
<td>E.K 11</td>
<td>3-18-63</td>
<td>100</td>
<td>37</td>
</tr>
<tr>
<td>12</td>
<td>3-23-63</td>
<td>100</td>
<td>26</td>
</tr>
<tr>
<td>13</td>
<td>4-1-63</td>
<td>100</td>
<td>24</td>
</tr>
<tr>
<td>14</td>
<td>4-15-63</td>
<td>100</td>
<td>26</td>
</tr>
<tr>
<td>15</td>
<td>4-25-63</td>
<td>100</td>
<td>28</td>
</tr>
<tr>
<td>16</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Pipe Incident Vrs hfe

**E.K 1-10**

<table>
<thead>
<tr>
<th>hfe</th>
<th>No Visible Pipes</th>
<th>Visible Pipes</th>
</tr>
</thead>
<tbody>
<tr>
<td>&gt;100</td>
<td>0, 0, 1, 5, 2, 0, 0, 0, 5, 1, 2</td>
<td>0, 0, 0, 0, 0, 0, 0, 0, 0, 1, 1</td>
</tr>
<tr>
<td>70-100</td>
<td>2, 3, 2, 3, 2, 4, 3, 2, 5, 2</td>
<td>1, 0, 1, 0, 0, 0, 0, 0, 0, 2</td>
</tr>
<tr>
<td>&lt;70</td>
<td>7, 6, 2, 1, 6, 6, 7, 0, 3, 1, 2</td>
<td>0, 1, 4, 1, 0, 0, 0, 0, 0, 2, 1</td>
</tr>
<tr>
<td>hfe</td>
<td>No Visible Pipes</td>
<td>Visible Pipes</td>
</tr>
<tr>
<td>-----</td>
<td>-----------------</td>
<td>---------------</td>
</tr>
<tr>
<td>&gt;100</td>
<td>0, 5, 0, 0, 3</td>
<td>0, 1, 0, 0, 2</td>
</tr>
<tr>
<td>70-100</td>
<td>1, 2, 0, 2, 3</td>
<td>3, 1, 0, 2, 2</td>
</tr>
<tr>
<td>&lt;70</td>
<td>4, 1, 9, 0</td>
<td>2, 0, 1, 0, 0</td>
</tr>
</tbody>
</table>
Experiment run to keep both at 1050 am
by identical process then check changes at a later

Useful experiments to do:
1. Ap-type wiper in an ox furnace to check for diffusing pipes.
2. A fresh spotless wiper to see if pipe at base diffusing clatter.
3. Check wiper (afternoon) after base diffusing for each spot, with the CP to check. We will run both these people.
1. The base pumpkin point pipe

This kind of pipe can be removed by etching off 1/2 of Si.

It is important to note that this type pipe gains a 'soft' characteristic.

Get some or good wafers from Paul Hill.

These wafers had way far of the other kinds of point pipes.

2. Irregular circle pipe -

These can occur irregular in the surface.?
PIPE PROJECT REVIEW OUTLINE

PROJECT NO. 105
J. E. Lawrence

I. OUTLINE FOR STUDY:
   A. Define problem
   B. Establish methods of analysis
   C. Determine priority for investigation
   D. Is this particular type of pipe associated with
      1. Dislocations (bulk or surface)
      2. Contamination
      3. Poor oxide mask?
   E. Can this particular type of pipe be produced at will?
   F. What is this pipe as defined by
      1. Electrical theory
      2. Crystallographic theory
      3. Chemical theory?

II. DEFINE PROBLEM:
   (Find causes for all localized centers of undesirable electrical activity)
   A. Categories:
      1. Base periphery point pipe
      2. Irregular oxide pipe
      3. Regular oxide pipe
      4. Diffused pipe

III. METHODS OF ANALYSIS:
   A. Characteristic electrical trace
   B. Emission under reverse bias (2000x)
   C. Location and natural surface appearance
D. P-N stain (CP-20 and intense light)
E. Light preferential etch (CP-10)
F. Diffusion profile or pipe and near environment (SIRTL)

IV. BASE PERIPHERY POINT PIPE (193 OF 205 DEVICES TESTED)
A. Soft junctions, not low breakdown voltages, \( I_{CBO} = 50 \text{ ma} \)
B. Emission from points
C. No surface appearance
D. Stains as n-type
E. No dislocation etching
F. No diffusion profile
*G. Can be eliminated by removing 1.2\( \mu \text{s} \) of device by 1 minute SIRTL etch

V. IRREGULAR OXIDE PIPE (% VARIES, NORMALLY 80% OF ALL PIPES)
A. Low breakdown voltage, saturated leakage current
B. Emission from line or ring (individual microplasmas and internal field emission)
C. "Crystalline" oxide of different thickness from normal
D. Stains n-type
E. No dislocation etching
F. Very unique diffusion profile (mesa and trough)
*G. Can create crystalline oxide at will from contaminant
VI. REGULAR OXIDE PIPE (% VARIES, NORMALLY 20% OF ALL PIPES)
   A. & B. As above in V
   C. Regular oxide no discoloring
   D. Stains n-type
   E. Bar dislocation pattern usually
   F. Diffusion profile (mesa no trough)
   *G. Both this and the previous pipe are not positioned relative to any device. (Found in base and collector)

VII. DIFFUSED PIPE (Not widely studied yet)
PLAN PROJECT REVIEW OUTLINE
J. E. LAWRENCE

REGULAR OXIDE PIPE

(1) SIRTL etched one minute
(2) Mesa extends 1.2 microns above the base
(3) Mesa surface dimensions 9 X 13 microns
(4) Emission ring
(5) Leakage current 12 ma
(6) Low breakdown 20 v
(7) Normal breakdown 115 v
(8) Cross section

(9) Electrical characteristics

(10) Photograph
This method of preferential etching is now the best way to delineate pipe.

This blistered oxide is related to surface contamination.

3. Regular oxide pipe

Same U-1 characteristics.

This etch to make a mesa, but will no menat, etc.

original surface

after SMT etc.

atami as a U-1 pattern plot comes well light-sensitive

these develop pits on etching

Favorene has observed a correlation of softness and HF dilution.

He has etched an irregular oxide pipe picture and placed it through the box.

Tough etch: #1 793/205% will last at best one of three.

#2 soft etch density

#3 About 1/5 density

#4

→ John — 1. Not good uneven

2. Examine when the non-stable propagations are.

The concentration of Grade and contamination is now very high.
Flint

looking at surface from hills but material will sink etch.

etch the cold steel ball points on mean edge of copper.

with the small copper plate during a related high concentration over in an ammonia ring which the cold water mix near the pipette.

Flint points out that in straight HCl service we are in the region where Cu plate out. This occurs for acid, a basic soln of HCl containing fluoride.

Cu contamination gives characteristic stain. (see 1-10 fig.)

Fe

The rounded area like in 1-14 show some peculiar long range order.

Hypotheses:

1. Surface gets contaminated roughly uniformly with metal up.

   This needs detailed log out. I'll work that out with Flint.

Chink:

For work on a 1454 C or radiation diffusion.

Some fused optics have evidence B + P diffusion.

Many correlate with KPR pipeline.

Harder and defects (order 63X) did not correlate with pipe diffusion, than the etched. Why are these positive,伸びた(20X) and different.

some pitted near top occur with no porosity - so, they are contamination.

Cu type pits did not correlate with pipes. - Many more pits than pitted.
An irregular oxide pyte
after etching.

From Elin Laurene

4/30/63  500 X
4200 Wafers (Krueger's - Mt. View)

Gave Dash Etch after each of the following steps:

1. Chemical Etch
2. Oxidation
3. First Mask
4. Base Predep
5. Base Diffusion

Results: Not definitive. Obtained chiefly small or pits randomly distributed in (1). After (2) they were denser in an annulus next to the crystal skin. A few dumbbell pits were observed very near the skin. After (4) observed greater density of small pits in base.

Need to repeat on more wafers, particularly on rejects.

Studies of Bulk Material

Attempts at deliberate contamination of wafer surfaces. Using 0.5 ohm-cm. material, although 0.005 material showed no real difference.

Copper Contamination from Aqueous CuCl₂

1. Straight Aqueous - no plating of copper
2. In HF Medium - copper plates out readily
3. In HF + HNO₃ Medium - copper does not plate out

After exposure of the wafer to copper in one of the above ways, the wafer was oxidized, the oxide removed in HF, and defects were delineated with Dash Etch.

Results: All types of exposure to copper gave characteristic etch pits after oxidation (see photos), but the large amount of copper obtained from HF alone gave most definitive results. The copper plating appears to be a displacement reaction.

Overall, we must conclude that we can readily contaminate our wafers from pure HF solutions.

Iron Contamination from Aqueous FeSO₄

Iron did not plate out from HF medium, but did give characteristic etch pits (see photos).

Present studies are covering Phosphorus Contamination. There may be some preliminary results to report.

Quenching Effects

Dislocations loops are commonly formed in metals by quenching in a high concentration of vacancies.

Methods of Cyclic Quenching:

1. Cycle from 1200°C. in steam to 25°C. (ordinary cooling)
2. " " " " " " " " " (water quench)

The above can be done with or without previous longer oxidation.

Results: In each case, obtain lines of rounded triangular etch pits, probably indicative of slip traces. Also obtained vestiges of loops. Should combine with metal contamination.
P-14
(1) CP8 Etched
(2) HF + FeSO₄
(3) Oxid. 14h @ 1100°C in O₂
(4) Dark Etch.
Dendrites (Stars) (200X)

P-14
Line Pits
(with fine structure) (400X)

P-14
Rounded Triangular Pits
distinctively oriented (200X)

Iron Contamination on Silicon Surfaces

P.S. Flint
4/29/63
Copper Contamination of Silicon Surfaces

P-16
1. CP-8 Etch
2. Oxid. 4 hr @ 1200°C, steam
3. HF + C6Cl6
4. Oxid. 30 min @ 1100°C O2

(200X)

P-10
1. CP-8 Etch
2. HF + C6Cl6
3. Oxid. 30 min @ 1100°C O2
4. HF stripped

(100X)

P-11
1. CP-8 Etched
2. CPb + C6Cl6
3. Oxid. 30 min @ 1100°C O2

(100X)

Afer oxide stripped and the surface section etched.
Cyclically Quenched Oxidized Silicon Waters

P-15
1. CPS Etched
2. Cyclic Oxidation (4 cycles)
   5h at 1200°C in steam,
   cooled (standing) in air 5h.
3. Dash Etch.
   (200X)
   Slip Traces?

P-15

(400X)
Loops?

P-20
1. CP-8 Etched
2. Oxid. 4h at 1200°C in steam
3. Cyclic Oxidation (4 cycles)
   10h at 1200°C in steam,
   Quenched in H2O.
4. Dash Etch.
   (400X)

P. L. Flint
4/29/63
FAIRCHILD SEMICONDUCTOR
RESEARCH & DEVELOPMENT LABORATORY

TO: List
FROM: C. T. Sah
SUBJECT: Agenda for Project Review Meeting - Tuesday, April 30, 1963

DATE: April 25, 1963
CC: G. E. Moore
V. H. Grinich

AGENDA:
8:30 - Categorize the Observed Pipes and Diffusion and Oxidation Defects (Lawrence)
Experimental Results on 4200 CB Diode Rejects (Lawrence)

9:30 - Induced Pipes and Dislocation by Surface Contaminants (Flint)

10:30 - Pipes from Weak Oxide (Ornik)

Please have all data summarized and brief outline of discussion reproduced (10 copies) for distribution prior to talk.

CTS:jt
LIST:

J. Lawrence
P. Flint
L. Ornik
P. Ferguson (2)
G. Reddi
W. Shepherd
R. Tucker

RECEIVED
APR 26 1963
V. H. Grinich
SUBJECT: Project Review on Oxide Defect Studies in Conjunction with SCR Development

DATE: April 30, 1963

1. The four layer SCR structure requires p-isolation diffusion. A single pipe within the 60x60 mil area will diffuse through the future active area and either produce a short or decrease the available width for depletion layer (Fig. 1, 2).

2. Pipes originating through photoresist pinholes are due to mask imperfections or due to local photoresist breakdown (Fig. 3, 4). They extend to the same depth as the isolation diffusion. The pinholes can be observed under 100X magnification.

3. Some pipes can originate prior to first oxidation as evidenced by leaving a wafer in oxidation furnace until they diffuse to sufficient size to be suitable for staining (24 hr. at 1200°C). With good housekeeping rules this pipe count has been kept between zero to five pipes per wafer.

4. However, eliminating the photoresist process and predepositing and diffusing the unphotoresistted wafers, a substantial density of pipes was still present. Only few of these pipes could be related to visible oxide imperfections (Fig. 5).

5. Chlorine etch showed two defects on a wafer from a run with pipe counts in the order of 100 per wafer.

6. Boron particle deposition was shown to occur during predeposition by diffusing wafers which have partially stripped and not stripped at all (Fig. 6). Non-dipped parts of wafer showed higher pipe densities with many small and many very large irregularly shaped pipes. However, any amount of stripping (including total strip) beyond 30 seconds 2 DI:1 HF has not improved the pipe count significantly (Fig. 6).
7. Method for lapping and staining the wafers for pipe detection was time consuming even without the long diffusions needed to attain pipes sufficiently large for visual observation. It was noticed that a wafer predeposited with boron and then CP-6 etched for 2 minutes:

a. shows no pipes upon diffusion
b. develops a density of etchpits similar to the observed pipe densities (Fig. 7).

8. A further experiment was performed which indicated that CP-6 induced etchpits on original oxide do correspond closely to the pipe condition when a 2-minute CP-6 etch time was used. (Fig. 8) A three-minute etch results in number of etchpits which is about twice the number of pipes introduced with 190°C predeposition to V/I ~ 1.0 and diffusion at 1280°C. Thus, although CP-6 is a convenient means of oxide imperfection detection, the etch time has to be tailored to suit each diffusion condition.

9. Using CP-6 etch the effect of various materials was evaluated, as shown in Table I. Even in the case of not purposely contaminated wafers the etchpits could be correlated to surface contamination or surface damage (Fig. 11B). Thus, the effect of material appears to be insignificant. A rare case of an etchpit on top of a pyramid (Fig. 9) was possibly induced by oxide abrasion after oxidation. Examples of water drop contamination are shown in Fig. 10, 11.

10. Further two-minute CP-6 checks of treatment prior to oxidation show:

a. Nickel tweezer scratch no etchpits (Fig. 12)
b. Steel tweezer scratch 6 etchpits at the end of the scratch (Fig. 13)
c. Silicon scratch no etchpits (Fig. 14)
d. KPR residue (polymerized but not developed)  
   no etchpits (Fig. 15)

e. Fingerprint  
   many etchpits (Fig. 16)

f. Mechanically polished wafer  
   56/wafer

g. Mech. polish and Chem. polish  
   (24 µ removed)  
   14/wafer

h. 2 hr. dry O₂ oxidation + 2 hr. steam oxidation  
   4 /wafer

i. 2 hr. steam oxidation (1200°C)(control)  
   1 /wafer

11. It was found, however, that the damage to oxidized wafer can be induced quite readily with:

a. Silicon scratch (Fig. 17, 17A)
b. Abrasion between a silicon wafer and an oxidized wafer (Fig. 18)
c. Nickel tweezer prick (Fig. 19)
d. Carboloid scriber prick (Fig. 20)
e. Diamond scribe prick (Fig. )

No etchpits could be discovered after stainless steel tweezer prick. Evaluation of abrasion between wafers in a typical ultrasonic agitation, including dust from broken chips, has not been completed.

12. In most of the CP-6 etching a fine array of small slightly deeper etched oxide spots has been observed. The size of the spots is about 2µ and the density varies from about 1 to 10 per 25µx25µ area. (Fig. 22) The origin of the dots will not be investigated at present.
<table>
<thead>
<tr>
<th>SOURCE</th>
<th>TYPE</th>
<th>$n_2$ cm</th>
<th>WAFFER Dia.</th>
<th>WAFERS 1 to 7 etched 60µ each side, rinsed in DI, blown dry &amp; immediately oxidized 2 hr at 1200°C; others as noted.</th>
<th>NO. OF ETCH-PITS PER WAFFER</th>
</tr>
</thead>
<tbody>
<tr>
<td>FT(Sterling Rd.)</td>
<td>N</td>
<td>28</td>
<td>27</td>
<td></td>
<td>9</td>
</tr>
<tr>
<td>KEP</td>
<td>N(Sb)</td>
<td>52</td>
<td>24</td>
<td></td>
<td>8</td>
</tr>
<tr>
<td>DOW Corning</td>
<td>N</td>
<td>41</td>
<td>32</td>
<td>Float-zoned, disloc.dens. 20,000 cm$^{-2}$ min.</td>
<td>3</td>
</tr>
<tr>
<td>KOLLSTAN (As)</td>
<td>N</td>
<td>28</td>
<td>24</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>KOLLSTAN (P)</td>
<td>N</td>
<td>33</td>
<td>24</td>
<td></td>
<td>3</td>
</tr>
<tr>
<td>TI</td>
<td>N</td>
<td>80</td>
<td>19</td>
<td>Pedestal grown disloc.dens 2,000 cm$^{-2}$ max.</td>
<td>16</td>
</tr>
<tr>
<td>DUP (St. Rd)</td>
<td>N(4200) 1.6-2.0</td>
<td>24</td>
<td>Front side (normal lap)</td>
<td>Rear side (rough, saw marks)</td>
<td>8</td>
</tr>
<tr>
<td>7A</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DUP (St. Rd)</td>
<td>N(4200) 1.6-2.0</td>
<td>24</td>
<td>Blotted dry w/filter paper and left exposed on lab bench for 2 hours. Handled with tweezers which have not been CP-6 cleaned.</td>
<td>251</td>
<td></td>
</tr>
<tr>
<td>9 DUP (St. Rd)</td>
<td>N(4200) 1.6-2.0</td>
<td>24</td>
<td>A drop of DI rinsing water left to evaporate. Etchpits along the edge &amp; within 4mm diameter of the water mark area.</td>
<td>117</td>
<td></td>
</tr>
</tbody>
</table>

The following data is from various test wafers which were not part of the above experiment:

| SCR 71              |     | 19       | 24          |                                                                                                          | 74                          |
| SCR 77A(KOLLSTAN)   | N    | 31       | 24          |                                                                                                          | 61                          |
| SCR 79 (St. Rd)     | N    | 8        | 24          |                                                                                                          | 32                          |
| SCR 79 (St. Rd)     | N    | 8        | 24          |                                                                                                          | 14                          |
| SCR 80 (St. Rd)     | N    | 8        | 24          |                                                                                                          | 32                          |
| SCR 81 (St. Rd)     | N    | 8        | 24          |                                                                                                          | 44                          |
| REP IV (µL)         | P    | 2        |             | OXide 1.5 hr at 1200°C                                                                                   | 58                          |
Date, time of t, predicts m between pipe - Up to 30 sec the number of pipes are decreasing. If diffusion starts will steam diffuse, then, even completely stripping gets to minimum pipe density.

Hydride in that B-containing particles are side surface precipitate. Spotty precipitate (4, 2 min)

A wafer dipped in CP-6 twice no pipe - Caution in CP-6 attaches the pipe.

On one wafer 2 min CP-6 corresponds to 8 precipitate.

Plan:

Amni.

Why diffusion in regain oxide.

Mat in how is oxide damaged after growing.

Who is going to do the equivalent of P? (see JPF first)
\[ h = \frac{C(S, 12)}{C(S, 5)} \]

Ataka tried to confirm these results — and did. — We disagree on 10^6, 10^7.

From the previous analysis of where a \( x \)大事ly depended while \( 10^{-10} \) we confirm \( h \approx 10^{-3} \).

Consider the solution from the energy band point of view.

Analysis technique:
\[ C = \frac{kE_0}{Q} \]
\[ Q = \int N(x) dx \quad C = \frac{dQ}{dV} = \frac{dW}{dV} N(W) \]
\[ N(W) = -\frac{C^2}{kE_0} \frac{dV}{dC} \]

2. M - O - S Capacitor

Cost \( C_P \) — majority charge cap.

\[ V_{\text{applied}} = V + \Delta V \]
\[ C = \frac{dQ}{dV} \quad Q = \int [C(P - m) + \ldots] \Delta V + Nt \int [N_0 + N_t] \Delta V dx \]
This can be related if $N_T$ and $C$ are constant:

Consider a high voltage $V$.

\[ C = \frac{C_0(C_0 + C_L)}{C_0 + C_L + C_m} \]

At high frequencies, the degenerative nature, $C_m$ will not be seen.

OK, if the oxide is thick, we get a depletion-type situation, and

the capacitance of a reverse biased junction
Ox. condition

\[ T = 1250 \]
\[ t = 2.15 \text{ hrs} \]

Dry \( \text{O}_2 \), wet \( \text{O}_2 \), steam, \( \text{N}_2 \)

---

For the measured conductance, the \( C \) is \( \sim 2x \) at high \( C \) and \( \sim 10^{-1} \) at low \( C \).

---

\[ C \approx 10^{-3} \times 10^{-16} \]

This lump seems characteristic of \( \text{Bf}_2 \); a lower conductance.

---

Getting conductance \( C \), set \( \sim 7 \times 10^{-15} \) for \( C \). Get \( k \approx 12 \) for steam + \( \text{O}_2 \).

---

\( \text{Ga} \) also out-diffuses in \( \text{O}_2 \), but definitely more in \( \text{Ni} + \text{H}_2 \), not to correspond to \( \text{O}_2 \) oxidation rate.

---

In \( \text{O}_2 \) diffusion, \( \text{O} \) rises.

---

\( \text{MoS}_2 \)

---

is, all strongly \( \text{O}_2 \)-type surfaces.
Three approximations of \( C_i \):

1. \( N_D - N_P + p - m \) (Ent field change, most likely)
2. \( N_D - N_A + p \) (electric can't follow)
3. \( N_D - N_A \) (leaky oxide)

2 or 3 run them together.

Assume effective surface states charge:

1. \( \xi_s \)
2. A correction for effect of lowering by just enough

\( \frac{1}{\alpha_x} \)

\[ V_C + \phi_s + \phi_s + \phi_s \]

Need \( \phi_s + \phi_s + \phi_s \)

With the curve, get \( \phi_s \)

a. Field of curve
b. \( \phi_s \) offset
3. \( \phi_s \) offset
4. \( V_B \) for major minus

Red:

various oxide compared

but oxide varied, but all showed

dry oxide was uniform, but didn't get back up
people went to pot
another asked a very an an emission of 2

The diode constant was all over the map. Only the dry or
agree well with the fixed Si or rules
May 6, 1963 — Thin film resistors — Planning meeting

ref. p. 113 (4/4/63)

On question from last time:

1. NiCr + Ta spotted film — no results yet.

2. A couple of runs of NiCr at high <100-210 (30-90) seem to show the same range of percentage variation during alloying.

3. The double masking to avoid the alloying cycle does not really seem to work yet.

My evaluation of the status of thick film films:

At present they are useful only if a ± 50% variation in the un-adjusted resistor can be used. In that case, the results are significantly better, although I am not sure how close.

The FCC films are Pe 90%, Pe 10% 6.8 kg dyns aging in air. They died down 150 to 600 dyns after aging.

On Ta — Nobody talks about a half if T cycle. Everybody knows it covers a thermal aging step.

There is a strong indication that the thick film films do not vary randomly but change abruptly. It seems possible to run a test which to determine how the system is behaving and then adjust the monitor value accordingly.

Hsiao Hung will run thickfilm with this test wafer method.

We will have a man spontaneous to try to do the effect of residual gases. If it trades things down, we'll try out.

We will also try to see why film work.

a) Labeled
b) Chemical compositions
c) A structure
**Table III**

Mean res. change a. TCR for different alloying ambients
(2 min 580°C in clean furnace). Film evaporated from Ni-Cr wire. Substrate temp. 350°C.

<table>
<thead>
<tr>
<th>Run#</th>
<th>Cool down in air</th>
<th>10 min cooldown in N₂ or Ar</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>alloyed in N₂</td>
<td>Ar</td>
</tr>
<tr>
<td>63</td>
<td>-4% +250</td>
<td>-6.8%</td>
</tr>
<tr>
<td>64</td>
<td>-16.8% +160</td>
<td>-8.9%</td>
</tr>
<tr>
<td>65</td>
<td>-18% +350ppm</td>
<td>-13.4% +380ppm</td>
</tr>
<tr>
<td>66</td>
<td>-21.3% -12.4%</td>
<td>-19.2%</td>
</tr>
</tbody>
</table>

*(Previously all changes were indicated by *)

**Table IV**

Mean res. change for alloying in clean furnace and in standard furnace. Film evaporated from Ni-Cr wire, substrate temp. 350°C.

<table>
<thead>
<tr>
<th>Run#</th>
<th>Standard form, 2 min 580°C, N₂, cool in air</th>
<th>Clean furnace, 2 min 580°C, N₂</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Cool in air</td>
<td>10 min cool in N₂</td>
</tr>
<tr>
<td>69</td>
<td>+19%</td>
<td>+19%</td>
</tr>
<tr>
<td>70</td>
<td>+3%</td>
<td>-3%</td>
</tr>
</tbody>
</table>

(5 min cure at 650°C in vacuum)
### Table V

Res. change of films on different substrates.
(2 min 580°C N₂ alloying, Evap. from Mîc. wire, Substrate at 350°C)

<table>
<thead>
<tr>
<th>Run #</th>
<th>Cooling in air after all.</th>
<th>Cooling in N₂ for 10 min.</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Si-SiO₂ - wafer</td>
<td>micr. glassslide</td>
</tr>
<tr>
<td>68</td>
<td>-4%</td>
<td>sl. 1</td>
</tr>
<tr>
<td>72 Cen. furn</td>
<td>-19%</td>
<td>+5%</td>
</tr>
<tr>
<td>73 Cen. furn</td>
<td>+4%</td>
<td>+6%</td>
</tr>
</tbody>
</table>

### Table VI

Res. change for different alloy temperatures.
(Evap. from wire; Substrate at 350°C; 2 min in N₂, cool down in air; stand. furnaces)

<table>
<thead>
<tr>
<th>Run #</th>
<th>Alloy T⇒</th>
<th>550°C</th>
<th>5 65°C</th>
<th>580°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>71</td>
<td>+4%</td>
<td>+2%</td>
<td>+7%</td>
<td></td>
</tr>
</tbody>
</table>
a) Q. Is a "red" alphabet equivalent to a frankly critical book? Henry Hepp will answer this one.

b) Q. We know that contact resistance does not better we in the 2-3x resistor range. What is the influence of contact resistance? We will design a unit and contact resistance measuring probe that allows a definitive statement of what the contact resistance is.

c) Q. What physical phenomena correlate with the change?

- Can measure
- dV/dT
- Hall effect
- Angle from ellipsometer
- Electron probe
- Diffraction

d) Q. What process variable is it?

The man spectrometer is on best bet.

For the TA work:

1. Prepare a quoting capability on ceramic - get a test vehicle from D.D. that they would use.
   - Henry will supply test vehicle.
2. Track down problem ASAP
   - Join have a program laid out on a few and will need a copy to me.

The helium read back double at 5 AM. Be vacuum edited, and read to come in, data looks pretty good will +35% or better. Ready for a Per Dev. test vehicle.

Per phase Consute for most all being possible for ceramic switches.
On the epi

Cam yield (lot) > 5000

Faults before die out < 1.7%

12,000 in (25 units) @ 200°C strong = 2 failures

1. Busted
2. "Vanishing metal" open (also lots with)

02,000 in lot of 0.15% - no failures, but much scaling

More than a little problem with drift of units of originally high leakage. Jim
does not think that it is clean.

In order to eliminate the "vanishing metal" problem, M.U. has stopped using

about 3/4 of M.U. foil as crystals across the isolators. They had high 1/4

one long isolation (diffusion). We have not seen the problem up here. Roy is shopping

for ASG.

Both Section

RTV II running the B8, F, C deal.

Mti. They is finding up their testing reactors.

Kit. Components:

Transistors: KTA (10 ma)
KTB (4 KTA)
KTC (Metal pair of Weston, somewhat larger emitter)
KTD (KTA + 100 ma)

Resistors:
R-1 & R-2 The old pk, made long ago.

R-1 New, used (old made to

short 

R-2 long ago, new made, 

epi test)

A test vehicle to compare 0.5, 1, 2, 6a, FET, reactors is in the mill.

Diodes: Use the multiple emitter of a KTA.
There are many in the strong team, ranging 8-30 ms and more, facing problems and want to look like a problem in keeping the time.

We are presently running 10-14 ms and try hard that possibly will settle the problem and bring the time we can get them all <10 ms.

1. Epitaxy - is good control for min violation
2. Opt. coil - perfect?
3. What is we need a coil control? - What anyway reduction?

- Straight

As soon as these are licked down, we feel that our technology is the one we must ride with.

A major problem looks like the probing of die. It starts to look impossible.

Chat form 2: - Form 2

A lot of people have T2L.

Psi is probing.

Silicono is routed briefly, then changed it into a non-set membrane.

<table>
<thead>
<tr>
<th>Name</th>
<th>T (ms)</th>
<th>Pd</th>
<th>Feature</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPC, T2L</td>
<td>10-14</td>
<td>15</td>
<td>15</td>
</tr>
<tr>
<td>Silicono</td>
<td>12-15</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>(Lift-hand) Sightline</td>
<td>20-30</td>
<td>6</td>
<td>10</td>
</tr>
<tr>
<td>FSC, T2L</td>
<td>12</td>
<td>5-6</td>
<td>13</td>
</tr>
<tr>
<td>DTL</td>
<td>10</td>
<td>5-6</td>
<td>13</td>
</tr>
<tr>
<td>MECO</td>
<td>3.5</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>FSC, DTL</td>
<td>3.0</td>
<td>3</td>
<td>10</td>
</tr>
<tr>
<td>DCTL-2</td>
<td>8</td>
<td>15</td>
<td>10</td>
</tr>
<tr>
<td>CML #1</td>
<td>5-6</td>
<td>15</td>
<td>20</td>
</tr>
</tbody>
</table>
We modified to:
1. Put 2 followers on input to new steady flow.
2. Add 2 count source.

Our is not very powerful logically - various functions are difficult.
The mask is just about ready to be cut for our new CMOS gates.

What are the requirements for an new family of digital circuitry?

1. No DTL
2. Highest possible speed (or less power at reasonable speed)
3. Powerful logical capabilities including a do-able binary.

Some points on that by using semi-gated DTL for low power like good, it is not compatible well anyway.

Main device:

DNN shift register - Don Tomin line reservation about our objective. It has delay line capabilities, however.

There is evidently useful one for some extremely specific use of a register. Arguments against it are one of compatibility.

Power modification gives for CI diffusion and an epitaxial growth. Be close to plan properly. We only advantage in edge.
TO: G. E. Moore
V. H. Grinich
FROM: J. P. Ferguson
SUBJECT: Agenda for Digital Integrated Circuits Project Review

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Status of Epitaxial Micrologic (15 min.)

- Mt. View status
  1. Characterization
  2. Process differences
- Life tests
- Kit parts

Future Process Work (15 min.)

- Oxide/metal improvement
- Epitaxy
- Size reduction
- Resistors

Circuit Forms

- Competitive evaluation
- High speed
  1. CML - straight and differential
  2. Improved DCTL
  3. Binary implementation possibilities
- Low Power
  1. Non-saturating NAND
  2. DCTL
  3. Binary implementation possibilities

Miscellaneous Circuits (30 min.)

- PNPN registers
- Diode converter and diode matrices

JPF: jh
to pursue a slot hole.

which then gets changed to something "horrible complex" using p-type MOSFET with added kink and even a Zener diode.

As near as I can see this whole area of digital integrated circuitry is fully up in the air. I have no confidence in an 'layout of program.'

Dick matrix? - This is still alive?

Also trying complement.

Try to sell restoring by this.

If this goes on, it shall be an object. Can get a Birger-Joan Carlini 3x4x0 one.

For some reason that escapes me this is a strong effort to make everything more complicated in order to fit it into the PCB processing exactly.
General discussion 2-3 June 1963

Process control limitations: drift (day to day) + trend (day to day)

Low level (a relatively long lasting market) 0-50 mV
High level (a very small market) 0-5-7 V

We see 1% and not excellent, realistic characteristics.

The low level stuff should be 500 R bridge

And be 100-500 ohm/1% in

30-130°F 1 1/2 %

Need for extended range, the rod in steel
-65-250°F

Make 0.01%/°F or 0.05, thin and sensitive.

People are putting for ± 0.005 to 0.003, now take 0.005.

High level arc

Use an arc weld, power 25-300 W

Smaller and countable (all visible)
5 V out

Use 2 or 3 or 6 in contrast linear + logarithmic.

Shunt calibrator

100 W output: singalize.

Must take a "fell of a leading" -65° ~ 200°F

Must be <1000, pref ~ 500.

The high level market in 1975 ~ 1M$/year

As far as there in concerned, more are interested at all
in anything but 0-50 mV or 0-5 V. "The gap that when
250 mV must have been a pound on their balance":

A 0-15 lb wet-wet differential would be a world better.
1. The will check possibility of a replacement front door.
2. A different model. He will get Moore's recommendations.
3. I will investigate channel of he can build one in a finite amount of time.

"If we can spend $15k to get on the air quickly, we will be happy to fund the tech to write manual."