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FAIRCHILD SEMICONDUCTOR

Memo From Central Region

DATE: November 8, 1962

CC: W. Richmond
R. Graham
~~C. Sheridan~~ al mattal

TO: T. H. Bay

FROM: Bernard T. Marren

SUBJECT: Avco - Cincinnati Power Transistor Requirement

ANSWER REQUIRED BY:

Dear Tom,

Per our conversation of this week, I am enclosing a copy of Avco's tentative specification requirements for a power transistor.

Avco is interested in giving us a development contract for this type of unit.

The dollar figure they talked about is $25K to $50K. For this they would expect about 12 units for evaluation in six to eight months.

They would also consider something in the area of $1,000 each for the first 50 units and $100 each for subsequent orders.

P.S.I. has looked at their spec but as yet they have made no definite proposal.

I promised Avco an answer by November 16, 1962.

Regards,
Bernie

Gordon —
PLS CALL BAY AFTER YOU LOOK AT THIS.
DAB 11/12

15 August 1962

E. G. Spierling

PRC-42

Power TRANSISTOR REQUIREMENTS

High Power

One device or max. of 2 in parallel

Power Output (RF)

40 watts min. at V_{cc} = 28 VDC

Class of Operation

AB Linear

V'_{cc}

28 volts standard
18 to 30 volts service

Frequency

88 mc.

Power Gain

10 db min. over frequency range

Neutralization

None

Emitter Tuning

None

Collector

Collector DC and RF isolated from case. RF isolation impedance of 500 ohms min. over frequency range.

Mounting

Stud

Leads

Axially or collector separated from base and emitter as much as possible.

Collector Efficiency (RF out vs. DC in)

45 percent min. at max. drive.

Material

Silicon

Distortion

Output intermodulation distortion products shall be at least 25 db below one of (2) two equal amplitude desired tones; the amplitude of the tones such that the peak envelope power output can be from 0 to 40 watts at V_{CC} = 28 VDC and the tone frequencies can be anywhere in the 2 - 30 mc range but separated from each other by 500 cps.

DC Beta Gain

15 min.

Temperature

Operating	-40°C to +65°C
Storage	-65°C to +100°C

August 15, 1962

H. C. Spierling

TRANSISTOR REQUIREMENTS

Low Power

One device

Power Output (RF)

4 watts min. at V_{ce} = 22 VDC

Remaining requirements same as for high power device.

Problem:

D.C. & RF isolation from case

axial leads

4 watts at 88 Mc, Class AB must mean something abt power dissipation.

Review of Power Device data – 11/15/62

Grinich, Sparks, Lamond, Fogiet, Underwood, Moore, Bay, Richmond, Yost

Our reverse epitaxial is not quite there –
It is only 1 ~~[illegible]~~ mm anyway and it has ~~high~~ low BV_{CBO}.

On triple diffused, Mtn View is working

On Westinghouse 17, 12, 7 % on 3 runs at 7000 diesort to collector-base and emitter-base junction.
$LV_{CEO} \geq 100v$.

Planar material: 35 % on thick base

Some material of many kinds there. Nothing conclusive, as far as I am concerned.

 Meeting 11/19/62 - New policy - planning meeting. Ferguson Farina Smith Schultz Seeds

G.M. Kick-off

D.F. Meet on epitaxial development: 1 for low power
1 for highest speed

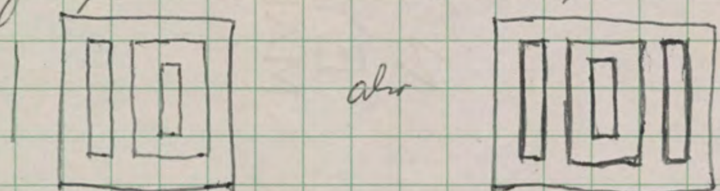
The material: (substrate ~6 Ω-cm p-type

	L.P.	H.S.
	0.5 Ω-cm layer	0.2-0.3 Ω-cm
	10-12 μ thick	8-10 μ
	1000°C Au	1100°C Au
	(KT-1-mini Xstor with rules)	KT-1
W_f		6-8 fingers
C_{ob} 5V	3pf	4pf
C_{TE} 0.5V	3pf	4pf
τ_s	<20 ns	<10 ns
V_{SAT} (ĉ prady)	~10Ω	~10Ω
DCTL t_{pd}	60 ns @ 1 mw	9-11 ns @ 15 mw, -55-125°C (on igt gate ĉ midrange)
r_e	<5Ω	<5Ω

# of runs: ➤ (of gates) (1) (1)

We have also a test vehicle which makes four different Xstor geometries

More run of separate Xstors in mil. These have geometries like.



Scale: 1/4" = 0.001"

These violate the rules for metal cuts.

Nov. 19, 1962

February Production

	Micrologic, M.V.		ML, Palo Alto	New Family
Nov. 19			epi D. F. -10 Gate Mask Must be μL Replacement	D. F. - 60 R. S. - 70
Dec. 1	Define Changes 1 step		D. F. S. Mask P. L. G's out 2 runs	Layout Start +
Jan. 1	MT. VIEW EVALUATION | All Masks Available	MT. VIEW EVALUATION	S out, 2 runs Prod. Facilities 10 runs ea. G-S @ R&D	Start 10 runs
Feb. 1	MT. VIEW EVALUATION	MT. VIEW EVALUATION	All masks made Send to M. V.	10 runs out
Mar. 1	Test Spec	—	Test Spec	

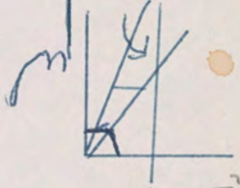
11/19

1. Define Objective
2. Breadboard contender
3. Evaluate Contender

12/1

4. Start layout of Contender Max. 2 types, 1 prime $2\,G_2 + (R)$, alternate $2G_2$ only.
5. Masks complete - 12-21 for G-R. Masks complete- R Jan. 1

	A	
o/o Distr.	100	β^2 Requires device
Noise Immunity over temp. range	200	30<B<200



$$F.M. \propto a^{-1} A^{-1} V^{-1/2} \cdot \frac{h_{fe}\,max - h_{fe}\,min}{h_{fe}\,min} \cdot \left[\frac{R_c\,max - R_c\,min}{R_c\,min}\right]^2$$

August 21, 1962

DRIFT STUDIES OF SURFACE POTENTIAL CONTROLLED F.E.T.

Otto Leistiko

I. OBJECT

A. To make a stable surface potential controlled field effect transistor.

B. To understand the mechanism that causes the change in channel current, under set conditions, with time.

II. For the experiments, the viewpoint will be adopted that the cause of drift is intimately connected with the dielectric between the surface gate and channel, and that the dielectric is SiO_2. The regions of the dielectric to be investigated in detail are:

C. Surface of the dielectric

B. Bulk of the dielectric

A. The interface of the dielectric and channel region.

III. Since there are a great many factors which affect the structure of the dielectric and its immediate surroundings, we will consider each region separately. The following is a list of processes and effects which can be associated with each region, more or less.

- A. The interface of the dielectric and channel.
  - 1. The dopants used in the starting material
    - a. Al-P, Al-Sb, Al-As, Ga-P, Ga-Sb, Ga-As or others, epitaxial
  - 2. Surface preparation before first oxidation
    - a. Special cleaning, Formic - H_2O_2
    - b. Short oxidation - strip off then oxidize again
  - 3. Agglomeration of fast diffusing in purities
    - a. Gold
    - b. Nickel
  - 4. Oxide growth
    - a. Dry O_2
    - b. Steam O_2
  - 5. Regrown oxide
- B. Bulk of the dielectric
  - 1. Oxide growth
    - a. Dry O_2
    - b. Steam O_2
    - c. Temperature
  - 2. Regrown oxide

3. Impurities in the oxide resulting from starting material and process
    a. Al
    b. Ga
    c. B
    d. P
    e. OH

C. Surface of the dielectric
1. Cleanliness
    a. Special cleanliness throughout process
    b. Special cleaning before last very high temperature step
    c. Special cleaning before last high temperature step
2. Impurities resulting from process
    a. Al (metalizing)
    b. B
    c. P

IV. The experimental procedure for making the device will be that of having a standard process then making variations to either lessen or accentuate the drift characteristics.

A. Standard Process
1. Resistivity
2. Cleaning wafers, (TCE, acetone, H_2O igepal)
3. Chemical polish (CP-6)
4. Special cleaning prior to oxidation (Formic acid - H_2O_2)
5. Outdiffusion (T=1250, dry O_2)
6. 1st mask
7. Clean wafers
8. Isolation predep (T=1200, Boron)
9. 2:1 HF dip
10. Isolation diffusion (dry O_2)
11. 2nd mask
12. Clean wafers
13. Contact predep (T=805 Phosphorous)
14. Clean wafers
15. Ni plate and Getter (T=1100, dry Ar, O_2)
16. 3rd mask or contact oxide remove (quench control)
17. Clean wafers, 2:1 HF just prior to
18. Metal evaporation (Aluminum, double 60 mg, on glass slides, outgas)
19. 4th mask
20. Clean wafers

21. Metal alloy (T=580°, dry N_2)

22. Back lap

23. Dice

24. Mount, bond, lead weld (Au-Si, 1 mil Al-Si wire, thermo compression)

25. Bak out (dry N_2)

26. Can (dry N_2)

B. Run 1. Purpose - Effect of ultra clean techniques, introduction of as little OH ions as possible.

1. Use standard process

Run 2. Purpose - Effect of oxide grown with steam

1. Standard process - substitute steam 0_2 for dry 0_2 at steps 5, 10

Run 3. Purpose - Effect of Phosphorous

1. Omit contact predept, steps 12, 13, 14

Run 4. Purpose: Agglomeration of Ni at interface?

1. Step 15. Ni plate, getter and quench from 1100°C
2. Step 15. No nickel, slow pull in dry As, 0_2

Run 5. Purpose: Effect of gold

1. Diffuse in Au prior to beginning standard process
2. Diffuse in Au instead of Ni getter step 15

Run 6. Purpose: Effect of regrown, supposedly uncontaminated, oxide and variation of oxide thickness

1. Remove oxide and regrow prior to step 15. Ni plate and getter.

V. EVALUATION

A. Select 20 good dice with scope

1. Measure BV_{GS}, I_{DO}, oxide gate unshorted three pt. probe.

B. Mount the 20 selected dice

1. Measure BV_{GS}, I_{DO}, V_{PJ}, V_{PO}, I_{GS} at 10 volts

C. Bake out and can as in IV, A, 25-26

1. Measure BV_{GS}, I_{DO}, V_{PJ}, V_{PO}, I_{GS} at 10 volts, C (of oxide gate) at 0 volts
2. Select four typical units and plot on x-y recorder I_{SD} vs V_{SD} V_G is the parameter

D. Preliminary age the four selected units for approximately 16 hours (overnight)

1. Conditions: V_{SD} = const, V_G = const, T = const
2. Plot I_{SD} vs time
3. Store with all leads shorted

E. Select one device from the four. After having accumulated four devices (representing four different runs), plot the following:

1. I_{SD} vs time at T = -50°C, + 50°C, + 100°C

   V_{SD} = const, V_G = const

2. I_{SD} vs time at different fields

   V_{SD} = const, T = const

VI. Schedule of time for device fabrication and evaluation

	RUN	1	2	3	4A	4B	5A	5B	6A	6B
A. Fabrication IV - A, B	Start Finish	8-21 9-5	8-21 9-5	8-22 9-6	8-22 9-5	8-22 9-5	8-23 9-12	8-23 9-12	8-27 9-13	8-27 9-13
B. Selection of devices V - A, B, C, D	Start Finish	9-6 9-10	9-7 9-11	9-10 9-12	9-11 9-13	9-12 9-17	9-13 9-18	9-14 9-19	9-17 9-20	9-18 9-21
C. Age V - E	Start Finish	9-17 10-4	9-17 10-4	9-17 10-4	9-17 10-4	10-5 10-24	10-5 10-24	10-5 10-24	10-5 10-24	10-25 11-1

* Assumes only one Varian recorder for data taking

Meeting re $Si-SiO_2$ interface

~~Stark~~ Leistiko
Tremere
Salt

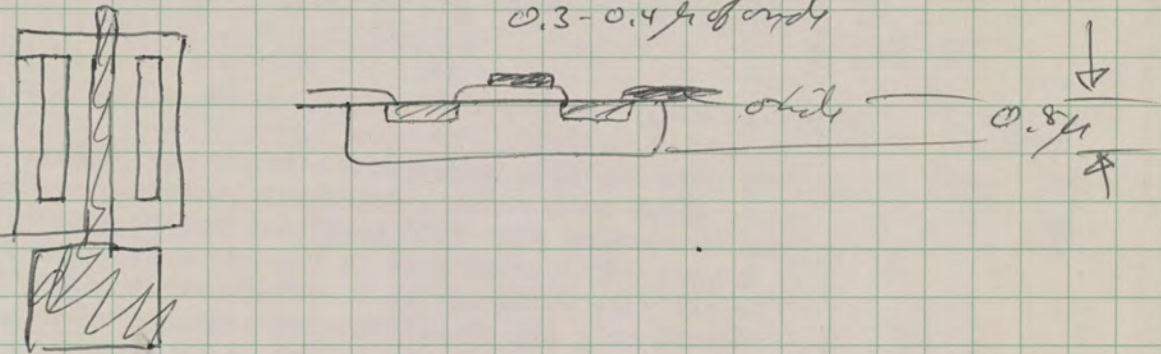
Otto has info that a similar structure with the regular V-1 diffusion that did not change @ 150°C and voltage.

These differed by having a separate oxide cut rather than a dip.
The split run will be tried.

A series of 6 runs were set up:

Structure:

Scale
1/4" = 1 mil

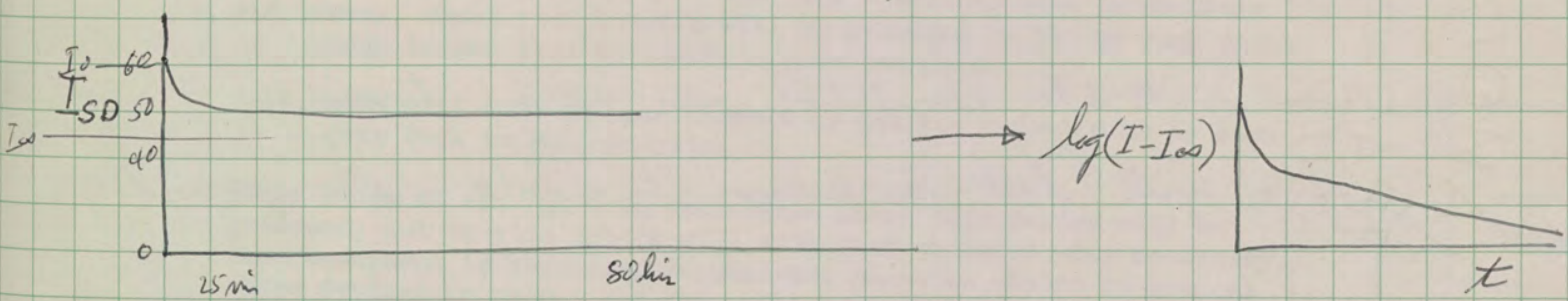


Std: dry O_2 for ~~oxidation~~ out diffusion, isolation, gettering

Six experimental runs made
Evaluated
Some aging done:

Std one after canning

~~10~~ 10v V_{SD}, both gates grounded to stabilize.
Then put −4 v on oxide gate. Junction gate grounded.



This usually fits c̄ $I_0 - I_\infty = Ae^{-t/\tau_1} + Be^{-t/\tau_2}$

On one device studied in detail, $\tau_2 \propto e^{.222/kT}$

The magnitude of $I_0 - I_\infty$ is strongly temp dependent —

6 11/20/62 – Review of ~~Ni~~ Nichrome Resistors, especially the data of Talbert.

Talbert, Perkins, Waite, Waring, Farnsworth, Ferguson, Grinich, Moore, Farina

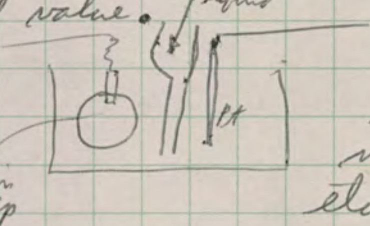
Dave Talbert: Review of his data

80 runs of 4 wafers each – aim @ 150 Ω/□ most of time
180 Ω/□ part of the time

~~(1)~~ The process:
W - filament c̄ nichrome wire clips
evaporate in < 1 min. Start @ ~5×10^{-6} mm.

Wafers baked prior to loading @ 200°C in air
No other in-situ treatment.
Monitor was 1/4 × 1/4" area on a similar substrate strip.
~60 runs used Al contacts, but got variability
later tried Au and Au + Al c̄ no apparent improvement.
Monitor can be stopped at the desired value.

KMER masked and etched (electro)



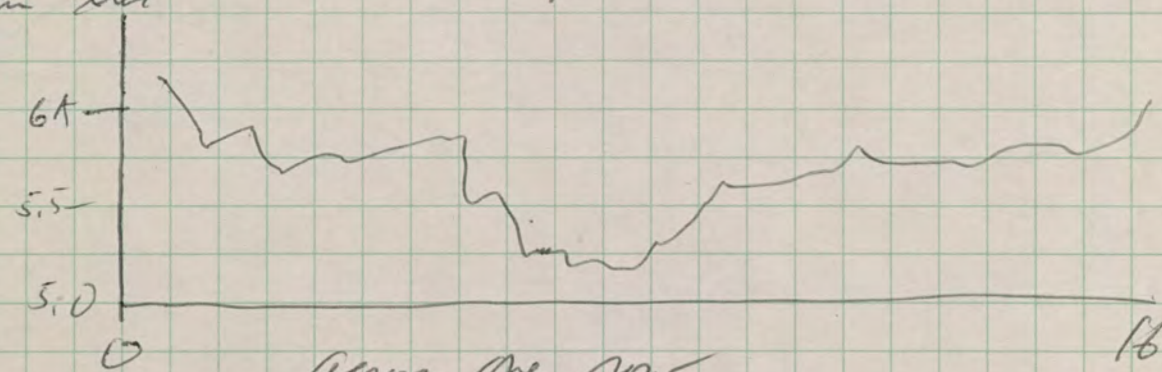
The liquid is poured in slowly and the metal etches at the interface.

Wafers then get Al evap (full thickness) all over followed by std metal etch (NaOH).
KMER removed by hot ethanolamine (MEA). This is an undesirable side reaction that caused trouble. It attacks both Al & Nichrome – New technique ~~eliminates~~ eliminate the problem. – This appears to be

Heat-treated for 5 min at 580°C. (Std. Al-alloy)

Resistance increases ~ **4-5%** consistently upon exposure to air.

Across a wafer, with best procedures to date, the spread looks like



Dip in center is typical, but not always. Spread 53 – 62 in one wafer.

R. GRAHAM November 14, 1962

M. H. Phelps

IBM Card Reader Phototransistor (XFT-3)

T. Bay
C. Sporck
J. Smith
E. Biegel

This is to advise the status of the above subject as of 11/14/62.

Jack Smith, Elmer Biegel, and I had a meeting on this day with the intent to finalize our position, formulate a sales plan which we could follow and propose to IBM and--generally--get some decisions made by both companies before the end of this month. The intent was to get Harold Rudder in Poughkeepsie on the phone with all of us, after checking several points internally, to get a commitment from IBM which could enable us to make some plans.

Previous to the call we decided prices, answers to their questions regarding specs, the position we would take regarding delivery rate, and what test results we could show them in a few weeks. Unfortunately, Harold Rudder went home ill that day and we were unable to get the decision. Hence the reason for this memo to you requesting follow-up in my absence.

Charlie Sporck verified that we could build up to a production rate of 1,000 per week with 90 day lead time and that 250 on the first order should be no problem, because R & D has many wafers going through right now. Charlie got this from Phil Ferguson.

Elmer Biegel has the specifications we can agree to over and above those which were initially provided IBM (maximum temperature permissible, maximum dissipation, etc.). Approximately 50 devices are presently being placed back on life test (were observed after two or three days) to observe the long term stability with temperature and power. These test results will be promised to IBM by Jack Smith as a wedge to get them to commit a purchase order.

Jack Smith will take it upon himself to get the order to us as soon as he goes back to Poughkeepsie.

As of today it has not been determined where this device will be produced, but Charlie Sporck will make that decision when necessary. Some equipment is necessary in whatever plant is chosen to produce these devices in volume and this will have to be decided.

It is our intention to get an order for at least 100 pieces (hopefully 200 to 250 pieces) out of them for the initial purchase. It is Jack Smith's opinion that this is probably the largest volume semiconductor we can hope to sell IBM in the next year or two and represents the largest dollar potential. Jack bases his opinion on the fact that he lived through the Texas Instruments' fiasco on the 1N2175 with which

IBM was never satisfied, but continued to buy in spite of themselves. They need a good card reader desperately, and Jack is quite optimistic that ours will be the best thing they can buy--resulting in orders for hundreds of thousands.

It is doubtful that we will see orders for more than 100,000 during 1963 which would sell for about $2.00 each. Eventually these will have to get well under $1.00 in very large quantities, but we made the initial quote (see IBM file) high to maintain a negotiating level from which to bargain.

Regards,

M. H. Phelps

MHP:jg

cont.

All units were baked out and canned.
Au - ball bonded.

Aiming at ~~10K~~ 9K, run 5-10K except for a few spots
Range over 10 samples in ~ 2K Ω in one run.

The over all process capability with 1 mil lines looks like ± 30%

Line-width measurements look like abt ~~0.0014~~ 4% too wide.

Early results c̄ long evaporation looks like much higher resistance films.

Stability:

~~Rm~~ 200°C storage
300°C storage
Room temp op. life. (5 failures @ 500 mw @ 500 hrs; 2 @ 200 @ 200 (- Most who't immediately) 1/10

Power	T	t	# started	# surviving at t	became open
500	25	500	10	7	3 failed in 24
100	25	500	10	9	1 " " "
100	25	1000	10	8	1 failed @ 100, 1000
500	25	250	10	8	2 @ 24 hrs
100	25	250	10	10	0
500	25	250	10	10	0
100	25	250	10	10	0

All power failures look like mechanical problems in the film - scratches, bubbles, etc.

Some randomly selected units vs time look pretty good - run oriented

At ~~300~~ storage, the units drifted much more. At 200°C variations of the order of 1%. At 300°C they go up and down all over the map.

All opens found on storage (~10%) were for problems other than nichrome.

All power failures were in the nichrome.
No storage " " " " " ".

H.S.

 Nichrome, cont

Bob Waits

Heated substrate resulted in even greater changes during heat treatment.

He agrees roughly on storage drifts.

Pierre Lamond:

If alloy is @ 550°C, one can get a non-ohmic resistance. For example one 446Ω - 552Ω depending upon direction of current → 352Ω after vacuum bake out

At 580°, this is less of a problem after 2 min, but at 550°, which is compatible c̄ the rest of the S city, this is a problem - until bake out.

With the mask designed to check contacts, there is no contact resistance observable compared to 150Ω - after bakeout

Problems:

1. Power life failure mode - must be eliminated.
2. Drift
3. Lack of predictability of the R's from the monitor
4. Spread on wafer.

Dev. Dev. work:

H.R. needs the things for dif amp.

Dave Talbert plans:
1. Look for cause of flaws.
2. Much thicker films.

Bob Waits:
1. Substrate temp
2. Aging in a vacuum.

Dave Talbert will do a little more c̄ "thick" michrome evaporated slowly.

Epitaxial meeting, 11/20/62
(Reference, 11/6/62 - book II, p. 144-146)

Still - Bldg problem with $SiHCl_3$

1st runs of ϕ. c̄ pure silane are just starting.

Graphite - They are using the correct one

Hank has a single run showing that c̄ 50 mil mesas that there is a e-c short problem (15/40 vs 6/40 with ~~no~~ CP-8).

Surfaces:

We do ~20 wafers at a time in CP-6.

CP-8 would be 5 wafers at a time.

(Come back)

Evaluation of 1341 - We gave the 6 runs.

~~Maybe~~ The comparison was not too far off.

Our runs show much ~~less~~ greater spread around a ~~row~~ row, but an awful lot more row-to-row spread.

Rectification and surface rejects are way down.

Our stuff was ~ 80% of "room" within spec
they run ~20%.

White paper on epitaxial.

	Present R+D	Present Production		New reactor
Silane	Distilled $SiHCl_3$ >10Ω-cm n-type	Impure $SiHCl_3$ variable, high p		Pure $SiCl_4$
Hydrogen	Pd purified 2ppm H_2O	Electrolyzer ~50ppm H_2O		Pd purified
Surface prep.	CP-8	CP-6 + HAc		CP-6 + HAc
In situ treatment	Pure HCl etch	none		HCl + $SiCl_4$ etch
Silane feed	liquid, volume-monitored	liquid, rate monitored		H_2 saturation @ 0°C.
Doping	added to silane	Accepted in silane added if necessary		From PH_3 in H_2
Type operation	Needle valve control	Diaphragm valve control		Push-button control

JM

Items still to be checked out on new reactor:

a) Is the material at least as good on 1341, 1321, FD-6?

b) Can it make 7000 material?

c) What is the production spread on thickness and ρ?

d) How flexible is the machine to change ρ?

e) What is the effect of substrate doping?

f) Can quartz plates be added without problems?

Items where our present production systems and operations could be improved:

a) Switch to distilled $SiHCl_3$ from R+D still.

b) Re-install old still at Sterling road to supply $SiHCl_3$.

c) Include provision for vapor etch with straight HCl.

d) Change to volume-control or positive pump liquid feed.

e) Sort substrate wafers to narrower resistivity spreads.

f) Eliminate handling of wafers with metal tweezers

g) Pd purified hydrogen

EPITAXIAL PRODUCTION IMPROVEMENT MEETING -

Held: 11-6-62

Summary of Proposals:

1. Begin use of distilled trichlorosilane as soon as system can be fabricated and installed under direction of R&D.
2. Insure use of standard CCT graphite mandril.
3. Determine if present etch used by Materials gives pitting as compared to CP-8 etch.
4. Evaluate results of R&D 1341 runs using their distilled silane and wafers grouped in a resistivity range of .0062 - .0075 ohm cm.
5. Materials present results of 1341 yield from standard production.
6. Investigate correlation of IR versus metallurgical methods of evaluation epitaxial film.
7. Materials present vapor etching data.
8. Materials report on results of using tighter resistivity grouping of antimony substrates.
9. Miscellaneous improvements for production area:
   (a) insure flowmeter control values after flowmeters.
   (b) install coil stabilizers.
   (c) place extra envelopes over mandrils when etching.
   (d) use quartz flasks for distilled silane.

Vapor etching:

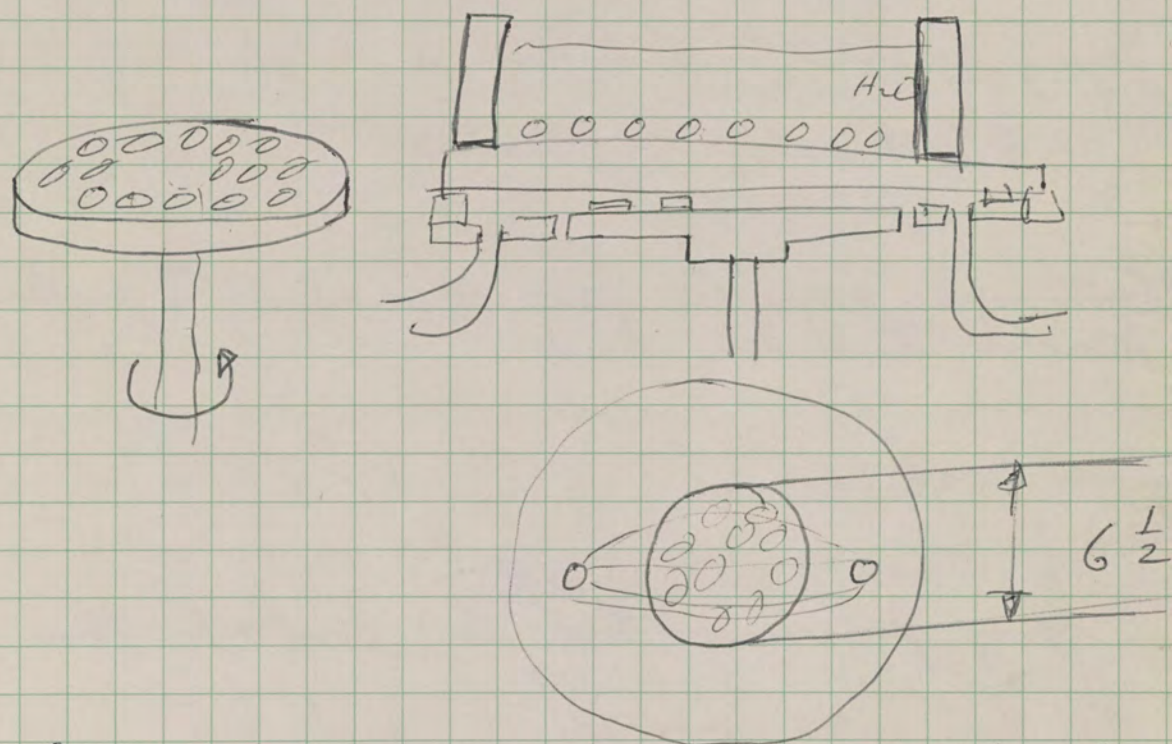
Schroeder tried to use $SiHCl_3$ + HCl. He was able to get some polishing action.

He also showed that some types of crud are removed, but that others are not.

HCl etch as a std should be considered.

We have ~~data on~~ evaluation on Cl_2, no Cl_2.

Schroeder on his new reactor.



Measured $SiCl_4$ consumption is way down. Est @ 3 l/month.

Capacity ≅ 135 wafers/hr.

At this rate, one reactor handles all the n-type.

Surfaces:

CP-6 - HAc

CP-8

Best mech - CeO, 1 stage, pit-free & scratches.

Metallization protection – Proj Rev. Mtng.

Shmid Burns
Waring Liddicke
Durnil Moore.
Perkins Ferguson

JPF: Status

M.D. S;O over entire wafer. 50 FF's on life test in un sealed TO-5's.

Process in coat S;O $\bar{c}$ Al
Etch pattern in Al
Use Al for mask against S;O etch 100 parts HNO_3, 35 parts HF
KPR – coat again over holes
etch off the Al

∴ This represents two additional masking steps and two evaporations.

50 gates @ 125°C – no problems yet

Trying to do the etch with a single AMER masking.

Etch with HF, NH_4F, HAc + H_2O + HNO_3 or H_2O_2

Units were evaporated thru a mask. No problems related to the monoxide have been found

Glass:

L.S. Spray pyroceram ~~thru~~ with an airbrush thru a metal mask.

Very thin – < 0.1 mils – v. hard.
devitrify @ ~450°C in N_2.

Problems:

1. flow-out of the glass onto pads + sintering

Schedule on evap. thru mask:

Decide today on masks to wafer glue with pyroceram.

Run here next week

Mtn View by week after next.

A possible real improvement to the existing spec is possible with epitaxy. Ie, this could even be done without changing the epitaxy point. This, however, is not making optimum use of the epitaxy.

On Next week: I_b vs Φ I_c confirmation due to prime S-element layout.

New Family   10 ns, 3 mw stuff

Objectives (in order of importance?)

1. < 10 ns
2. < 5 mw
3. > 200 mw worst case
4. $-55°C < T_A < 125°C$
5. F.O. = F.I. = 5

Design acceptance tolerances

β	25 – 200
R (2 mil)	± 20%
R (1 mil)	± 35%
R matching	± 5%
R temp tracking	± 2%

Mask tolerances

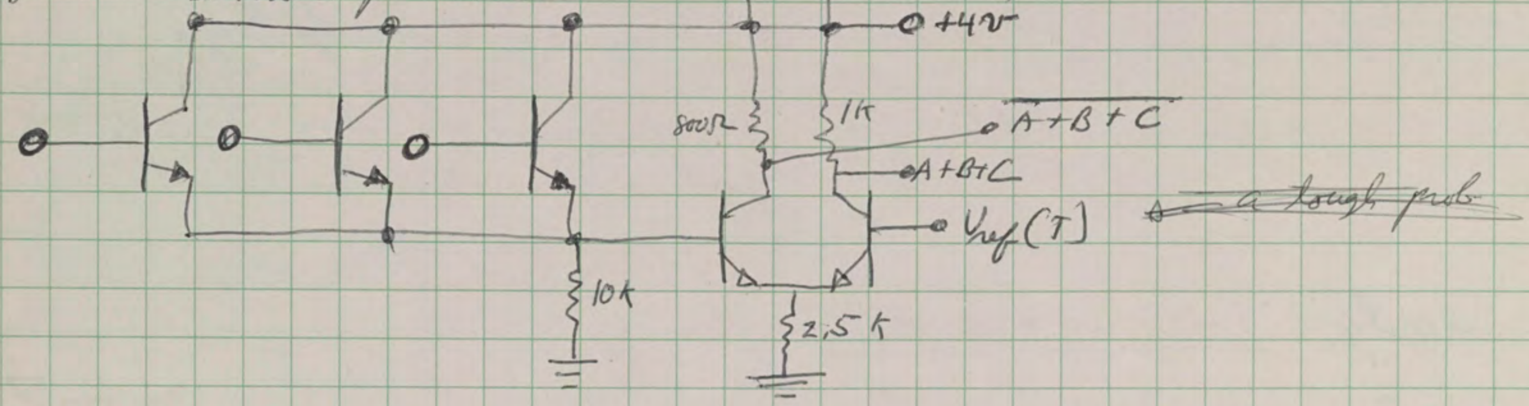
Metal stripe – 1 mil min
0.75 " " separation for l < 3 mil
1 " " clearance otherwise
0.5 oxide cuts for length > 2 mils
1.0 mil from isolation cut to active area
.25 mil cut precision.
full ¼ mil alignment tolerance

∴ Circuit possibilities

1. NON saturating NOR
" " NAND

 11/26/62, con't

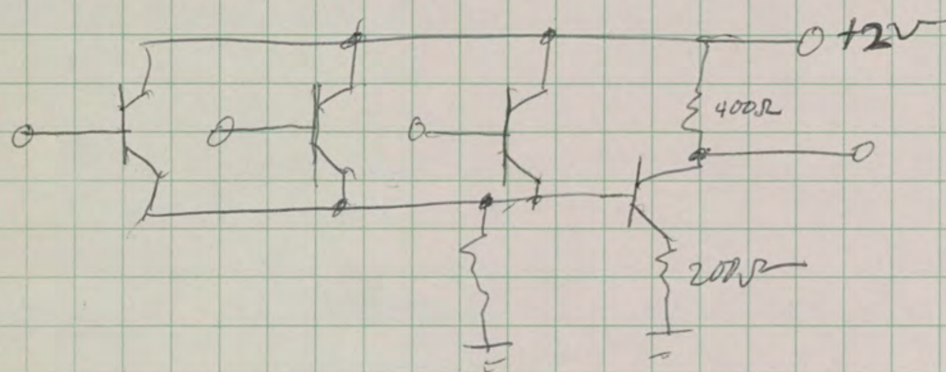
Seeds circuit possibilities: (Inverted MECL)



This does everything that MECL does, only at lower power.

This looks like @ ~5 mw one gets 10 n.s. best case, 40 n.s. worst case @ Temp T.

LOGIC	$\bar{t}_{pd}$	Pow	Problems	N.I.
LCEM (above)	10–40 20 n.s.	5 mw	V_{ref} – (a bitch!)	200 mv ?
FICL ~~MECKL~~	8–20 14 ns	3 mw	Vcc must track $\bar{c}$ temp amplifier noise	$\frac{200\text{ mv}}{9}$



11/26/62 Pressure Xducer Mtng
(ref: Vol II, 107 (9/12/62

Pearson
Plz
Kidell
Black
Shimil

10 units were presented c̄ data on them

These were all the PTA (large geometry) type.

Units look good except for 0-shift. This is an order of magnitude too high.

Sensitivity is repeatable 255 mv/10v

Linearity −0.38 % F.S. ± 0.09 % (range 9/10)

Hysteresis 9/10 had avg < 0.1 %

Thermal hysteresis 1st cycle ~ −0.3 to + 1.02 @ 250° (5 samples)
−0.11 to +.47 @ 250° (5 ")

3rd −0.06 +.56 from 250° units
−0.09 to +0.08 for 200° units

Zero shift ~ 0.05 % typical, but non-linear

The PTB gauge mask still needs some diddling to balance the bridges.
New masks using new technique will be made.

Problems:

1. High temp joint between Si diaphragm & block
   a) high temp epoxy — we will know in a couple of weeks.
   b) electron beam welding.
   c) glass has not worked well - an expansion coeff problem.

N.P. thinks that this is not serious. We will assume that if nothing untoward is discovered that the high temp epoxy ~~sits~~ works.

2. Need data on shake, rattle & roll
   a) Vibration, effect/g and is freq < 20 kc?
   b) Mechanical shock
   c) Thermal shock

3. Life test
   a) high T, high P 150 % of P at full T ~~xx~~ vs t
   b) environment
   c) Pressure cycling
   d) T cycling

Xducer, cont.

The PTB needs scheduling for a pilot run.

There is the possibility of a hot (wipe out Amelco) flush diaphragm.

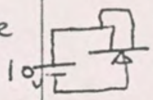
DATE 11-8 1962
EQUIP. USED
TAKEN BY G. Held
REQUESTED BY P. Lamond

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION
ENGINEERING DATA

( ) ~~FT~~ FET II CLASS
REMARKS Epitaxial N type Channel
GROUP XFE-62-10-1A

LOT No.	DE.	OP.	GR.	TYPE No.	CL.	TE.	COND.	DATE	ELAPSED TIME	SP.	SP.	

200°C storage



LOT No.	UNIT No.	0 I_{GO} na 0 hr	1 I_{GO} na 60 hr	2 I_{GO} na 100 hr	3	4	5	6	7	8	9
	1	0.22	0.02	0.01							
	2	1.30	1.10	1.10							
	4	3.30	2.40	3.0							
	5	1.30	1.30	1.10							
	6	0.66	0.60	0.60							
	8	2.00	1.80	1.60							

SFJ106A Rev.

DATE 11-27 1962
EQUIP. USED
TAKEN BY P. LAMOND
REQUESTED BY

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION
ENGINEERING DATA

FT. EFET-1 CLASS
REMARKS Epitaxial
GROUP EFET-1 A

LOT No.	DE.	OP.	GR.	TYPE No.	CL.	TE.	COND.	DATE	ELAPSED TIME	SP.	SP.

LOT No.	UNIT No.	0 I_{GO} pa @5V	1 V_{po} V	2 I_{SDO} μa	3 g_{mo} μΩ⁻¹	4 V_n mV	5 R_n MΩ	6 $BV_{G(SD)}$	7	8	9
	1	10	5.8	840	240	16	2.5	>50			
	2	10									
	3	10	6.0	800	230	15	2.3	>50			
	4	12	5.0	780	240	16	2.5	>50			
	5	9	5.8	800	265	14	2.0	>50			
	6	12	5.0	800	245	12	1.5				
	7	<10	5.2	620	235	12.5	1.65				
	8	<10	5.4	820	255	14	2.0				
	9	10	6.2	840	230	15	2.3				
	10	12	5.65	800	235	15	2.3				
	11										
	12										
	13	<10	6.4	830	230						
	14	<10	5.6	820	240						
	15	<10	5.2	790	250						
	16										
	17	<10	5.6	800	240						
	18	<10	5.7	810	235						
	19										
	20	<10	5.6	840	230						
	21	<10	5.7	850	240						
	22	<10	7.7	880	230						
	23	150	5.7	410	260	14					
	24	120	5.7	790	250	15					
	25										

DATE 11/26/ 19 62

EQUIP. USED

TAKEN BY B

REQUESTED BY

FAIRCHILD SEMICONDUCTOR

A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

ENGINEERING DATA

( ) FT. U-1 CLASS A

REMARKS

EPITAXIALS

GROUP

LOT No.	DE.	OP.	GR.	TYPE No.	CL.	TE.	COND.	DATE	ELAPSED TIME	SP.	SP.	

LOT No.	UNIT No.	0 I_{DS} $V_{DS}=10V$ $V_G=0$ mA	1 I_{GDS} $V_{DS}=10V$ uuA	2 BV_{GDS} $I_G=1\mu A$ VOLTS	3 V_{PO} $I_D=1mA$ $V_{DS}=10V$ VOLTS	4 gm $V_{DS}=10V$ $V_G=0$ 1KC umhos	5 * C_m $V_{DG}=10V$ f=1MC pf	6	7	8	9
	1	1.35	6	73	6.1	290	1.4				
	2	1.00	2	70	5.2	286	1.4				
	3	1.18	17	67	5.2	300	1.4				
	4	1.10	1	66	4.4	290	1.4				
	5	1.30	1	68	6.0	275	1.4				
	6	1.31	1	65	5.3	310	1.4				
	7	1.06	2	62	5.3	255	1.3				
	8	1.15	2	69	5.6	270	1.3				
	9	1.25	3	70	5.8	270	1.3				
	10	1.05	2	68	5.6	250	1.4				
	11	1.20	2	67	5.4	280	1.4				
	12	1.30	2	66	5.9	285	1.3				
	13	1.40	3	65	6.5	280	1.3				
	14	.245	4	66	2.5	195	1.4				
	15	1.50	1	64	6.2	300	1.4				
	16	1.20	1	64	5.2	305	1.3				
	17	OPEN	—	—	—	—	—				
	18	.490	1	68	3.7	220	1.2				
	19	1.80	1	65	7.9	290	1.4				
	20	1.70	2	80	7.5	290	1.3				
	21										
	22										
	23										
	24										
	25										

* TO-5 standard

FT. U-1 CLASS B

REMARKS

EPITAXIALS

FAIRCHILD SEMICONDUCTOR CORPORATION

ENGINEERING DATA

DATE 11-26 62.

TAKEN BY B. Worley.

EQUIP. USED

GROUP Appl. Eng.

REQUESTED BY B. Barranger.

LOT No.	DE.	OP.	GR.	TYPE No.	CL.	TE.	COND.	DATE	ELAPSED TIME	SP	SP

LOT No.	UNIT No.	0 C.T. BV_{GDS} $I_G = 1\mu A$ V	1 I_{GDS} $V_{DS}=10V$ $\mu\mu A$	2 gm $V_D = 10V$ f = 1KC	3 RN EN mV	4 I_{DS} $V_{DS}=5V$ mA	5	6	7	8	9
	1	65	6.8	299	2.9	1.4					
	2	65	5.4	300	4.0	1.4					
	3	65	3.8	299	2.8	1.5					
	4	64	4.0	298	5.4	1.2					
	5	64	84.	310	2.5	1.6					
	6	66	4.0	298	4.5	1.3					
	7	66	12.	300	3.8	1.3					
	8	65	7.6	298	2.9	1.4					
	9	65	19.	299	4.1	1.2					
	10	66	4.8	300	9.8	1.2					
	11	65	7.6	300	4.1	1.3					
	12	64	10.	300	4.1	1.3					
	13	64	4.6	300	4.7	1.3					
	14	65	66.	298	3.1	1.4					
	15	64	5.6	300	4.5	1.3					
	16	60	4.0	300	2.3	1.5					
	17	58	4.8	280	3.5	1.4					
	18	64	4.0	290	4.3	1.2					
	19	62	30.	310	4.1	1.4					
	20	63	4.4	310	5.6	1.3					
	21	64	3.8	310	3.1	1.4					
	22	62	3.0	300	4.4	1.3					
	23	63	3.6	300	2.5	1.5					
	24	62	4.4	300	2.4	1.5					
	25	63	4.6	290	3.7	1.2					

NOTES:

FET Mtng to review epitaxial 11/27/62

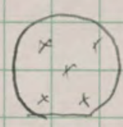
Yost, Leo Pyzler, Smith, Samuel, Ferguson, Rogel, Leibbi, Lynn, Rewz, Beringer, Cole, Bittman, Santos, Schiller

Status:

Material: asked for
$\rho \cong 1.5\ \Omega$-cm

$t \cong 3\mu$ (2.5 - 3.2) by groove + stain

Substrates $\cong$ 0.2 - 0.3 Ω-cm

V/I variation of 20% over a wafer 
50% around a row

Prime has only 4 runs - and one of these in only 2 rows.

~~Wafe~~ Wafers are sorted for V/I and process adjusted for the thic under the assumption that whole variation is thickness rather than doping.

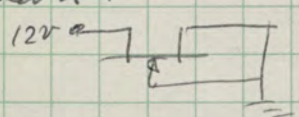
(minutes present) Status of runs (from done material)

FFET-1 - Test chip thru, rest at Die sort - all from one epitaxial run
11/30 2 - Test chip @ die sort — rest at gate diffusion
12/3 3 - " " " " —
12/4 4 - T.C. in back lap — } Test chips thru die sort by 11/30
12/5 5 - " " " " —
12/6 6 - " " " " —
12/7 7 - " " " " —
12/8 8 - " " " " —

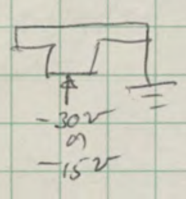
V/I sorted { 9 - 2nd mask
10 - 2nd mask
11 - 2nd mask }

These were dipped.
Other by Seastiko were U-2's, a similar process. ~~But~~
The U-1 units were all from one test chip.

Life test data:



stored at 200°C. After ___ hrs 3 units out of 20 had I60 go up from ~5 pa to ~100 pa. - But the oven burned out over the weekend.

Beringer did 

no failures in 60 hrs ~~as~~ 100% by outdiffusion in a few minutes.

Material:

Yield ~ 100 good wafers during the next week

New reactor, Sterling Rd. - 5 runs. ~5 wafers from each run to here, hold rest in bonded reserve. Try to do during next couple of weeks.

Make some on regular reactor in Mtn View.

Summary:

Hal + Leo to work at R&D to get runs out on schedule

Lou Reis gets ≅ 100 representative units ASAP to life test.

ROBE Meeting 11/27/62

Lang
Fagan
Hill
Blom
Fole

Robinson
Moss
McCall

Pinhole density: 4200 runs ~5/55 mil²
Small geometry is much less (~25)
μL runs ~50-60/55 mil² on regular stuff
some of their double spun stuff is ~20.

(Paul Hill is running some μL thru his area ~~c̄ the pinholes~~ c̄ std masking)

Chrome masks: Being held up on 4200 because of potential parameter distribution problems with scalloped edges.

Some 1250's made c̄ ~~std Masking~~ Std Masking had bad low current β. Examination of these showed no special correlation with masking resolution, but a whole bag of crudy problems.

Methyl Borate: R&D is using it on μ electronics yet.

Chrome mask status - Robinson

A separation of ~3 mils between chrome mask and wafer gives a very wavy fine edge.
Gene shows that some of this can be gotten with photographic masks.

However, it is true that there is more loss of resolution with the chrome mask than with the emulsion mask.

Suggest experiments
1. Get some optical jig results so that contact is good. Proc. Dev.
2. Try ~~lacquer~~ laquer coated Cr. mask.
3. Selected glass substrates
4.

It is suggested that this problem might be a multiple reflection problem. This sounds good.

ROBE, cont.

Paul is laying out experiments to look at last ~~week~~ time's pipe problems.

A wafer after predep, before diffusion was cut in half. Diodes were checked before and after. (½ each

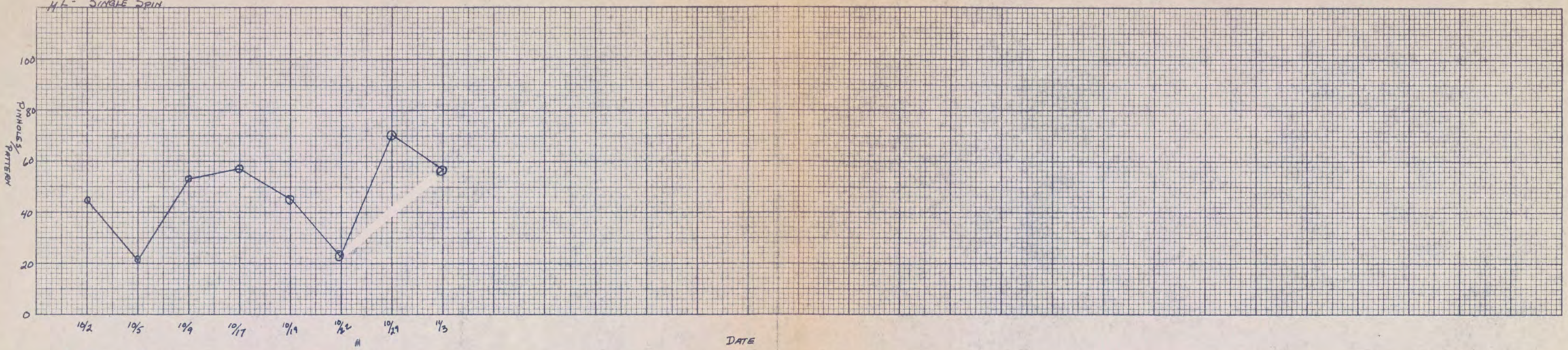
	before	after
Total checked	50	51
pipes	14	28
near BC	5	12
in base area	9	11

Thus Sang concludes that this is a significant source of pipes.

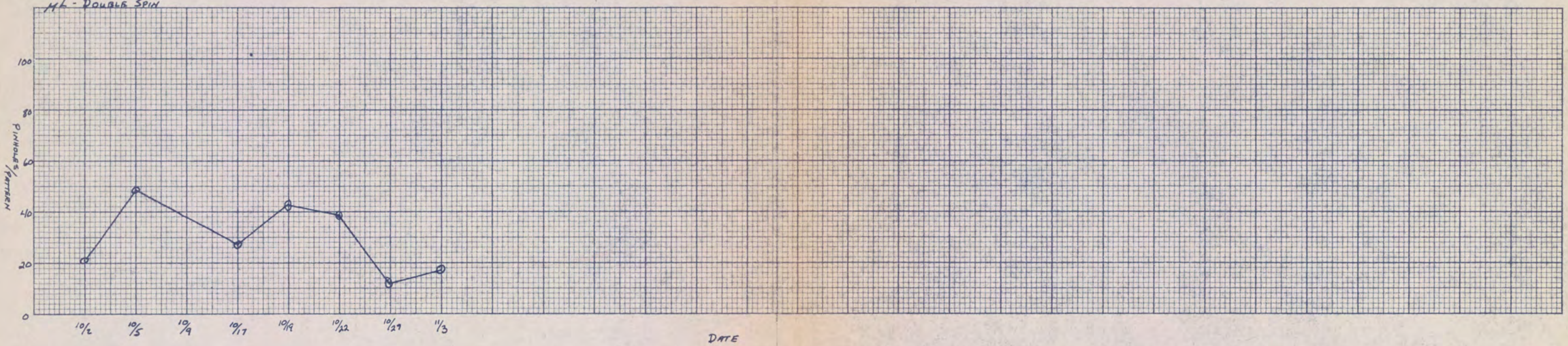
Next meeting on Monday afternoon — 2:00

PINHOLES PER .055" x .055" SQUARE

ML - SINGLE SPIN

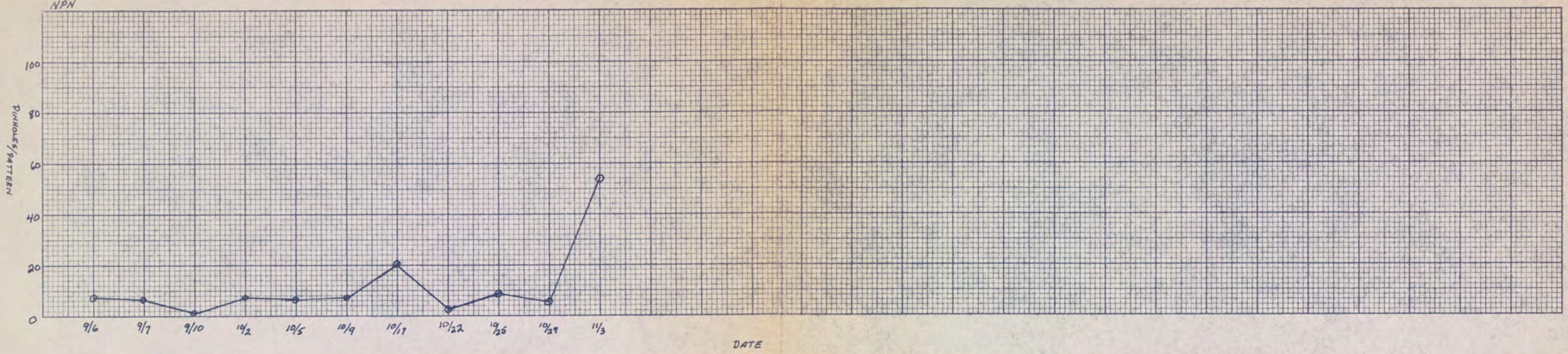


ML - DOUBLE SPIN

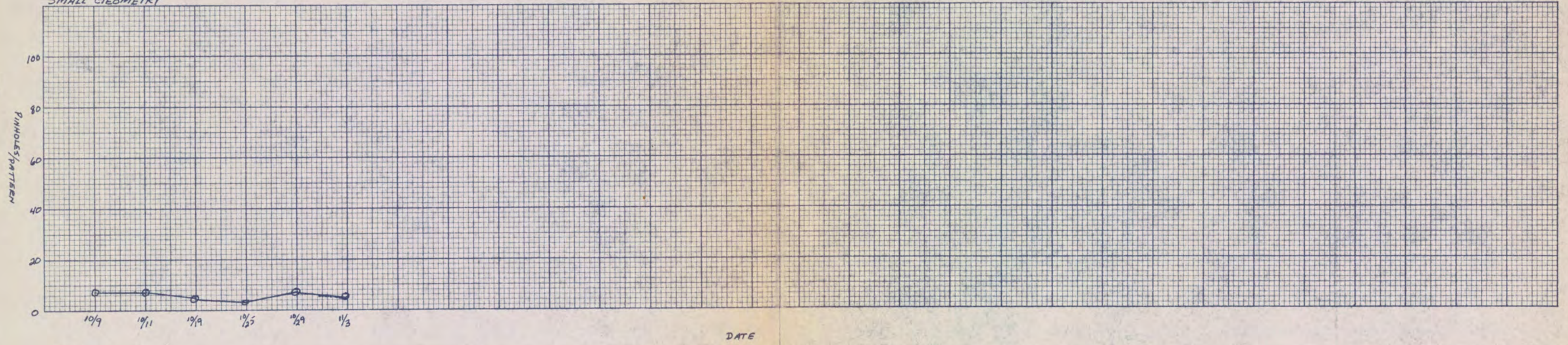


PINHOLES PER .055" x .055" SQUARE

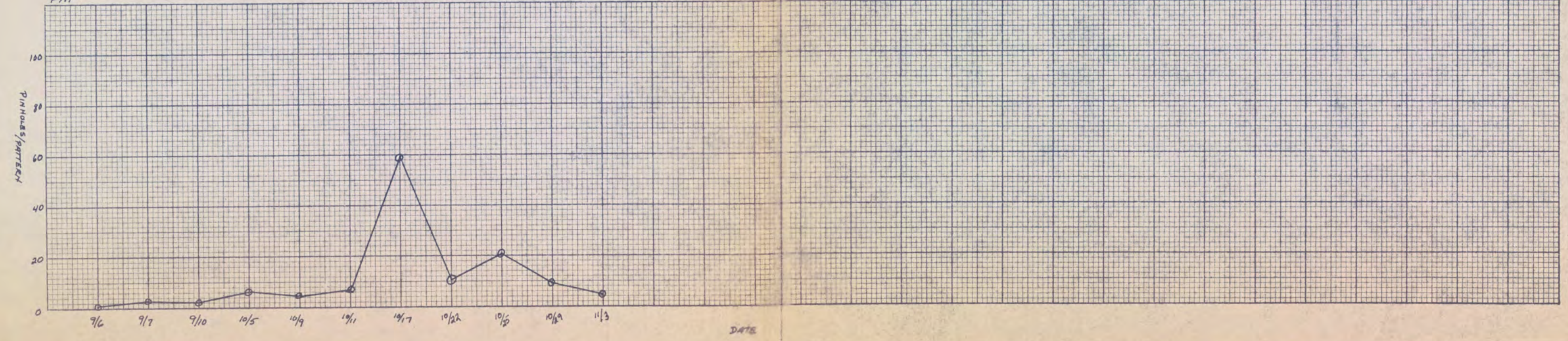
NPN



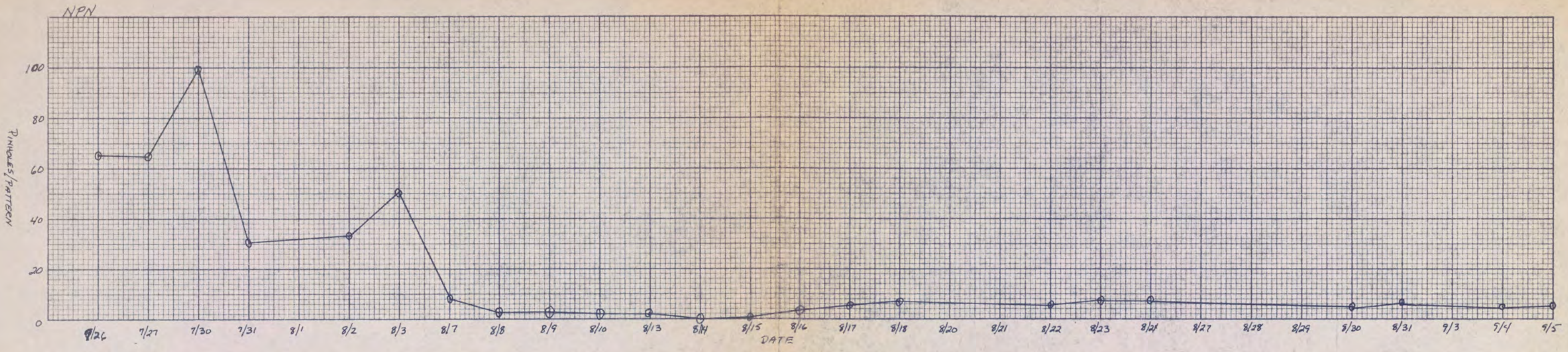
SMALL GEOMETRY

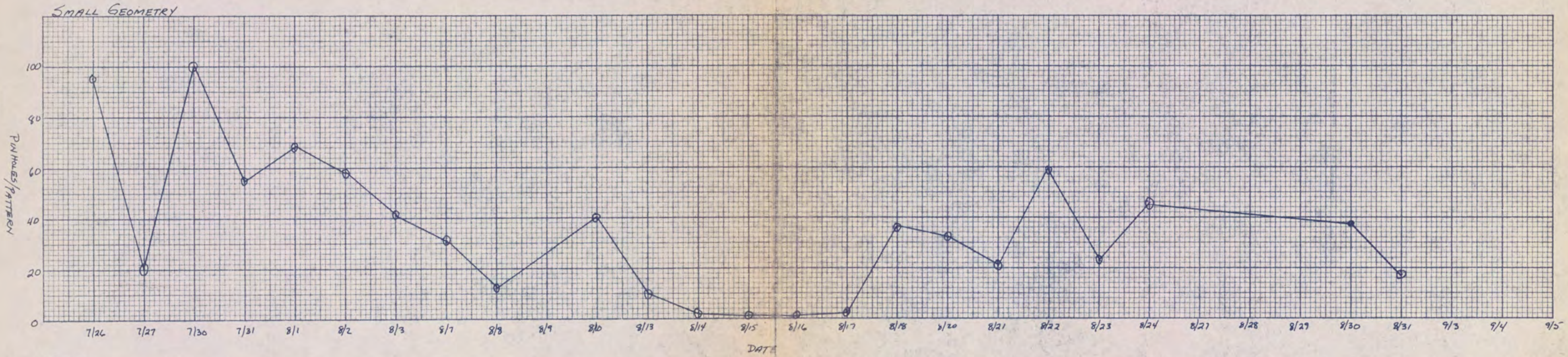


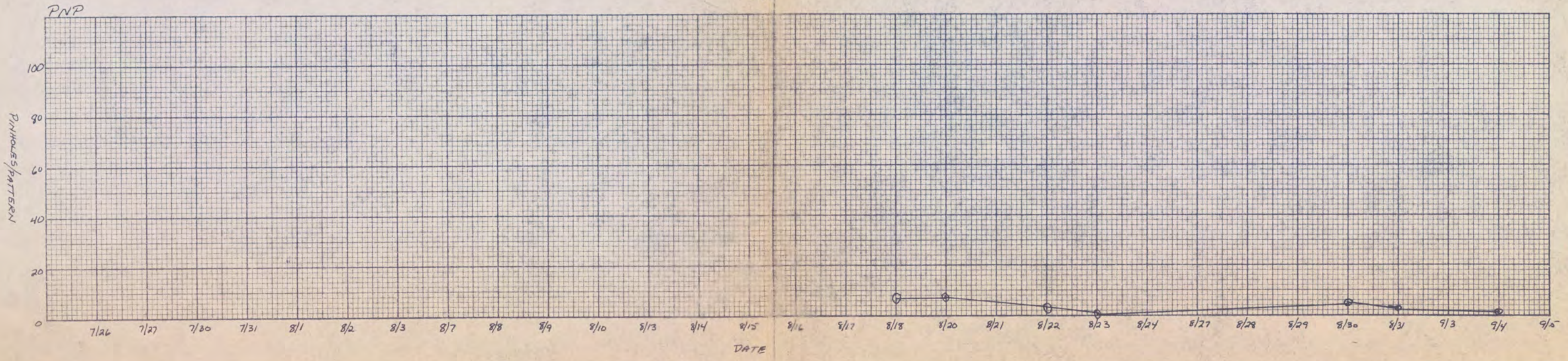
PNP



PINHOLES PER .055 INCH SQUARE PATTERN







Section Meeting: 11/28/62

Engwall
Van Ness
Fols
Blome

Chrome masks
~~Equip~~ Mask making
Test pattern
Engwall memo
Pinhole tester

Chrome masks:
Equipment: An etch jig plate holder

Need ~28 ea of 2 types - Run ~$2000 - Jigs getting estimate

Quantitative study of pin hole.
A **large** quantity of plates must be checked.

We will make a integrating counter of pinholes and continue to check on the individual

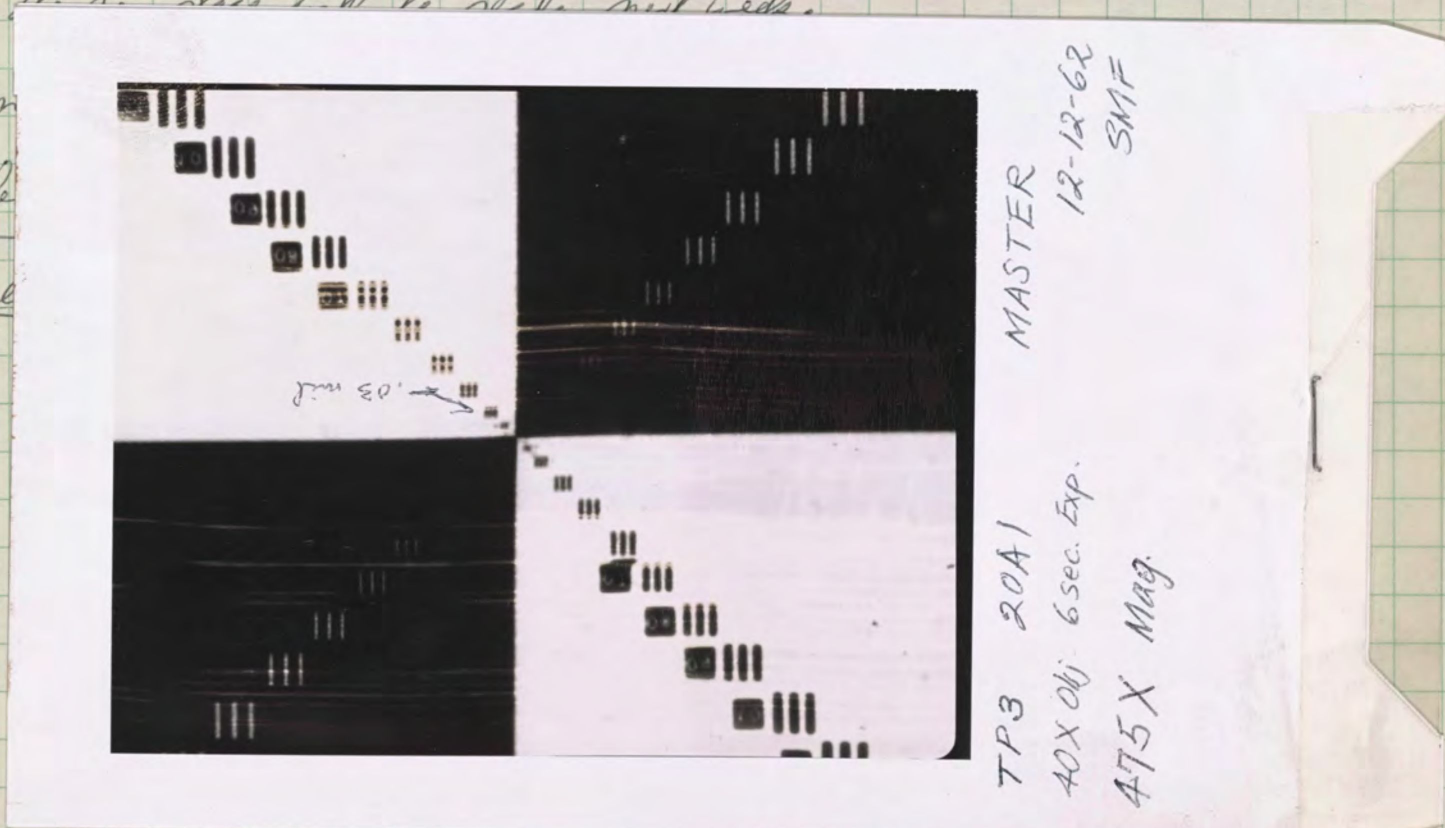
Chrome mask making is in pilot line room. There is room.

Mask making: Need stepping switch replacement.
Accuracy on machine is better going from 1→0 rather 0→1.
Can get a total speed of > factor of 2 less. It is also faster this way.
Can do 9/min rather than 5.5/min. This asymmetry is the result of faulty servo valves.
The [illegible] stage will be ready next week.

The m[illegible]

The de[illegible]

Engwal[illegible]



Section Meeting: 11/28/62

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We will make a integrating counter of pinholes and [illegible] to check on the individual

Chrome mask making is in pilot line room. There is room.

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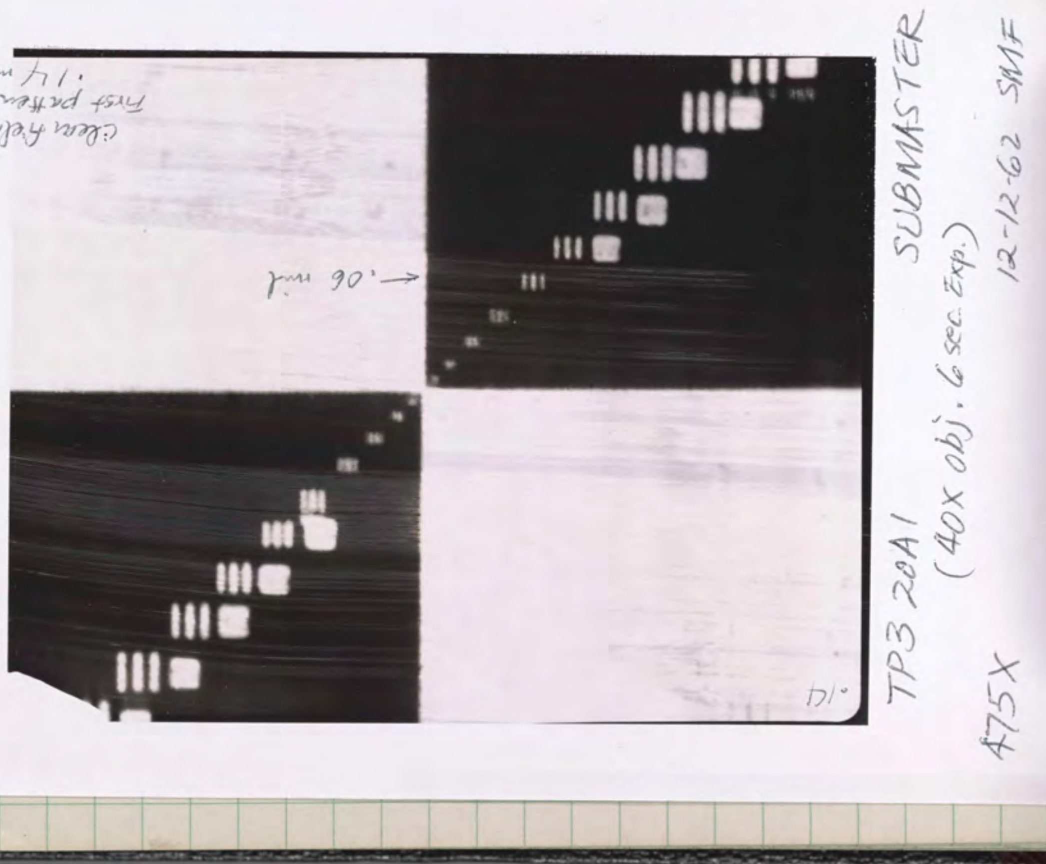
The [illegible] will be ready next week.

The m[illegible]

The de[illegible]

Engwal[illegible]



Section Meeting: 11/28/62

Engwall
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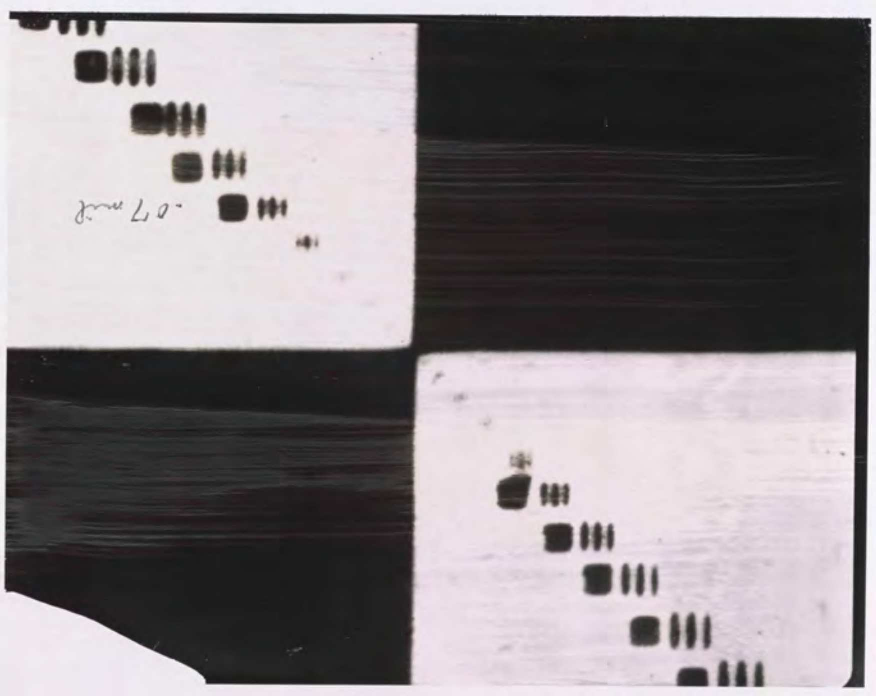
Chrome mask making is in pilot line room. There is room.

Mask making: Need stepping switch replacement.
Accuracy on machine is better going from 1→0 rather 0→1.
Can get a total speed of ≯ factor of 2 less. It is also faster this way.
Can do 9/min rather than 5.5/min. This asymmetry is the result of faulty servo valves.
These steps will be ready next week.

The m

The de

Engwal



TP3 20A1 Working Plate
40X obj. - 6sec. exp.)
12-12-62 SMF
475X

Section Meeting: 11/28/62

Engvall
Van Ness
Fols
Blome

Chrome masks
~~Equip~~ Mask making
Test pattern
Engvall memo
Pinhole tester

Chrome masks:
Equipment: An etch jig plate holder

Need ~ 28 ea of 2 types - Run ~ $2000 - Jigs getting estimate

Quantitative study of pin hole.
A large quantity of plates must be checked.

We will make a integrating counter of pinholes and continue to check on the individual

Chrome mask making is in pilot line room. There is room.

Mask making: Need stepping switch replacement.
Accuracy on machine is better going from 1→0 rather 0→1.
Can get a total speed of > factor of 2 down. It is also faster this way.
Can do 9/min rather than 5.5/min. This asymmetry is the result of faulty servo valves.
The new stage will be ready next week.

The manual S&R camera is out of wack. It must be re-auto-colli[mated]

The check to see if we can get rid of row & column in in mil.

Engvall on pinholes:

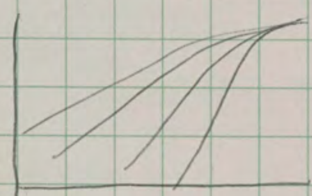
Wants to start here

Oct 28, 1962 — Epitaxial evaluation.

Wigton
Roder
Seh
Moore

Experiment to evaluate diffusion constant of substrate into film:

Take grown film + bed for various t's



If these follow a $\sqrt{Dt}$, then a D is good number

Film thickness:

We have several techniques

Texture lens [?]
Oxide
Stain
I.R.
Profile deviation from flat

The oxide masked wafer will do the job. It will be done.

Higher Ga conc.

Before Roder goes on vacation we want to answer the question:

Is the diffusion constant in the film higher than in the substrate on films grown at as low a T as possible?

at the regular growth temp?

1/29/62 Quickey pL mtg

Hoerni
Ferguson
Farina
Seeds
Cuppen

Seeds emitter follower:

One run thru. Rc distribution: mini 460
5 ohmits (600 nominal)
102 tile −510
90 −830
max 1200
} These were 1 mil resistors

β distribution 30 − 130

Questions? ~~Final~~ Chan yield on run? 25/31
Size of S element ? — Goes on 70 mil chip (vs 75 now)
Die yield — all passed

The oscillation problem theoretically exists, but no evidence of even any overshoot has appeared.

Essentially all the logic done c̄ pL can be done with these.

17 ns @ −55 °C
24 @ 125 °C

Advantages
Performance − ok — speed-power varies in: tougher
Size − ok
Yield − ok − big advantage

Disadvantages
Eat crow on DCTL and influence next family
~~Minor~~ Changes in logic!
a) Problem of coupling a C to an S − ~~unfortunate~~
b) Paralleling ~~a [illegible]~~ outputs
c) Minimizing C's again is different
d) People w/ paralleled gates are in trouble.
Added lead bond for G element. Possible need for two G's.

Comparison

	S chip size
DCTL, grid isolation	75
SSC, " "	70
DCTL, epi	~~60~~ 55
SSC, epi.	?, est 60

[redacted] A second run is in the mill. We don't know where, but it will not be thru in the next few days.

This does not provide a direct retrofit. If one were making a new family, it would entitle this.

Seeds recommends consideration of switching to epitaxial pL direct replacement. If good yield and 100 mv.

Farming on epitaxial DCTL.

Low power gates c̄ ~~extra~~ leads brought out

i.e. T I's, epitaxial. All high β devices

a) GY ~~gate~~ c̄ optimal resistors ± 20% R's over range $R_c = 750$, $R_f = 450$

get F/I, F/O 5, 3 c̄ 20 mv N.I @ 125

0 mv N.I @ −55

Est > 75% yield for A spec, w/ B's for β = 40 − 155

10 mw, 19 nsec t_p

~~Est~~

b) Stay at 575 Ω, grid isolation, take yield loss to 65% Don A.

c) Epitaxy c̄ T-I Xstor → 750 575Ω is best R_c (d)

Don was reporting upon was the apparent low temp advantage of this that looked like α_I. This is a fraction of the advantage, it turns out.

Possible paths

O —(test point)→ d

O —(~~op point~~ ~~test point~~ T.P.)→ b → d

O —(op. point ~~test point~~)→ a → c ~~→~~ d

O —(logic tests / test eq / est curr)→ e → e^2

O is present

a is non epi GY Xstor, 750 Ω R_c, $R_f = 450$

b " " " " , 575 , 350

c " epi T-I , 750 Ω ,

d " " " , 575 ,

~~Nov.~~ Dec 3, 1962 - Monday product meeting

Hennis, Schultz, Fegmann, Lannard, Moore, Farina

Review Z-transistor:

	B	V_{CE} @5,1	R_{CS}
GY			
Z			

Only 1 unit of the test vehicle had all four Xstors hooked up after assembly. On this one ~~Z~~ Z was better than GY on VCE

	VCE 5,1
Z_1	175
Z_2	190
GY_1	200
GY_2	225

Of 11 GY's, range was 170-230 mv
of 6 Z's, range 175-220 mv

The Z's, as expected had lower α inverse. These were non-epitaxial.

GY Xstor - GO-GO for std ckts.

New family:

The charter looks rough. The 10ns, 5 mv, 200 mv may be out of the question.

5 nsec, 10 mv } both look "feasible", but require different ckty.
25 nsec, 3 mv

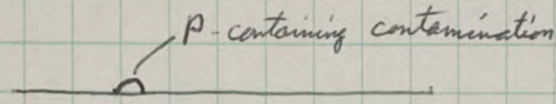
 ROBE 12/2/62

Sang
Hill
Fok
Flint
Moore

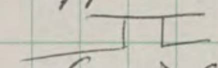
Shunich

P.F. — Rundown on his pipe work — up to base diffusion:

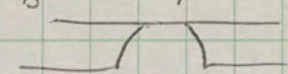
Goetzberger (@ Shockley) blames them on atmospheric contamination. He thinks they are a diffusion phenomenon.



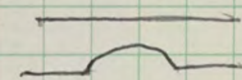
1. If into a B-diffused layer and starting at same time we get a cylindrical pipe. $C_{SP} > C_{SB}$, $\sqrt{Dt_P} = \sqrt{Dt_B}$



2. If $\sqrt{Dt_P} > \sqrt{Dt_B}$ $C_{SP} > C_S$, get an ellipsoid of revolution



3. If $\sqrt{Dt_P} > \sqrt{Dt_B}$, $C_{SP} < C_S$, get



Points, experimental are numbered

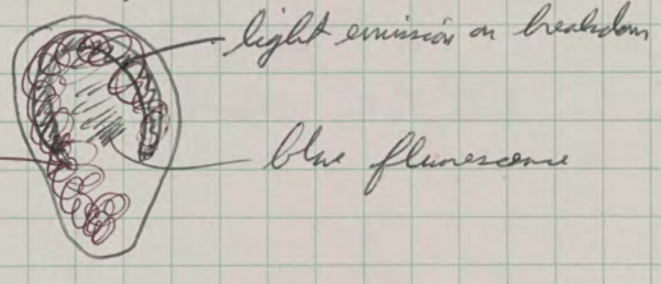
1. The incidence of pipes is a function of bulk doping. It gets larger with increasing bulk doping.
   This observation is based on many isolated runs, no split runs.
   Bob Sang points out that 4205 is worse than 4200, however.
   P.F. will either find data on a split run. Either old, or he will re-do.

2. In every case (~20 pipes) the electron probe has shown P. Some up to 1000 ppm.

3. The silicon concentration does not seem to drop more than a few percent at most. (Therefore one concludes that they do not represent a separate phase.) In some recent samples it looks more like 10%.

4. Many of the pipes show a pink fluorescence. V of C feels that this is almost certainly a glassy layer.

Typical



5. Approximately half of the pipes have shown heavy metals - Cu, Zn, Fe, Ni.

6. Discrete spots of metal exist over the surface of the wafer. Very patchy, but it does not necessarily associate with pipes.

7. In the metal Fe + Ni associate and Cu + Zn associate.

8. The metals are being found on etched wafers.

FAIRCHILD SEMICONDUCTOR

Inter-Office Correspondence

To: D. Yost
R. Fouquet
N. Walker
R. Robinson
S. Fok (R&D)

December 3, 1962

From: Paul Hill

Subject: Minutes - Chrome Masks 4200, November 23 Meeting on Resuming Chrome Mask Usage.

Subject of Meeting: Re-instating 4200 use of chrome masking in production.

1) Major objection to current usage:

a) Oxide cutout resolution is poorer than those obtained from emulsion masks (see exhibit I).

b) The effects of pattern resolution as in exhibit I may have significant parameter shifts as yet unknown.

c) A production classification yield loss is possible due to irregular oxide cut-out patterns.

d) Belief that irregular edges tended to increase KPR lifting during aluminum etching.

2) Approach the chrome mask implementation:

a) Run no more chrome masks until classification yields of chrome mask vs. emulsion mask units have been evaluated.

b) On the basis of Process Development work showing degree of irregular oxide cut-out patterns is a matter of degree to which mask image and wafer contact is made, run no more chrome masks until the contact problem is solved (mechanical masking). See exhibit II.

3) Required:

a) Pressure pad for wafer on mechanical alignment (N. Walker).

b) Classification results on 3000 wafers processed on 4200 line with chrome masks, (R. Fouquet).

c) Test on degree of scallop edges vs. parameter change or degradation (R. Robinson).

d) De-bug pressure pad mechanical masking device of item (a) and equip 4200 masking stations with the device.

4) On 4500 devices the same requirements are assumed to also apply.

Paul Hill

Paul Hill

PH:ch

KEY TO EXHIBITS

EXHIBIT I - Oxide Cut-Out Resolution at 500X

Fig. No.	Subject
61	4200 Base pattern using emulsion mask
62	4200 Base pattern using chromium mask
63	4200 Emitter pattern using emulsion mask
64	4200 Emitter pattern using chromium mask

EXHIBIT II - 1340, 4th Mask Pattern at 200X

Fig. No.	Subject
33	1340 Chromium Mask
34	Oxide etched wafer showing progressively
35	Poorer edge definition from the left (Fig. 34)
36	To the right (Fig. 36) edge of a warped wafer

FIG 33

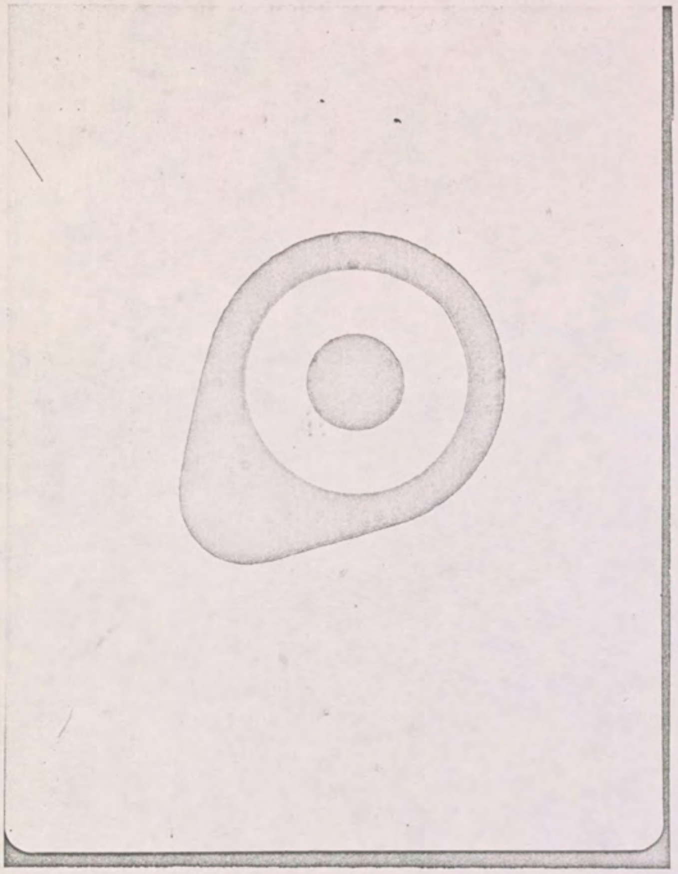


FIG 34

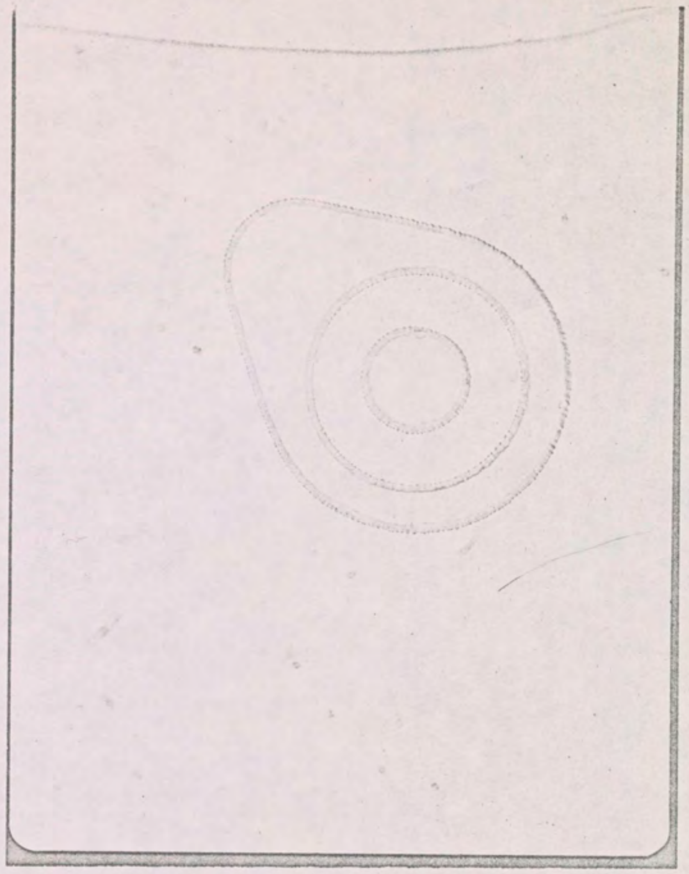


FIG 35

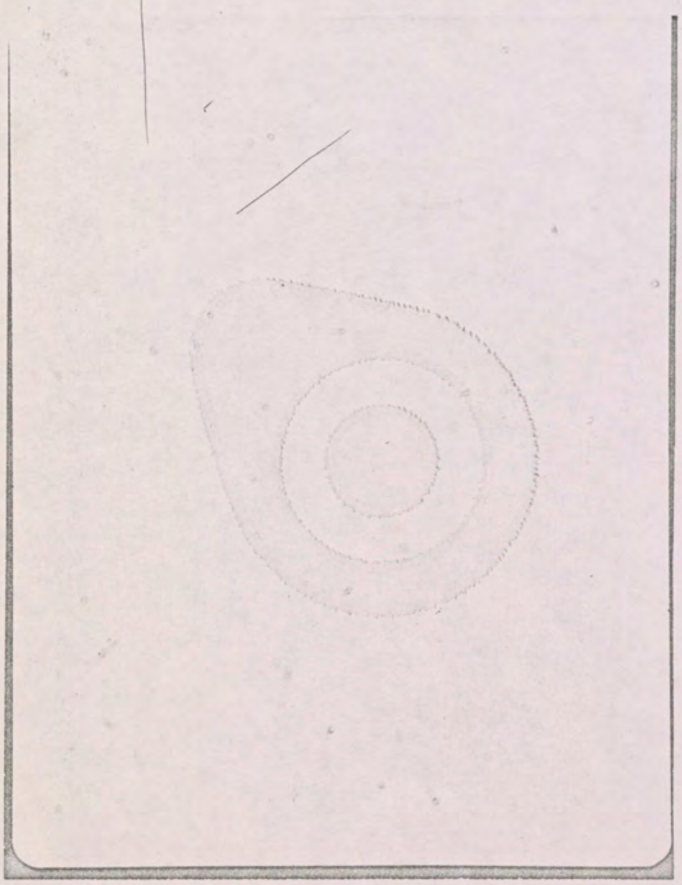


FIG 36

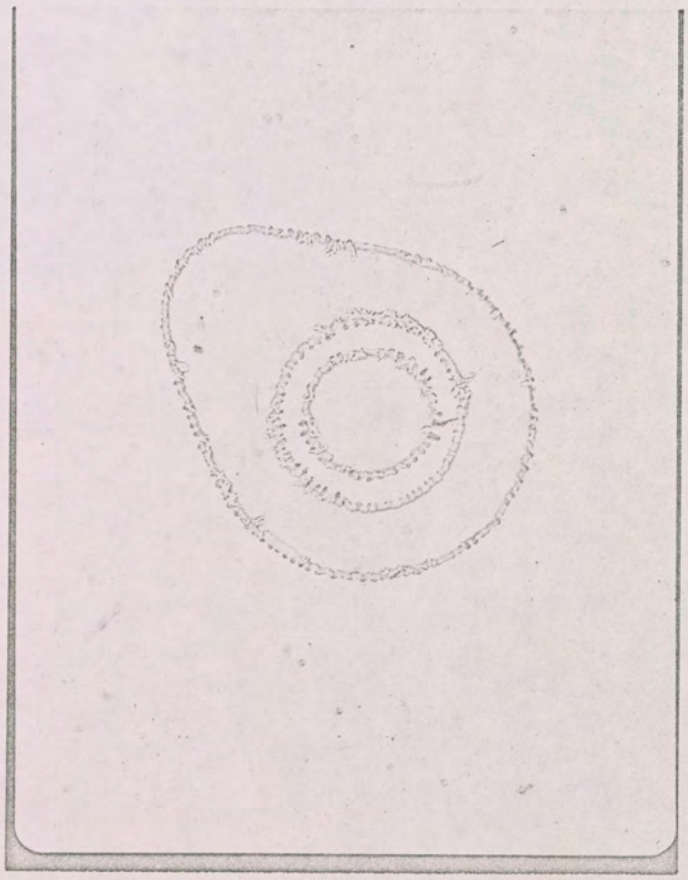


FIG 61

FIG 62

FIG 63

FIG 64

9. Edge dislocations do not correlate with pipes.

10. We can now develop the small, circular dislocation loops in <u>all</u> oxidized wafers (no others). None have been seen in un-oxidized wafers.

Phil thinks these are important in pipes.

11. Pipes were made by putting various salts on 1, 10^{-2}, 100 Ω-cm. Only the 10^{-2} Ω-cm got pipes. These were put on c atomizer. Correlation c spots was shown.

Program:
- Look at segregation at all stages for by electron probe.
- Look at loops vs Conc, depth, metal impurities.
- Surface contamination studies

12. Pipes usually have visual spots. Spots don't show pipes.

Sang program

1. Split between Flint pipes & process.
2. Proposed mechanism:
   Weak area on sloped region at oxide edge due to boron doping.

   Experiment: 1. segregate by visual observation sharp and sloped edges and compare density.
   2. Much heavier oxide to start c step edge.
   3. strip and re-grow

3. The Ni plating does it (an impurity?).
   1. Evaporated Ni
4. Pitting during base deposition
   1. Make badly pitted ones to compare.
5.

Meet again in 5 weeks + 1 day — Jan 8.

12/4/62

Thin film resistors for pckts

Sah — Noyce
Wajta — Campbell
Price — Moore

Resistors in 100 - 200 Ω/□
Candidates:
1. Nichrome
2. Cr-SiO ceremet
3. Rhenium (preliminary data not encouraging)
4. Ta - we know nothing at present

Nichrome:

(1) 300° substrates seem to cause problems.

(2) Most like variables. Structure — Process
a) Impurity content from ambient during evap. — Rate and ambient of evap.
b) Microstructure of film. — Substrate temp, rate of evaporation
c) Tungsten content — Analysis - not thought impt. - Tungs.
d) (Substrate contamination?)
e)

Cr-SiO - cermets:

We have used 2 sources and electron beam heating. R/□. 300-20,000 Ω/□
BUT - unpredictable
Etching in CP-6. or can be done with Al negative.
T.C. ~200-250 ppm @ 5KΩ/□.
Cold substrate evap. "Alloy" cycle change by 50%

The only possibility to (that I can see) to get this working is to get over to a monitored system.

Proposed program.

Get to a nichrome film whose V/I varies predictably to within 1%.

1. High substrate temp.
2. Controlled oxygen ambient during evap
   a) High substrate
   b) Low "

Check these out this week. After that we will get the rest checked out.

Heinz Rengg has done some 1/2 mil resistors c̄ HCl (dil) etch
10-90% $\frac{\Delta R}{R}$ 8-17%
10-90% $\frac{\Delta R}{R}$ 1.2-7%

(den Dean)

 Dec 4, 1962 — Epitaxial Meeting

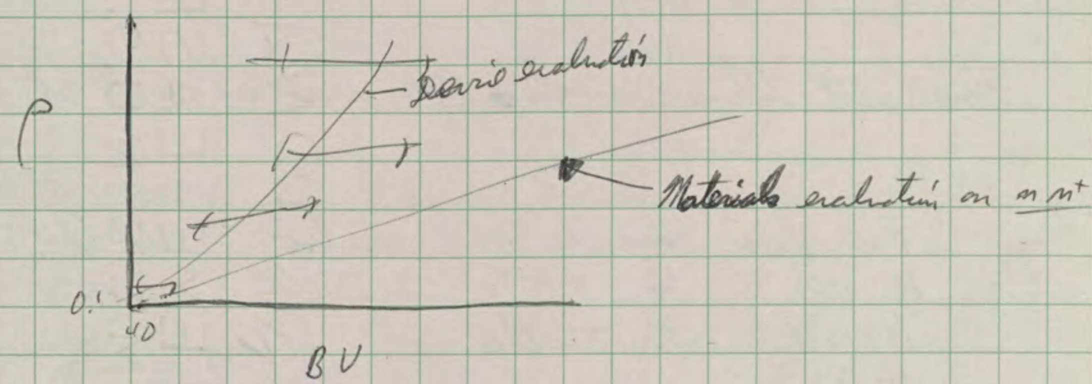
Cole
Schroeder
Gupta
Martin

Wrighton
Ferguson
Moore

New reactor evaluation:

First 1341 evaluation at die sort, seven runs, 3 thought to be within range – they were.

The evaluation c̄ an opposite conductivity wafer goes like



Summary: 1321–1311 being done
Want more 1341

From now on, they will run ~10% on the new reactor. Dick Cole feels that by the end of December a majority of the N–N+ material will be run on the new machine.

Schroeder says that 0.3 μ difference in 10 between where n n+ stain and n p.

1341 line might accept 100% next week.

It looks like we are evolving into this system rapidly. Change will be evolutionary.

Present System: running 50% out of 83% possible
58–59% on n-type
the 1713 material made the other tough

The P–P+ is a problem. Still a 30° spread of T.

My agenda for epitaxy.

Last time everything hinged on the new reactor evaluations and estimates of time necessary to switch of after decision to switch.

A. ∴ 1st discussion – Evaluation of new reactor systems

a) # of runs
b) type
c) results thru evaluation
d) " " devices

2nd discussion of further evaluation required.

3rd date for decision concerning switch

4th time scale for switch after positive decision.

B. Discussion of advisibility of making changes in the existing systems in view of A above.

1st present status
a) overall yield
b) targetability
c) spreads

2nd possible changes to consider
a) still installation — not necessary now
b) HCl vapor etch — being done
c) silane feed system —
d) new reactor flange system —
e) Better temp distribution —

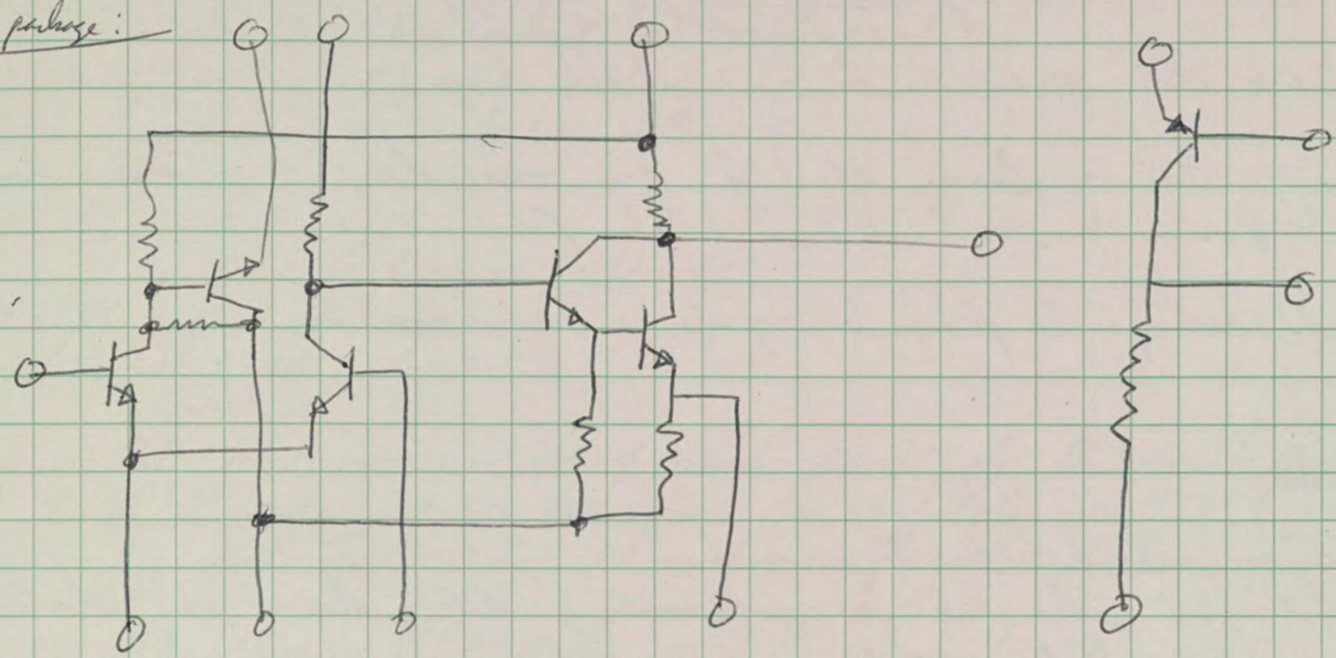
12/4/62

Litton revisited -VAX

Need ~100 pieces of 3 different circuits.

Package: flat

All in one package:



+ bad one

Conclusion:

If this is the hottest job of this general type likely to be around in the next 4-6 months, we should have the guy come up to talk to us.

Pete thinks will talk to Graham, etc, to see.

 Epitaxial project review - R&D. 12/5/62

Wrigley
Saly
Grinich
Ferguson

Hank on problems:

Surface preparation -

in situ HCl etching sometimes gives nonpyramids.

Our CP-8 etch seems to be as good as any.

1. The in situ etch is being studied vs variables. (Ernie is doing)
Ie, rate of removal vs $SiHCl_3$ and HCl flows.

A powerful technique to photograph defects is now available.

2. Evaluation

Thickness methods being compared.
Profiling: The technique is working. We have no data that is consistent.

Tie down substrate effects on profile of n-type films.

1. On ~~low~~ high ρ n or on high ρ p.
2. Sb doped substrates, Sb predep level all over, "small" spot,
0.006, 0.05
3. As " " 0.006, 0.05
4. P " " maybe?

Film resistivity. - No good ideas.

3. Systems:
a) O-ring c̄ three liquid feeds
b) horizontal reactor - no advantage at present

4. Equipment.

We want to end up with

1. D.D. with their own reactor

2. Facility for

a) Reactor & system development
b) Fuel studies
c) Special structures
d) Service

+ Other materials

Switch in time

Now

a) Move service out of present #2 RF to #3 with new reactor
b) Order W.G. reactor for installation in #3 (60 days est)
c) Get Talbert to clean up the #2 portion to his needs
d) " " " continue to run in #2
e) Have JPF order a RF generator
f) Get Wrighton people!

Out 30 days

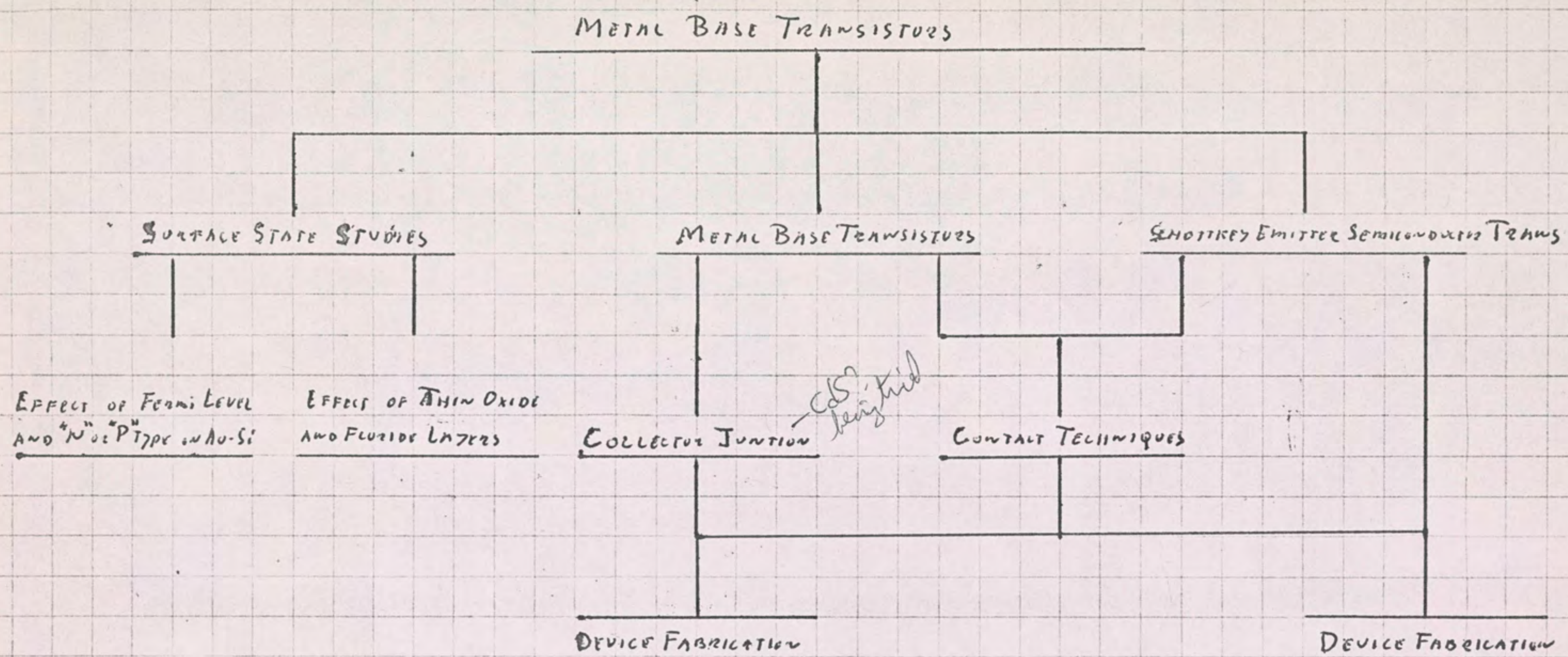
a) Consider ordering two more W.G. reactors, one for Dev. Dev., one for service, etc.

 Metal base amplifiers - Proj 177 12/5/62

Saxena
Bittmann
Sah
Grimil

Moore

Surface state study at metal - semiconductor surface shows very interesting results (after Atalla & Archer)



C Bittmann
A Saxena
12-5-62

PROJECT 177 - METAL BASE TRANSISTOR - A. N. Saxena & C. A. Bittmann

I. METAL-SEMICONDUCTOR BARRIER STUDIES

A single crystal of Si was cleaved in the vacuum system while Au was being evaporated. Thus an atomically clean Au-Si contact was achived. The thickness of the Au film evaporated was ~ 330 Å as monitored by the resistance monitor. Using a concentrated solution of black wax in T. C. E. in a syringe, small dots of black wax were put on the Au film without touching or scratching it. Au film outside the dots was etched away, thus obtaining islands of Au on Si. Capacitance as a function of bias was measured and diffusion voltage was determined. This is plotted in Fig. 1 (which is similar to Atalla's plot) if we use the ordinate $(\Phi_M - \Phi_{Si})$ on the right, and if we use the ordinate on the left, we get a plot of diffusion voltage versus the Fermi level in Si as suggested by Sah. The 45° straight line corresponds to zero charge in surface states, i.e., $Q_{ss} = 0$. For n-type Si without the oxide, we will have Au^- on surface and $Q_{ss} < 0$. Thus, the diffusion voltage V_o given by

$$V_o = \Phi_M - (X + V_F) + \frac{2\pi q N_D K \delta^2}{K_s^{\,2}} - \frac{4\pi \delta Q_{ss}}{K_s}$$

will be larger for Au-Si (cleaved-not oxidized) case than for Au-Si (oxidized) case. To verify this, the other half of the cleaved Si crystal was oxidized in room air for ~ 72 hours (left over the week-end). A Au film, again ~ 330 Å thick, was evaporated on the cleaved-oxidized Si surface and the above procedure repeated. The diffusion voltage obtained for this case is plotted in Fig. 1 which is found to be less than that obtained for the cleaved-not oxidized Si surface.

On p-type Si without oxide, we should have Au^+ on surface and $Q_{ss} > 0$. Thus the diffusion voltage V_o for Au-p Si (cleaved-not oxidized) case should be less than for Au-p Si (oxidized) case. A p-type Si crystal is being obtained in the proper shape to do this part of the experiment.

The above measurements were also done on photoresisted Si surface, which was previously oxidized. The diffusion voltage obtained is plotted in Fig. 1. Also plotted in Fig. 1 is the diffusion voltage for samples obtained by displacement plating of gold on "N" type silicon by the technique previously reported by Bittmann. Gold ions are added to the oxide etch in this process. The gold displaces Si atoms as the oxide is etched off the Si surface.

The Spectral photoresponse of the various units was determined with Rudy Dyck's help using his experimental setup. The general behavior of the Response per incident photon versus λ (in μ) curve is similar to that published by Crowell et. al. (Phys. Rev. 127, 2006 (1962)). Response measurements done by Crowell et. al. and by us are in arbitrary units and not absolute. A plot of square root of response per incident photon versus photon energy (in ev) would yield the threshold energy for the Au-Si barrier. Crowell et. al. find a value of 0.795 for the Au-Si (cleaved) case from a set of curves for different Au thicknesses whereas our value comes out to be about 1 ev as determined from data on one Au film thickness, i.e., 330 Å. Data for other Au film thicknesses will be obtained soon from which the mean free path for "hot" electrons in the Au film can be estimated.

The cleaving jig developed some trouble recently crushing rather than cleaving the Si crystals. It has been re-designed.

II. METAL BASE TRANSISTOR

A. Schottky Emitter

Schottky emission from Si-Au junction or In-CdS junction will be used for emitter. CdS has been obtained which will be evaporated on the metallized glass slides at first and diode characteristics will be studied. Tungsten boats are being coated with Al_2O_3 from which CdS will be evaporated (resistance heating). Electron beam evaporation will be done when the gun is installed in the system.

B. Collector

CdS will be used as a collector when Si-Au is used as an emitter and vice-versa for these initial studies.

C. Contact Problems

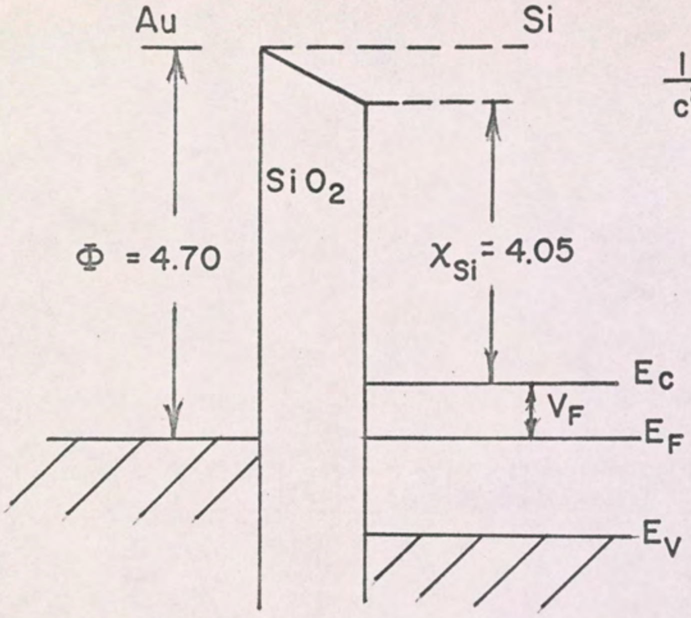
Since Au lifts off the SiO_2 surface, an annular ring of Al over SiO_2 will be used as a support for Au film and to prevent the lifting of the latter. This method gave an unexpected bump in the I-V plot of Au-Si surface barrier diode as observed sometime ago by us. This bump has not been investigated in detail yet. However, a modified etching procedure is being tried to see whether we still observe the bump or not. This involves oxidation of Si, evaporation of Al on SiO_2 layer and then etching holes through Al and SiO_2 layers simultaneously in one etching step. A run is in process.

III. SCHOTTKY EMITTER DIFFUSED BASE SILICON TRANSISTOR

This idea, first proposed by C. T. Sah, consists of diffusing a very shallow base on which a Schottky emitter is used. A run has been started with the help of Gary Parker in which Au-Si will be used as a Schottky emitter.

IV. ELLIPSOMETER

The table for the ellipsometer arrived minus a few parts. It is understood that, at the time of writing this report, the missing parts plus the right parts in place of wrong ones have arrived and the assembly of the table is under way. Messrs. Rudolph & Sons are supposed to call us any day now when they put the ellipsometer on the plane because we are supposed to go to the airport and pick it up.



$$\frac{1}{c^2}\text{ intercept} = V_0$$
$$= \Phi_M - \Phi_{Si}$$
$$= \Phi_M - (\chi + V_F) + \frac{2\pi q N_D K \delta^2}{{K_s}^2} - \frac{4\pi\delta Q_{ss}}{K_s}$$

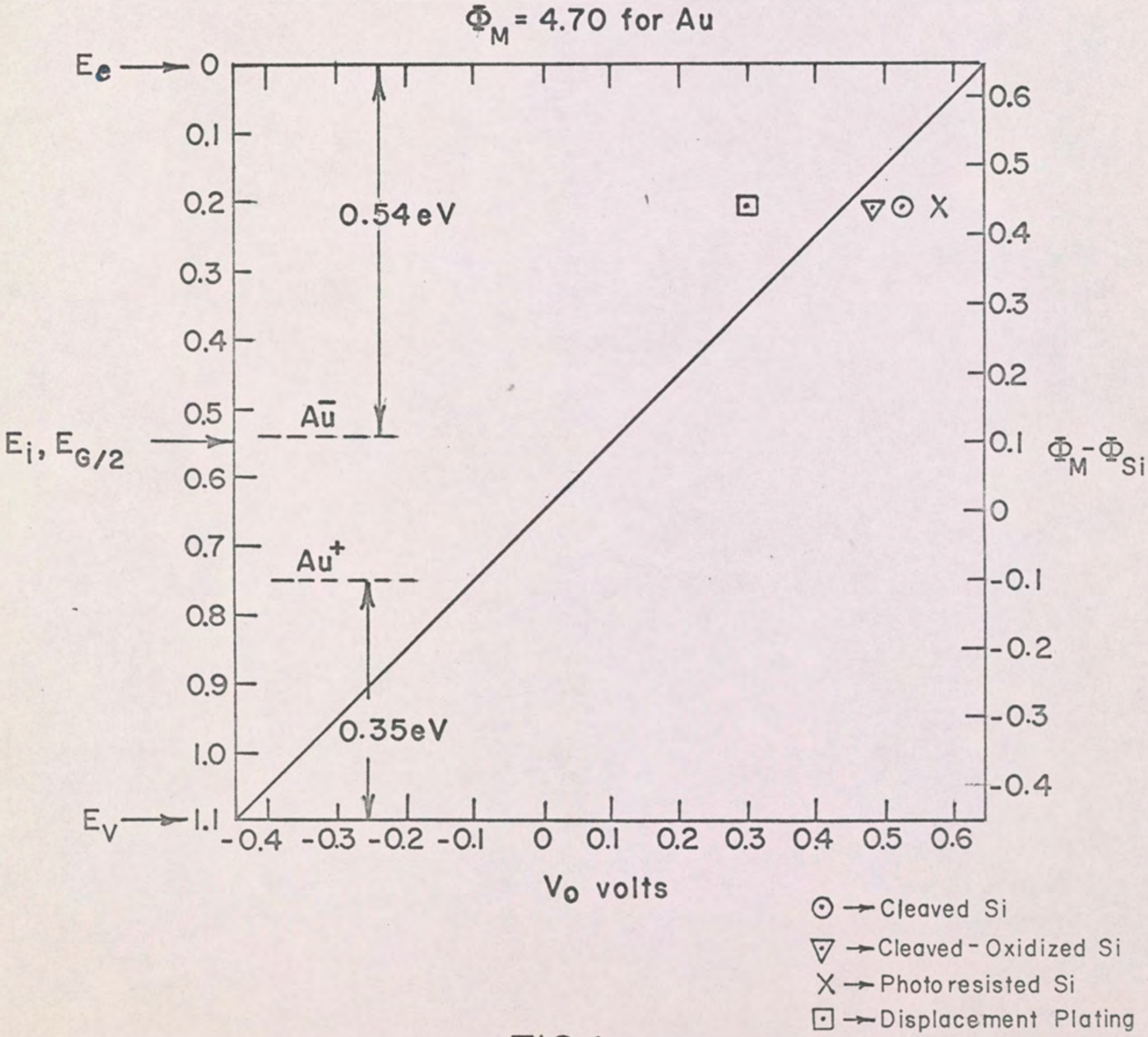
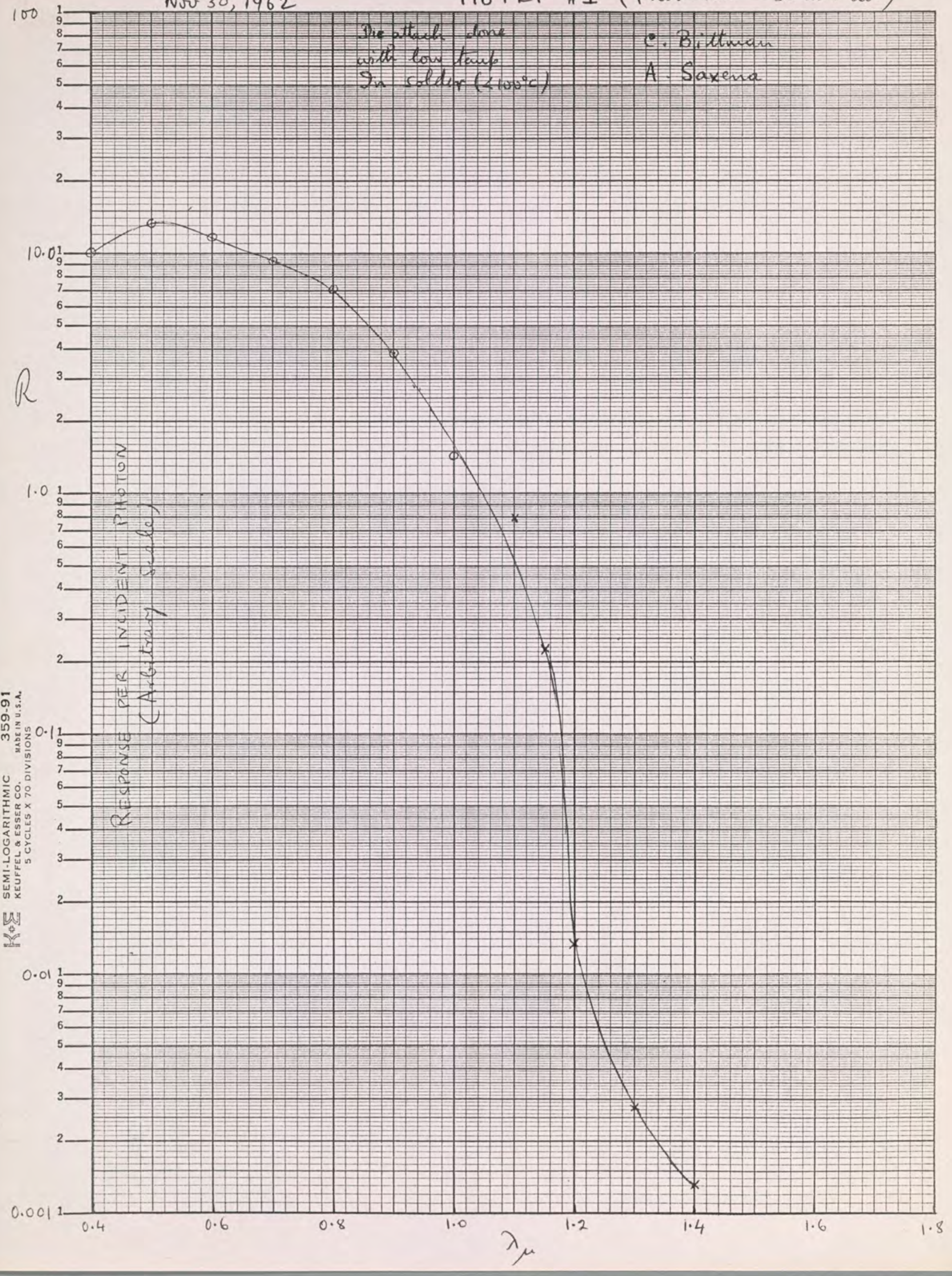
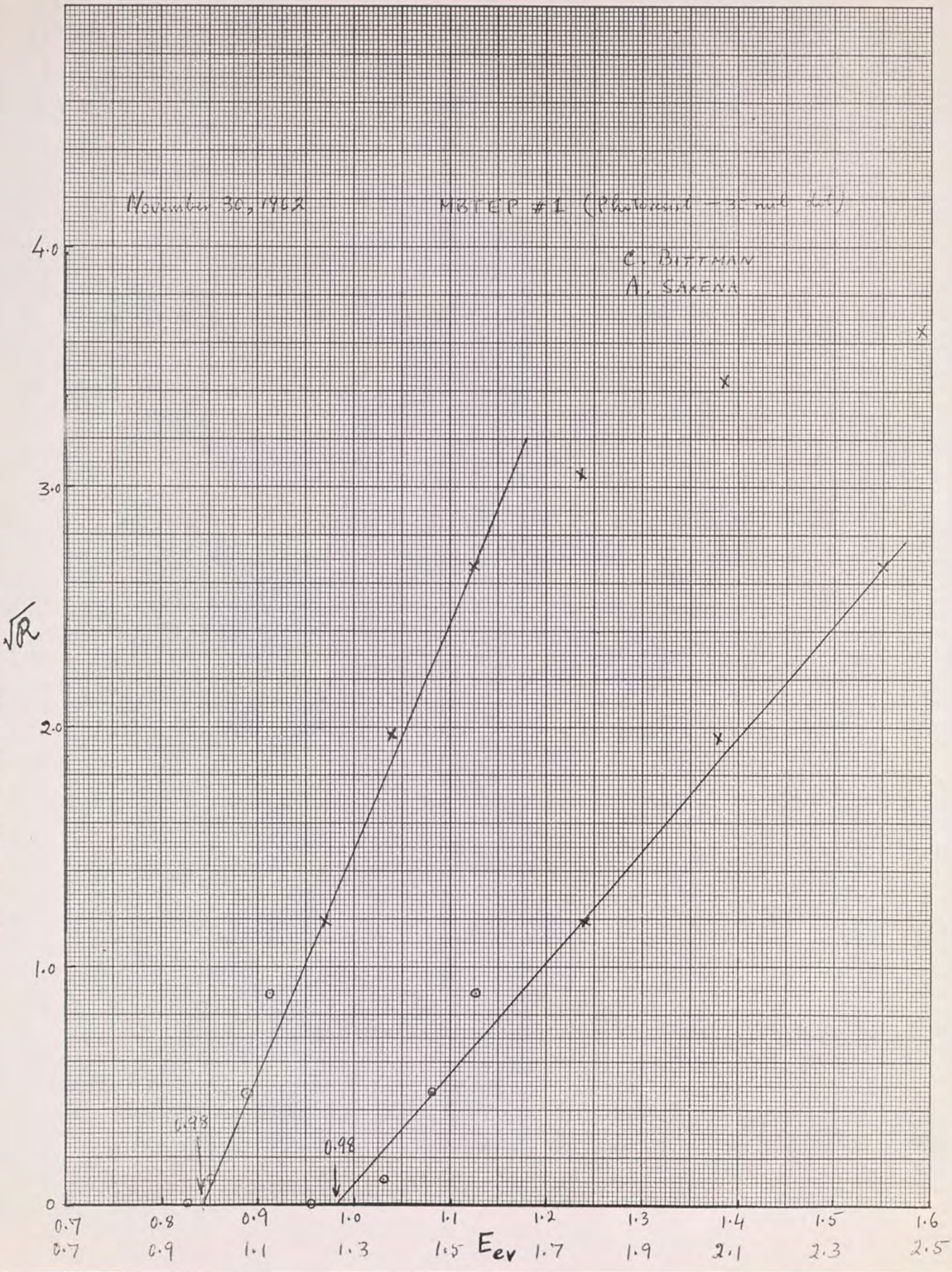


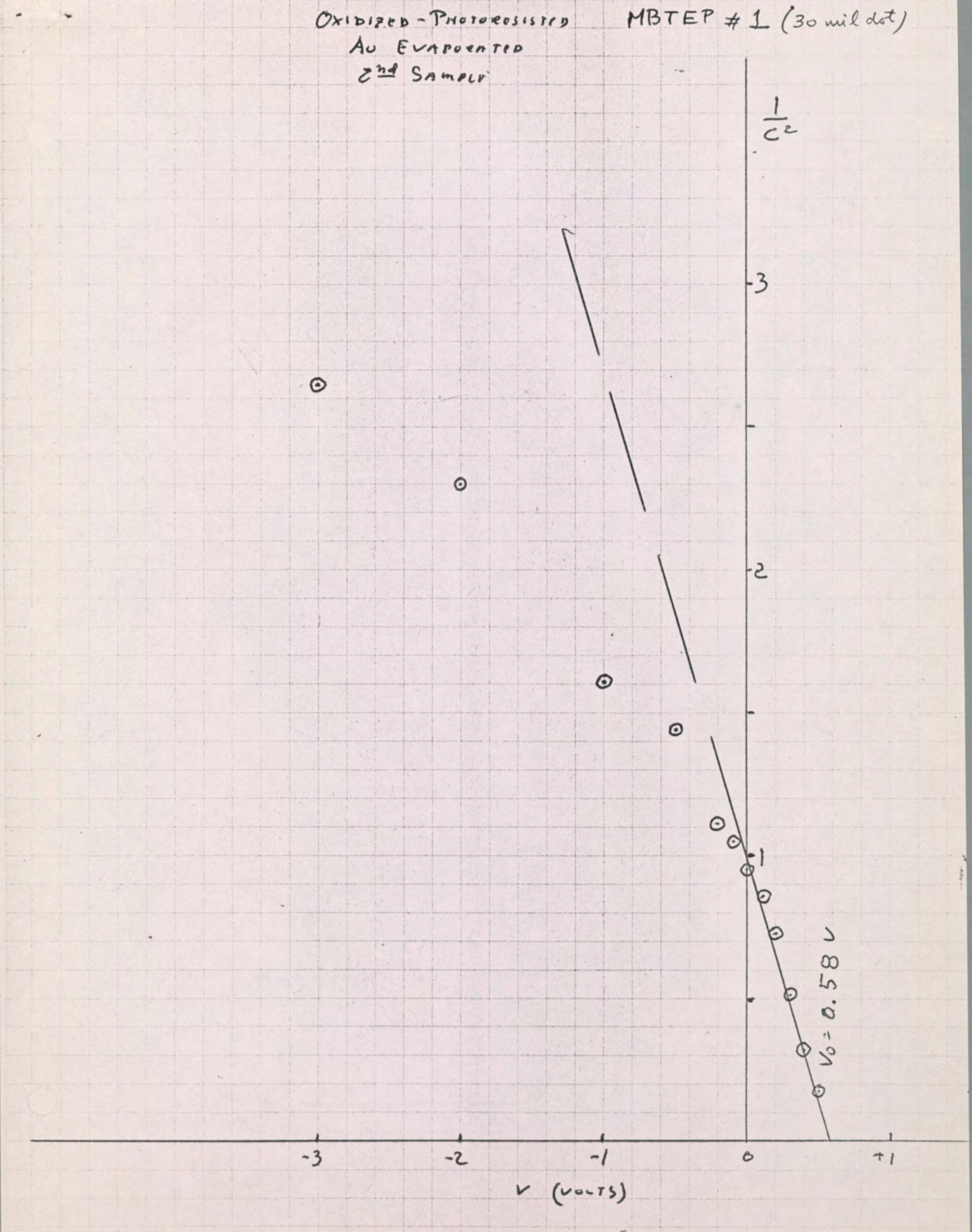
FIG. 1

Nov 30, 1962

MBTEP #1 (Photoresist — 30 mil dot)



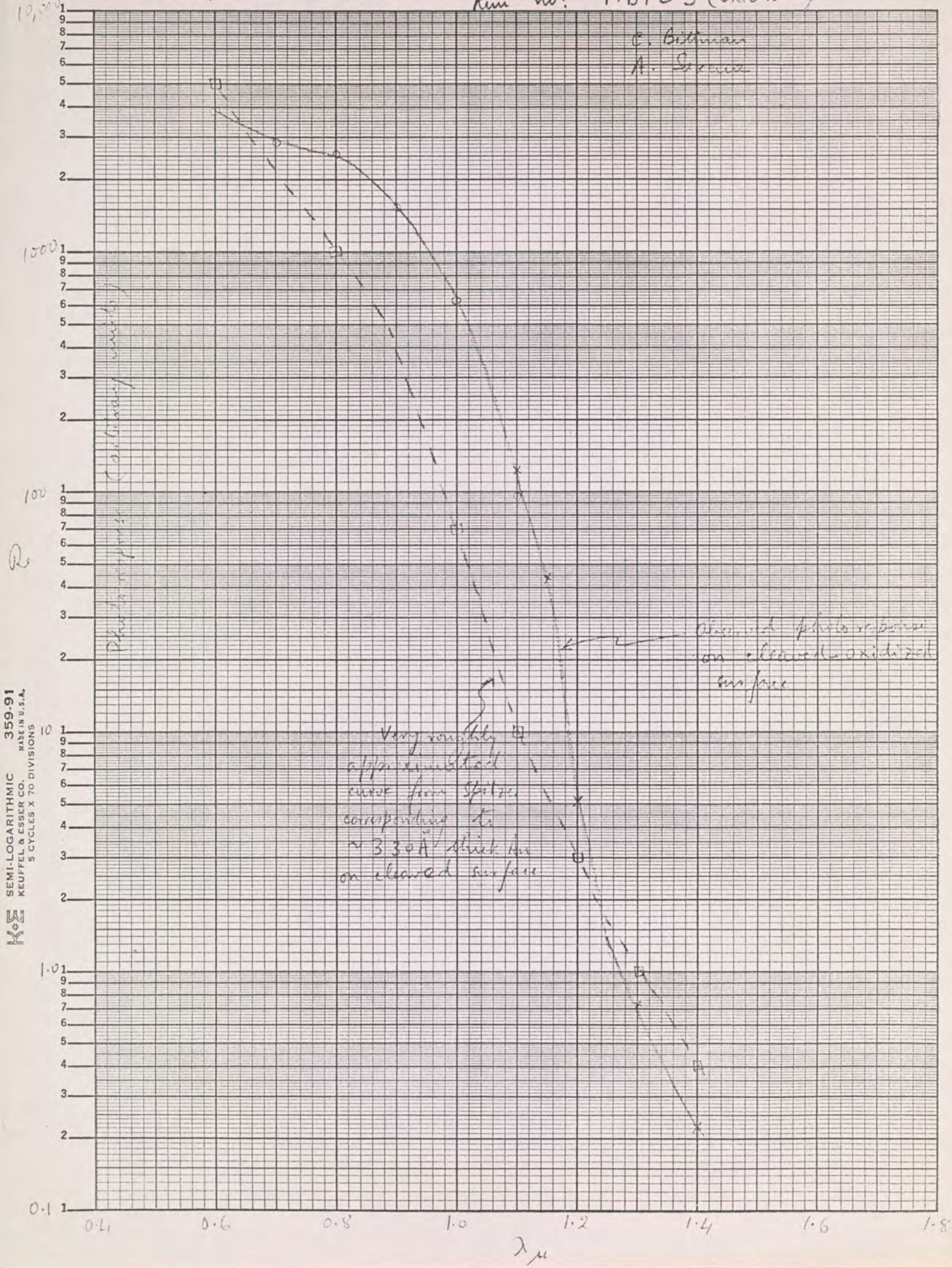

November 30, 1962
MBTEP #1
C. BITTMAN
A. SAXENA
√R
4.0
3.0
2.0
1.0
0
0.98
0.98
0.7 0.8 0.9 1.0 1.1 1.2 1.3 1.4 1.5 1.6
0.7 0.9 1.1 1.3 1.5 1.7 1.9 2.1 2.3 2.5
E_{ev}

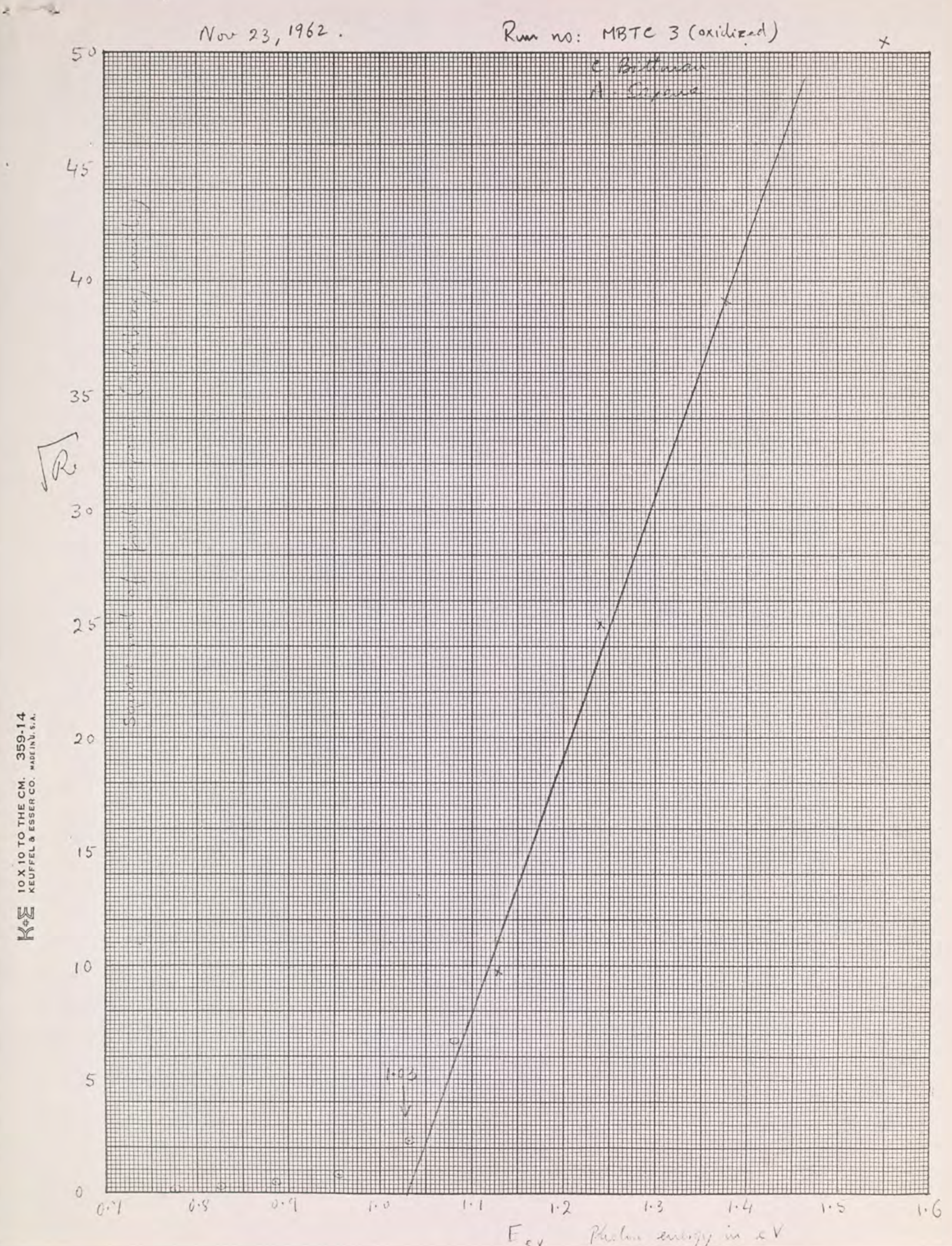


OXIDIZED - PHOTORESISTED
AU EVAPORATED
2nd SAMPLE
MBTEP # 1 (30 mil dot)
1/C²
3
2
1
Vo = 0.58 v
-3
-2
-1
0
+1
V (VOLTS)

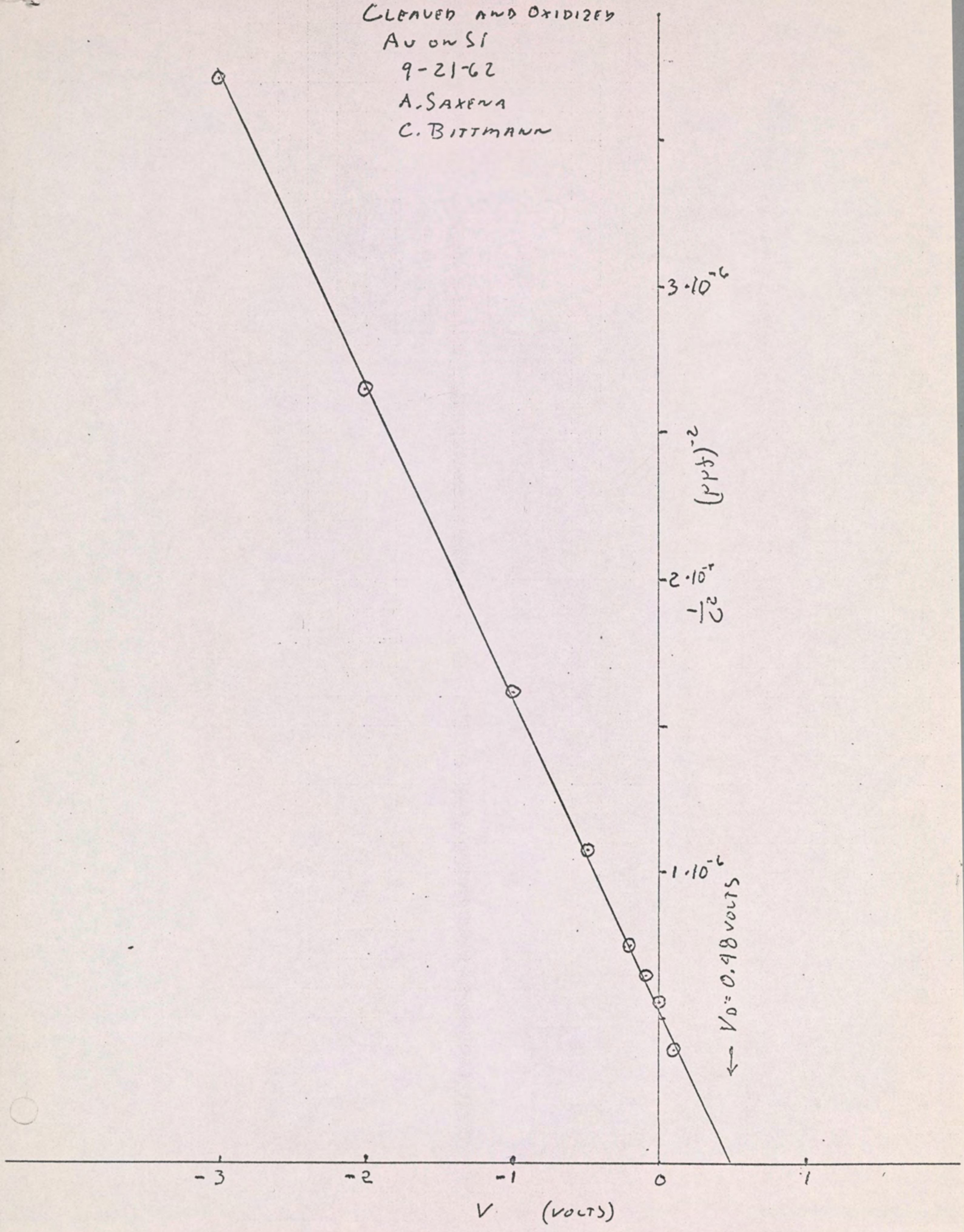
Nov 23, 1962

Run no: MBTC 3 (oxidized)



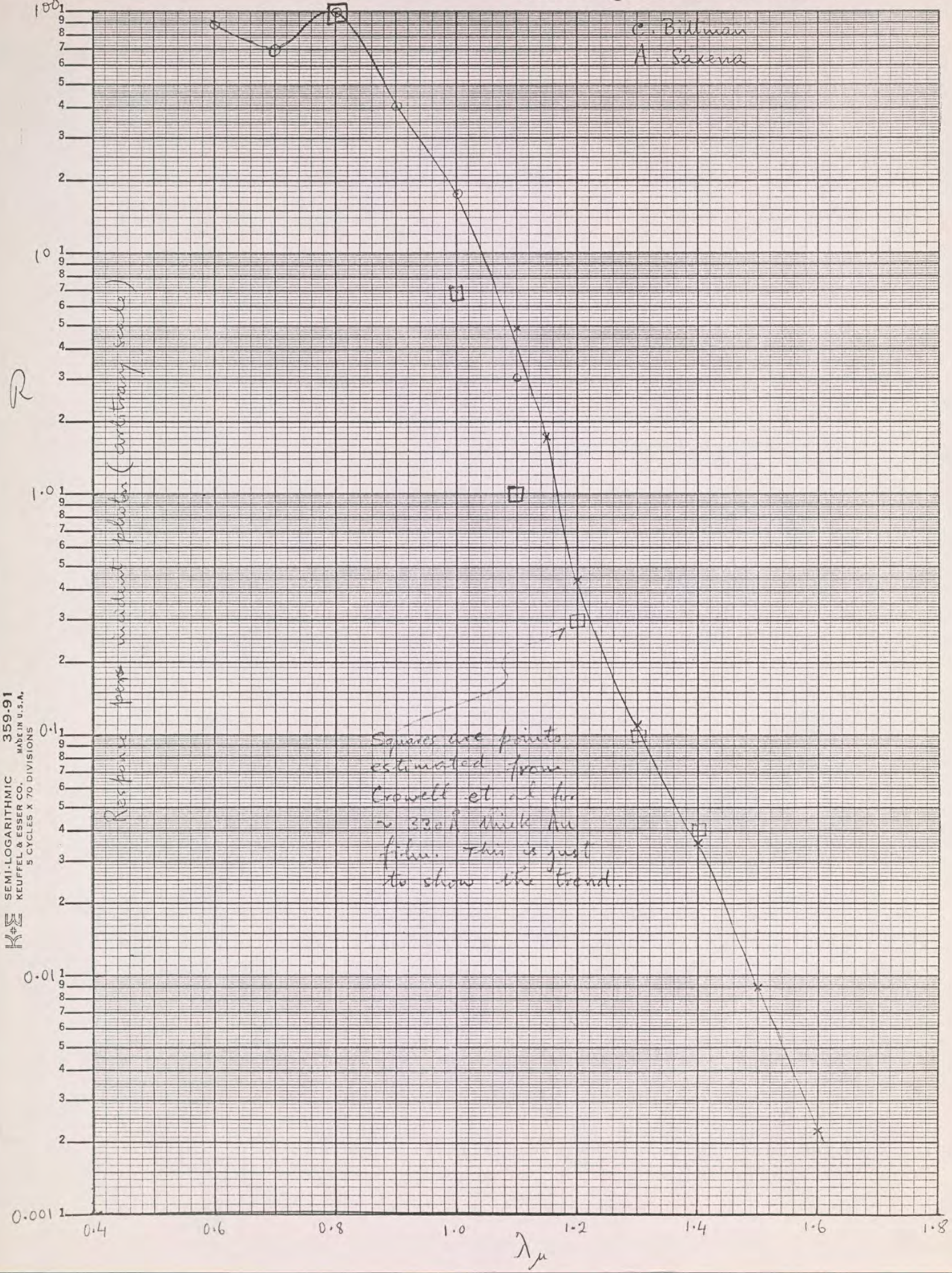


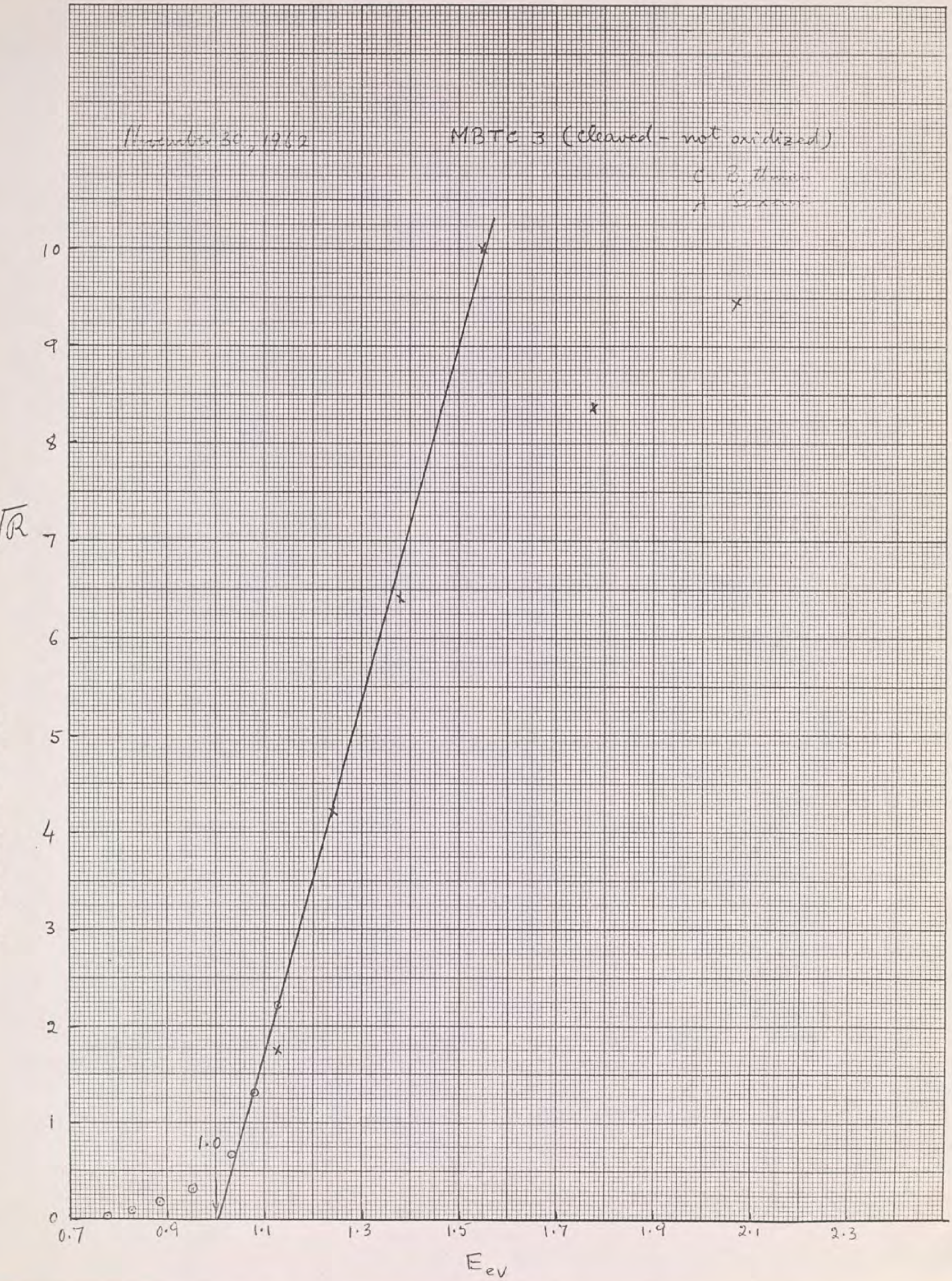
Nov 23, 1962.
Run no: MBTC 3 (oxidized)
C. Bittman
A. Sayama
$\sqrt{R}$
Square root of photo response (arbitrary units)
1.03
E_{ev} Photon energy in eV
0.7
0.8
0.9
1.0
1.1
1.2
1.3
1.4
1.5
1.6
0
5
10
15
20
25
30
35
40
45
50
K+E 10 X 10 TO THE CM. 359-14 KEUFFEL & ESSER CO. MADE IN U.S.A.


CLEAVED AND OXIDIZED
Au on Si
9-21-62
A. SAXENA
C. BITTMANN
3·10⁻⁶
2·10⁻⁶
1·10⁻⁶
$\frac{1}{C^2}$ (pfd)⁻²
← V_D = 0.48 VOLTS
-3
-2
-1
0
1
V (VOLTS)

Nov. 26, 1962.

MBTC 3 (Cleaved – not oxidized)

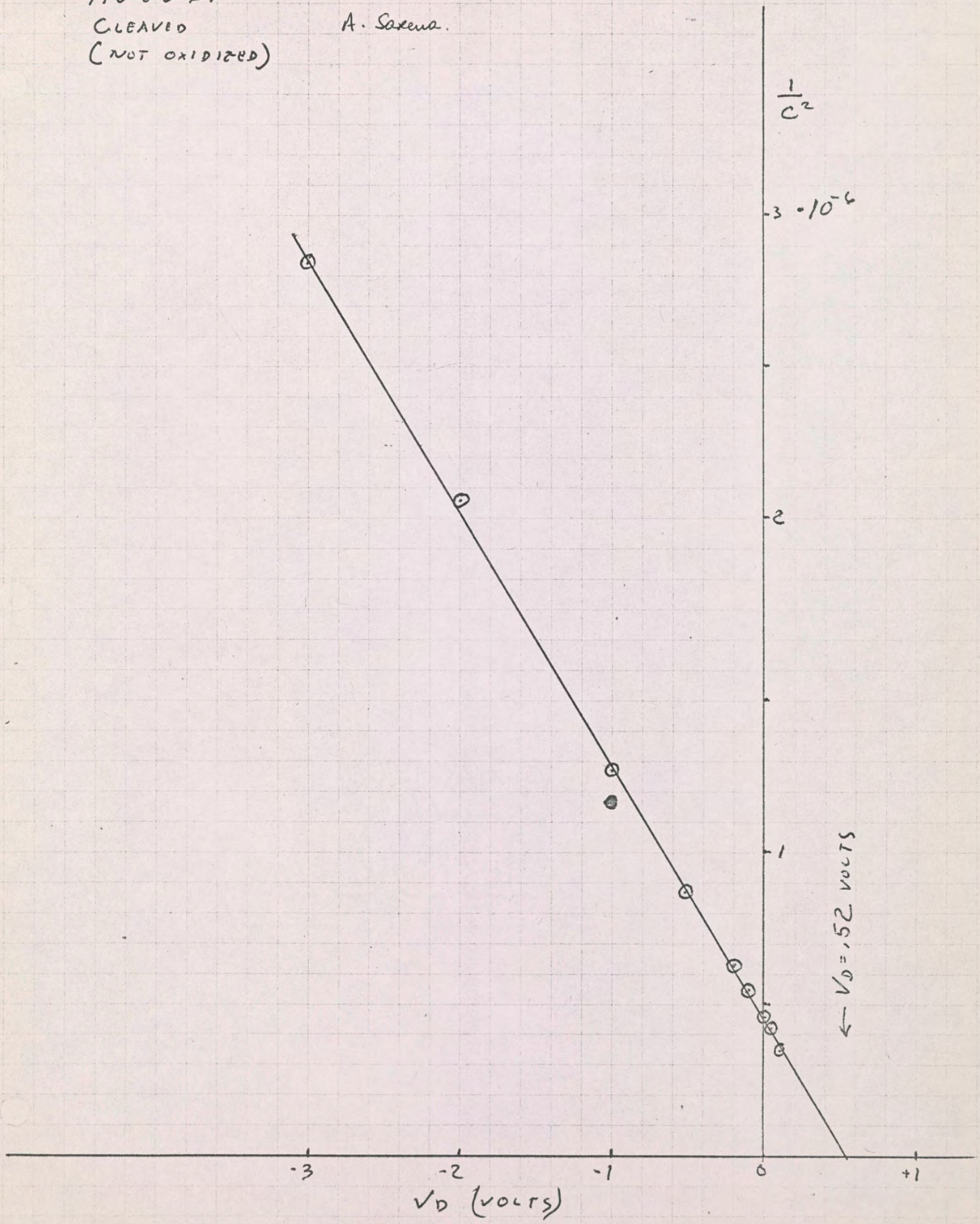


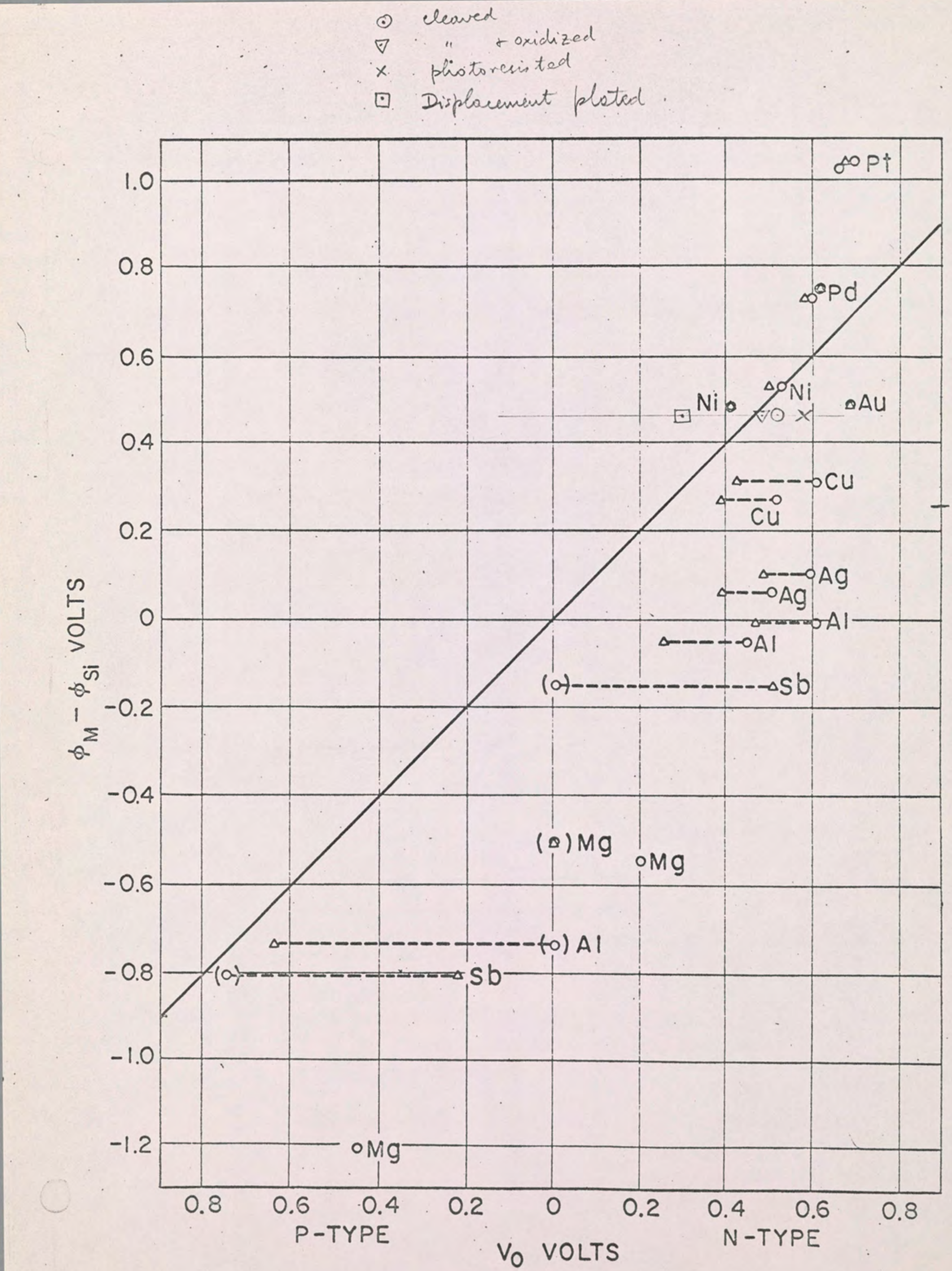

November 30, 1962
MBTC 3 (cleaved - not oxidized)
$\sqrt{R}$
10
9
8
7
6
5
4
3
2
1
0
1.0
0.7
0.9
1.1
1.3
1.5
1.7
1.9
2.1
2.3
E_{ev}

MBTC 3
Au on Si
CLEAVED
(NOT OXIDIZED)

Nov. 26, 1962

C. Bittman
A. Saxena





cleaved
" + oxidized
photoresisted
Displacement plated
Pt
Pd
Ni
Ni
Au
Cu
Cu
Ag
Ag
Al
Al
Sb
Mg
Mg
Al
Sb
Mg
1.0
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1.0
-1.2
$\phi_M - \phi_{Si}$ VOLTS
0.8
0.6
0.4
0.2
0
0.2
0.4
0.6
0.8
P-TYPE
N-TYPE
V_0 VOLTS

PROJECT REVIEW - PROJECT 178

PROBLEMS, POSSIBLE SOLUTIONS, AND REQUIREMENTS

—////—

I. MAGNETIC FILMS

A. $\frac{H_c}{H_k} \sim 1$ is presently not available at H_c, H_k of 5 - 10.

Solutions: (1) adjustment of evaporation parameters

(2) adjustment of impurities in the alloys

(3) substrate surface control.

B. Array uniformity requires improvement.

Solutions: (1) above (1)

(2) above (3)

Requirements: 1 vacuum system (18" bell)

1 experienced engineer or MTS

1 experienced technician.

II. PROTOTYPE DEVELOPMENT

A. Adherence at Ag-SiO_2 and SiO-Cu: interfaces are poor and maybe the permalloy - SiO interfaces also.

Solutions: (1) Improvement of technique

(2) Variation of insulators and conductor materials

(3) Variation of etching solutions

B. Pinholes are due to atmospheric dirt, substrate imperfections and SiO splatter.

Solutions: (1) Dust free hood and a good method

(2) Substrate coatings (SiO)

(3) Splatter preventing source for SiO

C. Masking and Etching procedures have to combine mechanical and photoresist masking. Need a KPR remover compatable with copper or use another metal for conductors. Need etching solutions that will not lift the films.

Solutions: (1) Need better etching solutions

(2) Will have to use thicker aluminum films for conductors.

Requirements: 1 Vacuum system (18" bell)

1 Experienced engineer or MTS

2 Experienced technicians.

APH:jt
12-5-62

III. FUNDAMENTALS

A. Magnetic films and switching behavior are not understood.

Solutions: (1) Bitter pattern observation of domains

(2) Correlation of magnetic and metallurgical properties

(3) Correlation of stress and magnetic properties

(4) Sensitive torquemeter measurements

Requirements: Sensitive torquementer

1 experienced MTS

IV. PRACTICAL SYSTEM AND JIGGING FOR "PILOT LINE" MEMORIES

Requirements: 1 large vacuum system

1 experienced engineer

1 experienced technician

APH:jt
12-4-62

THIN FILM DEPOSITION

The present rate of progress in solving the formidable problems of deposition of film and conductor arrays makes timely completion of a thin film memory as previously proposed unlikely (per memo "Development Plan for a Magnetic Thin Film Memory" to V. H. Grinich dated 8/31/62 by H. A. Perkins). Aside from the delay in acquiring the requisite thin film technology, the effectiveness of circuit and system design is greatly hampered by lack of a memory film array model. The locally available film technology is being reviewed in an attempt to provide a useful interim model of lower storage density which does not require high coercivity magnetic material or a deposited conductor matrix. (the most formidable problems at present). The intention is to provide a test vehicle hopefully permitting effective circuit and system work to continue while deposition problems either are solved or the probable eventual limits of our thin film capability are more clearly defined.

Since 30 x 60 spots exhibit some switching on the dynamic tester, and presumably should have H_C compatible with H_D, the following program should be pursued for the next few weeks (also mask exists):

1. Lay down Cu-SiO-Cu to finish present experiment until electromagnet is ready.
2. Lay down Ag-SiO-NiFe (30 x 60) (spots thru mask)
   a. To evaluate spots over ground plane dynamically
   b. To permit making an overlay breadboard so that some approximation of the storage matrix problem is available for circuit and system development.
3. Lay down Ag-SiO-NiFe in continuous films.
   a. Evaluate unetched with looper and dynamic tester
   b. Etch 30 x 60, and 10 x 20 spots and re-evaluate
4. Determine means to get H_C as high as we are able with other usable film properties (hopefully > 5 oe).
5. Determine techniques to get rid of pinholes thru oxide so that conductors may be evaporated on assumption that (1) above will disclose such a problem.
6. After (4) and (5) are solved, try to make complete 1"x1" spot and conductor array per proposed design.

12/4/62

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12/4/62

12/5/62 — Project 178 — Magnetic Film

Sah
Hale
Perkins
Schmidt
Moore

We are way short handed!
Many problems.

(at G.E. Raffael Rappiano ?)

Perkins suggestion:
First aim at getting large spots to try.
Second need high Hc

Hale thinks that aiming at correct impurities will raise Hc.

Small geometry reliability meeting: 12/6/62

VHG
GM
Everybody from Mtn View

Jay Early: The problems:

1. Al wire
2. Epitaxial I_{co} @ 300°C
3. Popping of epitaxial during testing — EC problem, some β degrad (50→3 for eg.)

		300°C @ 300 hrs
118	1340	0 failure
96	1341	15 I_{CBO}
87	TI 2N706	2 catastrophic, 1 I_{EBO}

(Ross Tucker)

12/7/62, <u>Imperfections</u>

Pyramids (Pyr's)
Triangles (Δ's)
Holes

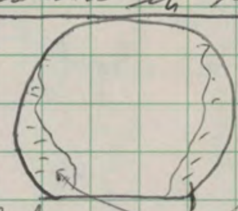
Tucker
Lucius
Flint
Sah
Wigton

Pyramids + Triangles: 5μ B-diffused layer on 20-25μ layer ~10-cm. Mesa around pyramid
All c̄ Pyr or T were soft 3 ma @ 100 v
or 115 v hard breakdown except base.
For two wafers ~~one~~ and one run the Pyr, Δ's all showed 3 ma ± 1 softness @ 100 v.

Some of the Pyr have n-type cores above the original wafer – i.e., no real evidence of preferential diffusion.

Pyr's & Δ's appear in the same area in ratio ~ 5 : 1.

By etching away Pyr's with pitting Pyr were followed and <u>dislocations in the substrate don't correlate.</u>



Some preliminary evidence (~~and lots of speculation~~) suggest that there are "bad regions" in dense pitted Δ's called stacking faults because of orientation & dislocation pattern.

A Pyr always is on top of a Δ.

Proposal is that a Δ gets Δ (have even seen Δ at starting
Presumably the truncated Pyr don't intersect at a point.

In order to write nice H's on the Pyr planes, we must strain the Xtal 5°.

 Dec 10, 1962 - prelating

Schultz
Farina
Seeds
Lamond
Moore

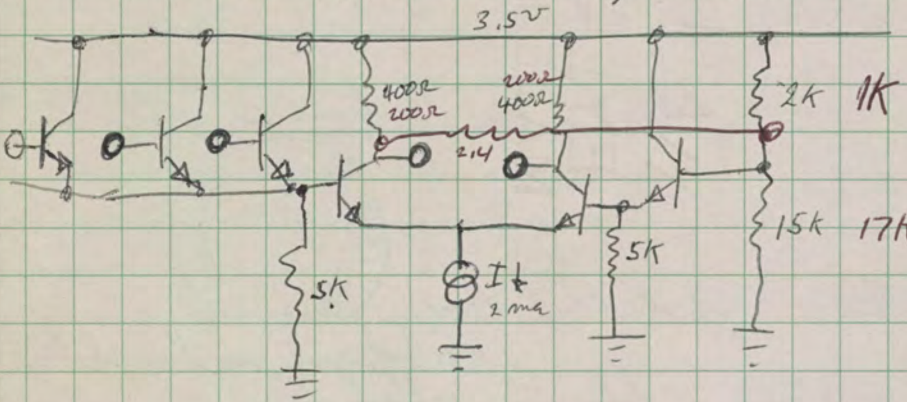
S-epi released to 55 X 55 chip

We are already behind schedule

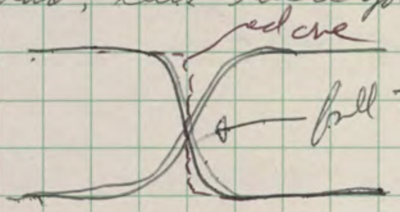
New stuff

High Speed: We have a couple of good possibilities

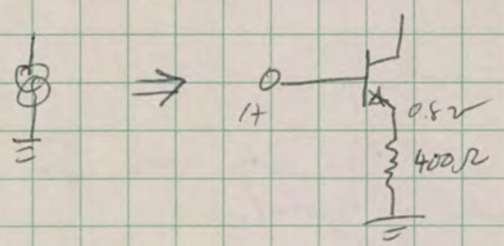
Instead of our old way of looking at, Don + Bob said: lets look at only <10 ns and take mw, lets look at <3 mw, take speed.



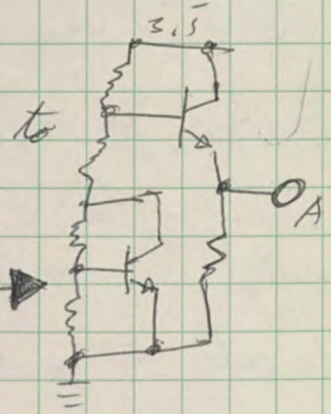
If the current source tracks with temperature, this has a good characteristic



7 X 5 = 35
7 X 2 + 28 = 42
4 X 8 = 32
points 109



, also A converts to

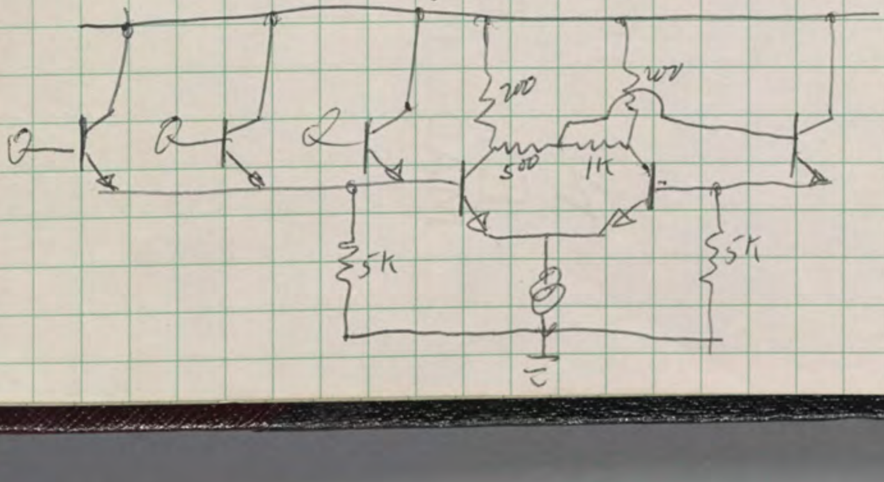


One reference block per board. Reference and elements must be the same T.

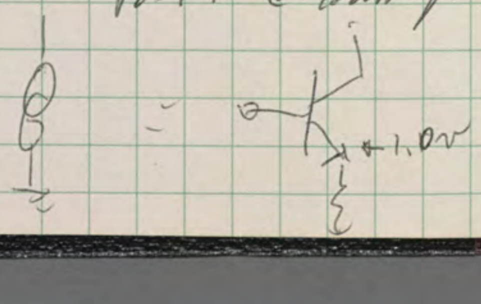
using 1312's
5 n sec @ F/I = F/O = 1
12 n sec @ " " = 1 + 24 pf added to look like F/O of 5.

By adding the red line feedback, sharpen the output and help the tpd at loaded conditions

One can go further



by a little diddle one gets a FF @ same power.



Design Rules

Resistors:

R_1: centertapped 2 mil wide diffused P-type - 100 Ω/□

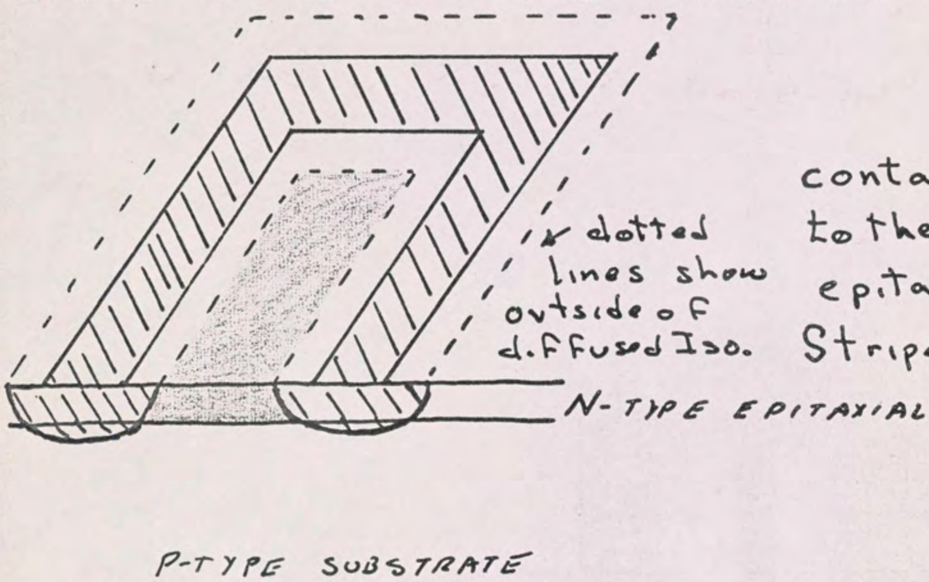
R_2: (a) 1 mil wide diffused P-type - 100 Ω/□

(b) N-type epitaxial region

R_3: 2 mil wide diffused P-type - 100 Ω/□

R_4: 2 mil wide 1500 Ω - tapped for three 500 Ω resistors - diffused P-type - 100 Ω/□

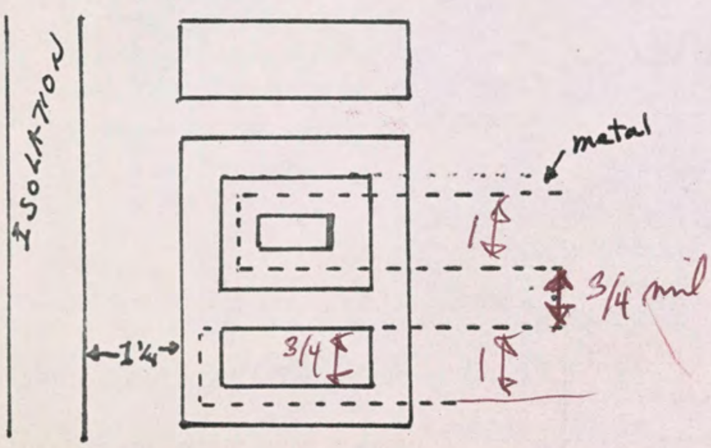
I dea for a 500 Ω/□ Resistor:



contact to be made to the (shaded) N-type epitaxial layer. Striped area is Isolation.

Transistors:

A. 1 square = 0.25 mil



This cuts indexing tolerance to ± 1/4 mil from ± 1/2 mil. It changes metal cut to 3/4 mil and oxide to 1/2 mil cut.

Type A: Collector - 1 x 3 mil 1/2 mil from base.

Base - 3.75 x 3 mil with 0.75 x 2 mil cutout 1/2 mil from bottom and edges.

Emitter - 1.5 x 2 mil, 1/2 mil from edges, with 1/2 x 1 mil cutout centered.

B.

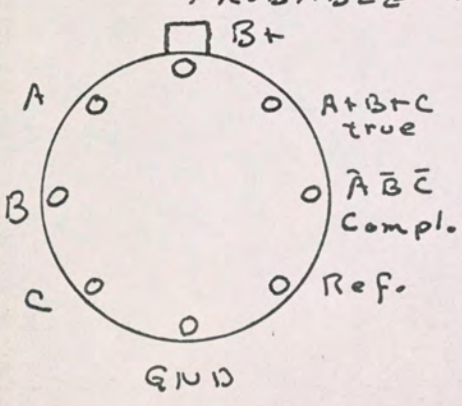
The type-B transistor is similar to the type-A, the difference being that the emitter and base cutouts are made 1/2 mil shorter (em. 1/2 x 1/2 + base 1/2 x 3/4) so that the entire transistor can be made 1/2 mil narrower.

In both cases the collector metal need only cover its cutout; the emitter metal should always overlap by 1/4 mil on all sides; the base metal should overlap 1/4 mil when possible.

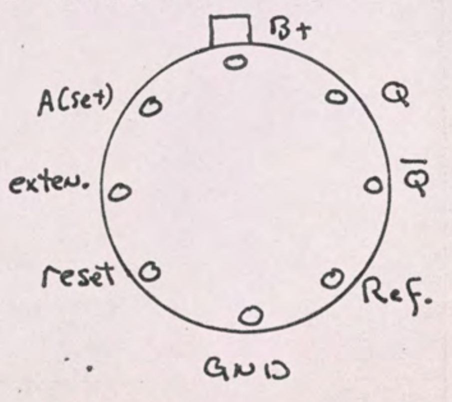
Two metal conductors may pass no ~~less~~ than 1 mil from one another except for very short distances when absolutely necessary this may be made 3/4 mil (eg. between base contact + emitter contact).

The isolation region can be brought to 1 1/4 mil from diffused devices and can be only 3/4 mil wide.

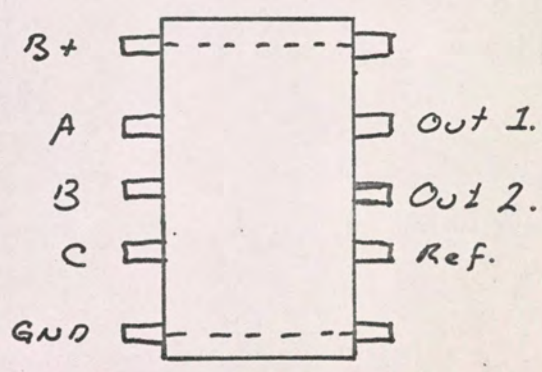
PROBABLE PAD LAYOUT:



GATE



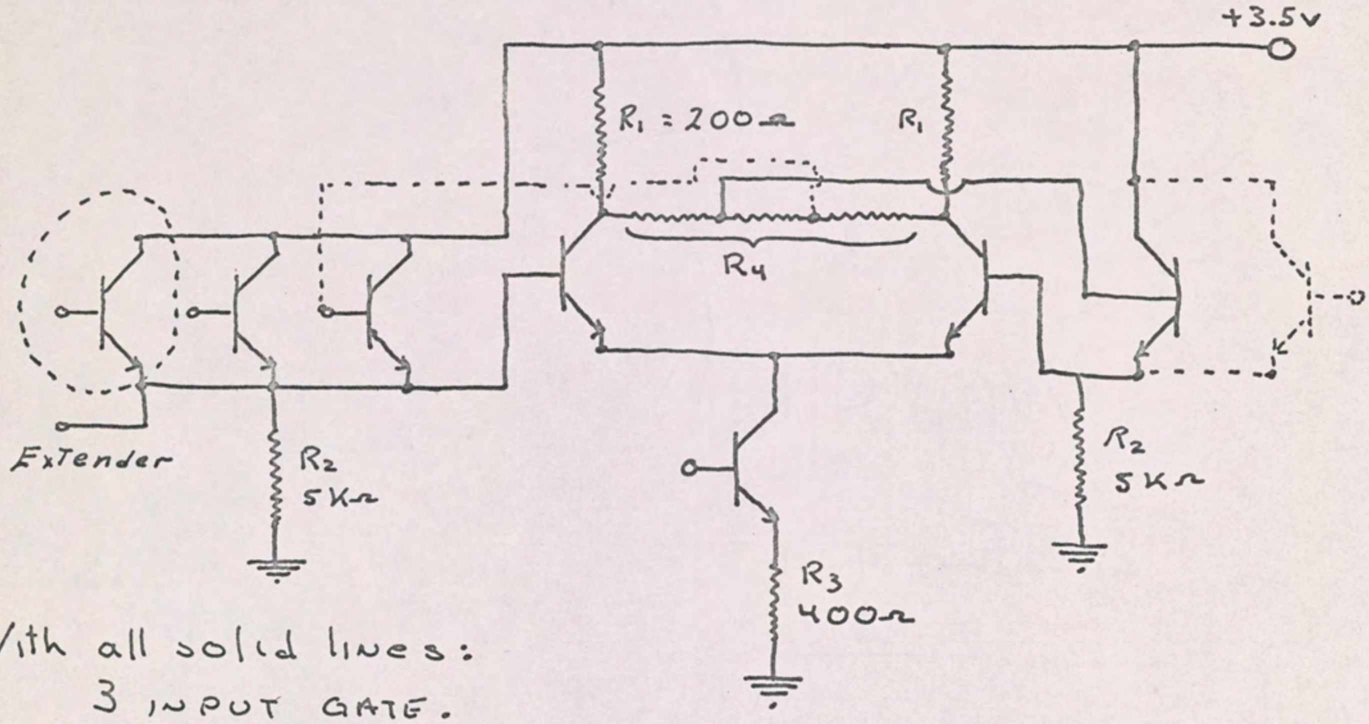
Flip-Flop



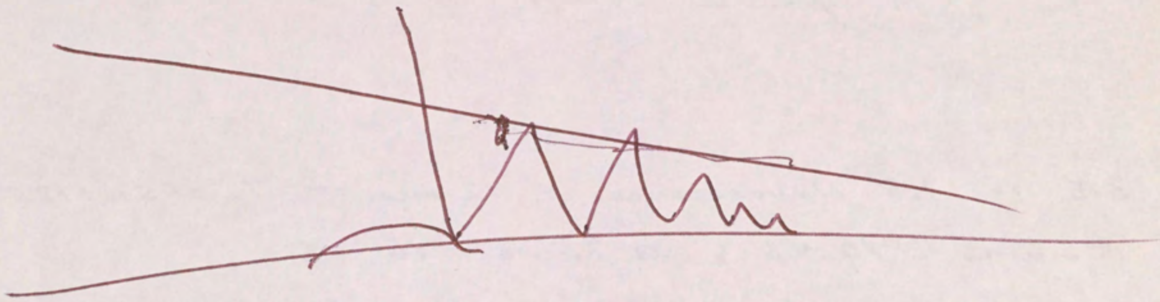
μL-II HIGH SPEED

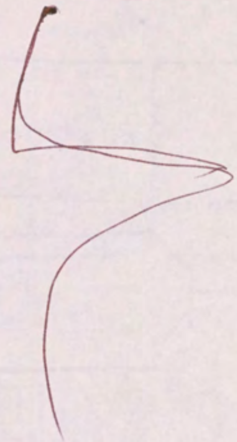
3.5 to 7.5 Nanoseconds @ 12 mw. – T. -55 to +125 °C

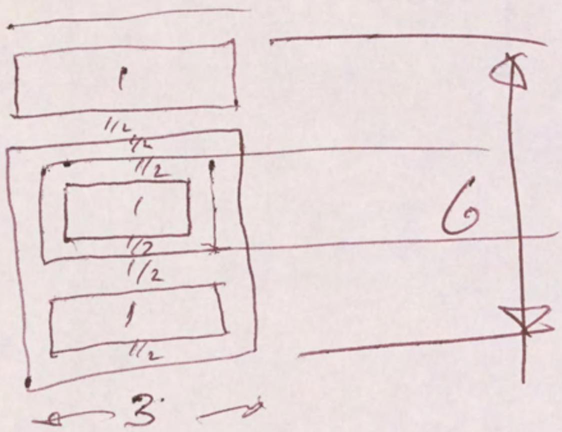
@ 3.5 ns · F/O → 1 ; @ 7.5 ns – F/O → 5 .



With all solid lines:
3 INPUT GATE.
With dotted lines, and Removing circled transistor: Flip-Flop.






1
1/2
1/2
1/2
1
1/2
1/2
1
1/2
6
3

Schultz thinks this looks great !!

We should layout a Gate/FF.
Don laid out c̄ a ~~80~~ pinch-off resistor to get 35 mil² 135 active area

Dec 17, 1962 #

HSG –
Layout c̄ epitaxial layer for resistors for 5K can get gates and flipflop on 50 mils center

List of proprietary FSC μ ckts.
0.
1. CML – (G + FF) per above.
   ⊘ Layout to Fok — 12/19
   Masks to Fairina — 1/4, Get ~~isolation~~ N+ mask (orig. master) ASAP)
   Dice to Die sort — 1/25
   1st two-runs evaluated — 2/4 – for this meeting.
2. ~~R element~~ S-epitaxial test vehicle, ½ line, 1/4 tolerances 3 mil pad vs 1 mil, ½ mil line 6 mil pad
   Layout to Fok 1/4, Both geometry masks 2/4, Runs thru 3/1, D.S. evaluation by 3/11, cancel units.
3. Reference voltage Diode for CML – Wait for Gates to see voltage.

4. Low power ~~gate~~ family — 2X3 GATE, BINARY. — Ckt layout on Jan 7 and go-go-go decision
5. μL-1 R-element }
   Probably the same ckt
6. Binary μL element } Have ckt determined 1/4, Rough layout 1/4. We will do here as soon as some evaluation runs are thru.

7. Automatic low power gate (2-3 input gates)

8

9.

10.

For next time → 1/7/63

1. Evaluation of epi G's. — Don
2. CML G - mask & schedule — Ron
3. Discussion of low Power family. — Dan + Bob
4. Ckt & layout in lg then for μL-1 R element – Don

 Dec 18, 1962 Section meeting

KPR first - Gene Blom

1. Basic resolution study KOR ~~KPR~~ KPA, KMER

2. Small geometry edge definition by use of Cr with SiO antihalation coating,
   Comparative results in next few days.

3. Cleaning cycle evaluation. Flat substrate.

Mtn View is doing work with a bleached image that is transparent to visible and opaque to UV.

Mask making:

S+R shut down on Thurs. Final grinding of reference being done.

Lens settings are not reproducible.

Today check the possibility of setting the control unit to minimize the error.

Trying to use broader band light to use with the S+R camera.

Manual Camera used just to test various parts.

File being cut down.

Dec 18, 1962 - Epitaxial Meeting

New Reactor Material:

Getting some fall out from film apparently too thin. Bimodal dist. on BV for thin.

John Schroeder will run Sb in As vs T for Xstain - X_{IR}.

~~Gupta~~ will give me a picture of chevrons.

CP-6 vs CP-8 and mechanical polish.

~~Mtm View will try CP 8.~~

Harl & John will look at surfaces

~~Before~~

For next time:

Them:

Before & after (Ruf) Mech. pol — J.S. Vapor etch

We will supply best mech polished material.

Film grown on chem mech.

We:

Junction evaluation

Orig prep.

Vapor etch ~~vs~~ none,

CP-8, CP-6, Chem Mech, Mech. Pol.

Next meeting. Jan 15

Dec 20 – Small geometry reliability

Of 675 units called 1340, 163 were 1341's

25 failed on life (all condition)
15 were 1341
10 " 1340

lots 6137 were 75/75 1341's – 6 failures, 5 ~~were~~ I_{CBO} on 300°C, 1 open on environmental
lot 6139 " 65/75.

	300	200	Op
1340	4 (2 I_{CBO}, 1 open, 1 V_{BE}) / 225	0 / 75	4 I_{CBO} / 225
1341 mixed	15 I_{CBO}, 1 open / 225	0/75	7 I_{CBO}, 3 O.dm – 2 h_{FE}, 1 open / 150 · ~~[illegible]~~
1341	4 I_{CBO} / 50	0 / 25 · 500	2 I_{CBO} / 50 · 1000 hrs

3 · 1000	3000	25	75
2 · 500	1000	25	25
1 · 250	250	25	15

All I_{CBO}'s are between 50 na and 100 μa.

∴ Ball park figures MTF

	300	200	op
1340	50K	>50K	50K
1341	6K	>50K	12K

The 200°C data certainly seems to suggest that test equipment is not at fault.

Dec 26 – Look at the Xducer Plan

Zinker
Kobell
Blinder

1st needs – assembly – test

Mike Dragonis can do now. We will talk with him re: possibility.

We will get a diffusion-machining body

Hire three techs – Fab
– Sub-assembly & assembly
– Test & calibrate

These will be trained in lab and Xfer.

Equipment order

1st product to be chosen as 0-100 or 0-500. Blinder to get these ASAP.

Nozzone staff mtg. 12/27/63

List for Jim fest. — Next time.

List of ideas for a Weekend discussion

COMPONENTS	1961	1962	1963	1964	1965	1966	1967
Transistors (Si)	106 24	120 33	160 45	210 55	250 60	250 61	250 62
Diodes (Si)	114 4	100 8	120 10	135 13	150 15	150 15	150 15
Microcircuits	0 0	3 1	20 5	50 12	100 25	150 40	224 55
Memory (separate) Film & Active	0 0	1 0	5 0	25 1	50 5	75 10	100 20
Transducers	101 0	123 0	135 1	140 2	150 5	150 8	150 10
Inst: (Big Test Machines)	10 0	13 0	15 2	18 3	22 3	26 4	30 5
Lab Eqpt. (Pulse Gen. (D. V. M. (D. C. Amp.	45 0	53 0	65 1	80 2	95 3	105 4	120 5
Circuit Modules	5 0	6 0	7 0	8 1	10 1	11 1	12 2
Systems: Military	3000	3500	3500	3500	3600	3600	3600
Commercial	964	1140	1140	1140	1200	1200	1200

GEM/VHG
12/13/62

1/2/63 - Preproduct planning meeting meeting

Lemil
Ferguson

Small Geometry:

— Decision, Oct 29 Mtg

ABC 0000 — } a quy by 1/31
spi R.F 0001 —
14,500 0002 - } a quy by 1/31
~~0003~~
2½ 500 0006 } est ~~11~~/62, ready 4/1

1210 — as soon as adequate material
1211 →
1310 drop 10/29
1311 →
1321 ASAP (CDC)
1312 →
1324
1221 drop 10/29

1240
1243
1250
1340
1341

1450

3010
3011
3111 →
U-1

NPN
4200 →
4205 →
4300 ?(Slightly)
4011 ASAP
4016 →
4111 to develop, no schedule
3001 - 3006 drop immediately

PNP - Power
4500 -ASAP (automation)
4511 →
3511 →
1712 ASAP
1713 →
7500 R&D to make MIT units + 250 by 7/1 and life data

6206 - ? When?
7000 - When?

SCR-1 (400v) —
SCR-3 (IBM) —

 Product planning Meeting:

U-1.
The failure rate @ 30v, 150°C (~~200~~) fail at random times
the rate is high, the mechanism sick.

Try the opposite polarity FET's. — Us

Step stress — here.

Until we get a fix, we are out of the FET business.

1311 — Some runs have CB go soft at emitter diffusion —
~20% come thru c̄ good hard diodes.

1321 — does not have this problem

Only real difference is a 2-step base diffusion on 1311 and
one step on 1321

1211 — Header problem — electrical leakage

3111 — Fouled up.
Prefer >30 on LV_{CEO}, but accept to 20.
Material should be a little thinner than 9-12 called out.

1221 — Stay dead, push 0002

1450 — Hard to make to spec. Bad low current.
Poor ratio, low values.

NPM

4016 Being made in production on schedule
No consistency, but ? no knowledge on units.
Spec characterization by 2/1. Jack up to 2000/wk ASAP
Tom R. to get life test.

4011 — Drop

PNP

1712-1713 - 1 run per day — Continue to aim @ 5K/week

There is a reliability problem on these (??)

2000mw 100°C — 2/10 fail over weekend - bad CB junction
10v 160°C — 1/10 " " " — " " "

(Three Northern Electric units looked good under life — these were high voltage (and presumably planar)).

Ehlen will ~~[illegible]~~ life test 1713.
Characterize by 1/15

4511

200, 300 static
op. (10v) 100°C, 150mw

Friday @ 300

3511 — Data sheet out

6205
~~6205~~ — Had lead bond problem. 1st units out this week. ~200 will go to ap eng. ~~Go~~ Good die sort yield (>30% for ever).

Application to get ~ ~~[illegible]~~ more units in sept this week

Characteristics by 2/15.

7000 150 units given to [illegible]
60 of these were Xstors.

~~7005~~ is still fighting them. ~~At~~ M.O. will get ~5 runs thru on 2/1. Characterization is lower priority than others

This is wiped out now because HP-9 masks must be used.

∴ Make new mask.

→ Work hard at R+D to get >50 watts

SCR-1 Run ~~[illegible]~~ Mtn View at Feb 15. TO-5 @ 9/16" stud

SCR-3 (IBM) —

Jan 3, 1963 — Resistors
last ~~Jan~~ Dec 4

Campbell
Waits
Talbert
Sah
Moore

Nichrome:

Work on annealing after evaporation:

	Evap	anneal
1.	room temp	—
2.	" "	½ hr @ 300°
3.	100°	—
4.	200°	—
5.	200°	½ hr @ 300°
6.	500°	25 min @ 400°

Only conclusion: Change in R during alloying went down on last 3
on " " " " " up on other.

Run not well split.
~~TCR~~ TCR in 150 - 350 except 500° run ~ 500-600 ppm.

Talbert - saga base res made low TCR's

Plan:
1. Make a film that will not change during alloying
a) V. high substrate T
b) Evap. in a O_2 atmosphere
c) Alloy in vacuum.

Check on data in two weeks when CTS comes back

Cermets: 300-400 ppm
poor stability @ 200°C - drifting and drifting (2000-4000 Ω/□)
have ~50% change during alloy

AlOxors

A contact problem exists, they must be "formed". Then the R's have a nice spread.

Below Distribution December 10, 1962

0

Visit of Applicant - Eugene Meieran Donald Palmer

Eugene Meieran - Ph.D. Metallurgy, February 1963 - plans to visit with us on Wednesday, December 19, to discuss employment possibilities with various members of our Technical Staff. A copy of his personnel file is attached for your information.

In order to make his visit as enlightening as possible for all concerned, the following schedule of activities should, if possible, be followed on the day of his visit:

10:00 - 10:30	Don Palmer
10:30 - 12:00	Meet with Gordon Moore, Worden Waring and Tom Sah in Executive Conference Room.
12:00 - 1:30	Lunch with available members of above group.
1:30 - 3:00	Worden Waring and members of his group.
3:00 - 4:00	Tom Sah and members of his group.
4:00 - 4:30	Gordon Moore
4:30	Don Palmer

In order to complete Meieran's personnel file, the attached evaluation form should be completed and returned to me within two days after your meeting with him.

Your help in making his visit a pleasant one will be appreciated.

DOP

Donald Palmer

Distribution:
- Gordon Moore
- Tom Sah
- Worden Waring

RECEIVED
DEC 10 1962
C. T. SAH

APPLICANT EVALUATION FORM

Applicant's name ____MEIERAN,________________Eugene____________________________
Last First Middle

Degree Ph.D. Metallurgy Expected February 1963 Date of Interview December 19, 1962

Please give us a brief statement regarding your evaluation of applicant's experience and technical competence

____

____

____

____

____

____

In your opinion, do you feel that applicant should be considered for employment with Fairchild: Definitely__________ Perhaps__________ No__________

If you do recommend him for employment, in what area(s) do you feel he could contribute the most:____

____

Any other comments you might wish to make concerning applicant:__________

____

____

____

____________________ ______________________________
Date Signature of Interviewer

(Please complete form and return to Don Palmer, Personnel, R&D Department, within two days after interview)

MEIERAN

FAIRCHILD SEMICONDUCTOR

PROFESSIONAL APPLICATION BLANK

Answer All Applicable Questions

NAME Last	First	Middle	Maiden	Soc. Security No.	Male	Female
MEIERAN	EUGENE	STUART		271-32-5880	X	

Address No. Street City Zone State	Home Phone No.	How Long At This Address?	Bus. Phone	May We Phone You There?
Rm 8-432 M I T CAMBRIDGE, MASSACHUSETTS	KI 78474		UN46700 EXT 3413	Yes ☒ No ☐

Position Desired	Date Available	Salary Expected
RESEARCH metallurgist	1963 ?	$ per

By Whom Were You Referred to Fairchild? MR WORDEN WARING

Any Relative Working at Fairchild Semiconductor? If Yes, Please Give Name ☐ Yes ☒ No

Have You Ever Been Employed by Fairchild Semiconductor or Other Division of Fairchild Camera and Instrument? Yes ☐ No ☒

If Yes, Where and When?

EDUCATION BACKGROUND

	Name and Address of School	Major and Minor	Letter Grade Average	Dates of Attendance	Diploma or Degrees	Why Did You Leave?
HIGH SCHOOL	CLEVELAND HEIGHTS HIGH CLEVE. HTS. 18, OHIO	SCIENCE	B+	1952-1955	DIPLOMA	GRADUATE
UNIVERSITY	PURDUE UNIVERSITY W. LAFAYETTE, INDIANA	METALLURGY	B+	1955-1959	B.S.	"
~~UNIVERSITY~~ GRADUATE SCHOOL	M I T CAMBRIDGE, MASS	"	B+	1959 —	S.M	STILL HERE
GRADUATE SCHOOL						
SPECIAL TRAINING						

PROFESSIONAL ACTIVITIES

List Memberships in Professional, Honorary and/or Engineering Societies

AIME, ASM, Tau Beta Pi (Engineering), Phi Lambda Upsilon (Chemistry), Sigma Gamma Epsilon (Metallurgy), Sigma Xi (Research), AEC Fellow 1959-1960 (MIT)

List Patents Applied for and/or Granted

List Publications Authored or Co-Authored

Use of the Reciprocal Lattice for the Determination of a New Pole Figure Technique.

In What Special Projects or Research Assignments Have You Participated? (Describe Specific Assignments)

EMPLOYMENT BACKGROUND

Complete information on all employment and periods of unemployment during last 10 years must be given. List present or most recent employer. Work back. Include periods of unemployment.

Company ATOMICS INTERNATIONAL div North American Aviation | Address De Soto Ave. Canoga Park, California | Type of Business Atomic Power Metallurgy Research | Telephone

YOUR JOB TITLE(S) Research Engineer | From Mo./Yr. 6/60 | To Mo./Yr. 9/60 | RATE OF PAY PER $610 ✓ Month ____ Week ~~$610~~ ____ Hour

____ | ____ | ____ | ____ Month ____ Week ____ Hour

DESCRIBE PRIMARY DUTIES: Phase diagrams of metal-gas system (exact detail classified)

What Did You Like Most? | What Did You Dislike?

How Many Employees Did You Supervise? 1 | What Were Their Job Titles? Technician

Your Supervisor's Name and Title Mr Don Atkins, Supervisor, Dept 773-35 | May We Contact Him or others in This Company for Reference? YES X NO

EMPLOYMENT BACKGROUND

Company GENERAL ELECTRIC ANP Division | Address Evendale, Ohio | Type of Business Nuclear Aircraft Engine Development | Telephone

YOUR JOB TITLE(S) Research Engineer | From Mo./Yr. 6/59 | To Mo./Yr. 9/59 | RATE OF PAY PER $790 Month ____ Week ____ Hour

____ | ____ | ____ | ____ Month ____ Week ____ Hour

DESCRIBE PRIMARY DUTIES: Develop high temperature corrosion resistant materials (classified)

What Did You Like Most? | What Did You Dislike?

How Many Employees Did You Supervise? 1 | What Were Their Job Titles? Technician

Your Supervisor's Name and Title Mr. Jim McGurty, Supervisor, Metallurgy Fuels & Materials | May We Contact Him or others in This Company for Reference? YES X NO

EMPLOYMENT BACKGROUND

Company	Address	Type of Business	Telephone
Thompson Pds. TAPCO Div.	Euclid Ave, Cleveland, Ohio	Air Craft parts Metallurgy research	

YOUR JOB TITLE(S)	From Mo./Yr.	To Mo./Yr.	RATE OF PAY PER Month	Week	Hour
Technician	6/58	9/57	$375		

DESCRIBE PRIMARY DUTIES: Metallurgy research - structure & properties of titanium alloys

What Did You Like Most?	What Did You Dislike?

How Many Employees Did You Supervise?	What Were Their Job Titles?
None	

Your Supervisor's Name and Title	May We Contact Him or others in This Company for Reference?	YES	NO
Dr. Al Nemy Research Metallurgist		X	

MILITARY SERVICE WITH U. S. ARMED FORCES

Branch of Service	Rank at Discharge	Date Entered	Date Discharged	Type of Discharge

Primary Duties	Schools Attended or Special Experience

Are You Receiving A Pension?	Selective Service Classification	Reserve Status
YES ☐ NO ☐		

CITIZENSHIP

(IF HIRED APPLICANTS MAY BE REQUIRED TO SUBMIT PROOF OF CITIZENSHIP)

Are You A Citizen of the U. S.? ☒ Yes ☐ No (If No, Please Answer The Following Questions)

		YES	NO
A.	HAVE YOU A LEGAL RIGHT TO REMAIN PERMANENTLY IN THE UNITED STATES?	☐	☐
B.	DO YOU INTEND TO REMAIN PERMANENTLY IN THE UNITED STATES?	☐	☐
C.	HAVE YOU APPLIED FOR NATURALIZATION PAPERS?	☐	☐
D.	HAVE YOU EVER BEEN ARRESTED OR INTERNED AS AN ENEMY ALIEN?	☐	☐

SECURITY CLEARANCE

Have You Ever Applied for Security Clearance?	If Yes, What Classification?	Agency	Current?
☒ YES ☐ NO	"Q"	AEC	No

Have You Ever Been Denied Security Clearance?	If, Yes, Explain Fully
YES ☐ NO ☒	

Do You Know of Any Reason Why You Might Be Denied Security Clearance?	If, Yes, Explain Fully
☐ YES ☒ NO	

PERSONAL DATA

Date of Birth	Height	Weight	Have You Any Physical Limitations?	If Yes, Please Describe Fully
12/23/37	5' 11"	185	☐ Yes ☒ No	

Have You Ever Been Convicted for Other Than Minor Traffic Violations?	If Yes, Explain Fully
☐ Yes ☒ No	

Color of Eyes	Color of Hair
Blue	Brown

MARITAL STATUS

Single ☐	Married ☒	Remarried ☐	Separated ☐	Divorced ☐	Widowed ☐
	How Long Just married	How Long	How Long	How Long	How Long

Is Your Spouse Employed?	YES	NO	If Yes, Name of Company	Kind of Work	Job Title
	X		Harvard University	Secretarial	Secretary

DEPENDENTS

NAME	Relationship	Age
Mrs. Rosalind Meieran	Wife	24

REFERENCE

PLEASE LIST AT LEAST TWO (2) PROFESSIONAL REFERENCES

NAME	Position	Employer	Address
Dr. Morris Cohen	Professor	MIT	MIT, Cambridge, Mass
Dr. David Thomas	"	"	"
Mr. Joseph Greenhut	Engineer	self	2569 Saybrook Rd. University Hts 18, Ohio
Prof R. Schuhmann	Professor	Purdue University	Metallurgy Dept Purdue University W. Lafayette Indiana

AFFIDAVIT

I expressly waive all provisions of law prohibiting any physician, person, hospital, or other institution that has or may hereafter attend or furnish me with treatment from disclosing to Fairchild any knowledge or information thereby acquired. Further, I agree to the performance of a medical examination by a company designated physician and understand that medical approval must be obtained before employment can be effected.

I authorize all schools which I attended and all previous employers to furnish to Fairchild my record, reason for leaving, and all information they may have concerning me, whether or not it is contained in their records. I hereby release them and Fairchild from all liability for any damage whatsoever arising therefrom.

I certify that I have never been a member of any organization that advocates or has advocated the overthrow of the constitutional government of the United States.

I agree to sign a contract of employment upon employment or at any time requested thereafter on the company's usual form and abide by the provisions thereof.

I understand that, in the event of my employment by Fairchild, I shall be subject to discharge if any of the information I have given in this application is false or if I have failed to give any material information herein requested.

1/24/67 — Date

Eugene S. Meieran — Usual Signature

INTERVIEWER'S COMMENTS

DATE

Job Title	Rate	Shift	Starting Date	Dept.	Section	For Dept.	For Personnel

FAIRCHILD
SEMICONDUCTOR CORPORATION

OUTGOING MESSAGE

( ) TWX (X) WUX DATE NOVEMBER 12, 1962

ADDRESSEE:	ORIGINATOR:
REGISTRAR MASSACHUSETTS INSTITUTE OF TECHNOLOGY CAMBRIDGE 39, MASSACHUSETTS	DONALD PALMER DEPT: PERSONNEL EXT: 301

MESSAGE INFORMATION:

MR. EUGENE S. MEIERAN BORN DECEMBER 23, 1937 INDICATES ON HIS EMPLOYMENT APPLICATION THAT HE EXPECTS TO RECEIVE HIS Ph.D. DEGREE IN METALLURGY APPROXIMATELY LATE 1962 OR EARLY 1963 STOP WOULD YOU PLEASE VERIFY THIS INFORMATION BY RETURN COLLECT WIRE STOP WOULD ALSO APPRECIATE BEING ADVISED HIS CLASS STANDING IF YOU RANK STUDENTS THIS MANNER STOP THIS INFORMATION WILL BE HELD STRICTEST CONFIDENCE STOP

DONALD PALMER

Eugene Stuart Meieran currently registered at MIT.
He expects to complete requirements for degree of
Doctor of Science in field of metallurgy in February '63.
Rank in class not available.

W. D. Wells
Associate Registrar

MESSAGE SENT:	MESSAGE NOT SENT BECAUSE:
MESSAGE No. ______ DATE ______ TIME ______ OPERATOR ______	

MORRIS COHEN
DEPARTMENT OF METALLURGY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
CAMBRIDGE 39, MASS.

27 November 1962

Mr. Donald Palmer, Personnel Manager
Fairchild Semiconductor Corporation
4001 Junipero Serra Boulevard
Palo Alto, California

Subject: Mr. Eugene S. Meieran

Dear Mr. Palmer:

In reply to your letter of November 12, I can recommend Eugene Meieran very highly for employment on your Technical Staff. Meieran is now completing his thesis for the Doctorate in Metallurgy at MIT, and he is giving a good account of himself. His work on electron microscopy and preferred orientations is first-class, requiring both experimental skill and fairly sophisticated interpretation.

Meieran knows how to keep his eye on the ball, and as a result he has made excellent progress in his graduate program. At first, he seemed to be disconcerted by the rapid pace here, but after a while he demonstrated that he could hold his own with the best of the graduate students here.

You will find that Meieran has drive, perseverance, and a sincere desire to find meaning in what he is doing. He knows how to design research projects and follow through. However, he is still a young man, and benefits from senior advice and encouragement from time-to-time.

Sincerely yours,

Morris Cohen

MC:m

DAVID A. THOMAS
DEPARTMENT OF METALLURGY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
CAMBRIDGE 39, MASS.

December 4, 1962

Mr. Donald Palmer
Personnel Manager
Fairchild Semiconductor Corp.
4001 Junipero Serra Blvd.
Palo Alto, California

Dear Mr. Palmer:

I am writing concerning the application of Mr. Eugene S. Meieran for employment with your organization. He has given my name as a reference.

Meieran has been carrying out his graduate work at MIT under my supervision since he arrived from Purdue in 1958. Meieran has a strong interest in x-ray diffraction, electron diffraction, experimental crystallography, and related fields. He has a particular knack for devising equipment to do experiments in these fields. His most recent experience has been with transmission electron microscopy of tungsten, which is closely associated with the diffraction problems that are of such interest to him. He has made significant contributions to our work in this area.

Meieran is also competent theoretically, but he is more reluctant to apply himself there than in experimental studies. However, he shows increasing interest in crossing the lines between experimental and theoretical work.

Meieran is an intense individual, occasionally to the irritation of others. However, he has worked in the electron microscopy laboratory quite successfully in the past year or two, and I think he appreciates the results of cooperation better than ever before.

Sincerely,

David A. Thomas

David A. Thomas,
Associate Professor of Metallurgy

DAT:mpp

FAIRCHILD SEMICONDUCTOR

Inter-Office Correspondence

RECEIVED
FEB 6 1963
GORDON E. MOORE

To: Paul Hill

From: Dick Robinson

cc: D. Yost
G. Moore ✓
C. Plough
Technical File (Mt.View)

February 5, 1963

Subject: Standard Masking, Micrologic

Project: No. 48 - Standard Masking Procedure, Micrologic

Object: Evaluate Standard Masking (30 cs. KPR) for Micrologic and Implement if feasible.

Summary: This report contains the results of comparison of production micrologic masking with standard masking by process development for the same micrologic patterns. The present production method was found to give superior pattern fidelity on the etched wafers.

Method: All pattern measurements were made with a calibrated filar eye piece at 500X. Resistor bar widths were measured at the bottom of the oxide cutout and at the center of the bar. The mask measurements were made for a previous report (Project No. 59 - Review of Mask Manufacturing Methods, December 14, 1962). The three largest wafers from each run were selected for comparison and all samples were from the center 10 patterns of row 13, µL Mask H-60-Y-3 (the row with three missing patterns). The runs for comparison were selected at random, the line runs from whatever was available on the date the measurements were made and the standard mask runs from four runs masked by Process Development.

Data: Nomenclature

$\bar{X}$ = mean of 10 measurements, mil.
s = sample standard deviation, mil.

Line Masks:

Resistor	$\bar{X}$	s	$\bar{X}$	s
1.	2.029	0.008	2.032	0.016
2.	2.038	0.008	2.031	0.012
3.	2.031	0.010	2.027	0.015

Process Dev. Mask:

Resistor	$\bar{X}$	s
1.	2.044	0.017
2.	2.044	0.023
3.	2.031	0.018

Line Masked Wafers:

Run No.	Resistor	$\bar{X}$	s	$\bar{X}$	s	$\bar{X}$	s
HY 237	1	2.003	0.034	1.888	0.036	1.974	0.043
(12-7-62)	2	2.022	0.027	1.917	0.044	2.006	0.027
	3	2.020	0.029	1.920	0.032	2.006	0.022
HY 272	1	1.947	0.028	1.923	0.036	1.929	0.032
(12-17-62)	2	1.965	0.018	1.940	0.038	1.946	0.037
	3	1.964	0.017	1.931	0.029	1.940	0.047

Standard Masked Wafers (Process Development):

Run No.	Resistor	$\bar{X}$	s	$\bar{X}$	s	$\bar{X}$	s
HY 245	1	1.668	0.085	1.808	0.035	1.826	0.044
(12-10-62)	2	1.708	0.086	1.815	0.041	1.833	0.040
	3	1.691	0.077	1.831	0.037	1.834	0.033
HY 245	1	1.892	0.026	1.852	0.031	1.854	0.043
(12-17-62)	2	1.923	0.025	1.887	0.037	1.884	0.044
	3	1.923	0.028	1.890	0.031	1.889	0.047

Analysis of Results:

The data show that standard masked wafer patterns are smaller than the specified 2.00 mil. by a greater amount than line masked wafers. This can be also seen by comparing mean mask size with mean etched image size:

	Mask	Image		Difference
Line Mask	2.030	1.958	=	0.072 mil.
Standard Mask	2.040	1.834	=	0.206 mil.

Conclusions and Recommendations:

1. The present micrologic process should be retained where etched pattern dimensions are critical (base, emitter, and oxide removal masks).
2. Standard masking could be used for isolation masks if pinhole reduction is required since image size is not as critical for these masks.

Dick Robinson

Dick Robinson
Process Development

DR:ch

Noyce meeting: 1/3/62

1. List of people
2. Write a yearly progress rept compared with goals.
3. Feb 1 meeting

Jan 7, 1963 – Monday Microcircuit Meeting (Last Dec 10)

Schultz, Ferguson, Seeds, Farris, Daniel, Moore

1. μL gate – epi
Mask ok
1st run looks ok (1 good wafer, 1 bad) – i.e., 1st two wafers
Bad spread on mandarel – 5–15 μ!

12–14 Ω $V_{CE SAT}$, ~15v isolation – which seems low.

2 other runs, 1 in emitter, 1 in base
2 wafers at dicing
~20 wafers in one run @ Au diffusion
1 run in emitter
1 run in base diffusion
flow behind that

Thru diesort
8
1/7
1/10
1/11
1/16

3. Sc – in Sb diffusion for 1st run (55×55 die)

The Ge mask is in with the wrong resistor size now. Plough is re-laying out the pads.

1. Presumably the "GY" X-stor masks for the ... have been stopped by Bay.

2. Bay has edited that 1 mil wire and 4.5 mil bonding pads will be used.

3.

Status of stuff:

μL I GY

G, S, + H runs in process
2 runs of G's in evaluation (Seeds)
$R_c = 650$
$R_c = 550$
Rest of masks stopped.

C. Plough doing the other epitaxial masks

INTERNAL CORRESPONDENCE

FAIRCHILD SEMICONDUCTOR

A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

TO: L. G. Reis

DATE: February 8, 1963

FROM: H. B. Grutchfield

CC: B. C. Knudson

SUBJECT: Results of Tests to Evaluate the Model Proposed to Explain "Secondary Breakdown" in Transistors

Purpose

To document the results of tests conducted to evaluate the model proposed to explain secondary breakdown in transistors.

Conclusions

The test results agree with the results predicted by considering a one-dimensional transistor model in which the V_{BE}, at any operating condition with a forward biased base-emitter diode, is assumed to vary in a random manner as a function of lateral displacement from a reference point on the junction.

Summary of Tests and Results

Six TC4016's were selected at random from a bucket of unclassified units. The units were checked for opens and shorts. However, the only criteria used to select the devices to be used was that each unit have an $LV_{CEO} \geq 80$ volts. No attempt was made to match h_{FE}'s or V_{BE}'s.

The units were then soldered into a 2" x 1" x 1/2" copper heat sink and wired for parallel operation. Each emitter was brought out separately so that a resistor could be connected in series with the individual emitters.

The thermal resistance of each individual transistor was measured in a heat dissipating bath biased at $V_{CB} = 10$ V and $I_E = 0.1$ A. Values were:

Unit No.	θ (°C/W)
1	39
2	37.4
3	37.4
4	39.8
5	40.5
6	35.4

The thermal resistance was then measured at a constant $I_E = 0.5$ A at several collector voltages on the paralleled devices; first with no resistor in the emitters, next with a one ohm resistor in each emitter, and finally with a 10 ohm resistor in each emitter. The results are plotted in Figure 1.

Next, the emitter current of each individual unit was measured, first with no resistor in the emitters and then with a 10 ohm resistor in each emitter. Again, the total $I_E = 0.5$ A. The results are plotted in Figure 2.

It can be seen, by comparing Figures 1 and 2, that the increase in thermal resistance with no resistor in the emitters is a result of current "hogging" by device #5. The cause of the high thermal resistance at low collector voltages with a 10 ohm resistor in each emitter can also be seen -- device #3 is "hogging".

Figure 3 shows the thermal resistance as a function of collector voltage at $I_E = 0.5$ A for a different group of six TC4016's mounted in an identical manner. The current would appear to be more evenly distributed in this group. (This group was destroyed before the current distribution could be measured.) Nevertheless, the effect of the stabilizing resistors can be clearly seen.

The secondary breakdown voltage of the unit depicted in Figures 1 and 2 was measured with and without the stabilizing resistors. The total emitter current was again 0.5 A. Secondary breakdown occurred at $V_{CB} = 20$ V with no emitter resistors; at $V_{CB} = 50$ V with a 10 ohm resistor in each emitter. The secondary breakdown voltage was also measured on each individual device at $I_E = 0.25$ A. With the exception of device #5, secondary breakdown occurred at a collector voltage of 26 V to slightly in excess of 30 V. Secondary breakdown occurred on device #5 at $V_{CB} = 18$ V.

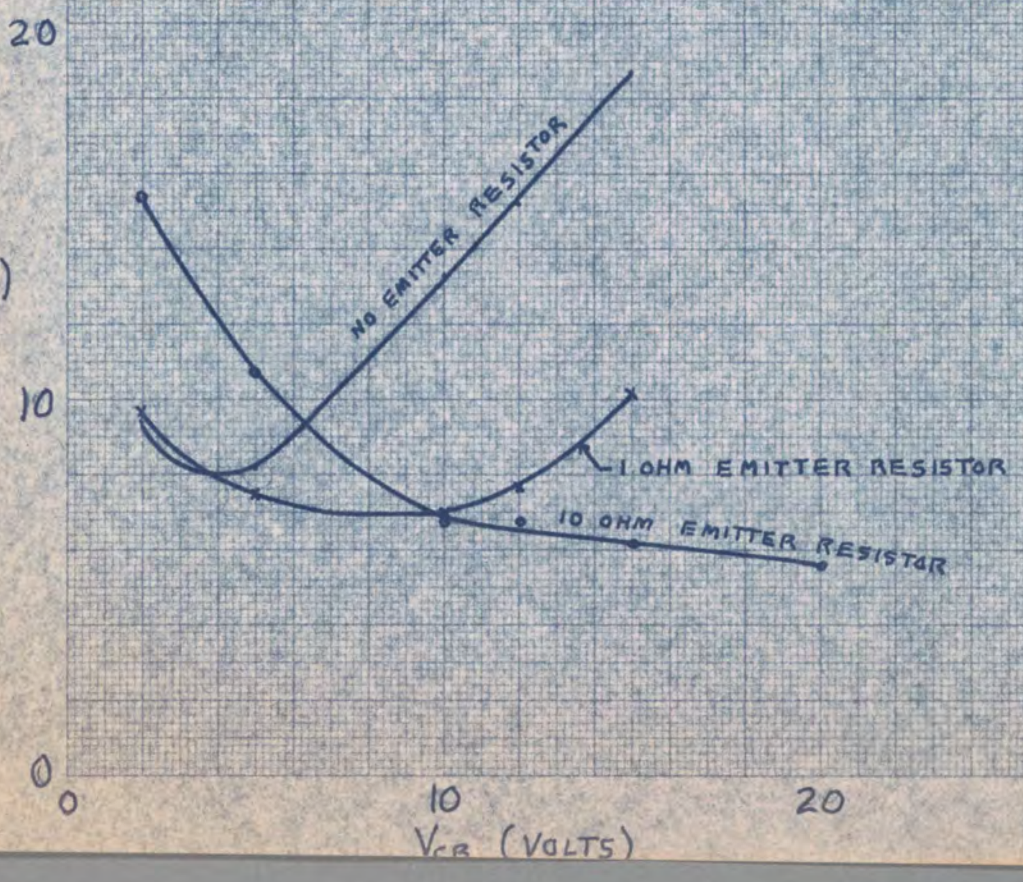
The secondary breakdown characteristics of the unit shown in Figures 1 and 2, without stabilizing resistors, is similar to some of the poorer 7000's and 6206's measured by the author. The characteristic of the unit shown in Figure 3 is similar to the better 6206's.

H. B. Crutchfield

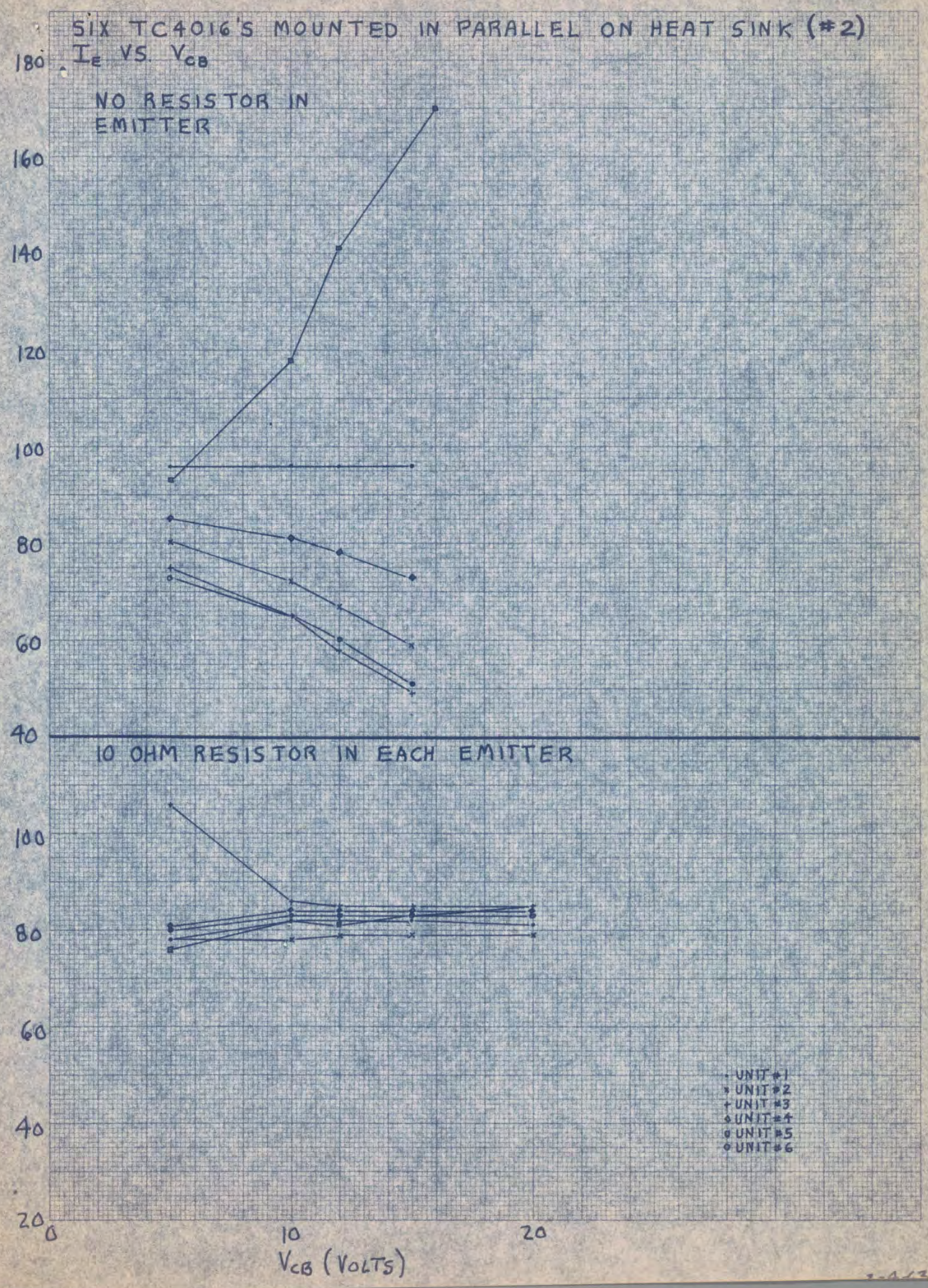
HBG:s

Fig. 1

SIX TC 4016'S MOUNTED IN PARALLEL ON HEAT SINK
THERMAL RESISTANCE IN TCE BATH, θ VS. V_{CB}
I_E = 0.5 A.
(UNIT #2)

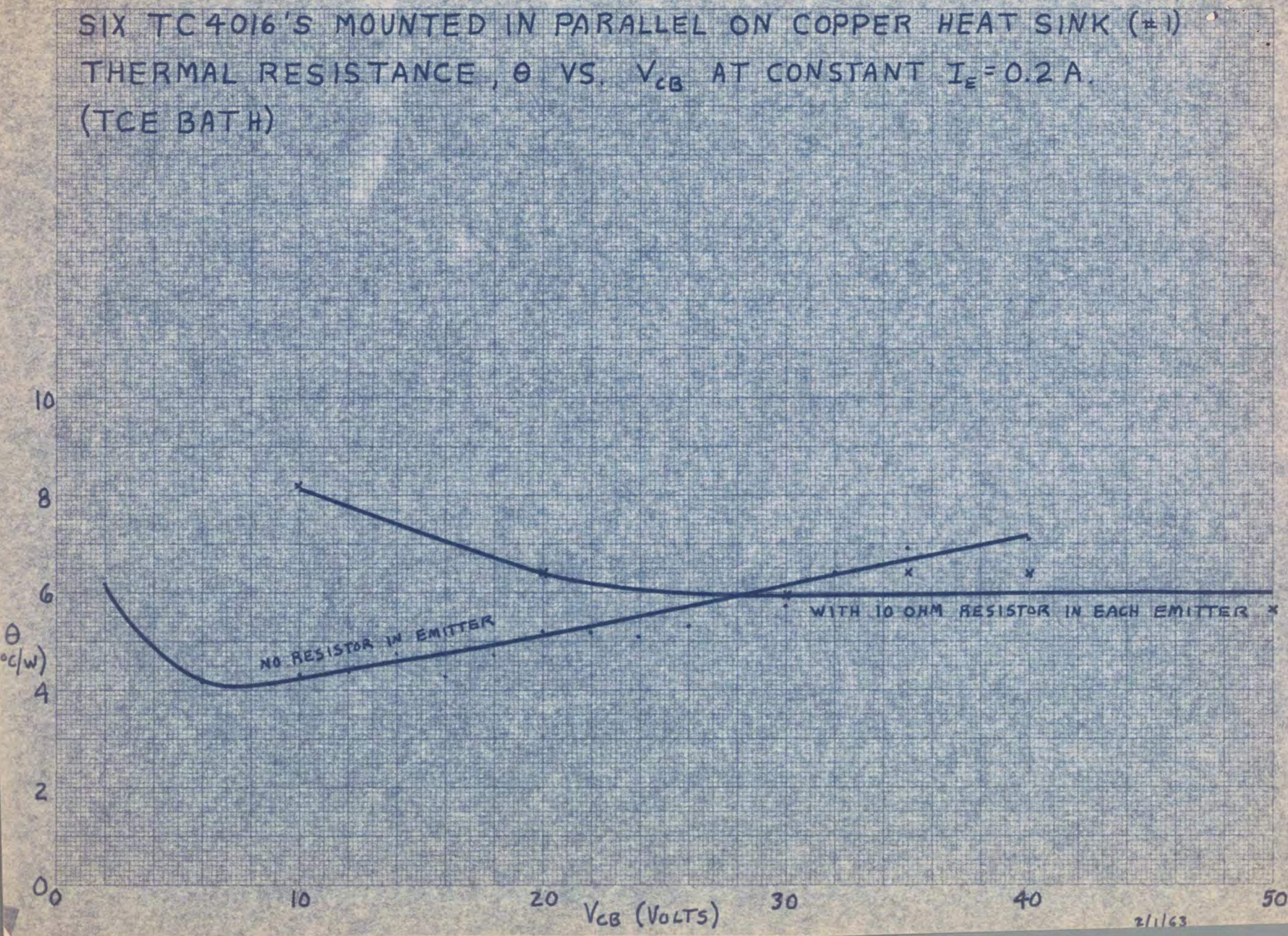


2-4-63

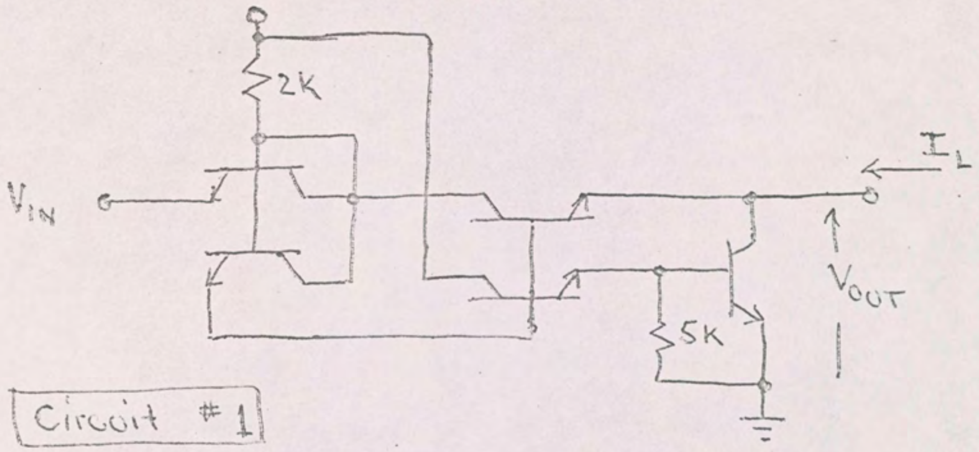

SIX TC4016'S MOUNTED IN PARALLEL ON HEAT SINK (#2)
IE VS. VCB
NO RESISTOR IN EMITTER
10 OHM RESISTOR IN EACH EMITTER
180
160
140
120
100
80
60
40
100
80
60
40
20
0
10
20
IE (mA)
IE (mA)
VCB (VOLTS)
UNIT #1
UNIT #2
UNIT #3
UNIT #4
UNIT #5
UNIT #6

NO. 340-MP DIETZGEN GRAPH PAPER MILLIMETER — EUGENE DIETZGEN CO. MADE IN U. S. A.

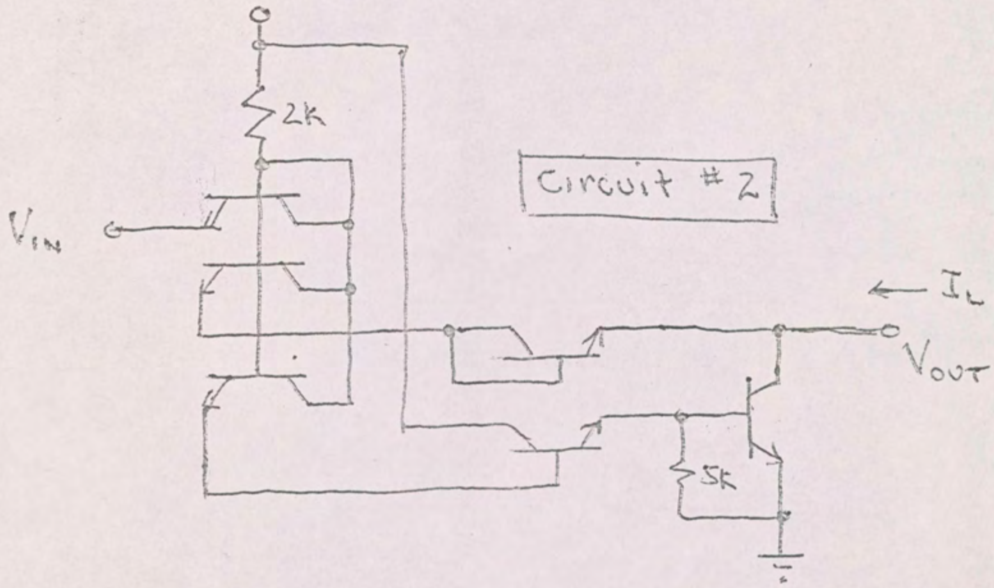
Fig. 3



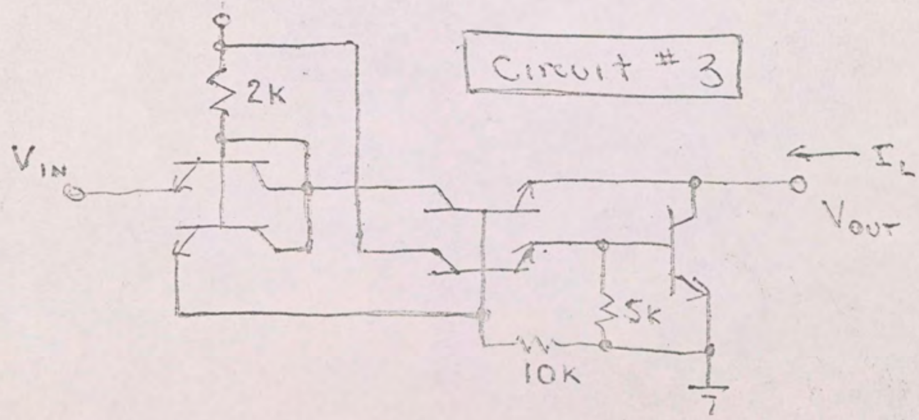
Integrated NAND Alternatives



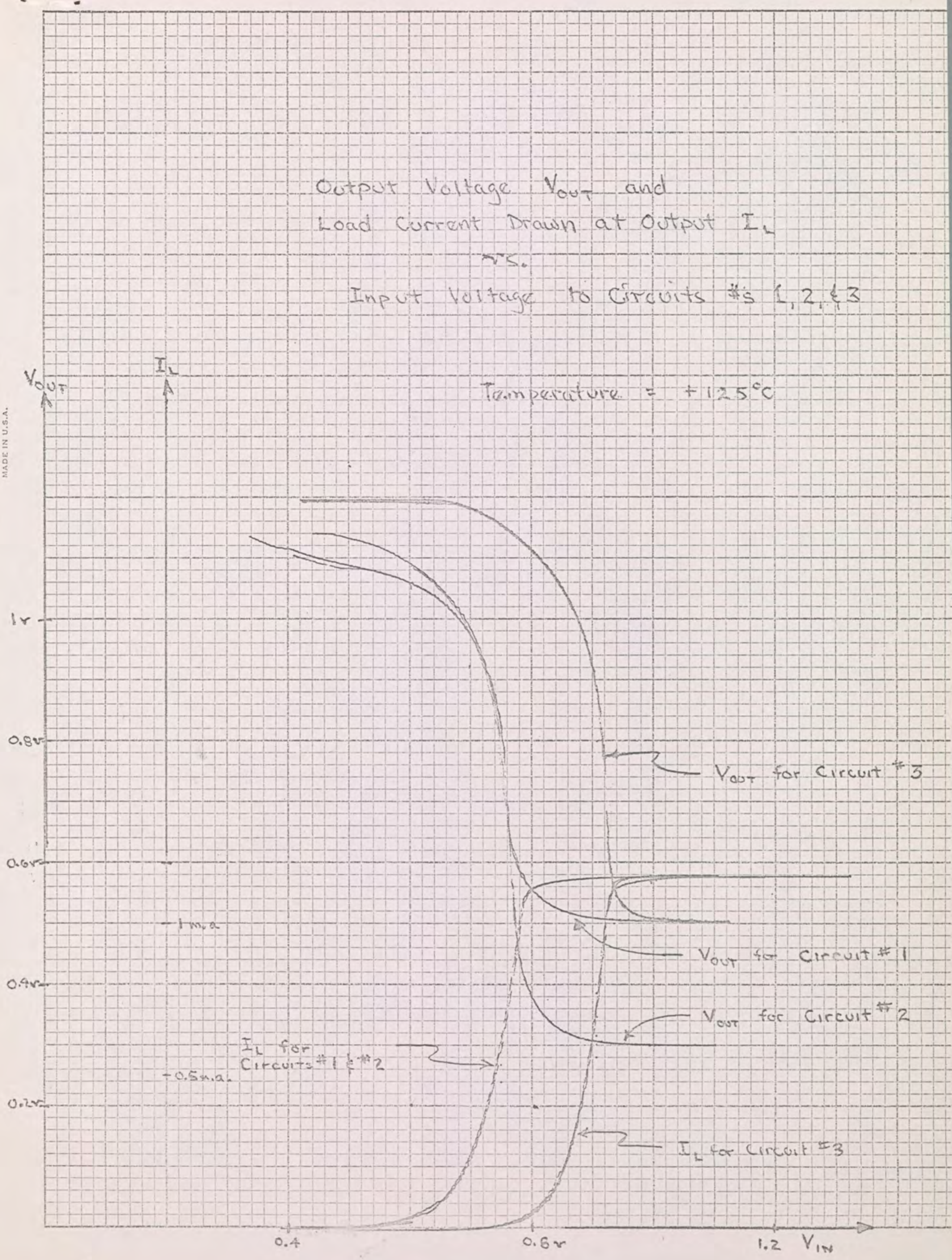
Circuit #1



Circuit #2



Circuit #3



Output Voltage V_OUT and
Load Current Drawn at Output I_L
vs.
Input Voltage to Circuits #s 1, 2, & 3
Temperature = +125°C
V_OUT
I_L
1v
0.8v
0.6v
0.4v
0.2v
1 m.a
0.5m.a.
V_OUT for Circuit #3
V_OUT for Circuit #1
V_OUT for Circuit #2
I_L for Circuits #1 & #2
I_L for Circuit #3
0.4
0.6v
1.2 V_IN

1/7, cont.

Decision on GY revisited:

ROBE Jan 8, 1963 (last 12/2/62)
See pp. 28

Flint, Sang, Ozmik, Cox, Brown, Fok, Moore, Hill, Spink, Yost

1. Cr masks

Wafer flattening problems not solved on large geometry.
No masks for small yet.

We will supply a Cr small geometry for a master.

Gene still fighting problems in film. He is confident.

1. Should we try larger coating.

2. What about the halo effect?

3. What about 6126 process?

2. "Pipe" problems

a. Original oxide thickness appears to raise test 70 yield. - 80% @ 6 pings vs 65 @ 4

b. More oxide at base diffusion (std original) looks better. 78% on thick vs 57% on thin

c. Sharper gradient at step helps.

d. It seems to help to do O_2 ox first then H_2O on base.

1) A split test to look at the effect of all of these on die sort yield is being started. There is a 6-7 week cycle time in regular production line.

2) Re-do experiment c̄ a larger sample.

A pilot line on the 4200 c̄ minimum handling is running (c̄ good preliminary results)

SP v. Flint — No P before oxidation or after oxidation
but on same wafers after B-diffusion we get them!

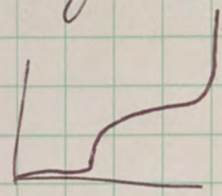
On some older mesa pipes we have no P and possibly a marked drop in Si.

56-800

Phil Flint will look for P into high ρ N by stacks.

 PNP reliability meeting – Mtn View. (Everybody but sales)

1 month 4511 @ 200°C, 10V – just about every unit failed – channels



3511

∴ looked at all PNP

4511 & 1772 looked bad

everything looked good 1746, 3511,

If stored @ 200°, they will come back.

Epitaxial Meeting 1/15/63

Shroeder
Yim
Cole
Moore

New reactor:

Only 1341 will accept it - up to 20% of total
None is being supplied now because Materials wants to wait until it looks good.
It still has a lot of bugs. Needs shop priority
Hope to supply material again by about the end of this week.

Material problems:

1. Surface appearance.

Data shows that there is more wafer-to-wafer transfer for As over Sb.

It looks to me like min possible time to switch:
1 week to start 1341 material
4 " to get data from them
then they want samples
4 " to give samples
4 " to get evaluation
13 weeks - to change

Agenda items.

1. New reactor problems
2. Substrates.
3. Group flash data
4. Large wafer mandrels - out of system

G.M. - Call Spark!!

16 weeks of substrates (small) in inventory
6-8 weeks delivery on flanges & mandrels for the big system.
What about junking these for large or running them.

Large Mandrels are \$50 ea @ 20, \$100 ea for 2. We will split an order for 20.

Large still is ~\$2500 and 1 mo to set up.

Diamond c̄ vapor etch looks good.

→ R&D will check out the wafers on devices

On substrates:
from junction

Monsanto	50%	bad (2 wafers ea)
CP-6	60%	
CP-8	80%	

HCl etched.

→ Hank will report a re-do to check substrate

Next meeting scheduled in 4 weeks. Moore call in 2.

 Metallization – Ag-Cr

Process

600°C substrates @ 10^{-4}, start Cr evap
Shut off substrate heater.
When Cr ~~[illegible]~~ is about gone start Ag.

No subsequent alloy cycle.

We have from Philco
1 wafer from Philco
some small geometry units – call Lou.
some more will come.
we are sending 20 G wafers for Philco to metallize.

We have done:

G's, 1340, ~~1321~~ 1211's

Inverted set up.
Somewhat lower substrate T

Maurice thinks there is no proven reason for getting chrome resistance now.

Being done:

1. Make ~500 units (G's) then. These will be put on the life tests shown in the attached memo. Yield data also to be collected during ~~[illegible]~~ assembly.
Units by 1/28 out/pwnt, 25 days to 250 hr data, + 6 weeks to end of test.
2. Small geometry – It is not clear that we have all bases covered. – Smaller or Senter?
3. M.D. will check out Au necessary for chrome
4. 42~~00~~'s – we will make some.

Data on ~6 units, 300°C storage – remained good
centrifuge – all ok – 2N2651 (like 1321)
1 mil. Au ball.

Ours would have shorted in an

On 1/22/63 I looked at Philco data on 100 units for 2000 hrs @ 300°C. Bonds looked great, but there was some VBE problem.

INTER-DEPARTMENTAL CORRESPONDENCE

FAIRCHILD SEMICONDUCTOR CORPORATION

TO: Don Farina CC: DATE: 1/18/63

SUBJECT: FROM: Gordon E. Moore

Please fill in your shcedule for the following and give it to me (leave with Helen) by 12:00 today:

1. Mask layouts for Micrologic elements to Sam

	My original date to be beaten	Your date as of now
G	This week	Yesterday
H	Today	Today
C	Next Wednesday	Next Tuesday (1/22/63)
B	Next Friday	Next Friday (1/25/63)
F	One week after the H (also 4 input G & (2) 2 input G alt.)	1/29/63

2. When will S's be thru -- please give best guess.

	Die sort-1st units	rest of run	evaluation
1st run	Wed.-Thurs (1/23 - 24)	1/25	1/31 no test spec
2nd run	1/31/63	2/1	2/8
3rd-5th	2/4 (3rd run) 2/8 (5th run)	2/5 - 2/8	2/12 - 2/15

Thanks.

Gordon

G.E.M./ll

FORM S120

INTERNAL CORRESPONDENCE

FAIRCHILD SEMICONDUCTOR

A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

TO: G. E. Moore ✓

DATE: January 17, 1963

FROM: J. P. Ferguson

CC: V. Grinich, C. Sporck, D. Farina, C. Plough, D. Cole

SUBJECT: Material Requirements for Epitaxial μL

The following schedule comprises the R&D contribution to the supply of material for the epitaxial micrologic evaluation:

	Week Beginning				
Wafers/week	1/28	2/4	2/11	2/18	
Sb & Epitaxy at R&D	75	75	75	75	Continue until no longer needed
Sb at R&D, Epitaxy at Stierlin Rd.	75	150	150	150	Continue until no longer needed

At present, the only pre-dep mask available is that of the S element. Hence, all of the material until about 2/4 will be for this element. After that, the material will be split as pre-dep masks for the other elements become available so that units of each element type will be available for characterization as soon as possible.

C. Plough plans on having his Sb furnace in operation by 2/1/63. At that time he will begin supplying wafers to Stierlin Road.

The material specification is as follows:

Wafer Size	1-1/4" max.
Wafer Thickness	180-220 μ
Substrate Resistivity	3-6Ω - cm "P" type
Layer Thickness	10μ + 2
Layer Resistivity	.3 - .6 Ω cm "N" type
Sb pre-dep V/I	$\leq$ 4 Ω/□

It is most important that all the material used meets these specifications since undue variations in Sb pre-dep V/I, layer thickness and layer resistivity will significantly affect the electrical specifications which may be guaranteed.

Phil Ferg

S-184

Micro-ckty "policy" meeting - 1/18/63

Beg Sprk Mgr — Finish More

Action from last week:

1. Eq. on the blast has been ~~ordered~~ slated - blanket PBA to issue
2. Lonnie has been assigned to do
3. On metal
   1. Run glass to get the
   2. Stick a centrifuge in after 250 hrs
   3. Examine situation @ 250 hrs - about Feb 25.
4. Check on Au bond on flat package

Jan 18, 1963 Meeting concerning something on μL products

Sprak, Talbert, Plough, Gyle, Schultz, Seeds, Graham, Phelps, Moore, Stein, Nozel, Farina, Ferguson, Craig, Berg

1. Data on epi
2. Data on G4 (GB)
3. Any other discussion of this.
4. Be sure that the mask cross-check is made

Ron Farina:

4 runs made to date — one only canned
Of the good wafers, leakage then isolation was good
$V_{CE(sat)}$ ran 15-20Ω typical
Caution problem of evaluating for in/out c̄ units of only 1 mmo
These will require a complete spec change to get yield on V_{BE}.

UGH →

On the 2,3&4th runs we have some channel problems. These channels appeared during metallization. Before metallization things looked great.

Yield data on GB — It was to be a direct plug in replacement, Internal tests for correlation needed changing

7 runs out, 5 had high resistors
other two had base doping right, but some contact problem
∴ (1) only 1 run that was good.
Should give a 40% yield to A spec on gates if tested only at room T.
higher if tested at extremes

All masks shall be designed for fixed base V/I (≈27.5Ω?)

Conclusion on GB.

1. Run c̄ present GB mask and Seeds prelim. spec
2. Change mask on base resistor - Plough

Ref. p. 61

F - Feasibility Samples
D - Design Samples
R - Reproducibility Samples
T - Transfer

HIGH FREQUENCY PROJECT PLANS

PROJECT	GOAL	1963										
		F	M	A	M	J	J	A	S	O	N	D
SATURATING SWITCHES:												
1. 1200°C gold with diffused emitter-NPN	$\tau_s \leqq 2$ nsec.			F								
2. Heavily doped substrate, epitaxially grown base												
a. NPN	$\tau_s \leqq 2$ nsec.		F									
b. PNP	$\tau_s \leqq 20$ nsec.											
3. Inverted structure NPN	$\tau_s \leqq 2$ nsec.			F								
4. CDC, 2 stripe, three input gate, nichrome resistors optional	Sat. and non-sat.		F									
5. Minimum τ_s PNP, reverse biased junctions	$\tau_s \leq 20$ nsec.			F								
6. One ampere ~~core~~ film driver	4011 performance		(F)→		(D)→		(T)→					
7. Other impurities on epi. substrates												
R.F. TRANSISTORS AND DIODES:												
1. Straight size reduction, majority base, one device	.1 mil stripes and spacing							F				D
2. High f_T device (Sandia contract)	2-3 kmc.											
a. All diffused					F							
b. Surface Barrier emitter							F					
3. FT-0006 aggregate	2.5 watt at 500 mc				D		R		T			
4. FT-0007 aggregate	5.0 watt at 500 mc						D		R		T	
5. Harmonic generation diodes	Misc. geometries and structures											
a. FD-7 w-w/o gold, different layer thicknesses			F									
b. FD-6 w-w/o gold, different layer thicknesses			F									
LOW CURRENT DEVICES (LOW NOISE):												
1. Inverted NPN/PNP	$h_{FE} \geq 10$ at 1 na				F							
2. Guard ring structure	$h_{FE} \geq 10$ at 1 na				F							

PROJECT	GOAL	1963 F	M	A	M	J	J	A	S	O	N	D
CHARACTERIZATION:												
1. Stripline		—	—	—	→							
2. Aggregate interconnection inductance		—	→									
3. Co-axial		—	—	—	—	—	→					
4. Aggregates in BeO power package			—	→								

2σ in ±15% on

10 - 90% ±15% on a run

Peak in ± 10%

Jan 23, 1963 High frequency devices Project Review

So
Casso
Ferguson
Grinich
Tripp
G. Parker

Sat switches:

1. Work on how to get to ~~[illegible]~~ low storage NPN logic - (needs invention)

2. Work toward faster PNP - looks possible

3. Develop film driver - fairly straight forward

4. CDC gate - straight forward.

R.F. Transistors and diodes:

1. The 0.1 mil test vehicle 0004.

2. High f_T device for Sandia

3. High power, r.f. device — what should we do?

Back-up work needed:

1. Upside down assembly techniques

2. Other impurities

3.

Discrete chip [illegible]

1. Test vehicle - a wide band ~~[illegible]~~ direct coupled amplifier. S of A [illegible].

Schedule & Priority
Small geometry, cont.

Priority

1. Sat switches
   a) NPN next generation — ~~Design~~ Data by Apr. 30
   b) PNP $\tau_s \sim 20$ ns (big step) — Design samples by May 31
   c) CDC triplet
   d) [illegible] driver

2. Low current - low noise

3. Wide band D-C coupled amp (separate dep)

4. R.F transistors
   a) [illegible]
   b) 0.1 mil Volatile
   c) Power RF
   d) μ wave diode

μ ckty coordinatn 1/24/63

G.B - all masks laid out G, B S+H masks made
no possible change on S+H to drop r_b'

∴ It looks like S+H must be re-done, if this is the case, then G must be re-done.

Acc. to Bob Graham, he would rather stay with the fallout for I_A because that he thinks he can sell lower fan-out "A" units.

Action:

The sample of 50 units from each of 11 runs will be
in 1 week < measured to "A" spec, "A" spec but fan-out of 4 with correlated test
and again to A spec and A-4 by temp extremes measurements
Also for B-units
In addition we want reasons for complete rejects.

in 1 week Plough will present resistor and beta spread data.

As soon as possible Bob Schultz will get yield on what would happen if we did not insist on compatibility by paralleling old μL c GB's.

Farina will run impedance plot on a sample of categ. A - correlated
A-4 "
A @ temp

Agree: on on data re: a spread we take 10-90%.

No masks changes on the GB.

Epitaxial will run with its present bar resistors.

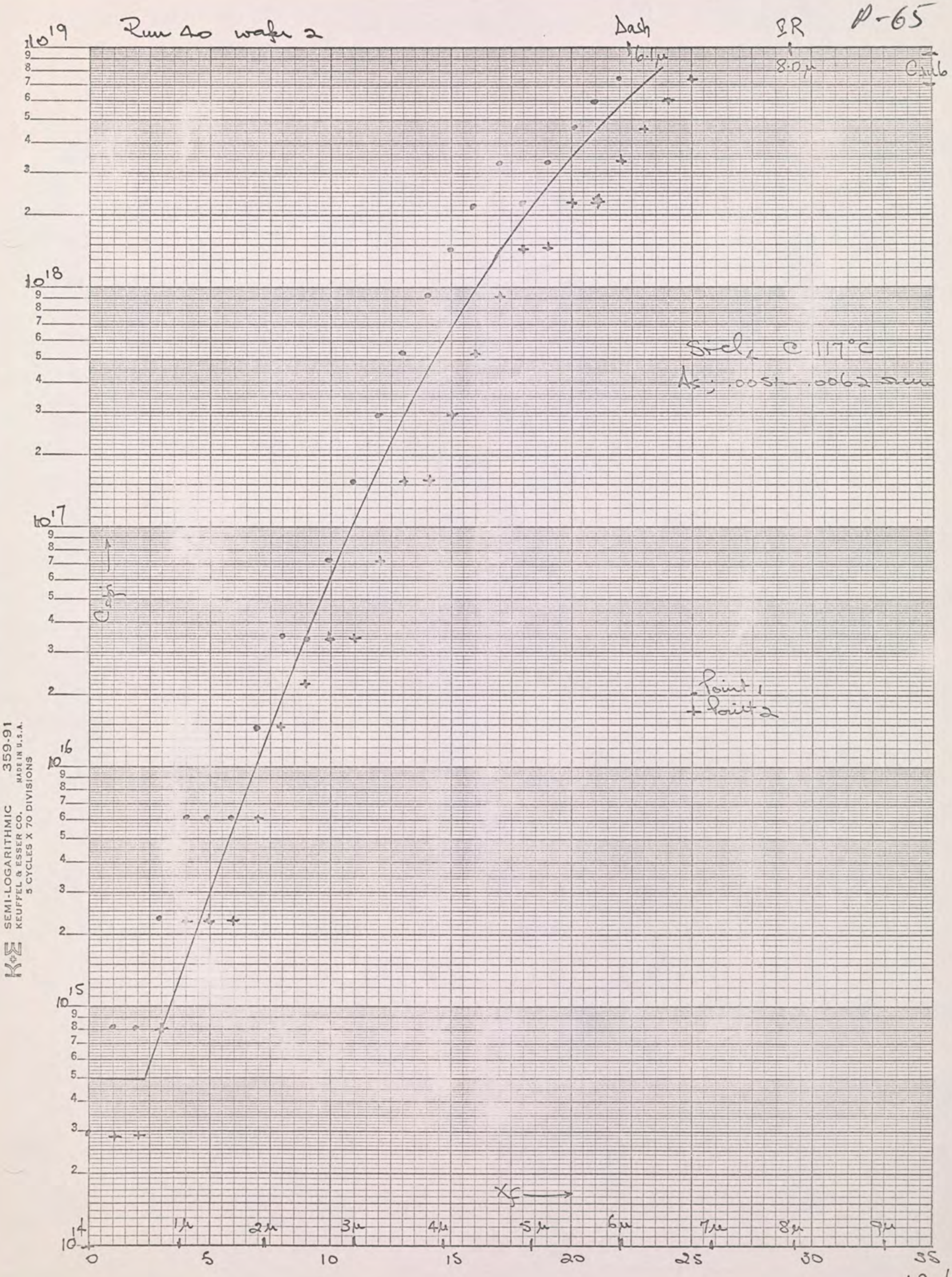
Section Meeting Jan 24, 1963

Blomo
Van Ness
Fohr

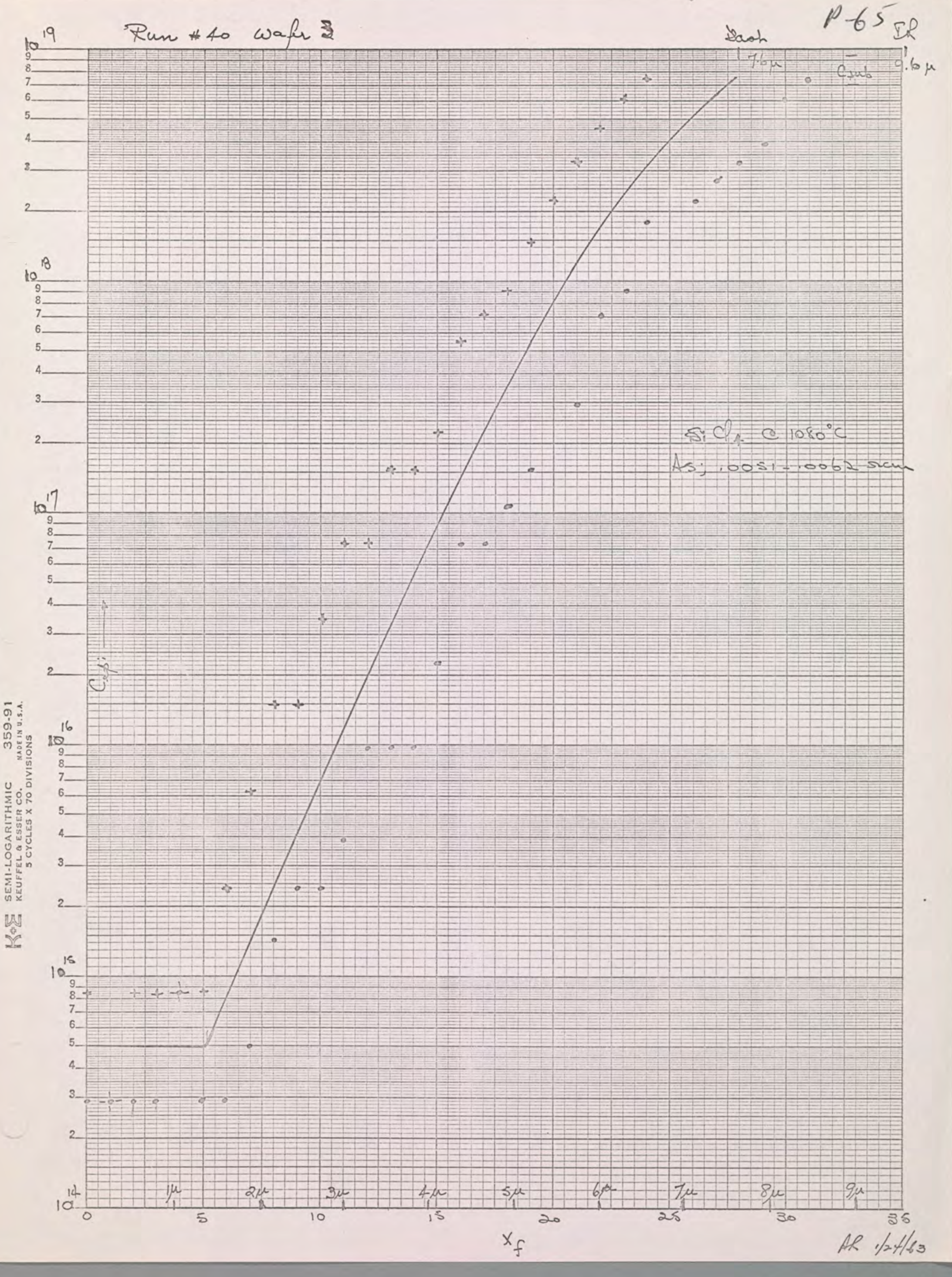
Mask making

Van feels that copy camera will do the memory array job. He will do the test job.

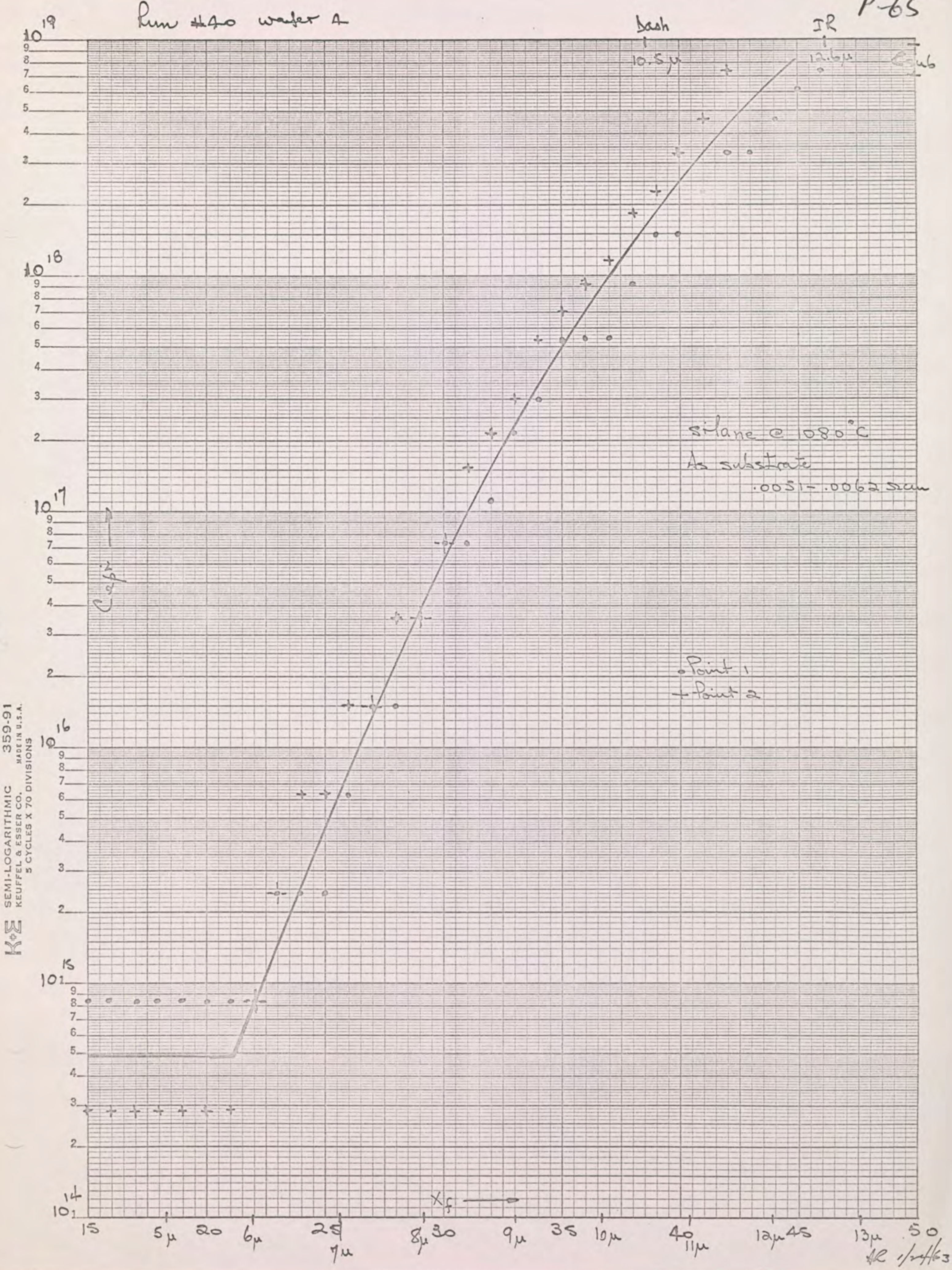
Chrome masks


Run 40 wafer 2
Dash
6.1μ
IR
8.0μ
C in 6
SiCl4 @ 1170°C
As; .0051 - .0062 mm
· Point 1
+ Point 2
C
Xj →
1μ
2μ
3μ
4μ
5μ
6μ
7μ
8μ
9μ
0
5
10
15
20
25
30
35
SEMI-LOGARITHMIC 359-91
KEUFFEL & ESSER CO. MADE IN U.S.A.
5 CYCLES X 70 DIVISIONS

AR 1/24/63


P-65
Run #40 wafer 3
Dash
7.6μ
9.6μ
C sub
SiCl4 @ 1080°C
As; .0051 - .0062 Ωcm
C epi
X f
1μ 2μ 3μ 4μ 5μ 6μ 7μ 8μ 9μ
0 5 10 15 20 25 30 35
10^19 10^18 10^17 10^16 10^15 10^14
AR 1/24/63
K&E SEMI-LOGARITHMIC 359-91
KEUFFEL & ESSER CO. MADE IN U.S.A.
5 CYCLES X 70 DIVISIONS

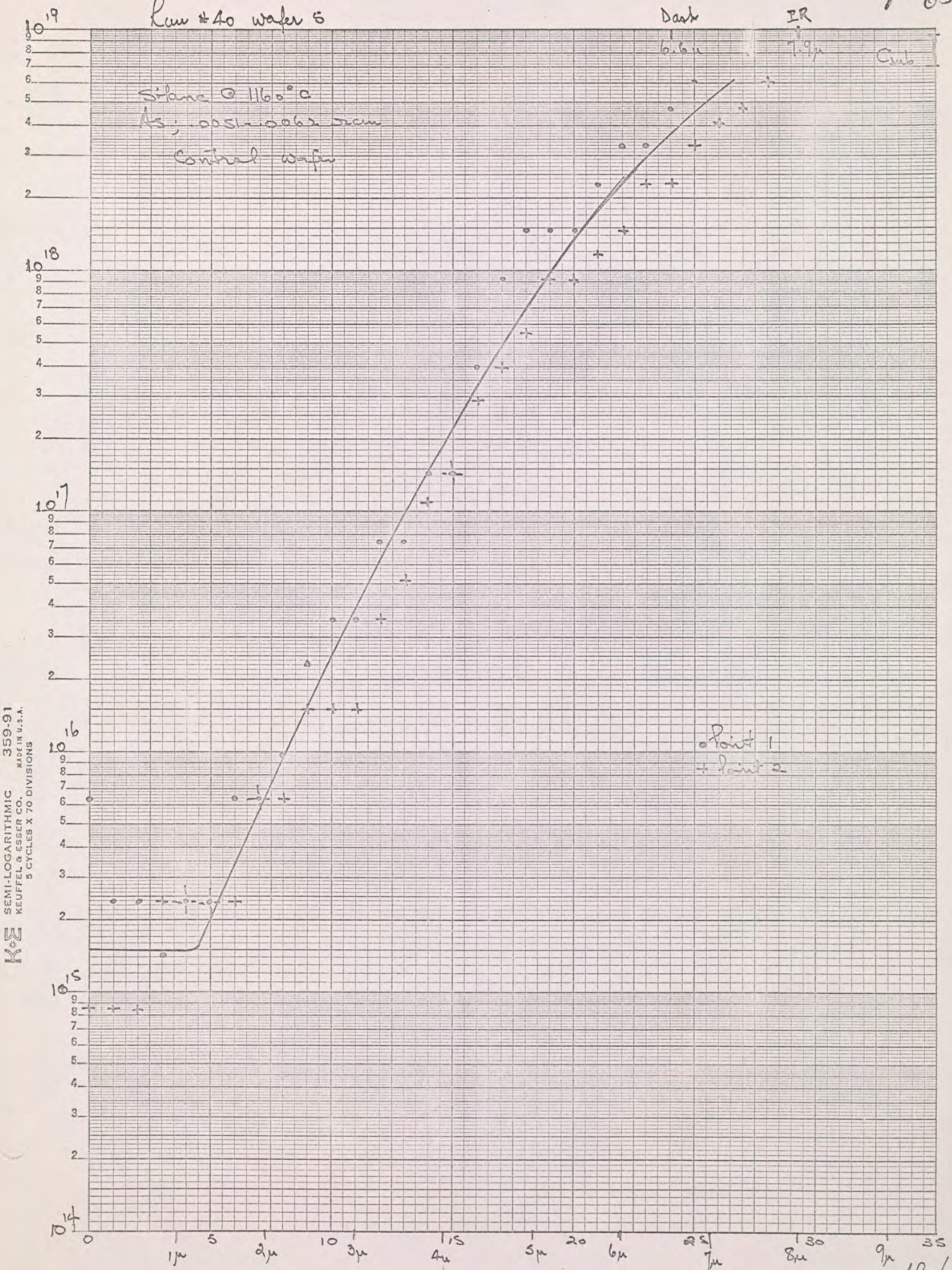
P-65



Run #40 wafer 4
Dash
10.5μ
IR
12.6μ
C_{sub}
10^{19}
10^{18}
10^{17}
10^{16}
10^{15}
10^{14}
silane @ 1080°C
As substrate
.0051-.0062 Ωcm
∘ Point 1
+ Point 2
C_{epi}
X_f
15
5μ
20
6μ
25
7μ
8μ
30
9μ
35
10μ
40
11μ
12μ
45
13μ
50
SEMI-LOGARITHMIC 359-91
KEUFFEL & ESSER CO. MADE IN U.S.A.
5 CYCLES X 70 DIVISIONS

AR 1/24/63

P-65


Run #40 wafer 5
Silane @ 1160°C
As; .0051-.0062 ncm
Control wafer
Dash
6.6μ
IR
7.9μ
Cub
o Point 1
+ Point 2
1μ
2μ
3μ
4μ
5μ
6μ
7μ
8μ
9μ
K+E SEMI-LOGARITHMIC 359-91
KEUFFEL & ESSER CO. MADE IN U.S.A.
5 CYCLES X 70 DIVISIONS

AR 1/23/63

Epitaxial Project Review 1/25/63

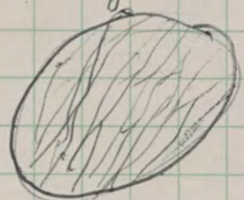
Barry, Roder, Wrigten, Yim, [illegible], Sah, Allen

Barry on Surface preparation:

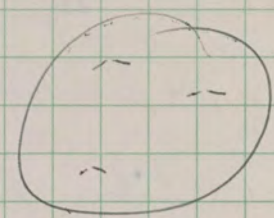
Sawed, lapped + stages of polishing
replicated and electron micrographed

There are still the little bumps (or pits?) that carry across everything

Looking at Sterling Rd material after vapor etch it is all covered c seam



is clean except for



+ ~~after~~ their growth.

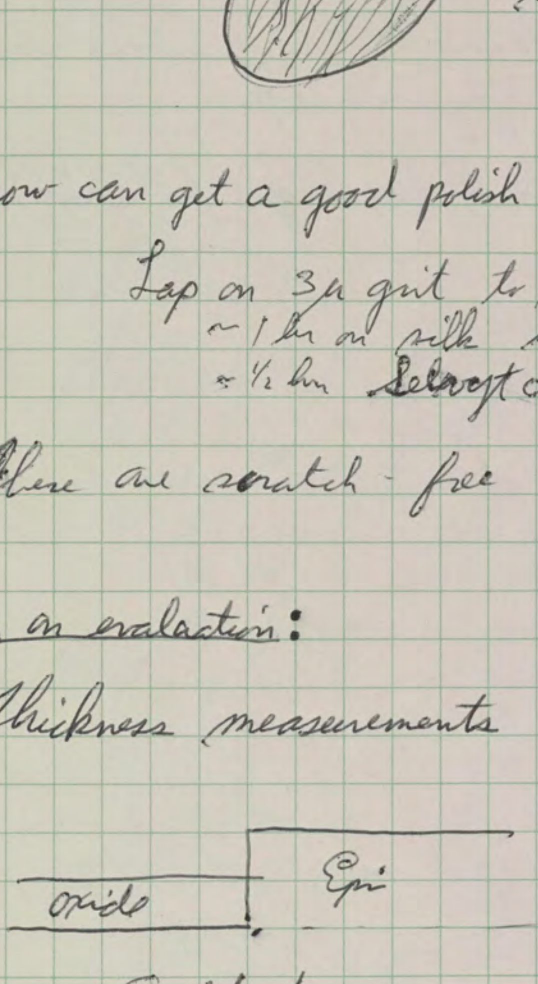
We now can get a good polish on Si

Lap on 3μ grit to remove 10μ/min for several min to get good and flat
~1 hr on silk with CeO
~1/2 hr ~~Selvyt~~ cloth with CeO or ZrO_2 — 30μ total removed

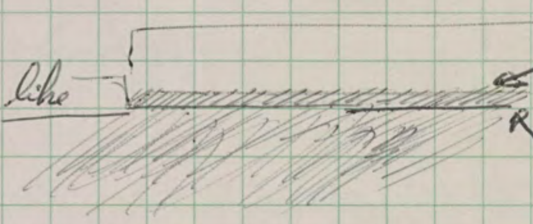
These are scratch-free to 400X light and dark field.

Roder on evaluation:

1. Thickness measurements



stain looked like



The IR "always" reads thicker even than one gets by proper interpretation of the dash etch stain.

Runs were made with $SiHCl_3$ + $SiCl_4$ at 1117 and 1080° and up to 1160°. We get identical gradients over about 5μ length.

 Epitaxial, cont - afternoon

It looks like the profile is error function. The Sb on one sample is in fair agreement $\bar{c}$ only solid state diffusion.

On the Sb vs As exp.

As .006 10μ

Sb .01 20μ

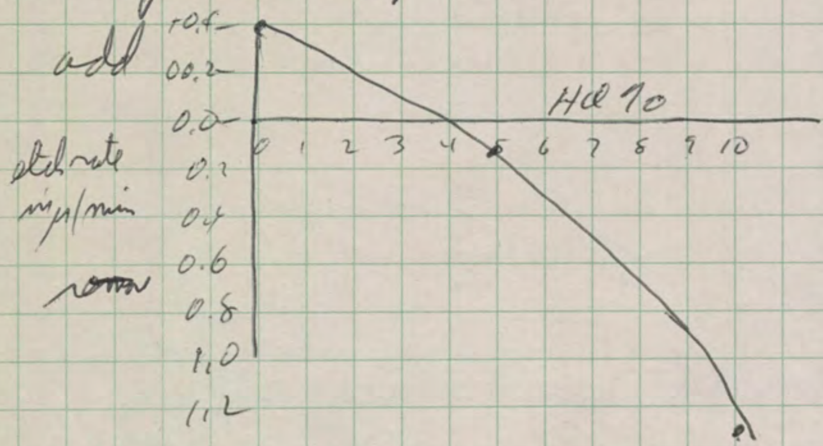
Confirm the dopant by chem analysis

The grown film will be high resistivity n and p.

One of the p-type will be used for Hall mobility. - Otto Leistiko

< This will be done in ~3 weeks.

Yinn on vapor etch



Packaging Project Review 1/25/63

Kobell, Sarbeck, Perkins, Brown, Blank, Ferguson, ?, Fagin, Weiss, Duquid, Stewart

1. Power – No work planned beyond where we are

2. High frequency – Strip line looks better than the co-ax.

3. TO-18 glass as a back-up for Hong Kong. This is necessary because they use a glass multiform which breaks upon spreading to TO-5.

4. Mtn View is completely over to their own flat package. (Special products is doing something shaky on using epoxy over non devitrified glass.

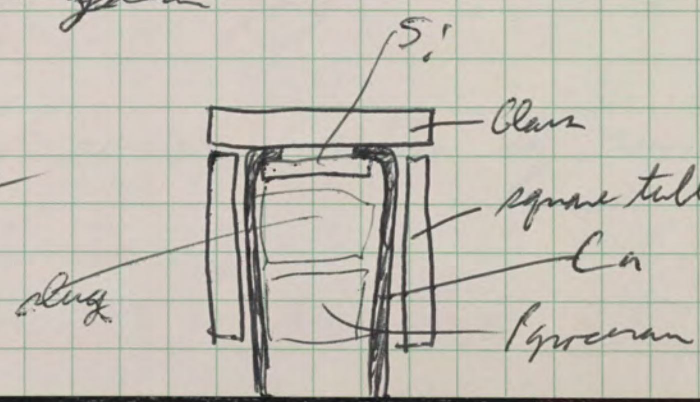
5. Metallization
   a) Silk screen
   b) Plate & etch

6. Base Assembly eliminating the little wires and/or a flexible chip assembly.
   Problems: (for face down)
   1. Contact area build-up
   2. Insulator over device
   3. Fine line patterns
   4. Joining of contact to substrate
   Finer grained summary of the face down

Brown & Ferg – giving them to try to put a ball & preform right side up assembly.
   a) Au balls
   b) Ag pads
   c) Coined preform

1st priority is solid package c̄ no separate little wires
2nd is separate chip assembly
3rd is assembly of packages to system

7. We have agreed on a unified approach to the YP-3 package



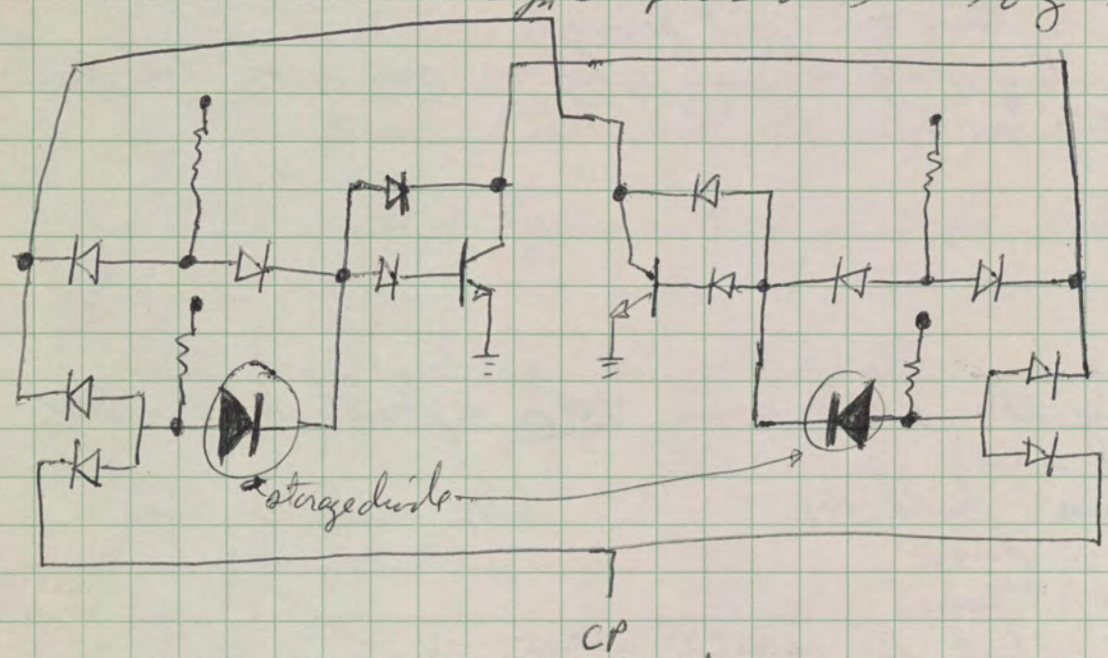
 Monday policy meeting 1/28/63 Seeds, Schultz, Farina, Thirkell, Moore, Fagan, O'Shea

CML - Seeds has the test vehicle laid out - a circulating form bit-~~serial~~ multiplier. It uses 108 G.F.'s.

Nothing else to do until the elements come out

Seeds will write up design.

New "R" element design: This is the long-missing NAND Binary



The test vehicle should be a storage diode and ~~as~~ fast are on the same chip.

Anodic oxide project review 1/28/63

Atriel	Carlson
Sah	Lewis
Grinich	Duffick
Davis	Dyke
Nowlan	Orsnik

The channel problem:

Lewis: Literature on heat treatment of O-containing material.

The channel fits the temp. dependence.

Lewis blames channels on the oxide states within the Si. It disappears upon F.

There is a geometry effect. This will be checked out.
(2 mil spaced devices gave channels. Wide ones didn't)

Proposed experiments to distinguish mechanism:

1. Strip & recoat
" " , etch & recoat.

My proposals: (neither conclusive).

1. Try F^- ions on high ρ n

2. Measure channels vs ρ-doping - high ρ should have lower channel.

We have no experiments to distinguish between the two proposed mechanisms.

PNP channel problem & anodic oxide.

Len Carlson:
1. After initial oxide by anodic — all groups had channels.
2. Reoxidized after diffusion — units being canned.
Data will start coming out soon.
Life data on a) Power aging
b)

(We can strip and re-grow oxides by anodic, pyrolytic or thermal.)

 Anodic oxide, con't

On anodic FET's :

Lewis says that they are stable at 300°C storage as not for thermal.
4500 type Inman says that the units he has are higher on anodic I_CBO, but are not changing so much.

The program :

1. Grind out PNP's to see what happens.
2. ? ~ SiO

Other items :

1. There is a reduction of pipes on SCR's with original anodic oxide. This is pipes defined as places where boron penetrates. – Len Ornika data.

2. Being tried to re-oxidize p-slots

3. " tried for 4200 (Bill O'Keefe)

4. tried for some of the transducer stuff

5. Capacitors – Price.

GPM 1/25/63

Mcktry Sanity summary:

Definitions

Compatability:

The new ckts can be plugged into a system made with the old units in any combination and the ~~circuits will~~ system will continue to function over the entire temperature range.

Absolute compatability:

Compatability will always be assured because of the test specification of the new ckts.

Statistical compatability:

Compatability depends upon the extreme unlikelyhood of getting a worst-worst case, but is not guaranteed by the specifications.

Customer specification:

All those numbers on the data sheets and in special customer specs that are guaranteed on an individual unit. This does not include "typical" numbers.

Internal specification:

Those internal tests which are performed in order to assure that the customer specifications are achieved.

Questions:

μL
GB
Epi

There is some yield (~10%) that is absolutely compatible with μL.

There is probably some yield of Epi to μL ~~tests but~~ specs, but because of the internal test of I necessary for clamped V_{CE}, V_{BE}, these ~~are not~~ do not meet internal specifications.

Because we lucked out — or at least it is in the right direction — the GB and Epi may be absolutely compatible.

Resolved:

1. Nothing shall stand in the way of making an optimum epitaxial family tested and speced to give optimum yield & performance.
This will involve changed test points internally as well as new external specs.

There will be no yield of units absolutely compatible with μL.

There will be a yield (perhaps very low) that is compatible with GB's.

2. It shall be necessary to produce for an indefinite period units that are absolutely compatible with μL.
This can be
a) The GB structure properly tested
or b) A new epitaxial structure distorted to give compatibility. This is useful only to be able to completely drop the old technology.

Continuing, $(\frac{2.76}{R_C})(1000)(R_{SAT}) \leq 190$, or R_C must be $\geq$ 14 or 15 R_{SAT} for good yield.

R_C/R_{SAT} was greater than 15 in most of the units to date, excluding an R_{SAT} tail; it appears that initially material should stay on the low side and R_C in the 540 - 620 Ω area for optimum yield to FO = 5.

7. Tabulated distributions are given:

RUN #	100	102	103	104	105	106	116	117	130	134	137	
R_C 10%	600	640	610	610	570	570	610	620	560	550	550	Ω
R_C 50%	700	710	690	690	670	660	680	660	610	610	610	Ω
R_C 90%	800	800	780	760	770	740	760	710	730	690	690	Ω
β 5 mA 10%(1 Pin)	48	45	35	30	45	30	25	26	24	30	35	
β 50% (1 Pin)	80	70	60	50	75	62	50	38	43	50	65	
β 90% (1 Pin)	120	125	90	70	130	120	80	59	62	100	130	
R_{SAT} 10% (1 Pin)	29	28	28	31	27	25	26	25	30	26	27	Ω
R_{SAT} 50% (1 Pin)	34	35	36	36	34	35	28	28	40	33	34	Ω
R_{SAT} 90% (1 Pin)	40	42	50	43	39	44	34	35	48	40	38	Ω
V_{SAT} 10% (1 Pin)	.149	.140	.160	.160	.150	.147	.142	.145	.172	.140	.170	V
V_{SAT} 50% (1.5V)	.173	.180	.180	.210	.180	.187	.165	.158	.223	.190	.190	V
V_{SAT} 90% (V_{BE})	.217	.210	.250	.230	.210	.244	.189	.182	.269	.230	.230	V

P. 71

RUN	100	102	103	104	105	106	116	117	130	134	137	TOTAL	% OF TOTAL
TOTAL TESTED	50	49	50	40	50	50	50	50	48	41	50	528	100%
Good FO = 5 Mk II tester	7	2	5	0	4	6	2	0	1	6	22	55	10.4%
Good μEE but bad Mk II 25°C FO5 Digital Readout tester	2	1	0	1	3	1	0	0	0	2	0	10	
NET GOOD 25°C FO5	9	3	5	1	7	7	2	0	1	8	22	65	12.3%
Good +125°C -55°C Not Good 25°C FO5	1	1	1	1	1	3	1	0	2	2	3	16	
Not Good +125°C -55°C Good 25°C FO5	Not tested	0	Not tested	Not tested	NOT TESTED	NOT TESTED	NOT TESTED	0	NOT TESTED	NOT TESTED	NOT TESTED	--	
NET GOOD +125°C -55°C FO5	10	4	6	2	8	10	3	0	3	10	25	81	15.2%
Good FO = 4 Mk II	28	25	16	3	32	20	19	4	3	12	27	189	36%
Good μEE but bad Mk II 25°C FO4	2	1	1	1	0	1	0	-1	0	3	0	+9 -1	
NET GOOD 25°C FO4	30	26	17	4	32	21	19	3	3	15	27	197	37.4%
Good +125°C -55°C Not Good 25°C FO4	1	1	6	3	2	2	0	0	2	2	4	23	
Not Good +125°C -55°C Good 25°C FO4	NOT TESTED	NOT TESTED	-1	NOT TESTED	-2	-1	NOT TESTED	FEW TESTED	NOT TESTED	NOT TESTED	NOT TESTED	-4	
NET GOOD +125°C -55°C FO4	31	27	22	7	32	22	19	3	5	17	31	216	41%
TOTAL REJECT UNITS Mk II FO5	43	47	45	40	46	44	48	50	49	35	28	485	100%
Verified Marginal Reject Units FO4 & FO5	32	25	26	24	20	17	26	11	21	11	15	228	47%
Not Verified, Not Marginal Reject Units	11	22	19	16	26	27	22	50	28	24	13	257	53%
Changes by Verification at 25°C	+2	+1	+1	+1	+3	+2	0	+2 -1	0	+3	0	+15 -1	NOTE 1
Changes by Verification at -55°C & +125°C (+ means change bad to good)	+3	+2	+6 -1	+3	+5 -2	+5 -1	+1	+3 -2	+2	+2	+4	+36 -6	
Mk II Rejects I_{A5} ($R_{C\ MAX}$)	32	41	34	32	30	25	31	21	11	11	10	278	53%
Mk II Rejects, Pass I_{A5}, Fail I_{A5}/V_{OFF}	1	0	2	0	1	0	1	0	0	0	0	5	1%
Mk II Rejects I_{A4}	1	4	1	4	0	0	0	0	1	0	0	11	2%
Mk II Rejects, Pass I_{A4}, Fail I_{A4}/V_{OFF}	1	3	0	0	0	0	0	0	0	0	0	4	1%
V_{BE} Rejects, Mk II double tested	18	18/20 (1st 2nd)	31/33	30/33	17/19	29	30	46/49	44	29	22	314/326	NOTE 1
Verified V_{BE} Rejects 25°C	16/17	9/11	15/17	17/17	12/14	7/10	13/13	8/8	14/14	7/10	10/10	118/131	
Verified V_{BE} Rejects -55°C	14/17	8/11	12/17	13/17	11/14	6/10	13/13	6/8	12/14	5/10	6/10	106/131	i.e., all but 25
Mk II Changed Decision	0	2	2	3	2	0	0	3	0	0	0	12	
V_{SAT} Rejects, Passing V_{BE} Mk II	3	0	3	0	1	1	0	0	2	0	0	10	2%
Probable V_{SAT} Rejects (Both Pass and Fail V_{BE}) μEE Data (1 Pin)	3	1	7	0	1	8	0	0	15	3	6	44	8%
ALL OTHER REJECTS	0	0	0	1	0	1	0	0	0	1	0	3	<1%
Good I_{A5} Mk II	18	7	14	8	19	25	19	29	11	30	40	220	42%
Good I_{A5}, Bad V_{BE} Mk II	9	5	10	6	15	19	17	25	9	24	18	132	25%
Good I_{A4} Mk II	48	42	49	36	50	50	50	50	47	41	50	517	98%
Good I_{A4}, Bad V_{BE} Mk II	18	18	30	31	16	21	31	46	44	29	22	316	60%

NOTE 1: For example, in Run 103, on FO = 5 pass, Mark II rejected 33 units for V_{BE} (V_{ON}), on FO = 4 pass, 31 units. 17 units of the 33 were verified in μEE; 16 were not since prior data indicated very low beta. 15 of 17 were reject in μEE at 25°C; 12 of 17 were verified reject at -55°C. This would be reported as +2 Change by Verification at 25°C and +5 Change by Verification at -55°C, +125°C.

FAIRCHILD SEMICONDUCTOR
Inter-Office Correspondence

RECEIVED
JAN 28 1963
GORDON E. MOORE

1/25/63

TO: D. Yost

FROM: D. Talbert

SUBJECT: SUMMARY, MEETING Jan. 24.

cc: R. Craig, D. Farina, P. Ferguson, R. Graham, V. Grinich, G. Moore ✓, C. Plough, R. Schultz, R. Seeds, C. Sporck

---

1. Micrologic process is frozen as is.

2. C. Plough's people will test the 11 GB runs to new 25°C. specs. This includes FO = 5 and FO = 4

3. R. Seed's people will test rejects from "2" at -55°C + 125° to analyze cause. This will also determine additional yield added by temperature testing.

4. C. Plough's people will gather process data from these runs.

5. Epitaxial micrologic will transfer with present R & D process including bar resistors.

D. Talbert

D. Talbert

DT:af

Microcktry meeting – 1/29/63

Data on the first 11 runs of gates (GB) presented and discussed.

The only run that was in the range of desired logic (#137) was consistent with our original estimate of 50% yield to FO=5.

Seeds proposes changing loading factor for GB

	L.F.	Line factor
old μL	– 3,4,5	20
new GB	– 2,5,3,3	16

If we do this, we will get (with the present mask)

allow min β = 40

		μL	GB	Rc	R_c/R_b, $R_b = \frac{4V_{in}}{a I_m}\Big\vert_{I=1ma}$
	NOW	10%	36%	670	1.3
opt to GB	ALT I	35%	80%	640	1.8
opt to old μL	ALT II	45%	65%	570	1.8

What should be the epitaxial resistor be to be compatible as so far as possible with the GB? – Answer next time – Farina.

~~Plough bias curves~~.

Action items:

Start masks – Plough for alternate I
Wafers (small) to μL starting today.
Seeds will get a test spec for GB's tomorrow.
Data sheet revision will be started.
Farina will look at epitaxial resistor to see if optimum
Farina " order functional testers
SB evaluation ASAP
ES " "

 1/30/63 - Power transistors

Grinich — Lamond — Kattell
Sah — Reddi — Faires
Ornido — Cordaro
Fegan — Rankin

A. High Power Capability FT-7000

Present production goes at 20-35 ~~watts~~ volts at 1 amp, D.C. (8.3μ base)

Some experimental non-epi units, c only 15 Mc ~~base~~ f_T were 33 W vs 22 for control (3μ base).

We have never made any good 7000's on ~~our~~ Fairchild epitaxial material. We have on Merck, T.I and Westinghouse.

Three possibilities:

1) Wide base — straight / epi base / both sides — to raise switch back
2) Aggregate with limiting resistors — to balance for " "
3) Inverse epitaxy — to lower V_{SAT}.

In discussing the possibility of an epi base, it ~~is~~ has been pointed out that on SCR material Ornido got a spread of 5-22μ around ~~one~~ row.

Lamond says that the Mtn View P diffusion system is much worse on ours on resizing devices. (Using R&D emitter diffusion they get 50% do not spill)

Prieve recommends making an epitaxial 6206 designed as an optimum for 20 watt unit.

!! Our power program:

1. Bail out the region of high f_T 7000, 6205 to make good devices.

2. Make a power device above 85 watt, damn the f_T.

B. 7500

MIT is getting non-epi devices that meet their specs, but they don't like them because of very borderline VCE (SAT).

Some inverse epitaxy units were made. Unfortunately they had too high ρ material, so ran into limiting velocity problems.

Our PNP power program:

1. Aim at the complement of 85 watt NPN, damn the f_T.

2. Keep MIT happy.

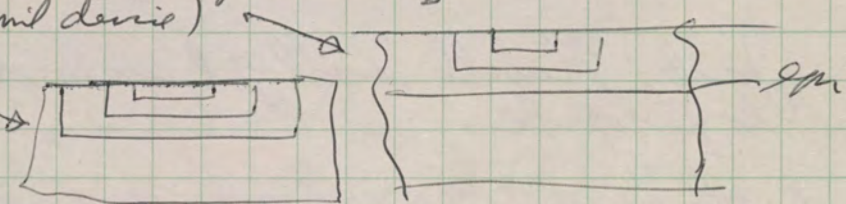
C. FT-8000 – When ever there is a significant improvement on 7000, try to make some big ones.

D. High voltage device. ; ≈400V LV_{CEO}, 7000 geometry – low priority

E. SCR-1 – Now a good lamp, high sensitivity

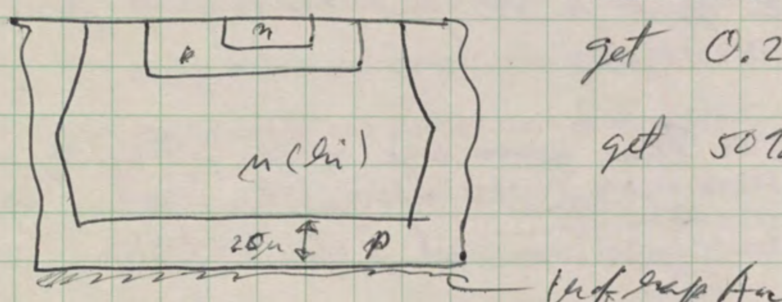
a) IBM spec (a 25 mil device)

b) High voltage.



F. SCR-3

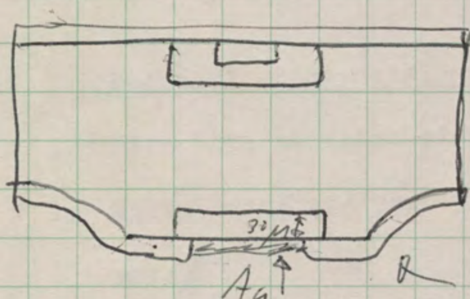
Structure 1



get 0.2 yields breakdown spec/device

get 50% of junction > 300v

Structure 2



This requires $POCl_3$ gettering of a severe type.

Problem of thin sharp corner.

Question: Which structure to xfer.

When will Mtn View be ready.

FET Meeting - Project Review 1/31/63

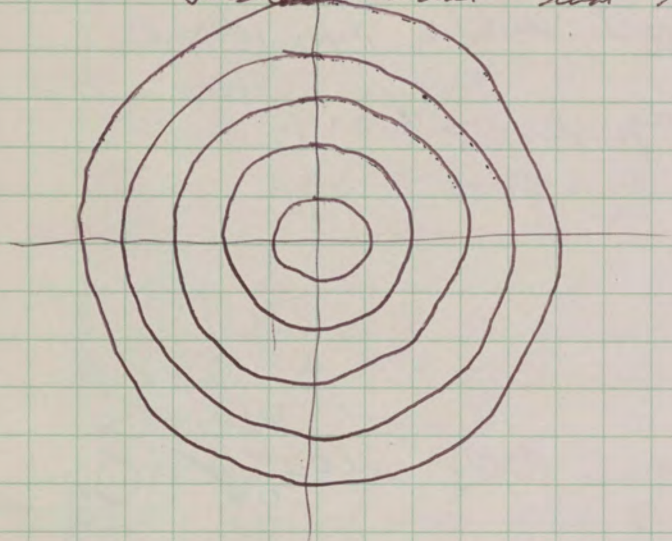
Ferguson, Ragle, Hilbiber, Tremere, Sarnitsen, Waring, Kabell, Perkins, Bittenger, Ginn, Sah

Ragle says that he is under the impression that epitaxial and outdiffused are roughly equal

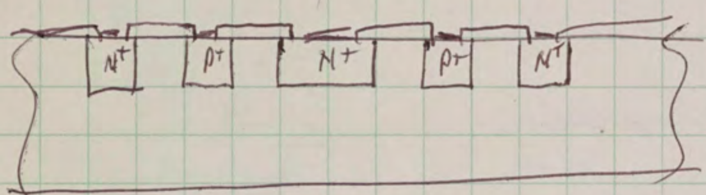
No real information on the mechanism.

Jack Kabell will get units from ~~the~~ Ragle and try to photoprobe.

Leistiko structure that looks good for the first 100 lines so far



These ~~were~~ were made identically with the out diffused devices. Except for a separate oxide removal before oxidation



Hilbiber has tested some of these (13 good ones)

FET TESTS IN PROGRESS

A. Variations of oxide characteristics

1. No N^+, ~~or~~ gettering N: –ie, no P (not out)
2. N^+ and gettering in single step (lowered noise, failed)
3. Strip oxide and re-oxidize pyrolytically (at die next)
4. Strip oxide and re-oxidize anodically ( )
5. Strip oxide, etch slightly, and re-oxidize anodically (starting)
6. Getter and N^+ pre-dep, pyrolytically oxidize before oxide removal mask (all along)
7. Strip and evaporate SiO (just starting)
8. CP-6 etching of failed units to see if failure point has thin oxide

B. To check effect of metal-over-oxide

1. More Otto Leistiko circular units to Mt. View
2. Extra oxide via pyrolytic to minimize possibility of pinhole penetration by metal
3. Chromium metallization (done & failed)
4. No metal over junction
5. Big base U-1

C. Miscellaneous tests

1. P channel (waiting epitaxial
2. Base doping level isolation
3. CO surface stabilization
4. No top gate

1/31/63

SHORT SUMMARY OF FET LIFE TEST - January, 1963 (B. Barranger)

The Fet life tests are divided into three groups; Outdiffused, Epitaxial and Special Runs for L. Ragle.

Outdiffused:

The first life test consisting of twenty units from three runs were 100% failures after 12 hours under 30 v reverse bias at 100°C. 10 v leakages ranged from 1 μA to 2 mA, the majority between 100 and 500 μA. Subsequent test of 5 runs under the same conditions were recorded hourly. Wthin one hour, most unit showed a 100% increase in leakage and within four hours, 80% had leakages over 1 μA. At twelve hours, all but two (of 25 units total) had leakages over 10 μA.

The failure mode appeared to be a classical channel which did not pinch-off completely. With time (and increased leakage) the pinch off became less prominent until it was hardly notciable.

Epitaxial

The first three runs (actually three test wafers) showed a marked improvement over the outdiffused runs. Run # 2 completed a 1000 hour 30 v, 150°C stress without any problems. The other two runs produced failures at various times, anywhere from 50 to 700 hours. All other runs (13 in all) showed 80% failures at various times. Because of space limitation, a run was removed upon reaching 80% failure rate.

The failure mode was similar to the outdiffused except for a more prominent pinch-off. But it too tended to become less prominent with time.

Special Runs from L. Ragle

The only run worth mentioning is # 9 which is gettered with phosphorous rather than nickle. Three groups were received as follows:

(10 units) Group 1. Completed 1000 hours at 30 v, 150°C with no problems.

(10 units) Group 2. Two failures at 100 hours. The eight others completed 1000 hours without other problems.

(10 units) Group 3. 5 of 10 failures up to 130 hours (still in progress)

Short Summary of FET Life Test - January, 1963 (B. Barranger) - continued

Others

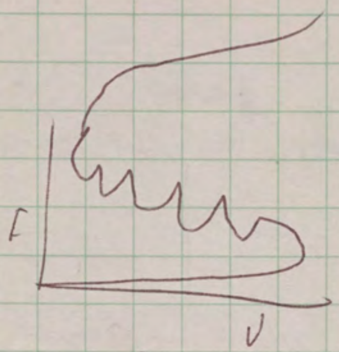
Phosphorous vs nickle gettered epitaxial - no difference.

Double-gatted (circular geometry).

1/31/63 μ wave philosophy

Sat · Shimizu

Harmonic generation – Harmonic Gen
Switches – Diode
Neg resistance gadget – Problems of
– Gunn



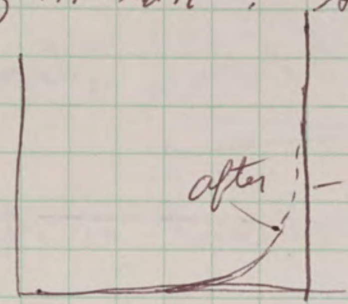
∴ No single valued load line.

None is talking about anything broad band or tunable.

 FC-1 2/6/52

Summary of data

Sandia 125°C, 5 ma, Ni & noNi $ and no$. Got 100% failure.



- It was just a general softening of the characteristic

Sandia 125°C, 1 ma., 15 units, all failed in 100 hours, all $ units
The junction that goes soft first is the one under forward bias.

On our data

3/10 @ 100 μa, 125°C for 23 hrs P-gettered $ failed

0/6 @ 100 μa, 125°C " " " Ni-gettered (?no$, ns) failed

Elmer found ~10% going sick @ 100 μa and 125°C. (But he thinks it looks like a 125° mean problem)

"All" this data is on glass encapsulated units.

Of the 3 units we had fail, one had recovered after 4 hours

Paulsen at S.R. has done some step stressing at various T using I_2 as the stress. At high temp, everything crapped out.

Possible ~~problems~~ hypotheses:

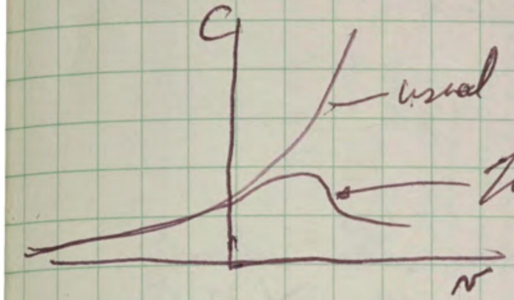
1. Its the package. – Run 1240, 1243 Xstors

2. The Ni gettering is bad. – Run some Ni ones.

Harmonic Generation   1/6/63

Solt
Henselbar
Grimil
Moore
Hazeem
Parker

The C v V of the FD-6's is variable.



These are bad for harmonic gen.

↖ G.P. point out that this can happen in a over compensated Au-doped unit.

Except for this, correlation don't look so good

Efficiency vs BV
" " forward drop @ 200
" " @ 100

"Yield" ≅ 7/43 ">50%"
20/43 ">40%"

No one talks about tunability or broadband multipliers.

Get the Dept of Commerce Journal info for Solt.

We must

a) Continue to look at our capability

b) Pick a more specific objective

c) Get our device capability better tied down.

Feb 11, 1963 – Film resistors
Ref p. 50 (Jan 3)

Ferguson
Campbell
Waite
Ruegg
Sah

Nichrome:

Waite evaporates fast from a W wire.
Ruegg is now using an Nichrome wire.

At ~630°C substrate temperature Waite made a run that had a very ~~lar~~ large non-uniformity over a wafer, say 10 - 300 Ω/□ on one wafer. Alloying didn't help.

At substrate slightly higher T, then ~20°C during alloy the film goes down in R

O_2 can be bled in. The more O_2, the greater the change during alloying.

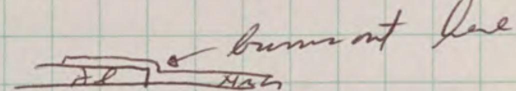
The only encouraging thing is that ~~a~~ 2 runs made at 2×10^{-5} mm of Hg of O_2 changed relatively slightly during alloying.

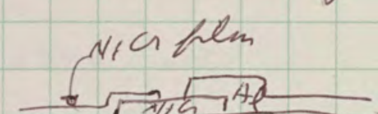
Ruegg agrees on the W-evaporated ones.
He did some from a nichrome wire @ ~ ~ 3×10^{-5}

The spread is still primarily systematic across a wafer – on all of our films.
No one knows why – i.e., is it not tied down to geometry or film.

Ruegg has data on 125°C life test @ 100 w/cm² – looks good!

Waite has shown that contacts first is not the way to fly – they burn out too soon





better, but still burns out

In the mill:

H.R. has reproducibility runs (9 of them covering the whole substrate T range, mostly at 300-400°C).

Rugger data — Page 78

Change of resistance of Nichrome resistors during 2min-580°C alloying cicle

$r_s \approx 150\,\Omega/\square$, evap. from NiCr-wire ; pressure = $3\cdot10^{-6} - 10^{-5}$ mm (no O_2)

Run Nr.	Substrate Temp	V/I before alloying	Mean R before all.	Mean R after all.	10%-90% spread before all.	10%-90% spread after all.	Mean ΔR = $R_{after} - R_{before}$	10 percentile of ΔR	90 percent. ΔR	TCR
31	≈ 250°C	40 - 45Ω	18.9k	17.9k	10.4% (2W)	14%	- 5.3%	-7.2%	0%	
30	≈ 320°C	31 - 33Ω	14.3k	12.9k	7.5%	4.5%	- 10.1%	-12.2%	- 8%	!!
36	≈ 420°C	24 - 27Ω	2.01k	2.14k	3.5%	4%	+6%	+ 5%	+ 7%	
32	≈ 450°C	22 - 24Ω	9.4k	10.15k	10% (2W)	13%	+10.3%	+7.8%	+13.2%	
38	≈ 500°C	32 - 36Ω	2.67k	3.01k	3.75%	4.0%	+ 12.4%	+10.6%	+15.2%	

different geometry

2-10-63 H.R.

Nichrome films evap. in a residual oxygen atmosphere

Run Nr.	Substrate temp	O_2-pressure	Mean res before all.	Mean R after all.	10% - 9% spr. before all.	10%-90% spr. after all.	Mean ΔR. $R_{aft} - R_{bef.}$	10 percentile ΔR	90 percentile ΔR	TCR
33-34 (Ni-Cr wire)	450°C	$3 \cdot 10^{-5}$	V/s = 41-50		could not be etched					
40 (Ni-Cr wire)	30°C	$3 \cdot 10^{-5}$	600 (36-44 V/s)	1.15k	10%	7%				
35 (NiCr-wire)	450°C	$3 \cdot 10^{-5}$	1.80	1.58	3.9%	3.8%	-13%	-14%	-12%	60-120 ppm/°C
28 (tungsten)	450°C	$3 \cdot 10^{-5}$ air					+0.8%	-0.7%	+1.6%	170-230 ppm/°C
29 (tungsten)	450°C	$8 \cdot 10^{-5}$	8.9k	7.1k	12.2% (2w)	9.9%	-21.5%	-20%	-23.4%	290-330 ppm/°C

2-10-63 H.R.

Question:

Reproducibility. Best point looks like evaporation from a Ni Cr wire in a "pure" vacuum at ~400°C substrate. H.R.

Process sensitivity:

Null hypothesis: It is due (good results) to a dirty vacuum system.

Experiment: Use H.R. jig in Varian system for good comparison.

Effect of crudy oxides – those that have been thru everything but masking for n+.

Variation across wafer.

Postulate: It is geometry.

Experiment: a) Measure geometry or R. across wafer
b) Compare data on the different width resistors

It would be useful to measure diffused resistor variations across the wafer and to life-test these. H.R will ~~consult~~ talk with JPF re. the advisibility of doing this.

 Feb 11, 1963 – Epitaxial Vapor Etch

Slaphead
Wigton
Sah

Clean up the old Schaleburg system to get rid of everything in the way of problems.

Measure rates and perfection of films.

Other films, con't 2/11/63

→ Boron doped oxide (V/I = 20)
Diffused for 1 hr total (15 min dry, 45 min wet)

1000 Å, 750°, 20 min get ≥ 33 K (bad spread, lots of grown on 1 run)
vs ~100 K for pure oxide.

P-doped oxide (P_2O_5 for V/I = 0.7 - 0.9)
Diffused @ 1100° per µL process

1000 Å, 750, 20 min get ≤ 1~~14~~K. (avg ~135 KΩ) Spread looks pretty good.

These have been processed over c ~~the~~ KPR – no problem.

Problems:
1. Contacts without forming
2. Need non-p-killing heat treatment.
3. Life test data.
4. How does it work on re-grown oxide.

Feb 11, 1963 – Other film resistors

Campbell
Waits
Sah

Looking @
1. Si thin film
2. Cermet
3. SnO_2
4. TaN

?? Pure Cr / Ta

TaN + SnO_2 are unstable as sputtered.
SnO_2 will stabilize @ ~900°C. This is from Sn + 7% Sb.

SnO_2: If we want to do any more, we should go to spray.
Intalux can (or will) coat oxidized Si wafers. – We will send some

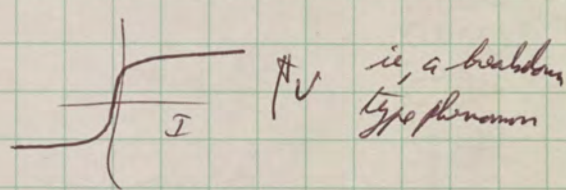
TaN: Still too early to tell. We are way off on ρ, ~10^{-5} off – too high ρ.

Cermets: Cr + SiO_x
Our early work was separate sources by electron bombardment.
Now we use flash evaporation from a heated Ta (or W room) boat.
ρ is in 10^{-4} Ω-cm range.

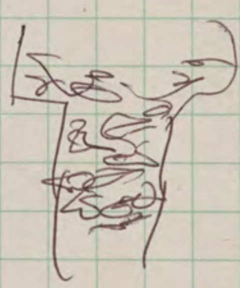
Problems:
1. Etching
2. Bad changes on heat cycling – down 50% or so.

Possibly some spike alloying combined with a subsequent anneal to value is worth trying

Si thin film:
580°, 750°, 630° reaction temperatures
At 580°C get non-uniform films which show
they also look this way at 630.
These films look good, but perform poorly.



At higher temperatures the films look "terrible"
There is an appearance of a grossly divorced 2-D eutectic.
Contacts need forming.



One run came thru that required no forming.

Some run for 8 hrs @ 500 mw – almost no change.
out of 11 units, the largest change was ~5%.

 Section Meeting 2/11/63 – Everybody

Folk
Blyth
Van Ness
Engvall
Sloane

Memory array is in mill –

Manpower – add a girl.

An interesting point contour.

We will take the periodic error down further.

Optical jigs:

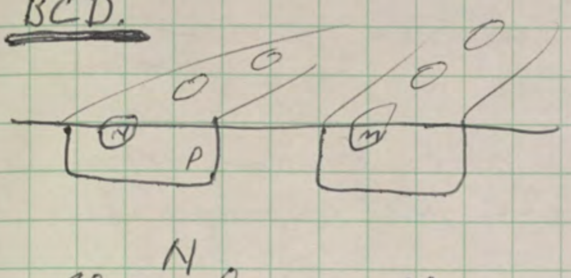
Art Engvall will examine the economics and use of lacquer coating instead of wax

Gene will recommend on a mask check program.

Diode matrix 2/11/62

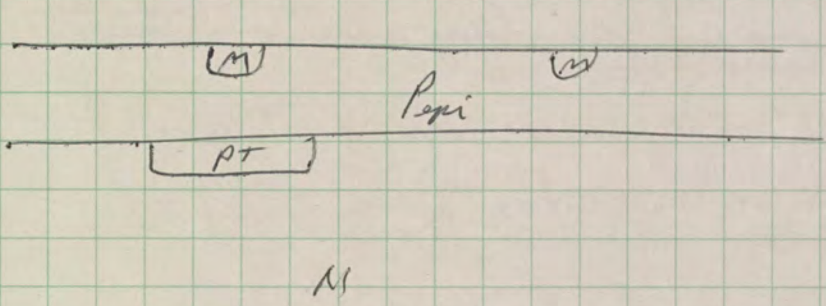
Campbell
Ferguson
Price
Grinich
Moore

BCD.



This has problems of Xstor action.
By Au doping this can be made smaller, but leakage goes up to what is probably an intolerable level.

New structure



Using this structure a BCD matrix we can get it @ 50×100 mil (40×90) for the full 40 diodes.

It should be the other polarity for compatibility with processing. This, however, results in problems for logic because it makes ~~again~~ the buried line the Sb diffusion before epitaxy, which is too long. Especially because it then must be 18' long.

No good diodes anyway like this have yet been made.

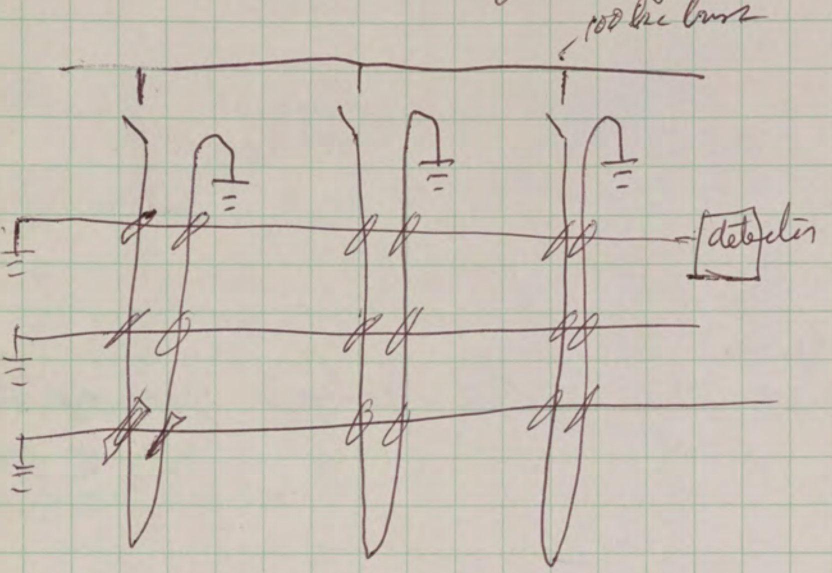
I feel this project is useful, but much more useful is to put Price in the Dev. Dev. section c̄ the ~~FXXX~~ shift as his first project.

Al fuses.

On the burn out our all fuses go from 500 - 1000 ma
Get ~ 99.8% diode yield
But pieces don't fit together - isolation is the problem.
Some life test data on fuses (Al).

 Feb 13, 1963 – Jim Angel rundown on Adaptive Systems

Angel
Rozze
Girval
Perkins



This can also be done on the a film with erasing leads.

glycine phosphate is presumably a ferroelectric that does not tire.

It turns out that there aren't many companies are doing adaptive ~~[illegible]~~ components

Even the magnetic array takes ~$1/weight – ie, 30¢ sa tape wound cores.

Possible uses:
1. Voice control to a computer (only α-numeric computer)
2.

P. 84

(1)

Self Organizing Systems - 1962

Contents

6. International Simulation: An Example of A Self O.S.

H. Guetzkow — Northwestern University

7. On the Automatic Formation of a Computer Program Which Represents a Theory

Saul Amarel — RCA Labs.

8. Optimization Through Evolution & Recombination

H. J. Bremermann — Math Dept, U of Cal, Berkeley

9. Natural and Artificial Synapses

L. D. Harmon. — BTL - MH.

10. On Probabilistic Push-Down Storages

M P Schützenberger — Harvard Med School.

11 Concerning Efficient Adaptive Systems

John H. Holland — Communications Sciences Lab. U of Michigan

12. Empirical Laws & Physical Theories - Information & Imagination
L. Brillouin — Columbia U.

13 Majority Logic and Problems of Probabilistic Behavior
Saburo Muroga — IBM Research.

14 Interaction Between a Group of Subjects and an Adaptive Automation to Produce a LOS for Decision Making
Gordon Pask — (System Research, LTD) England

15 Cybernetic Ontology and Transjunctional Operations
Gotthard Günther — Elec Eng Res Lab, U of Illinois

16 Some Problems of Basic Organization in Problem-Solving Programs
Allen Newell — Carnegie Inst of Tech

17 Training Sequences for Mechanized Induction
R. J. Solomonoff — Zator Company, Camb Mass.

18 Adalines - BW — SU

19 A Comparison of Several Perceptron Models
Frank Rosenblatt — Cornell U.

20 A New Class of Multilayer Series-Coupled Perceptrons
Alan G. Konheim — IBM Research.

21. A Test for Linear Separability As Applied to Self Organizing Machines

Richard C. Singleton SRI

22 Function Algebra and Propositional Calculus

Karl Menger Illinois Tech.

23 Some Similarities Between the Behavior of a Neural Network Model & Electrophysiological Experiments

B. G. Farley Lincoln Lab.

1962 COSOS

Lincoln, MIT	III
Case	I
England	II
Michigan U	II
Northwestern	I
RCA	I
Cal Berkeley	I
BTL	I
Harvard	I
Columbia	I
IBM	II
Cornell	I
Illinois	II
Stanford-SRI	II
Carnegie	I
Yale	I

Work in Artificial Intelligence and Self Organizing Systems

I <u>Artificial Intelligence a la Minsky</u> — Proc. IRE, Jan 1961

1. Search -- trial and error, hill climbing, false Peaks

2. Pattern Recognition .. experience, etc.
   Classification, invariances

   adaline (bracketing 2 and 3)

3. Learning — generalize on past experience in reaching goals
   - try ideas that worked.
   - reinforcement

4. Problem Solving & Planning

5. Induction & inference.

II <u>Self-Organizing Systems</u> — Also a Proc IRE, Jan 1961

1. Recognition (fixed)
2. Learning. (variable nets)

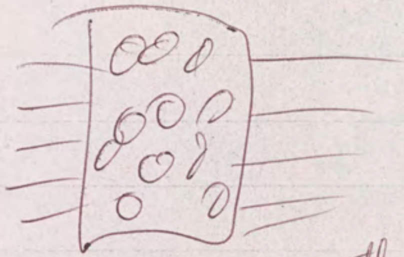
A. Perception
B. Madaline
C. Artron
D. Neuristor

III Implementations

A. Transfluxor
- GE 1st
- Aeroneutronics 2nd
- SRI (Ted Brain)

B. SHMAC (second armonic magnetic adaptive component) (Craftron)

- SU
- SRI
- Cornell - Rosenblatt
- Matrix
- Thin Films



C. Memistor
- SU - MC

D. Solion - not very promising
- BTL - ~~TRE~~ out of business

E. Speculation
- Flexode - RCA - lithium doped resistor.
- Repairable Paths - SU (Beadle) Sandia, Space-General.
- Silver Halides - SU
- Ferroelectric - Pulvari, Moll
- [illegible]

F. Neuristor
- Melpar
- SRI
- SU — Japan

IV <u>Digital Simulations</u> - definitely an important competitor
- S U
- Lockheed - Mattson
- I B M - We'll have at SU

V <u>Hardware Simulations</u>
- B T L - Harmon
- Adaptronics, Astronics, Melpar } Astron

VI COSOS (conference on self organizing systems) - Proceedings edited by Yovits

VII <u>Theory</u> - non adaptive implementation
- Philco (Post Office)
- R C A
- I B M
- Melpar
- M I T
- Carnegie, Princeton } Problem Solvers.

Feb 13

Data we have

100 μa, 125°, glass vs tester, $, a$

			1hr	after 48 hrs	
$	glass	P-getter	0	no failures out of 10	
$	"	Ni	1	7 out of 10	(2 recovered at room temp)
AS	"	none	1	7 out of 10	
AS	TO-5	none	1	16 out of 18	(5 recovered at room temp)

 Epitaxial defects 2/18/63

Larry — Victor
Lawrence — Sah
Lynn — Shepherd
Davis — ~~Moore~~
Tucker — Hunt

Lawrence

Pyramids & raised triangles cause soft junction (diodes). No low-diode B.D.

"Hole" defects are not bounded crystallographically

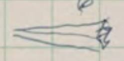
"P's form on ~~impurity~~ foreign contaminants on substrate"

1. SiO_2 ~~as anodic~~ anodic film 2000Å thick. At the holes in the oxide growth of P is shown. The hole came from nowhere – 10/½ wafer.

2. 200Å of SiO_2 (anodic) no more P's than an ordinary wafer.

3. Ground up wafer on to a mech polished wafer gave P's ~~by~~ by the thousands

4. Thermal etch pits (made in A in a diffusion furnace) no P's, but ~~...~~ other defects that look like



of flow line appearance in one-to-one correspondence.

5. N_2 thermal etch pits did not make P's

6. Al_2O_3 – 3μ – loaded with P's

7. .3μ (.4μ) – " " "

8. SiC – " " "

9. ZrO – " " "

10. Carnauba wax residue shows some

11. $CaCO_3$ or NaOH or CeO will make P's, but especially a lot of raised triangles.

12. Chemical etch pits are ~~...~~ inconclusive. Too many everywhere.

In any case, we still have a P problem. Even on our best films we run a few per wafer on the average.

We will not be satisfied until there is < 0.1 per run.

INTERNAL CORRESPONDENCE

FAIRCHILD SEMICONDUCTOR

A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

TO: Distribution DATE: February 18, 1963

FROM: V. H. Grinich CC: G. E. Moore

SUBJECT: Microcircuitry
Minutes of Meeting held February 18, 1963

In order to minimize the amount of repetition we will review action items that were discussed at the January 29th meeting on μL Review and then proceed on to new business.

Items from μL review held January 29, 1963

Policy Decisions 1 and 2: The two policy decisions that were stated in the minutes of the January 29 meeting were re-emphasized and all parties agreed to it. In addition it was stated that we would closely evaluate the epitaxial versions of μL elements by means of bringing out a lead from the base of at least one transistor in order to monitor resistance, and also to get a closer handle on transistor characteristics.
This will allow us to establish a base for any further modifications that may be deemed desirable.

Action Items from January 29 minutes

Item 1) 10 units of the GBY elements (double dog bone resistors) were evaluated with good results in regard to resistance ratios and turn on voltage. GBZ, SBZ and HBZ masks exist (these are hybrid resistors with some dog bone and some slip contact resistors). 40% classifications yield has been obtained with the SBZ, however. SBYs, HBYs and other of the family will be stepped as soon as the GBY units are completely evaluated. This is all being done through Mountain View in Production and Applications Engineering.

Item 2) Epitaxial material was supplied to Mountain View from R & D. However, due to Mountain View's other commitments they did not feed back information or take the data as to die sort yield for the epitaxial "S" element. Yields on present HSG-3 epitaxial units are 50-80% hard breakdown at V_{CC} = 5V.

Item 3) Completed by Applications Engineering.

Item 4) Work under way by Applications Engineering.

Item 5) The present minimum geometry layout will be evaluated before any modifications are considered.

Item 6) Work order in process.

Item 7) SBY units need to be evaluated before this can be recorded.

Item 8) Epitaxial material was sent to Mountain View as discussed under Item 2. New runs are near die sort in R & D.

Microcircuitry February 18, 1963
Minutes of Meeting held February 18, 1963

The following new business was discussed:

1) Current Mode Logic Gate is at metallizing.

2) Discussion of new design for higher speed current mode gate was concluded with a decision that we will bring out extender tabs on both sides of the present current mode gate in order to evaluate ways of getting temperature compensation within each device, and at the same time allow us to operate with a 500Ω in place of a 5000Ω resistor. We expect to be able to get with this new circuit at 1200 μV dissipation 3.5 nsec delay for a fan out of 1 and 7.5 nsec for a fan out of 5.

3) Discussion of yield on DPD circuits showed the following results have been obtained in Mountain View. For the R element with 40 wafers into the line, 12 wafers made it to metallizing, giving 96 devices at pre-sort from which 14 finished units were accepted by DPD. For the adder circuit 440 wafers provided 39 finished units; for the four input gate 220 wafers provided 147 finished units. Before we make any epitaxial masks for the DPD circuits we will get more yield information on the epitaxial S element.

4) Discussion of the binary circuit using storage diode steering indicates that we have some problems in getting a tight control with both a minimum and maximum on the diode storage time. It appears that we will need 10 microns collector region thickness (distance from diode junction to isolation junction) in order to obtain 100 nsec effective life time. Some minimum beta on the pnp transistor is a sufficient condition to imply we have the life time but because of emitter efficiency effects it may not be a necessary condition.

There will not be a Microcircuitry meeting on Monday, February 25. Notice will be sent out prior to the next meeting so there will be no mixup.

VHG:ef
Distribution:
D. Farina
P. Ferguson
R. Seeds
R. Shultz

Lawrence would like to continue to track down the causes.

1. Other contaminants
2. Thin films around a known contaminant

Yim: Working on J film growth with a 10 min slow step. 0.1-0.2μ/min.

A density ~ independent of T growth.

We will observe stacking faults for now to see if we can see any correlation.

Section Meeting 2/19/63

The S&R camera has been frozen c a small (~100 pixel) p to p error

We are going to try some Nikon lenses for large field coverage and 0.2 N.A.

Some Belgian plates are being tried.

G. Moore

WEEKLY NON PRODUCT STATUS REPORT

SMALL GEOMETRY SECTION W/E 2/17/63

PRODUCT	ENGINEER	STATUS
3111	BOTTE	APPLICATIONS STILL EVALUATING THE MOST RECENT RUNS. I_{EBO} IS DEFINITELY OUR BIGGEST PROBLEM ON THIS DEVICE. RESULTS FROM 1060°C GOLD DIFFUSED AND PYROLITICALLY OXIDIZED RUNS SHOULD BE AVAILABLE BY 2/25/63. APPLICATIONS LIFE TEST DATA ON RUN #6 SHOW NO FAILURES AFTER 500 HRS.
0000/1	SMULLEN	NON-EPITAXIAL 0000'S (5.1-5.6 Ω cm) STARTED IN 1211/1311 GROUP DURING THE WEEK. FIRST RUNS SHOULD BE AT DIE SORT BY 3/4/63 AND AT CLASSIFICATION BY 3/15/63.

C.C. T. BAY
V. GRINICH
G. MOORE
C. SPORCK
D. YOST
B. SCHULTZ
B. KNUDSON
P. FERGUSON
R. GRAHAM
W. RICHMOND
R. CORE
P. LAMOND

DATE PREPARED 2/18/63

SIGNED John L. Santana

W/E 2/17/63

PROJECT	ENGINEER	STATUS
0002	REITER	FIRST MT. VIEW RUN WILL BE AT DIE SORT ON 2/19/63. IT WAS MADE USING MATERIAL MANUFACTURED AT STIERLIN RD AND LOOKED QUITE GOOD AT T-84. AT LEAST 2 MORE FSC RUNS SHOULD REACH DIE SORT BY THE END OF THE WEEK. THE LAST 5 RUNS STARTED AT R & D (USING MERCK WAFERS) GAVE PRACTICALLY NO YIELD AT DIE SORT AND THE 2 MERCK RUNS IN PROCESS AT MT VIEW ALSO LOOK BAD. THE EXACT PROBLEM WITH THE MERCK MATERIAL HAS NOT BEEN DETERMINED AS YET. LIFE TEST DATA (O.L.) ON THE 0002 IS BEHIND SCHEDULE DUE TO PROBLEMS IN APPLICATIONS.

FAIRCHILD SEMICONDUCTOR
Inter-Office Correspondence

2/11/63

TO: D. Yost

cc: C. Sporck
J. Sentous
J. P. Ferguson (R&D)

FROM: P. Lamond

SUBJECT: NEW PRODUCTS SCHEDULE - SMALL GEOMETRY SECTION

The following is an updated schedule for the introduction of new products in the Small Geometry area:

Product	Dates	
	Engineer At R&D	Product in M.V.
0000/1 AG C & RF	2-11-63	2-11-63
1340/41 Replacement	5-1-63	5-1-63
3 x 1312 TO5 -5 leads	5-1-63	5-1-63
0008 T.F.D.	6-1-63	6-30-63
I.B.M. S.C.R.	8-1-63	8-30-63

Pierre R. Lamond
P. Lamond

PL:af

RECEIVED
FEB 12 1963
PHIL FERGUSON

Pre product planning meeting[2]

From Pierre Lamond memo - 2/11/63
Small Sig.

0000/1 into line @ 2/11
1340/41 replacement
3 x 1312 - TO5-5 leads for CDC
0008 T.F.D. 6/1
IBM S.C.R. 8/1

1221 - ?
1450 - only if brought up.

"The tridents"
3111 - flying

We should plan the trident family.

FET's - not much new

PNP
4511 —
1713 — they had fr trouble, but now looks ok. Rating problem for 1702?
3511 — looks good
1702 — Bring up.
7500 — Not a real competitive bird?

6205 —
6206 —
7000 —

Large Geo

4116 — 4201

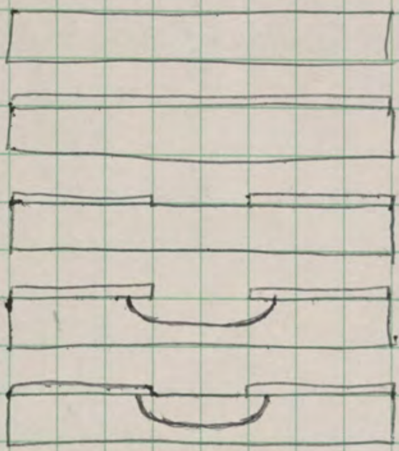
SCR - IBM
- H.V.

 Feb. 26, 1963

– Project Review – Special Epitaxial Device Structures

Pre-meeting ideas

1. Simple cut and backfill



A. oxidizing

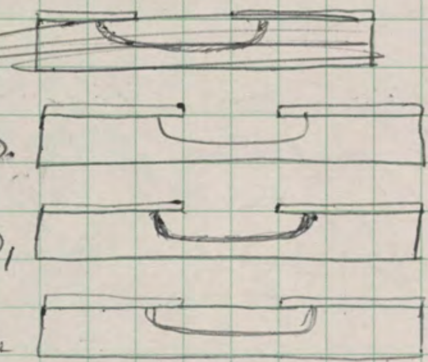
B. mask & etch oxide

C. vapor etch

D. grow epitaxial

E.

2. Cut and backfill with an additional diffusion step between D & E



~~D_1~~

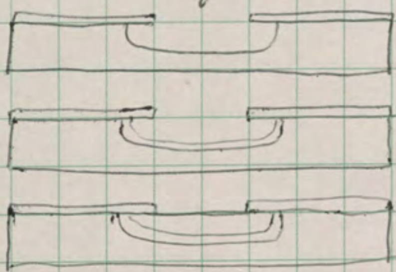
D. As predep, min O_2

D_1 ~~HF dip~~ epitaxial growth

D_2

This one has the potential problem of not allowing adequate clean-up between diffusion and growth.

3. Cut and back fill, controlled doping



D grow heavy n-type (As doped)

D_3 Switch to lightly doped

D_4

DATE 7/25 19 63
EQUIP. USED
TAKEN BY Dick Craig
REQUESTED BY

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION
ENGINEERING DATA

( ) FT. HSG3 CLASS
REMARKS Metallized Wafer yield
GROUP (Epitaxial Gate)

LOT No.	DE.	OP.	GR.	TYPE No.	CL.	TE.	COND.	DATE	ELAPSED TIME	SP.	SP.

RUN ~~LOT~~ No.	Wafer ~~UNIT~~ No.	0: Yield I_{CEO} <10uA @ 5v.	1: Yield I_{CEO} <100uA @ 5v.	2	3: Typical h_{FE} 5mA	4: Typical LV_{CEO} 5mA	5	6: X_i Epitaxial Layer Thickness Hg	7	8	9
HSG3-5											
	A	44 %	56 %		60	10 v.					
	B	30	35		40-60	15					
	X	0	0								
	Y	0	0					(10-20 fr.)			
	Z	0	0								
7											
	A1	0	12 %			7 v.					
	B2	0	5								
	C3	12	48		40-80						
	D	0	6			12					
9											
	A	0	22 %			12 v.					
	B	32	76		40-70	14					
	E	8	21								
	C	8	16		50-70						
	D	50	50		50-70						
10											
	A	12	66 %		35	8 v.					
	B	30	50		40-60	12					
	C	22	57		30-70	12					
	A2	52	64		30-70	10					
	B2	60	62		30-70	13					
	C2	32	55		40-70	10					
11											
	A	32 %	60 %		100-140	7 v.					
	B	12	12			8					
	C	25	35			7					
	D	20	20		70-130	7					
	E	0	0		>200	<2v.		~21 fr.			
12											
	A	72 %	80 %		30-45	14 v.					
	B	64	72		25-45	14					
	C	36	44		30-70	13					
	D	64	84		25-30	16					
	E	52	56		25-45	15					
	F	76	76		30-55	15					
13											
	A	65 %	66 %		20-50	13 v.					
	B	48	56		40-70	13					
	C	66	66		40-90	11					
	D	64	74		30-55	15					

S-1308A Rev.

DATE ______ 19 ____

EQUIP. USED ______

TAKEN BY ______

REQUESTED BY ______

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

ENGINEERING DATA

( ) FT. HSG3 CLASS ______

REMARKS ______

METALLIZED WAFER YIELD

GROUP (EPITAXIAL GATE)

LOT No.	DE.	OP.	GR.	TYPE No.	CL.	TE.	COND.	DATE	ELAPSED TIME	SP.	SP.	

RUN ~~LOT~~ No.	Wafer ~~UNIT~~ No.	0 Yield ICEO <10 uA @ 5v.	1 Yield ICEO <100 uA @ 5v.	2	3 Typical hFE 5mA	4 Typical LVCEO ~~hFE~~ 5mA	5	6 X_i Epitaxial Layer Thickness (Hg)	7	8	9
HSG3-15											
	A	46 %	52 %		60-160	15 v.					
	B	42	51		50-170	13					
	C	60	64		55-65	15		~~34~~			
17											
	A	42 %	42 %		80-100	13 v.					
	B	75	78		70-100	18					
	C	62	67		—	14		34-38 fv.			
	D	58	61		50	12					
	E	68	86		80-100						
	X	0	0		~200	2-4v.		27fv.			
	Y	0	0		~200	2-4v.					

THESE YIELDS INCLUDE ALL WAFRS WHICH REACHED ALLOY EXCEPT FIRST THREE RUNS

Yim:

Grown junctions

Start c̄ 0.3Ω cm p substrate

A. Grow 0.3Ω cm P for 5μ
Grow 3μ of 1.5 Ω-cm.

Get "v. hard" mesa diodes on ~~80% of 10 mil mesas.

These were grown for FET people — no feed back.

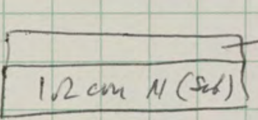
B. 0.2, 0.1, 0.02 p-type substrate
grow 1.5Ω cm n
0.5 Ω cm p

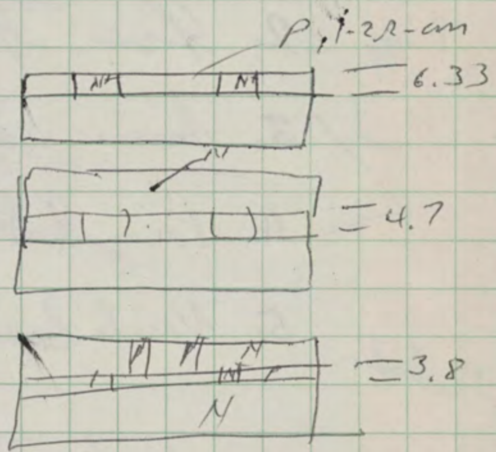
Get 8-7μ "base"
2.5-3.5μ "emitter" (2600 - 4200 V/I [illegible] over 1 wafer)

Get BV of ~100 on c-b, 10-30 on other.

On 4 X-section, only one show parallel junction. The collector varies all over the map.

C. ~~1Ω cm N~~



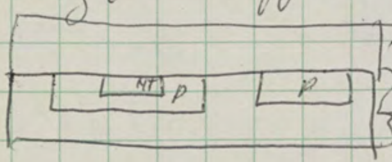


do isolation diffusion N+ grid

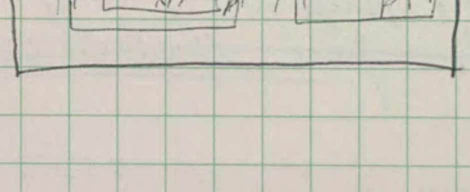
grow 4-5μ of 1-2 Ω cm N type

Do p-type isolation.

D. Many other diffused & grown structures

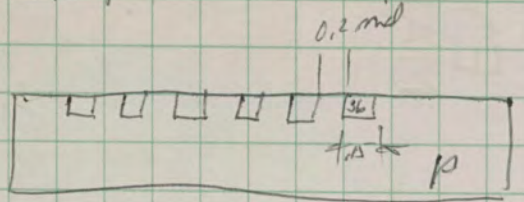


to make



 Epi structures, cont

FET



grow 3μ of P-type

After growth there is no evidence of lateral growth.

There are detailed run sheets on everything.

On oxide masking, pinholes in the oxide are a problem.

Oxide masked structures:

None have been done on cut and fill.

Things we would like:

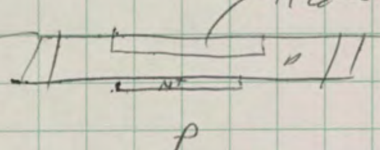
R. Craig 1. Cut and backfill, pref with high doping layer growth (see p. 90). — aim at epitaxial isolation replacement.

H. Ruegg 2. Grown bases for good Xstors.

for Orwick 3. Inverse epitaxial for power Xstors

4. Power Xstor - need 35μ min for switch back problem.

G. Poecher 5. Upside down Xstors (both grown & diffused base)



$\beta_{S+C} \cong 1/2\, \beta_N$

This is an important device in my estimation

G. Poecher 6. ~~High~~ very close control of thickness inc. outdiffusion of substrates

for Orwick 7. High ρ N-type growth, >20 Ω cm.

~~7. grow thick N on P~~. Cut and backfill for isolation.

INTERNAL CORRESPONDENCE

FAIRCHILD SEMICONDUCTOR

A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

TO: List

DATE: February 22, 1963

FROM: Gordon E. Moore

CC:

SUBJECT: Agenda for Project Review Meeting
Tuesday-2/26, 9:00 a.m.
Special Epitaxial Device Structures

The purpose of the meeting is to discuss and plan efforts to make advanced device structures not presently needed specifically by device development projects, but of interest when capability is established.

Agenda:

9:00		Wigton & Yim on special structures that have been made with photos and data.
9:30		Group discussion of other structures of interest.
10:30		Preparation of plan to make certain structures and assignment of device development responsibility to evaluate or use after structures have been shown feasible.
11:00		Adjournment

Please have all data summarized for efficient presentation.

Gordon E. Moore [signature]
Gordon E. Moore hb

GEM:hb

List: (Participants)

A. Davis
P. Ferguson (3)
V. Grinich
T. Sah
H. Wigton
E. Yim

SUMMARY OF PIPE REDUCTION AND ROBE EXPERIMENTS

Exp'mt No.	Objective	Method	Decision to Make	Results	Analysis and Remarks
1.	Determine pipe density and oxide thickness as pipe increments during processing.	Use 3, 5, and 7 fringe thicknesses, and observe pipe density as processing proceeds.	Relation of O_2 thickness to pipe density or pipe occurance at various processing stages. (4200)	Conditions | T-70 % | Pipe increase between Diode & T-70 | D.S. fringes 6-3/4 | 80% | 11% fringes 3-1/4 | 67% | 22%	Tests showed significant difference in both T-70 yield & pipe density increase
2.	Determine effects of oxide cut out slopes as dopant barrier at junction areas.	Use sloped and sharp oxide cutouts, observing differences in pipe density as processing proceeds.	Relation of oxide cutout sharpness as dopant barrier in function areas. (4200)	slope cut out | 72% | 18.5% sharp cut out | 76% | 8.5% standard	Tests shows significance in pipe density increase.
3.	Determine if boron doped oxide is permitting faster diffusion of phosphorous than believed, such that doped oxide is not an efficient phosphorous mask.	Compare original boron doped oxide pipe density with stripped and regrown oxide after base and emitter diffusion.	Effectiveness of doped oxide as a mask against phosphorous. (4200)	Due to complication of channel formation test was abandoned. No further tests planned.	
4. (Item 9 of Moore list)	Determine if a thick oxide before boron doping of oxide is effective as oxide mask against phosphorous doping (compliment to Exp'mt 3).	Compare thick and thin oxides for pipe density after phosphorous diffusion.	Effectiveness of oxide thickness as compensation against phosphorous penetration of boron doped oxide. (4200)	O_2 thickness | T-70 | Pipe Increase. Heavier Base Diff Oxide | 78% | 4.5% Std. | 76% | 8.5%	Heavier base oxide indicated a better mask against phosphorous diffusion.
5.	Determine if pipes near junction not detected in early processing expand by lateral diffusion into junction area.	Arrange oxide-steam time cycle to yield equal O_2 thickness, but different X, and longer diffusion times of two groups, forcing lateral expansion of "close-in" pipes into function area.	Magnitude of "close-in" pipes not detected at base diffusion on completed device. (4200)	Diff. Time | T-70 | Pipe Increase Longer Diff (4.5 hrs) | 78% | 4.5% Std. (3 hrs) | 76% | 8.5%	Longer diffusion showed no significant effect in pipe density increase.
6.	Determine amount of pipe-type contamination is associated with Ni plating operations.	Compare groups with Ni plated vs. no nickel, and Ni plated vs. Ni evaporation.	Magnitude of pipe generation associated with Ni plate solutions and possible alternate nickeling procedures.		

Page 93 NPN Simplification Process 12-31-62

Original Objectives	Process Steps	Condition
1- High Yield	1- Diffusion	1- Std. Diffusion
2- Low cost	2- Masking	2- Std. Masking
3- Process cycle time	3- Cleaning	3- Unknown
	4- Ambient	4- Bad.

Method used

1- All Std Diffusion Practices
2- All Std Masking Practices
3- No in Process testing or cleaning, Cycle time = 5 days
4- Wafers KPR coated when not in Furnace.

Results

1- Yield As Good or Better than Std.
2- Cost Low, due to Yield and Short Process time

NPN Simplification Process 12-31-62

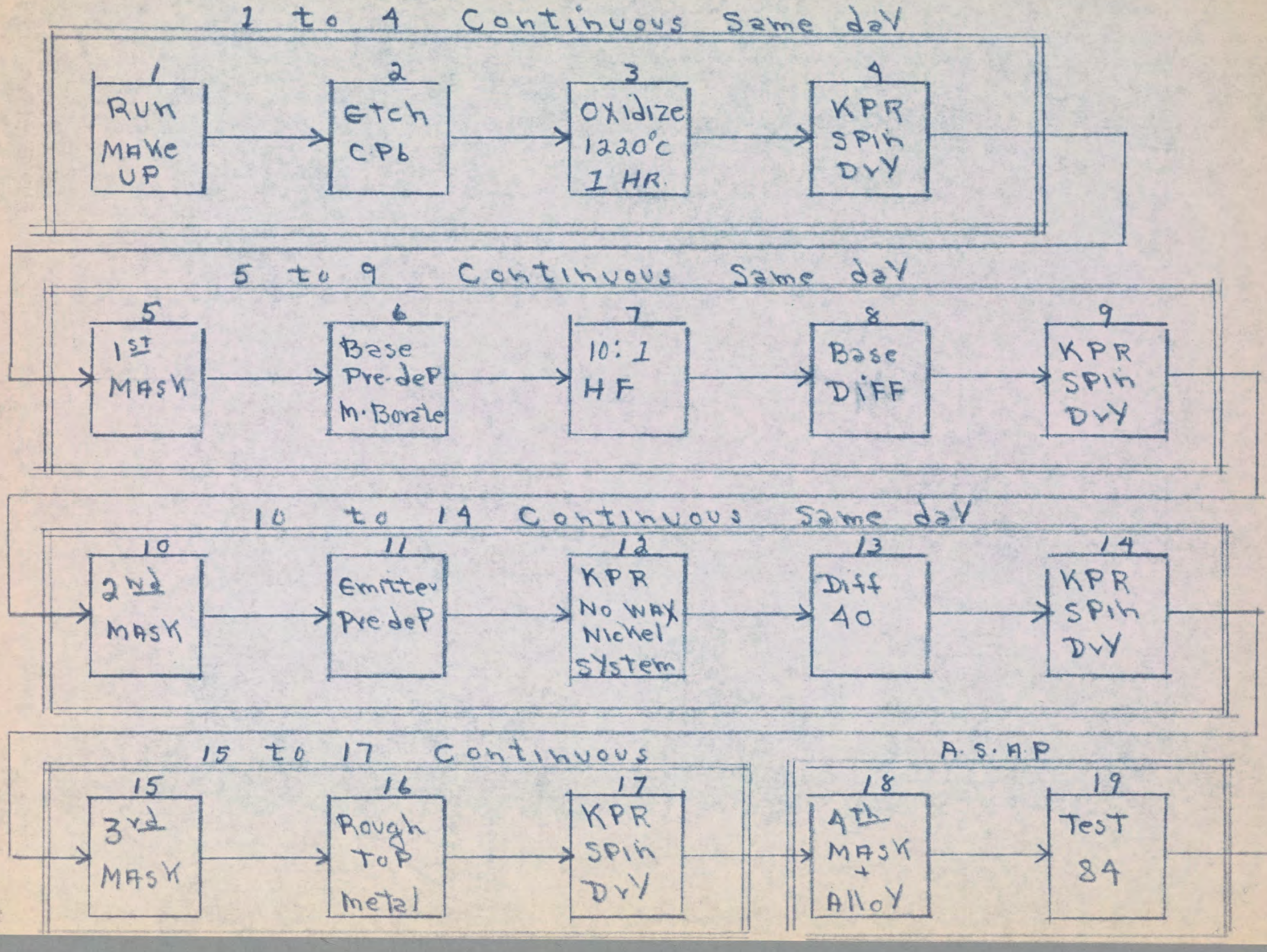
No in Process testing or Cleaning

Total Time cycle For Wafer Fab = 5 days

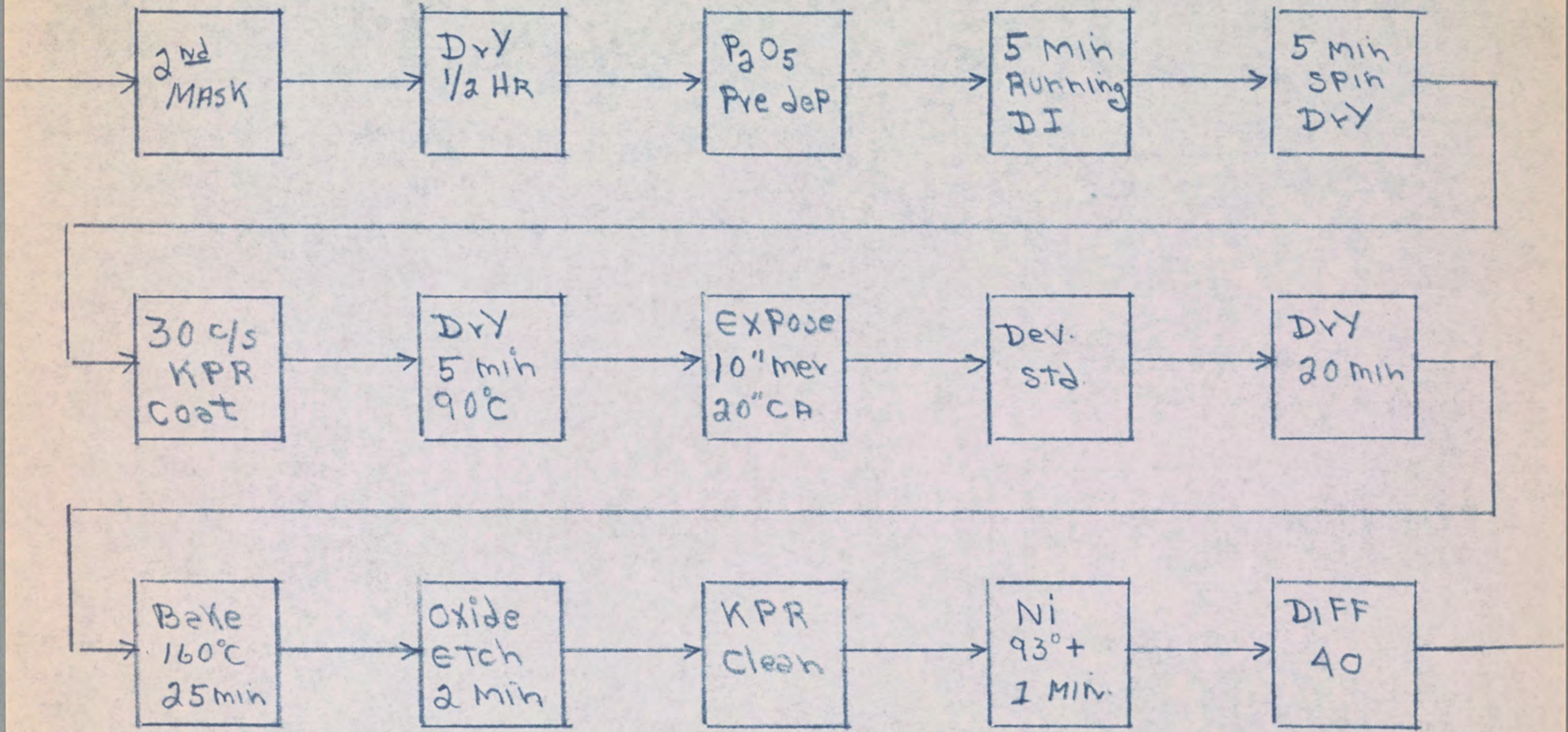
Item	Comment
1.	Run size will be equal to Base Pre-dep. Limit
2.	Will be Loaded direct to oxidation Boat
3.	Steam Flask cleaned For each run.
4.	Air dry in dark, dust Free container.
5-	Masking operators start at 0600
6.	Base Pre dep Boat Loading done in Masking Room and carried under cover into Furnace.
7-8	Std. Process
9	Same as #4
10	New Mask
11.	Under cover direct from 2nd Mask
12.	K.P.R Nickel Process in Place of Black Wax.
15	Direct to TopSide metal, No Testing
16	Rough Al metal System
17	Same as #4
19	Only Testing Station in Process.

NPN Simplification Process

EJK



NPN Ni Plate



Ed K.

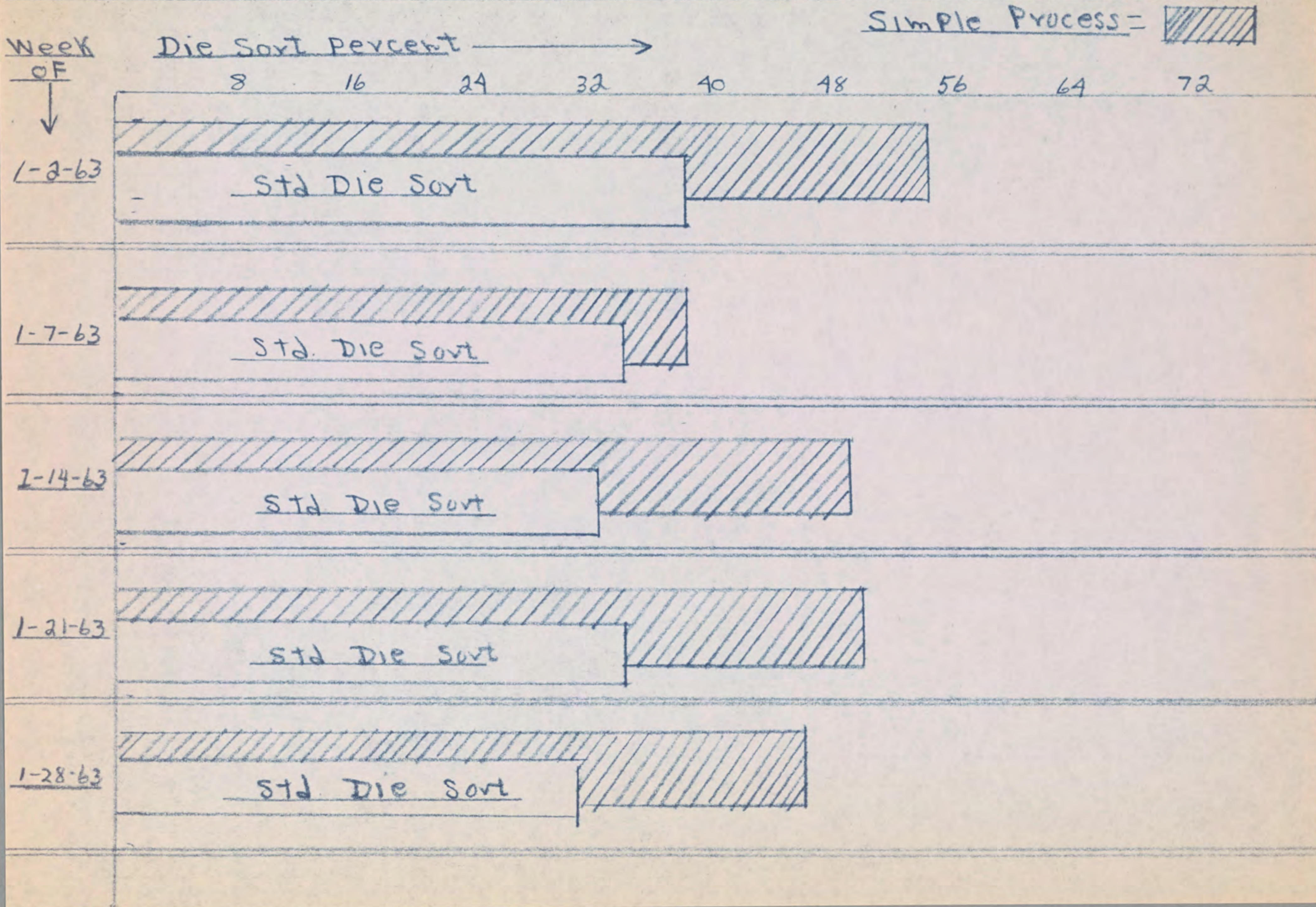
Simple Process

Die Sort Sample BY 4200 Line

Run#	Die in	E.C	E B	Soft	Pipes	Good	%	FACTORY Week Ave
EK#1	531	25	20	57	132	297	54	38
EK#2	412	60	6	54	132	160	38	34
EK#3	210	17	1	5	83	104	49	32
EK4-A	400	—	3	15	185	187	46	34
EK4B	400	10	5	15	150	220	55	
EK5-A	300	34	8	41	98	119	39	31
EK5B	602	75	10	43	154	319	53	
EK6	Rejected After Emitter Pre dep							Boron Pits
EK7	300	11	6	9	118	156	52	34
EK-8	Rejected After Emitter Pre-dep							Scum on Wafers
EK9								
EK10								

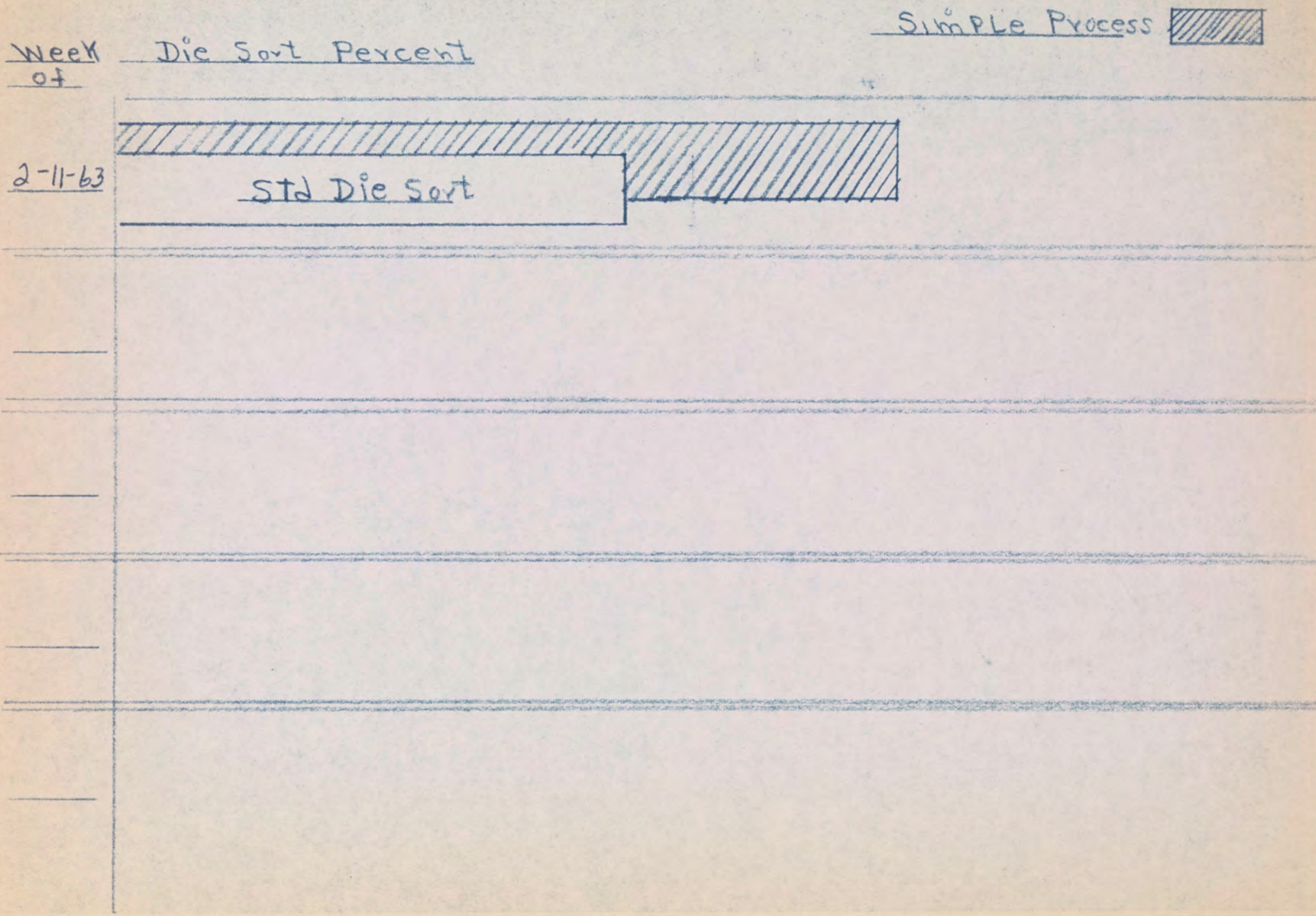
Simple Process to Std. 4200 Process

ALL Die Sort Data Obtained BY 4200 Line



Simple Process to Std. 4200 Process

ALL Die Sort Data BY 4200 Line



ROBE — Feb 25, 1963.

Ed ~~Kruegger~~ Hill Sang Fok Farrar Bleomo Moore Ferguson Orrnich

Paul presented a "pipe" picture we have found.

Sang

From data on oxide thickness, etc., a run was made to try thicker oxides, etc. A die sort yield of 62% was obtained.

Production has a very good correlation c̄ low breakdown & observable pipes.

Control line with minimal process - min residence time ~~30/57 pipes fails~~ ~~10% pipes rested~~.
The percentage of pipes in die rejects is then showing only 10% of rejects.

~~Agenda for~~ Paul Hill & I will get together to discuss an adgenda for a meeting in 4 weeks.

 Feb 26, 1963 — Structural Changes on PNP's

Dummerill, Sang, Hill, Waring, Bytheway, Lewis, Duffek, Tarp, Smithfield, Grinich, Ferguson, Sah

Carlson:

1. What is the effect of Ga.

The Ga cycle: (done after 3rd mask)

5 min preheat in N_2

Measure BV_{CBO} @ 5 ma and 50 μa
I_{CBO} @ 1 2 20 v

Before have channels in μa or ma range

One device:

Cycle soak	min pull 5 ma	50 μa	β (Alma Tyl)	I_{CBO} @ 1 v	2 v	5 v
0 – H_2 only – !	59	53	50	—	—	—
0 – N_2 only – 1 min	17	14	44	44	68	x
0 – N_2 " – 1 min	38	31	80	1.2	3.8	100
at 10 min @ 950° !!	41	38	90	1.2	3.6	100

Others behave similarly – "long" H_2 soak help I_{CBO}.

Len Carlson feels comfortable on 7500's @ 60v LV_{CEO} — he bases this on essentially dry life test data.

Typically β's go up on Ga treatment, down again on alloy, the 80% is not recovered

Why not a long pre-diffusion for oxide trim.

2. Oxide trimming.

At O_2 has no curve-tracer-visible channels, but they are there.

From C_{OB}'s on 4515's (2.5 Ω cm)

	0 v	10 v
nontrimmed	90 pf	12 pf
trimmed	43 pf	12 pf

58 devices, narrow spread!

INTERNAL CORRESPONDENCE

FAIRCHILD SEMICONDUCTOR

A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

TO: List

DATE: February 22, 1963

FROM: Gordon E. Moore

CC:

SUBJECT: Agenda for Project Review Meeting
Tuesday-2/26, 3:30 p.m.
PNP Channel Problems

The purpose of the meeting is to review the effects of structural changes which have been made and evaluated in planar PNP devices in an attempt to eliminate the channel problem and planning of program to evaluate other structural changes in the light of various models of channel causes.

Agenda:

3:30	Statement of problem and review of prehistoric data - (Moore).
3:40	Review of more recent data on oxide cut and gallium treatment - (Carlson).
4:00	Summary of life testing results with respect to channels on 1740 and 4511 - (Reis or Grutchfield).
4:30	Discussion of other hard data from group.
4:40	Discussion to generate structural changes worth considering from group.
5:00	Preparation of plan to make and evaluate recommended structural changes.

Please have all data summarized for efficient presentation.

Gordon E. Moore

Gordon E. Moore

GEM:hb

List: (Participants)
L. Carlson
P. Ferguson (3)
V. Grinich
H. Grutchfield
L. Reis
T. Sah (3)

$ — a monopoly we are about to lose
Effort — aimed at understanding, not at ~~for~~ PNP fix.
Competition
40 W solution
Automation ~~[illegible]~~ program · on posture.

The double break is not associated with trimmed oxide.

3. Of 10 units with trimmed anodic oxide ($BV_{CBO} \sim 30v$)
5 developed 0.1-0.3 ma channels during life.

Crutchfield

1740 - 1741 The only channels he has ever seen are when Ga was purposely left out.

4511 Op @ 800 mw, free air
100°C, reduced pwr
150°C, CB bias

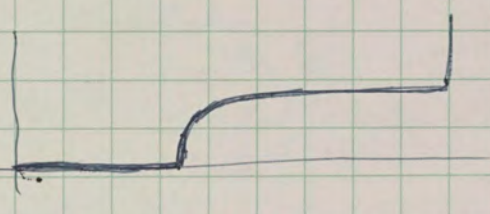
All of our PNP's were put on same condition. Only the 4511 and 1712 developed problems

The Ga treated units show a large increase of low current h_{FE} on aging (~~say~~, e.g., 300°C).

4511 (Ga treated)
induce channels by power life
eliminate them by 300°C age

3511 didn't change

A lot of the channels get to be



(~~Lewis says this is a pump out effect~~)

Competitor devices: T.I., Hughes, Sperry — have channels, don't grow (1 mil μa - 10 mya, stable, they not much change)
Motorola is going fast.

Sang has done a run that uses Au metal, no Ga and has no problem(?) yet. These are 1741 200,300 mw, 200, 300° storage. These run in the 20-30 v range mostly with a few to 60 v.
Heat treatment in 1000° ~~amA~~ after every diffusion step.

Al onto Si: before diffusion — no good result.
Pyrolytic & Anodic start — channels
Monoxide — in mill
~~Can not put monoxide on finished devices~~
We now have monoxide over 4511's to try - had
Anodic
Thermally

 Small Geometry product planning Feb 27, 1963

Sprik, Ysart, Noyce, Grinich, Lewis, Valentin, Schultz, Knudsen, Sexton, Laman, Ferguson, Moore

1312 — This has a 150°C I_{CBO} problem. This is evidently common to all epitaxial units. Other problems are only spacing — get 85% class; get 70% old 2N #'s

1311 — Hot I_{CO} unit meet 2N709 — about 10% fail the 150° C spec. These can't be correlated out.

1211 — Wiped out completely on hot I_{CBO} on these. 1210's must be made again

3111 — A basic spec today — It has a hot I_{CBO} problem

30v CEO
60v CBO
500 ma β @ sat 1v
40 nsec 40 ns off
200 μa, 150° I_{CBO}

To meet this, we must drop our CEO 750 off.

Our 20-30 volt units will meet all "the doubletooth" specs.

0002 — This is a 35 mil die. There is an epitaxial material problem. On nothing but our (R&D) first material was there a good yield.

0000 } — Not being pushed at Mtn View, but dice will be out on ~~the~~ next Monday.
Aim @ 5000 / mo in plastic by May
Make some in "M" package

0001 — Waits for strip line package.

FET — We are sick still — next ~~time~~

1221 — Nothing but evaluation of what we now have.

1450 — Doesn't look like much. — or does it?
40-100 at 100 μa (55°) (d.c. β). If we look at a.c. β, it looks good at 100 μa. VHG thinks it should fly.

1250 — Fly

1340, 1341 — Would like a unit whose fallout is 708 matched
Our best yield of 1340 is ~40% yield to 2N708.

CDC core driver - no yield. We will make a mask for an intermediate. We will design mask, nothing else.

PNP

4511
3511
1713

4511 ~~Most~~ Minuteman business can take 40 v BV_{CBO}, LV_{CEO}. We will run some 40 v ones. You will get us some that have developed channels for photo-resist work.
There is a real potential problem on ~~BVEB~~ V_{BE} in the glass package.

3511 — A production product 2N2695, 2N2696.

1713 — It is producible @ f_T of 400 mc.

There is evidence of a channeling problem.
400 mw, 25 °C case
200 mw in set
200 °C storage
} ok

165 °C ambient, 10 v V_{CB}. These developed small channels.

1702 — Wait until we find out what field acceptance is. It is just a new mask on 1713.

6205 — Dead
6206 — 80 v LV_{CEO}, (15 watt device) @ 200 mw
This has the old switch-back problem.

Competition - TI - 2N1560 (and Transitron) — obsolete

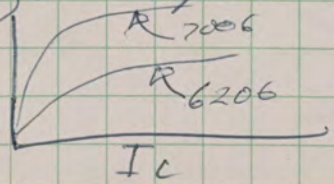
(- 18th of March on 1 gun machine)

TI 2N2150 (a 2 amp device
M.H. 2N2634 (good amplifier to 2 amps)

The 6206 has a double break type set @ 2 amps which is undesirable.

We will make 6206's, ~~on~~ spec them, and sell them.

Spec the thing Power



Power, cont.

7006 — in 9/16

SCR (small) IBM high sen. — easy device.
Accord to Valentine, IBM requirements of size are not before late 3rd quarter. We will shut down on this one after the first 500 units.

SCR — (3 amp, 400 v) — Leave demand @ R+D. This looks like two months.

7500 — No action.

NPN — Large geometry

4011/16
4201
> A couple of split runs in now. Out in 4 weeks.

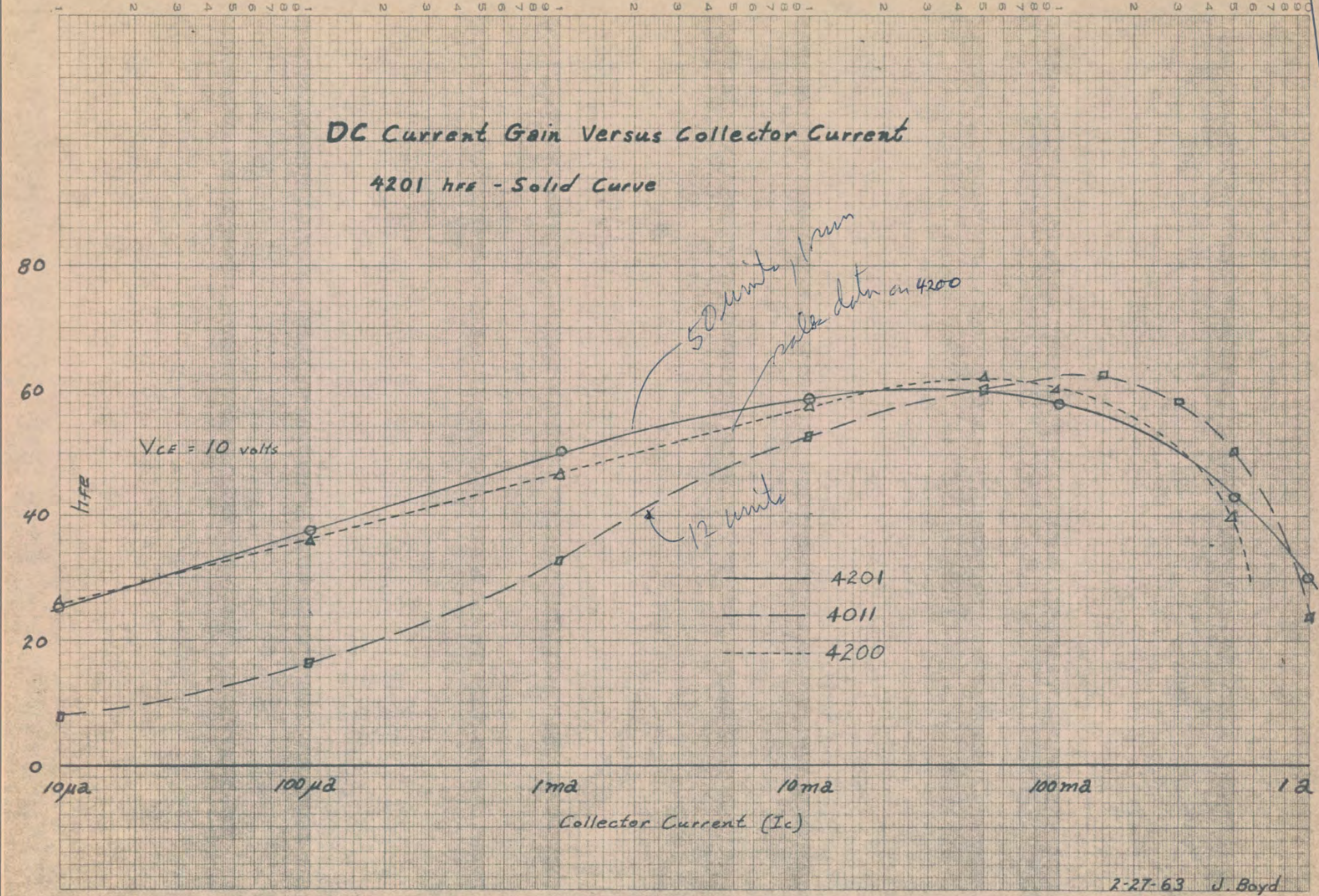
We will look at some of the bad 4011 that production has made ~~[illegible]~~ with infrared.

We are now worried about the low current β problem.

We will grind out a optimum family recommendation across everything. Schultz, Ferguson, Grinich, Moore, & Graham. For report in next meeting.

4111 — Being run, 1 run. It came out of the woods.

150 mc 4205
4207 — For various things. — Being run.


DC Current Gain Versus Collector Current
4201 hFE - Solid Curve
50 units, 1 run
sales data on 4200
12 units
VCE = 10 volts
hFE
80
60
40
20
0
10μa
100μa
1ma
10ma
100ma
1a
Collector Current (Ic)
4201
4011
4200
2-27-63 J. Boyd

SCD $\frac{25°C}{150°C}$ N^+ type Summary.

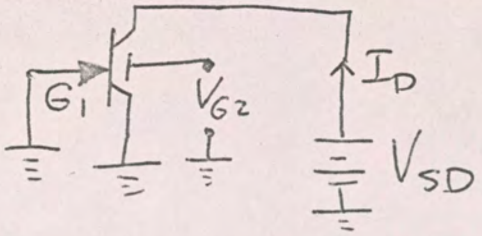
$V_{EB} = 20v$

Run	No. Unit	V_{go}	$I_{t=0}$ ma	%ΔI 100 hr	%ΔI 1000 hr	I_j (10v) junction 0 hr	I_j (10v) junction 1000 hr
62-11-10A getter	3	−4	7.2	−26	−33		
1100°C 11 min Steam	3	−8	1.9	−25	−34		
$+O_2$, 40 min dry N_2	3	−12	.88	−55	−75		
62-11-10AA	3	−4	7.5	−5.	−6		
getter same above	3	−8	5.3	−7.6	−12		
plus 1100°C 15 min CO	3	−12	1.8	−2.8	−9		
62-11-10B repeat 10A above	1	−4	1.808	−2.7			
62-11-10BB repeat 10BB above	1	−4	6.49	−0.8			
62-12-3A 1100°C 15 min (N_2)	5	−4	8	−8	−16		
3B 15 min (O_2)	5	−4	3 μa	−6	−8	3.5 pa	3.4 pa
3C 15 min (CO)	10	−4	5 ma	0	0		
150°C V_{EB}=20v aging	1	−12	1.105	−32.1	−35.7	1.6 pa	1.6 pa
	1	−12	1.285	−10.1	−10.5		
Selected 3C (CO)							
clean appearance	5	−12	0.25	−6			
poor mask	5	−12	0.25	−12			
3D 25 min CO	5	−12	0.5	−26			
3E 60 min CO	5	−4	2.5	−15			

① % large (A) Small ~~large~~ channel
(B) No CO
(C) higher V_{go} with No CO

SCFET Summary

$V_{G1} = 0$



Run	No. unit	V_{SD} volts	V_{G2} volts	I_D ma	% I_D 100 hours	220	1000	T C°	I_{G1} SD 0hr	I_{G1} SD 138hr	220	1000
62-11-7B anodic	5	10	-4	0.25	-0.9	-6	-5	25°C	0.02na			i-300na
					13	15	41					
					11	-1.4	0					
					18	9.6	-22					
					2.7	-5.2	-5.1					
62-12-1A CO gettered	5	10	-12	1.4	0	-4	0	25				
62-12-4A CO gettered	5	10	-12	1.2	-0.9	0.		25				
				3.5	-0.6	0.						
62-12-1A	5	10	-12	1.5	-40			150	2.6na	1.6		
4A	5			2	-20			150	0.1na	0.1		

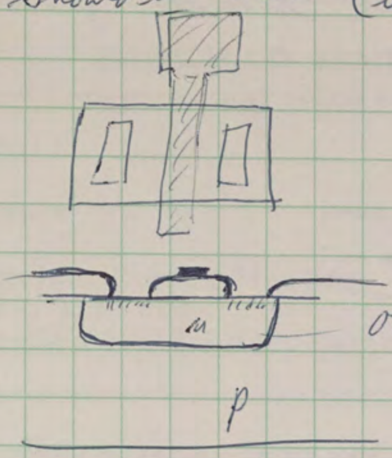
Feb 28, 1963 — SCT ~~Field Effect device~~ Should be SCD (ie, MOST)

Sah | [illegible]
Waring | Duffek
Wanlass | Lewis
Tremere | Bittmann
Leistiko | Grinich
Ferguson | Seeds

Leistiko + Tremere

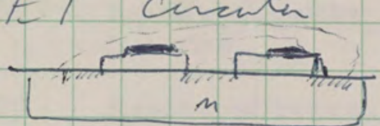
Three devices

1.

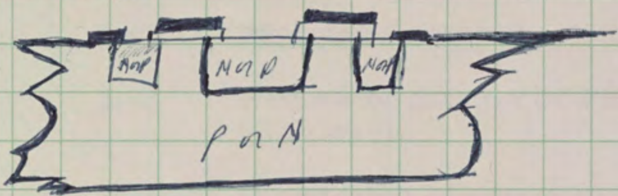


outdiffused or epitaxially grown channel.

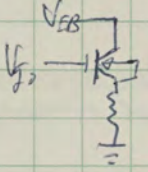
2. SCFET circuits



3. SCD



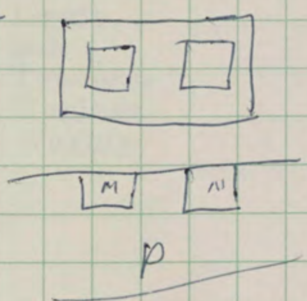
The three have the same general drift with time



All the SCD's made to date are "NPN" with a large channel at $t=0$. — This is thought to be a dirty furnace tube.

On all these structures the 15 min CO gettered units didn't drift at max. −4, −8, −12 volts on V_{go}, room temperature. This is 1 ~~[illegible]~~ run data.
For longer CO treatment, the data is not so encouraging.

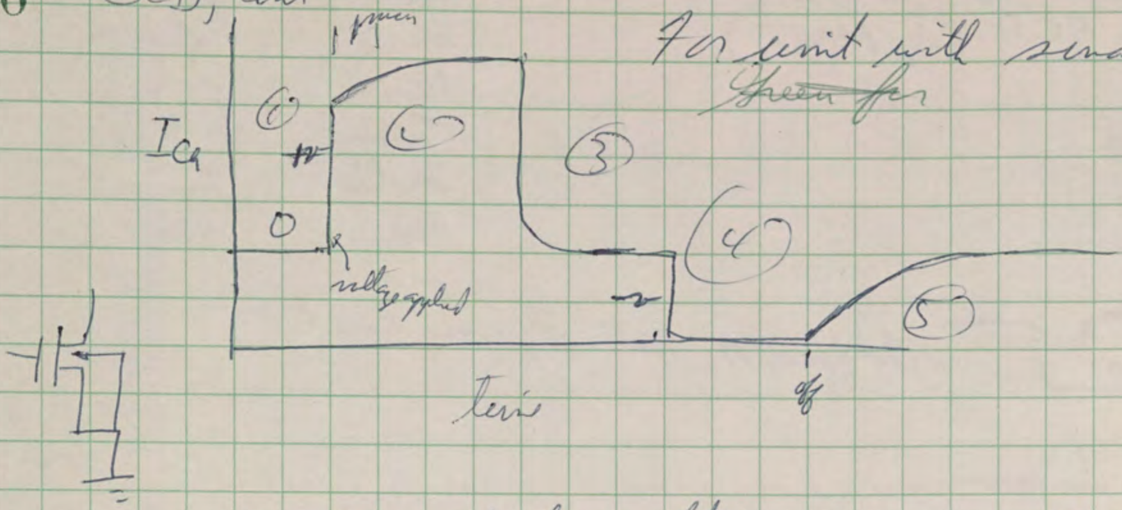
Lewis



with two type field electrode
a) not over junction
b) over everything

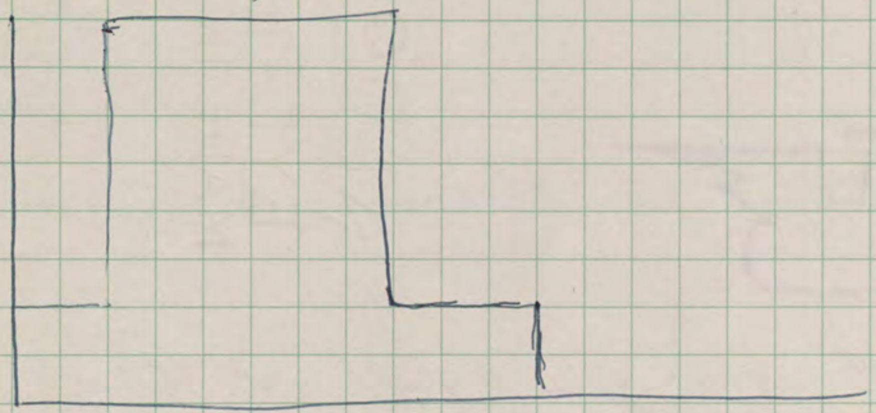
 SCD, cont

For unit with small field probe
~~Screen for~~



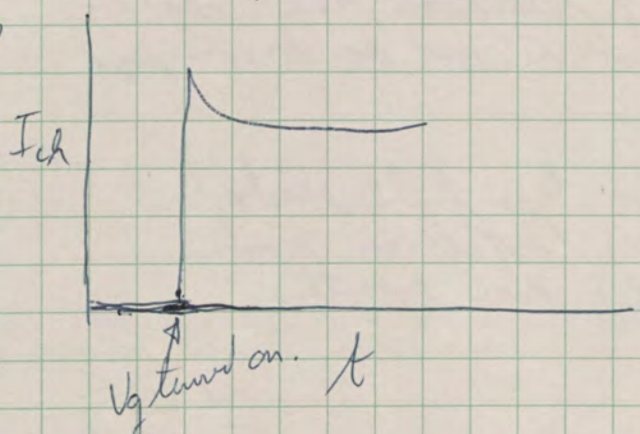
can get to condition in region 5, we can get the case where it takes a while for conductance to return.

For large area gate



Art Still claims that the correlation between drift and imperfection is definite. He still swears by his hole aging experiment.

First PNP's with no $V_g = 0$ channels have looked at show the opposite type drift, i.e.,



Suddenly this (except the step) looks like ion drift on the surface. It is possible a ambient problem.
We should tie this down to an ambient effect if possible —
Lewis is co-assigned — Confirm to WW in writing.

INTERNAL CORRESPONDENCE

FAIRCHILD SEMICONDUCTOR

A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

TO: List
DATE: February 22, 1963

FROM: Gordon E. Moore
CC:

SUBJECT: Agenda for Project Review Meeting
Thursday-2/28, 1:30 p.m.
Surface Controlled Field Effect Devices

The purpose of the meeting is to review progress which has been made in making stable surface controlled field effect devices and to plan program both with respect to individual devices and integrated circuits.

Agenda:

1:30	Review of recent data on reliability - (Tremere and Leistiko).
2:00	Review of recent data on reliability and old Rabinovitch data - (Lewis).
2:30	Group discussion of reliability data including what additional tests need to be made.
~~3:00~~	~~Plan for work to be done on SCFET.~~
3:45	Review of data on SCFET integrated digital circuitry - (Wanlass).
4:15	Discussion of potential of integrated SCFET circuitry.
4:45	Plan for additional work on SCFET integrated circuitry.

Please have all data summarized for efficient presentation.

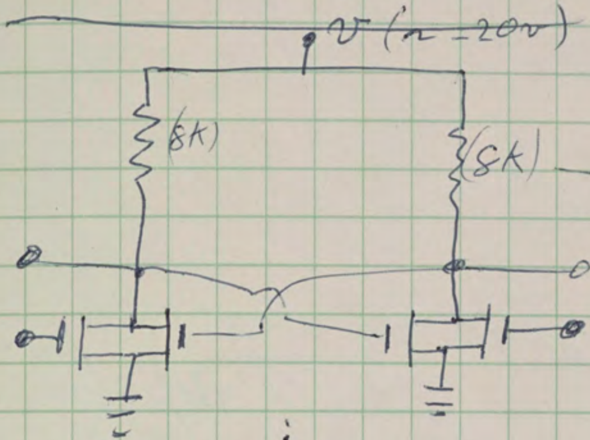
Gordon E. Moore
Gordon E. Moore hb

GEM:hb
List: (Participants)
P. Ferguson
V. Grinich
O. Leistiko
A. Lewis
T. Sah
D. Tremere
F. Wanlass
W. Waring

Wanlass

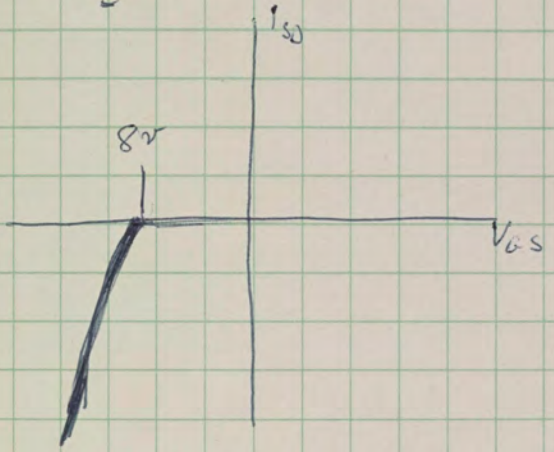
Wanlass has stored some of these @ 300°C and finds that they go stick - side - side at with Au. Ones with Al bonds are much better (ie, non-catastrophic), but still drift.

Frank Wanlass



Principal problem is the need for high resistor because of high voltage.

Made of same diff as diffused islands. These are made of 0.2 mil stripes.

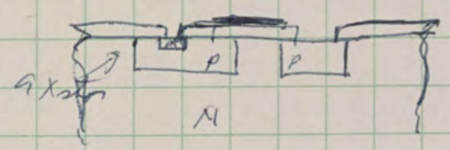


>90% were "good" on a wafer — (ie, they flipped)
only 50% after canning

A 1μsec pulse flips them.

→ Get some electronic evaluation help for Frank!

If you make



, one gets β multiplication

Micrologic Product Meeting: March 1, 1963, March 4, 1963

We send ~ 75 wafer / wk., ~ 50-50.

We will send all our excess S's in wafer form.

In 3 weeks 1st G's come out.

They are starting 2 runs / day this week
3 " " next "
4 " " follow "
5 " " " "

For now send A.E. at least 100 units (functional) for their preliminary evaluation. This should take until 3/6/63.

To Applications:

R&D units G's 100 from total of 6 runs
Prod " G's 6 runs

R&D units S's 100 from total of 6 runs
Prod " S's 6 runs

P-105

CUSTOM CIRCUIT SCHEDULE

Responsible engr	PROJECT	Breadboard	Masks In	Runs Started	Units Out	Unit Requirements	REMARKS
D.F.	1. Autonetics dual NAND gate	-	-	-	3/22		
H.R.	2. Litton VAX NPN driver	3/29	4/5	4/19	5/17	80	60v
J.S.	3. Litton VAX preamplifier	4/5	4/12	4/26	5/24	80	
J.S.	4. MIT sense amplifier	4/12	4/19	5/3	5/31	100	
H.R.	5. Litton VAX NPN/PNP driver	4/26	5/3	5/17	6/14	80	
J.S.	6. Litton flip-flop - Chip A	5/17	5/24	6/7	7/5	80	
J.S.	7. Litton flip-flop - Chip B	5/17	5/24	6/7	7/5	80	
J.S.	8. Rem-Rand 3-input buffer	6/7	6/14	6/28	7/26	100	
H.R.	9. Autonetics general purpose amplifiers					0	R&D test vehicle
	10. Autonetics power switch					0	Finish chips

3/19/63

INTERNAL CORRESPONDENCE

FAIRCHILD SEMICONDUCTOR

A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

P-105

TO: List

DATE: March 21, 1963

FROM: Gordon E. Moore

CC:

SUBJECT: Custom Integrated Circuitry Group

This is to announce the formation of a Custom Integrated Circuitry Group in the Device Development Section.

The purposes of establishing this group are as follows:

1. To train a nucleus of people for the design and production of custom integrated circuits.

2. To supply sample quantities of custom integrated circuits on an interim basis.

This group will report to Phil Ferguson. John Sentous, on assignment from Mountain View, will be Group Leader. He will have responsibility for:

1. Scheduling and producing custom circuits using R&D fabrication and Mountain View assembly insofar as possible.

2. Arranging for capability in Mountain View to take over this custom circuitry in late 1963.

The technology employed in making these custom circuits will be restricted to that which we are reasonably confident will be ready for transfer to production when the facility is installed. R&D will define the boundaries of this technology.

It is possible that other custom circuits will be made as test vehicles to allow R&D to experiment with the inclusion of new technology. In such cases, these circuits will be the responsibility of regular R&D personnel.

The pilot line capacity to be committed to the custom circuitry group is that necessary to start ~ 150 wafers per week. New masks at a rate of ~ one every two weeks can be accepted by R&D mask making for custom circuitry needs.

Since only circuits upon which one can expect production-worthy yields will be accepted, this should result in adequate samples, both for internal evaluation and for delivery of quantities up to ~ 100 to customers.

Gordon E. Moore

Gordon E. Moore

GEM:hb

List

R&D:		M.V:	
J. Blank	H. Perkins	T. Bay	J. Sentous
P. Ferguson	T. Sah	R. Graham	C. Sporck
V. Grinich	I. Solt	R. Noyce	D. Yost
J. Kabell	W. Waring	M. Phelps	
H. Leifer			

INTERNAL CORRESPONDENCE

FAIRCHILD SEMICONDUCTOR

A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

TO: Jack Kabell
Phil Ferguson

DATE: March 4, 1963

FROM: V. H. Grinich

CC:

SUBJECT: Project Review Schedule on Photo Transistors
Tuesday, March 5 at 3:00 p.m.

Please prepare a written summary on the following material with the schedule given below:

1) Chip fabrication with yield information and process permutations.

2) Packaging status and proposed variations.

3) Hard reliability data.

We would like to have 10 copies of all hard data available for distribution at the meeting. The schedule calls for:

3:00-3:15 p.m.	Discussion on Fabrication by Warren Wheeler
3:15-3:45 p.m.	Packaging Discussion by Jack Kabell
3:45-4:30 p.m.	Reliability Data by Jack Kabell

V H Grinich

VHG:ef

HEAT TREATMENT EXPERIMENTS ON THE YP3
(500°C, 1 HR, N_2)

originally sorted hard and >50v.

RUN NO.	REMARKS	NO. TESTED	PERCENT * CHANNELED	PERCENT WITH V_{CEO} < 40V.
26	Ni	6 dice	0	17
30	Ni	7 "	43	28
32	Ni	8 "	0	12
38	Ni; 20% yield	6 "	33	83
38A	No Ni; 11% yield	10 "	20	30
39	Ni	10 "	10	30
50	No Ni; 20% yield	10 "	0	30
50A	No Ni; pyro. after em. diff.	8 "	0	38
49A**	Before Al; one chip.	38	0	V_{CEO} of all units increased slightly and breakdown hardened.
49A**	Closed ring oxide removal around base; before Al; one chip	34	0	
49A**	Closed ring; Al dot on emitter.	27	0	

*Actually, percent with channel currents ≳100na.

**These were baked at 530°C instead of 500°C.

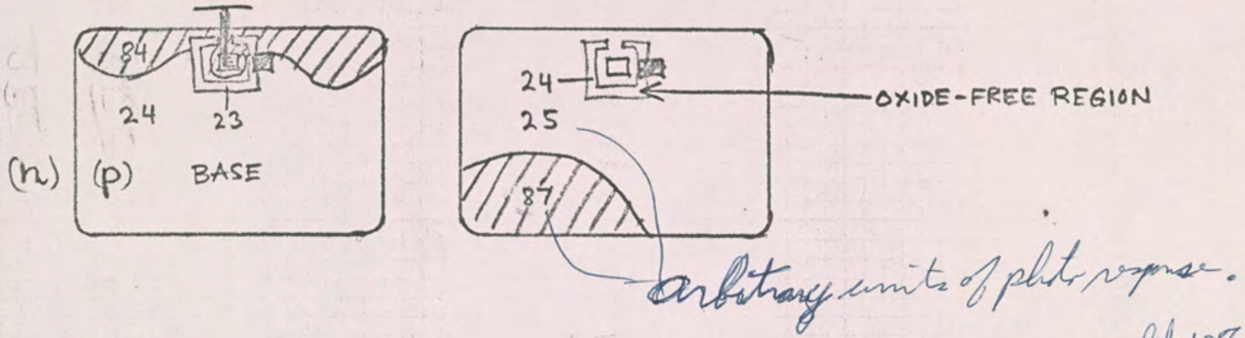
Only these units had not seen the 300° for 18 hrs die stabilization

RHW
3/5/63

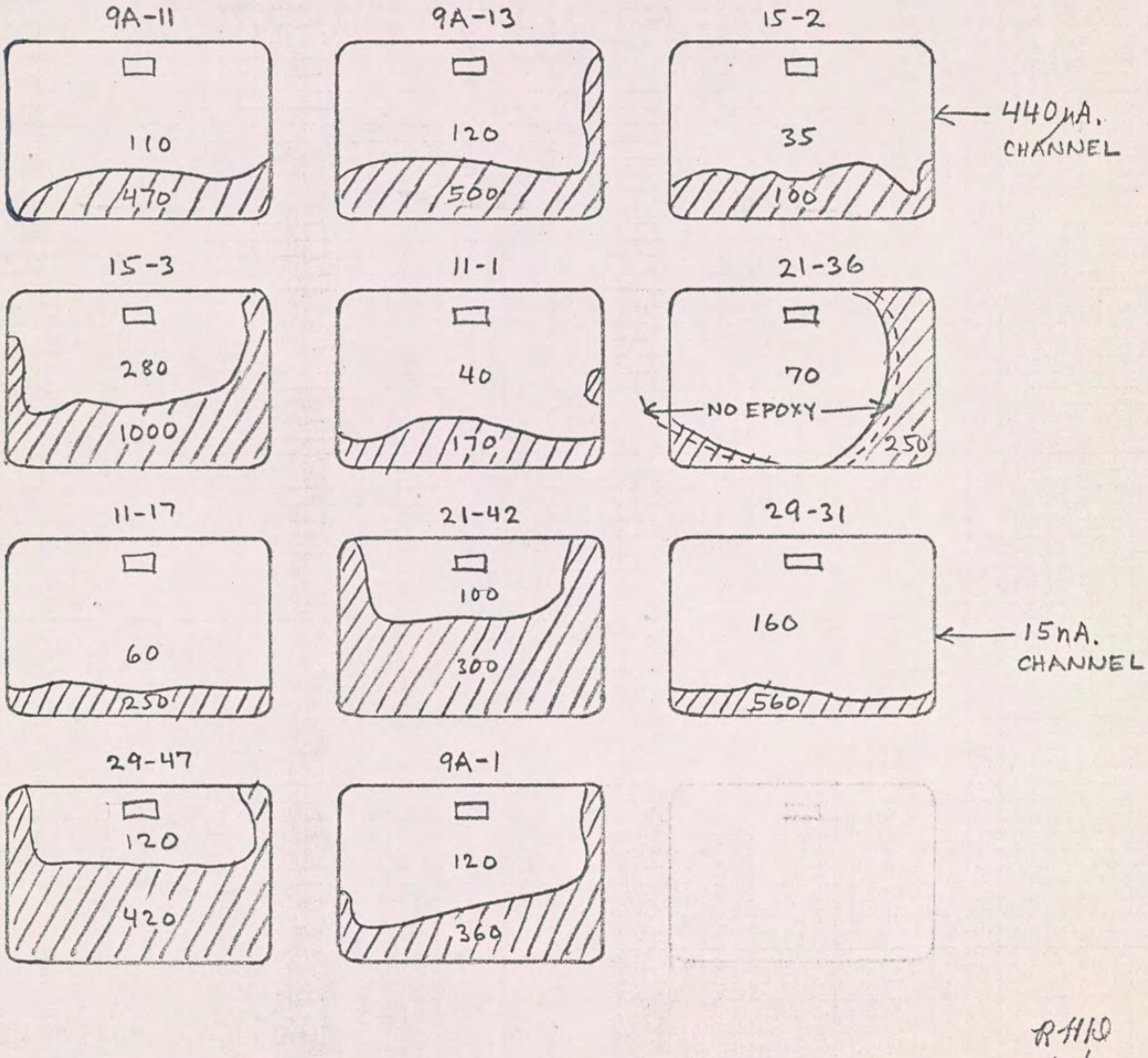
CHANNEL POSITIONS IN YP3 FAILED UNITS

METHOD OF DETERMINATION: BLUE LIGHT SPOT PROBING. (2μ penetration) ////// – CHANNEL

I. UNMOUNTED DICE BAKED AT 500°C FOR 1 HR IN N_2. RUN #30

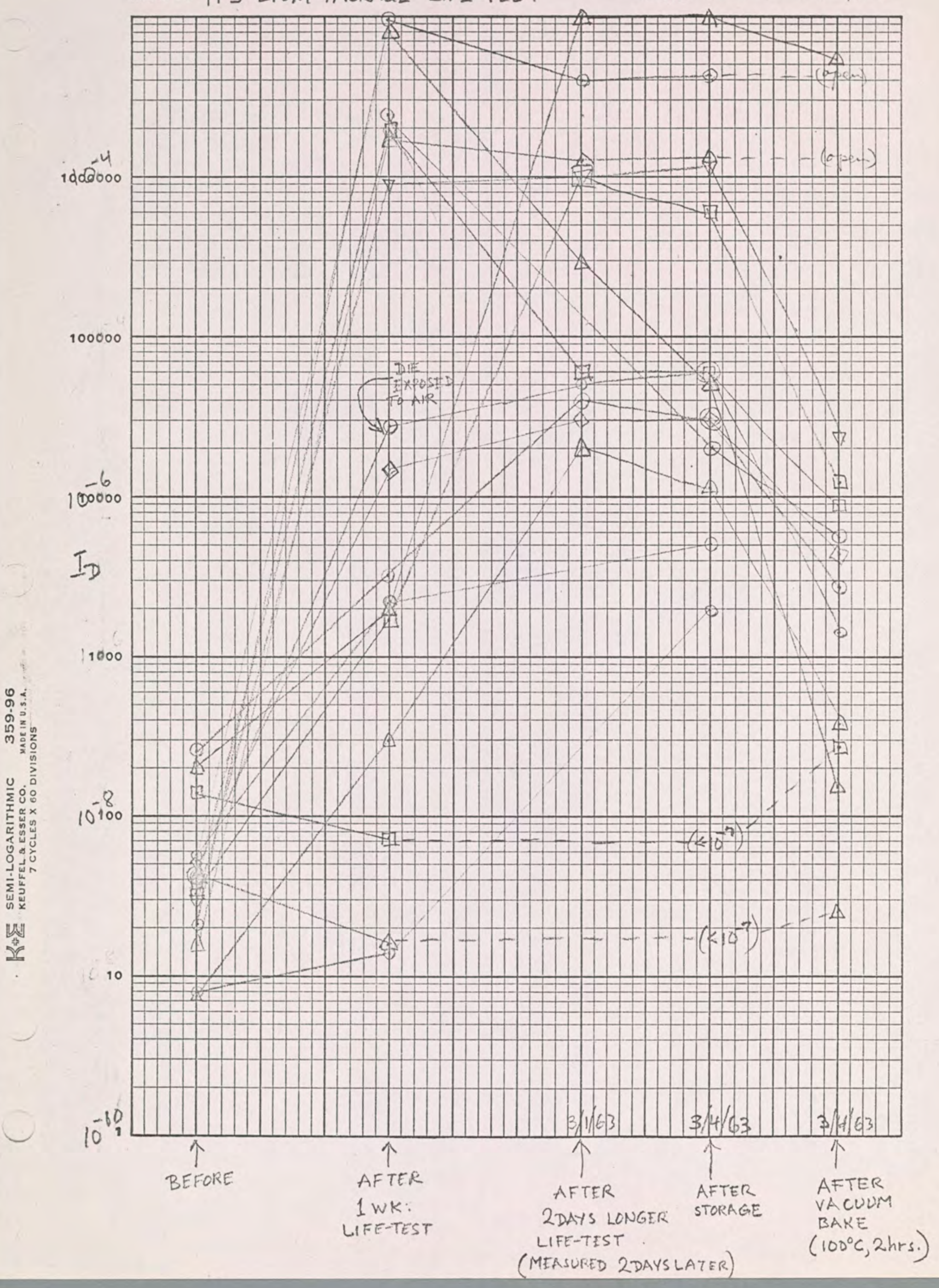


II. EPOXY-PACKAGED UNITS LIFE-TESTED AT 85°C FOR 9 DAYS (~~100%~~ more like 10% HUMIDITY, ~100 ft-c.)



RHW
3/5/63

MODEL YP3 EPOXY-PACKAGE LIFE-TEST DATE BEGUN 2/18/63



RHD
3/5/63

Ref: p. 103

YP-3 PROJECT REVIEW

Chip Fabrication

Fifteen runs of YP-Series completed through Die Sort.

Yield data tabulated on separate sheet.

Runs after #29 have not been completely sorted and are being used for experimental purposes.

Chip Problems

- Softs after metal. Changed alloy to 550°C - 4 min. Was 580°.
- Shorts on packaging. Thin oxide - return to two hour oxide of XP-3.
- Al reaction with N+ and Ni region.

Experiments now in progress to determine causes of chip instability with temperature.

1. No metal over E.B. junction and oxide cut.
2. Metal vs No Metal.
3. Hot stage work and sectioning by W. Wandry.

DIE SORT YIELD AND P.K.G.

YP-#	% Die Sort	% P.K.G.	Classification
1	Lost at E.D.f.		
2	70%	56%	Soft epoxy
3	Lost at Experimental Silicone varnish		
4	Experimental complete ring - lost at E.D. and package experiments.		
5	Lost at E.D.		
6	52%	76%	57%
7	38%	64%	80% (Start life tests and IBM sampling)
8	Lost at E.D.		
9	Data not available	61%	87%
10	58%	53%	73%
11	52%	70%	89%
12	Lost at E.D.		
13	Lost at E.D.		
14	62%	Did not bond	(Changed to Bc-3)
15	Did not bond properly		
16	Base overdif.		
17	Channeled		
18	21%	Did not bond	
19	33%	50%	0% High Id
20	Lost?		
21	29%	39%	77%
22	19%	No bondable	Alloy trouble
23	15%	Not bonded	Alloy trouble
24	9%	Not bonded	Alloy trouble
29	51%	28%	96%
25	47%	33.3%	Experimental 550 Alloy P.K.G. - LTV + Glass

PACKAGING - HERMETIC

1. Silver leads. Mold pyroceram with Face Plate-lead bond okay - 560°C - Can't mold pyroceram.

2. Silver leads - Glass sandwich - Preform Block - Okay except (A) too expensive and (B) devices failed in devitrification cycle. Also IBM didn't like Ag leads.

3. Copper leads - Glass Sandwich - Poor bonding properties and bond strength.

4. μLogic Package - 48 dice from several runs packaged in flat package with standard aluminum lead attach, glazing and devitrification. Result - 2 dice electrically good. Failures randomly distributed between opens, softs, channels, shorts.

5. 48 Bare dice through devitrification cycle.
   Result - 27 no change - 6 soft.
   15 substantial decrease in V_{ceo}. (Creepers)
   (> 10%)

6. Now investigating cause of Heat Treat induced changes. (R. Dyck) - and possibility of short time high temperature bonding to Face Plate for composite Package.

PLASTIC PACKAGE

1. Channel Investigation indicates trouble starts at collector contact and spreads across base - (R. Dyck).

2. Teflon Jacket package being investigated.

LIFE TEST DATA

PLASTIC PACKAGES -

Run # 6 - 9 - 10 - 11	100% failed by CB leakage.
# 7	6 out of 20 failed by C.B. leakage.
Total	Of 90 units 74 failed by C.B. leakage.
To - 18 Package	23 units on test approximately 2000 hours. Data attached. 2 went open. One showed large increase in Id.
To - 5 and Epoxy	Data attached. 2000 hours. All increased in Id.

LIFE TEST HEADER MOUNT YP-3

	$3 Dec. I_1$	$1 March I_1$	$3 Dec. I_d$	$1 March I_d$
YP-3 -19	1.35 Ma	1.35 Ma	7.0 na	7.3 na
	2.40	2.30	.56	68 na
	1.65	1.75	2.2	1.8 na
	1.20	1.20	2.0	1.8
	1.20	open	8.1	open
	.82	.80	.70	1.2
-21	1.10	open	.45	open
	1.35	1.30	1.6	2.5
	1.70	1.40	1.9	3.2
	1.60	1.55	2.8	4.6
	2.10	1.80	1.6	4.0
	1.45	1.35	0.9	0.8
-14	.55	.55	6.0	6.0
	1.40	1.40	24.5	28.0
	.54	.45	16.5	16.5
	1.82	1.75	1.3	1.1
	.37	.35	2.0	.43
	1.25	1.25	6.0	5.8
-18	1.35	1.45	1.0	1.1
	1.20	1.38	18.0	17.0
	1.35	1.48	1.9	2.4
	2.10	2.15	2.3	3.0
	2.65	3.60	.52	.8

EPOXY ON HEADER XP-3

I_1 12/5	I_1 3/1	I_d 12/5	I_d 3/1
.30 ma	.30 ma	100 na	110 na
.28	.30	32	43
.72	.65	85	140
.23	.22	16	22
.35	.35	460	610

Room Temp. Set. Epoxy

RECEIVED
MAR 20 1963
GORDON E. MOORE

V. H. Grinich G. E. Moore March 19, 1963

Custom Integrated Circuit Schedule J. P. Ferguson

Attached is the schedule of presently planned custom integrated circuit work to be performed at R&D. You will notice that the Radiation and the IBM CML and DTL circuits are not included since the Radiation circuits are being done as information becomes available and the IBM circuits are actually proprietary products.

In general, custom circuits will be handled in the same manner as is proposed for the normal factory operation, i.e., with John Hulme doing the breadboarding and circuit checkout. This will include all circuits for which the necessary components have adequate epitaxial kit counterparts. At present, this will include transistors, diodes, resistors and junction capacitors and, within a month, should be expanded to include MOS capacitors and NPN/PNP combinations. While the custom work is being done at R&D we will consider every technique which has been shown to be feasible as fair gaime for use.

When a circuit is selected as a test vehicle, as in the case of the high voltage Litton VAX driver, it will remain the responsibility of Ruegg or Farina. All other circuits will be the responsibility of Sentous.

Since we are only able to commit 150 wafers/week into the process it will be desirable to cut off immediately any circuit which encounters problems of such a magnitude as to necessitate brute force as a means of completing the order. Also, repeat requirements will tend to reduce the number of new circuits which may be attempted.

There will be a status review every Friday morning at 8:30 at R&D between Hulme, Sentous, and appropriate R&D people.

JPF:jh
Encl.

March 5, 1963 XP-3 Project Review Meeting

Wheeler, Saddick, Brown, Saffky, Dyke, Ullman, Kabell, Grinich, Ferguson, Moore

Wheeler: On the die.

We have made a lot of processing changes in an attempt to run high β.

Dyke: Photo-probing of channel shows the interesting patterns in accompanying sheet. Note that the channel does not cross the base Si.

Note on the epoxy-packaged units that all channels start from the base contact side.

These units were decreased in channel current ($\times 10^{-2}$ or 10^{-3}) by vacuum baking. Even then we got no change in channel extent by photo-probe.

Units $\bar{c}$ no channels are ok on photo response.

Kabell

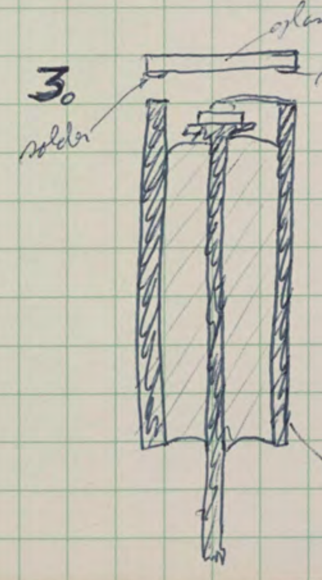
Some units have $\bar{c}$ teflon on over dice under epoxy in old type package.

Proposed directions:

A. Package

1. Epoxy over teflon $\bar{c}$ glass face plate - lacks life test
2. A glass plate metallized with built up Ag balls.
   lacks: a) ball build upon glass
   b) assembly technology
   c) sealing
   d) life test.

3.



metal. - Mn-Ag evaporated film $\bar{c}$ Sn solder.

Lacks
a) Sealing
b) Life test
c) parts supply
d) convincing customer

80 mil diameter Kovar tube.

Another version could use square tube.

 XP-3, con't

B. The die

We have a die in the TO-18 package

We have no die for packaging at >400°C,

Units with no epoxy look ok, even smashed. The same units in epoxy went bad.

Level of present effort

Lofly — 20%

Ullman — ~~10%~~ 15%

Wheeler — 25%

Dyke — (Consulting on demand

Brown & Siddick — 5%

Kobell — 30%

Our customer would be dismayed if we don't deliver.

March 22, 1963 — Custom Integrated Circuitry

Phelps Ferguson
Hoyme Farina
Grinich Shirk
Legg

Epitaxial kit parts:

KT-A , a 2X2 emitter Xstor —Runs in process – out ~4/15
(μT-4 , 4 isolated Xstors of different geometry in 2 sizes) ← This is primarily a test vehicle
XL-7 , a pair of ~~isolated T-1's~~ common collector T-1's

The std. epi technology

March 22, 1963 – Pressure Xducers Review
Ref p 17

Blank
Pearson
Soffy
Middleton
Moore
Simmons
Kabell

One PTC has been put together. It has been tested and looks "good" with respect to 1% error band

~~Problems:~~
~~Wafer prep:~~

Major problems:

1. The gadgets have a Zero offset. This must be balanced out.
Two ways are suggested
a) Mounting of diaphragm on ring under jig to pre-stress to eliminate the unbalance.

b) A diddle technique such as exposing a ~~leg~~ spot on one leg to try to adjust after assembly to the ring.

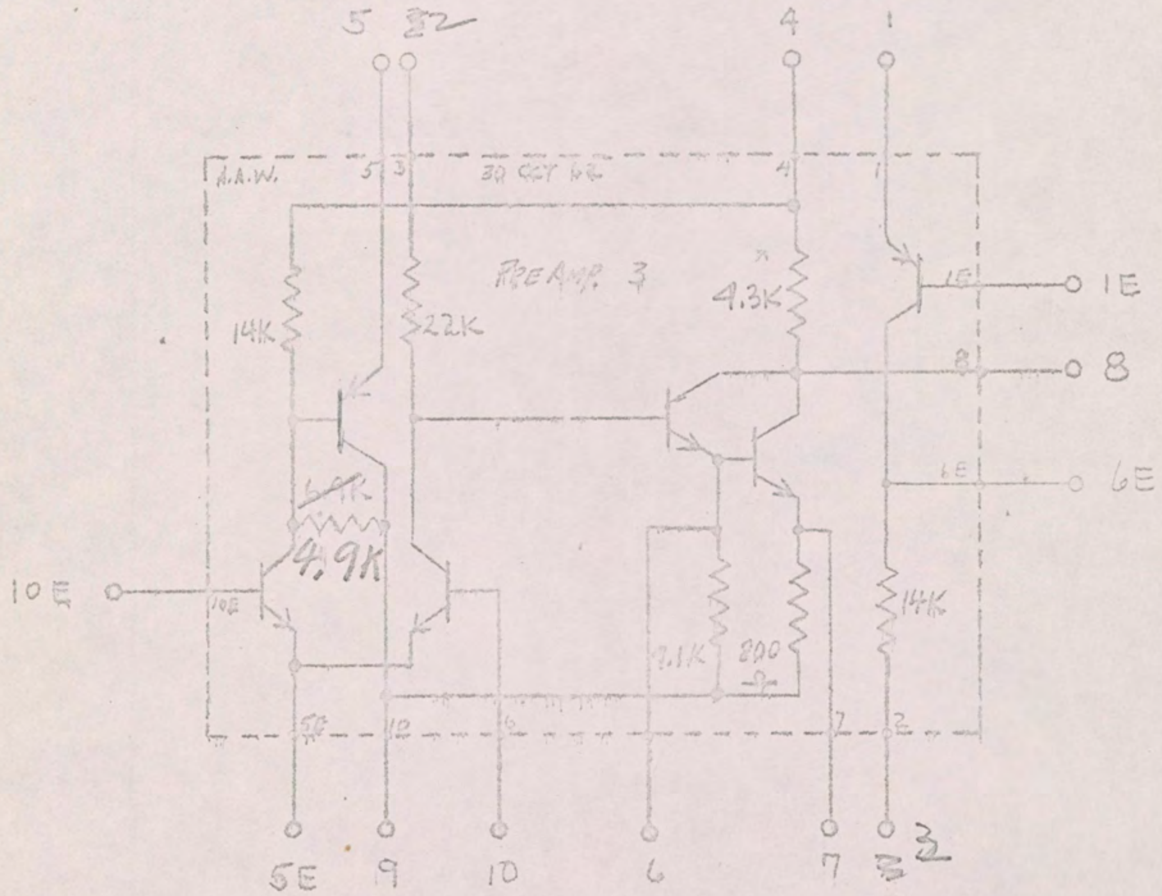
2. No one knows which way to turn to enter this market...
a) We need an odd-ball power supply - essentially a current source

Program:
1. Make 25 units as a schedule for life-testing, etc.
2. Make some 0-offset units.
3. Have data on the 25 and
4. Samples of 0-offset units by June 1.

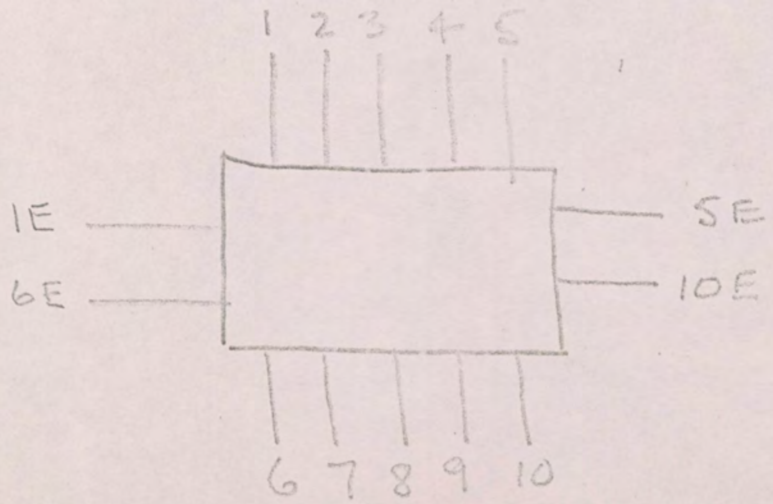
#3

Litton Proprietary Drwg.

This must be converted to all NPN — or possibly with a separate PNP output device.



PREAMP 3



PACKAGE LEAD CONFIGURATION

PROJECT REVIEW

PROJECT 4140

I. DIAPHRAGM FABRICATION

A. Wafer Preparation

1. Yields
2. Loss

   Reason: Breakage, wedging, and size control.
3. Straight service yield ________ 45 %.
4. Supervising process ____ and actual work 72 %.

B. Mechanical Polishing

1. Problems -

   Undersize and wedging. Physics polishing overloaded. May help in future.

C. Wafer Area - Crystal Uniformity — Uses 110

1. R&D - poor.
2. S. Rd. - small, but more uniform.
3. Knapic - large and uniform.

D. Processing

Major Process Permutations -

1. Phos. Gettering - Yield to new spec. 25% (1457 device total) = 1.77 Dia./wafer
2. No Phos. Gettering - Yield to new spec. 2.5% (745 devices total)
3. Crystal orientation - <111>, <110> - no final data.
4. Mapping - Time required

   10 min. full wafer; 20 min., chips.
5. Mounting, Marking - 5 min/wafer.
6. Alignment and cutting - with a cookie cutter

   10 min/Dia. for 100 psi (1 mil./min).

   Yield - 50%

   Loss cause - breakage, cutting and cleaning.
   Learning curve - operator dependent.
   Forecast - 80% - (Bob Brand).

   Yield electrical - Problem -
   Soft after cutting - no. Al. Note: %. (Run 26, 0%; Run 24, 100%)
   With Al. 100 %.

8. Lead Bond - 4 in 1_{out}.

II. PACKAGE FABRICATION

1. Housings - Design frozen.
   50 complete - except plating.
   Estimated cost . . . . $ 1.41 (500)

2. Spacers - 50 due 3-19-63 . . . . $ .99 "

3. Plugs - Electrical
   50 in house . . . . $ 6.00 "

4. Sintered Plugs
   100 in house . . . . $ .10 "

5. Silicon Rings - 35 in house
   20 oxidized - pyrolytic . . . . $ 5.00 "

6. "O" Rings - Buna N.
   50 in house . . . . $ .30 "

7. Solder seal - Induction - Built and tested 5 packages - 4 to burst.
   Burst pressure - 5000 psi
   All sustained for 1 min. at 5000 psi.

8. Assembly Techniques
   a. R.D. seal. H.T. epoxy - 400°F. cure (215°C) Checked on PTB and PTA + 1 PTC. PTB gave 100% bond yield.
   b. Lead welds - Problem solved by new spacer design. No yield data yet.
   c. Final seal - Induction soldered in 6 secs with 15 mil preform.

III. P.T.B. DATA + P.T.C.

N.P. Data Sheets.

IV. P.T.C. SCHEDULE

INTERPRETATION OF HAMMOCK-SLUNG DATA

PTB-1

Excluding the two extremes (150 and 74 mv), the total spread of zero outputs is 20 mv. This would indicate that by proper mask redesign, one could produce diaphragms with a zero balance of less than 10 mv with 75% yield. But consider -

PTB-28

Once again, eliminating the two extremes, we see a tight distribution (11 mv total spread). However, the average imbalance here differs from the average imbalance of run PTB-1 by 65 mv. An explanation exists: Devices on a single working plate match each other quite well, whereas a comparison of devices between working plates shows lack of reproducibility.

~~PTB~~ PTC-20

Exclude the worst case. Average imbalance is improved over PTB by at least 50 mv. Spread is worse (40 mv). Explanations exist for the worse spread, but will be deferred at present on the grounds of insufficient data.

Note on PTC Header Yield:

Wafers with 25 good devices on them were backside mechanically scribed.

9 devices met electrical specifications on subsequent die sort.

5 devices survived hammock slinging.

PTB Linearity

Unit No.	Linearity, or lack thereof
PTB-6	-.50%
PTB-11	-.40%
PTB-12	-.45%
PTB-13	-.49%
PTB-3	-.47%
PTC-1	-.36

PRESSURE VS. TEMPERATURE (WITH EMPHASIS ON HYSTERESIS)

	UNIT NO.	SENSITIVITY BEFORE TEST (mv)	SENS. AFTER 200°F (mv)	SENS. AFTER −20°F (mv)	ZERO BEFORE TEST (mv)	ZERO AFTER 200°F (mv)	ZERO AFTER −20°F (mv)
LOW TEMP. CEMENT	PTA-17-3	271.78	286.35 UNIT TOOK 27mv SHIFT AT 98°C BETWEEN 240 & 320 PSI		0.03	4.95	
	PTB-3	222.15 (?)	231.23 9mv SHIFT BETWEEN 240 & 320 PSI @ 24°C		−1.12	−2.41	
	PTB-6	256.11	261.46		0.96	1.64	
HIGH TEMP. CEMENT	PTA-22-2	302.72	299.38		−1.11	−2.56	
	PTA-22-3	263.19	263.38		.05	.06	
	PTA-22-4	291.31	SHORT TO CASE		.71		
	PTB-11	290.49	290.63	290.66	.03	.00	−1.75
	PTB-12	245.20	245.82	245.80	.18	−1.09	2.91
	PTB-13	295.35	295.38	295.61	2.43	1.18	1.39

PTB Hammock-Slung Headers

Unit No.	V_{out} @ 10 volts in (mv)	
PTB-1-A-1	84	
-2	150	
-3	90	
-4	95	AVERAGE ≈ 93 mv
-5	97	(excluding the two extremes)
-6	104	
-7	95	
-8	74	
PTB-28-4-1	163	
-2	152	
-3	130	AVERAGE = 158 mv
-4	163	(excluding the two extremes)
-5	229	
-6	154	

PTC HAMMOCK-SLUNG HEADERS

UNIT No.	V_{OUT} @ 10 VOLTS IN (mv)
PTC-20-2-1	58
-2-2	20
-5-1	32
-5-2	60
-8-1	280

AVERAGE = $42\frac{1}{2}$ mv
(excluding single worst case)

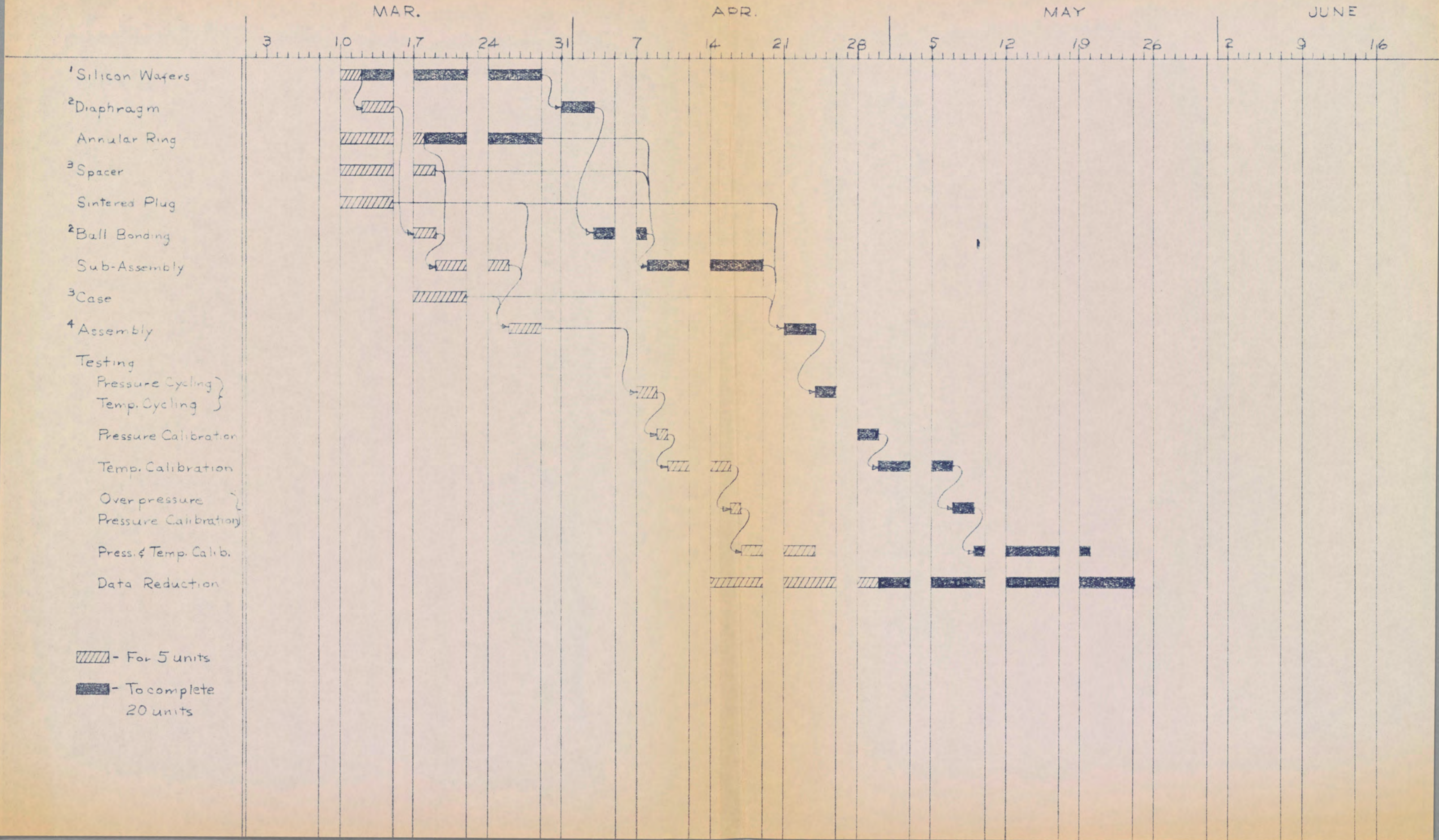
PTA BURST TESTS

UNIT No.	LINEARITY (%) @ 400 psi	@ 600 psi	@ 800 psi	@ 1000 psi	HYSTERESIS (%) @ 400 psi	@ 600 psi	@ 800 psi	@ 1000 psi	BURST PRESSURE (psi)
PTA-15-3	-.52	-.75	-.92	-1.04	-.02	-.011	-.014	-.05	1250
PTA-15-6	-.51 -.50	-.74	-.93	CRACKED @ 1000 PSI	-.16 .04	.03	.03	CRACKED @ 1000 PSI	1350
PTA-15-1	-.43	-.65	-.83	-.97	-.04	.004	.013	.02	1425+

CRACKED @ 1050 PSI

N. Zinker
3/12/63

FLOW CHART PTC



To: Meeting Attendees

From: N. Zinker

Subject: NOTES FOR PRESSURE TRANSDUCER PROJECT REVIEW MEETING MARCH 19, 1963

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1. Due to new specification for devices (>30 volts breakdown hard; leakage <20 nano amps at 30 volts) time was lost trying to find devices which meet the specification. This problem appears to be resolved by using phosphorous gettering. Up to six usable diaphragms per wafer have been obtained from the most recent wafers. This phase of the schedule is dependent on our ability to get devices with the desired electrical characteristics.

2. Diaphragm cutting and ball bonding schedules are dependent on scraping the deposited metal leads as a temporary fix. This fix may not be adequate for the following reasons:

   a. Empirical evidence shows that devices which have good electrical characteristics on the wafer do not meet diode specification after diaphragm cutting. In addition, creepers have been generated; and since there is insufficient knowledge about this phenomenon acceptance or rejection of these devices is uncertain.

   b. Empirical evidence also shows that dice which were scraped and had good electrical characteristics before ball bonding had degraded after ball bonding.

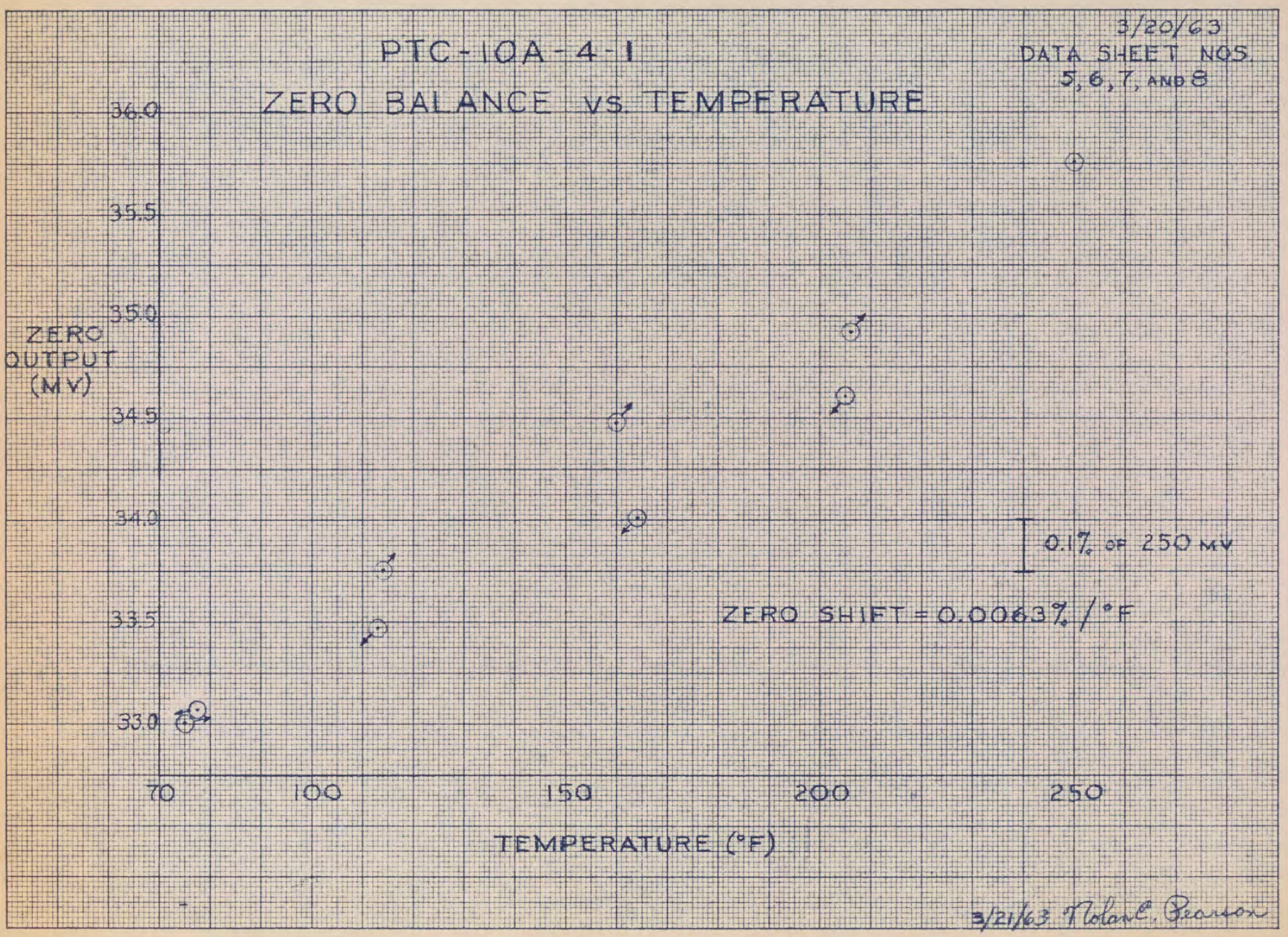
   Suggested corrections:

   a. Cutting diaphragms to the originally required diameter (.210 in) instead of the new diameter (.203 in). This will eliminate the need for lead scraping since the old diameter did not cut through the metalized area, which is the initial cause of the problem. The diaphragm would then be mounted on the annular ring using a locating rig, eliminating the need for a counter-bored annular ring (which increased the cost of the fabrication of the annular ring).

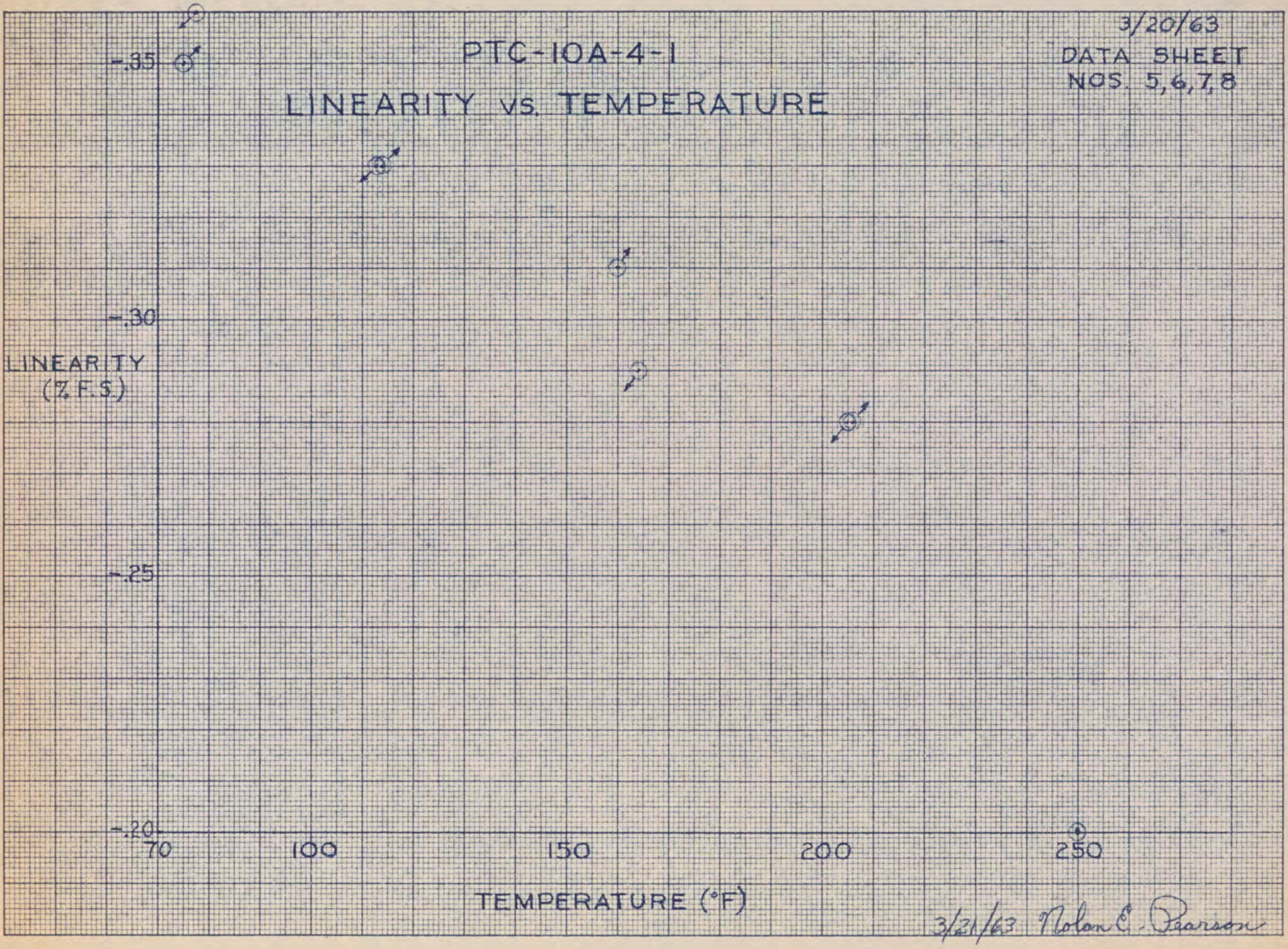
   b. Redesigning the metalizing mask so that the leads are shorter. Hence the leads will not be cut during the diaphragm cutting process. A new set of masks must then be stepped.

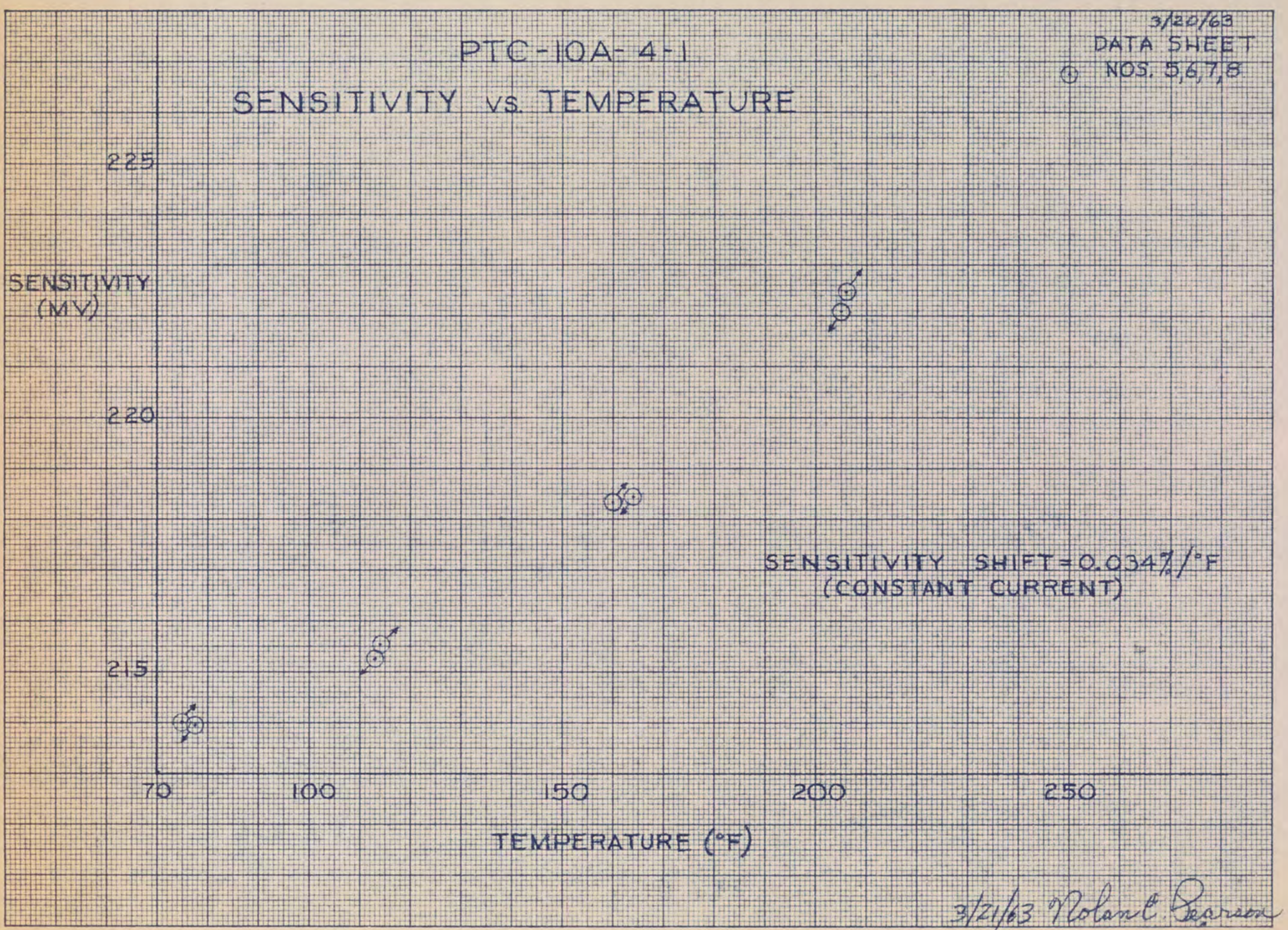
3. Spacer and case fabrication schedule is dependent on the ability of outside sources to meet the required tolerances. A reason for not meeting the completion date on the original schedule was due to the inability of the lowest bidder (Jet Fittings) to satisfactorily machine the parts. The substitute machine shop (Swiss Precision) was able to fabricate and deliver satisfactory cases. They are now working on the spacers, and it is expected that they will meet the required tolerances. Therefore, they appear to be a suitable source for the fabrication of cases and spacers.

4. Final transducer assembly schedule is dependent on R. Brown's induction soldering unit being available when it is required. All final assembly fixtures have been designed to fit his unit.


PTC-10A-4-1
ZERO BALANCE vs. TEMPERATURE
3/20/63
DATA SHEET NOS. 5, 6, 7, AND 8
ZERO OUTPUT (MV)
36.0
35.5
35.0
34.5
34.0
33.5
33.0
70
100
150
200
250
TEMPERATURE (°F)
0.1% OF 250 MV
ZERO SHIFT = 0.0063% / °F
3/21/63 Nolan E. Pearson

K+E 10 X 10 TO THE CM. KEUFFEL & ESSER CO. 359-14G MADE IN U.S.A.




3/20/63
DATA SHEET
NOS. 5,6,7,8
PTC-10A-4-1
SENSITIVITY vs. TEMPERATURE
225
SENSITIVITY
(MV)
220
215
SENSITIVITY SHIFT = 0.034%/°F
(CONSTANT CURRENT)
70
100
150
200
250
TEMPERATURE (°F)
3/21/63 Noland Pearson

μcktry Monday Meeting - 3/15/63 — Trotter, Faurie, Hogan, Grant

NAND

The storage diode for the (NAND? binary) does not look reliable.
Other possibilities are

a) a collector diffusion before epitaxy at low C to extend the volume of N-type.

I don't like this.

b) a P+ ?B predeposited substrate for long out-diffusion.

c) vapor etch & backfill

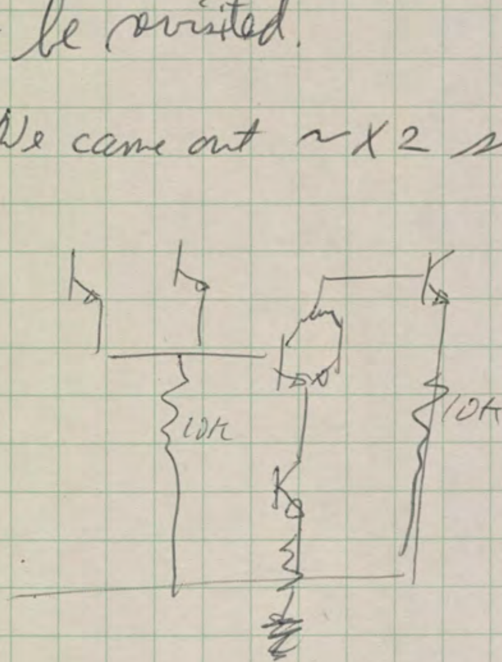
Some more circuit work is needed to show that the possibility of compatible devices will do the job. Until done, no masks to be made.

Gates will be out in ~ 3 weeks, but the usefulness is dependent upon the possibility of making the R.

The series-gated R-element is in the mill (Porter) — ~ 2 weeks.
Still considering a C-coupled S element for a DCTL-compatible Binary.
To be revisited.

CML

We came out ~ X 2 slower than expected



As made	~11.5 ns
mod. c R's	~8.5
	8.5
Breadboard	~5.5

Most of this

Epitaxial Meeting 3/26/63

Davis, Wilson, Yin, Moore, Gupta, Schroeder, Montier, Conant, Cole

Some report on old data on the quality of the grown junctions:

Hank will see that an evaluation wafer gets run periodically to evaluate the comparative surface defect density on a continuing basis.

(Dick feels that he can buy much better surfaces (low pits) than he can grow).

→ (Get Cole on Tech Reports list) – Especially on those epi-related

New Reactor:

Old machine is still running. It has a pit problem.

1) We should be concerned c̄ pits removal and comparison c̄ std.

2) What is inertia of system. We don't know.

Cole needs an additional reactor. He will try to order 1.

We can supply $SiCl_4$ for a while.

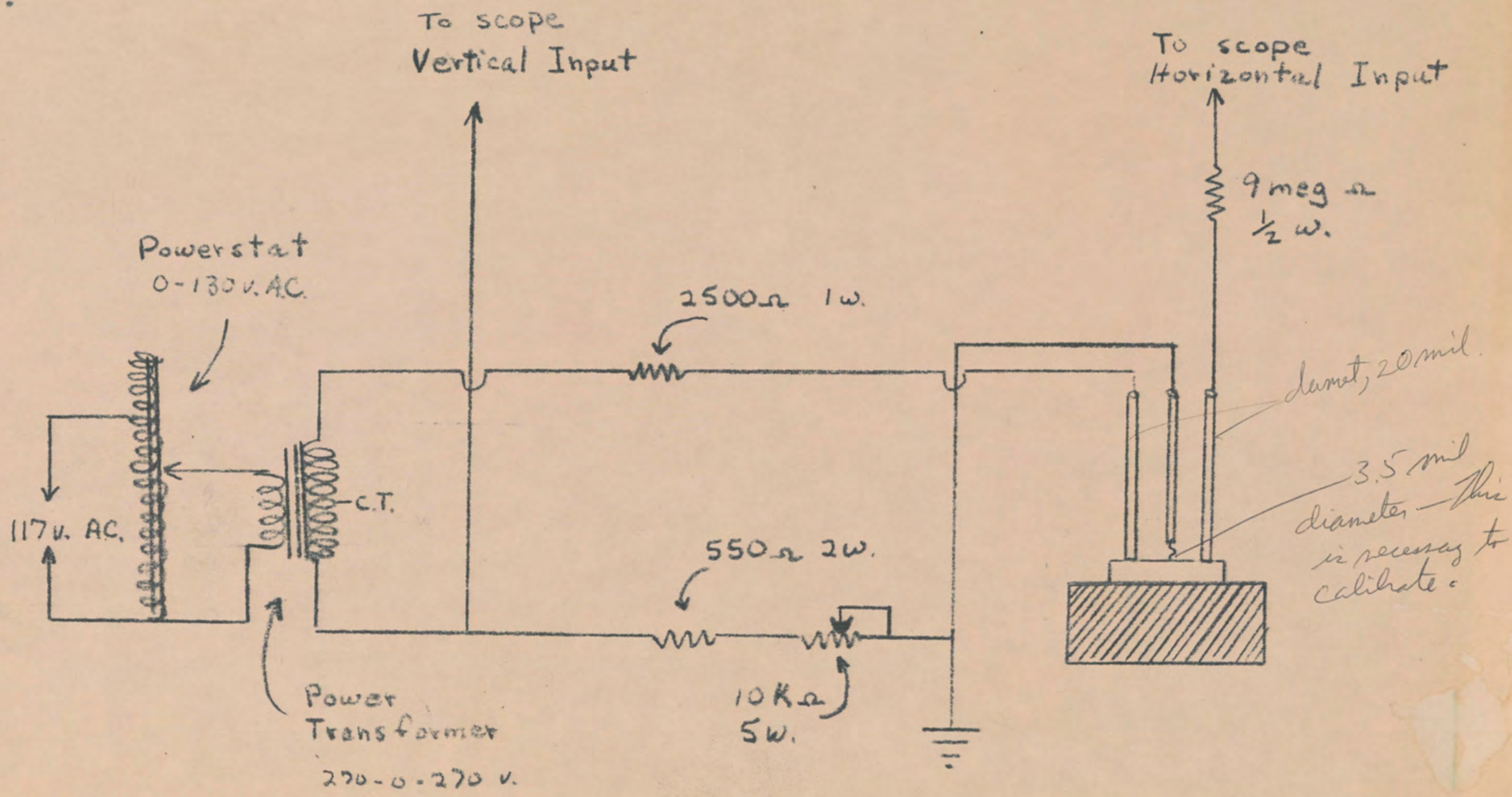

To scope
Vertical Input
To scope
Horizontal Input
9 meg Ω
½ w.
Powerstat
0-130 v. A.C.
2500Ω 1w.
dumet, 20 mil
C.T.
117 v. AC.
3.5 mil
diameter — This
is necessary to
calibrate.
550Ω 2w.
Power
Transformer
270-0-270 v.
10KΩ
5w.

Fig. I

Section Meeting 4/13/63 — Blome, Egvall, Van Ness, Ivanich, Fok

Mask making:

Mask alignment check has been stopped - no problem since Sept 26 and that was on old machine.

Matrix stepping is good to < 0.1 mil.

The multiple ~~emitter~~ geometry one is in.

We are using many more plates than usual.

Projection printing is being tried. —— Needs layout of project.

The original memory job was do-able (½ mil lines). However they keep changing - now are to a 20"x10" array.

Optical alignment jigs:

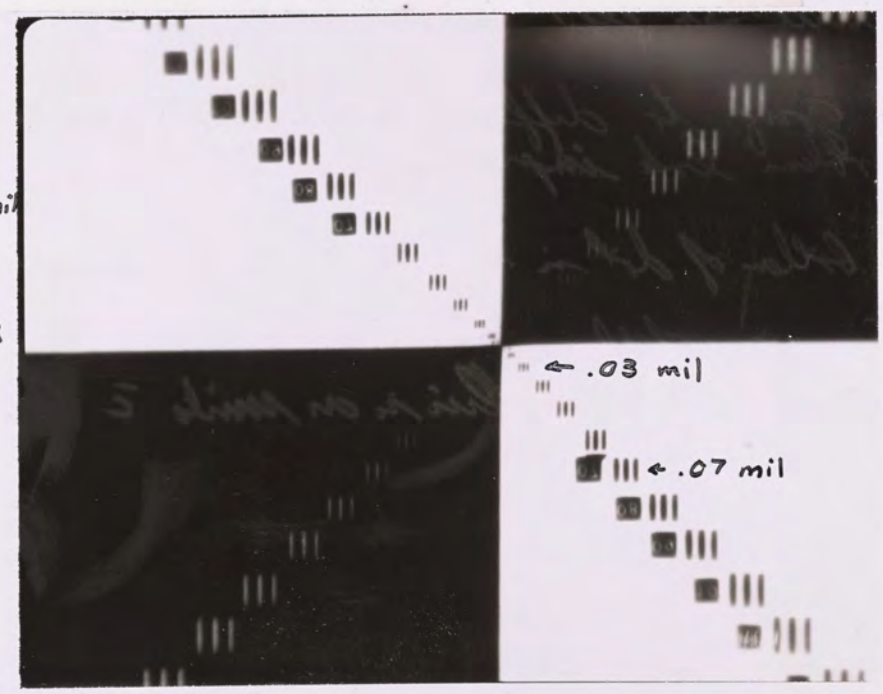
TP3 20B1

B&L 21X/0.50

50X Red.

Resolution .02 mil

Reduction made 3-19-63



(Sam Fok)

 4/3/63 — Diode Problem

Diffek, Waing, Grind, Lenom, Chin, Fronte, Bradek, Geynes, Windey, G. Parker

Mainly 2 problems:

1. The silver button structure
2. Whisker ē it.

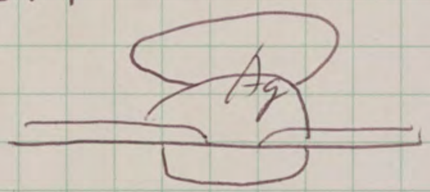
History:
Done first for ADAM (18 MO ago)

But ADAM vs reg FD-1 is less reliable at high temp. The problem is I_R. leakage 1/80 of ADAM 10^{-4} for FD-1 — but from a variety of mechanisms.
Also C of ADAM device is > FD-1.

Now trying to convert FD-1 and FD-7 to it.

On FD-1
C about 2pf vs <1 on regular p. bonite. Stable @ 200°C.

Test 379



Problems:

1. High C at t=0
2. I_R stability N.G. on T separately
3. Mechanical problem
4. Recovery of mechanical failures & op. failures for no apparent reason.

These were with Sn-clad whiskers

Now be by going to different whisker (Ni 4x20 mil) the mechanical problem look improved.

Diameter of bottom of dot is ~ 6-7 mils by keeping smaller than 6

At 200° C is stable
→ At 300° C it climbs — this is on units ē Ge-Au solder

Action Items: FD-1

1. JPF will try the new assembly techniques. Ray to bring wafers just after metal.
2. Duffek will try to plate two other materials, to see where we sit. Ni (because GE does) and one other. Wafers to be supplied after metal flashing.
3. Ray Brown will bring down some of these units with unusually high capacitance.
   Ni'l will evaluate electrically &/or analytically for mechanism.
   " " try heat & grind.

4. ~~Postulate that~~ ~~dirty~~ environment in pkg is reason for I_R drift. Check ē Xstor can.

For the Ag ball we want a ^personal^ contact.

Have tried Pd - Ru
Pd - Au
Ni

Problems are

 Layout of Project Layout - Projection printing

Fole
Blome
Engvall

Moore

We should layout a "blugs" jig

Do forming, exposure & alignment feasibility tests

After this, lens comparison -

TABLE I

Resistance change during alloying (2 min N_{21} 580°C)
for different substrate temperatures

Run RNC#	Date Evaporated	Date Alloyed	Substrate Temp. (°C)	10-90 Percentile Spread %		R(after) - R(before) (%)			TRC ρpm/oC
				Before All.	After All.	Mean	10 Perc.	90 Perc.	
42	1/25	2/7/63	400°	7.9	7.6	-3.1	-2.3	-3.9	60-140
43	1/29	2/7	600°	24.0	27.0	+38.5	+ 31.0	+59.8	20-180
45	1/30	2/7	500°	18.3	19.5	+42.0	+ 35.8	+49.2	30-290
46	1/31	2/8	410°	4.82	4.1	+ 0.57	- 0.75	+ 2.0	80-120
47	2/1	2/8	310°	6.15	4.47	- 4.1	- 3.5	- 5.2	100-150
48	2/5	2/15	300°	5.77	8.86	+ 2.7	+ 2.0	+ 5.2	40-100
50	2/7	2/15	350°	2.95	3.52	- 0.7	- 0.25	+ 0.5	90-130
51	2/11	2/15	350°	2.90	3.20	+ 6.1	+ 5.7	+ 6.5	50-90
52	2/12	2/15	300°	4.33	9.38	+ 6.1	+ 3.2	+11.2	60-200
53-A	2/13	2/15	400°	4.54	3.98	+ 7.6	+ 7.1	+ 8.0	50-90
53-B	2/13	2/15	400°	3.94	3.07	+ 2.4	+ 1.8	+ 3.4	10-100
54	2/13	2/18	340°	5.32	5.03	+21.7	+ 20.2	+22.8	90-190
56	2/14	2/18	340°	3.34	3.19	+ 4.7	+ 4.3	+ 5.1	90-150
57	2/14	2/19	360°	4.31	4.04	+ 4.2	+ 3.8	+ 4.6	80-160
58	2/15	2/19	320°	6.35	5.50	+ 6.8	+ 6.2	+ 7.6	40-80
59	2/15	2/19	380°	4.47	4.02	+ 6.9	+ 6.1	+ 7.5	50-310
60	2/18	2/20	340°	4.89	5.07	+12.5	+ 11.7	+13.3	80-120
61	2/18	2/26	380°	6.58	5.67	+11.2	+ 10.3	+12.4	40-140
62	2/18	2/26	340°	3.24	3.23	+17.5	+ 16.7	+18.3	30-110

4/4/63

p. 113
4/4/63

Nichrome

Evapn. Conditions vs. Change during Alloy

Vacuum

Evapn E

T(°C)	ΔR (%)	
25°	−1.3	+35
25°	+5.1	+10
100°	+18	+30
150°	+20	+27
200°	−27	−20
200° (300°)	−7.8	−25
480°	−4.5	−16
600°	~10X	

Sublim. S

T°C	ΔR (%)	
380° V	−4.0	−20
391-380 V	+19.8	+20.7
380-340	+6.7	−8.8
380-320	+8.9	+17
390-360	−7.1	+7.1

Oxygen

	P_{O_2} (Torr)	T (°C)	ΔR (%)	
E	$2 \cdot 10^{-5}$	50°	−24	+7.0
E	$2 \cdot 10^{-5}$	80°	0	+12.0
E	$5 \cdot 10^{-5}$	50°	−46.	−59.
E	$1 \cdot 10^{-4}$	60°	−70.	−75.
E	$5 \cdot 10^{-5}$	210	−74.	−75.

Carbon Monoxide

	P_{CO} (Torr)	T(°C)	ΔR(%)	
E	$2 \cdot 10^{-5}$	70	−28.	−46.
E	$1 \cdot 10^{-4}$	50	−16.	−38.
E	$2 \cdot 10^{-5}$	130	−35.	−50.
E	$1 \cdot 10^{-4}$	50.	~~+~~20	~~+~~21
S	$2 \cdot 10^{-5}$	300-260	−18	−23
S	$2 \cdot 10^{-5}$	200	−46	−52
S	$1 \cdot 10^{-4}$	300-225	−33	−49

rkw
4 April 63

Nichrome - 4/4/63 Waits Rugg Campbell Solo

Ref. p. 78, 79

Rugg ~~[illegible]~~ reproducibility data showed general pretty good results c̄ alloy, but it correlates with nothing except date of evaporation.

In Varian system we did two runs, ~~@~~

ΔR_{min} (%)	ΔR_{max} (%)
−4.0	−20
+19.8	+20.7

As far as we know, these were done identically.

The experiment to correlate R c̄ geometry was inconclusive. One wafer correlated and one didn't.

A wafer that is "wild" before is likely to vary erratically ~~[illegible]~~ during alloying.

In reviewing the process we do not know what the problem relates to. A strong dependence on vacuum purity is indicated. At this time an end run is required.

Shots in the dark,

Waits {
- Ta_2 ~50 Ω/□ — Bob Waits thinks it is better.
- Sputtered film of Ni Cr.
- Ta_2 Ta sputtered film
}

Heinz ~~Rugg~~ will try a double-Al to eliminate the need for "alloy cycle for Ni Cr.

Meeting on ckt modules — Blastoff 4/8/63

Ness, Kabell, Russell, Landolfi (R&D); Spark, Grimm, Moore

	Mkt import	Sales intro / Cum supply	
1. Gen Pur. Amp., epoxy pot	*	5/27	
2. S.S. Chop Amp, card & can	*	6/10	
3. Photo Chop Stab op amp	(*)	7/8	
4. High Gain Dif amp	*		( )
5. AC Dif amp	*		( ) ?
6. Current Source		6/3	
7. Voltage ref	*	7/22	
8. Voltage comp	*	7/8	
9. Std cell replacement	*		( )
10. Log amp	*		( )
11. FET op amp	*		( )
12. V to I converter		6/17	( ) – limited mkt.
13. Wide band d.c. amp (a big lab / panel job)	*	7/1	– this is a hot one, but is optimistic or h...
14. Low frequency sweep gen.			
15. Lab decade amp.			
16. Function Gen.			
17. DVM			
18. Isolated power supply			

Our program: Make 10 ea in R&D. Follow as necessary.

On the DVM the problem

1. Is there a capacitor problem? — Kabell – Russel

We will turn out a weekly status rept every Friday.
The 1st week it will be a time schedule.

Action
1. Pkg settlement
2. Objective specs on blocks
3. Resolve C problem on DVM
4. Send Johnson to check out.

INTERNAL CORRESPONDENCE

FAIRCHILD SEMICONDUCTOR

A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

TO: Distribution DATE: April 8, 1963

FROM: V. H. Grinich CC:

SUBJECT: Instrumentation Circuit Modules
Minutes of Meeting held April 8, 1963

The following is a list of the items discussed with a description of the package in which they will be available, and a date indicating a time by which sales personnel will receive samples for distribution to customers:

No.	Product	Date Sales Samples Available
1*	General Purpose Amplifier (replace PP65), Epoxy Pack.	5/27
2*	Solid State Chopper Operational Amplifier (redesign to eliminate FET), Card & Can	6/10
3	Photo-chop. STAB Operational Amplifier	7/18
4*	High Gain Differential Amplifier (need greater output) Epoxy Pack.	
5*	AC Differential Amplifier, Epoxy Pack	
6	Current Source	6/3
7*	Voltage Ref.	7/22
8*	Voltage Comp.	7/8
9*	Standard Cell Repl.	
10*	Log Amplifier	
11*	FET Operational Amplifier	
12	V to I Conv.	6/17
13*	Wide Band DC Amplifier	7/7
14	Low Frequency Sweep Generator	
15	Lab Decade Amplifier	
16	Functional Generator	
17	Digital Voltmeter	
18	Power Supply ISO	

The following action items were discussed. The name in parentheses after the item indicates the person responsible for providing information. The date after the person's name indicates the time at which a memo giving the results of the action item should be sent to the same distribution as these minutes are sent:

1) Instrumentation Marketing to provide input regarding desirable package arrangements, including colors, marking, etc. (G. Ness & R. Randolph) 4/15/63

2) R&D will present Instrumentation Marketing with a preliminary objective

---

spec on Items 4, 10, 11, 12 and 18. The specs on Items 4, 12 and 18 will be issued by April 15 and those on 10 and 11 will be issued on April 22. Item 9 will be issued August 15 (this awaits our precision potentiometer arrival and use). (J. Kabell) 4/15, 4/22 and 8/15.

3) Instrumentation Marketing will send copies of all objective specs and data sheets to R&D prior to final printing so that R&D will have an opportunity to modify if necessary. (G. Ness and R. Randolph)

4) E. Russell and J. Kabell are to resolve the capacitor temperature coefficient problem by finding a person who will look over all the existing data and do the necessary experiments to resolve the questions on the present ramp capacitor. (E. Russell and J. Kabell) Report due 4/22

5) E. Russell will assign Doug Johnson to work on the debugging of the two other DVM chassis under R&D supervision. This assignment to take place as soon as possible. (E. Russell)

6) R&D will issue objective specs on 14, 15 and 16. (J. Kabell) 4/29

7) Weekly status reports will be issued by Instrumentation and R&D concerning modules that are in pilot production. These status reports should be written and issued on Friday and should be one 8-1/2" x 11" sheet of paper. Items for reporting are assigned as follows, with the exception of Item 5. This item was left in "no man's land" since no schedule or objective spec has been proposed. At the next meeting it will be a point of business to resolve this question of Item 5.

(M. Norby, Instrumentation)------------------Items 1, 2, 3, 6, 7, 8 and 13

(H. Borden, R&D)-----------------------------Items 4, 9, 10, 11 and 12.

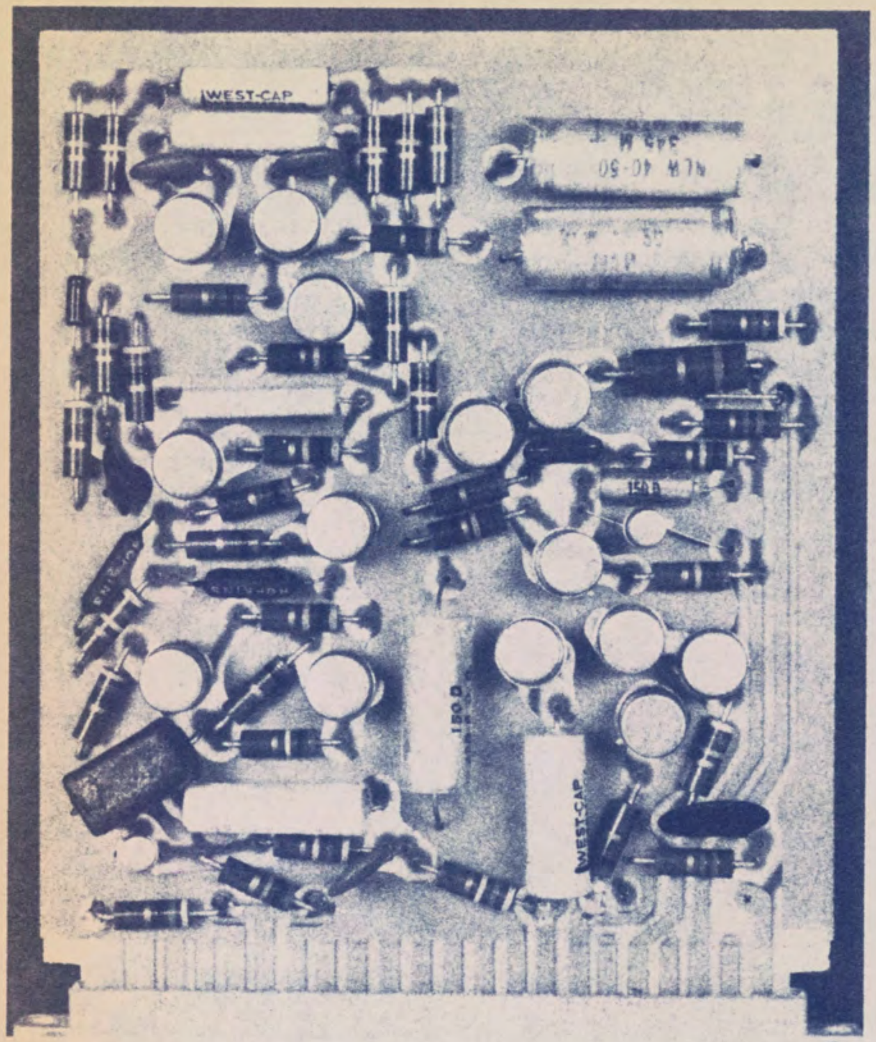
The next meeting will be held at 8:00 a.m., Monday, April 29, in my office.

VHGrinich

VHG:ef

Distribution:

T. Bay
V. Grinich
J. Kabell
G. Moore ✓
G. Ness
R. Randolph
E. Russell
C. Sporck



All solid state (no mech. chopper, no tubes)

All silicon

No chopper drive required

SOLID STATE OPERATIONAL AMPLIFIER

GAIN:

Open Loop

D.C.	2×10^6 (Min.)
Gain-Bandwidth-Product	2MC (Min.)

Closed Loop (Unity Gain)

$R_{in} = R_F = 10K$	-3DB at 1.5MC

INPUT:

Temperature Drift

-20°C to +80°C, less than 10μV/°C

Voltage Offset Less than 200μV

Can be adjusted to zero with external pot.

Current Offset Less than 200pA

Can be adjusted to zero with external pot.

Input Impedance

D.C.	1 Megohm
Above 1 CPS	600K

NOISE: Less than 100μV RMS, (referred to summing junction, bandwidth 0 to 1KC. $R_F = R_{in} = 100K$)

OUTPUT:

Output Current	2mA at ±24V
	7mA at ±10V
	10mA at 0V
Output Impedance	Less than 30Ω (Open Loop)

POWER REQUIREMENT:

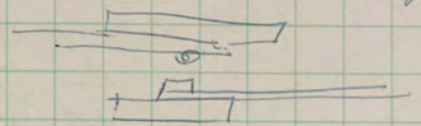
+30V 30mA 1% regulation

-30V 30mA 1% regulation

Diode packaging meeting 4/8/63

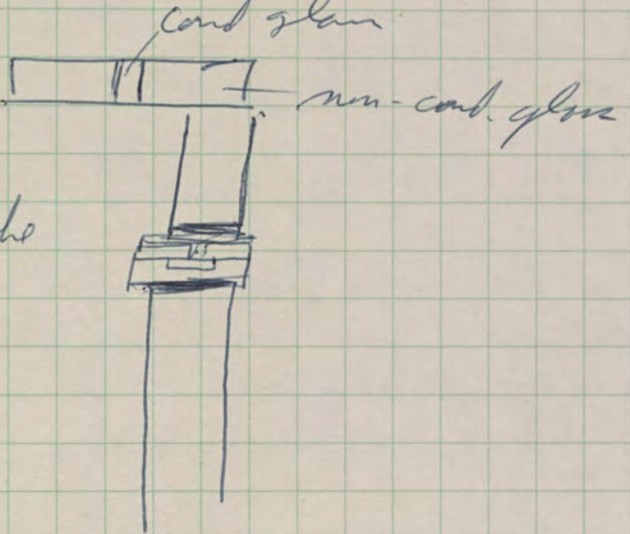
Saddick Shim
Brown Moore
Seymour

Free thinking:
Using conductive glass



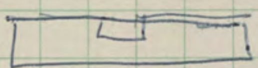
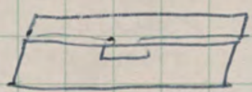
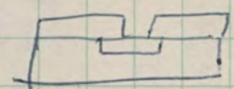
Making the 10μ thick insulating layer looks like the best way to go.

Another way, make a preform



Then take

Probably the easiest to try is to use the process c̄ conducting glass

 add process  etch a hole 

Add conducting glass  assemble in a ceramic bead

 Pre PNP Product Planning ~~Meeting~~ Meeting : 4/9/63 JPF VHG

10

1713 – Very need

~~0005~~
~~45H~~ Still appears to be a borrowed time

Q₁ What happens under other life test conditions eg, Automatic Matrix.

Q₂ What range of Ga treatment is needed

We (R&D) feels that from what we now know it is ~~any~~ important to continue to keep to low voltage products.
Suggest a "joint effort" with Bittman to check out

7500 – Our epitaxial has problem of thickness, ρ & so on.
get spread of 10 μ at 4 20 avg.

In order to be a ~~problem~~ product we must clean up the channels & material.

Looks like a min of 4–6 mo

SCR-2 – Unit looks good, final diddle underway.
Needs 2ff life test for new backside

Problem: Requires much special processing.

2 MO MIN to life test
~~at~~ 3–6 MO to put into prod.

April 10, 1963

WADC REPORT DRAFT

0.33 mil spacing

Description of Approach and Progress During the Reporting Period:

During the reporting period two runs of UIV geometry FET's were finished successfully! The first UIV devices obtained had the following typical d-c characteristics: $I_{SDO} \cong .5 - 1.5$ ma, $V_P \cong 1.5 - 2.5$ volts, gm $\cong$ 1,000 - 2,000 μmhos, and BV $\cong$ 8.5 volts.

No ¶ Currently the Y-parameters are being measured, and some initial results will be given in the third quarterly engineering report.

No ¶ The d-c characteristics meet every expectation for the UIV geometry devices save break-down voltage and are in line with theoretical predictions. The 8.5 volt break-down of the first UIV's is due to a higher-than-desired top gate impurity concentration. This concentration has been reduced considerably, and recent UIV FET'S have break-down voltages ranging from 25 to 50 volts, other characteristics remaining about the same.

Using the identical starting material and diffusion schedule, but substituting the UIII mask set, one can expect about a two fold increase in gm and I_{SDO}; whereas V_P and BV will remain unchanged. Three UIII geometry FET device runs have been started which are being diffused the same way as the successful UIV's.

Mr. Bill Edwards, contracting officer, made a visit to the R & D laboratory of Fairchild Semiconductor on March 15, 1963. The integrated cascode was discussed with him as a very promising solution to the contract objectives. The cascode approach to a high input impedance FET device is quite independent from the approach now being pursued. Several low noise UI geometry FET's were sent to Mr. Edwards for his possible evaluation of the cascode idea.

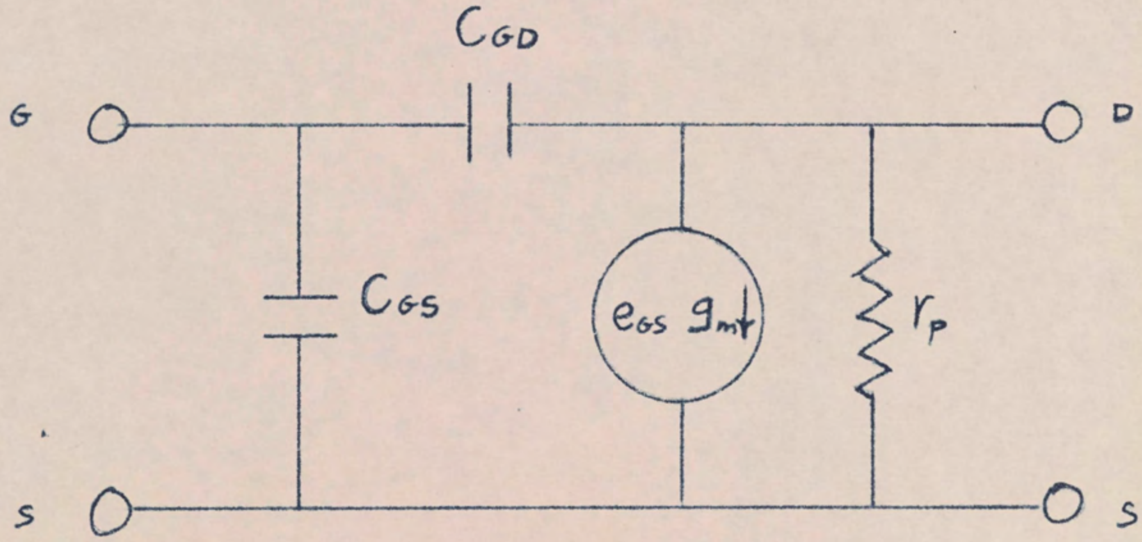
WADC Report

Anticipated Work for April 1963:

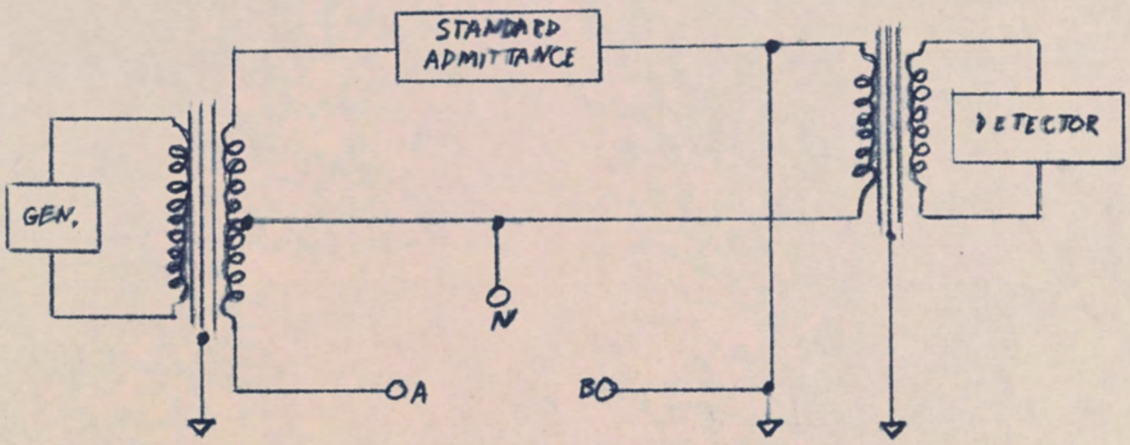
In the next reporting period UIII runs now being processed should be completed, and at the same time additional runs will be started. In the a-c evaluation area Y-parameter and voltage gain measurements will be made on UIV devices.

Cumulative Percent Completion Toward Contract Objectives

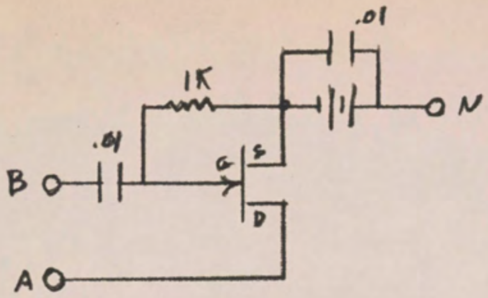
(65% - Don't forget accumulated hours).



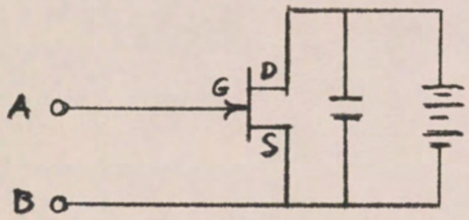
EQUIVALENT CIRCUIT



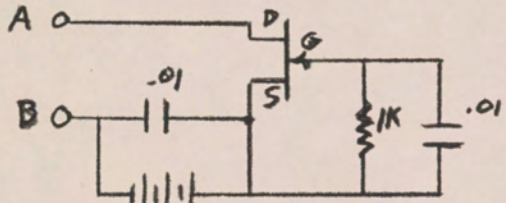
Wayne Kerr Bridge
Simplified Circuit Diagram



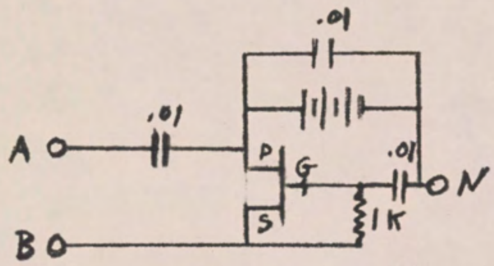
$-Y_{12S}$



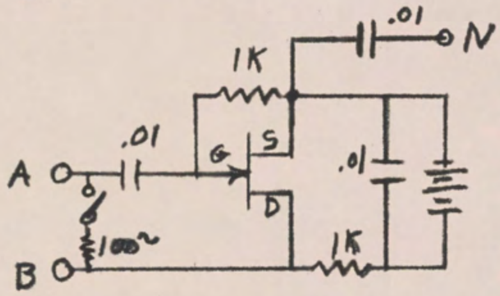
Y_{11S}



Y_{22S}



$-Y_{21G}$



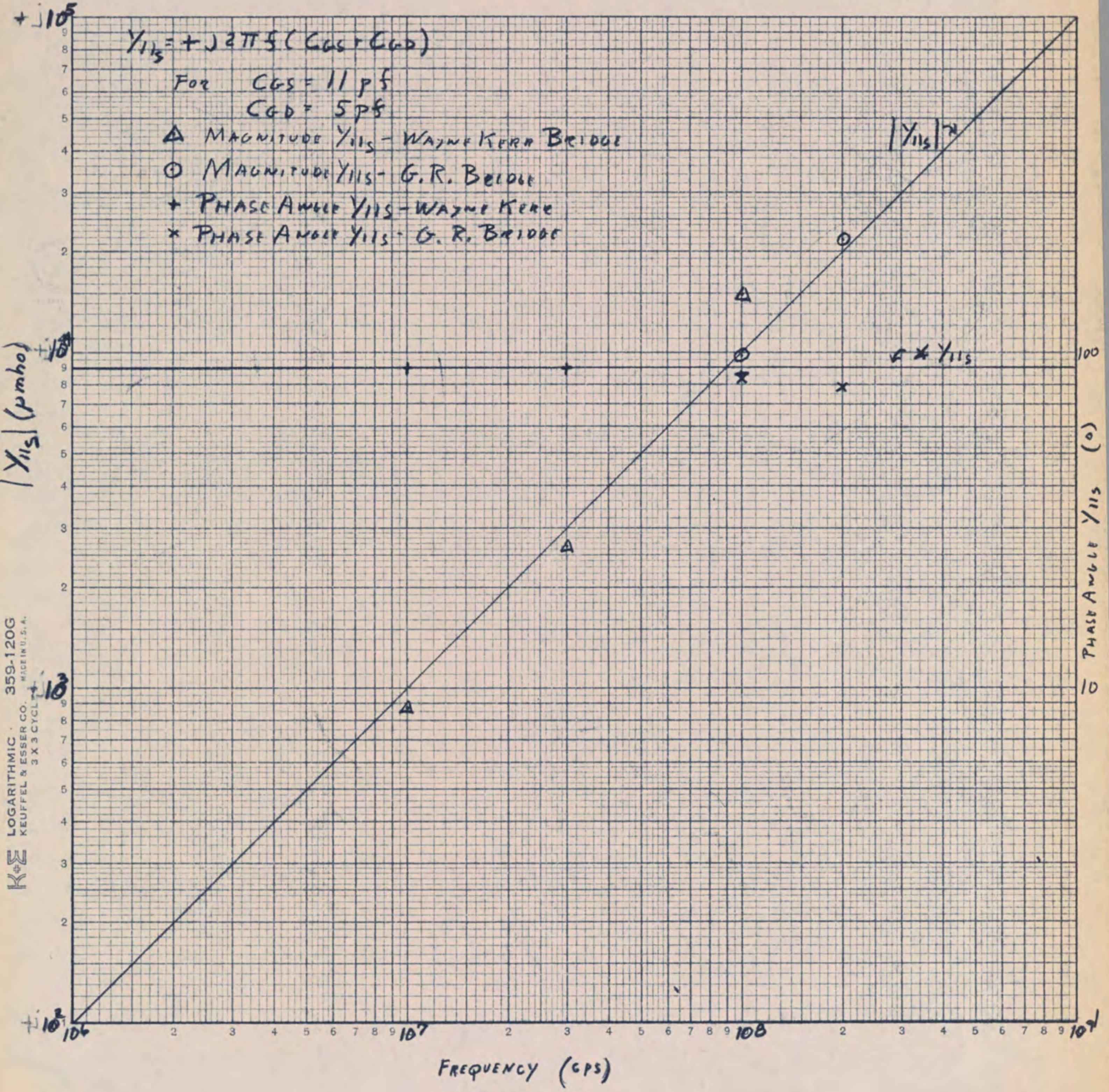
$-Y_{21S}$

"Y" PARAMETER JIGS

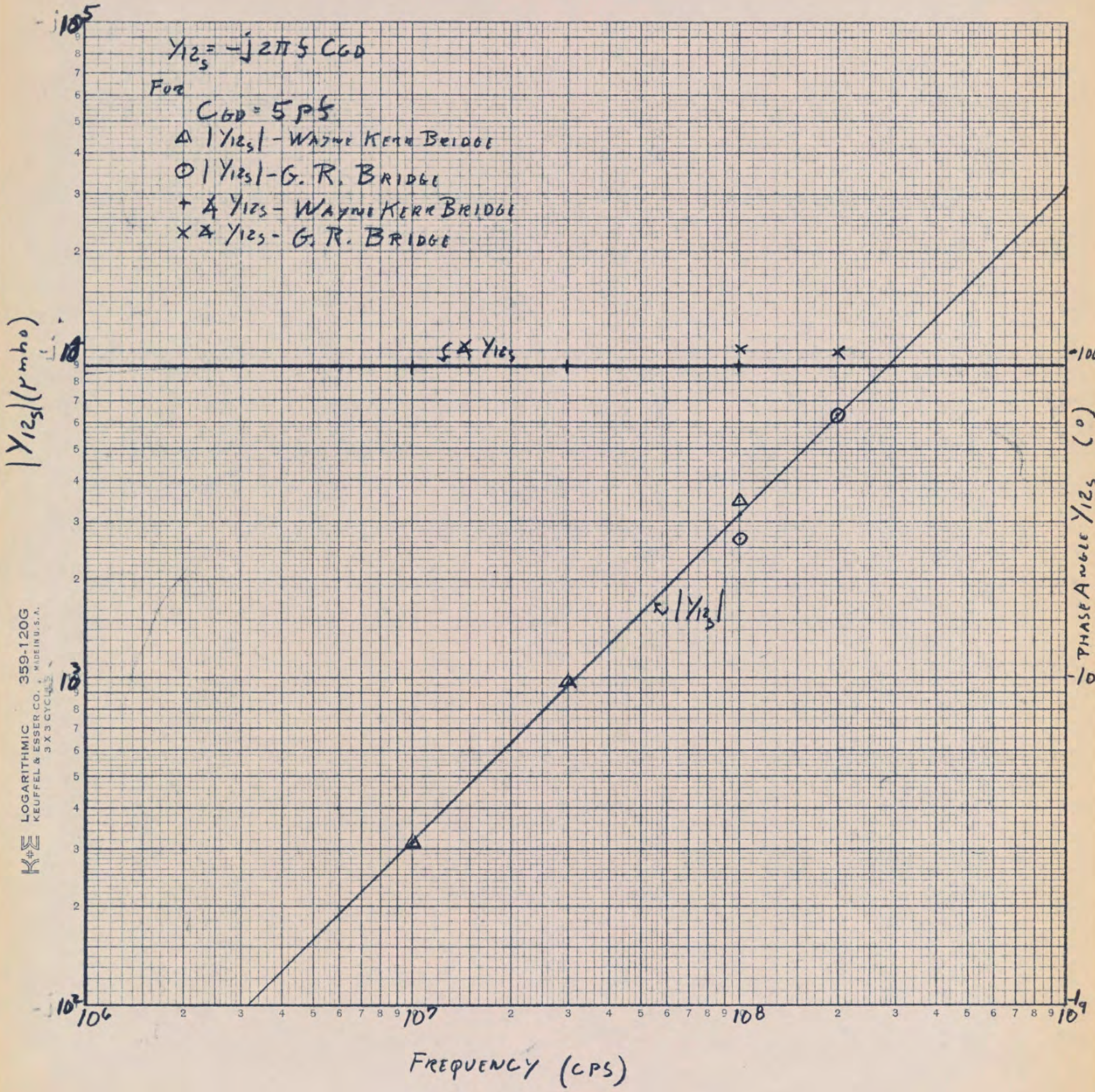
MEASURED AT

V_{GS} = 0 VOLTS

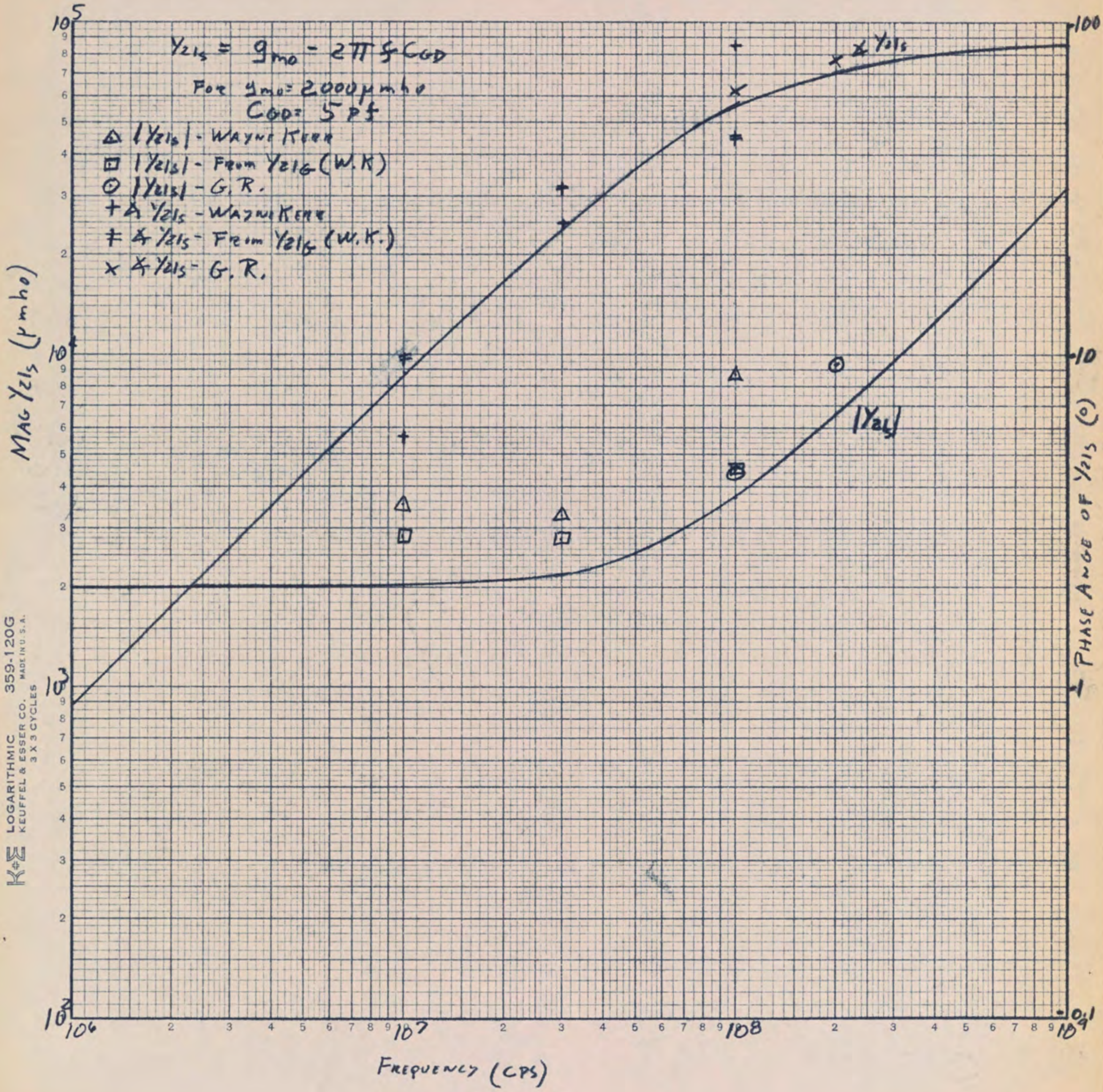
V_{DS} = 6 VOLTS

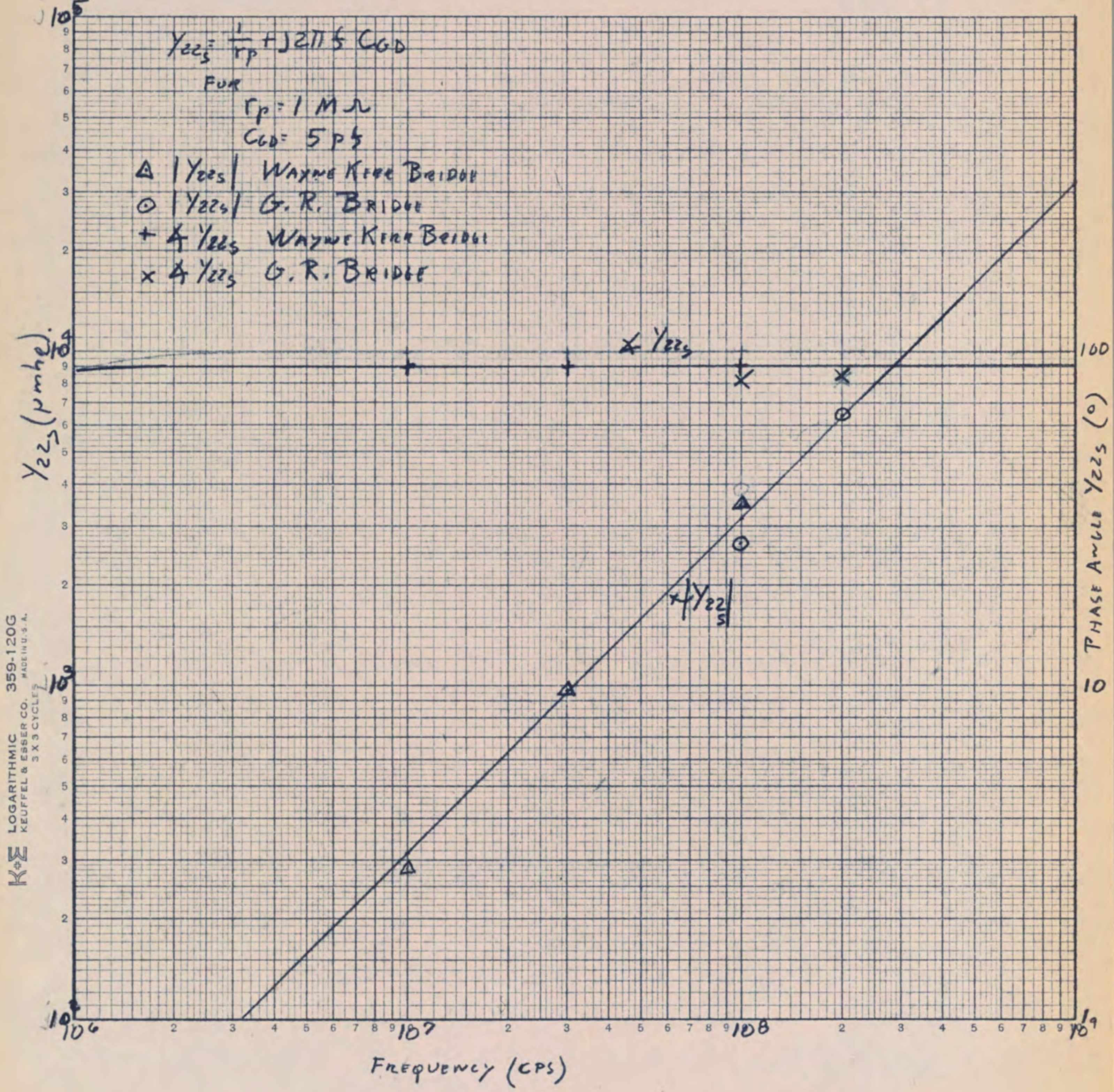


Y11s = +j 2πf (CGS + CGD)
For CGS = 11 pf
CGD = 5 pf
△ Magnitude Y11s - Wayne Kerr Bridge
⊙ Magnitude Y11s - G.R. Bridge
+ Phase Angle Y11s - Wayne Kerr
× Phase Angle Y11s - G.R. Bridge
|Y11s|
∠ Y11s
|Y11s| (μmho)
Phase Angle Y11s (°)
Frequency (cps)
+j10^5
+j10^4
+j10^3
+j10^2
100
10
10^6
10^7
10^8
10^9
K+E LOGARITHMIC 359-120G
KEUFFEL & ESSER CO. MADE IN U.S.A.
3 X 3 CYCLES

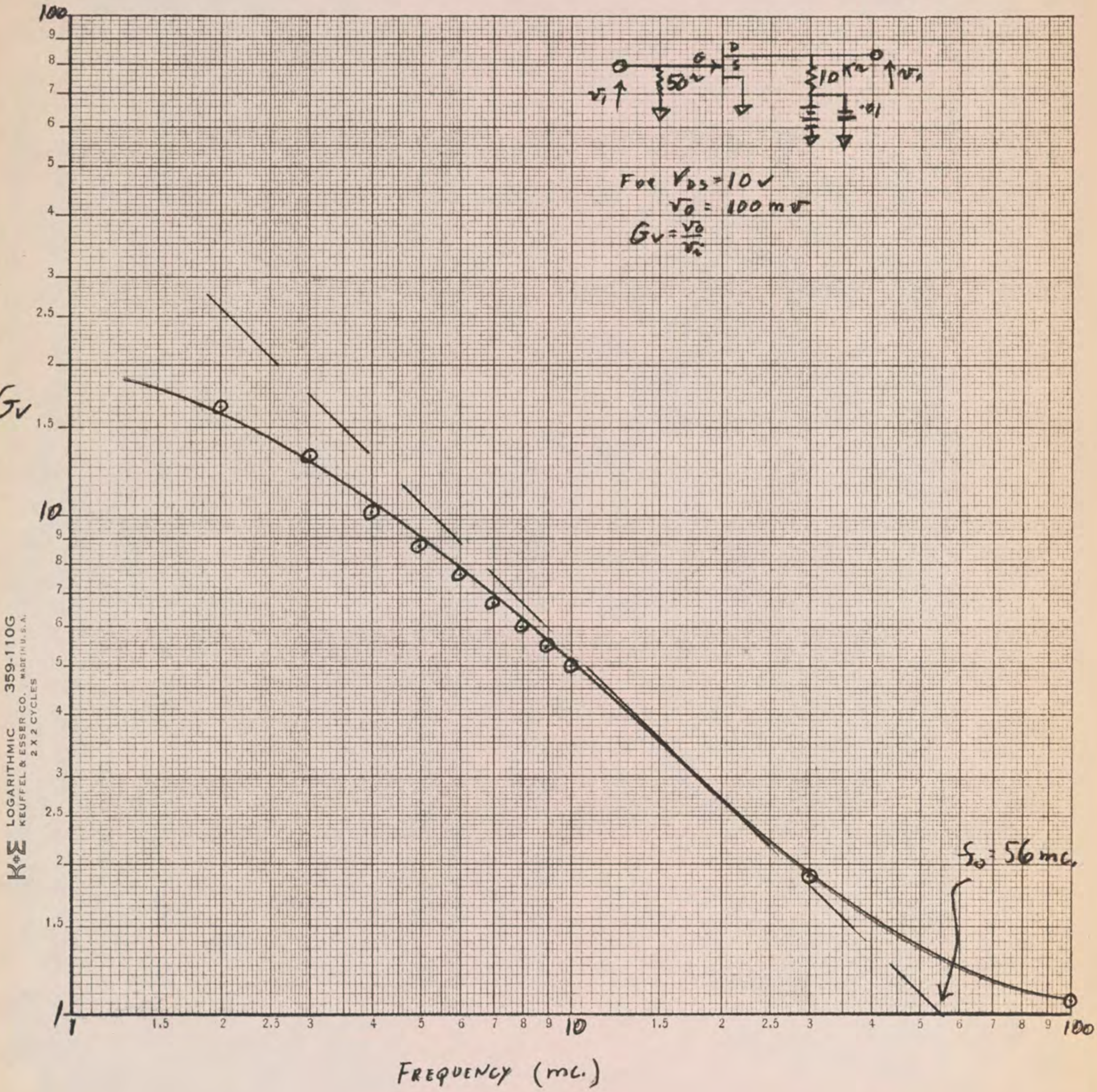


Y12s = -j2πf CGD
For
CGD = 5pf
△ |Y12s| - Wayne Kerr Bridge
⊙ |Y12s| - G. R. Bridge
+ ∡ Y12s - Wayne Kerr Bridge
× ∡ Y12s - G. R. Bridge
f ∡ Y12s
|Y12s|
|Y12s| (μmho)
Phase Angle Y12s (°)
Frequency (cps)
LOGARITHMIC 359-120G
KEUFFEL & ESSER CO. MADE IN U.S.A.
3 X 3 CYCLES

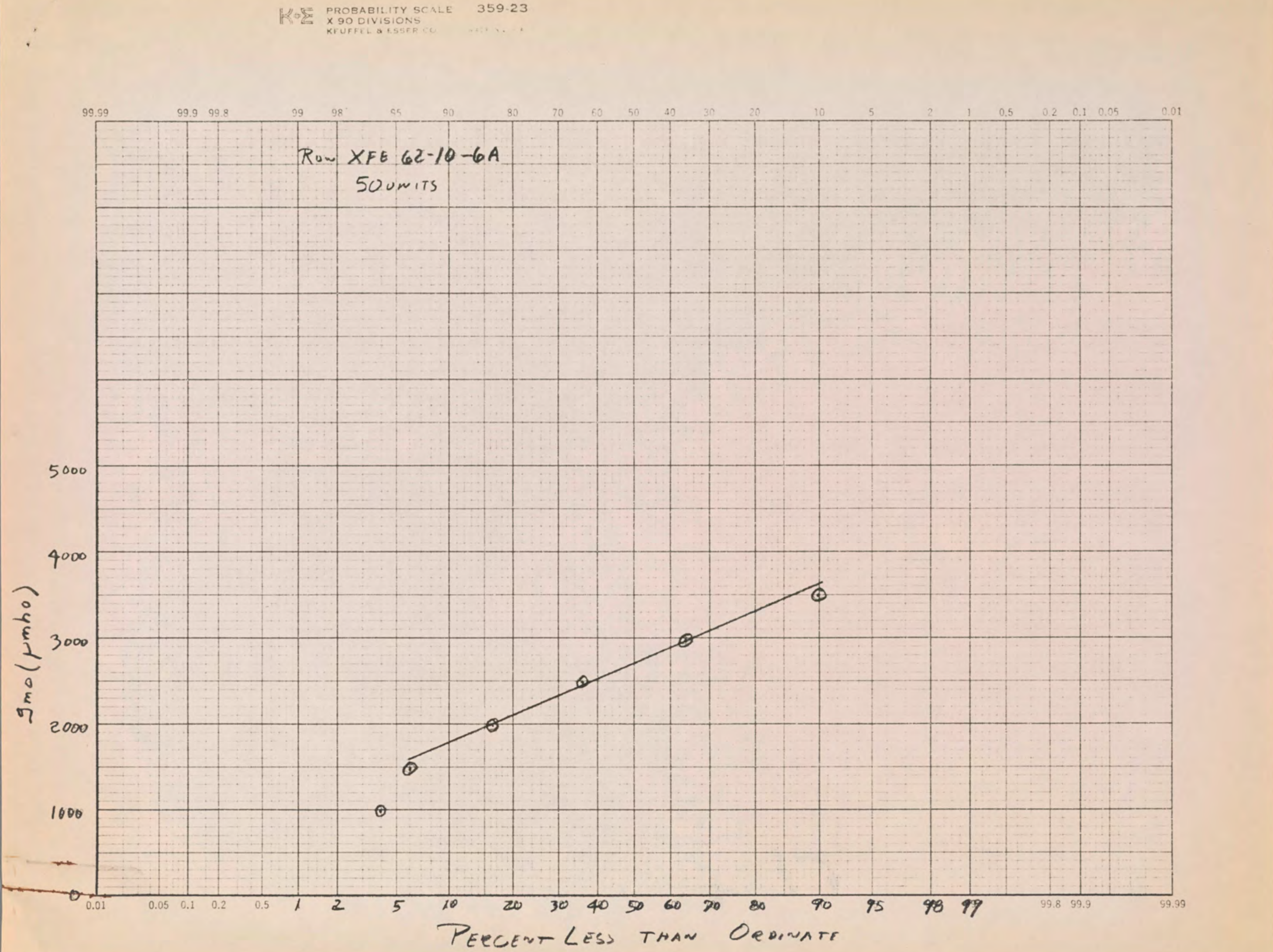

Y21s = gmo - 2π f CGD
For gmo = 2000 μmho
CGD = 5 pf
△ |Y21s| - Wayne Kerr
□ |Y21s| - From Y21G (W.K)
⊙ |Y21s| - G.R.
+ ∡ Y21s - Wayne Kerr
ǂ ∡ Y21s - From Y21G (W.K.)
× ∡ Y21s - G.R.
∡ Y21s
|Y21s|
MAG Y21s (μmho)
PHASE ANGLE OF Y21S (°)
FREQUENCY (CPS)
10^5
10^4
10^3
10^2
10^6
10^7
10^8
10^9
100
10
1
0.1
K+E LOGARITHMIC 359-120G
KEUFFEL & ESSER CO. MADE IN U.S.A.
3 X 3 CYCLES

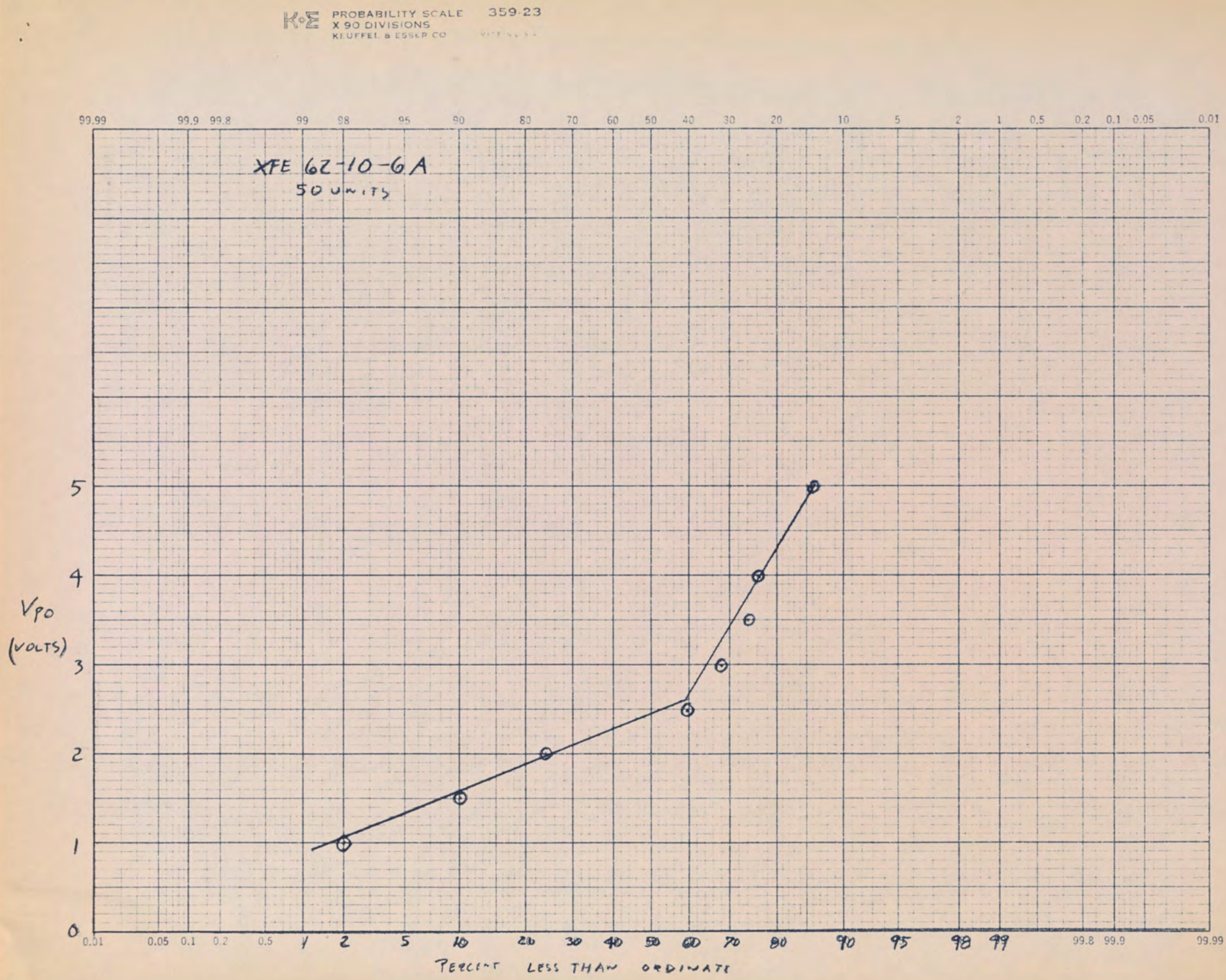


Y22s = 1/rp + j2πf CGD
FOR
rp = 1 MΩ
CGD = 5 pf
△ |Y22s| WAYNE KERR BRIDGE
⊙ |Y22s| G.R. BRIDGE
+ ∠Y22s WAYNE KERR BRIDGE
× ∠Y22s G.R. BRIDGE
∠Y22s
|Y22s|
Y22s (μmho)
PHASE ANGLE Y22s (°)
FREQUENCY (CPS)
10^5
10^4
10^3
10^2
10^6
10^7
10^8
10^9
100
10
K&E LOGARITHMIC 359-120G
KEUFFEL & ESSER CO. MADE IN U.S.A.
3 X 3 CYCLES

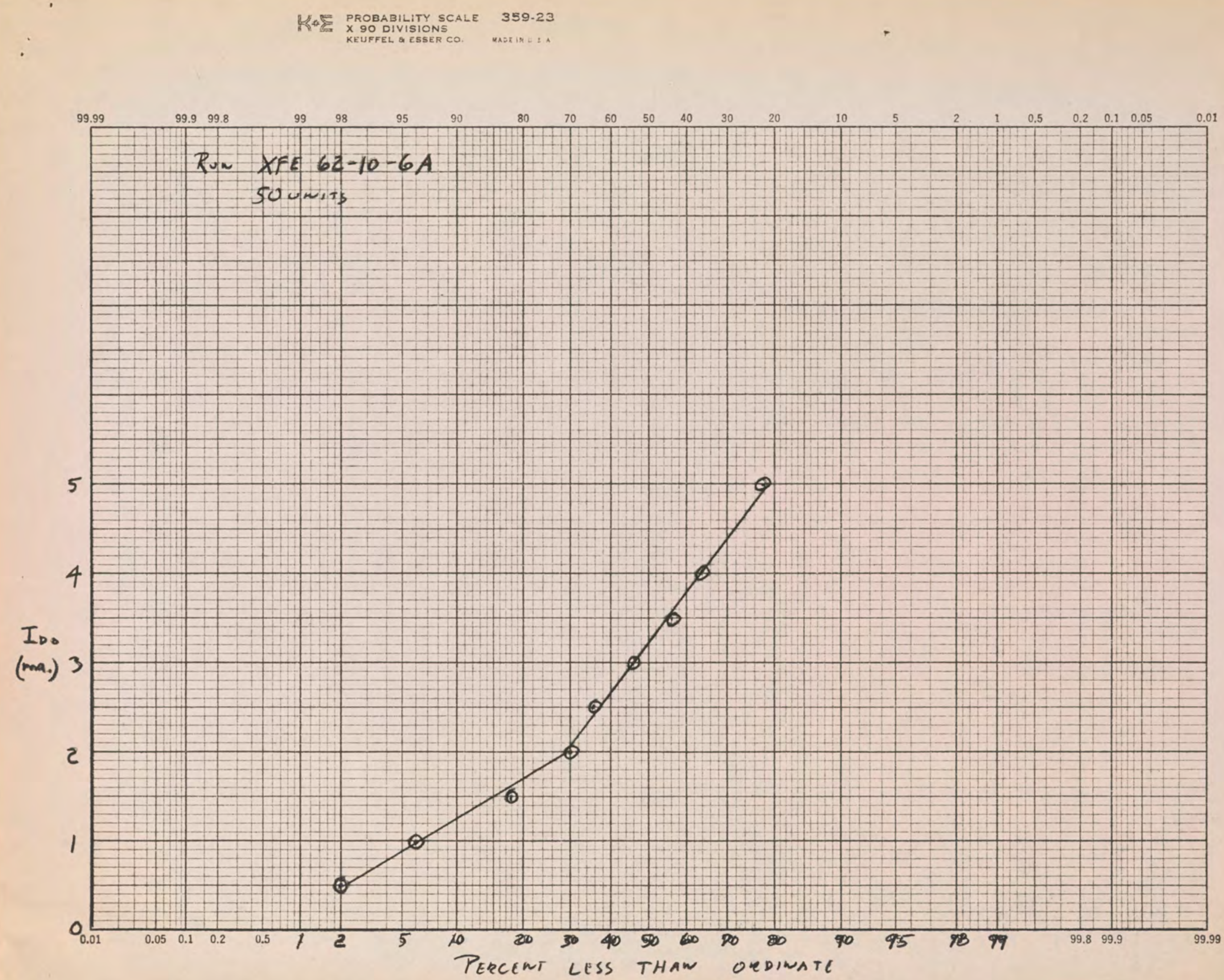


D
G
S
50Ω
$10K\Omega$
v_i
v_o
.01
For $V_{DS} = 10v$
$v_0 = 100mv$
$G_v = \frac{v_0}{v_i}$
G_v
$f_0 = 56$ mc.
FREQUENCY (mc.)
K&E LOGARITHMIC 359-110G
KEUFFEL & ESSER CO. MADE IN U.S.A.
2 X 2 CYCLES

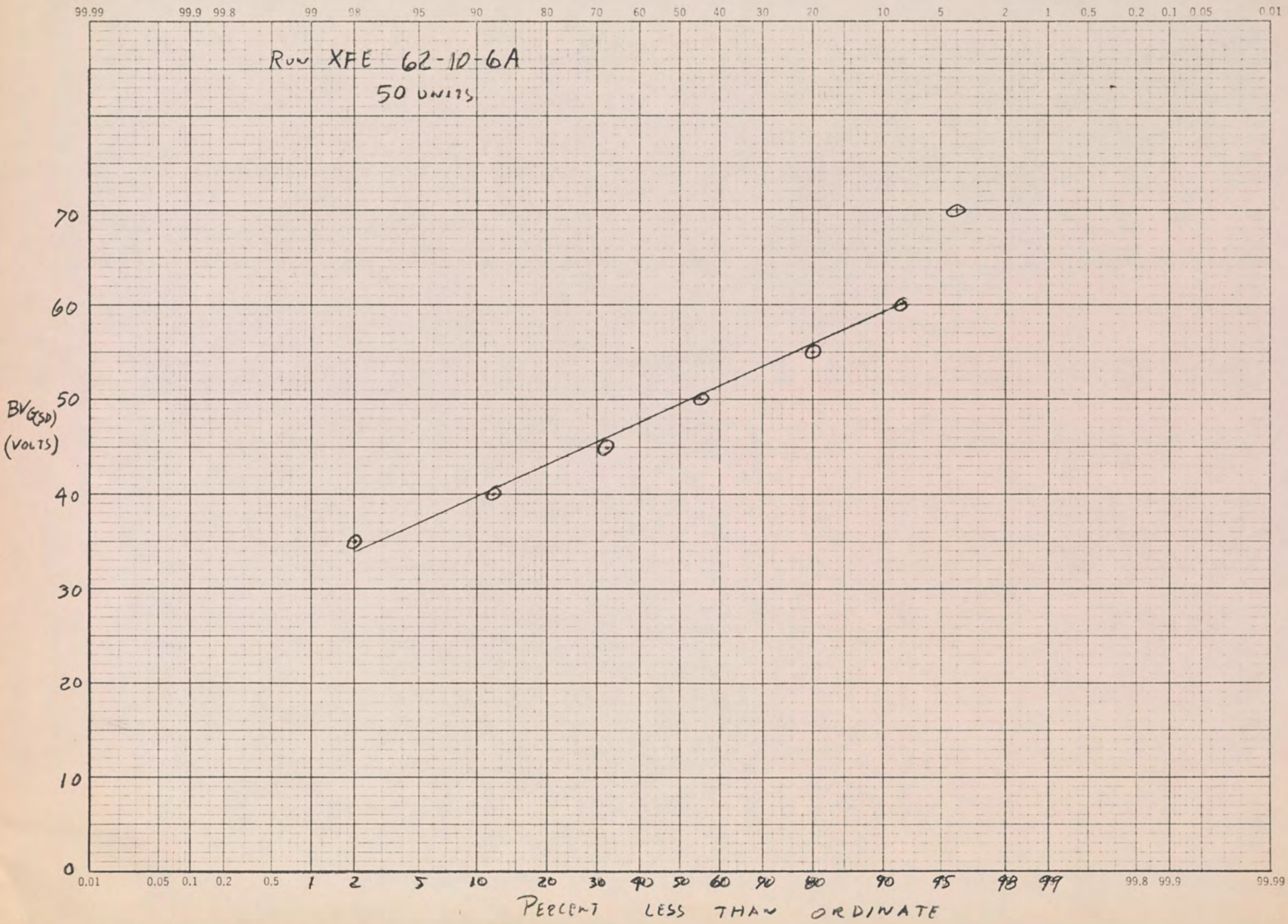

K+E PROBABILITY SCALE X 90 DIVISIONS KEUFFEL & ESSER CO. 359-23
Row XFE 62-10-6A
50 UNITS
gmo (μmho)
5000
4000
3000
2000
1000
0
PERCENT LESS THAN ORDINATE
0.01 0.05 0.1 0.2 0.5 1 2 5 10 20 30 40 50 60 70 80 90 95 98 99 99.8 99.9 99.99
99.99 99.9 99.8 99 98 95 90 80 70 60 50 40 30 20 10 5 2 1 0.5 0.2 0.1 0.05 0.01

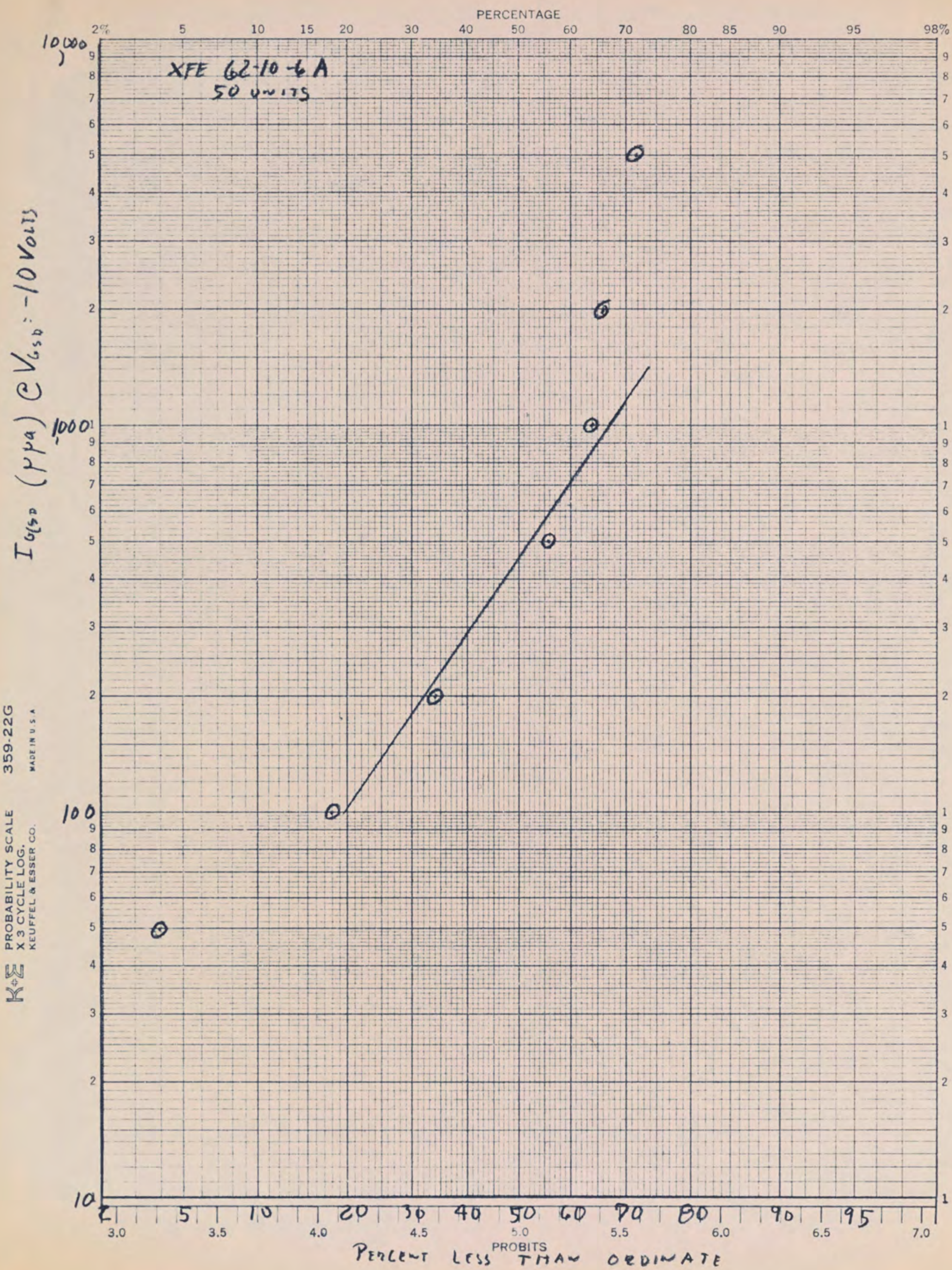


K+E PROBABILITY SCALE X 90 DIVISIONS
KEUFFEL & ESSER CO
359-23
XFE 62-10-6A
50 UNITS
Vpo (VOLTS)
PERCENT LESS THAN ORDINATE


K+E PROBABILITY SCALE 359-23
X 90 DIVISIONS
KEUFFEL & ESSER CO. MADE IN U.S.A.
Run XFE 62-10-6A
50 units
I_{DO} (ma.)
0
1
2
3
4
5
0.01 0.05 0.1 0.2 0.5 1 2 5 10 20 30 40 50 60 70 80 90 95 98 99 99.8 99.9 99.99
99.99 99.9 99.8 99 98 95 90 80 70 60 50 40 30 20 10 5 2 1 0.5 0.2 0.1 0.05 0.01
PERCENT LESS THAN ORDINATE

K+E PROBABILITY SCALE 359-23
X 90 DIVISIONS
KEUFFEL & ESSER CO





XFE 62-10-6A
50 UNITS
PERCENTAGE
PROBITS
PERCENT LESS THAN ORDINATE
I_{GSD} (pA) @ V_{GSD} = -10 VOLTS
10,000
1000
100
10
K+E PROBABILITY SCALE X 3 CYCLE LOG.
KEUFFEL & ESSER CO.
359-22G
MADE IN U.S.A.

P. 117
4/10/63

April 10, 1963

FET Status

An outdiffused run with structures as shown in figs. 1, 2 and 3 has recently failed. It was desired to have no metal touching oxide but, due to the dimensions of the FET, the bonds not only touched the oxide but, in most cases, also crossed the junction. More units are presently being bonded with 0.4 mil wire in an attempt to isolate the metal contacts. One other outdiffused run and one epitaxial run are in the latter stages of processing and will be out by 15 April 1963.

Two runs of outdiffused circular geometry have been tested. One had no failures at 1000 hours and the other had two failures at 170 hours, but the alignment was poor on this run. We will start immediately five more runs of this geometry to obtain more extensive data.

Opaque prints of our 1-12 mil circle masks will be available this afternoon. These will be used to check out the structures shown in figs. 1 thru 5 and will be of sufficient size to allow containment of bond areas by the metallization.

In addition, new sets of masks are being designed, really a modification of other circular designs, to incorporate separate gate contacts, cut oxide over N-channel, N+ wider than metallization. The option will also be provided for oxide removal over all gate area, a la Amelco. Of necessity, this device will be much larger than the U-I.

The P channel units are surviving on life test, but the initial run had 0 hour nanoamp leakages and equivalent noise resistances of 5-6 MΩ. The leakages have decreased by a factor of 5-10 by 81 hours.

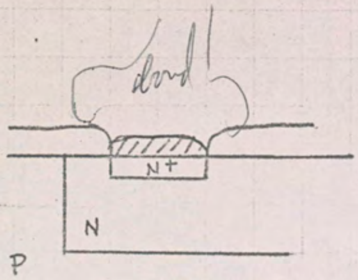


fig 1

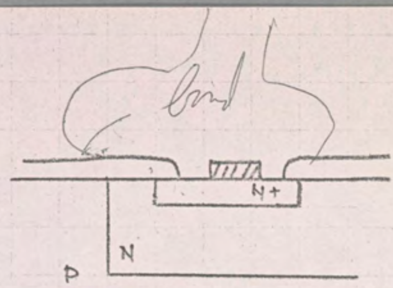


fig. 2

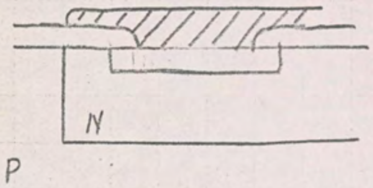


fig. 3

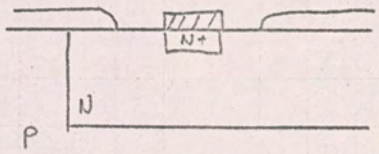


fig 4

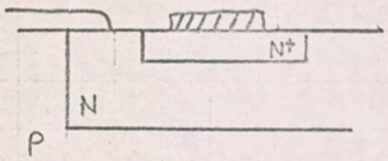


fig. 5

Field Effect Meeting 4/10/63

Smith, Seeh, Ragle, Jezarn, Moore, Hilbiber, Ardeff, Bittmann, Seistiko, Bethel

Seistiko:

63 circular devices from 4 runs tested.
Out of this bunch 8 "failed" at various times. A failure is defined as I_{SGO} going to ~1 ma at 30v
~~30v~~ 22½v, 200°C

All other tests are at 30v, 150°C.

It appears to me that in order for this to fly it is necessary that we establish that almost adequate reliability exists.

"almost adequate" reliability
≜ < 1%/1000 hrs under any conditions within rating.

Program:

1. Geometry effect check out to see any differences — testing or geometry.
2. More p-channel and collect data.
3. After data on diodes (2 weeks) (end of next week), then new masks.

4/16/63

Discussion c RHN on Signal Corps proposal for 10 Mc logic ckts.

RHN
JPF

Required: Delivery of 25 ea of ~ 5 ckts in 6 MO
" " additional units at end of year.

a) A std gate - ~5-input NOR

b) gate expander

c) Flip-flop - a "R" element c all extra garbage

d) Delay element - a 1-shot c an external capacitor

e) Power gate - (gate c emitter follower) fan out of 30; but only one clock delay)

These are for all Signal Corps ~~Field Data~~ equipment. They will also be the high speed set for SOSO's present customers.

Questions to answer:

1. Can we take on this job? —Yes - JPF

2. If we can, is it worth taking on? —Yes JPF

3. Shall we take it on? —Yes - ME.

JPF says this looks good on the basis that we can use it to try DTL, on present idea of highest speed, and then ~~recovery~~ recover on the DCTL, which is adequate, if necessary.

Potential is 50,000,000 units.

We will do ~~all~~ all the contract units

4/17/63 — PNP & power product planning meeting

Richmond, Yost, Ouchall, Bay, Knudsen, Schultz, G Doster, Hoerni, Moore, Valentine

6206 – Internal specs out
Data sheet posted by 4/30. Give a power vs voltage at two points
38v @ 400 ma at room temp for test. → 93% yield of units ok otherwise
Guarantee 10 watt at 400; 15 watt @ 1 amp.
M.O. would like to not set leakage spec at 100 ma @ 60 v. – Decision on Apr 30.
Aim at 1500 units then lead weld/jobs
668 made to date on (TR) header
4 -- on other header FC
The $V_{CE(SAT)}$ is left with slop in case we go to an emitter resistance structure.
Ouchall is trying masks with emitter resistance included. Will know by next meeting.
Will have 2000 in stores in 3 weeks in inventory
need 2000 for distributors.

R&D new work — There is a need for a pulse switching power device. We should look at it.
This is a device to switch power without dissipating it.

Ouchall wants to isolate collector. As yet we have no method of doing this job. Doster is looking at this from the point of view of using metallized BeO.

R&D → R&D should look at some of the new materials for this, say pyrolytic BN.
Then will take out that on BeO.

We are better than all competition across the board.

7006 – M.O. has started 2 - runs a - none out. (placed about it) Exactly like 6206 except for mask.

WHG & BK. think that the extra power will be trivial, so it is not really worth doing.
M.V. thinks we would be better off than the limited competition.
It would be ~ 7½ amp device and ~ 30 watts.
Schedule 6 runs with new mask using built in emitter resistor will be out in 30 days.

 Product planning meeting, cont.

8000 – JPF thinks we should only work on either this or the big SCR, but not both.

SCR-3 3amp, 400v
We are ok on all but V_{SAT}. Frank is fixing up to make runs down here.
R+D will run in parallel until M.V. is running.

SCR – IBM (We have) shipped 800 R+D units? Nobody knows.
Because we were late, we missed out on 500,000 units.
Marketing will

SCR-1 ~200v, 1amp – maybe after SCR-3

7506 – Ours got channels on life. No product until we solve high^tht voltage problem.

1713 – In production, aim at 10,000 lead welds per week at April 30.
Boggs for 20v.
– Announce end of May. ~~with 7000~~

1702 – This is faster than the Ge devices above 10 ma, the important region. It is a 3-stripes.

As M.V. ~~gen~~ can do and as marketing wants, we consider

0005 – Two runs which aborted on life. ∴ 3511 + 4511 done again
We have made 6 runs of 3511's that looked ok.

four current device.

4/18/63 — Meeting c̄ ~~Stats~~ u ckts (p. 105)

Graham
Ferguson
Shrimit
Mann

Litton ckts:

Ø Drivers: Masher "about" ~~going~~ in "a in". This was delayed or two weeks by specs. negotiation.

~~Preamp~~

Preamp. — Kearns & Barnett doing work to define what ckt will do their function. When we agree on a ckt, this can be re-scheduled.

Our Modus-Operandi will be straightened out.

Meeting on Contract Proposal: 4/22/63
SDSD (See p. 118)

SDSD
Rudin
Anderson
Bogart

Novadel
Tatter
Farina
Ferguson
Grinich
Moore

They want a prop. delay than 7 stage ring counter (loaded) corresponding to 10 ns.

	6 MO	12 MO
"FLIP FLOP" (Calculon R)	25	250
GATE	25	250
POWER GATE	25	25
GATE EXPANDER	25	75
Delay element	25	25

What have we breadboarded?

1. The gate (c̄ epi bit parts) - get ~ 12 ns @ 10 mw.
   It won't go much faster at ~~lower~~ ~~power~~. higher power

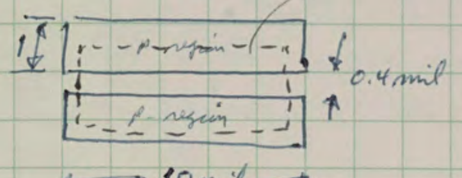
2. The Flip Flop (breadboarded except no storage diode c̄ isolation). Speed looked marginal at regular power. Needs higher power to load diode.

Meeting on MOSTs – 4/22/63

Grinich
Ferguson
Sah
Wanlass
B Parker

Single unit:

No basic problems except those of flat wafers for fine tolerances.



On some of our devices we have evidently had problems etching all the oxide in the ~~sed~~ black square before re-growing. This has been ~~the~~ a limitation on the number of devices to come out.

For breadboarding series gates we should bring out 4 leads.

There seems to be no problem controlling the 1000Å oxide, a value ~~that~~ was chosen "because it is a nice round number".

Ox has been 4 hrs in dry O_2 @ 920°.

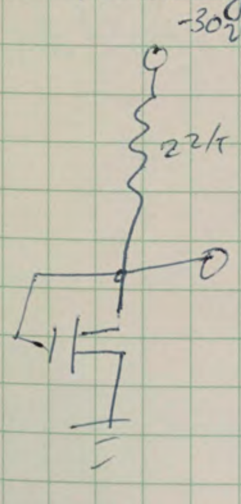
Probed yield on wafer is "a hell of a lot better" than Xstors – looks like 90%
1Ω-cm material should have 2.9v threshold @ 1000Å oxide. They do not, however, track the resistivity ~~po~~ correctly.

Improvements: a) Shorted sources
b) Variety of oxide thickness

~~As soon as~~

As soon as we get some of these experiments thru, we will be ready for reproducibility runs.

Reliability data



@ 125°C get some initial drift, then stable.

MOST, cont 4/22/63

— Other polarity complementary device, individual structure.

We still cannot make zero conductance at 0 V_{GS}.
To date our best ~~gun~~ bar been anodic oxide.

(Hle - We could use a guy here to learn to make.)

CTS will try to get a guy near here to switch over.

— Complementary structure in one wafer
(Nothing now being done)

— Memory array

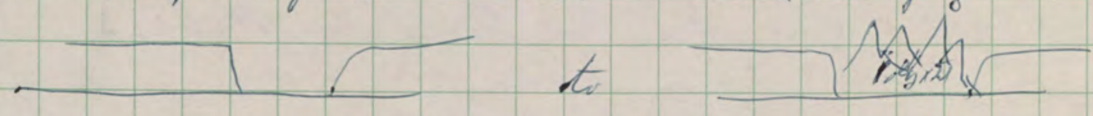
 April 24, 1963 – Epitaxial defects

Barnes
Sandor

Tucker

Defects:

1. Pyramids
2. Macroscopic pit defects (crater) – most annoying now



3. Mesa

4. Stacking fault (usually need a light etch)
5. Extreme surface roughness

Mapping to follow.

They have been consistent in tracking Macroscopic Pit Defects

Causes ~~identified~~ accused.

1. Surface contamination
2. Surface condition
3. ? Points in surface that do not etch or polish like the rest
4. Strained crystal
5. Condition of run.
   a) Contaminated reactants
   b) vapor etching
   c) growth condition
6. Variables in the reactor.
   a) flow or turbulence
   b) thermal gradients.

Crater

Cause of ~~pit~~ crater is a tightly adherent, flat, black spot. It can removed with tweezers.

Such a particle is also shown as a bad spot in the grids.
These are, however, evidently air-born contamination. Range up to 5μ in size.

Mesa: Irregularity in substrate making "sand dunes".

Roughness: 1. Bad H_2
2.

F/4 - 4/23

FAIRCHILD SEMICONDUCTOR

RESEARCH & DEVELOPMENT LABORATORY

TO: List

DATE: April 18, 1963

FROM: C. T. Sah

CC: → G. E. Moore
V. H. Grinich

SUBJECT: Agenda for Project Review Meeting
Wednesday, April 24, 1963 - 10:00 A.M.
Imperfections in Epitaxial Films
Project 120 and 128

The purpose of the meeting is to review the experiments and results that have been obtained recently on the origins and elimination of imperfections in silicon epitaxial films, the effect of substrate surface preparation on the film perfection and the characteristics, properties, and origin of stacking faults in these films.

AGENDA:

10:00 A general and brief outline of the results obtained. (Tucker)

10:30 Stacking faults. (Tucker)

11:00 Effect of substrate surface preparation. (Barry)

11:30 Experiments and results of elimination of defects. (Davis, Barry & Yim) 6

Please have all data summarized and important data and photographs reproduced each for 10 copies for efficient presentation.

C T Sah

C. T. Sah
Solid State Physics Section

CTS:jt

List: (Participants)

R. Tucker ✓
D. Barry ✓
A. Davis ✓
C. Bittmann ✓
P. Flint ✓
J. Gordon ✓
J. Lawrence
A. Grove ✓
A. Roder ✓
W. Shepherd ✓
H. Wigton ✓
E. Yim ✓
Seymour
Moore

105

103 SILK CrO, ZrO₂, chem etch

101 SILK C&O

104

102

100

COMPANY PRIVATE

FAIRCHILD SEMICONDUCTOR

RESEARCH & DEVELOPMENT LABORATORY

PROJECT 128 - STATUS REPORT

D. BARRY
4-23-63

SUBJECT: PREPARATION OF PERFECT SUBSTRATE

The preparation of a perfect substrate in this project is interpreted as the preparation of flat silicon wafers free of scratches and pits.

Several methods are available to prepare substrate material; chemical etching, mechanical polishing, mechanical-chemical polishing, and anodic polishing. The only method to obtain flat surfaces, however, is the mechanical polish procedure. Therefore, this report will be limited to experiments in mechanically polishing silicon.

The procedure for mechanically polishing silicon consists of 1 1/2 hour polish or Buehler silk with cerium oxide on the Lapmaster followed by a 1/2 hour polish on Buehler microcloth with zirconium oxide on the AO bowl polisher. Before polishing, the wafers are mounted on a steel block, lapped flat at least 90 μ of material removed to get below saw damage.

Several experiments were performed to improve the mechanically polished surface.

1. Use of 1/4 micron diamond on Buehler microcloth with kerosene lubricant on AO polisher.
2. Cerium oxide on silk on the Lapmaster for 1 1/2 hour.
3. Cermium oxide on silk for 1 1/2 hour followed by 1/4 hour on microcloth with lustrox (a zirconium oxide precipitated solution).

4. Cerium oxide on pellon cloth on Highland Park for two hours.
5. Cerium oxide on pellon cloth on Highland Park for 1 1/2 hour followed by 1/2 hour on microcloth with cerium oxide on Highland Park.
6. Shamvra (MgO) on microcloth on AO polisher followed by 1 1/2 hour on silk with cerium oxide on Lapmaster.
7. Zirox (zirconium oxide) on microcloth on AO polisher 1/2 hour followed by 1 1/2 hour on silk with cermium oxide on Lapmaster.

The results obtained in all cases is strongly dependent on the lapped surface obtained before mechanical polish is initiated, chipped edges and non-flat lapped surfaces lead to scratches or uneven polishing. The procedure using zirconium oxide on microcloth on the bowl polisher tends to round out the edges of the lapped wafer. Then, a final polish on silk on the Lapmaster with cerium oxide produces a polished surface practically free of scratches and other surface blemishes. This procedure seems to give the best results to date.

DB:jt

COMPANY PRIVATE

PROJECT 128 - SILICON EPITAXIAL FILM

E. Yim

I. To eliminate defects which are associated with dirts and other foreign particles on substrate surface, drying and loading are carried out in the positive pressure hood with clean air.

II. To eliminate pyramids, the following HCl vapor etching steps are used:

Step 1: 20 minute zero point HCl vapor etch @ 1175-1180°C optical;

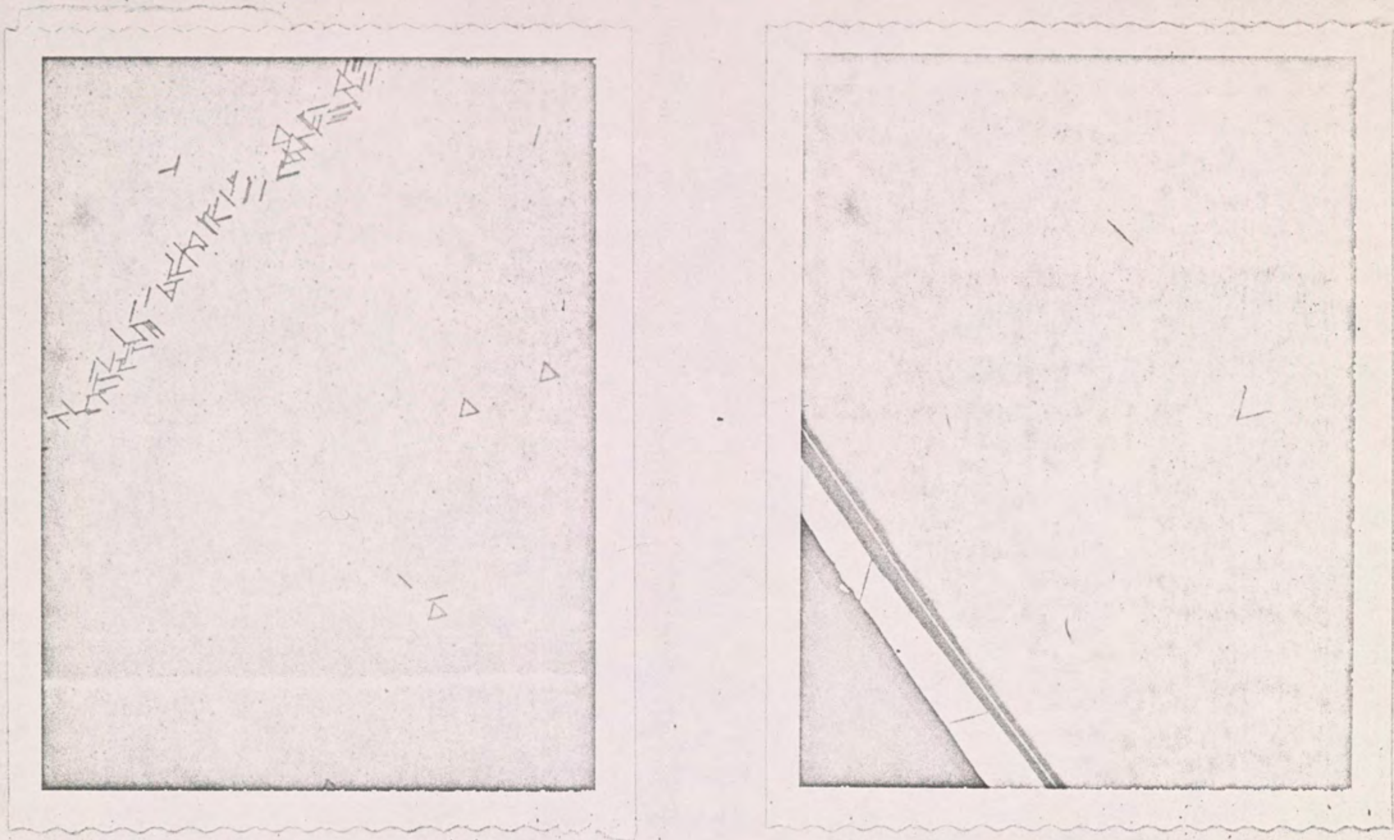
Step 2: 5 minute slow growth with HCl vapor;

Step 3: fast growth to obtain desired film thickness.

In the following table, partial pressures and meter settings for the growth cycle are presented:

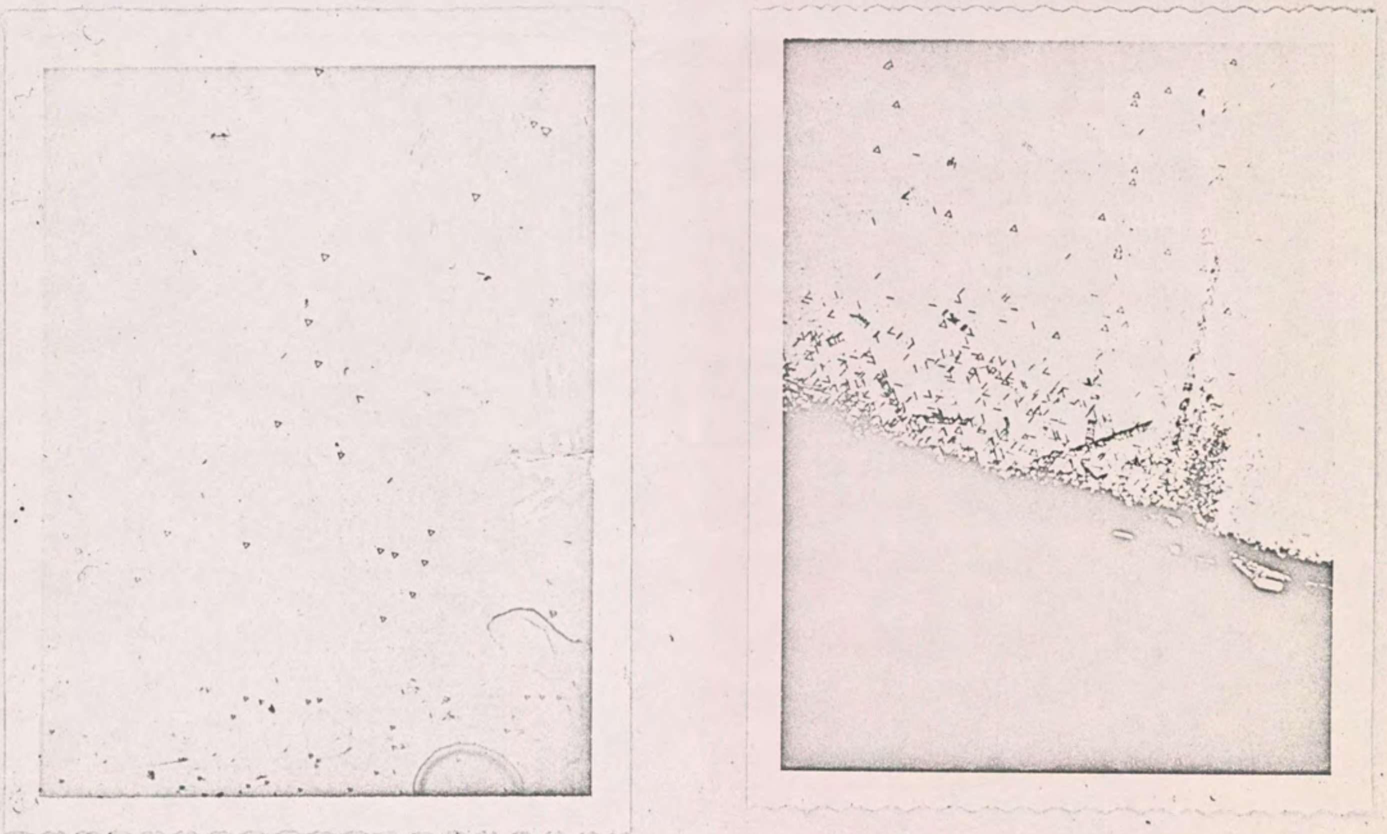
				TABLE			
	P_{H_2}	P_{HCl}	P_{SiHCl_3}	2 SCFM H_2 meter reading	0.15 SCFM H_2 meter reading	ml $SiHCl_3$ per min.	μ Si deposited
Step 1	0.924	0.0116	0.00195	100	55	0.5	0
Step 2	0.991	0.008	0.00196	100	45	0.5	+ 0.16
Step 3	0.995	0	0.0047	100	0	1.2	1.0

Photographs, substrates, epitaxial films and electrical results are presented.



E3

2 c) Substrate oxidized (steam, 1200°C, 2 hrs) and stripped prior to epitaxy.



D-1

2 d) Substrate oxidized (pyrolytic) and stripped prior to epitaxy.

Stacking fault Study.

Run 1-517 — Wafer C

Silver dot (?)

1st row nearest edge

28 { 2 soft (2 SF)
1 DB (✓)
1 short (1 SF)
24 good

2nd row

28 { 2 soft (1 D, 1 good)
1 DB ✓
1 short ✓
24 good ✓

3rd row

28 { 2 DB (2 SF)
26 good (25 ✓, 1 SF)

94 — ✓	96 — ✓	95 S ✓
92 — ✓	92 — ✓	90 — S
90 — ✓	90 S ✓	85 S F
90 — ✓	89 — ✓	89 — ✓
90 — ✓	89 — ✓	89 — ✓
90 — ✓	88 — ✓	89 — ✓
90 — ✓	89 — ✓	89 — ✓
90 — ✓	90 — ✓	90 — ✓
90 — ✓	90 — ✓	DB · ✓
90 — ✓	90 — ✓	90 — ✓
90 — F	DB · ✓	90 — ✓
90 — ✓	90 — ✓	90 — ✓
90 — ✓	91 — ✓	90 — ✓
90 — ✓	90 — ✓	90 — ✓
90 — ✓	90 — ✓	90 — ✓
90 — ✓	90 — ✓	90 — ✓
91 — ✓	90 — ✓	90 — ✓
92 — ✓	91 — ✓	90 — ✓
92 — ✓	91 — ✓	91 — ✓
91 — ✓	91 — ✓	92 — ✓
90 — ✓	92 — ✓	92 — ✓
92 — ✓	92 — ✓	91 — ✓
DB · F	92 — ✓	92 — ✓
92 — ✓	93 — ✓	93 — ✓
93 — ✓	93 — ✓	92 — ✓
93 — ✓	93 — ✓	92 — ✓
94 — ✓	94 — ✓	90 — ✓
95 — ✓	95 S D	96 S F
DB · F	Short — · ✓	Short — · F

stacking faults (6) → 2 : soft
1 : short
2 : double break down
1 = good.

defective junctions (10) → 5 = stacking fault
1 = other defect.
4 = no apparent defect.

Run 4-394

Chem polish wafer.

stacking faults (10) → 6 : double breakdown
2 : soft
2 : good.

defective junctions (34) → 8 : stacking faults.
6 - other defects
20 - no apparent damage.

Mech. Polished wafer:

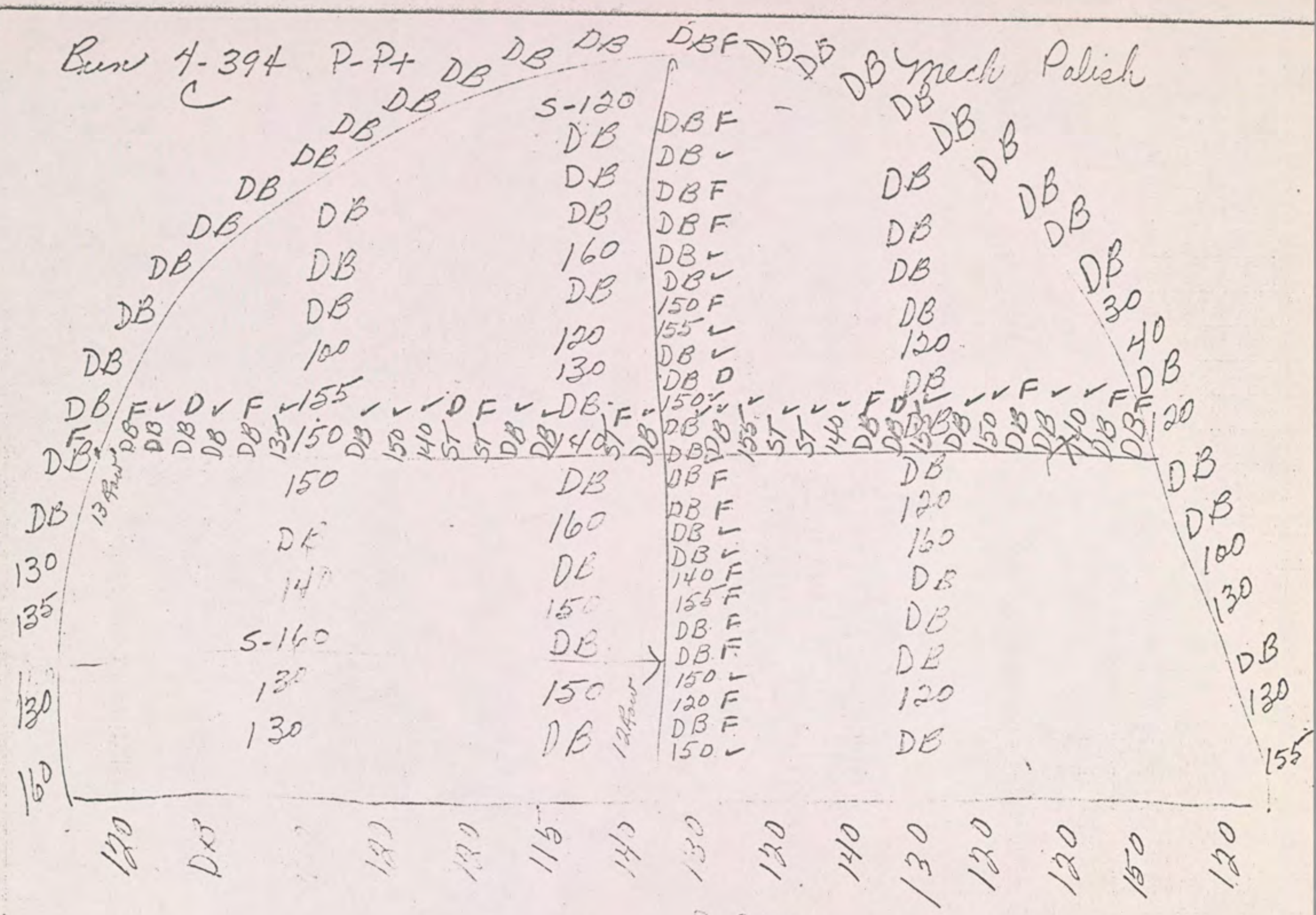
stacking faults - (22) → 16 = double breakdown
2 - soft
4 - good

defective junctions - (41) → ~~18 soft~~
18 : stacking faults
4 = other defects
19 = no apparent defects.

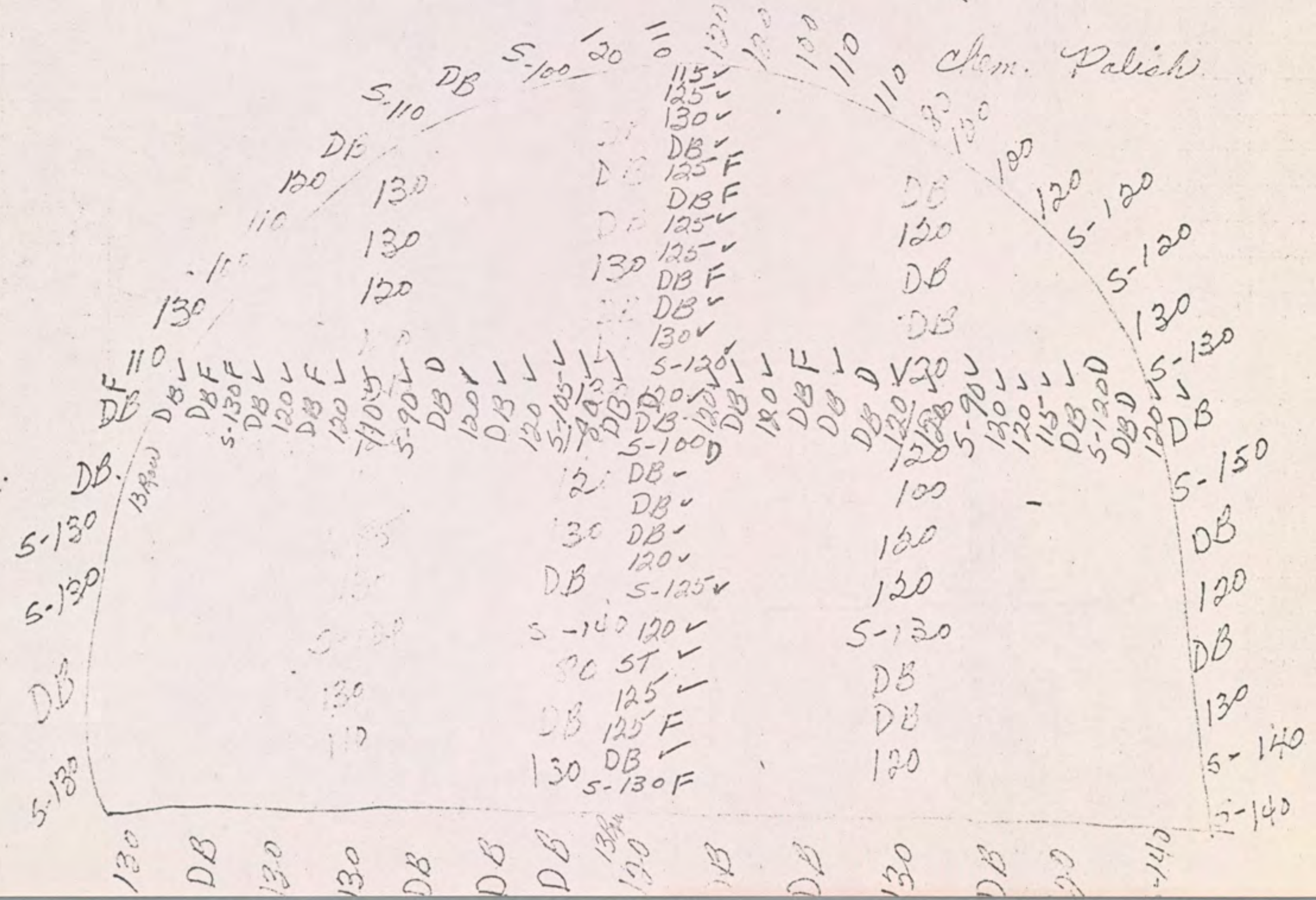
Totals.

stacking faults : (38) → 24 double breakdown.
6 soft.
1 short
7 good

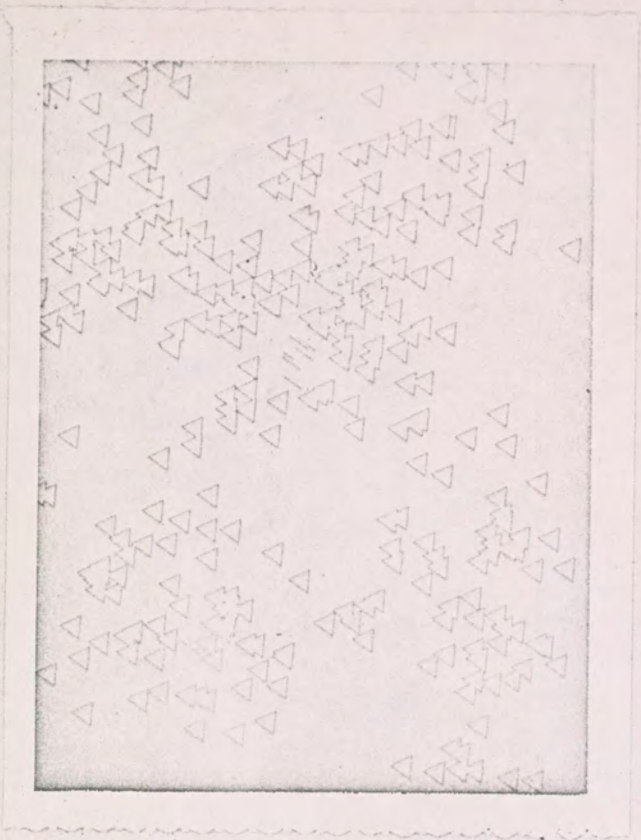
defective junctions (85) → 38 stacking faults
11 other defects
36 no apparent defects.



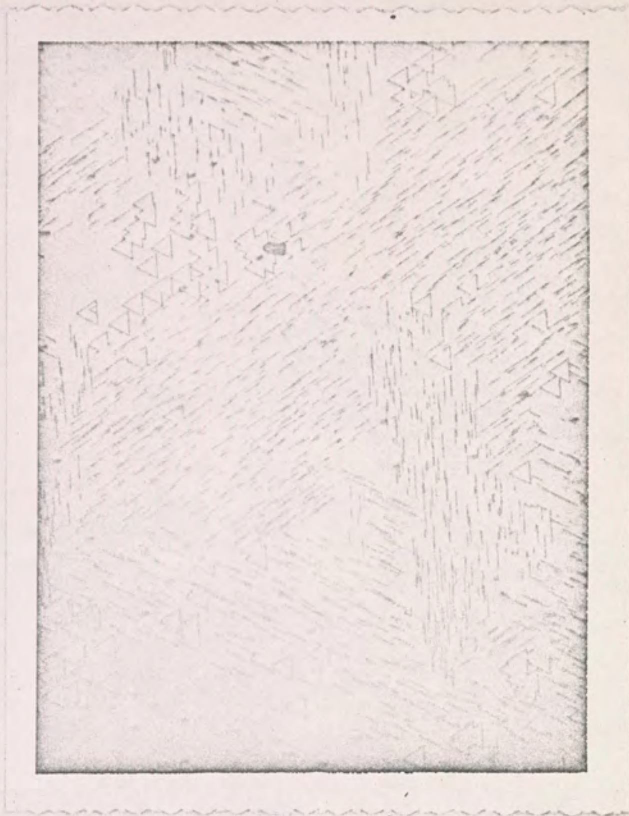
Run 4-394 C
P-P+
Mech Polish
S-120
S-140



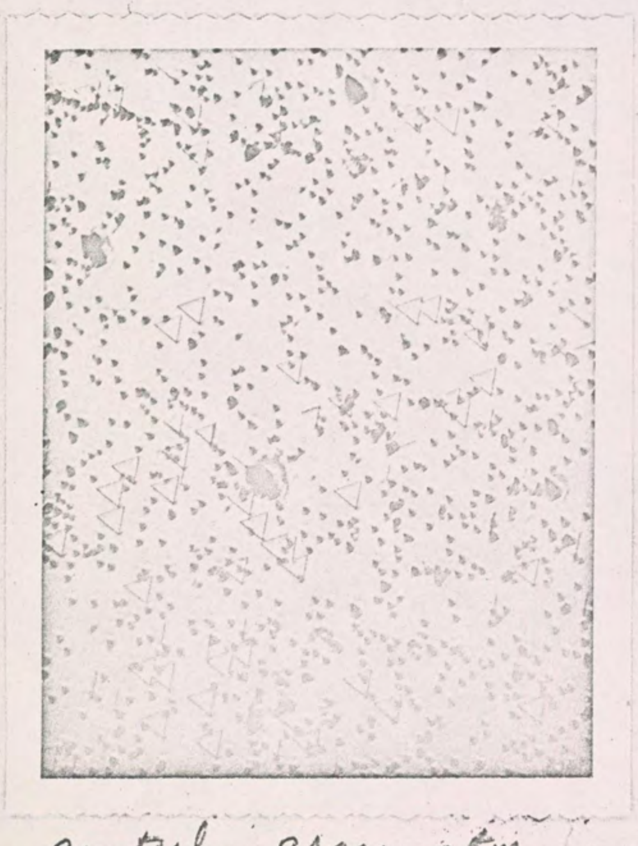
Chem. Polish
S-110
S-100
S-120
S-130
S-150
S-140



5a) Control - steam oxidized and stripped prior to epitaxy.

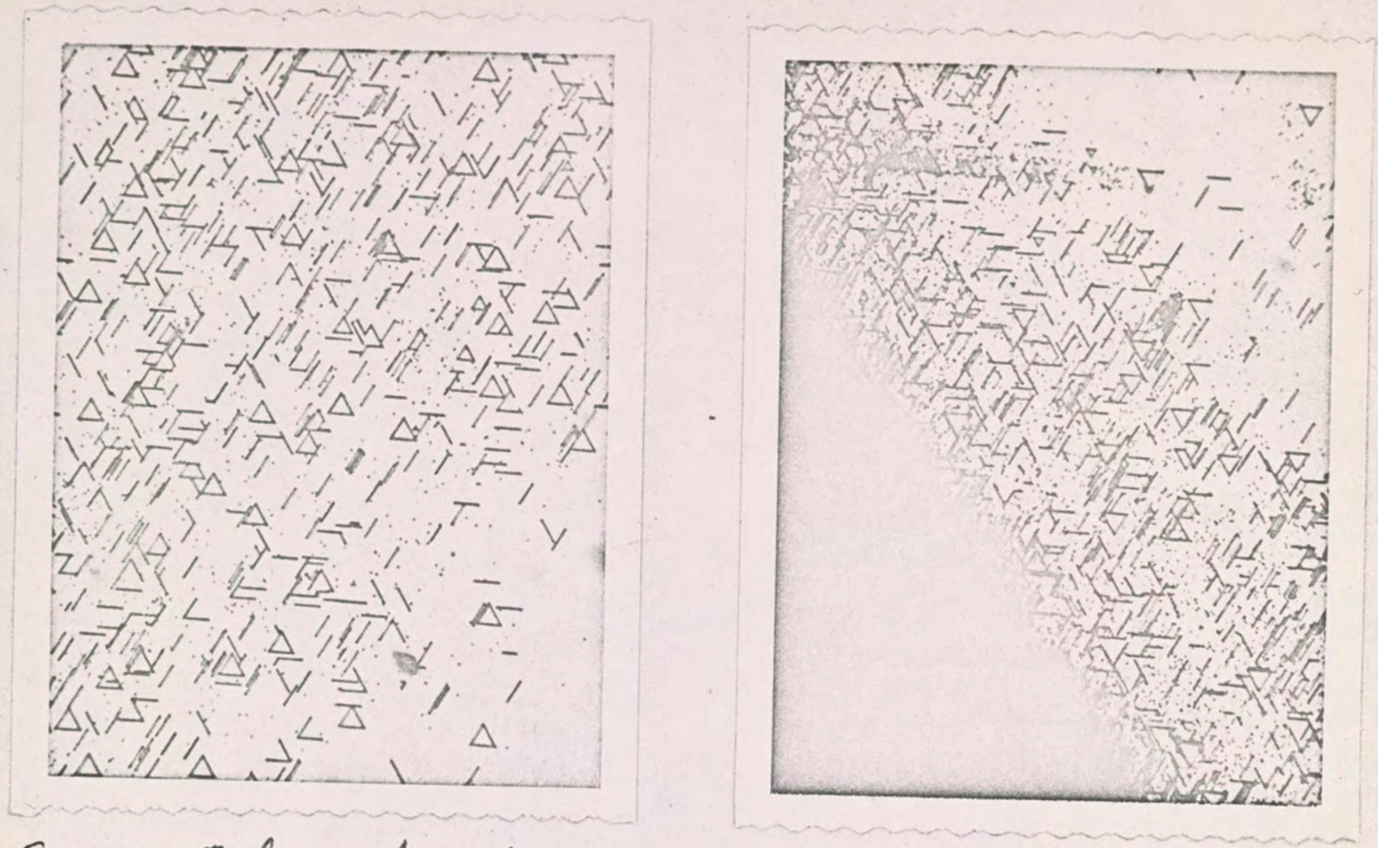


5b) Strained wafer, steam oxidized prior to epitaxy



5c. Control - argon atm. 15 min @ 1200°

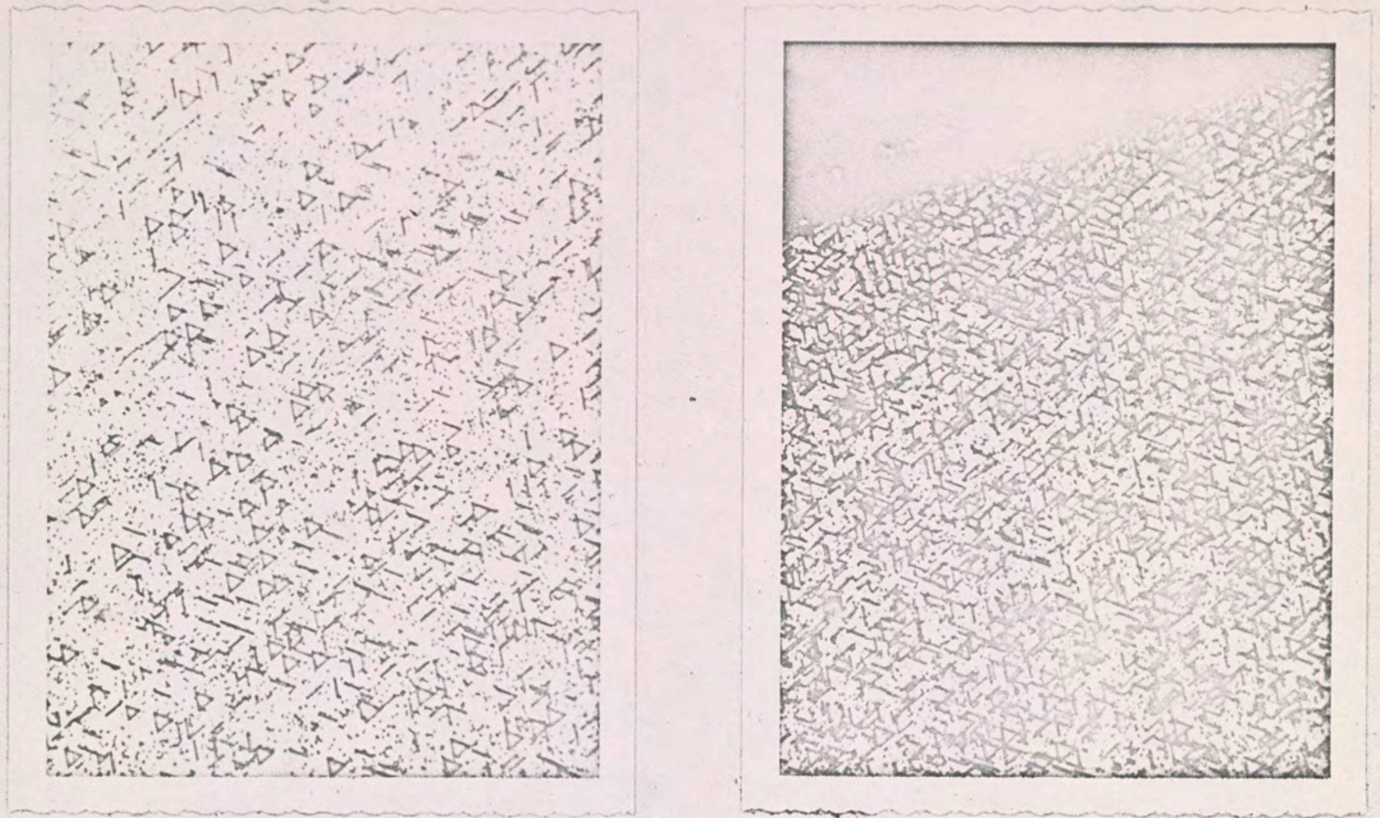
5d). Strained wafer, argon atm. 15 min @ 1200°



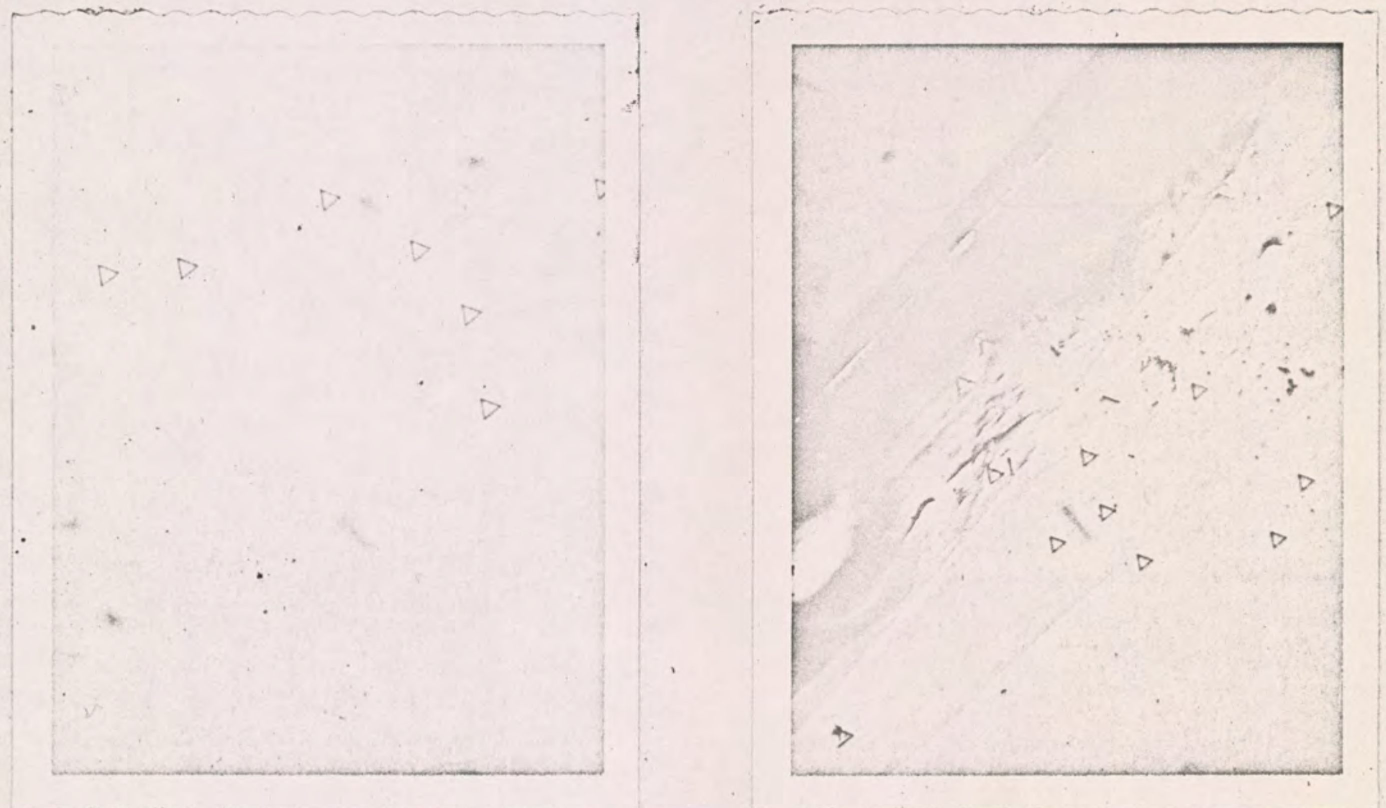
2 a. Control wafer (mechanically polished substrate).

2 b). Substrate heated for 20 minutes in argon at 920°C prior to epitaxy.

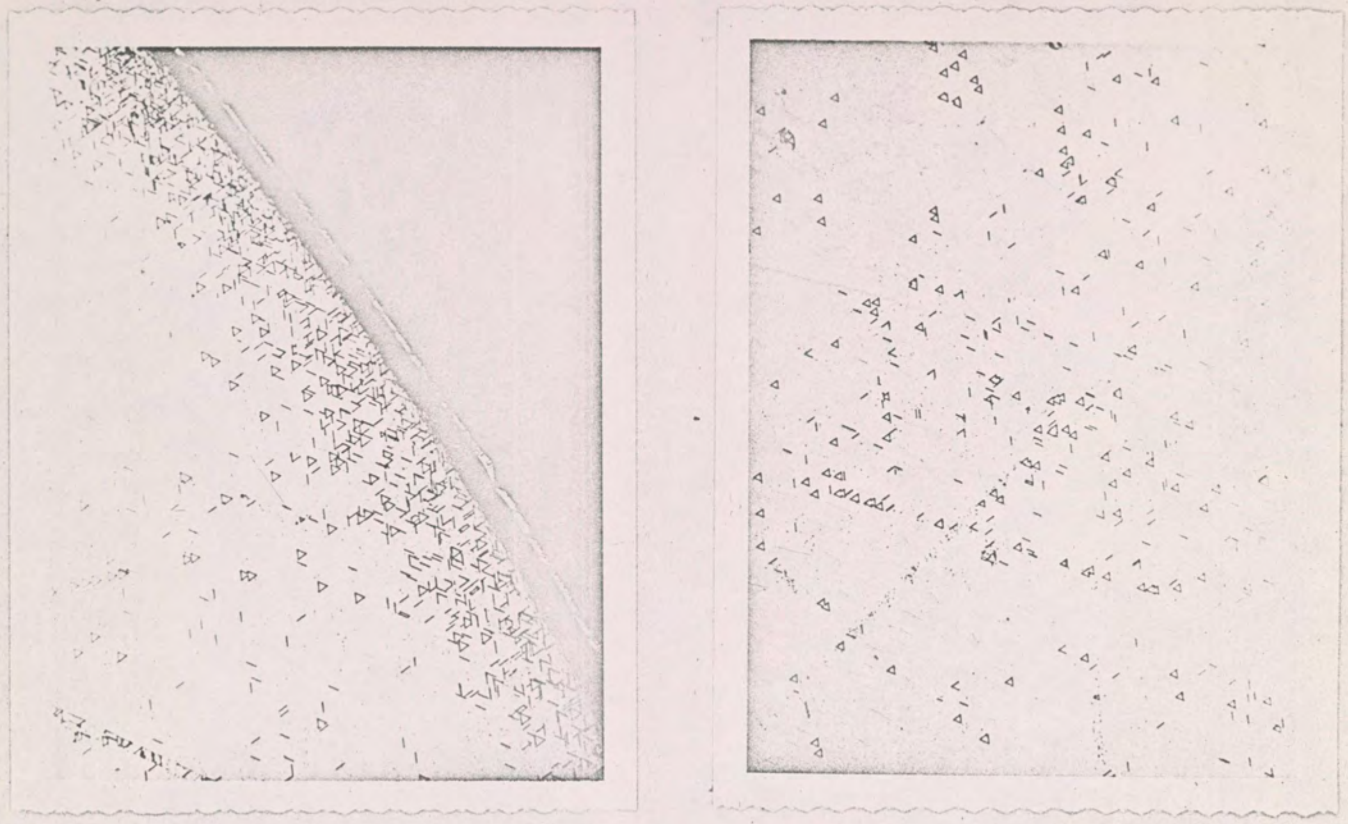
Stacking Faults



1 a). Control wafer: mechanically polished substrate, zero etch 20 min, slow dep. 5 min, fast dep. 18 min → ~25 μ.

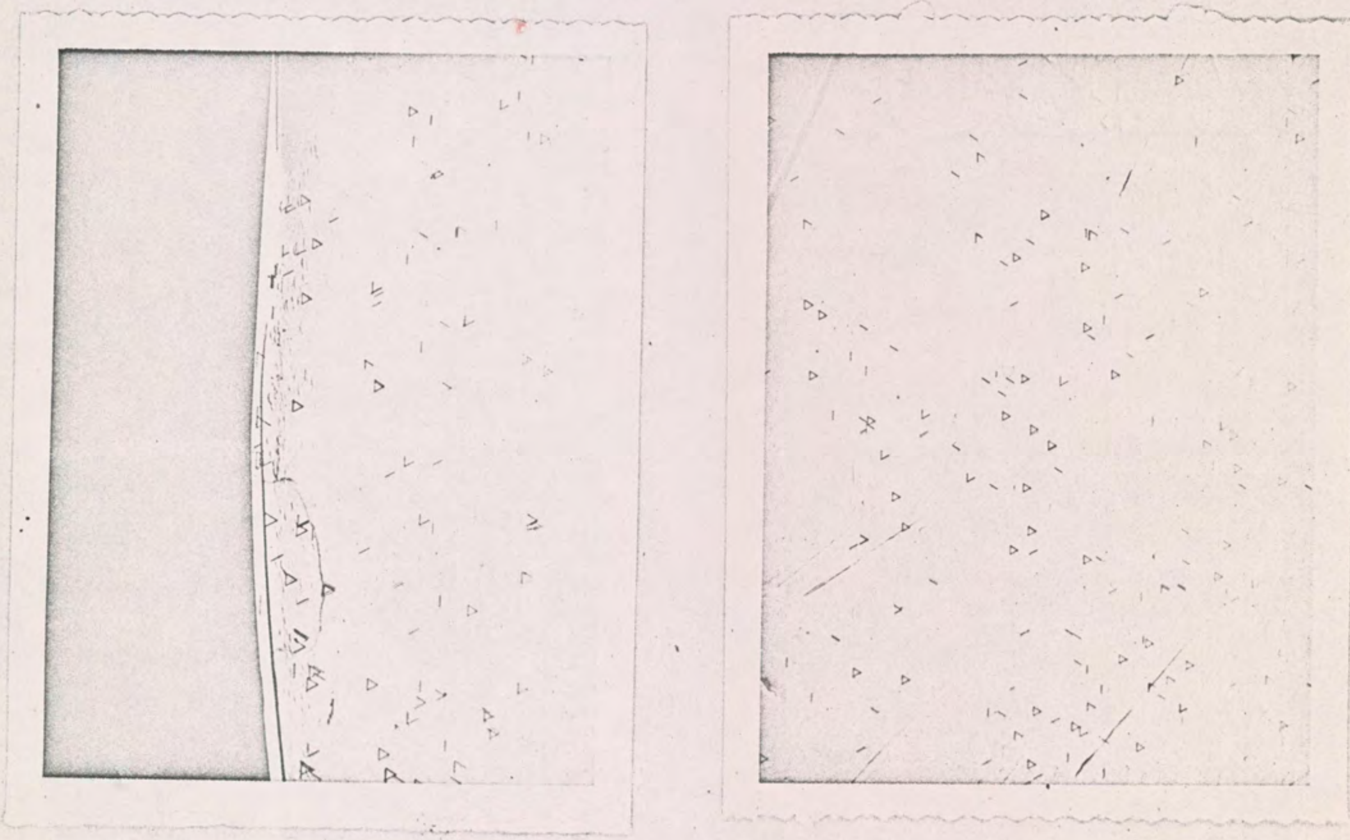


1 b). Substrate etched in dilute CP4 (HAc dilutant) to remove ~5 μ prior to epitaxy.



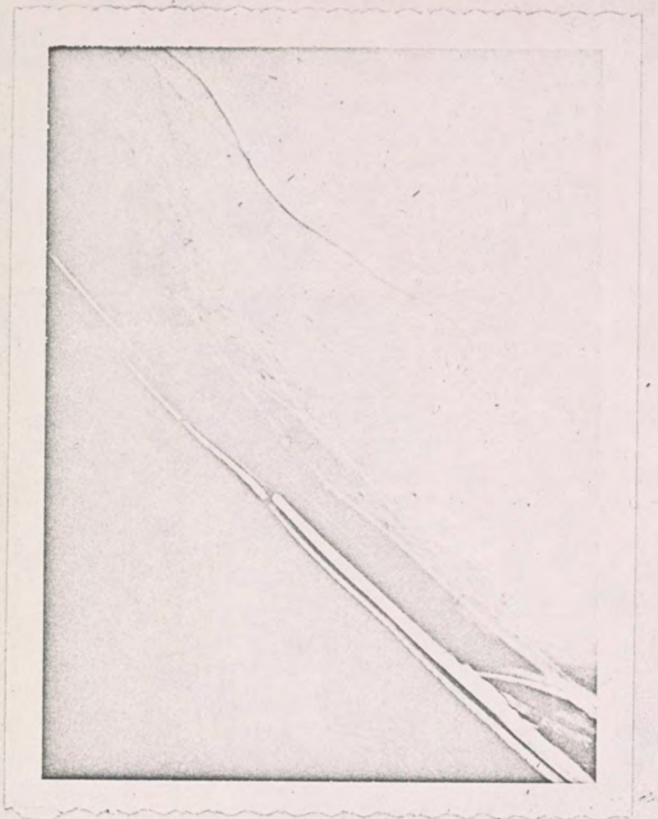
L7C

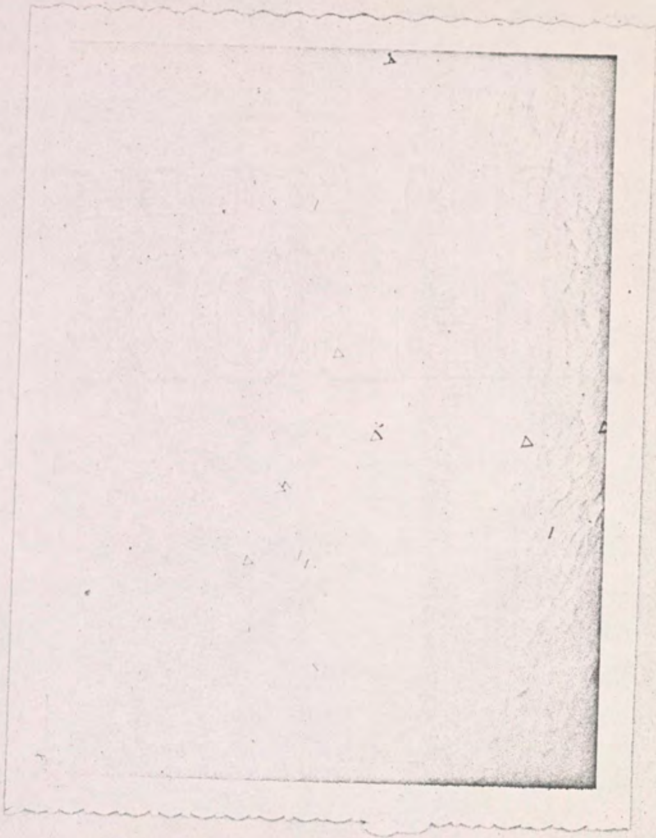
3 a) Control: mechanically polished substrate.



M4 W

3 b), Substrate etched to remove ~ 1 μ prior to epitaxy.





M4
1t

3 C) Substrate etched to remove ~ 20 μ prior to epitaxy.

7

4. Stacking faults grown over a smeared region on substrate.

April 24, Epidefects, con't

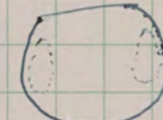
Tucker, con't

Doing defect analysis on 1000 rejects from our good run (42% die not yield)

3 A's (This is probably all the A's there were)
34 Craters
11 Shorted metal
10 Mesa and other overgrowth (~~?~~ Possibly statistical)
31 Stacking faults
42 No obvious epitaxial defects

Sometimes the O-etch removes defects like scratches (but not always)

Tucker ~~thinks~~ thinks there are inclusions in the substrates.

For a wafer in the reactor like so  — region of special smoothness and region most likely to get A's. It is also often thinner.

We have a reactor that has two positions that make A's in a particular pattern!!

Stacking Faults:

Mechanical polishing, especially not well polished, has lots.
A light chemical etch helps (say 5μ)
20 min of O rate vapor etch does not.

Probable cause: a) Localized strain at surface of substrate – not dislocations
b) Some means

Stacking faults do not necessarily ruin junctions, but areas of high density in general make poorer junctions.
The correlation is strong! Out of 84 junctions tested there were 10 bad ones and 6 stacking faults – 5 of the 10 bad ones contained 5 of the 6 stacking faults

 Epitaxial ~~[illegible]~~ defects, cont.

Dan Barry: – <u>Substrate preparation.</u>

Even the best mechanically polished surfaces have texture. Wigton thinks that this is bad for faceting when one grows.

<u>Yim:</u> (See written report)

FAIRCHILD SEMICONDUCTOR

Inter-Office Correspondence

RECEIVED
APR 19 1963
GORDON E. MOORE

To: See Distribution List April 18, 1963

From: P. Lamond

Subject: NPN Product Planning Meeting Agenda

The NPN Planar Section Product Planning Meeting will take place on April 24 at 4:00 pm in the Large Conference Room. The following items will be discussed for all devices listed:

1. Status of production - Product Manager
2. Discussion of Characteristics - Applications
3. Production Schedule, Present and Future Sales - Marketing

	PRODUCT	SPECIFIC PROBLEMS	
1.	0000/0001	Packaging of 0001	- P. Ferguson
2.	0002	Reliability	- Applications
3.	1312	New 2N Number	- Applications/Marketing
4.	0014	New 2N Number	- Applications/Marketing
5.	3011	Competitive Devices	- Applications/Marketing
6.	1221	Objective Specifications	- Applications/Marketing
7.	FET	Status	- P. Ferguson
8.	4011	Status	- P. Lamond
9.	4111	Objective Specifications	- Applications/Marketing
10.	4206	Objective Specifications	- Applications/Marketing
11.	4207	Objective Specifications	- Applications/Marketing
12.	New Devices 0017 - film driver		- P. Ferguson

Pierre R. Lamond

Pierre R. Lamond, Head
NPN Planar Section

Distribution List:

T. Bay
P. Ferguson
R. Graham
V. Grinich
B. Knudson
G. Moore
W. Richmond
R. Shultz
C. Sporck
D. Valentine
D. Yost

INTERNAL CORRESPONDENCE

FAIRCHILD SEMICONDUCTOR CORPORATION

COMPANY PRIVATE

TO: See Distribution

DATE: March 4, 1963

FROM: C. E. Sporck

CC:

SUBJECT: Results of NPN Large Geometry
Product Planning Meeting
February 26, 1963

No significant changes will be made in these instructions without the knowledge and agreement of the writers.

4011 - 16 - 4201 - Three split runs to be made by factory to compare these products. Data by 3/29/63.

Ferguson to look at present 4011 devices to explain poor low current beta performance.

Moore, Ferguson, Shultz, Graham and Grinich to decide upon definition of optimum family of devices by 3/29/63.

4111 - Units out by 3/8/63, there evaluation will determine any application.

4207 - 150 V LV_{CEO} (4205) 1 run/wk. Units to Applications by mid April. Volume requirements in last five months. Use TC package.

TB
T. Bay

GM
G. Moore

CES
C. Sporck

RECEIVED
MAR 6 - 1963
V. H. GRINICH

INTERNAL CORRESPONDENCE

FAIRCHILD SEMICONDUCTOR CORPORATION

COMPANY PRIVATE

TO: See Distribution

DATE: March 4, 1963

FROM: C. E. Sporck

CC:

SUBJECT: Results of Small Geometry Product Planning Meeting February 26, 1963

No significant changes shall be made in these instructions without the knowledge and agreement of the writers.

1312	-	Now a production product. Will not have 2N's written around this product at this time. When product is well established and in good inventory position, optimum 2N's will be written.
1311 1211	-	Production products. Have hot I_{CBO} problem. R & D will look at this problem in addition to the product group.
		The 1210 will be rescheduled for special requirements.
3111	-	Now running in production. This product will be announced at the IRE.
0002	-	35 mil die, gold bonds and TC package. Running 20 wafers out/week. Product should have sufficient life test data for announcement around end of March.
0000 0001	-	Working directly on 0000. Will have dice at die sort by 3/4/63. Will send die sorted dice to Hong Kong by 3/8/63.
		Some units will be assembled at Mountain View in TM packages.
		Volume will be 20 wafers out/week by 3/11/63.
		Product will be waiting for characterization by Applications.
		The 0001 will wait until 0000 is established.
FET	-	Under development at R & D.
1221	-	Marketing and Applications to decide by 3/11/63 what should be done with this product.
1450	-	Dropped - stop all work.
CDC Core Driver	-	R & D to make recommendation on possible device to fill this requirement.

RECEIVED
MAR 6 - 1963
V. H. GRINICH

COMPANY PRIVATE

TB
T. Bay

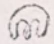
GM
G. Moore

CES
C. Sporck

Distribution

R. Cole
P. Ferguson
R. Fouquet
R. Graham
V. Grinich ✓
B. Knudson
P. Lamond
J. Magarian
B. O'Keefe
M. Oudewaal
W. Richmond
J. Sentous
R. Shultz
R. Smullen
D. Valentine
D. Yost

R&D DEVICE DESIGNATION

DEVICE NO.	FUNCTION	NPN/PNP	A_C	A_E	NO. BASES	NO. EMIT.	GEOM.	MIN. OXIDE CUT	LV_{ceo}			REMARKS
0000	RF AGC	NPN	10.8	1.50	3	2		.35	50			
0001	RF	NPN	10.8	1.50	3	2		.35	25			
0002	Power RF	NPN	88.00	12	12	8		.50	25			1.0 W at 500 mc aggregate
0003	Sat.Switch	NPN	2.45	.245	3	2		.35	6			< 2 nsec τ_s switch
0004	Sat.Switch	NPN	1.54	.28	1	1		.10	6			.1 mil test vehicle
0005	Sat.Switch	PNP			1	1		.50	70			Outside emitter Trident II
0006	Power RF	NPN	196	24	16	8		.50	25			2.5 W at 500 mc aggregate
0007	Power RF	NPN	350	47.5	10	5		.50	25			5.0 W at 500 mc aggregate
0008	Chopper	NPN		3.0	1	2			20			Dual transistor chopper
0009	Sat.Switch	PNP			1	2			25			Formerly FT-1701
0010	RF	NPN	10.8	1.50	3	2		.35	25			> 2 kmc f_T device
0011	RF	NPN							15			3 devices/chip
0012	Sat.Switch		7.88	2.25	1	1		.35	6			3 units per chip
0013	RF		6.1	.96	5	4		.2	20			Low noise RF device
0014	Sat.Switch		22.5	9.0	2	3		.35	12			CDC core driver
0015			25	4.5	4	2		.25	20			FT-1221 re-design
0016			21.3	4.5	3	2		.25	20			FT-1221 re-design
0017A	Sat.Switch		52.4	24	5	4		.5	12			Film driver
0017B	Sat.Switch		105	24	10	8		.35	12			Film driver

4/24/63 jpf

NPN Planar Product Planning 4/24/63

0000 20 wafers/ck to of 0000 — aiming at 100% yield.
For present — because of header supply — run only the entertainment version.
There are real test eq. problems.

0001 — Still needs pkg — we were expecting parts this week.
We have evaluated in hand-made pkgs. The supply of pkg from outside is not yet established. Est 1 mo. Uses 0000 mask, 1211 material

0002 — Masks made with emitter cuts need re-do.
TI material looks better on yield.

75% > 750 mw @ 500 Mc of the 50% good DC.

We will make some 0002's in strip line pkg.
Announce what we have.

1312 — No new 2N# for now.

0014 — CDC likes it ok.

3011 — 3 runs are at test 84
3 more right behind — Aim at 50v LVCEO.
Being made for star replacement

1221 — Run the single base region one.

FET — Our n-channel devices are still sick.
The P " " ones, for some reason, look ok — 1 run, U-1 structure.

4011 — Being run for 2N2297 (old 3001) commitment. P.L. thinks the masks might be no good. Also there are some problems on bonding.

4111 — By the next ~~meet~~ meeting we will define the device

~~Summary of Large Quantity~~

Reine will run split 4201–3011.

 4/25/63 – Epitaxial films

Roden:

Double grown tech. c̄ Ga –
1. There is a great deal of uncertainty in the measurements
2. The high temp bia distorts the profile considerably
3. Precision of meas depends upon having many fringes.

The capacitance measurements are not working well at all. On the surface barrier diode the agreement is non-existent.

→ It is necessary to get together with CTS re: where Roden's work is going.

Is there any selective ~~diffusion~~ transport into the film? (by the predep of interface tech.)

There is no apparent vapor transport of B or Ga into growing films.

Wigton:

Plot of ml/min vs μ/ml being a straight line is a 1st order deposition reaction.

$$\text{Rate of deposition} = k\left(y - \frac{x^2}{0.72}\right)$$

The deposition is controlled by

$$H_2 + SiCl_2 \rightleftharpoons 2HCl + Si \qquad (K = 0.72 \text{ at } 1550\,°K;\ 0.74 \text{ @ } 1600\,°K;\ 0.68 \text{ @ } 1500\,°K)$$

~~One has a rapidly equilibrium~~
~~$SiHCl_3 + H_2 \rightleftharpoons 3HCl + Si$~~

The rate limiting step is

$$SiHCl_3 \longrightarrow SiCl_2 + HCl$$

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HCl ETCHING STUDIES

H. Wigton

PROJECT 128 - SILICON EPITAXIAL FILM

For deposition with no HCl added, the best equation is

$$r_D = \left(\frac{1 - 0.347 \ln \left[\frac{yo}{.0027} \right]}{.004} \right) y_o \qquad (1)$$

in which

r_D = deposition rate in microns/minute

y_o = partial pressure of $SiHCl_3$ in the entering H_2 in atmospheres

Etching with HCl and H_2 only is best expressed by the relationship

$$r_E = 0.438 \times 10^3 \left(\frac{x_A^2}{0.36 + 2x_A} \right) \qquad (2)$$

in which

r_E = etching rate in microns/minute

x_A = partial pressure of HCl in the entering H_2 gas in atmospheres

The reaction when both HCl and $SiHCl_3$ are added appears to be kinetically limited by the conversion of $SiHCl_3$ to $SiCl_2$ and equilibirum (3)
limited by the reaction $SiCl_2 + H_2 \rightleftarrows Si + 2HCl$ (4)

The forward reaction is stopped by the addition of HCl sufficient to balance the activities in equation (4) if approximately 15% of the initial $SiHCl_3$ is assumed converted to $SiCl_2$. This is several orders of magnitude less HCl than would be required to stop the overall reaction.

att #2

When both $SiHCl_3$ and HCl <u>or</u> both $SiCl_4$ and HCl are added, the rate is controlled by the relationship

$$r = k\left(y - \frac{x^2}{K}\right)$$

r = deposition or etch rate in microns/min.

$k = 1.15 \times 10^3$ = diffusion or reaction constant

y = partial pressure of $SiCl_2$ in the gas film in atmospheres

$\frac{x^2}{K}$ represents p^*SiCl_2, the equilibrium activity (concentration) of $SiCl_2$ on the surface

x = partial pressure of HCl (atmospheres)

= pHCl added + $y_0(3c_3 + c_1)$ for $SiHCl_3$

= " + $y_0(4c_4 + c_2 + c_1)$ " $SiCl_4$

y_0 = partial pressure of $SiCl_4$ or $SiHCl_3$ entering in atmospheres

$$y = c_1 y_{avg.} = c_1 y_0 (1 - c_3)\left(\frac{2 - c_1}{2}\right) \text{ for } SiHCl_3$$

c_1 = reaction constant mols $SiCl_2$/mol $SiHCl_3$

$c_1 = 0.28 - 0.30$

c_4 or c_3 = mols Si deposited/mol Si entering

$$y = (c_1)(c_2)(1 - c_4)\left(\frac{2 - c_1}{2}\right) y_0 \text{ for } SiCl_4$$

c_2 = reaction constant mols $SiHCl_3$/mol $SiCl_4$

$c_2 = 0.9$

$$c_3 \text{ or } c_4 = r \times \frac{1.12 \times 10^{-3}}{y_0} = \frac{r \times 320 \times 10^{-4} \times 2.45}{y_0 \times 2.5 \times 28}$$

area; Si density; mol wt; 2.5 moles/min going in

To avoid trial + error, the following rearrangment can be used for $SiCl_4$

$$r = 1.15 \times 10^3 \left[\frac{0.195 y_0 - x(x + 2.4 y_0)}{1.65 + 1.15 \times 10^3 (10.7 y_0 + .2 r 10^4 + 9(x) 10^{-3})}\right]$$

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K.W. 3

Sample Calculation

$SiCl_4$ deposition run zero HCl added

Basis 1 minute: 2.5 mols H_2 added 0.87 ml./min $SiCl_4$

$r = 0.63\ \mu$ Si deposited Mols $SiCl_4 = \frac{0.87 \times 1.5}{170} = 7.7 \times 10^{-3}$ (1.5 = density; 170 = Mol Wt)

$y_0 = \frac{7.7}{2.5} = 3.1 \times 10^{-3}$ $c_4 = \frac{r_D \times 2.8 \times 10^{-3}}{y_0 \times 2.5} = 0.225$

$r = 0.63 = 10^{-3}k_1\left(y \times 10^3 - \frac{x^2}{.72} \times 10^3\right) = 10^{-3}k\left(.3 \times .775\left(\frac{2-.3}{2}\right) \times 3.1 - .06\right)$

$y = y_0(1-c_4)(c_2)(c_1)\left(\frac{2-c}{2}\right)$ Assume $c_2 = 0.9$

$v = 4y_0c_4 + y_0c_2 + y_0c_1 = y_0(.9 + .9 + .3) = 2.1\,y_0$

$\frac{x^2}{.72} = \frac{4.2}{.72} \times 10^{-5} = 0.06 \times 10^{-3}$

$10^{-3}k = \frac{0.63}{.155} = 1.15 \therefore c_2 = 0.9$ as assumed

$SiCl_4$ "zero" point (no etch or deposit)

$x_{added} = \sqrt{3.25 \times 10^{-4}} = 1.8 \times 10^{-2}$ (from curve)

$y = y_0(1-c_4)(c_2)(c_1)\frac{(2-c_1)}{2} = 10^{-3}(3.1)(1)(.9)(.3)(.85)$

$= 0.70 \times 10^{-3}$

$\Delta x = y_0(1 + .3) = 10^{-3}(3.1)(1.3) = 0.405 \times 10^{-2}$

$\frac{x^2}{.72} = \frac{2.25^2 \times 10^{-4}}{.72} = .647 \times 10^{-3} \neq 0.70 \times 10^{-3}$

Close enough

HCl Corrected $SiHCl_3$ etch Data N.N.

H_2 flow 100% 1/4" meter glass ball 2.5 g mol/min
10 psig

HCl flow on 1/8" meter w SS ball temp = 1170° optical
24 psig

HCl, H_2 only

r	HCl Meter	ml HCl/min	x_A p_{HCl}	y_0 p_{SiHCl_3}	$X^2(10^4)$
−0.14 avg. 5.	20%	510	0.89×10^{-2}	—	0.79
−0.34 avg 4	55		1.67×10^{-2}	—	2.79
−0.66, −.70	100		2.62×10^{-2}	—	6.85
−0.33	55		1.67×10^{-2}	—	2.79
−.45, −.45 *	55 *		Different temp		
−1.43	~165				14.

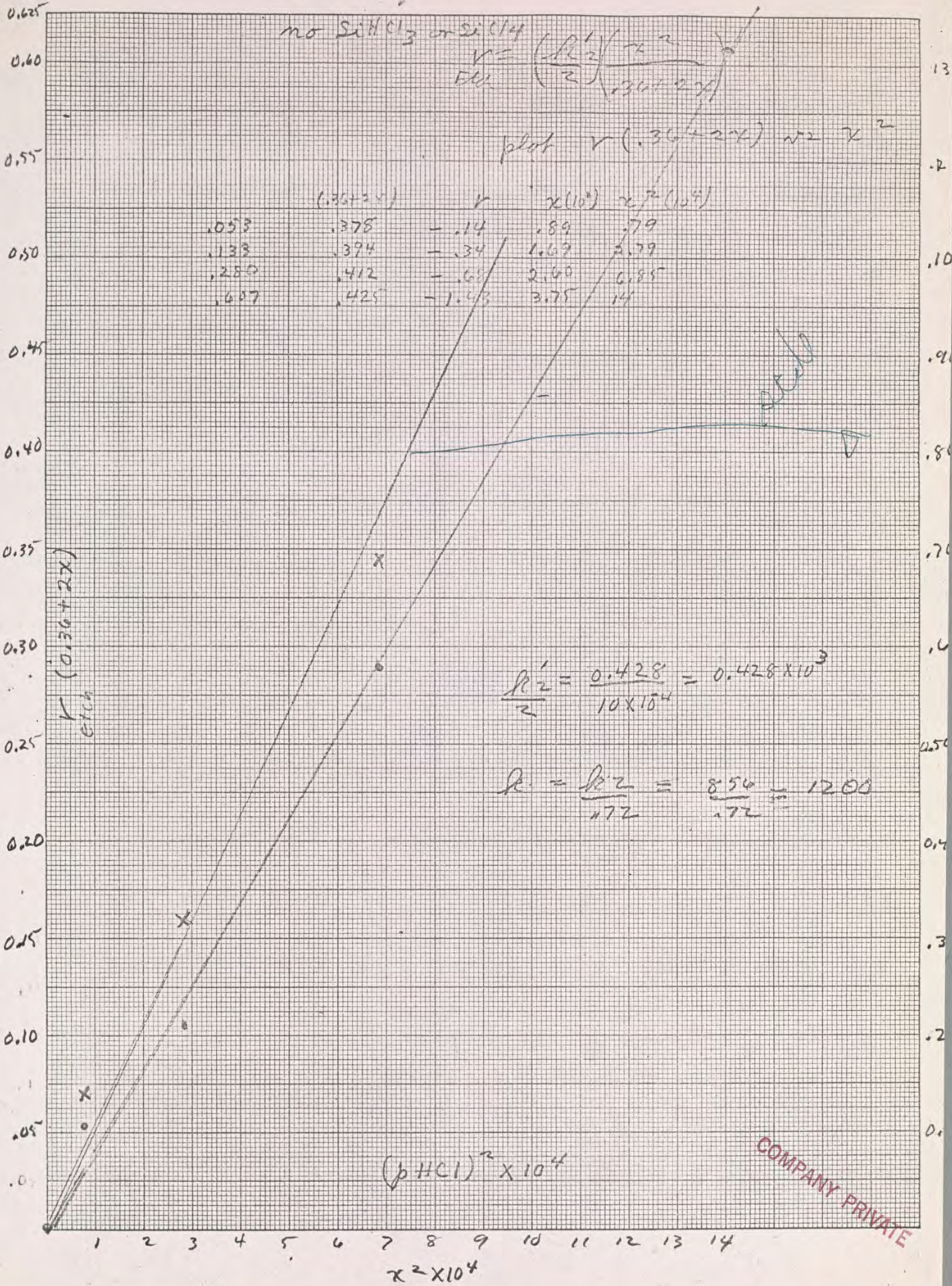
0.50 ml/min $SiHCl_3$ $2\times10^{-3} = y_0$

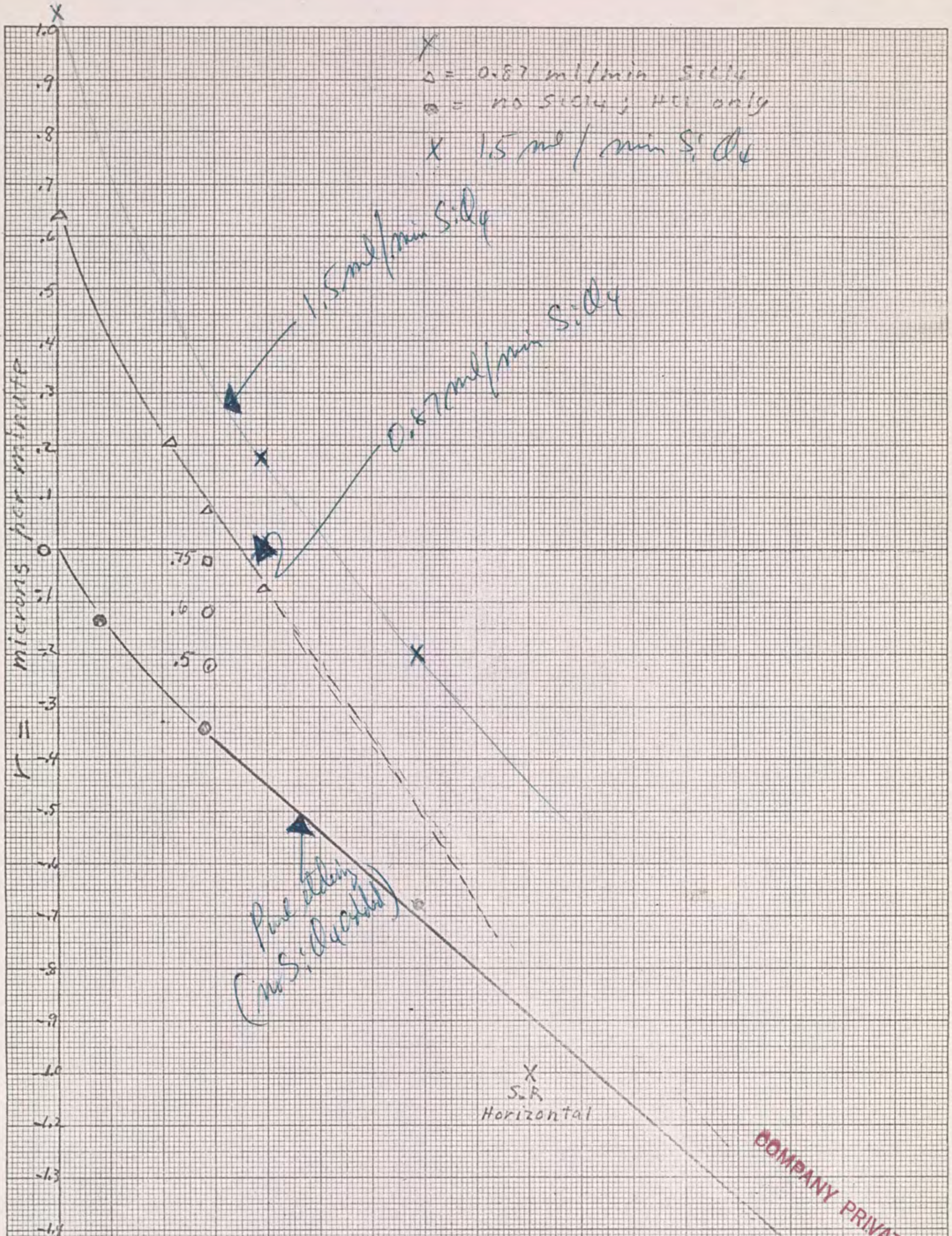
r	HCl Meter	x_A	$X^2(10^4)$
+0.16	~ 44%	1.43×10^{-2}	2.05
+0.035	55	1.67×10^{-2}	2.79
+0.02	62	1.82	3.30
−0.44	~100	2.62	6.85
−0.6, −.72	~107.5	2.78	7.75
+.06, 0	~65	1.87	3.5
−1.57, −1.2	~165	3.75	14

1.0 ml/min $SiHCl_3$ $4\times10^{-3} = y_0$

r	HCl Meter	x_A	$X^2(10^4)$
+.70, +.59	45	1.44×10^{-2}	2.08
+.64	52	1.59	2.54
−.42, −0.33	100	2.62×10^{-2}	6.85
+.09, +0.13	80	2.20×10^{-2}	4.83
−1.23, −1.34	~165	3.75	14

Evaluation of k_2





△ = 0.87 ml/min SiCl4
● = no SiCl4; HCl only
X 1.5 ml/min SiCl4
1.5 ml/min SiCl4
0.87 ml/min SiCl4
.75
.60
.5
Pure etching (no SiCl4 added)
r = microns per minute
(p HCl)² X 10⁴
Horizontal
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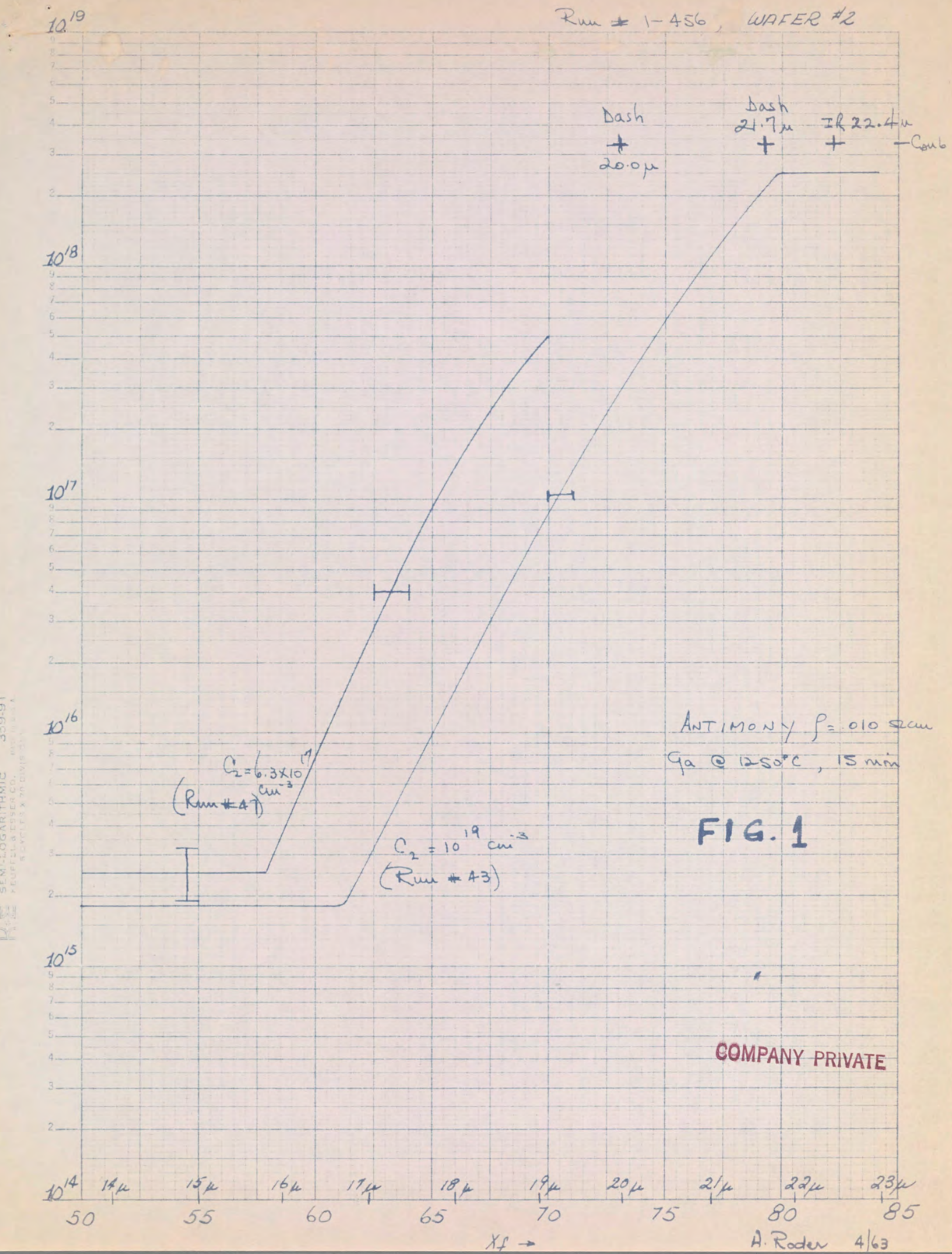

FIG. 1

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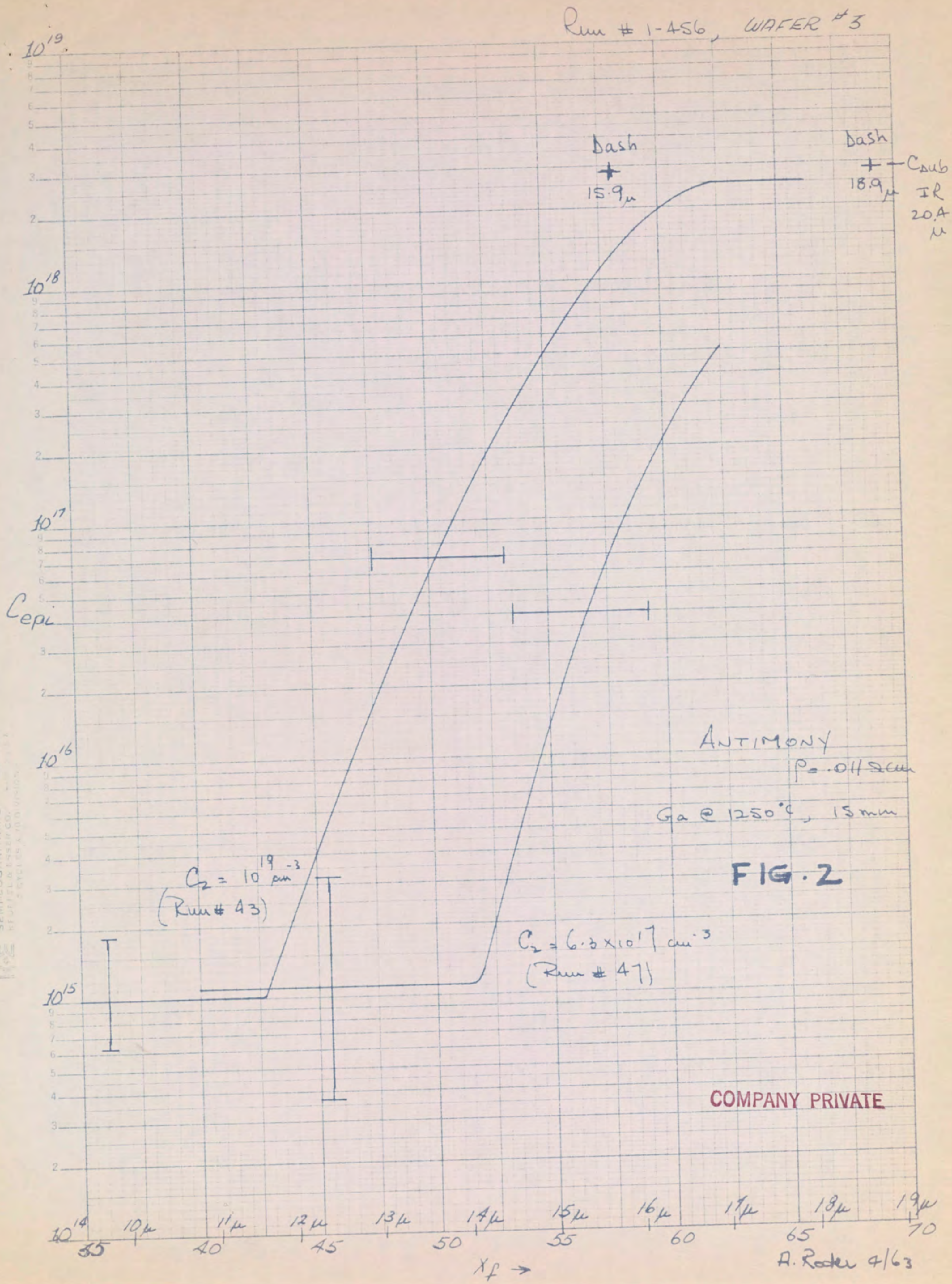
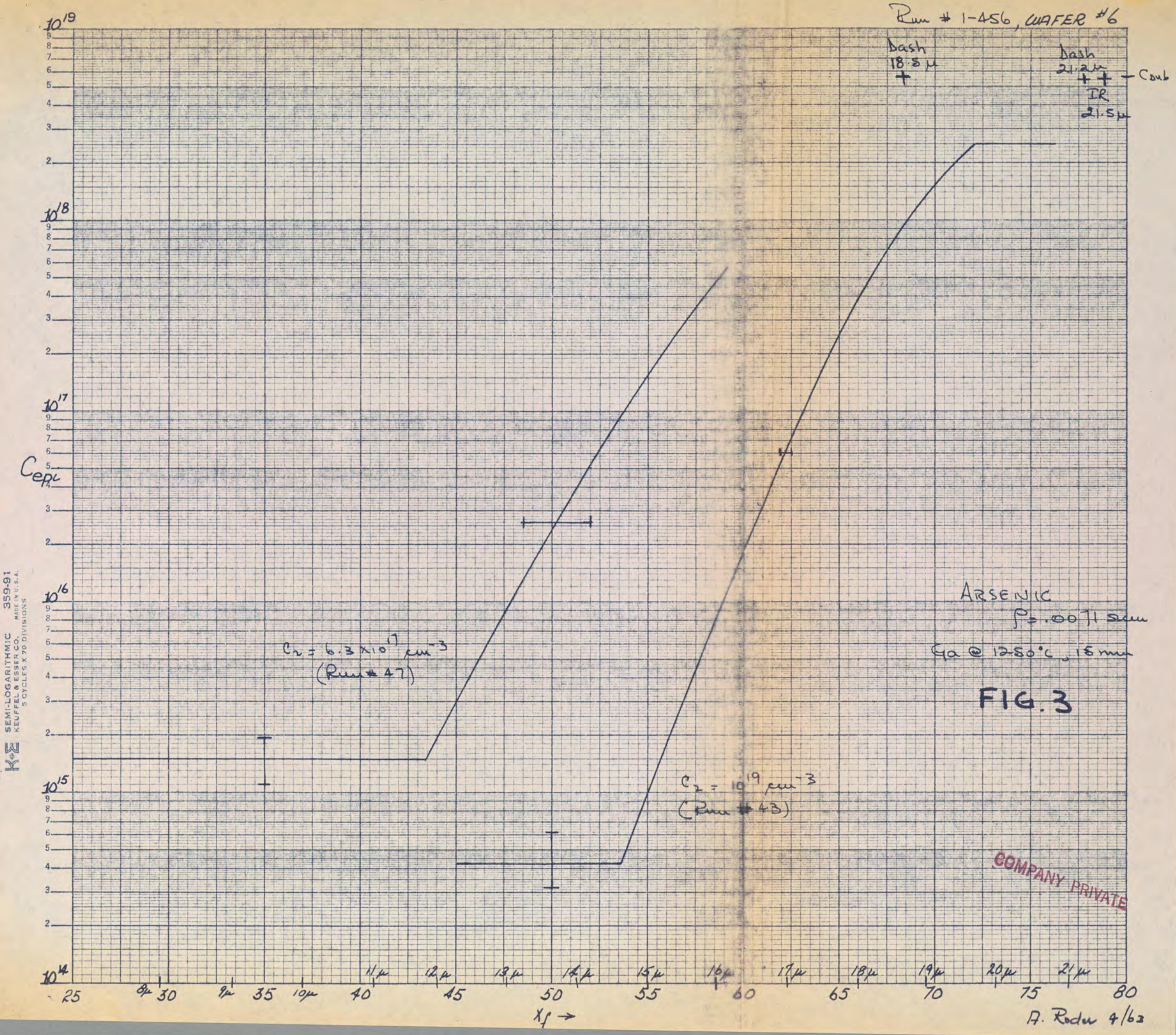
A. Roder 4/63



Run # 1-456, WAFER #3
10^19
10^18
10^17
10^16
10^15
10^14
Cepi
Dash
15.9μ
Dash
18.9μ
Csub
IR
20.4 μ
ANTIMONY
ρ = .011 Ωcm
Ga @ 1250°C, 15 min
C2 = 10^19 cm^-3
(Run # 43)
C2 = 6.3 x 10^17 cm^-3
(Run # 47)
10μ
11μ
12μ
13μ
14μ
15μ
16μ
17μ
18μ
19μ
35
40
45
50
55
60
65
70
Xf →
A. Rodder 4/63

FIG. 2



Run # 1-456, WAFER #6
Dash 18.5 μ
Dash 21.2 μ
– Csub
IR 21.5 μ
C_{epi}
$C_2 = 6.3 \times 10^{17}$ cm^{-3} (Run # 47)
$C_2 = 10^{19}$ cm^{-3} (Run # 43)
ARSENIC
ρ = .0071 Ωcm
Ga @ 1250°C, 15 min
COMPANY PRIVATE
x_j →
A. Roder 4/63
SEMI-LOGARITHMIC 359-91
KEUFFEL & ESSER CO. MADE IN U.S.A.
5 CYCLES X 70 DIVISIONS

FIG. 3

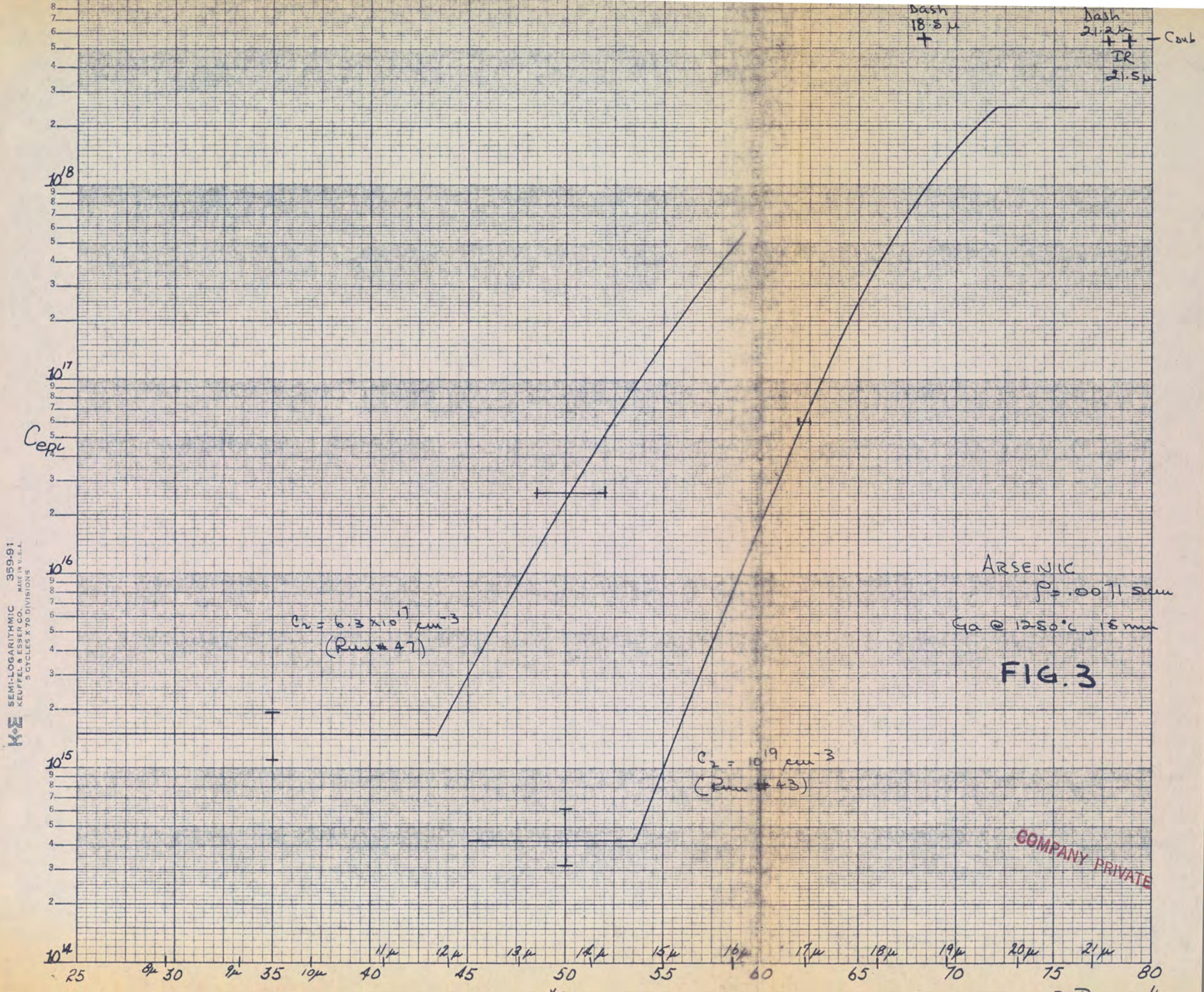


FIG. 3

A. Roder 4/63

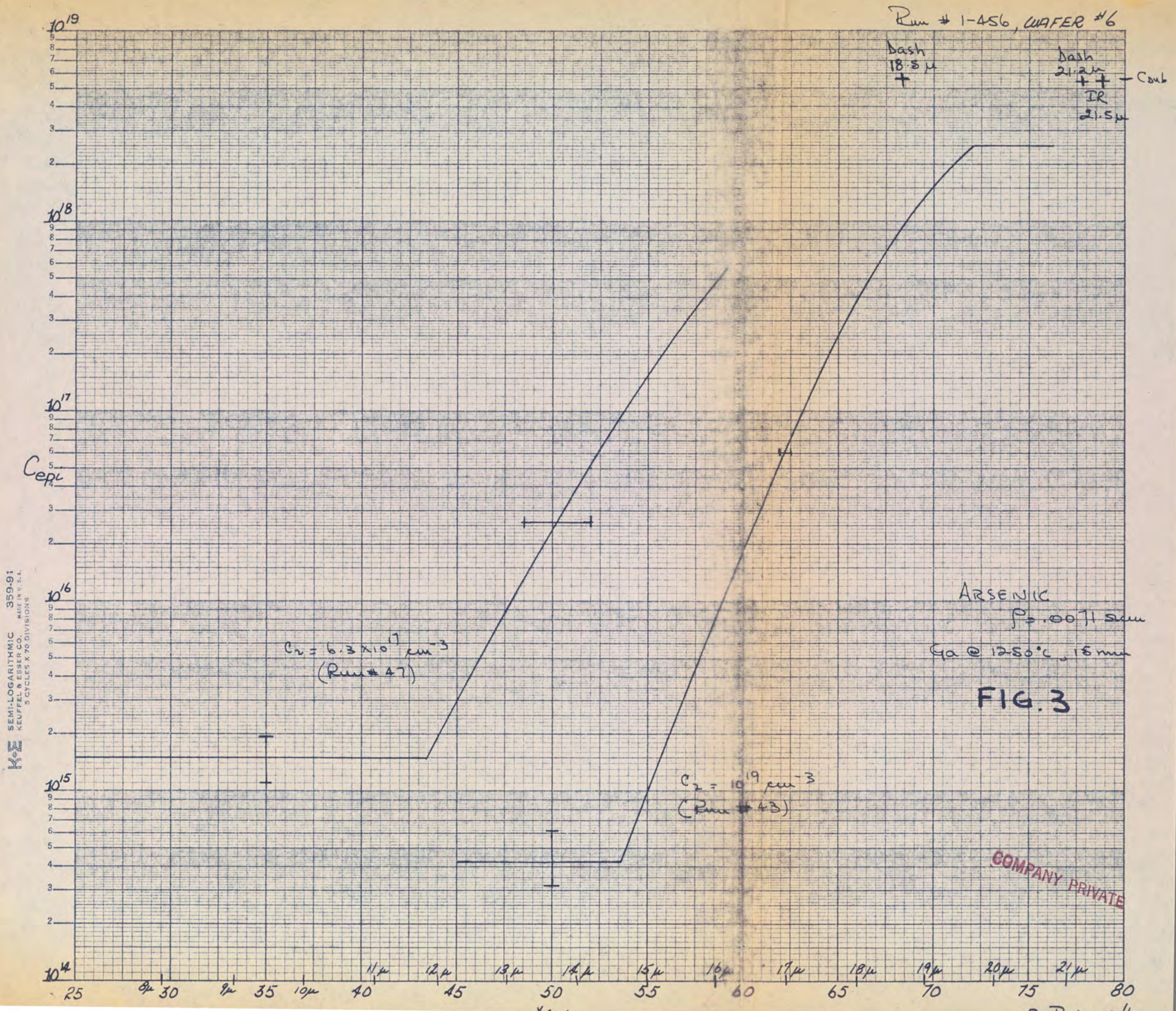
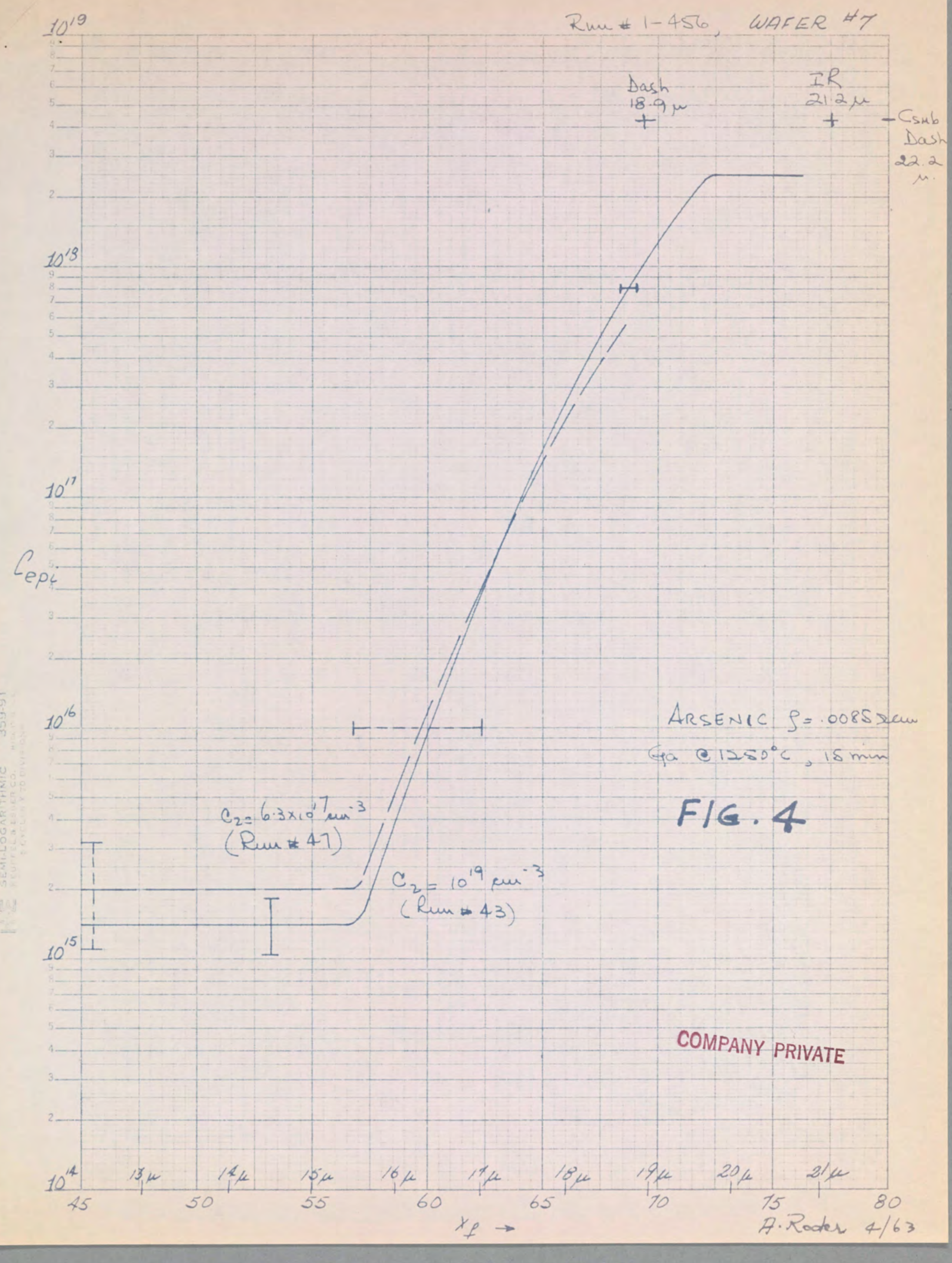

Run # 1-456, WAFER #6
Dash
18.5 μ
Dash
21.2μ
Csub
IR
21.5μ
C_{epi}
C_2 = 6.3 x 10¹⁷ cm⁻³
(Run # 47)
C_2 = 10¹⁹ cm⁻³
(Run # 43)
ARSENIC
ρ = .0071 Ωcm
Ga @ 1250°C, 15 min
COMPANY PRIVATE
K+E SEMI-LOGARITHMIC 359-91
KEUFFEL & ESSER CO. MADE IN U.S.A.
5 CYCLES X 70 DIVISIONS

FIG. 3



Run # 1-456, WAFER #7
Dash 18.9μ
IR 21.2μ
Csub Dash 22.2 μ.
10^{19}
10^{18}
10^{17}
10^{16}
10^{15}
10^{14}
C_{epi}
ARSENIC ρ = .0085 Ωcm
Ga @ 1250°C, 15 min
$C_2 = 6.3 \times 10^{17}\ cm^{-3}$ (Run # 47)
$C_2 = 10^{19}\ cm^{-3}$ (Run # 43)
13μ 14μ 15μ 16μ 17μ 18μ 19μ 20μ 21μ
45 50 55 60 65 70 75 80
x_j →
A. Roder 4/63
COMPANY PRIVATE
SEMI-LOGARITHMIC 359-91

FIG. 4

RUN # 49
WAFER # 4'

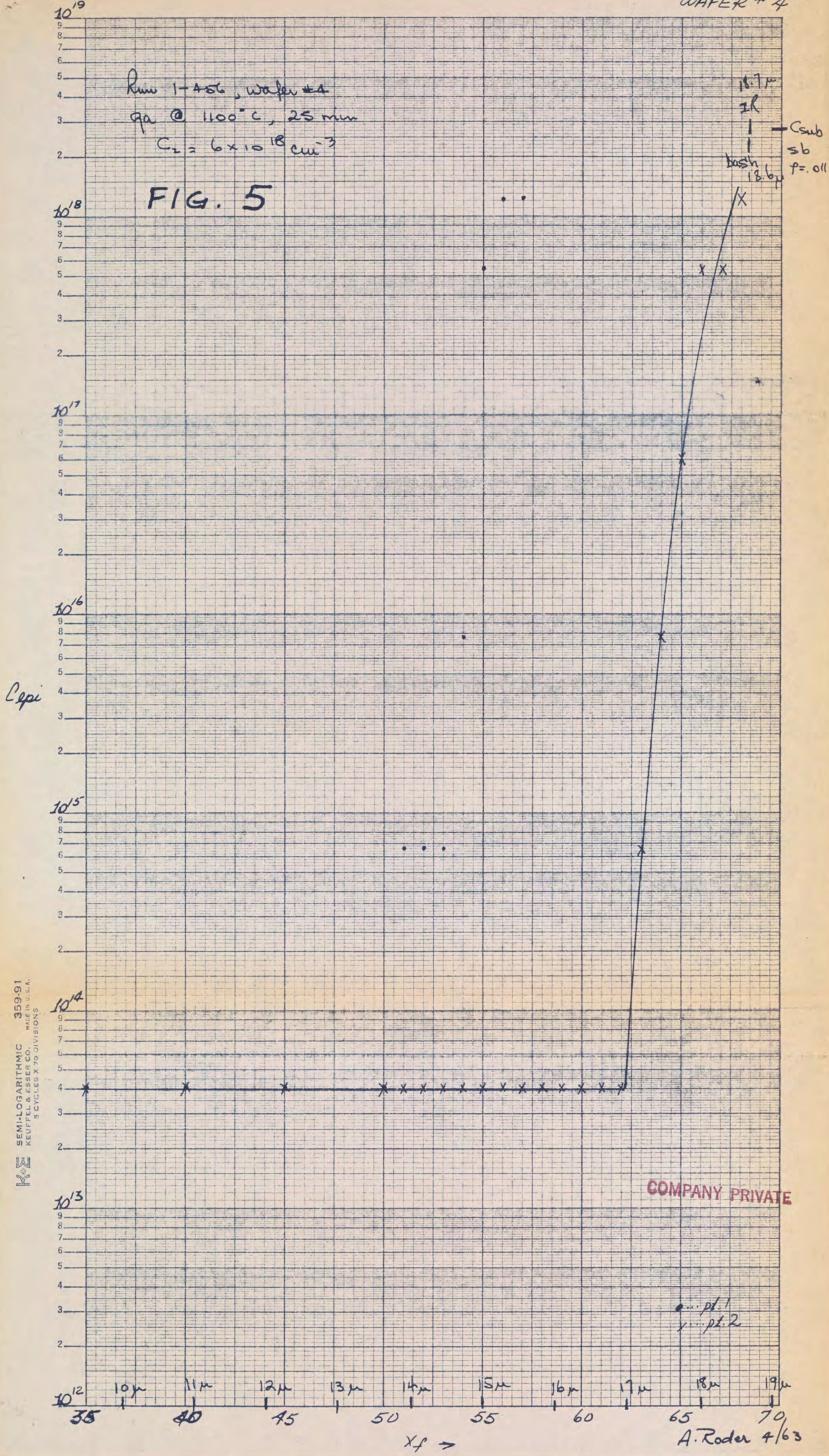
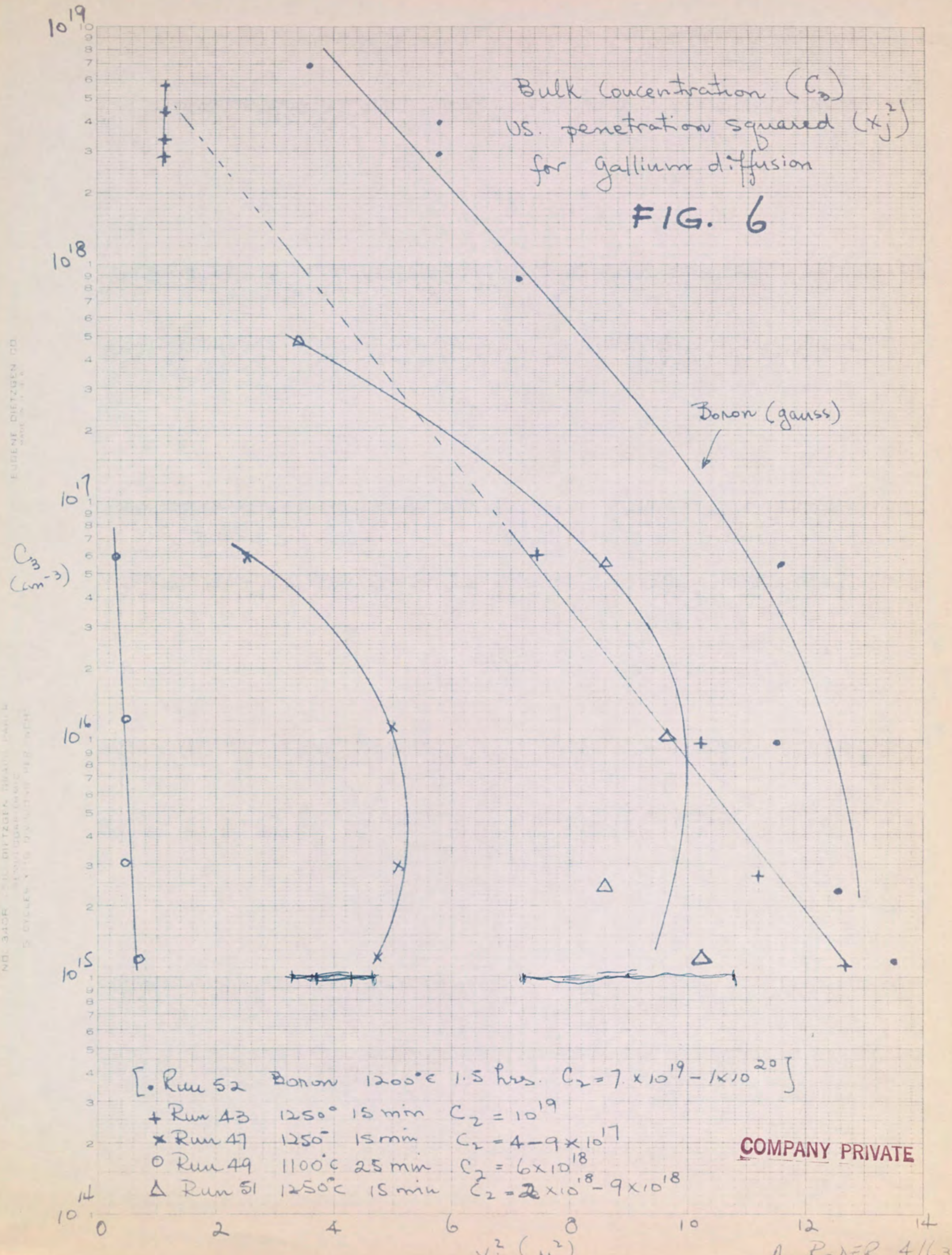


FIG. 5

COMPANY PRIVATE

A. Roder 4/63


Bulk concentration (C_3) vs. penetration squared (x_j^2) for Gallium diffusion
FIG. 6
Boron (gauss)
C_3 (cm^{-3})
x_j^2 (μ^2)
[• Run 52 Boron 1200°C 1.5 hrs. $C_2 = 7 \times 10^{19} - 1 \times 10^{20}$]
+ Run 43 1250° 15 min $C_2 = 10^{19}$
✶ Run 47 1250° 15 min $C_2 = 4-9 \times 10^{17}$
○ Run 49 1100°C 25 min $C_2 = 6 \times 10^{18}$
△ Run 51 1250°C 15 min $C_2 = 2 \times 10^{18} - 9 \times 10^{18}$

A. RODER 4/63

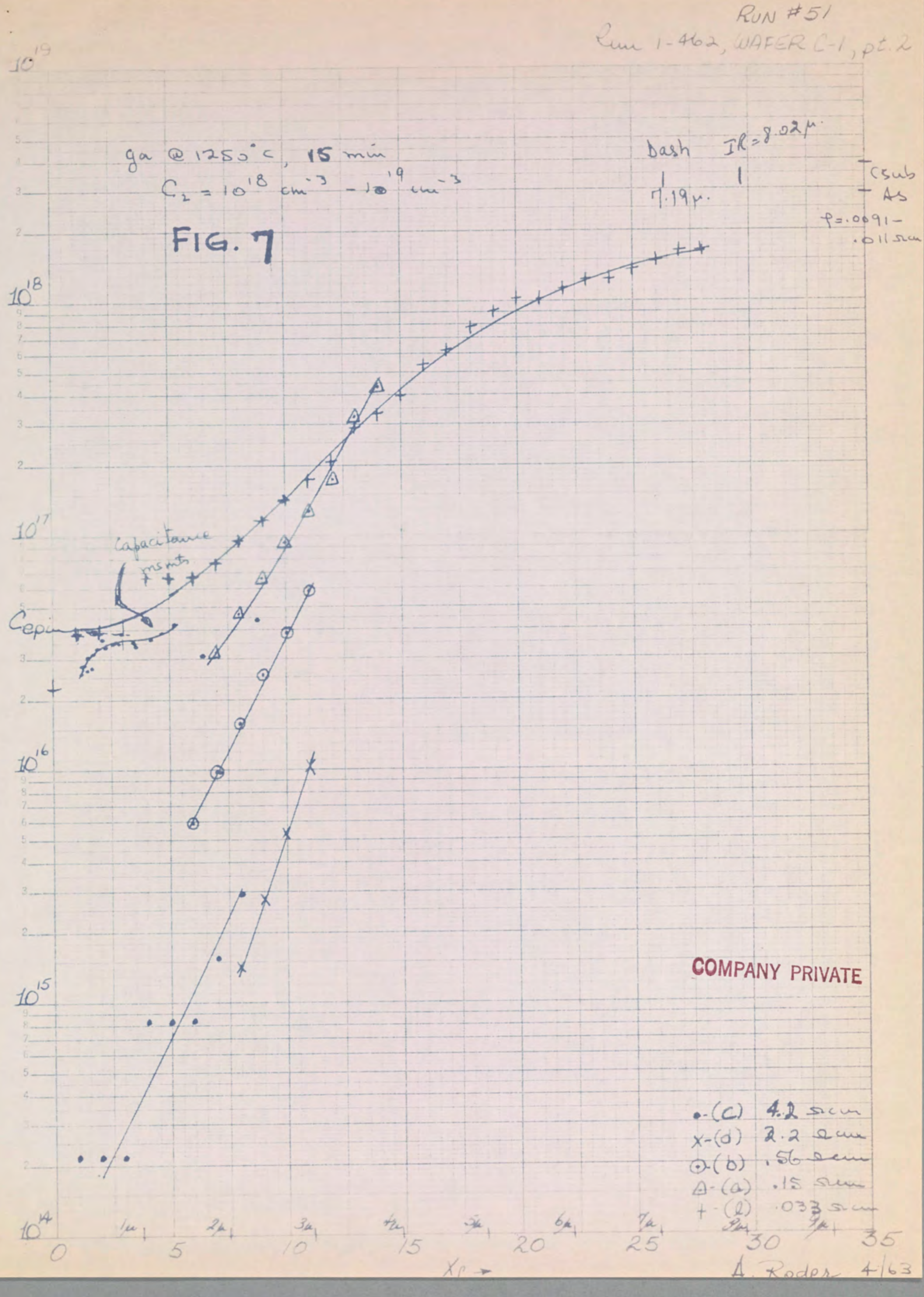
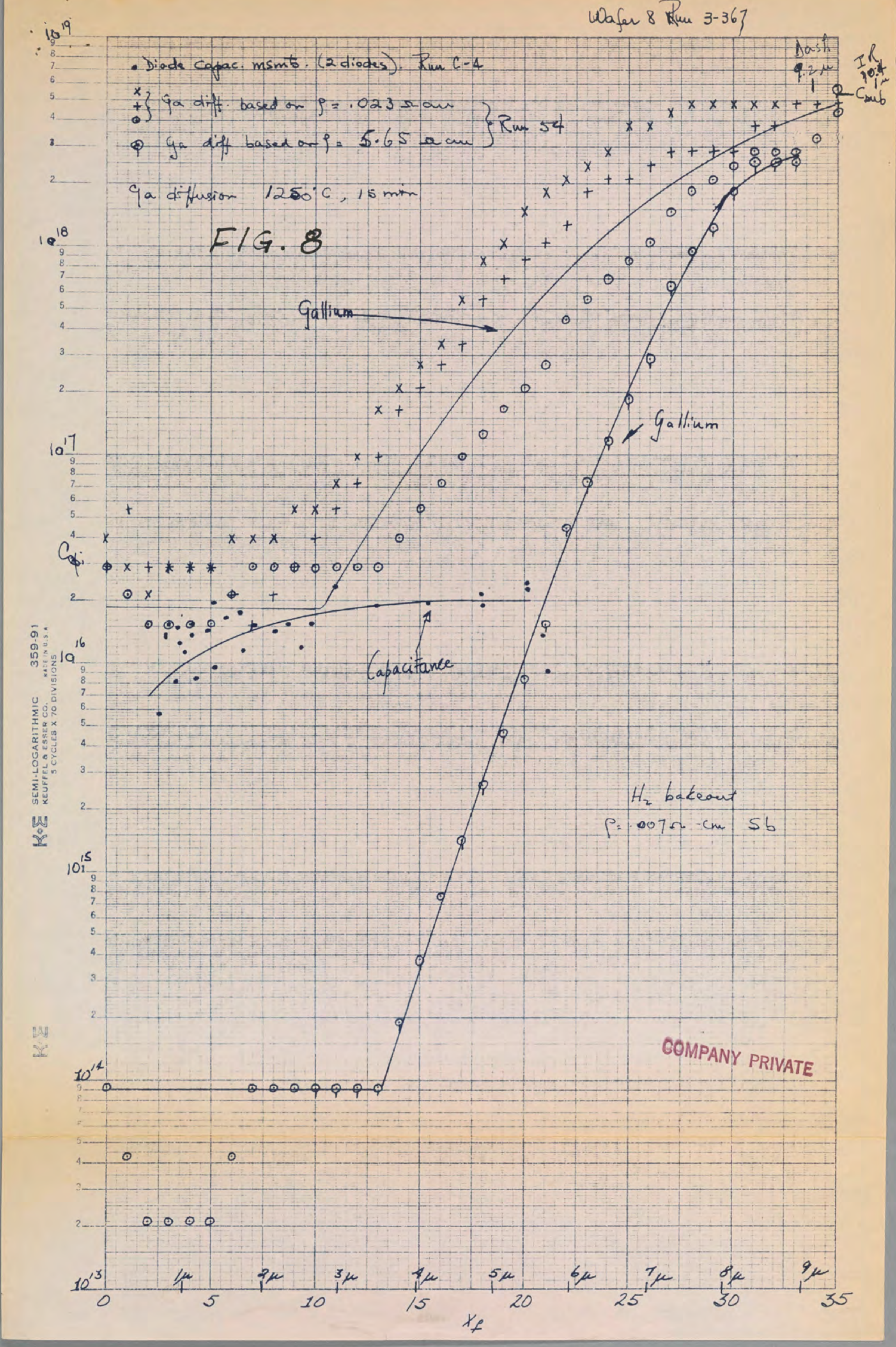

RUN #51
Run 1-462, WAFER C-1, pt. 2
Ga @ 1250°C, 15 min
$C_2 = 10^{18}$ cm^{-3} – 10^{19} cm^{-3}
Dash
7.19μ.
IR = 8.02μ.
Csub
As
ρ = .0091 – .011 Ωcm
Capacitance msmts
Cepi
COMPANY PRIVATE
•-(C) 4.2 Ωcm
x-(d) 2.2 Ωcm
⊙-(b) .56 Ωcm
△-(a) .15 Ωcm
+-(l) .033 Ωcm
10^{19}
10^{18}
10^{17}
10^{16}
10^{15}
10^{14}
0 5 10 15 20 25 30 35
1μ 2μ 3μ 4μ 5μ 6μ 7μ 8μ 9μ
X_P →
A. Roder 4/63

FIG. 7



Wafer 8 Run 3-367
• Diode capac. msmts. (2 diodes). Run C-4
×, + } Ga diff. based on ρ = .023 Ω cm
⊙ Ga diff. based on ρ = 5.65 Ω cm
} Run 54
Ga diffusion 1250°C, 15 min
FIG. 8
Gallium
Gallium
Capacitance
C_{0i}
Dash 9.2 μ
IR 10.4 μ
1 μ
Csub
H_2 bakeout
ρ = .007 Ω-cm Sb
COMPANY PRIVATE
1μ 2μ 3μ 4μ 5μ 6μ 7μ 8μ 9μ
0 5 10 15 20 25 30 35
x_f
10^{13} 10^{14} 10^{15} 10^{16} 10^{17} 10^{18} 10^{19}
K+E SEMI-LOGARITHMIC 359-91
KEUFFEL & ESSER CO. MADE IN U.S.A.
5 CYCLES X 70 DIVISIONS

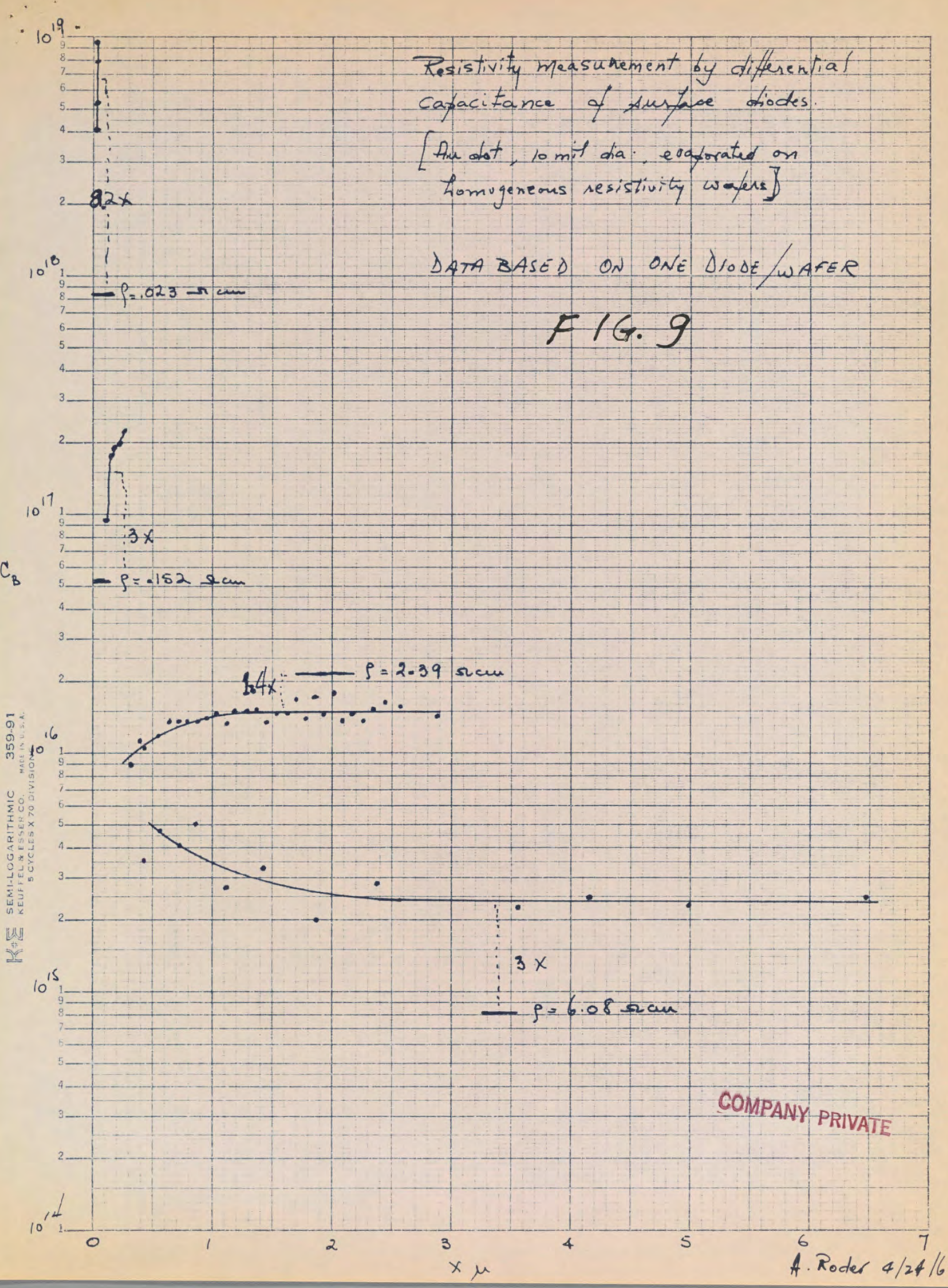


FIG. 9

A. Roder 4/24/63

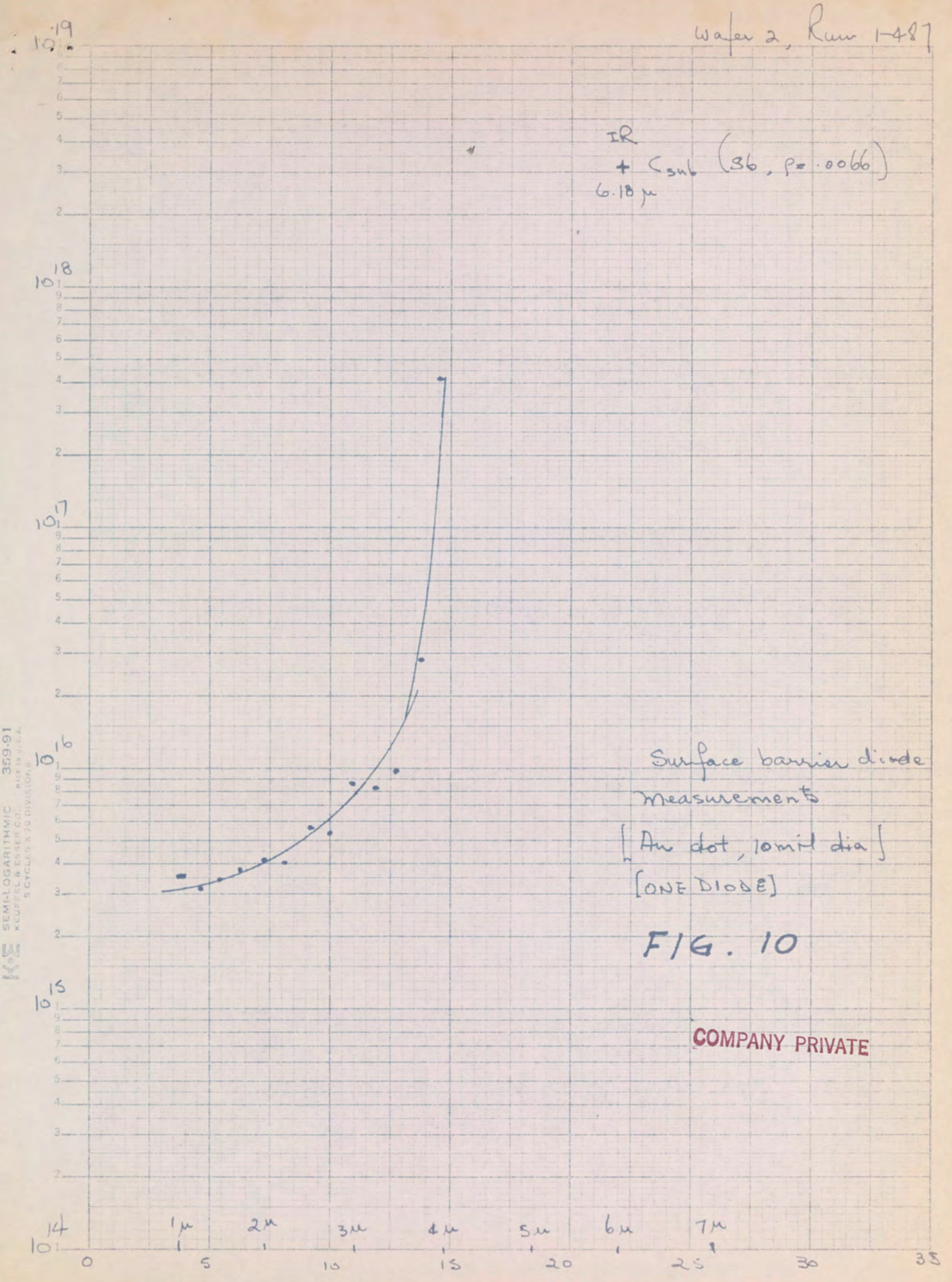

Wafer 2, Run 1-487
IR
+ Csub (Sb, ρ= .0066)
6.18 μ
Surface barrier diode
measurements
[Au dot, 10 mil dia]
[ONE DIODE]
10^19
10^18
10^17
10^16
10^15
10^14
1μ
2μ
3μ
4μ
5μ
6μ
7μ
0
5
10
15
20
25
30
35
K&E SEMI-LOGARITHMIC 359-91
KEUFFEL & ESSER CO.
5 CYCLES X 70 DIVISIONS

FIG. 10

F/11-4/24

$(4,3)^2 = 16 + .6 \times 4$
$= (2.4\mu^2)$

FAIRCHILD SEMICONDUCTOR

RESEARCH & DEVELOPMENT LABORATORY

TO: List

DATE: April 18, 1963

FROM: C. T. Sah

CC: → G. E. Moore
V. H. Grinich

SUBJECT: Agenda for Project Review Meeting
Thursday, April 25, 1963 - 8:30 A.M. to 10:55 A.M.
Impurity Diffusion & Growth Kinetics of Silicon Epitaxial Film Growth
Project 128

The purpose of the meeting is to review the data of impurity profile in epitaxial films and to review the data and model of etching and growth rate of films.

AGENDA:

8:30 Presentation of experimental data of impurity profile for various growth and etching conditions with the various profiling techniques.
(Roder)

9:30 Summary of etching and growth rate data and outline of an analysis of the data and the model employed.
(Wigton)

10:55 Meeting adjourned

Please have all data summarized and important data and photographs reproduced each for 10 copies for efficient presentation.

C T Sah

C. T. Sah
Solid State Physics Section

CTS:jt

List: (Participants)

A. Roder
H. Wigton
R. Tucker
D. Barry
C. Bittmann X
A. Davis
J. Gordon
A. Grove
W. Shepherd
E. Yim
Ferguson

$$C = K \frac{1}{(V+V_0)^{\frac{1}{2}}}$$

$$\frac{dC}{dV} = -\frac{1}{2} K \frac{1}{(V+V_0)^{\frac{3}{2}}} \quad \text{as } V >> V_0, \; \frac{dC}{dV} \rightarrow \frac{k}{V^{\frac{3}{2}}}$$

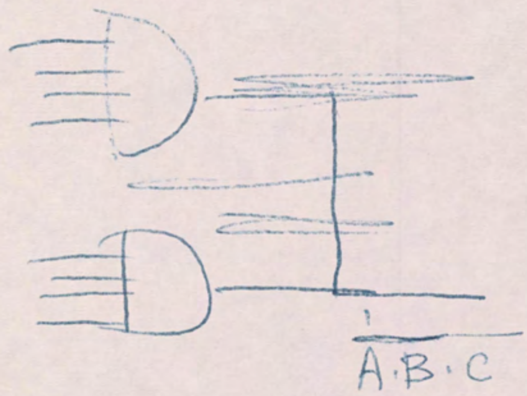
COMPANY PRIVATE

1962 EXEMPT TERMINATIONS

	Terminated	Rating: Outstand'g	Good	Average	Marg.	Poor	Reason: Resig.	Forced	Discharged
Department 11-	5		2	2	1		1	3	1
15-	4		1		2	1	3		1
20-	17		4	8	3	2	11	4	2
36-	3			1	1	1	2		1
30-	12		5	4	3		10	2	
40-	30	4	11	8	4	3	23	5	2
50-	3		1	1	1		2	1	
70-	7		4	2	1		*	*	*
80-	18	1	4	5	8		10	8	
TOTAL	99	5	32	31	24	7			

Note * --Department was unable or unwilling to complete last column.

Prepared April 15, 1963
by C.D. Campbell


$\overline{A \cdot B \cdot C}$

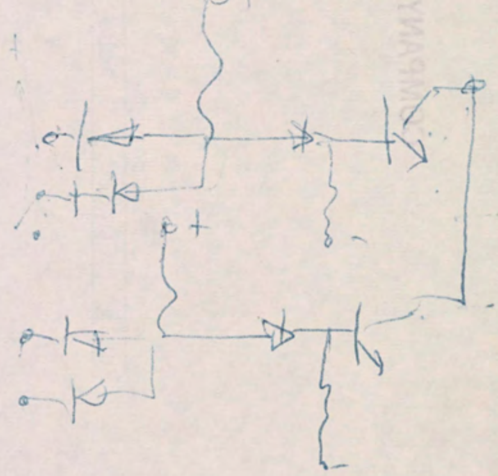
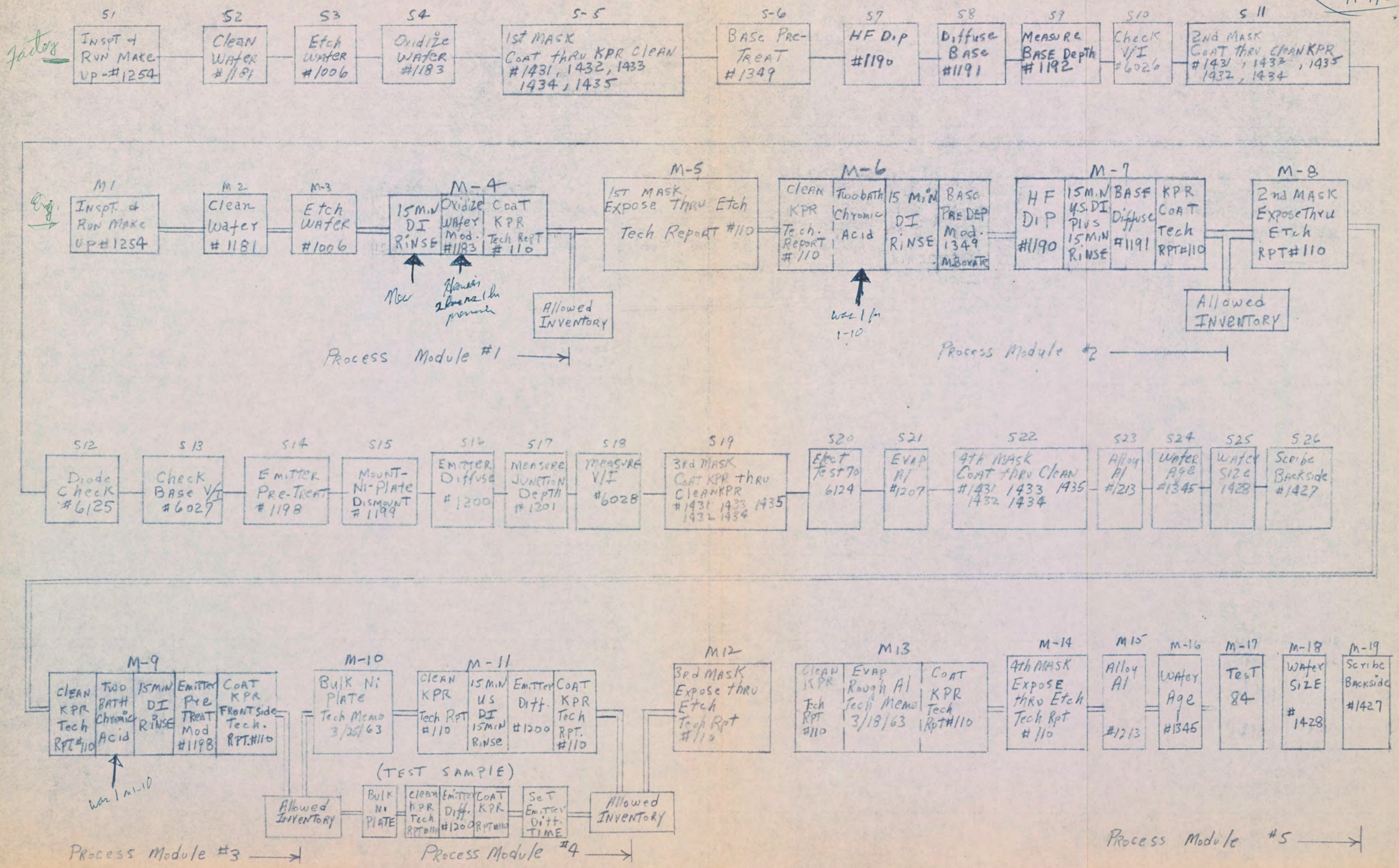


Figure #2 Standard (S), and Modified (M) Process Comparison
Runs 11-14

P. 131
4/29/63



SUMMARY of EXPERIMENTS

EK 1-10

RUN #	START RUN DATE	WAFERS STARTED	WAFERS LOST INTENTIONALLY	WAFERS LOST IN PROCESS		DIE SORT BVCES>70V
EK1	1-2-63	50	7	11	2-Etch 1-2nd MASK 5-Ni PLATE 3-4th MASK	56%
2	1-7-63	55	11	8	2-OxidATION 1-BASE Diff. 2-Ni PLATE 3 4Th MASK 1 LAP	38.8%
3	1-14-63	50	10	2	1-Ni PLATE 1-3rd MASK	49.5%
4	1-21-63	50	16	8	1-BASE Diff 3-Ni PLATE 2-3rd MASK 2 METAL	51.5%
5	1-29-63	40	3	4	2-METAL 2-MASK	46.3%
6	2-4-63	50	Rejected AT 2nd MASK due To Severe Boron PITTING			
7	2-11-63	50	6	9	1-OxidATION 2-3rd MASK 6-4th MASK	52%
8	2-18-63	45	Rejected AT 3rd MASK due to Residue from Chromic Acid bath which could NOT be removed			
9	2-25-63	49	7	5	5-OxidATION	40.7%
10	3-11-63	47	2	8	3-basediff. 2-Ni PLATE 3-MASK	53.5%

SUMMARY of EXPERIMENTS

E.K. 11-20

RUN #	START RUN Date	Wafers Started	Wafers Lost Intentionally	Wafers Lost In Process		Die Sort BVces>70V
EK 11	3-18-63	25	3	10	2 - Etch 5 - 1st MASK 1 Ni PlATe 1 3rd MASK 1 4th MASK	69.3 %
12	3-27-63	25	4	0		62.0 %
13	4-1-63	50	11	2	1 3rd MASK 1 4th MASK	72.0%
14	4-15-63	25	4	8	1 etch. 1 base diff. 3 Ni PlATe 3 3rd MASK	70.0%

Analysis of Die Sort
E.K. Runs 1-10

Run #	Run Start Date	Dice In	Good Dice %	Losses by Cause: Low B.D. $BV_{CES}<70V$	Shorts	Softs	Other	Total
E.K. 1.	1-2-63	531	56	24.8	8.4	10.7	0	100%
2.	1-7-63	412	38.8	32.	16	13.1	0	100%
3.	1-14-63	210	49.5	39.5	8.6	2.4	0	100%
4A	1-21-63	390	48	47.5	0.77	3.84	0	100%
4-B	1-21-63	400	55	37.4	3.8	3.8	0	100%
5-A	1-29-63	300	39.6	32.7	14.0	13.7	0	100%
5-B	1-29-63	602	53	25.7	14.1	6.9	0	100%
6	2-4-63	—	Lot Rejected for Boron Pits at 2nd Mask					—
7	2-11-63	300	52	39.3	5.65	3.0	0	100%
8	2-18-63	—	Lot Rejected for Scum on Wafer at 3rd Mask					—
9	2-25-63	290	40.7	50.6	1.72	6.9	0	100%
10	3-11-63	261	53.5	39.5	2.68	4.6	0	100%

Analysis of Die Sort %
E.K. 11-20

Run #	Run Start Date	Dice In	Good Dice %	Losses by Cause: Low B.D. B.V.$_{CES}$ <70V	Shorts	Softs	Other	Tota[l]
E.K. 11	3-18-63	238	69.3	18.8	4.2	7.6	0	100
12	3-27-63	244	62	18.4	13.9	5.7	0	100
13	4-1-63	251	72	15.9	10.8	1.2	0	100
14	4-15-63	250	70	22.8	3.6	3.6	0	100%
15								
16								
17								
18								
19								
20								

PiPe Count (Dice prior to die sort)
E.K. 1–10 (by emitted light under scope.)

Run #	Date Started	Dice Checked	No. of Pipes (maybe >70 v a)	
E.K. 1.	1-2-63	50	8	25
2.	1-7-63	50	11	32
3.	1-14-63	50	15	40
4-A	1-21-63	50	7	48
4-B	1-21-63	50	7	
5-A	1-29-63	50	8	
5-B	1-29-63	50	8	
6.	2-4-63	—	—	
7.	2-11-63	50	5	
8	2-18-63	—	—	
9	2-25-63	50	19	
10	3-11-63	50	20	

PiPe Count
E.K 11-20

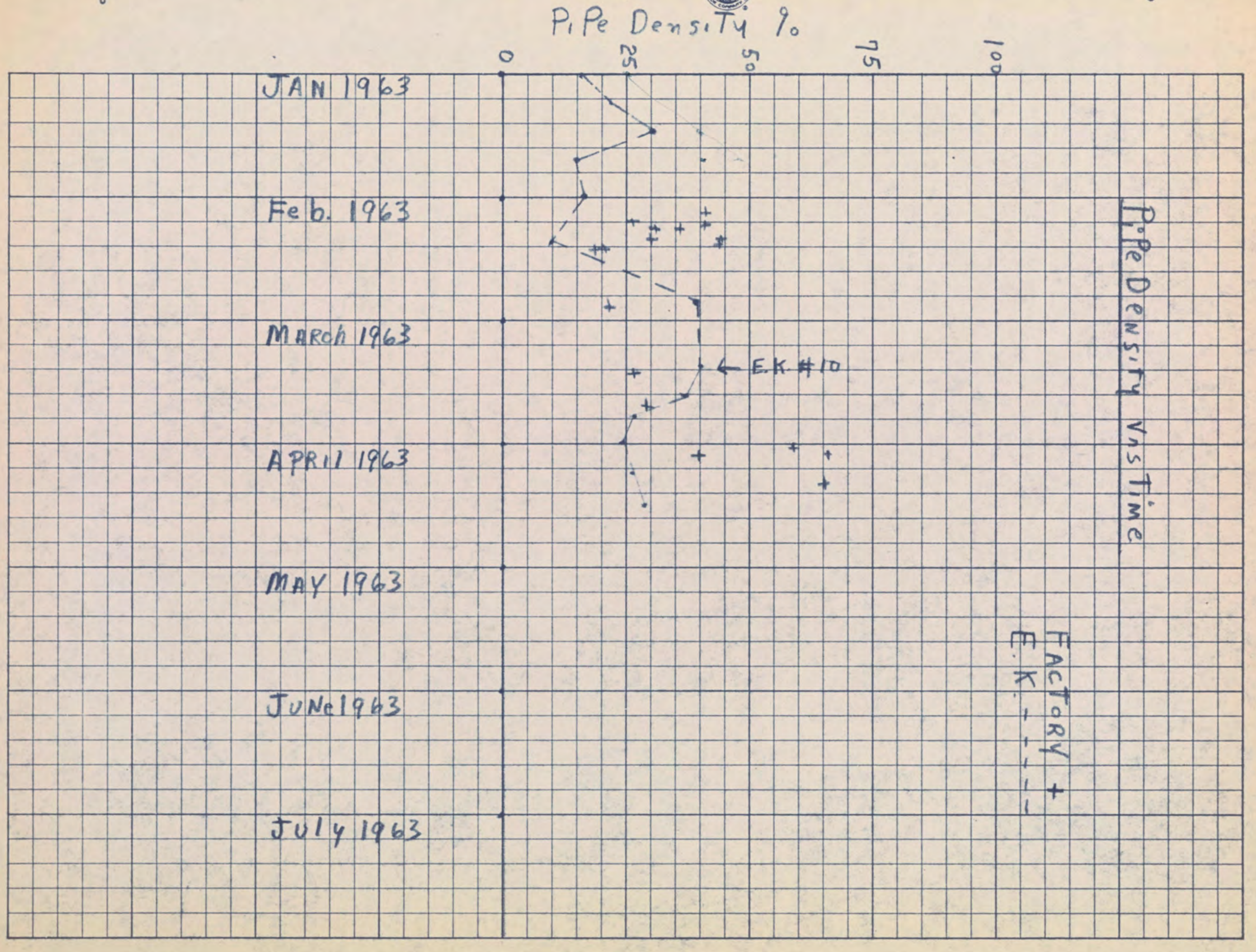
Run #	Date Started	Dice Checked	No of PiPes
E.K 11	3-18-63	100	37
12	3-23-63	100	26
13	4-1-63	100	24
14	4-15-63	100	26
15	4- -63	100	28
16			

Pipe Incident Vrs hfe
E.K 1-10

hfe	No Visiable Pipes	Visiable Pipes
>100	0, 0, 1, 5, 2, 0, 0 $\frac{6}{-}$, 5 $\frac{8}{-}$, 1, 2	0, 0, 0, 0, 0, 0, 0, $\frac{6}{-}$ 0 $\frac{8}{-}$, 1, 1
70-100	2, 3, 2, 3, 2, 4, 3 $\frac{6}{-}$, 2, $\frac{8}{-}$, 5, 2	1, 0, 1, 0, 0, 0 0, $\frac{6}{-}$ 0 $\frac{8}{-}$, 0, 2
<70	7, 6, 2, 1, 6, 6, 7, $\frac{6}{-}$ 3, $\frac{8}{-}$, 1, 2	0, 1, 4, 1, 0, 0, 0, $\frac{6}{-}$ 0 $\frac{8}{-}$, 2, 1

PiPe Incident Vrs. hfe
E.K. 11-20

hfe	No Visiable PiPes	Visiable PiPes
>100	0, 5, 0, 0, 3	0, 1, 0, 0, 2
70-100	1, 2, 0, 2, 3	3, 1, 0, 2, 2
<70	4, 1, 9, 6, 0	2, 0, 1, 0, 0


Pipe Density %
0
25
50
75
100
JAN 1963
Feb. 1963
MARCH 1963
APRIL 1963
MAY 1963
JUNE 1963
JULY 1963
← E.K. #10
Pipe Density vs Time
FACTORY +
E.K. - - - -

4/29/63 – Meeting with Process Eng. on Pipes

From R&D
Ferguson
Ormiston
Moore

Experiment was to keep batch of 100 run by identical process then add all changes at one time

Useful experiments to do:

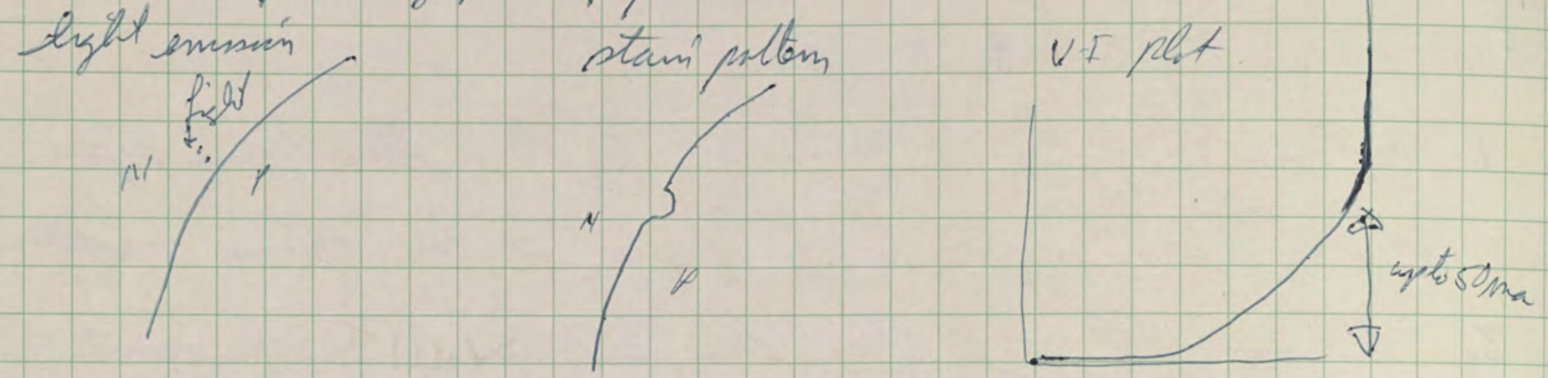
1. A p-type wafer in an ox furnace to check for diffusion pipes
2. A fresh epitaxial wafer to see if pipes at base diffusion clobber.
3. Check wafers (of 4200) after base diffusion for weak spots with the CP-6 etch. We will run with Paul's people.

 4/30/63 — Pipes and Related Phenomena

Sah, Ormute, Lawrence, Tucker, Flint — Shepherd, Kelley, Waring, Blom

Lawrence

1. The base periphery point pipe



This kind of pipe can be <u>removed</u> by etching off 1.2μ of Si.

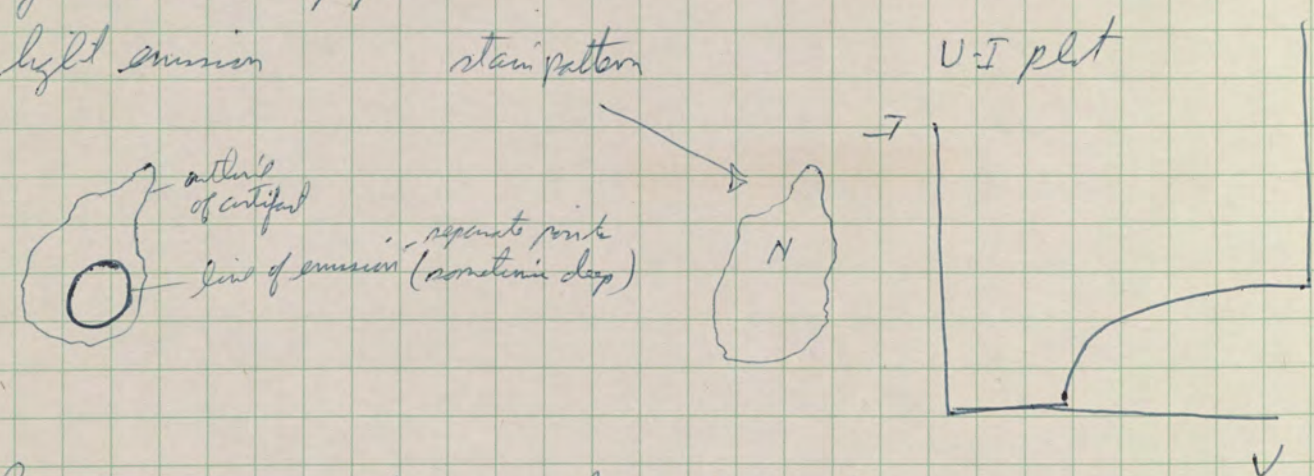
It is important to note that this type pipe gives a "soft" characteristic.

On the reject wafers he looked at, 193 out of 205 devices studied had pipes.

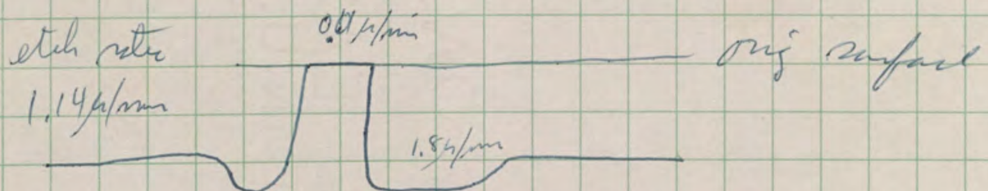
➡ Get some v. good wafers from Paul Hill.

These wafers had very few of the other kinds of ~~points~~ pipes.

2. Irregular oxide pipe —



These can occur anywhere on the surface. ?
These are usually localized to regions of the wafer.
Crossection by Sirtl etch:



COMPANY PRIVATE

P-132
4/30/63

PIPE PROJECT REVIEW OUTLINE

PROJECT NO. 105

J. E. Lawrence

I. OUTLINE FOR STUDY:

A. Define problem

B. Establish methods of analysis

C. Determine priority for investigation

D. Is this particular type of pipe associated with

1. Dislocations (bulk or surface)

2. Contamination

3. Poor oxide mask?

E. Can this parituclar type of pipe be produced at will?

F. What is this pipe as defined by

1. Electrical theory

2. Crystallographic theory

3. Chemical theory?

II. DEFINE PROBLEM:

(Find causes for all localized centers of undesirable electrical activity)

A. Categrories:

1. Base periphery point pipe

2. Irregular oxide pipe

3. Regular oxide pipe

4. Diffused pipe

III. METHODS OF ANALYSIS:

A. Characteristic electrical trace

B. Emission under reverse bias (2000x)

C. Location and natural surface appearence

D. P-N stain (CP-20 and intense light)

E. Light preferential etch (CP-10)

F. Diffusion profile or pipe and near environment (SIRTL)

IV. BASE PERIPHERY POINT PIPE (193 OF 205 DEVICES TESTED)

A. Soft junctions, not low breakdown voltages, I_{CBO} = 50 ma

B. Emission from points

C. No surface appearence

D. Stains as n-type

E. No dislocation etching

F. No diffusion profile

*G. Can be eliminated by removing 1.2μs of device by 1 minute SIRTL etch

V. IRREGULAR OXIDE PIPE (% VARIES, NORMALLY 80% OF ALL PIPES)

A. Low breakdown voltage, saturated leakage current

B. Emission from line or ring (individual microplasmas and internal field emission)

C. "Crystalline" oxide of different thickness from normal

D. Stains n-type

E. No dislocation etching

F. Very unique diffusion profile (mesa and trough)

*G. Can create crystalline oxide at will from contaminant

VI. REGULAR OXIDE PIPE (% VARIES, NORMALLY 20% OF ALL PIPES)

A. & B. As above in V

C. Regular oxide no discoloring

D. Stains n-type

E. Bar dislocation pattern usually

F. Diffusion profile (mesa no trough)

*G. Both this and the previous pipe are not positioned relative to any device. (Found in base and collector)

VII. DIFFUSED PIPE (Not widely studied yet)

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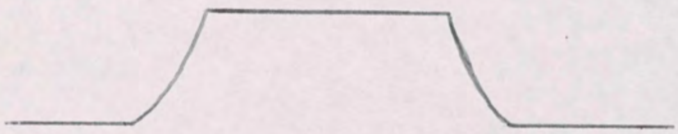
PIPE PROJECT REVIEW OUTLINE

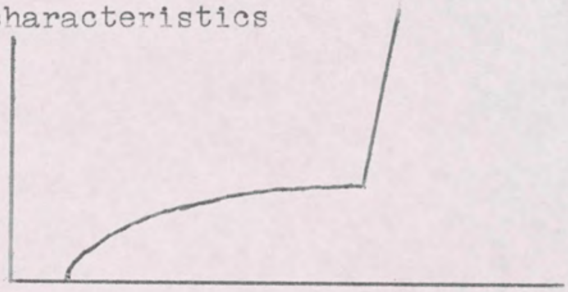
J. E. LAWRENCE

REGULAR OXIDE PIPE

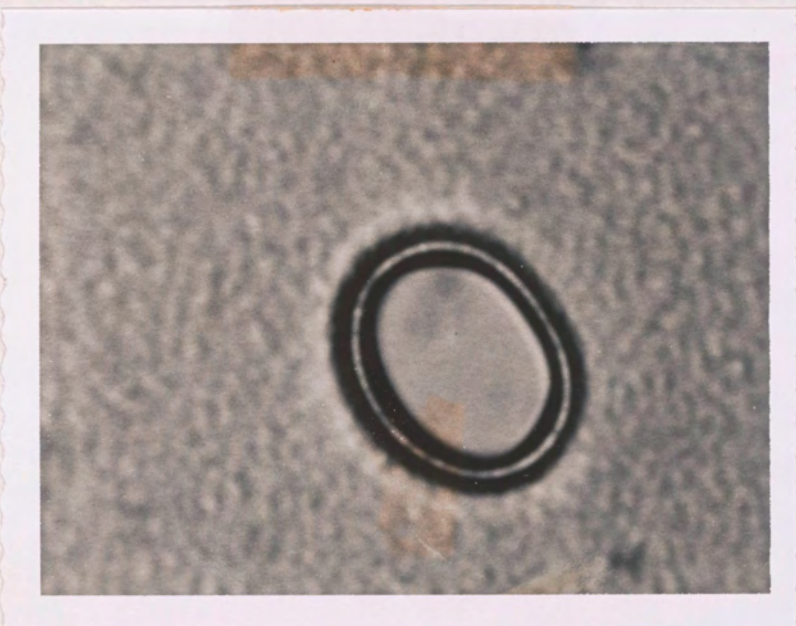
(1) SIRTL etched one minute
(2) Mesa extends 1.2 microns above the base
(3) Mesa surface dimensions 9 X 13 microns
(4) Emission ring
(5) Leakage current 12 ma
(6) Low breakdown 20 v
(7) Normal breakdown 115 v
(8) Cross section



(9) Electrical characteristics



(10) Photograph



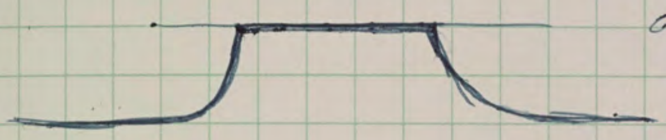
This method of preferential etching is now the best way to delineate pipes.

This blistered oxide is related to surface contamination.

3. Regular oxide pipe

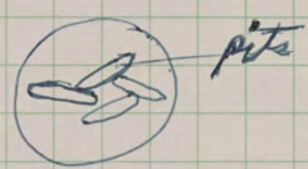
Same V-I characteristics

These etch to make a mesa, but with no moat, i.e.,



stains in a n-pattern that coincides with light emission.

These develop pits on etching



Lawrence has observed a correlation of softness and # of dislocations.

J H has sectioned an irregular oxide pipe ~~in section~~ and followed it thru the base.

Rough densities #1 193/205 units had at least one of these.

#2 localized density

#3 about 1/5 devices

#4

→ John — 1. Get good wafers

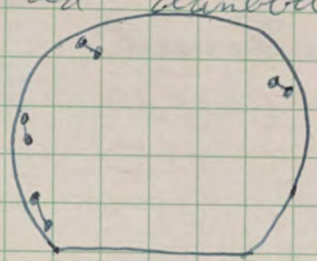
2. Examine when the non-etchable impurities come in.

The concentration of black crud contamination is now very high.

 4/30/63 — Pipes, etc, cont.

Flint —

Looking at wafer from Hills best material with Dash etch. Get the old dumbbell pits only near edge of wafer.



with the usual background pits having a relatively high concentration ~~xx~~ in an annular ring region ~~the~~ about 5 mm wide near the piping.

Phil points out that in straight HF rinses ~~xxx~~ we are in the region where Cu plates out. This occurs for acid & basic solns of ~~xx~~ Cu containing fluoride.

Cu contamination gives characteristic stars. (See P-10 fig)

Fe " " " pits, 3 types

The rounded ones like in P-14 show some peculiar long range order.

Hypotheses:

1. Surface gets contaminated roughly uniformly with metals & P. It aglomerates during oxidization.

This needs detailed layout — I'll work thru it with Flint

Ornik: From work on a PNPN with an isolation diffusion.

Some weak spots show successive B & P diffusion

Many correlate with KPR pinholes.

Visible oxide defects (under 63X) did not correlate with pipes by diffusion thru the oxide. Wafers were predeped, dipped (5 sec) and diffused.

Some pipes of this type seen with no predep — i.e., they are contamination

Cl_2 etch pits did not correlate with pipes. — Many more pipes than pits.

500X

47

An irregular oxide pipe
after etching.

From John Laurence

4/30/63 500 X

P 134
4/30/63

Surface Contamination and Dislocation Effects on Silicon Wafers

P. S. Flint
4/30/63

4200 Wafers (Krueger's - Mtn. View)

Gave Dash Etch after each of the following steps:

(1) Chemical Etch
(2) Oxidation
(3) First Mask
(4) Base Predep
(5) Base Diffusion

Results: Not definitive. Obtained chiefly small or pits randomly distributed in (1). After (2) they were denser in an annulus next to the crystal skin. A few dumbbell pits were observed very near the skin. After (4) observed greater density of small pits in base.

Need to repeat on more wafers, particularly on rejects.

Studies of Bulk Material

Attempts at deliberate contamination of wafer surfaces. Using 0.5 ohm-cm. material, although 0.005 material showed no real difference.

Copper Contamination from Aqueous $CuCl_2$

(1) Straight Aqueous - no plating of copper
(2) In HF Medium - copper plates out readily
(3) In HF + HNO_3 Medium - copper does not plate out

After exposure of the wafer to copper in one of the above ways, the wafer was oxidized, the oxide removed in HF, and defects were delineated with Dash Etch.

Results: All types of exposure to copper gave characteristic etch pits after oxidation (see photos), but the large amount of copper obtained from HF alone gave most definitive results. The copper plating appears to be a displacement reaction.

Overall, we must conclude that we can readily contaminate our wafers from pure HF solutions.

Iron Contamination from Aqueous $FeSO_4$

Iron did not plate out from HF medium, but did give characteristic etch pits (see photos).

Present studies are covering Phosphorus Contamination. There may be some preliminary results to report.

Quenching Effects

Dislocations loops are commonly formed in metals by quenching in a high concentration of vacancies.

Methods of Cyclic Quenching:

(1) Cycle from 1200°C. in steam to 25 °C. (ordinary cooling)
(2) " " " " " " " (water quench)

The above can be done with or without previous longer oxidation.

Results: In each case, obtain lines of r ounded triangular etch pits, probably indicative of slip traces. Also obtained vestiges of loops. Should combine with metal contamination.

P-14

① CP8 Etched

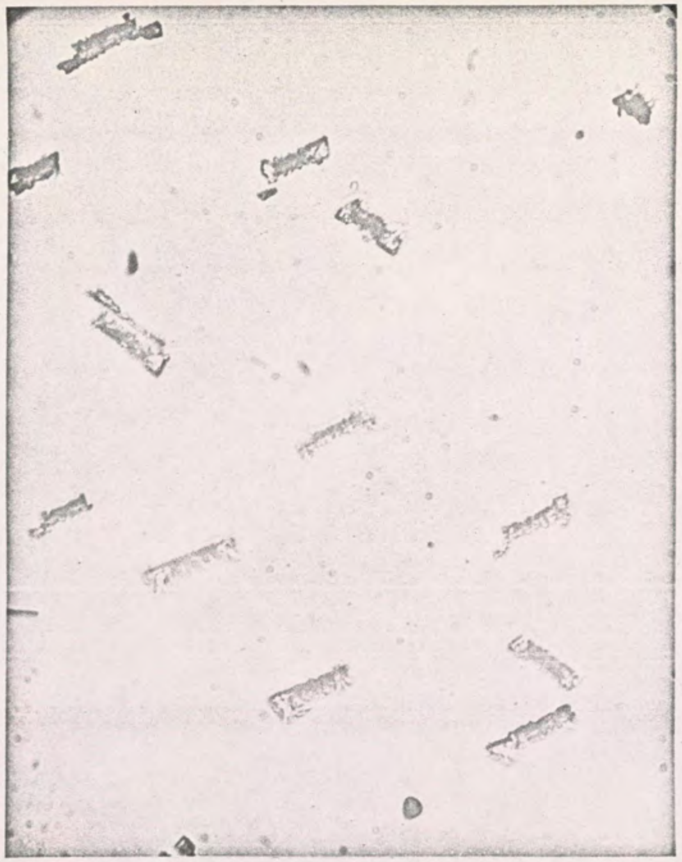
② HF + $FeSO_4$

③ Oxid. 1 hr @ 1100°C in O_2.

④ Dash Etch.

Dendrites (Stars)

(200X)



P-14

Line Pits

(with fine structure)

(400X)

P-14

Rounded Triangular Pits

(distinctively oriented)

(200X)

Iron Contamination on Silicon Surfaces

P.S. Flint
4/29/63

P-16
① CP-8 Etch
② Oxid. 4^h @ 1200°C. Steam
③ HF + $CuCl_2$.
④ Oxid. 30^m @ 1100°C. ~~Steam~~ O_2

(200 X)

After oxide stripped and the surface "dislocation" etched

P-10
① CP-8 Etch
② HF + $CuCl_2$
③ Oxid. 30^m @ 1100°C O_2.
④ HF stripped

(100X)

⑤ "Dash" etched (5-3-20)
HNO_3 HF HAc

P-11
① CP-8 Etched
② CP6 + $CuCl_2$
③ Oxid. 30^m @ 1100°C O_2

(100X)

Copper Contamination of Silicon Surfaces

P. S. Flint
4/29/63

P-15 ① CP8 Etched

② Cyclic Oxidation (4 cycles)

5 hr @ 1200°C. in Steam, cooled (standing) in air 5 hr.

③ Dash Etch.

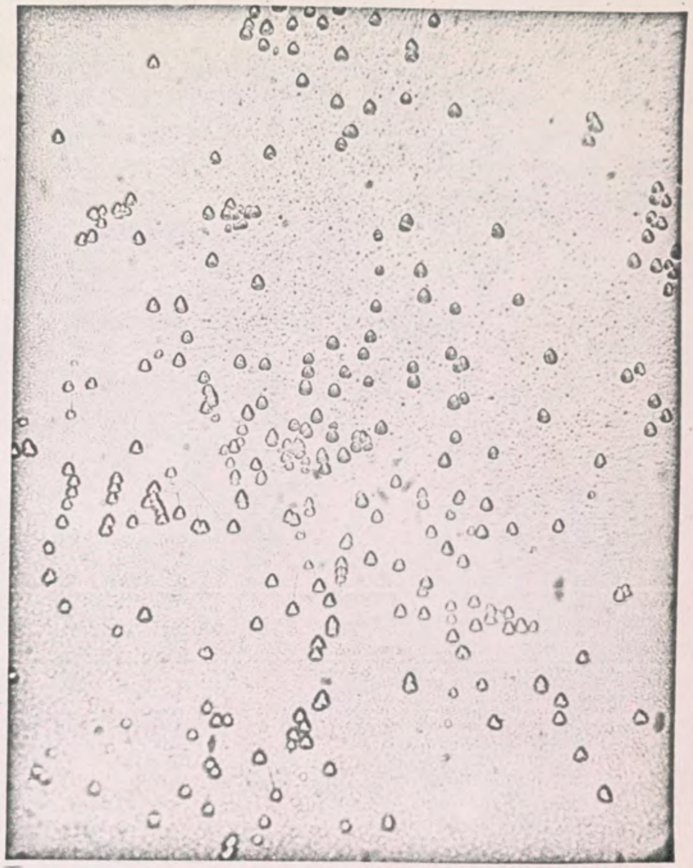
(200X)

Slip Traces?

P-15

(400X)

Loops?



P-20 ① CP-8 Etched

② Oxid. 4 hr @ 1200°C. in Steam

③ Cyclic Oxidation (4 cycles)

10 hr @ 1200°C. in Steam, Quenched in H_2O.

④ Dash Etch.

(400X)

Cyclically Quenched Oxidized Silicon Wafers

P. S. Flint
4/29/63

P-132
4/30/63

FAIRCHILD SEMICONDUCTOR

RESEARCH & DEVELOPMENT LABORATORY

TO: List

DATE: April 26, 1963

FROM: C. T. Sah

CC: G. E. Moore
V. H. Grinich

SUBJECT: Agenda for Project Review
Meeting - Tuesday, April 30, 1963
8:30 A.M. - 12:00 Noon
PIPES AND RELATED PHENOMENA

AGENDA: 8:30 - Categorize the Observed Pipes and Diffusion and Oxidation Defects
(Lawrence)
Exprimental Results on 4200 CB Diode Rejects
(Lawrence)

9:30 - Induced Pipes and Dislocation by Surface Contaminants
(Flint)

10:30 - Pipes from Weak Oxide
(Ornik)

Please have all data summarized and brief outline of discussion reproduced (10 copies) for distribution prior to talk.

C. T. Sah
C. T. Sah
Solid State Physics Section

CTS:jt

LIST:

J. Lawrence
P. Flint
L. Ornik
P. Ferguson (2)
G. Reddi
W. Shepherd
R. Tucker

RECEIVED
APR 26 1963
V. H. GRINICH

P-134
4/30/63

SUBJECT: Project Review on Oxide Defect Studies in Conjunction with SCR Development   DATE: April 30, 1963

1. The four layer SCR structure requires p-isolation diffusion. A single pipe within the 60x60 mil area will diffuse through the future active area and either produce a short or decrease the available width for depletion layer (Fig. 1, 2).

2. Pipes originating through photoresist pinholes are due to mask imperfections or due to local photoresist breakdown (Fig. 3, 4). They extend to the same depth as the isolation diffusion. The pinholes can be observed under 100X magnification.

3. Some pipes can originate prior to first oxidation as evidenced by leaving a wafer in oxidation furnace until they diffuse to sufficient size to be suitable for staining (24 hr. at 1200°C). With good housekeeping rules this pipe count has been kept between zero to five pipes per wafer.

4. However, eliminating the photoresist process and predepositing and diffusing the unphotoresisted wafers, a substantial density of pipes was still present. Only few of these pipes could be related to visible oxide imperfections (Fig. 5).

5. Chlorine etch showed two defects on a wafer from a run with pipe counts in the order of 100 per wafer.

6. Boron particle deposition was shown to occur during predeposition by diffusing wafers which have partially stripped and not stripped at all (Fig. 6). Non-dipped parts of wafer showed higher pipe densities with many small and many very large irregularly shaped pipes. However, any amount of stripping (including total strip) beyond 30 seconds 2 DI:1 HF has not improved the pipe count significantly (Fig. 6).

7. Method for lapping and staining the wafers for pipe detection was time consuming even without the long diffusions needed to attain pipes sufficiently large for visual observation. It was noticed that a wafer predeposited with boron and then CP-6 etched for 2 minutes:

   a. shows no pipes upon diffusion
   b. develops a density of etchpits similar to the observed pipe densities (Fig. 7).

8. A further experiment was performed which indicated that CP-6 induced etchpits on original oxide do correspond closely to the pipe condition when a 2-minute CP-6 etch time was used. (Fig. 8) A three-minute etch results in number of etchpits which is about twice the number of pipes introduced with 190°C predeposition to V/I = 1.0 and diffusion at 1280°C. Thus, although CP-6 is a convenient means of oxide imperfection detection, the etch time has to be tailored to suit each diffusion condition.

9. Using CP-6 etch the effect of various materials was evaluated, as shown in Table I. Even in the case of not purposely contaminated wafers the etchpits could be correlated to surface contamination or surface damage (Fig. 11B). Thus, the effect of material appears to be insignificant. A rare case of an etchpit on top of a pyramid (Fig. 9) was possibly induced by oxide abrasion after oxidation. Examples of water drop contamination are shown in Fig. 10, 11.

10. Further two-minute CP-6 checks of treatment prior to oxidation show:

a. Nickel tweezer scratch	no etchpits (Fig. 12)
b. Steel tweezer scratch	6 etchpits at the end of the scratch (Fig. 13)
c. Silicon scratch	no etchpits (Fig. 14)

d.	KPR residue (polymerized but not developed)	no etchpits (Fig. 15)
e.	Fingerprint	many etchpits (Fig. 16)
f.	Mechanically polished wafer	56/wafer
g.	Mech. polish and Chem. polish (24 μ removed)	14/wafer
h.	2 hr. dry O_2 oxidation + 2 hr. steam oxidation	4 /wafer
i.	2 hr. steam oxidation (1200°C)(control)	1 /wafer

11. It was found, however, that the damage to <u>oxidized</u> wafer can be induced quite readily with:

    a. Silicon scratch (Fig. 17, 17A)
    b. Abrasion between a silicon wafer and an oxidized wafer (Fig. 18)
    c. Nickel tweezer prick (Fig. 19)
    d. Carboloid scriber prick (Fig. 20)
    e. Diamond scribe prick (Fig.)

    No etchpits could be discovered after stainless steel tweezer prick. Evaluation of abrasion between wafers in a typical ultrasonic agitation, including dust from broken chips, has not been completed.

12. In most of the CP-6 etching a fine array of small slightly deeper etched oxide spots has been observed. The size of the spots is about 2μ and the density varies from about 1 to 10 per 25μx25μ area. (Fig. 22) The origin of the dots will not be investigated at present.

COMPANY PRIVATE

	SOURCE	TYPE	Ω-cm	WAFER Dia. mm	WAFERS 1 to 7 etched 60μ each side, rinsed in DI, blown dry & immediately oxidized 2 hr at 1200°C; others as noted.	NO. OF ETCH-PITS PER WAFER 2 Min. of CP-6	3 Min. of CP-6
1	FT(Sterling Rd.)	N	28	27		9	48
2	KEP	N(Sb)	52	24		8	23
3	DOW Corning	N	41	32	Float-zoned, disloc.dens. 20,000 cm^{-2} min.	3	6
4	KOLLSTAN	N(As)	28	24		1	22
5	KOLLSTAN	N(P)	33	24		3	12
6	TI	N	80	19	Pedestal grown disloc.dens 2,000 cm^{-2} max.	16	62
7	DUP (St. Rd)	N(4200)	1.6-2.0	24	Front side (normal lap)	8	25
7A					Rear side (rough, saw marks)	8	19
8	DUP (St. Rd)	N(4200)	1.6-2.0	24	Blotted dry w/filter paper and left exposed on lab bench for 2 hours. Handled with tweezers which have not been CP-6 cleaned.	251	
9	DUP (St. Rd)	N(4200)	1.6-2.0		A drop of DI rinsing water left to evaporate. Etchpits along the edge & within 4mm diameter of the water mark area.	117	

The following data is from various test wafers which were not part of the above experiment:

SCR 71	+ N	19	24		74	
SCR 77A(KOLLSTAN)	N	31	24		61	
SCR 79 (St. Rd)	N	8	24		32	
SCR 79 (St. Rd)	N	8	24		14	
SCR 80 (St. Rd)	N	8	24		32	
SCR 81 (St. Rd)	N	8	24		44	
REP IV (μL)	P	2		Oxide 1.5 hr at 1200°C	58	

TABLE 1

Shorter dips after predep make more pipes - Up to 30 sec the number of pipes were decreasing. If diffusion starts with steam diffusion, then even completely stripping gets to minimum pipe density.

Hypothesis is that B-containing particles on oxide surface penetrate oxide.

A wafer dipped in CP-6 (dip after predep for 2 min) has no pipes - Conclusion - CP-6 attacks the pipes.

On one wafer 2 min CP-6 corresponds to B penetration.

—

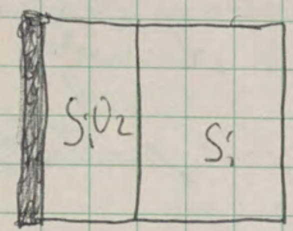
Plan:

Ormila: Why difference in regions oxides.
More on how is oxide damaged after growing.

→ Who is going to do the equivalent on P? (see JPF first)

 5/2/63 Channels & Related Phenomena

Sah:



Consider:
in Si: impurity redistribution
[surface / bulk] state

in SiO_2 - impurities

Metal - work function difference

Thurmond from thermodynamic theoretical analysis calculated the $k = \frac{C(SiO_2)}{C(Si)}$ for the various impurities.

	Al	B	Ga	In	As	P	Sb
k	10^3	10^{-3} ? to 10^3	10^{-3}	10^{-3}	10^{-3}	10^{-3}	10^{-3}

Attala tried to confirm these results — and did. — We disagree on B, Ga, In

From the reaction analysis of oxide on v. heavily P doped Xtals (~10^{19}) we confirm $k \sim 10^{-3}$.

Consider the sandwich from the energy band point of view.

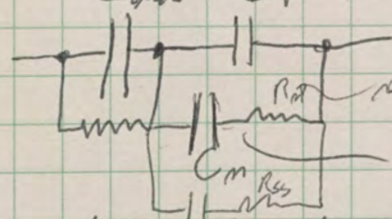
Analysis techniques: 1. Very shallow diffused junction (0.1μ) to get profile in Si

$$C = \frac{K\varepsilon_0}{W}$$

$$Q = q\int_0^W N(x)\,dx \qquad C = \frac{dQ}{dV} = q\frac{dW}{dV}N(W)$$

$$N(W) = -\frac{C^3}{K\varepsilon_0}\frac{dV}{dC}$$

2. M-O-S capacitor



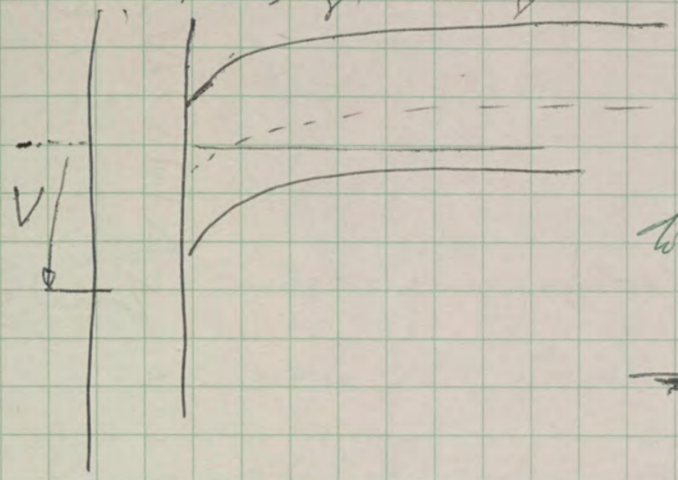
$V_{applied} = V_0 + \Delta\psi_s$
impressed ~ drop in Si

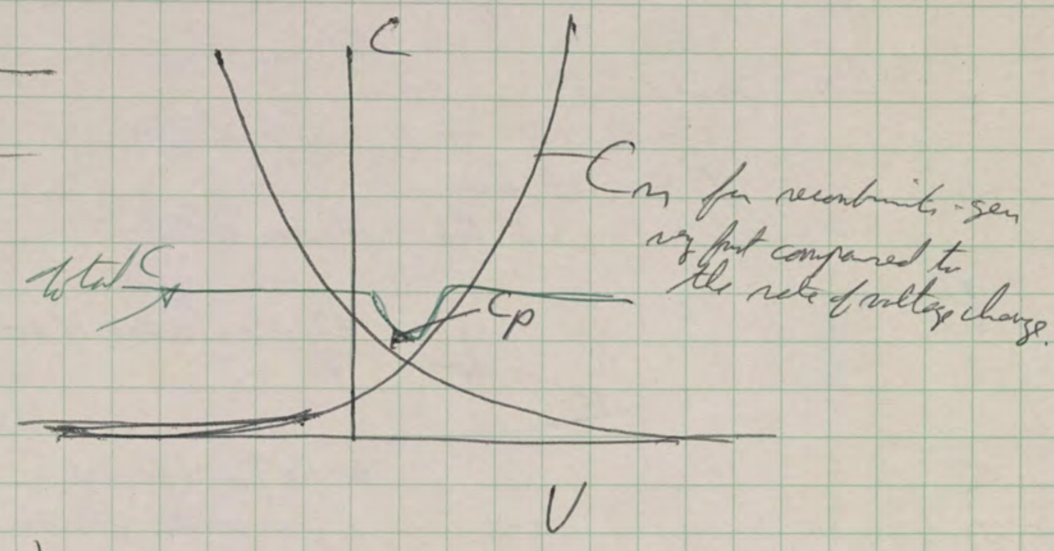
fraction ionized.

$$C = \frac{dQ}{d\psi_s} \qquad Q = q\int_0^\infty \left[(p - n + N_D - N_A) + N_t f_t{}_{bulk} + (N_T f_t)_{surface}\right]dx$$

This can be solved if N_T ~~small~~ (bulk) is ~~constant~~ neglected.

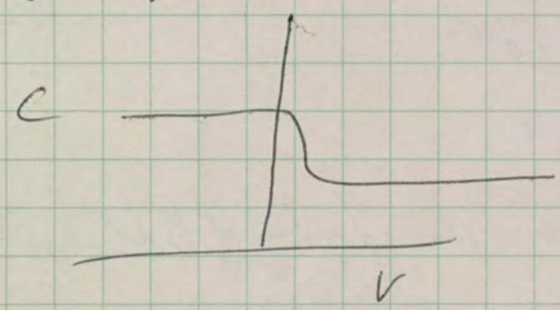
Consider a high voltage



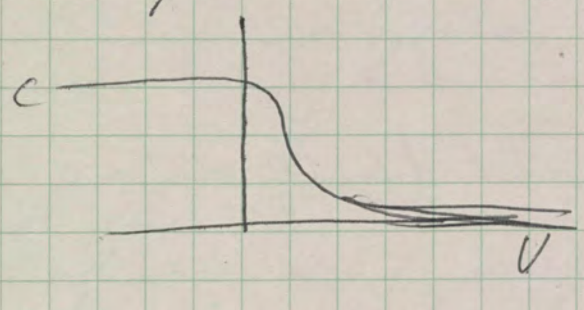


$$\therefore C = \frac{C_0(C_p+C_n)}{C_0+C_p+C_n}$$

At high frequency, ~~or~~ regeneration rate, C_n will not be impt



OR, if the oxide is leaky, one gets a depletion-type situation and gets the capacitance of a reverse biased junction

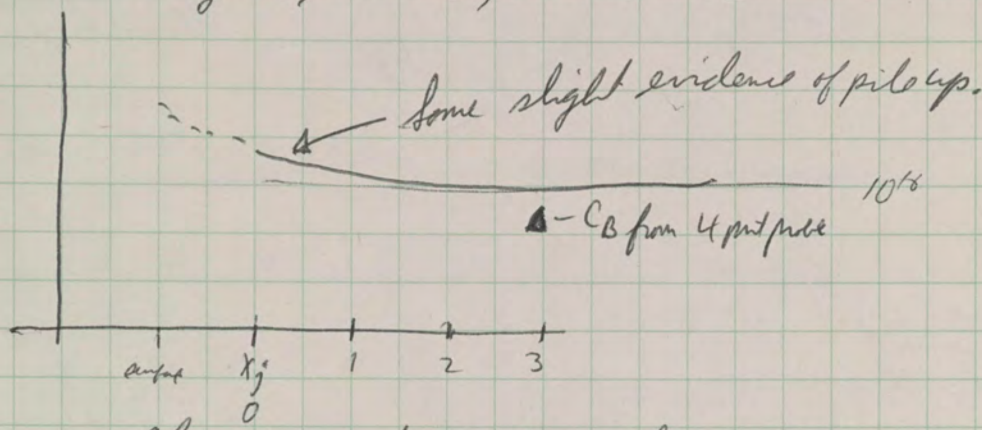


 5/2/63 - Channels, etc, cont.

Leistiko: Outdiffusion of P B Ga In

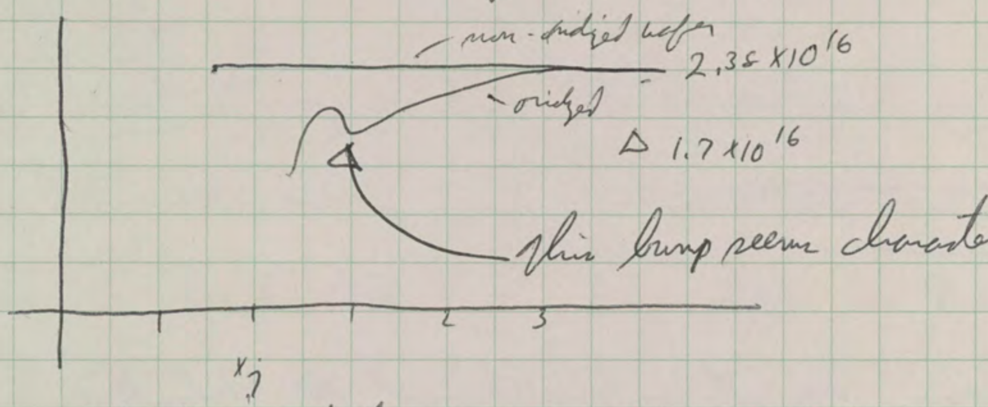
Ox. conditions
$T = 1250$
$t = 2, 15$ hrs
dry O_2, wet O_2, steam + O_2

P.



The measured C_B from the C is ~2X as high as from 4-pt probe.

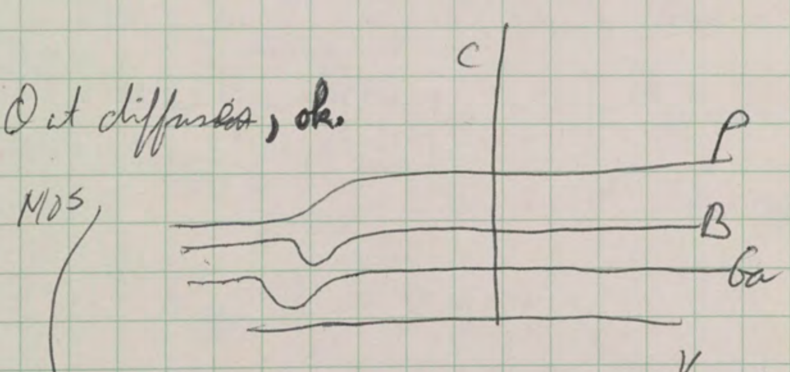
B



Fitting Atalla eqn, get ~7×10^{15} for C_0. Get k ~12 for steam + O_2.

Ga also out-diffuses in O_2, but definitely more in $N_2 + H_2$, and t correspond to O_2 oxidization rate.

In Out diffuses, ok.



ie, all strongly n-type surfaces.

5/2/63, cont

Grove: for MOS capacitance

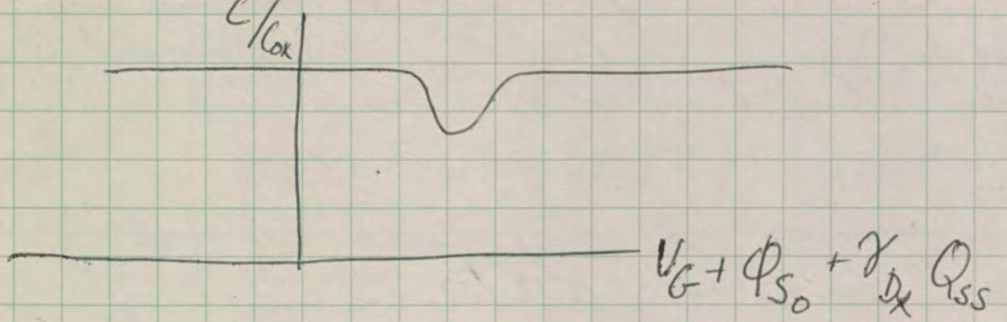
Three approximations of C_S:

1. $N_D - N_A + p - n$ (Const fixed charge, no oxide leakage)
2. $N_D - N_A + p$ (electrons can't follow)
3. $N_D - N_A$ (leaky oxide)

2 & 3 run them together.

Assume effective surface ~~state~~ charge.

1. SS
2. A correction for effect of bending by out diffusion.



Match this with C/C_{ox} vs V_G experimental data.

read off $\phi_{S_0} + \gamma_{Dx} Q_{SS}$

With other curves, get 1. ϕ_{S0}
2. Field at surface
3. Q_{SS} effective
4. V_g for surface inversion

Deal:

various oxides compared
wet oxides varied, but all showed dips
dry oxides were uniform, but didn't go back up
pyrolytic went to pot
anodic showed a swing or a variation of ε

The dielectric constants are all over the map. Only the dry O_2 agrees well with the fused SiO_2 value

 May 6, 1963 — Thin film resistors - planning meeting

ref. p.113 (4/4/63)

On question from last time:

1. NiCr + Ta sputtered film — no results yet.

2. A couple of runs of NiCr at ~~high~~ ~~ss~~ <100 Ω/□ (30-90) seemed to show the same range of percentage variation during alloying.

3. The double masking to avoid the alloying cycle has not really been done yet

My evaluation of the status of Nichrome film:

At present they are useful only if a ±50% variation in the un-adjusted resistor can be used. In that case ~~they are good~~ the ratios are significantly better, although I'm not sure how close.

The FCC films are Ru 90%, Pt 10%. They drop ~ ~~80~~ to 1/4 or 1/5 during aging in air. They do, however, have several KΩ/□.

On Ta — Nobody talks about our kind of T cycle. Everybody, however, includes a thermal aging step.

There is a strong indication that the Nichrome films do not vary randomly, but change abruptly. It seems possible to run a test batch to determine how the system is behaving and then adjust the monitor value accordingly.

Heinz Ruegg will run Nichrome with this test wafer method.

We will borrow a mass spectrometer to try to tie down the effect of residual gas. If it tracks things down, we'll buy one.

We will also try to see why films vary.
a) Substrate
b) Chemical composition
c) μ structure.

Table III

Mean res. change a. TCR for different alloying ambients (2 min 580°C in clean furnace). Film evap. from NiCr wire. Substrate temp. 350°C.

Run#	cool down in air		10 min cool down in N_2 or Ar	
	alloyed in N_2	Ar	all. and cooled in N_2	Ar
63	-4% +250	-4.8%	-8%	-
64	-16.8% +160		-19.9%	
65	-18% +358ppm	-13.4% +380ppm	-20.8% +410ppm	-12% +395ppm
66	-21.3%	-12.4%	-19.2%	-24.1%

(Previously all changes were + instead of —)

Table IV

Mean res. change for alloying in clean furnace and in standard furnace. Film evap. from NiCr wire. Substrate temp. 350°C.

Run #	Standard furn. 2 Min 580°C, N_2. Cool in air	Clean furnace, 2 Min 580°C, N_2	
		cool in air	10 min cool in N_2
69 (5min cure at 650°C in vacuum)	+19%	+19%	+27%
70 (no cure)	+3%	-3%	0

P-140
5/6/63

Table V

Res. change of films on different substrates.
(2 min 580°C N_2 alloying. Evap. from NiCr. wire, Substrate at 350°C)

Run #	Cooling in air after all.		cooling in N_2 for 10 min.	
	Si-SiO_2 - wafer	micr. glass slide	wafer	slide
68	−4%	sl. 1 +5%, sl. 2 −12%		
72 clean furn	−19%	+22%	−21%	−7.5%
73 stand. furn.	+4%	+6%		

Table VI

Res. change for different alloy temperatures.
(Evap. from wire; Substrate at 350°C; 2 min in N_2, cooldown in air; stand. furnaces)

Run # ↓ Alloy T →	550°C	565°C	580°C
71	+4%	+2%	+7%

a) Q. Is a "real" substrate equivalent to a freshly oxidized wafer?
Heinz Ruegg will answer this one.

b) Q. We know that contact resistance does not bother us in the 2-3 K Ω resistor range. What is the influence of contact resistance? We will design a universal contact resistance measuring mode that allows a definitive statement of what the contact resistance is.

c) Q. What physical phenomena correlate with the changes?

Can measure
R
dR/dT
Hall effect
Angles from ellipsometer
electron microscope
" diffraction

d) Q. What process variables control?

The mass spectrometer is our best bet.

For the Ta work

→ 1. "Duplicate" our existing capability on ceramic - get a test vehicle from D.D. that they could use.
Heinz will supply test vehicle.

2. Track down problem ASAP
Jim has a program laid out on wafers and will send a copy to us.

The Alexsons now look usable at 5 KΩ/□. By vacuum alloying and anneal to recover β, data looks pretty good with ~±30% or better. Ready for a Dev. Dev. test vehicle.

Downgrade Cermets for now, although possible for ceramic substrates

 Project Review — Digital Integrated Circuits —(Almost the whole lab)
Inc. JPF, VHG, CTS, WV, HP, RR, and JPF people (Craig, Farina, Potter, Reid, Graff, Porter, Gault, Noelle) Schmidt, Daniel, Weidner, Yim, Wegton

On the epi μL

Cum yield (fab) >50%
Last weeks die sort = 17%

12,000 hr (25 units) @ 200°C storage — 2 failures
1. Scratch
2. "Vanishing metal" open. (Also had a scratch)

32,000 dev hrs op @ 125°C @ 4X regular power — no failures but much scatter
More than a little problem with drift of units of originally high leakage. Farina does not think that it is channels.

In order to eliminate the "vanishing metal" problem, M.V. has stopped washing.

About 1/2 of M.V. failures are channels across the isolation. They had high V/I and long isolation diffusion. We have not seen the problem up here. They are dropping V/I ASAP.

~~Porter~~ Sentnor is running the B, H, F, C deal.
Mtn View is fixing up their rotary reactor.

Kit. components

Transistors: KTA (10 ma) — also making on relatively high ρ material 1-1.5 Ω cm.
KTB (4 KTA)
KTC (Matched pair of xstors, somewhat larger emitter)
μTA (— to 100 ma)

Resistors:
R-1, R-2 } The old μL masks. Two more old
Sentnor laying out new masks.

A test vehicle to compare 0.5, 1, 2, Ga, FET, epi bulk, resistors is in the mill.

Diodes: — Use the multiple emitters of a KTA.

Future process work:

1. There is an anomaly in the storage time - range 8-30 ns on a run basis. Reason - unknown, but it looks like a problem in keeping the Au in.

We are presently running 10-14 nsec. JPF thinks that possibly with better thickness control and higher T Au we can get them all < 10 ns.

2. Epitaxy - 1. good control for min isolation
   2. Opt. oxide - pyrolytic?
   3. What do we need on ε oc contacts? - Potential size reduction.
   ~~4. Straight~~

3. Straight size reduction

As soon as these are tied down, we feel that our technology is that which we must ride with.

A major problem looks like probing of dice. It starts to look impossible.

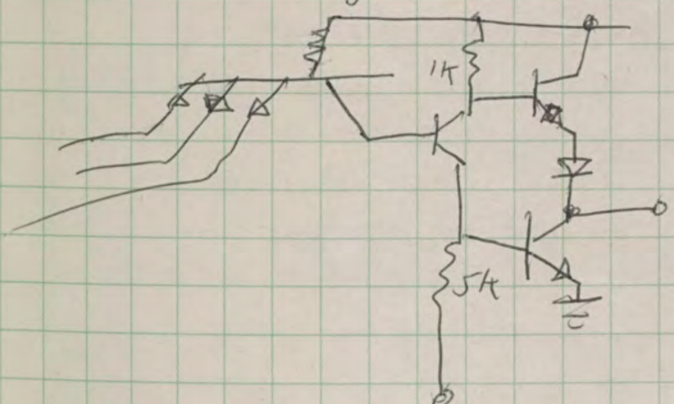
Ckt Forum: - Farina

Comp. review

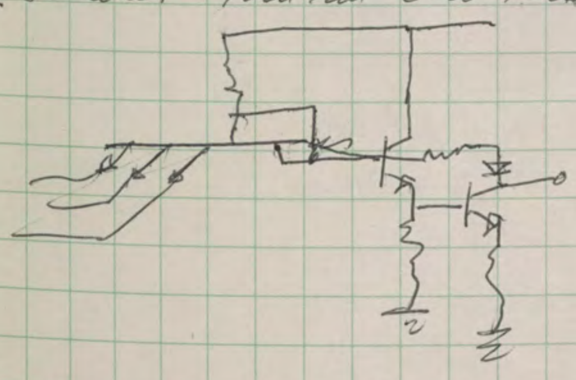
A lot of people have T^2L.

PSI is making

Sylvania advertised briefly, then changed it into a non-sat NAND



Sillconix - non sat diode network



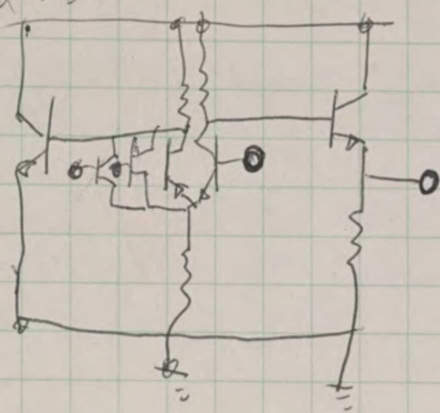
	$\bar{t}_{pd}$	P_d	Junctions (#)
epi μL	10-14	15	15
Sylvania	12-15	10	10
(diode NAND) Signetics	20-30	6	10
(very small, ½ ¼ ml) Siliconix	12	5-6	13
FSC DTL	10	5-6	13
MECL	3.5	35	
FSC, low power	30	3	10
DCTL-3	8	15	10
CML #1	5-6	15	20

FSC DTL is different

Future Fan

Farina – discussion of future:

~~Model~~ MECL



We modified to: 1. put E-follower on input to save standby power
2. added current source

Ours is not very powerful logically – various functions are difficult

The mask is just about ready to be cut for our new CML gate.

What are the requirements for our next family of digital circuitry?

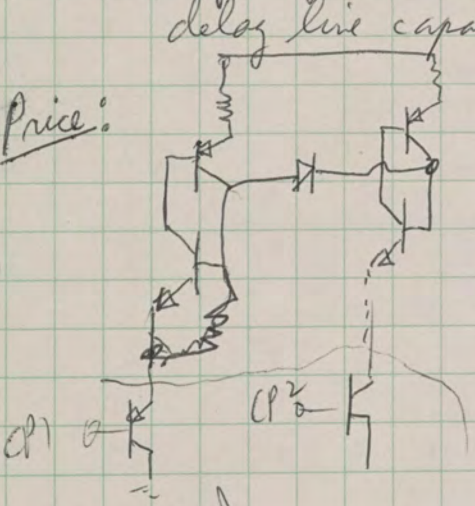
1. No DCTL
2. Highest possible speed (or low power at reasonable speed)
3. Powerful logical capabilities including a do-able binary.

Porter points out that by using series-gated DCTL for low power looks good.

Misc. devices.

PNPN shift register – Don Farina has reservations about our objectives, it is not compatible with anything. It has delay line capabilities, however.

Price:



This is evidently useful only for some extremely specific use of a register. Arguments against it are ones of compatibility.

Price's modification goes to 4 diffusions and an epitaxial growth. – Back to p-c processing. The only advantage is size.

The clock pulses must be ~~optimal~~ properly phased. –

RECEIVED
MAY 7 1963
GORDON E. MOORE

INTERNAL CORRESPONDENCE

FAIRCHILD SEMICONDUCTOR

A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

TO: G. E. Moore ✓
V. H. Grinich

DATE: May 6, 1963

FROM: J. P. Ferguson

CC: Section Heads
D. E. Farina

SUBJECT: Agenda for Digital Integrated Circuits Project Review

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Status of Epitaxial Micrologic (15 min.)

a. Mt. View status
   1. Characterization
   2. Process differences
b. Life tests
c. Kit parts

Future Process Work (15 min.)

a. Oxide/metal improvement
b. Epitaxy
c. Size reduction
d. Resistors

Circuit Forms

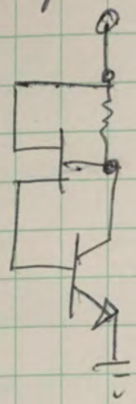
a. Competitive evaluation
b. High speed
   1. CML - straight and differential
   2. Improved DCTL
   3. Binary implementation possibilities
c. Low Power
   1. Non-saturating NAND
   2. DCTL
   3. Binary implementation possibilities

Miscellaneous Circuits (30 min.)

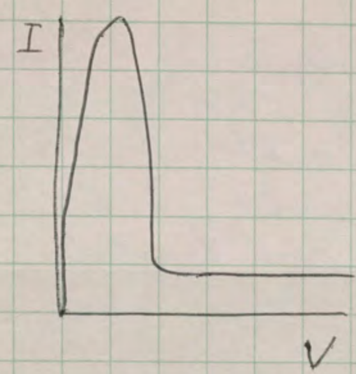
a. PNPN registers
b. Diode converter and diode matrices

JPF:jh

So Price proposes a ckt like



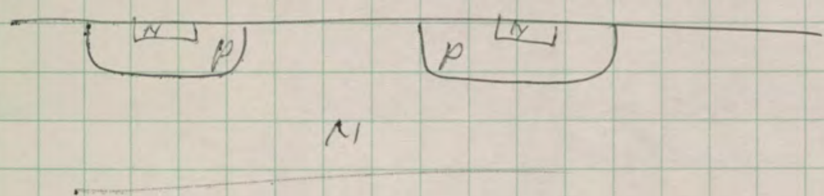
— gives a



which then gets designed to something "horrible complex" using p-type MOSTS with isolated Xstors and even a Zener diode.

As near as I can see this whole area of digital integrated circuitry is badly up in the air. I have no a) understanding
b) confidence in our layout of program.

Diode matrices: — This is still alive!



also trying complement.

Try to kill ~~Xstor~~ action by Au.

If this goes on, it should have an objective. Can get a Binary-Decimal Converter in 30×40 mils.

For some reason that escapes me, there is a strong effort to make everything more complicated in order to fit it into the μL processing exactly.

General discussion c̄ Dick Stone on Xducers: 5/7/63 UHG Pleasure J.K. Dick Stone

Process control limitations: drift (long term) + thermal hysteresis

Low level (a relatively large existing market) 0-50 mv
High level (" " new & small market) 0-5 v - Telemetry
We were 1st and had excellent vibration characteristics

The low level stuff should be 350Ω bridge
Should be 100 - 5000 lbs/sq in
30 - 130°F ± ½%

Need for extend T range, the rest is tough
-65 - 250°F
Needs .01%/°F - if .005, then real competitive.

People are pushing for ½% 0-offset; now take 3%.

High level one
Works on unregulated power, 24-32 v
Single end common (ie isolated)
5 v out
Can be as bad as ½% on combined linearity + hysteresis.
Shunt calibration
1000Ω output impedance.
"Must take a hell of a beating"
-65° - ~200°F

Must be < $1000, pref ~ $700.

The high level market is only ≈ 1M$/year

As far as Stone is concerned, no-one is interested at all in anything but 0-50 mv or 0-5 v. "The guy that chose 250 mv must have had a gourd on his shoulders".

A 0-15 lb wet-wet differential would be a world beater.

Discussion on the S&R camera:

1. Fde will check possibility of a replacement front door.
2. " " " " " a different-Cursal. He will get Moore's recommendation.

3. I will investigate c Russel if he can build ~~one~~ one in a finite amount of time.

"If we can spend $15K to get on the air reliably, we will be happy to."

Russels tech to write manual.