IBM FIRST IN IC MEMORY

1970 — IBM System/370 Model 145 is announced with Burlington’s 128-bit memory chip, “Phase 2I.” It is the first IBM computer to use monolithic circuits for all memory and logic functions.

IBM SP 95
First COMPUTER IC MEMORY SP95- 16 BITS, IBM System 360 Model 95-1965

Phase 2I Memory
First COMMERCIAL IC MEMORY
PHASE 2-64 Bits Buffer
PHASE 2I-128 Bits Main Store, IBM System- 370 Model 145 - 1970
IBM has filed applications for a patent on the 16-bit monolithic memory array developed by IBM's component development department at East Fishkill. It is the first application from East Fishkill on a monolithic integrated structure.

Three separate applications were filed—the basic one and two others on inventions used in the monolithic chip which could be used in other monolithic structures. Six men listed as inventors on one or more of the three applications are Dr. Benjamin Agusta, Dr. Paul Berdell, Paul G. Henie, Martin S. Hess, and Raymond P. Peconno.

Although only two and a half times the size of an SLT chip, each monolithic chip has 80 transistors, in addition to several components. The new chips are compatible with SLT and involve almost the same amount of processing time.

"Sixteen-bit" refers to the 16 circuits on each chip. Each circuit represents one byte of information by being "on" or "off.

The circuits are called "integrated" because they cannot be broken down into separate components. Integrated circuits on which all electrical elements are fabricated within a single chip of silicon are called "monolithic.

Filing a patent application indicates commercial interest in an invention," says Alvin J. Riddles, manager of patent operations, Fishkill. He pointed out that time and expense are involved and that three years or more can go by after filing before a patent is issued.

To give IBM the fullest protection on the invention, the basic application covers monolithic structures, package, and fabrication methods. The basic application, says Mr. Riddles, patent attorney who prepared the application.

Monolithic integrated circuit chip, below, on which patent applications have been filed, is only 2 1/2 times as large as SLT chip, above, but contains 80 transistors plus 64 resistors and 4 diodes.

**United States Patent Office**

**3,508,299**

**MONOLITHIC INTEGRATED MEMORY ARRAY STRUCTURE INCLUDING FABRICATION AND PACKAGE THEREOF**

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**ABSTRACT OF THE DISCLOSURE**

A monolithic integrated semiconductor structure is described that has a plurality of functionally isolated individual cells that are electrically interconnected. Each of the cells is an isolated or intermixed plate cell that is vertically, horizontally and diagonally displaced from the other cell. The plurality of cells provide a memory array with electrical components of each memory cell comprised of active and passive semiconductor devices. Other important aspects of the structure include intercell connection and active devices on a common portion of the structures which are electrically interconnected at the same node potential by means of a highly doped doped region within the common portion of the structure.

This invention relates generally to monolithic integrated structures including the fabrication and packaging thereof and, more particularly, to a monolithic integrated memory cell that is expandable into a memory array of 256 x 256 number of integrated memory cells where q and i are integers and q is either zero or an integer greater than zero.

Ferreoci coast over the years have established an opinion regarding the having electrical characteristics that are not a function of time. However, the metallic wire that threads the wires is subject to corrosion and must be protected, depending upon the atmosphere in which the wire will operate. In some instances, wherein corrosion of the wire in the array can cause physical damage resulting in a short circuit.

A monolithic memory array containing 64,000 words has been fabricated with a minimum size of component and interconnection. A 5-bit monolithic memory array utilizing the unit cell of the invention would have 25 million transistors and 25 million other components in the same area. The addition of the dedicated storage and decade circuitry will greatly increase the density of the memory cell. These limitations on the reliability considerations must be determined in aggregate, in IBM (Basic Operating Memory) times.

The key to the formation of a monolithic memory array in the monolithic memory cell.

**Corporations, etc.**

(1) The cell should be capable of being expanded into a memory array and each memory cell with minimum damage to the memory performance.

(2) It should consist of devices that occupy a small area to obtain maximum arrays per package.

(3) The cell should consume very little power so as to permit high package densities and minimum power supplies and power line requirements.

(4) The cell should have a fast read capability when expanded into an array.

**1.** The cell should have a fast write time capability when expanded into an array.

**2.** The cell should have low internal inductance in order to obtain fast switching capability.

**3.** The cell should have a fast recovery time after reading or writing operations so as to permit fast cycle repetition rates.

**4.** The cell should have non-destructive read capability, thus permitting faster memory operation since no read or write cycles do not have to be followed by a write cycle.

**5.** The memory state of the cell in an array should be AC and DC isolated from the sense line and thereby not be sensitive to output signals and other noise generated by read or write operations and noise pulses on the sense line.

**6.** The memory line in an array should be randomly accessible as opposed to serial fabrication storage device such as to permit fast cycle time.

**7.** The cell should consist of component devices that permit topological interconnection relationships such that the fabric array can be simply fabricated and interconnected. This results in the use of a costly second conductive level or insulating layer and reduces the amount of underpass connectors needed.

**8.** The cell and array should preferably have reactive components such as capacitors and/or inductors since these are relatively difficult to fabricate in a monolithic structure.

**9.** The cell and array should haveiode fabrication techniques that are easily achievable with monolithic lithium fabricating techniques.

**10.** The cell and array should be operable over a wide temperature range without performance degradation.

**11.** The cell should have a complementary output, thus permitting differential signals and, if needed, in large arrays or for logic purposes.

**12.** The cell should contain a minimum number of low value supply voltages and be consistent with logic circuit voltages.

**13.** In order to obtain universality of usage, the cell and array should be adapted to operate over a wide range of voltages without performance degradation. This feature also permits a longer life and greater reliability since it is less sensitive to device degradation time. Also, it can withstand adverse environments without degradation effects.

**14.** The cell should preferably not contain complementary devices (PNP and NPN), thereby making the monolithic structure designed for a particular purpose.

**15.** The required overflow, drive, sense, and decode circuits, which will expand the memory array, a monolithic integrated chip, must have device requirements compatible with the cell, preferably without the need for additional process steps.

**16.** The device specifications of the read, drive, sense, and decode circuits should be such that they take advantage of technology in the development of a clearer photomask and diffusion tolerances which give greater integration and, hence, process tolerance that simultaneously improves memory performance and cost.

**17.** The cell can either be modified to accommodate memory applications.

**18.** The cell can be readily modified for either 2 or 3 dimensional operation. A 3 dimensional operation takes advantage of the first stage of address decoding. A square or rectangular mask of either 2 or 3 dimensional results in minimum external control connections.

**19.** The cell and array should have a minimum number of input/output signal lines.

**20.** The cell should have some inherent error correction.
Phase 2I 128 bit IC Memory-1970
Lying on a Magnetic Core Mat
MEMO TO: Mr. P. P. Castrucci

SUBJECT: SP95 Terminal Report

Please express my sincere appreciation to everyone for their part in the SP95 program and, especially, the extra effort to make this illustrious report.

The SP95 program has laid the groundwork for a new technology revolution in IBM.

R. E. Markle

rem/cd

cc: Mr. R. P. Pecoraro
Hello, and welcome to the 40th Anniversary Dinner of the IC Memory Patent. As I look around the room I see a lot of familiar faces and I know that several of you were directly involved in the development and manufacturing of the first integrated circuit memory. I also know that everyone in the room has been touched by the IC Memory. The IC Memory technology has made possible today's digital world. It has affected the way we work play and many other aspects of our lives. How did it happen?

Let's take a walk down memory lane. Our walk will take us from Textile Mills to the Moon - from Winooski in the 50's to Essex Junction in the 90's. A short trip of 40 years. In the 1950's Winooski was experiencing very tough times. The Textile Companies were closing their Mills and moving south. There was widespread unemployment in the area. GBIC (Greater Burlington Industrial Corporation) wanted to attract new businesses to the area to alleviate the unemployment. They put up an industrial building in Essex Junction on the Winooski River. That winter, Tom Watson President of IBM, came to Vermont on a ski trip. GBIC met with Watson and convinced him to start a manufacturing operation in Vermont. IBM started their Vermont operation in 1955 - 50 years ago. The plant's first product was a mechanical, electrical relay - a computer device that was an end of life technology. Vermont was thankful for the IBM plant but it was concerned that the demand for computer relays would diminish and IBM's future in Vermont would be in doubt. Lucky for Vermont, a significant new memory technology was being developed at IBM East Fishkill.

The 1950's computers utilized magnetic, donut shaped cores for memory, a technology that was lacking in many ways - too slow - too expensive and with very low density. Without the invention of the IC Memory, computers could never be what they are today and IBM could not have grown into a $96 Billion International Company.

A paper written in 1970 by Professor Michael Rappa of the MIT Sloan School states: "The relentless pace of progress in computer Memory Storage is widely recognized as one of the twentieth century's most remarkable technological achievements. What is less known is that it occurred largely within the confines of a single company, IBM." In 1965, the Semiconductor Line in East Fishkill was developing ultra fast high performance transistors that were required to drive High Speed Core Memories.

In the spring of 1965 Eric Bloch, IBM VP of engineering, who later became the Director of the National Science Foundation, called several of us to his office. - Dr Ben Augusta, Ed Hec, Jack Shortel and myself. Ben and I were from the Components Division an Ed and Jack were from the Computer Systems Division. Eric told us that Bob Henley (The Components Division First Fellow) had written a White Paper stating that Integrated Circuits are good for logic applications but even better for Memory applications. Eric told us that IBM would ship a High End, Scientific, System 360, Model 95 to NASA in 1966. The Computer had a small Systems Protect Memory for data security. Eric said that he wanted us to build it out of integrated circuits. None of us had any experience with integrated circuits. As we went out of his office, he said "Don't worry if you can't do it, I can build it out of other technologies, even tubes."

Ben and I went to work! Ben decided what circuit design to use and I modified the Silicon, bipolar, wafer, processes in the line to meet the specifications that Ben required. We also developed techniques and processes to produce the photo masks that we needed. We also designed and built the first of a kind tester to electrically check our memory wafers.

Our first SP95 wafers reached electrical test two weeks before Christmas. We couldn't believe our eyes. The circuits were flipping and flopping at speeds that we never anticipated. We packaged the Memory chips and installed the System Protect Memory in the Model 95 Computer. The High End Computer was shipped to NASA in mid 1966. Based on the rapid success of the SP95, IBM, decided to develop IC Memories for their Commercial Computers.

A 64 bit IC Memory was developed for the Buffer Memory and the 128 bit IC Memory for the Main Memory. These first of a kind IC Memories were developed in East Fishkill and transferred to Essex Junction, Vermont for volume production. On October 21, 1970 the New Digital Age was born when IBM announced the Model 145- the first computer with 100% logic and memory electronics. IBM Vermont became the source for the Memory and for the next 20 years became the IC Memory capital of the world.

The IC Memory is a classical example of "Disruptive Technology". Disruptive Technology dramatically changes the status quo and affects the way we live, work, and play. Examples of disruptive technology are the Automobile, the Electric Light, the Jet Engine and the Microprocessor. Disruptive technologies usually take 10 to 15 years to go from test tube to market place. The IC Memory only took 12 Months from concept to the Market Place. The IC Memory invention enabled the digital age and it dramatically changed man’s ability to manage, explore, change, and improve our earthly home. It has also allowed us to explore space, land men on the moon and put robots on Mars.

The best in IC memories is yet to come! When it does, you can be sure that IBM and Vermont will be the leaders for the new technology and for tomorrow's advanced Digital age.

Paul Castrucci