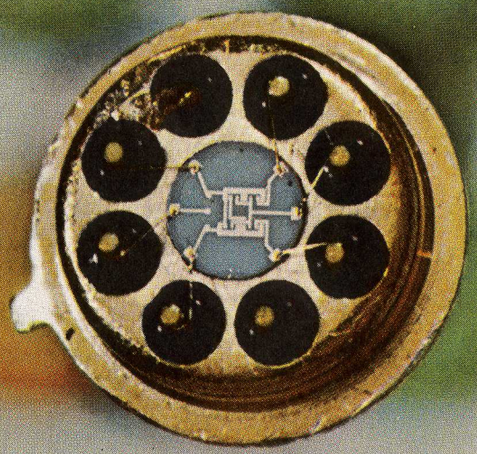
EDN

ELECTRICAL DESIGN NEWS

A CAHNERS PUBLICATION

JULY 1961



Micrologic Circuit Applications
Recording and Text Pg. 44

EDN SPECIAL REPORT

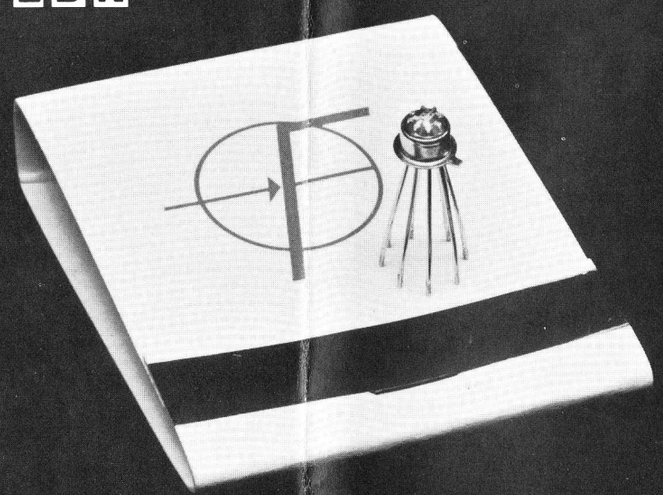


Fig. 1—MICROLOGIC FLIP-FLOP on (TO-18)-size header

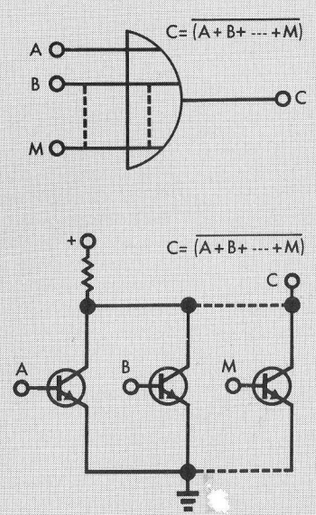


Fig. 3—LOGIC SYMBOL and SCHEMATIC for basic DCTL NOR gate

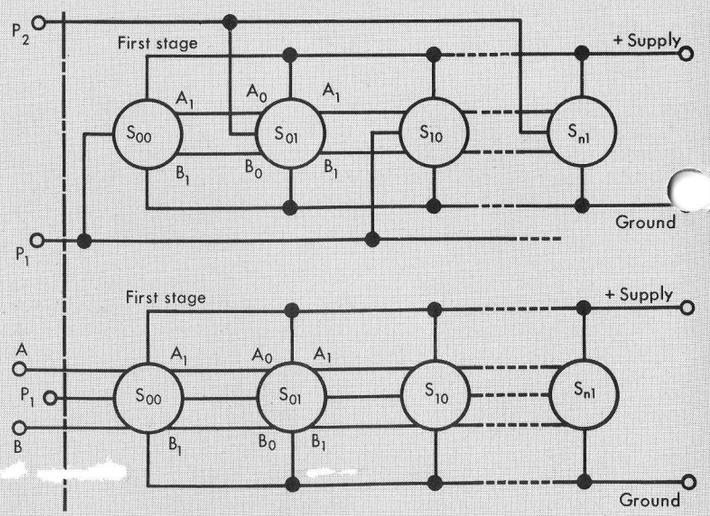
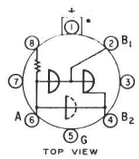


Fig. 4—INTERCONNECTIONS FOR SHIFT REGISTERS, using two methods of clocking

MICROLOGIC ELEMENT "B"
BUFFER

SUPPLY VOLTAGE + 3 V_{dc} ± 30%
POWER DISSIPATION 25 mW (TYP.)
TEMPERATURE -55°C TO +125°C

$B_1, B_2 = \overline{A}$

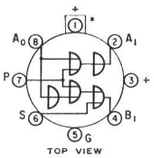


INPUT (TERMINAL 6) - CAN BE DRIVEN BY ANY MICROLOGIC ELEMENT - 2.2 MICROLOGIC LOADS
OUTPUT (TERMINAL 2) - CAN DRIVE UP TO 5 OTHER MICROLOGIC ELEMENT LOADS IN PARALLEL (TERMINAL 4) - CAN DRIVE UP TO 25 OTHER MICROLOGIC ELEMENT LOADS IN PARALLEL
(NOTE - TERMINALS 2 AND 4 MAY NOT BE USED CONCURRENTLY)
AVERAGE DELAY - (TERMINAL 2) - 50 nsec., (TERMINAL 4) - 60 nsec.
MULTIVIBRATOR OPERATION - CONNECTING TERMINALS 1 AND 8 PROVIDES A POSITIVE RETURN FOR A CAPACITOR INPUT TO TERMINAL 6

MICROLOGIC ELEMENT "C"
COUNTER ADAPTER

SUPPLY VOLTAGE +3 V_{dc} ±30%
POWER DISSIPATION 75 mW (TYP.)
TEMPERATURE -55°C TO +125°C

$\overline{A}_1 = \overline{A}_0 \overline{P}$
$\overline{B}_1 = A_0 \overline{P} + S$

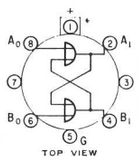


INPUT - CAN BE DRIVEN BY ANY MICROLOGIC ELEMENT.
A_0, P (TERMINALS 7,8) - 2 MICROLOGIC LOADS
S (TERMINAL 6) - 1 MICROLOGIC LOAD.
OUTPUT (TERMINALS 2,4) - CAN DRIVE UP TO 5 OTHER MICROLOGIC ELEMENT LOADS IN PARALLEL.
AVERAGE DELAY - 100 nsec.
NOTE - THE NODE RESISTORS OF THE OUTPUT INVERTERS ARE RETURNED TO TERMINAL 3 WHICH IS NORMALLY CONNECTED TO THE SUPPLY VOLTAGE.

MICROLOGIC ELEMENT "F"
FLIP - FLOP

SUPPLY VOLTAGE + 3 V_{dc} ± 30%
POWER DISSIPATION 30 mW (TYP.)
TEMPERATURE -55°C TO +125°C

$\overline{A}_1 = B_1 + A_0$
$\overline{B}_1 = A_1 + B_0$

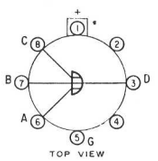


INPUT (TERMINALS 6,8) - CAN BE DRIVEN BY ANY MICROLOGIC ELEMENT - 1 MICROLOGIC LOAD
OUTPUT (TERMINALS 2,4) - CAN DRIVE UP TO 4 OTHER MICROLOGIC ELEMENT LOADS IN PARALLEL.
AVERAGE DELAY - 50 nsec.

MICROLOGIC ELEMENT "G"
GATE

SUPPLY VOLTAGE + 3 V_{dc} ± 30%
POWER DISSIPATION 15 mW (TYP.)
TEMPERATURE -55°C TO +125°C

$D = (\overline{A + B + C})$

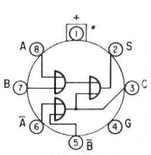


INPUT (TERMINALS 6, 7, 8) - CAN BE DRIVEN BY ANY MICROLOGIC ELEMENT - 1 MICROLOGIC LOAD.
OUTPUT (TERMINAL 3) - CAN DRIVE UP TO 5 OTHER MICROLOGIC ELEMENT LOADS IN PARALLEL.
AVERAGE DELAY - 50 nsec.

MICROLOGIC ELEMENT "H"
HALF ADDER

SUPPLY VOLTAGE + 3 V_{dc} ± 30%
POWER DISSIPATION 45 mW (TYP.)
TEMPERATURE -55°C TO +125°C

$S = A\overline{B} + \overline{A}B$
$C = AB$

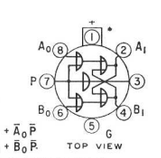


INPUT (TERMINALS 5, 6, 7, 8) - CAN BE DRIVEN BY ANY MICROLOGIC ELEMENT - 1 MICROLOGIC LOAD.
OUTPUT (TERMINAL 2) - CAN DRIVE UP TO 5 OTHER MICROLOGIC ELEMENT LOADS IN PARALLEL.
OUTPUT (TERMINAL 3) - CAN DRIVE UP TO 4 OTHER MICROLOGIC ELEMENT LOADS IN PARALLEL.
AVERAGE DELAY - (TERMINAL 2) - 100 nsec., (TERMINAL 3) - 50 nsec.

MICROLOGIC ELEMENT "S"
HALF SHIFT REGISTER

SUPPLY VOLTAGE + 3 V_{dc} ± 30%
POWER DISSIPATION 75 mW (TYP.)
TEMPERATURE -55°C TO +125°C

$\overline{A}_1 = B_1 + \overline{A}_0 \overline{P}$
$\overline{B}_1 = A_1 + \overline{B}_0 \overline{P}$



INPUT - CAN BE DRIVEN BY ANY MICROLOGIC ELEMENT.
A_0, B_0 (TERMINALS 6,8) - 1 MICROLOGIC LOAD
P (TERMINAL 7) - 3 MICROLOGIC LOADS.
OUTPUT (TERMINALS 2,4) - CAN DRIVE UP TO 4 OTHER MICROLOGIC ELEMENT LOADS IN PARALLEL.
(TERMINAL 3) - CAN DRIVE 5 MICROLOGIC LOADS.
AVERAGE DELAY - 100 nsec.

* TAB LOCATES LEAD No. 1

Fig. 2—PRELIMINARY CHARACTERISTICS OF MICROLOGIC ELEMENTS

COVER STORY

MICROLOGIC ELEMENTS
Their Applications in Circuit Design

Robert H. Norman, Section Head, Device Evaluation, and Richard C. Anderson, Engineer, Device Evaluation, Fairchild Semiconductor Corp., Mountain View, Calif.

ROBERT H. NORMAN is a graduate in Electrical Engineering of Oklahoma State University and a member of the I.R.E. and the American Ordnance Association. His primary duties at Fairchild include evaluation of new semiconductor devices and engineering guidance of the Micrologic program. He was formerly with Sperry Gyroscope Co. where he was concerned with development of transistorized logic circuitry. He has various patents pending in semiconductor computer circuits.

RICHARD C. ANDERSON is a member of Tau Beta Pi engineering honor society, the I.R.E., and has an M.S. in Electrical Engineering from Stanford University. Prior to his association with Fairchild he was a Lt. (j.g.) in the U. S. Navy. His major assignments in his present position have been the evaluation of developmental Micrologic elements, logic design, and Micrologic applications.

A complete logic-function circuit in a single crystal of silicon is now available as a product from Fairchild Semiconductor Corp.

This circuit, a Micrologic flip-flop, is the first member of a set of six compatible digital functional building blocks, each circuit diffused by the Planar process into a single chip of silicon. The second member of the set, the gate, will be in production shortly, and the remaining members will be made available at intervals thereafter.

Each Micrologic element contains from three to nine equivalent transistors and their associated circuits. The chip containing the circuit is mounted in a hermetically sealed TO-5 or TO-18 eight-lead package. The elements operate at speeds up to 1 mc with a fan-out of five over the full range of military environments, including a temperature range of —55C to +125C. As is the case with similar functional blocks, the use of Micrologic elements can result in a 10-to-1

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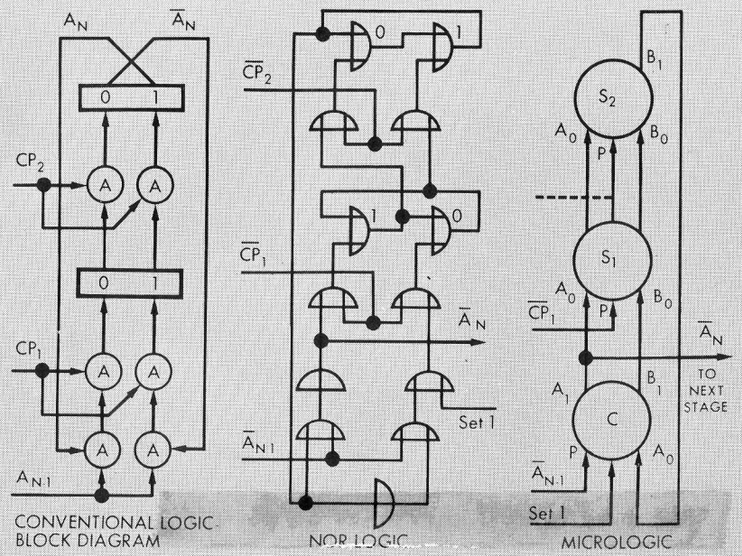
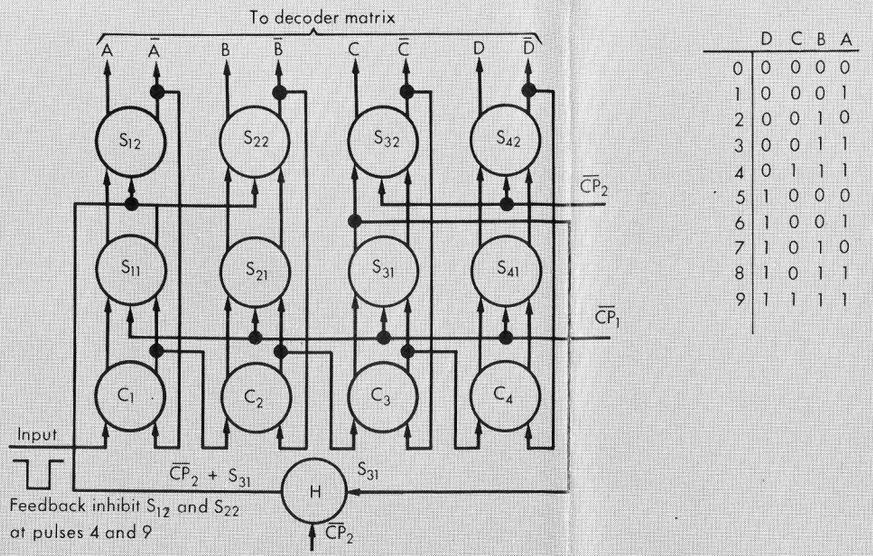


Fig. 5—BINARY COUNTER STAGE WITH CARRY GATE



	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	1	1
5	1	0	0	0
6	1	0	0	1
7	1	0	1	0
8	1	0	1	1
9	1	1	1	1

Fig. 6—MICROLOGIC DECIMAL FAST-CARRY COUNTER

savings in the number of components handled. A computer logic section fabricated by using Micrologic elements will occupy approximately one-tenth the volume of one using best conventional techniques. This volume reduction can be achieved with the TO-5 package. Use of the TO-18 package with welded-wire construction techniques will yield another order of magnitude reduction in logic section volume. At the same time, it is expected that the production cost of a logic section fabricated by using Micrologic elements ultimately will be about one-fourth the cost of contemporary logic sections. This will result from the low cost of the elements themselves as well as the reduced design, fabrication and testing cost of a Micrologic computer.

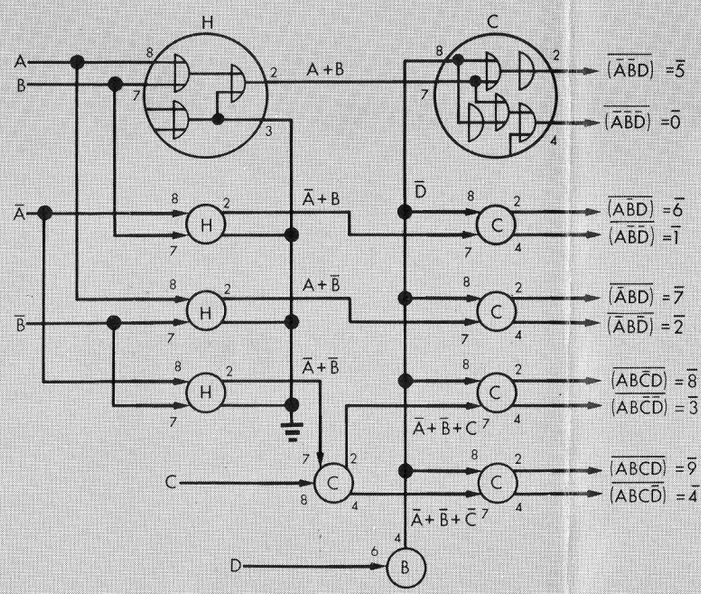
Preliminary characteristic sheets of the six Micrologic elements comprising the set are shown in Fig. 2. The basic NOR gate structure used in these elements, as well as its associated logic symbol, is shown in Fig. 3.

The functions of the "G", "F" and "H" elements are self-explanatory. The "S" element, or half-shift register, is a gated flip-flop. When connected in cascade as shown in Fig. 4, these elements can be used to form a shift register. The arrangement shown is the familiar master-slave shift register configuration. This element, of course, also finds wide use as simply a gated flip-flop.

The "C" element was developed for use with "S" elements to form various counter configurations such as those shown in Figs. 5 and 6, hence the name counter adapter.

The elements described above have fan-outs of either four or five. This is usually adequate for logic circuitry; in those cases where higher fan-out is required, the buffer element may be used. This element has a fan-out of 25. It is encountered most often as a shift

(Continued on next page)



	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	1	1
5	1	0	0	0
6	1	0	0	1
7	1	0	1	0
8	1	0	1	1
9	1	1	1	1

Fig. 7—MICROLOGIC DECIMAL DECODING MATRIX

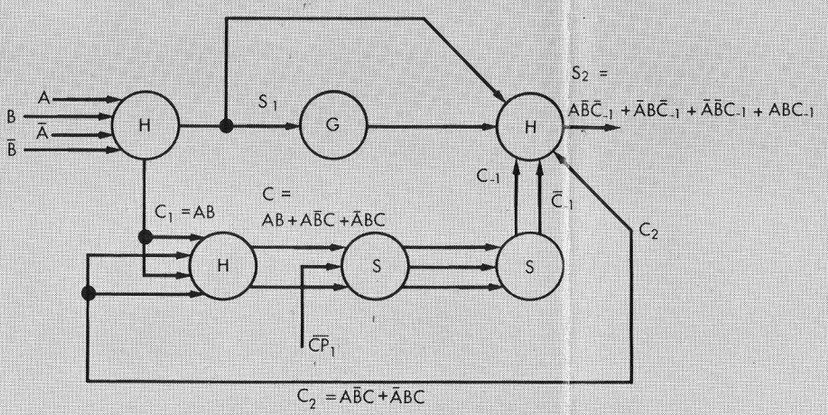
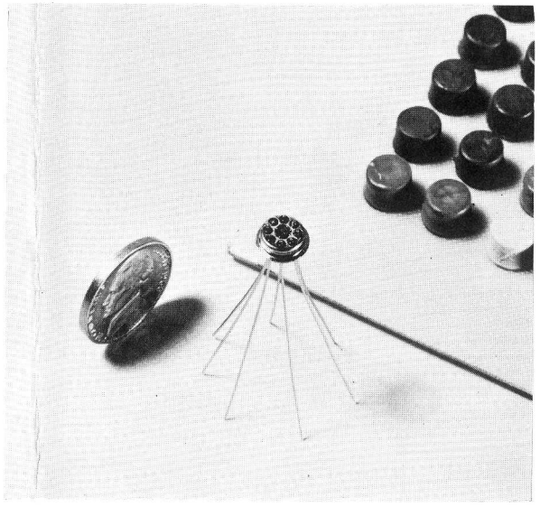
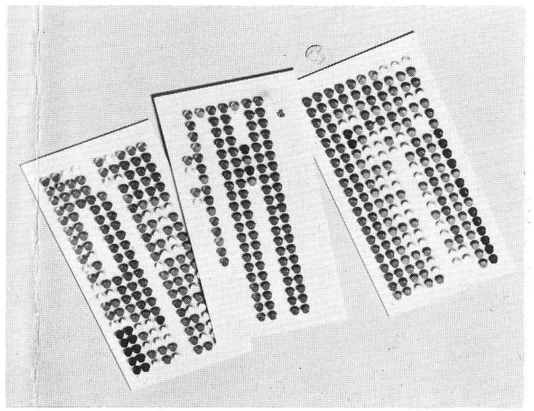


Fig. 8—MICROLOGIC SERIAL FULL ADDER



MICROLOGIC flip-flop on (TO-5)-sized header.



COMPUTER LOGIC SECTIONS fabricated by using Micrologic elements.

pulse or clock pulse driver in a logic section. The application of Micrologic elements to some typical logic configurations is shown in Figs. 6, 7 and 8. The use of the more complex logical capabilities of some of the Micrologic elements in these configurations results in a significant reduction in the number of Micrologic elements required.

Because the process for making the elements is so similar to the making of individual Planar transistors, it is felt that the Micrologic elements are basically reliable and stable. In addition, the reliability of a Micrologic element should be at least as high as that of any well-designed logic circuit. A reliability evaluation program is under way, but as yet insufficient information is available with which to make definitive statements concerning reliability.

Preliminary information from the program indicates that Micrologic elements are as reliable as Planar transistors; no measurable parameter changes were observed in production flip-flops after the first 3000 hours of operation at 125C. When sufficient reliability information is accumulated, it will be published. Of course, system reliability improvements will be gained through the reduced number of intercomponent connections as well as interassembly connections.

More detailed descriptions of these Micrologic elements, as well as discussions of the development program philosophy and implications of their use to the equipment manufacturer, appear in publications listed in the references.

In conclusion, a set of miniature, digital, functional blocks is becoming available which is intended to be economical, useful and reliable. These Micrologic elements, which are adequate for most logic function requirements, and which can be interconnected by using already developed contemporary techniques, will yield reduced logic section costs through economies in component costs as well as fabrication costs. At the same time they will give a logic section reliability equal to or better than that which can be achieved by using contemporary techniques.

References:

1. D. Farina, J. Nall, R. Anderson, "Application of Micrologic Elements", presented at National Electronics Conference, Oct. 10, 1960.

2. R. Norman, R. Anderson, "Testing of Micrologic Elements", presented at Western Joint Computer Conference, May 9, 1961.

3. J. Nall, R. Norman, R. Anderson, D. Farina, J. Campbell, "The Fairchild Semiconductor Microelectronics Program", presented at AIEE Symposium on Microelectronics, May 17, 1961.

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