CUSTOM MICROCIRCUIT DESIGN HANDBOOK

FAIRCHILD
SEMICONDUCTOR
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1. INTRODUCTION

The requirement for larger, more complex systems for military and commercial applications continues to increase. Generally, in conjunction with this trend, there is the demand for more reliable, trouble-free system operation.

Practical considerations to keep systems within physical bounds have called for miniaturization. The subsequent emergence of solid state techniques and the development of miniaturized passive elements have made considerable size reduction and performance improvement possible. Unique packaging arrangements, whereby miniaturized parts are combined into miniature circuits, succeeded in accomplishing size reduction. However, in many cases connections are the conventional type, involving tedious microscopic techniques, and the reliability improvement achieved is questionable.

Another circuit miniaturization technique, arising quite naturally from the semiconductor field, has been the combination of basic semiconductor dice (transistors and diodes) along with miniaturized or thin film passive elements on single headers and in small packages.

A third approach is the silicon integrated microcircuit, existing in a single semiconductor substrate. This approach more nearly fulfills all of the miniaturization and reliability requirements and offers significant potential system cost reduction. It also offers possibilities of remarkable increase in reliability at circuit costs potentially approaching that of a single transistor. These integrated microcircuits are produced by proven Planar methods of the semiconductor industry including masking, oxide photolithographic etching, diffusion, evaporation and epitaxial growth. These processes are useful in producing circuits for both digital and linear application.

Furthermore, the usual batch processing, a technique with excellent repeatability, is very adaptable to the production of large quantities of integrated circuits at low cost.

Integrated circuits, by their very nature, must be produced as complete units. Design errors, or even minor circuit changes will involve expensive re-tooling costs. The earliest integrated circuits were fabricated using successive design, whereby a circuit was built and tested to determine the corrections required in following circuits. In this "evolutionary" design manner a partial repetition of the total processing expense had to be incurred for each of the interim design steps. Using such an approach, the final circuit cost becomes unnecessarily excessive owing to the extensive development costs.

This handbook points out the unique characteristics of integrated circuit parts, such as transistors and resistors, and how they may be represented electrically in a realistic breadboard, how to determine the level of complexity allowable for a practical integrated circuit and what special design rules must be observed in designing a custom integrated circuit.

Design examples of a linear amplifier and a logic gate are included to illustrate circuit selection, initial design procedures, and final circuit results. A realistic performance specification describing an integrated circuit is shown as a model to illustrate a specification geared to fully insure performance, yet not unnecessarily penalize yield.

The role of the hybrid circuit which contains a combination of an integrated circuit and conventional elements, is discussed. A number of conditions calling for this type of an approach are listed.

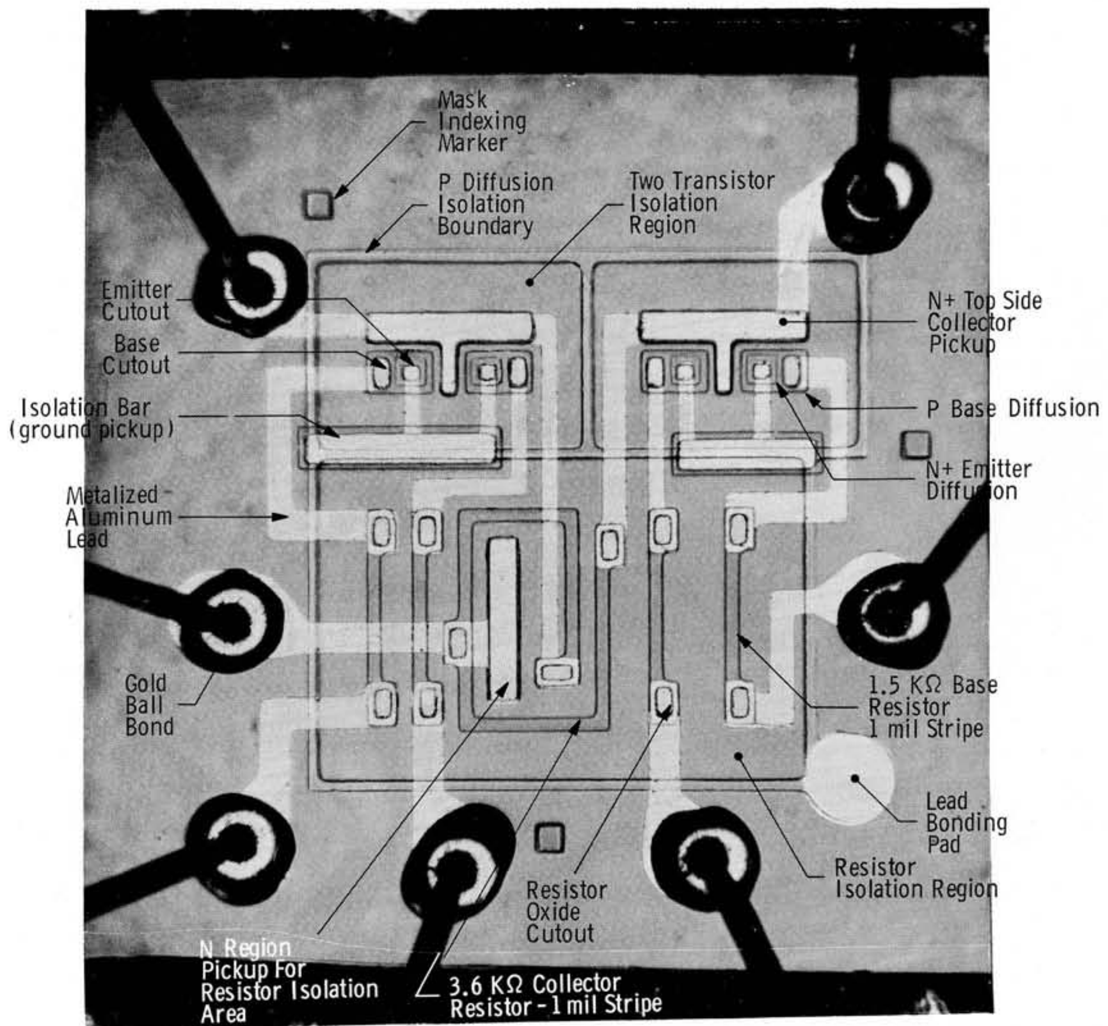
Data sheets are available for some of the integrated circuit parts. These will be augmented with additional data covering individual parts and complete circuits as new developments are made.

2. INTEGRATED CIRCUIT DESIGN AND MANUFACTURE

Fairchild technical papers and brochures are available which describe the complete fabrication process for integrated circuits. Briefly, a wafer is sliced from a grown N-type doped silicon crystal. After polishing and cleaning, a layer of oxide (SiO_2) is grown over the entire wafer. The first, or isolation diffusion, is P-type doping which separates the wafer into individual N-regions. These are designed to be isolated electrically from each other by reverse-biased diode junctions. Next, resistors and transistor bases are formed within these N-regions by a second P-diffusion. Finally, an N+ diffusion of very high impurity density is made to form the transistor emitters inside the base diffusion areas, and to form low resistivity topside collector contact points. The oxide which serves as a diffusion mask and a junction protector is then selectively etched away only where contact to the circuit parts is desired. Metal is deposited on the surface of the wafer to make contact with the circuit where the oxide was etched away, and over the oxide to form the circuit intraconnections. The circuits are next physically separated into dice by cutting the wafer with a diamond scribe. They are optically inspected, sorted according to electrical behavior, mounted in a package, connected to wires with thermal compression bonds, sealed in the package, temperature cycled, spun in a centrifuge, and then retested electrically. One finished circuit is shown in Figure 2-1.

The pockets of N+ material around transistor bases are the transistor collectors' topside contacts. The collectors are isolated from each other by the back-to-back diodes created by the isolation diffusion (see Section 3.1). If the isolation region is connected to the most negative circuit potential, then each transistor has its collector connected to the cathode of a diode which can never become forward biased. This isolation diode contributes extra leakage current and shunt capacity at the collector. Since the resistors are formed by a P-diffusion into N-material, they have distributed capacity and a distributed diode associated with them.

Figure No. 2-1 Chip with Construction Callouts



Thus these parts in an integrated circuit have different characteristics from conventional parts, and are difficult to analyze. However, this does not mean an integrated circuit must be made before its performance can be known. Individual integrated circuit parts are available which have been diffused in isolation regions using the same diffusion schedules as the ultimate integrated circuit. Therefore they exhibit the same characteristics as the corresponding parts of completed integrated circuits. The data sheets for these parts and the design rules presented in the following sections enable the designer to determine the performance of each element in an integrated circuit prior to its fabrication. The parts are described in Section 3, and some design rules are listed in Section 4.

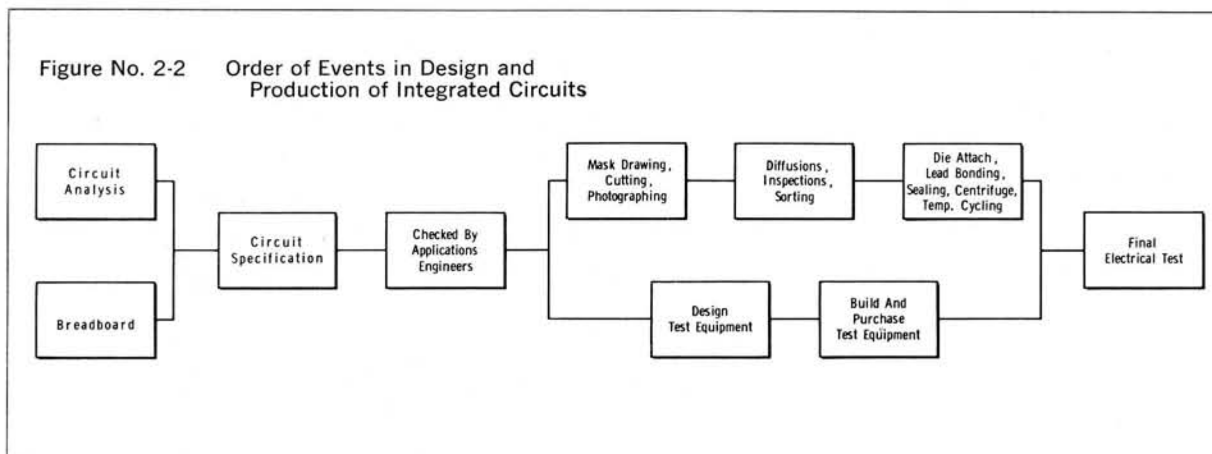
A circuit using conventional parts employs combinations of resistors, transistors, capacitors, etc. which have been individually screened from production runs on the basis of performance. The parts of an integrated circuit obviously cannot be selected in such a manner. Therefore a rigorous analysis of the static conditions of the circuit using the normal range of production tolerances is mandatory to insure circuit operation within the expected parameter distributions. Measurement of static conditions using single integrated circuit parts is not practical because it does not account for the overall distributions which will be encountered. Moreover, it is difficult to select parts to represent all worst case conditions. Therefore a worst case analytical design considering performance requirements and ranges of expected parameter values is necessary for static conditions.

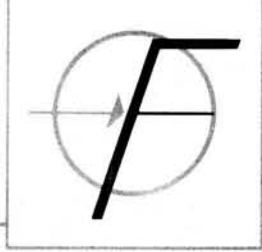
On the other hand, the dynamic characteristics cannot accurately be determined analytically because the equivalent electrical models for the parts are complex (see Section 3). However, the integrated circuit parts are nearly exact models for dynamic considerations. Breadboards of the circuit using these parts have repeatedly predicted the dynamic performance of the integrated circuit with good accuracy. Examples of integrated circuit designs are given in Section 5.1 and 5.2.

When the circuit configuration has been finalized by analysis and breadboard, a functional specification is written. An example of this is given in Section 6. The specification and circuit design are given to application engineers who check the analysis and the breadboard to aid in optimizing production yield. When the schematic and specification are agreed upon, two development programs, parallel in time, are started. This is illustrated in Figure 2-2.

One program is initiated in Production, where mask drawings are made corresponding to the circuit which has been designed and breadboarded. The masks are then cut and photographed to produce a set of plates which are used to mask the areas on the silicon wafers. When all diffusion and metal deposition processes are completed, the dice are scribed from the wafer, sorted electrically, and optically inspected. Those which function electrically are attached to metal headers or placed on a ceramic preform, depending on the package desired. Leads are bonded to the die, and the package is hermetically sealed. After temperature cycling and centrifuge, the integrated circuits are again tested electrically. They are now ready for final electrical classification test.

During the time that mask making and circuit production occur, the equipment for final electrical testing is designed, components purchased, and equipment assembled. This is not a small part of the total effort because the test equipment must be complete, accurate, and easy to use so that minimum time is consumed in testing each circuit. The circuits which pass the final electrical test are marked, tested for hermetic seal, and then shipped to the customer.





FAIRCHILD SEMICONDUCTOR

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TENTATIVE SPECIFICATIONS

μE T-1

NOVEMBER 1962

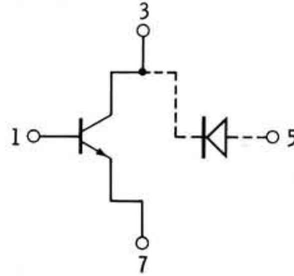
FAIRCHILD DIFFUSED SILICON INTEGRATED CIRCUIT TRANSISTOR

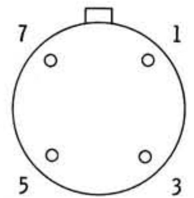
μET-1 is an NPN silicon planar* transistor intended for use in integrated circuit breadboards. It has very small junction capacitances, and is designed for high speed, low power applications. It is manufactured by the Fairchild Micrologic Process to ensure that it will be representative of transistors in the final integrated circuit.

Note: μET-1 must always be incorporated into circuits with the isolation diode terminal (Pin 5) committed.

*Planar: A patented Fairchild process

PHYSICAL DIMENSIONS in accordance with JEDEC (TO-33) outline





PIN NUMBERING BOTTOM VIEW

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures

Storage Temperature	-65°C to +150°C
Operating Case Temperature	+125°C Maximum
Lead Temperature (Soldering - 3 minute time limit)	+300°C Maximum

Maximum Power Dissipation

The total power dissipation of any circuit incorporating μET-1 must not exceed 500 milliwatts

Maximum Voltages

V_{CIO}	Collector to Isolation Voltage	12 Volts
V_{CBO}	Collector to Base Voltage	12 Volts
V_{CEO}	Collector to Emitter Voltage (Note 2)	12 Volts
V_{EBO}	Emitter to Base Voltage	5.0 Volts

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)(Note 4)

Symbol	Characteristics	10th Percentile	Typical	90th Percentile	Units	Test Conditions	
h_{FE}	DC Current Gain (Note 5)	40	80	160		I_C = 3.0 mA	V_{CE} = 5.0 V
V_{BE}(sat)	Base Saturation Voltage	.70	.75	.80	Volts	I_C = 3.0 mA	I_B = 0.3 mA
V_{CE}(sat)	Collector Saturation Voltage		.25	.35	Volts	I_C = 3.0 mA	I_B = 0.3 mA
h_{fe}	High Frequency Current Gain f = 100 mc (Note 3)	3.0	3.8			I_C = 3.0 mA	V_{CE} = 5.0 V
C_{ob}	Output Capacitance		3.3	4.5	pf	I_E = 0	V_{CB} = 5.0 V
C_{TE}	Emitter Transition Capacitance		2.3	3.5	pf	I_C = 0	V_{EB} = 0.5 V
C_{CI}	Isolation Capacitance		8.5	12	pf	I_E = 0	V_{CI} = 5.0 V
BV_{CIO}	Collector to Isolation Breakdown Voltage	12			Volts	I_C = 0.01 mA	I_B = I_E = 0
BV_{CBO}	Collector to Base Breakdown Voltage	12			Volts	I_C = 0.01 mA	I_E = 0
V_{CEO}(sust)	Collector to Emitter Sustaining Voltage (Pulsed)(Note 2)	12			Volts	I_C = 10 mA	I_B = 0
BV_{EBO}	Emitter to Base Breakdown Voltage	5.0			Volts	I_C = 0	I_E = 0.01 mA
τ_s	Charge Storage Time Constant (Note 3)		12		nsec	I_C = I_{B1} = I_{B2} = 5.0 mA	
t_{pd}	Propagation Delay		9.0		nsec	I_C = 2.0 mA	V_{CE} = 5.0 V
I_{CBO}	Collector Cutoff Current		0.5	500	nA	I_E = 0	V_{CB} = 10 V
I_{CBO}(125°C)	Collector Cutoff Current		0.3	5.0	μA	I_E = 0	V_{CB} = 10 V
I_{CIO}	Collector to Isolation Leakage Current		15	1000	nA	I_E = 0	V_{CI} = 10 V
I_{CIO}(125°C)	Collector to Isolation Leakage Current		10	50	μA	I_E = 0	V_{CI} = 10 V
I_{EBO}	Emitter Cutoff Current		2.0		nA	I_C = 0	V_{EB} = 3.0 V

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NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) Ratings refer to a high current point where collector-to-emitter voltage is lowest.

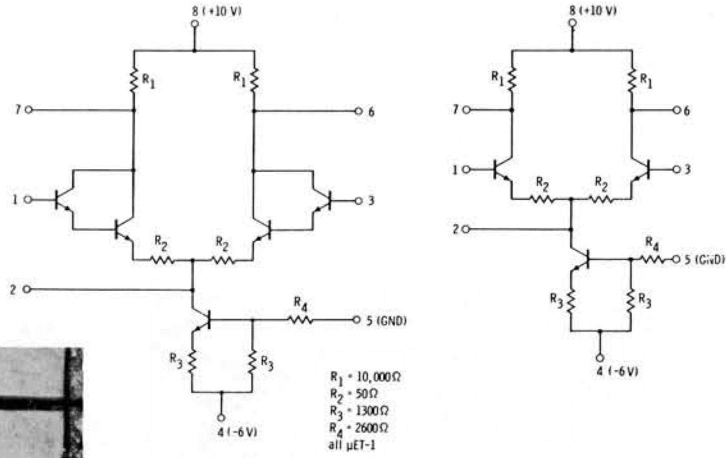
(3) The isolation diode terminal (Pin 5) is tied to the emitter for these measurements.

(4) The 90th and 10th percentiles given on this data sheet are representative and may vary for any given run.

(5) Pulse Width = 300 μsec; Duty Cycle = 1%.

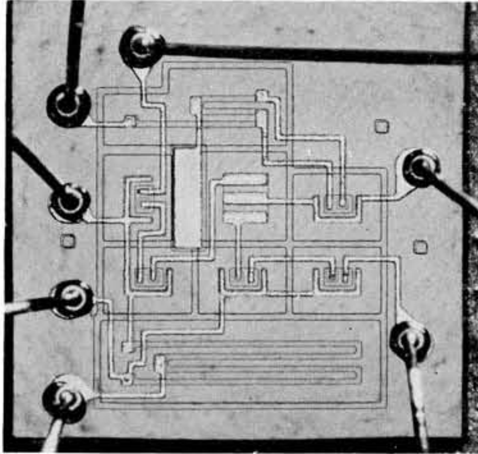
EXAMPLES OF CUSTOM INTEGRATED CIRCUITS

1. Differential Amplifier



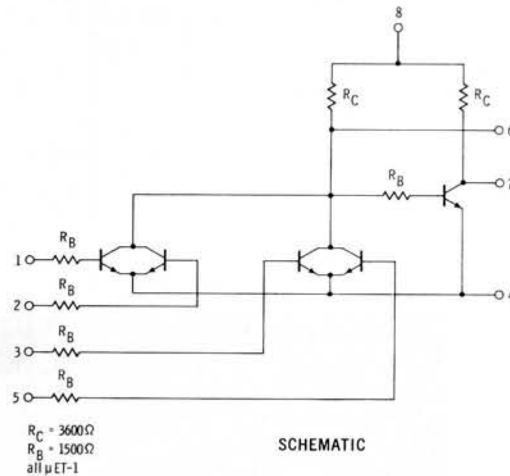
DARLINGTON INPUT

CONVENTIONAL INPUT

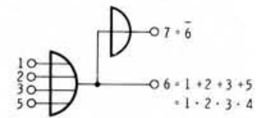


Output Offset	±500mV (max)
CMRR	-90db (typ)
Differential Gain (Darlington)	40 (min)
Differential Gain (Conventional)	50 (min)
Specifications (25°C)	

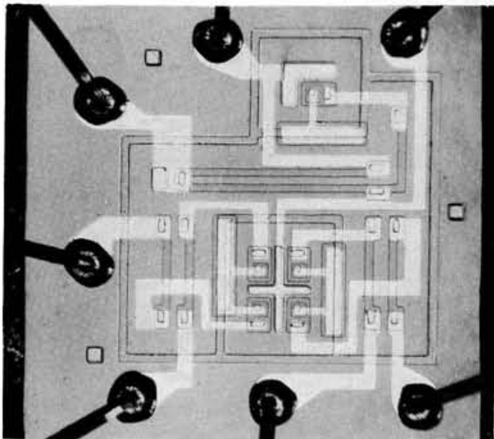
2. Low Power, Four-Input Gate and Inverter



SCHEMATIC

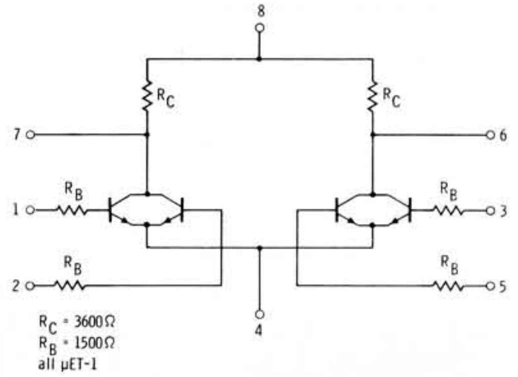


BLOCK DIAGRAM



Propagation Delay/Node	40 nsec (typ)
Fanout/Node	5 (min)
Power Dissipation	4 mw (typ)
Specifications (3V., 25°C)	

3. Low Power, Double Two-Input Gate



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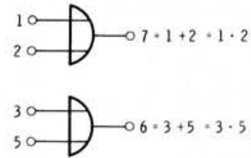

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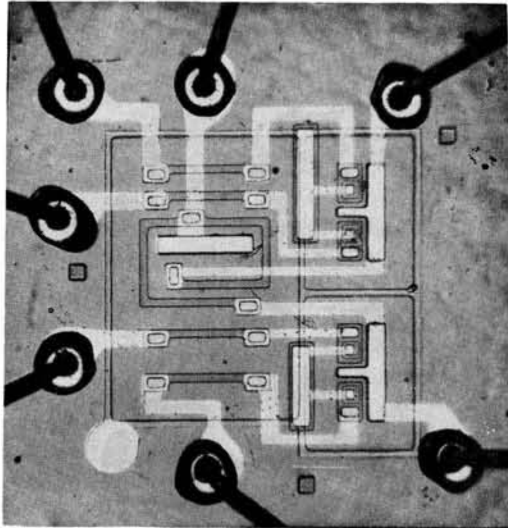
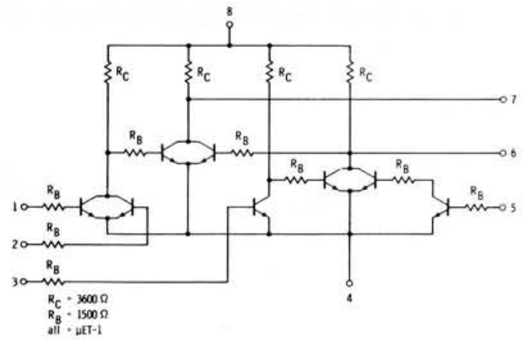


Propagation Delay	40 nsec (typ)
Fanout	5 (min)
Power Dissipation/Node	2 mw (typ)
Specifications (3V., 25°C)	

4. Low Power Adder



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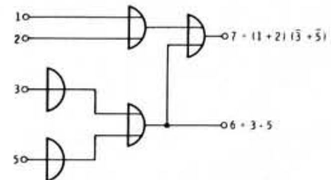

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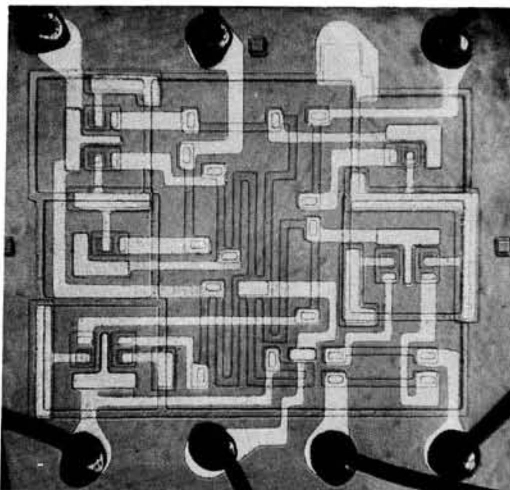

Propagation Delay/Node	40 nsec (typ)
Fanout/Node	5 (min)
Power Dissipation	9mw (typ)
Specifications	