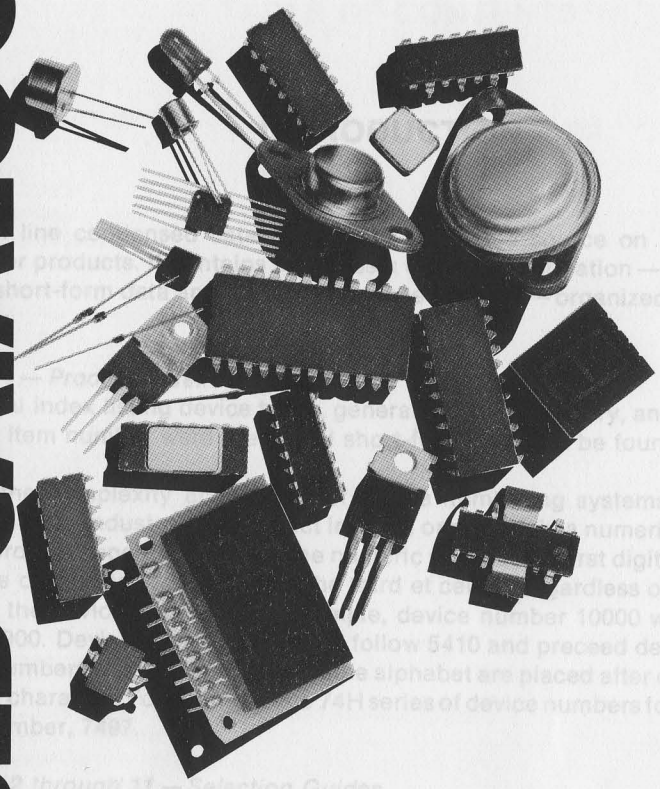
FULL LINE CONDENSED CATALOG

FAIRCHILD

$4.00

FULL LINE CONDENSED CATALOG



FAIRCHILD

464 Ellis Street, Mountain View, California 94042

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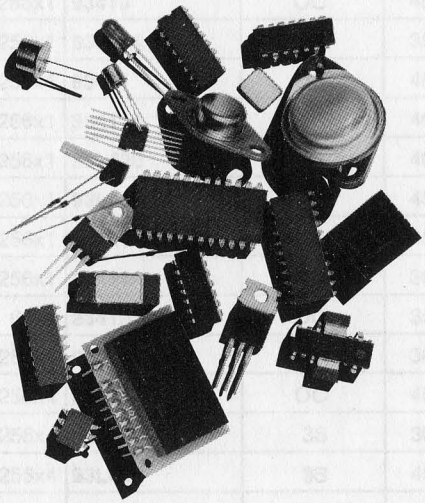

RANDOM ACCESS MEMORIES

BIPOLAR RAMs

Item	Organization	DEVICE NO.	Description[1]	Address Access Time ns (Typ)	Chip Select Access Time ns (Typ)	Read/Write Cycle Time		Power Dissipation mW (Typ)	Logic/Connection Diagram	Package(s)
						Comm 0°C to +70°C ns (Max)	-55°C to +125°C ns (Max)			
TTL										
1	16x4	**54LS/74LS89**[4]	OC	—	—	—	—	—	M1	4L,7B,9B
2	16x4	**54LS/74LS189**[4]	3S	—	—	—	—	—	M1	4L,7B,9B
3	16x4	**54LS/74LS289**[4]	OC	—	—	—	—	—	M1	7B,9B
4	16x4	**7489**	OC	30	30	60/55	60/55	—	M1	4L,7B,9B
5	16x4	**9410**	3S	35	25	50[2]	—	375	M50	7D,9M
6	256x1	**93410**	OC	45	25	60/45	70/55	450	M2	4B,6F,9B
7	256x1	**93410A**	OC	35	20	45	—	450	M2	6D,9B
8	256x1	**93411**	OC	45	25	55/45	65/55	475	M3	4B,6D,9B
9	256x1	**93411A**	OC	40	25	45	—	475	M3	6D,9B
10	256x1	**93L420**	3S	40	20	45	55	250	M3	4B,6D,9B
11	256x1	**93L421**	3S	45	30	90/75	100/90	275	M3	4B,6D,9B
12	256x1	**93421**	3S	35	20	50/35	60/45	475	M3	4B,6D,9B
13	256x1	**93421A**	3S	30	20	40/35	—	475	M3	6D,9B
14	64x9	**93419**	OC	35	15	45	60	725	M4	7Y
15	256x4	**93412**	OC	30	20	45	60/55	475	M5	4K,4R,8T
16	256x4	**93L412**	OC	45	20	60	75/70	250	M5	4K,4R,8T
17	256x4	**93422**	3S	30	20	45	60/55	475	M5	4K,4R,8T
18	256x4	**93L422**	3S	45	20	60	75/70	250	M5	4K,4R,8T
19	1024x1	**93415**	OC	30	15	45	60	475	M6	4B,6D,9B
20	1024x1	**93L415**	OC	35	20	60	70	200	M6	4B,6D,9B
21	1024x1	**93415A**	OC	25	15	30	—	475	M6	6D,9B

1. OC = open collector, 3S = 3-state
2. Measured @ $T_A = 25°C$
3. Typical Data In to Match Out
4. To be announced

RANDOM ACCESS MEMORIES

BIPOLAR RAMs (Cont'd)

Item	Organization	DEVICE NO.	Description[1]	Address Access Time ns (Typ)	Chip Select Access Time ns (Typ)	Read/Write Cycle Time 0°C to +70°C ns (Max)	Read/Write Cycle Time -55°C to +125°C ns (Max)	Power Dissipation mW (Typ)	Logic/Connection Diagram	Package(s)
TTL										
1	1024x1	**93425**	3S	30	15	45	60	475	M6	4B,6D,9B
2	1024x1	**93L425**	3S	35	20	60	70	200	M6	4B,6D,9B
3	1024x1	**93425A**	3S	25	15	30	—	475	M6	6D,9B
4	4096x1	**93470**	OC	30	15	50/55	60/70	800	M15	7D,9M
5	4096x1	**93471**	3S	30	15	50/55	60/70	800	M15	7D,9M
6	4096x1	**93481**	Dynamic, 3S	90	35	120	—	45/350	M16	4B,6E,9B
7	4096x1	**93481A**	Dynamic, 3S	80	35	100	—	45/350	M16	4B,6E,9B
ECL										
8	4x4	**100142**	—	2.7	—	3.3[3]	—	730	M40	4Q,6Q
9	16x4	**95400**	—	14	6.5	17.5/25.5[2]	—	435	M13	6B
10	16x4	**10145A**	—	6.5	4.5	9.0/10[2]	—	500	M14	4L,6B,9B
11	16x4	**100145A**	—	4.8	—	—	—	765	M41	4Q,6Q
12	128x1	**10405**	—	12	5.0	15[2]	—	475	M7	4B,6D
13	256x1	**10410**	—	18	7.0	30/38[2]	—	475	M8	4B,6D,9B
14	256x1	**10411**	—	20	7.0	35/47[2]	—	360	M8	6D,9B
15	256x1	**10414**	—	7.0	4.0	—	—	450	M8	4B,6D
16	256x1	**100414**	—	7.0	4.0	—	—	500	M8	4B,6D
17	1024x1	**10415**	—	25	7.0	35/38[2]	—	475	M9	4B,6D
18	1024x1	**10415A**	—	12	5.0	20/27[2]	—	475	M9	4B,6D
19	1024x1	**100415**	—	12	5.0	20/30[2]	—	500	M9	4Q
20	4096x1	**10470**	—	25	10	—	—	900	M15	7D

1. OC = open collector, 3S = 3-state
2. Measured @ T_A = 25°C
3. Typical Data In to Match Out
4. To be announced

RANDOM ACCESS MEMORIES

MOS/CMOS RAMs

Item	Organization	DEVICE NO.	Description	Access Time ns (Max)	Cycle Time ns (Min)	Power Dissipation mW (Max)	Temperature[1]	No. of Pins	Logic/Connection Diagram	Package(s)
MOS										
1	1024x1	**21L02H**	Static	250	250	158/24[4]	C	16	M22	6Z,8K,8U,9B
2	1024x1	**21L02F**	Static	350	350	158/24[4]	C	16	M22	6Z,8K,8U,9B
3	1024x1	**21L021**	Static	450	450	158/24[4]	C	16	M22	6Z,8K,8U,9B
4	1024x1	**21L022**	Static	650	650	158/24[4]	C	16	M22	6Z,8K,8U,9B
5	1024x1	**2102LH**	Static	250	250	158[2]/220[3]	C,L,M	16	M22	6Z,8K,8U,9B
6	1024x1	**2102LF**	Static	350	350	158[2]/220[3]	C,L,M	16	M22	6Z,8K,8U,9B
7	1024x1	**2102L1**	Static	450	450	158[2]/220[3]	C,L,M	16	M22	6Z,8K,8U,9B
8	1024x1	**2102L2**	Static	650	650	158[2]/220[3]	C,L,M	16	M22	6Z,8K,8U,9B
9	1024x1	**2102H**	Static	250	250	289[2]/385[3]	C,L,M	16	M22	6Z,8K,8U,9B
10	1024x1	**2102F**	Static	350	350	289[2]/385[3]	C,L,M	16	M22	6Z,8K,8U,9B
11	1024x1	**21021**	Static	450	450	289[2]/385[3]	C,L,M	16	M22	6Z,8K,8U,9B
12	1024x1	**21022**	Static	650	650	289[2]/385[3]	C,L,M	16	M22	6Z,8K,8U,9B
13	1024x1	**3542/2102S**	Static	150	150	289	C	16	M22	6Z,8K,8U,9B
14	1024x1	**3542A/2102R**	Static	200	200	289	C	16	M22	6Z,8K,8U,9B
15	256x8	**3539**	Static	650	650	500	C	22	M23	6V
16	256x8	**35392**	Static	500	500	500	C	22	M23	6V

1. C = Commercial temperature range; L = Limited military temperature range; M = Military temperature range
2. Commercial temperature range
3. Military and limited military temperature range
4. Standby power
5. To be announced
6. Typical value @ V_{DD} = 10V

RANDOM ACCESS MEMORIES

MOS/CMOS RAMs (Cont'd)

Item	Organization	DEVICE NO.	Description	Access Time ns (Max)	Cycle Time ns (Min)	Power Dissipation mW (Max)	Temperature[1]	No. of Pins	Logic/Connection Diagram	Package(s)
MOS										
1	1024x4	**F2114**[7]	Static	200	200	350	C	18	M24	—
2	4096x1	**M40272**	Dynamic	150	320	470/36[4]	C,L	16	M25	8K,8R
3	4096x1	**M40273**	Dynamic	200	375	470/36[4]	C,L	16	M25	8K,8R
4	4096x1	**M40274**	Dynamic	250	375	470/36[4]	C,L	16	M25	8K,8R
5	4096x1	**M40275**	Dynamic	300	430	470/36[4]	C,L	16	M25	8K,8R
6	16,384x1	**F16K3**	Dynamic	200	375	465/20[4]	C	16	M26	6Z,8K,8R
7	16,384x1	**F16K4**	Dynamic	250	410	465/20[4]	C	16	M26	6Z,8K,8R
8	16,384x1	**F16K5**	Dynamic	300	500	465/20[4]	C	16	M26	6Z,8K,8R
CMOS										
9	16x4	**4710B**	Static	95[6]	—	0.4	C,M	18	M42	7D,9M
10	16x4	**4725B**	Static	100[6]	—	0.4	C,M	16	M43	4L,6B,9B
11	256x1	**4720B**	Static	95[6]	—	0.4	C,M	16	M44	4L,6B,9B
12	256x4	**4721B**	Static	240[6]	—	0.7	C,M	22	M45	4K,4M,6V,7I
13	1024x1	**4736B**[5]	Static	320[6]	—	0.7	C,M	16	M46	4L,6B,9B

1. C = Commercial temperature range; L = Limited military temperature range; M = Military temperature range
2. Commercial temperature range
3. Military and limited military temperature range
4. Standby power
5. To be announced
6. Typical value @ V_{DD} = 10V
7. Consult factory for package information

READ ONLY MEMORIES

BIPOLAR ROMs AND PROMs

Item	Organization	DEVICE NO.	Description [1]	Address Access Time ns (Typ)	Chip Select Access Time ns (Typ)	Read Cycle Time		Power Dissipation mW (Typ)	Logic/Connection Diagram	Package(s)
						0°C to +70°C ns (Max)	−55°C to +125°C ns (Max)			
TTL										
1	16x48x8	**93458**	FPLA,OC	25	15	—	—	750	M20	8E,9Y
2	16x48x8	**93459**	FPLA,3S	25	15	—	—	750	M20	8E,9Y
3	256x4	**93457**	ROM,OC	25	12	45	60	425	M17	3D,6D,9B
4	256x4	**93467**	ROM,3S	25	12	45	60	425	M17	3D,6D,9B
5	256x4	**93417**	PROM,OC	25	12	45	60	425	M17	3D,6D,9B
6	256x4	**93427**	PROM,3S	25	12	45	60	425	M17	3D,6D,9B
7	512x4	**93436**	PROM,OC	30	15	50	60	475	M10	3D,6D,9B
8	512x4	**93446**	PROM,3S	30	15	50	60	475	M10	3D,6D,9B
9	512x4	**93431**	ROM,OC	30	15	50	60	475	M10	4B,6D,9B
10	512x4	**93441**	ROM,3S	30	15	50	60	475	M10	4B,6D,9B
11	512x8	**93432**	ROM,OC	35	15	55	70	650	M11	4R,6M,7L,9N
12	512x8	**93442**	ROM,3S	35	15	55	70	650	M11	4R,6M,7L,9N
13	512x8	**93438**	PROM,OC	35	15	55	70	650	M11	4R,6M,7L,9N
14	512x8	**93448**	PROM,3S	35	15	55	70	650	M11	4R,6M,7L,9N
15	1024x4	**93452**	PROM,OC	30	15	55	70	650	M18	8F,9M
16	1024x4	**93453**	PROM,3S	30	15	55	70	650	M18	8F,9M
17	1024x8	**93450**	PROM,OC	30	20	45	60	550	M21	4R,6M,9N
18	1024x8	**93451**	PROM,3S	30	20	45	60	550	M21	4R,7L,9N
19	1024x8	**93454**	ROM,OC	30	20	45	60	550	M12	4R,6M,7L,9N
20	1024x8	**93464**	ROM,3S	30	20	45	60	550	M12	4R,6M,7L,9N
ECL										
21	256x4	**10416**	PROM	15	4.0	25 [2]	—	650	M19	4B,6D
22	256x4	**100416**	PROM	15	4.0	25 [2]	—	650	M19	4B,6D

1. OC = open collector, 3S = 3-state
2. -30°C to +85°C

READ ONLY MEMORIES

MOS/CMOS ROMs, EPROMs AND CHARACTER GENERATORS

Item	Organization	DEVICE NO.	Description	Access Time ns (Max)	Power Dissipation mW (Max)	Temperature [1]	No. of Pins	Logic/Connection Diagram	Package(s)
MOS									
1	64x5x7	**3257**	Character Generator	1000	715	C	24	M28	7M
2	64x7x5	**3258**	Character Generator	800	500	C	16	M29	6Z
3	64x9x7	**3260**	Character Generator	1000	660	C	24	M30	7M
4	512x8	**35141**	ROM	850	580	C	24	M33	7M
5	512x8	**35142**	ROM	1000	580	C	24	M33	7M
6	512x8	**35151**	ROM	600	510	C	24	M33	7M
7	512x8	**35152**	ROM	700	510	C	24	M33	7M
8	1024x8	**F2708**	EPROM	450	800	C,L,M	24	M31	QA
9	1024x8	**F27081**	EPROM	350	800	C,L	24	M31	QA
10	1024x8	**F3508**	ROM	450	330	C	24	M32	7M
11	2048x8	**F3516E**	ROM	450	330	C	24	M34	7M
CMOS									
12	256x8	**4735B**	ROM	152[3]	0.7[3]	C,M	24	M47	4M,6Q,9U

1. C = Commercial temperature range; L = Limited military temperature range; M = Military temperature range
2. To be announced
3. Typical value at V_{DD} = 10V

SERIAL MEMORY

FIFOs, LIFOs AND SHIFT REGISTERS

Item	Organization	DEVICE NO.	Description	Frequency MHz (Max)	Power Dissipation mW (Max)	Temperature[1]	No. of Pins	Logic/Connection Diagram	Package(s)
MOS									
1	32x6	**3348**	Static Shift Register	1.0	150	C	24	M36	7M
2	32x6	**3349**	Static Shift Register	1.0	150	C	16	M37	6Z,8K,9B
3	64x4	**3341**	FIFO	0.7	450/625[2]	C,L,M	16	M38	6Z,8K
4	64x4	**3341A**	FIFO	1.0	450	C	16	M38	6Z,8K
5	64x4	**3342**	Static Shift Register	1.5	380	C	16	M35	6Z,8K,9B
6	80x4	**3347**	Static Shift Register	1.5	380	C	16	M35	6Z,8K,9B
7	80x4	**33571**	Static Shift Register	4.0	375	C	16	M35	6Z
8	80x4	**33572**	Static Shift Register	2.0	285	C	16	M35	6Z
9	40x9	**33511**	FIFO	2.0	420	C	28	M39	8E
10	40x9	**35512**	FIFO	1.0	520	C,L,M	28	M39	8E
11	16x4Kx1	**F464-2**	CCD Dynamic Shift Register	1.0-5.0[4]	336/66[3]	C	16	M27	QB
12	16x4Kx1	**F464-3**	CCD Dynamic Shift Register	1.0-4.0[4]	336/66[3]	C	16	M27	QB
13.	16x4Kx1	**F464-4**	CCD Dynamic Shift Register	1.0-2.0[4]	336/66[3]	C	16	M27	QB
CMOS									
14	16x4	**4703B**	FIFO	5.3	0.5	C,M	24	M48	4M,6Q,9U
15	16x4	**4706B**	LIFO	5.3	0.5	C,M	24	M49	4M,6Q,9U
TTL									
16	16x4	**9403**	FIFO	10	850	C,M	24	M51	6Q,9U
17	16x4	**9406**	LIFO	10	800	C,M	24	M52	6Q,9U

1. C = Commercial temperature range; L = Limited military temperature range; M = Military temperature range
2. Military and limited military temperature range
3. Standby power
4. Minimum frequency specification

FAIRCHILD

FULL LINE CONDENSED CATALOG

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