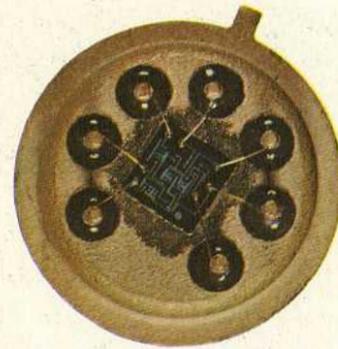
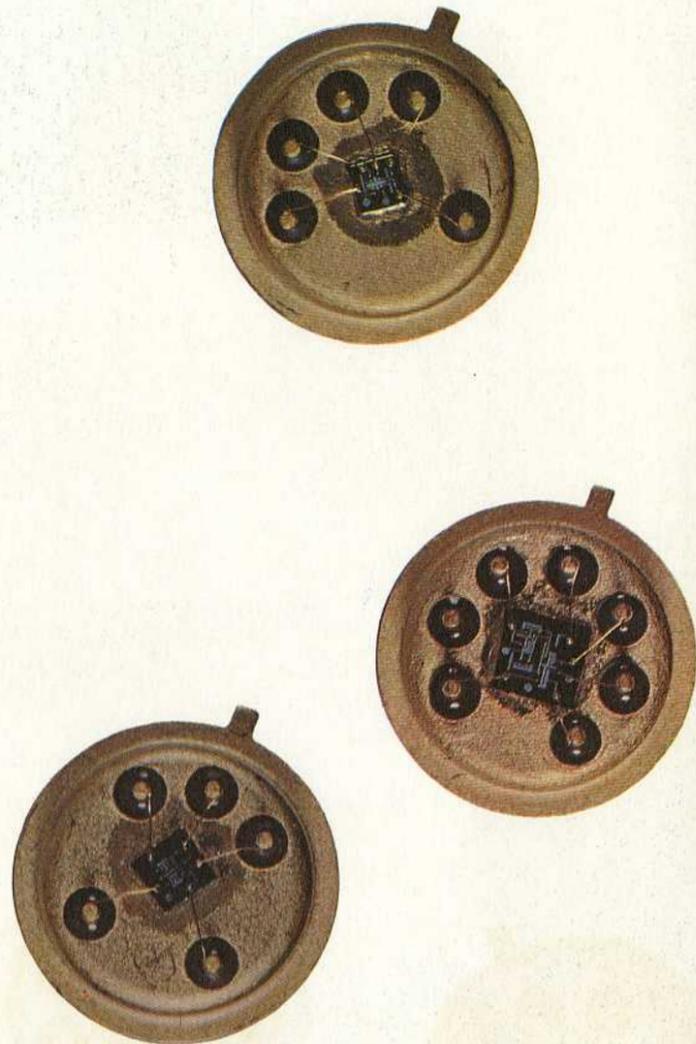


A high-magnification, close-up photograph of a microchip, likely a Fairchild micrologic device. The image shows a circular, metallic-looking structure with a central opening. Inside this opening, there are numerous fine, parallel lines or ridges, possibly representing the internal circuitry or a specific component of the chip. The lighting is dramatic, with a strong orange and yellow glow emanating from the center, creating a sense of depth and highlighting the intricate details of the microchip's surface.

**THE  
INSIDE  
STORY  
ON  
FAIRCHILD  
MICROLOGIC**

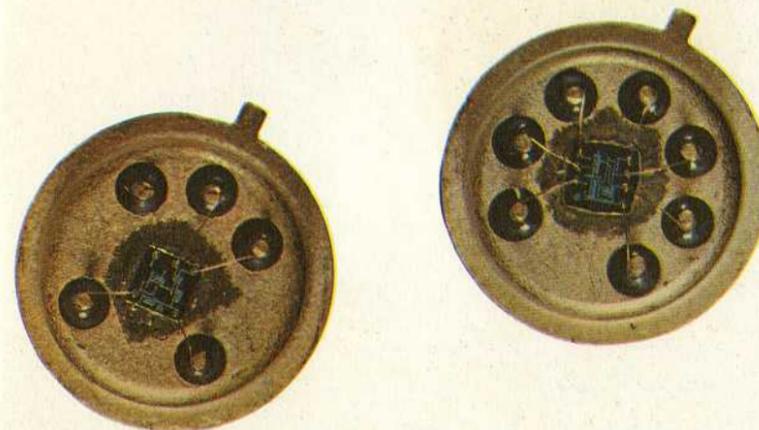


Micrologic elements are a compatible set of miniature logic circuit blocks, each built into a single, monolithic chip of silicon about 1/16 inch square. Micrologic circuits are a modified form of DCTL — direct-coupled transistor logic. DCTL was chosen for five reasons: (1) fewest number of components, (2) fewest kinds of components, (3) non-critical component values, (4) low power consumption, and (5) low supply voltage.

This family of functional elements can be used to fabricate a low cost, highly reliable computer logic section using no other components. They will operate at 1 mc (50 nsec stage delay) clock rates over a temperature range of  $-50^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

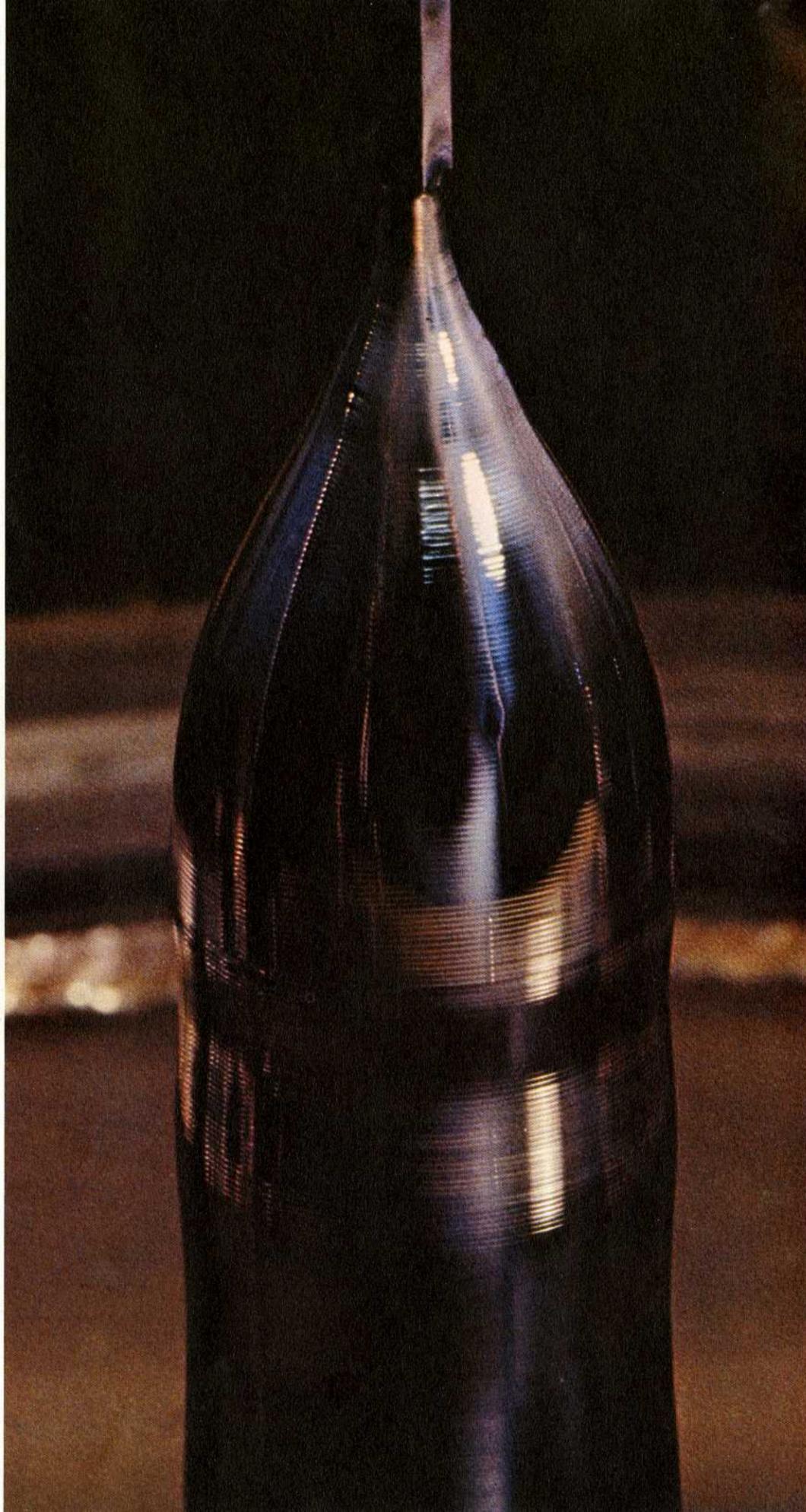
This brochure will guide you through the manufacture of a typical Micrologic element — the Half-Shift Register — from the crystal to final inspection. The story is told for just one reason: it demonstrates Fairchild's production capabilities in the field of integrated circuitry.

**THE  
INSIDE  
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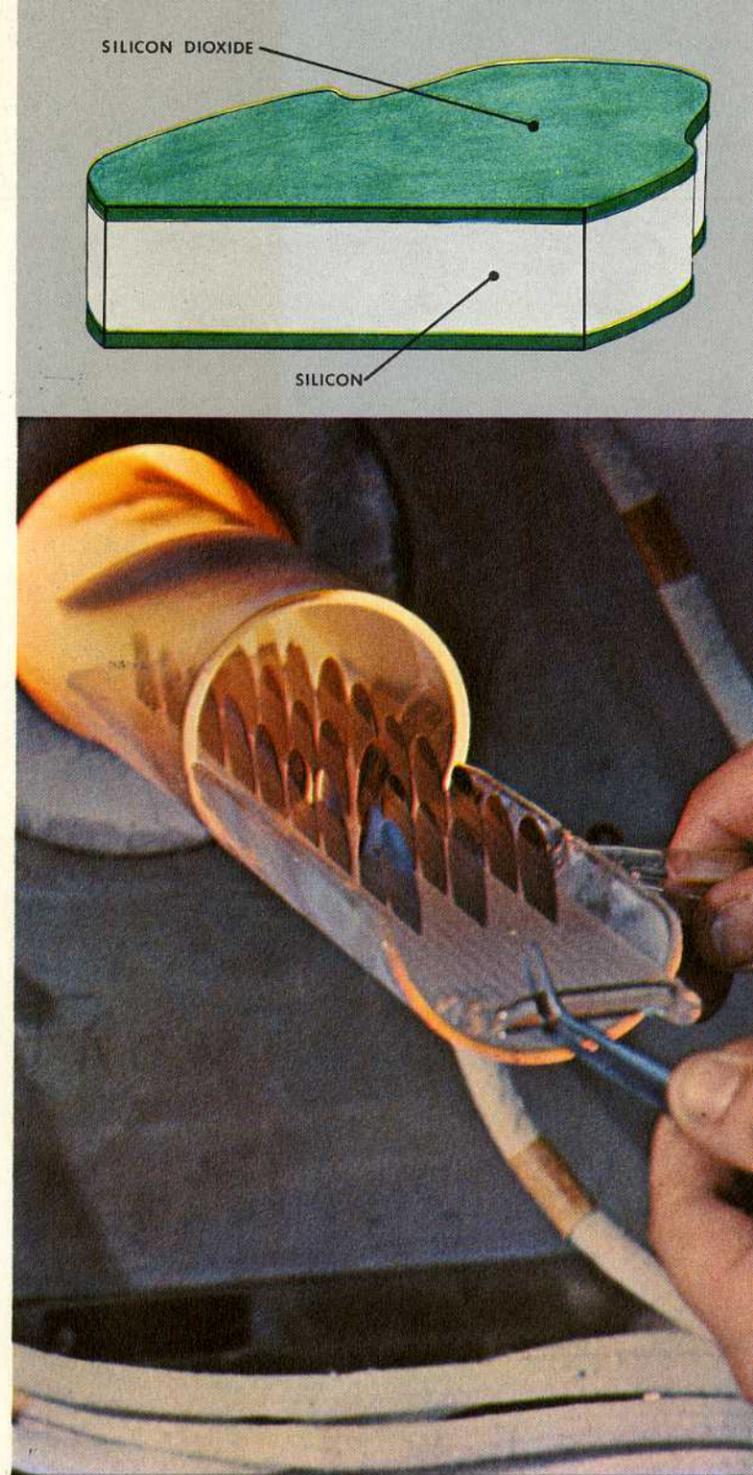
## CRYSTAL GROWING

The starting material for Micrologic elements is the same high-purity silicon which is grown by Fairchild and used in its transistor production. The crystals are carefully selected for low dislocation and imperfection counts of the crystalline structure. The silicon crystals are grown by the Czochralski method: a small perfect seed crystal is lowered into molten silicon, and slowly pulled out to form a crystal about six inches long and one inch in diameter. For Micrologic, the crystal is grown with a phosphorus impurity to make it n-type.



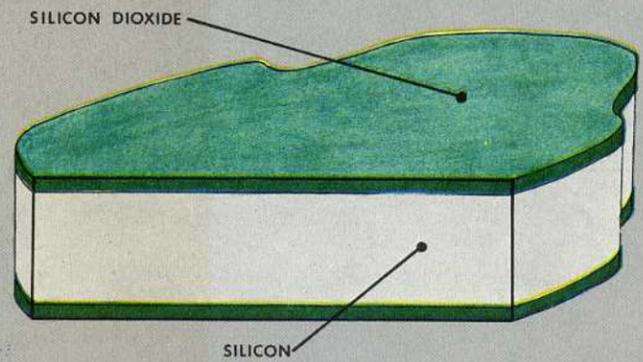
## CUTTING AND LAPPING

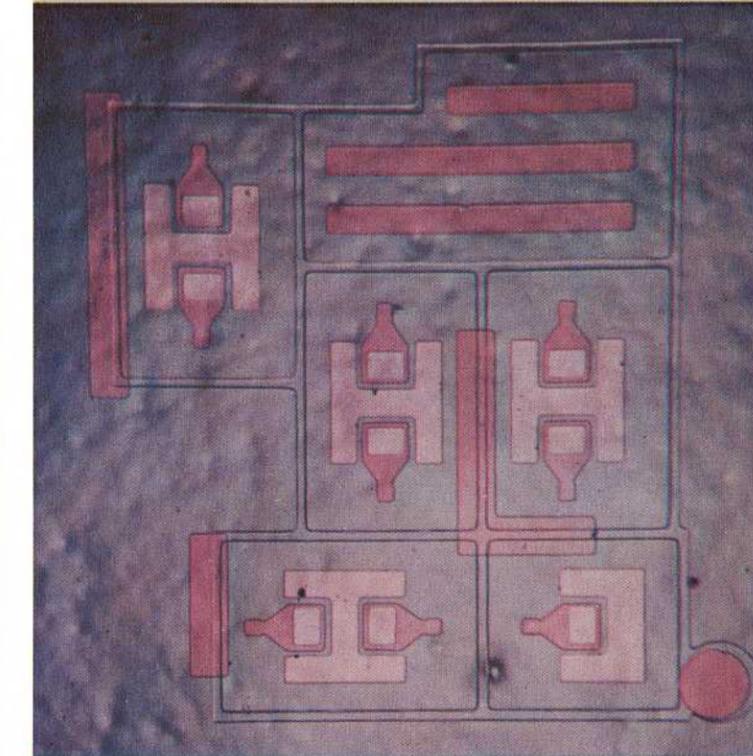
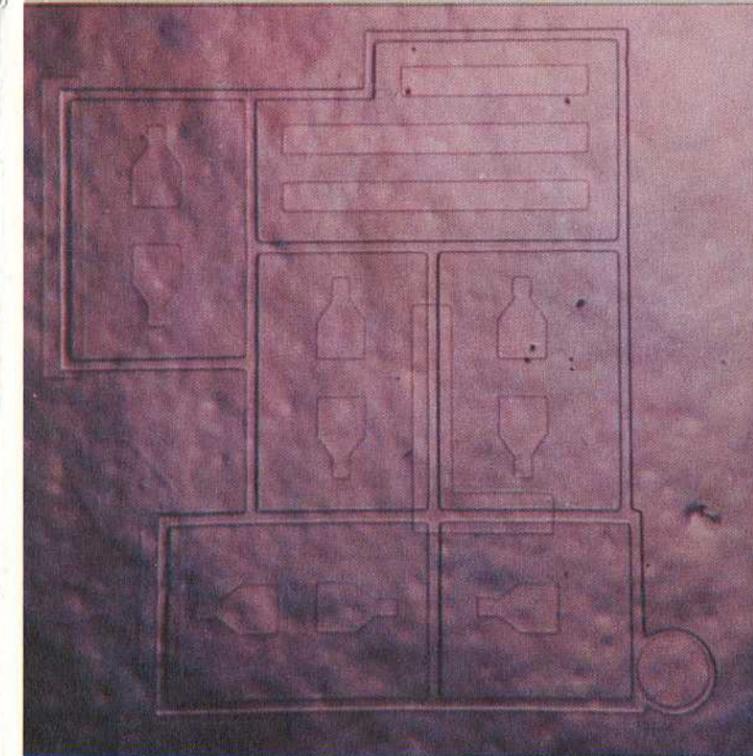
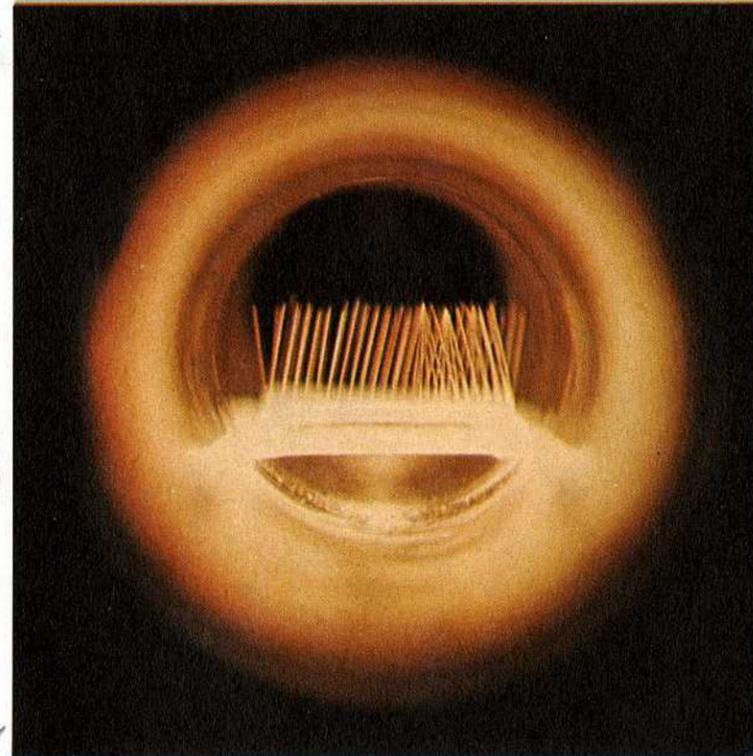
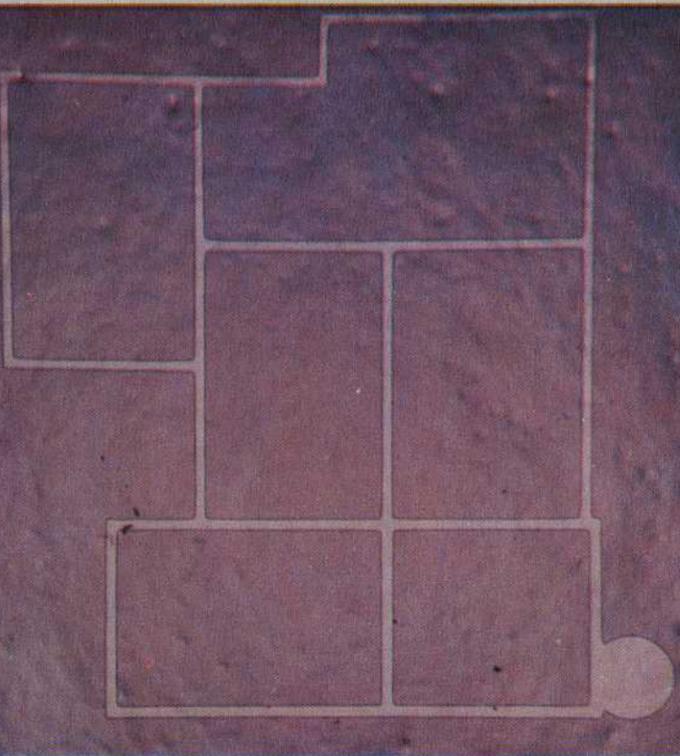
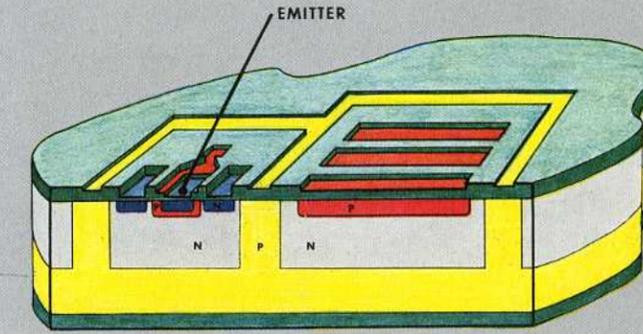
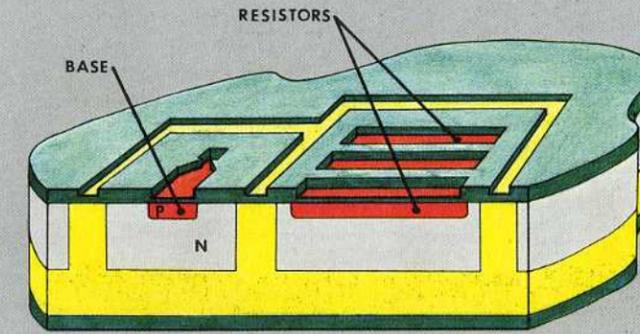
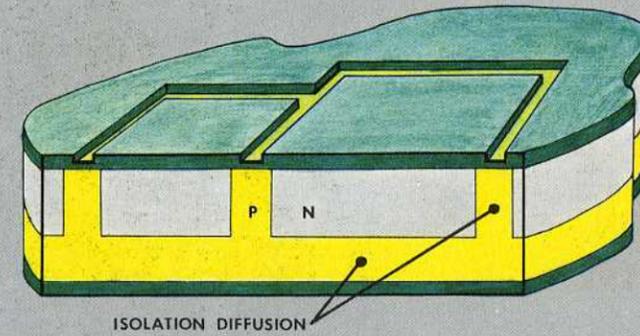
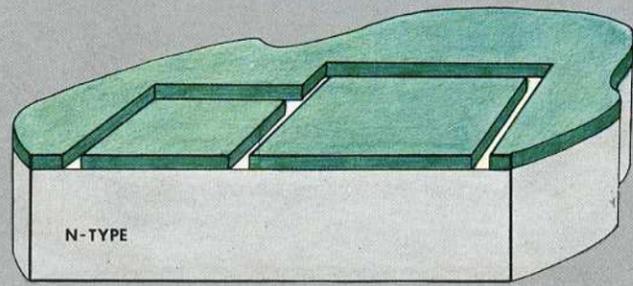
The crystal is sawed into wafers approximately eight thousandths (.008) of an inch thick, using a diamond saw. Each wafer is then lapped flat automatically, using very fine grit abrasive. A chemical etching results in a final thickness of about three thousandths inch (.003), and a smooth shiny surface. These steps are the same as those used in the preparation of Fairchild Planar transistor wafers.



## OXIDE GROWTH

Many wafers of silicon — representing thousands of potential Micrologic elements — are placed into a furnace containing an oxidizing atmosphere at 1200° C. Oxygen penetrates the crystal lattice at the surface of the wafer and combines chemically with these surface silicon atoms to form the inert, stable compound  $\text{SiO}_2$  (silicon dioxide). Through this process, standard at Fairchild, the silicon wafers are virtually encapsulated and the surfaces are passivated. This one step — the beginning of the planar process — is the key to reliability and production economy.





### ISOLATION MASKING

The following steps are performed in order to isolate electrically the individual transistors and resistors from one another. The wafers are coated with a photosensitive material in a darkroom. This material is exposed to light through a high-resolution mask. The portions not exposed are soluble and are easily removed by a solvent rinse. Then, an etch is used to dissolve the silicon dioxide from the areas not protected by the film of photosensitive material. In this way, a thin band, or "windows" surrounding the transistor areas, are photo-engraved through the protective silicon dioxide.

### ISOLATION DIFFUSION

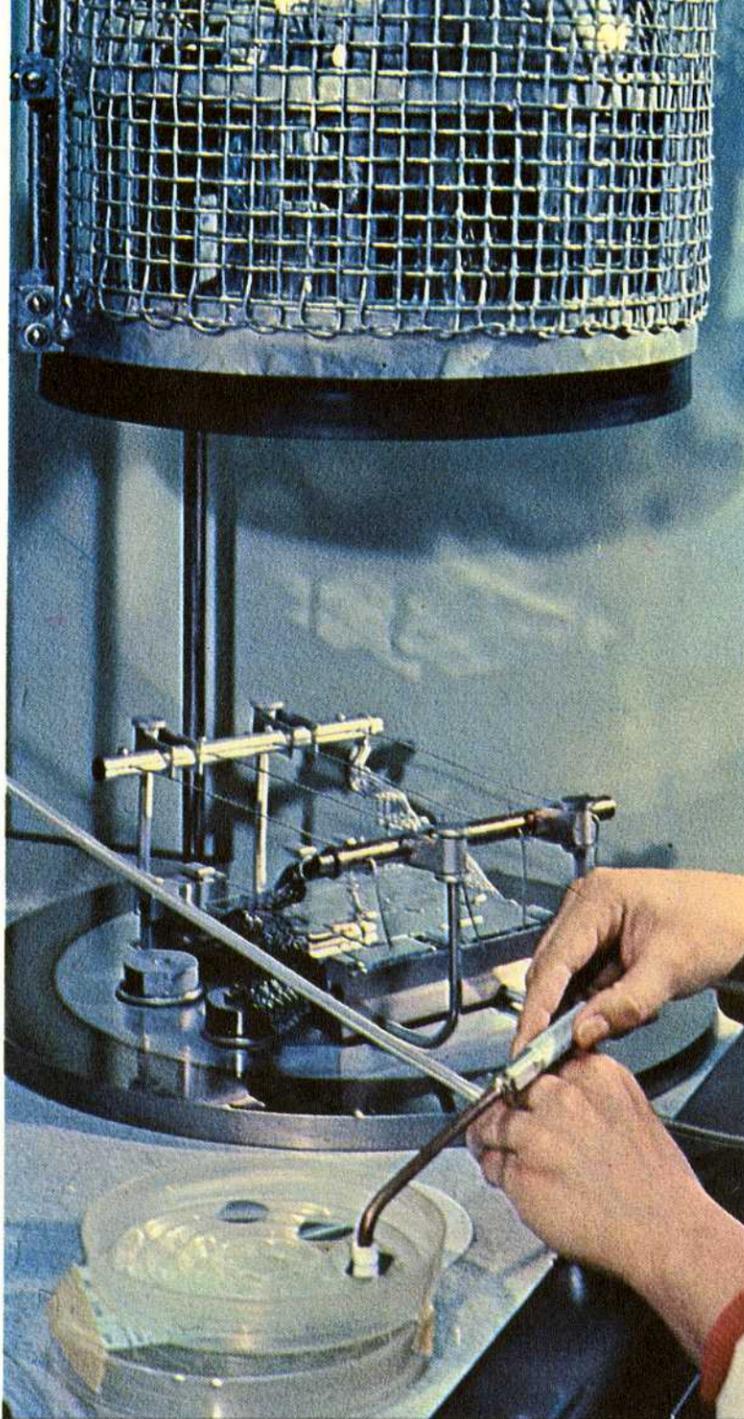
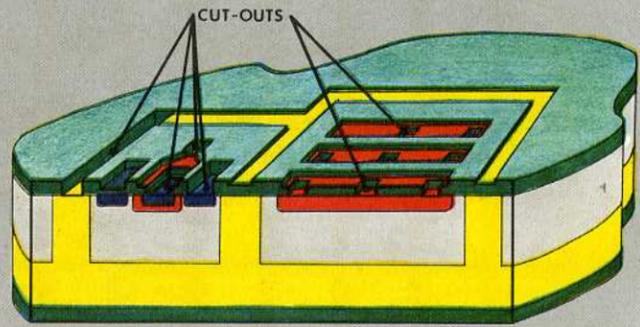
The wafers are placed into a special, high-temperature furnace where the atmosphere contains boron in a gaseous state. The boron impurity diffuses into the surface of the silicon wafer only where it has been exposed by the preceding photo-engraving steps. Even at elevated temperatures the silicon dioxide protects the underlying silicon from the dopants. The temperature is then raised to 1300°C; oxygen is introduced, and the boron impurity diffuses simultaneously from both sides of the wafer to meet in the middle, leaving pockets of the original n-type material which will become the collector regions of the transistors. These regions are separated from one another by the presence of the diffused isolation. In areas where the original silicon dioxide was etched away, a new layer is formed by surface oxidation during the diffusion.

### MASKING AND BASE DIFFUSION

The wafer is again masked and etched for the simultaneous diffusion of the base region and resistors. Once again boron is used as the diffusing impurity in this high-temperature diffusion. The base region is diffused into the n-type starting material to form the collector-base diode of each transistor as well as all the resistors in the circuit. As the diffusion progresses, the oxygen atmosphere in the furnace re-oxidizes the cutout portions of the wafer surface and seals them against contamination or injury. As the diffusion progresses downward into the wafer, it also proceeds laterally, diffusing into the silicon covered by the original protective oxide. The doping level of the base of the Micrologic transistor is very similar to that of standard Fairchild Planar transistors. The resistivity of the diffused area is thus a convenient value for use in the diffused resistors.

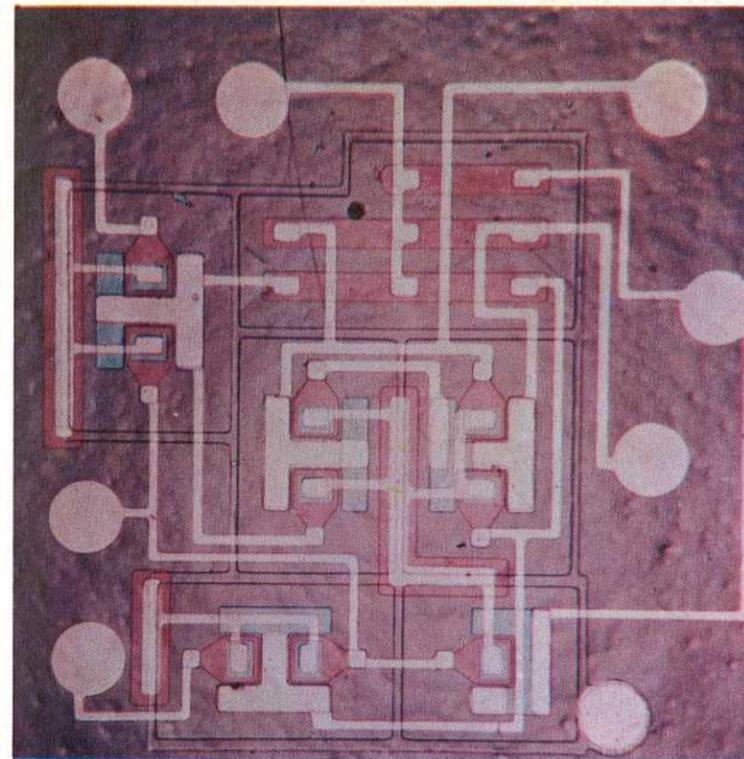
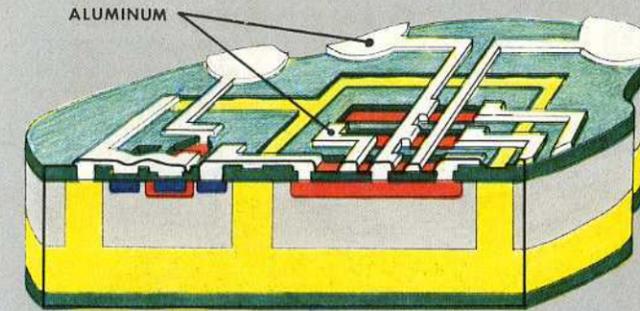
### EMITTER MASKING AND DIFFUSION

Another precisely indexed masking step is performed to remove oxide for the emitter diffusion and for the top-side collector contacts. In another high-temperature step, phosphorus — an n-type impurity — is deposited on the surface. Diffusion then takes place at about 1200°C. Again silicon dioxide forms as the diffusion progresses, covering the photo-engraved area and sealing the surface. Side diffusion carries the junction underneath the protective layer. Notice that in each case the diffused region ends underneath an oxide which existed previously. This oxide permanently protects the actual junctions of the device against exposure to the outside environment.



### METALIZATION

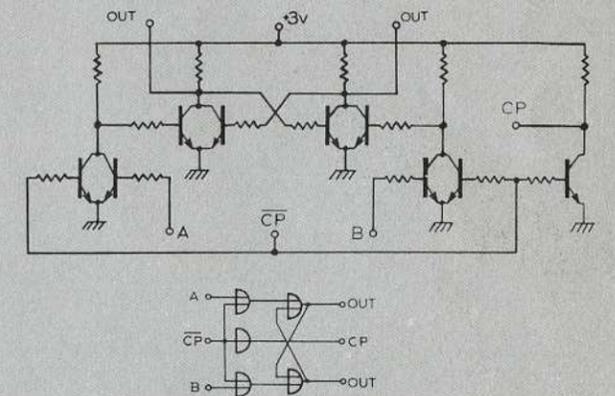
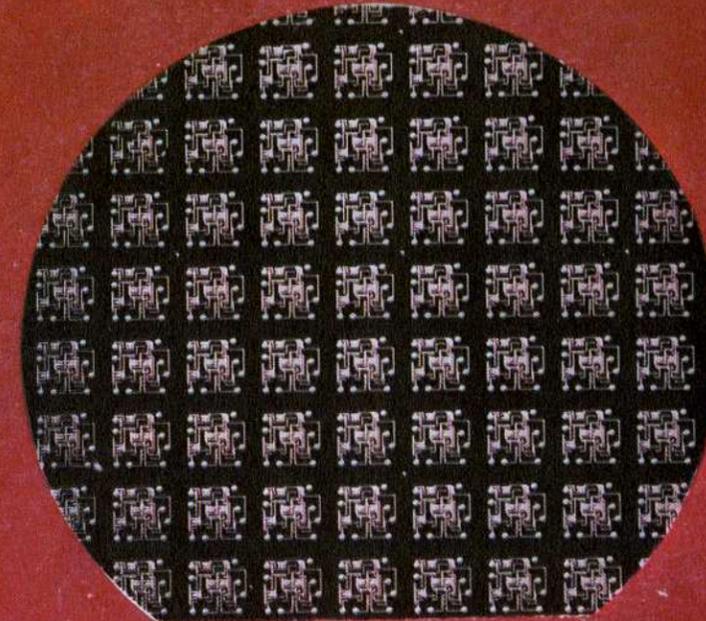
The wafers are now placed into a vacuum chamber. Under high vacuum, aluminum is heated and boiled from a hot tungsten filament. This evaporated metal deposits in a thin, even coat over the entire wafer surface. Many wafers, comprising hundreds of Micrologic units, may be processed at one time in this fashion.



### METAL INTERCONNECTIONS

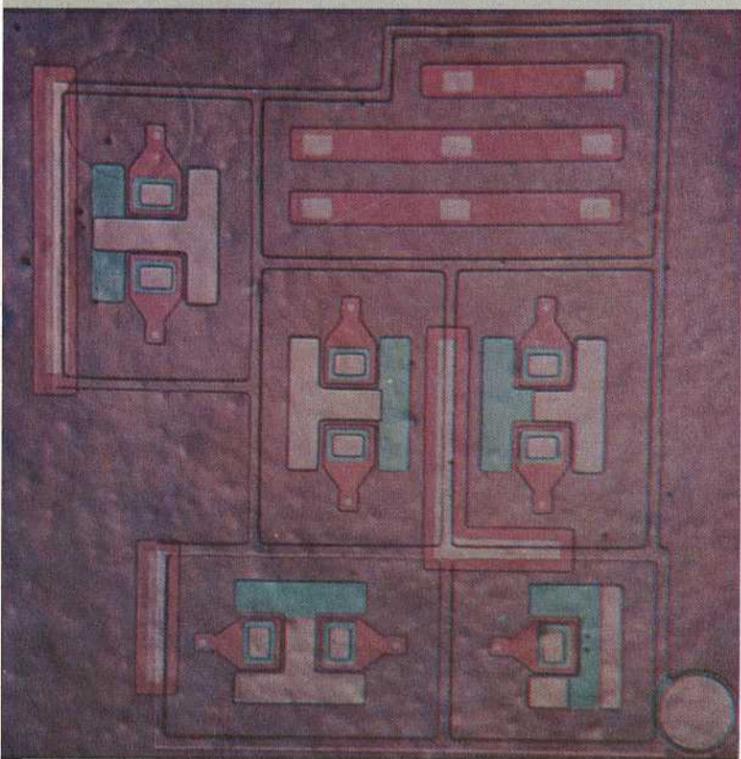
In another precise photo-engraving step, the aluminum layer is masked and selectively etched to leave a pattern of interconnections between transistor and resistor elements in the logic circuit. The Micrologic Half-Shift Register wafer is now complete electrically and needs only to be cut into individual circuits and packaged. Up to this point, all operations have been done on many wafers at a time. The elimination of the handling of each device separately is a major factor in the reduction of production costs. This batch processing also increases the reliability and compatibility of the devices.

Compare the electrical schematic to the color photomicrograph of the finished element. Notice the flip-flop section in the center of the picture, with the metal interconnections from the collector of one side to the base of the other. The collectors of each gate may be seen connected to the base of each flip-flop. All connections to the outside — inputs, outputs, power supply and ground — are brought out to the periphery of the element as large, circular aluminum pads, for easy, reliable connections. The power supply pad on the device may be traced to the center-tap on the 1200 ohm resistor, and from there through 600 ohms to each collector. All emitters have been tied to the isolation, which acts as the common ground.



### EXPOSURE OF CONTACT AREAS FOR INTERCONNECTIONS

At this point the transistors and resistors of the Micrologic circuit are completed. They must now be connected together into the desired logic circuit. This is done by evaporating metal interconnections onto the surface of the silicon wafer. Before this can be done, however, a hole must be photo-engraved over the appropriate regions of the devices so that the evaporated metal can make contact. This is done in a masking step similar to the others.



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