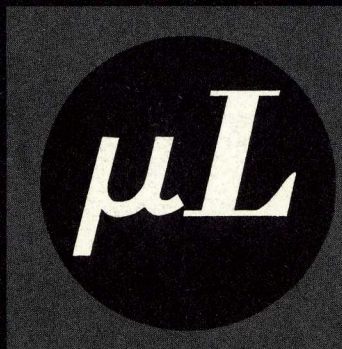
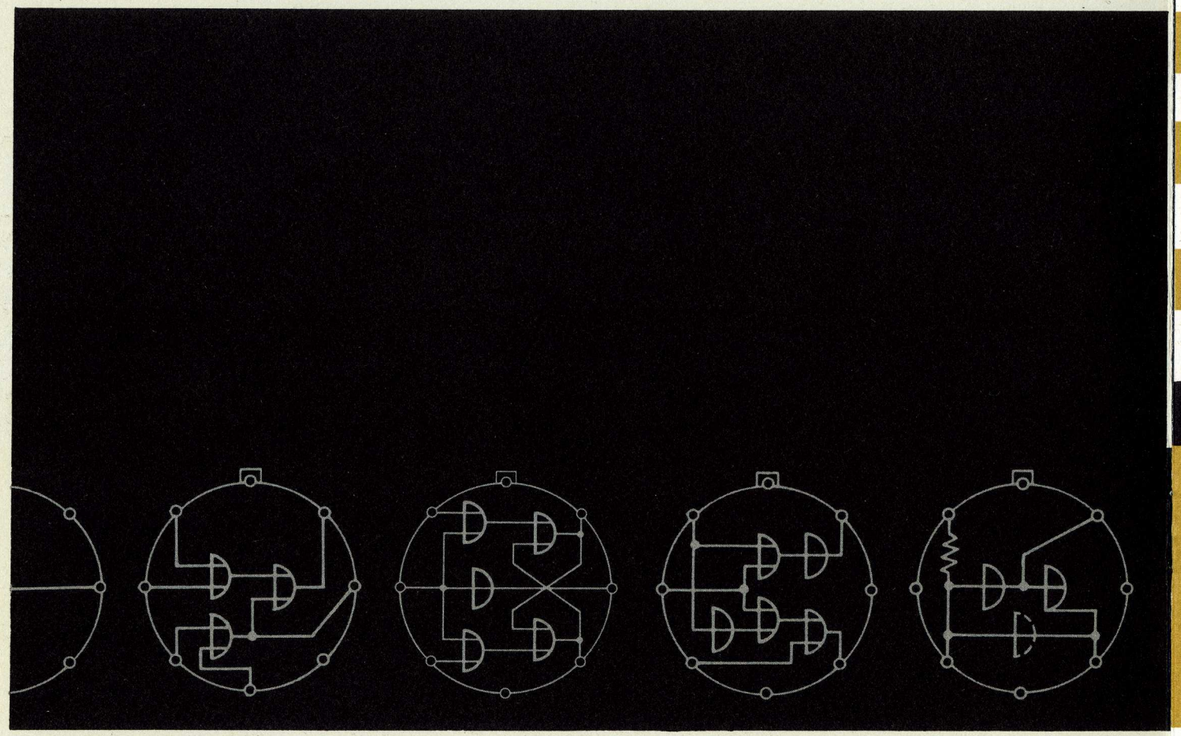
FAIRCHILD SEMICONDUCTOR

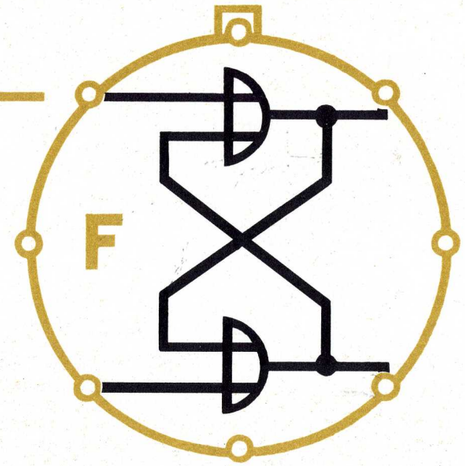


MICROLOGIC

ANNOUNCING THE FIRST OF A FAMILY



THE MICROLOGIC FLIP-FLOP



HIGH SPEED

LOW POWER

LOW COST

COMPATIBLE

MINIATURE

CONVENIENT

NOW AVAILABLE

The first element of the micrologic family of digital functional blocks is now available. The flip-flop, like other members of the family, operates over the full military environment at bit rates above 1 mc.

These integrated semiconductor logic elements are not laboratory curiosities; they are designed to be:

RELIABLE

The new order of reliability inherent in the Fairchild planar process is complemented by the use of deposited metallic film intraconnections.

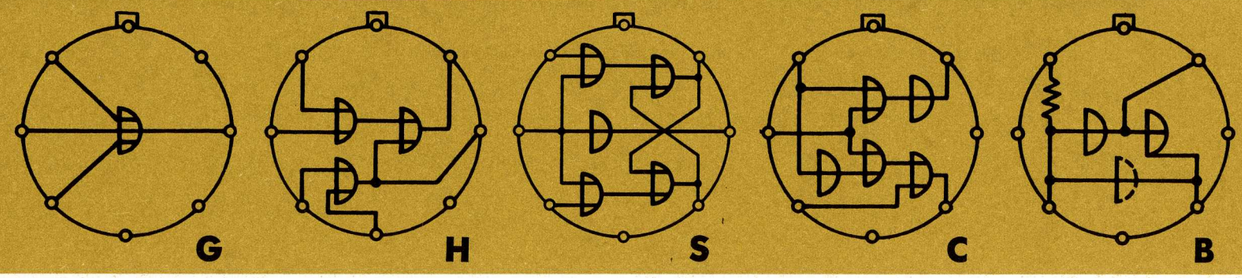
USEFUL

The six elements of the micrologic family are in themselves sufficient to efficiently build the complete logic section of a digital computer or control system. The (TO-5) elements are designed for use with conventional printed circuit boards, the (TO-18) packages for use with welded-wire interconnections.

ECONOMICAL

Low component cost is achieved by use of the batch diffusion process. The logic-function capability and the pin layout of each element are such that the time required for logic design and circuit layout is drastically reduced.

ADDITIONAL TYPES TO COME



THE FIRST OF A FAMILY

Fairchild Semiconductor Corporation announces the first of a family of high-speed, low-power logic building blocks for digital computers. This family is sufficient to handle all the logic-function requirements of a digital machine operating at bit rates in excess of 1 mc ; no other components are required in the logic section of such a machine.

The following elements comprise the family:

"F" Element—Flip-flop
"S" Element—Half-shift Register
"G" Element—Gate
"B" Element—Buffer
"H" Element—Half Adder
"C" Element—Counter Adapter

In both the development and use of these elements emphasis is placed on the logic function to be performed. The elements are characterized in terms familiar to logic design personnel. For these reasons, the term "micrologic" is preferred to the terms "microcircuitry" or "microelectronics" for treating the high-density packaging of digital logic functions.

All elements are packaged in 8-lead JEDEC TO-5 and TO-18 packages. They dissipate an average power of 30 mW, and they operate over a temperature range of —55°C to +125°C, at speeds in excess of 1 mc .

The potential savings which can be realized using micrologic elements over best contemporary single layer (printed circuit board) computer packaging methods can be summarized as follows:

A. Volume—micrologic requires 5% of the volume of contemporary techniques.
B. Power—micrologic requires 25% of the power for the same speed and temperature range (ultimately 1%).
C. Component Cost—the cost of a micrologic element is of the same order as that of the equivalent circuit fabricated by conventional means. This cost will be markedly reduced as production volume increases.
D. Assembly Cost—micrologic elements are handled exactly as transistors and represent a 90% saving in the number of components handled.
E. System Design—the design of a system using micrologic requires only 5% of the time using contemporary techniques (through to the printed master).

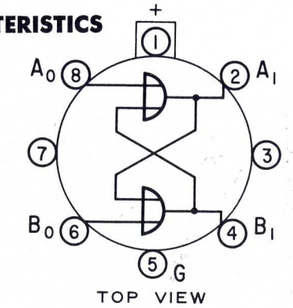
The preceding is expected ultimately to effect a 70-80% reduction in the cost of the logic section to the computer manufacturer.

It should be noted that micrologic elements are being developed as a product line. As a product, they will all be required to meet the same high standards of quality and reliability found in other Fairchild Semiconductor products.

PRELIMINARY CHARACTERISTICS

MICROLOGIC ELEMENT
"F"
FLIP-FLOP

SUPPLY VOLTAGE +3 V DC ±30%
POWER DISSIPATION 30 M W (TYP.)
TEMPERATURE —55°C TO +125°C



TOP VIEW

INPUT (TERMINALS 6, 8)
CAN BE DRIVEN BY ANY MICROLOGIC ELEMENT
1 MICROLOGIC LOAD.

OUTPUT (TERMINALS 2, 4)
CAN DRIVE UP TO 4 OTHER MICROLOGIC ELEMENT LOADS IN PARALLEL.

$\overline{A}_1 = A_0 + B_1$
$\overline{B}_1 = B_0 + A_1$

AVERAGE DELAY—50nsec.

TO OPERATE THE "F" ELEMENT

In normal use, micrologic elements are the only components used in a logic section or data system. If, however, it is desired to operate an individual element for test purposes, a circuit similar to that of Figure 1 can be used.

This circuit simulates micrologic inputs and loads for the "F" element. With an applied 3-volt pulse or square wave, the input 2N708's, representing preceding micrologic stages, generate 200 nsec .8-volt pulses.

Each of the output transistors, with its base resistor, represents one micrologic load. Four such loads may be connected in parallel at each output.

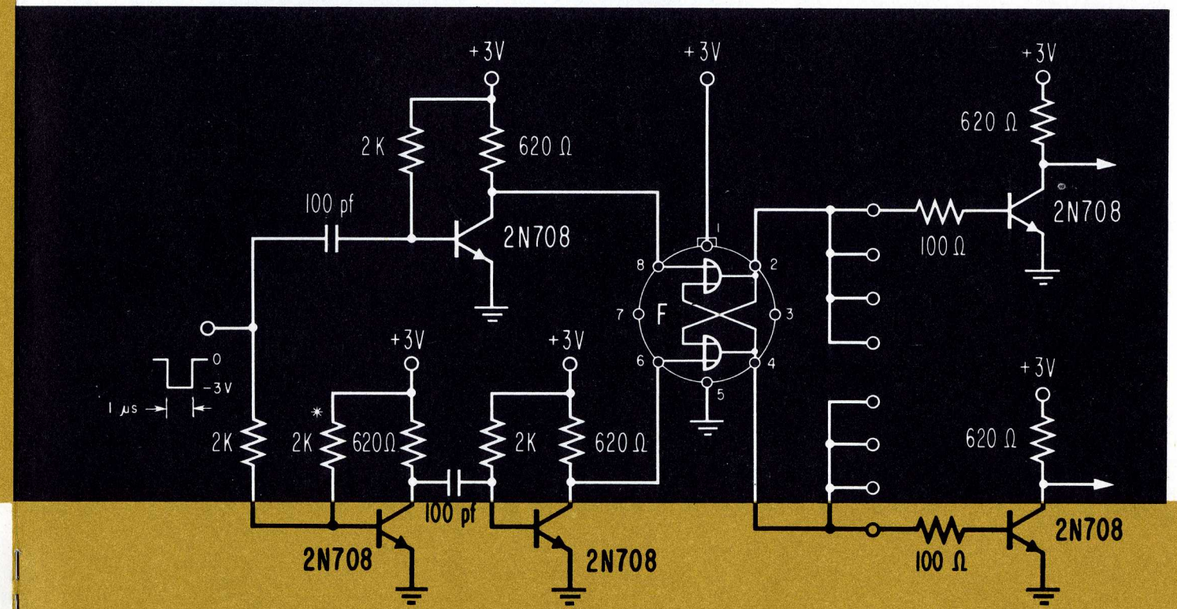


Figure 1

*IF THE INPUT PULSE IS POSITIVE (0 TO +3V), THIS RESISTOR SHOULD BE OMITTED.

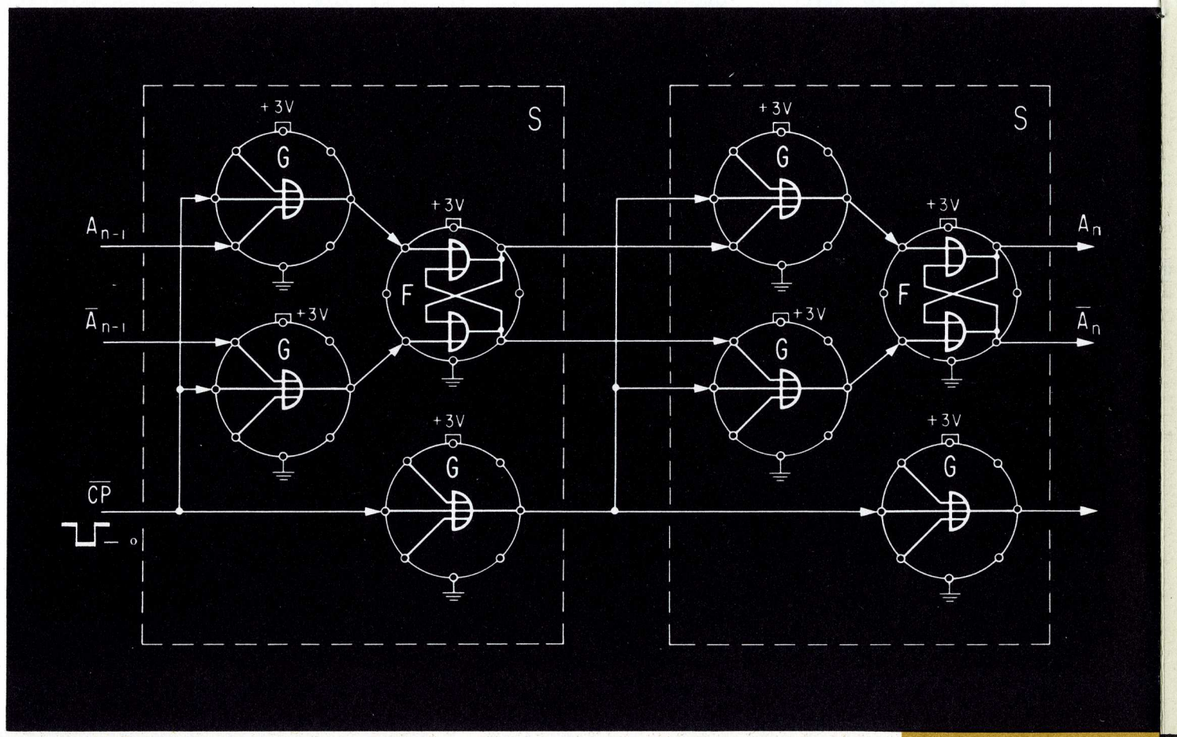
APPLICATION

Micrologic utilizes the two-phase or master-slave flip-flop method of storing bits; it requires, therefore, no delay lines or RC delays. Two "S" elements are used for each shift register or counter stage.

Figure 2 shows the master and slave flip-flops for a one-bit section of shift register, using "F" and "G" elements. This is the equivalent of two "S" elements, as indicated by the dotted lines.

This circuit becomes a binary counter if outputs A_N and $\overline{A}_N$ are connected to inputs $\overline{A}_{N-1}$ and A_{N-1} respectively. Pulses applied at input $\overline{CP}$ will trigger the binary.

Figure 2



REFERENCES:

1. R. Norman, J. Last, I. Haas: "Solid State Micrologic Elements" presented at Solid State Circuits Conference, Feb. 1960.
2. R. Norman: "Status Report on Micrologic Elements," presented at 51st Bumblebee Guidance Panel, June 22, 1960.
3. D. Farina, J. Nall, R. Anderson: "Application of Micrologic Elements" presented at National Electronics Conference, Oct. 10, 1960.
4. R. Norman, R. Anderson: "Testing of Micrologic Elements" to be presented at Western Joint Computer Conference, May 9, 1961.

Reprints of these papers may be obtained from your Fairchild Sales Representative or by writing to Fairchild Semiconductor Corp., ATTN: Micrologic. The WJCC reprint will be available after the conference .

LOGIC DESIGN

The basic logic block of micrologic, and the basic symbol shown in the characteristics, is the NOR gate. As indicated in Figure 3, the NOR output is a "one" only if none of the inputs is a "one". This gate gives the OR function, with inversion, of positive inputs; it generates the AND function when complemented inputs are used.

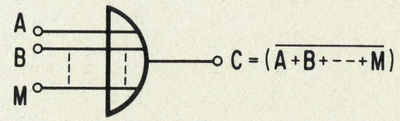


Figure 3

Micrologic utilizes NPN transistors in DCTL configuration; the transistors are of a new type, developed and optimized particularly for use in the micrologic DCTL configuration. A "one" is represented by a positive potential, while "zero" is a near-ground potential.

In working with micrologic the only restrictions that must be borne in mind by the logic designer are those of fan-out, propagation delay, and non-shorted outputs.

The fan-out specification requires that no more than five micrologic loads may be connected to an output node; one "micrologic load" is defined as the base of a transistor whose collector sees a normal fan-in (typically three or less). Certain elements, the flip-flop for example, contain internal loads; the external fan-out is then equal to four. When a greater load-driving capability is required, the buffer—or "B" element—is used. This element drives 25 micrologic loads.

Only in special cases may two output pins be connected together. If the +3V supply is not connected to the node resistors at the outputs of the "G" and "C" elements, these outputs may be connected to the output nodes of other elements; the resultant output is the logical AND function of the individual outputs.

As long as the logic designer operates within the above conditions, he is free to consider micrologic elements as logic-function generators and to interconnect them in any network he desires.

A typical usage of micrologic elements is illustrated in Figure 4. Here six elements comprise a serial full adder.

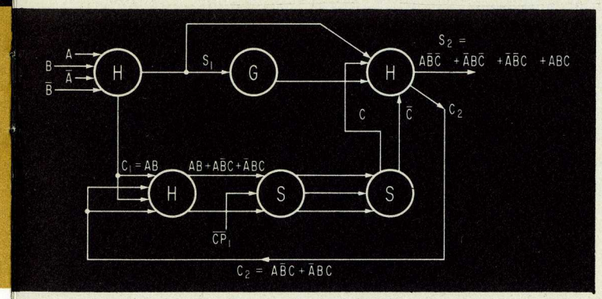
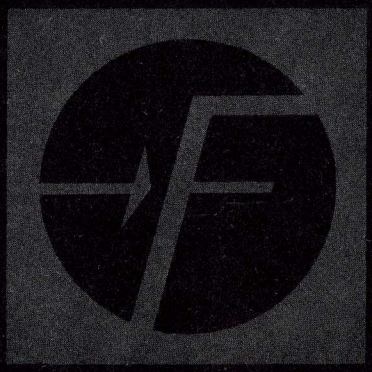


Figure 4

CREATIVE ENTERPRISE LITHO IN U.S.A.

FAIRCHILD SEMICONDUCTOR



545 WHISMAN ROAD

MOUNTAIN VIEW

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