TENTATIVE SPECIFICATIONS NOVEMBER 1962
REPLACES TENTATIVE SPECIFICATIONS, AUGUST 1962

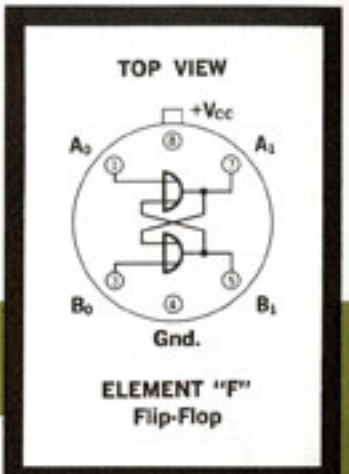
FAIRCHILD MICROLOGIC

µLF

FLIP-FLOP ELEMENT

The Fairchild Micrologic Flip-Flop is one of a set of compatible, integrated logic building blocks. The F element, as are all other elements, is manufactured using the Fairchild Planar Process, by which all the necessary transistors and resistors are diffused into a single silicon wafer.

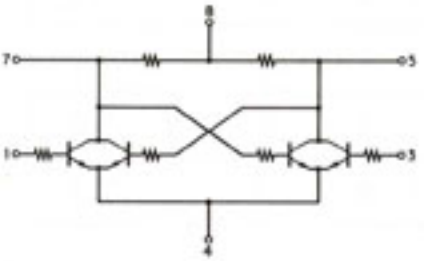
PLANAR: A Patented Fairchild Process.



ELEMENT "F"
Flip-Flop

ABSOLUTE MAXIMUM RATINGS (+25°C)

Maximum voltage applied to Pin 8	+15.0 volts
Maximum voltage applied to any input pin	±4.0 volts
Storage Temperature	−65°C to +200°C
Operating Temperature	−55°C to +125°C



PHYSICAL DIMENSIONS

NOTE: TO-47 and type 00 package options also available.

ELECTRICAL SPECIFICATIONS (+25°C ±2°C)

State	SYM.	TEST CONDITIONS [Note 1]	MIN.	TYP.	MAX.
	I_4	$V_1 = 0.760V \pm 2mV$, $V_5 = 0.790V \pm 10mV$ (Fan in = 2) [Note 2]			600µA
	I_3	$V_3 = 0.760V \pm 2mV$, $V_7 = 0.790V \pm 10mV$ (Fan in = 2) [Note 2]			600µA
1	I_5	$V_1 = V_5 = 0.760V \pm 2mV$, $V_3 = 0.550V \pm 2mV$	−2.7mA		
1	V_7	$V_1 = 0.760V \pm 2mV$, $V_3 = 0.550V \pm 2mV$			0.400V
2	I_7	$V_3 = V_7 = 0.760V \pm 2mV$, $V_1 = 0.550 \pm 2mV$	−2.7mA		
2	V_5	$V_3 = 0.760V \pm 2mV$, $V_1 = 0.550 \pm 2mV$			0.400V
3	V_5	$V_1 = V_5 = 0.760V \pm 2mV$			0.400V
3	V_7	$V_1 = V_3 = 0.760V \pm 2mV$			0.400V
4	I_5	$V_1 = V_5 = 0.760V \pm 2mV$, $V_3 = 0.550V \pm 2mV$	−2.7mA		
4	V_7	$V_5 = 0.760V \pm 2mV$			0.400V
5	I_7	$V_3 = V_7 = 0.760V \pm 2mV$, $V_1 = 0.550V \pm 2mV$	−2.7mA		
5	V_5	$V_7 = 0.760V \pm 2mV$			0.400V
	Tpd	Propagation delay time [Note 3]		25nsec	35nsec
	T_1	Leading edge delay time [Note 3]		24nsec	
	T_2	Leading edge rise time [Note 3]		20nsec	
	T_3	Trailing edge delay time [Note 3]		20nsec	
	T_4	Trailing edge fall time [Note 3]		22nsec	

(1) Voltages specified refer to the pin number to which the voltage is applied or measured. All currents are into the specified pin. Supply voltage is 3.00 volts ±.010v and pin 4 is ground for the complete test.
(2) Fan in conditions may best be simulated using the voltages as specified. This voltage is selected to force maximum input current requirements.
(3) Driven by and loaded by micrologic elements.

DESIGN INFORMATION

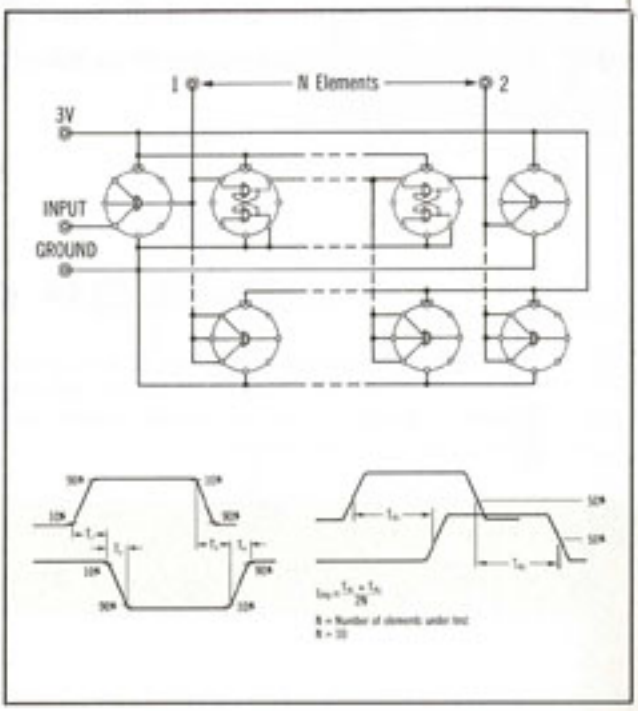
Supply Voltage	+3.00 volts ± 10%
Power Dissipation	30mW (typical)
Function:	

$$\overline{A_1} = A_0 + B_1$$
$$\overline{B_1} = B_0 + A_1$$

TRUTH TABLE						
	Bit-Time n		Bit-Time (n+1)			
State	A_1	B_1	A_0	B_0	A_1	B_1
1	x①	x	1	0	0	1
2	x	x	0	1	1	0
3	x	x	1	1	0	0
4	0	1	0	0	0	1
5	1	0	0	0	1	0

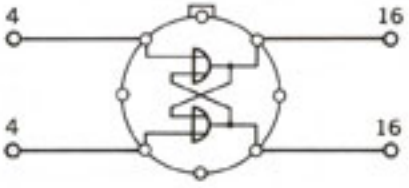
① Don't Care

PROPAGATION DELAY CIRCUIT

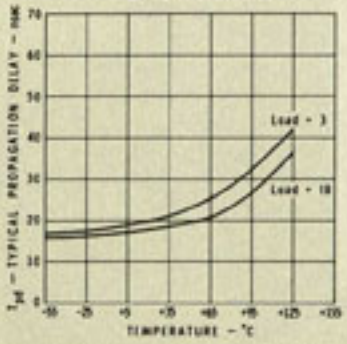


LOADING CHARACTERISTICS

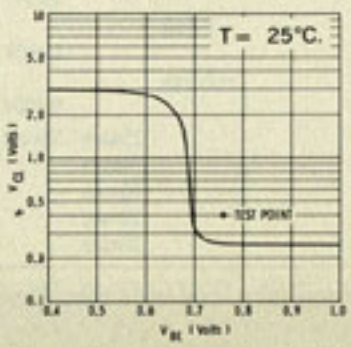
Each of the Micrologic elements has been assigned input load requirements and output driving capabilities. In the Flip-Flop this input load requirement is 4, which is identical with that of any other Micrologic element that has a fan-in of 2. Due to the current required by the internally cross-connected base in the Flip-Flop, the output drive capability must be reduced to 16. The load that may be driven from the Flip-Flop outputs could consist of any combination of elements whose summation of input loading does not exceed 16.



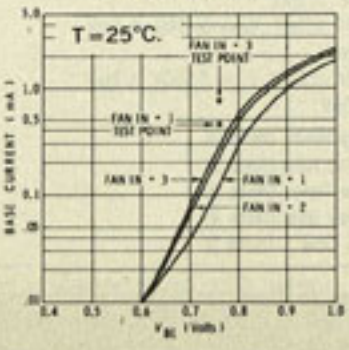
TYPICAL PROPAGATION DELAY VS. TEMPERATURE



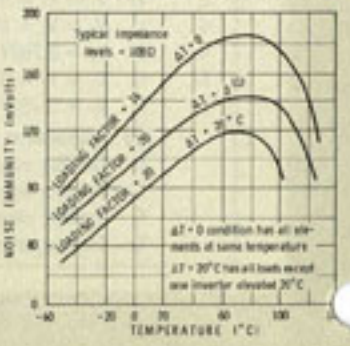
TYPICAL COLLECTOR VOLTAGE VS. BASE VOLTAGE



TYPICAL BASE CURRENT VS. BASE VOLTAGE



TYPICAL NOISE IMMUNITY



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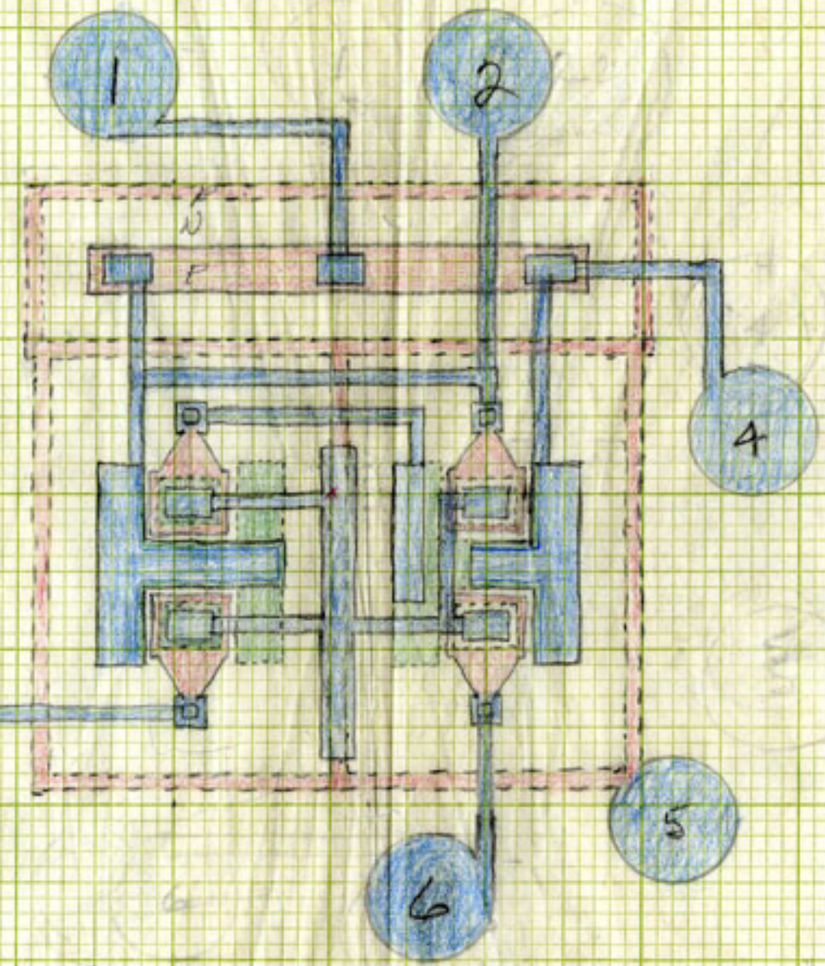
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